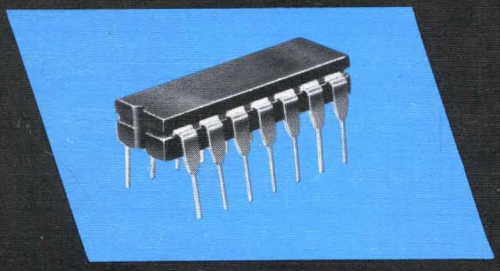
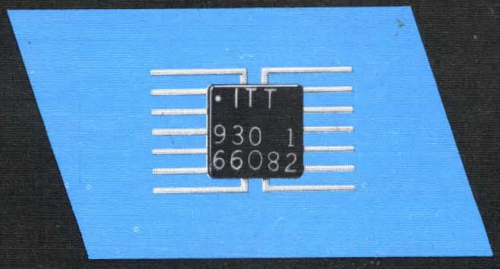
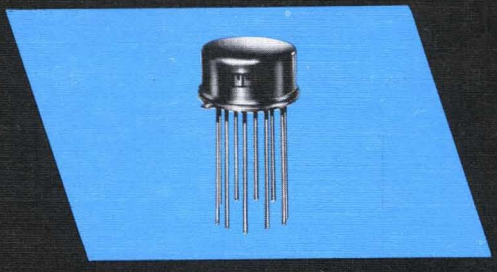
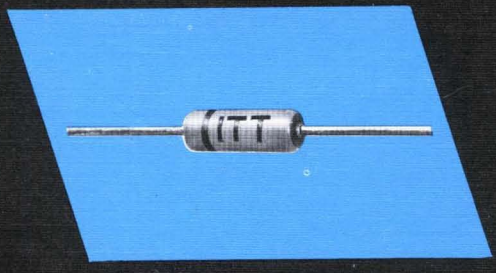
PRODUCT CATALOG 1974









SEMICONDUCTORS

ITT

WORLDWIDE

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30M474

Printed in U.S.A.

HIGH RELIABILITY PROCESSING

ITT Semiconductors maintains a broad capability for high reliability microcircuit screening.

Since its release, ITT has been a leader in qualifications to MIL-M-38510, the military specification creating "JAN IC's".

ITT's approach to these requirements differs from several "acronym" programs. We offer a full and complete "NO EXCEPTION" approach to each of the normally used military specifications.

Certain applications require various class levels of environmental screening and electrical test. The ITT approach to High Reliability provides a solid easily understood processing sequence. Each class level is geared exactly to the screening procedures outlined in Method 5004 of Military Standard 883 — **Test Methods and Procedures for Integrated Circuits.** The various screening class levels are outlined in the following section:

A — Mil STD 883 Method 5004 Class A Processing — Generally used in ultra high reliability applications.

B4 — Mil STD 883 Notice 4, Method 5004 Class B Processing — Used in many avionics systems requiring burned-in product and 100% DC temperature testing.

B2 — Same as B4 without 100% post burn-in temperature testing.

C — Mil STD 883 Method 5004 Class C Processing. Used in many ground-based systems. Includes complete environmental screening.

Note: These screening procedures are available in all ceramic and metal packages.

METHODS ARE MIL STD 883

SCREEN [Spec Paragraph]	CLASS "A" [Methods]	CLASS "B" [Methods]	CLASS "B4" [Methods]	CLASS "C" [Methods]
3.1.1 Precap Visual (100% inspection per specified method)	2010 A 1008	2010 B 1008	2010 B 1008	2010 B 1008
3.1.2 Stabilization Bake — 24 hrs. @ 150 C	1008	1008	1008	1008
3.1.3 Thermal Shock — 0 C to 100 C 15 cycles, 5 min, at extreme, 10 sec. transfer time. Liquid to liquid	1011	None	None	None
3.1.4 Temp-Cycle — minus 65 C to 150 C 10 cycles, 10 min. at extreme, 5 min. max. transfer time	1010 (may be replaced with thermal shock)	1010 (may be replaced with thermal shock)	1010 (may be replaced with thermal shock)	1010 (may be replaced with thermal shock)
3.1.5 Mechanical Shock	2002, "F" 1 Shock or 5 pulses at B (.5 msec. @ 1500 g)	None	None	None
3.1.6 Centrifuge	2001, E 30,000 g in Y_2, then Y_1 plane	2001, E 30,000 g in Y_1	2001, E 30,000 g in Y_1	2001, E 30,000 g in Y_1 plane
3.1.7 Hermeticity Fine Leak Gross Leak	Method 1014 Radioflo Bubble Test	Radioflo Bubble Test	Radioflo Bubble Test	Radioflo Bubble Test
3.1.8 Critical Elect. Para. (Go-No-Go or Datalog)	Per Electrical Spec.	Per Electrical Spec.	Per Electrical Spec.	None

METHODS ARE MIL STD 883

SCREEN [Spec Paragraph]	CLASS "A" [Methods]	CLASS "B" [Methods]	CLASS "B4" [Methods]	CLASS "C" [Methods]
3.1.9 Burn-In	1015 125 C for 240 hours	1015 125 C for 168 hours	1015 125 C for 168 hours	None
3.1.10 Critical Elect. Para. (Go-No-Go or Datalog)	Per Elect. Spec.	None	None	None
3.1.11 HTRB	72 hrs @ 150 C	None	None	None
3.1.12 Final Elect. Test				
(a) D.C. @ 25 C	Per Spec.	Per Spec.	Per Spec.	Per Spec.
(b) D.C. @ Hi/Low Temp.	Per Spec.	None	Per Spec.	None
(c) A.C. Para. @ 25 C	Per Spec.	Per Spec.	Per Spec.	None
(d) Functional Tests	Per Spec.	Per Spec.	Per Spec.	Per Spec.
3.1.13 Radiographic Insp.	Method 2012	None	None	None
3.1.14 Qualification and Quality Conformance Procedures	5005	5005	5005	5005
3.1.15 External Visual	2009	2009	2009	2009

Optional Additions.

Class A - Scanning Electron Microscope Wafer Inspection

All Classes - Read and Record Data (DC at Temperature) With Delta Calculations as Required

All Classes - Switching Measurements at Temperature Extremes with Data

All Classes - Lot Conformance Testing (Life Tests) and Generic Reliability Data.

Classes A & B - Elevated Temperature Burn-in.

MIL 38510 — JAN MICROCIRCUITS

ITT also offers a broad line of fully qualified MIL-38510 microcircuits. At this writing, 20 devices are fully qualified and qualification plans are in process for an additional 21 types. The rigorous life qualification test are conducted in full compliance to Method 5005 of MIL 883 and are available on all ceramic and metal can integrated circuits.

Through QPL 38510-11 dated 16 July, 1973, ITT qualification status is as follows:

1] Full Qualified Part I

5400	5405	5450	5472
5401	5410	5451	5473
5402	5420	5453	5474
5403	5430	5454	5486
5404	5440	5470	54H30

TOTAL 20

Packages

A - 1/4 x 1/4 Flatpack
C - 14 pin Dip

Lead Finishes

A Package - A - Solder Dipped
B - Tin Plated
C - Gold
C Package - B - Tin Plated
C - Gold

2] Interim Qualification Part II

5482	5407	54H72	54H10*
5483	5417	54H73	54H00*
5406	5442	54H30*	54H04*
5416	54121	54H20*	

TOTAL 15

These qualifications are rigorously controlled by the Defense Electronics Supply Center, Dayton, Ohio.

* Flat Pack Only

ORDERING INFORMATION A cross reference guide for ordering of JAN microcircuits is shown below:

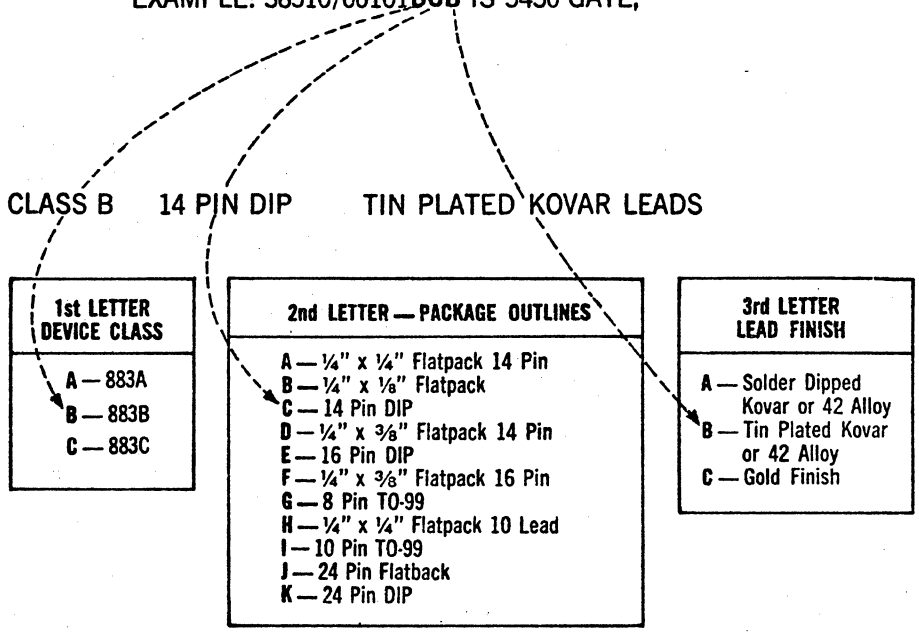
Jan No.	Part No.	Jan No.	Part No.
00101	5430	01302	5493
00102	5420	01303	54160
00103	5410	01304	54163
00104	5400	01305	54162
00105	5404	01306	54161
00106	5412	01401	54150
00107	5401	01402	9312
00108	5405	01403	54153
00109	5403	01404	9309
00201	5472	01405	9322
00202	5473	02001	54L30
00203	54107	02002	54L20
00204	5476	02003	54L10
00205	5474	02004	54L00
00206	5470	02005	54L04
00207	5479	02006	54L03
00301	5440	02101	54L71
00302	5437	02102	54L72
00303	5438	02103	54L73
00401	5402	02104	54L78
00402	5423	02105	54L74
00403	5425	02201	54H72
00404	5427	02202	54H73
00501	5450	02203	54H74
00502	5451	02301	54H30
00503	5453	02302	54H20
00504	5454	02303	54H10
00601	5482	02304	54H00
00602	5483	02305	54H04
00701	5486	02306	54H01
00801	5406	02307	54H22
00802	5416	02401	54H40
00803	5407	02601	54L86
00804	5417	02701	54L02
00901	5495	02801	54L95
00902	5496	02802	54L164
00903	54164	02901	54L42
00904	54165	02902	54L43
01001	5442	02903	54L44
01002	5443	02904	54L46
01003	5444	02905	54L47
01004	5445	05301	4007A
01005	54145	05302	4019A
00106	5446	10101	741
01007	5447	10102	747
01008	5448	10103	LM101A
01009	5449	10104	LM108A
01101	54181	10201	723
01201	54121	10301	710
01202	54122	10302	711
01203	43123	10303	LM106
01301	5492	10202	MCM5304

Part No.	Jan No.	Part No.	Jan No.
710	10301	54L47	02905
711	10302	5448	01008
723	10201	5449	01009
741	10101	5450	00501
747	10102	5451	00502
4007A	05301	5453	00503
4019A	05302	5454	00504
5400	00104	5470	00206
54H00	02304	54L71	02101
54L00	02004	5472	00201
5401	00107	54H72	02201
54H01	02306	54L72	02102
5402	00401	5473	00202
54L02	02701	54H73	02202
5403	00109	54L73	02103
54L03	02006	5474	00205
5404	00105	54H74	02203
54H04	02305	54L74	02105
54L04	02005	5476	00204
5405	00108	54L78	02104
5406	00801	5479	00207
5407	00803	5482	00601
5410	00103	5483	00602
54H10	02303	5486	00701
54L10	02003	54L86	02601
5412	00106	5492	01301
5416	00802	5493	01302
5417	00804	5495	00901
5420	00102	54L95	02801
54H20	02302	5496	00902
54L20	02002	9309	01404
54H22	02307	9312	01402
5423	00402	9322	01405
5425	00403	54107	00203
5427	00404	54121	01201
5430	00101	54122	01202
54H30	02301	54123	01203
54L30	02001	54145	01005
5437	00302	54150	01401
5438	00303	54153	01403
5440	00301	54160	01303
54H40	02401	54161	01306
5442	01001	54162	01305
54L42	02901	54163	01304
5443	01002	54164	00903
54L43	02902	54L164	02802
5444	01003	54165	00904
54L44	02903	54181	01101
5445	01004	LM101A	10103
5446	01006	LM106	10303
54L46	02904	LM108A	10104
5447	01007	MCM5304	20102

SUFFIX DEFINITIONS

ALL MIL-M38510 DEVICES MUST HAVE A THREE LETTER SUFFIX AFTER THEIR NUMBER

EXAMPLE: 38510/00101**BCB** IS 5430 GATE,



The JAN number is a complete processing and electrical description of the part odered.

All full Jan parts are completely assembled, fabricated and tested in the United States.

SOURCE CONTROL DRAWINGS

ITT maintains a completely staffed specification review group for analysis of customer controlled specifications.

In many cases, the customer may find one of the standard ITT Hi-Rel processing sequences exactly equivalent to his needs and his only requirement is to specify the final electrical specification. Since ITT performs with "NO Exception" to the standard military screening documents, the need for exact selection of particular processing is relieved. In addition, test plans for exact conformance to customer drawings are generated if required and as a standard practice, submitted to the customer for final approval.

DELIVERY

The West Palm Beach factory of ITT Semiconductors is dedicated to manfacture of High-reliability circuits. A complement in excess of 100,000 burn-in sockets is maintained. In addition, if a contractual or specification limitation does not exist our offshore facilities are completely equipped for all Class C assembly and screening techniques. All class B final work is done in the U.S.

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2N5220	105
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INTEGRATED CIRCUITS DICE AND WAFERS

All ITT integrated circuits are available both in wafer and in chip form. Since the completed individual encapsulated product is capable of being more extensively and thoroughly tested than the wafer, these specifications are limited to the capability of the chip and the attendant testing equipment.

USE

DTL and Linear circuits are normally supplied with plain backing. Gold backing can be furnished upon special request. All other circuits are supplied with gold backing. Recommended die attach temperature is 420°C for either type of backing. A 98% gold, 2% silicon preform is recommended for die attach with all plain-backed chips. One mil aluminum wire, ultrasonically bonded to the pads, is recommended for connecting the chip to the circuit.

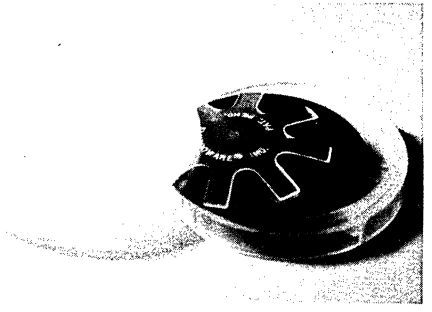
PACKAGING FOR SHIPMENT

Wafers will be shipped in the plastic package shown. Chips will be packaged in carriers as indicated.

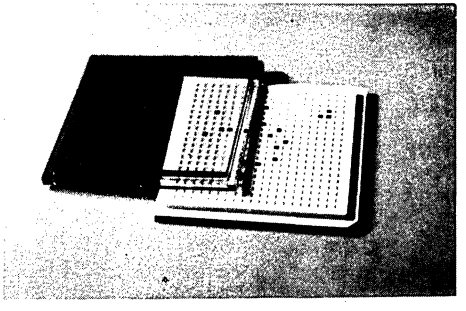
IDENTIFICATION

All integrated circuit dice will be identified by the appropriate three or four-digit code, together with the individual suffix number indicating the temperature range.

For example, a 930 limited-temperature range chip would be a "930-5." A 930 full-temperature range chip would be a "930-1."



I. C. WAFER PACKAGE



CHIP PACKAGE

MIL AND HI-REL SEMICONDUCTORS

Virtually all ITT Semiconductors are available with hi-rel processing. IC's, for example, can be processed for any portions of, or all of, MIL-STD-883 and MIL38510. Many diodes and transistors are available as JAN, JAN/TX, or MIL types.

Whenever you need hi-rel semiconductors, check ITT. Your local representative can give up-to-date information on availability, price, etc.

Type	Description
ITT 7400	Quad 2 i/p NAND
ITT 7401	Quad 2 i/p NAND (open collector 5.5V rating)
ITT 7402	Quad 2 i/p NOR
ITT 7403	Quad 2 i/p NAND (open collector 5.5V rating)
ITT 7404	Hex inverter
ITT 7405	Hex inverter (open collector 5.5V rating)
ITT 7406	Hex inverter buffer/driver (open collector 30 V rating)
ITT 7407	Hex buffer/driver (open-collector 30 V rating)
ITT 7408	Quad 2 i/p AND
ITT 7409	Quad 2 i/p AND (open-collector)
ITT 7410	Triple 3 i/p NAND
ITT 7411	Triple 3 i/p AND
ITT 7412	Triple 3 i/p NAND (open-collector 5V rating)
ITT 7413	Dual 4 i/p Schmitt Trigger
ITT 7416	Hex inverter buffer/driver (open-collector 15V rating)
ITT 7417	Hex buffer/driver (open-collector 15V rating)
ITT 7420	Dual 4 i/p NAND
ITT 7421	Dual 4 i/p AND
ITT 7425	Dual 4 i/p NOR (with strobe)
ITT 7426	Quad 2 i/p high voltage interface NAND (open collector)
ITT 7428	Quad 2 i/p NOR buffer
ITT 7430	8 i/p NAND
ITT 7432	Quad 2 i/p OR
ITT 7433	Quad 2 i/p NOR buffer (open collector 5.5V rating)
ITT 7437	Quad 2 i/p NAND buffer
ITT 7438	Quad 2 i/p NAND buffer (open collector 5.5V rating)
ITT 7440	Dual 4 i/p NAND buffer
ITT 7442	B.C.D. to decimal decoder
ITT 7443	Excess 3 to decimal decoder
ITT 7444	Excess 3 gray to decimal decoder
ITT 7445	B.C.D. to decimal decoder (open collector 30V rating)
ITT 7446A	BCD to seven segment Decoder/driver (open collector 30V rating)
ITT 7447A	BCD to seven segment Decoder/driver (open collector 15V rating)
ITT 7448	BCD to seven segment decoder/Driver (2k pullup)
ITT 7450	Expandable dual 2 wide, 2 i/p A.O.I.
ITT 7451	Dual 2 wide, 2 i/p A.O.I.
ITT 7453	Expandable 4 wide, 2 i/p A.O.I.
ITT 7454	4 wide, 2 i/p A.O.I.
ITT 7460	Quad 2 i/p expander
ITT 7470	Edge-triggered J-K flip-flop
ITT 7472	J-K master-slave flip-flop
ITT 7473	Dual J-K master-slave flip-flop
ITT 7474	Dual D-type edge-triggered flip-flop
ITT 7475	Quad bistable latch
ITT 7476	Dual J-K master-slave flip-flop with preset and clear
ITT 7480	Gated full adder
ITT 7482	2-bit full adder
ITT 7483	4-bit full adder
ITT 7486	Quad 2 i/p exclusive-OR
ITT 7490	Decade counter
ITT 7491A	8-bit shift register
ITT 7492	Divide by 12 counter
ITT 7493	4-bit binary counter
ITT 7494	5-bit shift register
ITT 7495A	4-bit shift register (reversible)
ITT 7496	4-bit shift register
ITT 74104	Gated J-K master-slave flip-flop
ITT 74105	Gated J-K master-slave flip-flop
ITT 74107	Dual J-K master-slave flip-flop
ITT 74109	Dual J-K positive-edge-triggered flip-flop with preset and clear
ITT 74118	Hex set-reset latch
ITT 74121	Monostable multivibrator
ITT 74122	Retriggerable monostable multivibrator with clear
ITT 74123	Dual retriggerable monostable multivibrator with clear
ITT 74124	Universal pulse generator
ITT 74130	Quad 2 i/p AND buffer (open collector 30V rating)
ITT 74131	Quad 2 i/p AND buffer (open collector 15V rating)
ITT 74135	Quad 2 i/p positive NAND schmitt trigger
ITT 74137	Hex inverter Schmitt Trigger
ITT 74138	Quad 2 i/p OR buffer (open collector 30V rating)
ITT 74139	Quad 2 i/p OR buffer (open collector 15V rating)
ITT 74141	B.C.D. to decimal decoder/driver
ITT 74145	B.C.D. to decimal decoder (open-collector 15V rating)
ITT 74150	16-bit data selector/multiplexer
ITT 74151	8-bit data selector/multiplexer
ITT 74153	Dual 4-line-to-1-line data selector/multiplexer
ITT 74154	4-line-to-16-line decoder/demultiplexer

TTL NUMERICAL INDEX

Type	Description
ITT 74155	Dual 2 to 4 line decoder/demultiplexer
ITT 74156	Dual 2 to 4 line decoder/demultiplexer (o/c 5-5V rating)
ITT 74157	Quad 2-line-to-1-line data selector/multiplexer
ITT 74160	Synchronous 4-bit counter
ITT 74161	Synchronous binary up counter
ITT 74162	Fully synchronous counter
ITT 74163	Fully synchronous counter
ITT 74164	8-bit parallel-out serial shift register
ITT 74165	Parallel-load 8-bit shift register
ITT 74174	Hex D-type flip-flop
ITT 74175	Quad D-type flip-flop
ITT 74180	8-bit parity generator/checker
ITT 74181	Arithmetic logic unit / function generator
ITT 74182	Look-ahead carry generator
ITT 74190	Synchronous up/down counter with down/up mode control
ITT 74191	Synchronous up/down counter with down/up mode control
ITT 74192	Synchronous BCD-up/down counter
ITT 74193	Synchronous binary 4-bit up/down counter
ITT 74194	4-bit bidirectional universal shift register
ITT 74195	4-bit parallel-access shift register
ITT 74H00	Quad 2 i/p NAND
ITT 74H01	Quad 2 i/p NAND (open-collector output)
ITT 74H04	Hex inverter
ITT 74H05	Hex inverter with open-collector output
ITT 74H10	Triple 3 i/p NAND
ITT 74H11	Triple 3 i/p AND
ITT 74H20	Dual 4 i/p NAND
ITT 74H21	Dual 4 i/p AND
ITT 74H30	8-input NAND
ITT 74H40	Dual 4 i/p NAND
ITT 74H50	Dual 2-wide 2 i/p and-or-invert gate (one gate expandable)
ITT 74H51	Dual 2-wide 2 i/p and-or-invert gate
ITT 74H53	Expandable 4-wide and-or-invert gate
ITT 74H54	4-wide and-or-invert gate
ITT 74H60	Dual 4 i/p expander
ITT 74H72	and-gated J-K master-slave flip-flops with preset and clear
ITT 74H73	Dual J-K flip-flops with clear
ITT 74H74	Dual d-type positive-edge-triggered flip-flop with preset and clear
ITT 74H76	Dual J-K flip-flops with preset and clear
ITT 9000	J-K Flip-flop
ITT 9001	J-K Flip-flop
ITT 9002	Quad 2 i/p NAND gate
ITT 9003	Triple 3 i/p NAND gate
ITT 9004	Dual 4 i/p NAND gate
ITT 9005	AND-OR-invert gate, dual 2-wide, 2 i/p, expandable
ITT 9006	Dual 4 i/p extender
ITT 9007	Single 8 i/p NAND gate
ITT 9008	And-or-invert gate, expandable 4 wide, 2 i/p
ITT 9009	Dual 4 i/p Buffer
ITT 9016	Hex inverter
ITT 9020	Dual J-K Flip flop
ITT 9022	Dual J-K Flip flop
ITT 9300	4-Bit Shift Register
ITT 9301	One-of-Ten Decoder
ITT 9304	Dual Full Adder
ITT 9308	Dual 4-Bit Latch
ITT 9309	Dual 5-Input Multiplexer
ITT 9311	One-of-16 Decoder
ITT 9312	8-Input Multiplexer
ITT 9316	Hexidecimal Counter
ITT 9322	Quad. 2-Input Multiplexer
ITT 9328	Dual 8-Bit Shift Register
ITT 9601	Retriggerable One Shot
ITT 9602	Dual Retriggerable One Shot

Positive-NAND Gates And Inverters With Totem-Pole Outputs

Function	Type
Hex Inverters	74H04
	7404
	9016
Quad 2 i/p NAND	74H00
	7400
	9002
Triple 3 i/p NAND	74H10
	7410
	9003
Dual 4 i/p NAND	74H20
	7420
	9004
8 i/p NAND	74H30
	7430
	9007

Positive-NAND Gates And Inverters With Open-Collector Outputs

Hex Inverters	74H05
	7405
	9017
Quad 2 i/p NAND	74H01
	7401
	7403
	9012
Triple 3 i/p NAND	7412

Positive-NOR Gates With Totem-Pole Outputs

Quad 2 i/p NOR	7402
Dual 4 i/p NOR with strobe	7425

Positive-AND Gates With Totem-Pole Outputs

Quad 2 i/p AND	7408
Triple 3 i/p AND	74H11
Dual 4 i/p AND	74H21

Positive-AND Gates With Open-Collector Outputs

Quad 2 i/p AND	7409

Schmitt-Trigger Positive-NAND Gates And Inverters With Totem-Pole Outputs

Hex Schmitt Trigger Inverters	74137
Quad 2 i/p NAND Schmitt Triggers	74135
Dual 4 i/p NAND Schmitt Triggers	7413

Buffers/Clock Drivers With Totem-Pole Outputs

Quad 2 i/p NOR	7428
Quad 2 i/p NAND	7437
Dual 4 i/p NAND	74H40
	7440
	9009

Buffer And Interface Gates With Open-Collector Outputs

Function	Type
Hex Buffers/Drivers	7407
	7417
Hex Inverter Buffers/Drivers	7406
	7416
Quad 2 i/p NAND	7426
	7438
Quad 2 i/p NOR	8433
Quad 2 i/p AND	74130
	74131
Quad 2 i/p OR	74138
	74139

Positive-OR Gates With Totem-Pole Outputs

Quad 2 i/p OR	7432

AND-OR Invert Gates With Totem-Pole Outputs

4-Wide 2-2-3-2-input	74H54
4-Wide 2 i/p	7454
Dual 2-Wide 2 i/p	74H51
	7451

Expandable Gates

4-Wide AND-OR invert	74H53
	7453
	9008
Dual 2-Wide AND-OR invert	74H50
	7450
	9005

Expanders

Dual 4 i/p	7460
	74H60
	9006

Flip-Flops

Dual J-K edge-triggered	74109
	9024
Single J-K edge-triggered	7470
Dual pulse-triggered	74H73
	7473
	74107
	74H76
	7476
	9020
	9022
Single pulse-triggered	74H72
	7472
Gated J-K Master Slave	74104
	74105
	9000
	9001

D-Type Flip-Flops

Dual	7474, 74H74

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Monostable Multivibrators With Schmitt-Trigger Inputs

Function	Type
Single	74121

Retriggerable Monostable Multivibrators

Single	74122
	9601
Dual	74123
	9602

S-R Latches

Hex S-R	74118

Adders

Single 1-bit gated full	7480
Single 2-bit full	7482
4-bit arithmetic logic units/ function generators	74181
Look-ahead carry generators	74182
Dual 1-bit full	9304

Parity Generators/Checkers

8-bit odd/even	74180

Other Arithmetic Operators

Quad 2 i/p exclusive-or gates with totem-pole outputs	7486

Shift Registers

4-bit parallel-in parallel-out (bidirectional)	74194
5-bit parallel-in, parallel-out	7496
4-bit parallel-in, parallel-out	74195
	9300
	7495A
Serial-in, parallel-out, 8-bit	74164
8-bit parallel-in, serial-out	74165
4-bit parallel-in, serial-out	7494
8-bit serial-in, serial-out	7491A
Dual 8 Bit serial in - serial out	9328

Other Registers

Hex D-type registers	74174
Quad D-type registers	74175

Synchronous Counters-Positive-Edge Triggered

Decade	74162
	74160
Decade up/down	74192
	74190
4-bit binary	74163
	74161
	74193
	74191
	9316

Pulse Generators

Function	Type
Universal pulse generator	74124

Latches

D_G (clocked) latches	7475
Dual 4-Bit	9308

Decoders/Demultiplexers

4-line-to-16-line	74154
	9311
Dual 2-line-to-4-line	74155
	74156
4-line to 10-line	7442
	7443
	7444
	9301

Open-Collector Display Decoders/Drivers

BCD-to-decimal	7445
	74145
	74141
BCD-to-seven-segment	7446A
	7447A
	7448

Data Selectors/Multiplexers

Dual 4-bit	9309
	74153
8-bit	9312
	74151
Quad 2-bit	9322
	74157
16-bit	74150

Asynchronous Counters

Decade	7490
Divide by 12	7492
4-bit Binary	7493

This series offers a wide range of digital integrated circuit devices from simple NAND gates to large complex functions. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges.

Military range, 54 series	−15°C to 125°C
Industrial range, 74 series	0°C to 75°C

All devices operate over a frequency range between D.C. and typically 20 MHz, and are fully compatible with all 54/74 series TTL and 930 series DTL.

Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e. high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

FEATURES

- **High speed**—typical propagation delay (gate) of 9 ns.
- **Guaranteed noise margin**—greater than 400 mV.
- **Low power dissipation**—10 mW per gate at 50% duty cycle.
- **Worst case fan-out of 10.**
- **Low output impedance.**
- **Logic levels guaranteed over range of supply voltage and operating temperature.**
- **Wide range of functions**—many SSI and MSI functions.
- **Compatible with other DTL, TTL logic series.**

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease of reading, the data only refers to the ITT7400 series family but it is equally applicable to the ITT5400 series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but <0.8 V
Logical '1' = High voltage; typically 3.3 V but >2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES (except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74 series	4.75	5.25	V
54 series	4.5	5.5	V
Operating temperature:			
74 series	0	75	°C
54 series	−55	125	°C

D.C. noise margin typically greater than 1 V.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1)	7 V
Input voltage	5.5 V
Voltage between inputs	5.5 V
Continuous input current	−10 mA
Standard output voltage	−0.5 to 5.5 V
Storage temperature!	−65°C to 150°C

Note 1
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS (limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

PARAMETER	LIMIT (Note 8)					CONDITIONS
	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	V_{OL} <0.4 V or V_{OH}> 2.4 V (Note 1)
V_{IL}			0.8	V	Min.	V_{OL} <0.4 V or V_{OH}> 2.4 V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL} = 16 mA, V_{IH} = 2 V or V_{IL} = 0.8 V (Note 3)
V_{OL} (buffer output) V_{OH}	2.4	3.3		V	Min.	V_{IL} = 0.8 V or V_{OH} = 2.0 V (Note 4)
I_{CEX} open collector only			250	uA	Min.	V_{IL} = 0.8 V, V_{IH} = 2 V, V_{OUT} = max. o/p voltage rating
$-I_F$		1.0	1.6	mA	Max.	V_F = 0.4 V (Note 5)
I_R			40	uA	Max.	V_R = 2.4 V, input loading-1 unit load (Note 6)
I_R			1.0	mA	Max.	V_R = 5.5 V irrespective of input loading
$-I_{SC}$						
54 series	20		55	mA	Max.	V_{OUT} = 0 V (Note 7)
74 series	18		55	mA	Max.	V_{IH} = 2.0 V or V_{IL} = 0.8 V; apply according to logic function

Where characteristics for devices differ from the above table these are shown in the data sheets.

Note 1
Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, V_{OL} <0.4 V applies, and for flip-flops, shift registers, counters, decoders, etc. either V_{OL} <0.4 V or V_{OH} >2.4 V applies at each output. Output conditions do not apply for 7486, 7460, 7445, 74145, and 7441A. This parameter does not apply for 7413 and 74121 because of the Schmitt trigger inputs.

Note 2
Conditions at outputs dependent on the the truth table of the device, for example, for gates and inverters V_{OH} >2.4 V. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3
Conditions V_{IH} and V_{IL} depend on device truth table. Limits for 7441A, 7445 and 74145 are shown on the appropriate data sheets.

Note 4
This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table.

I_{OH} = −400 uA for devices with Fan-out=10; I_{OH} = −800 uA for devices with Fan-out=20; I_{OH} = −1.2 mA for devices with Fan-out=30, etc.

Note 5
Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6
For other inputs at 0 V for 7472, 7473, 7476, 74107. For 7470 all other inputs at 0 V except J and K which are at 4.5 V. For 7474 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7
Maximum limit = 57 mA for devices with internal feedback connections, (e.g. flip-flops and some complex devices). For 7400 series simple NAND gates not more than two outputs may be shorted at any time. For all other devices and for all 5400 series not more than one output to be shorted at any time. Open collector devices; no parameter for I_{SC}.

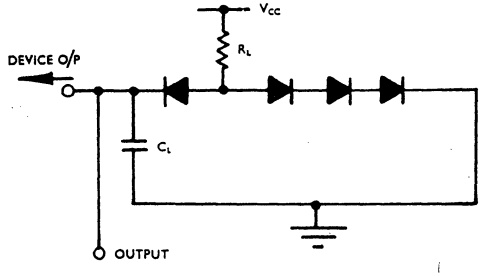
Note 8
Typical limits are at ambient temperature.
$T_A = 25°C$ and $V_{CC} = 5$ V.

A.C. TESTS

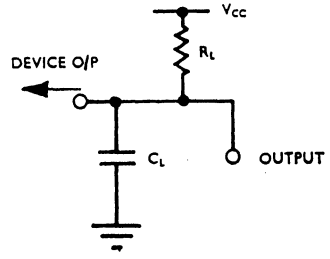
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:



ORDERING CODE FOR TTL CIRCUITS

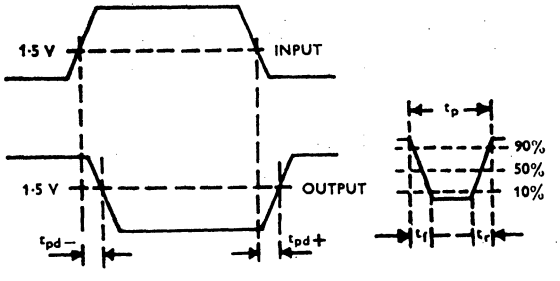
Operating Temperature Range
5400 series −55 to +125°C
7400 series 0 to +70°C

Package (add)
B for Flat Pack
J for Ceramic Dual In-Line
N for Plastic Dual In-Line

Example:
ITT7400J
is 0°C to +70°C Range in
Ceramic Dual In-Line Package

Notes
1. Diodes are type 1N4148.
2. The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.
3. The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: V_{OUT} = 3.5 V; Rise time, tr, = Fall time, t_f, = less than 15 ns; Zo = 50 O; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, t_p = 500 ns.

Waveforms



1. HIGH LOGIC STATE '1' (ON STATE)

The NAND gate has two stable operating states. These are illustrated in Figs. 1A and 1B.

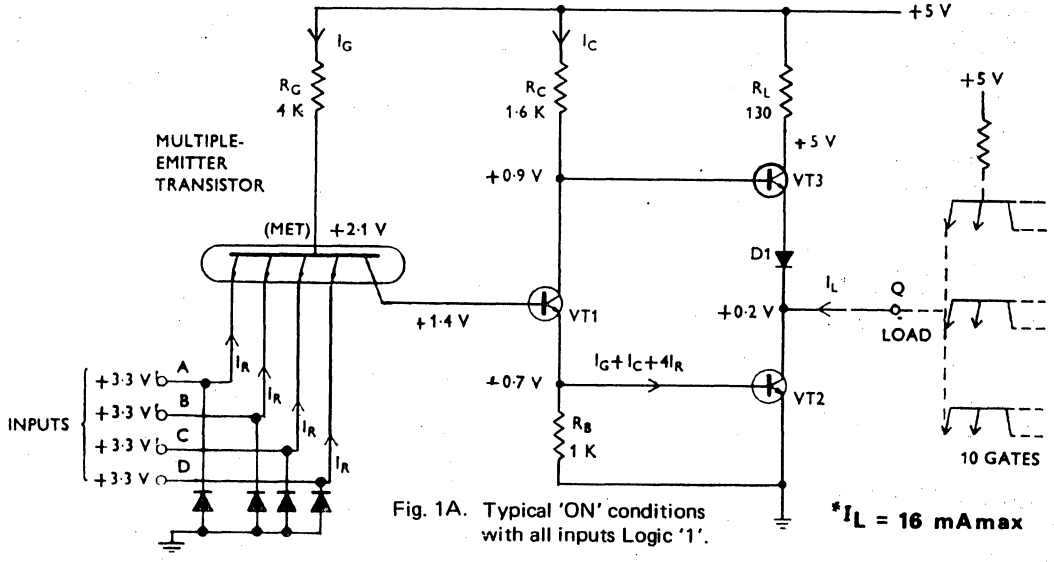


Fig. 1A. Typical 'ON' conditions with all inputs Logic '1'.

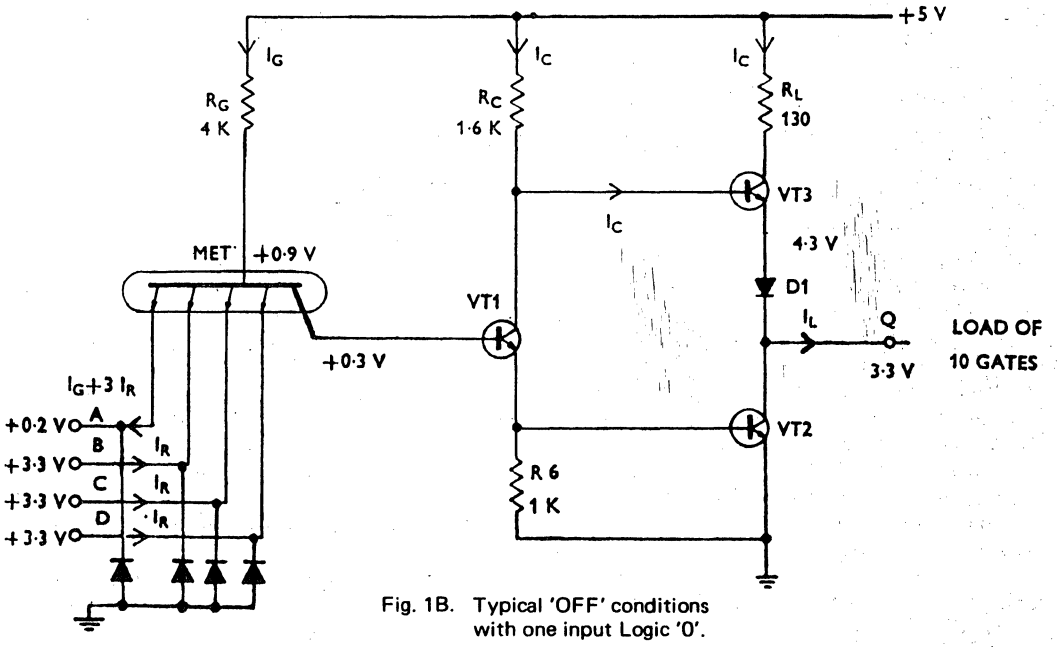
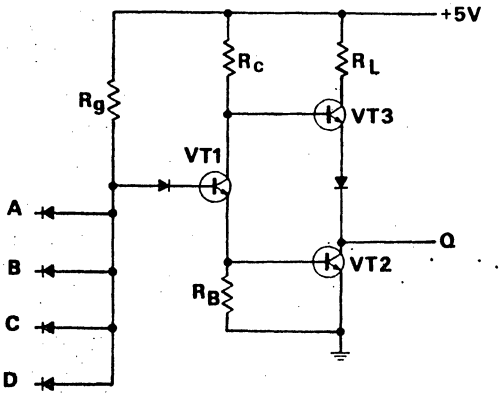


Fig. 1B. Typical 'OFF' conditions with one input Logic '0'.

The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_g into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

2. LOW OR OFF STATE

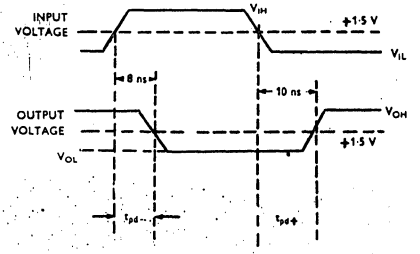
The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about +1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.

Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.

NOISE IMMUNITY

The noise immunity of the TTL gate is typically greater than 1 volt and is guaranteed 0.4 V minimum under worst case conditions for temperature and loading tolerances. The noise immunity is derived from the difference between extreme limits of input voltage and the voltage required to ensure the change of a logic state. This is illustrated by the transfer characteristic shown in Fig. 4.

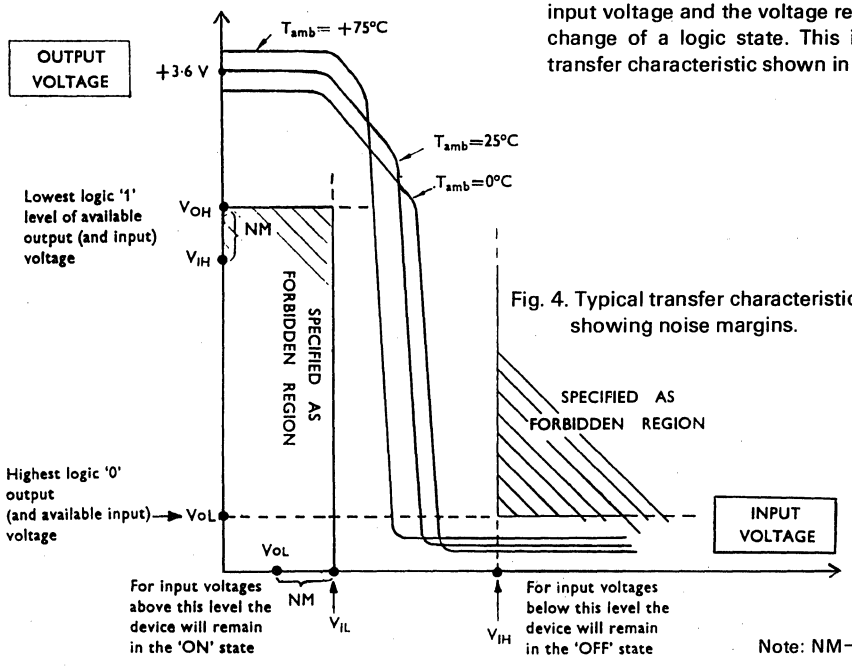


Fig. 4. Typical transfer characteristic showing noise margins.

Note: NM—Noise margin

BASIC RULES FOR THE USE OF TTL DEVICES

1. Spare inputs should be connected to used inputs if the fan-out permits. Otherwise connected to the V_{CC} power line via a resistor of value 1 K ohm or greater. This is particularly important for the 'preset' and 'clear' asynchronous inputs.
2. Gates from the same package may be paralleled where necessary for better driving capability.
3. Interconnection lengths of 12 inches or less (capacitance of about 50 pF) are unlikely to give ringing problems; lengths up to 24 inches are possible with good ground arrangements. Greater length will probably require line driving precautions (see separate Application Note)
4. Wired-OR' can be performed at the output terminals of open-collector networks however a speed penalty is incurred by the introduction of a resistive pull-up.
5. In calculating system speeds, due allowance should be made for the maximum set-up and minimum clock pulse width times on flip-flops, as well as the propagation delays of the elements used.
6. If relays are driven from TTL circuitry, care must be taken to ensure that the load connection wires to the relay contacts do not introduce noise into the logic system. This can be done by allowing these wires only to enter the logic system enclosure at a point close to the relay contacts, or in extreme cases by also shielding the relay.

7. Similarly external inputs should be brought on to the printed circuit connections at right angles to the other wiring, the printed circuit itself being laid out to ensure least coupling between inputs and other connections.
8. If system speed is high, allowance should be made when calculating power supply requirements for the increased network supply currents due to current spiking and line driving. An allowance at 10 MHz of 15% for spiking and up to 0.5 mA per each gate node for the line driving will be adequate for this.
9. Decouple every 10 gates or their equivalent in MSI functions with 0.01 uF to 0.1 uF capacitors of R.F. rating.

In conclusion, a careful perusal of the data sheet together with the points mentioned above, will help in achieving a trouble free logic design at the first attempt.

DRIVING DTL LOGIC FROM TTL DEVICES

When driving ITT930 series DTL from 74/5400 series TTL the full fan-out of the TTL is available

DRIVING TTL LOGIC FROM DTL DEVICES

Driving ITT7400 series TTL from ITT930 series DTL necessitates a reduction of the full fan-out from 8 to 3 for standard gates and from 25 to 20 for buffers. Increased fan-out can be achieved with standard DTL gates by using an additional pull-up resistor.

SYMBOLS AND THEIR DEFINITIONS

C_L	Load capacitor in switching test circuit (includes probe and jig capacitance).
Fan-out	Number of unit loads an output can drive.
f_{max}	Maximum clock frequency.
I_{CCH}	Supply current for highest dissipation logic state.
I_{CCL}	Supply current for lowest dissipation logic state.
I_F	Input forward current.
I_R	Input reverse current.
I_{SC}	Output short circuit current.
I_{CEX}	Output leakage current.
I_{OL}	Low state output current.
I_{OH}	High state output current.
I_{CC}	Supply current.
$I_{IN}+$	Input current at V_T+
$I_{IN}-$	Input current at V_T-
P_{dyn}	Dynamic power dissipation.
R_L	Load resistor in switching test circuit.
T_A	Ambient temperature.
t_h	Input hold time.
t_h+	Logical '1' hold time.
t_h-	Logical '0' hold time.
t_{cp}	Clock pulse width.
t_p	Preset or clear pulse width.
t_{po}	Output pulse width.
$t_{pd}+$	Propagation delay to logical '1' on output.
$t_{pd}-$	Propagation delay to logical '0' on output.
t_n	State of output (or input) before the active edge of the clock pulse.
t_n+1	State of output (or input) after the active edge of the clock pulse.
t_{min}	Minimum width trigger pulse.
$t_{sp}+$	Logical '1' input set up time.
$t_{sp}-$	Logical '0' input set up time.
V_{CC}	Supply voltage.
V_H	Hysteresis voltage.
V_{IH}	Input high voltage to ensure V_{OL} (or V_{OH})*
V_{IL}	Input low voltage to ensure V_{OH} (or V_{OL})*
V_{OL}	Output low voltage.
V_{OH}	Output high voltage.
$V_{OH(M)}$	Output breakdown voltage of open collector device.
V_{IN}	Voltage at an input.
V_{OUT}	Voltage at an output.
V_T+	Positive edge threshold voltage.
V_T-	Negative edge threshold voltage.
WIRED-OR	The commoning of open collector outputs with a pull-up resistor to perform the AND function.

*Output level dependent on device logic as found from truth table.

APPLICATION DATA FOR OPEN COLLECTOR DEVICES

Combined Fan-Out and Wire-OR Capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R), may be paralleled with other similar TTL gates to perform the wire-OR function, and simultaneously, will drive from one to nine TTL loads. When no other open-collector gates are paralleled, this gate may be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and I_{out} current (through paralleled outputs) will be available during a logical 1 level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

in both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

Logical 1 (off level) Circuit Calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

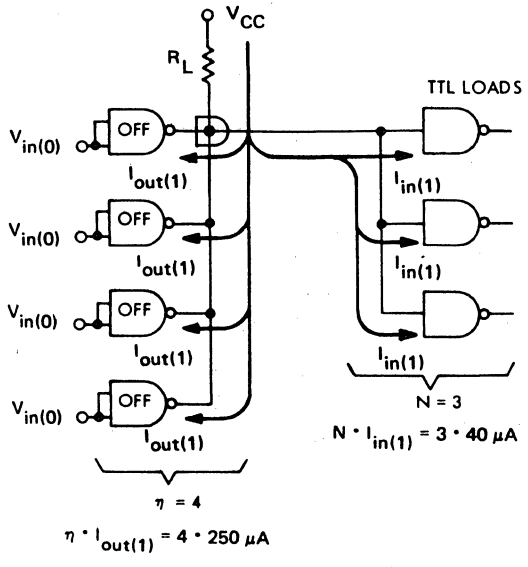
The total current through the load resistor (I_{RL}) is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-OR connected outputs:

$$I_{RL} = n \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{n \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: n = number of gates wire-OR connected, and
N = number of TTL loads.



Calculation

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{n \cdot I_{out(1)} + N \cdot I_{load}}$$

Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012} = \frac{2.6}{0.00112} = 2321\ \Omega$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012} = \frac{2.6}{0.00112} = 2321\Omega$$

FIGURE A – LOGICAL 1 CIRCUIT CONDITIONS

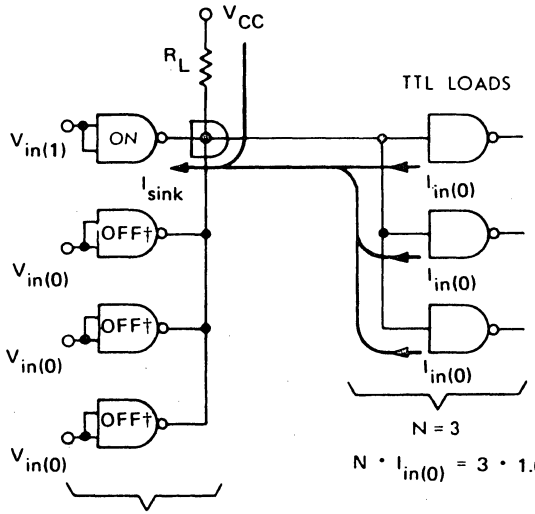
Logical 0 (on level) Circuit Calculations (see figure B)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)}\ \text{required}}{I_{SINK}\ \text{capability} - I_{SINK}\ \text{from TTL loads}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)}\ \text{required}}{I_{sink}\ \text{capability} - I_{sink}\ \text{from TTL loads}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048} = \frac{4.6}{0.0112} = 410\ \Omega$$

†Current into OFF outputs is negligible at logical 0.

Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)}\ \text{required}}{I_{SINK}\ \text{capability} - I_{SINK}\ \text{from TTL loads}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048} = \frac{4.6}{0.0112} = 4100\ \Omega$$

FIGURE B — LOGICAL 0 CIRCUIT CONDITIONS

APPLICATION DATA FOR OPEN COLLECTOR DEVICES

Driving TTL Loads and Combining Outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-OR connecting two to seven parallel outputs. Each value shown for wire-OR output one is determined by the fan-out plus the leakage of a single output transistor. Extension beyond seven wire-OR connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} - 0 = \infty$) however, the use of a 4 kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43V.

TABLE I

Fan-Out To TTL Loads	Wire-OR Outputs							
	1	2	3	4	5	6	7	1 To 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000#
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

X — Not recommended or not possible.
— The theoretical value is ∞. See explanation in text.
All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5V, $V_{out(1)}$ required = 2.4V
Logical 0 conditions: V_{CC} = 5V, $V_{out(0)}$ required = 0.4V

This series is designed to be used in conjunction with the 54/7400 Series TTL in system locations requiring minimum propagation delays. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges:

54H Series	−55°C to 125°C
74H Series	0°C to 75°C

All devices operate over a frequency range between D.C. and typically 30 and 50 MHz, and are fully compatible with all 54H/74H series TTL and 930 series DTL.

Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e., high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

All functions are available in plastic or ceramic and Flat Pack.

FEATURES

- **High speed**—typical propagation delay (gate) of 6 ns. @ C_L = 25 pF
- **Guaranteed noise margin**—greater than 400 mV.
- **Low power dissipation**—23 mW per gate at 50% duty cycle.
- **Worst case fan-out of 10.**
- **Low output impedance.**
- **Logic levels guaranteed over range of supply voltage and operating temperature**
- **Compatible with other DTL, TTL logic series.**

INDEX FOR STANDARD 7400H SERIES

For the military range, replace 74H in the type number by 54H.

Prefix the type number by ITT and end with J which indicates the ceramic dual-in-line package.
For example: ITT5400 is a Quad 2-input NAND gate device in 54 series logic with a ceramic dual-in-line package.

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease of reading, the data only refers to the 74H series family but it is equally applicable to the 54H series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but <0.8 V
Logical '1' = High voltage; typically 3.3 V but >2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES (except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74H series	4.75	5.25	V
54H series	4.5	5.5	V
Operating temperature:			
74H series	0	75	°C
54H series	−55	125	°C

D.C. noise margin typically greater than 1 V.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1) ..... 7 V
Input voltage ..... 5.5 V
Voltage between inputs ..... 5.5 V
Continuous input current ..... −10 mA
Standard output voltage ..... −0.5 to 5.5 V
Storage temperature! ..... −65°C to 150°C

Note 1
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS (limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

PARAMETER	LIMIT (Note 8)				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	V_{OL} <0.4 V or V_{OH}> 2.4 V (Note 1)
V_{IL}			0.8	V	Min.	V_{OL} <0.4 V or V_{OH}> 2.4 V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL} = 20 mA, V_{IH} = 2 V or V_{IL} = 0.8 V (Note 3)
V_{OH}	2.4	3.3		V	Min.	V_{IL} = 0.8 V or V_{OH} = 2.0 V (Note 4)
I_{CEX} open collector only			250	uA	Min.	V_{IL} = 0.8 V, V_{IH} = 2 V, V_{OUT} = max. o/p voltage rating
$-I_F$			2.0	mA	Max.	V_F = 0.4 V (Note 5)
I_R			50	uA	Max.	V_R = 2.4 V, input loading-1 unit load (Note 6)
I_R			1.0	mA	Max.	V_R = 5.5 V irrespective of input loading
$-I_{SC}$						
54 series	40		100	mA	Max.	V_{OUT} = 0 V (Note 7)

Where characteristics for devices differ from the above table these are shown in the data sheets.

Note 1
Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, $V_{OL} \leq 0.4V$ applies, and for flip-flops, either $V_{OL} \leq 0.4V$ or $V_{OH} \geq 2.4V$ applies at each output. Output conditions do not apply for 74H60.

Note 2
Conditions at outputs dependent on the truth table of the device, for example; for gates and inverters $V_{OH} > 2.4V$. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3
Conditions V_{IH} and V_{IL} depend on device truth table.

Note 4
This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table. I_{OH} = −500 uA for devices with Fan-out = 10; I_{OH} = −1.0mA for 54H/74H74; I_{OH} = −1.5mA for 54H/74H40.

Note 5
Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6
All other inputs at 0V for 74H72, 74H73, 74H76. For 74H74 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7
For all devices not more than one output to be shorted at any time. Open collector devices; no parameter for $-I_{SC}$.

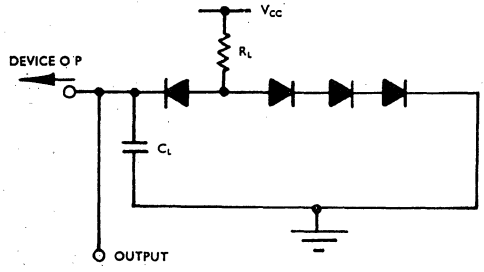
Note 8
Typical limits are at ambient temperature, T_A = 25°C and V_{CC} = 5V.

A.C. TESTS

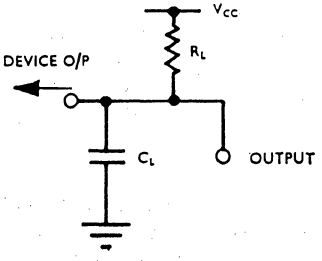
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:

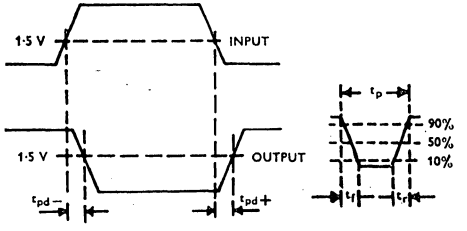


Diodes are type 1N4148 or equiv.

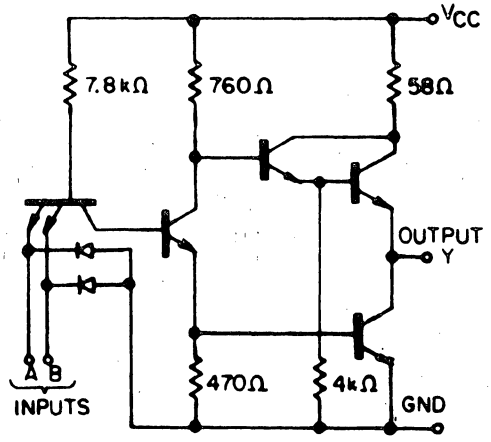
The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.

The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: V_{OUT} = 3V; Rise time, tr, = Fall time, t_f, = less than 7 ns; Z_o = 50; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, t_p = 500 ns.

Waveforms



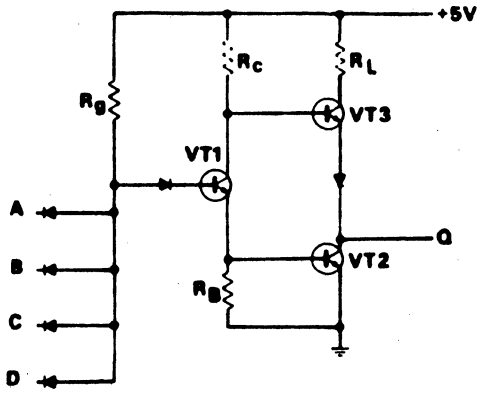
CIRCUIT DIAGRAM ITT74H00 GATE



COMPONENT VALUES ARE NOMINAL

The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_g into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

2. LOW OR OFF STATE

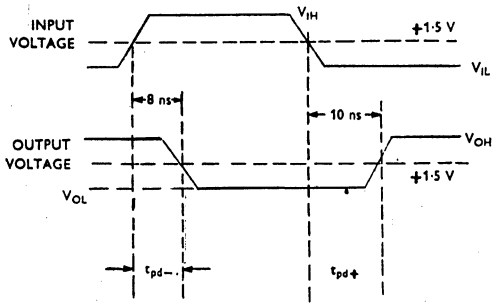
The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about +1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.

Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

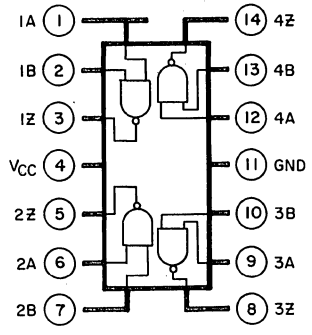
Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.

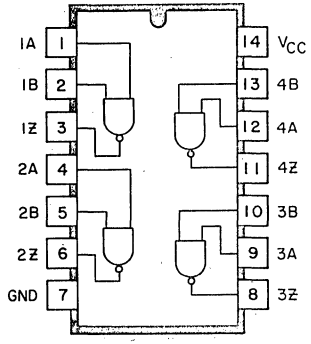
QUADRUPLE 2-INPUT POSITIVE NAND GATES

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



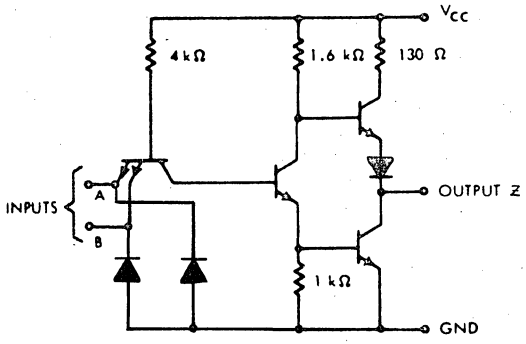
POSITIVE LOGIC: $Z = \overline{AB}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{AB}$

schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5400 Circuits	4.5	5	5.5	V
	7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5400 Circuits	−55	25	125	°C
	7400 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			40 1	uA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−20 −18		−55 −55	mA	V_{CC} = MAX ITT5400 ITT7400
$I_{CC(0)}$	Logical 0 level supply current		12	22	mA	V_{CC} = MAX, V_{in} = 5 V
$I_{CC(1)}$	Logical 1 level supply current		4	8	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		11	22	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

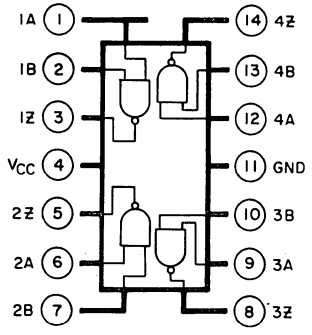
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

ITT SEMICONDUCTORS

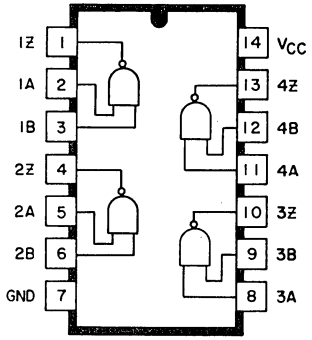
QUADRUPLE 2-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



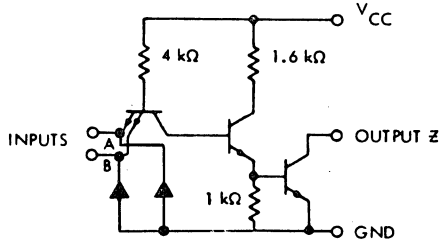
POSITIVE LOGIC: $Z = \overline{AB}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{AB}$

schematic (each gate)



NOTE: Component values shown are nominal.

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5401 Circuits	4.5	5	5.5	V
	7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5401 Circuits	−55	25	125	°C
	7401 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$I_{out(1)}$	Output reverse current			250	uA	V_{CC} = MIN, V_{in} = 0.8V, $V_{out(1)}$ = 5.5V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{CC(0)}$	Logical 0 level supply current		12	22	mA	V_{CC} = MAX, V_{in} = 5V
$I_{CC(1)}$	Logical 1 level supply current		4	8	mA	V_{CC} = MAX, V_{in} = 0

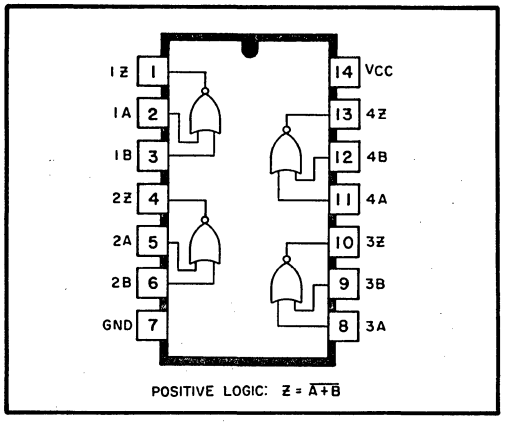
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		35	45	ns	C_L = 15 pF, R_L = 4 kΩ

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

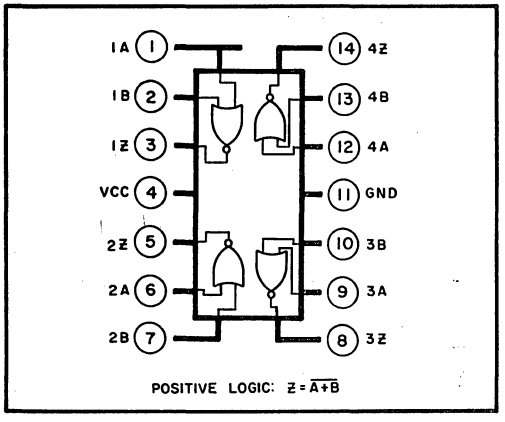
QUADRUPLE 2-INPUT POSITIVE NOR GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



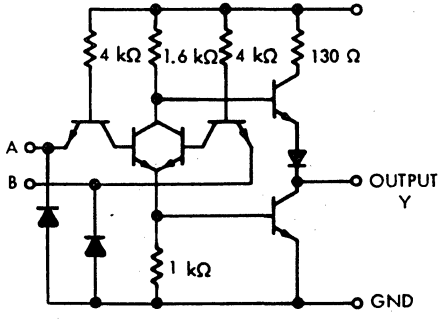
POSITIVE LOGIC: $Z = \overline{A+B}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{A+B}$

schematic (each gate)



NOTE: Component values are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5402 Circuits	4.5	5	5.5	V
	7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5402 Circuits	−55	25	125	°C
	7402 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX ITT5402
		−18		−55		ITT7402
$I_{CC(0)}$	Logical 0 level supply current		14	27	mA	V_{CC} = MAX, V_{in} = 5 V
$I_{CC(1)}$	Logical 1 level supply current		8	16	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level		12	22	ns	C_L = 15 pF, R_L = 400Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

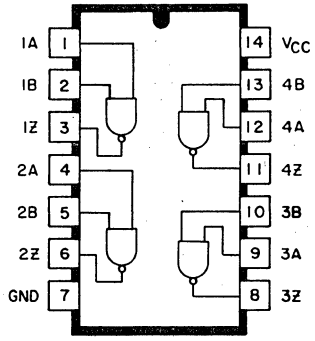
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

ITT SEMICONDUCTORS

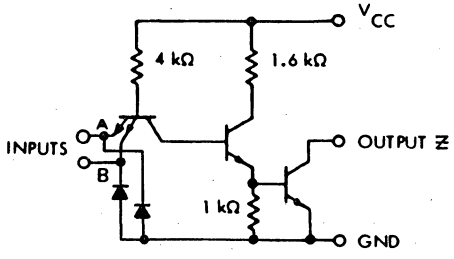
QUADRUPLE 2-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{AB}$

schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5403 Circuits	4.5	5	5.5	V
	7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5403 Circuits	−55	25	125	°C
	7403 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$I_{out(1)}$	Output reverse current			250	µA	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			40	µA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{CC(0)}$	Logical 0 level supply current		12	22	mA	V_{CC} = MAX, V_{in} = 5 V
$I_{CC(1)}$	Logical 1 level supply current		4	8	mA	V_{CC} = MAX, V_{in} = 0

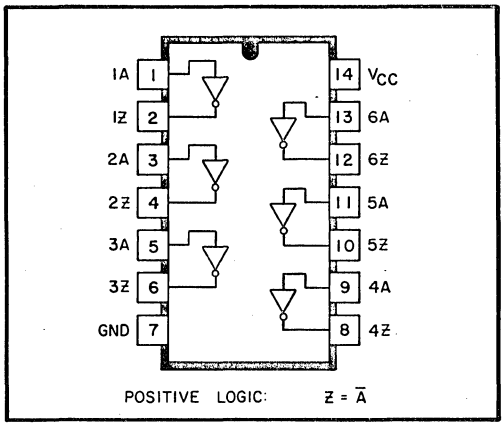
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

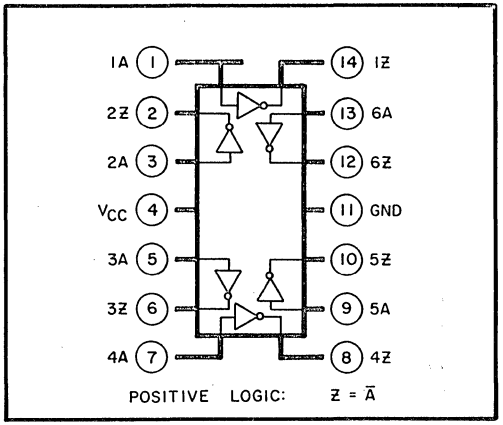
	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level		35	45	ns	C_L = 15 pF, R_L = 4 kΩ

HEX INVERTERS

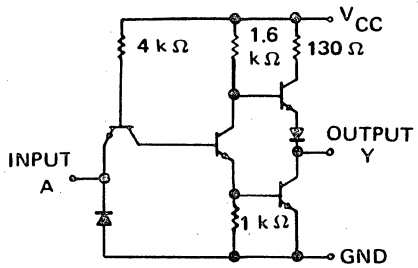
DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic (each inverter)



NOTE: Component values shown are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5404 Circuits	4.5	5	5.5	V
	7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5404 Circuits	−55	25	125	°C
	7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	2			V		
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA	
$I_{in(0)}$	Logical 0 level input current			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V	
$I_{in(1)}$	Logical 1 level input current			40	uA	V_{CC} = MAX, V_{in} = 2.4 V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT5404
		−18		−55			ITT7404
$I_{CC(0)}$	Logical 0 level supply current		18	33	mA	V_{CC} = MAX, V_{in} = 5 V	
$I_{CC(1)}$	Logical 1 level supply current		6	12	mA	V_{CC} = MAX, V_{in} = 0	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		12	22	ns	C_L = 15 pF, R_L = 400 Ω

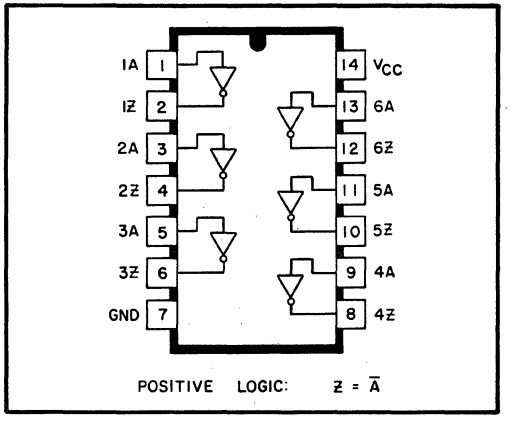
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

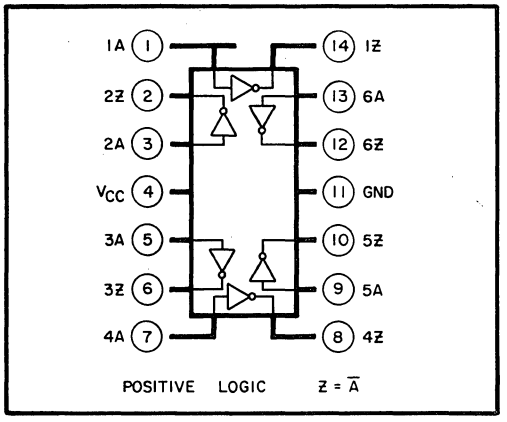
[3] Not more than one output should be shorted at a time.

HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

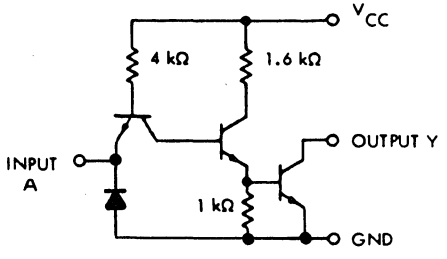
DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic (each inverter)



NOTE: Component values are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5405 Circuits	4.5	5	5.5	V
	7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5405 Circuits	−55	25	125	°C
	7405 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$I_{out(1)}$	Output reverse current			250	uA	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current			40	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{CC(0)}$	Logical 0 level supply current		18	33	mA	V_{CC} = MAX, V_{in} = 5 V, T_A = 25°C
$I_{CC(1)}$	Logical 1 level supply current		6	12	mA	V_{CC} = MAX, V_{in} = 0 T_A = 25°C

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		40	55	ns	C_L = 15 pF, R_L = 4 kΩ

[1] These typical values are at V_{CC} = 5 V, T_A = 25°C.

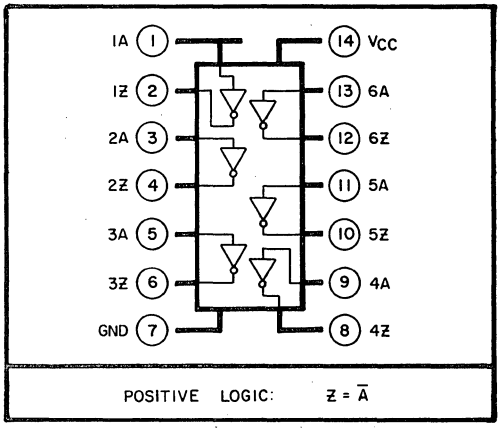
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

ITT SEMICONDUCTORS

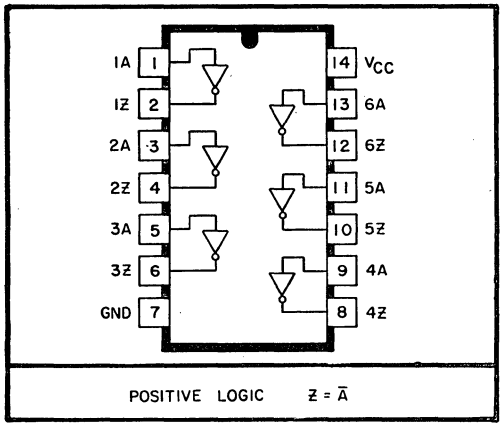
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)

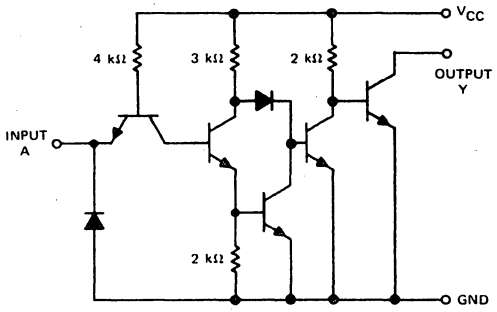


DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 15 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation; 105 mW

schematic (each inverter)



Note: Component values shown are nominal.

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS or Hi NIL), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The ITT5406 and ITT7406 have minimum breakdown voltages of 30 volts and the ITT5416 and ITT7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the ITT5406 and ITT5416, and 40 milliamperes for the ITT7406 and ITT7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The ITT5406 and ITT5416 are characterized, for operation over the full military temperature range of −55°C to 125°C; the ITT7406 and ITT7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Output Voltage (see Notes 1 and 2):
ITT5406, ITT7406 Circuits ..... 30 V
ITT5416, ITT7416 Circuits ..... 15 V
Operating free-air temperature range:
ITT5406, ITT5416 Circuits ..... −55°C to 125°C
ITT7406, ITT7416 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		ITT5406, ITT5416			ITT7406, ITT7416			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	ITT5406, ITT7406			30			30	V
	ITT5416, ITT7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN I_i = −12 mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX
V_{OL}	Low-level output voltage			0.7	V	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX
				0.4		V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4 V
				1	mA	V_{CC} = MAX, V_I = 5.5 V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4 V
I_{CCH}	Supply current, high-level output		30	42	mA	V_{CC} = MAX, V_I = 0
I_{CCL}	Supply current, low-level output		27	38	mA	V_{CC} = MAX, V_I = 5 V

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

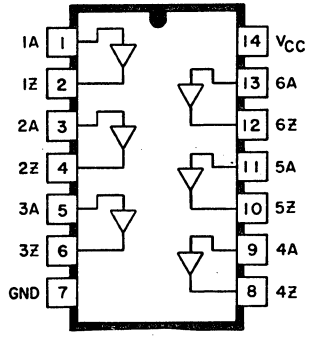
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		10	15	ns	C_L = 15 pF, R_L = 110Ω
t_{PHL}	Propagation delay time, high-to-low-level output		15	23	ns	C_L = 15 pF, R_L = 110Ω

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

- **Converts TTL voltage levels to MOS levels**
- **High sink-current capability**
- **Input clamping diodes simplify system design**
- **Typical propagation delay time: 14 ns**
- **Open-collector driver for indicator lamps and relays**
- **Inputs fully compatible with most TTL and DTL circuits**
- **Typical power dissipation: 145 mW**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



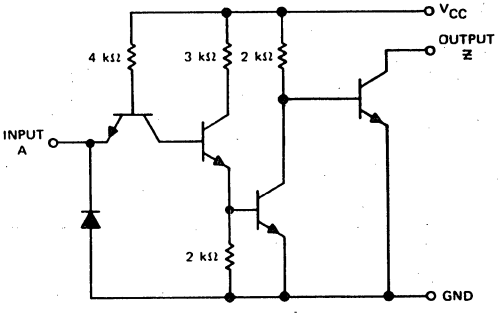
POSITIVE LOGIC: $Z = A$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Output Voltage (see Notes 1 and 2):
ITT5407, ITT7407 Circuits 30V
ITT5417, ITT7417 Circuits 15V
Operating free-air temperature range:
ITT5407, ITT5417 Circuits ..... −55°C to 125°C
ITT7407, ITT7417 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

schematic (each buffer/driver)



Note: Component values shown are nominal.

ITT5407, ITT5417, ITT7407, ITT7417
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS or Hi NIL), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. For increased fan-out, several buffers in a single package may be paralleled. The ITT5407 and ITT7407 have minimum breakdown voltages of 30 volts and the ITT5417 and ITT7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the ITT5407 and ITT5417, and 40 milliamperes for the ITT7407 and ITT7417.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The ITT5407 and ITT5417 are characterized for operation over the full military temperature range of −55°C to 125°C; the ITT7407 and ITT7417 are characterized for operation from 0°C to 70°C.

recommended operating conditions		Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	ITT5407, ITT7407			30			30	V
	ITT5417, ITT7417			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ[1]	Max	Unit	Test Conditions[2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN I_I = −12 mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_I = 2V, V_{OH} = MAX
V_{OL}	Low-level output voltage			0.7	V	V_{CC} = MIN, V_I = 0.8V, I_{OL} = MAX
				0.4		V_{CC} = MIN, V_I = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		29	41	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		21	30	mA	V_{CC} = MAX, V_I = 0V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

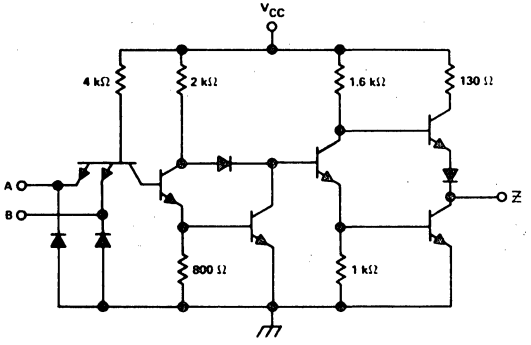
	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		6	10	ns	C_L = 15 pF, R_L = 110 Ω
t_{PHL}	Propagation delay time, high-to-low-level output		20	30	ns	C_L = 15 pF, R_L = 110 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

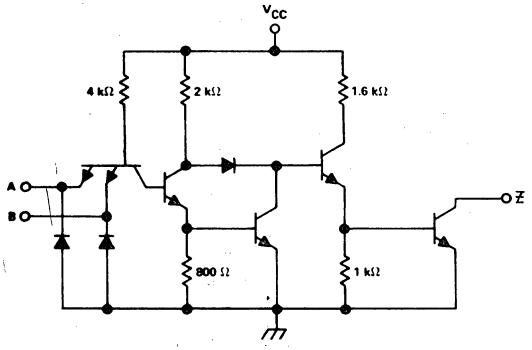
QUADRUPLE 2-INPUT POSITIVE AND GATES

schematics (each gate)

ITT5408/ITT7408

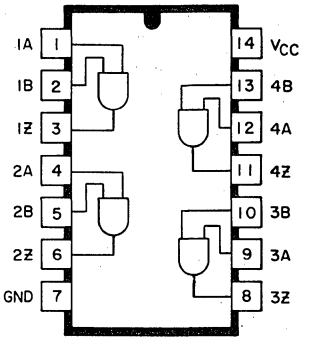


ITT5409/ITT7409



Component values shown are nominal.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = AB$

The ITT5408 and ITT5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the ITT7408 and ITT7409 are characterized for operation from 0°C to 70°C.

Choice of Totem-Pole Outputs (ITT5408/ITT7408) or Open-Collector Outputs (ITT5409/ITT7409)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Output voltage (see Notes 1 and 3)
(ITT5409/ITT7409) 5.5V
Operating free-air temperature range:
ITT5408/ITT5409 ..... −55°C to 125°C
ITT7408/ITT7409 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The ITT5408/ITT7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The ITT5409/ITT7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The ITT5409/ITT7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

recommended operating conditions

	Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5408, ITT7408 Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12 mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800 uA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX, ITT5408
		−18		−55		ITT7408
I_{CCH}	Supply current, high-level output		11	21	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		20	33	mA	V_{CC} = MAX, V_I = 0V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		ITT5408, ITT7408 Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		17.5	27	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output		12	19	ns	C_L = 15 pF, R_L = 400Ω

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5409, ITT7409			Unit	Test Conditions [2]
		Min	Typ [1]	Max		
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_1	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_i = −12 mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_{IH} = 2V, V_{OH} = 5.5V
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		11	21	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		20	33	mA	V_{CC} = MAX, V_I = 0V

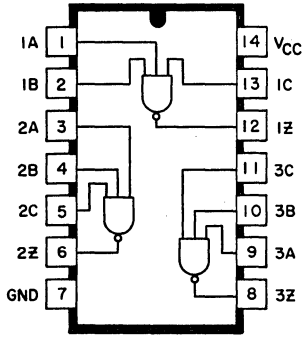
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		ITT5409, ITT7409			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Propagation delay time, low-to-high-level output		21	32	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output		16	24	ns	C_L = 15 pF, R_L = 400Ω

[1] All typical values at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

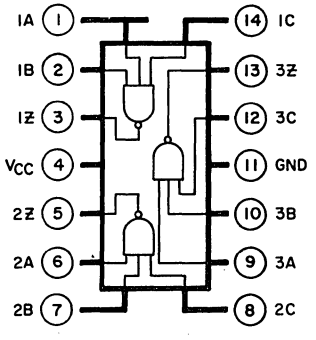
TRIPLE 3-INPUT POSITIVE NAND GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



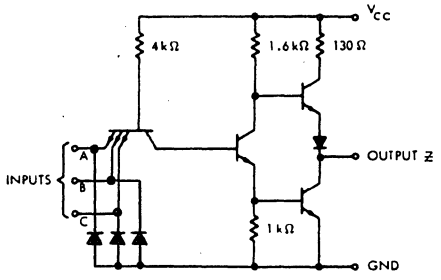
POSITIVE LOGIC: $Z = \overline{ABC}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC $Z = \overline{ABC}$

schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 5410 Circuits	4.5	5	5.5	V
7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: 5410 Circuits	−55	25	125	°C
7410 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			40 1	uA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = 5.5 V ITT5410
		−18		−55		ITT7410
$I_{CC(0)}$	Logical 0 level supply current		9	16.5	mA	V_{CC} = MAX, V_{in} = 5 V
$I_{CC(1)}$	Logical 1 level supply current		3	6	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		11	22	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

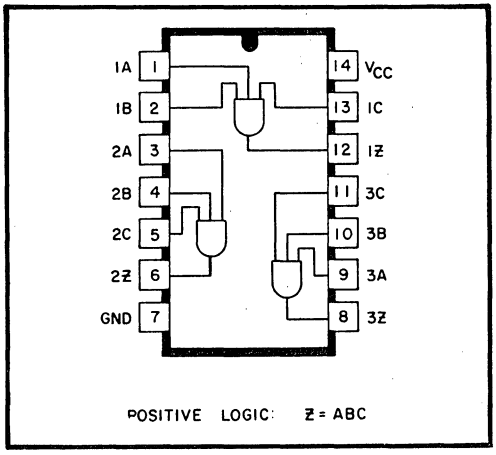
TRIPLE 3-INPUT POSITIVE AND GATES

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The ITT5411/ITT7411, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)

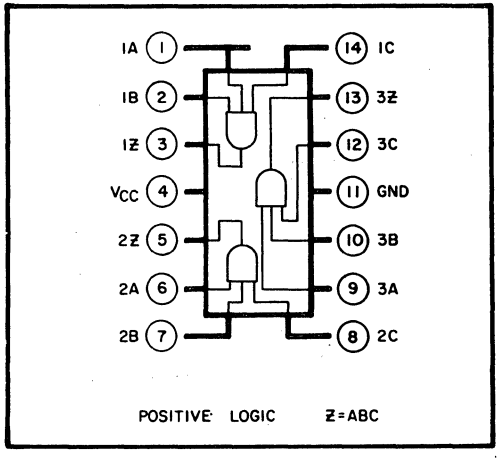


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

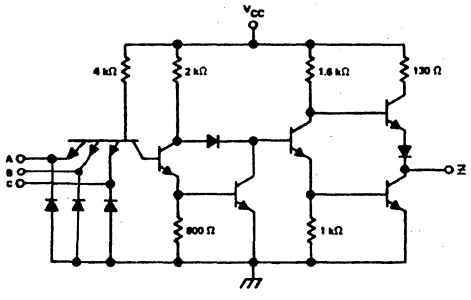
Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT5411/ITT5411 ..... −55°C to 125°C
ITT7411/ITT7411 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic



recommended operating conditions

	ITT5411			ITT7411			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12 mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800 uA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX, ITT5411
		−18		−55		ITT7411
I_{CCH}	Supply current, high-level output		11	21	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		20	33	mA	V_{CC} = MAX, V_I = 0V

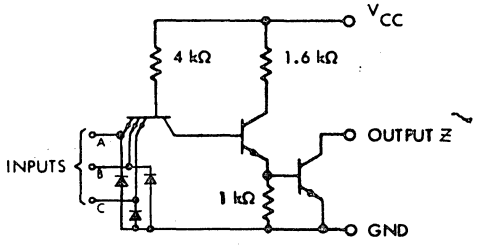
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		17.5	27	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output		12	19	ns	C_L = 15 pF, R_L = 400Ω

ITT SEMICONDUCTORS

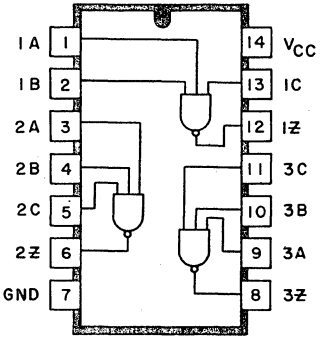
TRIPLE 3-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{ABC}$

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5412 Circuits	4.5	5	5.5	V
	7412 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5412 Circuits	−55	25	125	°C
	7412 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$I_{out(1)}$	Output reverse current			250	µA	V_{CC} = MIN, $V_{in(0)}$ = 0.8V, $V_{out(1)}$ = 5.5V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			40	µA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{CC(0)}$	Logical 0 level supply current		9	16.5	mA	V_{CC} = MAX, V_{in} = 5V
$I_{CC(1)}$	Logical 1 level supply current		3	6	mA	V_{CC} = MAX, V_{in} = 0

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		35	45	ns	C_L = 15 pF, R_L = 4 kΩ

DUAL NAND SCHMITT TRIGGERS

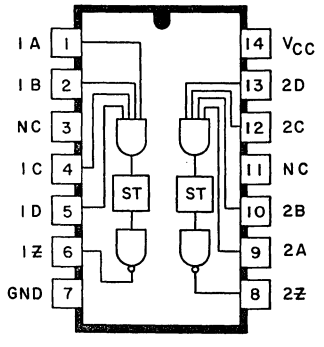
- **Operation from Very Slow Edges**
- **Temperature-Compensated Threshold**
- **Temperature-Compensated Hysteresis, Typically 0.8V**
- **High Noise Immunity**

The ITT5413 and ITT7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800 mV.

An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The ITT5413/ITT7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can also be triggered from straight d-c levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The ITT5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT7413 is characterized for operation from 0°C to 70°C.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

NC – NO INTERNAL CONNECTION
†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT5413 Circuits ..... −55°C to 125°C
ITT7413 Circuits ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions		ITT5413 MIN	ITT5413 NOM	ITT5413 MAX	ITT7413 MIN	ITT7413 NOM	ITT7413 MAX	UNIT
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	0	125	0	25	70	°C
Maximum input rise and fall times		No restriction			No restriction			

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{T+}	Positive-going threshold voltage	1.5	1.7	2	V	V_{CC} = 5V
V_{T-}	Negative-going threshold voltage	0.6	0.9	1.1	V	V_{CC} = 5V
V_{T+} $-V_{T-}$	Hysteresis	0.4	0.8		V	V_{CC} = 5V
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage	2.4	3.3		V	V_{CC} = MIN, V_I = 0.6V I_{OH} = −800 uA
V_{OL}	Low-level output voltage		0.22	0.4	V	V_{CC} = MIN, V_I = 2V, I_{OL} = 16 mA
I_{T+}	Input current at positive-going threshold		−0.65		mA	V_{CC} = 5V, V_I = V_{T+}
I_{T-}	Input current at negative-going threshold		−0.85		mA	V_{CC} = 5V, V_I = V_{T-}
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	µA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current		−1	−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−18		−55	mA	V_{CC} = MAX
I_{CCH}	Supply current, high-level output		14	23	mA	V_{CC} = MAX, V_I = 0
I_{CCL}	Supply current, low-level output		20	32	mA	V_{CC} = MAX, V_I = 4.5V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		18	27	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output		15	22	ns	C_L = 15 pF, R_L = 400Ω

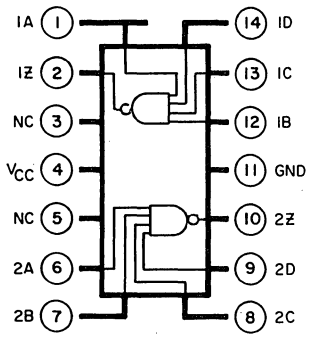
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

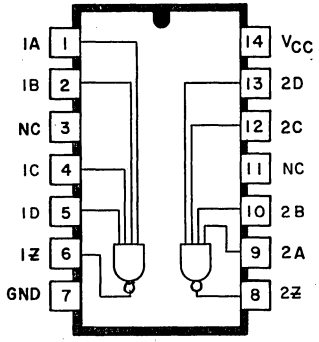
DUAL 4-INPUT POSITIVE NAND GATES

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



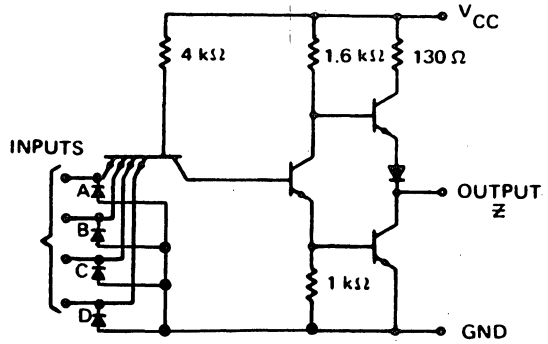
POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

schematic (each gate)



Component values shown are nominal.

NC-No internal connection.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5420 Circuits	4.5	5	5.5	V
	7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5420 Circuits	−55	25	125	°C
	7420 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0 8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			40	µA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX ITT5420
		−18		−55		ITT7420
$I_{CC(0)}$	Logical 0 level supply current		6	11	mA	V_{CC} = MAX, V_{in} = 5 V
$I_{CC(1)}$	Logical 1 level supply current		2	4	mA	V_{CC} = MAX, V_{in} = 0

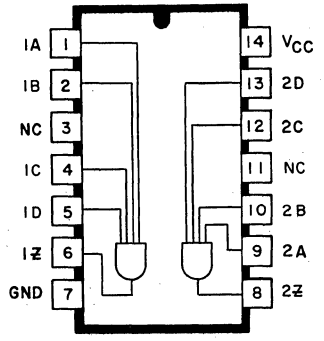
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		12	22	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

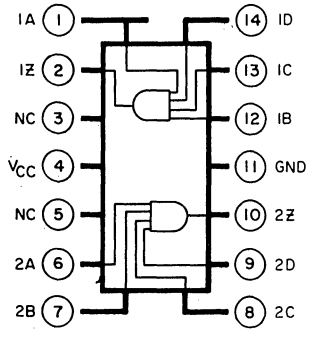
DUAL 4-INPUT POSITIVE AND GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = ABCD$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



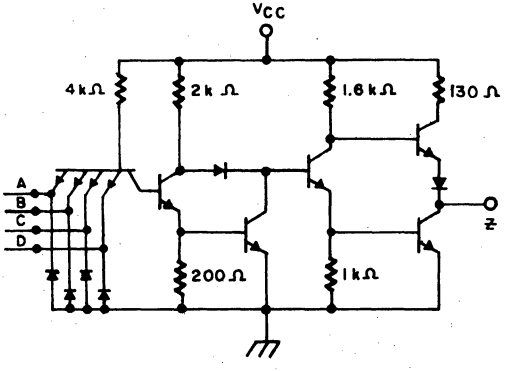
POSITIVE LOGIC: $\overline{Z} = ABCD$

This Series 54/74 TTL gate provides the system designer with direct implementation of the positive AND or negative OR functions.

The ITT5421/ITT7421 with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level.

The ITT5421 is characterized for operation over the full military temperature range of -55°C to 125°C; the ITT7421 is characterized for operation from 0°C to 70°C.

Circuit schematic



COMPONENT VALUES SHOWN ARE NOMINAL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT5421 ..... −55°C to 125°C
ITT7421 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5421, ITT7421 Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA	
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800 uA	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16 mA	
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT5421
		−18		−55			ITT7421
I_{CCH}	Supply current, high-level output		11	21	mA	V_{CC} = MAX, V_I = 5V	
I_{CCL}	Supply current, low-level output		20	33	mA	V_{CC} = MAX, V_I = 0	

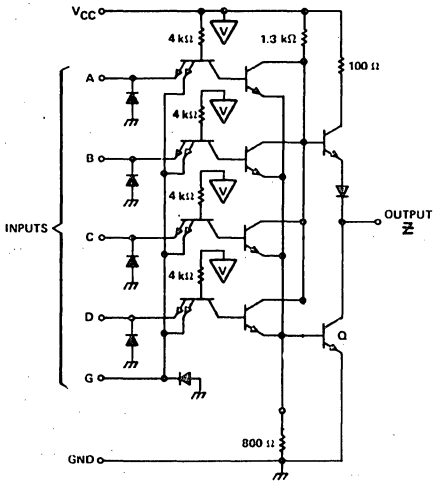
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		ITT5421, ITT7421 Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		17.5	27	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level output		12	19	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

DUAL 4-INPUT NOR GATES WITH STROBE

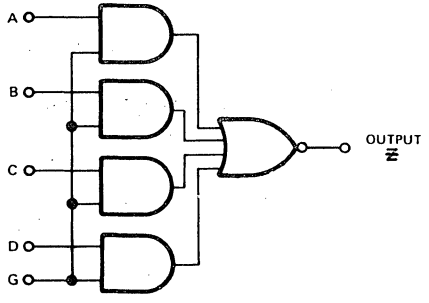
schematic (each gate)

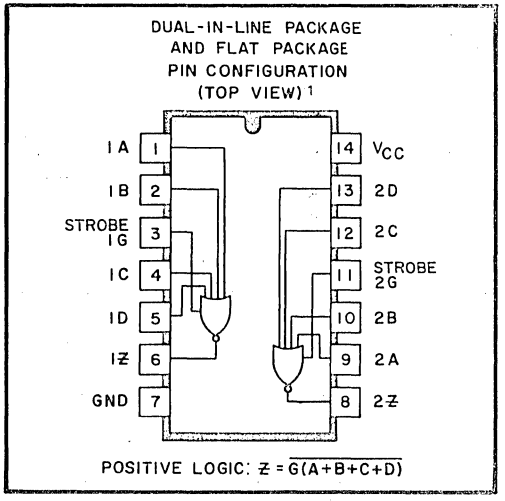


Notes: A. Component values shown are nominal.

V — V_{CC} bus

logic and functional block diagram (each gate)





[1] Pin assignments for these circuits are the same for all packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT5425 ..... −55°C to 125°C
ITT7425 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

TRUTH TABLE

Inputs					Output
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

H = high level, L = low level, X = irrelevant.

recommended operating conditions

		ITT5423,ITT5425			ITT7423,ITT7425			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter			Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_I	Input clamp voltage				−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage		2.4	3.3		V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = −800uA
V_{OL}	Low-level output voltage			0.22	0.4	V	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA
I_I	Input current at maximum input voltage				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current	data inputs			40	uA	V_{CC} = MAX, V_I = 2.4V
		strobe inputs			160		
I_{IL}	Low-level input current	data inputs			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
		strobe inputs			−6.4		
I_{OS}	Short-circuit output currents [3]		−20		−55	mA	V_{CC} = MAX
I_{CCH}	Supply current, high-level output			8	16	mA	V_{CC} = MAX, All inputs at 0V
I_{CCL}	Supply current, low-level output			10	19	mA	V_{CC} = MAX, All inputs at 5V

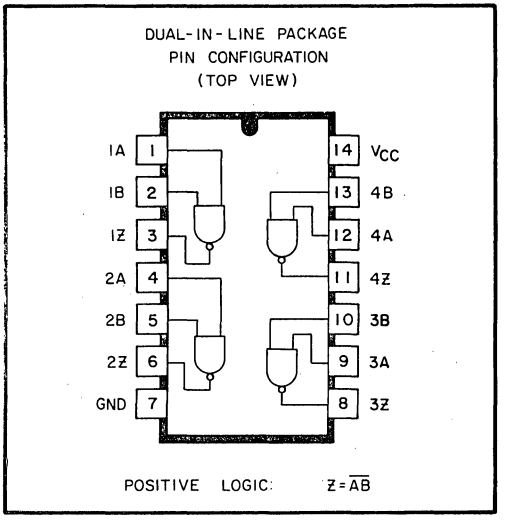
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

ITT SEMICONDUCTORS

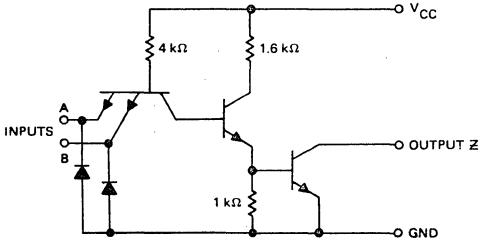
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE NAND GATES

These open-collector NAND gates feature high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source. The output transistor will sink 16 milliamperes while maintaining a low-level output voltage of 0.4 volt maximum thus providing a high-fan-out driver with the nominal power dissipation of standard Series 54/74 gates.

The ITT5426 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT7426 is characterized for operation from 0°C to 70°C.



schematic (each gate)



Note: Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Output voltage (see Notes 1 and 2): 15V
Operating free-air temperature range:
ITT5426 Circuits ..... −55°C to 125°C
ITT7426 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	ITT5426			ITT7426			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN I_i = −12 mA
V_{OH}	High-level output voltage	15			V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = 1 mA
I_{OH}	High-level output current			50	uA	V_{CC} = MIN, V_{IL} = 0.8V, V_{OH} = 12V
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA
I_{IH}	High-level input current (each input)			40 1	uA mA	V_{CC} = MAX, V_I = 2.4V V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		4	8	mA	V_{CC} = MAX, V_I = 0
I_{CCL}	Supply current, low-level output		12	22	mA	V_{CC} = MAX, V_I = 5V

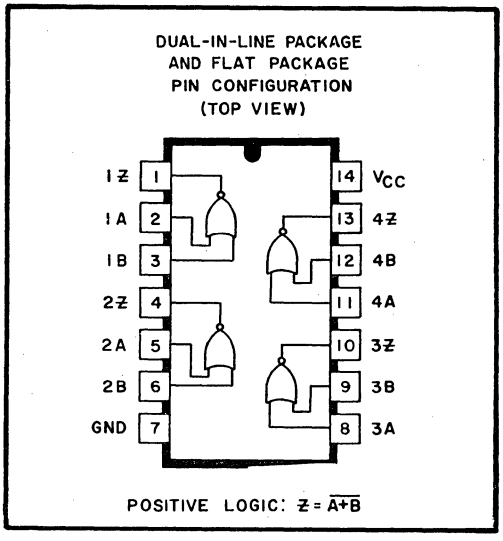
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		16	24	ns	C_L = 15 pF, R_L = 1kΩ
t_{PHL}	Propagation delay time, high-to-low-level output		11	17	ns	C_L = 15 pF, R_L = 1kΩ

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

QUADRUPLE 2-INPUT POSITIVE NOR BUFFERS

Choice of Totem Pole Outputs (ITT5428/ITT7428)
or Open Collector Outputs (ITT5433/ITT7433)



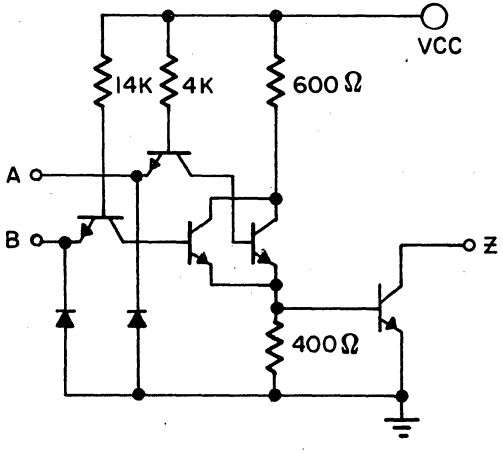
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Output voltage of
ITT5433, ITT7433 (Note 2) 5.5V
Operating free-air temperature range:
ITT5428, ITT5433 ..... −55°C to 125°C
ITT7428, ITT7433 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

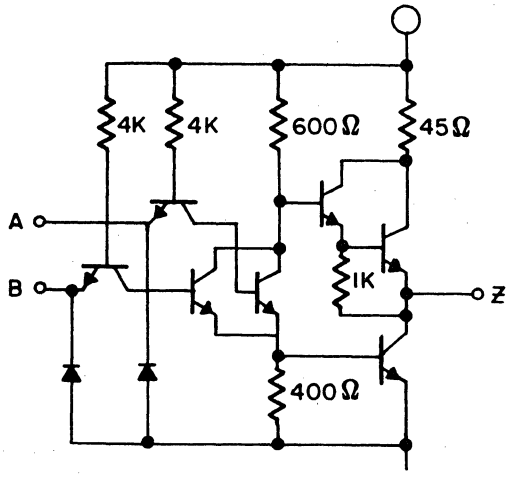
Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

schematics (each gate)

ITT5428/ITT7428



ITT5433/ITT7433



recommended operating conditions

	ITT5428			ITT7428			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			30			30	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5428, ITT7428			Unit	Test Conditions [2]
		Min	Typ [1]	Max		
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min, I_i = −12mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{CC} = 0.8V I_{OH} = −2.4mA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2.0V I_{OL} = 48mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 55V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−70		−180	mA	V_{CC} = MAX
I_{CCH}	Supply current, high-level output			21	mA	V_{CC} = MAX, V_I = 0V
I_{CCL}	Supply current, low-level output			57	mA	V_{CC} = MAX, V_I = 5V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		ITT5408, ITT7408			Unit	Test Conditions
		Min	Typ	Max		
1 t_{PLH}	Propagation delay time, low-to-high-level output			9	ns	C_L = 50 pF R_L = 133 Ω
t_{PHL}	Propagation delay time, high-to-low-level output			12	ns	C_L = 50 pF R_L = 133 Ω

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

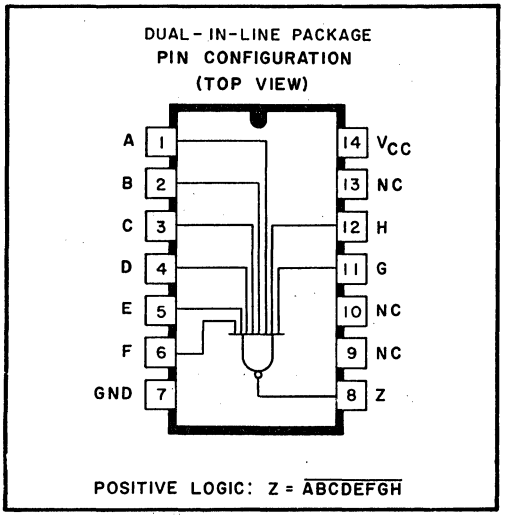
	Parameter	ITT5409, ITT7409 Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_{IL} = 0.8V V_{OH} = 5.5V
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2.0V I_{OL} = 48mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output			21	mA	V_{CC} = MAX, V_I = 0V
I_{CCL}	Supply current, low-level output			57	mA	V_{CC} = MAX, V_I = 5V

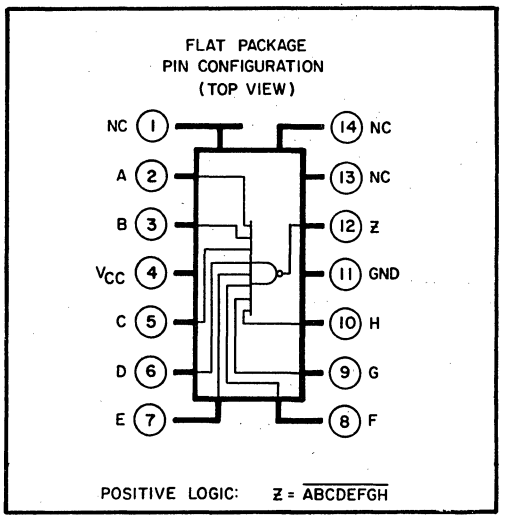
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	ITT5409, ITT7409 Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output			15	ns	C_L = 50 pF R_L = 133 Ω
t_{PHL}	Propagation delay time, high-to-low-level output			18	ns	C_L = 50 pF R_L = 133 Ω

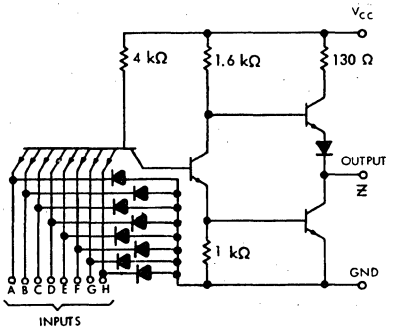
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

8-INPUT POSITIVE NAND GATES





schematic



NOTES: 1. Component values shown are nominal
2. NC — No internal connection

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5430 Circuits	4.5	5	5.5	V
	7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	5430 Circuits	−55	25	125	°C
	7430 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V		
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16 mA	
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V	
$I_{in(1)}$	Logical 1 level input current (each input)			40 1	uA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT5430
		−18		−55			ITT7430
$I_{CC(0)}$	Logical 0 level supply current		3	6	mA	V_{CC} = MAX, V_{in} = 5 V	
$I_{CC(1)}$	Logical 1 level supply current		1	2	mA	V_{CC} = MAX, V_{in} = 0	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level		13	22	ns	C_L = 15 pF, R_L = 400 Ω

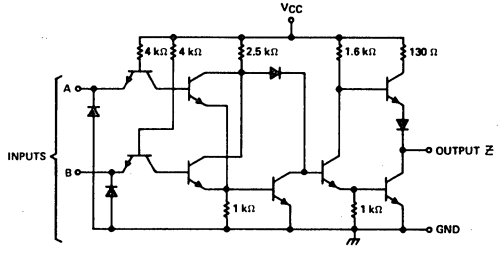
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE-OR GATES

schematic (each gate)

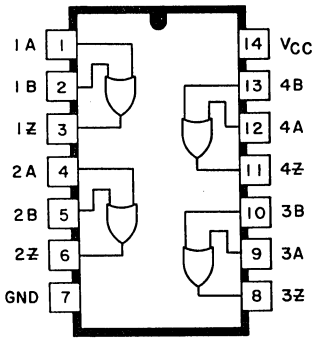


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Operating free-air temperature range:
ITT5432 Circuits ..... −55°C to 125°C
ITT7432 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note: 1. Voltage values are with respect to network ground terminal.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: Z = A+B

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

recommended operating conditions

		ITT5432			ITT7432			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MAX, I_I = −12mA
V_{OH}	High-level output voltage	2.4	3.3		V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800uA
V_{OL}	Low-level output voltage		0.22	0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX ITT5432
		−18		−55		ITT7432
I_{CCH}	Supply current, high-level output		15	22	mA	V_{CC} = MAX, See Note 2
I_{CCL}	Supply current, low-level output		23	38	mA	V_{CC} = MAX, See Note 3

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

Notes: 2. I_{CCH} is measured with one input of each gate at 4.5V, the remaining inputs grounded, and outputs open.
3. I_{CCL} is measured with both inputs of all gates grounded, and outputs open.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{PHL}	Propagation delay time, high-to-low-level output		14	22	ns	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level output		10	15	ns	C_L = 15 pF, R_L = 400Ω

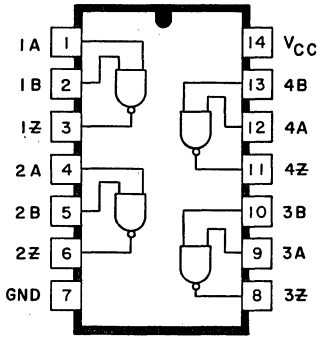
QUADRUPLE 2-INPUT POSITIVE NAND BUFFERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Interemitter voltage (see Note 2) ..... 5.5 V
Output voltage (see Notes 1 and 3):
ITT5438, ITT7438 Circuits ..... 5.5 V
Operating free-air temperature range:
ITT5437, ITT5438 Circuits ..... −55°C to 125°C
ITT7437, ITT7438 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

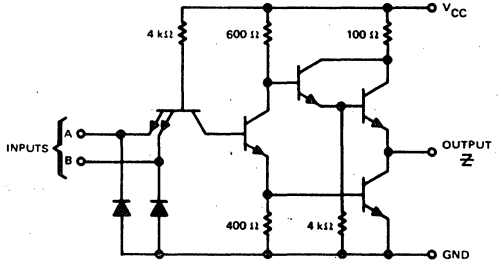
DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



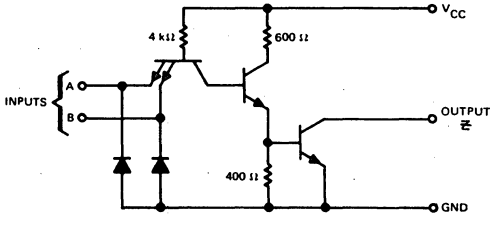
POSITIVE LOGIC: $Z = \overline{AB}$

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

schematics (each buffer)



ITT5437, ITT7437 (TOTEM-POLE OUTPUT)



ITT5438, ITT7438 (OPEN-COLLECTOR OUTPUT)

recommended operating conditions

	ITT5437, ITT5438			ITT7437, ITT7438			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			30			30	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5437, ITT7437			Unit	Test Conditions [2]
		Min	Typ [1]	Max		
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = −1.2mA
V_{OL}	Low-level output voltage		0.22	0.4	V	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 48mA
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−70	mA	V_{CC} = MAX, V_I = 0
I_{CCH}	Supply current, high-level output		9	15.5	mA	V_{CC} = MAX, All inputs at 0V
I_{CCL}	Supply current,low-level output		34	54	mA	V_{CC} = MAX, All inputs at 5V

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5438, ITT7438 Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_{IL} = 0.8V, V_{OH} = 5.5V
V_{OL}	Low-level output voltage		0.22	0.4	V	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 48mA
I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		5	8.5	mA	V_{CC} = MAX, All inputs at 0V
I_{CCL}	Supply current, low-level output		34	54	mA	V_{CC} = MAX, All inputs at 5V

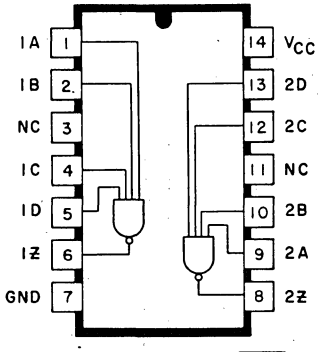
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

Parameter		ITT5437, ITT7437 Min	Typ	Max	ITT5439, ITT7438 Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		13	22		14	22	ns	C_L = 45pF, R_L = 133Ω
t_{PHL}	Propagation delay time, high-to-low-level output		8	15		11	18	ns	C_L = 45pF, R_L = 133Ω

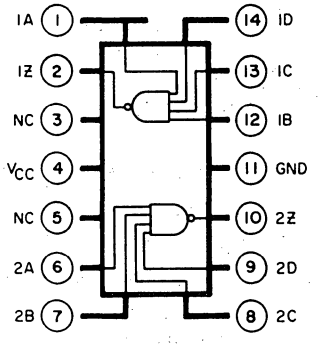
DUAL 4-INPUT POSITIVE NAND BUFFERS

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



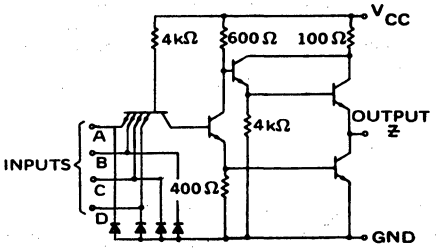
POSITIVE LOGIC: $\bar{Z} = \overline{ABCD}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC $\bar{Z} = \overline{ABCD}$

schematic (each gate)



Component values shown are nominal.
NC—No Internal Connection

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	5440 Circuits	4.5	5	5.5	V
	7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				30	
Operating Free-Air Temperature Range, T_A:	5440 Circuits	−55	25	125	°C
	7440 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V		
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.2 uA	
$V_{out(0)}$	Logical 0 output voltage		0.28	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 48 mA	
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V	
$I_{in(1)}$	Logical 1 level input current (each input)			40 1	uA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V	
I_{OS}	Short-circuit output current [3]	−20		−70	mA	V_{CC} = MAX	ITT5440
		−18		−70	mA		ITT7440
$I_{CC(0)}$	Logical 0 level supply current		17	27	mA	V_{CC} = MAX, V_{in} = 5 V	
$I_{CC(1)}$	Logical 1 level supply current		4	8	mA	V_{CC} = MAX, V_{in} = 0	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	C_L = 15 pF, R_L = 133 Ω
t_{pd1}	Propagation delay time to logical 1 level		13	22	ns	C_L = 15 pF, R_L = 133 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

4-LINE-TO-10-LINE DECODERS (1-OF-10)

- **BCD-to-Decimal**
- **Excess-3-to-Decimal**
- **Excess-3-Gray-to-Decimal**

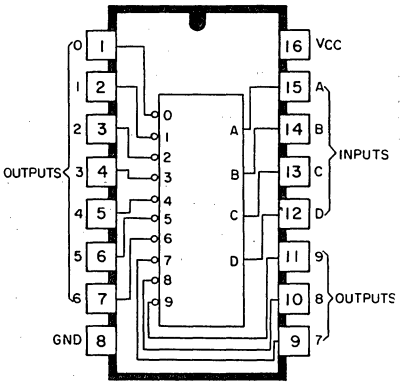
Also for applications as

- **4-Line-to-16-Line Decoders**
- **3-Line to 8-Line Decoders**

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The ITT5442/ITT7442 BCD-to-decimal, ITT5443/ITT7443 excess-3-to-decimal, and ITT5444/ITT7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE FUNCTION TABLE

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Note 1) 5.5V
Operating Free-Air Temperature Range:
ITT5442, ITT5443,
ITT5444 Circuits ..... −55°C to 125°C
ITT7442, ITT7443,
ITT7444 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC} (See Note 1): ITT5442, ITT5443, ITT5444 Circuits	4.5	5	5.5	V
ITT7442, ITT7443, ITT7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

Note: 1. Voltage values are with respect to network ground terminal.

TRUTH TABLES

ITT5442/ITT7442 BCD INPUT

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

ITT5443/ITT7443 EXCESS 3 INPUT

D	C	B	A
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

ITT5444/ITT7444 EXCESS 3 GRAY INPUT

D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
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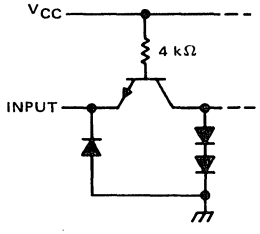
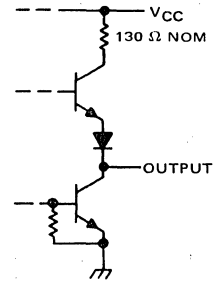
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



ELECTRICAL CHARACTERISTICS Over Recommended Operating Temperature Range (unless otherwise noted)

	PARAMETER	MIN	TYP‡	MAX	UNIT	TEST CONDITIONS†	
Vin(1)	Input voltage required to ensure logical 1 at any input terminal	2			V		
Vin(0)	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
Vout(1)	Logical 1 output voltage	2.4			V	Vcc = MIN, Vin(1) = 2V, Vin(0) = 0.8V, Iload = — 400uA	
Vout(0)	Logical 0 output voltage			0.4	V	Vcc = MIN, Vin(0) = 0.8V,	
Iin(1)	Logical 1 level input current (each input)			40	uA	Vcc = MAX,	Vin = 2.4V
				1	mA	Vcc = MAX,	Vin = 5.5V
Iin(0)	Logical 0 level input current (each input)			— 1.6	mA	Vcc = MAX	Vin = 0.4V
Ios	Short-circuit output current§	— 20		— 55	mA	Vcc = MAX	5442, 5443, 5444
		— 18		— 55			7442, 7443, 7444
Icc	Supply current		28	41	mA	Vcc = MAX,	5442, 5443, 5444
			28	56			7442, 7443, 7444
V1	Input Clamp Voltage			— 1.5	V	Vcc = Min	Ii = — 12mA

SWITCHING CHARACTERISTICS, (Vcc = 5V, TA = 25°C, N = 10)

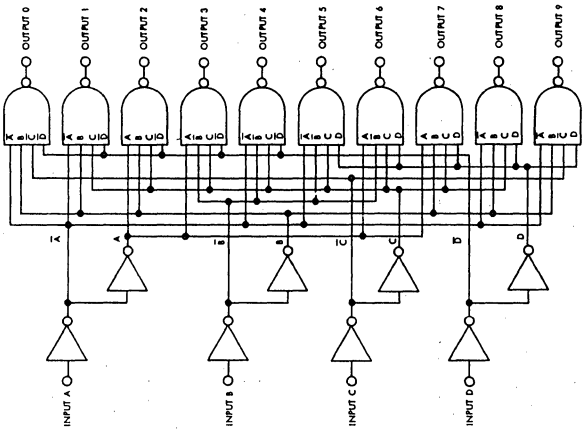
	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
tpd0	Propagation delay time to logical 0 level through two logic levels	10	22	30	ns	CL = 15pF, RL = 400 Ω
tpd0	Propagation delay time to logical 0 level through three logic levels		23	35	ns	CL = 15pF, RL = 400 Ω
tpd1	Propagation delay time to logical 1 level through two logic levels	10	17	25	ns	CL = 15pF, RL = 400 Ω
tpd1	Propagation delay time to logical 1 level through three logic levels		26	35	ns	CL = 15pF, RL = 400 Ω

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

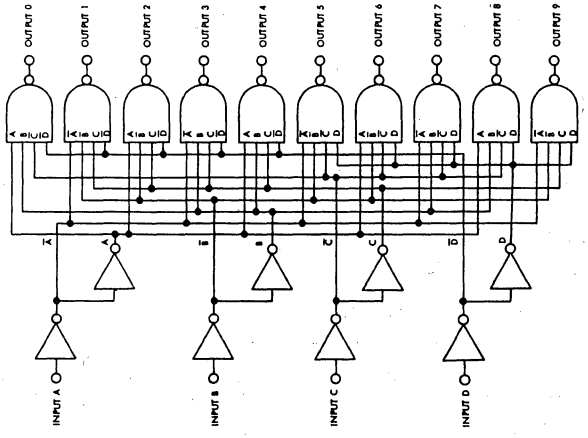
‡ All typical values are at Vcc = 5V, TA = 25°C.

§ Not more than one output should be shorted at a time.

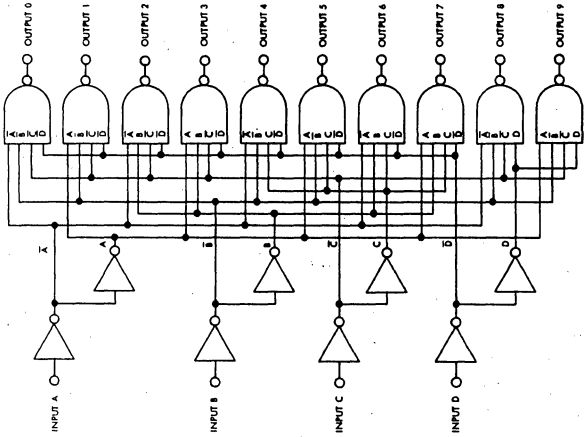
functional block diagrams



5444/7444 EXCESS-3-GRAY-TO-DECIMAL



5443/7443 EXCESS-3-TO-DECIMAL



5442/7442 BCD-TO-DECIMAL

BCD-TO-DECIMAL DECODER/DRIVERS

TTL MSI LAMP, LOGIC, OR MOS DRIVERS

- **Full Decoding of Input Logic**
- **80 mA Sink-Current Capability**

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers.

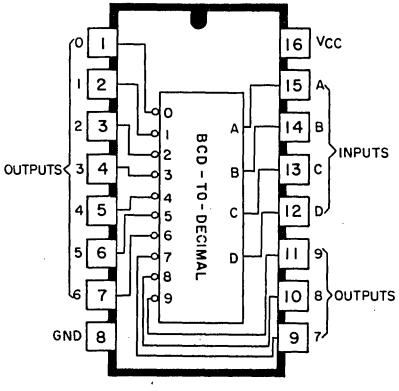
Each of the high-breakdown output transistors (ITT5445, ITT7445 = 30 volts and ITT54145, ITT74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) ..... 7 V
Input Voltage, V_{in} (See Note 1) ..... 5.5 V
Maximum Current into each Output (See Note 2) ..... 1 mA
Operating Free-Air Temperature Range:
ITT5445, ITT54145 Circuits ..... −55°C to 125°C
ITT7445, ITT74145 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 1. These voltage values are with respect to network ground terminal.
2. This rating applies when the output is off.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE FUNCTION TABLE

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
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1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

recommended operating conditions	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): ITT5445, ITT54145 Circuits	4.5	5	5.5	V
ITT7445, ITT74145 Circuits	4.75	5	5.25	V
Voltage on any Output (See Note 2): ITT5445, ITT7445 Circuits			30	V
ITT54145, ITT74145 Circuits			15	V

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

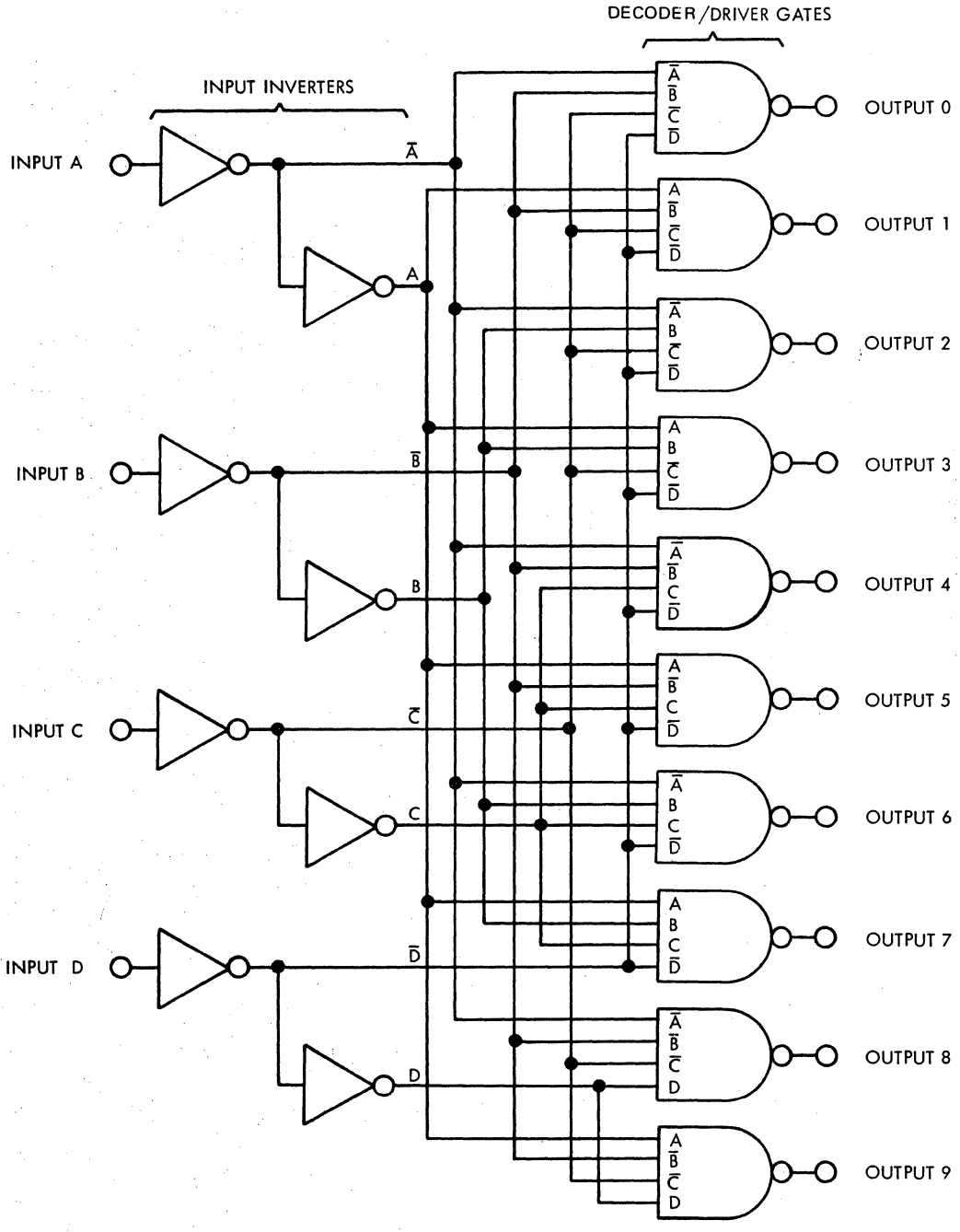
	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_{on}	On-state output voltage		0.5	0.9	V	V_{CC} = MIN, I_{sink} = 80 mA	
				0.4	V	V_{CC} = MIN, I_{sink} = 20 mA	
V_{CC}	Off-state output voltage (ITT5445 or ITT7445)	30			V	V_{CC} = MAX, I_{off} = 250uA	
V_{off}	Off-state output voltage (ITT54145 or ITT74145)	15			V	V_{CC} = MAX, I_{off} = 250 uA	
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4 V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V	
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V	
I_{CC}	Supply current		43	62	mA	V_{CC} = MAX	ITT5445, ITT54145
			43	70	mA		ITT7445, ITT74145

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

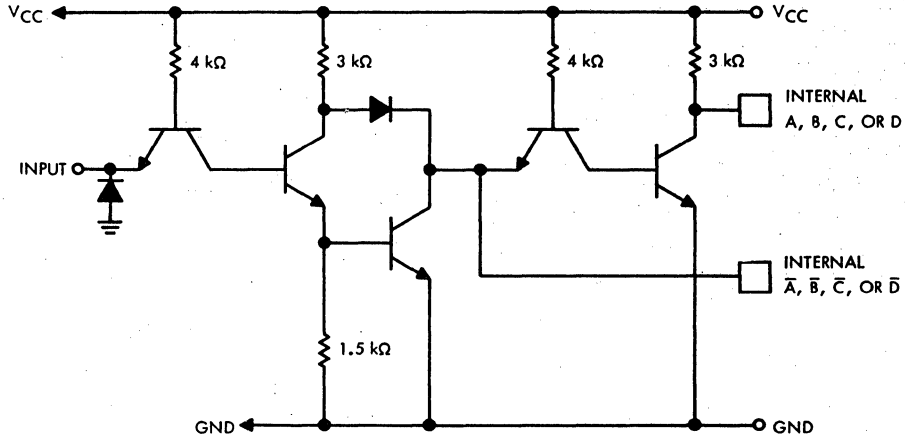
	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
t_{pd1}	Propagation delay time to logical 1 level			50	ns	C_L = 15 pF, R_L = 100 Ω
t_{pd0}	Propagation delay time to logical 0 level			50	ns	C_L = 15 pF, R_L = 100 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

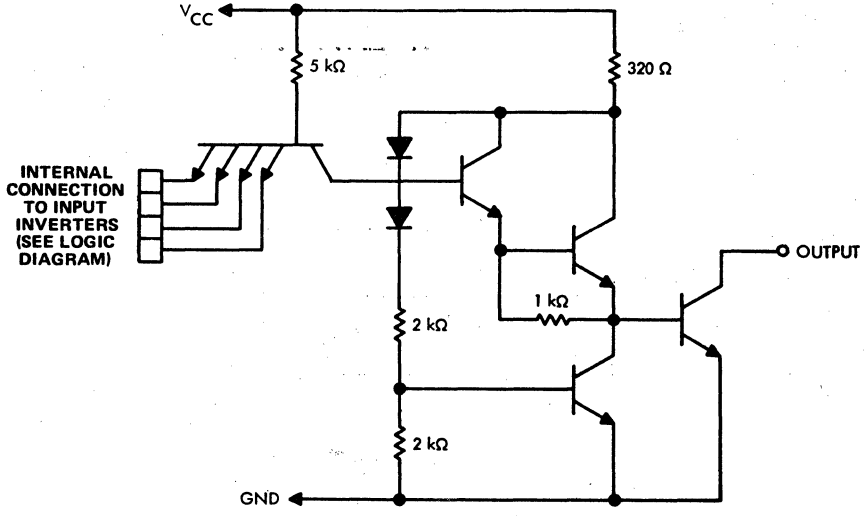
functional block diagram



schematic



EACH PAIR OF INPUT INVERTERS



EACH DECODER/DRIVER GATE

Note: 1. Component values shown are nominal.

ITT SEMICONDUCTORS

Package: Dual In-Line and Flat Pack

BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

ITT5446A, ITT5447A, ITT7446A, ITT7447A
featuring

- **Direct Drive For Indicators**
- **Open Collector Outputs**
- **Lamp Test Provision**
- **Leading/Trailing Zero Suppression**
- **Ceramic Or Plastic Dual In Line Packages**

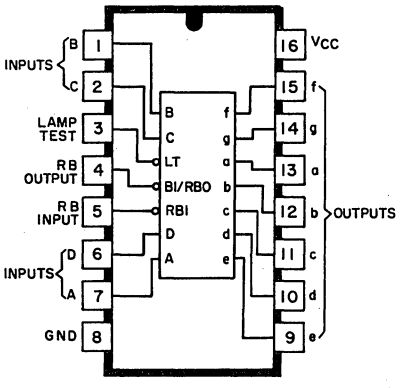
ITT5448, ITT7448
featuring

- **Passive Pull Up Outputs**
- **Lamp Test Provision**
- **Leading/Trailing Zero Suppression**
- **Ceramic Or Plastic Dual In Line Packages**

ALL CIRCUIT TYPES FEATURE:

- **TTL-DTL Compatibility**
- **Full Decoding of all 16 Input Combinations**
- **Lamp Intensity Modulation Capability**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE TRUTH TABLES

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. Two configurations offer active-low, high-sink-current outputs (ITT5446A and ITT5447A) for driving indicators directly; active-high, passive-pull-up outputs, (ITT5448) for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates, and the remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output, and ripple-blanking input for the ITT5446A, ITT5447A and ITT5448.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator (ITT5446A and ITT5447A) or other components (ITT5448). The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the ITT5446A and ITT-5447A are designed to withstand the relatively high voltages required for seven segment indicators. The ITT5446A outputs will withstand 30 volts, and the ITT5447A will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 40 milliamperes of current may be driven directly from the ITT5446A or ITT5447A high-performance output transistors. Segment identification with resultant displays are shown in Figure A. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The ITT5446A, ITT5447A, and ITT5448 circuits incorporate automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is a logical 1. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs. All inputs except the BI/RBO nodes are one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs. Power dissipation is typically 320 milliwatts (ITT5446A, ITT5447A, and ITT-5448).

The ITT5446A, ITT5447A, and ITT5448 are characterized for operation over the full military temperature range of −55°C to 125°C. The ITT-7446A, ITT7447A, and ITT7448, (electrically identical to the corresponding Series 54 types) are for operation over the temperature range of 0°C to 70°C.

TRUTH TABLE ITT5446A, ITT5447A, ITT7446A, ITT7447A

	Inputs							Outputs							
Decimal or Function	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	Note
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

Notes:

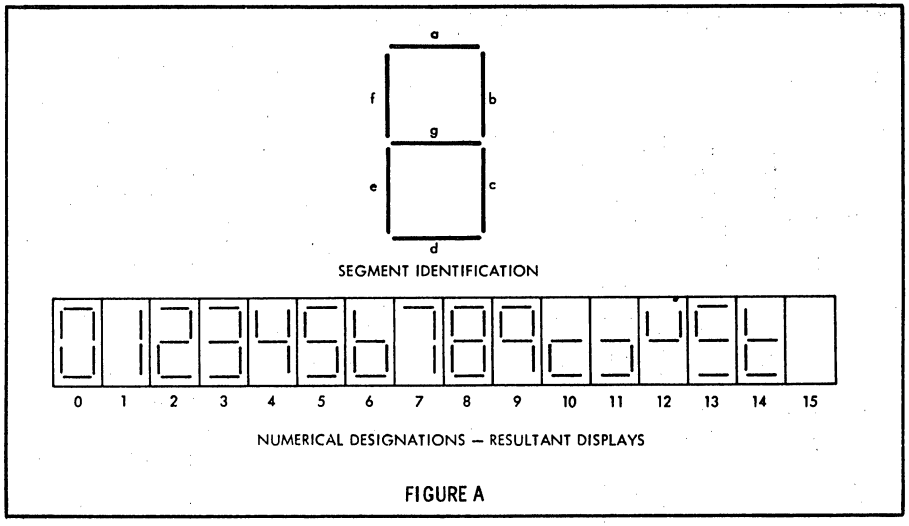
1. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.
2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.
3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test input at logical 1, all segment outputs go to a logical 1 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 0.

TRUTH TABLE ITT5448, ITT7448

	Inputs							Outputs							
Decimal or Function	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	Note
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	3	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

Notes:

1. BI/RBO is wire AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.
2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.
3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test at logical 1, all segment outputs go to a logical 0 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1 , and a logical 0 is applied to the lamp test input, all segment outputs go to a logical 1.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

FIGURE A

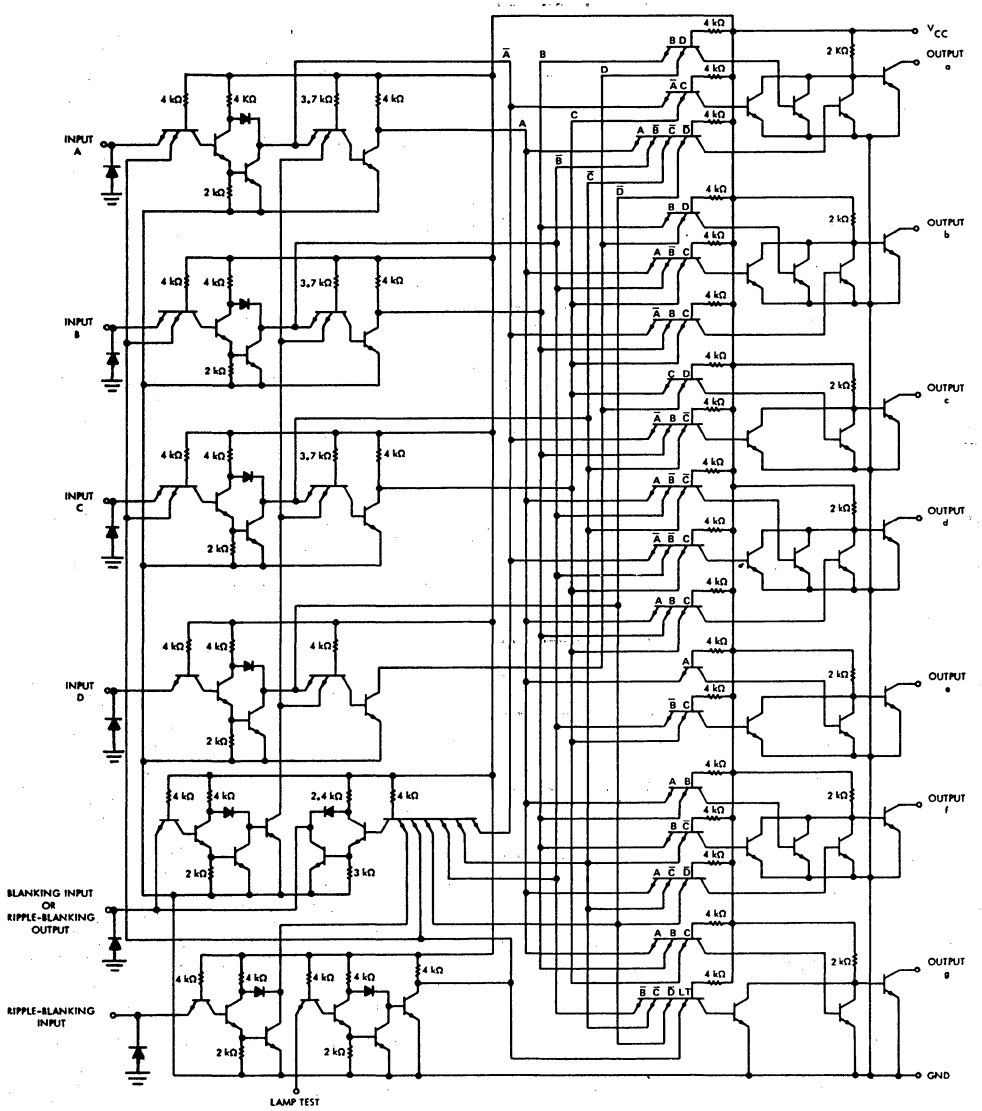
Absolute Maximum Ratings Over Operating Temperature Range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Notes 1 and 2) 5.5V
Current Into any Output of 5446A, 7446A, 5447A, 7447A Circuits (See Note 3) ..... 1 mA
Operating Free Air Temperature Range:
5446A, 5447A, 5448 Circuits ..... —55 C to 125 C
7446A, 7447A, 7448 Circuits ..... 0 C to 70 C
Storage Temperature Range ..... —65 C to 150 C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

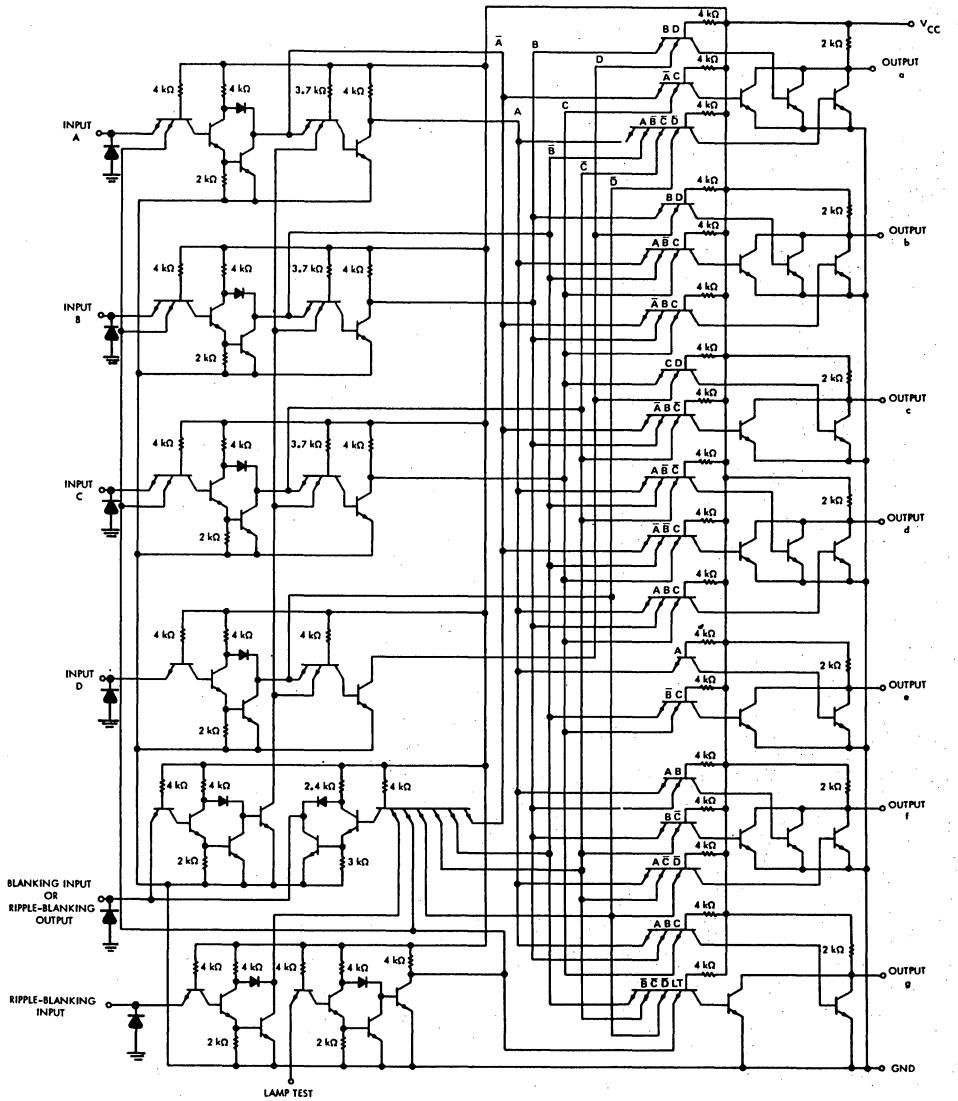
Recommended Operating Conditions	**MIN**	**NOM**	**MAX**	**UNIT**
Supply Voltage V_{CC} (See Note 1):				
5446A, 5447A, 5448	4.5	5	5.5	V
7446A, 7447A, 7448	4.75	5	5.25	V
Continuous Voltage at Outputs a through g:				
5446A, 7446A			30	V
5447A, 7447A			15	V
Normalized Fan-Out From Outputs a through g to Series 54/74 Loads: 5446A, 7446A, 5447A, 7447A			24	
5448, 7448			4	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads: 5446A, 7446A, 5447A, 7447A, 5448			5	
Output Sink Current, I_{sink}:				
5446A, 7446A, 5447A, 7447A Outputs a through g			40	mA
5448, 7448 Outputs a through g			6.4	mA
5446A, 7446A, 5447A, 7447A, 5448, 7448 BI/RBO Node			8	mA

schematic diagram ITT5446A, ITT5447A, ITT7446A, ITT7447A



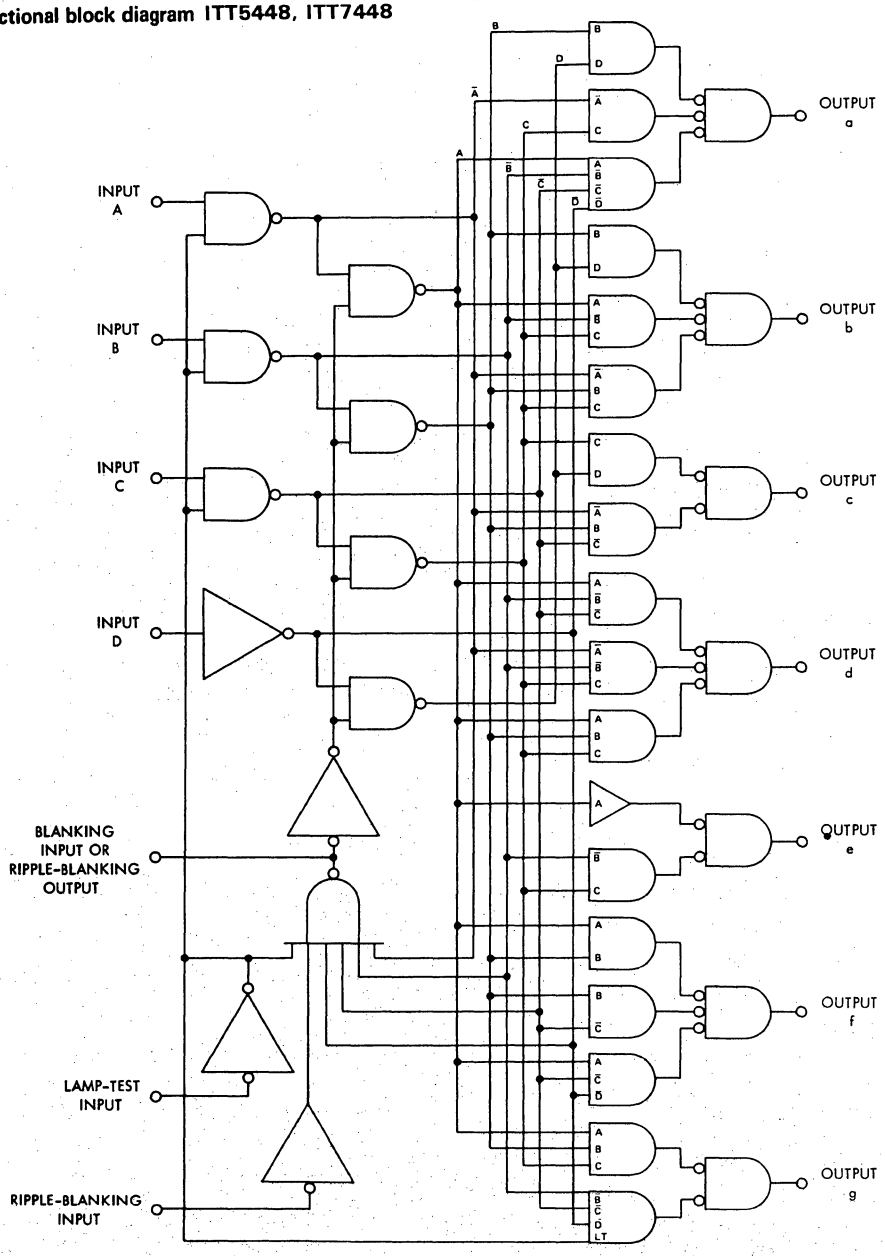
Component values shown are nominal

schematic diagram ITT5448, ITT7448

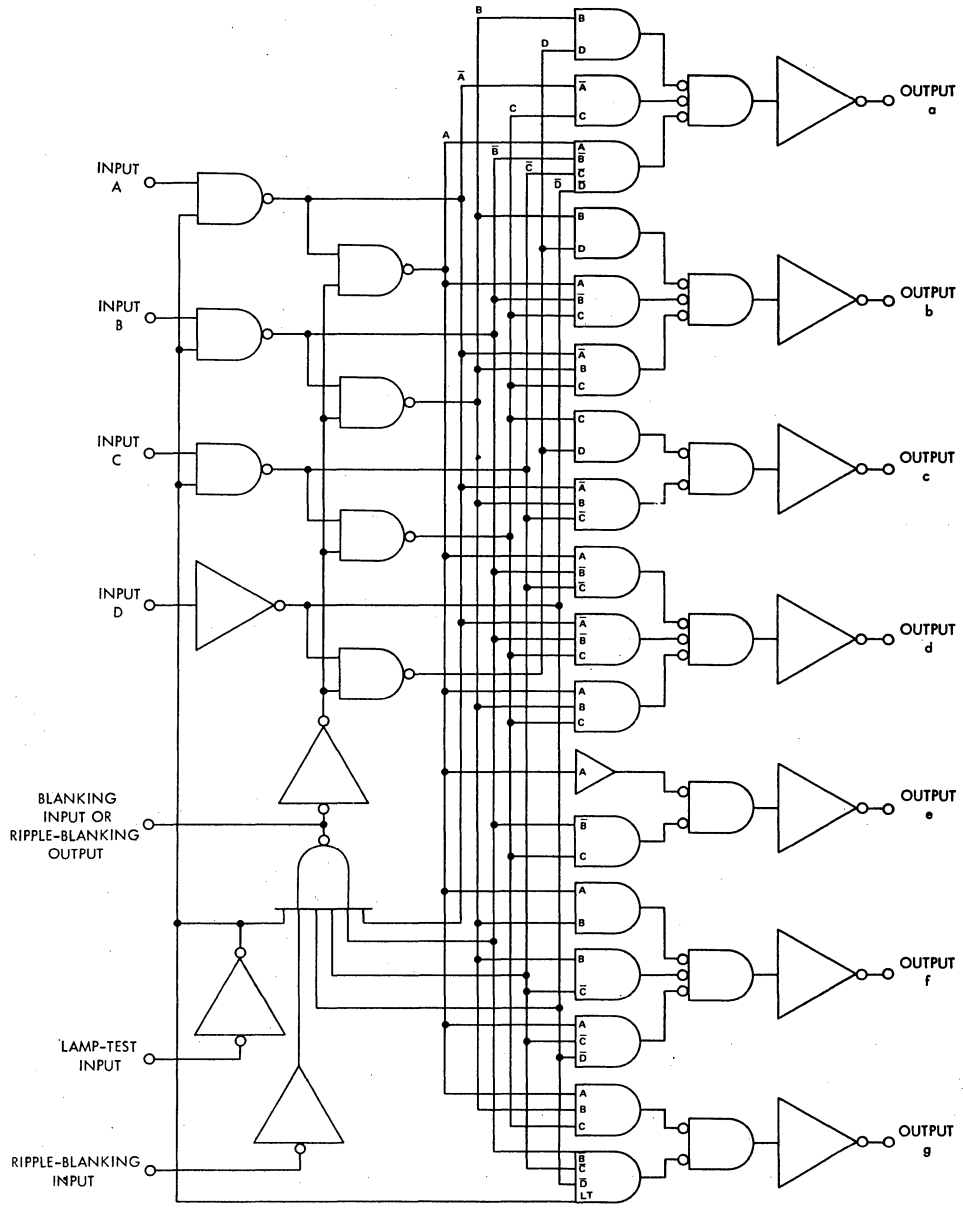


Component values shown are nominal

functional block diagram ITT5448, ITT7448



functional block diagrams ITT5446A, ITT5447A, ITT7446A, ITT7447A



Electrical Characteristics Over Recommended Operating Free-air Temperature Range
(unless otherwise noted)

	Parameter		Min	Typ‡	Max	Unit	Test Conditions†
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_I	Input clamp voltage, any input except BI/RBO				−1.5	V	V_{CC} = MIN, I_I = −10mA
V_{OH}	High-level output voltage	BI/RBO	2.4	3.7		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −200μA
V_{OL}	Low-level output voltage	BI/RBO		0.3	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 8mA
$I_{O(off)}$	Off-state output current	a thru g			250	μA	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, $V_{O(off)}$ = MAX
$V_{O(on)}$	On-state output voltage	a thru g		0.3	0.4	V	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, $I_{O(on)}$ = 40mA
I_I	Input current at maximum input voltage	Any input except BI/RBO			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current	Any input except BI/RBO			40	μA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current	Any input except BI/RBO			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
		BI/RBO			−4		
I_{OS}	Short-circuit output current	BI/RBO			−4	mA	V_{CC} = MAX
I_{CC}	Supply current			64	85	mA	V_{CC} = MAX, 5446A,5447A
				61	103		See Note 2, 7446A,7447A

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at V_{CC} = 5V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

Parameter		Test Conditions	Min	Typ	Max	Unit
t_{off}	Turn-off time from A input	C_L = pF, R_L = 120Ω			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

Electrical Characteristics Over Recommended Operating Free-air Temperature Range
(unless otherwise noted)

	Parameter		Min	Typ‡	Max	Unit	Test Conditions†	
V_{IH}	High-level input voltage						2 V	
V_{IL}	Low-level input voltage						0.8 V	
V_I	Input clamp voltage, any input except BI/RBO				−1.5	V	V_{CC} = MIN, I_I = −10mA	
V_{OH}	High-level output voltage	a thru g	2.4	4.2		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	
		BI/RBO	2.4	3.7				
I_O	Output current	a thru g	−1.3	−2		mA	V_{CC} = MIN, V_O = 0.85V, Input conditions as for V_{OH}	
V_{OL}	Low-level output voltage			.27	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX	
I_I	Input current at maximum input voltage	Any input except BI/RBO			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current	Any input except BI/RBO			40	μA	V_{CC} = MAX, V_I = 2.4V	
I_{IL}	Low-level input current	Any input except BI/RBO			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
					−4			
I_{OS}	Short-circuit output current	BI/RBO			−4	mA	V_{CC} = MAX	
I_{CC}	Supply current			53	76	mA	V_{CC} = MAX, See Note 2	5448
				53	90			7448

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at V_{CC} = 5V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

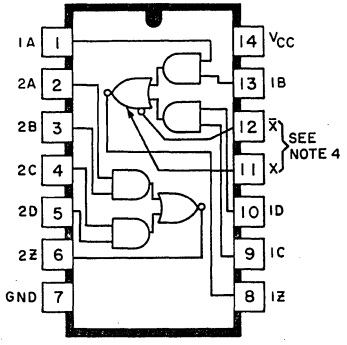
Switching Characteristics, V_{CC} = 5V, T_A = 25°C

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PHL}	Propagation delay time, high-to-low-level output from A input			100	ns	C_L = 15 pF, 5448: R_L = 1kΩ 7448: R_L = 677 Ω
t_{PLH}	Propagation delay time, low-to-high-level output from A input			100		
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input			100	ns	
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input			100		

ITT SEMICONDUCTORS

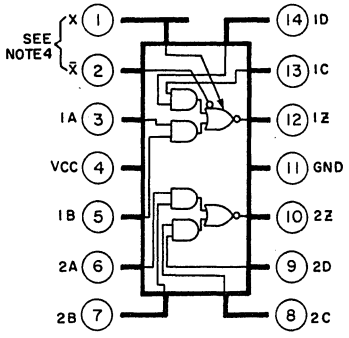
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



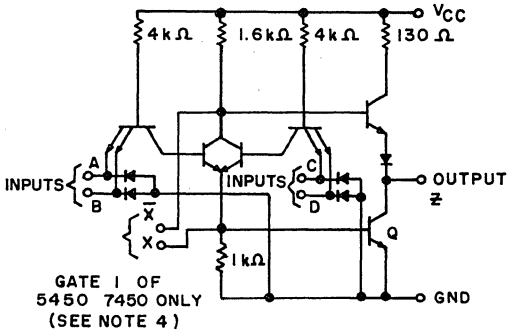
POSITIVE LOGIC:
$\bar{Z} = \overline{(AB)+(CD)+(X)}$
X = OUTPUT OF ITT5460/ITT7460

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
$\bar{Z} = \overline{(AB)+(CD)+(X)}$
X = OUTPUT OF ITT5460/ITT7460

schematic (each gate)



Notes:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and X̄ pins open.
4. Make no external connection to X and X̄ pins of the ITT5451 and ITT7451.
5. A total of four expander gates can be connected to the expander inputs.

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	ITT5450, ITT5451 Circuits	4.5	5	5.5	V
	ITT7450, ITT7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	ITT5450, ITT5451 Circuits	−55	25	125	°C
	ITT7450, ITT7451 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	2			V		
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8V, I_{load} = −400uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16mA	
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT5450, ITT5451
		−18		−55			ITT7450, ITT7451
$I_{CC(0)}$	Logical 0 level supply current		7.4	14	mA	V_{CC} = MAX, V_{in} = 5V	
$I_{CC(1)}$	Logical 1 level supply current		4	8	mA	V_{CC} = MAX, V_{in} = 0	

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X are open.

[3] Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (ITT5450 circuits) using expander inputs, $V_{CC} = 4.5V, T_A = -55°C$

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions
I_X	Expander current			2.9	mA	$V_1 = 0.4V, I_{sink} = 16mA$
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)			1.1	V	$I_{sink} = 16mA, I_1 = 0.41mA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	$I_{load} = -400uA, I_1 = 0.15mA, I_2 = -0.15mA$
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	$I_{sink} = 16mA, I_1 = 0.3mA, R_1 = 138\Omega$

ELECTRICAL CHARACTERISTICS (ITT7450 circuits) using expander inputs, $V_{CC} = 4.75V, T_A = 0°C$

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions
I_X	Expander current			3.1	mA	$V_1 = 0.4V, I_{sink} = 16mA$
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)			1	V	$I_{sink} = 16mA, I_1 = 0.62mA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	$I_{load} = -400uA, I_1 = 270uA, I_2 = -270uA$
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	$I_{sink} = 16mA, I_1 = 0.43mA, R_1 = 130\Omega$

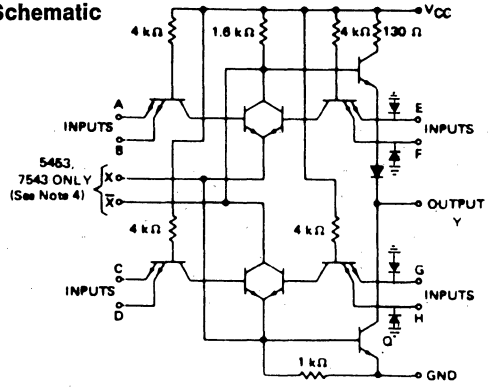
SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25°C, N = 10$

	Parameter	Min	Typ	Max	Unit	Test Conditions [2]
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	$C_L = 15\ pF, R_L = 400\Omega$
t_{pd1}	Propagation delay time to logical 1 level		13	22	ns	$C_L = 15\ pF, R_L = 400\Omega$

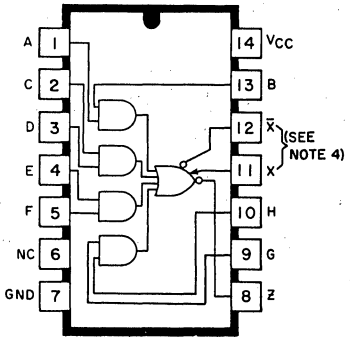
[1] All typical values are at $V_{CC} = 5V, T_A = 25°C$.
[2] Expander pins X and X are open.

EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES

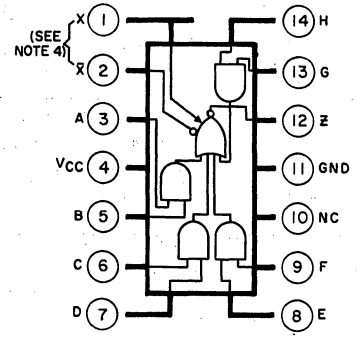
Schematic



DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
$\bar{Z} = \overline{(AB)+(CD)+(EF)+(GH)+(X)}$
X = OUTPUT OF ITT5460/ITT7460

Notes:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X pins open.
4. Make no external connection to X and X pins of the ITT5454 and ITT7454.
5. A total of four expander gates can be connected to the expander inputs.
6. NC—No Internal Connection.

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	ITT5453, ITT5454 Circuits	4.5	5	5.5	V
	ITT7453, ITT7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N				10	
Operating Free-Air Temperature Range, T_A:	ITT5453, ITT5454 Circuits	−55	25	125	°C
	ITT7453, ITT7454 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, V_{in} = 0.8V, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16mA
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = 5.5V, ITT5453, ITT5454
		−18		−55		ITT7453, ITT7454
$I_{CC(0)}$	Logical 0 level supply current		5.1	9.5	mA	V_{CC} = MAX, V_{in} = 5V
$I_{CC(1)}$	Logical 1 level supply current			8	mA	V_{CC} = MAX, V_{in} = 0

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X are open.
[3] Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (ITT5453 circuits) using expander inputs, V_{CC} = 4.5V, T_A = −55°C

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
I_X	Expander current			2.9	mA	V_I = 0.4V, I_{sink} = 16mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)			1.1	V	I_{sink} = 16mA, I_i = 0.41mA, R_1 = 0
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	I_{load} = −400 uA, I_1 = 0.15mA, I_2 = −0.15mA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	I_{sink} = 16mA, I_1 = 0.3mA, R_1 = 138 Ω

ELECTRICAL CHARACTERISTICS (ITT7453 circuits) using expander inputs, $V_{CC} = 4.75V, T_A = 0°C$

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
I_X	Expander current			3.1	mA	$V_1 = 0.4V, I_{sink} = 16mA$
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)			1	V	$I_{sink} = 16mA, I_1 = 0.62mA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4	33		V	$t_{load} = -400\ uA, I_1 = 270\ uA, I_2 = -270\ uA$
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	$I_{sink} = 16mA, I_1 = 0.43mA, R_1 = 130\ \Omega$

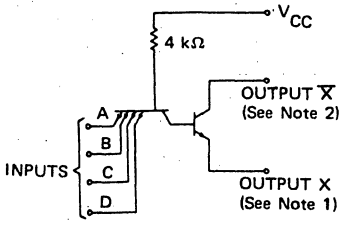
SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25°C, N = 10$

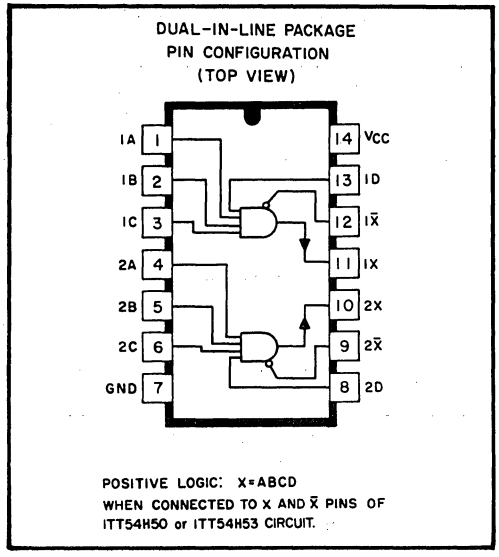
Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
t_{pd0}	Propagation delay time to logical 0 level		8	15	ns	$C_L = 15\ pF, R_L = 400\ \Omega$
t_{pd1}	Propagation delay time to logical 1 level		13	22	ns	$C_L = 15\ pF, R_L = 400\ \Omega$

[1] All typical values are at $V_{CC} = 5V, T_A = 25°C$.
[2] Expander inputs X and X are open.

DUAL 4-INPUT EXPANDER

schematic (each expander)

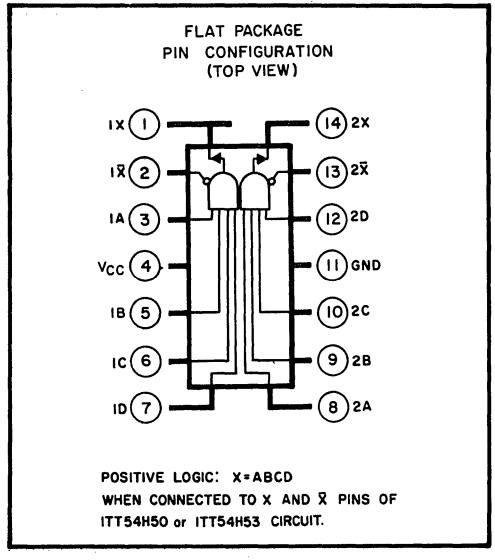




Notes:
1. Connect to X input of ITT5450/ITT7450 or ITT7453 circuit.
2. Connect to $\overline{X}$ input of ITT5450/ITT7450 or ITT7453 circuit.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} ..... 4.75V to 5.25V
Maximum number of expanders that may be fanned-in to one ITT5450/ITT7450 or one ITT5453/ITT7453 4



ELECTRICAL CHARACTERISTICS ITT7460 (unless otherwise noted T_A = 0°C to 70°C)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals is in the on state	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal is in the off state			0.8	V	
V_{on}	On-state output voltage			0.4	V	V_{CC} = 4.75V, V_{in} = 2V, V_1 = 1V, R = 1.1 kΩ, T_A = 0°C
I_{off}	Off-state output current			270	uA	V_{CC} = 4.75V, V_{in} = 0.8V, V_1 = 4.5V, R = 1.2 kΩ, T_A = 0°C
I_{on}	On-state output current	−0.43			mA	V_{CC} = 4.75V, V_{in} = 2V, V_1 = 1V
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = 5.25V, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = 5.25V, V_{in} = 2.4V
				1	mA	V_{CC} = 5.25V, V_{in} = 5.5V
$I_{CC(on)}$	On-state supply current		1.2	2.5	mA	V_{CC} = 5.25V, V_{in} = 5V V_1 = 0.85V
$I_{CC(off)}$	Off-state supply current		2	4	mA	V_{CC} = 5.25V, V_{in} = 0, V_1 = 0.85V

ELECTRICAL CHARACTERISTICS ITT5460 (unless otherwise noted $T_A = -55°C$ to $125°C$)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state			0.8	V	
V_{on}	On-state output voltage			0.4	V	$V_{CC} = 4.5V$, $V_{in} = 2V$, $V_1 = 1V$, $R = 1.1\ k\Omega$, $T_A = -55°C$
I_{off}	Off-state output current			150	uA	$V_{CC} = 4.5V$, $V_{in} = 0.8V$, $V_1 = 4.5V$, $R = 1.2\ k\Omega$, $T_A = -55°C$
I_{on}	On-state output current	−0.3			mA	$V_{CC} = 4.5V$, $V_{in} = 2V$, $V_1 = 1V$, $T_A = -55°C$
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	$V_{CC} = 5.5V$, $V_{in} = 0.4V$
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	$V_{CC} = 5.5V$, $V_{in} = 2.4V$
				1	mA	$V_{CC} = 5.5V$, $V_{in} = 5.5V$
$I_{CC(on)}$	On-state supply current		1.2	2.5	mA	$V_{CC} = 5.5V$, $V_{in} = 5V$, $V_1 = 0.85V$
$I_{CC(off)}$	Off-state supply current		2	4	mA	$V_{CC} = 5.5V$, $V_{in} = 0$, $V_1 = 0.85V$

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25°C$, $N = 10$

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level (through ITT5450 or ITT5453 circuit)		10	20	ns	$C_L = 15\ pF$, $R_L = 400\Omega$
t_{pd1}	Propagation delay time to logical 1 level (through ITT5450 or ITT5453 circuit)		15	30	ns	$C_L = 15\ pF$, $R_L = 400\Omega$

[1] All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

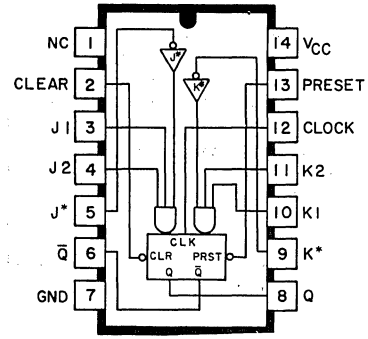
EDGE-TRIGGERED J-K FLIP-FLOPS

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

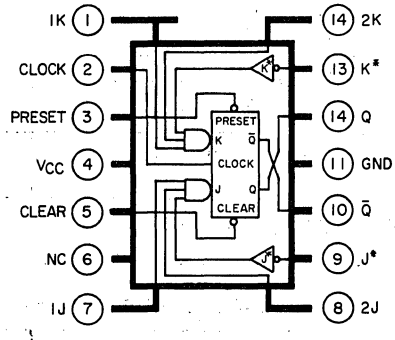
Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed application and can result in a significant saving in system power dissipation and package count where input gating is required.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:

LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET OR CLEAR FUNCTION CAN OCCUR ONLY WHEN CLOCK INPUT IS LOW.

logic

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Notes: 1. $J = J1 \cdot J2 \cdot \overline{J^*}$
2. $K = K1 \cdot K2 \cdot \overline{K^*}$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J* or K* are not used they must be grounded.
6. NC - No Internal Connection

recommended operating conditions	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: ITT5470 Circuits	4.5	5	5.5	V
ITT7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: ITT5470 Circuits	−55	25	125	°C
ITT7470 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 68)	5		150	ns
Width of Clock Pulse, $t_{p(clock)}$	20			ns
Width of Preset Pulse, $t_{p(prese}$	25			ns
Width of Clear Pulse, $t_{p(clear)}$	25			ns

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16 mA
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at preset or clear			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock			40	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{in(1)}$	Logical 1 level input current at preset or clear			80	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{in} = 0 — ITT5470
		−18		−57		ITT7470
I_{CC}	Supply current		13	26	mA	V_{CC} = MAX, V_{in} = 5 V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

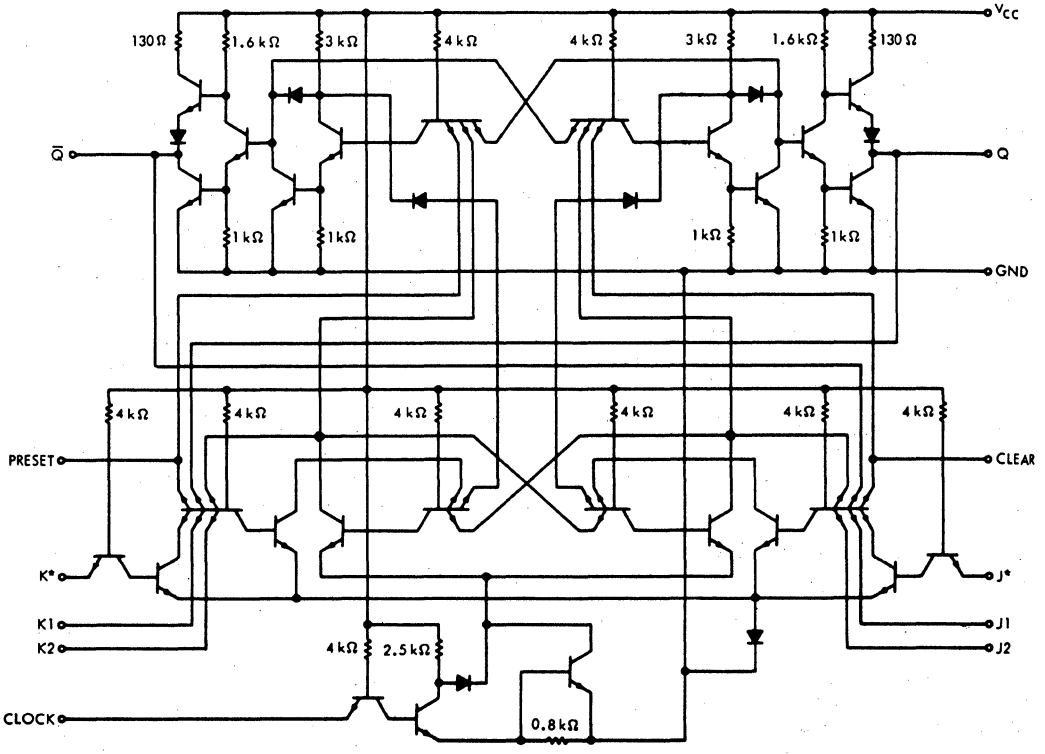
Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	20	35		MHz	C_L = 15 pF, R_L = 400 Ω
t_{setup}	Minimum input setup time		10	20	ns	C_L = 15 pF, R_L = 400 Ω
t_{hold}	Minimum input hold time		0	5	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output			50	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output			50	ns	C_L = 15 pF, R_L = 400 Ω

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 **(continued)**

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd1}	Propagation delay time to logical 1 level from clock to output	10	27	50	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	18	50	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

schematic

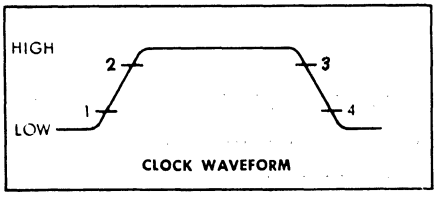


NOTE: Component values shown are nominal.

J-K MASTER-SLAVE FLIP-FLOPS

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



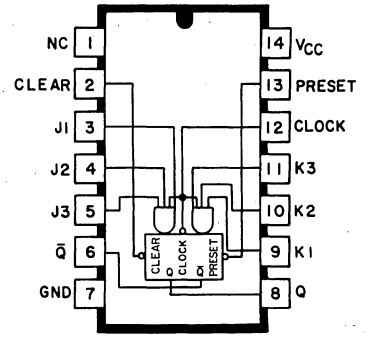
CLOCK WAVEFORM

TRUTH TABLE

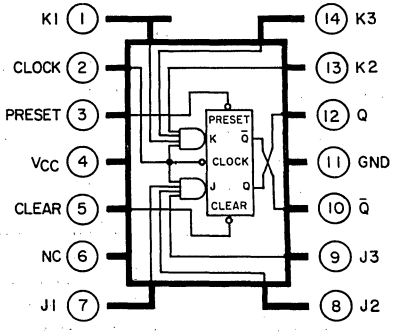
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Notes:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:

LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET OR CLEAR ARE INDEPENDENT OF CLOCK

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: ITT5472 Circuits	4.5	5	5.5	V
ITT7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: ITT5472 Circuits	−55	25	125	°C
ITT7472 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

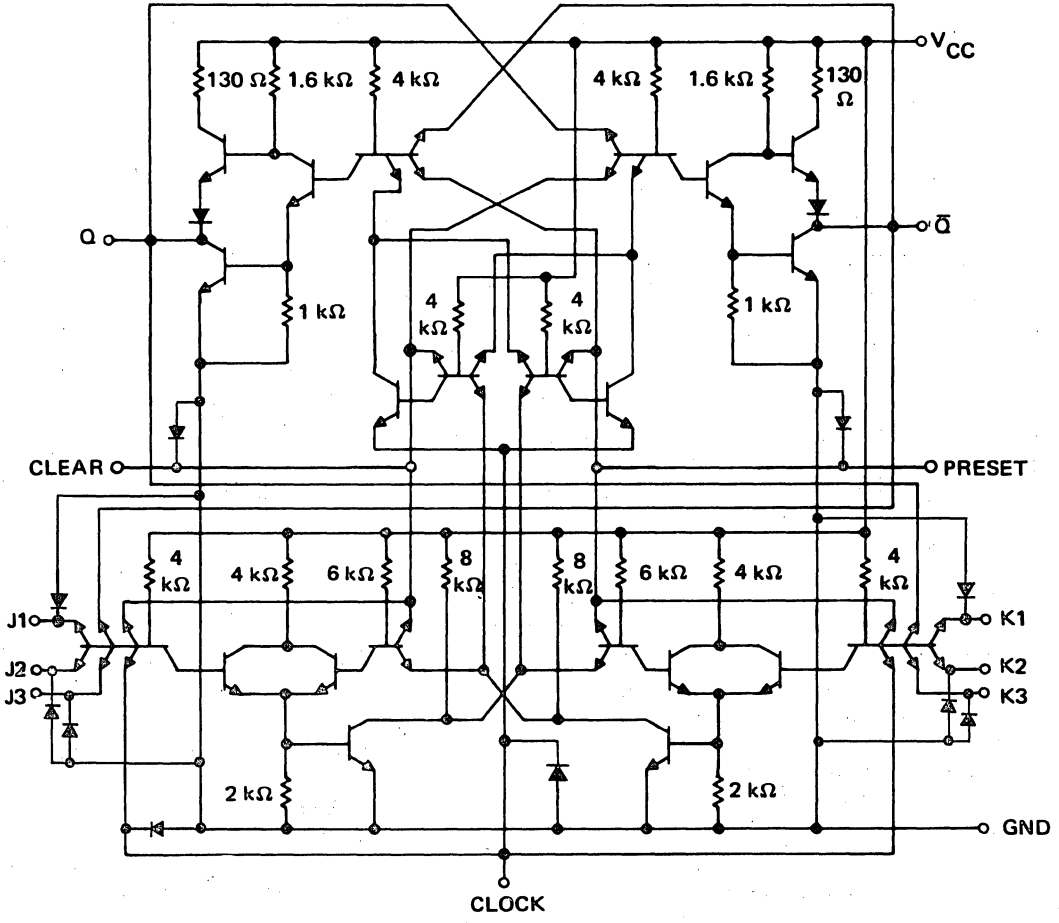
	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16mA
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3			40 1	uA mA	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock			80 1	uA mA	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−20 −18		−57 −57	mA	V_{CC} = MAX, V_{in} = 0 — ITT5472 ITT7472
I_{CC}	Supply current		10	20	mA	V_{CC} = MAX, V_{in} = 5V

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	15	20		MHz	C_L = 15pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output		16	25	ns	C_L = 15pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output		25	40	ns	C_L = 15pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	10	16	25	ns	C_L = 15pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	25	40	ns	C_L = 15pF, R_L = 400 Ω

schematic

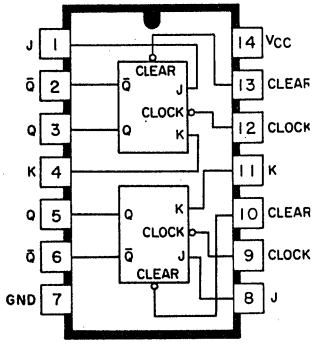


Note: Component values shown are nominal.

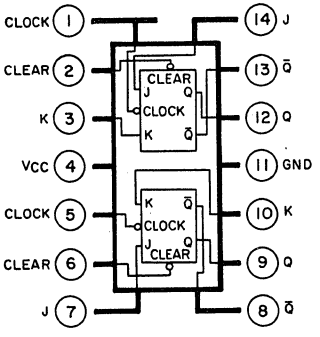
DUAL J-K MASTER-SLAVE FLIPS-FLOPS

ITT5473, ITT7473

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)

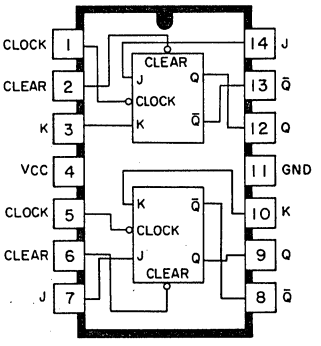


FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



ITT54107, ITT74107

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0.
CLEAR IS INDEPENDENT OF CLOCK.

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

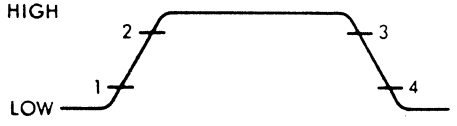
1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE
(Each Flip-Flop)

t_n		t_{n+1}
J	**K**	**Q**
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Notes: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	ITT5473, ITT54107			ITT7473, ITT74107			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 69)	20			20			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 70)	25			25			ns
Input setup time, t_{setup} (See Figure 69)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

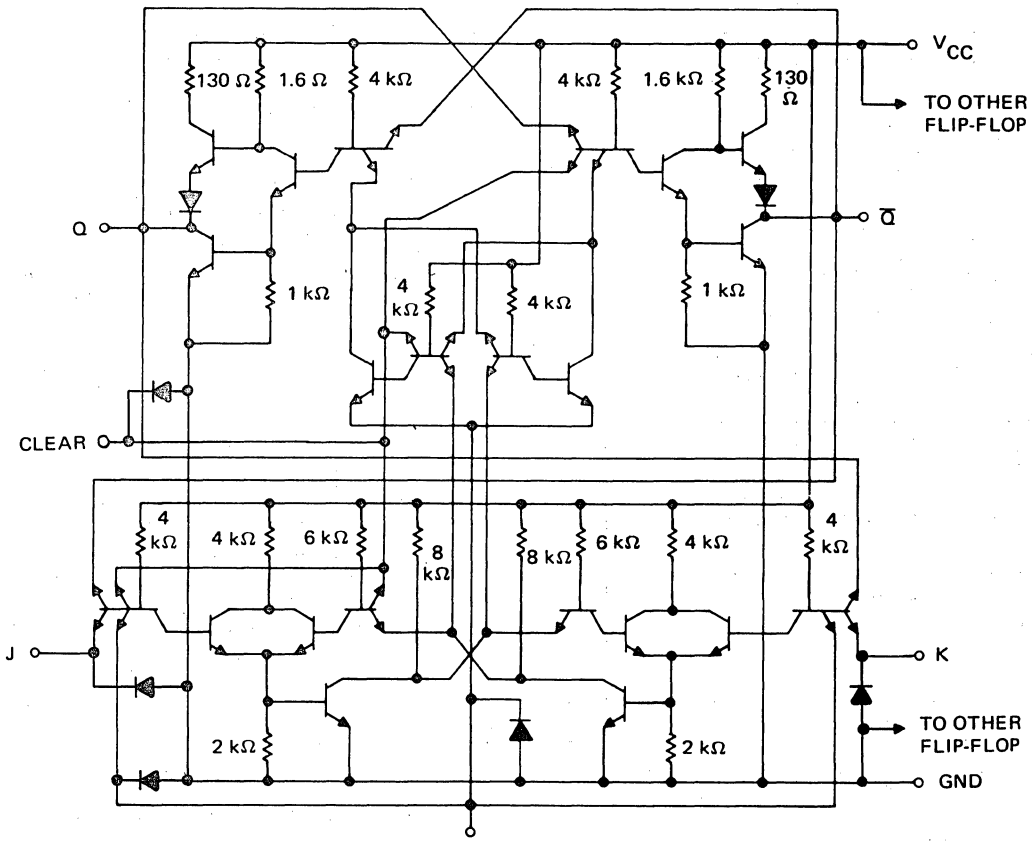
Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16mA	
$I_{in(0)}$	Logical 0 level input current at J or K			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at clear or clock			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at J or K			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at clear or clock			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short circuit output current [3]		−20	−57	mA	V_{CC} = MAX, V_{in} = 0	ITT5473, 54107
			−18	−57			ITT7473, 74107
I_{CC}	Supply current		20	40	mA	V_{CC} = MAX	

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	15	20		MHz	C_L = 15pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear to output		16	25	ns	C_L = 15pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear to output		25	40	ns	C_L = 15pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	10	16	25	ns	C_L = 15pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	25	40	ns	C_L = 15pF, R_L = 400 Ω

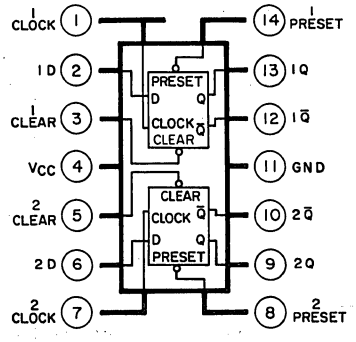
schematic (each flip-flop)



Note: Component values shown are nominal.

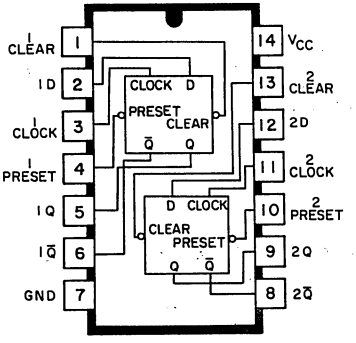
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

description

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

These dual flip-flops have the same clocking characteristics as the ITT5470/ITT7470 gated (edge-triggered) flip-flop circuits, and both are ideally suited for medium-to-high-speed applications. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

logic

TRUTH TABLE
(Each Flip-Flop)

t_n	$t_n + 1$	
Input	**Output**	**Output**
D	Q	$\overline{Q}$
0	0	1
1	1	0

Notes: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

recommended operating conditions

	ITT5474			ITT7474			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 71)	30			30			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 67)	30			30			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 67)	30			30			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

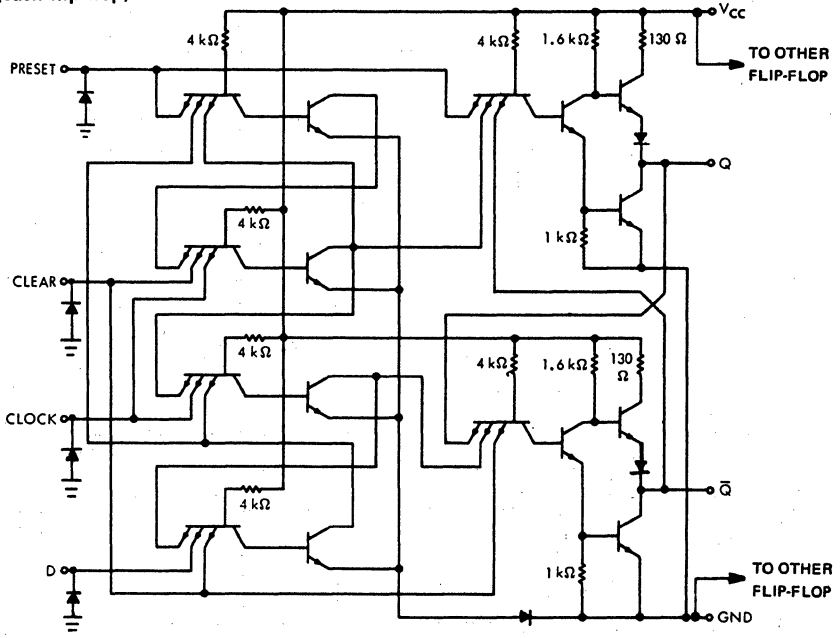
Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400 uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16 mA	
$I_{in(0)}$	Logical 0 level input current at preset or D			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at clear or clock			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at D			40	µA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at preset or clock			80	µA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at clear			120	µA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{in} = 0	ITT5474
		−18		−57			ITT7474
I_{CC}	Supply current		17	30	mA	V_{CC} = MAX	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	15	25		MHz	C_L = 15 pF, R_L = 400 Ω
t_{setup}	Minimum input setup time		15	20	ns	C_L = 15 pF, R_L = 400 Ω
t_{hold}	Minimum input hold time		2	5	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output			25	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output			40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	10	14	25	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	20	40	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

schematic (each flip-flop)



NOTE: Component values shown are nominal.

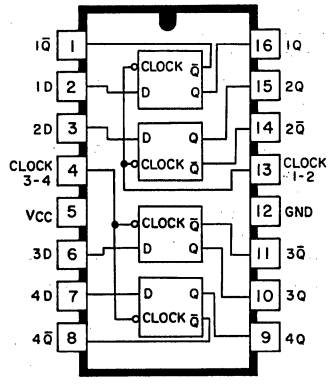
4-BIT BISTABLE LATCHES

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The ITT5475/ITT7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages.

These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

logic

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

Notes: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3) ..... 7 V
Input Voltage, V_{in} (See Notes 3 and 4) ..... 5.5 V
Operating Free-Air Temperature Range:
ITT5475 ..... −55°C to 125°C
ITT7475 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): ITT5475	4.5	5	5.5	V
ITT7475	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	

Note: 3. These voltages are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal			0.8	V		
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −400 uA	
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 16 mA	
$I_{in(0)}$	Logical 0 level input current at D			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at clock			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at D			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at clock			160	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{out} = 0	ITT5475
		−18		−57	mA		ITT7475
I_{CC}	Supply current		32	46	mA	V_{CC} = MAX,	ITT5475
			32	53	mA		ITT7475

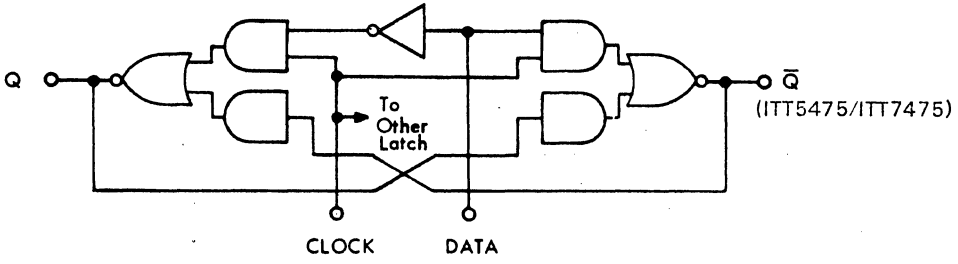
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

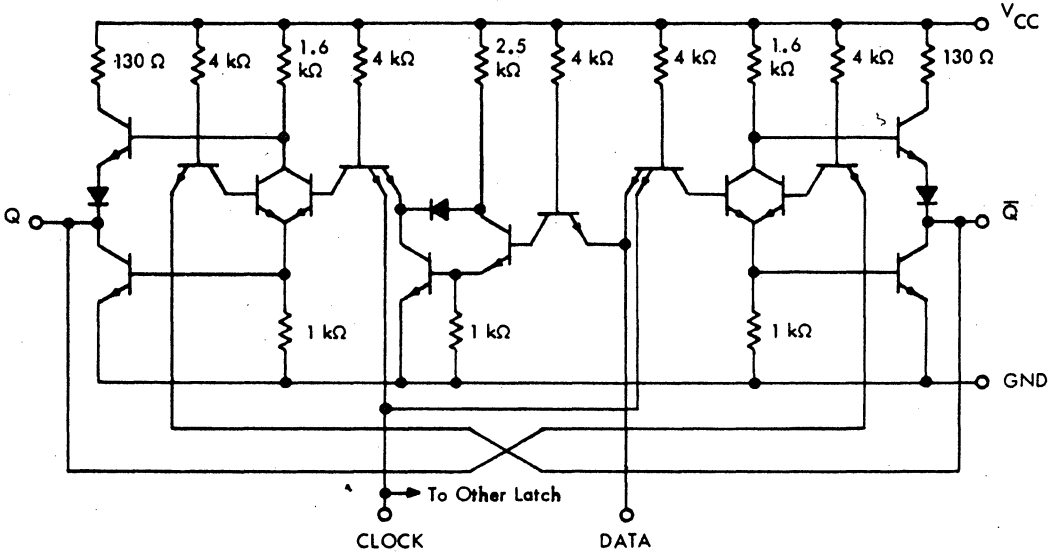
Parameter		Min	Typ	Max	Unit	Test Conditions
t_{setup1}	Minimum logical 1 level input setup time at D input		7	20	ns	C_L = 15 pF, R_L = 400 Ω
t_{setup0}	Minimum logical 0 level input setup time at D input		14	20	ns	C_L = 15 pF, R_L = 400 Ω
t_{hold1}	Maximum logical 1 level input hold time required at D input	0	15 [1]		ns	C_L = 15 pF, R_L = 400 Ω
t_{hold0}	Maximum logical 0 level input hold time required at D input	0	6 [1]		ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output		16	30	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output		14	25	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output		24	40	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output		7	15	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output		16	30	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output		7	15	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output		16	30	ns	C_L = 15 pF, R_L = 400 Ω
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output		7	15	ns	C_L = 15 pF, R_L = 400 Ω

[1] These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

functional block diagram (each latch)



schematic (each latch)



Note: Component values shown are nominal.

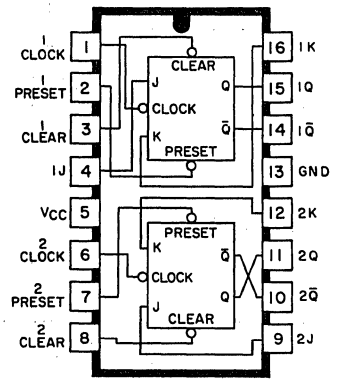
ITT SEMICONDUCTORS

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

The ITT7476 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



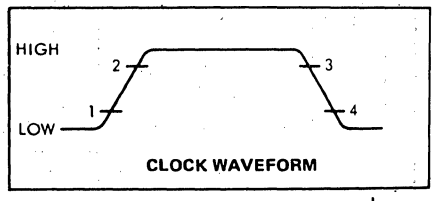
POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
CLEAR AND PRESET ARE INDEPENDENT OF CLOCK

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Notes: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



CLOCK WAVEFORM

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	ITT5476 Circuits	4.5	5	5.5	V
	ITT7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	ITT5476 Circuits	−55	25	125	°C
	ITT7476 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			ns

ITT5476, ITT7476
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

ELECTRICAL CHARACTERISTICS, T_A = 0°C to 70°C (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16mA	
$I_{in(0)}$	Logical 0 level input current at J or K			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at J or K			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{in} = 0	ITT5476
		−18		−57			ITT7476
I_{CC}	Supply current (each flip-flop)		20	40	mA	V_{CC} = MAX	

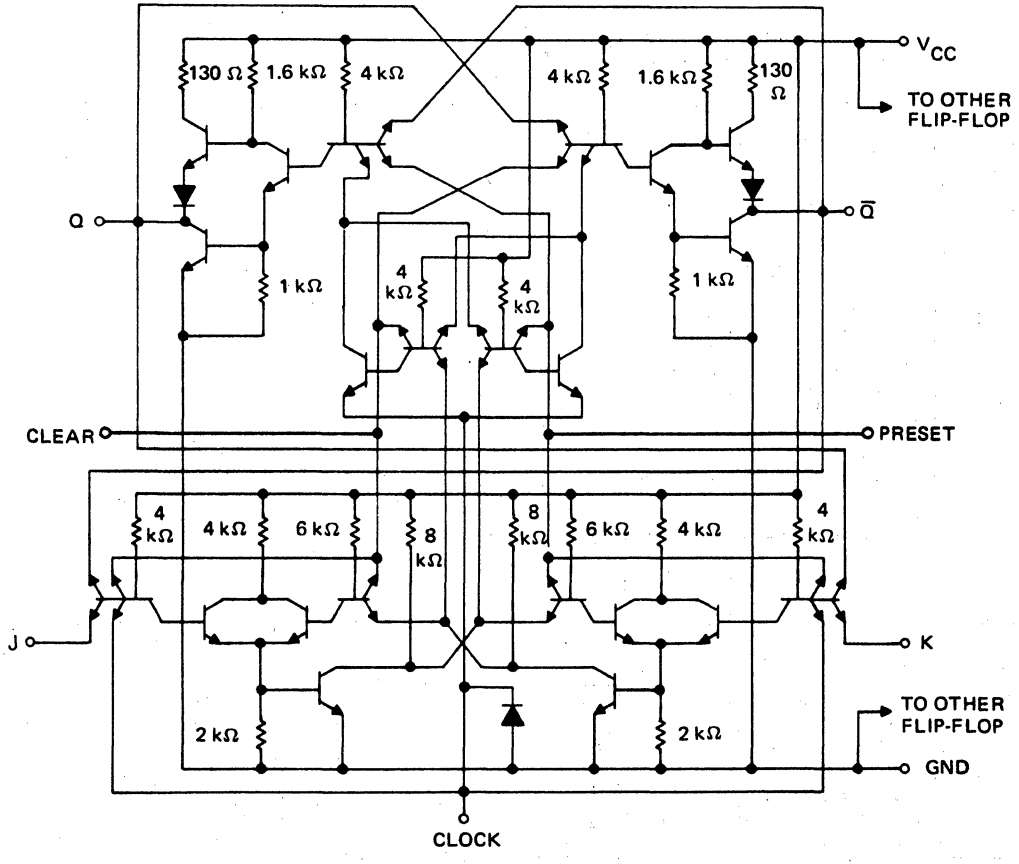
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	15	20		MHz	C_L = 15 pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output		16	25	ns	C_L = 15 pF, R_L = 400Ω
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output		25	40	ns	C_L = 15 pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	10	16	25	ns	C_L = 15 pF, R_L = 400Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	25	40	ns	C_L = 15 pF, R_L = 400Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

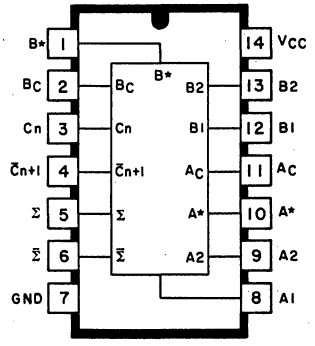


Note: Component values shown are nominal.

schematic (each flip-flop)

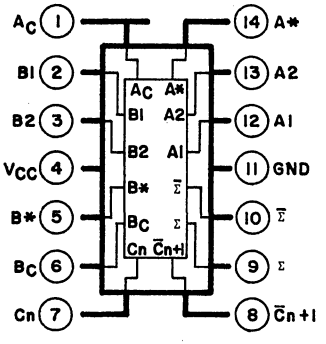
GATED FULL ADDERS

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE FUNCTION TABLE

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE FUNCTION TABLE

These single-bit, high-speed, binary full adders with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output are designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. These circuits (see schematic) utilize diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs and are entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) 7V
Input voltage (see Note 5) 5.5V
Operating free-air temperature range:
ITT5480 ..... −55°C to 125°C
ITT7480 ..... 0° to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 4. Voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

logic

FUNCTION TABLE
(See Notes 1, 2, and 3)

Inputs			Outputs		
C_n	B	A	C_{n+1}	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = high level, L = low level

Notes: 1. $A = \overline{A}_C + \overline{A}^* + A1 \cdot A2$,
$B = \overline{B}_C + \overline{B}^* + B1 \cdot B2$.
2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

RECOMMENDED OPERATING CONDITIONS

		ITT5480			ITT7480			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Σ or $\overline{\Sigma}$			−400			−400	μA
	$\overline{C}_{n+1}$			−200			−200	
	A* or B*			−120			−120	
Low-level output current, I_{OL}	Σ or $\overline{\Sigma}$			16			16	mA
	$\overline{C}_{n+1}$			8			8	
	A* or B*			4.8			4.8	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			ITT5480 Min	ITT5480 Typ[1]	ITT5480 Max	ITT7480 Min	ITT7480 Typ[1]	ITT7480 Max	Unit	Test Conditions[2]	
V_{IH}	High-level input voltage		2			2			V		
V_{IL}	Low-level input voltage				0.8			0.8	V		
V_{OH}	High-level output voltage	Σ or $\overline{\Sigma}$	2.4	3.5		2.4	3.5		V	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V	I_{OH} = −400uA
		$\overline{C}_n+1$									I_{OH} = −200uA
		A* or B*									I_{OH} = −120uA
V_{OL}	Low-level output voltage	Σ or $\overline{\Sigma}$		0.22	0.4		0.22	0.4	V	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V	I_{OL} = 16mA
		$\overline{C}_n+1$									I_{OL} = 8mA
		A* or B*									I_{OL} = 4.8mA
I_I	Input current at maximum input voltage				1			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current	A_1, A_2, B_1, B_2, A_C, or B_C			15			15	uA	V_{CC} = MAX, V_I = 2.4V	
		A* or B*		−1.1			−1.1				
		C_n			200			200			
I_{IL}	Low-level input current	A_1, A_2, B_1, B_2, A_C, or B_C			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
		A* or B*			−2.6			−2.6			
		C_n			−8			−8			
I_{OS}	Short-circuit output-current[3]	Σ or $\overline{\Sigma}$	−20		−57	−18		−57	mA	V_{CC} = MAX	
		$\overline{C}_n+1$	−20		−70	−18		−70			
		A* or B*	−0.9		−2.9	−0.9		−2.9			
I_{CC}	Supply current			21	31		21	35	mA	V_{CC} = MAX, See Note 6	

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type
[3] Not more than one output should be shorted at a time.

Note: 6. I_{CC} is measured with all inputs and outputs open.

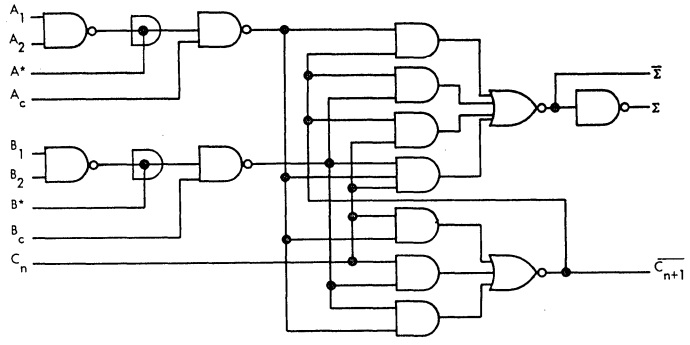
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	C_n	$\overline{C}_{n+1}$		13	17	ns	C_L = 15pF, R_L = 780Ω
t_{PHL}				8	12		
t_{PLH}	B_C	$\overline{C}_{n+1}$		18	25	ns	C_L = 15pF, R_L = 780Ω
t_{PHL}				38	55		
t_{PLH}	A_C	Σ		52	70	ns	C_L = 15pF, R_L = 400Ω
t_{PHL}				62	80		
t_{PLH}	B_C	$\overline{\Sigma}$		38	55	ns	C_L = 15pF, R_R = 400Ω
t_{PHL}				56	75		
t_{PLH}	A_1	A*		48	65	ns	C_L = 15pF, See Note 7
t_{PHL}				17	25		
t_{PLH}	B_1	B*		48	65	ns	C_L = 15pF, See Note 7
t_{PHL}				17	25		

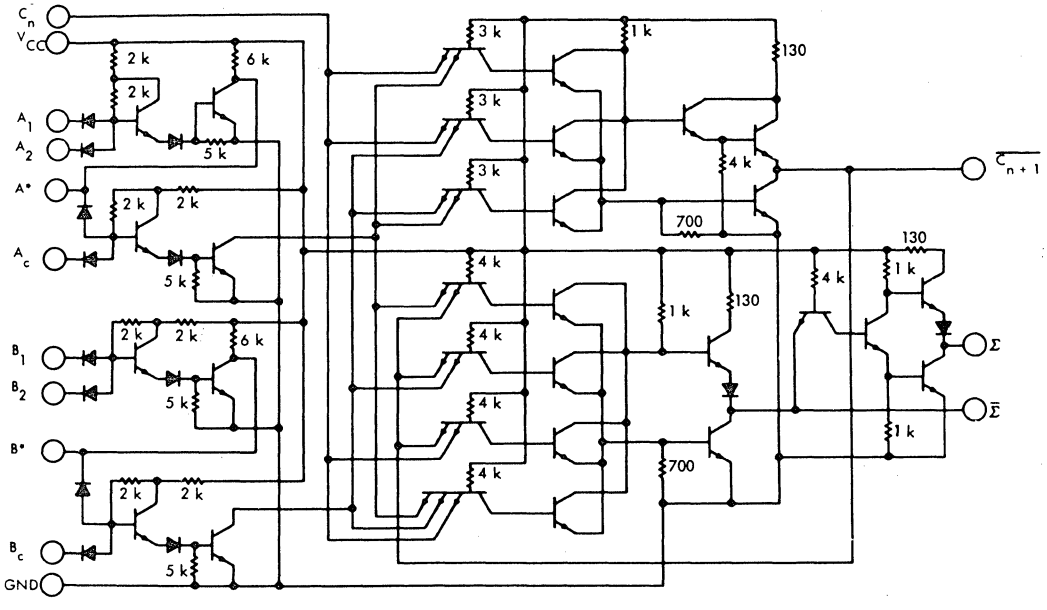
[1] t_{PLH} propagation delay time, low-to-high-level output
t_{PHL} propagation delay time, high-to-low-level output

Note: 7: The load for testing outputs A* and B* consists only of capacitance C_L to ground.

functional block diagram



schematic



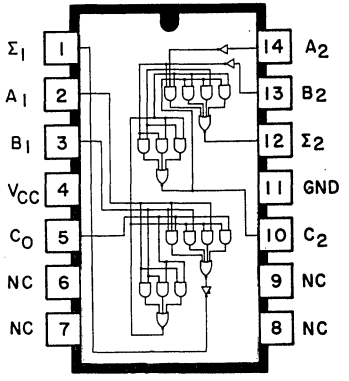
MSI 2-BIT BINARY FULL ADDERS

A HIGH-SPEED TTL 2-BIT FULL ADDER FOR APPLICATION IN

- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

NC-No Internal Connection

logic

TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Notes 1 and 2) 5.5V
Operating Free-Air Temperature Range:
ITT5482 Circuits ..... −55°C to 125°C
ITT7482 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC} (See Note 1):	ITT5482 Circuits	4.5	5	5.5	V
1	ITT7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_2				5	
E_1 or E_2				10	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage E_1 or E_2	2.4			V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OH} = −400 μA
	C_2						I_{OH} = −200 μA
$V_{out(0)}$	Logical 0 output voltage E_1 or E_2			0.4	V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OL} = 16 mA
	C_2						I_{OL} = 8 mA
$I_{in(0)}$	Logical 0 level input current at A_1, B_1, or C_0			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0			160	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current at E_1 or E_2 [3]	−20		−55	mA	V_{CC} = MAX	ITT5482
		−18		−55	mA		ITT7482
I_{OS}	Short-circuit output current at C_2 [3]	−20		−70	mA	V_{CC} = MAX	ITT5482
		−18		−70	mA		ITT7482
I_{CC}	Supply Current [4]		35	50	mA	V_{CC} = MAX	ITT5482
			35	58	mA		ITT7482

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

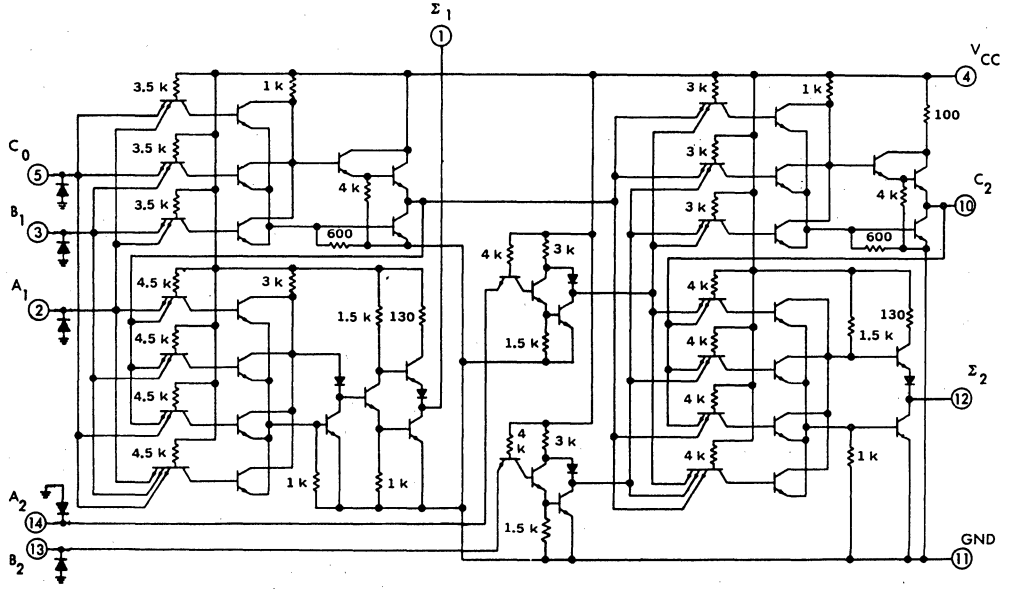
[4] I_{CC} is measured with outputs open, B1 and B2 grounded, and 4.5 V applied to A1, A2, and C0.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C (unless otherwise noted N = 10)

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Test Conditions
t_{pd1}	C_0	E_1			34	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	B_2	E_2			40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					35	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	E_2			38	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					42	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	C_2		12	19	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}				17	27	ns	C_L = 15 pF, R_L = 780 Ω

[1] t_{pd1} is propagation delay time to logical 1 level, t_{pd0} is propagation delay time to logical 0 level.

schematic



Note: Component values shown are nominal.
Resistor values are in ohms.

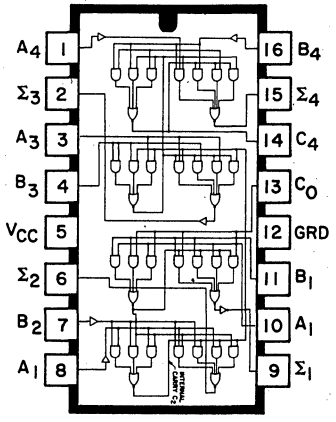
MSI 4-BIT BINARY FULL ADDERS

HIGH-SPEED TTL 4-BIT FULL ADDERS FOR APPLICATION IN

- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)[1]



[1] Pin assignments for these circuits are the same for all packages.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Notes 1 and 2) 5.5V
Operating Free-Air Temperature Range:
ITT5483 Circuits ..... −55°C to 125°C
ITT7483 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic

TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0=0$ / WHEN $C_2=0$			WHEN $C_0=1$ / WHEN $C_2=1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note: 3. Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

recommended operating conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}: (See Note 1)	ITT5483 Circuits	4.5	5	5.5	V
	ITT7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
$\Sigma_1, \Sigma_2, \Sigma_3$ or Σ_4				10	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OH} = −400 µA
							I_{OH} = −200 µA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OL} = 16 mA
							I_{OL} = 8 mA
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0			160	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
I_{OS}	Short-circuit output current at E_1, E_2, E_3, or E_4 [3]	−20		−55	mA	V_{CC} = MAX	ITT5483
		−18		−55	mA		ITT7483
I_{OS}	Short-circuit output current at C_4 [3]	−20		−70	mA	V_{CC} = MAX	ITT5483
		−18		−70	mA		ITT7483
I_{CC}	Supply Current		78	110	mA	V_{CC} = MAX	ITT5483
			78	128	mA		ITT7483

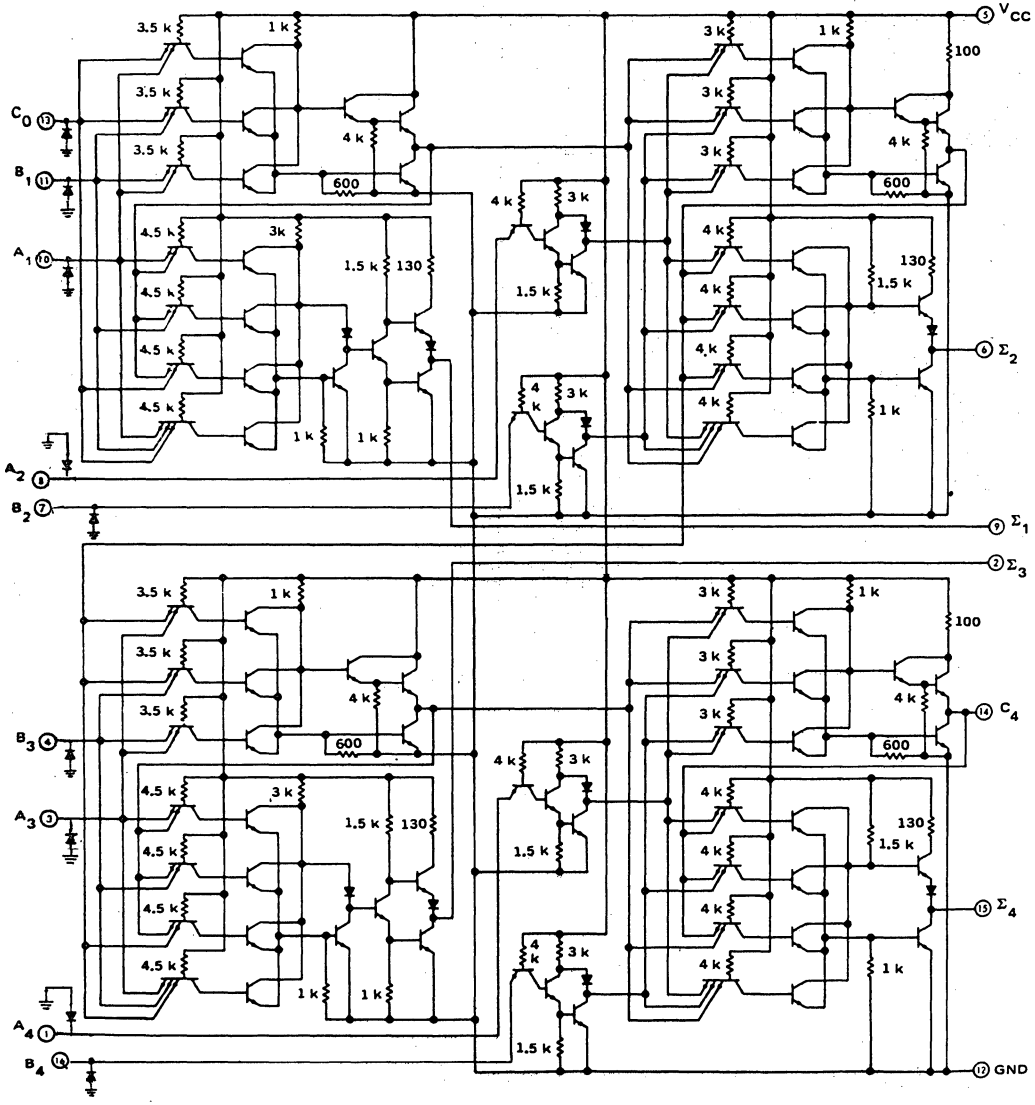
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Test Conditions
t_{pd1}	C_0	1			34	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	2			38	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					42	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	3			50	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					60	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	4			55	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					55	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	C_0	C_4		35	48	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}				22	32	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd1}	A_2 or B_2	2			40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					35	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	A_4 or B_4	4			40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}					35	ns	C_L = 15 pF, R_L = 400 Ω

[1] t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

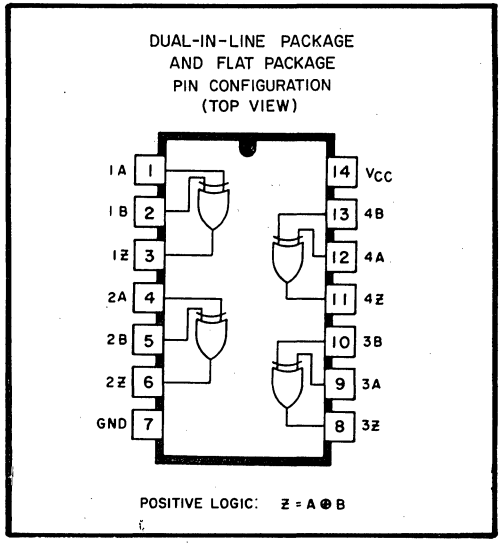
schematic



Note: Component values shown are nominal.
Resistor values are in ohms.

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- **Input-Clamping Diodes Simplify System Design**
- **Fully Compatible with TTL, DTL, and Other MSI Circuits**
- **Typical Propagation Delay Times: 12 ns**



description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

The ITT5486 is characterized for operation over the full military temperature range of −55°C to 125°C and the ITT7486 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage 5.5V
Operating free-air temperature range:
ITT5486 ..... −55°C to 125°C
ITT7486 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note: 1. These voltage values are with respect to network ground terminal.

recommended operating conditions

	ITT5486			ITT7486			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	uA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5486 Min	ITT5486 Typ [1]	ITT5486 Max	ITT7486 Min	ITT7486 Typ [1]	ITT7486 Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.8			0.8	V	
V_I	Input clamp voltage			−1.5			−1.5	V	V_{CC} = MIN, I_I = −8 mA
V_{OH}	High-level output voltage	2.4	3.4		2.4	3.4		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800 uA
V_{OL}	Low-level output voltage		0.2	0.4		0.2	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA
I_I	Input current at maximum input voltage			1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−55	−18		−55	mA	V_{CC} = MAX
I_{CC}	Supply current		30	43		30	50	mA	V_{CC} = MAX, See Note 2

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[3] Not more than one output should be shorted at a time.

Note: 2. I_{CC} is measured with the inputs grounded and the outputs open.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter[1]	From (Input)	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	A or B		15	23	ns	Other input low C_L = 15 pF, R_L = 400Ω
t_{PHL}	A or B		11	17	ns	Other input low C_L = 15 pF, R_L = 400Ω
t_{PLH}	A or B		18	30	ns	Other input high C_L = 15 pF, R_L = 400Ω
t_{PHL}	A or B		13	22	ns	Other input high C_L = 15 pF, R_L = 400Ω

[1] t_{PLH} = propagation delay time, low-to-high-level output. t_{PHL} = propagation delay time, high-to-low-level output

DECADE COUNTERS

MSI TTL HIGH-SPEED DECADE COUNTERS
for applications in

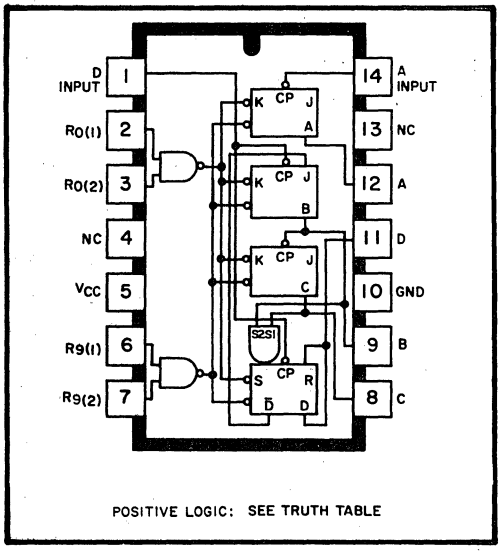
- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) 7V
Input Voltage V_{in} (See Notes 3 and 4) 5.5V
Operating Free-Air Temperature Range:
ITT5490 Circuits ..... −55°C to 125°C
ITT7490 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

logic

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TRUTH TABLES

RESET COUNT
(See Note 2)

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

NC—No Internal Connection

Notes: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logic 1 or a logic 0 may be present.

recommended operating conditions	**MIN**	**NOM**	**MAX**	**UNIT**
Supply Voltage V_{CC} (See Note 3) ITT5490 Circuits	4.5	5	5.5	V
ITT7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

Note: 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

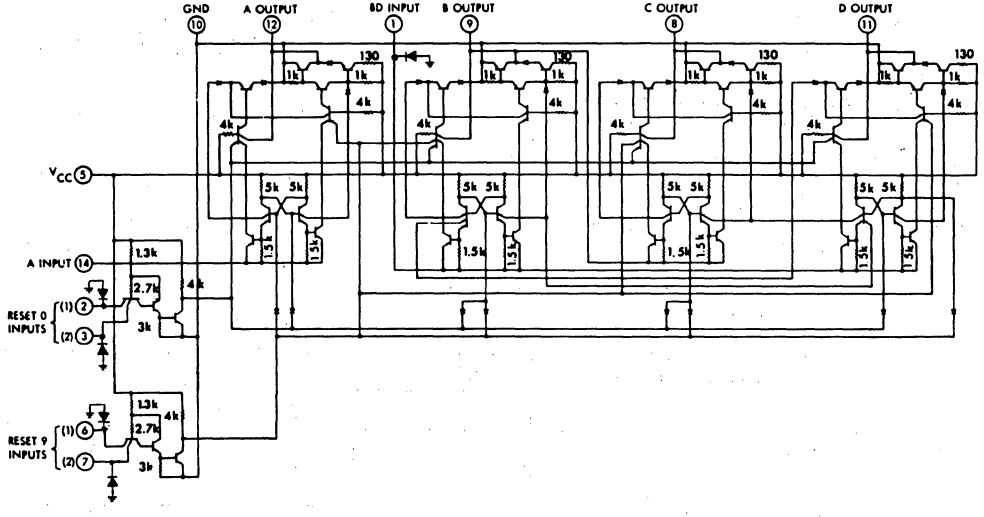
Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −400 uA	
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 16 mA	
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			40	µA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at input A			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at input BD			160	µA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at input A			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at input BD			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX	ITT5490
		−18		−57	mA		ITT7490
I_{CC}	Supply current		32	46	mA	V_{CC} = MAX	ITT5490
			32	53	mA		ITT7490

[1] All typical values are at V_{CC} = 5V, T_A = 25°C
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
f_{max}	Maximum frequency of input count pulses	10	18		MHz	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical I level from input count pulse to output C		60	100	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C		60	100	ns	C_L = 15 pF, R_L = 400 Ω

schematic



Component values shown are nominal.
Resistor values are in ohms.

8-BIT SHIFT REGISTERS

MSI TTL SHIFT REGISTERS
for applications in

- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

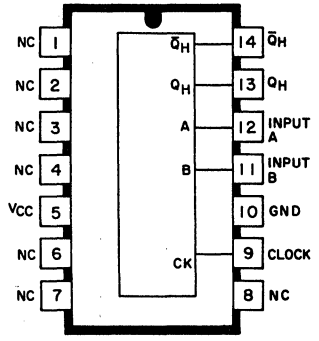
Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

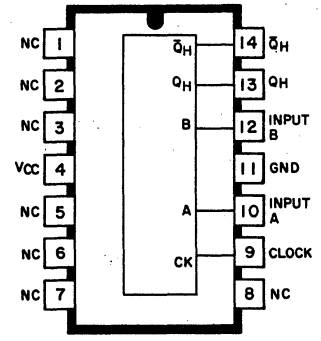
Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT5491A ..... −55°C to 125°C
ITT7491A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
TOP VIEW



POSITIVE LOGIC: SEE FUNCTION TABLE

NC - NO INTERNAL CONNECTION

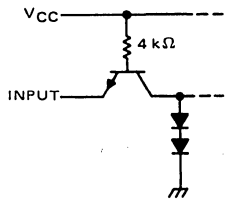
FUNCTION TABLE

Inputs AT t_n		Outputs AT t_{n+8}	
A	B	Q	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

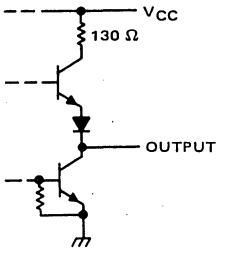
H = high, L = low, X = irrelevant
t_n = Reference bit time, clock low
t_{n+8} = Bit time after 8 low-to-high clock transitions.

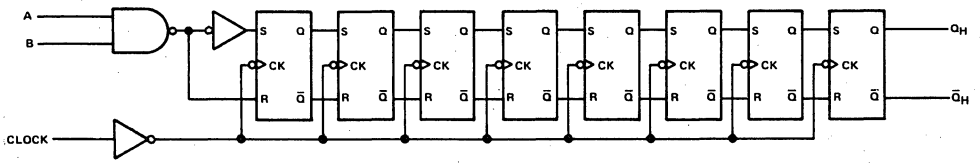
Schematics of inputs and outputs

EQUIVALENT OF ALL INPUTS



TYPICAL OF BOTH OUTPUTS





functional block diagram

recommended operating conditions

	ITT5491A			ITT7491A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level output current, I_{OH}			−400			−400	uA
Low level output current, I_{OL}			16			16	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{setup} (see Figure 1)	25			25			ns
Hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT5491A			ITT7491A			Unit	Test Conditions [2]
		Min	Nom	Max	Min	Nom	Max		
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.8			0.8	V	
V_I	Input Clamp Voltage			−1.5			−1.5	V	V_{CC} = MIN, I_i = −12mA
V_{OH}	High-level output voltage	2.4	3.5		2.4	3.5		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400uA
V_{OL}	Low-level output voltage		0.2	0.4		0.2	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA
I_I	Input current at maximum input voltage			1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−57	−18		−57	mA	V_{CC} = MAX
I_{CC}	Supply current		35	50		35	58	mA	V_{CC} = MAX, See Note 4

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{max}	Maximum clock frequency	10	18		MHz	C_L = 15 pF, R_L = 400 Ω
t_{PLH}	Propagation delay time, low-to-high-level output		24	40	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level output		27	40	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[3] Not more than one output should be shorted at a time.
[4] I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

DIVIDE-BY-TWELVE COUNTERS

MSI TTL HIGH-SPEED COUNTERS
for applications in

- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

logic

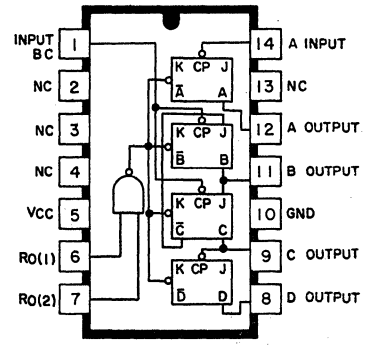
TRUTH TABLE
(See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

Notes: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both. $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

These high-speed, monolithic 4-bit binary counters consist of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

NC—No Internal Connection

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 155 mW.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) 7V
Input Voltage V_{in} (See Notes 4 and 5) 5.5V
Operating Free-Air Temperature Range:
ITT5492 Circuits ..... −55°C to 125°C
ITT7492 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC} (See Note 4): ITT5492 Circuits	4.5	5	5.5	V
ITT7492 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

Note: 6. Fan-out from output A to input BC and to 10 additional Series 54/74 loads is permitted.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 16 mA
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs			40	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at input A			80	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at input BC			160	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at input A			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted) **(continued)**

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
$I_{in(0)}$	Logical 0 level input current at input BC			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX,	ITT5492
		−18		−57	mA	V_{out} = 0	ITT7492
I_{CC}	Supply current		31	44	mA	V_{CC} = MAX	ITT5492
			31	51	mA	V_{in} = 4.5V	ITT7492

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

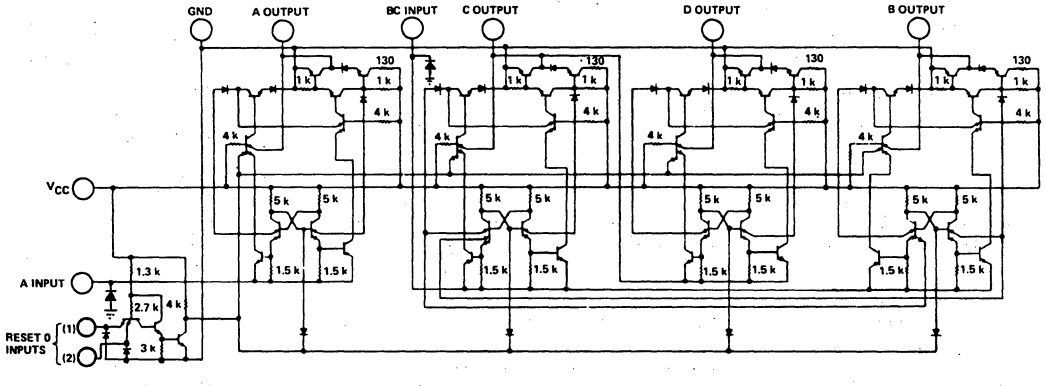
	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum frequency of input count pulses	10	18		MHz	C_L = 15pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D		60	100	ns	C_L = 15pF, R_L = 400Ω
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D		60	100	ns	C_L = 15pF, R_L = 400Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

[3] Not more than one output should be shorted at a time.

Schematic



4-BIT BINARY COUNTERS

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

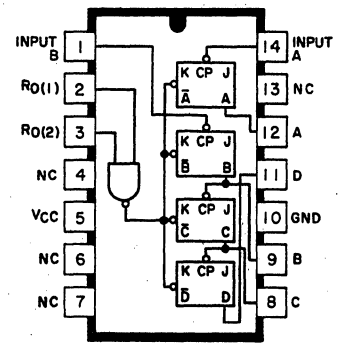
- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 ITT and DTL logic families. Average power dissipation is 40 mW per flip-flop (160 mW total).

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

NC—No Internal Connection

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) 7V
Input Voltage, V_{in} (See Notes 4 and 5) 5.5V
Operating Free-Air Temperature Range:
ITT5493 Circuits ..... −55°C to 125°C
ITT7493 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

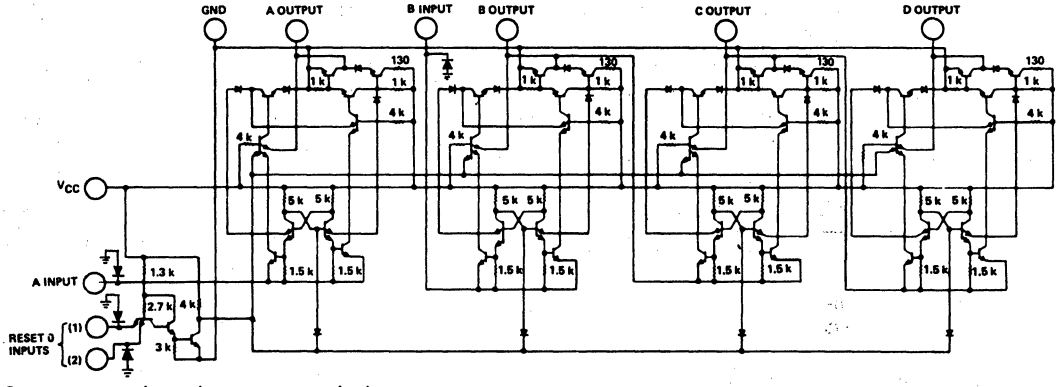
recommended operating conditions		**Min**	**Nom**	**Max**	**Unit**
Supply Voltage V_{CC} (See Note 4):	ITT5493 Circuits	4.5	5	5.5	V
	ITT7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

Note 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

TRUTH TABLE
(See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Notes: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be a logical 0 to count.



Component values shown are nominal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} =−400uA	
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 16mA	
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at A or B inputs			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at A or B inputs			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{out} = 0	ITT5493
		−18		−57	mA		ITT7493
I_{CC}	Supply current		32	46	mA	V_{CC} = MAX, V_{in} = 4.5V	ITT5493
			32	53	mA		ITT7493

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum frequency of input count pulses	10	18		MHz	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D		75	135	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D		75	135	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
[3] Not more than one output should be shorted at a time.

4-BIT SHIFT REGISTERS

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS for application as

- **Dual-Source, Parallel-To-Serial Converter**
- **Serial-In Serial-Out Register**

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

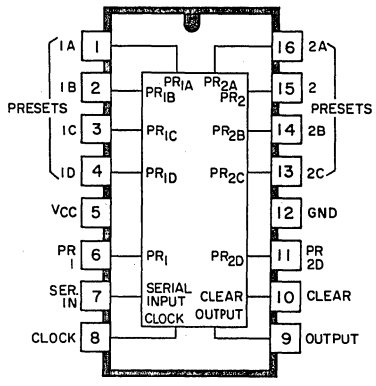
All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: HIGH INPUT TO CLEAR SETS Q_A, Q_B, Q_C AND Q_D TO LOGICAL 0.

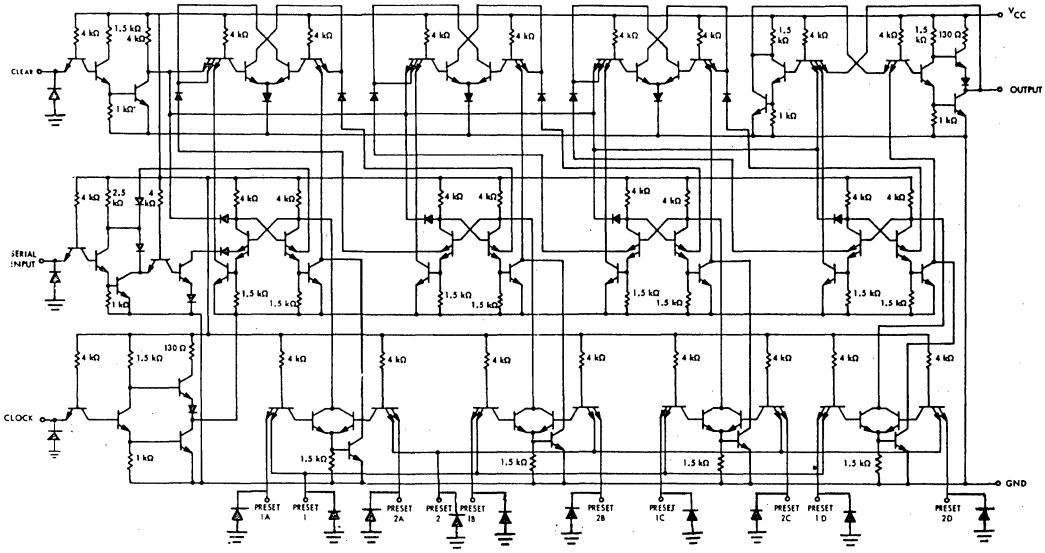
†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage V_{in} (See Notes 1 and 2) 5.5V
Operating Free-Air Temperature Range:
ITT5494 Circuits ..... −55°C to 125°C
ITT7494 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

schematic



Note: Component values shown are nominal.

recommended operating conditions	Min	Typ	Max	Unit
Supply Voltage V_{CC} (See Note 1): ITT5494 Circuits	4.5	5	5.5	V
ITT7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(l)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

Note: 1. These voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted) **(continued)**

Parameter		Min	Typ [1]	Max	Unit	Test Conditions	
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN, I_{load} = −400uA	
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16mA	
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2			160	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2			−6.4	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short-circuit input current [3]	−20		−57	mA	V_{CC} = MAX,	ITT5494
		−18		−57	mA	V_{out} = 0	ITT7494
I_{CC}	Supply current		35	50	mA	V_{CC} = MAX	ITT5494
			35	58	mA		ITT7494

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	10			MHz	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output		25	40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output		25	40	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from preset to output			35	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear to output			40	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
[3] Not more than one output should be shorted at a time.

4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

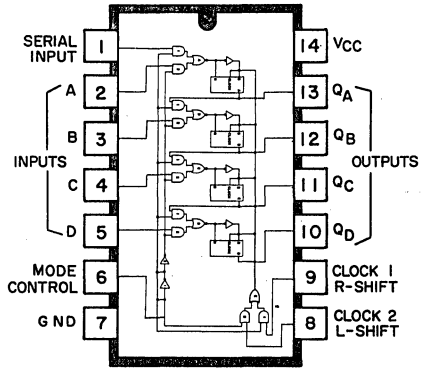
This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:

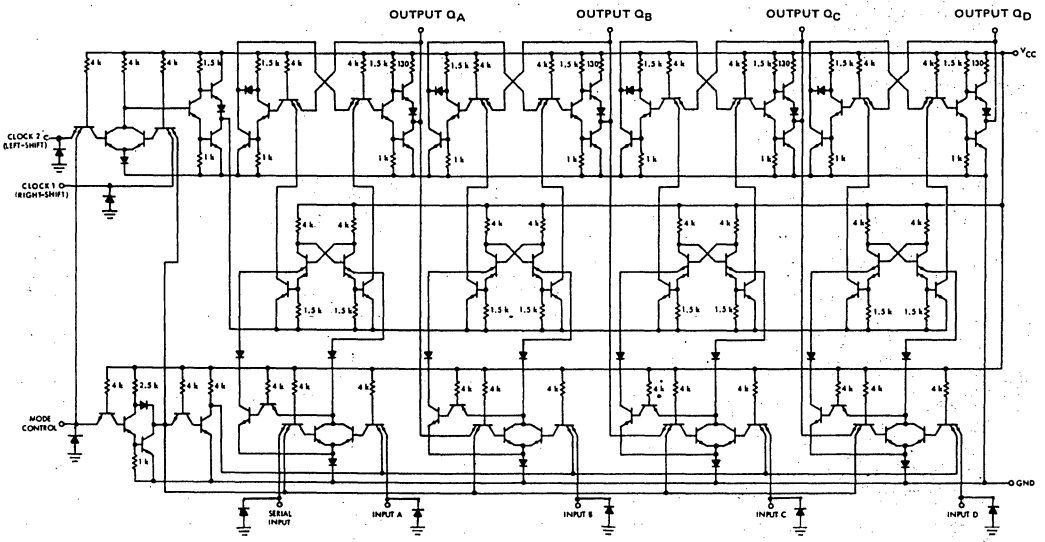
MODE CONTROL = 0 FOR RIGHT SHIFT
MODE CONTROL = 1 FOR LEFT SHIFT OR PARALLEL LOAD

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 195 milliwatts. The ITT5495A and ITT7495A are unilaterally interchangeable with and replace ITT5495 and ITT7495, respectively, but offer diode-clamped inputs, improved speed, and reduced power dissipation.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage V_{in} (See Notes 1 and 2) 5.5V
Operating Free Air Temperature Range:
ITT5495A Circuits ..... −55°C to 125°C
ITT7495A Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

schematic



Notes: 1. Register values are in ohms.
2. Component values shown are nominal.

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC} (See Note 1): ITT5495A Circuits	4.5	5	5.5	V
ITT7495A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output: High logic level			20	
Low logic level			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): ITT5495A Circuits	20	10		ns
ITT7495A Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D inputs t_{setup}	10			ns
Hold Time Required at Serial, A, B, C, or D inputs t_{hold}	0			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)	15			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)	15			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)	5			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)	5			ns

Notes: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} =−800uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 16mA
$I_{in(0)}$	Logical 0 level input current at any input except mode control			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at mode control			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current at any input except mode control			40	ua	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at mode control			80	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−18		−57	mA	V_{CC} = MAX
I_{CC}	Supply current	39		63	mA	V_{CC} = MAX

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum shift frequency	25	36		MHz	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs		18	27	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs		21	32	ns	C_L = 15 pF, R_L = 400 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
[3] Not more than one output should be shorted at a time.

5-BIT SHIFT REGISTERS

TTL MSI MULTIFUNCTION SHIFT REGISTERS
for application as

- **N-Bit Serial-To-Parallel Converter**
- **N-Bit Parallel-To-Serial Converter**
- **N-Bit Storage Register**

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

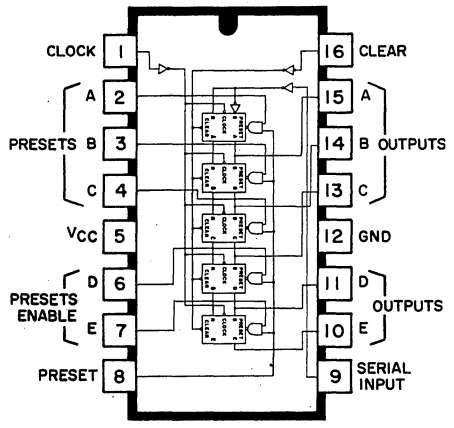
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The preset-enable input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



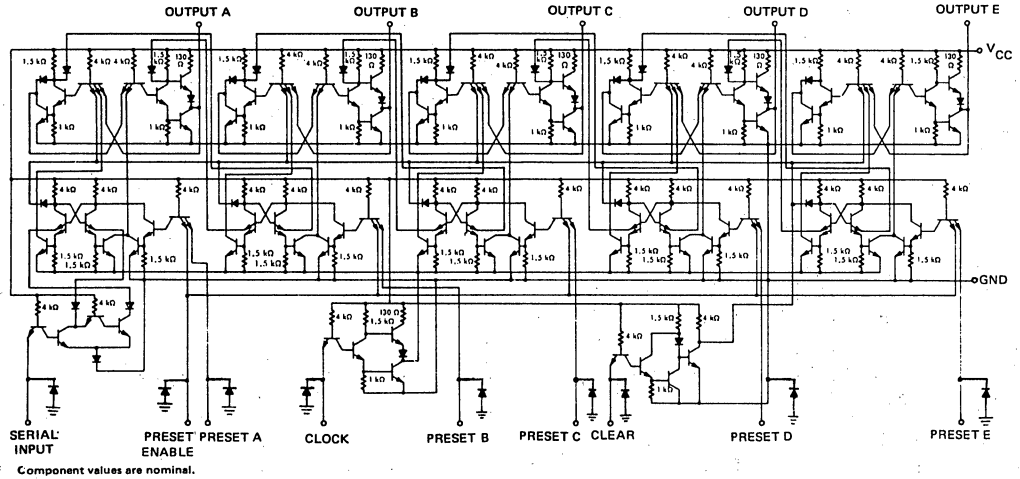
POSITIVE LOGIC: LOW INPUT AT CLEAR SETS ALL OUTPUTS TO LOGICAL 0.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage V_{in} (See Notes 1 and 2) 5.5V
Operating Free-Air Temperature Range:
ITT5496 Circuits ..... −55°C to 125°C
ITT7496 Circuits ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Notes: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

schematic



recommended operating conditions	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): ITT5496 Circuits	4.5	5	5.5	V
ITT7496 Circuits	4.75	5	5.25	V
Normalized Fan Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage	2			V	
$V_{in(0)}$	Logical 0 input voltage			0.8		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −12 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.5		V	V_{CC} = MIN I_{load} = −400 uA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN. I_{sink} = 16 mA

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted) **(continued)**

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
$I_{in(1)}$	Logical 1 level input current at any input except preset-enable			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(1)}$	Logical 1 level input current at preset-enable			200	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at any input except preset-enable			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(0)}$	Logical 0 level input current at preset-enable			−8	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX, V_{out} = 0	ITT5496
		−18		−57	mA		ITT7496
I_{CC}	Supply current		48	68	mA	V_{CC} = MAX	ITT5496
			48	79	mA		ITT7496

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	10			MHz	C_L = 15pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output		25	40	ns	C_L = 15pF, R_L = 400Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output		25	40	ns	C_L = 15pF, R_L = 400Ω
t_{pd1}	Propagation delay time to logical 1 level from preset or preset-enable to output		25	35	ns	C_L = 15pF, R_L = 400Ω
t_{pd0}	Propagation delay time to logical 0 level from clear to output			55	ns	C_L = 15pF, R_L = 400Ω

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

J-K FLIP FLOPS

The ITT54104 is identical to the ITT9000-1
The ITT74104 is identical to the ITT9000-5
The ITT54105 is identical to the ITT9001-1
The ITT74105 is identical to the ITT9001-5
The ITT54109 is identical to the ITT9024-1
The ITT74109 is identical to the ITT9024-5

Refer to the 9000 series TTL section for these devices.

HEX SET-RESET LATCH

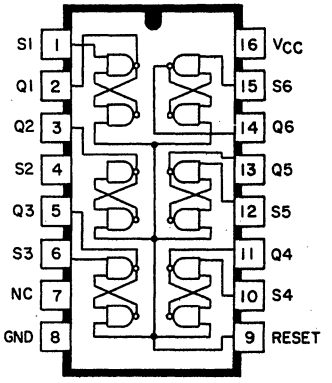
The ITT74118 consists of six cross coupled NAND gates each forming a simple bistable circuit. A reset line is common to all six latches. Information is stored within a latch when both the set line and the common reset line are held at logical '1'. The state of each bistable can be changed by taking either the set or reset to logical '0' as shown in the truth table.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

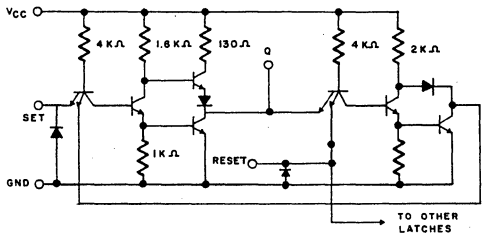
Supply voltage V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Operating free-air temperature range, T_A:
ITT54118 ..... −55°C to 125°C
ITT74118 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

Pin configuration
(top view)
Dual-In-Line and Flat Package



Circuit Schematic (each Latch)



Truth Table

S	Reset	Q
0	X	1
1	0	0
1	1	Store

1. X indicates input may be logical '1' or '0'.
2. Reset is common to all latches.

recommended operating conditions

	ITT54118			ITT74118			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800uA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA
I_{IH}	High-level input current (set inputs)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current (reset inputs)			200	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (set inputs)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{IL}	Low-level input current (reset inputs)			−8	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX, ITT54118
		−18		−55		ITT74118
I_{CCH}	Supply current, high-level output		11	21	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		20	33	mA	V_{CC} = MAX, V_I = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10
(unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
t_{PLH}	Propagation delay time to logical '1' level from set		18	29	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time to logical '0' level from set		10	17	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time to logical 0 level from reset		18	29	ns	C_L = 15 pF, R_L = 400Ω

[1] All typical values at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

MONOSTABLE MULTIVIBRATORS

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL compatible and featuring temperature-independent backlash), for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i. e., pin 9 connected to pin 14, pins 10, 11 open) an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

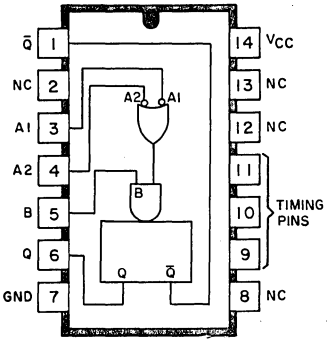
Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 uF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwats at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwats.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ: Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

FLAT PACK AND DUAL-IN-LINE PACKAGE PIN CONFIGURATION (TOP VIEW)



TRUTH TABLE
(See Notes 1 thru 3)

INPUTS			OUTPUTS	
A1	A2	B	Q	Q̄
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

$H = V_{in(1)} \geq 2V$

$L = V_{in(0)} < 0.8V$

Notes: 1. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).

Notes (continued)

2. NC = No Internal Connection.
3. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
4. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table).
5. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30 ns is obtained.
6. To use the internal timing resistor (2 kΩ nominal), connect pin 9 to pin 14.
7. To obtain variable pulse width connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
8. For accurate repeatable pulse widths, connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit.

recommended operating conditions	**Min**	**Nom**	**Max**	**Unit**
Supply Voltage V_{CC}: ITT54121 Circuits	4.5	5	5.5	V
ITT74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/us
Input Pulse Width	50			ns
External Timing Resistance Between Pins 11 and 14 (Pin 9 open)	1.4			kΩ
External Timing Resistance: ITT54121			30	kΩ
ITT74121			40	kΩ
Timing Capacitance	0		1000	uF
Output Pulse Width			40	s
Duty Cycle: R_T = 2 kΩ			67%	
R_T = 30 kΩ (ITT54121) or R_T = 40 kΩ (ITT74121)			90%	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	**Min**	**Typ** [1]	**Max**	**Unit**	**Test Conditions** [2]
V_{T+}	Positive-going threshold voltage at A input		1.4	2	V	V_{CC} = MIN
V_{T-}	Negative-going threshold voltage at A input	0.8	1.4		V	V_{CC} = MIN

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{T+}	Positive-going threshold voltage at B input		1.55	2	V	V_{CC} = MIN
V_{T-}	Negative-going threshold voltage at B input	0.8	1.35		V	V_{CC} = MIN
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN I_i = −12 mA
$V_{out(0)}$	Logical 0 output voltage		0.22	0.4	V	V_{CC} = MIN, I_{sink} = 16 mA
$V_{out(1)}$	Logical 1 output voltage	2.4	3.3		V	V_{CC} = MIN, I_{load} = −400 uA
$I_{in(0)}$	Logical 0 level input current at A1 or A2		−1	−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at B		−2	−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current at A1 or A2		2	40	uA	V_{CC} = MAX, V_{in} = 2.4V
			0.05	1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at B		4	80	uA	V_{CC} = MAX, V_{in} = 2.4V
			0.05	1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short circuit output current at Q or Q [3]	−20	−25	−55	mA	V_{CC} = MAX ITT54121
		−18	−25	−55		ITT74121
I_{CC}	Power supply current in quiescent (unfired) state		13	25	mA	V_{CC} = MAX
I_{CC}	Power supply current in fired state		23	40	mA	V_{CC} = MAX

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	15	35	55	ns	C_L = 15 pF, C_T = 80 pF
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output	25	45	70	ns	C_L = 15 pF, C_T = 80 pF
t_{pd0}	Propagation delay time to logical 0 level from B input to Q output	20	40	65	ns	C_L = 15 pF, C_T = 80 pF
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to Q output	30	50	80	ns	C_L = 15 pF, C_T = 80 pF

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

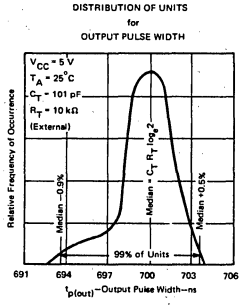
Parameter		Min	Typ	Max	Unit	Test Conditions
$t_{p(out)}$	Pulse width obtained using internal timing resistor	70	110	150	ns	C_L = 15 pF, C_T = 80 pF, R_T = Open, Pin 9 to V_{CC}
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	20	30	50	ns	C_L = 15 pF, C_T = 0, R_T = Open, Pin 9 to V_{CC}
$t_{p(out)}$	Pulse width obtained using external timing resistor	600	700	800	ns	C_L = 15 pF, C_T = 100 pF R_T = 10 kΩ Pin 9 Open
		6	7	8	ms	C_L = 15 pF, C_T = 1 uF, R_T = 10 kΩ Pin 9 Open
t_{hold}	Minimum duration of trigger pulse		30	50	ns	C_L = 15 pF, C_T = 80 pF, R_T = Open, Pin 9 to V_{CC}

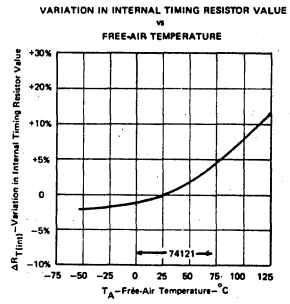
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

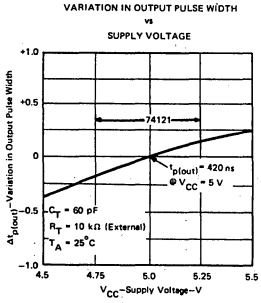
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

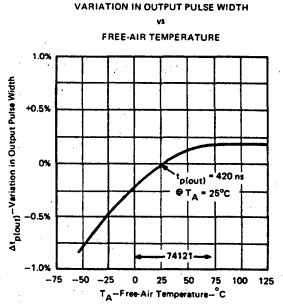
[3] Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS [1]





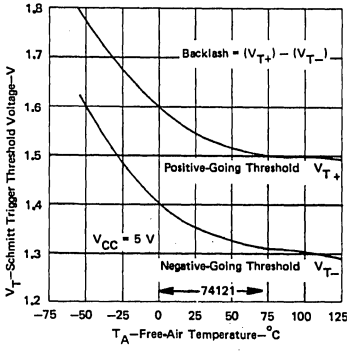




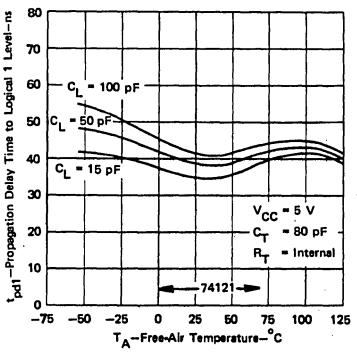
[1] Unless otherwise noted data is applicable for ITT54121 and ITT74121.

TYPICAL CHARACTERISTICS [1]

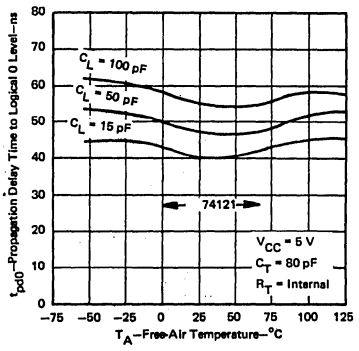
SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



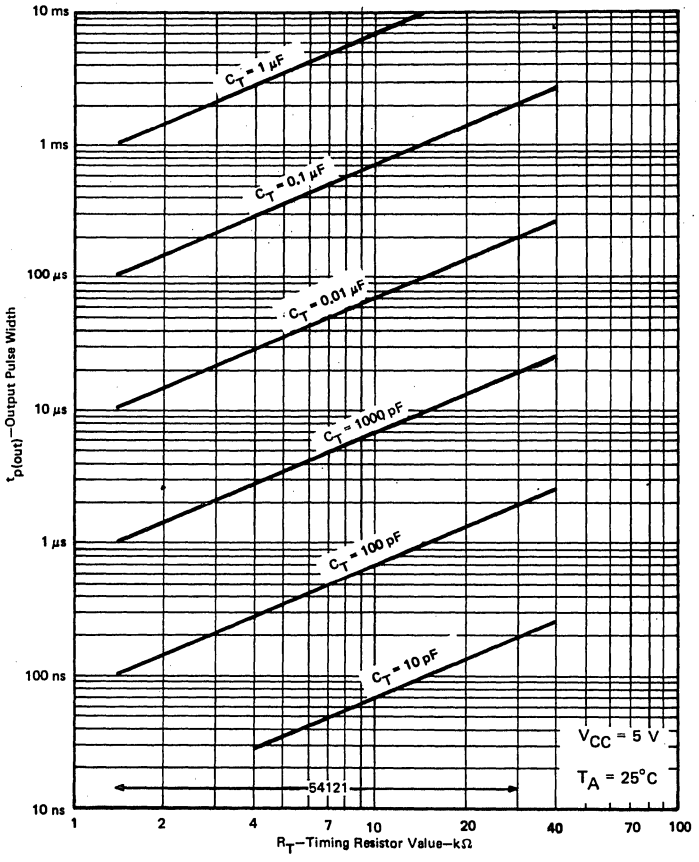
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
(B INPUT TO Q OUTPUT)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
(B INPUT TO $\overline{Q}$ OUTPUT)
vs
FREE-AIR TEMPERATURE

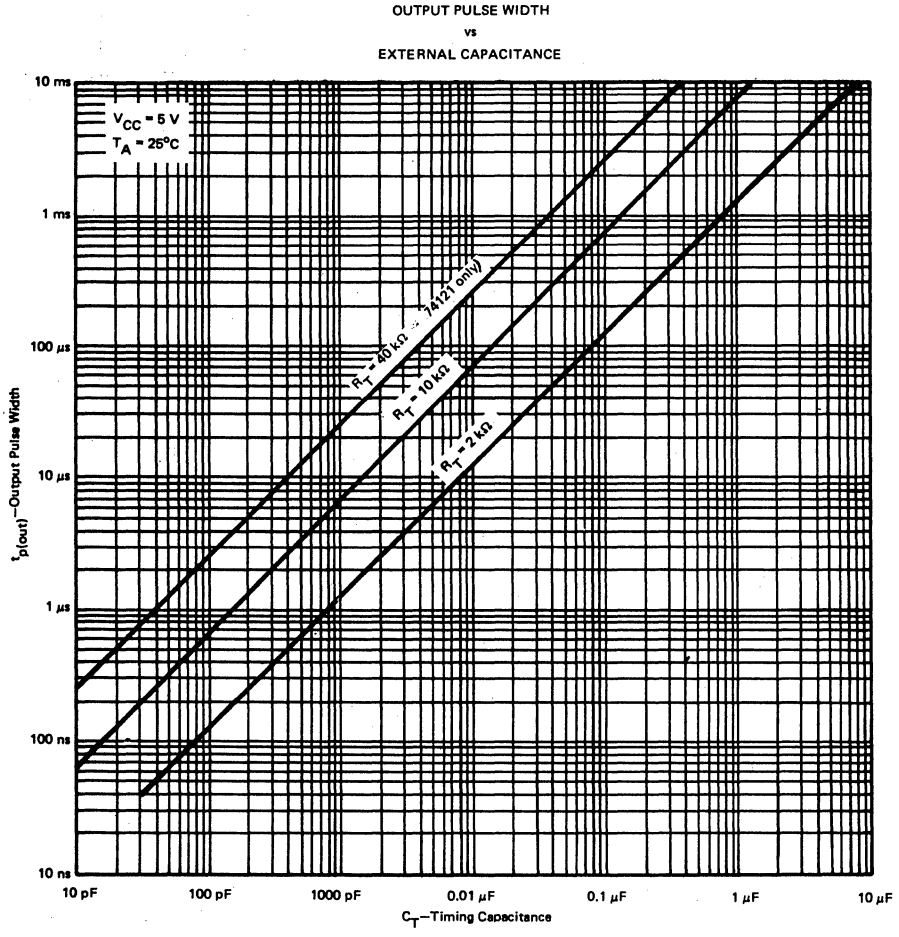


OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE



[1] Unless otherwise noted data is applicable for ITT54121 and ITT74121.

TYPICAL CHARACTERISTICS [1]



[1] Unless otherwise noted data is applicable for ITT54121 and ITT74121

ITT SEMICONDUCTORS

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Diode-Clamped Inputs**
- **D-C Triggered from High- or Low-Level Gated Logic Inputs**
- **Compatible for Use with TTL or DTL**
- **Typical Average Propagation Delay to Output Q...21 ns**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage, ITT54122, ITT74122 Circuits only (see Note 2) 5.5V
Operating free-air temperature range:
ITT54122, ITT54123 Circuits .... −55°C to 125°C
ITT74122, ITT74123 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

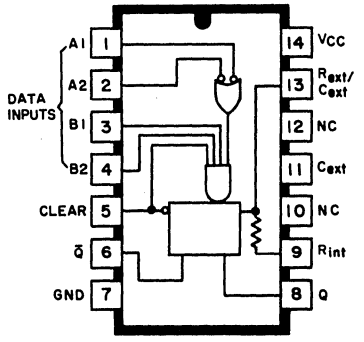
TRUTH TABLE—ITT54122, ITT74122

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	Q
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

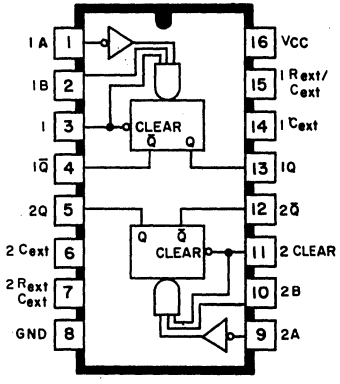
Notes: A. H = high level (steady state), L = low level (steady state), I = transition from low to high level, ↑ = transition from high to low level, ↓ = one high-level pulse, U = one low-level pulse, X = irrelevant (any input, including transitions).

PIN CONFIGURATION OF DIP AND FLAT PACKAGE

ITT54122/ITT74122



ITT54123/ITT74123



POSITIVE LOGIC: LOW INPUT TO CLEAR RESETS Q TO LOW LEVEL AND INHIBITS DATA INPUTS

NOTES: NC = No internal connection.
To use the internal timing resistor of ITT-54122/ITT74122 (10 kΩ nominal), connect R_{int} to V_{CC}.
An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

TRUTH TABLE - ITT54123/ITT74123

Inputs			Outputs	
Clear	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

Notes: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, I = one high-level pulse, U = one low-level pulse, X = irrelevant (any input, including transitions).

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.

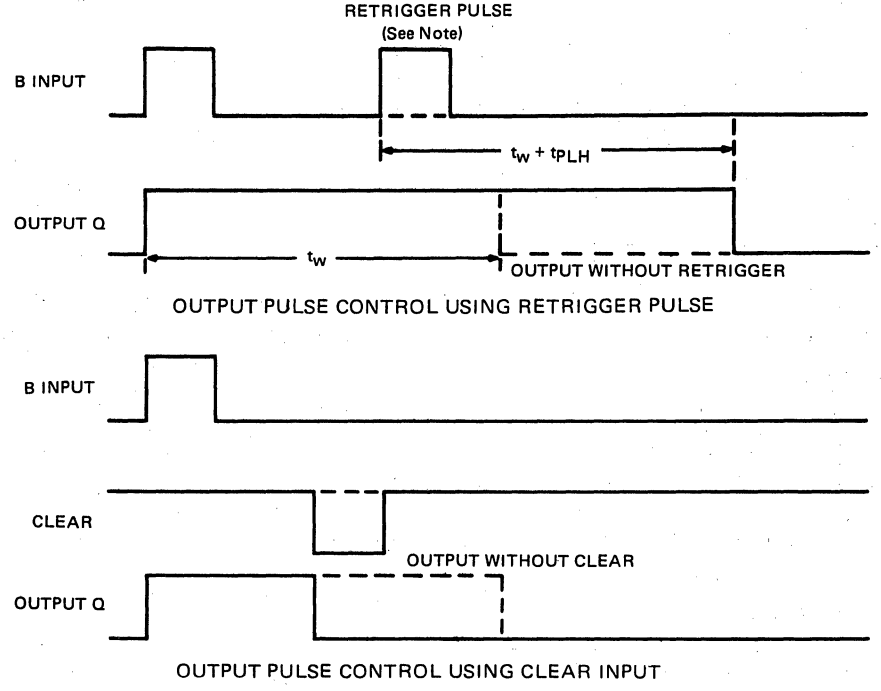


FIGURE A—TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. ITT54122/ITT74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with ITT54121/ITT74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\, R_T C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} < 1000$ pF, see Figure B.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The ITT54122 and ITT54123 are characterized for operation over the full military temperature range of 55°C to 125°C; the ITT74122 and ITT74123 are characterized for operation from 0°C to 70°C.

recommended operating conditions

		54122, 54123			74122, 74123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3)		40†			40†			ns
Input data hold time, t_{hold} (see Note 4)		40†			40†			ns
Width of clear pulse, $t_{w(clear)}$		40†			40†			ns
External timing resistance		5		25	5		50	kΩ
External capacitance		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

NOTES:

1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the 54122/74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, I_{OH} = −800uA, See Note 5

ELECTRICAL CHARACTERISTICS (continued)

V_{OL}	Low-level output voltage			0.22	0.4	V	V_{CC} = MIN, I_{OL} = 16mA, See Note 5
I_I	Input current at maximum input voltage				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current	data inputs			40	uA	V_{CC} = MAX, V_I = 2.4V
		clear input			80		
I_{IL}	Low-level input current	data inputs			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
		clear input			−3.2		
I_{OS}	Short-circuit output current [3]		−10		−40	mA	V_{CC} = MAX, See Note 5
I_{CC}	Supply current (quiescent or triggered)			23	28	mA	V_{CC} = MAX. ITT54122, ITT74122
				46	66		See Notes 6 and 7 ITT54123, ITT74123

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

Notes: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02uF, and R_{ext} = 25kΩ, R_{int} of ITT54122, ITT74122 is open.
7. I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02uF, and R_{EXT} = 25kΩ. R_{int} of ITT54122, ITT74122 is open.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input		22	33	ns	C_{ext} = 0, R_{ext} = 5kΩ, C_L = 15pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input		19	28	ns	C_{ext} = 0, R_{ext} = 5kΩ, C_L = 15pF, R_L = 400 Ω.
t_{PHL}	Propagation delay time, high-to-low-level Q output, from either A input		30	40	ns	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level Q output, from either B input		27	36	ns	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input		18	27	ns	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400 Ω

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 **(continued)**

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level Q output, from clear input		30	40	ns	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400 Ω
$t_{w(min)}$	Minimum width of Q output pulse		45	65	ns	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400 Ω
t_w	Width of Q output pulse	3.00	3.42	3.78	ns	C_{ext} = 1000pF, R_{ext} = 10kΩ C_L = 15pF, R_L = 400 Ω

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

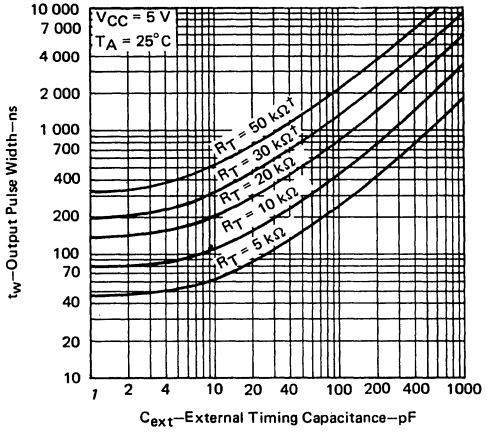


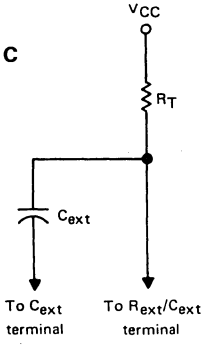
FIGURE B

† These values of resistance exceed the maximums recommended for use over the full temperature range of the ITT54122 and ITT54123.

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure D be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

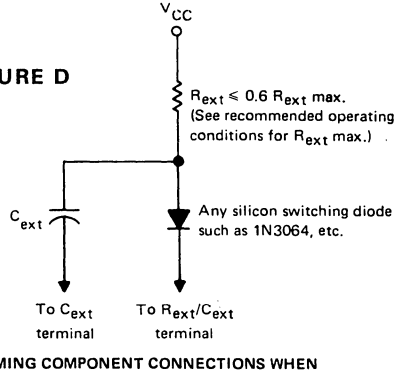
TYPICAL APPLICATION DATA

FIGURE C



TIMING COMPONENT CONNECTIONS WHEN C_{ext} ≤ 1000 pF

FIGURE D



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

$$t_w = 0.28\, R_{ext} C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

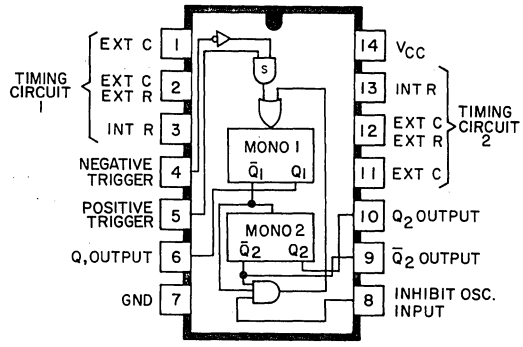
where R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

ITT SEMICONDUCTORS

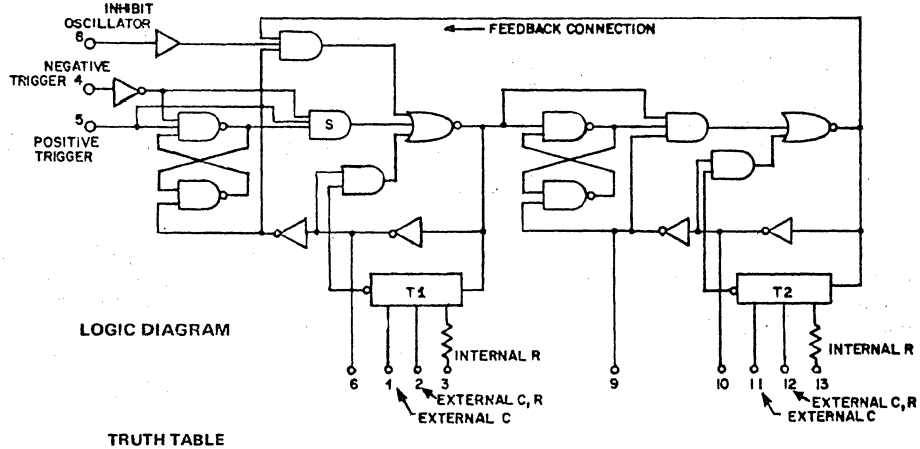
UNIVERSAL PULSE GENERATOR

- Delayed Pulse Generator.
- Controllable high stability oscillator.
- Applications include clock generator, Timing pulse generation, Synchronized oscillator, and pulses frequency divider.
- Outputs available from the two incorporated Cascade Monostables.
- No jitter self start.
- Complete output waveforms.
- Positive Schmitt Trigger input.
- Delays and pulse widths from 35 ns to 40 second.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



PIN CONFIGURATION (top view)



LOGIC DIAGRAM

TRUTH TABLE

Mode	Inputs			Outputs During Time Period:		
	INH OSC	POS TRIG	NEG TRIG	T_1 Q_1	T_2 Q_2	T_2 $\bar{Q}_2$
OSCILLATOR MODE	1	0	X	⎍	⎍	⎎
	1	X	1	⎍	⎍	⎎
DELAYED PULSE MODE	0	↑	0	⎍	⎍	⎎
	0	1	↓	⎍	⎍	⎎
STABLE STATE MODE	ALL OTHER LEVELS			0	0	1

Notes:
↑ = Transition from 0 to 1.
↓ = Transition from 1 to 0.
X = Indicates that 0, 1 or any transition may be present.
⎍ = 1 level pulse of width = timing period T_1 or T_2.
⎎ = 0 level pulse of width = timing period T_2.
Timing period T_1 set by timing circuit 1.
Timing period T_2 set by timing circuit 2.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Propagation delay, trigger input to Q_1 ..... 43 ns
Inhibit Oscillator input to Q_1 ..... 26 ns
Q_1 to Q_2 ..... 15 ns
Power dissipation (50% duty cycle) ..... 150 mW
Input loading factor ..... 1 Unit Load
Maximum fan out ..... 10 unit loads
External timing resistor, R_T ..... 1.4 kΩmin
(54124 25K max.) 50 kΩmax.
External timing capacitor, C_T ..... 0 pF min.
50 uF max.
Recommended maximum
output frequency ..... 10 MHz
Recommended input pulse width:
Inhibit Oscillator input ..... 15 ns min.
Trigger input ..... 50 ns min.
Trigger input setup time ..... 10 ns
Maximum mark space ratio:
R_T = Max. Value 100: 1
R_T = Min. Value 5: 1
Output pulse width ..... 0.695 $C_T R_T$
Timing Stability:
Typical Timing period change
with supply voltage ..... 0.2% per Volt
Typical Timing period change
over 0° to 75°C Temperature range 0.15%

The ITT 74124 Universal Pulse Generator has been designed specifically for clock and delayed pulse generation applications. This versatile device incorporates two cascaded monostable circuits to provide the delayed pulse facility and a gated feedback path allows its operation as a controllable high stability oscillator. The external timing components which control the delay and pulse width periods in the delayed pulse generator mode are used to determine the oscillator mark — space ratios (duty cycle). The true output, Q_1 from the first monostable and true and complements outputs, Q_2 and $\overline{Q_2}$ from the second monostable are provided. These outputs are of standard totem pole configuration and provide a maximum fan-out of 10 T.T.L. loads.

Delayed Pulse Generator Mode

When operating in the delayed pulse mode the feedback loop is inhibited by maintaining the inhibit oscillator input at '0'. The device can then be triggered from the positive edge trigger input with the negative edge input held at '0', or from the negative edge trigger input with the positive edge trigger input held at '1'. The positive trigger input incorporates a Schmitt trigger circuit for slow edges or level detection. Once triggered further transistions on the inputs have no effect on the Q_1 output pulse until after the first monostable timing period is completed. The second monostable is triggered from the first monostable output pulse by its trailing edge and is not effected by any further transistions from the first monostable until its timing period is over. The output of the second monostable is therefore a single pulse having a width determined by the time-constant of the second monostable and which is delayed from the initiating input trigger edge by the time constant of the first monostable.

Oscillator (Astable Multivibrator) Mode

The feedback path is operative when the inhibit oscillator input is taken to logical '1', and for operation in the oscillator mode the positive trigger input and/or the negative trigger input must be maintained at '1'. The feedback path enables the trailing edge from the second monostable to retrigger the first monostable to maintain the oscillations. As soon as the inhibit oscillator input is taken to logical '0', the device reverts to its delayed pulse mode and the oscillations stop when the second monostable timing period is over. In this way only whole cycles are produced. It is a feature of the design that a locked-up state, preventing the circuit from oscillating, cannot occur. The first monostable is immediately triggered on application of '1' to the inhibit oscillator input with the correct trigger input levels, and will not lock-up when the supplies are switched on with the correct input signals applied. By virtue of the inhibit oscillator input it is possible to gate the oscillator on and off to produce bursts of pulses. It is also possible to synchronize the oscillator by applying appropriate waveforms at the inputs. This facility allows for its use as a pulse frequency divider.

The time period for the first monostable, which determines the pulse width from the Q_1 output and the delay before the pulse from the Q_2 and $\overline{Q_2}$ outputs begins, is set by the timing circuit on pins 1, 2, and 3. The time period for the second monostable determines the pulse width obtained from the Q_2 and $\overline{Q_2}$ outputs is set by the timing components connected to pins 11, 12, and 13. The timing components may be connected as follows:

a. External timing capacitor, C_T, may be connected between pin 1 (11) positive and pin 2 (12). With no external capacitance an output pulse width of typically 25 ns is obtained with $R_T = 1.5K\Omega, +10K\Omega$

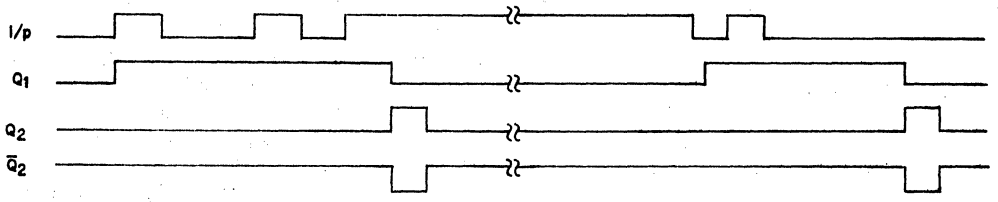
b. To use the internal timing resistor (normally $7.2K\Omega$) connect pin 3 (13) to V_{CC} (pin 14). The pulse width or time delay is approximately given by $t = 5 \times 10^3 C_T$.

c. To obtain variable resistor between pin 3 (13) and V_{CC} (pin 14). Add the value of the internal resistor, $7.2K\Omega$ to the external resistance used, to obtain the R_T value.

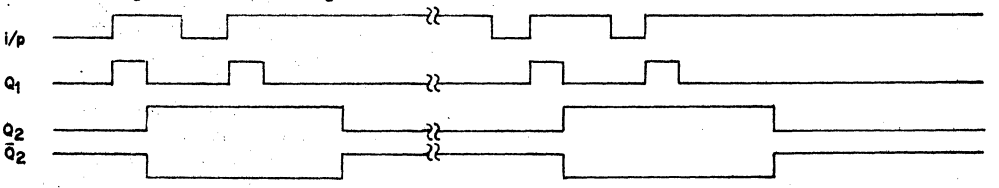
d. For accurate timing connect an external resistor between pin 2 (12) and V_{CC} (pin 14). Leave pin 3 (13) open circuit.
Relationship for timing period, $t = 0.695 C_T R_T$ where C_T and R_T are the timing components values used.

Note: Timing periods of the order of one second are obtained when using the maximum recommended R_T and C_T component values.

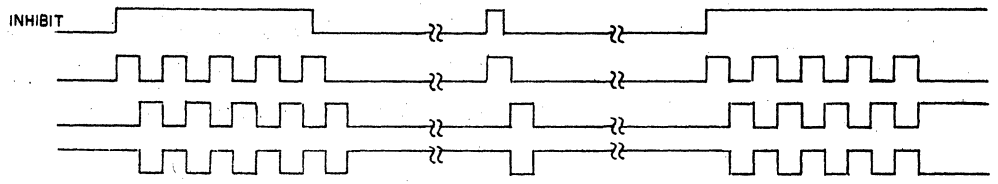
1/ Delayed Pulse Mode **a) Timing Period T1 ≫ Timing Period T2 (inhibit = negative trigger = '0').**



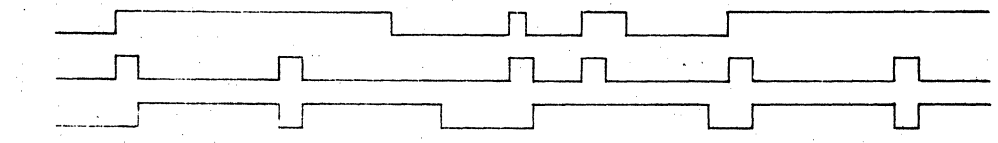
b) Timing Period T1 ≪ Timing Period T2.



2/ Oscillating Mode **a) Timing Period T1 = Timing Period T2 (positive trigger = '0').**



b) Timing Period T1 ≪ Timing Period T2.



Waveforms illustrating the function of the circuit in the delayed pulse and oscillating modes.

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions
V_{T+}	Positive edge threshold Voltage at trigger input (positive)		1.75	2	V	5V C_T = 1000 pf R_T = 10 KΩ
V_T	Negative edge threshold Voltage at trigger input (positive)	0.8	1.4		V	5V C_T = 1000 pf R_T = 10 KΩ
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 uA
V_{OL}	Low-level output voltage		0.2	0.4	V	V_{CC} = MIN, I_{OL} = 16 mA
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−18		−55	mA	V_{CC} = MAX
I_{CC}	Supply current, Input high		30	60	mA	Max) C_T = 1000 pf
I_{CC}	Supply current, Inputs low		30	60	mA	Max) R_T = 10 KΩ
	MKS mark space ratio (duty cycle)	90.1	100.1			R_T = max, value minimum space width = 100 ns with 5% degradation in pulse width set at equal mark space ratio.

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

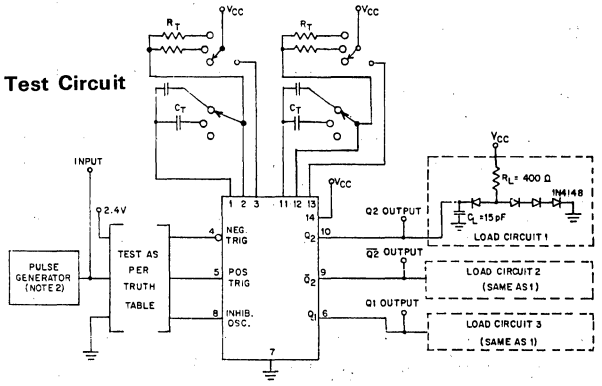
[3] Not more than one output should be shorted at a time.

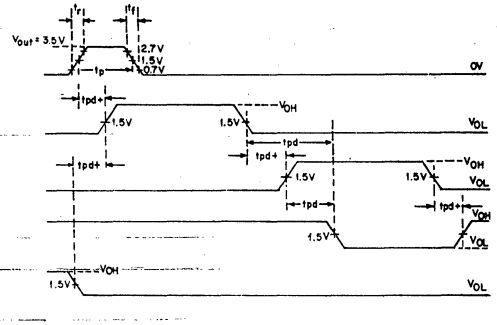
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{pd+}	From Inhibit Oscillator to Q_1		26	50	ns	Use Test Circuit C_T 100 pf
	From Neg Trigger to Q_1		45	85	ns	Use Test Circuit C_T 100 pf
	From Pos Trigger to Q_1		40	75	ns	Use Test Circuit C_T 100 pf
	From Q_1 to Q_2		15	30	ns	Use Test Circuit C_T 100 pf
	From Q_2 to Q_2		15	30	ns	Use Test Circuit C_T 100 pf
	From Q_2 to Q_1		18	35	ns	Use Test Circuit C_T 100 pf
T_{pd-}	From Q_2 to Q_2		8	15	ns	Use Test Circuit C_T 100 pf
	From Q_1 to Q_2		20	45	ns	Use Test Circuit C_T 100 pf
t_{po}	Output pulse width					
	C_T = 0pf, R_T = 1.5Ω→10KΩ		25	35	ns	Use Test Circuit
	C_T = 100 pf, R_T = 10KΩ	600	700	800	ns	Use Test Circuit
	C_T = 1 uf, R_T = 10KΩ	6	7	8	ms	Use Test Circuit
[1] T_{min},	Minimum width pulse into:					
	Trigger Inputs		30	50	ns	Use Test Circuit
	Inhibit Oscillator		10	15	ns	Use Test Circuit
	T set-up			10	ns	Use Test Circuit

T_{min} = The hold time which is the interval immediately following the trigger transition, during which interval the input must be maintained at the steady state level shown in the Truth Table to ensure correct operation. Applied to the inhibit oscillator input, t_{min}, is the minimum input pulse width required to ensure the generation of one period of oscillator, with the other inputs at the logic levels given in the truth table.

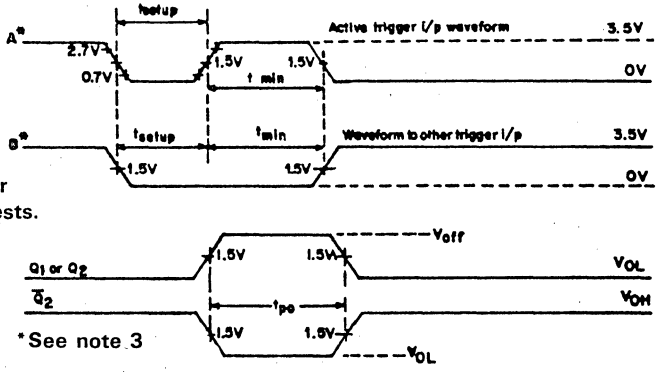
Test Circuit





T_{pd} Voltage Waveform

Note: 1. T_{pd} + Q_2 output to Q_1 output progagation delay when in the oscillatory mode, apply input logic levels as shown in the Truth Table.



Voltage Waveforms for set-up and pulse width tests.

Note: 2. The Pulse generator characteristics are:
Amplitude = 3.5V..... PRF = 1 MH
t_r = 10 ns ..... $Z_o = 50\Omega$
t_f = 4 ns..... t_p = 10 to 50 ns

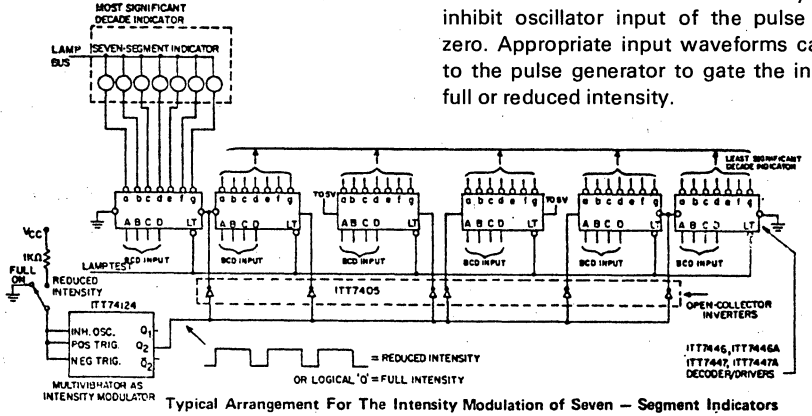
Note: 3. Use the waveforms given for triggering from the positive trigger input. Apply the inverse of both waveforms for triggering from the negative trigger transition (active input = negative trigger input). Ground the inhibt oscillator input for testing the delayed pulse mode of operation.
A positive pulse should be applied to the inhibit oscillator input to test for t min in the oscillatory mode of operation.

APPLICATION NOTES

The universal pulse generator has been specifically designed for clock and delayed pulse generation. However, full use can be made if its two modes of operation to perform functions previously requiring many logic devices in a wide variety of logic circuits, for example in timing pulse generation where several monostables and gates are employed. The following application notes show a selection of these applications to illustrate some useful features of the device.

INTENSITY MODULATOR

Modulation of the intensity of seven segment indicators driven from decoder/drivers can be easily achieved using the universal pulse generator. Using variable timing components the duty cycle of the modulating waveform from the pulse generator can be altered to adjust the indicator brightness. The indicators can be run at full intensity by taking the inhibit oscillator input of the pulse generator to zero. Appropriate input waveforms can be applied to the pulse generator to gate the indicators from full or reduced intensity.



Typical Arrangement For The Intensity Modulation of Seven – Segment Indicators

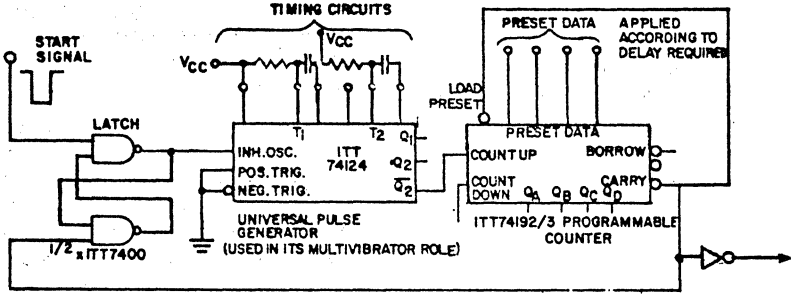
LONG TIMING PERIODS

GENERAL PURPOSE APPLICATIONS

It is possible to use large timing capacitors up to 1,000µf to produce timing periods up to about 40 seconds. However, the recommended maximum timing capacitor of 50µf has been set to permit precise operation and good stability from the universal pulse generator (timing periods to 1 second). Several problems occur when using very large capacitors. The relative high leakage current of electrolytics makes accurate timing difficult and the normal operation of the pulse generator cannot be guaranteed with very long timing periods. However, for some general purpose applications large timing capacitors may be used up to 1,000µf. A settling down period after switch-on of the supply is recommended. The maximum mark-space ratio will also depend upon the timing period length.

ACCURATE LONG TIMING PERIOD

An arrangement which takes advantage of the high stability of the pulse generator when using lower capacitance values is shown below.



Typical Arrangement for Long Timing Periods Short Pulse Obtained After Long Delay.

The universal pulse generator is used in its oscillator mode with the output pulses counted by the programmable counter. A start signal initiates the train of pulses which causes the counter to advance to its highest state. The next input clock pulse appears at the carry output with the same pulse width and this is the desired output pulse of duration equal to the second timing period of the universal pulse generator. The delay time period depends primarily on the period of the output from the pulse generator and the initial preset state of the programmable counter.

In the arrangement shown the counter output is used to preset the counter to a state depending on the preset data input. The long delay can therefore be varied using the preset data inputs. The carry output also resets the input latch so inhibiting further output pulses from the pulse generator.

Very long delays can be obtained by cascading the counters using the same basic carry output arrangement from the last counter. In calculating delays the ripple delay from cascaded counters must be taken into account.

By incorporating an additional latch in the circuit the same basic arrangement can be used to produce short delay and long pulse outputs.

FREQUENCY SYNCHRONISM

By applying appropriate waveforms to the pulse generator inputs as determined from the device operation modes the output frequency can be synchronized to an input frequency (usually a multiple of the output frequency desired). The range of synchronism is dependent on the ratio of the input and output frequencies, the ratio of the two timing periods the input mark-space ratio and any restrictions such as minimum input pulse widths.

Equal mark-space output waveforms can be obtained using an additional flip-flop toggled from the pulse generator output.

EXAMPLE Pulse Frequency Divider.

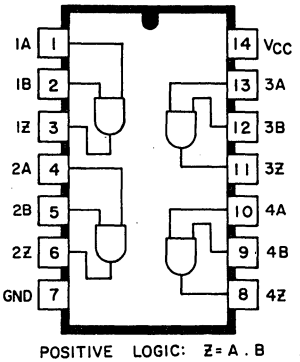
Basically the universal pulse generator should be arranged to give the desired output frequency and short positive pulses applied to the inhibit oscillator input at a frequency slightly slower than some multiple of the natural frequency of the device. Output waveforms of a frequency division of the input pulse frequency can be obtained i.e. ÷ 10, ÷ 1.5, ÷ 2/3 etc.

ITT SEMICONDUCTORS

QUAD 2-INPUT AND BUFFERS WITH OPEN COLLECTOR OUTPUT

- High Current and High Voltage Drivers
- Inputs Are Compatible With All Other 74 Series Devices
- Large Wire-AND Capability

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



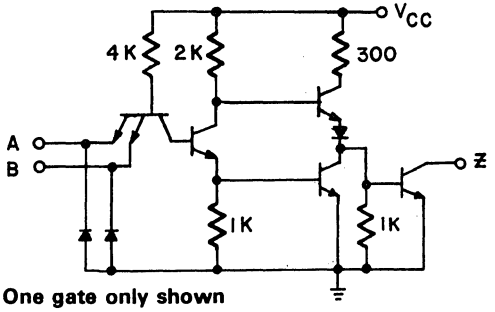
POSITIVE LOGIC: Z = A . B

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Output voltage (see Notes 1 and 2):
ITT54130, ITT74130 ..... 30V
ITT54131, ITT74131 ..... 15V
Operating free-air temperature range:
ITT54130, ITT54131 ..... −55°C to 125°C
ITT74130, ITT74131 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

Circuit Schematic



One gate only shown

recommended operating conditions

		ITT54130, ITT54131			ITT74130, ITT74131			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	ITT54130, ITT74130			30			30	V
	ITT54131, ITT74131			15			15	V
Low-level output current, I_{OL}				100			100	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_I = 2V, V_{OH} = MAX
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_I = 0.8V, I_{OL} = 100mA
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		12	24	mA	V_{CC} = MAX, V_I = 5V
I_{CCL}	Supply current, low-level output		47	75	mA	V_{CC} = MAX, V_I = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output			18	ns	C_L = 15 pF, R_L = 50Ω
t_{PHL}	Propagation delay time, high-to-low-level output			35	ns	C_L = 15 pF, R_L = 50Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type

ITT SEMICONDUCTORS

QUAD 2-INPUT POSITIVE, NAND SCHMITT TRIGGER, HEX INVERTER SCHMITT TRIGGER

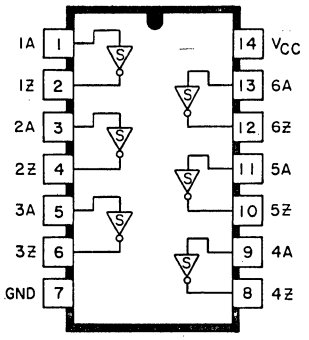
- High Input Impedance — Input Directly Compatible With 74L
- Applications Include Pulse Shaping, Clock Generation, and Interfacing to T.T.L. From 74L, T.T.L., D.T.L., M.O.S., H.L.L. and High Voltage Transducers
- Temperature Compensated Thresholds
- Hysteresis 0.8V
- Operates From Slow Rise and Fall Time Signals
- 15V Input Rating

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

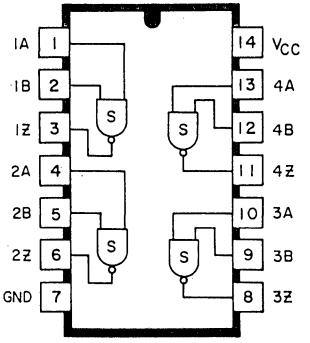
Voltage between inputs (ITT74137) 15.0V
Continuous input current 1.0mA
Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 15.0V
Operating free-air temperature range:
ITT54135, ITT54137 ..... −55°C to 125°C
ITT74135, ITT74137 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.

ITT54/74135
DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



ITT54/74137
DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



recommended operating conditions

		ITT54135/7			ITT74135/7			
		Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55		125	0	25	70	°C
Maximum input rise and fall times		No restriction			No restriction			

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter			Min	Typ	Max	Unit	Test Conditions
V_{T+}	Positive-going threshold voltage		1.5	1.7	2	V	V_{CC} = 5V
V_{T-}	Negative-going threshold voltage		0.6	0.9	1.1	V	V_{CC} = 5V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5V
V_I	Input clamp voltage				−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage		2.4	3.3		V	V_{CC} = MIN, V_I = 0.6V, I_{OH} = −800uA
V_{OL}	Low-level output voltage			0.22	0.4	V	V_{CC} = MIN, V_I = 2V, I_{OL} = 16mA
I_{T+}	Input current at positive-going threshold			74		uA	V_{CC} = 5V, V_I = V_{T+}
I_{T-}	Input current at negative-going threshold			97		uA	V_{CC} = 5V, V_I = V_{T-}
I_I	Input current at maximum input voltage				100	uA	V_{CC} = MAX, V_I = 15.0V
I_{IH}	High-level input current				10	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current				0.18	mA	V_{CC} = MAX, V_I = 0.3V
I_{OS}	Short-circuit output current [3]		−18		−55	mA	V_{CC} = MAX
I_{CCH}	Supply current high-level output	54/74135		6	12	mA	V_{CC} = MAX, V_I = 0
		54/74137		9	18		
I_{CCL}	Supply Current low-level output	54/74135		22	35	mA	V_{CC} = MAX, V_I = 4.5V
		54/74137		33	52		

[1] All typical values are at V_{CC} = 5V, T_A = 25°C

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

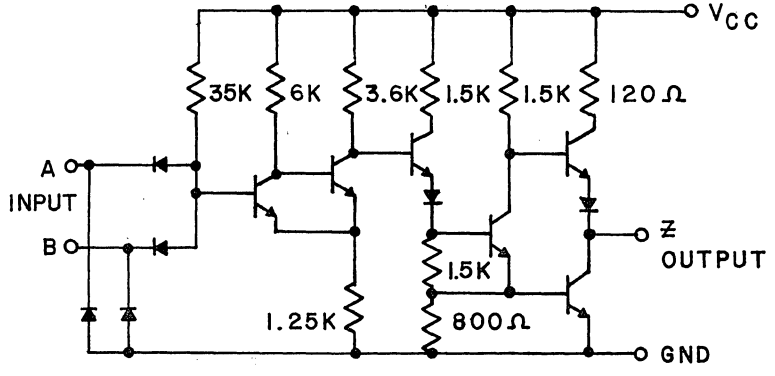
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output		20	30	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level output		25	37	ns	C_L = 15 pF, R_L = 400 Ω

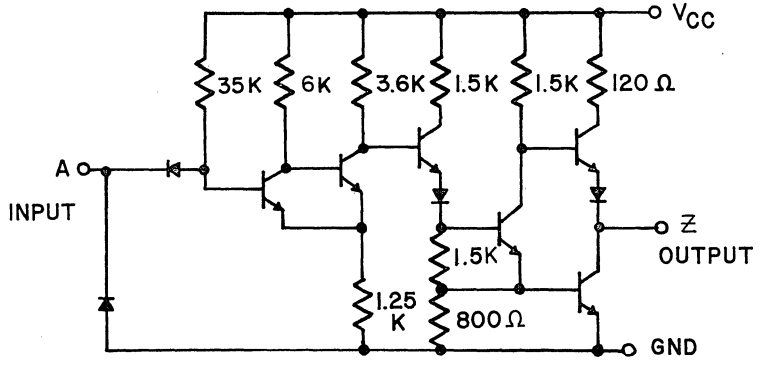
Circuit Diagram

ITT54/74135



Circuit Diagram

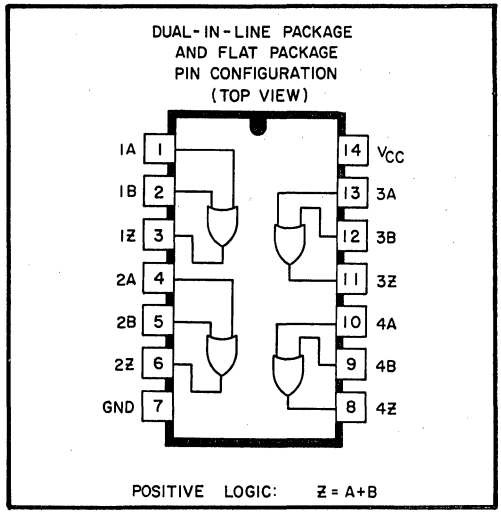
ITT54/74137



ITT SEMICONDUCTORS

QUAD 2-INPUT OR BUFFER WITH OPEN COLLECTOR OUTPUT

- **High Current and High Voltage Drivers**
- **Inputs Are Compatible With All Other 74 Series Devices**
- **Large Wire-AND Capability**

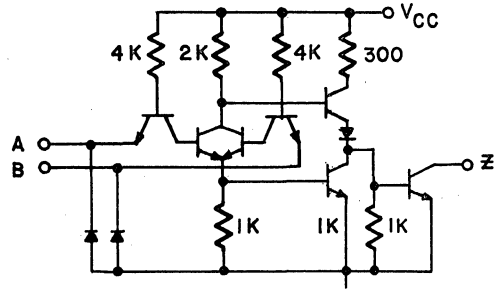


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Output voltage (see Notes 1 and 2):
ITT54138, ITT74138 ..... 30 V
ITT54139, ITT74139 ..... 15 V
Operating free-air temperature range:
ITT54138, ITT54139 ..... −55°C to 125°C
ITT74138, ITT74139 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values, are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

Circuit Schematic



One gate only shown

recommended operating conditions

		54138, 54139			74138, 74139			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	ITT54138, ITT74138			30			30	V
	ITT54139, ITT74139			15			15	V
Low-level output current, I_{OL}				100			100	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_I = 2V, V_{OH} = MAX
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_I = 0.8V I_{OL} = MAX
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{CCH}	Supply current, high-level output		30	42	mA	V_{CC} = MAX, V_I = 0
I_{CCL}	Supply current, low-level output		27	38	mA	V_{CC} = MAX, V_I = 5V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

	Parameter	Min	TYP	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output			16	ns	C_L = 15pF, R_L = 50Ω
t_{PHL}	Propagation delay time, high-to-low-level output			35	ns	C_L = 15pF, R_L = 50Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

BCD-TO-DECIMAL DECODER/DRIVER

- **Drives gas-filled cold-cathode indicator tubes directly**
- **Fully decoded inputs ensure all outputs are off for invalid codes**
- **Input clamping diodes minimize transmission-line effects**
- **Power dissipation typically 55 mW**

logic

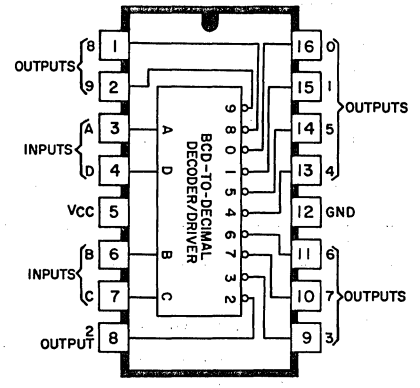
TRUTH TABLE

Input				Output
D	C	B	A	On [1]
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

[1] All other outputs are off

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE TRUTH TABLE

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

The ITT74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the ITT74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts. The ITT-74141 is characterized for operation over the temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} 7V
Input voltage (see Note 1) 5.5V
Current into any output (off-state) ..... 2 mA
Operating free-air temperature range .. 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions	**Min**	**Nom**	**Max**	**Unit**
Supply voltage V_{CC} (see Note 1)	4.75	5	5.25	V
Output voltage (see Notes 1 and 2)			65	V
Operating free-air temperature range	0	25	70	°C

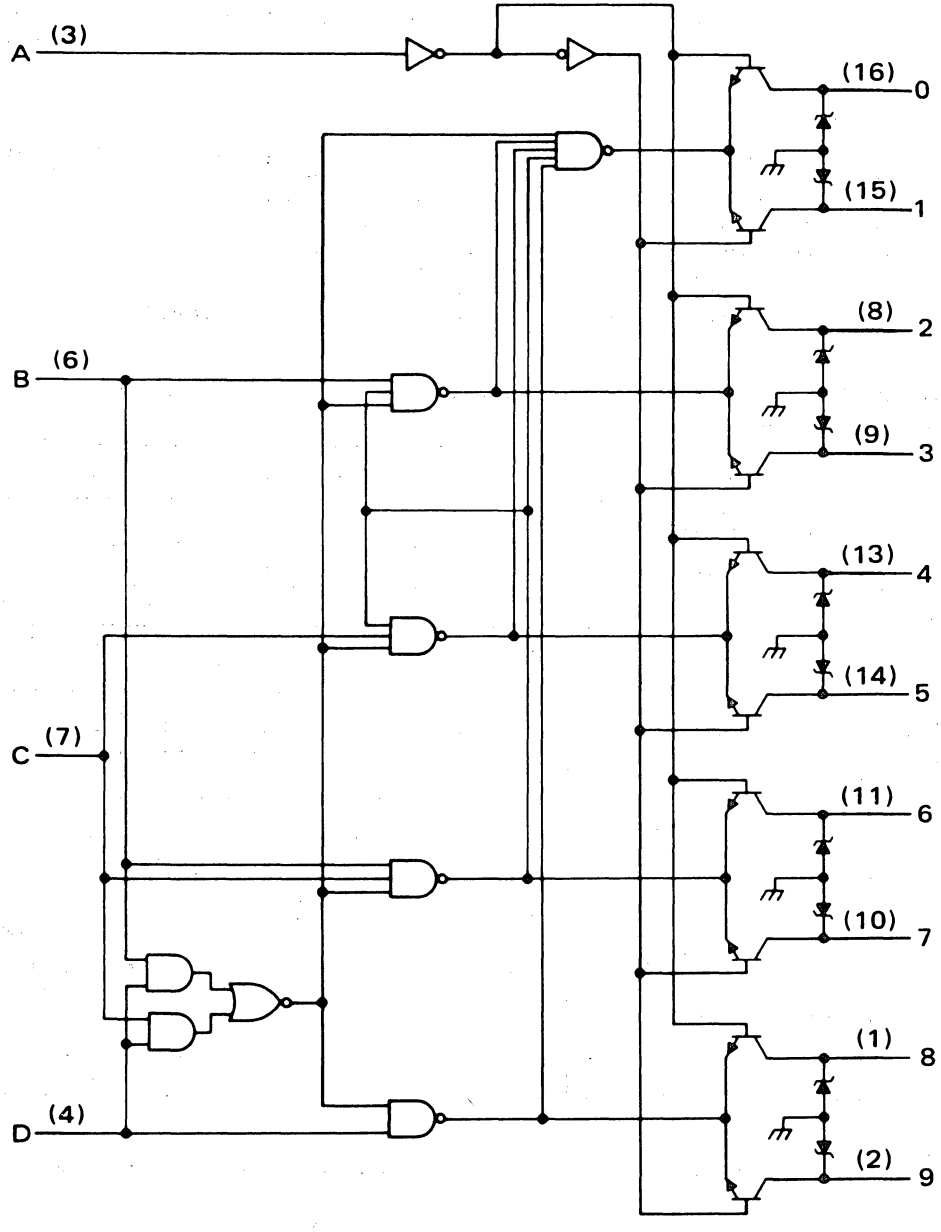
Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	**Min**	**Typ** [1]	**Max**	**Unit**	**Test Conditions** [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
$V_{O(on)}$	On-state output voltage			2.5	V	V_{CC} = MIN, I_O = 7mA
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	60			V	V_{CC} = MAX, I_O = 0.5mA
$I_{O(off)}$	Off-state reverse current			50	uA	V_{CC} = MAX, V_O = 55V
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15			5	uA	V_{CC} = MAX, V_O = 30V
I_{IH}	High-level input current at A			40	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current at B, C, or D			80	uA	V_{CC} = MAX, V_I = 2.4V
				1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current into A			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{IL}	Low-level input current into B, C, or D			−3.2	mA	V_{CC} = MAX, V_I = 0.4V
I_{CC}	Supply current		16	25	mA	V_{CC} = MAX

[1] This typical value is at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

functional block diagram



SEMICONDUCTORS

DATA SELECTORS/MULTIPLEXERS

features

- **selects one-of-sixteen (or one-of-eight) data sources**
- **serves as a five-variable-function generator (ITT54150, ITT74150)**
- **performs parallel-to-serial conversion**
- **permits multiplexing from N lines to 1 line**
- **input-clamping diodes simplify system design**
- **typical propagation delay times:**
  through 4 select levels — 28 ns
  through 3 select levels — 20 ns
  data input to output — 10 ns
- **high fan-out, low impedance, totem-pole outputs**
- **fully compatible with TTL, DTL and other MSI circuits**

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The ITT54151/ITT74151 features complementary outputs whereas the ITT54150/ITT74150 has inverted outputs only. The circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

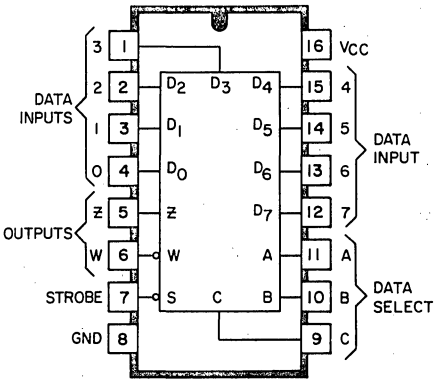
These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

ITT54150/ITT74150 — 200 milliwatts
ITT54151/ITT74151 — 145 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The ITT54150, and ITT54151, are characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74150, and ITT74151 are characterized for operation from 0°C to 70°C.

ITT54151/ITT74151

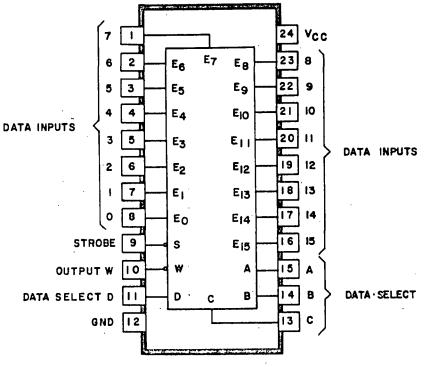
DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)[1]



$$\bar{Z} = \bar{S}(A\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}\bar{B}\bar{C}D_2 + A\bar{B}\bar{C}D_3 + \bar{A}\bar{B}\bar{C}D_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Z}$$

ITT54150/ITT74150

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)[1]



POSITIVE LOGIC

$$W = \bar{S}(A\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7 + \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

[1] Pin assignments for these circuits are the same for all packages.

logic

TRUTH TABLE (ITT54150/ITT74150 ONLY)

Inputs																			Output
D	C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (ITT54151/ITT74151 ONLY)

Inputs											Outputs	
C	B	A	Strobe(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

Note: When used to indicate an input, X = irrelevant.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Note 1) 5.5V
Operating Free-Air Temperature Range:
ITT54150, ITT54151 ..... −55°C to 125°C
ITT74150, ITT74151 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

recommended operating conditions	**Min**	**Nom**	**Max**	**Unit**
Supply Voltage V_{CC} (See Note 1): ITT54150, ITT54151	4.5	5	5.5	V
ITT74150, ITT74151	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ[1]	Max	Unit	Test Conditions[2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12 mA	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = −800 uA	
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16 mA	
$I_{in(1)}$	Logical 1 level input current (each input)			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current (each input)			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short circuit output current[3]	−20		−55	mA	V_{CC} = MAX, V_{out} = 0	ITT54150, ITT54151
		−18		−55	mA		ITT74150, ITT74151
I_{CC}	Supply current (ITT54150/ITT74150)		40	68	mA	V_{CC} = MAX, V_{in} = 4.5V	
I_{CC}	Supply current (ITT54151/ITT74151)		29	48	mA	V_{CC} = MAX, V_{in} = 4.5V	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

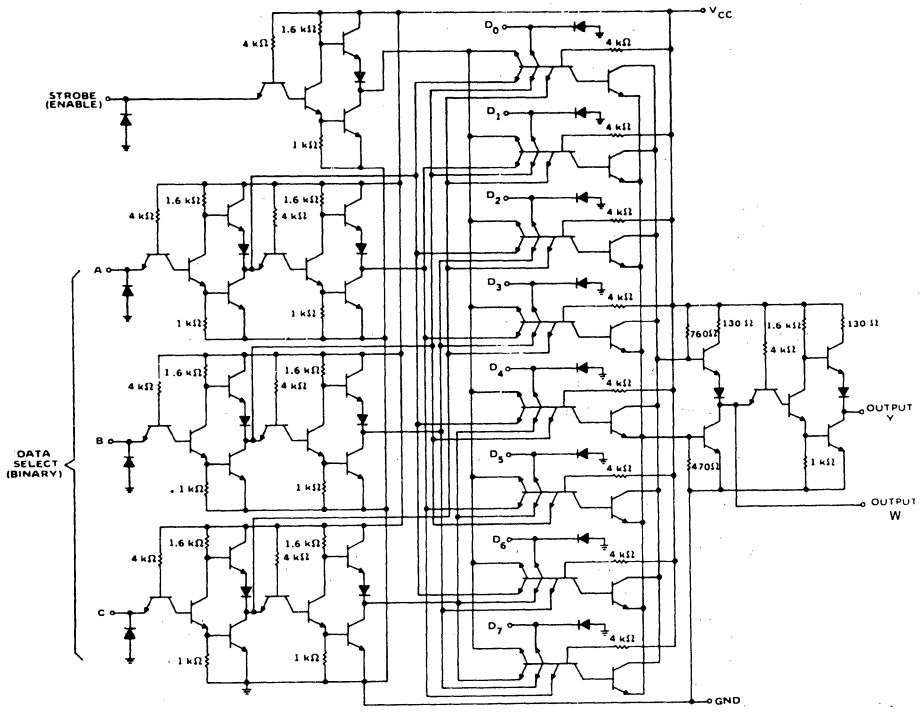
Parameter	From (Input)	To (Output)	Min	Typ	Max	Unit	Conditions
t_{pd0}	A, B, or C (4 levels)	Y		20	30	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	A, B, or C (4 levels)	Y		35	52	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	A, B, C, or D (3 levels)	W		22	33	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	A, B, C, or D (3 levels)	W		23	35	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	STROBE	Y		19	30	ns	C_L = 15 pF, R_L = 400 Ω

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter	From (Input)	To (Output)	Min	Typ	Max	Unit	Conditions
t_{pd1}	STROBE	Y		35	52	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	STROBE	W		21	30	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	STROBE	W		15.5	24	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	D_0 thru D_7	Y		16	24	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	D_0 thru D_7	Y		19	29	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}	E_0 thru E_{15} D_0 thru D_7	W		8.5	14	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	E_0 thru E_{15} D_0 thru D_7	W		13	20	ns	C_L = 15 pF, R_L = 400 Ω

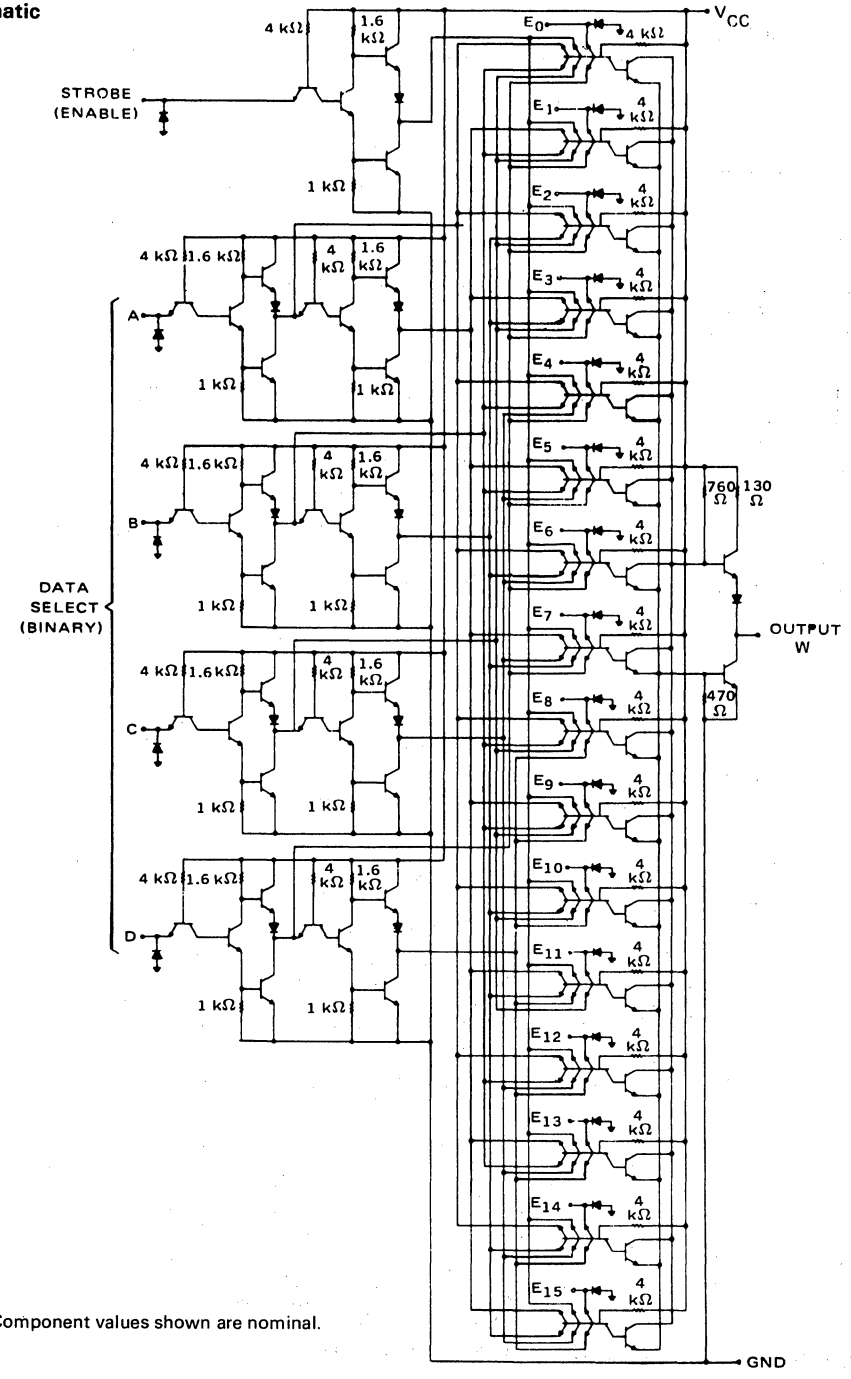
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
[3] Not more than one output of the ITT54151/ITT74151 should be shorted at a time.

schematic



Note: Component values shown are nominal.

schematic



Note: Component values shown are nominal.

DUAL 4-LINE-TO-1 LINE DATA SELECTORS/MULTIPLEXERS

- **Permits Multiplexing from N lines to 1 line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Typical Average Propagation Delay Times:**
  - **Data Input to Output ..... 14 ns**
  - **Strobe Input to Output ..... 17 ns**
  - **Select Input to Output ..... 22 ns**
- **High-Fan-Out, Low Impedance, Totem-Pole Outputs**
- **Fully Compatible with most TTL and DTL Circuits**

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

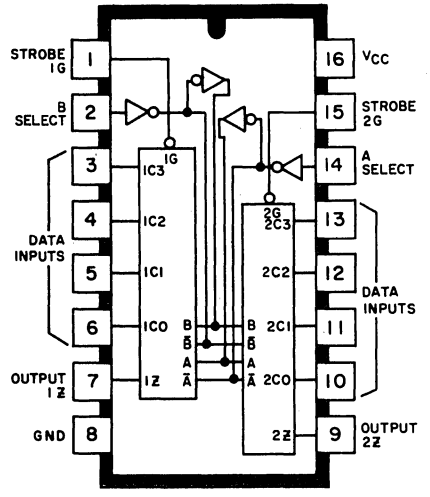
Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The ITT54153 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Operating free-air temperature range:
ITT54153 ..... −55°C to 125°C
ITT74153 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1. Voltage values are with respect to network ground terminal.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE TRUTH TABLE

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Z
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

recommended operating conditions

		ITT54153			ITT74153			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA	
V_{OH}	High-level output voltage	2.4	3.1		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA	
V_{OL}	Low-level output voltage		0.2	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT54153
		−18		−57			ITT74153
I_{CCL}	Supply current, low-level output		36	52	mA	V_{CC} = MAX	ITT54153
			36	60			ITT74153

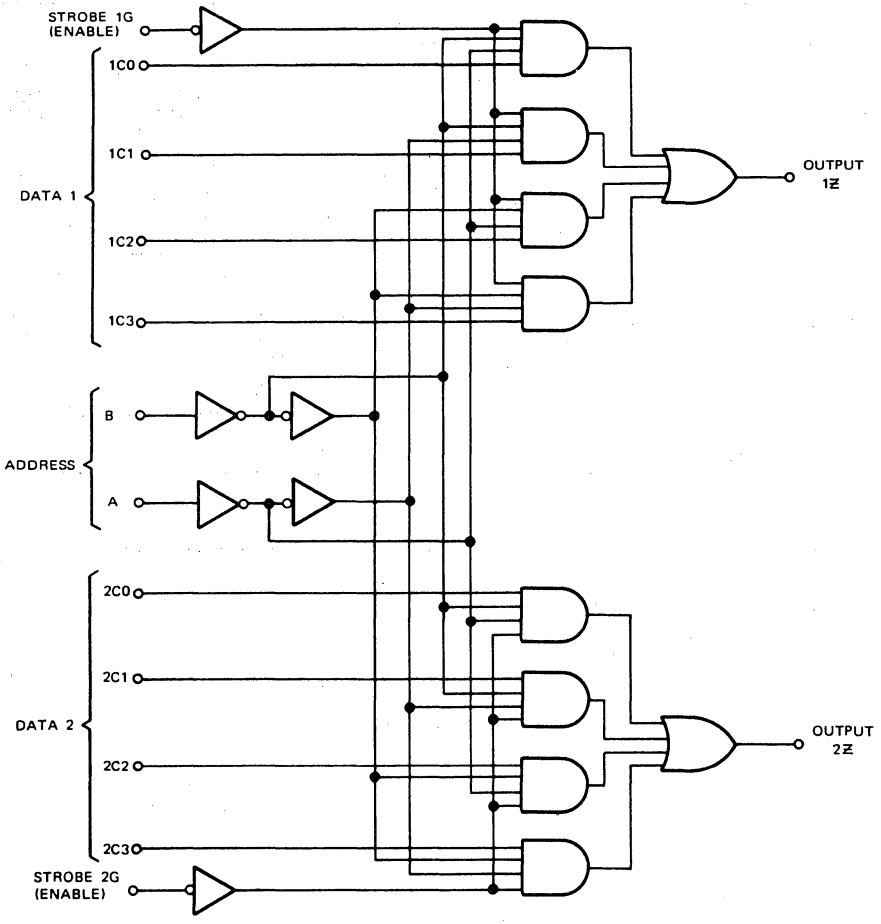
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

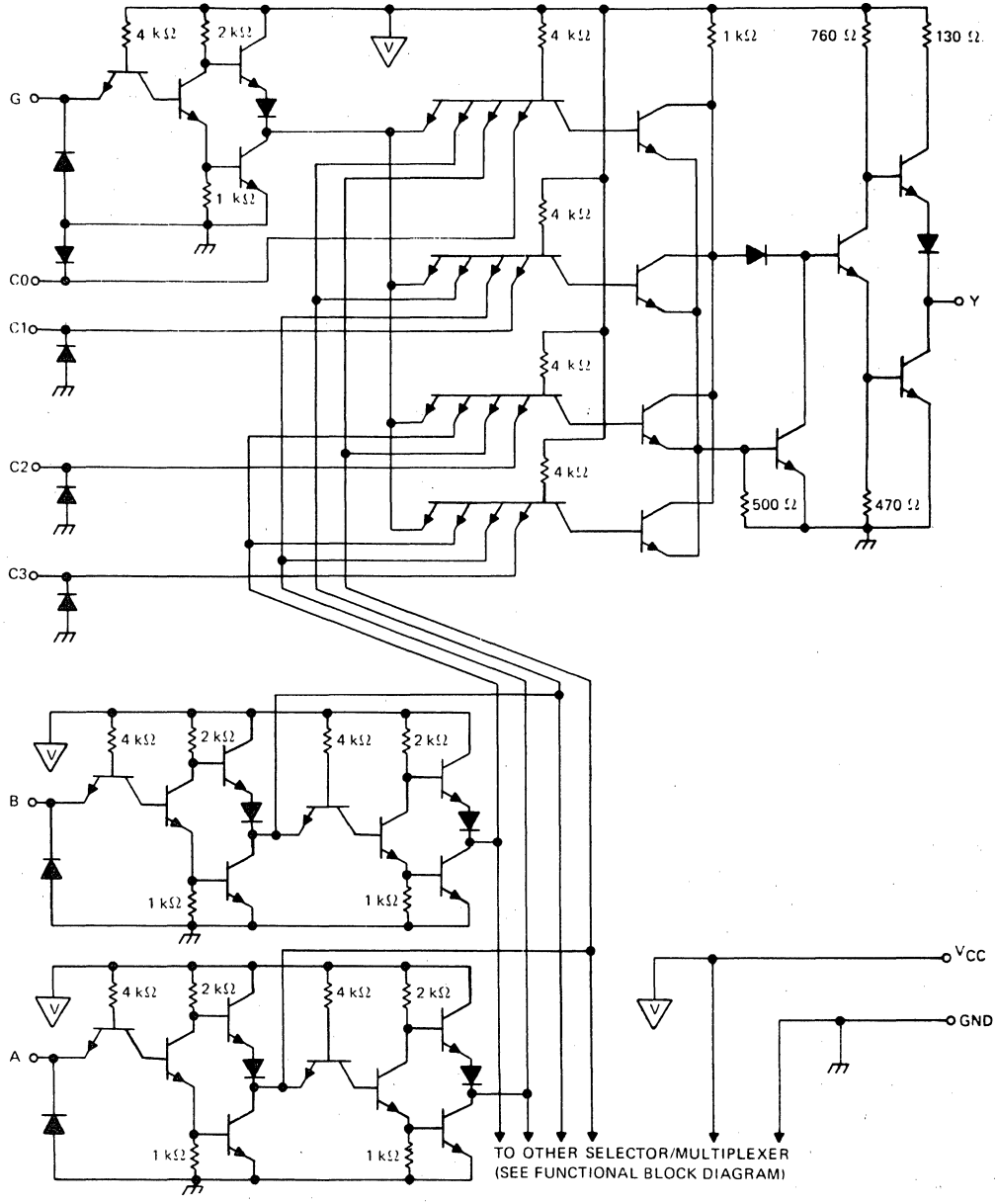
Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Conditions
t_{PLH}	Data	Z		12	18	ns	C_L = 30 pF, R_L = 400 Ω
t_{PHL}	Data	Z		15	23	ns	C_L = 30 pF, R_L = 400 Ω
t_{PLH}	Address	Z		22	34	ns	C_L = 30 pF, R_L = 400 Ω
t_{PHL}	Address	Z		22	34	ns	C_L = 30 pF, R_L = 400 Ω
t_{PLH}	Strobe	Z		19	30	ns	C_L = 30 pF, R_L = 400 Ω
t_{PHL}	Strobe	Z		15	23	ns	C_L = 30 pF, R_L = 400 Ω

[1] t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

functional block diagram



schematic (each selector/multiplexer, and the common address section)



NOTE: Component values shown are nominal.

$-V_{CC}$ bus

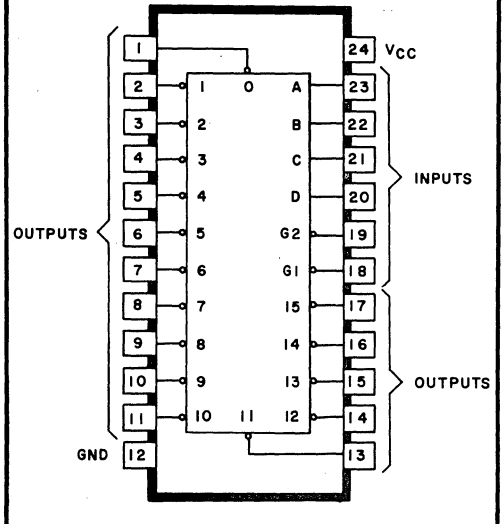
ITT SEMICONDUCTORS

4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

FOR APPLICATIONS IN COMMUNICATIONS EQUIPMENT COMPUTERS, AND ELECTRONIC INSTRUMENTATION

- **Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs**
- **Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs**
- **Input clamping diodes simplify system design**
- **High fan-out, low-impedance, totem-pole outputs**
- **Typical average propagation delay times:**
  23 ns through 3 levels of logic
  19 ns from strobe input
- **Typical power dissipation ...170 mW**
- **Fully compatible with most TTL, DTL, and MSI circuits**

DUAL-IN-LINE PACKAGE AND FLAT PACKAGE PIN CONFIGURATION (TOP VIEW)†



POSITIVE LOGIC: SEE TRUTH TABLE

† Pin assignments for these circuits are the same for all packages.

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state and 20 in the high-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The ITT54154 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74154 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Operating free-air temperature range:
ITT54154 ..... −55°C to 125°C
ITT74154 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		ITT54154			ITT74154			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800 uA	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT54154
		−18		−57			ITT74154
I_{CC}	Supply current		34	49	mA	V_{CC} = MAX	ITT54154
			34	56			ITT74154

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

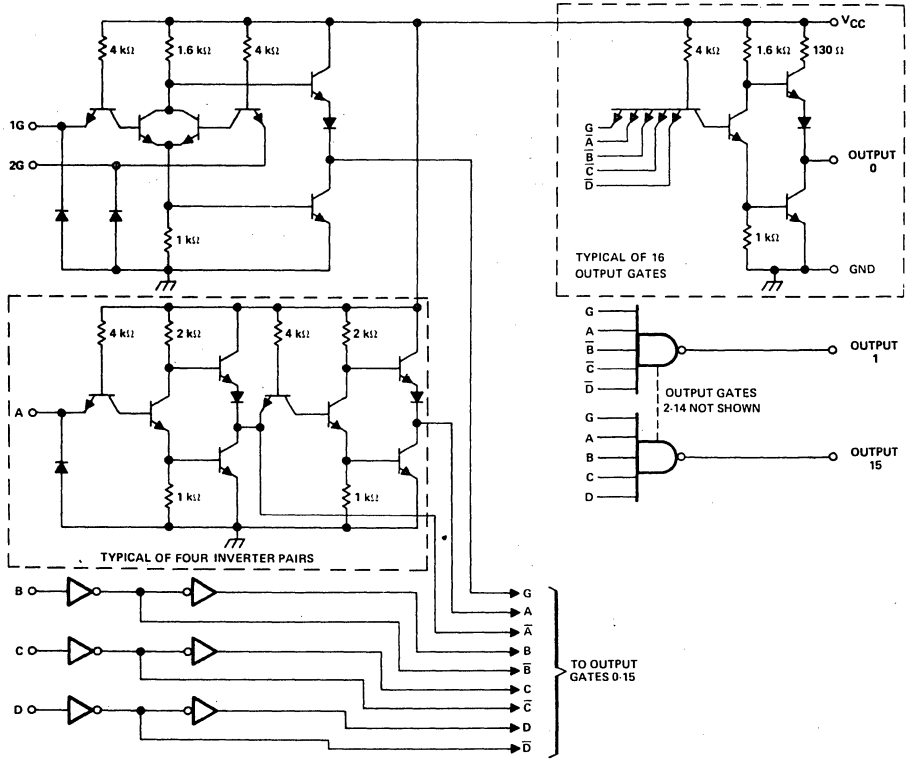
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic		24	36	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic		22	33	ns	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input		20	30	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output from either strobe input		18	27	ns	C_L = 15 pF, R_L = 400Ω

TRUTH TABLE

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

schematic

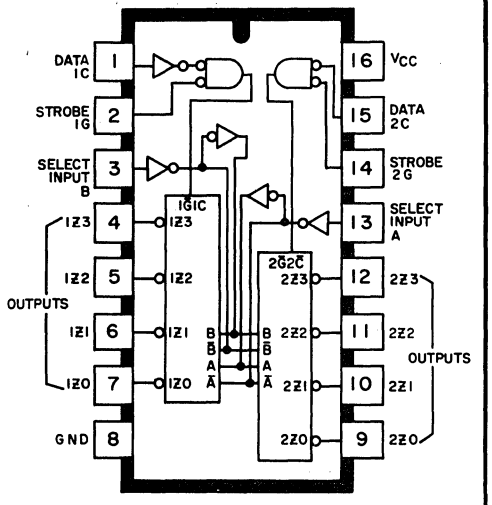


Note: Component values shown are nominal.

DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

- **Applications:**
  - **Dual 2-to-4-Line Decoder**
  - **Dual 1-to-4-Line Demultiplexer**
  - **3-to-8-Line Decoder**
  - **1-to-8-Line Demultiplexer**
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
  - **Totem Pole (ITT54155, ITT74155)**
  - **Open-Collector (ITT54156, ITT74156)**
- **Typical Average Propagation Delay Times:**
  - **16 ns through 2 levels of logic**
  - **21 ns through 3 levels of logic**
- **Typical Power Dissipation...125 mW**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE TRUTH TABLE

† Pin assignments for these circuits are the same for all

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

The ITT54155/ITT74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The ITT54156/ITT74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the ITT54155/ITT74155.

The ITT54155 and ITT54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74155 and ITT74156 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Operating free-air temperature range:
ITT54155, ITT54156 ..... −55°C to 125°C
ITT74155, ITT74156 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1. Voltage values are with respect to network ground terminal.

truth tables (H • high level, L • low level, X • irrelevant)

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

Inputs				Outputs			
Select		Strobe	Data				
B	A	1G	1C	1Z0	1Z1	1Z2	1Z3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	2G	2C	2Z0	2Z1	2Z2	2Z3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C[1]	B	A	G[2]	2Z0	2Z1	2Z2	2Z3	1Z0	1Z1	1Z2	1Z3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

[1] C = inputs 1C and 2C connected together
[2] G = inputs 1G and 2G connected together

recommended operating conditions

		ITT54155			ITT74155			
		Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

	ITT54156			ITT74156			
	Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT54155, ITT74155 Min	Typ[1]	Max	Unit	Test Conditions[2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = −800uA	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA	
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current[3]	−20		−55	mA	V_{CC} = MAX	ITT54155
		−18		−57			ITT74155
I_{CC}	Supply current		25	35	mA	V_{CC} = MAX	ITT54155
			25	40			ITT74155

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT54156, ITT74156 Min	Typ[1]	Max	Unit	Test Conditions[2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
I_{OH}	High-level output current			250	uA	V_{CC} = MIN, V_I = 2V, V_{OH} = 5.5V	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA	
I_{IH}	High-level input current (each input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (each input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{CC}	Supply current		25	35	mA	V_{CC} = MAX	ITT54156
			25	40			ITT74156

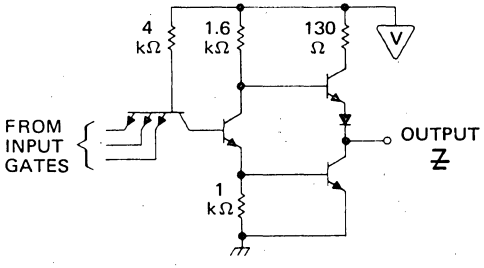
[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

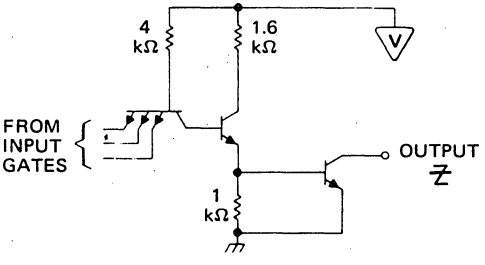
Parameter [1]	From (Input)	To (Output)	Levels of Logic	ITT54155, ITT74155			ITT54156, ITT74156			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max		
t_{PLH}	A, B, 2C, 1G, or 2G	Z	2		13	20		15	23	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	A, B, 2C, 1G, or 2G	Z	2		18	27		20	30	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH}	A or B	Z	3		21	32		23	34	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	A or B	Z	3		21	32		23	34	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH}	1C	Z	3		16	24		18	27	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	1C	Z	3		20	30		22	33	ns	C_L = 15 pF, R_L = 400 Ω

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

schematic

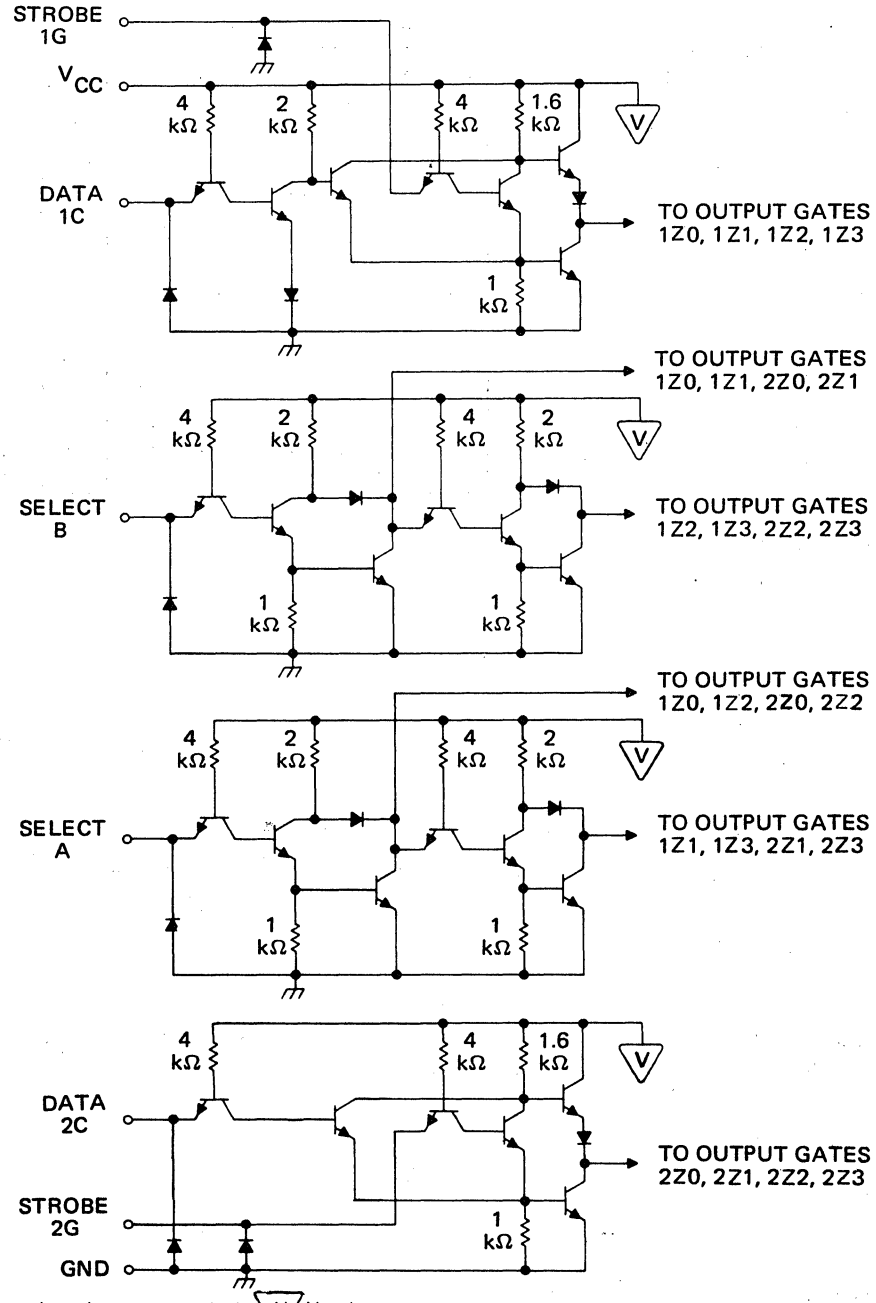


OUTPUT GATE FOR 54155, 74155
(ONE OF EIGHT SHOWN)



OUTPUT GATE FOR 54156, 74156
(ONE OF EIGHT SHOWN)

schematic



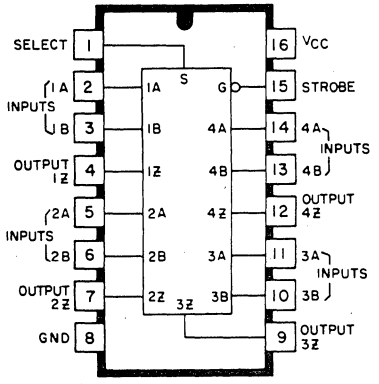
Component values shown are nominal. V...V_{CC} bus

Quadruple 2-Line-To-1-Line Data Selectors/ Multiplexers

- **Buffered Inputs and Outputs**
- **Three Speed/Power Ranges Available**
- **Typical Average Propagation Time 9 ns**
- **Typical Power Dissipation 150 mW**
- **Expand Any Data Input Point**
- **Multiplex Dual-Data Buses**
- **Generate Four Functions of Two Variables (One Variable is Common)**
- **Source Programmable Counters**

This monolithic, data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
LOW LOGIC LEVEL AT S SELECTS A INPUTS.
HIGH LOGIC LEVEL AT S SELECTS B INPUTS.

FUNCTION TABLE

INPUT				OUTPUT
STROBE	SELECT	A	B	$\overline{Z}$
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) 7v
Input voltage 5.5V
Operating free-air temperature range: 54157 ..... — 55°C to 125°C
74157 ..... 0°C to 70°C
Storage temperature range: ..... — 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

Recommended operating conditions

	54157			74157			
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			— 800			— 800	uA
Low-level output current, IOL			16			16	mA
Operating free-air temperature TA	— 55		125	0		70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	TYP‡	MAX	UNIT	TEST CONDITIONS†
VIH	High-level input voltage	2			V	
VIL	Low-level input voltage			0.8	V	
VI	Input clamp voltage			— 1.5	V	VCC = MIN, I_I = — 12mA
VOH	High-level output voltage	2.4	3.4		V	VCC = MIN, VIH = 2V, VIL = 0.8V, IOH = — 800uA
VOL	Low-level output voltage		0.2	0.4	V	VCC = MIN, VIH = 2V, VIL = 0.8V, IOL = 16mA
II	Input current at maximum input voltage			1	mA	VCC = MAX, VI = 5.5V
IIH	High-level input current			40	uA	VCC = MAX, VI = 2.4V
IIL	Low-level input current			— 1.6	mA	VCC = MAX, VI = 0.4V
IOS	Short-circuit output current §	— 20*		— 55	mA	VCC = MAX
ICC	Supply current		30	48	mA	VCC = MAX, See Note 2

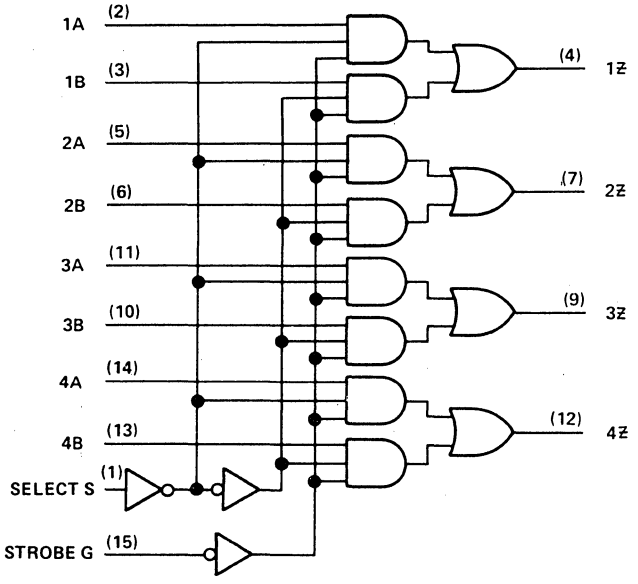
* ITT74157 MIN is — 18.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at VCC = 5V, TA = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: ICC is measured with 4.5V applied to all inputs and all outputs open.

Switching characteristics, VCC = 5V, TA = 25°C

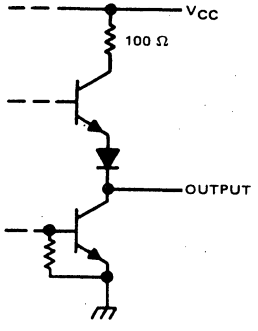
PARAMETER	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Data	CL = 15pF, RL = 400 Ω		9	14	ns
tPHL				9	14	ns
tPLH	Strobe			13	20	ns
tPHL				14	21	ns
tPLH	Select			15	23	ns
tPHL				18	27	ns

tPLH = propagation delay time, low-to-high-level output
tPHL = propagation delay time, high-to-low-level output

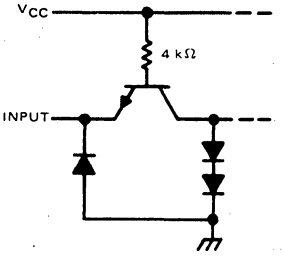
Block Diagram



TYPICAL OF ALL OUTPUTS



EQUIVALENT OF EACH INPUT



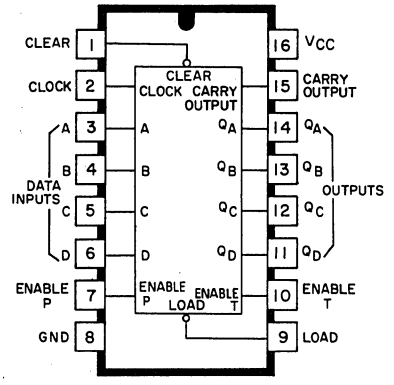
ITT SEMICONDUCTORS

SYNCHRONOUS 4-BIT COUNTERS

ITT54160, ITT54161, ITT74160, ITT74161,...SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
ITT54162, ITT54163, ITT74162, ITT74163...FULLY SYNCHRONOUS COUNTERS

- **Internal Look-Ahead for Fast Counting Schemes**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Load Control Line**
- **Diode-Clamped Inputs**
- **Typical Maximum Input Clock Frequency...32 MHz**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE DESCRIPTION

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The ITT54160, ITT54162, ITT74160, and ITT74162 are decade counters and the ITT54161, ITT54163, ITT74161, and ITT74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either state. As presetting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the ITT54160, ITT54161, ITT74160, and ITT74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock. The clear function for the ITT54162, ITT54163, ITT74162, and ITT74163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously set the counter to 0000 (LLLL).

The carry look ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is

fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

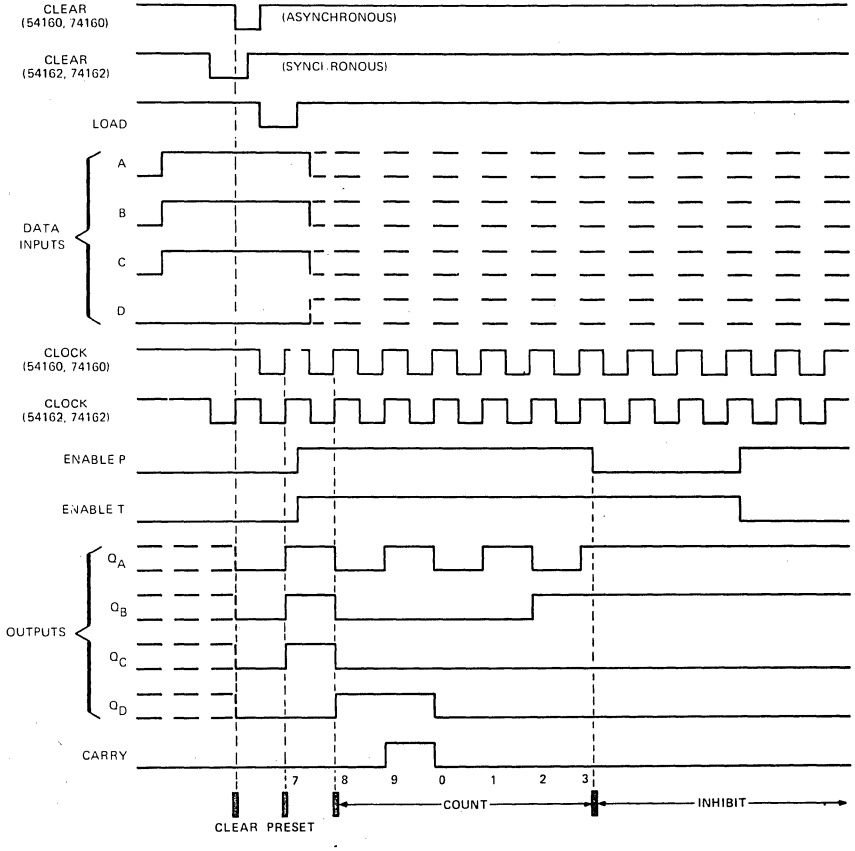
Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

ITT54160, ITT54162, ITT74160, ITT74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibt.

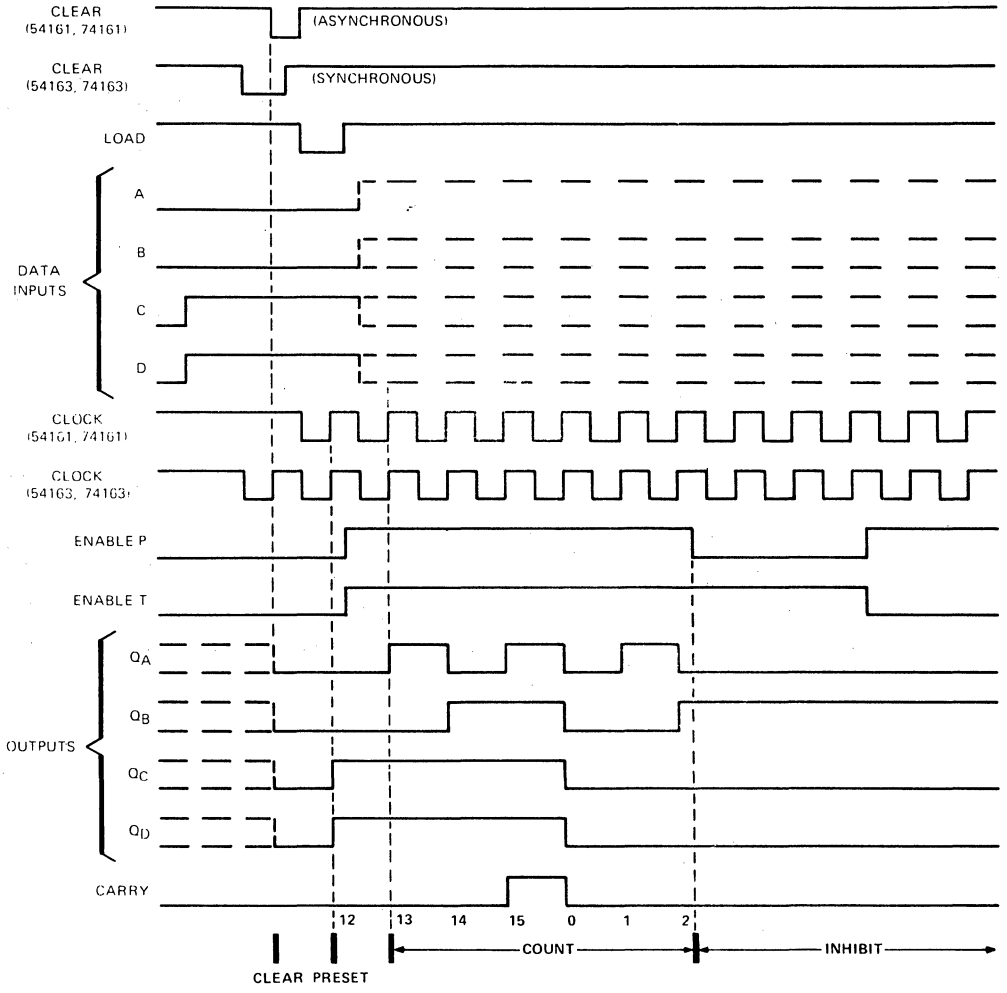


ITT54161, ITT54163, ITT74161, ITT74163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT54160, ITT54161,
ITT54162, ITT54163 Circuits... −55°C to 125°C
ITT74160, ITT74161,
ITT74162, ITT74163 Circuits..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		ITT54160, ITT54161, ITT54162, ITT54163			ITT74160, ITT74161, ITT74162, ITT74163			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			ns
	Load	15			15			ns
	Clear *	20			20			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	C

*This applies only for ITT54162, ITT54163, ITT74162, and ITT74163 which have synchronous clear inputs.

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	ITT54160, ITT54161, ITT54162, ITT54163			ITT74160, ITT74161, ITT74162, ITT74163			Unit	Test Conditions [2]
		Min	Typ [1]	Max	Min	Typ [1]	Max		
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.8			0.8	V	
V_I	Input clamp voltage			−1.5			−1.5	V	V_{CC} = MAX, I_I = −12mA
V_{OH}	High-level output voltage	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA
V_{OL}	Low-level output voltage			0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA
I_I	Input current at maximum input voltage			1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current (Clock or enable T)			80			80	uA	V_{CC} = MAX, V_I = 2.4V
I_{IH}	High-level input current (Other inputs)			40			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current (Clock or enable T)			−3.2			−3.2	mA	V_{CC} = MAX, V_I = 0.4V
I_{IL}	Low-level input current (Other inputs)			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−57	−18		−57	mA	V_{CC} = MAX
I_{CCH}	Supply current, all outputs high		59	85		59	94	mA	V_{CC} = MAX, See Note 3
I_{CCL}	Supply current, all outputs low		63	91		63	101	mA	V_{CC} = MAX, See Note 4

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

Notes: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

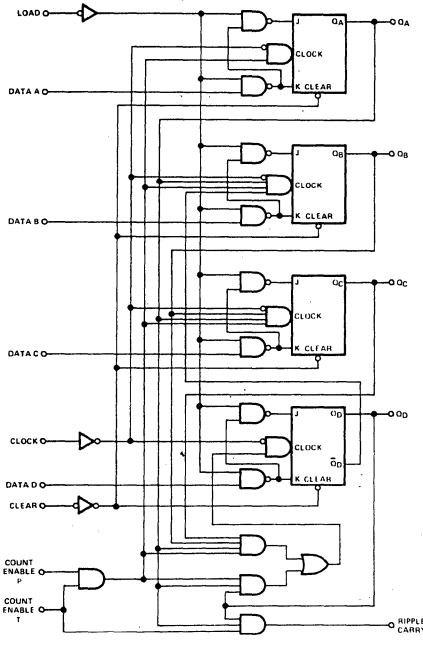
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{max}	Maximum input clock frequency	25	32		MHz	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock		23	35	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock		23	35	ns	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock		13	20	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock		15	23	ns	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T		8	13	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T		10	15	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear		20	30	ns	C_L = 15 pF, R_L = 400Ω

functional block diagrams

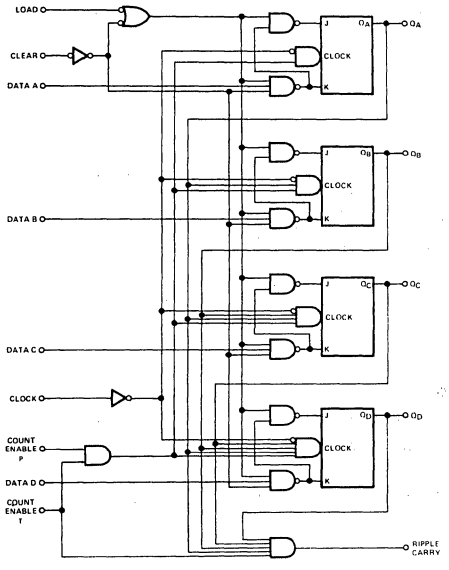
ITT54160, ITT74160 SYNCHRONOUS DECADE COUNTERS

ITT54162, ITT74162 synchronous decade counters are similar; however the clear is synchronous as shown for the ITT54163, ITT74163 binary counters at right.



ITT54163, ITT74163 SYNCHRONOUS BINARY COUNTERS

ITT54161, ITT74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the ITT54160, ITT74160 decade counters at left.



8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

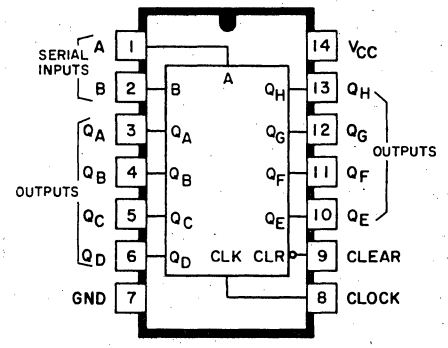
- **Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Asynchronous Clear**
- **Typical Maximum Input Clock Frequency...36 MHz**

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The ITT54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74164 is characterized for operation from 0°C to 70°C.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



LOW INPUT TO CLEAR RESETS ALL OUTPUTS TO THE LOW LEVEL.

†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

Inputs AT t_n		Output AT t_{n+1}
A	**B**	**Q_A**
H	H	H
L	H	L
H	L	L
L	L	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V

Operating free-air temperature range:
ITT54164 ..... −55°C to 125°C
ITT74164 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1: Voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT54164 Min	ITT54164 Typ [1]	ITT54164 Max	ITT74164 Min	ITT74164 Typ [1]	ITT74164 Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage			0.8			0.8	V		
V_I	Input clamp voltage			−1.5			−1.5	V	V_{CC} = MAX, I_I = −12mA	
V_{OH}	High-level output voltage	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400uA	
V_{OL}	Low-level output voltage			0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 8mA	
I_I	Input current at maximum input voltage			1			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current			40			40	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IL}	Low-level input current			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−10		−27.5	−9		−27.5	mA	V_{CC} = MAX	
I_{CC}	Supply current		30			30		mA	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4V
			37	54		37	54			$V_{I(clock)}$ = 2.4V

Note 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V, applied to clear.

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than two outputs should be shorted at a time.

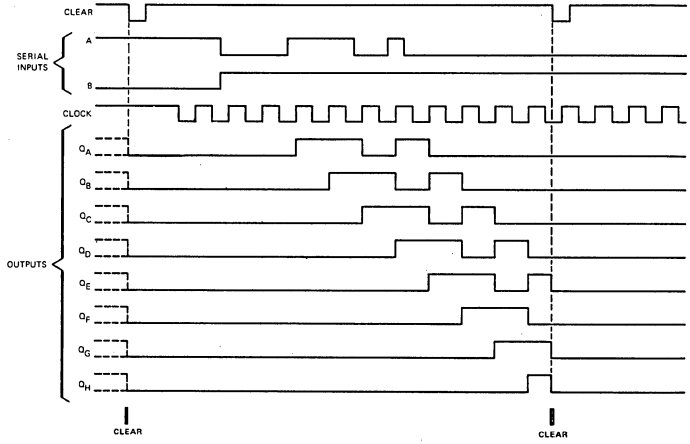
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum input count frequency	25	36		MHz	R_L = 800Ω, C_L = 15 pF
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		24	36	ns	R_L = 800Ω, C_L = 15 pF
			28	42		C_L = 50 pF R_L = 800Ω
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input	8	17	27	ns	R_L = 800Ω, C_L = 15 pF
		10	20	30		C_L = 50 pF R_L = 800Ω
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input	10	21	32	ns	R_L = 800Ω, C_L = 15 pF
		10	25	37		C_L = 50 pF R_L = 800Ω

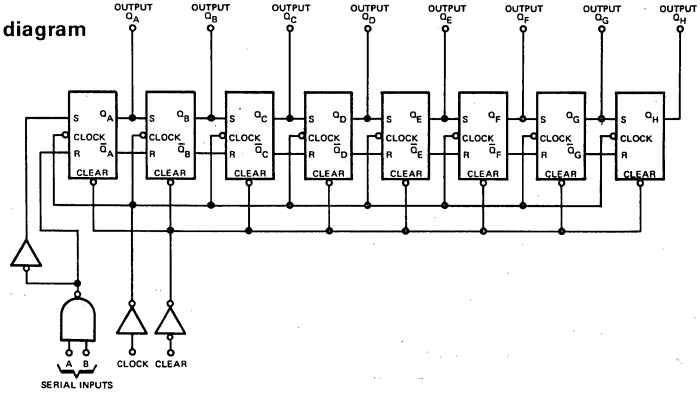
recommended operating conditions

		ITT54164			ITT74164			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			10			10	
	Low logic level			5			5	
Input clock frequency, t_{clock}		0		25	0		25	MHz
Width of clock or clear input pulse, t_w		20			20			ns
Data setup time, t_{setup} (see Figure 1)		15			15			ns
Data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

typical clear, inhibit, shift, clear, and inhibit sequences

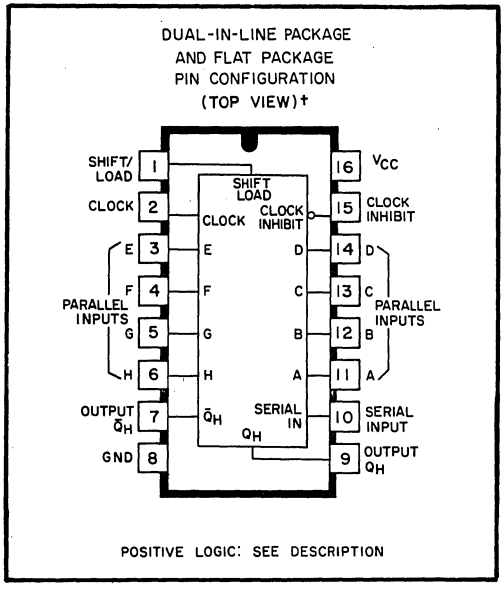


functional block diagram



PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- **Typical Maximum Input Clock Frequency...26 MHz**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**



†PIN ASSIGINMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

The ITT54165 and ITT74165 are 8-bit serial shift registers which shift the data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

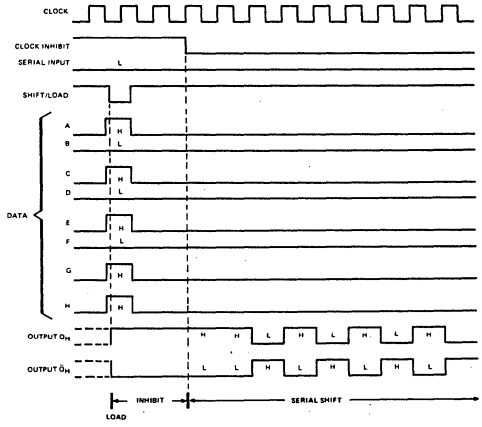
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The ITT54165 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74165 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

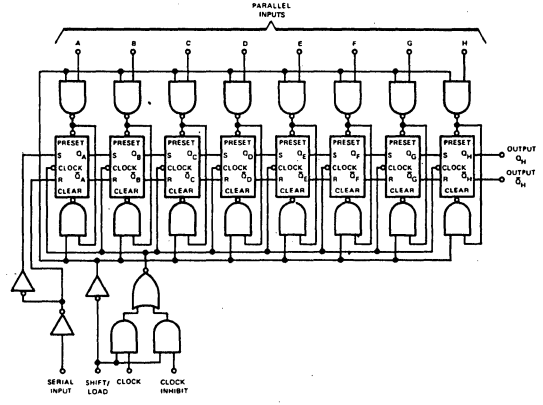
Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT54165 Circuits ..... −55°C to 125°C
ITT74165 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the shift/load input in conjunction with the clock or clock-inhibit inputs.



typical shift, load, and inhibit sequences

functional block diagram



recommended operating conditions

		ITT54165			ITT74165			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (see Figure 1)		30			30			ns
Parallel input setup time, t_{setup} (see Figure 1)		10			10			ns
Serial input setup time, t_{setup} (see Figure 2)		20			20			ns
Shift setup time, t_{setup} (see Figure 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter			ITT54165 Min	ITT54165 Typ [1]	ITT54165 Max	ITT74165 Min	ITT74165 Typ [1]	ITT74165 Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage		2			2			V	
V_{IL}	Low-level input voltage				0.8			0.8	V	
V_I	Input clamp voltage				−1.5			−1.5	V	V_{CC} = MAX, I_I = −12mA
V_{OH}	High-level output voltage		2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA
V_{OL}	Low-level output voltage				0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA
I_I	Input current at maximum input voltage				1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current	Load input			80			80	uA	V_{CC} = MAX, V_I = 2.4V
		Other inputs			40			40		
I_{IL}	Low-level input current	Load input			−3.2			−3.2	mA	V_{CC} = MAX, V_I = 0.4V
		Other inputs			−1.6			−1.6		
I_{OS}	Short-circuit output current [3]		−20		−55	−18		−55	mA	V_{CC} = MAX
I_{CC}	Supply current			42	63		42	63	mA	V_{CC} = MAX, See Note 3

Note: 3. With the outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Conditions
f_{max}			20	26		MHz	C_L = 15 pF, R_L = 400 Ω
t_{PLH}	Load	Any		21	31	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}				27	40		
t_{PLH}	Clock	Any		16	24	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}				21	31		
t_{PLH}	H	Q_H		11	17	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}				24	36		
t_{PLH}	H	Q_H		18	27	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}				18	27		

[1] f_{max} = Maximum input count frequency. t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

ITT SEMICONDUCTORS

HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

- **ITT54/74174 Contain Six Flip-Flops with Single-Rail Outputs**
- **ITT54/74175 Contain Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the ITT-54/74175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

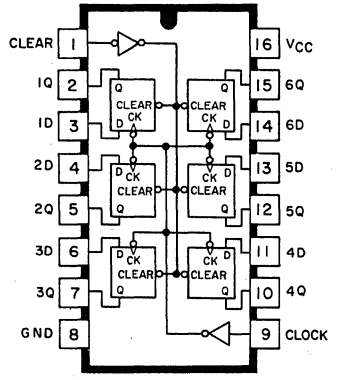
These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

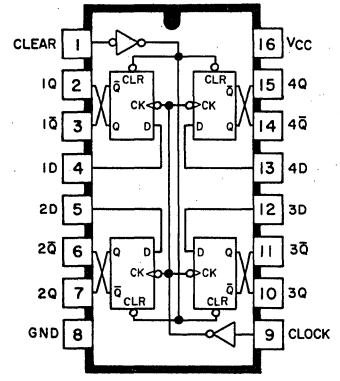
Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}^1$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
[1] = ITT54/74175

ITT74174
DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



ITT74175
DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)

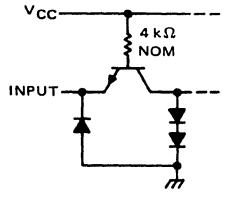


POSITIVE LOGIC: SEE FUNCTION TABLE

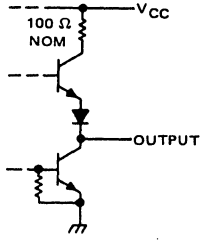
schematics of inputs and outputs

ITT54174, ITT54175, ITT74174, ITT74175

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage 5.5V

Operating free-air temperature range:
ITT54174, ITT54175 ..... −55°C to 125°C
ITT74174, ITT74175 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		ITT54174, ITT54175			ITT74174, ITT74175			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	uA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHZ
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Data input	20			20			ns
Setup time, t_{setup}	Clear inactive-state	25			25			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA	
V_{OH}	High-level output voltage	2.4	3.4		V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA	
V_O	Low-level output voltage		0.2	0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current			40	mA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	Low-level input current			−1.6	uA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX	ITT54174 ITT54175
		−18		−57			ITT74174 ITT74175
I_{CC}	Supply current		45	65	mA	V_{CC} = MAX, See Note 2	ITT54174 ITT74174
			30	45			ITT54175 ITT74175

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

Note: 2. With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to clock.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum clock frequency	25	35		MHz	C_L = 15pF, R_L = 400 Ω
t_{PLH}	Propagation delay time, low-to-high-level output from clear		16	25	ns	C_L = 15pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level output from clear		23	35	ns	C_L = 15pF, R_L = 400 Ω
t_{PLH}	Propagation delay time, low-to-high-level output from clock		20	30	ns	C_L = 15pF, R_L = 400 Ω
t_{PHL}	Propagation delay time, high-to-low-level output from clock		21	30	ns	C_L = 15pF, R_L = 400 Ω

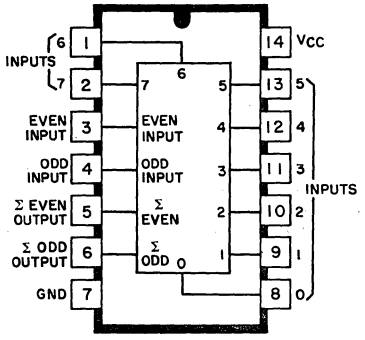
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even parity applications. The word-length capability is easily expanded by cascading.

The ITT54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The ITT54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the ITT74180 is characterized for operation from 0°C to 70°C.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage, V_{in} (See Note 1) 5.5V
Operating Free-Air Temperature Range:
ITT54180 ..... −55°C to 125°C
ITT74180 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

Note: 1. These voltage values are with respect to network ground terminal.

logic

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

recommended operating conditions

		Min	Nom	Max	Unit
Supply Voltage V_{CC} (See Note 1):	ITT54180	4.5	5	5.5	V
	ITT74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	
	Logical 1			20	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

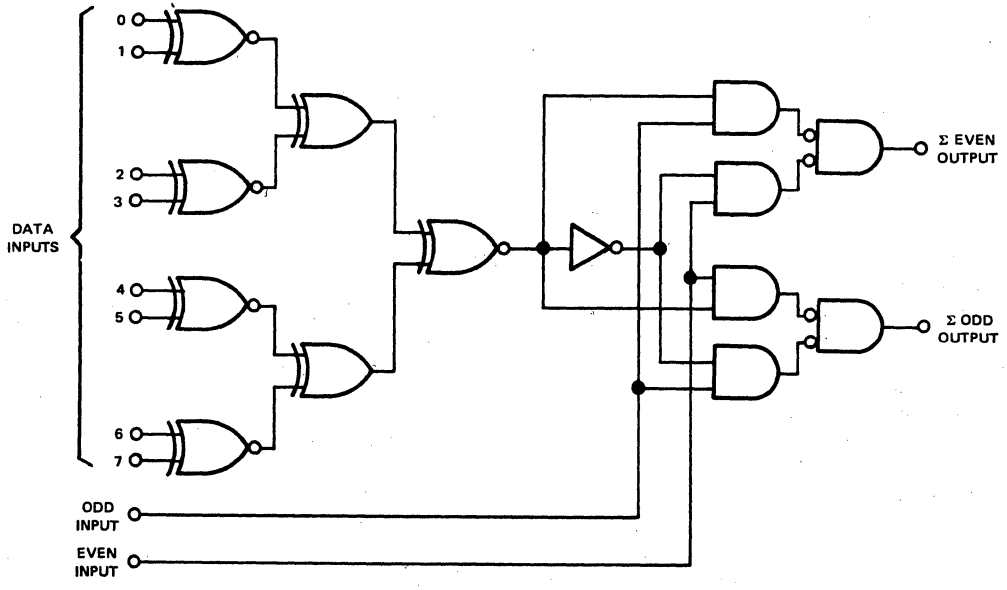
Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V		
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V		
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = 800uA	
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA	
$I_{in(1)}$	Logical 1 level input current at each data input			40	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at each data input			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4V	
$I_{in(1)}$	Logical 1 level input current at even or odd input			80	uA	V_{CC} = MAX, V_{in} = 2.4V	
				1	mA	V_{CC} = MAX, V_{in} = 5.5V	
$I_{in(0)}$	Logical 0 level input current at even or odd input			−3.2	mA	V_{CC} = MAX, V_{in} = 0.4V	
I_{OS}	Short circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT54180
		−18		−55	mA		ITT74180
I_{CC}	Supply current		34	49	mA	V_{CC} = MAX	ITT54180
			34	56	mA		ITT74180

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter	From (Input)	To (Output)	Min	Typ	Max	Unit	Conditions
t_{pd1}	Data	Σ Even		40	60	ns	C_L = 15 pF,
t_{pd0}				45	68		R_L = 400Ω
t_{pd1}	Data	Σ Odd		32	48	ns	Odd input grounded
t_{pd0}				25	38		
t_{pd1}	Data	Σ Even		32	48	ns	C_L = 15 pF,
t_{pd0}				25	38		R_L = 400Ω
t_{pd1}	Data	Σ Odd		40	60	ns	Even input grounded
t_{pd0}				45	68		
t_{pd1}	Even or Odd	Σ Even or Σ Odd		13	20	ns	C_L = 15 pF,
t_{pd0}	Even or Odd	Σ Even or Σ Odd		7	10	ns	R_L = 400Ω

functional block diagram



ITT SEMICONDUCTORS

MSI ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

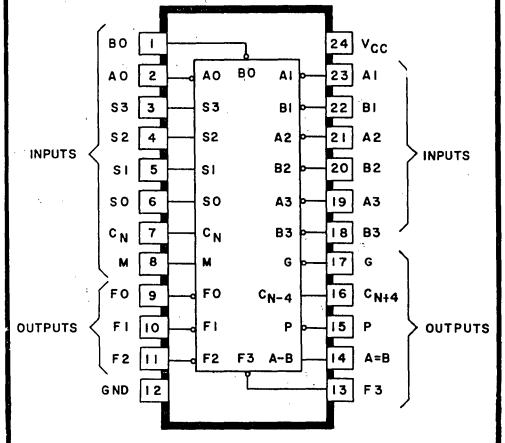
- **Full Look-Ahead for High-Speed Operations on Long Words**
- **Input Clamping Diodes Minimize Transmission-Line Effects**
- **Darlington Outputs Reduce Turn-Off Time**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
  - **Plus Twelve Other Arithmetic Operations**
- **Logic Function Modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
  - **Plus Ten Other Logical Operations**
- **Typical Add Time for Four Bits . . . . 24 ns**
- **Typical Carry Time for Four Bits . . . . 12 ns**

The ITT54181 and ITT74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the ITT54/ITT74181 for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the ITT-54182 or ITT74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the ITT-54181/ITT74181 is 24 nanoseconds for four bits. When expanding to 16-bit addition with the ITT-54182/ITT74182, only 13 nanoseconds further delay is added so that the total addition time is 37 nanoseconds, or 2.2 nanoseconds per bit. One ITT-54182/ITT74182 is needed for every 16 bits (four ITT54181/ITT74181 circuits).

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

DUAL-IN-LINE PACKAGE AND FLAT PACKAGE
PIN CONFIGURATION (TOP VIEW)†



LOGIC: SEE FUNCTION TABLES

† Pin assignments for these circuits are the same for all packages.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits. With a typical addition time of 24 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

The ITT54181 and ITT74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Figure I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y
Active-low data (Figure II)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1 which requires an end-around or forced carry to provide A−B.

The ITT54181 or ITT74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The ITT54181/ITT74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

	Input C_n	Output C n+4	Indicates
Active-High Data (Figure I)	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active-Low Data (Figure II)	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR, and OR functions.

The ITT54181/ITT74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The ITT54181 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74181 is characterized for operation from 0°C to 70°C.

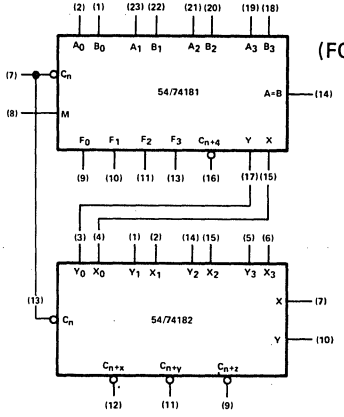


FIGURE I
(FOR TABLE I)

ALU Signal Designations

The ITT54181 and ITT74181 can be used with either the signal designations as shown in Figures I or II.

The logic functions and arithmetic operations obtained with signal designations as in Figure I are given in Table I; those obtained with the signal designations of Figure II are given in Table II.

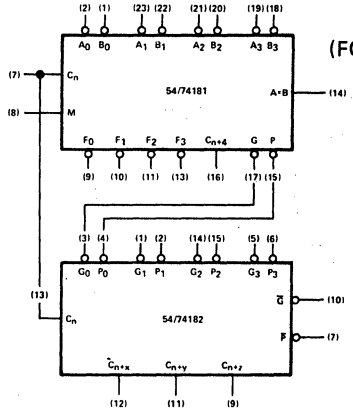


FIGURE II
(FOR TABLE II)

TABLE I

Selection S_1 S_2 S_1 S_0	Active-High Data: M = H, Logic Functions	M = L, Arithmetic Operations: $\overline{C_n} = 0$, $\overline{C_n} = 1 = H$	M = L, Arithmetic Operations: $\overline{C_n} = 1$, $\overline{C_n} = 0 = L$
L L L L	$F = \overline{A}$	F = A	F = A PLUS 1
L L L H	$F = \overline{A + B}$	F = A + B	F = (A − B) PLUS 1
L L H L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	$F = \overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	$F = \overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

* Each bit is shifted to the next more significant position.

TABLE II

Selection S_3 S_2 S_1 S_0	Active-Low Data: M = H, Logic Function	Active-Low Data: M = L; Arithmetic Operations, C_n = 0, C_n = 0 = L	Active-Low Data: M = L; Arithmetic Operations, C_n = 1, C_n = 1 = H
L L L L	$F = \overline{A}$	F = A MINUS 1	F = A
L L L H	$F = \overline{AB}$	F = AB MINUS 1	F = $A\overline{B}$
L L H L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L L H H	$F = 1$	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	$F = \overline{A + B}$	F = A PLUS $(A + \overline{B})$	F = A PLUS $(A + \overline{B})$ PLUS 1
L H L H	$F = \overline{B}$	F = AB PLUS $(A + \overline{B})$	F = AB PLUS $(A + \overline{B})$ PLUS 1
L H H L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = MINUS B
L H H H	$F = A + \overline{B}$	F = $A + \overline{B}$	F = $(A + \overline{B})$ PLUS 1
H L L L	$F = A\overline{B}$	F = A PLUS $(A + B)$	F = A PLUS $(A + B)$ PLUS 1
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = $A\overline{B}$ PLUS $(A + B)$	F = $A\overline{B}$ PLUS $(A + B)$ PLUS 1
H L H H	F = A + B	F = $A + B$	F = $(A + B)$ PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	$F = A\overline{B}$	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H H H L	$F = AB$	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT54181 ..... −55°C to 125°C
ITT74181 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For this circuit, this rating applies to each A input conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

		ITT54181 Min	ITT54181 Nom	ITT54181 Max	ITT74181 Min	ITT74181 Nom	ITT74181 Max	Unit
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_{OH}	High-level output voltage any output except A = B	2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800 uA	
I_{OH}	High-level output current, A = B output only			250	uA	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA	
I_{IH}	High-level input current (mode input)			40	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (any A or B input)			120	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (any S input)			160	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (carry input)			200	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (any input)			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (mode input)			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (any A or B input)			−4.8	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (any S input)			−6.4	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (carry input)			−8	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−55	mA	V_{CC} = MAX	ITT54181
		−18		−57			ITT74181
I_{CC}	Supply current		88	127	mA	V_{CC} = MAX	ITT54181
			88	140			ITT74181
I_{CC}	Supply current		94	135	mA	V_{CC} = MAX	ITT54181
			94	150			ITT74181

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

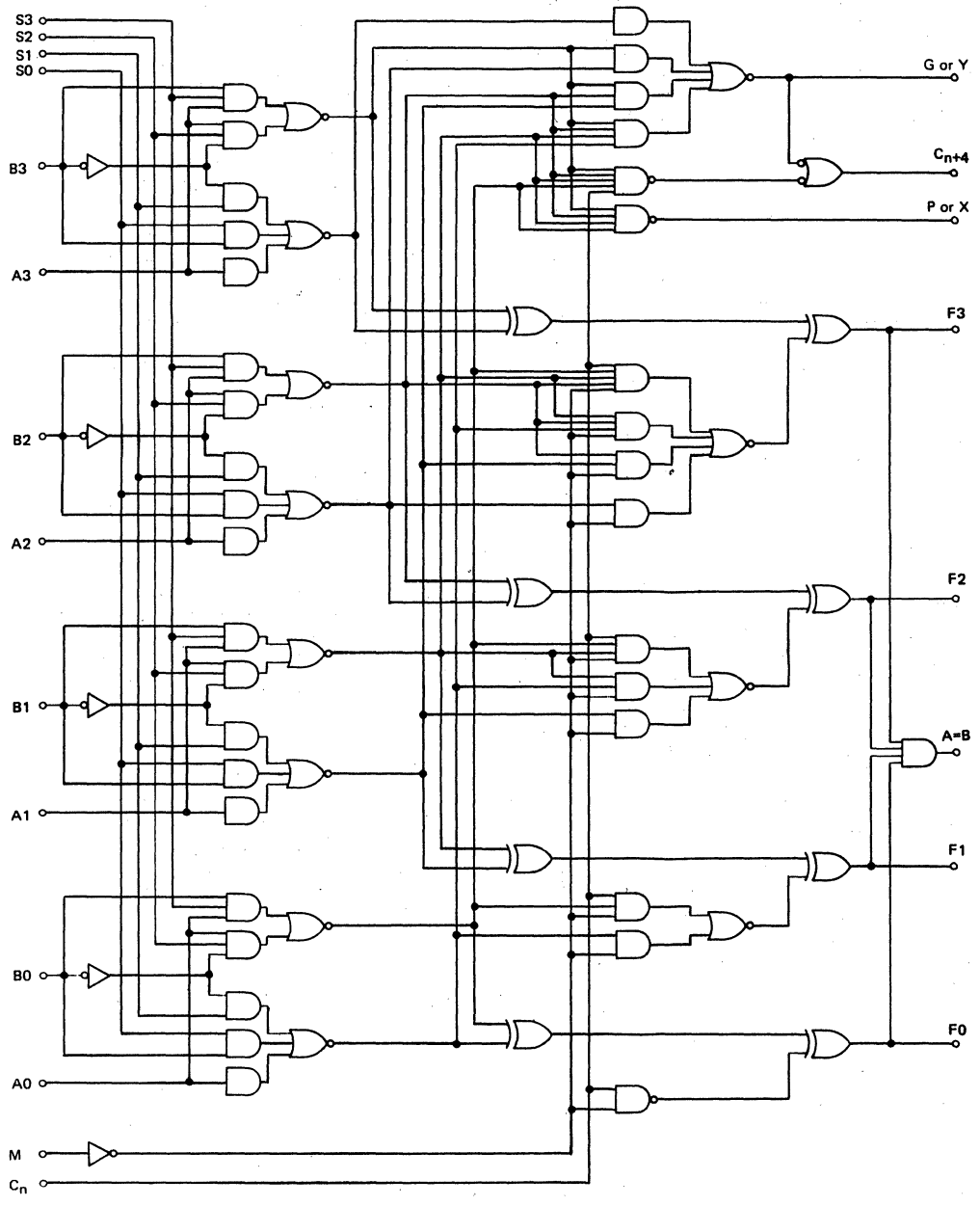
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400Ω)

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Test Conditions
t_{PLH}	C_n	C_{n+4}		12	18	ns	
t_{PHL}				13	19		
t_{PLH}	C_n	Any F		13	19	ns	M = 0V (SUM or DIFF model)
t_{PHL}				12	18		
t_{PLH}	Any A or B	G		13	19	ns	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM model)
t_{PHL}				13	19		
t_{PLH}	Any A or B	G		17	25	ns	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF model)
t_{PHL}				17	25		
t_{PLH}	Any A or B	P		13	19	ns	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM model)
t_{PHL}				17	25		
t_{PLH}	Any A or B	P		17	25	ns	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF model)
t_{PHL}				17	25		
t_{PLH}	Any A or B	Any F		28	42	ns	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM model)
t_{PHL}				21	32		
t_{PLH}	Any A or B	Any F		32	48	ns	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF model)
t_{PHL}				23	34		
t_{PLH}	Any A or B	Any F		32	48	ns	M = 4.5V (logic model)
t_{PHL}				23	34		
t_{PLH}	Any A or B	A = B		35	50	ns	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF model)
t_{PHL}				32	48		

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

functional block diagram



MSI LOOK-AHEAD CARRY GENERATOR

The ITT54182, ITT74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanosecond delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

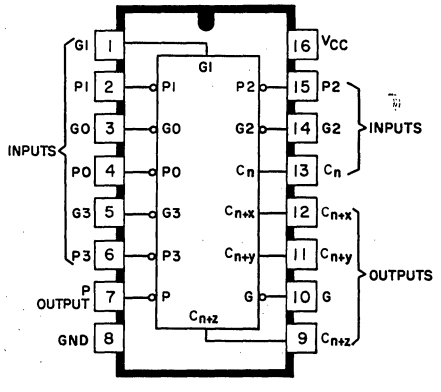
The ITT54182 or ITT74182, when used in conjunction with the ITT54181 or ITT74181 arithmetic logic unit (ALU) provides full high-speed carry look-ahead capability for up to n-bit words. Each ITT-54182/ITT74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

Carry inputs and outputs of the ITT-54181/ITT74181 are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms. Reinterpretations of carry functions at the ITT54181/ITT74181 are also applicable and compatible with the look-ahead package. Logic equations are:

$$C_{n+x} = G_0 + P_0 C_n$$
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$
$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$
$$\overline{G} = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$
$$P = \overline{P_3 P_2 P_1 P_0}$$

Inputs of the ITT54182/ITT74182 are diode-clamped to minimize transmission-line effects, and Darlington outputs are employed to improve turn-off times and reduce propagation delay times. Typically, the average carry time is 13 nanoseconds, and power dissipation is typically 180 milliwatts or 11 milliwatts per gate. The ITT54182 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74182 is characterized for operation from 0°C to 70°C.

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



LOGIC: SEE DESCRIPTION

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Interemitter voltage (see Note 2) 5.5V
Operating free-air temperature range:
ITT54182 ..... −55°C to 125°C
ITT74182 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each G input in conjunction with any other G input or in conjunction with any P input.

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

recommended operating conditions

		ITT54182			ITT74182			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_R	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −12 mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800 uA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current (C_n input)			80	uA	V_{CC} = MAX, V_I = 2.4V
I_{IH}	High-level input current (P3 input)			120	uA	V_{CC} = MAX, V_I = 2.4V
I_{IH}	High-level input current (P2 input)			160	uA	V_{CC} = MAX, V_I = 2.4V

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted) **(continued)**

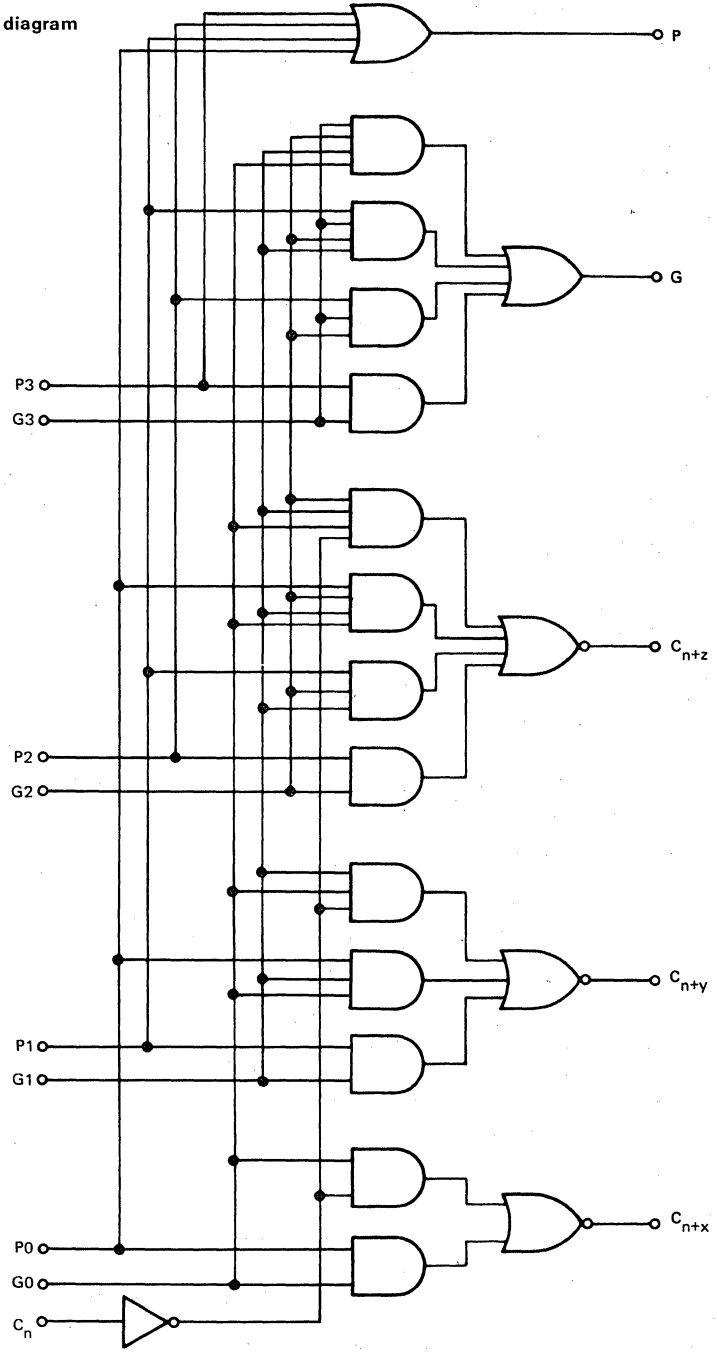
	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
I_{IH}	High-level input current (P0, P1, or G3 input)			200	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (G0 or G2 input)			360	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (G1 input)			400	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IH}	High-level input current (any input)			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current (C_n input)			−3.2	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (P3 input)			−4.8	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (P2 input)			−6.4	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (P0, P1, or G3 input)			−8	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (G0 or G2 input)			−14.4	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current (G1 input)			−16	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX	
I_{CCH}	Supply current, all outputs high		27		mA	V_{CC} = MAX	ITT54182
			27				ITT74182
I_{CCL}	Supply current, all outputs low		45	65	mA	V_{CC} = MAX	ITT54182
			45	72			ITT74182

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
t_{PLH}	Propagation delay time, low-to-high-level output		11	17	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output		15	22	ns	C_L = 15 pF, R_L = 400Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed 1 second.

functional block diagram

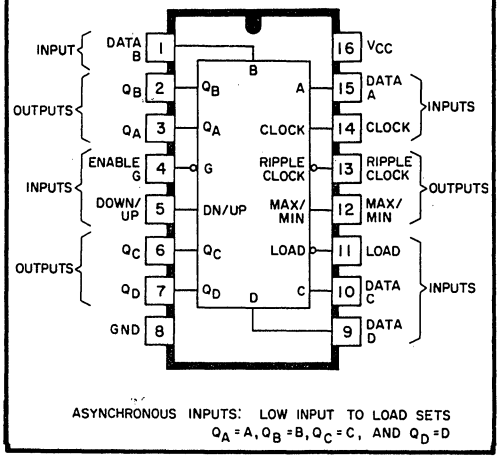


ITT SEMICONDUCTORS

SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

- **Counts 8-4-2-1 BCD or Binary**
- **Single Down/Up Count Control Line**
- **Count Enable Control Input**
- **Ripple Clock Output for Cascading**
- **Asynchronously Presettable with Load Control**
- **Parallel Outputs**
- **Cascadable for n-Bit Applications**
- **Typical Average Propagation Delay (Clock to Q Output)...20 ns**
- **Typical Power Dissipation...325 mW**
- **Typical Maximum Clock Frequency...25 Mhz**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



ASYNCHRONOUS INPUTS: LOW INPUT TO LOAD SETS $Q_A = A, Q_B = B, Q_C = C$, AND $Q_D = D$

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

The ITT54190, ITT54191, ITT74190, and ITT-74191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The ITT54191 and ITT74191 are 4-bit binary counters and the ITT54190 and ITT74190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Input buffers have been used to lower the fan-in requirement to only one normalized Series 54/74 load at all inputs except enable. This is important when the output of the driving circuitry is somewhat limited.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.

The ITT54190 and ITT54191 are characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74190 and ITT74191 are characterized for operation from 0°C to 70°C.

ITT54190, ITT74190 DECADE COUNTERS

typical load, count, and inhibit sequences

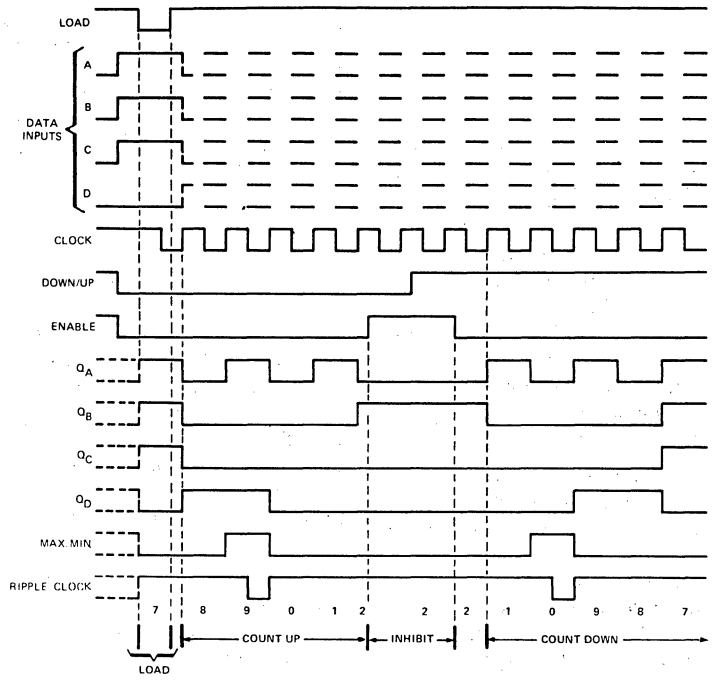
Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Operating free-air temperature range:
ITT54190, ITT54191 ..... −55°C to 125°C
ITT74190, ITT74191 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1: Voltage values are with respect to network ground terminal.



recommended operating conditions

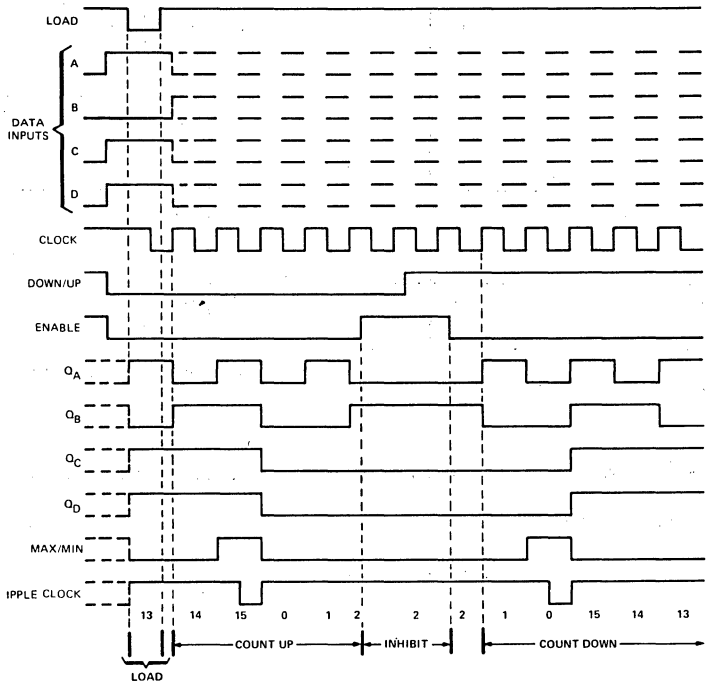
		ITT54190, ITT54191			ITT74190, ITT74191			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)		20			20			ns
Data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

ITT54191, ITT74191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Parameter		ITT54190, ITT54191 Min	Typ [1]	Max	ITT74190, ITT74191 Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			2			V	V_{CC} = MIN
V_{IL}	Low-level input voltage			0.8			0.8	V	V_{CC} = MIN
V_I	Input clamp voltage			−1.5			−1.5	V	V_{CC} = MIN, I_I = −12mA
V_{OH}	High-level output voltage	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA
V_{OL}	Low-level output voltage			0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA
I_I	High-level input current at maximum input voltage			1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current at any input except enable			40			40	uA	V_{CC} = MAX, V_I = 2.4V
I_{IH}	High-level input current at enable input			120			120	uA	V_{CC} = MAX, V_I = 2.4V
I_{IL}	Low-level input current at any input except enable			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{IL}	Low-level input current at enable input			−4.8			−4.8	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−65	−18		−65	mA	V_{CC} = MAX
I_{CC}	Supply current		65	105		65	105	mA	V_{CC} = MAX, See Note 2

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

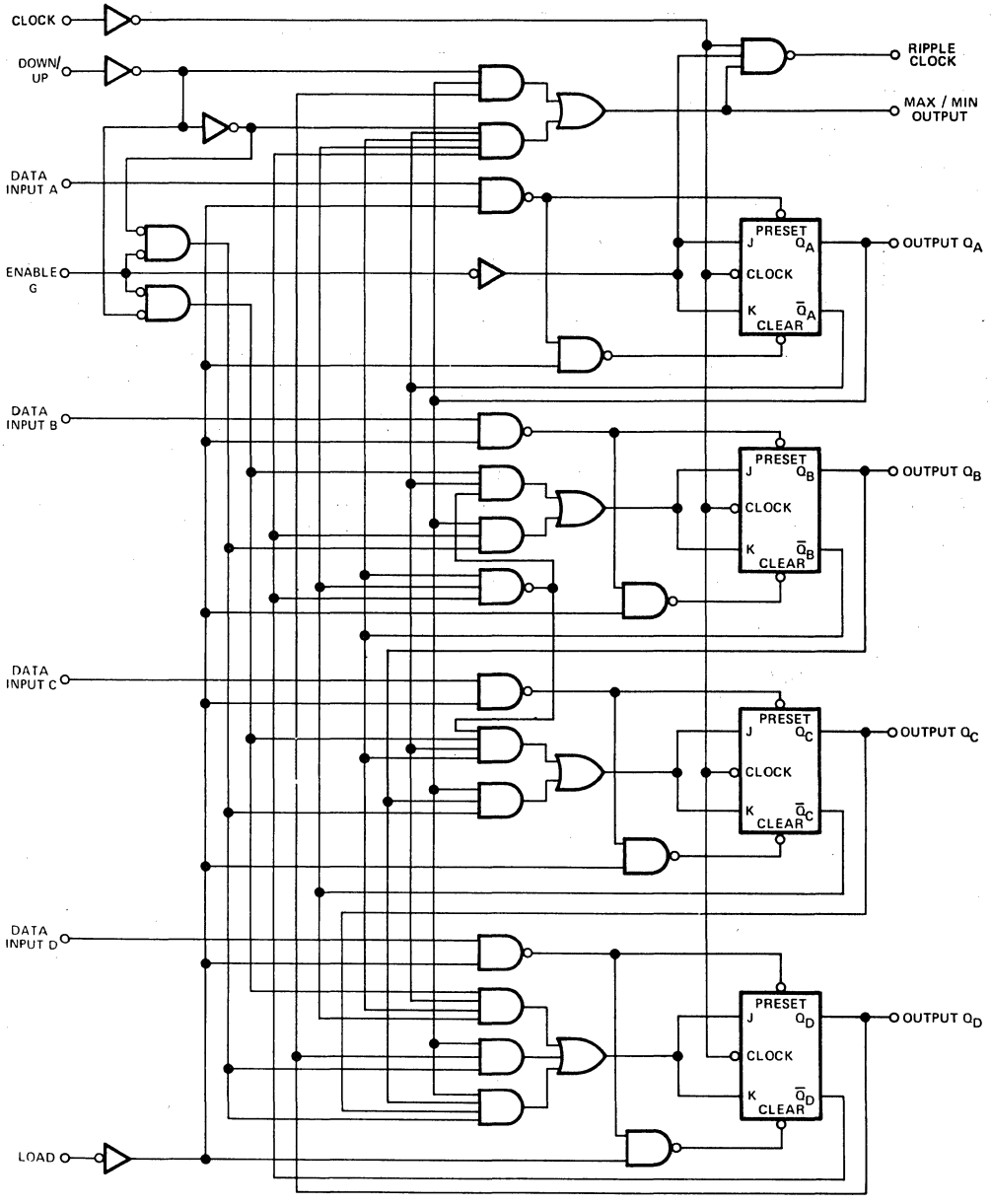
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter [1]	From (Input)	To (Output)	Min	Typ	Max	Unit	Test Conditions
t_{max}			20	25		MHz	C_L = 15 pF, R_L = 400Ω
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D		22	33	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				33	50		
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D		14	22	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				35	50		
t_{PLH}	Clock	Ripple Clock		13	20	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				16	24		
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D		16	24	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				24	36		
t_{PLH}	Clock	Max/Min		28	42	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				37	52		
t_{PLH}	Down/Up	Ripple Clock		30	45	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				30	45		
t_{PLH}	Down/Up	Max/Min		21	33	ns	C_L = 15 pF, R_L = 400Ω
t_{PHL}				22	33		

[1] t_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

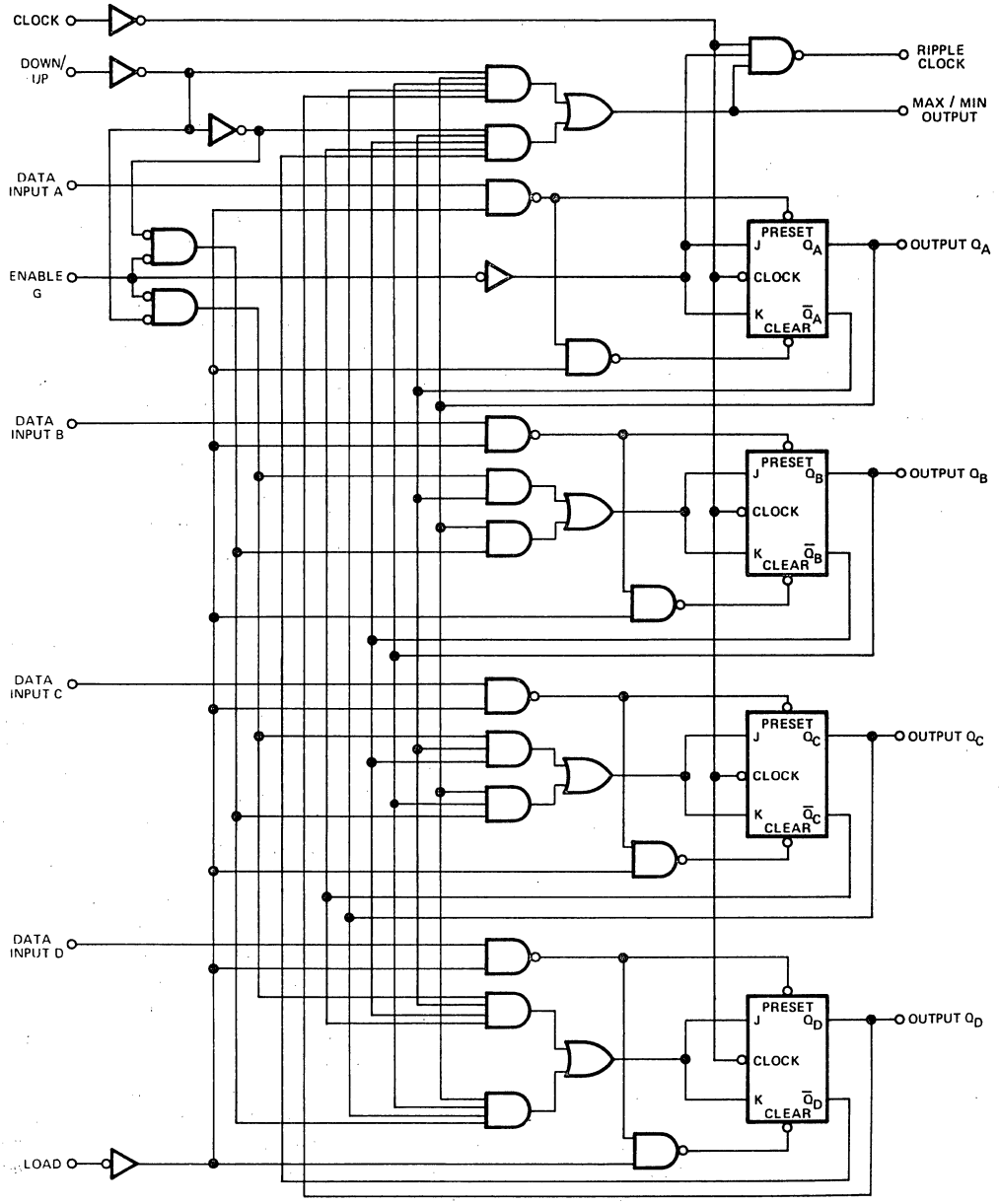
ITT54191, ITT74191 BINARY COUNTERS

functional block diagram



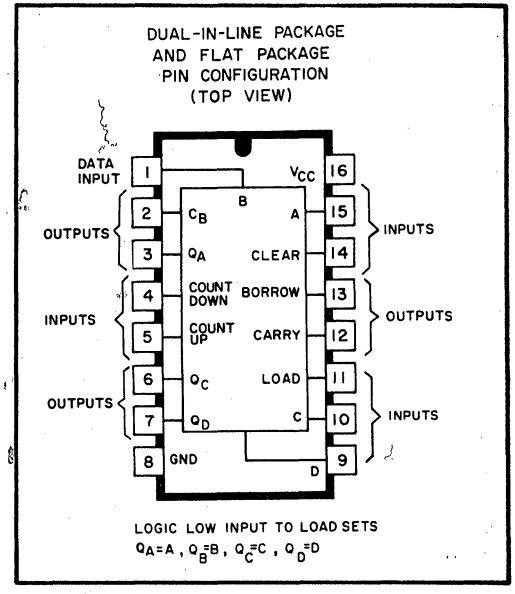
ITT54190, ITT74190 DECADE COUNTERS

functional block diagram



SYNCHRONOUS 4-BIT UP-DOWN COUNTER (dual clock with clear)

- Cascading Circuitry Provided Internally
- Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges.
- High capacitive drive capability.
- Individual Preset to Each Flip Flop.
- Typical power dissipation of 325 mW
- The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families.
- Input clamp diodes limit high speed line termination effects
- Fully Independent Clear Input
- Typical Maximum Input Count Frequency....32 MHz



The MSI ITT54/74192 is a synchronous up/down decade counter with separate up/down clocks, parallel load (asynchronous) facility, two terminal count outputs for multi-decade operation, and an asynchronous overriding master reset.

The MSI ITT54/74193 is a synchronous up/down 4-bit binary counter with separate up/down clocks, parallel load (asynchronous) facility, terminal count outputs for multi-decade operations, and an asynchronous overriding master reset.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CP_U) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are pulsed simultaneously.) The counter will respond to a clock pulse on either input by changing to the next appropriate state of a binary sequence.

The counter has a parallel load (asynchronous) facility which permits the counter to be reset. Whenever the data enable (PL) input is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the data enable input goes low, this information is stored in the counter and when the counter is clocked it changes to the next appropriate state in the counts sequence. The data inputs are inhibited when the data enable is high and have no effect on the counter.

The terminal count-up (TC_U) and terminal count-down (TC_D) outputs (Carry and Borrow respectively) allow multistage binary counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and the terminal count-down output to the count-down input of the following counter.

absolute maximum ratings (above which the useful life may be impaired)

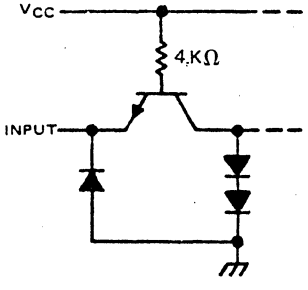
Storage Temperature ..... −65°C to +150°C
Temperature (Ambient)
Under Bias ..... −55°C to +125°C
V_{CC} Pin Potential to Ground Pin −0.5V to +7 Volts
Voltage Applied to Outputs
for high output state ..... −0.5V to V_{CC} value
Input Voltage (D.C.) ..... −0.5V to +5.5 Volts

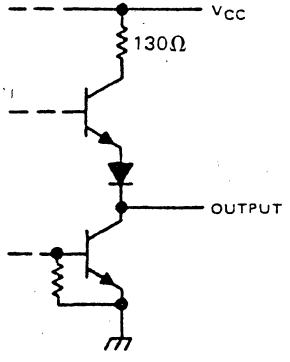
recommended operating conditions

	ITT54192, ITT54193			ITT74192, ITT74193			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_W	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

Notes: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

schematics of inputs and outputs





ELECTRICAL CHARACTERISTICS, over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Characteristics	ITT54192, ITT54193			ITT74192, ITT74193			Unit	Conditions [2]
		Min	Typ [1]	Max	Min	Typ [1]	Max		
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.8			0.8	V	
V_{OH}	High-level output voltage	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = 400 uA
V_{OL}	Low-level output voltage			0.4			0.4	V	V_{CC} = MIN, V_{OH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA
I_{IH}	High-level input current			40			40	uA	V_{CC} = MAX, V_I = 2.4V
				1			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IL}	Low-level input current			−1.6			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current [3]	−20		−65	−18		−65	mA	V_{CC} = MAX
65_{CC}	Supply current		65	89			102	mA	V_{CC} = MAX

[1] All typical values are at V_{CC} = 5V, T_A = 25°C
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

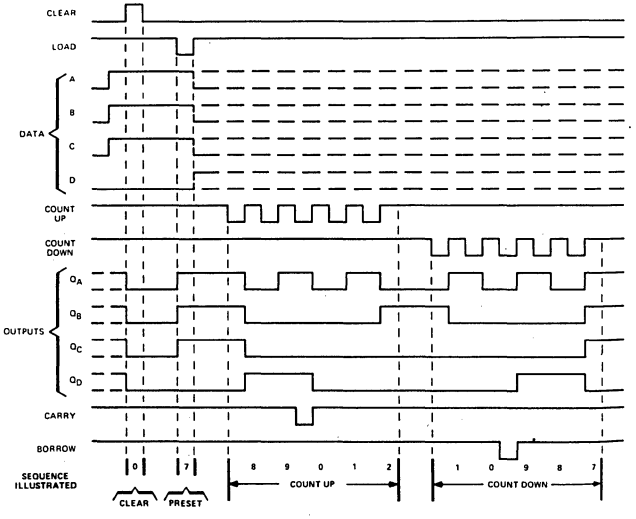
Parameter [1]	From Input	To Output	Min	Typ	Max	Units	Conditions
f_{max}			25	32		MHz	C_L = 15 pF, R_L = 400 Ω
t_{setup}				14	20	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH} t_{PHL}	Count-up	Carry		17 16	26 24	ns	C_L = 15, pF, R_L = 400 Ω
t_{PLH} t_{PHL}	Count-down	Borrow		16 16	24 24	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH} t_{PHL}	Either Count	Q		25 31	38 47	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH} t_{PLH}	Load	Q		27 29	40 40	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Clear	Q		22	35	ns	C_L = 15 pF, R_L = 400 Ω

[1] f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

ITT54/74192 DECADE COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

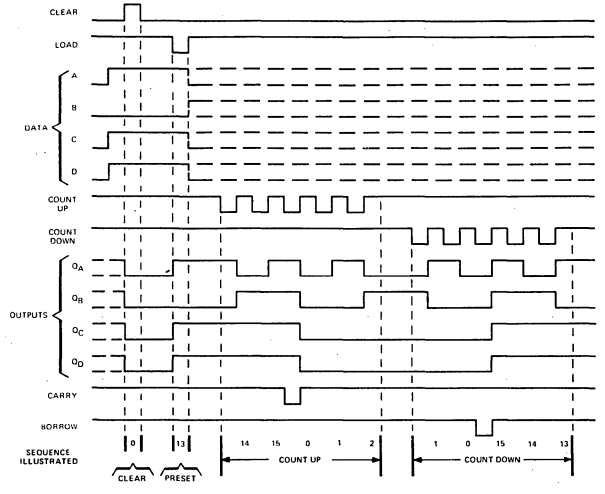
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



ITT54/74193 BINARY COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

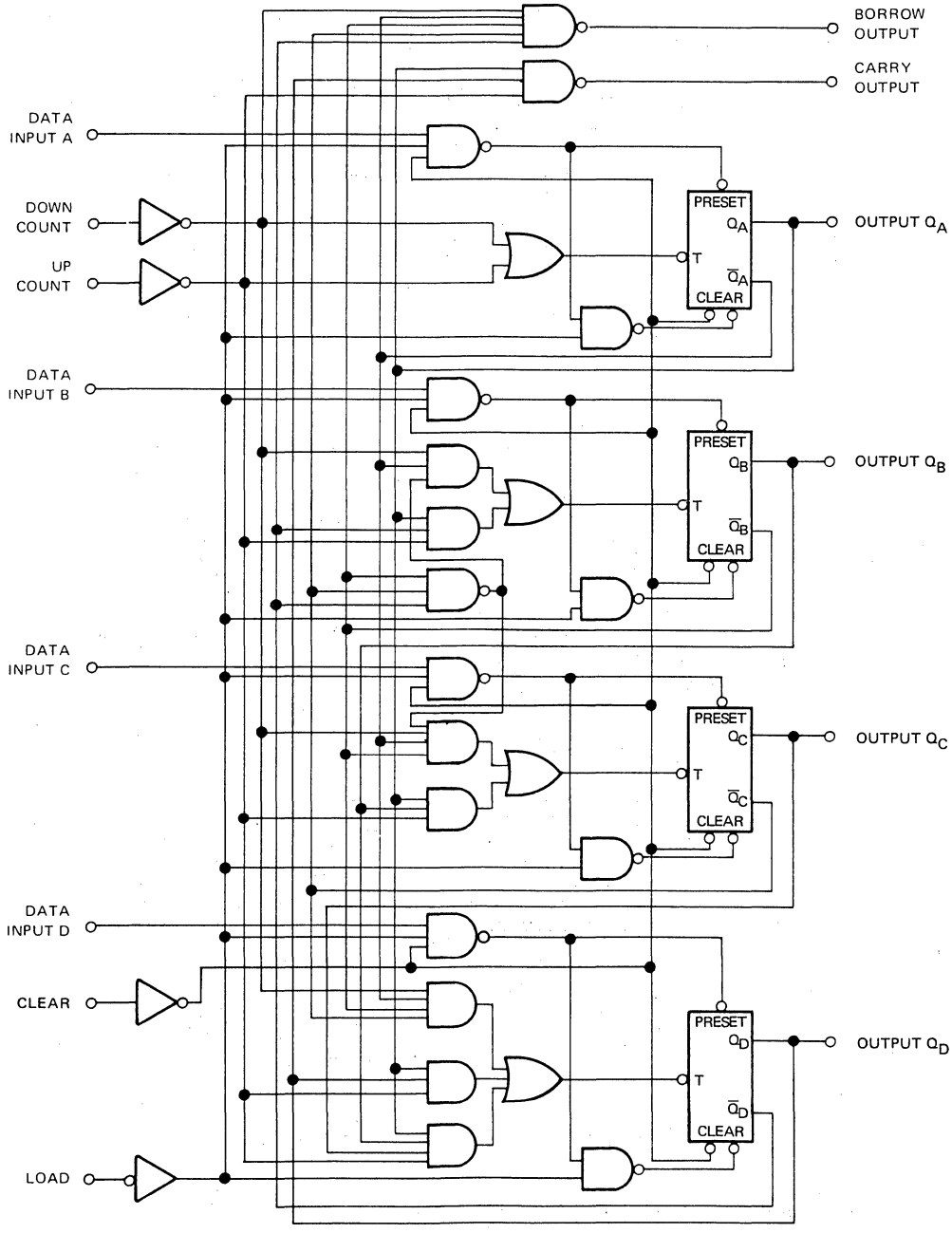
1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



Notes: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high. When counting down, count-up input must be high.

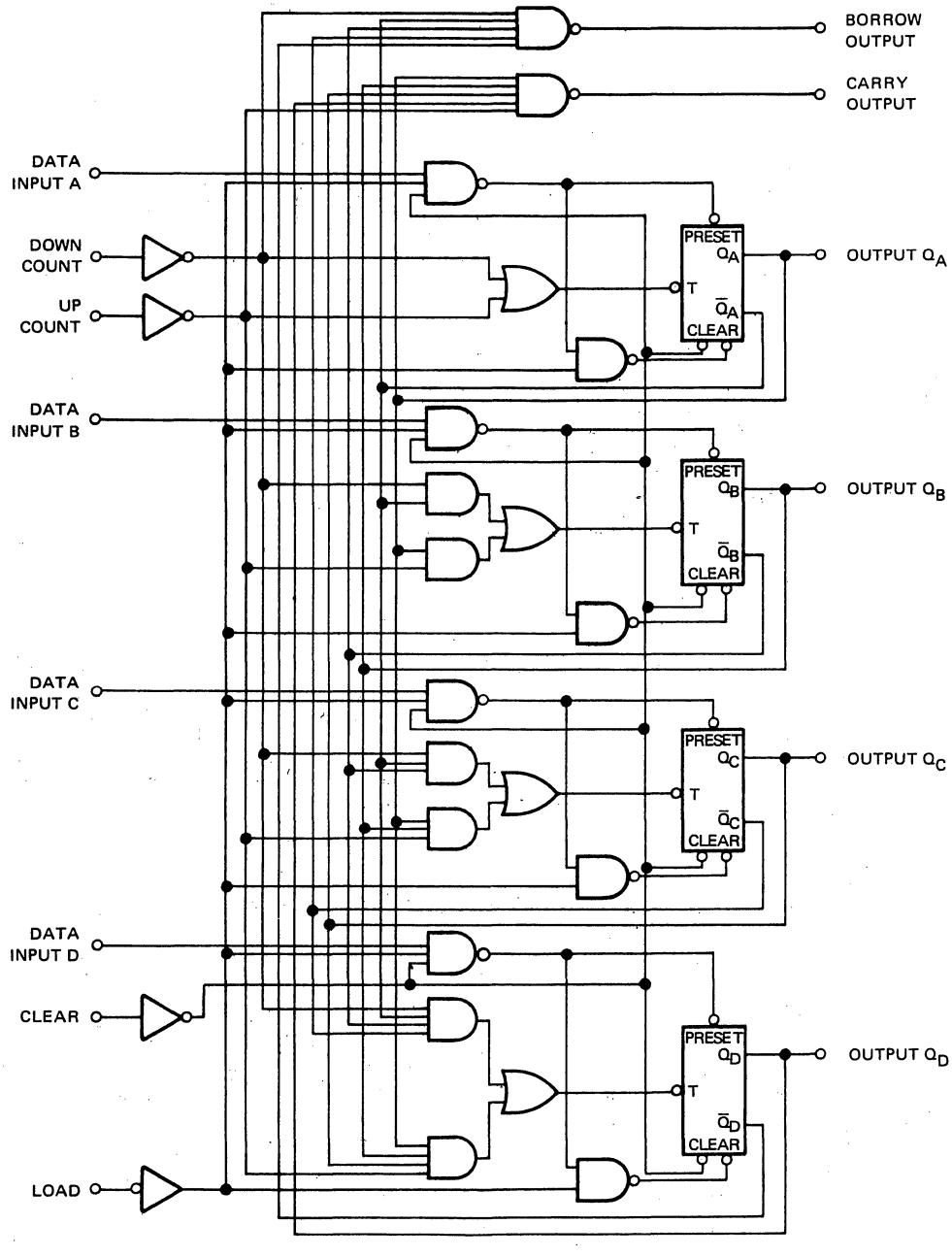
ITT54/74192 DECADE COUNTERS

FUNCTIONAL BLOCK DIAGRAM



ITT54/74193 BINARY COUNTERS

FUNCTIONAL BLOCK DIAGRAM



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

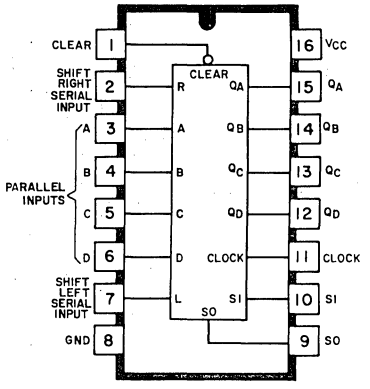
- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  - **Synchronous Parallel Load**
  - **Left Shift**
  - **Right Shift**
  - **Do Nothing**
- **Positive Edge-Triggered Clocking**
- **Direct Overriding Clear**

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear-line. The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	**S0**
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Do nothing)	L	L

In the parallel load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE DESCRIPTION

† Pin assignments for these circuits are the same for all packages.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195 mW.

The ITT54194 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74194 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) 7V
Input voltage (see Note 1) 5.5V

Operating free-air temperature range
ITT54194 ..... −55°C to 125°C
ITT74194 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		ITT54194			ITT74194			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup} (See Figure 1)	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_i = −12mA
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800 uA
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA
I_i	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted) **(continued)**

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V
I_{OS}	Short-circuit output current[3]	−20		−57	mA	V_{CC} = MAX ITT54194
		−18		−57		
I_{CC}	Supply current		39	63	mA	V_{CC} = MAX, See Note 2

Note: 2. With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V, applied to clock.

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

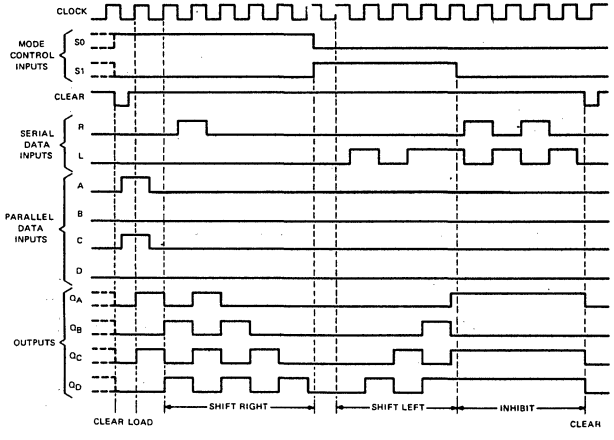
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

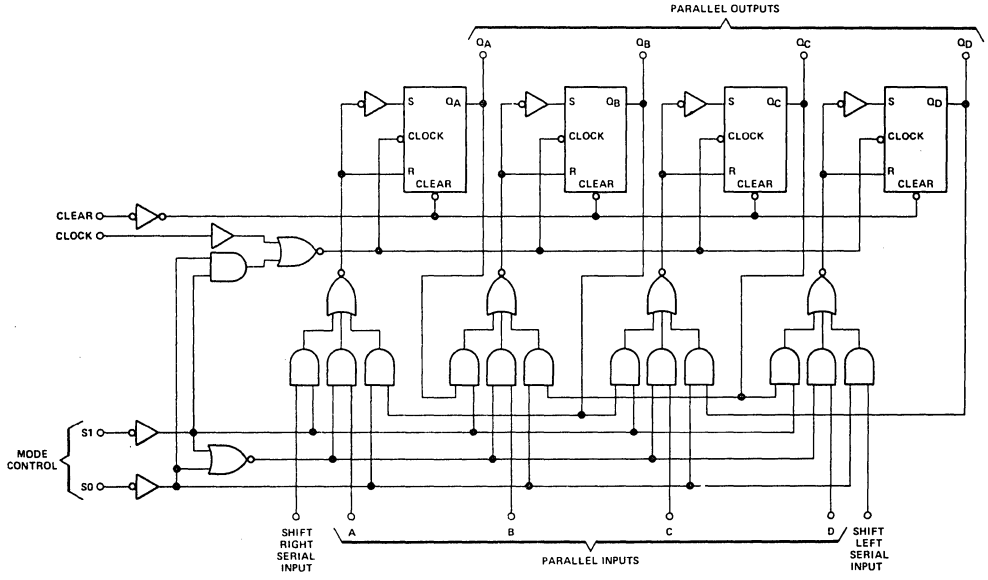
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum input clock frequency	25	36		MHz	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Propagation delay time high-to-low-level output from clear		19	30	ns	C_L = 15 pF, R_L = 400 Ω
t_{PLH}	Propagation delay time low-to-high-level output from clock	7	14	22	ns	C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Propagation delay time high-to-low-level output from clock	7	17	28	ns	C_L = 15 pF, R_L = 400 Ω

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



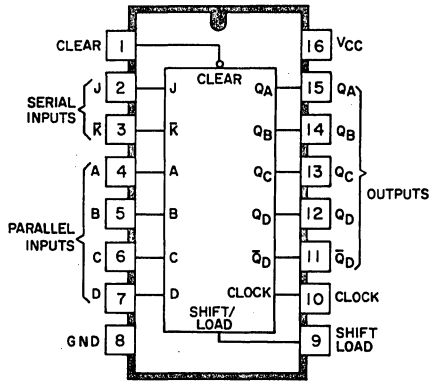
functional block diagram



4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- **Synchronous Parallel Load**
- **Positive Edge-Triggered Clocking**
- **Parallel Inputs and Outputs from Each Flip-Flop**
- **Direct Overriding Clear**
- **J and $\overline{K}$ Inputs to First Stage**
- **Complementary Outputs from Last Stage**

DUAL-IN-LINE PACKAGE
AND FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)†



POSITIVE LOGIC: SEE DESCRIPTION

† Pin assignments for these circuits are the same for all packages.

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The ITT54195 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74195 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level

Notes: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) 5.5V
Operating free-air temperature range:
ITT54195 Circuits ..... −55°C to 125°C
ITT74195 Circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		ITT54195			ITT74195			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			
	Serial and parallel data	15			15			ns
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$				10			10	ns
Serial and parallel data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_I	Input clamp voltage			−1.5	V	V_{CC} = MIN, I_I = −12mA	
V_{OH}	High-level output voltage	2.4			V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800uA	
V_{OL}	Low-level output voltage			0.4	V	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	
I_I	Input current at maximum input voltage			1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current			40	uA	V_{CC} = MAX, V_I = 2.4V	
I_{IL}	Low-level input current			−1.6	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−20		−57	mA	V_{CC} = MAX	ITT54195
		−18		−57			ITT74195
I_{CC}	Supply current		39	63	mA	V_{CC} = MAX, See Note 2	

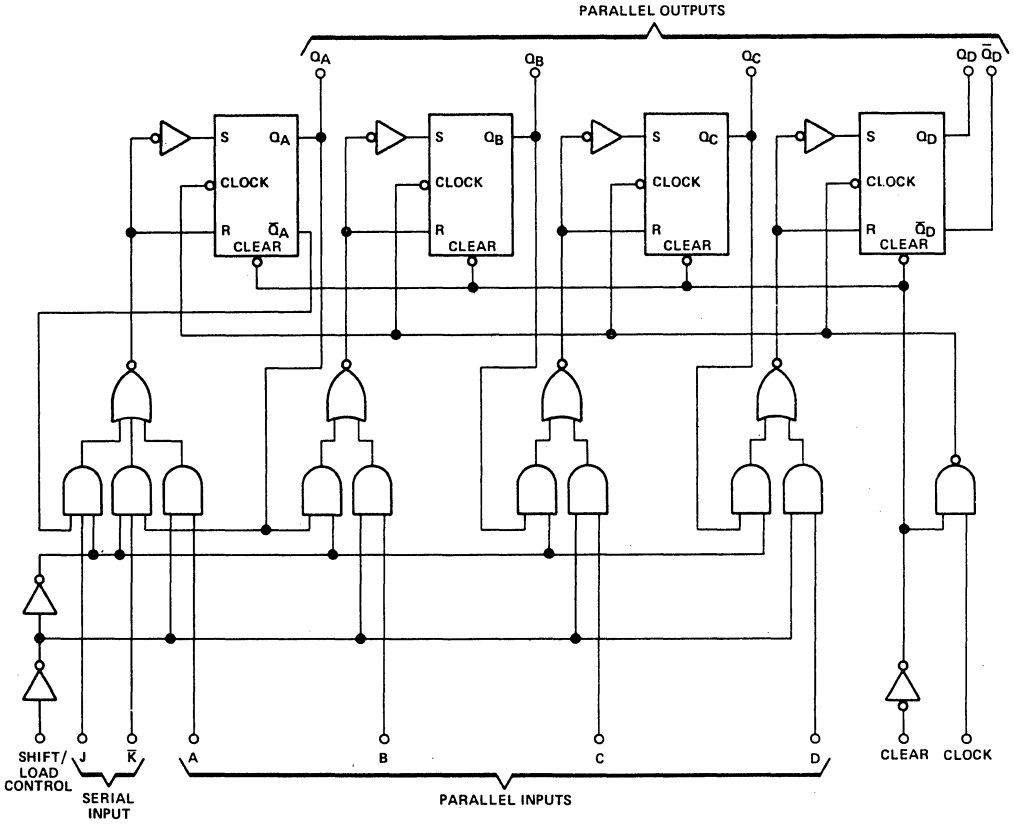
Note: 2. With all outputs open, shift/load grounded, and 4.5V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time.

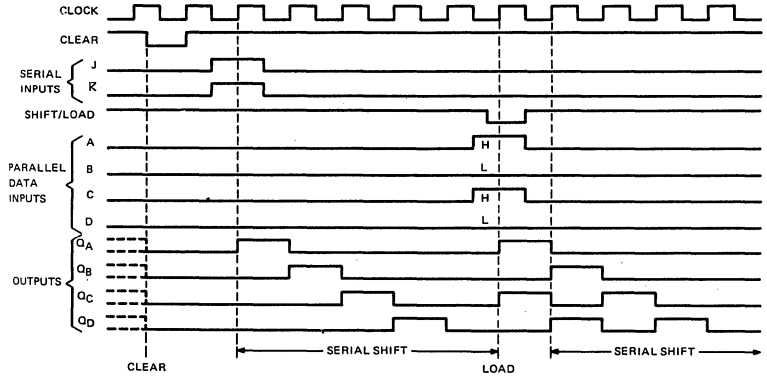
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{max}	Maximum input clock frequency	30	39		MHz	C_L = 15pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output from clear		19	30	ns	C_L = 15pF, R_L = 400Ω
t_{PLH}	Propagation delay time, low-to-high-level output from clock	6	14	22	ns	C_L = 15pF, R_L = 400Ω
t_{PHL}	Propagation delay time, high-to-low-level output from clock	7	17	26	ns	C_L = 15pF, R_L = 400Ω

functional block diagram

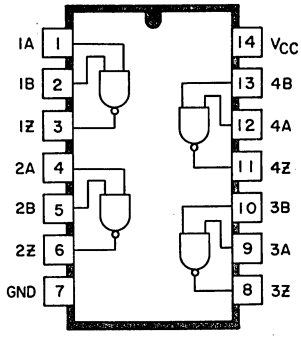


typical clear, shift, and load sequences



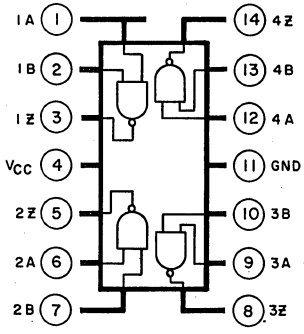
QUADRUPLE 2-INPUT POSITIVE NAND GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



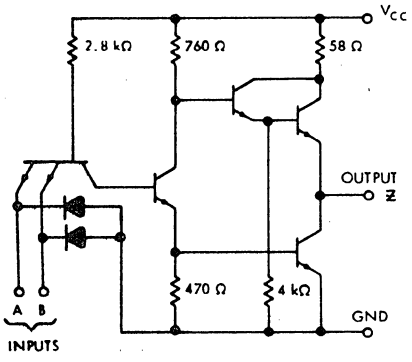
POSITIVE LOGIC $\overline{Z} = \overline{AB}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{AB}$

schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	54H00 Circuits	4.5	5	5.5	V
	74H00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	54H00 Circuits	−55	25	125	°C
	74H00 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{IN} I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		26	40	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		10	16.8	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.2	10	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		5.9	10	ns	C_L = 25 pF, R_L = 280 Ω

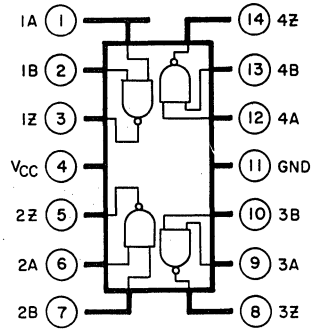
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

ITT SEMICONDUCTORS

QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

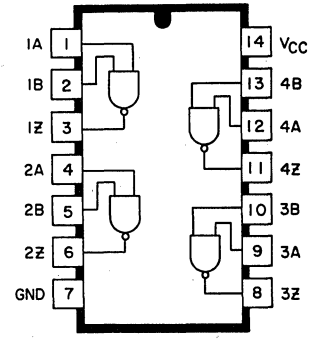
QUADRUPLE 2-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



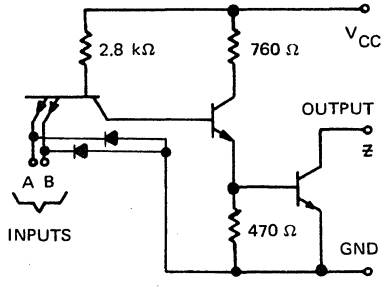
POSITIVE LOGIC $\bar{Z} = \overline{AB}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\bar{Z} = \overline{AB}$

schematic (each gate)



NOTE: Component values shown are nominal.

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H01 Circuits	4.5	5	5.5	V
74H01 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range: 54H01 Circuits	−55	25	125	°C
74H01 Circuits	0	25	70	°C

CIRCUIT TYPES ITT54H01, ITT74H01
QUADRUPLE 2-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min, I_i = −8 mA
$I_{out(1)}$	Output reverse current			250	uA	V_{CC} = MIN, V_{in} = 0.8V, $V_{out(1)}$ = 5.5V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{CC(0)}$	Logical 0 level supply current		26	40	mA	V_{CC} = MAX, V_{in} = 4.5V
$I_{CC(1)}$	Logical 1 level supply current		6.8	10	mA	V_{CC} = MAX, V_{in} = 0

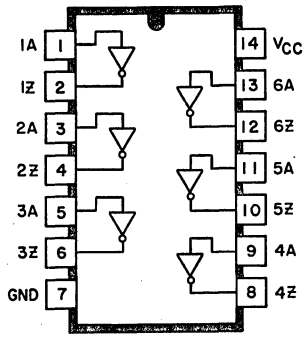
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7.5	12	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		10	15	ns	C_L = 25 pF, R_L = 280 Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

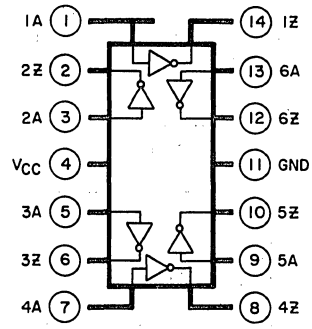
HEX INVERTERS

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



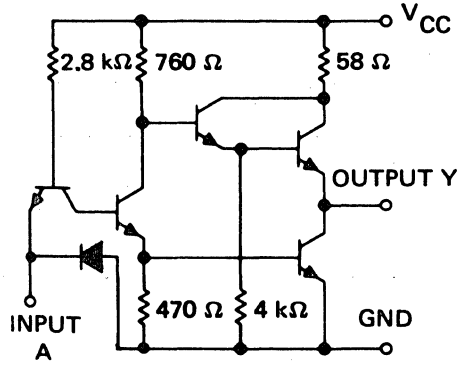
POSITIVE LOGIC: $Z = \overline{A}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{A}$

schematic (each inverter)



Component values shown are normal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	54H04 Circuits	4.5	5	5.5	V
	74H04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	54H04 Circuits	−55	25	125	°C
	74H04 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		10	58	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		16	26	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.5	10	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		6	10	ns	C_L = 25 pF, R_L = 280 Ω

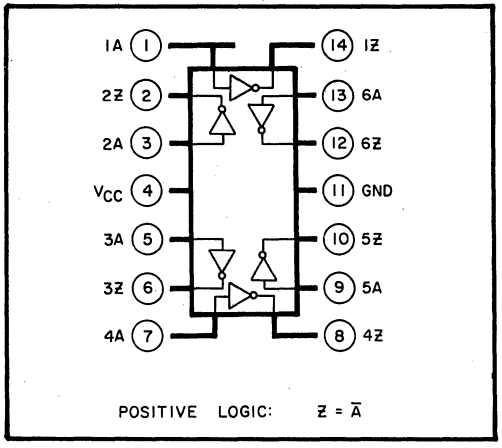
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

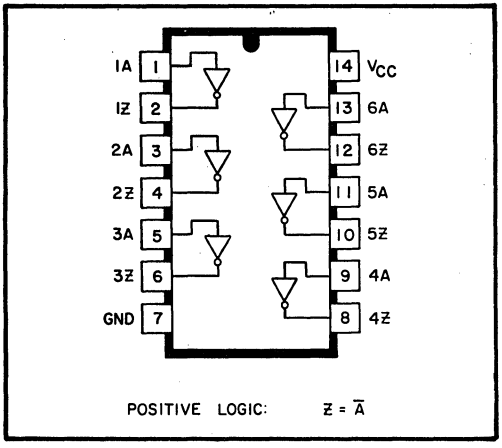
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

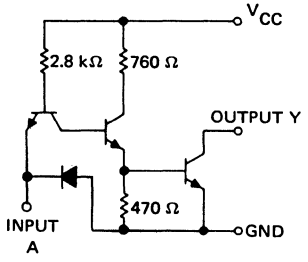
FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic (each inverter)



NOTE: Component values shown are normal.

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H05 Circuits	4.5	5	5.5	V
74H05 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N	−55	25	125	°C
Operating Free-Air Temperature Range, T_A: 54H05 Circuits	0	25	70	°C
74H05 Circuits			10	

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −8 mA
$I_{out(1)}$	Output reverse current			250	uA	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V
$V_{out(0)}$	Logical 0 output voltage (on level)			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{CC(0)}$	Logical 0 level supply current		40	58	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		16	26	mA	V_{CC} = MAX, V_{in} = 0

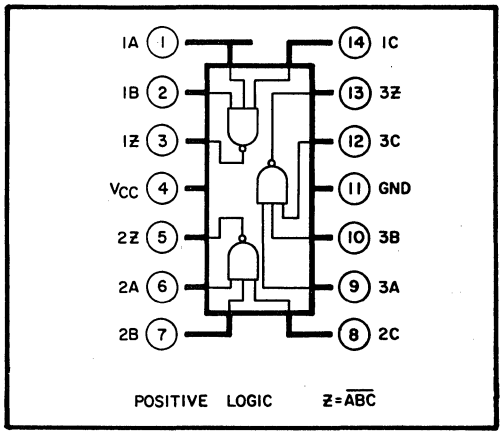
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7.5	12	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		10	15	ns	C_L = 25 pF, R_L = 280 Ω

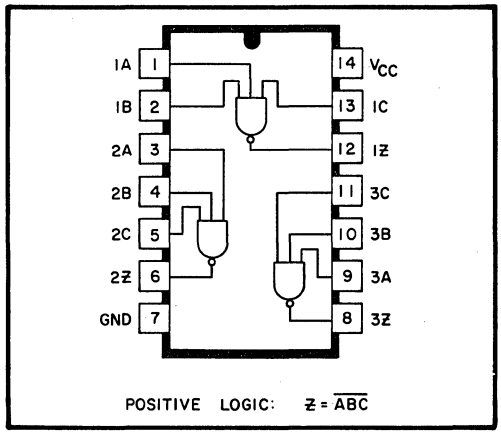
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

TRIPLE 3-INPUT POSITIVE NAND GATES

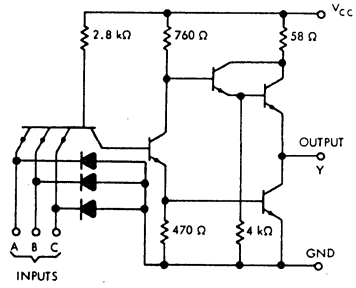
FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H10 Circuits	4.5	5	5.5	V
74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: 54H10 Circuits	−55	25	125	°C
74H10 Circuits	0	25	70	°C

CIRCUIT TYPES ITT54H10, ITT74H10

TRIPLE 3-INPUT POSITIVE NAND GATES

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		19.5	30	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		7.5	12.4	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.3	10	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		5.9	10	ns	C_L = 25 pF, R_L = 280 Ω

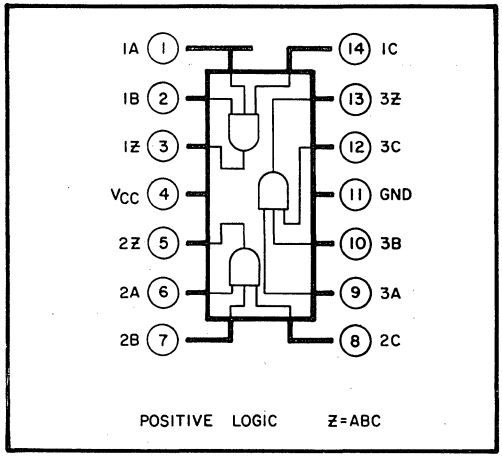
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

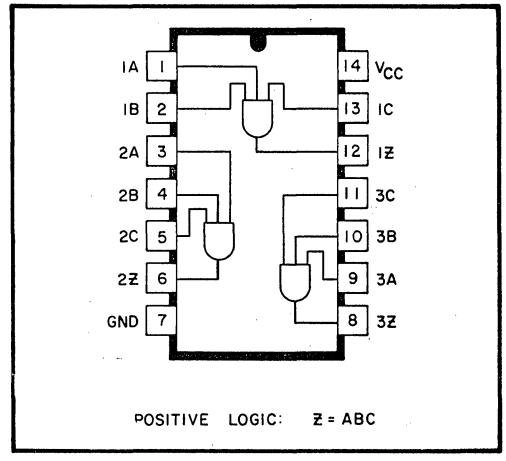
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

TRIPLE 3-INPUT POSITIVE AND GATES

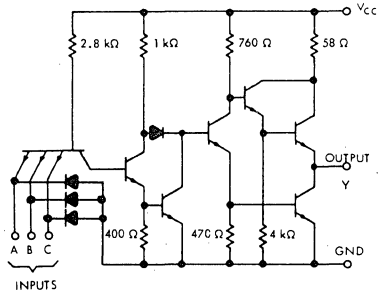
FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions		Min	Nom	Max	Unit
Supply Voltage V_{CC}:	54H11 Circuits	4.5	5	5.5	V
	74H11 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	54H11 Circuits	−55	25	125	°C
	74H11 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 2 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 0.8 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(0)}$	Logical 0 level supply current		30	48	mA	V_{CC} = MAX, V_{in} = 0
$I_{CC(1)}$	Logical 1 level supply current		18	30	mA	V_{CC} = MAX, V_{in} = 4.5 V

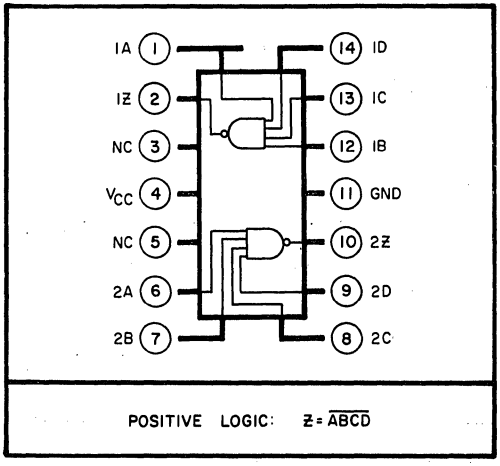
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8.8	12	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		7.6	12	ns	C_L = 25 pF, R_L = 280 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

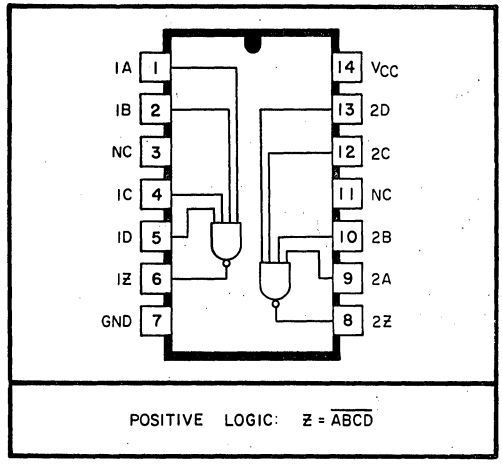
DUAL 4-INPUT POSITIVE NAND GATES

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



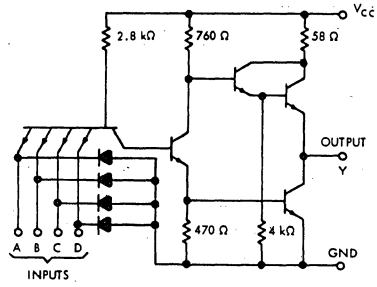
POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

schematic (each gate)



NOTES: 1. Component values shown are nominal.
2. NC—No internal connection.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H20 Circuits	4.5	5	5.5	V
74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: 54H20 Circuits	−55	25	125	°C
74H20 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 voltage output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		13	20	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		5	8.4	mA	V_{CC} = MAX, V_{in} = 0

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7	10	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		6	10	ns	C_L = 25 pF, R_L = 280 Ω

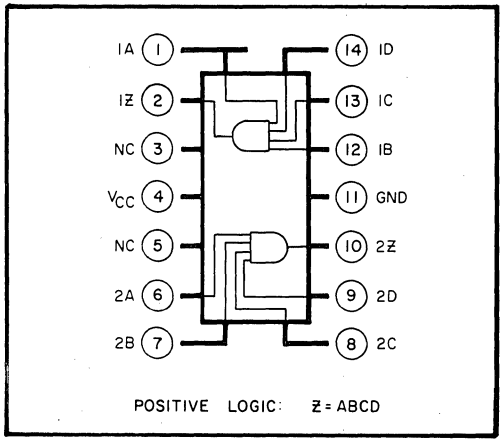
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

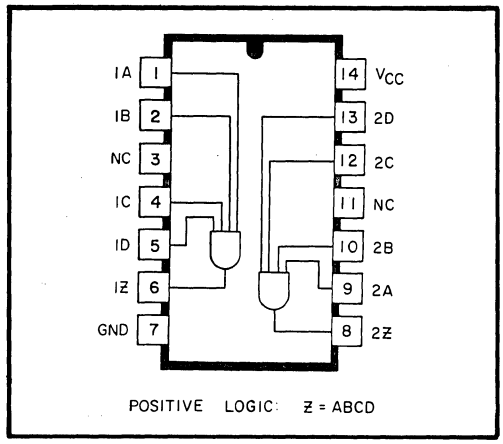
DUAL 4-INPUT POSITIVE AND GATES

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



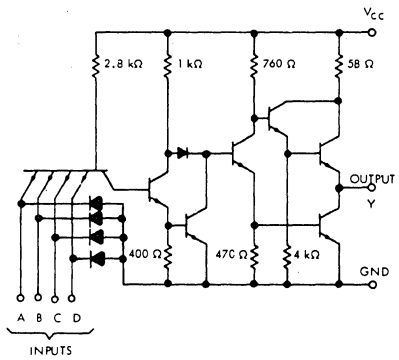
POSITIVE LOGIC: $\bar{Z} = ABCD$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\bar{Z} = ABCD$

schematic (each gate)



NOTE: Component values shown are nominal.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H21 Circuits	4.5	5	5.5	V
74H21 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, $\dot{N}$			10	
Operating Free-Air Temperature Range, T_A: 54H21 Circuits	−55	25	125	°C
74H21 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 2 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 0.8 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(0)}$	Logical 0 level supply current		20	32	mA	V_{CC} = MAX, V_{in} = 0
$I_{CC(1)}$	Logical 1 level supply current		12	20	mA	V_{CC} = MAX, V_{in} = 4.5 V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8.8	12	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		7.6	12	ns	C_L = 25 pF, R_L = 280 Ω

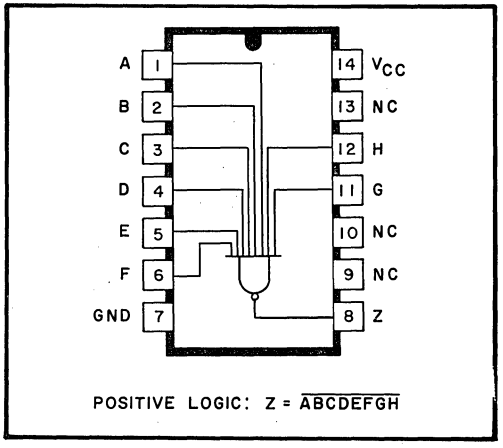
[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

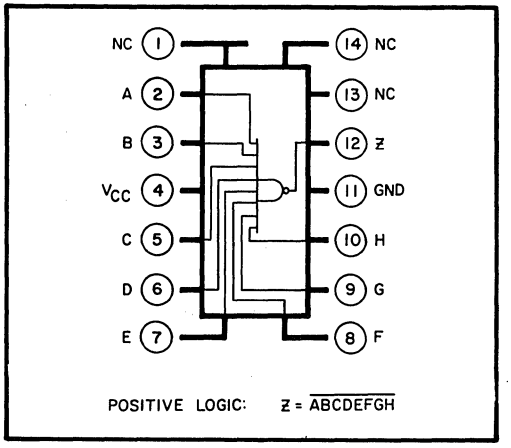
8-INPUT POSITIVE NAND GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



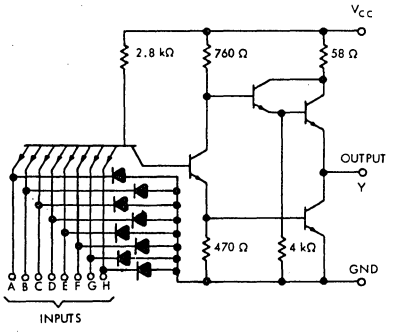
POSITIVE LOGIC: $Z = \overline{ABCDEFGH}$

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Z = \overline{ABCDEFGH}$

schematic



NOTES: 1. Component values shown are nominal.
2. NC—No internal connection.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H30 Circuits	4.5	5	5.5	V
74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: 54H30 Circuits	−55	25	125	°C
74H30 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		6.5	10	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		2.5	4.2	mA	V_{CC} = MAX, V_{in} = 0

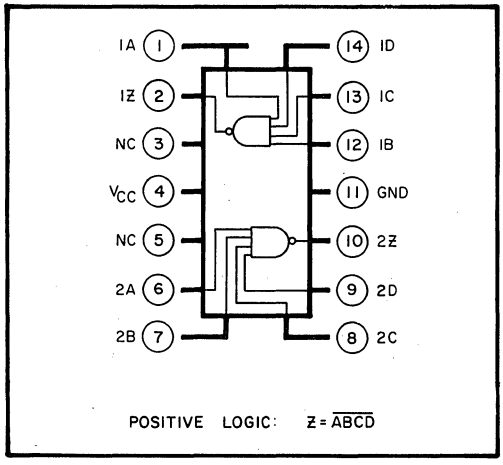
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		8.9	12	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level		6.8	10	ns	C_L = 25 pF, R_L = 280 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Duration of short-circuit test should not exceed 1 second.

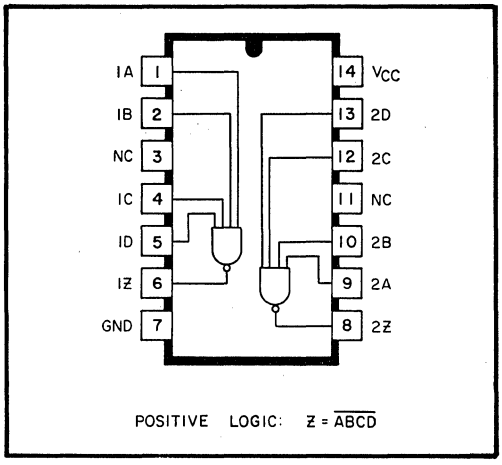
DUAL 4-INPUT POSITIVE NAND BUFFERS

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



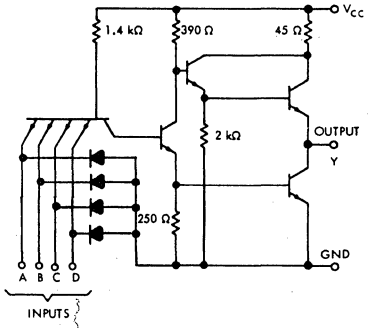
POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z} = \overline{ABCD}$

schematic (each gate)



NOTES: 1. Component values shown are nominal.
2. NC—No internal connection.

Recommended Operating Conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H40 Circuits	4.5	5	5.5	V
74H40 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			30	
Operating Free-Air Temperature Range, T_A: 54H40 Circuits	−55	25	125	°C
74H40 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.5 mA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 60 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−4	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current (each input)			100	uA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−125	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		25	40	mA	V_{CC} = MAX, V_{in} = 4.5 V
$I_{CC(1)}$	Logical 1 level supply current		10.4	16	mA	V_{CC} = MAX, V_{in} = 0

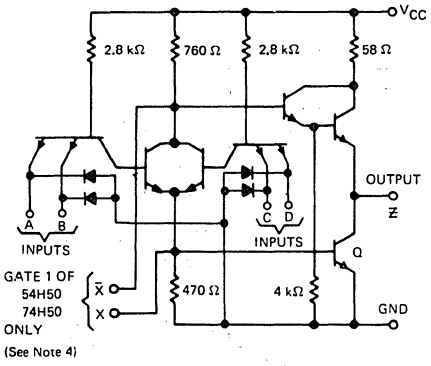
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.5	12	ns	C_L = 25 pF, R_L = 93 Ω
t_{pd1}	Propagation delay time to logical 1 level		8.5	12	ns	C_L = 25 pF, R_L = 93 Ω

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

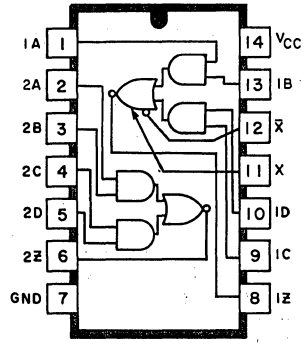
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

schematic (each gate)

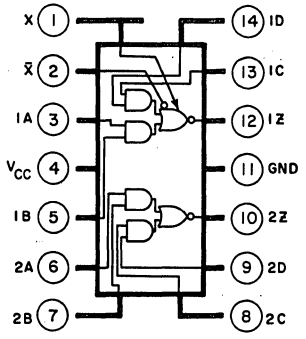


Notes:
1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the ITT54H50 and ITT75H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the ITT54H51 and ITT74H51.
5. A total of four ITT54H60/ITT74H60 expander gates may be connected to the expander inputs.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
$Z = \overline{(AB)+(CD)+(X)}$
(X = OUTPUT OF ITT 54H60/ITT 74H60

recommended operating conditions	Min	Nom	Max	Unit
Supply Voltage V_{CC}: 54H50, 54H51	4.5	5	5.5	V
74H50, 74H51	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: 54H50, 54H51	−55	25	125	°C
74H50, 74H51	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{cc} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8V, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		15.2	24	mA	V_{CC} = MAX, V_{in} = 4.5V
$I_{CC(1)}$	Logical 1 level supply current		8.2	12.8	mA	V_{CC} = MAX, V_{in} = 0

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

ELECTRICAL CHARACTERISTICS (ITT54H50 circuits only) using expander inputs, $V_{CC} = 4.5V, T_A = -55°C$

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$I_{in\overline{X}}$	Expander-node input current			−5.85	mA	$V_{\overline{X}} = 1.4V$
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q			1.1	V	$I_{sink} = 20mA, I_1 = 700uA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4			V	$I_{load} = -500uA, I_1 = 320uA, I_2 = -320uA$
$V_{out(0)}$	Logical 0 output voltage			0.4	V	$I_{sink} = 20mA, I_1 = 470uA, R_1 = 68\Omega$

ELECTRICAL CHARACTERISTICS (ITT74H50 circuits only) using expander inputs, $V_{CC} = 4.75V, T_A = 0°C$

Parameter		Min	Typ	Max	Unit	Test Conditions
$I_{in\overline{X}}$	Expander-node input current			−6.3	mA	$V_{\overline{X}} = 1.4V$
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q			1	V	$I_{sink} = 20mA, I_1 = 1.1mA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4			V	$I_{load} = -500uA, I_1 = 570uA, I_2 = -570uA$
$V_{out(0)}$	Logical 0 output voltage			0.4	V	$I_{sink} = 20mA, I_1 = 600uA, R_t = 63\Omega$

SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25°C, N = 10$, expander pins are open

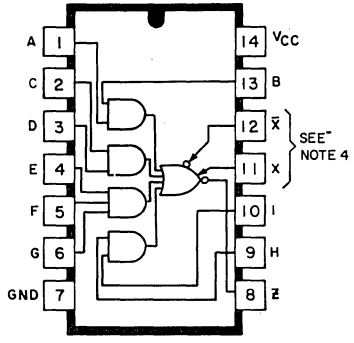
Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.2	11	ns	$C_L = 25 pF, R_L = 280\Omega$
t_{pd1}	Propagation delay time to logical 1 level		6.8	11	ns	$C_L = 25 pF, R_L = 280\Omega$

SWITCHING CHARACTERISTICS, (ITT54H50/ITT74H50 circuits only)
$V_{CC} = 5V, T_A = 25°C, N = 10, C_{\overline{X}} = 15 pF$

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7.4		ns	$C_L = 25 pF, R_L = 280\Omega$
t_{pd1}	Propagation delay time to logical 1 level		11.4		ns	$C_L = 25 pF, R_L = 280\Omega$

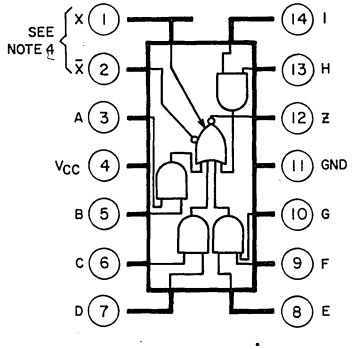
EXPANDABLE 2-2-2-3-INPUT AND-OR-INVERT GATES

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



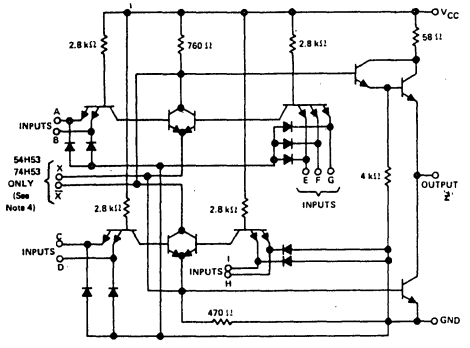
POSITIVE LOGIC: $\overline{Z=(AB)+(CD)+(EFG)+(HI)+(X)}$
(X=OUTPUT OF ITT54H60/ITT74H60 or ITT54H62/ITT74H62)

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $\overline{Z=(AB)+(CD)+(EFG)+(HI)+(X)}$
(X=OUTPUT OF ITT54H60/ITT74H60 or ITT54H62/ITT74H62)

schematic



Notes:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the ITT54H53 and ITT74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the ITT54H54 and ITT74H74.
5. A total of four ITT54H60/ITT74H60 expander gates may be connected to the expander inputs.

recommended operating conditions

	Min	Nom	Max	Unit
Supply Voltage V_{CC}: ITT54H53, ITT54H54	4.5	5	5.5	V
ITT74H53, ITT74H54	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: ITT54H53, ITT54H54	−55	25	125	°C
ITT74H53, ITT74H54	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	2			V	
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output			0.8	V	
V_1	Insure Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −8mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, V_{in} = 0.8V, I_{load} = −500uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 20mA
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX
$I_{CC(0)}$	Logical 0 level supply current		9.4	14	mA	V_{CC} = MAX, V_{in} = 4.5V
$I_{CC(1)}$	Logical 1 level supply current		7.1	11	mA	V_{CC} = MAX, V_{in} = 0

[1] Duration of short-circuit test should not exceed 1 second
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
[3] All typical values are at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (ITT54H53 circuits only) using expander inputs, $V_{CC} = 4.5V, T_A = -55°C$

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$I_{in\overline{X}}$	Expander-node input current			−5.85	mA	$V_{\overline{X}} = 1.4V$
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q			1.1	V	$I_{sink} = 20mA, I_1 = 700uA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4			V	$I_{load} = -500uA, I_1 = 320uA, I_2 = -320uA$
$V_{out(0)}$	Logical 0 output voltage			0.4	V	$I_{sink} = 20mA, I_1 = 470uA, R_1 = 68\Omega$

ELECTRICAL CHARACTERISTICS (ITT74H53 circuits only) using expander inputs, $V_{CC} = 4.75V, T_A = 0°C$

Parameter		Min	Typ	Max	Unit	Test Conditions
$I_{in\overline{X}}$	Expander-node input current			−6.3	mA	$V_{\overline{X}} = 1.4V$
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q			1	V	$I_{sink} = 20mA, I_1 = 1.1mA, R_1 = 0$
$V_{out(1)}$	Logical 1 output voltage	2.4			V	$I_{load} = -500uA, I_1 = 570uA, I_2 = -570uA$
$V_{out(0)}$	Logical 0 output voltage			0.4	V	$I_{sink} = 20mA, I_1 = 600uA, R_t = 63\Omega$

SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25°C, N = 10$, expander pins are open

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		6.2	11	ns	$C_L = 25 pF, R_L = 280\Omega$
t_{pd1}	Propagation delay time to logical 1 level		7	11	ns	$C_L = 25 pF, R_L = 280\Omega$

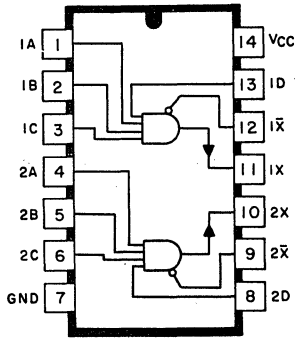
SWITCHING CHARACTERISTICS, (ITT54H53/ITT74H53 circuits only) $V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15 pF$

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{pd0}	Propagation delay time to logical 0 level		7.4		ns	$C_L = 25 pF, R_L = 280\Omega$
t_{pd1}	Propagation delay time to logical 1 level		11.4		ns	$C_L = 25 pF, R_L = 280\Omega$

ITT SEMICONDUCTORS

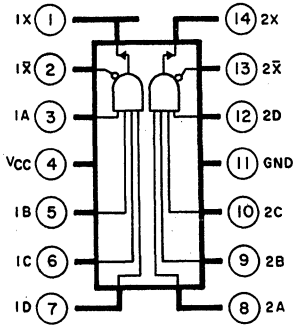
DUAL 4-INPUT EXPANDER

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



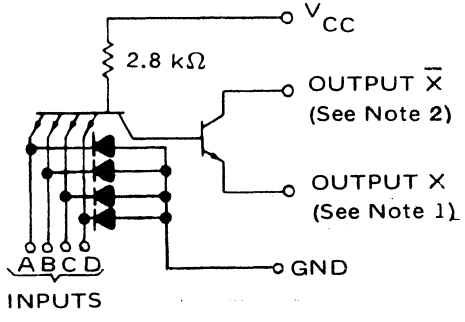
POSITIVE LOGIC: X=ABCD
WHEN CONNECTED TO X AND X̄ PINS OF ITT54H50, ITT54H53, or ITT54H55 CIRCUIT.

FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:
X=ABCD
WHEN CONNECTED TO X AND X̄ PINS OF ITT7450 OR 7453

schematic (each expander)



recommended operating conditions

Supply Voltage V_{CC} ..... 4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one ITT54H50, ITT54H53 circuit ... 4

Notes:
1. Connect to X input of ITT54H50, ITT54H53 circuit.
2. Connect to X̄ input of ITT54H50, ITT54H53 circuit.
3. Component values shown are nominal.

ITT54H60
DUAL 4-INPUT EXPANDER
(FOR USE WITH ITT54H50, ITT54H53, CIRCUITS)

ELECTRICAL CHARACTERISTICS (unless otherwise noted $T_A = -55°C$ to $125°C$)

Parameter		Min	Typ	Max	Unit	Test Conditions
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	2			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state			0.8	V	
V_{on}	On-state output voltage			0.4	V	$V_{CC} = 4.5V, V_{in} = 2V, V_1 = 1V, I_{on} = 5.85mA, T_A = -55°C$
				0.4	V	$V_{CC} = 5.5V, V_{in} = 2V, V_1 = 0.6V, I_{on} = 7.85mA, T_A = 125°C$
I_{off}	Off-state output current			320	uA	$V_{CC} = 4.5V, V_{in} = 0.8V, V_1 = 4.5V, R = 575\,\Omega, T_A = -55°C$
I_{on}	On-state output current	−470			uA	$V_{CC} = 4.5V, V_{in} = 2V, V_1 = 1V, T_A = -55°C$
$I_{in(0)}$	Logical 0 level input current (each input)			−2	mA	$V_{CC} = 5.5V, V_{in} = 0.4V$
$I_{in(1)}$	Logical 1 level input current (each input)			50	uA	$V_{CC} = 5.5V, V_{in} = 2.4V$
				1	mA	$V_{CC} = 5.5V, V_{in} = 5.5V$
$I_{CC(on)}$	On-state supply current		1.9	3.5	mA	$V_{CC} = 5.5V, V_{in} = 4.5V, V_1 = 0.85V$
$I_{CC(off)}$	Off-state supply current		3	4.5	mA	$V_{CC} = 5.5V, V_{in} = 0, V_1 = 0.85V$

[1] All typical values are at $V_{CC} = 5V, T_A = 25°C$.

OUTPUT CAPACITANCE, V_{CC} and GND terminals open, $T_A = 25°C$

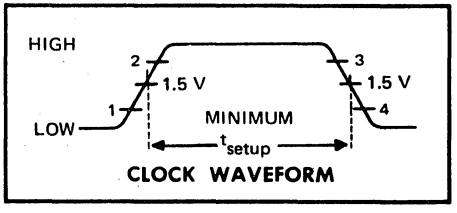
Parameter		Min	Typ	Max	Unit	Test Conditions
C_x	Effective capacitance of output transistor Q_1		1.3		pF	f = 1 MHz

J-K MASTER-SLAVE FLIP-FLOPS

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

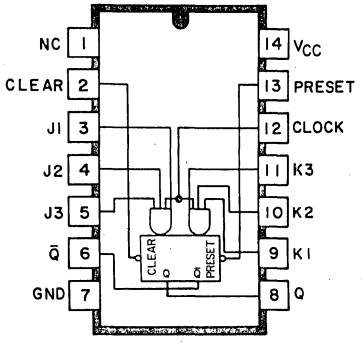
1. Isolate salve from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

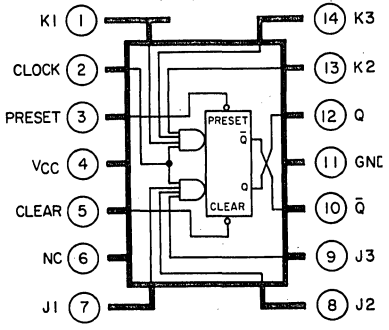


CLOCK WAVEFORM

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC:

LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET OR CLEAR ARE INDEPENDENT OF CLOCK

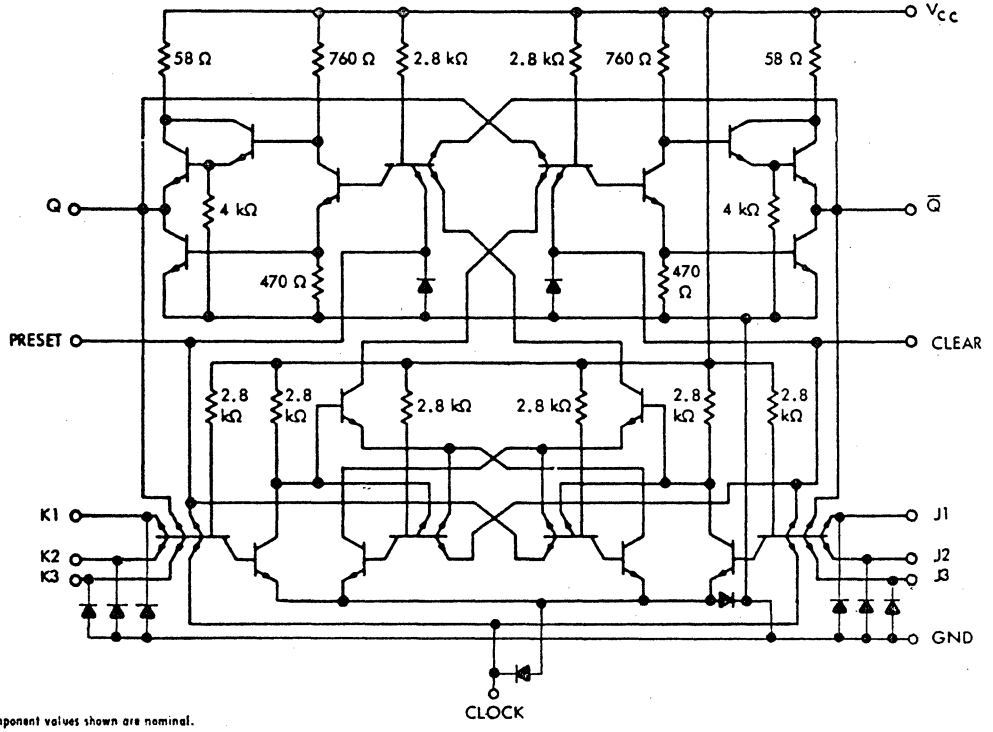
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Notes:
1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

recommended operating conditions		Min	Nom	Max	Unit
Short Voltage V_{CC}:	ITT54H72	4.5	5	5.5	V
	ITT74H72	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	ITT54H72	−55	25	125	°C
	ITT74H72	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)		12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)		16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)		16			ns
Input Setup Time, t_{setup} (See Above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

schematic



Component values shown are nominal.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −500uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 20mA
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_1 = −8mA
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock			−2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at preset or clear			−4	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at clock			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at preset or clear			100	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit current [3]	−40		−100	mA	V_{CC} = MAX, V_{in} = 0
I_{CC}	Supply current		16	25	mA	V_{CC} = MAX

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
f_{clock}	Maximum clock frequency	25	30		MHz	C_L = 25 pF, R_L = 280Ω
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output		6	13	ns	C_L = 25 pF, R_L = 280Ω
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output		12	24	ns	C_L = 25 pF, R_L = 280Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	6	14	21	ns	C_L = 25 pF, R_L = 280Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	22	27	ns	C_L = 25 pF, R_L = 280Ω

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type

[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

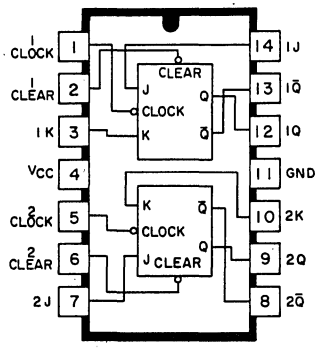
DUAL J-K MASTER-SLAVE FLIP-FLOPS

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.
The sequence of operation is as follows:

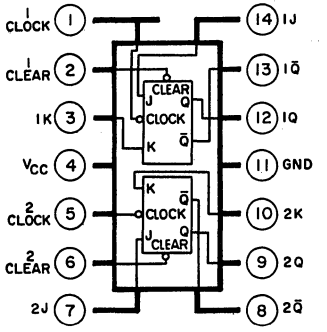
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



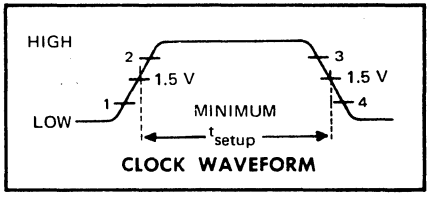
POSITIVE LOGIC:
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
CLEAR IS INDEPENDENT OF CLOCK

Logic

TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES 1. t_n = Bit time before clock pulse.
2. t_n+1 = Bit time after clock pulse.



CLOCK WAVEFORM

recommended operating conditions		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC}	ITT54H73 Circuits	4.5	5	5.5	V
	ITT74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	ITT54H73	−55	25	125	°C
	ITT74H73	0	25	70	°C
Normalized Fan-Out from Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}		$t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
V_1	Input Clamp Voltage			−1.5	V	V_{CC} = Min I_i = −8 mA
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −500 uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 20 mA
$I_{in(0)}$	Logical 0 level input current at J, K, or clock			−2	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at clear			−4	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current at J or K			50	µA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{in(1)}$	Logical 1 level input current at clock			50	µA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
$I_{in(1)}$	Logical 1 level input current at clear			100	µA	V_{CC} = MAX, V_{in} = 2.4 V
				1	mA	V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX, V_{in} = 0
I_{CC}	Supply current		32	50	mA	V_{CC} = MAX

[1] All typical values are at V_{CC} = 5 V, T_A = 25°C.

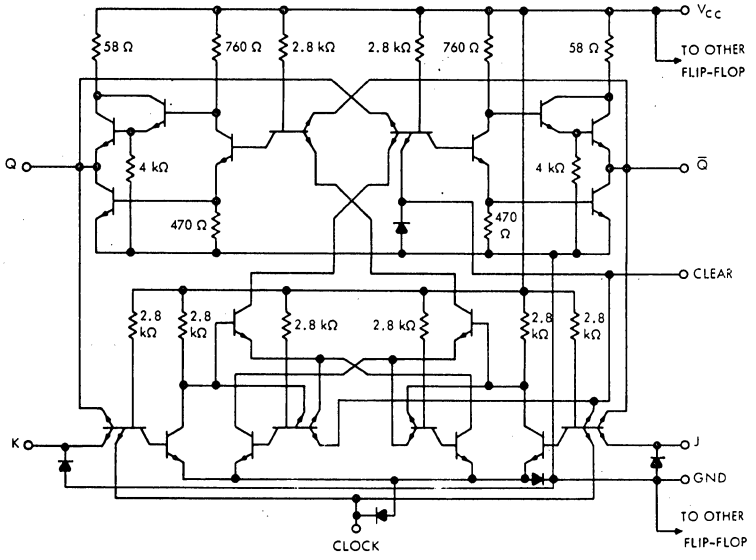
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time, and duration of short-circuit should not exceed 1 second.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{clock}	Maximum clock frequency	25	30		MHz	C_L = 25pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear to output		6	13	ns	C_L = 25pF, R_L = 280 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear to output		12	24	ns	C_L = 25pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	6	14	21	ns	C_L = 25pF, R_L = 280 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	22	27	ns	C_L = 25pF, R_L = 280 Ω

schematic (each flip-flop)



Component values shown are nominal

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- **Maximum Clock Frequency: 35 Megahertz**
- **Positive-Edge Triggering**
- **High-Fan Out, Low-Impedance, Totem-Pole Outputs**
- **Input Clamping Diodes Simplify System Design**
- **Fully Compatible with most TTL and DTL Circuits**
- **Typical Power Dissipation: 75 Milliwatts per Flip-Flop**

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

logic

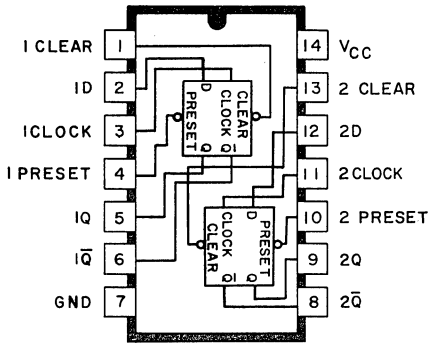
TRUTH TABLE
(Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

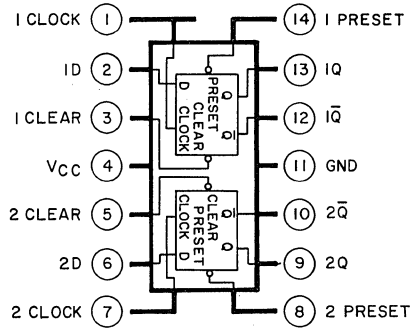
H = high level, L = low level

Notes: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



FLAT PACKAGE
PIN CONFIGURATION
(TOP VIEW)



ASYNCHRONOUS INPUTS:
LOW INPUT TO PRESET SETS Q TO HIGH LEVEL
LOW INPUT TO CLEAR SETS Q TO LOW LEVEL
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

CIRCUIT TYPES ITT54H74, ITT74H74

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs.

Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The ITT54H74 is characterized for operation over the full military temperature range of −55°C to 125°C; the ITT74H74 is characterized for operation from 0°C to 70°C.

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

	Parameter	Min	Typ [1]	Max	Unit	Test Conditions [2]	
V_{IH}	High-level input voltage	2			V		
V_{IL}	Low-level input voltage			0.8	V		
V_L	Input Clamp Voltage			−1.5	V	V_{CC} = MIN, I_i = −8 mA	
V_{OH}	High-level output voltage	2.4	3.5		V	V_{CC} = MIN, I_{OH} = −1 mA	
V_{OL}	Low-level output voltage		0.22	0.4	V	V_{CC} = MIN, I_{OL} = 20 mA	
I_{IH}	High-level input current into D			50	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current into preset or clock			100	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IH}	High-level input current into clear			150	uA	V_{CC} = MAX, V_I = 2.4V	
				1	mA	V_{CC} = MAX, V_I = 5.5V	
I_{IL}	Low-level input current into preset or D			−2	mA	V_{CC} = MAX, V_I = 0.4V	
I_{IL}	Low-level input current into clear or clock			−4	mA	V_{CC} = MAX, V_I = 0.4V	
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX	
I_{CC}	Supply current		30	42	mA	V_{CC} = MAX	ITT54H74
			30	50			ITT74H74

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

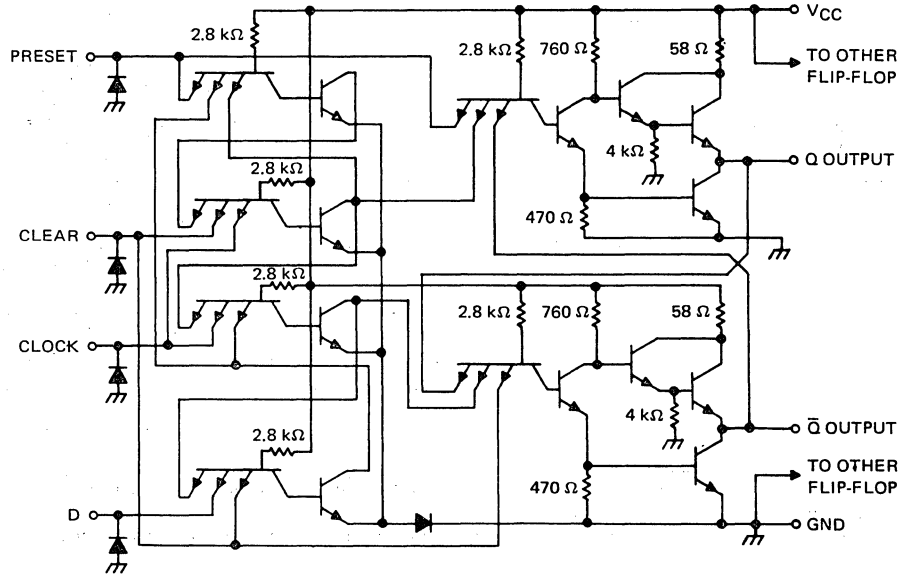
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
f_{max}	Maximum clock frequency	35	43		MHz	C_L = 25 pF, R_L = 280Ω
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs			20	ns	C_L = 25 pF, R_L = 280Ω
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs			30	ns	C_L = 25 pF, R_L = 280Ω
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input	4	8.5	15	ns	C_L = 25 pF, R_L = 280Ω
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input	7	13	20	ns	C_L = 25 pF, R_L = 280Ω

schematic (each flip-flop)



Note: Component values shown are nominal.

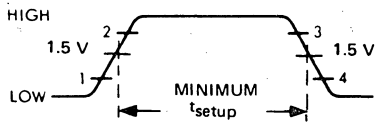
DUAL J-K MASTER-SLAVE FLIP-FLOPS

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

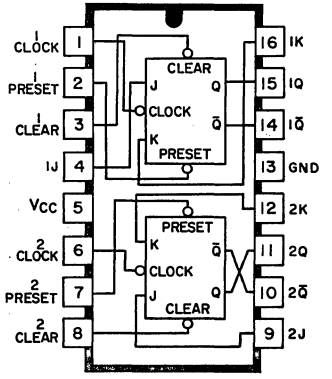
1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

CLOCK WAVEFORM



DUAL-IN-LINE PACKAGE AND FLAT PACKAGE
PIN CONFIGURATION (TOP VIEW)†



POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
CLEAR AND PRESET ARE INDENPENDENT OF CLOCK

†PIN ASSIGNMENTS FOR THESE CIRCUITS ARE THE SAME FOR ALL PACKAGES.

logic

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

Notes: 1. t_n = Bit time before clock
2. t_{n+1} = Bit time after clock pulse

recommended operating conditions

	ITT54H76			ITT74H76			
	Min	Nom	Max	Min	Nom	Max	Unit
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output N			10			10	
Width of clock pulse, $t_{p(clock)}$	12			12			ns
Width of preset pulse, $t_{p(preset)}$	16			16			ns
Width of clear pulse, $t_{p(clear)}$	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input setup time, t_{setup}							
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Min	Typ [1]	Max	Unit	Test Conditions [2]
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	2			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal			0.8	V	
$V_{out(1)}$	Logical 1 output voltage	2.4			V	V_{CC} = MIN, I_{load} = −500uA
$V_{out(0)}$	Logical 0 output voltage			0.4	V	V_{CC} = MIN, I_{sink} = 20mA
$I_{in(0)}$	Logical 0 level input current at J, K, or clock			−2	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(0)}$	Logical 0 level input current at clear or preset			−4	mA	V_{CC} = MAX, V_{in} = 0.4V
$I_{in(1)}$	Logical 1 level input current at J, K, or clock			50	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
$I_{in(1)}$	Logical 1 level input current at clear or preset			100	uA	V_{CC} = MAX, V_{in} = 2.4V
				1	mA	V_{CC} = MAX, V_{in} = 5.5V
I_{OS}	Short-circuit output current [3]	−40		−100	mA	V_{CC} = MAX, V_{in} = 0
I_{CC}	Supply current		32	50	mA	V_{CC} = MAX, V_{in} = 4.5V

[1] All typical values are at V_{CC} = 5V, T_A = 25°C.

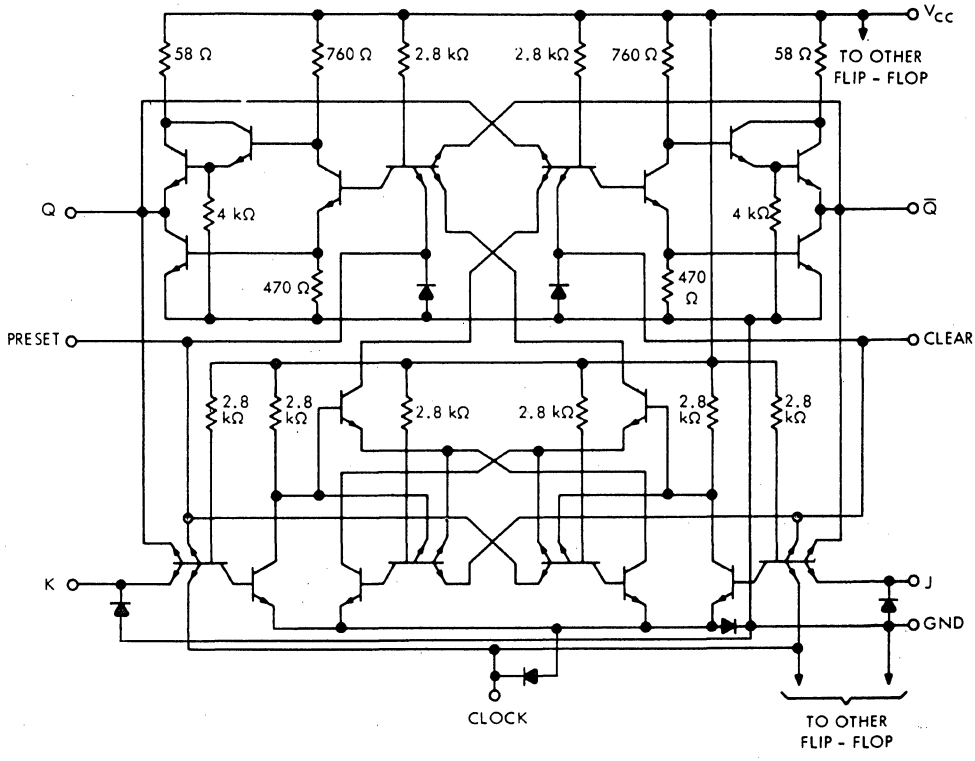
[2] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

Parameter		Min	Typ	Max	Unit	Test Conditions
t_{clock}	Maximum clock frequency	25	30		MHz	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output		6	13	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output		12	24	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd1}	Propagation delay time to logical 1 level from clock to output	6	14	21	ns	C_L = 25 pF, R_L = 280 Ω
t_{pd0}	Propagation delay time to logical 0 level from clock to output	10	22	27	ns	C_L = 25 pF, R_L = 280 Ω

schematic (each flip-flop)



Component values shown are nominal.

HIGH SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS

- **Single power supply requirements: 5 volts optimum, 4.5 to 5.5 volts range**
- **High speed: typical gate propagation delay time of 7 ns**
- **High DC noise margin: typically one volt**
- **Added input diodes and low output impedance provides minimum AC noise susceptibility**
- **Fan Out: 10TTL loads**
- **Power dissipation: 11mw per NAND gate at a 50% duty cycle**
- **Compatible with ITT DTL family and other DTL and TTL circuits**
- **NAND gate pin configurations are compatible with DTL**

The ITT9000 Series of TTL circuits is designed to be used in any digital system where good noise immunity, high spped, medium power and high fan-out performance is required. The line is characterized by a broad number of functions available in a variety of packages. The basic elements of the family are active low level output AND gates commonly known as NAND gates.

Typical high level noise immunity of every device in the family is 1.9 V and typical low level noise immunity is 0.9 V. Worst case immunity is 400 mV over the entire temperature range. Power dissipation is typically 11 mW per gate function at a 50% duty cycle, and the average propagation delay is 7 nanoseconds per gate function. A single 5 V 10 per cent power supply is used with the circuits.

The gates were designed to provide low output impedance in both high and low states which results in good capacitive drive capability and good immunity to crosstalk. The output impedance in the low state is about 10 ohms and in the high state, about 20 ohms. To further enhance noise immunity, all inputs of all devices incorporate diode clamps which considerably reduces the ringing which can result from long lines and impedance mismatches. The binary elements are of a JK, DC master slace design and will toggle at 40 MHz, except for the 9000 element. The 9000 has capacitors purposely incorporated in the design to increase its set-up time and provide it with considerable immunity to long clock skew. Due to the longer set-up time the 9000 toggle frequency is 20 MHz. A common JK input is incorporated on all binary elements to provide data entry inhibit/enable. The input to the clock on each element is buffered to reduce the clock input loading.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allows two degrees of freedom in routing of power and ground leads on the PC boards. Special care has been taken in establishing pin-outs for the flip-flop so as to minimize cross-overs when laying out common dynamic functions with these elements. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device will be quickly established.

The ITT9000 series TTL is compatible with DTL and MSI devices as well as the more complex functions which will be available in the future.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to 150°C
Temperature (Ambient) Under Bias (ITT9000-1)	—55°C to + 125°C
Temperature (Ambient) Under Bias ITT9000-5)	0°C to + 75°C
V_{CC} Pin Potential to Ground (See Note 1)	—0.5V to + 8.0V
Input Voltage (D.C.) (See Note 2)	—0.5V to + 5.5V
Input Current (See Note 2)	—30mA to + 5.0 mA
Output Voltage, Output Normally High	0 V to + V_{CC} value
Current Into Output Terminal, Output Low (except 9009)	50 mA
Current Into Output Terminal, Output Low 9009	100 mA

NOTE 1

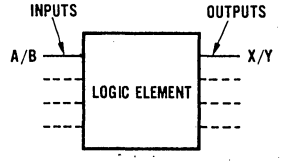
The maximum VCC value of 8.0 volts is not the primary factor in determining the maximum VCC which may be applied to a number of interconnected devices. The voltage at a high output is approximately 2 VBE's below the VCC voltage, so the primary limit on the VCC is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system VCC to approximately 7.0 volts.

NOTE 2

Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than —0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where A = high logic level input load factor
B = low logic level input load factor
X = high logic level output drive factor
Y = low logic level output drive factor

When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for the low level load and drive factors. These rules apply only within the TTL ITT9000 series.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the TTL circuits of this data sheet, current per unit is —1.6 mA maximum at the low logic level and is 60uA maximum at the high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for the inputs will be the number of inputs shorted together times the high logic input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

UNUSED INPUTS

Proper termination of unused inputs will result in maximum operating speed. Substantial degradation of turn-on delay may occur if unused inputs are left open.

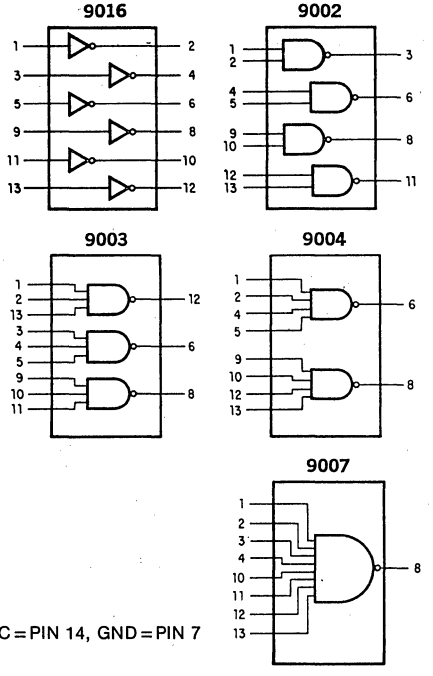
The following are acceptable ways to terminate unused inputs:

1. Tie the input to a used input on the same gate. The TTL 9000 series has made special provision for this method by offering extra high level drive factor on all inputs.
2. Tie the input to Vcc through a resistor. This resistor should be chosen to keep the input current within absolute maximum ratings for any possible extrem of the Vcc supply. More than one input may be terminated through one resistor.
3. Tie inputs to a separate supply between 4.5 and 2.4 V, if one should be available.
4. Tie he inputs to the output of an unused gate. The unused gate must provide a constant high level output.

NAND GATES—9002, 9003, 9004 AND 9007 HEX INVERTER—9016

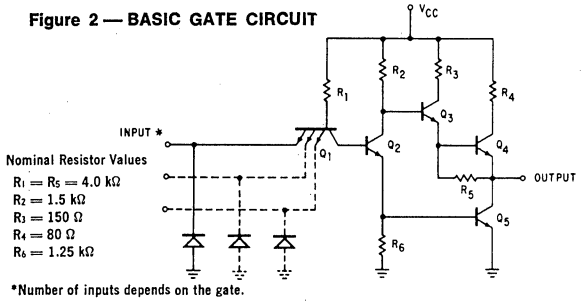
The 9002, 9003, 9004 and 9007 are active low level output AND gates commonly known as NAND gates. The 9016 is a hex inverter with input and output characteristics identical to the 9002, 9003, 9004 and 9007. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

Figure 1 — LOGIC SYMBOL AND PIN CONFIGURATIONS



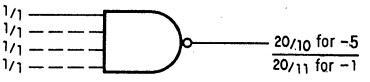
VCC = PIN 14, GND = PIN 7

Figure 2 — BASIC GATE CIRCUIT



*Number of inputs depends on the gate.

Figure 3 — LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = −55°C to 125°C, V_{CC} = 5.0 V ± 10%)

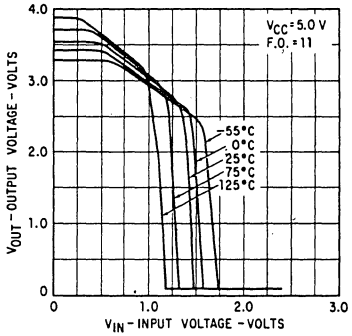
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.32 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 13.6 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−1.24		−0.87	−1.24		-1.24		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		1.6		1.07	1.6		1.6		Inputs at gnd
t_{pd+}	Switching Speed			3.0		10			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		12			ns	C_L = 15 pF

ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = 0°C to 75°C, V_{CC} = 5.0 V ± 5%)

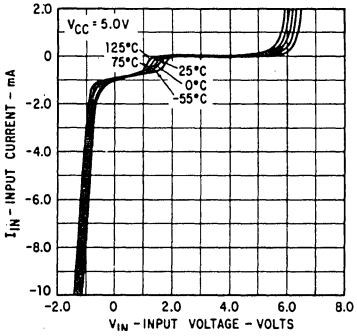
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75V I_{OH} = −1.2 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			-1.41		−0.91	−1.41		-1.41		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		6.1		3.6	6.1		6.1	mA	Inputs high V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		1.7		1.07	1.7		1.7		Inputs at gnd
t_{pd+}	Switching Speed			3.0		13			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		15			ns	C_L = 15 pF

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9002, 9003, 9004, 9007 and 9016

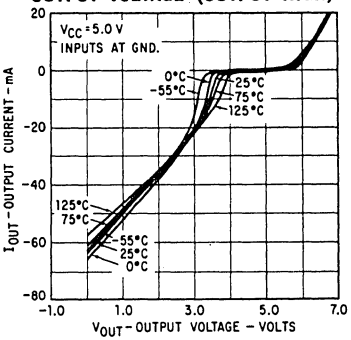
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



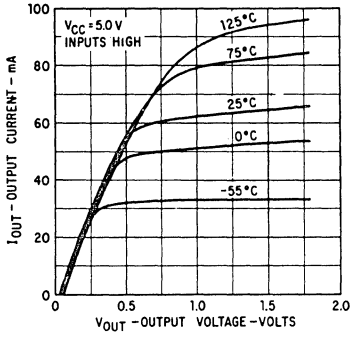
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

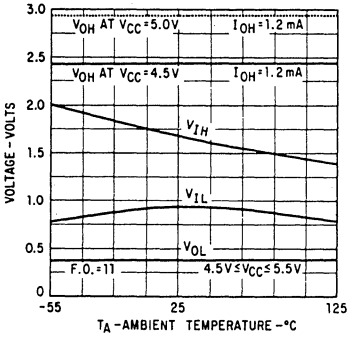


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

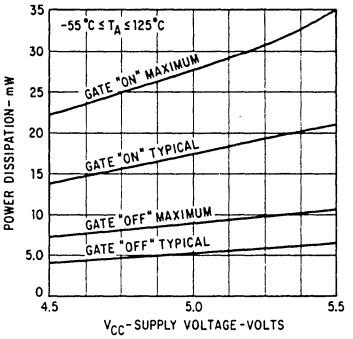


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

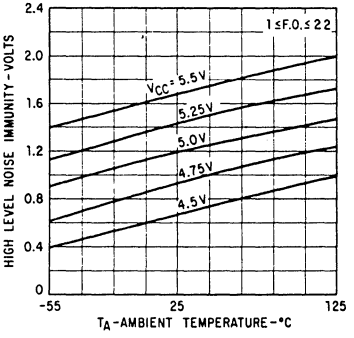
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



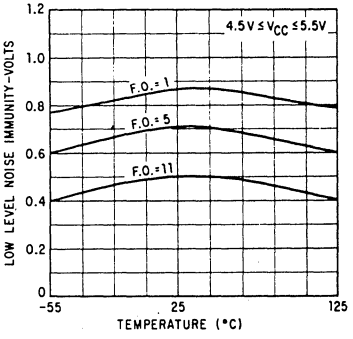
POWER DISSIPATION VERSUS SUPPLY VOLTAGE



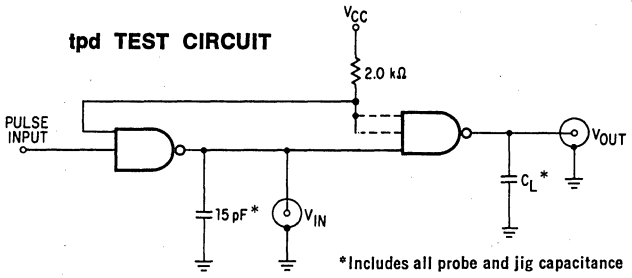
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



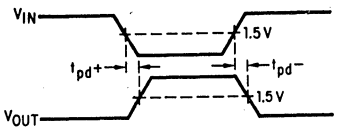
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



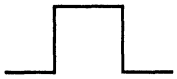
tpd TEST CIRCUIT



SWITCHING WAVEFORM



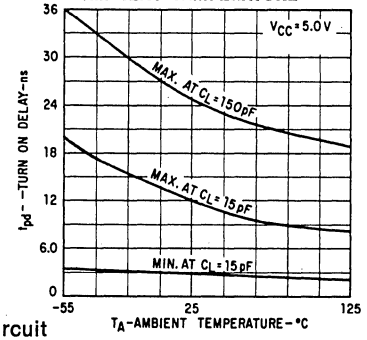
SWITCHING CHARACTERISTICS



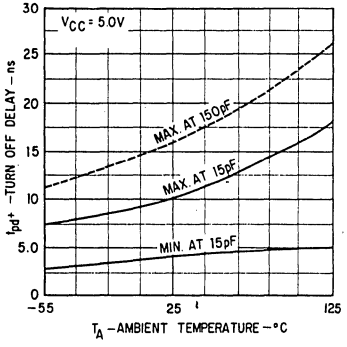
f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_f = t_r \leq 10$ ns

*See t_{pd} test circuit

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



NAND BUFFER — 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fanout applications. Logically it is the same as the 9004.

Figure 4 LOADING FACTORS

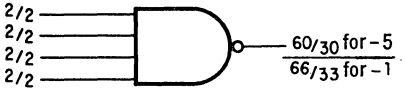


Figure 6 CIRCUIT DIAGRAM (One Gate)

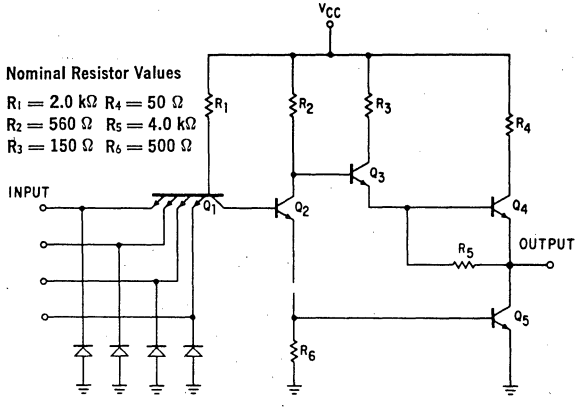
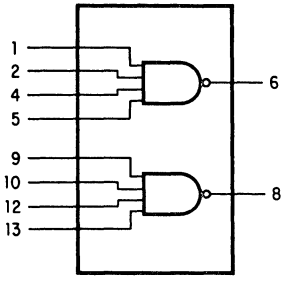


Figure 5 LOGIC DIAGRAM AND PIN CONFIGURATION



VCC = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS 9009

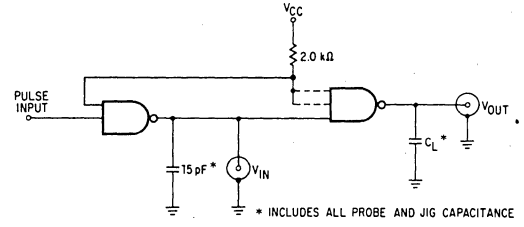
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC}=4.5$ V $I_{OH}=-3.96$ mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC}=5.5$ V $I_{OL}=52.8$ mA $V_{IH}=5.5$ V
										$V_{CC}=4.5$ V $I_{OL}=40.8$ mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		3.2		2.15	3.2		3.2	mA	$V_{CC}=5.5$ V, $V_F=0.4$ V
			−2.48		−1.74	−2.48		−2.48		$V_{CC}=4.5$ V, 5.5 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	$V_{CC}=5.5$ V $V_R=4.5$ V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	$V_{CC}=5.0$ V, Inputs high
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2	mA	$V_{CC}=5.0$ V, Inputs grounded
t_{pd+}	Switching Speed				4.0	15			ns	$V_{CC}=5.0$ V, See t_{pd} test circuit
t_{pd-}	Switching Speed				3.0	10			ns	$C_L=15$ pF

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	$V_{CC}=4.75$ V $I_{OH}=-3.6$ mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC}=5.25$ V $I_{OL}=48.0$ mA $V_{IH}=5.25$ V
										$V_{CC}=4.75$ V $I_{OL}=42.3$ mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC}=5.25$ V, $V_F=0.45$ V
			−2.82		−1.82	−2.82		−2.82	mA	$V_{CC}=4.75$ V, 5.25 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	$V_{CC}=5.25$ V $V_R=4.5$ V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs high, $V_{CC}=5.0$ V
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4	mA	Inputs at gnd, $V_{CC}=5.0$ V
t_{pd+}	Switching Speed				3.0	17			ns	$V_{CC}=5.0$ V, See t_{pd} test
t_{pd-}	Switching Speed				2.0	13			ns	circuit $C_L=15$ pF

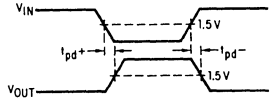
SWITCHING CHARACTERISTICS

f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

tpd TEST CIRCUIT

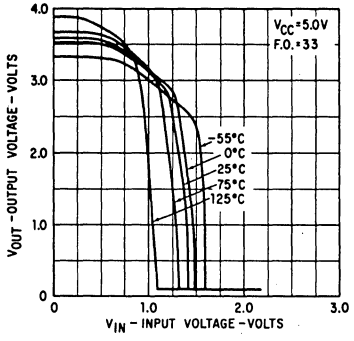


SWITCHING WAVEFORM

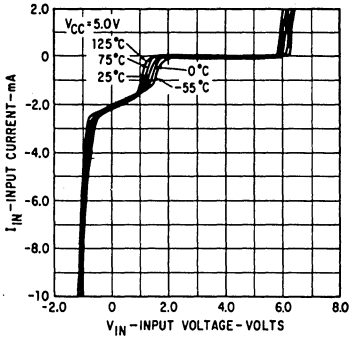


TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9009

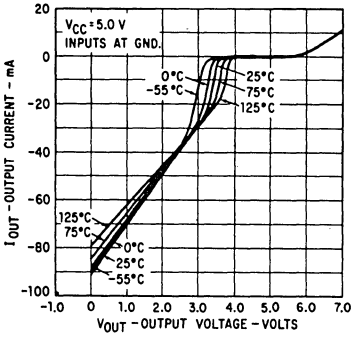
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



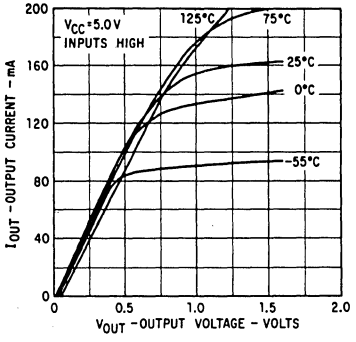
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

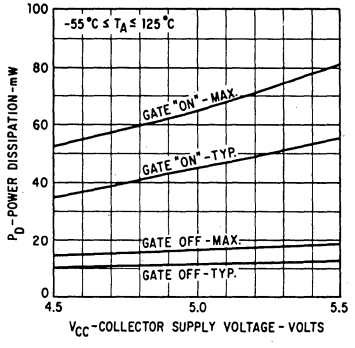


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

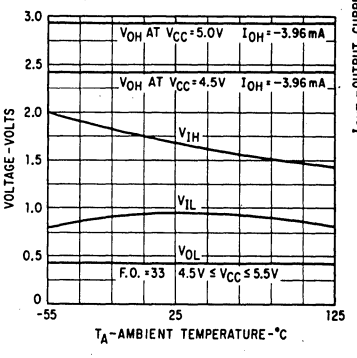


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

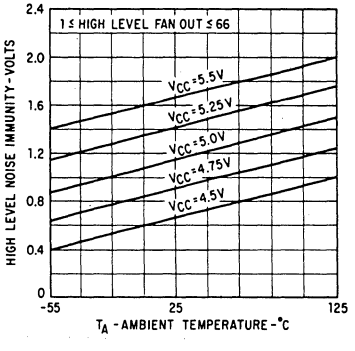


WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

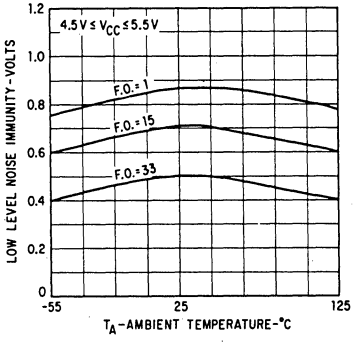


9009-1

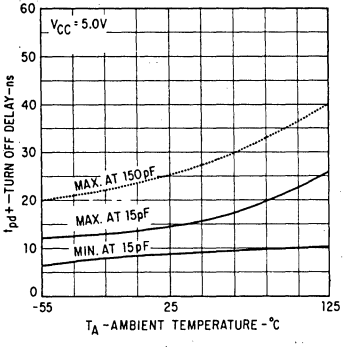
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



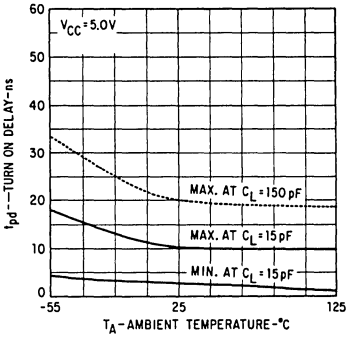
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



*SEE TEST CIRCUIT

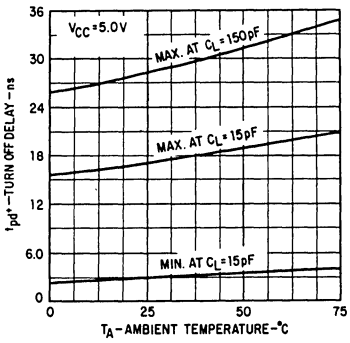
9009-1

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

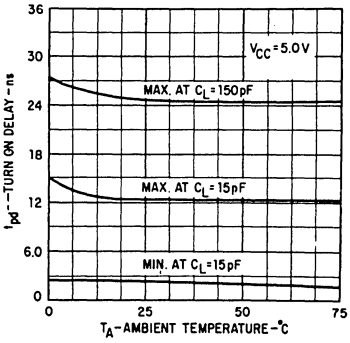


9009-5

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



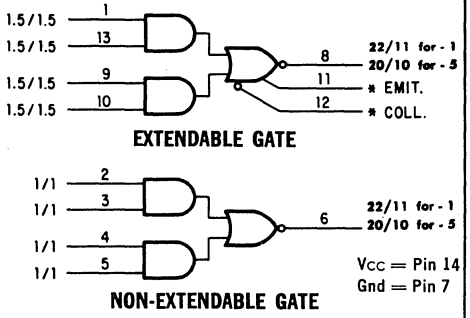
EXTENDABLE AND-OR-INVERT GATES — 9005, 9008, EXTENDER — 9006

The TTL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section.

LOGIC DIAGRAMS AND LOADING FACTORS

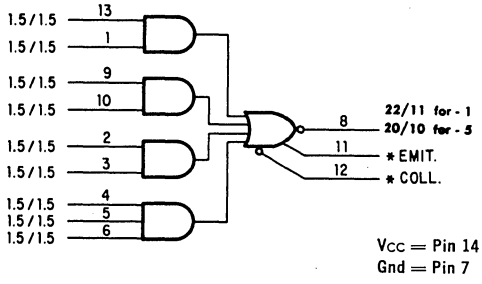
The numbers by each input and output give the input loading and output drive capability. For complete expanation see Page 2 and 3.

9005



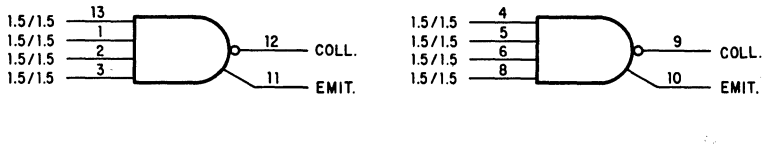
*Four Extenders (9006) may be tied to these terminals

9008



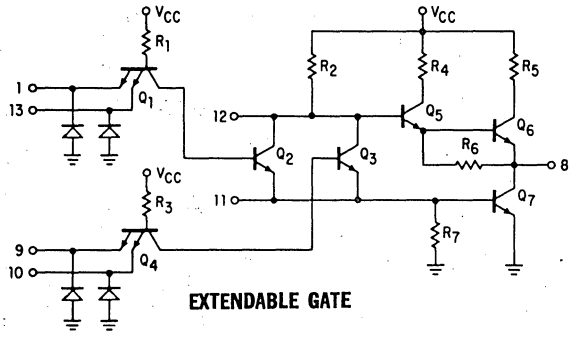
*Four Extenders (9006) may be tied to these terminals

9006

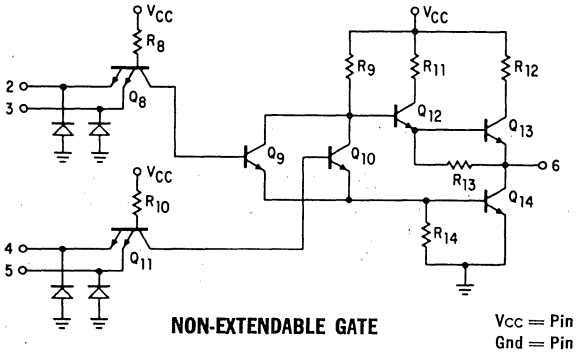


CIRCUIT DIAGRAMS

9005



EXTENDABLE GATE



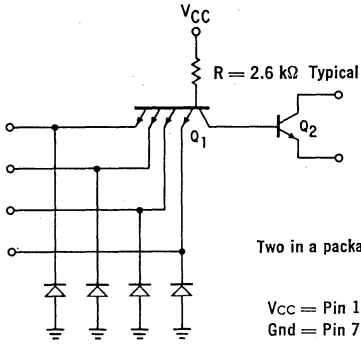
NON-EXTENDABLE GATE

VCC = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} = 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

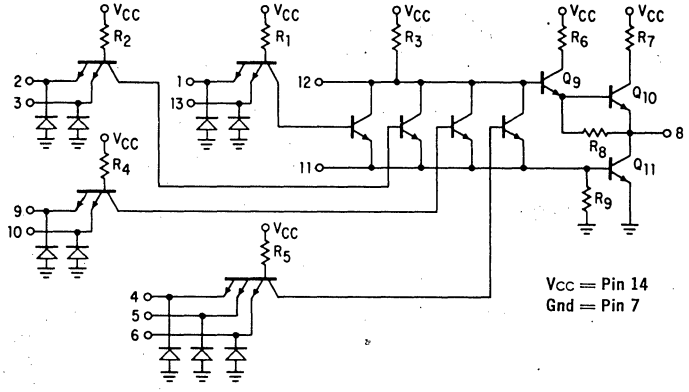
9006



Two in a package

VCC = Pin 14
Gnd = Pin 7

9008



VCC = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

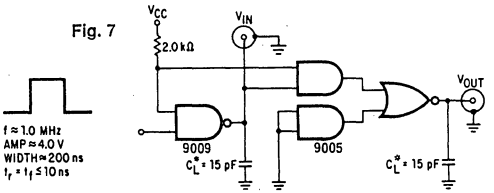
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.32\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 17.6\ mA$ $V_{IH} = 5.5\ V$
										$V_{CC} = 4.5\ V$ $I_{OL} = 13.6\ mA$ V_{IH} = (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$
	9005 Non-Extendable Gate		−1.24		-0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$ $V_F = 0.4\ V$, 5.5 V on other inputs
	Input Load Current		−2.4		−1.5	−2.4		−2.4	μA	$V_{CC} = 5.5\ V$
	Extendable Gate and Extender		−1.86		-1.31	−1.86		−1.86		$V_{CC} = 4.5\ V$
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	mA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Gnd on all other inputs
	Input Leakage Current Extendable Gate and Extender				7.5	90		90		
I_{PD}	V_{CC} Current, Gate "ON"								mA	
	9005 Non-Extendable Gate		6.5		4.5	6.5		6.5		$V_{CC} = 5.0\ V$ All inputs open
	9005 Extendable Gate		11.3		7.6	11.3		11.3		
	9008		12.5		9.3	12.5		12.5		
	V_{CC} Current, Gate "OFF"								mA	
	9005 Non-Extendable Gate		3.1		2.1	3.1		3.1		$V_{CC} = 5.0\ V$ All inputs except extender inputs gnd.
	9005 Extendable Gate		4.7		3.3	4.7		4.7		
	9008		9.4		6.6	9.4		9.4		
ΔI_{PD}	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	$V_{CC} = 5.0\ V$ All inputs high 9006 attached to a 9005
	Extra Current Drain from one 9006 Extender Gate "OFF"		2.35		1.65	2.35		2.35	mA	$V_{CC} = 5.0\ V$ All inputs grounded 9006 attached to a 9005

Note:
Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

AC CHARACTERISTICS tpd Test Circuit

9005 NON-EXTENDABLE GATE

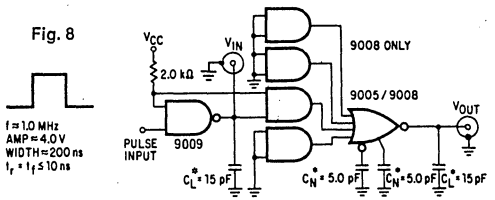
Fig. 7



*Includes all probe and/or jig capacitance.

9005 OR 9008 EXTENDABLE GATE

Fig. 8



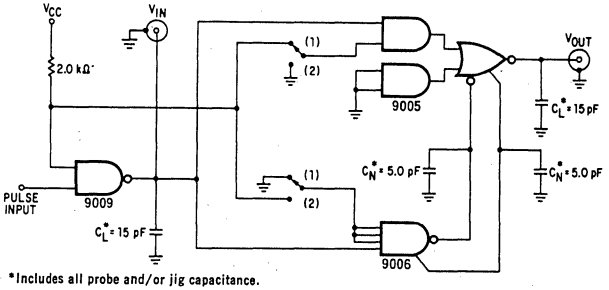
*Includes all probe and/or jig capacitance.

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.04	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$
	9005 Non-Extendable Gate		−1.41		−0.79	−1.41		−1.41		$V_{CC} = 4.75\ V$
	Input Load Current		−2.4		−1.56	−2.4		−2.4	mA	$V_{CC} = 5.25\ V$
	9005 Extendable Gates and Extender		−2.12		−1.19	−2.12		−2.12		$V_{CC} = 4.75\ V$
										$V_F = 0.45\ V$, 5.25 V on other inputs
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	μA	$V_R = 4.5\ V$ $V_{CC} = 4.75\ V$ Gnd on all other inputs
	Input Leakage Current Extendable Gates and Extender				7.5	90		90		
I_{PD}	V_{CC} Current, Gate "ON"								mA	$V_{CC} = 5.0\ V$ All inputs open
	9005 Non-Extendable Gate		7.7		4.5	7.7		7.7		
	9005 Extendable Gate		13.6		7.6	13.6		13.6		
	9008		17.7		9.3	17.7		17.7		
	V_{CC} Current, Gate "OFF"								mA	$V_{CC} = 5.0\ V$ All inputs except extender inputs gnd.
	9005 Non-Extendable Gate		3.4		2.2	3.4		3.4		
	9005 Extendable Gate		5.1		3.3	5.1		5.1		
	9008		10.2		6.6	10.2		10.2		
$\triangle I_{PD}$	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	$V_{CC} = 5.0\ V$ All inputs high
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "OFF"		2.54		1.65	2.54		2.54	mA	$V_{CC} = 5.0\ V$ All inputs grounded

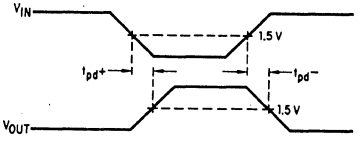
Note: Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external

Figure 9 **9006 EXTENDER**



*Includes all probe and/or jig capacitance.

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure tpd of 9005. With switch in position (2) measure tpd (9005) + Δtpd (9006). Capacitances include probe and jig capacitances.

AC CHARACTERISTICS (T_A = 25 C) 9005-1, 9006-1, AND 9008-1

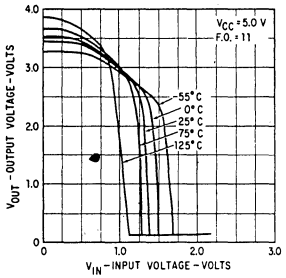
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{pd-}	3.0	15		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	18	ns	V_{CC} = 5.0 V, C_L = 15 pF, C_N = 5.0 pF
t_{pd-}	3.0	13		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−3.0	5.0	ns	9006 only
Δt_{pd-}	−3.0	5.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

AC CHARACTERISTICS (T_A = 25 C) 9005-5, 9006-6, AND 9008-5

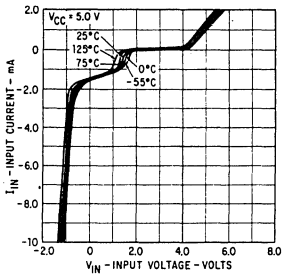
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	12	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{pd-}	3.0	14		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, C_N = 5.0 pF
t_{pd-}	3.0	12		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−2.0	4.0	ns	9006 only
Δt_{pd-}	−2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS
(EXTENDABLE GATES*)

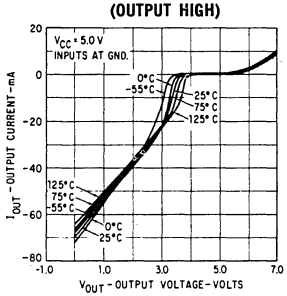
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



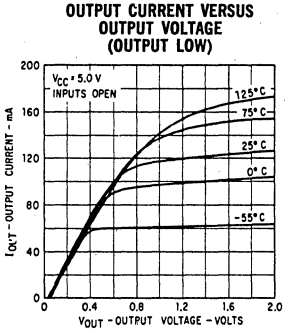
INPUT CURRENT VERSUS INPUT VOLTAGE

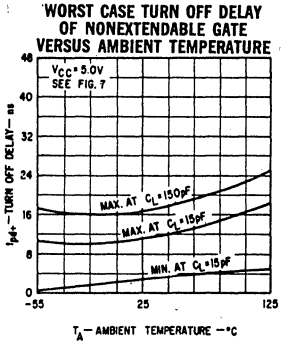


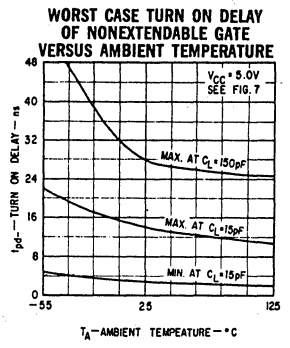
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

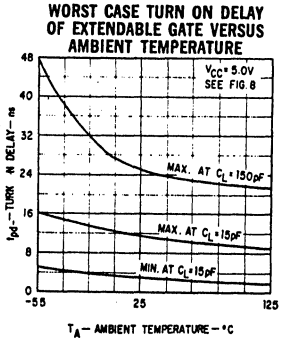


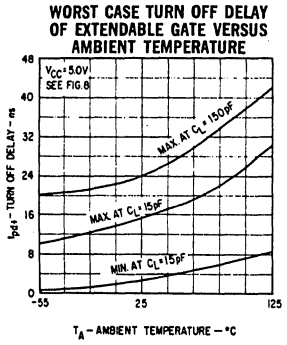
9005–1. 9006–1 AND 9008–1











J-K FLIP-FLOPS — 9000, 9001, DUAL J-K FLIP-FLOPS — 9020, 9022

The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master-slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to further engance the noise immunity.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequency of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RD dlip-dlop. These additional "don't care" conditons will, in most cases, reduce the amount of gating elements required to implement the input function.

The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

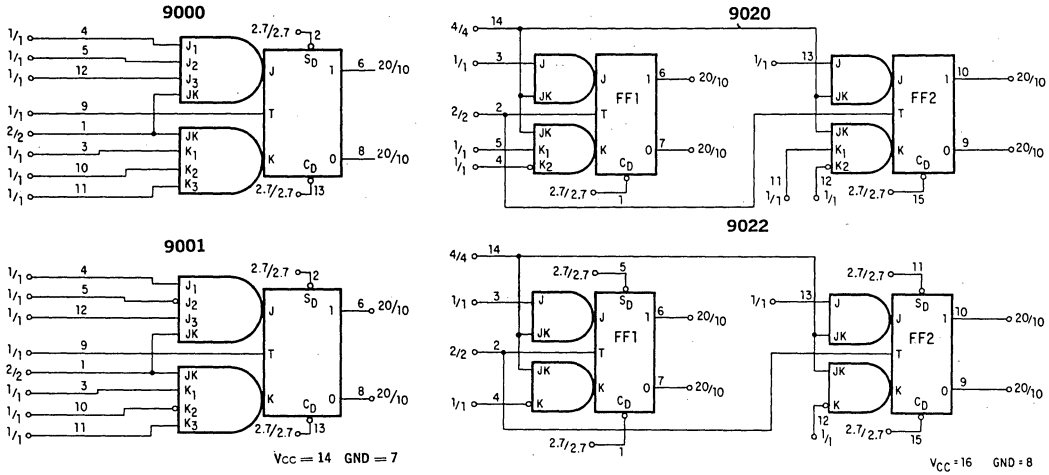
Data is accepted by the master while the clock is in the low state. Refer to the truth table for definition of "ONE" and "ZERO" data. Transfer from the master to the slave occurs on the low to high transition of the clock. When the clock is high, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applicaitons. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line, if the load exceeds the F.O. capability of the 9009 buffer.

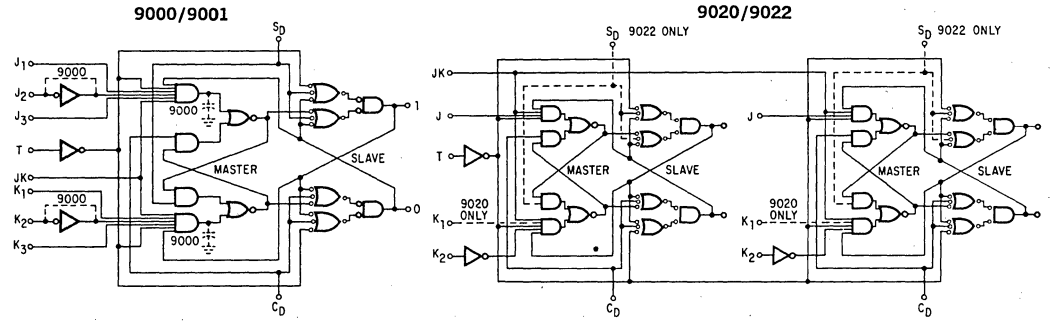
The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020,

which because of a logic trade-off has only clear inputs. The set or clear pin being low absolutely guarantees that one input will be high, but if opposing data is present at the synchronous inputs and the flip-flop if clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the low output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

LOGIC DIAGRAMS AND LOADING FACTORS



FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a low-to-high transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that that input does not go high at any time while the clock is low.

The H* symbol in the J and K input column is defined as meaning that the input has been high at some time while the clock was low.

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

UNUSED INPUTS

The 9001, 9020 and 9022 all have active level low synchronous inputs. When not in use they must be grounded. All other unused inputs including asynchronous should be tied high for maximum operating speed. Use one of the methods recommended on Page 3.

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022

($T_A = -55$ C to 125 C, $V_{CC} = 5.0$ V 10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS & COMMENTS	
		−55°C		25°C		125°C				
		MIN.	MAX.	MIN.	TYP.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7	2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -1.2$ mA	
V_{OL}	Output Low Voltage		0.4		0.21		0.4	Volts	$V_{CC} = 4.5$ V, $I_{OL} = 12.4$ mA $V_{CC} = 5.5$ V, $I_{OL} = 16.0$ mA	
V_{IH}	Input High Voltage	2.0		1.7		1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8		0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14		60 120 240 160	μA	$V_{CC} = 5.5$ V $V_R = 4.5$ V Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.1 −2.2 −4.4 −2.97		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.5$ V	$V_F = 0.4$ V 5.5 V Gnd on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.24 −2.48 −4.96 −3.35		−0.87 −1.74 −3.48 −2.35		−1.24 −2.48 −4.96 −3.35	mA	$V_{CC} = 4.5$ V	
I_{PD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		24 28 27		13 14 14		24 28 27	mA	S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0$ V

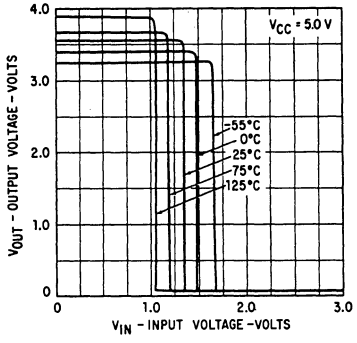
Series ITT9000-1, ITT9000-5
HIGH SPEED TTL

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022
($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0V$ 5%)

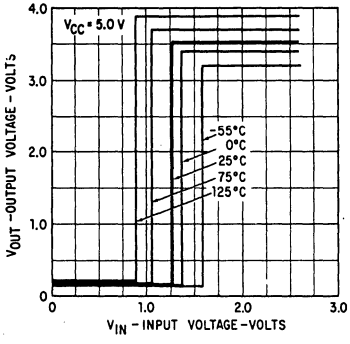
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75$ V, $I_{OH} = -1.2$ mA	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75$ V, $I_{OL} = 14.1$ mA $V_{CC} = 5.25$ V, $I_{OL} = 16$ mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14	60 120 240 160		60 120 240 160	μA	VCC = 5.25 V, $V_R = 4.5$ V Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.0 −2.0 −4.0 −2.7	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.25$ V	$V_F = 0.45$ V 5.25 V on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.41 −2.82 −5.64 −3.78		−0.94 −1.88 −3.76 −2.54	−1.41 −2.82 −5.64 −3.78		−1.41 −2.82 −5.64 −3.78	mA	$V_{CC} = 4.75$ V	
I_{PD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		28 33 30			28 33 30		28 33 30	mA	S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0$ V

TYPICAL INPUT-OUTPUT CHARACTERISTICS 9000, 9001, 9020 AND 9022

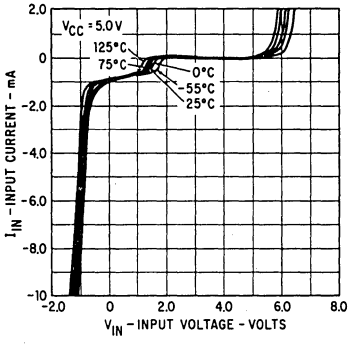
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS



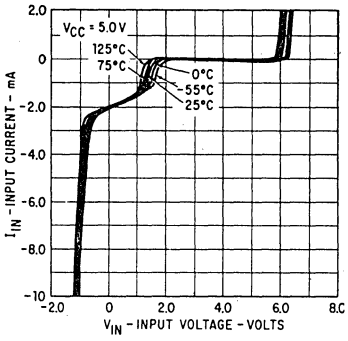
CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



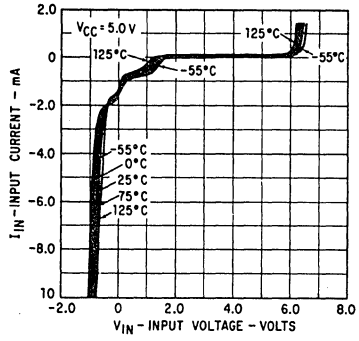
INPUT CURRENT VERSUS INPUT VOLTAGE 9004



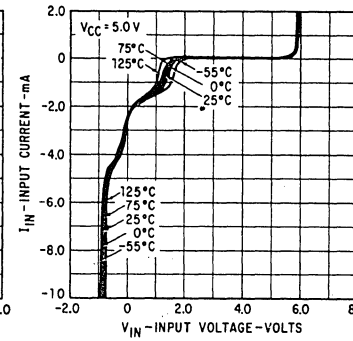
INPUT CURRENT VERSUS INPUT VOLTAGE 9009



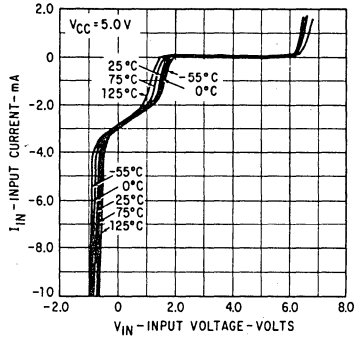
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001



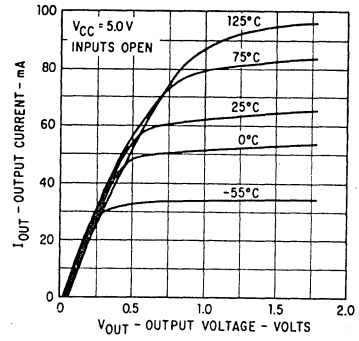
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022



INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS — ALL FLIP-FLOPS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

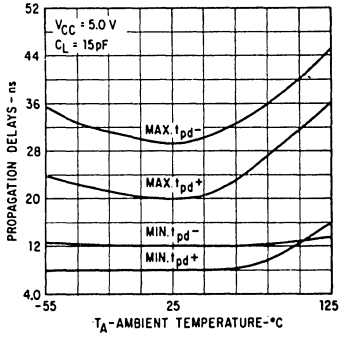


SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = C_l = 15$ pF of all flip-flops unless otherwise noted)

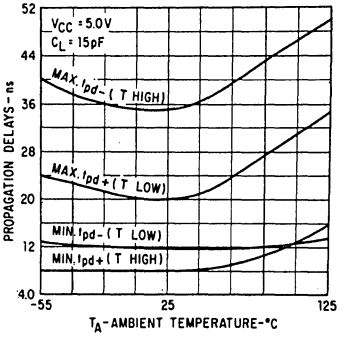
	CHARACTERISTICS			MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock-to-Output				12	20	ns	10, 11, 12
	S_D or C_D-to-Otuput				12	20	ns	10, 11. 12
t_{pd-}	Clock-to-Output				20	30	ns	10, 11, 12
	S_D or C_D-to-Output				25	35	ns	10, 11. 12
t_{set-up}	J, K or JK		9000 Only	30* 35	22		ns	10, 12
	Data Entry			10* 12	8.0		ns	10, 11, 12
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12		ns	10, 11, 12
$t_{release}$	J, K or JK		9000 Only		18	12	ns	10, 12
	Data Entry				7.0	1.0	ns	10, 11, 12
	$\overline{J}$ or $\overline{K}$ Data Entry				11	4.0	ns	10, 11, 12
Pulse Widths	Clock	9000 Only	Positive		20		ns	10, 12
			Negative		25		ns	10, 12
			Positive		8.0		ns	10, 11, 12
			Negative		10		ns	10, 11, 12
	S_D or C_D		Negative		25		ns	10, 11, 12
Toggle Frequency			9000 Only		20		MHz	10, 12
					50		MHz	10, 11, 12

*For —1 types

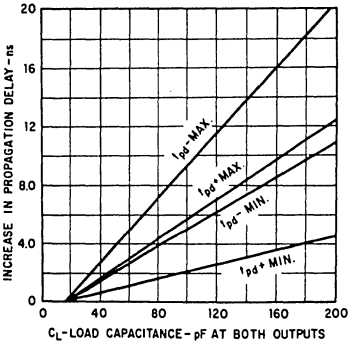
MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE TO OUTPUT



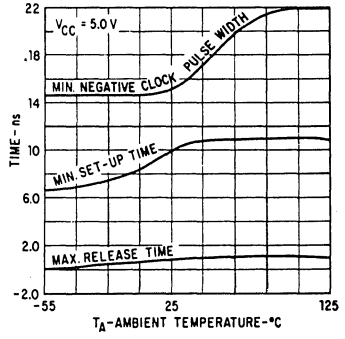
MAX. AND MIN. PROPAGATION DELAYS VERSUS TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS



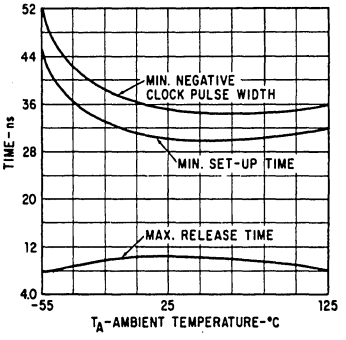
INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE



9001-9020-9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE



9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TEST CIRCUITS

Fig. 10 9000/9001

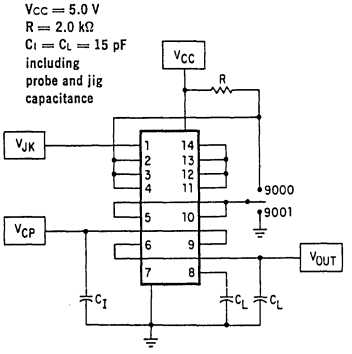
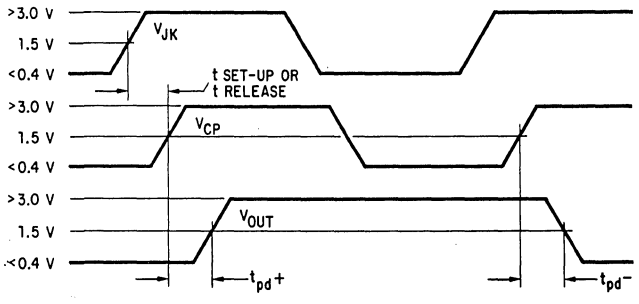
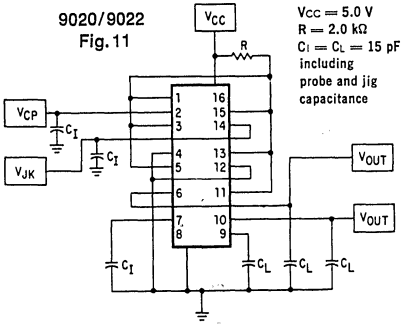


Figure 12 WAVEFORMS



9020/9022
Fig. 11



SWITCHING TEST NOTES

tpd +and tpd—

1. V_{JK} should be kept at the high logic level when performing tpd tests.
2. Drive the clock pulse input with a suitable pulse source. tpd +and tpd— delays are as defined in the waveforms.

tset-up

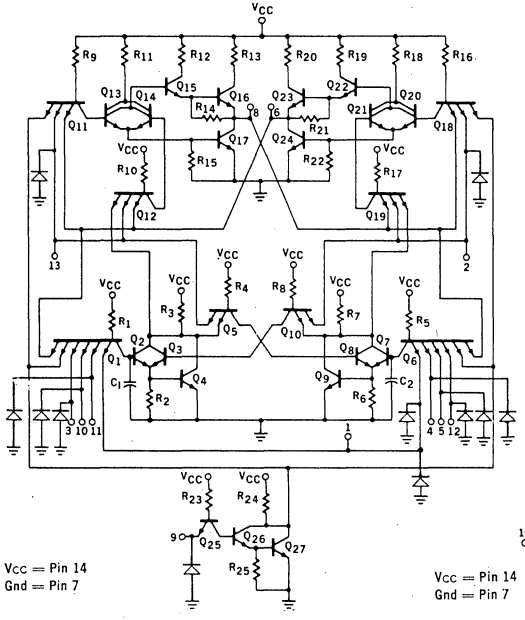
1. tset-up is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.
2. The test for tset-up is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the tset-up minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the tset-up test will remain at a static logic level (no switching will occur).

trelease

1. trelease is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.
2. The test for trelease is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the trelease maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the trelease test will exhibit pulses instead of static levels.

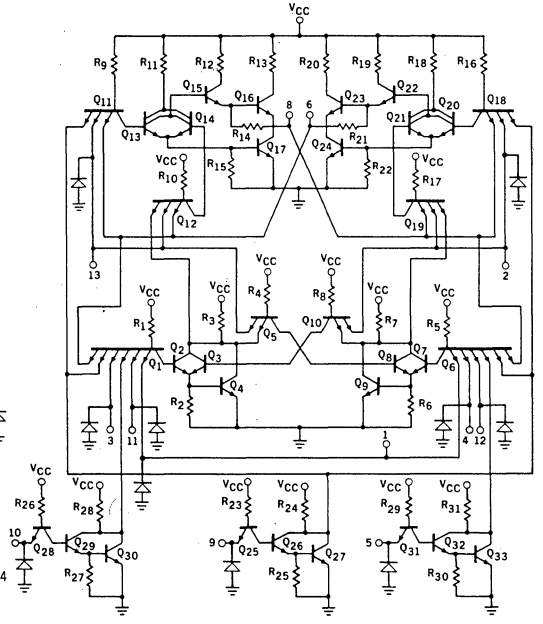
9000 SCHEMATIC DIAGRAM

For resistor values,see page 16

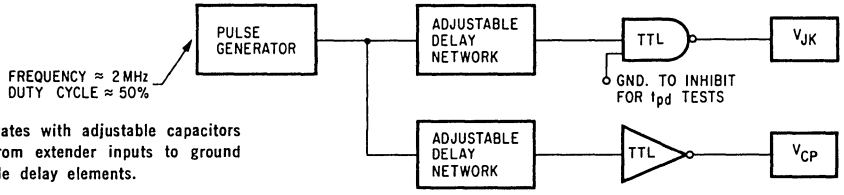


9001 SCHEMATIC DIAGRAM

For resistor values,see page 16

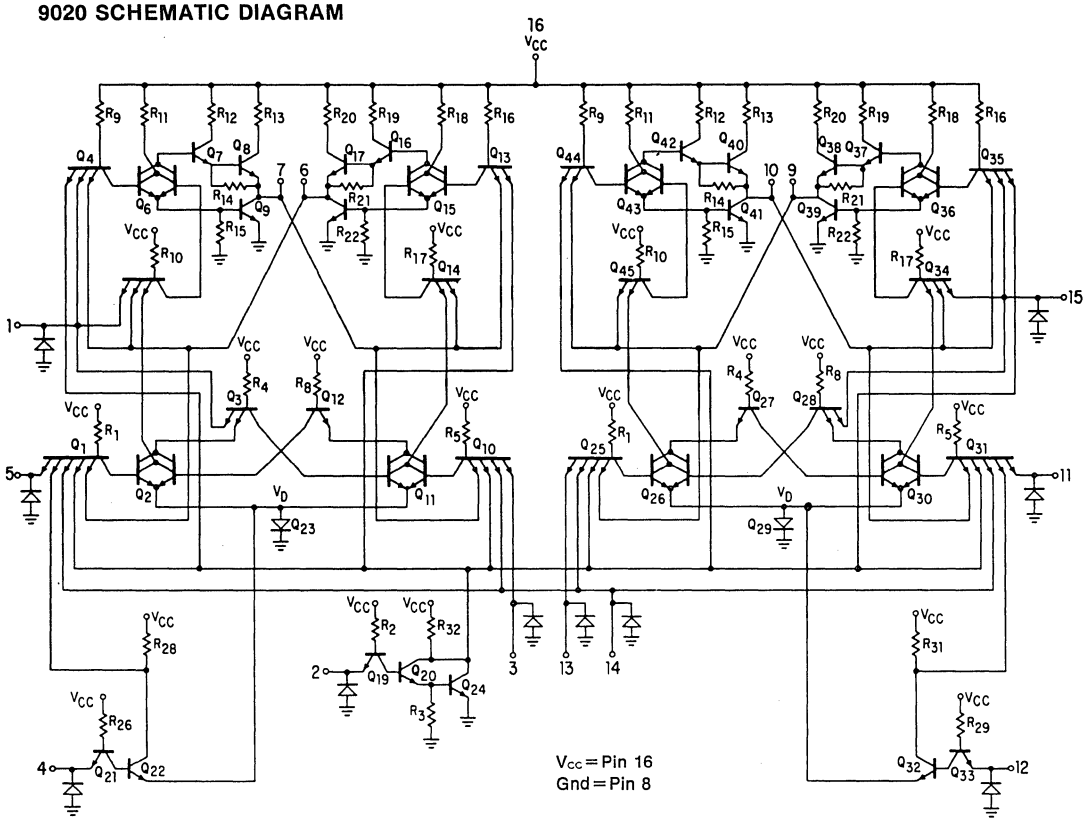


RECOMMENDED INPUT PULSE SOURCES



DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

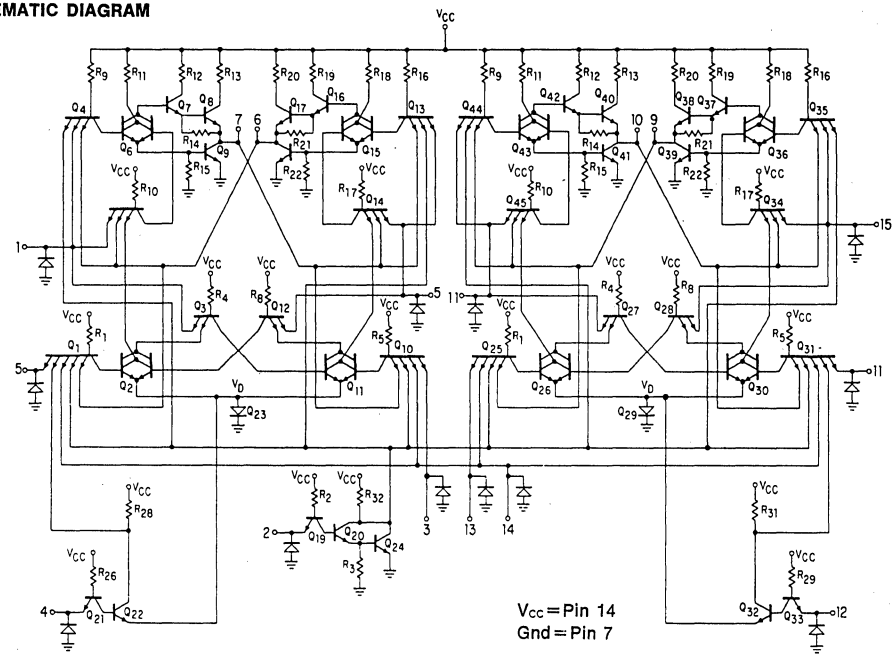
9020 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES [ALL FLIP-FLOPS]

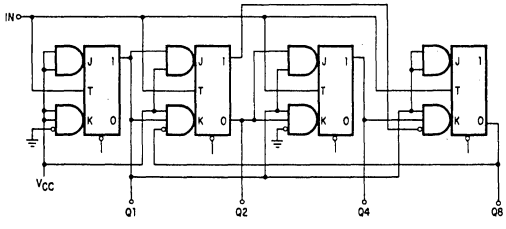
R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

9022 SCHEMATIC DIAGRAM



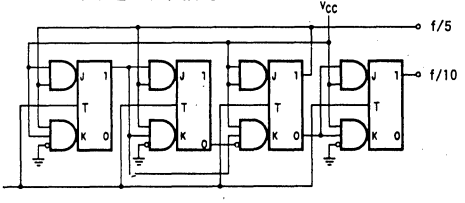
APPLICATIONS

SYNCHRONOUS BCD COUNTER



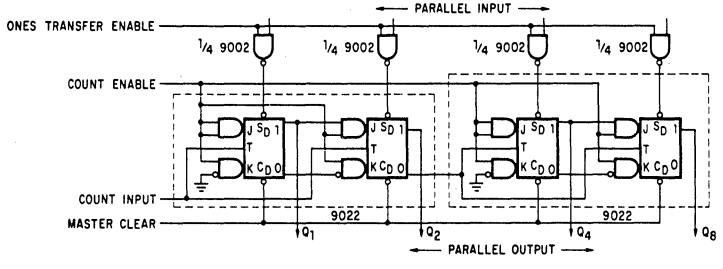
Two TTL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR



Binary counter using synchronous 2 bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

ITT SEMICONDUCTORS

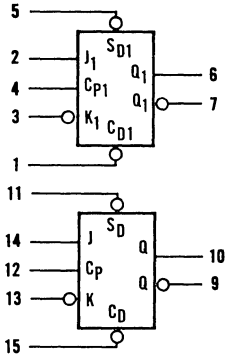
Packages: 16 lead DIP and Flat Packages

DUAL JK [OR D] FLIP-FLOP

- Dual Rank Type Circuit
- Separate Clocks
- Separate Asynchronous Set and Clear Inputs
- Low Power Dissipation
- Compatible with ITT DTL and Other TTL Families
- Input Diode Clamping
- 25 MHz Operation

The ITT9024 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by simply connecting the J and K pins together.

LOGIC SYMBOL

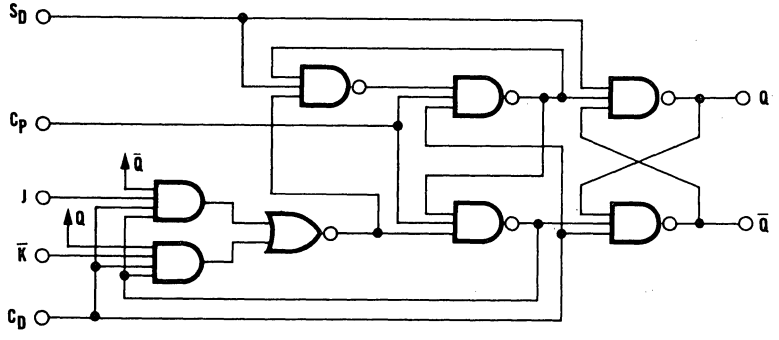


ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature .....—65 to +150	C
Temperature (Ambient Under Bias .....—55 to +125	C
Vcc Pin Potential to Ground Pin (See Note 1).....—0.5 to +8	Volts
Voltage applied to output when output is high ..0 V to + Vcc	value
Input Voltage (DC) (See Note 2) .....—0.5 to +5.5	Volts
Input Current (DC) (See Note 2).....—30 to +5	mA
Current into output when output is low.....+30	mA

Notes 1 and 2 following page

LOGIC DIAGRAM



ITT 9024

DUAL JK (OR D) FLIP-FLOP

***ELECTRICAL CHARACTERISTICS** ($T_A = -55°C$ to $125°C$, $V_{CC} = 5$ V 10%) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS AND COMMENTS
		−55°C		25°C		125°C			
		MIN.	MAX.	MIN.	TYP. MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	2.7	2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -1.2$ mA
V_{OL}	Output Low Voltage		0.4		0.2 0.4		0.4	Volts	$V_{CC} = 4.5$ V, $I_{OL} = 12.4$ mA
			0.4		0.25 0.4		0.4	Volts	$V_{CC} = 5.5$ V, $I_{OL} = 16$ mA
V_{IH}	Input High Voltage	2.0		1.7		1.4		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.8		0.9		0.8	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R	J, K Leakage Current				5.0 60		60	µA	$V_{CC} = 5.5$ V, $V_R = 4.5$ V
$2I_R$	Clock Input, S_D				10 120		120		Gnd. on other inputs
$4\ I_R$	C_D				20 240		240		
I_F	J, K Input Current		−1.6		−1.1 −1.6		−1.6	mA	$V_{CC} = 5.25$ V, $V_F = 0.4$ V
$2\ I_F$	Clock Input, S_D		−3.2		−2.2 −3.2		−3.2		4.5 V on other inputs
$3\ I_F$	C_D(Note 4)		−4.8		−3.3 −4.8		−4.8		
I_F	J, K Input Current		−1.24		−0.91 −1.24		−1.24	mA	$V_{CC} = 5.5$ V
$2\ I_F$	Clock Input, S_D		−2.48		−1.82 −2.48		−2.48		
$3\ I_F$	C_D (Note 4)		−3.72		−2.73 −3.72		−3.72		
I_{PD}	Current Drain				9.0 14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65			mA	Logic 1 Output Short Circuit

***ELECTRICAL CHARACTERISTICS** ($T_A = 0°C$ to $75°C$, $V_{CC} = 5$ V 5%) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS AND COMMENTS
		0°C		25°C		75°C			
		MIN.	MAX.	MIN.	TYPE MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.0	2.4		Volts	$V_{CC} = 4.75$ V, $I_{OH} = -1.2$ mA
V_{OL}	Output Low Voltage		0.45		0.21 0.45		0.45	Volts	$V_{CC} = 4.75$ V, $I_{OH} = 14.1$ mA
									$V_{CC} = 5.25$ V, $I_{OH} = 16$ mA
V_{IH}	Input High Voltage	1.9		1.8		1.6		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.85		0.85		0.85	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R	J, K Leakage Current				5.0 60			uA	$V_{CC} = 5.25$ V, $V_R = 4.5$ V
$2I_R$	Clock Input, S_D				10 120				Gnd. on other inputs
$4\ I_R$	C_D				20 240				
I_F	J, K Input Current		−1.6		−1.0 −.16		−1.6	mA	$V_{CC} = 5.25$ V $V_F = 0.4$ V
$2\ I_F$	Clock Input, S_D		−3.2		−2.0 −3.2		−3.2		4.5 V on other
$3\ I_F$	C_D (note 4)		−4.8		−3.0 −4.8		−4.8		inputs
I_F	J, K Input Current		−1.41		−0.94 −1.41		−1.41	mA	$V_{CC} = 4.75$ V.
$2\ I_F$	Clock Input, S_D		−2.82		−1.88 −2.82		−2.82		
$3\ I_F$	C_D(Note 4)		−4.23		−2.82 −4.23		−4.23		
I_{PD}	Current Drain				9.0 14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65			mA	Logic 1 Output Short Circuit

(1) The maximum VCC value of 8.0 volts is not the primary factor in determining the maximum VCC which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 VBE below the VCC voltage, so the primary limit on the VCC is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system VCC to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

(3) Positive current is into device and negative current is out of device.

(4) Denotes maximum current under normal operation. These currents may increase up to 4 IF if J, K=Logic 1 and SD=Logic 0.

TRUTH TABLES

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

L = Low Logic Level, H = High Logic Level

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOADING RULES

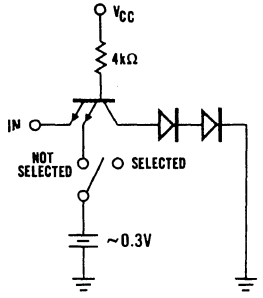
INPUT	LOADING
J and $\overline{K}$	1 U.L.
C_P and S_D	2 U.L.
C_D* (Note 4)	3 U.L.

OUTPUTS	FAN OUT	
	High State	Low State
Q	20	10
$\overline{Q}$	20	10

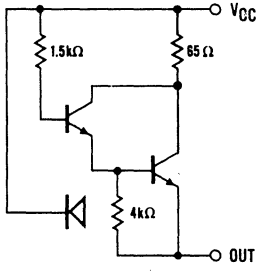
1 U.L. = 1 TTL Unit Load as defined by the entries I_R and I_F tables.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

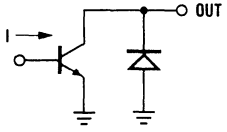
EQUIVALENT INPUT CIRCUIT



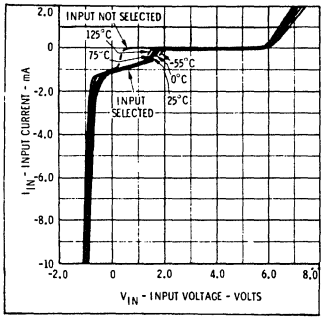
OUTPUT HIGH EQUIVALENT CIRCUIT



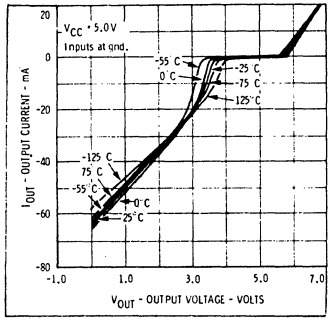
OUTPUT LOW EQUIVALENT CIRCUIT



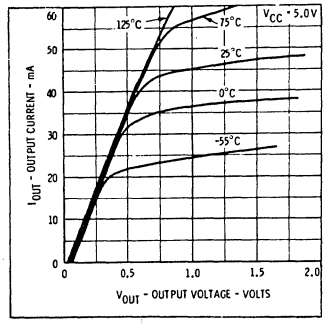
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



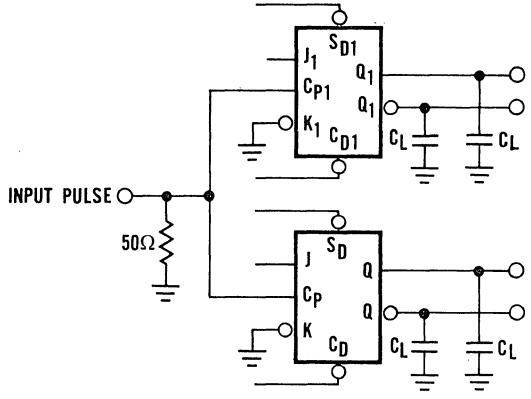
ITT 9024

DUAL JK (OR D) FLIP-FLOP

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF)

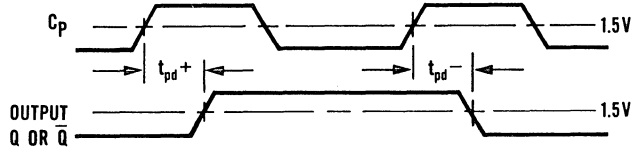
SYMBOL	CHARACTERISTIC	LIMITS 25°C MIN.	TYP.	MAX.	UNITS	COMMENTS
t_{pd+}	J, K, D		25		ns	Each Flip-Flop
t_{pd-}	J, K, D		20		ns	
$t_{release}$			2.0		ns	
$t_{set\text{-}up}$			15		ns	
t_{pd+}	S_D to Q		10		ns	
t_{pd-}	S_D to Q		25		ns	
	Toggle Frequency		25		MHz	

SWITCHING TEST CIRCUIT



C_L includes probe and jig capacitance

WAVEFORMS



MSI 4-BIT SHIFT REGISTER

The ITT9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTL for high speed and high fanout capability, and is compatible with DTL, and TTL digital integrated circuits.

- **15 MHz Shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16 pin Dual In-Line package**
- **Input diode clamping**

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65°C to +150	°C
Temperature (Ambient) Under Bias ...—55°C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5V to +7	Volts
Voltage Applied to Outputs for high output state .....—0.5V to +Vcc	value
Input Voltage (D.C.) .....—0.5V to +5.5	Volts

LOGIC SYMBOL

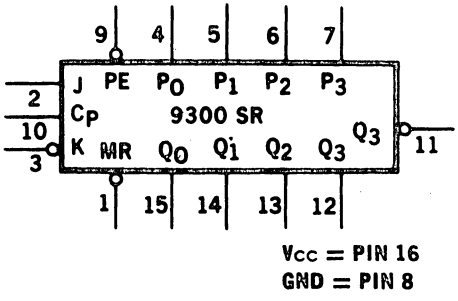


Figure 1

FUNCTIONAL DESCRIPTION

The logic symbol of Figure 1 provides an indication of the functional characteristics of the ITT9300 four bit shift register. Several special logical features of the ITT9300 design which provide a high degree of general usefulness are described below:

1. A JK input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the K input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or K inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flop occurs after the low to high transition of the clock input.

4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

TABLE I — TRUTH TABLE FOR SERIAL ENTRY

(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES
[1 U.L. = 1 TTL Gate Input Load]

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	4 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

ELECTRICAL CHARACTERISTICS [ITT9300-1X]

(T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	V_{CC} = 5.5 V V_{CC} = 4.5 V, V_F = 0.4 V
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V

ELECTRICAL CHARACTERISTICS [ITT 9300-5X]

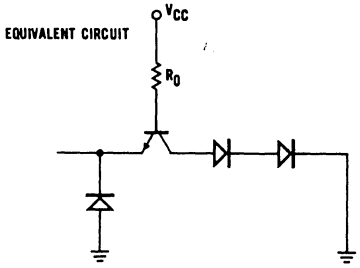
(T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 9.6 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	V_{CC} = 4.75 V, I_{OL} = 8.5 mA Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	V_{CC} = 5.25 V V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V

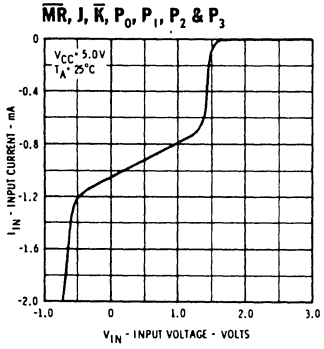
*For CP and $\overline{PE}$ input currents, use load factors in Table II

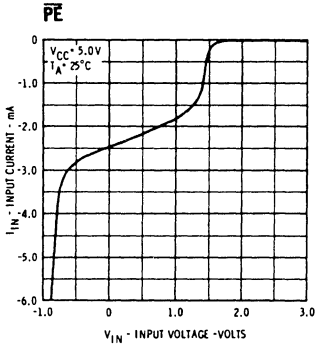
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

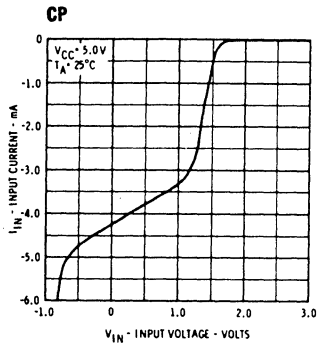
INPUTS



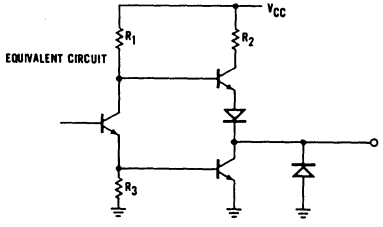
INPUT CURRENT VS INPUT VOLTAGE



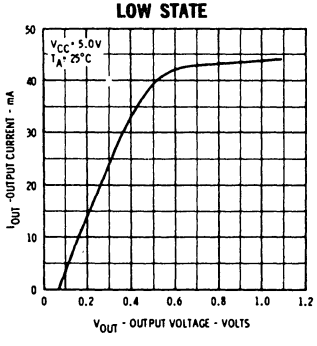


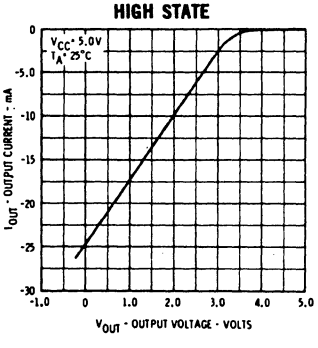


OUTPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE





SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 4 & 6a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 4 & 6c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 6a & 6b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET-UP TIME: ts is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.
RELEASE TIME: tr is defined as the maximum time allowed for the logic evel to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.
RECOVERY TIME FOR MR: trec (MR) is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Figure 2

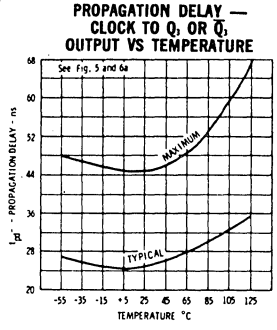
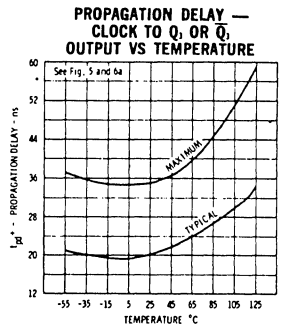
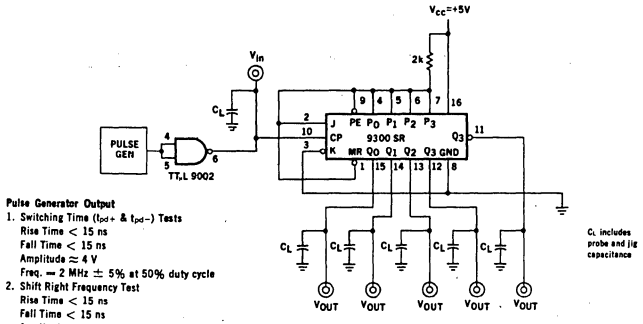


Figure 3





Pulse Generator Output
1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

Figure 4 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Figure 6a

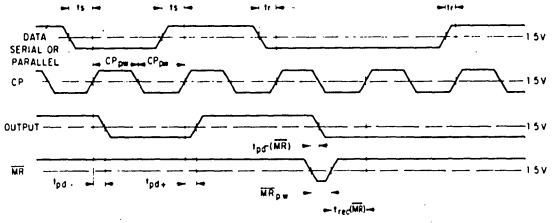


Figure 6b

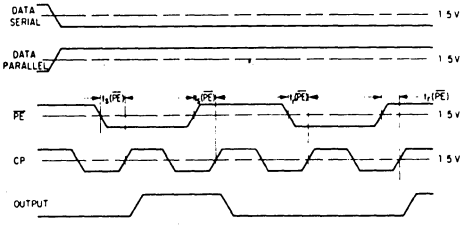


Figure 6c

VOUT Frequency = ½ X VIN Frequency

Figure 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The ITT9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the ITT9300 is illustrated by the applications shown below.

Figure 7 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

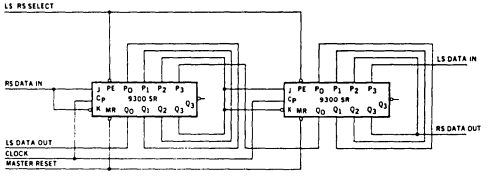
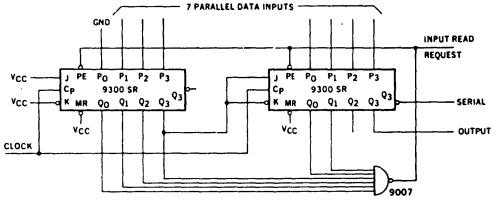


Figure 8 — SEVEN BIT PARALLEL to SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.



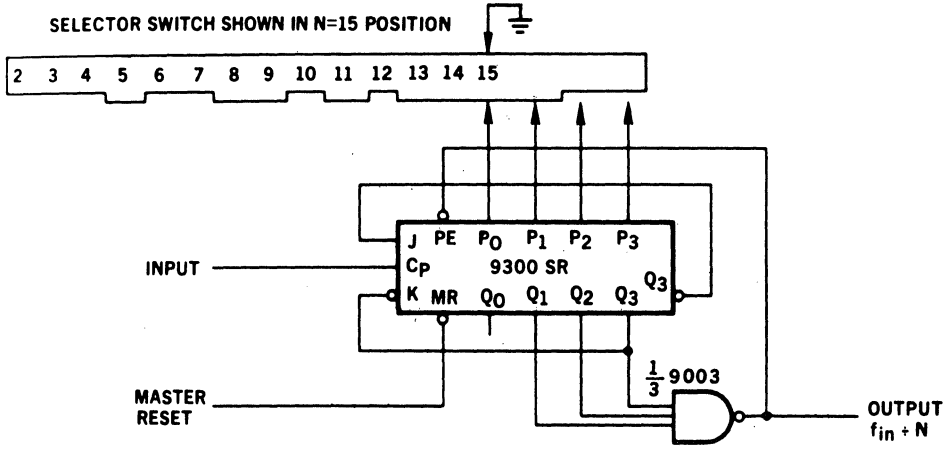
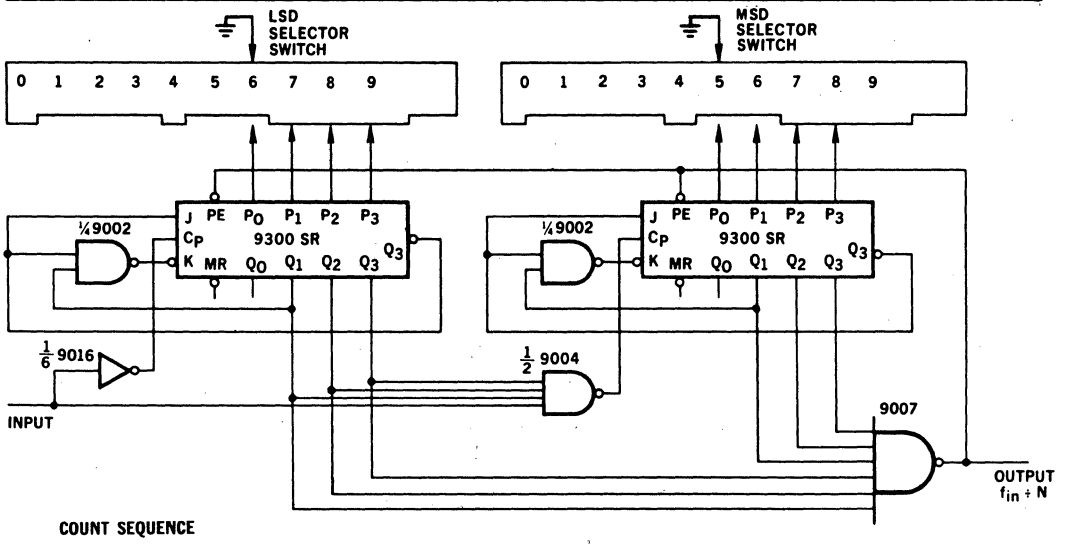


Figure 9 — DIVIDE BY N COUNTER FOR N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT SEQUENCE

9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Figure 10 — TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switched are showing 56, therefore the circuit will divide by 57 with this setting.

MSI ONE-OF-TEN DECODER

The ITT9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive output. The circuit uses TTL for high speed and high fan out capability, and is compatible with DTL, and TTL digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16-pin Dual -In-Line package**
- **Input clamp diodes limit high speed line termination effects**

TABLE I — TRUTH TABLE

A0	A1	A2	A3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65°C to +150	°C
Temperature (Ambient) Under Bias ...—55°C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5V to +7	Volts
Voltage Applied to Outputs for high voltage state .....—0.5V to +Vcc	value
Input Voltage (D.C.) .....—0.5V to +5.5	Volts

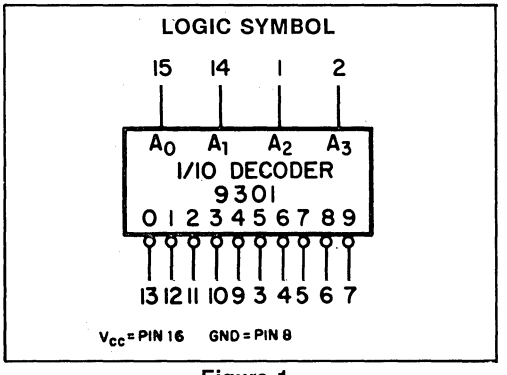


Figure 1

FUNCTIONAL DESCRIPTION

The ITT9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements.

The logic design of the ITT9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A3 input produces a useful inhibit function when the ITT9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the ITT9301 are shown in Table I and Table II.

ELECTRICAL CHARACTERISTICS [ITT9301-1X] ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC}=4.5$ V, $I_{OH}=-0.6$ mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC}=4.5$ V, $I_{OL}=12.4$ mA $V_{CC}=5.5$ V, $I_{OL}=16.0$ mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			.09		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC}=5.5$ V, $V_F=0.4$ V
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC}=4.5$ V, $V_F=0.4$ V
I_R	Input Leakage Current				15	60		60	μA	$V_{CC}=5.5$ V, $V_R=4.5$ V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC}=5.0$ V
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L=15$ pF See Fig. 8

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC}=4.75$ V, $I_{OH}=-0.6$ mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC}=4.75$ V, $I_{OL}=14.1$ mA $V_{CC}=5.25$ V, $I_{OL}=16.0$ mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC}=5.25$ V, $V_F=0.45$ V
			−1.41		−0.9	−1.41		−1.41	mA	$V_{CC}=4.75$ V, $V_F=0.45$ V
I_R	Input Leakage Current				15	60		60	μA	$V_{CC}=5.25$ V, $V_R=4.5$ V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC}=5.0$ V
t_{pd-}	Turn On Delay				20	30			ns	$C_L=15$ pF See Fig. 8

TABLE II — LOADING RULES
[1 U.L. = TTL Gate Input Load]

INPUTS	LOADING	OUTPUTS	FANOUT
A0, A1, A2 & A3	1 U.L.	0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

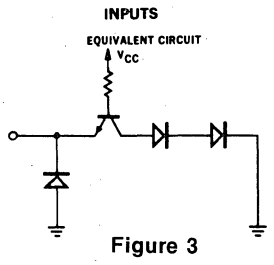
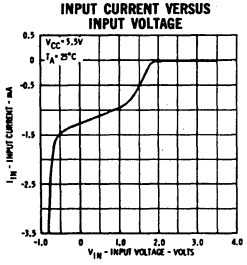


Figure 3



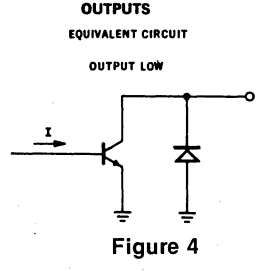
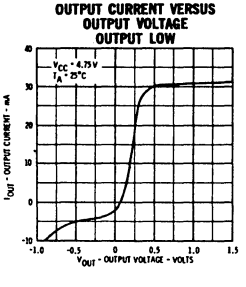


Figure 4



TYPICAL INPUT AND OUTPUT CHARACTERISTICS (continued)

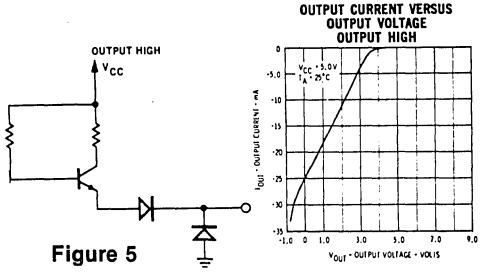


Figure 5

SWITCHING PERFORMANCE

Figure 6

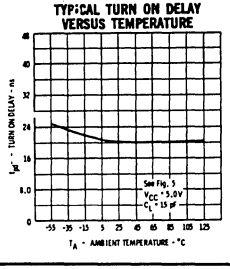
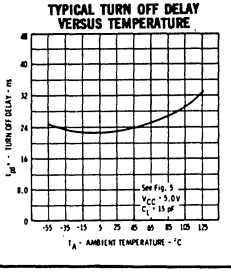
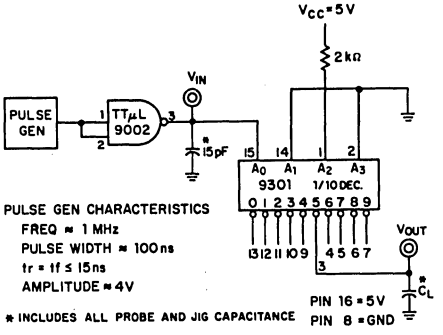


Figure 7



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



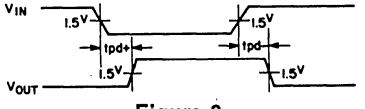


Figure 8

APPLICATIONS — The ITT9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the ITT9301 is indicated by its use in the following applications.

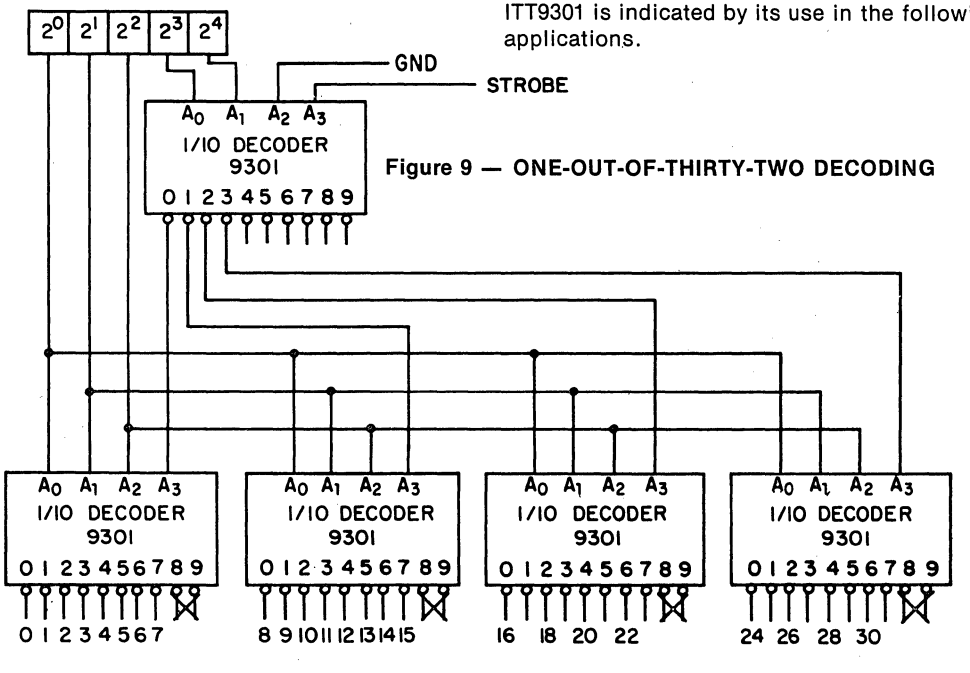
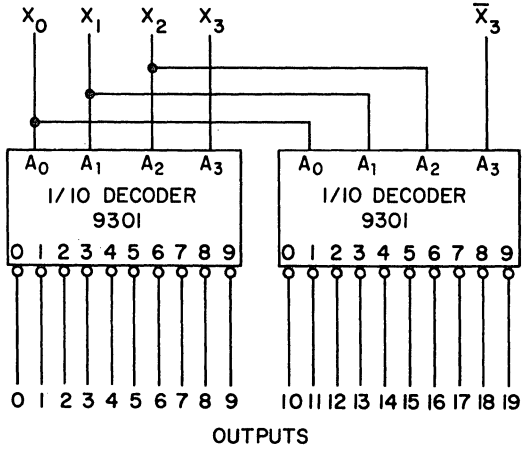


Figure 9 — ONE-OUT-OF-THIRTY-TWO DECODING

BCD CODE

Figure 10 — DECODE ANY BCD CODE



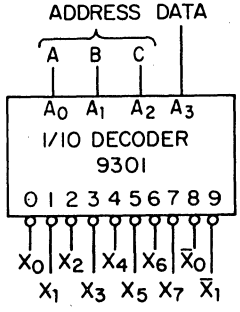
DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

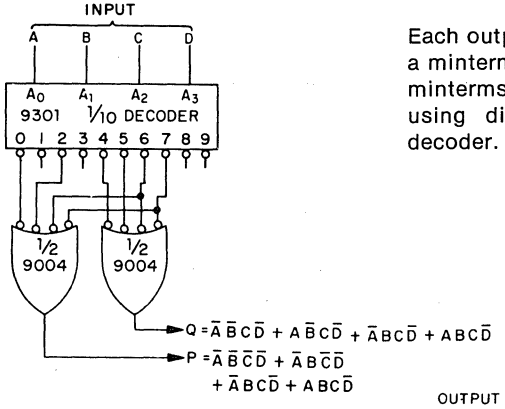
Figure 11 — DIGITAL DEMULTIPLEXER

Data may be routed from a source to any of 8 outputs by addressing that output. All non-addressed output remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.



ADDRESS A	B	C	OUTPUT LINE
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7



Each output of the ITT9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one ITT9301 decoder.

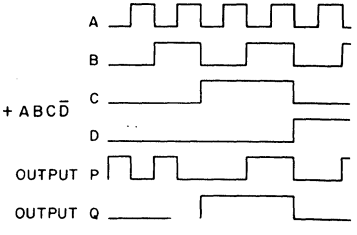


Figure 12 — MINTERM GENERATOR

MSI DUAL FULL ADDER

- Multi-function capability
- 8ns carry propagation delay
- Complementary inputs and outputs available
- Typical power dissipation of 150mW
- The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families
- All ceramic HERMETIC 16-pin Dual In-Line package
- Input clamp diodes limit high speed termination effects

The ITT9304 consists of two indepenent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTL for high speed, high fanout operation and is compatible with DTL, and TTL digital integrated circuits.

LOGIC SYMBOL

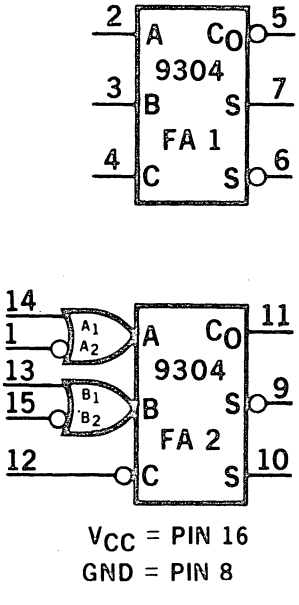


Figure 1

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65°C to +150	°C
Temperature (Ambient) Under Bias .....—55°C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5V to +7	Volts
Voltage Applied to Outputs for high output state .....—0.5V to +Vcc	value
Input Voltage (D.C.) —0.5V to +5.5	Volts

FUNCTIONAL DESCRIPTION

The ITT9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sums when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the ITT9304 are shown in Table I and Table II.

ELECTRICAL CHARACTERISTICS (ITT9304-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4$ mA (Pins 7 & 9) $I_{OL} = 11.2$ mA (Pins 6 & 10) $I_{OL} = 8.7$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F $4\ I_F$	Input Load Current Input Load Current		−1.6 −6.4		−1.1 −4.4	−1.6 −6.4		−1.6 −6.4	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
I_F $4\ I_F$	Input Load Current Input Load Current		−1.24 −4.96		−0.97 −3.88	−1.24 −4.96		−1.24 −4.96	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
I_R $4\ I_R$	Input Leakage Current Input Leakage Current				15 60	60 240		60 240	µA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Ground on other inputs
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$ $C_L = 15$ pF See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_i to S				28	40			ns	
t_{pd-}	A_i to S				25	35			ns	

ELECTRICAL CHARACTERISTICS (ITT9304-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1$ mA (Pins 7 & 9) $I_{OL} = 12.7$ mA (Pins 6 & 10) $I_{OL} = 9.85$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F $4\ I_F$	Input Load Current Input Load Current		−1.6 −6.4		−1.0 −4.0	−1.6 −6.4		−1.6 −6.4	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
I_F $4\ I_F$	Input Load Current Input Load Current		−1.41 −5.64		−0.9 −3.6	−1.41 −5.64		−1.41 −5.64	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
I_R $4\ I_R$	Input Leakage Current Input Leakage Current				15 60	60 240		60 240	µA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Ground on other inputs
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$ $C_L = 15$ pF See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_i to S				28	45			ns	
t_{pd-}	A_i to S				25	40			ns	

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

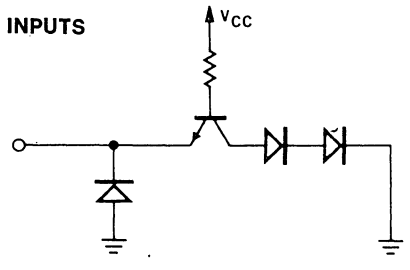
H = High Voltage Level L = Low Voltage Level

TABLE II — LOADING RULES
[1 U.L. = TTL Gate Input Unit Load]

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

EQUIVALENT CIRCUIT



INPUT CURRENT VS INPUT VOLTAGE

PINS 1, 2, 3, 4, 12, 15

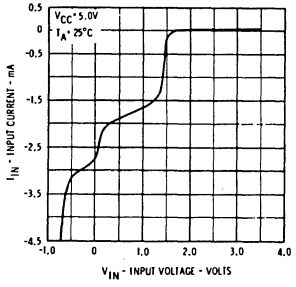


FIG. 4

PINS 13, 14

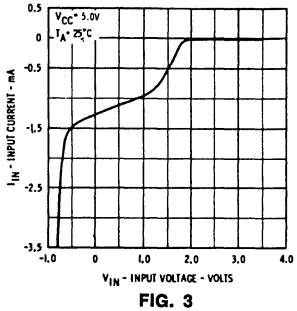
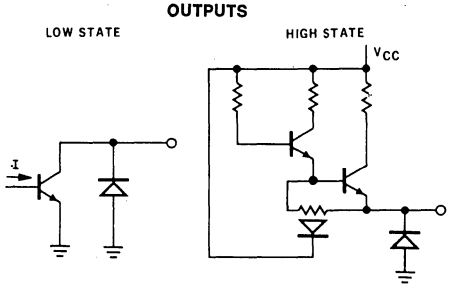


FIG. 3



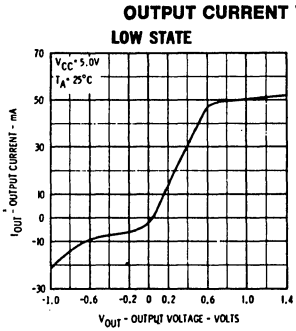


FIG. 5

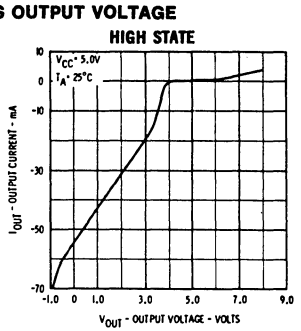


FIG. 6

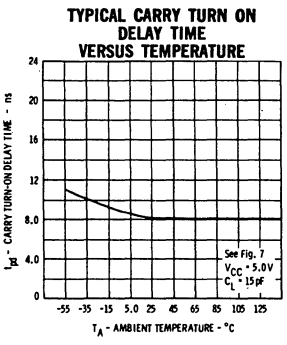


Fig. 7

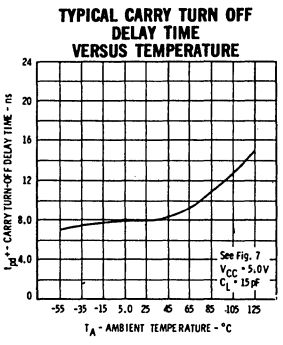
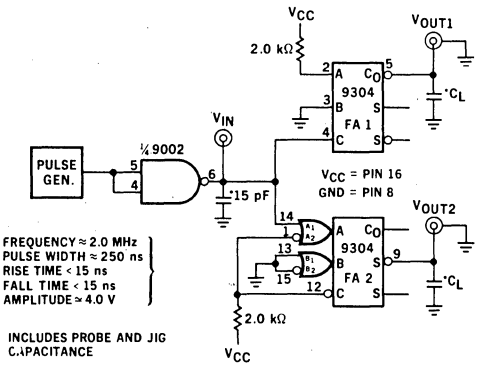


Fig. 8



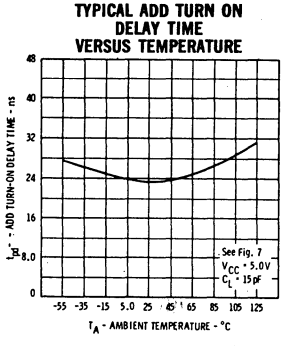


Fig. 9

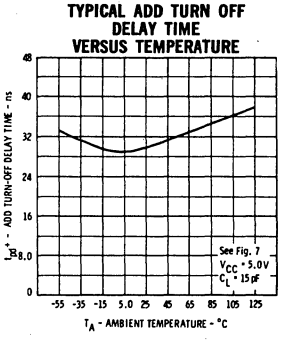


Fig. 10

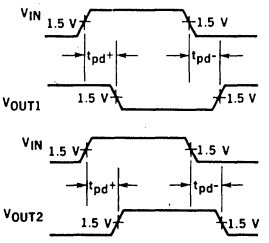


Fig. 11 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The ITT9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunction capabilities of the ITT9304 dual adder can be seen from reference to the applications shown.

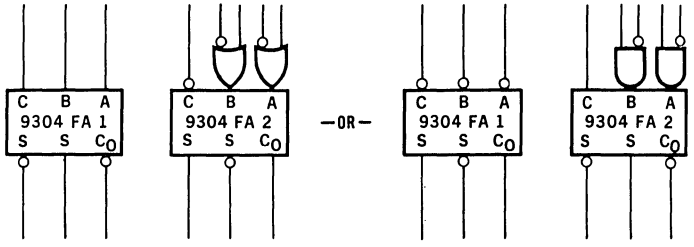


Figure 12 — FUNCTIONAL BLOCK REPRESENTATION

The principal of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

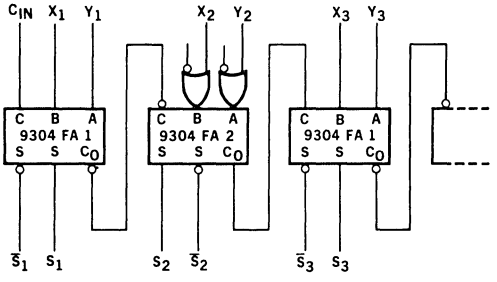


Figure 13 — RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate delay is incurred at each stage allowing a typical addition speed of (N + 1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

PROPAGATION DELAY AND PACKAGE COUNT AGAINST WORD LENGTH FOR RIPPLE CARRY ADDITION

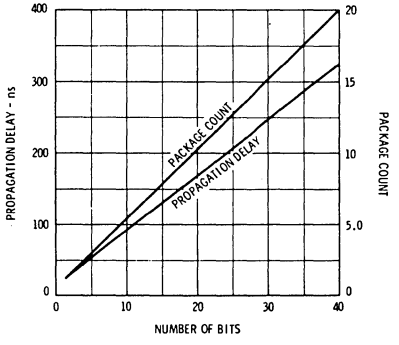


Figure 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

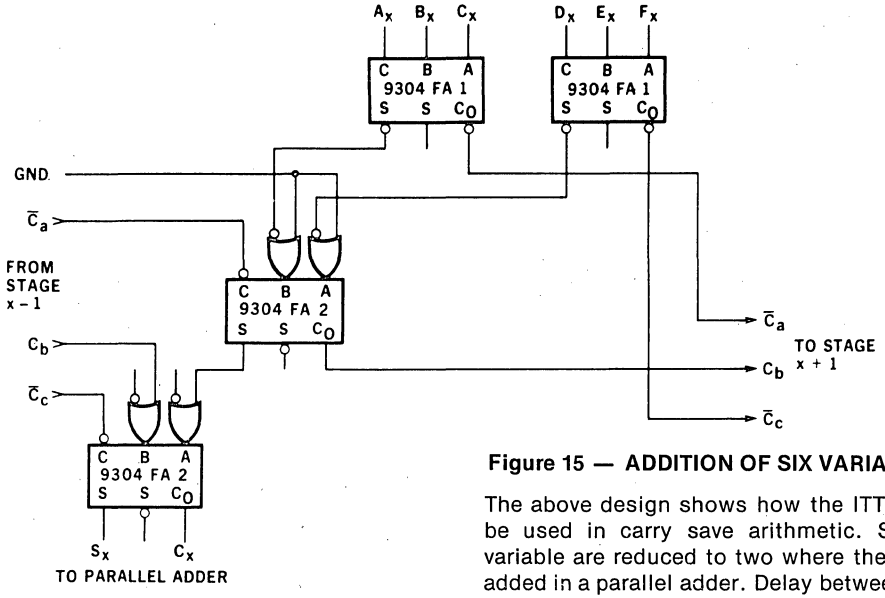


Figure 15 — ADDITION OF SIX VARIABLES

The above design shows how the ITT9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

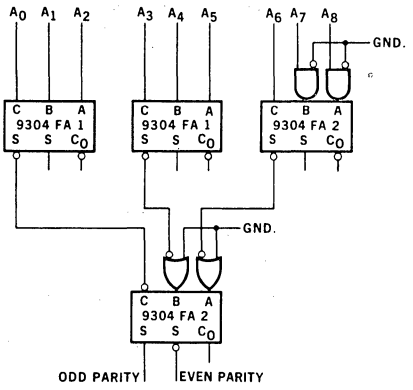


Figure 16 — BYTE PARITY GENERATION OR CHECKING

The ITT9304 can be used for parity checking or generating. The above design uses 2 ITT9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

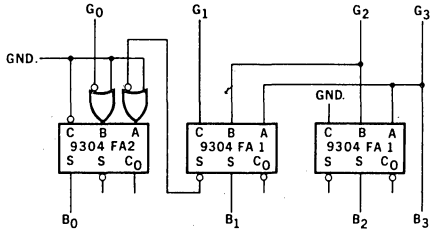


Figure 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

SEMICONDUCTORS

MSI DUAL FOUR-BIT LATCH

Active Level Low Enable Gate Inputs
Overriding Master Reset
25 ns Through Delay
The Input/Output Characteristics Provide Direct Interfacing With ITT DTL and TTL
Input Clamp Diodes Limit High Speed Termination Effects.

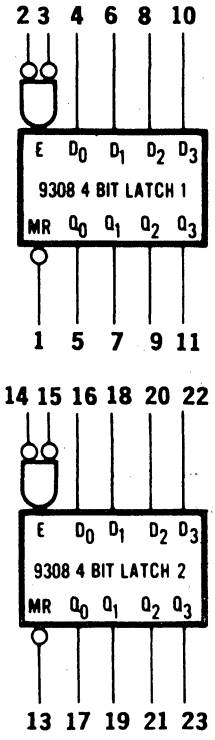
The MSI ITT9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The ITT9308 uses TTL technology. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Conditions	Units
Storage Temperature .....—65 to +150	C
Temperature (Ambient) Under Bias .....—55 to +155	C
Vcc Pin Potential to Ground Pin .....—0.5 to +7	Volts
Input Voltage (D.C.))see Note 1) .....—0.5 to +5.5	Volts
Input Current (D.C.) (See Note 1) .....—30 to +5	mA
Voltage Applied to Outputs (Output High) ..—0.5 to +Vcc	value
Output Current (D.C.) (Output Low) .....+30	mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

Description of Latch Operation — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 14.4\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 11.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_o, E_i and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_o, E_i and MR Inputs				10	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

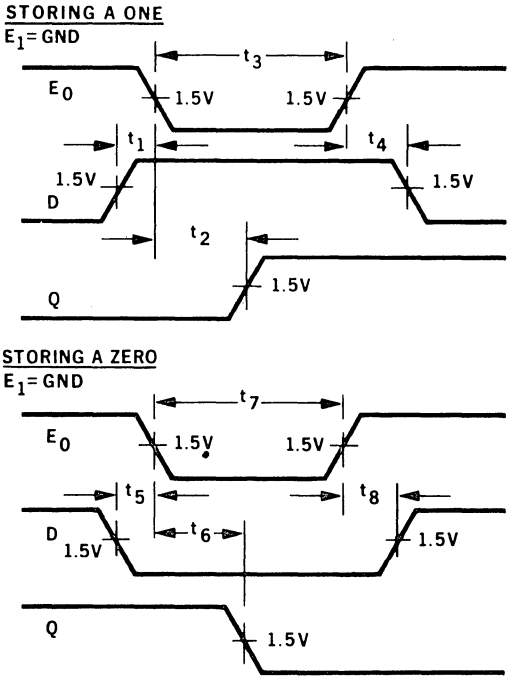
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OUT} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OUT} = 14.4\ mA$ $V_{CC} = 4.75\ V$, $I_{OUT} = 12.7\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_o, E_i and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_o, E_i and MR Inputs				10	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

NOTES:
1. Units are pulse tested.
2. Output Voltages are guaranteed for either the input enabled or input diabled case.
3. This current is measured at VIN = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at VIN = 0.4 V is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4)			
		MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

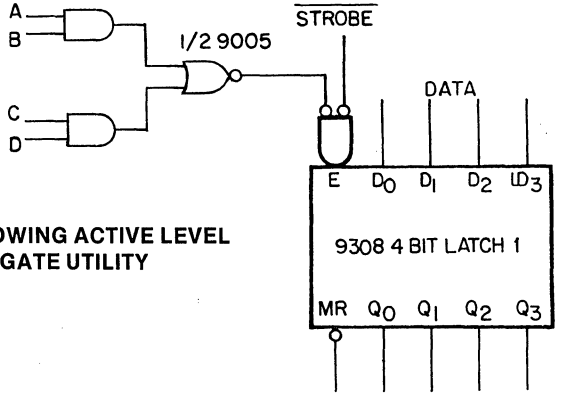
NOTE 4: Limits indicated by X will be shown on final data sheets.

	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3 MR, E_0, E_1	1.5 1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

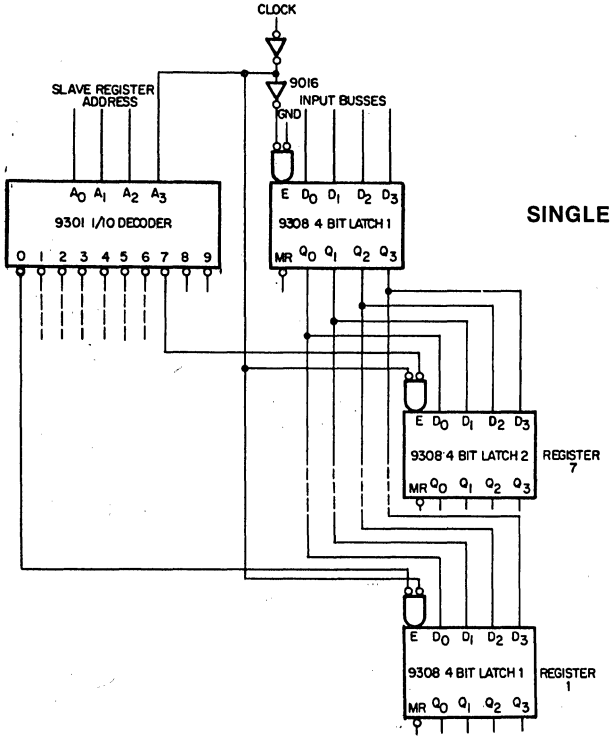
LOADING RULES

All delays are measured with VCC = 5.0 V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTuL gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

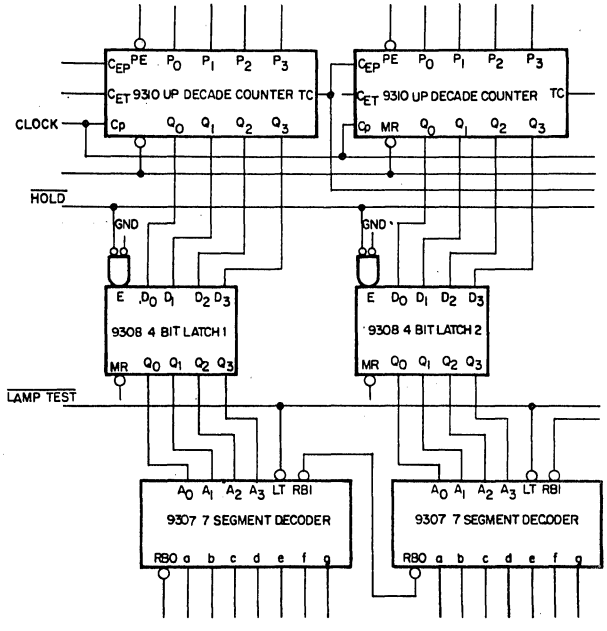
APPLICATIONS



AND-OR ENABLE SHOWING ACTIVE LEVEL LOW ENABLE GATE UTILITY



SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP



ITT9308 AS A HOLDING REGISTER IN COUNTING & DISPLAY APPLICATION

SEMICONDUCTORS

Package: Dual In-Line and Flat Pack

MSI DUAL FOUR-INPUT MULTIPLEXER

- **Multifunction Capability**
- **25 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Complementary Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL 7400 and MSI Families**
- **Input Clamp Diodes Limit High Speed Termination Effects**

The ITT9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with a planar epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the ITT9309 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the ITT9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL for high speed, high fanout operation and is compatible with all DTL, and TTL digital integrated circuits.

LOGIC SYMBOL

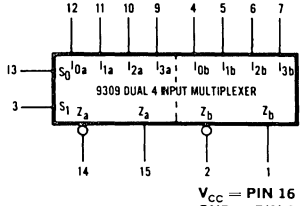


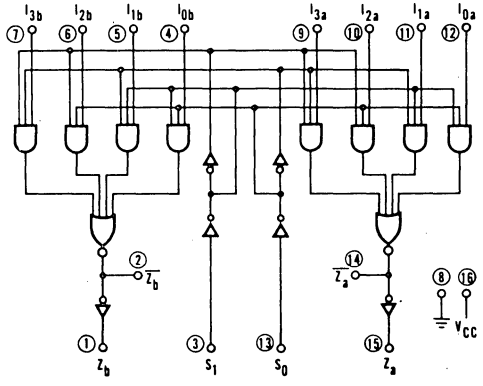
Figure 1

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65°C to +150	°C
Temperature (Ambient) Under Bias ....—55°C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5 V to +7	Volts
Voltage applied to Output when output is high ....0 V to +Vcc	value
Input Voltage (DC) (See Note 1) ....—0.5 V to +5.5	Volts
Input Current (DC) (See Note 1) ....—30 mA to +5	mA
Current into Output when output is low .....+30	mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

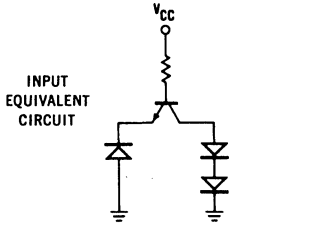
LOGIC DIAGRAM

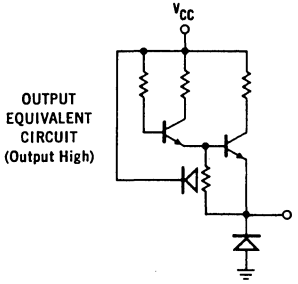


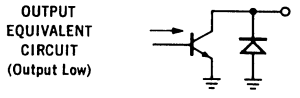
9309
Dual four input multiplexer
Logic diagram

Figure 2

TYPICAL INPUT AND OUTPUT CHARACTERISTICS







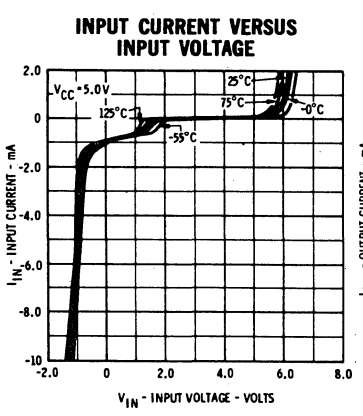


Figure 3

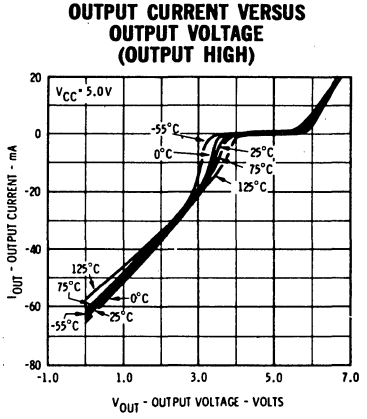


Figure 4

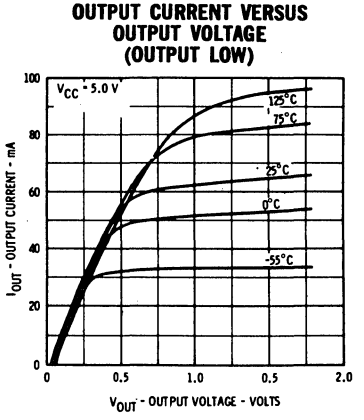


Figure 5

FUNCTIONAL DESCRIPTION

The ITT9309 dual four input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The ITT9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

A common use of the ITT9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The ITT9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

LOADING RULES

(1 U.L. = 1 TTL gate input load)

INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

OUTPUTS	FANOUT AT LOGIC LEVEL HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	18 U.L.	9 U.L.

ELECTRICAL CHARACTERISTICS* [ITT9309-1X] (T_A = −55°C to +125°C, V_{CC} = 5.0 V 10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.2 mA (Pins 1 & 15) V_{CC} = 4.5 V I_{OH} = −1.08 mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 16.0 mA (Pins 1 & 15) I_{OL} = 14.4 mA (Pins 2 & 14) V_{CC} = 4.5 V I_{OL} = 12.4 mA (Pins 1 & 15) I_{OL} = 11.2 mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −.85	−1.6 −1.24		−1.6 −1.24	mA mA	V_{CC} = 5.5 V V_F = 0.4 V V_{CC} = 4.5 V Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	V_{CC} = 5.0 V All inputs high
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* [ITT9309-5X] ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0$ V 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75$ V $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75$ V $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25$ V $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75$ V $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −.91	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25$ V $V_F = 0.45$ V $V_{CC} = 4.75$ V Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25$ V $V_R = 4.5$ V Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0$ V All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	36			ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	36			ns	

*Pulse tested

A.C. CHARACTERISTICS

SWITCHING WAVEFORMS

All inputs are outputs of TTL MIC9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

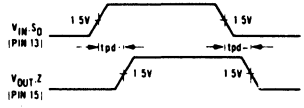


Figure 6

t_{pd}; S_0 to $\overline{Z}_a$
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

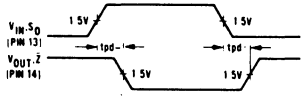


Figure 7

t_{pd}; I_{a0} to $\overline{Z}_a$
CONDITIONS
Pins 3, 13 = GND.

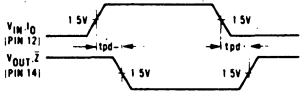


Figure 8

SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

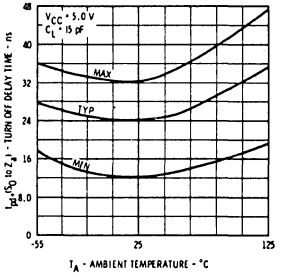


Figure 9

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

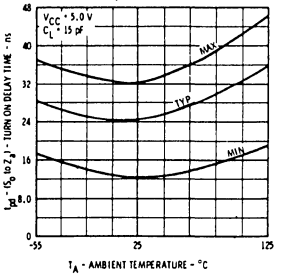


Figure 10

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

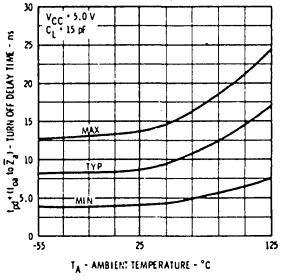


Figure 11

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

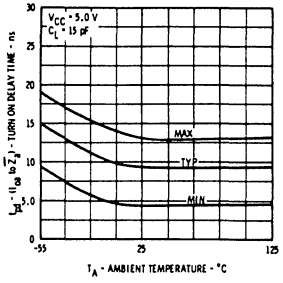


Figure 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

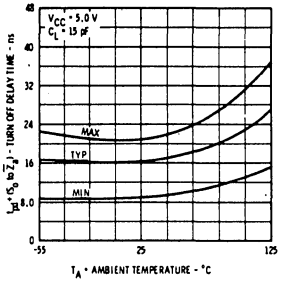


Figure 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

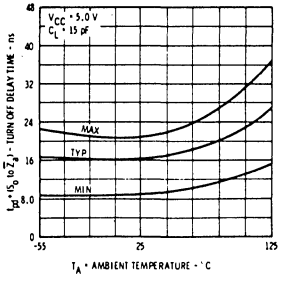


Figure 14

APPLICATIONS

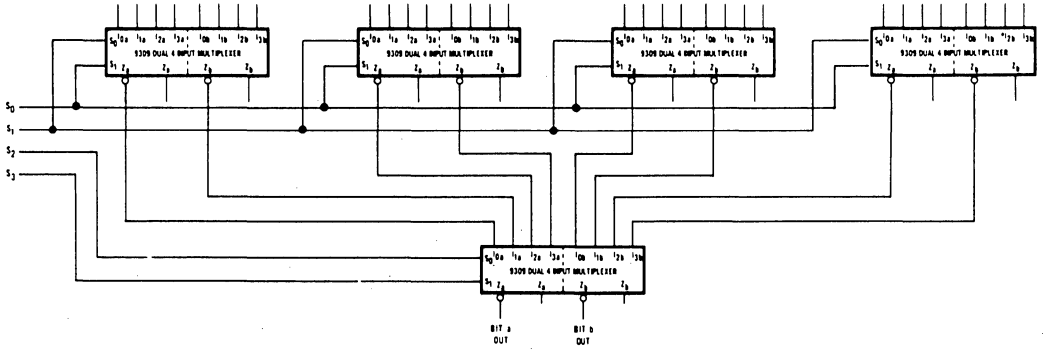
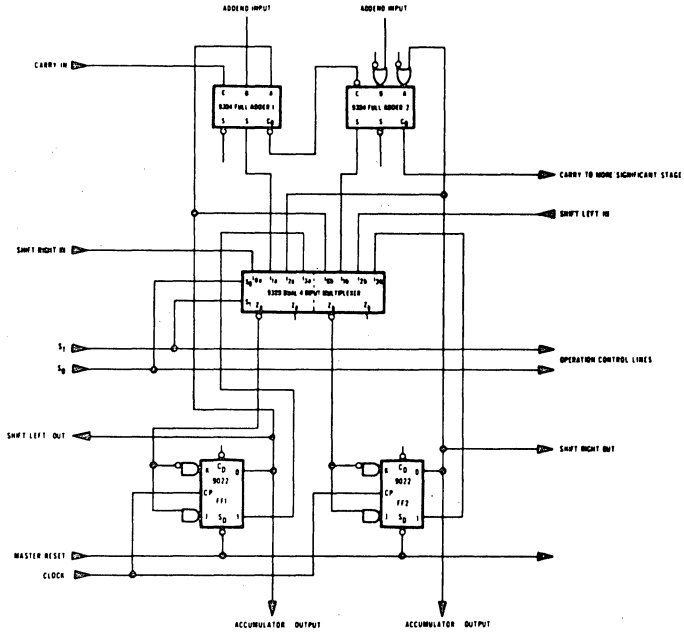


Figure 15

Figure 15 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five ITT9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a tow bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2, and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.



OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

Figure 16 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of: 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator shown above.

The D input capability of the ITT9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the ITT9309 multiplexer.

Under the operation code instructions the multiplexer provides an input to the ITT9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) Q outputs of ITT9022 for the complement operation. The operation code at the right of Figure 18 shows the instruction codes to perform the various operations. The accumulator should be capable of 20-25MHz operation.

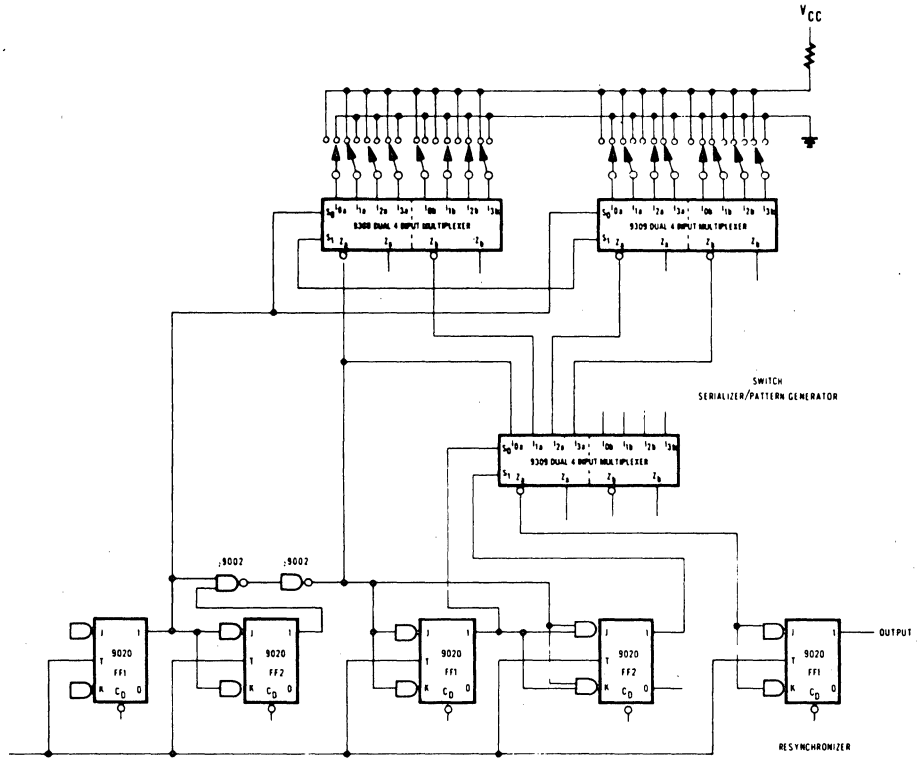
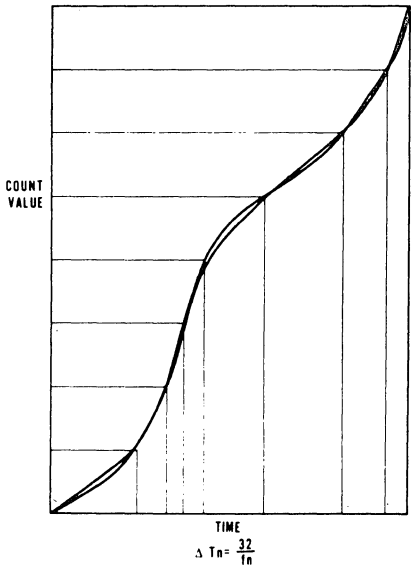


Figure 17 — 16-BIT PATTERN GENERATOR

This application illustrates the use of ITT9309 and ITT9020 in the design of one channel of a 16 bit pattern generator. Each channel requires 1/2 ITT9020, 1/2 ITT9002 and 2-1/2 ITT9309. Each channel consists of a switch serializer/ pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

The resynchronizer flip flop is used to eliminate decoding spikes.



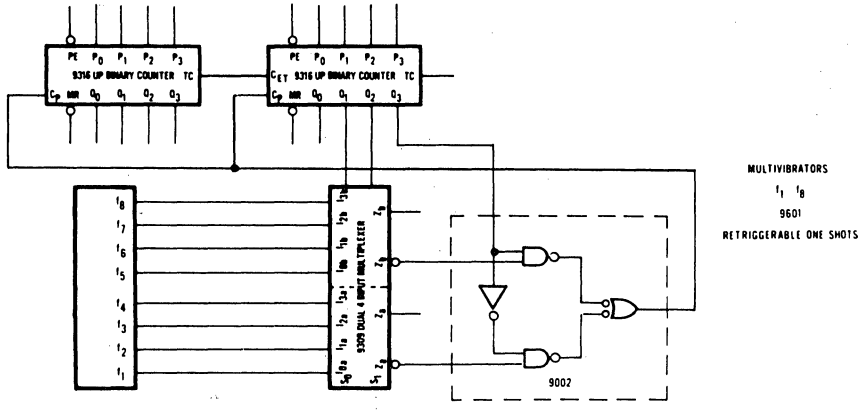


Figure 18 — NON-LINEAR COUNTER

The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by an ITT9309 dual 4-input multiplexer and one ITT9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

MSI ONE-OF-SIXTEEN DECODER

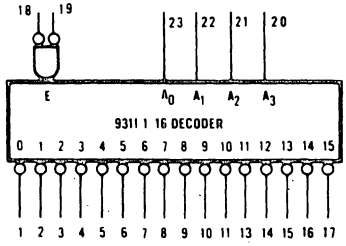
- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage range**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 175 mW**
- **The input/output characteristics provide easy interfacing with DTL, 930 and TTL54/7400 and 9300 families**
- **All ceramic "Hermetic" 24-pin dual in-line package**
- **Input clamp diodes limit high speed line termination effects**
- **Two input enable gate**

The ITT9311 is a multi-purpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL for high speed and high fan-out capability, and is compatible with all members of the 930 DTL, 54/7400 and 9300 families.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65 to +150	°C
Temperature (Ambient) Under Bias .....—55 to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5 to +7	Volts
Voltage Applied to Outputs for high output state .....—0.5V to + Vcc	value
Input Voltage (D.C.) —0.5 to +5.5	Volts

LOGIC SYMBOL



Vcc = Pin 24
Gnd = Pin 12

TRUTH TABLE

E0	EI	A0	A1	A2	A3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

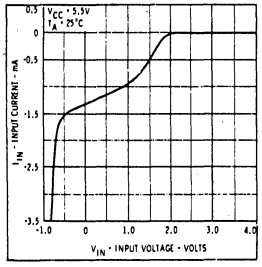
H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

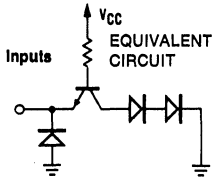
FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four active high BCD inputs and provides 16 mutually exclusive active low outputs, as shown by Figure 1. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The most significant A_3 input produces a useful inhibit function when the 9311 is used as a 1 out of 8 decoder.

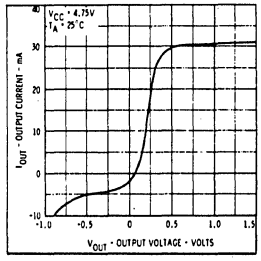
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

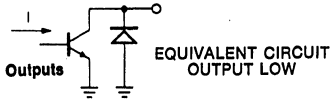
INPUT CURRENT VERSUS INPUT VOLTAGE



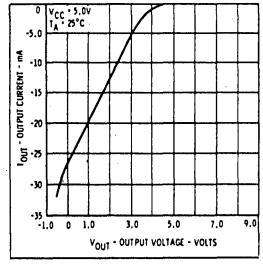


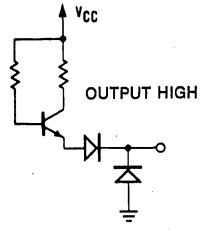
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW





OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH





TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	DRIVE FACTOR
All Outputs	10 U.L.

(1 U.L. = TTL Gate Input Load)

INPUT LOAD AND DRIVE FACTORS

GRADE	INPUTS	LOADING
59	All Inputs	12/11
51	All Inputs	12/10

GRADE	OUTPUTS	DRIVE FACTOR
59	All Outputs	120/94
51	All Outputs	120/78

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
			−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	60			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output			10	23	40			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output			7.0	20	35			ns	
t_{pd+}	Turn Off Delay E Input to Output			10	17	31			ns	
t_{pd-}	Turn On Delay E Input to Output			7.0	17	26			ns	

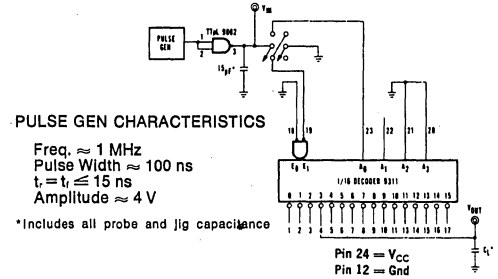
NOTE 1: Units are pulse tested.

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	55			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output				23	35			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output				20	30			ns	
t_{pd+}	Turn Off Delay E Input to Output				17	26			ns	
t_{pd-}	Turn On Delay E Input to Output				16	21			ns	

NOTE 1: Units are pulse tested.

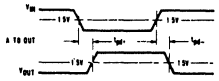
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

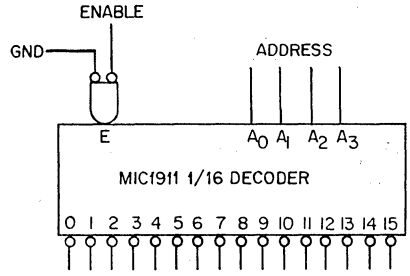


PULSE GEN CHARACTERISTICS

Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V

*Includes all probe and jig capacitance

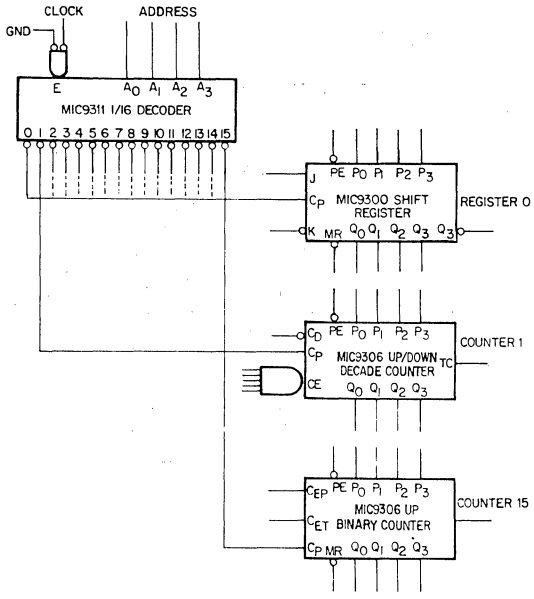




DECODE ANY BCD CODE

Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

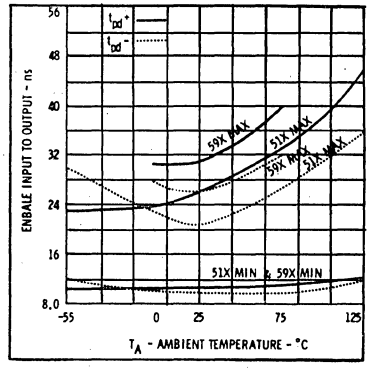
DECIMAL DIGIT	OUTPUT SELECTION			
	BCD CODE			
	8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13



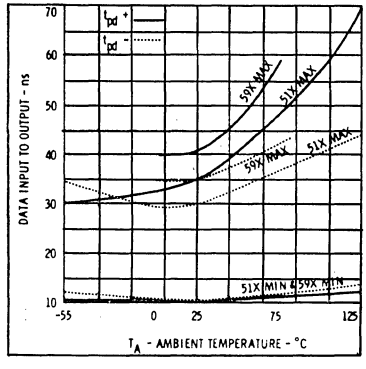
CLOCK DEMULTIPLEXING

The 9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder ouput allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

PROPAGATION DELAY ENABLE INPUT TO OUTPUT VERSUS TEMPERATURE



PROPAGATION DELAY DATA INPUT TO OUTPUT VERSUS TEMPERATURE



SWITCHING PERFORMANCE

MSI EIGHT-INPUT MULTIPLEXER

- Multifunction Capability
- 25 ns Through Delay
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families
- Input Clamp Diodes Limit High Speed Termination Effects

The ITT9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The ITT9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation output are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all DTL and TTL digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65°C to +150	°C
Temperature (Ambient) Under Bias ....—55°C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5 V to+7	Volts
Voltage Applied to Output when output is high ....0 V to + Vcc	value
Input Voltage (DC) (See Note 1) ...—0.5 V to + 5.5	Volts
Input Current (DC) (See Note 1) ....—30 mA to + 5	mA
Current into Output when output is low .....+ 30	mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

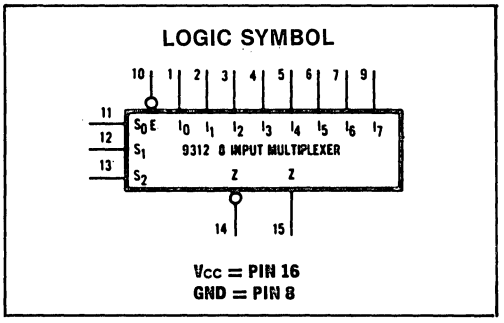


Figure 1

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	FAN-OUT	
	High State	Low State
$\bar{Z}$	18	9
Z	20	10

1 U.L. = 1 TTL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

Figure 2

TRUTH TABLE

E	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	Z	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Lw voltage level
X = Level does not affect output

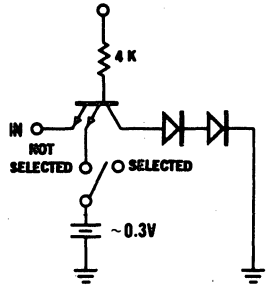
Figure 3

ITT9312
MSI Eight-Input Multiplexer

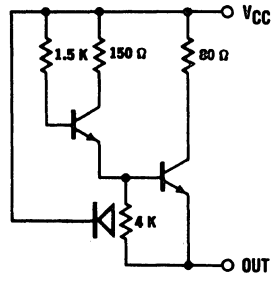
FUNCTIONAL DESCRIPTION — The ITT9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other outputs.

The ITT9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the ITT9312 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one ITT9312.

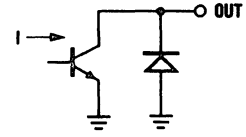
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

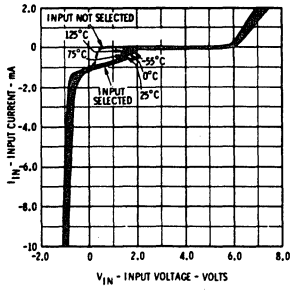


Figure 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

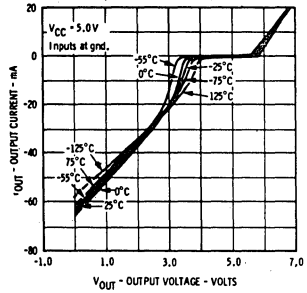


Figure 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

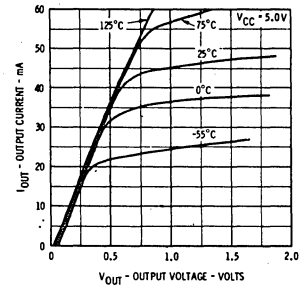


Figure 6

ELECTRICAL CHARACTERISTICS* (MIC9312-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		.04	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pin 15) $I_{OL} = 11.2$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table

ELECTRICAL CHARACTERISTICS* (MIC9312-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) **(continued)**

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −0.85	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		27	40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

*Pulse tested

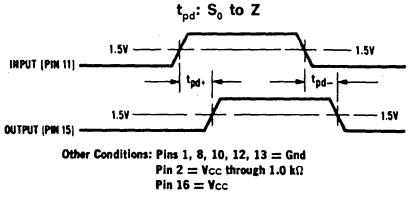
ELECTRICAL CHARACTERISTICS* (MIC9312-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2\ mA$ (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0\ mA$ (Pin 15) $I_{OL} = 14.4\ mA$ (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1\ mA$ (Pin 15) $I_{OL} = 12.7\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −0.91	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		27	43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

*Pulse tested

A.C. CHARACTERISTICS

All measurements are made with Vcc = 5.0 V applied to pin 16 and with pin 8 grounded. The active input is driven by an ITT9002 TTL gate with the output loaded with 15 pF. Both outputs of the ITT9312 are loaded with 15 pF.



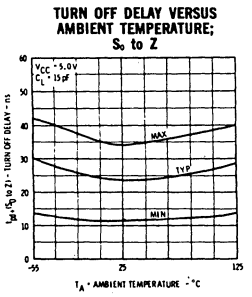


Figure 7

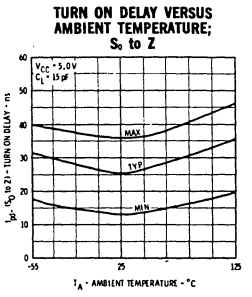
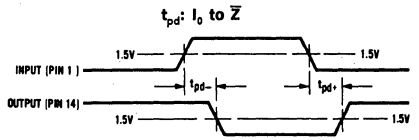
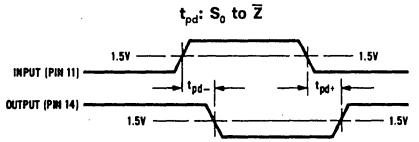


Figure 8





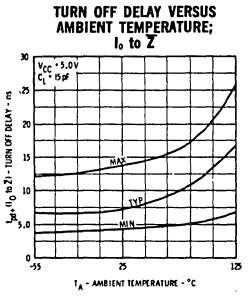


Figure 9

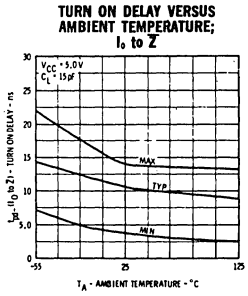


Figure 10

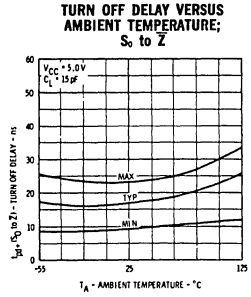


Figure 11

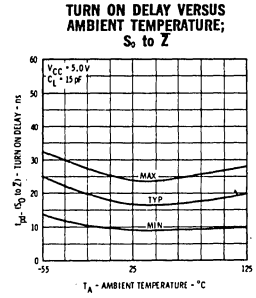
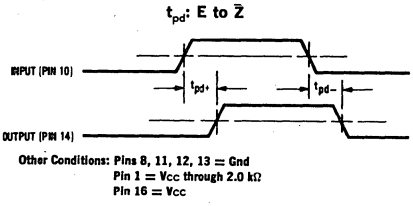


Figure 12



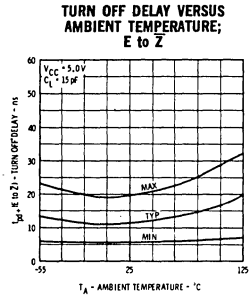


Figure 13

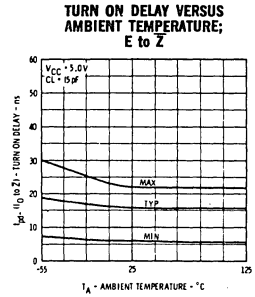


Figure 14

APPLICATIONS

A Multi-Port Memory Module

The four bit by eight word multi-port memory module shown in the diagram below uses only thirteen MSI packages; four ITT9308 24 pin dual four bit latches, eight ITT9312 eight input multiplexers, and one ITT9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.

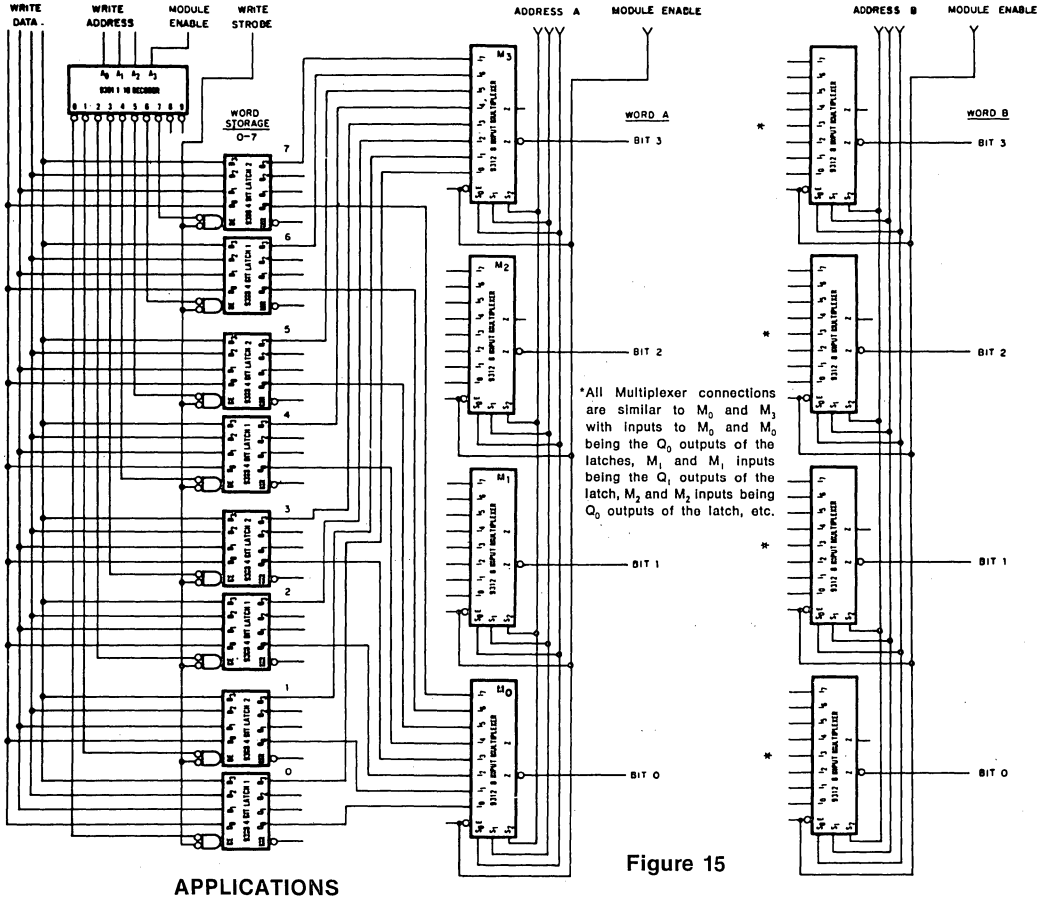


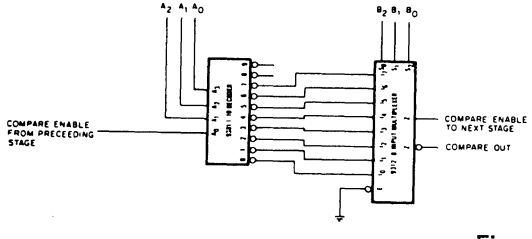
Figure 15

APPLICATIONS

3 Bit Comparator

Three bits of data to be compared are supplied to the address and select inputs of the ITT9301 and ITT9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exlucisve active low output of the ITT9301 1/10 decoder and the selected input of the ITT9312 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

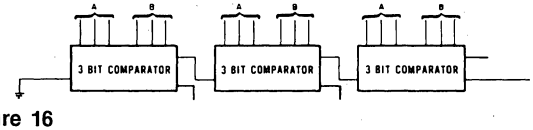


Figure 16

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The ITT9312 input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

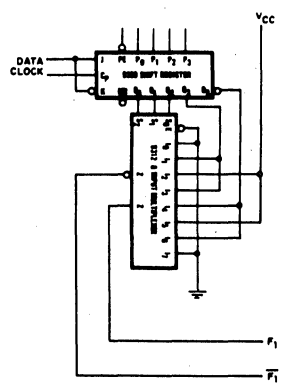
The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the ITT9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the ITT9312. In order to implement the function each input of the ITT9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is an ITT9312 decoding condition of an ITT9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the ITT9312 for this function are also shown in the illustration.

In many applications, using the ITT9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the ITT9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the ITT9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.



Q_0	Q_1	Q_2	Q_3	F_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

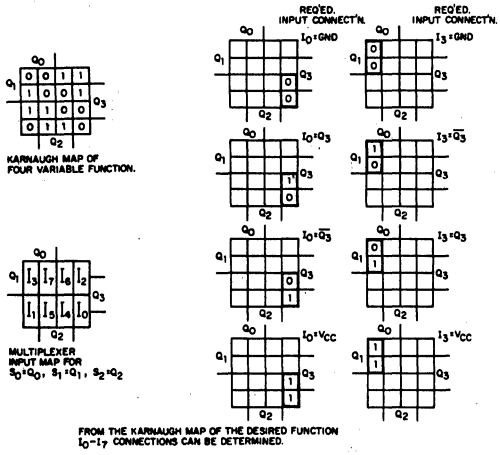


Figure 17

MSI 4-BIT BINARY COUNTER

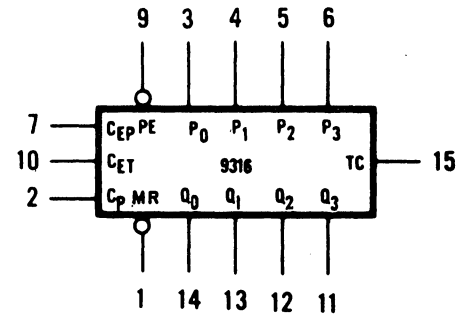
- **Synchronous Counting and Parallel Entry**
- **Decoded Terminal Count**
- **Built-In Carry Circuitry**
- **Typical Power Dissipation of 300 mW**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families.**
- **All Ceramic Hermetic 16 Pin Dual In-Line Package and Flat Package**
- **Input Diode Clamps Limit High Speed Line Termination Effects**

The ITT9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presettable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65 C to +150	C
Temperature (Ambient) Under Bias .....—55 C to +125	C
Vcc Pin Potential to Ground Pin .....—0.5V to +7	Volts
Voltage Applied to Outputs for high output state .....—0.5V to Vcc	value
Input Voltage (D.C.) —0.5V to +5.5	Volts

LOGIC DIAGRAM

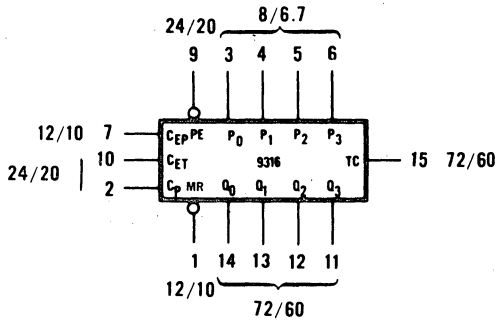


V_{CC} = Pin 16
Gnd = Pin 8

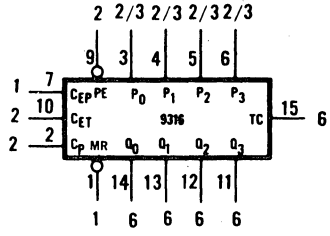
FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

LOADING RULES

CCSL LOAD AND DRIVE FACTORS



TTL LOAD AND DRIVE FACTORS



ELECTRICAL CHARACTERISTICS (MIC9316-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
$\frac{2}{3}\ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120		120	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
$\frac{2}{3}\ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS (MIC9316-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$\frac{2}{3}\ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	

ELECTRICAL CHARACTERISTICS (MIC9316-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\,V \pm 5\%$) **(continued)**

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60	60	μA	
2 I_R	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120	120	μA	$V_{CC} = 5.25\,V$ $V_R = 4.5\,V$
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40	40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\,V$ $C_L = 15\,pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s(CE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\,V$
t_r (CE)	Release Time for CE		12		ns	$C_L = 15\,pF$ (Fig. 2)
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\,V$ $C_L = 15\,pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s ($\overline{PE}$)	Set-Up Time for $\overline{PE}$		30		ns	
t_r ($\overline{PE}$)	Release Time for $\overline{PE}$		28		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay for $\overline{MR}$		33		ns	$V_{CC} = 5.0\,V$, $C_L = 15\,pF$ (Fig. 4)
t_{p+}	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\,V$, $C_L = 15\,pF$ (Fig. 5)

SET-UP TIME: ts is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: tr is deinfed as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

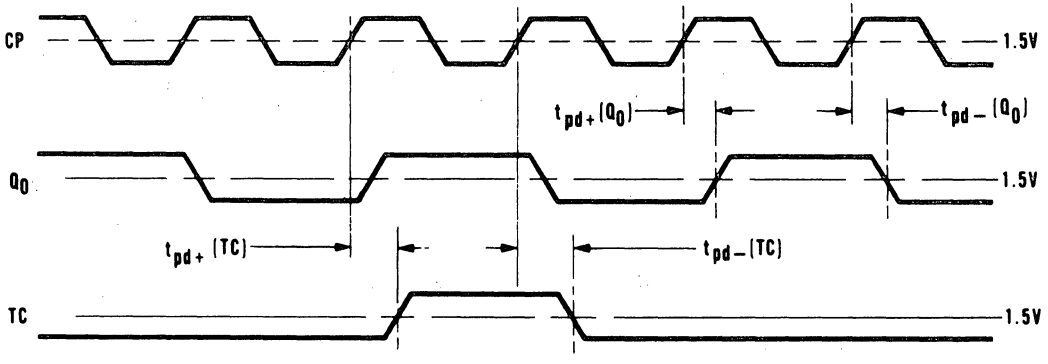


Figure 1

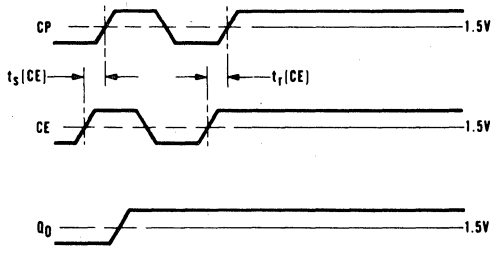


Figure 2

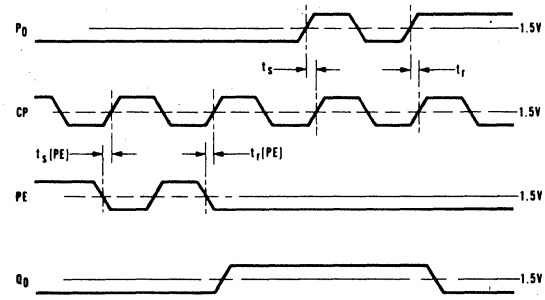


Figure 3

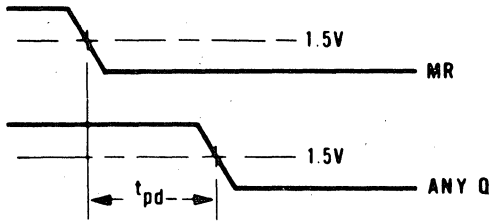


Figure 4

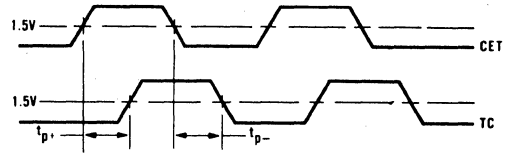
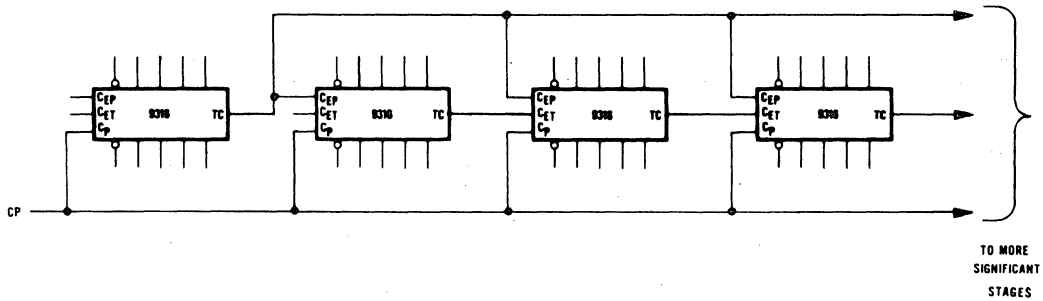


Figure 5

APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

MSI QUAD TWO-INPUT MULTIPLEXER

- **Multifunction Capability**
- **20 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with ITT DTL930, ITT TTL 9000, MSI and other DTL and TTL Families.**
- **Input Clamp Diodes Limit High Speed Termination Effects.**

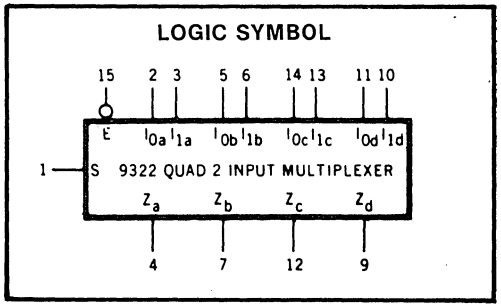
The ITT9322 is a monolithic, high speed, quad two-input digital multiplexer circuit, constructed with the ITT epitaxial process. It consists of four multiplexing circuits with common select and enable logic, each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fanout operation and is compatible with all other members of the DTL and TTL family of digital integrated circuits.

A common use of the ITT9322 would be the moving of data from a group of registers to four common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The ITT9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

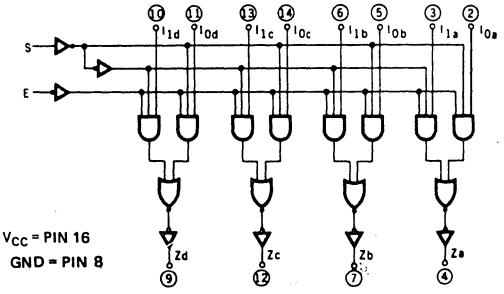
$$Z_a = E \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \qquad Z_b = E \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$
$$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \qquad Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

FUNCTIONAL DESCRIPTION — The ITT9322 quad two input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The enable input (E) is active low. When not activated all outputs (Z) are low regardless of all other inputs.

LOGIC SYMBOL



LOGIC DIAGRAM



The ITT9322 quad two input multiplexer is the logical implementation of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65 C to +150	C
Temperature (Ambient) Under Bias .....—55 C to +125	C
Vcc Pin Potential to Ground Pin .....0.5V to +7.0	V
Voltage Applied to Output when output is high.....0 V to + Vcc	value
Input Voltage (DC) (See Note 1).....—0.5 V to + 5.5	V
Input Current (DC) (See Note 1).....—30 mA to +5	mA
Current into Output when output is low .....+30	mA

NOTE 1: either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ELECTRICAL CHARACTERISTICS (T_A = −55 C to +125 C, V_{CC} = 5.0V 10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+125°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 16.0 mA V_{CC} = 4.5 V I_{OL} = 12.4 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−1.24		−0.85	−1.24		−1.24	mA	V_{CC} = 4.5 V Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V
I_{PDH}	V_{CC} Current		43		30	43		43	mA	V_{CC} = 5.0 V All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	25			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	27			ns	

*Pulse Tested

ELECTRICAL CHARACTERISTICS (T_A = 0 C to +75 C, V_{CC} = 5.0V 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+125°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V I_{OH} = −1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−1.41		−0.91	−1.41		−1.41	mA	V_{CC} = 4.75 V Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V
I_{PDH}	V_{CC} Current		45		30	45		45	mA	V_{CC} = 5.0 V All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	30			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	31			ns	

*Pulse Tested

TRUTH TABLE
Identical for Each Multiplexer

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

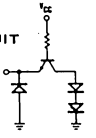
L = low voltage level
H = high voltage level
X = Either high or low logic level

LOADING RULES
(1 U.L. = 1 TTL gate input load)

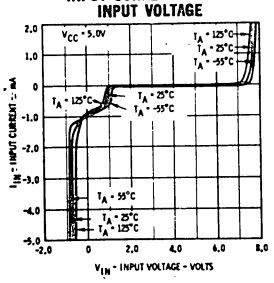
INPUTS	LOADING	
I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d} S, E	1 U.L.	
OUTPUTS	FANOUT AT LOGIC LEVEL HIGH	LOW
Z_a, Z_b, Z_c, Z_d	20 U.L.	10 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

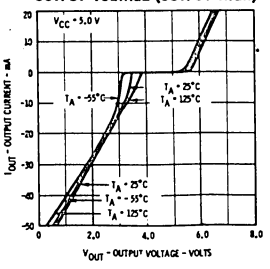
INPUT EQUIVALENT CIRCUIT



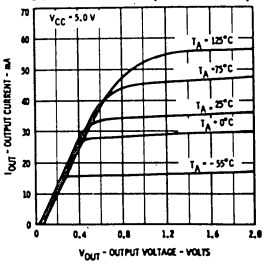
INPUT CURRENT VERSUS INPUT VOLTAGE



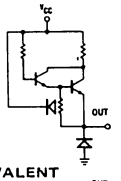
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



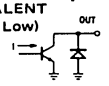
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



OUTPUT EQUIVALENT CIRCUIT (Output High)



OUTPUT EQUIVALENT CIRCUIT (Output Low)

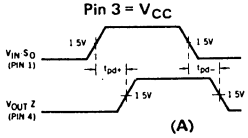


A.C. CHARACTERISTICS

SWITCHING WAVEFORMS — All inputs are outputs of TTL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S to Z_a

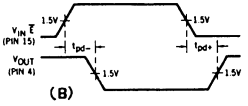
CONDITIONS — Pins 2, 15 = GND
Pin 3 = V_{CC}



(A)

t_{pd}; $\overline{E}$ to Z_a

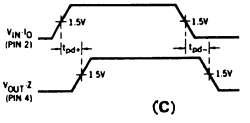
CONDITIONS — All Other Inputs High



(B)

t_{pd}; I_{0a} to Z_a

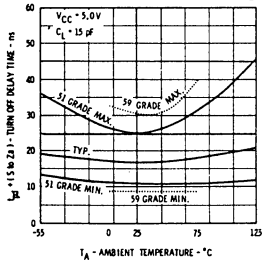
CONDITIONS—Pins 1, 15 = GND.



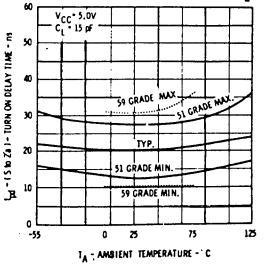
(C)

SWITCHING CHARACTERISTICS

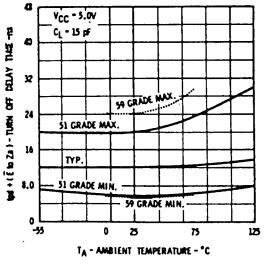
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



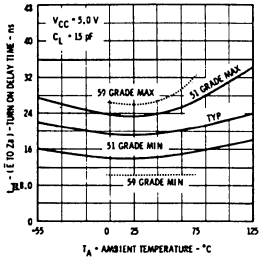
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



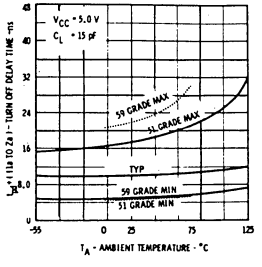
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



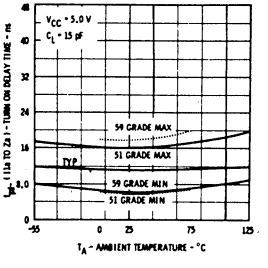
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



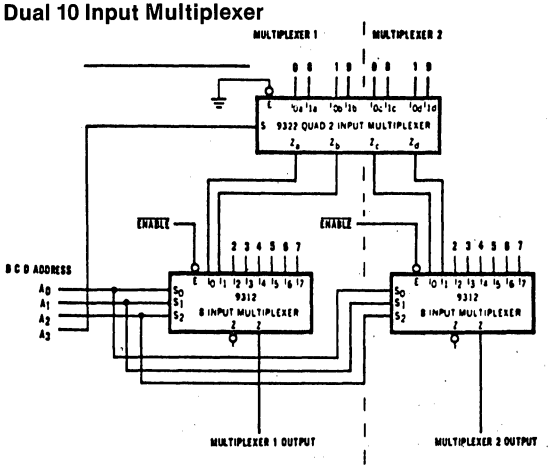
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)



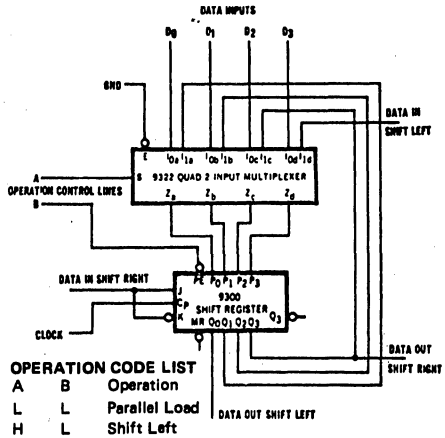
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)



APPLICATIONS
Dual 10 Input Multiplexer



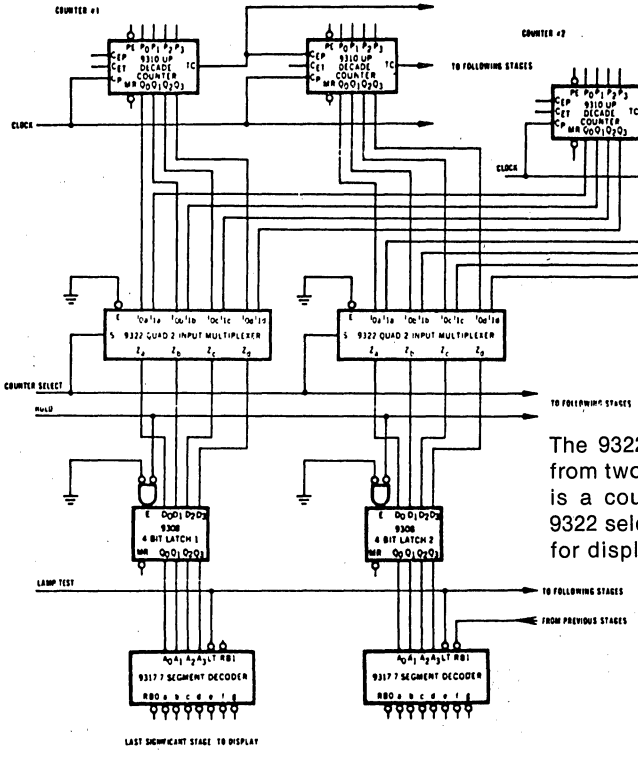
SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



OPERATION CODE LIST

A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.



APPLICATIONS
Register Selection

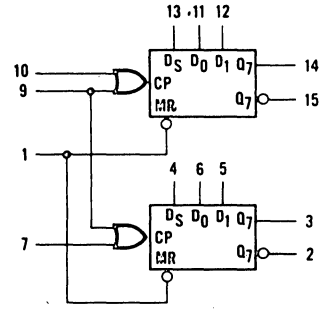
The 9322 can be used to select parallel data from two multiple bit sources. Illustrated above is a counting and display system where the 9322 selects the content of one of the counters for display.

SEMICONDUCTORS

MSI DUAL 8-BIT SHIFT REGISTER

- 20 MHz Shift Frequency
- Two Input Multiplexer Provided at Data Input of Each Register
- Gated Clock Input Circuitry
- Both True and Complementary Outputs Provided from Last Bit of Each Register
- Asynchronous Master Reset Common to Both Registers
- Typical Power Dissipation of 300 mW
- Compatible with TTL and DTL families
- Input Diode Clamping

LOGIC DIAGRAM



Vcc = Pin 16 Gnd = Pin 8

The ITT 9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.

ABSOLUTE MAXIMUM RATINGS

(above which useful life may be impaired)

Characteristics	Units
Storage Temperature .....—65 C to +150	°C
Temperature (Ambient) Under Bias .....—55 C to +125	°C
Vcc Pin Potential to Ground Pin .....—0.5 V to +7	V
Voltage Applied to Outputs for high output state.—0.5V to + Vcc	value
Input Voltage (D.C.) —0.5V to +5.5	V

FUNCTIONAL DESCRIPTION — The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RD master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the

master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:

Serial data in: $S_D = D_S D_0 + D_S D_I$

An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

LOADING RULES

(1 U.L. = TTL input gate load)

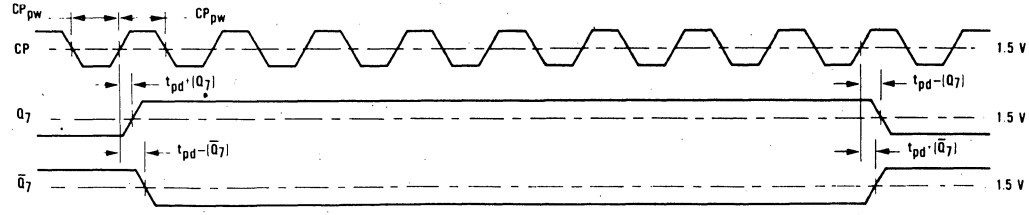
INPUT	FAN IN
MR, D_0 D_I	1 Unit Load
Separate CP (pins 9 & 10)	1.5 Unit Loads
D_S	2 Unit Loads
Common CP (pin 9)	3 Unit Loads

OUTPUT	FAN OUT
Q_7, $\overline{Q}_7$	6 Unit Loads

ELECTRICAL CHARACTERISTICS (T_A = −55°C to + 125°C, V_{CC} = 5.0V ± 10%)

		LIMITS							
		−55°C		+25°C			+125°C		
SYMBOL	CHARACTERISTICS	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC}=4.5V, I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC}=5.5V, I_{OL}=9.6mA
										V_{CC}=4.5V, I_{OL}=7.44mA
V_H	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_I)		−1.6		−1.0	−1.6		−1.6	mA	
1.5 I_F	Input Load Current (separate CP pins 7 & 10		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.5V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_P	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	
1.5 I_P	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.5V
2 I_P	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_P	Input Leakage Current (common CP pin 9)		1801		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

SWITCHING WAVEFORMS



NOTE: Q7 is connected to D1. Other clock is grounded.

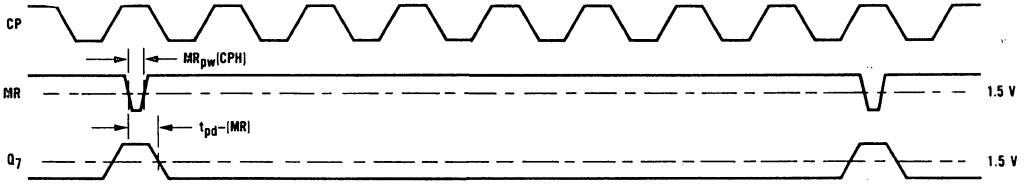
Figure 1

ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{cc} = 5.0V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+ 25°C MIN.	TYP.	MAX.	+ 75°C MIN.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC}=4.75V, I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC}=5.25V, I_{OL}=9.6mA V_{CC}=4.75V, I_{OL}=8.5mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_1)		−1.6		−1.0	−1.6		−1.6	mA	
1.5 I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.25V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.25V
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

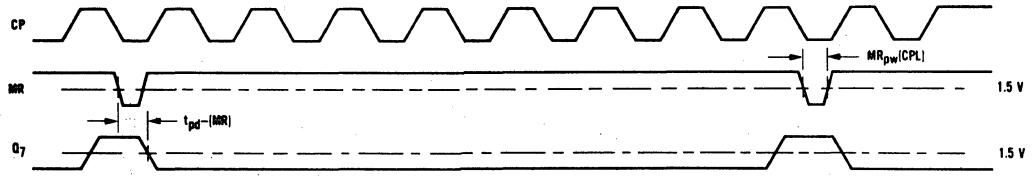
SWITCHING CHARACTERISTICS (T_A= 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
t_{pd}−(Q_7& Q_7	Turn-Off Delay (clock to output)		13		ns	V_{cc}=5.0V, C_L=15 pF Fig.1
t_{pd}−(Q_7&$\bar{Q}_7$)	Turn-On Delay (clock to output)		22		ns	
t_{pd}−(MR)	Turn-On Delay (Master reset to output)		35		ns	V_{cc}=5.0V, C_L=15pF Fig. 2 & 3
CP_{pw}	Min. Clock Pulse Width		14		ns	V_{cc}=5.0V, C_l=15 pF Fig. 1
MR_{pw}(CPH)	Min. Master Reset pulse width with clock high		15		ns	V_{cc}5.0V, C_L=15 pF Fig. 2
MR_{pw}(CPL)	Min. Master Reset pulse width with clock low		28		ns	V_{cc}=5.0V, C_L=15pF Fig. 3



NOTE: DS, D1, D0, are high. Other clock input is grounded.

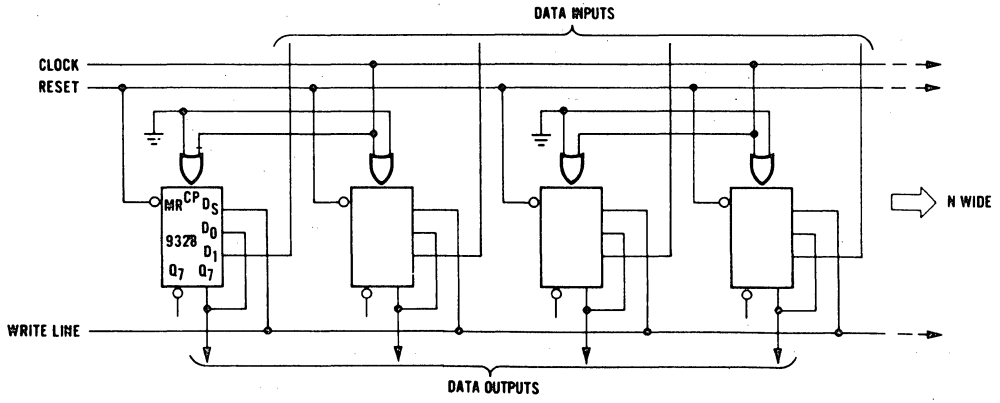
Figure 2



NOTE: DS,D1, D0 are high. Other Clock input is grounded.

Figure 3

APPLICATION:



N-BIT BY 8-WORD HIGH-SPEED MEMORY

Packages: 14 lead Dip and Flat Pack

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TTL

- **Complementary Outputs and Complementary DC level sensitive inputs — insensitive to input pulse transition time.**
- **"Leading edge" or "trailing edge" triggering.**
- **High speed operation — maximum input repetition rate greater than 10 MHz.**
- **High noise immunity — 400 mV worst case.**
- **High fanout — up to 8 TTL loads.**
- **Accurate timing — determined by external R and C — 50 nsec. to output pulse width range.**
- **Choice of operating mode — inputs can normally allow retriggering, but can also be locked out.**
- **Input diode clamps prevent ringing.**
- **Logic levels are compatible with ITT DTL 930, ITT TTL 9000, MSI and other DTL and TTL families.**
- **Pulse width compensated for V cc and temperature variations.**

The retriggerable monostable multivibrator or one-shot provides an output pulse with high accuracy and a very wide duration range (50 nsec. to ∞). It has four DC level-sensitive inputs, two are active-level High and two are active-level Low. Designed for high speed operation, the ITT9601 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

The unique design of the ITT9601 makes it very useful in applications such as in square-wave and variable delay pulse generators, long delay timers, pulse absence detectors, digital low-pass filters, and even FM demodulators.

ABSOLUTE MAXIMUM RATINGS

Characteristics		Units
Storage Temperature	—65 to +150	C
Temperature (Ambient) Under Bias	—55 to +125	C
Vcc Pin Potential to Ground (See Note 1)	—0.5 to +8.0	Volts
Input Voltage (D.C.) (See Note 2)	—0.5 to +5.5	Volts
Input Current (See Note 2)	—30 to +5.0	mA
Voltage Applied to Output When Output is High	0 V to +Vcc	value
Current Into Output When Output is Low	50	mA

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation (Q) output back to an active level high input.

Active pullups are provided for good drive capability into capacitive loads.

NOTES:

(1) The maximum VCC value of 8.0 volts is not the primary factor in determining the maximum VCC which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 VBE below the VCC voltage so the primary limit on the VCC is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system VCC to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than —0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

ITT9601
Retriggerable Monostable Multivibrator TTL

OPERATION RULES

1. An external resistor Rx and an external capacitor Cx are required as shown in the logic diagram. The values of Rx may vary from 5.0 kΩ to 50 kΩ for 0 to +75°operation, and 5.0 kΩ to 25 kΩ for −55 to +125° operation. Cx may vary from 0 to any value necessary and obtainable.

2. If a fixed value of Rx is used, the following values are recommended: Rx = 30 kΩ for 0 to +75°C operation; Rx = 10 kΩ for −55 to +125°C operation.

3. The output pulse width T is defined as follows:

   $T = 0.32\ RxCx\ [1 + \frac{0.7}{Rx}]$ (For Cx greater than 10^3 pF)

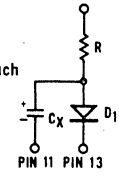
   Where Rx is in kΩ, Cx is in pF, T is in ns

   For Cx < 10^3 pF, see Figure 14

4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:

   R < 0.6 Rx (Max)

   D_1: any silicon type diode, such as FD700

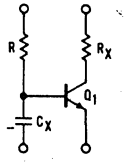


   This circuit also amplifies Cx allowing for longer output pulse width.

   R < Rx (0.7) ($h_{fe}Q_1$)

   Rx (min) < Rx < Rx (max)

   Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

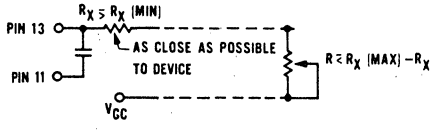


   Both circuits prevent reverse voltage across Cx. The pulse width T for the circuits is defined as follows:

   $T \approx 0.36\ RCx\ [1 + \frac{0.7}{R}]$

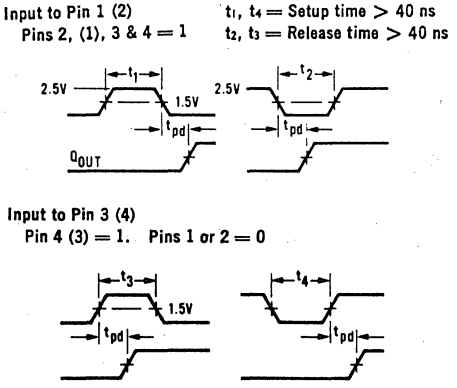
   Where R is in kΩ, Cx is in pF, T is in ns

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

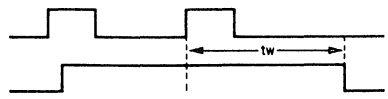


6. Under any operating condition, Cx and Rx (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules.



8. The retrigger pulse width is calculated as shown below:

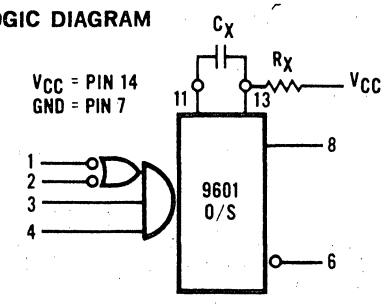


$tw = tpw + tpd+ = 0.32\ RxCx\ (1 + \frac{0.7}{Rx}) + tpd+$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering will not occur if the retrigger pulse comes within .32 RXCX ($\frac{.7}{Rx}$) ns after the initial trigger pulse.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS (Note 1)
		−55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.72$ mA (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10$ mA (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	$V_{CC} = 4.5\ V$ (Note 3)
V_{IL}	Input Low Voltage		0.85			0.90		0.85	Volts	$V_{CC} = 5.5\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.5\ V$
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II — ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96$ mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 12.8$ mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage		.85			0.85		0.85	Volts	$V_{CC} = 5.25\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{Fd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.25\ V$ Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

NOTES:

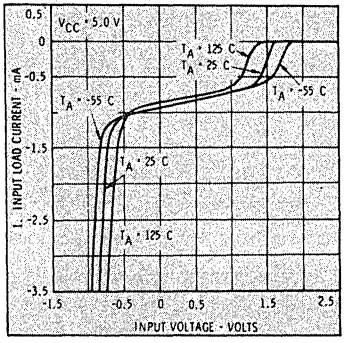
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.

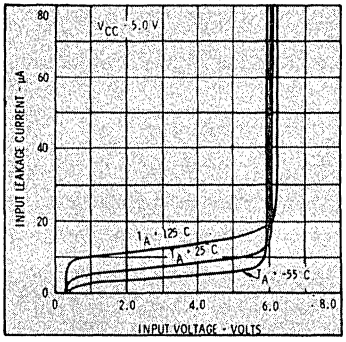
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

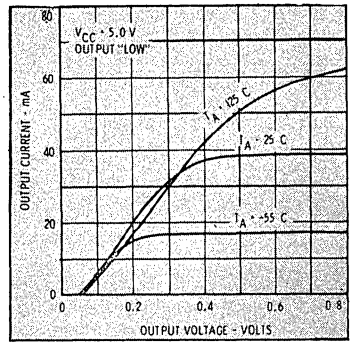
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



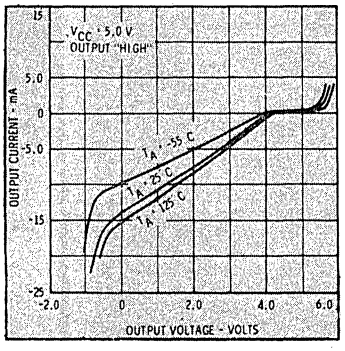
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



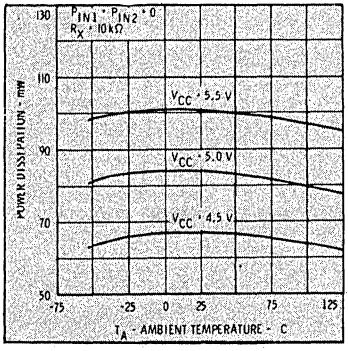
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



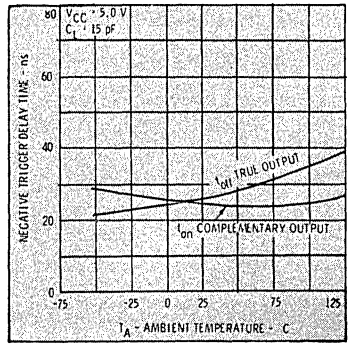
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



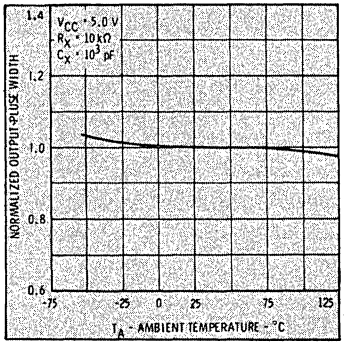
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



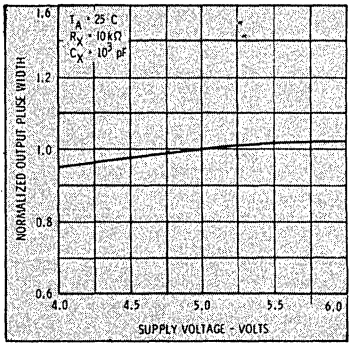
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



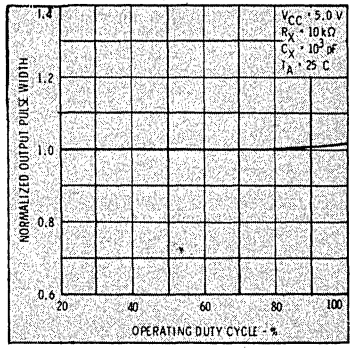
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



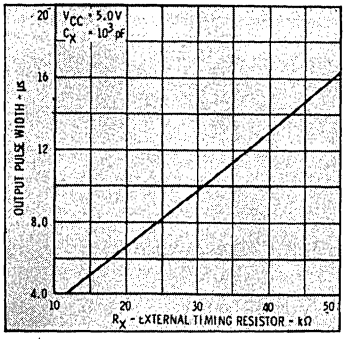
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



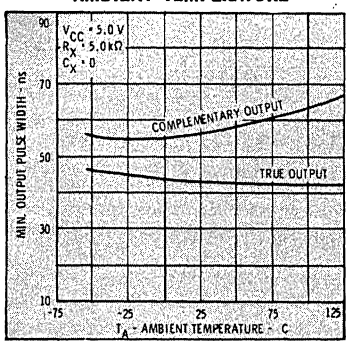
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



PULSE WIDTH VERSUS TIMING RESISTANCE

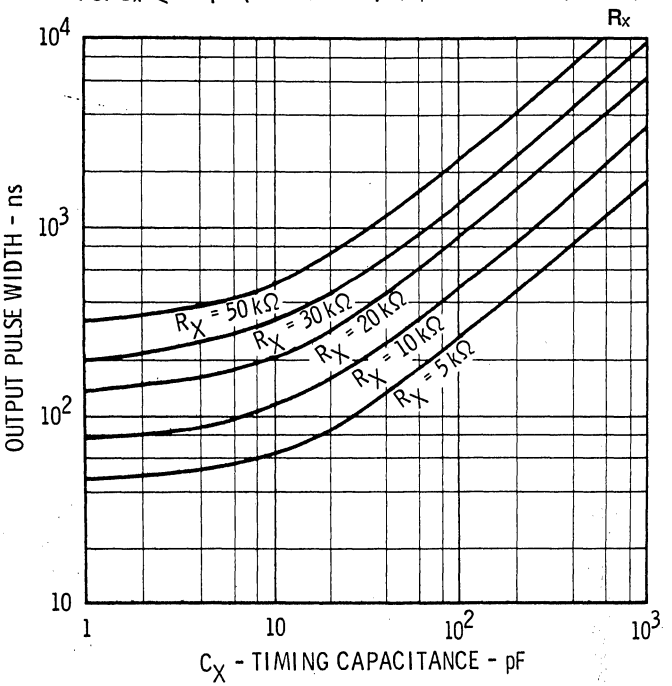


OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

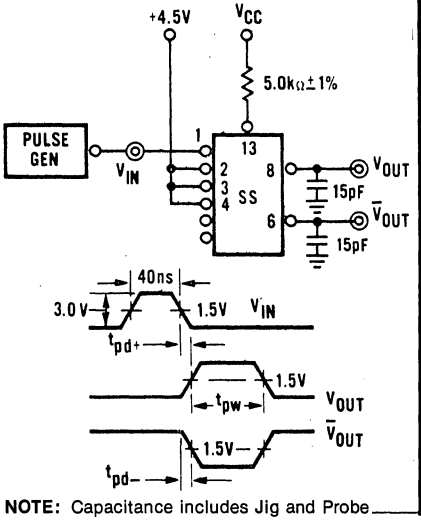


OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF (For $C_X \geq 10^3$pF, $t_{pw} = 0.32\ R_X C_X\ (1 + 0.7)$



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTµL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	12
Low	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	16
Low	8

CCSL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

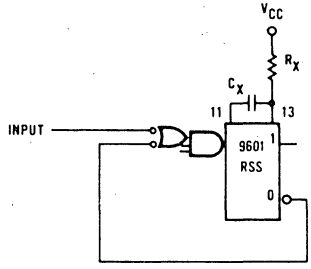
INPUT LEVEL	LOAD FACTOR
High	12
Low	10
OUTPUT STATE	DRIVE FACTOR
High	144
Low	62

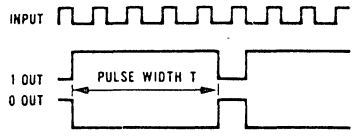
0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	12
Low	10.5
OUTPUT STATE	DRIVE FACTOR
High	192
Low	85

ITT9601
Retriggerable Monostable Multivibrator TTL

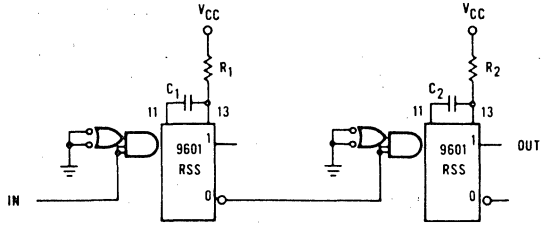
APPLICATIONS





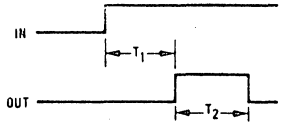
FREQUENCY DIVISION

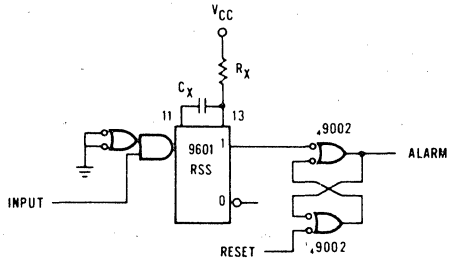
This configuration make the 9601 non-retriggerable and capable of frequency division.



DELAYED PULSE GENERATION

The first 9601 determines the time T1 before the initiation of the output pulse. The second 9601 determines t2, the output pulse width.



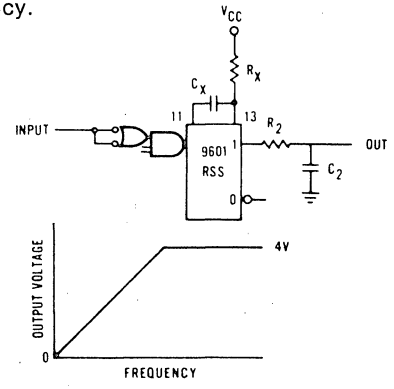


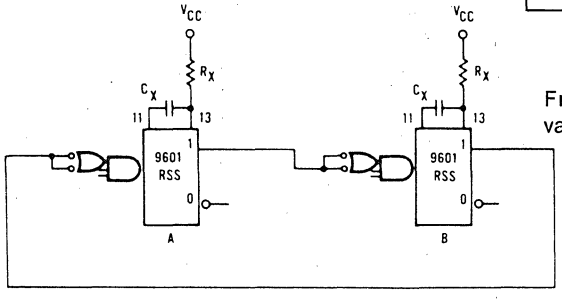
MALFUNCTION INDICATOR

The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input, may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.

DISCRIMINATOR

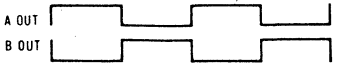
The 9601 can be used to produce a voltage output proportional to input frequency. For a fixed TC of Rx and Cx, the duty cycle of the output will vary with frequency. This is integrated by R2C2 producing a voltage proportional to frequency.





ASTABLE MULTIVIBRATOR

Frequency of operation is dependent upon value of Rx and Cx.



ITT
SEMICONDUCTORS

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

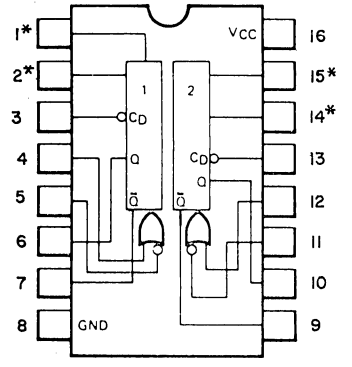
The TTL/Monostable ITT9602 is a dual retriggerable, resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The ITT9602 has excellent immunity to noise on the Vcc and ground lines. The ITT9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the TTL family.

- **72 ns to ∞ Output Width Range**
- **Retriggerable 0 to 100% Duty Cycle**
- **TTL Input Gating - Leading or Trailing Edge Triggering**
- **Complementary TTL Outputs**
- **Optional Retrigger Lock-Out Capability**
- **Pulse Width Compensated for Vcc and Temperature Variations**
- **Resettable**

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Characteristics	Units
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Vcc Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	−0.5 V to +Vcc value
Current Into Ouput When Output is Low	50mA

CONNECTION DIAGRAM
(TOP VIEW)



*Pins for external timing

FUNCTIONAL DESCRIPTION

The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active high and one active low. This allows leading edge or trailing ege triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. (See Rule 9.) The output pulse may be determined at any time by correcting the reset pin to a low logic level pin. Active pullups are provided on the outputs for good drive capability into the capacitive loads.

NOTES:

1. The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

ITT9602

Dual Retriggerable Resettable Monostable Multivibrator

OPERATION RULES

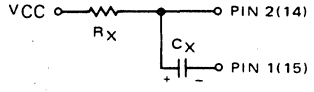
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75 C operation. The value of R_X may vary from 5.0 to 25 kΩ for −55°to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \left[1 + \frac{1}{R_X}\right]$$

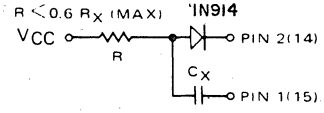
Where R_X is in kΩ
C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 17.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

A. Use with low leakage electrolytic capacitors.
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range and Rule 3 above is satisfied.



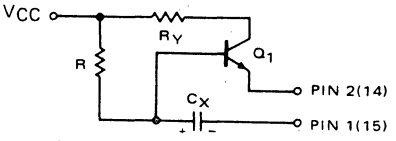
B. Use with high inverse leakage current electrolytic capacitors.
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



C. Use to obtain extended pulse widths:

$$t \approx 0.3\ RC_X$$

This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electolytics with high inverse leakage currents can be used.



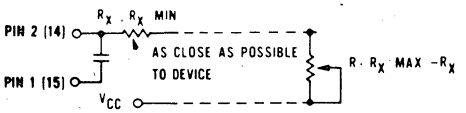
$R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or <2.5 MΩ whichever is the lesser
$R_X\ (min) < R_Y < R_X\ (max)$

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\ RC_X$$

This configuration is not recommended with retriggerable operation.

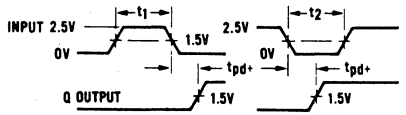
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



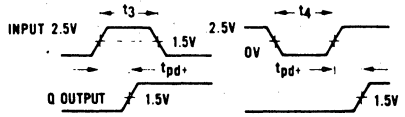
7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Tables, page 5.

Input to Pin 5 (11)
Pin 4 (12) = Low
Pin 3 (13) = High

t_1, t_3 = Min. Positive Input Pulse Width >40 ns
t_2, t_4 = Min. Negative Input Pulse Width >40 ns

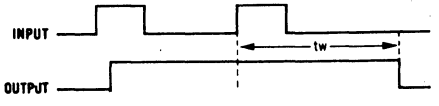


Input to Pin 4 (12)
Pin 5 (11) = High, Pin 3 (13) = High



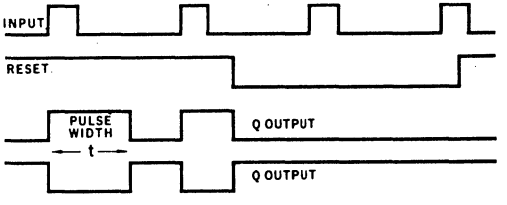
9. The retriggerable pulse width is calculated as shown below:

$$tw = tpw + t_{pd+} = 0.31\ R_X C_X\ (1 + \frac{1}{R_X}) + t_{pd+}.$$



The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw. Retriggering will not occur if the retrigger pulse comes within ≈0.3 Cx ns after the initial trigger pulse. (i.e. during the discharge cycle).

10. Reset Operation — An overriding active low level reset is provided on each one-shot. By applying a low to the reset, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.



11. Vcc and Ground wiring should conform to good high frequency standards so that switching transients on Vcc and Ground leads do not cause interaction between one-shots.

ELECTRICAL CHARACTERISTICS (T_A = —55°C to 125°C, V_{CC} = 5 V ±10%)

Symbol	−55°C Min.	−55°C Max.	Limits +25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.62 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	2.0		1.7			1.5		Volts	Guaranteed input high
V_{IL}		0.85			0.90		0.85	Volts	Guaranteed input low
I_{IL}		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
		−1.24		−0.97	−1.24		−1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}				10	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}					−25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		45		39	45		45	mA	V_{CC} = 5.0 V
t_{pd+}				25	35			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{pd-}				29	43			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	90			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	100			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	25	5.0		25	5.0	25	kΩ	

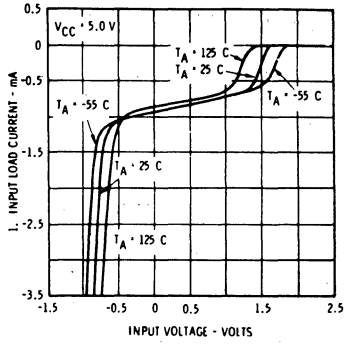
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	−0°C Min.	−0°C Max.	Limits +25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	1.9		1.8			1.65		Volts	Guaranteed input high
V_{IL}		0.85			0.85		0.85	Volts	Guaranteed input low
I_{IL}		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
		−1.41			−1.41		−1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}				10	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}					−35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		52		39	50		52	mA	V_{CC} = 5.0 V, Ground, Pins 1 and 2
t_{pd+}				25	40			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{pd-}				29	48			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	100			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	110			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	50	5.0		50	5.0	50	kΩ	

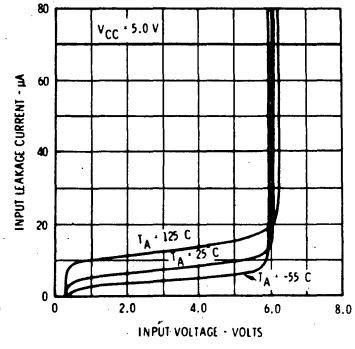
1. Unless otherwise noted, 10kΩ resistor placed between Pin 2 (14) and VCC, for all tests. (RX)
2. Ground Pin 1 (15) for VOL on Pin 7 (9), or VOH on Pin 6 (10), or for ISC on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for VOL on Pin 6 (10), or for VOH on Pin 7 (9), or for ISC on Pin 7 (9).

TYPICAL ELECTRICAL CHARACTERISTICS

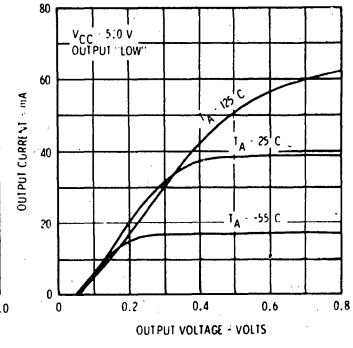
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



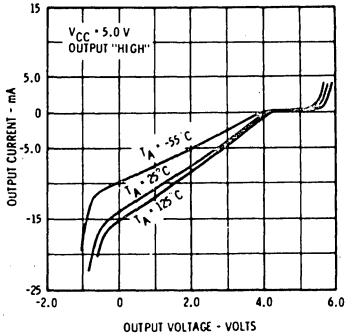
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



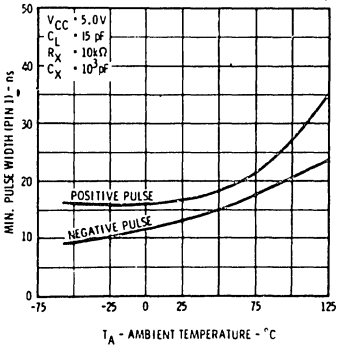
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



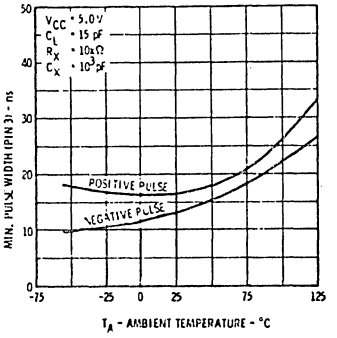
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



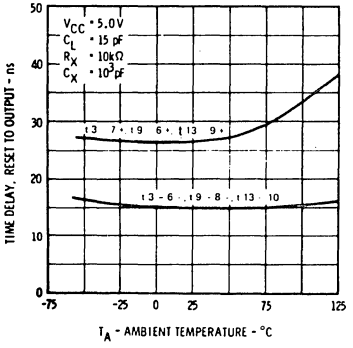
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)



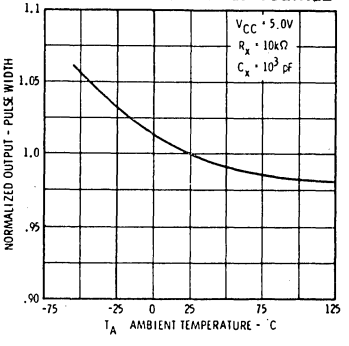
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)



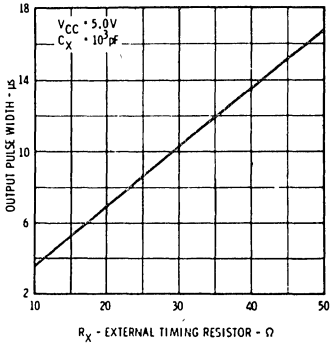
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE



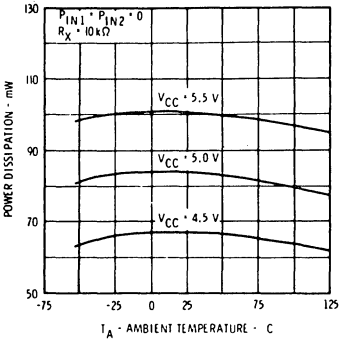
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



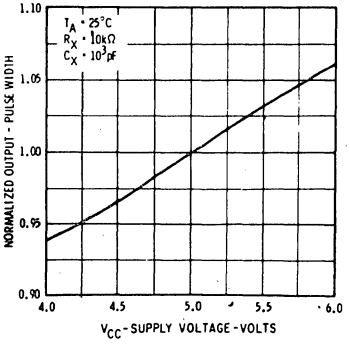
PULSE WIDTH VERSUS TIMING RESISTOR



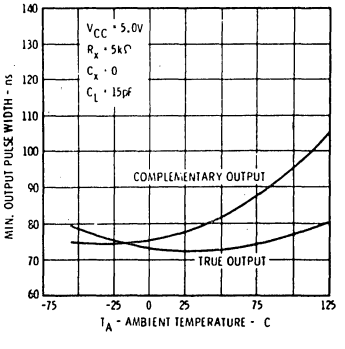
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



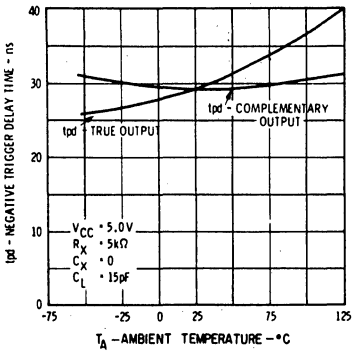
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

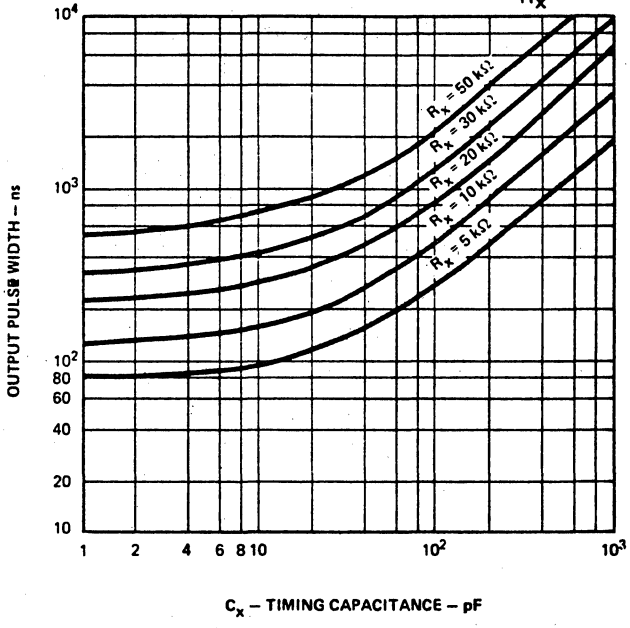


NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR Cx<10₃ pF

For $C_x \geq 10^3$ pF, $t_{pw} = 0.31\ R_xC_x\ (1 + \frac{1}{R_x})$



LOADING RULES
TTuL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

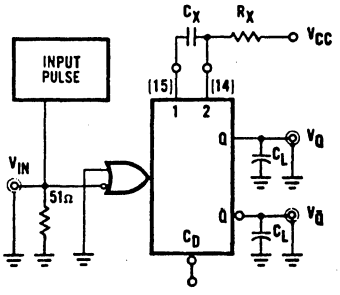
1 U.L. = 1 TTL Gate Input Load

TRIGGERING TRUTH TABLES

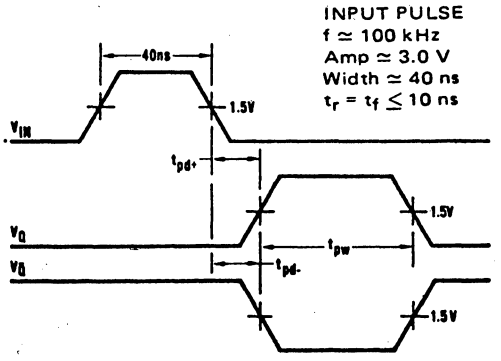
PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

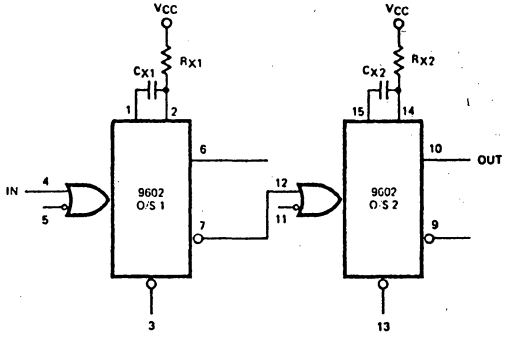
SWITCHING CIRCUITS AND WAVEFORMS

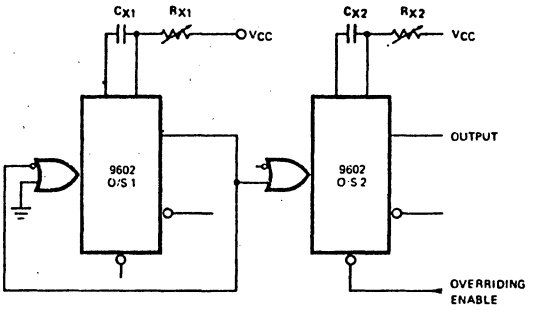


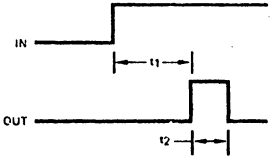
V_{CC} = Pin 16
GND = Pin 8

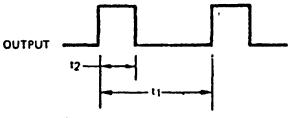


APPLICATIONS









The first one-shot determines the time t_1 before the initiation of the output pulse. The second one-shot determines t_2 the output pulse width.

PULSE GENERATOR

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. O/S 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while O/S 2 extends the pulse width to the required value.

Package: Dual In-Line and Flat Pack

DTL DUAL FOUR-INPUT GATE

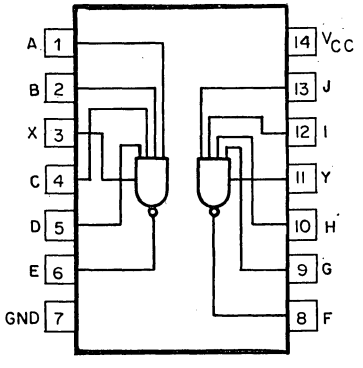
FAST DTL DUAL FOUR-INPUT GATE

The ITT930 and ITT961 elements are dual four-input NAND/NOR gates.

In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function. Both gate inputs may be extended using ITT933 elements to allow increased fan-in.

The ITT930 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT961 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.



Pinout: Dual In-Line and Flat Pack

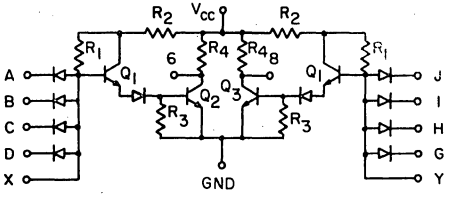
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES

R_1 = 2.0 K
R_2 = 1.75 K
R_3 = 5.0 K
R_4 = 6.0 K (930)
R_4 = 2.0 K (961)

ITT930 DTL DUAL FOUR-INPUT GATE
ITT961 FAST DTL DUAL FOUR-INPUT GATE

ELECTRICAL CHARACTERISTICS ITT930-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+125°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.18$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16		−0.93	−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"					3.25 1.47			mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10		80 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$ $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT930-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	LIMITS 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} (Per Gate)	Power Drain Current					4.0			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					4.0			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10		80 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$ $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT961-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.54$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 10.8$ mA $V_{CC} = 5.5V$, $I_{OL} = 13.5$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5V$, $V_F = 0.4V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open $V_{CC} = 5.0V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT961-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	4.3		4.3			4.2		Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage		0.5			0.5		0.55	Volts	$V_{CC} = 5.0V$, $I_{OL} = 10.5$ mA $V_{CC} = 5.0V$, $I_{OL} = 10.2$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current				1.85	3.68			mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} (Per Gate)	Power Drain Current					5.9			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					2.86			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+}	Turn Off Delay				10	50			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay				10	30			ns	$V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ITT SEMICONDUCTORS

Package: Dual In-Line and Flat Pack

DUAL FOUR-INPUT BUFFER

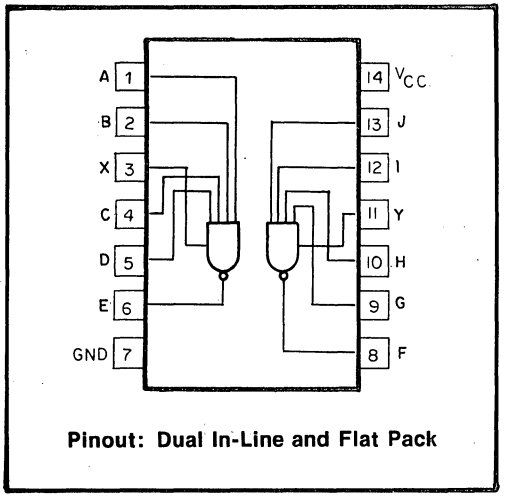
DUAL FOUR-INPUT POWER GATE

The ITT932 and ITT944 elements are dual four-input NAND/NOR buffer and power gates respectively.

Both elements have typical output currents of up to 100 ma. This enables them to provide much higher fan-out than a typical NAND/NOR gate. Both elements are extendable. The ITT932 incorporates an emitter follower pull-up which combines high fan-out with superior capacitance driving capability.

The ITT932 cannot be externally connected to perform the "wired OR" logic function. The ITT944, which does not incorporate the emmitter pull-up, can be used either as a high fan-out interface driver or low power lamp driver. The output can be tied to an external pull-up resistor and returned to a supply voltage of up to 12 volts. The supply may be located near the output or at the far end of an open transmission line or twisted pair interconnection. This allows the ITT944 to be used as a line driver.

The ITT944 can be externally connected to perform the "wired OR" logic function.



Pinout: Dual In-Line and Flat Pack

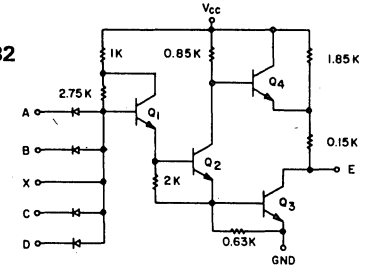
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1.0 sec.	+12 Volts
Output Current, Into Outputs, Continuous	150 mA
Output Current, Into Outputs, Pulsed, <30 milliseconds	300 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°C

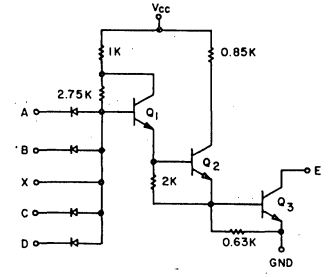
NOTES: 1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC (ONE GATE ONLY)

ITT932



ITT944



attachment and thermal paths thru leads, as well as number of soldered leads.

ITT932, DUAL FOUR—INPUT BUFFER
ITT944 DUAL FOUR—INPUT POWER GATE

ELECTRICAL CHARACTERISTICS ITT932-1 (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.5V, Inputs at V_{IL} (See Below); I_{OH} = −2.0 mA at −55°C, = −2.5 mA at 25°C, = −4.0 mA at 125°C
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 36 mA; V_{CC} = 5.5V, I_{OL} = 37.5 mA; Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5			−1.5		−1.4	mA	V_{CC} = 5.5V, V_F = 0.4V
			−1.16			−1.16		−1.08	mA	V_{CC} = 4.5V, V_F = 0.4V
I_R	Input Leakage Current					2.0		5.0	μA	V_R = 4.0V, Other inputs grounded
I_{PD} (per gate)	V_{CC} Current "Gate On"					13.3			mA	V_{CC} = 5.0V, Inputs Open
	V_{CC} Current "Gate Off"					1.47			mA	V_{CC} = 5.0V, Inputs Grounded
t_{pd+}	Turn Off Delay				25	80			ns	V_{CC} = 5.0V, R_L = 510Ω, C_L = 500pf,
t_{pd-}	Turn On Delay				15	40			ns	R_L = 150Ω, C_L = 500pf

ELECTRICAL CHARACTERISTICS ITT932-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 5.0V, Inputs at V_{IL} (See Below); I_{OH} = −2.0 mA at 0°C, = −2.5 mA at 25°C, = −3.0 mA at 75°C
V_{OL}	Output Low Voltage		0.45			0.45			Volts	V_{CC} = 5.0V, I_{OL} = 36 mA
								0.5		V_{CC} = 5.0V, I_{OL} = 34 mA; Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.4			−1.4			mA	V_{CC} = 5.0V, V_F = 0.45V
								−1.33	mA	V_{CC} = 5.0V, V_F = 0.5V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_R = 4.0V, Other inputs grounded
I_{PD}	V_{CC} Current "Gate On"					30.0			mA	V_{CC} = 5.0V, Inputs Open
I_{MAX}	Maximum V_{CC} Current					8.0			mA	V_{CC} = 8.0V, Inputs Grounded
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 5.0V
I_{SC}	Output Short Circuit Current	15.0		16.0			14.0		mA	V_{CC} = 5.0V, V_{OUT} = GND
t_{pd+}	Turn Off Delay				25	80			ns	V_{CC} = 5.0V, R_L = 510Ω, C_L = 500pf,
t_{pd-}	Turn On Delay				15	40			ns	R_L = 150Ω, C_L = 500pf

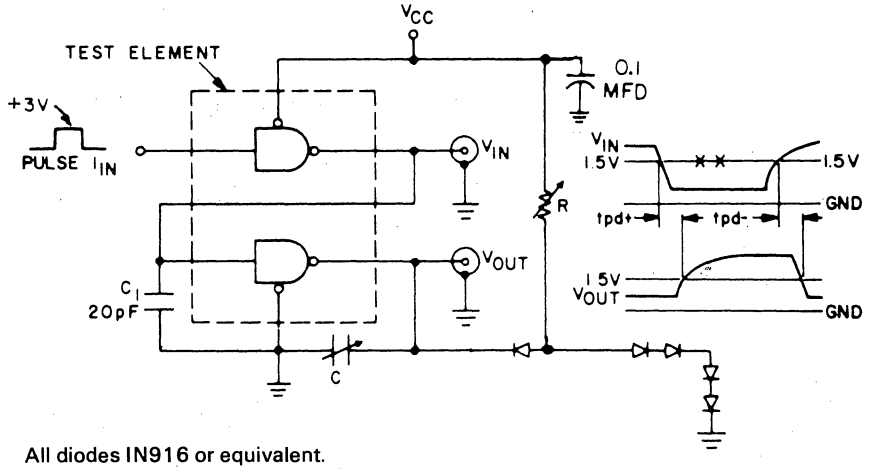
ELECTRICAL CHARACTERISTICS ITT944-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 36$ mA $V_{CC} = 5.5V$, $I_{OL} = 37.5$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_{CEX}	Output Leakage		50			100		200	μA	$V_{CEX} = 4.5V$ Inputs at V_{IL} (See Above)
I_F	Input Load Current		−1.5 −1.16			−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, $V_F = 0.4V$
I_R	Input Leakage Current					2.0*		5.0	μA	$V_R = 4.0V$ Other Inputs Grounded
I_{PD}	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"					20 2.94			mA mA	$V_{CC} = 5.0V$, Inputs Open $V_{CC} = 5.0V$, Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			15 10		50 35			ns ns	$V_{CC} = 5.0V$, $R_L = 510\Omega$, $C_L = 20pf$ $R_L = 150\Omega$, $C_L = 100pf$

ELECTRICAL CHARACTERISTICS ITT944-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

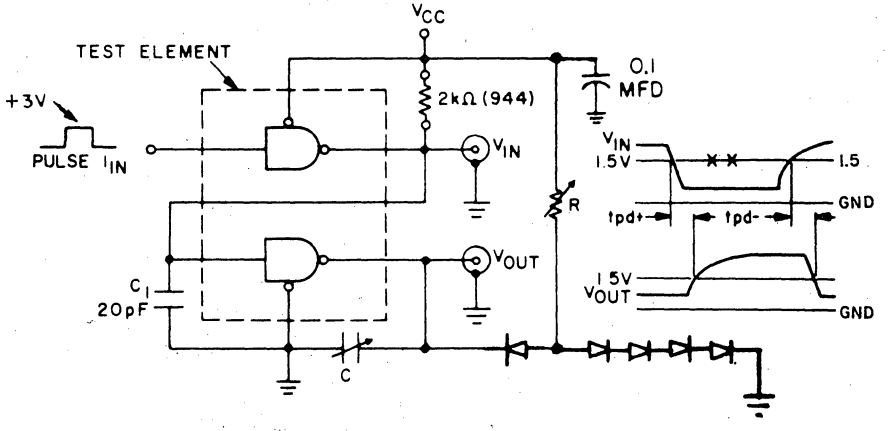
Symbol	Characteristic	0°C Min.	Max.	+75°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OL}	Output Low Voltage		0.45			0.45		0.5	Volts	$V_{CC} = 5.0V$, $I_{OL} = 36$ mA $V_{CC} = 5.0V$, $I_{OL} = 34$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_{CEX}	Output Leakage					100			μA	$V_{CEX} = 5.0V$ Inputs at V_{IL} (See Above)
I_F	Input Load Current		−1.4			−1.4		−1.33	mA mA	$V_{CC} = 5.0V$, $V_F = 0.45V$ $V_{CC} = 5.0V$, $V_F = 0.5V$
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_R = 4.0V$ Other Inputs Grounded
I_{PD}	V_{CC} Current "Gate On"					20.0			mA	$V_{CC} = 5.0V$, Inputs Open
I_{MAX}	Maximum V_{CC} Current					6.0			mA	$V_{CC} = 8.0V$, Inputs Grounded
LV_{CE}	Output Latching Voltage			6.0					Volts	$I_{CE} = 5.0$ mA, $V_{CC} = 5.0V$
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			15 10		50 35			ns ns	$V_{CC} = 5.0V$, $R_L = 510\Omega$, $C_L = 20pf$ $R_L = 150\Omega$, $C_L = 100pf$

TPD TEST CIRCUIT FOR ITT932



All diodes IN916 or equivalent.
C_1 and C includes probe and jig capacitance.

TPD TEST CIRCUIT FOR ITT944



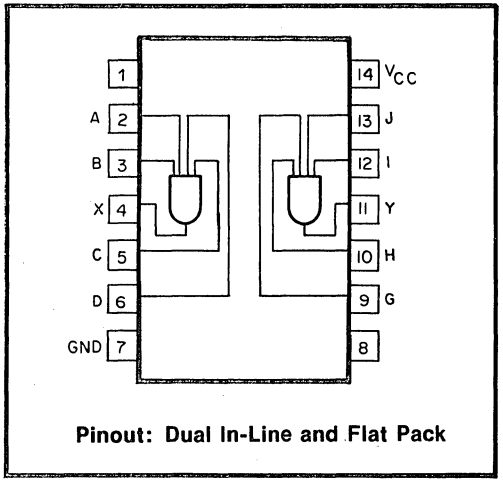
C_1 and C includes probe and jig capacitance.

Package: Dual In-Line and Flat Pack

DUAL FOUR-INPUT EXTENDER

The ITT933 element is a dual four-input extender. The ITT933 consists of two independent diode arrays identical in every respect to the input diodes of the DTL gates and buffer elements. It can be used to extend the fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the elements to which they are connected. Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The ITT933 has a typical input capacitance of 2pf and an output capacitance of 5pf.

The ITT933 can extend the fan-in of the ITT930, 932, 944, and 901 elements.



Pinout: Dual In-Line and Flat Pack

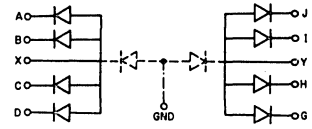
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1.0 sec	+12 Volts
Output Current, Into Inputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt o_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt O_{J-C} for TO-5; 180°C/Watt O_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS 933

Symbol	Characteristics	Limits 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
I_R	Input Leakage Current		5.0			5.0		10.0	A	V_R = 4.0V Ground on other inputs
V_{FD}	Forward Diode Voltage	0.700	0.900	0.660		0.840	0.560	0.760	Volts	I_F = 2.0 mA

Symbol	Characteristics	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
I_R	Input Leakage Current		2.0			2.0		5.0	A	V_R = 4.0V Ground on other inputs
V_{FD}	Forward Diode Voltage	0.840	0.980	0.700		0.820	0.480	0.620	Volts	I_F = 2.0 mA

ITT SEMICONDUCTORS

Package: Dual In-Line and Flat Pack

EXTENDABLE HEX INVERTER
HEX SINGLE-INPUT GATE
FAST HEX SINGLE-INPUT GATE
OPEN COLLECTOR HEX INVERTER

The ITT935, ITT936, and ITT937 elements are hex single-input inverters.

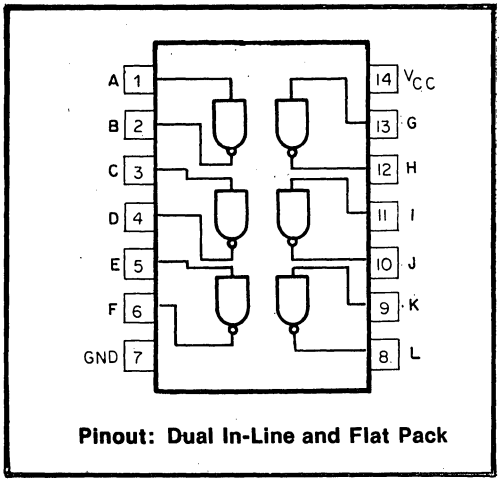
The ITT935 is intended for use with discrete diode expansion of the input. When extending inputs with diodes, care should be taken to minimize capacitance on the input node.

These inverter gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

The ITT936 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

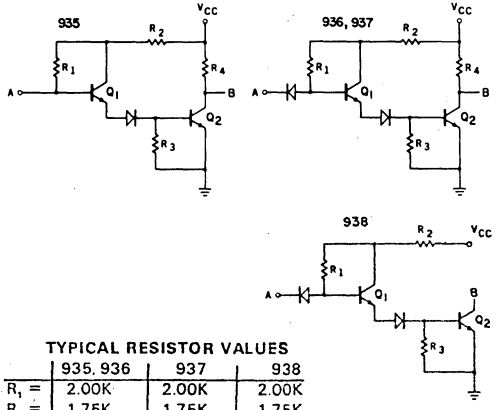
The ITT937 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

The ITT938 has uncommitted collector outputs, making the device useful as a lamp driver or other interface element.



Pinout: Dual In-Line and Flat Pack

CIRCUIT SCHEMATICS (ONE GATE ONLY)



TYPICAL RESISTOR VALUES

	935, 936	937	938
R_1 =	2.00K	2.00K	2.00K
R_2 =	1.75K	1.75K	1.75K
R_3 =	5.00K	5.00K	5.00K
R_4 =	6.00K	2.00K	

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Current	5 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F
Output Voltage (938)	25 Volts

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

ITT935 EXTENDABLE HEX INVERTER
ITT936 HEX SINGLE-INPUT GATE
ITT937 FAST HEX SINGLE-INPUT GATE
ITT938 OPEN COLLECTOR HEX INVERTER

ELECTRICAL CHARACTERISTICS ITT935-1 (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5			2.6		2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.18 mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.4			0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12 mA V_{CC} = 5.5V, I_{OL} = 15 mA Inputs at V_{IH}
V_{IH}	Input High Voltage	3.29		2.6			2.21		Volts	Guaranteed Input High Threshold
V_{IL}	Input Low Voltage		2.32			1.7		1.01	Volts	Guaranteed Input Low Threshold
I_F	Input Load Current		−1.5			−1.5		−1.5	mA	V_{CC} = 5.5V, V_F = 1.0V At 25°C, V_F = 1.16V At −55°C, V_F = 0.81V At 125°C
			−1.2			−1.2		−1.2	mA	V_{CC} = 4.5V
I_{PD}*	V_{CC} Current "Gate On"					3.1			mA	V_{CC} = 5.0V, Inputs Open
	V_{CC} Current "Gate Off"					1.7			mA	V_{CC} = 5.0V, Inputs Grounded
t_{pd+}*	Turn Off Delay				25	80			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay				10	40			ns	V_{CC} = 5V, R_L = 400, C_L = 50pf

* (per gate)

ELECTRICAL CHARACTERISTICS ITT935-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage		2.6			2.6		2.5	Volts	V_{CC} = 5.0V I_{OH} = −.120 mA Inputs at V_{IL}
V_{OL}	Output Low Voltage		0.45			0.45		0.5V	Volts	V_{CC} = 5.0V, I_{OL} = 12 mA V_{CC} = 5.0V, I_{OL} = 11.4 mA Inputs at V_{IH}
V_{IH}	Input High Voltage	2.75		2.6			2.37		Volts	Guaranteed Input High Threshold
V_{IL}	Input Low Voltage		1.9			1.7		1.47	Volts	Guaranteed Input Low Threshold
I_F	Input Load Current		−1.5			−1.5		−1.5	mA	V_{CC} = 5.0V, V_F = 1.05V at +25° V_F = 1.1V at 0°, V_F = 0.97V at +75°
I_{PDH}	V_{CC} Current "Gate On"					3.7			mA	V_{CC} = 5.0V, Inputs Open
I_{MAX}	V_{CC} Current, Maximum					3.0			mA	V_{CC} = 8.0V, Inputs GND
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	V_{CC} = 5.0V V_{OUT} = GND
I_{CEX}	Output Leakage Current					100			µA	V_{CC} = V_{CEX} = 5.0V
t_{pd+}	Turn Off Delay				25	80			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay				15	40			ns	V_{CC} = 5V, R_L = 400 Ω, C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT936-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.18$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16		−1.2 −0.93	−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"				2.41 1.15	3.25 1.47			mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10	45 20	80 30			ns ns	$V_{CC} = 5.0V$, $R_L = 3.9K$, $C_L = 30pf$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT936-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	LIMITS 0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	µA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			µA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} (Per Gate)	Power Drain Current					4.0			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					4.0			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10		80 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400\ \Omega$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT937-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5V, I_{OH} = -0.54$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5V, I_{OL} = 10.8$ mA $V_{CC} = 5.5V, I_{OL} = 13.5$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5V$, $V_F = 0.4V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	$V_{CC} = 5.5V, V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open $V_{CC} = 5.0V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5V, R_L = 3.9K, C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V, R_L = 400\ \Omega, C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT937-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	4.3		4.3			4.2		Volts	$V_{CC} = 5.0V, I_{OH} = -.12$ mA
V_{OL}	Output Low Voltage		0.5			0.5		0.55	Volts	$V_{CC} = 5.0V, I_{OL} = 10.5$ mA $V_{CC} = 5.0V, I_{OL} = 10.2$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$
I_R	Input Leakage Current		5.0			5.0		10.0	µA	$V_{CCC} = 5.0V, V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current			1.85		3.68			mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			µA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD}	Power Drain Current (Per Gate)					5.9			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX}	Max V_{CC} Current (Per Gate)					2.86			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5V, R_L = 3.9K, C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V, R_L = 400, C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT938-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
I_{CEX}	Output Leakage Current		50			100		200	A	$V_{CC} = 4.5V$, $V_{CEX} = 4.5V$ Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16			−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"					3.25 1.47			mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded
t_{pd+}	Turn Off Delay			25		80			ns	$V_{CC} = 5.0V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10		30			ns	$R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT938-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	LIMITS 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0	1.0	1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	µA	$V_{CCC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
LV_{CE}	Output Latching Voltage			6.0						$V_{CC} = 5.0V$, $I_{CF} = 5.0$mA
I_{CEX}	Output Leakage Current		50			100		200	µA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD}	Power Drain Current (Per Gate)					4.0			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX}	Max V_{CC} Current (Per Gate)					4.0			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+}	Turn Off Delay			25		80			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10		30			ns	$V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

Package: Dual In-Line and Flat Pack

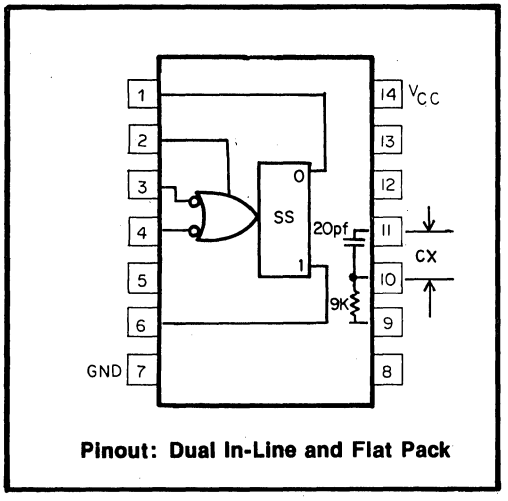
MONOSTABLE MULTIVIBRATOR

The ITT941/951 is a monostable multivibrator. These circuits are identical with the exception of 3 input clamp diodes on ITT941.

The ITT941/951 provides a pair of complementary output pulses which are typically 100 nsec wide when it is triggered with an external pulse. The width of the output pulse is adjustable to greater than 100ns by the addition of an external resistor and/or capacitor.

The output pulse width is very stable as either power supply voltage or temperature are varied when an external timing resistor is used instead of the internal diffused resistor.

This circuit is very useful in providing DTL compatible pulses from other sources.



Pinout: Dual In-Line and Flat Pack

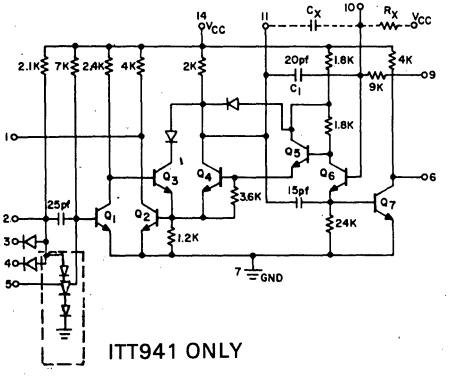
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−0.5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	50 mA
Current Into Pin 10	5 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Lead Temp. (soldering, 60 sec.)	300°C
Input Voltage Applied To Input	−1.5 to +5.5 Volts

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC



ITT941 ONLY

Rules For Use Of ITT951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 100 ns.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: T 4.5(C_X = 20) with C_X in pF and T in ns.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9.0k minimum to 15k maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: T 0.5 R_X (C_X = 20) with R_X in k , C_X in pF and T in ns.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2.0k resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.
6. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10k resistor between Pin 5 and V_{CC}.
7. For pulse widths greater than 1.0 s, Pin 1 should be used as the output and inverted if required.
8. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground

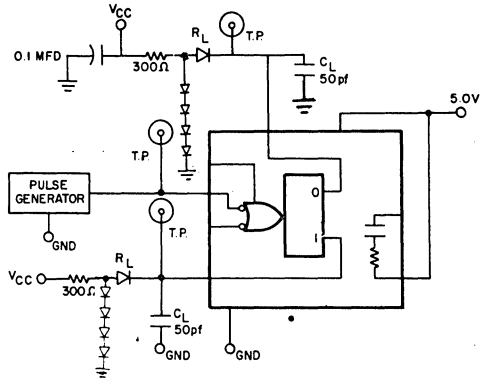
ELECTRICAL CHARACTERISTICS ITT941-1,ITT951-1 (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%)

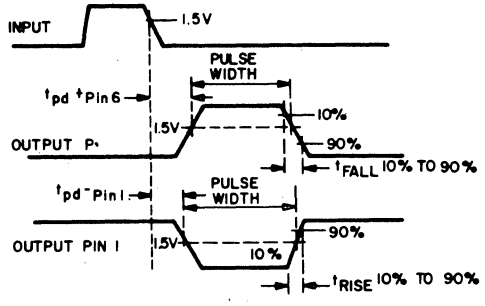
		Limits								
		−55°C		+25°C			+125°C			
Symbol	Characteristic	Min.	Max.	Min	Typ.	Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.5			2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.18 mA
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 5.5V, I_{OL} = 15 mA V_{CC} = 4.5V, I_{OL} = 15 mA
I_{PDL}	Power Dissipation Current With Inputs Grounded					9.0			mA	V_{CC} = 5.0V, Inputs = Gnd. Pin 9 Connected to Pin 14
I_F	Input Load Current		−2.93			−2.93		−2.75	mA	V_{CC} = 5.5V, V_F = 0.4V
			−2.26			−2.26		−2.22	mA	V_{CC} = 4.5V, V_F = 0.4V
I_R	Input Leakage Current		5.0			5.0		10.0	μA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
t_{pd+}	Turn Off Delay					40			ns	Pin 6 V_{CC} = 5.0V
t_{pd-}	Turn On Delay					40			ns	Pin 1
PW	Pulse Width									
	941			90		330			ns	Pin 1
				70		330			ns	Pin 6
	951			90		220			ns	Pin 1
				70		160			ns	Pin 6

ELECTRICAL CHARACTERISTICS ITT941-5 ITT951-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	Limits 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	3.2		3.2			3.2		Volts	V_{CC} = 5.0V, I_{OH} = −0.15 mA
V_{OL}	Output Low Voltage		0.5			0.45			Volts	V_{CC} = 5.0V, I_{OL} = 14.8 mA
								0.5		V_{CC} = 5.0V, I_{OL} = 14.0 mA
I_{PDL}	Power Dissipation Current With Inputs Grounded					11.8			mA	V_{CC} = 5.0V, Inputs = Gnd. Pin 9 Connected to Pin 14
I_F	Input Load Current	0.65	−2.6	0.6		−2.8			mA	V_{CC} = 5.0V, V_F = 0.45V
							0.65	−2.66	mA	V_{CC} = 5.0V, V_F = 0.5V
I_R	Input Leakage Current		5.0			5.0		10.0	μA	V_{CC} = 5.5V, V_R = 4.0V Pin 2 = Gnd
t_{pd+}	Turn Off Delay					40			ns	Pin 6 V_{CC} = 5.0V
t_{pd-}	Turn On Delay					40			ns	Pin 1
PW	Pulse Width									
	941			90		330			ns	Pin 1
				70		270			ns	Pin 6
	951			90		330			ns	Pin 1
				70		270			ns	Pin 6
I_{MAX}	Maximum V_{CC} Current					23.1			mA	V_{CC} = 8.0V, Inputs Gnd

SWITCHING TIME AND PULSE WIDTH TEST CIRCUIT





Package: Dual In-Line and Flat Pack

CLOCKED FLIP-FLOP

The ITT945 and ITT948 elements are clocked flip-flops.

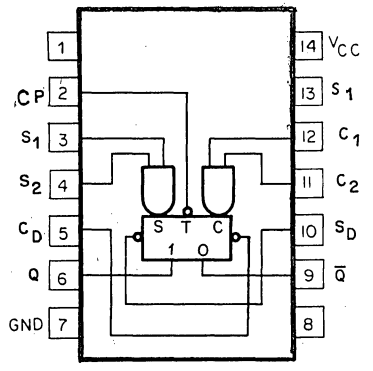
Both the ITT945 and ITT948 flip-flops operate on the "master-slave" principle. Information enters the "master" flip-flop when trigger clock input voltage is high and transfers to the "slave" flip-flop when trigger clock input voltage goes low. Since operation depends only on voltage levels any sort of waveshape having the proper voltage levels may be used as a trigger signal. (The rise and fall times are irrelevant.)

Both the ITT945 and ITT948 have an improved direct set and direct clear design which allow unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset counters or control flip-flops.

Both flip-flops incorporate output buffers which provide isolation between the "slave" flip-flop and the output load, thereby enhancing immunity to signal line noise.

The ITT945 incorporates a 6K ohm output pull up resistor which allows for a fan-out of up to 12 DTL loads.

The ITT948 incorporates a 2K ohm output pull up resistor which allows for typically 30% faster rise times for capacitive loads at a fan-out of up to 11 DTL loads.

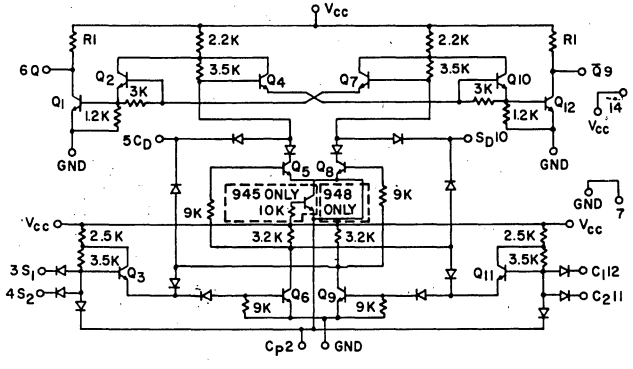


Pinout: Dual In-Line and Flat Pack

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

CIRCUIT SCHEMATIC



NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

NOTES: Pins 1, 8, 13 not used
945, R_1 = 6K
948, R_1 = 2K

ITT945, ITT948
CLOCKED FLIP-FLOPS

SYNCHRONOUS ENTRY

Inputs t_n				Output $t_n + 1$
3	4	11	12	6
0	Φ	0	Φ	NC
0	Φ	Φ	0	NC
Φ	0	0	Φ	NC
Φ	0	Φ	0	NC
0	Φ	1	1	0
Φ	0	1	1	0
1	1	0	Φ	1
1	1	Φ	0	1
1	1	1	1	Undeter-mined

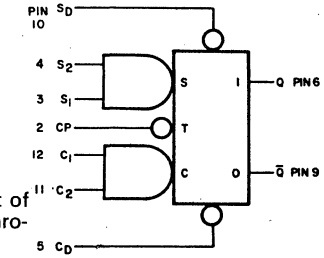
For J-K Mode Operation:
Connect 4 to 9 and 11 to 6

ASYNCHRONOUS ENTRY

Inputs		Outputs	
5	10	6	0
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

Asynchronous entry is independent of all other inputs and overrides synchronous entry.

POSITIVE LOGIC SYMBOLS



NC = no change, the trigger-pulse has equal effect.
0 = low, the more negative voltage level.
1 = high, the more positive voltage level
(In all cases, unused pins have the same effect as high.)
Φ = immaterial, either 1 or 0 has no effect on outputs.

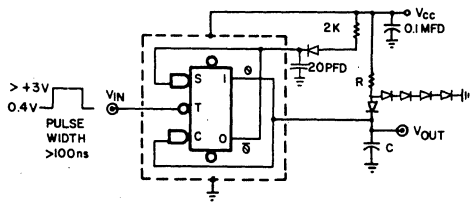
ELECTRICAL CHARACTERISTICS ITT945-1,ITT948-1(T_A = −55°C to +125°C, V_{CC} = 5.0V±10%)

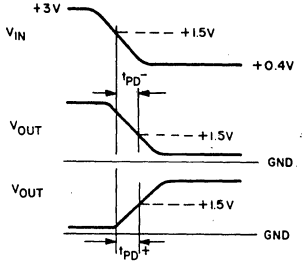
Symbol	Characteristic	Limits −55°C Min.	Max	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage									
	945	2.5		2.5			2.5		Volts	V_{CC} = 4.5V, I_{OH} = −180 µA
	948	2.5		2.5			2.5			V_{CC} = 4.5V, I_{OH} = −540 µA
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12.0 mA
	945									V_{CC} = 5.5V, I_{OL} = 15.0 mA
	948		0.4			0.4		0.4		V_{CC} = 4.5V, I_{OL} = 13.0 mA (at −55°C)
										V_{CC} = 5.5V, I_{OL} = 13.6 mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_R	Input Leakage, all J,K S,C,S_D,C_D, inputs					2.0		5.0	µA	V_{CC} = 5.5V, V_R = 4.0V Gnd on other inputs
I_{RCP}	Input Leakage, CP inputs					10		20	µA	V_{CC} = 4.0V, V_R = 4.0V Gnd on other inputs
I_F	Input Current, all J,K,S,C inputs		−.98			−.98		−.92	mA	V_{CC} = 5.5V, V_F = 0.4V 4.0V on other inputs
	Input Current, 945		−2.93			−2.93		−2.57		
	CP inputs 948		−2.35			−2.35		−2.03		
I_F	Input Current, all J,K,S,C inputs		−0.76		−0.62	−0.76		−0.72	mA	V_{CC} = 4.5V, V_F = 0.4V 4.0V on other inputs
	Input Current, 945		−2.26			−2.26		−2.02		
	CP inputs 948		−1.83			−1.83		−1.59		
I_{FSI}	Input Current, C_D,		−2.93			−2.93		−2.57	mA	V_{CC} = 5.5V, V_F = 0.4V
	S_D inputs		−2.26			−2.26		−2.20		V_{CC} = 4.5V, 4.0V on other inputs
I_{PD}	V_{CC} Current 945					14.0			mA	V_{CC} = 5.0V, all inputs open
	948					16.2				
t_{pd+}	Turn Off Delay 945		35			75			ns	V_{CC} = 5.0V
	948		30			65				R_L = 2.0K, C_L = 30pf
t_{pd-}	Turn On Delay 945		30			75			ns	R_L = 330 Ω, C_L = 50pf
	948		30			75				

ELECTRICAL CHARACTERISTICS ITT945-5,ITT948-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage 945	2.6		2.6			2.5		Volts	V_{CC} = 5.0V, I_{OH} = −120 µA
	948	4.3		4.3			4.2			V_{CC} = 5.0V, I_{OH} = −120 µA
V_{OL}	Output Low Voltage		0.45		0.45					V_{CC} = 5.0V, I_{OL} = 16.8 mA
	945		0.45		0.45				Volts	V_{CC} = 5.0V, I_{OL} = 16.0 mA
	948							0.5		V_{CC} = 5.0V, I_{OL} = 15.4 mA
								0.5		V_{CC} = 5.0V, I_{OL} = 14.6 mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1			0.8	Volts	Guaranteed input low threshold for all inputs
I_R	Input Leakage, all J-K S, C, S_D, C_D inputs		5.0		5.0			10.0	µA	V_{CC} = 5.0V, V_R = 4.0V Gnd on other inputs
I_{RCP}	Input Leakage, CP inputs		10.0		10.0			20.0	µA	V_{CC} = 4.0V, V_R = 4.0V GND on other inputs
I_F	Input Current, all J,K,S,C inputs		−0.95		−0.95			−0.90	mA	V_{CC} = 5.0V, V_F = 0.4V 4.0V on other inputs
	Input Current, CP Inputs									
	945		−2.8		−2.8			−2.66		
	948		−2.24		−2.24			−2.13		
I_{FSI}	Input Current, C_D, S_D inputs		−2.8		−2.8			−2.66	mA	
I_{PD}	V_{CC} Current 945							15.0	mA	V_{CC} = 5.0V, Inputs Open
	948							17.5		
I_{cex}	Output Leakage Current				100.0				µA	V_{CC} = V_{cex} = 5.0V
I_{SC}	Output Short Circuit Current									
	945	0.59	1.41	0.59	1.41		0.55	1.38	mA	V_{CC} = 5.0V
	948	1.77	4.2	1.77	4.2		1.6	4.0		V_{OUT} = GND
I_{MAX}	Maximum V_{CC} Current									V_{CC} = 8.0 , All inputs GND
	945				17.0				mA	
	948				17.5					
t_{pd+}	Turn Off Delay 945				35	75			ns	V_{CC} = 5.0V
	948				30	65				R_L = 2.0K, C_L = 30pf
t_{pd-}	Turn On Delay 945				30	75			ns	R_L = 330 Ω C_L = 50pf
	948				30	75				

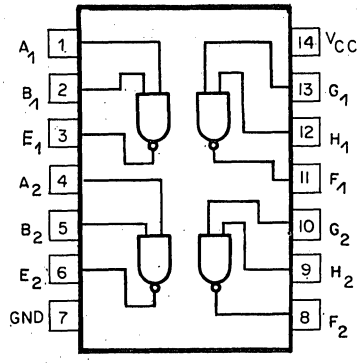
tpd TEST CIRCUIT





QUAD TWO-INPUT GATE

FAST QUAD TWO-INPUT GATE



Pinout: Dual In-Line and Flat Pack

The ITT946 and ITT949 elements are quad two-input NAND/NOR gates.

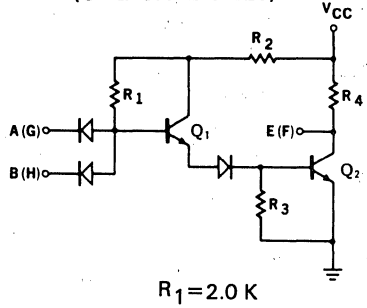
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These quad two-input gates can also be wired to perform the "exclusive OR" function, while two elements can be wired together to form a full adder.

The ITT946 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT949 incorporates a 2K output pull-up resistor which allows for typically 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

CIRCUIT SCHEMATIC (ONE GATE ONLY)



TYPICAL RESISTOR VALUES

$R_1 = 2.0$ K
$R_2 = 1.75$ K
$R_3 = 5.0$ K
$R_4 = 6.0$ K (946)
$R_4 = 2.0$ K (949)

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt O_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt O_{J-C} for TO-5; 180°C/Watt O_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

ELECTRICAL CHARACTERISTICS ITT946-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

		Limits							
		−55°C		+25°C		+125°C			
Symbol	Characteristic	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.18 mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12 mA V_{CC} = 5.5V, I_{OL} = 15 mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	V_{CC} = 5.5V, V_F = 0.4V
			−1.16		−0.93	−1.16		−1.08	mA	V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.25			mA	Inputs Open V_{CC} = 5.0V
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			25	45	80			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay			10	20	30			ns	V_{CC} = 5V, R_L = 400 C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT946-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

		LIMITS								
		0°C		+25°C			+75°C			
Symbol	Characteristics	Min.	Max.	Min	Typ.	Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	V_{CC} = 5.0V, I_{OH} = −12 mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	V_{CC} = 5.0V, I_{OL} = 12 mA V_{CC} = 5.0V, I_{OL} = 11.4 mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4			mA	V_F = 0.45V, V_{CC} = 5.0V
								1.33	mA	V_F = 0.5V, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	V_{CC} = 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 5.0V
I_{PD} (Per Gate)	Power Drain Current					4.0			mA	V_{CC} = 5.0V Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					4.0			mA	V_{CC} = 8.0V Inputs Gnd
t_{pd+}	Turn Off Delay			25		80			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay			10		30			ns	V_{CC} = 5V, R_L = 400 C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT949-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

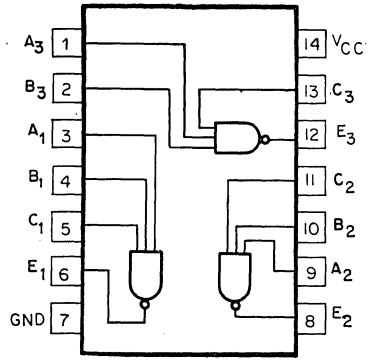
Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.54$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 10.8$ mA $V_{CC} = 5.5V$, $I_{OL} = 13.5$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5V$, $V_F = 0.4V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	A	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open $V_{CC} = 5.0V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V$, $R_L = 400$ $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT949-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

		0°C	+25°C		+75°C		
V_{OH}	Output High Voltage	4.3	4.3		4.2	Volts	$V_{CC} = 5.0V$, $I_{OH} = -12$ mA
V_{OL}	Output Low Voltage			0.5		Volts	$V_{CC} = 5.0V$, $I_{OL} = 10.5$ mA
					0.55		$V_{CC} = 5.0V$, $I_{OL} = 10.2$ mA
V_{IH}	Input High Voltage	2.0	1.9		1.8	Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage			1.1	0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current			1.4		mA	$V_F = 0.45V$ $V_{CC} = 5.0V$
					1.33		$V_F = 0.5V$ 4.0V on other inputs
I_R	Input Leakage Current	5.0		5.0	10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current		1.85	3.68		mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current			100		μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} (Per Gate)	Power Drain Current			5.9		mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current			2.86		mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+}	Turn Off Delay		25	50		ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay		10	30		ns	$V_{CC} = 5V$, $R_L = 400$ $C_L = 50pf$

TRIPLE THREE-INPUT GATE

FAST TRIPLE THREE-INPUT GATE



Pinout: Dual In-Line and Flat Pack

The ITT962 and ITT963 elements are triple three-input NAND/NOR gates.

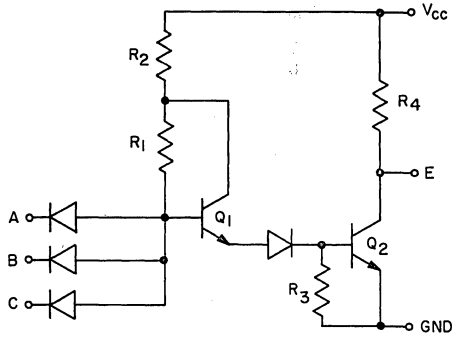
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These triple three-input gates can also be wired together to perform the "exclusive OR" function.

The ITT962 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT963 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

CIRCUIT SCHEMATIC (ONE GATE ONLY)



TYPICAL RESISTOR VALUES

$R_1 = 2.0$ K
$R_2 = 1.75$ K
$R_3 = 5.0$ K
$R_4 = 6.0$ K (962)
$R_4 = 2.0$ K (963)

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1.0 sec.	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

ITT962 TRIPLE THREE-INPUT GATE
ITT963 FAST TRIPLE THREE-INPUT GATE

ELECTRICAL CHARACTERISTICS ITT962-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.18$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5V$, $V_F = 0.4V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.25			mA	Inputs Open $V_{CC} = 5.0V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			25	45	80			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT962-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	LIMITS 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4			mA	$V_F = 0.45V$, $V_{CC} = 5.0V$
								1.33	mA	$V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	µA	$V_{CCC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			µA	$V_{CC} = V_{CEX} = 5.0V$
I_{PC} (Per Gate)	Power Drain Current					4.0			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					4.0			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+}	Turn Off Delay			25	45	80			ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$
t_{pd-}	Turn On Delay			10	20	30			ns	$V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT963-1 (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.54 mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 10.8 mA V_{CC} = 5.5V, I_{OL} = 13.5 mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current	1	−1.5		−1.2	−1.5		−1.4	mA	V_{CC} = 5.5V, V_F = 0.4V
			−1.16		−0.93	−1.16		−1.08	mA	V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open V_{CC} = 5.0V
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
$t_{pd}+$	Turn Off Delay			10	35	50			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
$t_{pd}-$	Turn On Delay			10	20	30			ns	V_{CC} = 5V, R_L = 400 , C_L = 50pf

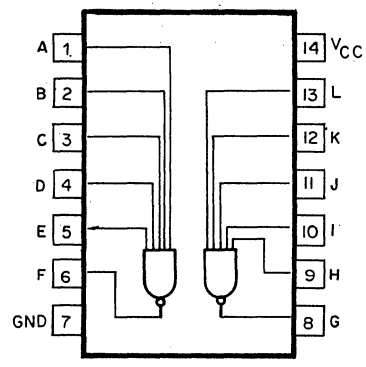
ELECTRICAL CHARACTERISTICS ITT963-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristics	LIMITS 0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	4.3		4.3			4.2		Volts	V_{CC} = 5.0V, I_{OH} = −0.12 mA
V_{OL}	Output Low Voltage		0.5			0.5		0.55	Volts	V_{CC} = 5.0V, I_{OL} = 10.5 mA V_{CC} = 5.0V, I_{OL} = 10.2 mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4			mA	V_F = 0.45V, V_{CC} = 5.0V
								1.33	mA	V_F = 0.5V 4.0V on other inputs
I_R	Input Leakage Current		5.0			5.0		10.0	µA	V_{CC}= 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current			1.85		3.68			mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			µA	V_{CC} = V_{CEX} = 5.0V
I_{PD} (Per Gate)	Power Drain Current					5.9			mA	V_{CC} = 5.0V Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					2.86			mA	V_{CC} = 8.0V Inputs Gnd
$t_{pd}+$	Turn Off Delay			10	35	50			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
$t_{pd}-$	Turn On Delay			10	20	30			ns	V_{CC} = 5V, R_L = 400 , C_L = 50pf

Package: Dual In-Line and Flat Pack

DTL DUAL FIVE INPUT GATE

The ITT1800 is a dual five input NAND/NOR gate. The device is similar to the ITT930 in all respects, except for the replacement of the expander node with a standard input diode.

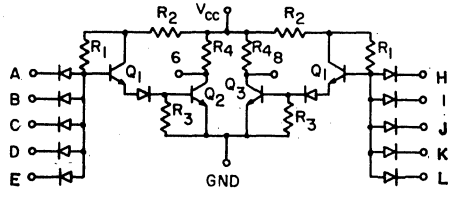


Pinout: Dual In-Line and Flat Pack

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, < 1	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125 °C
Storage Temperature	−65 to +150 °C
Operating Junction Temperature[2]	+175 °C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temperature (soldering, 60 sec	300 °F

CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES	R_1=2.0 K R_2=1.75 K R_3=5.0 K R_4=6.0 K

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

ITT1800
DTL DUAL FIVE INPUT Gate

ELECTRICAL CHARACTERISTICS ITT1800-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.18$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16			−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"					3.25 1.47			mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay				25 10	80 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT1800-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	0°C Min.	0°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	$V_{CC} = 5.0V$, $I_{OH} = -12$ mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PC} (Per Gate)	Power Drain Current					4.0			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} (Per Gate)	Max V_{CC} Current					4.0			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay				25 10	80 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400\Omega$, $C_L = 50pf$

Package: Dual In-Line and Flat Pack

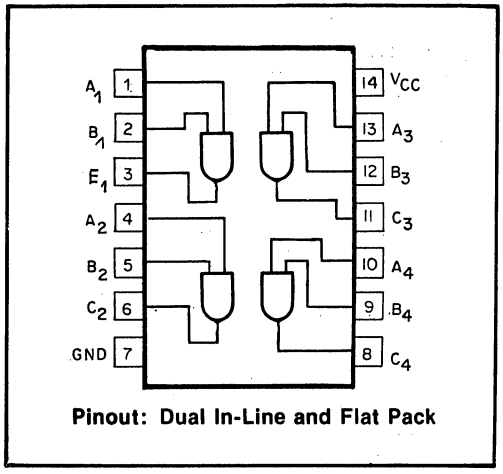
DTL QUAD TWO-INPUT AND GATE

FAST DTL QUAD TWO-INPUT AND GATE

The ITT1806 and 1807 perform the logical AND function. Thus the device can be used to expand the inputs of other DTL NAND, OR, or NOR gates, or flip flops, greatly simplifying logic design. As with all ITT DTL gates, the outputs can be tied together to perform the wire-AND function.

the ITT1806 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT1807 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.



Pinout: Dual In-Line and Flat Pack

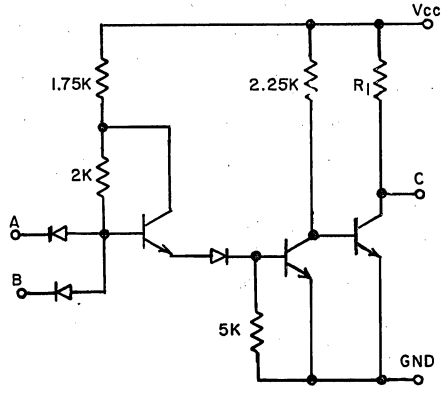
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt O_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt O_{J-C} for TO-5; 180°C/Watt O_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SCHEMATIC DIAGRAM — EACH GATE



R_I = 6K FOR 1806

R = 2K FOR 1807

ELECTRICAL CHARACTERISTICS ITT1807-1 (T_A = −55 C to +125 C, V_{CC} = 5.0V +10%)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.54 mA Inputs at V_{IH} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0 4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 10.8 mA V_{CC} = 5.5V, I_{OL} = 13.5 mA One Input at V_{IL} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	V_{CC} = 5.5V, V_F = 0.4V
			−1.16		−0.93	−1.16		−1.08	mA	V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	µA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD}	V_{CC} Current "Gate Off"					5.15			mA	Inputs Open V_{CC} = 5.0V
Per gate	V_{CC} Current "Gate On"					7.25			mA	Inputs Grounded
t_{pd+}	Turn Off Delay					65			ns	V_{CC} = 5V, R_L = 3.9K C_L = 30pf
t_{pd-}	Turn On Delay					65			ns	V_{CC} = 5V, R_L = 400 Ω, C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT1807-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	4.3		4.3			4.2		Volts	V_{CC} = 5.0V, I_{OH} = −0.12 mA Inputs at V_{IH}
V_{OL}	Output Low Voltage		0.5			0.5		0.55	Volts	V_{CC} = 5.0V, I_{OL} = 10.5 mA V_{CC} = 5.0V, I_{OL} = 10.2 mA One Input at V_{IL}
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA	V_F = 0.45V, V_{CC} = 5.0V V_F = 0.5V
I_R	Input Leakage Current		5.0			5.0		10.0	µA	V_{CC}= 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current				1.85	3.68			mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			µA	V_{CC} = V_{CEX} = 5.0V
I_{PD} Per gate	Power Drain Current					7.75			mA	V_{CC} = 5.0V Inputs GND
I_{MAX} Per gate	Max V_{CC} Current					9.75			mA	V_{CC} = 8.0V Inputs Open
t_{pd+}	Turn Off Delay				10	65			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay				10	65			ns	V_{CC} = 5V, R_L = 400 Ω, C_L = 50pf

ITT1806 DTL QUAD TWO-INPUT AND GATE
ITT1807 FAST DTL QUAD TWO-INPUT GATE

ELECTRICAL CHARACTERISTICS ITT1806-1 (T_A = −55 C to +125 C, V_{CC} = 5.0V +10%)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	+125°C Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.18 mA Inputs at V_{IH} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12 mA V_{CC} = 5.5V, I_{OL} = 15 mA One Inputs at V_{IL} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5			−1.5		−1.4	mA	V_{CC} = 5.5V, V_F = 0.4V
			-1.16		−0.93	−1.16		−1.08	mA	V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD}	V_{CC} Current "Gate Off"					5.15			mA	Inputs Open V_{CC} = 5.0V
Per gate	V_{CC} Current "Gate On"					4.88			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			25		80			ns	V_{CC} = 5.0V, R_L = 3.9K, C_L = 30pf,
t_{pd-}	Turn On Delay			10		65			ns	V_{CC} = 5.0V, R_L = 400Ω, C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT1806-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	0°C Min.	Max.	+25°C Min.	Typ.	+75°C Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	V_{CC} = 5.0V, I_{OH} = −0.12 mA Inputs at V_{IH}
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	V_{CC} = 5.0V, I_{OL} = 12 mA V_{CC} = 5.0V, I_{OL} = 11.4 mA One input at V_{IL}
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4			mA	V_F = 0.45V, V_{CC} = 5.0V
								1.33	mA	V_F = 0.5V, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	V_{CC} = 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 5.0V
I_{PD} Per gate	Power Drain Current					5.75			mA	V_{CC} = 5.0V Inputs Gnd
I_{MAX} Per gate	Max V_{CC} Current					8.5			mA	V_{CC} = 8.0V Inputs Open
t_{pd+}	Turn Off Delay			25		80			ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf
t_{pd-}	Turn On Delay			10		65			ns	V_{CC} = 5V, R_L = 400Ω, C_L = 50pf

Package: Dual In-Line and Flat Pack

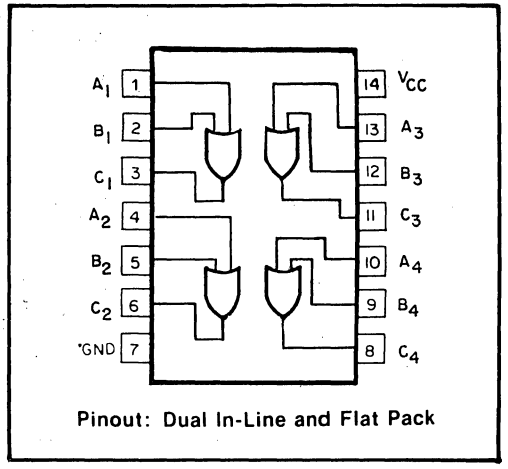
DTL QUAD TWO-INPUT OR GATE

FAST DTL QUAD TWO-INPUT OR GATE

The ITT 1808 and 1809 elements are quad two input positive OR/negative AND gates. In addition to performing the OR function with full fanout available, outputs can be connected together to perform the wire-AND function, thereby reducing system complexity.

The ITT1808 incorporate a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT1809 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.



Pinout: Dual In-Line and Flat Pack

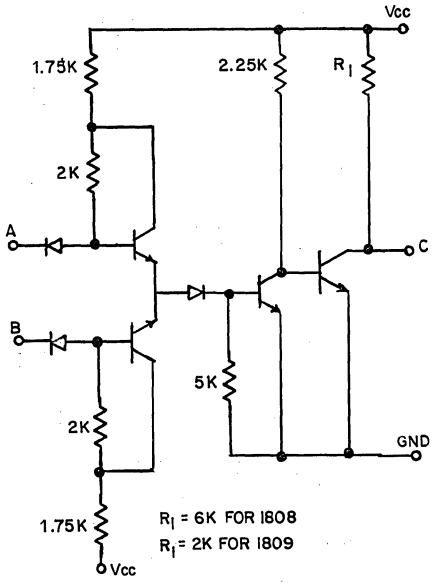
ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature[2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt θ_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC



ITT1808 DTL QUAD TWO-INPUT OR GATE
ITT1809 FAST DTL QUAD TWO-INPUT OR GATE

ELECTRICAL CHARACTERISTICS ITT1808-1 (T_A = −55 C to +125 C, V_{CC} = 5.0V + 10%)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.18 mA One Input at V_{IH} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12 mA V_{CC} = 5.5V, I_{OL} = 15 mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16		−0.93	−1.5 −1.16		−1.4 −1.08	mA mA	V_{CC} = 5.5V, V_F = 0.4V V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD} Per gate	Vcc Current "Gate Off" Vcc Current "Gate On"					7.61 6.25			mA mA	Inputs Open V_{CC} = 5.0V Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay					90 65			ns ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf, V_{CC} = 5V, R_L = 400Ω, C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT1808-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	V_{CC} = 5.0V, I_{OH} = −0.12 mA One Input at V_{IH}
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	V_{CC} = 5.0V, I_{OL} = 12 mA V_{CC} = 5.0V, I_{OL} = 11.4 mA Inputs at V_{IL}
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	V_F = 0.45V, V_{CC} = 5.0V V_F = 0.5V, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	V_{CC} = 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 5.0V
I_{PD} Per gate	Power Drain Current					7.25			mA	V_{CC} = 5.0V Inputs Open
I_{MAX} Per gate	Max V_{CC} Current					14.25			mA	V_{CC} = 8.0V Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay					90 65			ns ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf V_{CC} = 5V, R_L = 400Ω, C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT1809-1 (T_A = −55 C to +125 C, V_{CC} = 5.0V + 10%)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	V_{CC} = 4.5V, I_{OH} = −0.54 mA One Input at V_{IH} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 10.8 mA V_{CC} = 5.5V, I_{OL} = 13.5 mA Inputs at V_{IL} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16		−1.2 −0.93	−1.5 −1.16		−1.4 −1.08	mA mA	V_{CC} = 5.5V, V_F = 0.4V V_{CC} = 4.5V, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	V_{CC} = 5.5V, V_R = 4.0V Ground on other inputs
I_{PD} Per gate	Vcc Current "Gate Off" Vcc Current "Gate On"							7.61 8.38	mA mA	Inputs Open V_{CC} = 5.0V Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay							75 65	ns ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf V_{CC} = 5V, R_L = 400 C_L = 50pf

ELECTRICAL CHARACTERISTICS ITT1809-5 (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	4.3		4.3			4.2		Volts	V_{CC} = 5.0V, I_{OH} = −0.12 mA
V_{OL}	Output Low Voltage		0.5		0.5			0.55	Volts	V_{CC} = 5.0V, I_{OL} = 10.5 mA V_{CC} = 5.0V, I_{OL} = 10.2 mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2		1.1			0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4		1.4			1.33	mA	V_F = 0.45V, V_{CC} = 5.0V V_F = 0.5V, 4.0V on other inputs
I_R	Input Leakage Current		5.0		5.0			10.0	μA	V_{CC} = 5.0V, V_R = 4.0V Gnd On Other Inputs
I_{SC}	Output Short Circuit Current				1.85	3.68			mA	V_{CC} = 5.0V V_{OUT} = Gnd
I_{CEX}	Output Leakage Current				100				μA	V_{CC} = V_{CEX} = 5.0V
I_{PD} Per gate	Power Drain Current				9.38				mA	V_{CC} = 5.0V Inputs Open
I_{MAX} Per gate	Max V_{CC} Current				14.25				mA	V_{CC} = 8.0V Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay				75 65				ns ns	V_{CC} = 5V, R_L = 3.9K, C_L = 30pf V_{CC} = 5V, R_L = 400 Ω, C_L = 50pf

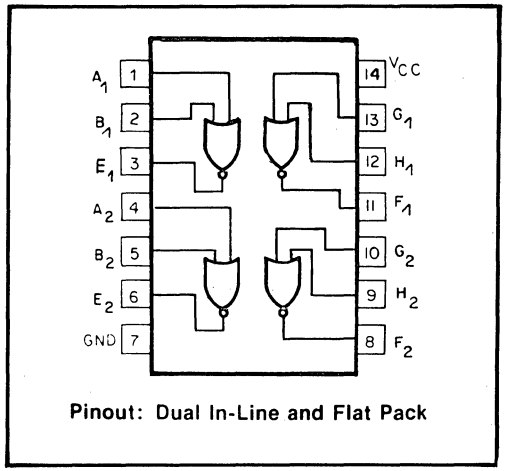
DTL QUAD TWO-INPUT NOR GATE

FAST DTL QUAD TWO-INPUT NOR GATE

The ITT1810 and ITT1811 elements are quad four-input positive NOR gates. In addition to performing the positive NOR and negative NAND logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

The ITT1810 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The ITT1811 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.



Pinout: Dual In-Line and Flat Pack

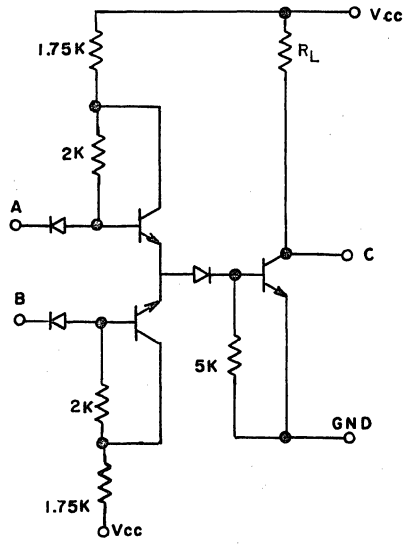
ABSOLUTE MAXIMUM RATINGS [1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8.0 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C
Operating Junction Temperature [2]	+175°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°F

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt O_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt O_{J-C} for TO-5; 180°C/Watt O_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

CIRCUIT SCHEMATIC — EACH GATE



R1 = 6K for 1810
R1 = 2K for 1811

ITT1810 DTL QUAD TWO-INPUT NOR GATE
ITT1811 FAST DTL QUAD TWO-INPUT NOR GATE

ELECTRICAL CHARACTERISTICS ITT1810-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

Symbol	Characteristic	Limits −55°C Min.	Max.	+25°C Min.	Typ.	Max.	+125°C Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.18$ mA Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 12$ mA $V_{CC} = 5.5V$, $I_{OL} = 15$ mA Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5 −1.16		−0.93	−1.5 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs
I_{PD} Per gate	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"					5.0 2.94			mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10		90 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT1810-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristics	0°C Min.	Max.	+25°C Min.	Typ.	Max.	+75°C Min.	Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	2.6		2.6			2.5		Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage		0.45			0.45		0.50	Volts	$V_{CC} = 5.0V$, $I_{OL} = 12$ mA $V_{CC} = 5.0V$, $I_{OL} = 11.4$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		1.4			1.4		1.33	mA mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$, 4.0V On Other Inputs
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current	0.61	1.30	0.61		1.30	0.535	1.25	mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current					100			μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} Per gate	Power Drain Current					5.5			mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} Per gate	Max V_{CC} Current					5.62			mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			25 10		90 30			ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400\,\Omega$, $C_L = 50pf$

ELECTRICAL CHARACTERISTICS ITT1811-1 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)

		LIMITS							
		−55°C	+25°C		+125°C			
Symbol	Characteristic	Min. Max.	Min. Typ.	Max.	Min. Max.	Units	Conditions and Comments	
V_{OH}	Output High Voltage	2.5	2.6 3.5		2.5	Volts	$V_{CC} = 4.5V$, $I_{OH} = -0.54$ mA Inputs at V_{IL} (See Below)	
V_{OL}	Output Low Voltage	0.4	0.27	0 4	0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 10.8$ mA $V_{CC} = 5.5V$, $I_{OL} = 13.5$ mA Inputs at V_{IH} (See Below)	
V_{IH}	Input High Voltage	2.1	1.9		1.7	Volts	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage	1.4		1.1	0.8	Volts	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current	−1.5 −1.16	−1.2 −1.5 −0.93 −1.16		−1.4 −1.08	mA mA	$V_{CC} = 5.5V$, $V_F = 0.4V$ $V_{CC} = 4.5V$, 4.0V on other inputs	
I_R	Input Leakage Current			2.0	5.0	μA	$V_{CC} = 5.5V$, $V_R = 4.0V$ Ground on other inputs	
I_{PD} Per gate	V_{CC} Current "Gate On" V_{CC} Current "Gate Off"			6.9 2.94		mA mA	Inputs Open $V_{CC} = 5.0V$ Inputs Grounded	
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			75 30		ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$	

ELECTRICAL CHARACTERISTICS ITT1811-5 ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$)

		0°C	+25°C		+75°C		
Symbol	Characteristics	Min. Max.	Min. Typ.	Max.	Min. Max.	Units	Conditions & Comments
V_{OH}	Output High Voltage	4.3	4.3		4.2	Volts	$V_{CC} = 5.0V$, $I_{OH} = -0.12$ mA
V_{OL}	Output Low Voltage	0.5		0.5	0.55	Volts	$V_{CC} = 5.0V$, $I_{OL} = 10.5$ mA $V_{CC} = 5.0V$, $I_{OL} = 10.2$ mA
V_{IH}	Input High Voltage	2.0	1.9		1.8	Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage	1.2		1.1	0.95	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current	1.4		1.4	1.33	mA	$V_F = 0.45V$, $V_{CC} = 5.0V$ $V_F = 0.5V$
I_R	Input Leakage Current	5.0		5.0	10.0	μA	$V_{CC} = 5.0V$, $V_R = 4.0V$ Gnd On Other Inputs
I_{SC}	Output Short Circuit Current		1.85 3.68			mA	$V_{CC} = 5.0V$ V_{OUT} = Gnd
I_{CEX}	Output Leakage Current			100		μA	$V_{CC} = V_{CEX} = 5.0V$
I_{PD} Per gate	Power Drain Current			7.65		mA	$V_{CC} = 5.0V$ Inputs Open
I_{MAX} Per gate	Max V_{CC} Current			5.62		mA	$V_{CC} = 8.0V$ Inputs Gnd
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay		10 10	75 30		ns ns	$V_{CC} = 5V$, $R_L = 3.9K$, $C_L = 30pf$ $V_{CC} = 5V$, $R_L = 400$, $C_L = 50pf$

DUAL DTL MASTER-SLAVE J-K FLIP-FLOPS

The ITT9093 and ITT9094 are single chip dual flip-flops with circuitry similar to the ITT945 and ITT948 respectively. They feature internal J-K connections, separate clock pins, and separate SD pins. They are useful in ripple-carry counters and many other J-K flip-flop applications.

The ITT9097 and ITT9099 are single chip dual flip-flops with circuitry similar to the ITT948 and ITT945 respectively. They feature internal J-K connections, a common clock pin, a common CD pin, and separate SD pins. They are useful in shift registers, shift counters, and synchronous counters.

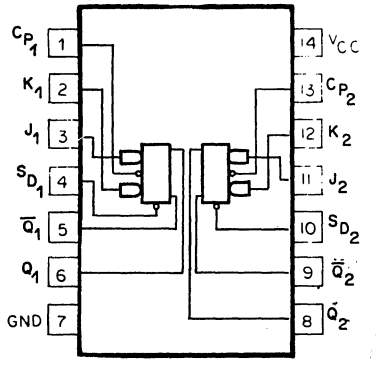
The ITT9093 and ITT9099 are usable with clock frequencies up to 5 MHz and feature a DC level sensitive clock input for stable operation regardless of clock waveshape.

The ITT9094 and ITT9097 are usable with clock frequencies up to 8 MHz.

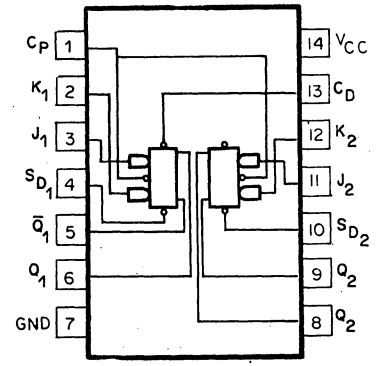
These circuits are fully compatible with the ITT930 series DTL family and the ITT9000 series TTL family.

The ITT9099 series of flip-flops feature J-K feedback connections directly from the output stage of the device. This configuration increases the inherent noise immunity of the circuit, but prevents the circuit from being used in a wired - OR mode. Wired - OR capability is obtained with the ITT9099X series of devices, which are functionally equivalent to the ITT9099 series, but have J-K feedback connections from the buffer stage of the slave flip-flop.

ITT9093/9094
(DUAL ITT945/948 SEPARATE S_D; SEPARATE C_P)



ITT9097/9099
(DUAL ITT948/945 COMMON C_p; COMMON C_D)



Pinout: Dual In-Line and Flat Pack

ABSOLUTE MAXIMUM RATINGS[1]

Characteristics	Units
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−0.5 to +8 Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12 Volts
Output Current, Into Outputs	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Operating Temperature	−55 to +125°C
Storage Temperature	−65 to +125°C
Input Voltage Applied to Input	−1.5 to +5.5 Volts
Lead Temp. (soldering, 60 sec.)	300°C

NOTES:

1. Above which useful life may be impaired.
2. Allow 300°C/Watt O_{J-A} for 1/4" x 1/4" flatpack and dual in-line. Allow 50°C/Watt O_{J-C} for TO-5; 180°C/Watt O_{J-C} for 1/4" x 1/4" flatpack and dual in-line. Heat removal in 1/4" x 1/4" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

NOTES:

1. Positive logic: 0 = L, 1 = H is shown.
2. With synchronous entry, output changes occur as clock level changes from High to Low. For operation in accordance with the table, J and K inputs should normally be changed while the clock is low, and maintained while the clock is high.
3. Asynchronous entry overrides synchronous entry, regardless of clock level. If S_D and C_D are both low, then both go high simultaneously, final condition cannot be predicted. For proper operation, the S_D or C_D terminals must be held in the low state for at least 50 nanoseconds.
4. From circuit symmetry, the S_D and C_D pin designations may be interchanged by interchanging the J and K, and also the Q and Q pin designations. Thus, the 9093-9094 may be used as a dual flip-flop having C_D terminals available, and the 9097-9099 may be used as a dual flip-flop having separate C_D terminals and a common S_D terminal. All rules for ITT945 apply to ITT9093 and 9099. All rules for ITT948 apply to ITT9094 and 9097.
5. Refer to the ITT945/948 for typical operating characteristics.

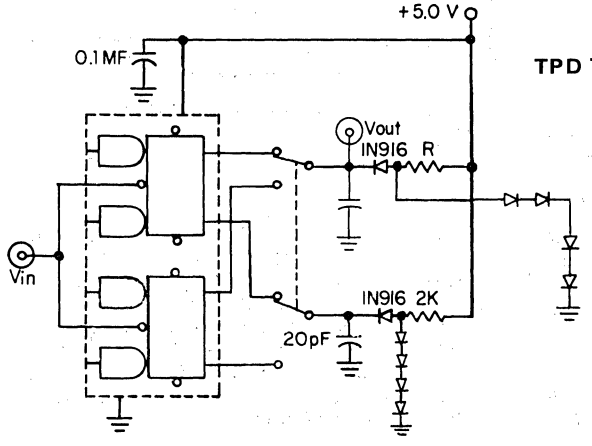
TRUTH TABLES

ASYNCHRONOUS ENTRY

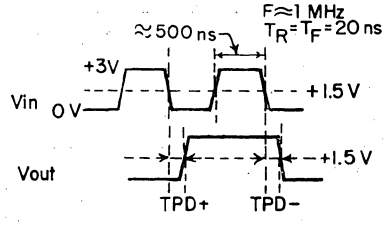
Inputs		Outputs	
S_D	C_D	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No Change	

SYNCHRONOUS ENTRY

Inputs		Output
J	K	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	Qn



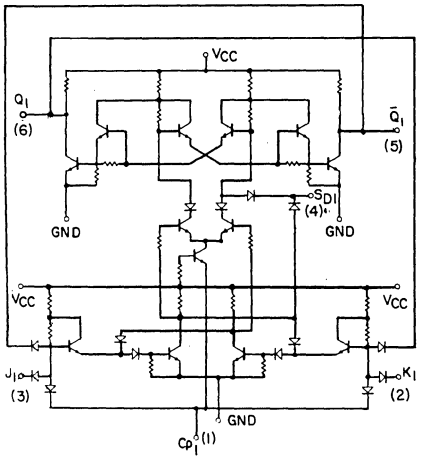
TPD TEST CIRCUIT



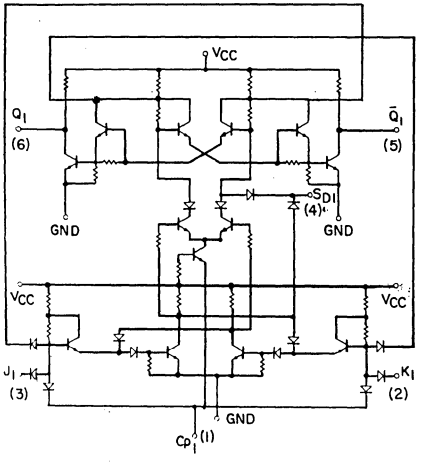
CIRCUIT SCHEMATICS

FOR COMPONENT VALUES, REFER TO ITT945/948

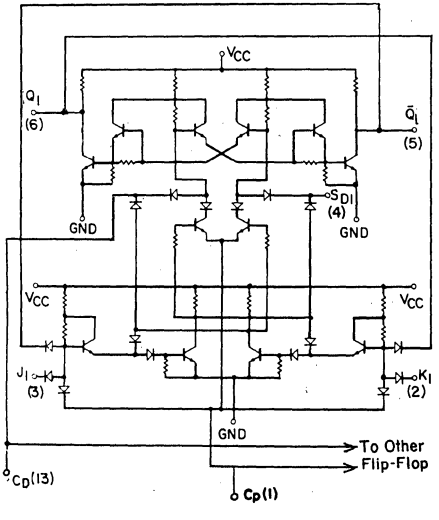
ITT9093/9094 (1/2 OF 9093 SHOWN)



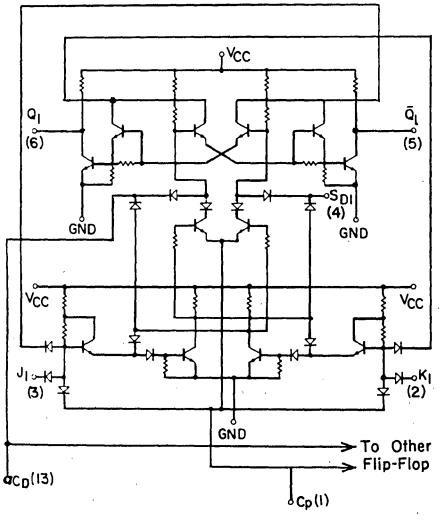
ITT9093X/9094X (1/2 OF 9094X SHOWN)



ITT9097/9099 (1/2 OF 9097 SHOWN)



ITT9097X/9099X (1/2 OF 9099X SHOWN)



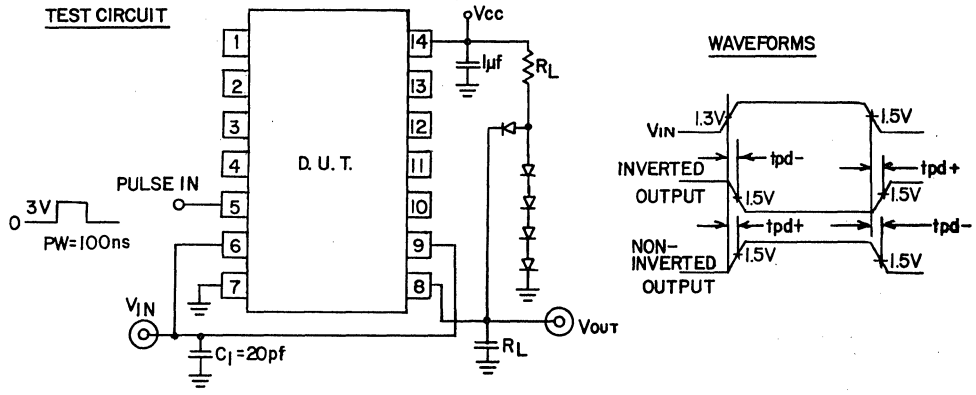
ELECTRICAL CHARACTERISTICS ITT9093-1, 9094-1, 9097-1, 9099-1(T_A = −55°C to +125°C, V_{CC} = 5.0V±10%)

Symbol	Characteristic	Limits −55°C Min.	−55°C Max	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max.	Units	Conditions and Comments
V_{OL}	Output High Voltage									
	9093, 9099	2.5		2.5			2.5		Volts	V_{CC} = 4.5V, I_{OH} = −180 µA
	9094, 9097	2.5		2.5			2.5			V_{CC} = 4.5V, I_{OH} = −540 µA
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12.0 mA
	9093, 9099									V_{CC} = 5.5V, I_{OL} = 15.0 mA
	9094, 9097		0.4			0.4		0.4		V_{CC} = 4.5V, I_{OL} = 13.0 mA
										V_{CC} = 5.5V, I_{OL} = 13.6 mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_R	Input Leakage, All J,K S,C,S_D,C_D, Inputs (except C_D of 9097, 9099)					2.0		5.0	µA	V_{CC} = 5.5V, V_R = 4.0V GND On Other Inputs
	Input Leakage of C_D 9097, 9099					4.0		10		
I_{RCP}	Input Leakage, CP Inputs									
	9093, 9094					10		20		V_{CC} = 4.0V, V_R = 4.0V
	9097, 9099					20		40		
I_F	Input Current, All J,K,S,C Inputs		−.98			−.98	−.92		mA	V_{CC} = 5.5V V_F = 0.4V 4.0V On Other Inputs
	Input Current, S_D or C_D 9093, 9094		−2.2			−2.2		−1.93		
	Input Current, CP Inputs									
	9093		−2.93			−2.93		−2.57		
	9094		−2.35			−2.35		−2.03		
	9097		−4.68			−4.68		−4.04		
	9099		−5.86			−5.86		−5.14		
I_F	Input Current, All J,K,S,C Inputs		−0.76			−0.76		−0.72	mA	V_{CC} = 4.5V
	Input Current, S_D Or C_D Inputs 9093,9094		−1.7			−1.7		−1.5		V_F = 0.4V 4.0V On Other Inputs
	Input Current, CP Inputs									
	9093		−2.26			−2.26		−2.02		
	9094		−1.83			−1.83		−1.59		
	9097		−3.66			−3.66		−3.18		
	9099		−4.52			−4.52		−4.04		
I_{FSI}	Input Current, C_D, S_D Inputs			−2.93			−2.93	−2.57	mA	V_{CC} = 5.5V, V_F = 0.4V
	9097, 9099		−2.26			−2.26		−2.20		V_{CC} = 4.5V 4.0V On Other Inputs
I_{PD}	V_{CC} Current								mA	V_{CC} = 5.0V, All Inputs Open Momentary Ground On S_D
	9093				16.6	28.0				
	9094				19.8	32.4				
	9097				19.8	32.4				
	9099				16.6	28.0				
t_{pd+}	Turn Off Delay - Clock									
	9094, 9097			35		65			ns	V_{CC} = 5.0V
	9093, 9099			35		75				R_L = 2K, C_L = 30pf
t_{pd-}	Turn On Delay									
	9093, 9094,			30		75			ns	R_L = 330 , C_L = 50pf
	9097, 9099			30		75				

ELECTRICAL CHARACTERISTICS ITT9093-5, 9094-5, 9097-5, 9099-5 (T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%)

		Limits							
		0°C		+25°C			+75°C		
Symbol	Characteristic	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Units	Conditions and Comments
V_{OH}	Output High Voltage									
	9093, 9099	2.6		2.6			3.1		Volts	V_{CC} = 5.0V
	9094, 9097	4.3		4.3			4.3			I_{OH} = −110 µA
V_{OL}	Output Low Voltage									V_{CC} = 5.0V
	9093, 9099		0.45			0.45		0.45	Volts	I_{OL} = 15.8 mA
	9099, 9097		0.45			0.45		0.45		I_{OL} = 15.1 mA
										I_{OL} = 14.4 mA
										I_{OL} = 13.7 mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_R	Input Leakage, All J-K S, C, S_D, Inputs (except C_D of 9097, 9099)		5.0			5.0		10.0	µA	V_{CC} = 5.0V, V_R = 4.0V
	Input Leakage Of C_D 9097, 9099		10.0			10.0		20.0		
I_{RCP}	Input Leakage, CP									
	Inputs 9093, 9094		20.0			20.0		30.0	µA	V_{CC} = 4.0V, V_R = 4.0V
	9097, 9099		40.0			40.0		60.0		GND On Other Inputs
I_F	Input Current, All J,K,S,C Inputs		0.95			0.95		0.90	mA	V_{CC} = 5.0V, V_F = 0.45V 4.0V On Other Inputs
	Input Current, S_D Or C_D (9093, 9094)		2.10			2.10		2.00		
I_{FCP}	Input Current, CP Inputs									
	9093		2.80			2.80		2.66	mA	V_{CC} = 5.0V, V_F = 0.45V
	9094		2.24			2.24		2.13		4.0V On Other Inputs
	9097		4.48			4.48		4.26		
	9099		5.60			5.60		5.32		
I_{FSI}	Input Current									
	9097, 9099 Inputs C_D		5.60			5.60		5.32	mA	V_{CC} = 5.0V, V_F = 0.45V
	9097, 9099 Inputs S_D		2.80			2.80		2.66		4.0V On Other Inputs
I_{SC}	Output Short Circuit Current									
	9093, 9099	0.59	1.41	0.59		1.41	0.59	1.41	mA	V_{CC} = 5.0V, V_{OUT} = GND
	9094, 9097	1.77	4.2							−1.0V On Opposite J Or K
I_{cex}	Output Leakage					105			A	V_{CC} = V_{cex} = 5.0V
I_{PD}	V_{CC} Current									
	9093, 9099					30			mA	V_{CC} = 5.0V, Inputs Open
	9094, 9097					35				Clock Pulse On S_D
I_{MAX}	Maximum V_{CC} Current									V_{CC} = 8.0 . All Inputs GND
	9093					42			mA	
	9094					48				
	9097					35				
	9099					38				
t_{pd+}	Turn Off Delay									
	9094, 9097			35		65			ns	V_{CC} = 5.0V
	9093, 9099			35		75				R_L = 2.0K, C_L = 30pf
t_{pd-}	Turn On Delay									
	9093, 9094			30		75				R_L = 330 C_L = 50pf
	9097, 9099			30		75				

DTL TEST CIRCUIT



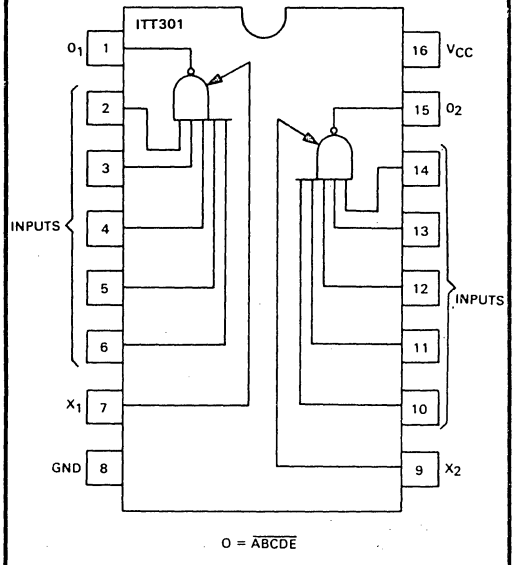
NOTES:

a) All Diodes 1N914 or equivalent
b) C_1 and C_I include Probe and Jig Capacitances
c) 1N914 Diodes are added to Pins 5 and 9 when testing
d) 6Ku Pull-up resistors are added to Pins 6 and 8 when testing ITT938
e) Pins 4 and 10 are open or grounded as required by device logic

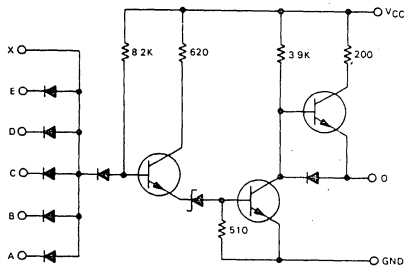
DUAL EXPANDABLE FIVE-INPUT NAND BUFFER

The ITT301 is an active pull-up element featuring high current capability in both the high and low state. It is an excellent choice for driving long transmission lines, as a system clock driver, or for driving any load with high capacitance.

Pin Configuration



SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	—65°C to +150°C
Operating Temperature Range	
301 H-1, 301-1	—55°C to +125°C
301 H-5	—30°C to +75°C
301-5	—30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
301 -1, 301 -5	—0.5V to 16.5V
301 H-1, 301 H-5	—0.5V to 18V
Input Voltage-Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at: +125°	500mw
at +85°	900mw

ITT301, ITT301H
DUAL EXPANDABLE FIVE-INPUT NAND BUFFER

ELECTRICAL CHARACTERISTICS ITT301-1, ITT301-5 over recommended operating free air temperature range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =300ua
V_{OL}	Output Low Voltage		 1.5 1.8	 V V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=42mA I_{OL}=63mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		48	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	15.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V
tpd+	Propagation Delay, Positive Going Output		400	NS	C_L=300pf, R_L=330Ω
tpd−	Propagation Delay, Negative Going Output		240	NS	C_L=300pf, R_L=330Ω

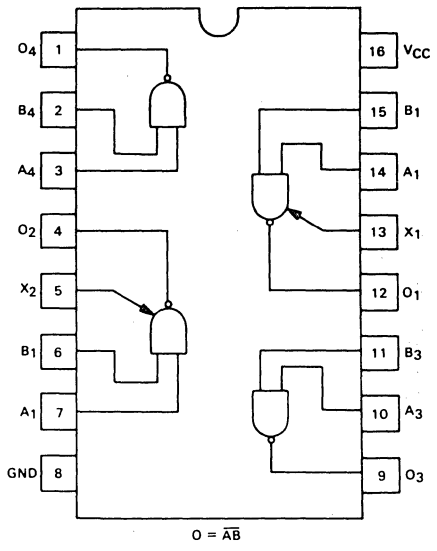
ELECTRICAL CHARACTERISTICS ITT301H-1, ITT301H-5 over recommended operating free air temperature range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−250ua
V_{OL}	Output Low Voltage		 1.8 2.0	 V V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=52mA I_{OL}=65
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current 301H-5		68	mA	V_{cc}=16.0V
	301H-1		40	mA	
I_{OH}	Output Source Current	15.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V
tpd+	Propagation Delay, Positive Going Output		400	NS	C_L=300pf, R_L=330Ω
tpd−	Propagation Delay, Negative Going Output		240	NS	C_L=300pf, R_L=330Ω

QUAD 2-INPUT (2 EXPANDABLE) NAND BUFFER

The ITT302 open collector quad buffer finds application as a lamp or relay driver in addition to its use as a high-sink-current logic element. the open collector allows easy interfacing with other logic systems and can be wired-OR for increased design flexibility.

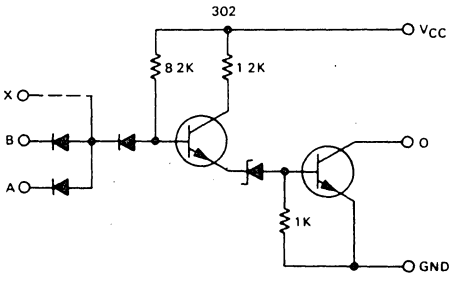
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
302H-1, 302-1	−55°C to +125°C
302H-5	−30°C to +75°C
302-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
302-1, 302-5	−0.5 to 16.5V
302H-1, 302H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5 to 16.5V
Sink Current, Continuous Buffers	80mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ELECTRICAL CHARACTERISTICS ITT302-1, 302-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage				V_{cc}=11.0V, V_{IH}=6.5V
			1.5	V	I_{OL}=62mA
			0.4	V	I_{OL}=16mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		40	mA	V_{cc}=13.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=13.0V, V_{IL}=5.0V V_{CEX}=13.0V
LV_{CE}	Collector Latching Voltage	13.0		V	V_{CC}=13.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

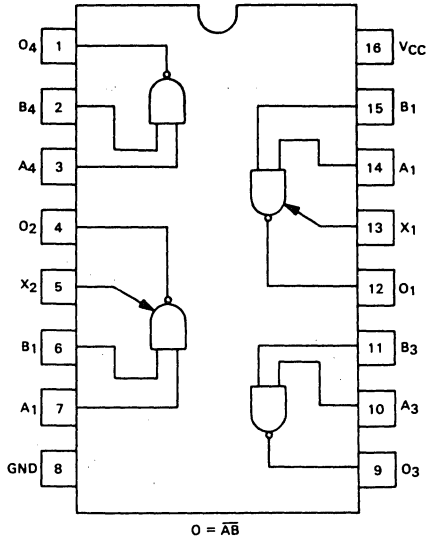
ELECTRICAL CHARACTERISTICS ITT302H-1, 302H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage				V_{cc}=14.0V, V_{IH}=6.5V
			1.8	V	I_{OL}=64mA
			0.4	V	I_{OL}=16mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current 302H-1		40	mA	V_{cc}=16.0V
	302H-5		60	mA	
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=16.0V, V_{IL}=5.0V V_{CEX}=16.0V
LV_{CE}	Collector Latching Voltage	16.5		V	V_{CC}=16.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

QUAD 2-INPUT NAND BUFFERS (2 EXPANDABLE)

The ITT303 is a high sink current buffer with passive pull-up resistors on the chip. It is useful in the collector-OR configuration, as a system buffer, or as a lamp driver. For use as a high-fan out gate, a supplemental external pull-up resistor should be used.

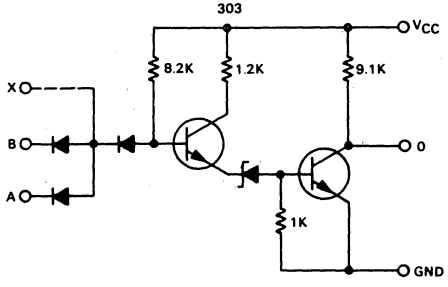
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
303H-1, 303-1	−55°C to +125°C
303H-5	−30°C to +75°C
303-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
303-1, 303-5	−0.5V to 16.5V
303H-1, 303H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ITT303, ITT303H
QUAD 2-INPUT (2 EXPANDABLE) NAND BUFFERS

ELECTRICAL CHARACTERISTICS 303-1, 303-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{1L}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{1H}=6.5V I_{OL}=60.5mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		49	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

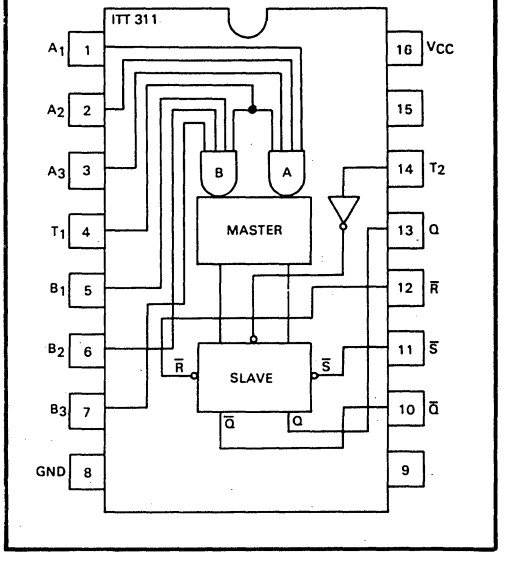
ELECTRICAL CHARACTERISTICS 303H-1, 303H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage		13.0	V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{1H}=6.5V I_{OL}=60mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V. V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current 303H-1 303H-5		40 70	mA mA	V_{cc}=16.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

MASTER SLAVE FLIP-FLOP

The ITT311 is a universal HiNiL flip-flop. It has separate clocks which allow two-phase (dual inhibit) operation, direct set and reset inputs, six data inputs, and is level sensitive. It can be operated as a J-K flip-flop by external wiring and features active outputs.

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

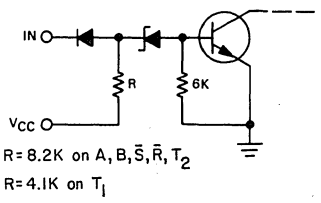
Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
311H-1, 311-1	−55°C to +125°C
311H-5	30°C to +75°C
311-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
311-1, 311-5	−0.5V to 16.5V
311H-1, 311H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

J-K Operation ***R Operation**

A	B	Q [1]	A	B	Q [1]
L	L	Q	L	L	Q
L	H	L	L	H	L
H	L	H	H	L	H
H	H	Q	H	H	X

*Undetermined

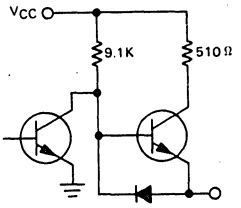
Schematic Typical Input



R=8.2K on A, B, $\bar{S}$, $\bar{R}$, T_2

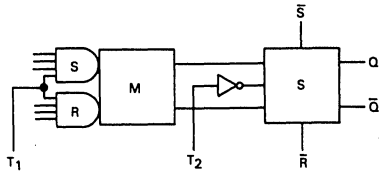
R=4.1K on T_1

Typical Output

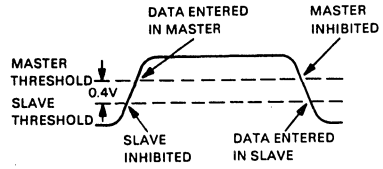


ITT311, ITT311H
MASTER SLAVE FLIP-FLOP

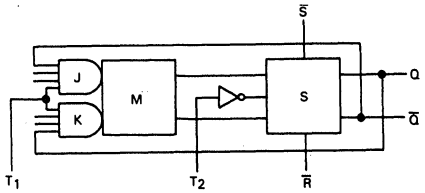
Circuit Diagram
Set-Reset Mode



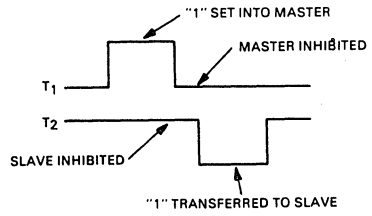
Single-Phase Timing



J-K Mode



Two-Phase Timing



ELECTRICAL CHARACTERISTICS 311-1, 311-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	A, B, T Inputs
			7.0	V	S, R Inputs
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=12.6mA
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			10	ua	A, B, R, S, T_2 Inputs
			20	ua	T_1 Input
I_{IL}	Input Low Level Current				V_{cc}=13.0V, V_F=1.5V
			−2.1	mA	A, B, R, S, T_2 Inputs
			−4.2	mA	T_1 Input
I_{CC}	Power Supply Current		18	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			820	NS	T− Q+
			400	NS	R− Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			610	NS	T− Q−
			250	NS	R− Q−

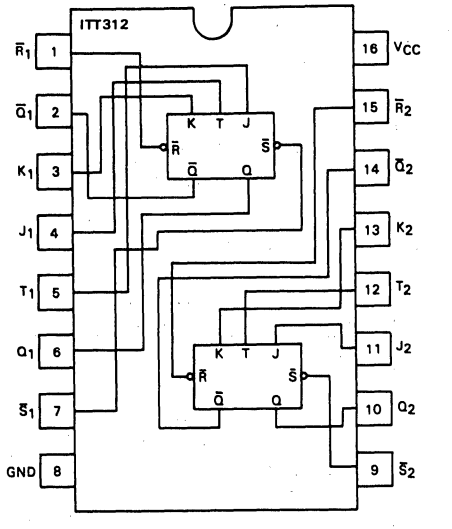
ELECTRICAL CHARACTERISTICS 311H-1, 311H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5 7.0	V V	A, B, T Inputs S, R, Inputs
V_{IL}	Input Low Threshold Voltage	5.0 4.8		V V	A, B, R, S, T_2 Inputs T_1 Inputs
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=15.6mA
I_{IH}	Input High Level Current		 10 20	 ua ua	V_{cc}=16.0V, V_R=16.0V A, B, R, S, T_2 Inputs T_1 Input
I_{IL}	Input Low Level Current		 −2.6 −5.2	 mA mA	V_{cc}=16.0V, V_F=1.8V A, B, S, R, T_2 Inputs T_1 Input
I_{CC}	Power Supply Current		25	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output		 820 400	 NS NS	C_L=50pf, R_L=2kΩ T− Q+ R− Q+
tpd−	Propagation Delay, Negative Going Output		 610 250	 NS NS	C_L=50pf, R_L=2kΩ T− Q− R− Q−

DUAL J-K FLIP-FLOP

Two completely separated J-K flip-flops are incorporated on one 312 chip. Each flip-flop has its own separate clock, set, and reset inputs. The device clock is negative edge sensitive, requiring a clock fall time of 3 volts per microsecond or faster. Active-high outputs are provided.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
321H-1, 321-1	−55°C to +125°C
H-5	−30° to +75°C
-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed <0.1 Second	18V
Input Voltage (exclusive of expanders)	
321-1, 321-5	−0.5V to 16.5V
321H-1, 321-H5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Truth Table

S-R Mode			J-K Mode		
S	R	Q	J	K	Q^1
H	H	X	L	L	Q
H	L	L	L	H	L
L	H	H	H	L	H
L	L	H	H	H	Q

X=Indeterminate state

ELECTRICAL CHARACTERISTICS 312-1, 312-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5 mA

ITT312, ITT312H
DUAL J-K FLIP-FLOP

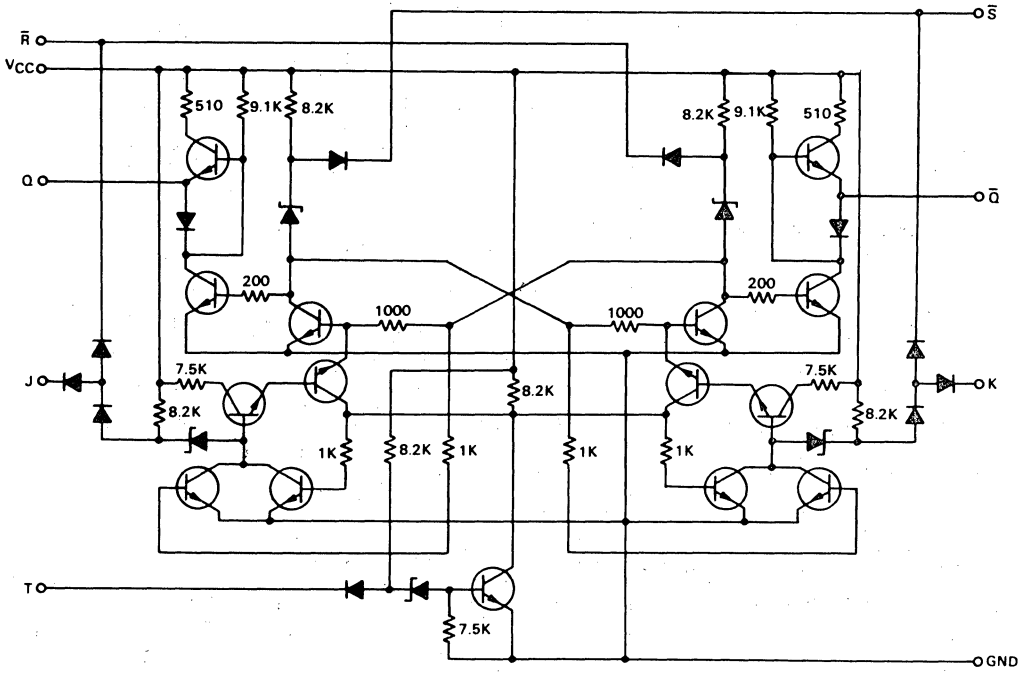
ELECTRICAL CHARACTERISTICS 312-1, 312-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			10	ua	J, K, T Inputs
			20	ua	S, R Inputs
I_{IL}	Input Low Level Current				V_{cc}=13.0V, V_F=1.5V
			−2.1	mA	J, K, T Inputs
			−4.2	mA	S, R Inputs
I_{CC}	Power Supply Current		30	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V
					V_{OH}=7.0V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			300	NS	T− Q+
			600	NS	R− Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			230	NS	T− Q−
			320	NS	R− Q−

ELECTRICAL CHARACTERISTICS 312H-1, 312H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{iL}=5.0V
					I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{iH}=6.5V
					I_{OL}=13.0mA
I_{IH}	Input High Level Current				V_{cc}=16.0V, V_R=16.0V
			10	ua	J, K, T Inputs
			20	ua	S, R Inputs
I_{IL}	Input Low Level Current				V_{cc}=16.0V, V_F=1.8V
			−2.6	mA	J, K, T Inputs
			−5.2	mA	S, R Inputs
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V
					V_{OH}=9.5V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			300	NS	T− Q+
			600	NS	R− Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			230	NS	T− Q−
			320	NS	R− Q−

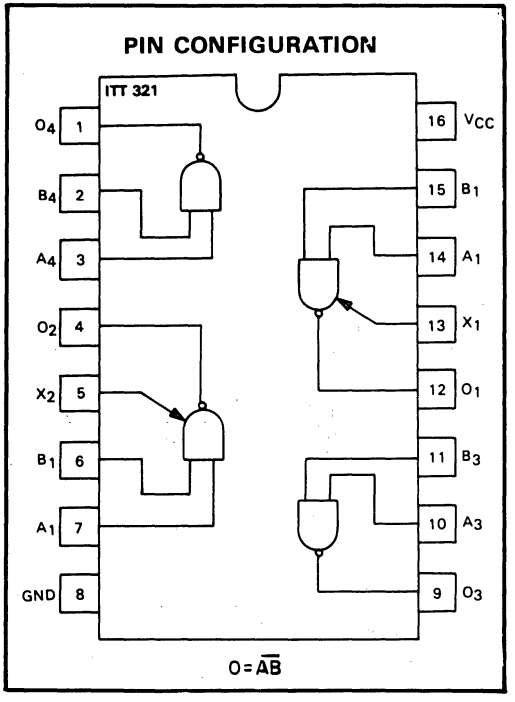
SCHEMATIC (EACH FLIP-FLOP)



ITT SEMICONDUCTORS

QUAD 2-INPUT (2 EXPANDABLE) NAND GATE

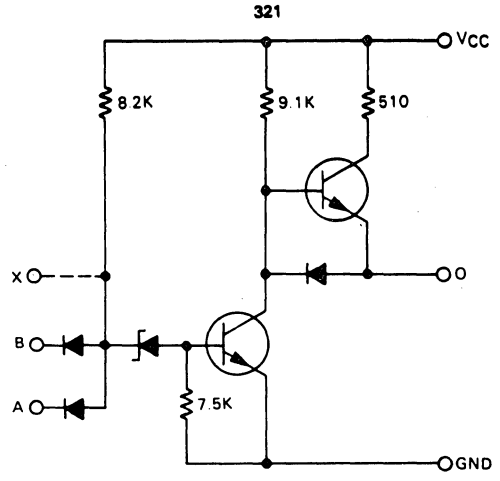
The ITT321 contains four two input active pull-up nand gates. Two of these gates are expandable by addition of discrete diodes or a 331 expander.



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
321H-1, 321-1	−55°C to +125°C
H-5	−30° to +75°C
-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed <0.1 Second	18V
Input Voltage (exclusive of expanders)	
321-1, 321-5	−0.5V to 16.5V
321H-1, 321-H5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ITT321, ITT321H
QUAD 2-INPUT (2 EXPANDABLE) NAND GATE

ELECTRICAL CHARACTERISTICS 321-1, 321-5 Over Recommended Operating Free Air Temperature Range

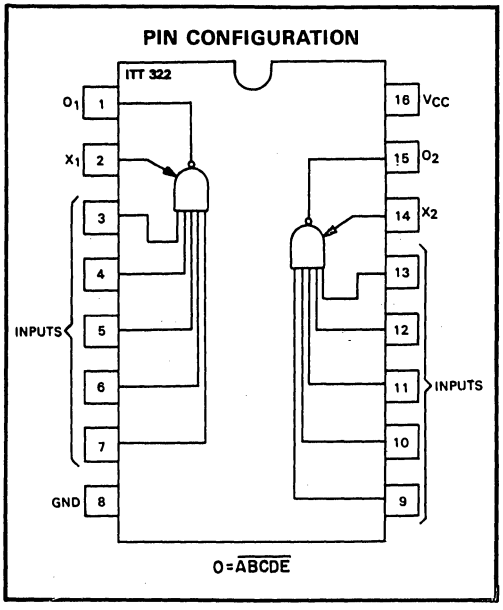
Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5 mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		15.0	mA	V_{cc}=13.0V Inputs Open
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

ELECTRICAL CHARACTERISTICS 321H-1, 321H-5 OVer Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IH}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		20.0	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

DUAL 5-INPUT EXPANDABLE NAND GATE

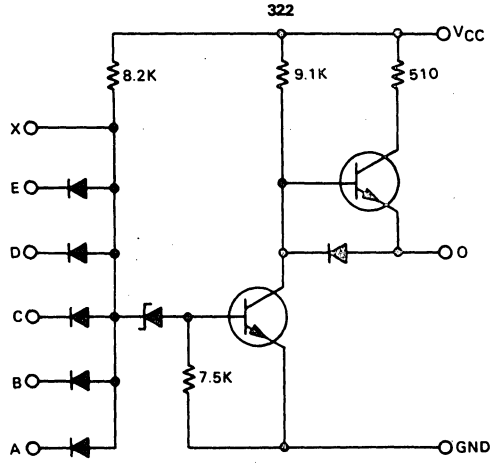
The ITT322 contains two 5-input active pull-up Nand Gates. Both gates are expandable by addition of discrete diodes or a 331 expander.



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
322H-2, 322-1	−55°C to +125°C
322H-5	−30° to +75°C
322-5	−30° to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed <0.1 Second	18V
Input Voltage (exclusive of expanders)	
322-1, 322-5	—0.5V to 16.5V
322H-1, 322H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ITT322, ITT322H
DUAL 5-INPUT EXPANDABLE NAND GATE

ELECTRICAL CHARACTERISTICS 322-1, 322-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5 mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		8.0	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

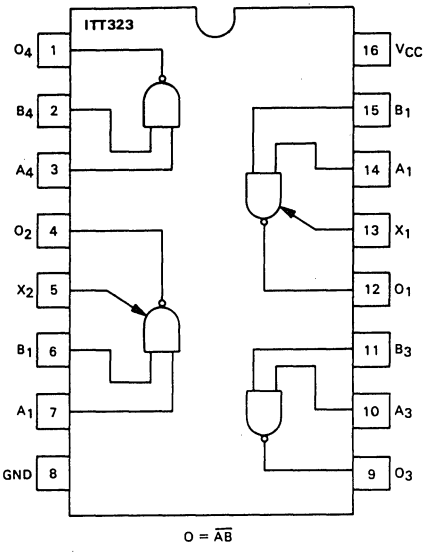
ELECTRICAL CHARACTERISTICS 322H-1, 322H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		11.0	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

QUAD 2-INPUT (2 EXPANDABLE) NAND GATE

The ITT323 is a highly versatile expandable Quad-2 input nand gate. Its open-collector outputs find application in interface and wire-OR applications.

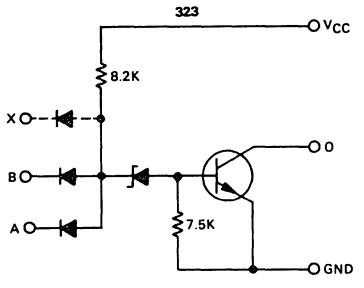
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
323H-1, 323-1	−55°C to +125°C
323H-5	−30°C to +75°C
323-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
323-1, 323-5	−0.5V to 16.5V
323H-1, 323H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5 to 16.5V
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

SCHEMATIC



ELECTRICAL CHARACTERISTICS 323-1, 323-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage		 1.5 0.4	 V V	V_{cc}=13.0V, V_{IH}=6.5V I_{OL}=10.5 mA I_{OL}=6.4mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		5.5	mA	V_{cc}=13.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=13.0V, V_{IL}=5.0V V_{CEX}=13.0V
LV_{CE}	Collector Latching Voltage	13.0		V	V_{CC}=13.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

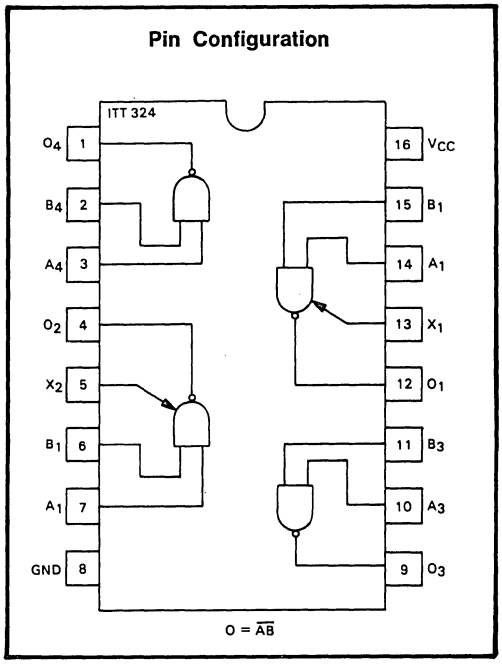
ELECTRICAL CHARACTERISTICS 323H-1, 323H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		8.0	mA	V_{cc}=16.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=16.0V, V_{IL}=5.0V V_{CEX}=16.0V
LV_{CE}	Collector Latching Voltage	16.5		V	V_{CC}=16.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

QUAD 2-INPUT (2 EXPANDABLE) NAND GATE

The ITT324 expandable Quad two input nand gate is a basic building block featuring collector OR-able passive pull-up outputs. Nominal fanout is five, but fanout can be increased to seven by addition of an external 10KΩ pull-up resistor.

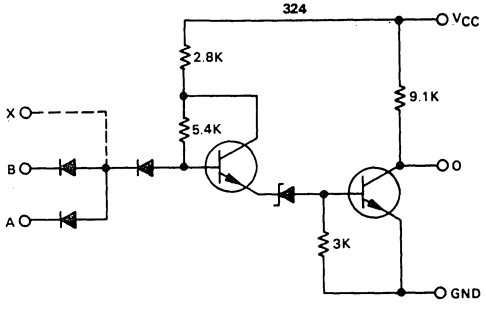
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
324H-1, 324-1	−55°C to +125°C
324H-5	−30°C to +75°C
324-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
324-1, 324-5	−0.5V to 16.5V
324H-1, 324H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ITT324, ITT324H
QUAD 2-INPUT (2 EXPANDABLE) NAND GATE

ELECTRICAL CHARACTERISTICS 324H-1, 324H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

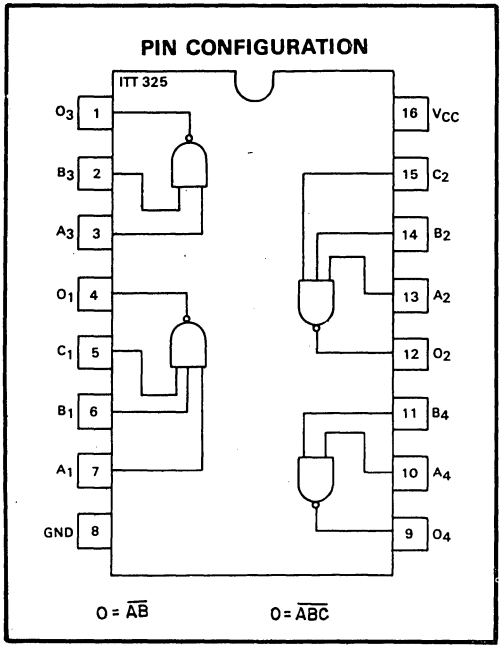
ELECTRICAL CHARACTERISTICS 324-1, 324-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=16.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		28	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

DUAL 2, DUAL 3-INPUT NAND GATE

The ITT325 Dual Two, Dual three input gate is a basic building block for HiNiL systems. It has active pull-up outputs for maximum noise immunity and drive capability.

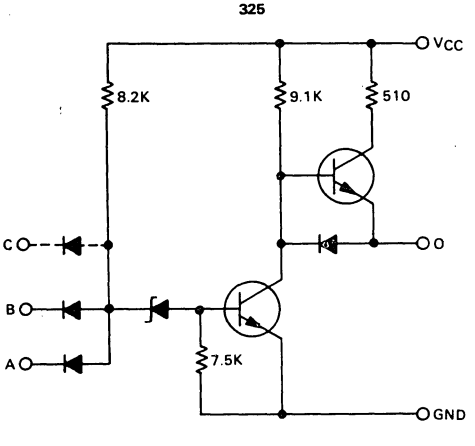
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
325H-1, 325-1	−55° to +125°C
325H-5	−30°C to +75°C
325-5	−30°C to 85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
325-1, 325-5	−0.5V to 16.5V
325H-1, 325H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

SCHEMATIC (EACH GATE)



ITT325, ITT325H
DUAL 2, DUAL 3-INPUT NAND GATE

ELECTRICAL CHARACTERISTICS 325-1, 325-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=14.0V, V_{IH}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5 mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		15.0	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

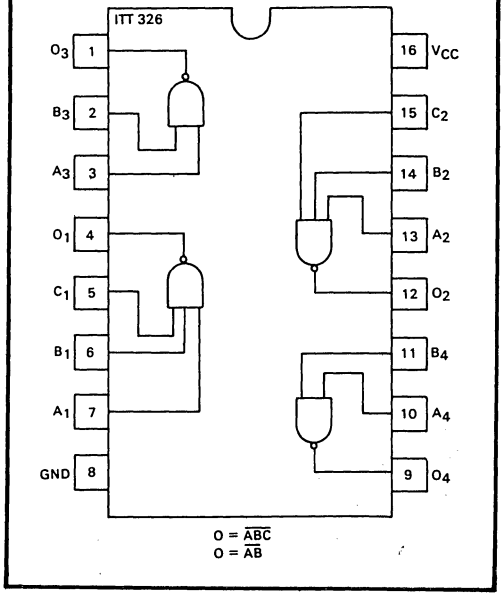
ELECTRICAL CHARACTERISTICS 325H-1, 325H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		20.0	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

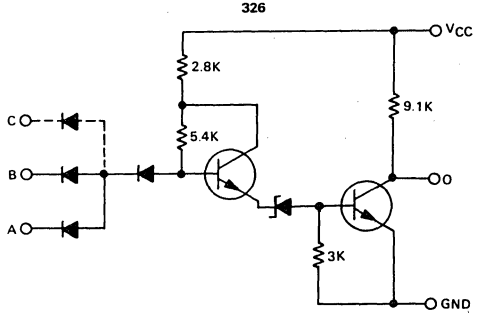
DUAL 2, DUAL 3-INPUT NAND GATE

The ITT326 provides two two-input gates and two three-input gates in a single package. It has passive pull-ups to enable its use in the wired OR configuration.

Pin Configuration



Schematic (Each Gate)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
326H-1, 326-1	−55°C to +125°C
326H-5	−30°C to +75°C
326-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
326-1, 326-5	−0.5V to 16.5V
326H-1, 326H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

ITT326, ITT326H
DUAL 2, DUAL 3-INPUT NAND GATE

ELECTRICAL CHARACTERISTICS 326-1, 326-5 Over Recommended Operating Free Air Temperature Range

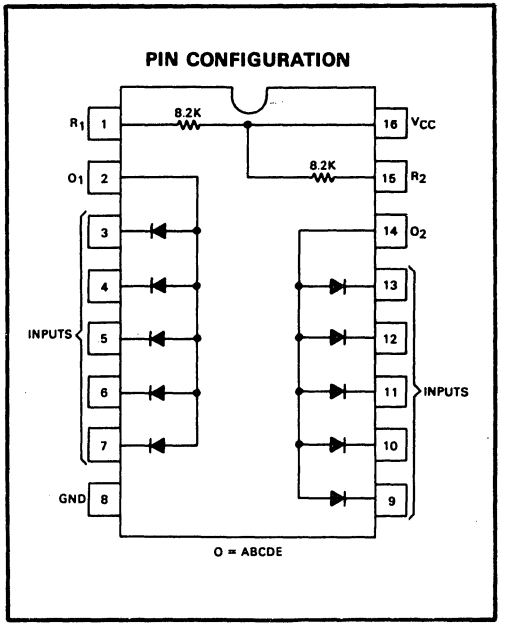
Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=16.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		28	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

ELECTRICAL CHARACTERISTICS 326H-1, 326H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} = −50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

DUAL 5-INPUT EXPANDER

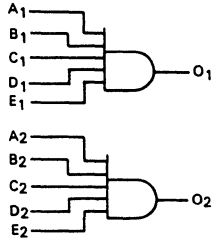
The ITT331 consists of two arrays of H_INiL input diodes which are used on the expander inputs of H_INIL devices. Two 8.2K nominal resistors are also available on the chip, allowing the 331 to be used as a second level dual 5-input AND gate.



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
331H-1, 331-1	−55°C to +125°C
331H-5	−30°C to +75°C
331-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage	
331-1, 331-5	−0.5V to 16.5V
331H-1, 331H-5	−0.5V to 18V
Voltage applied to output	−0.5V to V_{IN}
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS 331-1, 331-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{CC}	Power Supply Current		4.2	mA	V_{cc}=13.0V

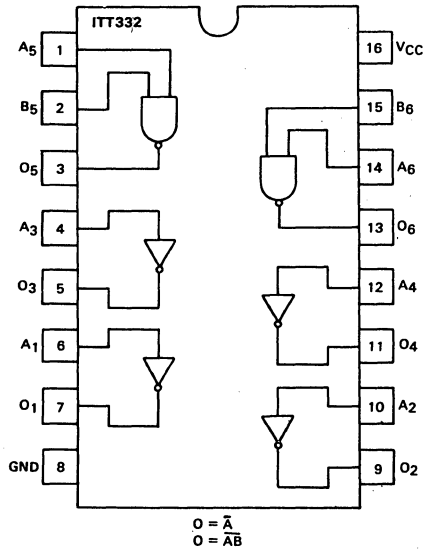
ELECTRICAL CHARACTERISTICS 331H-1, 331H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{CC}	Power Supply Current		5.2	mA	V_{cc}=16.0V

QUAD INVERTER, DUAL 2-INPUT NAND GATE

The ITT332 contains four inverters and two two-input nand gates. Its open collector configuration with a 20 or 24-volt rating makes it very useful as an interface element.

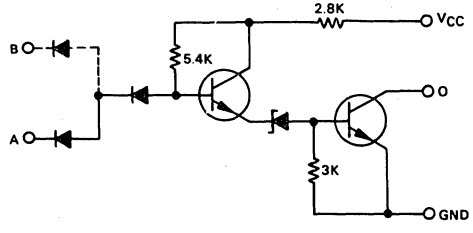
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
332H-1, 332-1	−55°C to +125°C
332H-5	−30°C to +75°C
332-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
Voltage applied to output	−0.5V to 25V
332-1, 332-5	−0.5V to 16.5V
332H-1, 332H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ITT332, ITT332H
QUAD INVERTER, DUAL 2-INPUT NAND GATE

ELECTRICAL CHARACTERISTICS 332-1, 332-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=16.8mA
			0.4	V	I_{OL}=6.4mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		28	mA	V_{cc}=13.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=13.0V, V_{IL}=5.0V V_{CEX}=13.0V
LV_{CE}	Collector Latching Voltage	20.0		V	V_{CC}=13.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

ELECTRICAL CHARACTERISTICS 332H-1, 332H-5 Over Recommended Operating Free Air Temperature Range

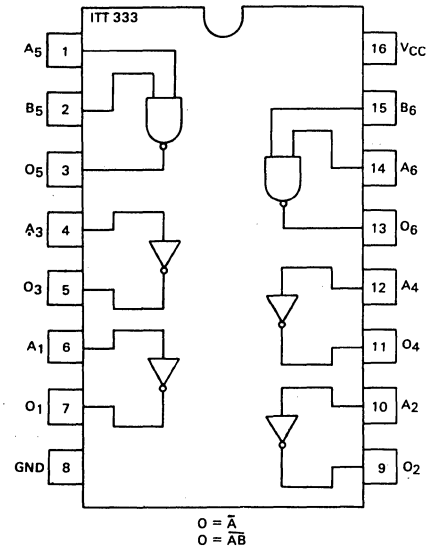
Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
			0.4	V	I_{OL}=6.4mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		42	mA	V_{cc}=16.0V 332-1, 332H-5
			40	mA	332H-1
I_{CEX}	Output Leakage Current		25	ua	V_{CC}=16.0V, V_{IL}=5.0V V_{CEX}=16.0V
LV_{CE}	Collector Latching Voltage	24.0		V	V_{CC}=16.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

ITT SEMICONDUCTORS

QUAD INVERTER, DUAL 2-INPUT NAND GATE

The ITT333 is another basic system building block. It is a passive pull-up device containing four inverters and two two-input nand gates.

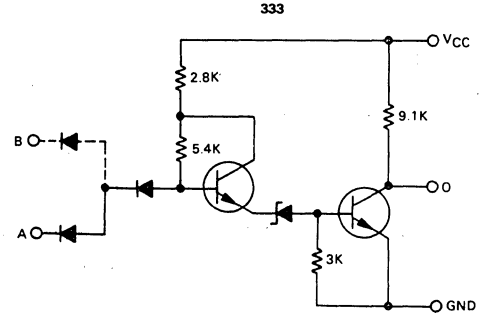
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
333H-1, 333-1	−55°C to +125°C
333H-5	−30°C to +75°C
333-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
333-1, 333-5	−0.5V to 16.5V
333H-1, 333H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic (Each Gate)



ELECTRICAL CHARACTERISTICS 333H-1, 333H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V 333H-1
			60	mA	333H-5
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

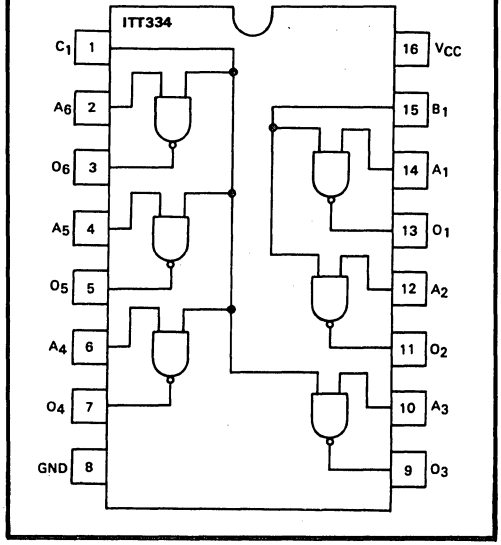
ELECTRICAL CHARACTERISTICS 333-1, 333-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=16.8mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		42	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

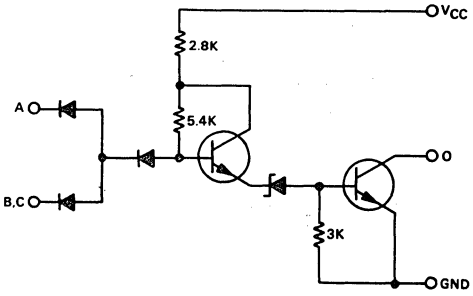
STROBED HEX INVERTER

The ITT334 is a hex inverter with inputs which allow disabling of two, four, or six gates with a single strobe input signal. This configuration is useful in data transfer applications. The 334 has open collector outputs.

Pin Configuration



Schematic



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
334H-1, 334-1	−55°C to +125°C
334H-5	−30° to +75°C
334-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
334-1, 334-5	−0.5 to 16.5V
334H-1, 334H-5	0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to 25.0V
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

ITT334, ITT334H
STROBED HEX INVERTER

ELECTRICAL CHARACTERISTICS 334-1, 334-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage				V_{cc}=11.0V, V_{IH}=6.5V
			1.5	V	I_{OL}=16.8mA
			0.4	V	I_{OL}=6.4mA
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			10	ua	A Inputs
			20	ua	B Input
			40	ua	C Input
I_{IL}	Input Low Level Current				V_{cc}=13.0V, V_F=1.5V
			−2.1	mA	A Inputs
			−4.2	mA	B Input
			−8.4	mA	C Input
I_{CC}	Power Supply Current		28	mA	V_{cc}=13.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=13.0V, V_{IL}=5.0V V_{CEX}=13.0V
LV_{CE}	Collector Latching Voltage	20.0		V	V_{CC}=13.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

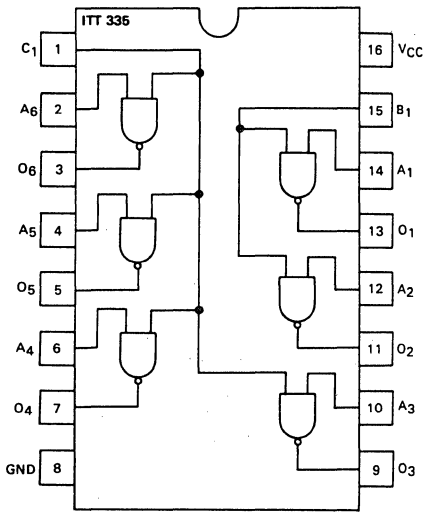
ELECTRICAL CHARACTERISTICS 334H-1, 334H-5 Over Recommended Operating Free Air Temp. Range

V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
			0.4	V	I_{OL}=6.4mA
I_{IH}	Input High Level Current				V_{cc}=16.0V, V_R=16.0V
			10	ua	A Inputs
			20	ua	B Input
			40	ua	C Input
I_{IL}	Input Low Level Current				V_{cc}=16.0V, V_F=1.8V
			−2.6	mA	A Inputs
			−5.2	mA	B Input
			−10.4	mA	C Input
I_{CC}	Power Supply Current 334H-1		40	mA	V_{cc}=16.0V
	334H-5		42	mA	
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=16.0V, V_{IL}=5.0V V_{CEX}=16.0V
LV_{CE}	Collector Latching Voltage	24.0		V	V_{CC}=16.0V, V_{IL}=5.0V I_{CE}=4.0mA
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

STROBED HEX INVERTER

The ITT335 has the same strobe configuration as the ITT334. The ITT335, however, has pullup resistors on the chip.

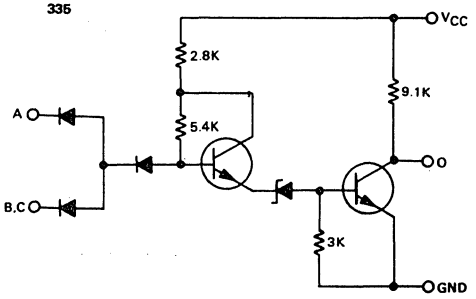
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
335H-1, 335-1	−55°C to +125°C
335H-5	−30°C to +75°C
335-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
335-1, 335-5	−0.5V to 16.5V
335H-1, 335H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

SCHEMATIC



ELECTRICAL CHARACTERISTICS 335-1, 335-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua

ITT335, ITT335H
STROBED HEX INVERTER

ELECTRICAL CHARACTERISTICS 335-1, 335-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=16.8mA
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			10	ua	A Inputs
			20	ua	B Input
			40	ua	C Input
I_{IL}	Input Low Level Current				V_{cc}=13.0V, V_F=1.5V
			−2.1	mA	A Inputs
			−4.2	mA	B Input
			—8.4	mA	C Input
I_{CC}	Power Supply Current		42	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

ELECTRICAL CHARACTERISTICS 335H-1, 335H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−50ua
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=20.8mA
I_{IH}	Input High Level Current				V_{cc}=16.0V, V_R=16.0V
			10	ua	A Inputs
			20	ua	B Input
			40	ua	C Input
I_{IL}	Input Low Level Current				V_{cc}=16.0V, V_F=1.8V
			−2.6	mA	A Inputs
			−5.2	mA	B Input
			—10.4	mA	C Input
I_{CC}	Power Supply Current				V_{cc}=16.0V
	335H-1		40	mA	
	335H-5		60	mA	
tpd+	Propagation Delay, Positive Going Output		600	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		200	NS	C_L=50pf, R_L=2kΩ

DUAL MONOSTABLE MULTIVIBRATOR

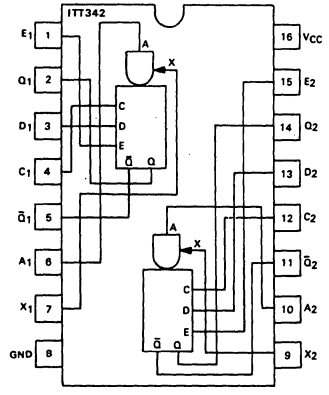
Two completely independent one-shots are provided on the 342 chip. Each one shot has an expandable trigger and provides complimentary output pulses of any length, as determined by an external timing capacitor. Outputs are active-high.

The 342 is triggered on the positive going edge of the input pulse. Maximum operating frequency is limited by the pulse width and recovery time of the particular circuit application. An external timing capacitor is required in conjunction with an internal or external timing resistor.

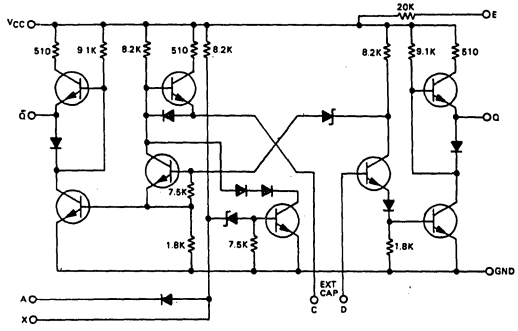
Pulse width is determined by the formula PW≈ 0.7 RC, with PW in Nanoseconds, R in ohms, and C in Picofarads. The timing capacitor C has no restriction on value, but the timing resistor should be held between 2 and 62 kΩ An internal 20 Km ±25% resistor is provided for normal applications.

Recovery time is given by $T_R = 3C$ with T_R in Nanoseconds and C in Picofarads. This is the time required to recharge the timing capacitor to the proper voltage.

Pin Configuration



Schematic (Each Multivibrator)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
342H-1, 342-1	−55°C to +125°C
342H-5	−30°C to +75°C
342-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
342-1, 342-5	−0.5V to 16.5V
342H-1, 342H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

ELECTRICAL CHARACTERISTICS 342-1, 342-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua, V_{IH}=6.5V
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5mA, V_{IL}=5.0V
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		17	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output		260	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		160	NS	C_L=50pf, R_L=2kΩ

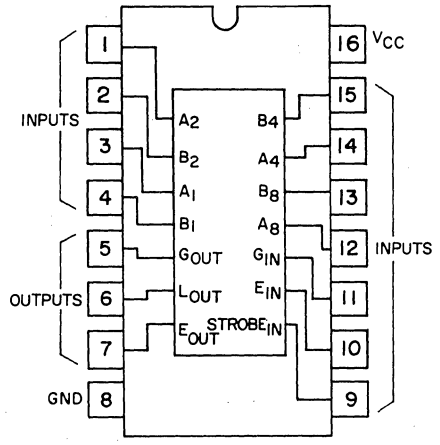
ELECTRICAL CHARACTERISTICS 342H-1, 342H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=11.0V, V_{IH}=6.5V I_{OH} =−50ua, V_{IH}=6.5V
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA, V_{IL}=5.0
I_{IH}	Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current		23	mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output		260	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		160	NS	C_L=50pf, R_L=2kΩ

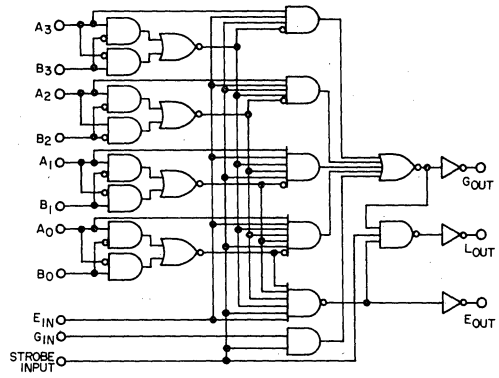
FOUR-BIT COMPARATOR

The ITT343 compares two four-bit binary numbers to give one of three active-high outputs indicating A <B, A=B, A> B. Inputs are provided so that 343's can be cascaded, enabling the system designer to compare n - bit numbers. A strobe is also provided to disable the unit.

Pinout (Top View)



Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
343H-1, 343-1	−55°C to +125°C
343H-5	−30°C to +75°C
343-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
343-1, 343-5	−0.5V to 16.5V
343H-1, 343H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

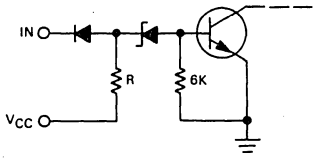
ITT343, ITT343H
FOUR-BIT COMPARATOR

Truth Table

Inputs				Outputs		
	E_{IN}	G_{IN}	Strobe	E_{OUT}	G_{OUT}	L_{OUT}
A>B	1	0	1	0	1	0
A=B	1	0	1	1	0	0
A<B	1	0	1	0	0	1
A>B	1	1	1	0	1	0
A=B	1	1	1	1	1	0
A<B	1	1	1	0	1	0
A>B	0	1	1	0	1	0
A=B	0	1	1	0	1	0
A<B	0	1	1	0	1	0
A>B	0	0	1	0	0	1
A=B	0	0	1	0	0	1
A<B	0	0	1	0	0	1
x	x	x	0	0	0	0

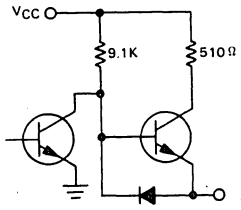
NOTE: If the device is being used correctly E_{IN} and G_{IN} will never be high at the same time. Whenever the strobe is low (logical "O"), all outputs will be low regardless of the input status.

Typical Input



R = 8.2K ON A,B
R = 16.4K ON G_{IN}
R = 4.1K ON E_{IN}, STROBE

Typical Output



ELECTRICAL CHARACTERISTICS 343-1, 343-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{IL}=5.0V I_{OH} =−50ua, V_{IH}=6.5V
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{IH}=6.5V I_{OL}=10.5mA, V_{IL}=5.0V
I_{IH}	Input High Level Current		 10 5 20	 ua ua ua	V_{cc}=13.0V, V_R=13.0V A, B Inputs G_1 Input E, S Inputs
I_{IL}	Input Low Level Current		 −2.1 —1.05 −4.2	 mA mA mA	V_{cc}=13.0V, V_F=1.5V A, B Inputs G_1 Input E, S Inputs
I_{CC}	Power Supply Current		42	mA	V_{cc}=13.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=12V, V_{IL}=5.0V V_{OH}=7.0V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output		1000	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		1000	NS	C_L=50pf, R_L=2kΩ

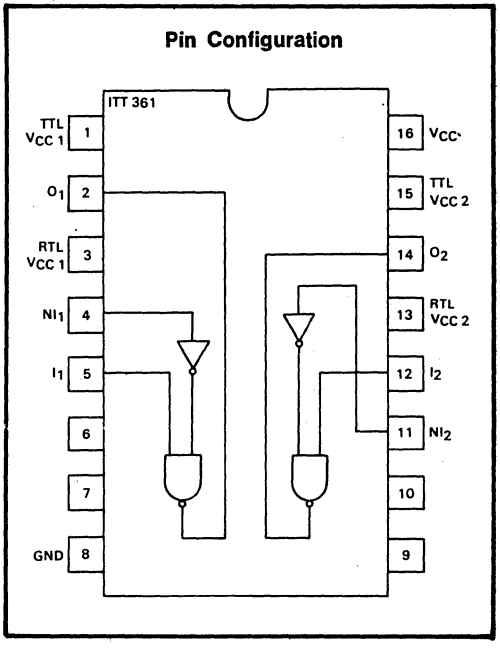
ELECTRICAL CHARACTERISTICS 343H-1, 343H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{IL}=5.0V I_{OH} =−50ua, V_{IA}=6.5V
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{IH}=6.5V I_{OL}=13.0mA, V_{IL}=5.0
I_{IH}	Input High Level Current		 10 5 20	 ua ua ua	V_{cc}=16.0V, V_R=16.0V A, B Inputs G_1 Input E, S Inputs
I_{IL}	Input Low Level Current		 −2.6 −1.3 −5.2	 mA mA mA	V_{cc}=16.0V, V_F=1.8V A, B Inputs G_1 Input E, S Inputs
I_{CC}	Power Supply Current 343H-1 343H-5		40 56	mA mA	V_{cc}=16.0V
I_{OH}	Output Source Current	−5.0		mA	V_{cc}=15.0V, V_{IL}=5.0V V_{OH}=9.5V, V_{IH}=6.5V
tpd+	Propagation Delay, Positive Going Output		1000	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		1000	NS	C_L=50pf, R_L=2kΩ

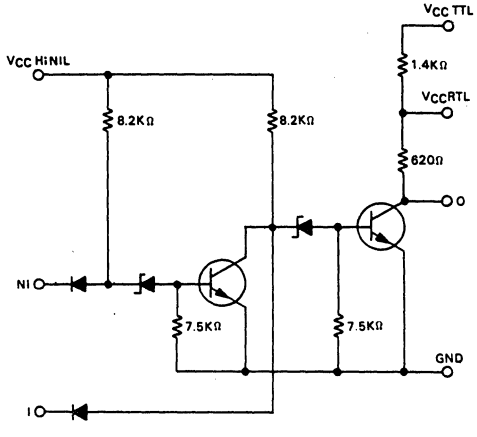
DUAL HIGH TO LOW INTERFACE

The ITT361 directly converts HiNIL signal levels to DTL, TTL, and RTL levels. The 361 output is connected directly to the low level logic input, and the 361 low level V_{CC} is connected to the low level power supply. The 361 can be used either as an inverting or non-inverting interface element, but only one of these functions should be used at a time, with the unused input disabled.

Pin Configuration



Schematic (Each Gate)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
361H-1, 361-1	−55°C to +125°C
361H-5	−30°C to +75°C
361-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
361-1, 361-5	−0.5V to 16.5V
361H-1, 361H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

ITT361, ITT361H
DUAL HIGH TO LOW INTERFACE

ELECTRICAL CHARACTERISTICS 361-1, 361-5 Over Recommended Operating Free Air Temperature Range

Parameter	Min	Max	Units	Test Conditions
V_{IH} Input High Threshold Voltage		6.5	V	
V_{IL} Input Low Threshold Voltage	5.0		V	
V_{OH} Output High Voltage TTL Interface	2.4		V	$H_INIL V_{CC}=11.0$ TTL $V_{CC}=4.5V$, $I_{OH}=-160ua$ $V_{IL}=5.0V$, $V_{IH}=6.50$
V_{OL} Output Low Voltage TTL Interface		0.4	V	$H_INIL V_{CC}=11.0$ TTL $V_{CC}=5.5V$, $I_{OL}=6.4mA$ $V_{IL}=5.0V$, $V_{IH}=6.50$
I_{IH} Input High Level Current		10	ua	$V_{cc}=13.0V$, $V_R=13.0V$
I_{IL} Input Low Level Current		−2.1	mA	$V_{cc}=13.0V$, $V_F=1.5V$
I_{CC} Power Supply Current		8	mA	$V_{cc}=13.0V$
V_{OL} Output Low Voltage RTL Interface				$H_INIL V_{CC}=11.0$ RTL $V_{CC}=3.0V$ $V_{IL}=5.0V$, $V_{IH}=6.50$
		0.35	V	+125°/+85°
		0.3	V	+25°
		0.33	V	−55°/—30°
I_{OH} Output Source Current RTL Interface				$H_INIL V_{CC}=11.0$ RTL $V_{CC}=3.0V$ $V_{IL}=5.0V$, $V_{IH}=6.50$
	−2.3		mA	361-1 $V_O=0.675V$ $T_A=+125°$
	−2.5		mA	$V_O=0.85V$ $T_A=+25$
	−2.5		mA	$V_O=1.0_1V$ $T_A=-55°$
	—2.0		mA	361-5 $V_O=0.76V$ $T_A=-85°$
	—2.2		mA	$V_O=0.85V$ $T_A=+25°$
	−2.3		mA	$V_O=0.9V$ $T_A=-30°$
tpd+ Propagation Delay, Positive Going Output		325	NS	$C_L=15pf$, $R_L=400\Omega$
tpd− Propagation Delay, Negative Going Output		260	NS	$C_L=15pf$, $R_L=400\Omega$

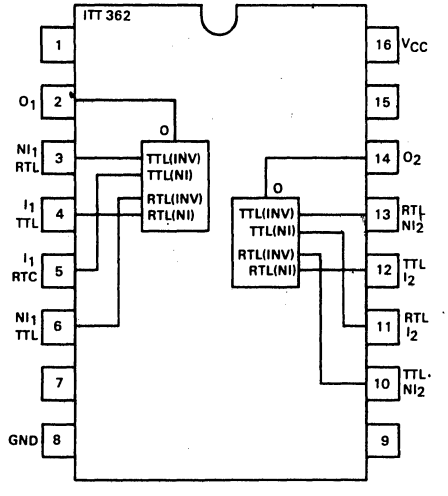
ELECTRICAL CHARACTERISTICS 361H-1, 361H-5 Over Recommended Operating Free Air Temperature Range

Parameter	Min	Max	Units	Test Conditions
V_{IH} Input High Threshold Voltage		6.5	V	
V_{IL} Input Low Threshold Voltage	5.0		V	
V_{OH} Output High Voltage TTL Interface	2.4		V	H_INIL Vcc=14.0v TTL V_{CC}=4.5V, I_{OH} =−160ua V_{IL}=5.0V, V_{IH}=6.50
V_{OL} Output Low Voltage TTL Interface		0.4	V	H_INIL Vcc=14.0v TTL V_{CC}=5.5V, I_{OL}=6.4mA V_{IL}=5.0V, V_{IH}=6.50
I_{IH} Input High Level Current		10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL} Input Low Level Current		−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC} Power Supply Current		11	mA	V_{cc}=16.0V
V_{OL} Output Low Voltage RTL Interface				H_INIL Vcc=14.0v RTL V_{CC}=3.0V V_{IL}=5.0V, V_{IH}=6.50
		0.35	V	+125/+70°
		0.3	V	+25°
		0.33	V	−55°/30°
I_{OH} Output Source Current RTL Interface				H_INIL Vcc=14.0v RTL V_{CC}=3.0V V_{IL}=5.0V, V_{IH}=6.50
	−2.3		mA	361H-1 V_O=0.675V T_A=+125°
	−2.5		mA	V_O=0.85V T_A=+25°
	−2.5		mA	V_O=1.01V T_A=−55°
	−2.0		mA	361H-5 V_O=0.76V T_A=+70°
	−2.2		mA	V_O=0.85V T_A=+25°
	−2.3		mA	V_O=0.9V T_A=−30°
tpd+ Propagation Delay, Positive Going Output		325	NS	C_L=15pf, R_L=400Ω
tpd− Propagation Delay, Negative Going Output		260	NS	C_L=15pf, R_L=400Ω

DUAL LOW TO HIGH INTERFACE

The ITT362 converts low level signals from TTL or RTL to high level signals for H_1NIL processing. Both inverting and non-inverting inputs are available for interfacing with RTL or TTL. Only one input should be used at a time, with the other three being tied to Vcc or ground to remove them from the circuit.

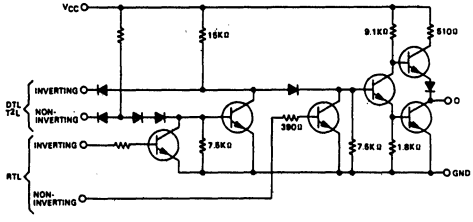
Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
362H-1, 362-1	−55°C to +125°C
362H-5	−30°C to +75°C
362-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage	
TTL Inputs	−0.5V to 8.0V
RTL Inputs	−0.5V to 5.0V
Voltage applied to output	−0.5V to Vcc
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

Schematic



ITT362, ITT362H
DUAL LOW TO HIGH INTERFACE

ELECTRICAL CHARACTERISTICS 362-1, 362-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions	
V_{IH}	Input High Threshold Voltage					
V_{IL}	Input Low Threshold Voltage	0.7		V		362-1
		0.8		V		362-5
V_{OH}	Output High Voltage TTL Inputs	8.5		V	Vcc=11.0V I_{OH} =−50ua One Input at Threshold	
V_{OL}	Output Low Voltage TTL Inputs		1.5	V	Vcc=11.0V I_{OL}=10.5 mA One Input at Threshold	
I_{IH}	Input High Level Current		10	ua	Vcc=13.0V, V_R=4.0V	
			−1.6	mA	Vcc=13.0V, V_F=0.4V	
I_{CC}	Power Supply Current		.10	mA	V_{cc}=13.0V	
tpd+	Propagation Delay, Positive Going Output		400	NS	C_L=50pf, R_L=2kΩ	
tpd−	Propagation Delay, Negative Going Output		335	NS	C_L=50pf, R_L=2kΩ	

ELECTRICAL CHARACTERISTICS 362H-1, 362H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions	
V_{IH}	Input High Threshold Voltage TTL Inputs			V		
V_{IL}	Input Low Threshold Voltage TTL Inputs	0.7		V		362H-1
		0.8		V		362H-5
V_{OH}	Output High Voltage	11.5		V	V_{cc}=14.0V I_{OH} =−50ua One Input at Threshold	
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=11.0V I_{OL}=10.5 mA One Input at Threshold	
I_{IH}	Input High Level Current TTL Inputs		10	ua	V_{cc}=16.0V, V_R=4.0V	
I_{IL}	Input Low Level Current TTL Inputs		−1.6	mA	V_{cc}=16.0V, V_F=0.4V	
I_{CC}	Power Supply Current		13.0	mA	V_{cc}=16.0V	
tpd+	Propagation Delay, Positive Going Output		400	NS	C_L=50pf, R_L=2kΩ	
tpd−	Propagation Delay, Negative Going Output		335	NS	C_L=50pf, R_L=2kΩ	

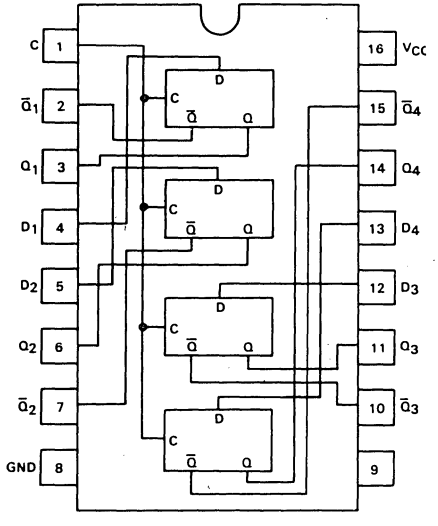
RTL INPUT SPECIFICATIONS FOR 362, 362H

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		1.01	V	362-1, 362H-1@−55°
			0.95	V	362-5, 362H-5@−30°
			0.85	V	362-1, 362H-1, 362-5,
			0.70	V	362H-5@+25°C
			0.675	V	362-5, 362H-5@+70/+75°
					362-1, 362H-1@125°
V_{IL}	Input Low Threshold Voltage		0.71		362-1, 362H-1@−55°
			0.6		362-5, 362H-5@−30°
			0.5		362-1, 362H-1, 362-5,
			0.38		362H-5@+25°C
			0.32		362-5, 362H-5@+70/85°
					362-1, 362H-1@125°
I_{IH}	Input High Level Current		0.495	mA	362-1, 362H-1@−55°
			0.460	mA	362-5, 362H-5@−30°
			0.440	mA	362-1, 362H-1, 362-5,
			0.470	mA	362H-5@+25°C
			0.470	mA	362-5, 362H-5@+70/85°
					362-1, 362H-1@125°
					Inputs at V_{IH}, Vcc-13V for 362-1, 362-5, Vcc-16V for 362H-1, 362H-5
I_{IL}	Input Low Level Current		10	uA	Inputs at V_{IL} Vcc=13V for 362-1, 362-5 Vcc=16V for 362H-1, 362H-J

QUAD D FLIP-FLOP

Four D-type flip-flops utilizing a common clock line make up the 370. Each flip-flop has complimentary passive pull up outputs with a single D input. This circuit is ideal as a quad latch for temporary storage of 4-bit binary numbers. Data is transferred from D inputs to outputs when the clock line is low. With the clock line high, output data is held and D inputs are ignored.

Pin Configuration



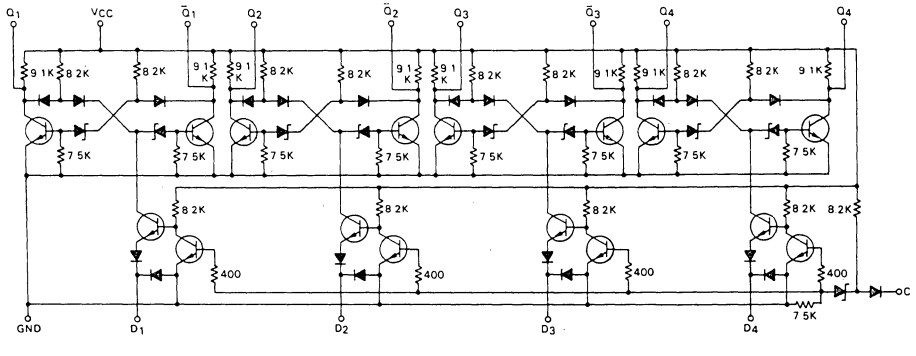
ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
370H-1, 370-1	−55°C to +125°C
370H-5	−30°C to +75°C
370-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
370-1, 370-5	−0.5V to 16.5V
370H-1, 370H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

TRUTH TABLE

C	D	Q_{n+1}
1	1	Q_n
1	0	Q_n
0	1	1
0	0	0

Schematic



ELECTRICAL CHARACTERISTICS 370-1, 370-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	10.0		V	V_{cc}=11.0V, V_{1L}=5.0V I_{OH} = −40ua, V_{IH}=6.5V
V_{OL}	Output Low Voltage		1.5	V	V_{cc}=11.0V, V_{1H}=6.5V I_{OL}=8.4mA
I_{IH}	Input High Level Current		 10 20	 ua ua	V_{cc}=13.0V, V_R=13.0V C Input D Inputs
I_{IL}	Input Low Level Current		 −2.1 −4.2	 mA mA	V_{cc}=13.0V, V_F=1.5V C Input D Inputs
I_{CC}	Power Supply Current		38	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output		500	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		500	NS	C_L=50pf, R_L=2kΩ

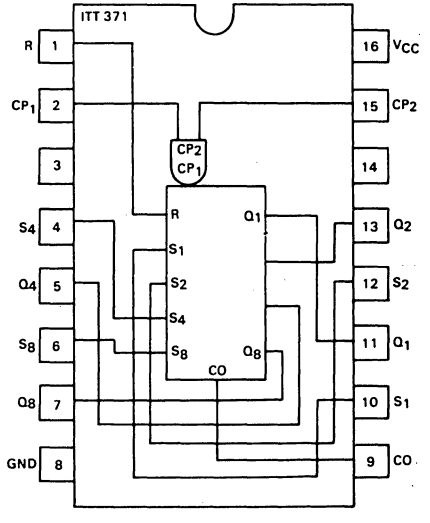
ELECTRICAL CHARACTERISTICS 370H-1, 370H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage	13.0		V	V_{cc}=14.0V, V_{1L}=5.0V I_{OH} =.40ua, V_{IH}=6.5V
V_{OL}	Output Low Voltage		1.8	V	V_{cc}=14.0V, V_{1H}=6.5V I_{OL}=10.4mA
I_{IH}	Input High Level Current		 10 20	 ua ua	V_{cc}=16.0V, V_R=16.0V C Input D Inputs
I_{IL}	Input Low Level Current		 −2.6 −5.2	 mA mA	V_{cc}=16.0V, V_F=1.8V C Input D Inputs
I_{CC}	Power Supply Current 370H-1 370H-5		40 48	mA mA	V_{cc}=16.0V
tpd+	Propagation Delay, Positive Going Output C− Q+		500	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output C− Q+		500	NS	C_L=50pf, R_L=2kΩ

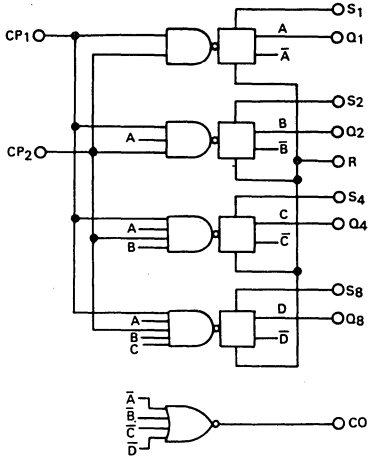
DECADE COUNTER

The ITT371 HLL MS1 counter generates BCD on its outputs. It has direct set inputs for each of its four internal flip-flops and a common reset. Two clock inputs are provided, facilitating the input ENABLE function. A ninth count output is provided as a carry output for cascading 371's so a decimal number of any size may be generated. The passive outputs are ideal inputs to the 380 Series BCD decoders. The 371 is level sensitive, counting as the clock goes low. Holding either clock low will inhibit the count sequence. Direct set or reset is accomplished by switching the desired input high. All unused direct set and reset inputs must be grounded.

Pin Configuration



Logic Diagram

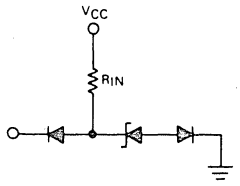


ABSOLUTE MAXIMUM RATINGS

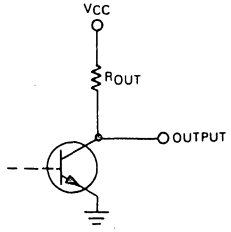
Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
371H-1, 371-1	−55°C to +125°C
371H-5	−30°C to +75°C
371-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
371-1, 371-5	−0.5V to 16.5V
371H-1, 371H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

ITT371, ITT371H
DECADE COUNTER

TYPICAL INPUT



TYPICAL OUTPUT



Input	R_{IN}
CP_1 CP_2	5 KΩ Typ.
Reset	5 KΩ Typ.
All Sets	20 KΩ Typ.

Output	R_{OUT}
Q_1 Q_2	9.1 KΩ Typ.
$Q_3 + Q_4$	9.1 KΩ Typ.
CO	

TRUTH TABLE

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	Q_1 Q_8
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	1
1	1	0	0	1	1

ELECTRICAL CHARACTERISTICS 371-1, 371-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage				V_{cc}=11.0V, V_{IL}=5.0V V_{IH}=6.5V
		10.0		V	C Output I_{OH}=−20μA
		10.0		V	Q Outputs I_{HO}=−50uA
V_{OL}	Output Low Voltage				V_{cc}=11.0V, V_{IH}=6.5V V_{IL}=5.0V
			1.5	V	C Output I_{OL}=4.2mA
			1.5	V	Q Outputs I_{OL}=10.5mA
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			20	ua	CP Inputs
			10	ua	R Input
			5	ua	S Inputs
I_{IL}	Input Low Level Current				V_{cc}=13.0V
			−4.2	mA	CP Inputs
			−2.1	mA	R Input
			−1.05	mA	S Inputs

ELECTRICAL CHARACTERISTICS 371-1, 371-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
I_{CC}	Power Supply Current		41	mA	
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			800	NS	C− Q+
			600	NS	S+ Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			300	NS	C− Q−
			200	NS	R+ Q−

ELECTRICAL CHARACTERISTICS 371H-1, 371H-5 Over Recommended Operating Free Air Temperature Range

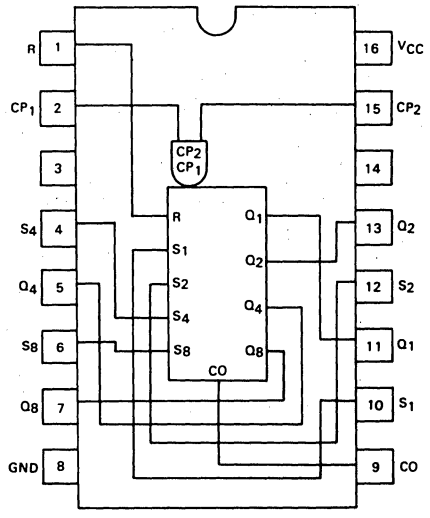
Parameter		Min	Max	Units	Test Conditions	
V_{IH}	Input High Threshold Voltage		6.5	V		
V_{IL}	Input Low Threshold Voltage	5.0		V		
V_{OH}	Output High Voltage				V_{cc}=14.0V, V_{IL}=5.0V V_{IH}=6.5V	
		13.0		V	C Output I_{OH}=−20μA	
		13.0		V	Q Outputs IOH=−50ua	
V_{OL}	Output Low Voltage				V_{cc}=14.0V, V_{IL}=5.0V V_{IH}=6.5V	
			1.8	V	C Output I_{OL}=5.2mA	
			1.8	V	Q Outputs I_{OL}=13.0mA	
I_{IH}	Input High Level Current				V_{cc}=16.0V, V_R=16.0V	
			20	ua	CP Inputs	
			10	ua	R Input	
			5	ua	S Inputs	
I_{IL}	Input Low Level Current		−5.2	mA	CP Inputs	
			−2.6	mA	R Input	
			−1.3	mA	S Inputs	
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V	371H-1
			53	mA		371H-5
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ	
			800	NS	C− Q+	
			600	NS	S+ Q+	
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ	
			300	NS	C− Q−	
			200	NS	R+ Q−	

DIVIDE BY 16 (HEXADECIMAL) COUNTER

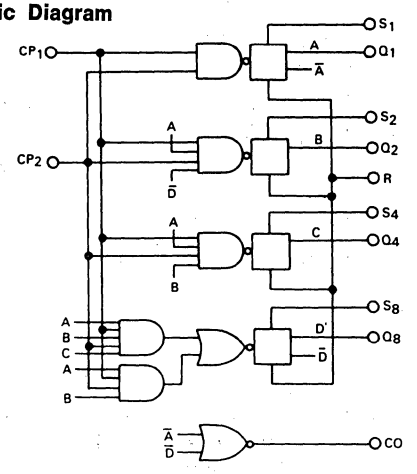
The ITT372 is identical to the ITT371 except its outputs are coded in the standard 4-bit binary (1-2-4-8) code.

Operation of the 372 is identical to that of the 371. Internal construction produces divide-by-sixteen operation.

Pin Configuration



Logic Diagram

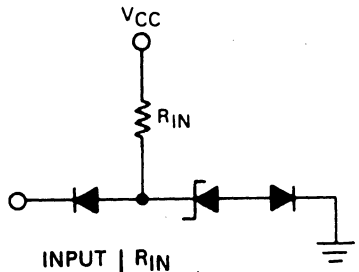


ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
372H-1, 372-1	−55°C to +125°C
372H-5	−30°C to +75°C
372-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
372-1, 372-5	−0.5V to 16.5V
372H-1, 372H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to V_{CC}
Sink Current, Continuous Buffers	80mA
All Other Devices	25mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

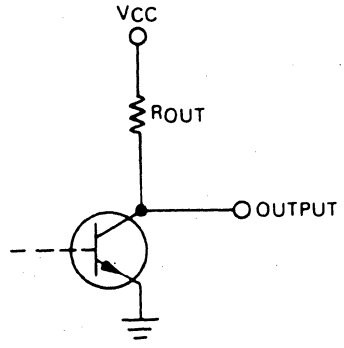
ITT372, ITT372H
DIVIDE BY 16 (HEXADECIMAL) COUNTER

Typical Input



INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	5 KΩ TYP.
ALL SETS	20 KΩ TYP.

Typical Output



OUTPUT	R_{OUT}
Q_1 Q_2	9.1 KΩ TYP.
$Q_3 + Q_4$ CO	9.1 KΩ TYP.

Truth Table

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	Q_1 Q_2 Q_4 Q_8
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	0	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	0
1	0	0	1	1	0
0	1	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	1	1	1	1
1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS 372-1, 372-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage				V_{cc}=11.0V, V_{IL}=5.0V V_{IH}=6.5V
		10.0		V	C Output I_{OH}=−50uA
		10.0		V	Q Outputs I_{OH}=−50uA
V_{OL}	Output Low Voltage				V_{cc}=11.0V, V_{IH}=6.5V V_{IL}=5.0V
			1.5	V	C Output I_{OL}=4.2mA
			1.5	V	Q Outputs I_{OL}=10.5mA
I_{IH}	Input High Level Current				V_{cc}=13.0V, V_R=13.0V
			20	ua	CP Inputs
			10	ua	R Input
			5	ua	S Inputs
I_{IL}	Input Low Level Current				V_{cc}=13.0V, V_F=1.5V
			−4.2	mA	CP Inputs
			−2.1	mA	R Input
			—1.05	mA	S Inputs
I_{CC}	Power Supply Current		41	mA	V_{cc}=13.0V
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			800	NS	C− Q+
			600	NS	S+ Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			300	NS	C− Q−
			200	NS	R+ Q−

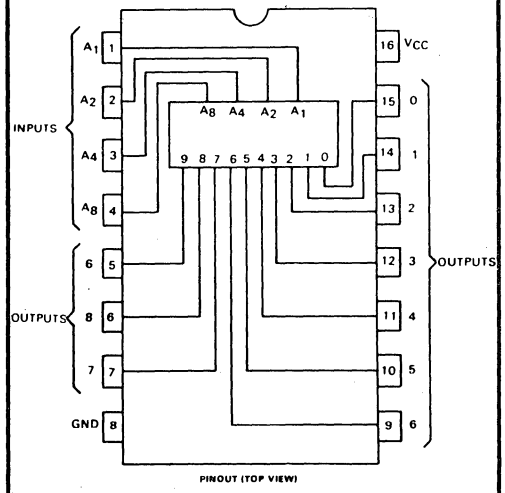
ELECTRICAL CHARACTERISTICS 372H-1, 372H-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OH}	Output High Voltage				V_{cc}=14.0V, V_{IL}=5.0V V_{IH}=6.5V
		13.0		V	C Output I_{OH}=−20μA
		13.0		V	Q Outputs I_{OH}=−50uA
V_{OL}	Output Low Voltage				V_{cc}=14.0V, V_{IL}=5.0V V_{IH}=6.5V
			1.8	V	C Output I_{OL}=5.2mA
			1.8	V	Q Outputs I_{OL}=13.0mA
I_{IH}	Input High Level Current				V_{cc}=16.0V, V_R=16.0V
			20	ua	CP Inputs
			10	ua	R Input
			5	ua	S Inputs
I_{IL}	Input Low Level Current				
			−5.2	mA	CP Inputs
			−2.6	mA	R Input
			−1.3	mA	S Inputs
I_{CC}	Power Supply Current		40	mA	V_{cc}=16.0V 37H-1
			53	mA	37H-5
tpd+	Propagation Delay, Positive Going Output				C_L=50pf, R_L=2kΩ
			800	NS	C− Q+
			600	NS	S+ Q+
tpd−	Propagation Delay, Negative Going Output				C_L=50pf, R_L=2kΩ
			300	NS	C− Q−
			200	NS	R+ Q−

BCD TO DECIMAL DECODER

The ITT380 and ITT381 decode standard BCD (1-2-4-8) inputs to produce a low state on one of the ten open collector outputs. Internal design insures that no ambiguous outputs are produced, turning off all outputs when addressed by input codes for 10-15. The ITT380 is intended to drive small lamps directly or can be used with various interface buffering schemes. The ITT381 is identical to the ITT380 with the exception of its output ratings and is intended for use as an internal circuit element.

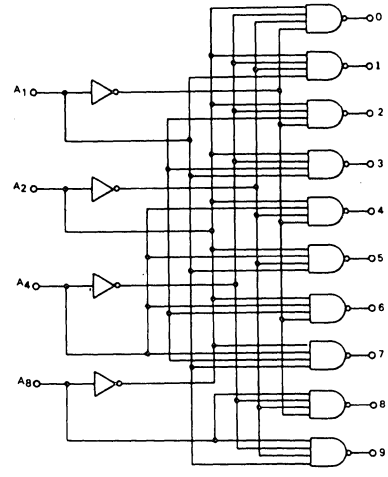
PIN CONFIGURATION



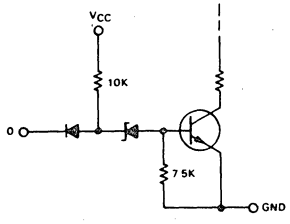
ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
380H-1, 380-1, 381H-1	−55°C to +125°C
380H-5, 381H-5, 381-1	−30°C to +75°C
380-5, 381-5	−30°C to +85°C
Lead Temperature, 1/16 inch from case, 60 seconds Maximum	300°C
Supply Voltage	
Continuous	+16.5V
Pulsed 0.1 Second	18V
Input Voltage (exclusive of expanders)	
380-1, 381-1, 380-5, 381-5	−0.5V to 16.5V
380H-1,381H-1,380H-5,381H-5	−0.5V to 18V
Input Voltage - Expanders	0V to 6.0V
Voltage applied to output	−0.5V to
Sink Current, Continuous	40mA
Output short circuit duration to ground	Continuous
(Not more than 1 output shorted simultaneously)	
Maximum package power dissipation (free air)	
at +125°	500mw
at +85°	900mw

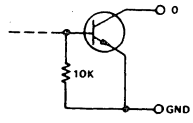
LOGIC DIAGRAM



TYPICAL INPUT



TYPICAL OUTPUT



ITT380, ITT381, ITT380H, ITT381H
BCD TO DECIMAL DECODER

Truth Table

Inputs				Outputs									
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS 380H-1, 381H-1, 380H-1 Over Recommended Operating Free Air Temperature Range

Parameter			Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage			6.5	V	
V_{IL}	Input Low Threshold Voltage		5.0		V	
V_{OL}	Output Low Voltage					V_{cc}=14.0V, V_{IL}=5.0V V_{IH}=6.5V
		380		1.2	V	I_{OL}=30mA
				0.4	V	I_{OL}=6.4mA
		381		1.8	V	I_{OL}=20.8mA
				0.4	V	I_{OL}=6.4mA
I_{IH}	Input High Level Current			10	ua	V_{cc}=16.0V, V_R=16.0V
I_{IL}	Input Low Level Current			−2.6	mA	V_{cc}=16.0V, V_F=1.8V
I_{CC}	Power Supply Current			38	mA	V_{cc}=16.0V
I_{CEX}	Output Leakage Current			25	μA	V_{CC}=16.0V, V_{IL}=5.0V V_{IH}=6.5V
LV_{CE}	Collector Latching Voltage					V_{CEX}=16.0V V_{CC}=16.0V, V_{IL}=5.0V V_{IH}=6.5V I_{CE}=0.5mA
		380	24.0		V	
		381	16.0		V	

ELECTRICAL CHARACTERISTICS 380H-1, 381H-1, 380H-1 Over Recommended Operating Free Air Temperature Range **(continued)**

Parameter		Min	Max	Units	Test Conditions
tpd+	Propagation Delay, Positive Going Output		500	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		500	NS	C_L=50pf, R_L=2kΩ

ELECTRICAL CHARACTERISTICS 380-1, 381-1, 380-5, 381-5 Over Recommended Operating Free Air Temperature Range

Parameter		Min	Max	Units	Test Conditions
V_{IH}	Input High Threshold Voltage		6.5	V	
V_{IL}	Input Low Threshold Voltage	5.0		V	
V_{OL}	Output Low Voltage				V_{cc}=11.0V, V_{IL}=5.0V V_{IH}=6.5V
	380		1.2	V	I_{OL}=30mA
			0.4	V	I_{OL}=10.5mA
	381		1.2		I_{OL}=16.8mA
			0.4		I_{OL}=6.4mA
I_{IH}	Input High Level Current		10	ua	V_{cc}=13.0V, V_R=13.0V
I_{IL}	Input Low Level Current		−2.1	mA	V_{cc}=13.0V, V_F=1.5V
I_{CC}	Power Supply Current		30	mA	V_{cc}=13.0V
I_{CEX}	Output Leakage Current		25	μA	V_{CC}=13.0V, V_{IL}=5.0V V_{IH}=6.5V V_{CEX}=13.0V
LV_{CE}	Collector Latching Voltage				V_{CC}=13.0V, V_{IL}=5.0V V_{IH}=6.5V I_{CE}=0.5mA
	380	24.0		V	
	381	15.0		V	
tpd+	Propagation Delay, Positive Going Output		500	NS	C_L=50pf, R_L=2kΩ
tpd−	Propagation Delay, Negative Going Output		500	NS	C_L=50pf, R_L=2kΩ

Package: 16 Pin Ceramic and Plastic Dual In-Line

SENSE AMPLIFIERS

HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

Performance Features

- **High speed and fast recovery time**
- **Time and amplitude signal discrimination**
- **Adjustable input threshold voltage levels**
- **Narrow region of threshold voltage uncertainty**
- **Multiple differential-input preamplifiers**
- **High d-c noise margin—typically one volt**
- **Good fan-out capability**

Ease-of-Design Features

- **Choice of output circuit function**
- **TTL or DTL drive capability**
- **Standard logic supply voltages**
- **Plug-in configuration ideal for flow-soldering techniques**
- **Pins on 100-mil grid spacings for industrial-type circuit boards**

Description

The ITT7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry betweeen the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple, differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise-ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The ITT7520 and ITT7521 circuits may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The ITT7522 and ITT7523 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an ITT7520 or ITT7521 circuit, or to perform the wired-AND function.

The ITT7524 and ITT7525 circuits provide for independent, dual-channel sensing with separate outputs.

The ITT7528 and ITT7529 circuits are similar to the ITT7524 and ITT7525 except that the output of each preamplifier is available as a test point.

NOTICE

Series 7520 will also be available in —55°C to 125°C temperature range. Data sheet to be published will contain the necessary specifications. please notify factory of your data requirements.

Design Characteristics

The ITT7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly snsitive to changes in the d-c levels throughout the amplifier. This was due primarily to the requried tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of ITT-7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a functon not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

Circuit Operation

The basic ITT7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept which takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage which is distributed to the input amplifiers. Application of an input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T.

The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier, through changes in temperature or power-supply voltage levels, are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.

The second stage of the input amplifier is a TTL gate. The gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

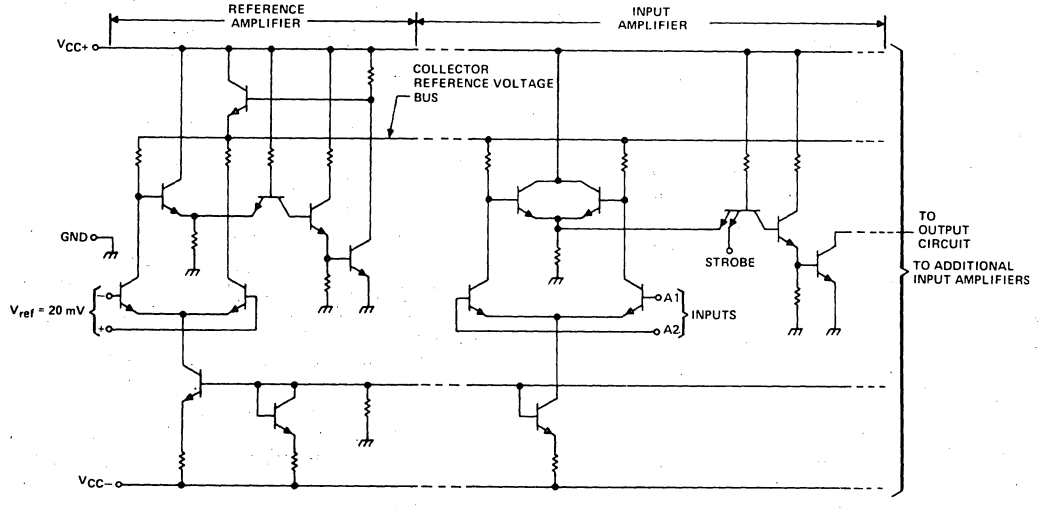


Figure A—Basic ITT7520 Sense-Amplifier Circuit

The logic inputs (i.e., gate and strobe) of ITT-7520 sense amplifiers are designed to be compatible with TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same guaranteed noise margin and logic threshold voltage as for TTL are assured each of the gate and strobe inputs. This is accomplished by testing each logic input under standard TTL test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

ITT7520 and ITT7521 Circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output crcuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Y input results in a flip-flop or register Z to G_Y results in output pulse stretching. In either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of ITT7520/ITT7521 can be expanded by connecting the Y output of ITT7522/ITT7523 to the G_Y input of the circuit being expanded.

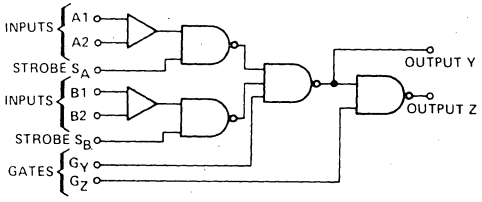


Figure B
ITT7520/ITT7521 Logic Diagram

Logic:

$Y = G_Y + A \circ S_A + B \bullet S_B$

$Z = \overline{G_Z \circ Y}$

$Z = G_Z + G_Y (\overline{A \circ S_A}) (\overline{B \bullet S_B})$

ITT7522 and ITT7523 Circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output which permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the ITT7520/ITT7521 circuit.

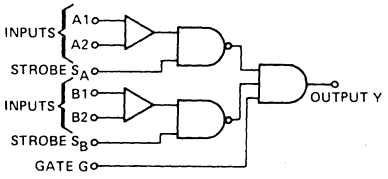


Figure C
ITT7522/ITT7523 Logic Diagram

Logic:

$Y = G (\overline{A \bullet S_A}) (\overline{B \bullet S_B})$

ITT7524 and ITT7525 Circuit

This circuit features two completely independ sense amplifiers in a single package. Each channel features high fan-out capability.

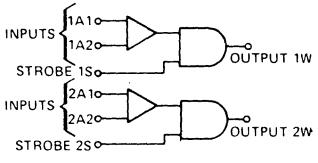


Figure D
ITT7524/ITT7525 Logic Diagram
ITT75234/ITT75235 Same Except Inverted Output

Logic:

$W = \overline{AS}$ for ITT7524 and ITT7525

$W = AS$ for ITT75234 and ITT75235

ITT7528 and ITT7529 Circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

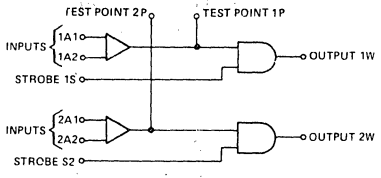


Figure F
ITT7528/ITT7529 Logic Diagram

Logic:
W = AS for ITT7528 and ITT7529

ITT75234, ITT75235, ITT75238, ITT75239 Circuits

These dual sense amplifier circuits are the same as ITT7524, ITT7525, ITT7528, and ITT7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added.

Reference Voltage Considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. Several methods may be used to supply this reference voltage; however, methods given here will be limited to the discussion of fundamental design considerations. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure G. This type of voltage divider may be used to supply an individual reference amplifier or to supply a numbr of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (normally 30μA) therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

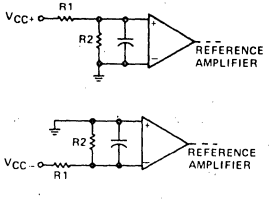


Figure G

Input Line Layout Considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors, and use of a good ground plane to separate strobe and output lines from sense and reference input lines, is recommended.

Sense-input Termination Resistor Considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values which will be compatible with the particular application. Matched termination resistors, (R_T, Figure H), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

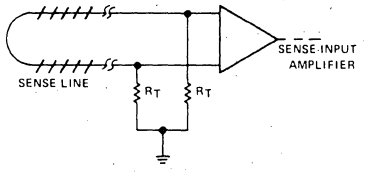


Figure H

Output Drive Capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current. This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the ITT7522/ITT7523 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

Logic Input Current Requirements

Logic input current requirements are specified at worst-case power-supply conditions over the operating free-air temperature range of 0°C to 70°C. The logic input currents are identical to and compatible with TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. current into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Absolute Maximum Ratings (over free-air temperature range unless otherwise noted)

Supply voltages (see Note 1):
V_{CC+} 7V
V_{CC-} ..... −7V
Differential input voltage, V_{ID} or V_{ref} ..... ±5V
Voltage from any input to ground (see Note 2) 5.5V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} −55°C to 150°C

Recommended Operating Conditions

	Min	Nom	Max	Unit
V_{CC+} (see Note 1)	4.75	5	5.25	V
V_{CC-} (see Note 1)	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

NOTES:
1. These voltage values are with respect to network ground terminal.

2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

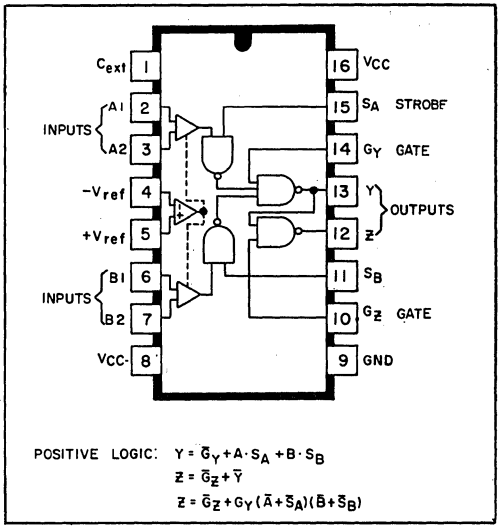
ITT SEMICONDUCTORS

DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLEMENTARY OUTPUTS

TRUTH TABLE

Inputs						Outputs	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

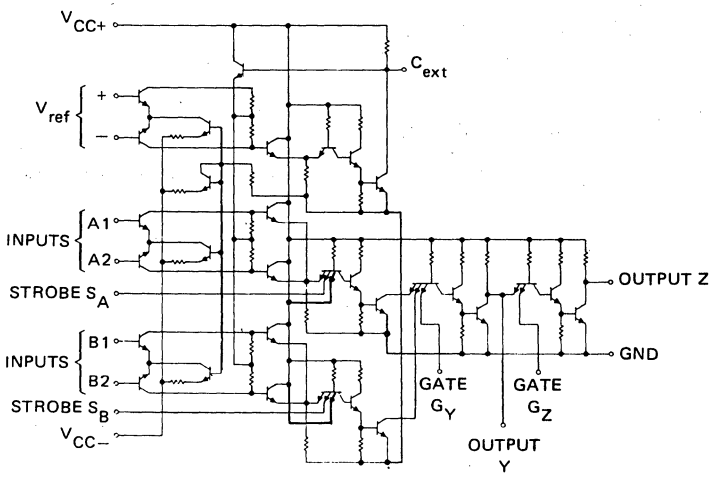
$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

Definition of Logic Levels

Input	H	L	X
A or B*	$V_{ID} \geqslant V_T$ max	$V_{ID} \leqslant V_T$ min	Irrelevant
Any G or S	$V_I \geqslant V_{IH}$ min	$V_I \leqslant V_{IL}$ max	Irrelevant

* A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

Schematic



ITT7520, ITT7521
DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLIMENTARY OUTPUTS

ELECTRICAL CHARACTERISTICS (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$V, $T_A = 0°C$ to $70°C$)

	Parameter	Test Fig.	Min	Typ**	Max	Unit	Test Conditions	
V_T	Differential input threshold voltage	1	(10)11	15	(20)19	mV	V_{ref} = 15mV	ITT7520 (5520)*
			8	15	22	mV		ITT7521 / 5521
			(35)36	40	(45)44	mV	V_{ref} = 40 mV	ITT7520 (5520)
			33	40	47	mV		ITT7521 / 5521
V_{ICF}	Common-mode input firing voltage			±2.5		V	V_{ref} = 40 mV Common-mode input pulse: t_r = 15 ns, $t_f \leqslant$ 15 ns t_w = 50 ns	
I_{IB}	Differential-input bias current	2		30	75 (100)	µA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, (5520/21) V_{ID} = 0	
I_{IO}	Differential-input offset current	2		3		µA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	
V_{IH}	High-level input voltage (strobe and gate inputs)	3	2			V		
V_{IL}	Low-level input voltage (strobe and gate inputs)	3			0.8	V		
V_{OH}	High-Level output voltage	3	2.4	4		V	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 µA	
V_{OL}	Low-level output voltage	3		0.25	0.4	V	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA	
I_{IH}	High-level input current (strobe and gate inputs)	4			40	µA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V V_{IH} = 2.4 V	
					1	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V V_{IH} = 5.25 V	
I_{IL}	Low-level input current (strobe and gate inputs)	4		−1	−1.6	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V V_{IL} = 0.4 V	
$I_{os(Y)}$	Short-circuit output current into Y	5	−3		−5	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	
$I_{os(Z)}$	Short-circuit output current into Z	5	−2.1		−3.5	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	
I_{CC+}	Supply current from V_{CC+}	6		28	35	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V T_A = 25 C	
I_{CC-}	Supply current from V_{CC-}	6		−14	−18	mA	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V T_A = 25 C	

** All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$

* Numbers in parenthesis apply to 5520 or 5521 as indicated.

SWITCHING CHARACTERISTICS, $V_{CC+} = 5$ V, $V_{CC-} = -5$V, 100 pF, $T_A = 25°C$

Propagation Delay Times			Test					
Symbol	From Input	To Output	Fig.	Min	Typ	Max	Unit	Test Conditions
$t_{PLH(DY)}$	A1-A2 or B1-B2	Y	32		25	40	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(DY)}$					20		ns	
$t_{PLH(DZ)}$	A1-A2 or B1-B2	Z	32		30		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(DZ)}$					35	55	ns	
$t_{PLH(SY)}$	Strobe A or B	Y	32		15	39	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(SY)}$					20		ns	
$t_{PLH(SZ)}$	Strobe A or B	Z	32		30		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(SZ)}$					35	55	ns	
$t_{PLH(GY,\ Y)}$	Gate G_Y	Y	33		15	25	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(GY,\ Y)}$					10		ns	
$t_{PLH(GY,\ Z)}$	Gate G_Y	Z	33		15		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(GY,\ Z)}$					20	30	ns	
$t_{PLH(GZ,\ Z)}$	Gate G_Z	Z	34		15		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(GZ,\ Z)}$					10	20	ns	

TYPICAL RECOVERY AND CYCLE TIMES, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $C_{ext} \geqslant 100$ pF, $T_A = 25°C$

	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{or}D$	Differential-input overload recovery time (see Note 5)		20		ns	Differential Input Pulse: $V_{ID} = 2$ V, $t_r = t_f = 20$ ns
$t_{or}C$	Common-mode-input overload recovery (see Note 6)		20		ns	Common-Mode-Input Pulse: $V_{IC} = \pm 2$ V, $t_r = t_f = 20$ ns
$t_{cyc(min)}$	Minimum cycle time		200		ns	

NOTES:

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

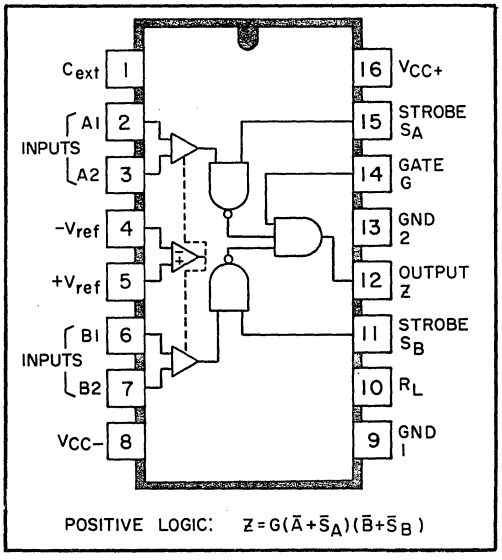
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

DUAL-CHANNEL SENSE AMPLIFIERS

TRUTH TABLE

Inputs					Output
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)

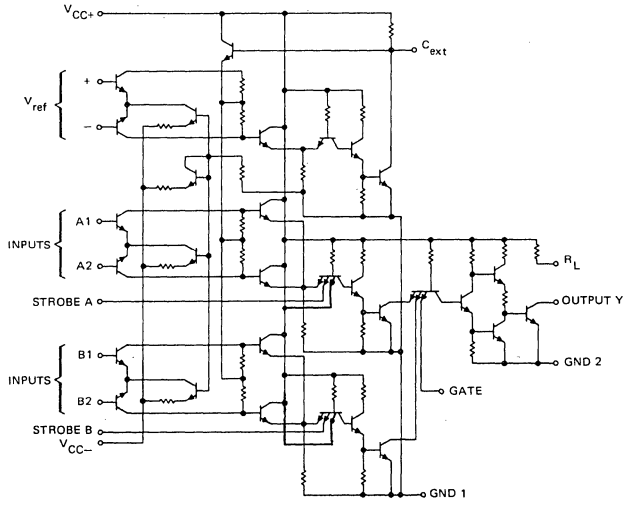


Definition of Logic Levels

Input	H	L	X
A or B*	$V_{ID} \geqslant V_T$ max	$V_{ID} \leqslant V_T$ min	Irrelevant
Any G or S	$V_I \geqslant V_{IH}$ min	$V_I \leqslant V_{IL}$ max	Irrelevant

* A and B are differential voltages (V_{ID}))between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

Schematic



ELECTRICAL CHARACTERISTICS

(unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, T_A = O°C to 70°C)

	Parameter	Test Fig.	Min	Typ**	Max	Unit	Test Conditions
V_T	Differential input threshold voltage (see Note 3, page 17)	7	(10)11	15	(20)19	mV	V_{ref}=15 mV, ITT7522 (5522)*
			8	15	22	mV	ITT7523 / 5523
			(35)36	40	(45)44	mV	V_{ref}=40mV, ITT7522 (5522)
			33	40	47	mV	ITT7523 / 5523
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)			±2.5		V	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ **Common-mode input pulse:** $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, $t_w = 50$ ns
I_{IB}	Differential-input bias current	2		30	75 (100)	μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, (5522/23) $V_{ID} = 0$
I_{IO}	Differential-input offset current	2		3		μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$
V_{IH}	High-level input voltage (strobe and gate inputs)	8	2			V	
V_{IL}	Low-level input voltage (strobe and gate inputs)	8			0.8	V	
V_{OH}	High-level output voltage	8	2.4	4		V	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA
V_{OL}	Low-level output voltage	8		0.25	0.4	V	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA
I_{IH}	High-level input current (strobe and gate inputs)	9			40	μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V
					1	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V
I_{IL}	Low-level input current (strobe and gate inputs)	9		−1	−1.6	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V
I_{OH}	High-level output current	10			250	μA	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $V_O = 5.25$ V
I_{OS}	Short-current output current	11	-2.1		−3.5	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V

*Numbers in parenthesis apply to 5522 or 5523 as indicated.

ELECTRICAL CHARACTERISTICS (continued)
(unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

Parameter		Test Fig.	Min	Typ**	Max	Unit	Test Conditions
I_{CC+}	Supply current from V_{CC+}	6		27	36	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$
I_{CC-}	Supply current from V_{CC-}	6		−15	−18	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$

** All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$

SWITCHING CHARACTERISTICS, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $C_{ext} \geqslant 100$ pF, $T_A = 25°C$

Propagation Delay Times			Test					
Symbol	From Imput	To Output	Fig.	Min	Typ	Max	Unit	Test Conditions
$t_{PLH(D)}$	A1-A2 or B1-B2	Y	35		20		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(D)}$					30	45	ns	
$t_{PLH(S)}$	Strobe A or B	Y	35		20		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(S)}$					20	40	ns	
$t_{PLH(G)}$	Gate	Y	36		10		ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(G)}$					15	25	ns	

TYPICAL RECOVERY AND CYCLE TIMES, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $C_{ext} \geqslant 100$ pF, $T_A = 25°C$

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{orD}	Differential-input overload recovery time (see Note 5)		20		ns	Differential Input Pulse: $V_{ID} = 2$ V, $t_r = t_f = 20$ ns
t_{orC}	Common-mode-input overload recovery (see Note 6)		20		ns	Common-Mode Input Pulse: $V_{IC} = \pm 2$V, $t_r = t_f = 20$ ns
$t_{cyc(min)}$	Minimum cycle time		200		ns	

NOTES:
5. Differential-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

DUAL SENSE AMPLIFIERS

TRUTH TABLE

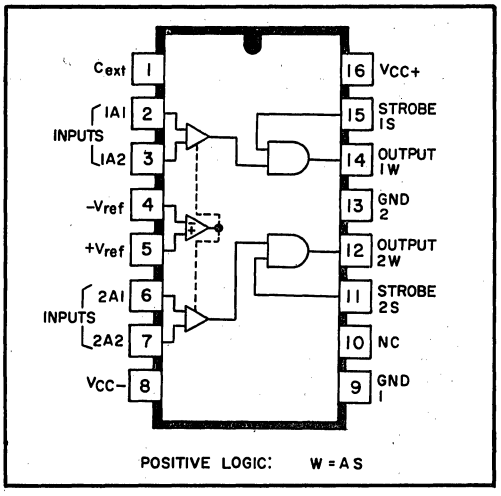
INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	X	L
X	L	L

Definition of Logic Levels

Input	H	L	X
A*	$V_{ID} \geqslant V_{T\ max}$	$V_{ID} \leqslant V_{T\ min}$	Irrelevant
S	$V_I \geqslant V_{IH\ min}$	$V_I \leqslant V_{IL\ max}$	Irrelevant

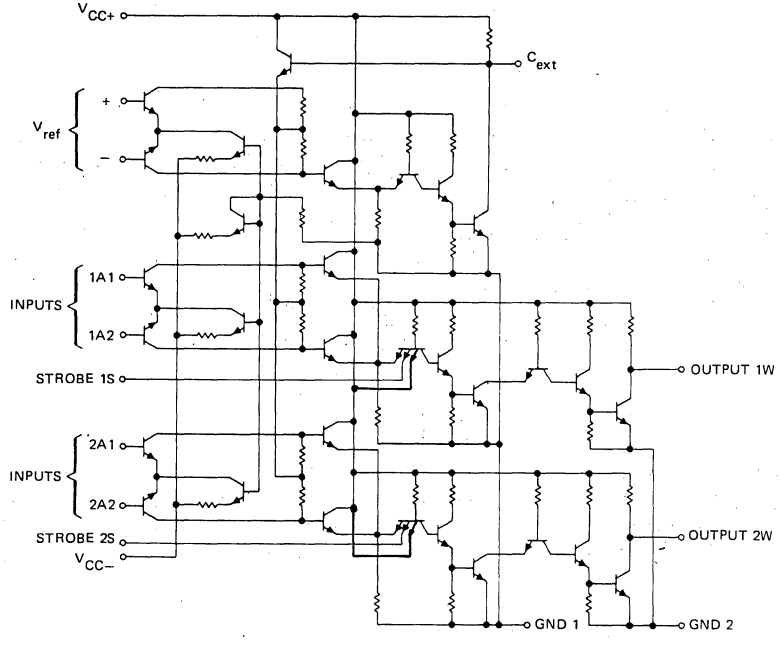
* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



NC - NO INTERNAL CONNECTION

Schematic



ELECTRICAL CHARACTERISTICS (unless otherwise noted $V_{cc+} = 5$ V, $V_{cc-} = -5$ V, T_A = 0°C to 70°C)

	Parameter	Test Fig.	Min	Typ*	Max	Unit	Test Conditions
V_T	Differential-input threshold voltage (see Note 3, page 17)	12	(10)11	15	(20)19	mV	V_{ref} = 15 mV ITT7524(5524)*
			8	15	22	mV	ITT7525/ 5525
			(35)36	40	(45)44	mV	V_{ref} = 40mV ITT7524(5524)
			33	40	47	mV	ITT7525/ 5525
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)			±2.5		V	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leqslant$ 15ns, $t_r \leqslant$ 15 ns, t_w = 50 ns
I_{IB}	Differential-input bias current	2		30	75 (100)	μA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, (5524/25) V_{ID} = 0
I_{IO}	Differential-input offset current	2		− 3		μA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, V_{ID} = 0
V_{IH}	High-level input voltage (strobe inputs)	13	2			V	
V_{IL}	Lov-level input voltage (strobe inputs)	13			0.8	V	
V_{OH}	High-level output voltage	13	2.4	4		V	V_{cc+} = 4.75 V, V_{cc-} = −4.75 V, I_{OH} = −400 μA
V_{OL}	Low-level output voltage	13		0.25	0.4	V	V_{cc+} = 4.75 V, V_{cc-} = −4.75 V, I_{OL} = 16 mA
I_{IH}	High-level input current (strobe inputs)	14			40	μA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, V_{IH} = 2.4 V
					1	mA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, V_{IH} = 5.25 V
I_{IL}	Low-level input current (strobe inputs)	14		—1	—1.6	mA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, V_{IL} = 0.4 V
I_{OS}	Short-circuit output current	15	−2.1		−3.5	mA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V
I_{cc+}	Supply current from V_{cc+}	6		25	40	mA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, T_A = 25°C
I_{cc-}	Supply current from V_{cc-}	6		—15	− 18	mA	V_{cc+} = 5.25 V, V_{cc-} = −5.25 V, T_A = 25°C

** All typical values are at V_{cc+} = 5 V, V_{cc-} = −5 V, T_A = 25°C.

*Numbers in parenthesis apply to 5524 or 5525 as indicated

SWITCHING CHARACTERISTICS, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $C_{ext} \geqslant 100$ pF, $T_A = 25°C$

Propagation Delay Times			Test					
Symbol	From Input	To Output	Fig.	Min	Typ	Max	Unit	Test Conditons
$t_{PLH(D)}$	A1—A2	W	37		25	40	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(D)}$					20		ns	
$t_{PLH(S)}$	Strobe	W	37		15	30	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(S)}$					20		ns	

TYPICAL RECOVERY AND CYCLE TIMES, $V_{CC+} = 5$ V, $V_{CC-} = -5$V, $C_{ext} \geqslant 100$ pF, $T_A = 25°C$

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{orD}	Differential-input overload recovery time (see Note 5)		20		ns	Differential Input Pulse: $V_{ID} = 2$ V, $t_r = t_f = 20$ ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)		20		ns	Common-Mode Input Pulse: $V_{IC} = \pm 2$ V, $t_r = t_f = 20$ ns
$t_{cyc(min)}$	Minimum cycle time		200		ns	

NOTES:

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

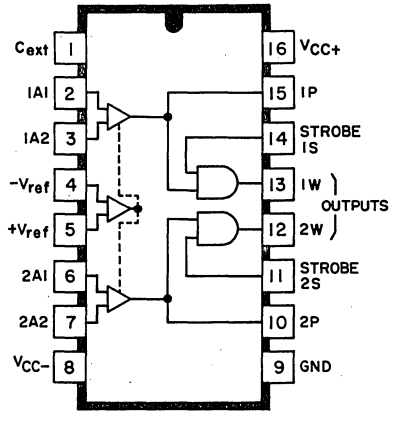
INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	X	L
X	L	L

Definition of Logic Levels

Input	H	L	X
A*	$V_{ID} \geqslant V_{T\ max}$	$V_{ID} \leqslant V_{T\ min}$	Irrelevant
S	$V_I \geqslant V_{IH\ min}$	$V_I \leqslant V_{IL\ max}$	Irrelevant

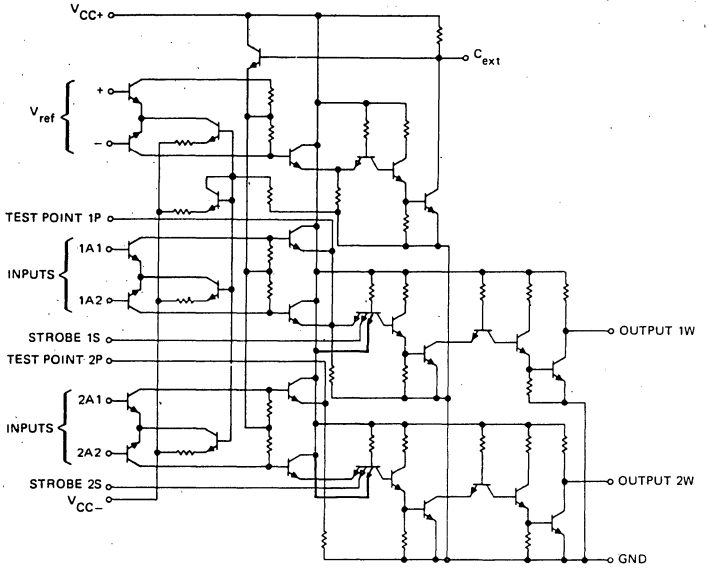
* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



POSITIVE LOGIC: W = AS

Schematic



ELECTRICAL CHARACTERISTICS (unless otherwise noted $V_{CC+}=5V$, $V_{CC-}=-5V$, $T_A=0°C$ to $70°C$)

	Parameter	Test Fig.	Min	Typ**	Max	Unit	Test Conditions
V_T	Differential-input threshold voltage (see Note 3, page 17)	20	(10)11	15	(20)19	mV	ITT7528 (5528)* $V_{ref}=15mV$
			8	15	22		ITT7529 / 5529
			(35)36	40	(45)44		ITT7528 (5528) $V_{ref}=40mV$
			33	40	47		ITT7529 / 5529
V_{ICF}	Common--mode input firing voltage (see Note 4, page 17)			±2.5		V	$V_{ref}=40mV$, $V_{I(S)}=V_{IH}$ Common-Mode Input Pulse: $t_r \leqslant 15ns$, $t_f \leqslant 15ns$, $t_w=50ns$
I_{IB}	Differential-input bias current	2		30	75 (100)	μA	$V_{CC+}=5.25V$, (5528/29) $V_{CC-}=-5.25V$, $V_{ID}=0$
I_{IO}	Differential-input offset current	2		3		μA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $V_{ID}=0$
V_{IH}	High-level input voltage (strobe inputs)	21	2			V	
V_{IL}	Low-level input voltage (strobe inputs)	21			0.8	V	
V_{OH}	High-level output voltage	21	2.4	4		V	$V_{CC+}=4.75V$, $V_{CC-}=-4.75V$, $I_{OH}=-400\mu A$
V_{OL}	Low-level output voltage	21		0.25	0.4	V	$V_{CC+}=4.75V$, $V_{CC-}=-4.75V$, $I_{OL}=16mA$
I_{IH}	High-level input current (strobe inputs)	22			40	μA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $V_{IH}=2.4V$
					1	mA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $V_{IH}=5.25V$
I_{IL}	Low-level input current (strobe inputs)	22		−1	−1.6	mA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $V_{IL}=0.4V$
I_{OS}	Short-circuit output current	23	-2.1		−3.5	mA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$,
I_{CC+}	Supply current from V_{CC+}	6		25	40	mA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $T_A=25°C$
I_{CC-}	Supply current from V_{CC-}	6		−15	−18	mA	$V_{CC+}=5.25V$, $V_{CC-}=-5.25V$, $T_A=25°C$

** All typical values are at $V_{CC+}=5$ V, $V_{CC-}=-5$ V, $T_A=25°C$

* Numbers in parenthesis apply to 5528 or 5529 as indicated.

SWITCHING CHARACTERISTICS, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25_e C$

Propagation Delay Times

Symbol	From Input	To Output	Test Fig.	Min	Typ	Max	Unit	Test Conditions
$t_{PLH(D)}$	A1—A2	W	39		25	40	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(D)}$					20		ns	
$t_{PLH(S)}$	Strobe	W	39		15	30	ns	$C_L = 15$ pF, $R_L = 288\ \Omega$
$t_{PHL(S)}$					20		ns	

TYPICAL RECOVERY AND CYCLE TIMES, $V_{CC-} = -5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$

	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{orD}	Differential-input overload recovery time (see Note 5)		20		ns	Differential Input Pulse: $V_{ID} = 2$ V, $t_f = 20$ ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)		20		ns	Common-Mode Input Pulse: $V_{IC} = \pm 2$ V, $t_r = t_f = 20$ ns
$t_{cyc(min)}$	Minimum cycle time		200		ns	

NOTES:

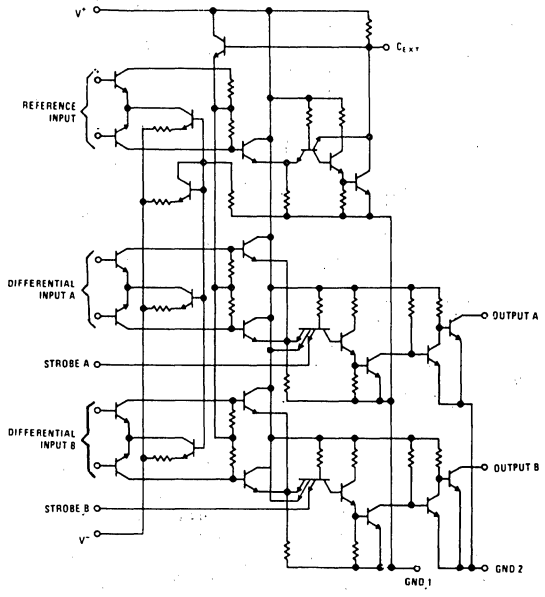
3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

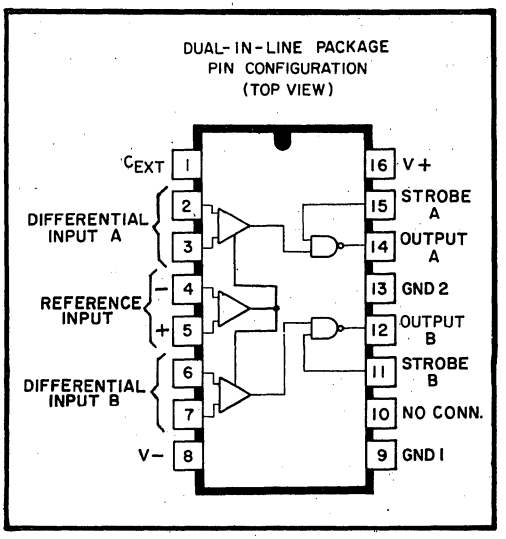
4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specifed common-mode input signal is applied with a strobe-enable present.

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

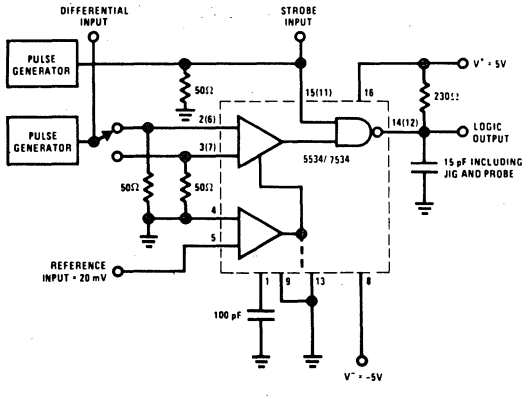
schematic diagram



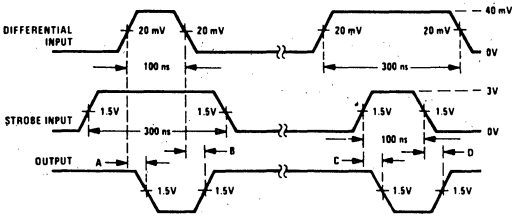


connection diagram

AC test circuit



Voltage Waveforms



1. Pulse generators have the following characteristics
   $Z_{out}=500\Omega$ $t_r=t_f=15(.5)$ ns, PRR=1 MHz

2. Propagation delays
   A=Differential input to logical "0" output
   B=Differential input to logical "1" output
   C=Strobe input to logical "0" output
   D=Strobe input to logical "1" output

ELECTRICAL CHARACTERISTICS

ITT5534/ITT5535: The following apply for $-55°C \leqslant T_A \leqslant 125°C$, $V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$ $-5V \pm 5\%$ (Note 1)

Parameter	Min	Typ	Max	Unit	Test Conditions (Each Amplifier) Diff. Input	Ref. Input	Strobe Input	Logic Output	Supply Volt	Comments
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15mV	+5V	+5.25V	$\pm 5V \pm 5\%$	Logic Output $<250\mu A$
		15	20(22)	mV	$\pm V_{TH}$	15mV	+5V	+20mA	$\pm 5V \pm 5\%$	Logic Output $<0.4V$
	35(33)	40		mV	$\pm V_{TH}$	40mV	+5V	+5.25V	$\pm 5V \pm 5\%$	Logic Output $<250\mu A$
		40	45(47)	mV	$\pm V_{TH}$	40mV	+5V	+20mA	$\pm 5V \pm 5\%$	Logic Output $<0.4V$
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5.25V		$\pm 5.25V$	

ITT7534(ITT7535):* The following apply for $0°C \leqslant T_A \leqslant 70°C$, $V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$

Parameter	Min	Typ	Max	Unit	Test Conditions (Each Amplifier) Diff. Input	Ref. Input	Strobe Input	Logic Output	Supply Volt	Comments
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15mV	+5V	+5.25V	$\pm 5V \pm 5\%$	Logic Output $<250\mu A$
		15	19(22)	mV	$\pm V_{TH}$	15mV	+5V	+20mA	$\pm 5V \pm 5\%$	Logic Output $<0.4V$
	36(33)	40		mV	$\pm V_{TH}$	40mV	+5V	+5.25V	$\pm 5V \pm 5\%$	Logic Output $<250\mu A$
		40	44(47)	mV	$\pm V_{TH}$	40mV	+5V	+20mA	$\pm 5V \pm 5\%$	Logic Output $<0.4V$
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5.25V		$\pm 5.25V$	

* Numbers in parenthesis apply to 5535 or 7535 as indicated.

ITT5534/ITT5535: The following apply for $-55°C \leqslant T_A \leqslant 125°C$, $V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$
ITT7534/ITT7535: The following apply for $0°C \leqslant T_A \leqslant 70°C$, $V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$

Parameter	Min	Typ	Max	Unit	Test Conditions (Each Amplifier)					
					Diff. Input	Ref. Input	Strobe Input	Logic Output	Supply Volt	Comments
Diff. Input Offset Current		3		μA	0V	0V	+5.25V		±5.25V	
Logic "0" Input Voltage			0.8	V	40mV	20mV	+0.8V	+5.25V	±4.75V	Logic Output <250μA
Logic "1" Input Voltage	2.0			V	40mV	20mV	+2.0V	+20mA	±4.75V	Logic Output <0.4V
Logic "0" Input Current		—1	−1.6	mA	40mV	20mV	+0.4V		±5.25V	
Logic "1" Input Current		5	40	μA	0V	20mV	+2.4V		±5.25V	
		0.02	1	mA	0V	20mV	+5.25V		±5.25V	
Logic "0" Output Voltage		0.25	0.40	V	40mV	20mV	+2V	+20mA	±4.75V	
Output Leakage Current		0.01	250	μA	40mV	20mV	+0.8V	+5.25V	±4.75V	
V+ Supply Current		28	38	mA	0V	20mV	0V		±5.25V	
V− Supply Current		13	—18	mA	0V	20mV	0V		±5.25V	

ITT5534/ITT5535 and ITT7534/ITT7535: The following apply for $T_A = 25°C$, $V+ = 5V$, $V- = -5V$

Parameter	Min	Typ	Max	Unit	Test Conditions (Each Amplifier)					
					Diff. Input	Ref. Input	Strobe Input	Logic Output	Supply Volt	Comments
AC Common-Mode Input Firing Voltage		±2.5		V	Pulse	20mV	+5V	Scope		
Propagation Delays:										
Differential Input to Logical "1" Output		24		ns		20mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20mV				AC Test Circuit

ITT5534/ITT5535 and ITT7534/ITT7535: The following apply for $T_A = 25°C$, $V+ = 5V$, $V- = -5V$

Parameter	Min	Typ	Max	Unit	Test Conditions (Each Amplifier)					
					Diff. Input	Ref. Input	Strobe Input	Logic Output	Supply Volt	Comments
Strobe Input to Logical "0" Output		10	30	ns		20mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time	5			ns						
Min. Cycle Time	200			ns						

Note 1—For $0°C \leqslant T_A \leqslant 70°C$ operation, electrical characteristics for ITT5534 and ITT5535 are guaranteed the same as ITT7534 and ITT7535 respectively.

Note 2—Limits in parentheses pertain to ITT-5535, other limits pertain to ITT5534.

Note 3—Limits in parentheses pertain to ITT-7535, other limits pertain to ITT5534.

Note 4—Positive current is defined as current into the referenced pin.

Note 5—Pin 1 to have $\geqslant$ 100 pF capacitor connected to ground.

DUAL SENSE AMPLIFIERS

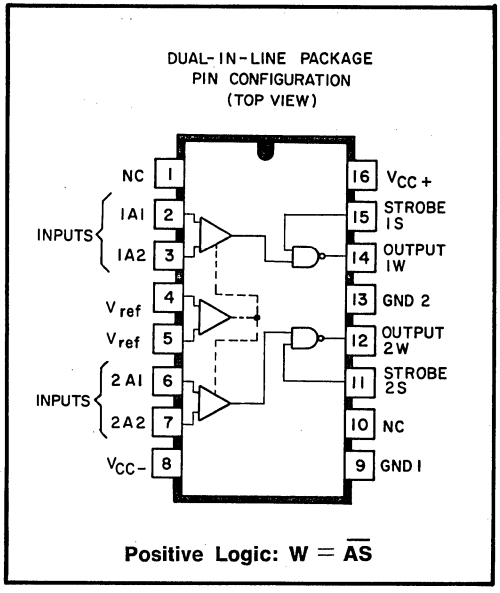
TRUTH TABLE

Inputs A	Inputs S	Output W
H	H	L
L	X	H
X	L	H

Definition of Logic Levels

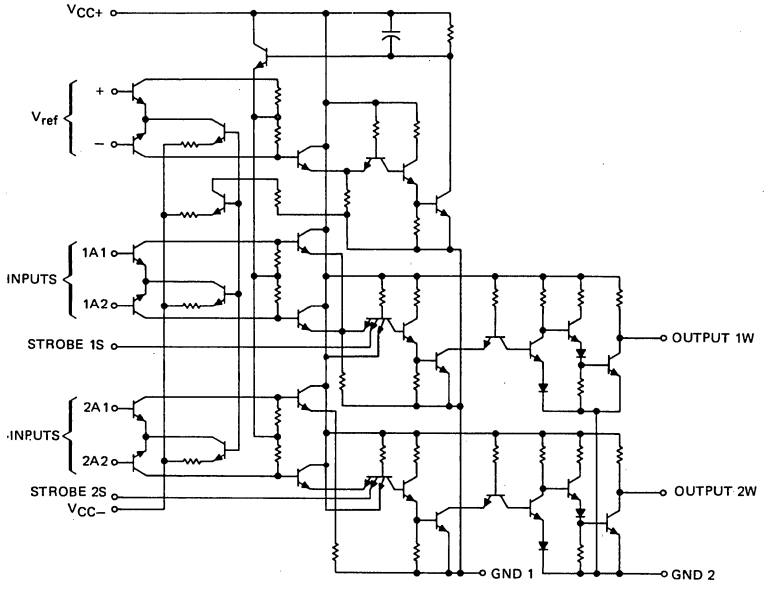
Input	H	L	X
A*	$V_{ID} \geqslant V_T$max	$V_{ID} \leqslant V_T$min	Irrelevant
S	$V_I \geqslant V_{IH}$min	$V_I \leqslant V_{IL}$max	Irrelevant

*A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.



NC—No internal connection

Schematic



ELECTRICAL CHARACTERISTICS (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$V, $T_A = 0°C$ to $70°C$)

	Parameter	Test Fig.	Min	Typ**	Max	Unit	Test Conditions
V_T	Differential-input threshold voltage (see Note 3, page 17)	24	(10)11	15	(20)19	mV	V_{ref}=15mV ITT75234(55234)*
			8	15	22	mV	ITT75235/55235
			(35)36	40	(45)44	mV	V_{ref}=40mV ITT75234(55234)
			33	40	47	mV	ITT75235/55235
I_{ICF}	Common-mode input firing voltage (see Note 4, page 17)			±2.5		V	V_{ref} = 40 mV $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, $t_w \leqslant 50$ ns
I_{IB}	Differential-input bias current	2		30	75 (100)	μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V,(55234/35) $V_{ID} = 0$
I_{IO}	Differential-input offset current	2		3		μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$
V_{IH}	High-level input voltage (strobe inputs)	25	2			V	
V_{IL}	Low-level input voltage (strobe inputs)	25			0.8	V	
V_{OH}	High-level output voltage	25	2.4	4		V	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA
V_{OL}	Low-level output voltage	25		0.25	0.4	V	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA
I_{IH}	High-level input current (strobe inputs)	26			40	μA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V
					1	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V
I_{IL}	Low-level input current (strobe inputs)	26		—1	—1.6	mA	$V_{CC-} = -5.25$ V, $V_{CC+} = 5.25$ V, $V_{IL} = 0.4$ V
I_{OS}	Short-circuit output current	27	−2.1		—3.5	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V,
I_{CC+}	Supply current from V_{CC+}	6		25	40	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$
I_{CC-}	Supply current from V_{CC-}	6		−15	—18	mA	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$

** All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

* Numbers in parenthesis apply to 55234 or 55235 as indicated.

SWITCHING CHARACTERISTICS, V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C

Symbol	From Input	To Output	Test Fig.	Min	Typ	Max	Unit	Test Conditions
$t_{PLH(D)}$	A1-A2	W	40			25	ns	C_L = 15pF, R_L = 288 Ω
$t_{PHL(D)}$					25	40	ns	
$t_{PLH(S)}$	STROBE	W	40		25		ns	C_L = 15pF, R_L = 288 Ω
$t_{PHL(S)}$					15	30	ns	

TYPICAL RECOVERY AND CYCLE TIMES, V_{CC+} = 5V, V_{CC-} = 5V, T_A = 25°C

	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{OR}D$	Differential-input overload recovery time (see Note 5)		20		ns	Differential Input Pulse: V_{ID} = 2 V, $t_r = t_f$ = 20 ns
$t_{OR}C$	Common-mode-input overload recovery time (see Note 6)		20		ns	Common-Mode Input Pulse: V_{IC} = ±2 V,
$t_{cyc(min)}$	Minimum cycle time		200		ns	$t_r = t_f$ = 20 ns

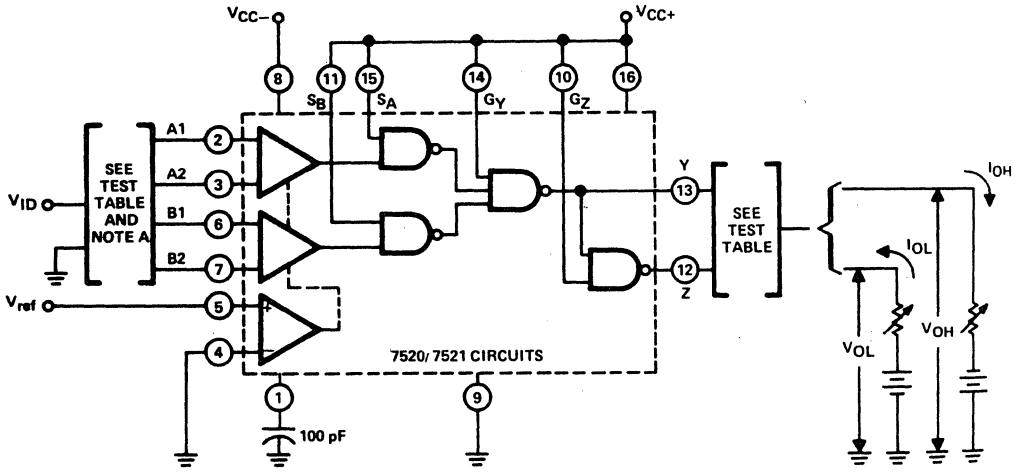
NOTES:

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

SENSE AMPLIFIERS

PARAMETER MEASUREMENT INFORMATION
d-c test circuits*



TEST TABLE

CIRCUIT TYPE	INPUTS V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
			V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
ITT7520	A1-A2 or B1-B2 15 mV	⩽11 mV	⩽0.4 V		16 mA	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2 15 mV	⩾19 mV	⩾2.4 V	−400 μA		⩽0.4 V		16 mA
	A1-A2 or B1-B2 40 mV	⩽36 mV	⩽0.4 V		16 mA	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2 40 mV	⩾44 mV	⩾2.4 V	−400 μA		⩽0.4 V		16 mA
ITT7521	A1-A2 or B1-B2 15 mV	⩽ 8 mV	⩽0.4 V		16 mA	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2 15 mV	⩾22 mV	⩾2.4 V	−400 μA		⩽0.4 V		16 mA
	A1-A2 or B1-B2 40 mV	⩽33 mV	⩽0.4 V		16 mA	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2 40 mV	⩾47 mV	⩾2.4 V	−400 μA		⩽0.4 V		16 mA

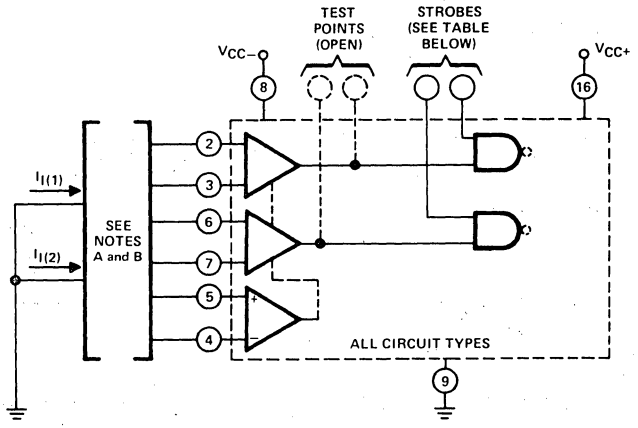
NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1—V_T

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits* (continued)



NOTES:

A. Each preamplifier is tested separately. Inputs not under test are grounded.

B. $I_{IB} = I_{I(1)}$ and/or $I_{I(2)}$, $I_{IO} = I_{I(1)} - I_{I(2)}$, are the currents into the two inputs of the pair under test.

Pin Connections (Other Than Those Shown Above)

Circuit Types	100 pF to GND	Apply V_{CC+}	Apply GND	Leave Open	Other
ITT7520, ITT7521	C_{ext} (1)	G_Y,G_Z,S_A,S_B (14) (10) (15) (11)		Y, Z (13) (12)	
ITT7522, ITT7523	C_{ext} (1)	G, S_A, S_B (14) (15) (11)	GND 2 (13)		R_L, Y (10) (12)
ITT7524, ITT7525	C_{ext} (1)	1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	
ITT7528, ITT7529	C_{ext} (1)	1S, 2S (14) (11)		1P, 2P, 1W, 2W (15) (10) (13) (12)	
ITT75234, ITT75235		1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	

Figure 2—I_{IB}, I_{IO}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

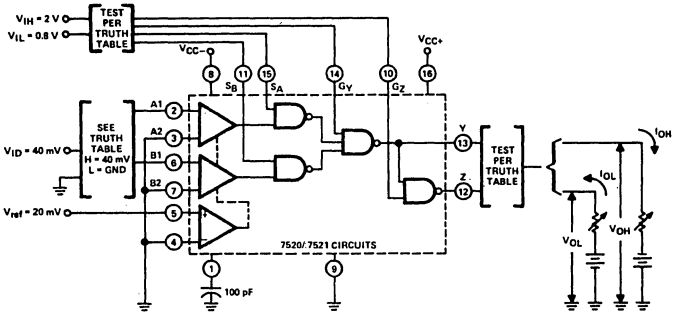
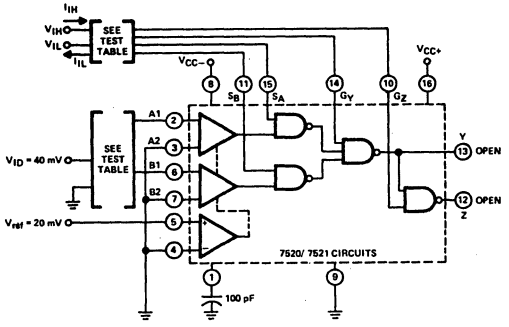


FIGURE 3—V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

Test	Input A1	Input B1	Strobe S_A	Strobe S_B	Gate G_Y	Gate G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4—I_{IH}, I_{IL}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

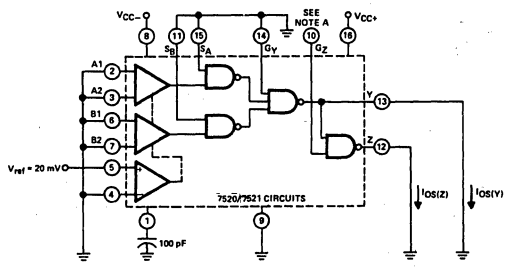
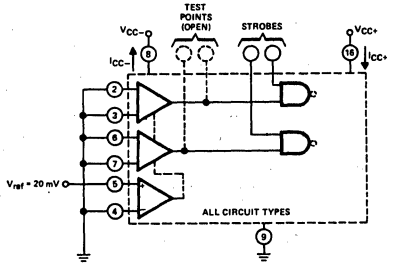


FIGURE 5—I_{OS}

NOTE A:
When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



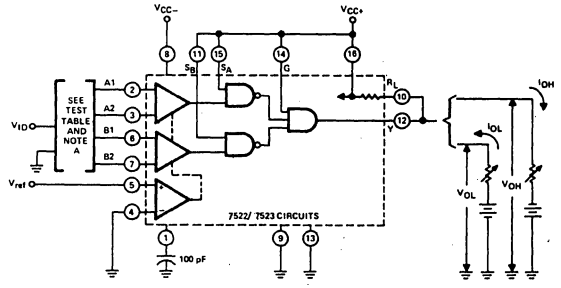
Pin Connections (Other Than Those Shown Above)

Circuit Types	100 pF to GND	Apply GND	Leave Open
ITT7520, ITT7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)	Y, Z (13) (12)
ITT7522, ITT7523	C_{ext} (1)	G, S_A, S_B, GND 2 (14) (15) (11) (13)	R_L, Y (10) (12)
ITT7524, ITT7525	C_{ext} (1)	1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
ITT7528, ITT7529	C_{ext} (1)	1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)
ITT75234, ITT75235		IS, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)

Figure 6—I_{CC+}, I_{CC-}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)



TEST TABLE

Circuit Type	Inputs	V_{ref}	V_{ID}	Output		
				V_O	I_{OH}	I_{OL}
ITT7522	A1-A2 or B1-B2	15 mV	⩽11mV	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	⩾19 mV	⩽0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	⩽36 mV	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	⩾44 mV	⩽0.4 V		16 mA
ITT7523	A1-A2 or B1-B2	15 mV	⩽ 8 mV	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	⩾22 mV	⩽0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	⩽33 mV	⩾2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	⩾47 mV	⩽0.4 V		16 mA

NOTE A:
Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7—V_T

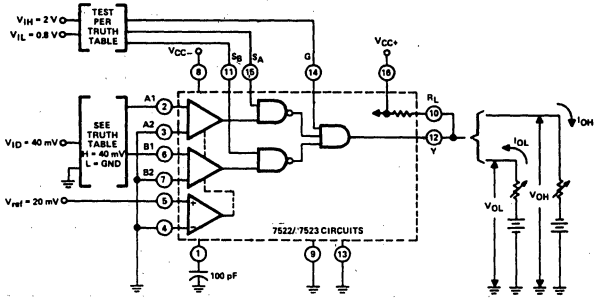
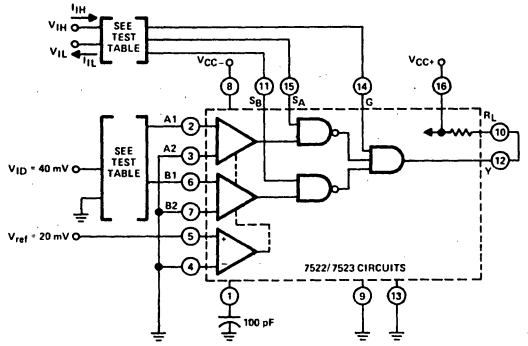


FIGURE 8—V_{IH}, V_{IL}, V_{OH}, V_{OL}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)



TEST TABLE

Test	Input A_1	Input B_1	Strobe S_A	Strobe S_B	Gate G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9—I_{IH}, I_{IL}

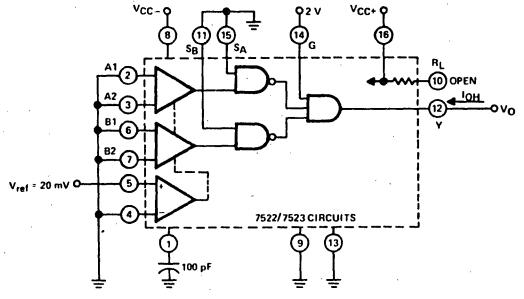


FIGURE 10—I_{OH}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c Test Circuits*

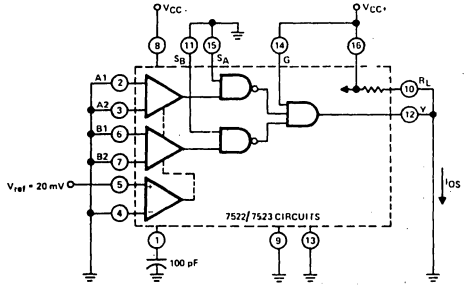
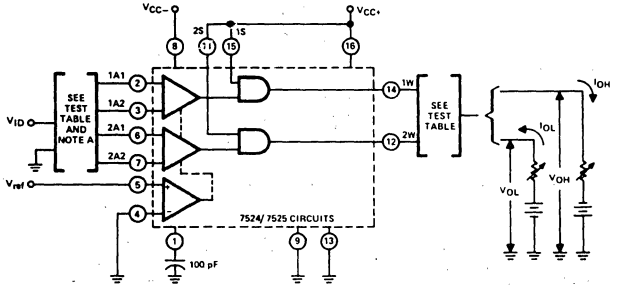


FIGURE 11—I_{OS}



TEST TABLE

Circuit Type	Inputs	V_{ref}	V_{ID}	Output		
				V_O	I_{OH}	I_{OL}
ITT7524	A1-A2	15 mV	⩽11mV	⩽0.4 V		16 mV
	A1-A2	15 mV	⩾19 mV	⩾2.4 V	—400 μA	
	A1-A2	40 mV	⩽36 mV	⩽0.4 V		16 mV
	A1-A2	40 mV	⩾44 mV	⩾2.4 V	—400 μA	
ITT7525	A1-A2	15 mV	⩽ 8 mV	⩽0.4 V		16 mV
	A1-A2	15 mV	⩾22 mV	⩾2.4 V	—400 μA	
	A1-A2	40 mV	⩽33 mV	⩽0.4 V		16 mV
	A1-A2	40 mV	⩾47 mV	⩾2.4 V	—400 μA	

NOTE A:
Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12—V_T

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits*

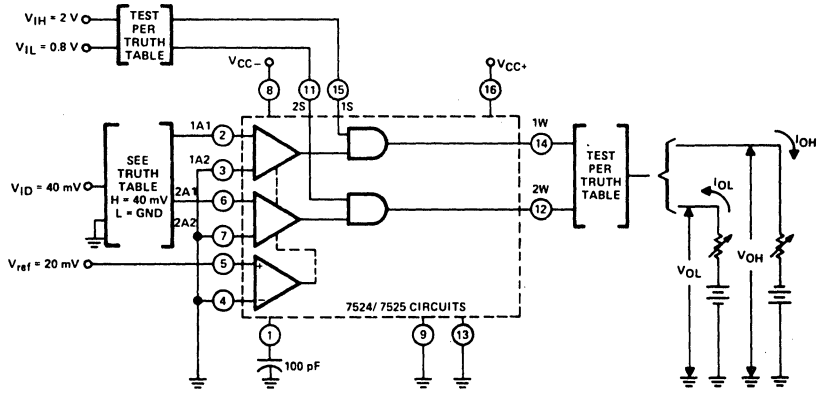
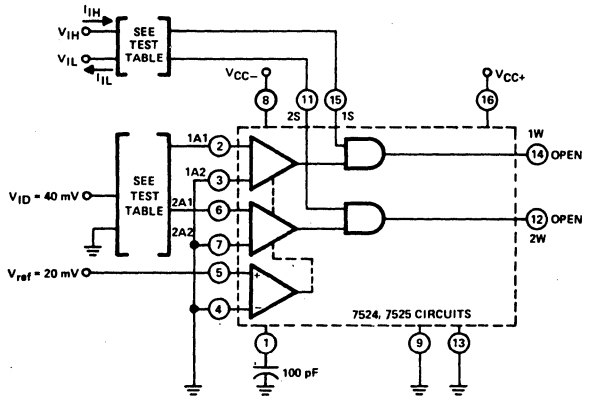


FIGURE 13—V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

Test	Input 1A1	Input 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14—I_{IH}, I_{IL}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

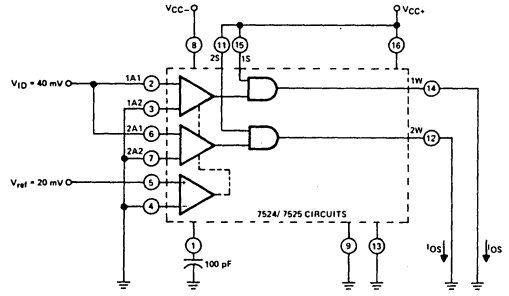
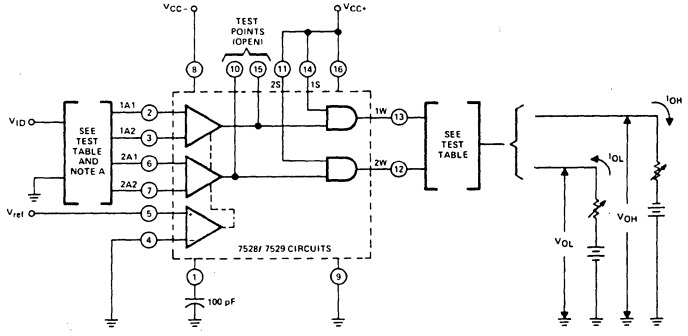


FIGURE 15—I_{OS}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.



TEST TABLE

Circuit Type	Inputs	V_{ref}	V_{ID}	Output		
				V_O	I_{OH}	I_{OL}
ITT7528	A1-A2	15 mV	⩽11 mV	⩽0.4 V		16 mA
	A1-A2	15 mV	⩾19 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩽36 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩾44 mV	⩾2.4 V	−400 μA	
ITT7529	A1-A2	15 mV	⩽8 mV	⩽0.4 V		16 mA
	A1-A2	15 mV	⩾22 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩽33 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩾47 mV	⩾2.4 V	−400 μA	

NOTE A:
Each pair of inputs is tested separately with its corresponding output.

FIGURE 16—V_T

PARAMETER MEASUREMENT INFORMATION

d-c test circuits* (continued)

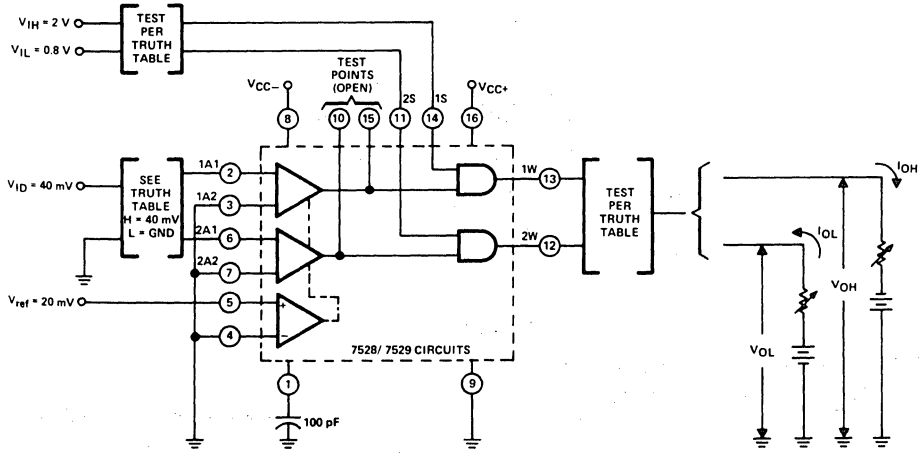
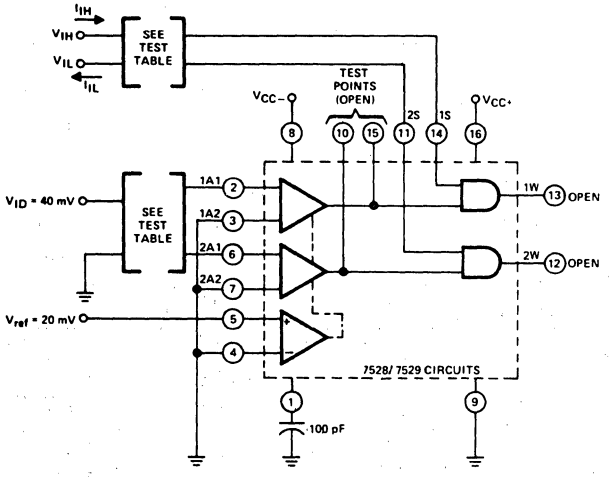


FIGURE 17—V_{IH}, V_{IL}, V_{OH}, V_{OL}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.



TEST TABLE

Test	Input 1A1	Input 2A1	Strobe 1S	Strobe 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 18—I_{IH}, I_{IL}

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

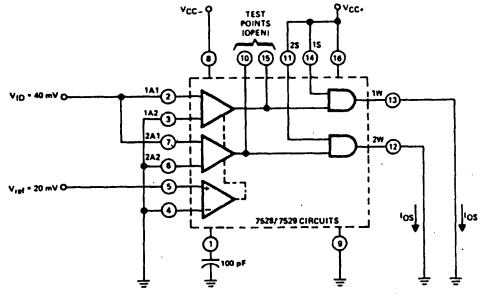
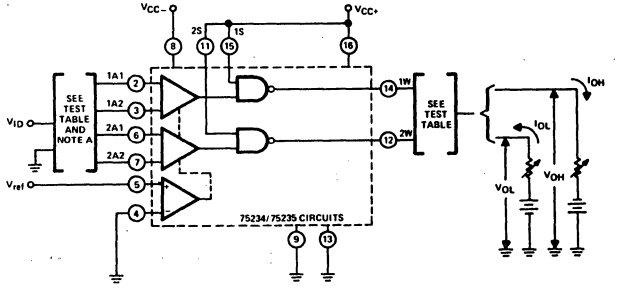


FIGURE 19—I_{OS}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.



TEST TABLE

Circuit Type	Inputs	V_{ref}	V_{ID}	Output		
				V_O	I_{OH}	I_{OL}
ITT75234	A1-A2	15 mV	⩽11 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾19 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽36 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾44 mV	⩽0.4 V		16 mA
ITT75235	A1-A2	15 mV	⩽ 8 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾22 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽33 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾47 mV	⩽0.4 V		16 mA

NOTE A:
Each pair of differential inputs is tested separately with its correspondng output.

Figure 20—V_T

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

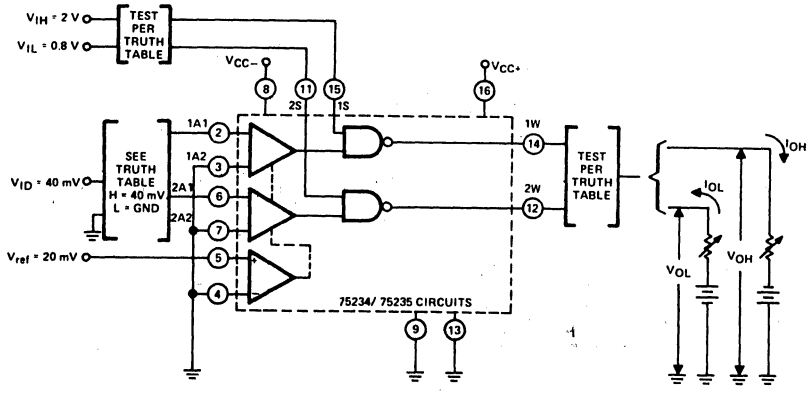
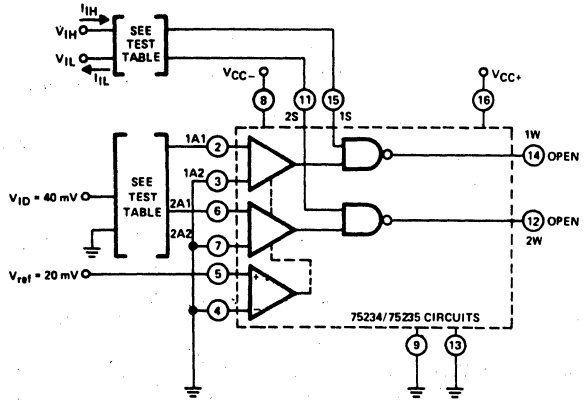


Figure 21—V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

Test	Input 1A1	Input 2A1	Strobe 1S	Strobe 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Figure 22—I_{IH}, I_{IL}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive-value.

PARAMETER MEASUREMENT INFORMATION
d-c test circuits* (continued)

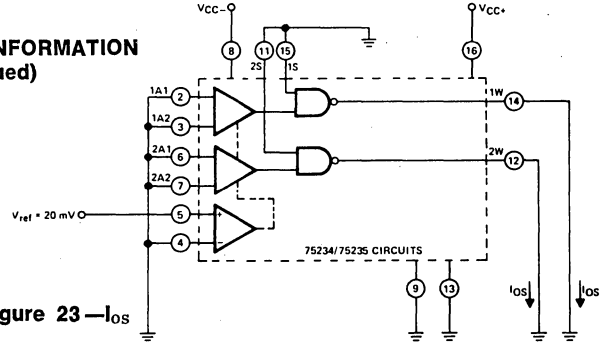
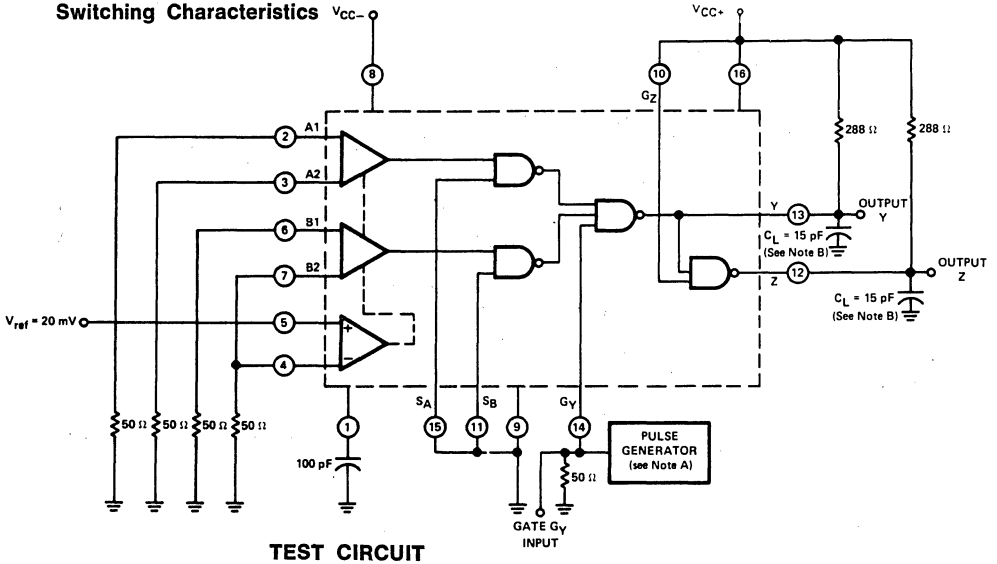


Figure 23—I_{OS}

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics



TEST CIRCUIT

VOLTAGE WAVEFORMS

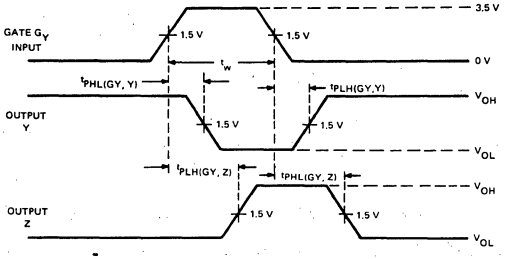


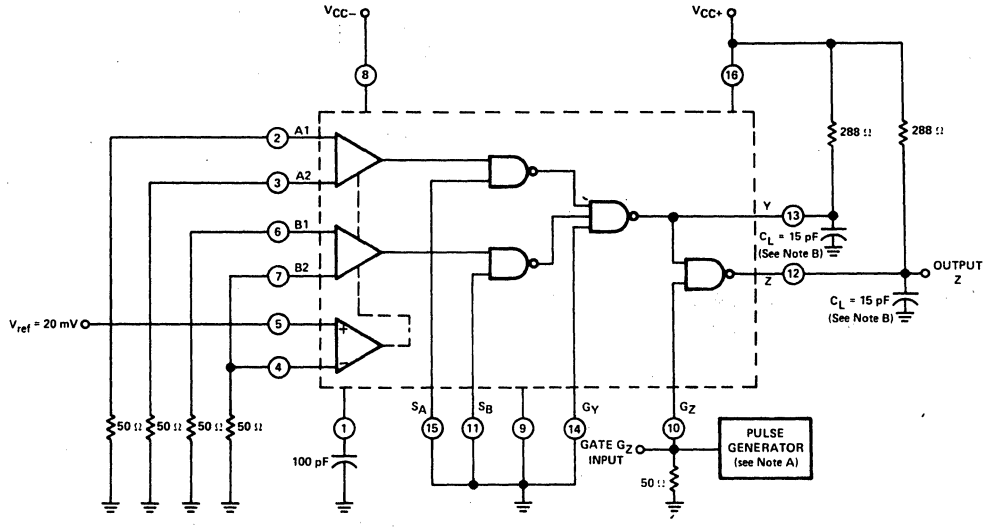
Figure 24—ITT7520/ITT7521 Propagation Delay Times From Gate G_Y

NOTES:

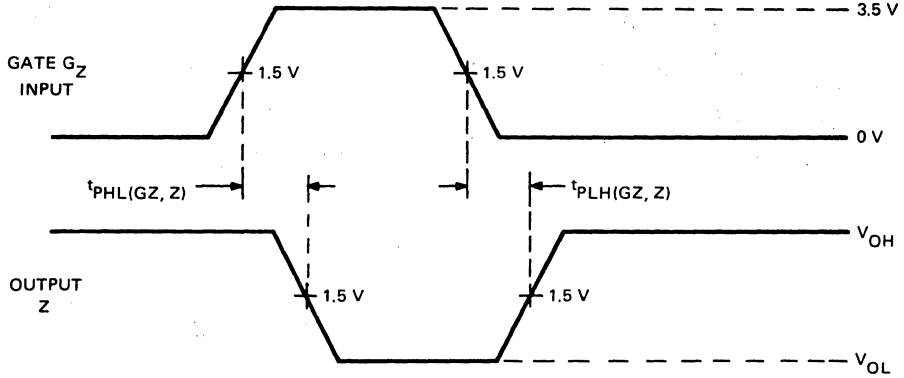
A. The pulse generator has the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15 \pm 5$ns, tw = 100 ns, and PRR = 1 MHz.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



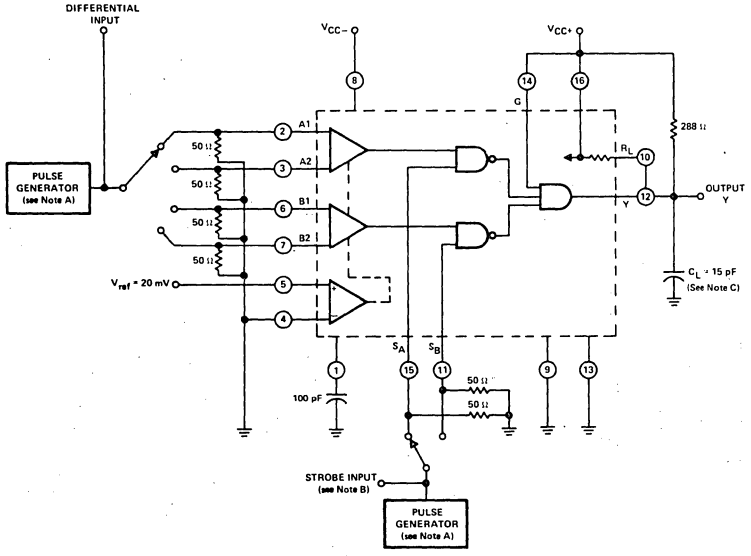
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15 \pm 5$ns, tw = 100 ns, and PRR = 1 MHz.

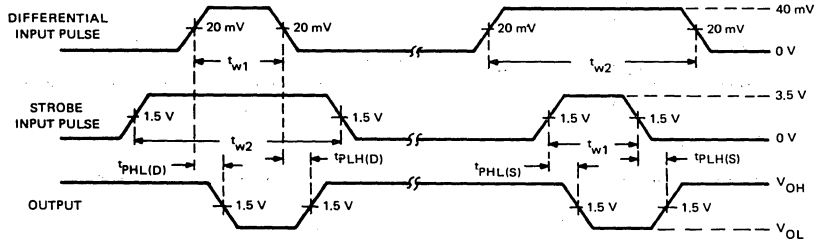
B. C_L includes probe and jig capacitance.

Figure 25—ITT7520/ITT7521 Propagation Delay Times From Gate G_Z

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

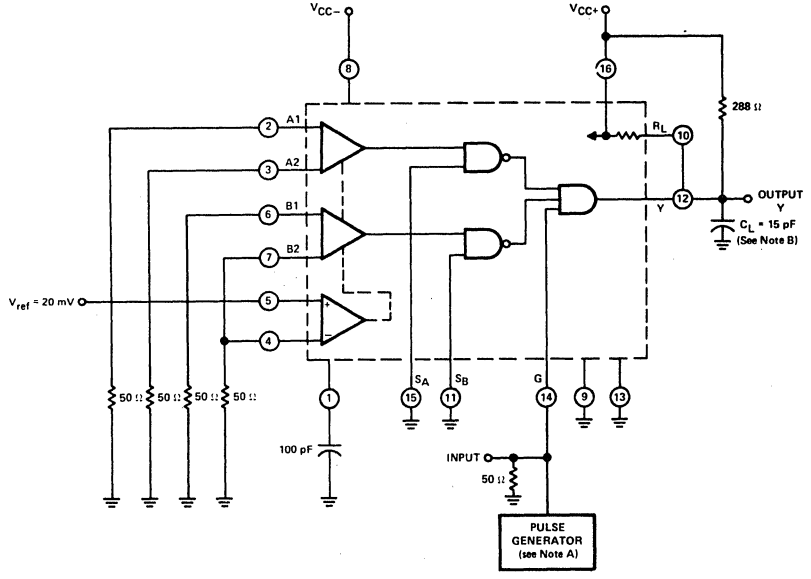
A. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15 \pm 5$ns, $t_{w1} = 100$ns, $t_{w2} = 300$ ns, PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.

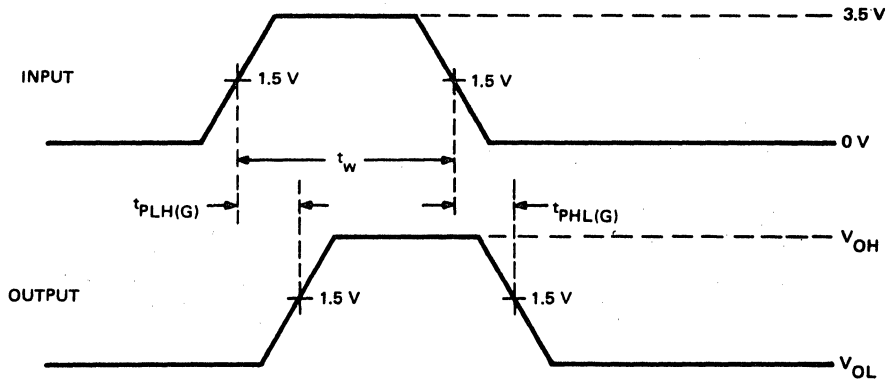
C. C_L includes probe jig capacitance.

Figure 26—ITT7522/ITT7523 Propagation Delay Times From Differential and Strobe Inputs

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



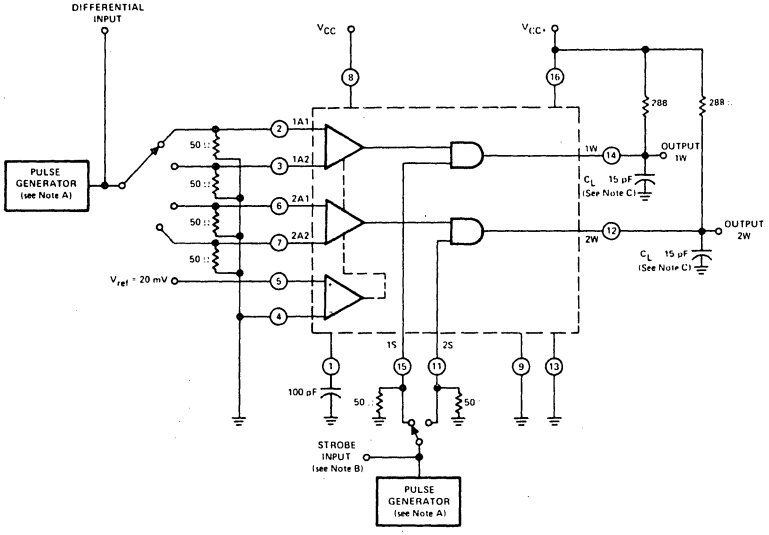
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, $t_{p1} = 100$ ns, $t_{p2} = 300$ ns, $t_{p3} = 0.8\ \mu$s, PRR = 1 MHz.

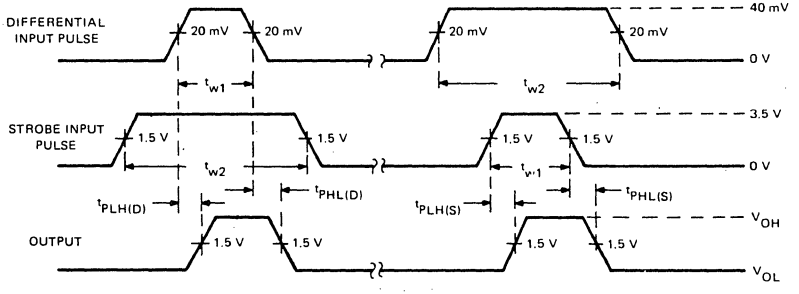
B. C_L includes probe and jig capacitance.

Figure 27—ITT7522/ITT7523 Propagation Delay Times From Gate Input

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

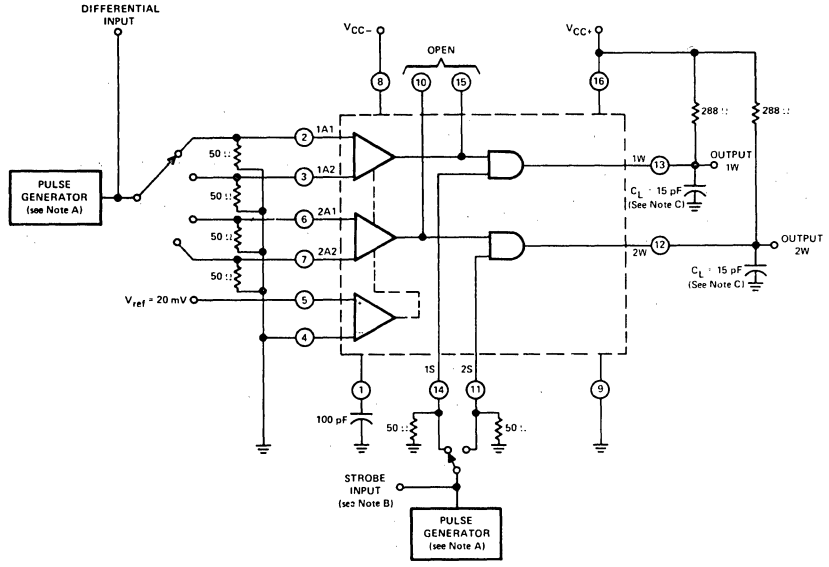
A. The pulse generators have the following characteristics:
Z_{out} = 50 Ω, t_r = t_f = 15 ± 5 ns,
t_{w1} = 100ns, t_{w2} = 300 ns, PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when input 2A1-2A2 are being tested.

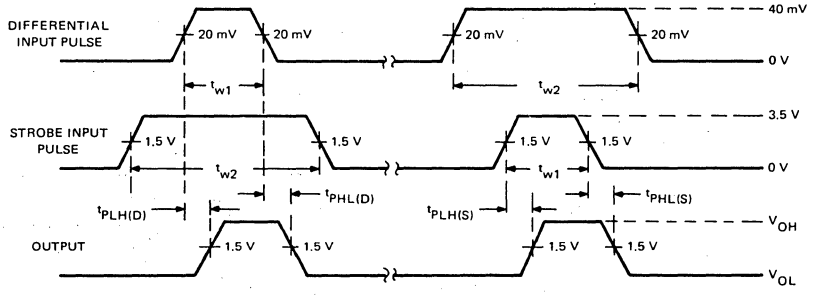
C. C_L includes probe and jig capacitance.

Figure 28—ITT7524/ITT7525 Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

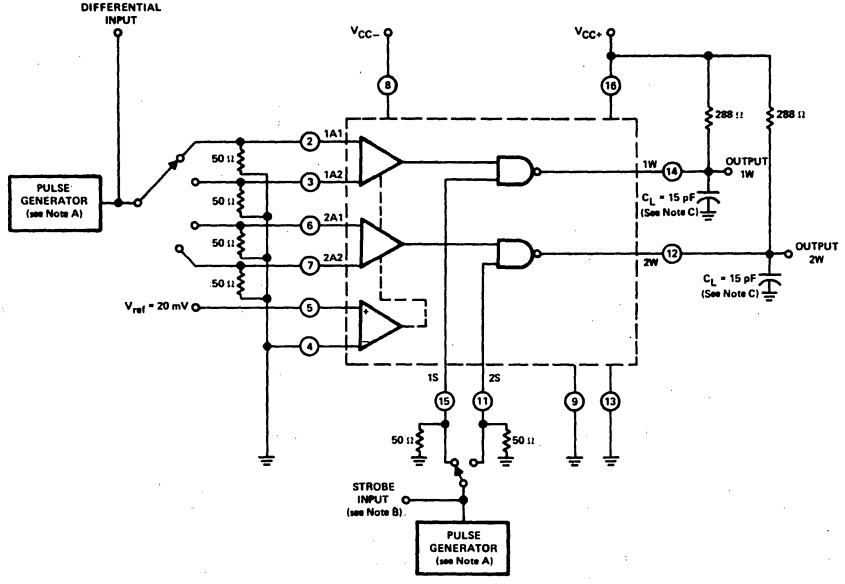
A. The pulse generators have the following characteristics:
$Z_{out} = 50\Omega$, $t_r = t_f = 15 \pm 5$ns, $t_{w1} = 100$ns, $t_{w2} = 300$ ns, and PRR = 1 MHz.

B. The strobe pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

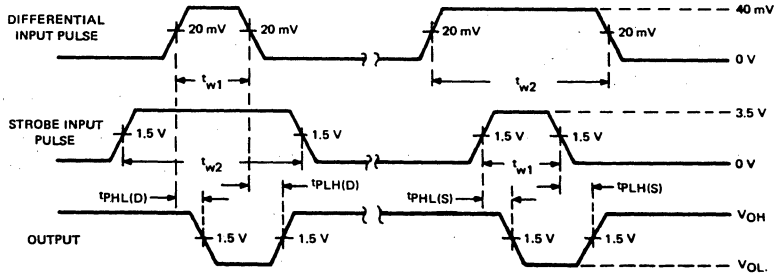
C. C_L includes probe and jig capacitance.

Figure 29—ITT7528/7529 Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION
Switching Characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES

A. The pulse generators have the following characteristics:
Z_{out} = 50Ω, t_r = t_f = 15 ± 5ns, t_{w1} = 100ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when input 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

Figure 30—ITT75234/ITT75235 Propagation Delay Times

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
RFERENCE VOLTAGE

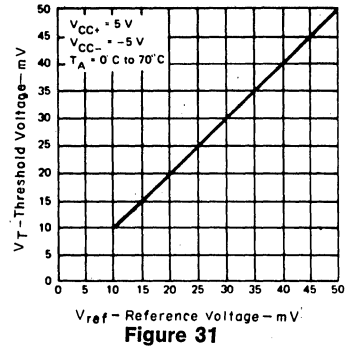


Figure 31

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

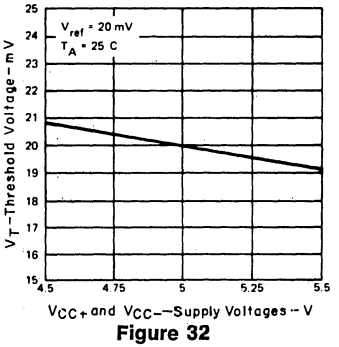


Figure 32

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

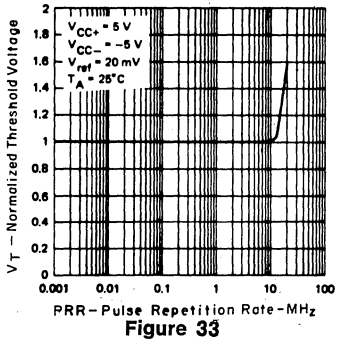


Figure 33

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

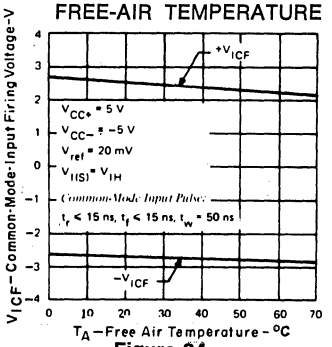


Figure 34

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

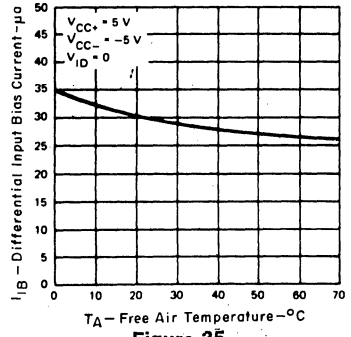


Figure 35

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

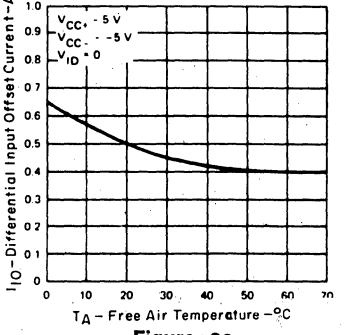


Figure 36

TYPICAL CHARACTERISTICS

HIGH-LEVEL INPUT CURRENT
VS
INPUT VOLTAGE

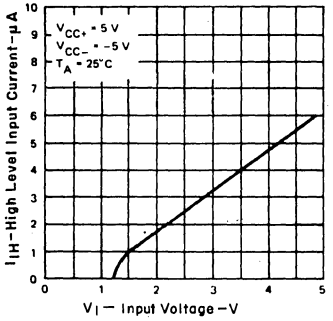


Figure 37

LOW-LEVEL INPUT CURRENT
VS
INPUT VOLTAGE

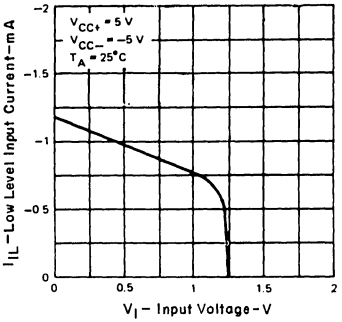


Figure 38

OUTPUT VOLTAGE
VS
DIFFERENTIAL-INPUT VOLTAGE

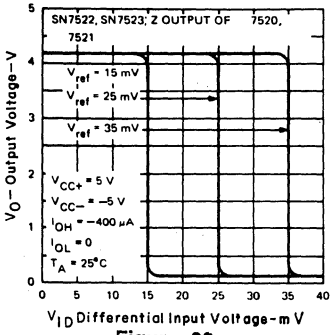


Figure 39

OUTPUT VOLTAGE
VS
DIFFERENTIAL-INPUT VOLTAGE

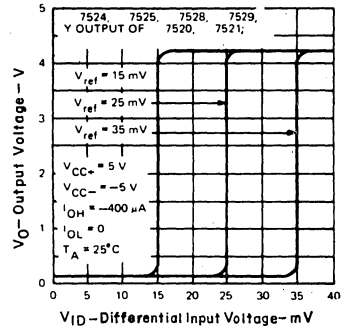


Figure 40

HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

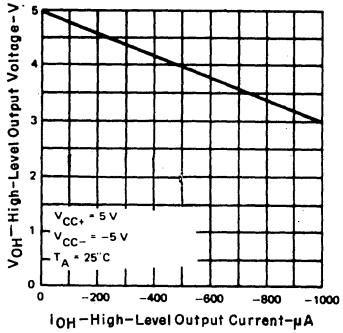


Figure 41

LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT

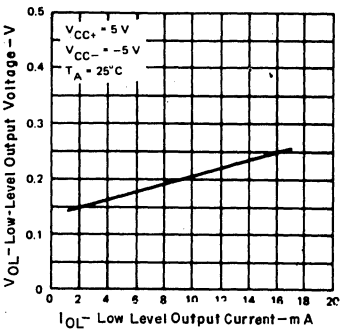


Figure 42

TYPICAL APPLICATIONS

Small Memory Systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel ITT7524 or ITT7525 sense amplifiers, see Figure K. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

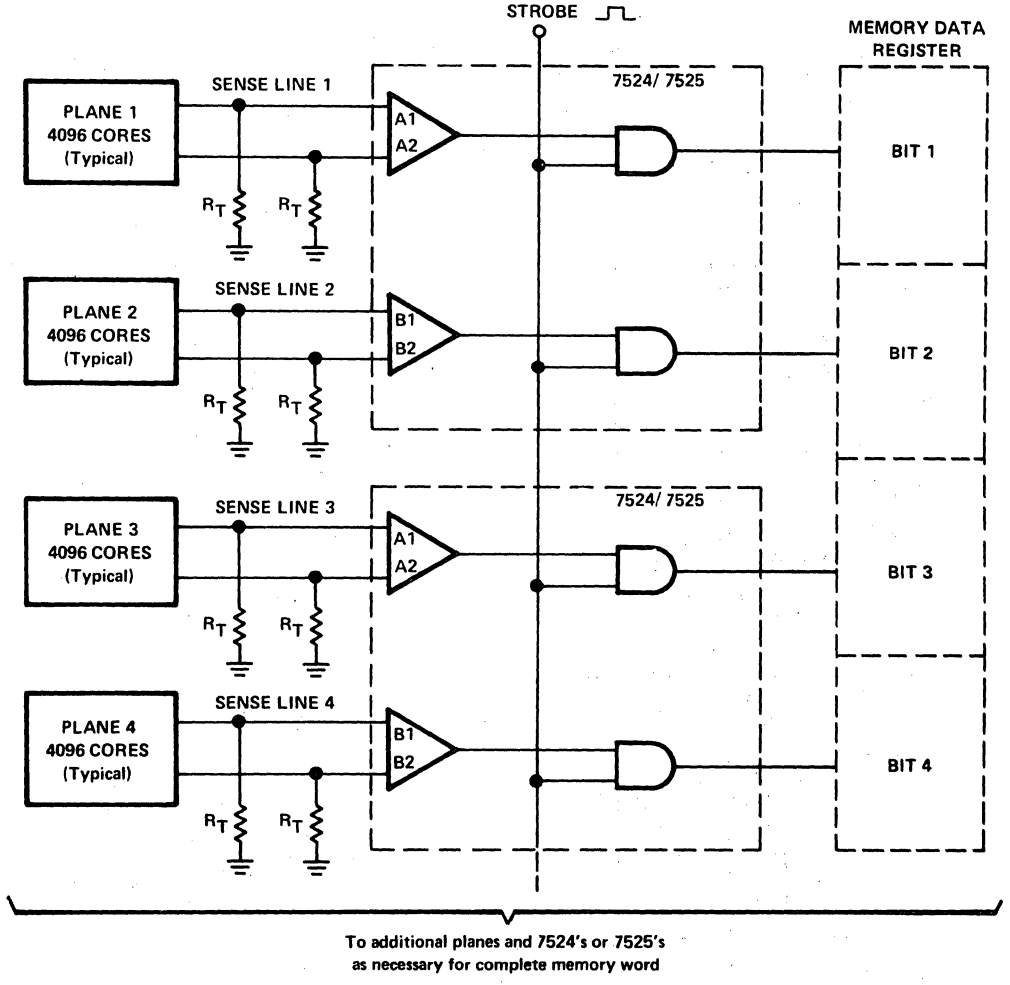


Figure K—Sensing Small Memory Systems

Large Memory Systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure L. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of ITT7420/ITT7421 or ITT7422/ITT7423 sense amplifiers. The cascaded output gates of ITT-7520/ITT7521 circuits may be connected to serve as the memory data register (MDR). A number of ITT7522/ITT7523 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

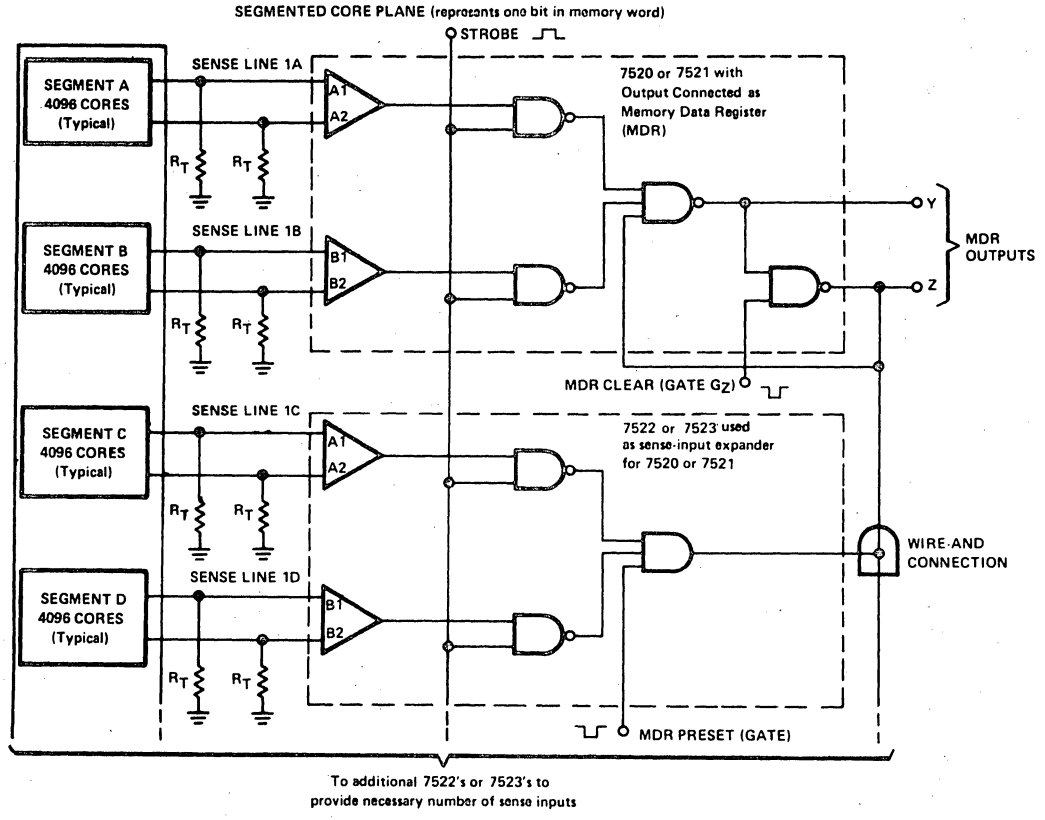


Figure L—Sensing Large Memory Systems

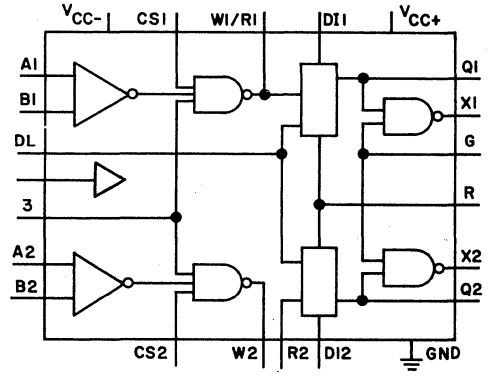
HIGH-SPEED DUAL SENSE AMPLIFIER

High-speed dual sense amplifier with built-in data register and data buffer for application in coincident-current core memories.

The ITT3671 is a dual sense amplifier with a built-in data register and data buffer. It is designed for use in high speed core memory systems. It detects bi-polar differential-input signals from the memory and provides the complete interface between the memory and logic section.

The ITT3671 sense amplifier is completely dc coupled, and utilizes a "matched-amplifier" technique. The reference amplifier circuit is inherently stable and requires no external or internal frequency compensation.

Functional Diagram

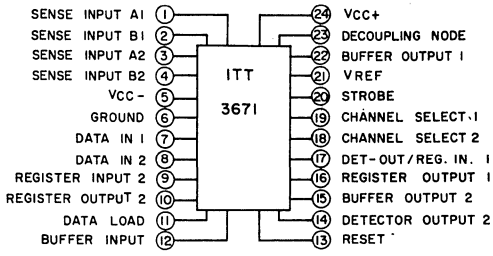


Features

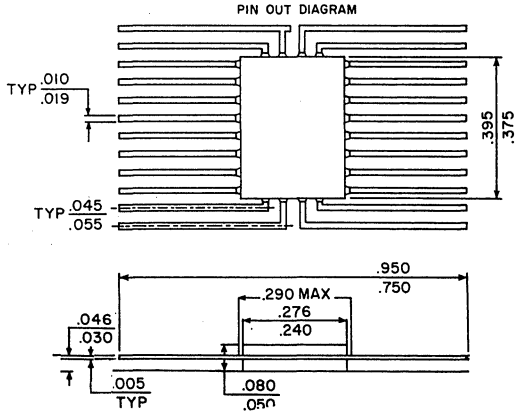
- ±2 mv threshold sensitivity
- Threshold voltage independent of temperature and supply voltage variations
- Reference amplifier inherently stable
- Built-in data register with provisions for external data inputs
- Built-in data buffer
- Low power consumption
- Internal reference voltage attenuator
- Two independent channels
- TTL compatible logic inputs and outputs

Customer Benefits

- System performance
- No external frequency compensation required
- Package count, space, cost reduction, increased reliability
- Drive 450 pf load in 15 ns
- Reduced system power
- Reference amplifier less sensitive to noise
- Ease of design



PIN OUT DIAGRAM



TRUTH TABLE

Diff.	Logic Inputs							Output	
Input	S	CSI	DI	DL	G	R	Reg. In	O	X
X	L	L	L	L	L	ML	·	L	H
X	L	L	L	L	H	ML	·	L	H
X	L	L	L	H	L	X	·	H	H
X	L	L	L	H	H	X	·	H	L
X	L	L	H	L	L	ML	·	L	H
X	L	L	H	L	H	ML	·	L	H
X	L	L	H	H	L	X	·	L	H
X	L	L	H	H	H	X	·	L	H
X	L	H	L	L	L	ML	·	L	H
X	L	H	L	L	H	ML	·	L	H
X	L	H	L	H	L	X	·	H	H
X	L	H	L	H	H	X	·	H	L
X	L	H	H	L	L	ML	·	L	H
X	L	H	H	L	H	ML	·	L	H
X	L	H	H	H	L	X	·	L	H
X	L	H	H	H	H	X	·	L	H
X	H	L	L	L	L	ML	·	L	H
X	H	L	L	L	H	ML	·	L	H
X	H	L	L	H	L	X	·	H	H
X	H	L	L	H	H	X	·	H	L
X	H	L	H	L	L	ML	·	L	H
X	H	L	H	L	H	ML	·	L	H
X	H	L	H	H	L	X	·	L	H
X	H	L	H	H	H	X	·	L	H
L	H	H	L	L	L	ML	·	L	H
L	H	H	L	L	H	ML	·	L	H
L	H	H	L	H	L	X	·	H	H
L	H	H	L	H	H	X	·	H	L
L	H	H	H	L	L	ML	·	L	H
L	H	H	H	L	H	ML	·	L	H
L	H	H	H	H	L	X	·	L	H
L	H	H	H	H	H	X	·	L	H
H	H	H	X	X	L	X	·	H	H
H	H	H	X	X	H	X	·	H	L
·	L	L	H	L	L	H	ML	H	H
·	L	L	H	L	H	H	ML	H	L
·	L	L	H	H	L	H	·	L	H
·	L	L	H	H	H	H	·	L	H

Definition of logic levels

Input	H	L	X
A	V_{ID} V_T max	V_{ID} V_T min	Irrelevant
S	V_I V_{IH} min	V_I V_{IL} max	Irrelevant

*Connect to detector output unless otherwise noted.

ML=Momentary low followed by a high

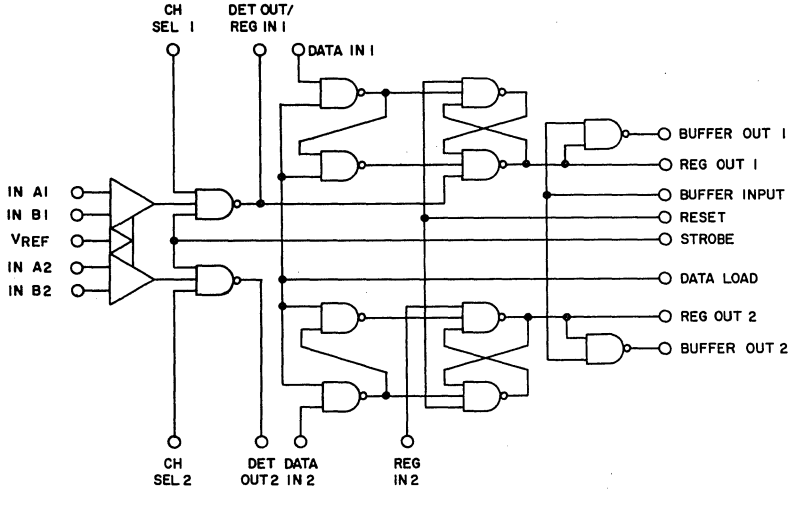
Absolute Maximum Ratings

Supply Voltages (See Note 1)
V_{CC+} 7V
V_{CC-} 7V
Differential Input Voltage, V_{ID} or V_{REF} ....±5V
Voltage any Input to Ground 5.5V
Storage Temperature Range −55°C to 150°C
Operating Temperature Range
3671-1, 3673-1 T_C .....—55°C to 125°C
3671-5, 3673-5 T_A .....0°C to 70°C

Recommended Operating Conditions

	Min	Nom	Max	Unit
V_{CC+} (See Note 1)	4.75	5	5.25	V
V_{CC-} (See Note 1) ..	−4.75	−5	—5.25	V
V_{REF} (See Note 1) ..	±1.5	±2.1	±4.5	V

Block Diagram — ITT3671



ELECTRICAL CHARACTERISTICS Over Specified Free-Air Temperature Range
V_{CC+} =5V, V_{CC-} = −5V, V_{REF} = —2.1V (Unless Otherwise Noted)

Symb.	Parameter	Min	Typ	Max	Test Fig.	Unit	Test Conditions	
V_T	Differential - Input	5		9			T_A =25°C	3671-1
		3		11			V_{CC+} =5V, V_{CC-} = −5V	3673-1
	Threshold Voltage	4		10			V_{REF} = −2.1V	3671-5
		1		13	1	mV		3673-5
							Oper. Temp. Range	
		4.5		9.5			V_{CC+} =5V ±5%	3671-1
		2		12			V_{CC-} = 5V ±5%	3673-1
		4		10			V_{CC+} =5V	3671-5
		1		13			V_{CC-} = −5V	3673-5
I_{IB}	Differential - input bias current		20		2	μA	V_{CC+} =5V, V_{CC-} = —5V, V_{ID} = OV	
I_{IO}	Differential - input offfset current		0.5		2	μA	V_{CC+} = 5V, V_{CC-} = —5V, V_{ID} = OV	
V_{IH}	High-level input voltage (strobe and logic inputs)	2			4,5	V		
V_{IL}	Low-level input voltage (strobe and logic inputs)			.8	4,5	V		
V_{OH}	High-level output voltage (register output)	2.4			4	V	V_{CC+} = 4.75V, V_{CC-} = —4.75V, I_{OH} = −120 μA	
V_{OH}	High-level output voltage (detector output)	2.4			5	V	V_{CC+} = 4.75V, V_{CC-} = —4.75V,	
I_{OH}	High-level output voltage (buffer output)			250	4	μA	V_{CC+} = 4.75V, V_{CC-} = —4.75V, V_{OH} = 5.25V	
V_{OL}	Low-level output voltage (register output)			.4	4	V	V_{CC+} = 4.75V, V_{CC-} = —4.75V, I_{OL} = 4.8ma	
V_{OL}	Low-level output voltage (detector output)			.4	5	V	V_{CC+} = 4.75V, V_{CC-} = —4.75V	
V_{OL}	Low-level output voltage (buffer output)			.5	4	V	V_{CC+} = 4.75V, V_{CC-} = —4.75V, I_{OL} = 25mA	

ELECTRICAL CHARACTERISTICS Over Specified Free-Air Temperature Range
V_{CC+} =5V, V_{CC-} = −5V, V_{REF} = —2.1V (Unless Otherwise Noted)

Symb.	Parameter	Min	Typ	Max	Test Fig.	Unit	Test Conditions
$-I_F$	Low-level input current: Strobe, reset, buffer input			−3.2	6	mA	V_{CC+} = 5.25V
	Register 2 channel select			—3.0 −1.6		mA mA	V_{CC-} = −5.25V,
	data load data in			—6.4 2.0		mA mA	V_{IL} = 0.4V
I_{RB}	High-level input current (strobe and logic inputs)			1	6	mA	V_{CC+} = 5.25V V_{CC-} = −5.25V, V_{IM} = 5.25V
I_R	High-level input current: Data in channel select			40 −750		μA μA	V_{CC+} = 5.25V
	Register Strobe, reset buffer input Data load			80 160		μA μA	V_{CC-} = −5.25V, V_{IH} = 2.4V
I_{OS}	Short-circuit output current register output	−20		—60	3	mA	V_{CC+} = 5V, V_{CC-} = −5.25V, V_O = OV −20
I_{REF}	Reference input current			.5	2	mA	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{REF} = −2.17, T_A = 25°C
I_{CC-}	Supply current from V_{CC-}			18	2	mA	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C
I_{CC+}	Supply current from V_{CC+}			55	2	mA	V_{CC+} = 5.25V V_{CC-} = −5.25V, T_A = 25°C

NOTE 1:
These voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS, V_{CC+} = 5V, V_{CC-} = -5V, V_{ref} = -2.1V, T_A = 25°C

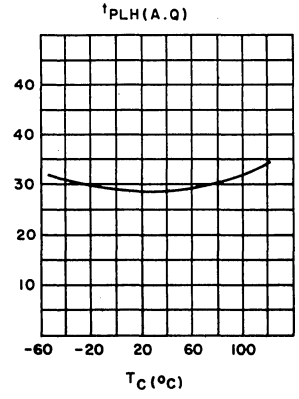
Delay Times

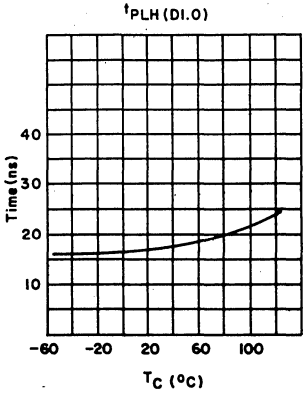
Symbol	From Input	To Output	Test Fig.	Min	Typ	Max	Unit	Test Conditions
t_{PLH} (A, Q)	A_I, A_2 or B_1, B_2	Q	7		28		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf
t_{PLH} (S, Q)	Strobe	Q	8		15		ns	R_Q=820Ω C_Q=50pf
t_{PLH} (DI, Q)	Data in	Q	9		17		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf
t_{PLH} (DL, Q)	Data load	Q	8		15		ns	R_Q=820Ω C_Q=50pf
t_{PHL} (R, Q)	Reset	Q	9		12		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf
t_{PLH} (R, X)	Reset	X	9		100		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf
tt_{PHL} (G, X)	Buffer In	X	9		15		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf
tt_{PHL} (A, X)	A_1, A_2 or B_I, B_2	X	7		42		ns	R_Q=820Ω C_Q=50pf R_X=520Ω C_X=450pf

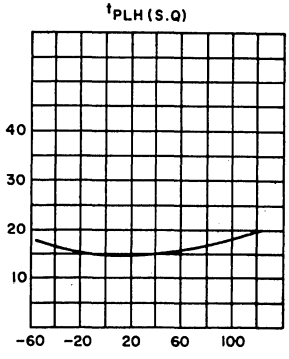
Transition Times		Test					
Symbol	Output	Fig.	Min	Typ	Max	Unit	Test Conditions
t_{TLH}(Q)	Q						R_Q = 820Ω
t_{THL}(Q)	Q	9					C_Q = 50pf
t_{TLH}(X)	X			150			R_X = 520Ω
t_{THL}(X)	X			12			C_X = 450pf

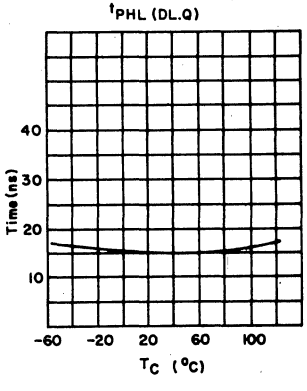
Parameter		TYP.	Unit	Test Conditions
t_{ORI}	One response to differential overload			
t_{ORO}	Zero response to differential overload			
V_{CMF}	Common mode firing voltage	1.5	V	f = 0.1 to 20 MHz

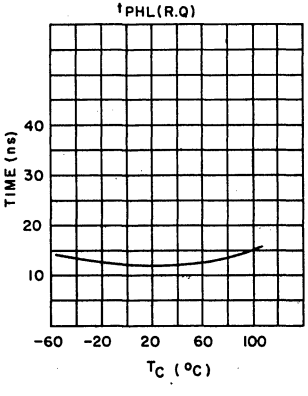
SWITCHING CHARACTERISTICS,
V_{CC+} = 5V, V_{CC-} = 5V, V_{REF} = −2.1V

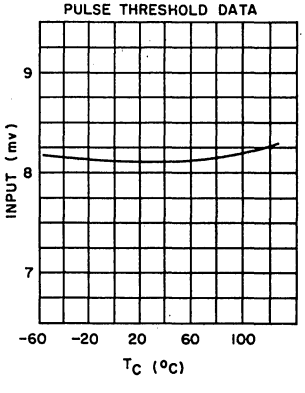


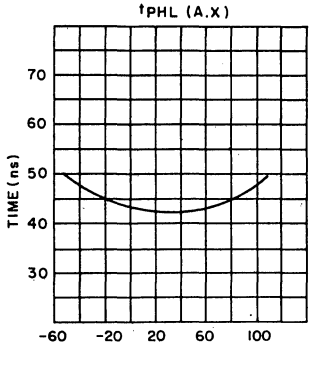












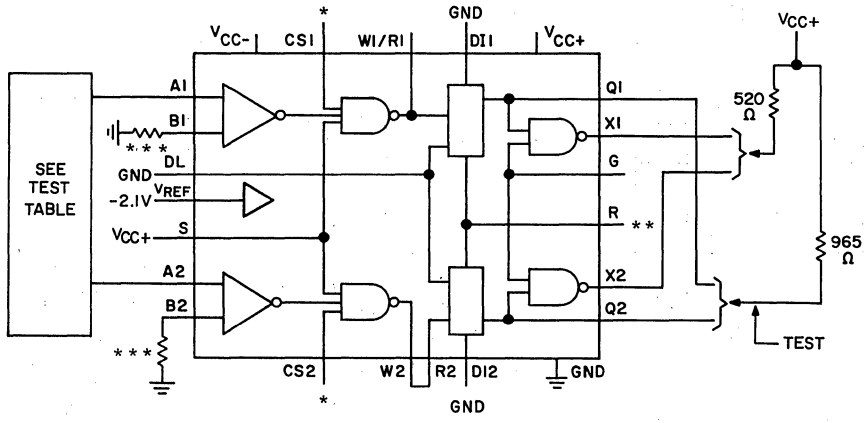


Fig. 1—V_T

*** Match impedance of B_1 and B_2 to A_1 and A_2.
** Apply a momentary low then a high.
* Apply Vcc+ to side under test, GND to other.

Test	Apply at Input A	Measure Output Q
Vt min.	+Vt min.	0.4V max.
Vt min.	—Vt min.	0.4V max.
Vt max.	+Vt max.	2.4V min.
Vt max.	—Vt max.	2.4V min.

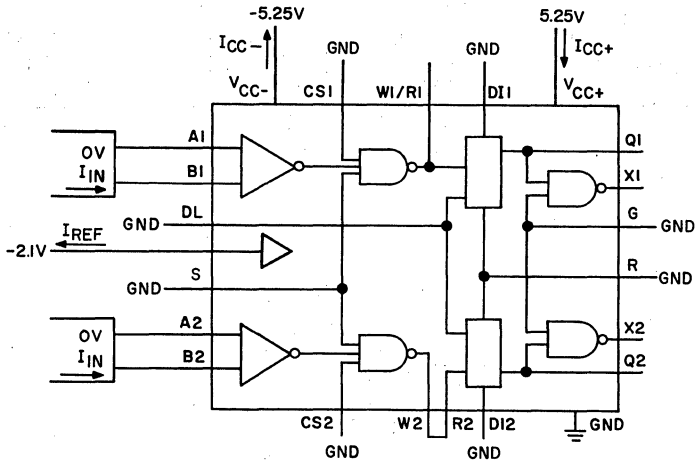
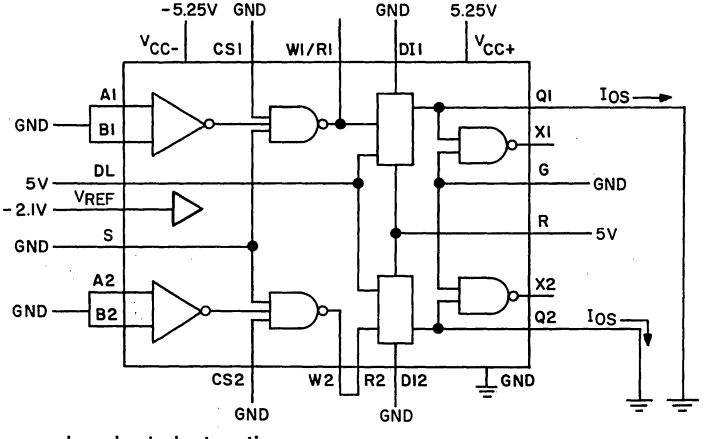


Fig. 2 — I'_B, I_{IO} = $I_{CC}+$, $I_{CC}-$, I_{REF}



Note:

Only one output may be shorted at a time.

Fig. 3—IOS

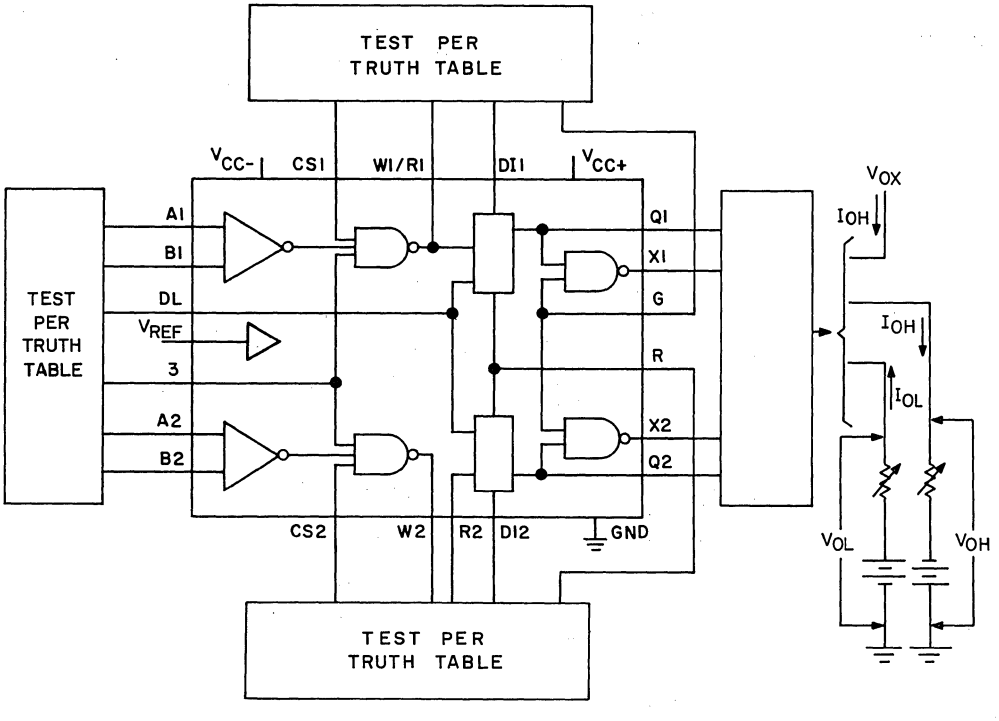
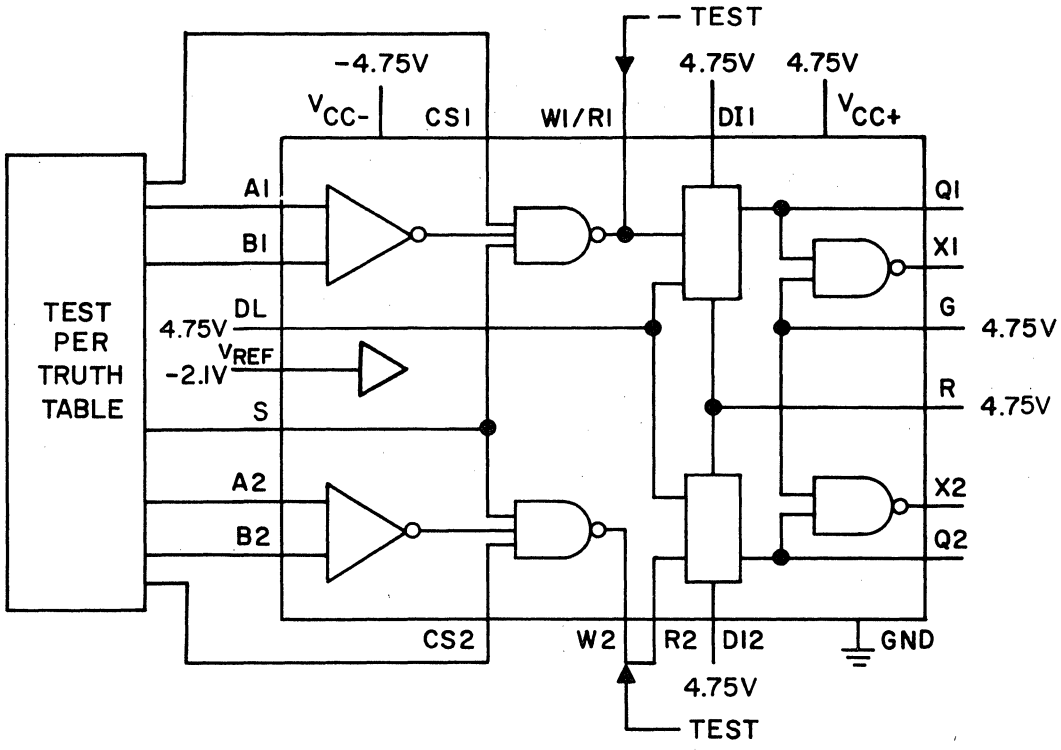
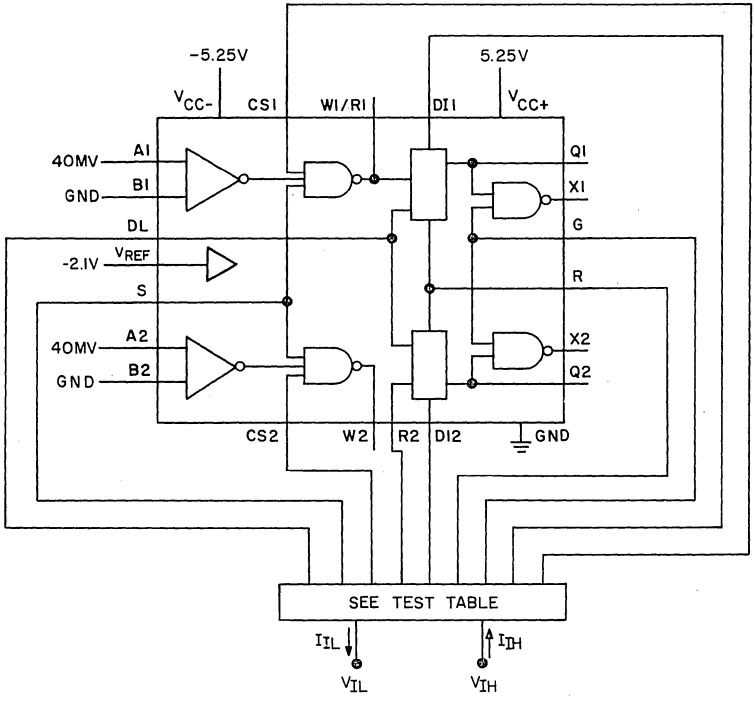


Fig. 4 —V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{OH}



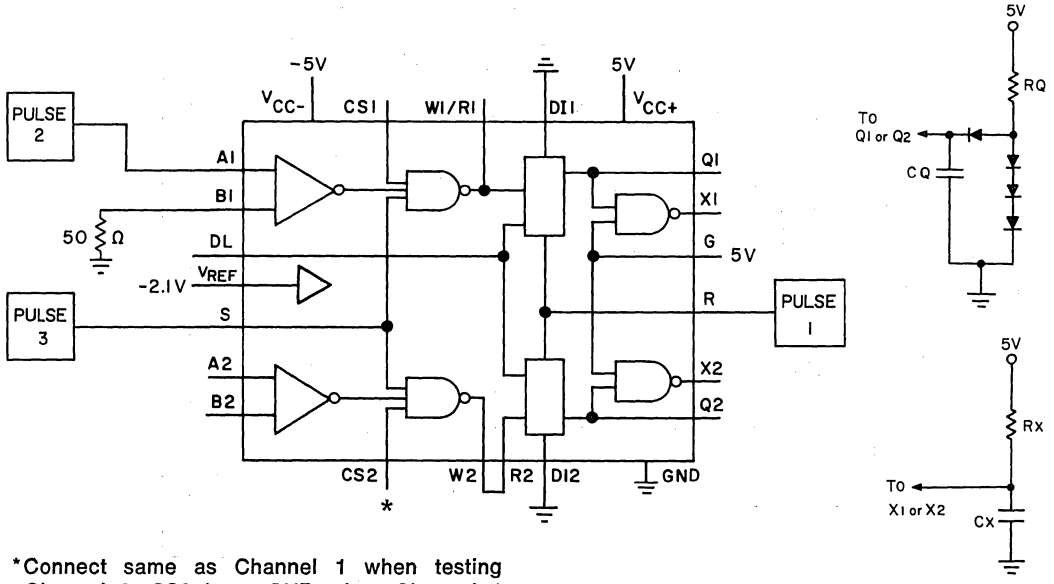
Test	Diff. Input	S	CS1	CS2
VOH at W1	GND	VIH	VIH	VIL
VOH at W1	40mV	VIL	VIH	VIL
VOH at W1	40mV	VIH	VIL	VIL
VOL at W1	40mV	VIH	VIH	VIL
VOH at W2	GND	VIH	VIL	VIH
VOH at W2	40mV	VIL	VIL	VIH
VOH at W2	40mV	VIH	VIL	VIL
VOL at W2	40mV	VIH	VIL	VIH

Fig. 5—V_{OH}, V_{OL}, V_{IH}, V_{IL}



Test	Strobe S	Channel CS1	Select CS2	Data DI 1	Input DI 2	Data Load DL	Reset R	Buffer Input 6	Register Input R2
IR at S	VIH	VIL	VIL	X	X	X	X	X	W2
IR at CS1	VIL	VIH	X	X	X	X	X	X	W2
IR at CS2	VIL	X	VIH	X	X	X	X	X	W2
IR at D11	X	X	X	VIH	X	VIL	X	X	W2
IR at D12	X	X	X	X	VIH	VIL	X	X	W2
IR at DL	X	X	X	VIL	VIL	VIH	X	X	W2
IR at R	X	X	X	VIH	VIH	VIH	VIH	X	W2
IR at G	VIL	X	X	X	X	VIL	VIL	VIH	W2
- IF at S	VIL	VIH	VIH	X	X	X	X	X	W2
- IF at CS1	VIH	VIL	VIL	X	X	X	X	X	W2
- IF at CS2	VIH	VIL	VIL	X	X	X	X	X	W2
- IF at D11	X	X	X	VIL	VIL	VIH	X	X	W2
- IF at D12	X	X	X	VIL	VIL	VIH	X	X	W2
- IF at DL	X	X	X	VIH	VIH	VIL	X	X	W2
- IF at R	VIH	VIH	VIH	X	X	VIL	VIL	X	W2
- IF at G	X	X	X	VIL	VIL	VIH	X	VIL	W2
- IF at R2	X	X	X	X	VIL	VIH	X	X	VIH
- IF at R2	X	X	X	X	X	VIL	VIL	X	VIL

Figure 6. - IF, IR



*Connect same as Channel 1 when testing Channel 2. CS2 is at GND when Channel 1 is tested.

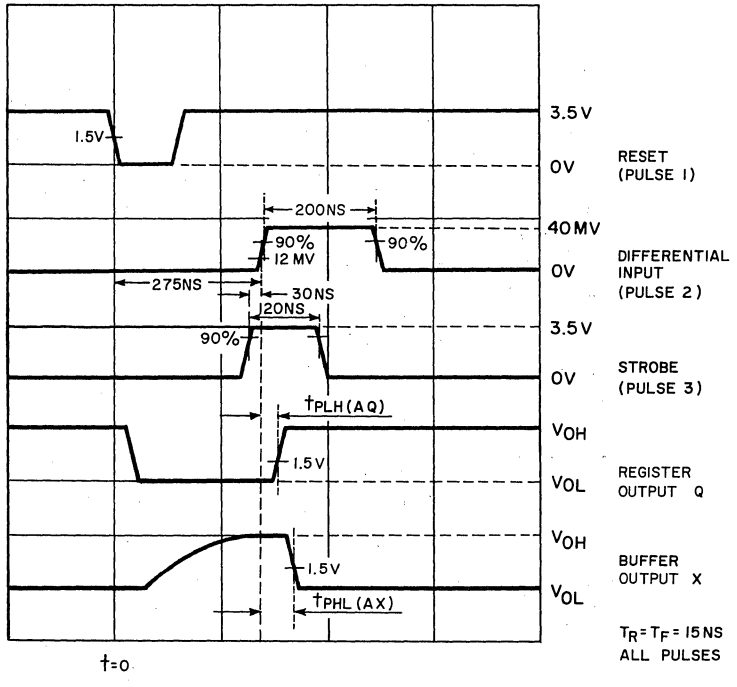
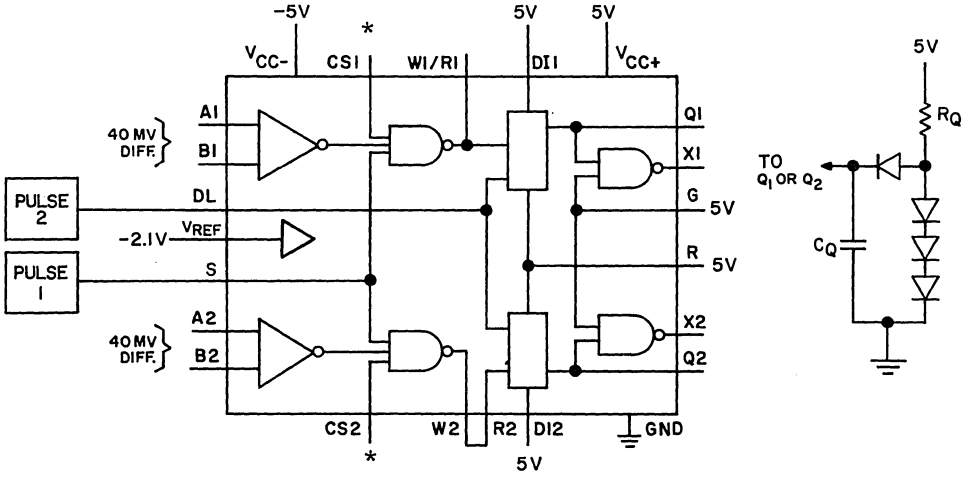


Figure 7



*GND channel select of unused side.

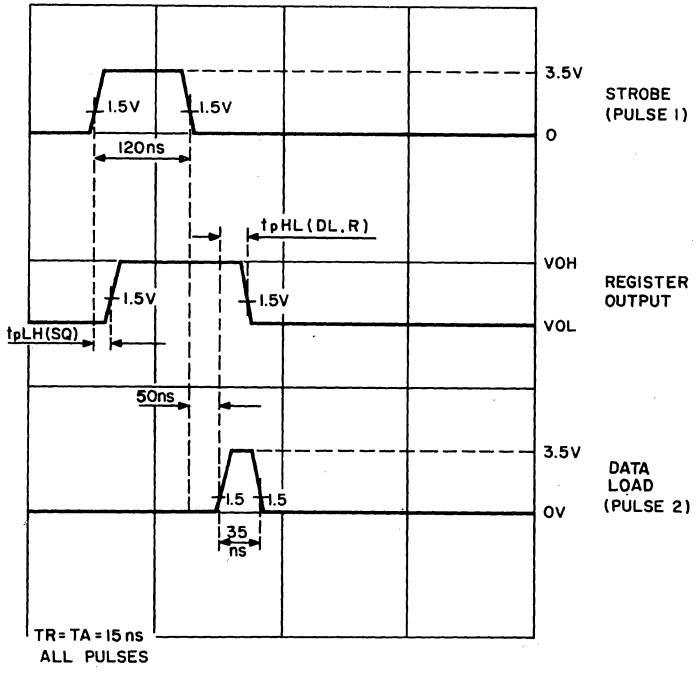
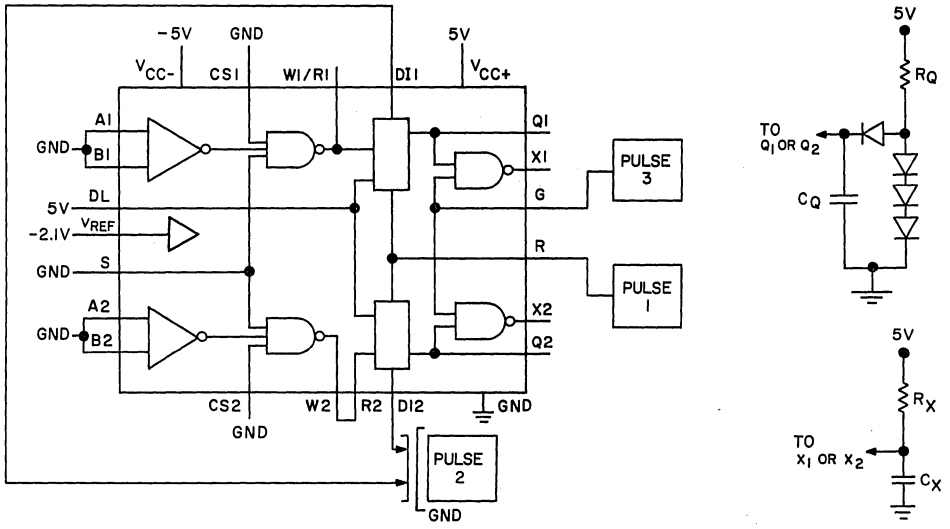


Figure 8


-5V
GND
5V
VCC-
CS1
WI/RI
DI1
VCC+
A1
GND
B1
DL
5V
-2.1V
VREF
S
GND
A2
GND
B2
Q1
X1
G
R
X2
Q2
PULSE 3
PULSE 1
CS2
GND
W2
R2
DI2
GND
PULSE 2
GND
5V
RQ
TO Q1 OR Q2
CQ
5V
RX
TO X1 OR X2
CX

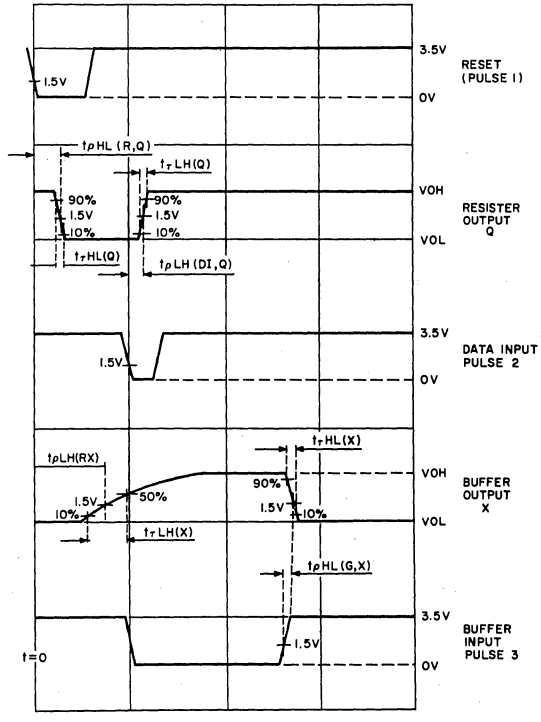

3.5V
1.5V
0V
RESET (PULSE 1)
tpHL (R,Q)
tTLH(Q)
VOH
90%
1.5V
10%
90%
1.5V
10%
VOL
RESISTER OUTPUT Q
tTHL(Q)
tpLH (DI,Q)
3.5V
1.5V
0V
DATA INPUT PULSE 2
tTHL(X)
tpLH(RX)
VOH
90%
1.5V
10%
50%
1.5V
10%
VOL
BUFFER OUTPUT X
tTLH(X)
tpHL(G,X)
3.5V
1.5V
t=0
0V
BUFFER INPUT PULSE 3

Figure 9

APPLICATION INFORMATION

Reference Voltage Considerations

The threshold level of both channels is determined by applying an external voltage to the V_{REF} terminal (Pin 21). The ratio of the external threshold reference voltage to the internal threshold reference voltage is 300 to 1. An internal reference of 7 mV may be established by applying ±2.1V to the V_{REF} input. The internal threshold reference voltage may be varied for individual system applications by adjusting the external reference voltage (see figure 10).

Input Line Layout Considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors, and the use of good ground planes to separate logic inputs and outputs from sense and reference input lines are recommended.

Sense-Input Termination Consideration

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values which will be compatible with the particular application. Matched termination resistors, (R_T, Figure 11), normally in the range of 25 ohms to 200 ohms each, are required not only to terminate the sense line in a desired impedance, but also to provide a dc path for the input bias current. Careful matching of the resistor pairs should be observed or the effective common-mode rejection will be reduced.

Output Drive Capability

The detector outputs, shown in figure 12, are intended to drive the internal data register. Detector output 1 is internally connected to input of data register 1 and available at pin 17. Detector output 2 is not connected internally to the input of data register 1 but is available at pint 14. The input of data register 2 is available at pin 9. For dual operation pin 9 is connected to pin 14; for dual channel operation pin 14 is connected to pin 17, this ANDs the two sense channels and provide an extra data register for other system applications.

The data register outputs, shown in figure 13, feature the ability to sink or supply load current and are rated at 3 series 74 loads.

The open-collector outputs of the data buffer, shown in figure 12, may be connected to similar outputs to perform the wire-AND function. These outputs are specially designed to drive high capacitive loads.

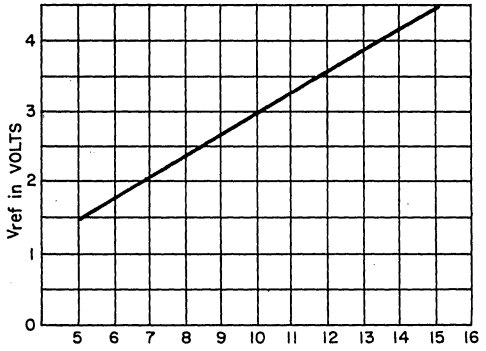


Fig. 10—Internal Reference Voltage in nV

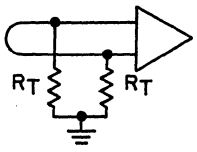


Figure 11

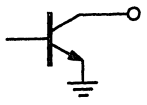


Figure 12

Equivalent Output Circuit
Detector Output
Buffer Output

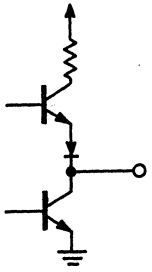


Fig. 13—Register Output

Logic Input Current Requirements

Logic input current requirements are specified at worse case power supply conditions over the operating temperature range. The logic currents are compatible with Series 74 TTL integrated Circuits. Input circuits are shown in figures 14 thru 17; current requirements are specified in the dc characteristics table.

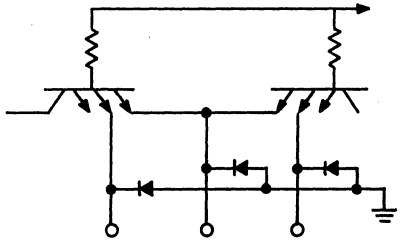


Fig. 14—Equivalent Input Circuit Strobe and Channel Select

Decoupling Node

An 0.01 uf capacitor may be placed between pin 23 and ground to enhance the stability of the input amplifiers.

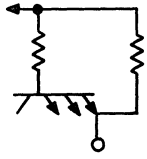


Fig. 15

Equivalent Buffer Input Buffer

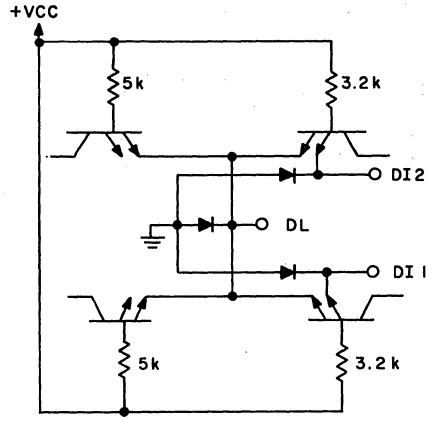


Fig. 16—Equivalent Circuit Data Input & Data Load

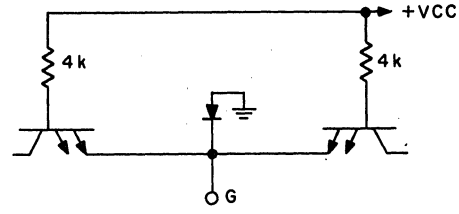


Fig. 17—Equivalent Buffer Input Circuit

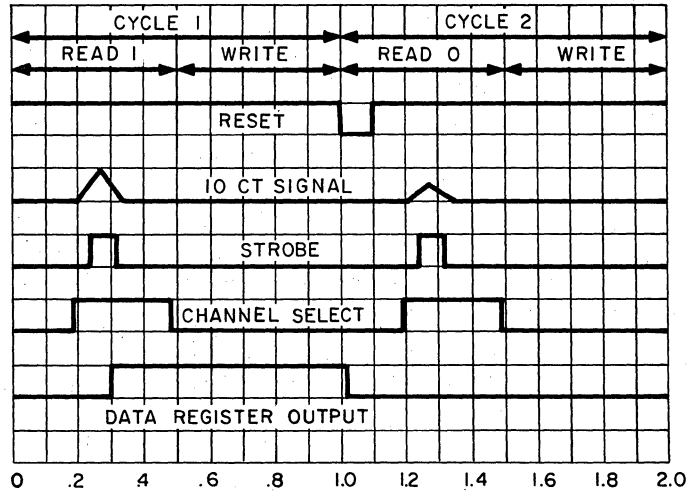


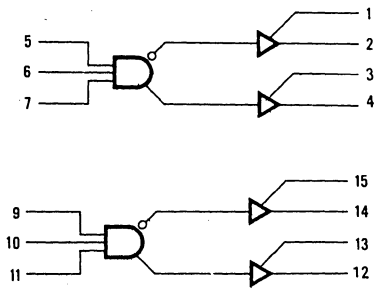
Fig. 18—Typical System Timing Diagram

DUAL DIFFERENTIAL LINE DRIVER

- Single 5 Volt Supply
- TTL Compatible Inputs
- Output Short Circuit Protection
- Input Clamp Diodes
- Output Clamp Diodes for Termination of Line Transients
- Complimentary Outputs for 'NAND', 'AND' Operation
- Uncommitted Collector Outputs for Wired-OR Application
- Military Temperature Range

The ITT9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 3). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both, input and output, to handle line transients.

Logic Diagram



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55° to +125°C
V_{CC1} Pin Potential to Ground Pin ..... −0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs) ..... ±20 V
Voltage Applied to Outputs for High Output State without Active Pull-up ..... 0.5 V to +13.2 V
Voltage Applied to Strobe.. −0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds) ..... 300°C
Internal Power Dissipation (Note 1)
Ceramic DIP ..... 730 mW
Flatpak ..... 570 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

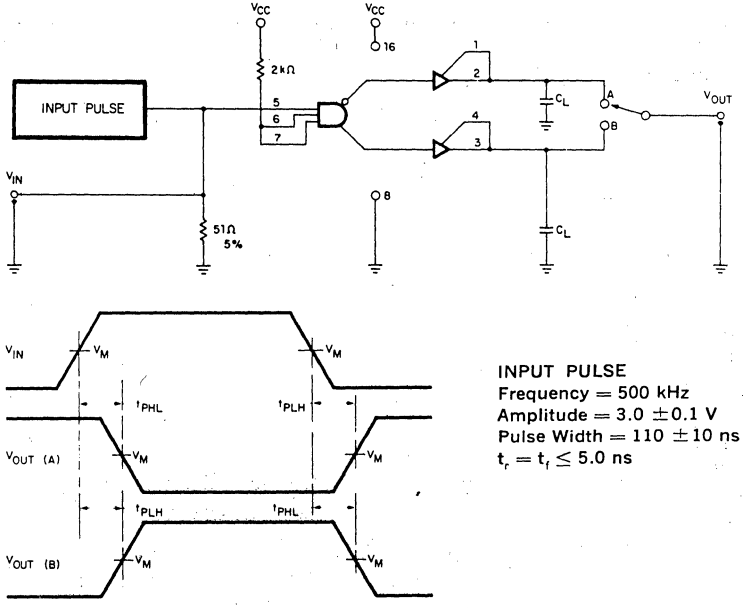
ELECTRICAL CHARACTERISTICS 9614-5
(0° C to +75° C, V_{CC} = 5.0V ±5%)

Symbol	Characteristic	Limits						Units	Conditions & Comments
		0°C		+25°C			+75°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OL}	Output Low Voltage		450		200	450	450	mV	I_{OL} = 40mA V_{CC} = 4.75V
V_{OH}	Output High Voltage Output	2.4		2.4	3.2		2.4	V	I_{OH} = −10mA V_{CC} = 4.75V
I_{SC}	"Short Circuit" Current			−40	−90	−120		mA	V_{OUT} = 0.0V V_{CC} = 5.25V
I_{CEX}	Output Leakage Current				10	100	200	μA	V_{CEX} = 5.25V V_{CC} = 5.25V
I_F	Input Forward Current		−1.60		−1.10	−1.60	−1.60	mA	V_F = 0.45V V_{CC} = 5.25V
I_R	Input Reverse Current				35	60	100	μA	V_R = 4.5V V_{CC} = 5.25V
V_{IL}	Guaranteed Input Low Voltage		0.85		1.3	0.85	0.85	V	V_{CC} = 5.25V
V_{IH}	Guaranteed Input High Voltage	1.9		1.8	1.5		1.6	V	V_{CC} = 4.75V
V_{OLC}	Clamped Low Output Voltage				−0.8	−1.5		V	I_{OLC} = −40mA V_{CC} = 5.25V
I_{CC}	Supply Current				33	48.7		mA	Inputs = O V V_{CC} = 5.25V
I_{max}	Supply Current				46	70		mA	Inputs = O V V_{MAX} = 7.0V
t_{PLH}	Turn-Off Time				14	30		ns	C_L = 30pF V_{CC} = 5.0V
t_{PHL}	Turn-On Time				18	30		ns	See Fig. 4 V_M = 1.5V
V_{IC}	Input Clamp Voltage				−1.0	−1.5		V	V_{CC} = 4.75V I_{IC} = −12mA

ELECTRICAL CHARACTERISTICS 9614-1
(—55° C to +125° C, V_{CC} =5.0V ±10%)

Symbol	Characteristic	Limits						Units	Conditions & Comments
		−55°C		+25°C			+125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OL}	Output Low Voltage		400		200	400	400	mV	I_{OL} =40mA V_{CC} =4.5V
V_{OH}	Output High Voltage	2.4		2.4	3.2		2.4	V	I_{OH} =−10mA V_{CC} =4.5V
I_{SC}	Output "Short Circuit" Current			−40	−90	−120		mA	V_{OUT} =0.0V V_{CC} =5.5V
I_{CEX}	Output Leakage Current				10	100	200	μA	V_{CEX} =12.0V V_{CC} =5.5V
I_F	Input Forward Current	−1.60			−1.10	−1.60	−1.60	mA	V_F =0.4V V_{CC} =5.5V
I_R	Input Reverse Current				35	60	100	μA	V_R =4.5V V_{CC} =5.5V
V_{IL}	Guaranteed Input Low Voltage		0.8		1.3	0.9	0.8	V	V_{CC} =5.5V
V_{IH}	Guaranteed Input High Voltage	2.0		1.7	1.5		1.4	V	V_{CC} =4.5V
V_{OLC}	Clamped Output Low Voltage				−0.8	−1.5		V	I_{OLC} =−40mA V_{CC} =5.5V
I_{CC}	Supply Current				34	48.7		mA	Inputs =O V V_{CC} =5.5V
I_{max}	Supply Current				46	65.7		mA	Inputs =O V V_{MAX} =7.0V
t_{PLH}	Turn-Off Time				14	20		ns	C_L =30pF V_{CC} =5.0V
t_{PHL}	Turn-On Time				18	20		ns	See Fig. 4 V_M =1.5V
V_{IC}	Input Clamp Voltage				−1.0	−1.5		V	V_{CC} =4.5V I_{IC} =−12mA

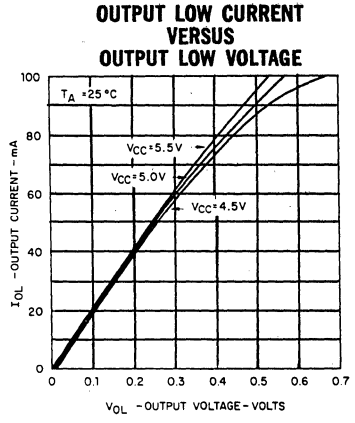
Switching Circuit and Waveforms

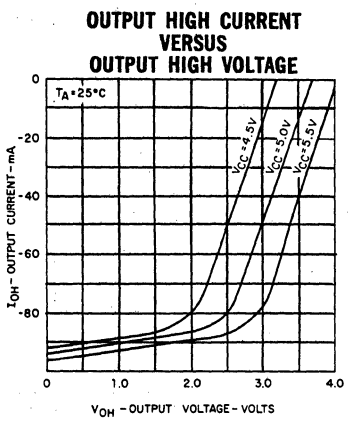


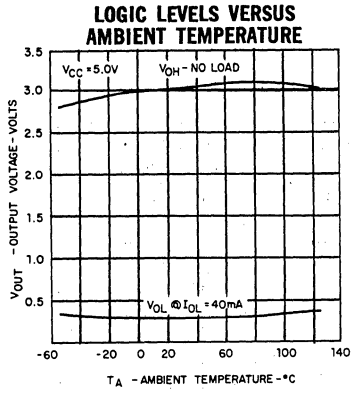
INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

Fig. 2

TYPICAL ELECTRICAL CHARACTERISTICS

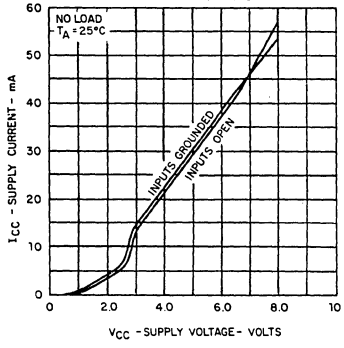




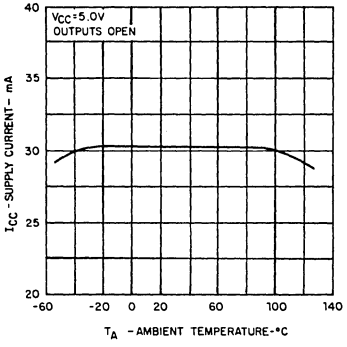


TYPICAL ELECTRICAL CHARACTERISTICS (continued)

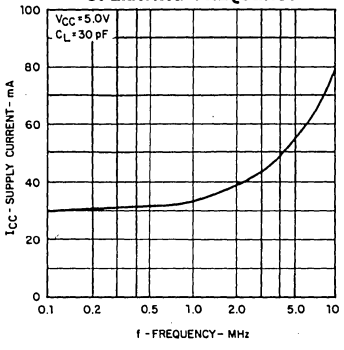
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



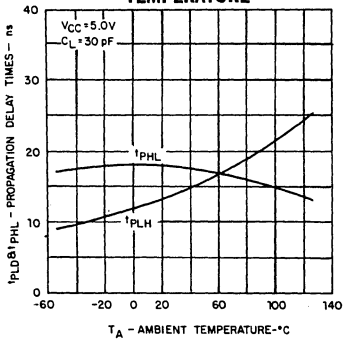
SUPPLY CURRENT VERSUS TEMPERATURE



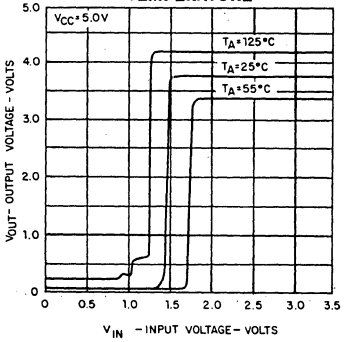
SUPPLY CURRENT VERSUS OPERATING FREQUENCY



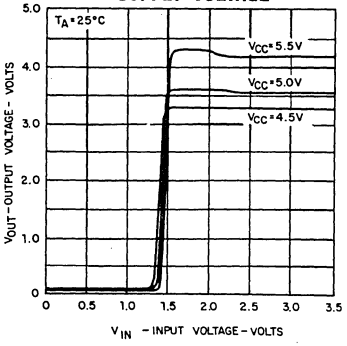
PROPAGATION DELAY TIME VERSUS TEMPERATURE



TRANSFER CHARACTERISTICS VERSUS TEMPERATURE

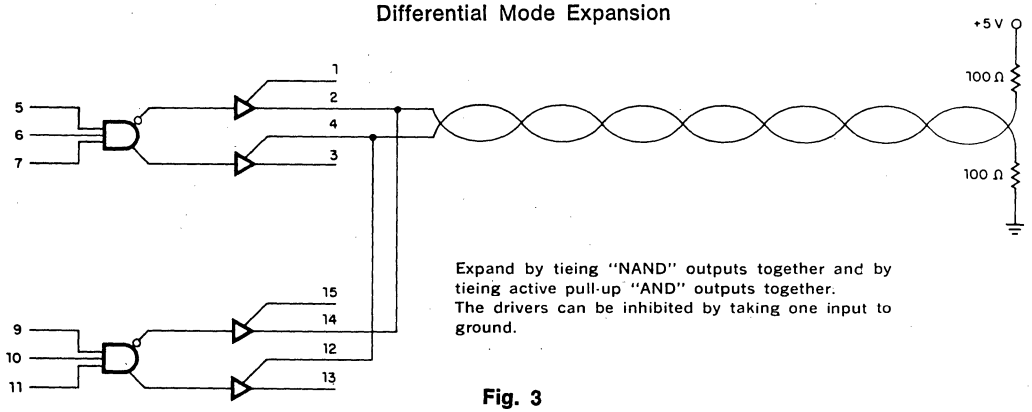


TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



Applications

Differential Mode Expansion



Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together.
The drivers can be inhibited by taking one input to ground.

Fig. 3

Typical Reflection Diagram

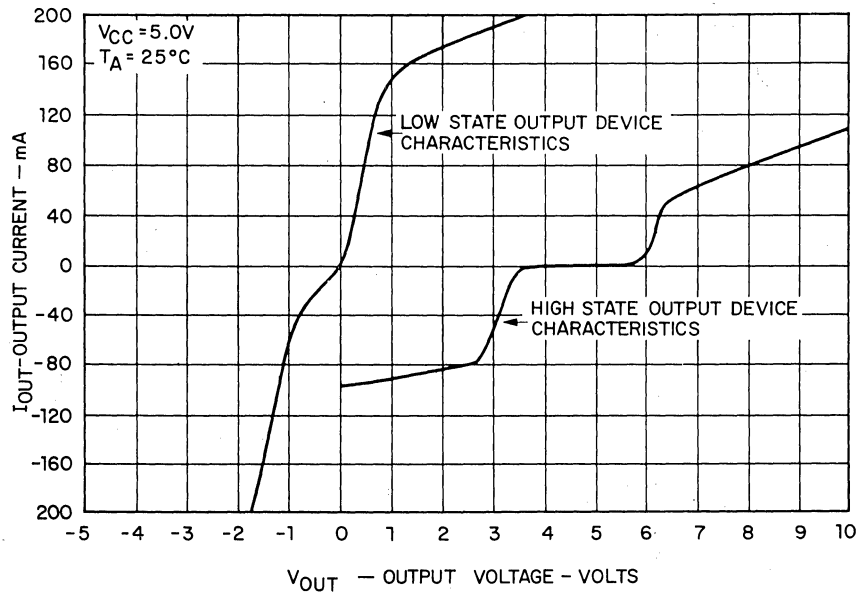
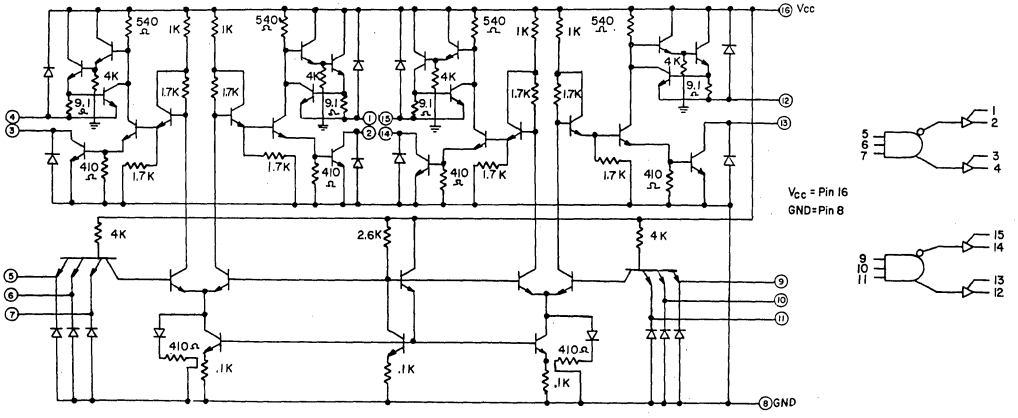


Fig. 4

CIRCUIT SCHEMATIC



DUAL DIFFERENTIAL LINE RECEIVER

- **TTL Compatible Output**
- **High Common Mode Voltage Range**
- **Choice of an Uncommitted Collector or Active Pull-Up**
- **Strobe**
- **Full Military Temperature Range**
- **Single 5 Volt Supply Voltages**
- **Frequency Response Control**
- **130 Ω Terminating Resistor**

GENERAL DESCRIPTION:

The ITT9615 is a dual differential line receiver designed to recieve differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe is provided along with a 130 Ω terminating resistor (at the inputs). The output has an uncommitted collector with an active pull-up available on an adjacent pin.

APPLICATIONS

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55° to +125°C
V_{CC1} Pin Potential to Ground Pin ..... −0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs) ..... ±20 V
Voltage Applied to Outputs for High Output State without Active Pull-up ..... 0.5 V to +13.2 V

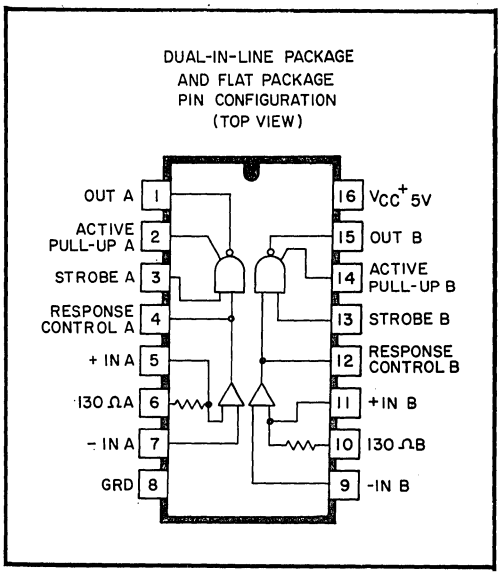


Fig. 3

Voltage Applied to Strobe.. −0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds) ..... 300°C
Internal Power Dissipation (Note 1)
Ceramic DIP ..... 730 mW
Flatpak ..... 570 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

ELECTRICAL CHARACTERISTICS 9615-1 (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%)

Symbol	Characteristics	Limits −55°C Min.	Limits −55°C Max.	Limits +25°C Min.	Limits +25°C Typ.	Limits +25°C Max.	Limits +125°C Min.	Limits +125°C Max.	Units	Conditions & Comments
V_{OL}	Output Low Voltage		0.40		0.18	0.40		0.40	Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.2		2.4	3.2		2.4		Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = 5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF}=V_{CC}=4.5 V
I_{SC}	Output Shorted Current			−15	−39	−80			mA	V_{CC} = 5.5 V, **V_{SC} = O V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = −0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = −0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	-15	+15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			ohms	V_{CC} = 5.0 V, $V_{N(R)}$ = 1.0 V, +Input = Gnd.
V_{TH}	Differential Input Threshold Voltage		500		80	*500		500	mV	V_{CC} = 5.0 V ± 10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, −Inputs = O V, +Inputs = 0.5 V

ELECTRICAL CHARACTERISTICS 9615-1 (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%) **(continued)**

Symbol	Characteristics	Limits −55°C Min.	Limits −55°C Max.	Limits +25°C Min.	Limits +25°C Typ.	Limits +25°C Max.	Limits +125°C Min.	Limits +125°C Max.	Units	Conditions & Comments
t_{pd-}	Turn-off Time				30	50			ns	R_L = 3.9 KΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig 4
t_{pd-}	Turn-on Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4

*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "—IN B".

**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

ELECTRICAL CHARACTERISTICS 9615-5 (Temperature Range O°C to + 75°C, V_{CC} = 5.0 V ±5%)

Symbol	Characteristics	Limits O°C Min.	Limits O°C Max.	Limits +25°C Min.	Limits +25°C Typ.	Limits +25°C Max.	Limits +75°C Min.	Limits +75°C Max.	Units	Conditions & Comments
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, V_{OUT} = **, I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.75 V, V_{OUT} = **, I_{OH} = 5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC} = 4.75V
I_{SC}	Output Shorted Current			−14		—100			mA	V_{CC} = 5.25 V, **V_{SC} = OV, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	—0.7		−0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V, Other Input = 5.25V
$I_{IN(ST)}$	Strobe Input Current				−1.15	—2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V, *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	—3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V

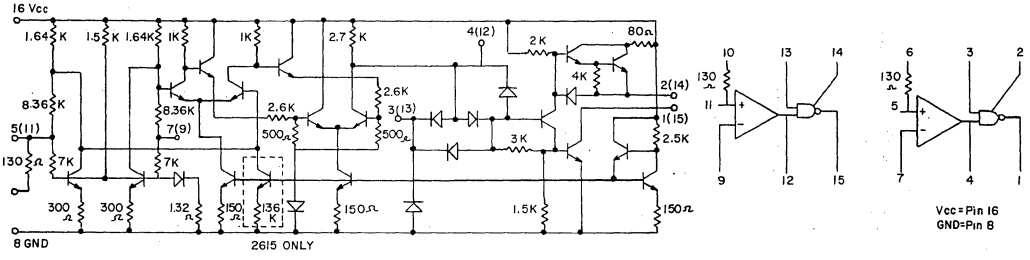
ELECTRICAL CHARACTERISTICS 9615-5 (Temperature Range O°C to + 75°C, V_{CC} = 5.0 V ±5%) **(continued)**

Symbol	Characteristics	Limits						Units	Conditions & Comments
		O°C		+25°C			+75°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	-15 +15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0	10	μA	V_{CC} = 4.75 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179		ohms	V_{CC} = 5.0 V, $V_{N(R)}$ = 1.0 V, +Input = Gnd.
V_{IH}	Differential Input Threshold Voltage	500			80	500	500	mV	V_{CC} = 5.0 V ± 5%
I_{CC}	Power Supply Current				28.7	50		mA	V_{CC} = 5.25 V, + Inputs = 0.5 V, −Inputs = O V
t_{pd-}	Turn-off Time				30	75		ns	R=3.9Ω, V_{CC} =5.0 V, C_L = 30 pF. Fig. 4
t_{pd-}	Turn-on Time				30	75		ns	R_L = 390Ω, V_{CC} =5.0 V, C_L = 30 pF. Fig. 4

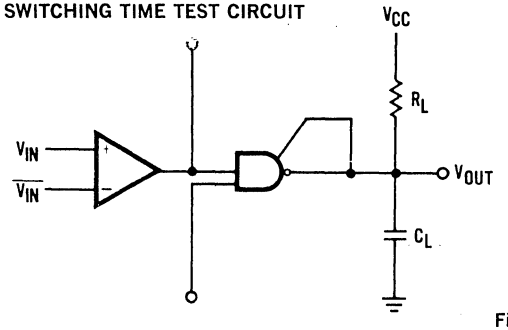
*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "—IN B"

*Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up B"

Schematic



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

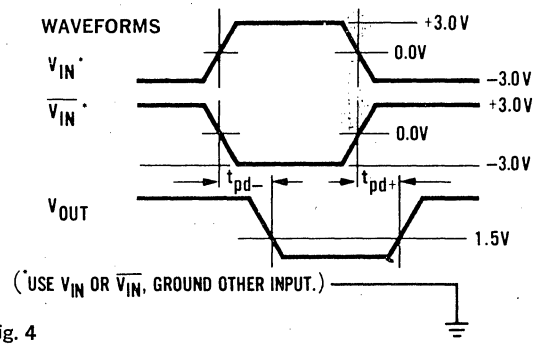


Fig. 4

Photograph of a 9615 switching differential data in the presence of high common mode noise.

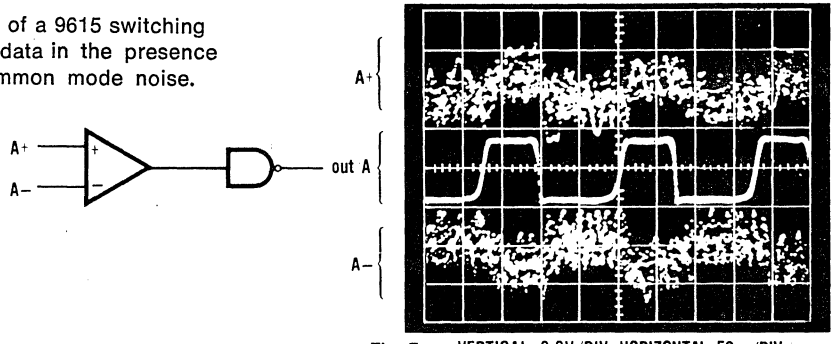


Fig. 5 VERTICAL=2.0V/DIV. HORIZONTAL=50ns/DIV.

STANDARD USAGE

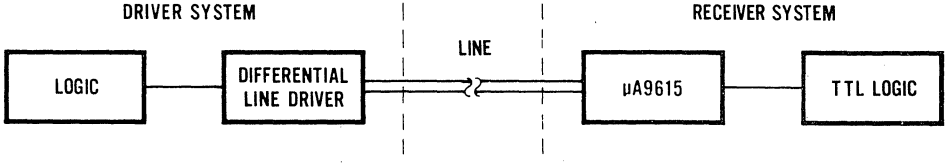
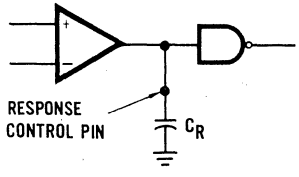


Fig. 6

FREQUENCY RESPONSE CONTROL



FREQUENCY RESPONSE VERSUS CAPACITANCE

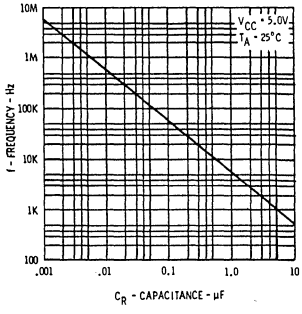
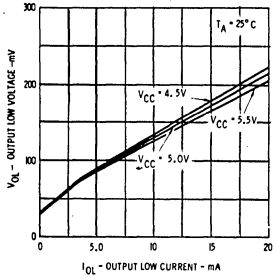


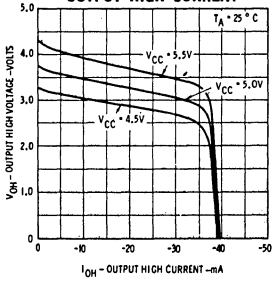
Fig. 7

TYPICAL ELECTRICAL CHARACTERISTICS

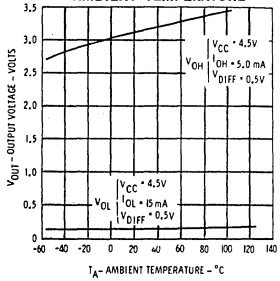
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



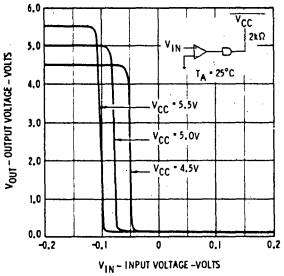
OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



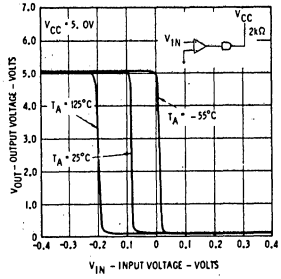
OUTPUT VOLTAGE VERSUS AMBIENT TEMPERATURE



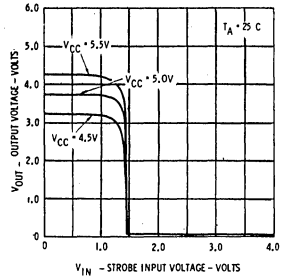
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



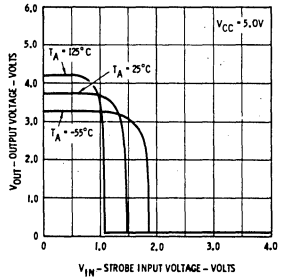
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS TEMPERATURE



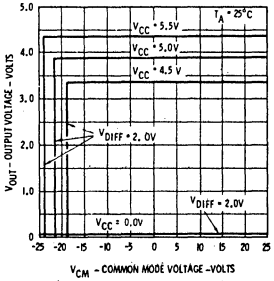
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



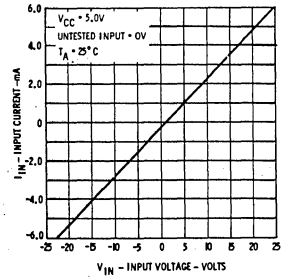
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS AMBIENT TEMPERATURE



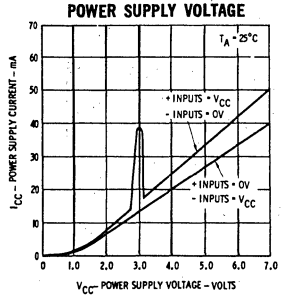
OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



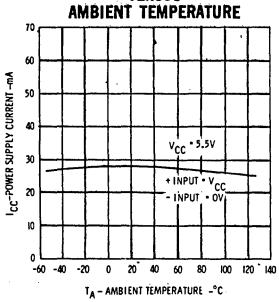
INPUT CURRENT VERSUS INPUT VOLTAGE



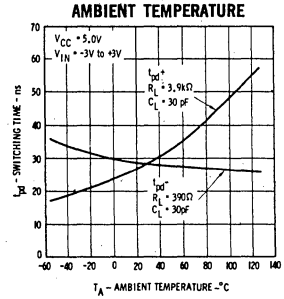
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

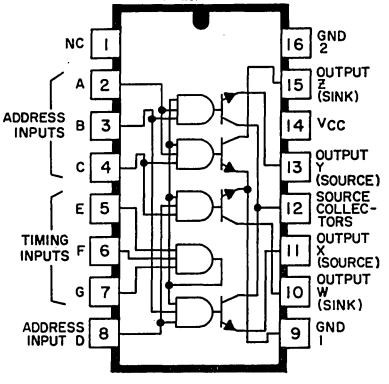


SWITCHING TIME VERSUS AMBIENT TEMPERATURE



MEMORY DRIVER WITH DECODE INPUTS

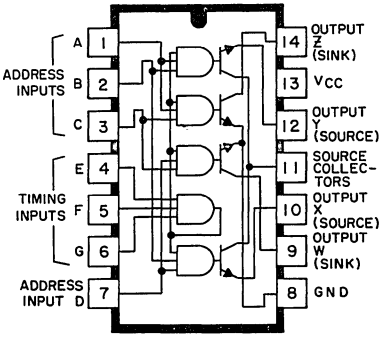
DUAL-IN-LINE PACKAGE (TOP VIEW)
Ceramic



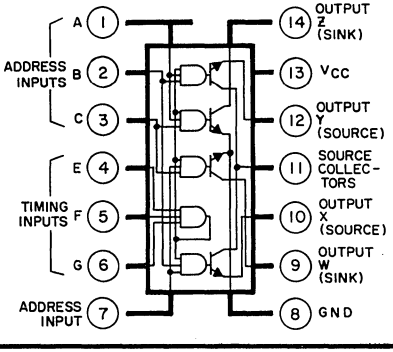
GND 1 and GND 2 are to be used in parallel

NC—No internal connection

DUAL-IN-LINE PACKAGE (TOP VIEW)
Plastic



FLAT PACKAGE (TOP VIEW)



PERFORMANCE

- **fast switching times**
- **400-mA output capability**
- **internal decoding and timing circuitry**
- **dual sink/source outputs**
- **output short-circuit protection**

EASE OF DESIGN

- **TTL or DTL compatibility**
- **eliminates transformer coupling**
- **reduces drive-line lengths**
- **increases reliability**
- **minimizes external components**
- **choice of flat or dual-in-line packages**

Description

The ITT75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source of sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

The ITT75324 is characterized for operation from 0°C to 70°C.

ITT75324
MEMORY DRIVER WITH DECODE INPUTS

TRUTH TABLE

Inputs							Outputs			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	On	Off	Off	Off
0	1	0	1	1	1	1	Off	On	Off	Off
1	1	0	0	1	1	1	Off	Off	On	Off
1	0	1	0	1	1	1	Off	Off	Off	On
x	x	x	x	0	x	x	Off	Off	Off	Off
x	x	x	x	x	0	x	Off	Off	Off	Off
x	x	x	x	x	x	0	Off	Off	Off	Off

NOTES:

1. X = Logical 1 or logical 0.
2. Not more than one output is to be allowed to be ON at one time: When all timing inputs are at a logical 1, two of the address inputs must be at logical 0.

Standard positive logic applies with the following definitions used for specifying digital-level signals:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

Absolute Maximum Ratings Over Operating Case Temperature Range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) 17V
Input voltage (See Note 2) 5.5V
Operating case temperature range 0°C to 70°C
Continuous total power dissipation at (or below) 70°C case temperature 800mV
Storage temperature range .. −65°C to 150°C

NOTES:

1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 14V, T_C = 0°C to 70°C)

	Parameter	Min	Typ*	Max	Unit	Test Conditions
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	3.5			V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input			0.8	V	
$I_{in(1)}$	Logical 1 level address input current			200	μA	V_{in} = 5V
$I_{in(1)}$	Logical 1 level timing input current			100	μA	V_{in} = 5V
$I_{in(0)}$	Logical 0 level address input current			−6	mA	V_{in} = 0V
$I_{in(0)}$	Logical 0 level timing input current			−12	mA	V_{in} = 0V
$V_{(sat)}$	Sink saturation voltage		0.75	0.85	V	$I_{sink} \cong$ 420 mA, R_L = 53Ω
$V_{(sat)}$	Source saturation voltage		0.75	0.85	V	$I_{source} \cong$ −420 mA, R_L = 47.5Ω
I_{off}	Output reverse current (off state)		125	200	μA	V_{in} = 0V
I_{CC}	Supply current, all sources and sinks off		12.5	15	mA	V_{in} = 0V
I_{CC}	Supply current, either sink selected		30	40	mA	
I_{CC}	Supply current, either source selected		25	35	mA	

*These typical values are at T_C = 25°C.

Switching Characteristics, V_{CC} = 14 V, T_C = 25°C

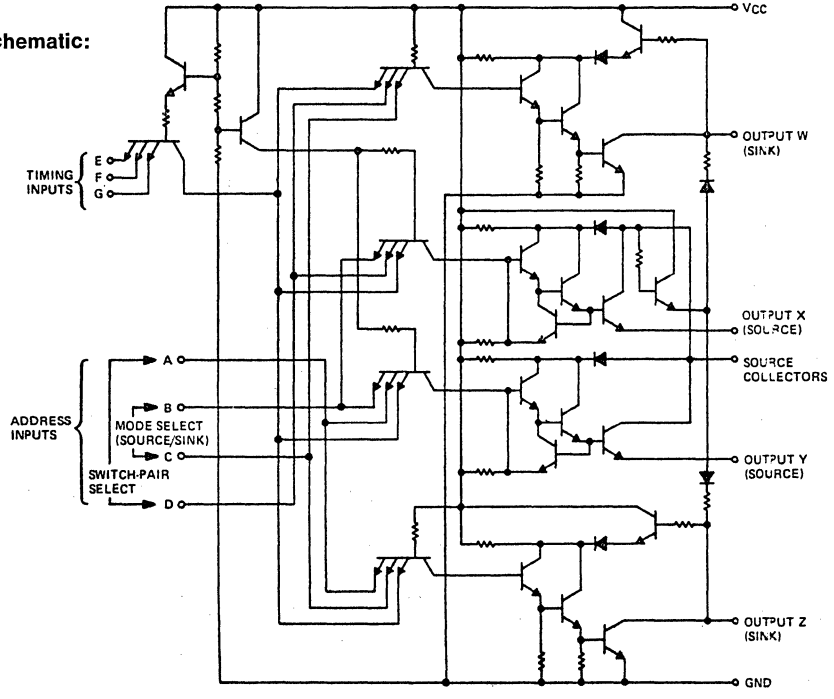
	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{pd(1)}$	Propagation delay time to logical 1 level, source output			90	ns	R_{L1} = 53Ω, R_{L2} = 500Ω, C_L = 20 pF
$t_{pd(0)}$	Propagation delay time to logical 0 level, source output			50	ns	
$t_{pd(1)}$	Propagation delay time to logical 1 level, sink output			110	ns	R_L = 53Ω, C_L = 20pF
$t_{pd(0)}$	Propagation delay time to logical 0 level, sink output			40	ns	
t_s	Sink storage time			70	ns	

Thermal Information

The ITT75324 is designed to be used at a case temperature not to exceed 70°C. Under this condition, infrared microradiometer and X-ray studies indicate that a safe junction temperature is maintained under specified worst-case conditions.

ITT75324 circuits should be mounted so that minimum thermal resistance is achieved. A thermal compound should be used between bottom of the flat package and a heat sink. This, in conjunction with unrestricted forced air flow across the heat sink and package, has been found to adequately satisfy thermal requirements. No thermal compound is required with the dual-in-line package. Air flow should be across the short dimension of either package.

Schematic:



PARAMETER MEASUREMENT INFORMATION

D-C Test Circuits*

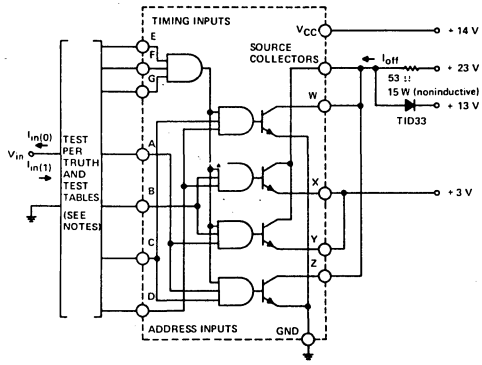


FIGURE 1 — $V_{in(0)}$, $V_{in(1)}$, $I_{in(0)}$, $I_{in(1)}$, and I_{off}

NOTES:

1. Check $V_{in(1)}$ and $V_{in(0)}$ per Truth Table.
2. Measure $I_{in(0)}$ per Test Table.
3. When measuring $I_{in(1)}$, all other inputs are at ground. Each input is tested separately.

TEST TABLE FOR $I_{in(0)}$

Apply. 3.5V	Ground	Test $I_{in(0)}$
B, C. E. F, and G	A and D	A
B, C. E. F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

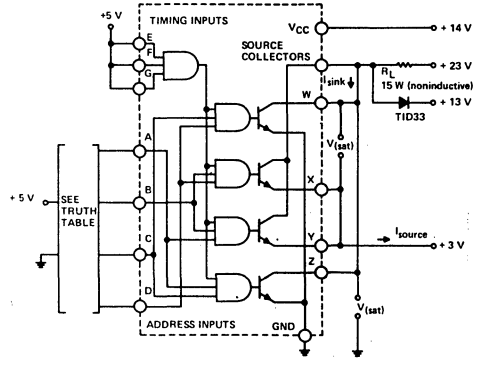


FIGURE 2 — $V_{(sat)}$

*Arrows indicate actual direction of current flow.

NOTE:

This parameter must be measured using pulse techniques. t_p = 500 ns, duty cycle ⩽ 1%.

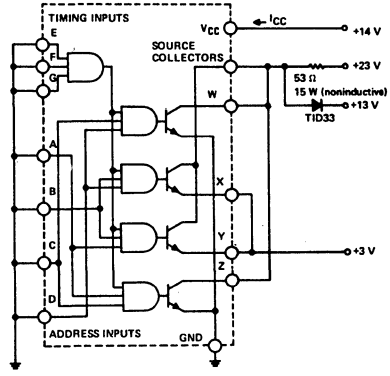


FIGURE 3 — I_{CC} (All Outputs Off)

PARAMETER MEASUREMENT INFORMATION

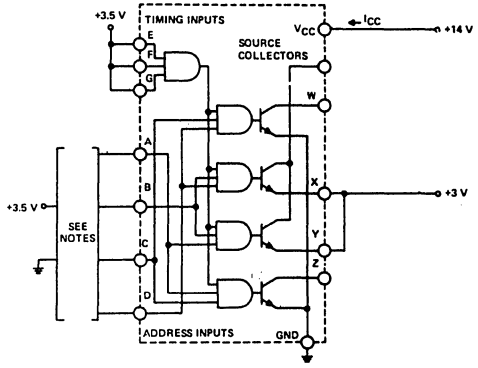
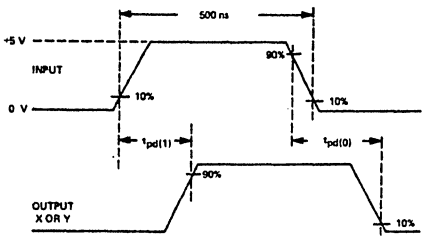


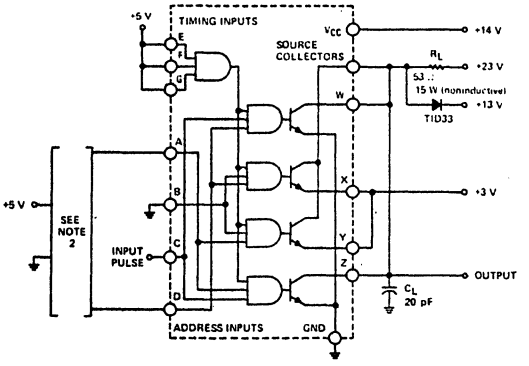
FIGURE 4 — I_{CC} (One Output On)

NOTES:

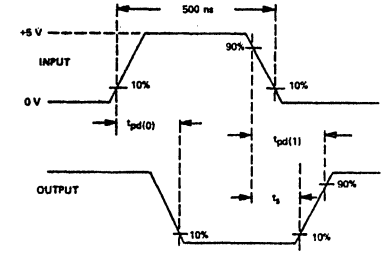
1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).



VOLTAGE WAVEFORMS

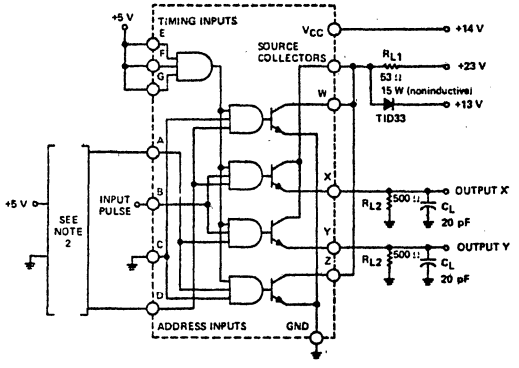


TEST CIRCUIT



VOLTAGE WAVEFORMS

Switching Characteristics



TEST CIRCUIT

NOTES:

1. The input waveform is supplied by a generator with the following characteristics: t_r = t_f = 10 ns, duty cycle $\leqslant$ 1%, and $Z_{out} \approx 50\Omega$.
2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **Tight Transient Response Specs**
- **Low Input Offset Voltage**
- **Large Input Common Mode Range**
- **High Output Voltage Swing**

The ITT709-1 and ITT709-5 are high-gain operational amplifiers consctructed on a single silicon chip using the ITT Planar epitaxial process. They feature low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The devices display exceptional temperature stability and will operate over a wide voltage range with little degradation of performance. These amplifiers are intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. The devices utilize the same pin configuration.

ABSOLUTE MAXIMUM RATINGS

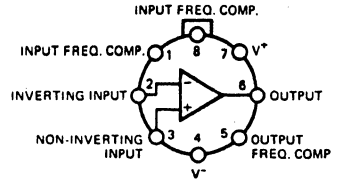
Characteristics	Units
Supply Voltage	±18 Volts
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5.0 Volts
Input Voltage	±10 Volts
Output Short-Circuit Duration (T_A = 25°C)	5 sec.
Storage Temperature Range	−65 to +150°C
Operating Temperature Range (Note 2)	−55 to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE 1

Rating applies to the ITT709-1 at case temperatures to + 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C. The rating for the ITT709-5 is 250mW and applies for case temperatures to +70°C.

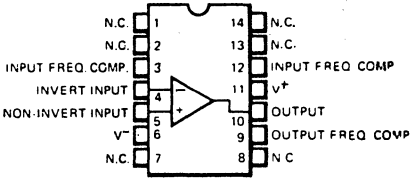
CONNECTION DIAGRAMS
(TOP VIEWS)

8 LEAD METAL CAN

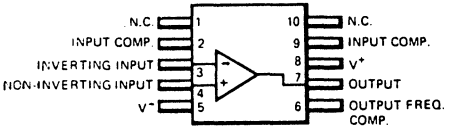


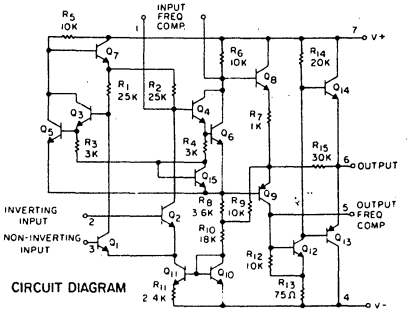
NOTE: Pin 4 connected to case

14 LEAD DIP



FLATPAK





CIRCUIT DIAGRAM

NOTE 2:

Rating for the ITT709-5 is 0° to +70°C.

ELECTRICAL CHARACTERISTICS ITT709-A (T_A = + 25° C, ±9V≤V_S≤±15V unless otherwise noted)

Parameter (see definitions)	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		0.6	2.0	mV	R_S≤10KΩ
Input Offset Current		10	50	nA	
Input Bias Current		100	200	nA	
Input Resistance	350	700		KΩ	
Output Resistance		150		Ω	
Power Consumption		75	108	mW	V_S = ±15V
Transient Response Risetime			1.5	μs	V_{in} = 20mV, R_L = 2 KΩ C_1 = 5000 pF, R_1 = 1.5 KΩ C_2 = 200pF, R_2 = 50Ω
Overshoot			30	%	C_L≤100pF
The following specifications apply for —55°C≤T_A≤+125°C:					
Input Offset Voltage			3.0	mV	R_S ≤ 10KΩ
Average Temperature Coefficient of Input Offset Voltage		1.8	10	μV/°C	R_S = 50Ω T_A = +25°C TO T_A = +125°C
		1.8	10	μ/V°C	R_S = 50Ω T_A = +25° TO T_A = —55°C
		2.0	15	μ/V°C	R_S≤10KΩ T_A = +25°C TO T_A = 125°C
		4.8	25	μ/V°C	R_S = 10KΩ T_A = +25°C TO T_A = —55°C
		0.08	0.5	nA/°C	T_A = +25°C TO T_A = +125°C
		0.45	2.8		T_A = +25°C TO T_A = +55°C
Large-Signal Voltage Gain	25,000		70,000		V_S = ±15V, R_L≥2KΩ, V_{out} = ±10V
Output Voltage Swing	±12	±14		V	V_S = ±15V, R_L≥10KΩ
	±10	±13		V	V_S = ±15V, R_L≥2KΩ
Input Voltage Range	±8.0			V	V_S = ±15V
Common Mode Rejection Ratio	80	110		db	R_S≤10KΩ
Supply Voltage Rejection Ratio		40	100	μV/V	R_S≤10KΩ
Supply Current		2.1	3.0	mA	T_A = +125°C, V_S = ±15V
		2.7	4.5	mA	T_A = —55°C, V_S = 15V
Power Consumption		63	90	mA	T_A = +125°C, V_S = ±15V
		81	135	mA	T_A = —55°C, V_S = 15V
Input Offset Current		35	50	nA	T_A = +125°C
		40	250	nA	T_A = —55°C
Input Bias Current		300	600	nA	T_A = —55°C
Input Resistance	85	170		KΩ	

ELECTRICAL CHARACTERISTICS ITT709-1 ($T_A = +25°C$, $\pm 9V \leqslant V_S \leqslant 15V$ unless otherwise noted)

Parameter (see definitions)	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	5.0	mV	$R_S \leqslant 10K\Omega$
Input Offset Current		50	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	150	400		KΩ	
Output Resistance		150		Ω	
Power Consumption		80	165	mW	$V_S = \pm 15V$
Transient Response					$V_{in} = 20mV$, $R_L = 2K\Omega$,
Risetime		0.3	1.0	μs	$C_1 = 5000pF$, $R^1 = 1.5\ K\Omega$
					$C_2 = 200pF$, $R_2 = 50\Omega$
Overshoot		10	30	%	$C_L \leqslant 100pF$

The following specifications apply for $-55° \leqslant T_A \leqslant +125°C$

Input Offset Voltage			6.0	mV	$R_S \leqslant 10K\Omega$
Average Temperature					
Coefficient of Input Offset		3.0		μV/°C	$R_S = 50\Omega$
Voltage		6.0		μV/°C	$R_S \leqslant 10K\Omega$
Large-Signal Voltage Gain	25,000	45,000	70,000	μV/°C	$V_S = \pm 15V$, $R_L \geqslant 2K\Omega$ $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$V_S = \pm 15V$, $R_L \geqslant 10K\Omega$
	±10	±13		V	$V_S = \pm 15V$, $R_L \geqslant 2K\Omega$
Input Voltage Range	±8.0	±10		V	
Common Mode Rejection Ratio	70	90		db	$V_S = \pm 15V$
Supply Voltage Rejection Ratio		25	150	μV/V	$R_S \leqslant 10K\Omega$
Input Offset Current		20	200	nA	$R_S \leqslant 10K\Omega$
		100	500	nA	$T_A = +125°C$
Input Bias Current		0.5	1.5	μA	$T_A = -55°C$
Input Resistance	40	100		KΩ	$T_A = -55°C$

ITT709 , ITT709-A
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

ELECTRICAL CHARACTERISTICS ITT709-5

(V_S = ±15V, T_A = 25°C unless otherwise specified)

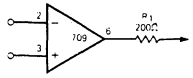
Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		2.0	7.5	mV	$R_S \leqslant 10K$, $\pm 9V \leqslant V_S \leqslant \pm 15V$
Input Offset Current		100	500	nA	
Input Bias Current		0.3	1.5	μA	
Input Resistance	50	250		KΩ	
Output Resistance		150		Ω	
Large-Signal Voltage Gain	15,000	45,000			$R_L \geqslant 2K$, V_{out} = ±10V
Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geqslant 10K$ $R_L \geqslant 2K$
Input Voltage Range	±8.0	±10		V	
Common Mode Rejection Ratio	65	90		db	$R_S \leqslant 10K$
Supply Voltage Rejection Ratio		25	200	μV/V	$R_S \leqslant 10K$
Power Consumption		80	200	mW	
Transient Response Risetime		0.3	1.0	μs	V_{in} = 20mV, R_L = 2KΩ, C_1 = 5000pF, R_1 = 1.5KΩ C_2 = 200pF, R_2 = 50Ω
Overshoot		10	30	%	$C_L \leqslant 100pF$

The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$

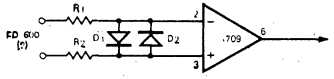
Input Offset Voltage			10	mV	$R_S \leqslant 10K$, $\pm 9V \leqslant V_S \pm 15V$
Input Offset Current			750	nA	
Input Bias Current			2.0	μA	
Large-Signal Voltage Gain	12,000				$R_L \geqslant 2K$, V_{out} = ±10V
Input Resistance	35			kΩ	

PROTECTION CIRCUITS

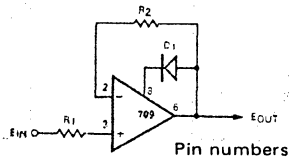
OUTPUT SHORT-CIRCUIT PROTECTION



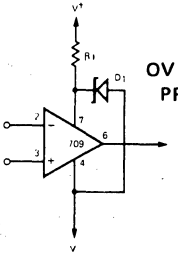
INPUT BREAKDOWN PROTECTION



LATCH-UP PROTECTION



SUPPLY OVERVOLTAGE PROTECTION



Pin numbers only apply to metal can package.

DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input teriminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

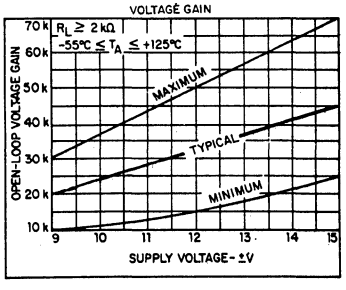
POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

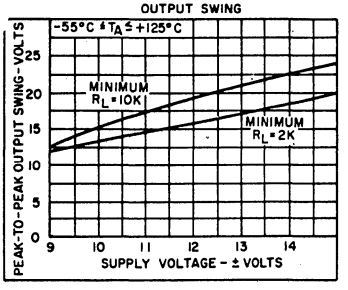
SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

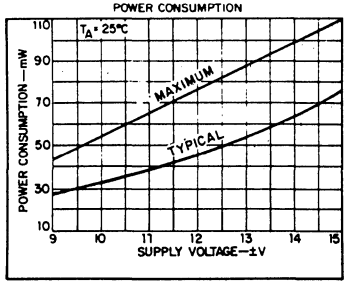
TRANSIENT RESPONSE—Te closed-loop step function response of the amplifier under small-signal conditions.

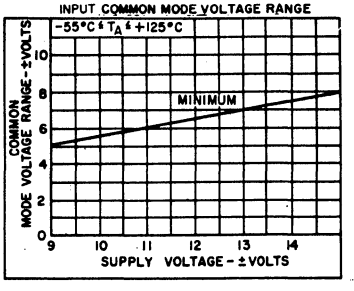
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

GUARANTEED ELECTRICAL CHARACTERISTICS ITT709-A



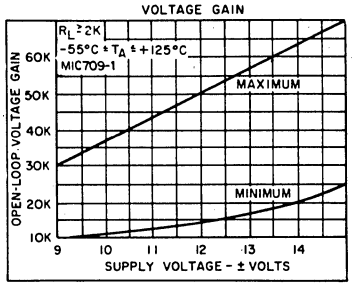


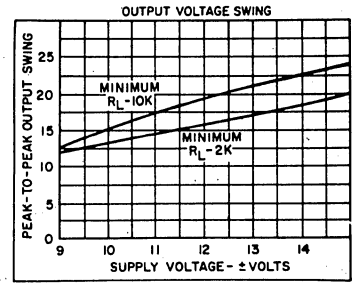


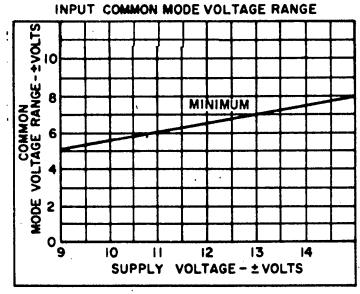


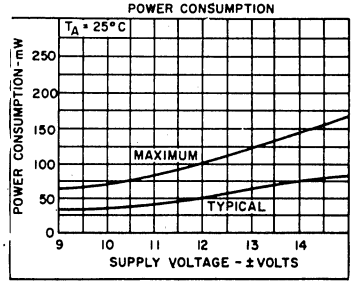
ITT709, ITT709-A
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

GUARANTEED ELECTRICAL CHARACTERISTICS ITT709-1

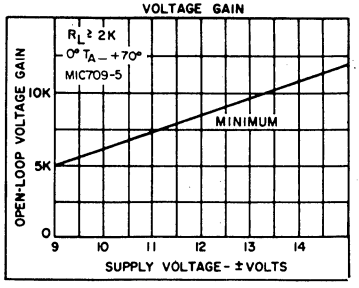


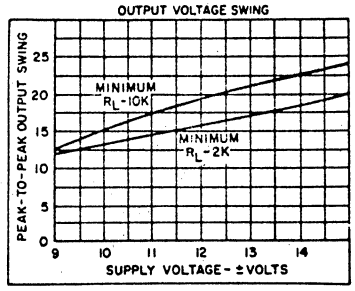


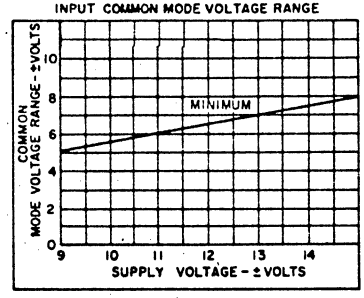




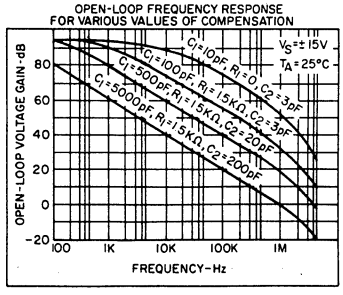
GUARANTEED ELECTRICAL CHARACTERISTICS ITT709-5

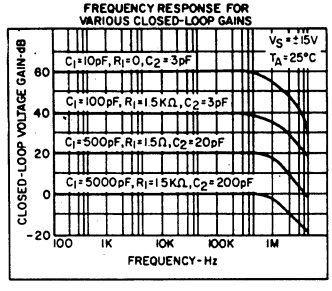


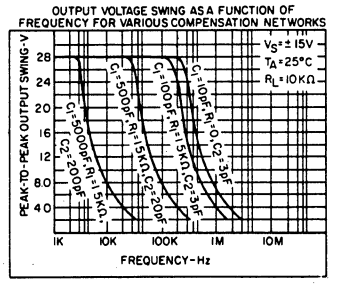




FREQUENCY COMPENSATION CURVES ITT709-A, ITT709-1, ITT709-5

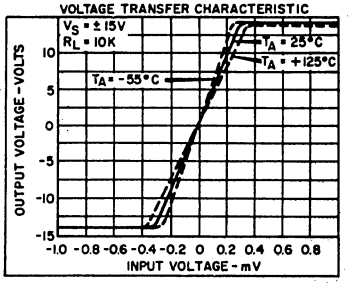




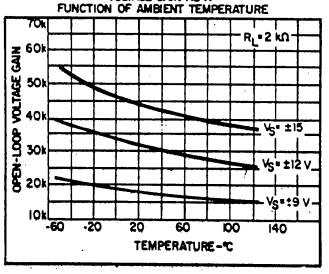


TYPICAL PERFORMANCE CURVES ITT709-A

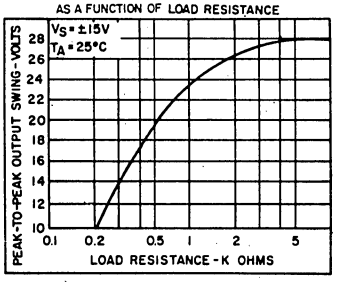
VOLTAGE TRANSFER CHARACTERISTIC



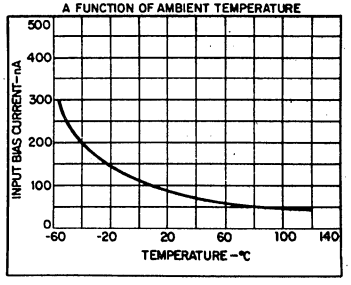
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



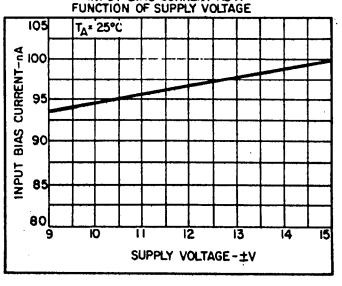
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



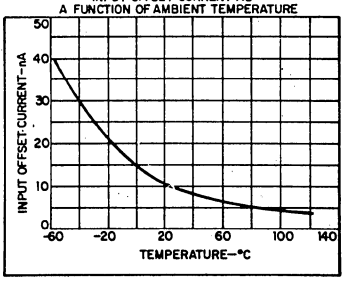
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



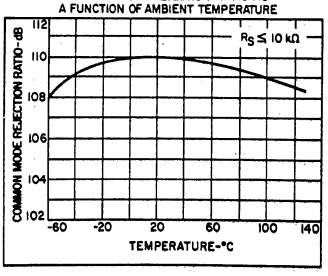
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



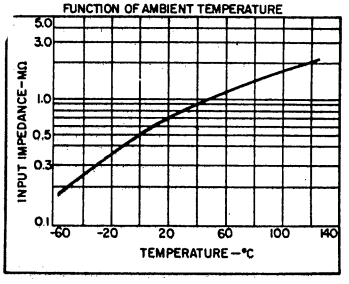
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



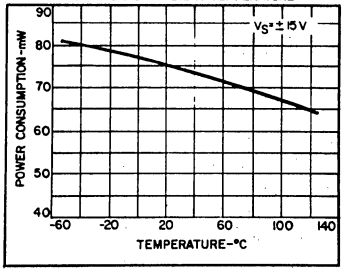
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



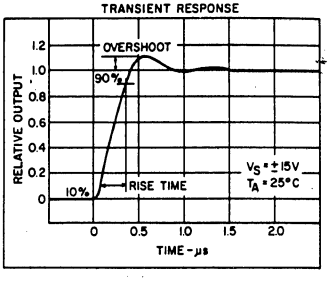
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



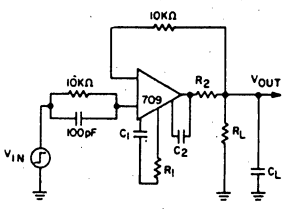
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



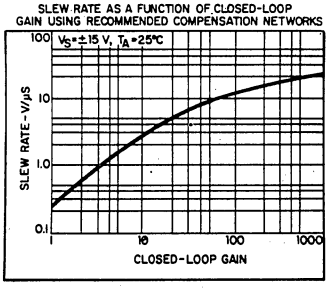
TRANSIENT RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



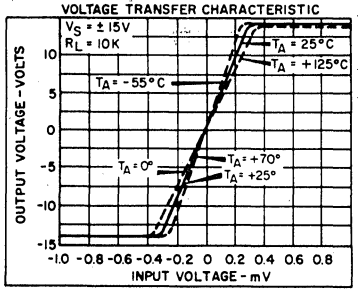
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



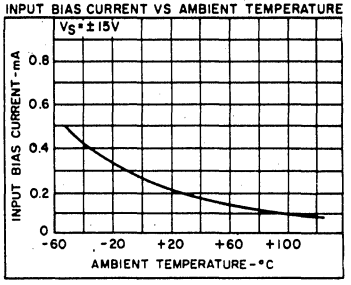
ITT709, ITT709-A
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

TYPICAL PERFORMANCE CURVES ITT709-1, ITT709-5

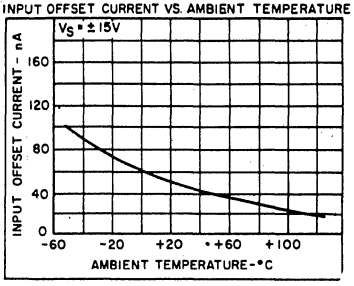
VOLTAGE TRANSFER CHARACTERISTIC



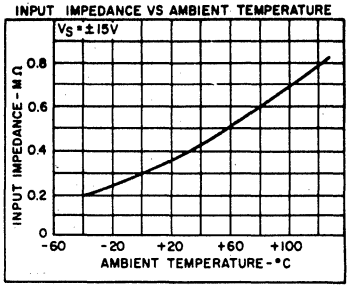
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



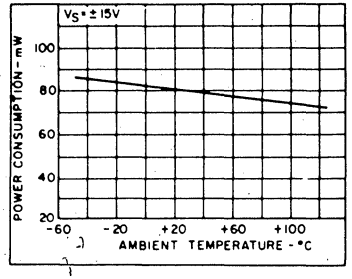
INPUT OFFSET CURRENT VS AMBIENT TEMPERATURE



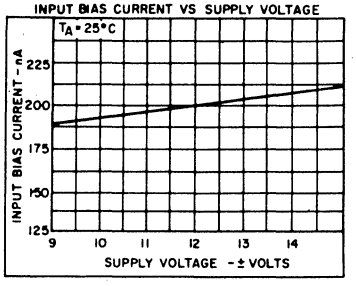
INPUT IMPEDANCE VS AMBIENT TEMPERATURE



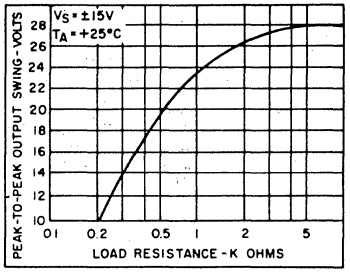
POWER CONSUMPTION VS AMBIENT TEMPERATURE



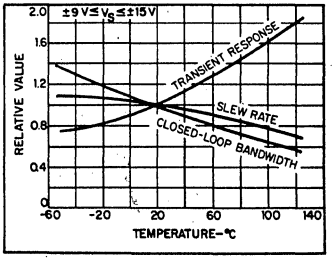
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



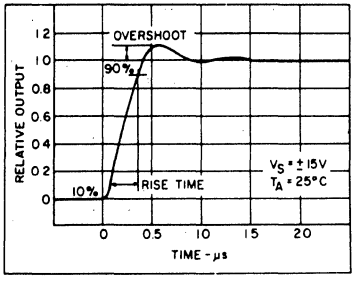
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



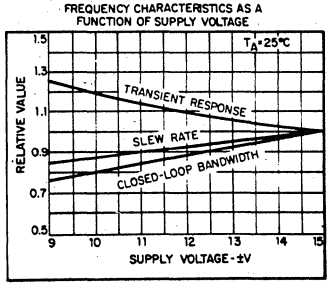
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



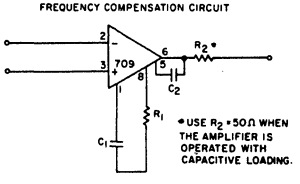
TRANSIENT RESPONSE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY COMPENSATION CIRCUIT



ITT SEMICONDUCTORS

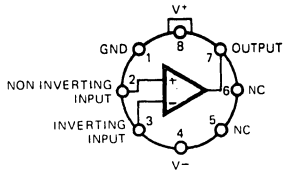
HIGH SPEED DIFFERENTIAL COMPARATOR

- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT710 is a differential voltage comparator which offers high accuracy and fast response times. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the ITT10 is compatible with all integrated logic forms. The ITT710 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.

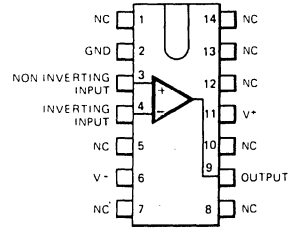
CONNECTION DIAGRAMS
(TOP VIEW)

8 LEAD METAL CAN

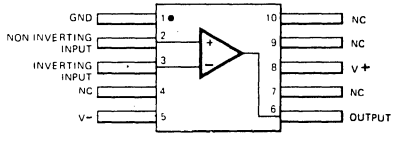


NOTE: PIN 4 CONNECTED TO CASE.

14 LEAD DIP



FLATPAK



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (ITT710-1 Note 1, ITT710-5 Note 2)	300mW
Operating Temperature Range	
ITT710-1	−55° to +125°C
ITT710-5	0° to 70°C
Storage Temperature Range	−65° to + 150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +105°C.

(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

ELECTRICAL CHARACTERISTICS for ITT710-1 (T_A=+25°C, V=12.0V, V=−6.0V unless otherwise specified)

PARAMETER (see definitions)	**Min.**	**Typ.**	**Max.**	**Units**	**CONDITIONS** (Note 4)
Input Offset Voltage		0.6	2.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Response Time (Note 3)		40		ns	
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$					
Input Offset Voltage			3.0	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		3.5	10	uV/°C	$R_S = 50\Omega$, TA=25°C to TA= +125°C
		2.7	10	uV/°C	$R_S = 50\Omega$, TA=25°C to TA= −55°C
Input Offset Current		0.25	3.0	uA	TA= +125°C
		1.8	7.0	uA	$T_A = -55°C$
Average Temperature Coefficient of Input Offset Current		5.0	25	nA/°C	T_A=25°C to T_A= +125°C
		15	75	nA/°C	T_A = 25°C to T_A = −55°C
Input Bias Current		27	45	uA	$T_A = -55°C$
Input Voltage Range	±5.0			V	V= −7.0V
Common Mode Rejection Ratio	80	100		dB	$R_S \leqslant 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \geqslant 5mV$, $O \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{IN} \geqslant 5mV$
Output Sink Current	0.5	1.7		mA	$T_A = +125°C$, $\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
	1.0	2.3		mA	$T_A = -55°C$, $\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

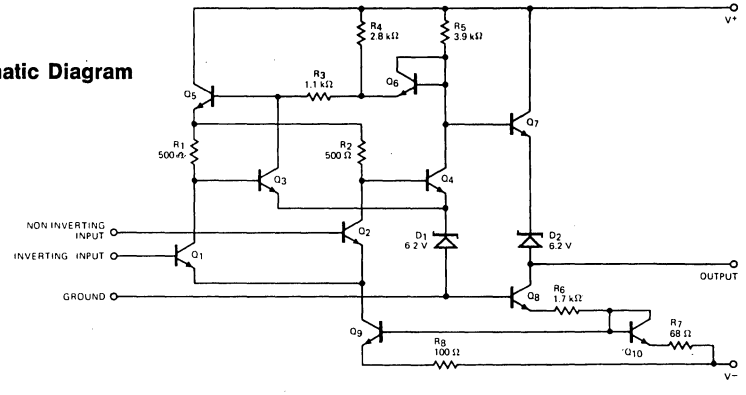
ELECTRICAL CHARACTERISTICS FOR ITT710-5 (TA=25°C, V=12.0V, V=−6.0V unless otherwise specified)

Parameter (see definitions)	Min.	Typ.	Max.	Units	Conditions (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Response Time (Note 3)		40		ns	

The following specifications apply for $0°C \leqslant TA \leqslant +70°C$:

Input Offset Voltage			6.5	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		5.0	20	uV/°C	$R_S=50\Omega$ TA=0°C to TA=+70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of Input Offset Current		15 24	50 100	nA/°C nA/°C	TA=25°C teo TA=+70°C TA=25°C to TA=0°C
Input Bias Current		25	40	uA	TA=0°C
Input Voltage Range	±5.0			V	V =−7.0V
Common Mode Rejection Ratio	70	98		dB	$R_S \leqslant 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \geqslant 5mV$, $0 \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqslant 5mV$
Output Sink Current	0.5			mA	$\Delta V_{IN} \geqslant 5mV$, $V_{out}=0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

Schematic Diagram



DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

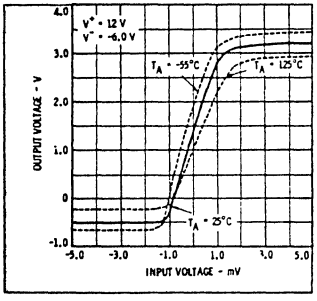
STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

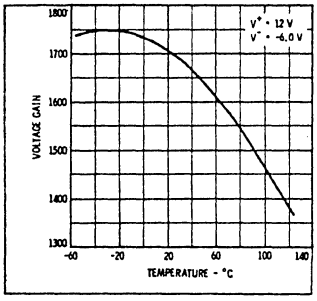
*These definitions apply for either side with the other disabled with the strobe.

TYPICAL CHARACTERISTICS ITT 710-1 (TA = 25°C. V = 12.0V. V = −6.0V unless otherwise specified)

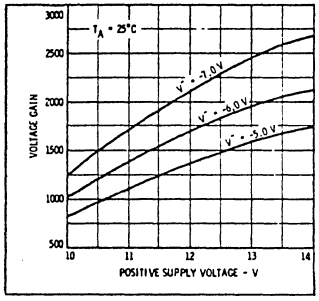
VOLTAGE TRANSFER CHARACTERISTIC



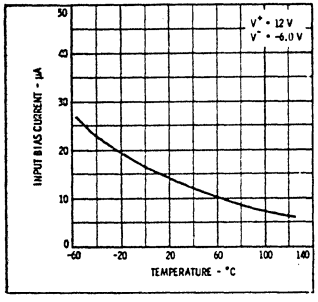
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



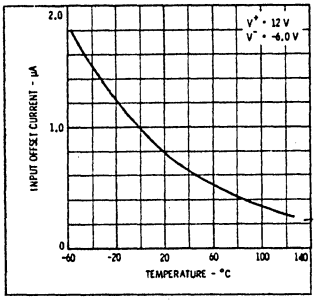
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



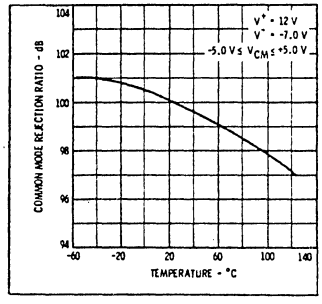
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



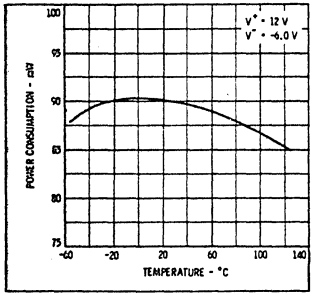
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



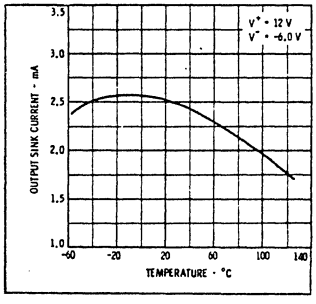
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



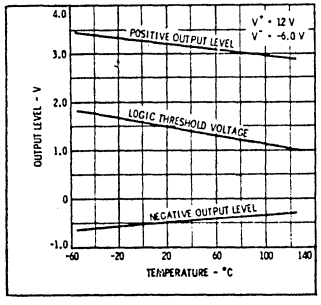
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

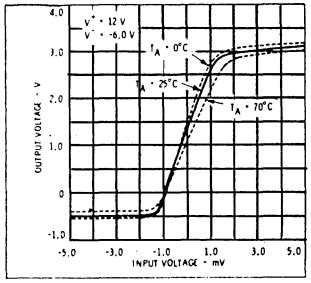


OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

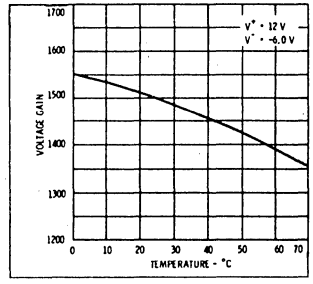


TYPICAL CHARACTERISTICS MIC 710-5 (TA = 25 C, V = 12.0V, V = −6.0V unless otherwise specified)

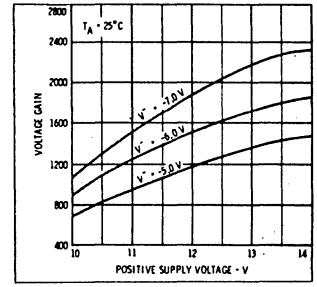
VOLTAGE TRANSFER CHARACTERISTIC



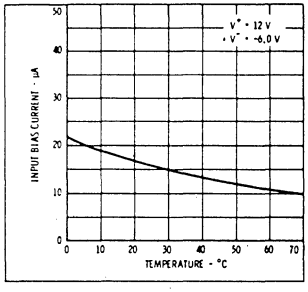
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



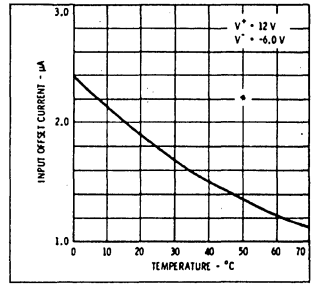
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



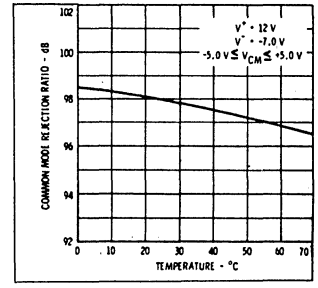
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



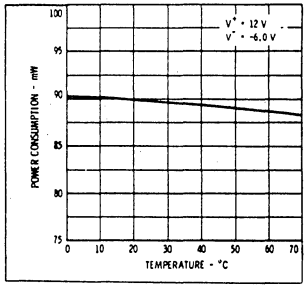
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



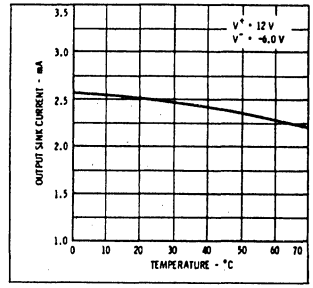
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



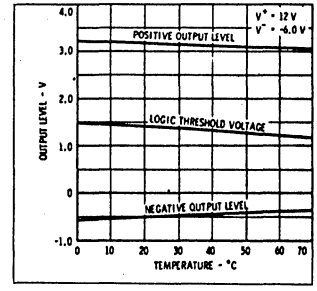
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



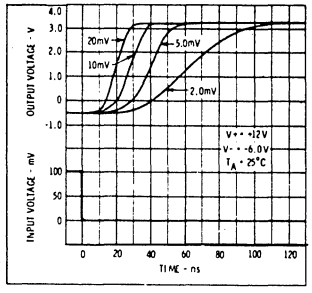
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



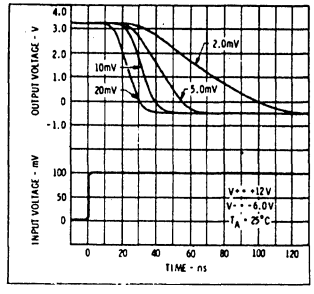
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



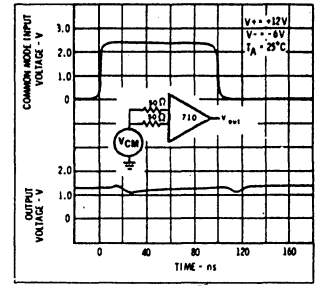
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

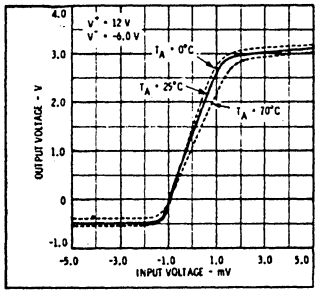


COMMON MODE PULSE RESPONSE

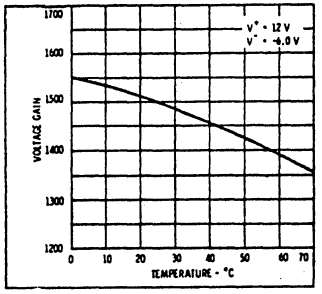


TYPICAL CHARACTERISTICS ITT 710-5 (TA= +25°C, V=12.0V, V= −6.0V unless otherwise specified)

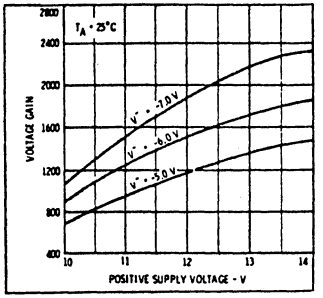
VOLTAGE TRANSFER CHARACTERISTIC



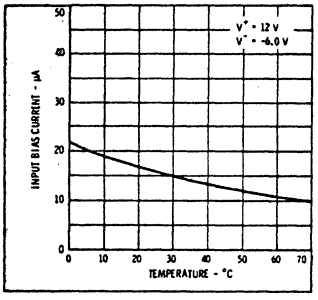
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



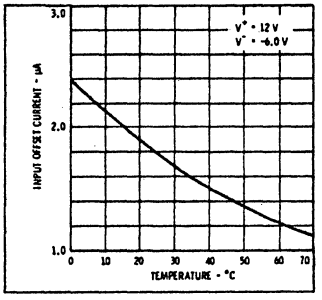
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



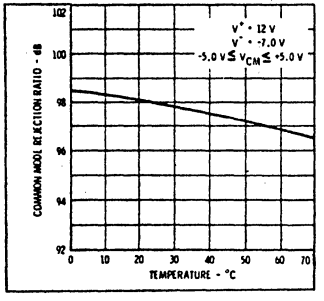
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



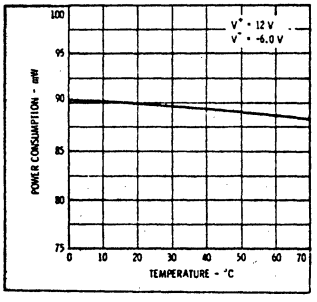
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



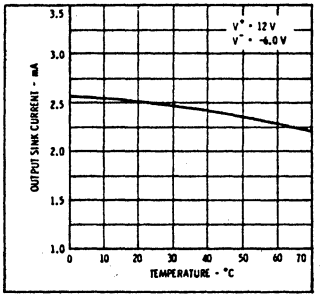
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



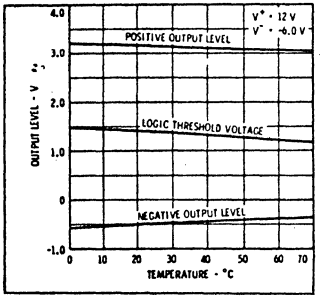
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



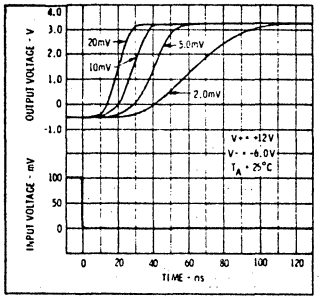
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



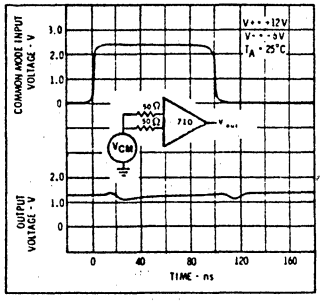
TYPICAL CHARACTERISTICS ITT 710-1, ITT 710-5

(TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

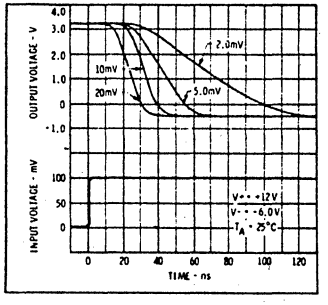
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



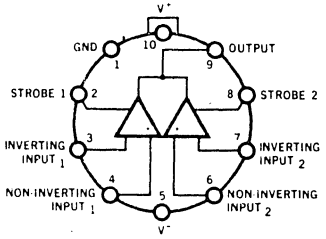
DUAL COMPARATOR

- **High Accuracy**
- **Fast Response Time**
- **Large Input Voltage Range**
- **Low Power Consumption**

The ITT711 is a dual differential voltage comparator. It was primarily designed for core-memory sense amplifiers which require high accuracy, fast response times, large input voltage range, and low power consumption. The output voltage is compatible with most integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Each comparator channel is provided with independent strobing. Pulse stretching on the output is easily accomplished. Double-ended detection for automatic GO/NO-GO test equipment and pulse height detection (window discriminator) are additional applications of the dual comparator. The entire circuit is contained on a silicon chip and is manufactured using ITT Planar Epitaxial process.

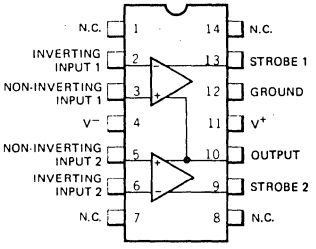
CONNECTION DIAGRAMS
(TOP VIEW)

10 LEAD METAL CAN

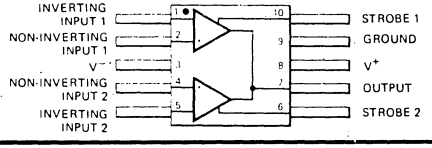


Note. Pin 5 connected to case.

14 LEAD DIP



10 LEAD FLATPAK



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Positive Supply Voltage	+14.0V
Negative Supply Voltage	—7.0V
Peak Output Current	50mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (ITT711-1 Note 1, ITT711-5 Note 2)	300 mW
Operating Temperature Range	
ITT711-1	—55° to +125°C
ITT711-5	0° to +50°C
Storage Temperature Range	—65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

1. Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

2. Rating applies for ambient temperatures to +70°C.

3. The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

4. The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

5. The input offset voltage is specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

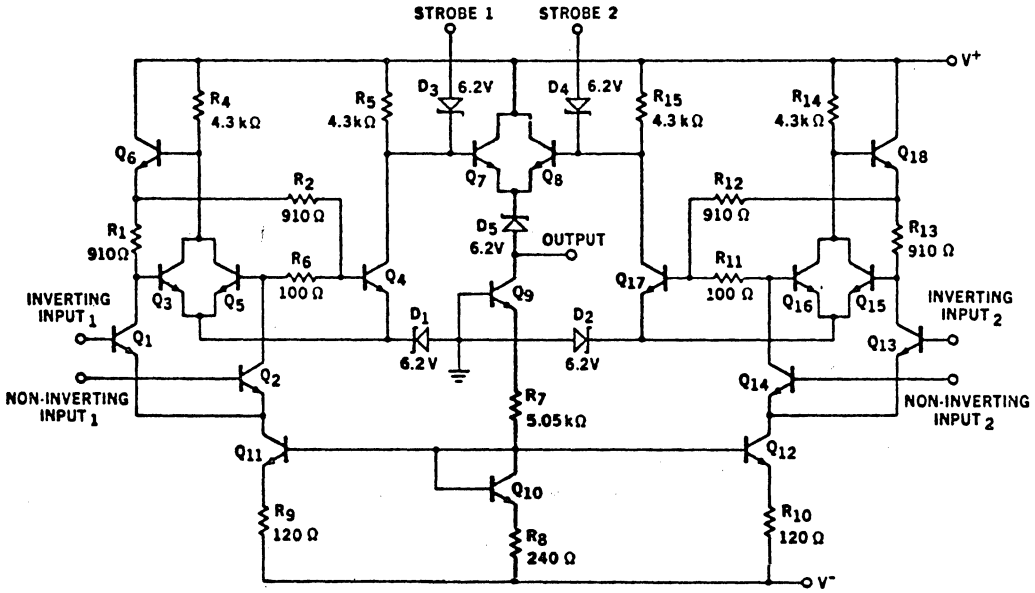
ELECTRICAL CHARACTERISTICS FOR ITT711-1 (T_A=25°C, V+=12.0V, V−=—6.0V unless otherwise specified)

PARAMETER (see definitions)	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	3.5	mV	V_{out} = +1.4V, $R_S \leqslant 200\Omega$, V_{CM} = O
		1.0	5.0	mV	V_{out} = +1.4V, $R_S \leqslant 200\Omega$,
Input Offset Current		0.5	10.0	uA	V_{out} = +1.4V
Input Bias Current		25	75	uA	
Voltage Gain	750	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	V− = −7.0V
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	$V_{in} \geqslant 10mV$,
Loaded Positive Output Level	2.5	3.5		V	$V_{in} \geqslant 10mV$, I_0 = 5mA
Negative Output Level	−1.0	—0.5	0	V	$V_{in} \geqslant 10mV$,
Strobed Output Level	−1.0		0	V	$V_{strobe} \leqslant 0.3V$
Output Sink Current	0.5	0.8		mA	$V_{in} \geqslant 10mV$, $V_{out} \geqslant 0$
Strobe Current		1.2	2.5	mA	V_{strobe} = 100mV
Positive Supply Current		8.6		mA	$V_{out} \leqslant 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	200	mW	

The following specifications apply for $-55°C \leqslant T \leqslant 125°C$:

Input Offset Voltage (Note 4)			4.5	mV	$R_S \leqslant 200\Omega$, V_{CM} = O
			6.0	mV	$R_S \leqslant 200\Omega$,
Input Offset Current (Note 4)			20	uA	
Input Bias Current			150	uA	
Temperature Coefficient of		5.0		uV/°C	
Input Offset Voltage					
Voltage Gain	500				

Schematic Diagram



ELECTRICAL CHARACTERISTICS FOR ITT711-5 (T_A=25°C, V+=12.0V, V—= −6.0V unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	5.0	mV	V_{out}=+1.4V,R_s≤200Ω, V_{CM}=0
		1.0	7.5	mV	V_{out}=+1.4V,R_s≤200Ω,
Input Offset Current		0.5	15	uA	V_{out}=+1.4V
Input Bias Current		25	100	uA	
Voltage Gain	700	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	V− = −7.0V
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	V_{in}≥10mV
Loaded Positive Output Level	2.5	3.5		V	V_{in}≥10mV, I_Q=5mA
Negative Output Level	—1.0	−0.5	0	V	V_{in}≥10mV
Strobed Output Level	−1.0		0	V	V_{strobe}≤0.3V
Output Sink Current	0.5	0.8		mA	V_{in}≥10mV, V_{out}≥0

ELECTRICAL CHARACTERISTICS FOR ITT711-5 (T_A=25°C, V+=12.0V, V—= −6.0V unless otherwise specified) **(continued)**

Parameter	Min.	Typ.	Max.	Units	Conditions
Strobe Current		1.2	2.5	mA	V_{strobe}=100mV
Positive Supply Current		8.6		mA	$V_{out} \leqslant 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	230	mW	

The following specifications apply for 0°C$\leqslant$T $\leqslant$+70°C:

Input Offset Voltage (Note 5)			6.0 10	mV mV	$R_S \leqslant 200\Omega$, V_{CM}=0 $R_S \leqslant 200\Omega$
Input Offset Current (Note 5)			25	uA	
Input Bias Current			150	uA	
Temperature Coefficient of Input Offset Voltage		5.0		uV/°C	
Voltage Gain	500				

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage on the strobe terminal equal to or less than a minimum specified amount.

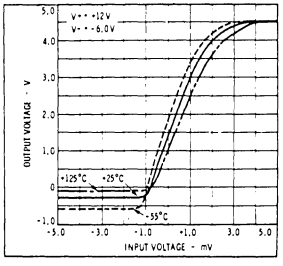
STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

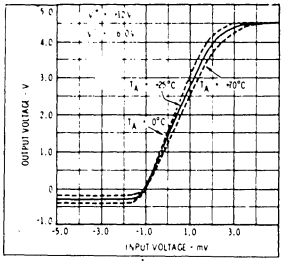
TYPICAL PERFORMANCE CURVES ITT711-1

VOLTAGE TRANSFER CHARACTERISTIC



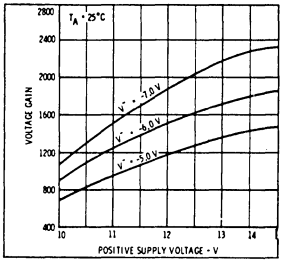
TYPICAL PERFORMANCE CURVES ITT711-5

VOLTAGE TRANSFER CHARACTERISTIC

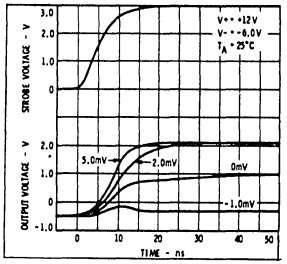


TYPICAL PERFORMANCE CURVES

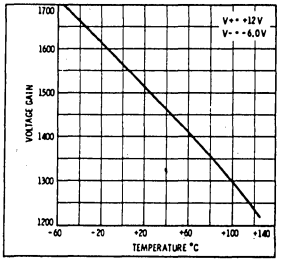
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



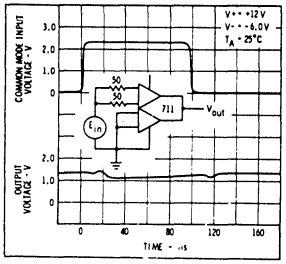
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



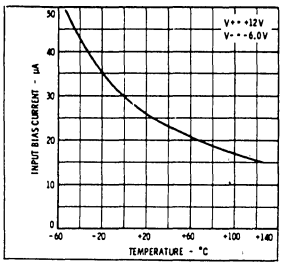
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



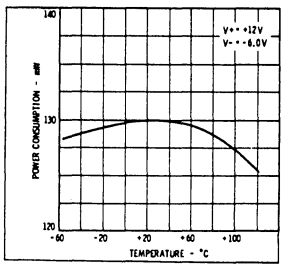
COMMON MODE PULSE RESPONSE



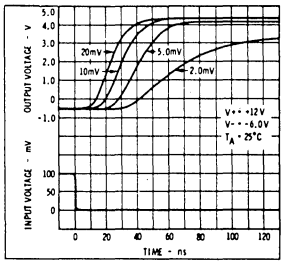
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



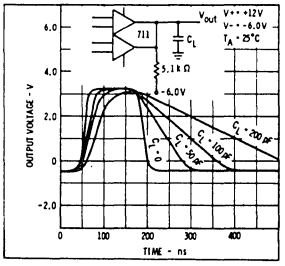
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



ITT SEMICONDUCTORS

HIGH-GAIN WIDEBAND DC AMPLIFIER

- **Low Offset Voltage**
- **High Voltage Gain**
- **Low Offset Voltage Drift**

The ITT712 is a general purpose amplifier for use as an operational amplifier in high speed analog computers, a precision instrumentation amplifier or in other applications requiring a feedback amplifier capable of operating within the frequency ranges of DC to as high as 30MHz. The ITT712 amplifier achieves low DC offset and low thermal drift, wideband operation and low power consumption as a result of ITT Planar epitaxial manufacturing process.

Absolute Maximum Ratings
Characteristics **Units**

Voltage between V+ and V— terminals ..... ±21 Volts
Internal Power Dissipation (TO-5) 300mW
(ITT712-1 note 1,
ITT712-5 note 2)
Differential Input Voltage ..... ±5.0 Volts
Input Voltage .....+1.5 to —6.0 Volts
Peak Output Voltage 50mA
Storage Temperature Range ..—65 to +150°C
Operating Temperature Range
ITT 712-1 .....—55 to +125°C
ITT712-5 .....0 to +70°C
Lead Temperature
(Soldering, 60 sec.) .....300°C

NOTES:

1. Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

2. Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS for ITT712-1

Parameter (See definitions)	Min.	Typ	Max.	Min.	Typ	Max	Units	Conditions
	V+ = 12.0V, V− = 6.0V			V+ = 6.0V, V− = —3.0V				
Input Offset Voltage		0.5	2.0		0.7	3.0	mV	$R_S \leqslant 2k\Omega$
Input Offset Current		180	500		120	500	nA	
Input Bias Current		2.0	5.0		1.2	3.5	uA	
Input Resistance	16	40		22	67		kΩ	
Input Voltage Range	−4.0		+0.5	—1.5		+0.5	V	
Common Mode Rejection Ratio	80	100		80	100		dB	$R_S \leqslant 2k\Omega$, $f \leqslant 1kHz$
Large Signal Voltage Gain	2500	3600	6000	600	900	1500		$R_L \geqslant 100k\Omega$, $V_{out} = \pm 5.0V$ $R_L \geqslant 100k\Omega$, $V_{out} = \pm 2.5V$
Output Resistance		200	500		300	700	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		10	30	mW	$V_{out} = 0$

ELECTRICAL CHARACTERISTICS for ITT712-1 (continued)

Parameter (See definitions)	Min.	Typ.	Max.	Min.	Typ.	Max	Units	Conditions
	V+ = 12.0V, V− = 6.0V			V+ = 6.0V, V− = −3.0V				
Transient Response (Unity-Gain) Rise Time		25	120				ns	C_L=0.01 uF, R_L=20Ω $R_L \geq$100kΩ, V_{in}=10mW
Overshoot		10	50				%	$C_L \leq$100pF
Transient Response (x100 gain) Risetime		10	30				ns	C_3=50pF, $R_L \geq$100kΩ V_{in}=1 mV
Overshoot		20	40				%	

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Input Offset Voltage			3.0			4.0	mV	$R_s \leq 2k\Omega$
Average Temperature Coefficient of Input		2.5	10		3.5	15	uV/°C	R_s=50Ω T_A=25°C to T_A=+125°C
Offset Voltage		2.0	10		3.0	15	uV/°C	R_S=50Ω T_A=25°C to T_A=−55°C
Input Offset Current		80 400	500 1500		50 280	500 1500	nA nA	T_A=+125°C T_A=−55°C
Average Temperature Coefficient of Input Offset Current		1.0 3.0	5.0 16		0.7 2.0	4.0 13	nA/°C nA/°C	T_A=25°C to T_A=+125°C T_A=25°C to T_A=−55°C
Input Bias Current		4.3	10		2.6	7.5	μA	T_A=55°C
Input Resistance	6.0			8.0			kΩ	
Common Mode Rejection Ratio	70	95		70	95		dB	$R_s \leq 2k\Omega$, f≤1kHz
Supply Voltage Rejection Ratio		75	200		75	200	uV/V	V+=12V, V−=−6Vto V+=6V, V−=−3V $R_s \leq 2k\Omega$
Large Signal Voltage Gain	2000		7000	500		1750		$R_L \geq$100KΩ, V_{out}=±5.0V $R_L \geq$100kΩ, V_{out}=±2.5V
Output Voltage Swing	±5.0 ±3.5	±5.3 ±4.0			±2.5 ±1.5	±2.7 ±2.0	V V	$R_L \geq$100kΩ $R_L \geq$10kΩ
Supply Current		4.4 5.0	6.7 7.5		1.7 2.1	3.3 3.9	mA mA	T_A=+125°C, V_{out}=0 T_A=−55°C, V_{out}=0
Power Consumption		80 90	120 135		15 19	30 35	mW mW	T_A=+125°C, V_{out}=0 T_A=−55°C, V_{out}=0

ELECTRICAL CHARACTERISTICS for ITT712-5

Parameter (see definitions)	V+ = 12.0V, V− = 6.0V Min.	Typ.	Max.	V+ = 6.0V, V− = −3.0V Min.	Typ.	Max	Units	Conditions
The following specifications apply for T_A = 25°C								
Input Offset Voltage		1.5	5.0		1.7	6.0	mV	$R_S \leq 2K\Omega$
Input Offset Current		0.5	2.0		0.3	2.0	μA	
Input Bias Current		2.5	7.5		1.5	5.0	μA	
Input Resistance	10	32		16	55		KΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	70	92		70	92		dB	$R_S \leq 2K\Omega$, f ≤ 1KHz
Large Signal Voltage Gain	2000	3400	6000					$R_L \geq 100$ KΩ $V_{out} = \pm 5.0$ V
				500	800	1500		$R_L \geq 100$ KΩ $V_{out} = \pm 2.5$ V
Output Resistance		200	600		300	800	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		19	30	mW	$V_{out} = 0$
Transient Response (unity gain)								$C_I = 0.01$ μF, $R_I = 20\Omega$ $R_L \leq 100$ KΩ $V_{in} = 10$ mV
Risetime		25	120				ns	
Overshoot		10	50				%	$C_L \leq 100$ pF
Transient Response (X100 gain)								$C_3 = 50$ pF $R_L \geq 100$ KΩ $V_{in} = 1$ mV
Risetime		10	30				ns	
Overshoot		20	40				%	
The following specifications apply for 0°C T_A +70°C								
Input Offset Voltage			6.5			7.5	mV	$R_S \leq 2$ KΩ
Average Temperature Coefficient of Input Offset Voltage		5.0	20		7.5	25	μV/°C	$R_S = 50\Omega$ $T_A = +70$°C to $T_A = 0$°C
Input Offset Current			2.5			2.5	μA	
Average Temperature Coefficient of Input Offset Current		4.0 6.0	10 20		3.0 5.5	8.0 18	nA/°C nA/°C	$T_A = 25$°C to $T_A = +70$°C $T_A = 25$°C to $T_A = 0$°C

ELECTRICAL CHARACTERISTICS for ITT712-5 (continued)

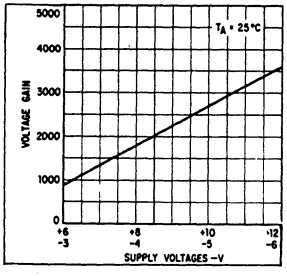
Parameter (see definitions)	V+ =12.0V, V− =6.0V Min.	Typ.	Max.	V+ =6.0V, V− =−3.0V Min.	Typ.	Max	Units	Conditions
The following specifications apply for T_A=25°C								
Input Offset Voltage		1.5	5.0		1.7	6.0	mV	$R_S \leq 2K\Omega$
Input Offset Current		0.5	2.0		0.3	2.0	μA	
Input Bias Current		2.5	7.5		1.5	5.0	μA	
Input Resistance	10	32		16	55		KΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	70	92		70	92		dB	$R_S \leq 2K\Omega$, f≤1KHz
Large Signal Voltage Gain	2000	3400	6000					$R_L \geq 100$ KΩ $V_{out} = \pm 5.0$ V
				500	800	1500		$R_L \geq 100$ KΩ $V_{out} = \pm 2.5$ V
Output Resistance		200	600		300	800	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	V_{out}=0
Power Consumption		90	120		19	30	mW	V_{out}=0
Transient Response (unity gain) Risetime		25	120				ns	C_I=0.01 μF, R_I=20Ω $R_L \leq 100$ KΩ V_{in}=10 mV
Overshoot		10	50				%	$C_L \leq 100$ pF
Transient Response (X100 gain) Risetime		10	30				ns	C_3=50 pF $R_L \geq 100$ KΩ V_{in}=1 mV
Overshoot		20	40				%	
The following specifications apply for 0°C T_A+70°C								
Input Offset Voltage			6.5			7.5	mV	$R_S \leq 2$ KΩ
Average Temperature Coefficient of Input Offset Voltage		5.0	20		7.5	25	μV/°C	R_S=50Ω T_A=+70°C to T_A=0°C
Input Offset Current			2.5			2.5	μA	
Average Temperature		4.0	10		3.0	8.0	nA/°C	T_A=25°C to T_A=+70°C
Coefficient of Input		6.0	20		5.5	18	nA/°C	
Offset Current								T_A=25°C to T_A=0°C

ELECTRICAL CHARACTERISTICS for ITT712-5 (continued)

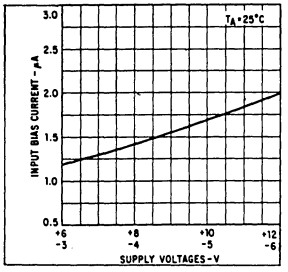
Parameter (see definitions)	V+ =12.0V, V− =6.0V Min.	Typ.	Max.	V+ =6.0V, V− =−3.0V Min.	Typ.	Max	Units	Conditions
Input Bias Current		4.0	12		2.7	8	μA	T_A=0°C
Input Resistance	6.0	18		9.0	27		KΩ	
Common Mode Rejection Ratio	65	86		65	86		dB	$R_S \leq 2K\Omega, f \leq 1$ KHz
Supply Voltage Rejection Ratio		90	300		90	300	μV/V	V+ =12V,V− =−6V to V+ =6V,V− =−3V $R_S \leq 2$ KΩ
Large Signal Voltage Gain	1500		7000	400		1750		$R_L \geq 100$ KΩ V_{out} = ±5.0V $R_L \geq 100$KΩ V_{out} = ±2.5V
Output Voltage Swing	±5.0 ±3.5	±5.3 ±4.0			±2.5 ±1.5	±2.7 ±2.0	V V	$R_L \geq 100$ KΩ $R_L \geq 10$ KΩ
Supply Current		5.0	7.0		2.1	3.9	mA	V_{out}=0
Power Consumption		90	125		19	35	mW	

TYPICAL PERFORMANCE CURVES ITT712-1, 712-5

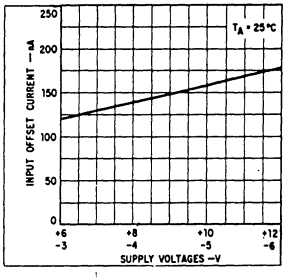
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



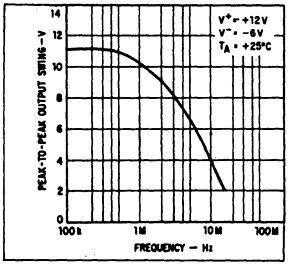
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



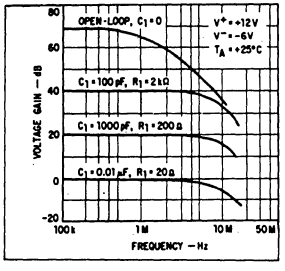
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



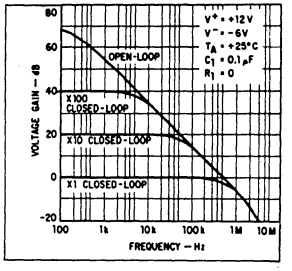
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)

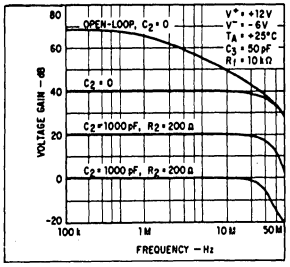


FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK

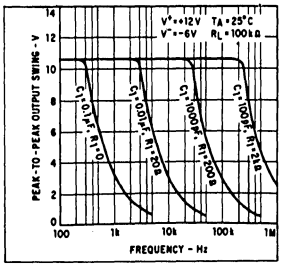


TYPICAL PERFORMANCE CURVES ITT712-1, 712-5 (continued)

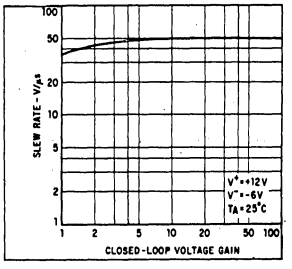
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



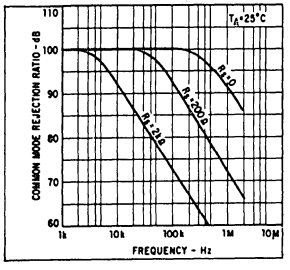
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



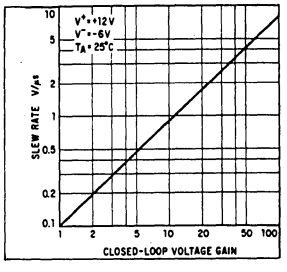
SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



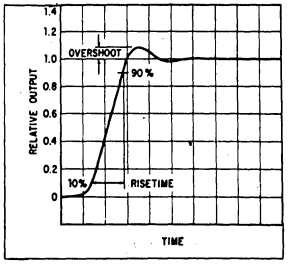
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

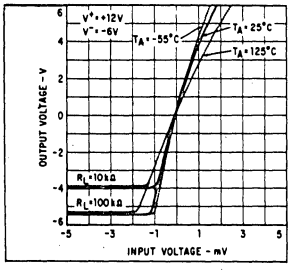


TRANSIENT RESPONSE

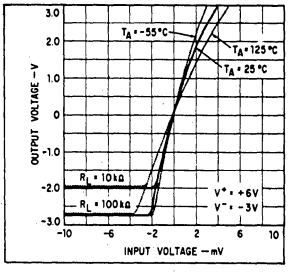


ELECTRICAL CHARACTERISTICS for ITT712-1

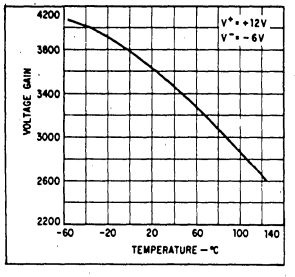
VOLTAGE TRANSFER CHARACTERISTIC



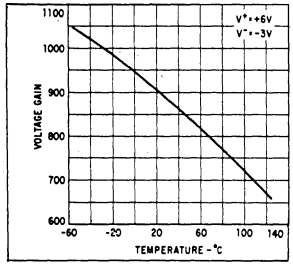
VOLTAGE TRANSFER CHARACTERISTIC



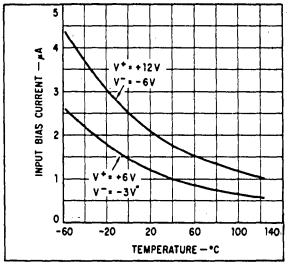
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



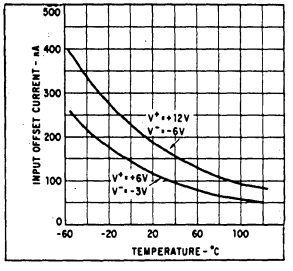
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

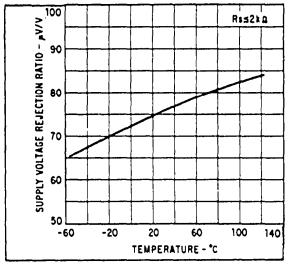


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

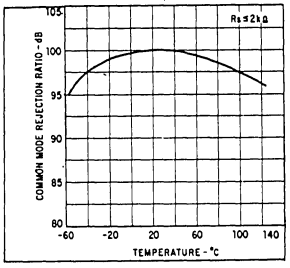


TYPICAL PERFORMANCE CURVES ITT712-1 (continued)

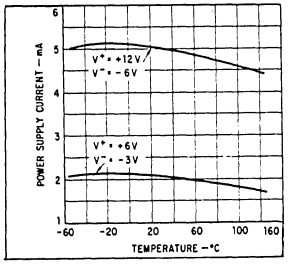
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



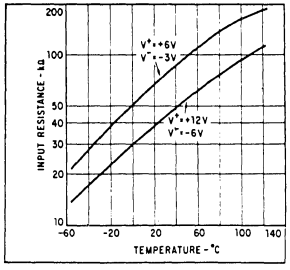
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



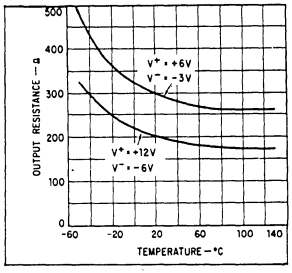
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



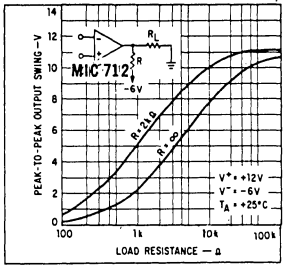
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

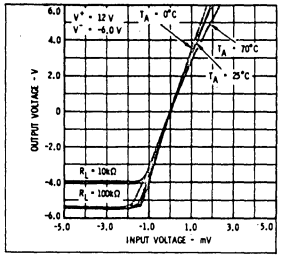


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

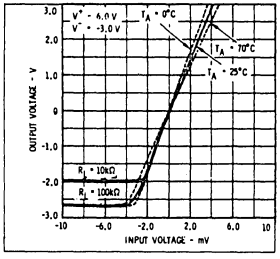


TYPICAL PERFORMANCE CURVES ITT712-5 (continued)

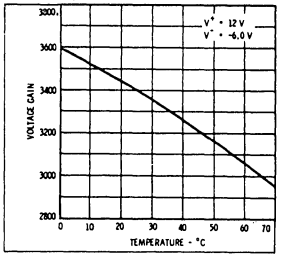
VOLTAGE TRANSFER CHARACTERISTIC



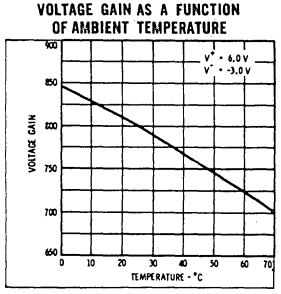
VOLTAGE TRANSFER CHARACTERISTIC



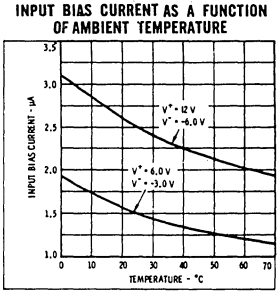
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



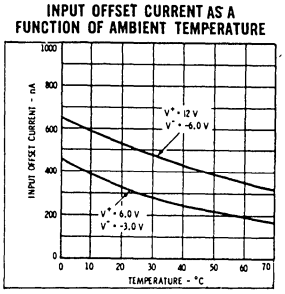
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

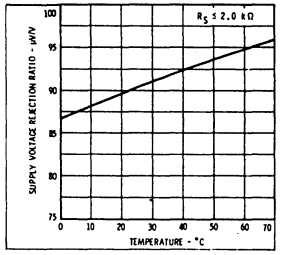


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

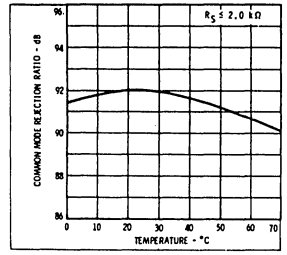


TYPICAL PERFORMANCE CURVES ITT712-5 (continued)

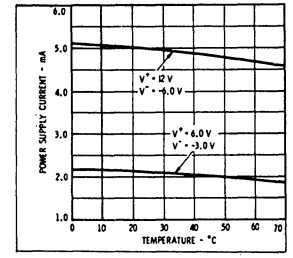
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



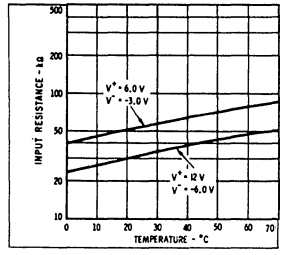
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



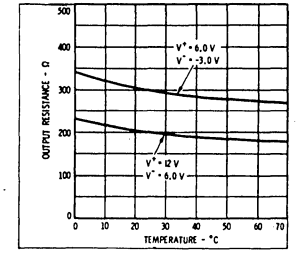
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



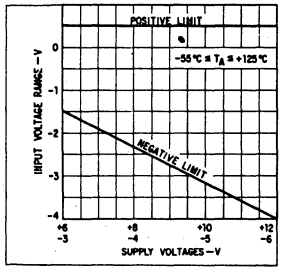
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



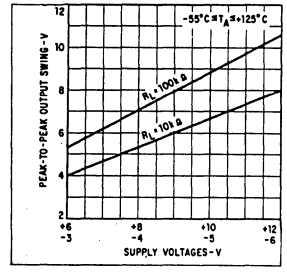
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



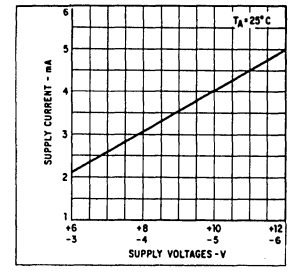
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES

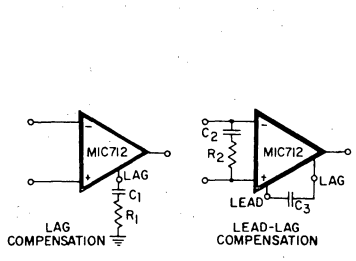


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES

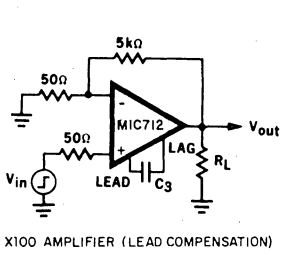


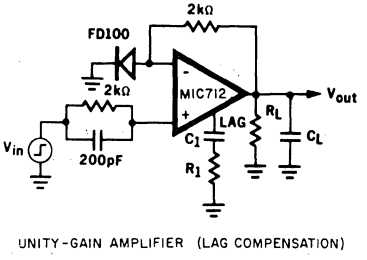
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



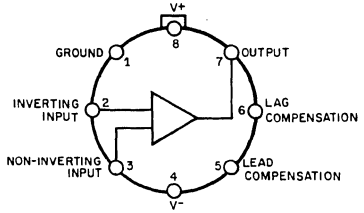


Frequency Compensation Circuits



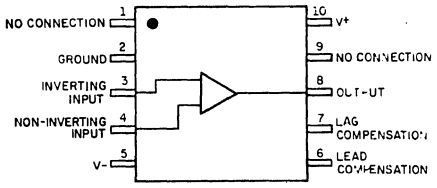


Transient Response Test Circuits

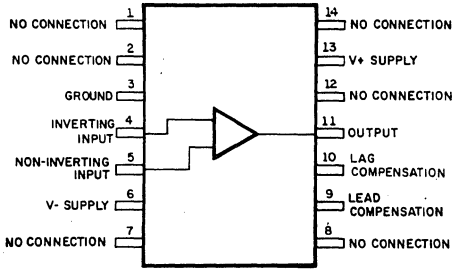


NOTE: PIN 4 CONNECTED TO CASE

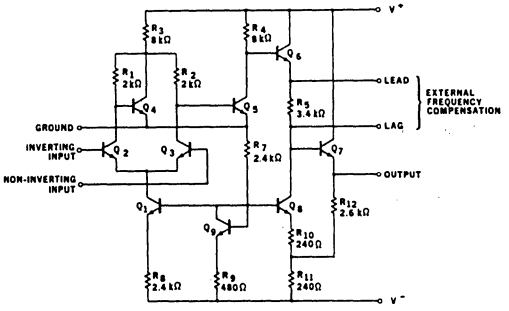
FLAT PACK (Top View)



DUAL IN-LINE



Connection Diagrams



Schematic Diagram

DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input teriminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE—Te closed-loop step function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

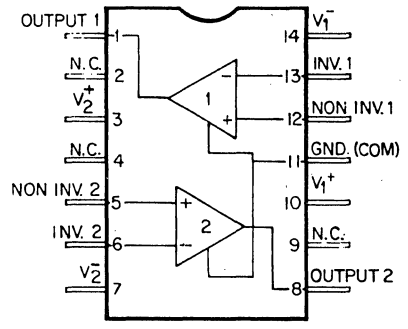
ITT SEMICONDUCTORS

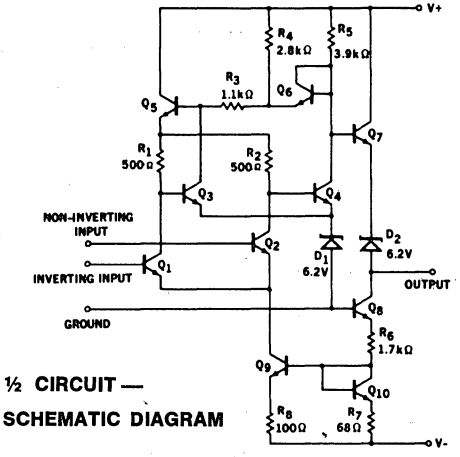
DUAL HIGH SPEED DIFFERENTIAL COMPARATOR

- **Better Temperature Tracking**
- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT720 differential voltage dual comparator, offering high accuracy and fast response consists of two separate ITT710 high speed differential comparators. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the ITT720 is compatible with all integrated logic forms. The ITT720 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.

CONNECTION DIAGRAM





½ CIRCUIT — SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation	300 mV
(ITT720-1 Note 1, ITT720-5 Note 2)	200 mW
Operating Temperature Range	
ITT720-1	−55° to + 125°C
ITT720-5	0° to +70°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +105°C.

(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

ITT720
DUAL HIGH SPEED DIFFERENTIAL COMPARATOR

ELECTRICAL CHARACTERISTICS FOR ITT720-1 (T=+25°C, V=12.0V, V=−6.0V unless otherwise specified)

PARAMETER (see definitions)	**Min.**	**Typ.**	**Max.**	**Units**	**CONDITIONS** (Note 4)
Input Offset Voltage		0.6	2.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Response Time (Note 3)		40		ns	

The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$

Input Offset Voltage			3.0	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		3.5	10	uV/°C	$R_S = 50\Omega$, TA=25°C to TA= +125°C
		2.7	10	uV/°C	$R_S = 50\Omega$, TA=25°C to TA= −55°C
Input Offset Current		0.25	3.0	uA	TA= +125°C
		1.8	7.0	uA	T_A = −55°C
Average Temperature Coefficient of Input Offset Current		5.0	25	nA/°C	T_A=25°C to T_A= +125°C
		15	75	nA/°C	T_A = 25°C to T_A = −55°C
Input Bias Current		27	45	uA	T_A = −55°C
Input Voltage Range	±5.0			V	V= −7.0V
Common Mode Rejection Ratio	80	100		dB	$R_S \leqslant 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \geqslant 5mV$, $O \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{IN} \geqslant 5mV$
Output Sink Current	0.5	1.7		mA	T_A = +125°C, $\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
	1.0	2.3		mA	T_A = −55°C, $\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

ELECTRICAL CHARACTERISTICS FOR .ITT720-5 (TA=25°C, V=12.0V, V=−6.0V unless otherwise specified)

Parameter (see definitions)	Min.	Typ.	Max.	Units	Conditions (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Response Time (Note 3)		40		ns	

The following specifications apply for $0°C \leqslant TA \leqslant +70°C$:

Input Offset Voltage			6.5	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of		5.0	20	uV/°C	$R_S=50\Omega$, TA=0°C to TA=+70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of		15	50	nA/°C	TA=25°C to TA=+70°C
Input Offset Current		24	100	nA/°C	TA=25°C to TA=0°C
Input Bias Current		25	40	uA	TA=0°C
Input Voltage Range	±5.0			V	V =−7.0V
Common Mode Rejection Ratio	70	98		dB	$R_S \leqslant 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \geqslant 5mV$, $O \leqslant I_{out} \leqslant 5.mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqslant 5mV$
Output Sink Current	0.5			mA	$\Delta V_{in} \geqslant 5mV$, $V_{out}=0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

ITT720
DUAL HIGH SPEED DIFFERENTIAL COMPARATOR

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage on the strobe terminal equal to or less than a minimum specified amount.

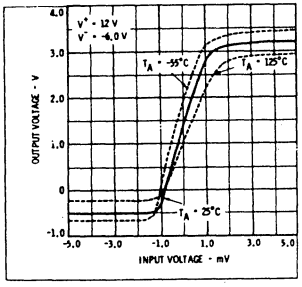
STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

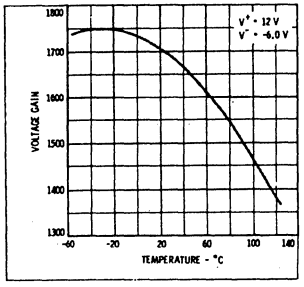
*These definitions apply for either side with the other disabled with the strobe.

TYPICAL CHARACTERISTICS ITT720-1 (T = +25°, V=12.0V. V= −6.0V unless otherwise specified)

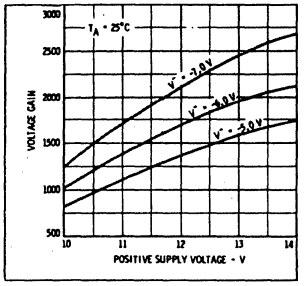
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

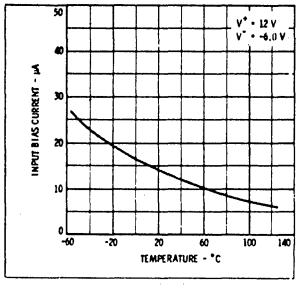


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

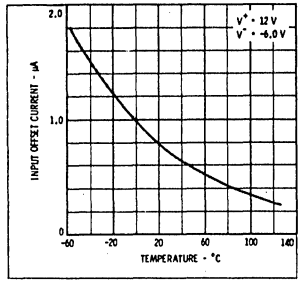


TYPICAL CHARACTERISTICS ITT720-1 ($T = +25°$, $V=12.0V$. $V= -6.0V$ unless otherwise specified) **(continued)**

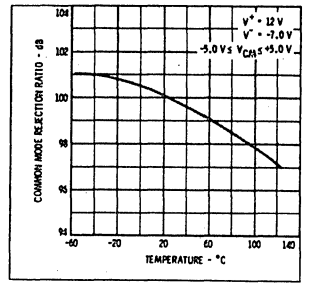
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



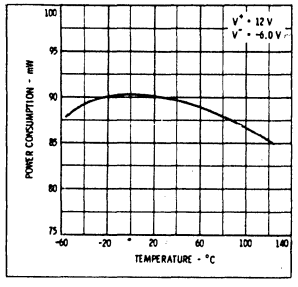
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



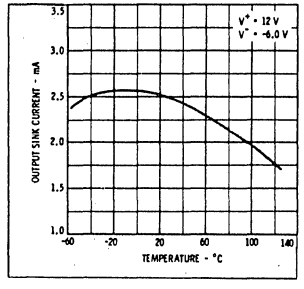
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



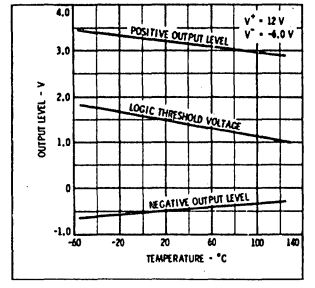
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



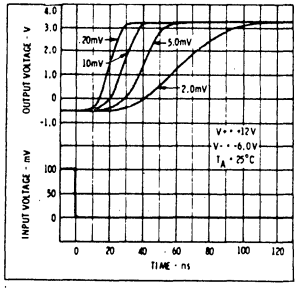
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



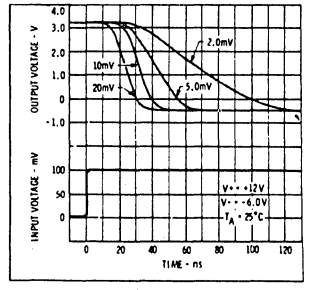
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



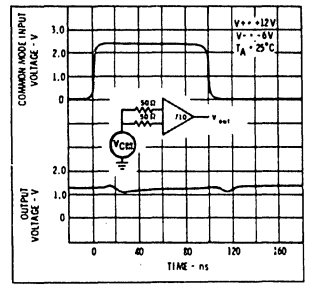
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

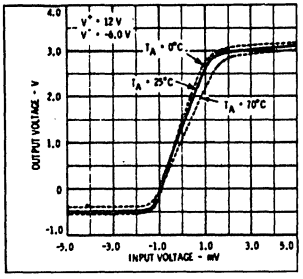


COMMON MODE PULSE RESPONSE

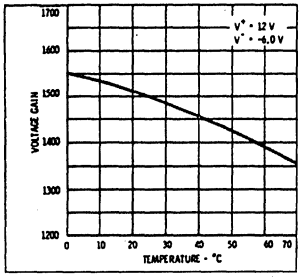


TYPICAL CHARACTERISTICS ITT720-5 (T_A=25°C, V^+ =12.0V = −6.0V unless otherwise specified)

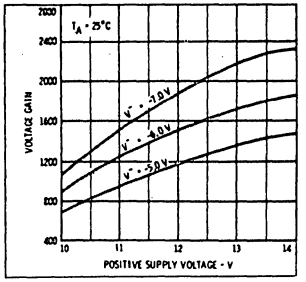
VOLTAGE TRANSFER CHARACTERISTIC



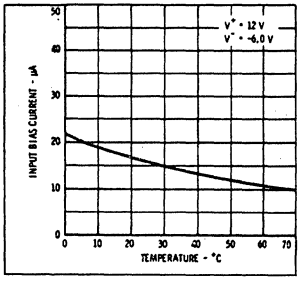
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



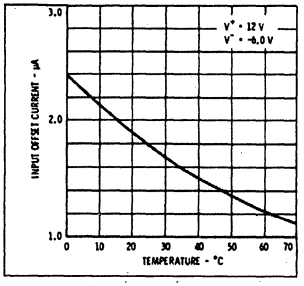
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



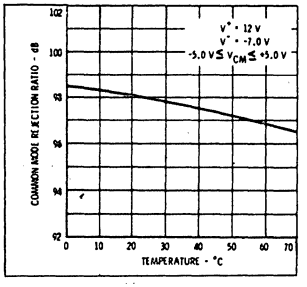
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



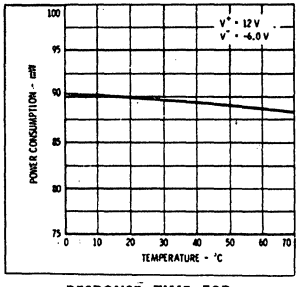
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



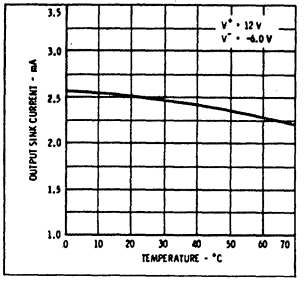
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



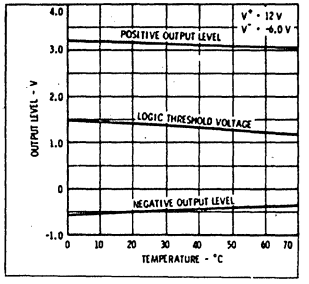
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



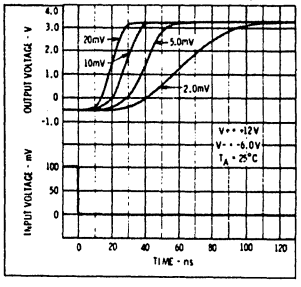
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



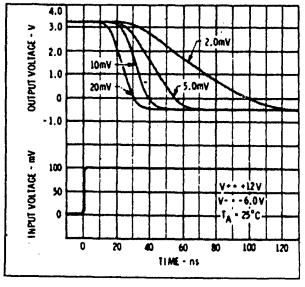
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



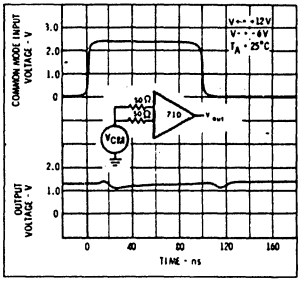
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



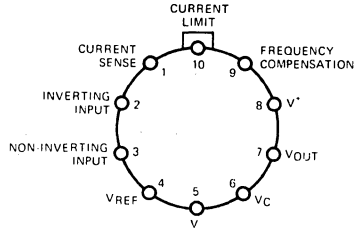
PRECISION VOLTAGE REGULATOR

PRECISION VOLTAGE REGULATOR ITT723

- **Positive or Negative Supply Operation**
- **Series, Shunt, Switching or Floating Operation**
- **.01% Line and Load Regulation**
- **Output Voltage Adjustable From 2 to 37 Volts**
- **Output Current to 150 mA Without External Pass Transistor**

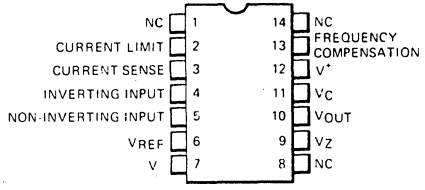
The ITT723 is a monolithic voltage regulator constructed on a single silicon chip using the epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass tansistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The ITT723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

Connection Diagrams
Top Views



Note: On metal can, pin 5 is connected to case.

14 LEAD DIP
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

Characteristics	ITT723-1	ITT723-5	Units
Pulse Voltage from V+ to V− (50 msec)	50		V
Voltage from V+ to V−		40	V
Continuous Voltage from V+ to V−	40		V
Maximum Output Current.....		150	mA
Input-Output Voltage Differential.....	40	40	V
Current from V_Z.....	25	25	mA
Current from V_{REF}.....	15	15	mA
Internal Power Dissipation—Metal Can (Note 1)	800	800	mW
Internal Power Dissipation—DIP (Note 1).....	900	900	mW

Characteristics (continued)	ITT723-1	ITT723-5	Units
Operating Temperature Range	−55 to +125	0 to +70	°C
Storage Temperature Range	−65 to +150	−65 to +150	°C
Lead Temperature (Soldering, 60 sec.)	300	300	°C

Note: On metal can, pin 5 is connected to case.

ELECTRICAL CHARACTERISTICS FOR ITT723-1 (Note 2)

Parameter (see definitions)	Min.	Typ.	Max.	Units	Conditions
Line Regulation		.01	0.1	$\%V_{OUT}$	V_{IN}=12V to V_{IN}=15V
		.02	0.2	$\%V_{OUT}$	V_{IN}=12V to V_{IN}=40V
			0.3	$\%V_{OUT}$	−55°C≤T_A≤+125°C, V_{IN}=12V to V_{IN}=15V
Load Regulation		.03	0.15	$\%V_{OUT}$	I_L=1 mA to I_L=50 mA
			0.6	$\%V_{OUT}$	−55°C≤T_A≤+125°C, I_L=1mA to I_L=50 mA
Ripple Rejection		74		dB	f=50 Hz to 10 kHz, C_{REF}=0
		86		dB	f=50 Hz to 10 kHz, C_{REF}=0 C_{REF}=5μF
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	−55°C≤T_A≤+125°C,
Short Circuit Current Limit		65		mA	R_{SC}=10Ω, V_{OUT}=0
Reference Voltage	6.95	7.15	7.35	V	
Output Noise Voltage		20		μV_{rms}	BW=100Hz to 10 kHz, C_{REF}=0
		2.5		μV_{rms}	BW=100Hz to 10 kHz, C_{REF}=5μF
Long Term Stability		0.1		%/1000hrs	
Standby Current Drain		2.3	3.5	mA	I_L=0, V_{IN}=30V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	

Definition of Terms

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.

SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.

Equivalent Circuit

OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.

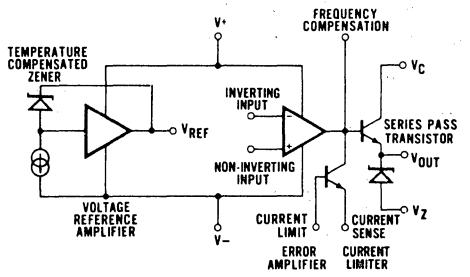
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operatae.

SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

EQUIVALENT CIRCUIT



NOTES:

1. Derate metal can package at 6.8 mW/°C and dual-in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.

2. Unless otherwise specified, T_A=25°C, V_{IN}= V+=V_C=12V, V−=0, V_{out}=5V, 1_L =1mA, R_{SC}=0,

C_1=100pF, C_{REF}=0 and divider impedance as seen by error Amplifier≤10KΩ connected as shown in Fig. 1.

3. L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

4. Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.

5. Replace R_1R_2 in figures with divider shown in figure 13.

6. V+ must be connected to a +3V or greater supply.

ELECTRICAL CHARACTERISTICS FOR ITT723-5 (Note 2)

PARAMETER (see definitions)	Min.	Typ.	Max.	Units	Conditions
Line Regulation		.01	0.1	%V_{OUT}	V_{IN}=12V to V_{IN}=15V
		0.1	0.5	%V_{OUT}	V_{IN}=12V to V_{IN}=40V
			0.3	%V_{OUT}	0°C≤T_A≤70°C, V_{IN}=12V to V_{IN}=15V
Load Regulation		.03	0.2	%V_{OUT}	I_L=1 mA to I_L=50 mA
			0.6	%V_{OUT}	0°C≤T_A≤70°C, I_L=1 mA to I_L=50 mA
Ripple Rejection		74		dB	f=50 Hz to 10 kHz, C_{REF}=0
		86		dB	f=50 Hz to 10 kHz, C_{REF}=5μF
Average Temperature Coefficient of Output Voltage		.003	.015	%/°C	0°C≤T_A≤70°C
Short Circuit Current Limit		65		mA	R_{SC}=10Ω, V_{OUT}=0

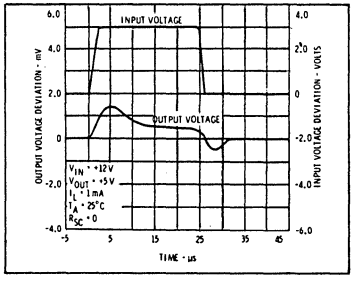
ITT723
PRECISION VOLTAGE REGULATOR

ELECTRICAL CHARACTERISTICS FOR ITT723-5 (Note 2)

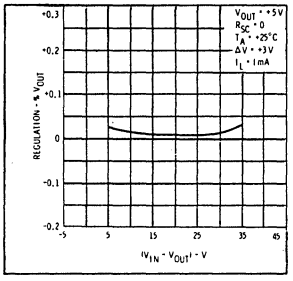
PARAMETER (see definitions)	Min.	Typ.	Max.	Units	Conditions
Reference Voltage	6.80	7.15	7.50	V	
Output Noise Voltage		20		μV_{rms}	BW=100Hz to 10 kHz, $C_{REF}=0$
		2.5		μV_{rms}	BW=100 Hz to 10 kHz, $C_{REF}=5\mu F$
Long Term Stability		0.1		%/1000hrs	
Standby Current Drain		2.3	4.0	mA	$I_L=0$, $V_{IN}=30V$
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Differential	3.0		38	V	

TYPICAL PERFORMANCE CURVES ITT723-1,ITT723-5

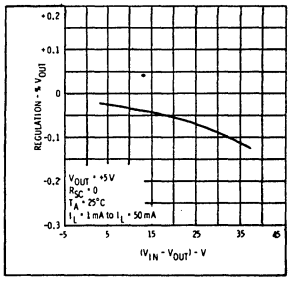
LINE TRANSIENT RESPONSE



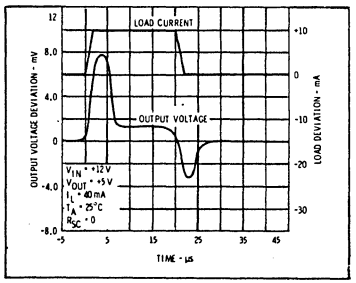
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



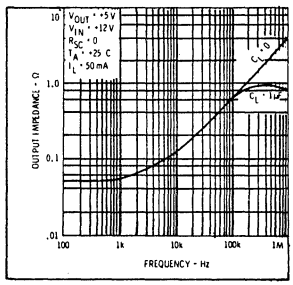
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



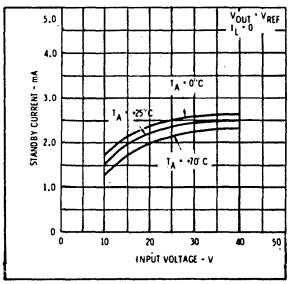
LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

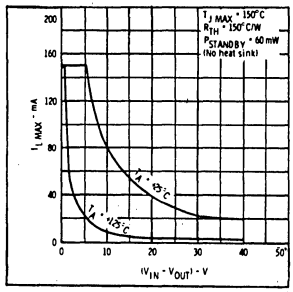


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

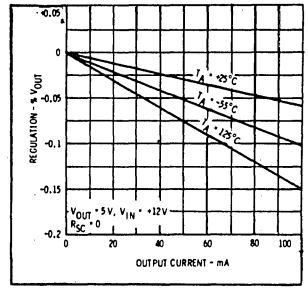


TYPICAL PERFORMANCE CURVES ITT723-1

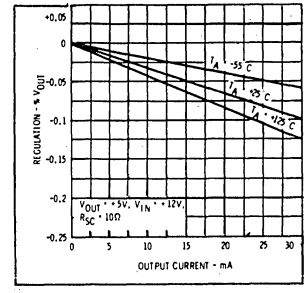
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



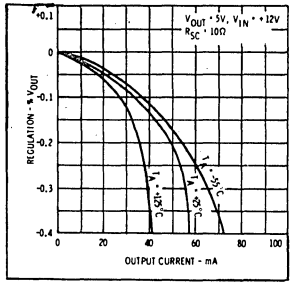
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



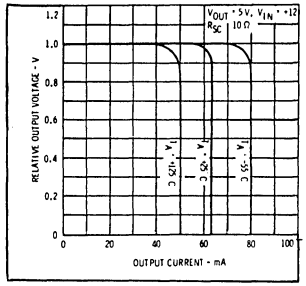
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



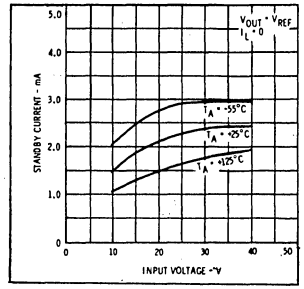
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

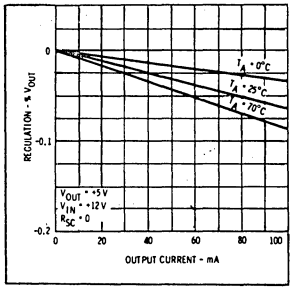


AS A STANDBY CURRENT DRAIN FUNCTION OF INPUT VOLTAGE

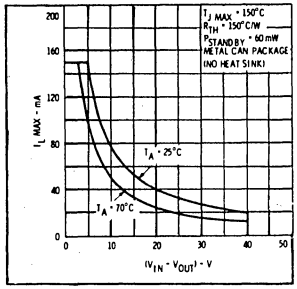


TYPICAL PERFORMANCE CURVES ITT723-5

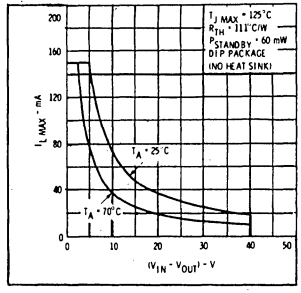
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



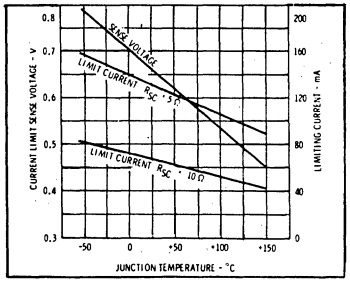
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



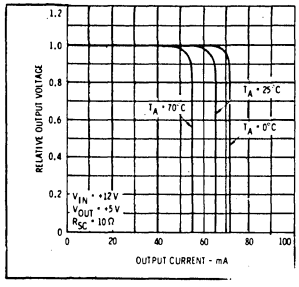
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



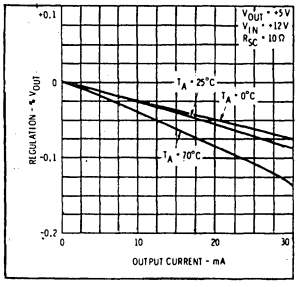
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



CURRENT LIMITING CHARACTERISTICS



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



ITT723
PRECISION VOLTAGE REGULATOR

TABLE I — RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II — FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

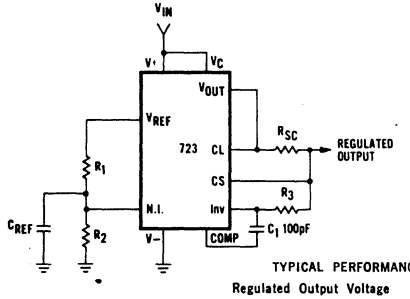
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\,R_3}{R_{SC}\,R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\,R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



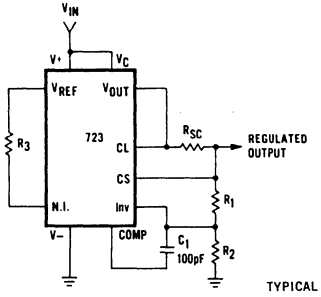
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\,R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



TYPICAL PERFORMANCE

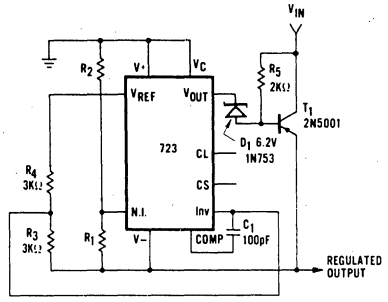
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\,R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 3

NEGATIVE VOLTAGE REGULATOR

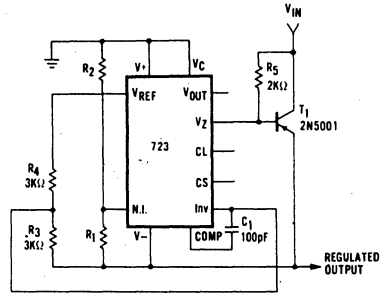


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Figure 3A*

NEGATIVE VOLTAGE REGULATOR



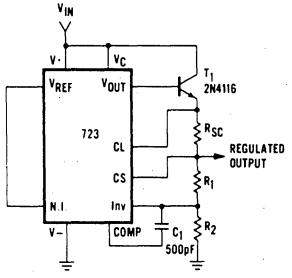
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

Figure 4

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

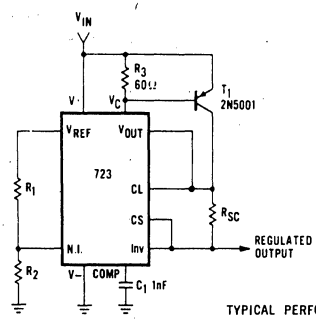


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

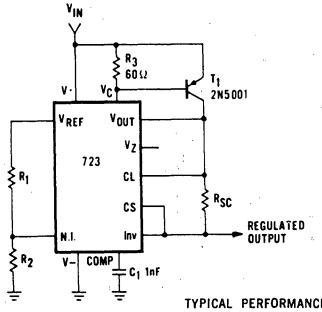


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Figure 5A*

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

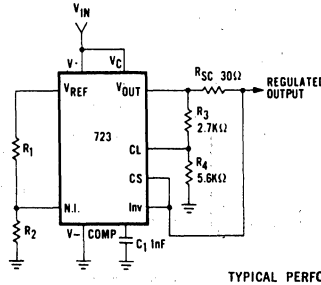


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

* Figure numbers followed by "A" indicate low temperature range

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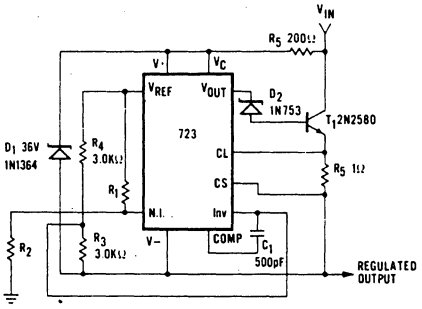
PRECISION VOLTAGE REGULATOR

Figure 7

POSITIVE FLOATING REGULATOR

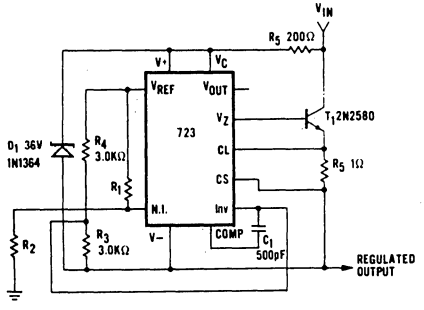


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

Figure 7A*

POSITIVE FLOATING REGULATOR

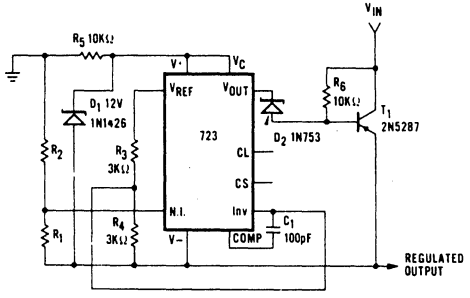


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

Figure 8

NEGATIVE FLOATING REGULATOR

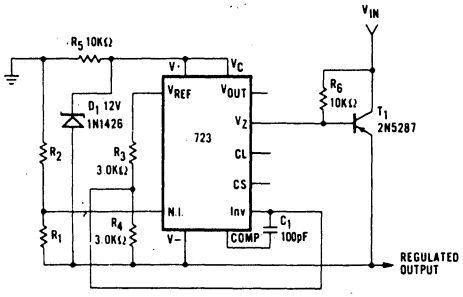


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_{IN} = 20 V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 8A*

NEGATIVE FLOATING REGULATOR

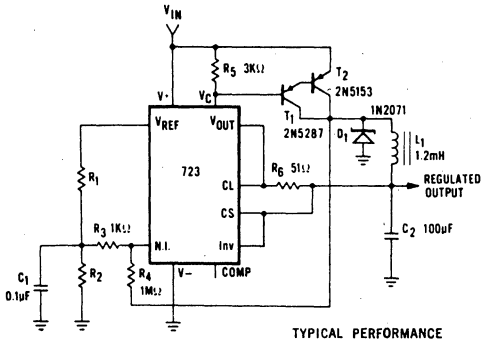


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_{IN} = 20 V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 9

POSITIVE SWITCHING REGULATOR



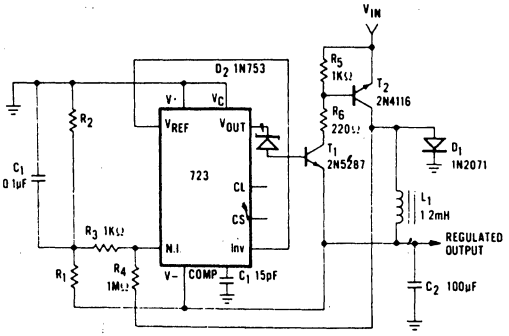
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

Note 3

Figure 10

NEGATIVE SWITCHING REGULATOR



TYPICAL PERFORMANCE

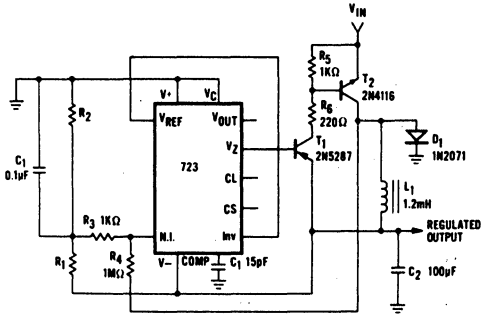
Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3

* Figure numbers followed by "A" indicate low temperature range

Figure 10A*

NEGATIVE SWITCHING REGULATOR



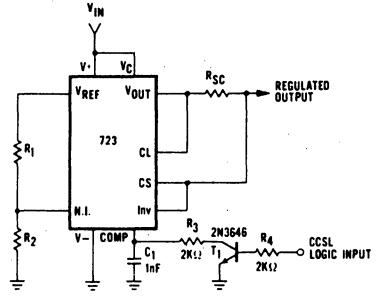
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3
Note 7

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



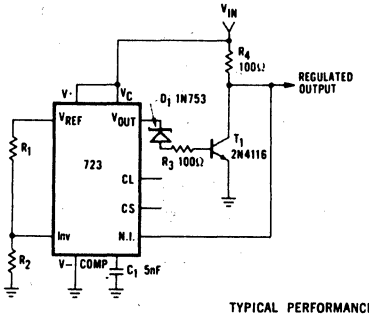
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12

SHUNT REGULATOR



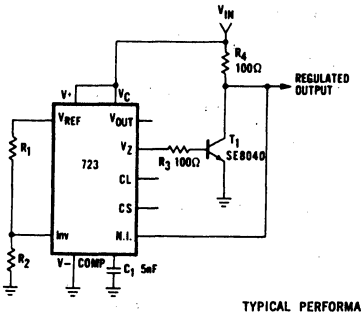
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Note 3

Figure 12

SHUNT REGULATOR

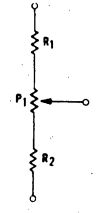


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM

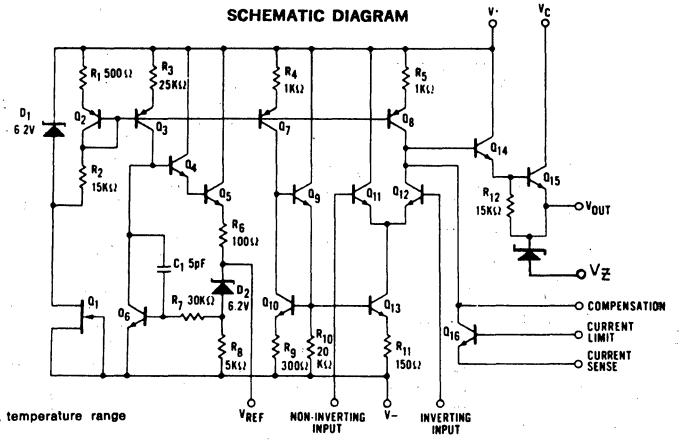


Figure numbers followed by "A" indicate low temperature range

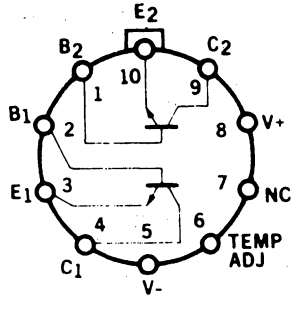
SEMICONDUCTORS

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

- **Excellent Transistor Matching**
- **Close Thermal Coupling**
- **Fast Thermal Response**
- **Tight Temperature Control**

ITT726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictible exponential relation between emitter-base voltage and collector current matching, close thermal coupling and fast a single silicon chip using the ITT Planar process.

Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

Maximum Ratings For Each Transistor

Characteristics	Units
Maximum collector-to-substrate voltage ..	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

NOTE:
1. Measured at 1 mA collector current.

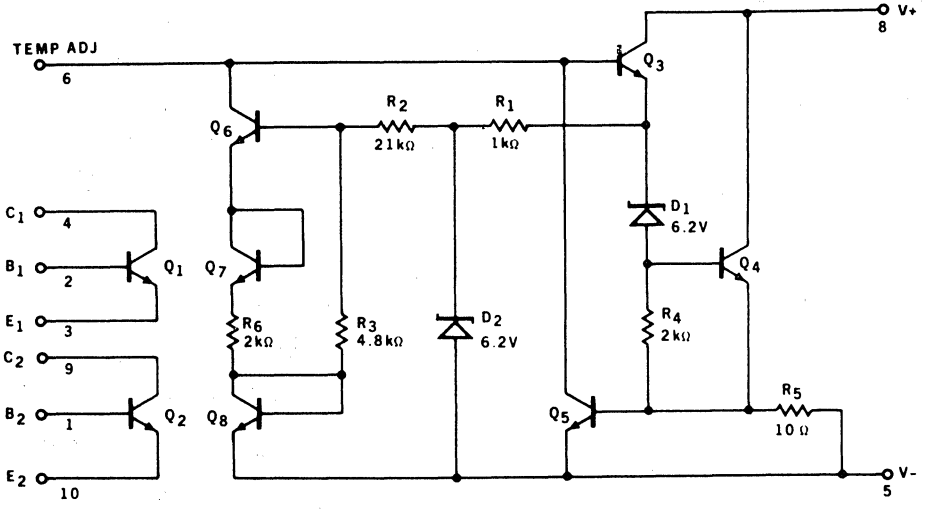
ELECTRICAL CHARACTERISTICS FOR ITT726-1

($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15V$, $R_{adj} = 62k\Omega$ unless otherwise specified)

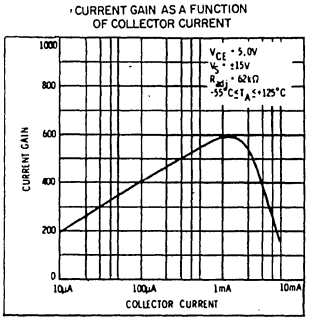
Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	2.5	mV	$10\mu A \leq I_C \leq 100\mu A$ $V_{CE}=5V$, $R_S \leq 50\Omega$
Input Offset Current		10	50	nA	$I_C=10\mu A$, $V_{CE}=5V$
Input Offset Current		50	200	nA	$I_C=100\mu A$, $V_{CE}=5V$
Average Input Bias Current		50	150	nA	$I_C=10\mu A$, $V_{CE}=5V$
Average Input Bias Current		250	500	nA	$I_C=100\mu A$, $V_{CE}=5V$
Offset Voltage Change		0.3	6.0	mV	$I_C=10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$

ELECTRICAL CHARACTERISTICS FOR ITT726-1
($-55°C \leqslant T_A \leqslant +125°C$, $V_S = \pm 15V$, $R_{adj} = 62k\Omega$ unless otherwise specified) **(continued)**

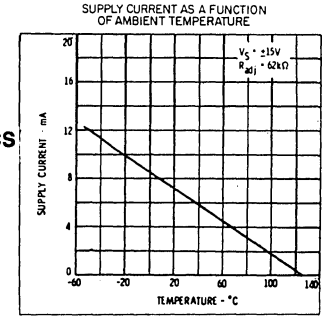
Parameter	Min.	Typ.	Max.	Units	Conditions
Offset Voltage Change		0.3	6.0	mV	$I_C = 100\mu A$, $5V \leqslant V_{CE} \leqslant 25V$, $R_S \leqslant 10k\Omega$
Input Offset Voltage Drift		0.2	1.0	$\mu V/°C$	$10\mu A \leqslant I_C \leqslant 100\mu A$, $V_{CE} = 5V$, $R_S \leqslant 50\Omega$, $+25°C \leqslant T_A \leqslant +125°C$
Input Offset Voltage Drift		0.2	1.0	$\mu V/°C$	$10\mu A \leqslant I_C \leqslant 100\mu A$, $V_{CE} = 5V$, $R_S \leqslant 50\Omega$, $-55°C \leqslant T_A \leqslant +25°C$
Input Offset Current Drift		10		pA/°C	$I_C = 10\mu A$, $V_{CE} = 5V$
Input Offset Current Drift		30		pA/°C	$I_C = 100\mu A$, $V_{CE} = 5V$
Supply Voltage Rejection Ratio		25		$\mu V/V$	$10\mu A \leqslant I_C \leqslant 100\mu A$, $R_S \leqslant 50\Omega$,
Low-Frequency Noise		4.0		μVpp	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leqslant 50\Omega$, BW = .001Hz to 0.1Hz
Broadband Noise		10		μVpp	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leqslant 50\Omega$, BW = 0.1Hz to 10kHz
Long-Term Drift		5.0		μV/week	$10\mu A \leqslant I_C \leqslant 100\mu A$, $V_{CE} = 5V$, $R_S \leqslant 50\Omega$, $T_A = 25°C$
High-Frequency Current Gain	1.5	3.5			f = 20MHz, $I_C = 100\mu A$, $V_{CE} = 5V$
Output Capacitance		3.0		pF	$I_E = 0$, $V_{CB} = 5V$
Emitter Transition Capacitance		1.0		pF	$I_E = 100\mu A$
Collector Saturation Voltage		0.5	1.0	V	$I_B = 100\mu A$, $I_C = 1mA$



Schematic Diagram-1-5



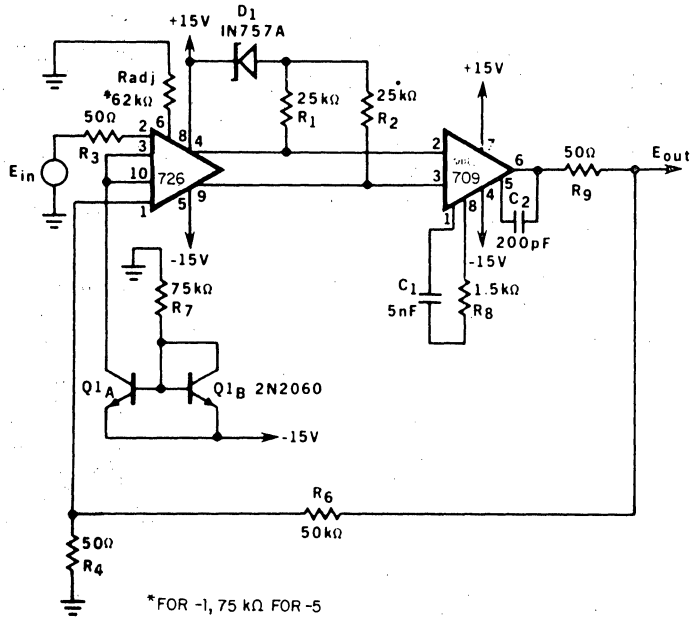
TYPICAL CHARACTERISTICS FOR ITT726-1



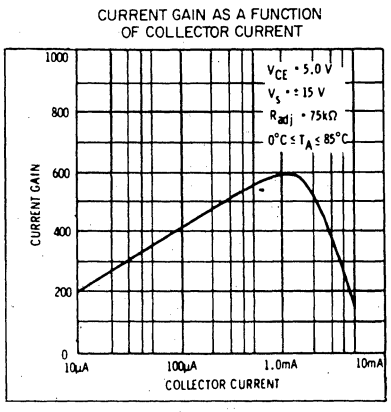
ELECTRICAL CHARACTERISTICS FOR ITT726-5 ($0°C \leqslant T_A \leqslant +85°C$, $V_S = \pm 15V$, $R_{adj} = 75k\Omega$ unless otherwise specified)

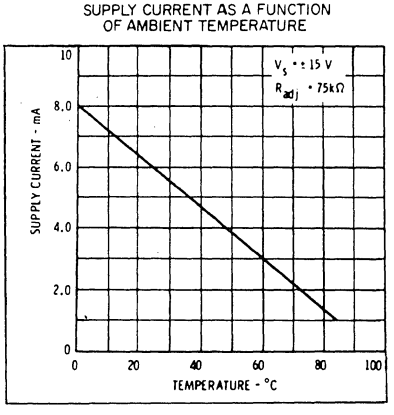
Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	3.0	mV	$10\mu A \leqslant I_C \leqslant 100\mu A$ $V_{CE}=5V$, $R_S \leqslant 50\Omega$
Input Offset Current		10	100	nA	$I_C=10\mu A$, $V_{CE}=5V$
Input Offset Current		50	400	nA	$I_C=100\mu A$, $V_{CE}=5V$
Average Input Bias Current		50	300	nA	$I_C=10\mu A$, $V_{CE}=5V$
Average Input Bias Current		250	1000	nA	$I_C=100\mu A$, $V_{CE}=5V$
Offset Voltage Change		0.3	6.0	mV	$I_C=10\mu A$, $5V \leqslant V_{CE} \leqslant 25V$, $R_S \leqslant 100k\Omega$
Offset Voltage Change		0.3	6.0	mV	$I_C=100\mu A$, $5V \leqslant V_{CE} \leqslant 25V$, $R_S \leqslant 10k\Omega$
Input Offset Voltage Drift		0.2	2.0	$\mu V/°C$	$I_C=100\mu A$, $V_{CE}=5V$ $R_S \leqslant 50\Omega$,
Input Offset Current Drift		10		pA/°C	$I_C=10\mu A$, $V_{CE}=5V$
Input Offset Current Drift		30		pA/°C	$I_C=100\mu A$, $V_{CE}=5V$
Supply Voltage Rejection Ratio		25		$\mu V/V$	$I_C=100\mu A$, $R_S \leqslant 50\Omega$
Low-Frequency Noise		4.0		μVpp	$I_C=10\mu A$, $V_{CE}=5V$ $R_S \leqslant 50\Omega$, BW=0.001Hz to 0.1Hz
Broadband Noise		10		μVpp	$I_C=10\mu A$, $V_{CE}=5V$ $R_S \leqslant 50\Omega$, BW=0.1Hz to 10kHz
Long-Term Drift		5.0		μV/week	$I_C=100\mu A$, $V_{CE}=5V$ $R_S \leqslant 50\Omega$, $T_A=25°C$
High-Frequency Current Gain	1.5	3.5			f=20MHz, $I_C=100\mu A$, $V_{CE}=5V$
Output Capacitance		3.0		pF	$I_E=0$, $V_{CB}=5V$
Emitter Transition Capacitance		1.0		pF	$I_E=100\mu A$
Collector Saturation Voltage		0.5	1.0	V	$I_B=100\mu A$, $I_C=1mA$

ITT726
TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR



Typical X1000 Circuit





Typical Characteristics For ITT726-5

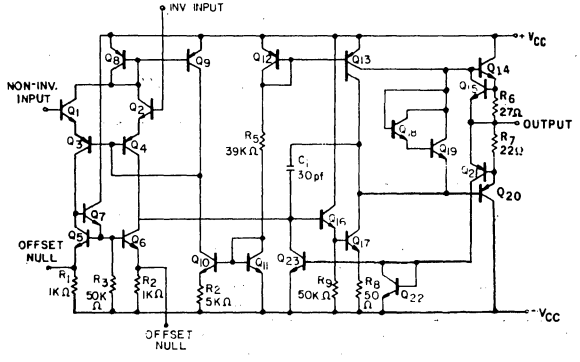
ITT SEMICONDUCTORS

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **No Frequency Compensation Required**
- **Short-Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

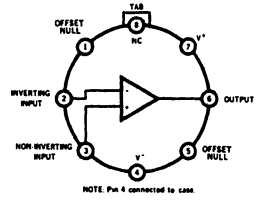
The ITT741 is a high performance monolothic operational amplifier constructed on a single silicon chip, using the ITT Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the ITT741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The ITT741 is short-circuit protected, has the same pin configuration as the popular ITT709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

Schematic Diagram

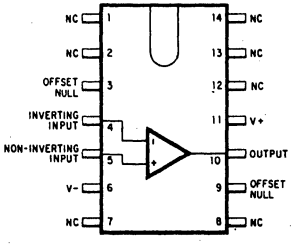


CONNECTION DIAGRAMS
(TOP VIEW)

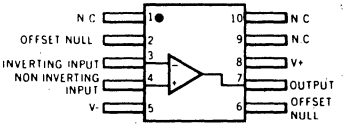
8 LEAD METAL CAN



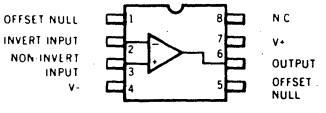
14 LEAD DIP



FLATPACK



MINIDIP



ITT741
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Characteristics	ITT741-1	ITT741-5	Units
Supply Voltage	±22	±18	V
Internal Power Dissipation	500 (Note 1)	500	mW
Differential Input Voltage	±30	±30	V
Input Voltage (Note 2)	±15	±15	V
Storage Temperature Range	−65 to +150	−65 to +150	°C
Operating Temperature Range	−55 to +125	0 to +70	°C
Lead Temperature (Soldering, 60 sec)	300	300	°C
Output Short-Circuit Duration	Indefinite (Note 3)	Indefinite (Note)	

NOTES:
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature and 75°C ambient temperature.
4. Short circuit may be to ground or either supply.

ELECTRICAL CHARACTERISTICS FOR ITT741-1 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		1.0	5.0	mV	R_S 10kΩ
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10k\Omega$
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3	1.0	μs	
Overshoot		5.0	10	%	
Slew Rate (unity gain) (Pulsed)		0.5		V/μs	

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Input Offset Voltage		6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		500	nA	
Input Bias Current		1.5	μA	
Large-Signal Voltage Gain	25,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±10		V	$R_L \geq 2k\Omega$

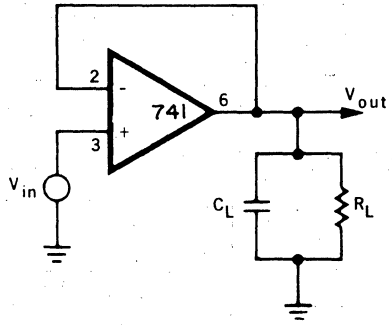
ELECTRICAL CHARACTERISTICS FOR ITT741-5 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	20,000	100,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10k\Omega$
Power Consumption		50	85	mV	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Overshoot		0.3		μs	
Risetime		5.0		%	
Slew Rate (unity gain)		0.5		V/μs	$R_L \geq 2k\Omega$

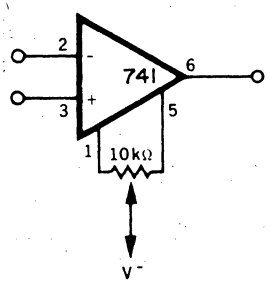
The following specifications apply for $0°C \leq T_A \leq +70°C$:

Input Offset Voltage		7.5	mV	$R_S \leq 10k\Omega$
Input Offset Current		300	nA	
Input Bias Current		800	nA	
Large-Signal Voltage Gain	15,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±10		V	$R_L \geq 2k\Omega$

Transient Response Test Circuit

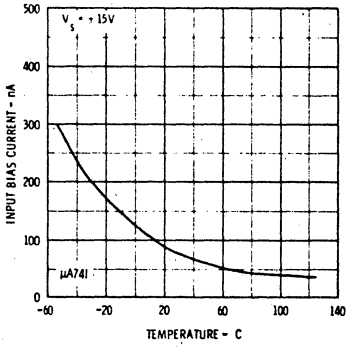


Voltage Offset Null Circuit

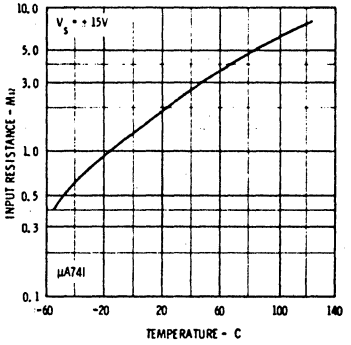


TYPICAL PERFORMANCE CURVES ITT741-1

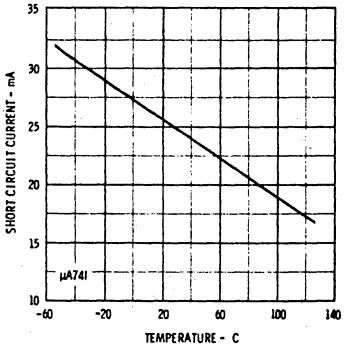
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



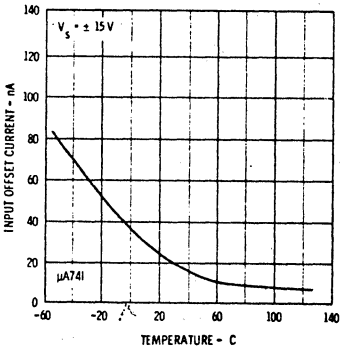
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



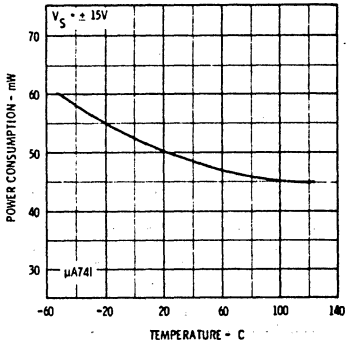
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



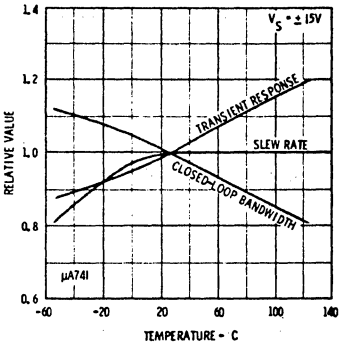
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



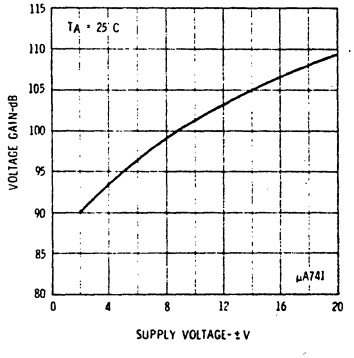
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



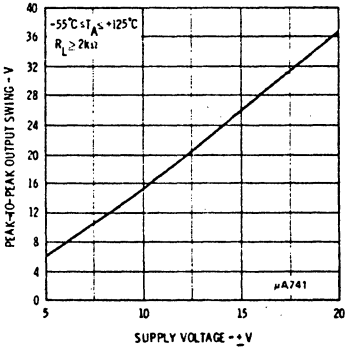
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



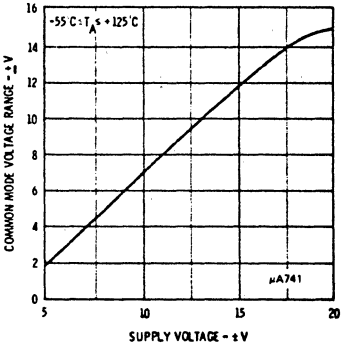
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

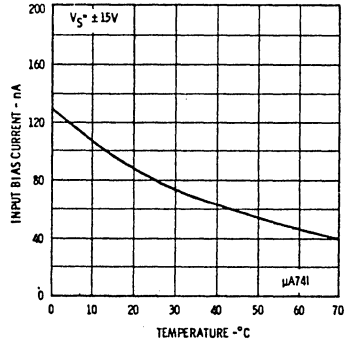


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

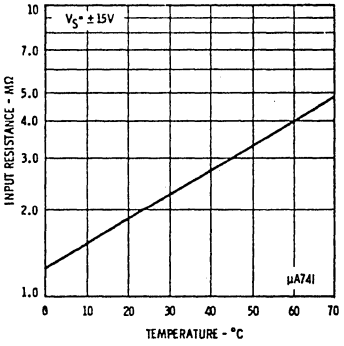


TYPICAL PERFORMANCE CURVES ITT741-5

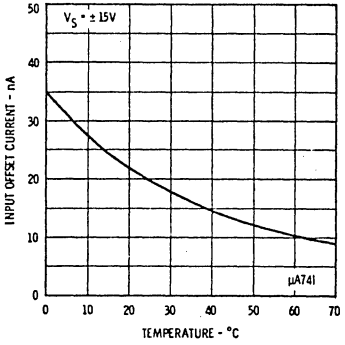
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



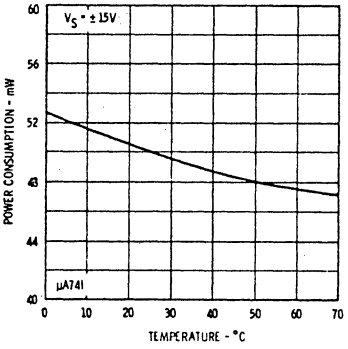
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



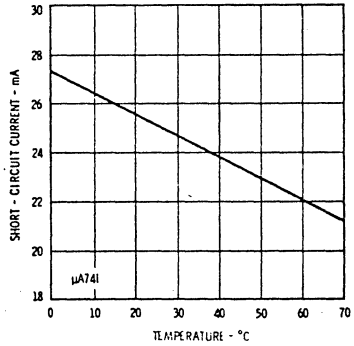
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



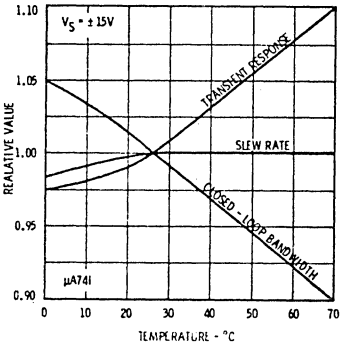
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



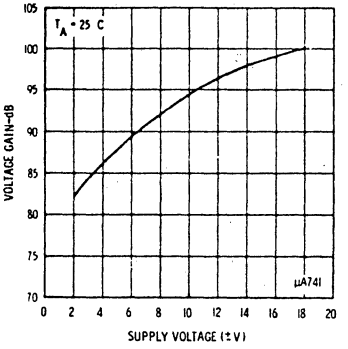
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



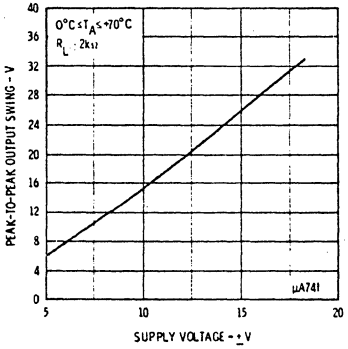
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



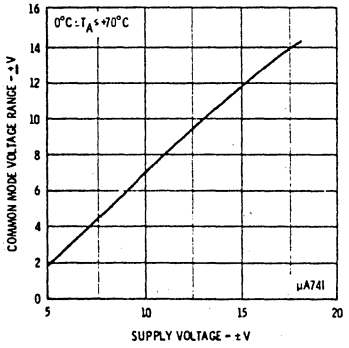
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

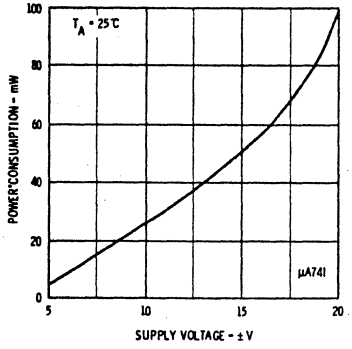


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

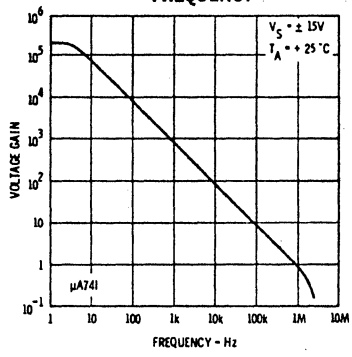


TYPICAL PERFORMANCE CURVES ITT741-1, ITT741-5

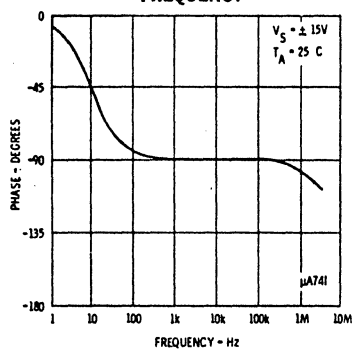
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



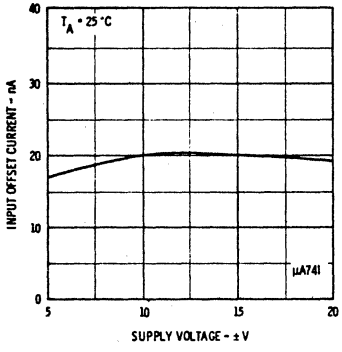
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



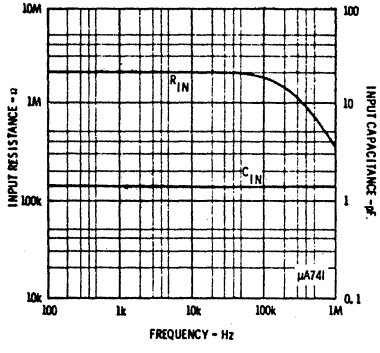
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



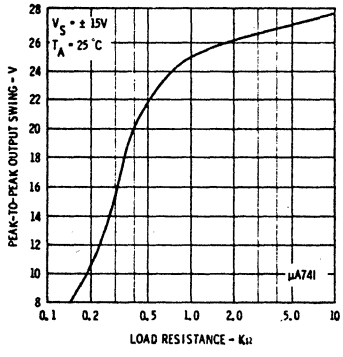
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



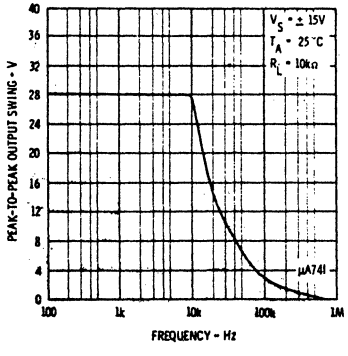
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

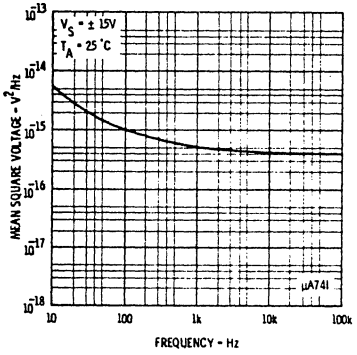


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

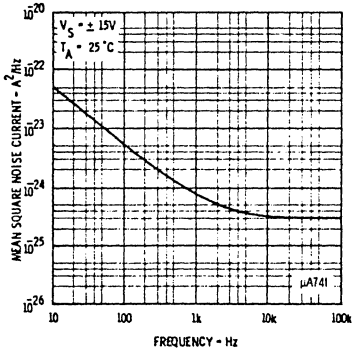


TYPICAL PERFORMANCE CURVES ITT741-1, ITT741-5 (continued)

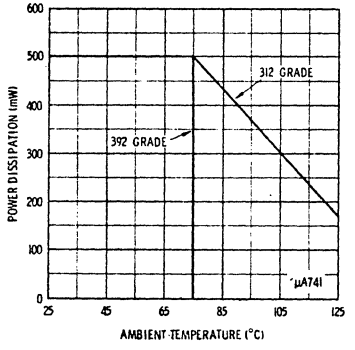
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



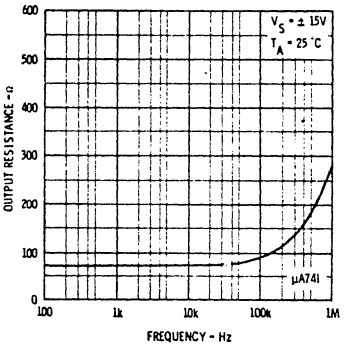
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



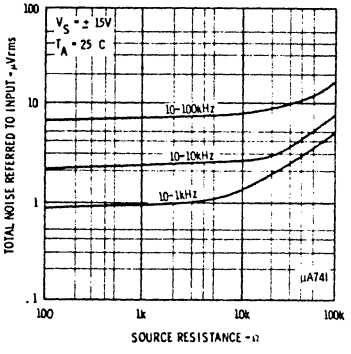
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



BROADBAND NOISE FOR VARIOUS BANDWIDTHS



ITT SEMICONDUCTORS

Package Dual In-Line

MOS TO LED SEGMENT AND DIGIT DRIVERS

Quad Segment Driver and Hex Digit Driver for interfacing between MOS and Light Emitting Diode (LED) displays.

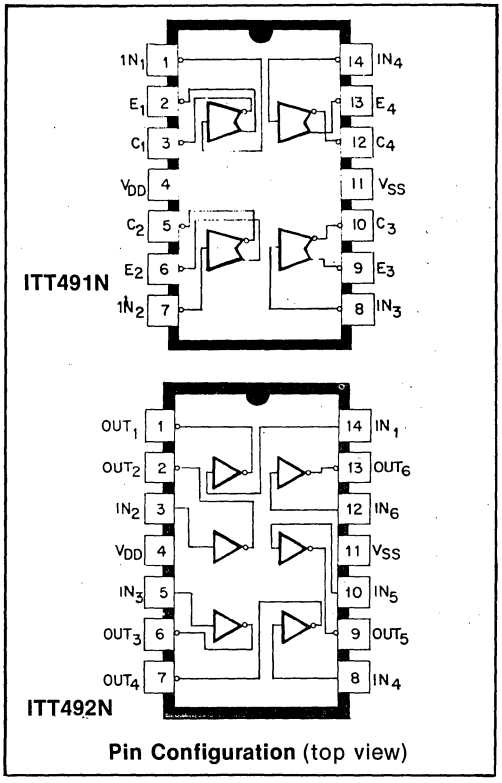
ITT491

- **50 mA Source or Sink capability**
- **Low Input Current for MOS compatibility**
- **Low Standby Power**
- **Quad High Gain Darlington Circuits**

ITT492

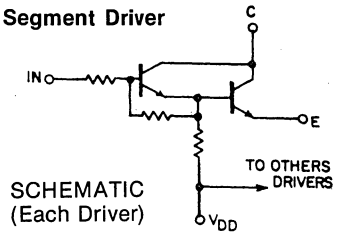
- **250 mA Sink capability**
- **Low Input Current for MOS compatibility**
- **Low Standby Power**
- **Hex High Gain Darlington Circuits**

The ITT491 and ITT492 were designed to be used together with MOS IC's and with common cathode LED's in serially addressed multi-digit displays. This time multiplexed system using a segment address and digit scan method of LED drive minimizes the number of drivers required.



Pin Configuration (top view)

ITT491 Quad Segment Driver



SCHEMATIC (Each Driver)

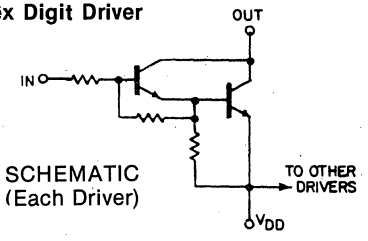
ITT491 TRUTH TABLE

Input	Output E	Output C
L	L	H
H	H	L

ITT492 TRUTH TABLE

Input	Output
L	H
H	L

ITT492 Hex Digit Driver



SCHEMATIC (Each Driver)

ITT491, ITT492
MOS TO LED SEGMENT AND DIGIT DRIVERS

ABSOLUTE MAXIMUM RATINGS (over free air temperature range unless otherwise noted).

PARAMETER	ITT491	ITT492	UNITS
Supply Voltage Vss (1)	10	10	V
Input Voltage	Vss	Vss	
Collector Voltage (2)	10	10	V
Collector to Emitter Voltage	10		V
Collector to Input Voltage	10	10	V
Emitter Voltage	5	—	V
Emitter to Input Voltage	5	—	V
VDD to Input Voltage (3)	5	5	V
Continuous Collector Current	50	250	mA
Continuous VDD Current	—	600	mA
Continuous Total Power Dissipation	800	800	mW
Operating Free-Air Temperature Range	0 to70	0 to 70	C
Storage Temperature Range	-65 to 150	-65 to 150	C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260	260	C

NOTES: (1) Vss terminal voltage is with respect to any other device terminal.
(2) Voltage values are with respect to Vss terminal unless otherwise noted.
(3) With the exception of the inputs, the Vdd terminal must always be the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (unless otherwise noted $V_{SS} = 10V$, $T_A = 0$ C to 70 C).

ITT491

PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{CEL} Low-Level collector-to-emitter voltage		0.9	1.2	V	$V_{IN} = 8.5V$ through 1K $I_{OL} = 50mA$, $V_E = 5V$, $T_A = 25$ C
		0.9	1.5	V	$V_{IN} = 8.5V$ through 1K $I_{OL} = 50mA$, $V_E = 5V$
I_{CH} High-Level collector current			100	µA	$V_{CH} = 10V$, $V_E = 0$ $I_{IN} = 40uA$
			100	µA	$V_{CH} = 10V$, $V_E = 0$ $V_{IN} = 0.7V$
I_I Input current at maximum input voltage		2.0	3.3	mA	$V_{IN} = 10V$; $I_{OL} = 20mA$ $V_{IN} = 0$, $V_E = 5V$
I_{ER} Reversed biased emitter current			100	µA	$I_C = 0$
I_{SS} supply current			1.0	mA	

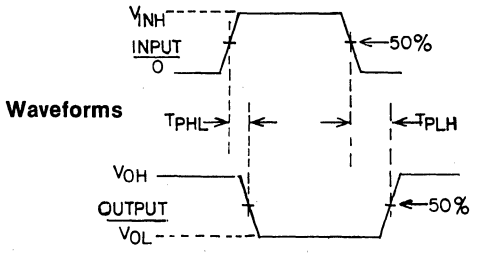
ITT492

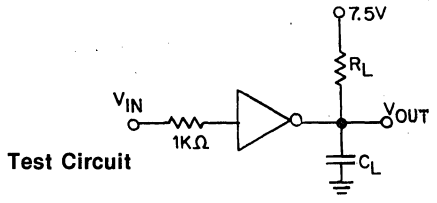
PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL} Low-Level output voltage		0.9	1.2	V	V_{IN} = 6.5V through 1K I_{OL} = 250mA, T_A = 25 C
		0.9	1.5	V	V_{IN} = 6.5V through 1K I_{OL} = 250mA
I_{OH} High-Level output current			200	µA	V_{OH} = 10V, I_{IN} = 40uA
			200	µA	V_{OH} = 10V, V_{IN} = 0.5V
I_I Input current at maximum input voltage		2.0	3.3	mA	V_{IN} = 10V, I_{OL} = 20mA
I_{SS} supply current			1.0	mA	

NOTE: All typical values are at TA = 25 C.

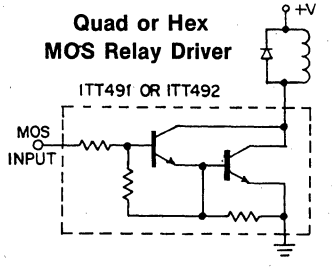
SWITCHING CHARACTERISTICS: V_{SS} = 7.5V, T_A = 25 C

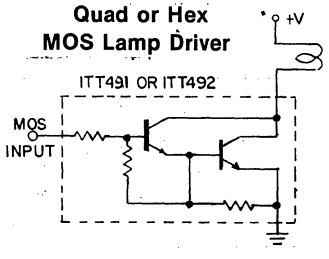
DEVICE	MIN.	TYP.	MAX.	UNIT	TEST	CONDITIONS
ITT491		20		ns	T_{PHL}	R_L = 200 , V_{INH} = 4.5V
		100		ns	T_{PLH}	C_L = 15pF, V_E = 0
ITT492		40		ns	T_{PHL}	R_L = 39 , V_{INH} = 7.5V
		600		ns	T_{PLH}	C_L = 15pF

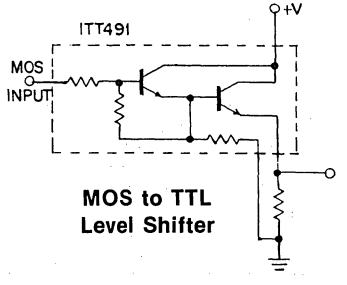




APPLICATIONS — MOS INTERFACE ITT491 AND ITT492

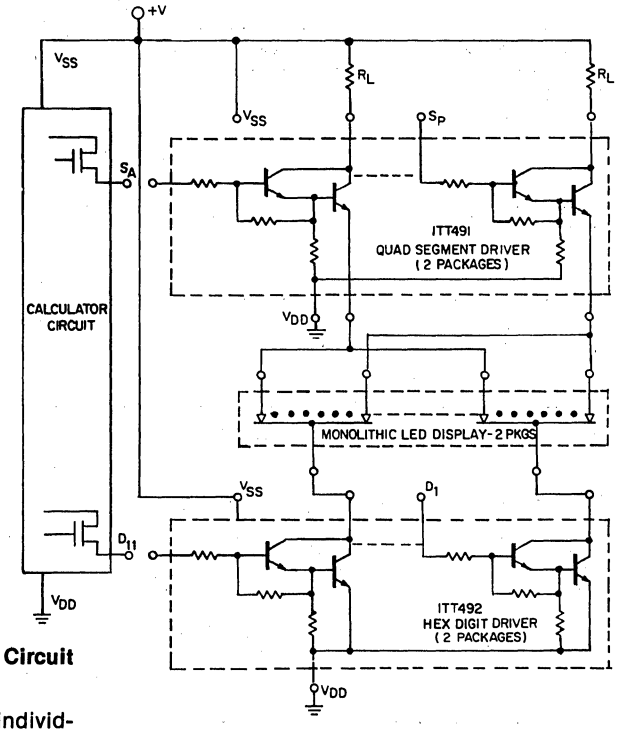






ITT491, ITT492
MOS TO LED SEGMENT AND DIGIT DRIVERS

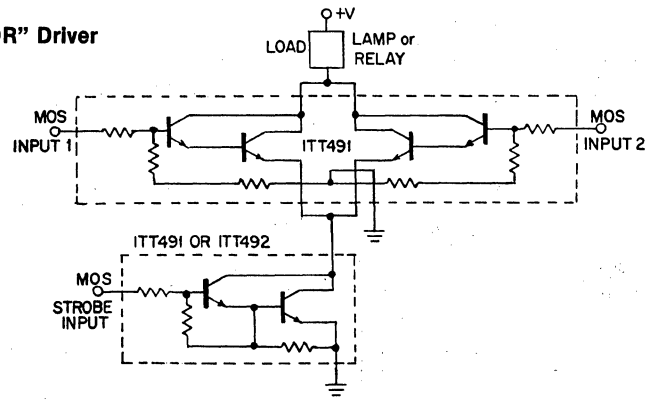
TYPICAL APPLICATION
ITT491 and ITT492



Interfacing Between MOS Calculator Circuit and LED Multi-Digit Display

This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a seven-segment display plus decimal point may be displayed using only two ITT491 and two ITT492 drivers.

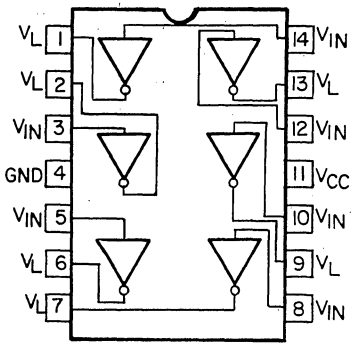
MOS Strobed "NOR" Driver



HEX DIGIT DRIVER

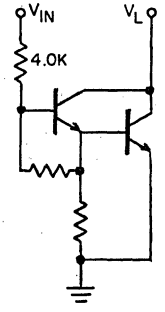
- **MOS to LED digit driver**
- **250 mA sink capability**
- **Suitable for desk top and pocket calculators**
- **Operation down to 5V**
- **High gain Darlington Outputs**

The ITT 500 is a monolithic integrated circuit which provides the interface between MOS integrated circuits and Light Emitting Diode (LED) digit displays. The ITT too is designed to be used in serially addressed multi-digit displays. This time-multiplexed system, using a segment address and digit scan method of LED drive, minimizes the number of drivers required. The ITT 500 together with the ITT 501 segment driver will operate over a wide range of supply voltages to 5 volts. The Vcc terminal must be connected to the most positive supply.



Pin Configuration (Top View)

schematic



(Each Driver, 6 per package)

ABSOLUTE MAXIMUM RATINGS
(Measurement with respect to GND)

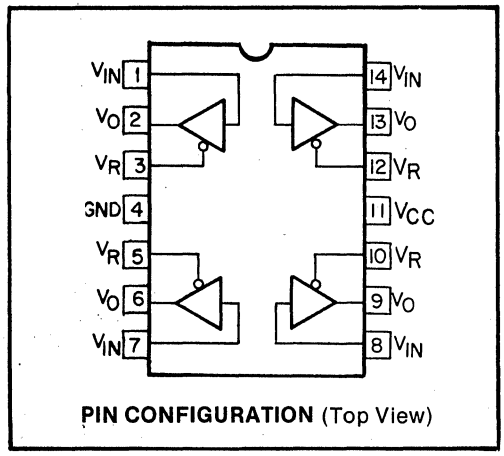
Characteristic	Unit
Collector Voltage V_{IL}	18 V
Supply Voltage V_{CC}	18 V
Input Voltage ($V_{in} \leqslant V_{CC}$) V_{in}	18 V
Continuous total power dissipation	800 mW
Storage temperature range	−55 °C to +125 °C
Operating temperature range	0 °C to +50°C

ELECTRICAL CHARACTERISTICS (Unless otherwise notes $T_A = 25$ C, $V_{CC} = 15$ V)

PARAMETER	MIN	MAX	UNIT	NOTES	Test Condition
I_{OL}	250		mA	One driver 'on'	$I_{IN} > 0.9$ MA $V_{OL} = 1.25$ V
I_{OH}		200	µA		V_{IL} <0.4 V $V_{OH} = 15$V
I_{IH}	0.2	0.9	mA	Slope typically 4 kΩ	$V_{IH} = 3.0$V
I_{IL}	25		µA	Slope typically 11 kΩ	$V_{IL} = 0.4$V $I_{OH} = 200$ UA

QUAD SEGMENT DRIVER

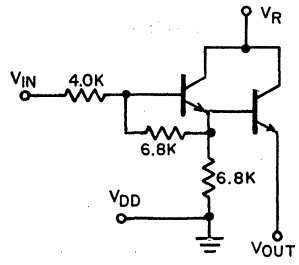
- **MOS to LED segment driver**
- **50 mA source or sink capability**
- **Suitable for desk top and pocket calculator**
- **Operation down to 5V**
- **High gain Darlington Outputs**



PIN CONFIGURATION (Top View)

The ITT 501 is a monolithic, integrated circuit which provides the interface between MOS integrated circuits and Light Emitting Diode (LED) displays. The ITT 501 is designed to be used in serially addressed multi-digit displays. This time-multiplexed system, using a segment address and digit scan method of LED drive, minimizes the number of drivers required. This circuit is designed to be used with current source resistors in series with the LED segments. This aids in matching segment intensity and reduces the total power dissipation. A resistor value of 200 ohms provides a good current source for each segment when the ITT 501 together with the ITT 500 (Digit Driver) is used at 15 volts with 2 volt/25mA LED displays. The V_{CC} terminal must be connected to the most positive supply.

SCHEMATIC



(Each Drive, 4 per package)

ABSOLUTE MAXIMUM RATINGS
(Measurement with respect to GND)

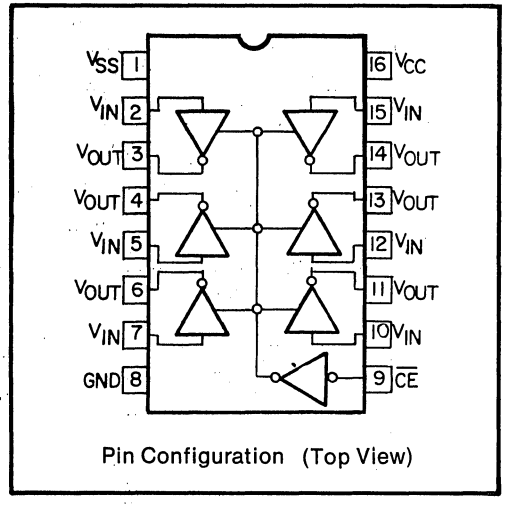
Characteristics	Unit
Supply Voltage V_{CC}	18 V
Input Voltage ($V_{IN} \geq V_{CC}$) V_{in}	18 V
Isolation Voltage V_{SS}	18 V
Continuous Total Power-Dissipation	800 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +50°C

D.C. SPECIFICATIONS — ITT 501 At 25 C unless otherwise specified. All voltages are with respect to Gnd. All currents into the device are + .

PARAMETER	V cc	MIN	MAX	UNITS	NOTES	TEST CONDITIONS
I_{OL}	15v	—50		ma		I_{IN} = 0.35 ma V_O = 2.7v V_R = 4.6v
I_{OH}	15v		100	µa		V_{IL} .7v V_O = 2.7v V_R = 18v
I_{IH}	15v	0.35	2.0	ma	Typical 4kΩ Slope	V_{IH} = 8.5v V_O = 2.7v
I_{IL}	15v	25		µa	Typical 17.6KΩ Slope	V_{IL} = 0.7v V_O = 2.7v V_R = Open

HEX DIGIT DRIVER

- **MOS to LED digit driver**
- **200 mA sink capability at 0.4 volts**
- **Suitable for pocket calculators**
- **"Chip enable" for extended battery life**
- **High gain Darlington Outputs**

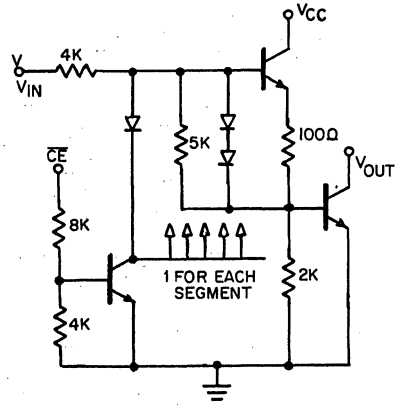


Pin Configuration (Top View)

ITT 502 is a monolithic integrated circuit which provides the interface between MOS integrated circuits and Light Emitting Diode (LED) Digit Displays. The ITT 502 is designed to be used in serially addressed multi-digit displays. This time-multiplexed system, using a segment address and digit scan method of LED drive, minimizes the number of drivers required. This circuit, together with the ITT 503 (segment driver), was designed to operate with two different power supplies.

The first being a battery (VCC) where the voltage may range from 3.5 to 9 volts and supplies the majority of the load currents (display currents). The second (VSS) supply, being a D.C. to D.C. converter or regulator which maintains the voltage between 7 and 9 volts. In order to maximize the voltage from the battery across the load, the ITT 502 output was designed to provide 200 mA with only 0.4V VOL. The "Chip Enable" circuit allows turning the load (display) "off" independently of the input signals.

SCHEMATIC



(Each driver, 6 per package)

Characteristics	Units
VSS (VSS VIN or VCE)	9 V
VCC	9 V
Continuous total power dissipation	800 mW
Storage temperature range	—55 C to 125 C
Operating temperature	0 C to 50 C

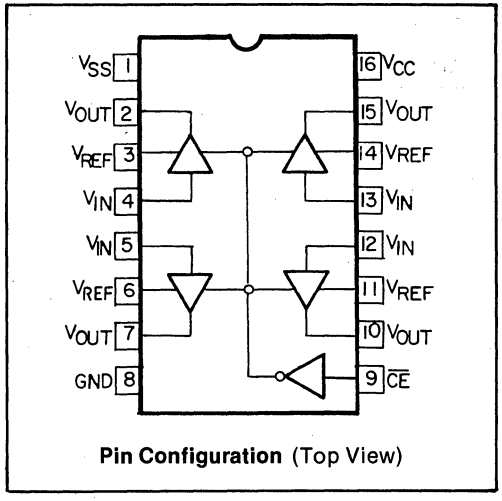
ELECTRICAL CHARACTERISTICS
(Unless otherwise noted $T_A = 25$ C, measurements with respect to GND)

PARAMETER	V ss	V cc	MIN	MAX	UNITS	NOTES	TEST CONDITIONS
I_{OL}	6.5	3.2	200		mA		$V_{IH} = 6.5$ $V_{\overline{CE}} = 0v$ $V_{OL} = 0.4v$
I_{OH}	8,8	8.8		400	µA		$V_{IN} \leqslant 0.9$ $V_{\overline{CE}} = 0v$ $V_{OH} = 8.8v$
I_{OH}	8.8	8.8		400	µA		$V_{IH} = 8.8v$ $V_{\overline{CE}} \geqslant 6.5v$ $V_{OH} = 8.8v$
I_{IH}	8.8	8.8		2.0	mA	Slope typically 4KΩ	$V_{IH} = 8.8v$ $V_{\overline{CE}} = 0v$ V_{OUT} = **Open**
I_{IL}	8.8	Open	15		µA	Slope typically 11KΩ	$V_{IL} = 0.5v$ $V_{\overline{CE}} = 0v$ V_{OUT} = Open
I_{CEL}	8.8	8.8		150	µA	Slope typically 12KΩ	$V_{\overline{CE}} = 0.95v$ $V_{IN} = 0v$ V_{OUT} = Open
I_{CEH}	8.8	8.8	0.40	1.50	mA	Slope typically 8KΩ	$V_{\overline{CE}} = 6.5$ $V_{IN} = 0v$ V_{OUT} = Open

QUAD SEGMENT DRIVER

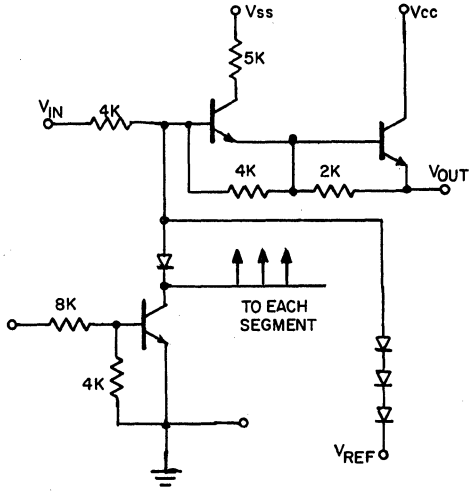
- **MOS to LED segment driver**
- **Constant current source, programmable.**
- **Suitable for pocket calculators**
- **"Chip enable" for extended battery life**
- **High gain Darlington Outputs**

The ITT 503 is a monolithic integrated circuit which provides the interface between MOS integrated circuits and Light Emitting Diode (LED) displays. The ITT 503 is designed to be used in serially addressed multi-digit displays. This time-multiplexed system, using a segment address and digit scan method of LED drive, minimizes the number of drivers required. This circuit, together with the ITT 502 was designed to operated with two different power supplies. The first being a battery, (V_{CC}) where the voltage may vary from 3.5 to 9 volts and supplies the majority of the load currents (display currents). The second, (V_{SS}) supply, being a D.C. to D.C. converter or regulator which maintains the voltage between 7 and 9 volts. By connecting a resistor in series with the V_{OUT} terminal and the LED anode (i.e. resistor across V_{OUT} and V_{REF}) an adequate current source is generated. The voltage across the resistor is equivalent to a diode forward voltage drop (+ 0.6V), thus in order to control 20 mA, a resistor value of 30Ω is required. The "chip enable" circuit allows turning the load (display) "off" independently of the input signals.



Pin Configuration (Top View)

SCHEMATIC



(Each Driver, 4 per package)

ABSOLUTE MAXIMUM RATINGS
(Measurements with respect to GND)

Characteristics	Unit
V_{SS} (V_{SS} V_{IN} or V_{CE})	9 V
V_{CC}	9 V
Continuous total power dissipation	800 mW
Storage temperature range	−55°C to + 125°C
Operating temperature range	0°C to + 50°C

ELECTRICAL CHARACTERISTICS
(Unless otherwise noted T_A = 25 C, measurement with respect to GND)

PARAMETER	V ss	V cc	MIN	MAX	UNITS	TEST CONDITIONS
I_{OL}	6.5	3.2	−20		mA	V_{IN} = 6.5v $V_{\overline{CE}}$ = 1.0v V_{OUT} = 2.2v
I_{OH}	8.8	8.8		−0.3	mA	V_{IN} = 8.8v $V_{\overline{CE}}$ = 6.5v V_{OUT} = 0.0v
$I_{IN\ H}$	7.0	Open		1.5	mA	V_{IN} = 5.0v $V_{\overline{CE}}$ = 0.0v V_{OUT} = 0.0v V_{REF} = Open
I_{INL}	7.0	Open		100	µA	V_{IN} = 1.5v $V_{\overline{CE}}$ = 0.0v V_{REF} = 0.0v
$I_{\overline{CEL}}$	8.8	Open	20		µA	$V_{\overline{CE}}$ = 0.5v V_{IN} = 0.0v
$I_{\overline{CEH}}$	8.8	Open		1.5	mA	$V_{\overline{CE}}$ =6.5 v V_{IN} = 0.0v V_{OUT} = Open

NOTE: IINH — Slope typically 10KΩ

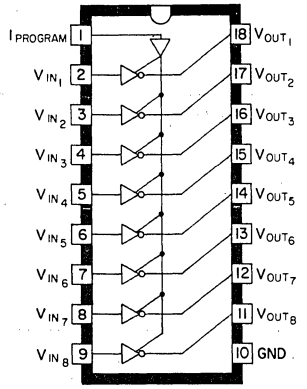
ITT SEMICONDUCTORS

GAS DISCHARGE SEGMENT DISPLAY DRIVER

GAS DISCHARGE SEGMENT DISPLAY DRIVER

- **Segment Drivers**
- **18 Pin Ceramic Package**
- **Programmable Current**
- **.2 to 2.0 mA (Note 2)**
- **90 Volt Operation**

Pin Configuration
(Top View)



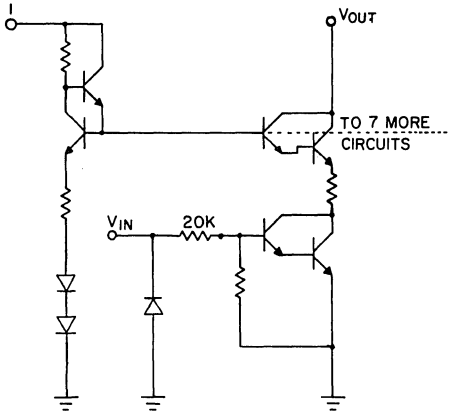
The ITT505 is a monolithic integrated circuit designed to provide the interface to gas discharge type display drivers.

The ITT505 incorporates eight segment drivers with equal segment currents. All eight segment currents are programmed by a single resistor at Pin 1. The segment current may be varied from .2 to 2.0 mA.

The device also incorporates diode clamps on all eight inputs to permit rapid recharging of input capacitor in applications where input signal is capacitively coupled.

Absolute Maximum Ratings

V_{out} .....90 VDC (See Note 1)
V_{in} .....-1.0 to 35 VDC
I_{out}.....3.0mA
Power dissipation.....800mW
Operating Temperature .....0 to 70°C
Storage Temperature .....-55° to 125°C



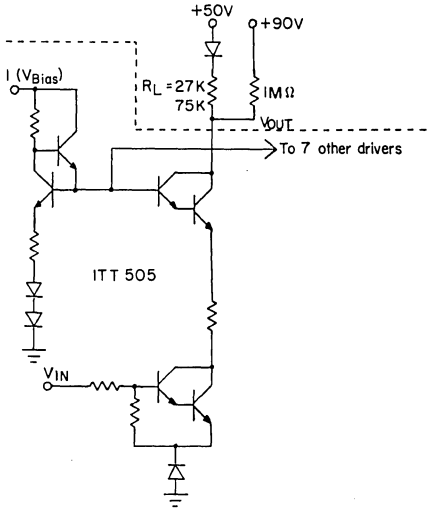
Circuit Schematic

NOTE: Current limiting resistor should be incorporated for testing.

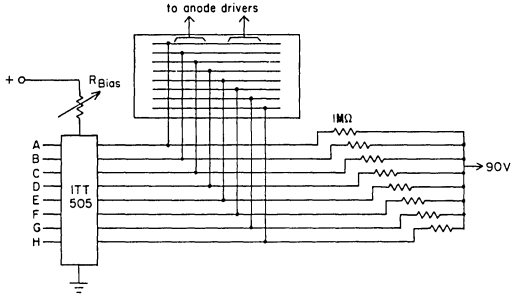
NOTE: Inputs to unloaded stages should be grounded.

ITT505
GAS DISCHARGE SEGMENT DISPLAY DRIVER

Test Circuit



Typical Application

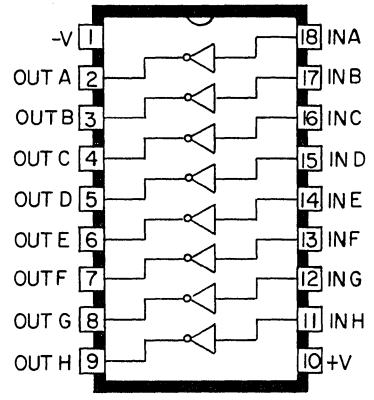


Electrical Characteristics (T_A = 25°C, all voltages with respect to Pin 10)

Parameter	Min	Typ.	Max	Units	Conditions
I_{out}	.2		2.0	mA	V_{in} = 3.5 3V ≤ V_{Bias} ≤ 5V
Vin	3.5				I_{out} = .2 to 2.0mA
V_{Bias}	2.5 5.0	2.8 6.0	3.25 7.0	V V	V_{in} = 8V, I_{out} = .2mA V_{in} = 8V, I_{out} = 2.0mA
V_{in}	8.0	11.0	15.0	V	I_{in} = .5mA I_{in} = -1.0mA
I_{out} Matching		1	10	%	I_{out} = .2mA to 2.0mA
Output Leakage			10	uA	V_{out} = 90V V_{in} = gnd R_L = 1 MΩ

OCTAL DIGIT DRIVER

- **Drivers per package**
- **MOS to LED interface**
- **40ma sink capability at .45 volts Vol**
- **Input current 500uA max. for 40mA sink**



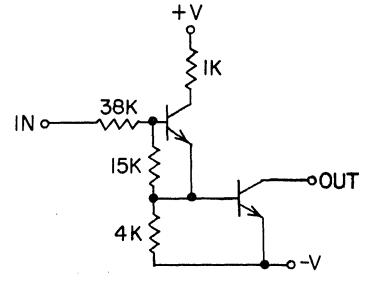
Pin Configuration

The ITT508 is a monolithic integrated circuit which is designed to provide the interface between MOS integrated circuits and Light Emitting Diodes.

The ITT508 is ideally suited for use in serially addressed multidigit displays. This time multiplexed system using a segment address and digit scan method of LED drive, minimizes the drivers required.

The ITT508 when used with the ITT509 requires only two IC packages to drive eight digits, seven segments and one decimal.

The ITT508 contains eight independent drivers, each capable of sinking 40mA with a Vol of .45 volts. The maximum input current of 400uA is all that is required to sink 40mA.



Schematic Diagram

Maximum Ratings)TA at 25°C)

V+ .....10 Volts
Vin..... Vt
Iout 80mA

ELECTRICAL CHARACTERISTICS
(Unless otherwise noted TA = 25°C, all measurements with respect to GND)
(V+ = 10 volts, V- = GND unless otherwise noted)

Parameter	Condition	Limits		Units
		Min.	Max.	
Output Leakage	$I_{in} \leq 25uA$	-	300	uA
Input Current	I_{out} = 40mA V_{in} = V+ *	-	500	uA
Input Current	$I_{out} \leq 300uA$	-	25	uA
Output Voltage	I_{out} = 40mA V_{in} = V+ *	-	.45	Volts
I_S	V+ = 10 volts	-	10.0	mA
I_S	V+ = 5 volts	-	5.0	mA
t_{on}	to 90% I_{out}	-	5.0	u sec
t_{off}	to 10% I_{out}	-	5.0	u sec

* $5V \leq V+ \leq 10V$

OCTAL SEGMENT DRIVER

- 8 Segment Drivers
- MOS to LED Interface
- 500uA Input Current
- Constant Current Source
- Output Current Matched to 15%

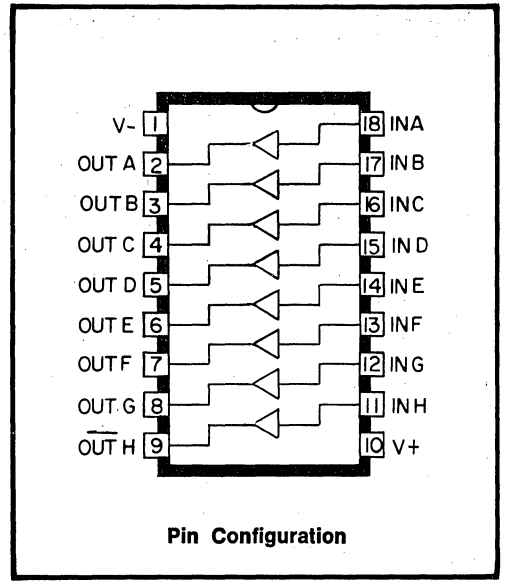
The ITT509 is a monolithic integrated circuit designed to interface MOS circuits and light emitting diode displays.

The ITT509 was designed for use with serially addressed multi-digit displays. The time multiplexed system using a segment address digit scan technique minimizes the number of drivers required.

The ITT509 when used with the ITT508 Octal Digit Driver requires only two IC's to drive eight digits, seven segments and one decimal.

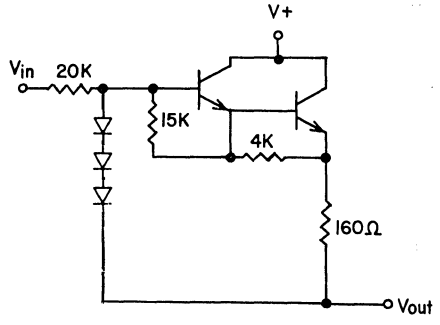
Maximum ratings (TA = 25°C)
V+ .....10 volts
Vin .....V+

PACKAGE 18 PIN DUAL-IN-LINE



Pin Configuration

Schematic Diagram



Electrical characteristics
(T_A 25°C, V+ = 10 VDC, all measurements with respect to GND unless otherwise noted)

Parameter	Condition	Limit		Units
		Min.	Max.	
Output Leakage	$I_{in} \leq 25uA$	—	300	uA
Input Current	$I_{out} = I_{nom}$ $V_{in} = V+$ *	—	500	uA
Input Current	$I_{out} \leq 300uA$	—	25	uA
Differential Output Current (Between drivers)	$V_{in} = V+$ *	—	±15	%
Output Current	$V_{in} = V+$ * $V_{out} = 2V$	3.0		mA
Output Current	$V_{in} = V+$ * $2V \leq V_{out} \leq 9V$	—	5.5	mA
t_{on}	to 90% I_{out}	—	5.0	usec
t_{off}	to 10% I_{out}	—	5.0	usec

*$5V \leq V+ \leq 10V$

SEVEN SEGMENT DRIVER

These circuits are monolithic MOS chips which contain all the electronics required to provide the necessary interface between the G.I. C550 and C540 series of single MOS calculator chips, and the 7-digit segments of an LED display. Designed in p-channel silicon gate MOS, the circuits are designed to run off a single −15V nominal supply rail and are capable of providing typically 8.5mA drive per segment, dependent upon battery voltage. A feature of the design is the very low power dissipation which is typically on 1.8mW per package. Power dissipation is independent of the logic state and thus allows for very simple adjustment of the LED intensity by means of an external resistor in series with the V_{DD} supply rail. All inputs are fully protected against static charge and includes on chip built in pull down resistors.

The circuits are designed for use with the ITT7104 and ITT7105 eight digit drivers to provide a complete LED monolithic interface system between the G.I. C550-554 series of single MOS calculator chips and LED displays.

MAXIMUM RATINGS

V_{DD} (with respect to V_{SS}) .... −20V to +0.3V
Input voltage rating (with respect to V_{SS}) ..... −20V to +0.3V
Storage temperature range.. −55°C to +85°C
Operating temperature range..0°C to +50°C

ELECTRICAL CHARACTERISTICS
V_{DD} = −13.0V to −15.5V, V_{SS} = OV

D.C. Specification

Applicable over the temperature range 0 to +50°C. All voltages are measured with respect to V_{SS} = OV.

Terminology

I_{DDO} Current drain from V_{DD} with inputs at OV.
I_{DD1} Current drain from V_{DD} with inputs open.
I_{OL} Current sourced by an ON output held at $-V_{out}$.
I_{OH} Leakage current from an off output at −9.0V.
I_{IH} Current into an input at OV.

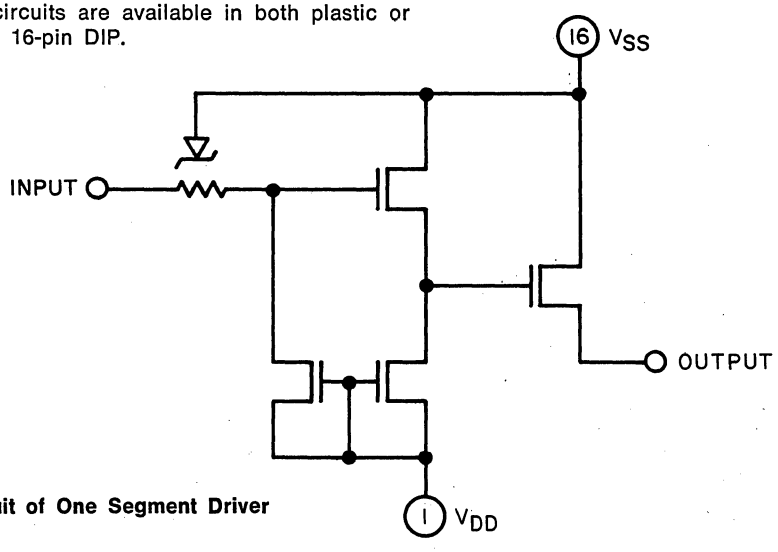
ELECTRICAL CHARACTERISTICS

Parameter	V_{DD}	Min.	Typ.	Max.	Units	Test Conditions
I_{DDO}	−15.5V		—120	—200	μA	V_{in} to all inputs = OV
I_{DD1}	−15.5V		—120	—200	μA	V_{in} to all inputs open circuit
I_{OL}						V_{in} = OV,
	−15.0V	3.1	3.8	4.7	mA	V_{out} = −2.0V
	−15.0V	6.8	8.5	10.2	μA	V_{out} = −6.0V
I_{OH}	−15.5V			—25	μA	V_{in} = OV to all gates not under test.
						Input to gate under test open.
						V_{out} = −9.0V
I_{IH}	−15.5V	8	20	30	μA	V_{in} = OV

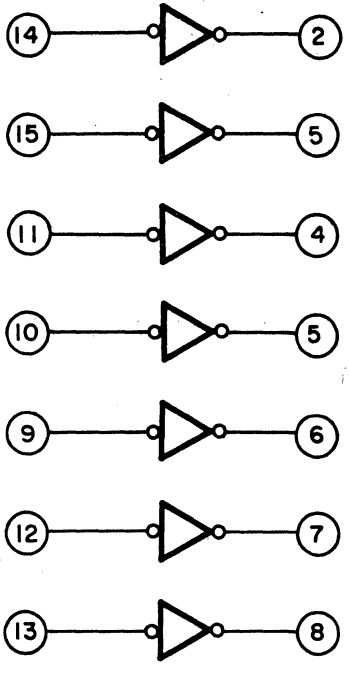
ITT7103
SEVEN SEGMENT DRIVER

Packaging

These circuits are available in both plastic or ceramic 16-pin DIP.



Circuit of One Segment Driver



Pin 16 :—V_{SS}

Pin 1 :—V_{DD}

Logic Diagram - Pin Configuration

LED Segment Driver

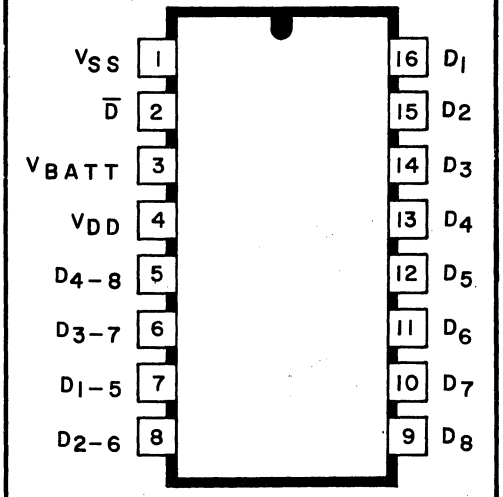
Package 16-pin Dual in-line

EIGHT DIGIT DRIVER

These circuits are monolithic bipolar chips which contain all the electronics required to provide the necessary digit strobe drive interface between the G.I. C550 and C540 series of single MOS calculator chips for LED displays. Designed in bipolar, the circuits are designed to run off two supply rails, i.e. the MOS supply rail, V_{DD} of nominally −15V and a second battery supply rail of between −3.6 and −6.0V. A feature of the circuit arrangement is that the input current is constant regardless of the supply voltages over the specified range. The main features of the design is in the very low power dissipation which is typically only 3.3mW per package total both supplies and the inclusion of built in on chip pull down resistors.

The circuits are designed for use with the ITT7103 series of LED segment drivers to provide a complete LED monolithic interface system between the G.I. C550-554 series of single MOS calculator chips and LED displays.

DUAL-IN-LINE PACKAGE
PIN CONFIGURATION
(TOP VIEW)



TECHNICAL DESCRIPTION

MAXIMUM RATINGS

V_{DD} (with respect to V_{SS}) .... −20V to +0.3V
$V_{Battery}$ (with respect to V_{SS})... −7V to +0.3V
Input voltage rating (with respect to V_{SS}) ..... −20V to +0.3V
Storage temperature range.. −55°C to +85°C
Operating temperature range.. 0°C to +50°C

ELECTRICAL CHARACTERISTICS

V_{DD} = −13.0V to −15.5V

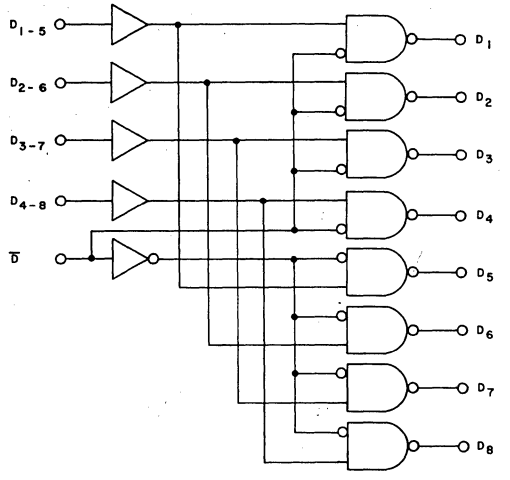
$V_{Battery}$ = 3.6V to −6.0V

V_{SS} = 0V

Packaging

These circuits are available in both plastic and ceramic 16-pin DIP.

Digit Driver Circuit



D.C. Specification

Specification to apply over the temperature range of O°C to +50°C and for all states of the truth table. All voltages are measured with respect to V_{SS} = OV.

Parameter	$V_{Battery}$	V_{DD}	Typ	Max	Units	Test Conditions
V_{OL}	—5.0V	—15.5V	0.9	1.1	V	V_{IH} = OV applied through 3.6 kΩ, I_{OL} = 20mA
I_{OH1}	—5.0V	—15.5V		—50	μA	V_{IH} = OV, V_{OH} = 3.OV
I_{OH}	—5.0V	—15.5V	200	300	μA	V_{IH} = OV
$I_{Battery\ 0}$	—5.0V	—15.5V	—220	—500	μA	V_{IH} = OV, all inputs data and select open
$I_{Battery\ 1}$	—5.0V	—15.5V	—350	—800	μA	V_{IH} = OV, select and any 1 data input = OV
I_{DD}	—5.0V	—15.5V	—100	—300	μA	V_{IH} = OV

Terminology

V_{OL} Output ON voltage.

I_{OL} Load current into an ON output.

I_{OH} Leakage curent into an OFF output biased at V_{OH}.

I_{IH} Current into a high input biased at V_{IH}.

V_{IH} Voltage used for turning an input ON.

$I_{Battery}$ Current drawn by the circuit from $V_{Battery}$.

I_{DD} Current drawn by the circuit from V_{DD}.

TRUTH TABLE

	INPUTS					OUTPUTS							
LOGIC	D	D1-5	D2-6	D3-7	D4-8	D1	D2	D3	D4	D5	D6	D7	D8
PIN NOS.	2	7	8	6	5	16	15	14	13	12	11	10	9
	0	0	0	0	0	1	1	1	1	1	1	1	1
	0	1	0	0	0	0	1	1	1	1	1	1	1
	0	0	1	0	0	1	0	1	1	1	1	1	1
	0	0	0	1	0	1	1	0	1	1	1	1	1
	0	0	0	0	1	1	1	1	0	1	1	1	1
	1	0	0	0	0	1	1	1	1	1	1	1	1
	1	1	0	0	0	1	1	1	1	0	1	1	1
	1	0	1	0	0	1	1	1	1	1	0	1	1
	1	0	0	1	0	1	1	1	1	1	1	0	1
	1	0	0	0	1	1	1	1	1	1	1	1	0

For inputs

0 represents the pin left open circuit.

1 represents the pin taken to a positive potential.

For outputs

0 represents the output turned on and capable of sinking up to 20 mA to ground.

1 represents the output turned off.

ITT SEMICONDUCTORS

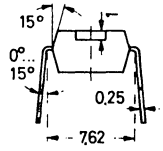
HORIZONTAL DEFLECTION PROCESSOR FOR THYRISTOR (SCR) OUTPUT STAGES

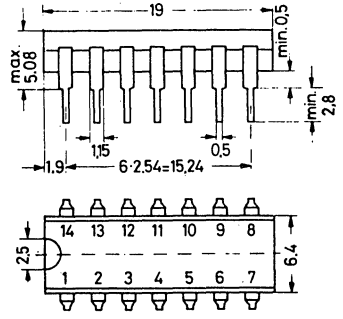
HORIZONTAL DEFLECTION PROCESSOR FOR THYRISTOR (SCR) OUTPUT STAGES

Monolithic integrated circuit for pulse separation and line synchronization in television receivers with thyristor line output stages (SCR). The TBA940 comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic change-over of noise immunity, the line oscillator with frequency range limiter, a phase control circuit, the output stage and a supply voltage stabilizer. It delivers a prepared frame sync pulse for triggering the frame oscillator. Its phase comparator may be switched over for video recording operation. Due to large scale integration only a few external components are needed. Fig. 1 shows the block diagram.

Fig. 2 —
"A" in Plastic Dual In-Line TO-116 package

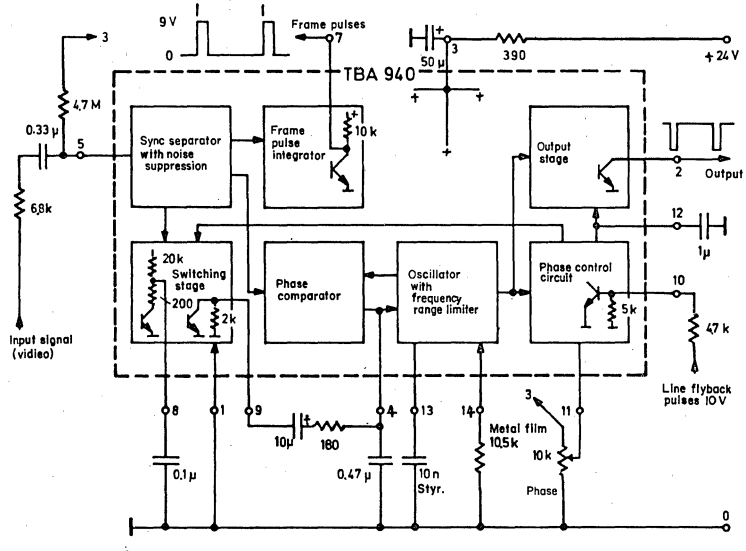
Dimensions in mm





Upon request there is also available a quad in-line version TBA 940 "B".

Fig. 1 — Block diagram and Test Circuit



TBA940
HORIZONTAL DEFLECTION PROCESSOR FOR THYRISTOR (SCR) OUTPUT STAGES

MAXIMUM RATINGS

I_3	Supply current (see Fig. 6)	50mA
I_5	Input current	2mA
V_5	Input voltage	−6V
I_2	Output current	22mA
V_2	Output voltage	12V
I_8	Switch-over current for video recording operation	5mA
V_{11}	Phase adjustment voltage	0 to V_3
I_{10}	Flyback peak pulse current	5 mA
T_{amb}	Ambient temperature	60°C

RECOMMENDED OPERATING CONDITIONS FOR OPERATING CIRCUIT Figs. 4 and 5

I_5	Input current during sync pulse	$-> \mu A$
V_{inpp}	Video input signal	3(1 to 6)V
I_{10}	Input current duing line flyback pulse	0.2 to 2mA
I_8	Switch over current	>2 mA
t_d	Time difference of output signal Pin 2 and line flyback pulse at pin 10	$<20 \mu S$
I_3	Current consumption (see Fig. 6)	40mA
T_{amb}	Ambient temperature range	0 to +60°C

CHARACTERISTICS At T_{amb}=25°C, f_o=15625Hz*) in the test circuit Fig. 1

V_7	Amplitude of frame pulse	>8V
t_7	Frame pulse duration	$>150 \mu s$
R_{out7}	Output resistance (high-state) at terminal 7	10(7.5 to 13)kΩ
t_2	Output pulse duration	4 to 8μs
R_{out2}	Output resistance (high-state) at terminal 2. See fig. 3	≈5.6Ω
V_{2res}	Output voltage at I_2=20mA	<0.55V
f_o	Oscillator frequency at $C_{13/1}$=10nf and $R_{14/1}$=10.5K	15625±1562Hz
$\pm\Delta f_p$	Frequency pull-in range	400 to 800Hz
$\pm\Delta f_H$	Frequency hold-in range	400 to 800Hz
df_o/dt_d	Slope of phase comparator control loop	2kHz/μs
dt_d/dt_p	Gain of phase control	20
t_p	Adjustable phase shift between leading edge of video signal and line flyback pulse	see Fig. 3
t_p	Phase shift at t_d=6μS and Pin 11 open	1.6(0.5 to 2.7)μS

* By modifying the resistor of the oscillator at pin 14 the TBA940 can also be used for other line frequencies.

Design and Operation of the TBA940

The sync separator separates the synchronizing pulses from the composite video signal. The noise suppression circuit which does not need any external components comprises an integrating and differentiating network which cleans the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limiting of the synchronizing signal, and is available at terminal 7. The RC network normally required between the sync separator and frame oscillator is no longer needed.

The line oscillator frequency is set by a 10nF capacitor (Polystyrene, pin 13) which is charged and discharged periodically by two internal current sources. The external resistor at pin 14 defines the charging current and consequently, in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator (see Fig. 3) with the line sync pulses. Simultaneously an AFC voltage is generated influencing the oscillator frequency. A frequency range limiter restricts the frequency hold-in range to ±800Hz. The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stages. The correct phase position and hence the horizontal position of the picture can be adjusted by a 10kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g. due to non-symetrical picture tube, should not be corrected by the phase potentiometer. In any case the flyback pulse must overlap the sync pulse on both edges. (See Fig. 3).

The switching stage has an auxiliary function. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is paralleled to the integrated 2kΩ resistor at terminal 9 and ground. Thus the time constant of the filter network at terminal 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50Hz. This arrangement ensures distortion-free operation.

For video recording operation this automatic switchover can be blocked by a positive current fed into terminal 8, e.g. via a resistor connected to pin 3. It can also be useful to connect a resistor of about 680Ω or 1kΩ between pin 9 and ground. The capacitor at terminal 4 may be lowered, e.g. to 0.1μF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched out, when changing from VTR to TV or vice versa.

The short circuit proof output stage delivers at terminal 2 output pulses of duration and polarity suitable for driving the output driver stage. If the supply voltage goes off (e.g. by switching off the A.C. voltage) a built-in protection circuit takes care to provide defined line frequency pulses down to V_3=4V and shuts off when V_3 gets below 4V preventing pulses of undefined duration and frequency. Vice versa if the supply voltage rises, defined pulses in duration and frequency will appear at the output terminal when V_3 reaches 4.5V. In the range between V_3=4.5V and full supply voltage the shape and frequency of the output pulse are nearly constant.

Fig. 3 — Phase relations of the TBA940. The line flyback pulse overlaps the video signal sync pulse on both edges.

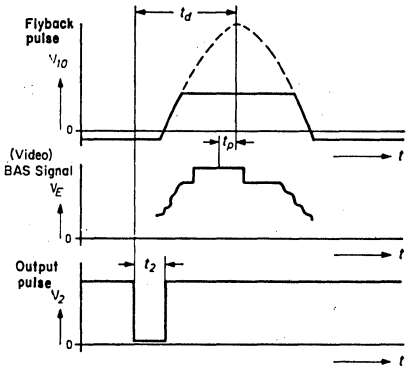
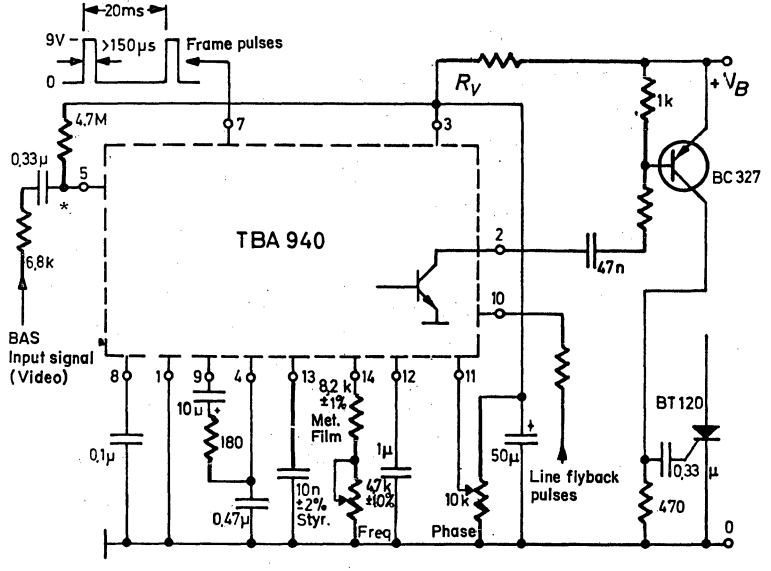


Fig 4: Operating circuit



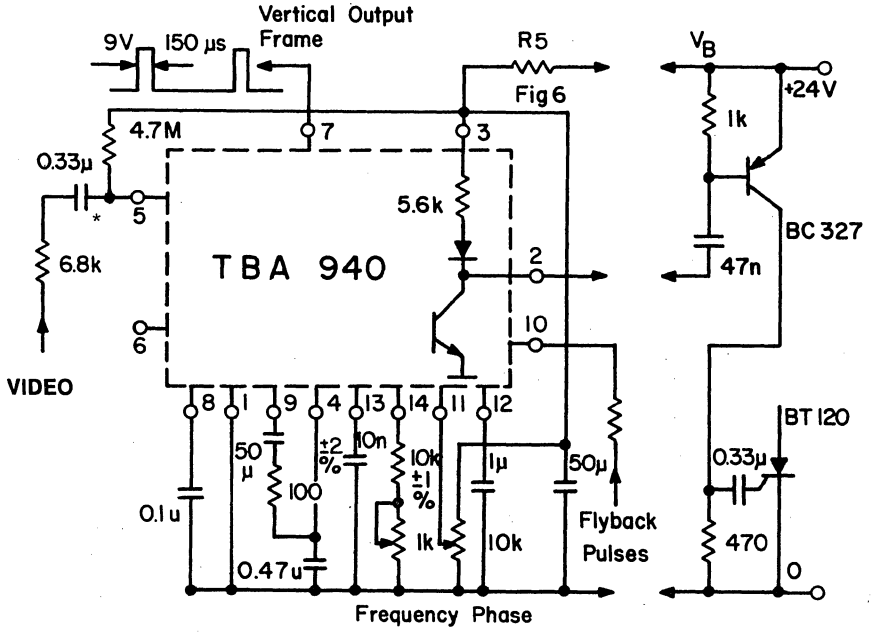


Fig 5: Another possibility for the line frequency adjustment

*** Input circuit should be optimised for particular design of TV receiver.**

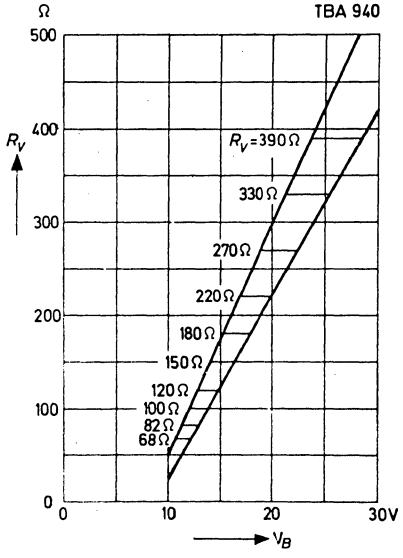


Fig. 6 — Graph for determining series resistance R_S.

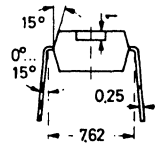
ITT SEMICONDUCTORS

HORIZONTAL DEFLECTION PROCESSOR FOR TV RECEIVERS

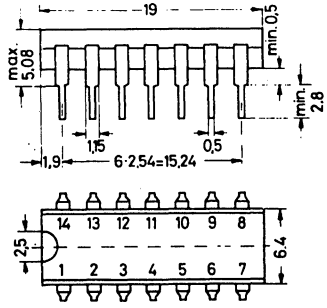
Monolithic integrated circuits for pulse separation and line synchronization in television receivers with transistor and tube output stages. Each circuit comprises the sync-separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic change-over for noise immunity, the line oscillator with frequency range limiter, a phase control circuit, the output stage and a supply voltage stabilizer. The circuit delivers a prepared frame sync pulse for triggering the frame oscillator. The phase comparator may be switched over for video recording operation. Due to large scale integration very few external components are needed. Fig. 1 shows the block diagram.

The TBA950 is available in two groups with different output pulse widths.

Fig. 2—
"A" in Plastic Dual In-Line TO-116 package

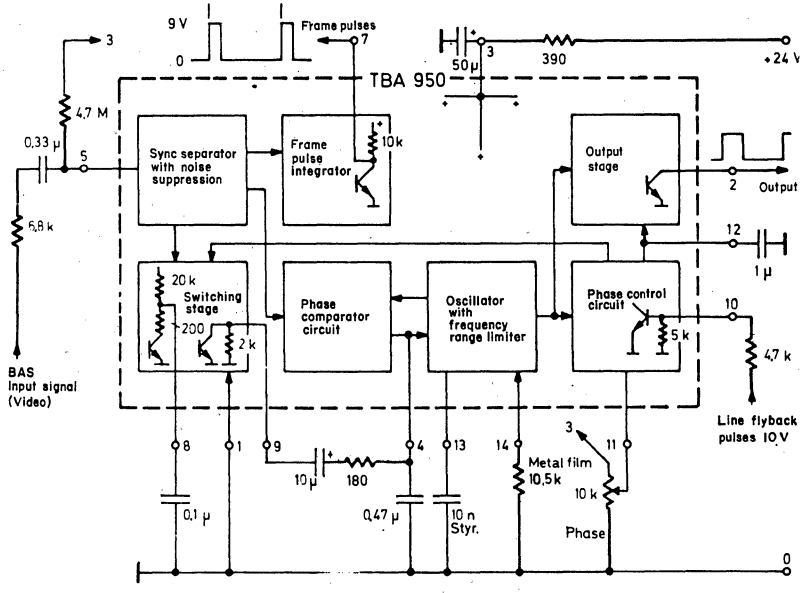


Dimensions in mm



Upon request there is also available a quad in-line version TBA 950 "B".

Fig. 1 — Block diagram and Test Circuit



TBA950
HORIZONTAL DEFLECTION PROCESSOR FOR TV RECEIVERS

MAXIMUM RATINGS

I_3	Supply current (see Fig. 6)	50mA
I_5	Input Current	2mA
V_5	Input voltage	−6V
I_2	Output current	22mA
V_2	Output voltage	20V
I_8	Switch-over current for video recording operation	5mA
V_{11}	Phase adjustment voltage	0 to V_3
I_{10}	Flyback peak pulse current	5mA
T_{amb}	Ambient temperature	60°C

RECOMMENDED OPERATING CONDITIONS
for operating circuit Fig. 4 and 5

I_5	Input current during sync pulse	$>5\mu A$
$V_{5\ pp}$	Video input signal	3(1 to 6)V
I_{10}	Input current during line flyback pulse	0.2 to 2mA
I_8	Switch over current	>2mA
t_d	Time between leading edge of the output signal and the middle of the flyback-pulse at pin 10	$<20\mu S$
I_3	Current consumption (see Fig. 6)	40mA
T_{amb}	Ambient temperature range	0 to +60°C

CHARACTERISTICS
at T_{amb} = 25°C, to= 15,625Hz* in the test circuit of Fig. 3

V_7	Amplitude of frame pulse	>8V
t_7	Frame pulse duration	$>150\mu s$
$R_{out\ 7}$	Output resistance at Pin 7 (High state)	10(7.5 to 13)KΩ
	Duration of output pulse	
t_2	TBA950-1	22 to 26μs
t_2	TBA950-2	25 to 28μs
$R_{out\ 2}$	Output resistance at Pin 2 (High state) see Fig. 3	≈5.6KΩ
$V_{2\ res}$	Output voltage at I_2 = 20mA.	<0.55V
f_o	Oscillator frequency at $C_{13/1}$ = 10nF and $R_{13/1}$ = 10.5KΩ	15,625±1562Hz
$\pm\ \Delta f_p$	Frequency pull-in range	400 to 800Hz
$\pm\ \Delta f_H$	Frequency hold-in range	400 to 800Hz
df_o/dt_d	Slope of phase comparator control loop	2KHz/μS
dt_d/dt_p	Gain of phase control	20
t_p	Adjustable phase shift betwen leading edge of video signal and line flyback pulse	See Fig. 3
t_p	Phase shift at t_d = 6μs, Pin 11 open	1.6(0.5 to 2.7)μS

*By modifying the resistor of the oscillator at pin 14 the TBA950 can also be used for other line frequencies.

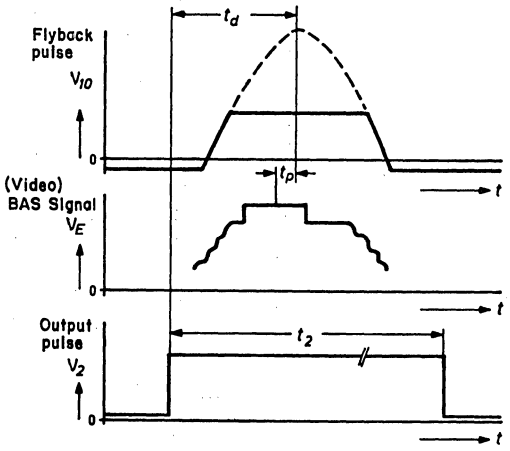
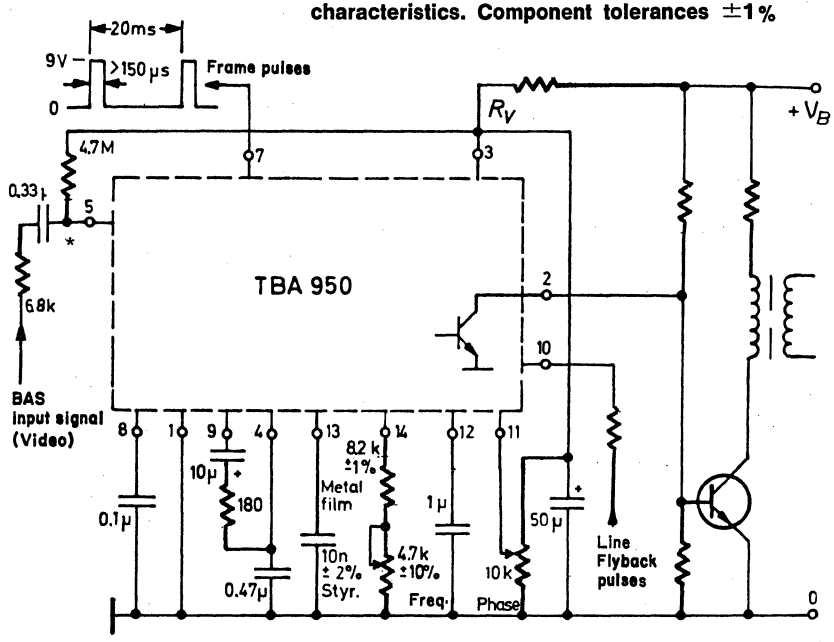


Fig. 3—Phase relations of the TBA950. The clipped line flyback pulse must overlap the video signal. Sync. pulse.

Fig. 4—Block diagram and test circuit for the characteristics. Component tolerances ±1%



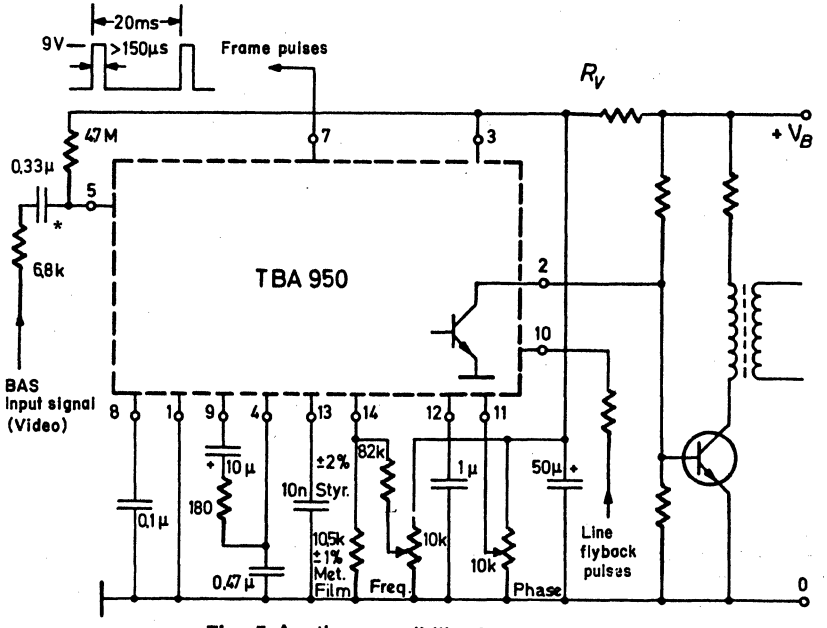


Fig. 5 Another possibility for line frequency adjustment

***Input circuit should be optimized for particular design of TV receiver.**

Design and Operation of the TBA950

The sync separator separates the synchronizing pulses from the composite video signal. The noise suppression circuit which does not need any external components comprises an integrating and differentiating network which cleans the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limiting of the synchronizing signal, and is available at terminal 7. The RC network normally required between the sync separator and frame oscillator is no longer needed.

The line oscillator frequency is set by a 10nF capacitor (Polystyrene, Pin 13) which is charged and discharged periodically by two internal current sources. The external resistor at Pin 14 defines the charging current and consequently in conjuction with the oscillator capacitor, the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator (see Fig. 3) with the line sync pulses. Simultaneously an AFC voltage is generated influencing the oscillator frequency. A frequency range limiter restricts the frequency hold-in range to ±800Hz. The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stages. The correct phase position and hence the horizontal position of the picture can be adjusted by a 10kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (Pin 2) is constant. Any larger displacements of the picture, e.g. due to non-symetrical picture tube, should not be corrected by the phase potentiometer. In any case the flyback pulse must overlap the sync pulse on both edges (see Fig. 4).

The switching stage has an auxiliary function. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is paralleled to the integrated 2kΩ resistor at terminal 9 and ground. Thus the time constant of the filter network at terminal 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50Hz. This arragement ensures distortion-free operation.

For video recording operation this automatic switchover can be blocked by a positive current fed into terminal 8, e.g. via a resistor connected to Pin 3. It can also be useful to connect a resistor of about 68Ω or 1KΩ between Pin 9 and ground. The capacitor at terminal 4 may be lowered, e.g. to 0.1μF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched out when changing from VTR to TV or vice versa.

The short circuit proof output stage delivers at terminal 2 output pulses of duration and polarity suitable for driving the output driver stage. If the supply voltage goes off (e.g. by switching off the A.C. voltage) a built-in protection circuit takes care to provide defined line frequency pulses down to $V_3 = 4V$ and shuts off when V_3 gets below 4V preventing pulses of undefined duration and frequency. Vice versa if the supply voltage rises, defined pulses in duration and frequency will appear at the output terminal when V_3 reaches 4.5V. In the range between $V_3 = 4.5V$ and full supply voltage, the shape and frequency of the output pulses are nearly constant.

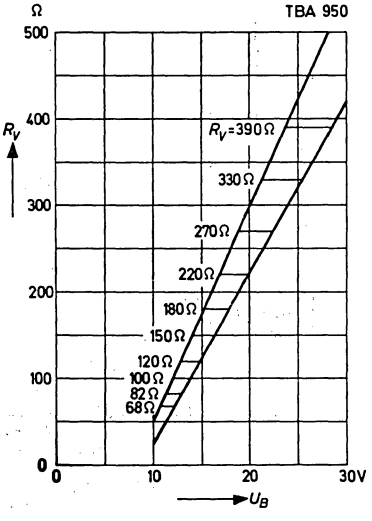
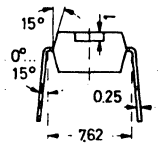


Fig. 6—Graph for determining series resistance P_S

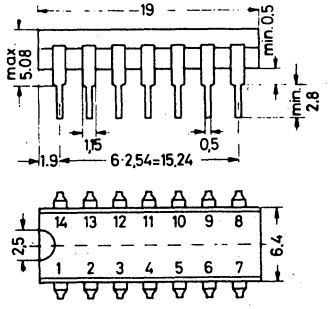
INTEGRATED FM/IF AMPLIFIER AND DEMODULATOR

The monolithic integrated FM/IF amplifier TBA 120 S is designed specifically for use in the sound IF part of television receivers and the FM/IF part of radio receivers. It comprises a broadband symmetrical amplifier and a coincidence circuit for the demodulation. For the volume control, a potentiometer may be connected between pin 5 and ground. Since the potentiometer carries DC only the leads to and from the potentiometer will not be affected by hum; remote operation thus presents no difficulty. The gain is 68 dB and AM rejection ratio 55 dB. The TBA 120 S has excellent limiting properties, and needs only very few external components. The frequency characteristic of the demodulator curve shows excellent stability. The permitted supply voltage range is 6 . . . 18 V.
Pin 3 is the collector and pin 4 the base of an additional transistor suitable for use as an AF preamplifier or as a switching transistor for treble cut by means of an RC combination. An internal 12 V Zener diode connected to terminal 12 may be used for stabilizing the supply voltage for the TBA 120 S or for other stages. Max. Zener current 15 mA.

Fig. 2—
"A" in Plastic Dual In-Line TO-116 package



Dimensions in mm



Upon request there is also available a quad in-line version TBA 120 S "B"

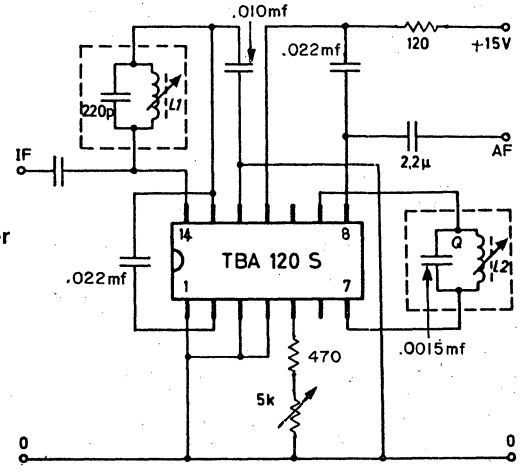


Fig. 1: Application as 5.5 MHz sound IF amplifier

In connection with the integrated output resistor R8/11 = 2.6 kΩ the 22 nF capacitor between pins 8 and 11 determines the time constant of the de-emphasis.

All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	V_{11}	18	V
Voltage at pin 5	V_5	4	V
Current into pin 3	I_3	5	mA
Current into pin 4	I_4	2	mA
Resistor parallel to pins 13 and 14	$R_{13/14}$	1	kΩ
Operating current of the Z-diode permanent	I_{12}	15	mA
1 min max.	I_{12}	20	mA
Power dissipation permanent	P_{tot}	400	mW
1 min max.	P_{tot}	500	mW
Ambient operating temp. range	T_{amb}	−15...+70	°C
Storage temperature range	T_S	−40...+125	°C

Characteristics
for $V_{11} = 12$ V, $f_{in} = 5.5$ MHz, $T_{amb} = 25$ °C

Supply voltage range	V_{11}	6...18	V
Current consumption pin 5 open	I_{11}	14 (10...18)	mA
pin 5 grounded	I_{11}	16 (12...20)	mA
Frequency range	f_{in}	0...12	MHz
IF voltage gain	G_V	68	dB
IF output voltage in case of limitation	V_{6pp}, V_{10pp}	250	mV
AF output voltage for $\Delta f_{in} = \pm 50$ kHz, $V_{in} = 10$ mV, $f_{AF} = 1$ kHz, $Q = 45$, $k = 4$ %	V_8	1.1	V
for $\Delta f_{in} = \pm 25$ kHz, $V_{in} = 10$ mV, $f_{AF} = 1$ kHz, $Q = 20$, $k = 1$ %	V_8	0.55	V
Input voltage for start of limitation for $\Delta f_{in} = \pm 50$ kHz, $f_{AF} = 1$ kHz, $Q = 45$	V_{in}	30 (< 60)	μV
Input impedance	Z_{in}	40 kΩ || 4.5 pF (>15 kΩ || < 6 pF)	
Output resistance	$R_{8/11}$	2.6	kΩ

Volume control range	$\frac{V_8\ (P = 5\ k\Omega)}{V_8\ (P = 0)}$	70	dB
DC level of output signal at $V_{in} = 0$	$V_{8=}$	7.3	V
AM rejection ratio for $\Delta f_{in} = \pm 50$ kHz, $V_{in} = 500\ \mu V$, $f_{AF} = 1$ kHz, $m = 30\ \%$	α'	55 (> 45)	dB
Resistance of potentiometer for −1 dB output voltage decrease	P	3.7 (< 4.7)	kΩ
Voltage at pin 5 for −1 dB output voltage decrease	V_5	2.4 (< 2.6)	V
Resistance of potentiometer for −70 dB output voltage decrease	P	1.4 (> 1)	kΩ
Voltage at pin 5 for −70 dB output voltage decrease	V_5	1.3	V

Characteristics of Integrated Components
at pins 4, 3, and 12

Operating voltage of Z-diode at $I_{Z12} = 5$ mA	V_{Z12}	12 (11.2 . . . 13.2)	V
Dynamic differential resistance	r_{zi}	30	Ω
Collector emitter breakdown voltage at $I_3 = 500\ \mu A$	$V_{3/1/0}$	> 13	V
DC current gain at $I_3 = 1$ mA	h_{FE}	> 30	
Thermal resistance die to ambient air	$R_{th\ A}$	< 120	°C/W

The integrated circuit TBA 120 S is delivered in 4 groups. Depending on the group a decrease of 30 dB requires a resistor from pin 5 to ground as indicated in the table below. The No. of the group is printed on the IC.

Group	II	III	IV	V	
P	1.9 . . . 2.2	2.1 . . . 2.5	2.4 . . . 2.9	2.8 . . . 3.3	kΩ

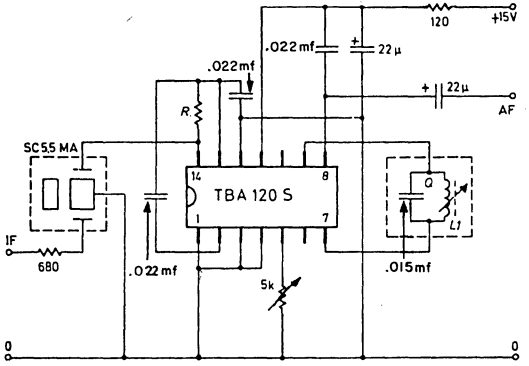


Fig. 2: Operating circuit using a ceramic filter (Murata)

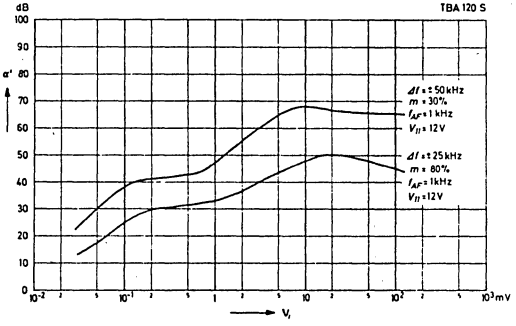


Fig. 3: AM rejection ratio versus input voltage

For good far-off selectivity the ceramic filter should be combined with an *LC* filter.

Frequency	Filter	Resistor *R*
10.7 MHz	SFC 10.7 MA	300 . . . 390 Ω
5.5 MHz	SFC 5.5 MA	560 . . . 680 Ω
4.5 MHz	SFC 4.5 MA	1000 . . . 1200 Ω

Fig. 4: Internal circuitry

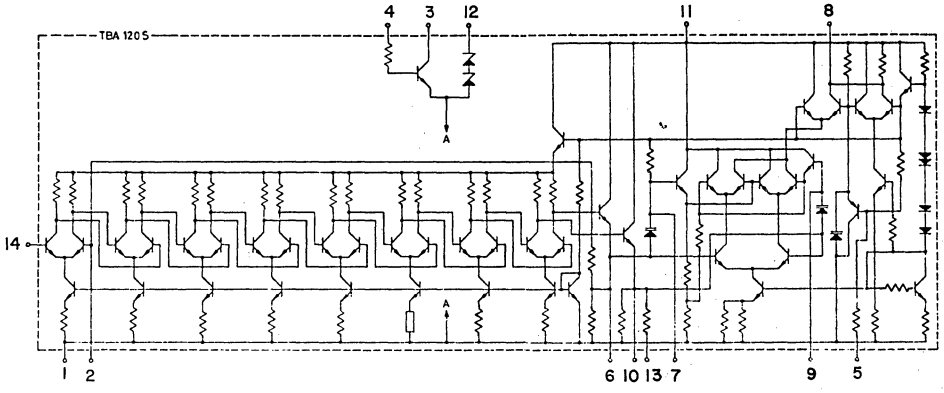


Fig. 5:
Output level versus resistance from pin 5 to ground

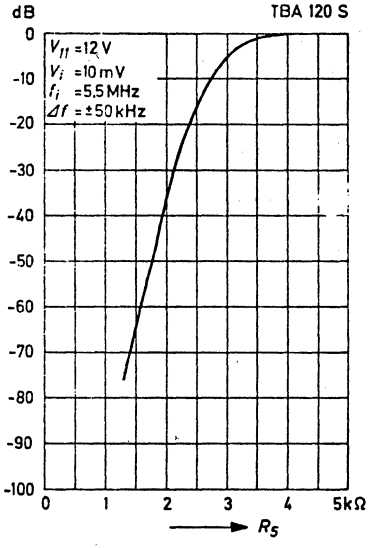


Fig. 6:
Output level versus voltage at pin 5

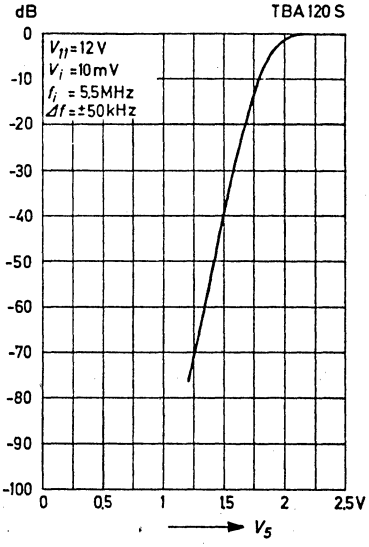


Fig. 7:
AF output voltage versus supply voltage

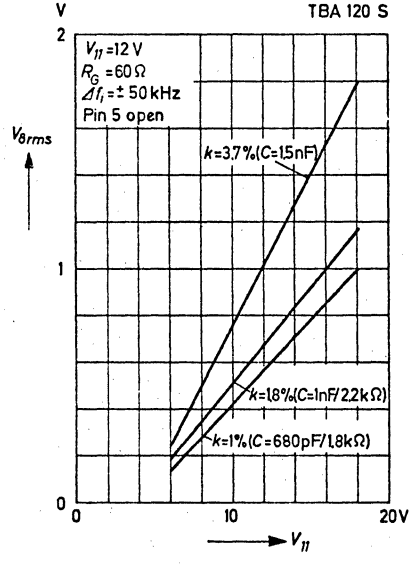
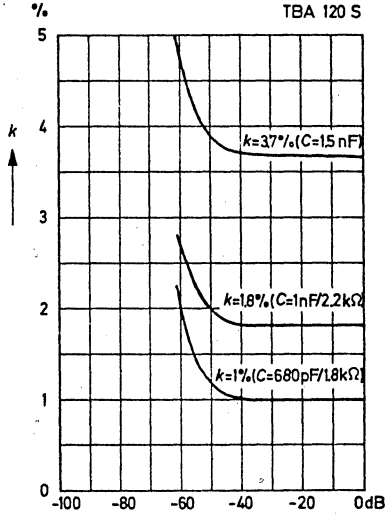


Fig. 8:
Distortion factor versus output level



TV AUTOMATIC FINE-TUNING CIRCUIT

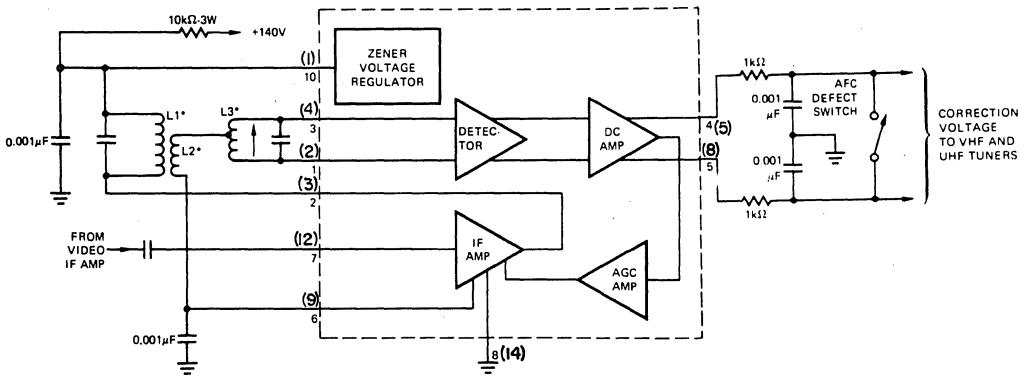
- **HIGH SENSITIVITY**
- **25kHz MAX. FREQUENCY DEVIATION**
- **INTERNAL VOLTAGE REGULATOR**
- **INTERNAL AGC**

GENERAL DESCRIPTION—The ITT3064 is a TV automatic fine-tuning linear integrated circuit constructed on a single chip. It combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level I.F. amplifiers can now achieve tuning accuracies of ±25 kHz due to the ITT3064's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... Note 2
Internal Power Dissipation (Note 3)... 700 mW
Detector Differential Voltage (V_{1-3}) .....±10V
Detector Input Voltage Range
(V_1, V_3) ..... +5V, −6V
I.F. Amp Output (V_2) .....+20V, OV
Bias Voltage (V_6) ..... +2V, OV
Storage Temperature Range −65°C to +150°C
Operating Temperature Range −40°C to +85°C
Lead Temperature (soldering,
60 seconds) ..... 300°C

BLOCK DIAGRAM



The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.

Metal Package, Pin 9— no connection
Plastic Package, Pins 6, 7, 10, 11, 13 — no connection

NOTES:

1. All voltages referenced to V except as noted.
2. V terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
3. Derate linearly at 5.6 mW/°C for ambient temperatures above +25°C.

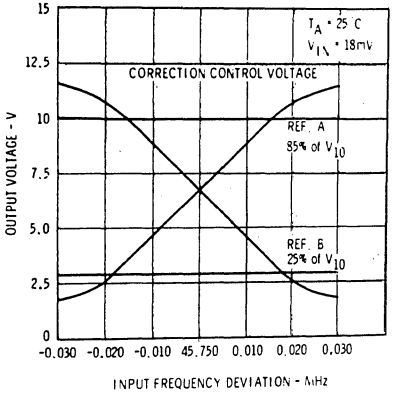
ELECTRICAL CHARACTERISTICS

(V_{CC} = +30 V, R_S = 1.5 kΩ, T_A = 25°C unless otherwise specified)

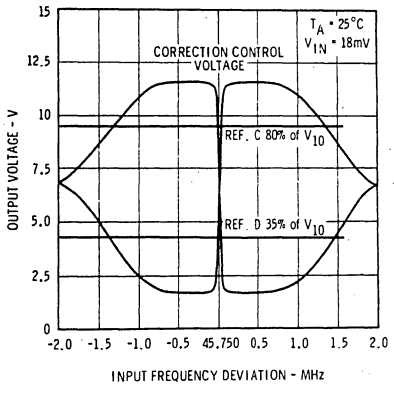
PARAMETER	Min.	Typ.	Max.	Units	CONDITIONS
Power Consumption	130	140	150	mW	T_A = +25°C
		135	150	mW	T_A = −25°C
		145	150	mW	T_A = +85°C
Supply Current — 1	4.0	6.5	9.5	mA	V = +10.5 V
Regulated Supply Voltage — V	10.9	11.8	12.8	V	
Quiescent Operating Voltage —1_2	1.0	2.0	4.0	mA	
Quiescent					
Operating Voltages — V_4, V_5	5.0	6.9	8.0	V	
Output Offset Voltage — (V_4 —V_5)	−1.0	0	1.0	V	
Input Admittance — Y_{11}		0.41+j1.0		mmho	f = 45.75 MHz
Reverse Transfer Admittance — Y_{12}		0+j3.4		μmho	f = 45.75 MHz
Forward Transfer Admittance — Y_{21}		24.5−j29		mmho	f = 45.75 MHz
Output Admittance — Y_{22}		0.04+j0.9		mmho	f = 45.75 MHz
Correction Control Voltage — V_4 (Test Circuit 1)					V_{IN} = 18 mV RMS f_O = 45.750 MHz Δf as listed (MHz)
	85			%V+	−0.030
			25	%V+	+0.030
	80			%V+	—0.900
			35	%V+	+0.900
			80	%V+	−1.500
	35			%V+	+1.500
Correction Control Voltage — V_5 (Test Circuit 1)					V_{IN} = 18 mV RMS f_O = 45.750 MHz Δf as listed (MHz)
			25	%V+	−0.030
	85			%V+	+0.030
			35	%V+	—0.900
	80			%V+	+0.900
	35			%V+	−1.500
			80	%V+	+1.500

TYPICAL PERFORMANCE CURVES

Narrow- Band Dynamic Control Voltage Characteristics

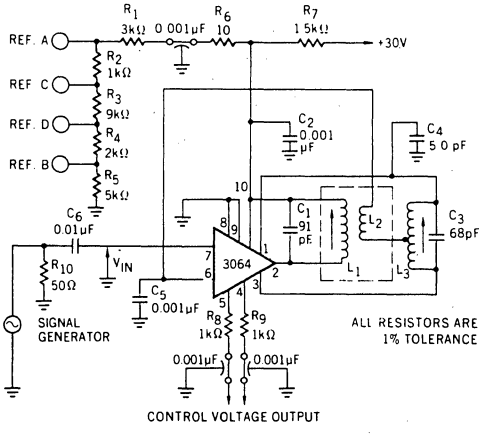


Wide-Band Dynamic Control Voltage Characteristics



See Test Circuit 1

Test Circuit 1
Correction Voltages



NOTE: Parts placement is critical. Use P.C. board layout on last page for best results.

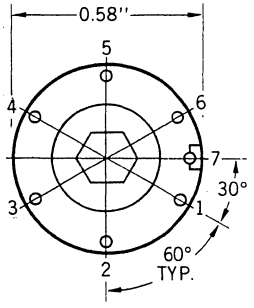
connections shown for metal can only

L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.

L_2 tertiary winding wound on L_1 coil form

L_3 is aligned for zero differential output between terminals 4 and 5 at f_o = 45.750 MHz

COIL FORM BASE TERMINAL DIAGRAM



ITT3064
TV AUTOMATIC FINE-TUNING CIRCUIT

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 — Discriminator Primary: 3 1/6 turns; #20, Enamel-covered wire—close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_0 = 120 at f_0 = 45.75 MHz.
Start winding at Terminal #6, finish at Terminal #1. See Notes below.

L_2 — Tertiary Windings: 2 1/6 turns; #20 Enamel-covered wire—close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See notes below.

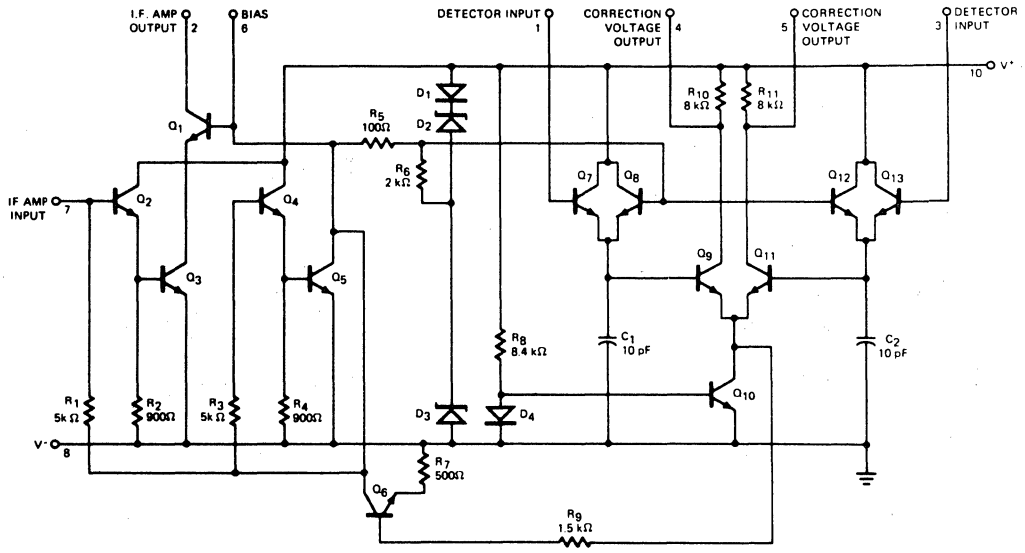
L_3 — Discriminator Secondary: 3 1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180μH; Q_0 = 150 at f_0 = 45.75 MHz.

Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

NOTES:

1. Coil Forms; Cylindrical; 0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   :Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

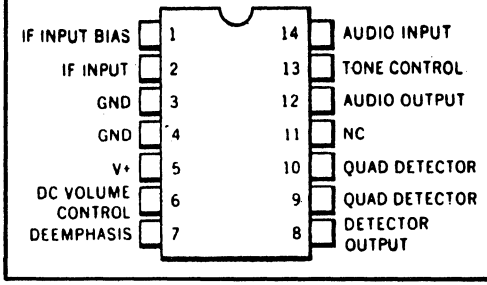
ITT3064 Equivalent Circuit



TV/FM SOUND SYSTEM

- **DC Volume Control Eliminates Need For Shielded Cables**
- **Excellent AM Rejection 50dB Typical at 4.5 MHz**
- **Differential Peak Detector Requires Only One Single-Tuned Coil**
- **Internal Zener Diode Regulated Supply**
- **Low Harmonic Distortion**

CONNECTION DIAGRAM
(TOP VIEW)



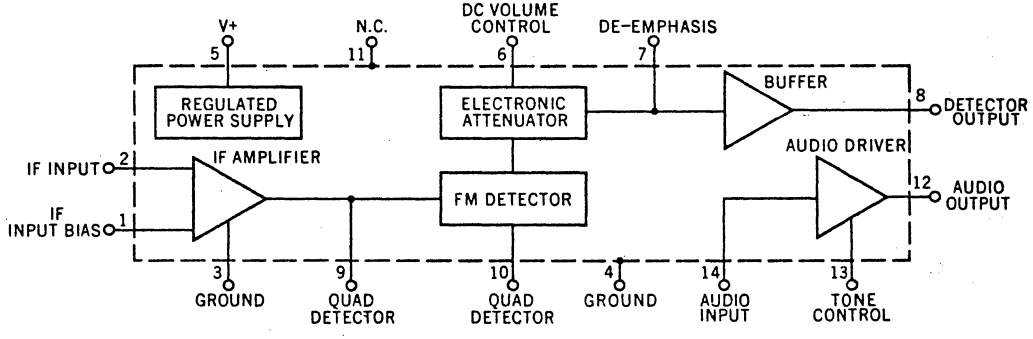
Connection Diagram (Top View)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Supply Voltage	Note 1
Internal Power Dissipation (Note 2)	670mW
Power Supply Current	50 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 seconds)	300°C

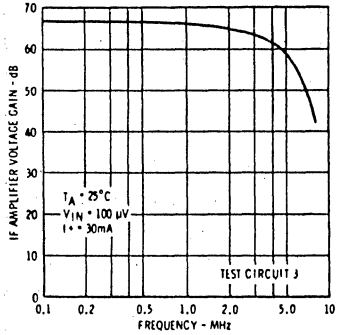
The ITT3065 Monolithic TV/FM Sound System consists of a Multistage Limiting IF Amplifier, DC Gain (Volume) control, FM Detector, and an Audio Driver constructed in a single silicon chip using the planar epitaxial process. Excellent sensitivity, high AM rejection and an internally regulated power supply coupled with low external component requirement makes the ITT3065 suitable for a wide varity of applications including TV Sound Channels, Line Operated and Automobile FM Radios and Mobile Communications Equipment.

BLOCK DIAGRAM

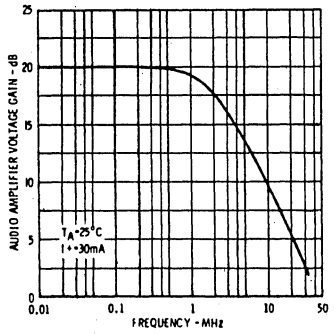


TYPICAL PERFORMANCE CURVES

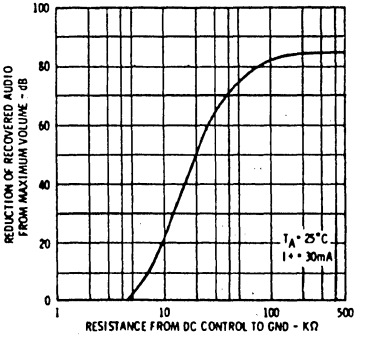
FREQUENCY RESPONSE OF IF AMPLIFIER SECTION



FREQUENCY RESPONSE OF AUDIO AMPLIFIER SECTION



AUDIO GAIN REDUCTION VERSUS DC VOLUME CONTROL RESISTANCE



NOTES
1. V^+ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
2. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly 8.3 mW/°C for the Ceramic DIP.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I = 30 mA unless otherwise specified)

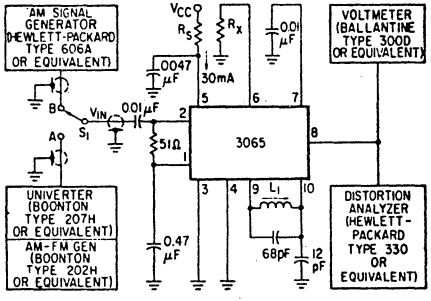
PARAMETER	Test Circuit	Min.	Typ.	Max.	Units	Conditions
STATIC CHARACTERISTICS						
Zener Regulating Voltage (V_5)		10.5	11.5	12.5	Volts	
Supply Current (I_5)		10	16	24	mA	V_{Supply} = 9.0 V
Internal Power Dissipation		343	370	400	mW	I = 33mA
Voltage at IF Input Vias (V_1)			2.0		Volts	
Voltage at DC Volume Control (V_6)			4.8		Volts	
Voltage at De Emphasis (V_7)			6.1		Volts	
Voltage at Quad Detector (V_9)			3.7		Volts	
Voltage at Audio Output (V_{12})		4.0	5.1	5.8	Volts	
DYNAMIC CHARACTERISTICS						
IF AMPLIFIER Input Limiting Voltage at −3dB point	1		200	400	μV	(f_o = 4.5 MHz, FM±25 KHz at 400 Hz, V_{IN} = 100μV)
AM Rejection	1	40	50		dB	AM = 30% at 4.5 MHz
IF Transconductance Magnitude Phase Angle			500 46		mmho degrees	f = 4.5 MHz
Feedback Capacitance			≤0.02		pF	f = 1.0 MHz, Pin 2 to Pin 9
Input Impedance Components						f = 4.5 MHz, Pin 1 to Pin 2

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I = 30 mA unless otherwise specified)

PARAMETER	Test Circuit	Min.	Typ.	Max.	Units	Conditions
Parallel Input Resistance			17		kΩ	
Parallel Input Capacitance			4.0		pF	
Output Impedance Components						f = 4.5 MHz, Pin 9 to Ground
Parallel Output Resistance			3.25		kΩ	
Parallel Output Capacitance			75		pF	
DETECTOR						(f_o = 4.5 MHz, FM = ±25kHz at 400 Hz, V_{IN} = 100 mV)
Recovered AF Voltage	1	0.5	0.75		Vrms	
Total Harmonic Distortion	1		0.9	2.0	%	
Output Resistance						
De emphasis Output			7.5		kΩ	
Detector Output			300		Ω	
ATTENUATOR						
Max. Attenuation	1	60	80		dB	R_X = ∞
Max. Play-through Voltage*	1		0.075	1.0	mV	R_x = ∞
AUDIO AMPLIFIER						
Voltage Gain	2	17.5	20		dB	V_1 = 0.1 Vrms, f = 400 Hz
Total Harmonic Distortion	2		1.5		%	V_o = 2 Vrms, f = 400Hz
Undistorted Output Voltage	2	2.0	2.5		Vrms	THD = 5% f = 400Hz
Input Resistance			70		kΩ	f = 400Hz
Output Resistance			270		Ω	f = 400Hz

*Play-through voltage is the unwanted signal, measured at the detector output, when the volume control is set for minimum output.

Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.



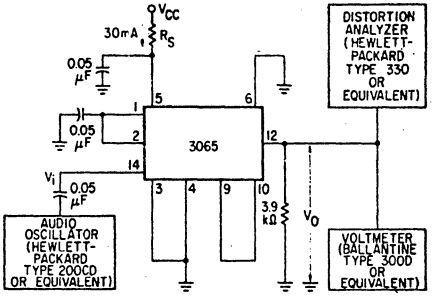
PINS 11, 12, 13, 14 NO CONNECTION

*L_1 = 16μH NOMINAL

$Q_{(UNLOADED)}$ = 50

TEST CIRCUIT 1

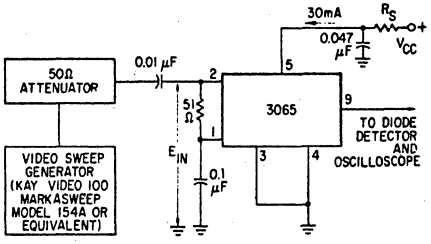
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 2

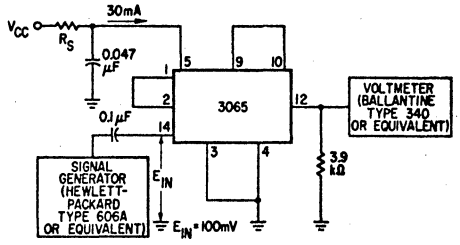
IF AMPLIFIER SECTION



E_{IN} = 100μVrms

TEST CIRCUIT 3

AUDIO AMPLIFIER SECTION

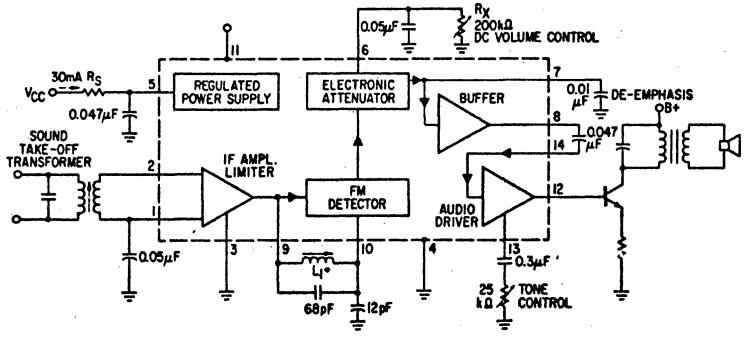


E_{IN} = 100 mV

TEST CIRCUIT 4

TYPICAL APPLICATION

TV SOUND SYSTEM



LOW-LEVEL VIDEO DETECTOR

The TDA1330 is a monolithic integrated circuit designed for use in both colour and monochrome television receivers. It is designed to replace the third IF stage, the detector, the video buffer and the AFC buffer. An important feature is the extremely linear video characteristics and wide band width.

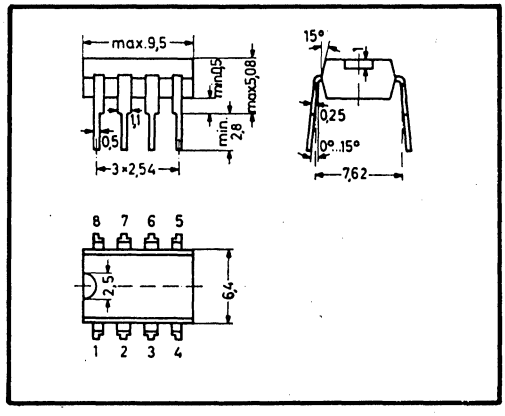


FIG. 1
TDA1330 in the mini Dual-in-line plastic package similar to TO-116.

Absolute Maximum Ratings

V_S	Supply voltage	24V
I_S	Supply current	26mA
V_i	Input voltage (rms)	1.0V
P_{tot}	Total power dissipation (see note) with T_{amb} = 25°C	625 mW
T_{amb}	Operating temperature range	0 to 75°C
T_S	Storage temperature range	−65 to 150°C

NOTE
Derate above T_{amb}=25°C at 5.0mW/°C

ELECTRICAL CHARACTERISTICS

With V_S=20V, Q=30, f_c=45MHz, T_{amb}=25°C in the test circuit shown in FIG. 3 (unless otherwise stated)

V_S	Supply voltage range	20 (12-24)V
I_S	Supply current	15 (20 max)mA
V_o	Quiescent output voltage	7.7 (6.8-8.3)V
V_o	Maximum signal output voltage	0V
V_i	Input signal voltage for 3.0V pk-pk, Video output (90% modulation) rms	36 (25-65)mV
V_o	Maximum output voltage swing pk-pk	7.7V
	Carrier rejection at output	60 (40 min)db
	Carrier output voltage (at 3.0V pk-pk output) rms	
	$f_{out}=f_c$	1.0mV
	$f_{out}=2f_c$	3.0mV
	3db Band width of IF carrier	80MHz
	3dB Band width of video output	12.3MHz
R_i	Input resistance	3.5 (2.4-4.0)KΩ
C_i	Input capacitance	3.0pF
R_o	Output resistance	180Ω
R_s	Internal resistance	4.4KΩ
C_s	Internal capacitance	1.0pF
	Carrier buffer output at carrier frequency (pk-pk)	350mV
	Carrier buffer level	6.5V

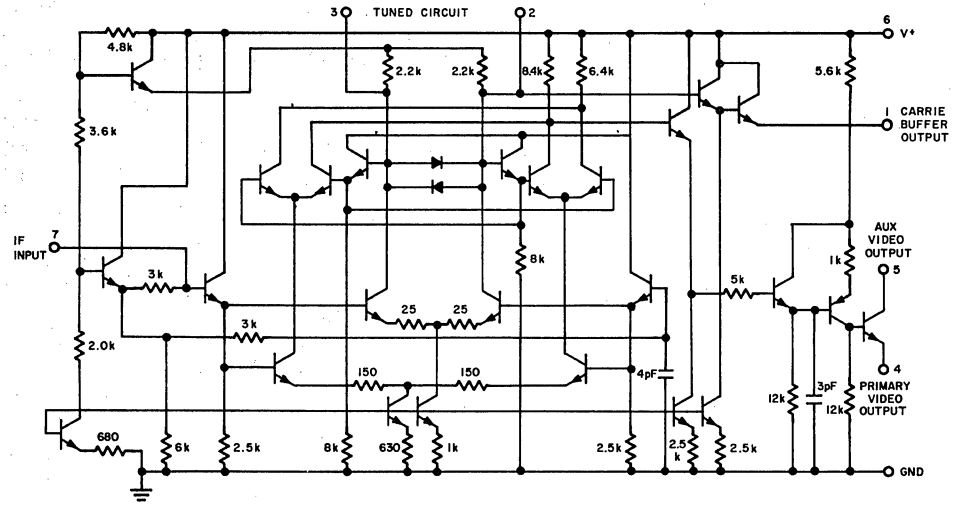


FIG. 2 Internal Circuitry

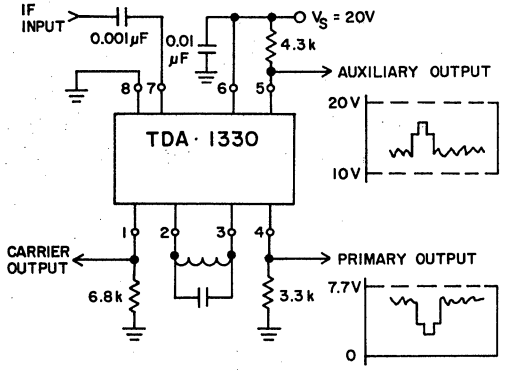


FIGURE 3- TEST CIRCUIT

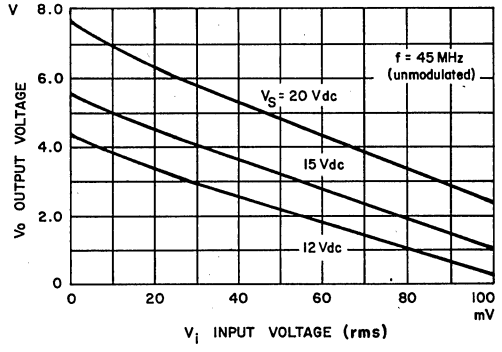


FIGURE 4 - OUTPUT VOLTAGE

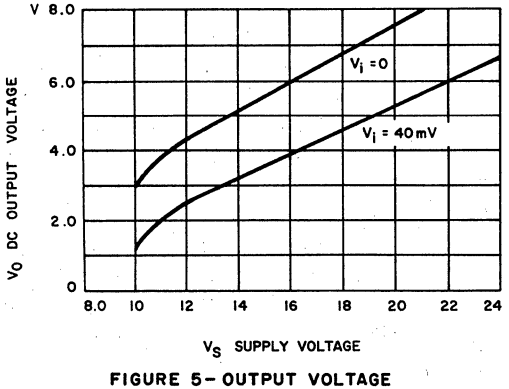


FIGURE 5- OUTPUT VOLTAGE

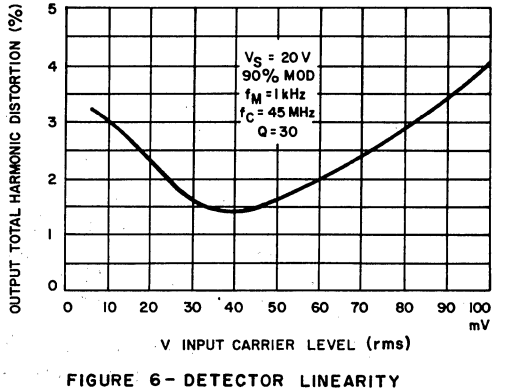


FIGURE 6- DETECTOR LINEARITY

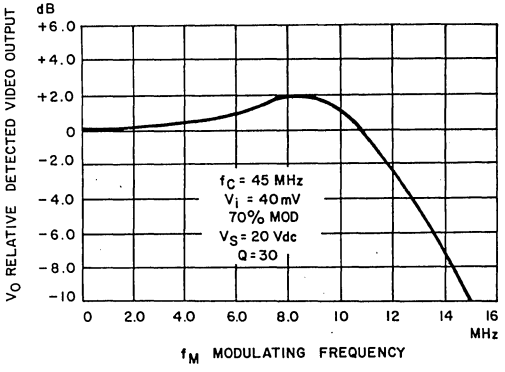


FIGURE 7- VIDEO FREQUENCY RESPONCE

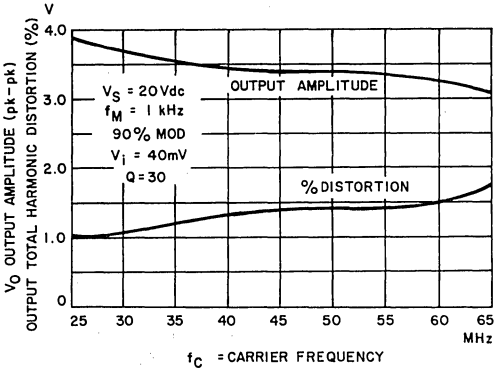


FIGURE 8- CARRIER FREQUENCY PERFORMANCE

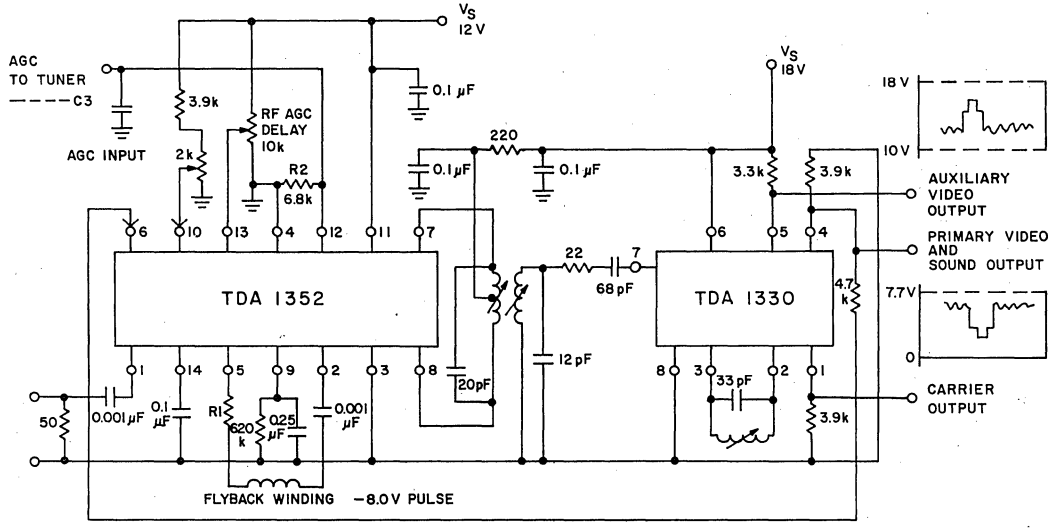


FIG. 9 Typical Application of TDA1330

General Information

Linear detection is simplified with the TDA1330 as it can be carried out at lower power signal levels than previously possible. It offers considerable advantages to the designer some of which are listed below:

1. As FIG. 4 shows, the linearity of output voltage is excellent. It can also be seen that as the slopes are parallel the video amplitude will not change with supply voltage variations.

2. The output level is a linear function of supply voltage and corrections for this can be achieved by regulation of the supply or referring to the video amplifier supply.

3. A video output with positive-going sync is provided but it should be used with care due to its higher output impedance. When it is not used the output should be connected to the supply.

4. A carrier buffer output is provided giving 350mV, sufficient to drive a ratio detector with one additional stage.

TV VIDEO IF AMPLIFIER WITH GATED AGC

The TDA1352 is a monolithic integrated circuit designed for use in either colour or monochrome TV receivers. It consists of an IF amplifier with gated wide-range AGC and is designed to replace the 1st and 2nd IF stages. A single supply of 12V is required for the device and a feature is the power gain of 52dB (typical) at 45MHz. Exhibiting extremely low reverse-transfer admittance, the device has nearly constant input and output admittance over the entire AGC range. A control signal for delayed AGC of the tuner is available from an output.

Normally the TDA1352 is delivered in a dual-in-line plastic package TO-116 (FIG. 1). Upon special request it is also available in the quad-in-line plastic package (FIG. 2).

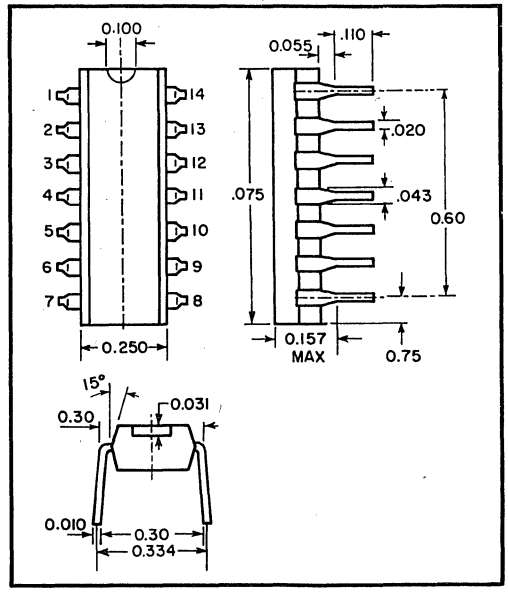


FIG. 1
TDA1352A in dual-in-line plastic TO-116 package.

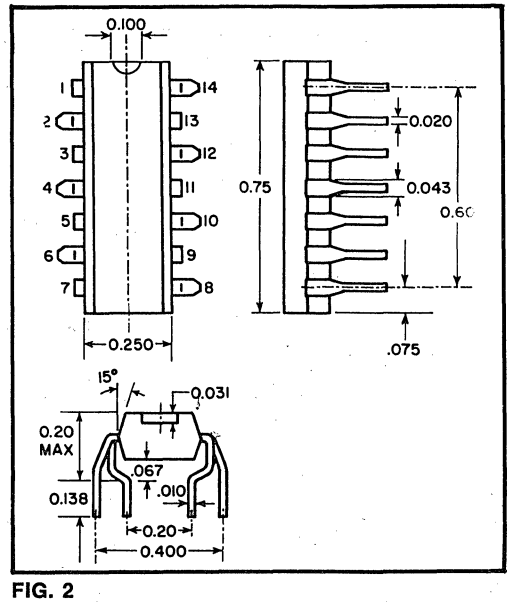


FIG. 2
TDA1352B in quad-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

V_S	Supply Voltage	18V
V_{OS}	Output supply voltage	18V
V_i	Input voltage (pk-pk)	10V
V_{age}	AGC input voltage	6V
V_{gv}	Gating voltage	+10, −20V
P_{tot}	Total power dissipation (see note 1)	625mW
T_{amb}	Operating temperature	0 to 75°C
T_S	Storage temperature	−55 to 150°C

ELECTRICAL CHARACTERISTICS

V_S=12V T_{amb}=25°C unless otherwise stated

	Typ.
AGC Range	75dB
Power Gain	
f=35 or 45MHz	52 (46 min)dB
f=58MHz	50dB
Voltage range for RF-AGC (pk-pk)	
Maximum	7.0V
Minimum	0.2V

ELECTRICAL CHARACTERISTICS (continued)

Maximum differential output voltage swing (pk-pk)
- OdB AGC 16.8V
- −30dB AGC 8.4V

IF gain change over RF-AGC range..... 10dB
Output current 5.7mA
Supply current 27mA
Power dissipation 325mW

General Information

For correct operation of the AGC section of the TDA1352, a gating pulse, a reference level, and a composite video signal must be supplied. A voltage is maintained across the external capacitor C2 (see FIG. 3) by the gating section, which is dependent on the video level and DC reference setting. This voltage results from the charge passed by D1 and the charges drained by T1 during the gating pulse; the magnitude of the charge passed is dependent on the relative amplitude of the video signal to reference level. The voltage passes through the IF-AGC amplifier and is applied to the RF-AGC amplifier where it is compared to the fixed RF-AGC delay voltage by the differential amplifier formed by T2 and T3. The output of T2 is further amplified and the RF-AGC voltage varies (positive-going) due to the change in DC levels. Input impedance is independent of AGC action as the input amplifiers operate at constant emitter currents. Single-ended or differential inputs may be applied. The IF input may be transformer driver, but no DC path to ground is allowed on either terminal.

Increased voltage on the bases of T4 and T5 causing AGC action as the transistors conduct more heavily thereby shunting the original current from the interstage amplifiers (T6 and T7). Output admittance is nearly constant as the output amplifiers are constant current fed (maintaining a constant quiescent bias).

The supply must have a low AC impedance to prevent low-frequency instability in the RF-AGC loop.

A balance between AGC stability and recovery speed has to be achieved in choosing values for C1, C2 and C3 (typical values 0.1μF, 0.25μF and 10μF respectively). For receiver alignment a fixed IF-AGC operating point can be set by connecting a 22KΩ resistor across pins 9 and 11 (minimum gain), and pin 14 biased by means of a 10KΩ variable resistor to ground.

DESIGN PARAMETERS

Typical values at V_S = 12V, T_{amb} = 25°C

	f=35MHz	f=45MHz	f=58MHz	Units
Single-ended input admittance	0.55	0.70	1.1	m mhos
	2.25	2.80	3.75	
Input admittance change with AGC	50	60	—	μ mhos
(0 to 60dB)	0	0	—	
Differential output admittance	20	40	75	μ mhos
	430	570	780	
Output admittance change with AGC	3.0	4.0	—	μ mhos
(0 to 60dB)	80	100	—	
Reverse transfer admittance	<<1.0	<<1.0	<<1.0	μ mhos
Forward transfer admittance magnitude	260	240	210	m mhos
Angle (OdB AGC)	−73	−100	−135	degrees
Angle (−30dB AGC)	−52	−72	−96	
Single-ended input capacitance	9.5	10	10.5	pf
Differential output capacitance	2.0	2.0	2.5	pf

Notes 1. Derate above T_{amb} = 25°C at 5mW/°C

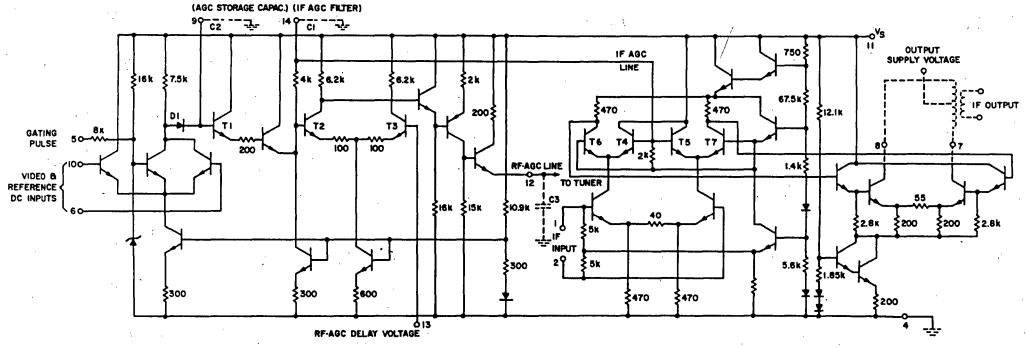


FIG. 3 Internal Circuit

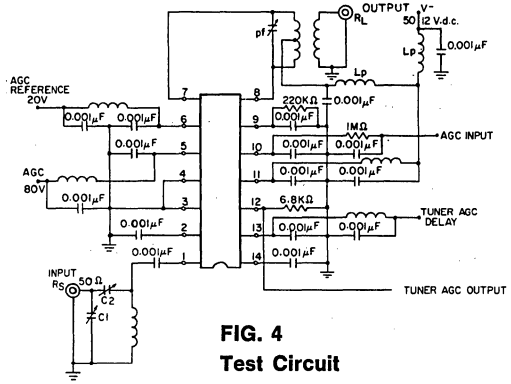


FIG. 4 Test Circuit

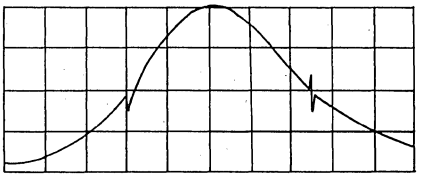


FIG. 5 Response Curve (45 & 58 MK2)

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 RI (Ω)
Negative Going Sync.	5.5 / 2.0 / 0	Adj. 1.0 4.0 Vdc Nom 2.0 V	0
Positive Going Sync.	Adj. 1.0 8.0 Vdc Nom 4.5 V	4.5 / 0	3.9k

FIG. 6 AGC Operation

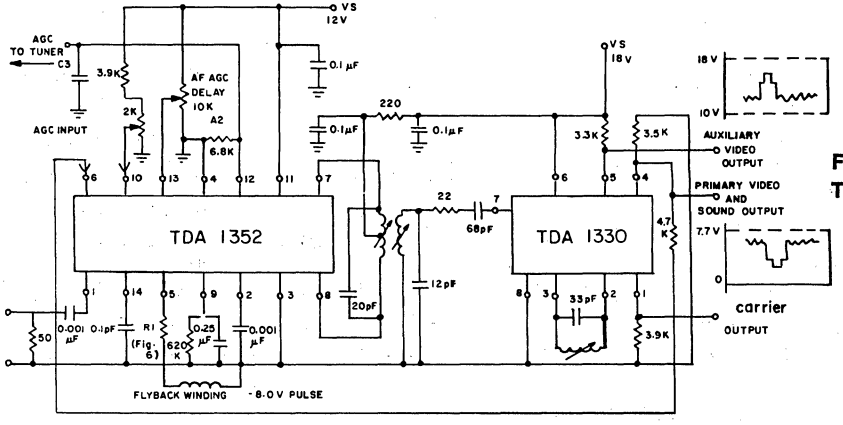


FIG. 7 Typical Application

FIGURE 8 - SINGLE ENDED INPUT ADMITTANCE

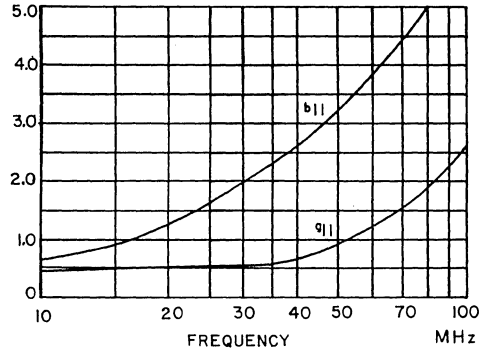


FIGURE 9 - DIFFERENTIAL OUTPUT ADMITTANCE

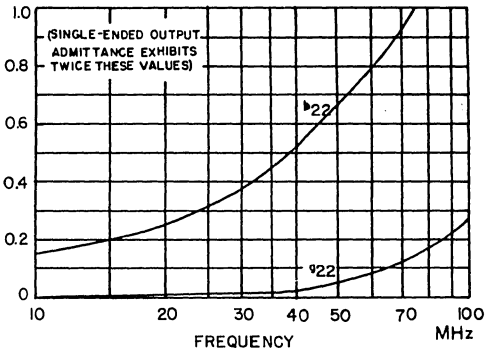


FIG. 10

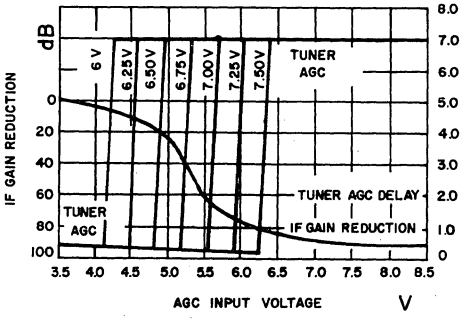


FIG. 11

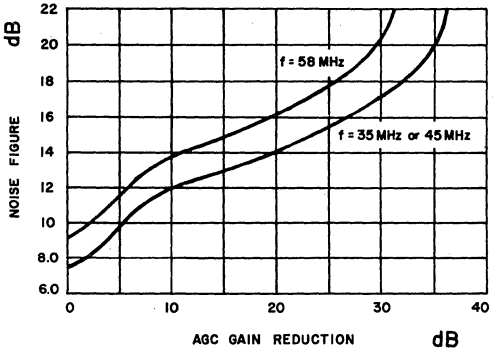


FIG. 12

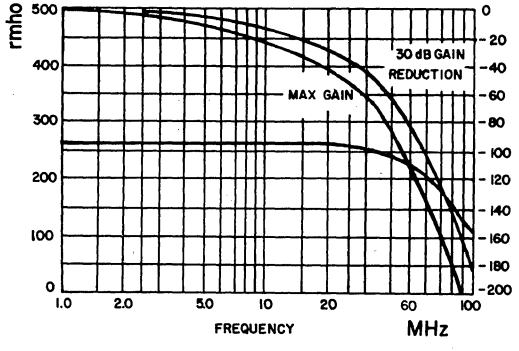
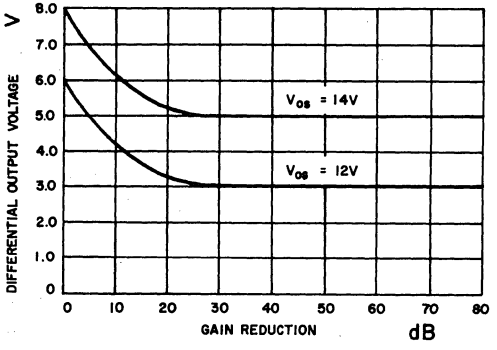


FIG. 13



2 WATT TV SOUND SYSTEM

- **Monolithic 2 watt sound channel**
- **Minimum external components**
- **24 volt operation**
- **Short circuit protection**
- **Low thermal resistance power package**

The ITT3701 is a monolithic integrated circuit which uses a minimum of external components to provide the complete sound function of a TV receiver. Current designs require either two integrated circuits or one integrated circuit and a discrete power transistor to perform the functions incorporated in the ITT3701. The functional block diagram and the required external components are shown in Fig. 3.

The integrated circuit includes: a high gain limiter - IF amplifier, a quadrature type FM detector, a DC operated volume control, and an internally compensated 2 watt audio amplifier.

The ITT3701 is supplied in a modified 14 lead dual in line package with an integral heat sink bracket. (See figure 2.) The device will operate satisfactorily at an ambient temperature of 60° C with worst case program material when the device leads and heat sink bracket are soldered into a suitably designed printed circuit board. For more severe operating conditions, tapped holes are provided to permit easy addition of extra radiators.

The ITT3701 will also be supplied without the heat sink bracket for those applications requiring a different heat sink configuration. Figure 1 shows the 3701 without the bracket and illustrates the tinned mounting surface available for heat sink attachment. (Note 3).

Maximum Ratings:

Supply Voltage	V9	28 volts
Supply Current	I_{11}	50 ma
Output Current	I_8	750 ma

Fig. 1— 14-Lead Plastic Dual-In-Line

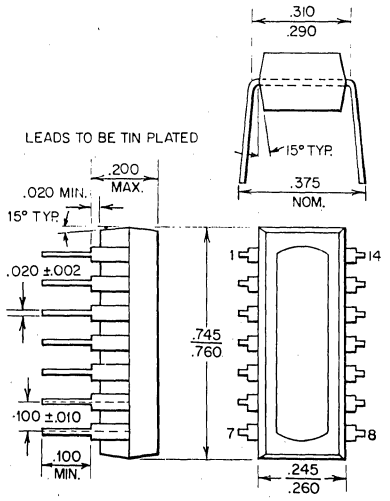
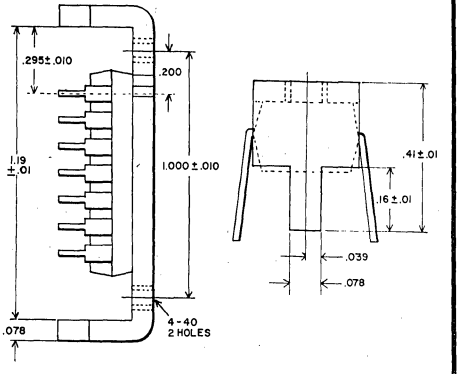


Fig. 2— 14-Lead Plastic Package With Heat Sink Bracket



ITT3701
2 WATT TV SOUND SYSTEM

ELECTRICAL CHARACTERISTICS:

Test Conditions: Circuit Fig. 6
Supply Voltage = 24 volts
Input at Pin 13 = 100mv rms, = 4.5 MHz,
Modulation ± 25 KHz at frequency of 400Hz.

I.F. Section

Quiescent current (I_{11})
(V_{11}=11.0v) ..... 15ma typical
Zener voltage
(I_{11})=25ma) .....12 volts typical
Limitting sensitivity
(—3dB) (Fig. 4) .....100 μv maximum
Recovered audio (v_4) .....700mv±3dB
Total harmonic distortion
(±25kHz deviation) .....1.5% maximum
A.M. rejection (A.M. modulation
30% 500 $\mu V \leqslant V_{13} \leqslant 100mv$) ..40dB minimum
Volume control attenuation
(V_3 = 0) .....60dB minimum
Volume control characteristic:
vout $\propto$ Log (V_3) (FIG. 5)

Audio Section:

Test conditions: Circuit Fig. 7
Audio input frequency = 400Hz
Quiescent current (I_9)
(V_9 = + 24v, v = 0) .....15ma typical
Power output (Total harmonic
distortion = 5%) .....2 watt minimum
Total harmonic distortion
(Pout = 1 watt) .....0.5% maximum
Voltage gain (Note 4) .....30dB ±1.5dB
Hum rejection .....30dB minimum
Input resistance .....40K minimum

POWER DISSIPATION:

With heat sink bracket—
a) Case temperature (Tc)
85°C (note 1) .....4 watts
b) Ambient temperature (Ta)
25°C (note 2) .....2 watts
derate at 16.7mw/°C for Ta = 25°C

Without heat sink bracket—
a) Case temperature (Tc)
85°C (note 1) .....4 watts
b) Ambient temperature (Ta)
25°C .....1.25 watts
derate at 10mw/°C for Ta = 25°C

Storage Temperature
Range .....—40 to + 150°C
Operating Temperature
Range .....—40 to + 85°C

Note 1: Measured at the center of the heat sink bracket directly above the device or at the center of the mounting surface.

Note 2: Operating with no extra external radiator and with heat sink bracket in free air (not soldered into PC board).

Note 3: Extreme care must be used when affixing heat sink to the mounting surface of the 3701. The preferred method is by the use of a thermally conductive epoxy cement. An alternative method is by use of a low temperature solder preform. When using this method do not permit the temperature of the device mounting surface to exceed 150°C.

Note 4: To give nominal overdrive capability of 12 dB at 100% modulation.

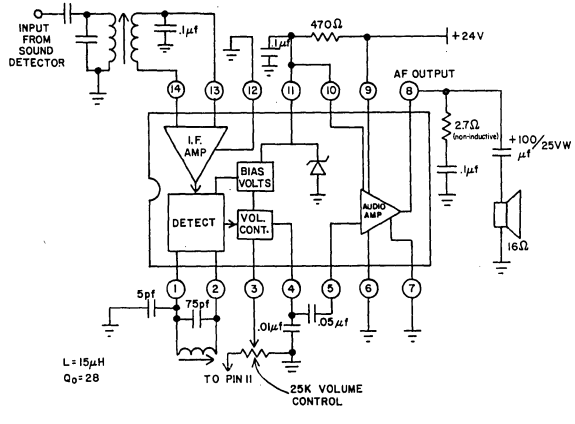


Fig. 3
Typical Applications

Fig. 4

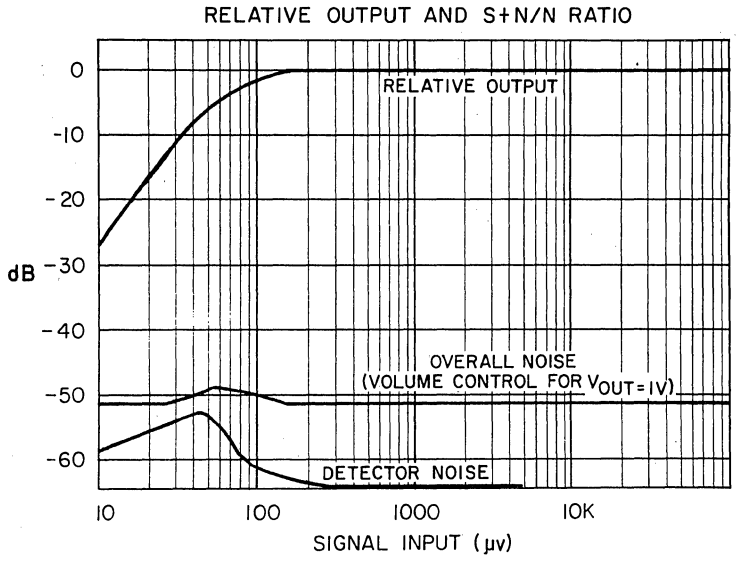

RELATIVE OUTPUT AND S+N/N RATIO
0
-10
-20
dB -30
-40
-50
-60
RELATIVE OUTPUT
OVERALL NOISE
(VOLUME CONTROL FOR VOUT=1V)
DETECTOR NOISE
10
100
1000
10K
SIGNAL INPUT (μv)

Fig. 5

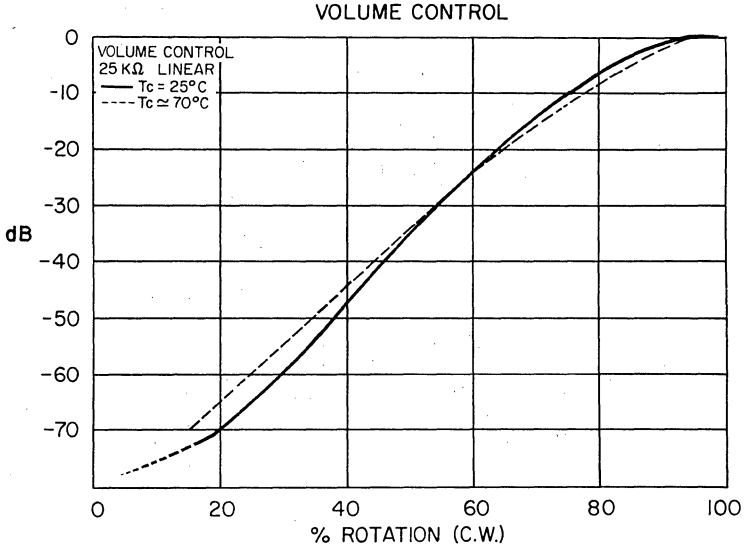

VOLUME CONTROL
0
-10
-20
-30
dB
-40
-50
-60
-70
VOLUME CONTROL
25 KΩ LINEAR
Tc = 25°C
Tc ≃ 70°C
0
20
40
60
80
100
% ROTATION (C.W.)

FIG. 6
I. F. Test Circuit

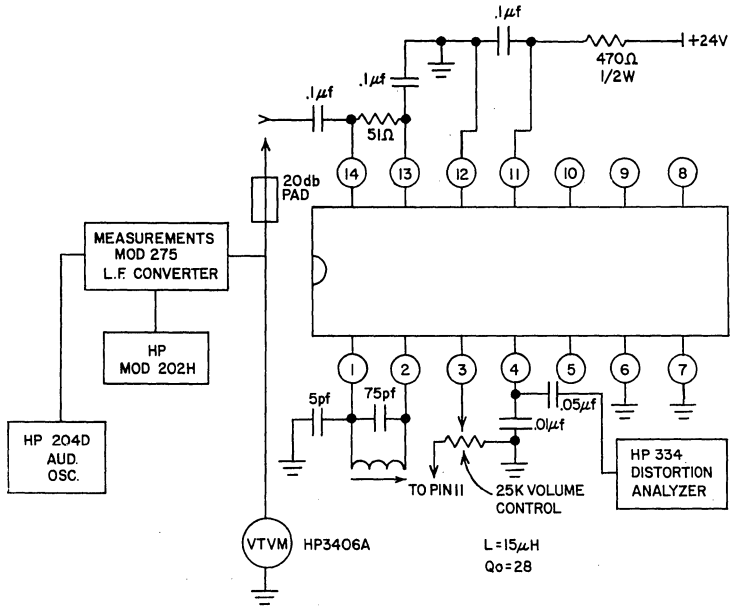
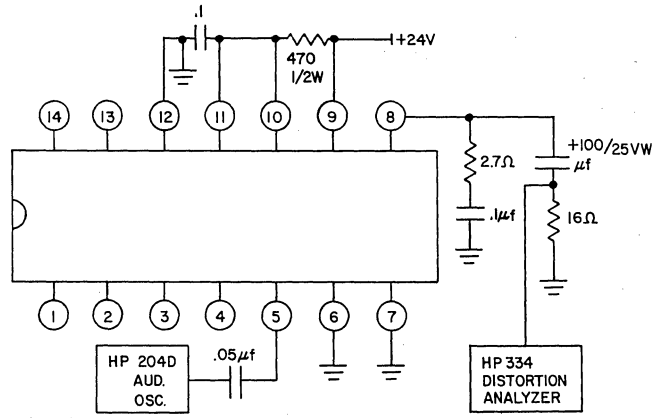


FIG. 7
Audio Test Circuit



SEVEN STAGE FREQUENCY DIVIDER

Monolithic integrated circuit in bipolar technique, designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs.

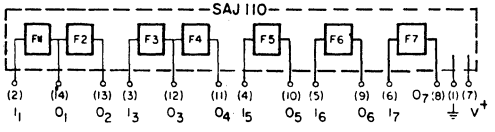
Each flip-flop changes state on application of a positive-going input pulse. The individual flip-flops can be interconnected to form a divider chain. Two flip-flop pairs are already internally series-connected as shown in Fig. 2.

An emitter-follower is interposed between each flip-flop and the associated output terminal to ensure that the output voltage is largely independent of load. Because no internal emitter resistors are provided, the emitter-follower delivers undirectional output currents.

When used in electronic organs the frequency divider SAJ110 may be driven by sine-wave as well as square-wave signals. The shape of the square-wave output signal can be modified by connection of RC filters.

If, by means of an appropriate circuit, all inputs and outputs are brought to a potential below 1.5 volts for a short time, all outputs remain in the low state.

Fig. 2: Block Diagram



The figures in brackets correspond to the pin numbers.

All voltages are referred to terminal 1.

Normally, the SAJ110 is delivered in the dual-in-line plastic package TO-116 (Fig. 1a, add suffix "A" to type No.). Upon special request it is also available in the quad-in-line package (Fig. 1b, add suffix "B" to type No.).

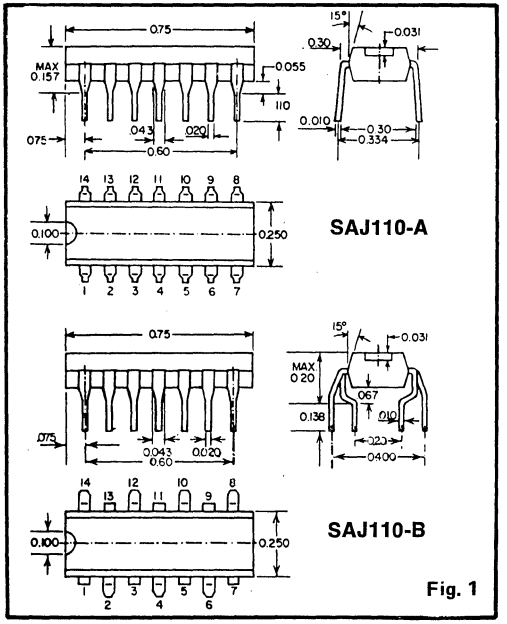


Fig. 1

ABSOLUTE MAXIMUM RATINGS

	Characteristic	Unit
V_7	Supply voltage	11 V
	Input voltage see Fig. 4	
I_O	Output current per stage	5 mA*
V_{ext}	External voltage at output terminals	±5V
T_{amb}	Ambient temperature range	−10 to +60°C
T_S	Storage temperature range	−30 to +125°C

CHARACTERISTICS PER DIVIDER STAGE

at V_7 = 9 V, R_L = 2.2 kΩ, T_{amb} = 25°C

	Characteristic	Unit
I	Supply current (low state at output)	<3 mA
V_i	Input voltage high state (see Fig. 4)	6 to 9 V
V_i	Input voltage low state	<1 V
V_0	Output voltage low state	<0.1 V
V_0	Output voltage high state ...	>7.0 V
t_r	Rise time of output voltage ..	<0.2 us
t_f	Fall time of output voltage ..	<0.2 us
r_i	Input resistance (see Fig. 5)	6 to 9 kΩ

ITT SAJ110
SEVEN STAGE FREQUENCY DIVIDER

CHARACTERISTICS PER DIVIDER STAGE

at V_T=9 V, R_L=2.2 kΩ, T_{amb}=25°C

r_o Output resistance low state .. >1 MΩ

r_o Output resistance high state .. 200 Ω

Recommended Operating Conditions

V_T Supply voltage ..... 9 V

f_{imax} Max input frequency ..... 50 kHz

R_L Load resistance ..... 2 to 20 kΩ

Fig. 3 — Output voltage versus supply voltage.

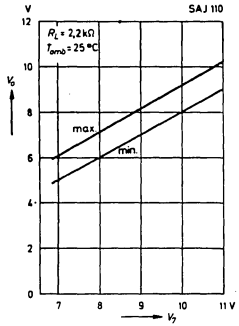


Fig. 4 — Max. admissible and min. required value of input pulses (high state) versus supply voltage.

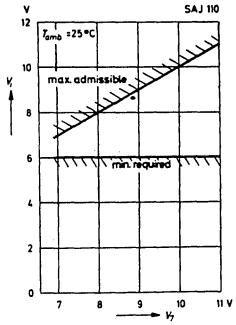


Fig. 5 — Input characteristic

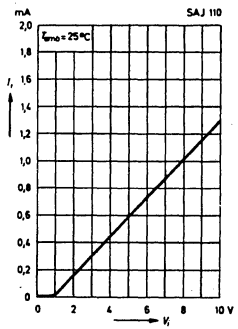
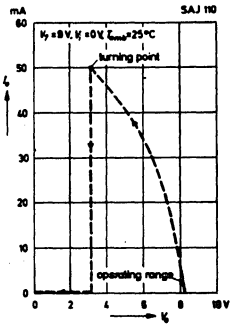


Fig. 6 — Output characteristic



ITT SAJ110 IN FREQUENCY DIVIDER CIRCUITS

Introduction

Integrated digital frequency dividers have for long been widely used in professional digital equipment but have so far found little application in the entertainment sector of the electronic industry. This, no doubt, is due to the fact that the devices presently available do not quite meet the specific requirements of the consumer market, and that they were, until recently, rather expensive. Advances in integration techniques have now made it possible to produce inexpensive linear, as well as digital integrated circuits which should be of special interest to the electronic consumer industry. These devices offer many advantages when compared with circuits employing dicrete components and are in many instances already cheaper. It is certain that the availability of these new integrated circuits will lead to rapid new developments in all branches of the electronic industry.

The new monolithic integrated frequency divider circuit SAJ110, developed by ITT Semiconductors, incorporates seven divider stages which can be used either individually or interconnected to form a divider chain. Because the SAJ110 requires no additional components and can be used in place of conventional discrete-component flipflop dividers, its use as a frequency divider in electronic organs is particularly advantageous.

The Integrated Circuit SAJ110

Integration of a conventional flipflop circuit would offer virtually no advantage over a discrete component circuit — only a circuit which does not incorporate capacitors or other charge-storing elements is suitable for integration. Because the master slave flipflop (a frequency divider often used in digital equipment) is far too complex for consumer applications,

development of a new circuit was necessary. This circuit had to function in a similar manner to a conventional flipflop but had to be designed so that no additional charge-storing elements were required. The result is a device which combines seven single divider stages on a single chip.

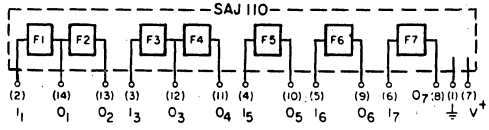


Fig. 7 — SAJ110 Block diagram — The figures in brackets are the same as the pin numbers of package.

In order to make maximum use of the 14 connections available on a TO-116 package the pins are connected as shown in Fig. 1, being arranged so that access to two divider pairs and three single divider stages is possible. The circuits can thus be used either singly or interconnected in various combinations.

Functional Description of an SAJ110 Divider Stage

Each stage used in the SAJ110 comprises basically a trigger network, two transistors connected as a flipflop, and an output stage (Fig. 8). The input is first applied to a trigger network which always steers the input pulse to that transistor which is cut off at the time. Fig. 8 shows the input and output waveforms produced by one such stage. Each positive edge of the input waveform causes the flipflop to change state so that frequency division by two results. The flipflop output is fed to a transistor connected as an emitter follower output stage, this being provided to isolate the flipflop from an external load and to supply output pulses of constant amplitude. The output pin is connected to the emitter of this transistor.

Performance Requirement Summary for the Integrated Frequency Divider SAJ110

The integrated frequency divider had to meet the following customer requirements:

Supply voltage ..... 7 - 11 V
Input (trigger waveforms) ..... Sinusoid or square wave
Output voltage ..... Not less than 6V — high enough to permit reliable triggering of another divider stage under all operating conditions.
Permissible load range ..... 2k to 100kΩ
Ambient operating temperature range ..... 0° to 60°C
Number of stages to be accommodated in one package 7
Packaging . 14-pin DIP or QIL plastic package

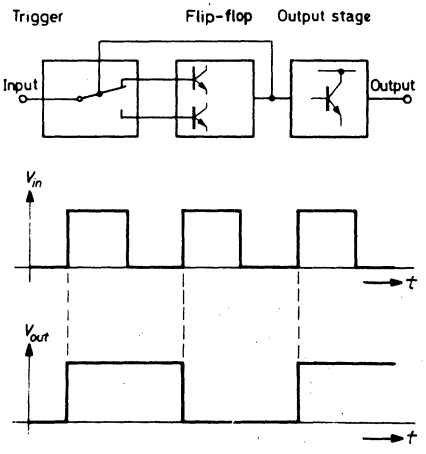


Fig. 8 — Block diagram of one divider stage with input and output waveforms

For reason of economy and reliability, it was also considered desirable that the number of integrated elements and the total resistance of all the resistors used in the IC should be kept to a minimum.

The curves shown in Figs. 3 to 6 illustrate the performance of the divider in more detail.

The input parameters of a frequency divider stage at various supply voltages can be deduced from Figs. 3 and 4. The input pulse amplitude should be not less than 6V, but should, on the other hand, not exceed the supply voltage. The curves in Fig. 3 give the maximum permissible input pulse amplitude range as a function of supply voltage. The input corresponding to "low" level should be less than 1V. Fig. 4 may be used to determine the static input resistance, which varies between 6 and 9kΩ.

In the curve shown in Fig. 5 the output voltage is plotted as a function of supply voltage. As can be seen, the output voltage is 1 to 1.5V lower than the supply voltage and varies somewhat with the load. Assuming the same loading conditions the output voltages of all individual stages are within ±5% — this applies to stages on the same IC as well as to stages on different IC's.

Fig. 6 shows the loading characteristic of a divider stage which gives a "high" output. Note that as the output current of the stage is increased (by reducing the load resistor, for example), point "B" on the curve moves towards "C" (I_{out} = 35 mA and V_{out} = 1.7V) at which point the stage flips into the "low" state and remains there. This bistable output effect is discussed further on in connection with the resetting of dividers used in counting circuits.

Applications for the SAJ110

Use in Electronic Organs

The heart of modern electronic organs is usually a set of LC master oscillators tuned to the frequencies of the highest octave. The frequencies of the lower octaves are then derived from these master oscillators by frequency division. In most conventional organs this frequency division is accomplished by the use of bistable multivibrators (flip-flops). These have the disadvantage of producing a square wave output, which contains practically no even harmonics and offers only limited scope for modifying the character of the notes produced.

However, if the SAJ110 is used, simple RC networks can be connected across the outputs to generate sawtooth waveforms which contain even harmonics. An additional advantage of the SAJ110 is its small size, making it particularly suitable for use in portable instruments.

Fig. 9 shows the usual frequency generating circuits employed in electronic organs. Twelve master oscillators produce the frequencies of the highest octave while all the frequencies for the lower octaves are generated by frequency division. The arrangement shown in Fig. 9 requires up to twelve SAJ110 circuits for one organ. If the organ has less than seven octaves, then there are several spare divider stages which may be utilized in the divider chains associated with other frequencies so that in this case less than 12 integrated circuits are required.

Depression of one of the organ keys, T, causes several outputs to be switched to a common line, S, via high value resistors, R, and this signal, which is a combination of several frequencies, is then further processed. The spectrum of this signal is considerably richer in harmonics than that of an ordinary square wave.

It is an advantage to give a signal to the following filters the mean value of which does little change when the organ keys are pressed. In order to obtain this, the ground of resistor R/10 (Fig. 9) should be connected to a positive potential. Another possibility is to ensure that the divider outputs supply proper AC signals. Fig.10 shows such an alternative circuit. Use of a suitable bias causes the full alternating divider output component to be developed across the load R_L.

The circuit shown in Fig. 11 fully exploits the high output voltage and low output resistance of the frequency divider SAJ110. In this circuit RC networks are connected, via protection diodes, to the outputs of individual divider stages so that waveforms which are not very different from that of an ideal sawtooth are presented across the load R_L. The protective resistor R_S connected in series with each capacitor C_L is included to limit the capacitor surge to a value which the output stage can safely handle.

In Fig. 12 the frequency spectrum of the waveform V_{RL} is compared with that of two sawtooth waveforms, and it can be seen that the spectrum attained with the circuit arrangement of Fig. 10 approaches that of an ideal sawtooth. Note that the sub-harmonic component is extremely small — much smaller than is necessary for this application.

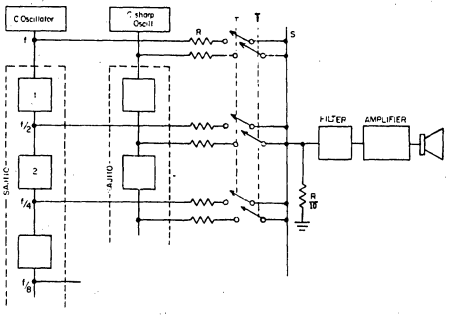


Fig. 9—Block diagram of the tone generating circuits in electronic organs

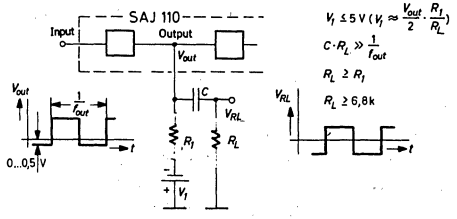


Fig. 10-Conversion of divider undirectional output into alternating output

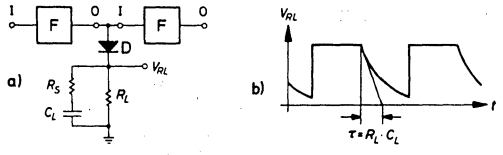


Fig. 11—Modification of the divider frequency spectrum using RC networks

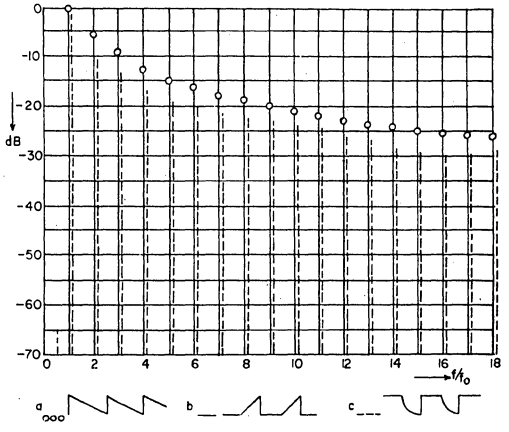


Fig. 12 —Frequency spectrum associated with various waveforms

Use of the SAJ110 in Counting Circuits

Use of the SAJ110 in a counting circuit raises the problem of how to reset the flipflops. With the SAJ110 it is possible to reset a single stage as well as several stages connected in a counting chain. However, when designing a suitable reset circuit the following features of the device must be taken into account:

The output of a divider stage can change state only while its input is positive going.

The frequency divider SAJ110, unlike a master slave flipflop, does not possess a buffer stage between input and output, nor a special reset input.

It is, however, possible to use the inputs and outputs for reset purpose. Because the reset capability of an SAJ110 stage depends on its input state, it is necessary to use both the input and the output terminals for reset purpose.

Output Characteristic

Referring to the output characteristic of a single stage (Fig. 6) it can be seen that a "high" output can only be flipped to "'low" if the output is pulled down to 1.5V or less by some external means, and this can only be accomplished while the input voltage V_{in} is "low". The output characteristic in Fig. 6 is divided into the sections A-B and B-C, section

A-B being the normal operating range. As mentioned previously, in order to initiate a reset it is necessary to force the output through the range B-C to point "C", and this should be effected in the shortest time possible (t_r < 0.1msec) to avoid overheating the device (the output transistor dissipates considerable power during this period).

If the divider input potential is higher than OV, then the trigger point C is shifted to the left on the curve, which means that the output potential would then have to be pulled down to a level below 1.5V. If the input and output of a divider stage or if several inputs and outputs of a divider chain are to be pulled down to a low potential together, then this potential should be less than 1.5V to ensure that the circuits reset reliably under any condition (refer to Fig. 13).

Reset Circuit.

Fig. 13 outlines a reset circuit suitable for a seven stage counting chain. All the output points as well as the input point I are connected, via isolating diodes, to the collector of a switching transistor type 2N2218, or alternatively to a RESET switch. It is important that the transistor collector voltage drops to a saturation level of less than 0.6V for the duration of the reset pulse, and that the transistor is capable of passing up to 400 mA of collector current under the most unfavorable conditions (i.e. when all outputs are in "high" condition prior to the application of a reset pulse). The pulse source must therefore be capable of supplying at lease approximately 15mA to the base of the 2N2218 so that the requirement $V_{I1}=V_{O1}=\ldots V_{O7}>1.5V$ is fulfilled. The reset pulse duration is, however, not very critical provided it is not less than approximately 1μsec.

As mentioned previously, the output state of all the stages depends on the input state of the first stage immediately after the occurrence of the reset pulse. There are two possible conditions:

V_{I1} = "low" (Fig. 14)
V_{I1} = "high" (Fig. 15)

In Fig. 14 I_I was "low" at the instant when the reset was applied; under this condition all the outputs which were in the "high" state immediately before application of the reset pulse change to "low" and maintain this state after the reset pulse has been removed. The next input pulse to I_I then causes all the outputs to be triggered to "high", this corresponding to a "PRESET" condition of the counter. Only the second input pulse is counted. These conditions are summarized in the truth table in Fig. 14 and it can be seen that the counter counts (n-1).

Fig. 15, on the other hand, illustrates a condition in which all the outputs are in the "PRESET" state immediately after the occurrence of the reset pulse so that the next pulse is correctly counted as No. 1. The explanation for this is as follows: Although in this case the reset pulse initially pulls all the outputs, as well as the input I_I, to "low", the input I_I is immediately returned to "high" at the end of the pulse ($t = t_i$), because the positive edge at the end of the pulse is equivalent to the application of a logic "H" to the input. This positive edge triggers first output O_I and then, in turn, all the other outputs to "high" — this corresponding to the "PRESET" state of the counter.

Conclusion

The SAJ110 is an inexpensive seven-stage frequency divider which, in comparison with equivalent discrete-component circuits, offers many advantages, the most important ones being: small size and low wiring and assembly cost. The device, because of its electrical characteristics, is particularly suitable for use in electronic organs where its performance is superior to that of discrete component flipflops. Being insensitive to the waveform of the input signal, the SAJ110 will accept a square wave as well as other types of waveforms (e.g. sinusoids; moreover, the low output impedance ensures that the output remains virtually constant irrespective of load, the lowest permissible load being approximately 2kΩ. At maximum loading the output amplitude is only 1.5V less than supply voltage.

The generation of output waveforms which are very similar to, and possess virtually the same frequency spectrum as, that of an ideal sawtooth, is possible simply by connection of RC networks across the outputs.

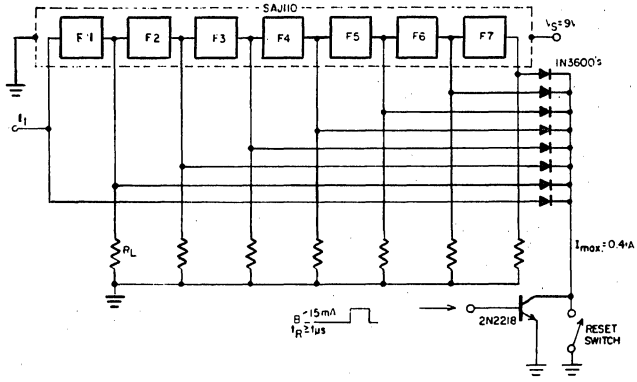
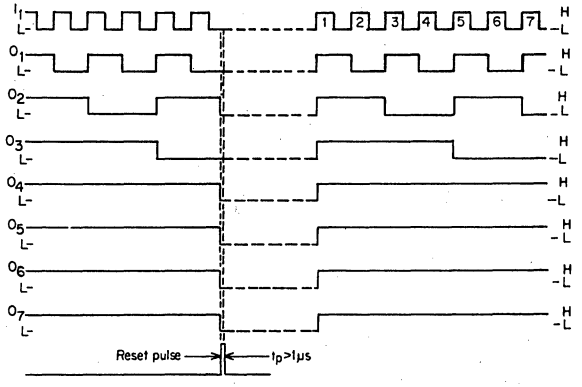


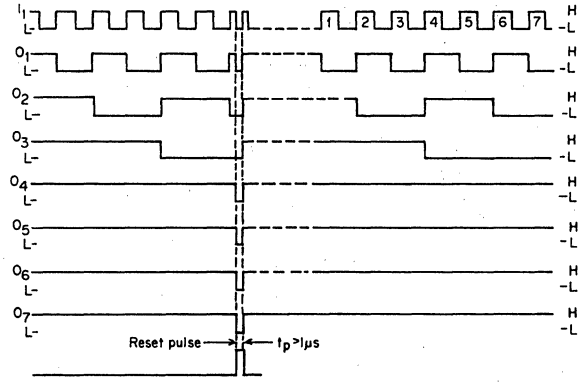
Fig. 13—Reset circuit for a seven stage counter



TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	L	L	L	L	L	L	L
1	H	H	H	H	H	H	H
2	L	H	H	H	H	H	H
3	H	L	H	H	H	H	H
4	L	L	H	H	H	H	H
5	H	H	L	H	H	H	H
6	L	H	L	H	H	H	H
7	H	L	L	H	H	H	H

Fig. 14—Reset action at V_{I1} = "low"



TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	H	H	H	H	H	H	H
1	L	H	H	H	H	H	H
2	H	L	H	H	H	H	H
3	L	L	H	H	H	H	H
4	H	H	L	H	H	H	H
5	L	H	L	H	H	H	H
6	H	L	L	H	H	H	H
7	L	L	L	H	H	H	H

Fig. 15—Reset action at V_{I1} = "high"

MOS TONE GENERATOR

The SAH190 is a monolithic, MOC integrated, special LSI circuit. Only three SAH190 circuits are required to generate the twelve notes of the highest octave in electronic organs. A two-phase clock generator, which is in practice the master oscillator of the organ, is required for driving the SAH190. This generator delivers a frequency considerably higher than that of the highest octave. The SAH190 generates four tones, the frequency spacing of which corresponds to an interval of three semitones by dividing the clock frequency. By externally switching the connection Option 1 these four notes can be lowered as desired by a semitone or by a whole tone so that the twelve master oscillators required hitherto can be replaced by three SAH190 units. By switching the connection Option 11, the output frequencies of the SAH190 can be modified by one octave. One can therefore choose whether the tones generated are to lie in the third octave or the fourth octave above middle C, for instance. The outputs A to D of the SAH190 are specifically designed for directly driving the integrated frequency divider SAJ110, see Fig. 3. In addition, a further load with a resistance of greater then 10kΩ can be connected. The output signal has a square wave form with a pulse duty factor of 0.5. The greatest deviation of the twelve tones from the equal temperament scale is ±0.03 0/00.

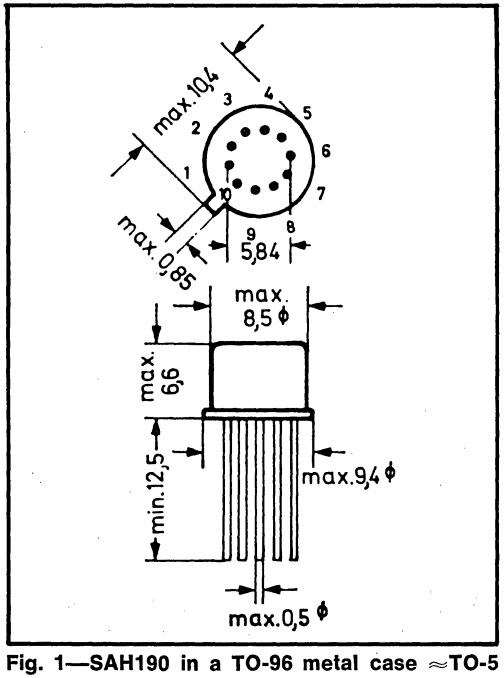


Fig. 1—SAH190 in a TO-96 metal case ≈TO-5 with 10 terminals. Weight approx. 1 g. Dimensions in mm

Terminals

1. Ground, O, Substrate, case
2. Option II
3. V_{dd}
4. Output A
5. Output B
6. Output C
7. Output D
8. Clock pulse t2
9. Clock pulse t1
10. Option I

MAXIMUM RATINGS

V_8, V_9	Clock voltages	−30 to +0.3V
V_3	Drain voltage	−30 to +0.3V
I_4, I_5	Output currents	−5mA
I_6, I_7		−5mA
T_S	Storage temperature range	−20 to +80°C

RECOMMENDED OPERATING CONDITIONS

V_3	Drain voltage	−17 (−15 to −19) V
V_8, V_9	Clock voltages	−20 (−18 to −22) V
f_t	Clock frequency	1 to 1.5MHz

CHARACTERISTICS

r_{out}	Output resistance	<500Ω
I_D	Drain current	−5mA

Divider ratio, which can be set using the connection Option II:

Option II to ground	$\frac{f_t}{f_1}$	176
Option II open	$\frac{f_t}{f_1}$	352

CHARACTERISTICS (continued)

Generating the twelve semitones by different voltages at the connection Option I:

The frequencies f_1 to f_{12} are the twelve semitones of the octave, f_1 being the highest and f_{12} being the lowest note. A to D are the four outputs.

	A	B	C	D
Option I to t_1	f_1	f_4	f_7	f_{10}
Option I open	f_2	f_5	f_8	f_{11}
Option I to ground	f_3	f_6	f_9	f_{12}

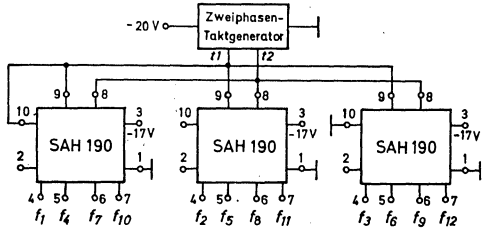


Fig. 2—Block circuit diagram of a twelve tone generator with these three SAH190 units

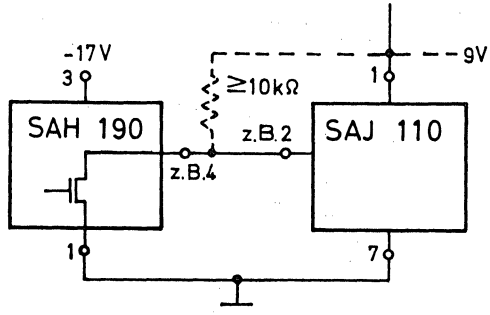


Fig. 3—SAH190 driving SAJ110

APPLICATION INFORMATION

The tweleve independently oscillating master oscillators used in organs of conventional construction have some disadvantages. The influences of temperature, voltage, aging and changes caused by mechanical impacts generally affect the frequencies of the individual oscillators differently, so the organ can become out-of-tune. In addition, frequency modulation by a vibrato voltage can result in different frequency shifts for the individual oscillators.

It is apparent that efforts should be made to find a way of rigidly coupling the twelve master tones together so that they cannot become out-of-tune internally. Such possibilities are discussed below, in particular an LSI circuit in MOS technique, SAH190, developed by ITT Semiconductors for this application is described.

The principle of the phase-locked-loop offers one possibility for rigid coupling. This is based on the fact that the frequency ratio of two neighbouring semitones of the equal tempered tone scale is equal to $\sqrt[12]{2}$.

This value can be approximated by a fraction of 196/185 to within an error of 3×10^{-6}. Pairs of oscillators are coupled in the following way: The oscillations of each of the oscillators are counted using one counter each with the end positions 196 and 185 respectively. If the two counters which are started at the same time reach their final position simultaneously, the frequencies of the two oscillators have the exact ratio of 196/185. If the counters do not reach the end position simultaneously, a control signal is generated to retune one of the oscillators. The twelve master oscillators can be coupled together in this way. This is shown in Fig. 4.

Considerably more interesting possibilities, from the point of view of the integrated-circuit technique, are, however, obtained from circuits with just one clock pulse generator, in which the twelve tones are generated by division or addition. The procedures described below are known.

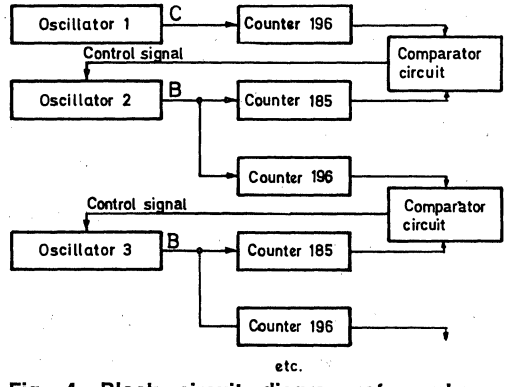


Fig. 4—Block circuit diagram of a phase-locked-loop oscillator

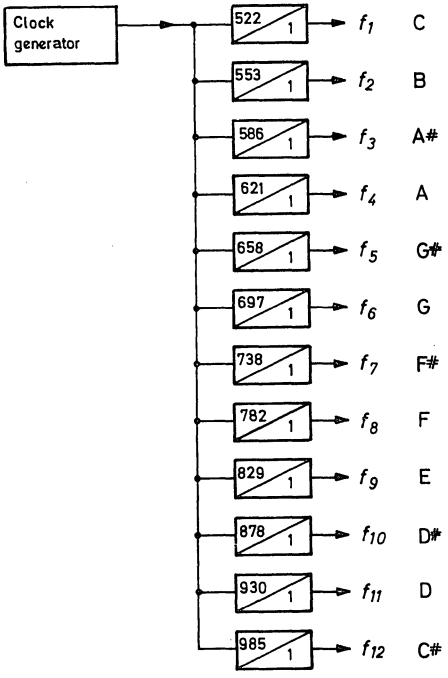


Fig. 5—Block circuit diagram of a clock generator with twelve frequency dividers.

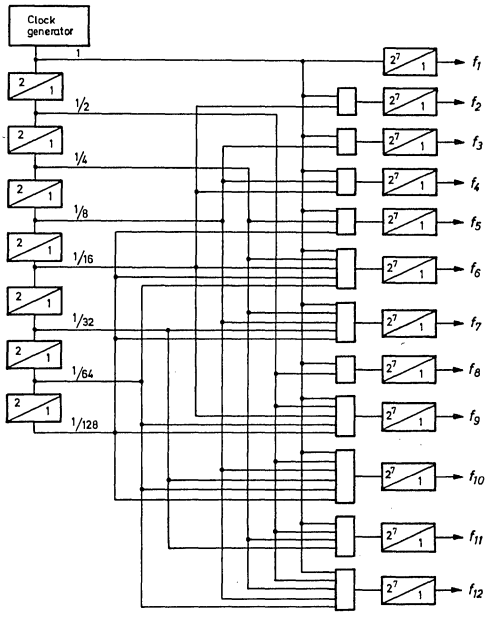


Fig. 6—Block circuit diagram of tone generation by frequency synthesis.

FREQUENCY DIVISION

Twelve frequency dividers are connected to a high frequency oscillator. The output frequencies of these dividers form the tones of the highest octave. As it is only possible to produce frequency dividers with whole numbers, good results, that is small deviations from the equal tempered scale, can only be achieved if the divider ratios are chosen sufficiently large — approximately between 500 and 1000. Fig. 5 gives as an example a block circuit diagram of such a divider arrangement.

FREQUENCY SYNTHESIS

Fig. 6 shows the block circuit diagram of an arrangement which generates the twelve notes of the highest octave by frequency synthesis. The frequency of an oscillator is divided by two several times in a divider chain. The number of necessary binary dividers depends on the permitted frequency error with reference to the equal temperament. The individual outputs are fed to eleven linking circuits in such a way that at each output of a link circuit the sum of the frequencies given at the input is present. The cycle durations of the frequencies thus generated are however not constant, they oscillate about a mean value. This effect is known as jitter and is sometimes perceived as interfering background noise. Jitter can be reduced with a binary divider chain which is connected in series. After seven divider stages it is sufficienty attenuated to be no longer audible.

FREQUENCY DIVISION ON THE SUPPRESSION PRINCIPLE

If every tenth pulse is suppressed in a cyclic pulse sequence of the frequency, f, the remaining pulses — averaged over a long period of time — have the frequency $9/10 \times f$. This method of producing a fixed ratio between two frequencies is known as the suppression principle. Fig. 7 shows the block circuit diagram of a type of tone generator operating on this principle. The pulses of a clock generator

are fed to a frequency divider T and to an 11 out of 196 suppression circuit. This suppresses 11 of every 196 pulses which arrive. The remaining pulses are again fed to a divider T and the next suppression circuit. The output frequencies of the dividers T differ in each case by 185/196, which exactly corresponds to the interval of a semitone.

The signals at the outputs of the dividers T have no constant cycle duration, as is the case with frequency synthesis. The frequency f_2 has two different cycle durations, f_3 has three cycle durations, and so on. The individual cycle durations differ by one duration of a cycle of the clock generator frequency. The difference between the longest and shortest cycle duration is defined as jitter and indicated in multiples of the cycle duration of the clock frequency.

Examination of the possibilities described gives the following: With the phase-locked-loop the frequency error is small and the output signal is free from jitter. The procedure is however expensive on account of the large amount of circuitry required. Frequency division and frequency synthesis give a quantisation error which is only sufficiently small if a high clock frequency, and hence a high divider ratio is used. These procedures are also too exxpensive, on account of the high cost of the circuitry, and the synthesis procedure also requires extra cost to reduce the jitter. With the suppression principle according to Fig. 7 excellent frequency accuracy is obtained, but the jitter of the last divider stage is unacceptably high, as it becomes larger from stage to stage when the suppression circuits are connected in series .

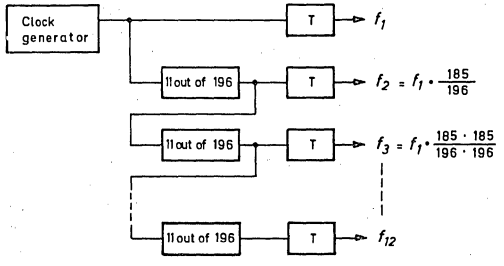


Fig. 7—Block circuit diagram of tone generation according to the suppression principle.

When developing SAH190, the great accuracy of the suppression principle was used to advantage — the maximum deviation of a tone from the equal temperament is only 0.03 0/00. The excessively high jitter in an arrangement as shown in Fig. 7 was reduced to tolerable values by the structure shown in Fig. 8, in which a maximum of only five suppression circuits is connected together, instead of having twelve suppression stages directly connected in series. In the block circuit diagram of the whole arrangement for generating the

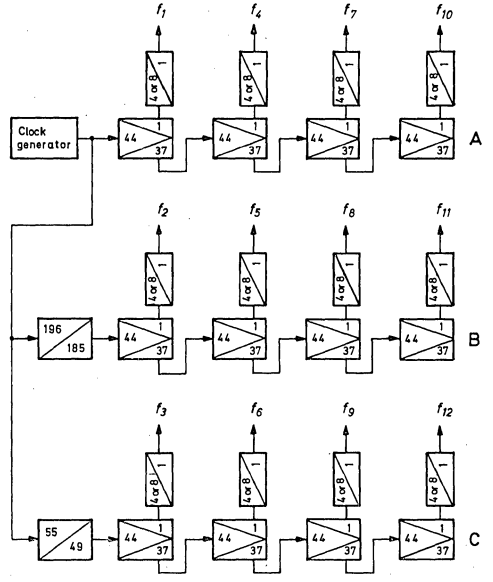


Fig. 8—Block circuit diagram of the layout used with the SAH190

twelve notes of the highest octave, shown in Fig. 8, there are three chains of frequency dividers connected one after the other. Each chain consists of one SAH190. The first divider of each chain is driven by the common clock generator.

Chain A consists of four dividers connected in series one after the other. Fig. 9 shows the block circuit diagram of one divider which has a dual function. It divides first of all the input frequency by 44 and drives an output divider with this frequency. It also divides the input frequency by 44/37 with the aid of the suppression circuit shown next, and drives the

next identically designed divider with the input frequency divided by 44/37.

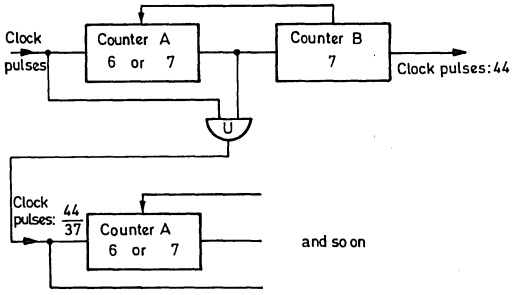


Fig. 9—Block circuit diagram of a 44/1 or 44/37 divider

The divider shown in Fig. 9 consists of two counters, A and B, and a suppression circuit U. Counter A counts the clock pulses and each time when it is reset to its initial position it emits a pulse to the suppression circuit and to counter B.

Counter B has the end position 7. It counts the output pulses of counter A and also controls the final position of the latter. If counter B is in the position 1, 2, 3, 5, or 6, counter A counts up to six. When counter B is in position 4 or 7, counter A counts up to seven. Counter B therefore emits an output pulse on every 44th clock pulse. Each output pulse of counter A suppresses a clock pulse in the suppression circuit. At the output of the suppression circuit, which leads to the input of the next divider, only 37 output pulses appear from the 44 clock pulses. The pulse frequency at the output of the suppression circuit of the second divider is also reduced by the factor 44/37 with reference to the value at the output of the suppression circuit of the first divider. The fraction 44/37 is a good approximation for the frequency ratio $\sqrt[12]{2^7}$.

That is the interval of three semitones, a minor third.

Switchable output dividers are driven from the outputs of counters B. Depending on whether the highest octave is the third or fourth octave above middle C, a divider ratio of 8 or 4 is set. These switchable output dividers give a square wave signal with the pulse duty factor of 0.5, having a sufficiently small amount of jitter.

The divider chain A (Fig. 8) generates four notes at an interval of a minor third in each case, that is the notes C, A, F* and D*. The notes B, G*, F and D are generated in divider chain B. This chain also has four 44/37 dividers, which have a 196/185 divider connected in front of them, reducing the clock frequency and hence all output frequencies of divider chain B by the amount of one semitone. The notes A*, G, E and C* which are still missing are generated by divider chain C. A preliminary divider is required here to lower the clock frequency and hence the four output frequencies of divider chain C by an amount equal to one whole tone. This corresponds to a frequency ratio $\sqrt[12]{2^2}$.

The fraction 55/49 is a good approximation for this value. The preliminary dividers also operate on the basis of the suppression principle explained using Fig. 9.

Splitting the divider system into three chains, each producing four tones, is very advantageous for integration. The SAH190 (Fig. 10) which is constructed according to the principle described, contains a chain with four 44/37 dividers with the associated switchable output dividers and the two 55/49 and 196/185 preliminary dividers. By switching over the connection Option I externally, it is possible to select one of the two preliminary dividers or to put both of them out of service. Three SAH190 units are required to build up a complete twelve tone generator, as shown in Fig. 2. The following Table 1 shows the exact numerical values of a twelve tone generator in accordance with Fig. 2.

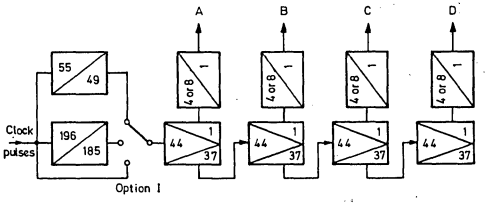


Fig. 10—Block circuit diagram of the SAH190

Table 1: The divider characteristics of a twelve tone generator circuit according to Fig. 2.

Cycle duration T_n of the output frequencies f_1 to f_{12} as a multiple of the cycle duration T_g of the clock frequency	Jitter	Mean divider ratio	Relative frequency error ppm*
$T_1=176T$		176	+29
$352T_g$		352	+29
$T_4=209/210T_g$	$1T_g$	209.28730	+14
$418/419T_g$	$1T_g$	418.59460	+14
$T_7=248/249/250T_g$	$2T_g$	248.89408	−1
$497/498/499T_g$	$2T_g$	497.78816	−1
$T_{10}=294/295/296/297/298T_g$	$4T_g$	295.98215	−17
$590/591/592/593/594T_g$	$4T_g$	591.96430	−17
$T_2=186/187T_g$	$1T_g$	186.46486	+25
$372/373T_g$	$1T_g$	372.92973	+25
$T_5=221/222/223T_g$	$2T_g$	221.74200	+10
$442/443/444T_g$	$2T_g$	443.48400	+10
$T_8=262/263/264/265T_g$	$3T_g$	263.69319	−6
$526/527/528/529T_g$	$3T_g$	527.38638	−6
$T_{11}=311/312/313/314/315/316T_g$	$5T_g$	313.58109	−21
$625/626/627/628/629/630T_g$	$5T_g$	627.16220	−21
$T_3=197/198T_g$	$1T_g$	197.55102	+17
$395/396T_g$	$1T_g$	395.10204	+17
$T_6=234/235/236T_g$	$2T_g$	234.92554	+2
$469/470/471T_g$	$2T_g$	469.85107	+2
$T_9=278/279/280/281T_g$	$3T_g$	279.37091	−14
$557/558/559/560T_g$	$3T_g$	558.74182	−14
$T_{12}=330/331/332/333/334/335T_g$	$5T_g$	332.22486	−29
$663/664/665/666/667T_g$	$4T_g$	664.44973	−29

*1ppm=1 part per million, that is 1×10^{-6}

The Clock Generator for the SAH190

A two-phase clock generator emitting two clock pulses t1 and t2 which do not overlap, and the amplitudes of which are −20V is required for driving the SAH190. The two clocks may overlap at the most in the range from 0 to −3V, and the duration of the negative flat tops of the pulses must not fall below 0.2μs if reliable operation of the SAH190 is to be ensued see the oscillogram in Fig. 11.

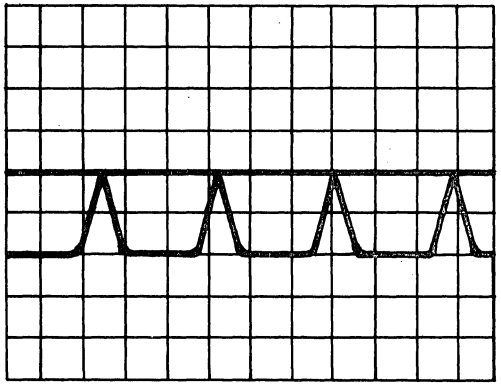


Fig. 11—Oscillogram of the clock signals t1 and t2 in the circuit of Fig. 12. Vertical: 10V/division. Horizontal: 0.2μs/division.

An LC oscillator with a pulse shaping stage connected in series after it, as shown in Fig. 12 is proposed as the clock generator. The oscillator consists of transistors T3 and T4 and the frequency-determining tank circuit C1, L1. Frequency modulation for the vibrato effect is generated by modifying the operating points of the oscillator transistors. With a vibrato voltage of 15V peak-to-peak, vibrato of ± one quarter tone can be obtained.

When designing the clock generator the coil for convergence adjustment in colour television sets proved useful as the oscillator coil. This coil has a knob which can be used for changing the overall pitch. For this purpose the coil is mounted in the control panel of the organ and linked with the oscillator circuit via screened cables with a maximum length of approximately 25cm. If it is not necessary for the oscillator frequency to be modified within wide limits, any other coil with a lower inductance variation can be used. When the highest octave is to be c^5 to b^5 the first type is to be wound with 80 turns 0.3mm ϕenamelled copper wire, and the second coil with 72 turns 0.1mm ϕenamelled copper wire.

To adjust the pitch from the console, it is possible for instance to connect a small variable capacitor with a final capacitance of approximately 50pF in parallel with the capacitor C1, located among the controls of the organ and connected via screened cables with a maximum length of 25cm to the oscillator

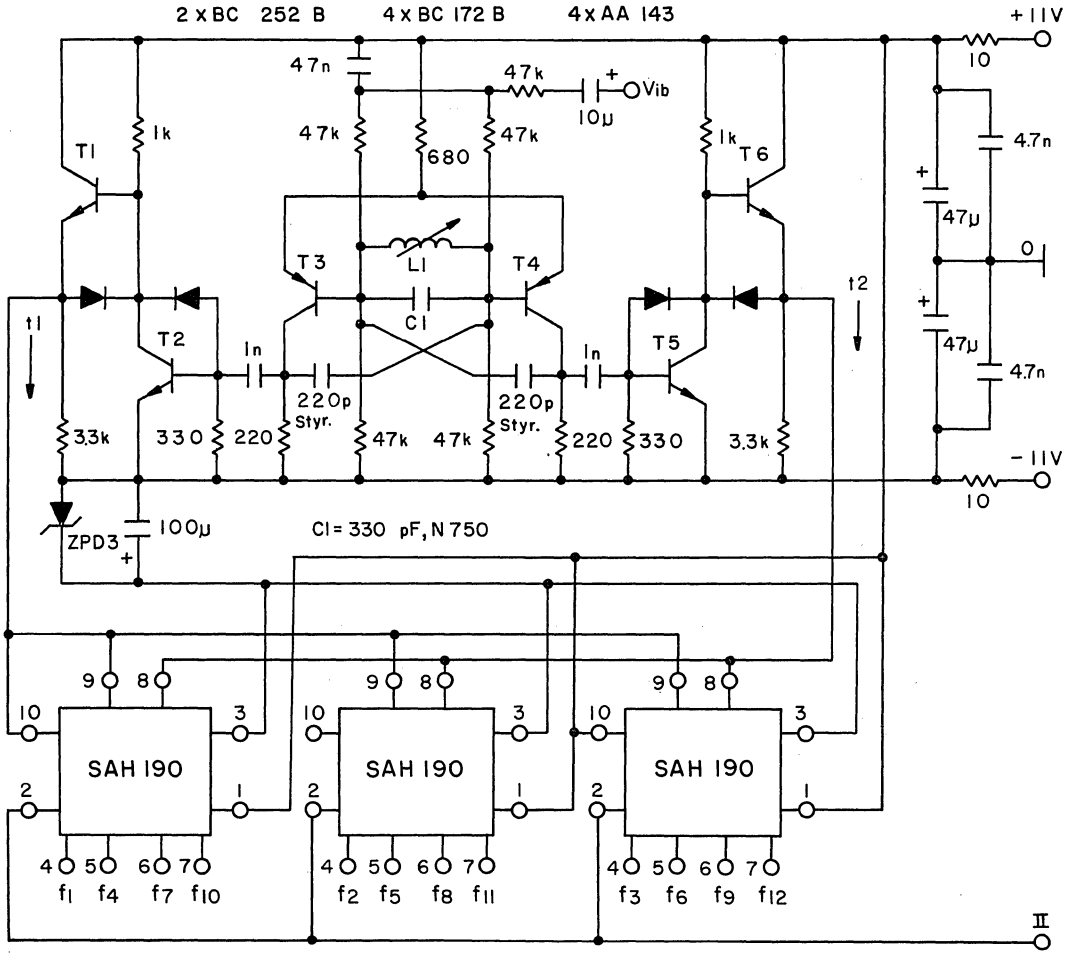


Fig. 12—Circuit diagram of the clock generator with integrated SAH190 circuits connected in accordance with the block diagram of Fig. 2

circuit. An adjustable series inductance of approximately 3 to 10μH can also be used for adjusting the pitch. Care must always be taken to ensure that the symmetry of the oscillator circuit is not impaired.

For each of the two clock pulses the circuit shown in Fig. 12 contains, in addition to the actual oscillator circuit, a pulse shaper consisting of two transistors T1 and T2 or T5 and T6, which ensures short rise and fall times of the pulses of approximately 50 to 80 μs; see also Fig. 11.

The connection of the integrated frequency divider SAJ110 to the outputs of the SAH190 which is schematically indicated in Fig. 3 is shown in more detail in Fig. 13 based on the circuit shown in Fig. 12. As the SAJ110 requires a supply voltage of 10V, and the MOS circuit SAH190 requires a voltage of 20V, it is advisable to provide two stabilized power supplies of +11V, and −11V respectively in the organ, which can be reduced to 10V in each case by the filter resistors which are recommended for each printed circuit board. The linked connections of Option II of the three SAH190 units can, as implied in Fig. 13,

be connected by a single-pole switch with +10V. The twelve output frequencies are one octave lower when the switch is open.

As the clock generator is a high frequency oscillator which can cause radio interference, attention should be given to the applicable regulations.

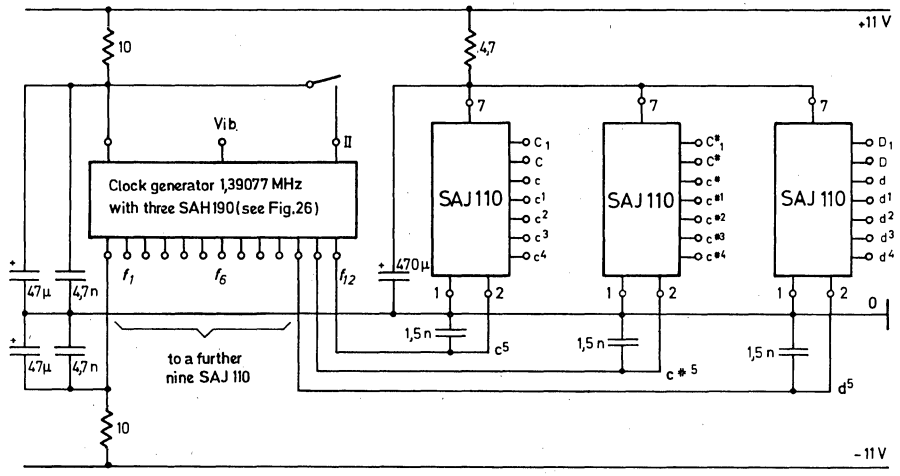


Fig. 13—Connection of the integrated frequency dividers SAJ110 to the circuit shown in Fig. 26

The characteristics of the circuit shown in Fig. 12 are given below.

Supply voltage ..... ±10V

Current consumption
Clock generator alone 45mA

The circuit of Fig. 12 with twelve frequency dividers SAJ110 connected 150mA

Clock frequency adjustable coil ..... 0.8 to 1.6MHz

Vibrato with V_{vib} = 15V peak-to-peak ..... ± one quarter tone

Temperature coefficient of the frequency ..... approx. $3 \times 10^{-5}/^{0}$

Influence of the supply voltage on the frequency ..... approx. 2×10^{-4}/V

GATE FOR ELECTRONIC ORGANS

The TBA470 is a monolithic integrated circuit designed primarily for use in electronic organs. The device incorporates ten transistors, each replacing a mechanical key-contact. Thus it is possible to reduce the numerous mechanical key-contacts on conventional organs (up to ten per key) to one single contact per key. Each of the ten emitters may be driven by a tone-signal. The sum of all signals will be derived from the common collector (terminal 14) or if the signals are supplied into the base terminals, via an integrated diode from terminal 1. Any undesired peaks caused by saturated transistors are suppressed by this diode and an external capacitor.

The TBA470 is delivered in the dual in-line plastic package TO-116 (Fig. 1a, add suffix "A" to type No.). Upon special request it is also available in the quad in-line plastic package (Fig. 1b, add suffix "B" to type No.).

MAXIMUM RATINGS:

I_C	Collector current (terminal 14 or 1)	25mA
I_E	Emitter current (each emitter)	-5mA
I_B	Base current (terminal 7 or 8)	25mA
V_{CEO}	Collector emitter voltage	22V
P_{tot}	Total power dissipation at T_{amb} = 60°C	250mW
T_{amb}	Ambient temperature range	-10 to +60°C

CHARACTERISTICS AT T_{amb} = 25°C (each transistor)

B	DC current gain at V_{CE} = 2V, I_C = 1mA	>40
V_{CEsat}	Collector saturation voltage at I_C = 1mA, I_B = 9.1mA	<0.4V
I_{CEO}	Collector emitter cutoff current at V_{CE} = 15V	<100nA

Dimensions in mm

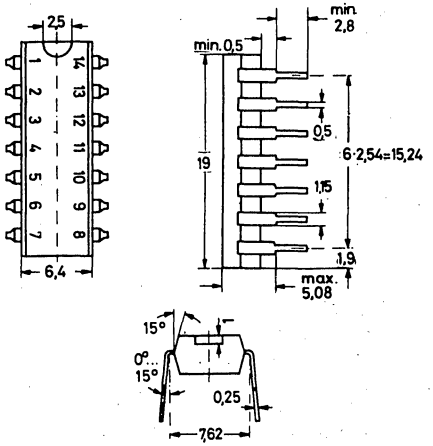


Fig. 1a—TBA470 "A" in dual in-line (Dil) plastic TO-116 package.

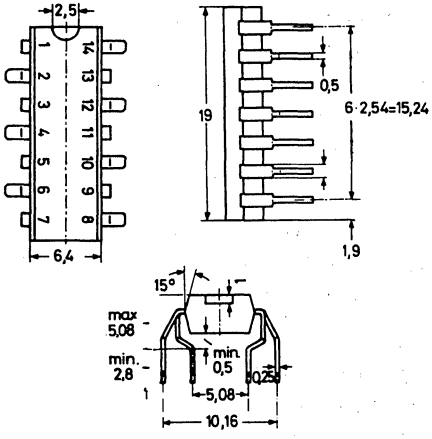


Fig. 1b—TBA470 "B" in quad in-line (Quil) plastic package

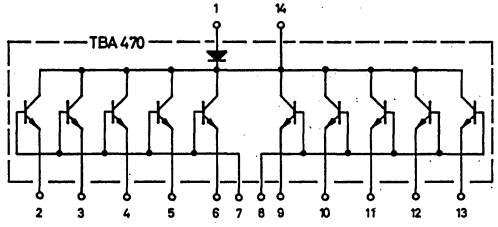


Fig. 2—Circuit Diagram of the TBA470

5 WATT AUDIO AMPLIFIER

- **Usable over 5 - 30V supply voltage range.**
- **Output currents up to 1 amp.**
- **High efficiency 70% at 4 watts output power**
- **Low distortion.**

The TBA 800 is a monolithic class-B power integrated circuit. It is available in a plastic power package similar to TO-116 with 12-pins. These are quad-in-line formed suitable for low cost applications. The package contains heat tabs which allow a power output of 2.5 watts without extra heat sinking. If a suitable extra heat sink e.g. copper area on P.C. board, a power output of 5 watts is possible.

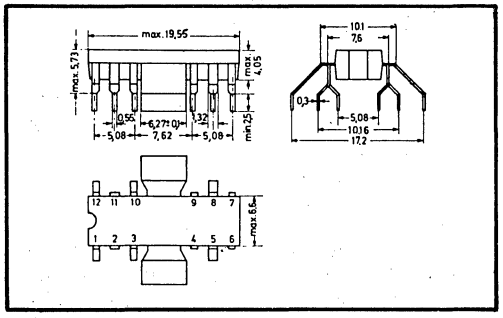


Fig. 1—Package-Power tab plastic dual in-line. Dimensions in mm.

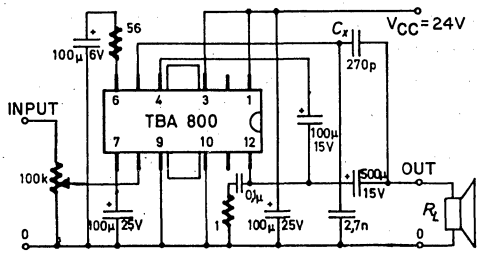


Fig. 2—Test circuit for characteristics.

Maximum Ratings

(All voltages with reference to pins 9 and 10)

V_1, V_3	Supply voltage	30V Max
	Peak output current	
I_{12}	a) (non periodic)	2A Max
I_{12}	b) periodic	1A Max
	Total dissipation	
P_{tot}	a) at Tamb.=70°C	1W Max
P_{tot}	b) at T_{tab}=75°C	5W Max
T_j	Junction temperature	150°C Max
T_s	Storage temperature range	−25 to +85°C

ELECTRICAL CHARACTERISTICS

(at V_{CC}=24V, R_{load}=16Ω, f=1KHz Tamb.=25°C in circuit Fig. 1)

		Min	Typ	Max	Units
V_{12}	Output Quiescent voltage	11	12	13	V
I_1+I_3	Quiescent current .		8.5	20	mA
	Input bias current ..		1		µA
P_o	Output power	5			W
	at THD=10%				
P_o	at THD=2%	4			W
V_8	Input signal (AC) for 5W output ...		70		mV
r_3	Input resistance ...	1	5		mΩ
f_{3dB}	Frequency range 3dB points 35-20,000				Hz
	Total harmonic distortion at P_{out}=0.05−2.5W		0.5		%
A_v	Voltage gain a) with feedback as in Fig. 2 ...	40	43	46	dB
	b) open loop		74		dB
V_n	Noise voltage at Input		10		µV
	Efficiency at P_{out}=4W		70		%
	Thermal resistance				
R_{TH-A}	a) Junction-Ambient		80		°/W
R_{TH-T}	b) Junction-Tab ..		15		°/W

CIRCUIT LAYOUT

RECOMMENDATIONS

The side heat tabs help to ensure that the maximum junction temperature of 150°C is not exceeded. These tabs alone, suffice for output power not exceeding 2.5 watts. However, for high output power extra heat sinking must be provided. For example, the tabs can be soldered to a printed board copper area for heat sinking (Fig. 16) purposes. With a thickness of 35μM the required square side dimension L may be obtained from Fig. 9. This applies for an $T_{amb}=55°C$.

CALCULATION OF REQUIRED COPPER PC BOARD AREA

1) Calculate max. power dissipation

$$P_{tot} = 0.4 \cdot \frac{(V_{CC\,max})^2}{8 \cdot R_L} + V_{CC\,max} \cdot I_{Quiescent}$$

Where $V_{CCmax}=V_{CC}+10\%$ if not stabilized

R_L=load resistance. $I_{Quiescent}$ can be obtained from Fig. 8. For worst case analysis use $I_{Quiescent}$ at 20 mA for 24V supply voltage.

2) From Fig. 9, one can obtain the minimum side length of the square heat sink.

Example

a) $V_{CC}=24V$. unregulated, $R_L=16\Omega$

$$P_{tot}=0.4\ \frac{(24+2.4)2}{8.16}+$$

$$(24+2.4)\times 20\times 10^{-3}=2.6W$$

From Fig. 9 obtain L=app. 25 mm.

For geometries different from the one of Fig. 16 note that copper areas near the tabs have better efficiency as regards power dissipation. Therefore additional safety factors must be added for worst case designs.

b) $V_{CC}=12V$ regulated, $R_L=8\Omega$

$$P_{tot}=0.4\times\frac{12^2}{8.8}+12\times 20\times 10^{-3}=1W$$

From Fig. 9 it is seen that for $T_A\leqslant 55°C$, no extra heat sinks are necessary.

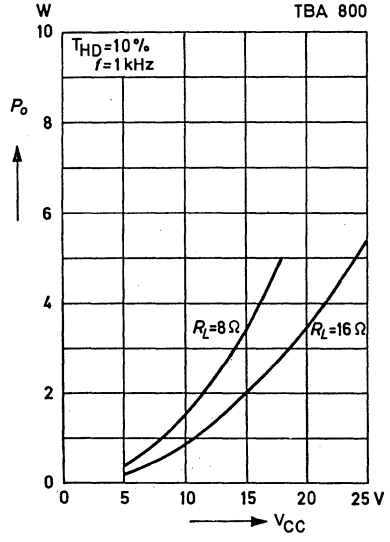


Fig. 3—Output power versus supply voltage (circuit as Fig. 2)

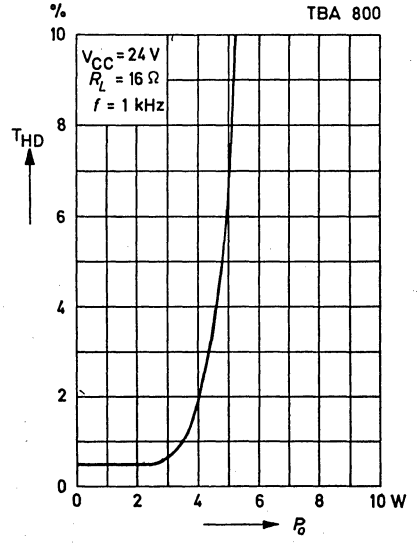


Fig. 4—Total harmonic distortion versus output power (circuit as Fig. 2)

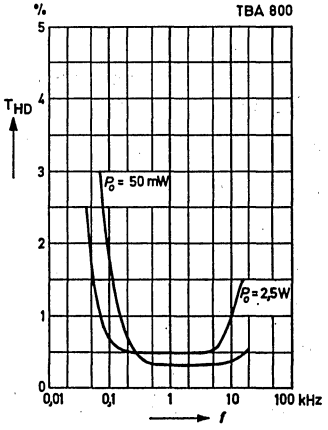


Fig. 5—THD versus frequency (circuit as Fig. 2)

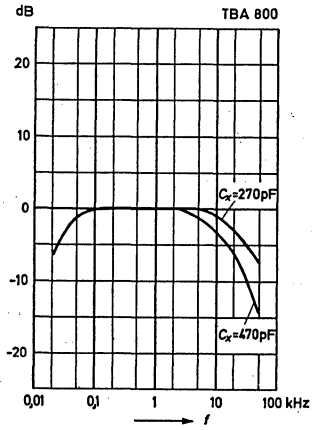


Fig. 6—Frequency range off amplifier of Fig. 2.

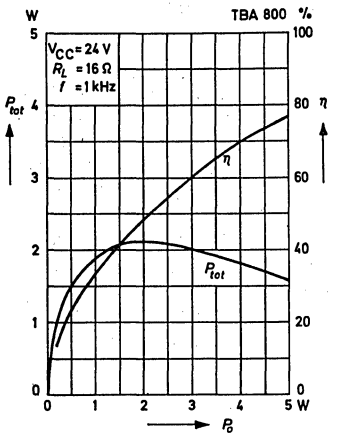


Fig. 7—Power dissipation and efficiency versus output power (circuit as Fig. 2)

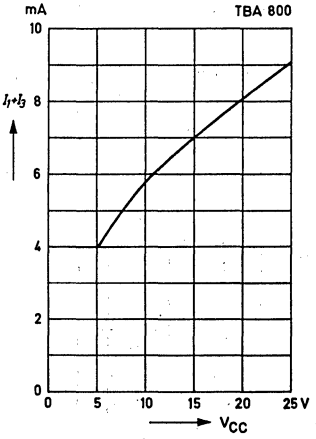


Fig. 8—Quiescent current versus supply voltage (circuit as Fig. 2)

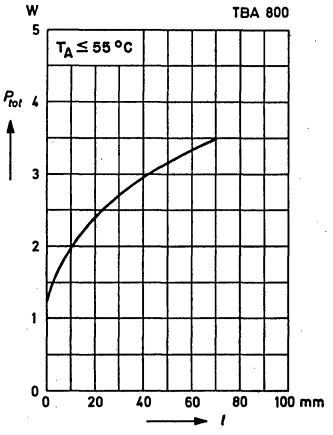


Fig. 9—Total power dissipation versus heat sink length (square heat-sink) for Tambient ≤55 C (See Fig. 16)

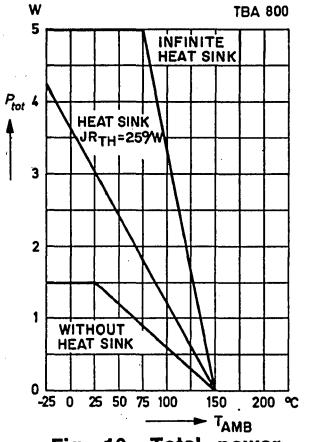


Fig. 10—Total power dissipation versus Ambient temperature.

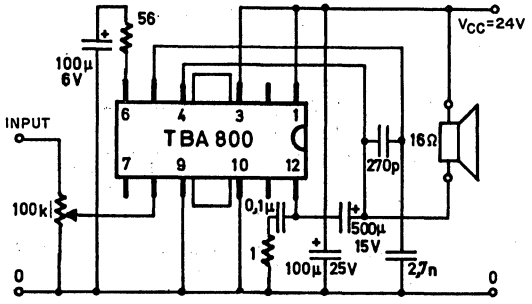


Fig. 11—Application circuit for TBA800 with the loudspeaker connected to positive. This circuit uses minimum external components and is suitable for applications with lower supply voltages.

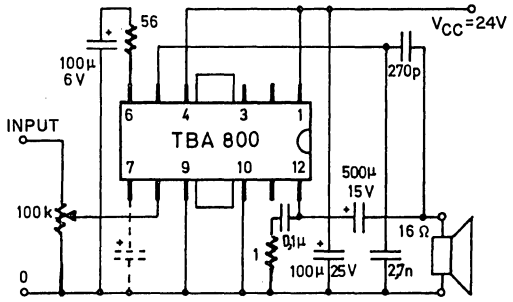


Fig. 12—Application circuit for the TBA800 with the loudspeaker connected to negative or ground. This circuit is more suitable for higher supply voltages due to the bootstrap circuit characteristics. A capacitor from Pin 7 to ground 10 . . 100μF, 25VW will improve hum rejection power supply distortion effects.

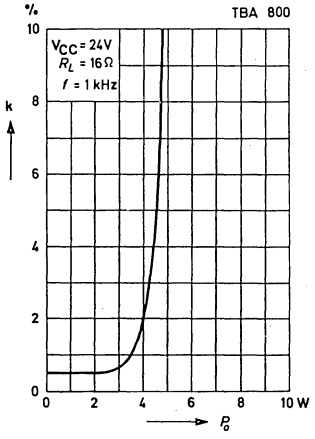


Fig. 13—Total harmonic distortion virsus output power (Circuit as Fig. 12)

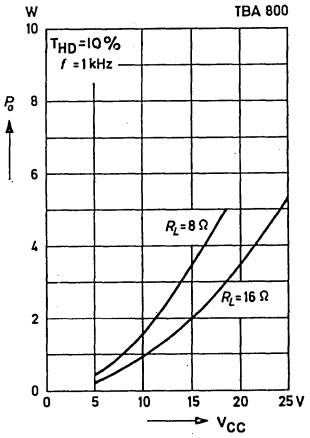


Fig. 14—Output power versus supply voltage (Circuit as in Fig. 12)

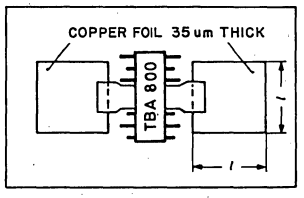


Fig. 16

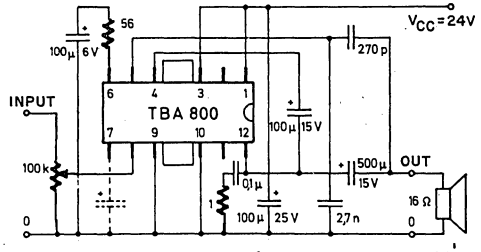


Fig. 15—Application of TBA800. The 100 μF bootstrap capacitor between pins 12 and 14 allows this circuit to provide the same electrical performance as the text circuit of Fig. 2. For use with lower supply voltages e.g. 9 to 14V, a resistor of 150 Ω should be connected between pins 1 & 4. A capacitor from Pin 7 to ground N 10—100μF, 25VW will improve hum rejection and power supply distortion effects.

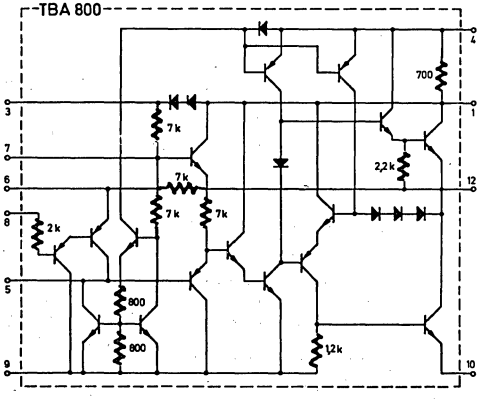


Fig. 17

DUAL FILTER AMPLIFIER

The TCA250 is a monolithic integrated dual-amplifier circuit. The TCA250 is intended for use in active-filters in the audio frequency range and is especially suitable for electronic organ applications.

It consists of two independent amplifiers and features high voltage gain, high input resistance and push-pull output stages.

Connections

1. Output 1
2. Output frequency compensation 1
3. 4. Input frequency compensation 1.
5. Non-inverting input 1 (+)
6. Inverting input 1 (—)
7. −Vcc
8. Inverting input 2 (—)
9. Non-inverting input 2 (+)
10. 11. Input frequency compensation 2
12. Output frequency compensation 2
13. Output 2
14. +Vcc

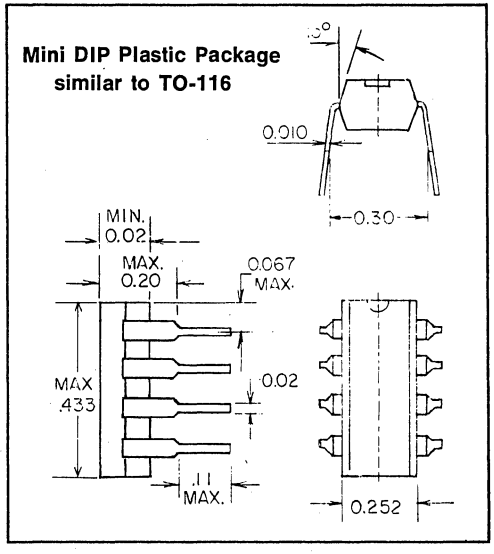
CHARACTERISTICS

at $V_{14} = -V_7 = 9V$, f = 1KHZ, $T_{amb} = 25°C$

G_V	No-load small signal voltage gain	82(72 to 90) dB
f_{3db}	Cut-off frequency of Voltage	>100 KHZ
r_{in}	Input resistance	50 KΩ
r_{out}	Output resistance	200 Ω
$\pm V_{out\ p-p}$	Output Voltage Swing at R_L=1KΩ	5.5(>4.5)V
I_{14}	Current consumption (no load)	5 mA

RECOMMENDED OPERATING CONDITIONS

V_{14}	Supply Voltage	9V
$-V_7$	(Symmetrical)	9V
$V_{14/7}$	(Asymmetrical)	18V



Available in TO-116 dual in-line plastic package

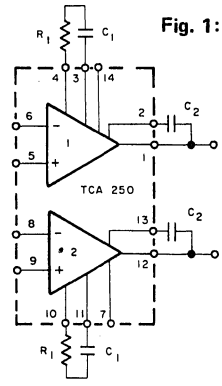


Fig. 1: **Block Diagram**

MAXIMUM RATINGS

V_{14}	Supply Voltage	11V
$-V_7$		11V
V_{in}	Common Mode input Voltage	V_7 to V_{14}
V_D	Differential input Voltage	± 5V
I_A	Output Current	10 mA
$-I_A$		10 mA
T_{amb}	Ambient Temperature Range	0 to +60°C

APPLICATIONS INFORMATION

Circuit example 1: Second order tunable RC lowpass with symmetrical voltage supply.

Using one half of the integrated filter amplifier TCA250 RC lowpass and highpass filters of the 2nd or 3rd orders, as well as selective RC filters can be devised. The lowpass 2nd order shown in Fig. 2 uses very few passive components, is stable and has an adjustable frequency limit f_o.

Adjustments of the cut-off frequency is possible over a relatively large range by varying R2 by the factor, a. When using this circuit as a sine-wave filter in electronic musical instruments, tuning is not necessary if the passive components have tolerances of + 2%.

Table 1:

Component values for a Tschebyscheff-filter with amplification constant within +1.5 dB in the transmission band (fig. 2)

A single-ended voltage supply is also possible; as is shown in the following example.

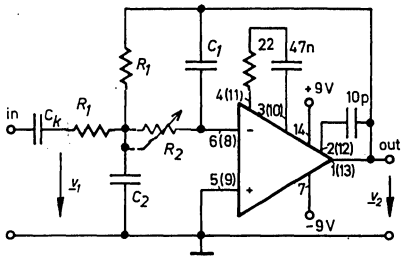
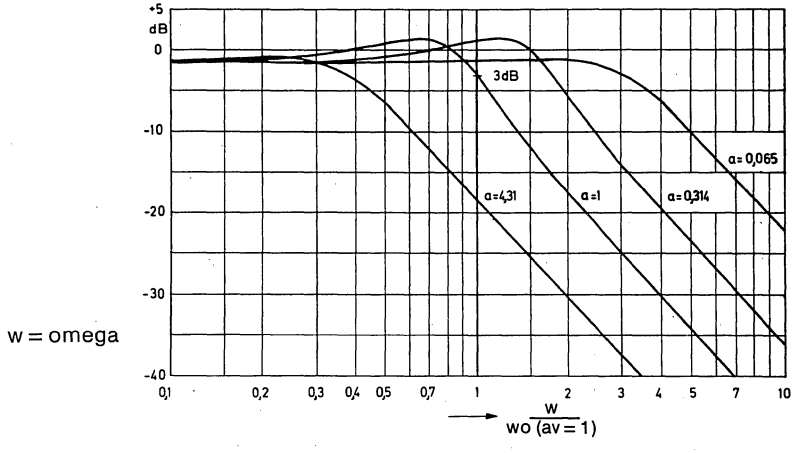


Fig. 2 Tunable Low Pass Filter
2nd order with frequency compensation for Av = 1

fo in the band	C1 nF	C2 nF	R1 K	R2 k
16Hz - 250Hz	6.8	100	$\frac{1000Hz}{f_o}$ 7.318	$\frac{1000Hz}{f_o}$ 8.466
250Hz - 16Hz	1	15	$\frac{1000Hz}{f_o}$ 55.04	$\frac{1000Hz}{f_o}$ 51.02

With the circuit values of table 1 the characteristic a = 1, in fig. 3 is obtained.

Fig. 3 — Frequency Response of Low Pass Filter of Fig. 2, a: Variation of R2



w = omega

Circuit example 2:
Fourth order RC lowpass with single-ended voltage supply

By arranging two 2nd order lowpass filters in series a 4th order filter is obtained. Other circuit values are necessary, however, (see fig. 4 and table 2). The frequency characteristic given by the values of table 2 is shown in fig. 5. When using single-ended supply voltages the non-inverting inputs of the amplifier are connected to a voltage divider and decoupled.

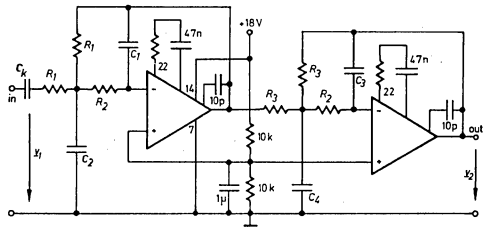


Fig. 4 — Low Pass 4th Order with Frequency Compensation for AV = 1

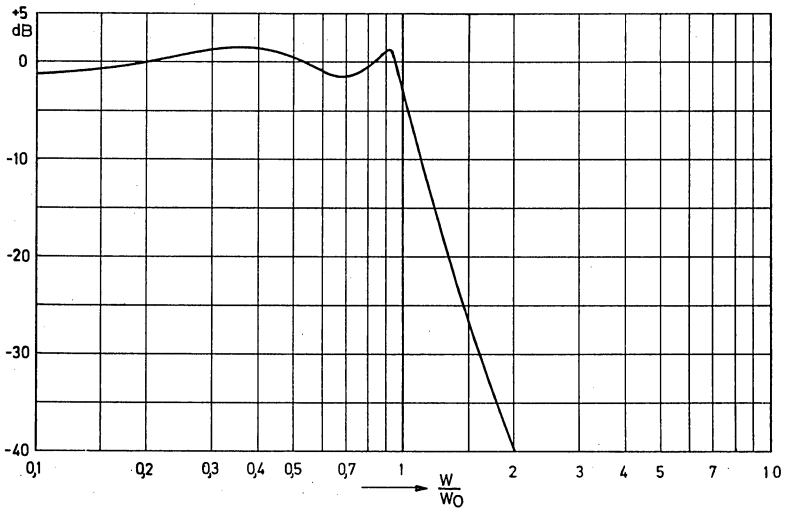


Fig. 5 — Frequency Response of Low Pass Filter of Fig. 4

Table 2:

Component values for the Tschebyscheff-filter shown in fig. 4, having amplification constant within +1.5 dB in the transmission band

Vo in the band	C1 nF	C2 nF	C3 nF	C4 nF	R1 k	R2 k	R3/k
16Hz - 250Hz	22	220	2.2	680	1000Hz/fo 5.6	1000Hz/fo 4.94	1000Hz/fo 4.01
250Hz - 16kHz	2.2	22	0.22	68	1000Hz/fo 56	1000Hz/fo 49.4	1000Hz/fo 40.1

SYNCHRONOUS DEMODULATOR

The TCA270 is a monolithic integrated circuit designed for use in colour and monochrome television receivers. It consists of a synchronous demodulator, video amplifier with buffer output stages, noise inverters, AGC detector with output stages for npn tuner and IF amplifiers, and AFC demodulator with buffer output stage. Opposite polarity video signals are available from emitter followers.

Normally the TCA270 is delivered in dual-in-line plastic packages (similar to TO-116) (see Fig. 1). Upon special request it is also available in the quad-in-line plastic package (see Fig. 2).

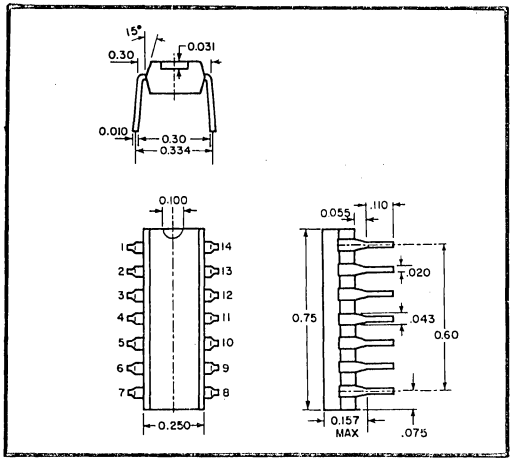


Fig. 1—TCA270A in dual-in-line plastic TO-116 package.

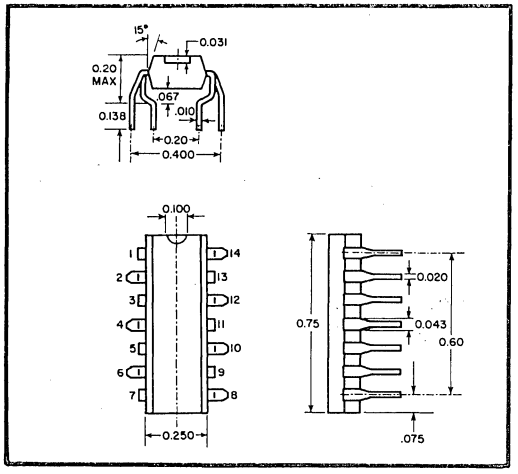


Fig. 2—TCA270B in quad-in-line plastic package.

Electrical Characteristics **Typ.**

V_S	Supply voltage range	12.0(10.1-13.8)V
I_S	Supply current range	47(33-59)mA
V_o	Quiescent output voltage both outputs)	+6V
V_o	Output voltage at start of AGC (pin 9)	+3V
V_i	Unbalanced RMS input voltage for AGC	70 (50-100)mV
R_i	Input resistance (both inputs)	3KΩ
	3dB band width of video output	5MHz
	Differential gain (see note 1)	10max %
	Differential phase (see note 1)	10max deg.
	Intermodulation products (blue colour bar)	
	1.6MHz	−60dB
	2.8MHz	−67dB
	Carrier frequency rejection at outputs	−40min dB
	Twice carrier frequency rejection at outputs	−40min dB

Absolute Maximum Ratings

V_S	Supply voltage	18V
P_{tot}	Total power dissipation	1W
T_{amb}	Operating temperature range	−25 to 55°
T_S	Storage temperature range	−25 to 125°C

TCA270
SYNCHRONOUS DEMODULATOR

AGC

V_{sat}(pin 4)	Saturation voltage of tuner control at 10ma ..... +0.3V
V_o (pin 5)	Saturation voltage of IF control at 10mA .. 0.7min, 1.2max V
V_{BR}	Breakdown voltage at 1mA (pin 4 & 5) ..... 14min V
I_o	Control current (pin 4 & 5) ..... 10min mA
	Signal expansion for complete AGC ..... 0.5max dB
	AGC gating (optional) by negative line fly back pulse
	V_i ..... 2min, $V_S$max V
	R_i 1.8KΩ
	Current ratio of unsaturated outputs 14/15 for I_5=1mA 6min

AFC

Output control voltage swing (pk-pk) 10minV

Change of frequency for complete output voltage swing 400maxKHz

Change of frequency to maintain peak output voltage ..... ±1min MHz

Noise Inverters (see note 2)

Negative going noise pulses in pin 9 inversion threshold ..... ±2.55V

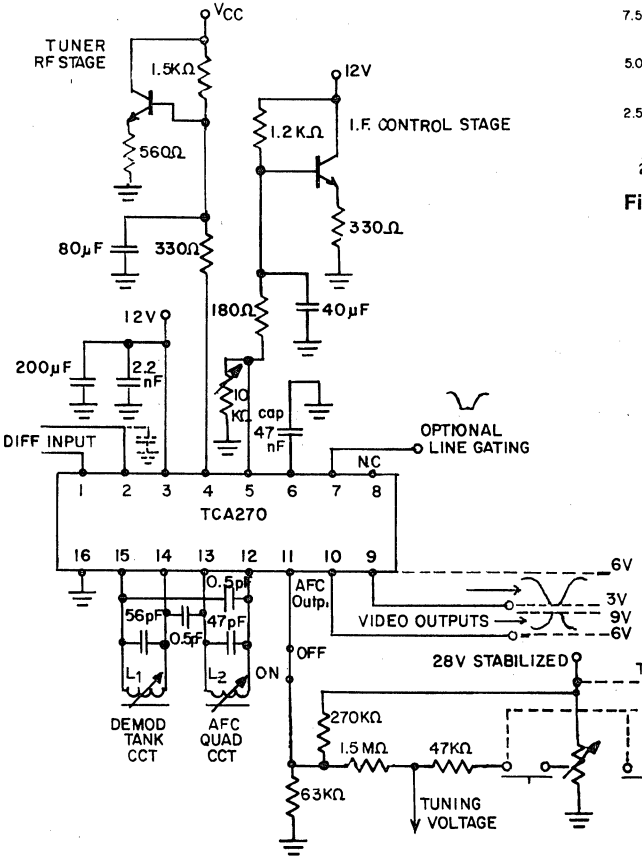
Positive going noise pulses in pin 9 inversion threshold ..... ±6.6V

NOTES

1. CC1R system of modulation, peak white= 10% carrier

2. Noise pulses are inverted to a point near black level

Fig. 4—Typical Application



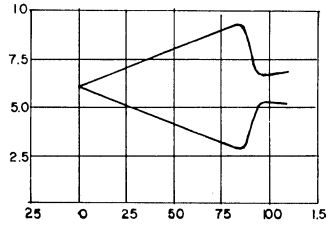


Fig. 5—Transfer Characteristic

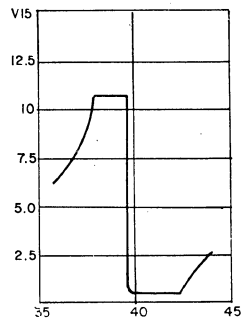


Fig. 6—AFC Characteristic

ANALOG SHIFT REGISTER (DELAY LINE)

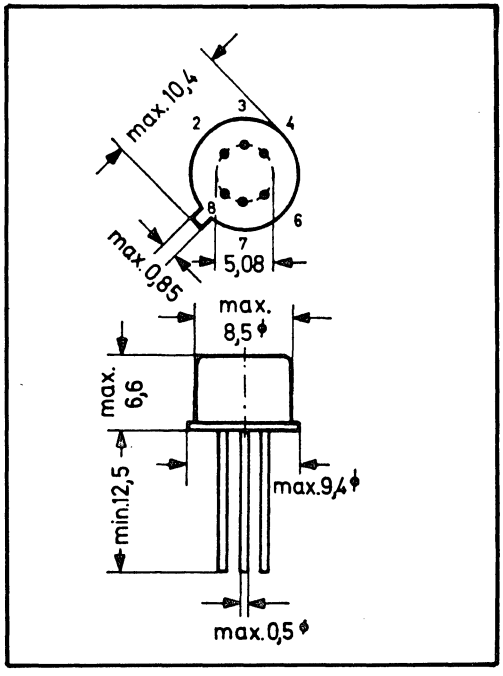


Fig. 1—TCA350 in metal package JEDEC TO-77 (≈TO-5 with 6 leads)

Features

- 185 stage "Bucket-Brigade"
- Delay line for audio frequencies
- Symmetrical clock inputs up to 500 KHz
- Variable delay $t_D = \frac{185}{2f_{clock}}$

The TCA350 is a monolithic integrated circuit using MOS technology for the delay of analog signals up to 250 KHz. It uses the "bucket-brigade" principle and consists of 185 series-connected MOS transistors together with 185 integrated capacitors.

Maximum Ratings

V_{DD}	Drain voltage	−30 to +0.3V
V_E	Input voltage	−30 to +0.3V
V_{t1}, V_{t2}	Clock voltages	−30 to +0.3V
I_A	Output current	−5mA
T_S	Storage temperature range	−40 to +100°C

Recommended Operating Conditions

V_{DD}	Drain voltage	−24V
V_{t1}, V_{t2}	Clock voltages	−19(−18 to 20)V
f_{clock}	Clock frequency	5 to 500KHz
t_1/t	Duty cycle of clock	0.25
t_2/T	(T=1/f_{clock})	0.25
V_E	Input bias voltage	−8(−7.5 to −8.5)V
$\frac{R_1 \times R_2}{R_1 + R_2}$	Biasing resistance at input	<20KΩ
$V_{E\ pk-pk}$	Input signal amplitude	<6V
T_A	Ambient temperature range	−20 to +60°C

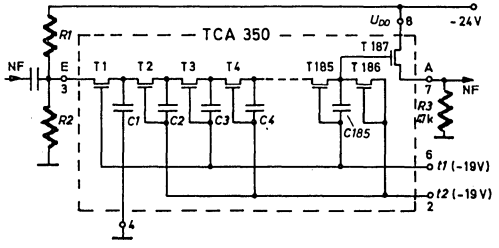


Fig. 2—TCA350

CHARACTERISTICS

Attenuation with R_3=47k	G	4	dB
Delay time	$t_D = \frac{185}{2f_{clock}}$		

OPERATION AND APPLICATION INFORMATION

Fig. 2 shows the internal circuit of the TCA-350 and associated external components. The output transistor requires a drain voltage of −24V; the input bias voltage of ≈-8V should be generated from the above —24V by using a potentiometer R_1, R_2. The output stage T_{187} is a source follower and the output signal is developed across R_3 (47KΩ). If this resistor is replaced by a 0.5mA current source, the signal damping (loss) and distortion are improved. The output signal has clock pulses superimposed and a suitable filter must be used.

The clock generator must be designed to supply pins t_1 and t_2, non-overlapping antiphase pulses of ≈−19 volts each. According to the Sampling Theorem, the clock frequency should at least be double the frequency of the highest signal frequency.

The principle of delaying a signal using "bucket-brigades" is almost equivalent to sampling methods of Joubert and experiments with osillography and high frequency oscilloscopes.

Each period of the signal to be delayed is sampled by consecutive pulses which shift one-after-the-other through the bucket brigade. Thus each is delayed by a time depending on the clock frequency and the number of buckets. TCA350 has 185 buckets. Thus

$$\text{Delay} \quad t_D = \frac{185}{2f_{clock}}$$

The clock pulses at the output and must be filtered out in order to obtain the original signal. An active low-pass filter connected to the source of output transistor T_{187} is a convenient method.

QUAD RC-OSCILLATOR

The monolithic integrated circuit TCA430-N contains four RC oscillators in one package and is designed for use in electronic organs. Three TCA430-N integrated circuits provide the twelve master oscillators of the highest octave. The symmetrical square wave output signals of the oscillators are suitable for driving the integrated frequency divider SAJ 110, with which the lower octaves are obtained. Since the TCA430 is thermally neutral, the frequency stability of the oscillators is solely dependent on the temperature coefficients of the frequency determining RC elements. A vibrato effect can be generated for all the oscillators via the vibrato input Pin 4. The TCA430-N replaces the TCA430, differing in pin configuration only. Pins 5 and 8 have been exchanged.

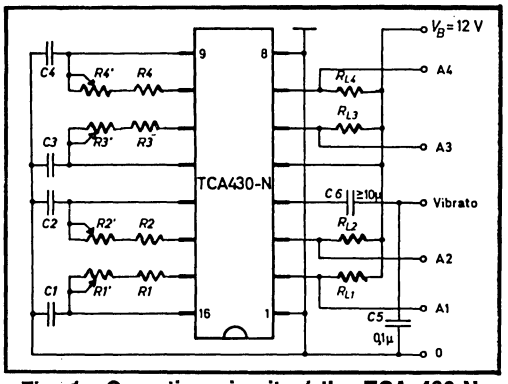


Fig. 1—Operating circuit of the TCA 430-N

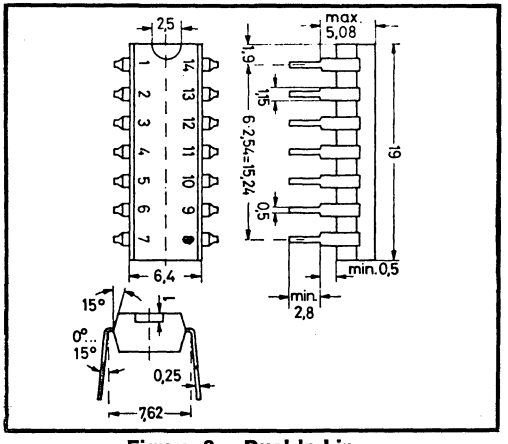


Figure 2 Dual-In-Line

MAXIMUM RATINGS

(All voltages referred to Pin 1)

V_B	Supply voltage	15V
I_2, I_3, I_6, I_7	Output current	7.5mA
V_{4pp}	Vibrato voltage, peak-to-peak, (pin 4 must be driven via a capacitor)	6V
T_{amb}	Ambient temperature range	−10 to +60°C
T_s	Storage temperature range	−30 to 125°C

RECOMMENDED OPERATING CONDITIONS

V_B	Supply voltage	12(>9)V
R_{L1} to R_{L4}	Load resistors	3.3(>2)kΩ
R_1 to R_4	Frequency-determining resistors (Metal film resistors with a temp. coefficient $\leqslant 50\times10^{-6}$/°C)	5 to 50 kΩ
C_1 to C_4	Frequency-determining capacitors (MKC polycarbonate foil capacitors)	⩽1F
f_o	Oscillator frequency	20 to 30,000Hz

CHARACTERISTICS

at V_B=12V, R_{L1} to R_{L4}=3.3 kΩ, T_{amb}=25°C

I_5	Current consumption	22mA
V_{ol}	Output voltage at low state	<0.5V
V_{oh}	Output voltage at high state	V_B
υ	Pulse duty factor of the square wave output voltage	0.5V
f_o	Oscillator frequency $\frac{865}{R/k\Omega \cdot C/\mu F}$ Hz	
$r_4/_1$	Input resistance of the vibrato circuit	4kΩ
	Slope of the vibrato circuit For a vibrato of ± one semitone, a peak-to-peak voltage of 1.7V is required at pin 4.	
$\Delta f_o/f_o$	Change of oscillator frequency in the supply voltage range V_B=12V ± 3V	±0.05%

ZTK6.8 to ZTK33 (TAA550)
MONOLITHIC TEMPERATURE COMPENSATED ZENER DIODE

Monolithic linear integrated circuits producing an extremely constant temperature-compensated voltage, particularly suitable for stabilizing the tuning voltage in television and radio tuners employing capacitance diodes. The effects of differential resistance and temperature coefficient on stabilized voltage are very small compared to those of conventional Zener diodes and a high stability circuit can be achieved using fewer additional components.

MAXIMUM RATINGS

Zener Current	@ T_{amb}=45°C with heat sink		@T_C=45°C
ZTK 6.8 Iz	36	60	90 mA
ZTK 9 Iz	27	38	63 mA
ZTK 11 Iz	19	31	53 mA
ZTK 18 Iz	13	19	32 mA
ZTK 22 Iz	10	16	27 mA
ZTK 27 Iz	8	13	22 mA
ZTK 33 Iz (TAA550)	7	11	19 mA

Junction temperature T_j 150°C

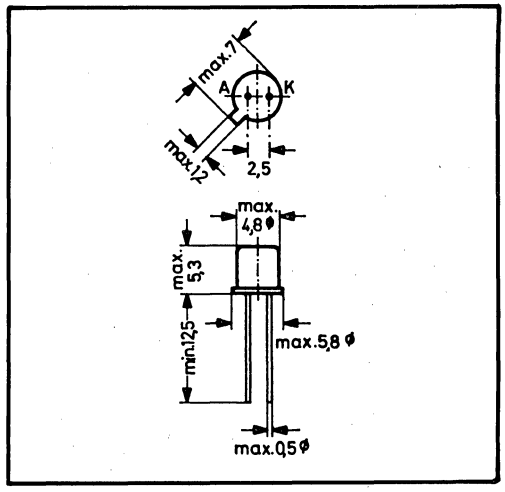
Storage temperature range T_s —20 to +150°C

(T_C=Case Temperature)

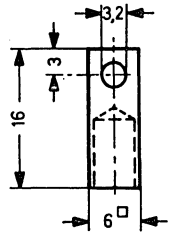
CHARACTERISTICS @ T_{amb}=25°C

Type	Zener voltage @ I_z=5mA V_zV	Dynamic resistance @ I_z=5mA $r_{zi}\Omega$
ZTK 6.8	6.5 to 7.2	10 (<25)
ZTK 9	8 to 10	10 (<25)
ZTK 11	10 to 12	10 (<25)
ZTK 18	16 to 20	11 (<25)
ZTK 22	20 to 24	11 (<25)
ZTK 27	24 to 30	12 (<25)
ZTK 33 (TAA550)	30 to 36	12 (<25)

a_{vz} Temperature coefficient of Zener voltage @ I_z=5mA ±0.5mA ..... —2(—10 to +5)10 —5/°C



Metal case JEDEC TO-18 Weight approximately 0.3 g Cathode connected to case. Dimensions in mm.



Accessory—A heat sink, Order No. 00409, will be delivered on request. Dimensions in mm.

Thermal resistance

R_{thC} Junction to case ..... 0.15°C/mW

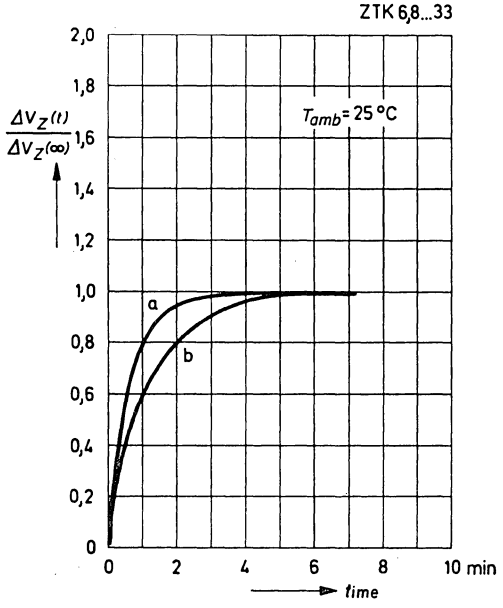
R_{thA} Junction to ambient air .. 0.4°C/mW

R_{thA} Junction to ambient air with heat sink ..... 0.25°C/mW

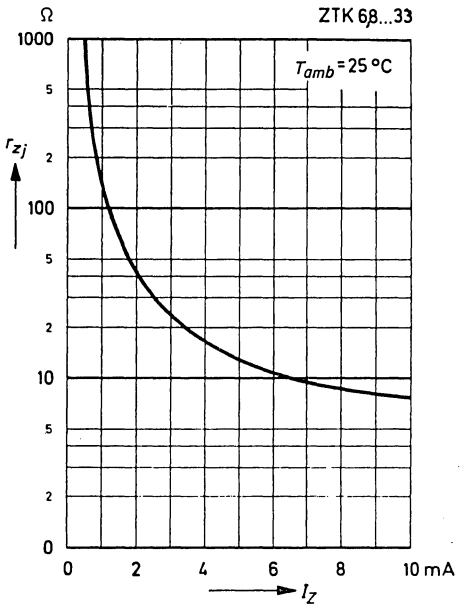
ZTK 6.8 to ZTK 33

Relative change of ΔV_z versus time starting at turn-on
a) without
b) with heat sink No. 00409

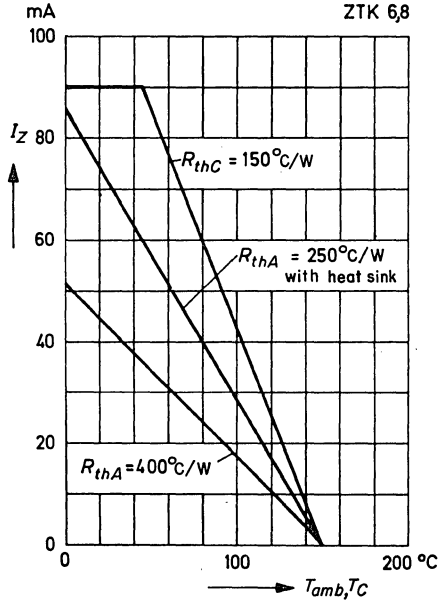
Dynamic resistance versus Zener current



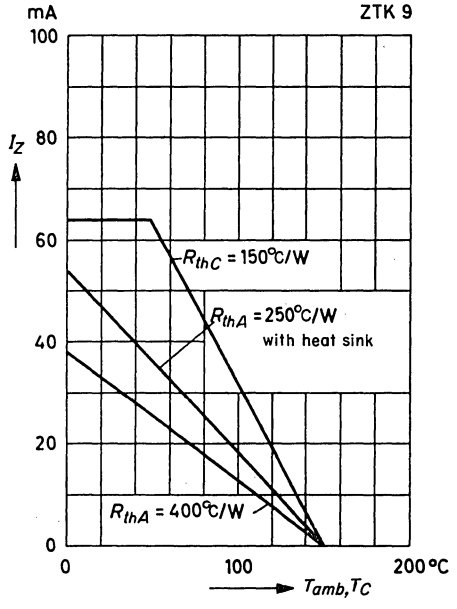
Admissible Zener current versus temperature



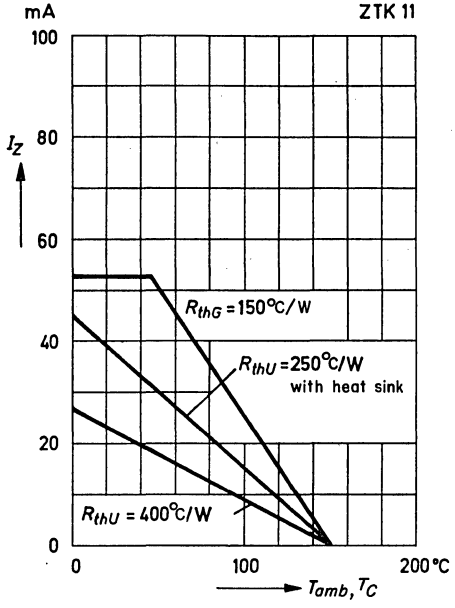
Admissible Zener current versus temperature



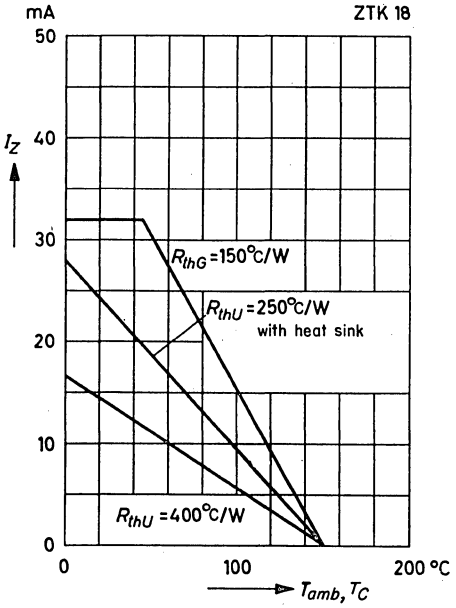
Admissible Zener current versus temperature



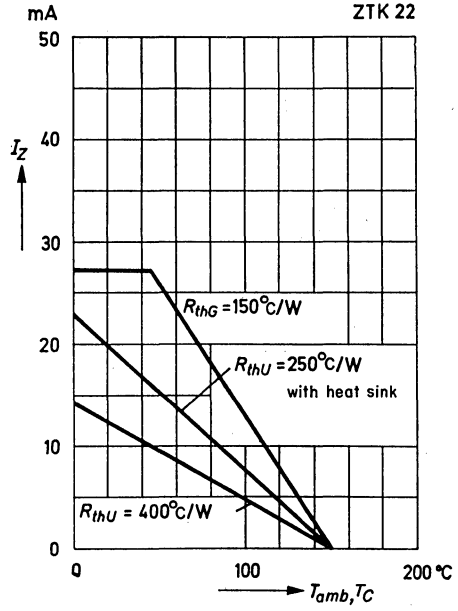
Admissible Zener current versus temperature



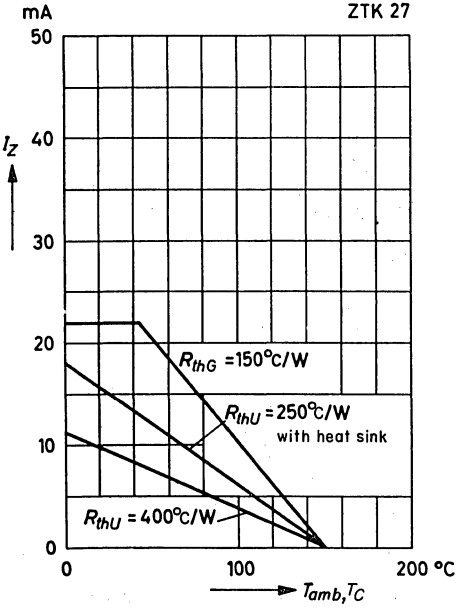
Admissible Zener current versus temperature



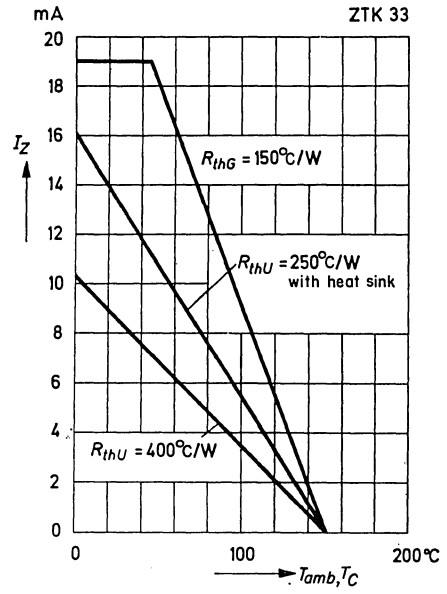
Admissible Zener current versus temperature



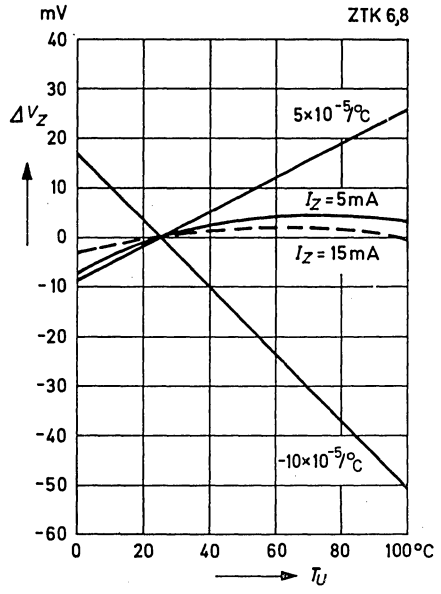
Admissible Zener current versus temperature



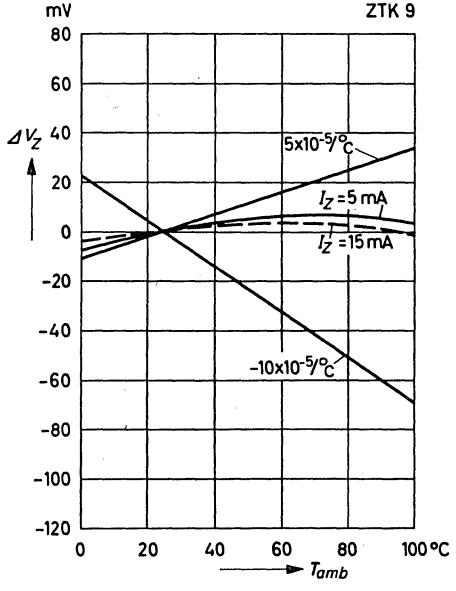
Admissible Zener current versus temperature



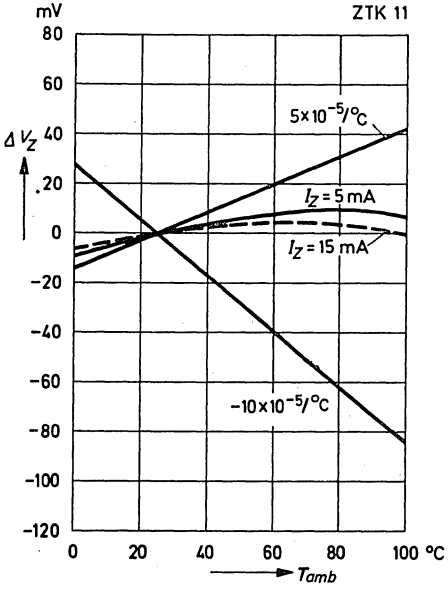
Change of Zener voltage versus ambient temperature



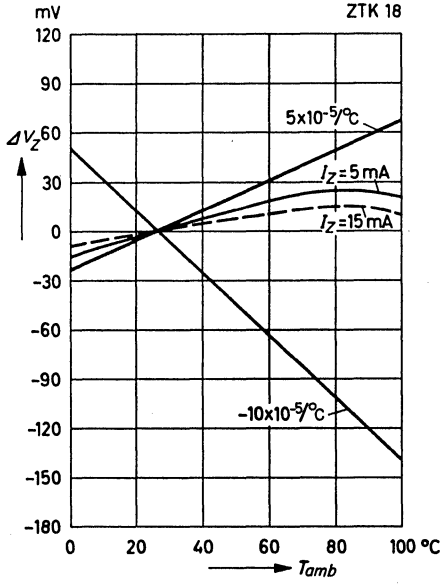
Change of Zener voltage versus ambient temperature



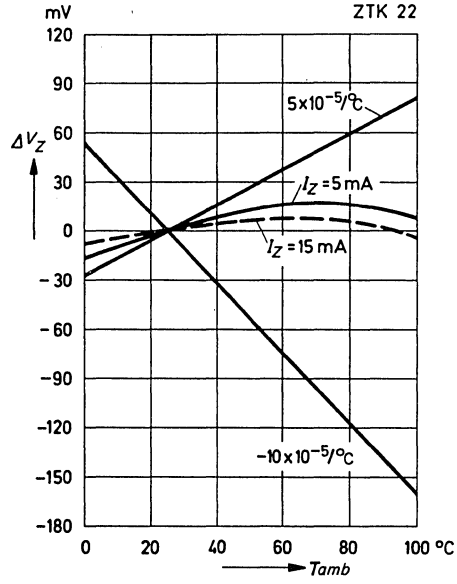
Change of Zener voltage versus ambient temperature



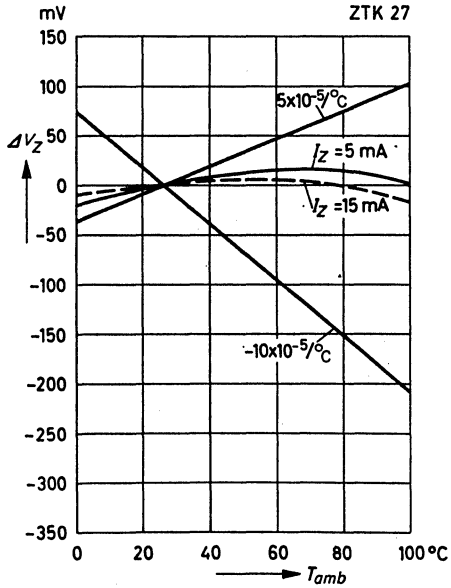
Change of Zener voltage versus ambient temperature



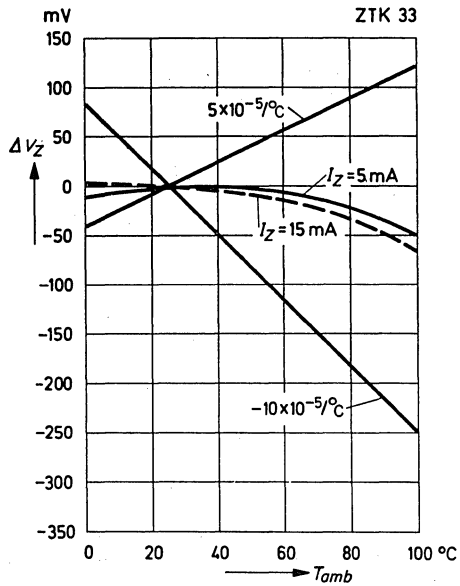
Change of Zener voltage versus ambient temperature



Change of Zener voltage versus ambient temperature



Change of Zener voltage versus ambient temperature



Change of Zener voltage versus ambient temperature

MONOLITHIC TEMPERATURE COMPENSATED ZENER DIODE

Monolithic linear integrated circuit producing an extremely constant temperature-compensated voltage, particularly suitable for stabilizing the tuning voltage in Television and Radio tuners employing capacitance diodes. This device is available in a low-cost diode package.

CHARACTERISTICS

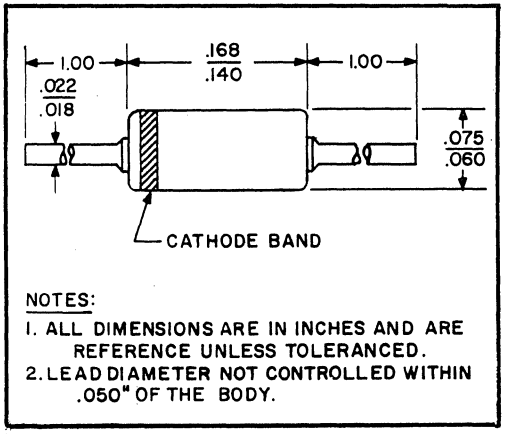
(At $T_{amb}=25°C$, $I_z=5mA$)

V_z	Reference voltage	30 to 36V
r_{zi}	Inherent Dynamic Resistance	13(<25)Ω
$\propto V_z$	Temp. Coefficient of Reference Voltage at $I_z=5mA+0.5mA$ with Range T_{amb} 20°C to 60°C	$-2(-10$ to $+5)\times10^{-5}$/°C
t_{th}	Thermal Time Constant (turn-on)	20 sec.**
R_{thj-a}	Thermal Resistance Junction to air	<0.3°C/mW*

*This value applies when the connection leads 8mm from the package and are maintained at ambient temperature.

**At the end of the thermal time constant (turn-on) 90% of the reference voltage ΔV_{zmax} spread fades away.

$\Delta V_{zmax}=V_z(\infty)-V_z(O)$
with $V_z(O)=V_z$ at instant of switch-on.
and $V_z(\infty)=V_z$ when thermal stability (balance) is reached.



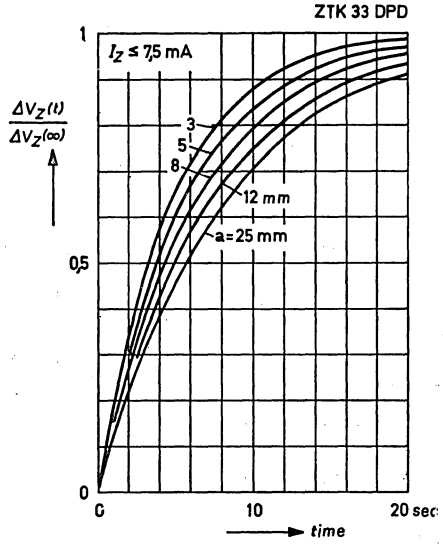
NOTES:
1. ALL DIMENSIONS ARE IN INCHES AND ARE REFERENCE UNLESS TOLERANCED.
2. LEAD DIAMETER NOT CONTROLLED WITHIN .050" OF THE BODY.

Package—Jedec DO-35 Double Plug Diode Type

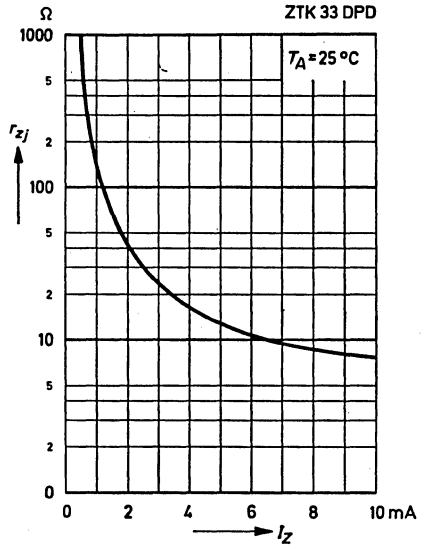
MAXIMUM RATINGS

I_z	Operating Current at $T_{amb}=45°C$	10mA*
T_j	Junction Temperature	150°C
T_s	Storage Temperature Range	−20 to +150°C

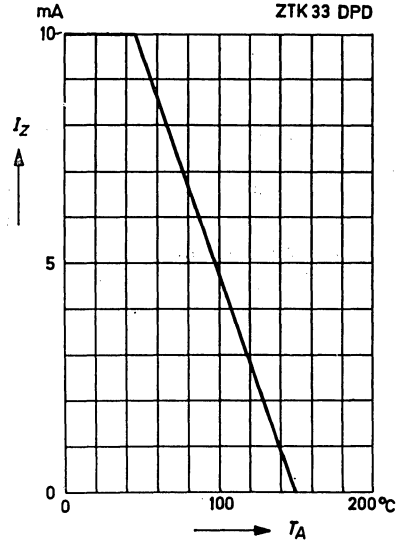
ZTK33DPD
MONOLITHIC TEMPERATURE COMPENSATED ZENER DIODE



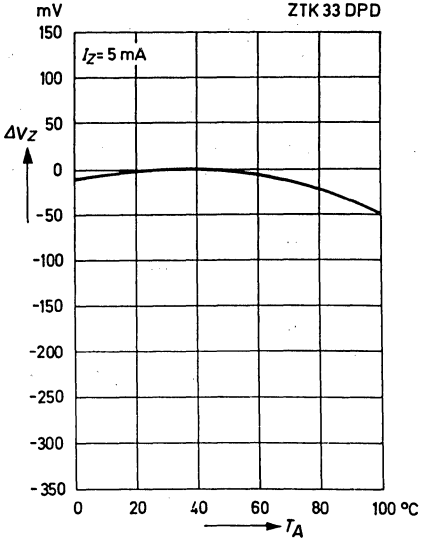
Curves showing relationships of ΔV_z after switch-on for different lead lengths between the package and solder point maintained at ambient temperature.



Inherent Dynamic resistance versus operating current.



Permissible operating current versus ambient temperature
(see note*)



Change of reference voltage versus ambient temperature

CAMERA INTEGRATED CIRCUIT

A monolithic integrated cricuit for the control and monitoring of all functions of an electronic (single-shot) camera. Fig. 2 shows the circuit diagram of such a camera using the UAA-110. In order to avoid over-exposure while taking brightly-lit scenes and camera movement in dim light, a measurement phase precedes the automatic setting of the exposure time. In this phase, the light intensity is measured as the shutter release is depressed half way. The indicator-lamps L_U (over-exposure indicator) and L_S (tripod-indicator) show respectively whether the aperture must be reduced or whether a tripod (or a larger aperture) should be used. For this purpose two voltage comparators are used which are driven during the measurement-phase from the photo-resistor R_F. In addition, the state of the battery can be checked by blocking, (with the finger, for example) the light to the photoresistor. If the lamp L_S does not light, the batter is exhausted. If the shutter-release is fully depressed, the photoresistor is connected to the integrated capacitor at input of the threshold amplifier. At the same time, the shutter is opened and held open with a latch during the exposure. The exposure time is determined by the charging of the capacitor C_F through the photoresistor whose resistance is dependent of the illumination. When the voltage on the capacitor reaches the threshold voltage of the amplifier (determined by the voltage divider R_y, R_x) the electromagnet M is activated and the shutter latch is released, permitting the shutter to be closed by means of a spring.

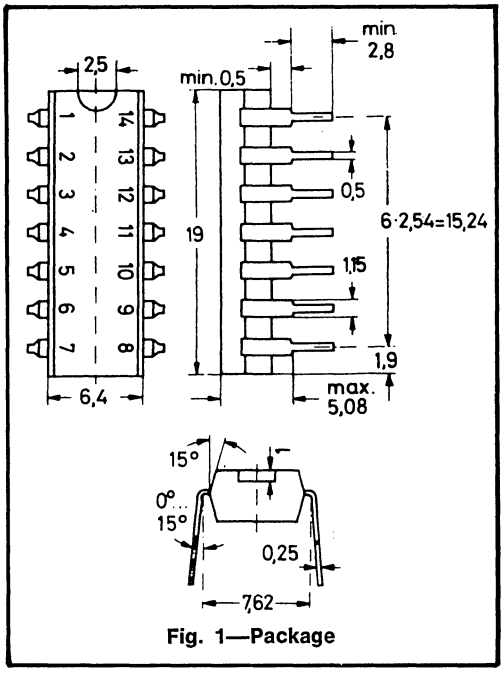


Fig. 1—Package

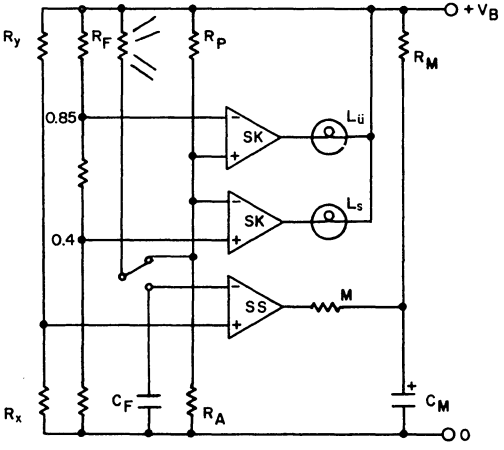


Fig. 2—Block diagram of camera

RECOMMENDED OPERATING CONDITIONS
(see the circuit of fig. 3)

V_B	Supply voltage	3,5 to 6V
V	Potential divider ratio	0,55 to 0,8
R_F	Photoresistor	100 to $2x10^7\Omega$
R_{isol}	Insulation resistance	$>250M\Omega$
T_A	Ambient temperature range	-18 to $+50°C$

UAA110
CAMERA INTEGRATED CIRCUIT

All voltages are referred to Pins 4 + 7.

Definitions

Operating voltage limit
(lowest voltage) V_{9A}: maximum supply voltage at which the voltage $V_2 > 2{,}5$ V for a specified value of X

Potential divider ratio ..... $X = \frac{R_A}{R_A + R_P} = \frac{V_{12}}{V_9}$

Equivalent resistance ..... $R_P = \frac{R_P \times R_F}{R_P + R_F}$

Potential divider ratio ..... $V = \frac{R_X}{R_X + R_Y} = \frac{V_{11}}{V_9}$

Delay time ..... $t_v = R_F \times C_F \times 1n \frac{1}{1{,}043 - V}$

Insulation resistance ..... $R_{isol} = \frac{R_C \times R_S}{R_C + R_S}$

R_S = insulation resistance of the printed circuit board and R_C = insulation resistance of the capacitor C_F

MAXIMUM RATINGS

V_9	Supply voltage	6,5V
I_1, I_2	Output pulse currents at an operating frequency 1Hz Lamp current, pulse duration <50ms	120mA
I_8	Electromagnetic coil current, pulse duration <5ms	350mA
I_1, I_2	Lamp current, continuous	40mA
I_8	Reverse current while switching an inductive load	−20mA
T_S	Storage temperature range	−30 to +70°C

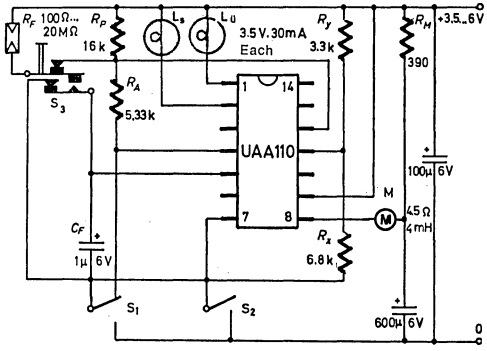


Fig. 3—Measurement circuit for UAA110

MEASUREMENT CONDITIONS FOR THE CHARACTERISTICS
(see measurement circuit, fig. 4)

V_9	Supply voltage (± 1%)	5V
T_A	Ambient temperature	23 to 25°C
V_1,V_2,V_8	Output voltages in "L" state ..	<1,4V
V_1,V_2,V_8	Output voltages in "H" state ..	>4,5V
P_1,P_2	Threshold potentiometer	1kΩ
P_3	Reference potentiometer	10kΩ
V_{11}	Reference voltage (± 0.1%) ..	3,375V
R_{L1},R_{L2}	Equivalent resistance of the lamps	133Ω
R_M	Equivalent resistance to the electro-magnet	13,3Ω

CHARACTERISTICS MEASURED UNDER THE ABOVE MENTIONED CONDITIONS

I_9	Current consumption at V_{12} =2,5V, V_4 = 0	<6mA
I_9	at V_5 = 1V, V_4 = 5V	<6mA
I_8	Output leakage current at V_9 = 6V, V_4 = 0	<0,1mA
I_5	Input curent at V_5 = 2V	<8nA
I_{5t}	Input switching current at V_5 = V_{5t}	<25nA
I_{12}	Input current at V_{12} = 4,35V, V_4 = 0	<2µA
	Saturation voltage	
V_{1sat}	at V_{12} = 5V, V_4 = 0	<1,2V
V_{2sat}	at V_{12} = 0, V_4 = 0	<1,2V
V_{8sat}	at V_5 = 5V, V_4 = 5V	<1,3V
V_{12s}	"Tripod"-threshold volt. range at V_4 = 5V	1,9 to 2,11V
V_{12u}	Over-exposure threshold volt. range at V_4 = 0	4.14 to 4.35V
V_{5t}	Exposure-time threshold volt. range at V_4 = 5V ..	2,97 to 3,335V
	Relative exposure-time error	
$\pm\Delta t_v/t_v$	at V_4=V_9=3,5 to 6V	<15%
$+\Delta t_v/t_v$	at R_F 10MΩ, T_A=24°C	<30%
$-\Delta t_v/t_v$	at R_F 10MΩ, T_A=−18 to +50°C	<25%
$+\Delta t_v/t_v$	at R_F=20MΩ, T_A=24°C ...	<100%
$-\Delta t_v/t_v$	.....	<30%
V_{9A}	Offset voltage limit of battery at X=0,3, V_O = 3, 5V, T_A=24°C	3.1 to 3.5V
$\Delta V_{9A}/\Delta T_A$	Temperature coefficient of offset voltage	−10 mV/°C

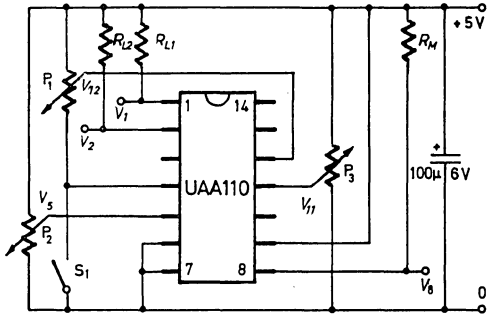


Fig. 4 — Measurement circuit for UAA110 ...

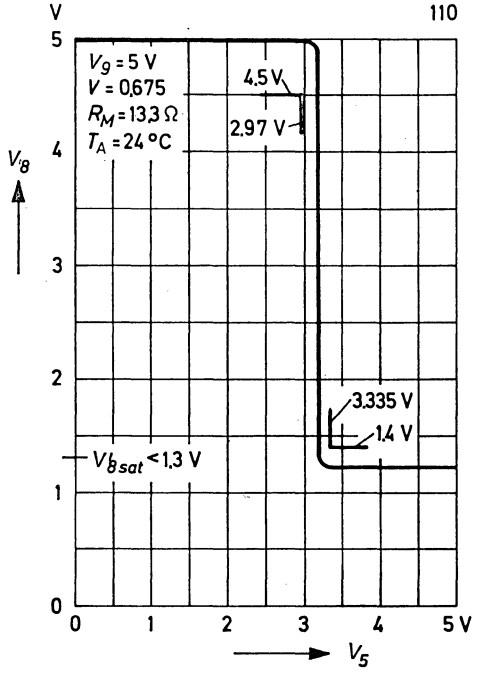


Fig. 5 — Transfer characteristic of the exposure-time forming circuit

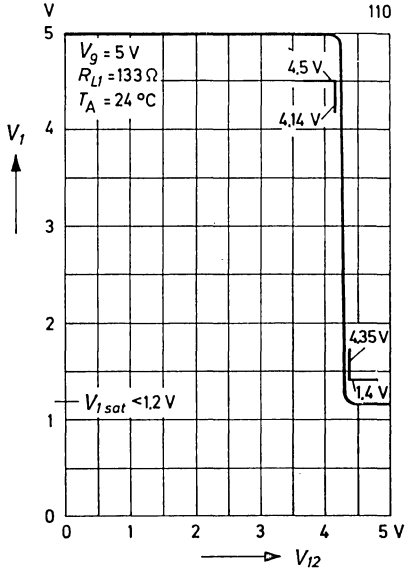


Fig. 6 — Transfer characteristic of the over-exposure indicator

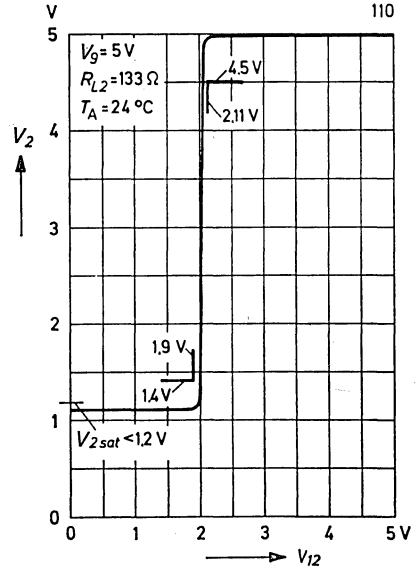


Fig. 7 — Transfer characteristic of the tripod indicator

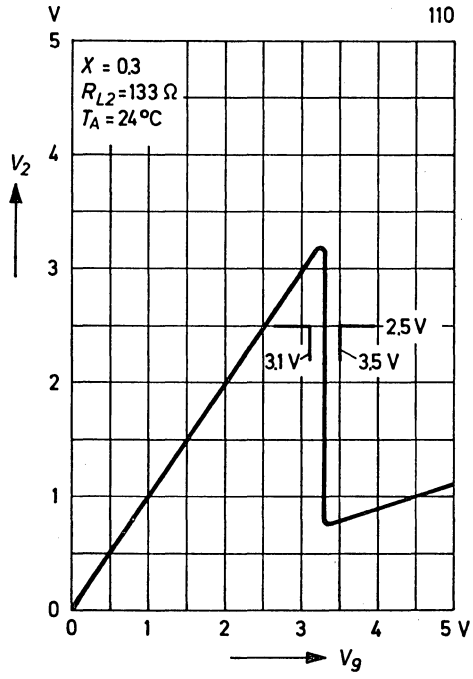


Fig. 8 — Transfer characteristic of the operating (triggering, firing voltage)

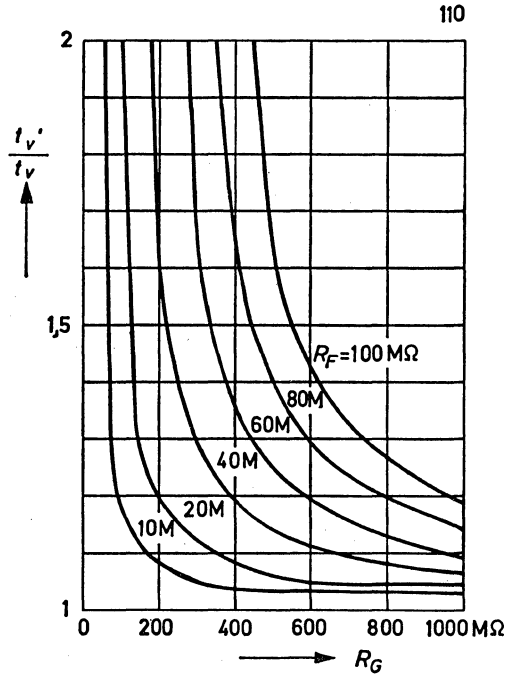
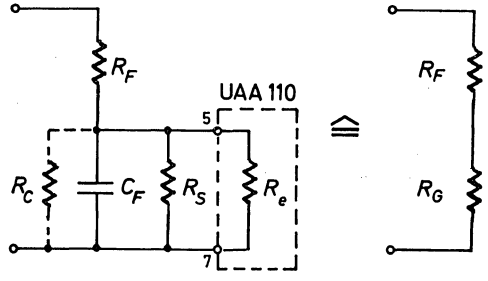


Fig. 9 — Influence of the shunt resistance on the exposure time



$$\text{Es ist } R_G = \frac{R_C \cdot R_S \cdot R_e}{R_C \cdot R_S + R_S \cdot R_e + R_C \cdot R_e}$$

Fig. 10 — Equivalent circuit for the shunt resistance R_G

ITT SEMICONDUCTORS

QUARTZ WATCH & CLOCK INTEGRATED CIRCUITS

This family of monolithic integrated circuits has been specially designed for use as frequency dividers in Quartz Crystal controlled wrist watches and clocks. The devices consist of an oscillator, frequency divider chain, pulse shaper and output stage. An external resistor is used for current consumption programming. The output stages have been designed to suit the majority of available movements. These devices are available in several different circuit variations. Please contact factory for special requirements.

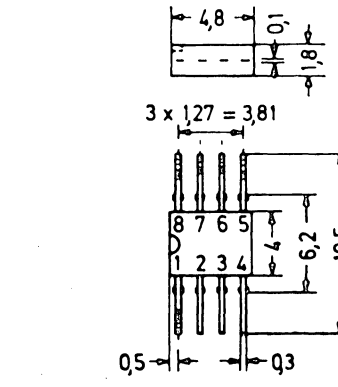
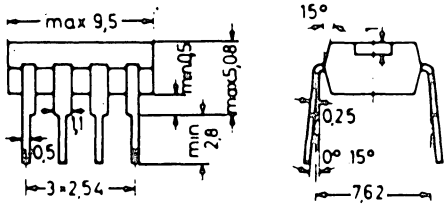


Fig. 1 — Dimensions in mm



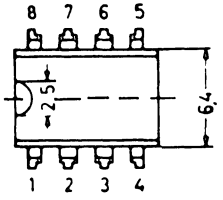


Fig. 2 — Dimensions in mm

MAXIMUM RATINGS

V_B	Supply Voltage	3V
T_A	Operating Temperature Range	−10 to +60°C
T_S	Storage Temperature Range	−30 to +125°C

TYPE	220C	220D	220H	220M	220P	220S
Characteristics	Note 1	Note 1	Note 1	Note 1	Note 2	Note 2
Stages	16	16	15	16	16	15
Current Consumption (I_B)	8μA	8μA	8μA	8μA	20μA	20μA
Output Frequency (fo)	0.5Hz	0.5Hz	1Hz	0.5Hz	0.5Hz	1Hz
Output Pulse Form	Push-Pull	Push-Pull	Unipolar	Bi-direc-tional	2 Phase Unipolar	Unipolar
Output Pulse time (To)	16mS	8mS	8mS	12mS	32mS	32mS
Output Saturation Voltage V	(RL=2.2KΩ) 0.25V	(RL=2.2KΩ) 0.25V	(RL=1.2KΩ) O.1V	(RL=2.2KΩ) 0.25V	(RL=1KΩ) 0.25V	(RL=200Ω) 1.2V

RECOMMENDED OPERATING CONDITIONS

			Note 3			
Supply Voltage V_B	1-2V	1-2V	1-2V	1-2V	1-2V	1-2V
Programming Resistor R_P	2.5MΩ	2MΩ	2.4MΩ	2.2MΩ	470KΩ	470KΩ
Quartz Series Resonance Frequency f_Q	32768Hz	32768Hz	32768Hz	32768Hz	32768Hz	32768Hz
Quartz Series Resistance R_S	<30KΩ	<30KΩ	<30KΩ	<30KΩ	<30KΩ	<30KΩ
Trimmer Capacitance C_T	10-50pf	10-50pf	10-50pf	10-50pf	8-56pf	10-50pf
Output Load Resistance R_L	>2KΩ	>2KΩ	>1.2KΩ	>2KΩ	>1KΩ	>200Ω
Package	Fig. 1	Fig. 1	Fig. 1	Fig. 1	Fig. 2	Fig. 2
Application	Watch Fig. 3	Watch Fig. 3	Watch Fig. 4	Watch Fig. 5	Clock Fig. 6	Clock Fig. 7

NOTES:

1. V_B=1.35V, Rp=2.4MΩ, T_A=25°C, f_Q=32,768KHz
2. V_B=1.5V, Rp=470KΩ, T_A=25°C, f_Q=32,768KHz
3. Reset with switching Pin 1 to negative. Fig. 4.

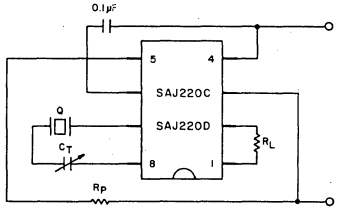


Fig. 3

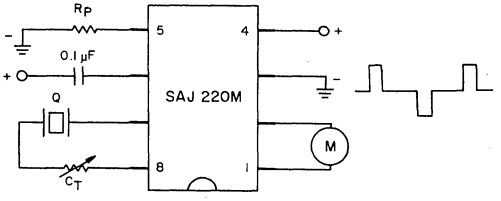


Fig. 5

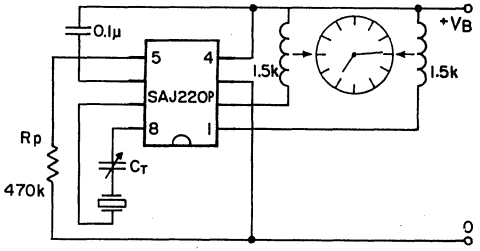


Fig. 4

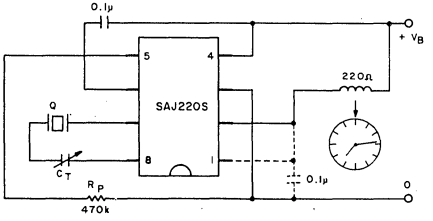


Fig. 6

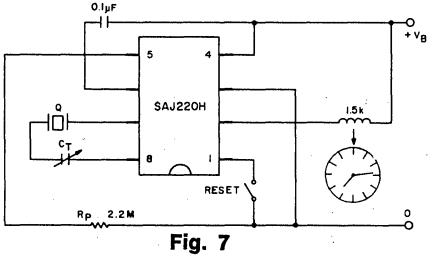


Fig. 7

1.1V STABILIZING CIRCUIT

Monolithic integrated circuit, e.g. for the voltage-stabilized drive of clocks and for the stabilization of the operating point in transistor circuits. The circuit comprises the operating transistor T1 (see fig. 2) and a control circuit for the stabilization of the output voltage $V_{3/4}$ to 1.1V.

Normally the TAA780 is delivered with vertical leads (Fig. 1a, add suffix "A" to the type No.). Upon special request, it is also available with horizontal leads (Fig. 1b, add suffix "B" to the type No.).

All characteristics and maximum ratings indicated below refer to the test circuit (Fig. 2) shown on page 30. The figure 0 in the index of some characteristics means that in this case all other terminals are open.

The following definitions apply:

$$S_{V3/4} = \frac{\Delta V_{2/4} \cdot V_{3/4}}{\Delta V_{3/4} \cdot V_{2/4}} \quad \text{and} \quad \alpha_{V3/4} = \frac{\Delta V_{3/4}}{V_{3/4} \cdot \Delta T_{amb}}$$

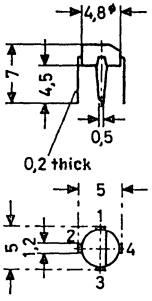


Fig. 1a — TAA780 "A" Plastic package with vertical leads. Dimensions in mm.

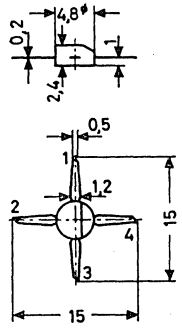
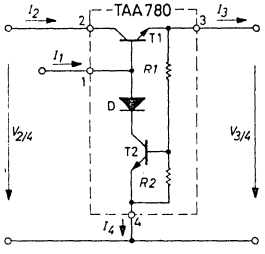


Fig. 1b — TAA780 "B" Plastic package with horizontal leads. Dimensions in mm.

MAXIMUM RATINGS

$V_{2/1/0}$	Collector base voltage	3V
$V_{2/3R}$	Collector emitter voltage at $R_{1/3}=5k$ (ext. connected)	2V
$V_{3/1/0}$	Emitter base voltage	2V
$V_{4/1/0}$	Substrate base voltage	2V
I_2	Collector current	15mA
I_1	Stabilizing current	1mA
T_{amb}	Ambient temperature range	−20 to +40°C
T_s	Storage temperature range	−20 to +125°C



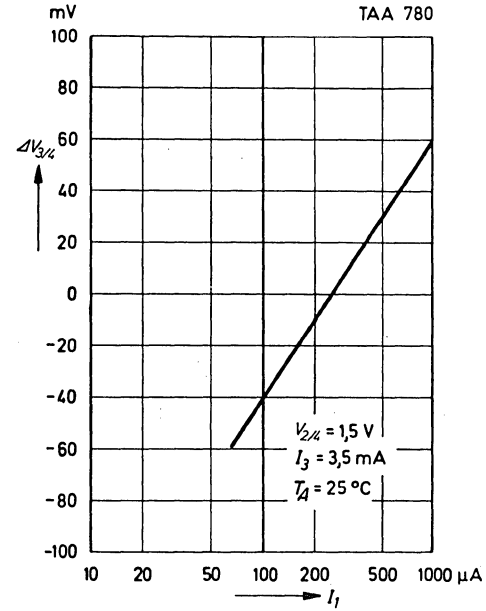
T1: Operating transistor
T2: Regulation transistor
D: Blocking diode
R1, *R2*: Voltage divider

Fig. 2 — Circuit diagram and test circuit for characteristics and maximum ratings

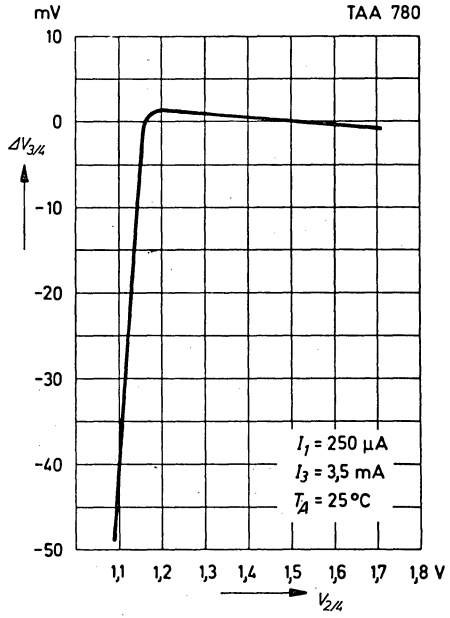
TAA780
1.1V STABILIZING CIRCUIT

CHARACTERISTICS at $T_{amb}=25°C$

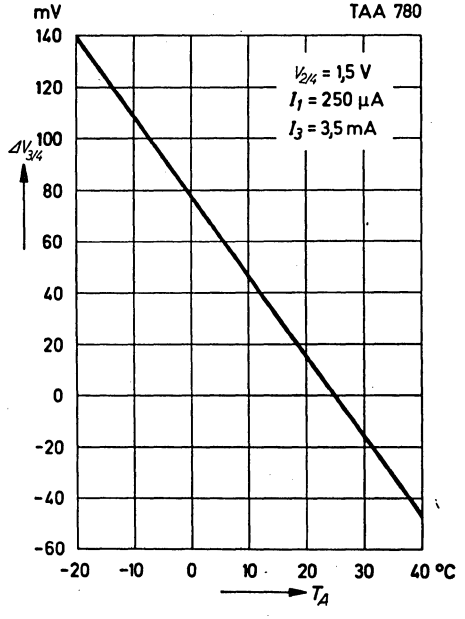
$B_{0\ 3}$	DC current gain of transistor T_1 at $V_{2/3}=1.5V$, $I_2=0.3mA$, $I_4=0$ ..... 250(>120)
$V_{2/3sat}$	Collector saturation voltage at transistor T1 at $I_2=3.5mA$, $I_1=35\mu A$, $I_4=0$ ..... 0.1(<0.12)
$V_{1/3sat}$	Base saturation voltage of transistor T1 at $I_2=3.5mA$, $I_1=35\mu A$, $I_4=0$ 0.7V
R1+R2	Total resistance of voltage divider ..... 15(>10)kΩ
$V_{3/4}$	Stabilized voltage at $V_{2/4}=1.5V$, $I_1=250\mu A$, $I_3=3.5mA$ ..... 1.1±0.06
$S_{V3/4}$	Voltage stabilization coefficient at $V_{2/4}=1.3$ to $1.7V$, $I_1=250\mu A$, $I_3=3.5mA$ ..... 1.1±0.06V
$a_{V3/4}$	Temperature coefficient of the stabilized voltage at $V_{2/4}=1.5V$, $I_1=250\mu A$, $I_3=3.5mA$ ..... -2.8×10^{-3} 1/°C
h_{fe}	Small signal current gain of transistor T1 at $V_{2/3}=1.5V$, $I_2=0.3mA$, $I_4=0$ 250



Variation of output voltage $V_{3/4}$ versus current I_1 referred to $I_1=250\mu A$, $V_{3/4}=1.1V$



Variation of output voltage $V_{3/4}$, versus input voltage $V_{2/4}$, referred to $V_{2/4}=1.5V$, $V_{3/4}=1.1V$



Variation of output voltage $V_{3/4}$ versus ambient temperature referred to $T_{amb}=25°C$, $V_{3/4}=1.1V$

WRIST-WATCH BALANCE WHEEL DRIVERS

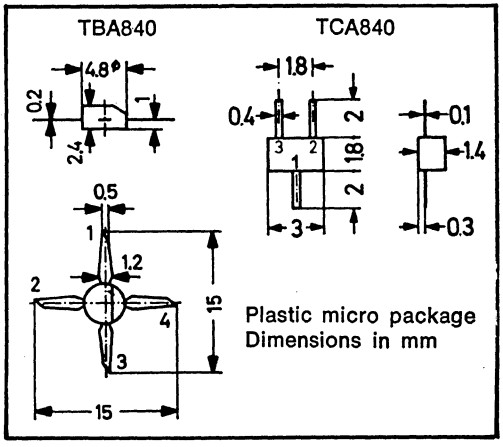
The TBA840 and TCA840 are monolithic integrated circuits for driving wrist watches with single coil balance systems. Besides the driving-coils, the TBA840 and TCA840 require only one external capacitor and allow for extremely space-saving circuitry inside an electronic wrist watch. Self-starting is guaranteed for oscillation systems with sufficient induced voltage. The mechanical oscillation amplitude is stabilized against external influences. The amplitude variation within the specified temperature range is of a few rotation degrees only. The circuitry may be operated from conventional mercury oxide or silver oxide batteries. The internal current consumption is small. The TCA840A (geen) is recommended for use with miniature watches with lightweight balance systems whereas the TCA840B (red) is for use with tuning-fork or heavier systems. The TBA840 has a somewhat larger package and may also be used in above applications.

MAXIMUM RATINGS

V_B	Supply voltage	3V
I_1 & I_3	Currents I_1 TBA840, I_3TCA840	1mA
T_A	Ambient temperature range	−10 to +60°C

RECOMMENDED OPERATING CONDITIONS

V_B	Nominal Supply Voltage	1.35 or 1.5V
f_D	Frequency of driving pulses	2.5 to 12Hz
C	Capacitor	0.5 to 4μF
$t_{i/T}$	Duty cycle (fig. 3)	0.03 to 0.1
R_L	Coil resistance	1.5 to 3.5KΩ



Packages: Fig. 1

MEASURING CONDITIONS FOR CHARACTERISTICS

The characteristics are measured in the test circuit of Fig. 4. The actual signal conditions within a watch were simulated using a function generator with signals as shown in Fig. 5.

V_B	Supply voltage	1.5V
R_L	Load resistance	2.5KΩ
V_{GS}	Signal voltage (fig. 5)	0.9V
f_D	Frequency of drive pulse	6Hz
C	Capacitor	1μF

CHARACTERISTICS at $T_A = 25°C$. See measuring conditions.

I_{tot}	Current consumption total	8.5μA
$\frac{I_{drive}}{I_{tot}}$	Ratio of driving current for the oscillator to total current consumption	0.9
t_i	Drive pulse duration	7.8 mS
$t_{i/T}$	Drive pulse duty cycle	0.05
V_{sat}	Saturation voltage V_2, TCA840, V_3, TBA840	0.3V
R_i	Output series resistance (See fig. 2)	1KΩ
$I_{pk}=\frac{V_B-V_S}{R_L+R_i}$	Peak Value of operating current I_2, TCA840, I_3, TBA840	
$V_{S1}=V_{S2}$	Switching thresholds	0.5V

Circuit Design Information

The optimum position for an output pulse is when the switch-on threshold V_{S1} and the switch-off threshold V_{S2} are equal. This is dependent upon the capacitor, C, chosen, the mechanical clockwork, induced coil voltage $V_{in\ s}$, driving frequency, f_d, duty cycle t_i/T and the coil resistance R_L.

With two-magnet systems, the output drive pulse must appear only once per total oscillation because the polarity of the induced voltage changes with each change in oscillation direction. Care must be taken when designing the external components with this system.

The switching threshold is changed together with the induced coil voltage. For optimum pulse conditions, i.e. $V_{S1} = V_{S2}$, the switching threshold is only dependent on the maximum induced voltage.

The self-starting properties of the system are dependent on the operation of the oscillator and coil. The start-up time is limited by the movement of the balance wheel, magnets, value of the induced voltage and the coil resistance.

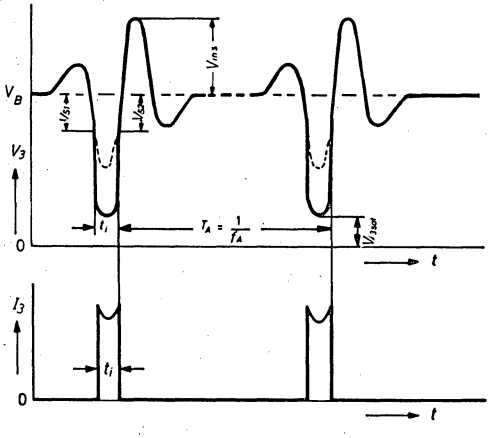
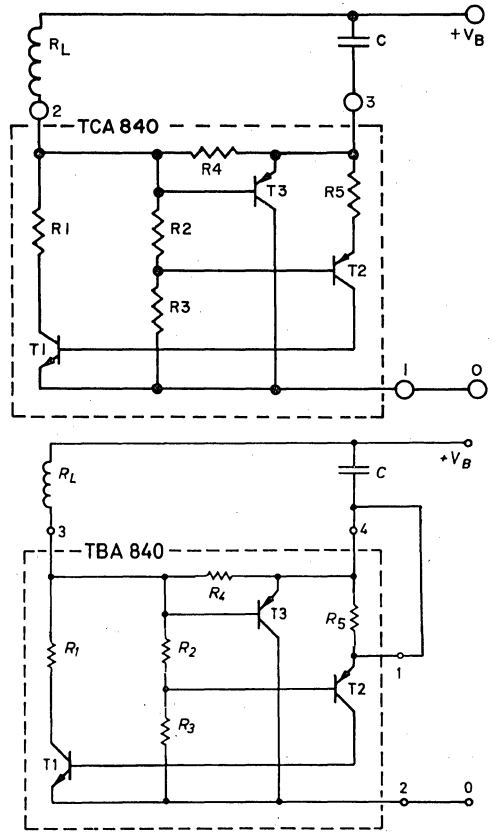


Fig. 3—Operating waveforms for V_{coil} and I_{coil} with a 3-magnet balance system. (V_C & I_C)



Circuit Diagram

Fig. 2—Internal circuit diagrams TBA840, TCA840

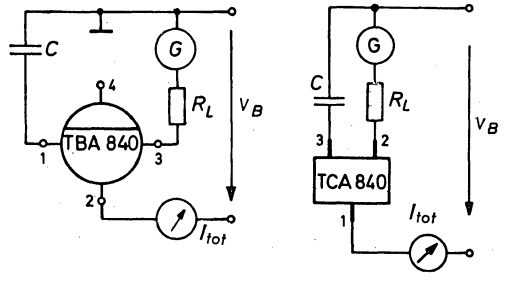


Fig. 4—Test Circuits

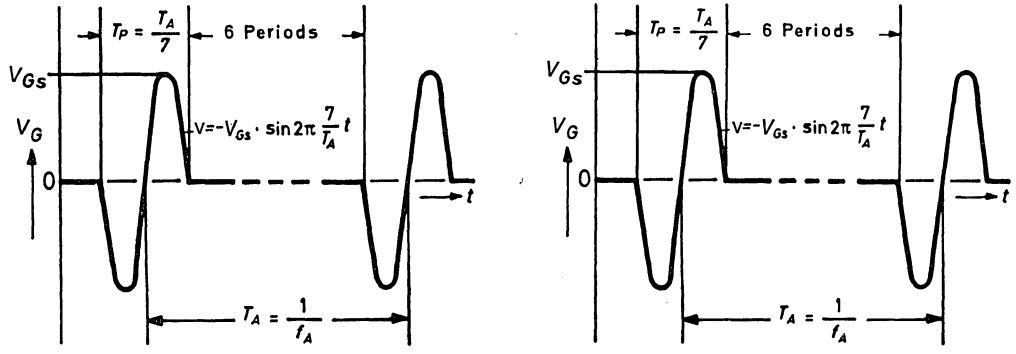


Fig. 5—Signal induced Waveforms

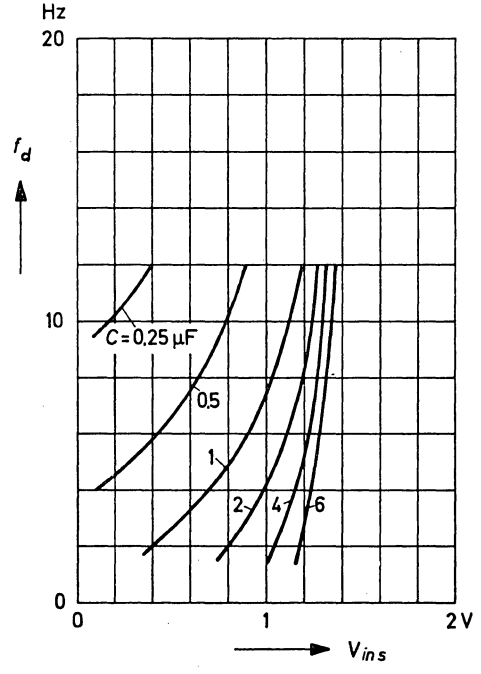


Fig. 6—Calculation of capacitor Value, C. See measurement conditions.

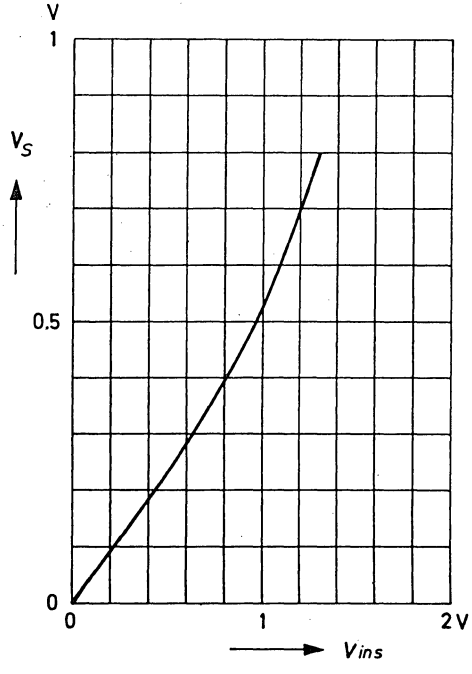


Fig. 7—Switching thresholds versus induced voltage.

POWER OSCILLATOR

Monolithic integrated circuit in bipolar technique. Particularly suited as electronic pulse generator for direction blinker and emergency blinker in cars with 12 V DC supply. Also suited for other applications, e. g. for interval wind-screen wipers.

The TAA775G is an oscillator, the frequency of which is determined by an external RC network and which supplies rectangular output pulses. The output terminal 10 is connected to the collector of the output transistor operating in common emitter configuration. An integrated diode between the collector of the output transistor and the supply voltage terminal 1 allows for operation with inductive loads.

As can be seen from the terminal diagram Fig. 1, the TAA775G has two oscillator input terminals 5 and 6, for the connection of the frequency-determining RC network. By applying a suitable control voltage to the control input (terminal 7) the following operating modes are possible (see Fig. 5):

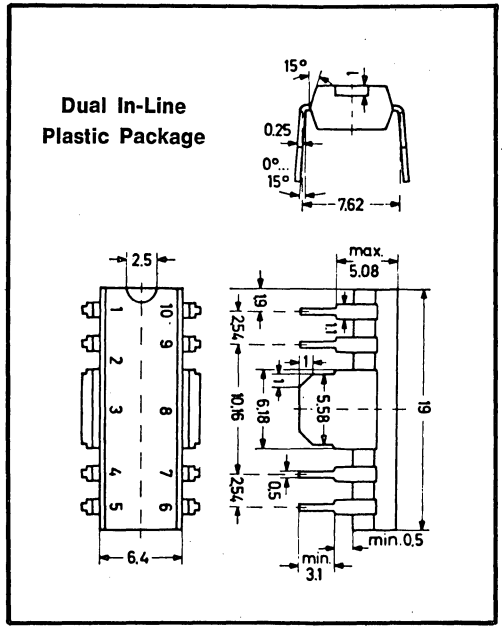
a) Operation at nominal frequency f_0
b) Operation at increased frequency f'_0
c) Oscillator not oscillating

When a control voltage for operating mode a) or b) is applied, oscillation starts in the on-state. Since the control voltage is effective only during the off-state, blocking of the oscillator in the on-state is possible only at the end of the normal on-state.

Maximum Ratings (All voltages are referred to terminals 3 and 8.)

Terminals 3 and 8 grounded

V_1	Supply Voltage	15V
V_7	Control voltage	$<V_1$
V_{10}	External Voltage on terminal 10	$<V_1$
I_{10}	Output Current	150mA
T_{amb}	Ambient temperature range	-25 to $+85°C$



Static Characteristics @ $V_1=12V$:$V_3=V_8=0V$, $T_{amb}=25°C$ (see Fig. 3)

I_1	Average current consumption	8mA
$-I_{5R}$	Leakage current of the oscillator input at $V_5=0V$	$<1\mu A$
I_5	Required oscillator input current for turning on the oscillator output	$>10\mu A$
V_{10sat}	Output saturation voltage in the on-state at $I_{10}=110mA$	$<1V$
I_{10R}	Output leakage current in the off-state at $V_{10}=V_1$ and $V_5=0V$ or $V_7=V_1$	$<1\mu A$

Fig. 3. Test Circuit for Static Characteristics

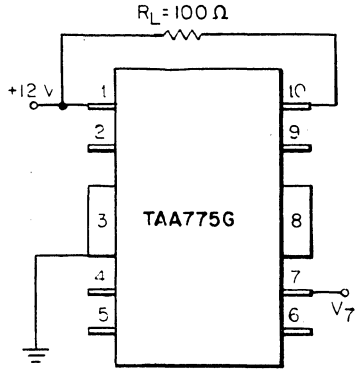
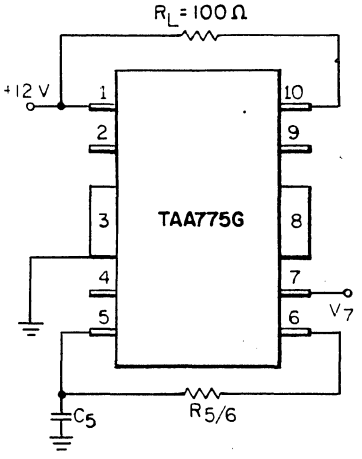
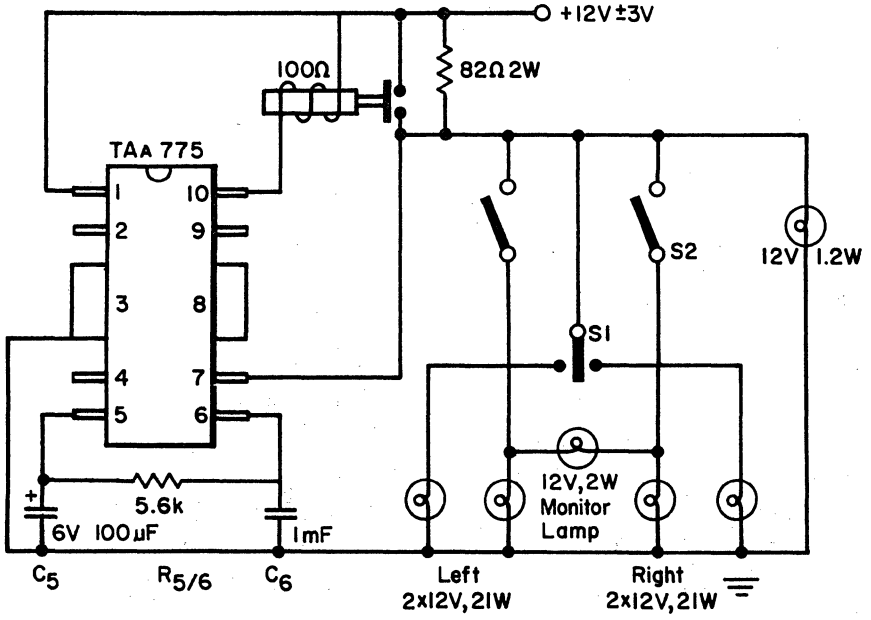


Fig. 4. Test Circuit for Dynamic Characteristics



Circuit Diagram of a combined car flasher-emergency system with TAA775G



Dynamic Characteristics @V_1=12V, V_3=V_8=0V, T_{amb}=25°C (see Fig. 4)

$R_{5/6}$ Frequency-determining resistor ..... 1 to 120kΩ

C_5 Frequency-determining capacitor ..... optional, but the leakage current of the capacitor must be taken into consideration

Oscillator frequency (see Fig. 5)

at V_7=0 to 0.35V ..... $f_o = \frac{800}{R_{5/6} \times C_5}$ Hz

$R_{5/6}$ in kΩ
C_5 in μF

at V_7=0.45 to 5V ..... $f'_o = 2.2 f_o$

at V_7=8V to V_4 ..... f''_o=0; Output transistor blocked

on/off ratio (see Fig. 5)

at V_7=0 to 0.35V ..... t_{on}/t_{off}=0.8

at V_7=0.45 to 5V ..... t'_{on}/t'_{off}=1.1

Application of the TAA775G as direction and emergency blinker (See Circuit Diagram)

In conjunction with a frequency-determining RC network (e. g. $R_{5/6}$ = 5.6 kΩ, C_5 = 100μF/6 V) and a relay (coil resistance min. 100Ω) the TAA775G replaces a conventional hot wire interval switch and a current monitoring relay. The previous arrangement of the terminals on the blinker relay package (plus and minus pole of the battery and connection to steering-wheel changeover switch) can be retained. In the case of direction, blinking, the bulbs are monitored: the breakdown of a bulb causes a greatly increased blink frequency. The capacitor C_6 prevents battery voltage transients affecting the operation of the TAA775G.

Characteristics of a blinker circuit using TAA-775G at V_1=12V, T_{amb}=25°C, as in circuit Fig.6

Operation starts with a bright interval

t Duration of the first bright interval ..... <1sec

f_o Nom. frequency in normal operating with two 21 W bulbs ..... 85min^{-1}

f_o Nom. frequency in emergency operation with four 21 W bulbs ..... 85min^{-1}

υ Ratio of on-time to total period at nom. frequency 45%

$\pm\Delta f_o/f_o$ Dependence of operating frequency on the supply voltage in the range of 9 to 15V ..... <2%

Control of the lamps:

Defect in one of the two direction indicating lamps causes an increase of the blink frequency by the factor 2.2

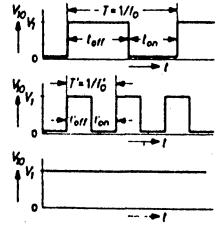
υ' Ratio of on-time to total period in the case of increased frequency 52%

Other applications of the TAA775G

The frequency and the on/off ratio of the output voltage can be varied within a wide range by variation of the time-determining RC network. For the charging resistor R_a and the discharging resistor R_e the following conditions must be met:

1 kΩ < R_a < 120 kΩ 1 kΩ < R_e < 120 kΩ

The TAA775G can be used for frequencies up to 20 kHz. The approximate equations given below are, however, only valid for frequencies up to 4 kHz. Fig. 7 gives the output voltage wave form with load resistor connected.



V_7 = 0...0.35 V

V_7 = 0.45...5 V

V_7 = 8 V...V_1

Fig. 5: Operation of the control input 7 (steady state)

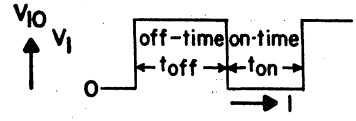


Fig. 7: Behaviour of the output voltage as a function of time

For the circuit in Fig. 8 these equations are valid:

$T = 1/f_0 = \frac{RXC}{800}$ sec

R in kΩ
C in μF

$t_{on} = 0.45\ T$
$t_{off} = 0.55\ T$

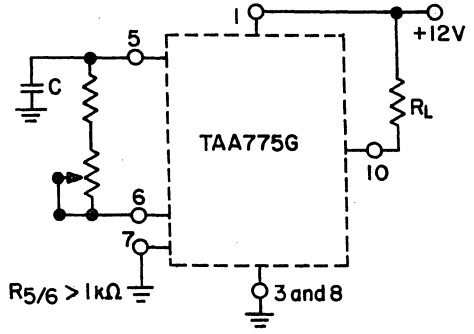


Fig. 8: TAA775G as pulse generator with adjustable frequency and constant on/off ratio. Charging and discharging of the time-determining capacitor through the same resistor.

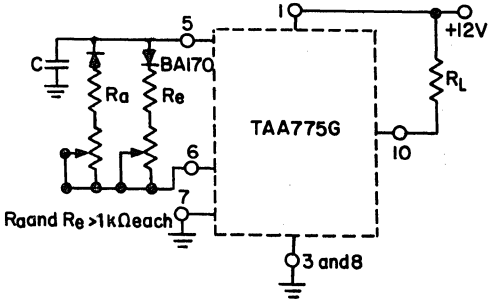


Fig. 9: TAA775G as pulse generator with adjustable frequency and constant on/off ratio. Charging and discharging of the time-determining capacitor is effected through separate resistors.

For the circuit in Fig. 9 these equations are valid:

$t_{on} = 0.7XCXR_e$ msec
$t_{off} = CXR_a$ msec

R in kΩ
C in μF

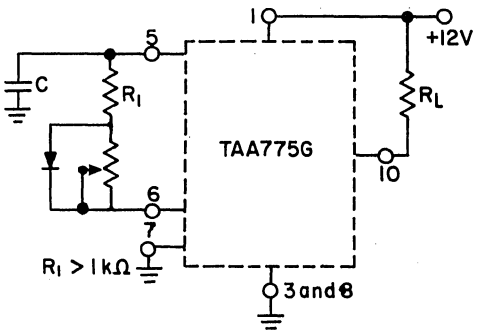


Fig. 10: TAA775G as pulse generator with adjustable on-time

For the circuit in Fig. 10 these equations are valid:

$t_{on} = 0.6XCX(R_1 + R_2)$ msec
$t_{off} = CXR_1$ msec

R in kΩ
C in μF

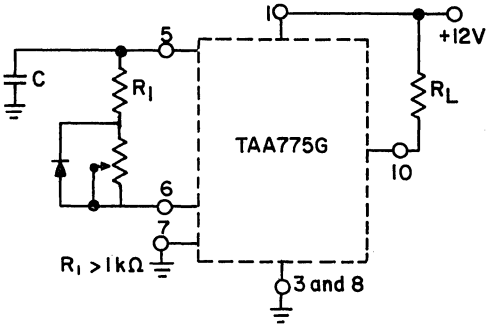


Fig. 11: TAA775G as pulse generator with adjustable off-time

For the circuit in Fig. 11 these equations are valid:

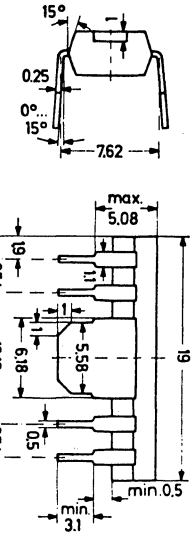
$t_{on} = 0.7XCXR_1$ msec
$t_{off} = 0.75XCX(R_1 + R_2)$ msec

R in kΩ
C in μF

TACHOMETER INTEGRATED CIRCUIT

The SAK115 is a monolithic integrated circuit designed for use as a pulse shaper in tachometer/rev-counter applications. By choosing suitable external components, the SAK115 can be used with 2 to 8 cylinder engines. It is designed for a nominal 12V supply. The basis of the SAK115 is a monostable multivibrator which converts the input signal (derived, for example, from the contact breaker) into square pulses of constant voltage and duration. Using an 8 mA moving-coil instrument, it is possible to design a simple frequency meter. The circuit features good noise immunity as it can only be triggered by input pulses exceeding 8 volts. An internal diode parallel to input terminals 1 and 3 prevents triggering from negative pulses. The circuit is so designed that with the use of a suitable instrument, the readings will be practically independent of temperature. The push-pull output allows use of instruments with meter coils of high inductance even at high frequencies. Fig. 2 shows the circuit of a tachometer/rev-counter with a full scale deflection at 6000 rpm (2 input pulses with each crankshaft revolution).

Dual In-Line Plastic Package



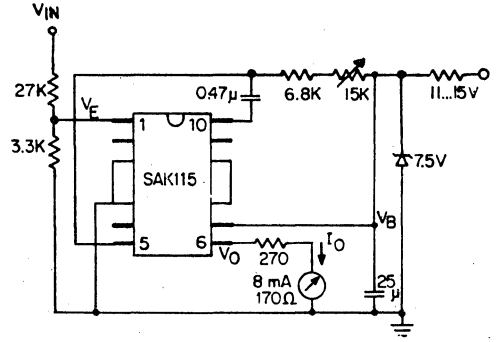


Fig. 2: Circuit diagram or a rev-counter for a four-cylinder four-stroke engine. Full-scale deflection at 6,000 RPM. Nominal voltage of car battery 12 V.

Maximum Ratings

V_B, $V_{7/3}$	Supply voltage	9V
I_6	Currents	−20mA
I_1	average value	2mA
I_1	at pulse duration<0.5ms	20mA
I_5	at pulse duration<0.5ms	75mA
I_{10}	at pulse duration<0.5ms	−75mA
T_{amb}	Ambient temperature range	−40 to +85°C

Recommended Operating Data

$V_{7/3}$	Supply voltage	7.5 to 8V
f_i	Frequency of input pulses	<10kHz
t_o/T	Pulse duty factor of output voltage	<0.85
$R_{5/7}$	Timing resistor	3 to 20kΩ
t_i	Input pulse width	>1.0µsec

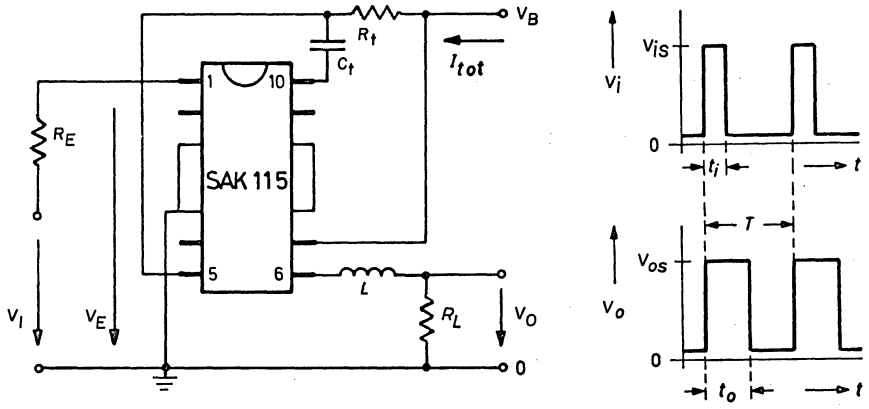


Fig. 3: Measuring circuit. The duration of the input pulses must always be shorter than the duration of the output pulses.

Measuring Conditions for Characteristics

(See measuring circuit Fig. 3)

$V_{7/3}$	Supply voltage(±1%)	8V
$R_{5/7}$	Timing resistor (±0.1%)	10kΩ
$C_{5/10}$	Timing capacitor (±0.1%)	0.47μF
R	Load resistance (±0.5%)	440
L	Load inductance (±5%)	80mH
R_1	Series resistance at input (±1%)	10kΩ
V_{is}	Voltage amplitude of input pulses (±2%)	10V
t_i	Duration of input pulses (±5%)	0.5ms
f_i	Frequency of input pulses (±0.1%)	250Hz

Characteristics at T_{amb}=25°C

(See preceeding measuring conditions.)

I_{tot}	Supply current at V_i=0	12 to 22mA
$V_{1/3}$	Input voltage drop	6.5 to 8V
t_o	Duration of output pulses	2.7 to 3.1ms
V_{os}	Voltage amplitude of output pulses	5 to 5.8V
V_o	Output voltage average value	3.3 to 4.5V
$\pm\frac{\Delta V_o}{V}$	Change of output voltage for a supply voltage change of supply volt. of $\pm V_{7/3}$=0.3V	<2%
$\propto V_o$	Temperature coefficient of output voltage	$<2\times10^{-3}$ 1/°C
V_{ores}	Residual output voltage	<30mV

At input frequencies in the range of f_i = 25 to 250Hz:

Dependence of output voltage on the frequency

$$V_{o\,lin} = \frac{V_{o\,max} - V_{o\,res}}{f_{i\,max}} \cdot f_i + V_{o\,res}$$

Deflection linearity error $\left|\frac{V_o - V_{olin}}{V_{omax}}\right| < 0.3\%$

Definitions:

V_o = Actual value of output voltage (average value)

V_{olin} = nominal value of output voltage

V_{omax} = final value of output voltage at $f_i = f_{i\,max}$=250 Hz (full scale deflection)

The period of the input pulse must be smaller than the period of the output pulse.

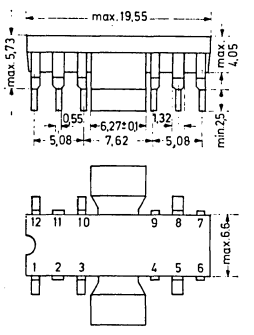
ITT SEMICONDUCTORS

SPEEDOMETER INTEGRATED CIRCUIT

The SAY115 is a monolithic integrated circuit designed for use in electronic speedometers and odometers in automobiles and other vehicles. As shown in Fig. 1, it consists of a Schmitt Trigger, a monostable multivibrator, a current source for supplying a moving-coil instrument, an analog output, a binary 5 or 6 stage frequency divider with a power output stage for direct drive of a two-coil stepping motor. This is used for mileage or distance indication. The analog output allows a warning signal to be set off when the speed falls below or exceeds pre-set limits.

SAY115X—5 stage (÷ 32)

SAY115Y—6 stage (÷ 64)



Dual In-Line Plastic Package

Maximum Ratings

$V_{9/13}$	Supply voltage, continuous	16V
$V_{9/13}$	Supply voltage, pulsed <5 ms	20V
V_1	Input voltage	−0.5 to +20V
I_3, I_5	Output current at the motor terminals	300mA
I_6	Output current for moving coil instrument	−30mA
T_{amb}	Ambient temperature range	−40 to +85°C
T_S	Storage temperature range	−40 to +125°C

RECOMMENDED OPERATION DATA

$V_{9/13}$	Supply voltage	11 to 16V
f_i	Input frequency	<10kHz
$R_{2/11}$	Timing resistor for monostable	15 to 100kΩ
$R_{7/8}$	Potentiometer for current source	>100Ω
t_p	Duty Cycle of monostable	<0.9
T_{period}		
C_S	Filtering network	33Ω
R_S		>25uF

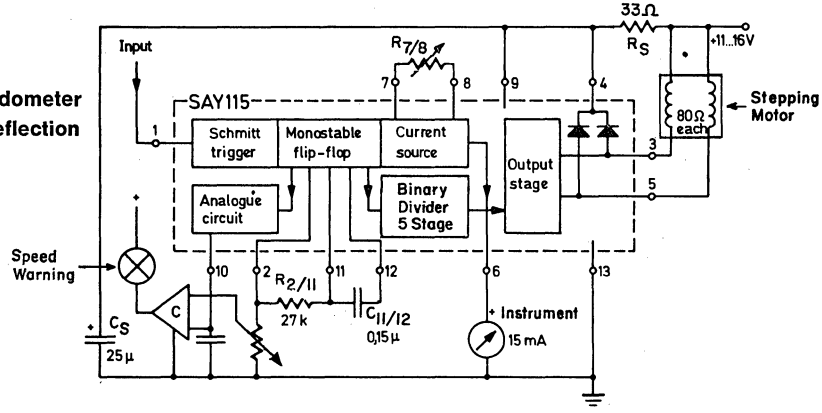


Fig. 1—
Diagram of a Speedometer Circuit with full deflection at F_i=300 Hz

SAY115
SPEEDOMETER INTEGRATED CIRCUIT

CHARACTERISTICS $T_A = 25°$ C

$V_{9/13}$	Supply voltage	11 to 16V
I_9	Quiescent Current (without stepping motor)	16mA
	Input trigger thresholds	
V_{IL}	"low"	2.5V
V_{IH}	"high"	3.5V
	Input Current	
I_1	at $V_I < V_{IL}$	−100uA
I_1	AT $V_I > V_{IH}$	≈0

NOTE—The monostable will trigger on the trailing edge of the input signal if V_{IL} is exceeded.

$V_{2/13}$	Reference voltage	6.5V
$V_{6/13}$	Current source voltage range	0 to 5V
I_6	Instrument current, peak value	$\frac{2.3V}{R_{7/8}}$
t_{p6}	Output pulse period (Pin 6)	$0.67 \times R_{2/11} \times C_{11/12}$
	Analog output voltage D.C.	
V_{10}	$f = 0$	6.5V
V_{10}	$f = f_{max}$, $\frac{t_p}{T_{period}} = 0.9$	2.1V
$R_{out\ 10}$	Output resistance of analog output	10KΩ
fi/fo	Divider ratio of binary divider Note (1)	32 or 64
V_{3sat},	Saturation voltage of motor	
V_{5sat}	outputs at $I_3 = I_5 = 200mA$	1.2V

NOTE (1)—Ordering Instructions:
Order SAY115X for ÷ 32 (5 stage).
Order SAY115Y for ÷ 64 (6 stage).

Application Information

The speedometer SAY115 is usually driven from the gearbox (transmission) of an automobile vi, for example, a reed-relay contact, a proximity switch or an inductive sensor. The monostable is triggered by the trailing edge (negative going) of the input signal and is therefore not susceptible to contact bounce of a reed relay. This assumes that the input signal meets trigger threshold limits shown in the data. The pulse width of the monostable is set by RC components $R_{2/11}$ and $C_{11/12}$ and can be adapted to a wide input frequency range.

The current source output at Pin 6 is proportional to the input frequency and can be adjusted by a resistor or potentiometer, $R_{7/8}$. The resistors $R_{7/8}$ or $R_{2/11}$ can be chosen for calibration of the speedometer system. Due to the current source, temperature variation of the resistance of the moving-coil instruments do not affect the reading. The current source is essentially thermally neutral. Thus, temperature effects are limited to the external components $R_{2/11}$, $R_{7/8}$ and $C_{11/12}$. Therefore, virtually all temperature drift effects on the reading are eliminated when the supply voltage is turned on.

One side of the instrument is connected to ground thus simplifying mechanical construction.

If required, a filter capacitor can be connected to the analog output in order to generate a d.c. voltage as a linear function of speed. Thus by using a simple comparator, K, a warning signal can be set off when the speed exceeds or falls below a pre-set value. For convenience, a stabilized reference voltage is available at pin 2 of 6.5 volts. A potentiometer may be used and the temperature dependence of the comparator switching point is therefore, a function of the comparator, potentiometer, and the RC components ($R_{2/11}$ and $C_{11/12}$).

The binary divider divides the input frequency by 2^5 or 2^6 and drives an output stage consisting of two NPN Darlingtons. Both outputs change alternately to "high" and "low" during half periods of the output signal. Both outputs have a freewheeling diode with a common cathode output at Pin 4.

In order to protect the circuit from high voltage spikes generated in an automobile electrical system an external filter network R_S, C_S should be used as shown. The stepping motor current does not flow through the filter resistor, R_s, thus allowing sure starting of the stepping motor even under low battery voltages. The cooling pins of the package are the ground connection pins of the SAY115 and should be soldered to the PC board to allow good thermal conduction.

INTRODUCTION

ITT has a wide selection of planar transistor chips and wafers available for those who require devices in this form. Since the large number of JEDEC specifications are derived from a few chip types, many differing applications can be satisfied with a relatively small quantity of basic chip families.

SPECIFICATIONS

The accompanying DC parameters identifying each family are tested on each chip in the wafer. These are the probe specifications. As shipped from our factory, THE PROBE PARAMETERS ARE GUARANTEED TO AN AQL = 2.5%.

The design parameters such as $V_{CE(SAT)}$, t_{on}, t_{off}, C_{ob}, etc. are not probed. These characteristics can best be tested after the chip is suitably mounted; and, therefore, have little significance in chip form.

The chips will have a high yield to the specified limits. The actual yield will vary with the mechanical techniques used to assemble the device, and the type of package used.

In all cases, the lowest useable voltage and the lowest useable h_{FE} should be chosen in specifying chip parameters. This will provide the highest possible yield and the most economical design.

USE

The entire wafer is manufactured with approximately 3000 A° of gold for die attach to a suitable substrate or base. Recommended die attach temperature for all families is 450°C, maximum. 9,000 to 12,000 angstroms of aluminum are deposited on the chip for metalization purposes. ITT recommends aluminum wire for connection to the aluminum base and emitter bonding pads. Ultrasonic techniques may be used for the wire-bond operation.

PACKAGING FOR SHIPMENT

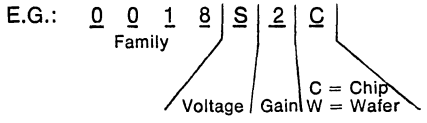
Chips will be shipped in appropriate containers, with the devices packaged to protect them from damage in shipment. Wafers will be shipped in a similar manner. Unless otherwise specified, wafers will not be scribed prior to shipment.

CROSS REFERENCE CHART

The list of JEDEC specifications, together with the respective chip specification, will provide a means of ordering the proper chip required in an application. This chart is not exhaustive, and is provided as a guide. Specific requirements may necessitate a different chip specification from available JEDEC "2N" numbers. In such cases, the accompanying list of chip parameters will provide the necessary information.

ORDERING

All chips and wafers should be ordered according to the alpha-numeric coding system referred to in the specification chart. The four-digit geometry family, together with the voltage letter and DC gain number (from the accompanying geometry parameter chart) will completely determine the specification which ITT will provide. A third letter specifies in which form, chip or wafer, the product is to be shipped.



IDENTIFICATION

All small-signal transistor dice will be identified by the appropriate four-digit family number together with the particular classification code for voltage and current gain.

By way of example:

The 2N2222 is a "0018" chip. The voltage class is "M," the current gain is "A." Therefore, when ordering a 2N2222 in chip or wafer form, the correct part would be a "0018MA" chip. This method applies to dice and to a wafer which has been tested 100%.

If a wafer is needed which does not require all the chips to be tested, then the alpha-numeric suffix will apply. For a 2N2222 device, in wafer form, sample probe-tested only, the proper part number will be a "0018S1."

TRANSISTOR WAFER INSPECTION CRITERIA

MECHANICAL INSPECTION

Measure overall thickness of one (1) wafer if run contains five (5) or less wafers. Measure two (2) wafers if run size is greater than six (6) wafers. Reject the run if any of the measured wafers are not per limits specified in Table I.

Q.C. will 100% measure overall thickness of each wafer in a rejected run.

VISUAL INSPECTION

Inspect ten (10) randomly selected devices on each wafer with no more than three (3) die in any one quadrent using 100X magnification.

TABLE I

UNAIDED EYE INSPECTION

1. Backside gold — the backside gold must cover 90% of the wafer surface. The gold must exhibit a gold, orange, or yellow cast. The gold must show no evidence of peeling or blistering.

Microscope Inspection (100X) — Combined 1.0% AQL

1. Aluminum bridging—the base metal, emitter metal, and EQR ring metal may not be connected or bridged by unetched or smeared aluminum.

2. Aluminum adherance—the aluminum may show no evidence of peeling, blistering, or flaking.

3. Aluminum color — the aluminum may not be dark brown or black.

4. Aluminum reduction — aluminum fingers must be continuous along 75% of the oxide cutout length nearest the bond pad on metal over oxide devices. Aluminum fingers may not be reduced more than 50% of the oxide cutout width on metal over oxide devices, nor more than 25% in width at an oxide step-down point. Bond pads must not be reduced more than 25% of their intended area. EQR rings may not be discontinuous at more than one place.

5. Oxide holes—silicon may not be exposed within .0002 in. of any junction.

6. Mask misalignment — the outline of one oxide mask definition may not cross over the outline of another mask definition. Aluminum mask outlines must cover more than 50% of the intended oxide cutouts.

TRANSISTOR DIE INSPECTION CRITERIA

Inspect per Table II using 100X to combined 2.5% AQL.

TABLE II

1. Broken die — broken corners, edges, or shell chips may not extend closer than .001" to a junction or bond pad.

2. Cracks—cracks which are not terminated at each end at the periphery of the die may not extend toward a junction or bond pad.

NPN SILICON AUDIO TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic		Unit
Collector-Emitter Voltage	60	Vdc
Collector-Base Voltage	60	Vdc
Emitter-Base Voltage	4.0	Vdc
Collector Current - Continuous	500	MAdc
Total Device Dissipation		
@ T_A = 25°C	500	mW
Derate above 25°C	4.54	mW/°C
Total Device Dissipation		
@ T_C = 25°C	800	mW
Derate above 25°C	7.27	mW/°C
Operating and Storage Junction		
Temperature Range	-55 to +135	°C
Thermal Resistance, Junction		
to Case	0.137	°C/mW
Thermal Resistance, Junction		
to Ambient	0.220	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	60	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 60 Vdc, I_E = 0
h_{FE}	50	125	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	50	150	–		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
	–	90	–		I_C = 350 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	–	0.08	0.25	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	0.75	–		I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(on)}$	–	0.7	1.2	Vdc	I_C = 100 mAdc, V_{CE} = 1.0 Vdc
f_T	50	200	–	MHz	I_C = 100 mAdc, V_{CE} = 1.0 Vdc, f = 100 MHz
C_{ob}	–	6.0	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	15	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz

ITT SEMICONDUCTORS

GENERAL PURPOSE NPN
SILICON AMPLIFIER TRANSISTORS

Package: To-92

NPN SILICON GENERAL PURPOSE AMPLIFIER TRANSISTORS

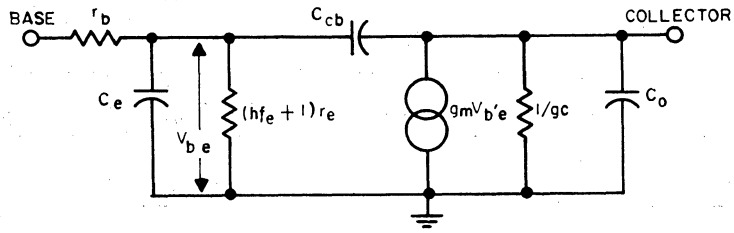
ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	–	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
f_T	50	–	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 20 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1–Simplified AC Equivalent Circuit (Common Emitter)



NPN SILICON AMPLIFIER TRANSISTORS

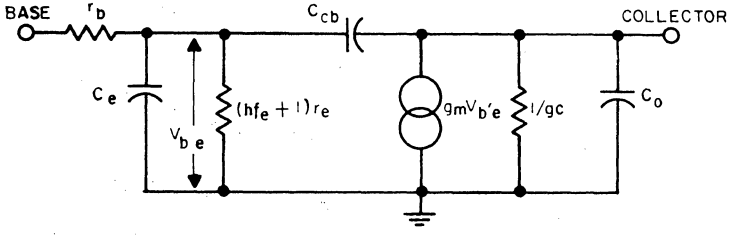
ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	–	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	125	–	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1—Simplified AC Equivalent Circuit (Common Emitter)



ITT SEMICONDUCTORS

MPS-A55
PNP SILICON AMPLIFIER TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic		Unit
Collector-Emitter Voltage	60	Vdc
Collector-Base Voltage	60	Vdc
Emitter-Base Voltage	4.0	Vdc
Collector Current - Continuous	500	mAdc
Total Device Dissipation @ T_A = 25°C	500	mW
Derate above 25°C	4.54	mW/°C
Total Device Dissipation @ T_C = 25°C	800	mW
Derate above 25°C	7.27	mW/°C
Operating and Storage Junction Temperature Range	-55 to +135	°C
Thermal Resistance, Junction to Case	0.137	°C/mW
Thermal Resistance, Junction to Ambient	0.220	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	60	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 60 Vdc, I_E = 0
h_{FE}	50	150	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	50	125	–		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
	–	80	–		I_C = 350 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	–	0.09	0.25	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	0.78	–	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(on)}$	–	0.73	1.2	Vdc	I_C = 100 mAdc, V_{CE} = 1.0 Vdc
f_T	50	100	–	MHz	I_C = 100 mAdc, V_{CE} = 1.0 Vdc, f = 100 MHz
C_{ob}	–	6.5	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	20	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz

ITT SEMICONDUCTORS

MPS-A70
GENERAL PURPOSE
PNP SILICON AMPLIFIER TRANSISTORS

Package: To-92

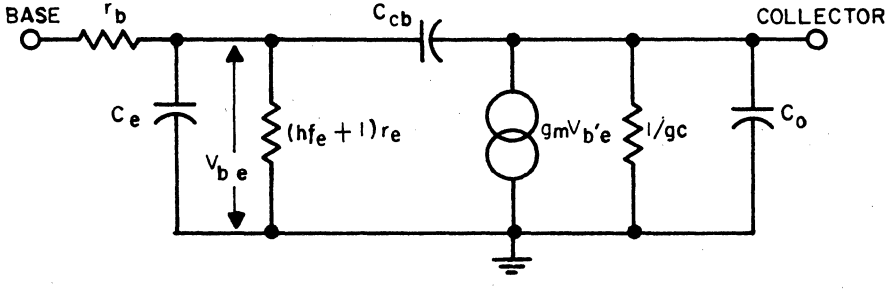
ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	–	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	125	–	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1—Simplified AC Equivalent Circuit (Common Emitter)



ITT SEMICONDUCTORS

HIGH-SPEED NPN SILICON
LOW-LEVEL SWITCHING TRANSISTORS

Package: To-92

NPN SILICON HIGH-SPEED LOW-LEVEL SWITCHING TRANSISTORS

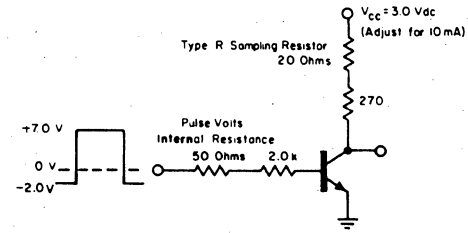


Figure 1 – Switching Time Test Circuit

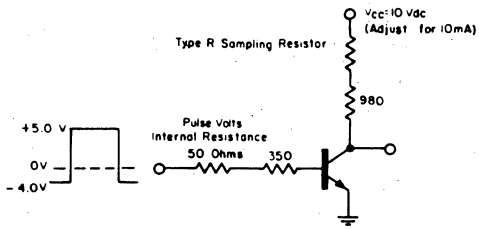


Figure 2 – Storage Time Test Circuit

ABSOLUTE MAXIMUM RATINGS

Characteristic	MPS706	MPS706A	Unit
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	20		Vdc
Collector-Base Voltage	25		Vdc
Emitter-Base Voltage	3.0	5.0	Vdc
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CER}	20	–	Vdcq	I_C = 10 mAdc, R_{BE} = 10 Ohms
I_{CBO}	–	0.5	*u*Adc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	10	*u*Adc	V_{EB} = 3.0 Vdc, I_C = 0
h_{FE}*	20	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc MPS706
	20	60		MPS706A
$V_{CE(sat)}$*	–	0.6	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$*	–	0.9	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc MPS706
	0.7	0.9		MPS706A
f_T	200	–	MHz	I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 100 MHz
C_{ob}	–	6.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
r_b	–	50	Ohms	I_E = 10 mAdc, V_{CE} = 15 Vdc, f = 300 MHz
t_{on}**	–	40	ns	Turn-On Time See Figure 1
t_{off}**	–	75	ns	Turn-Off Time See Figure 1
T_S**	–	60	ns	Charge Storage Time Constant ** See Figure 2 MPS706
	–	25		MPS706A

*Pulse Test: Pulse Width ≤ 12 ns, Duty Cycle ≤ 2.0%.
**Measured with Tektronix Type R Plug-In (50-Ohm Internal Impedance) and circuits shown.

ITT SEMICONDUCTORS

MPS834

HIGH-SPEED NPN SILICON SWITCHING TRANSISTOR

Package: To-92

NPN SILICON HIGH-SPEED SWITCHING TRANSISTORS

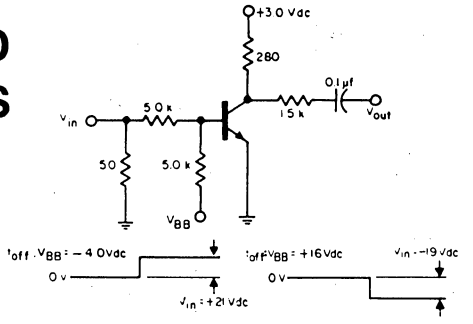


Figure 1 — Turn-On and Turn-Off Time Measurement Circuit

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Total Device Dissipation @ T_C = 25°C	500 mW
Derate above 25°C	4.55 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C

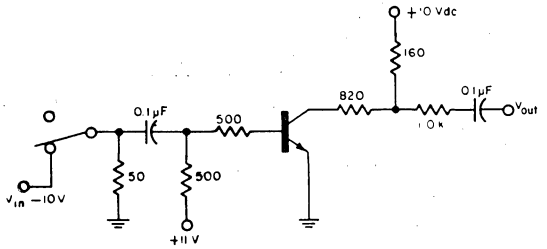


Figure 2 — Charge Storage Time Constant Measurement Circuit

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	—	Vdc	I_C = 10 uAdc, I_E = 0
BV_{EBO}	5.0	—	Vdc	I_E = 10 uAdc, I_C = 0
I_{CES}	—	10	uAdc	V_{CE} = 30 Vdc, V_{BE} = 0
I_{CBO}	—	0.5	uAdc	V_{CB} = 20 Vdc, I_E = 0
h_{FE}*	25	—	—	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$*	—	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
	—	0.4		I_C = 50 mAdc, I_B = 5.0 mAdc
$V_{BE(sat)}$*	—	0.9	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	350	—	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz
C_{ob}	—	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
t_{on}	—	16	ns	Turn-On Time I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc See Figure 1
t_{off}	—	30	ns	Turn-Off Time I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc See Figure 1
t_s	—	25	ns	Storage Time I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc See Figure 2

*Pulse Test: Pulse Width ≥ 12 ns, Duty Cycle ≥ 2.0%.

NPN HIGH-SPEED SWITCHING TRANSISTORS

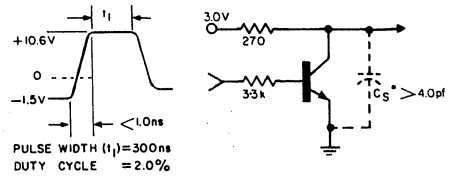


Figure 1 – t_{on} Circuit

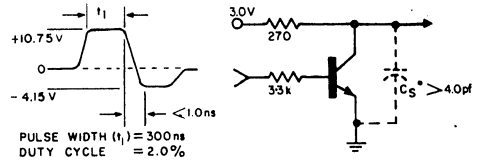


Figure 2 – t_{off} Circuit

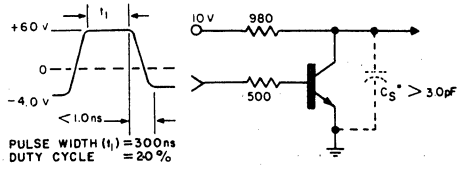


Figure 3 – Storage Test Circuit

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	4.5 Vdc
Collector Current-Peak	500 mAdc
Total Device Dissipation	
@ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction	
Temperature Range	-55 to +135 °C
Thermal Resistance, Junction	
to Ambient	0.355 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	40	–	Vdc	I_C = 10 μAdc, V_{BE} = 0
BV_{CBO}	40	–	Vdc	I_C = 10 μAdc, I_E = 0
BV_{EBO}	4.5	–	Vdc	I_E = 10 μAdc, I_C = 0
I_{CBO}	–	0.4	μAdc	V_{CB} = 20 Vdc, I_E = 0
	–	30		V_{CB} = 20 Vdc, I_E = 0, T_A = 125°C
h_{FE}*	40	120	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	20	–		I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = 55°C
	20	–		I_C = 100 mAdc, V_{CE} = 2.0 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$*	0.70	0.85	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
C_{ob}	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz
h_{fe}	5.0	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
t_{on}	–	12	ns	V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc Figure 1
t_{off}	–	18	ns	V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc Figure 2
t_s	–	13	ns	I_{B1} = I_{B2} = I_C = 10 mAdc Figure 3

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2.0%.

ITT SEMICONDUCTORS

Package: To-92

NPN SILICON LOW-POWER SMALL-SIGNAL TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	18 Vdc
Collector-Base Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.5	*u*Adc	V_{CB} = 18 Vdc, I_E = 0
	–	1.5		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	0.5	*u*Adc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	30	90	–	V_{CE} = 4.5 Vdc, I_C = 2 mAdc MPS2711
	75	225		MPS2712
C_{ob}	–	4.0	pF	V_{CB} = 10 V, I_E = 0 f = 1 MHz
h_{fe}	30	120	–	V_{CE} = 10 Vdc, I_C = 2 mAdc, f = 1 kHz MPS2711
	80	200		MPS2712

MPS2713, MPS2714

GENERAL PURPOSE LOW-LEVEL NPN SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Base Voltage	18 Vdc
Collector-Emitter Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mAdc
Total Device Dissipation @ T_A = 60°C	210 mW
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Thermal Resistance, Junction to Ambient	0.357 °C/mW
Junction Operating Temperature	135 °C
Storage Temperature Range	-55 to +135 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
I_{CBO}	–	–	0.5	uAdc	V_{CB} = 18 Vdc, I_E = 0
	–	–	15		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	0.5	uAdc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	30	60	90	–	I_C = 2 mAdc, V_{CE} = 4.5 Vdc MPS2713
	75	150	225		MPS2714
$V_{CE(sat)}$	–	0.16	0.3	Vdc	I_C = 50 mAdc, I_B = 3 mAdc
$V_{BE(sat)}$	0.6	0.75	1.3	Vdc	I_C = 50 mAdc, I_B = 3 mAdc
h_{fe}	30	–	120	–	I_C = 2 mAdc, V_{CE} = 4.5 Vdc, f = 1 kHz MPS2713
	80	–	300		MPS2714
f_T	–	250	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	2.5	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
h_{ie}	–	3000	–	ohms	I_C = 0.5 mAdc, V_{CE} = 1 Vdc, f = 1 kHz
t_d	–	7.0	–	ns	Delay Time I_C = 10 mA, I_{B1} = 3 mA,
t_r	–	6.0	–	ns	Rise Time V_{CC} = 10 V
t_s	–	12	–	ns	Storage Time I_C = 10 mA, I_{B1} = 3 mA,
t_f	–	9.0	–	ns	Fall Time I_{B2} = 1 mA, V_{CC} = 10 V

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GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Base Voltage	25 Vdc
Collector-Emitter Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector dc Current	100 mAdc
Total Device Dissipation	200 mW
@ 25°C Ambient Temperature	
Derating Factor above 25°C	2.67 mW/°C
Total Device Dissipation	120 mW
@ 55°C Ambient Temperature	
Derating Factor above 25°C	2.67 mW/°C
Junction Temperature-Operating	100 °C
Storage Temperature Range	-30 to +125 °C

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.5	uA	V_{CB} = 25 V, I_E = 0
	–	15	uA	V_{CB} = 25 V, I_E = 0, T_A = 100°C
I_{EBO}	–	0.5	uA	V_{EB} = 5 V
h_{fe}			–	V_{CE} = 10 V, I_C = 2 mA
	90	180		MPS2923
	150	300		MPS2924
	235	470		MPS2925
C_{ob}	–	12	pF	V_{CB} = 10 V, I_E = 0, f = MHz

MPS2926, MPS3721

Package: To-92

GENERAL PURPOSE NPN SILICON TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	18 Vdc
Collector-Base Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ 25°C Ambient Temperature	310 mW
Total Device Dissipation @ 60°C Ambient Temperature	210 mW
Thermal Resistance, Junction to Ambient	0.357 °C/mW
Junction Temperature, Operating	135 °C
Storage Temperature Range	-55 to +135 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
I_{CBO}	–	–	0.5	uA	V_{CB} = 18 Vdc, I_E = 0
	–	–	15		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	0.5	uA	V_{EB} = 5 Vdc, I_C = 0
f_T	–	300	–	MHz	I_C = 4 mA, V_{CE} = 5 V MPS 2926
C_{ob}	–	–	3.5	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{fe}	35	–	470	–	V_{CE} = 10 V, I_C = 2 mA, f = 1 kHz MPS2926
	60	–	660		MPS3721

NPN SILICON SMALL-SIGNAL AUDIO TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	–	Vdc	I_C = 1 mAdc, I_B = 0
I_{CBO}	–	0.1	*u*Adc	V_{CB} = 18 Vdc, I_E = 0
I_{EBO}	–	0.1	*u*Adc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	150	300	–	V_{CE} = 4.5 Vdc, I_C = 2 mAdc MPS3392
	90	180		MPS3393
	55	110		MPS3394
	150	500		MPS3395
C_{ob}	–	3.5	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{fe}	150	500	–	V_{CE} = 4.5 V, I_C = 2 mA, f = 1 kHz MPS3392
	90	400		MPS3393
	55	300		MPS3394
	150	800		MPS3395

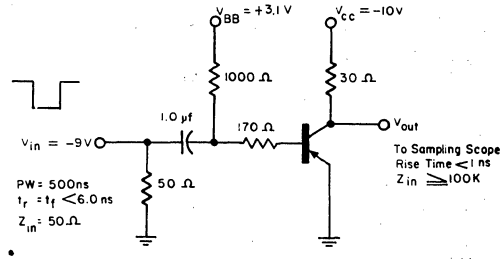
MPS3638, MPS3638A
PNP SILICON TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	25	–	Vdc	I_C = 100 uAdc, V_{BE} = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CES}	–	0.035	uAdc	V_{CE} = 15 Vdc, V_{BE} = 0
	–	2.0		V_{CE} = 15 Vdc, V_{BE} = 0, T_A = 65°C
I_B	–	0.035	uAdc	V_{CE} = 15 Vdc, V_{BE} = 0
h_{FE}*	80	–	–	I_C = 1 mAdc, V_{CE} = 10 Vdc MPS3638A
	20	–		I_C = 10 mAdc, V_{CE} = 10 Vdc MPS3638
	100	–		MPS3638A
	30	–		I_C = 50 mAdc, V_{CE} = 1 Vdc MPS3638
	100	–		MPS3638A
	20	–		I_C = 300 mAdc, V_{CE} = 2 Vdc MPS3638
	20	–		MPS3638A
$V_{CE(sat)}$*	–	0.25	Vdc	I_C = 50 mAdc, I_B = 2.5 mAdc
	–	1.0		I_C = 300 mAdc, I_B = 30 mAdc
$V_{BE(sat)}$*	–	1.1	Vdcq	I_C = 50 mAdc, I_B = 2.5 mAdc
	0.80	2.0		I_C = 300 mAdc, I_B = 30 mAdc
f_T	100	–	MHz	V_{CE} = 3 Vdc, I_C = 50 mAdc, f = MHz MPS3638
	150	–		MPS3638A
C_{ob}	–	20	pF	V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz MPS3638
	–	10		MPS3638A

ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified

SYMBOL	MIN	MAX	UNIT	CONDITIONS
C_{ib}	–	65	pF	V_{CE} = 0.5 Vdc, I_C = 0, f = 140 kHz MPS3638
	–	25		MPS3638A
h_{fe}	25	180	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, F = 1.0 kHz MPS3638
	100	–		MPS3638A
h_{oe}	–	1.2	mmhos	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz
h_{ie}	–	1500	Ohms	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz MPS3638
	–	2000		MPS3638A
h_{re}	–	26	X10-4	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz MPS3638
	–	15		MPS3638A
t_d	–	20	ns	Delay Time V_{CC} = 10 Vdc, I_C = 300 mAdc,
t_r	–	70	ns	Rise Time I_{B1} = 30 mAdc, $V_{BE(off)}$ = 3.1 Vdc
t_s	–	140	ns	Storage Time V_{CC} = 10 Vdc, I_C = 300 mAdc,
t_f	–	70	ns	Fall Time I_{B1} = 30 mAdc, I_{B2} = 30 mAdc
t_{on}	–	75	ns	Turn-On Time I_C = 300 mAdc, I_{B1} = 30 mAdc
t_{off}	–	170	ns	Turn-Off Time I_C = 300 mAdc, I_{B1} = 30 mAdc, I_{B2} = 30 mAdc

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 1%.

ITT SEMICONDUCTORS

Package: To-92

NPN SILICON GENERAL PURPOSE RF AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	45 Vdc
Collector-Base Voltage	45 Vdc
Emitter-Base Voltage	4.0 Vdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
$BV_{CEO(sus)}$*	45	–	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	45	–	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 10 uAdc, I_C = 0
I_{CBO}	–	–	50	nAdc	V_{CB} = 35 Vdc, I_E = 0
	–	–	5.0	uAdc	V_{CB} = 35 Vdc, I_E = 0, T_A = 65°C
h_{FE}	40	–	160	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
f_T	200	–	–	MHz	I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 100 MHz
C_{ob}	–	–	3.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
r'_bC_c	–	–	55	ps	I_E = 10 mAdc, V_{CB} = 15 Vdc, f = 31.8 MHz
NF	–	4.0	–	dB	I_C = 3.0 mAdc, V_{CE} = 10 Vdc, R_S = 300 ohms, f = 1.0 MHz

*Pulse Test: Pulse Width $\leq$ 300 us; Duty Cycle $\leq$ 1.0%.

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ABSOLUTE MAXIMUM RATINGS

Characteristics	MPS3702	MPS3703	Unit
Collector-Emitter Voltage	25	30	Vdc
Collector-Base Voltage	40	50	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current - Continuous	200		mAdc
Total Device Dissipation @ 25°C Case Temperature	.8		W
Operating and Storage Junction Temperature Range	-55 to +135		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	25	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS3702
	30	–			MPS3702
BV_{CBO}	40	–	Vdc	I_C = 100 uAdc, I_E = 0	MPS3702
	50	–			MPS3703
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	60	300	–	I_C = 50 mAdc, V_{CE} = 5 Vdc	MPS3702
	30	150			MPS3703
$V_{CE(sat)}$*	–	0.25	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(on)}$*	0.6	1.0	Vdc	I_C = 50 mAdc, V_{CE} = 5 Vdc	
f_T	100	–	MHz	I_C = 50 mAdc, V_{CE} = 5 Vdc, f = 20 MHz	
C_{ob}	–	12	pF	V_{CB} = 10 Vdc, f = 1 MHz	

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 2%.

NPN SILICON LOW-POWER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	MPS3704 MPS3705	MPS3706	Unit
Collector-Emitter Voltage ...	30	20	Vdc
Collector-Base Voltage	50	40	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current - Continuous	600		mAdc
Total Device Dissipation			
@ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction			
Temperature Range	-55 to +135		°C
Thermal Resistanct, Junction			
to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 10 mAdc, I_E = 0	MPS3704
	30	–			MPS3705
	20	–			MPS3706
BV_{CBO}	50	–	Vdc	I_C = 100 uAdc, I_E = 0	MPS3704
	50	–			MPS3705
	40	–			MPS3706
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	100	300	–	I_C = 50 mAdc, V_{CE} = 2 Vdc	MPS3704
	50	150			MPS3705
	30	600			MPS3706
$V_{CE(sat)}$*	–	0.6	Vdc	I_C = 100 mAdc, I_B = 5 mAdc	MPS3704
	–	0.8			MPS3705
	–	1.0			MPS3706
$V_{BE(on)}$*	0.5	1.0	Vdc	I_C = 100 mAdc, V_{CE} = 2 Vdc	
f_T	100	–	MHz	I_C = 50 mAdc, V_{CE} = 2 Vdc, f = 20 MHz	
C_{ob}	–	12	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz	

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 2%.

ITT SEMICONDUCTORS

Package: To-92

NPN SILICON GENERAL PURPOSE AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	30 Vdc
Emitter-Base Voltage	6.0 Vdc
Collector Current	30 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}	30	–	Vdc	I_C = 1 mAdc, I_B = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{EB} = 6 Vdc, I_C = 0	
h_{FE}	100	400	–	I_C = 100 uAdc, V_{CE} = 5 Vdc	MPS3707
	45	660		I_C = 1 mAdc, V_{CE} = 5 Vdc	MPS3708
	45	165			MPS3709
	90	330			MPS3710
	180	660			MPS3711
$V_{CE(sat)}$	–	1.0	Vdc	I_C = 10 mAdc, I_B = 0.5 mAdc	
V_{BE}	0.5	1.0	Vdc	I_C = 1 mAdc, V_{CE} = 5 Vdc	
h_{FE}	100	550	–	I_C = 100 uAdc, V_{CE} = 5 Vdc, f = 1 kHz MPS3707	
	45	800		I_C = 1 mAdc, V_{CE} = 5 Vdc, f = 1 kHz MPS3708	
	45	250			MPS3709
	90	450			MPS3710
	180	800			MPS3711
NF	–	5.0	dB	V_{CE} = 5 V, I_C = 100 uA, R_G = 5 kΩ, Noise Bandwidth = 15.7 kHz Note 1	MPS3707

Note 1 Average Noise Figure is measured in an amplifier with low frequency response down 3 dB at 10 Hz.

ITT SEMICONDUCTORS

Package: To-92

NPN SILICON GENERAL PURPOSE AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	210 mW
Derate above 25°C	1.91 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.524 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	25	–	–	Vdc	I_C = 10 mAdc, I_B = 0
I_{CES}	–	–	100	nAdc	V_{CE} = 25 Vdc, V_{BE} = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 25 Vdc, I_E = 0
	–	–	10	uAdc	V_{CB} = 25 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	100	nAdc	V_{BE} = 5.0 Vdc, I_C = 0
h_{FE}	100	–	500	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	0.75	–	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	0.5	–	1.2	Vdc	I_C = 10 mAdc, V_{CE} = 10 Vdc
f_T	–	120	–	MHz	I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc
C_{cb}	1.6	–	10	pF	V_{CB} = 0, I_E = 0, f = 1.0 MHz
h_{fe}	100	–	750	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

MPS6530 thru MPS6532

NPN SILICON AMPLIFIER TRANSISTORS

Package: To-92

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic			Unit
Collector-Base Voltage			
MPS6530, MPS5631	60		Vdc
MPS6532	50		
MPS6530, MPS6531	40		
MPS6532	30		
Emitter-Base Voltage	5.0	4.0	

Collector Current	600	600	mAdc
Total Device Dissipation			
@ T_A = 60°C	210	210	mW
@ T_A = 25°C	310	310	
Thermal Resistance, Junction to Ambient	0.357	0.357	°C/mW
Junction Temperature	135	135	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions	
BV_{CBO}	60	–	–	Vdc	I_C = 10 uAdc, I_E = 0	MPS6530, MPS6531
	50	–	–			MPS6532
BV_{CEO}	40	–	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS6530, MPS6531
	30	–	–			MPS6532
BV_{EBO}	5.0	–	–	Vdc	I_B = 10 uAdc, I_C = 0	
I_{CBO}	–	–	0.05	uAdc	V_{CB} = 40 Vdc, I_E = 0	MPS6530, MPS6531
	–	–	0.1			MPS6532
	–	–	2.0		V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C	MPS6530, MPS6531
	–	–	5.0		V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C	MPS6532
h_{FE}	30	75	–	–	I_C = 10 mAdc, V_{CE} = V_{CE} = 1 Vdc	MPS6530
	60	120	–			MPS6531
	40	85	120		I_C = 100 mAdc, V_{CE} = 1 Vdc	MPS6530
	90	150	270			MPS6531
	30	–	–			MPS6532
	25	60	–		I_C = 500 mAdc, V_{CE} = 10 Vdc	MPS6530
	50	80	–			MPS6531
$V_{CE(sat)}$	–	0.2	0.5	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6530, MPS6532
	0.13	0.13	0.3			MPS6531
$V_{BE(sat)}$	–	0.82	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6530, MPS6531
	–	0.85	1.2			MPS6532
C_{ob}	–	3.5	5.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz	
f_T	–	390	–	MHz	I_C = 50 mAdc, V_{CE} = 10 Vdc	

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PNP SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic			Unit
Collector-Base Voltage			
MPS6533, MPS6534		40	Vdc
MPS6535		39	
Collector-Emitter Voltage			
MPS6533, MPS6534		40	
MPS6535		30	

Emitter-Base Voltage	5.0	4.0	Vdc
Collector Current	600	600	mAdc
Total Device Dissipation			
@ T_A = 60°C	210	210	mW
@ T_A = 25°C	310	310	
Thermal Resistance, Junction to Ambient	0.357	0.357	°C/mW
Junction Temperature	135	135	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions	
BV_{CBO}	40	–	–	Vdc	I_C = 10 *u*Adc, I_E = 0	MPS6533, MPS6534
	30	–	–			MPS6535
BV_{CEO}	40	–	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS6533, MPS6534
	30	–	–			MPS6535
BV_{EBO}	4.0	–	–	Vdc	I_B = 10 *u*Adc, I_C = 0	
I_{CBO}	–	–	0.05	*u*Adc	V_{CB} = 30 Vdc, I_E = 0	MPS6533, MPS6534
	–	–	0.1		V_{CB} = 20 Vdc, I_E = 0	MPS6535
	–	–	2.0		V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C	MPS6533, MPS6534
	–	–	5.0		V_{CB} = 20 Vdc, I_E = 0, T_A = 60°C	MPS6535
h_{FE}	30	70	–	–	I_C = 10 mAdc, V_{CE} = 1 Vdc	MPS6533
	60	110	–			MPS6534
	40	85	120		I_C = 100 mAdc, V_{CE} = 1 Vdc	MPS6533
	90	140	270			MPS6534
	30	–	–			MPS6535
	25	55	–		I_C = 500 mAdc, V_{CE} = 10 Vdc	MPS6533
	50	70	–			MPS6534
$V_{CE(sat)}$	–	0.2	0.5	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6533, MPS6535
	–	0.13	0.3			MPS6534
$V_{BE(sat)}$	–	0.84	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6533, MPS6534
	–	0.87	1.2			MPS6535
C_{ob}	–	4.8	6.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz	
f_T	–	260	–	MHz	I_C = 50 mAdc, V_{CE} = 10 Vdc	

Package: To-92

GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	45 Vdc
Collector-Base Voltage	60 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	200 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	45	–	–	Vdc	I_C = 1 mAdc, I_B = 0
BV_{CBO}	60	–	–	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	–	160	–	I_C = 10 mAdc, V_{CE} = 10 Vdc MPS6565
	100	–	400		MPS6566
$V_{CE(sat)}$	–	0.1	0.4	Vdc	I_C = 10 mAdc, I_B = 1 mAdc
C_{ob}	–	–	3.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	3.7	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz
h_{fe}	2.0	–	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
h_{oe}	–	60	–	*u*mhos	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{ie}	–	500	–	ohms	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{re}	–	2.5	–	$X10^{-4}$	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
NF	–	4.0	–	dB	I_C = 100 *u*Adc, V_{CE} = 5 Vdc, R_S = 1000 ohms, f = 10 Hz to 15.7 kHz

MPS6591®

NPN SILICON AMPLIFIER TRANSISTOR

Package: To-92

High Voltage ..... BV_{CEO} = 80 V (Min) MPS6590
Low Noise ..... NF = 3.0 dB (Typ) Wideband

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Total Dissipation (Notes 2 and 3)	
at 25°C Case Temperature	1.0 W
at 25°C Ambient Temperature	.625 W
at 70°C Ambient Temperature	.400 W
Collector to Base Voltage	60 V
Collector to Emitter Voltage (Note 4)	50 V
Emitter to Base Voltage	4.0 V
DC Collector Current	250 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Test Conditions
BV_{CEO}	50			Volts	I_C = 1.0 mA, I_B = 0
BV_{CBO}	60			Volts	I_C = 100 uA, I_E = 0
BV_{EBO}	4.0			Volts	I_E = 100 uA, I_C = 0
I_{CBO}				nA	V_{CB} = 50 V, I_E = 0
I_{CBO}			100	nA	V_{CB} = 30 V, I_E = 0
h_{FE}	40				I_C = 10 mA, V_{CE} = 10 V
$V_{CE(sat)}$			0.6	Volt	I_C = 10 mA, I_B = 1.0 mA
C_{cb}			12	pF	V_{CB} = 10 V, I_E = 0, f = 100 kHz
C_{eb}			50	pF	V_{BE} = 0.5 V, I_C = 0, f = 100 kHz
h_{ie}		1.4		kΩ	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
h_{re}		0.8		$X10^{-4}$	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
h_{fe}	2.0				I_C = 10 mA, V_{CE} = 10W, f = 30 MHz
h_{oe}		75		umhos	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
NF		3.0		dB	I_C = 100 uA, V_{CE} = 5.0 V, f = 10 Hz to 15.7 kHz, R_s = 4kΩ

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 150°C and junction to case thermal resistance of 125° C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C).
(4) Rating refers to a high current point where collector to emitter voltage is lowest.
(5) Pulse conditions: length = 300 us; duty cycle = 1%.

GENERAL PURPOSE NPN SILICON PLANAR EPITAXIAL TRANSISTOR

For Improved Performance See ITT 2N2217.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage	35	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	175	•C
Storage Temperature	-65 to +200	•C
P_D @ T_C = 25•C	2.0	Watts
P_D @ T_A = 25•C	0.6	Watt

ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	60		Vdc	I_C = 100 A
LV_{CER}	40		Vdc	I_C = 30mA, R_{BE} = 10 pulsed
BV_{EBO}	5		Vdc	I_E = 100 A
h_{FE}	20	60		I_C = 150mA, V_{CE} = 10V pulsed
V_{CE} (sat)		1.5	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{BE} (sat)		1.3	Vdc	I_C = 150mA, I_B = 15mA pulsed
I_{CBO}		1.0	A	V_{CB} = 30V
I_{CBO}		100	A	V_{CB} = 30V, T_A = +150•C
C_{ob}		35	pF	V_{CB} = 10V
h_{fe}	2			I_C = 50mA, V_{CE} = 10V, f = 20MHz

NOTES: Pulse width 300 sec, duty cycle 2%.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2368.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	25	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	3	Volts
Operating Junction Temperature	200	°C
Storage Temperature	-65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

ELECTRICAL CHARACTERISTICS (25C• free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	25		Vdc	I_C = 1.0µA
V_{CER}	20		Vdc	I_C = 30mA, R_{BE} = 10Ωpulsed
BV_{EBO}	3		Vdc	I_E = 10µA
h_{FE}	20			I_C = 10mA, V_{CE} = 1.0V
V_{CE} (sat)		0.6	Vdc	I_C = 10mA, I_B = 1.0mA
V_{BE} (sat)		0.9	Vdc	I_C = 10mA, I_B = 1.0mA
I_{CBO}		50	nA	V_{CB} = 15V
I_{CBO}		30	µA	V_{CB} = 15V, T_A = +150•C
C_{ob}		6.0	pF	V_{CB} = 10V
h_{fe}	2			I_C = 10mA, V_{CE} = 15V, f = 100MHz
t_{pd}	5	11	ns	I_C = 4.5mA
t_s		60	ns	I_C = I_{B1} = I_{B2} = 10mA, V_{CC} = 10V, R_L = 1KΩ

NOTE: Pulse width 300 sec, duty cycle 2%.)

2N706, 2N706A, 2N706B

SILICON SWITCHING TRANSISTOR

ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	25		Vdc	I_C = 10µA
LV_{CER}	20		Vdc	I_C = 10mA, R_{BE} = 10Ωpulsed
BV_{EBO}	5		Vdc	I_E = 10µA
h_{FE}	20			I_C = 10mA, V_{CE} = 1V
V_{CE} (sat)		0.6	Vdc	I_C = 10mA, I_B = 1mA
V_{BE} (sat)	0.7	0.9	Vdc	I_C = 10mA, I_B = 1mA
I_{CBO}		0.5	µA	V_{CB} = 15V
I_{CBO}		30	µA	V_{CB} = 15V, T_A = 150•C
C_{ob}		5	pF	V_{CB} = 5V
h_{fe}	2			I_C = 10mA, V_{CE} = 10V, f = 100MHz
t_s		25	ns	I_C = I_{B1} = I_{B2} = 10mA, V_{CC} = 10V, R_L = 1KΩ
t_{on}		40	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω
t_{off}		75	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω

ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	25		Vdc	I_C = 10 A
LV_{CER}	20		Vdc	I_C = 10mA, R_{BE} = 10 pulsed
LV_{CEO}	15		Vdc	I_C = 10mA pulsed
BV_{EBO}	5		Vdc	I_E = 10µA
h_{FE}	20	60		I_C = 10mA, V_{CE} = IV
V_{CE} (sat)		0.4	Vdc	I_C = 10mA, I_B = 1mA
V_{BE} (sat)	0.7	0.9	Vdc	I_C = 10mA, I_B = 1mA
I_{CBO}		0.5	µA	V_{CB} = 15V
I_{CBO}		30	µA	V_{CB} = 15V, T_A = 150•C
I_{CER}		10	µA	V_{CE} = 20V, R_{BE} = 100K
C_{ob}		5	pF	V_{CB} = 5V
h_{fe}	2.0			I_C = 10mA, V_{CE} = 10V, f = 100MHz
$r_{b/}$		50	ohms	I_C = 10mA, V_{CE} = 15V, f = 300MHz
T_s		25	ns	I_C = I_{B1} = I_{B2} = 10mA, V_{CC} = 10V, R_L = 1KΩ
t_{on}		40	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω
t_{off}		75	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω

NOTE: Pulse width 300 sec, duty cycle 2%.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369A.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	200	°C
Storage Temperature	-65 to +200	°C
P_D @ T_C = 25°C	1.2	Watts
P_D @ T_A = 25°C	.36	Watt

ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	40		Vdc	I_C = 1μA
LV_{CER}	20		Vdc	I_C = 3mA pulsed, R_{BE} = 10Ω
LV_{CEO}	15		Vdc	I_C = 30mA pulsed
BV_{EBO}	5		Vdc	I_E = 10μA
h_{FE}	30	120		I_C = 10mA, V_{CE} = 1V
h_{FE}	15			I_C = 0.5mA, V_{CE} = 1V, T_A = -55•C
h_{FE}	15			I_C = 10mA, V_{CE} = 1V
V_{CE} (sat)		.40	Vdc	I_C = 10mA, I_B = 1.0mA
V_{CE} (sat)		.40	Vdc	I_C = 7mA, I_B = .7mA, T_A = +125•C
V_{BE} (sat)	.72	.80	Vdc	I_C = 10mA, I_B = 1.0mA
V_{BE} (sat)		.90	Vdc	I_C = 10mA, I_B = 1.0mA, T_A = -55•C
I_{CBO}		25	nA	V_{CB} = 20V
I_{CBO}		15	μA	V_{CB} = 20V, T_A = +150•C
I_{EBO}		0.1	μA	V_{EB} = 4V
I_{CEX}		10	μA	V_{CE} = 20V, V_{EB} = .25V, T_A = 125•C
C_{ob}		6	pF	V_{CB} = 10V
h_{fe}	3			I_C = 10mA, V_{CE} = 10V, f = 100MHz
r_b		50	ohms	I_C = 10mA, V_{CE} = 10V, f = 300MHz
T_s		25	ns	I_C = I_{B1} = I_{B2} = 10mA
t_{on}		40	ns	I_C = 10mA, I_{B1} = 3mA, V_{EB} = 2V
t_{off}		75	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA

NOTE: Pulse width ≤300μsec, duty cycle ≤2%.

HIGH SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	20	Volts
Collector-to-Emitter Voltage	12	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	200	°C
Storage Temperature	-65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	20		Vdc	I_C = 1µA
LV_{CEO}	12		Vdc	I_C = 10mA pulsed
BV_{EBO}	5		Vdc	I_C = 10µA
h_{FE}	20			I_C = 1.0mA, V_{CE} = 0.25V
h_{FE}	40	120		I_C = 10mA, V_{CE} = 0.35V
h_{FE}	20			I_C = 100mA, V_{CE} = 1.0V pulsed
h_{FE}	20			I_C = 10mA, V_{CE} = 0.35V, T_A = -55•C
V_{CE} (sat)	0.35		Vdc	I_C = 10mA, I_B = 1mA, T_A = 170•C
V_{CE} (sat)	1		Vdc	I_C = 100mA, I_B = 10mA, T_A = 170•C pulsed
V_{BE} (sat)	0.65	0.85	Vdc	I_C = 10mA, I_B = 1 mA
V_{BE} (sat)		1.5	Vdc	I_C = 100mA, I_B = 10mA pulsed
V_{BE} (sat)		1.1	Vdc	I_C = 10mA, I_B = 1 mA, T_A = -55•C
V_{BE} (sat)		1.6	Vdc	I_C = 100mA, I_B = 10mA, T_A = -55•C pulsed
I_{CBO}		1	µA	V_{CB} = 20V
I_{CEO}		30	µA	V_{CE} = 10V, V_{BE} = 0.35V, T_A = 100•C
I_{CES}		1	µA	V_{CE} = 20V
I_{CES}		100	µA	V_{CE} = 20V, T_A = 170•C
C_{ob}		5	pF	V_{CB} = 5V
h_{fe}	2.8			I_C = 10mA, V_{CE} = 10V, f = 100MHz
T_s		18	ns	I_C = I_{B1} = I_{B2} = 10mA
t_{on}		12	ns	I_C = 100mA, I_{B1} = 40mA, I_{B2} = 20mA
t_{on}		16	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1.5mA
t_{off}		45	ns	I_C = 100mA, I_{B1} = 40 mA, I_{B2} = 20mA
t_{off}		24	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1.5mA

NOTE: Pulse width≤300µsec, duty cycle ≤2%.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369.

2N834 ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage	25	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	175	°C
Storage Temperature	-65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

2N834 ELECTRICAL CHARACTERISTICS (25•C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	40		Vdc	I_C = 100 A
BV_{CES}	30		Vdc	I_C = 10 A
BV_{EBO}	5		Vdc	I_E = 100 A
h_{FE}	25			I_C = 10mA, V_{CE} = 1.0V
V_{CE} (sat)		0.25	Vdc	I_C = 10mA, I_B = 1.0mA
V_{CE} (sat)		0.4	Vdc	I_C = 50mA, I_B = 5.0mA pulsed
V_{BE} (sat)		0.9	Vdc	I_C = 10mA, I_B = 1.0mA
I_{CBO}		0.5	A	V_{CB} = 20V
I_{CBO}		30	A	V_{CB} = 20V, T_A = 150°C
C_{ob}		4	pF	V_{CB} = 10V
h_{fe}	3.5			I_C = 10mA. V_{CE} = 15V. f = 100MHz
s		25	ns	I_C = 10mA, I_{B1} = I_{B2} = 10mA
t_{on}		35	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA
t_{off}		75	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA

NOTE: Pulse width 300 sec, duty cycle 2%.

2N2195, 2N2195A, 2N2195B®
HIGH-SPEED NPN SILICON HIGH-CURRENT SWITCHING TRANSISTORS

Package TO-5

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	45 Volts
Collector-Emitter Voltage (Note 4)	25 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	1.0 Amp
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.8 Watts
T_C = 100°C (Notes 2 and 3)	1.6 Watts
T_A = 25°C (Notes 2 and 3)	0.6 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65 to +200 °C
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/watt (derating factor of 16 mW/°C); junction-to-ambient thermal resistance of 292°C/watt (derating factor of 3.42 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length ≤ 300 μsec, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	20	–	–	I_C = 150 mA, V_{CE} = 10 Volts
h_{FE}	10	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt
$V_{CE(sat)}$	–	0.35	Volt	I_C = 150 mA, I_B = 15 mA (2N2195)
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA (2N2195A
$V_{CE(sat)}$	–	0.18	Volt	I_C = 150 mA, I_B = 15 mA (2N2195B)
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts
C_{ob}	–	20	pF	I_E = 0, V_{CB} = 10 Volts
I_{CBO}	–	100	nA	I_E = 0, V_{CB} = 30 Volts
$I_{CBO(150°C)}$	–	50	μA	I_E = 0, V_{CB} = 30 Volts
I_{EBO}	–	100	nA	I_C = 0, V_{EB} = 3.0 Volts
BV_{CBO}	45	–	Volts	I_C = 100 μA, I_E = 0
$V_{CEO(sust)}$	25	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 100 min. @ I_C = 10 A**
- **Low Noise; 3dB max. @ I_C = 10 A**
- **High V_{CEO}; 45 Vdc min.**

The ITT 2N929 and 2N930 are NPN silicon planar transistors designed for application in low noise, low level amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		Units
Collector-to-Base Voltage	45	Volts
Collector-to-Emitter Voltage (open base)	45	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	30	mA
Junction Temperature (operating)	-65 to +175	°C
(storage)	-65 to +200	°C
Total Power Dissipation @ T_C = 25°C (derate 4.0 mW/°C above 25°C)	0.6	Watts
Total Power Dissipation @ T_A = 25°C (derate 2.0 mW/°C above 25°C)	0.3	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

Symbol	Min.	Max.	Unit	Conditions
LV_{CEO}	45		Vdc	I_C = 10mA
BV_{EBO}	5.0		Vdc	I_E = 10nA
h_{FE}				I_C = 10 A, V_{CE} = 5.0V
	40	120		2N929
	100	300		2N930
				I_C = 500 A, V_{CE} = 5.0V
	60			2N929
	150			2N930
				I_C = 10mA, V_{CE} = 5.0V
		350		2N929
		600		2N930
				I_C = 10 A, V_{CE} = 5.0V, T_A = -55°C
	10			2N929
	20			2N930

2N929, 2N930

SILICON GENERAL PURPOSE TRANSISTOR

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted **(continued)**

Symbol	Min.	Max.	Unit	Conditions
V_{CE} (sat) [1]		1.0	Vdc	I_C = mA, I_B = 0.5mA
V_{BE} (sat) [1]	0.6	1.0	Vdc	I_C = 10mA, I_B = 0.5mA
I_{CBO}		10	nA	V_{CB} = 45V
I_{CEO}		2	nA	V_{CE} = 5V
I_{EBO}		10	nA	V_{EB} = 5V
I_{CES}		10	nA	V_{CE} = 45V
I_{CES}		10	A	V_{CE} = 45V, T_A = 170 •C
C_{ob}		8	pF	V_{CB} = 5V
h_{fe}				I_C = 1.0mA, V_{CE} = 5V, f = 1KHz
	60	350		2N929
	150	600		2N930
	1.0	1.0		I_C = 500 A, V_{CE} = 5V, f = 30mHz
h_{ib}	25	32	ohms	I_C = 1.0mA, V_{CB} = 5V, f = 1mHz
h_{ob}		1.0	mho	I_C = 1.0mA, V_{CB} = 5V, f = 1mHz
h_{rb}		600	X10-^{6}	I_C = A, V_{CB} = 5V
NF				I_C = 10 A, V_{CE} = 5V, R_G = 10K B.W. = 200Hz, f = 1KHz
		4	dB	2N929
		3	dB	2N930

Notes: 1. Pulse width 300 sec; duty cycle 2%.
2. Lowest emitter to collector voltage.

GENERAL PURPOSE NPN SILICON PLANAR EPITAXIAL TRANSISTORS

- **Low V_{CE} (sat), 0.4V @ I_C = 150mA**
- **High Frequency, f_T = 250 MHz @ I_C = 20mA**
- **Wide Useful Current Range, 0.1 to 500mA**

The ITT 2N2217-19 are NPN silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500mA. Low saturation voltage and fast switching times make the 2N2217-19 ideal for core driving. The flat grain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	30	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	800	mA
Junction Temperature (operating)	-65 to +175	°C
(storage)	-65 to +300	°C
Total Power Dissipation @ T_C = 25°C	3.0	Watts
(derate 20mW/°C above 25°C)		
Total power Dissipation @ T_A = 25°C	0.8	Watts
(derate 5.33 mW/°C above 25°C)		

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

Symbol	Min.	Max.	Unit	Conditions
h_{FE} (1)				I_C = 150mA, V_{CE} = 10V
	20	60		2N2217
	40	120		2N2218
	100	300		2N2219
				I_C = 150mA, V_{CE} = IV
	10			2N2217
	20			2N2218
	50			2N2219
h_{FE}				I_C = 500mA, V_{CE} = 10V
	20			2N2218
	30			2N2219

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted **(continued)**

Symbol	Min.	Max.	Unit	Conditions
				I_C = 10mA, V_{CE} = 10V
	17			2N2217
	35			2N2218
	75			2N2219
				I_C = 1mA, V_{CE} = 10V
	12			2N2217
	25			2N2218
	50			2N2219
				I_C = 0.1mA, V_{CE} = 10V
	20			2N2218
	35			2N2219
V_{CE} (sat) (1)		0.4	Vdc	I_C = 150mA, I_B = 15mA
		1.6	Vdc	I_C = 500mA, I_B = 50mA
V_{BE} (sat) (1)		1.3	Vdc	I_C = 150mA, I_B = 15mA
		2.6	Vdc	I_C = 500mA, I_B = 50mA
I_{CBO}		10	nA	V_{CB} = 50V, I_E = 0
		10	A	V_{CB} = 50V, I_E = 0, T = 150•C
I_{EBO}		10	nA	V_{EB} = 3V, I_C = 0
f_T	250		MHz	I_C = 20mA, V_{CE} = 20V
C_{ob}		8	pf	V_{CB} = 10V, I_E = 0
$R_{e(hie)}$ (2)		60	Ohms	I_C = 20mA, V_{CE} = 20V, f = 300MHz
BV_{CBO}	60		Vdc	I_C = 10 A, I_E = 0
V_{CEO} (sust) (1)	30		Vdc	I_C = 10mA, I_B = 0
BV_{EBO}	5		Vdc	I_E = 10 A, I_C = 0

NOTES: 1. Pulse Measurement: width 300 sec, duty cycle 2%.
2. Real part of Common-Emitter high frequency input impedance.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS CHARACTERISTICS	UNITS
Collector-to-Base Voltage 75	Volts
Collector-to-Emitter Voltage 40	Volts
Emitter-to-Base Voltage 6	Volts
Operating Junction Temperature 175	°C
Storage Temperature ..... -65 to +200	°C
P_D @ T_C = 25°C 3.0	Watts
P_D @ T_A = 25°C 0.8	Watts

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	75		Vdc	I_C = 10μA
LV_{EBO}	40		Vdc	I_C = 10mA pulsed
BV_{EBO}	6		Vdc	I_E = 10μA
h_{FE}	35			I_C = 100μA, V_{CE} = 10V
h_{FE}	50			I_C = 1 mA, V_{CE} = 10V
h_{FE}	75			I_C = 10mA, V_{CE} = 10V
h_{FE}	100	300		I_C = 150mA, V_{CE} = 10V pulsed
h_{FE}	40			I_C = 500mA, V_{CE} = 10V pulsed
h_{FE}	50			I_C = 150mA, V_{CE} = 1V pulsed
h_{FE}	35			I_C = 10mA, V_{CE} = 10V, T_A = -55°C
V_{CE} (sat)		0.3	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{CE} (sat)		1.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
V_{BE} (sat)	0.6	1.2	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{BE} (sat)		2.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
I_{CBO}		10	nA	V_{CB} = 60V
I_{CBO}		10	A	V_{CB} = 60V, T_A = 150°C

2N2219A
SILICON SWITCHING TRANSISTOR

ELECTRICAL CHARACTERISTICS continued

Parameter	Min.	Max.	Unit	Conditions
I_{CEX}		10	nA	V_{CE}= 60V, V_{EB}= 3V
I_{EBX}		20	nA	V_{EB}= 3V, V_{CB}= 60V
I_{EBO}		10	nA	V_{EB}= 3V
C_{ob}		8	pF	V_{CB}= 10V
C_{ib}		25	pF	V_{EB}= 0.5V
h_{fe}	50	300		I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{fe}	75	375		I_C= 10mA, V_{CE}= 10V, f= 1KHz
h_{fe}	3			I_C= 20mA, V_{CE}= 20, f = 100MHz
h_{ie}	2	8	Kohms	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{ie}	0.25	1.25	Kohms	I_C= 10mA, V_{CE}= 10V, f= 1KHz
h_{re}		8	x10 $^{-4}$	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{re}		4	x10 $^{-4}$	I_C= 10mA, V_{CE}= 10V, f = 1KHz
h_{oe}	5	35	mho	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{oe}	25	200	mho	I_C= 10mA, V_{CE}= 10V, 1f = KHz
$R_{e(hie)}$		60	omhs	I_C= 20mA, V_{CE}= 20V, f = 300MHz
$r_b'C_C$		150	ps	I_C= 20mA, V_{CE}= 20V, f = 31.8MHz
N.F.		4	db	I_C= 100 A, V_{CE}= 10V, R_G= 1K , f = 1KHz
T_s		2.5	ns	I_C= 150mA, I_{B1}= 15mA, V_{CC}= 30V, V_{EB}= 0.5V
t_d		10	ns	I_C= 150mA, I_{B1}= 15mA, V_{CC}= 30V, V_{EB}= 0.5V
t_r		25	ns	I_C= 150mA, I_{B1}= 15mA, V_{CC}= 30V, V_{EB}= 0.5V
t_s		225	ns	I_C= 150mA, I_{B1}= I_{B2}= 15mA, V_{CC}= 30V
t_f		60	ns	I_C= 150mA, I_{B1}= I_{B2}= 15mA, V_{CC}= 30V

Note: Pulse width 30 sec, duty cycle 2%.

GENERAL PURPOSE HIGH-VOLTAGE NPN SILICON PLANAR EPITAXIAL TRANSISTORS

- **Low V_{CE} (sat), 0.4 V@ I_C = 150mA**
- **High Frequency, f_T = 250 MHz @ I_C = 20mA**
- **Wide Useful Current Range, 0.1 to 500mA**

The ITT2N2221-22 are NPN silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500 mA. Low saturation voltage and fast switching times make the 2N2221-22 ideal for core driving. The flat gain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		Units
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	30	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	800	mA
Junction Temperature (operating)	-65 to +175	°C
(storage)	-65 to +300	°C
Total Power Dissipation @ T_C = 25°C (derate 12mW/°C above 25°C)	1.8	Watts
Total Power Dissipation @ T_A = 25°C (derate 3.33 mW/°C above 25°C)	0.5	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

Symbol	Min.	Max.	Unit	Conditions
h_{FE} [1]				I_C = 150mA, V_{CE} = 10V
	40	120		2N2221
	100	300		2N2222
				I_C = 150mA, V_{CE} = IV
	20			2N2221
	50			2N2222
				I_C = 500mA, V_{CE} = 10V
	20			2N2221
	30			2N2222

2N2221, 2N2222
SILICON GENERAL PURPOSE TRANSISTORS

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

Symbol	Min.	Max.	Unit	Conditions
h_{FE}				I_C= 10mA, V_{CE}= 10V
	17			
	35			2N2221
	75			2N2222
				I_C= 1mA, V_{CE}= 10V
	12			2N2220
	25			2N2221
	50			2N2222
				I_C= 0.1mA, V_{CE}= 10V
	20			2N2221
	35			2N2222
V_{CE}(sat) [1]		0.4	Vdc	I_C= 150mA, I_B= 15mA
		1.6	Vdc	I_C= 500mA, I_B= 50mA
V_{BE}(sat) [1]		1.3	Vdc	I_C= 150mA, I_B= 15mA
		2.6	Vdc	I_C= 500mA, I_B= 50mA
I_{CBO}		10	nA	V_{CB}= 50V, I_E= 0
		10	A	V_{CB}= 50V, I_E= 0, T = 150°C
I_{EBO}		10	nA	V_{EB}= 3V, I_C= 0
f_T	250		MHz	I_C= 20mA, V_{CE}= 20V
C_{ob}		8	pf	V_{CB}= 10V, I_E= 0
$R_{e(h_{fe})}$ [2]		60	Ohms	I_C= 20mA, V_{CE}= 20V, f = 300 MH:
BV_{CBO}	60		Vdc	I_C= 10 A, I_E= 0
V_{CEO}(sust) [1]	30		Vdc	I_C= 10mA, I_B= 0
BV_{EBO}	5		Vdc	I_E= 10 A, I_C= 0

NOTES: 1. Pulse Measurement: width 300 sec, duty cycle 2%.
2. Real part of Common-Emitter high frequency input impedance.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	75	Volts
Collector-to-Emitter Voltage	40	Volts
Emitter-to-Base Voltage	6	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.8	Watts
P_D @ T_A = 25°C	0.5	Watt

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	75		Vdc	I_C=10μA
LV_{CEO}	40		Vdc	I_C=10mA pulsed
BV_{EBO}	6		Vdc	I_E=10μA
h_{FE}	20			I_C=100μA, V_{CE}=10V
h_{FE}	25			I_C=1mA, V_{CE}=10V
h_{FE}	35			I_C=10mA, V_{CE}=10V
h_{FE}	40	120		I_C=150mA, V_{CE}=10V pulsed
h_{FE}	25			I_C=500mA, V_{CE}=10V pulsed
h_{FE}	20			I_C=150mA, V_{CE}=1V pulsed
h_{FE}	15			I_C=10mA, V_{CE}=10V, T_A=−55°C
V_{CE}(sat)		0.3	Vdc	I_C=150mA, I_B=15mA pulsed
V_{CE}(sat)		1.0	Vdc	I_C=500mA, I_B=50mA pulsed
V_{BE}(sat)	0.6	1.2	Vdc	I_C=150mA, I_B=15mA pulsed
V_{BE}(sat)		2.0	Vdc	I_C=500mA, I_B=50mA pulsed
I_{CBO}		10	nA	V_{CB}=60V
I_{CBO}		10	μA	V_{CB}=60V, T_A=150°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
I_{CEX}		10	nA	$V_{CE}=60V$, $V_{EB}=3V$
I_{EBX}		20	nA	$V_{EB}=3V$, $V_{CB}=60V$
I_{EBO}		10	nA	$V_{EB}=3V$
C_{ob}		8	pF	$V_{CB}=10V$
C_{ib}		25	pF	$V_{EB}=0.5V$
h_{fe}	30	150		$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	50	300		$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	2.5			$I_C=20mA$, $V_{CE}=20V$, f=100MHz
h_{ie}	1	3.5	K ohms	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{ie}	0.2	1.0	K ohms	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{re}		5	$x10^{-4}$	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{re}		2.5	$x10^{-4}$	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	3	15	μmho	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	10	100	μmho	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
$R_{e(hie)}$		60	ohms	$I_C=20mA$, $V_{CE}=20V$, f=300MHz
$r_b'C_C$		150	ps	$I_C=20mA$, $V_{CE}=20V$, f=31.8MHz
τ_s		2.5	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_d		10	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_r		25	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_s		225	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$
t_f		60	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$

NOTES: Pulse width $\leq$ 300 μsec, duty cycle $\leq$ 2%.

ITT SEMICONDUCTORS

2N2222A
SILICON SWITCHING TRANSISTOR

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS	UNITS
CHARACTERISTICS	
Collector-to-Base Voltage 75	Volts
Collector-to-Emitter Voltage 40	Volts
Emitter-to-Base Voltage 6	Volts
Operating Junction Temperature 175	°C
Storage Temperature ..... -65 to +300	°C
P_D @ T_C = 25°C 1.8	Watts
P_D @ T_A = 25°C 0.5	Watt

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

Symbol	Min.	Max.	Unit	Conditions
BV_{CBO}	75		Vdc	I_C = 10 A
LV_{CEO}	40		Vdc	I_C = 10mA pulsed
BV_{EBO}	6		Vdc	I_E = 10 A
h_{FE}	35			I_C = 100 A, V_{CE} = 10V
h_{FE}	50			I_C = 1mA, V_{CE} = 10V
h_{FE}	75			I_C = 10mA, V_{CE} = 10V
h_{FE}	100	120		I_C = 150mA, V_{CE} = 10V pulsed
h_{FE}	40			I_C = 500mA, V_{CE} = 10V pulsed
h_{FE}	50			I_C = 150mA, V_{CE} = 1V pulsed
h_{FE}	35			I_C = 10mA, V_{CE} = 10V, T_A = -55•C
V_{CE} (sat)		0.3	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{CE} (sat)		1.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
V_{BE} (sat)	0.6	1.2	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{BE} (sat)		2.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
I_{CBO}		10	nA	V_{CB} = 60V
I_{CBO}		10	A	V_{CB} = 60V, T_A = 150•C

2N2222A
SILICON SWITCHING TRANSISTOR

ELECTRICAL CHARACTERISTICS continued

Parameter	Min.	Max.	Unit	Conditions
I_{CEX}		10	nA	V_{CE}= 60V, V_{EB}= 3V
I_{EBX}		20	nA	V_{EB}= 3V, V_{CB}= 60V
I_{EBO}		10	nA	V_{EB}= 3V
C_{ob}		8	pF	V_{CB}= 10V
C_{ib}		25	pF	V_{EB}= 0.5V
h_{fe}	50	300		I_C= 1mA, V_{CE}= 10V,f = 1KHz
h_{fe}	75	375		I_C= 10mA, V_{CE}= 10V, f = 1KHz
h_{fe}	2.5			I_C= 20mA, V_{CE}= 20V, f = 100MHz
h_{ie}	2.0	8	Kohms	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{ie}	0.25	1.25	Kohms	I_C= 10mA, V_{CE}= 10V, f = 1KHz
h_{re}		8	x10-4	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{re}		4	x10-4	I_C= 10mA, V_{CE}= 10V, f = 1KHz
h_{oe}	5	35	mho	I_C= 1mA, V_{CE}= 10V, f = 1KHz
h_{oe}	25	200	mho	I_C= 10mA, V_{CE}= 10V, f = 1KHz
$R_{e(hie)}$		60	ohms	I_C= 20mA, V_{CE}= 20V, f = 300MHz
$r_b'C_C$		150	ps	I_C= 20mA, V_{CE}= 20V, f = 31.8MHz
s		2.5	ns	I_C = 150mA, I_{B1} = 15mA, V_{CC} = 30V, V_{EB} = 0.5V
t_d		10	ns	I_C = 150mA, I_{B1} = 15mA, V_{CC} = 30V, V_{EB} = 0.5V
t_r		25	ns	I_C = 150mA, I_{B1} = 15mA, V_{CC} = 30V, V_{EB} = 0.5V
t_s		225	ns	I_C= 150mA, I_{B1}= I_{B2}= 15mA, V_{CC}= 30V
t_f		60	ns	I_C= 150mA, I_{B1}= I_{B2}= 15mA, V_{CC}= 30V

NOTES: Pulse width 300 sec, duty cycle 2%.

HIGH SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTORS

- **High f_T: 650 mHz, typ.**
- **High Gain: 40 min. @ I_C = 10mA**
- **Low C_{ob}: 4pf max. @ V_{CB} = 5V**
- **Low T_{on} = 9 nsec typ.**
- **Low t_{off} = 13 nsec typ.**

The ITT 2N2368 and 2N2369 are NPN silicon planar epitaxial saturated switching transistors for applications at current ranges from 0.1 to 100 mA. High gain and narrow base region provide excellent radiation resistance. They can operate at clock rates above 10MHz for commercial computer applications.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage (shorted base)	40	Volts
Collector-to-Emitter Voltage (open base)	15	Volts
Emitter-to-Base Voltage	4.5	Volts
Collector Current (10 sec. pulse)	500	mA
Junction Temperature (op. and stg.)	-65 to +200	°C
Total Power Dissipation @ T_C = 25C	1.2	Watts
(derate 6.8 mW/°C above 25°C)		
@ T_C = 100°C	0.68	Watts
Total Power Dissipation @ T_A = 25°C	0.36	Watts
(derate 2.06 mW/°C above 25°C)		

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	Min.	Typ.	Max.	Unit	Conditions
h_{FE} [1]					I_C = 10mA, V_{CE} = 1V
	20		60		2N2368
	40		120		2N2369
					I_C = 10mA, V_{CE} = 1V, T = -55°C
	10				2N2368
	20				2N2369
					I_C = 100mA, V_{CE} = 2V
	10				2N2368
	20				2N2369
V_{CE} (sat)		0.2	0.25	Vdc	I_C = 10mA, I_B = 1mA
V_{BE} (sat)	0.7	0.75	0.85	Vdc	I_C = 10mA, I_B = 1mA
I_{CBO}		0.1	0.4	A	V_{CB} = 20V, I_E = 0
		10	30	A	V_{CB} = 20V, I_E = 0, T = 150°C
f_T		650		MHz	V_{CE} = 10V, I_C = 10mA
C_{ob}		2.5	4.0	pf	V_{CB} = 5V, I_E = 0
s [2] (charge storage time)					I_C = I_{B1} 10mA, 10mA, I_{B2} -10mA - 10mA
			10	nsec	2N2368
			13	nsec	2N2369

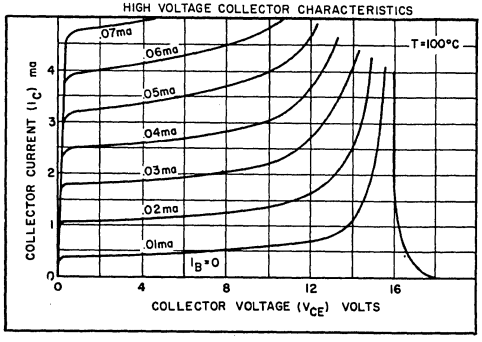
2N2368, 2N2369
SILICON SWITCHING TRANSISTORS

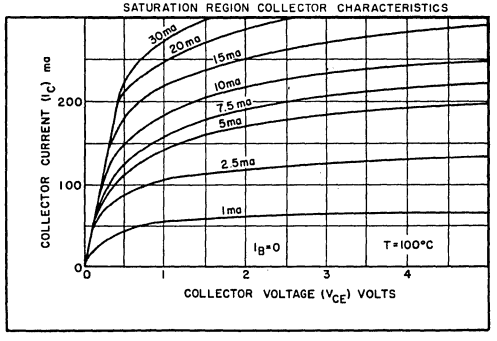
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted. **(continued)**

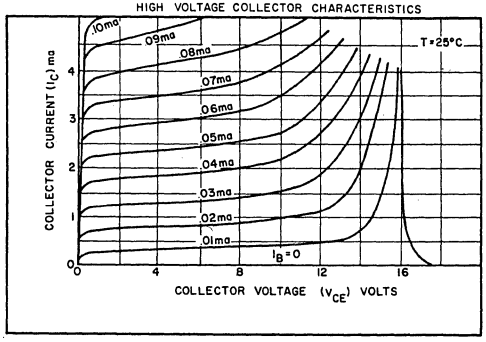
Symbol	Min.	Typ.	Max.	Unit	Conditions
t_{on} [2]		9.0	12	nsec	I_C 10mA, I_{B1} 3mA
t_{off} [2]					I_C 10mA, I_{B1} 3mA, I_{B2} -1.5mA
		10	15	nsec	2N2368
		13	18	nsec	2N2369
BV_{CBO}	40			Vdc	I_C= 10 A, I_E= 0
BV_{CES}	40			Vdc	I_C= 10 A, I_B= 0
V_{CEO} (sust)	15			Vdc	I_C=10mA, I_B= 0
BV_{EBO}	4.5			Vdc	I_E= 10 A, I_C= 0

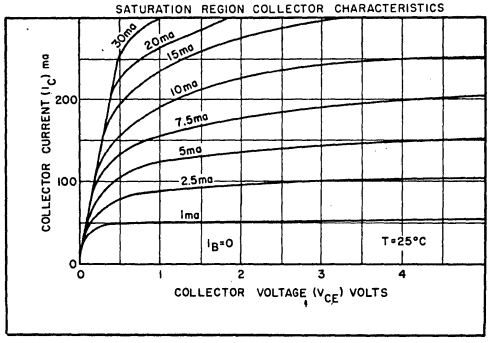
NOTES: 1. Pulse measurement: width 300 sec, duty cycle 2%.
2. Pulse switching circuits for exact IC, IB1, and IB2.

TYPICAL CHARACTERISTICS[1]



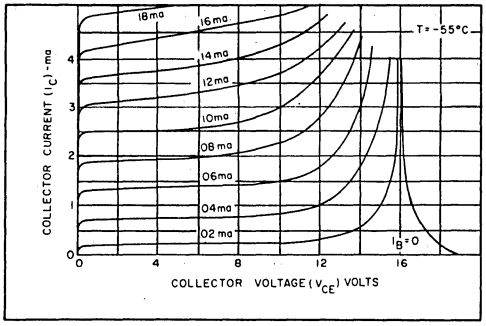




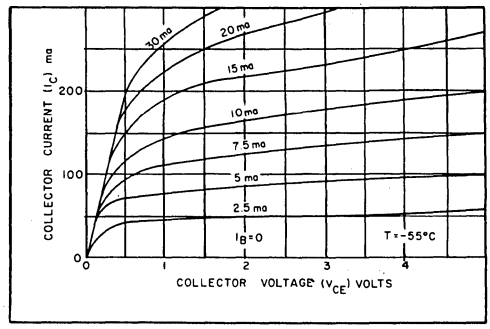


TYPICAL CHARACTERISTICS, continued

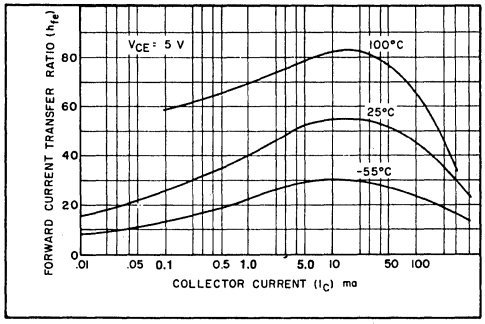
HIGH VOLTAGE COLLECTOR CHARACTERISTICS



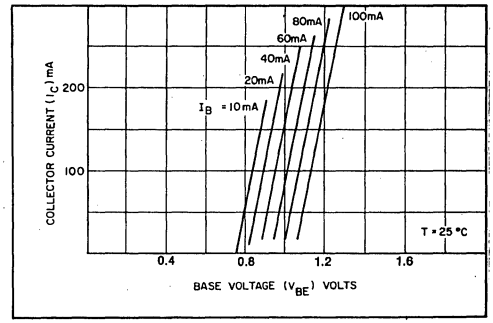
SATURATION REGION COLLECTOR CHARACTERISTICS



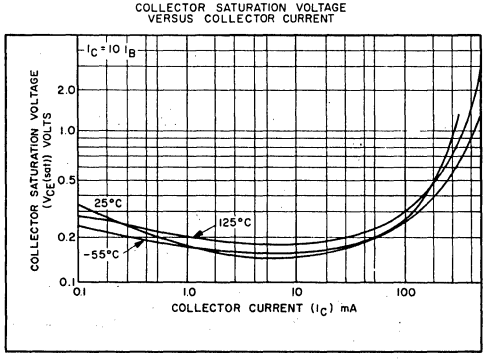
PULSE DC CURRENT GAIN VS COLLECTOR CURRENT



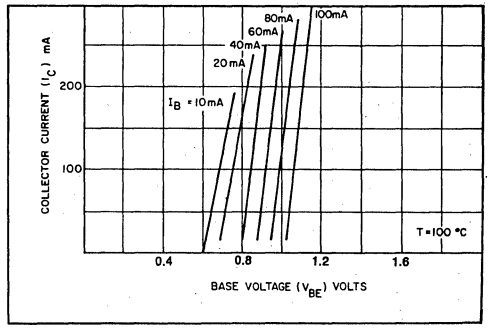
SATURATION REGION BASE CHARACTERISTICS



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

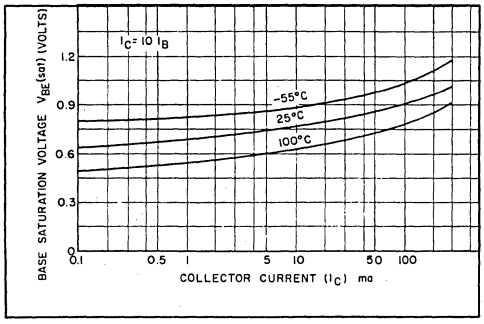


SATURATION REGION BASE CHARACTERISTICS

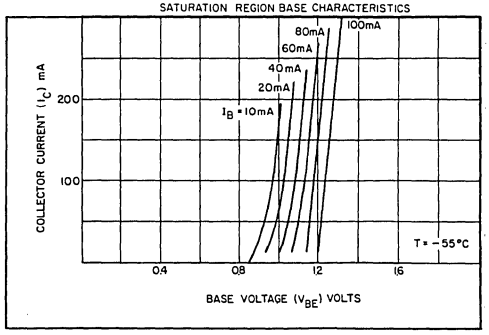


TYPICAL CHARACTERISTICS, continued

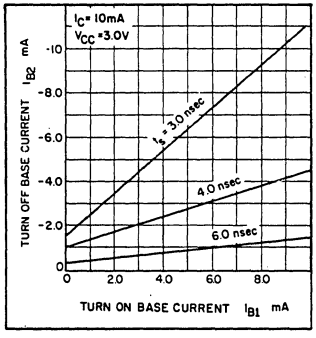
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



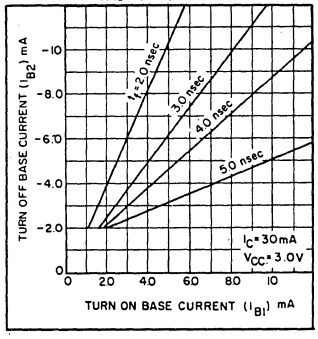
SATURATION REGION BASE CHARACTERISTICS



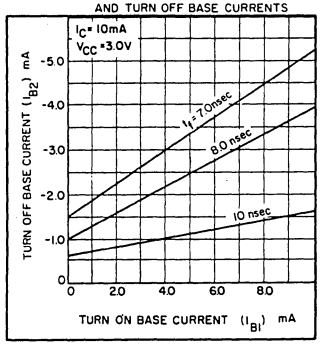
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



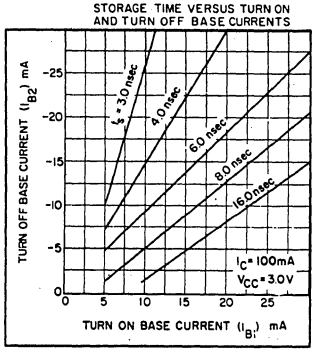
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



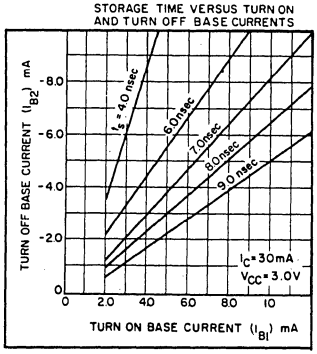
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



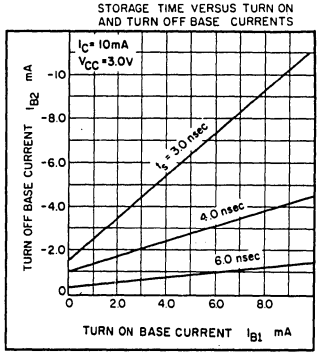
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

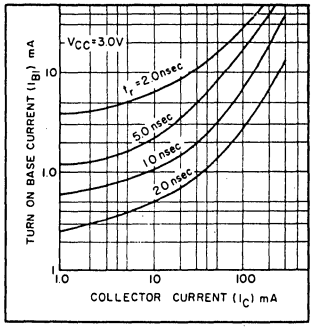


STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

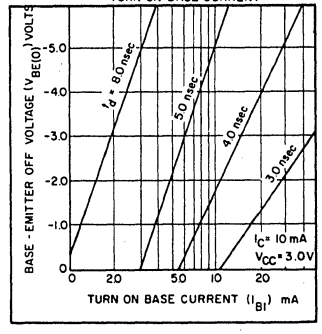


TYPICAL CHARACTERISTICS, continued

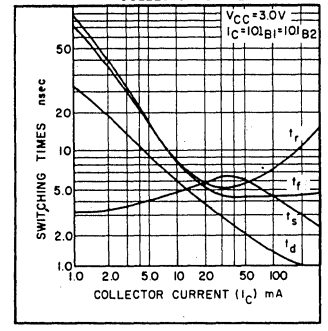
RISE TIME VERSUS TURN ON BASE CURRENT AND COLLECTOR CURRENT



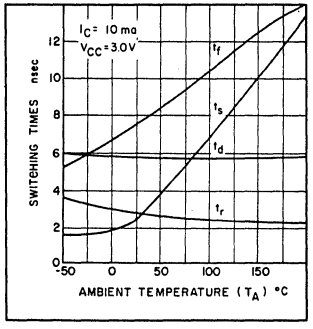
DELAY TIME VERSUS BASE-EMITTER OFF VOLTAGE AND TURN ON BASE CURRENT



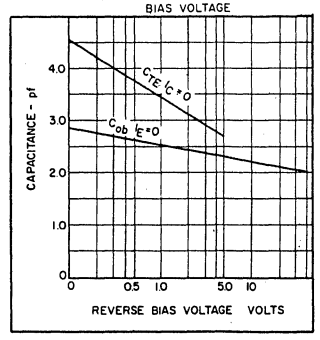
SWITCHING TIMES VERSUS COLLECTOR CURRENT



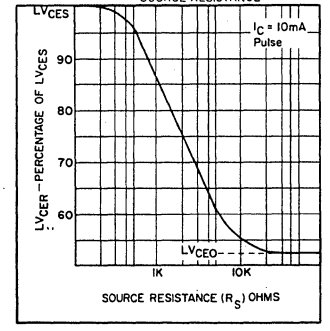
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



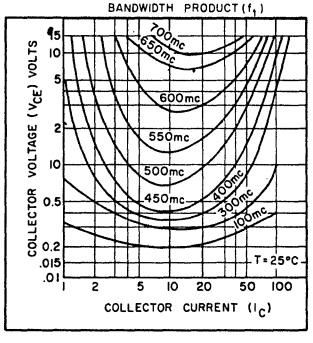
EMITTER TRANSITION AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



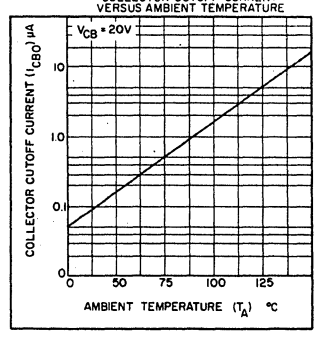
LOWER LIMITING VOLTAGE VERSUS SOURCE RESISTANCE



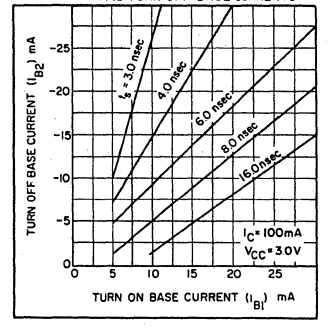
CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_t)



COLLECTOR CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE



STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



HIGH SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

- **High f_T: 675 MHz, typ.**
- **High Gain: 40 min. @ I_C = 10 mA**
- **Low C_{ob}: 4 pf max. @ V_{CB} = 5V**
- **Low t_{on}: 9 nsec typ.;**
- **Low t_{off}: 13 nsec typ.**

The ITT 2N2369A is a NPN silicon planar epitaxial saturated switching transistor for applications at current ranges from 0.1 to 100 mA. High gain and narrow base region provide excellent radiation resistance. The 2N2369A can operate at clock rates above 10 MHz for commercial computer applications.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage (shorted base)	40	Volts
Collector-to-Emitter Voltage (open base)	15	Volts
Emitter-to-Base Voltage	4.5	Volts
Collector Current (continuous)	200	mA
Collector Current (10 sec pulse)	500	mA
Junction Temperature (op. and stg.)	-65 to +200	°C
Total Power Dissipation @ T_C = 25°C (derate 6.8 mW/°C above 25°C)	1.2	Watts
@T_C = 100°C	0.68	Watts
Total Power Dissipation @ T_A = 25°C (derate 2.06 mW/°C above 25°C)	0.36	Watts

ELECTRICAL CHARACTERISTICS @ T_A = 25°C unless otherwise noted

Symbol	Min.	Typ.	Max.	Unit	Conditions
h_{FE1}	40	66	120		I_C = 10mA, V_{CE} = 1V
	40	63	120		I_C = 10mA, V_{CE} = 0.35V
	20	50			I_C = 10mA, V_{CE} = 0.35V, T = -55°C
	30	71			I_C = 30mA, V_{CE} = 0.4V
	20				I_C = 100mA. V_{CE} = 1V
V_{CE} (sat)		0.14	0.2	Vdc	I_C = 10mA, I_B = 1mA
		0.19	0.3	Vdc	I_C = 10mA, I_B = 1mA, T = 125°C
		0.17	0.25	Vdc	I_C = 30mA, I_B = 3mA
		0.28	0.5	Vdc	I_C = 100mA, I_B = 10mA

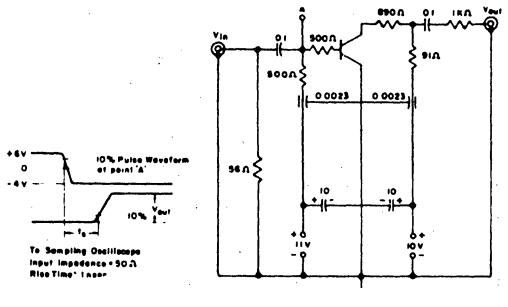
2N2369A
SILICON SWITCHING TRANSISTOR

ELECTRICAL CHARACTERISTICS @ T_A = 25°C unless otherwise noted **(continued)**

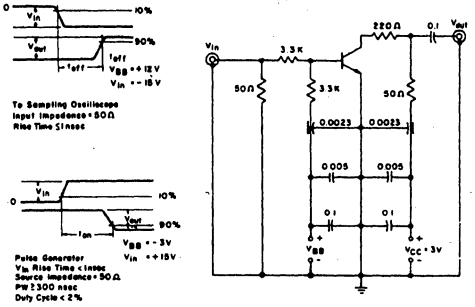
Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{BE} (sat)	0.7	0.8	0.85	Vdc	I_C= 10mA, I_B= 1mA
	0.59		1.02	Vdc	I_C= 10mA, I_C= 1mA, T = -65 to +125•C
		0.9	1.15	Vdc	I_C= 30mA, I_B= 3mA
		1.1	1.6	Vdc	I_C= 100mA, I_B= 10mA
I_{CES}		0.05	0.4	A	V_{CE}= 20V, V_{BE}= 0
I_{CBO}		10	30	A	V_{CB}= 20V, I_E= 0, T = 150°C
f_T	500	675		MHz	V_{CE}= 10V, I_C= 10mA
C_{ob}		2.3	4.0	pf	V_{CB}= 5V, I_E= o
τ_s (charge storage time)		6.0	13	nsec	I_C= I_{B1} 10mA, I_{B2}= -10mA
t_{on}		9.0	12	nsec	I_C 10mA I_{B1} 3mA
t_{off}		13	18	nsec	I_C 10mA I_{B1} 3mA I_{B2} -1.5mA
BV_{CBO}	40			Vdc	I_C= 10 A, I_E= 0
BV_{CES}	40			Vdc	I_C= 10 A, V_{BE}= 0
V_{CEO} (sust) 1,2	15			Vdc	I_C= 10mA, I_B= 0
BV_{EBO}	4.5			Vdc	I_E= 10 A, I_C= 0

NOTES: 1. Pulse measurement: width 300 sec, duty cycle 2%.
2.Rating refers to a high-current point where collector-to-emitter voltage is lowest.

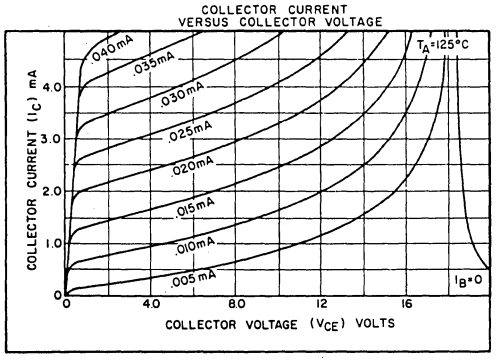
CHARGE STORAGE TIME MEASUREMENT CIRCUIT

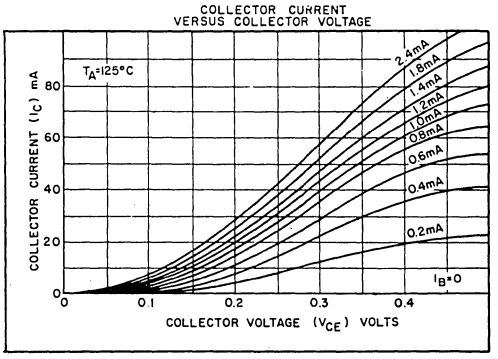


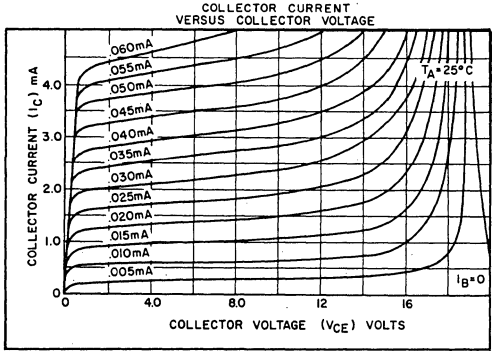
t_{ON} t_{OFF} MEASUREMENT CIRCUIT

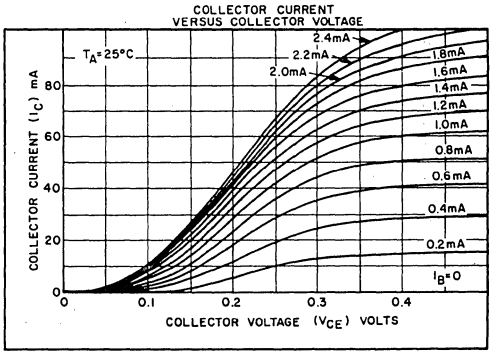


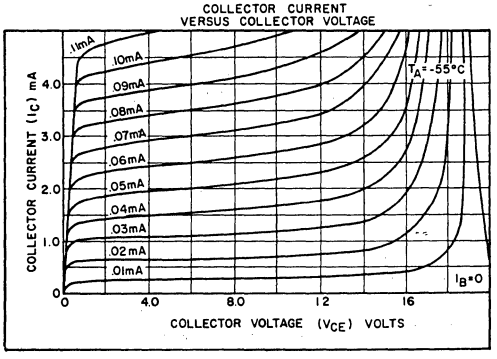
TYPICAL COLLECTOR CHARACTERISTICS[1]

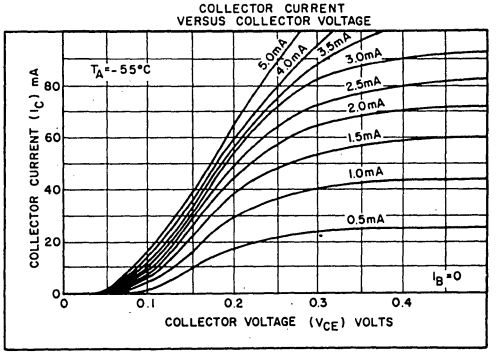






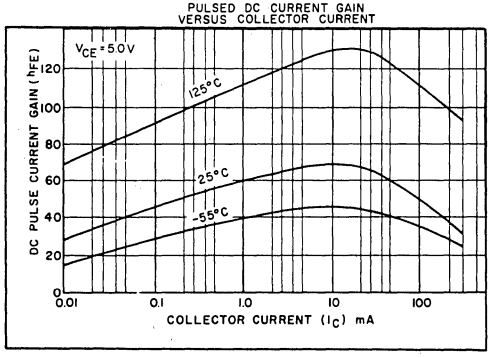


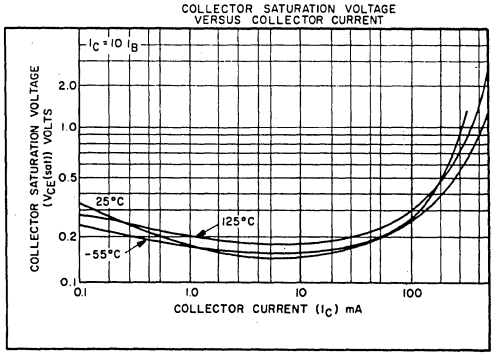




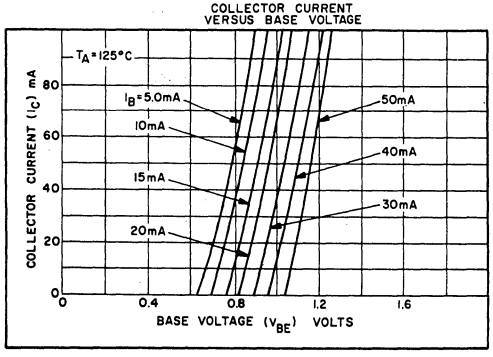
NOTE: Single family characteristics on Transistor Curve Tracer

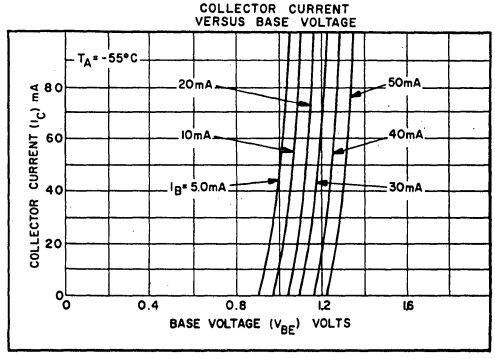
TYPICAL COLLECTOR CHARACTERISTICS, continued

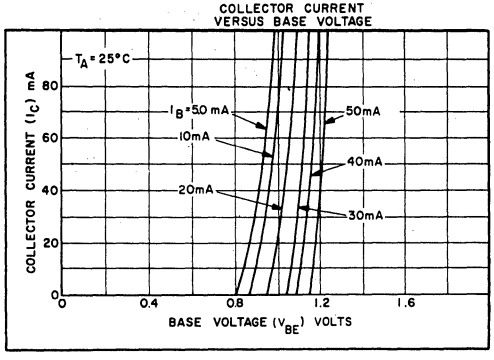


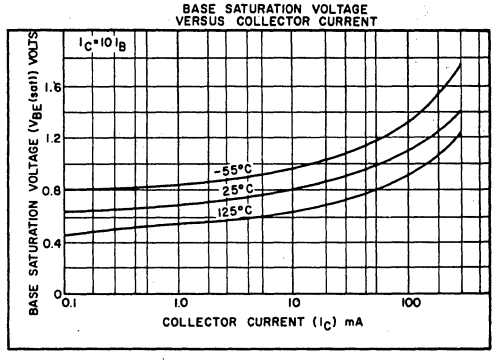


TYPICAL BASE CHARACTERISTICS[1]



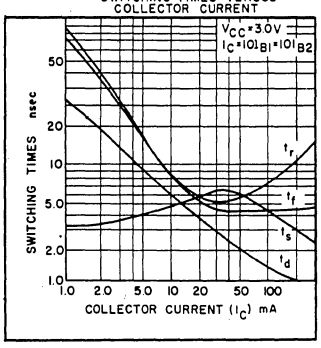




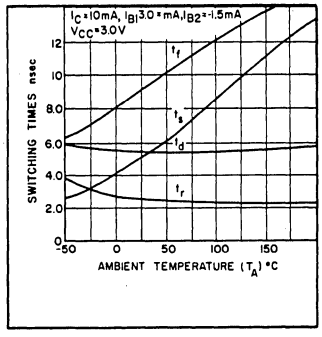


TYPICAL ELECTRICAL CHARACTERISTICS

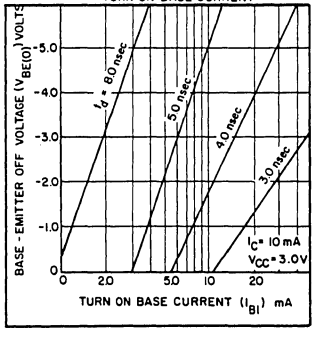
SWITCHING TIMES VERSUS COLLECTOR CURRENT



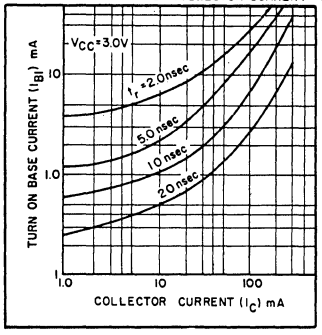
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



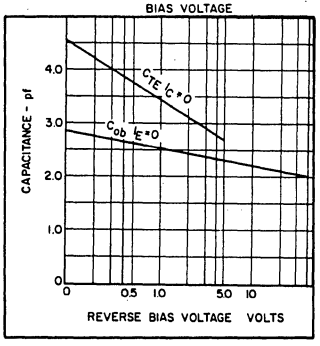
DELAY TIME VERSUS BASE-EMITTER OFF VOLTAGE AND TURN ON BASE CURRENT



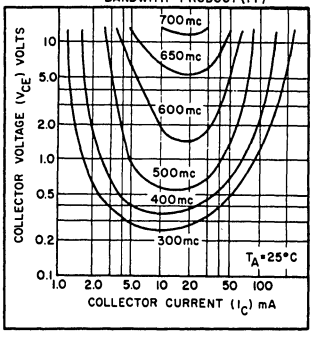
RISE TIME VERSUS TURN ON BASE CURRENT AND COLLECTOR CURRENT



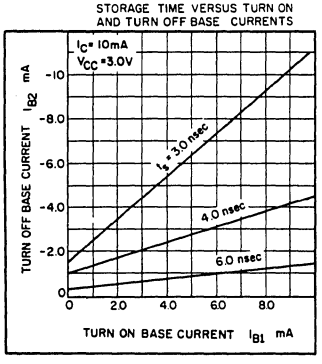
EMITTER TRANSITION AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



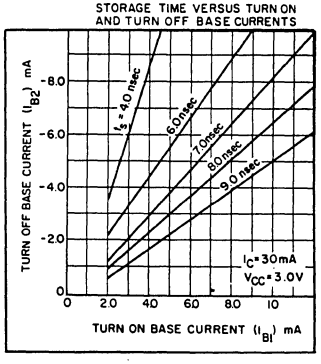
CONTOURS OF CONSTANT GAIN BANDWITH PRODUCT (f_T)



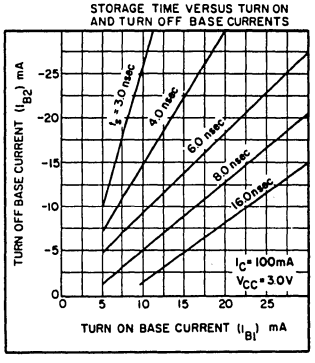
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



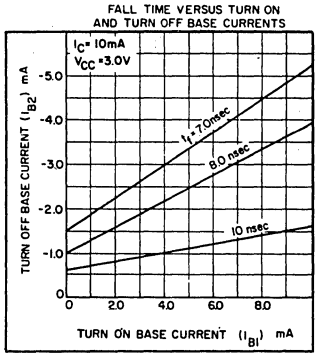
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

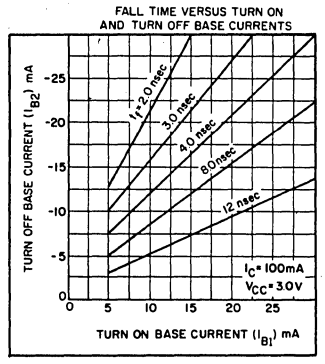


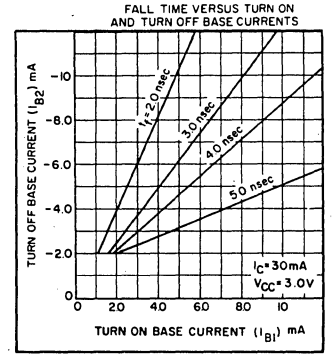
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

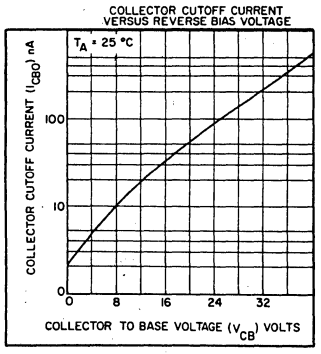


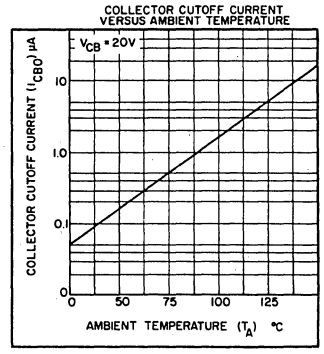
TYPICAL CHARACTERISTICS, continued

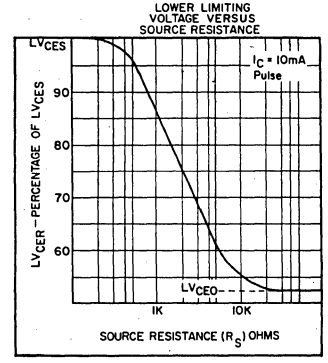












ITT SEMICONDUCTORS

2N2480, 2N2480A

NPN SILICON DUAL TRANSISTORS

Package: TO-92

ABSOLUTE MAXIMUM RATINGS (each side)

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage (2N2480)	75 Volts
Collector-Base Voltage (2N2480A)	80 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	500 mA
Operating Junction Temperature	200°C
Storage Temperature Range	−65 to +200°C
Total Dissipation @ T_A = 25°C (one side)	0.5 Watt
Derate above 25°C	2.86 mW/°C
Total Dissipation @ T_C = 25°C	1.6 Watts
Derate above 25°C	9.1 mW/°C
Total Dissipation @ T_A = 25°C (both sides)	0.6 Watt
Derate above 25°C	3.43 mW/°C
Total Dissipation @ T_C = 25°C	3.0 Watts
Derate above 25°C	17.2 mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	40	–	Volts	I_C = 20 mA, I_B = 0*
BV_{CBO}	75	–	Volts	(2N2480) I_C = 100 μA, I_E = 0
	80	–	Volts	(2N2480A)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0
I_{CBO}	–	15	μA	V_{CB} = 30 Volts, I_E = 0, T_A = 150°C
	–	0.050	μA	(2N2480) V_{CB} = 60 Volts, I_E = 0
	–	0.020	μA	(2N2480A)
I_{EBO}	–	50	nA	(2N2480) V_{BE} = 5.0 Volts, I_C = 0
	–	20	nA	(2N2480A)
h_{FE}	20	–	–	(2N2480) I_C = 100 μA, V_{CE} = 5.0 Volts
	35	–	–	(2N2480A)
h_{FE}	30	350	–	(2N2480) I_C = 1.0 mA, V_{CE} = 5.0 Volts
	50	200	–	(2N2480A)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CE(sat)}$	–	1.2	Volts	(2N2480) I_C = 50 mA, I_B = 5.0 mA
	–	1.3	Volts	(2N2480A)
$V_{BE(sat)}$	–	0.9	Volt	(2N2480) I_C = 50 mA, I_B = 5.0 mA
	–	1.0	Volt	(2N2480A)
f_T	50	–	MHz	I_C = 50 mA, V_{CE} = 10 Volts, f = 20 MHz
C_{ob}	–	20	pF	(2N2480) V_{CB} = 10 Volts, I_E = 0
	–	18	pF	(2N2480A) f = 1.0 MHz
C_{ib}	–	85	pF	(2N2480A) V_{BE} = 0.5 Volt, I_C = 0, f = 1.0 MHz
h_{ie}	1000	5000	ohms	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
h_{ib}	20	35	ohms	(2N2480A) I_C = 1.0 mA, V_{CB} = 5.0 Volts, f = 1.0 kHz
h_{fe}	50	300	–	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
h_{oe}	4.0	16	umhos	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
NF	–	8.0	dB	I_C = 0.3 mA, V_{CE} = 10 Volts, R_S = 510 ohms, f = 1.0 kHz, BW = 1.0 Hz

* Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2%.

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 100 Min. @ I_C = 10μA (2N2484)**
- **Low noise; 3dB Max. @ I_C = 10μA**
- **High V_{CEO};60 Vdc Min.**

The ITT 2N2483 and 2N2484 are NPN silicon planar transistors designed for application in low-noise, low-level, high-gain amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	60	Volts
Emitter-to-Base Voltage	6	Volts
Collector Current	50	mA
Junction Temperature (op. and stg.)	-65 to +200	°C
Total Power Dissipation @ T_C = 25°C	1.2	Watts
(derate 6.9 mW/°C above 25°C)		
@ T_C = 100°C	0.68	Watts
Total Power Dissipation @ T_A = 25°C	0.36	Watts
(derate 2.1 mW/°C above 25°C)		

ELECTRICIAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	2N2483 Min.	2N2483 Typ.	2N2483 Max.	2N2484 Min.	2N2484 Typ.	2N2484 Max.	Unit	Conditions
BV_{CBO}	60			60			Vdc	I_C= 10μA
LV_{CEO} [1,2]	60			60			Vdc	I_C= 10mA
BV_{EBO}	6.0			6.0			Vdc	I_C= 10μA
h_{FE}				30	200			I_C= 1μA, V_{CE}= 5V
	40	80	120	100	290	500		I_C= 10μA, V_{CE}= 5V
	75	140		175	375			I_C= 100μA, V_{CE}= 5V
	100	200		200	430			I_C= 500μA, V_{CE}= 5V
	175	230		250	450			I_C= 1mA, V_{CE}= 5V
		280	500		430	800		I_C= 10mA, V_{CE}= 5V
	10			20				I_C= 10μA, V_{CE}= 5V, T_A= -55°C
V_{CE} (sat)		0.2	0.35		0.2	0.35	Vdc	I_C= 1mA, I_B= 0.1mA
V_{BE} (on)	0.5	0.57	0.7	0.5	0.57	0.7	Vdc	I_C= 100μA, V_{CE}= 5V
I_{CBO}		0.1	10		0.1	10	nA	V_{CB}= 45V
		0.2	10		0.2	10	A	V_{CB}= 45V, T_A= 150°C
I_{CEO}		0.1	2.0		0.1	2.0	nA	V_{CE}= 5V
I_{EBO}		0.1	10		0.1	10	nA	V_{EB}= 5V
C_{ob}		3.5	6.0		3.5	6.0	pF	V_{CB}= 5V, f = 1mHz

2N2483, 2N2484
SILICON GENERAL PURPOSE TRANSISTORS

ELECTRICIAL CHARACTERISTICS @ 25°C unless otherwise noted. **(continued)**

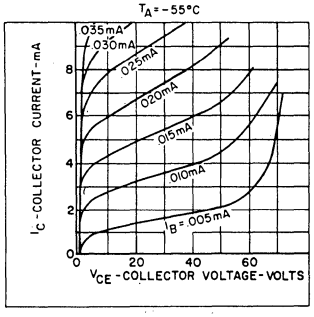
Symbol	2N2483 Min.	2N2483 Typ.	2N2483 Max.	2N2484 Min.	2N2484 Typ.	2N2484 Max.	Unit	Conditions
Cib		3.5	6.0		3.5	6.0	pF	V_{EB}= 0.5V, f = 1mHz
hfe	2.4	4.0		3.0	4.0			I_C= 50µA, V_{CE}= 5V, f = 5mHz
	2.0	2.3		2.0	2.6			I_C= 500µA, V_{CE}= 5V, f = 30mHz
	80	280	450	150	400	900		I_C= 1mA, V_{CE}= 5V, 5 = 1KHz
hie	1.5	7.5	13	3.5	15	24	Kohms	I_C= 1mA, V_{CE}= 5V, f = 1KHz
hre		300	800		425	800	X10 -6	I_C= 1mA, V_{CE}= 5V, f = 1KHz
hib	25	27	32	25	27	32	ohms	I_C= 1mA, V_{CE}= 5V, f = 1KHz
NF		1.9	4.0		1.8	3.0	dB	I_C= 10µA, V_{CE}= 5V, R_G= 10KΩ B.W. = 15.7KHz 3dB @ 10Hz & 10KHz
		1.9	4.0		1.8	3.0	dB	I_C= 10µA, V_{CE}= 5V, R_G= 10KΩ f = 1KHz, B.W. = 200Hz (Note 3)
		0.7	3.0		0.6	2.0	dB	I_C= 10µA, V_{CE}= 5V, R_G= 10KΩ f = 10KHz, B.W. = 2KHz (Note 3)
		4.0	15		4.0	10	dB	I_C= 10µA, V_{CE}= 5V, R_G= 10KΩ f = 100Hz, B.W. = 20Hz (Note 3)

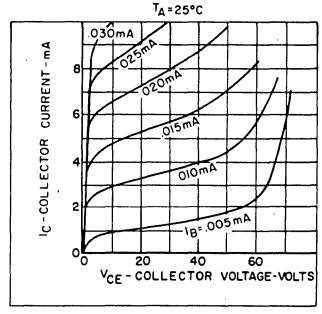
Notes: 1. Pulsed width 300 sec; duty cycle 2%.
2. Lowest emitter to collector voltage.
3. Narrow band noise.

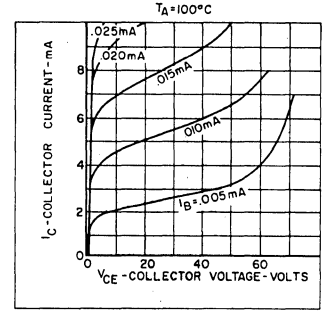
TYPICAL CHARACTERISTICS

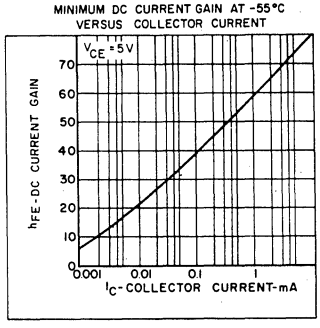
2N2483

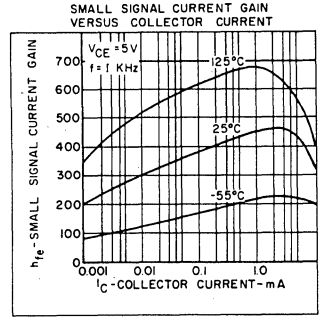
COLLECTOR CHARACTERISTICS

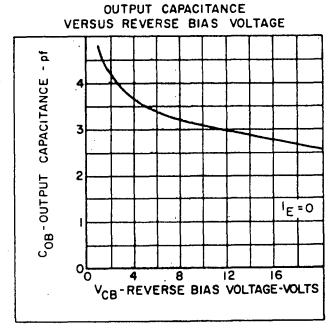








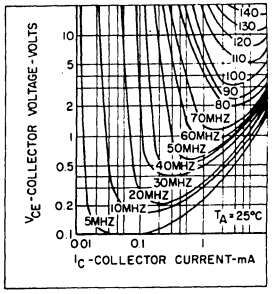




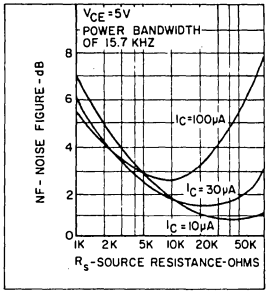
TYPICAL CHARACTERISTICS

2N2483
COLLECTOR CHARACTERISTICS (continued)

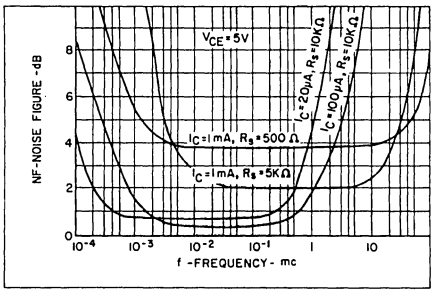
CONTOURS OF CONSTANT TRANSITION FREQUENCY



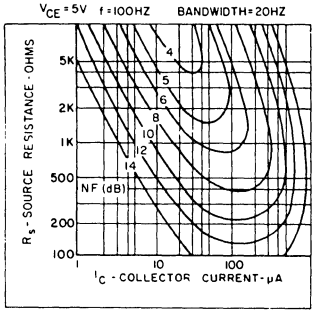
AVERAGE NOISE FIGURE VERSUS SOURCE RESISTANCE

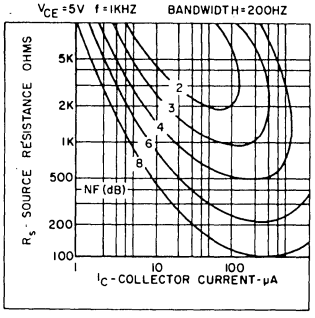


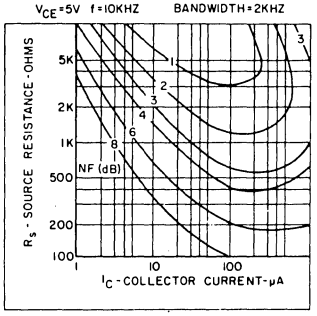
SPOT NOISE FIGURE VERSUS FREQUENCY

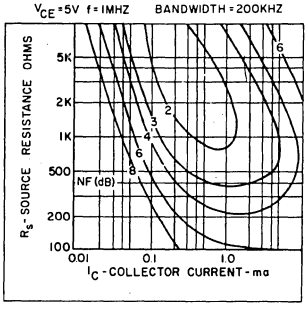


2N2483
CONSTANT NOISE FIGURE CONTOURS





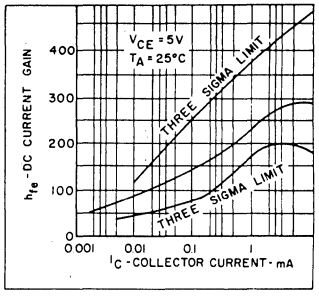




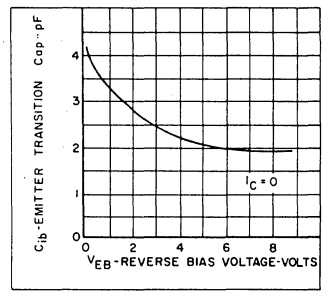
TYPICAL CHARACTERISTICS

2N2483
NORMALIZED COMMON EMITTER TRANSFER CHARACTERISTICS

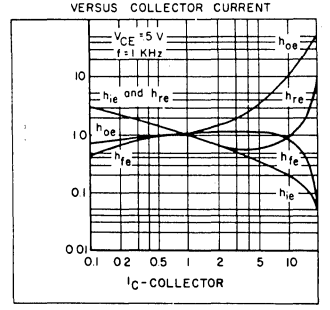
PULSED DC CURRENT GAIN VERSUS COLLECTOR CURRENT



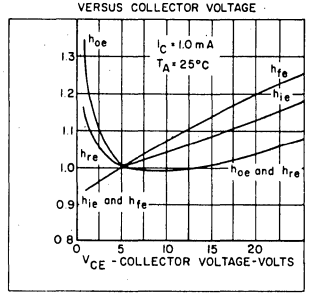
EMITTER TRANSITION CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



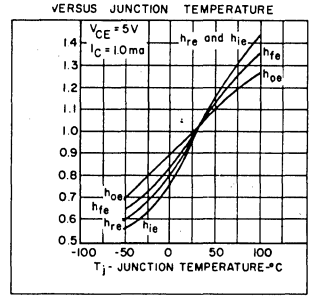
VERSUS COLLECTOR CURRENT



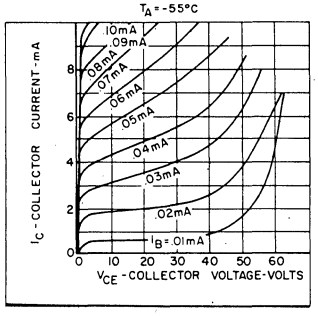
VERSUS COLLECTOR VOLTAGE

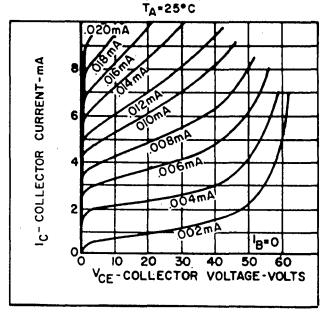


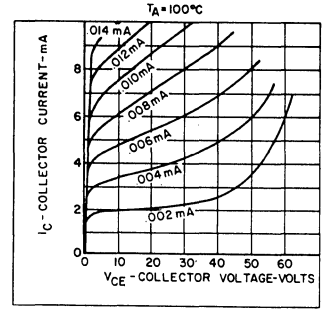
VERSUS JUNCTION TEMPERATURE



2N2484
COLLECTOR CHARACTERISTICS





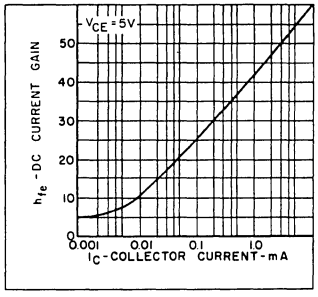


TYPICAL CHARACTERISTICS

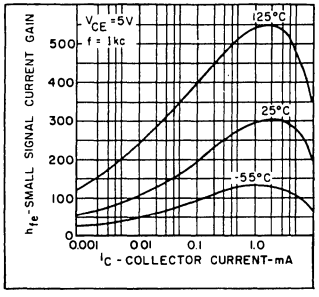
2N2484

COLLECTOR CHARACTERISTICS (continued)

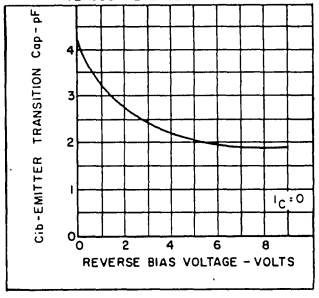
MINIMUM DC CURRENT GAIN AT -55°C VERSUS COLLECTOR CURRENT



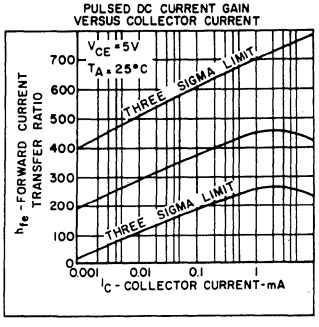
SMALL SIGNAL CURRENT GAIN VERSUS COLLECTOR CURRENT



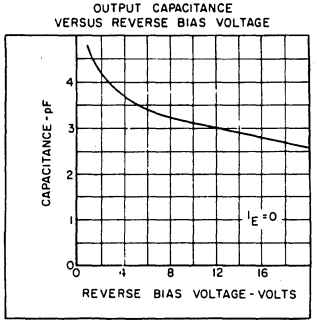
EMITTER TRANSITION CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



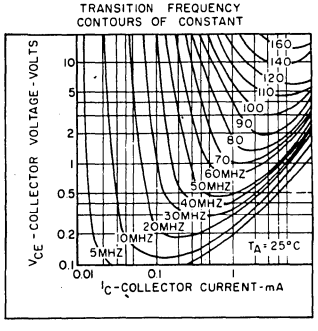
PULSED DC CURRENT GAIN VERSUS COLLECTOR CURRENT



OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE

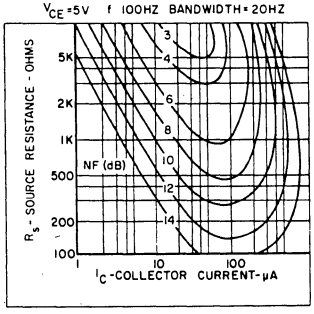


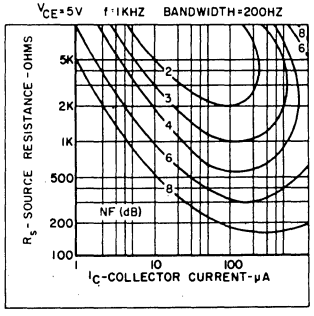
TRANSITION FREQUENCY CONTOURS OF CONSTANT

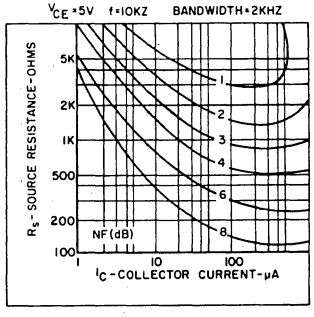


2N2484

CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE

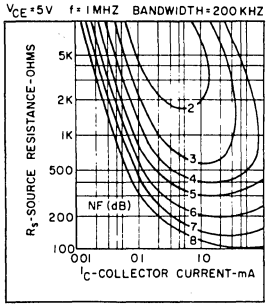




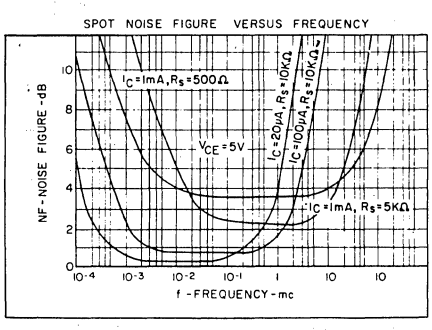


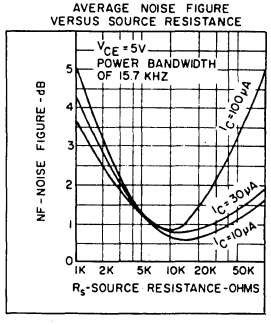
TYPICAL CHARACTERISTICS

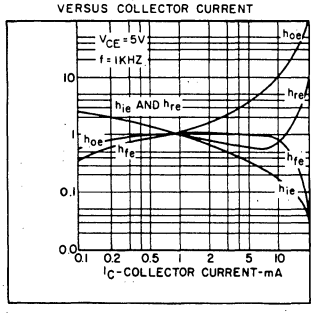
2N2484
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE (continued)

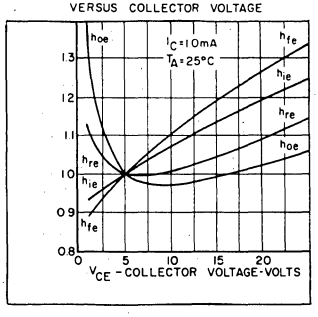


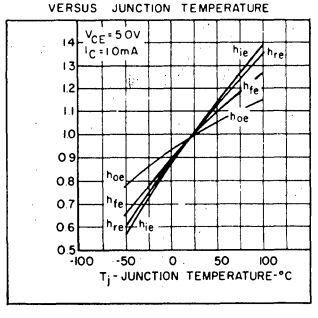
2N2484
NORMALIZED COMMON EMITTER TRANSFER CHARACTERISTICS











ITT SEMICONDUCTORS

2N2904A, 2N2905A, 2N2906A, 2N2907A
SILICON GENERAL PURPOSE TRANSISTORS

GENERAL PURPOSE PNP SILICON PLANAR EPITAXIAL TRANSISTORS

The ITT 2N2904A-7A are PNP silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500mA. Low saturation voltage and fast switching times make the 2N2904A, 5A ideal for core driving. The flat gain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits. Designed to complement the ITT 2N2217 thru 2N2222 NPN types.

- **High Voltage: -60V min.**
- **Low V_{CE} (sat): 0.4V @ 150mA**
- **h_{FE} guaranteed from 100 A to 500mA**

ABSOLUTE MAXIMUM RATINGS

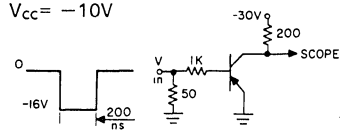
CHARACTERISTICS	2N2905A	2N2904A 2N2907A	UNITS
Collector-to-Base Voltage	-60	-60	Volts
Collector-to-Emitter Voltage (open base)	-60	-60	Volts
Emitter-to-Base Voltage	-5	-5	Volts
Collector Current (continuous)	600	600	mA
Junction Temperature (storage)	-65 to 200		°C
Total Power Dissipation @ T_C = 25°C	3.0	1.8	Watts
Derating factor above 25°C	17.3	10.3	mW/°C
Total Power Dissipation @ T_A = 25°C	0.6	0.4	Watts
Derating factor above 25°C	3.43	2.28	mW/°C

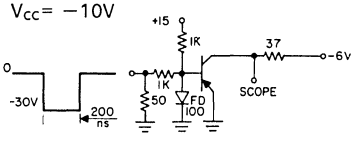
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	2N2904A 2N2906A MIN.	2N2904A 2N2906A MAX.	2N2905A 2N2907A MIN.	2N2905A 2N2907A MAX.	UNIT	CONDITIONS	
BV_{CBO}	−60		−60		Vdc	I_C = −10μA	
LV_{CEO}[1,2]	−60		−60		Vdc	I_C = −10mA	
BV_{EBO}	−5		−5		Vdc	I_E = −10μA	
h_{FE}[1]	40		75			I_C = −100μA	V_{CE} = −10V
	40		100			I_C = −1mA	V_{CE} = −10V
	40		100			I_C = −10mA	V_{CE} = −10V
	40	120	100	300		I_C = −150mA	V_{CE} = −10V
	40		50			I_C = −500mA	V_{CE} = −10V
V_{CE}(sat)[1]		−0.4		−0.4	Vdc	I_C = −150mA	I_B = −15mA
		−1.6		−1.6	Vdc	I_C = −500mA	I_B = −50mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted. **(continued)**

SYMBOL	2N2904A 2N2906A MIN.	MAX.	2N2905A 2N2907A MIN.	MAX.	UNIT	CONDITIONS
$V_{BE}(sat)$[1]		−1.3 −2.6		−1.3 −2.6	Vdc Vdc	I_C= −150mA I_B= −15mA I_C= −500mA I_B= −50mA
I_{CBO}		10		10	nA	V_{CB}= −50V
		10		10	μA	V_{CB}= −50V T_A=150°C
I_{CEX}		50		50	nA	V_{CE}= −30V V_{BE}=0.5V
I_B		50		50	nA	V_{CE}= −30V V_{BE}=0.5V
C_{ob}		8		8	pF	V_{CB}= −10V f=100KHz
C_{ib}		30		30	pF	V_{EB}= −2V f=100KHz
h_{fe}	2		2			I_C= −50mA V_{CE}= −20V f=100MHz
t_d		10		10	ns	I_C= −150mA I_{B1}= −15mA V_{CC}= −10V
t_r		40		40	ns	
t_s				80	ns	I_C= −150mA $I_{B1}=I_{B2}$ =15mA V_{CC}= −10V
t_f				30	ns	





Notes: 1. Pulsed width ≤ 300 μsec; duty cycle ≤ 2%.
2. Lowest emitter to collector voltage.

ITT SEMICONDUCTORS

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

Package: TO-18

The ITT 2N3011 is an NPN silicon planar eptiaxial transistor designed specifically for high-speed saturated switching applications in the 50-100 mc range at current levels from 100 microamperes to 100 milliamperes. It is suitable for most small-signal, RF, and digital type circuits.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	30 Volts
Collector-Emitter Voltage	30 Volts
Collector-Emitter Voltage (Note 4)	12 Volts
Emitter-Base Voltage	5.0 Volts
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300μsec; duty cycle = 1%.

(6) See switching circuits for exact values of I_C, I_{B1}, and I_{B2}.

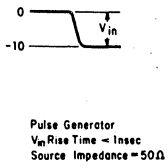
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	30	70	120	–	I_C = 10 mA, V_{CE} = 0.35 Volt (Note 5)
h_{FE}	25	75	–	–	I_C = 30 mA, V_{CE} = 0.4 Volt (Note 5)
h_{FE}	12	50	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (Note 5)
$V_{CE(sat)}$	–	0.17	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.18	0.25	Volt	I_C = 30 mA, I_B = 3.0 mA
$V_{CE(sat)}$	–	0.15	0.3	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.3	0.5	Volt	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	0.72	0.8	0.87	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$	–	0.9	1.15	Volts	I_C = 30 mA, I_B = 3.0 mA
$V_{BE(sat)}$	–	1.1	1.6	Volts	I_C = 100 mA, I_B = 10 mA
h_{fe}	4.0	6.5	–	–	I_C = 20 mA, V_{CE} = 10 Volts
C_{ob}	–	2.3	4.0	pf	I_E = 0, V_{CB} = 5.0 Volts

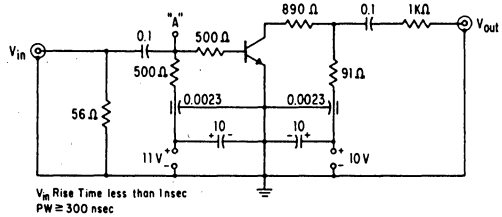
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

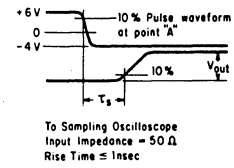
Symbol	Min	Typ	Max	Unit	Conditions
I_{CES}	–	0.05	0.4	μA	V_{CE} = 20 Volts, V_{BE} = 0
I_{CES}(85°C)	–	1.0	10	μA	V_{CE} = 20 Volts, V_{BE} = 0
BV_{CBO}	30	–	–	Volts	I_C = 10 μA, I_E = 0
BV_{CES}	30	–	–	Volts	I_C = 10 μA, V_{EB} = 0
$V_{CEO(sust)}$	12	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0
BV_{EBO}	5.0	–	–	Volts	I_E = 100 μA, I_C = 0
τ_S	–	–	13	nsec	$I_C = I_{B1} \approx$ 10 mA, $I_{B2} \approx -10$ mA (Note 6)
t_{on}	–	–	15	nsec	$I_C \approx$ 30 mA, $I_{B1} \approx$ 3.0 mA (Note 6)
t_{off}	–	–	20	nsec	$I_C \approx$ 30 mA, $I_{B1} \approx$ 3.0 mA, $I_{B2} \approx -3.0$ mA (Note 6)

SCHEMATIC

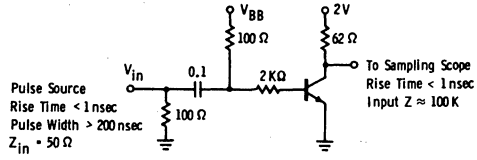


CHARGE STORAGE TIME — CONSTANT TEST CIRCUIT





t_{on}-t_{off} MEASUREMENT CIRCUIT



T_{on}: V_{CC} = 2V
V_{BB} Grounded
V_{in} = 7V

T_{off}: V_{CC} = 2V
V_{BB} = 7V
V_{in} = -13V

ITT SEMICONDUCTORS

NPN SILICON SWITCHING AND AMPLIFIER TRANSISTOR

Package: TO-5

NPN SILICON SWITCHING AND AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	60 Volts
Emitter-Base Voltage	5 Volts
Collector Current — Continuous	700 mA
Total Device Dissipation @ T_C = 25°C	5 Watts
Derate above 25°C	28.6 mW/°C
Operating Junction Temperature Range	200 °C
Storage Temperature Range	−65 to +200 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Volts	I_C = 100 μA, I_E = 0
BV_{CER}	50	–	Volts	I_C = 100 mA, R_{BE} = 10 ohms
BV_{CBO}	60	–	Volts	I_C = 100 μA, I_E = 0
BV_{EBO}	5	–	Volts	I_E = 100 μA, I_C = 0
I_{CEX}	–	0.25	μA	V_{CE} = 60 Volts, $V_{EB(off)}$ = 1.5 Volts
I_{BL}	–	0.25	μA	V_{CE} = 60 Volts, $V_{EB(off)}$ = 1.5 Volts
h_{FE}	25	–	–	I_C = 150 mA, V_{CE} = 2.5 Volts
h_{FE}	50	250	–	I_C = 150 mA, V_{CE} = 10 Volts*
$V_{CE(sat)}$	–	1.4	Volts	I_C = 150 mA, I_B = 15 mA
$V_{BE(sat)}$	–	1.7	Volts	I_C = 150 mA, I_B = 15 mA
$V_{BE(on)}$	–	1.7	Volts	I_C = 150 mA, V_{CE} = 2.5 Volts
f_T	100	–	MHz	I_C = 50 mA, V_{CE} = 10 Volts, f = 20 MHz
C_{ob}	–	15	pF	V_{CB} = 10 Volts, I_E = 0, f = 140 kHz
C_{ib}	–	80	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

2N3502, 2N3503, 2N3504, 2N3505 Ⓕ

PNP SILICON HIGH CURRENT SWITCHING TRANSISTORS

Packages:
2N3502/03, TO-5
2N3504/05, TO-18

These ITT PNP silicon planar epitaxial transistors are designed for digital and analog applications at current levels up to 500 milliamperes. Their high beta, high f_T at high current, high LV_{CEO}, and low noise figure make them ideal for use as line drivers, memory applications and low-noise amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	
(2N3502, 2N3503)	3.0 Watts
(2N3504, 2N3505)	1.3 Watts
T_A = 25°C (Notes 2 and 3)	
(2N3502, 2N3503)	0.7 Watt
(2N3504, 2N3505)	0.4 Watt
Collector-Base Voltage	
(2N3503, 2N3505)	−60 Volts
(2N3502, 2N3504)	−45 Volts
Collector-Emitter Voltage (Note 4)	
(2N3503, 2N3505)	−60 Volts
(2N3502, 2N3504)	−45 Volts
Emitter-Base Voltage	
(2N3503, 2N3505)	−5.0 Volts
(2N3502, 2N3504)	−5.0 Volts
Collector Current (Note 2)	
(2N3502, 2N3503, 2N3504, 2N3505)	600 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	80	120	–	–	I_C = 10μA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	120	–	–	–	I_C = 100μA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	135	200	–	–	I_C = 1.0 mA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	140	270	–	–	I_C = 10 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	100	150	300	–	I_C = 150 mA, V_{CE} = −10 Volts (Note 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	50	70	–	–	I_C = 500 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	115	160	300	–	I_C = 50 mA, V_{CE} = −1.0 Volt
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	−0.9	−1.0	Volt	I_C = 50 mA, I_B = 2.5 mA (Pulsed, see Note 1)
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	−1.0	−1.3	Volts	I_C = 150 mA, I_B = 15 mA (Pulsed, see Note 1)
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	−0.08	−0.25	Volt	I_C = 50 mA, I_B = 2.5 mA (Pulsed, see Note 1)
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	−0.18	−0.4	Volt	I_C = 150 mA, I_B = 15 mA (Pulsed, see Note 1)
h_{fe}	2N3503, 2N3505, 2N3502, 2N3504	2.0	2.50	–	–	I_C = 50 mA, V_{CE} = −20 Volts (f = 100 mc)
$V_{CEO(sust)}$	2N3503, 2N3505, 2N3502, 2N3504	−60 −45	– –	– –	Volts Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
t_{on}	2N3503, 2N3505, 2N3502, 2N3504	–	20	40	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA (Note 6)
t_{off}	2N3503, 2N3505, 2N3502, 2N3504	–	40	100	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx$ −30 mA (Note 6)
h_{FE}(−55°C)	2N3503, 2N3505, 2N3502, 2N3504	50	100	–	–	I_C = 50 mA, V_{CE} = −1.0 Volt
I_{CES}	2N3503, 2N3505	–	0.07	10	nA	V_{CE} = −50 Volts, V_{BE} = 0
I_{CES}	2N3502, 2N3504	–	0.05	10	nA	V_{CE} = −30 Volts, V_{BE} = 0
BV_{CBO}	2N3503, 2N3505 2N3502, 2N3504	−60 −45	– –	– –	Volts Volts	I_C = 10μA, I_E = 0
BV_{EBO}	2N3503, 2N3505, 2N3502, 2N3504	−5.0	–	–	Volts	I_E = 10μA, I_C = 0
C_{ob}	2N3503, 2N3505, 2N3502, 2N3504	–	4.5	8.0	pf	I_E = 0, V_{CB} = −10 Volts
C_{TE}	2N3503, 2N3505, 2N3502, 2N3504	–	15	25	pf	I_C = 0, V_{EB} = −0.5 Volt

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
NF	2N3503, 2N3505, 2N3502, 2N3504	–	1.0	4.0	dB	I_C = 30μA, V_{CE} = −5.0 Volts (Note 7)
I_{CBO}(+150)	2N3503, 2N3505	–	–	10	μA	V_{CB} = −50 Volts, I_E = 0
I_{CBO}(+150)	2N3502, 2N3504	–	–	10	μA	V_{CB} = −30 Volts, I_E = 0
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	−0.5	−1.6	Volts	I_C = 500 mA, I_B = 50 mA (Pulsed, see Note 5)
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	–	–	−2.0	Volts	I_C = 500 mA, I_B = 50 mA (Pulsed, see Note 5)

SMALL SIGNAL CHARACTERISTICS (f = 1kc)

Symbol	Min	Typ	Max	Unit	Conditions
h_{ie}	–	1050	2300	Ohms	I_C = 10 mA, V_{CE} = −10 Volts
h_{oe}	–	110	800	umhos	I_C = 10 mA, V_{CE} = −10 Volts
h_{re}	–	240	1500	$x10^{-6}$	I_C = 10 mA, V_{CE} = −10 Volts
h_{fe}	135	200	420	–	I_C = 10 mA, V_{CE} = −10 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 58.3°C/watt (derating factor of 17.2 mW/°C) for the 2N3502 and 2N3503, and 146°C/watt (derating factor of 6.85 mW/°C) for the 2N3504 and 2N3505; junction-to-ambient thermal resistance of 250°C/watt (derating factor of 4.0 mW/°C) for the 2N3502 and 2N3503, and 438°C/watt (derating factor of 2.28 mW/°C) for the 2N3504 and 2N3505.

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

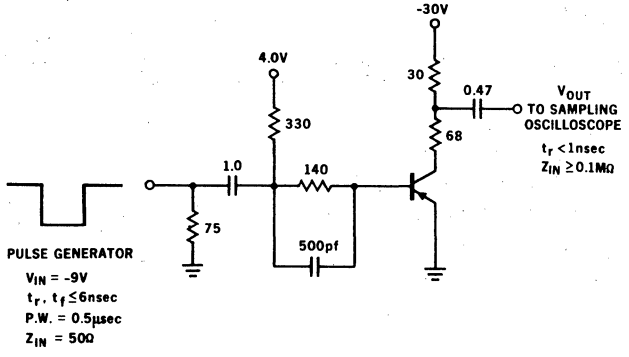
(5) Pulse Conditions: length = 300μsec; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

(7) f = 1.0 Kc; R_S = 10 KΩ.

SCHEMATIC

FIGURE 1 – T_{ON} AND T_{OFF} TEST CIRCUIT



HIGH SPEED NPN SILICON PLANAR EPITAXIAL HIGH-VOLTAGE HIGH-CURRENT TRANSISTORS

- **High Voltage: 80V min. 2N3725, 2N4014**
- **High Gain: 65 typ. @ 1000 mA**
- **Low V_{CE} (sat): 0.5V typ. @ 1000mA**
- **Low C_{ob}: 4.8 pF typ. @ 10V. 2N3725, 2N4014**
- **Fast t_{on}: 18 nsec typ. @ 500mA**
- **Fast t_{off}: 45 nsec typ. @ 500mA**

The ITT 2N3724 • 2N3725 and 2N4013 • 2N4014 are high-voltage, high-current NPN silicon planar epitaxial transistor useful for applications requiring breakdown voltages up to 50V and operating current to one ampere. Low saturation voltage and fast switching times make the transistor ideal for high-frequency amplifiers, core drivers, relay drivers and pulse generators.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	2N3724 2N4013	2N3725 2N4014	UNITS
Collector-to-Base Voltage	50	80	Volts
Collector-to-Emitter Voltage (shorted base)	50	80	Volts
Collector-to-Emitter Voltage (open base)	30	50	Volts
Emitter-to-Base Voltage	6.0	6.0	Volts
Collector Current (300 sec; 1% duty cycle)	1.0	1.0	Amps
Junction Temperature (op. and stg.)	-65 to +200		°C
Maximum Power Dissipation	**2N4013 2N4014**	**2N3724 2N3725**	
Total Dissipation @ T_C = 25°C	1.2	3.5	Watts
(derate above 25°C)	(6.8 mW/°C)	(20mW/°C)	
Total Dissipation @ T_A = 25°C	0.36	0.8	Watts
(derate above 25°C)	(2.06 mW/°C)	(4.56 mW/°C)	

2N3724, 2N3725, 2N4013, 2N4014
SILICON SWITCHING TRANSISTORS

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

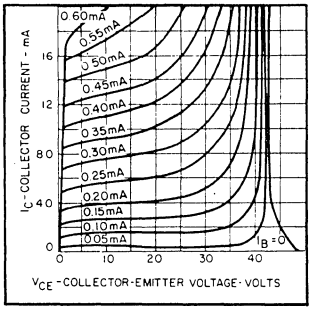
Symbol	2N3724 2N4013 Min.	Typ.	Max.	2N3725 2N4014 Min.	Typ.	Max.	Unit	Conditions
BV_{CBO}	50			80			Vdc	I_C= 10 A
BV_{CES}	50			80			Vdc	I_C10 A
LV_{CEO} [1,2]	30			50			Vdc	I_C= 10mA
BV_{EBO}	6.0			6.0			Vdc	I_E= 10 A
h_{FE} [1]	30	60		30	60			I_C= 10mA, V_{CE}= 1.0V
	60	90	150	60	90	150		I_C= 100mA, V_{CE}= 1.0V
	40	65		40	65			I_C= 300mA, V_{CE}= 1.0V
	35	50		35	50			I_C= 500mA, V_{CE}= 1.0V
	25	45		20	40			I_C= 800mA, V_{CE}= 2.0V
	30	65		25	65			I_C= 1000mA, V_{CE}= 5.0V
	30	45		30	40			I_C= 100mA, V_{CE}= 1.0V, T_A= -55°C
	20	40		20	35			I_C= 500mA, V_{CE}= 1.0V, T_A= -55°C
V_{CE} (sat) [1]		0.11	0.25		0.19	0.25	Vdc	I_C= 10mA, I_B= 1.0mA
		0.13	0.2		0.21	0.26	Vdc	I_C= 100mA, I_B= 10mA
		0.22	0.32		0.31	0.4	Vdc	I_C= 300mA, I_B= 30mA
		0.3	0.42		0.4	0.52	Vdc	I_C= 500mA, I_B= 50mA
		0.4	0.65		0.5	0.8	Vdc	I_C= 800mA, I_B= 80mA
		0.5	0.75		0.6	0.95	Vdc	I_C= 1000mA, I_B= 100mA
V_{BE} (sat) [1]		0.64	0.76		0.64	0.76	Vdc	I_C= 10mA, I_B= 1.0mA
		0.75	0.86		0.75	0.86	Vdc	I_C= 100mA, I_B= 10mA
		0.89	1.1		0.89	1.1	Vdc	I_C= 300mA, I_B= 30mA
	0.9	0.95	1.2	0.9	0.95	1.2	Vdc	I_C= 500mA, I_B= 50mA
		1.0	1.5		1.0	1.5	Vdc	I_C= 800mA, I_B= 80mA
		1.1	1.7		1.1	1.7	Vdc	I_C= 1000mA, I_B= 100mA
I_{CBO}		0.25	1.7				A	V_{CB}= 40V
					0.33	1.7	A	V_{CB}= 60V
		27	120				A	V_{CB}= 40V, T_A= 100°C
					25	120	A	V_{CB}= 60V, T_A= 100°C
C_{ob}		6.0	12		4.8	10	pF	V_{CB}= 10V
C_{ib}		40	55		40	55	pF	V_{EB}= 0.5V
h_{fe}	3.0	4.5		3.0	4.5			I_C= 50mA, V_{CE}= 10V, f = 100MHz
t_{on}		18	35		18	35	nsec	I_C = 500mA
t_{off}		45	60		45	60	nsec	I_{B1} = 50mA I_{B2} = 50mA

NOTES: 1. Pulse width 300 sec; 1% duty cycle.
2. Lowest emitter-to-collector voltage.

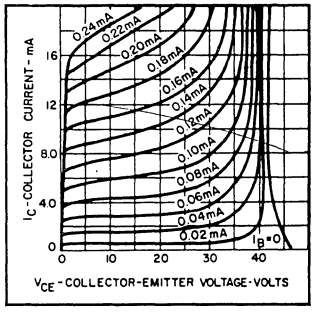
COLLECTOR CHARACTERISTICS 2N3724 2N4013

Collector Current vs. Collector Voltage, Low Base Current

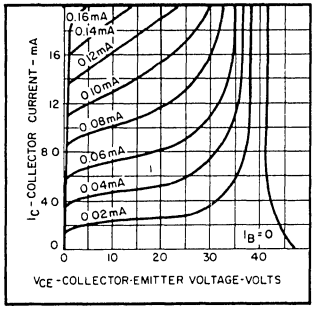
$T_A = -55°C$



$T_A = 25°C$

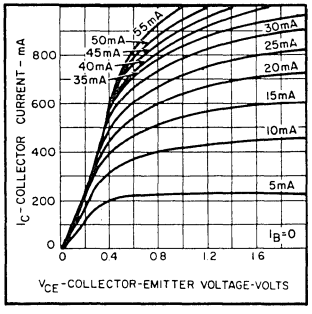


$T_A = 100°C$

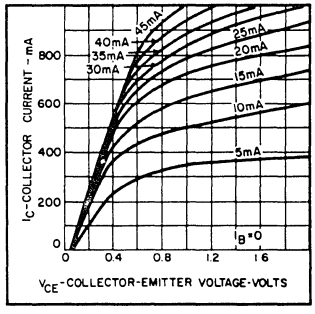


Collector Current vs. Collector Voltage, High Base Current

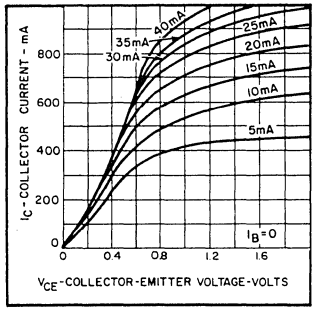
$T_A = -55°C$



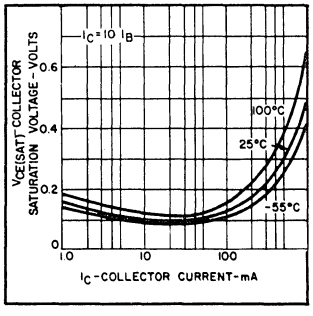
$T_A = 25°C$



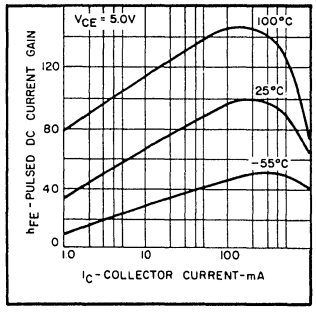
$T_A = 100°C$



COLLECTOR SATURATION VOLTAGE VS COLLECTOR CURRENT



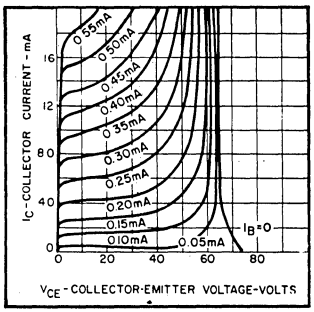
PULSED DC CURRENT GAIN VS COLLECTOR CURRENT



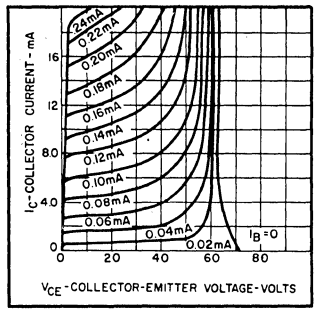
COLLECTOR CHARACTERISTICS 2N3725 2N4014

Collector Current vs. Collector Voltage, Low Base Current

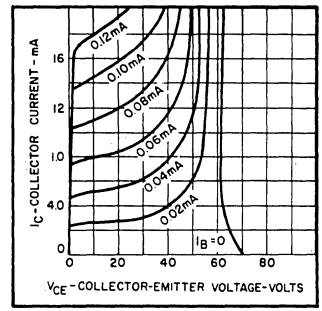
$T_A = -55°C$



$T_A = 25°C$

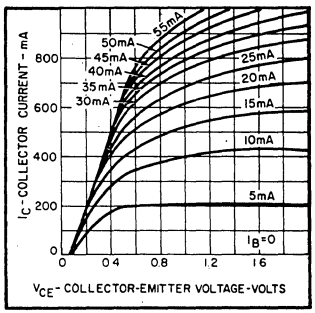


$T_A = 100°C$

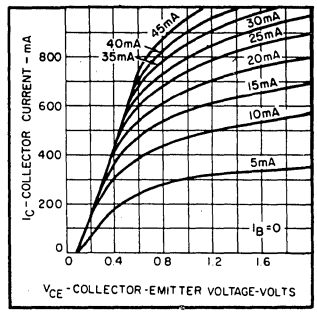


Collector Current vs. Collector Voltage, High Base Current

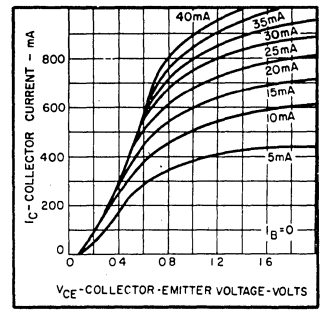
$T_A = -55°C$



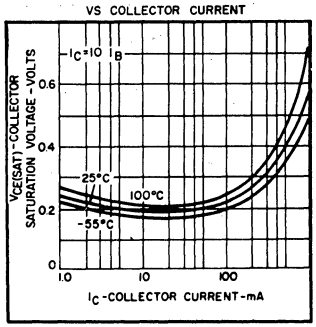
$T_A = 25°C$



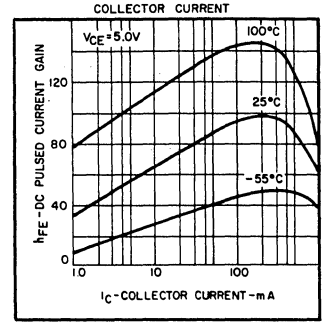
$T_A = 100°C$



COLLECTOR SATURATION VOLTAGE VS COLLECTOR CURRENT



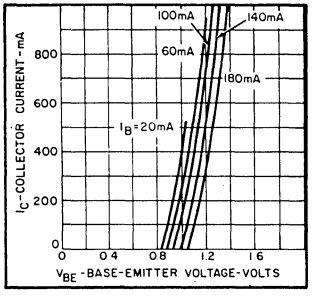
PULSED DC CURRENT GAIN VS COLLECTOR CURRENT



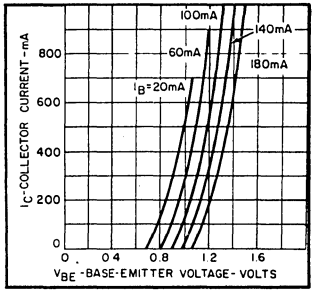
COLLECTOR CHARACTERISTICS 2N3724 2N3725 2N4013 2N4014

Collector Current vs. Base-Emitter Voltage

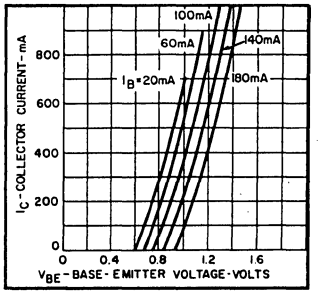
$T_A = -55°C$



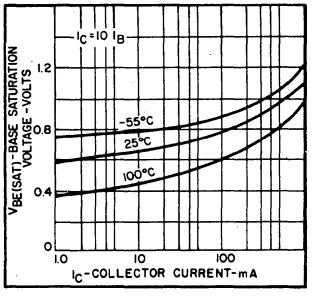
$T_A = 25°C$



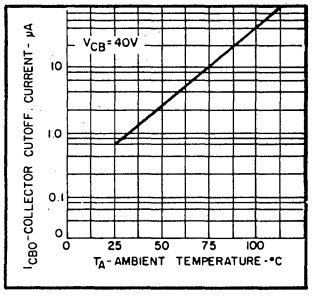
$T_A = 100°C$



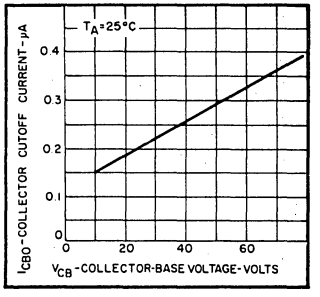
BASE SATURATION VOLTAGE VS COLLECTOR CURRENT



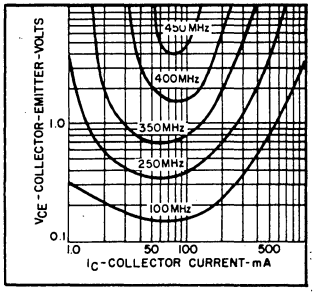
COLLECTOR CUTOFF CURRENT VS AMBIENT TEMPERATURE



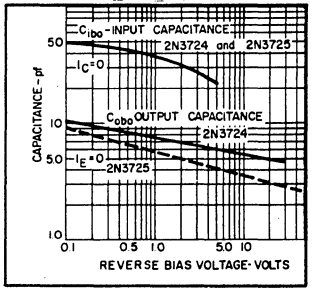
COLLECTOR CUTOFF CURRENT VS REVERSE BIAS VOLTAGE



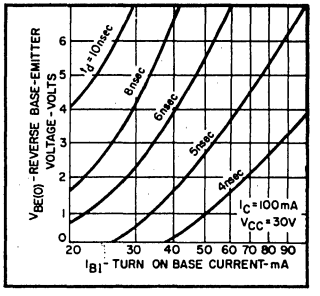
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



INPUT AND OUTPUT CAPACITANCE VS REVERSE BIAS VOLTAGE

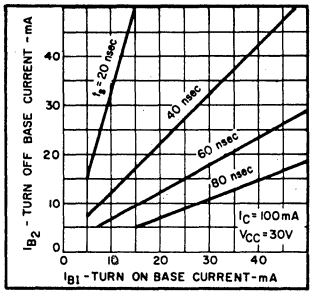


DELAY TIME VS TURN ON BASE CURRENT AND REVERSE BASE-EMITTER VOLTAGE

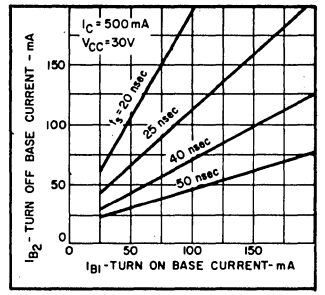


SWITCHING CHARACTERISTICS 2N3724 2N3725 2N4013 2N4014

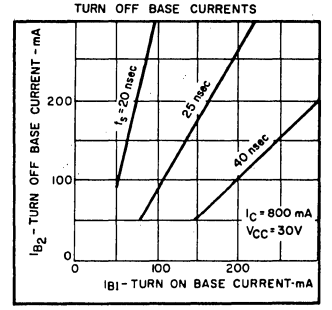
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



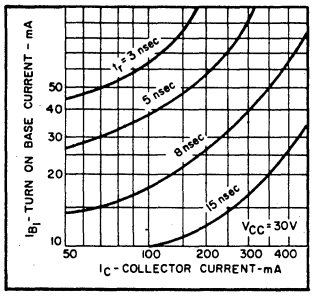
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



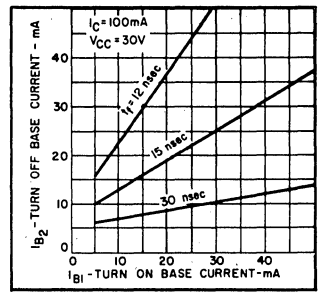
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



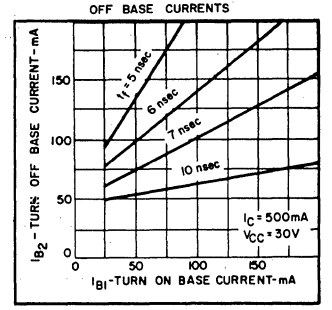
RISE TIME VS COLLECTOR AND TURN ON BASE CURRENTS



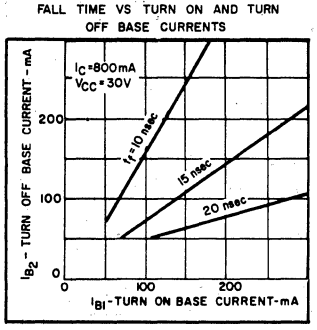
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



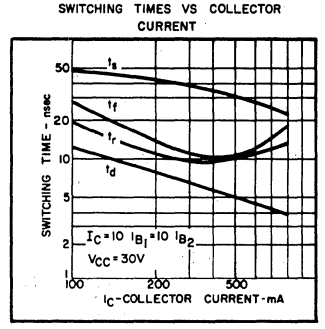
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



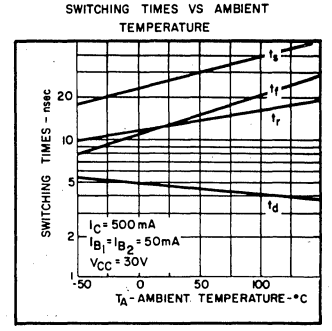
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



SWITCHING TIMES VS COLLECTOR CURRENT



SWITCHING TIMES VS AMBIENT TEMPERATURE



Package: TO-92

NPN SILICON GENERAL PURPOSE SWITCHING AND AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	60 Volts
Emitter-Base Voltage	6.0 Volts
Collector-Current	200 mA
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_A = 60°C	210 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	−55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	60	–	Volts	I_C = 10 μA, I_E = 0
BV_{CEO}*	40	–	Volts	I_C = 1.0 mA, I_B = 0*
BV_{EBO}	6.0	–	Volts	I_E = 10 μA, I_C = 0
I_{CEX}	–	50	nA	V_{CE} = 30 Volts, $V_{EB(off)}$ = 3.0 Volts
h_{FE}*	20	–	–	I_C = 0.1 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	40	–	–	I_C = 0.1 mA, V_{CE} = 1.0 Volt* (2N3904)
h_{FE}*	35	–	–	I_C = 1.0 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	70	–	–	I_C = 1.0 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	50	150	–	I_C = 10 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	100	300	–	I_C = 10 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	30	–	–	I_C = 50 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	60	–	–	I_C = 50 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	15	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	30	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (2N3904)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CE(sat)}$*	–	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA*
$V_{CE(sat)}$*	–	0.3	Volt	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	0.65	0.85	Volt	I_C = 10 mA, I_B = 1.0 mA*
$V_{BE(sat)}$*	–	0.95	Volt	I_C = 50 mA, I_B = 5.0 mA
f_T	250	–	MHz	I_C = 10 mA, V_{CE} = 20 Volts f = 100 MHz (2N3903)
f_T	300	–	MHz	I_C = 10 mA, V_{CE} = 20 Volts f = 100 MHz (2N3904)
C_{ob}	–	4.0	pF	V_{CB} = 5.0 Volts, I_E = 0, f = 100 kHz
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz
h_{ie}	0.5	8.0	k ohms	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{ie}	1.0	10	k ohms	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3904)
h_{re}	0.1	5.0	X 10^{-4}	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{re}	0.5	8.0	X 10^{-4}	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3904)
h_{fe}	50	200	–	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{fe}	100	400	–	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3904)
h_{oe}	1.0	40	μmhos	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz
t_d t_r	– –	35 35	ns ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = 0.5 Volt, I_C = 10 mA, I_{B1} = 1.0 mA
t_s	–	175	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA (2N3903)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
t_s	–	200	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA
t_f	–	50	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

SCHEMATIC

FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

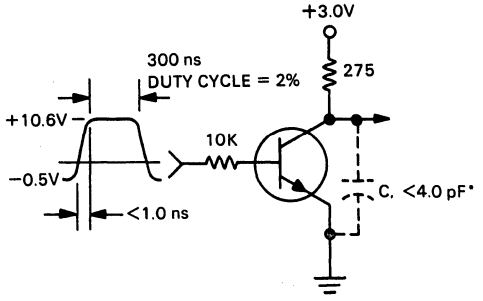
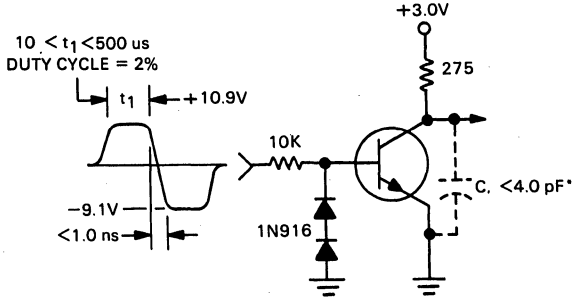


FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST TIME



*Total shunt capacitance of test jig and connectors

Package: TO-92

PNP SILICON GENERAL PURPOSE SWITCHING AND AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	200 mA
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_A = 60°C	210 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	−55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	–	Volts	I_C = 10μA, I_E = 0
BV_{CEO}*	40	–	Volts	I_C = 1.0 mA, I_B = 0
BV_{EBO}	5.0	–	Volts	I_E = 10μA, I_C = 0
I_{CEX}	–	50	nA	V_{CE} = 30 Volts, $V_{BE(off)}$ = 3.0 Volts
I_{BL}	–	50	nA	V_{CE} = 30 Volts, $V_{BE(off)}$ = 3.0 Volts
h_{FE}*	30	–	–	(2N3905) I_C = 0.1 mA, V_{CE} = 1.0 Volt
	60	–	–	(2N3906)
h_{FE}*	40	–	–	(2N3905) I_C = 1.0 mA, V_{CE} = 1.0 Volt
	80	–	–	(2N3906)
h_{FE}*	50	150	–	(2N3905) I_C = 10 mA, V_{CE} = 1.0 Volt
	100	300	–	(2N3906)
h_{FE}*	30	–	–	(2N3905) I_C = 50 mA, V_{CE} = 1.0 Volt
	60	–	–	(2N3906)
h_{FE}*	15	–	–	(2N3905) I_C = 100 mA, V_{CE} = 1.0 Volt
	30	–	–	(2N3906)
$V_{CE(sat)}$*	–	0.25	Volt	I_C = 10 mA, I_B = 1.0 mA
	–	0.4	Volt	I_C = 50 mA, I_B = 5.0 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{BE(sat)}$*	0.65	0.85	Volt	I_C = 10 mA, I_B = 1.0 mA
	–	0.95	Volt	I_C = 50 mA, I_B = 5.0 mA
f_T	200	–	MHz	(2N3905) I_C = 10 mA, V_{CE} = 20 Volts,
	250	–	MHz	(2N3906) f = 100 MHz
C_{ob}	–	4.5	pF	V_{CB} = 5.0 Volts, I_E = 0, f = 100 kHz
C_{ib}	–	10	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz
h_{ie}	0.5	8.0	k ohms	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	2.0	12	k ohms	(2N3906) f = 1.0 kHz
h_{re}	0.1	5.0	X 10^{-4}	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	1.0	10	X 10^{-4}	(2N3906) f = 1.0 kHz
h_{fe}	50	200	–	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	100	400	–	(2N3906) f = 1.0 kHz
h_{oe}	1.0	40	μmhos	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	3.0	60	μmhos	(2N3906) f = 1.0 kHz
NF	–	5.0	dB	(2N3905) I_C = 100 μA, V_{CE} = 5.0 Volts,
	–	4.0	dB	(2N3906) R_S = 1.0 k ohm, f = 10 Hz
				to 15.7 kHz
t_d	–	35	ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = 0.5 Volt,
t_r	–	35	ns	I_C = 10 mA, I_{B1} = 1.0 mA
t_s	–	200	ns	(2N3905) V_{CC} = 3.0 Volts, I_C = 10 mA,
	–	225	ns	(2N3906) I_{B1} = I_{B2} = 1.0 mA
t_f	–	60	ns	(2N3905) V_{CC} = 3.0 Volts, I_C = 10 mA,
	–	75	ns	(2N3906) I_{B1} = I_{B2} = 1.0 mA

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

SCHEMATIC

FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

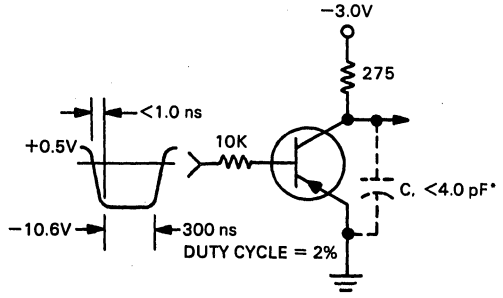
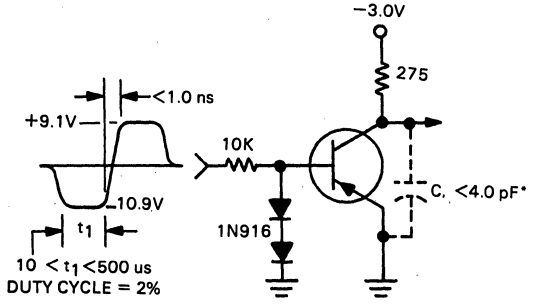


FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

2N3962, 2N3963, 2N3964, 2N3965 Ⓕ

PNP SILICON LOW-LEVEL, LOW-NOISE TYPE TRANSISTORS

Package: TO-18

- **LOW NOISE FIGURE** ..... NF = 2.0 dB (MAX) AT 1.0 kHz
  NF = 4.0 dB (MAX) AT 100 Hz
- **HIGH CURRENT GAIN** ..... h_{FE} = 180 (MIN) AT 1.0 μA
  h_{FE} = 250 - 500 AT 10 μA
  h_{FE} = 250 - 600 AT 1.0 mA
- **HIGH BREAKDWON VOLTAGE** ..... LV_{CEO} = 45, 60 AND 80 VOLTS
- **EXCELLENT BETA LINEARITY** ..... FROM 1.0 μA TO 50 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	
(2N3962, 2N3965)	−60 Volts
(2N3963)	−80 Volts
(2N3964)	−45 Volts
Collector-Emitter Voltage (Note 4)	
(2N3962, 2N3965)	−60 Volts
(2N3963)	−80 Volts
(2N3964)	−45 Volts
Emitter-Base Voltage	
(2N3962, 2N3963, 2N3964, 2N3965)	−6.0 Volts
Total Device Dissipation @:	
T_C = 25°C	1.2 Watts
T_A = 25°C	0.36 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	200°C
Lead Temperature (Soldering, 60 sec Time Limit)	300 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3962, 2N3963	60	175	–	–	I_C = 1.0 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	180	300	–	–	
h_{FE}	2N3962, 2N3963	100	210	300	–	I_C = 10 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	320	500	–	
h_{FE}	2N3962, 2N3963	100	240	–	–	I_C = 100 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	330	–	–	
h_{FE}	2N3962, 2N3963	100	260	450	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	330	600	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3962, 2N3963	100	280	–	–	I_C = 10 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	200	300	–	–	
h_{FE}	2N3962, 2N3963	90	260	–	–	I_C = 50 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	180	315	–	–	
h_{FE}(−55°C)	2N3962, 2N3963	40	90	–	–	I_C = 10μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	100	160	–	–	
h_{FE}(−55°C)	2N3962, 2N3963	45	150	–	–	I_C = 50 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	90	190	–	–	
h_{FE}(+100°C)	2N3962, 2N3963	–	375	600	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	–	400	800	–	
BV_{CBO}	2N3962	−60	–	–	Volts	I_C = 10μA, I_E = 0
	2N3964	−45	–	–	Volts	
BV_{CBO}	2N3963	−80	–	–	Volts	I_C = 10μA, I_E = 0
	2N3965	−60	–	–	Volts	
BV_{CES}	2N3962	−60	–	–	Volts	I_C = 10μA, I_B = 0
	2N3964	−45	–	–	Volts	
BV_{CES}	2N3963	−80	–	–	Volts	I_C = 10μA, I_B = 0
	2N3965	−60	–	–	Volts	
$V_{CEO(sust)}$	2N3962	−60	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0 (Notes 4 and 5)
	2N3964	−45	–	–	Volts	
$V_{CEO(sust)}$	2N3963	−80	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0 (Notes 4 and 5)
	2N3965	−60	–	–	Volts	
BV_{EBO}	2N3962, 2N3963	−6.0	–	–	Volts	I_C = 0, I_E = 10μA
	2N3964, 2N3965					
NF	2N3962, 2N3963	–	1.0	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	–	0.7	2.0	dB	R_S = 10 k ohms, BW = 15.7 kHz
NF	2N3962, 2N3963	–	0.8	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	0.5	2.0	dB	R_S = 10 k ohms, BW = 1.5 kHz
NF	2N3962, 2N3963	–	0.8	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	0.5	2.0	dB	R_S = 10 k ohms, BW = 150 Hz
NF	2N3962, 2N3963	–	3.0	10	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	1.8	4.0	dB	R_S = 10 k ohms, BW = 15 Hz
NF	2N3964, 2N3965	–	3.5	8.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts, R_S = 10 k ohms, BW = 2.0 Hz
I_{CES}	2N3962	–	0.5	10	nA	V_{CE} = −50 Volts, V_{EB} = 0
	2N3965					

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
I_{CES}	2N3963	–	0.5	10	nA	V_{CE} = −70 Volts, V_{EB} = 0
I_{CES}	2N3964	–	0.5	10	nA	V_{CE} = −40 Volts, V_{EB} = 0
I_{CES}(+150°C)	2N3962	–	2.0	10	μA	V_{CE} = −50 Volts, V_{EB} = 0
	2N3965	–	0.5	10	μA	
I_{CES}(+150°C)	2N3963	–	2.0	10	μA	V_{CE} = −70 Volts, V_{EB} = 0
I_{CES}(+150°C)	2N3964	–	2.0	10	μA	V_{CE} = −40 Volts, V_{EB} = 0
I_{EBO}	2N3962, 2N3963 2N3964, 2N3965	–	–	10	nA	I_C = 0, V_{EB} = −4.0 Volts
$V_{CE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	–	−0.1	−0.25	Volt	I_C = 10 mA, I_B = 0.5 mA
$V_{CE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	–	−0.16	−0.4	Volt	I_C = 50 mA, I_B = 5.0 mA (Note 5)
$V_{BE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	–	−0.72	−0.9	Volt	I_C = 10 mA, I_B = 0.5 mA
$V_{BE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	–	−0.81	−0.95	Volt	I_C = 50 mA, I_B = 5.0 mA (Note 5)
h_{ie}	2N3962, 2N3963 2N3964, 2N3965	2.5 6.0	8.0 10	17 20	k ohms k ohms	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{oe}	2N3962, 2N3963 2N3964, 2N3965	5.0 5.0	19 25	40 50	μmho μmho	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{re}	2N3962, 2N3963 2N3964, 2N3965	–	–	10	X 10^{-4}	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{fe}	2N3962, 2N3963 2N3964, 2N3965	100 250	300 360	550 700	– –	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{fe}	2N3962, 2N3963 2N3964, 2N3965	2.0 2.5	– –	8.0 8.0	– –	I_C = 0.5 mA, V_{CE} = −5.0 Volts
C_{obo}	2N3962, 2N3963 2N3964, 2N3965	–	–	6.0	pF	I_E = 0, V_{CB} = −5.0 Volts
C_{ibo}	2N3962, 2N3963 2N3964, 2N3965	–	–	15	pF	I_C = 0, V_{EB} = −0.5 Volt

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300μs; duty cycle = 1%.

2N4123, 2N4124
GENERAL PURPOSE NPN SILICON SWITCHING AND AMPLIFIER TRANSISTORS

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	2N4123	2N4124	Unit
Collector-Emitter Voltage	30	25	Vdc
Collector-Base Voltage	40	30	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW

Total Device Dissipation @ T_A = 25°C	310	mW
Derate above 25°C	2.81	mW/°C
Operating and Storage Junction Temperature Range	-55 to +135	°C
Thermal Resistance, Junction to Ambient	0.357	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4123
	25	–			2N4124
BV_{CBO}	40	–	Vdc	I_C = 10 uAdc, I_E = 0	2N4123
	30	–			2N4124
BV_{EBO}	5.0	–	Vdc	I_E = 10 uAdc, I_C = 0	
I_{CBO}	–	50	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	50	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	50	150	–	I_C = 2 mAdc, V_{CE} = 1 Vdc	2N4123
	120	360			2N4124
	25	–		I_C = 50 mAdc, V_{CE} = 1 Vdc	2N4123
	60	–			2N4124
$V_{CE(sat)}$*	–	0.3	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(sat)}$*	–	0.95	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$[h_{fe}]$	2.5	–	–	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4123
	3.0	–			2N4124
f_T	250	–	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4123
	300	–			2N4124
C_{ob}	–	4.0	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
h_{fe}	50	200	–	I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz	2N4123
	120	480			2N4124
NF	–	6.0	dB	I_C = 100 uAdc, V_{CE} = 5 Vdc, R_S = 1 k ohm, Noise Bandwidth = 10 Hz to 15.7 kHz	2N4123
	–	5.0			2N4124
t_d	Typ. 24		ns	Delay Time V_{CC} = 3 Vdc, $V_{EB(off)}$ = 0.5 Vdc,	
t_r	Typ. 13		ns	Rise Time I_C = 10 mAdc, I_{B1} = 1 mAdc	
t_s	Typ. 125		ns	Storage Time V_{CC} = 3 Vdc, I_C = 10 mAdc,	
t_f	Typ. 11		ns	Fall Time I_{B1} = I_{B2} = 1 mAdc	

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2%.

GENERAL PURPOSE NPN SILICON SWITCHING AND AMPLIFIER TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	2N4125	2N4126	Unit
Collector-Emitter Voltage	30	25	Vdc
Collector-Base Voltage	30	25	Vdc
Emitter-Base Voltage	4.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4125
	25	–			2N4126
BV_{CBO}	30	–	Vdc	I_C = 10 uAdc, I_E = 0	2N4125
	25	–			2N4126
BV_{EBO}	4.0	–	Vdc	I_E = 10 uAdc, I_C = 0	
I_{CBO}	–	50	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	50	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	50	150	–	I_C = 2 mAdc, V_{CE} = 1 Vdc	2N4125
	120	360			2N4126
	25	–		I_C = 50 mAdc, V_{CE} = 1 Vdc	2N4125
	60	–			2N4126
$V_{CE(sat)}$*	–	0.4	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(sat)}$*	–	0.95	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
h_{fe}	2.0	–	–	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4125
	2.5	–			2N4126
f_T	200	–	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4125
	250	–			2N4126
C_{ob}	–	4.5	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	10	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
h_{fe}	50	200	–	I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz	2N4125
	120	480			2N4126
NF	–	5.0	dB	I_C = 100 uAdc, V_{CE} = 5 Vdc, R_S = 1 ohm,	
	–				2N4125
	–	4.0		Noise Bandwidth = 10 Hz to 15.7 kHz	
					2N4126
t_d	Typ 25		ns	Delay Time V_{CC} = 3 Vdc, $V_{BE(off)}$ = 0.5 Vdc,	
t_r	Typ 18		ns	Rise Time I_C = 10 mAdc, I_{B1} = 1 mAdc	
t_s	Typ 140		ns	Storage Time V_{CC} = 3 Vdc, I_C = 10 mAdc,	
t_f	Typ 15		ns	Fall Time I_{B1} = I_{B2} = 1 mAdc	

*Pulse Test: Pulse Width = 300 usec, Duty Cycle = 2%.

2N4248, 2N4249, 2N4250®

PNP SILICON LOW LEVEL, LOW NOISE AMPLIFIER TRANSISTORS

Package: TO-92

- **Low Noise Figure** ..... 2.0 dB (max) at 1.0 kHz
- **High Current Gain** ..... 250-700 at 100 μA
- **High Breakdown** ..... 40 and 60 Volts (min) LV_{CEO}
- **Excellent Beta Linearity** ..... From 1 μA to 50 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperatures	−55°C to 125°C
Operating Junction Temperatures	125°C
Lead Temperature (Soldering, 10 seconds time limit)	260°C
Total Device Dissipation (Notes 2 and 3)	
@ T_C = 25°C	0.5 Watt
@ T_A = 25°C	0.2 Watt
Collector-Base Voltage	
(2N4248, 2N4250)	−40 Volts
(2N4249)	−60 Volts
Collector-Emitter Voltage	
(2N4248, 2N4250)	−40 Volts
(2N4249)	−60 Volts
Emitter-Base Voltage	
(2N4248, 2N4250)	−5.0 Volts
(2N4249)	−5.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
NF	2N4248	–	0.7	–	dB	I_C = 20 μA, V_{CE} = −5.0 Volts
	2N4249	–	0.7	3.0	dB	(Note 6)
	2N4250	–	0.5	2.0	dB	
NF	2N4248	–	1.0	–	dB	I_C = 20 μA, V_{CE} = −5.0 Volts
	2N4249	–	1.0	3.0	dB	(Note 7)
	2N4250	–	0.7	2.0	dB	
NF	2N4248	–	0.8	–	dB	I_C = 250 μA, V_{CE} = −5.0 Volts
	2N4249	–	0.8	3.0	dB	(Note 8)
	2N4250	–	0.7	2.0	dB	
h_{FE}	2N4248	–	90	–	–	I_C = 10 μA, V_{CE} = −5.0 Volts
	2N4249	–	190	–	–	
	2N4250	–	300	–	–	
h_{FE}	2N4248	50	100	–	–	I_C = 100 μA, V_{CE} = −5.0 Volts
	2N4249	100	240	300	–	
	2N4250	250	350	700	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N4248	50	110	–	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4249	100	250	–	–	
	2N4250	250	350	–	–	
h_{FE}	2N4248	50	120	–	–	I_C = 10 mA, V_{CE} = −5.0 Volts
	2N4249	100	280	–	–	(Note 5)
	2N4250	250	350	–	–	
BV_{CBO}	2N4248, 2N4250	−40	–	–	Volts	I_C = 10μA, I_E = 0
	2N4249	−60	–	–	Volts	
BV_{CES}	2N4248, 2N4250	−40	–	–	Volts	I_C = 10μA
	2N4249	−60	–	–	Volts	
$V_{CEO(sust)}$	2N4248, 2N4250	−40	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0
	2N4249	−60	–	–	Volts	(Notes 4 and 5)
BV_{EBO}	2N4248, 2N4249, 2N4250	−5.0	–	–	Volts	I_C = 0, I_E = 10μA
I_{CBO}	2N4248, 2N4249, 2N4250	–	–	10	nA	I_E = 0, V_{CB} = −40 Volts
$I_{CBO(65°C)}$	2N4248, 2N4249, 2N4250	–	–	3.0	μA	I_E = 0, V_{CB} = 40 Volts
I_{EBO}	2N4248, 2N4249, 2N4250	–	–	20	nA	I_C = 0, V_{BE} = 3.0 Volts
$V_{CE(sat)}$	2N4248, 2N4249, 2N4250	–	–	−0.25	Volt	I_C = 10 mA, I_B = 0.5 mA (Note 5)
$V_{BE(sat)}$	2N4248, 2N4249, 2N4250	–	–	−0.9	Volt	I_C = 10 mA, I_B = 0.5 mA (Note 5)
h_{fe}	2N4248	50	–	–	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4249	100	250	550	–	
	2N4250	250	350	800	–	
h_{fe}	2N4248, 2N4249	2.0	–	–	–	I_C = 0.5 mA, V_{CE} = −5.0 Volts
	2N4250	2.5	–	–	–	
C_{obo}	2N4248, 2N4249, 2N4250	–	–	6.0	pF	I_E = 0, V_{CB} = −5.0 Volts
C_{ibo}	2N4248, 2N4249, 2N4250	–	–	16	pF	I_C = 0, V_{BE} = 0.5 Volt

SMALL SIGNAL CHARACTERISTICS (f = 1 kHz)

Symbol		Min	Typ	Max	Unit	Conditions
h_{ie}	2N4249	2.5	8.0	17	k ohms	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	2N4250	6.0	10	20	k ohms	
h_{oe}	2N4249	5.0	19	40	μmho	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4250	5.0	25	50	μmho	
h_{re}	2N4249, 2N4250	–	–	10	$x10^{-4}$	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{fe}	2N4249	100	250	550	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4250	250	350	800	–	

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low-duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/watt (derating factor of 5.0 mW/°C); junction-to-ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

(4) This rating refers to a high-current point where collector to emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(6) R_S = 10 kΩ, Power Bandwidth of 150 Hz.

(7) R_S = 10 kΩ, Power Bandwidth of 15.7 kHz with 3.0 dB points at 10 Hz and 10 kHz.

(8) R_S = 1.0 kΩ, Power Bandwidth of 150 Hz.

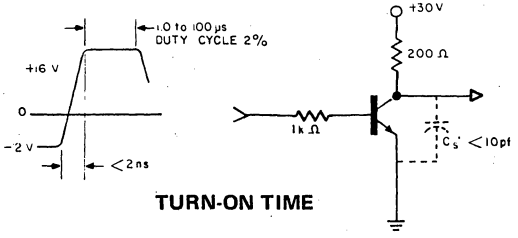
Package: To-92

ABSOLUTE MAXIMUM RATINGS

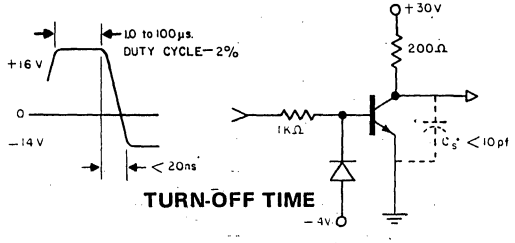
(T_A = 25°C unless otherwise noted)

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	60 Vdc
Emitter-Base Voltage	6.0 Vdc
Collector Current - Continuous	600 mAdc
Total Device Dissipation @ 25°C Case Temperature	.8W
Operating & Storage Junction Temperature Range	-55 to +135 °C

SWITCHING TIME EQUIVALENT TEST CIRCUITS



TURN-ON TIME



TURN-OFF TIME

SCOPE RISE TIME 4ns
*TOTAL SHUNT CAPACITANCE OF TEST JIG, CONNECTORS, AND OSCILLOSCOPE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	40	–	Vdc	I_C = 1 mAdc, I_B = 0	
BV_{CBO}	60	–	Vdc	I_C = 0.1 mAdc, I_E = o	
BV_{EBO}	6.0	–	Vdc	I_E = 0.1 mAdc, I_C = 0	
I_{CEX}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{EB(off)}$ = 0.4 Vdc	
I_{BL}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{EB(off)}$ = o.4 Vdc	
h_{FE}	20	–	–	I_C = 0.1 mAdc, V_{CE} = 1Vdc	2N4401
	20	–		I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4400
	40	–			2N4401
	40	–		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4400
	50	–			2N4401
	50	150		I_C = 150 mAdc, V_{CE} = 1 Vdc*	2N4400
	100	300			2N4401
	20	–		I_C = 500 mAdc, V_{CE} = 2 Vdc*	2N4400
	40	–			2N4401
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	0.75		I_C = 500 mAdc, I_B = 50 mAdc	
$V_{BE(sat)}$	0.75	0.95	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	1.2		I_C = 500 mAdc, I_B = 50 mAdc	
f_T	200	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz	
				2N4400	
	250	–		2N4401	

*Pulse Test: Pulse Width ≤ 300 us, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS	
C_{cb}	–	6.5	pF	V_{CB} = 5 Vdc, I_E = 0, f - 100 kHz, emitter guarded	
C_{eb}	–	30	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz, Collector guarded	
h_{ie}	0.5	7.5	k ohms	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = kHz	2N4400
	1.0	15			2N4401
h_{re}	0.1	8.0	x 10^4	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	
h_{fe}	20	250	–	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	2N4400
	40	500			2N4401
h_{oe}	1.0	30	*u*mhoe	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	
t_d	–	15	ns	V_{CC} = 30 Vdc, $V_{EB(off)}$ = 2 Vdc,	
t_r	–	20	ns	I_C = 150 mAdc, I_{B1} = 15 mAdc	
t_s	–	225	ns	V_{CC} = 30 Vdc, I_C = 150 mAdc,	
t_f	–	30	ns	I_{B1} = I_{B2} = 15 mAdc	

2N4402, 2N4403

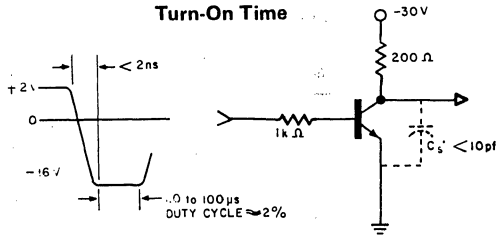
Package: To-92

GENERAL PURPOSE PNP SILICON SWITCHING AND AMPLIFYING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

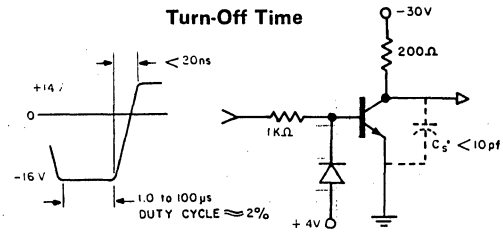
Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current - Continuous	600 mAdc
Total Device Dissipation @ 25°C Case Temperature	.8W
Operating & Storage Junction Temperature Range	-55 to +135 °C

Turn-On Time



SCOPE RISE TIME 4ns
TOTAL SHUNT CAPACITANCE OF TEST JIG, CONNECTORS, AND OSCILLOSCOPE

Turn-Off Time



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	40	–	Vdc	I_C = 1 mAdc, I_B = 0	
BV_{CBO}	40	–	Vdc	I_C = 0.1 mAdc, I_E = 0	
BV_{EBO}	5.0	–	Vdc	I_E = 0.1 mAdc, I_C = 0	
I_{CEX}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{BE(off)}$ = 0.4 Vdc	
I_{BL}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{BE(off)}$ = 0.4 Vdc	
h_{FE}	30	–		I_C = 0.1 mAdc, V_{CE} = 1 Vdc	2N4403
	30	–		I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4402
	60	–			2N4403
	50	–		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4402
	100	–			2N4403
	50	150		I_C = 150 mAdc, V_{CE} = 2 Vdc*	2N4402
	100	300			2N4403
	20	–		I_C = 500 mAdc, V_{CE} = 2 Vdc*	
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	0.75		I_C = 500 mAdc, I_B = 50 mAdc	
$V_{BE(sat)}$	0.75	0.95	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	1.3		I_C = 500 mAdc, I_B = 50 mAdc	
f_T	150	–	MHz	2N4402 I_C = 20 mAdc, V_{CE} = 10 Vdc,	
	200	–		2N4403 f = 100 MHz	

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2%.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
C_{cb}	—	8.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz, emitter guarded
C_{eb}	—	30	pF	V_{BE} = 0.5 Vdc, I_C = 0, f - 140 kHz, collector guarded
h_{ie}	750 1.5k	7.5k 15k	ohms	I_C - 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz 2N4402 2N4403
h_{re}	0.1	8.0	X 10^{-4}	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{fe}	30 60	250 500	—	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz 2N4402 2N4403
h_{oe}	1.0	100	*u*mhoe	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
t_d	—	15	ns	V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2 Vdc,
t_r	—	20	ns	I_C = 150 mAdc, I_{B1} = 15 mAdc
t_s	—	225	ns	V_{CC} = 30 Vdc, I_C = 150 mAdc,
t_f	—	30	ns	$I_{B1} = I_{B2}$ = 15 mAdc

Package: To-92

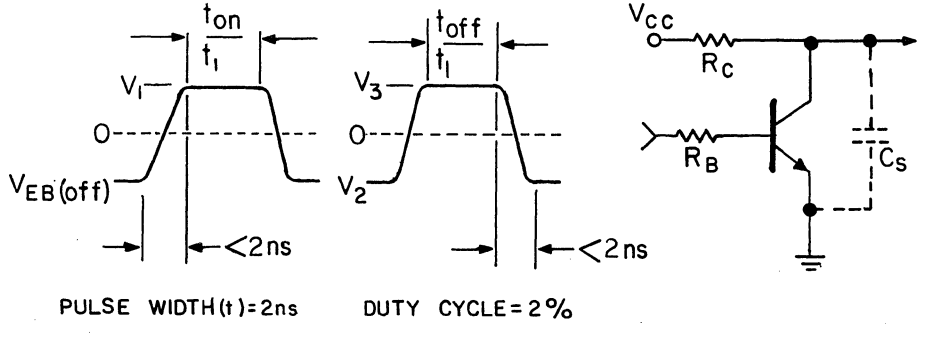
LOW-LEVEL NPN SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	2N4418	2N4419	Unit
Collector-Emitter Voltage	15	12	Vdc
Collector-Base Voltage	30		Vdc
Emitter-Base Voltage	6.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

TEST CONDITION	I_C	V_{CC}	R_B	R_C	$C_{S(max)}$	$V_{EB(off)}$	V_1	V_2	V_3
	mA	V	Ω	Ω	pF	V	V	V	V
A	10	3	3300	270	4	−15	10.55	−4.15	10.70
B	10	10	560	960	4	—	—	−4.65	6.55
C	100	10	560	96	12	−2.0	6.35	−4.65	6.55

Figure 1 — Switching Time Equivalent Test Circuit



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}	15	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4418
	12	–			2N4419
BV_{CBO}	30	–	Vdc	I_C = 10 *u*Adc, I_E = 0	
I_{CEX}	–	100	nAdc	V_{CE} = 12 Vdc, $V_{EB(off)}$ = 0.25 Vdc	
I_{BL}	–	0.1	*u*Adc	V_{CE} = 12 Vdc, $V_{EB(off)}$ = 0.25 Vdc	
	–	10		V_{CE} = 10 Vdc, $V_{EB(off)}$ = 0.25 Vdc, T_A = 100°C	
h_{FE}	25	–	–	I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4418
	50	–			2N4419
	40	160		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4418
	100	400			2N4419
	20	–		I_C = 10 mAdc, V_{CE} = 1 Vdc,	2N4418
	45	–		T_A = 55°C	2N4419
	40	–		I_C = 30 mAdc, V_{CE} = 1 Vdc	2N4418
	90	–			2N4419
	30	–		I_C = 100 mAdc, V_{CE} = 1 Vdc	2N4418
	55	–			2N4419
	20	–		I_C = 200 mAdc, V_{CE} = 1 Vdc	2N4418
	35	–			2N4419
$V_{CE(sat)}$	–	0.22	Vdc	I_C = 10 mAdc, I_B = 1 mAdc	
	–	0.35		I_C = 100 mAdc, I_B = 10 mAdc	
$V_{BE(sat)}$	0.65	0.80	Vdc	I_C = 10 mAdc, I_B = 1 mAdc	
	0.75	0.95		I_C = 100 mAdc, I_B = 10 mAdc	
f_T	300	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz	
C_{ob}	–	4.0	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
t_{on}	–	25	ns	Turn-On Time	Figure 1, Test Condition A V_{CC} = 3 Vdc, $V_{EB(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3 mAdc
t_{off}	–	35	ns	Turn-Off Time	Figure 1, Test Condition A V_{CC} = 3 Vdc, I_C = 10 mAdc, I_{B1} = 3 mAdc, I_{B2} = 1.5 mAdc
t_s	–	20	ns	Storage Time	Figure 1, Test Condition B V_{CC} = 10 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc
t_d	–	8.0	ns	Delay Time	Figure 1, Test Condition C V_{CC} = 10 Vdc, $V_{EB(off)}$ = 2 Vdc,
t_r	–	15	ns	Rise Time	I_C = 100 mAdc, I_{B1} = 10 mAdc
t_s	–	20	ns	Storage Time	Figure 1, Test Condition C V_{CC} = 10 Vdc, I_C = 100 mAdc,
t_f	–	15	ns		I_{B1} = I_{B2} = 10 mAdc
Q_T	–	80	pC	Total Control Charge	V_{CC} = 3 Vdc, I_C = 10 mAdc, I_B = mAdc

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	40 Vdc
Collector-Emitter Voltage	40 Vdc
Collector-Emitter Voltage Applicable 0. 01-200 mA	15 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mA
Collector Current (10 μs pulse)	500 mA
Total Device Dissipation @ T_A = 25°C	200 mW
Derate above 25°C	2.0 mW/°C
Total Device Dissipation @ T_C = 25°C	500 mW
Derate above 25°C	5.0 mW/°C
Operating Junction Temperature	125 °C
Storage Temperature Range	-55 to +125 °C

FIGURE 1–t_{on} and t_{off} TEST CIRCUIT

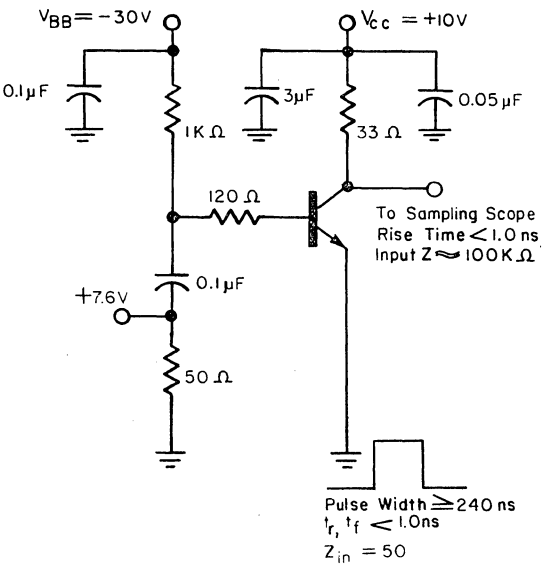
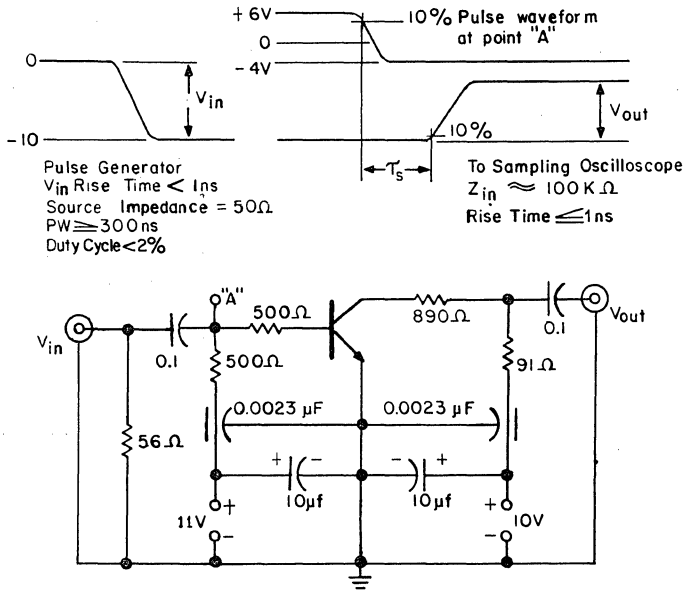


FIGURE 2–CHARGE STORAGE TIME MEASUREMENT CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{CES}	40	–	Vdc	I_C = 100 uAdc, V_{BE} = 0
$V_{CEO(sus)}$*	15	–	Vdc	I_C = 10 mAdc
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0
$V_{CE(sat)}$*	–	0.2	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	0.3		I_C = 30 mAdc, I_B = 3.0 mAdc, T_A = +65 C
	–	0.28		I_C = 100 mAdc, I_B = 10 mAdc
	–	0.5		I_C = 300 mAdc, I_B = 30 mAdc
$V_{BE(sat)}$*	0.75	0.95	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	1.2		I_C = 100 mAdc, I_B = 10 mAdc
	–	1.7		I_C = 300 mAdc, I_B = 30 mAdc
h_{FE}*	30	120	–	I_C = 30 mAdc, V_{CE} = 0.4 Vdc
	25	–		I_C = 100 mAdc, V_{CE} = 0.5 Vdc
	15	–		I_C = 300 mAdc, V_{CE} = 1.0 Vdc
I_{CES}	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
	–	3.0		V_{CE} = 20 Vdc, V_{EB} = 0, T_A = +65 C
I_B	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
C_{ob}	–	5.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 140 kHz
C_{ib}	–	8.0	pF	V_{BE} = 0.5 V, I_C = 0, f = 140 kHz
h_{fe}	3.5	–	–	I_C = 30 mA, V_{CE} = 10 V, f = 100 MHz
t_d	–	10	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_r	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_{on}	–	18	ns	I_C = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_s	–	20	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_f	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_{off}	–	28	ns	I_C = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
T_S	–	18	ns	I_C = 10 mA, I_{B1} = 10 mA, I_{B2} = -10 mA (Fig. 2)

*Pulse Conditions: PW $\leq$ 300 us; Duty Cycle $\leq$ 1%.

Package: To-92

2N5086, 2N5087

LOW-LEVEL, LOW-NOISE PNP SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	50 Vdc
Collector-Base Voltage	50 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	50 mAdc
Peak	100 mAdc

Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	50	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	50	–	–	Vdc	I_C = 100 uAdc, I_E = 0
I_{CBO}	–	–	10	nAdc	V_{CB} = 10 Vdc, I_E = 0
	–	–	50		V_{CB} = 35 Vdc, I_E = 0
I_{EBO}	–	–	50	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	150	–	500	–	I_C = 100 uAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	800		2N5087
	150	–	–		I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	–		2N5087
	150	–	–		I_C = 10 mAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	–		2N5087
$V_{CE(sat)}$	–	–	0.3	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	–	–	0.85	Vdc	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc
f_T	40	120	–	MHz	I_C = 500 uAdc, V_{CE} = 5.0 Vdc, f = 20 MHz 2N5086
	40	150	–		2N5087
C_{ob}	–	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz
h_{fe}	150	–	600	–	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz 2N5086
	250	–	900		2N5087
NF	–	–	3.0	dB	I_C = 20 uAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz 2N5086
	–	–	2.0		2N5087
	–	1.2	3.0		I_C = 100 uAdc, V_{CE} = 5.0 Vdc, R_S = 3.0 k ohmn, f = 1.0 kHz 2N5086
	–	1.0	2.0		2N5087

2N5221

Package: To-92

LOW-POWER GENERAL PURPOSE PNP SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	15 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	—	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	15	—	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	3.0	—	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	—	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	—	100	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	25	—	—	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	—	0.5	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
$V_{BE(sat)}$	—	1.1	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
f_T	100	—	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	—	15	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	—	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

2N5209, 2N5210

LOW-LEVEL, LOW-NOISE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	50 Vdc
Collector-Base Voltage	50 Vdc
Emitter-Base Voltage	4.5 Vdc
Collector Current - Continuous	50 mAdc
Peak	100 mAdc

Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	50	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	50	–	–	Vdc	I_C = 0.1 mAdc, I_E = 0
I_{CBO}	–	–	10	nAdc	V_{CB} = 10 Vdc, I_E = 0
	–	–	50		V_{CB} = 35 Vdc, I_E = 0
I_{EBO}	–	–	50	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
	–	–	100		V_{BE} = 4.5 Vdc, I_C = 0
h_{FE}	100	–	300	–	I_C = 100 uAdc, V_{CE} = 5.0 Vdc 2N5209
	200	–	600		2N5210
	150	–	–		I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc 2N5209
	250	–	–		2N5210
	150	–	–		I_C = 10 mAdc, V_{CE} = 5.0 Vdc 2N5209
	250	–	–		2N5210
$V_{CE(sat)}$	–	–	0.7	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	–	–	0.85	Vdc	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc
f_T	30	80	–	MHz	I_C = 500 uAdc, V_{CE} = 5.0 Vdc, f = 20 MHz
C_{cb}	–	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz emitter guarded
h_{fe}	150	–	600	–	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz 2N5209
	250	–	900		2N5210
NF	–	–	3.0	dB	I_C = 20 uAdc, V_{CE} = 5.0 Vdc, R_S = 22 k ohms, f = 10 Hz to 15.7 kHz 2N5209
	–	–	2.0		2N5210
	–	1.6	4.0		I_C = 20 uAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 1.0 kHz 2N5209
	–	1.4	3.0		2N5210

2N5219

Package: To-92

GENERAL PURPOSE NPN SILICON TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	20 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	20	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 2.0 Vdc, I_C = 0
h_{FE}	35	500	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	150	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	35	1500	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

2N5220

LOW-POWER GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	15 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	—	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	15	—	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	—	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	—	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	—	100	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	25	—	—	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	—	0.5	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
$V_{BE(sat)}$	—	1.1	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
f_T	100	—	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	—	10	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	—	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

ITT SEMICONDUCTORS

LOW-POWER GENERAL PURPOSE PNP SILICON AMPLIFIER TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	15 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	15	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	100	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.5	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
$V_{BE(sat)}$	–	1.1	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
f_T	100	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	15	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

2N5223

Package: To-92

LOW-LEVEL GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	20 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	20	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	50	800	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.7	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	1.2	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	150	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	50	1600	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

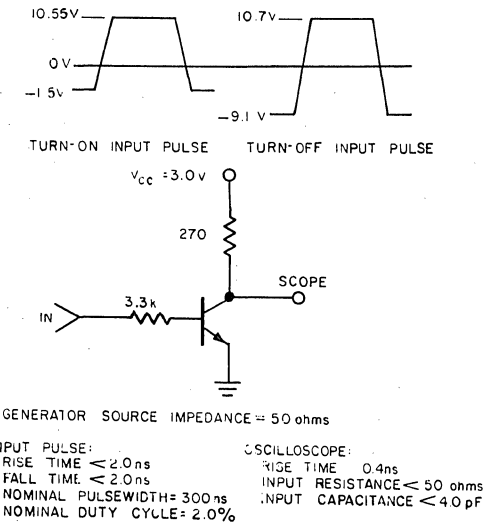
2N5224

GENERAL PURPOSE NPN SILICON LOW-LEVEL SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	12 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1 — Switching Time Test Circuit



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	12	—	Vdcq	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	—	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	5.0	—	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	—	500	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	—	100	uAdc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	40	400	—	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	15	—		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	—	0.35	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
$V_{BE(sat)}$	—	0.9	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
f_T	250	—	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{cb}	—	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
t_d	—	25	ns	Delay Time See Figure 1
t_r	—	20	ns	Rise Time See Figure 1
t_s	—	35	ns	Storage Time See Figure 1
t_f	—	25	ns	Fall Time See Figure 1

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2.0%.

Package: To-92

MEDIUM POWER NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	–	300	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.8	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
f_T	50	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	20	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

MEDIUM POWER PNP SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	300	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.8	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
f_T	50	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	20	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

2N5227

Package: To-92

GENERAL PURPOSE PNP SILICON LOW-LEVEL AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	30 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	50 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	30	—	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	30	—	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	—	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	—	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	—	500	nAdc	V_{BE} = 2.0 Vdc, I_C = 0
h_{FE}	30	—	—	I_C = 100 uAdc, V_{CE} = 10 Vdc
	50	700		I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	—	0.4	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	—	1.0	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	100	—	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	—	5.0	pF	V_{CB} = 10 Vdc, I_E = 0
h_{fe}	50	1500	—	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

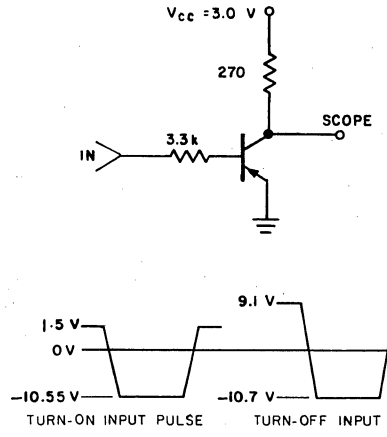
2N5228

GENERAL PURPOSE PNP SILICON LOW-LEVEL SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	5.0 Vdc
Collector-Emitter Voltage	6.0 Vdc
Collector-Base Voltage	5.0 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	50 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1 — Switching Time Test Circuit



GENERATOR SOURCE IMPEDANCE = 50 ohms

INPUT PULSE:
RISE TIME < 2.0 ns
FALL TIME < 2.0 ns
NOMINAL PULSEWIDTH = 300 ns
NOMINAL DUTY CYCLE = 2.0%

OSCILLOSCOPE:
RISE TIME 0.4ns
INPUT RESISTANCE < 50 ohms
INPUT CAPACITANCE < 4.0 pF

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	5.0	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	6.0	–	Vdc	I_C = 100 *u*Adc, V_{BE} = 0
BV_{CBO}	5.0	–	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CES}	–	100	nAdc	V_{CE} = 4.0 Vdc, V_{BE} = 0
I_{EBO}	–	100	*u*Adc	V_{BE} = 2.5 Vdc, I_C = 0
h_{FE}	30	–	–	I_C = 10 mAdc, V_{CE} = 0.3 Vdc
	15	–		I_C = 50 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
$V_{BE(sat)}$	0.65	1.25	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
f_T	300	–	MHz	I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz
C_{cb}	–	5.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
t_d	–	25	ns	Delay Time See Figure 1
t_r	–	50	ns	Rise Time See Figure 1
t_s	–	90	ns	Storage Time See Figure 1
t_f	–	50	ns	Fall Time See Figure 1

2N5368 thru 2N5371
GENERAL PURPOSE NPN SILICON TRANSISTORS

Package : TO-92

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C
Emitter-base voltage	5 V
Collector-base voltage	60 V
Collector-base voltage (2N5371)	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C = 10 mA)	30 V

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	50	nA	2N5368, 2N5369, 2N5370 V_{CB} = 40 V, I_E = 0
	–	50	nA	2N5371 V_{CB} = 30 V, I_E = 0
I_{EBO}	–	50	nA	V_{EB} = 3 V, I_C = 0
BV_{CBO}	60	–	V	2N5368, 2N5369, 2N5370 I_C = 10 *u*A, I_E = 0
	40	–	V	2N5371 I_C = 10 *u*A, I_E = 0
BV_{EBO}	5	–	V	I_E = 10 *u*A, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	20	–	–	2N5368
	50	–	–	2N5369
	75	–	–	2N5370 V_{CE} = 10 V, I_C = 1 mA
	20	–	–	2N5371
h_{FE}	40	–	–	2N5368
	75	–	–	2N5369
	150	–	–	2N5370 V_{CE} = 10 V, I_C = 10 mA, (Note 1)
	40	–	–	2N5371
h_{FE}	60	200	–	2N5368
	100	300	–	2N5369
	200	600	–	2N5370 V_{CE} = 10 V, I_C = 150 mA (Note 1)
	60	600	–	2N5371
V_{BE}	–	1.2	V	V_{CE} = 10 V, I_C = 150 mA (Note 1)
$V_{BE(sat)}$	–	1.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
$V_{CE(sat)}$	–	0.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
C_{cb}	–	8	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)
$[h_{fe}]$	2.5	–	–	V_{CE} = 10 V, I_C = 20 mA, f = 100 MHz
t_{on}	–	40	nsec	I_C = 150 mA, V_{CC} = 30 V, I_{B1} = 15 mA, (see fig. 1)
t_{off}	–	350	nsec	2N5368, 2N5369 I_C = 150 mA, V_{CC} = 30 V,
	–	400	nsec	2N5370, 2N5371 I_{B1} = I_{B2} = 15 mA (see fig. 2)

NOTES: 1. Pulse test: PW = 300 usec, duty cycle ≤ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

Package TO-92

GENERAL PURPOSE PNP SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C
Emitter-base voltage	5 V
Collector-base voltage	60 V
Collector-base voltage (2N5375)	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C - 10 mA	30 V

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	50	nA	2N5372, 2N5373, 2N5374 V_{CB} = 40 V, I_E = 0
	–	50	nA	2N5375 V_{CE} = 30 V, I_E = 0
I_{EBO}	–	50	nA	V_{EB} = 3 V, I_C = 0
BV_{CBO}	60	–	V	2N5372, 2N5373, 2N5374 I_C = 10 uA, I_E = 0
	40	–	V	2N5375 I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 10 uA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	20	–	–	2N5372
	50	–	–	2N5373
	100	–	–	2N5374 V_{CE} = 10 V, I_C = 1 mA
	20	–	–	2N5375
h_{FE}	30	–	–	2N5372
	75	–	–	2N5373
	150	–	–	2N5374 V_{CE} = 10 V, I_C = 10 mA (Note 1)
	30	–	–	2N5375
h_{FE}	40	120	–	2N5372
	100	300	–	2N5373
	200	400	–	2N5374 V_{CE} = 10 V, I_C = 150 mA (Note 1)
	40	400	–	2N5375
V_{BE}	–	1.2	V	V_{CE} = 10 V, I_C = 150 mA (Note 1)
$V_{BE(sat)}$	–	1.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
$V_{CE(sat)}$	–	0.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
C_{cb}	–	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)
$[h_{fe}]$	1.5	–	–	V_{CE} = 10 V, I_C = 20 mA, f = 100 MHz
t_{on}	–	50	nsec	I_C = 150 mA, V_{CC} = 30 V, I_{B1} = 15 mA, (see fig. 1)
t_{off}	–	150	nsec	2N5372, 2N5373 I_C = 150 mA, V_{CC} = 6 V,
	–	175	usec	2N5374, 2N5375 I_{B1} = I_{B2} = 15 mA (see fig. 2)

NOTES: 1. Pulse test: PW = 300 usec, duty cycle ≤ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

Package: TO-92

GENERAL PURPOSE NPN SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics **Unit**

Storage temperature range ..... -55 to +150 °C

Operating Collector Junction Temperature ..... +150 °C

Lead temperature 1/16" from case: 10 seconds max. ..... +260 °C

Emitter-base voltage ..... 5 V

Collector-base voltage ..... 60 V

Collector-emitter voltage (Applicable from I_C = 0 mA, to I_C = 10 mA) ..... 30 V

Collector current ..... 500 mA

Continuous device dissipation at or below 25°C free-air temperature ..... 360 mW

Linear derating factor above 25°C ..... 2.87 mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	10	nA	V_{CB} = 30 V, I_E = 0
BV_{CBO}	60	–	V	I_C = 10 *u*A, I_E = 0
BV_{EBO}	5	–	V	I_E = 100 nA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	100	500	–	2N5376 V_{CE} = 5 V, I_C = 10 *u*A
	40	200	–	2N5377 V_{CE} = 5 V, I_C = 10 *u*A
h_{FE}	120	600	–	2N5376 V_{CE} = 5 V, I_C = 1 mA
	100	500	–	2N5377 V_{CE} = 5 V, I_C = 1 mA
h_{FE}	150	–	–	2N5376 V_{CE} = 5 V, I_C = 10 mA (Note 1)
	120	–	–	2N5377
$V_{BE(sat)}$	0.65	0.80	V	I_C = 10 mA, I_B = 1 mA
$V_{CE(sat)}$	–	0.2	V	I_C = 10 mA, I_B = 1 mA
h_{ib}	20	32	Ohms	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{ob}	0.05	0.2	*u*mhos	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{fe}	120	1000	–	2N5376 I_C = 1 mA, V_{CE} = 5 V, f - 1 kHz
	100	900	–	2N5377
C_{cb}	–	8	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)
$[h_{fe}]$	30	150	–	V_{CE} = 5 V, I_C = 500 *u*A, f = 10 MHz
NF	–	2.0	dB	2N5376 I_C = 10 *u*A, V_{CE} = 5 V, Rg = 10 Ohms,
	–	3.0	dB	2N5377 Bandwith = 10 Hz to 15.7 kHz

NOTES: 1. Pulse test: Pulse width = 300 usec, duty cycle ≤ 2 %.

2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter shall be connected to the guard terminal of the bridge.

ITT SEMICONDUCTORS

2N5378, 2N5379

GENERAL PURPOSE PNP SILICON TRANSISTORS

Package: To-92

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Emitter-base voltage	5 V
Collector-base voltage	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C = 10 mA)	30 V
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	10	nA	V_{CB} = 30 V, I_E = 0
BV_{CBO}	40	–	V	I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 100 nA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	100	500	–	2N5378 V_{CE} = 5 V, I_C = 10 uA
	40	200	–	2N5379 V_{CE} = 5 V, I_C = 10 uA
h_{FE}	120	600	–	2N5378 V_{CE} = 5 V, I_C = 1 mA
	100	500	–	2N5379 V_{CE} = 5 V, I_C = 1 mA
h_{FE}	150	–	–	2N5378 V_{CE} = 5 V, I_C = 10 mA (Note 1)
	120	–	–	2N5379
$V_{BE(sat)}$	0.65	0.80	V	I_C = 10 mA, I_B = 1 mA
$V_{CE(sat)}$	–	0.2	V	I_C = 10 mA, I_B = 1 mA
h_{ib}	20	32	Ohms	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{ob}	0.06	0.5	umhos	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{fe}	120	1000	–	2N5378 I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
	100	900	–	2N5379
C_{cb}	–	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 Mhz (Note 2)
$[h_{fe}]$	20	100	–	V_{CE} = 5 V, I_C = 500 uA, f = 10 MHz
NF	–	2.0	dB	2N5378 I_C = 10 uA, V_{CE} = 5 V, Rg = 10 K Ohms,
	–	3.0	dB	2N5379 Bandwidth = 10 Hz to 15.7 kHz

NOTES:
1. Pulse: tPulse width = 300 usec, duty cycle ≤ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

2N5378, 2N5379

Package: To-92

GENERAL PURPOSE PNP SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Emitter-base voltage	5 V
Collector-base voltage	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C = 10 mA)	30 V
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	10	nA	V_{CB} = 30 V, I_E = 0
BV_{CBO}	40	–	V	I_C = 10 *u*A, I_E = 0
BV_{EBO}	5	–	V	I_E = 100 nA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	100	500	–	2N5378 V_{CE} = 5 V, I_C = 10 *u*A
	40	200	–	2N5379 V_{CE} = 5 V, I_C = 10 *u*A
h_{FE}	120	600	–	2N5378 V_{CE} = 5 V, I_C = 1 mA
	100	500	–	2N5379 V_{CE} = 5 V, I_C = 1 mA
h_{FE}	150	–	–	2N5378 V_{CE} = 5 V, I_C = 10 mA (Note 1)
	120	–	–	2N5379
$V_{BE(sat)}$	0.65	0.80	V	I_C = 10 mA, I_B = 1 mA
$V_{CE(sat)}$	–	0.2	V	I_C = 10 mA, I_B = 1 mA
h_{ib}	20	32	Ohms	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{ob}	0.06	0.5	*u*mhos	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{fe}	120	1000	–	2N5378 I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
	100	900	–	2N5379
C_{cb}	–	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 Mhz (Note 2)
$[h_{fe}]$	20	100	–	V_{CE} = 5 V, I_C = 500 *u*A, f = 10 MHz
NF	–	2.0	dB	2N5378 I_C = 10 *u*A, V_{CE} = 5 V, Rg = 10 K Ohms,
	–	3.0	dB	2N5379 Bandwidth = 10 Hz to 15.7 kHz

NOTES: 1. Pulse: tPulse width = 300 usec, duty cycle ≤ 2%.

2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

Package: To-92

PNP SILICON AMPLIFIER TRANSISTORS

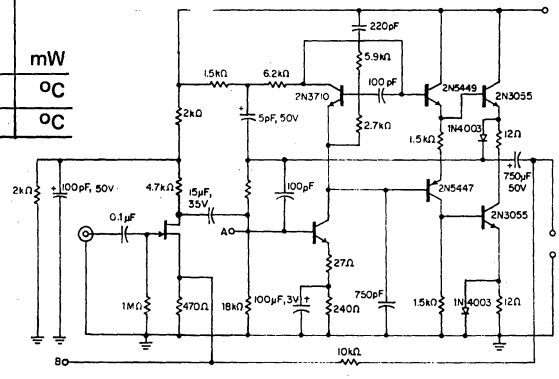
***ABSOLUTE MAXIMUM RATINGS** at 25°C free-air temperature (unless otherwise noted)

Characteristic	2N5447	2N5448	Unit
Collector-Base Voltage	−40	−50	V
Collector-Emitter Voltage (See Note 1)	−25	−30	V
Emitter-Base Voltage	−5	−5	V
Continuous Collector Current	200		mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360		mW
Continuous Device Dissipation at (or below) 25°C Lead Temperature (See Note 3)	500		mW
Storage Temperature Range	−65 to 150		°C
Junction Temperature-Operating	260		°C

NOTES:

1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/deg.
3. Derate linearly to 150°C lead temperature at the rate of 4 mW/deg. Lead temperature is measured on the collector lead 1/16 inch from the case.

SILICON 15-WATT QUASI-COMPLEMENTARY POWER AMPLIFIER



ELECTRICAL CHARACTERISTICS at 25°C free-air temperature

Symbol	2N5447 Min	2N5447 Max	2N5448 Min	2N5448 Max	Unit	Test Conditions
$V_{(BR)CBO}$	−40		−50		V	I_C = −100 uA, I_E = 0
$V_{(BR)CEO}$	−25		−30		V	I_C = −10 mA, I_B = 0, See Note 4
$V_{(BR)EBO}$	−5		−5		V	I_E = −100 uA, I_C = 0
I_{CBO}		−100		−100	nA	V_{CB} = 20 V, I_E = 0
I_{EBO}		−100		−100	nA	V_{EB} = −3 V, I_C = 0
h_{FE}	60	300	30	150		V_{CE} = −5 V, I_C = −50 mA, See Note 4
V_{BE}	−0.6	−1	−0.6	−1	V	V_{CE} = −5 V, I_C = −50 mA, See Note 4
V_{CE}		−0.25		−0.25	V	I_B = −5 mA, I_C = −50 mA, See Note 4
$[h_{fe}]$	5		5			V_{CE} = −5 V, I_C = −50 mA, f = 20 MHz
C_{cb}		12		12	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz See Note 5

NOTES: 4. These parameters must be measured using pulse techniques. t_p = 300 us, duty cycle $\leq$ 2%.
5. C_{cb} is measured using three-terminal measurement techniques with the emitter guarded.

2N5449, 2N5450, 2N5451
NPN SILICON AMPLIFIER TRANSISTORS

Package: To-92

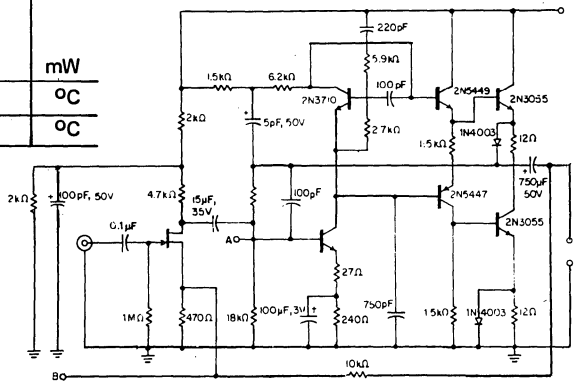
ABSOLUTE MAXIMUM RATINGS at 25°C free-air temperature (unless otherwise noted)

Characteristic	2N5449 2N5450	2N5451	Unit
Collector-Base Voltage	50	40	V
Collector-Emitter Voltage (See Note 1)	30	20	V
Emitter-Base Voltage	5	5	V
Continuous Collector Current	800		mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360		mW
Continuous Device Dissipation at (or below) 25°C Lead Temperature (See Note 3)	500		mW
Storage Temperature Range	-65 to 150		°C
Junction Temperature-Operating	260		°C

NOTES:

1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/deg.
3. Derate linearly to 150°C lead temperature at the rate of 4 mW/deg. Lead temperature is measured on the collector lead 1/16 inch from the case.

SILICON 15-WATT QUASI-COMPLEMENTARY POWER AMPLIFIER



***ELECTRICAL CHARACTERISTICS** AT 25°C FREE-AIR TEMPERATURE

Symbol	2N5449 Min	2N5449 Max	2N5450 Min	2N5450 Max	2N5451 Min	2N5451 Max	Unit	Test Conditions
$V_{(BR)CBO}$	50		50		40		V	I_C = 100 uA, I_E = 0
$V_{(BR)CEO}$	30		30		20		V	I_C = 10 mA, I_B = 0, See Note 4
$V_{(BR)EBO}$	5		5		5		V	I_E = 100 uA, I_C = 0
I_{CBO}		100		100		100	nA	V_{CB} = 20 V, I_B = 0
I_{EBO}		100		100		100	nA	V_{EB} = 3 V, I_C = 0
h_{fe}	100	300	50	150	30	600		V_{CE} = 2 V, I_C = 50 mA, See Note 4
V_{BE}	0.5	1	0.5	1	0.5	1	V	V_{CE} = 2 V, I_C = 100 mA, See Note 4
$V_{CE(sat)}$		0.6		0.8		1	V	I_B = 5 mA, I_C = 100 mA, See Note 4
$\|h_{fe}\|$	5		5		5			V_{CE} = 2 V, I_C = 50 mA, f = 20 MHz
C_{cb}		12		12		12	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz, See Note 5

NOTES: 4. These parameters must be measured using pulse techniques. Ip = 300 us, duty cycle — 3%.
5. C_{cb} is measured using three-terminal measurement techniques with the emitter guarded.

GOLD BOND GERMANIUM DIODES

How to Use This Buying Guide

Standard general purpose diodes are listed in numerical order below. Each diode has a line number referenced to the specification tables on pages 2, 3 and 4. Use this buying guide two ways: select the diode by type number, or locate the type number from the specification data.

Over 200 devices with their electrical specifications are listed. This represents a complete line of 18 milliwatt germanium gold bonded diodes.

ITT is the world's leading producer of diodes. Call your ITT sales engineer or distributor for quotation on all your diode needs.

Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N34	107	1N68	188	1N117	139	1N279	58
1N34A	100	1N68A	232	1N118	142	1N281	148
1N35	78	1N69	135	1N118A	146	1N283	47
1N38	201	1N69A	134	1N119	103	1N287	109
1N38A	191	1N70	224	1N120	105	1N288	177
1N38B	192	1N70A	225	1N126	136	1N289	175
1N44	211	1N71	73	1N126A	145	1N290	215
1N45	133	1N75	223	1N127	226	1N291	217
1N46	84	1N81	20	1N127A	230	1N292	149
1N47	212	1N81A	81	1N128	82	1N294	126
1N48	172	1N84	18	1N128A	83	1N294A	127
1N50	85	1N86	125	1N133	1	1N297	151
1N50	86	1N87	37	1N139	90	1N297A	152
1N51	79	1N87A	38	1N140	176	1N298	131
1N52	173	1N88	169	1N141	174	1N298A	52
1N52A	171	1N89	189	1N142	228	1N314	141
1N54	60	1N90	138	1N143	231	1N355	193
1N54A	87	1N95	140	1N144	57	1N367	23
1N55	234	1N96	143	1N145	53	1N417	99
1N55A	235	1N96A	111	1N191	182	1N418	106
1N55B	238	1N97	203	1N192	128	1N419	160
1N56	51	1N98	206	1N195	66	1N447	144
1N56A	72	1N98A	239	1N198	155	1N448	216
1N57	153	1N99	202	1N198A	194	1N449	92
1N58	199	1N100	205	1N198B	195	1N450	218
1N58A	197	1N100A	156	1N265	180	1N451	237
1N60	88	1N102	229	1N266	98	1N452	94
1N60A	68	1N103	15	1N267	41	1N453	221
1N61	233	1N104	16	1N268	50	1N454	150
1N62	209	1N107	14	1N270	166	1N455	95
1N63	227	1N108	93	1N270JAN	167	1N476	178
1N63A	196	1N111	129	1N273	55	1N477	179
1N65	170	1N112	130	1N276	110	1N478	198
1N66	101	1N113	122	1N276JAN	91	1N479	181
1N66A	102	1N114	123	1N277	220	1N480	104
1N67	154	1N115	124	1N277JAN	200	1N490	183
1N67A	190	1N116	137	1N278	108	1N497	56

GOLD BOND GERMANIUM DIODES

Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N498	116	1N770	31	1N996	44	G159	62
1N499	147	1N771	157	1N3110	7	G198	46
1N500	158	1N771A	164	1N3125	69	G199	36
1N501	207	1N771B	168	1N3146	45	G200	29
1N502	219	1N772	159	1N3287	2	G766	35
1N527	11	1N772A	132	1N3287WUSN	3	G788	96
1N541	76	1N773	120	1N3465	119	G790	28
1N542	77	1N773A	121	1N3466	75	G814	19
1N567	208	1N774	114	1N3467	24	G815	59
1N568	5	1N774A	118	1N3468	25	G816	13
1N569	21	1N775	115	1N3469	63	G819	187
1N571	20	1N776	33	1N3470	64	G820	112
1N616	32	1N777	117	1N3483	9	G821	65
1N617	210	1N781	70	1N3592	43	G822	49
1N618	213	1N781A	71	1N3666	165	G823	39
1N631	186	1N805	67	1N3666MUSN	161	G824	30
1N632	184	1N909	113	1N3666M1USN	162	G825	17
1N633	222	1N910	74	1N3666M2USN	163	G844	48
1N634	214	1N911	54	1N3769	185	G846	61
1N635	236	1N933	204	1N3773	40	G847	10
1N636	97	1N946	89	1N4523	27	G868	4
1N695	34	1N994	8	1N4524	12	G869	6
1N695A	42	1N995	22	G158	26		

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time			Part	Line
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to nsec	No.	No.
5	3	0.5	300	0.6				1N133	1
6	1	0.3	15	2				1N3287	2
6	100	1	15	2				1N3287W USN	3
6	100	1	15	2				G868	4
7	5	0.32	100	5				1N568	5
7	10	0.5	5	2				G869	6
8	5	0.45	20	8				1N3110	7
			100	8@65°C					
8	10	1	30	6	10	−6	3mA 2	1N994	8
8	10	0.6	10	3				1N3483	9
9	50	0.9	10	5	10		3mA 8	G847	10
10	1	0.3	50	10				1N527	11
10	10	0.65	12	6	10	−6	3	1N4524	12
10	10	0.65	12	6	10		10mA 3	G816	13
10	150	1	200	10				1N107	14
12	30	1	100	5				1N103	15
12	30	1	100	5				1N104	16
12	50	0.7	6	5	10		3mA 6	G825	17
12	60	1	100	5				1N84	18
12	100	0.85	15	5				G814	19
12	200	1	100	10@55°C	100	−5	10kΩ 4	1N571	20
12	250	0.5	50	10				1N569	21
15	10	0.5	10	6	10	−6	3mA 6	1N995	22
15	20	1						1N367	23

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time				Part	Line
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to	nsec	No.	No.
15	20	0.5	15	10	10	−6	1Ω	2	1N3467	24
15	20	0.5	60	10	10	−6	1Ω	2	1N3468	25
15	25	0.5	40	15	10	−6	1Ω	2	G158	26
15	100	1	30	10	10	−6		8	1N4523	27
15	100	1	30	10	10		1mA	8	G790	28
15	100	0.65	20	10	2			40	G200	29
18	50	0.76	8	5	2		0V	100	G824	30
20	5	0.42	40	10	5	−10	15*	350	1N770	31
20	8	1	400	20					1N616	32
20	50	1	200	10					1N776	33
			500	30						
20	100	1	2	10	5	−20	25kΩ	300	1N695	34
			20	10@70°C						
20	100	0.85	25	10	10		1	50	G766	35
20	100	0.7	10	10	2			50	G199	36
22.5	0.1	0.25	30	1.5					1N87	37
22.5	0.1	0.25				(subminiature 1N87)			1N87A	38
24	50	0.65	5	5	2		0V	80	G823	39
25	2	0.35	4	3	2	2mA**	0V	40	IN3773	40
25	3.5	1	12	10					1N267	41
25	10	1	2	10			0.2mA***	300	1N695A	42
			20	10@70°C						
25	15	0.5	4	4.5	2	0.2mA**		40	1N3592	43
25	40	0.8	15	5	5	−10	0.5mA	300	1N996	44
25	50	1	100	20	10	−6	3kΩ	2	1N3146	45
25	100	0.75	5	10	2			60	G198	46
25	200	1	20	10					1N283	47
25	300	1	20	6					G844	48
27	50	0.7	6	5	2		0V	350	G822	49
30	2.5	1	20	10					1N268	50
30	15	1	300	30					1N56	51
30	30	2	250	40					1N298A	52
30	40	1	100	10					1N145	53
30	100	1	10	10					1N911	54
30	100	1	20	20					1N273	55
30	100	1	20	20					1N497	56
30	100	1	200	100					1N144	57
30	100	1	200	20					1N279	58
30	100	0.85	30	20					G815	59
35	5	1	10	10					1N54	60
			100	50						
35	100	1	10	10	10		1mA	150	G846	61
35	600	1	60	20					G159	62
35	600	0.5	15	20					1N3469	63
35	600	0.5	30	20					1N3470	64
36	50	0.62	4	5	2		0V	250	G821	65
40	2	2	10	40				300	1N195	66
40	3	1	100	10					1N805	67
40	4	1	60	10					1N60A	68

GOLD BOND GERMANIUM DIODES

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time				Part No.	Line No.
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to	nsec		
40	5	0.4	100	40					1N3125	69
			125	20@71°C						
40	10	0.45	5	10	10	−10	0.1mA	500	1N781	70
			60	10@65°C						
40	10	0.45	5	10	10	−10	100μA	500	1N781A	71
			60	10@65°C						
40	15	1	300	30					1N56A	72
40	15	1	300	30					1N71	73
40	100	1	10	10					1N910	74
40	200	1	15	30					1N3466	75
45	10	2.2	18	10					1N541	76
			150	30						
45	10	2.2	18	10	(matched pair 1N541)				1N542	77
			150	30						
50			200	50		(matched pair)			1N35	78
50	2.5	1	1600	50					1N51	79
50	3	1	10	10					1N81	80
50	3	1	10	10					1N81A	81
50	3	1	10	10					1N128	82
50	3	1	10	10					1N128A	83
50	3	1	1500	50					1N46	84
50	4	1	200	20					1N49	85
50	4	1	80	20					1N50	86
50	5	1	7	10					1N54A	87
			100	50						
50	5	1	40	20					1N60	88
50	10	0.34	10	10					1N949	89
			50	10@55°C						
50	20	1	1500	50					1N139	90
50	40	1	20	10	5	−40		300	1N276JAN	91
			100	10@75°C						
50	50	1	30	30					1N449	92
50	50	1	200	50					1N108	93
50	100	1	30	30					1N452	94
50	300	1	30	30					1N455	95
55	150	1	5	10					G788	96
60	2.5	1	10	10					1N636	97
60	4	1	75	30					1N266	98
60	5	3.54			5	−40		300	1N417	99
60	5	1	30	10					1N34A	100
			500	50						
60	5	1	50	10					1N66	101
			800	50						
60	5	1	50	10					1N66A	102
60	5	1	125	50@55°C	30	−35	50kΩ	500	1N119	103
60	5	1	125	50@55°C		(solder-in 1N119)			1N480	104
60	5	1	250	50@55°C	30	−35	50kΩ	500	1N120	105
60	7	1			5	−40	2kΩ	300	1N418	106
60	8.5	1	15	10					1N34	107
			800	50						
60	20	1	125	50@75°C					1N278	108

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time			Part	Line
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to nsec	No.	No.
60	20	1	1500	50				1N287	109
60	40	1	100	50				1N276	110
			100	10@75°C					
60	40	1	500	50				1N96A	111
60	50	0.7	6	5				G820	112
60	100	1	10	10				1N909	113
60	100	1	15	10				1N774	114
			150	50					
60	100	1	20	10				1N775	115
			250	50					
60	100	1	25	40				1N498	116
60	100	1	25	10	30	−40	400Ω*	1N777	117
			125	50@55°C					
60	200	1	15	10				1N774A	118
			150	50					
60	200	1	20	45				1N3465	119
65	100	1	10	10				1N773	120
			100	50					
65	200	1	10	10				1N773A	121
			100	50					
70***	2.5	1	25	10@55°C				1N113	122
			125	50@55°C					
70***	2.5	1	50	10@55°C				1N114	123
			500	50@55°C					
70***	2.5	1	100	10@55°C				1N115	124
			500	50@55°C					
70	4	1	50	10				1N86	125
			833	50					
70	5	1	10	10				1N294	126
			800	50					
70	5	1	10	10				1N294A	127
70	5	1	20	10	30	−35	50kΩ 500	1N192	128
			50	70@50°C					
70****	5	1	25	10@55°C				1N111	129
			125	50@55°C					
70****	5	1	50	10@55°C				1N112	130
			250	50@55°C					
70	30	2	250	40				1N298	131
70	200	1	50	50				1N772A	132
75	3	1	410	50				1N45	133
75	5	1	30	10				1N69A	134
			500	50					
75	5	1	50	10				1N69	135
			850	50					
75	5	1	50	10				1N126	136
			800	50					
75	5	1	100	50				1N116	137
75	5	1	800	50				1N90	138
75	10	1	100	50				1N117	139
75	10	1	800	50				1N95	140

GOLD BOND GERMANIUM DIODES

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

PIV	mA	I_F V	I_R μA	@ V	Reverse Recovery Time I_FmA	V_R	Rec. to	nsec	Part No.	Line No.
75	15	1	50	10					1N314	141
75	20	1	100	50					1N118	142
75	20	1	800	50					1N96	143
75	25	1	20	10					1N447	144
			60	30						
75	25	1	50	10					1N126A	145
			850	50						
75	40	1	100	50					1N118A	146
75	100	1	30	50	5	−40		300	1N499	147
75	100	1	30	10					1N281	148
			500	50						
75	100	1	200	50					1N292	149
75	200	1	50	50					1N454	150
80	3.5	1	10	5					1N297	151
			100	50						
80	3.5	1	10	5					1N297A	152
			100	50						
80	3.6	1	300	75					1N57	153
80	4	1	5	5					1N67	154
80	4	1	10	10					1N198	155
			250	50@75°C						
80	40	1	50	50					1N100A	156
80	100	1	25	50					1N771	157
80	100	1	40	60					1N500	158
80	100	1	50	50					1N772	159
80	125	1	180	90	5	−40		300	1N419	160
80	200	1	10	20	30	−10		300	1N3666M USN	161
			150	20@70°C						
80	200	1	10	20	30	−10		300	1N3666M1 USN	162
			150	20@70°C						
80	200	1	10	20	30	−10		300	1N3666M2 USN	163
			150	20@70°C						
80	200	1	25	50					1N771A	164
80	200	1	25	50	30	−10	500μA	300	1N3666	165
80	200	1	100	50	5	−40		300	1N270	166
80	200	1	100	50					1N270JAN	167
			75	10@75°C						
80	400	1	25	50					1N771B	168
85	2.5	1	100	50					1N88	169
85	2.5	1	200	50					1N65	170
85	4	1	150	50					1N52A	171
85	4	1	833	50					1N48	172
85	5	1	150	50					1N52	173
85	20	1	50	50					1N141	174
85	20	1	50	50					1N289	175
85	40	1	300	50					1N140	176
85	40	1	350	50					1N288	177
90	2.5	1	11	10					1N476	178
			60	10@60°C						
90	2.5	1	11	10					1N477	179
			60	10@60°C						

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time				Part	Line
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to	nsec	No.	No.
90	3.2	1	100	60					1N265	180
90	5	1	7	10					1N479	181
90	5	1	25	10	30	−35	50kΩ	500	1N191	182
			125	50@55°C						
90	5	1	250	50@55°C		(solder-in	1N120)		1N490	183
90	7	1	120	60	5	−40	0.5mA	300	1N632	184
90	25	0.5	5	5					1N3769	185
			20	65						
90	50	3.5	120	60	5	−40	0.5mA	300	1N631	186
90	50	0.62	4	5					G819	187
100	3	1	625	100					1N68	188
100	3.5	1	8	5					1N89	189
100	4	1	5	5					1N67A	190
			50	50						
100	4	1	6	3					1N38A	191
			500	100						
100	4	1	6	3					1N38B	192
			500	100						
100	4	1	10	10					1N355	193
			50	50						
100	4	1	10	10					1N198A	194
			75	10@75°C						
100	4	1	50	50	2	−6	50k	300	1N198B	195
			250	50@75°C						
100	4	1	50	50					1N63A	196
100	4	1	600	100					1N58A	197
100	5	1	7	10					1N478	198
100	5	1	800	100					1N58	199
100	5	0.5	10	10					1N277JAN	200
			250	50@75°C						
100	7.5	1	25	10					1N38	201
100	10	1	50	50					1N99	202
100	10	1	100	50					1N97	203
100	14	1	10	10	5	−40	0.5mA***	400	1N933	204
			75	10@75°C						
100	20	1	5	50					1N100	205
100	20	1	100	50					1N98	206
100	100	1	40	80					1N501	207
100	150	1	150	100					1N567	208
110	5	1	700	125					1N62	209
115	3	1	11	10					1N617	210
			35	75@60°C						
115	3	1	410	50					1N44	211
115	5	1	4	3					1N47	212
			400	50						
115	5	1	70	10					1N618	213
115	50	1	45	45					1N634	214
			100	100						
120	5	1	100	100					1N290	215
120	25	1	30	30					1N448	216

GOLD BOND GERMANIUM DIODES

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

		I_F	I_R		Reverse Recovery Time				Part	Line
PIV	mA	V	μA	@ V	I_FmA	V_R	Rec. to	nsec	No.	No.
120	40	1	100	100					1N291	217
120	50	1	30	30					1N450	218
			100	100						
120	100	1	50	100					1N502	219
120	100	1	75	10@75°C					1N277	220
120	100	1	100	100					1N453	221
120	125	1	180	90	5	−40	0.5mA***	300	1N633	222
125	2.5	1	50	50					1N75	223
125	3	1	25	10					1N70	224
			300	50						
125	3	1	25	10					1N70A	225
			300	50						
125	3	1	25	10					1N127	226
			300	50						
125	4	1	50	50					1N63	227
125	5	1	100	100					1N142	228
125	15	1	3	25					1N102	229
125	25	1	25	10					1N127A	230
			300	50						
125	40	1	100	100					1N143	231
130	3	1	625	100					1N68A	232
130	5	1	300	100					1N61	233
			700	125						
150	3	1	800	150					1N55	234
150	4	1	500	150					1N55A	235
165	50	1	175	150					1N635	236
170	50	1	150	150					1N451	237
190	5	1	500	150					1N55B	238
250	40	1	100	50					1N98A	239

NOTES:
*Modified IBM Test Circuit
**I_R
***JAN Test Circuit
****@+55°C

ITT
SEMICONDUCTORS

SWITCHING DIODES TYPICAL CHARACTERISTICS

DPD TYPE #	DO-7 EQUIV. #	BV @ 5 μA V	MAXIMUM V_F @ 25°C V @ IF		V @ IF		V@ IF		V @ IF		V @ IF		V @ IF		T_{RR} ns	MAXIMUM REVERSE CURRENT μA @ 25°C	mA @ 150°C	V_R	CAP. @ 0.0V PF	T_{FR}	T_{RR} (5) ns	Stored Charge PC	ABSOLUTE MAXIMUM RATINGS Ave. Rect. Fwd. I @ 25°C mA	Max. Oper. Volt. Cont.	Power Diss. @ 25°C (12) MW
1N4148	1N914	75(1)	1.0	10											4(2)	.025	.05	20	4				75		500
1N4149	1N916	75(1)	1.0	10											4(2)	.025	.05	20	2				75		500
1N4150	1N3600		.54/.62	1.0	.66/.74	10	.76/.86	50	.82/.92	100	.87/1.0	200			(3)	0.1	0.1	50	2.5	10ns(4)			150		500
1N4151	1N3604	75	1.0	50											2(2)	.05	.05	50	2		4		150	50	500
1N4152	1N3605	40	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	30	2		4		150	30	500
1N4153	1N3606	75	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	50	2		4		150	50	500
1N4154	1N4009	35	1.0	30											2(2)	0.1	0.1	25	4		4		25	25	500
1N4305	1N4063	75	.505/.575	.25	.55/.65	1.0	.61/.71	2.0	.70/.85	10					2(2)	0.1	0.1	50	2		4		150		500
1N4444		70	.44/.55	0.1	.56/.68	1.0	.69/.82	10	.85/1.0	100						.05	.05	50	2		7		200	50	500
1N4446	1N914A	75(1)	1.0	20											4(2)	.025	.05	20	4				150	75	500
1N4447	1N916A	75(1)	1.0	20											4(2)	.025	.05	20	2				150	75	500
1N4448	1N914B	75(1)	.62/.72	5	1.0	100									4(2)	.025	.05	20	4	2.5V(6)			150	75	500
1N4449	1N916B	75(1)	.63/.73	5	1.0	30									4(2)	.025	.05	20	2	2.5V(6)			150	75	500
1N4450		40(1)	.42/.54	0.1	.52/.64	1.0	.64/.76	10	.80/.92	100	1.0	200			4(2)	.05	.05	30	4				200	30	500
1N4451		40	.40/.50	0.1	.51/.61	1.0	.62/.72	10	.75/.875	100	1.0	300				.05	.05	30	6		10		200	30	500
1N4452		40	.42/.54	0.1	.51/.62	1.0	.60/.71	10	.71/.83	100	1.0	600	.90/1.2	1A	50(7)	.05	.05	30	30				200	30	500
1N4453		30	.43/.55	.01	.51/.63	0.1	.60/.71	1.0	.69/.80	10	.80/92(8)	100				.05	.05	20	30			50/500(9)		20	400
1N4454	1N3064	75	1.0	10											2(2)	0.1	0.1	50	2	3.0V(10)	4			75	500
1N5194	1N483B	80(11)	1.0	100												.025	.005	70						80	250
1N5195	1N485B	200(11)	1.0	100												.025	.005	180						200	250
1N5196	1N486B	250(11)	1.0(13)	100												.025	.005	225						250	250
1N5605	1N457	70(11)	1.0	20												.025	.005	60						70	250
1N5606	1N458	150(11)	1.0	7.0												.025	.005	125						150	200
1N5607	1N459	200(11)	1.0	3.0												.025	.005	175						200	200
1N5608	1N658	120(11)	1.0	100											300(16)	.050	.025	50						120	250
1N5609	1N660	120(11)	1.0	6.0											300(17)	5.0	.050 (15)	100	2.7(14)					120	250

NOTES

1. BV=100V @ I_R 100μA
2. I_F=10mA Recover to 1mA
V_R=6V
R_L=100 Ohms
3. T_{RR}=4ns @ I_F=
I_R=10 to 200mA irr=0.1 I_F
T_{RR}=6ns @ I_F=
I_R=200 to 400mA irr=0.1 I_F
T_{RR}=6ns @ I_F=10mA,
I_R=1mA irr=0.1mA
4. I_F=200mA tr≤0.4ns, tp=100ns
V_{FR}=1.0V, DU≤1%
5. I_F=10mA
I_R=10mA
Recover to 1mA
6. 50mA peak square wave,
0.1 μs pulse width,
5 to 100 KC rep. rate,
generator tr≤30ns
7. I_F 500mA
V_R=adjust for I_R=500mA
Recover to 50mA
8. Pulse width=30μs, duty cycle=3%,
V_F measured at 25±3μs
9. Q @ I_F=1mA MIL-STD-750
method 4061
10. I_F=100mA peak square wave
0.1 μs pulse width
R_L=50 Ohms tr≤30 ns, 5 to 100KC
11. @ 100μA
12. Rated Max, Junction
Temp.=200°C
13. Pulse width=8.5msec,
duty cycle≤2%.
14. V_R=10V, f=1MHz
15. T =100°C
16. I_F=5mA, V_R=40V
R_I=2K, C_I=10pf
Recover to 80kΩ
17. I_F=30mA, V_R=35V
Recover to 400 kΩ

SILICON PLANAR DIODE

This section contains silicon diodes featuring:

- **Fast Switching**
- **High Conductance**
- **Low Leakage**
- **Voltages up to 250 Volts**

How To Use This Buying Guide

Standard general purpose diodes are listed in numerical order below. Each diode has a line number referenced to the specification tables on pages 2, 3 and 4. Use this buying guide two ways: select the diode by type number, or locate the type number from the specification data.

ITT is the world's leading producer of diodes. Call your ITT sales engineer or distributor for quotation on all your diode needs.

Part No.	Line No.	Part No.	Line No.
1N194	45	1N457A	84
1N194A	44	1N460	138
1N195	46	1N460A	139
1N196	43	1N461	28
1N251	20	1N461A	35
1N379	1	1N462	93
1N380	2	1N462A	96
1N381	3	1N464	169
1N382	6	IN482	38
1N383	11	1N482A	39
1N384	14	1N482B	58
1N385	23	1N483	94
1N386	40	1N483A	97
1N387	66	1N619	18
1N388	77	1N625	19
1N389	90	1N626	67
1N390	103	1N627	141
1N391	137	1N643	172
1N392	152	1N643A	173
1N393	168	1N658	161
1N456	31	1N658A	162
1N456A	36	1N659	68
1N457	80	1N662	126
1N662A	145	1N907A	30
1N663	129	1N908	53
1N663A	146	1N908A	56
1N690	60	1N914	107
1N691	130	1N914JAN	142
1N692	164	1N914A	114
1N696	54	1N914B	124
1N697	163	1N916	109
1N778	155	1N916A	115
1N789	25	1N916B	118
1N790	24	1N920	61
1N791	32	1N921	132
1N792	34	1N922	165
1N793	79	1N925	48
1N794	78	1N926	49
1N795	82	1N927	91
1N796	85	1N928	158
1N797	157	1N929	15
1N798	156	1N930	111
1N799	159	1N931	167
1N806	153	1N934	81
1N808	154	1N993	8
1N810	69	1N3062	112
1N811	7	1N3063	102
1N812	17	1N3064	105
1N813	4	1N3065	99
1N814	47	1N3066	106
1N815	5	1N3067	21
1N818	128	1N3068	22
1N837	149	1N3069	92
1N837A	150	1N3123	50
1N838	170	1N3124	51
1N840	70	1N3206	127
1N841	171	1N3298	136
1N844	151	1N3600	72
1N891	83	1N3600USN	73
1N892	160	1N3604	119
1N903	52	1N3605	42
1N903A	55	1N3606	101
1N904	26	1N3607	121
1N904A	29	1N3654	144
1N905	9	1N3669	98
1N905A	12	1N3731	147
1N906	10	IN3872	140
1N906A	13	1N4009*	16
1N907	27	1N4148*	108

SILICON PLANAR DIODE

Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N4149*	110	1N4446*	113	S398	65	S505	88
1N4150*	71	1N4447*	116	S400	131	S506	63
1N4151*	120	1N4448*	122	S401	75	S507	135
1N4152*	41	1N4449*	123	S402	143	S508	89
1N4153*	100	1N4450*	57	S403	125	S509	64
1N4154*	37	1N4451*	59	S500	133	WG140*	166
1N4305*	117	1N4453*	33	S501	87	WG141*	148
1N4380	76	1N4454*	104	S502	62	WG142*	74
1N4444*	95	S298	86	S504	134		

* Double plug diode package

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time t r r					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
9	35	1	0.5	8.2	5	8.2	100						35	6	1N379	1
11	30	1	0.5	10	5	10	100						30	6	1N380	2
13.5	24	1	0.5	12	5	12	100						28	64	1N381	3
15	5	1	0.5	5	10	5	125	5	−10	0.5mA	250	JAN 256			1N813	4
15	100	1.5	0.5	5	10	5	125	5	−10	0.5mA	250	JAN 256			1N815	5
17	17	1	0.5	15	5	15	100						25	6	1N382	6
20	1	1	1	10	10	10	125	5	−10	0.5mA	250	JAN 256	2	0	1N811	7
20	10	1.2	1	6				10	−6	3mA	4	R_L=75Ω			1N993	8
20	10	1	0.1	20	10	20	100	10	−5		4	R_L=100Ω	1	6	1N905	9
20	10	1	0.1	20	10	20	100	10	−5		4	R_L=100Ω	2.5	6	1N906	10
20	12	1	0.1	18	10	18	100						20	6	1N383	11
20	20	1	0.1	20	10	20	100	10	−5	1mA	4	R_L=100Ω	1	6	1N905A	12
20	20	1	0.1	20	10	20	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N906A	13
25	9	1	0.1	22	10	22	100						15	6	1N384	14
25	20	1	0.1	20											1N929	15
25	30	1	0.1	25	100	25	150	10	−6		2	R_L=100Ω	4	0	1N4009	16
30	2	1	1	10	10	10	125	5	−10	0.5mA	250	JAN 256	2	0	1N812	17
30	3	1	.08	10	16	10	100								1N619	18
30	4	1.5	1	20	30	20	100	30	−35	400kΩ	1000	IBM Y Mod			1N625	19
30	5	1	0.1	10	10	10	100	5	−10	0.5mA	150		1	0	1N251	20
30	5	1	0.1	20	100	20	150	10	−6	1mA	2	R_L=100Ω	4	0	1N3067	21
30	5	1	0.1	20	100	20	150	30	30mA*	1mA	50	R_L=100Ω	6	0	1N3068	22
30	7	1	0.1	27	10	27	100						12	6	1N385	23
30	10	1	5	20	30	20	100	5	−20	200kΩ	250				1N790	24
30	10	1	1	20	30	20	100	5	−20	200kΩ	500				1N789	25
30	10	1	0.1	30	10	30	100	10	−5		4	R_L=100Ω	1	6	1N904	26
30	10	1	0.1	30	10	30	100	10	−5		4	R_L=100Ω	2.5	6	1N907	27
30	15	1	0.5	25	30	25	150						10	0	1N461	28
30	20	1	0.1	30	10	30	100	10	−5	1mA	4	R_L=100Ω	1	6	1N904A	29
30	20	1	0.1	30	10	30	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N907A	30
30	40	1	0.025	25	5	25	150								1N456	31
30	50	1	5	20	30	20	100	5	−20	200KΩ	500				1N791	32
30	0.01	.43/.55	0.05	20	50	20	150						30	0	1N4453*	33
	0.1	.51/.63														
	1	.60/.71														
	10	.69/.80														
	100	.80/.92														
30	100	1	5	20	30	20	100	5	−20	100kΩ	500				1N792	34
30	100	1	0.5	25	30	25	150								1N461A	35
30	100	1	0.025	25	5	25	150						5	0	1N456A	36
35	30	1	0.1	25	100	25	150	10	−6	1mA					1N4154*	37
36	100	1.1	0.25	30	30	30	150				2	R_L=100Ω			1N482	38
36	100	1	0.025	30	15	30	150								1N482A	39
37	5.5	1	0.1	33	10	33	150						10	6	1N386	40
40	0.1	.49/.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4152*	41
	0.25	.53/.59														
	1	.59/.67														
	2	.62/.70														
	10	.70/.81														
	20	.74/.88														

ELECTRICAL CHARACTERISTICS, Continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time t r r					Cap. C		Part No.	Line No.
	mA	@ V_F	μA @ V_R		μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
40	0.1	0.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3605	42
40	1	2	10	40	300	50	150	30	−35		100				1N196	43
40	1	1	10	40	300	40	150	30	−35		200				1N194A	44
40	1.5	2	10	40	300	40	150	30	−35		200				1N194	45
40	2	2	10	40	300	40	150	30	−35		300				1N195	46
40	2	1	0.1	20	10	20	150	5	−10	0.5mA	250	JAN 256			1N814	47
40	5	1	1	10	20	10	100	5	−10	20kΩ	150	JAN 256			1N925	48
40	5	1	0.1	10	10	10	100	5	−10	20kΩ	150	JAN 256			1N926	49
40	10	1.5	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	0.8	6	1N3123	50
40	10	1.5	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	2	6	1N3124	51
40	10	1	0.1	40	10	40	100	10	−5		4	R_L=100Ω	1	6	1N903	52
40	10	1	0.1	40	10	40	100	10	−5		4	R_L=100Ω	2.5	6	1N908	53
40	10	1	0.015	20	20	20	150	10		10mA	5		4	0	1N696	54
40	20	1	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	1	6	1N903A	55
40	20	1	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N908A	56
40	0.1	.42/.54	0.05	30	50	30	150	10	−6	1mA	4	R_L=100Ω	4	0	1N4450*	57
	1	.52/.64														
	10	.64/.76														
	100	.80/.92														
	200	1														
40	100	1	0.025	30	5	30	150								1N482B	58
40	0.1	.40/.50	0.05	30	50	30	150						6	0	1N4451*	59
	1	.51/.61														
	10	.62/.72														
	100	.75/.88														
	300	1														
40	400	1	0.25	30	50	30	150	500	−30	10kΩ	800	R_L=1kΩ			1N690	60
40	400	1	0.25	30	50	30	150	500	−30	10kΩ	300	R_L=1kΩ	9	7.5	1N920	61
40	500	1	0.05	25				500	−30	10kΩ	15	R_L=100Ω	7	9	S502	62
40	500	1	0.05	25				500	−30	10kΩ	30	R_L=100Ω	7	9	S506	63
40	500	1	0.05	25				500	−30	10kΩ	50	R_L=100Ω	7	9	S509	64
40	500	0.9	0.2	25				500	−30	10kΩ	200	R_L=1kΩ	7	9	S398	65
43	4.5	1	0.1	39	10	39	100						8	6	1N387	66
50	4	1.5	1	35	30	35	100	30	−35	400kΩ	1000	IBM Y Mod			1N626	67
50	6	1	5	50	25	50	100	30	−35	400kΩ	300	JAN 256	2.7	10	1N659	68
50	10	1	1	40				10			50				1N810	69
50	150	1	0.1	40	15	40	100	30	−35	400kΩ	300	JAN 256			1N840	70
50	1	.54/.62	0.1	50	100	50	150	20 to 200	20 to 200**		4	irr=0.1 I_F	2.5	0	1N4150*	71
	10	.66/.74														
	50	.76/.86						200 to 400	200 to 400**		6	irr=0.1 I_F				
	100	.86/.92														
	200	.87/1.0						10	1**		6	irr=0.1 mA				
50	200	1	0.1	50	100	50	150	10		0.1mA	6		2.5	0	1N3600	72
50	200	1	0.1	50	100	50	150	10		1.1mA	4	R_L=100Ω	2.5	0	1N3600USN	73
50	250	1	0.1	30				10	−6	1mA	6	R_L=100Ω	4	0	WG142*	74
50	400	1	0.1	30				400	−30	10kΩ	15	R_L=100Ω	7	9	S401	75
50	570	1.4	50	50				570	−15	1mA	1.8	R_L=100Ω	3	15	1N4380	76
52	3.5	1	0.1	47	10	47	100						6	6	1N388	77
60	10	1	5	50	30	50	100	5	−40	200kΩ	250				1N794	78
60	10	1	1	50	30	50	100	5	−20	200kΩ	500				1N793	79
60	20	1	0.025	60	5	60	150						8	0	1N457	80
60	30	1	0.025	60	6	60	150	30	−35	400kΩ	1000				1N934	81
60	50	1	5	50	3	50	100	5	−40	200kΩ	500				1N795	82
60	50	1	0.1	50	25	50	100			80kΩ	300	JAN 256			1N891	83
60	100	1	0.025	60	5	60	150								1N457A	84
60	100	1	5	50	30	50	100	5	−40	100kΩ	500				1N796	85
60	500	1	0.2	30				500	−50	10kΩ	200	R_L=1kΩ	7	9	S298	86
60	500	1	0.1	30				500	−30	10kΩ	15	R_L=100Ω	7	9	S501	87
60	500	1	0.1	30				500	−30	10kΩ	30	R_L=100Ω	7	9	S505	88
60	500	1	0.1	30				500	−30	10kΩ	50	R_L=100Ω	7	9	S508	89
62	2.7	1	1	56	50	50	100						5.6	6	1N389	90
65	10	1	0.1	10	10	10	100	5	−10	20kΩ	150	Jan 256			1N927	91
65	50	1	0.1	50	100	50	100	30	30mA**	1mA	50	R_L=100Ω	6	0	1N3069	92
70	5	1	0.5	60	30	60	150						8	0	1N462	93
70	100	1.1	0.25	60	30	60	150								1N483	94
70	0.1	.44/.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4444*	95
	1	.56/.68														
	10	.69/.82														
	100	.85/1.0														
70	100	1	0.5	60	30	60	150								1N462A	96
70	100	1	0.025	60	15	60	150								1N483A	97
70	400	1.1	0.25	70				300	−10	1mA	200	R_L=100Ω	10	10	1N3669	98

SILICON PLANAR DIODE

ELECTRICAL CHARACTERISTICS, Continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time t r r					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
75	0.1	0.53	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1.5	0	1N3065	99
75	0.1	.49/.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4153*	100
	0.25	.53/.59														
	1	.59/.67														
	1	.62/.70														
	10	.70/.71														
	20	.74/.88														
75	0.1	0.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3606	101
75	0.25	0.58	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3063	102
75	2	1	1	68	50	68	100						5.2	6	1N390	103
75	10	1						10	−6	1mA	2	R_L=100Ω	2	0	1N4454*	104
75	10	1	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3064	105
75	10	1	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1	0	1N3066	106
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N914	107
75	10	1	0.025	20	50	20	150						4	0	1N4148*	108
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916	109
75	10	1	0.025	20	50	20	150						2	0	1N4149*	110
75	20	1	0.1	50											1N930	111
75	20	1	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1	0	1N3062	112
75	20	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N446*	113
75	20	1	0.025	20	50	20	150	10	−8	1mA	4	R_L=100Ω	4	0	1N914A	114
75	20	1	0.025	20	50	20		10	−6	1mA	4	R_L=100Ω	2	0	1N916A	115
75	20	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N447*	116
75	0.25	.50/.58						10	−6	1mA	2	R_L=100Ω	2	0	1N4305*	117
	1	.55/.65														
	2	.61/.71														
	10	.70/.81														
75	30	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916B	118
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3604	119
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4151*	120
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3607	121
75	5	.62/.72	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N4448*	122
	100	1.0														
75	5	.63/.73	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N4449*	123
	30	1.0														
75	100	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N914B	124
75	200	1	0.1	50	100	50	150	200	200mA**	0.1mA	6	R_L=100Ω	2.5	0	S403	125
80	10	1	1	10	100	50	100	5	−40	100kΩ	500		3	10	1N662	126
80	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N3206	127
80	30	1.5	0.25	60	20	60	100	20	−40		500	JAN 256			1N818	128
80	100	1	5	75	50	75	100	5	−40	200kΩ	500				1N663	129
80	400	1	0.25	60	50	60	150	500	−50	10kΩ	800	R_L=1kΩ			1N691	130
80	400	1	0.1	50				400	−30	10kΩ	15	R_L=100Ω	7	9	S400	131
80	500	1	0.25	60	50	60	150	500	−50	10kΩ	300	R_L=1kΩ			1N921	132
80	500	1	0.1	50				500	−30	10kΩ	15	R_L=100Ω	7	9	S500	133
80	500	1	0.1	50				500	−30	10kΩ	30	R_L=100Ω	7	9	S504	134
80	500	1	0.1	50				500	−30	10kΩ	50	R_L=100Ω	7	9	S507	135
80	500	0.9	0.2	60	45	60	150	500	−30	50mA	50	R_L=50Ω			1N3298	136
90	1.5	1	1	82	50	82	100						4.8	6	1N391	137
90	5	1	0.01	10	0.2	10	100						3	10	1N460	138
90	.15	1	0.01	10	0.2	10	100						4	10	1N460A	139
90	150	1	0.1	75				200	−20	5mA	50	R_L=100Ω	5	0	1N3872	140
100	4	1.5	1	75	30	75	100	30	−35	400kΩ	1000	IBM Y Mod			1N627	141
100	10	1	5	75	50	20	150	10			5	R_L=100Ω	2.8	1.5	1N914JAN	142
100	25	1	10	80	0.5	20	71	30	−35	400kΩ	100	R_L=2kΩ			S402	143
100	50	1	0.025	75	25	75	150	5	−6.5	1mA	4				1N3654	144
100	100	1	1	10	100	50	100	5	−40	100kΩ	300	JAN 256			1N662A	145
100	100	1	0.1	75	15	75	100	5	−40	200kΩ	300	JAN 256			1N663A	146
100	100	1	0.050	50	50	50	150	10	−6	1mA	3	R_L=100Ω	2	0	1N3731	147
100	100	1	0.050	50				10	−6	1mA	3	R_L=100Ω	2	0	WG141*	148
100	150	1	0.1	75	15	75	100	30	−35	400kΩ	500	JAN 256			1N837	149
100	150	1	0.1	80	15	80	100	30	−35	400kΩ	300	JAN 256			1N837A	150
100	200	1	0.1	80	15	80	100	30	−35	400kΩ	500	JAN 256			1N844	151
110	1.2	1	1	100	50	100	100						4.5	6	1N392	152
110	4	1	0.5	100	50	100	125	5	−40		300	JAN 256			1N806	153
110	100	1	1	100	50	100	125	30	−35		300	JAN 256			1N808	154
												R_L=500Ω				
112	10	1	0.5	100	30	100	125	5	−40	400kΩ	300	JAN 256			1N778	155
120	10	1	5	100	30	100	100	5	−40	200kΩ	250				1N798	156
120	10	1	1	100	30	100	100	5	−40	200kΩ	500				1N797	157
120	10	1	0.1	10	10	10	100	5	−10	20kΩ	150				1N928	158
120	50	1	5	100	30	100	100	5	−40	200kΩ	500				1N799	159

ELECTRICAL CHARACTERISTICS, Continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time t r r					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
120	50	1	0.1	100	25	100	100			80kΩ	300	JAN 256			1N892	160
120	100	1	0.05	50	25	50	150	5	−40	80kΩ	300				1N658	161
120	100	1	0.025	50	10	50	150	5	−40	80kΩ	300	JAN 256			1N658A	162
120	250	1	1	50				100	−10	10m	5		25	0	1N697	163
120	400	1	0.25	90	50	90	150	500	−50	10kΩ	800	R_L=1kΩ			1N692	164
120	500	1	0.25	90	100	90	150	500	−50	10kΩ	300	R_L=1kΩ			1N922	165
125	150	1						10	−6	1mA	4	R_L=100Ω			WG140*	166
125	20	1	0.1	100											1N931	167
135	0.9	1	1	120	50	120	100						4.2	6	1N393	168
150	3	1	0.5	125	30	120	150								1N464	169
150	150	1	0.1	125	15	125	100	30	−35	400kΩ	500	JAN 256			1N838	170
150	150	1	0.1	120	15	120	100	30	−35	400kΩ	300	JAN 256			1N841	171
175	10	1	0.025	10	15	100	100	5	−40	200kΩ	300				1N643	172
175	40	1	1.0	100	15	100	100						3	−10	1N643A	173

NOTES:
*Double plug diode package
**I_RmA

SILICON EPITAXIAL PLANAR DIODE

- **DO-35 Construction**
- **Hermetically Sealed**
- **Passivated Surfaces**
- **Inherently Reliable**

ABSOLUTE MAXIMUM RATINGS

Characteristics @ 25°C:	Units
Storage Temperature Range .....— 65 to 200	°C
Lead Temperature 1/16+ 1/32" from case for 10 sec 300	°C
Continuous Reverse Operating Voltage 75	Volts
Power Dissipation 500	mW
Derating Factor.....2.85	MW/°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Characteristic	Min.	Typ.	Max.	Unit	Conditions
Peak Inverse Voltage	75			V	5μa
Peak Inverse Voltage	100			V	100μa
Forward Voltage			1.0	V	10mA
Reverse Current			25	na	20V
Reverse Current		150	50	μa	20V
Capacitance			4	pf	0V
Reverse Recovery Time		*	4	nsec	1mA

*If=10mA Vr=6V R_L=100 ohms recover to 1. mA

SILICON EPITAXIAL PLANAR SWITCHING DIODE

- **DO-35 Construction**
- **Hermetically Sealed**
- **Passivated Surfaces**
- **Inherently Reliable**

ABSOLUTE MAXIMUM RATINGS

Characteristics @ 25°C	**Units**
Peak Inverse Voltage	100Volts
Power Dissipation	250 mV
Storage Temperature	−65 to +200°C
Avg. Rectified Fwd. Current	75 mA
Surge Current, 1 second	500mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
PIV	100			Vdc	I_R=100μA
I_R			25	nA	V_R=20V
			5.0	μA	V_R=75V
			50	μA	V_R=20V, T=150°C
			100	μA	V_R=75V, T=150°C
V_F			1.0	Vdc	I_F=10mA
C			4.0	pF	V_R=0V
			2.8	pF	V_R=1.5V
T_{rr}			5.0	nsec	I_F=I_R=10mA, C=3pF, R_L=100Ω, Rec. to 1.0mA
T_{fr}			5.0	Vdc	50mA/20 nsec, Rep. Rate Less than 100 KC

SILICON EPITAXIAL PLANAR SWITCHING DIODE

ABSOLUTE MAXIMUM RATINGS

Characteristics @ 25°C	Units
Peak Inverse Voltage	100Volts
Power Dissipation	250mW
Storage Temperature	−65 to +200°C
Avg. Rect. Fwd. Current	75mA
Surge Current, 1 sec.	500mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	Min.	Typ.	Max.	Unit	Conditions
PIV	100			Vdc	I_R=100μA
I_R			5.0	μA	V_R=75V
			.025	μA	V_R=20V
			50	μA	V_R=20V, T=150°C
V_F			1.0	Vdc	I_F=10mA
T_{rr}			4.0	nsec	I_F=10mA, V_R=6V
C			2.0	pF	V_R=OV
T_{fr}			2.5	Vdc	50mA Peak Square Wave, 0.1μsec Pulse Width, 5KC Rep. Rate, Max. Volt. Drop.

SILICON EPITAXIAL PLANAR SWITCHING DIODE

ABSOLUTE MAXIMUM RATINGS

Characteristics @ 25°C	Units
Peak Inverse Voltage	75Volts
Avg. Rect. Current	200mA
Recurrent Peak Fwd. Current	900mA
Surge Current, 1 sec.	1Amp
Power Dissipation	500mW
Operating Temperature	−65 to +150°C
Storage Temperature	−65 to +175°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	Min.	Typ.	Max.	Unit	Conditions
V_F	.87		1.0	Vdc	I_F=200mA
	.82		.92	Vdc	I_F=100mA
	.76		.86	Vdc	I_F=50mA
	.66		.74	Vdc	I_F=10mA
	.54		.62	Vdc	I_F=1mA
I_R			100	nA	V_R=50V
			100	μA	V_R=50V, T=150°C
PIV	75			Vdc	I_R=5μA
C			2.5	pF	V_R=0V
T_{rr}			4.0	nsec	I_F=I_R=10 to 200mA Rec. to 0.1 of I_F
			6.0	nsec	I_F=I_R=200 to 400mA Rec. to 0.1 of I_F

SILICON EPITAXIAL PLANAR SWITCHING DIODE

ABSOLUTE MAXIMUM RATINGS

Characteristics @ 25°C	Units
Peak Inverse Voltage	75Volts
Avg. Rect. Current	200mA
Recurrent Peak Fwd. Current	900mA
Surge Current, 1 sec.	1Amp
Power Dissipation	500mW
Operating Temperature	−65 to +150°C
Storage Temperature	−65 to +175°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

Symbol	Min.	Typ.	Max.	Unit	Conditions
V_F			1.2	Vdc	I_F=500mA
			1.0	Vdc	I_F=400mA
	.80		.90	Vdc	I_F=200mA
	.75		.85	Vdc	I_F=100mA
	.62		.70	Vdc	I_F=10mA
I_R			100	nA	V_R=30V
			100	μA	V_R=30V, T=150°C
PIV	50			Vdc	I_R=5μA
C			3.0	pF	V_R=0V
T_{rr}			6.0	nsec	I_F=I_R=10mA, R_L=100Ω Rec. to 1.0mA

SILICON EPITAXIAL PLANAR SWITCHING DIODE

For General Purpose High-Voltage Applications

MAXIMUM RATINGS @ 25°C (NOTE 1)

	ITT2001	ITT2002	ITT2003
Peak Inverse Voltage	100Volts	200Volts	250Volts
Average Rectified Current	150ma	150ma	150ma
Forward Current Steady State D.C.	250ma	250ma	250ma
Recurrent Peak Forward Current	400ma	400ma	400ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0A	1.0A	1.0A
Power Dissipation	300mw	300mw	300mw
Power Derating	3.3mw/°C	3.3mw/°C	3.3mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ELECTRICAL CHARACTERISTICS, ITT2001 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=100ma
IR_1	Reverse Current		0.1	ua	VR=50V
IR_2	Reverse Current (150°C)		100	ua	VR=50V
BV	Breakdown Voltage	100		Volts	IR=100ua
Q_S	Store Charge (Note 2)		500	pc	IF=10ma
C_O	Capacitance		5.0	pf	VR=0V, f=1MHz

NOTES:

1. The maximum ratings are limiting values above which life or satisfactory performance may be impaired.
2. This test is equivalent to T_{rr} @ IF = IR = 30 ma, RL — 100 ohms, recovered to 3 ma to be less than 50 nsec.

ITT2001, ITT2002, ITT2003
SILICON SWITCHING DIODE

ELECTRICAL CHARACTERISTICS, ITT2002 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=100ma
IR_1	Reverse Current		0.1	ua	VR=150V
IR_2	Reverse Current (150°C)		100	ua	VR=150V
BV	Breakdown Voltage	200		Volts	IR=100ua
Q_S	Storage Charge (Note 2)		500	pc	IF=10ma
C_O	Capacitance		5.0	pf	VR=0V, f=1MHz

ELECTRICAL CHARACTERISTICS, ITT2003 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=100ma
IR_1	Reverse Current		0.1	ua	VR=150V
IR_2	Reverse Current (150°C)		100	ua	VR=150V
BV	Breakdown Voltage	250		Volts	IR=100ua
Q_S	Store Charge (Note 2)		500	pc	IF=10ma
C_O	Capacitance		5.0	pf	VR=0V, f=1MHz

ITT SEMICONDUCTORS

HIGH VOLTAGE HIGH TEMPERATURE DOUBLE PLUG DIODE

MAXIMUM RATINGS (25°C) Note 1

	3001	3002	3003
Peak Inverse Voltage	70Volts	150Volts	200Volts
Average Rectified Current	100ma	100ma	100ma
Forward Current Steady State D.C.	200ma	200ma	200ma
Recurrent Peak Forward Current	300ma	300ma	300ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0A	1.0A	1.0A
Power Dissipation	250mw	250mw	250mw
Power Derating	2.0mw/°C	2.0mw/°C	2.0mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ELECTRICAL CHARACTERISTICS ITT3001 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=100ma
IR_1	Reverse Current		0.025	ua	VR=60V
IR_2	Reverse Current (150°C)		5	ua	VR=60V
BV	Breakdown Voltage	70		Volts	IR=100ua
C_O	Capacitance		8	pf	VR=0V, f=1MHz

NOTES:

1. The maximum ratings are limited values above which life or satisfactory performance may be impaired.
2. All Diodes must have black body coat.

ITT3001, ITT3002, ITT3003
HIGH VOLTAGE HIGH TEMPERATURE DOUBLE PLUG DIODE

ELECTRICAL CHARACTERISTICS ITT3002 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=200ma
IR_1	Reverse Current		1.0	na	VR=125V
IR_2	Reverse Current (150°C)		3.0	ua	VR=125V
BV	Breakdown Voltage	150		Volts	IR=100ua
C_O	Capacitance		6.0	pf	VR=0V, f=1MHz

ELECTRICAL CHARACTERISTICS ITT3003 (25°C unless otherwise noted)

Parameter		Min	Max	Units	Test Conditions
VF	Forward Voltage		1.0	Volts	IF=100ma
IR_1	Reverse Current		.025	ua	VR=175V
IR_2	Reverse Current (150°C)		5	ua	VR=175V
BV	Breakdown Voltage	200		Volts	IR=100ua

ITT SEMICONDUCTORS

GENERAL PURPOSE SILICON DIODE

This device is a Silicon Double Plug Diode for general-purpose, high-temperature application in computer, industrial and military applications.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... 55°C to +200°C

Lead or terminal temperature at a distance not less than 1/16" from the seated surface (or case) for 2 seconds ..... +275°C

Cross-Reference to Electrical Equivalents

DO-7 Types	DPD Types
1N483B	1N5194
1N485B	1N5195
1N486B	1N5196

	1N5194	1N5195	1N5196
Reverse voltage, 25°C free air	80V	200V	250V
Maximum steady state power dissipation at 25°C, free air	250mw	250mw	250mw
Derating factor	1.43mw/°C	1.43mw/°C	1.43mw/°C

ELECTRICAL CHARACTERISTICS	1N5194		1N5195		1N5196	
	Min	Max	Min	Max	Min	Max
Forward Voltage, Vf @ If=100ma...		1.0V		1.0V		1.0V**
Breakdown Voltage, Bvr Ir=100ua..	80V		200V		250V	
Reverse Current, Ir @ Vr=70V		25na		25na*		25na*
Reverse Current, Ir @ Vr=70V						
@ 150°C		5ua		5ua*		5ua*

**Pulsed—width 8.5 msec max duty cycle 2% or less

*Vr=180V

*Vr=225V

GENERAL PURPOSE SILICON DIODES

This device is a Silicon Double Plug Diode for general purpose use in computer, industrial and military applications.

Cross-Reference to Electrical Equivalents

DO-7 Types	DPD Types
1N457	1N5605
1N458	1N5606
1N459	1N5607
1N658	1N5608
1N660	1N5609

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... −65°C to +200°C

Lead or terminal temperature at a distance not less than 1/16" from the seated surface (or case) for 15 seconds ..... +275°C

	1N5605	1N5606	1N5607	1N5608/9
Reverse voltage, 25°C free air	70V	150V	200V	120V
Maximum steady state power dissipation at 25°C, free air	250mw	200mw	200mw	250mw
Derating factor				2mw/°C

ELECTRICAL CHARACTERISTICS

	1N5605		IN5606*		IN5607*	
	Min	Max	Min	Max	Min	Max
Forward Voltage, Vf @ If=20ma ...		1.0V		1.0V		1.0V
Breakdown Voltage, Bvr Ir=100ua..	70V		150V		200V	
Reverse Current, Ir @ Vr=60V		25na		25na		25na
Reverse Current, Ir @ Vr=60V @ 150°C		5ua		5ua		5ua

*If=7 ma, Vr=125V *If=3 ma. Vr=175V

ELECTRICAL CHARACTERISTICS—1N5608

	Min	Max
Forward Voltage, Vf@If=100ma..		1.0V
Breakdown Voltage, Bvr Ir−100ua	120V	
Reverse Current, Ir@50V		50na
Reverse Current, Ir @ 50V @ 150°C		25ua
*Reverse Recovery Time, Trr If=5 ma, Vr=40V R1=2K, C1=10pf Recover to 80K ohms		30 nsec

ELECTRICAL CHARACTERISTICS—1N5609

	Min	Max
Forward Voltage, Vf@If=6ma....		1.0V
Breakdown Voltage, Bvr Ir=100ua	120V	
Reverse Current, Ir @ 100V		5ua
Reverse Current, Ir @ 100V @ 100°C		50ua
Capacitance, C Vr=10V, f=1 mc		2.7pf
Reverse Recovery time, Trr If=30ma, Vr=35V, Recover to 400K ohms		300nsec

SELENIUM CONTACT PROTECTOR RECTIFIERS

- AC or DC Applications
- Low Cost
- Easy to Install
- Small Size
- Rugged Construction

These ITT selenium cells have been specifically processed for contact protector applications. Their long life, low leakage current and reliable operation provide a low-cost solution to arcing problems in switched inductive devices.

These circuit protectors prevent arcing by effectively suppressing the voltage surges which normally occur during switching. This eliminates the undesirable by-products of arcing, such as contact pitting and erosion, undesirable electrical noise, false triggering of adjacent control circuits or possible insulation breakdown.

ITT selenium cells may be used in a back-to-back arrangement on devices breaking either AC or DC circuits. In AC applications, each arm normally contains the same number of cells; for DC use, a different number of cells is generally specified for each arm.

TYPICAL APPLICATIONS

- Relays
- Stepping Switches
- Electromagnets
- Solenoids
- Small Motors
- Electric Clutches
- Telephone Switching Equipment
- Automobile Clocks & Horns
- Telemetering Equipment
- Magnetic Chucks
- Thermostats
- Electric Brakes
- Solenoid Valves
- Computers

ORDERING INFORMATION

Explanation of part number codes

8A4 P S 1

- 1 — No. of cells in position "A"
- S — "S" indicates DC suppressor; "A" indicates AC suppressor
- P — "P" indicates paper tube; "H" indicates hermetic seal

102 S 2 E X 1

- 1 — No. of cells in position "B"
- X — Finish
- E — No. of cells in position "A"
- S — "S" indicates DC suppressor; "A" indicates AC suppressor

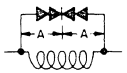


FIG. A

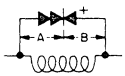


FIG. B

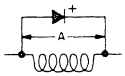


FIG. C

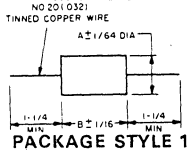
A=BLOCKING SECTION
B=SUPPRESSOR SECTION

Special finishes

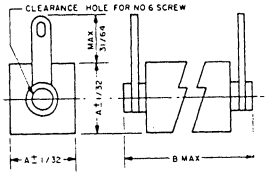
Package style 1 is supplied in a paper tube or in a hermetically sealed can which meets MIL specifications for environmental exposure. Package styles 2, 3 and 4 are supplied with a commercial protective finish. To order special finishes replace the **"X"** in the part number with letters as follows:

"Y" for humidity and salt spray protection
"W" for heavy duty industrial protection
"YF" for humidity, salt spray and fungus protection

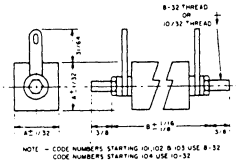
DIMENSIONS



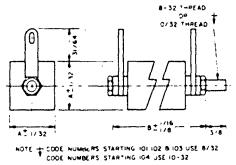
PACKAGE STYLE 1



PACKAGE STYLE 2



PACKAGE STYLE 3



PACKAGE STYLE 4

CHARACTERISTICS

DC APPLICATIONS — 10 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Curren For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	B	ITT Part No.	Package Style	Dimensions A	B
0-30	500		8A1PS0	1	25/64	5/8	8A1HS0*	1	1/2	29/32
	1000		15A1PS0	1	1/2	5/8	15A1HS0*	1	9/16	29/32
0-22	1750		101S1EX0	2	11/16	3/8	101S1AX0	4	11/16	9/16
	4700		102S1EX0	2	1	3/8	102S1AX0	4	1	9/16
	9000		103S1EX0	2	1-1/4	11/32	103S1AX0	4	1-1/4	5/8
	14000		104S1EX0	2	1-17/32	11/32	104S1AX0	4	1-17/32	11/16
31-60	500		8A2PS0	1	25/64	5/8	8A2HS0*	1	1/2	29/32
	1000		15A2PS0	1	1/2	5/8	15A2HS0*	1	9/16	29/32
23-44	1750		101S2EX0	2	11/16	1/2	101S2AX0	4	11/16	11/16
	4700		102S2EX0	2	1	1/2	102S2AX0	4	1	11/16
	9000		103S2EX0	2	1-1/4	1/2	103S2AX0	4	1-1/4	11/16
	14000		104S2EX0	2	1-17/32	1/2	104S2AX0	4	1-17/32	13/16
61-90	500		8A3PS0	1	25/64	5/8	8A3HS0*	1	1/2	29/32
	1000		15A3PS0	1	1/2	5/8	15A3HS0*	1	9/16	29/32
45-66	1750		101S3EX0	2	11/16	9/16	101S3AX0	4	11/16	11/16
	4700		102S3EX0	2	1	5/8	102S3AX0	4	1	27/32
	9000		103S3EX0	2	1-1/4	5/8	103S3AX0	4	1-1/4	13/16
	14000		104S3EX0	2	1-17/32	5/8	104S3AX0	4	1-17/32	31/32
91-120	500		8A4PS0	1	25/64	3/4	8A4HS0*	1	1/2	1-1/32
	1000		15A4PS0	1	1/2	3/4	15A4HS0*	1	9/16	1-1/32
67-88	1750		101S4EX0	2	11/16	5/8	101S4AX0	4	11/16	13/16
	4700		102S4EX0	2	1	11/16	102S4AX0	4	1	7/8
	9000		103S4EX0	2	1-1/4	3/4	103S4AX0	4	1-1/4	15/16
	14000		104S4EX0	2	1-17/32	23/32	104S4AX0	4	1-17/32	1
121-150	500		8A5PS0	1	25/64	3/4	8A5HS0*	1	1/2	1-1/32
	1000		15A5PS0	1	1/2	5/8	15A5HS0*	1	9/16	1-1/32
89-110	1750		101S5EX0	2	11/16	3/4	101S5AX0	4	11/16	1
	4700		102S5EX0	2	1	7/8	102S5AX0	4	1	1-1/16
	9000		103S5EX0	2	1-1/4	1	103S5AX0	4	1-1/4	13/32
	14000		104S5EX0	2	1-17/32	1	104S5AX0	4	1-17/32	1-3/16
151-180	500		8A6PS0	1	25/64	3/4	8A6HS0*	1	1/2	1-1/32
	1000		15A6PS0	1	1/2	15/16	15A6HS0*	1	9/16	1-1/32
111-132	1750		101S6EX0	2	11/16	1	101S6AX0	4	11/16	1-1/16
	4700		102S6EX0	2	1	1	102S6AX0	4	1	1-1/8
	9000		103S6EX0	2	1-1/4	1	103S6AX0	4	1-1/4	1-1/4
	14000		104S6EX0	2	1-17/32	1-1/8	103S6AX0	4	1-17/32	1-5/16
181-210	500		8A7PS0	1	25/64	15/16	8A7HS0*	1	1/2	1-7/32
	1000		15A7PS0	1	1/2	13/16	15A7HS0*	1	9/16	1-7/32
133-154	1750		101S7EX0	2	11/16	1	101S7AX0	4	11/16	1-1/8
	4700		102S7EX0	2	1	1	102S7AX0	4	1	1-1/4
	9000		103S7EX0	2	1-1/4	1-1/2	103S7AX0	4	1-1/4	1-3/8
	14000		104S7EX0	2	1-17/32	1-1/8	104S7AX0	4	1-17/32	1-7/16
211-240	500		8A8PS0	1	25/64	13/16	8A8HS0*	1	1/2	1-7/32
	1000		15A8PS0	1	1/2	13/16	15A8HS0*	1	9/16	1-7/32
155-176	1750		101S8EX0	2	11/16	1-1/8	101S8AX0	4	11/16	1-3/16
	4700		102S8EX0	2	1	1-5/32	102S8AX0	4	1	1-5/16
	9000		103S8EX0	2	1-1/4	1-1/4	103S8AX0	4	1-1/4	1-7/16
	14000		104S8EX0	2	1-17/32	1-1/4	104S8AX0	4	1-17/32	1-1/2
241-270	500		8A9PS0	1	25/64	15/16	8A9HS0*	1	1/2	1-7/32
	1000		15A9PS0	1	1/2	15/16	15A9HS0*	1	9/16	1-7/32
177-198	1750		101S9EX0	2	11/16	1-1/8	101S9AX0	4	11/16	1-1/4
	4700		102S9EX0	2	1	1-1/4	102S9AX0	4	1	1-15/32
	9000		103S9EX0	2	1-1/4	1-3/8	103S9AX0	4	1-1/4	1-9/16
	14000		104S9EX0	2	1-17/32	1-3/8	103S9AX0	4	1-17/32	1-3/8
271-300	500	375	8A10PS0	1	25/64	15/16	8A10HS0*	1	1/2	1-7/32
	1000	750	15A10PS0	1	1/2	15/16	15A10HS0*	1	9/16	1-7/32
199-220	1750	1300	101S10EX0	2	11/16	1-1/4	101S10AX0	4	11/16	1-5/16
	4700	3500	102S10EX0	2	1	1-3/8	102S10AX0	4	1	1-1/2
	9000	6750	103S10EX0	2	1-1/4	1-1/2	103S10AX0	4	1-1/4	1-5/8
	14000	11000	104S10EX0	2	1-17/32	1-1/2	104S10AX0	4	1-17/32	1-11/16
301-330	500	275	8A11PS0	1	25/64	1-1/8	8A11HS0*	1	1/2	1-13/32
	1000	550	15A11PS0	1	1/2	1-1/8	15A11HS0*	1	9/16	1-13/32
221-242	1750	950					101S11AX0	3	11/16	1-5/8
	4700	2600					102S11AX0	3	1	1-13/16
	9000	5000					103S11AX0	3	1-1/4	2
	14000	7750					104S11AX0	3	1-17/32	2-1/16
331-360	500	125	8A12PS0	1	25/64	1-1/8	8A12HS0*	1	1/2	1-13/32
	1000	250	15A12PS0	1	1/2	1-1/8	16A12HS0*	1	9/16	1-13/32
243-264	1750	450					101S12AX0	3	11/16	1-9/16
	4700	1200					102S12AX0	3	1	1-13/16
	9000	2250					103S12AX0	4	1-1/4	2
	14000	3500					104S12AX0	3	1-17/32	2-1/16

mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

DC APPLICATIONS — 40 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-30	250	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PS1	1	25/64	5/8
	600		15A1PS1	1	1/2	5/8
0-22	850		101S1EX1	2	11/16	15/32
0-22	2250		102S1EX1	2	1	15/32
	4300		103S1EX1	2	1-1/4	17/32
	6600		104S1EX1	2	1-17/32	17/32
31-60	250		8A2PS1	1	25/64	5/8
	600		15A2PS1	1	1/2	5/8
23-44	850		101S2EX1	2	11/16	9/16
	2250		102S2EX1	2	1	9/16
	4300		103S2EX1	2	1-1/4	17/32
	6600		104S2EX1	2	1-17/32	19/32
61-90	250		8A3PS1	1	25/64	3/4
	600		15A3PS1	1	1/2	3/4
45-66	850		101S3EX1	2	11/16	17/32
	2250		102S3EX1	2	1	9/16
	4300		103S3EX1	2	1-1/4	23/32
	6600		104S3EX1	2	1-17/32	23/32
91-120	250		8A4PS1	1	25/64	3/4
	600		15A4PS1	1	1/2	3/4
67-88	850		101S4EX1	2	11/16	21/32
	2250		102S4EX1	2	1	1
	4300		103S4EX1	2	1-1/4	1
	6600		104S4EX1	2	1-17/32	3/4
121-150	250		8A5PS1	1	25/64	3/4
	600		15A5PS1	1	1/2	3/4
89-110	850		101S5EX1	2	11/16	13/16
	2250		102S5EX1	2	1	7/8
	4300		103S5EX1	2	1-1/4	1-1/8
	6600		104S5EX1	2	1-17/32	1-1/8
151-180	250		8A6PS1	1	25/64	15/16
	600		15A6PS1	1	1/2	15/16
111-132	850		101S6EX1	2	11/16	1
	2250		102S6EX1	2	1	1
	4300		103S6EX1	2	1-1/4	1-1/8
	6600		104S6EX1	2	1-17/32	1-1/8
181-210	250		8A7PS1	1	25/64	15/16
	600		15A7PS1	1	1/2	15/16
133-154	850		101S7EX1	2	11/16	1-1/8
	2250		102S7EX1	2	1	31/32
	4300		103S7EX1	2	1-1/4	1-1/4
	6600		104S7EX1	2	1-17/32	1-1/4
211-240	250		8A8PS1	1	25/64	15/16
	600		15A8PS1	1	1/2	15/16
155-176	850		101S8EX1	2	11/16	1-1/8
	2250		102S8EX1	2	1	1-1/4
	4300		103S8EX1	2	1-1/4	1-3/8
	6600		104S8EX1	2	1-17/32	1-1/4
241-270	250		8A9PS1	1	25/64	15/16
	600		15A9PS1	1	1/2	15/16
177-198	850		101S9EX1	2	11/16	1-1/4
	2250		102S9EX1	2	1	1-3/8
	4300		103S9EX1	2	1-1/4	1-1/2
	6600		104S9EX1	2	1-17/32	1-1/2
271-300	250		8A10PS1	1	25/64	1-1/8
	600		15A10PS1	1	1/2	1-1/8
199-220	850					
	2250					
	4300					
	6600					
301-330	250		8A11PS1	1	25/64	1-1/8
	600		15A11PS1	1	1/2	1-1/8
221-242	850					
	2250					
	4300					
	6600					
331-360	250		8A12PS1	1	25/64	1-1/8
	600		15A12PS1	1	1/2	1-1/16
243-264	850					
	2250					
	4300					
	6600					

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B
			8A1HS1*	1	1/2	29/32
			15A1HS1*	1	9/16	29/32
			101S1AX1	4	11/16	5/8
			102S1AX1	4	1	25/32
			103S1AX1	4	1-1/4	3/4
			104S1AX1	4	1-17/32	13/16
			8A2HS1*	1	1/2	29/32
			15A2HS1*	1	9/16	29/32
			101S2AX1	4	11/16	1-3/16
			102S2AX1	4	1	29/32
			103S2AX1	4	1-1/4	3/4
			104S2AX1	4	1-17/32	7/8
			8A3HS1*	1	1/2	1-1/32
			15A3HS1*	1	9/16	1-1/32
			101S3AX1	4	11/16	1
			102S3AX1	4	1	1-1/32
			103S3AX1	4	1-1/4	25/32
			104S3AX1	4	1-17/32	1
			8A4HS1*	1	1/2	1-1/32
			15A4HS1*	1	9/16	1-1/32
			101S4AX1	4	11/16	1
			102S4AX1	4	1	1
			103S4AX1	4	1-1/4	1-1/16
			104S4AX1	4	1-17/32	1-1/8
			8A5HS1*	1	1/2	1-1/32
			15A5HS1*	1	9/16	1-1/32
			101S5AX1	4	11/16	1-1/16
			102S5AX1	4	1	1-1/8
			103S5AX1	4	1-1/4	1-1/4
			104S5AX1	4	1-17/32	1-3/8
			8A6HS1*	1	1/2	1-7/32
			15A6HS1*	1	9/16	1-7/32
			101S6AX1	4	11/16	1-1/8
			102S6AX1	4	1	1-1/4
			103S6AX1	4	1-1/4	1-3/8
			104S6AX1	4	1-17/32	1-7/16
			8A7HS1*	1	1/2	1-7/32
			15A7HS1*	1	9/16	1-7/32
			101S7AX1	4	11/16	1-3/16
			102S7AX1	4	1	1-5/16
			103S7AX1	4	1-1/4	1-7/16
			104S7AX1	4	1-17/32	1-9/16
			8A8HS1*	1	1/2	1-7/32
			15A8HS1*	1	9/16	1-7/32
			101S8AX1	4	11/16	1-1/4
			102S8AX1	4	1	1-7/16
			103S8AX1	4	1-1/4	1-9/16
			104S8AX1	4	1-17/32	1-5/8
			8A9HS1*	1	1/2	1-7/32
			15A9HS1*	1	9/16	1-7/32
			101S9AX1	4	11/16	1-15/16
			102S9AX1	4	1	1-1/2
			103S9AX1	4	1-1/4	1-5/8
			104S9AX1	4	1-17/32	1-3/4
			8A10HS1*	1	1/2	1-13/32
			15A10HS1*	1	9/16	1-13/32
			101S10AX1	3	11/16	1-5/8
			102S10AX1	3	1	1-13/16
			103S10AX1	3	1-1/4	1-7/8
			104S10AX1	3	1-17/32	2-1/16
			8A11HS1*	1	1/2	1-13/32
			15A11HS1*	1	9/16	1-13/32
			101S11AX1	3	11/16	1-5/8
			102S11AX1	3	1	1-7/8
			103S11AX1	3	1-1/4	2
			104S11AX1	3	1-17/32	2-1/16
			8A12HSA*	1	1/2	1-13/32
			15A12HS1*	1	9/16	1-13/32
			101S12AX1	3	11/16	1-5/8
			102S12AX1	3	1	1-7/8
			103S12AX1	3	1-1/4	2-1/16
			104S12AX1	3	1-17/32	2-3/16

AC APPLICATIONS

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-26	200	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PA1	1	25/64	5/8
	400		15A1PA1	1	1/2	5/8
	600		101A1EX1	2	11/16	15/32
	1600		102A1EX1	2	1	15/32
	3000		103A1EX1	2	1-1/4	1/2
	4700		104A1EX1	2	1-17/32	17/32
27-52	200	200	8A2PA2	1	25/64	5/8
	400	400	15A2PA2	1	1/2	3/4
	600	600	101A2EX2	2	11/16	1/2
	1600	1600	102A2EX2	2	1	11/16
	3000	3000	103A2EX2	2	1-1/4	11/16
	4700	4700	104A2EX2	2	1-17/32	23/32
53-78	200	60	8A3PA3	1	25/64	3/4
	400	140	15A3PA3	1	1/2	3/4
	600	250	101A3EX3	2	11/16	13/16
	1600	650	102A3EX3	2	1	7/8
	3000	1200	103A3EX3	2	1-1/4	1-3/16
	4700	2000	104A3EX3	2	1-17/32	1
			8A3HA3*	1	1/2	1-1/32
			15A3HA3*	1	9/16	1-1/32
			101A3AX3	4	11/16	27/32
			102A3AX3	3	1	1-7/16
			103A3AX3	4	1-1/4	1-1/4
			104A3AX3	4	1-17/32	1-5/16
			8A4HA4*	1	1/2	1-7/32
			15A4HA4*	1	9/16	1-7/32
			101A4AX4	3	11/16	1-3/16
			102A4AX4	4	1	29/32
			103A4AX4	4	1-1/4	1-1/4
			104A4AX4	4	1-17/32	1-1/2
			8A5HA5*	1	1/2	1-7/32
			15A5HA5*	1	9/16	1-7/32
			101A5AX5	4	11/16	1-1/8
			102A5AX5	3	1	1-5/8
			103A5AX5	4	1-1/4	1-7/16
			104A5AX5	3	1-17/32	1-7/8

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B
79-104	200	15	8A4PA4	1	25/64	15/16
	400	35	15A4PA4	1	1/2	15/16
	600	60	101A4EX4	2	11/16	29/32
	1600	160	102A4EX4	2	1	31/32
	3000	300	103A4EX4	2	1-1/4	1-5/32
	4700	470	104A4EX4	2	1-17/32	1-5/32
105-130	200	10	8A5PA5	1	25/64	15/16
	400	20	15A5PA5	1	1/2	15/16
	600	30	101A5EX5	2	11/16	1-1/8
	1600	80	102A5EX5	2	1	1-11/32
	3000	150	103A5EX5	2	1-1/4	1-1/4
	4700	250	104A5EX5	2	1-17/32	1-13/32
			8A4HA4*	1	1/2	1-7/32
			15A4HA4*	1	9/16	1-7/32
			101A4AX4	3	11/16	1-3/16
			102A4AX4	4	1	29/32
			103A4AX4	4	1-1/4	1-1/4
			104A4AX4	4	1-17/32	1-1/2
			8A5HA5*	1	1/2	1-7/32
			15A5HA5*	1	9/16	1-7/32
			101A5AX5	4	11/16	1-1/8
			102A5AX5	3	1	1-5/8
			103A5AX5	4	1-1/4	1-7/16
			104A5AX5	3	1-17/32	1-7/8

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

CAUSE OF CONTACT ARCING

Consider the circuit shown in **Figure 1.** Close the circuit contacts S_1 and the current flow as indicated by the ammeter M_1 builds up to 400 mA. The flow of current has set up a magnetic field through the core. Electrical energy has been stored in the magnetic field by the current, analogous to the mechanical energy stored in a spring by compression.

Now open the contacts S_1 thus breaking the steady flow of current. Just as the compressed spring will start to release its stored mechanical energy, the magnetic field starts to collapse, releasing its stored energy. While the magnetic field is collapsing it induces a voltage in the coil that acts to maintain the current through the coil in the same direction as the original current which built up the field. The magnitude of this induced voltage is equal to the product of the coil current, and the coil and circuit resistance; and it can attain very high values since the circuit resistance approaches infinity with the switch contacts open.

Theoretically, when the flow of current is suddenly stopped by the opening of S_1, the voltage that appears across the coil could go up to infinity. Approximately 300 volts is required to produce arcing across contacts in free air. Since air is not a perfect insulator, the instant that S_1 is opened and the high induced voltage appears across the contacts, an arc occurs. In typical applications, air breakdown across the contacts will limit the voltage rise to the region of 300 to 1,000 volts in an average 24-volt coil circuit. **See Figure 2.**

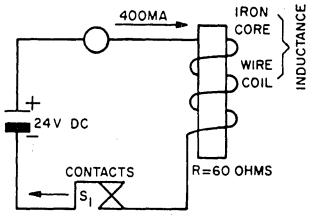


FIG. 1

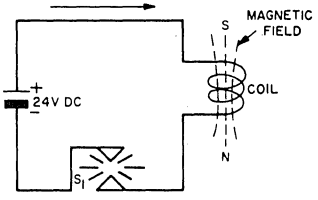


FIG. 2

HOW ITT SELENIUM CONTACT PROTECTORS WORK

Half-wave configuration for DC applications

Consider the circuit of **Figure 3,** showing contact protector cell A connected across the coil terminals. While contacts S_1 are held closed a current of 400 milliamperes flows through the coil, but no part of the coil current flows through the contact protector. When S_1 is opened coil current flows in the low-resistance direction of the contact protector, thus dissipating the energy stored in the coil through the resistance of the coil and contact protector. As the resistance of the contact protector is very low, usually a fraction of the coil resistance, the voltage across the contacts rises only slightly, to a few volts above battery voltage.

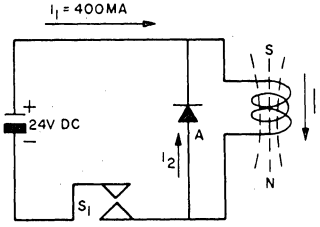


FIG. 3

Half-wave configuration, continued

In the circuit shown in **Figure 4,** cell B has been added in such a direction as to oppose the discharge current I_2. A semiconductor cell has the unique characteristic of exhibiting decreasing resistance with increasing voltage in the blocking direction.

At the instant switch S_1 is opened, the induced voltage rises to approximately 150 volts, due to the blocking action of cell B. This induced voltage is indicated in **Figure 4** and appears as a reverse voltage across cell B, i.e., the high-resistance direction.

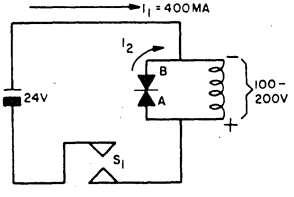


FIG. 4

Figure 5 shows the change in reverse resistance with application of reverse voltage to a typical semiconductor contact-protector cell. At the working voltage of 24 volts, the reverse resistance is approximately 1 megohm. When S_1 is opened, the voltage across the coil builds up to approximately −200 volts. At this voltage the reverse resistance of cell B will be less than 500 ohms. Much of the stored energy is dissipated in this low-resistance region of the cell characteristic.

As the energy is dissipated and the current decreases, the induced voltage also decreases. The remainder of the stored energy is dissipated in a higher-resistance region than initially. For example, as the induced voltage decays to −25 volts, the cell resistance rises to approximately one megohm.

Thus the effect of the nonlinear resistance of cell B is to provide, at the instant of switching, a path of relatively low resistance to prevent the induced voltage from rising to a value which will cause arcing. As the stored energy is dissipated the low resistance increases, due to the nature of the cell characteristics, and provides a damping effect on the discharge current. The result is to reduce the coil release time as compared to the action of the half-wave-type contact protector.

Figure 6. Oscillograph trace voltage across a set of contacts breaking the circuit of a 48-volt telephone relay, without contact protection. Sparking begins at 300 volts (see oscillations), continues as contacts are separated and rises to a voltage peak at 500 volts. Voltage decay is exponential.

Figure 7. Oscillograph trace of voltage across same set of contacts, protected by ITT half-wave semiconductor contact protector.

Figure 8. Oscillograph trace of voltage across same set of contacts, protected by ITT back-to-back semiconductor contact protector.

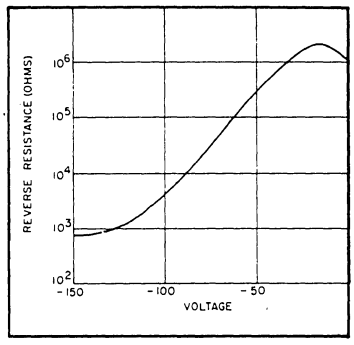


FIG. 5

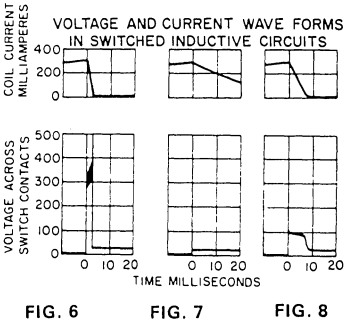


FIG. 6 FIG. 7 FIG. 8

Back-to-back configuration for AC applications

The back-to-back configuration is readily adapted to use in AC circuits by providing the same number of cells in each arm of the device. The number of cells in series per arm will depend on the applied AC voltage. The requirement for the same number of cells in each arm arises from the fact that both arms alternately are required to block the input voltage. This arrangement differs from the DC back-to-back configuration in which one arm has sufficient cells to block the battery voltage and the other has only one or two cells to provide the surge suppression.

Factors relating to the opening of inductive circuits

It can be shown mathematically that the time required for the coil current to drop to zero, after the switch contacts have opened, is inversely proportional to the sum of the coil resistance and protector resistance. Also, the magnitude of the voltage induced in the coil at the instant of switching is directly proportional to the sum of these resistances.

When the circuit energizing an inductance is opened the polarity of the voltage across the coil is reversed and is indicated by the equation $E = -L\frac{di}{dt}$

After the circuit opens, and assuming no arcing occurs, the time for the current to fall to a percentage of its initial value is given by the following equation:

$$t = \frac{-L}{R_L + r} \log \frac{i}{EI}$$

When R = Coil resistance
r = Forward resistance of rectifier
L = Inductance of coil
t = Time for current to decrease to i
i = Current at time t
I = Steady-state current through the coil
E = Supply voltage

The voltage induced across the coil is expressed by the equation

$$V = -L\frac{di}{dt} = (R_L + r)\, I_E - \frac{R_L + r}{L}t$$

The maximum value of voltage V occurs when t = 0 V max. = I(R+r) = E+Ir

In an inductive circuit with unprotected switch contacts, the coil current decays through a path that includes the widening air gap between the moving contacts. The high resistance of this gap results in a very short current decay time. However, the voltage induced in the coil at the instant of switching must reach a value high enough to force the current across the air gap. This leads to the electrical breakdown of the air gap with attendant arcing, contact damage and electrical noise.

In the half-wave configuration the resistance of the protector is low when it is acting as a suppressor, since the coil current flows in the low-resistance forward direction of the device. The forward resistance of the half-wave suppressor will usually be only a small fraction of the coil resistance and, for practical purposes, may be regarded as a short circuit around the coil. The low value of protector resistance prevents the induced voltage from rising more than a volt or two over the battery voltage, and increases the current decay time compared to the decay time of a coil with unprotected contacts.

In the back-to-back configuration the reverse resistance of the protector is inversely proportional to the induced voltage. This resistance will be the smallest at the instant of switching and will increase in value as the current decreases. This nonlinear resistance characteristic causes the induced voltage to rise to a value higher than it would reach in a circuit using the half-wave configuration, but it prevents the induced voltage from attaining the contact-damaging values existing in a circuit with unprotected contacts. Although the current decay time is increased somewhat compared to the decay time of a coil with unprotected contacts, it is very appreciably shorter than the decay time of a circuit using the half-wave configuration.

APPLICATION NOTES

Voltage Range

The words "voltage range" are used because the maximum voltage rating increases in discrete steps, according to the number of blocking cells in series. Each protector has a maximum permissible voltage rating which is the low-voltage end of the range for the next higher voltage group.

Max. Coil Current – mA

The maximum permissible coil current is based on the thermal dissipation characteristics of the contact protector when operated at maximum coil voltage and repetition rate.

Coil Current for 300-V Max. Rise – mA

At the instant of switching, the current through the protector is the same as the coil current, and the induced voltage at the coil terminals will rise to the value required to drive this current through the protector. This voltage will add to the supply voltage and appear across the contacts. Sparking at the contacts will be minimized if the sum of these two voltages does not exceed 300 volts, and this requirement is met if the induced voltage is no greater than the difference between 300 and the supply voltage. This condition is achieved by reducing, for a given cell size, the permissible coil current as the supply voltage increases. Thus, it will be observed that the coil current for 300-volt rise will be less than the maximum coil current for many of the higher-voltage units. Conversely, the coil current for 300-volt rise is so great that it exceeds the maximum coil current for the low-voltage units. These protectors carry the note in the rating table "MA for 300-Volt Rise Exceeds Max. Current Rating"; this means that operation at the listed maximum coil current will give a voltage rise of less than 300 volts at the contacts.

The current values listed in the column "Coil Current for 300-V Max. Rise" are representative values, based on the observation of typical relays and solenoids. The specific value of current that will limit the voltage at the contacts to 300 volts is a function of the coil design, the size of the coil, the number of turns of wire, etc., and it is possible for a contact protector to furnish adequate spark suppression when used with coils carrying currents greater than those listed; but the maximum current rating should not be exceeded. For this reason, it is wise to observe the action and efficiency of the protector before freezing a design. Samples and engineering assistance are available upon written request to the Engineering Department.

In selecting a suitable Contact Protector from the list in this data sheet, it should be noted:

Ratings are based upon operation in typical inductive circuits at temperatures of 50°C or lower. Current ratings given in the column headed "Coil Steady State Current for 300 volt max. rise" represent the rating of the protector to limit the voltage rise across the contacts to approximately 300 volts. This rating may be exceeded if a rise in excess of 300 volts is permissible, but the maximum peak current rating should not be exceeded. The voltage rating should not be exceeded under any circumstances.

Fast Contact Action

Rate of operation of contacts in the range 10 to 40 breaks per second. The back-to-back arrangement of the ITT Contact Protector provides adequate arc suppression with a negligible effect upon the release time of the relay. The protectors are fated for applications where the rate of operation of the contacts is in the range of 10 to 40 breaks per second. ITT should be consulted for recommendations if the rate of operation exceeds 40 breaks per second.

TRANSIENT VOLTAGE SUPPRESSOR RECTIFIERS

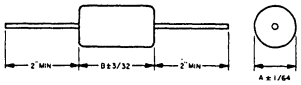
- **AC Input or DC Applications**
- **Improve Equipment Reliability**
- **Reduce Equipment Cost**

ITT transient voltage suppressors eliminate one of the major causes of failure of semiconductor rectifiers by instantaneously short-circuiting transient voltages in excess of the ratings of the rectifiers. They permit the circuit designer to use rectifiers with lower PIV ratings, thereby reducing equipment cost. These specially processed selenium cells have very sharp "zener" breakdown characteristics when operated in the reverse direction. Since the reverse characteristic is used instead of the forward characteristic, aging has very little effect on the resistance and suppressing voltage level of the protector. The small effects of aging and temperature variations have been taken into consideration in the volt-ampere curves and tabulated characteristics.

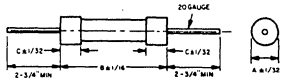
In inductive circuits using mechanical switches, these suppressors can be used to eliminate pitting of the switch contacts by absorbing the high peak voltages generated when the switch is opened. ITT contact protector selenium rectifiers can also be used in this application.

Transient voltage suppressors can be mounted by eyelets or studs in stack types and by clips or pigtail leads in tubular types. Stack types are supplied with a standard industrial finish or with a moisture resistant finish for protection against salt spray and humidity.

DIMENSIONS



PAPER TUBE TYPE



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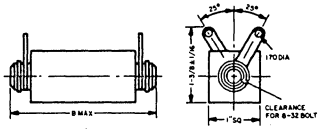
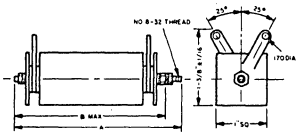


EYELET TYPE



STUD TYPE

RATINGS

CHARACTERISTICS	8A SERIES	25A SERIES	102 SERIES	UNITS
Steady State RMS Volts/Cell	30	30	25	Volts
Peak Volts/Cell	42.4	42.4	35	Volts
DC Volts/Cell	20	20	20	Volts
Stack RMS Volts	30-600	36-600	25-500	Volts
Stack DC Volts	20-400	20-400	20-320	Volts
Steady State Leakage Current (max.)	0.8	1.2	12	mA
Single Pulse Current (4 milliseconds) (max.)	0.75	2	8	Amps
Recurrent Pulse Current (1 millisecond @ 60 cps) (max.)	0.25	0.75	3	Amps
Ambient Temperature	—20 to +100	—20 to +100	—20 to +100	°C
Cell Operating Temperature (max.)	130	130	130	°C
Construction	Tubular	Tubular	Stud or Eyelet	

ELECTRICAL AND MECHANICAL CHARACTERISTICS – AC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	104	3/8	27/32	8A1PG1
60	85	208	3/8	27/32	8A2PG2
90	127	312	3/8	27/32	8A3PG3
120	170	416	3/8	27/32	8A4PG4
150	212	519	3/8	27/32	8A5PG5
180	254	623	3/8	1 3/32	8A6PG6
210	297	727	3/8	1 3/32	8A7PG7
240	339	831	3/8	1 3/32	8A8PG8
270	382	934	3/8	1 3/32	8A9PG9
300	424	1039	3/8	1 3/32	8A10PG10
330	467	1143	3/8	1 21/64	8A11PG11
360	509	1247	3/8	1 21/64	8A12PG12
390	551	1350	3/8	1 21/64	8A13PG13
420	594	1454	3/8	1 21/64	8A14PG14
450	636	1558	3/8	1 21/64	8A15PG15
480	679	1663	3/8	1 37/64	8A16PG16
510	721	1766	3/8	1 37/64	8A17PG17
540	764	1870	3/8	1 37/64	8A18PG18
570	806	1974	3/8	1 37/64	8A19PG19
600	848	2078	3/8	1 37/64	8A20PG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	87	37/64	1 1/64	25A1PG1
60	85	177	37/64	1 1/64	25A2PG2
90	127	266	37/64	1 1/64	25A3PG3
120	170	354	37/64	1 1/64	25A4PG4
150	212	443	37/64	1 1/64	25A5PG5
180	254	532	37/64	1 1/4	25A6PG6
210	297	620	37/54	1 1/4	25A7PG7
240	339	709	37/64	1 1/4	25A8PG8
270	382	798	37/64	1 1/4	25A9PG9
300	424	886	37/64	1 1/4	25A10PG10
330	467	975	37/64	1 1/2	25A11PG11
360	509	1063	37/64	1 1/2	25A12PG12
390	551	1152	37/64	1 1/2	25A13PG13
420	594	1241	37/64	1 1/2	25A14PG14
450	636	1329	37/64	1 1/2	25A15PG15
480	679	1417	37/64	1 3/4	25A16PG16
510	721	1507	37/64	1 3/4	25A17PG17
540	764	1595	37/64	1 3/4	25A18PG18
570	806	1684	37/64	1 3/4	25A19PG19
600	848	1772	37/64	1 3/4	25A20PG20

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	15/32	31/32	3/8	8A1QBG1	8A1ABG1
60	85	208	15/32	31/32	3/8	8A2QBG2	8A2ABG2
90	127	312	15/32	31/32	3/8	8A3QBG3	8A3ABG3
120	170	416	15/32	31/32	3/8	8A4QBG4	8A4ABG4
150	212	519	15/32	31/32	3/8	8A5QBG5	8A5ABG5
180	254	623	15/32	31/32	3/8	8A6QBG6	8A6ABG6
210	297	727	15/32	31/32	3/8	8A7QBG7	8A7ABG7
240	339	831	15/32	31/32	3/8	8A8QBG8	8A8ABG8
270	382	934	15/32	31/32	3/8	8A9QBG9	8A9ABG9
300	424	1039	15/32	31/32	3/8	8A10QBG10	8A10ABG10
330	467	1143	15/32	1 17/64	3/8	8A11QBG11	8A11ABG11
360	509	1247	15/32	1 17/64	3/8	8A12QBG12	8A12ABG12
390	551	1350	15/32	1 17/64	3/8	8A13QBG13	8A13ABG13
420	594	1454	15/32	1 17/64	3/8	8A14QBG14	8A14ABG14
450	636	1558	15/32	1 17/64	3/8	8A15QBG15	8A15ABG15
480	679	1662	15/32	1 1/2	3/8	8A16QBG16	8A16ABG16
510	721	1766	15/32	1 1/2	3/8	8A17QBG17	8A17ABG17
540	764	1870	15/32	1 1/2	3/8	8A18QBG18	8A18ABG18
570	806	1974	15/32	1 1/2	3/8	8A19QBG19	8A19ABG19
600	848	2078	15/32	1 1/2	3/8	8A20QBG20	8A20ABG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	31/32	1 1/32	13/32	25A1QBG1	25A1ABG1
60	85	208	31/32	1 1/32	13/32	25A2QBG2	25A2ABG2
90	127	312	31/32	1 1/32	13/32	25A3QBG3	25A3ABG3
120	170	416	31/32	1 1/32	13/32	25A4QBG4	25A4ABG4
150	212	519	31/32	1 1/32	13/32	25A5QBG5	25A5ABG5
180	254	623	31/32	1 1/32	13/32	25A6QBG6	25A6ABG6
210	297	727	31/32	1 1/32	13/32	25A7QBG7	25A7ABG7
240	339	831	31/32	1 1/32	13/32	25A8QBG8	25A8ABG8
270	382	934	31/32	1 1/32	13/32	25A9QBG9	25A9ABG9
300	424	1039	31/32	1 1/32	13/32	25A10QBG10	25A10ABG10
330	467	1143	31/32	1 29/64	13/32	25A11QBG11	25A11ABG11
360	509	1247	31/32	1 29/64	13/32	25A12QBG12	25A12ABG12
390	551	1350	31/32	1 29/64	13/32	25A13QBG13	25A13ABG13
420	594	1454	31/32	1 29/64	13/32	25A14QBG14	25A14ABG14
450	636	1558	31/32	1 29/64	13/32	25A15QBG15	25A15ABG15
480	679	1662	31/32	1 11/16	13/32	25A16QBG16	25A16ABG16
510	721	1766	31/32	1 11/16	13/32	25A17QBG17	25A17ABG17
540	764	1870	31/32	1 11/16	13/32	25A18QBG18	25A18ABG18
570	806	1974	31/32	1 11/16	13/32	25A19QBG19	25A19ABG19
600	848	2078	31/32	1 11/16	13/32	25A20QBG20	25A20ABG20

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS LENGTH (B)	ITT PART NO.
25	35	80	47/64	102G1EX1
50	70	159	13/16	102G2EX2
75	105	239	57/64	102G3EX3
100	140	319	31/32	102G4EX4
125	175	398	1 3/64	102G5EX5
150	210	478	1 1/8	102G6EX6
175	245	558	1 13/64	102G7EX7
200	280	637	1 19/64	102G8EX8

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
25	35	80	1 7/16	15/16	102G1BX1
50	70	159	1 1/2	1	102G2BX2
75	105	239	1 5/8	1 1/8	102G3BX3
100	140	319	1 11/16	1 3/16	102G4BX4
125	175	398	1 3/4	1 1/4	102G5BX5
150	210	478	1 7/8	1 3/8	102G6BX6
175	245	558	1 15/16	1 7/16	102G7BX7
200	280	637	2	1 1/2	102G8BX8
225	315	717	2 1/16	1 9/16	102G9BX9
250	350	797	2 3/16	1 11/16	102G10BX10
275	385	876	2 1/4	1 3/4	102G11BX11
300	420	956	2 5/16	1 13/16	102G12BX12
325	455	1035	2 3/8	1 7/8	102G13BX13
350	490	1115	2 1/2	2	102G14BX14
375	525	1195	2 9/16	2 1/16	102G15BX15
400	560	1274	2 5/8	2 1/8	102G16BX16
425	595	1354	2 3/4	2 1/4	102G17BX17
450	630	1434	2 13/16	2 5/16	102G18BX18
475	665	1513	2 7/8	2 3/8	102G19BX19
500	700	1593	2 15/16	2 7/16	102G20BX20
600	840	1913	3 5/16	2 13/16	102G24BX24

NOTES: 1. At 4 millisecond pulse current=0.75 Amperes
2. At 4 millisecond pulse current=2 Amperes
3. At 4 millisecond pulse current=8 Amperes

ELECTRICAL AND MECHANICAL CHARACTERISTICS – DC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	104	3/8	27/32	8A1PG0
40	63	208	3/8	27/32	8A2PG0
60	93	312	3/8	27/32	8A3PG0
80	126	416	3/8	27/32	8A4PG0
100	157	519	3/8	27/32	8A5PG0
120	188	623	3/8	27/32	8A6PG0
140	220	727	3/8	27/32	8A7PG0
160	251	831	3/8	27/32	8A8PG0
180	282	934	3/8	27/32	8A9PG0
200	314	1039	3/8	27/32	8A10PG0
220	345	1143	3/8	1 3/32	8A11PG0
240	377	1247	3/8	1 3/32	8A12PG0
260	409	1350	3/8	1 3/32	8A13PG0
280	440	1454	3/8	1 3/32	8A14PG0
300	472	1558	3/8	1 3/32	8A15PG0
320	502	1662	3/8	1 3/32	8A16PG0
340	534	1766	3/8	1 3/32	8A17PG0
360	566	1870	3/8	1 3/32	8A18PG0
380	597	1974	3/8	1 3/32	8A19PG0
400	628	2078	3/8	1 3/32	8A20PG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	87	37/64	1 1/64	25A1PG0
40	63	177	37/64	1 1/64	25A2PG0
60	93	266	37/64	1 1/64	25A3PG0
80	126	354	37/64	1 1/64	25A4PG0
100	157	443	37/64	1 1/64	25A5PG0
120	188	532	37/64	1 1/64	25A6PG0
140	220	620	37/64	1 1/64	25A7PG0
160	251	709	37/64	1 1/64	25A8PG0
180	282	798	37/64	1 1/64	25A9PG0
200	314	886	37/64	1 1/64	25A10PG0
220	345	975	37/64	1 1/4	25A11PG0
240	377	1063	37/64	1 1/4	25A12PG0
260	409	1152	37/64	1 1/4	25A13PG0
280	440	1241	37/64	1 1/4	25A14PG0
300	472	1329	37/64	1 1/4	25A15PG0
320	502	1417	37/64	1 1/4	25A16PG0
340	534	1507	37/64	1 1/4	25A17PG0
360	566	1595	37/64	1 1/4	25A18PG0
380	597	1684	37/64	1 1/4	25A19PG0
400	628	1772	37/64	1 1/4	25A20PG0

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	15/32	31/32	3/8	8A1QBG0	8A1ABG0
40	63	208	15/32	31/32	3/8	8A2QBG0	8A2ABG0
60	93	312	15/32	31/32	3/8	8A3QBG0	8A3ABG0
80	126	416	15/32	31/32	3/8	8A4QBG0	8A4ABG0
100	157	519	15/32	31/32	3/8	8A5QBG0	8A5ABG0
120	188	623	15/32	31/32	3/8	8A6QBG0	8A6ABG0
140	120	727	15/32	31/32	3/8	8A7QBG0	8A7ABG0
160	251	831	15/32	31/32	3/8	8A8QBG0	8A8ABG0
180	282	934	15/32	31/32	3/8	8A9QBG0	8A9ABG0
200	314	1039	15/32	31/32	3/8	8A10QBG0	8A10ABG0
220	345	1143	15/32	31/32	3/8	8A11QBG0	8A11ABG0
240	377	1247	15/32	31/32	3/8	8A12QBG0	8A12ABG0
260	409	1350	15/32	31/32	3/8	8A13QBG0	8A13ABG0
280	440	1454	15/32	31/32	3/8	8A14QBG0	8A14ABG0
300	472	1558	15/32	31/32	3/8	8A15QBG0	8A15ABG0
320	502	1662	15/32	31/32	3/8	8A16QBG0	8A16ABG0
340	534	1766	15/32	31/32	3/8	8A17QBG0	8A17ABG0
360	566	1870	15/32	31/32	3/8	8A18QBG0	8A18ABG0
380	597	1974	15/32	31/32	3/8	8A19QBG0	8A19ABG0
400	628	2078	15/32	31/32	3/8	8A20QBG0	8A20ABG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	31/32	1 1/32	13/32	25A1QBG0	25A1ABG0
40	63	208	31/32	1 1/32	13/32	25A2QBG0	25A2ABG0
60	93	312	31/32	1 1/32	13/32	25A3QBG0	25A3ABG0
80	126	416	31/32	1 1/32	13/32	25A4QBG0	25A4ABG0
100	157	519	31/32	1 1/32	13/32	25A5QBG0	25A5ABG0
120	188	623	31/32	1 1/32	13/32	25A6QBG0	25A6ABG0
140	220	727	31/32	1 1/32	13/32	25A7QBG0	25A7ABG0
160	251	831	31/32	1 1/32	13/32	25A8QBG0	25A8ABG0
180	282	934	31/32	1 1/32	13/32	25A9QBG0	25A9ABG0
200	314	1039	31/32	1 1/32	13/32	25A10QBG0	25A10ABG0
220	345	1143	31/32	1 1/32	13/32	25A11QBG0	25A11ABG0
240	377	1247	31/32	1 1/32	13/32	25A12QBG0	25A12ABG0
260	409	1350	31/32	1 1/32	13/32	25A13QBG0	25A13ABG0
280	440	1454	31/32	1 1/32	13/32	25A14QBG0	25A14ABG0
300	472	1558	31/32	1 1/32	13/32	25A15QBG0	25A15ABG0
320	502	1662	31/32	1 1/32	13/32	25A16QBG0	25A16ABG0
340	534	1766	31/32	1 1/32	13/32	25A17QBG0	25A17ABG0
360	566	1870	31/32	1 1/32	13/32	25A18QBG0	25A18ABG0
380	597	1974	31/32	1 1/32	13/32	25A19QBG0	25A19ABG0
400	628	2078	31/32	1 1/32	13/32	25A20QBG0	25A20ABG0

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	80	27/32	102G1EX0
40	63	159	7/8	102G2EX0
60	93	239	29/32	102G3EX0
80	126	319	15/16	102G4EX0
100	157	398	1	102G5EX0
120	188	478	1 1/32	102G6EX0
140	220	558	1 1/16	102G7EX0
160	251	637	1 1/8	102G8EX0
180	282	717	1 5/32	102G9EX0
200	314	795	1 3/16	102G10EX0
220	345	876	1 1/4	102G11EX0
240	377	956	1 9/32	102G12EX0
260	409	1035	1 5/16	102G13EX0
280	440	1115	1 11/32	102G14EX0
300	472	1195	1 3/8	102G15EX0
320	502	1274	1 7/16	102G16EX0

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
20	31	80	1 5/16	13/16	102G1BX0
40	63	159	1 3/8	27/32	102G2BX0
60	93	239	1 3/8	7/8	102G3BX0
80	126	319	1 7/16	29/32	102G4BX0
100	157	398	1 1/2	15/16	102G5BX0
120	188	478	1 5/8	1 3/32	102G6BX0
140	220	558	1 5/8	1 1/8	102G7BX0
160	251	637	1 11/16	1 3/16	102G8BX0
180	282	717	1 3/4	1 7/32	102G9BX0
200	314	797	1 3/4	1 1/4	102G10BX0
220	345	876	1 13/16	1 9/32	102G11BX0
240	377	956	1 7/8	1 11/32	102G12BX0
260	409	1035	1 15/16	1 3/8	102G13BX0
280	440	1115	1 15/16	1 13/32	102G14BX0
300	472	1195	1 15/16	1 15/32	102G15BX0
320	502	1274	2	1 1/2	102G16BX0

NOTES: 1. At 4 millisecond pulse current=0.75 Amperes
2. At 4 millisecond pulse current=2 Amperes
3. At 4 millisecond pulse current=8 Amperes

HOW TO SELECT THE PROPER RECTIFIER

Determination of Current Rating

Although the peak value and duration of a transient current cannot always be determined, certain valid assumptions can be made to determine the ITT suppressor rectifier current rating for the application.

For circuits in which a transformer is the power source, usually the greatest transient currents have been observed when the circuit is interrupted with no load on the transformer. The transient current is the magnetizing current of the transformer. If the actual transient current is not known, a valid assumption can be made by the use of the magnetizing current versus voltage on page 4. If the transient results from opening a circuit containing an inductance, the transient current will be the current through the inductance at the instant of interruption. To select the proper ITT suppressor series, assume a single pulse width of 4 milliseconds and refer to the pulse current versus time curve on page 4. The same curve can be used to select the appropriate ITT series when a single pulse width other than 4 milliseconds is known or assumed.

Voltage Rating

After the required current rating has been established, determine the maximum steady-state voltage which will appear across the suppressor rectifier and select the appropriate type number from the tables on pages 2 and 3. Note that both RMS and peak voltage ratings are tabulated for AC types and DC ratings for DC types. Use the RMS value for sinusoidal voltages; otherwise, use the peak value of the input voltage to select the proper rectifier.

Zener Voltage

The Zener voltages shown in the characteristics tables are the maximum instantaneous voltages that will appear across the rectifier if the 4 millisecond current rating is not exceeded. Any ITT suppressor rectifier can safely discharge higher currents than this rating, where the pulse width is less than 4 milliseconds.

For other values of peak current, however, the indicated Zener voltage will be as shown in the curves on page 4. To obtain the expected protection, rectifiers should be used within their rated currents. For optimum protection, the maximum Zener voltage should be below the PIV rating of the semiconductor devices being protected.

The maximum Zener voltages shown in the characteristics tables have been derived from the curves on page 4 which represent the conservative ratings placed on suppressor rectifiers. These volt-ampere curves apply to a single cell. To determine the Zener voltage for a particular rectifier, multiply the peak voltage values that are shown by the number of cells per arm for AC rectifiers, or by the total number of cells for DC rectifiers. The final step is to be sure that the silicon or germanium rectifier or silicon controlled rectifier to be protected has a PIV rating higher than the Zener voltage of the ITT protector rectifier. The volt-ampere curves are also valid for DC applications in determining the proper rectifier for a given peak transient voltage.

Similar protection is also provided to transformers, capacitors, resistors, switches, relays, or any electrical component subject to damage from transient over-voltage.

Example

Assume a single phase full-wave bridge rectifier application with a transformer rated at 8.5KVA, 115V. The rectifier to be protected is across the transformer secondary.

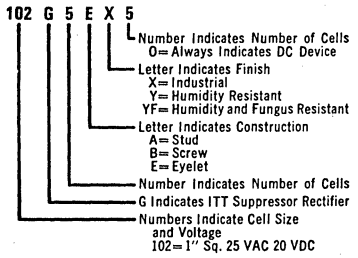
1. Assume a 4 millisecond pulse width.
2. From the curve on page 4, determine the per cent of magnetizing current. Using the "maximum" plot line, 8.5KVA ≈5.2% of full load current.

Full load current $\frac{VA}{V} \approx \frac{8500}{115} \approx 74A$

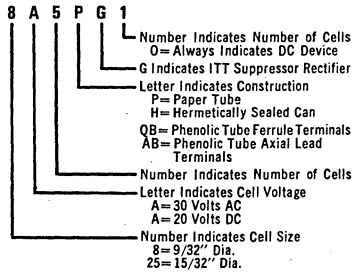
$74A \times 5.2\% \approx 3.85A$ peak.

3. From the RATINGS table on page 1, select a rectifier series which will withstand 3.85A peak @ 4 millisecond pulse width. The 102 series, either stud mounting or eyelet mounting may be used. Assume a stud type is preferred for this application.
4. Select the appropriate ITT part number from the stud mounting table on page 2 by finding a type with a RMS input voltage rating equal to or above 115V. 102G5BX5 meets this requirement.
5. Determine the PIV rating required for the rectifier to be protected. Use the 102 series curve on page 4 to determine the voltage corresponding to 3.85A. The maximum voltage is 73 volts per cell. The number of cells in each rectifier is indicated by the first number after the first letter in the part number. In this case the 102G5BX5 has five cells. The maximum voltage is 73 × 5 = 365V. The PIV rating required for the protected rectifier is 365V.

CODING SYSTEM FOR EYELET AND STUD TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

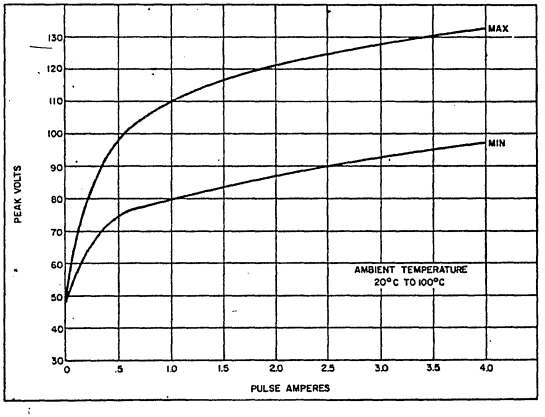


CODING SYSTEM FOR TUBULAR TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

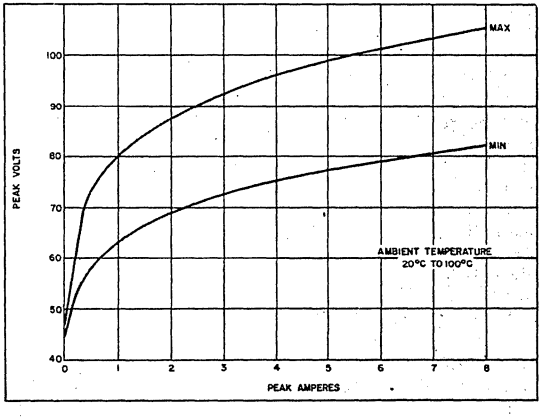


CHARACTERISTIC CURVES

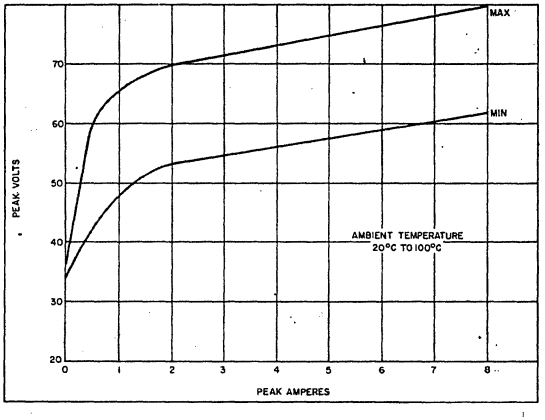
8A1 SERIES PEAK VOLTAGE VS CURRENT



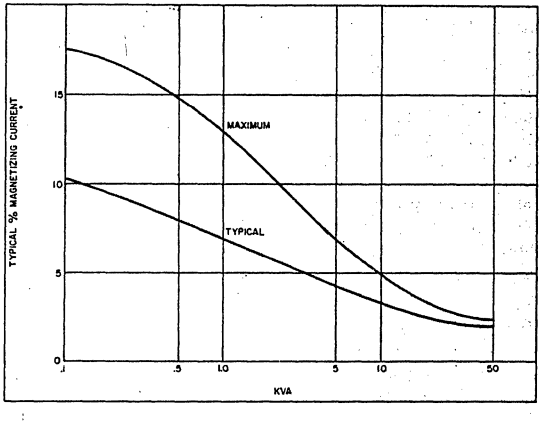
25A1 SERIES PEAK VOLTAGE VS CURRENT



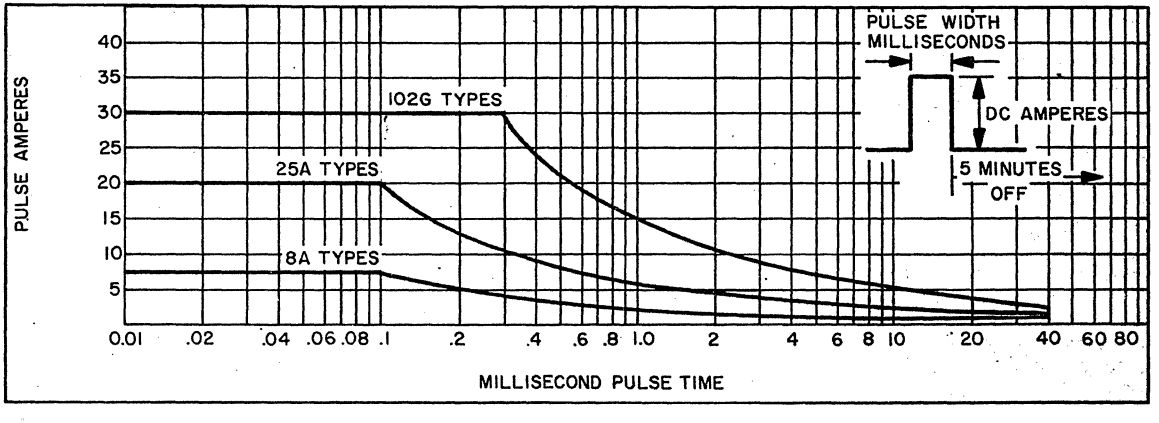
102 SERIES PEAK VOLTAGE VS CURRENT



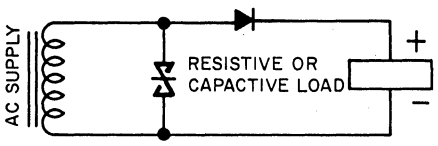
MAGNETIZING CURRENT VS VOLTAGE



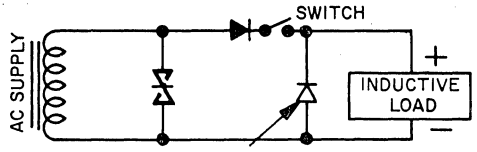
PULSE CURRENT VS TIME



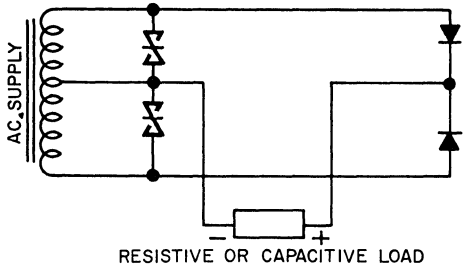
TYPICAL APPLICATIONS

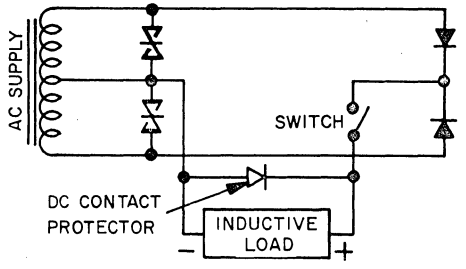


Single-Phase Half-Wave Silicon Rectifier

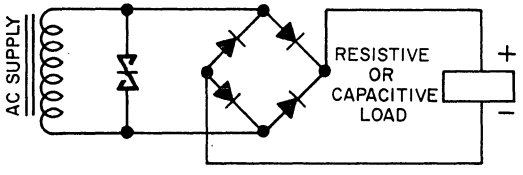


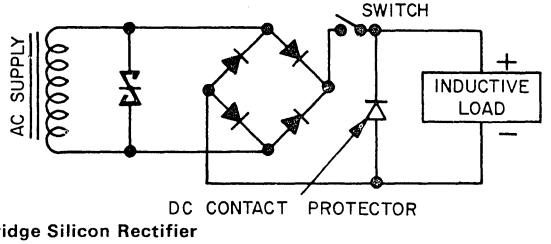
Single-Phase Full-Wave Center Tap Silicon Rectifier



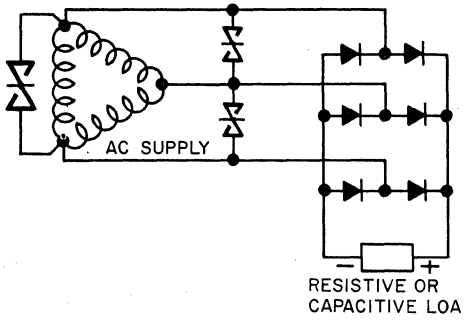


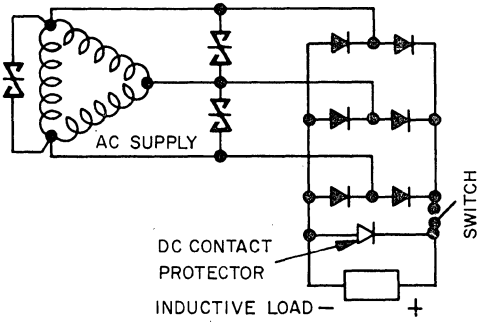
Single-Phase Full-Wave Bridge Silicon Rectifier





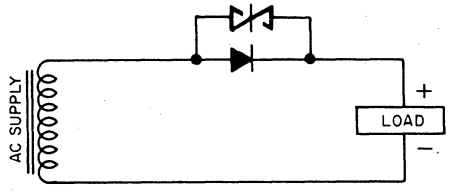
Three-Phase Full-Wave Bridge Silicon Rectifier

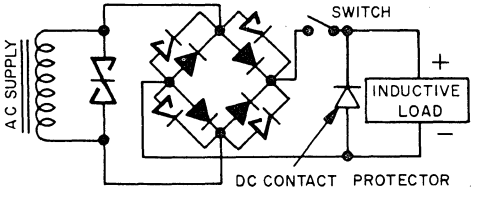




Single-Phase Half-Wave Silicon-Controlled Rectifier

Single-Phase Full-Wave Silicon Rectifier





ITT SEMICONDUCTORS

DIFFUSED SILICON GENERAL-PURPOSE DIODES

- **Hermetically sealed**
- **DO-7 package**
- **Rugged construction**
- **High reliability**

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature (unless otherwise noted)

Symbol	Characteristics	IN645	1N646	1N647	1N648	1N649	Unit
$V_{RM(wkg)}$	Working Peak Reverse Voltage over Operating Free-Air Temperature Range	225	300	400	500	600	V
I_O	Average Rectified Forward Current at (or below) 25°C Free-Air Temperature Range (See Note 1)	400					mA
I_O	Average Rectified Forward Current at 150°C Free-Air Temperature (See Note 1)	150					mA
$I_{FM(surge)}$	Peak Surge Current, One Second, at 25°C to 150°C Free-Air Temperature (See Note 2)	3					A
P	Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	600					mW
$T_{A(opr)}$	Operating Free-Air Temperature Range	−65 to 150					°C

*IN645, IN647 and IN649 are available in JAN and JAN TX versions.

ELECTRICAL CHARACTERISTICS @ 25°C Free Air Temperature (unless otherwise noted)

Symbol	Parameter	IN645 Min	IN645 Max	1N646 Min	1N646 Max	1N647 Min	1N647 Max	1N648 Min	1N648 Max	1N649 Min	1N649 Max	Unit	Conditions
$V_{(BR)}$	Reverse Breakdown Voltage	275		360		480		600		720		V	I_R=100μA, T_A=100°C
I_R	Static Reverse Current		0.2		0.2		0.2		0.2		0.2	μA	V_R=Rated $V_{RM(wkg)}$
			15		15		20		20		25	μA	V_R=Rated $V_{RM(wkg)1}$ T_A=100°C
V_F	Static Foward Voltage		1		1		1		1		1	V	I_F=400mA
C_T	Total Capacitance		6 typ		6 typ		6 typ		6 typ		6 typ	pF	V_R=12V, f=1 MHz

NOTES:

1. These values may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 25°C see Thermal Characteristics Chart.

2. These values apply for a one-second square-wave pulse with the device at nonoperating thermal equilibrium immediatelly prior to the surge.

3. Derate linearly to 200 mW at 150°C free-air temperature at the rate of 3.2 mW/deg.

1-AMP PLASTIC SILICON RECTIFIERS

- **Moisture resistant**
- **Voltages to 1000 volts**

The ITT Plastic Silicon Rectifier is molded using a new plastic formulation with the following advantages over silicone and epoxy compounds:

ELECTRICAL CHARACTERISTICS @ 25°C Unless Otherwise Noted

	*1N4000 Series	EM500 Series	Units
Peak Reverse Voltage (PRV) 50	1N4001 50	(EM500)	Volts
100	1N4002 100	(EM501)	
200	1N4003 200	(EM502)	
400	1N4004 400	(EM504)	
600	1N4005 600	(EM506)	
800	1N4006 800	(EM508)	
1000	1N4007 1000	(EM510)	
Average Rectified Current @ 25°C Ambient ..	1.0	1.0	Amps
Average Rectified Current @ 75°C Ambient ..	1.0	0.5	Amps
Foward Voltage Drop @ 1 Amp	1.1	1.1	Volts
Reverse Current @ Rated DC Voltage	10	1.0	Volts
Full Cycle Average Reverse Current @ Rated PRV @ 85°C Ambient @ Rated Average Rectified Current	200	200	Volts
100°C Ambient @ Rated Average Rectified Current	50	50	Volts
Half Cycle Surge Current, 60 Hz	30	50	Amps
Temperature Range (operating)	−65 to +175	−65 to +175	°C
Temperature Range — Storage	−65 to +200	−65 to +200	°C

*Electrical Equivalent

1N4000 SERIES, EM500 SERIES
PLASTIC SILICON RECTIFIER

ITT SILICON RECTIFIER CROSS-REFERENCE

Now you can replace older types of rectifiers with dependable, inexpensive ITT Plastic types. In most cases, the ITT types will have higher output current and PRV ratings than the types to be replaced. Case dimensions are not always physically identical, in many cases the ITT types are smaller.

Type To Be Replaced	ITT Replacement	Type To Be Replaced	ITT Replacement
1N253	1N4002	1N359A	1N4002
1N254	1N4003	1N360A	1N4002
1N255	1N4004	1N361A	1N4003
1N256	1N4005	1N362A	1N4004
1N316	1N4001	1N363A	1N4005
1N316A	1N4001	1N364A	1N4007
1N317	1N4002	1N365A	1N4007
1N317A	1N4002	1N440	1N4002
1N318	1N4003	1N440B	1N4002
1N318A	1N4003	1N441	1N4003
1N319	1N4004	1N441B	1N4003
1N319A	1N4004	1N442	1N4004
1N320	1N4005	1N442B	1N4004
1N320A	1N4005	1N443	1N4004
1N321A	1N4007	1N43B	1N4004
1N322A	1N4007	1N444	1N4005
1N323A	1N4001	1N44B	1N4005
1N324A	1N4002	1N445	1N4005
1N325A	1N4003	1N445B	1N4005
1N326A	1N4004	1N530	1N4002
1N327A	1N4005	1N531	1N4003
1N328A	1N4007	1N532	1N4004
1N329A	1N4007	1N533	1N4004
1N332	1N4004	1N534	1N4005
1N333	1N4004	1N535	1N4005
1N334	1N4004	1N536	1N4001
1N335	1N4004	1N537	1N4002
1N336	1N4003	1N538	1N4003
1N337	1N4003	1N539	1N4004
1N338	1N4002	1N540	1N4004
1N339	1N4002	1N547	1N4005
1N340	1N4002	1N550	1N4002
1N341	1N4004	1N551	1N4003
1N342	1N4004	1N552	1N4004
1N343	1N4004	1N553	1N4004
1N344	1N4004	1N554	1N4005
1N345	1N4003	1N555	1N4005
1N346	1N4003	1N560	IN4006
1N347	1N4002	1N561	1N4007
1N348	1N4002	1N562	1N4006
1N349	1N4002	1N563	1N4007
1N596	1N4005	1N687	1N4005
1N597	1N4006	1N689	1N4005
1N598	1N4007	1N846	1N4001
1N599	1N4001	1N847	1N4002
1N599A	1N4001	1N848	1N4003
1N600	1N4002	1N849	1N4004
1N600A	1N4002	1N850	1N4004
1N601	1N4003	1N851	1N4005
1N601A	1N4003	1N852	1N4005
1N602	1N4003	1N853	1N4006
1N602A	1N4003	1N854	1N4006
1N603	1N4004	1N855	1N4007
1N603A	1N4004	1N856	1N4007
1N604	1N4004	1N857	1N4001
1N604A	IN4004	1N858	1N4002
1N605	1N4005	1N859	1N4003
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1N606A	1N4005	1N862	1N4005
1N607	1N4001	1N863	1N4005
1N607A	1N4001	1N864	1N4006
1N608	1N4002	1N865	1N4006
1N608A	1N4002	1N866	1N4007
1N609	1N4003	1N867	1N4007
1N609A	1N4003	1N868	1N4001
1N610	1N4003	1N869	1N4002
1N610A	1N4003	1N870	1N4003
1N611	1N4004	1N871	1N4004
1N611A	1N4004	1N872	1N4004
1N612	1N4004	1N873	1N4005
1N612A	1N4004	1N874	1N4005
1N613	1N4005	1N875	1N4006
1N613A	1N4005	1N876	1N4006
1N614	1N4005	1N877	1N4007
1N614A	1N4005	1N878	1N4007
1N645	1N4004	1N879	1N4001
1N645A	1N4004	1N880	1N4002
1N646	1N4004	1N881	1N4003
1N647	1N4004	1N882	1N4004
1N648	1N4005	1N883	1N4004
1N649	IN4005	1N884	1N4005
1N676	1N4002	1N885	1N4005
1N677	1N4002	1N886	1N4006
1N678	1N4003	1N887	1N4006
1N679	1N4003	1N888	1N4007
1N681	1N4004	1N889	1N4007
1N682	1N4004	1N1081	1N4002
1N683	1N4004	1N1082	1N4003
1N684	1N4004	1N1083	1N4004
1N685	1N4005	1N1084	1N4004
1N686	1N4005	1N1095	1N4005

Type To Be Replaced	ITT Replacement	Type To Be Replaced	ITT Replacement	Type To Be Replaced	ITT Replacement	Type To Be Replaced	ITT Replacement
1N1096	1N4005	1N1692	1N4002	1N2483	1N4004	1N3640	1N4004
1N1100	1N4002	1N1693	1N4003	1N2484	1N4005	1N3641	1N4005
1N1101	1N4003	1N1694	1N4004	1N2485	1N4003	1N3642	1N4006
1N1102	1N4004	1N1695	1N4004	1N2486	1N4004	1N4245	1N4003
1N1103	1N4004	1N1696	1N4005	1N2487	1N4004	1N4246	1N4004
1N1104	1N4005	1N1697	1N4005	1N2488	1N4005	1N4247	1N4005
1N1105	1N4005	1N1701	1N4001	1N2489	1N4005	1N4248	1N4006
1N1122A	1N4004	1N1702	1N4002	1N2609	1N4001	1N4249	1N4007
1N1169	1N4004	1N1703	1N4003	1N2610	1N4002	1N4250	1N4006
1N1217	1N4001	1N1704	1N4004	1N2611	1N4003	1N4251	1N4007
1N1217A	1N4001	1N1705	1N4004	1N2612	1N4004	1N4361	1N4007
1N1218	1N4002	1N1706	1N4005	1N2613	1N4004	IN4364	1N4002
1N1218A	1N4002	1N1707	1N4001	1N2614	1N4005	1N4365	1N4003
1N1219	1N4003	1N1708	1N4002	1N2615	1N4005	1N4366	1N4004
1N1219A	1N4003	1N1709	1N4003	1N2616	1N4006	1N4367	1N4004
1N1220	1N4003	1N1710	1N4004	1N2617	1N4007	1N4368	1N4005
1N1220A	1N4003	1N1711	1N4004	1N2858	1N4001	1N4369	1N4005
1N1221	1N4004	1N1712	1N4005	1N2859	1N4002	1N4383	1N4003
1N1221A	1N4004	1N1730	1N4007	1N2860	1N4003	1N4384	1N4004
1N1222	1N4004	1N1763	1N4004	1N2861	1N4004	1N4385	1N4005
1N1223	1N4005	1N1764	1N4005	1N2862	1N4004	2E4	1N4004
1N1224	1N4005	1N1907	1N4001	1N2863	1N4005	3MS5	1N4001
1N1224A	1N4005	1N1908	1N4002	1N2864	1N4005	3MS10	1N4002
1N1225	1N4006	1N1909	1N4003	1N2878	1N4006	3MS20	1N4003
1N1225A	1N4006	1N1911	1N4004	1N2879	1N4006	3MS30	1N4004
1N1226	1N4006	1N1912	1N4005	1N2880	1N4007	3MS40	1N4004
1N1226A	1N4006	1N1913	1N4005	1N2881	1N4007	3MS50	1N4005
1N1251	1N4002	1N1914	1N4006	1N2882	1N4007	5A2	1N4003
1N1252	1N4002	1N1915	1N4006	1N2883	1N4007	5A4	1N4004
1N1253	1N4003	1N1916	1N4007	1N3189	1N4003	5A5	1N4005
1N1254	1N4004	1N2069	1N4003	1N3190	1N4004	5A6	1N4005
1N1255	1N4004	1N2069A	1N4003	1N3191	1N4005	5A8	1N4006
1N1443	1N4007	1N2070	1N4004	1N3193	1N4003	5A10	1N4007
1N1486	IN4005	1N2070A	1N4004	1N3194	1N4004	5E4	1N4004
1N1487	1N4002	1N2071	1N4005	1N3195	1N4005	5E5	1N4005
1N1488	1N4003	1N2071A	1N4005	1N3196	1N4006	5E6	1N4006
1N1489	1N4004	1N2072	1N4001	1N3253	1N4003	5MA2	1N4003
1N1490	1N4004	1N2073	1N4002	1N3254	1N4004	5MA4	1N4004
1N1491	1N4005	1N2074	1N4003	1N3255	1N4005	5MA5	1N4005
1N1492	1N4005	1N2075	1N4003	1N3256	1N4006	5MA6	1N4005
1N1538	1N4002	1N2076	1N4004	1N3544	1N4002	5MA8	1N4006
1N1539	1N4003	1N2077	1N4004	1N3545	1N4003	5MA10	1N4007
1N1540	1N4003	1N2078	1N4004	1N3546	1N4004	5MS5	1N4001
1N1541	1N4004	1N2079	1N4005	1N3547	1N4004	5MS10	1N4002
1N1542	1N4004	1N2103	1N4001	1N3548	1N4005	5MS20	1N4003
1N1543	1N4005	1N2104	1N4002	1N3549	1N4005	5MS30	1N4004
1N1544	1N4005	1N2105	1N4003	1N3611	1N4003	5MS40	1N4004
1N1617	1N4002	1N2106	1N4004	1N3612	1N4004	5MS50	1N4005
1N1618	1N4003	1N2107	1N4004	1N3613	1N4005	10B1	1N4002
1N1619	1N4004	1N2108	1N4005	1N3614	1N4006	10B2	1N4003
1N1620	1N4004	1N2482	1N4003	1N3639	1N4003	10B3	1N4004

1N4000 SERIES, EM500 SERIES

PLASTIC SILICON RECTIFIER

Type To Be Replaced	ITT Replace-ment	Type To Be Replaced	ITT Replace-ment	Type To Be Replaced	ITT Replace-ment	Type To Be Replaced	ITT Replace-ment
10B4	1N4005	359B	1N4002	AH805	1N4006	PA330	IN4004
10B5	1N4005	359D	1N4003	AH810	1N4006	PA340	1N4004
10B6	1N4005	359F	1N4404	AH815	1N4006	PA350	1N4005
10B8	1N4006	359H	1N4004	AH1005	1N4007	PA360	1N4005
10B10	1N4007	359K	1N4005	AH1010	1N4007	PA380	1N4006
10D2	1N4003	359M	1N4005	AH1015	1N4007	PT3	1N4004
10D3	1N4004	359P	1N4006	AM3	1N4001	PT5	1N4004
10D4	1N4004	359S	1N4006	AM13	1N4002	PT5B	1N4005
10D5	1N4005	359Z	1N4007	AM23	1N4003	PT505	1N4001
10D6	1N4005	A10A	1N4002	AM33	1N4004	PT510	1N4002
10D7	1N4006	A10B	1N4003	AM43	1N4004	PT515	1N4003
10D8	1N4006	A10C	1N4004	AM53	1N4005	PT520	1N4003
10D10	1N4007	A10D	1N4004	AM63	1N4005	PT525	1N4004
320A	1N4001	A10E	1N4005	G100K	1N4006	PT530	1N4004
320B	1N4002	A10M	1N4005	G100M	1N4007	PT540	1N4004
320C	1N4003	A10N	1N4006	PA3	1N4004	PT550	1N4005
320D	1N4003	A10P	1N4007	PA069	1N4003	PT560	IN4005
320F	1N4004	A13A2	1N4002	PA070	IN4004	S91	1N4002
320H	1N4004	A13B2	1N4003	PA071	IN4005	S91H	1N4002
320M	1N4005	A13C2	1N4004	PA305	1N4001	S92	1N4003
320K	1N4005	A13D2	1N4004	PA310	1N4002	S92H	1N4003
320P	1N4006	A13E2	1N4005	PA315	1N4003	S93	1N4004
320S	1N4006	A13F2	1N4001	PA320	1N4003	S93H	1N4004
320Z	1N4007	A13M2	1N4005	PA325	1N4004	S94	1N4004

1 AMP, 50 TO 1,000 VOLTS GLASS RECTIFIERS

- **Hermetic seal**
- **Glassivated epitaxial grown state of the art chip**
- **Peak inverse voltage to 1000V**
- **Average forward current, 1 Amp**
- **Surge current, 30 Amp max.**
- **Withstands lead pull, 18 lbs. for 15 sec.**

This series designed for power rectification in military and industrial. These devices are ideal for Appliance & Entertainment circuits, Test Equipment, Control circuits, Computer and Peripheral and many more. Ideal lead material for welding.

ABSOLUTE MAXIMUM RATINGS	UNITS
Max peak forward voltage drop @ 1A peak @ 25°C	1.1V
Max peak reverse current at rated PIV @ 25°C	10μA
Max average reverse current at rated full load	30μA
Max peak reverse current at rated PIV D.C.	50μA
Operating temperature range	−65°C to +175°C
Storage temperature range	−65°C to 200°C

MAXIMUM RATINGS AT 50°C AMBIENT

Type	Peak inverse voltage (volts)	Average forward current amps	Max ½ cycle surge @ 60 cps rated load in amps
1N4001	50	1.0	30
1N4002	100	1.0	30
1N4003	200	1.0	30
1N4004	400	1.0	30
1N4005	600	1.0	30
1N4006	800	1.0	30
1N4007	1,000	1.0	30

For additional ratings see figures 1, 2 and 3.

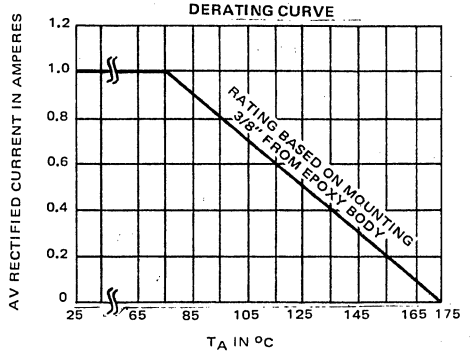


FIG. 1

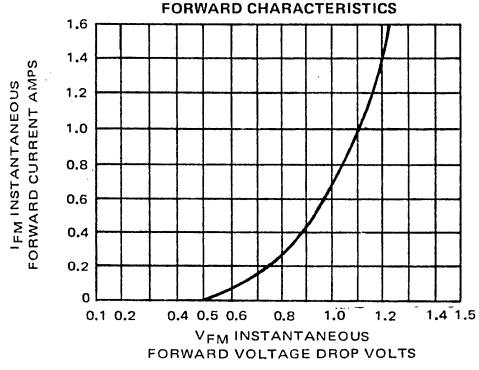


FIG. 2

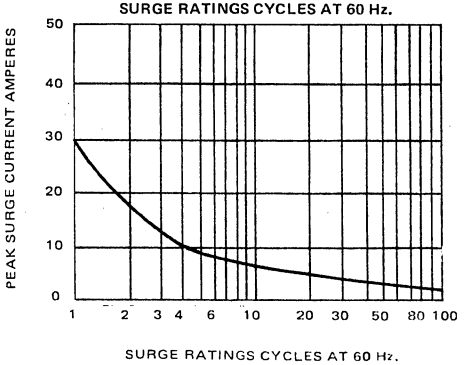


FIG. 3

1-AMP SILICON GLASS RECTIFIERS

- **V_R Ratings 50 to 1000 Volts**
- **Surge Current Rating 50 Amperes**
- **Series JAN approved**

The ITT 1N4383-5, 1N4585-6, offer up to one-amp rectified current at 100°C in a small, hermetically sealed DO-29 glass package. All units are passivated, 100 percent tested, and have a 50-amp surge current rating to insure a stable, highly reliable rectifier. Rectifiers are supplied with solderable leads and may be delivered reel-packed for automatic insertion equipment.

ABSOLUTE MAXIMUM RATINGS *

Characteristics	RG1122	RG1123	1N4383	1N4384	1N4385	1N4585	1N4586	Units
Maximum recurrent peak reverse voltage..	50	100	200	400	600	800	1000	Volts
Maximum RMS voltage	35	70	140	280	420	560	700	Volts
Maximum DC blocking voltage	50	100	200	400	600	800	100	Volts
Maximum average forward rectified current ⅜" lead length .. 50°C Ambient	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Amps
100°C Ambient	1.0	1.0	1.0	1.0	1.0	0.6	0.6	Amps
150°C Ambient	0.3	0.3	0.3	0.3	0.3	0.2	0.2	Amps
Maximum peak surge 1 Cycle	50	50	50	50	50	50	50	Amps
overload current 10 Cycles	16	16	16	16	16	16	16	Amps
100 Cycles	6	6	6	6	6	6	6	Amps
Maximum forward voltage drop at 1 amp DC, 25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Volts
Maximum full cycle average reverse current, @ rated average forward current and 100°C ambient	275	250	275	250	225	200	200	μamps
Maximum DC leakage at rated DC blocking voltage and 25°C ambient ...	10	10	10	10	10	10	10	μamps
Typical recovery time at 25°C ambient ...	10	10	10	10	10	10	10	μsecs
Temperature Range, op & stg.	−65 to +175							°C

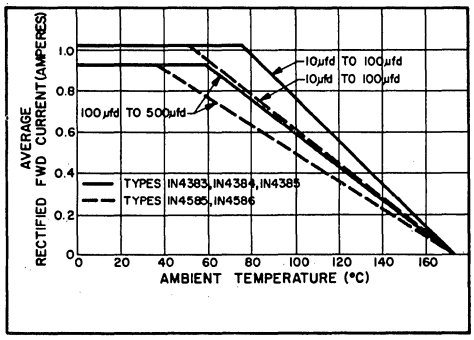
NOTE:

60 cps, inductive or resistive load, single phase half wave.

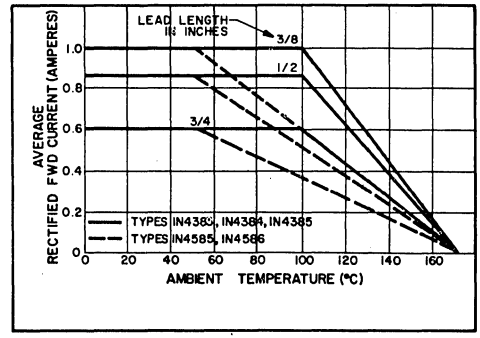
1N4383/5, 1N4585/6, RG1122/3
1-AMP GLASS RECTIFIERS

TYPICAL CHARACTERISTICS @ 25°C unless otherwise noted

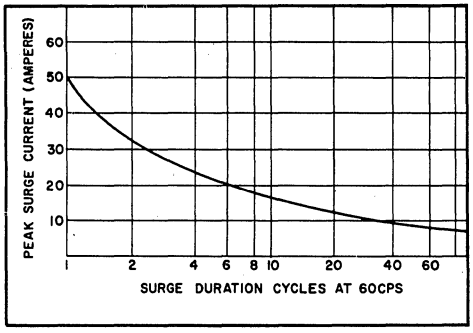
Maximum Average FWD Current Rating-⅜" Lead Length (Capacitive Load, Single Phase, 60cps)



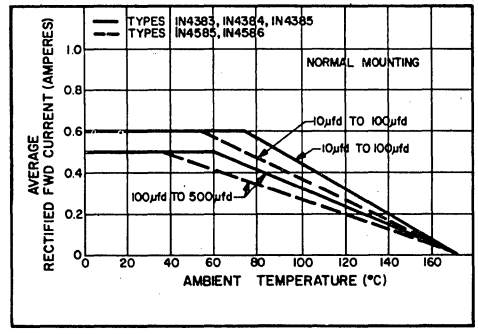
Maximum Average Forward Current Rating (Resistive or Inductive Load, Single Phase, 60cps)



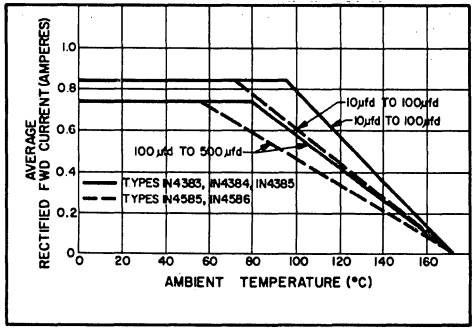
Non-Recurrent Surge Rating (−65° to 175°C)



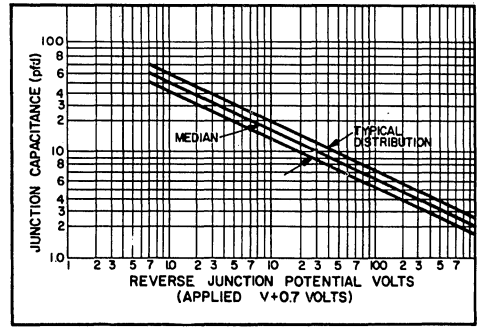
Maximum Average FWD Current Rating-¾" Lead Length (Capacitive Load, Single Phase, 60cps)



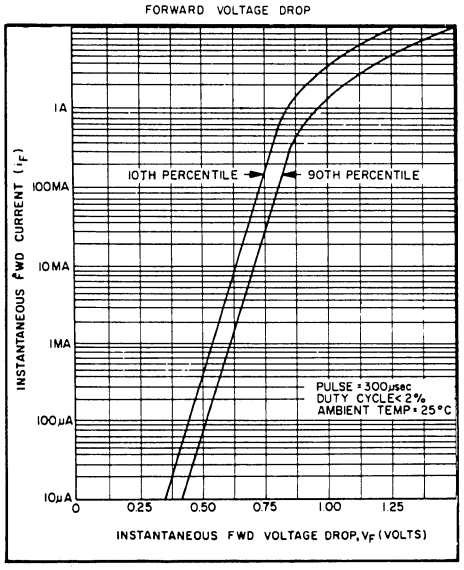
Maximum Average FWD Current Rating-½" Lead Length (Capacitive Load, Single Phase, 60cps)

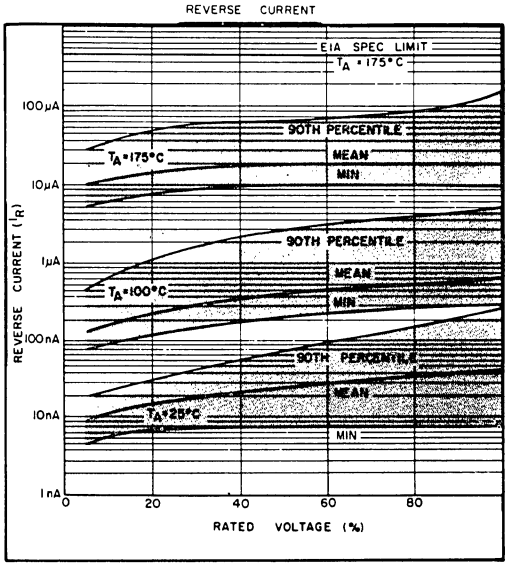


Junction Capacitance vs. Reverse Junction Potential



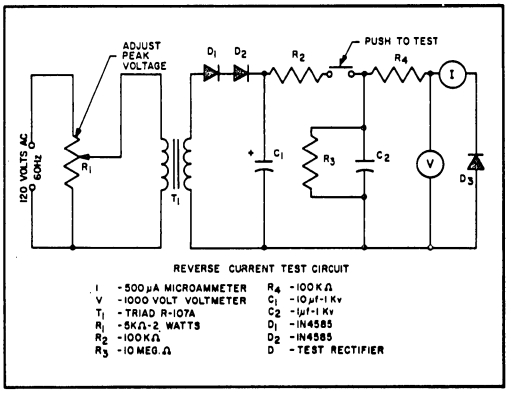
TYPICAL CHARACTERISTICS, continued





DC REVERSE LEAKAGE TEST

The circuit at right provides a simple and inexpensive means for checking the instantaneous leakage characteristics of the 1N4383 series and other low current rectifiers. The pushbutton switch should not be omitted as it minimizes junction heating when testing is being done at high voltage, and prevents the possibility of thermal runaway. Tests may be conducted at high temperature by placing the test rectifier(s) in an oven. Junction temperature rise above ambient due to internal heating is generally low enough to be neglected.



REVERSE CURRENT TEST CIRCUIT

I	-500 µA MICROAMMETER	R_4	-100K Ω
V	-1000 VOLT VOLTMETER	C_1	-10 µf-1 Kv
T_1	-TRIAD R-107A	C_2	-1µf-1 Kv
R_1	-5KΩ-2 WATTS	D_1	-IN4585
R_2	-100KΩ	D_2	-IN4585
R_3	-10 MEG.Ω	D	-TEST RECTIFIER

ITT SEMICONDUCTORS

1 AMP, 50 THROUGH 1,000 VOLTS GLASS RECTIFIERS

- **Hermetic seal**
- **Glassivated epitaxial grown state of the art chip**
- **Peak inverse voltage to 1000V**
- **Average forward current . . . 1 Amp**
- **Surge current . . . 50 Amp max**
- **Withstands lead pull — 18 lbs. for 15 sec.**

This series is designed for power rectification in military and industrial applications at low cost. These devices are ideal for telephone switching applications, appliance & entertainment circuits, test equipment, control circuits, computer and peripherals and many more. Ideal lead material for welding.

MAX RATINGS AT 100°C

Type	Peak Inverse Voltage	Average Forward Current	Max ½ Cycle Surge @ 60 Hz
EM050G,	50	1A	50A
EM501G,	100	1A	50A
EM502G, 1N3611, 1N4245	200	1A	50A
EM504G, 1N3612, 1N4246	400	1A	50A
EM506G, 1N3613, 1N4247	600	1A	50A
EM508G, 1N3614, 1N4248	800	1A	50A
EM510G, 1N3957, 1N4249	1000	1A	50A

For additional ratings see Figures 1, 2, & 3

ABSOLUTE MAXIMUM RATING	UNITS
Max peak forward voltage drop @ 1.0 Amp @ 25°C	1.0V
Max peak reverse current at rated PIV, 25°C	5μA
Max peak reverse current at rated PIV & 150°C	300μA
Operating temperature range	−65°C to +175°C
Storage temperature range	−65°C to 200°C

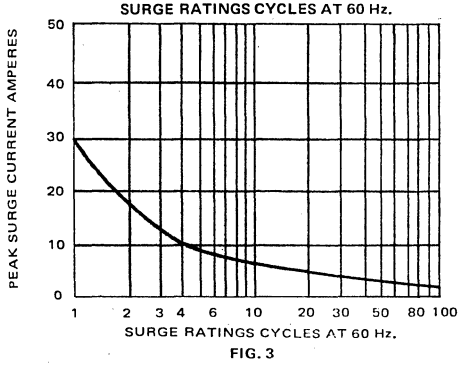


FIG. 3

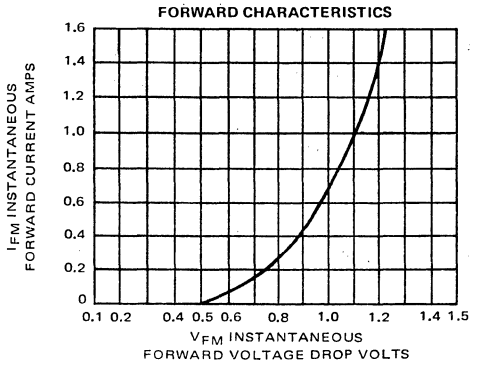


FIG. 2

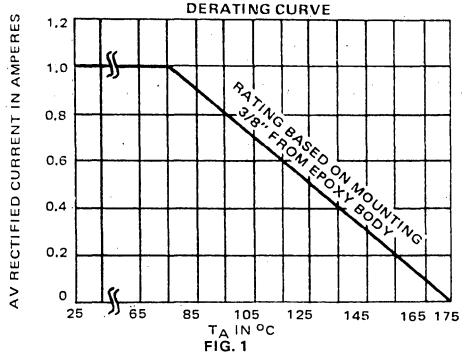


FIG. 1

3 AMPS, 50 VOLTS TO 1000 VOLTS SILICON RECTIFIERS

- **Diffused silicon construction**
- **PIV to 1000 volts**
- **Surge current . . . 300 amps max.**
- **Average forward current . . . 3A**
- **Molded epoxy construction**

ABSOLUTE MAXIMUM RATINGS	UNITS
Max peak forward voltage drop @ 3A	1.0Volt
Max peak reverse current at rated PIV @ 25°C	25μA
Max peak reverse current at rated PIV @ 50°C	250μA
Operating temperature range	−65°C to +150°C
Storage temperature range	−65°C to +150°C

Rectifier is designed for motor controls, appliance and entertainment industry, power supplies and test equipment. Design features rugged construction, 3 Amp forward current and 300 Amp surge.

MAXIMUM RATINGS AT 50°C

Type	PIV	Average Forward Current	Max ½ Cycle Surge	I^2t ≤8.3 ms amp² sec
IN5400	50	3A	300A	190
IN5401	100	3A	300A	190
IN5402	200	3A	300A	190
IN5403	300	3A	300A	190
IN5404	400	3A	300A	190
IN5405	500	3A	300A	190
IN5406	600	3A	300A	190
IN5407	800	3A	300A	190
IN5408	1000	3A	300A	190

For additional ratings see Figures 1, 2, 3, 4

1N5400 THROUGH 1N5408
SILICON RECTIFIERS

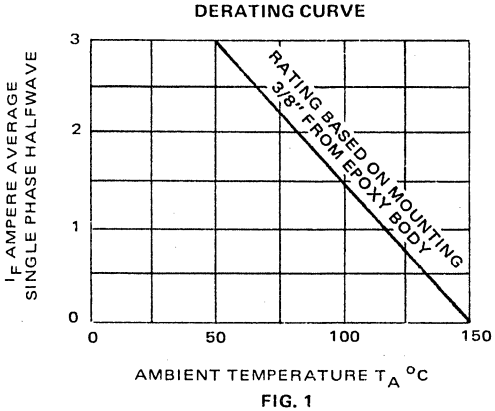


FIG. 1

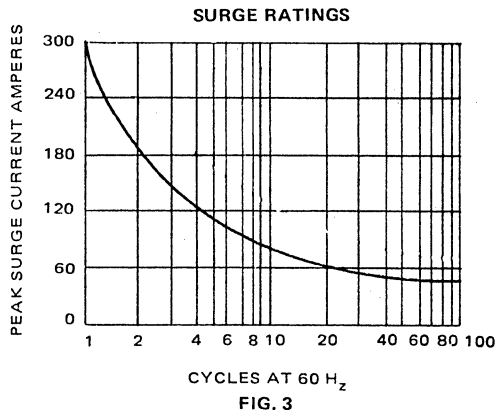


FIG. 3

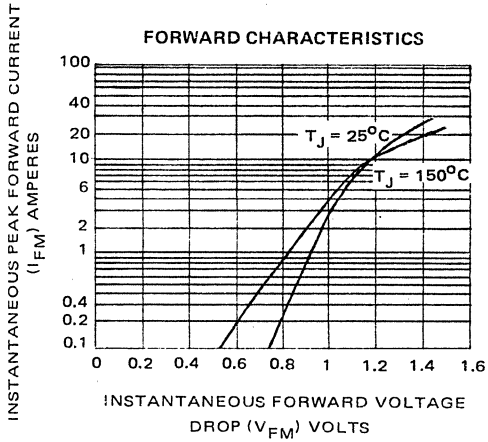


FIG. 2

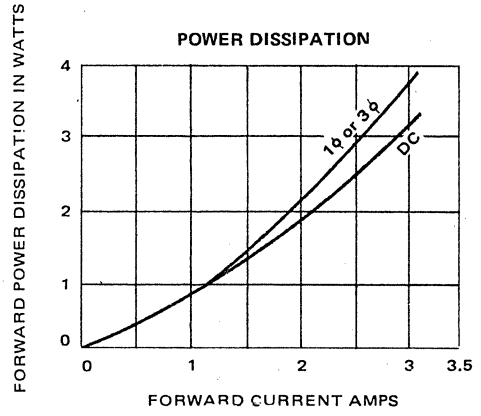


FIG. 4

ENTERTAINMENT TYPE SELENIUM RECTIFIERS

CARTRIDGE TYPE 676H100BCIT
(half size)

MINIATURE TYPE 1215
(actual size)

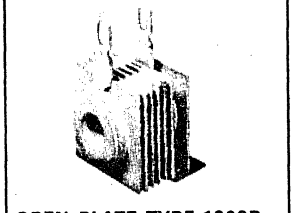
- Low Cost
- Small Size
- Easy Mounting
- Long Life
- High Voltage

The ITT selenium rectifiers in this catalog cover a wide range of applications. High voltage types lend themselves to compact power supply designs for mobile equipment. The "off-the-line" types are ideal for low-cost half wave and voltage doubler applications in a variety of equipment. Low power applications are especially appropriate for the clip-in types and miniature diodes.

ITT selenium rectifiers are available in several mounting and terminal styles. Miniature diodes and tubular type rectifiers are provided with tinned wire leads and are self-supporting. Open type rectifiers are available in stud and eyelet mounting styles, many can be supplied with clip-in mountings. These rectifiers can be supplied with conventional solder terminals, printed wiring board terminals or plug-in terminals.

ITT's vacuum disposition technique produces selenium rectifiers with extremely long life and minimum change in initial characteristics.

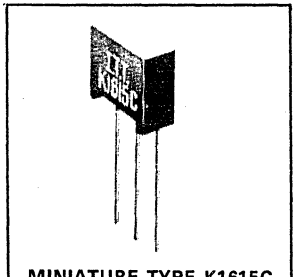
CLIP TYPE 6H65F
(actual size)



OPEN PLATE TYPE 1263B
(actual size)

APPLICATIONS

- Horizontal phase discriminator
- Diode matrix assemblies
- Oscilloscopes
- Gate circuits
- Wave shaping networks
- Modulators and demodulators
- Power supplies
- Hi-fi equipment
- DC motor control
- Electric appliances



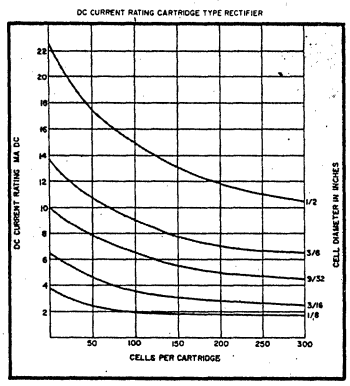
MINIATURE TYPE K1615C
(actual size)

HIGH VOLTAGE CARTRIDGE TYPE SELENIUM RECTIFIERS

CHARACTERISTICS

PIV	Rating (mA)	DIMENSIONS (inches)					ITT Part No.
		Rectifier Dim.		Cell Dia.	Lead Dim.(1)		
		Dia.	Length		Dia.	Length	
4650	2	7/32	3-9/32	1/8	.031(2)	1½	665H100ABI
4650	2	7/32	2-1/8	1/8	.031(2)	1½	665H100ABIT
4650	4	9/32	3-9/32	3/16	.031(2)	1½	676H100ABI
4650	4	9/32	2-1/8	3/16	.031(2)	1½	676H100ABIT
4650	6.5	13/32	3-9/32	9/32	.040(2)	1½	647H100ABI
4650	6.5	13/32	2-1/8	9/32	.040(2)	1½	647H100ABIT
4650	2	15/64	3-1/2	1/8	.031	1½	665H100BCI
4650	2	15/64	2-11/32	1/8	.031	1½	665H100BCIT
4650	4	19/64	3-1/2	3/16	.031	1½	676H100BCI
4650	4	19/64	2-11/32	3/16	.031	1½	676H100BCIT
4650	6.5	3/8	3-1/2	9/32	.031	1½	647H100BCI
4650	6.5	3/8	2-11/32	9/32	.031	1½	647H100BCIT
4650	15	39/64	3-23/32	1/2	.031	1½	629H100BCI
4650	15	39/64	2-9/16	1/2	.031	1½	629H100BCI
4650	25	15/16	3-23/32	3/4	.031	1½	630H100BCI
4650	25	15/16	2-9/16	3/4	.031	1½	630H100BCIT

NOTES: 1. Solder type terminals or radial leads also available.
2. Silver plated metal end ferrules.



HOW TO ORDER HIGHER VOLTAGE TYPES

Voltage ratings are available in 46.5 volt increments up to many thousands of volts. Contact ITT Semiconductors for applications assistance.

HOW TO CALCULATE CURRENT RATINGS

Current rating depends upon cell area and the number of cells in series. The curves at the right give the necessary information. The AB series of rectifiers in the characteristics table above have a maximum current rating of 10 mA in a half wave circuit. The BC series has a maximum current rating of 45 mA in a half wave circuit.

OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS

SPECIFICATIONS

Rated Input Voltage ..... 117 Volts RMS
Maximum Input Voltage ..... 130 Volts RMS
Maximum Inverse Voltage ..... 380 Volts Peak
Maximum Output Current ..... As Listed
Maximum RMS Current ..... 2.7 Times DC Rating
Maximum Peak Current ..... 10 Times DC Rating
Minimum Series Resistance ..... As Listed
Maximum Cell Operating Temperature .. 85°C

DIMENSIONS

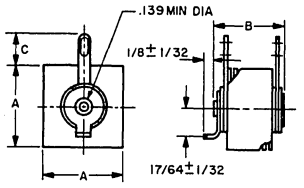


FIGURE 1

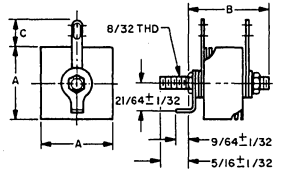


FIGURE 2

CHARACTERISTICS

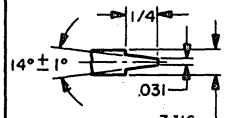
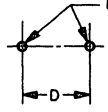
Max. Output (mA) DC	Dimensions (inches) Fig. No.	Cell Size (A)	Mtg Dim. (B) Max.	Term. Hgt (C) Max.	Series Resist. (Min.)	ITT Part No.
10		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1158
15		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5152
20		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1159
30		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5153
65	1	1	9/16	21/64	22	1002A
	1	1	9/16	13/32	22	1444(1)
	1	11/16	23/32	31/64	22	1263A
	1	11/16	21/32	9/16	22	1526(1)
	—	11/16	BKT MTD	31/64	22	1263B
75	1	1	3/4	21/64	22	1003A
	1	1	3/4	13/32	22	1445(1)
	1	11/16	21/32	31/64	22	6H75AE
100	1	1-1/4	3/4	25/64	22	1004A
	1	1	1-1/8	21/64	22	1101A
	1	1	1-1/8	13/32	22	1504(1)
	1	1	3/4	21/64	7.5	6H100AE
150	1	1-1/4	1	25/64	15	1005A
	1	1	1-1/8	21/64	7.5	6H150AE
200	1	1-1/2	1	31/64	4.7	1006A
	2	1	2	21/64	4.7	6H200A
250	1	1-1/2	1-1/8	31/64	4.7	1028A
	1	1-1/4	1-1/4	25/64	4.7	6H250AE
300	2	1-1/2	2-7/32	19/32	4.7	1090A
	1	1-1/4	1-13/32	25/64	4.7	6H300AE
350	2	1-3/4	2-7/32	19/32	4.7	1023A
	2	1-5/8	2-7/32	17/32	4.7	1356A
	2	1-1/4	2	25/64	4.7	6H350A
400	2	1-3/4	2-1/4	19/32	4.7	1277A
	1	1-1/2	1-1/2	31/64	4.7	6H400AE
450	2	2	2-7/32	15/32	4.7	1021A
	2	1-1/2	2-7/32	31/64	3.3	6H450A
500	2	2	2-7/32	15/32	4.7	1179A
	2	1-3/4	1-13/16	19/32	3.3	6H500A
600	2	2	2-1/2	15/32	4.7	1289A
	2	1-3/4	2	19/32	3.3	6H600A
750	2	2	2	15/32	3.3	6H750A

NOTE: Rectifier terminals designed for mounting in a printed circuit board. The "B" dimension listed here is the overall length; see page 4 for mounting information.

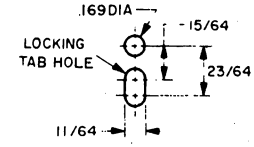
OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS, continued

MOUNTING DETAILS

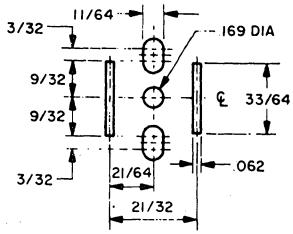
Taper Tip Design . . . for maximum ease of insertion in heavy-gauge printed circuit boards up to ⅛" thick. The tapered terminal may be inserted into round, diamond-shaped, or rectangular holes. Taper design keeps the rectifier plates off the board. As a result, the flow of cooling air through the cells is improved, and extra board area is freed beneath the rectifier for additional printing.

Mounting Detail	Terminal Detail	Rectifier Code No.	Dimension "D"
		1444	5/16
		1445	15/32
		1504	7/8
		1526	13/32

MOUNTING HOLES

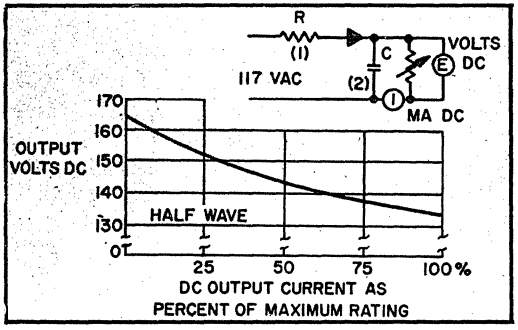


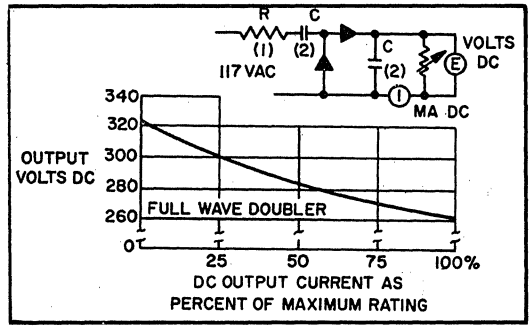
Mounting hole layout for stud and eyelet rectifiers.

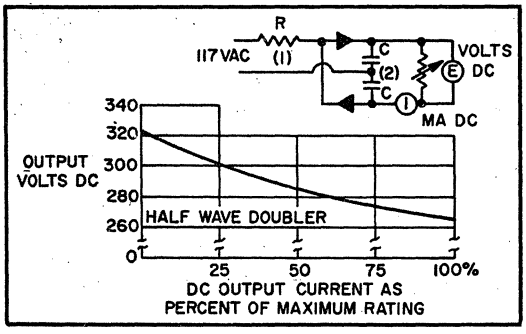


Mounting hole layout for clip mounted rectifiers; will also permit mounting of stud type rectifiers.

CIRCUIT DIAGRAMS and TYPICAL VOLTAGE REGULATION CURVES







NOTES:

1. Minimum series resistance specified in characteristics table.
2. Minimum filter capacitance in MFD to be ½ rectifier rating in milliamperes.

CLIP TYPE SELENIUM RECTIFIERS

CHARACTERISTICS FOR CAPACITIVE LOAD

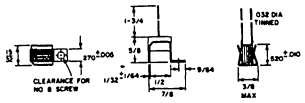
Nominal RMS Input Voltage	117
Maximum RMS Input Voltage	130
Maximum Peak Reverse Voltage	380
Maximum Peak Current (mA)	650
Maximum RMS Current (mA)	175
Maximum DC Output Current (mA)	65
Minimum Recommended Series Resistance (Ohms)	22
Maximum Cell Operating Temperature (°C)	85
Maximum Forward Voltage Drop (dc)	10
Dielectric Strength (Volts for 1 Min.)	900
Output Voltage with 117 Volts Input and 100 μf Capacitor and 65 mA dc (Volts)	130

ENVIRONMENTAL CHARACTERISTICS

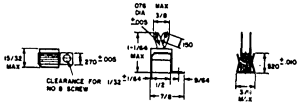
Humidity—Withstands 120 hours in 95% +RH at 65°C.

Vibration—Withstands 10 to 55 cps., .060" displacement for 2 hours in each plane.

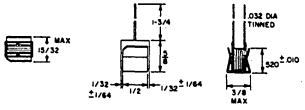
DIMENSIONS



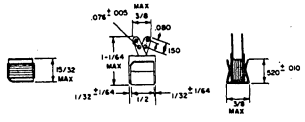
6H65HW



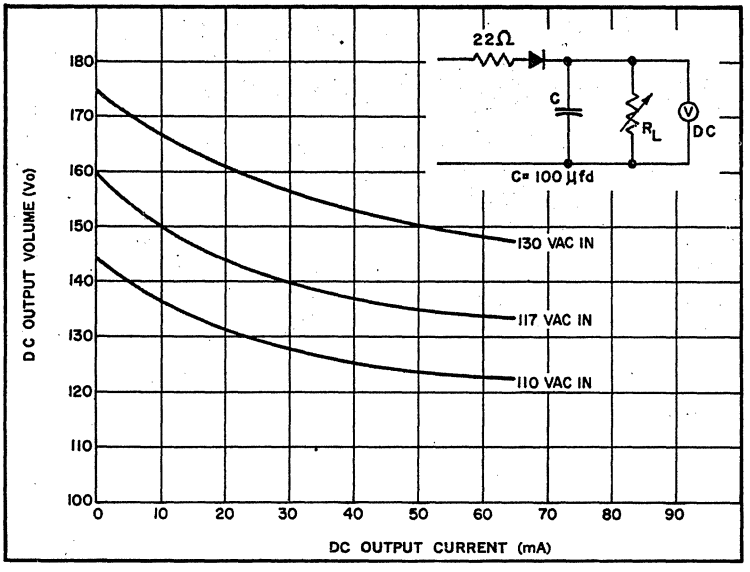
6H65F



6H65FW



6H65H

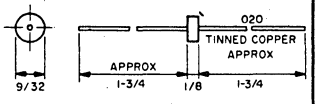


MINIATURE SELENIUM DIODES

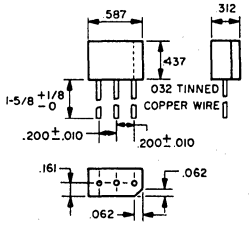
CHARACTERISTICS

AC APPLICATIONS	ITT Part No. 1215	ITT Part No. K1615AC K1616AC K1617AC
Max. DC forward current (mA)	.25	—
Max. peak forward current (mA)	2.5	—
Max. RMS input volts, resistive load	40	—
Max. peak reverse volts, resistive load	56	—
Max. peak reverse volts, capacitive load	68	—
*Max. shunt capacitance in $\mu\mu$f at 1 kc and —10 volts bias	—	50
Max. shunt capacitance unbalance ($\mu\mu$f)	—	5
Max. shunt capacitance in $\mu\mu$f at 200 kc	22	—
Max. ambient temperature	55°C	85°C
DC APPLICATIONS		
Max pure DC forward current (mA)	.37	.15
Max. continuous reverse volts	30	20
Max. reverse current at 40 volts (μA)	6	—
Max. reverse current at 20 volts (μA)	—	4

DIMENSIONS

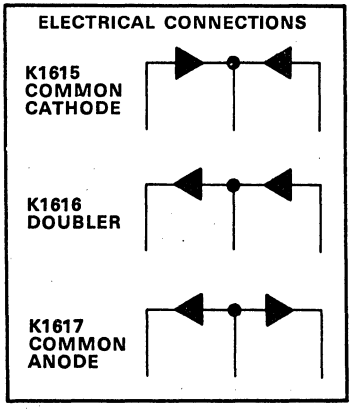


ITT Part Nos.
K1615AC, K1616AC, K1617AC



ITT Part No. 1215

ELECTRICAL CONNECTIONS



ITT SEMICONDUCTORS

1N746 THROUGH 1N759
ZENER DIODES

400mW, 3.3 VOLTS TO 12 VOLTS SILICON GLASS ZENER DIODES

FEATURES

- **Hermetically sealed**
- **Rugged construction**
- **Planar, nitride passivated**
- **Low dynamic impedance**
- **Weldable leads**

ITT's glass zeners are inherently reliable and are ideally suited for use under stringent environmental conditions. The applications include: Computers, Instruments, Automotive, Industrial and Entertainment markets.

DYNAMIC IMPEDANCE

The Zener Impedance is derived from the 60Hz AC voltage which results when an AC current having an RMS value equal to 10% of the DC Zener current (I_{zt} or I_{zk}) is superimposed on I_{zt} or I_{zk}. Zener Impedance is measured at two points to insure a sharp knee on the break down curve and eliminates unstable units.

IDENTIFICATION OF SYMBOLS

I_z	Zener Current
Z_z	Zener impedance
I_{zt}	Zener test current
V_z	Nominal Zener voltage
Z_{zt}	Zener impedance at test current (I_{zt})
I_{zk}	Zener current near breakdown knee
Z_{zk}	Zener impedance near breakdown knee (I_{zk})
I_{zm}	Maximum DC Zener current (limited by power dissipation)
If	Forward current
Vf	Forward voltage

ABSOLUTE MAXIMUM RATINGS

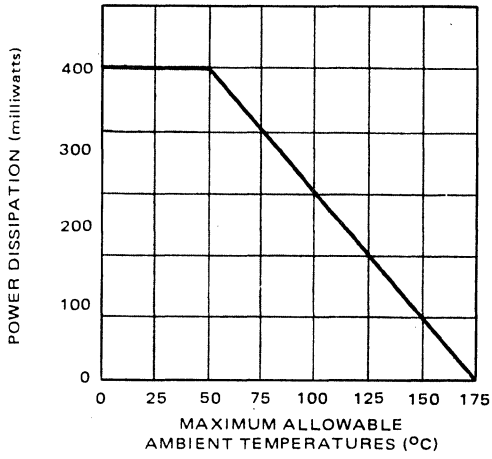
Characteristics	Units
Max power dissipation @ 50°C	400mW
Derating factor	3.2mW/°C
Max forward voltage @ 200 ma.....	1.2volts
Operating and storage temperature range	−65°C to 175°C

ELECTRICAL SPECIFICATIONS @ 25°C

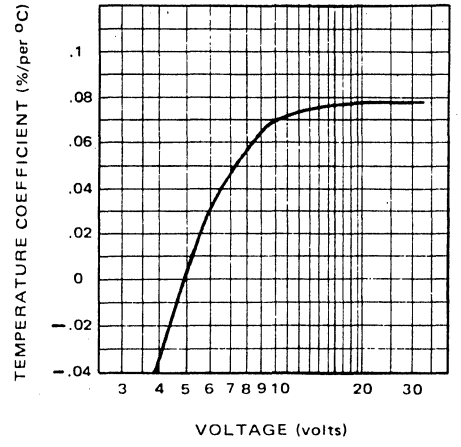
Type Number	Regulator Voltage (V_Z)	Test Current (I_{ZT})	Maximum Dynamic Impedance (Z_{ZT})	Maximum Regulator Current (I_{zm})	Maximum Reverse Current @ Vr=1.0V (I_R)		Typical Temperature Coefficient
					T_A=25°C	T_A=150°C	
	v	ma	ohms	ma	μa	μa	%/°C
1N746	3.3	20	28	110	10	30	− .062
1N747	3.6	20	24	100	10	30	− .055
1N748	3.9	20	23	95	10	30	− .049
1N749	4.3	20	22	85	2	30	− .036
1N750	4.7	20	19	75	2	30	− .018
1N751	5.1	20	17	70	1	20	− .008
1N752	5.6	20	11	65	1	20	+ .006
1N753	6.2	20	7	60	0.1	20	+ .022
1N754	6.8	20	5	55	0.1	20	+ .035
1N755	7.5	20	6	50	0.1	20	+ .045
1N756	3.2	20	8	45	0.1	20	+ .052
1N757	9.1	20	10	40	0.1	20	+ .056
1N758	10.0	20	17	35	0.1	20	+ .060
1N759	12.0	20	30	30	0.1	20	+ .060

1N746 THROUGH 1N759
ZENER DIODES

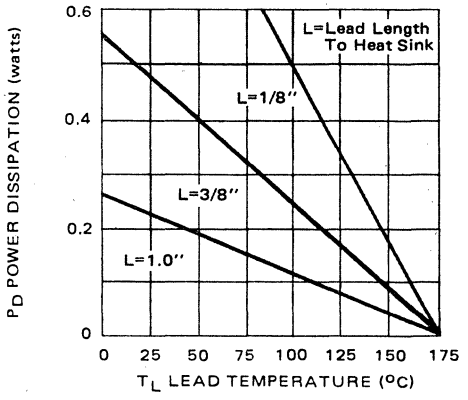
TEMPERATURE RATING



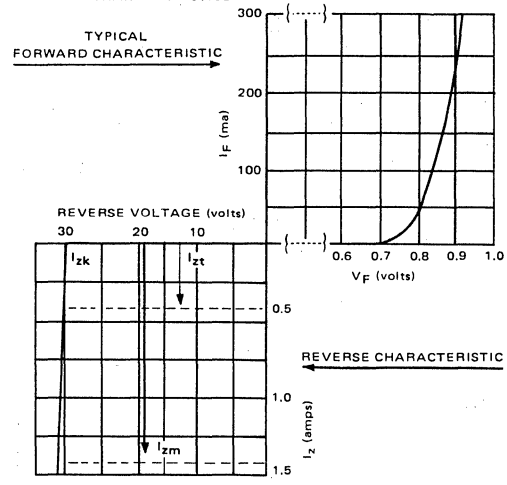
TEMPERATURE COEFFICIENT
(TYPICAL) VS. VOLTAGE



POWER TEMPERATURE DERATING CURVE



ZENER CHARACTERISTICS



400 mW, 6.8 VOLTS TO 33 VOLTS SILICON GLASS ZENER DIODES

- **Hermetically sealed**
- **Rugged construction**
- **Planar, nitride passivated**
- **Low dynamic impedance**
- **Weldable leads**

ITT's glass zeners are inherently reliable and are ideally suited for use under stringent environmental conditions. The applications include: Computers, Instruments, Automotive, Industrial and Entertainment markets.

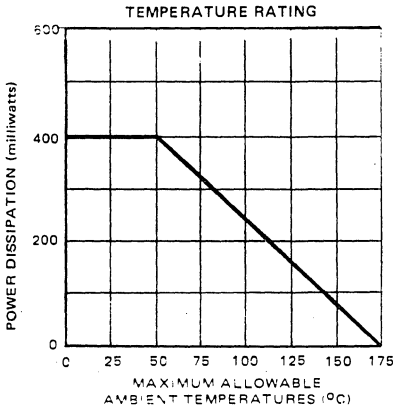
ABSOLUTE MAXIMUM RATINGS

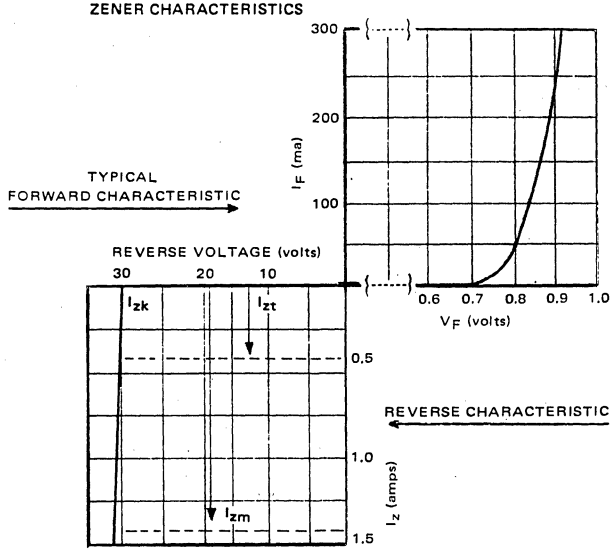
Characteristics	Units
Max power dissipation @ 50°C	400mW
Derating factor	3.2mW/°C
Max forward voltage @ 200 ma.....	1.2volts
Operating and storage temperature range	−65°C to 175°C

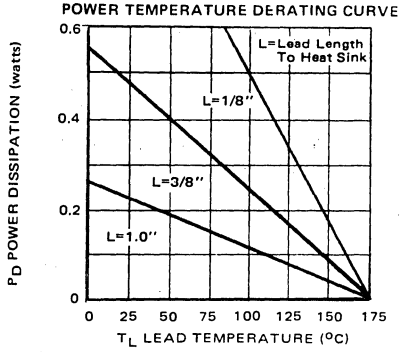
ELECTRICAL SPECIFICATIONS @ 25°C

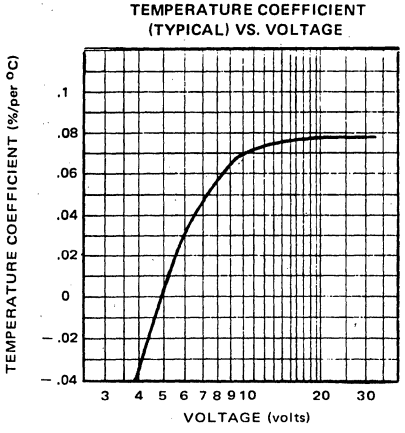
Type Number	Regulator Voltage (V_Z)	Test Current (I_{Zt})	Maximum Dynamic Impedance (Z_{Zt})	Maximum Reverse Current (I_R) 25°C	I_R Test Voltage (V_R) (For A Suffix)	I_R Test Voltage (V_R) (For B Suffix)	Maximum Regulator Current (I_{ZM})	Maximum Knee Impedance (Z_{zk}) Zzk @ Izk		Typical Temperature Coefficient
	v	ma de	ohms	μa	v	v	ma	ohms	ma	%/°C
1N957	6.8	18.5	4.5	150	4.9	5.2	47	700	1.0	+.050
1N958	7.5	16.5	5.5	75	5.4	5.7	42	700	0.5	+.058
1N959	8.2	15	6.5	50	5.9	6.2	38	700	0.5	+.062
1N960	9.1	14	7.5	25	6.6	6.9	35	700	0.5	+.068
1N961	10	12.5	8.5	10	7.2	7.6	32	700	0.25	+.075
1N962	11	11.5	9.5	5	8.0	8.4	28	700	0.25	+.076
1N963	12	10.5	11.5	5	8.6	9.1	26	700	0.25	+.077
1N964	13	9.5	13	5	9.4	9.9	24	700	0.25	+.079
1N965	15	8.5	16	5	10.8	11.4	21	700	0.25	+.082
1N966	16	7.8	17	5	11.5	12.2	19	700	0.25	+.083
1N967	18	7.0	21	5	13.0	13.7	17	750	0.25	+.085
1N968	20	6.2	25	5	14.4	15.2	15	750	0.25	+.086
1N969	22	5.6	29	5	15.8	16.7	14	750	0.25	+.087
1N970	24	5.2	33	5	17.3	18.2	13	750	0.25	+.088
1N971	27	4.6	41	5	19.4	20.6	11	750	0.25	+.090
1N972	30	4.2	49	5	21.6	22.8	10	1000	0.25	+.091
1N973	33	3.8	58	5	23.8	25.1	9.2	1000	0.25	+.092

IN957 THRU IN973
ZENER DIODES









IDENTIFICATION OF SYMBOLS

Iz	Zener current	Zzk	Zener impedance near breakdown knee (Izk)
Zz	Zener impedance	Izm	Maximum DC Zener current (limited by power dissipation)
Izt	Zener test current	If	Forward current
Vz	Nominal Zener voltage	Vf	Forward voltage
Zzt	Zener impedance at test current (Izt)		
Izk	Zener current near breakdown knee		

DYNAMIC IMPEDANCE

The Zener Impedance is derived from the 60Hz AC voltage which results when an AC current having an RMS value equal to 10% of the DC Zener current (Izt or Izk) is superimposed on Izt or Izk. Zener Impedance is measured at two points to insure a sharp knee on the breakdown curve and eliminates unstable units.

1 WATT, 3.6 VOLTS TO 33 VOLTS SILICON GLASS ZENER DIODES

- **Hermetically sealed**
- **Rugged construction**
- **Planar, nitride passivated**
- **Low dynamic impedance**
- **Weldable leads**

ITT's glass zeners are inherently reliable and are ideally suited for use under stringent environmental conditions. The applications include: Computers, Instruments, Automotive, Industrial and Entertainment markets.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Max power dissipation @ 50°C	1.0 watt
Derating factor	6.67 mw/°C
Max forward voltage @ 200 ma	1.2 volts
Operating and storage temperature range	−65°C to 200°C

ELECTRICAL SPECIFICATIONS @ 25°C

Jedec Type Number	Nominal Zener Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Zener Impedance			Reverse Leakage Current		Surge Current @ T_A=25°C I_R	Max DC Zener Current I_{ZM} mA
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} Ohms	I_{ZK} mA	I_R uA Max	V_R Volts		
1N4729	3.6	69	10	400	1.0	10	1	1,260	252
1N4730	3.9	64	9	400	1.0	10	1	1,190	234
1N4731	4.3	58	9	400	1.0	10	1	1,070	217
1N4732	4.7	53	8	500	1.0	10	1	970	193
1N4733	5.1	49	7	550	1.0	10	1	890	178
1N4734	5.6	45	5	600	1.0	10	2	810	162
1N4735	6.2	41	2	700	1.0	10	3	730	146
1N4736	6.8	37	3.5	700	1.0	10	4	660	133
1N4737	7.5	34	4.0	700	0.5	10	5	605	121
1N4738	8.2	31	4.5	700	0.5	10	6	550	110
1N4739	9.1	28	5.0	700	0.5	10	7	500	100
1N4740	10	25	7	700	0.25	10	7.6	454	91
1N4741	11	23	8	700	0.25	5	8.4	414	83
1N4742	12	21	9	700	0.25	5	9.1	380	76
1N4743	13	19	10	700	0.25	5	9.9	344	69
1N4744	15	17	14	700	0.25	5	11.4	304	61
1N4745	16	15.5	16	700	0.25	5	12.2	285	57
1N4746	18	14	20	750	0.25	5	13.7	250	50
1N4747	20	12.5	22	750	0.25	5	15.2	225	45
1N4748	22	11.5	23	750	0.25	5	16.7	205	41
1N4749	24	10.5	25	750	0.25	5	18.2	190	38
1N4750	27	9.5	35	750	0.25	5	20.6	170	34

1N4729 THROUGH 1N4752
ZENER DIODES

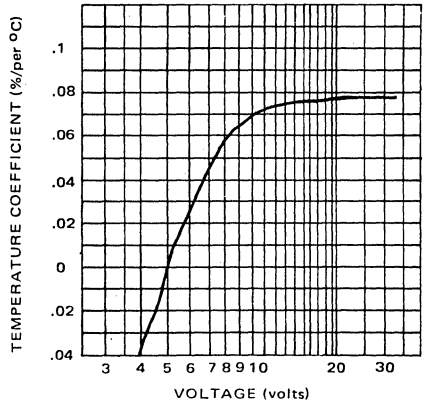
ELECTRICAL SPECIFICATIONS @ 25°C

Jedec Type Number	Nominal Zener Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Zener Impedance			Reverse Leakage Current		Surge Current @ T_A=25°C I_R	Max DC Zener Current I_{ZM} mA
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} Ohms	I_{ZK} mA	I_R uA Max	V_R Volts		
1N4751	30	8.5	40	1,000	0.25	5	22.8	150	30
1N4752	33	7.5	45	1,000	0.25	5	25.1	135	27

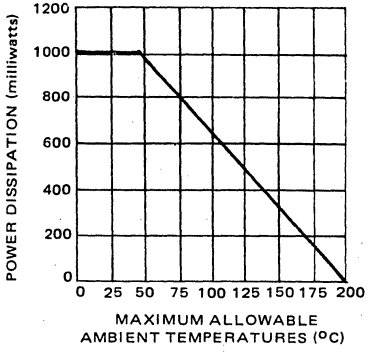
Standard Tolerance is ± 10%. Add Suffix "A" for ± 5% Tolerance.

Other Tolerances Available Upon Request — Consult the Factory for Non-Standard Voltages.

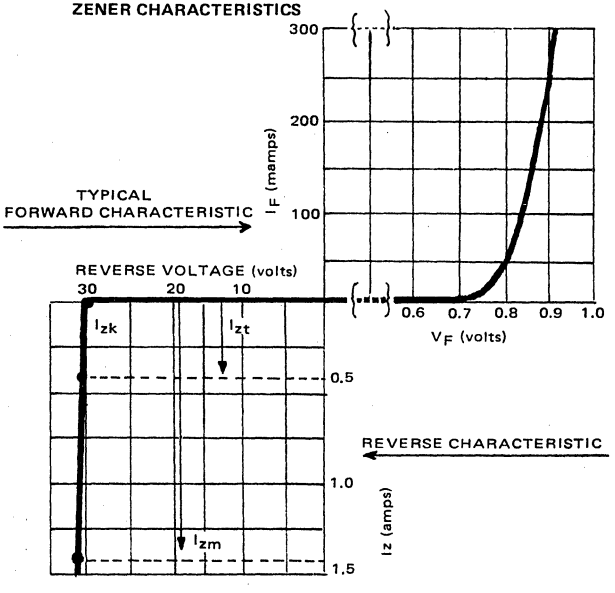
TEMPERATURE COEFFICIENT (TYPICAL) VS. VOLTAGE



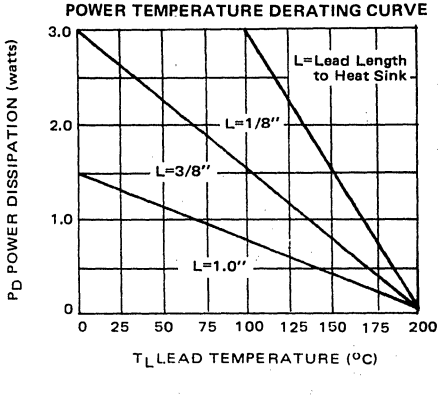
TEMPERATURE RATING



ZENER CHARACTERISTICS



POWER TEMPERATURE DERATING CURVE



IDENTIFICATION OF SYMBOLS

I_z Zener Current

Z_z Zener impedance

I_{zt} Zener test current

V_z Nominal Zener voltage

Z_{zt} Zener impedance at test current (I_{zt})

I_{zk} Zener current near breakdown knee

Z_{zk} Zener impedance near breakdown knee (I_{zk})

I_{zm} Maximum DC Zener current (limited by power dissipation)

If Forward current

Vf Forward voltage

DYNAMIC IMPEDANCE

The Zener Impedance is derived from the 60H_z AC voltage which results when an AC current having an RMS value equal to 10% of the DC Zener current (I_{zt} or I_{zk}) is superimposed on I_{zt} or I_{zk}. Zener Impedance is measured at two points to insure a sharp knee on the break down curve and eliminates unstable units.

500mW, 3.3 VOLTS TO 33 VOLTS SILICON GLASS ZENER DIODES

FEATURES

- **Hermetically sealed**
- **Rugged construction**
- **Planar, nitride passivated**
- **Low dynamic impedance**
- **Weldable leads**

ITT's glass zeners are inherently reliable and are ideally suited for use under stringent environmental conditions. The applications include: Computers, Instruments, Automotive, Industrial and Entertainment markets.

ABSOLUTE MAXIMUM RATINGS

Max power dissipation @T_L=75°C 500mW
Derating factor above 75°C ..... 4.0mW/°C
Max forward voltage @ 200 ma .... 1.1 volts
Operating and storage temperature range ..... −65°C to 200°C

ELECTRICAL SPECIFICATIONS @ 25 C

Type Number	Regulator Voltage (V_Z)	Test Current (I_{ZT})	Maximum Dynamic Impedance (Z_{ZT})	Maximum Reverse Current (I_R) 25°C	I_R Test Voltage (V_R) (For A Suffix)	I_R Test Voltage (V_R) (For B Suffix)	Maximum Regulator Current (I_{ZM})	Maximum Dynamic Knee Impedance Zzk	Typical Temperature Coefficient
	v	ma de	ohms	μ	v	v	ma	ohms	%/°C
1N5226	3.3	20	28	25	0.95	1.0	138	1600	−.070
1N5227	3.6	20	24	15	0.95	1.0	126	1700	−.065
1N5228	3.9	20	23	10	0.95	1.0	115	1900	−.060
1N5229	4.3	20	22	5	0.95	1.0	106	2000	−.055
1N5230	4.7	20	19	5	1.9	2.0	97	1900	±.030
1N5231	5.1	20	17	5	1.9	2.0	89	1600	±.030
1N5232	5.6	20	11	5	2.9	3.0	81	1600	+.038
1N5233	6.0	20	7	5	3.3	3.5	76	1600	+.038
1N5234	6.2	20	7	5	3.8	4.0	73	1000	+.045
1N5235	6.8	20	5	3	4.8	5.0	67	750	+.050
1N5236	7.5	20	6	3	5.7	6.0	61	500	+.058
1N5237	8.2	20	8	3	6.2	6.5	55	500	+.062
1N5238	8.7	20	8	3	6.2	6.5	52	600	+.065
1N5239	9.1	20	10	3	6.7	7.0	50	600	+.068
1N5240	10	20	17	3	7.6	8.0	45	600	+.075

1N5226 THROUGH 1N5257
ZENER DIODES

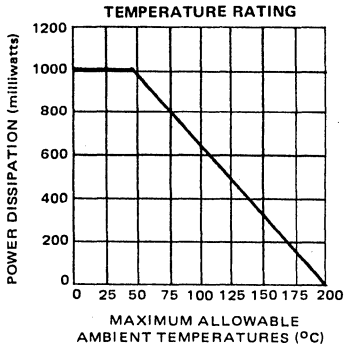
ELECTRICAL SPECIFICATIONS @ 25 C

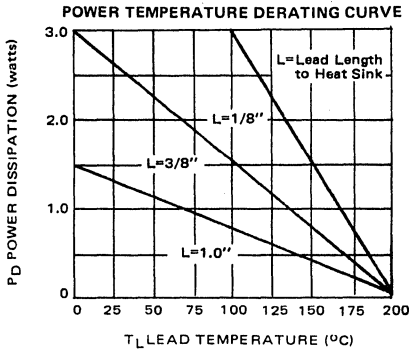
Type Number	Regulator Voltage (V_Z)	Test Current (I_{ZT})	Maximum Dynamic Impedance (Z_{ZT})	Maximum Reverse Current (I_R) 25°C	I_R Test Voltage (V_R) (For A Suffix)	I_R Test Voltage (V_R) (For B Suffix)	Maximum Regulator Current (I_{ZM})	Maximum Dynamic Knee Impedance Zzk	Typical Temperature Coefficient
	v	ma de	ohms	μ	v	v	ma	ohms	%/°C
1N5241	11	20	22	2	8.0	8.4	41	600	+.076
1N5242	12	20	30	1	8.7	9.1	38	600	+.077
1N5243	13	9.5	13	0.5	9.4	9.9	35	600	+.079
1N5244	14	9.0	15	0.1	9.5	10	32	600	+.082
1N5245	15	8.5	16	0.1	10.5	11	30	600	+.082
1N5246	16	7.8	17	0.1	11.4	12	28	600	+.083
1N5247	17	7.4	19	0.1	12.4	13	27	600	+.084
1N5248	18	7.0	21	0.1	13.3	14	25	600	+.085
1N5249	19	6.6	23	0.1	13.3	14	24	600	+.086
1N5250	20	6.2	25	0.1	14.3	15	23	600	+.086
1N5251	22	5.6	29	0.1	16.2	17	21	600	+.087
1N5252	24	5.2	33	0.1	17.1	18	19.1	600	+.088
1N5253	25	5.0	35	0.1	18.1	19	18.2	600	+.089
1N5254	27	4.6	41	0.1	20	21	16.8	600	+.090
1N5255	28	4.5	44	0.1	20	21	16.2	600	+.091
1N5256	30	4.2	49	0.1	22	23	15.1	600	+.091
1N5257	33	3.8	58	0.1	24	25	13.8	700	+.092

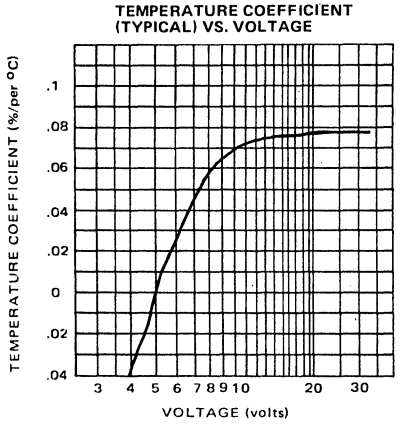
1ZK=6.25ma

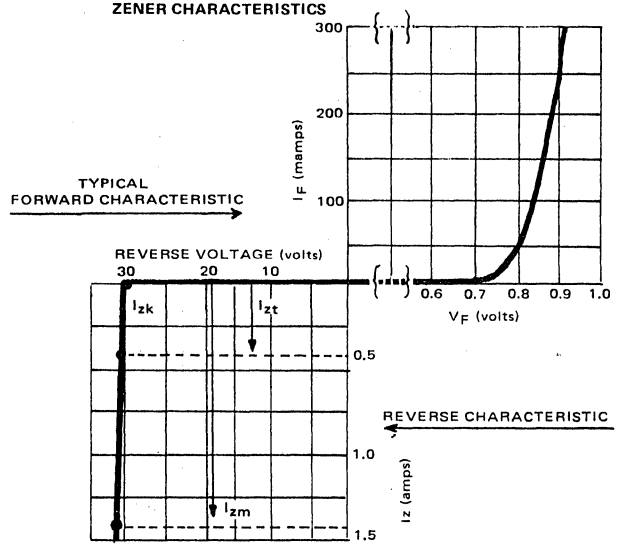
Standard tolerance is ±20%. Add suffix "A" for ±10% tol., suffix "B" for ±5% tol.

Consult factory for other tolerances and non-standard voltages.









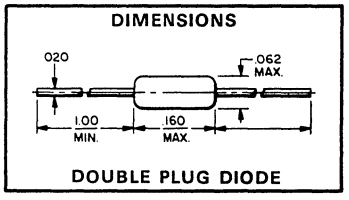
IDENTIFICATION OF SYMBOLS

Iz	Zener current	Zzk	Zener impedance near breakdown knee (Izk)
Zz	Zener impedance		
Izt	Zener test current	Izm	Maximum DC Zener current (limited by power dissipation)
Vz	Nominal Zener voltage		
Zzt	Zener impedance at test current (Izt)	If	Forward current
		Vf	Forward voltage
Izk	Zener current near breakdown knee		

DYNAMIC IMPEDANCE

The Zener Impedance is derived from the 60Hz AC voltage which results when an AC current having an RMS value equal to 10% of the DC Zener current (Izt or Izk) is superimposed on Izt or Izk. Zener Impedance is measured at two points to insure a sharp knee on the breakdown curve and eliminates unstable units.

SILICON PLANAR EPITAXIAL TUNER DIODE



The ITT silicon planar epitaxial tuner diode is intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.

ABSOLUTE MAXIMUM RATINGS

		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

SYMBOL		ITT 109			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
C_J			30.0		pF	$V_R = 3V$
		4.2		6.5	pF	$V_R = 25V$
$\frac{C(V=3V)}{C(V=25V)}$		5				
R_S			0.5		Ohms	$V_R = 3V$, f = 100 MHz
Q		200	280			$V_R = 3V$, f = 47MHz
		90				$V_R = 3V$, f = 100MHz
		55				$V_R = 3V$, f = 170MHz
L_S			2.5 nH			
I_R				0.5	μA	$V_R = 28V$

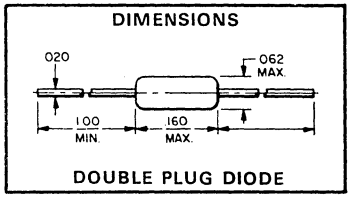
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is $\pm$ 1.5%.

These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

SILICON PLANAR EPITAXIAL TUNER DIODES

(LOW INDUCTANCE)



ITT silicon planar epitaxial tuner diodes are intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF and UHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts
Soldering temperature (5 secs. at body of diode package)	260	°C

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

SYMBOL	ITT 141			ITT 142			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
C_J		11			12		pF	$V_R = 3V$
		2.2	2.5	2.0	2.5	3.0	pF	$V_R = 25V$
$\frac{C_{3.0V}}{C_{25V}}$	4.5	4.8	5.5 5.2	4.0	4.8	6.0		
R_S		0.5			1.0		Ohms	$V_R = 3V$, $f \approx 330$ MHz
Q	300			160				$V_R = 3V$, f=47MHz
				80				$V_R = 3V$, f=100MHz
	80			50				$V_R = 3V$, f=170MHz
	30							$V_R = 3V$, f=470MHz
f_c	20			10			GHz	$V_R = 3V$, Q = 1.0
f_o	2.5			2.2			GHz	$V_R = 25V$
L_S		2.5			2.5		nH	At body of diode package
V_{BR}	30			30			Volts	
I_R			5.0			5.0	μA	$V_R = 28V$

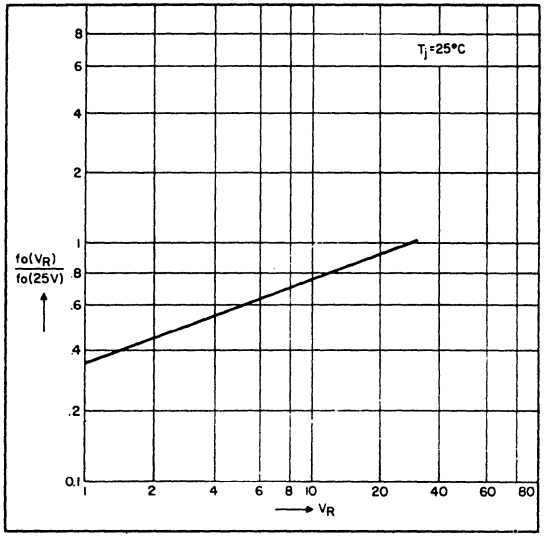
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is ± 1.5%.

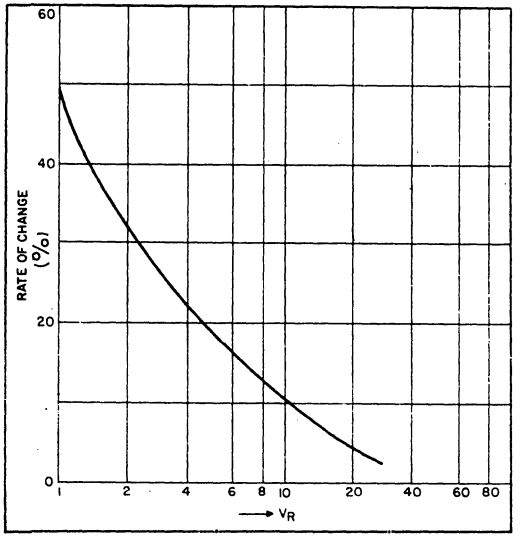
These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

TYPICAL CHARACTERISTICS

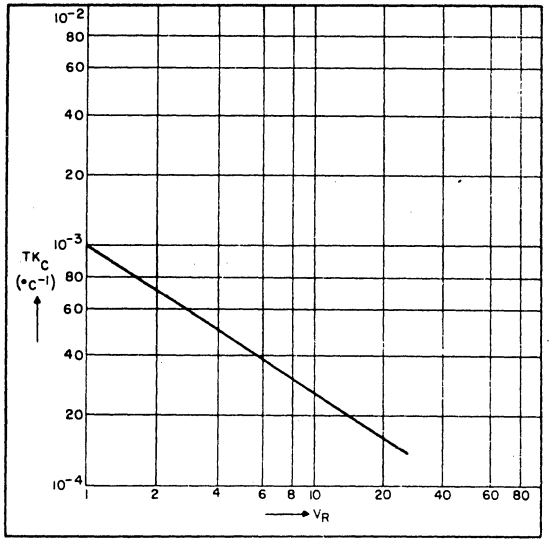
SERIES RESONANCE FREQUENCY AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



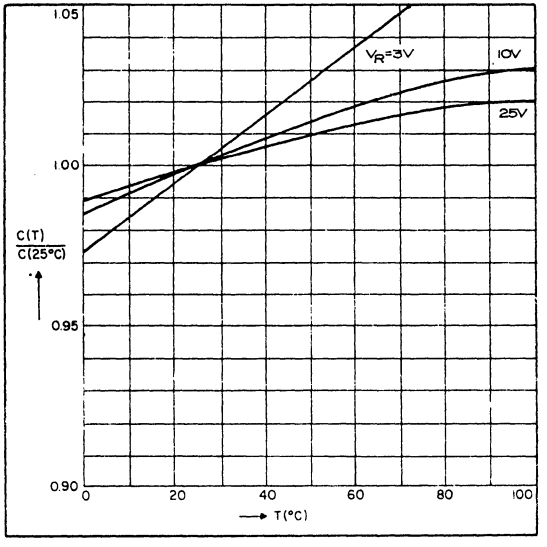
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



TEMPERATURE COEFFICIENT AS A FUNCTION OF VOLTAGE, RELATIVE VALUES

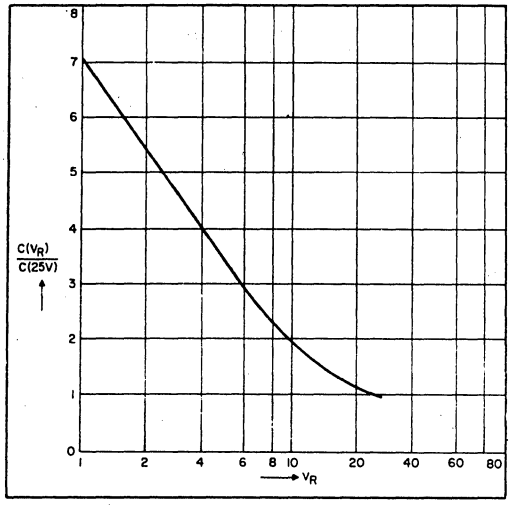


CAPACITANCE AS A FUNCTION OF TEMPERATURE, RELATIVE VALUES

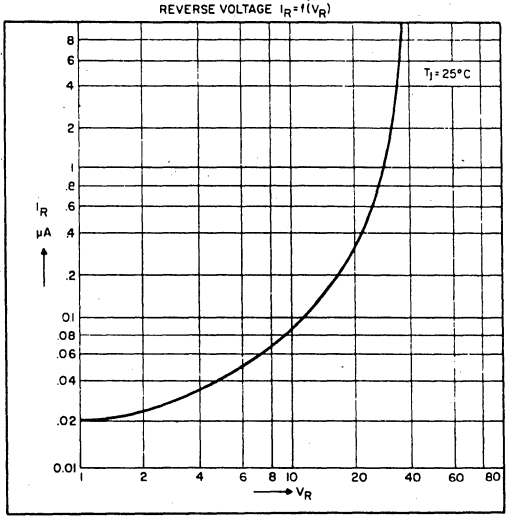


TYPICAL CHARACTERISTICS, continued

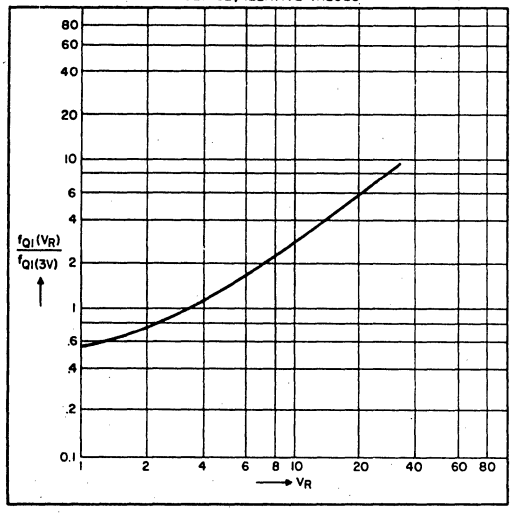
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



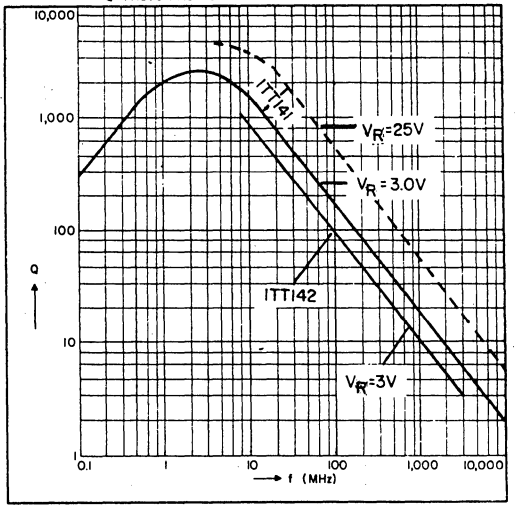
REVERSE CURRENT AS FUNCTION OF REVERSE VOLTAGE $I_R = f(V_R)$



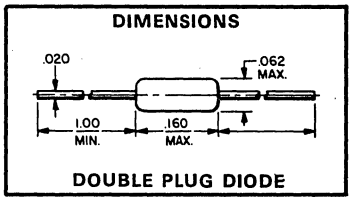
CUTOFF FREQUENCY (fc) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



Q-FACTOR AS FUNCTION OF FREQUENCY Q = f(f)



SILICON PLANAR EPITAXIAL CAPACITANCE DIODE



The ITT-210 is an improved variable capacitance diode intended for television receiver Automatic Frequency Control and other tuning applications between 1 and 1,000 MHz.

ABSOLUTE MAXIMUM RATINGS

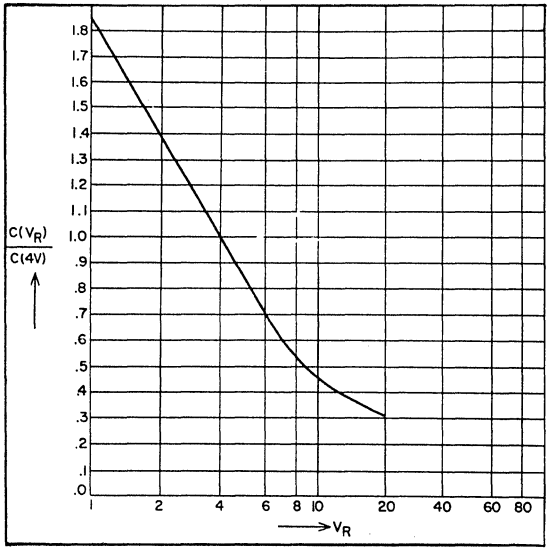
CHARACTERISTICS		UNITS
Reverse Voltage Breakdown @ 5μa	20	Volts
Power Dissipation @ 50°C	150	MW
Operating Temperature Range	0 to 100	°C
Storage Temperature Range	−50 to + 150	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

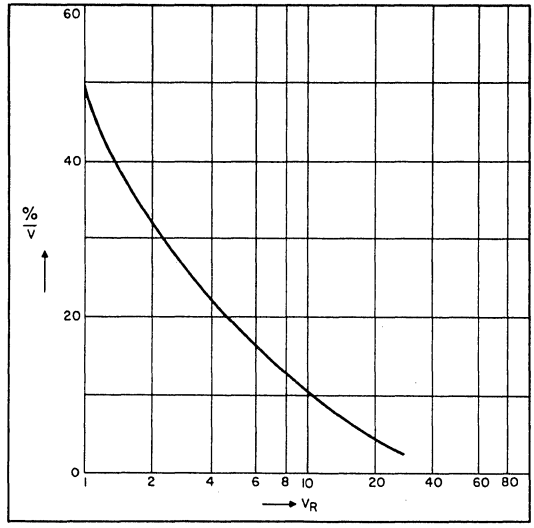
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C	8	20	12	pF	$V_r = 1.0V$
		10		pF	$V_r = 4V$
		8.3		pF	$V_r = 6V$
		5		pF	$V_r = 10V$
Rs		1.0		ohms	F = 30 MHz $V_r = 2V$
Q		540			F = 30 MHz $V_r = 5V$
V_F		.85	1.5	V.	$I_F = 60mA$

TYPICAL CHARACTERISTICS

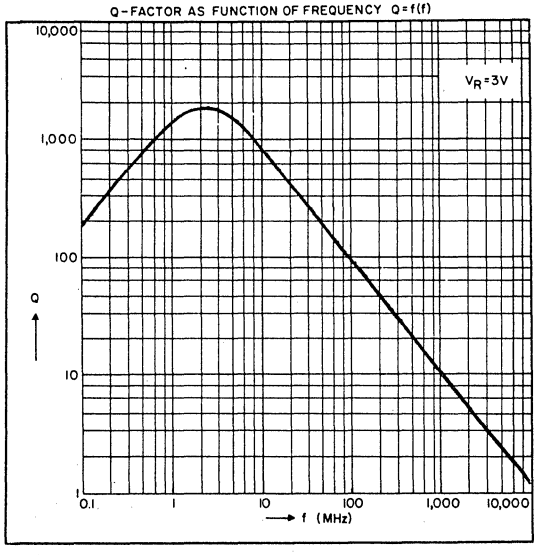
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



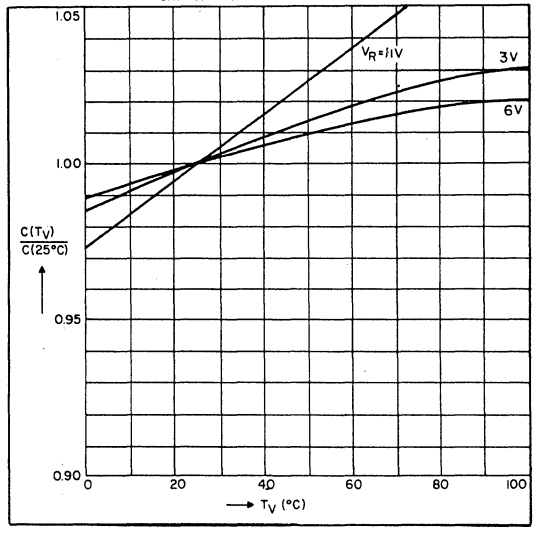
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



Q-FACTOR AS FUNCTION OF FREQUENCY Q=f(f)



TEMPERATURE AS FUNCTION OF JUNCTION CAPACITANCE (C) RELATIVE VALUES



UHF/VHF WAVE BAND SWITCH

Silicon planar epitaxial diode

Glass package DO-35

Low and consistant inductance

Silicon nitride passivated

MAXIMUM RATINGS

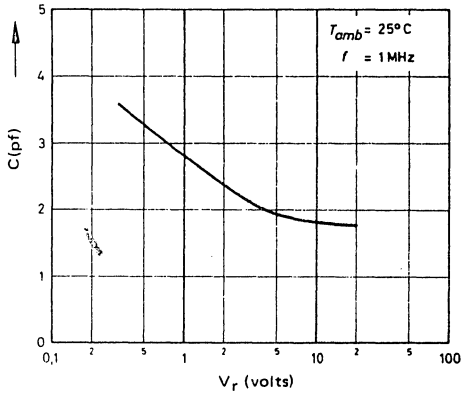
Operating and storage temperature range ...— 65°C to + 150°C

Maximum forward voltage drop at 100mA 1.2V

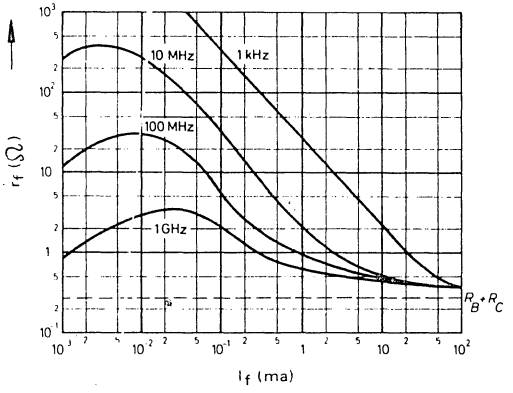
The ITT243/244 is a diode switch with low dynamic impedance in the ON-stage over a wide frequency range of 1 MHz to 1000 MHz and low capacitance in the OFF-stage. The application for this device is switching of channels or bands in high frequency circuitry, especially in television tuners.

SPECIFICATIONS 25°C	ITT244	ITT243
Maximum dynamic forward impedance at 10mA and 50 to 100MHz	.5	1
Maximum capacitance at 15 volts	2pf	
Typical capacitance at 1 volt	3pf	
Maximum series inductance (case)	2.5nH	
PIV at 10uA	20V	
Maximum leakage at 15 volts	100nA	

TYPICAL DYNAMIC IMPEDANCE VS FORWARD CURRENT



TYPICAL FORWARD CURRENT VS VOLTAGE



VARIABLE BETWEEN 5pF and 60 pF
TUNER DIODES
V — SERIES

Silicon Planar Epitaxial Diode

Ion Implanted

Glass Package DO-35

Low and Consistent Inductance

High Soldering Temperature

A Tuning Diode is a voltage variable capacitor whose junction capacitance can be varied with bias voltage. The applications for this device are tuning and AFC of resonance circuits and transmission lines, especially in television and radio receivers.

MAXIMUM RATINGS

Operating and storage temperature range .....— 65°C to + 150°C

Soldering temperature for t = 10 seconds maximum .....350°C

Max forward voltage at 100mA 1V

MATCHING INFORMATION:

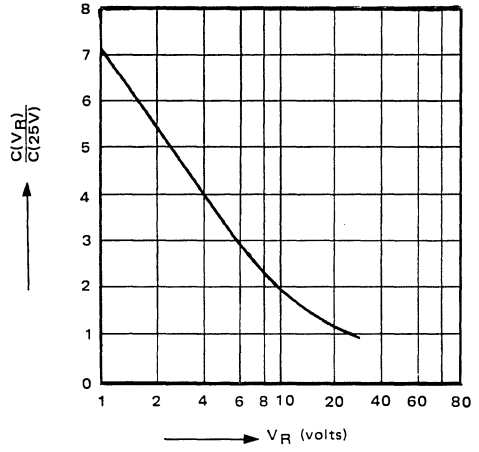
The capacitance matching is availble to within 1.5% over the entire voltage range. Different matching specifications available on request.

SPECIFICATIONS 25°C

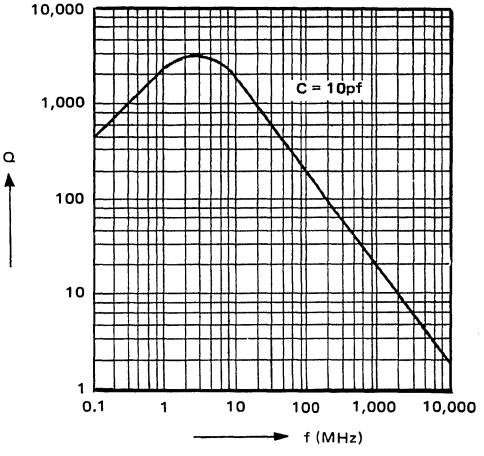
Type	PIV	IR Max. Capacitance		Capacitance VR		Capacitance VR		Minimum Capacitance Ratio		Min. Q-Factor 100 MHz
	(volts)	(ua)	(volts)	(pf.)	(volts)	(pf)	(volts)	ratio	CV1/CV2	
*V150	30	.5	28V	30	3V	4.2—6.5	25V	5	C3V/C25V	90; 3V
V151	28	.1	27V	26—32	3V	4.0—6.0	25V	5	C3V/C25V	90; 3V
V160	20	.1	15V	26—32	3V	6.0—9.0	15V			90; 4V
V161	20	.1	15V	20—30	4V	7.5	15V	2.5	C4V/C15V	90; 4V
V162	20	.1	15V	40 MIN.	1V					
V170	15	.1	12V	26—32	3V	7—11	12V			90; 4V
V171	15	.1	12V	20—30	4V	9—18	9V	1.7	C4V/C9V	90; 4V
V172	15	.1	9V	17—26	5V					
V180	12	.1	10V	40 MIN.	1V	8—14	10V	3	C1V/C10V	
V181	12	.1	9V	30—40	2V					

* This device is similar to the ITT109 Tuner Diode.
Capacitance is measured at 1 MHz.

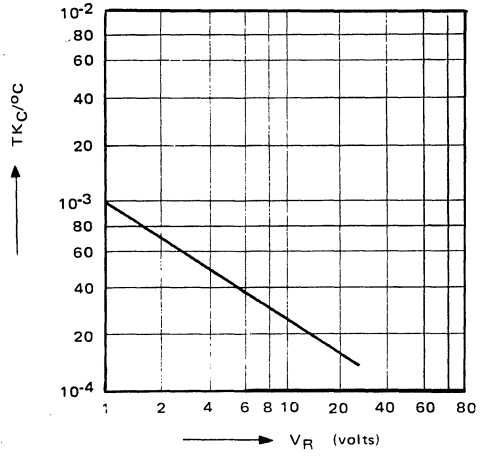
CAPACITANCE RATIO
AS A FUNCTION OF VOLTAGE



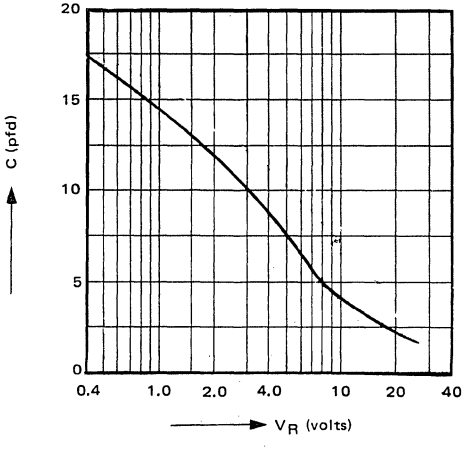
Q FACTOR AS FUNCTION OF FREQUENCY Q = (f)



TEMPERATURE COEFFICIENT AS A FUNCTION OF
VOLTAGE, RELATIVE VALUES



DIODE CAPACITANCE VS BIAS VOLTAGE



VARIABLE BETWEEN 2pF and 18pF TUNER DIODES U—SERIES

Silicon Planar Epitaxial Diode

Ion Implanted

Glass Package DO-35

Low and Consistent Inductance

High Soldering Temperature

A Tuning Diode is a voltage variable capacitor whose junction capacitance can be varied with bias voltage. The applications for this device are tuning and AFC of resonance circuits and transmission lines, especially in television and radio receivers.

MAXIMUM RATINGS

Operating and storage temperature range .....— 65°C to + 150°C

Soldering temperature for t = 10 seconds maximum .....350°C

Max forward voltage at 100mA 1V

MATCHING INFORMATION:

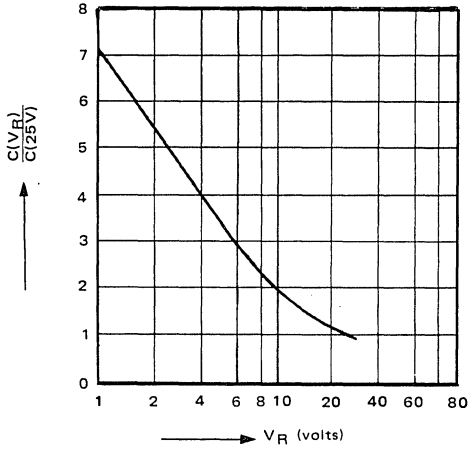
The capacitance matching is available to within 1.5% over the entire voltage range. Different matching specifications available on request.

SPECIFICATIONS 25°C

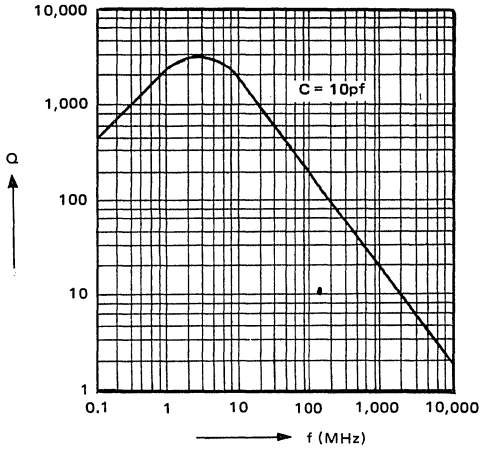
Type	PIV	IR MAX. VR		Capacitance VR		Capacitance VR		Minimum Capacitance Ratio		Min. Q-Factor 100 MHz
	(volts)	(ua)	(volts)	(pf)	(volts)	(pf.)	(volts)	ratio	CV1/CV2	
U150	30	.1	30V	9—14.04	3V	2.0—2.34	25V	4.5	3V/25V	230; 9pf
U151	30	.05	28V	10	3V	2.0—2.3	25V	4.5	3V/25V	240; 9pf
U152	30	.1	28V	12.5 MIN.	2V	2.25—2.55	25V			220; 9pf
(1)U153	30	5	28V	10	3V	2.5 MAX.	25V	4.5	3V/25V	140; 3V
U154	30	.1	28V	12.5 MIN.	2V	2.25—2.75	25V			170; 9pf
(2)U155	30	5	28V	10	3V	2.0—3.0	25V	4.0	3V/25V	-80; 3V
U160	20	.1	15V	7.0—11	4V	2.5—4.0	15V			100; 9pf
(3)U161	20			8—12	4V					160; 5V
U162	20	1	10V	7.5—11	4V			1.55	.5V/4V	
U170	15	1	10V	7—11	4V					100; 4V
U180	12	.1	10V	10	3V					

(1) Similar to ITT141
(2) Similar to ITT142 Capacitance is measured at 1MHz.
(3) Similar to ITT210

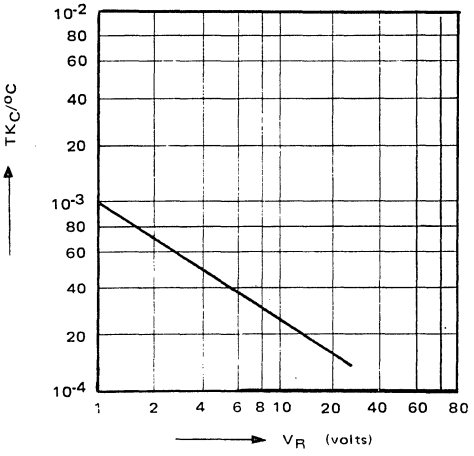
CAPACITANCE RATIO
AS A FUNCTION OF VOLTAGE



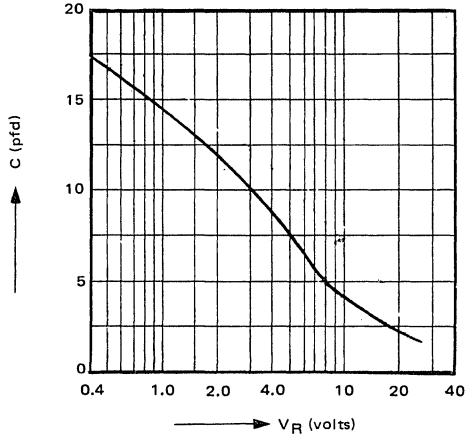
Q FACTOR AS FUNCTION OF FREQUENCY Q = (f)



TEMPERATURE COEFFICIENT AS A FUNCTION OF
VOLTAGE, RELATIVE VALUES



DIODE CAPACITANCE VS BIAS VOLTAGE



ITT SEMICONDUCTORS

1N3831 THROUGH **1N3846**

Package: DO-7

4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 100 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

ELECTRICAL SPECIFICATIONS

Type Number	Switching Voltage (V_S)		Reverse Breakdown Voltage (Min.)
	25°C	−40° to 85°C	
1N3831	20±4	14-25	12
1N3832	25±4	19-30	15
1N3833	30±4	23-36	18
1N3834	35±4	28-41	21
1N3835	40±4	32-46	24
1N3836	45±4	37-51	27
1N3837	50±4	41-57	30
1N3838	100±10	80-115	60
1N3839	20±4	14-25	12
1N3840	25±4	19-30	15
1N3841	30±4	23-36	18
1N3842	35±4	28-41	21
1N3843	40±4	32-46	24
1N3844	45±4	37-51	27
1N3845	50±4	41-57	30
1N3846	100±10	80-115	60

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

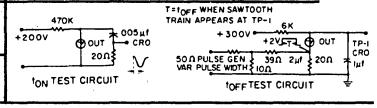
Marking:
The symbol for the 4-layer diode is a modified "4". The slant line of the "4" indicates the forward direction of current passing through the device when in the ON state.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_H (holding current)	0.5 14 5		15 50 40	mA mA mA mA	IN3831-38 IN3839-46 IN3831-38 @ −40°C IN3839-46 @ +85°C
I_{ik} (OFF state) (forward leakage current)			5	μA	60% of nom. V_S
V_{ON} (forward voltage drop)			1.2 2.7	V V	I_f = 70 mA I_f = 5A (pulsed)
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	
t_{off}		5		μsec	



HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

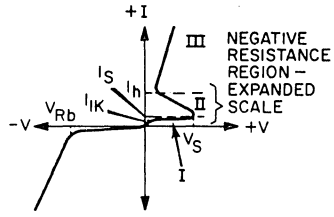
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

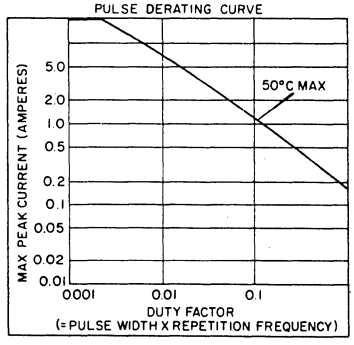


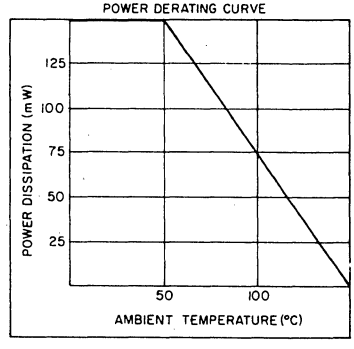
V-I CHARACTERISTICS

TERMS AND SYMBOLS

V_s	Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
I_s	Switching Current—Current which flows through the diode at V_S
I_h	Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
V_h	Holding Voltage—Voltage across the diode at I_h
I_p	Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
R_{on}	ON Resistance—Slope of V-I curve measured at currents > I_h
I_{ik}	Leakage Current—Measured in Region I at 60% V_S
V_{rb}	Reverse Breaker Voltage

DERATING CURVES





4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

ELECTRICAL SPECIFICATIONS

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)	Reverse Breakdown Voltage (Min.)
4E20-8	20±4	1-15	12
4E20-28	20±4	14-45	12
4E30-8	30±4	1-15	18
4E30-28	30±4	14-45	18
4E40-8	40±4	1-15	24
4E40-28	40±4	14-45	24
4E50-8	50±4	1-15	30
4E50-28	50±4	14-45	30
4E80-8	80±8V	1-15	48
4E80-28	80±8V	14-45	48
4E100-8	100±10	1-15	60
4E100-28	100±10	14-45	60
4E200-8	200±20 V	1-15	120
4E200-28	200±20 V	14-45	120
Series A (Broad Spec)			
4E20A	20±6	0.5-60	12
4E30A	30±6	0.5-60	18
4E40A	40±6	0.5-60	24
4E50A	50±6	0.5-60	30
4E80A	80±8	0.5-60	48
4E100A	100±10	0.5-60	60
4E200A	200±20	0.5-60	120

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

Marking:

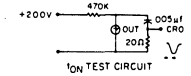
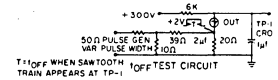
Cathode band
Type number
Manufacturer's Symbol

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −40 to +70°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−40 to +70	°C

TYPE E 4E20-4E200

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	 t_{ON} TEST CIRCUIT
t_{off}		5		μsec	 t_{OFF} WHEN SAWTOOTH TRAIN APPEARS AT TP-1 t_{OFF} TEST CIRCUIT

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

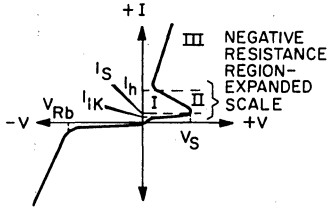
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

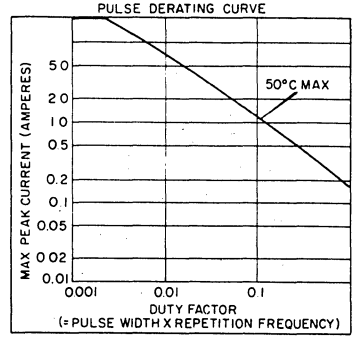


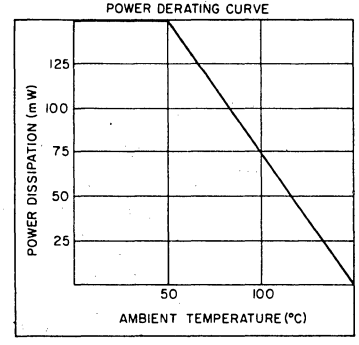
V-I CHARACTERISTICS

TERMS AND SYMBOLS

V_s	Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
I_s	Switching Current—Current which flows through the diode at V_S
I_h	Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
V_h	Holding Voltage—Voltage across the diode at I_h
I_p	Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
R_{on}	ON Resistance—Slope of V-I curve measured at currents > I_h
I_{ik}	Leakage Current—Measured in Region I at 75% V_S
V_{rb}	Reverse Breaker Voltage

DERATING CURVES





4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrices, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

ELECTRICAL SPECIFICATIONS

Mil-Line Series for extended temperature ranges

TYPE	Switching Voltage (V_S)		Holding Current (I_h) (mA) 25°C	Reverse Breakdown Voltage (Min.) −60 to 125°C
	25°C	−60 to 125°C		
4E20M-8	20±4	14-25	1-15	10
4E20M-28	20±4	14-25	14-45	10
4E30M-8	30±4	23-36	1-15	15
4E30M-28	30±4	23-36	14-45	15
4E40M-8	40±4	32-46	1-15	20
4E40M-28	40±4	32-46	14-45	20
4E50M-8	50±4	41-57	1-15	25
4E50M-28	50±4	41-57	14-45	25
4E30M-8	80±8	68-92	1-15	40
4E30M-28	80±8	68-92	14-45	40
4E100M-8	100±10	80-115	1-15	50
4E100M-28	100±10	80-115	14-45	50
4E200M-8	200±20	160-230	1-15	100
4E200M-28	200±20	160-230	14-45	100

MECHANICAL DATA

Case:
Hermetically sealed glass
Finish:
All external surfaces corrosion resistant and leads readily solderable
Leads:
Dumet, tin plated
Weight:
0.135 grams (approx.)
Mounting Position:
Any
Marking:

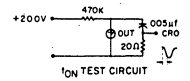
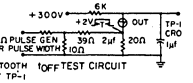
Cathode band
Type number
Manufacturer's Symbol

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

TYPE E 4E20M - 4E200M

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	 t_{ON} TEST CIRCUIT
t_{off}		5		μsec	 t_{OFF} WHEN SAWTOOTH TRAIN APPEARS AT TP-1 t_{OFF} TEST CIRCUIT

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

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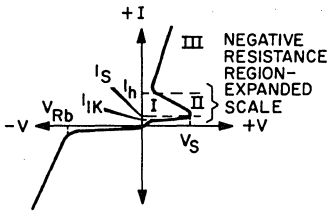
Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

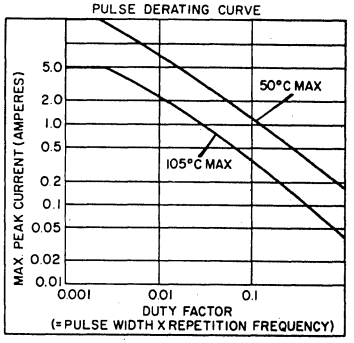


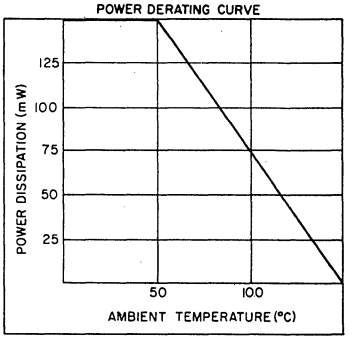
V-I CHARACTERISTICS

TERMS AND SYMBOLS

- V_s Switching Voltage—Closest point to p voltage in Region II where slope of curve is −330Ω. This definition is adopte because of instrumentation requirements
- I_s Switching Current—Current which flows through the diode at V_S
- I_h Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
- V_h Holding Voltage—Voltage across the diode at I_h
- I_p Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
- R_{on} ON Resistance—Slope of V-I curve measured at currents > I_h
- I_{ik} Leakage Current—Measured in Region I at 75% V_S
- V_{rb} Reverse Breaker Voltage

DERATING CURVES





TWENTY-FOUR CIRCUIT APPLICATIONS FOR ITT 4-LAYER DIODES

THEORY OF OPERATION

The ITT Semiconductor Four-Layer Diode is a two-terminal semiconductor switch, sometimes referred to as a negative-resistance diode. These PNPN silicon devices are useful in many applications including pulse generators, oscillators, telephone switching, sweep generators, and multivibrators.

The diode has two stable states; the ON or low impedance state, and the OFF or high impedance state. To turn the device ON, voltage across the terminals must exceed the switching voltage (V_s). The device can be turned OFF by reducing the current through the device below the holding current (I_h).

Figure 1

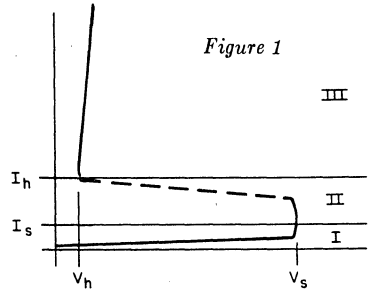


Figure 1 is the V-I characteristic of a typical device. V_s is the point at which the device breaks down and switches to the ON state where current is limited only by the external circuit impedance.

I_h is the minimum current that must be passed through the diode to keep it in the ON state. If the current drops below this value the diode will switch to the OFF state.

Figure 2A

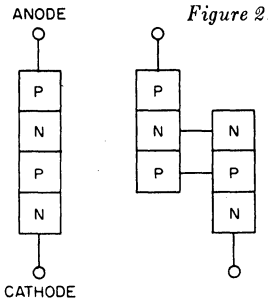
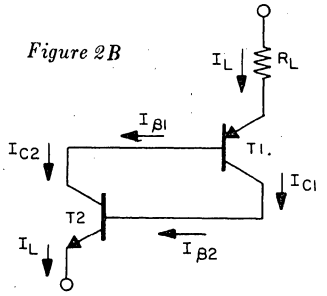


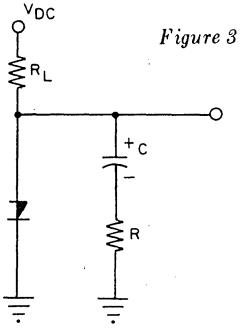
Figure 2B



The PNPN diode can be thought of as a complimentary pair of transistors, one a PNP and the other an NPN as shown in Figure 2A. Figure 2B shows the two transistors as they would appear schematically. The collector of T_2 drives the base of T_1 giving rise to a positive feedback loop with a gain of B_1B_2. As long as B_1B_2 is less than 1 the equivalent circuit is stable with the upper and lower PN junctions biased forward and the middle junction reversed biased. In this condition only a small leakage current flows.

The diode will remain in this condition until either the temperature or the anode voltage is increased to a point where $B_1B_2 = 1$. At this point, the middle junction breaks down and the circuit becomes regenerative. This occurs because the collector of each transistor supplies current to the base of the complimentary transistor in the equivalent circuit and their Betas are current dependent. As soon as they reach unity the device effectively "runs away" or "fires" and the current through the circuit is limited only by external impedance.

Figure 3

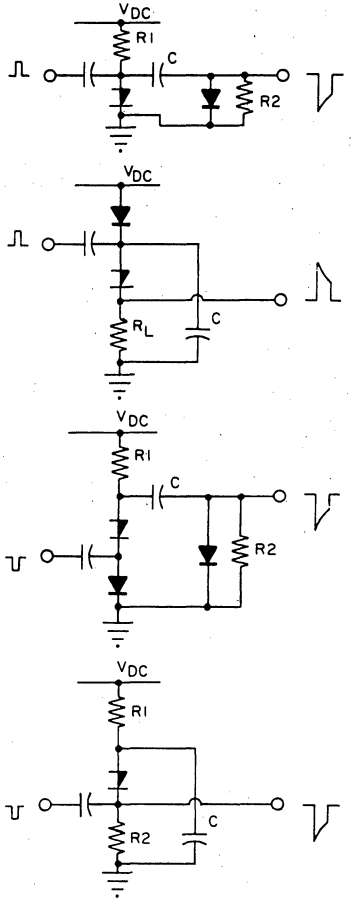


**Application notes will be found in the last pages of this section.

CIRCUITS

Relaxation Oscillator

Figure 3 illustrates a circuit used for oscillator, sweep generator, and timing applications. The output is a saw-tooth voltage the amplitude of which is dependent on the diode V_s. Frequency is dependent upon the $R_L C$ time constant and the supply voltage. The supply voltage should be chosen so that the charging of C is done in the linear portion of the curve. When C reaches V_s the diode breaks down and conducts. C rapidly discharges through the diode. R_L should be large enough so that it will not pass I_h or the diode will remain in the ON condition after C has discharged. With C discharged the diode turns OFF and C commences to charge again. R_L must be able to pass the switching current (I_s) when C reaches V_s and the diode fires again.



Triggered Pulse Generators

These circuits are used mainly for generating or amplifying pulses and for triggering purposes. They are similar to Figure 3 except that the switching voltage of the diode is greater than the supply voltage. Four variations, with their input and output pulses, are shown in Figure 4. A pulse, large enough to break down the diode, is capacitively coupled either positive to the anode or negative to the cathode. The conventional diode is used to present a high impedance to the input pulse.

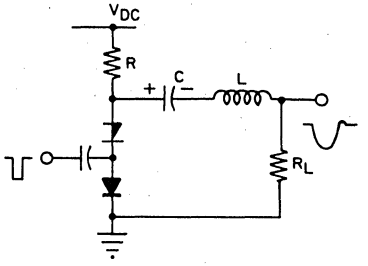
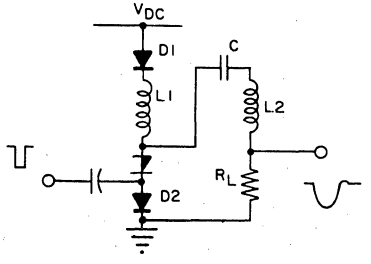


Figure 5

L-C Pulse Generators

As with the circuits in foregoing section, those in this section also require a pulse to fire the diode. V_s of the diode is greater than the supply voltage. In Figure 5, a negative pulse is applied to the cathode which breaks down the diode. C, which was charged to V_{DC} through R, discharges through the diode, L, and R_L. This is a resonant circuit and the wave shape across R_L is a half sinusoid. When the current goes through zero, the voltage across the diode becomes negative, turning it OFF. A small positive output will occur due to the pulse recovery current through the diode.

Figure 6



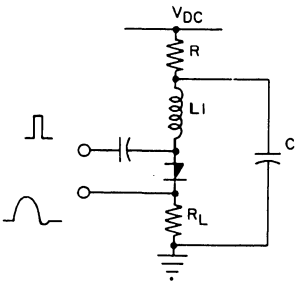


Figure 7

This type of generator does not depend on R being large enough not to pass I_h but rather on the fact that ringing of the L-C loop turns OFF the diode. During the OFF half cycle C charges to V_{DC} but in the opposite polarity. With the completion of the output pulse and the cessation of ringing, C begins to recharge toward the power supply voltage and polarity. Figures 6 and 7 illustrate the same principle but with a resonant charging circuit. C may charge to approximately twice the supply voltage if the circuit Q is high. The resistance of L must be large enough to keep the current through the four-layer diode below its rated maximum. The anode of the diode must be kept negative long enough to turn completely OFF, otherwise the diode will turn back ON when the anode goes positive. This requirement limits the maximum operating repetition rate.

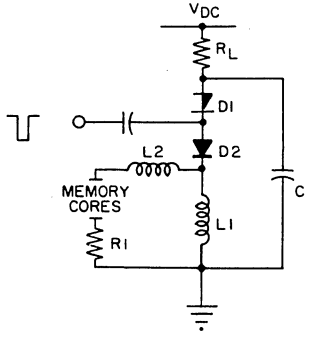


Figure 8

Magnetic Memory Driver Circuits

The purpose of a magnetic memory driving circuit is to provide a current wave form which reads the memory and then restores (writes) the initial flux condition. In Figure 8, the V_s of the four-layer diode is greater than V_{DC}. C charges to V_{DC} through R_L When a negative pulse of the proper magnitude is coupled to the cathode, the four-layer diode (D_1) conducts. R_L is made large enough so that it will not deliver the minimum I_h. C discharges through the four-layer diode (D_1) the conventional diode (D_2), and the inductive load. C must be large enough to supply the "read" peak current. The shape of the curve is dependent on the inductances and R_1. The R_LC product must be selected so that C charges in less time than the time from the end of the "read" pulse to the beginning of the next complete cycle.

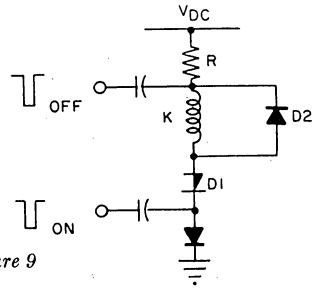


Figure 9

Relay Drivers

In Figure 9, V_s is greater than V_{DC}. A negative pulse on the cathode turns D_1 ON. It remains in this state until it is pulsed OFF by a negative pulse on the anode. This is a typical relay driver application. D_2 prevents excessive spiking caused by the relay inductance.

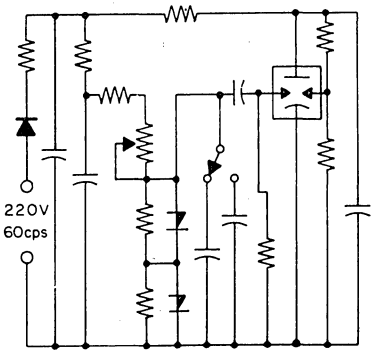


Figure 10

Stroboscope

In Figure 10, the four-layer diodes replace thyratrons as triggers to activate a stroboscope flash tube. The diodes form a relaxation oscillator delivering pulses up to 150V at a few hundred per second depending on the circuit constants. Because of the pulse magnitude two diodes are used in series with equalizing resistors across them.

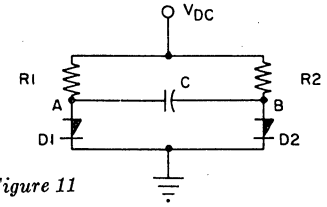


Figure 11

A-Stable Circuit

V_{DC} is greater than V_s of both diodes in Figure 11. When power is applied, one of the diodes will conduct. Let it be assumed that D_1 fires first. Point A will go approximately to ground potential and the current through R_1 will be greater than I_h. The capacitor C will begin to charge through R_2 and D_1 to ground. When the voltage at B exceeds the breakdown potential of D_2, it will conduct and point B will go to ground. Since the capacitor can not charge instantly, point A will drop approximately V_s volts. This puts a negative voltage at A, which if kept there until the turn OFF potential of D_1 is reached, will prevent it from switching back until the voltage at A reaches V_s. C therefore charges through R_1. The circuit oscillates back and forth from D_1 to D_2 with the frequency dependent on R_1C and R_2C and on V_{DC} and the switching voltage of the diodes.

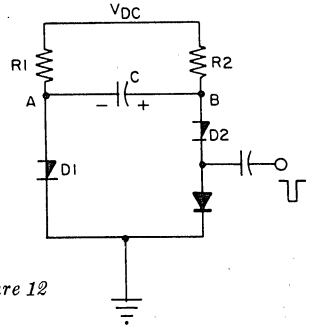


Figure 12

Monostable Multivibrator

If diode D_1 in Figure 12 is selected so that its switching voltage is less than V_{DC}, and diode D_2's is greater than V_{DC}, diode D_1 will normally be in the ON condition and D_2 will be OFF. Capacitor C will charge through R_2. When D_2 is pulsed ON, D_1 will turn OFF due to the commutating action of C. The voltage at point A will then start rising as C charges through R_1 and D_2. When the voltage at point A reaches the switchover voltage of D_1 it will turn ON and D_2 will turn OFF until another pulse is received. Frequency is determined by R_1C, V_{DC}, and V_s of diode D_1.

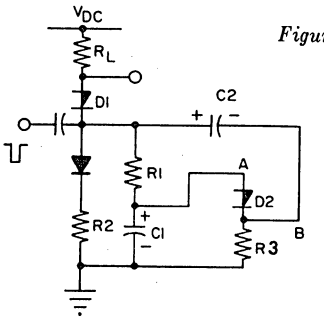


Figure 13

A modification of the gate circuit where both diodes are in the OFF state until a pulse is applied is shown in Figure 13. The V_s of D_1 is slightly higher than V_{DC}. A pulse of current is applied through R_L which turns D_1 ON. C_2 charges through D_1 and R_2 to V_{DC}. C_1 charges through R_1 and D_1 toward V_{DC} also. When the voltage at point A reaches V_s of D_2, it will commence to conduct. The voltage rise at B is commutated back to D_1, turning it OFF, which in turn, turns OFF D_2.

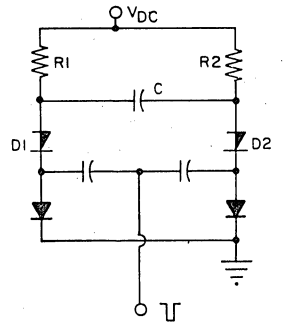


Figure 14

Bi-Stable Multivibrator Flip-Flop

The V_s of both diodes are chosen so that they are greater than V_{DC} in Figure 14. Whichever diode is ON, it remains in that condition until a trigger pulse arrives turning OFF the diode which was ON and turning ON the previously OFF diode by the commutating action of C.

By interchanging one 4-layer diode with its series cathode diode, the circuit will become sensitive to the polarity of the pulses. The circuit will then switchover only when the polarity of the trigger pulse reverses. This is shown in Figure 15. Diode 1 triggers on negative pulses only and diode 2 on positive pulses. Therefore, a positive pulse keeps branch B ON and a negative pulse keeps branch A ON.

Figure 15

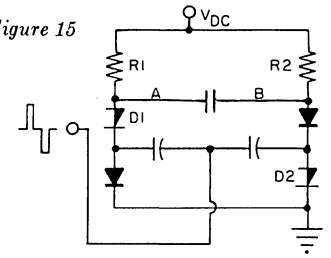
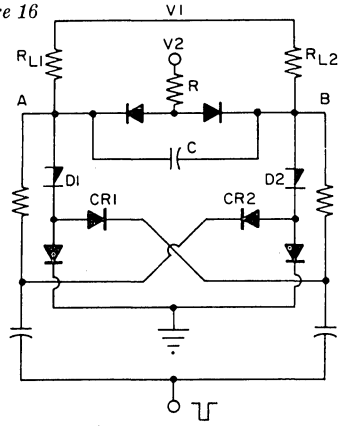
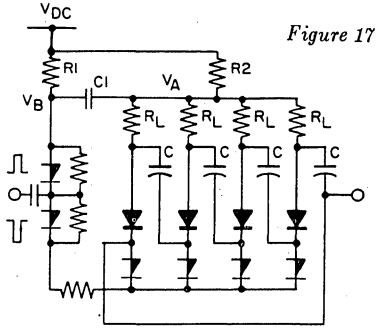


Figure 16



A different steering circuit is shown in Figure 16. Assume that D_1 is ON. Point A will be approximately at ground potential and point B at V_1. When a negative pulse is applied it is blocked by CR_1 but passes through CR_2, causing switchover to take place. Current from V_2 passes through R and D_2 to ground. The principal source of current for the conducting branch is V_2. The R_L's are needed to maintain a voltage of less than V_s across the OFF diode.

Figure 17



Ring Counters

The basic requirement of a ring counter is to turn one stage at a time ON in a simple progression. Each time a trigger pulse is applied, the ON stage will advance one stage. The circuit forms a closed loop, or ring, so that when the final stage has been activated the next pulse will move the ON condition back to the first stage where the cycle begins over again. In Figure 17, one stage will turn ON as soon as power is applied. The commutating capacitor C between the ON stage and the next successive stage charges through R_L and the ON 4-layer diode to V_A, which is less than the V_s of the diodes and keeps them from turning ON. A trigger pulse, either positive or negative, causes V_B to drop almost to ground potential, which in turn, causes V_A to drop at the same time due to the coupling action of C_1. Since R_1 is large enough so that a current of less than I_h flows through the trigger diodes, the pulse is only momentary. The drop in voltage at A turns OFF the ON diode. At the same time C_1 begins to charge and the voltage at A rises again.

The voltage at the high end of the charged commutating capacitor C adds to V_A causing the next stage to fire. The repetition rate of the output pulses equals the rate of the trigger pulses divided by the number of stages.

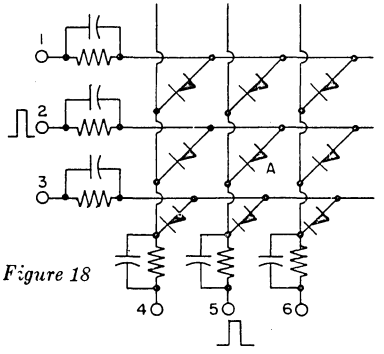


Figure 18

Telephone Switching

When trigger signals of the polarity shown in Figure 18 are simultaneously applied to the lines, one of positive polarity to lines 1, 2, or 3, and the other of negative polarity to lines 4, 5, or 6, two of the lines will be connected. If triggers are applied to lines 2 and 5 as shown, the 4-layer diode A will conduct connecting them together. The series resistors allow a current greater than I_h to flow, thus keeping the diode in the ON state. To open the circuit, a contact is opened to interrupt the flow of current through the diode which will then revert to its OFF condition.

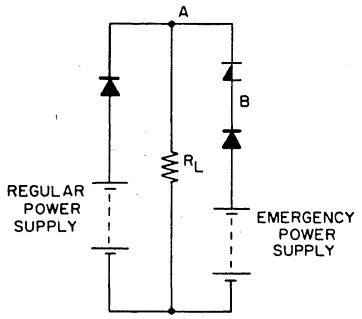


Figure 19

Emergency Power Transfer

In the normal state, the 4-layer diode in Figure 19 is OFF and the regular power supply is the source of power for the load R_L. If the supply voltage should fall off for any reason, the voltage at point A will drop. If this change in voltage is sufficient to cause the potential from B to A to exceed the diode V_s, it will turn ON and the emergency power supply will provide power to the load until the condition is corrected.

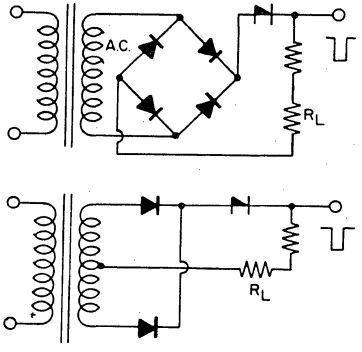


Figure 20

Rectifier Control Circuits

Figure 20 illustrates a method for controlling the power output of a rectifier by varying the point at which a 4-layer diode is triggered. Pulses may be applied at any phase angle from the start of the input waveform (100% power) to 180° (zero power).

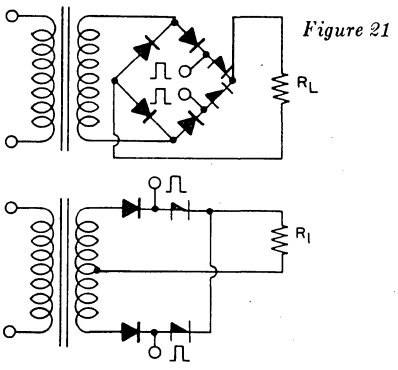


Figure 21

In Figure 21, succeeding half cycles can have different firing angles since there are two control diodes, one for each leg of the rectifier circuit.

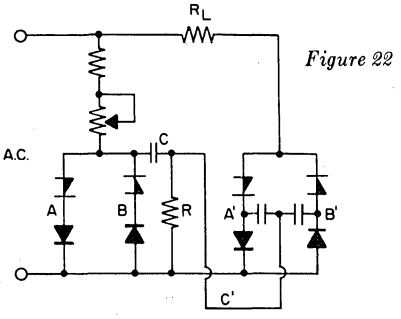


Figure 22

AC Control Circuits

The circuit in Figure 22 is useful for the control of AC power in such applications as light dimmers and motor controls. The trigger portion is composed of two back-to-back relaxation oscillators with an adjustable resistor controlling the time at which they fire the control diodes and thus the amount of current through the load.

The load resistor of the oscillator and C set up the time constant to fire the trigger diodes at approximately 90° in each half cycle. When a positive input cycle occurs the diode A will break down at approximately 90°. The charged capacitor C will discharge through diode A with the result that a negative pulse will appear at point C_1.

This pulse will turn ON control diode A_1 which will allow current to flow until the half cycle is completed. Both diodes will then turn OFF since the current through them will drop below their holding current. This cycle is repeated during the negative portion of the input waveform.

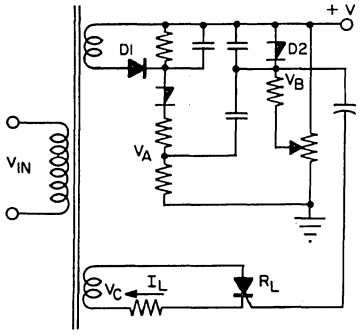


Figure 23

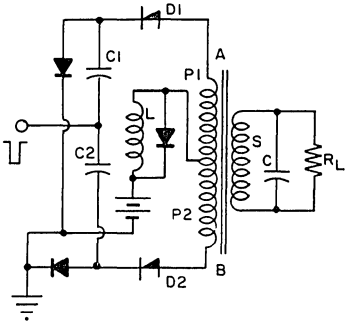


Figure 24

SCR Phasing Circuit

Diode 1 and 2 are both designed into relaxation oscillator circuits in Figure 23. The diode 1 circuit has a frequency of just under 60 cycles per second. The half-wave supply circuit at its anode causes the frequency of the oscillator to be synchronized with the line frequency. The output at V_A is a sawtooth which is coupled to the cathode of D_2. It is superimposed on a DC value set by the potentiometer in the cathode of D_2. As the voltage across D_2 is increased by decreasing the cathode potential, the negative peak of the waveform from D_1 will exceed V_s of D_2 putting it into oscillation at a frequency much greater than that of D_1. This signal is fed to the gate of the SCR which is fired by the steep wave front at the start of oscillations. The timing of the conduction of the SCR is controlled by the setting of the potentiometer.

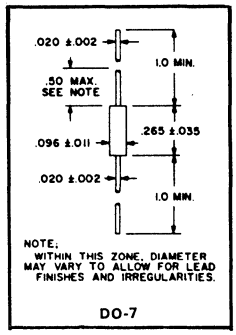
Inverter Circuits

The circuit in Figure 24 is a typical power inverter used to convert DC power to AC power over a range of frequency from 60 to a few thousand cycles. When power is applied, one of the 4-layer diodes begins to conduct. Assume this to be D_1. The battery supplies current through the coil L, primary 1 and D_1. The reflected load limits the current through D_1.

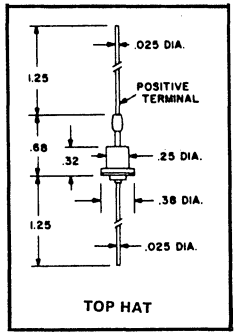
When a negative trigger pulse is applied D_2 will conduct. The commutating capacitor C which is reflected into the primary from across R_L will cause point A to go negative thus turning OFF D_1. L smooths the current during switching. The following negative trigger pulse turns D_1 ON again and C turns D_2 OFF. This completes one cycle.

The switchover voltage of the diodes must be greater than $2XV_{DC}$ and capacitor C must be big enough so that when reflected back into the primary it can turn OFF the diode which was ON just prior to the triggering pulse. The capacitor can be across the primary or the secondary.

THYRISTOR DIODES



DO-7



TOP HAT

DO-7 PACKAGE

TYPE	Switching Voltage (V_S) (Volts) 25°C	−40 to 85°C	Holding Current (I_h) (Milliamps) 25°C	−40°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3831	20 ± 4	14-25	0.5-15	40 max	12v min	80 pf
1N3832	25 ± 4	19-30	0.5-15	40 max	15v min	70 pf
1N3833	30 ± 4	23-36	0.5-15	40 max	18v min	60 pf
1N3834	35 ± 4	28-41	0.5-15	40 max	21v min	50 pf
1N3835	40 ± 4	32-46	0.5-15	40 max	24v min	45 pf
1N3836	45 ± 4	37-51	0.5-15	40 max	27v min	45 pf
1N3837	50 ± 4	41-57	0.5-15	40 max	30v min	40 pf
1N3838	100 ± 10	80-115	0.5-15	40 max	60v min	30 pf

TYPE	Switching Voltage (V_S) (Volts) 25°C	−40 to 58°C	Holding Current (I_h) (Milliamps) 25°C	85°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3839	20 ± 4	14-25	14-50	5 min	12v min	80 pf
1N3840	25 ± 4	19-30	14-50	5 min	15v min	70 pf
1N3841	30 ± 4	23-36	14-50	5 min	18v min	60 pf
1N3842	35 ± 4	24-81	14-50	5 min	21v min	50 pf
1N3843	40 ± 4	32-46	14-50	5 min	24v min	45 pf
1N3844	45 ± 4	37-51	14-50	5 min	27v min	45 pf
1N3845	50 ± 4	41-57	14-50	5 min	30v min	40 pf
1N3846	100 ± 10	80-115	14-50	5 min	60v min	30 pf

Commercial Series

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4E20-8	20 ± 4	1-15
4E20-28	20 ± 4	14-45
4E30-8	30 ± 4	1-15
4E30-28	30 ± 4	14-45
4E40-8	40 ± 4	1-15
4E40-28	40 ± 4	14-45
4E50-8	50 ± 4	1-15
4E50-28	50 ± 4	14-45
4E100-8	100 ± 10	1-15
4E100-28	100 ± 10	14-45
4E200-8	200 ± 20	1-15
4E200-28	200 ± 20	14-15

Mil-Line Series for extended temperature ranges

TYPE	Switching Voltage (V_S) 25°C	−60 to 125°C	Holding Current (I_h) (mA)
4E20M-8	20 ± 4	14-25	1-15
4E20M-28	20 ± 4	14-25	14-45
4E30M-8	30 ± 4	23-36	1-15
4E30M-28	30 ± 4	23-36	14-45
4E40M-8	40 ± 4	32-46	1-15
4E40M-28	40 ± 4	32-46	14-45
4E50M-8	50 ± 4	41-57	1-15
4E50M-28	50 ± 4	41-57	14-45
4E100M-8	100 ± 10	80-115	1-15
4E100M-28	100 ± 10	80-115	14-45
4E200M-8	200 ± 20	160-230	1-15
4E200M-28	200 ± 20	160-230	14-45

Series A (Broad Spec)

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4E20A	20 ± 6	0.5-60
4E30A	30 ± 6	0.5-60
4E40A	40 ± 6	0.5-60
4E50A	50 ± 6	0.5-60

TOP-HAT PACKAGE—TYPE J

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4J50-5	50 ± 5	1-10
4J50-25	50 ± 5	9-45
4J100-5	100 ± 10	1-10
4J100-25	100 ± 10	9-45
4J200-5	200 ± 20	1-10
4J200-25	200 ± 20	9-45

Current Carrying Capacity: 300 mA steady dc.

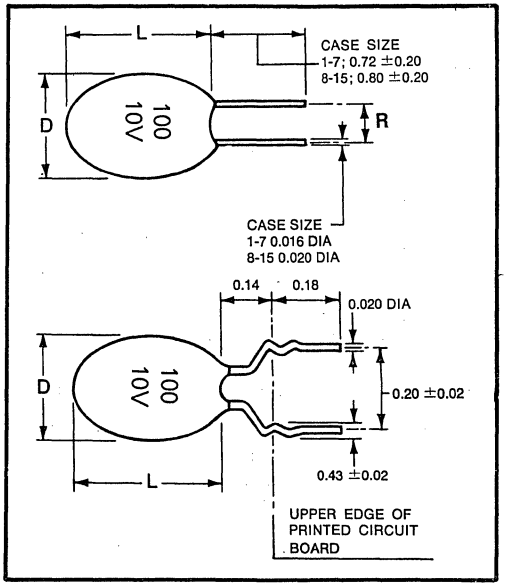
Maximum peak current rating 20 amperes — dependent on duty factor, repetition rate, pulse duration, ambient temperature.

TAG PLASTIC ENCAPSULATED TANTALUM CAPACITORS

- **Extremely low leakage current**
- **Small size — high component density**
- **Reliability — long term stability**
- **Outstanding performance over wide frequency range**
- **Wide temperature range**

The extremely stable oxide layer of TAG capacitors allows only a very small leakage current even after long storage. The solid electrolyte guarantees very stable electrical performance over wide temperature ranges and long time periods.

TAG capacitors are finished in red epoxy and can be mounted in any position. Rugged construction allows installation in moderate environments experiencing moderate shock and vibration.



RATINGS

Capacitance ..... 0.1 to 680μF
Tolerance Range ..... +50 −20%, (±20%)
Voltage ..... 3 to 50 volts
Temperature Range .... Continuous operation between −55°C to +85°C
Leakage Current ..... C×V×0.05 (μA) or 2μA, whichever is greater
Dissipation Factor at 120 Hz and 25°C
up to 100 μF ..... less than 10%
over 150 μF ..... less than 12%
Impedance ..... Nominally less than other electrolytic types, see table

For further requirements see ITT data sheet on TAP CAPACITORS featuring the following ratings:

Tolerance Range ..... ±20% (±10%, ±5%)
Leakage Current ..... C×V×0.02 (μA) or 1 μA, whichever is greater
Dissipation Factor at 120 Hz and 25°C
up to 100 μF ..... less than 6%
over 100 μF ..... less than 8%

TABLE — OUTLINE DIMENSIONS (maximum in inches)

Case Size	Diameter D	Length L	Lead Space R*
1	0.16	0.28	0.11
2	0.18	0.28	0.11
3	0.20	0.31	0.12
4	0.20	0.33	0.12
5	0.22	0.35	0.12
6	0.24	0.37	0.12
7	0.26	0.39	0.14
8	0.33	0.45	0.22
9	0.37	0.53	0.22
10	0.37	0.55	0.22
11	0.39	0.55	0.22
12	0.41	0.59	0.24
13	0.41	0.63	0.24
14	0.43	0.65	0.24
15	0.43	0.67	0.24

*Applies to capacitors w/straight leads only. For TAG/S see drawing.

TYPE TAG
Plastic Encapsulated Tantalum Capacitors

TABLE — STANDARD RATINGS

Capacitance μF	3 Volts			6.3 Volts			10 Volts			16 Volts			20 Volts			25 Volts			35 Volts			50 Volts		
	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.
0.1																			**1**	165	310	1	170	310
0.15																			1	110	200	1	105	180
0.22																			1	75	150	1	80	130
0.33																			1	51	105	2	50	85
0.47																			1	37	68	2	32	60
0.68																			1	27	53	3	25	45
1.0																			1	18	34	4	16	32
1.5																1	12	25	**2**	13	25	5	13	23
2.2										1	10	25				2	9	17	**3**	90	17	6	8	15
3.3							1	8	22	2	6.5	14.5				3	6.5	14.5	**4**	6	12	7	6.2	11
4.7				1	5.6	19	2	5	12	**3**	5	12				4	4.5	10	**5**	4	8	8	3.5	7
6.8	1	5.5	17	2	4	10.5	3	4	10.5	4	3.5	7.5				5	3	6	**6**	3	6	9	2.2	4.5
10.0	1	4.5	15.5	3	3	9.5	**4**	3	9.5	**5**	2.5	6.5				6	2	6.0	**7**	2.5	5.5	11	1.8	3.5
15.0	2	2	8.5	4	2	8.5	5	1.8	5.5	6	1.5	4	**7**	1.5	4	8	1.7	3.5	9	1.2	3			
22.0	3	1.8	7.5	5	1.5	5	6	1	3.5	**7**	1	3.5	8	1	3	9	1.2	2.5	11	1	2.2			
33.0	4	1.2	7	6	0.8	3.5	**7**	0.8	3.5				9	0.8	2.2	10	0.8	2.0	12	0.8	1.7			
47.0	5	0.9	4.2	**7**	0.6	3	8	0.6	2.4	10	0.6	1.9	11	0.7	1.5	12	0.7	1.4	14	0.6	1.2			
68.0	6	0.7	3.5	8	0.5	2.2	9	0.5	1.8	11	0.5	1.3	12	0.6	1.2	13	0.6	1.1						
100.0	**7***	0.5	3	9	0.5	1.7	**11**	0.4	1.2	13	0.4	1	14	0.5	0.9									
150.0	8	0.5	1.8	11	0.4	1.1	13	0.4	0.9	15	0.3	0.8												
220.0	9	0.4	1.1	12	0.4	0.9	14	0.3	0.7															
330.0	11	0.4	0.9	14	0.3	0.7																		
470.0	13	0.3	0.8																					
680.0	14	0.3	0.7																					

*Case sizes in bold type are factory stocked items. Sample quantities are available in most case sizes.

CATALOG ORDERING INFORMATION

(1) **Model No. TAG—F—20—4.7/35—50**

- Tantalum
- Performed Leads
- Lead Spacing .2 in.
- Capacitance 4.7 μF
- 35 Volts
- Tolerance +5 −20%

(2) Optional Features on Special Order
- A. Preformed 0.25" leads, model number code "25." Flexible leads, model number code "00."
- B. Capacitance tolerance of ±20%.
- C. Numerical Stamping.

(3) Minimum Packaging Quantity — 100 units.

Environment & Mechanical Properties

HUMIDITY—Capacitors are tested after exposure to a maximum humidity of 95% at 40°C for 21 days with no voltage applied.

LEAD STRENGTH—Leads are capable of withstanding a pull of 1 pound for 10 seconds and can tolerate two 90 degree bends without failure.

MOUNTING & SOLDERING—TAG capacitors can be dip-soldered with a maximum bath temperature of 270°C. Acid flux is not suitable and can damage the units. Soldering time should not exceed 3 seconds and the cases of the units should not be dipped to closer than ⅛" of the bath surface.

When bending leads, no stress should be applied to the case. Avoid mounting adjacent to heat radiating components.

Definitions and Ratings

RATED CAPACITANCE — Value measured at 60 cycles and +25°C.

CAPACITANCE TOLERANCE — Variation of actual value from nominal rated value in per cent (%).

RATED DC VOLTAGE — Listed rating in volts DC at a surface temperature of +40°C.

CONTINUOUS MAXIMUM VOLTAGE—Highest DC voltage which can be applied to capacitor. Max voltage equals rated voltage up to +85°C ambient temperature.

SURGE VOLTAGE—Maximum voltage to which capacitor may be subjected 5 times per hour for one minute. Maximum value is 1.15 times the rated voltage. Capacitors should not be used in electrical circuits where the capacitor is regularly charged and discharged to the peak of the surge voltage.

REVERSE VOLTAGE—Not to exceed 0.5 Reverse voltage higher than this limit can be handled by connecting 2 capacitors in anti-series (bipolar capacitor). Resulting capacitors will be of same voltage, but half capacity of single unit.

AC RIPPLE VOLTAGE—Sum of superimposed peak AC voltage and DC voltage must not exceed rated voltage. See figures 3, 6 and 9.

LEAKAGE CURRENT — Current measured through a 1,000Ω resistor with rated voltage applied for 3 minutes at +25°C. This current does not exceed 0.05 times capacitance (μF) times rated voltage (volts), or 2 μA, whichever is greater. At +85°C, typical leakage current is less than 10 times the value at +25°C. See figure 4.

IMPEDANCE—Measured at 10KHz and 25°C. See figure 8.

DISSIPATION FACTOR—(tangent of loss angle:, $\tan\vartheta$) defined by $\tan\vartheta = 2\pi fRC$, is measured at a frequency of 120 Hz, at room temperature, 25°C.

Variation of $\tan\vartheta$ with temperature is shown in figure 10.

Protective Circuit Resistance

The failure rate of TAG capacitors will be $\lambda = 4{,}2 \times 16_{-6}\, h_{-1}$ at 3 Ohm/voltage circuit resistance 85°C and rated voltage

Any lower resistance will increase the failure rate.

This can be compensated by voltage derating. See figures 12, 13, and 14.

Operational Reliability

The reliability is measured by the reject rate,

$$F_R = \frac{m}{n \times h}$$

where m = number of rejects. n × h = components × hours.

The reject rate increases with applied voltage V_B and ambient temperature and falls with increased circuit resistance R_s. As a result of comprehensive life-tests the reject rate has been determined as a function of V_B, and R_s. The reject rate for catastrophic failures for the particular case can be determined from Fig. 12 to 14 as follows:

1. Determine the reject rate of F_R'' as a function of the applied voltage from Fig. 12 with = +85°C and Rs = 3Ω/V.

2. Multiply F_R'' with the corresponding factor from Fig. 13 for the actual ambient temperature to obtain the reject rate F_R'.

3. Determine the final reject rate F_R as a function of the circuit resistance by multiplying F_R' with the corresponding correction factor obtained from Fig. 13 (ambient temperature as parameter).

EXAMPLE: Determination of F for

$V_B = 50\%$ $F_R'' = 2.8 \cdot 10^{-7} \cdot h^{-1}$ (from Fig. 12)

$\vartheta_U = 125°C$ $F_R' = 2.8 \cdot 10^{-7} \cdot 9 \cdot h^{-1}$ (from Fig. 13)

$R_S = 1\Omega/V$ $F_B'' = 2.8 \cdot 10^{-7} \cdot 9 \cdot 2.8 \cdot h^{-1}$ (from Fig. 14)

$F_R = 7.06 \times 10^{-6} h^{-1}$

TYPE TAG
Plastic Encapsulated Tantalum Capacitors

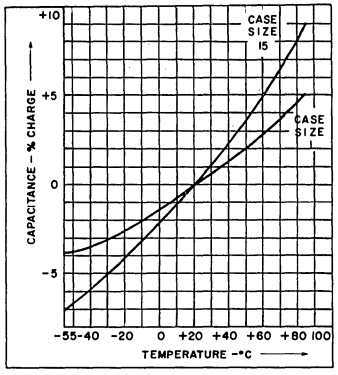
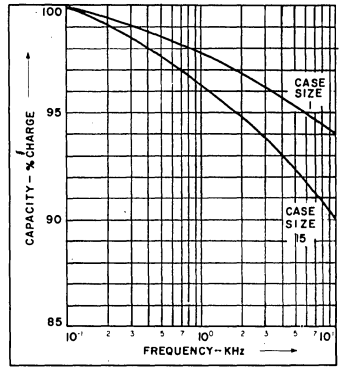


Figure 1



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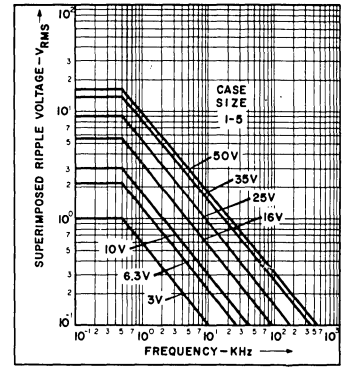

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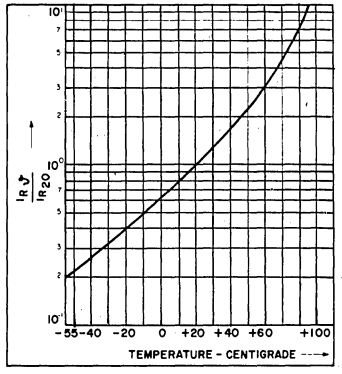
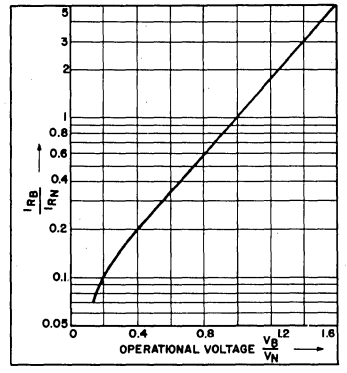


Figure 4



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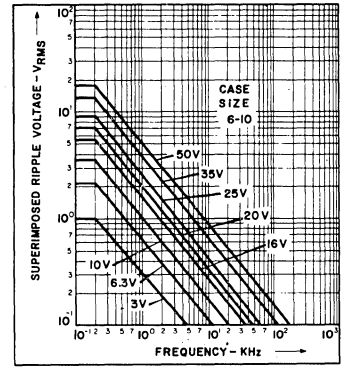

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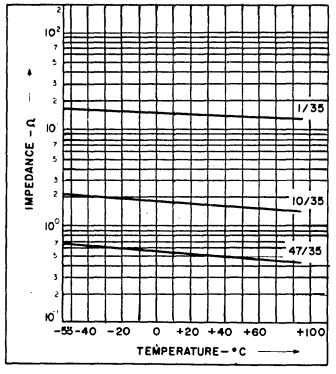

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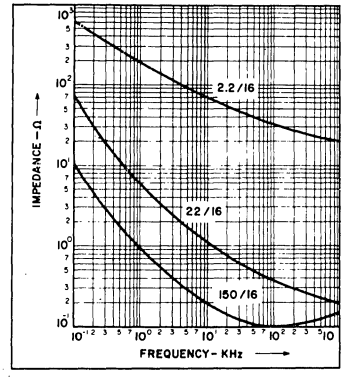


Figure 8

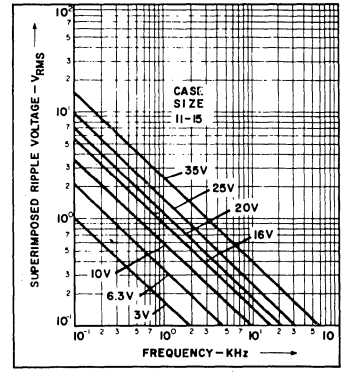


Figure 9

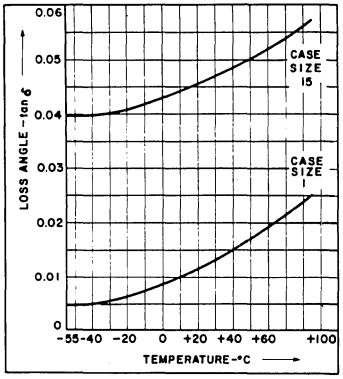


Figure 10

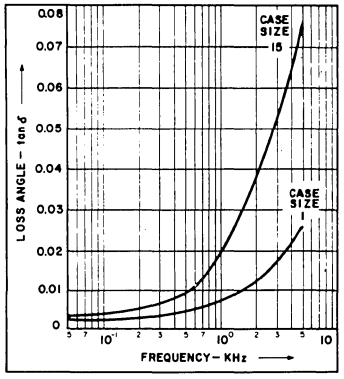


Figure 11

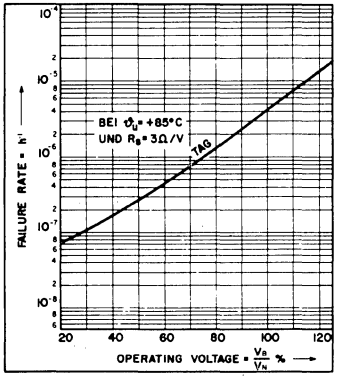


Fig. 12 Reject Rate vs Applied Voltage

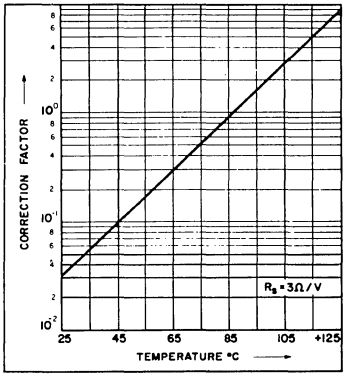


Fig. 13 vs Ambient Temperature

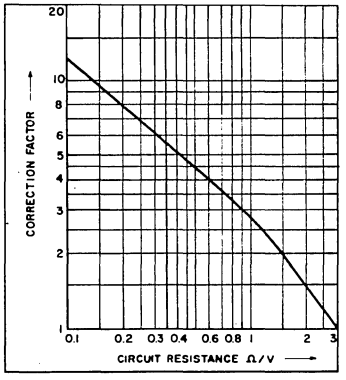


Fig. 14 vs Circuit Resistance

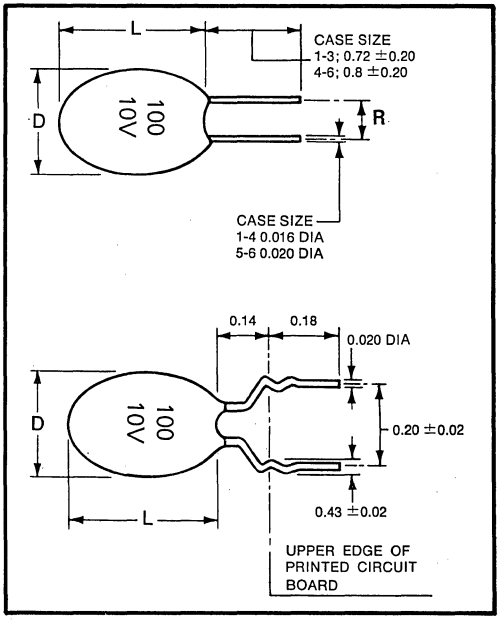
ITT SEMICONDUCTORS

TAP PLASTIC ENCAPSULATED TANTALUM CAPACITORS

- **Extremely low leakage current**
- **Small size — high component density**
- **Reliability — long term stability**
- **Outstanding performance over wide frequency range**
- **Wide temperature range**

The extremely stable oxide layer of TAP capacitors allows only a very small leakage current even after long storage. The solid electrolyte guarantees very stable electrical performance over wide temperature ranges and long time periods.

TAP capacitors are finished in red epoxy and can be mounted in any position. Rugged construction allows installation in moderate environments experiencing moderate shock and vibration.



CATALOG ORDERING INFORMATION

(1) **Model No. TAP—F—20—4.7/35—20**

- Tantalum
- Preformed Leads
- Lead Spacing .2 in.
- Capacitance 4.7 μF
- 35 Volts
- Tolerance ±20%

(2) Optional Features on Special Order

A. Preformed 0.25" leads, model number code "25."

B. Capacitance tolerance of ±10% or ±5%.

(3) Minimum Packaging Quantity — 100 units.

TABLE — OUTLINE DIMENSIONS
(maximum in inches)

Case Size	Diameter D	Length L	Lead Space R*
1	0.18	0.28	0.10
2	0.20	0.30	0.10
3	0.26	0.36	0.10
4	0.34	0.40	0.10
5	0.40	0.56	0.20
6	0.44	0.68	0.20

*Applies to capacitors w/straight leads only. For TAG/S see drawing.

TYPE TAP
PLASTIC ENCAPSULATED TANTALUM CAPACITORS MINIATURE TYPE SOLID-ELECTROLYTE

TABLE — STANDARD RATINGS

Capacitance μF	3 Volts			6.3 Volts			10 Volts			16 Volts			25 Volts			35 Volts			50 Volts		
	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.	Case Size	Nom. Imp.	Max. Imp.
0.1																1	165	170	1	170	270
0.15																1	110	180	1	105	280
0.22																1	75	130	1	80	130
0.33																1	51	85	1	50	85
0.47																1	37	58	2	32	55
0.68																1	27	40	2	25	38
1.0													1	19	30	2	18	28	3	16	26
1.5										1	12	25				2	13	20	3	13	18
2.2							1	10	22				2	9	15	3	90	13	4	8	12
3.3				1	8	20				2	6.5	13.5				3	6	10	4	6.2	9
4.7	1	6	18				2	5	12				3	4.5	7.5	4	4	7	5	3.5	6.5
6.8	1	5.5	16	2	4	10							3	3	5.5	4	3	4.5	6	2.2	4.2
10.0	2	4.5	12.5							3	2.5	5.0				4	2.5	3.2	6	1.8	3.0
15.0	2	2	8.5				3	1.8	4.5				4	1.7	2.8	5	1.2	2.5			
22.0				3	1.5	4.0				4	1	2.5				5	1	2.0			
33.0	3	1.2	5.5				4	0.8	2.2				5	0.8	1.8	6	0.8	1.6			
47.0	3	0.9	3.6	4	0.6	2.0				5	0.6	1.5				6	0.6	1.2			
68.0	4	0.7	2.5							5	0.5	1.1	6	0.6	1.0						
100.0	4	0.5	2.0				5	0.4	1.0	6	0.4	0.9									
150.0				5	0.4	0.9				6	0.3	0.8									
220.0	5	0.4	0.9				6	0.3	0.8												
330.0	5	0.4	0.8	6	0.3	0.7															
470.0	6	0.3	0.7																		
680.0	6	0.3	0.6																		

NOTE: Sample quantities are available in most case sizes.

RATINGS

Capacitance ..... 0.1 to 680 μF
Tolerance Range .... +20% (±10%, ±5%)
Voltage ..... 3 to 50 volts
Temperature Range .... Continuous operation between −55°C to +85°C
Leakage Current ..... C×V×0.02 (μA) or 1 μA, whichever is greater
Dissipation Factor ..... at 120 Hz and 25°C
up to 100 μF less than 6%
over 100 μF less than 8%
Impedance ..... Nominally less than other electrolytic types, see table

For standard requirements see ITT data sheet on TAG CAPACITORS featuring the following ratings:

Tolerance Range ..... +50 −20% (±20%)
Leakage Current ..... C×V×0.05 (μA) or 2 μA, whichever is greater
Dissipation Factor ..... at 120 Hz and 25°C
up to 150 μF less than 10%
over 150 μF less than 12%

Environment & Mechanical Properties

HUMIDITY—Capacitors are tested after exposure to a maximum humidity of 95% at 40°C for 21 days with no voltage applied.

LEAD STRENGTH—Leads are capable of withstanding a pull of 1 pound for 10 seconds and can tolerate two 90 degree bends without failure.

MOUNTING & SOLDERING—TAG capacitors can be dip-soldered with a maximum bath temperature of 270°C. Acid flux is not suitable and can damage the units. Soldering time should not exceed 3 seconds and the cases of the units should not be dipped to closer than ⅛" of the bath surface.

When bending leads, no stress should be applied to the case. Avoid mounting adjacent to heat radiating components.

TYPE TAP
PLASTIC ENCAPSULATED TANTALUM CAPACITORS MINIATURE TYPE SOLID-ELECTROLYTE

Definitions and Ratings

RATED CAPACITANCE — Value measured at 60 cycles and +25°C.

CAPACITANCE TOLERANCE — Variation of actual value from nominal rated value in per cent (%).

RATED DC VOLTAGE — Listed rating in volts DC at a surface temperature of +40°C.

CONTINUOUS MAXIMUM VOLTAGE—Highest DC voltage which can be applied to capacitor. Max voltage equals rated voltage up to +85°C ambient temperature.

SURGE VOLTAGE—Maximum voltage to which capacitor may be subjected 5 times per hour for one minute. Maximum value is 1.15 times the rated voltage. Capacitors should not be used in electrical circuits where the capacitor is regularly charged and discharged to the peak of the surge voltage.

REVERSE VOLTAGE—Not to exceed 0.5 Reverse voltage higher than this limit can be handled by connecting 2 capacitors in anti-series (bipolar capacitor). Resulting capacitors will be of same voltage, but half capacity of single unit.

AC RIPPLE VOLTAGE—Sum of superimposed peak AC voltage and DC voltage must not exceed rated voltage. See figures 3, 6 and 9.

LEAKAGE CURRENT — Current measured through a 1,000Ω resistor with rated voltage applied for 3 minutes at +25°C. This current does not exceed 0.02 times capacitance (μF) times rated voltage (volts), or 1 μA, whichever is greater. At +85°C, typical leakage current is less than 10 times the value at +25°C. See figure 4.

IMPEDANCE—Measured at 10KHz and 25°C. See figure 8.

DISSIPATION FACTOR—(tangent of loss angle:, tan ϑ) defined by tan $\vartheta = 2\pi fRC$, is measured at a frequency of 120 Hz, at room temperature, 25°C.

Variation of tan ϑ with temperature is shown in figure 10.

Protective Circuit Resistance

The failure rate of TAP capacitors will be

$\lambda = 1 \times 10_{-6}\ h_{-1}$

at 3 Ohm/voltage circuit resistance
85°C and rated voltage

Any lower resistance will increase the failure rate.

This can be compensated by voltage derating. See figures 12, 13, and 14.

CHARACTERISTIC CURVES

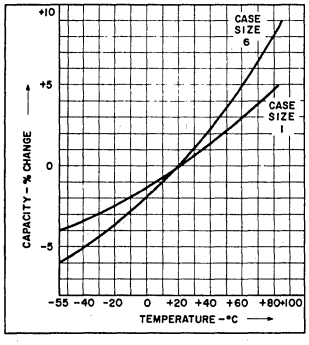


Figure 1

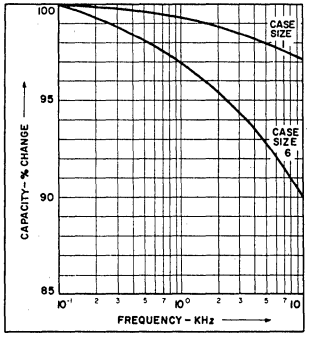


Figure 2

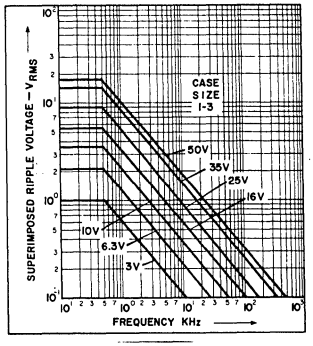


Figure 3

TYPE TAP
PLASTIC ENCAPSULATED TANTALUM CAPACITORS MINIATURE TYPE SOLID-ELECTROLYTE

CHARACTERISTIC CURVES (continued)

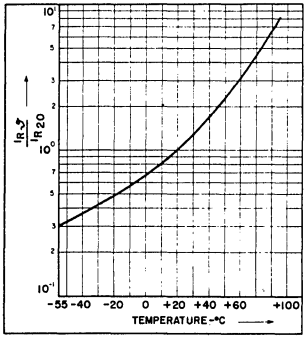


Figure 4

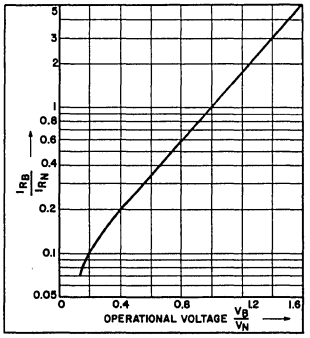


Figure 5

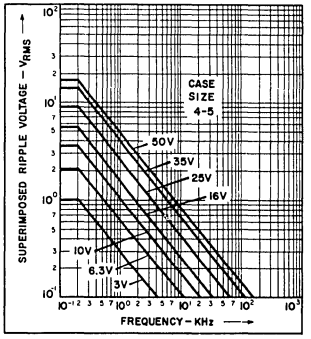


Figure 6

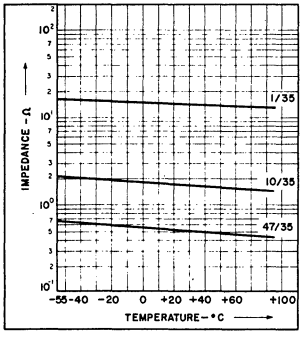


Figure 7

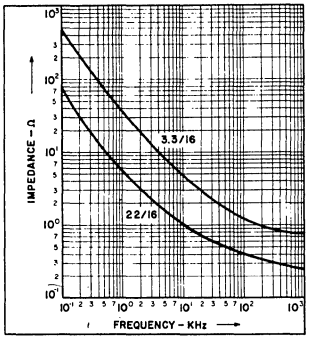


Figure 8

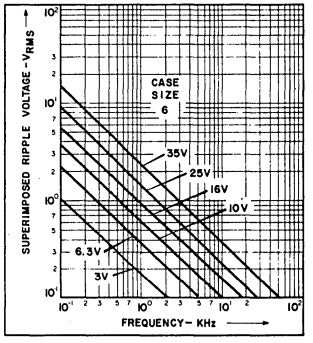


Figure 9

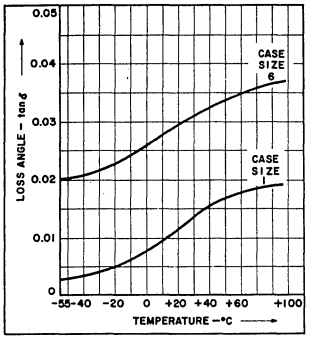


Figure 10

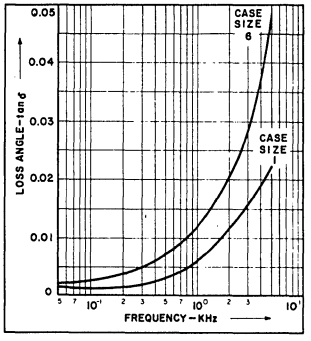


Figure 11

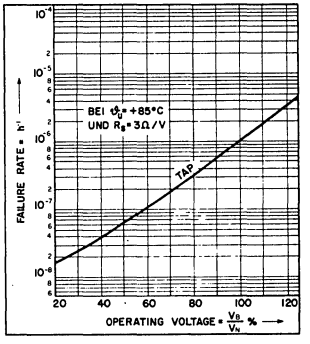


Fig. 12 Reject Rate vs Applied Voltage

CHARACTERISTIC CURVES (continued)

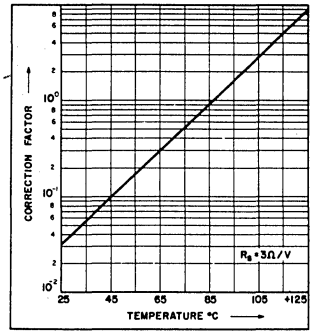


Fig. 13 vs Ambient Temperature

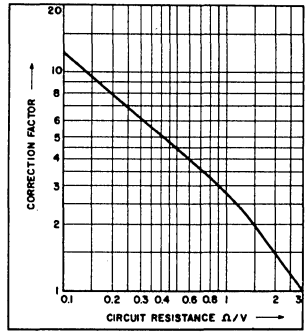


Fig. 14 vs Circuit Resistance

Operational Reliability

The reliability is measured by the reject rate,

$$F_R = \frac{m}{n \times h}$$

where m = number of rejects. n × h = components × hours.

The reject rate increases with applied voltage V_B and ambient temperature ϑ_U, and falls with increased circuit resistance R_s. As a result of comprehensive life-tests the reject rate has been determined as a function of V_B, ϑ_U and R_s. The reject rate for catastrophic failures for the particular case can be determined from Fig. 12 to 14 as follows:

1. Determine the reject rate of F_R'' as a function of the applied voltage from Fig. 12 with $\vartheta_U = +85°C$ and Rs = 3Ω/V.

2. Multiply F_R'' with the corresponding factor from Fig. 13 for the actual ambient temperature to obtain the reject rate F_R'.

3. Determine the final reject rate F_R as a function of the circuit resistance by multiplying F_R' with the corresponding correction factor obtained from Fig. 13 (ambient temperature as parameter).

EXAMPLE: Determination of F for

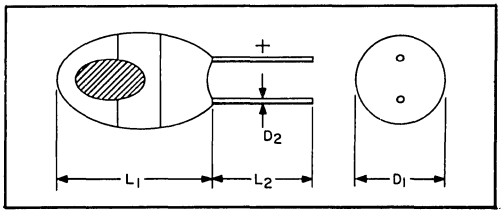
$V_B = 50\%$ $\quad F_R'' = 6.2 \cdot 10^{-8} \cdot h^{-1}$ (from Fig. 12)

$\vartheta_U = 125°C$ $\quad F_R' = 6.2 \cdot 10^{-8} \cdot 9 \cdot h^{-1}$ (from Fig. 13)

$R_S = 1\Omega/V$ $\quad F_R' = 6.2 \cdot 10^{-8} \cdot 9 \cdot 2.8 \cdot h^{-1}$ (from Fig. 14)

$F_R = 7.56 \times 70^{-6} \cdot h^{-1}$

TAM PLASTIC ENCAPSULATED TANTALUM CAPACITORS



- **Sub-Miniature size—high component density**

RATINGS

Capacitance ..... 0.015μF to 6.8μF
Tolerance Range ..... ±20%
Voltage ..... 3 to 35 volts
Temperature Range ... Continuous operation between −55°C to +85°C
Leakage Current ..... 1μA, Max.
Dissipation Factor ..... at 120 Hz and 25°C 10% Max.
Impedance ..... Nominally less than other electrolytic types

The extremely stable oxide layer of TAM capacitors allows only a very small leakage current even after long storage. The solid electrolyte guarantees very stable electrical performance over wide temperature ranges and long time periods.

TAM capacitors are finished in epoxy and can be mounted in any position. Rugged construction allows installation in moderate environments experiencing moderate shock and vibration.

Fixed Capacitor.
Tantalum Electrolytic.
Solid Electrolyte: Porous Anode: Polar: Resin Dipped:
Radial Terminations.
General Application.

TYPE TAM
CATALOG ORDERING INFORMATION

(1) **Model No. TAM — — — 4.7/35 — 20**

- Tantalum
- Capacitance 4.7 μF
- 35 Volts
- Tolerance ±20%

1. Manufacturing dimensions are in millimetres.
2. Length of terminations (L_2) 15mm (0.6in.) minimum.
3. Marking for polarity shall be indicated, as shown, by the position of the coloured spot relative to the positive terminal.
4. The complete capacitance/rated voltage range is given in Table 1.
5. The tolerance on the wire diameter is + 10% −0.05mm (0.002in.).
6. The maximum length of resin along the terminal wires is 1.5mm (0.055in.) and is contained within the maximum body length L_1.

Table — Outline Dimensions

Case Size	L_1 mm	Max. in.	D_1 mm	Max. in.	D^2 mm	Nom. in.	Capacitance Range and Rated Voltage Range	Typical Weight (g)
X	4.5	0.18	2.5	0.10	0.35	0.014	3.3μF 3V to 0.015μF 35V	0.064
Y	5.0	0.20	2.5	0.10	0.35	0.014	6.8μF 3V to 0.68μF 35V	0.073

These conditions apply at all temperatures up to 85°C. Ripple voltage ratings at higher frequencies are obtained by multiplying the above 100 Hz values by the following factors:—

Frequency	Factor
1 kHz	0.5
10 kHz	0.1
100 kHz	0.02

TYPICAL PERFORMANCE

Fig. 1—Variation of Capacitance with temperature (referred to 20°C)

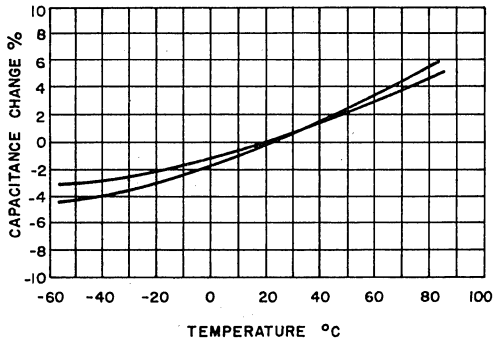


Fig. 2—Variation of Power Factor with temperature (measured at 120 Hz with maximum working voltage applied).

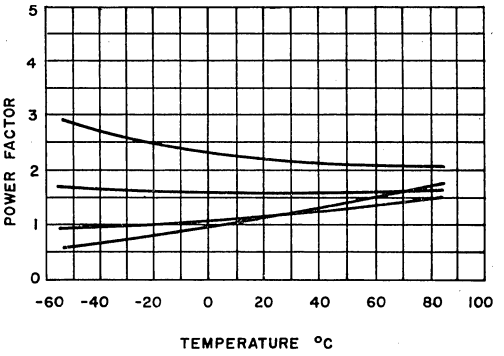


Fig. 3—Variation of leakage current with temperature (measured at maximum working voltage after 3 minutes).

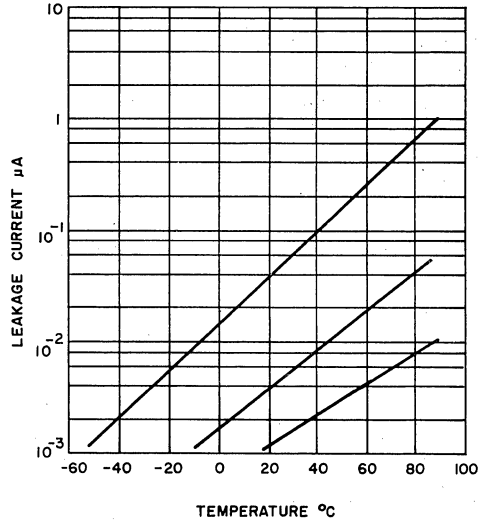
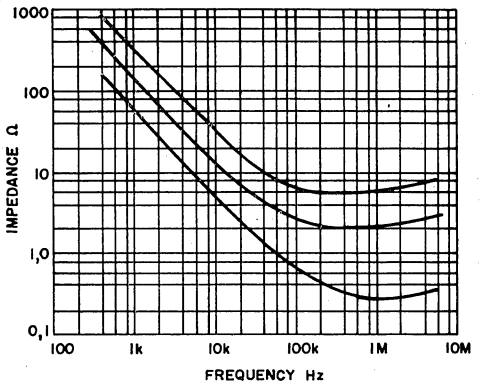


Fig. 4—Variation of Impedance with Frequency.



APPLICATION NOTES

These capacitors are suitable for coupling and decoupling and general applications in electronic circuits. The reliability of these capacitors depends on circuit impedance. In very low impedance (a.g. less than 3Ω/V) circuits, such as power supplies, particular care is necessary to ensure that the surge voltage rating is not exceeded. The main mode of failure is high leakage current or short circuit.

TYPE TAM
Plastic Encapsulated Tantalum Capacitors

TABLE STANDARD RATINGS
(letter denotes Case Size Code)

Capacitance μF	Case Size 3V	6.3V	10V	16V	25V	35V
0.015						X
0.022						X
0.033						X
0.047						X
0.068						X
0.10						X
0.15						X
0.22						X
0.33						X
0.47					X	
0.68				X		Y
1.0			X		Y	
1.5		X		Y		
2.2	X		Y			
3.3	X	Y				
4.7	Y					
6.8	Y					

Definitions and Ratings

Working Voltage	3	6.3	10	16	25	35V d.c.
Surge Voltage	3.5	7	12	13	30	40V d.c.
Maximum Reverse Voltage	0.3	0.5	0.5	0.5	0.5	0.5V d.c.

AC RIPPLE VOLTAGE—Table 2 gives the maximum r.m.s. ripple voltage which may be applied at 100 Hz. The sum of the D.C. voltage and the peak value of the superimposed alternating voltage must not exceed the normal rated voltage and no inadmissible reverse polarity must occur.

LEAKAGE CURRENT—Maximum Leakage Current $I_{\mu F}$ (after 3 minutes at rated voltage with 1,000 Ω series resistance).

IMPEDANCE—Measured at 10 KHz and 25°C.

DISSIPATION FACTOR—(tangent of loss angle:, tan defined by tan = 2−fRC, is measured at a frequency of 120 Hz at room temperature, 25°C. Dissipation Factor is 10% Max.

Variation of tan with temperature is shown in Figure 2.

Environment & Mechanical Properties

HUMIDITY — Capacitors are tested after exposure to a maximum humidity of 95% at 40°C for 21 days with no voltage applied.

LEAD STRENGTH—Leads are capable of withstanding a pull of .12 oz for 10 seconds and can tolerate three 90 degree bends without failure.

MOUNTING & SOLDERING—TAM capacitors can be dip-soldered with a maximum bath temperature of 270°C. Acid flux is not suitable and can damage the units. Soldering time should not exceed 3 seconds and the cases of the units should not be dipped to closer than ⅛" of the bath surface.

When bending leads, no stress should be applied to the case. Avoid mounting adjacent to heat radiating components.

Protective Circuit Resistance

The failure rate of TAM capacitors will be $\lambda = 4.2 \times 16_{-6}\ h_{-1}$ at 3 Ohm/voltage circuit resistance 85°C and rated voltage

Any lower resistance will increase the failure rate. This can be compensated by voltage derating.

Table 2—Ripple Voltage Ratings (r.m.s.)

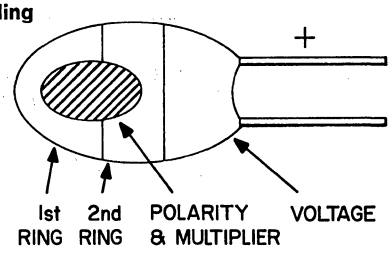
Capacitance μF	Rated Voltage D.G. 3	6.3	10	16	25	35
0.015						10
0.022						10
0.033						10
0.047						10
0.068						10
0.10						10
0.15						10
0.22						10
0.33						10
0.47					7.1	
0.68				4.3		10
1.0			2.8		5.7	
1.5		1.7		4.3		
2.2	0.9		2.8			
3.3	0.9	1.7				
4.7	0.9					
6.8	0.9					

TYPE TAM
Plastic Encapsulated Tantalum Capacitors

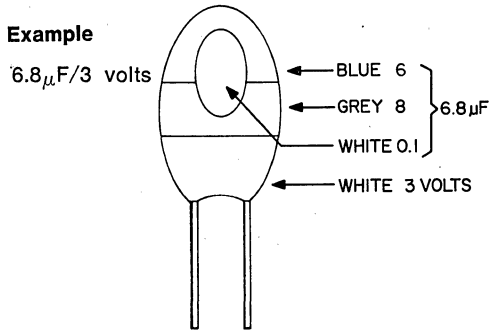
Capacitance in μF				D.C. Working	
Colour	1st Ring	2nd Ring	Polarity & Multiplier	Voltage Colour	Volts
Black	-	0		White	3
Brown	1	1		Yellow	6.3
Red	2	2		Black	10
Orange	3	3		Green	16
Yellow	4	4		Grey	25
Green	5	5		Pink	35
Blue	6	6			
Violet	7	7	$\times$0.001		
Grey	8	8	$\times$0.01		
White	9	9	$\times$0.1		

N.B.—The above sketch shows the position of the coloured spot which serves both as multiplier and anode indicator.

Coding



Example



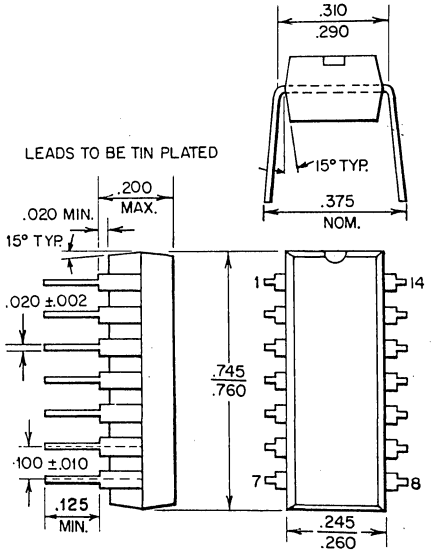
ORDERING CODE FOR 930 DTL, 9000 TTL, 9300 TTL, 950 CTL AND LINEAR CIRCUITS

Operating Temperature Range (add)
—1 for —55 to +125°C
—5 for 0 to +70°C
+75°C for digital

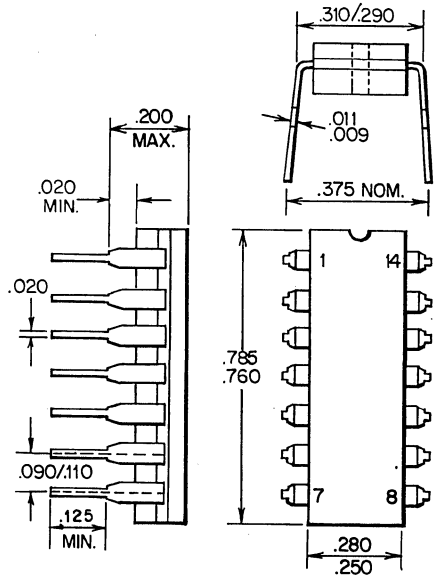
Package (add)
B for Flat Pack
C for TO-5 Style
D for Ceramic Dual In-Line
P for Plastic Dual In-Line

Example:
ITT709A-1D
is —55 to +125°C
Range in Dual In-Line Package

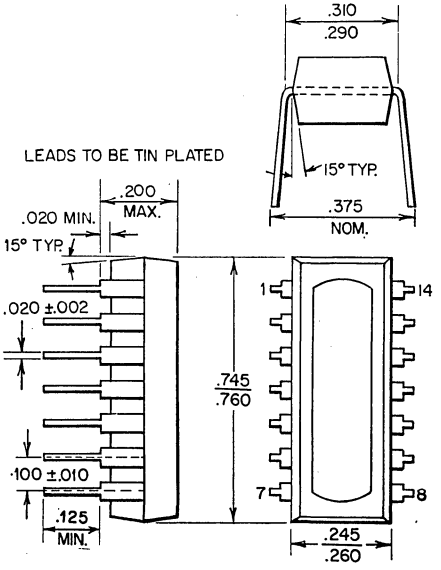
Dual In-Line Plastic Package TO-116



14-Lead Ceramic Dual-In-Line

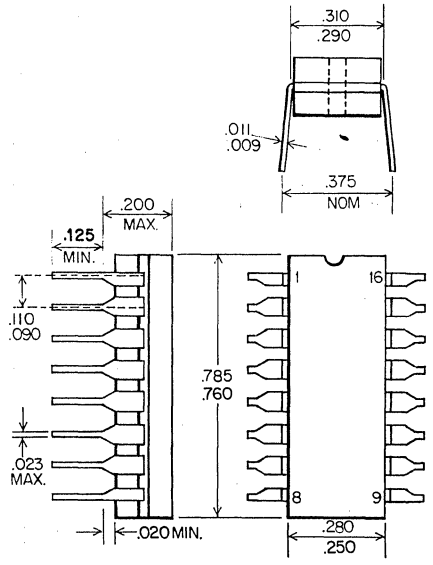


14-Lead Plastic Power Dual-In-Line



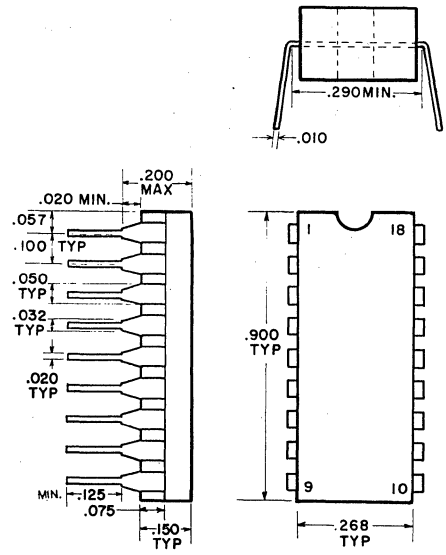
PACKAGE DIMENSIONS

16-Lead Ceramic Dual-In-Line

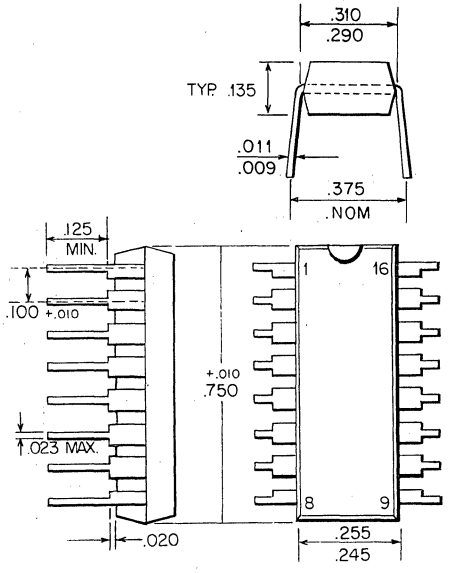


NOTES: All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.

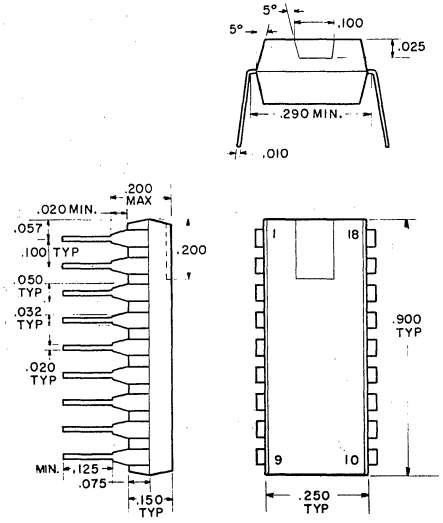
18-Lead Ceramic Dual-In-Line



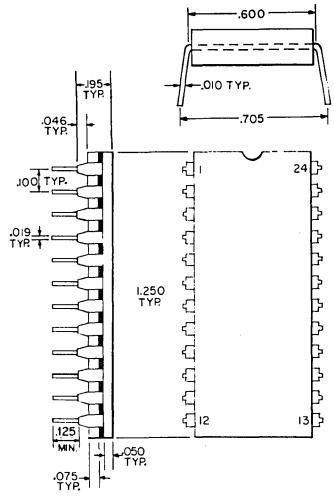
16-Lead Plastic Dual-In-Line



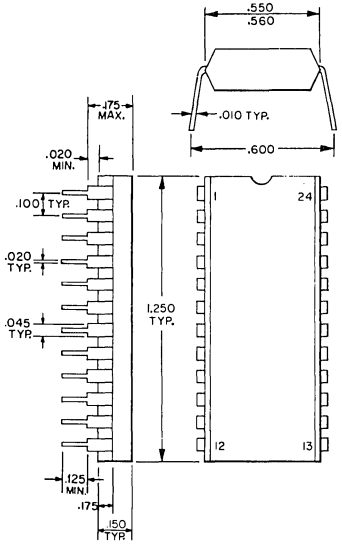
18-Lead Plastic Dual-In-Line



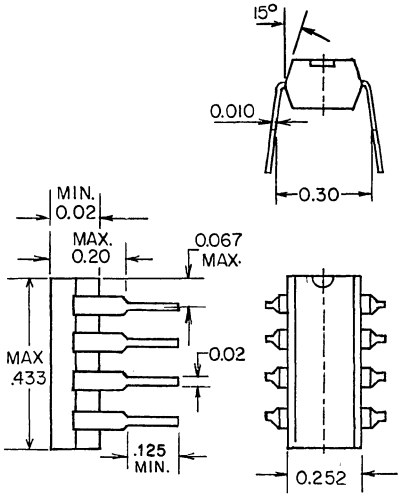
24-Lead Ceramic Dual-In-Line



24-Lead Plastic Dual-In-Line



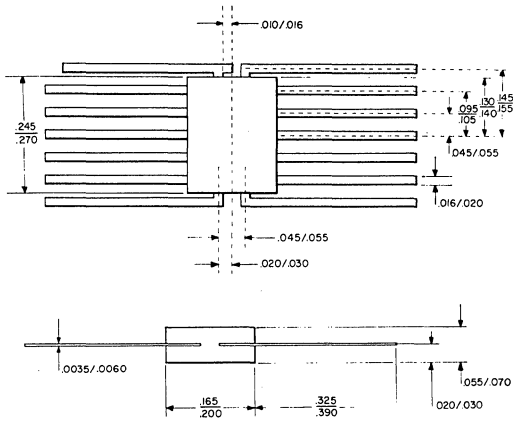
Mini DIP 8-Lead Plastic Package



PACKAGE DIMENSIONS

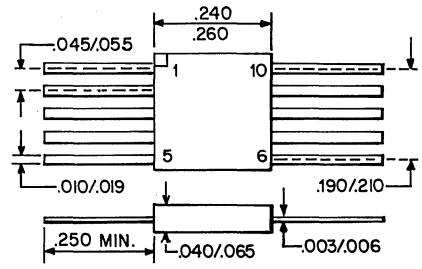
DIMENSIONS — FLAT PACK

1/4 X 3/16" 14 LEAD

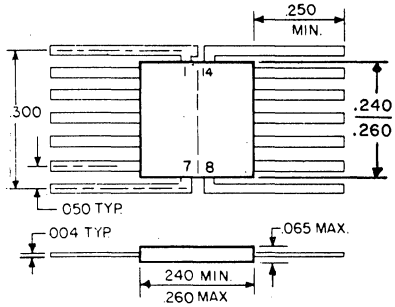


NOTES:
1. PACKAGE WEIGHT: 26 GRAMS

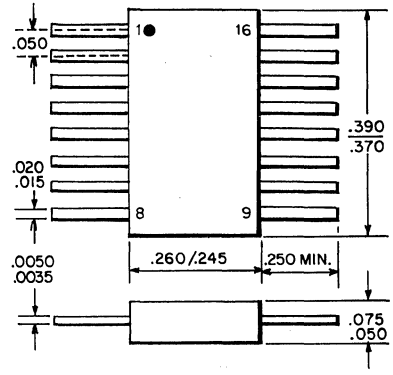
1/4 X 1/4" 10 LEAD



1/4 X 1/4" 14 LEAD



1/4 X 3/8" 16 LEAD



DIMENSIONS — DIODES

MECHANICAL DATA

Case: Hermetically sealed glass

Finish: All external surfaces corrosion resistant and leads readily solderable

Leads: Dumet, tin plated

Weight: 0.135 grams (approx.)

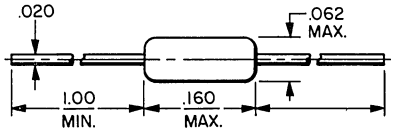
Mounting Position: Any

Marking: Diodes carry ITT identification, and are EIA Color Coded. Bands 1, 2, 3 and 4 on the illustration above indicate the first, second, third and fourth digit respectively of the type designation starting from the cathode end of the diode.

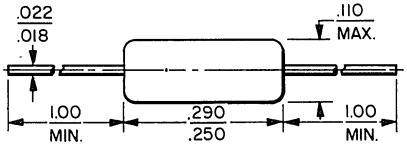
Black	0	Green	5
Brown	1	Blue	6
Red	2	Violet	7
Orange	3	Gray	8
Yellow	4	White	9

DOUBLE PLUG DIODE

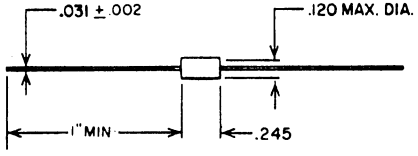
STANDARD



DO-35

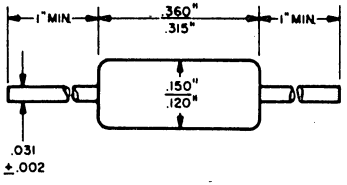


DO-7



EPOXY PACKAGE

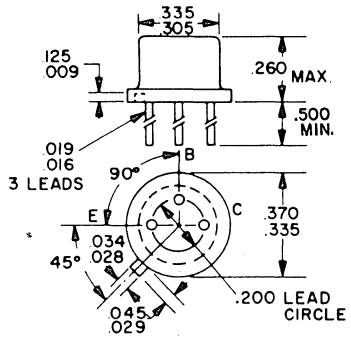
Lead-Material Silver Plated Copper



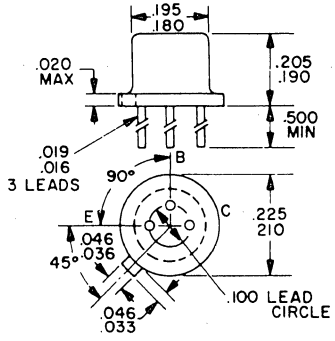
DO-29

PACKAGE DIMENSIONS

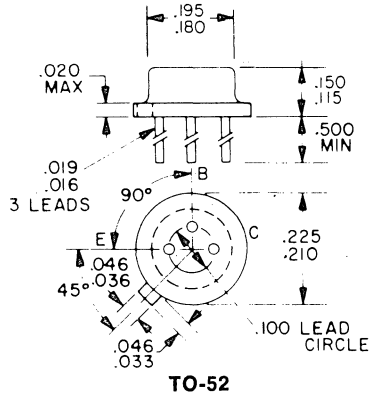
PHYSICAL DIMENSIONS



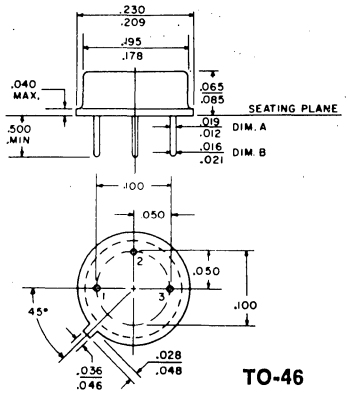
TO-5



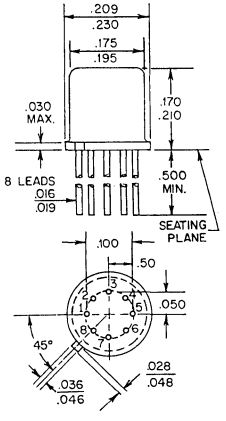
TO-18



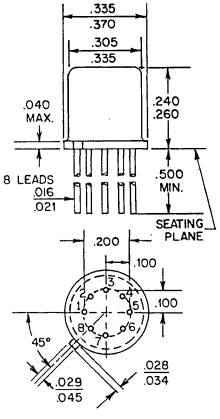
TO-52



TO-46

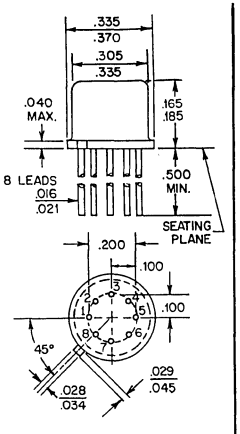


TO-71

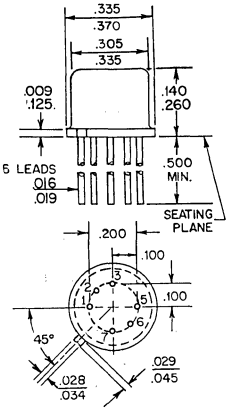


TO-77

NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.



TO-78

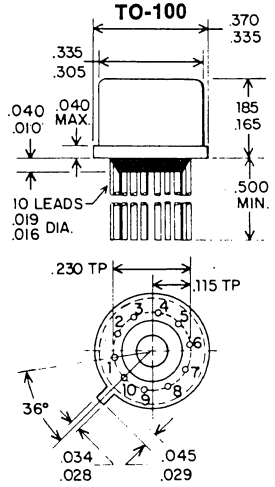


R-131c

ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.

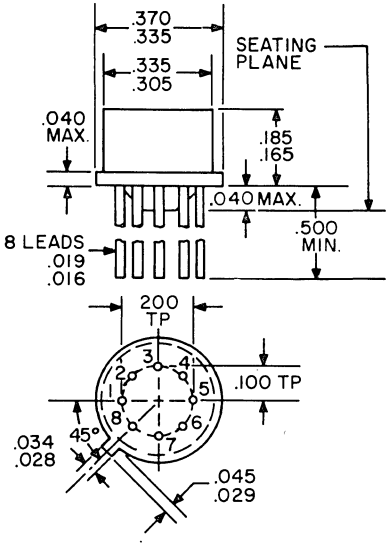
DIMENSIONS

TO-100



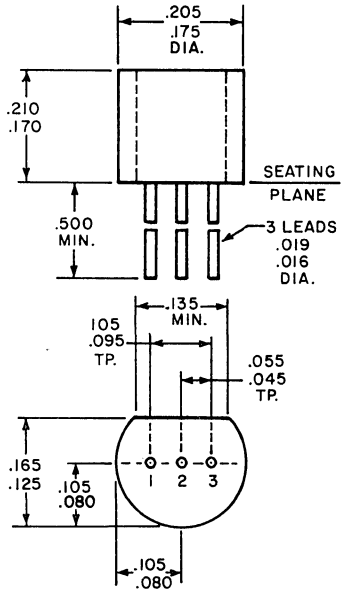
NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

TO-99



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.12 GRAMS.

TO-92 PACKAGE



NOTE-ON SPECIAL ORDER

ITT Semiconductors will provide TO-18, TO-46 and TO-52 units with formed leads to the requirements of the TO-5 package. In addition disc insulators on the above devices are also available by special order.

For Price and Delivery Information Call Your Local ITT Office

ARIZONA

ITT Semiconductors
Suite 209B
201 East Southern
Tempe, Arizona 85282
Telephone: 602-277-8166

CALIFORNIA

ITT Semiconductors
1121 San Antonio Road
Palo Alto, California 94303
Telephone: 415-961-5265
Telex: 0348-450

ITT Semiconductors
Suite 540
11222 La Cienega Boulevard
Inglewood, California 90304
Telephone: 213-649-4644
Telex: 653-552

ILLINOIS

ITT Semiconductors
Suite 709
8550 West Bryn Mawr
Chicago, Illinois 60631
Telephone: 312-693-7070
Telex: 025-4409
TWX: 910-253-4905

MASSACHUSETTS

ITT Semiconductors
Suite 19
594 Marrett Road
Lexington, Mass. 02173
Telephone: 617-861-0880
Telex: 092-3470

MICHIGAN

ITT Semiconductors
23629 Liberty Street
Suite 104
Farmington, Michigan 48024
Telephone: 313-477-6060
Telex: 023-5353

MINNESOTA

ITT Semiconductors
Office 140
4510 West 77th Street
Minneapolis, Minnesota 55435
Telephone: 612-920-2943
Telex: 029-0105

NEW YORK

ITT Semiconductors
Suite 3003
333 North Broadway
Jericho, Long Island, New York 11753
Telephone: 516-938-1191/2
Telex: 0961-416

ITT Semiconductors
7000 East Genesse Street
Fayetteville, New York 13066
Telephone: 315-445-0560
Telex: 093-7357

PENNSYLVANIA

ITT Semiconductors
676 East Swedesford Road
Wayne, Pennsylvania 19087
Telephone: 215-688-6990/1/2/3
Telex: 084-6351

TEXAS

ITT Semiconductors
2995 LBJ Freeway
Suite 204
Dallas,Texas 75234
Telephone: 214-243-6631

CANADA

ITT Semiconductors
Unit 2
1855 Dundas Street
Mississauga, Ontario, Canada
Telephone: 416-625-9022
Telex: 0696-1313

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