pLSI and ispLSI Data Book Supplement

▚ Lattice

Commercial Grade pLSI and ispLSI Devices

DEVICE	t_{pd}	f_{max}	DESCRIPTION	PAGE
pLSI 1016	12, 15, 20	90, 80, 60	44-pin programmable Large Scale Integration Device	3-1
pLSI 1024	15, 20	80, 60	68-pin programmable Large Scale Integration Device	3-17
pLSI 1032	15, 20	80, 60	84-pin programmable Large Scale Integration Device	3-33
pLSI 1048	18, 24	70, 50	120-pin programmable Large Scale Integration Device	3-49
ispLSI 1016	12, 15, 20	90, 80, 60	44-pin in-system programmable Large Scale Integration Device	4-1
ispLSI 1024	15, 20	80, 60	68-pin in-system programmable Large Scale Integration Device	4-21
ispLSI 1032	15, 20	80, 60	84-pin in-system programmable Large Scale Integration Device	4-41
ispLSI 1048	18, 24	70, 50	120-pin in-system programmable Large Scale Integration Device	4-61

Industrial Grade pLSI and ispLSI Devices

DEVICE	t_{pd}	f_{max}	DESCRIPTION	PAGE
pLSI 1016	20	60	44-pin programmable Large Scale Integration Device	3-1
pLSI 1024	20	60	68-pin programmable Large Scale Integration Device	3-17
pLSI 1032	20	60	84-pin programmable Large Scale Integration Device	3-33
pLSI 1048	24	50	120-pin programmable Large Scale Integration Device	3-49
ispLSI 1016	20	60	44-pin in-system programmable Large Scale Integration Device	4-1
ispLSI 1024	20	60	68-pin in-system programmable Large Scale Integration Device	4-21
ispLSI 1032	20	60	84-pin in-system programmable Large Scale Integration Device	4-41
ispLSI 1048	24	50	120-pin in-system programmable Large Scale Integration Device	4-61

Military Grade pLSI and ispLSI Devices

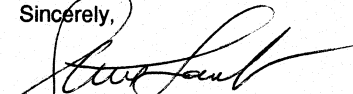| DEVICE	t_{pd}	f_{max}	DESCRIPTION	PAGE
pLSI 1016/883	20	60	44-pin programmable Large Scale Integration Device	5-3
pLSI 1024/883	20	60	68-pin programmable Large Scale Integration Device	5-13
pLSI 1032/883	20	60	84-pin programmable Large Scale Integration Device	5-23
pLSI 1048/883	24	50	132-pin programmable Large Scale Integration Device	5-33
ispLSI 1016/883	20	60	44-pin in-system programmable Large Scale Integration Device	5-43
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ispLSI 1048/883	24	50	132-pin in-system programmable Large Scale Integration Device	5-79

Thank you for your continued interest in our High-Density pLSI and ispLSI product families.

Lattice Semiconductor is pleased to provide you with this pLSI and ispLSI Data Book Supplement which includes Commercial, Industrial and Military data sheets for all eight members of the pLSI and ispLSI families of High-Density PLDs.

This Supplement is intended to be used in conjunction with our 1992 pLSI and ispLSI Data Book and Handbook which contains valuable information regarding development tools, design techniques, device quality and reliability.

We look forward to meeting your system design requirements with our high-performance pLSI and ispLSI Families.

Sincerely,

Steven A. Laub
Vice President and General Manager

pLSI and ispLSI
Data Book
Supplement

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Lattice

⋮⋮Lattice

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Introduction to pLSI and ispLSI

Introduction to pLSI and ispLSI

Lattice Semiconductor's pLSI (programmable Large Scale Integration) and ispLSI (in-system programmable Large Scale Integration) are two families of high-density and high-performance E^2CMOS® programmable logic devices (see figure 1-1). They provide design engineers with a superior system solution for integrating high-speed logic features on a single chip.

The Lattice pLSI and ispLSI families are the first programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI family also pioneers non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user reconfiguration.

Lattice's E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All the necessary development tools are available from Lattice and industry standard third-party vendors. Development tools offered range from Lattice's low cost pDS software, featuring Boolean entry in a graphical Windows™ based environment, to our pDS+ family of fitters that interfaces with third party development software packages. pDS+ features schematic capture, state machine and VHDL entry. Designs can now be completed in hours as opposed to days or weeks.

pLSI and ispLSI Product Features
- ❏ 90 MHz System Performance
- ❏ 12 ns Pin-to-Pin Delay
- ❏ Deterministic Performance
- ❏ High Density (2,000-8,000 PLD Gates)
- ❏ Flexible Architecture
- ❏ Easy-to-Use
- ❏ In-System Programmable (ispLSI)
- ❏ Low Power Consumption

pLSI and ispLSI Technology
- ❏ E^2CMOS — the PLD Technology of Choice
- ❏ Proven UltraMOS Technology
- ❏ Electrically Erasable/Programmable/ Reprogrammable
- ❏ 100% Tested During Manufacture
- ❏ 100% Programming Yield
- ❏ High-Speed Programming

pLSI and ispLSI Development Tools
- ❏ Easy-to-Use Graphical Interface (MS Windows)
- ❏ Boolean Equations and Macro Input
- ❏ VHDL and Schematic Capture Entry
- ❏ Industry-Standard Third-Party Design Environments and Platforms
- ❏ Timing and Functional Simulation

Figure 1-1. pLSI and ispLSI Device Families

pLSI 1016 ispLSI 1016	pLSI 1024 ispLSI 1024	pLSI 1032 ispLSI 1032	pLSI 1048 ispLSI 1048
44-Pin PLCC	68-Pin PLCC	84-Pin PLCC	120-Pin PQFP
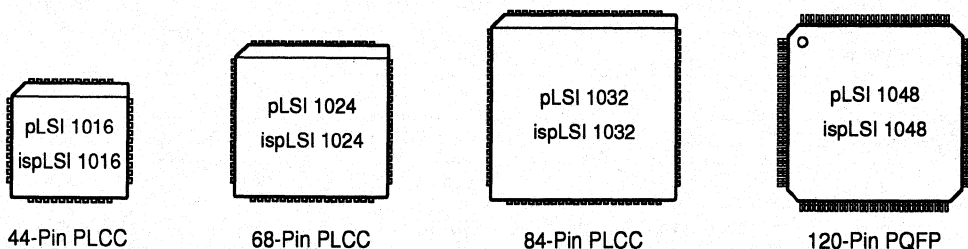
Introduction to pLSI and ispLSI

Family Overview

The pLSI and ispLSI families of high-density devices address high-performance system logic needs, ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD gate densities ranging from 2,000 to 8,000, the pLSI and ispLSI families provide a wide range of programmable logic solutions to meet design requirements for today's and tomorrow's needs.

Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1-1 describes the family attributes.

The pLSI and ispLSI Architecture

The pLSI and ispLSI architecture was constructed with actual system design requirements in mind. This architecture provides the designer with the following advantages. Figure 1-2 shows the pLSI 1032 architecture.

❑ High Speed

❑ Predictable Performance

❑ Integration of Multiple Logic Functions

❑ Asynchronous Designs

❑ Flexible Logic Paths

❑ Advanced Global Clock Network

The Global Routing Pool (GRP)

Central to the pLSI and ispLSI architecture is the Global Routing Pool (GRP) which connects all of the internal logic and makes it available to the designer. The GRP provides complete interconnectivity with fixed and predictable delays. This unique connection scheme consistently provides high performance and allows effortless implementation of complex designs.

The Output Routing Pool (ORP)

Pin assignment flexibility is maximized via the Output Routing Pool (ORP) which provides the connections between the GLB outputs and the output pins.

Figure 1-2. pLSI 1032 Architecture
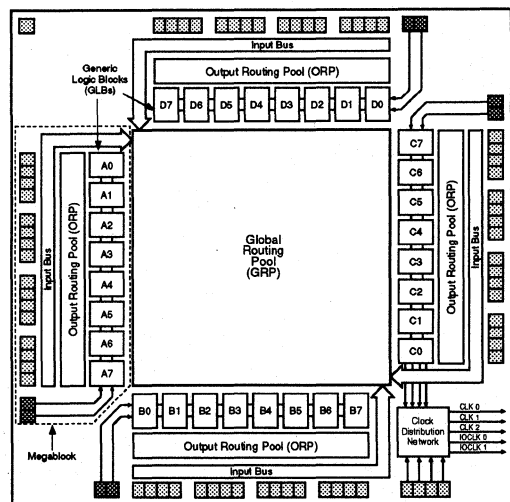
Table 1-1. pLSI and ispLSI Family Attributes

Family Member	1016	1024	1032	1048
Density (PLD Gates)	2,000	4,000	6,000	8,000
Speed: f_{max} (MHz)	90	80	80	70
Speed: t_{pd} (ns)	12	15	15	18
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs + I/O	36	54	72	106
Pin/Package	44-pin PLCC	68-pin PLCC	84-pin PLCC	120-pin PQFP

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Generic Logic Block (GLB)

The basic logic element in the pLSI and ispLSI architecture is the Generic Logic Block (GLB). This powerful logic element provides an input-to-output ratio greater than 4:1. With 18 inputs driving an array of 20 product terms (PTs) — which in turn feed four outputs — the GLB efficiently handles both wide and narrow gating functions. Figure 1-3 describes the GLB functionality.

One element of architectural flexibility is the Product Term Sharing Array (PTSA). The PTSA allows the 20 PTs from the AND array to be shared with any and all of the four GLB outputs as needed to implement logic designs. This ability to share PTs between all of the GLB outputs provides a highly efficient implementation of complex state machines by eliminating duplicate product term groups.

The architecture flexibility of the GLB, combined with its optimum input-to-output ratio, allows the GLB to implement virtually all 4-bit MSI functions.

Each of the four outputs from the PTSA feeds into a flexible Output Logic Macrocell (OLMC), consisting of a D-type flip-flop with an Exclusive-OR (XOR) gate on the input. The OLMC allows each GLB output to be configured either combinatorial or registered. Combinatorial mode is available as AND-OR or XOR; registered mode is available as D, T or J-K.

The GLB can be clocked synchronously or asynchronously. Global clocks from external pins or internally generated, provide all GLBs and I/O cells with synchronous clock signals with selectable polarity. This provides multiple synchronous clock phases to all GLBs and I/Os.

Figure 1-3. Simplified Generic Logic Block Functionality
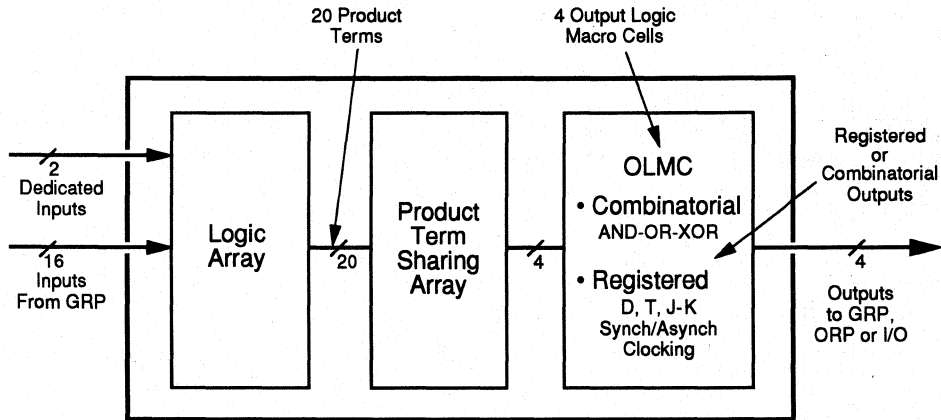
Introduction to pLSI and ispLSI

The GLB has several configuration options for each OLMC. These can be mixed within each GLB in any combination. The configurations are described individually for clarification and they are; standard, high-speed bypass, XOR and multi-mode configurations. Figure 1-4 demonstrates the multi-mode configuration.

Standard Configuration

❑ GLB Outputs have 4, 4, 5 or 7 Product Terms

❑ The PTSA Can Combine up to 20 PTs per GLB Output to Meet the Needs of Both Wide and Narrow Logic Functions.

High-Speed Bypass Configuration

❑ For Speed-Critical Timing Paths

❑ Enables Design of Fast Address Decoders

❑ Bypasses the PTSA and the Internal XOR Gate of the OLMC

❑ Provides Four Product Terms Per Output

XOR Configuration

❑ Utilizes Powerful XOR Architecture

❑ Powerful for Counters, Comparators and ALU Functions

Multi-Mode Configuration

❑ Individual Outputs are Independently Configurable

❑ PTSA Allows Flexibility on the Number and Selection of Product Terms Per Output

Figure 1-4. GLB: Multi-Mode Configuration
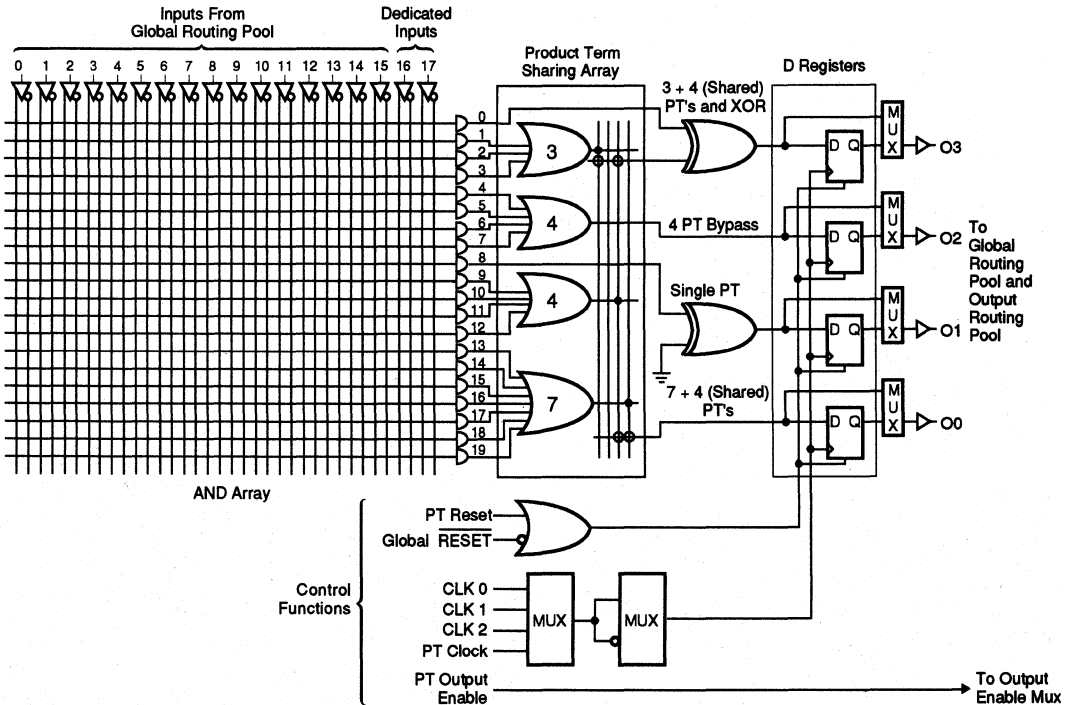
In-System Programmability

The in-system programmable Large Scale Integration (ispLSI) family is the industry's only high-density programmable logic family offering non-volatile in-system reconfigurability.

The ispLSI family is 100 percent functionally and parametrically compatible with the pLSI family, with the added ability of 5-volt in-system programmability and reprogrammability.

Complex logic functions can be implemented in multiple ispLSI devices, with complete on-board configurability. In-system programming of multiple ispLSI chip solutions is easily achieved through a proprietary in-system erase/program/verify technique.

In-system programmability can revolutionize the way boards are designed, manufactured and serviced (see figure 1-5).

Prototype Board Designs - In-system programming allows the programming and modification of logic designs "in-system" without removing the device(s) from the board.

This accelerates the system and board-level debug process and enables definition of board layout earlier in the design process.

Reconfigurable Systems - The options for accommodating changes are greatly increased when you have the ability to change the functionality of devices already soldered on a board. Multiple hardware configurations can be implemented with the same circuit board design. Multiple protocols or multiple system interfaces can be defined on a generic board as the last step in the manufacturing flow.

Diagnostic Capability - Using the ispLSI device, the diagnostic capability of the system can be enhanced. A test pattern can be programmed into the ispLSI device at board-test, enabling the logic to control and observe specific nodes on the board. After the diagnostic testing is complete, the functional pattern can be programmed into the device for normal system operation.

Easier Field Updates - With software reconfigurable systems, field updates are as easy as loading a new device configuration from a floppy, or downloading it through a modem.

Figure 1-5. In-System Programmable "Generic" Board
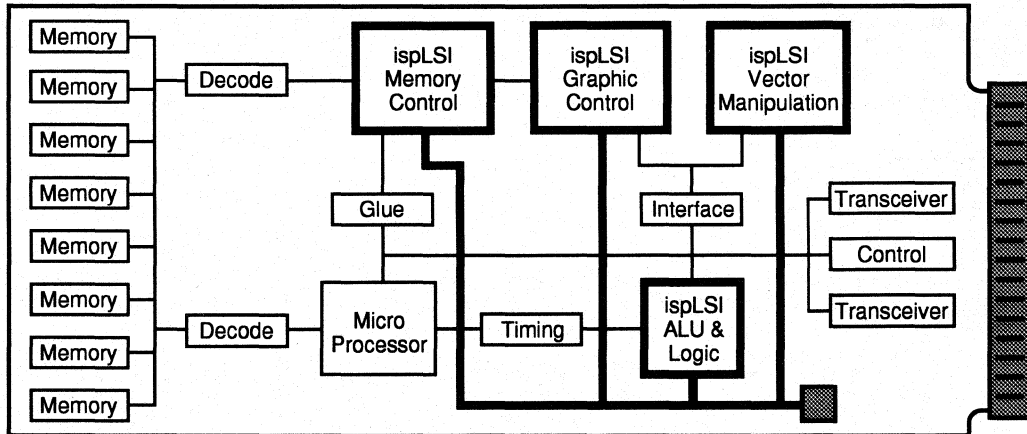
Multiple ispLSI devices can be reconfigured through multiplexed signals interfaced via an edge connector, 5-post connector, microcontroller or microprocessor.

ispLSI Devices

isp Interface

Introduction to pLSI and ispLSI

A powerful benefit of the ispLSI family is its potential to streamline the manufacturing process by eliminating the separate programming and labeling steps usually associated with PLDs. Quality is enhanced when product handling steps are reduced, in this case, those associated with programming, labeling and re-inventorying multiple device types. Eliminating socketing further improves quality and reduces board cost. Figure 1-6 shows the enhanced manufacturing with the ispLSI device.

All necessary programming is achieved via five TTL-level logic interface signals (see figure 1-7). These five signals control the on-chip programming circuitry, which protects against inadvertent reprogramming via on-chip state machines. The ispLSI family can also be programmed using popular third-party logic programmers.

Figure 1-6. Manufacturing Flow Comparison
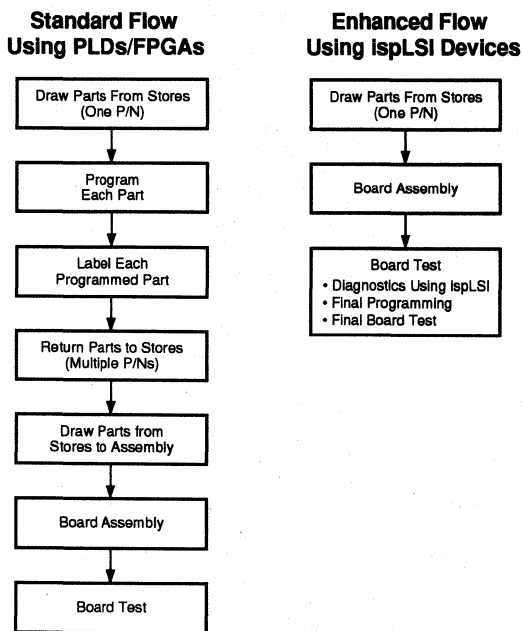
Figure 1-7. In-System Programming Interface (Multi-Chip Solution)
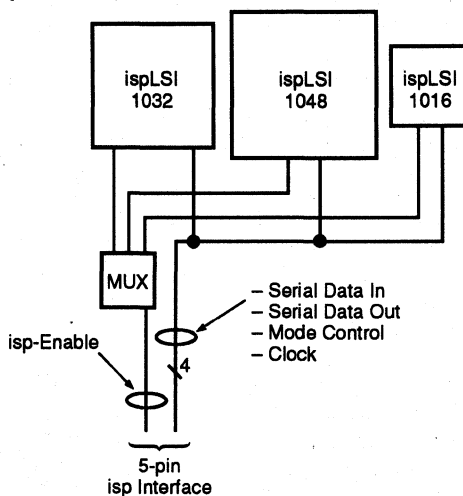
Lattice Development Systems

The Lattice pLSI/ispLSI Development System (pDS) software is used to implement designs in pLSI and ispLSI devices. Design alternatives can be quickly implemented using Lattice's low cost pDS software or the pDS+ family of fitters that interface with third-party development software packages. This section describes the pDS and pDS+ Development Systems. Programmer support is also discussed.

pLSI/ispLSI Development System (pDS)

Features

❑ High-Performance, Low-Cost Development Environment

❑ Supports pLSI and ispLSI Device Families

❑ Boolean Logic and Text File Design Entry

❑ Windows Based Graphical User Interface

❑ Over 225 Macros Available

❑ Automatic Place and Route

❑ Static Timing Table

❑ Logic Simulation with Viewlogic™ Viewsim™

❑ JEDEC File Download Direct to Programmer or ispLSI Device

General Description

Both the pLSI and ispLSI families are supported by Lattice's low-cost pDS software. It runs on IBM-compatible (386/486) PCs with Microsoft® Windows.

The easy-to-use graphical user interface with the familiar mouse driven pull-down menus, combined with Boolean logic data entry using ABEL™-like syntax, makes design entry with the pLSI and ispLSI quick and straightforward (see figure 1-8).

Figure 1-8. pDS Design Flow

Logic Design Entry	• Boolean Equations • Macros (>225) • "ABEL"-Like Syntax
Verification	• Logic Minimization • Checks for Signal Availability
Place and Route	• Automatic • Optimized • Fast
Simulation	• Viewsim • EDIF Compatible
Programming	• JEDEC File Generation • Download to Programmer or to Device (ispLSI)
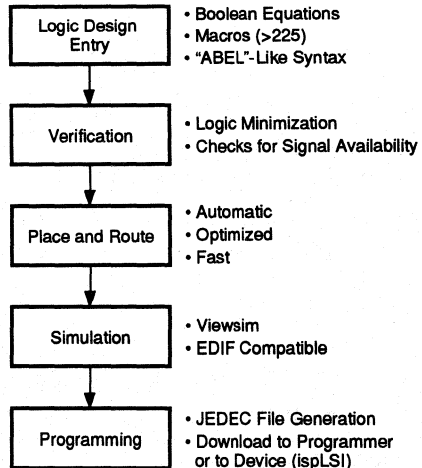
The pDS software supports over 225 macros to help the design process. These macros cover most TTL functions, from gate primitives to 16-bit counters. The software also supports user-definable macros which can be modifications of existing macros or custom creations.

The pDS software automatically verifies the design, performs logic minimization and checks for signal availability.

The Lattice Place and Route assigns pins and critical speed paths while routing the design.

Quick compilation speeds the design, debug and rework process dramatically. Incremental design techniques are also supported.

Timing and functional simulation are available from Lattice, using Viewsim simulation software.

The Windows graphical user interface makes programming easy, using pull-down menus, intuitive point-and-click commands and self explanatory instructions. Without any up-front training, designs can be completed within hours instead of days or weeks.

Introduction to pLSI and ispLSI

pLSI/ispLSI Development System Plus (pDS+)

Features

❑ Supports pLSI and ispLSI Device Families

❑ Schematic Capture, State Machine and VHDL Design Entry

❑ Expanded Macro Library (>350)

❑ Automatic Logic Minimization and Partitioning

❑ Automatic Place and Route

❑ Logic and Timing Simulation

❑ EDIF Compatible

❑ JEDEC File Download Direct to Programmer or ispLSI Device

General Description

For higher level design entry environments, Lattice offers pDS+ development software packages, which expand on the core capabilities of pDS. Schematic capture, state machine and VHDL entry are supported, along with an expanded macro library.

The pDS+ software utilizes industry standard third-party design environments such as Viewlogic's Viewdraw™ and Data I/O's ABEL.

Running on IBM compatible (386/486) PCs or workstation platforms, pDS+ software supports automatic logic minimization and partitioning as well as place and route, resulting in 100% routability at greater than 80% utilization.

For logic and timing simulation, support is available from Lattice through Viewlogic Viewsim simulation tools.

Third Party Programming Support

The pLSI and ispLSI families are supported by popular third-party logic programmers including Data I/O, Logical Devices, BP-Microsystems, Stag, System General, SMS Micro Systems and Advin. Table 1-2 describes each vendor's specific programmer models that support the pLSI and ispLSI devices. No proprietary, expensive, high pin-count programmers are required. Additionally, the ispLSI family can be programmed on the board (in-system), which eliminates the need for a stand-alone programmer. Package programming adapters are available from third-party manufacturers. For specific details refer to the Lattice Programming Tools Guide available from your local sales representative.

Table 1-2. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP-Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

isp Engineering Kit

The ispLSI family may also be programmed with Lattice's isp Engineering Kit. This kit is designed for engineering purposes only and is not intended for production use. By connecting an 8 wire cable to the parallel printer port of a PC, JEDEC files can be easily downloaded into the ispLSI device. Additionally, this cable can be connected directly to the circuit board facilitating on-board in-system programming.

2

pLSI and ispLSI
Architectural Description

Introduction

The basic unit of logic for the pLSI and ispLSI families is the Generic Logic Block (GLB). Figure 2-1 illustrates the pLSI 1032 with its 32 GLBs labelled A0, A1 .. D7. There are a total of 16 GLBs in the pLSI and ispLSI 1016 device, increasing to 48 GLBs in the pLSI and ispLSI 1048 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the Global Routing Pool (GRP) and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

The devices also have 32 to 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

The I/O cells are grouped in sets of 16 as shown in figure 2-1. Each of these I/O groups is associated with a Megablock through the use of the Output Routing Pool (ORP).

Eight GLBs, 16 I/O cells, one ORP and two dedicated inputs are connected together to make a Megablock. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each megablock shares a common Output Enable (OE) signal. The pLSI 1032 device, shown in figure 2-1 contains four Megablocks

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the devices are selected using the Clock Distribution Network. The dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (C0 on the pLSI and ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

2

Figure 2-1. pLSI 1032 Functional Block Diagram
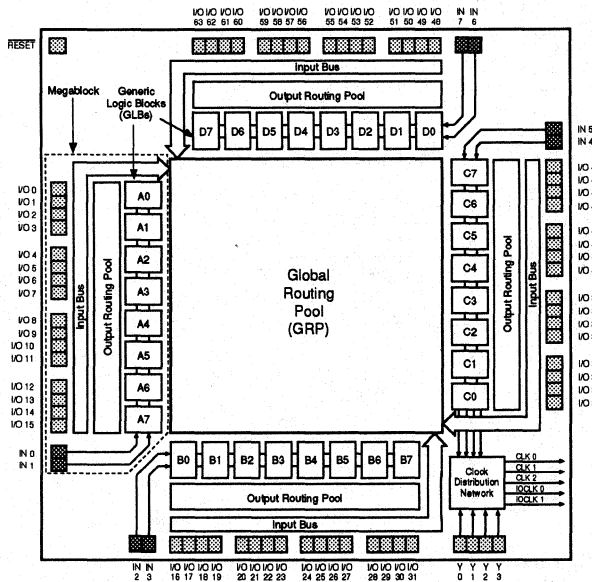
pLSI and ispLSI Architectural Description

Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of the Lattice High-Density pLSI and ispLSI devices. A GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections: the AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions (see figure 2-2). The AND array consists of 20 product terms which can produce the logical sum of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the GLBs or inputs from the external I/O cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes boolean logic reduction more efficient.

The PTSA takes the 20 product terms and routes them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms each (see figure 2-2). The output of any of these OR gates can be routed to any

of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. In addition, the PTSA can share product terms similar to a PLA device. If the user's main concern is speed, the PTSA can use a bypass circuit which provides four product terms to each output, to increase the performance of the cell (see figure 2-3). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop (see figure 2-4). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

Figure 2-2. GLB: Product Term Sharing Array Example
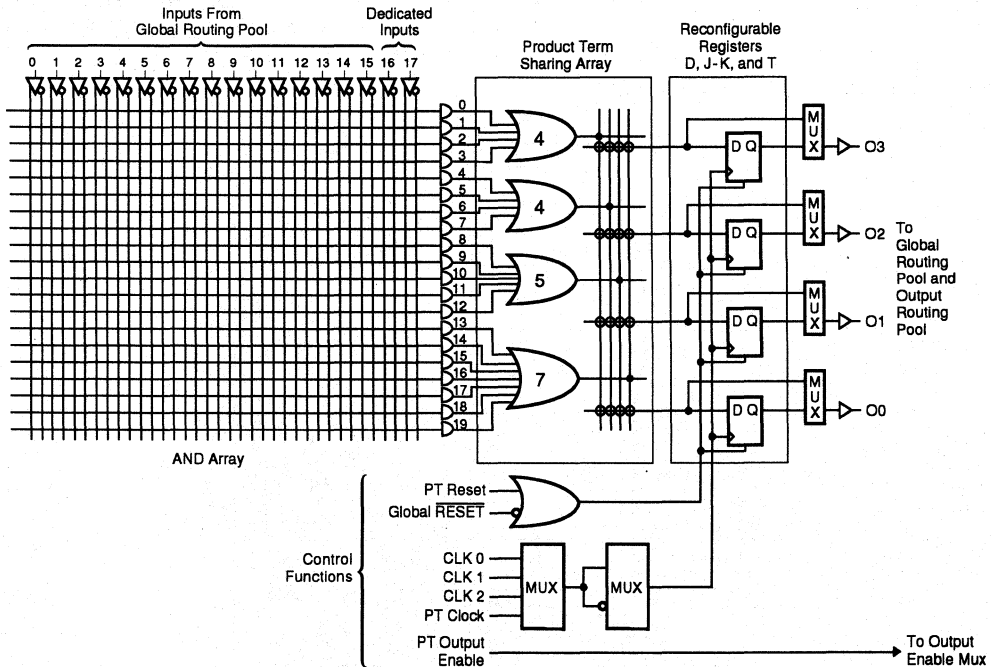
Figure 2-3. GLB: Four Product Term Bypass Example
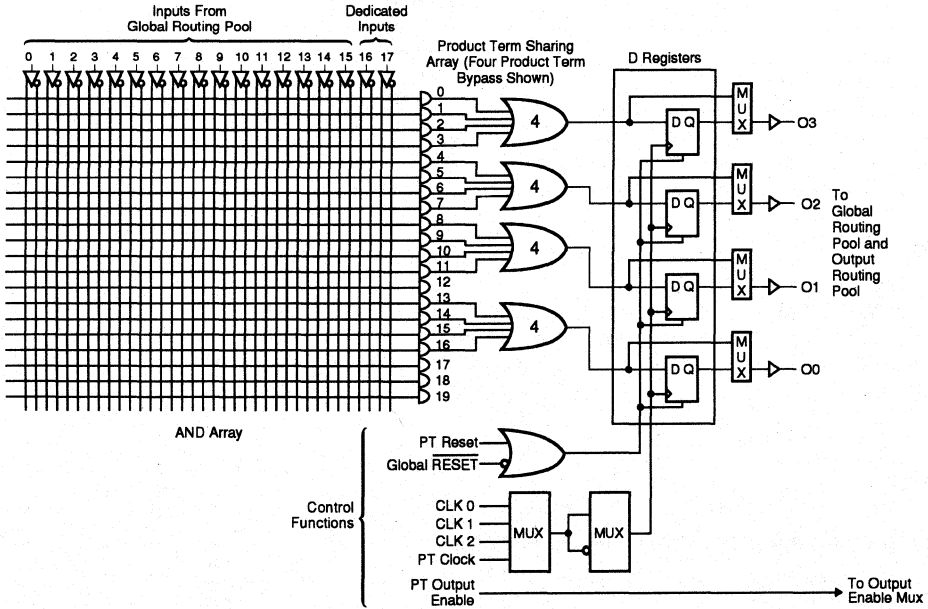
Figure 2-4. GLB: XOR Gate Example
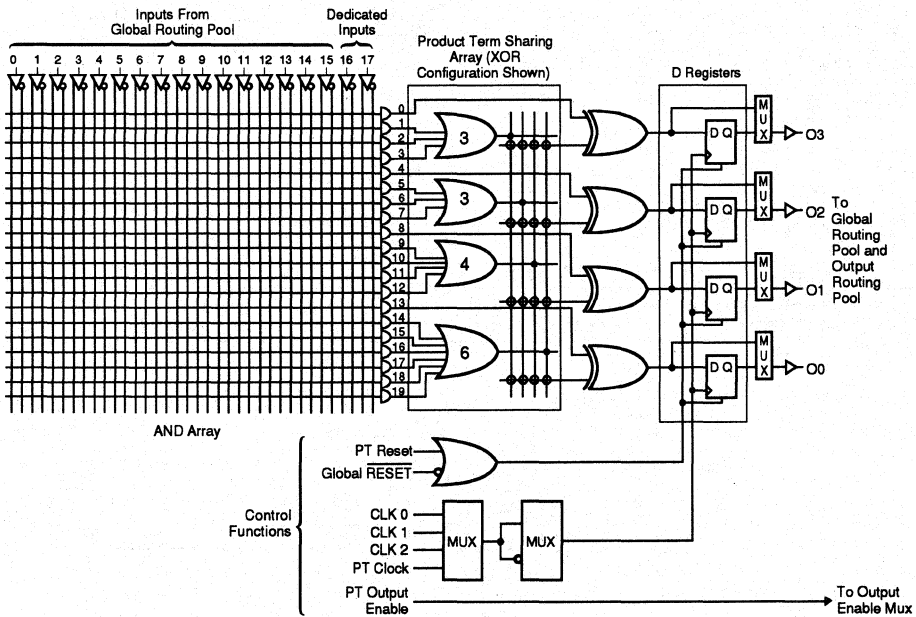
pLSI and ispLSI Architectural Description

Generic Logic Block (continued)

The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in figure 2-5, Output Three (O3) is configured using the XOR gate while Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals which control the operation of the GLB outputs are driven from the Control Functions (see figure 2-5). The clock for the registers can come from any of three sources developed in the Clock Distribution Network (see Clock Distribution Network section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin (RESET) or from a product term within the block. The global reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to a logic 0 state. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the Product Term Sharing Matrix (table 2-1) to determine which logic functions are affected.

There are many additional features in a GLB which allow implementation of logic intensive functions. These features are accessible using the Hard Macros from the software and require no intervention on the part of the user.

Figure 2-5. GLB: Various Logical Combination Examples
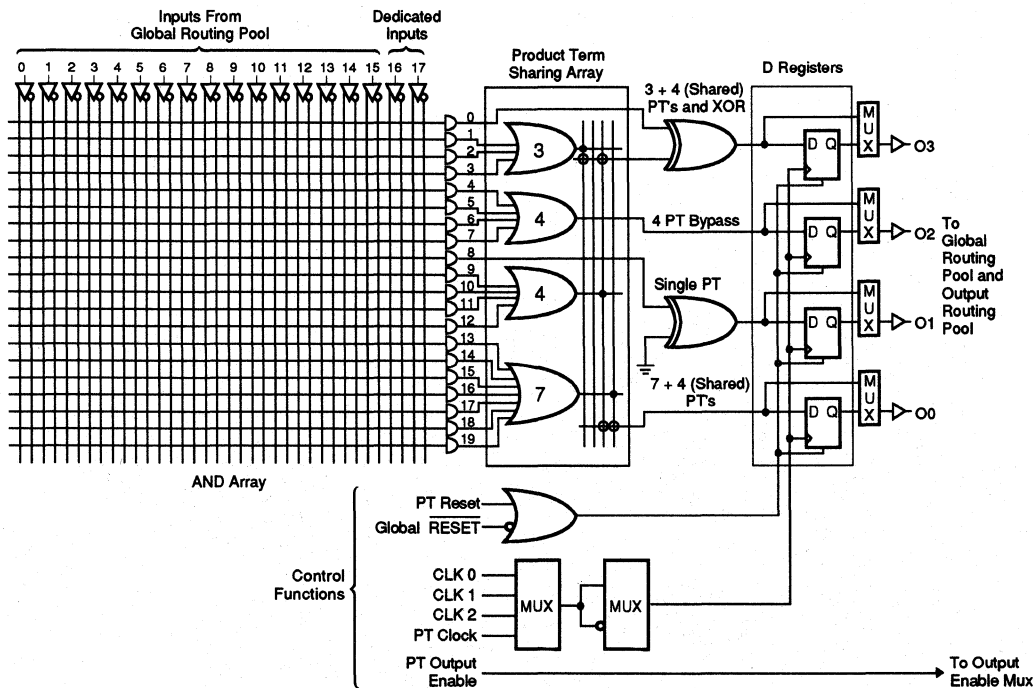
Product Term Sharing Matrix

This matrix shows how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the XOR mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

Table 2-1. Product Term Sharing Matrix

Product Term #	Standard Configuration Output Number				Four Product Term Bypass Output Number				Single Product Term Output Number				XOR Function Output Number								Alternate Function
	3	2	1	0	3	2	1	0	3	2	1	0	3	3	2	2	1	1	0	0	
0	■	■	■	■	■				■				■								
1	■	■	■	■	■									■							
2	■	■	■	■	■									■							
3	■	■	■	■	■									■							
4	■	■	■	■		■				■					■						
5	■	■	■	■		■										■					
6	■	■	■	■		■										■					
7	■	■	■	■		■										■					
8	■	■	■	■			■				■						■				
9	■	■	■	■			■											■			
10	■	■	■	■			■											■			
11	■	■	■	■			■											■			
12	■	■	■	■														■			■CLK/Reset
13	■	■	■	■				■				■							■		
14	■	■	■	■				■												■	
15	■	■	■	■				■												■	
16	■	■	■	■				■												■	
17	■	■	■	■																■	
18	■	■	■	■																■	
19	■	■	■	■																■	■ OE/Reset

The Megablock

A Megablock consists of eight GLBs, an ORP, 16 I/O cells, two dedicated inputs and a common OE. Each of these will be explained in detail in the following sections. These elements are coupled together as shown in figure 2-6. The various members of the pLSI and ispLSI families combine from two to six Megablocks on a single device (see table 2-2).

The eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-registered) inputs only and are automatically assigned by software. The OE signal is generated within the Megablock and is common to all sixteen of the I/O cells in the Megablock. The OE signal can be generated using a product term (PT19) in any of the eight GLBs within the Megablock (see the section on the Output Enable Control for further details).

Because of the shared logic within the Megablock, signals which share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

pLSI and ispLSI Architectural Description

Table 2-2. Device Resources

pLSI and ispLSI Devices	Megablocks	GLBs	I/O Cells	Dedicated Inputs
1016	2	16	32	4
1024	3	24	48	6
1032	4	32	64	8
1048	6	48	96	10

Figure 2-6. The Megablock Block Diagram
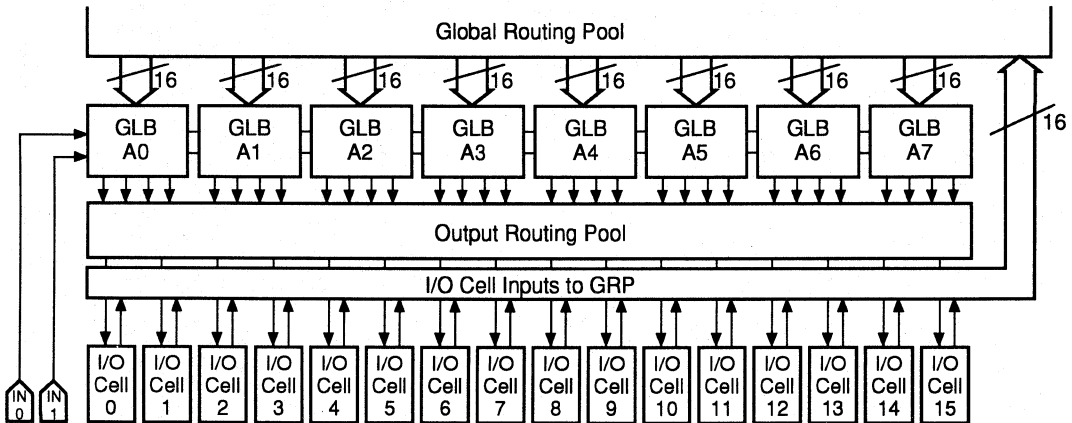
Input Routing

Signal inputs are handled in two ways within the device. First, each I/O cell within the device has its input routed directly to the GRP. This gives every GLB within the device access to each I/O cell input. Second, each Megablock has two dedicated inputs which are directly routed to the eight GLBs within the Megablock. Both input paths are shown in figure 2-6.

The Output Routing Pool

The ORP routes signals from the GLB outputs to I/O cells configured as outputs or bi-directional pins (see figure 2-7). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the ORP in figure 2-7, it can be seen that a GLB output can be connected to one of four I/O cells. Further flexibility is provided by using the PTSA, (figures 2-2 through 2-5) which makes the GLB outputs completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see figure 2-8) further increase the flexibility of the device. The ORP bypass connects specific GLB outputs to specific I/O cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

Figure 2-7. Output Routing Pool
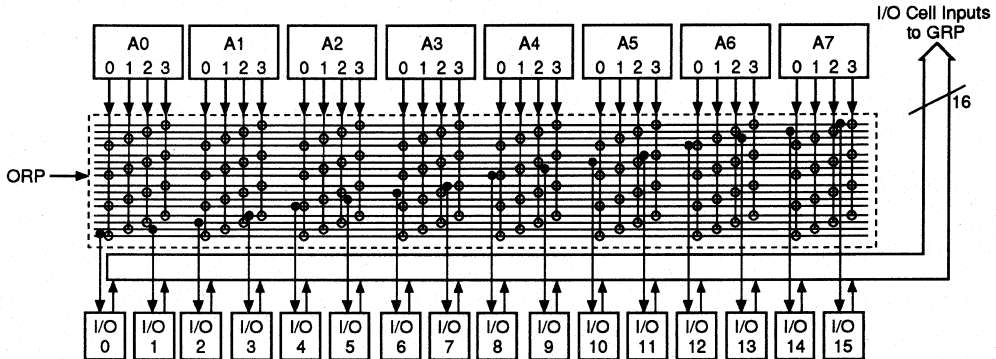
Figure 2-8. Output Routing Pool showing Bypass
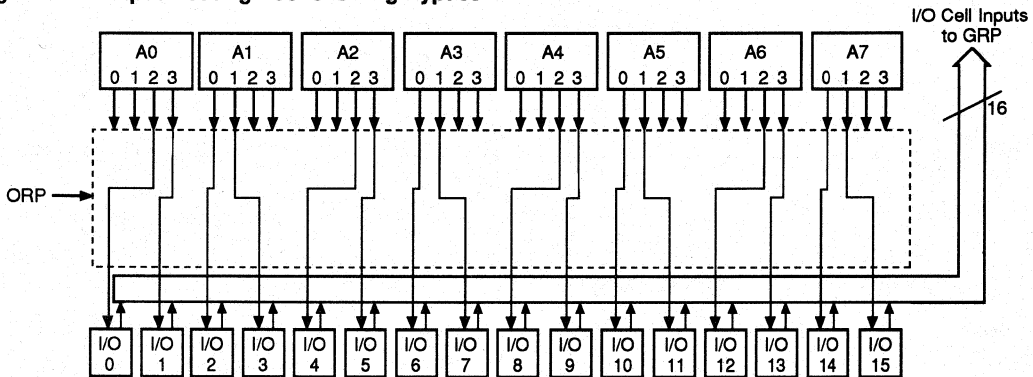
I/O Cell

The I/O cell (see figure 2-9) is used to route input, output or bi-directional signals connected to the I/O pin. The two logic inputs come from the ORP (see figure 2-9). One comes from the ORP, and the other comes from the faster ORP bypass. A pair of multiplexers select which signal will be used, and its polarity. The Output Enable of the I/O cell is controlled by the OE signal generated within each Megablock.

As with the data path, a multiplexer selects the signal polarity. The Output Enable can be set to a logic high (enabled) when an output pin is desired, or logic low (disabled) when an input pin is needed. The Global Reset (RESET) signal is driven by the active low chip reset pin.

This reset is always connected to all GLB and I/O registers. Each I/O cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). These clock signals are generated by the Clock Distribution Network.

Using the multiplexers, the I/O cell can be configured as an input, an output, a 3-stated output or a bi-directional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the incoming data. Figure 2-10 illustrates some of the various I/O cell configurations possible.

There is an active pull-up resistor on the I/O pins which is automatically used when the pin is not connected. An option exists to have active pull-up resistors connected to all pins. This improves the noise immunity and reduces Icc for the device.

pLSI and ispLSI Architectural Description

Figure 2-9. I/O Cell Architecture
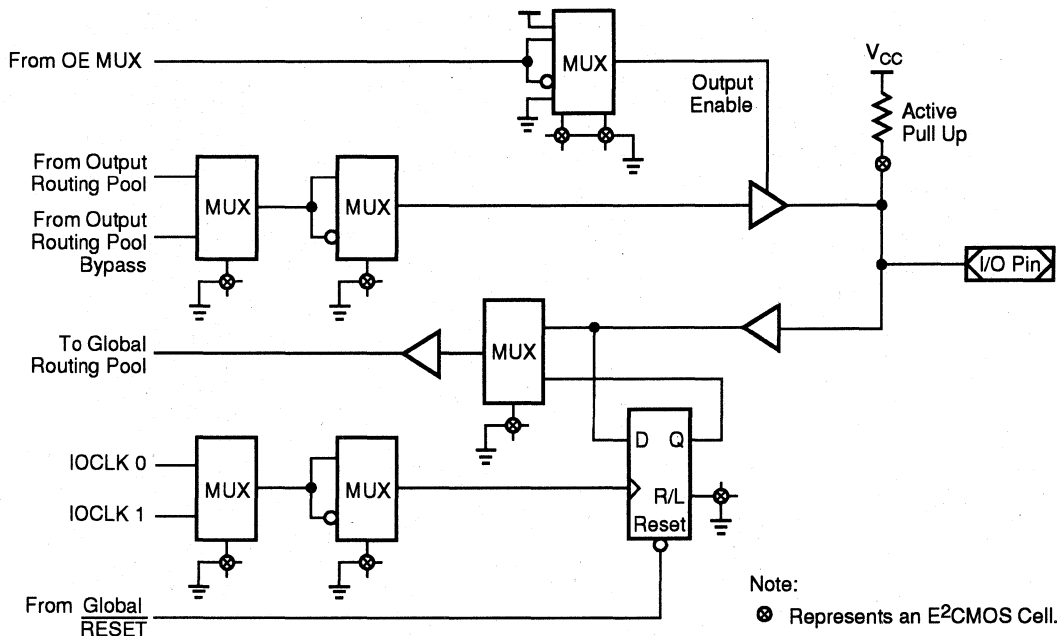
Figure 2-10. Examples of I/O Cell Configurations

Input Buffer

Latch Input

Registered Input

Input Cells

Output Buffer

Inverting Output Buffer

Output Buffer with 3-State Enable

Output Cells

Bi-Directional I/O Pin

Bi-Directional I/O Pin With Registered Input

Bi-Directional Cells
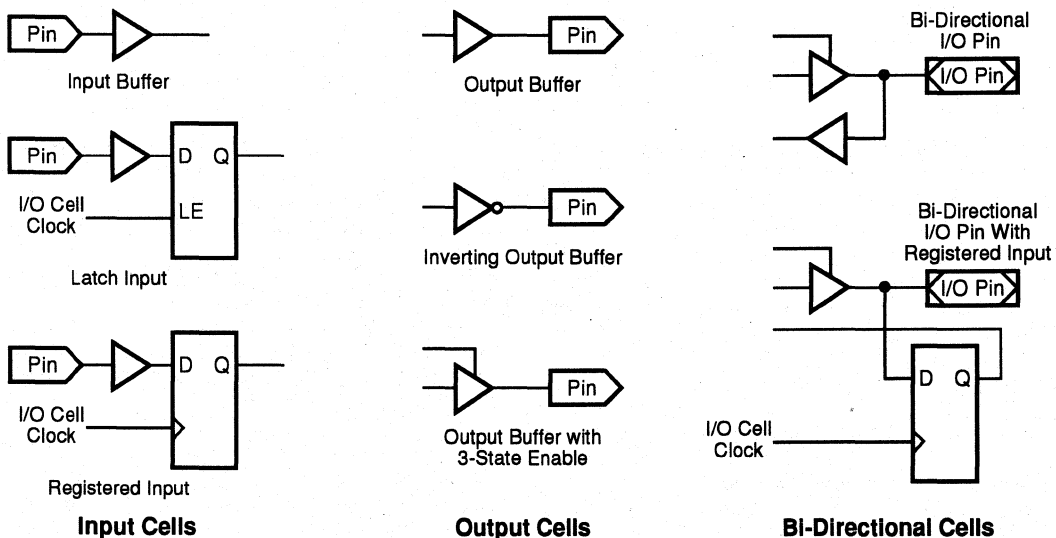
The Output Enable Control

One OE signal can be generated within each GLB using the OE Product Term (PT19). One of the eight OE signals within a Megablock is then routed to all of the I/O cells within that Megablock (see figure 2-11). This OE signal can simultaneously control all of the 16 I/O cells which are used in 3-state mode. Individual I/O cells also have independent control for permanently enabling or disabling the output buffer (refer to the I/O cell section). Only one OE signal is allowed per Megablock for 3-state operation. The advantage to this approach is that the OE signal can be generated in any GLB within the Megablock which happens to have an unused OE product term. This frees up the other OE product terms for use as logic.

Figure 2-11. Output Enable Control for a Megablock
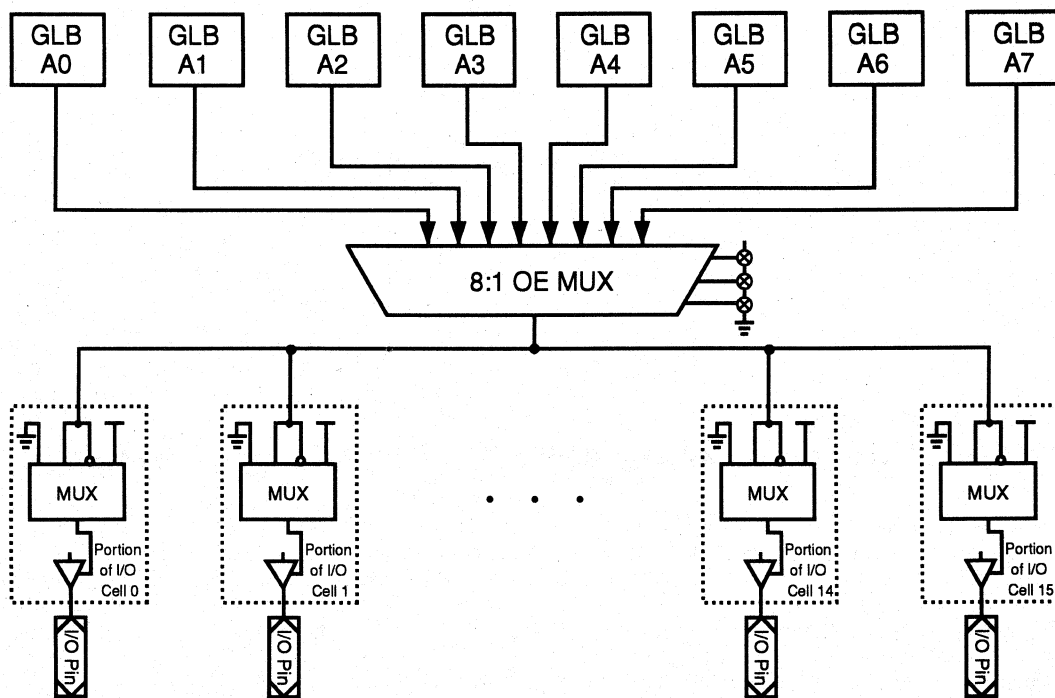
pLSI and ispLSI Architectural Description

The GRP is a Lattice proprietary interconnect structure which offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the pLSI and ispLSI devices, the delays through the GRP are both consistent and predictable. However, they are slightly affected by GLB loading as shown in the example pLSI 1032-80 GLB Loading Delay graph (see figure 2-12).

Figure 2-12. Example Graph of GRP Delay vs GLB Loading
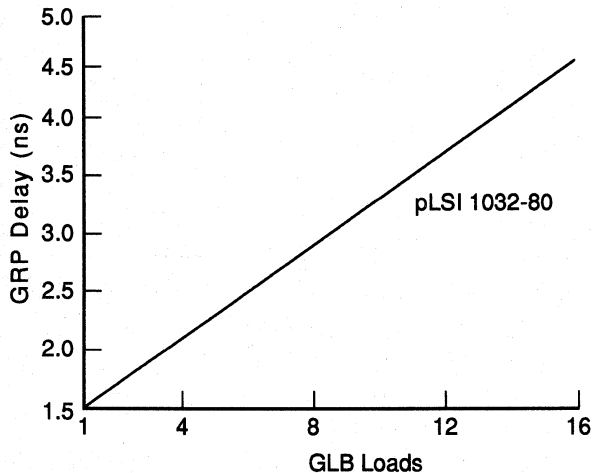
The Clock Distribution Networks are shown in figure 2-13. They generate five global clock signals CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 are used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O cells in the device. There are four dedicated system clock pins (Y0, Y1, Y2, Y3), three for the pLSI and ispLSI 1016 (Y0, Y1, Y2), which can be directed to any GLB or any I/O cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the four outputs of a dedicated clock GLB ("C0" for the pLSI 1032 is shown in figure 2-1). These clock GLB outputs can be used to create a user-defined internal clocking scheme.

For example, the clock GLB can be clocked using the external main clock pin Y0 connected to global clock signal CLK 0. The outputs of the clock GLB in turn can generate a "divide by" signal of the CLK 0 which can be connected to CLK 1, CLK 2, IOCLK 0 or IOCLK 1 global clock lines.

All GLBs have the capability of generating their own asynchronous clocks using the clock Product Term (PT12). CLK 0, CLK 1 and CLK 2 feed to their corresponding clock MUX inputs on all the GLBs (see figure 2-2).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all the I/O cells and the user programs the I/O cell to use one of the two.

Figure 2-13. Clock Distribution Networks
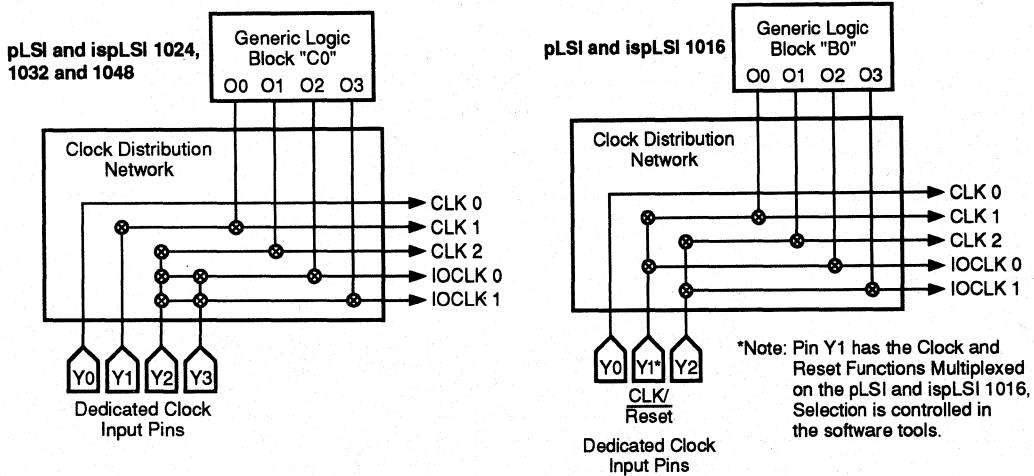
2

Security Cell

A security cell is provided in the pLSI and ispLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

pLSI and ispLSI devices are programmed using a Lattice-approved device programmer, available from a number of third party manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user. In-system programming is available with ispLSI devices only, this allows programming on the circuit board using Lattice programming algorithms and standard 5V system power.

Latch-up Protection

pLSI and ispLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latch-up. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

pLSI and ispLSI Architectural Description

Timing Model

The task of determining the timing through the device is simple and straightforward. The device timing model is shown in figure 2-14. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 2-15). Critical timing paths are shown in figure 2-14, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. (External timing parameters are tested and guaranteed on every device).

Figure 2-14. pLSI and ispLSI Timing Model[1]
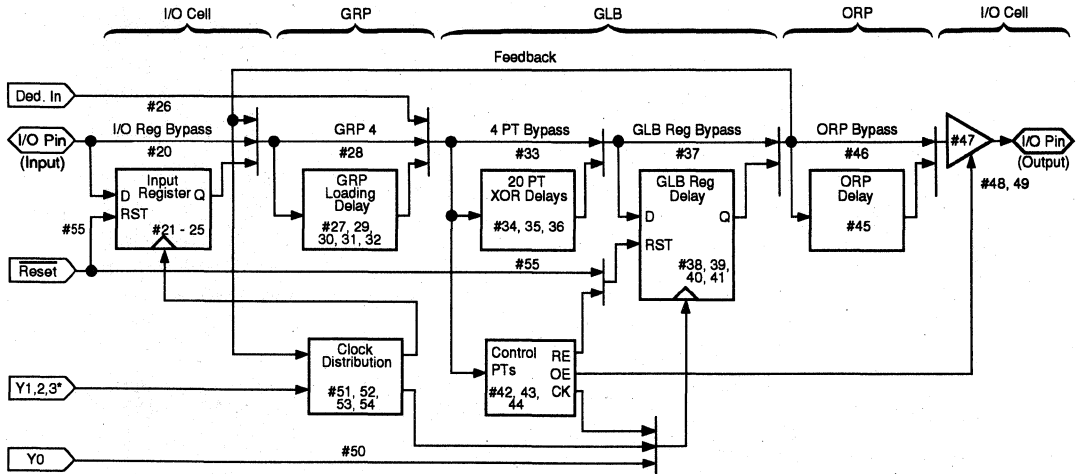
*Note: Y1 and Y2 only for the pLSI and ispLSI 1016.

Figure 2-15. pLSI and ispLSI Timing Model Examples[1]

Combinatorial Paths

t_{pd1}	=	t_{iobp}	+	t_{grp4}	+	t_{4ptbp}	+	t_{orpbp}	+	t_{ob}
#1	=	#20	+	#28	+	#33	+	#46	+	#47

t_{pd2}	=	t_{iobp}	+	t_{grp4}	+	t_{xoradj}	+	t_{orp}	+	t_{ob}
#2	=	#20	+	#28	+	#36	+	#45	+	#47

Registered Paths

General Form:

t_{su}	=	Logic	+	Regsu	-	Clock(min)
t_h	=	Clock(max)	+	Regh	-	Logic
t_{co}	=	Clock(max)	+	Regco	+	Output

Specific Examples:

t_{su1}	=	(t_{iobp}	+	t_{grp4}	+	t_{4ptbp})	+	t_{gsu}	-	t_{gy0}(min)
#6	=	(#20	+	#28	+	#33)	+	#38	-	#50

t_{h1}	=	t_{gy0}(max)	+	t_{gh}	-	(t_{iobp}	+	t_{grp4}	+	t_{4ptbp})
#8	=	#50	+	#39	-	(#20	+	#28	+	#33)

t_{co1}	=	t_{gy0}(max)	+	t_{gco}	+	(t_{orpbp}	+	t_{ob})
#7	=	#50	+	#40	+	(#46	+	#47)

1. The timing parameter reference numbers refer to the Internal Timing Parameters contained in the individual data sheets.

Figure 2-15. pLSI and ispLSI Timing Model Examples[1] (continued)

$$t_{su2} = (t_{iobp} + t_{grp4} + t_{xoradj}) + t_{gsu} + t_{gy0}(min)$$
$$\#9 = (\#20 + \#28 - \#36) + \#38 + \#50$$

$$t_{h2} = t_{gy0}(max) + t_{gh} - (t_{iobp} + t_{grp4} + t_{xoradj})$$
$$\#11 = \#50 + \#39 - (\#20 + \#28 + \#36)$$

$$t_{co2} = t_{gy0}(max) + t_{gco} + (t_{orp} + t_{ob})$$
$$\#10 = \#50 + \#40 + (\#45 + \#47)$$

2

1. The timing parameter reference numbers refer to the Internal Timing Parameters contained in the individual data sheets.

Circuit Timing Example

Figure 2-16. Timing Calculation Example

A design requires two logic levels (each uses the 20PTXOR path). The design then uses a GLB register before exiting the device using the ORP bypass. Calculate t_{su}, t_h and t_{co}.
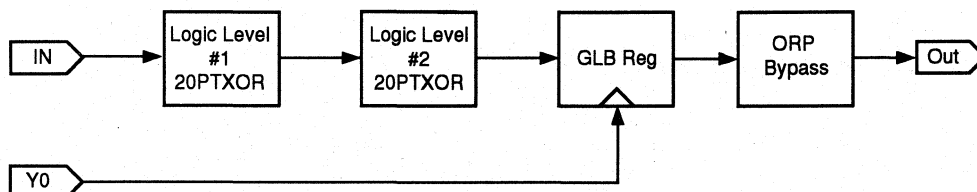
t_{su}		= Logic +Reg su - Clock (min)
	=	$(t_{iobp} + t_{grp4} + t_{20ptxor} + t_{gbp} + t_{grp4} + t_{20ptxor}) + t_{gsu} - t_{gy0}(min)$
	=	(#20 + #28 + #35 + #37 + #28 + #35) + #38 - #50
19.5 ns	=	(2.0 + 2.0 + 8.0 + 1.0 + 2.0 + 8.0) + 1.0 - 4.5

t_h		= Clock (max) + Reg h - Logic
	=	$t_{gy0}(max) + t_{gh} - (t_{iobp} + t_{grp4} + t_{20ptxor} + t_{gbp} + t_{grp4} + t_{20ptxor})$
	=	#50 + #39 - (#20 + #28 + #35 + #37 + #28 + #35)
-14.0 ns	=	4.5 + 4.5 - (2.0 + 2.0 + 8.0 + 1.0 + 2.0 + 8.0)

t_{co}		= Clock (max) + Reg co + Output
	=	$t_{gy0}(max) + t_{gco} + (t_{orpbp} + t_{ob})$
	=	#50 + #40 + (#46 + #47)
10.0 ns	=	4.5 + 2.0 + (0.5 + 3.0)

1. The delay values used are for a pLSI 1032-80 device.

ispLSI Programming Information

The following general programming information on the ispLSI (in-system programmable Large Scale Integration) devices describes how the internal state machine is implemented for programming and how to use the five programming interface signals to step through the state machine. The device specific information, such as timing and pin outs, can be found in the individual data sheets. The programming information given in this section applies to all ispLSI devices.

Programming Overview

To distinguish between normal operation and programming, two modes are defined: normal mode and edit mode. Once the device is in edit mode, the entire programming operation of the device is controlled by the internal isp state machine. The in-system programming enable (ispEN) signal controls the device operation modes.

The programming is controlled by the on-chip state machine via five programming interface signals. The ispEN signal is used to enable and disable the four programming control signals which include Serial Data In (SDI), Mode (MODE), Serial Data Out (SDO) and Serial Clock (SCLK). When the device is in normal mode, the four programming control signal pins can be used as normal Dedicated Input Pins. Figure 2-17 illustrates one such possible configuration for programming multiple ispLSI devices. With this scheme the ispEN signal for individual devices is enabled separately and one device is placed in the edit mode at a time. Since the other devices are in the normal mode, they can continue to perform normal system functions. This simple scheme requires connecting all four programming control signal pins together and precludes their use as dedicated inputs for normal system functions. ispEN is the only programming interface signal that is dedicated to a pin.

Figure 2-17. ispLSI Programming Interface
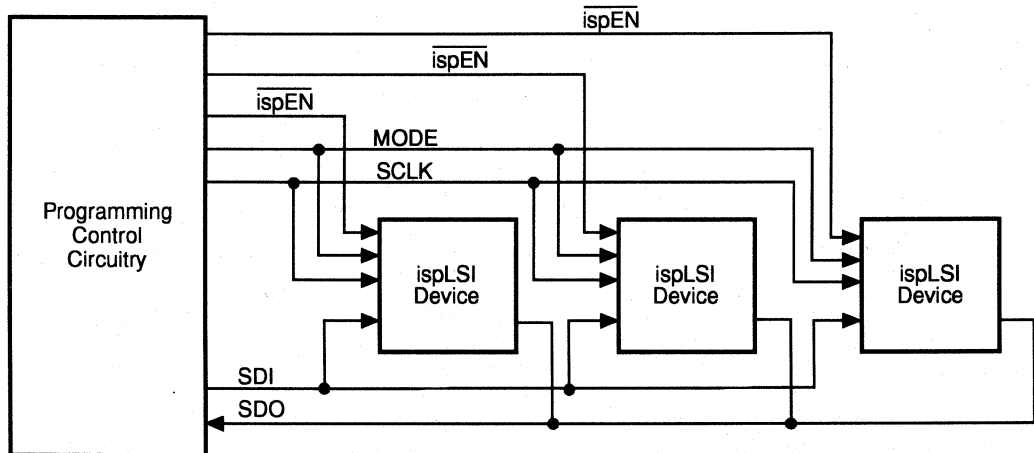
Normal Mode

In Normal Mode the four programming control pins become Dedicated Input pins. By multiplexing the programming control pins, these programming control pins can have a normal input function during Normal Mode. Figures 2-18 and 2-19 illustrate two alternate schemes which allow the designer to utilize the four programming control signal pins for performing normal system functions. Internal to the device, the programming functions are completely isolated from the normal operating functions when the device is in Normal Mode. Keeping the ispEN signal high puts the device in Normal Mode. For simplicity, the four programming control pins can be left unused for normal input functions. These pins can be reserved for isp use using the isp switch in the development tools. By leaving these pins unused, the programming interface is simplified when the programming signals and the Normal Mode input signals are not multiplexed.

Edit Mode

Programming circuitry is enabled by driving the ispEN signal low which puts the device in Edit Mode. In Edit Mode, all the functional I/O pins and input pins that are not used during programming are 3-stated. With the exception of the SDO signal, the remainder of the programming interface signals are input signals. When multiplexing the programming interface signals, the input driving the SDO pin must be 3-stated to make sure that there is no signal contention. All programming is accomplished in the Edit Mode by controlling the programming state machine with the MODE and SDI signals. SCLK is used to clock programming data in and out through SDI and SDO pins. SDI has a dual role as one of the two control signals for the state machine and as the serial data input. To avoid any internal register data contentions, Lattice recommends that the device Reset pin be pulled to ground when the device is in Edit Mode.

Programming Interface

The five programming interface pins are ispEN, SDI, MODE, SDO and SCLK. Once in Edit Mode, programming is controlled by SDI, MODE, SDO and SCLK signals. In Normal Mode, the programming control pins can be used as dedicated inputs to the device.

ispEN is an active low, dedicated enable pin, which enables the four programming control pins when it is driven low (V_{IL}) and disables the programming control pins when it is driven high (V_{IH}). All other I/O pins are 3-stated during Edit Mode and pulled up by the internal active pull-up resistors (equivalent to 100KΩ).

SDI performs two different functions. First, as the input to the serial shift register and second, as one of the two control pins for the programming state machine. Because of this dual role, SDI's function is controlled by the MODE signal. When MODE is low SDI is the serial input to the shift registers and when MODE is high SDI becomes the control signal. Internal to the device, the SDI is multiplexed to address shift register, high order data shift register and low order data shift register. The different shift instructions of the state machine determine which of these shift registers gets the input of the SDI.

The MODE signal combined with the SDI signal controls the programming state machine. This signal connects in parallel to all ispLSI devices.

SCLK is the serial shift register clock that is used to clock the internal serial shift registers. A low-to-high (positive) clock transition clocks the state machine. It also connects in parallel to all ispLSI devices. Similar to SDI, the shift instructions determine which of the shift registers are clocked for the data input from SDI.

SDO is the output of the serial shift registers. The selection of shift register is determined by the state machine's shift instruction. In the flow through instruction and when MODE is driven high, the SDO connects directly to the SDI, and bypasses the device's shift registers. Since this is the only output pin for the Edit Mode, this signal will drive the external devices that are connected to this pin.

Programming Details

The programming is completely controlled by the state machine, once the device is in the Edit Mode. The state machine consists of three states, in which all programming related operations are performed. In order to run these programming operations, five bit instructions are defined (see table 2-4). Each instruction is then shifted into the device in one of the three states and executed in another state. The initial state of the state machine is used when the device is idle during edit, or to shift out the eight bit device identification code.

The following sections describe the general information about the critical timing parameters, state machine, state machine instructions, and device layout that apply to all the ispLSI devices. Any device specific information like the size of the shift registers and the device specific timing information can be found in the individual device data sheet.

pLSI and ispLSI Architectural Description

Figure 2-18. The Scan and Multiplex Programming Mode
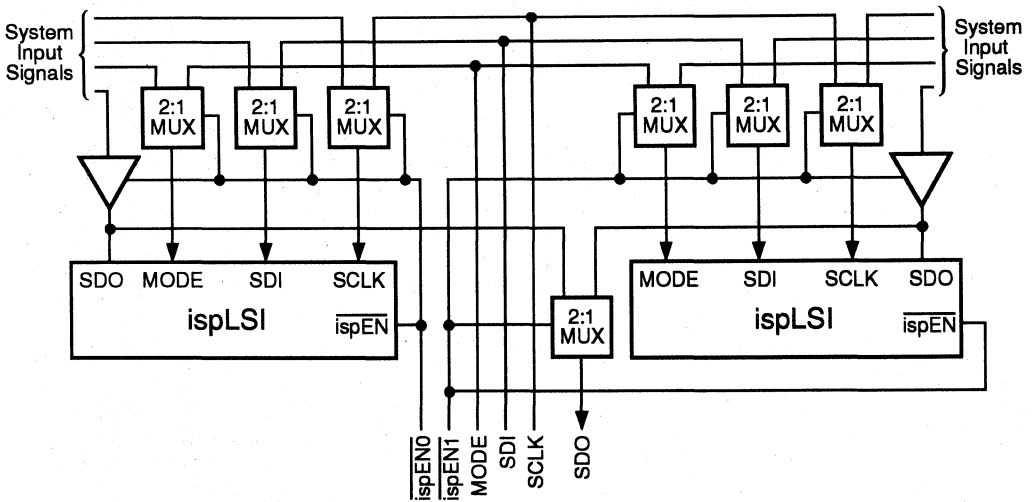
Figure 2-19. The Scan and Multiplex Programming Mode
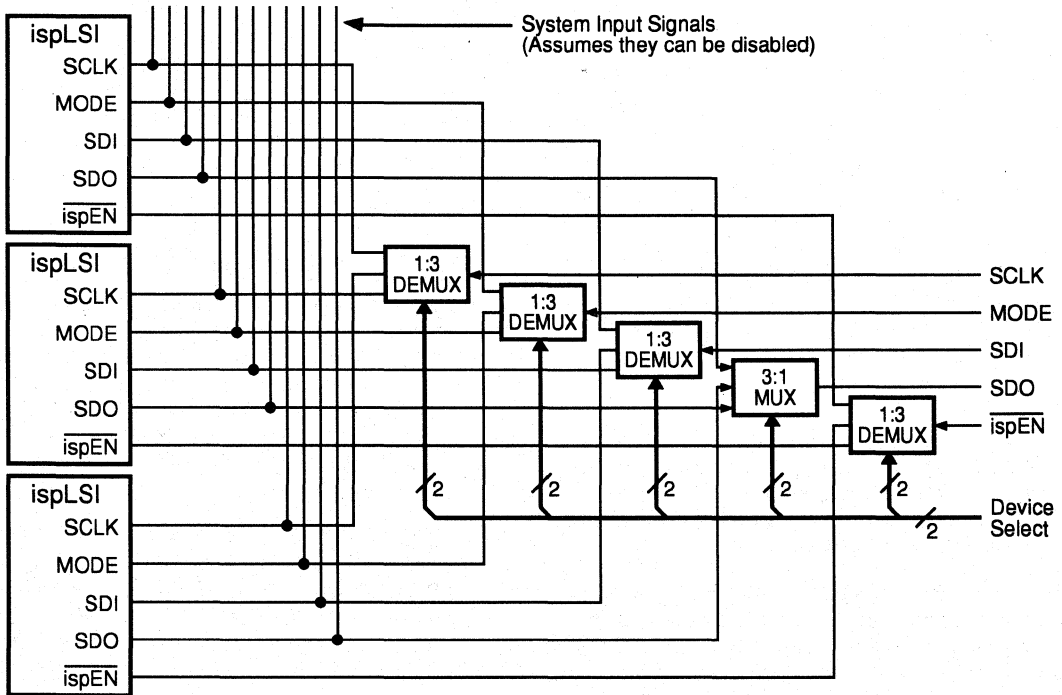
Critical Timing Parameters

When programming the ispLSI devices there are several critical timing parameters that must be met in order to program the devices properly. The most critical of these parameters are the programming pulse width (t_{pwp}) and the bulk erase pulse width (t_{bew}). These pulse widths determine the programming and erasing of the E^2 cells. Figure 2-20 shows these critical program and erase timing specifications.

Along with the two programming and erasing specification, the following timing specifications must also be met.

t_d - Time delay that must elapse between events. It is the time delay from the termination of the previous event.

t_{isp} - Specifies the time it takes to get into the isp mode after $\overline{ispEN}$ signal is activated or the time it takes to come out from the isp mode after the $\overline{ispEN}$ becomes inactive.

t_{su} - Set up time of the control signals before the SCLK or the set up time of input signals against other control signal where applicable.

t_h - Hold time of the control signal after the SCLK. It also applies to the same input signals from the set up time.

t_{clkl}, - Minimum clock pulse width.
t_{clkh}

t_{pwv} - Verify or read pulse width. The minimum time requirement from the rising clock edge of verify/load instruction execution to the next rising clock edge (see figure 2-20).

t_{rst} - Power on reset timing requirement. t_{rst} must elapse after power up before any operations are performed on the device.

All the programming timing parameters are summarized in the timing diagram (see figure 2-21).

Figure 2-20. Program, Verify & Bulk Erase Timing
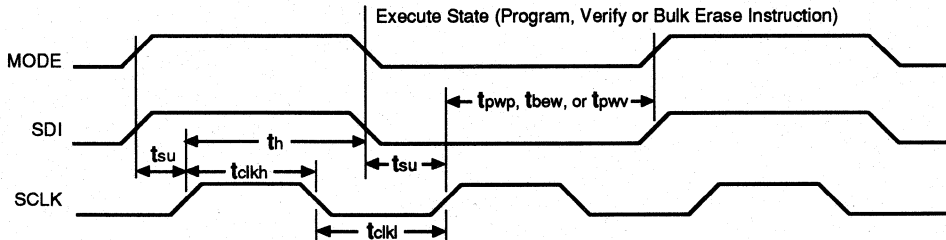
Figure 2-21. isp Programming Timing Requirements
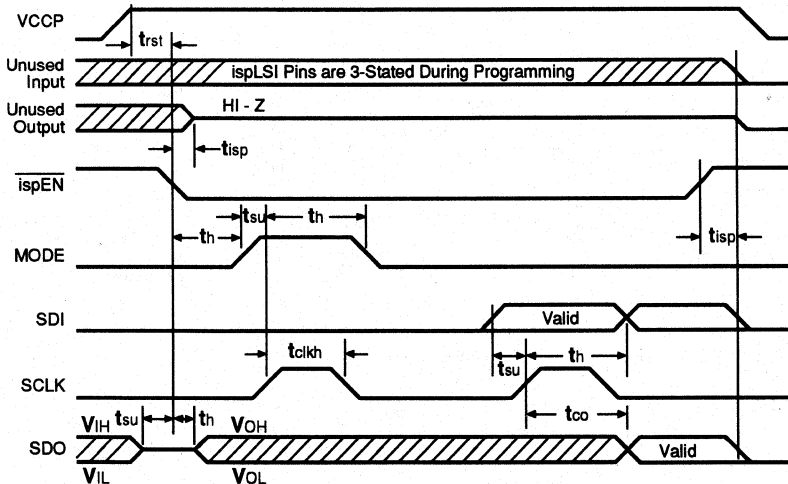
pLSI and ispLSI Architectural Description

Figure 2-22. Programming State Machine

Note:
Control signals: MODE, SDI
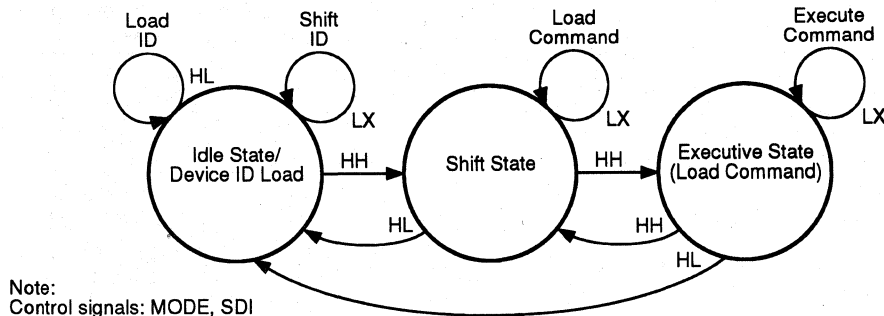
State Machine Operation

The state machine has three states to control the programming and uses the MODE and SDI as inputs for each state. Based on these input signals, each of the three states make decisions to either stay in the same state or to branch to another state. The three states are Idle/ID State, Command Shift State and Execute State. The programming state machine diagram in figure 2-22 shows the three states and the status of the control signals in each state for indicated operation.

Idle/ID State

The Idle/ID state is the first state which is active when the device gets into the Edit Mode. The state machine is in the Idle/ID state when the device is idle, in the Edit Mode, or when the user needs to read the device identification. The eight bit device identification is loaded into the shift register by driving MODE high, SDI low and clocking the state machine with SCLK. Once the ID is loaded, it is read out serially by driving MODE low. Notice that when reading the device ID serially, SDI can either be high or low (don't care) and the state machine needs only seven clocks to read out eight bits of ID. The default state for the control signals is MODE high and SDI low. State transition to Command Shift State occurs when both MODE and SDI are high while state machine gets a clock transition. Table 2-3 lists the eight bit device ID's for all the ispLSI devices. As with most shift registers the Least Significant Bit (LSB) of the ID gets shifted out from the SDO first.

Command Shift State

This state is strictly used for shifting in the command instructions into the state machine. The entire five-bit instruction set is listed in the next section. When MODE is low and SDI is don't care in the Command Shift State,

Table 2-3. IspLSI Device ID Codes

Device	MSB LSB
ispLSI 1016	00000001
ispLSI 1024	00000010
ispLSI 1032	00000011
ispLSI 1048	00000100

SCLK shifts the instruction into the state machine. Once the instruction is shifted into the state machine, the state machine must transition to the Execute State to execute the instruction. Driving both MODE and SDI high and applying the clock will transfer the state machine from Command Shift State to Execute State. If needed, the state machine can move from Command Shift State to Idle/ID State by driving MODE high and SDI low.

Execute State

In the Execute State, the state machine executes instructions that are loaded into the device in the Command Shift State. For some instructions, the state machine requires more than one clock to execute the command. An example of this multiple clock requirement is the address or data shift instruction. The number of clock pulses required for these instructions depends on the device shift register sizes (refer to the isp programming section of the data sheet). When executing instructions such as Program, Verify or Bulk Erase, the necessary timing requirements must be followed to make sure that the commands are executed properly. For specific timing information refer to the individual data sheets.

To execute a command, the MODE is driven low and SDI is don't care. For multiple clock instructions the control signals must remain in the same state throughout the

duration of the execution. MODE high and SDI high will take the state machine back to the Command Shift State and MODE high and SDI low will take the state machine to the Idle/ID State.

Instructions

Table 2-4 lists the instructions that can be loaded into the state machine in the Command Shift State and then executed in the Execute State. Notice that reading the device identification is done during the Idle/ID State and does not require an instruction.

Table 2-4. State Machine Instruction Set

Instruction	Operation	Description
00000	NOP	No operation performed.
00001	ADDSHIFT	Address Register Shift: Shift address into the address shift register from SDI.
00010	DATASHIFT	Data Register Shift: Shifts data into or out of the data serial register.
00011	UBE	User Bulk Erase: Erase the entire device.
00100	GRPBE	Global Routing Pool Bulk Erase: Bulk erases the GRP array only.
00101	GLBBE	Generic Logic Block Bulk Erase: Bulk erases all the GLB array only.
00110	ARCHBE	Architecture Bulk Erase: Bulk erases the architecture array and I/O configuration only.
00111	PRGMH	Program High Order Bits: The data in the shift register is programmed into the addressed row's high order bits.
01000	PRGML	Program Low Order Bits: The data in the data shift register is programmed into the addressed row's low order bits.
01001	PRGMSC	Program Security Cell: Programs the security cell of the device.
01010	VER/LDH	Verify/Load High Order Bits: Load the data from the selected row's high order bits into the data shift register for programmed verification.
01011	VER/LDL	Verify/Load Low Order Bits: Load the data from the selected row's low order bits into the data shift register for programmed verification.
01110	FLOWTHRU	Flow Through: Bypasses all the internal shift registers and SDO becomes the same as SDI.
10010	VE/LDH	Verify Erase/Load High Order Bits: Load the data from the selected row's high order bits into the data shift register for erased verification.
10011	VE/LDL	Verify Erase/Load Low Order Bits: Load the data from the selected row's low order bits into the data shift register for erased verification.

pLSI and ispLSI Architectural Description

While it is possible to erase the individual arrays of the device, it is recommended that the entire device be erased (User Bulk Erase) and programmed in one operation. This Bulk Erase operation should precede every programming cycle as an initialization.

When a device is secured by programming the security cell (PRGMSC), the on-chip verify and load circuitry is disabled. Securing of the device should be done as the last procedure after all the device verifications have been completed. The only way to erase the security cell is to perform a bulk erase on the device.

Device Layout

The purpose of knowing the device layout is to be able to translate the JEDEC format programming file into the serial data stream format for programming ispLSI devices. Two main factors determine how the translation is implemented. The length of the address shift register and the length of the data shift register. The length of the address shift register indicates how many rows of data are to be programmed into the device. The length of the data shift register indicates how many bits are to be programmed in each row. Both registers operate on the First In First Out (FIFO) basis where the Least Significant Bit (LSB) of the data or address is shifted in first and the Most Significant Bit (MSB) of the data or address is shifted in last. For the data shift register, the low order bits and the high order bits are separately shifted.

Figure 2-23 on page 2-21 illustrates the general layout of all the ispLSI devices. Between all ispLSI devices there are exactly the same number of rows for the I/O and architecture array as there are for the GLB array. The GRP array size is proportional to the size of the device. According to the size of the GRP array, the size of the address shift register is adjusted for different devices. Tables 2-5 and 2-6 summarize the array and shift register sizes for all ispLSI devices.

Using ispLSI 1032 as a specific example the transition from a JEDEC format programming file to the ispLSI device format is illustrated below. The JEDEC format programming file for the ispLSI 1032 is organized as follows:

L00000	01010101....	....010101010*
L00040	11111111....	....111111111*
L00080	00000000....	....000000000*
L00120	11111111....	....111111111*
L00160	01010101....	....010101010*

•

•

•

The L field in the JEDEC programming file indicates the first cell number of each row. The JEDEC standard requires that there is at least the beginning cell number L00000. L fields of the subsequent lines are optional. From this reference cell location all other cell locations can be determined. Zero in the cell location indicates that the E^2 cell in that particular location is programmed (or has a logic connection equivalent to a metal fuse being intact). A one (1) in the cell location indicates that the cell is erased (equivalent to a blown fuse). The successful operation of Fusemap in the Lattice software generates this JEDEC standard programming file. This is also the standard that is widely used in the PLD industry for translating design ideas into the device specific layout for programming.

Table 2-5. Summary of Address Shift Register Rows

Address SR Rows	IspLSI 1016	IspLSI 1024	IspLSI 1032	IspLSI 1048
I/O & Arch. Array	12	12	12	12
GLB Array	72	72	72	72
GRP Array	12	18	24	36
Total Address SR Rows	96	102	108	120

Figure 2-23. ispLSI Device & Shift Register Layout
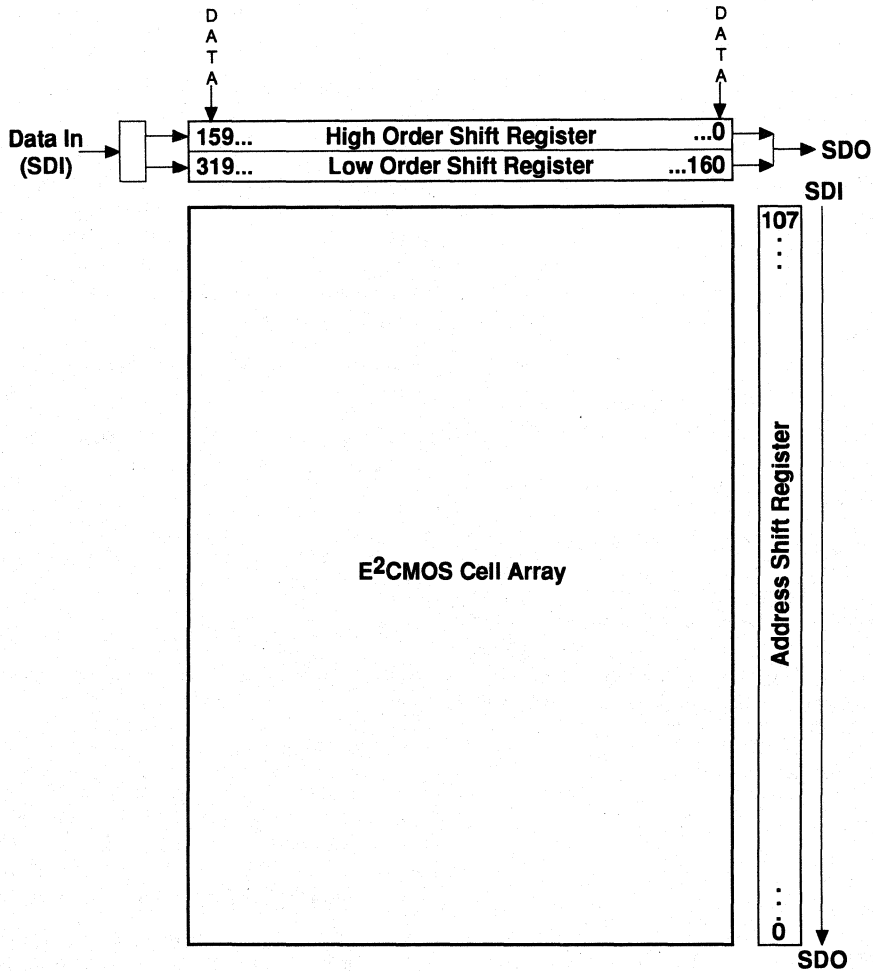
Table 2-6. Summary of Data Shift Register Bits

Data SR Bits	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048
High Order Data SR LSB	0	0	0	0
High Order Data SR MSB	79	119	159	239
Low Order Data SR LSB	80	120	160	240
Low Order Data SR MSB	159	239	319	479
Data SR Size (Bits)	160	240	320	480

Translating the JEDEC programming file into the ispLSI 1032 device format, the layout should be as follows:

		LSB	MSB
Row#	0000 High	L00000....	....L00159
Row#	0000 Low	L00160....	....L00319
Row#	0001 High	L00320....	....L00479
Row#	0001 Low	L00480....	....L00639

•

•

•

The least significant bit of the data shift register matches up with the lowest cell number of the corresponding cells from the JEDEC programming file.

Command Stream

The first step of programming the ispLSI devices is to determine the type of device to be programmed. This can be done by reading the eight-bit device ID of all the devices. By keeping the SDI to a known level (either high or low), the ID shift can be terminated when a sequence of eight ones or eight zeros is read. From the device ID the serial bit stream for programming can be arranged. A typical programming sequence is as follows:

1) ADDSHFT command shift

2) Execute ADDSHFT command

3) Shift address

4) DATASHFT command shift

5) Execute DATASHFT command

6) Shift high order data

7) PRGMH command shift

8) Execute PRGMH

9) DATASHFT command shift

10) Execute DATASHFT command

11) Shift low order data

12) PRGML command shift

13) Execute PRGML

14) Repeat from 1) until all rows are programmed.

Diagnostic Register Preload

This section explains how to preload all of the buried registers and I/O registers to a known state to test the logic function of a device. The process of loading the register will reduce the time necessary to test a function that is deeply into the logic of an ispLSI device.

To preload a device the isp state machine is used with the same five pins that are used for programming ispEN, SDI, MODE, SDO and SCLK. Two state machine commands preload all of the registers: GLBRLD and IOPRLD. These two commands enable two different shift registers and enable data to be loaded into the device. The process of loading data into the device is:

1. Enter the isp programming mode by driving $\overline{ispEN}$ pin to Vil.

2. Load command GLBRLD and execute command (wait one tclk).

3. Clock in the GLB preload data.

4. Load the command IOPRLD and execute the command (wait one tclk).

5. Clock in the I/O preload data.

6. Return to the normal mode by driving the $\overline{ispEN}$ pin to Vih.

7. Execute the vectors.

When preloading a device it is important to keep the dedicated input pins ($\overline{RESET}$, Y0, Y1, Y2 and Y3) in the same state as the previous vector. If the state of these pins is switched during the preload sequence the register may not load correctly and the results cannot be guaranteed.

The preload feature is not recommended on designs which use product term resets. The asynchronous nature of these resets can cause registers to be reset unexpectedly, therefore the results cannot be guaranteed.

There are two shift registers used to preload an ispLSI device, the GLB shift register and the I/O shift register (see table 2-7). The data format for both devices is shown in figure 2-24. The GLB registers are listed with their outputs (i.e. (A7 O0) indicating output 0, of GLB A7).

Table 2-7. Preload Shift Registers

Device	GLB Shift Reg. Length	I/O Shift Reg. Length
ispLSI 1016	64 bits	32 bits
ispLSI 1024	96 bits	48 bits
ispLSI 1032	128 bits	64 bits
ispLSI 1048	192 bits	96 bits

Figure 2-24. GLB Shift Register and I/O Shift Register Format

GLB Shift Register Format

1016 GLB Register Preload Format

Data In (SDI) → (A7 O0) (A7 O1)...(A0 O2) (A0 O3) (B0 O0) (B0 O1)...(B7 O2) (B7 O3) → Data Out (SDO)

1024 GLB Register Preload Format

Data In (SDI) → (B3 O0)...(B0 O3) (A7 O0)...(A0 O3) (B4 O0)...(B7 O3) (C0 O0)...(C7 O3) → Data Out (SDO)

1032 GLB Register Preload Format

Data In (SDI) → (B7 O0)...(B0 O3) (A7 O0)...(A0 O3) (C0 O0)...(C7 O3) (D0 O0)...(D7 O3) → Data Out (SDO)

1048 GLB Register Preload Format

Data In (SDI) → (C7 O0)...(C0 O3) (B7 O0)...(B0 O3) (A7 O0)...(A0 O3) *(continued)*

(continued) (D0 O0)...(D7 O3) (E0 O0)...(E7 O3) (F0 O0)...(F7 O3) → Data Out (SDO)

I/O Shift Register Format

1016 I/O Register Preload Format

Data In (SDI) → (I/O 15) (I/O 14) (I/O 13)...(I/O 1) (I/O 0) (I/O 16) (I/O 17)...(I/O 29) (I/O 30) (I/O 31) → Data Out (SDO)

1024 I/O Register Preload Format

Data In (SDI) → (I/O 23) (I/O 22) (I/O 21)...(I/O 1) (I/O 0) (I/O 24) (I/O 25)...(I/O 45) (I/O 46) (I/O 47) → Data Out (SDO)

1032 I/O Register Preload Format

Data In (SDI) → (I/O 31) (I/O 30) (I/O 29)...(I/O 1) (I/O 0) (I/O 32) (I/O 33)...(I/O 61) (I/O 62) (I/O 63) → Data Out (SDO)

1048 I/O Register Preload Format

Data In (SDI) → (I/O 47) (I/O 46) (I/O 45)...(I/O 1) (I/O 0) (I/O 48) (I/O 49)...(I/O 93) (I/O 94) (I/O 95) → Data Out (SDO)

pLSI and ispLSI Architectural Description

Diagnostics Using ispLSI Devices

A different type of diagnostic feature takes advantage of the in-system programmability. For diagnostics, the ispLSI devices can be programmed with the test functions in diagnostic mode. When the diagnostic is complete, the ispLSI devices can then be reprogrammed with the functional pattern.

Programming Tools

To support use of the ispLSI devices Lattice provides some sample C language routines which are available on the Lattice Bulletin Board System (BBS): (408)-980-9814. Included are sample routines of:

❏ Programming a Device.

❏ Verifying a Device.

❏ Reading a Device.

❏ Securing a Device.

❏ Bulk Erasing a Device.

These routines are provided to guide development of custom ispLSI drivers for individual applications.

Section 1: Introduction to pLSI and ispLSI
Section 2: pLSI and ispLSI Architectural Description
Section 3: pLSI Data Sheets

Section 4: ispLSI Data Sheets
Section 5: Military pLSI and ispLSI Data Sheets
Section 6: General Information

3

▦▦Lattice

pLSI™ 1016

programmable Large Scale Integration
High-Density Programmable Logic

Features

• **PROGRAMMABLE HIGH-DENSITY LOGIC**
  — Member of Lattice's pLSI Family
  — High-Speed Global Interconnects
  — 32 I/O Pins, Four Dedicated Inputs
  — 96 Registers
  — Wide Input Gating for Fast Counters, State
     Machines, Address Decoders, etc.
  — Small Logic Block Size for Random Logic
  — Security Cell Prevents Unauthorized Copying
• **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  — f_{max} = 90 MHz Maximum Operating Frequency
  — t_{pd} = 12 ns Propagation Delay
  — TTL Compatible Inputs and Outputs
  — Electrically Erasable and Re-Programmable
  — 100% Tested
• **COMBINES EASE OF USE AND THE FAST SYSTEM
  SPEED OF PLDs WITH THE DENSITY AND FLEX-
  IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  — Complete Programmable Device can Combine Glue
     Logic and Structured Designs
  — 100% Routable with High Utilization
  — Three Dedicated Clock Input Pins
  — Synchronous and Asynchronous Clocks
  — Flexible Pin Placement
  — Optimized Global Routing Pool Allows Global
     Interconnectivity
• **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
    — Easy to Use PC Windows™ Interface
    — Boolean Logic Compiler
    — Manual Partitioning
    — Automatic Place and Route
    — Static Timing Table

  pDS+™ Software
    — Industry Standard, Third Party Design
       Environments
    — Schematic Capture, State Machine, VHDL
    — Automatic Partitioning
    — Automatic Place and Route
    — Comprehensive Logic and Timing Simulation
    — PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice pLSI 1016 is a High-Density Programmable
Logic Device which contains 96 Registers, 32 Universal
I/O pins, four Dedicated Input pins, three Dedicated Clock
Input pins and a Global Routing Pool (GRP). The GRP
provides complete interconnectivity between all of these
elements.

The basic unit of logic on the pLSI 1016 device is the
Generic Logic Block (GLB). The GLBs are labeled A0,
A1 ..B7, (see figure 1). There are a total of 16 GLBs in the
pLSI 1016 device. Each GLB has 18 inputs, a program-
mable AND/OR/XOR array, and four outputs which can be
configured to be either combinatorial or registered. Inputs
to the GLB come from the GRP and dedicated inputs. All
of the GLB outputs are brought back into the GRP so that
they can be connected to the inputs of any other GLB on the
device.

Functional Block Diagram

Figure 1. pLSI 1016 Functional Block Diagram
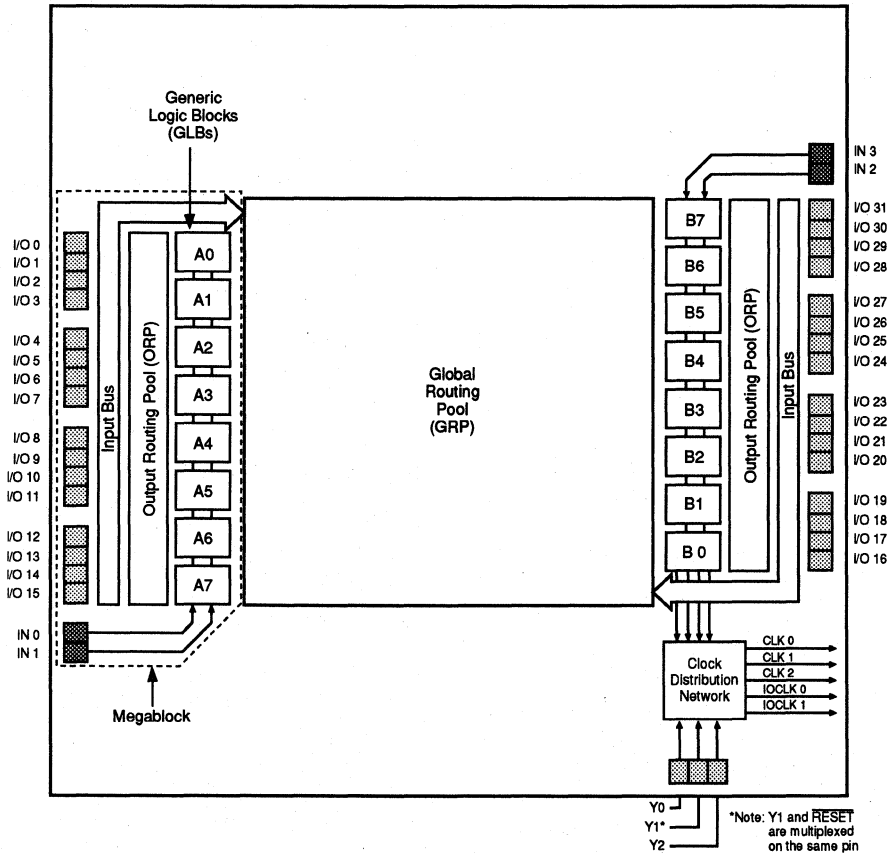
The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI 1016 device contains two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI 1016 device are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the pLSI 1016 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 125°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	$T_A = $ 0°C to +70°C	4.75	5.25	V
		Industrial	$T_A = $ -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

$^*C_L$ includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$		–	–	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	100	150	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	100	170	mA

1. One output at a time for a maximum duration of one second.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90 MIN.	-90 MAX.	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	–	15	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	17	–	20	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	90.9	–	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	58.8	–	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	–	7	–	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	8	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	9	–	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	10	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	15	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	15	–	18	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	15	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	6.5	–	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t$_{iobp}$	20	I/O Register Bypass	–	1.0	–	2.0	–	2.7	ns
t$_{iolat}$	21	I/O Latch Delay	–	2.0	–	3.0	–	4.0	ns
t$_{iosu}$	22	I/O Register Setup Time before Clock	4.5	–	5.5	–	7.3	–	ns
t$_{ioh}$	23	I/O Register Hold Time after Clock	2.0	–	1.0	–	1.3	–	ns
t$_{ioco}$	24	I/O Register Clock to Out Delay	–	2.0	–	3.0	–	4.0	ns
t$_{ior}$	25	I/O Register Reset to Out Delay	–	2.5	–	2.5	–	3.3	ns
t$_{din}$	26	Dedicated Input Delay	–	2.0	–	4.0	–	5.3	ns
GRP									
t$_{grp1}$	27	GRP Delay, 1 GLB Load	–	0.7	–	1.5	–	2.0	ns
t$_{grp4}$	28	GRP Delay, 4 GLB Loads	–	1.0	–	2.0	–	2.7	ns
t$_{grp8}$	29	GRP Delay, 8 GLB Loads	–	1.8	–	3.0	–	4.0	ns
t$_{grp12}$	30	GRP Delay, 12 GLB Loads	–	2.6	–	3.8	–	5.0	ns
t$_{grp16}$	31	GRP Delay, 16 GLB Loads	–	3.4	–	4.5	–	6.0	ns
GLB									
t$_{4ptbp}$	33	4 Product Term Bypass Path Delay	–	6.5	–	6.5	–	8.6	ns
t$_{1ptxor}$	34	1 Product Term/XOR Path Delay	–	7.0	–	7.0	–	9.3	ns
t$_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	8.0	–	10.6	ns
t$_{xoradj}$	36	XOR Adjacent Path Delay[3]	–	9.5	–	9.5	–	12.7	ns
t$_{gbp}$	37	GLB Register Bypass Delay	–	0.5	–	1.0	–	1.3	ns
t$_{gsu}$	38	GLB Register Setup Time before Clock	1.0	–	1.0	–	1.3	–	ns
t$_{gh}$	39	GLB Register Hold Time after Clock	3.5	–	4.5	–	6.0	–	ns
t$_{gco}$	40	GLB Register Clock to Output Delay	–	1.5	–	2.0	–	2.7	ns
t$_{gr}$	41	GLB Register Reset to Output Delay	–	2.5	–	2.5	–	3.3	ns
t$_{ptre}$	42	GLB Product Term Reset to Register Delay	–	10.0	–	10.0	–	13.3	ns
t$_{ptoe}$	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	9.0	–	12.0	ns
t$_{ptck}$	44	GLB Product Term Clock Delay	3.5	7.5	3.5	7.5	4.6	9.9	ns
ORP									
t$_{orp}$	45	ORP Delay	–	2.5	–	2.5	–	3.3	ns
t$_{orpbp}$	46	ORP Bypass Delay	–	0.5	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90 MIN.	-90 MAX.	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
Outputs									
tob	47	Output Buffer Delay	–	2.5	–	3.0	–	4.0	ns
toen	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
todis	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
tgy0	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.5	3.5	4.5	4.5	6.0	6.0	ns
tgy1/2	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.5	4.5	3.5	5.5	4.6	7.3	ns
tgcp	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.0	5.0	1.3	6.6	ns
tioy1/2	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	2.5	4.5	3.5	5.5	4.6	7.3	ns
tiocp	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.0	5.0	1.3	6.6	ns
Global Reset									
tgr	55	Global Reset to GLB and I/O Registers	–	7.5	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

3

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1016 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

8.0 ns = (1.0 + 1.0 + 8.0) + (3.5) - (1.0 + 1.0 + 3.5)

th = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

2.5 ns = (1.0 + 1.0 + 7.5) + (3.0) - (1.0 + 1.0 + 8.0)

tco = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

16.0 ns = (1.0 + 1.0 + 7.5) + (2.0) + (2.5 + 2.0)

Derivations of tsu, th and tco from the Clock GLB[1]

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.0 ns = (1.0 + 1.0 + 8.0) + (3.5) - (3.5 + 2.0 + 1.0)

th = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

3.5 ns = (3.5 + 2.0 + 5.0) + (3.0) - (1.0 + 1.0 + 8.0)

tco = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

17.0 ns = (3.5 + 2.0 + 5.0) + (2.0) + (2.5 + 2.0)

1. Calculations are based upon timing specs for the pLSI 1016-90.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 3	14, 24, 36, 2	Dedicated input pins to the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	This pin performs two functions: – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y2	33	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell in the device.
NC	13	This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND **V**CC	1, 23 12, 34	Ground (GND) V_{cc}

3

Pin Configuration

pLSI 1016 PLCC Pinout Diagram
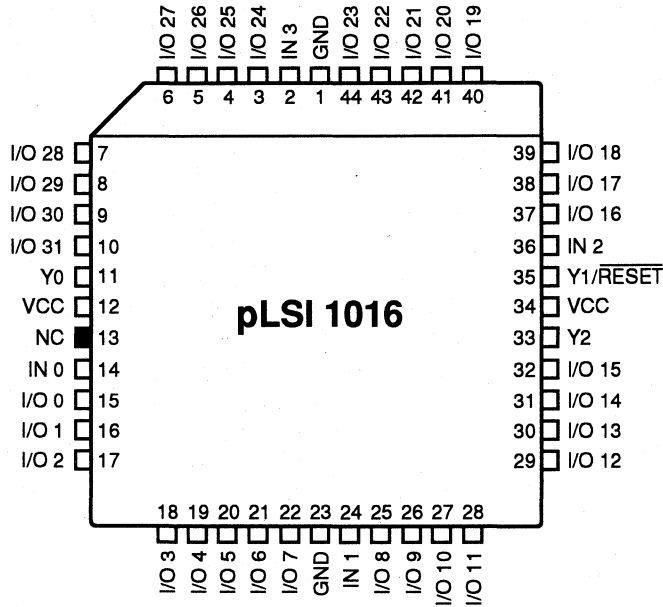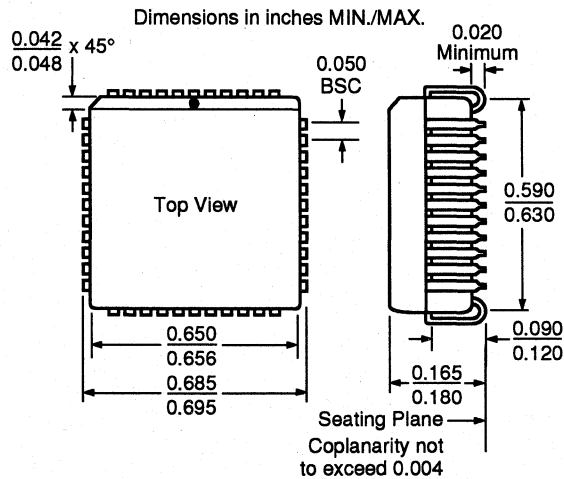
Package Diagram

44-Pin PLCC

Dimensions in inches MIN./MAX.

Part Number Description

pLSI 1016 – XX X X X

Device Family ──────────┘

Device Number ──────────────┘

Speed ──────────────────────────┘
90 = 90 MHz **f**max
80 = 80 MHz **f**max
60 = 60 MHz **f**max

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low
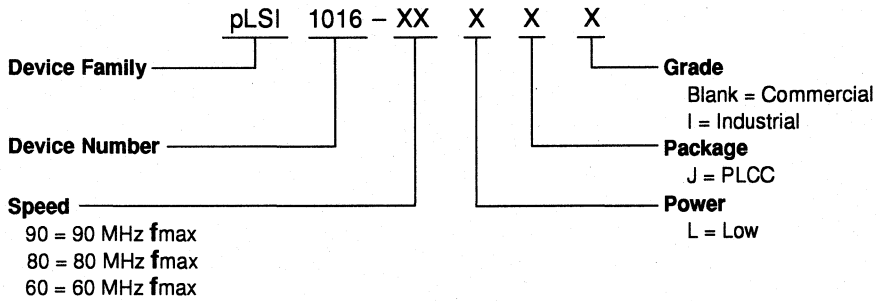
Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
90	12	pLSI 1016-90LJ	44-Pin PLCC
80	15	pLSI 1016-80LJ	44-Pin PLCC
60	20	pLSI 1016-60LJ	44-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1016-60LJI	44-Pin PLCC

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pLSI™ 1024

programmable Large Scale Integration
High-Density Programmable Logic

3

Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**

  — **Member of Lattice's pLSI Family**
  — **High-Speed Global Interconnects**
  — **48 I/O Pins, Six Dedicated Inputs**
  — **144 Registers**
  — **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  — **Small Logic Block Size for Random Logic**
  — **Security Cell Prevents Unauthorized Copying**

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**

  — **$f$max = 80 MHz Maximum Operating Frequency**
  — **$t$pd = 15 ns Propagation Delay**
  — **TTL Compatible Inputs and Outputs**
  — **Electrically Erasable and Re-Programmable**
  — **100% Tested**

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**

  — **Complete Programmable Device can Combine Glue Logic and Structured Designs**
  — **100% Routable with High Utilization**
  — **Four Dedicated Clock Input Pins**
  — **Synchronous and Asynchronous Clocks**
  — **Flexible Pin Placement**
  — **Optimized Global Routing Pool Allows Global Interconnectivity**

- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software

    — **Easy to Use PC Windows™ Interface**
    — **Boolean Logic Compiler**
    — **Manual Partitioning**
    — **Automatic Place and Route**
    — **Static Timing Table**

  pDS+™ Software

    — **Industry Standard, Third Party Design Environments**
    — **Schematic Capture, State Machine, VHDL**
    — **Automatic Partitioning**
    — **Automatic Place and Route**
    — **Comprehensive Logic and Timing Simulation**
    — **PC and Workstation Platforms**

Functional Block Diagram

Description

The Lattice pLSI 1024 is a High-Density Programmable Logic Device which contains 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1024 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..C7, (see figure 1). There are a total of 24 GLBs in the pLSI 1024 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated pins. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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Functional Block Diagram

Figure 1. pLSI 1024 Functional Block Diagram

The device also has 48 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also shares a common Output Enable (OE) signal. The pLSI 1024 device contains three of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI 1024 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B4 on the pLSI 1024 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

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Absolute Maximum Ratings [1]

Supply Voltage V_{cc}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 125°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

3

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}		–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	130	190	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	130	215	mA

1. One output at a time for a maximum duration of one second.
2. Measured using six 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

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Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t$_{iobp}$	20	I/O Register Bypass	–	2.0	–	2.7	ns
t$_{iolat}$	21	I/O Latch Delay	–	3.0	–	4.0	ns
t$_{iosu}$	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t$_{ioh}$	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t$_{ioco}$	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t$_{ior}$	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t$_{din}$	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t$_{grp1}$	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t$_{grp4}$	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t$_{grp8}$	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t$_{grp12}$	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t$_{grp16}$	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
t$_{grp24}$	32	GRP Delay, 24 GLB Loads	–	6.3	–	8.3	ns
GLB							
t$_{4ptbp}$	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t$_{1ptxor}$	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
t$_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t$_{xoradj}$	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t$_{gbp}$	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t$_{gsu}$	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t$_{gh}$	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t$_{gco}$	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t$_{gr}$	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t$_{ptre}$	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t$_{ptoe}$	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t$_{ptck}$	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t$_{orp}$	45	ORP Delay	–	2.5	–	3.3	ns
t$_{orpbp}$	46	ORP Bypass Delay	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t$_{iobp}$	20	I/O Register Bypass	—	2.7	ns
t$_{iolat}$	21	I/O Latch Delay	—	4.0	ns
t$_{iosu}$	22	I/O Register Setup Time before Clock	7.3	—	ns
t$_{ioh}$	23	I/O Register Hold Time after Clock	1.3	—	ns
t$_{ioco}$	24	I/O Register Clock to Out Delay	—	4.0	ns
t$_{ior}$	25	I/O Register Reset to Out Delay	—	3.3	ns
t$_{din}$	26	Dedicated Input Delay	—	5.3	ns
GRP					
t$_{grp1}$	27	GRP Delay, 1 GLB Load	—	2.0	ns
t$_{grp4}$	28	GRP Delay, 4 GLB Loads	—	2.7	ns
t$_{grp8}$	29	GRP Delay, 8 GLB Loads	—	4.0	ns
t$_{grp12}$	30	GRP Delay, 12 GLB Loads	—	5.0	ns
t$_{grp16}$	31	GRP Delay, 16 GLB Loads	—	6.0	ns
t$_{grp24}$	32	GRP Delay, 24 GLB Loads	—	8.3	ns
GLB					
t$_{4ptbp}$	33	4 Product Term Bypass Path Delay	—	8.6	ns
t$_{1ptxor}$	34	1 Product Term/XOR Path Delay	—	9.3	ns
t$_{20ptxor}$	35	20 Product Term/XOR Path Delay	—	10.6	ns
t$_{xoradj}$	36	XOR Adjacent Path Delay[3]	—	12.7	ns
t$_{gbp}$	37	GLB Register Bypass Delay	—	1.3	ns
t$_{gsu}$	38	GLB Register Setup Time before Clock	1.3	—	ns
t$_{gh}$	39	GLB Register Hold Time after Clock	6.0	—	ns
t$_{gco}$	40	GLB Register Clock to Output Delay	—	2.7	ns
t$_{gr}$	41	GLB Register Reset to Output Delay	—	3.3	ns
t$_{ptre}$	42	GLB Product Term Reset to Register Delay	—	13.3	ns
t$_{ptoe}$	43	GLB Product Term Output Enable to I/O Cell Delay	—	12.0	ns
t$_{ptck}$	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t$_{orp}$	45	ORP Delay	—	3.3	ns
t$_{orpbp}$	46	ORP Bypass Delay	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1024 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su}
= Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(min))$
= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$
5.5 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)$

t_h
= Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$
4.0 ns = $(2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co}
= Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
19.0 ns = $(2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su}
= Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0}(min) + t_{gco} + t_{gcp}(min))$
= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$
7.0 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (3.0 + 2.0 + 1.0)$

t_h
= Clock (max) + Reg h - Logic
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$
2.5 ns = $(3.0 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co}
= Clock (max) + Reg co + Output
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$
17.5 ns = $(3.0 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)$

1. Calculations are based upon timing specs for the pLSI 1024-80.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Six 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

Pin Description

Name	PLCC Pin Numbers				Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47	22, 26, 30, 37, 41, 45, 56, 60, 64, 3, 7, 11,	23, 27, 31, 38, 42, 46, 57, 61, 65, 4, 8, 12,	24, 28, 32, 39, 43, 47, 58, 62, 66, 5, 9, 13,	25, 29, 33, 40, 44, 48, 59, 63, 67, 6, 10, 14	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 3 IN 4 - IN 5	21, 2,	34, 15	49,	55,	Dedicated input pins to the device.
$\overline{\text{RESET}}$	20				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	19				This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND **V**CC	1, 17,	18, 36,	35, 53,	52 68	Ground (GND) V_{cc}

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Pin Configuration

pLSI 1024 PLCC Pinout Diagram

Top pins (left to right): I/O 42, I/O 41, I/O 40, I/O 39, I/O 38, I/O 37, I/O 36, IN 4, GND, VCC, I/O 35, I/O 34, I/O 33, I/O 32, I/O 31, I/O 30, I/O 29

Top pin numbers: 9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61

Left side:
I/O 43	10
I/O 44	11
I/O 45	12
I/O 46	13
I/O 47	14
IN 5	15
Y0	16
VCC	17
GND	18
NC	19
RESET	20
IN 0	21
I/O 0	22
I/O 1	23
I/O 2	24
I/O 3	25
I/O 4	26

pLSI 1024

Right side:
60	I/O 28
59	I/O 27
58	I/O 26
57	I/O 25
56	I/O 24
55	IN 3
54	Y1
53	VCC
52	GND
51	Y2
50	Y3
49	IN 2
48	I/O 23
47	I/O 22
46	I/O 21
45	I/O 20
44	I/O 19

Bottom pin numbers: 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

Bottom pins (left to right): I/O 5, I/O 6, I/O 7, I/O 8, I/O 9, I/O 10, I/O 11, IN 1, GND, VCC, I/O 12, I/O 13, I/O 14, I/O 15, I/O 16, I/O 17, I/O 18

Package Diagram

68-Pin PLCC

Dimensions in inches MIN./MAX.

$\dfrac{0.042}{0.048}$ x 45°

0.050 BSC

0.020 Minimum

Top View

0.890 / 0.930

0.950 / 0.956

0.985 / 0.995

0.090 / 0.120

0.165 / 0.180

Seating Plane
Coplanarity not
to exceed 0.004

Part Number Description

pLSI   1024 – XX   X   X   X

Device Family

Device Number

Speed
80 = 80 MHz fmax
60 = 60 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low

3

Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
80	15	pLSI 1024-80LJ	68-Pin PLCC
60	20	pLSI 1024-60LJ	68-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1024-60LJI	68-Pin PLCC

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pLSI™ *1032*
programmable Large Scale Integration
High-Density Programmable Logic

Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - Member of Lattice's pLSI Family
  - High-Speed Global Interconnects
  - 64 I/O Pins, Eight Dedicated Inputs
  - 192 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Fast Random Logic
  - Security Cell Prevents Unauthorized Copying

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 80 MHz Maximum Operating Frequency
  - t_{pd} = 15 ns Propagation Delay
  - Low Power Consumption
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Re-Programmable
  - 100% Tested

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity

- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice pLSI 1032 is a High-Density Programmable Logic Device which contains 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins, four Output Routing Pools and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7, (see figure 1). There are a total of 32 GLBs in the pLSI 1032 device. Each GLB has 18 inputs, a program-mable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI 1032 Functional Block Diagram

The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also shares a common Output Enable (OE) signal. The pLSI 1032 device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI 1032 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the pLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Lattice

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 125°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V ≤ V_{IN} ≤ V_{IL}$ (MAX.)		–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} ≤ V_{IN} ≤ V_{CC}$		–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V ≤ V_{IN} ≤ V_{IL}$		–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	135	195	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	135	220	mA

1. One output at a time for a maximum duration of one second.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
Inputs							
t_{iobp}	20	I/O Register Bypass	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	8.0	–	10.6	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_{orp}	45	ORP Delay	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

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Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

3

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	# [2]	DESCRIPTION [1]	-60		UNITS
				MIN.	MAX.	
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	—	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback [3]	60	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	38	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle [4]	83	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	—	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	—	13	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	13	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	16	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	—	22.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	13	—	ns
t_{en}	2	14	Input to Output Enable	—	24	ns
t_{dis}	3	15	Input to Output Disable	—	24	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	6	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	6	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	10.6	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1032 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

5.5 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

4.0 ns = $(2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

19.0 ns = $(2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.0 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (3.0 + 2.0 + 1.0)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

2.5 ns = $(3.0 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

17.5 ns = $(3.0 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)$

1. Calculations are based upon timing specs for the pLSI 1032-80.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of eight 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

Pin Description

Name	PLCC Pin Numbers				Description
I/O 0 - I/O 3	26,	27,	28,	29,	Input/Output Pins - These are the general purpose I/O pins used by the
I/O 4 - I/O 7	30,	31,	32,	33,	logic array.
I/O 8 - I/O 11	34,	35,	36,	37,	
I/O 12 - I/O 15	38,	39,	40,	41,	
I/O 16 - I/O 19	45,	46,	47,	48,	
I/O 20 - I/O 23	49,	50,	51,	52,	
I/O 24 - I/O 27	53,	54,	55,	56,	
I/O 28 - I/O 31	57,	58,	59,	60,	
I/O 32 - I/O 35	68,	69,	70,	71,	
I/O 36 - I/O 39	72,	73,	74,	75,	
I/O 40 - I/O 43	76,	77,	78,	79,	
I/O 44 - I/O 47	80,	81,	82,	83,	
I/O 48 - I/O 51	3,	4,	5,	6,	
I/O 52 - I/O 55	7,	8,	9,	10,	
I/O 56 - I/O 59	11,	12,	13,	14,	
I/O 60 - I/O 63	15,	16,	17,	18	
IN 0 - IN 3	25,	42,	44,	61	Dedicated input pins to the device.
IN 4 - IN 7	67,	84,	2,	19	
RESET	24				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	23				This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND	1,	22,	43,	64	Ground (GND)
V_{CC}	21,	65			V_{cc}

3

Pin Configuration

pLSI 1032 PLCC Pinout Diagram
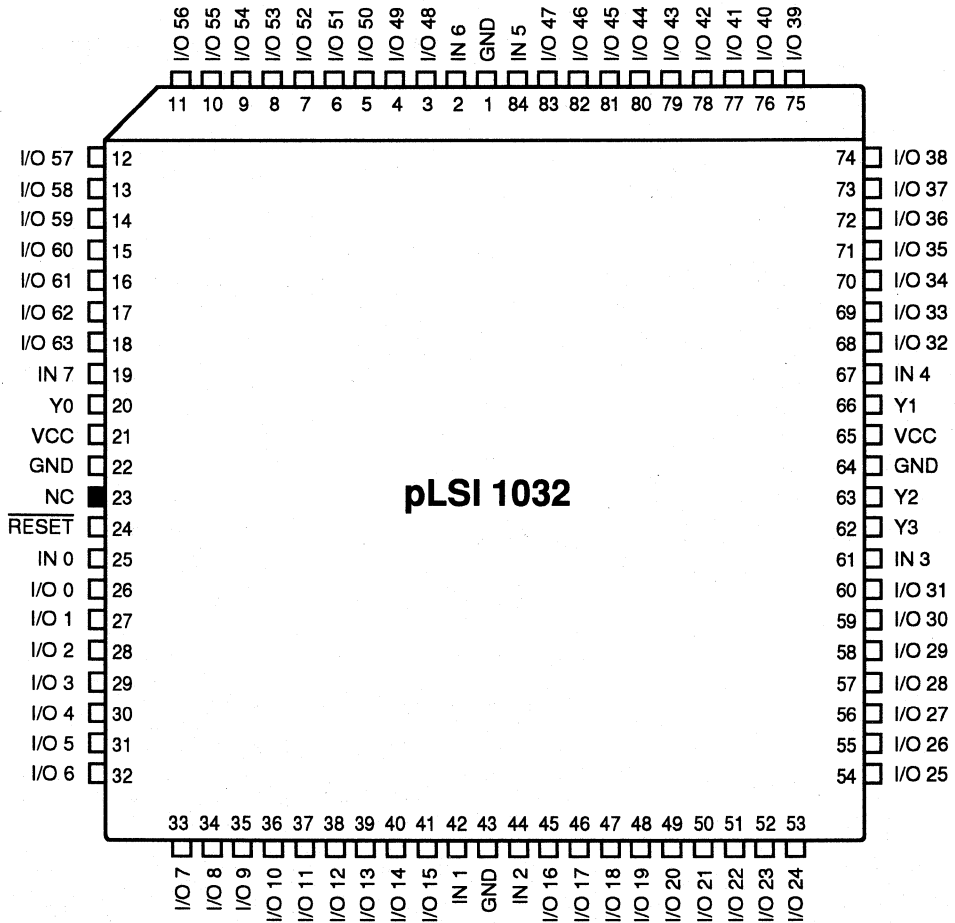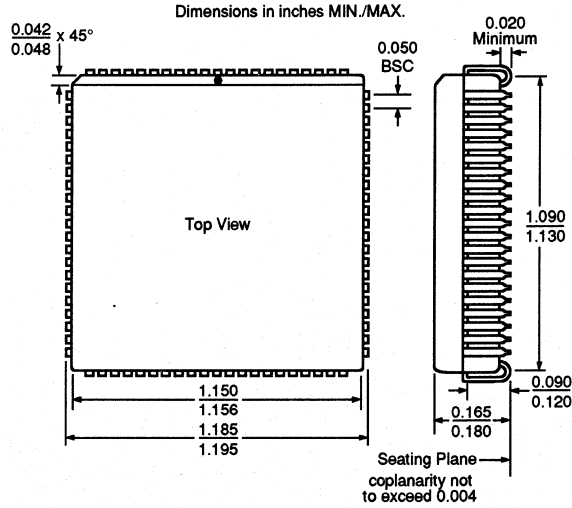
∷Lattice

Specifications *pLSI 1032*

Package Diagram

84-Pin PLCC

Dimensions in inches MIN./MAX.

$\frac{0.042}{0.048}$ x 45°

0.050
BSC

0.020
Minimum

Top View

1.090
1.130

1.150
1.156
1.185
1.195

0.165
0.180

0.090
0.120

Seating Plane
coplanarity not
to exceed 0.004

Part Number Description

pLSI 1032 – XX X X X

Device Family

Device Number

Speed
80 = 80 MHz fmax
60 = 60 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low
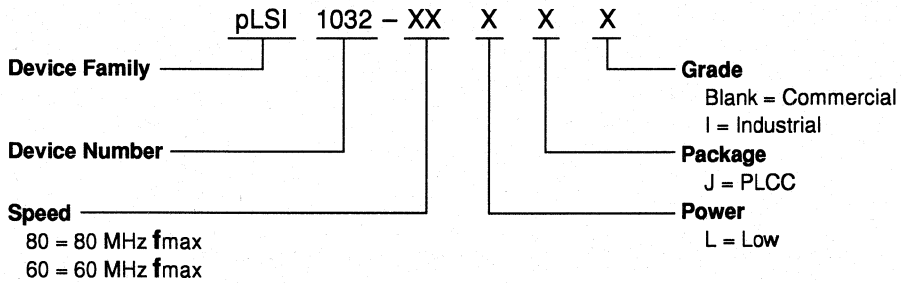
Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
80	15	pLSI 1032-80LJ	84-Pin PLCC
60	20	pLSI 1032-60LJ	84-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1032-60LJI	84-Pin PLCC

⁘Lattice

pLSI™ 1048
programmable Large Scale Integration
High-Density Programmable Logic

Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - **— Member of Lattice's pLSI Family**
  - **— High-Speed Global Interconnects**
  - **— 96 I/O Pins, Ten Dedicated Inputs**
  - **— 288 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— fmax = 70 MHz Maximum Operating Frequency**
  - **— tpd = 18 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Re-Programmable**
  - **— 100% Tested**

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device can Combine Glue Logic and Structured Designs**
  - **— 100% Routable with High Utilization**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Allows Global Interconnectivity**

- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**
  - **pDS Software**
    - **— Easy to Use PC Windows™ Interface**
    - **— Boolean Logic Compiler**
    - **— Manual Partitioning**
    - **— Automatic Place and Route**
    - **— Static Timing Table**

  - **pDS+™ Software**
    - **— Industry Standard, Third Party Design Environments**
    - **— Schematic Capture, State Machine, VHDL**
    - **— Automatic Partitioning**
    - **— Automatic Place and Route**
    - **— Comprehensive Logic and Timing Simulation**
    - **— PC and Workstation Platforms**

Functional Block Diagram

Description

The Lattice pLSI 1048 is a High-Density Programmable Logic Device which contains 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1048 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..F7, (see figure 1). There are a total of 48 GLBs in the pLSI 1048 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI 1048 Functional Block Diagram
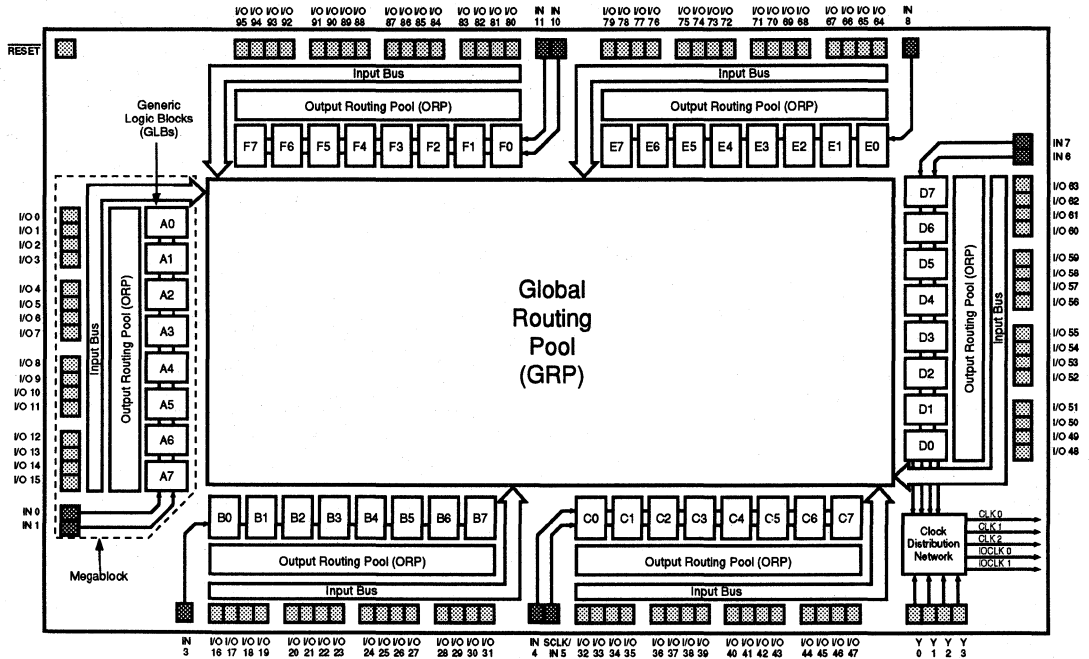
The device also has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs (one dedicated input in Megablock B and E) and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI 1048 device contains six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI 1048 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the pLSI 1048 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 125°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	$T_A = $ 0°C to +70°C	4.75	5.25	V
		Industrial	$T_A = $ -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

$^*C_L$ includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)		–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$		–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$		–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	165	235	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	165	260	mA

1. One output at a time for a maximum duration of one second.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	18	–	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	23	–	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	71.4	–	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	41.7	–	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	12	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	12	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	12	–	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	14	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	20	–	26.7	ns
t_{dis}	3	15	Input to Output Disable	–	20	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

3

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
Inputs							
t_{iobp}	20	I/O Register Bypass	–	3.0	–	4.0	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	–	5.3	ns
t_{iosu}	22	I/O Register Setup Time before Clock	6.0	–	8.1	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	0.5	–	0.9	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	3.9	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.5	–	4.6	ns
t_{din}	26	Dedicated Input Delay	–	6.0	–	8.0	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.5	–	3.3	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	3.0	–	4.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	–	5.3	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	–	6.7	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	–	8.0	ns
t_{grp48}	32	GRP Delay, 48 GLB Loads	–	16.0	–	21.3	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	7.5	–	10.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.5	–	2.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	8.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.5	–	3.3	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	11.9	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_{orp}	45	ORP Delay	–	3.5	–	4.7	ns
t_{orpbp}	46	ORP Bypass Delay	–	1.5	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	5.0	5.0	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.0	6.0	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.0	6.0	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.0	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

3

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	12	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	26.7	ns
t_{dis}	3	15	Input to Output Disable	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50		UNITS
			MIN.	MAX.	
Inputs					
t_{iobp}	20	I/O Register Bypass	–	4.0	ns
t_{iolat}	21	I/O Latch Delay	–	5.3	ns
t_{iosu}	22	I/O Register Setup Time before Clock	8.1	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	0.9	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.9	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	4.6	ns
t_{din}	26	Dedicated Input Delay	–	8.0	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	3.3	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	4.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	5.3	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	6.7	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	8.0	ns
t_{grp48}	32	GRP Delay, 48 GLB Loads	–	21.3	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	2.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	8.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	3.3	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	11.9	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	4.7	ns
t_{orpbp}	46	ORP Bypass Delay	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	—	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	—	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	—	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	—	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1048 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

$$t_{su} = \text{Logic} + \text{Reg su} - \text{Clock (min)}$$
$$= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$$
$$= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$$
$$5.5 \text{ ns} = (3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5)$$

$$t_h = \text{Clock (max)} + \text{Reg h} - \text{Logic}$$
$$= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$$
$$= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$$
$$6.0 \text{ ns} = (3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5)$$

$$t_{co} = \text{Clock (max)} + \text{Reg co} + \text{Output}$$
$$= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$$
$$= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$$
$$22.5 \text{ ns} = (3.0 + 3.0 + 7.5) + (2.5) + (3.5 + 3.0)$$

Derivations of tsu, th and tco from the Clock GLB[1]

$$t_{su} = \text{Logic} + \text{Reg su} - \text{Clock (min)}$$
$$= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$$
$$= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$$
$$6.5 \text{ ns} = (3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0)$$

$$t_h = \text{Clock (max)} + \text{Reg h} - \text{Logic}$$
$$= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$$
$$= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$$
$$5.0 \text{ ns} = (5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5)$$

$$t_{co} = \text{Clock (max)} + \text{Reg co} + \text{Output}$$
$$= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$$
$$= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$$
$$21.5 \text{ ns} = (5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)$$

1. Calculations are based upon timing specs for the pLSI 1048-70.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

Pin Description

Name	PQFP Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99,100,101,102,103, 109,110,111,112,113,114, 115,116,117,118,119,120, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 5 IN 6 - IN 11	14, 44, – 47, 48, 73, 79,104,105, – 108, 13	Dedicated input pins to the device. (IN 2 and IN 9 not available)
RESET	18	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	14	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	78	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	75	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	74	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	17	This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND Vcc	46, 76,106, 16 15, 45, 77, 107	Ground (GND) V_{cc}

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9/92. Rev. E

▦ Lattice

Pin Configuration

pLSI 1048 PQFP Pinout Diagram
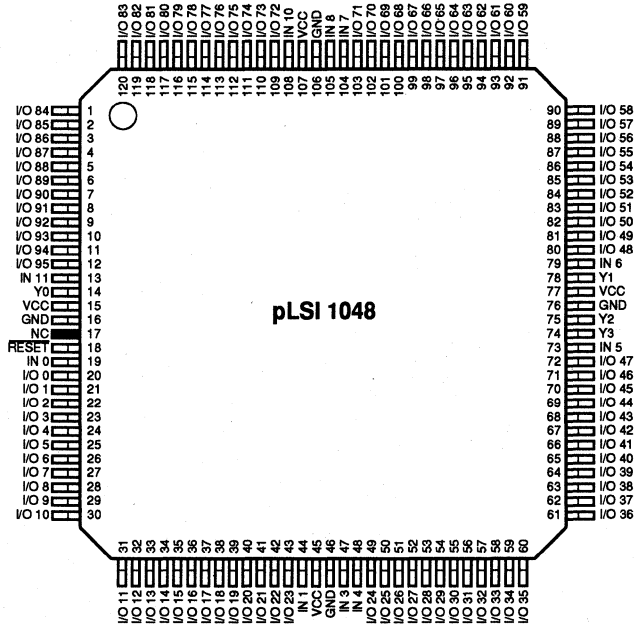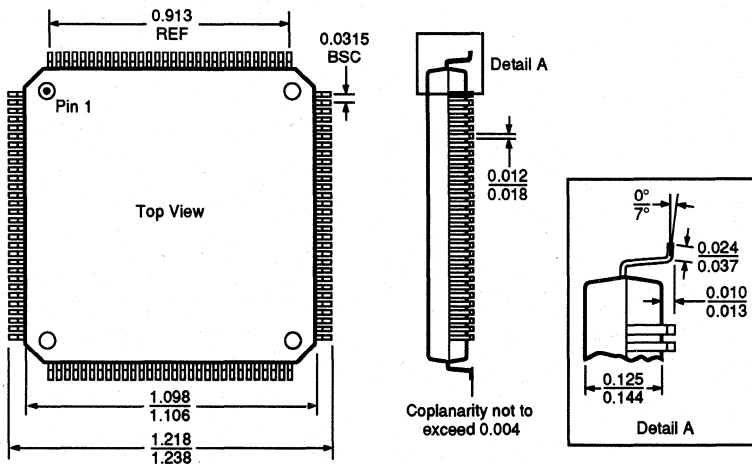
Package Diagram

120-Pin PQFP

Dimensions in inches MIN./MAX.

Coplanarity not to
exceed 0.004

Detail A

Part Number Description

pLSI 1048 – XX X X X

Device Family
Device Number
Speed
70 = 70 MHz fmax
50 = 50 MHz fmax

Grade
Blank = Commercial
I = Industrial
Package
Q = PQFP
Power
L = Low
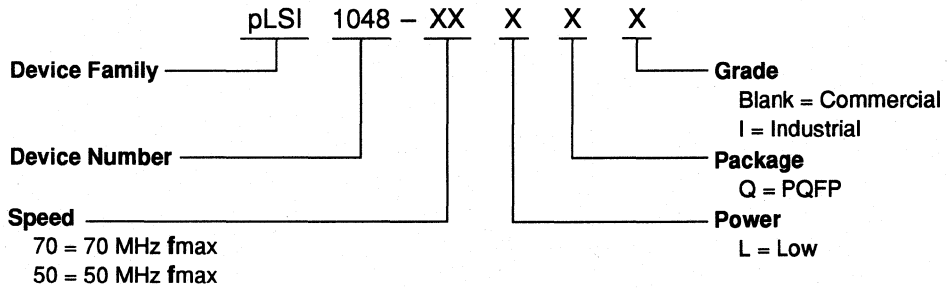
Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
70	18	pLSI 1048-70LQ	120-Pin PQFP
50	24	pLSI 1048-50LQ	120-Pin PQFP

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
50	24	pLSI 1048-50LQI	120-Pin PQFP

Section 1: **Introduction to pLSI and ispLSI**

Section 2: **pLSI and ispLSI Architectural Description**

Section 3: **pLSI Data Sheets**

Section 4: **ispLSI Data Sheets**

Section 5: **Military pLSI and ispLSI Data Sheets**

Section 6: **General Information**

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⁝⁝⁝⁝Lattice

ispLSI™ *1016*

in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - **— Member of Lattice's ispLSI Family**
  - **— Fully Compatible with Lattice's pLSI™ Family**
  - **— High-Speed Global Interconnects**
  - **— 32 I/O Pins, Four Dedicated Inputs**
  - **— 96 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— fmax = 90 MHz Maximum Operating Frequency**
  - **— tpd = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - **— Change Logic and Interconnects "on-the-fly" in Seconds**
  - **— Reprogram Soldered Device for Debugging**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED of PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device can Combine Glue Logic and Structured Designs**
  - **— 100% Routable with High Utilization**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Allows Global Interconnectivity**
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**
  - **pDS Software**
    - **— Easy to Use PC Windows™ Interface**
    - **— Boolean Logic Compiler**
    - **— Manual Partitioning**
    - **— Automatic Place and Route**
    - **— Static Timing Table**
  - **pDS+™ Software**
    - **— Industry Standard, Third Party Design Environments**
    - **— Schematic Capture, State Machine, VHDL**
    - **— Automatic Partitioning**
    - **— Automatic Place and Route**
    - **— Comprehensive Logic and Timing Simulation**
    - **— PC and Workstation Platforms**

Functional Block Diagram

Description

The Lattice ispLSI 1016 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1016 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see figure 1). There are a total of 16 GLBs in the ispLSI 1016 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 1016 Functional Block Diagram

The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI 1016 device contains two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1016 device are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the ispLSI 1016 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 125°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

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DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V ≤ V_{IN} ≤ V_{IL}$ (MAX.)		–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} ≤ V_{IN} ≤ V_{CC}$		–	–	10	μA
I_{IL-isp}	isp Input Low Leakage Current	$0V ≤ V_{IN} ≤ V_{IL}$ (MAX.)		–	–	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V ≤ V_{IN} ≤ V_{IL}$		–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	100	150	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	100	170	mA

1. One output at a time for a maximum duration of one second.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

Lattice

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	#[2]	DESCRIPTION[1]	-90 MIN.	-90 MAX.	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
tpd1	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	–	15	–	20	ns
tpd2	1	2	Data Propagation Delay, Worst Case Path	–	17	–	20	–	25	ns
fmax	1	3	Clock Frequency with Internal Feedback[3]	90.9	–	80	–	60	–	MHz
fmax (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	58.8	–	50	–	38	–	MHz
fmax (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	100	–	83	–	MHz
tsu1	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	–	7	–	9	–	ns
tco1	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	8	–	10	–	13	ns
th1	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
tsu2	–	9	GLB Reg. Setup Time before Clock	9	–	10	–	13	–	ns
tco2	–	10	GLB Reg. Clock to Output Delay	–	10	–	12	–	16	ns
th2	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
tr1	1	12	Ext. Reset Pin to Output Delay	–	15	–	17	–	22.5	ns
trw1	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
ten	2	14	Input to Output Enable	–	15	–	18	–	24	ns
tdis	3	15	Input to Output Disable	–	15	–	18	–	24	ns
twh	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	5	–	6	–	ns
twl	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	5	–	6	–	ns
tsu5	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2	–	2.5	–	ns
th5	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	6.5	–	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
tiobp	20	I/O Register Bypass	–	1.0	–	2.0	–	2.7	ns
tiolat	21	I/O Latch Delay	–	2.0	–	3.0	–	4.0	ns
tiosu	22	I/O Register Setup Time before Clock	4.5	–	5.5	–	7.3	–	ns
tioh	23	I/O Register Hold Time after Clock	2.0	–	1.0	–	1.3	–	ns
tioco	24	I/O Register Clock to Out Delay	–	2.0	–	3.0	–	4.0	ns
tior	25	I/O Register Reset to Out Delay	–	2.5	–	2.5	–	3.3	ns
tdin	26	Dedicated Input Delay	–	2.0	–	4.0	–	5.3	ns
GRP									
tgrp1	27	GRP Delay, 1 GLB Load	–	0.7	–	1.5	–	2.0	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	1.0	–	2.0	–	2.7	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	1.8	–	3.0	–	4.0	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	2.6	–	3.8	–	5.0	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	3.4	–	4.5	–	6.0	ns
GLB									
t4ptbp	33	4 Product Term Bypass Path Delay	–	6.5	–	6.5	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	7.0	–	7.0	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	8.0	–	8.0	–	10.6	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	9.5	–	9.5	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	0.5	–	1.0	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	1.0	–	1.0	–	1.3	–	ns
tgh	39	GLB Register Hold Time after Clock	3.5	–	4.5	–	6.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	1.5	–	2.0	–	2.7	ns
tgr	41	GLB Register Reset to Output Delay	–	2.5	–	2.5	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	10.0	–	10.0	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	9.0	–	12.0	ns
tptck	44	GLB Product Term Clock Delay	3.5	7.5	3.5	7.5	4.6	9.9	ns
ORP									
torp	45	ORP Delay	–	2.5	–	2.5	–	3.3	ns
torpbp	46	ORP Bypass Delay	–	0.5	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t$_{ob}$	47	Output Buffer Delay	–	2.5	–	3.0	–	4.0	ns
t$_{oen}$	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t$_{odis}$	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t$_{gy0}$	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.5	3.5	4.5	4.5	6.0	6.0	ns
t$_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.5	4.5	3.5	5.5	4.6	7.3	ns
t$_{gcp}$	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.0	5.0	1.3	6.6	ns
t$_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	2.5	4.5	3.5	5.5	4.6	7.3	ns
t$_{iocp}$	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t$_{gr}$	55	Global Reset to GLB and I/O Registers	–	7.5	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

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External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	—	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	38	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle[4]	83	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	—	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	—	13	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	13	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	16	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	—	22.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	13	—	ns
t_{en}	2	14	Input to Output Enable	—	24	ns
t_{dis}	3	15	Input to Output Disable	—	24	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	6	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	6	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2.5	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	8.5	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t iobp	20	I/O Register Bypass	—	2.7	ns
t iolat	21	I/O Latch Delay	—	4.0	ns
t iosu	22	I/O Register Setup Time before Clock	7.3	—	ns
t ioh	23	I/O Register Hold Time after Clock	1.3	—	ns
t ioco	24	I/O Register Clock to Out Delay	—	4.0	ns
t ior	25	I/O Register Reset to Out Delay	—	3.3	ns
t din	26	Dedicated Input Delay	—	5.3	ns
GRP					
t grp1	27	GRP Delay, 1 GLB Load	—	2.0	ns
t grp4	28	GRP Delay, 4 GLB Loads	—	2.7	ns
t grp8	29	GRP Delay, 8 GLB Loads	—	4.0	ns
t grp12	30	GRP Delay, 12 GLB Loads	—	5.0	ns
t grp16	31	GRP Delay, 16 GLB Loads	—	6.0	ns
GLB					
t 4ptbp	33	4 Product Term Bypass Path Delay	—	8.6	ns
t 1ptxor	34	1 Product Term/XOR Path Delay	—	9.3	ns
t 20ptxor	35	20 Product Term/XOR Path Delay	—	10.6	ns
t xoradj	36	XOR Adjacent Path Delay[3]	—	12.7	ns
t gbp	37	GLB Register Bypass Delay	—	1.3	ns
t gsu	38	GLB Register Setup Time before Clock	1.3	—	ns
t gh	39	GLB Register Hold Time after Clock	6.0	—	ns
t gco	40	GLB Register Clock to Output Delay	—	2.7	ns
t gr	41	GLB Register Reset to Output Delay	—	3.3	ns
t ptre	42	GLB Product Term Reset to Register Delay	—	13.3	ns
t ptoe	43	GLB Product Term Output Enable to I/O Cell Delay	—	12.0	ns
t ptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t orp	45	ORP Delay	—	3.3	ns
t orpbp	46	ORP Bypass Delay	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	—	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	—	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	—	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	—	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1016 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

8.0 ns = $(1.0 + 1.0 + 8.0) + (3.5) - (1.0 + 1.0 + 3.5)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

2.5 ns = $(1.0 + 1.0 + 7.5) + (3.0) - (1.0 + 1.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

16.0 ns = $(1.0 + 1.0 + 7.5) + (2.0) + (2.5 + 2.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.0 ns = $(1.0 + 1.0 + 8.0) + (3.5) - (3.5 + 2.0 + 1.0)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

3.5 ns = $(3.5 + 2.0 + 5.0) + (3.0) - (1.0 + 1.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

17.0 ns = $(3.5 + 2.0 + 5.0) + (2.0) + (2.5 + 2.0)$

1. Calculations are based upon timing specs for the ispLSI 1016-90.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB loads

In-System Programmability

The ispLSI devices are the in-system programmable version of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, the programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^{2}CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{ispEN}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this pLSI and ispLSI Data Book Supplement.

Figure 5. ispLSI Programming Interface

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 6. Timing Waveforms for In-System Programming

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Figure 7. Program, Verify & Bulk Erase Waveforms

Figure 8 illustrates the address and data shift register bits for the ispLSI 1016. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book Supplement.

Figure 8. ispLSI Device & Shift Register Layout

Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 3	2	Dedicated input pins to the device.
ispEN	13	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	14	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 2	36	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 1	24	Input/Output – This pin performs two functions. It is a dedicated clock input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/Y2	33	Input – This pin performs two functions. It is a dedicated clock input when ispEN is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.

Y1/RESET	35	This pin performs two functions:
		  – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
		  – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.

GND Vcc	1, 23 12, 34	Ground (GND) V_{cc}

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Pin Configuration

ispLSI 1016 PLCC Pinout Diagram

Top of chip (left to right): I/O 27 (6), I/O 26 (5), I/O 25 (4), I/O 24 (3), IN 3 (2), GND (1), I/O 23 (44), I/O 22 (43), I/O 21 (42), I/O 20 (41), I/O 19 (40)

Left side (top to bottom):
Pin	Signal
7	I/O 28
8	I/O 29
9	I/O 30
10	I/O 31
11	Y0
12	VCC
13	ispEN
14	SDI/IN 0
15	I/O 0
16	I/O 1
17	I/O 2

Center: **ispLSI 1016**

Right side (top to bottom):
Pin	Signal
39	I/O 18
38	I/O 17
37	I/O 16
36	MODE/IN 2
35	Y1/RESET
34	VCC
33	SCLK/Y2
32	I/O 15
31	I/O 14
30	I/O 13
29	I/O 12

Bottom of chip (left to right): I/O 3 (18), I/O 4 (19), I/O 5 (20), I/O 6 (21), I/O 7 (22), GND (23), SDO/IN 1 (24), I/O 8 (25), I/O 9 (26), I/O 10 (27), I/O 11 (28)

Package Diagram

44-Pin PLCC

Dimensions in inches MIN./MAX.

$\frac{0.042}{0.048}$ x 45°

0.050 BSC

0.020 Minimum

Top View

$\frac{0.590}{0.630}$

$\frac{0.650}{0.656}$

$\frac{0.685}{0.695}$

$\frac{0.165}{0.180}$

$\frac{0.090}{0.120}$

Seating Plane
Coplanarity not
to exceed 0.004

Part Number Description

ispLSI 1016 − XX X X X

Device Family

Device Number

Speed
90 = 90 MHz **f**max
80 = 80 MHz **f**max
60 = 60 MHz **f**max

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low

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Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
90	12	ispLSI 1016-90LJ	44-Pin PLCC
80	15	ispLSI 1016-80LJ	44-Pin PLCC
60	20	ispLSI 1016-60LJ	44-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1016-60LJI	44-Pin PLCC

Lattice

ispLSI 1024

in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

• IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC
  - Member of Lattice's ispLSI Family
  - Fully Compatible with Lattice's pLSI™ Family
  - High-Speed Global Interconnects
  - 48 I/O Pins, Six Dedicated Inputs
  - 144 Registers
  - Wide Input Gating for Fast Counters, State
    Machines, Address Decoders, etc.
  - Small Logic Block Size for Fast Random Logic
  - Security Cell Prevents Unauthorized Copying
• HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - $f$max = 80 MHz Maximum Operating Frequency
  - $t$pd = 15 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
• IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)
  - Change Logic and Interconnects "on-the-fly" in
    Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
• COMBINES EASE OF USE AND THE FAST SYSTEM
  SPEED OF PLDs WITH THE DENSITY AND FLEX-
  IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS
  - Complete Programmable Device can Combine Glue
    Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global
    Interconnectivity
• pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)

  pDS Software
    - Easy to Use PC Windows™ Interface
    - Boolean Logic Compiler
    - Manual Partitioning
    - Automatic Place and Route
    - Static Timing Table
  pDS+™ Software
    - Industry Standard, Third Party Design
      Environments
    - Schematic Capture, State Machine, VHDL
    - Automatic Partitioning
    - Automatic Place and Route
    - Comprehensive Logic and Timing Simulation
    - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice ispLSI 1024 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1024 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1024 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see figure 1). There are a total of 24 GLBs in the ispLSI 1024 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 1024 Functional Block Diagram

The device also has 48 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI 1024 device contains three of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1024 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B4 on the ispLSI 1024 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} . . . . -0.5 to +7.0V

Input Voltage Applied . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 125°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{cc}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{cc}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

$^*C_L$ includes Test Fixture and Probe Capacitance.

Output Load Conditions

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	$I_{OL} = 8$ mA		–	–	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4$ mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT}$		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	–	130	190	mA
		$f_{TOGGLE} = 20$ MHz	Industrial	–	130	215	mA

1. One output at a time for a maximum duration of one second.
2. Measured using six 16-bit counters.
3. Typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	#[2]	DESCRIPTION[1]	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	20	I/O Register Bypass	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
t_{grp24}	32	GRP Delay, 24 GLB Loads	–	6.3	–	8.3	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_{orp}	45	ORP Delay	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

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Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

4

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	# [2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp24}	32	GRP Delay, 24 GLB Loads	–	8.3	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1024 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

5.5 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

4.0 ns = $(2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

19.0 ns = $(2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.0 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (3.0 + 2.0 + 1.0)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

2.5 ns = $(3.0 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

17.5 ns = $(3.0 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)$

1. Calculations are based upon timing specs for the ispLSI 1024-80.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Six 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

::::Lattice

In-System Programmability

The ispLSI devices are the in-system programmable version of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, the programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this pLSI and ispLSI Data Book Supplement.

Figure 5. ispLSI Programming Interface

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage	Commercial	4.75	5	5.25	V
		Industrial ·	4.5	5	5.5	
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 6. Timing Waveforms for In-System Programming

Figure 7. Program, Verify & Bulk Erase Waveforms

Figure 8 illustrates the address and data shift register bits for the ispLSI 1024. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book Supplement.

Figure 8. ispLSI Device & Shift Register Layout

Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 5	2, 15	Dedicated input pins to the device.
ispEN	19	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	21	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 3	55	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 1	34	Input/Output – This pin performs two functions. It is a dedicated clock input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 2	49	Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	20	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	1, 18, 35, 52 17, 36, 53, 68	Ground (GND) V_{cc}

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Pin Configuration

ispLSI 1024 PLCC Pinout Diagram

Top pins (left to right): I/O 42, I/O 41, I/O 40, I/O 39, I/O 38, I/O 37, I/O 36, IN 4, GND, VCC, I/O 35, I/O 34, I/O 33, I/O 32, I/O 31, I/O 30, I/O 29

Top pin numbers: 9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61

Left side:
I/O 43 — 10
I/O 44 — 11
I/O 45 — 12
I/O 46 — 13
I/O 47 — 14
IN 5 — 15
Y0 — 16
VCC — 17
GND — 18
ispEN — 19
RESET — 20
SDI/IN 0 — 21
I/O 0 — 22
I/O 1 — 23
I/O 2 — 24
I/O 3 — 25
I/O 4 — 26

Center: **ispLSI 1024**

Right side:
60 — I/O 28
59 — I/O 27
58 — I/O 26
57 — I/O 25
56 — I/O 24
55 — MODE/IN 3
54 — Y1
53 — VCC
52 — GND
51 — Y2
50 — Y3
49 — SCLK/IN 2
48 — I/O 23
47 — I/O 22
46 — I/O 21
45 — I/O 20
44 — I/O 19

Bottom pin numbers: 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

Bottom pins (left to right): I/O 5, I/O 6, I/O 7, I/O 8, I/O 9, I/O 10, I/O 11, SDO/IN 1, GND, VCC, I/O 12, I/O 13, I/O 14, I/O 15, I/O 16, I/O 17, I/O 18

Package Diagram

68-Pin PLCC

Dimensions in inches MIN./MAX.

$\frac{0.042}{0.048}$ x 45°

0.050 BSC

0.020 Minimum

Top View

0.890 / 0.930

0.090 / 0.120

0.165 / 0.180

0.950 / 0.956
0.985 / 0.995

Seating Plane
Coplanarity not to exceed 0.004

Part Number Description

ispLSI 1024 – XX X X X

Device Family

Device Number

Speed
80 = 80 MHz fmax
60 = 60 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low

Ordering Information

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COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
80	15	ispLSI 1024-80LJ	68-Pin PLCC
60	20	ispLSI 1024-60LJ	68-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1024-60LJI	68-Pin PLCC

⣿Lattice

ispLSI™ *1032*
in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - Member of Lattice's ispLSI Family
  - Fully Compatible with Lattice's pLSI™ Family
  - High-Speed Global Interconnects
  - 64 I/O Pins, Eight Dedicated Inputs
  - 192 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Fast Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E^{2}CMOS® TECHNOLOGY**
  - f$_{max}$ = 80 MHz Maximum Operating Frequency
  - t$_{pd}$ = 15 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E^{2}CMOS Technology
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice ispLSI 1032 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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Functional Block Diagram

Figure 1. ispLSI 1032 Functional Block Diagram

The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI 1032 device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1032 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V$_{CC}$ . . . . -0.5 to +7.0V

Input Voltage Applied . . . . -2.5 to V$_{CC}$ +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V$_{CC}$ +1.0V

Storage Temperature . . . . -65 to 125°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V$_{CC}$	Supply Voltage	Commercial	T$_A$ = 0°C to +70°C	4.75	5.25	V
		Industrial	T$_A$ = -40°C to +85°C	4.5	5.5	
V$_{IL}$	Input Low Voltage			0	0.8	V
V$_{IH}$	Input High Voltage			2.0	V$_{CC}$ + 1	V

Capacitance (T$_A$=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C$_1$	Dedicated Input Capacitance	8	pf	V$_{CC}$=5.0V, V$_{IN}$=2.0V
C$_2$	I/O and Clock Capacitance	10	pf	V$_{CC}$=5.0V, V$_{I/O}$, V$_Y$=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	135	195	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	135	220	mA

1. One output at a time for a maximum duration of one second.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
Inputs							
t_{iobp}	20	I/O Register Bypass	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	8.0	–	10.6	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_{orp}	45	ORP Delay	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

4

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	10.6	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

4

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60		UNITS
			MIN.	MAX.	
Outputs					
t_{ob}	47	Output Buffer Delay	—	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	—	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	—	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	—	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1032 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

5.5 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

4.0 ns = $(2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

19.0 ns = $(2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.0 ns = $(2.0 + 2.0 + 8.0) + (1.0) - (3.0 + 2.0 + 1.0)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

2.5 ns = $(3.0 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

17.5 ns = $(3.0 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)$

1. Calculations are based upon timing specs for the ispLSI 1032-80.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of eight 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

In-System Programmability

The ispLSI devices are the in-system programmable version of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, the programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this pLSI and ispLSI Data Book Supplement.

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Figure 5. ispLSI Programming Interface

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 6. Timing Waveforms for In-System Programming

Figure 7. Program, Verify & Bulk Erase Waveforms

Figure 8 illustrates the address and data shift register bits for the ispLSI 1032. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book Supplement.

Figure 8. ispLSI Device & Shift Register Layout

Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers				Description
I/O 0 - I/O 3	26,	27,	28,	29,	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
I/O 4 - I/O 7	30,	31,	32,	33,	
I/O 8 - I/O 11	34,	35,	36,	37,	
I/O 12 - I/O 15	38,	39,	40,	41,	
I/O 16 - I/O 19	45,	46,	47,	48,	
I/O 20 - I/O 23	49,	50,	51,	52,	
I/O 24 - I/O 27	53,	54,	55,	56,	
I/O 28 - I/O 31	57,	58,	59,	60,	
I/O 32 - I/O 35	68,	69,	70,	71,	
I/O 36 - I/O 39	72,	73,	74,	75,	
I/O 40 - I/O 43	76,	77,	78,	79,	
I/O 44 - I/O 47	80,	81,	82,	83,	
I/O 48 - I/O 51	3,	4,	5,	6,	
I/O 52 - I/O 55	7,	8,	9,	10,	
I/O 56 - I/O 59	11,	12,	13,	14,	
I/O 60 - I/O 63	15,	16,	17,	18	
IN 4 - IN 7	67,	84,	2,	19	Dedicated input pins to the device.
ispEN	23				Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	25				Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1	42				Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2	44				Input/Output – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3	61				Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	24				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1,	22,	43,	64	Ground (GND)
VCC	21,	65			V$_{cc}$

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Pin Configuration

IspLSI 1032 PLCC Pinout Diagram

Top pins (left to right): I/O 56, I/O 55, I/O 54, I/O 53, I/O 52, I/O 51, I/O 50, I/O 49, I/O 48, IN 6, GND, IN 5, I/O 47, I/O 46, I/O 45, I/O 44, I/O 43, I/O 42, I/O 41, I/O 40, I/O 39

Top pin numbers: 11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75

Left side:
Pin	Number
I/O 57	12
I/O 58	13
I/O 59	14
I/O 60	15
I/O 61	16
I/O 62	17
I/O 63	18
IN 7	19
Y0	20
VCC	21
GND	22
$\overline{\text{ispEN}}$	23
$\overline{\text{RESET}}$	24
SDI/IN 0	25
I/O 0	26
I/O 1	27
I/O 2	28
I/O 3	29
I/O 4	30
I/O 5	31
I/O 6	32

Center: **ispLSI 1032**

Right side:
Number	Pin
74	I/O 38
73	I/O 37
72	I/O 36
71	I/O 35
70	I/O 34
69	I/O 33
68	I/O 32
67	IN 4
66	Y1
65	VCC
64	GND
63	Y2
62	Y3
61	SCLK/IN 3
60	I/O 31
59	I/O 30
58	I/O 29
57	I/O 28
56	I/O 27
55	I/O 26
54	I/O 25

Bottom pin numbers: 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53

Bottom pins (left to right): I/O 7, I/O 8, I/O 9, I/O 10, I/O 11, I/O 12, I/O 13, I/O 14, I/O 15, MODE/IN 1, GND, SDO/IN 2, I/O 16, I/O 17, I/O 18, I/O 19, I/O 20, I/O 21, I/O 22, I/O 23, I/O 24

Package Diagram

84-Pin PLCC

Dimensions in inches MIN./MAX.

$\frac{0.042}{0.048}$ x 45°

0.050 BSC

0.020 Minimum

Top View

1.090
1.130

1.150
1.156
1.185
1.195

0.165
0.180

0.020
0.120

Seating Plane
coplanarity not
to exceed 0.004

Part Number Description

ispLSI 1032 – XX   X   X   X

Device Family

Device Number

Speed
80 = 80 MHz fmax
60 = 60 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC

Power
L = Low

Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
80	15	ispLSI 1032-80LJ	84-Pin PLCC
60	20	ispLSI 1032-60LJ	84-Pin PLCC

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1032-60LJI	84-Pin PLCC

⠿Lattice

ispLSI™ 1048
in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - Member of Lattice's ispLSI Family
  - Fully Compatible with Lattice's pLSI™ Family
  - High-Speed Global Interconnects
  - 96 I/O Pins, Ten Dedicated Inputs
  - 288 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - $f$max = 70 MHz Maximum Operating Frequency
  - $t$pd = 18 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**
  - pDS Software
    - Easy to Use PC Windows™ Interface
    - Boolean Logic Compiler
    - Manual Partitioning
    - Automatic Place and Route
    - Static Timing Table
  - pDS+™ Software
    - Industry Standard, Third Party Design Environments
    - Schematic Capture, State Machine, VHDL
    - Automatic Partitioning
    - Automatic Place and Route
    - Comprehensive Logic and Timing Simulation
    - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice ispLSI 1048 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1048 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the ispLSI 1048 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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Functional Block Diagram

Figure 1. ispLSI 1048 Functional Block Diagram

The device also has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs (one dedicated input in Megablock B and E) and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI 1048 device contains six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1048 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI 1048 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V$_{CC}$. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V$_{CC}$ +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V$_{CC}$ +1.0V

Storage Temperature . . . . -65 to 125°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

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DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V$_{CC}$	Supply Voltage	Commercial	T$_A$ = 0°C to +70°C	4.75	5.25	V
		Industrial	T$_A$ = -40°C to +85°C	4.5	5.5	
V$_{IL}$	Input Low Voltage			0	0.8	V
V$_{IH}$	Input High Voltage			2.0	Vcc + 1	V

Capacitance (T$_A$=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C$_1$	Dedicated Input Capacitance	8	pf	V$_{CC}$=5.0V, V$_{IN}$=2.0V
C$_2$	I/O and Clock Capacitance	10	pf	V$_{CC}$=5.0V, V$_{I/O}$, V$_Y$=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}		-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	165	235	mA
		f_{TOGGLE} = 20 MHz	Industrial	–	165	260	mA

1. One output at a time for a maximum duration of one second.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	18	–	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	23	–	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	71.4	–	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	41.7	–	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	12	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	12	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	12	–	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	14	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	17	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	2	14	Input to Output Enable	–	20	–	26.7	ns
t_{dis}	3	15	Input to Output Disable	–	20	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
Inputs							
tiobp	20	I/O Register Bypass	–	3.0	–	4.0	ns
tiolat	21	I/O Latch Delay	–	4.0	–	5.3	ns
tiosu	22	I/O Register Setup Time before Clock	6.0	–	8.1	–	ns
tioh	23	I/O Register Hold Time after Clock	0.5	–	0.9	–	ns
tioco	24	I/O Register Clock to Out Delay	–	3.0	–	3.9	ns
tior	25	I/O Register Reset to Out Delay	–	3.5	–	4.6	ns
tdin	26	Dedicated Input Delay	–	6.0	–	8.0	ns
GRP							
tgrp1	27	GRP Delay, 1 GLB Load	–	2.5	–	3.3	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	3.0	–	4.0	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	4.0	–	5.3	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	5.0	–	6.7	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	6.0	–	8.0	ns
tgrp48	32	GRP Delay, 48 GLB Loads	–	16.0	–	21.3	ns
GLB							
t4ptbp	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	7.5	–	10.0	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	1.5	–	2.0	–	ns
tgh	39	GLB Register Hold Time after Clock	6.0	–	8.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	2.5	–	3.3	ns
tgr	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	11.9	ns
tptck	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
torp	45	ORP Delay	–	3.5	–	4.7	ns
torpbp	46	ORP Bypass Delay	–	1.5	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	5.0	5.0	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.0	6.0	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.0	6.0	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.0	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	12	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	26.7	ns
t_{dis}	3	15	Input to Output Disable	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
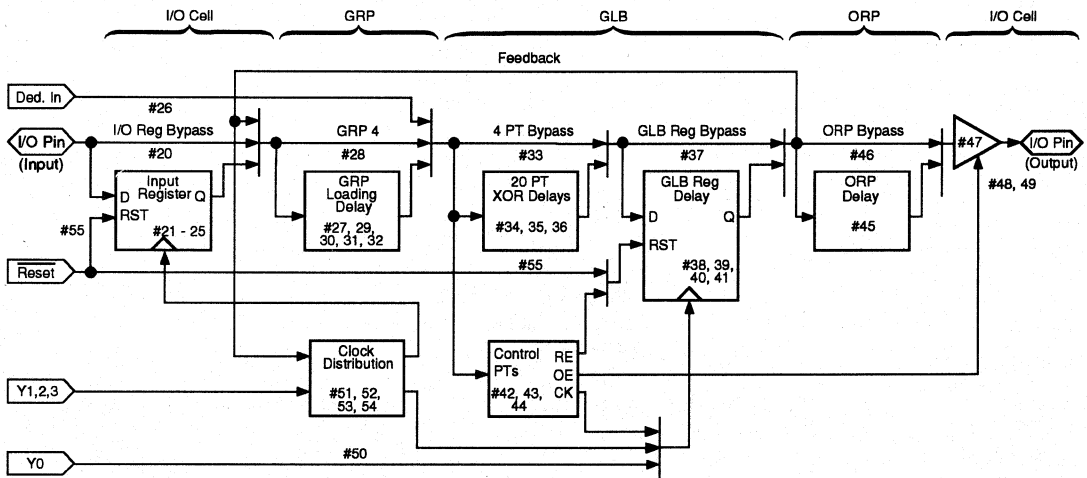5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Inputs					
tiobp	20	I/O Register Bypass	–	4.0	ns
tiolat	21	I/O Latch Delay	–	5.3	ns
tiosu	22	I/O Register Setup Time before Clock	8.1	–	ns
tioh	23	I/O Register Hold Time after Clock	0.9	–	ns
tioco	24	I/O Register Clock to Out Delay	–	3.9	ns
tior	25	I/O Register Reset to Out Delay	–	4.6	ns
tdin	26	Dedicated Input Delay	–	8.0	ns
GRP					
tgrp1	27	GRP Delay, 1 GLB Load	–	3.3	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	4.0	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	5.3	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	6.7	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	8.0	ns
tgrp48	32	GRP Delay, 48 GLB Loads	–	21.3	ns
GLB					
t4ptbp	33	4 Product Term Bypass Path Delay	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	10.0	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	2.0	–	ns
tgh	39	GLB Register Hold Time after Clock	8.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	3.3	ns
tgr	41	GLB Register Reset to Output Delay	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	11.9	ns
tptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
torp	45	ORP Delay	–	4.7	ns
torpbp	46	ORP Bypass Delay	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	—	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	—	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	—	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	—	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1048 Timing Model

Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(min))$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

5.5 ns = $(3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

6.0 ns = $(3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

22.5 ns = $(3.0 + 3.0 + 7.5) + (2.5) + (3.5 + 3.0)$

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0}(min) + t_{gco} + t_{gcp}(min))$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

6.5 ns = $(3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

5.0 ns = $(5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

21.5 ns = $(5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)$

1. Calculations are based upon timing specs for the ispLSI 1048-70.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

Figure 4. Maximum GRP Delay vs GLB Loads

In-System Programmability

The ispLSI devices are the in-system programmable version of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, the programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^{2}CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this pLSI and ispLSI Data Book Supplement.

Figure 5. ispLSI Programming Interface

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 6. Timing Waveforms for In-System Programming

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Figure 7. Program, Verify & Bulk Erase Waveforms

Figure 8 illustrates the address and data shift register bits for the ispLSI 1048. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectiural Description section of this Data Book Supplement.

Figure 8. ispLSI Device & Shift Register Layout

Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

::::: Lattice

Pin Description

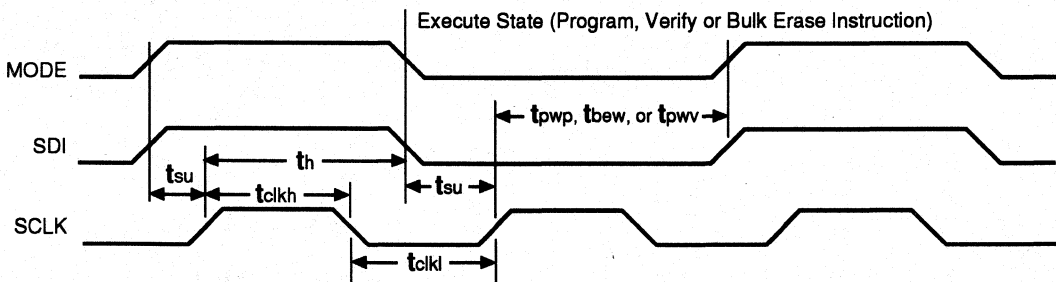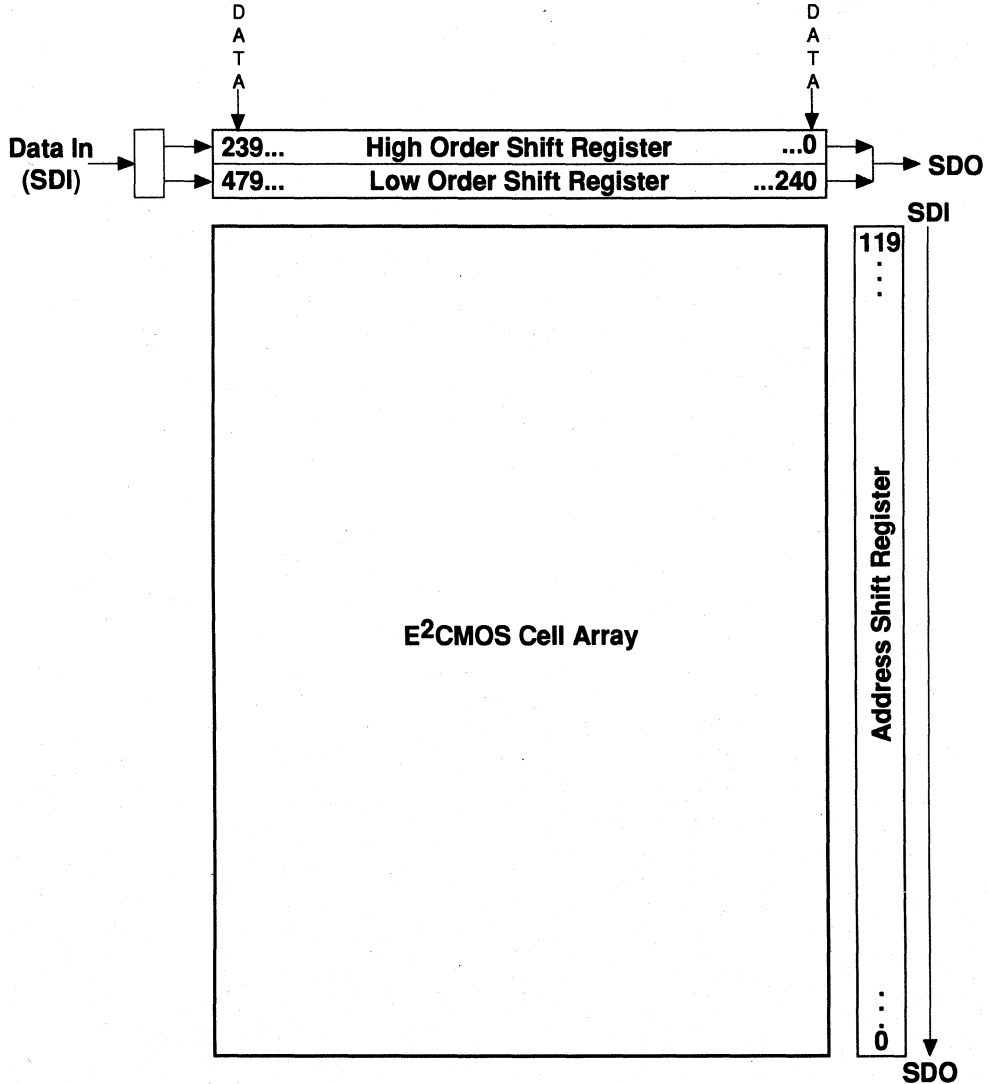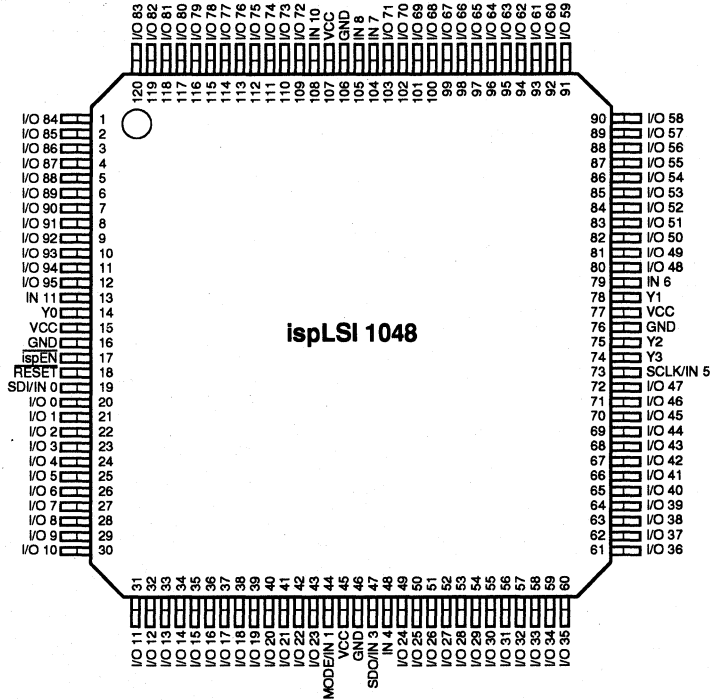| Name	PQFP Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99,100,101,102,103, 109,110,111,112,113,114, 115,116,117,118,119,120, 1, 2, 3, 4 5, 6, 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 IN 6 - IN 11	48, 79,104,105, – 108, 13	Dedicated input pins to the device. (IN 2 and IN 9 not available)
$\overline{\text{ispEN}}$	17	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	19	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1	44	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 3	47	Input/Output – This pin performs two functions. It is a dedicated clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 5	73	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	18	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	14	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	78	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	75	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	74	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND **V**CC	46, 76,106, 16 15, 45, 77, 107	Ground (GND) V_{cc}

4

Pin Configuration

IspLSI 1048 PQFP Pinout Diagram
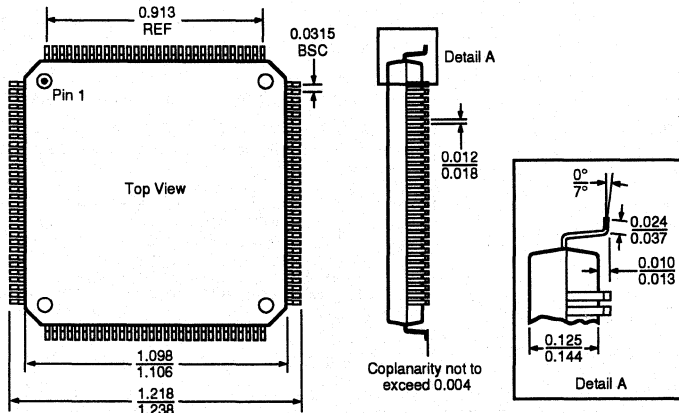
Package Diagram

120-Pin PQFP

Dimensions in inches MIN./MAX.

Part Number Description

ispLSI 1048 – XX X X X

Device Family

Device Number

Speed
70 = 70 MHz fmax
50 = 50 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
Q = PQFP

Power
L = Low
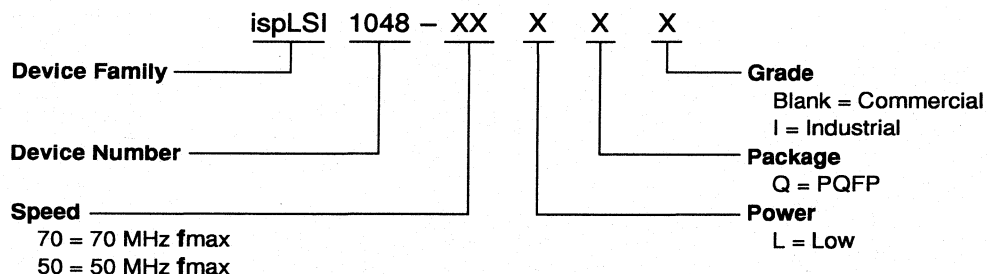
Ordering Information

COMMERCIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
70	18	ispLSI 1048-70LQ	120-Pin PQFP
50	24	ispLSI 1048-50LQ	120-Pin PQFP

INDUSTRIAL

fmax (MHz)	tpd (ns)	Ordering Number	Package
50	24	ispLSI 1048-50LQI	120-Pin PQFP

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Section 1: **Introduction to pLSI and ispLSI**

Section 2: **pLSI and ispLSI Architectural Description**

Section 3: **pLSI Data Sheets**

Section 4: **ispLSI Data Sheets**

Section 5: **Military pLSI and ispLSI Data Sheets**

Section 6: **General Information**

5

Military Program
Overview

CORPORATE PHILOSOPHY

Lattice Semiconductor is committed to leadership in performance and quality. Our families of Military pLSI and ispLSI devices are consistent with this philosophy. Lattice manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial through MIL-STD-883, are monitored under a quality program conformant to MIL-M-38510 Appendix A with inspections conformant to MIL-I-45208.

Complete reviews of Lattice's procedures, documentation and technical data are welcomed and can be arranged at the Company's facility near Portland, Oregon.

For the latest availability information on MIL-STD-883 processed pLSI and ispLSI devices, please contact your local sales office.

QUALITY AND TESTABILITY

Lattice Semiconductor processes its Military pLSI and ispLSI devices in strict conformance with MIL-STD-883 Class B. In conjunction with the Military flow, the inherent testability of E^2CMOS technology allows Lattice to achieve a quality level superior to other PLD or FPGA technologies.

All pLSI and ispLSI devices are patterned and tested dozens of times throughout the manufacturing flow. Every device is tested under worst case configurations to assure customers achieve 100% yields. Tests are performed using the same E^2 cell array that will be used for the final patterning of the devices. The 100% "actual test" philosophy eliminates the correlated and simulated testing that is necessary with other technologies.

MIL-STD-883 COMPLIANCE

MIL-STD-883 provides a uniform and precise method for environmental, mechanical and electrical testing which ensures the suitability of microelectronic devices for use in military and aerospace systems. Table I (page 5-2) summarizes the MIL-STD-883 Class B Flow. Table II summarizes the detailed Quality Conformance Inspection tests rigorously performed by Lattice as required by MIL-STD-883, Method 5005.

MIL-M-38510

MIL-M-38510, when used in conjunction with MIL-STD-883, defines design, packaging, material, marking, sampling, qualification and quality system requirements for military devices.

GROUP DATA

Group A and B data is taken on every inspection lot per MIL-STD-883, Class B requirements. This data, along with Generic Group C and D can be supplied upon written request, with your device shipment. Your Lattice sales representative can advise you of charges and leadtime necessary for providing this data.

STANDARD MILITARY DRAWINGS

Lattice actively supports the DESC Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883 product specifications to simplify military procurement.

Lattice recognizes the growing demand for SMD qualified devices, and in response, all new 883 products released by Lattice will be submitted to DESC for SMD qualification. Customers may facilitate this process by submitting a "Nonstandard Part Approval Request", DD Form 2052, to DESC. This form allows you to recommend to DESC the qualification of Lattice devices to SMD status.

5

Military Program Overview

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E, Y_1 axis	100%
Hermeticity	1014	100%
Fine	Cond. A or B	
Gross	Cond. C	
Endurance Test	1033	100%
Retention Test	Unbiased Bake	100%
	24 Hrs.	
	$T_A = 180°C$	
Pre Burn-in Electrical	Applicable Device	100%
	Specification	
	$T_C = 25°C$	
Dynamic Burn-in	1015 Cond. D	
Post Burn-in Electrical	Applicable Device	100%
	Specification	
	$T_C = 25°C$	
	PDA = 5%	
Final Electrical Test	Applicable Device	100%
	Specification	
	$T_C = 125°C$	
Final Electrical Test	Applicable Device	100%
	Specification	
	$T_C = 55°C$	
Final Electrical Test	Applicable Device	100%
	Specification	
	$T_C = 25°C$	
External Visual	2009	100%
QCI Sample Selection	MIL-M-38510	Sample
	Sec. 4.5 and	
	MIL-STD-883	
	Sec. 1.2	

Subgroup	Method	Sample
GROUP A: Electrical Tests		
Subgroups 1, 7, 9	Applicable Device Spec.	LTPD = 2
Electrical Test	25°C	
Subgroups 2, 8A, 10	Applicable Device Spec.	LTPD = 2
Electrical Test	Max. Operating Temp.	
Subgroups 3, 8B, 11	Applicable Device Spec.	LTPD = 2
Electrical Test	Min. Operating Temp.	
GROUP B: Mechanical Tests		
Subgroup 2		4(0)
Solvent Resistance	2015	
Sungroup 3		LTPD = 10
Solderability	2003	
Subgroup 5		LTPD = 15
Bond Strength	2011	
GROUP C: Chip Integrity Tests		
Sungroup 1		LTPD = 5
Dynamic Life Test	1005, 1,000 Hrs., 125°C	
End Point Electrical	Applicable Device Spec.	
Subgroup 2		LTPD = 5
Unbiased Retention	1,000 Hrs., 150°C	
End Point Electrical	Applicable Device Spec.	
GROUP D: Environmental Integrity		
Sungroup 1		LTPD = 15
Physical Dimensions	2016	
Subgroup 2		LTPD = 5
Lead Integrity	2004, Cond. B	
Hermeticity	1014	
Subgroup 3		LTPD = 15
Thermal Shock	1011, Cond. B, 15 Cycles	
Temp. Cycle	1010, Cond. C, 100 Cycles	
Moisture Resistance	1004	
Hermeticity	1014	
Visual Examination	1004, 1010	
Endpoint Electrical	Applicable Device Spec.	
Subgroup 4		LTPD = 15
Mechanical Shock	2002, Cond. B	
Vibration	2007, Cond. A	
Constant Acceleration	2001, Cond. E, Y_1 axis	
Hermiticity	1014	
Visual Examination	1010, 1011	
Endpoint Electrical	Applicable Device Spec.	
Subgroup 5		LTPD = 15
Salt Atmosphere	1009, Cond. A	
Hermeticity	1014	
Visual Examination	1009	
Subgroup 6		3(0)
Internal Water Vapor	1018<5,000 PPM, 100°C	
Subgroup 7		LTPD = 15
Lead Finish Adhesion	2025	

⠿Lattice

pLSI™ 1016/883

programmable Large Scale Integration
High-Density Programmable Logic

Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the pLSI 1016
  - High-Speed Global Interconnects
  - 32 I/O Pins, Four Dedicated Inputs
  - 96 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 60 MHz Maximum Operating Frequency
  - t_{pd} = 20 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Re-Programmable
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 pLSI 1016 is a High-Density Programmable Logic Device which contains 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1016/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..B7, (see figure 1). There are a total of 16 GLBs in the pLSI 1016/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 150°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	100	170	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_c = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
tiobp	20	I/O Register Bypass		2.7	ns
tiolat	21	I/O Latch Delay	—	4.0	ns
tiosu	22	I/O Register Setup Time before Clock	7.3	—	ns
tioh	23	I/O Register Hold Time after Clock	1.3	—	ns
tioco	24	I/O Register Clock to Out Delay	—	4.0	ns
tior	25	I/O Register Reset to Out Delay	—	3.3	ns
tdin	26	Dedicated Input Delay	—	5.3	ns
GRP					
tgrp1	27	GRP Delay, 1 GLB Load	—	2.0	ns
tgrp4	28	GRP Delay, 4 GLB Loads	—	2.7	ns
tgrp8	29	GRP Delay, 8 GLB Loads	—	4.0	ns
tgrp12	30	GRP Delay, 12 GLB Loads	—	5.0	ns
tgrp16	31	GRP Delay, 16 GLB Loads	—	6.0	ns
GLB					
t4ptbp	33	4 Product Term Bypass Path Delay	—	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	—	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	—	10.6	ns
txoradj	36	XOR Adjacent Path Delay[3]	—	12.7	ns
tgbp	37	GLB Register Bypass Delay	—	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	1.3	—	ns
tgh	39	GLB Register Hold Time after Clock	6.0	—	ns
tgco	40	GLB Register Clock to Output Delay	—	2.7	ns
tgr	41	GLB Register Reset to Output Delay	—	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	—	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	—	12.0	ns
tptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
torp	45	ORP Delay	—	3.3	ns
torpbp	46	ORP Bypass Delay	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1016/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(min))$
= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$
7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6)$

t_h = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$
5.3 ns = $(2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6)$

t_{co} = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
25.3 ns = $(2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)$

Derivations of tsu, th and tco from the Clock GLB

t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0}(min) + t_{gco} + t_{gcp}(min))$
= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$
7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3)$

t_h = Clock (max) + Reg h - Logic
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$
5.3 ns = $(6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6)$

t_{co} = Clock (max) + Reg co + Output
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$
25.3 ns = $(6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)$

Pin Description

Name	JLCC Pin Numbers				Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 19, 25, 29, 37, 41, 3, 7,	16, 20, 26, 30, 38, 42, 4, 8,	17, 21, 27, 31, 39, 43, 5, 9,	18, 22, 28, 32, 40, 44, 6, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 3	14,	24,	36,	2	Dedicated input pins to the device.
Y0	11				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35				This pin performs two functions: — Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. — Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y2	33				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell in the device.
NC	13				This is a factory test pin and it should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND	1,	23			Ground (GND)
VCC	12,	34			V_{cc}

Pin Configuration

pLSI 1016/883 JLCC Pinout Diagram
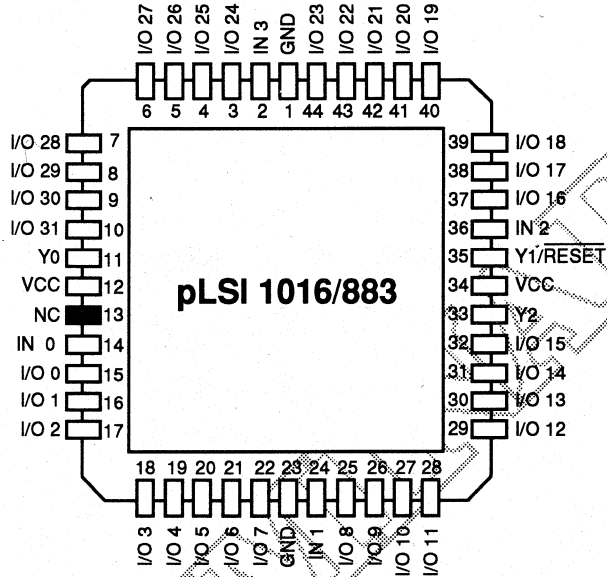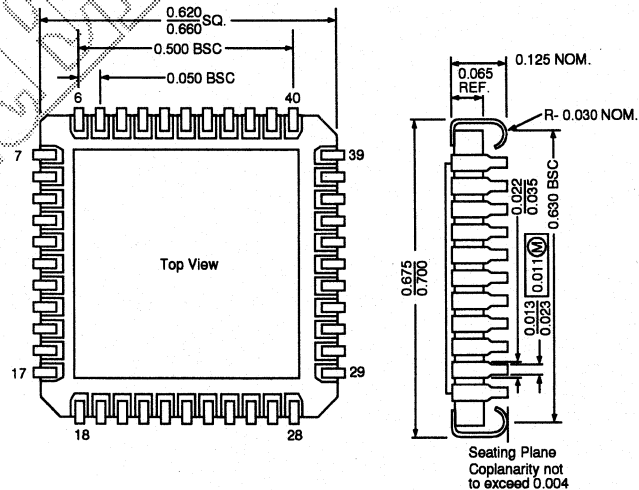
Package Diagram

44-Pin JLCC

Dimensions in inches MIN./MAX.

Top View

Seating Plane
Coplanarity not
to exceed 0.004

Part Number Description

pLSI   1016 – XX   X   X   X

Device Family

Device Number

Speed
60 = 60 MHz fmax

MIL Process   /883 = 883 Process

Package
H = 44-Pin JLCC

Power
L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1016-60LH/883	44-Pin JLCC

⋮⋮⋮Lattice

pLSI™ 1024/883

programmable Large Scale Integration
High-Density Programmable Logic
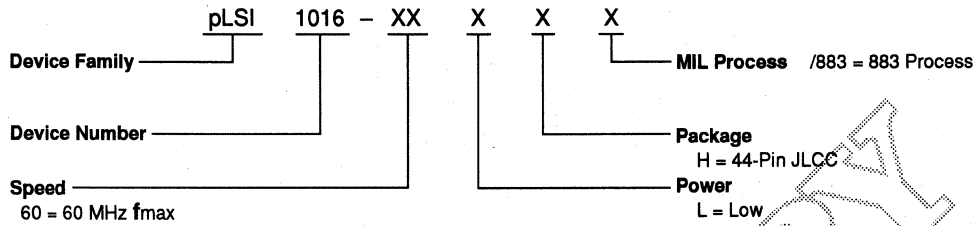
Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the pLSI 1024
  - High-Speed Global Interconnects
  - 48 I/O Pins, Six Dedicated Inputs
  - 144 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 60 MHz Maximum Operating Frequency
  - t_{pd} = 20 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Re-Programmable
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 pLSI 1024 is a High-Density Programmable Logic Device which contains 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1024/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..C7, (see figure 1). There are a total of 24 GLBs in the pLSI 1024/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated pins. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 150°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{cc} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	130	215	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using six 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_c = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp24}	32	GRP Delay, 24 GLB Loads	–	8.3	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

5

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

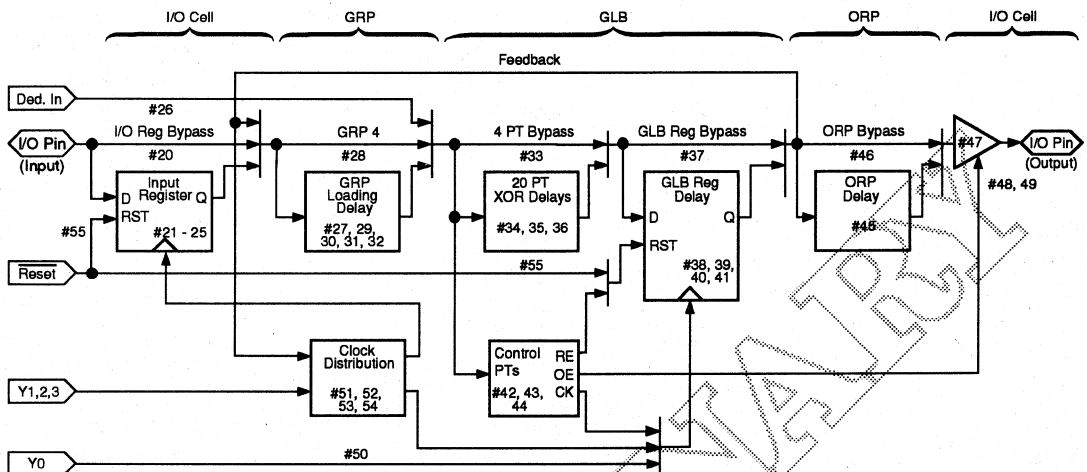1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1024/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
   = $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$
   = $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$
7.3 ns = (2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6)

th = Clock (max) + Reg h - Logic
   = $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
   = $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$
5.3 ns = (2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6)

tco = Clock (max) + Reg co + Output
   = $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
   = $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
25.3 ns = (2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)

Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su - Clock (min)
   = $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$
   = $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$
7.3 ns = (2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3)

th = Clock (max) + Reg h - Logic
   = $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
   = $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$
5.3 ns = (6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6)

tco = Clock (max) + Reg co + Output
   = $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
   = $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$
25.3 ns = (6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)

9/92. Rev. A

Pin Description

Name	JLCC Pin Numbers				Description
I/O 0 - I/O 3	22,	23,	24,	25,	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
I/O 4 - I/O 7	26,	27,	28,	29,	
I/O 8 - I/O 11	30,	31,	32,	33,	
I/O 12 - I/O 15	37,	38,	39,	40,	
I/O 16 - I/O 19	41,	42,	43,	44,	
I/O 20 - I/O 23	45,	46,	47,	48,	
I/O 24 - I/O 27	56,	57,	58,	59,	
I/O 28 - I/O 31	60,	61,	62,	63,	
I/O 32 - I/O 35	64,	65,	66,	67,	
I/O 36 - I/O 39	3,	4,	5,	6,	
I/O 40 - I/O 43	7,	8,	9,	10,	
I/O 44 - I/O 47	11,	12,	13,	14	
IN 0 - IN 3	21,	34,	49,	55,	Dedicated input pins to the device.
IN 4 - IN 5	2,	15			
$\overline{RESET}$	20				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50				Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	19				This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND	1,	18,	35,	52	Ground (GND)
V_{CC}	17,	36,	53,	68	V_{cc}

Pin Configuration

pLSI 1024/883 JLCC Pinout Diagram
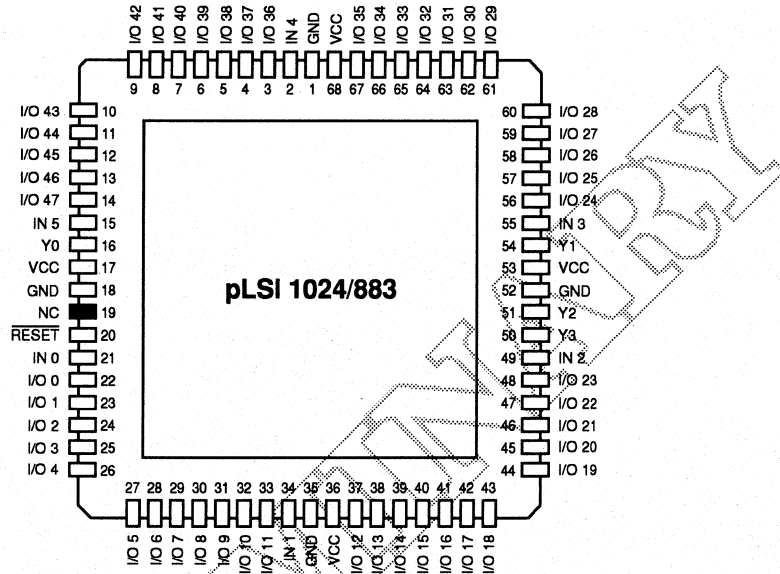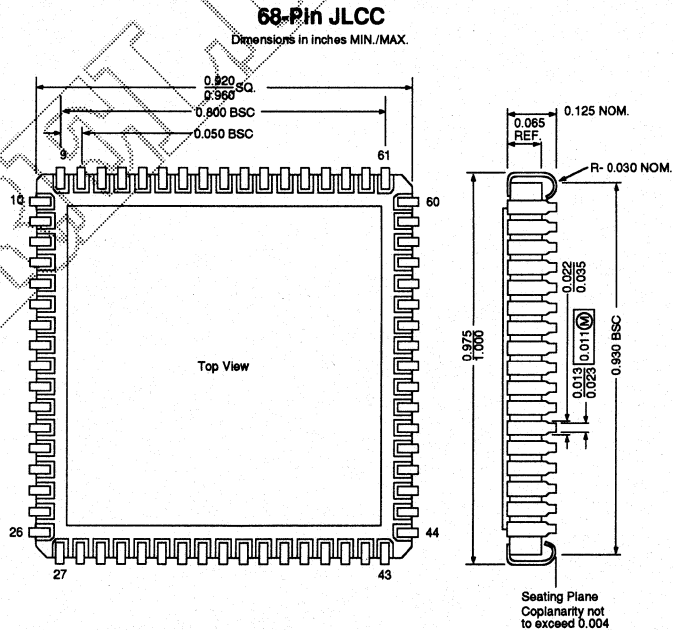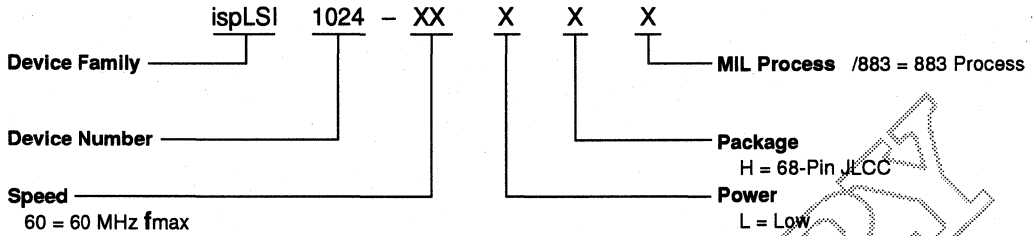
Package Diagram

68-Pin JLCC
Dimensions in inches MIN./MAX.

Part Number Description

```
        ispLSI   1024  —  XX    X    X    X
```

Device Family ────────┘   │
                               │
Device Number ─────────────────┘

Speed ──────────────────────────────────┘
  60 = 60 MHz fmax

MIL Process /883 = 883 Process

Package
  H = 68-Pin JLCC

Power
  L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1024-60LH/883	68-Pin JLCC

⠿⠿Lattice

pLSI™ 1032/883

programmable Large Scale Integration
High-Density Programmable Logic

Features

• **PROGRAMMABLE HIGH-DENSITY LOGIC**

  — MIL-STD-883 Version of the pLSI 1032
  — High-Speed Global Interconnects
  — 64 I/O Pins, Eight Dedicated Inputs
  — 192 Registers
  — Wide Input Gating for Fast Counters, State
    Machines, Address Decoders, etc.
  — Small Logic Block Size for Random Logic
  — Security Cell Prevents Unauthorized Copying

• **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**

  — $f$max = 60 MHz Maximum Operating Frequency
  — $t$pd = 20 ns Propagation Delay
  — TTL Compatible Inputs and Outputs
  — Electrically Erasable and Re-Programmable
  — 100% Tested

• **COMBINES EASE OF USE AND THE FAST SYSTEM
  SPEED OF PLDs WITH THE DENSITY AND FLEX-
  IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**

  — Complete Programmable Device can Combine Glue
    Logic and Structured Designs
  — 100% Routable with High Utilization
  — Four Dedicated Clock Input Pins
  — Synchronous and Asynchronous Clocks
  — Flexible Pin Placement
  — Optimized Global Routing Pool Allows Global
    Interconnectivity

• **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
    — Easy to Use PC Windows™ Interface
    — Boolean Logic Compiler
    — Manual Partitioning
    — Autimatic Place and Route
    — Static Timing Table

  pDS+™ Software

    — Industry Standard, Third Party Design
      Environments
    — Schematic Capture, State Machine, VHDL
    — Automatic Partitioning
    — Automatic Place and Route
    — Comprehensive Logic and Timing Simulation
    — PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 pLSI 1032 is a High-Density
Programmable Logic Device which contains 192 Regis-
ters, 64 Universal I/O pins, eight Dedicated Input pins, four
Dedicated Clock Input pins and a Global Routing Pool
(GRP). The GRP provides complete interconnectivity
between all of these elements.

The basic unit of logic on the pLSI 1032/883 device is the
Generic Logic Block (GLB). The GLBs are labeled A0,
A1 .. D7, (see figure 1). There are a total of 32 GLBs in the
pLSI 1032/883 device. Each GLB has 18 inputs, a pro-
grammable AND/OR/XOR array, and four outputs which
can be configured to be either combinatorial or registered.
Inputs to the GLB come from the GRP and dedicated
inputs. All of the GLB outputs are brought back into the
GRP so that they can be connected to the inputs of any
other GLB on the device.

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Absolute Maximum Ratings [1]

Supply Voltage V_{cc} . . . . -0.5 to +7.0V

Input Voltage Applied . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 150°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{cc} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{cc}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{cc}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	135	220	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

![Lattice logo]

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	10.6	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

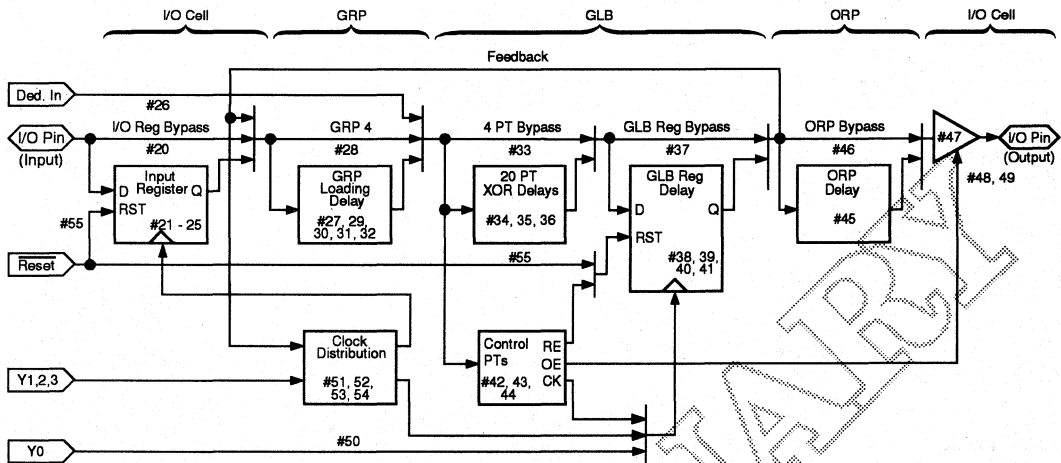| PARAMETER	#[2]	DESCRIPTION	-60		UNITS
			MIN.	MAX.	
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Lattice

pLSI 1032/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su − Clock (min)

= $(tiobp + tgrp4 + t20ptxor) + (tgsu) − (tiobp + tgrp4 + tptck(min))$

= $(\#20 + \#28 + \#35) + (\#38) − (\#20 + \#28 + \#44)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) − (2.7 + 2.7 + 4.6)$

th = Clock (max) + Reg h − Logic

= $(tiobp + tgrp4 + tptck(max)) + (tgh) − (tiobp + tgrp4 + t20ptxor)$

= $(\#20 + \#28 + \#44) + (\#39) − (\#20 + \#28 + \#35)$

5.3 ns = $(2.7 + 2.7 + 9.9) + (6.0) − (2.7 + 2.7 + 10.6)$

tco = Clock (max) + Reg co + Output

= $(tiobp + tgrp4 + tptck(max)) + (tgco) + (torp + tob)$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

25.3 ns = $(2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)$

Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su − Clock (min)

= $(tiobp + tgrp4 + t20ptxor) + (tgsu) − (tgy0(min) + tgco + tgcp(min))$

= $(\#20 + \#28 + \#35) + (\#38) − (\#50 + \#40 + \#52)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) − (6.0 + 2.7 + 1.3)$

th = Clock (max) + Reg h − Logic

= $(tgy0(max) + tgco + tgcp(max)) + (tgh) − (tiobp + tgrp4 + t20ptxor)$

= $(\#50 + \#40 + \#52) + (\#39) − (\#20 + \#28 + \#35)$

5.3 ns = $(6.0 + 2.7 + 6.6) + (6.0) − (2.7 + 2.7 + 10.6)$

tco = Clock (max) + Reg co + Output

= $(tgy0(max) + tgco + tgcp(max)) + (tgco) + (torp + tob)$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

25.3 ns = $(6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)$

5

Pin Description

Name	PGA Pin Numbers				Description
I/O 0 - I/O 3	F1,	H1,	H2,	J1,	Input/Output Pins - These are the general purpose I/O pins used by the
I/O 4 - I/O 7	K1,	J2,	L1,	K2,	logic array.
I/O 8 - I/O 11	K3,	L2,	L3,	K4,	
I/O 12 - I/O 15	L4,	J5,	K5,	L5,	
I/O 16 - I/O 19	L7,	K7,	L6,	L8,	
I/O 20 - I/O 23	K8,	L9,	L10,	K9,	
I/O 24 - I/O 27	L11,	K10,	J10,	K11,	
I/O 28 - I/O 31	J11,	H10,	H11,	F10,	
I/O 32 - I/O 35	E9,	D11,	D10,	C11,	
I/O 36 - I/O 39	B11,	C10,	A11,	B10,	
I/O 40 - I/O 43	B9,	A10,	A9,	B8,	
I/O 44 - I/O 47	A8,	B6,	B7,	A7,	
I/O 48 - I/O 51	A5,	B5,	C5,	A4,	
I/O 52 - I/O 55	B4,	A3,	A2,	B3,	
I/O 56 - I/O 59	A1,	B2,	C2,	B1,	
I/O 60 - I/O 63	C1,	D2,	D1,	E3	
IN 0 - IN 3	G2,	K6,	J7,	G10	Dedicated input pins to the device.
IN 4 - IN 7	E10,	C7,	A6,	E2	
$\overline{\text{RESET}}$	G1				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	G3				This pin should be left floating or tied to V_{cc}. This pin should never be tied to GND.
GND	C6,	F3,	F9,	J6	Ground (GND)
VCC	F2,	F11			V_{cc}

Pin Configuration

pLSI 1032/883 PGA Pinout Diagram

	11	10	9	8	7	6	5	4	3	2	1	
A	I/O38	I/O41	I/O42	I/O44	I/O47	IN6	I/O48	I/O51	I/O53	I/O54	I/O56	A
B	I/O36	I/O39	I/O40	I/O43	I/O46	I/O45	I/O49	I/O52	I/O55	I/O57	I/O59	B
C	I/O35	I/O37			IN5	GND	I/O50		INDEX	I/O58	I/O60	C
D	I/O33	I/O34								I/O61	I/O62	D
E	Y1	IN4	I/O32						I/O63	IN7	Y0	E
F	Vcc	I/O31	GND						GND	Vcc	I/O0	F
G	Y3	IN3	Y2						NC	IN0	RESET	G
H	I/O30	I/O29								I/O2	I/O1	H
J	I/O28	I/O26			IN2	GND	I/O13			I/O5	I/O3	J
K	I/O27	I/O25	I/O23	I/O20	I/O17	IN1	I/O14	I/O11	I/O8	I/O7	I/O4	K
L	I/O24	I/O22	I/O21	I/O19	I/O16	I/O18	I/O15	I/O12	I/O10	I/O9	I/O6	L

PIN A1

pLSI 1032/883
BOTTOM VIEW

Package Diagram

84-Pin PGA

Dimensions in inches MIN./MAX.

Part Number Description

Device Family

Device Number

Speed
60 = 60 MHz fmax

MIL Process /883 = 883 Process

Package
G = 84-Pin PGA

Power
L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	pLSI 1032-60LG/883	84-Pin PGA

⁙Lattice

pLSI™ 1048/883

programmable Large Scale Integration
High-Density Programmable Logic

Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the pLSI 1048
  - High-Speed Global Interconnects
  - 96 I/O Pins, Ten Dedicated Inputs
  - 288 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 50 MHz Maximum Operating Frequency
  - t_{pd} = 24 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Re-Programmable
  - 100% Tested

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity

- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 pLSI 1048 is a High-Density Programmable Logic Device which contains 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1048/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..F7, (see figure 1). There are a total of 48 GLBs in the pLSI 1048/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

5

Lattice

Absolute Maximum Ratings [1]

Supply Voltage V_{cc}. -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 150°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	165	260	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

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External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	# [2]	DESCRIPTION[1]	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	—	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	53.6	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	31.3	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle[4]	71.4	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	12	—	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	—	16	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	16	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	18.7	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	—	22.7	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	13	—	ns
t_{en}	2	14	Input to Output Enable	—	26.7	ns
t_{dis}	3	15	Input to Output Disable	—	26.7	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	7	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	7	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.7	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.7	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

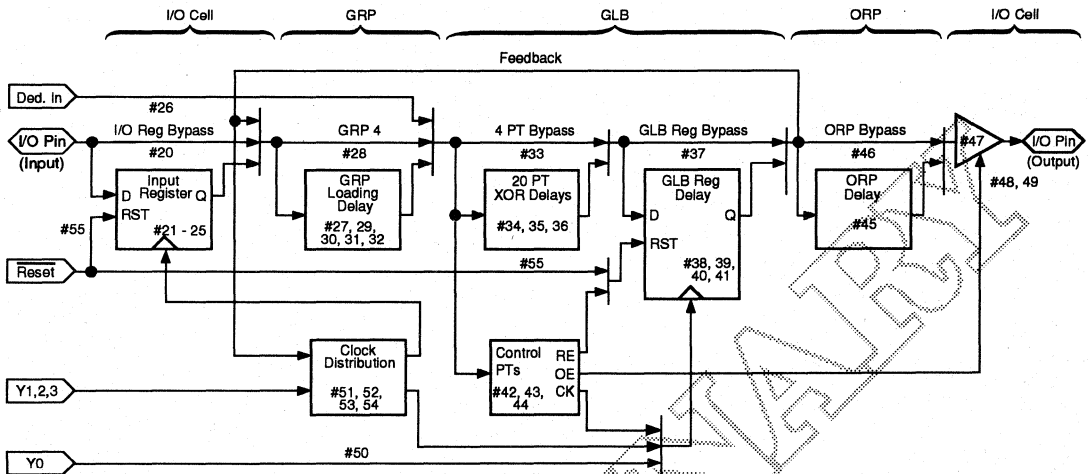| PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Inputs					
tiobp	20	I/O Register Bypass	–	4.0	ns
tiolat	21	I/O Latch Delay	–	5.3	ns
tiosu	22	I/O Register Setup Time before Clock	8.1	–	ns
tioh	23	I/O Register Hold Time after Clock	0.9	–	ns
tioco	24	I/O Register Clock to Out Delay	–	3.9	ns
tior	25	I/O Register Reset to Out Delay	–	4.6	ns
tdin	26	Dedicated Input Delay	–	8.0	ns
GRP					
tgrp1	27	GRP Delay, 1 GLB Load	–	3.3	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	4.0	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	5.3	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	6.7	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	8.0	ns
tgrp48	32	GRP Delay, 48 GLB Loads	–	21.3	ns
GLB					
t4ptbp	33	4 Product Term Bypass Path Delay	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	10.0	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	2.0	–	ns
tgh	39	GLB Register Hold Time after Clock	8.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	3.3	ns
tgr	41	GLB Register Reset to Output Delay	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	11.9	ns
tptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
torp	45	ORP Delay	–	4.7	ns
torpbp	46	ORP Bypass Delay	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50		UNITS
			MIN.	MAX.	
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI 1048/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(min))$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

7.4 ns = $(4.0 + 4.0 + 10.0) + (2.0) - (4.0 + 4.0 + 4.6)$

th = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

7.9 ns = $(4.0 + 4.0 + 9.9) + (8.0) - (4.0 + 4.0 + 10.0)$

tco = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

29.9 ns = $(4.0 + 4.0 + 9.9) + (3.3) + (4.7 + 4.0)$

Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0}(min) + t_{gco} + t_{gcp}(min))$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

8.7 ns = $(4.0 + 4.0 + 10.0) + (2.0) - (6.7 + 3.3 + 1.3)$

th = Clock (max) + Reg h - Logic

= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

6.6 ns = $(6.7 + 3.3 + 6.6) + (8.0) - (4.0 + 4.0 + 10.0)$

tco = Clock (max) + Reg co + Output

= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

28.6 ns = $(6.7 + 3.3 + 6.6) + (3.3) + (4.7 + 4.0)$

Pin Description

Name	PGA Pin Numbers						Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	J2, L2, M3, P4, N9, N11, M12, L14, F13, D13, C12, A11, B6, B4, C3, D1,	J3, K3, P2, M5 M9, M10, N14, K12, F12, E12, A13, C10, C6, C5, B1, E3,	K1, N1, N3, N5, P10, P13, M13, K13, E14, B14, B12, B10, A5, A2, C2, E2,	L1, M2, M4, P5, P11, N12, L12, K14, D14, C13, C11, A10, A4, B3, D3, E1,	K2, L3, P3, M6, N10, M11, M14, J12, E13, D12, A12, C9, B5, C4, C1, F3,	M1, P1, N4, N6, P12, P14, L13, J13, C14, A14, B11, B9, A3, A1, D2, F2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 5 IN 6 - IN 11	J1, F14,	P6, A9,	—, A8,	P8, —,	P9, A6,	J14, F1	Dedicated input pins to the device. (IN 2 and IN 9 not available)
RESET	H1						Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	G1						Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	G14						Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	H13						Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	H14						Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	B2, M8,	B8, N2,	B13, N8,	C8, N13	H3,	H12,	Ground (GND)
Vcc	B7, M7,	C7, N7	G2,	G3,	G12,	G13,	V_{cc}
NC	A7,	P7,	H2				These pins should be left floating, never connect these pins to ground.

Pin Configuration

pLSI 1048/883 PGA Pinout Diagram

pLSI 1048/883 BOTTOM VIEW

PIN A1

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O59	I/O61	I/O64	I/O66	I/O69	IN7	IN8	NC	IN10	I/O74	I/O75	I/O77	I/O80	I/O83	A
B	I/O56	GND	I/O62	I/O65	I/O68	I/O71	GND	Vcc	I/O72	I/O76	I/O78	IO81	GND	I/O85	B
C	I/O53	I/O57	I/O60	I/O63	I/O67	I/O70	GND	Vcc	I/O73	I/O79	I/O82	I/O84	I/O86	I/O88	C
D	I/O51	I/O54	I/O58					INDEX				I/O87	I/O89	I/O90	D
E	I/O50	I/O52	I/O55									I/O91	I/O92	I/O93	E
F	IN6	I/O48	I/O49									I/O94	I/O95	IN11	F
G	Y1	Vcc	Vcc									Vcc	Vcc	Y0	G
H	Y3	Y2	GND									GND	NC	RESET	H
J	IN5	I/O47	I/O46									I/O1	I/O0	IN0	J
K	I/O45	I/O44	I/O43									I/O7	I/O4	I/O2	K
L	I/O42	I/O41	I/O39									I/O10	I/O6	I/O3	L
M	I/O40	I/O38	I/O36	I/O34	I/O31	I/O25	GND	Vcc	I/O22	I/O19	I/O15	I/O12	I/O9	I/O5	M
N	I/O37	GND	I/O33	I/O30	I/O28	I/O24	GND	Vcc	I/O23	I/O20	I/O17	I/O14	GND	I/O8	N
P	I/O35	I/O32	I/O29	I/O27	I/O26	IN4	IN3	NC	IN1	I/O21	I/O18	I/O16	I/O13	I/O11	P

Package Diagram

132-Pin PGA

Dimensions in inches MIN./MAX.

Part Number Description

pLSI   1048 – XX   X   X   X

Device Family

Device Number

Speed
  50 = 50 MHz fmax

MIL Process /883 = 883 Process

Package
  G = 132-Pin PGA

Power
  L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
50	24	pLSI 1048-50LG/883	132-Pin PGA

::::Lattice

ispLSI™ 1016/883

in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the ispLSI 1016
  - Fully Compatible with Lattice's pLSI™ Military Family
  - High-Speed Global Interconnects
  - 32 I/O Pins, Four Dedicated Inputs
  - 96 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - fmax = 60 MHz Maximum Operating Frequency
  - tpd = 20 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**
  - pDS Software
    - Easy to Use PC Windows™ Interface
    - Boolean Logic Compiler
    - Manual Partitioning
    - Automatic Place and Route
    - Static Timing Table
  - pDS+™ Software
    - Industry Standard, Third Party Design Environments
    - Schematic Capture, State Machine, VHDL
    - Automatic Partitioning
    - Automatic Place and Route
    - Comprehensive Logic and Timing Simulation
    - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 ispLSI 1016 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016/883 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1016/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see figure 1). There are a total of 16 GLBs in the ispLSI 1016/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

September 1992. Rev. A

Absolute Maximum Ratings [1]

Supply Voltage V_{cc}. -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 150°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc + .1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	100	170	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t$_{iobp}$	20	I/O Register Bypass	–	2.7	ns
t$_{iolat}$	21	I/O Latch Delay	–	4.0	ns
t$_{iosu}$	22	I/O Register Setup Time before Clock	7.3	–	ns
t$_{ioh}$	23	I/O Register Hold Time after Clock	1.3	–	ns
t$_{ioco}$	24	I/O Register Clock to Out Delay	–	4.0	ns
t$_{ior}$	25	I/O Register Reset to Out Delay	–	3.3	ns
t$_{din}$	26	Dedicated Input Delay	–	5.3	ns
GRP					
t$_{grp1}$	27	GRP Delay, 1 GLB Load	–	2.0	ns
t$_{grp4}$	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t$_{grp8}$	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t$_{grp12}$	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t$_{grp16}$	31	GRP Delay, 16 GLB Loads	–	6.0	ns
GLB					
t$_{4ptbp}$	33	4 Product Term Bypass Path Delay	–	8.6	ns
t$_{1ptxor}$	34	1 Product Term/XOR Path Delay	–	9.3	ns
t$_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t$_{xoradj}$	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t$_{gbp}$	37	GLB Register Bypass Delay	–	1.3	ns
t$_{gsu}$	38	GLB Register Setup Time before Clock	1.3	–	ns
t$_{gh}$	39	GLB Register Hold Time after Clock	6.0	–	ns
t$_{gco}$	40	GLB Register Clock to Output Delay	–	2.7	ns
t$_{gr}$	41	GLB Register Reset to Output Delay	–	3.3	ns
t$_{ptre}$	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t$_{ptoe}$	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t$_{ptck}$	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t$_{orp}$	45	ORP Delay	–	3.3	ns
t$_{orpbp}$	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
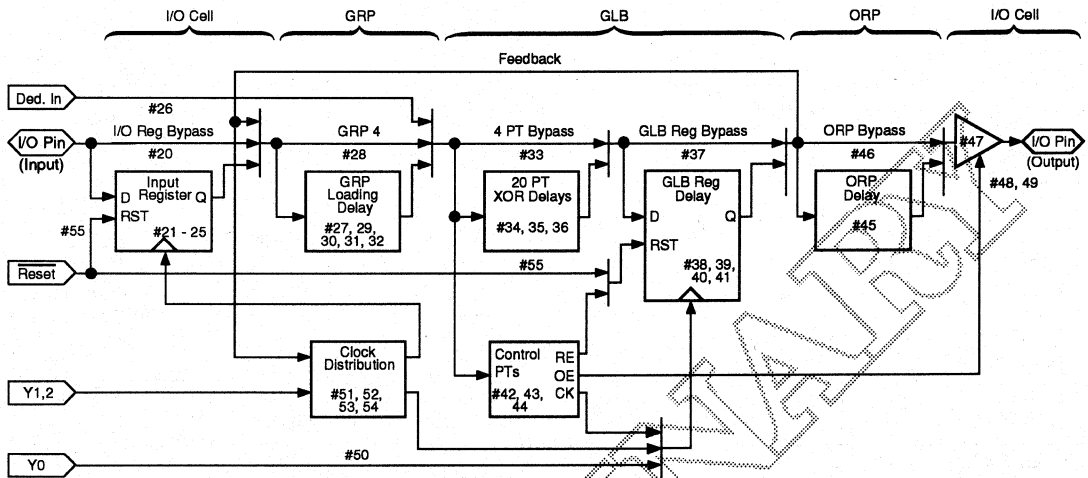2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1016/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6)$

th = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

5.3 ns = $(2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6)$

tco = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$

25.3 ns = $(2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)$

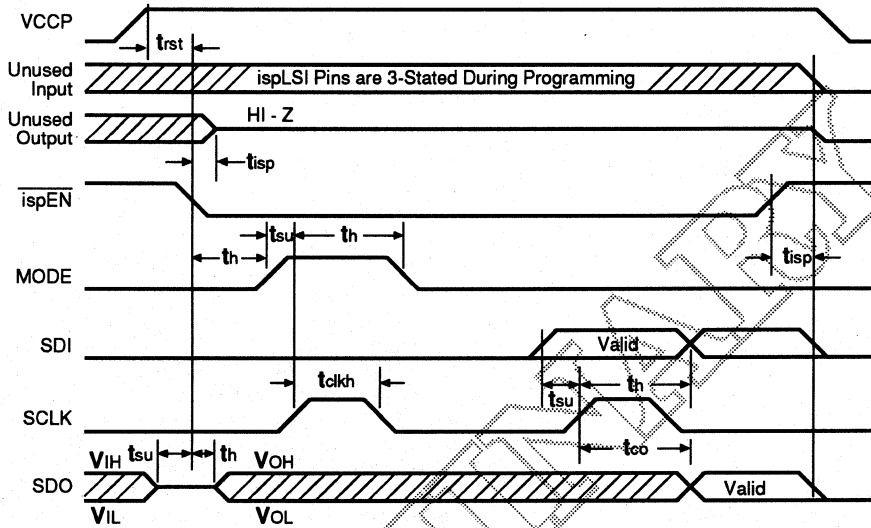### Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3)$

th = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

5.3 ns = $(6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6)$

tco = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

25.3 ns = $(6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)$
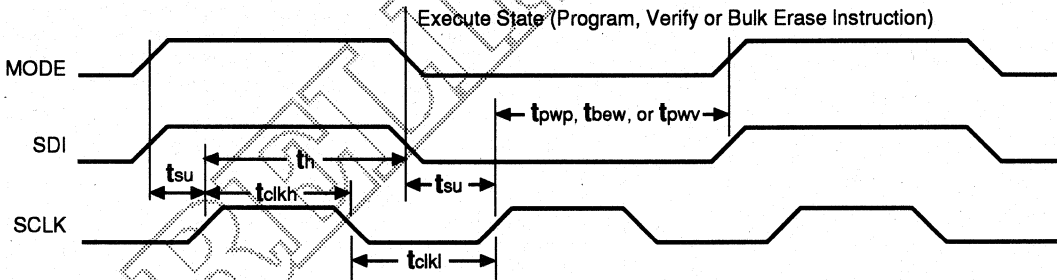
Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.5	5	5.5	V
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	μA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	μs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	μs
t_{su}	Setup Time		0.1	0.5	–	μs
t_{co}	Clock to Output		0.1	0.5	–	μs
t_h	Hold Time		0.1	0.5	–	μs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t_{pwv}	Verify Pulse Width		20	30	–	μs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	μs

Figure 3. Timing Waveforms for In-System Programming
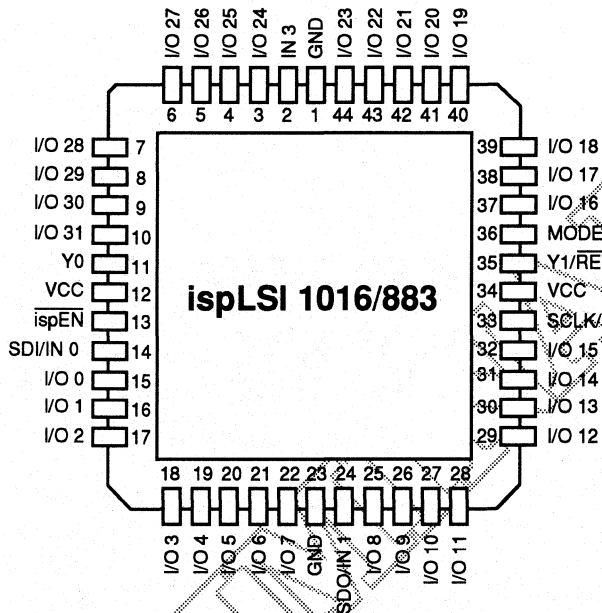

Figure 4. Program, Verify & Bulk Erase Waveforms

Pin Description

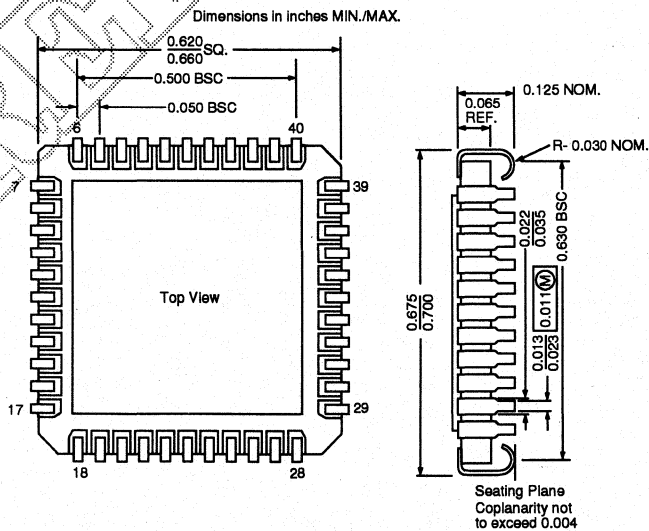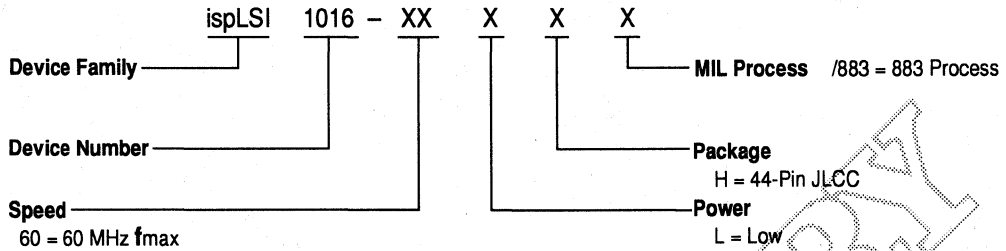| Name	JLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 3	2	Dedicated input pins to the device.
ispEN	13	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	14	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 2	36	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 1	24	Input/Output – This pin performs two functions. It is a dedicated clock input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/Y2	33	Input – This pin performs two functions. It is a dedicated clock input when ispEN is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/RESET	35	This pin performs two functions: – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND **V**CC	1, 23 12, 34	Ground (GND) V_{cc}

Pin Configuration

ispLSI 1016/883 JLCC Pinout Diagram

Package Diagram

44-Pin JLCC

Dimensions in inches MIN./MAX.

Top View

0.620/0.660 SQ.
0.500 BSC
0.050 BSC

0.125 NOM.
0.065 REF.
R- 0.030 NOM.
0.022/0.035
0.630 BSC
0.013/0.023
0.011 Ⓜ
0.675/0.700

Seating Plane
Coplanarity not
to exceed 0.004

Part Number Description

ispLSI   1016 – XX   X   X   X

Device Family

Device Number

Speed
  60 = 60 MHz fmax

MIL Process   /883 = 883 Process

Package
  H = 44-Pin JLCC

Power
  L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1016-60LH/883	44-Pin JLCC

::::: Lattice

ispLSI™ 1024/883

in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the ispLSI 1024
  - Fully Compatible with Lattice's pLSI™ Military Family
  - High-Speed Global Interconnects
  - 48 I/O Pins, Six Dedicated Inputs
  - 144 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Fast Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 60 MHz Maximum Operating Frequency
  - t_{pd} = 20 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX- IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table

  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 ispLSI 1024 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1024/883 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1024/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see figure 1). There are a total of 24 GLBs in the ispLSI 1024/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

September 1992. Rev. A

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 150°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications [0]

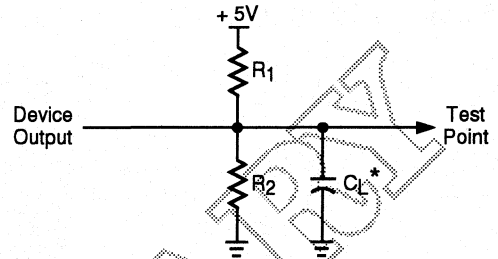| PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load

$^*C_L$ includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	—	—	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
$I_{IL\text{-}isp}$	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)	—	—	-150	μA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	—	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	—	130	215	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using six 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	24	ns
t_{dis}	3	15	Input to Output Disable	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

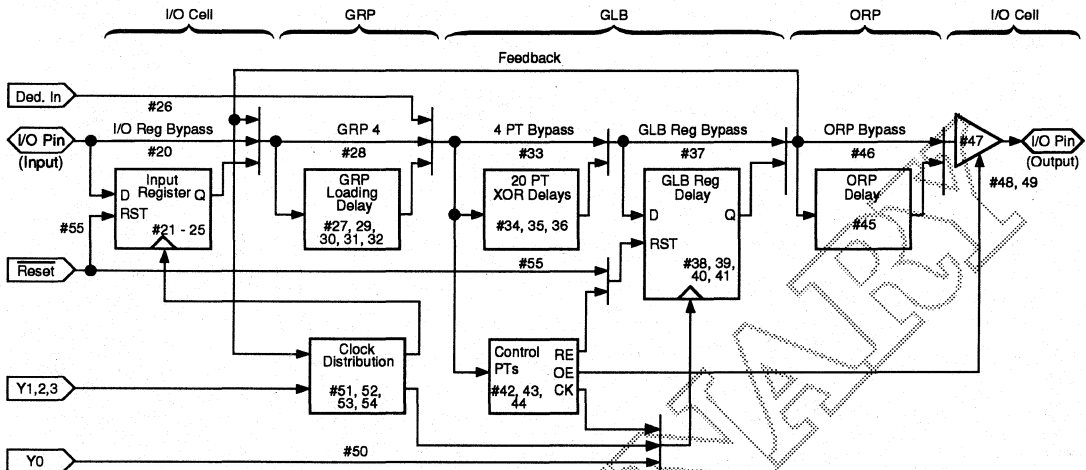| PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t iobp	20	I/O Register Bypass	—	2.7	ns
t iolat	21	I/O Latch Delay	—	4.0	ns
t iosu	22	I/O Register Setup Time before Clock	7.3	—	ns
t ioh	23	I/O Register Hold Time after Clock	1.3	—	ns
t ioco	24	I/O Register Clock to Out Delay	—	4.0	ns
t ior	25	I/O Register Reset to Out Delay	—	3.3	ns
t din	26	Dedicated Input Delay	—	5.3	ns
GRP					
t grp1	27	GRP Delay, 1 GLB Load	—	2.0	ns
t grp4	28	GRP Delay, 4 GLB Loads	—	2.7	ns
t grp8	29	GRP Delay, 8 GLB Loads	—	4.0	ns
t grp12	30	GRP Delay, 12 GLB Loads	—	5.0	ns
t grp16	31	GRP Delay, 16 GLB Loads	—	6.0	ns
t grp24	32	GRP Delay, 24 GLB Loads	—	8.3	ns
GLB					
t 4ptbp	33	4 Product Term Bypass Path Delay	—	8.6	ns
t 1ptxor	34	1 Product Term/XOR Path Delay	—	9.3	ns
t 20ptxor	35	20 Product Term/XOR Path Delay	—	10.6	ns
t xoradj	36	XOR Adjacent Path Delay[3]	—	12.7	ns
t gbp	37	GLB Register Bypass Delay	—	1.3	ns
t gsu	38	GLB Register Setup Time before Clock	1.3	—	ns
t gh	39	GLB Register Hold Time after Clock	6.0	—	ns
t gco	40	GLB Register Clock to Output Delay	—	2.7	ns
t gr	41	GLB Register Reset to Output Delay	—	3.3	ns
t ptre	42	GLB Product Term Reset to Register Delay	—	13.3	ns
t ptoe	43	GLB Product Term Output Enable to I/O Cell Delay	—	12.0	ns
t ptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t orp	45	ORP Delay	—	3.3	ns
t orpbp	46	ORP Bypass Delay	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1024/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(min))$
= (#20 + #28 + #35) + (#38) - (#20 + #28 + #44)
7.3 ns = (2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6)

th = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#20 + #28 + #44) + (#39) - (#20 + #28 + #35)
5.3 ns = (2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6)

tco = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#20 + #28 + #44) + (#40) + (#45 + #47)
25.3 ns = (2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)

Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0}(min) + t_{gco} + t_{gcp}(min))$
= (#20 + #28 + #35) + (#38) - (#50 + #40 + #52)
7.3 ns = (2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3)

th = Clock (max) + Reg h - Logic
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#50 + #40 + #52) + (#39) - (#20 + #28 + #35)
5.3 ns = (6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6)

tco = Clock (max) + Reg co + Output
= $(t_{gy0}(max) + t_{gco} + t_{gcp}(max)) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#50 + #40 + #52) + (#40) + (#45 + #47)
25.3 ns = (6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.5	5	5.5	V
I_{CCP}	Programming Supply Current	ispEN = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	ispEN to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 3. Timing Waveforms for In-System Programming
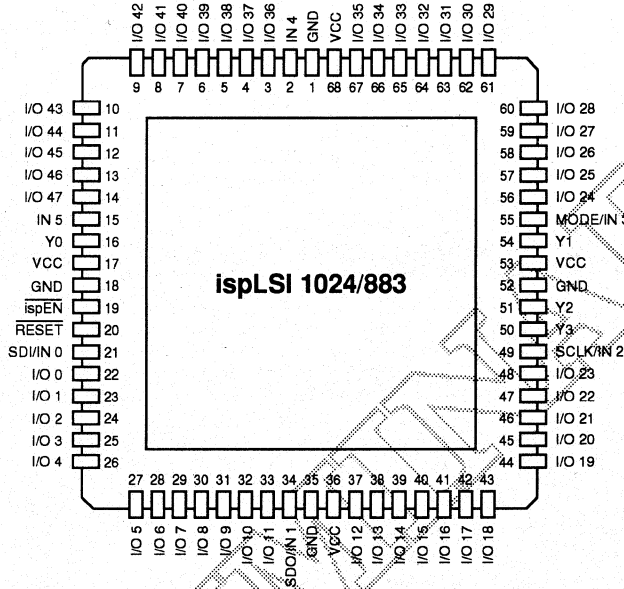

Figure 4. Program, Verify & Bulk Erase Waveforms

Pin Description

Name	JLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 5	2, 15	Dedicated input pins to the device.
ispEN	19	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	21	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 3	55	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 1	34	Input/Output – This pin performs two functions. It is a dedicated clock input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 2	49	Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	20	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND V_{CC}	1, 18, 35, 52 17, 36, 53, 68	Ground (GND) V_{cc}

Pin Configuration

ispLSI 1024/883 JLCC Pinout Diagram

Package Diagram

68-Pin JLCC

Dimensions in inches MIN./MAX.

Part Number Description

```
ispLSI    1024  –  XX    X    X    X
```

Device Family ——————┘

Device Number ————————————┘

Speed ——————————————————————————————┘
  60 = 60 MHz fmax

MIL Process /883 = 883 Process

Package
  H = 68-Pin JLCC

Power
  L = Low
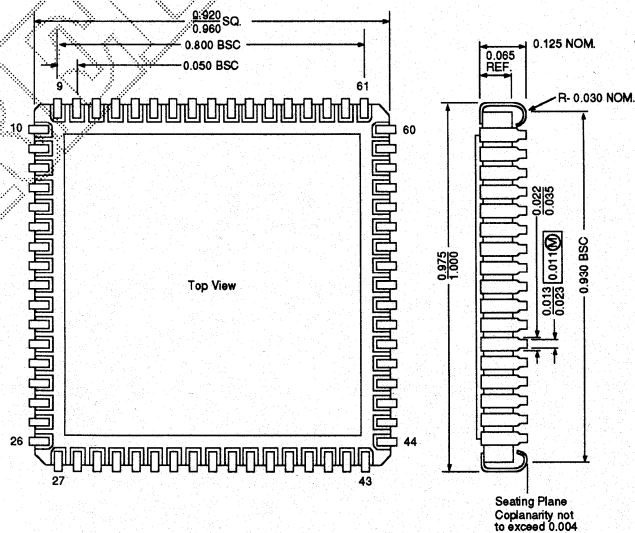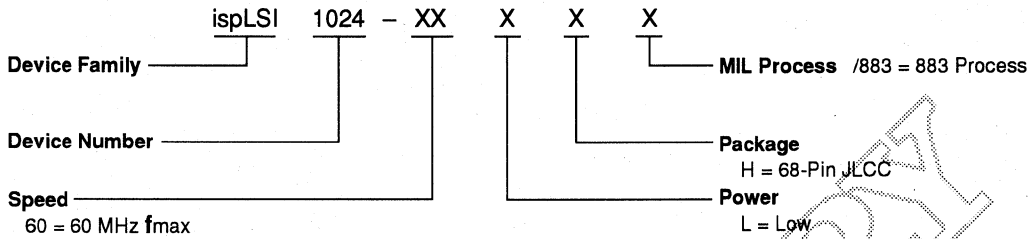
Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1024-60LH/883	68-Pin JLCC

:::Lattice

isplLSI™ 1032/883

in-system programmable Large Scale Integration
High-Denisty Programmable Logic

Features

- **IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC**
  - MIL-STD-883 Version of the ispLSI 1032
  - Fully Compatible with Lattice's pLSI™ Military Family
  - High Speed Global Interconnects
  - 64 I/O Pins, Eight Dedicated Inputs
  - 192 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - f_{max} = 60 MHz Maximum Operating Frequency
  - t_{pd} = 20 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED of PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)**
  - pDS Software
    - Easy to Use Windows™ Interface
    - Boolean Logic Compiler
    - Manual Partitioning
    - Automatic Place and Route
    - Static Timing Table
  - pDS+™ Software
    - Industry Standard, Third Party Design Environments
    - Schematic Capture, State Machine, VHDL
    - Automatic Partitioning
    - Automatic Place and Route
    - Comprehensive Logic and Timing Simulation
    - PC and Workstation Platforms

Functional Block Diagram
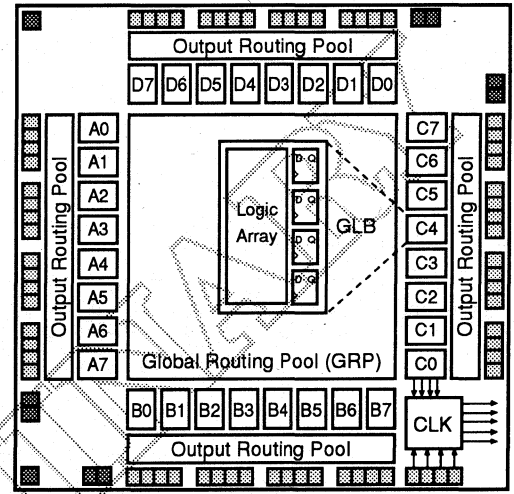
Description

The Lattice MIL-STD-883 ispLSI 1032 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032/883 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1032/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

September 1992. Rev. A

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . . -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . . -2.5 to V_{CC} +1.0V

Storage Temperature . . . . -65 to 150°C

Ambient Temp. with Power Applied . . . . -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.
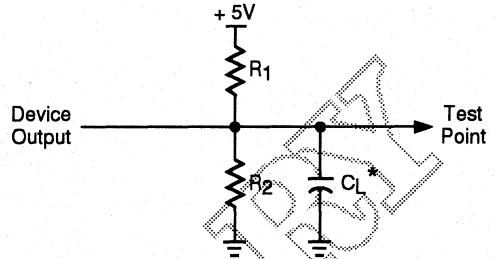
Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{IL}-isp	isp input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-150	μA
I_{IL}-PU	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	135	220	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST [5] COND.	# [2]	DESCRIPTION[1]	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	20	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	—	25	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	60	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	38	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle[4]	83	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	—	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	—	13	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	13	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	16	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	—	22.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	13	—	ns
t_{en}	2	14	Input to Output Enable	—	24	ns
t_{dis}	3	15	Input to Output Disable	—	24	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	6	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	6	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
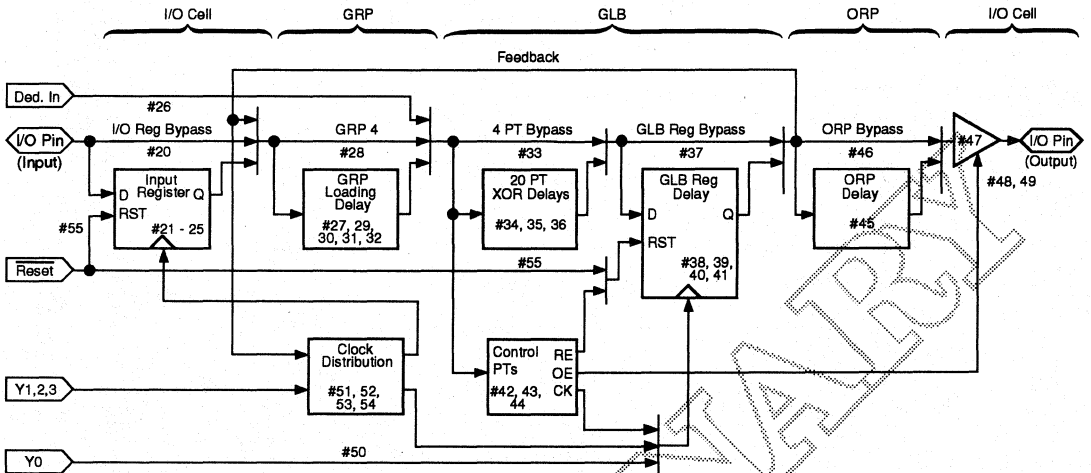5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60 MIN.	-60 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	5.3	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	10.6	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-60		UNITS
			MIN.	MAX.	
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1032/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

tsu   =   Logic + Reg su - Clock (min)

      = $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

      = $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6)$

th   =   Clock (max) + Reg h - Logic

      = $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

      = $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

5.3 ns = $(2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6)$

tco   =   Clock (max) + Reg co + Output

      = $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

      = $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
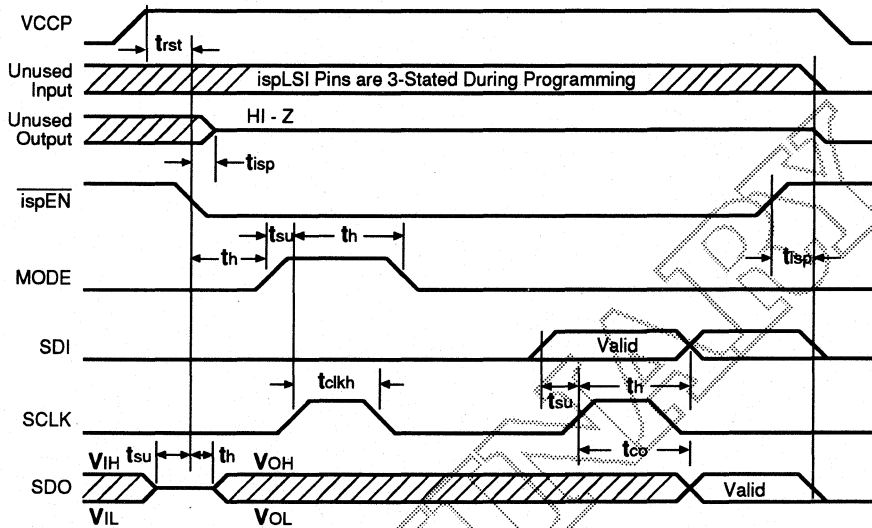
25.3 ns = $(2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)$

Derivations of tsu, th and tco from the Clock GLB

tsu   =   Logic + Reg su - Clock (min)

      = $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

      = $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

7.3 ns = $(2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3)$

th   =   Clock (max) + Reg h - Logic

      = $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

      = $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

5.3 ns = $(6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6)$

tco   =   Clock (max) + Reg co + Output

      = $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

      = $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

25.3 ns = $(6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)$
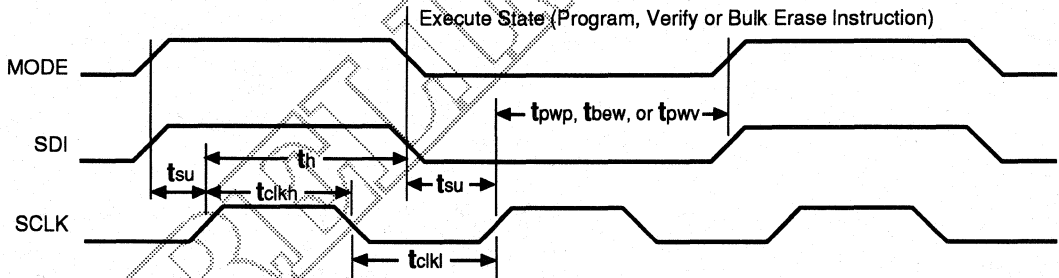
Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.5	5	5.5	V
I_{CCP}	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{isp}	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 3. Timing Waveforms for In-System Programming
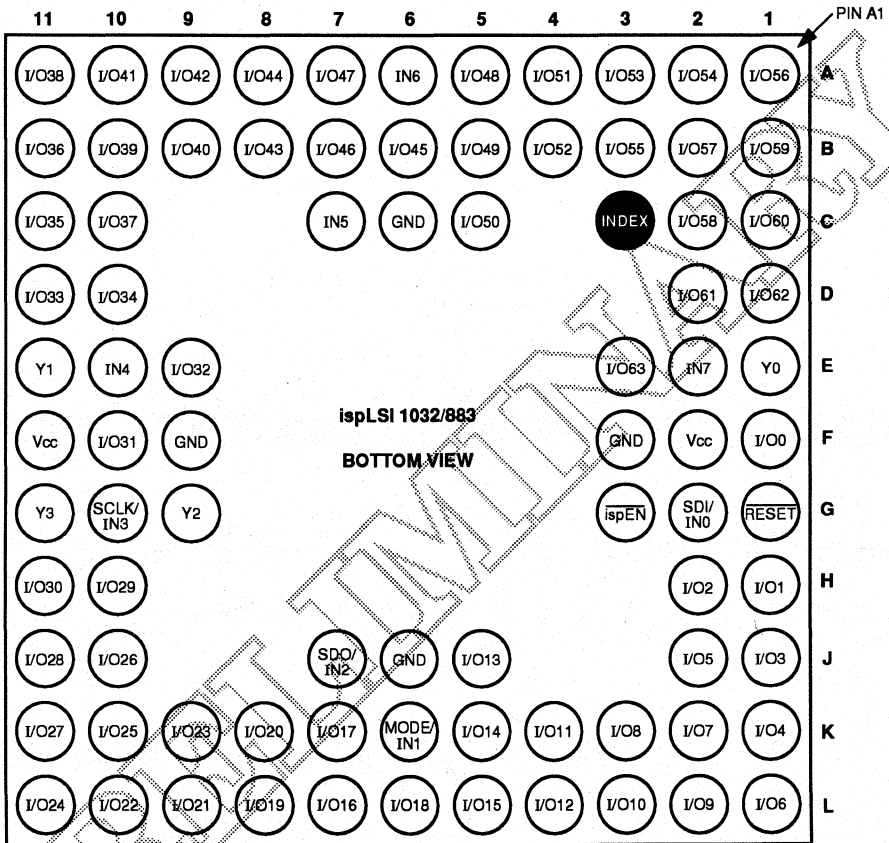

Figure 4. Program, Verify & Bulk Erase Waveforms

Pin Description

Name	PGA Pin Numbers				Description
I/O 0 - I/O 3	F1,	H1,	H2,	J1,	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
I/O 4 - I/O 7	K1,	J2,	L1,	K2,	
I/O 8 - I/O 11	K3,	L2,	L3,	K4,	
I/O 12 - I/O 15	L4,	J5,	K5,	L5,	
I/O 16 - I/O 19	L7,	K7,	L6,	L8,	
I/O 20 - I/O 23	K8,	L9,	L10,	K9,	
I/O 24 - I/O 27	L11,	K10,	J10,	K11,	
I/O 28 - I/O 31	J11,	H10,	H11,	F10,	
I/O 32 - I/O 35	E9,	D11,	D10,	C11,	
I/O 36 - I/O 39	B11,	C10,	A11,	B10,	
I/O 40 - I/O 43	B9,	A10,	A9,	B8,	
I/O 44 - I/O 47	A8,	B6,	B7,	A7,	
I/O 48 - I/O 51	A5,	B5,	C5,	A4,	
I/O 52 - I/O 55	B4,	A3,	A2,	B3,	
I/O 56 - I/O 59	A1,	B2,	C2,	B1,	
I/O 60 - I/O 63	C1,	D2,	D1,	E3	
IN 4 - IN 7	E10,	C7,	A6,	E2	Dedicated input pins to the device.
ispEN	G3				Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	G2				Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1	K6				Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2	J7				Input/Output – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3	G10				Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	G1				Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1				Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11				Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	C6,	F3,	F9,	J6	Ground (GND)
V_{CC}	F2,	F11			V_{cc}

Lattice

Pin Configuration

ispLSI 1032/883 PGA Pinout Diagram

```
        11     10      9      8      7      6      5      4      3      2      1    PIN A1

A     I/O38  I/O41  I/O42  I/O44  I/O47   IN6   I/O48  I/O51  I/O53  I/O54  I/O56

B     I/O36  I/O39  I/O40  I/O43  I/O46  I/O45  I/O49  I/O52  I/O55  I/O57  I/O59

C     I/O35  I/O37                 IN5    GND   I/O50              INDEX  I/O58  I/O60

D     I/O33  I/O34                                                      I/O61  I/O62

E      Y1     IN4   I/O32                                        I/O63   IN7    Y0

F      Vcc   I/O31   GND                                          GND    Vcc    I/O0

G      Y3    SCLK/   Y2                                          ispEN  SDI/   RESET
              IN3                                                        IN0

H     I/O30  I/O29                                                      I/O2   I/O1

J     I/O28  I/O26                SDO/    GND   I/O13                    I/O5   I/O3
                                  IN2

K     I/O27  I/O25  I/O23  I/O20  I/O17  MODE/  I/O14  I/O11  I/O8   I/O7   I/O4
                                         IN1

L     I/O24  I/O22  I/O21  I/O19  I/O16  I/O18  I/O15  I/O12  I/O10  I/O9   I/O6
```

ispLSI 1032/883

BOTTOM VIEW

5

Package Diagram

84-Pin PGA

Dimensions in inches MIN./MAX.

Part Number Description

| | Device Family | ispLSI | | | | | | |

Device Family — ispLSI

Device Number — 1032

Speed — XX
60 = 60 MHz fmax

MIL Process /883 = 883 Process

Package
G = 84-Pin PGA

Power
L = Low

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
60	20	ispLSI 1032-60LG/883	84-Pin PGA

≡≡Lattice

ispLSI™ 1048/883

in-system programmable Large Scale Integration
High-Density Programmable Logic

Features

- IN-SYSTEM PROGRAMMABLE HIGH-DENSITY LOGIC
  - MIL-STD-883 Version of the ispLSI 1048
  - Fully Compatible with Lattice's pLSI™ Military Family
  - High-Speed Global Interconnects
  - 96 I/O Pins, Ten Dedicated Inputs
  - 288 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - fmax = 50 MHz Maximum Operating Frequency
  - tpd = 24 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
- IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable with High Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- pLSI/ispLSI DEVELOPMENT SYSTEM (pDS™)
  pDS Software
  - Easy to Use PC Windows™ Interface
  - Boolean Logic Compiler
  - Manual Partitioning
  - Automatic Place and Route
  - Static Timing Table
  pDS+™ Software
  - Industry Standard, Third Party Design Environments
  - Schematic Capture, State Machine, VHDL
  - Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram

Description

The Lattice MIL-STD-883 ispLSI 1048 is a High-Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048/883 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1048/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the ispLSI 1048/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

September 1992. Rev. A

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. . . . . -0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 150°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	–	–	10	μA
I_{IL-isp}	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)	–	–	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	165	260	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_c = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	—	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	53.6	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	31.3	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle[4]	71.4	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	12	—	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	—	16	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	16	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	18.7	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	—	22.7	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	13	—	ns
t_{en}	2	14	Input to Output Enable	—	26.7	ns
t_{dis}	3	15	Input to Output Disable	—	26.7	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	7	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	7	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.7	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.7	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

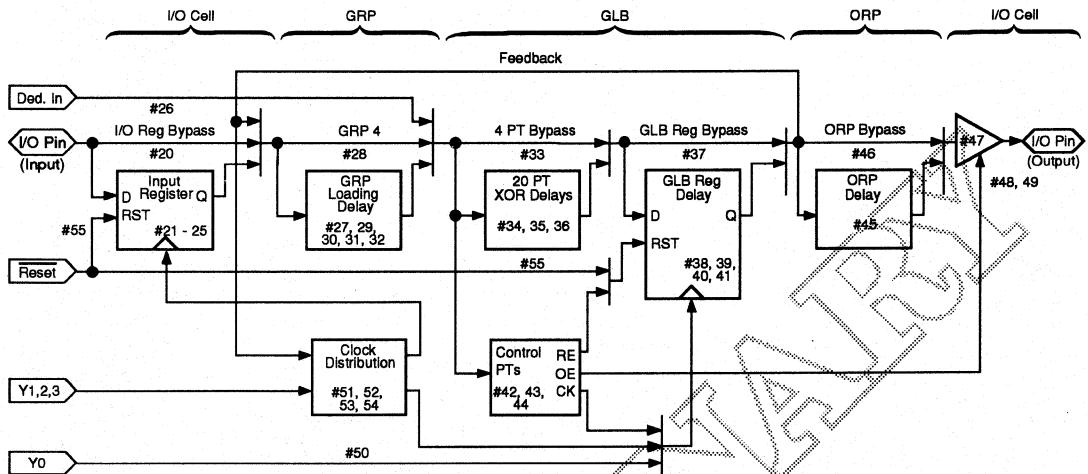| PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Inputs					
t_{iobp}	20	I/O Register Bypass	–	4.0	ns
t_{iolat}	21	I/O Latch Delay	–	5.3	ns
t_{iosu}	22	I/O Register Setup Time before Clock	8.1	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	0.9	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.9	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	4.6	ns
t_{din}	26	Dedicated Input Delay	–	8.0	ns
GRP					
t_{grp1}	27	GRP Delay, 1 GLB Load	–	3.3	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	4.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	5.3	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	6.7	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	8.0	ns
t_{grp48}	32	GRP Delay, 48 GLB Loads	–	21.3	ns
GLB					
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	10.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	2.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	8.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	3.3	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	11.9	ns
t_{ptck}	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
t_{orp}	45	ORP Delay	–	4.7	ns
t_{orpbp}	46	ORP Bypass Delay	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1048/883 Timing Model

Derivations of tsu, th and tco from the Product Term Clock

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$

7.4 ns = $(4.0 + 4.0 + 10.0) + (2.0) - (4.0 + 4.0 + 4.6)$

t_h = Clock (max) + Reg h - Logic

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$

7.9 ns = $(4.0 + 4.0 + 9.9) + (8.0) - (4.0 + 4.0 + 10.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
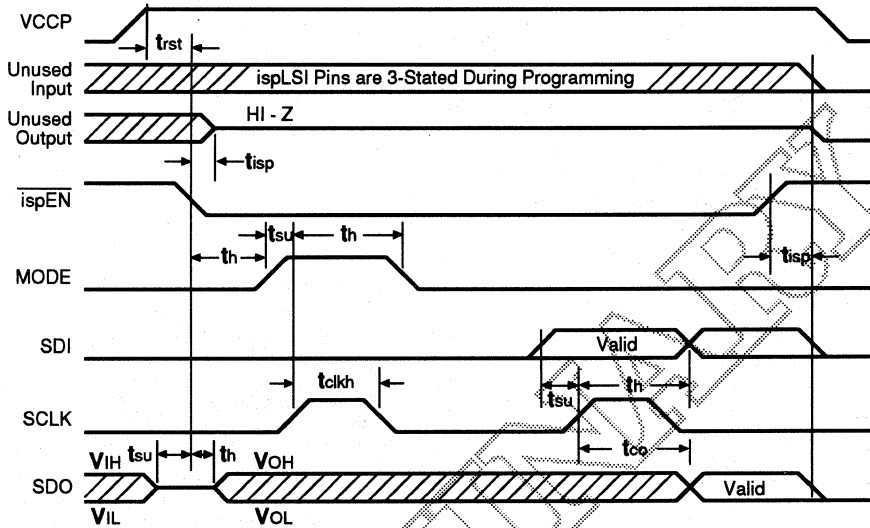
29.9 ns = $(4.0 + 4.0 + 9.9) + (3.3) + (4.7 + 4.0)$

Derivations of tsu, th and tco from the Clock GLB

t_{su} = Logic + Reg su - Clock (min)

= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$

= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$

8.7 ns = $(4.0 + 4.0 + 10.0) + (2.0) - (6.7 + 3.3 + 1.3)$

t_h = Clock (max) + Reg h - Logic

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$

= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$

6.6 ns = $(6.7 + 3.3 + 6.6) + (8.0) - (4.0 + 4.0 + 10.0)$

t_{co} = Clock (max) + Reg co + Output

= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$

= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$

28.6 ns = $(6.7 + 3.3 + 6.6) + (3.3) + (4.7 + 4.0)$
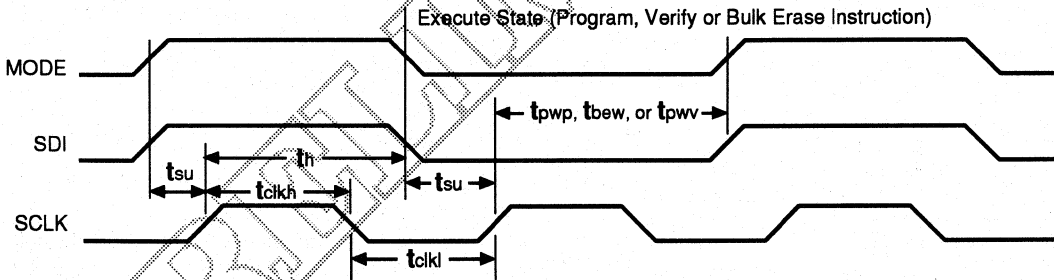
Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V$_{CCP}$	Programming Voltage		4.5	5	5.5	V
I$_{CCP}$	Programming Supply Current	$\overline{ispEN}$ = Low	–	50	100	mA
V$_{IHP}$	Input Voltage High		2.0	–	V$_{CCP}$	V
V$_{ILP}$	Input Voltage Low		0	–	0.8	V
I$_{IP}$	Input Current		–	100	200	µA
V$_{OHP}$	Output Voltage High	I$_{OH}$ = -3.2 mA	2.4	–	V$_{CCP}$	V
V$_{OLP}$	Output Voltage Low	I$_{OL}$ = 5 mA	0	–	0.5	V
t$_r$, t$_f$	Input Rise and Fall		–	–	0.1	µs
t$_{isp}$	$\overline{ispEN}$ to Output 3-State		–	2	10	µs
t$_{su}$	Setup Time		0.1	0.5	–	µs
t$_{co}$	Clock to Output		0.1	0.5	–	µs
t$_h$	Hold Time		0.1	0.5	–	µs
t$_{clkh}$, t$_{clkl}$	Clock Pulse Width, High and Low		0.5	1	–	µs
t$_{pwv}$	Verify Pulse Width		20	30	–	µs
t$_{pwp}$	Programming Pulse Width		40	–	100	ms
t$_{bew}$	Bulk Erase Pulse Width		200	–	–	ms
t$_{rst}$	Reset Time From Valid V$_{CCP}$		45	–	–	µs

Figure 3. Timing Waveforms for In-System Programming

Figure 4. Program, Verify & Bulk Erase Waveforms

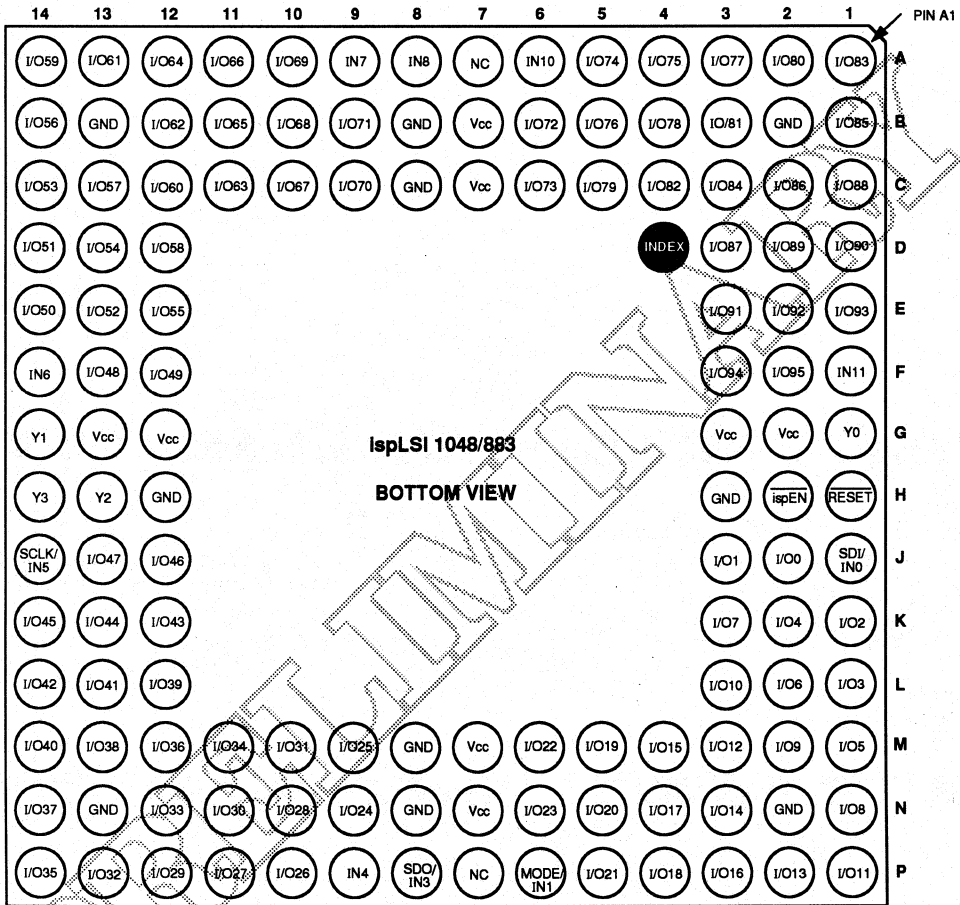## Pin Description

Name	PGA Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	J2, J3, K1, L1, K2, M1, L2, K3, N1, M2, L3, P1, M3, P2, N3, M4, P3, N4, P4, M5, N5, P5, M6, N6, N9, M9, P10, P11, N10, P12, N11, M10, P13, N12, M11, P14, M12, N14, M13, L12, M14, L13, L14, K12, K13, K14, J12, J13, F13, F12, E14, D14, E13, C14, D13, E12, B14, C13, D12, A14, C12, A13, B12, C11, A12, B11, A11, C10, B10, A10, C9, B9, B6, C6, A5, A4, B5, A3, B4, C5, A2, B3, C4, A1, C3, B1, C2, D3, C1, D2, D1, E3, E2, E1, F3, F2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 IN 6 - IN 11	P9 F14, A9, A8, —, A6, F1	Dedicated input pins to the device. (IN 2 and IN 9 not available)
ispEN	H2	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	J1	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1	P6	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 3	P8	Input/Output – This pin performs two functions. It is a dedicated clock input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 5	J14	Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	H1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	G1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	G14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	H13	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	H14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	B2, B8, B13, C8, H3, H12, M8, N2, N8, N13	Ground (GND)
VCC	B7, C7, G2, G3, G12, G13, M7, N7	V_{cc}
NC	A7, P7	These pins should be left floating, never connect these pins to ground.

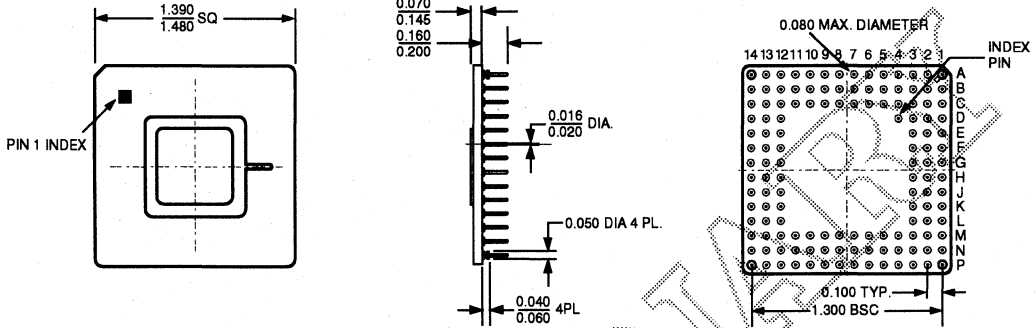## Pin Configuration
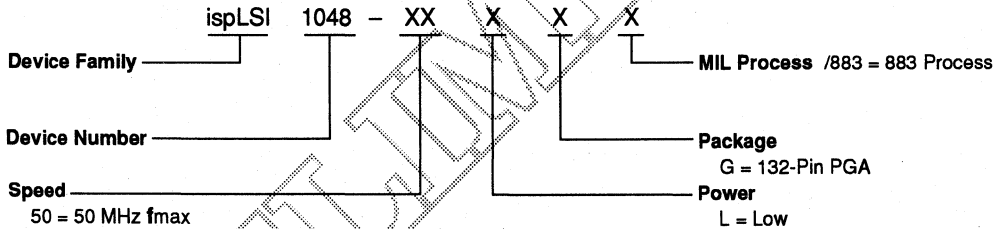
ispLSI 1048/883 PGA Pinout Diagram

PIN A1

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O59	I/O61	I/O64	I/O66	I/O69	IN7	IN8	NC	IN10	I/O74	I/O75	I/O77	I/O80	I/O83	A
B	I/O56	GND	I/O62	I/O65	I/O68	I/O71	GND	Vcc	I/O72	I/O76	I/O78	IO/81	GND	I/O85	B
C	I/O53	I/O57	I/O60	I/O63	I/O67	I/O70	GND	Vcc	I/O73	I/O79	I/O82	I/O84	I/O86	I/O88	C
D	I/O51	I/O54	I/O58					INDEX				I/O87	I/O89	I/O90	D
E	I/O50	I/O52	I/O55									I/O91	I/O92	I/O93	E
F	IN6	I/O48	I/O49									I/O94	I/O95	IN11	F
G	Y1	Vcc	Vcc									Vcc	Vcc	Y0	G
H	Y3	Y2	GND		ispLSI 1048/883							GND	ispEN	RESET	H
J	SCLK/IN5	I/O47	I/O46		BOTTOM VIEW							I/O1	I/O0	SDI/IN0	J
K	I/O45	I/O44	I/O43									I/O7	I/O4	I/O2	K
L	I/O42	I/O41	I/O39									I/O10	I/O6	I/O3	L
M	I/O40	I/O38	I/O36	I/O34	I/O31	I/O25	GND	Vcc	I/O22	I/O19	I/O15	I/O12	I/O9	I/O5	M
N	I/O37	GND	I/O33	I/O30	I/O28	I/O24	GND	Vcc	I/O23	I/O20	I/O17	I/O14	GND	I/O8	N
P	I/O35	I/O32	I/O29	I/O27	I/O26	IN4	SDO/IN3	NC	MODE/IN1	I/O21	I/O18	I/O16	I/O13	I/O11	P

5

Package Diagram

132-Pin PGA

Dimensions in inches MIN./MAX.

Part Number Description

ispLSI   1048 – XX   X   X   X

Device Family

Device Number

Speed
50 = 50 MHz fmax

Power
L = Low

Package
G = 132-Pin PGA

MIL Process /883 = 883 Process

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
50	24	ispLSI 1048-50LG/883	132-Pin PGA

Section 1: Introduction to pLSI and ispLSI
Section 2: pLSI and ispLSI Architectural Description
Section 3: pLSI Data Sheets
Section 4: ispLSI Data Sheets
Section 5: Military pLSI and ispLSI Data Sheets
Section 6: General Information

6

Package Thermal Resistance

The following table provides information on the package thermal resistance of Lattice pLSI and ispLSI Commercial and Industrial grade devices. For information on the package thermal resistance of Lattice Military grade devices, please refer to MIL-STD-1835.

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction to Ambient Thermal Resistance Measurements of IC Packages" with devices mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages".

Package Thermal Resistance

Commercial/Industrial Grade Devices

Package	Device Type	θ_{JA}	θ_{JC}
44-pin PLCC	pLSI 1016 ispLSI 1016	50° C/W	16° C/W
68-pin PLCC	pLSI 1024 ispLSI 1024	45° C/W	13° C/W
84-pin PLCC	pLSI 1032 ispLSI 1032	42° C/W	12° C/W
120-pin PQFP	pLSI 1048 ispLSI 1048	55° C/W	18° C/W

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