LOGIC

DEVICES INCORPORATED

FastCMOS

Data Book

March 1989

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Revison A

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Introduction

Logic Devices is committed to providing value to its customers by offering the highest performance products available, with continuously improving price/performance and quality levels. To do this, we bring to bear submicron CMOS technology on a par with the most advanced production processes in the world, coupled with an engineering capability which is known and respected throughout our industry. In recent years, Logic Devices has diversified its product offering in an attempt to supply total solutions; high-performance logic products, peripheral products, and memory, with more to come. This allows us to provide a greater percentage of the overall solution to our customers.

We are proud to present this new edition of the Logic Devices Product Catalog, containing our full line of some 45 different logic, memory and peripheral devices. Logic Devices products bring new levels of performance to a wide range of application environments, including general-purpose computing, DSP and image processing, computer peripherals, and embedded control. All data sheets have been revised and reformatted for this edition of the catalog, and several new reference sections have been added for your assistance.

Section 2 on Memory Products features our new family of high speed 16K and 64K-bit SRAMs. Already among the highest performance devices of their density, these products are continuously augmented by yet faster and denser devices.

Of special note in Section 3 - Logic Products are several new products now in advanced development, the L29C524/525 Dual Pipeline Register, the L10C11 Variable Length Shift Register and the L29C818 Serial Scan Register. Section 4; Peripheral Products describes the L5380/L53C80 CMOS SCSI Controllers. These continue to be among the fastest, lowest power SCSI Controllers on the market today.

New for this edition are Sections 5 & 6 providing background and reference information on the topics of Quality & Reliability, Latch Up, ESD Protection and Power Dissipation. Of related interest is Section 7 on Packaging which in addition to providing dimensional information on all available package types, includes a detailed discussion of thermal considerations. Application Notes and Technical Article reprints reside in Section 8 & 9 and feature solutions to typical design problems.

Lastly, if further information is required, please contact your local Logic Devices sales office. Logic Devices locations worldwide are listed in Section 10, conveniently located at the end of the catalog.

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Memory Products

Logic Products

Peripheral Products

Quality and Reliability

Technology and Design Features

Packaging

Application Notes

Technical Articles

Sales Offices

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Part Numbering System

To construct a valid part number:

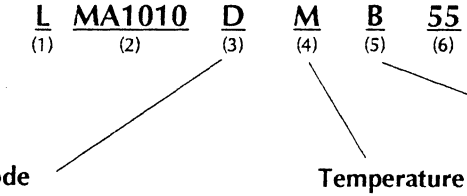
In order to construct a valid Logic Devices part number, begin with the generic number obtained from the datasheet header or the product selection guide. To this number, append three characters from the tables below indicating the desired package code, temperature range, and screening. Finally, append zero, one, or two digits indicating the performance grade desired. Most devices are offered in several speed grades with the part number suffix indicating a critical path delay in nanoseconds.

For more information on available part numbers:

All products are not offered with all combinations of package style, temperature range, and screening. The Ordering Information table on the last page of each product datasheet indicates explicitly all valid combinations of package, temperature, screening, and performance codes for a given product.

For more information on package options:

Also given in the Ordering Information tables in each product datasheet are the Logic Devices package codes. These are two character codes consisting of a letter designating a package type, and a number distinguishing the individual package drawing. Drawings giving detailed dimensions and tolerances for each package code can be found in the Mechanical Data section of this catalog. For example, the LMA1010DMB55 given below refers to a "D" or sidebraze, hermetic DIP package. The LMA1010/2010 datasheet indicates that the actual package used is D6. In the Mechanical Data section package type D6 is seen to be a 64-pin, cavity-down, sidebraze, hermetic DIP.



Key:
(1) Prefix, Logic Devices, Inc.
(2) Device number
(3) Package code
(4) Temperature range
(5) Screening
(6) Performance/speed

Package Code

Suffix	Description
C, I*	CerDIP
D, H*	Sidebraze, Hermetic DIP
F	Ceramic Flat Pack
G	Ceramic Pin Grid Array
J	Plastic J-Lead Chip Carrier
K	Ceramic Leadless Chip Carrier
L	Ceramic Leaded Chip Carrier
P, N*	Plastic DIP
U, V*	Plastic SOIC (Gull-Wing)
W	Plastic SOJ (J-Lead)
X	Dice

Temperature Range

Suffix	Description
C	Commercial 0°C to +70°C
M	Military −55°C to +125°C

Screening

Suffix	Description
No Designator	Commercial Flow
R	48 Hour Burn-in at 125°C
E	Extended Screening
B	MIL-STD-883 Class B Compliant

*Some devices are available in packages of two widths. For devices available in a single width, C, D, P, and V are used.

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Contents

Static RAM Package Availability Guide

Type >		Plastic DIP		Sidebraze Hermetic DIP		CerDIP		SOIC (Gull-wing)		SOJ (J-lead)	Ceramic LCC			
Package Code >		P	N	C	H	C	I	U	V	W	K			
	Width >	0.3"	0.6"	0.3"	0.6"	0.3"	0.6"	0.300"	0.331"	0.300"	290 x 425	290 x 490	450 x 450	350 x 550
Part No.	No. Pins													
16K														
L7C167	20	●		●		●		●		●	●			
L7C168	20	●		●		●		●		●	●			
L7C170	22	●		●		●								
L7C171	24 (28)	●		●		●							(28)	
L7C172	24 (28)	●		●		●							(28)	
L6116	24 (28)	●	●	●	●	●	●	●		●			(28)	
64K														
L7C187	22 (24)	●		●		●		(24)		(24)		●		
L7C164	22 (24)	●		●		●		(24)		(24)		●		
L7C165	24 (28)	●		●		●		●		●				
L7C166	24 (28)	●		●		●		●		●				(28)
L7C161	28	●		●		●		●		●				●
L7C162	28	●		●		●		●		●				●
L7C185	28	●	●	●	●	●	●	●	●	●				●

64K — Product Selection

Part No.	Description	Speed (ns) Com.	Speed (ns) Mil.	Power (mW) Opr.	Power (mW) Standby	Pins	Packages Available
L7C187	64K x 1 Separate I/O	15	20	225	25	22/24	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C164	16K x 4 Common I/O 1 Chip Enable	20	25	285	25	22/24	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C165	16K x 4 Common I/O 2 Chip Enables + OE	20	25	285	25	24/28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C166	16K x 4 Common I/O 1 Chip Enable + OE	20	25	285	25	24/28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C161	16K x 4 Separate I/O Transparent Write	20	25	285	25	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C162	16K x 4 Separate I/O High Impedance Write	20	25	285	25	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C185	8K x 8 Common I/O	20	25	290	25	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)

64K — Product Cross Reference

	LOGIC DEVICES PART NUMBER						
Competitor	L7C187 (64K x 1)	L7C164 (16K x 4)	L7C165 (16K x 4)	L7C166 (16K x 4)	L7C161 (16K x 4)	L7C162 (16K x 4)	L7C185 (8K x 8)
Cypress	CY7C187	CY7C164	NA	CY7C166	CY7C161	CY7C162	CY7C185/186
IDT	IDT7187	IDT7188	IDT7198	IDT6198	IDT71981	IDT71982	IDT7164
Performance	P4C187	P4C188	P4C198A	P4C198	P4C1981	P4C1982	P4C164
Saratoga	SSM7187	SSM7188	SSM7198	SSM7166	SSM7161	SSM7162	SSM7164
Hitachi	HM6287/6787	HM6288/6788	NA	HM6789	NA	NA	HM6264
Fujitsu	MB81C71	MB81C74	MB81C75	NA	NA	NA	MB81C78/8464
Toshiba	TC5561/5562	TC55416	NA	TC55417	NA	NA	TMM2088
Micron	MT5C6401	MT5C6404	NA	MT5C6405	MT5C6406	MT5C6407	MT5C6408
Motorola	MCM6287	MCM6288/89	NA	MCM6290	NA	NA	MCM61/6264
Inmos	IMS1600/01	IMS1620	NA	IMS1624	NA	NA	IMS1630
Sony	CXK5164	CXK5464	NA	CXK5465	NA	NA	CXK5864/65
NEC	µPD4361	µPD4362	NA	µPD4363	NA	NA	µPD4364/4464

16K — Product Selection

Part No.	Description	Speed (ns) Com.	Speed (ns) Mil.	Power (mW) Opr.	Power (mW) Standby	Pins	Packages Available
L7C167	16K x 1 Separate I/O	12	15	190	20	20	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C168	4K x 4 Common I/O	15	20	170	20	20	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C170	4K x 4 Common I/O + OE	15	20	170	20	22	DIP
L7C171	4K x 4 Separate I/O Transparent Write	15	20	170	20	24/28	DIP, LCC
L7C172	4K x 4 Separate I/O High Impedance Write	15	20	170	20	24/28	DIP, LCC
L6116	2K x 8 Common I/O + OE	20	25	260	20	24/28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)

16K — Product Cross Reference

Competitor	LOGIC DEVICES PART NUMBER L7C167 (16K x 1)	L7C168 (4K x 4)	L7C170 (4K x 4)	L7C171 (4K x 4)	L7C172 (4K x 4)	L6116 (2K x 8)
Cypress	CY7C167	CY7C168	CY7C170	CY7C171	CY7C172	CY7C128/6116
IDT	IDT6167	IDT6168	NA	IDT71681	IDT71682	IDT6116
Performance	NA	P4C168	P4C170	P4C1681	P4C1682	P4C116
Saratoga	SSM6167	SSM6168	SSM6170	SSM6171	SSM6172	SSM6116
Hitachi	HM6167/6267	HM6168/6268	NA	NA	NA	HM6116/6716
Fujitsu	MB81C67	MB81C68/69	NA	NA	NA	MB8416
Toshiba	NA	TMM2068	TMM2078	NA	NA	TMM2015/2018
Micron	MT5C1601	MT5C1604	MT5C1605	MT5C1606	MT5C1607	MT5C1608
Motorola	MCM2167	MCM6168/1423	NA	NA	NA	MCM2016/18
Inmos	IMS1400/03	IMS1420/21/23	NA	NA	NA	IMS1433
Sony	NA	CXK5416	NA	NA	NA	CXK5814/16
NEC	µPD4311	µPD4314	NA	NA	NA	µPD446

Features

- 64K by 1 Static RAM with separate I/O, Chip Select power down
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 15 ns worst-case
- Low Power Operation
  Active: 225 mW typical at 45 ns
  Standby: 50 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 7187, Cypress CY7C187
- Package styles available:
  - 22-pin Plastic DIP
  - 22-pin Sidebraze, Hermetic DIP
  - 22-pin CerDIP
  - 22-pin Ceramic LCC
  - 24-pin Plastic SOIC (Gull-Wing)
  - 24-pin Plastic SOJ (J-Lead)

Description

The **L7C187** is a high-performance, low-power CMOS static Random Access Memory. The storage circuitry is organized as 65,536 words by 1 bit per word. Parts are available in six speed categories with worst-case access times from 15 ns to 85 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 225 mW (typical) at 45 ns. Dissipation drops to 25 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 3 µW at 2 V, allowing effective battery back-up operation.

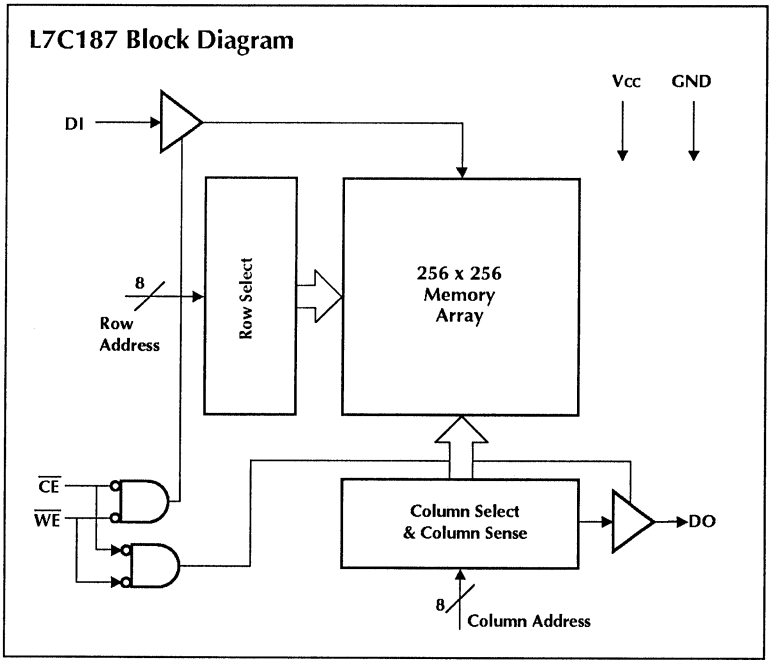
The L7C187 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C187 can withstand an injection current of up to 200 mA on any pin without damage.

L7C187 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	–3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			–350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		5.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		10	250	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		1.5	50	µA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C187-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	35	60	70	100	120	150	mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 22, 23, 24)*

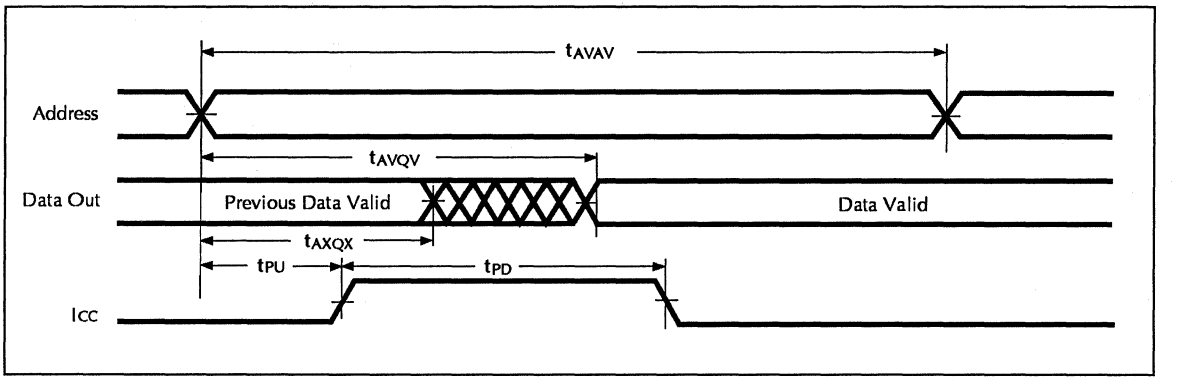
		L7C187-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		35		15		15		10		8		8
tPU	CE or WE Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

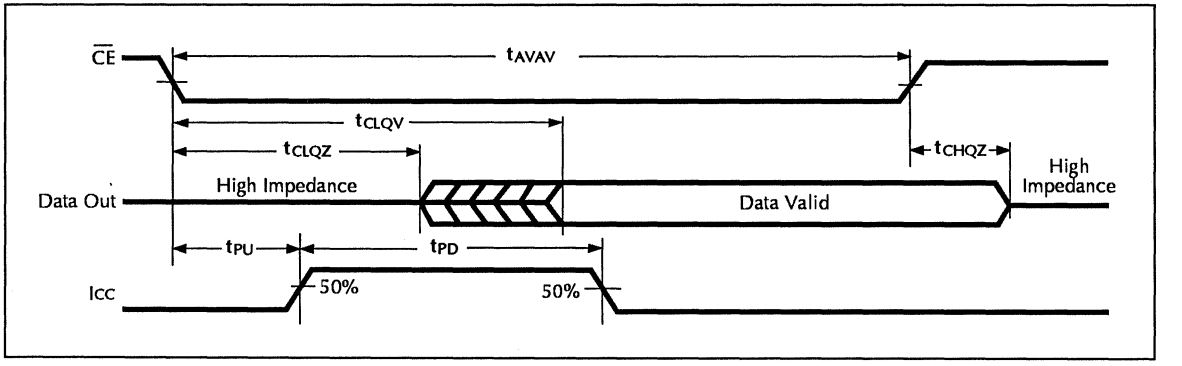
		L7C187-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		12		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

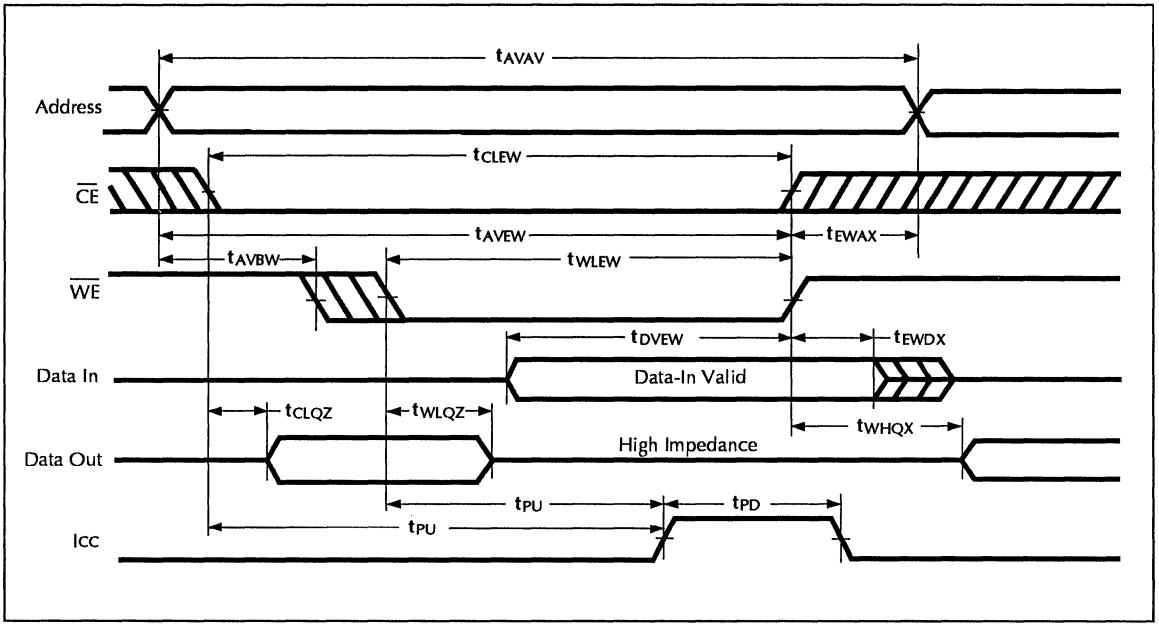
Read Cycle — Address Controlled *(Notes 13, 14)*



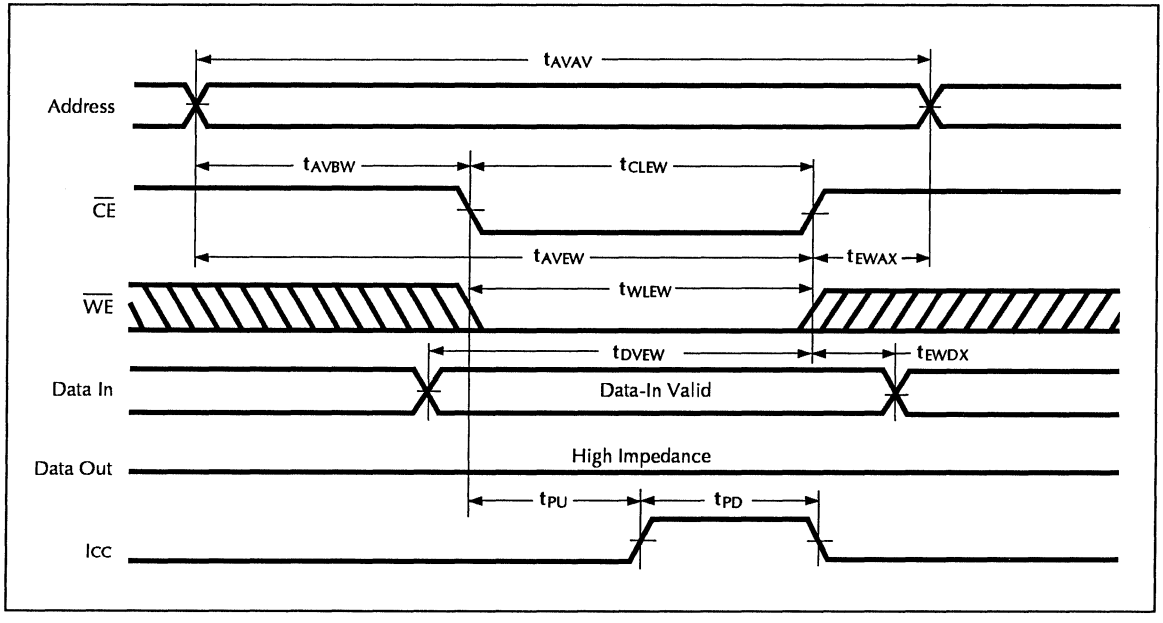
Read Cycle — $\overline{CE}$ Controlled *(Notes 13, 15)*



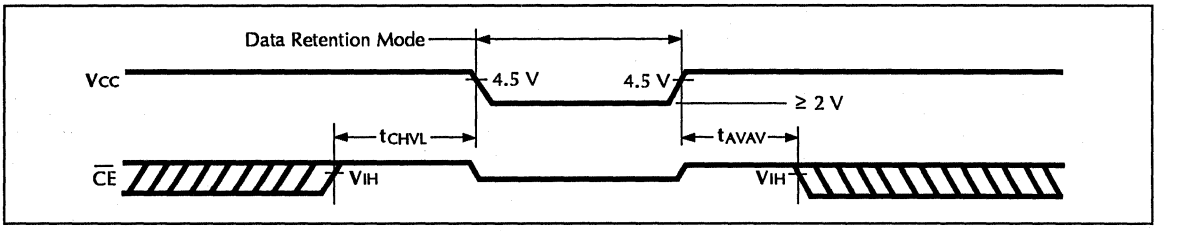
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

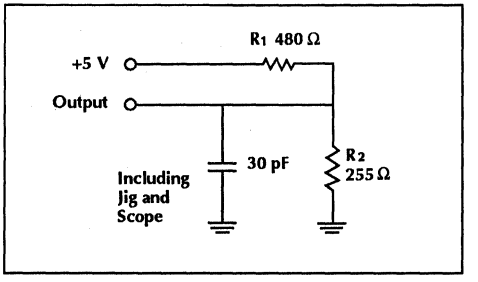


Figure 1b

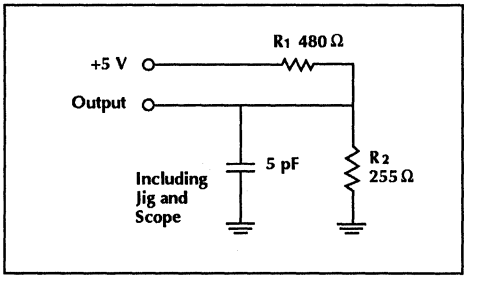
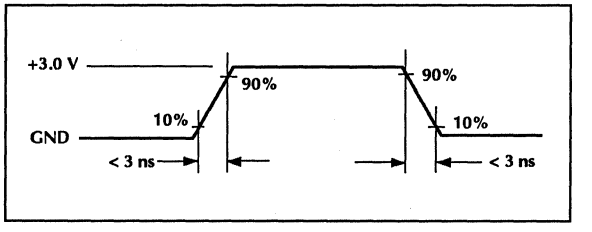


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
22-pin Plastic DIP (0.3") — P8	L7C187PC85	L7C187PC45	L7C187PC35	L7C187PC25	L7C187PC20	L7C187PC15
24-pin SOIC — U1	L7C187UC85	L7C187UC45	L7C187UC35	L7C187UC25	L7C187UC20	L7C187UC15
24-pin SOJ — W1	L7C187WC85	L7C187WC45	L7C187WC35	L7C187WC25	L7C187WC20	L7C187WC15
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C187DC85	L7C187DC45	L7C187DC35	L7C187DC25	L7C187DC20	L7C187DC15
22-pin CerDIP (0.3") — C3	L7C187CC85	L7C187CC45	L7C187CC35	L7C187CC25	L7C187CC20	L7C187CC15
22-pin Ceramic LCC — K4	L7C187KC85	L7C187KC45	L7C187KC35	L7C187KC25	L7C187KC20	L7C187KC15

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C187DM85 L7C187DME85 L7C187DMB85	L7C187DM45 L7C187DME45 L7C187DMB45	L7C187DM35 L7C187DME35 L7C187DMB35	L7C187DM25 L7C187DME25 L7C187DMB25	L7C187DM20 L7C187DME20 L7C187DMB20	
22-pin CerDIP (0.3") — C3	L7C187CM85 L7C187CME85 L7C187CMB85	L7C187CM45 L7C187CME45 L7C187CMB45	L7C187CM35 L7C187CME35 L7C187CMB35	L7C187CM25 L7C187CME25 L7C187CMB25	L7C187CM20 L7C187CME20 L7C187CMB20	
22-pin Ceramic LCC — K4	L7C187KM85 L7C187KME85 L7C187KMB85	L7C187KM45 L7C187KME45 L7C187KMB45	L7C187KM35 L7C187KME35 L7C187KMB35	L7C187KM25 L7C187KME25 L7C187KMB25	L7C187KM20 L7C187KME20 L7C187KMB20	

Pin Assignments *(P8, D8, C3, K4)*

Pin	Function	Pin	Function
1	A0	12	$\overline{CE}$
2	A1	13	DIN
3	A2	14	A8
4	A3	15	A9
5	A4	16	A10
6	A5	17	A11
7	A6	18	A12
8	A7	19	A13
9	DOUT	20	A14
10	$\overline{WE}$	21	A15
11	GND	22	VCC

Pin Assignments *(U1, W1)*

Pin	Function	Pin	Function
1	A0	13	$\overline{CE}$
2	A1	14	DIN
3	A2	15	A8
4	A3	16	A9
5	A4	17	A10
6	A5	18	A11
7	*NC*	19	*NC*
8	A6	20	A12
9	A7	21	A13
10	DOUT	22	A14
11	$\overline{WE}$	23	A15
12	GND	24	VCC

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Features

- 16K by 4 Static RAM with common I/O
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 20 ns worst-case
- Low Power Operation
  Active: 285 mW typical at 45 ns
  Standby: 50 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 7188/7198, Cypress CY7C164/166
- Package styles available:
  - 22/24-pin Plastic DIP
  - 22/24-pin Sidebraze, Hermetic DIP
  - 22/24-pin CerDIP
  - 22/28-pin Ceramic LCC
  - 24-pinPlastic SOIC (Gull-Wing)
  - 24-pin Plastic SOJ (J-Lead)

Description

The **L7C164**, **L7C165**, and **L7C166** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C164 has a single active-low Chip Enable. The L7C165 has two Chip Enables and a separate Output Enable. The L7C166 has a single Chip Enable and an Output Enable. Parts are available in five speed categories with worst-case access times from 20 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 285 mW (typical) at 45 ns. Dissipation drops to 25 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C164, L7C165, and L7C166 consumes only 3 µW (typical) at 2 V, for effective battery back-up operation.

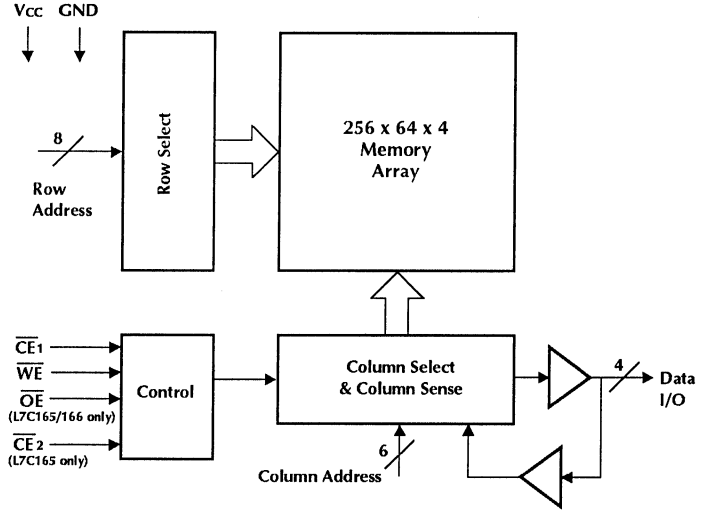
The L7C164, L7C165, and L7C166 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A13. For the L7C164, reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}_1$ low while $\overline{WE}$ remains high. For the L7C165 and L7C166, both $\overline{CE}_1$ and $\overline{CE}_2$ must be low. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C164, L7C165, and L7C166 can withstand an injection current of up to 200 mA on any pin without damage.

L7C164/165/166 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	–3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			–350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		5.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		10	250	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		1.5	50	µA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C164/165/166-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	45	70	85	120	145		mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 21, 22, 23, 24)*

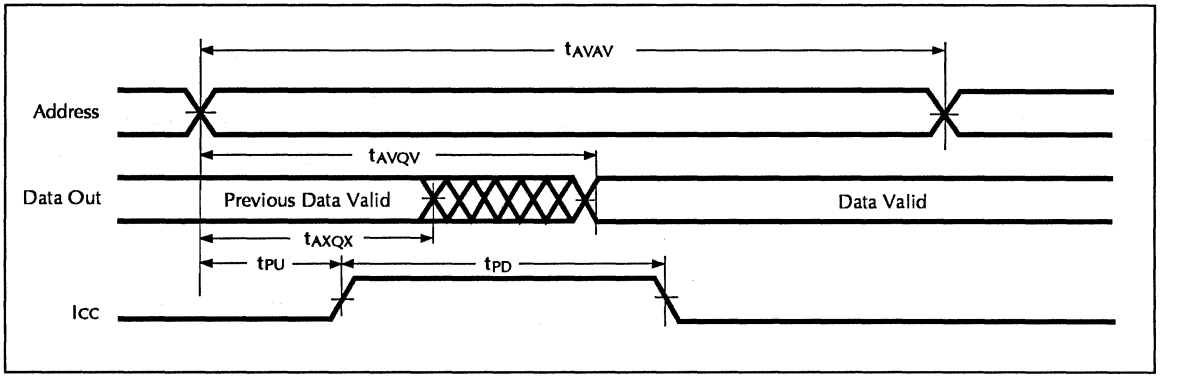
		L7C164/165/166-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	85		45		35		25		20		15	
t_{AVQV}	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
t_{AXQX}	Addr Change to Output Change	5		5		5		5		5		3	
t_{CLQV}	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
t_{CHQZ}	Chip Enable High to Output High Z (20, 21)		30		15		15		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		35		20		15		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
t_{OHQZ}	Output Enable High to Output High Z (20, 21)		30		15		12		10		8		8
t_{PU}	$\overline{CE}$ or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0		0	
t_{PD}	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

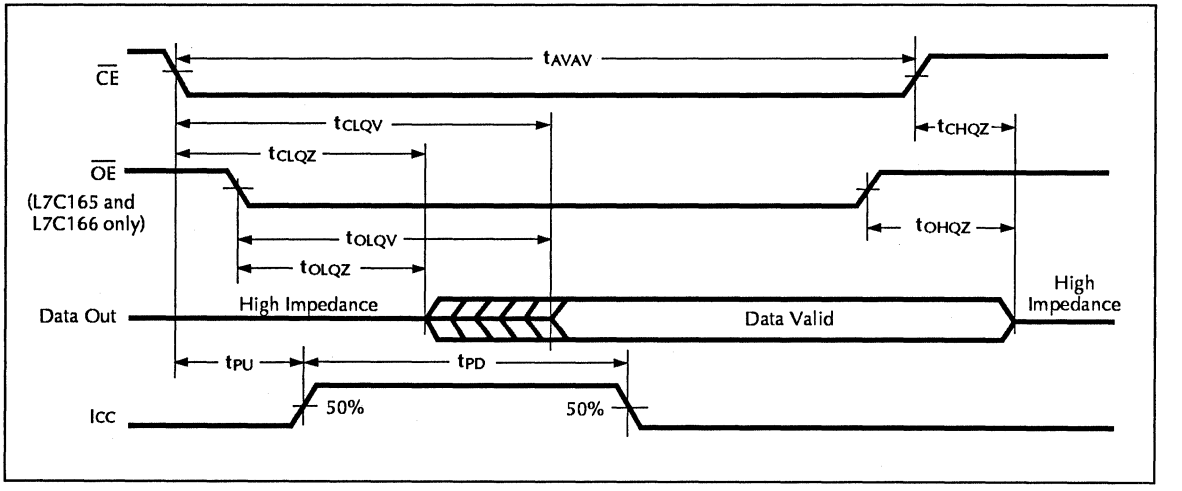
		L7C164/165/166-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	75		40		25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	65		30		25		20		17		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	65		30		25		20		17		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
t_{DVEW}	Data Valid to End of Write Cycle	35		15		15		15		13		10	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
t_{WLQZ}	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
t_{CHVL}	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

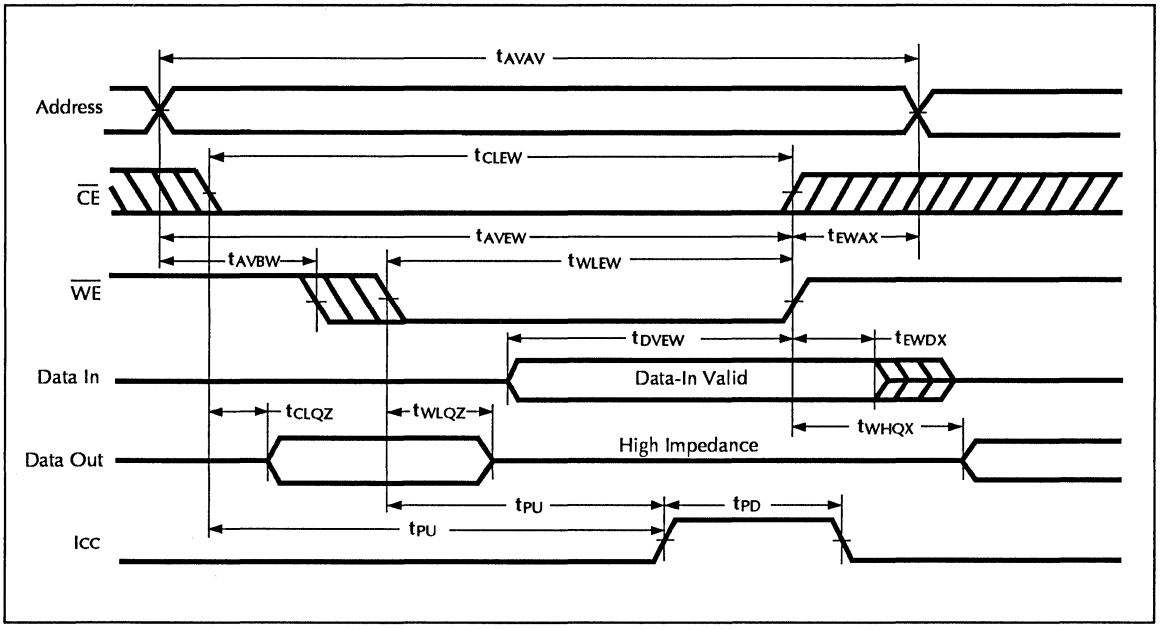
Read Cycle — Address Controlled *(Notes 13, 14)*



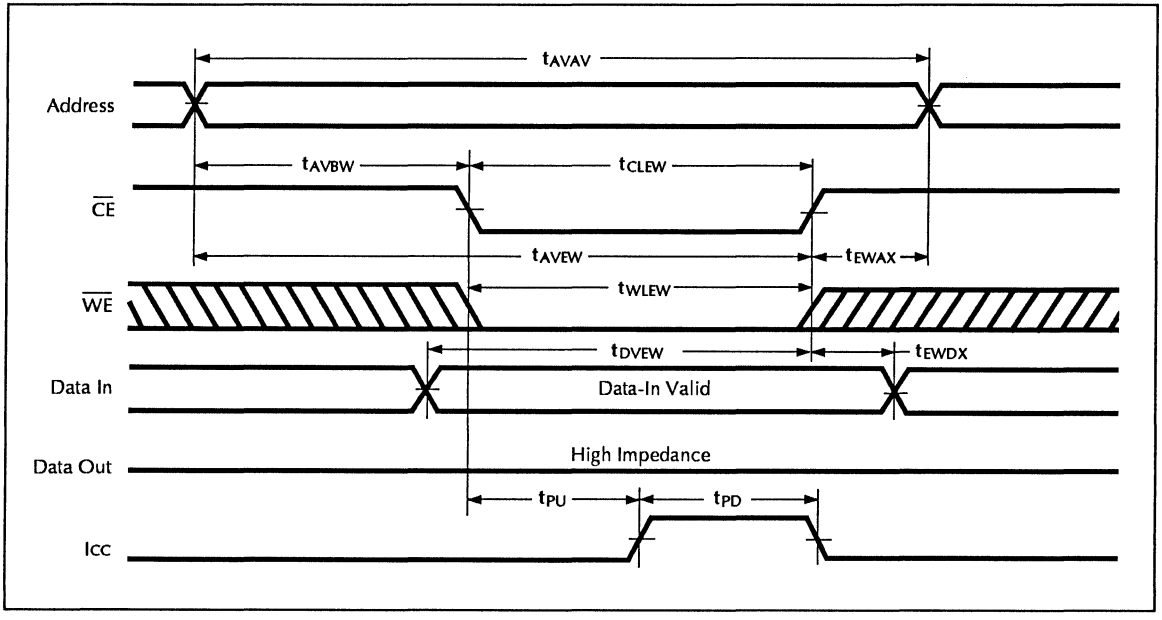
Read Cycle — $\overline{CE}$/$\overline{OE}$ Controlled *(Notes 13, 15)*



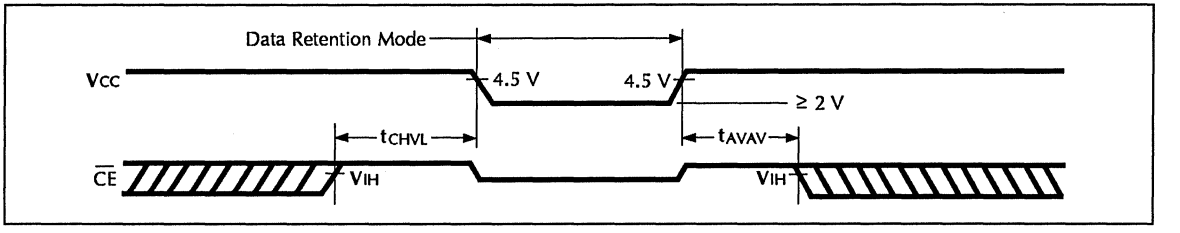
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

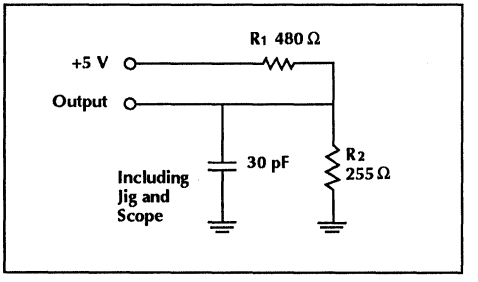


Figure 1b

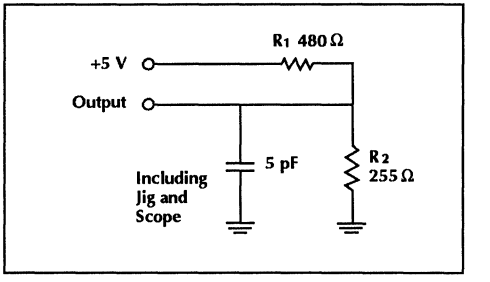
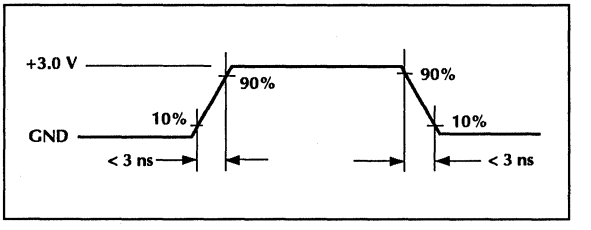


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
L7C164						
22-pin Plastic DIP (0.3") — P8	L7C164PC85	L7C164PC45	L7C164PC35	L7C164PC25	L7C164PC20	
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C164DC85	L7C164DC45	L7C164DC35	L7C164DC25	L7C164DC20	
24-pin SOIC — U1	L7C164UC85	L7C164UC45	L7C164UC35	L7C164UC25	L7C164UC20	
24-pin SOJ — W1	L7C164WC85	L7C164WC45	L7C164WC35	L7C164WC25	L7C164WC20	
22-pin CerDIP (0.3") — C3	L7C164CC85	L7C164CC45	L7C164CC35	L7C164CC25	L7C164CC20	
22-pin Ceramic LCC — K4	L7C164KC85	L7C164KC45	L7C164KC35	L7C164KC25	L7C164KC20	
L7C165						
24-pin Plastic DIP (0.3") — P2	L7C165PC85	L7C165PC45	L7C165PC35	L7C165PC25	L7C165PC20	
24-pin SOIC — U1	L7C165UC85	L7C165UC45	L7C165UC35	L7C165UC25	L7C165UC20	
24-pin SOJ — W1	L7C165WC85	L7C165WC45	L7C165WC35	L7C165WC25	L7C165WC20	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C165DC85	L7C165DC45	L7C165DC35	L7C165DC25	L7C165DC20	
24-pin CerDIP (0.3") — C1	L7C165CC85	L7C165CC45	L7C165CC35	L7C165CC25	L7C165CC20	
L7C166						
24-pin Plastic DIP (0.3") — P2	L7C166PC85	L7C166PC45	L7C166PC35	L7C166PC25	L7C166PC20	
24-pin SOIC — U1	L7C166UC85	L7C166UC45	L7C166UC35	L7C166UC25	L7C166UC20	
24-pin SOJ — W1	L7C166WC85	L7C166WC45	L7C166WC35	L7C166WC25	L7C166WC20	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C166DC85	L7C166DC45	L7C166DC35	L7C166DC25	L7C166DC20	
24-pin CerDIP (0.3") — C1	L7C166CC85	L7C166CC45	L7C166CC35	L7C166CC25	L7C166CC20	
28-pin Ceramic LCC — K5	L7C166KC85	L7C166KC45	L7C166KC35	L7C166KC25	L7C166KC20	

Ordering Information

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
L7C164						
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C164DM85 L7C164DME85 L7C164DMB85	L7C164DM45 L7C164DME45 L7C164DMB45	L7C164DM35 L7C164DME35 L7C164DMB35	L7C164DM25 L7C164DME25 L7C164DMB25		
22-pin CerDIP (0.3") — C3	L7C164CM85 L7C164CME85 L7C164CMB85	L7C164CM45 L7C164CME45 L7C164CMB45	L7C164CM35 L7C164CME35 L7C164CMB35	L7C164CM25 L7C164CME25 L7C164CMB25		
22-pin Ceramic LCC — K4	L7C164KM85 L7C164KME85 L7C164KMB85	L7C164KM45 L7C164KME45 L7C164KMB45	L7C164KM35 L7C164KME35 L7C164KMB35	L7C164KM25 L7C164KME25 L7C164KMB25		
L7C165						
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C165DM85 L7C165DME85 L7C165DMB85	L7C165DM45 L7C165DME45 L7C165DMB45	L7C165DM35 L7C165DME35 L7C165DMB35	L7C165DM25 L7C165DME25 L7C165DMB25		
24-pin CerDIP (0.3") — C1	L7C165CM85 L7C165CME85 L7C165CMB85	L7C165CM45 L7C165CME45 L7C165CMB45	L7C165CM35 L7C165CME35 L7C165CMB35	L7C165CM25 L7C165CME25 L7C165CMB25		
L7C166						
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C166DM85 L7C166DME85 L7C166DMB85	L7C166DM45 L7C166DME45 L7C166DMB45	L7C166DM35 L7C166DME35 L7C166DMB35	L7C166DM25 L7C166DME25 L7C166DMB25		
24-pin CerDIP (0.3") — C1	L7C166CM85 L7C166CME85 L7C166CMB85	L7C166CM45 L7C166CME45 L7C166CMB45	L7C166CM35 L7C166CME35 L7C166CMB35	L7C166CM25 L7C166CME25 L7C166CMB25		
28-pin Ceramic LCC — K5	L7C166KM85 L7C166KME85 L7C166KMB85	L7C166KM45 L7C166KME45 L7C166KMB45	L7C166KM35 L7C166KME35 L7C166KMB35	L7C166KM25 L7C166KME25 L7C166KMB25		

L7C164 Pin Assignments

(22-pin — P8, D8, C3)

Pin	Function	Pin	Function
1	A0	12	$\overline{WE}$
2	A1	13	I0/O0
3	A2	14	I1/O1
4	A3	15	I2/O2
5	A4	16	I3/O3
6	A5	17	A9
7	A6	18	A10
8	A7	19	A11
9	A8	20	A12
10	$\overline{CE}$	21	A13
11	GND	22	Vcc

L7C164 Pin Assignments

(22-pin — K4)

Pin	Function	Pin	Function
1	A5	12	$\overline{WE}$
2	A6	13	I0/O0
3	A7	14	I1/O1
4	A8	15	I2/O2
5	A9	16	I3/O3
6	A10	17	A0
7	A11	18	A1
8	A12	19	A2
9	A13	20	A3
10	$\overline{CE}$	21	A4
11	GND	22	Vcc

L7C164 Pin Assignments

(24-pin — U1, W1)

Pin	Function	Pin	Function
1	A0	13	$\overline{WE}$
2	A1	14	I0/O0
3	A2	15	I1/O1
4	A3	16	I2/O2
5	A4	17	I3/O3
6	A5	18	*NC*
7	A6	19	A9
8	A7	20	A10
9	A8	21	A11
10	$\overline{CE}$	22	A12
11	*NC*	23	A13
12	GND	24	Vcc

L7C165 Pin Assignments

(24-pin — P2, D2, C1, U1, W1)

Pin	Function	Pin	Function
1	A0	13	$\overline{WE}$
2	A1	14	I0/O0
3	A2	15	I1/O1
4	A3	16	I2/O2
5	A4	17	I3/O3
6	A5	18	$\overline{CE}2$
7	A6	19	A9
8	A7	20	A10
9	A8	21	A11
10	$\overline{CE}1$	22	A12
11	$\overline{OE}$	23	A13
12	GND	24	Vcc

L7C166 Pin Assignments

(24-pin — P2, D2, C1, U1, W1)

Pin	Function	Pin	Function
1	A0	13	$\overline{WE}$
2	A1	14	I0/O0
3	A2	15	I1/O1
4	A3	16	I2/O2
5	A4	17	I3/O3
6	A5	18	*NC*
7	A6	19	A9
8	A7	20	A10
9	A8	21	A11
10	$\overline{CE}1$	22	A12
11	$\overline{OE}$	23	A13
12	GND	24	Vcc

L7C166 Pin Assignments

(28-pin — K5)

Pin	Function	Pin	Function
1	*NC*	15	*NC*
2	*NC*	16	$\overline{WE}$
3	A0	17	I0/O0
4	A1	18	I1/O1
5	A2	19	I2/O2
6	A3	20	I3/O3
7	A4	21	A9
8	A5	22	A10
9	A6	23	A11
10	A7	24	A12
11	A8	25	A13
12	$\overline{CE}1$	26	*NC*
13	$\overline{OE}$	27	*NC*
14	GND	28	Vcc

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LOGIC DEVICES INCORPORATED

Features

- 16K by 4 Static RAM with separate I/O, transparent write (L7C161), or high impedance write (L7C162)
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 20 ns worst case
- Low Power Operation
  Active: 285 mW typical at 45 ns
  Standby: 50 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 71981/71982, Cypress CY7C161/162
- Package styles available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Ceramic LCC
  - 28-pinPlastic SOIC (Gull-Wing)
  - 28-pin Plastic SOJ (J-Lead)

Description

The **L7C161** and **L7C162** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out are separate. Parts are available in five speed categories with worst-case access times from 20 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 285 mW (typical) at 45 ns. Dissipation drops to 25 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C161 and L7C162 consumes only 3 µW (typical) at 2 V, allowing effective battery back-up operation.

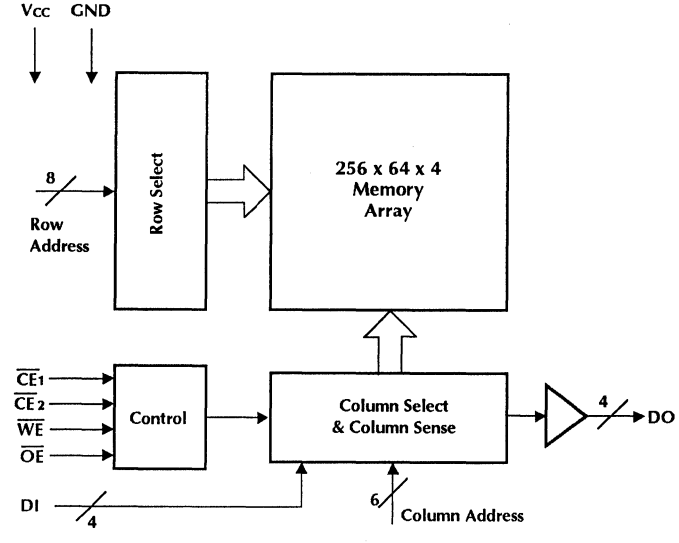
The L7C161 and L7C162 provides asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state bus output with a separate output enable line simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{13}. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}_1$ and $\overline{CE}_2$ low while Write remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is low (L7C162 only) or $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{OE}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{CE}_1$ and $\overline{CE}_2$ and $\overline{WE}$ inputs are all low. Any of these signals may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C161 and L7C162 can withstand an injection current of up to 200 mA on any pin without damage.

L7C161/162 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	−3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			−350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		5.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		10	250	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		1.5	50	µA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C161/162-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	45	70	85	120	145		mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 21, 22, 23, 24)*

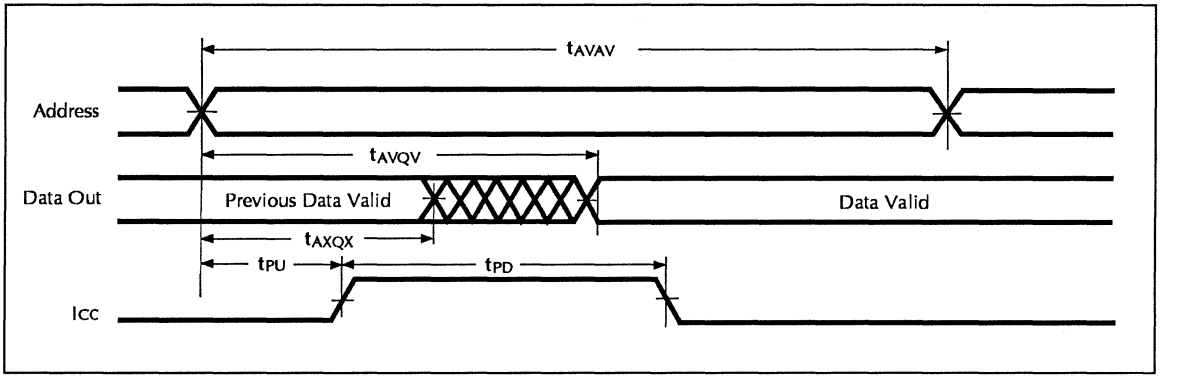
		L7C161/162-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		30		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		35		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
tOHQZ	Output Enable High to Output High Z (20, 21)		30		15		12		10		8		8
tPU	$\overline{CE}$ or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 21, 22, 23, 24)*

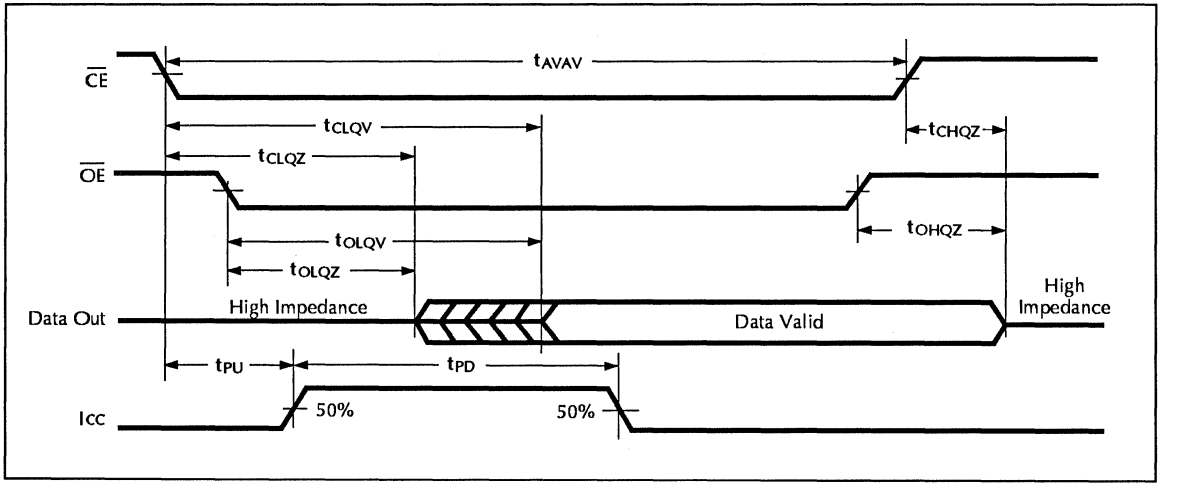
		L7C161/162-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		17		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	
tWLQV	Write Enable Low to Output Valid		50		35		30		20		15		15
tDVQV	Data Valid to Output Valid		50		35		30		20		15		15

Switching Waveforms

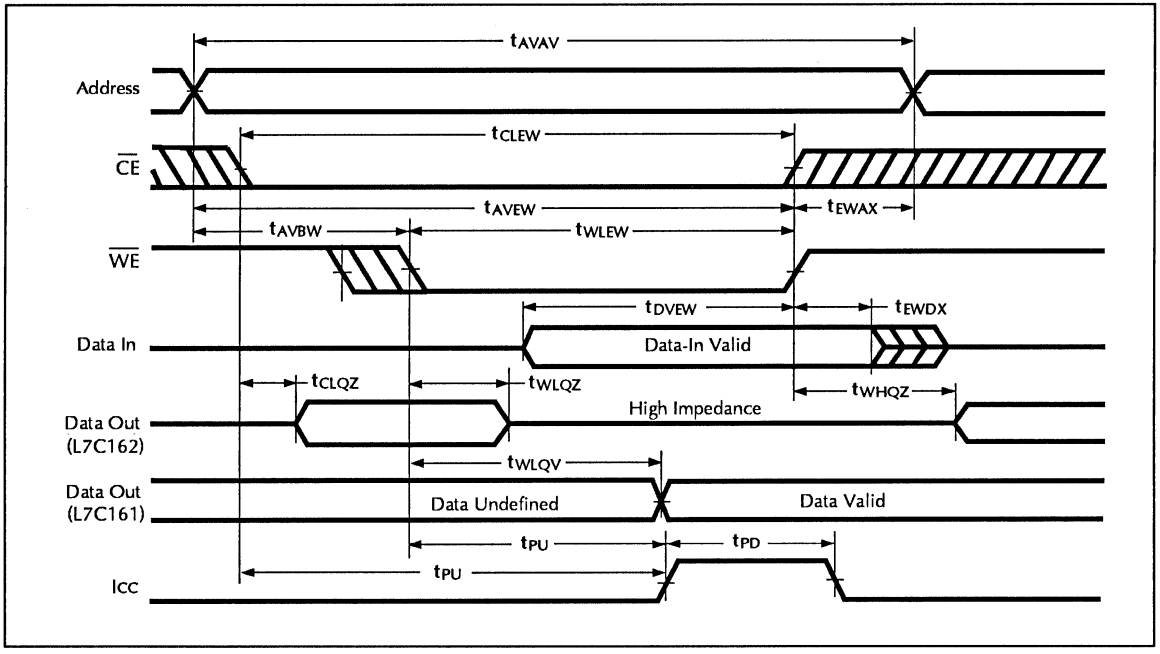
Read Cycle — Address Controlled *(Notes 13, 14)*



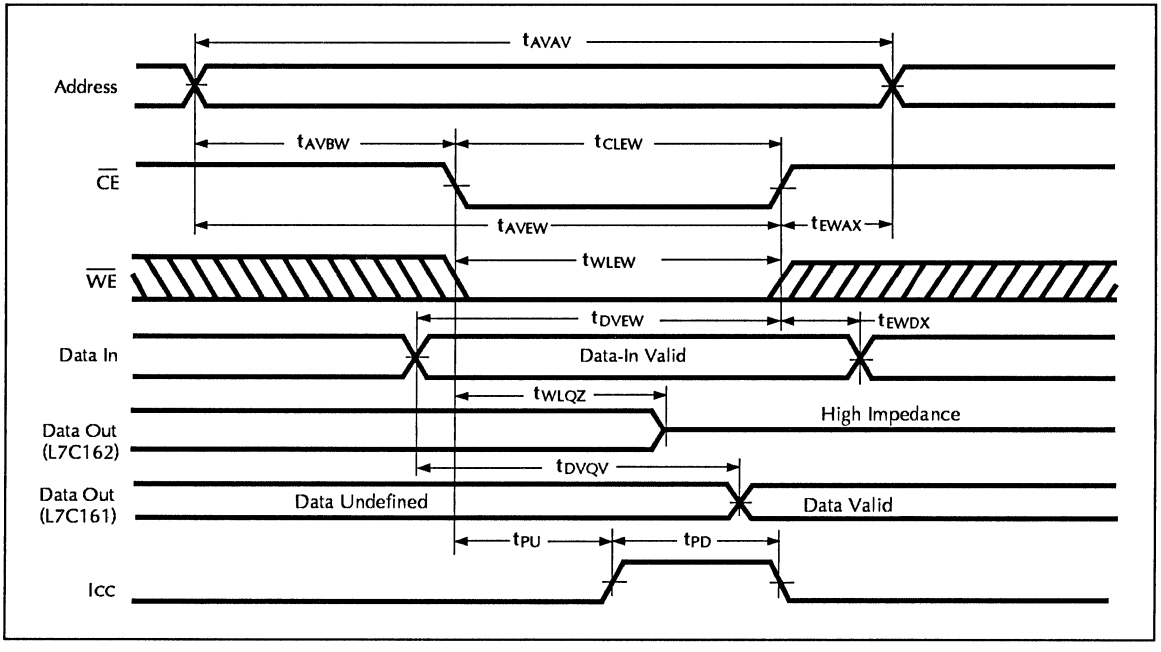
Read Cycle — $\overline{CE}/\overline{OE}$ Controlled *(Notes 13, 15)*



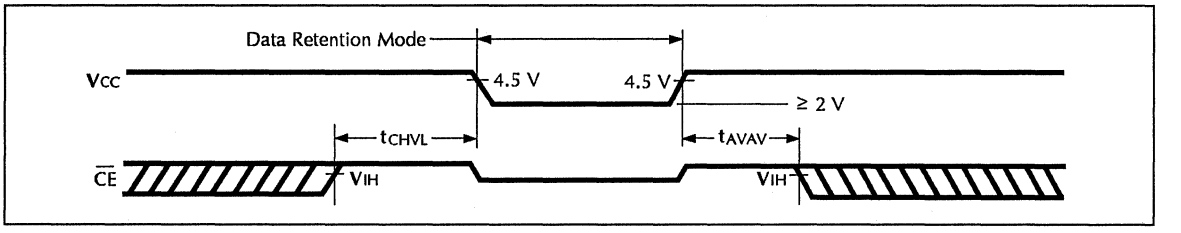
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

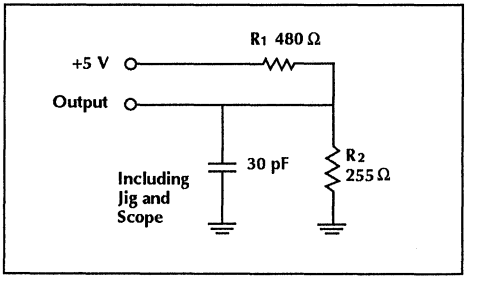


Figure 1b

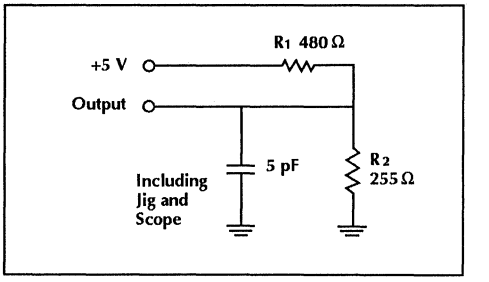
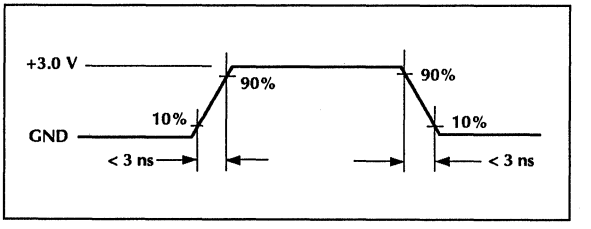


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
L7C161						
28-pin Plastic DIP (0.3") — P10	L7C161PC85	L7C161PC45	L7C161PC35	L7C161PC25	L7C161PC20	
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C161DC85	L7C161DC45	L7C161DC35	L7C161DC25	L7C161DC20	
28-pin SOIC — U2	L7C161UC85	L7C161UC45	L7C161UC35	L7C161UC25	L7C161UC20	
28-pin SOJ — W2	L7C161WC85	L7C161WC45	L7C161WC35	L7C161WC25	L7C161WC20	
28-pin CerDIP (0.3") — C5	L7C161CC85	L7C161CC45	L7C161CC35	L7C161CC25	L7C161CC20	
28-pin Ceramic LCC — K5	L7C161KC85	L7C161KC45	L7C161KC35	L7C161KC25	L7C161KC20	
L7C162						
28-pin Plastic DIP (0.3") — P10	L7C162PC85	L7C162PC45	L7C162PC35	L7C162PC25	L7C162PC20	
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C162DC85	L7C162DC45	L7C162DC35	L7C162DC25	L7C162DC20	
28-pin SOIC — U2	L7C162UC85	L7C162UC45	L7C162UC35	L7C162UC25	L7C162UC20	
28-pin SOJ — W2	L7C162WC85	L7C162WC45	L7C162WC35	L7C162WC25	L7C162WC20	
28-pin CerDIP (0.3") — C5	L7C162CC85	L7C162CC45	L7C162CC35	L7C162CC25	L7C162CC20	
28-pin Ceramic LCC — K5	L7C162KC85	L7C162KC45	L7C162KC35	L7C162KC25	L7C162KC20	

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
L7C161						
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C161DM85 L7C161DME85 L7C161DMB85	L7C161DM45 L7C161DME45 L7C161DMB45	L7C161DM35 L7C161DME35 L7C161DMB35	L7C161DM25 L7C161DME25 L7C161DMB25		
28-pin CerDIP (0.3") — C5	L7C161CM85 L7C161CME85 L7C161CMB85	L7C161CM45 L7C161CME45 L7C161CMB45	L7C161CM35 L7C161CME35 L7C161CMB35	L7C161CM25 L7C161CME25 L7C161CMB25		
28-pin Ceramic LCC — K5	L7C161KM85 L7C161KME85 L7C161KMB85	L7C161KM45 L7C161KME45 L7C161KMB45	L7C161KM35 L7C161KME35 L7C161KMB35	L7C161KM25 L7C161KME25 L7C161KMB25		
L7C162						
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C162DM85 L7C162DME85 L7C162DMB85	L7C162DM45 L7C162DME45 L7C162DMB45	L7C162DM35 L7C162DME35 L7C162DMB35	L7C162DM25 L7C162DME25 L7C162DMB25		
28-pin CerDIP (0.3") — C5	L7C162CM85 L7C162CME85 L7C161CME85	L7C162CM45 L7C162CME45 L7C162CMB45	L7C162CM35 L7C162CME35 L7C162CMB35	L7C162CM25 L7C162CME25 L7C162CMB25		
28-pin Ceramic LCC — K5	L7C162KM85 L7C162KME85 L7C162KMB85	L7C162KM45 L7C162KME45 L7C162KMB45	L7C162KM35 L7C162KME35 L7C162KMB35	L7C162KM25 L7C162KME25 L7C162KMB25		

Pin Assignments *(P10, D10, C5, K5, U2, W2)*

Pin	Function	Pin	Function
1	A_0	15	$\overline{CE}_2$
2	A_1	16	$\overline{WE}$
3	A_2	17	O_0
4	A_3	18	O_1
5	A_4	19	O_2
6	A_5	20	O_3
7	A_6	21	I_2
8	A_7	22	I_3
9	A_8	23	A_9
10	I_0	24	A_{10}
11	I_1	25	A_{11}
12	$\overline{CE}_1$	26	A_{12}
13	$\overline{OE}$	27	A_{13}
14	GND	28	V_{CC}

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Features

- 8K by 8 Static RAM with chip select powerdown, output enable
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 20 ns worst case
- Low Power Operation
  Active: 290 mW typical at 45 ns
  Standby: 50 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT7164, Cypress CY7C185/186
- Package styles available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Ceramic LCC
  - 28-pin Plastic SOIC (Gull-Wing)
  - 28-pinPlastic SOJ (J-Lead)

Description

The **L7C185** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 8,192 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. Parts are available in five speeds with worst-case access times from 20 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 290 mW (typical) at 45 ns. Dissipation drops to 25 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C185 consumes only 3 µW at 2 V (typical), for effective battery back-up operation.

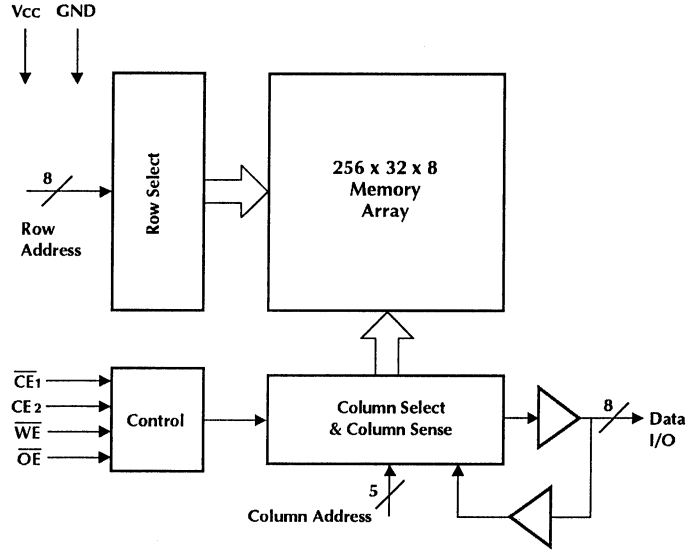
The L7C185 provides asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state I/O bus with a separate output enable simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A12. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE_1}$ low and CE_2 high while Write remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE_1}$ is high or CE_2 or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE_1}$ and $\overline{WE}$ inputs are both low, and CE_2 is high. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C185 can withstand an injection current of up to 200 mA on any pin without damage.

L7C185 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	−3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			−350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		5.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		10	250	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		1.5	50	µA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C185-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	45	80	100	140	180		mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 21, 22, 23, 24)*

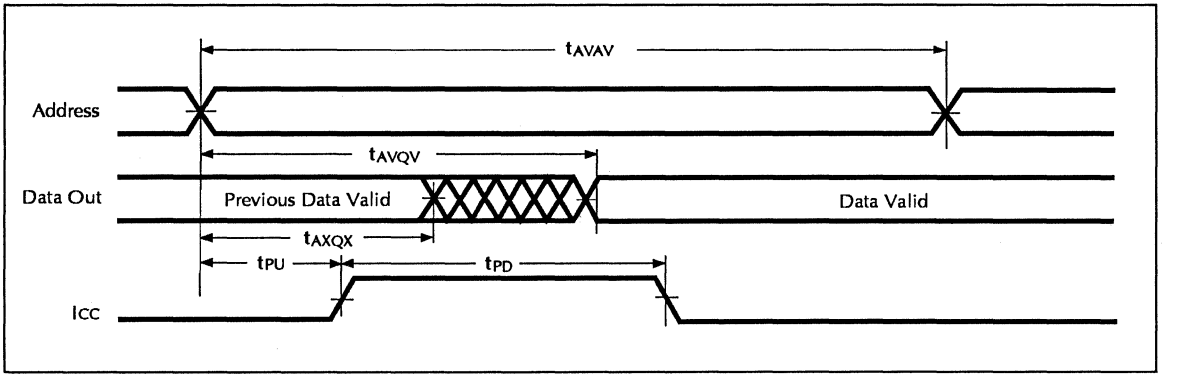
		L7C185-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Active to Output Valid (13, 15)		85		30		25		25		20		15
tCLQZ	Chip Enable Active to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable Inactive to Output High Z (20, 21)		35		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		35		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
tOHQZ	Output Enable High to Output High Z (20, 21)		30		15		12		10		8		8
tPU	CE Active or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

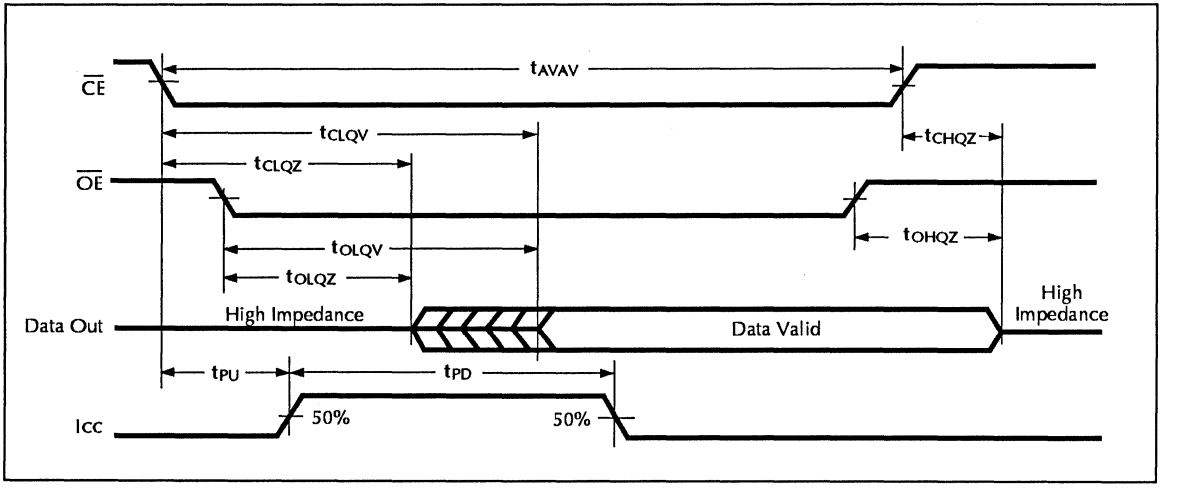
		L7C185-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Active to End of Write Cycle	65		30		25		20		17		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		30		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable Inactive to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

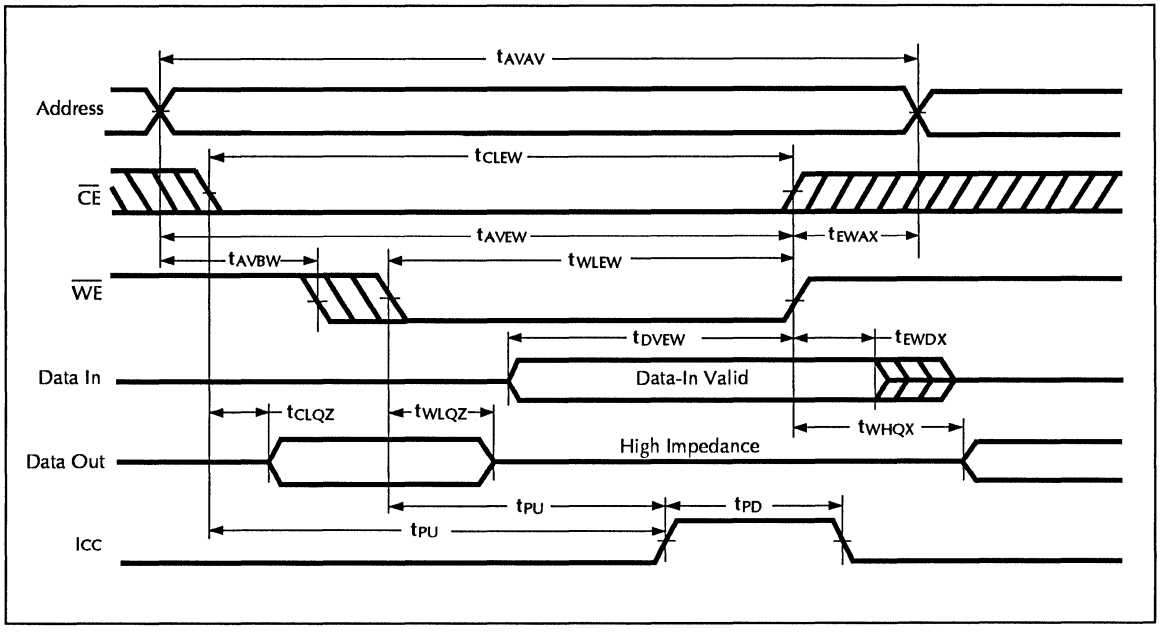
Read Cycle — Address Controlled (Notes 13, 14)



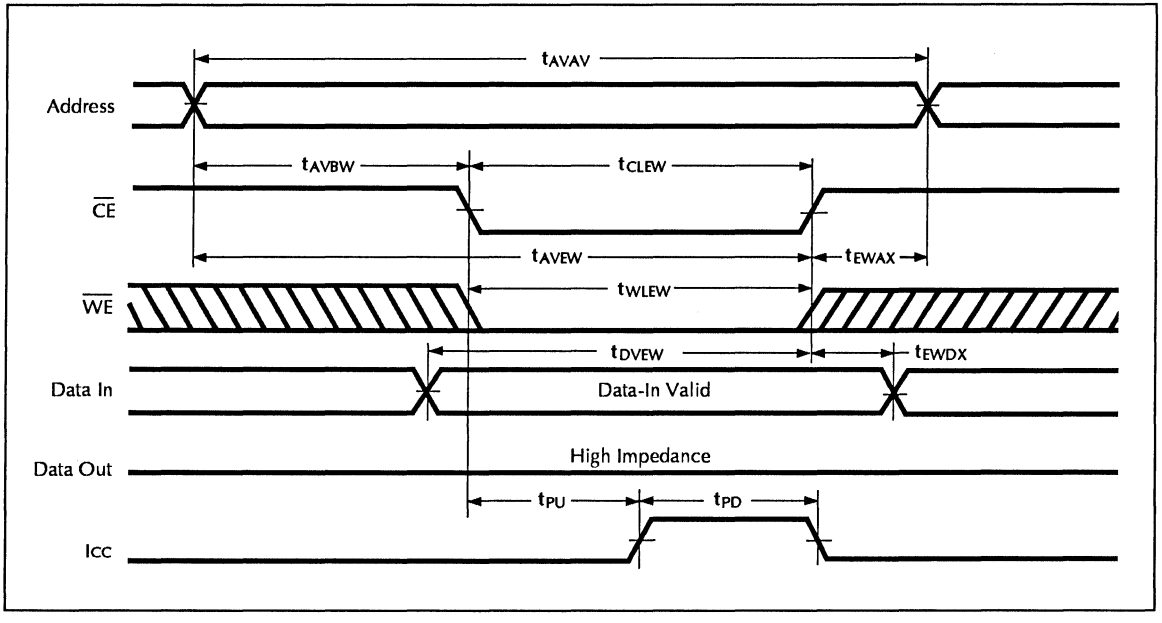
Read Cycle — $\overline{CE}$/$\overline{OE}$ Controlled (Notes 13, 15)



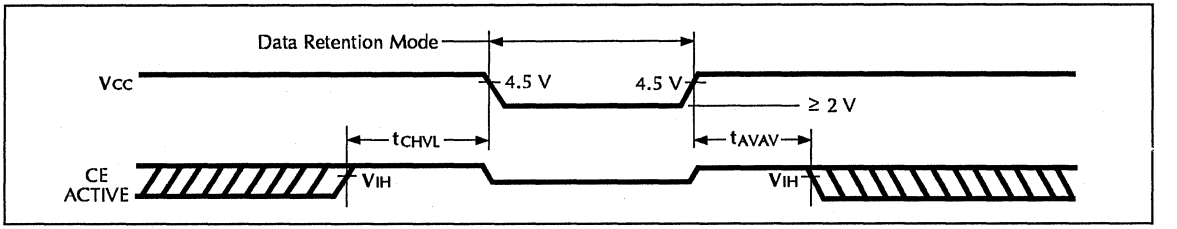
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

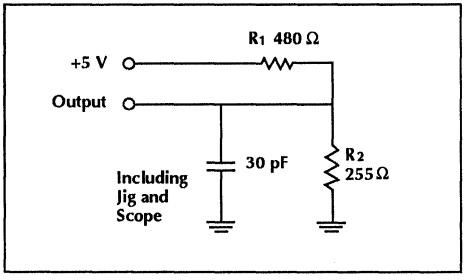


Figure 1b

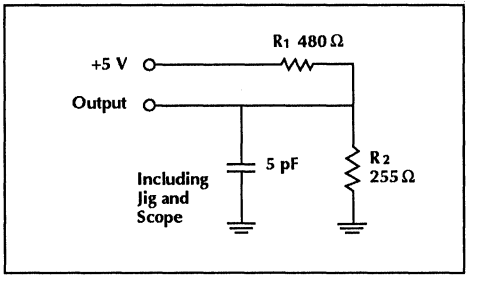
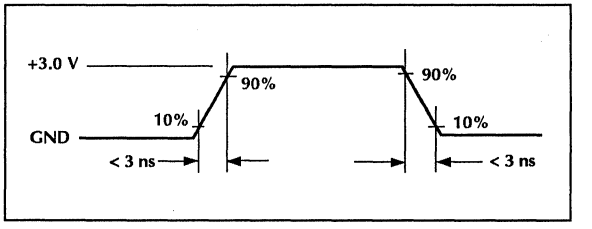


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
28-pin Plastic DIP (0.3") — P10	L7C185PC85	L7C185PC45	L7C185PC35	L7C185PC25	L7C185PC20	
28-pin Plastic DIP (0.6") — P9	L7C185NC85	L7C185NC45	L7C185NC35	L7C185NC25	L7C185NC20	
28-pin SOIC — U2 (0.300")	L7C185UC85	L7C185UC45	L7C185UC35	L7C185UC25	L7C185UC20	
28-pin SOIC — V2 (0.331")	L7C185VC85	L7C185VC45	L7C185VC35	L7C185VC25	L7C185VC20	
28-pin SOJ — W2	L7C185WC85	L7C185WC45	L7C185WC35	L7C185WC25	L7C185WC20	
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C185DC85	L7C185DC45	L7C185DC35	L7C185DC25	L7C185DC20	
28-pin Sidebraze (0.6") Hermetic DIP — D9	L7C185HC85	L7C185HC45	L7C185HC35	L7C185HC25	L7C185HC20	
28-pin CerDIP (0.3") — C5	L7C185CC85	L7C185CC45	L7C185CC35	L7C185CC25	L7C185CC20	
28-pin CerDIP (0.6") — C6	L7C185IC85	L7C185IC45	L7C185IC35	L7C185IC25	L7C185IC20	
28-pin Ceramic LCC — K5	L7C185KC85	L7C185KC45	L7C185KC35	L7C185KC25	L7C185KC20	

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
28-pin Sidebraze (0.3") Hermetic DIP — D10	L7C185DM85 L7C185DME85 L7C185DMB85	L7C185DM45 L7C185DME45 L7C185DMB45	L7C185DM35 L7C185DME35 L7C185DMB35	L7C185DM25 L7C185DME25 L7C185DMB25		
28-pin Sidebraze (0.6") Hermetic DIP — D9	L7C185HM85 L7C185HME85 L7C185HMB85	L7C185HM45 L7C185HME45 L7C185HMB45	L7C185HM35 L7C185HME35 L7C185HMB35	L7C185HM25 L7C185HME25 L7C185HMB25		
28-pin CerDIP (0.3") — C5	L7C185CM85 L7C185CME85 L7C185CMB85	L7C185CM45 L7C185CME45 L7C185CMB45	L7C185CM35 L7C185CME35 L7C185CMB35	L7C185CM25 L7C185CME25 L7C185CMB25		
28-pin CerDIP (0.6") — C6	L7C185IM85 L7C185IME85 L7C185IME85	L7C185IM45 L7C185IME45 L7C185IMB45	L7C185IM35 L7C185IME35 L7C185IMB35	L7C185IM25 L7C185IME25 L7C185IMB25		
28-pin Ceramic LCC — K5	L7C185KM85 L7C185KME85 L7C185KMB85	L7C185KM45 L7C185KME45 L7C185KMB45	L7C185KM35 L7C185KME35 L7C185KMB35	L7C185KM25 L7C185KME25 L7C185KMB25		

Pin Assignments *(P9, P10, D9, D10, C5, C6, U2, W2)*

Pin	Function	Pin	Function
1	*NC*	15	I3/O3
2	A12	16	I4/O4
3	A7	17	I5/O5
4	A6	18	I6/O6
5	A5	19	I7/O7
6	A4	20	$\overline{CE}$1
7	A3	21	A10
8	A2	22	$\overline{OE}$
9	A1	23	A11
10	A0	24	A9
11	I0/O0	25	A8
12	I1/O1	26	CE2
13	I2/O2	27	$\overline{WE}$
14	GND	28	VCC

Pin Assignments *(K5)*

Pin	Function	Pin	Function
1	A12	15	I3/O3
2	A7	16	I4/O4
3	A6	17	I5/O5
4	*NC*	18	I6/O6
5	A5	19	I7/O7
6	A4	20	$\overline{CE}$1
7	A3	21	A10
8	A2	22	$\overline{OE}$
9	A1	23	A11
10	A0	24	A9
11	I0/O0	25	A8
12	I1/O1	26	CE2
13	I2/O2	27	$\overline{WE}$
14	GND	28	VCC

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Features

- 16K by 1 Static RAM with separate I/O, Chip Select power down
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 12 ns worst-case
- Low Power Operation
  Active: 190 mW typical at 35 ns
  Standby: 12.5 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 6167, Cypress CY7C167
- Package styles available:
  - 20-pin Plastic DIP
  - 20-pin Sidebraze, Hermetic DIP
  - 20-pin CerDIP
  - 20-pinCeramic LCC
  - 20-pin Plastic SOIC (Gull-Wing)
  - 20-pin Plastic SOJ (J-Lead)

Description

The **L7C167** is a high-performance, low-power CMOS static Random Access Memory. The storage circuitry is organized as 16,384 words by 1 bit per word. Parts are available in six speed categories with worst-case access times from 12 ns to 85 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 190 mW (typical) when being operated at 35 ns. Dissipation drops to 20 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 1 µW at 2 V, allowing effective battery back-up operation.

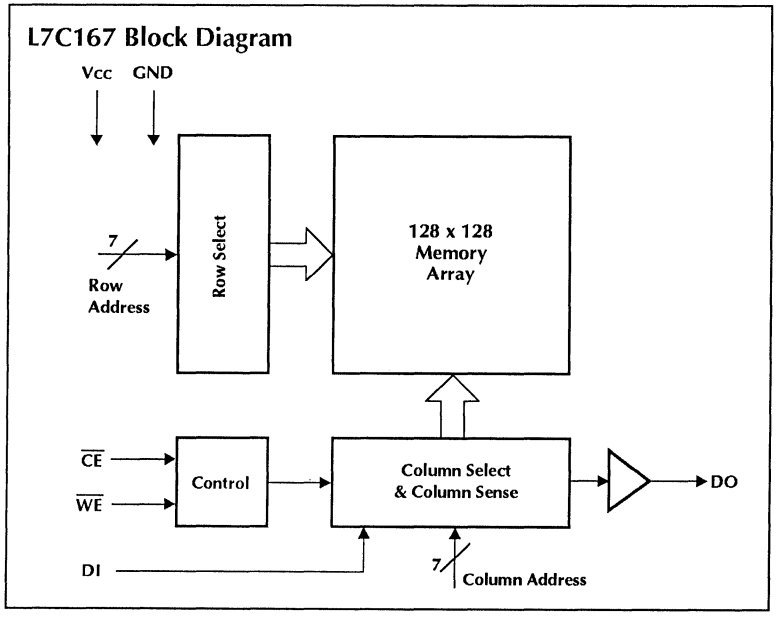
The L7C167 provides asynchronous (unclocked) operation with matching access and cycle times. Active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{13}. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C167 can withstand an injection current of up to 200 mA on any pin without damage.

L7C167 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	−3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			−350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		4.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		0.5	10	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		5	500	nA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C167-						
Symbol	Parameter	Test Condition	85	35	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	25	50	65	80	100	125	mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 22, 23, 24)*

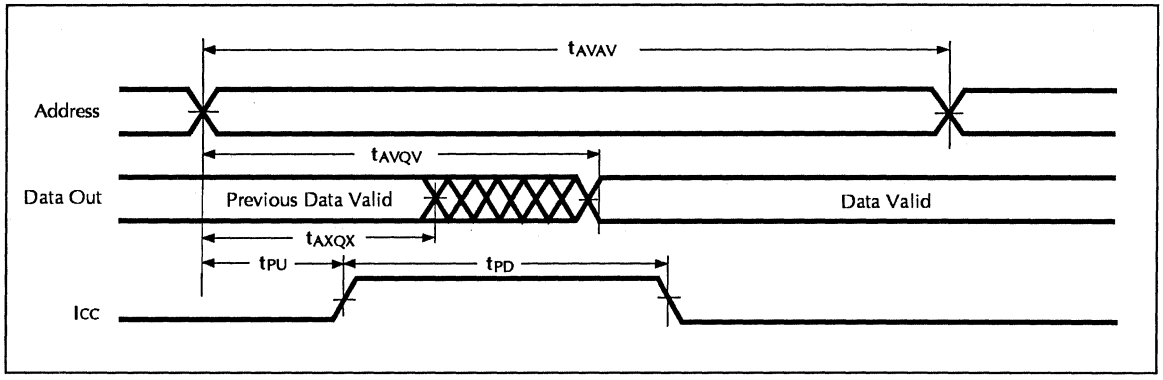
		L7C167-											
		85		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		35		25		20		15		12	
tAVQV	Addr Valid to Output Valid (13, 14)		85		35		25		20		15		12
tAXQX	Addr Change to Output Change	5		5		5		5		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		35		25		20		15		12
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		30		15		10		8		8		8
tPU	CE or WE Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		35		25		20		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

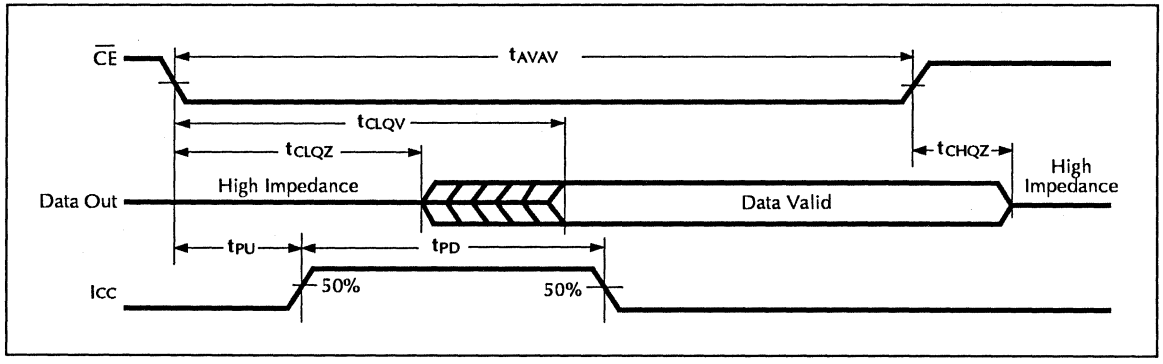
		L7C167-											
		85		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		25		20		20		15		12	
tCLEW	Chip Enable Low to End of Write Cycle	65		25		20		17		12		10	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		25		20		17		12		10	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		17		12		10	
tDVEW	Data Valid to End of Write Cycle	35		15		15		13		10		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		10		7		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

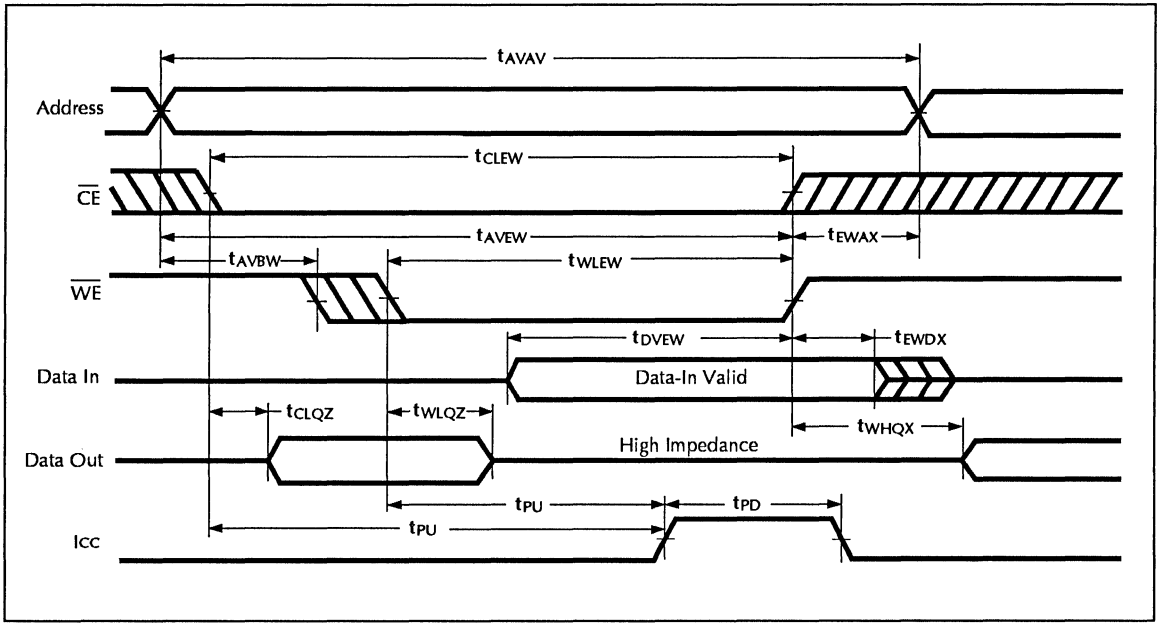
Read Cycle — Address Controlled *(Notes 13, 14)*



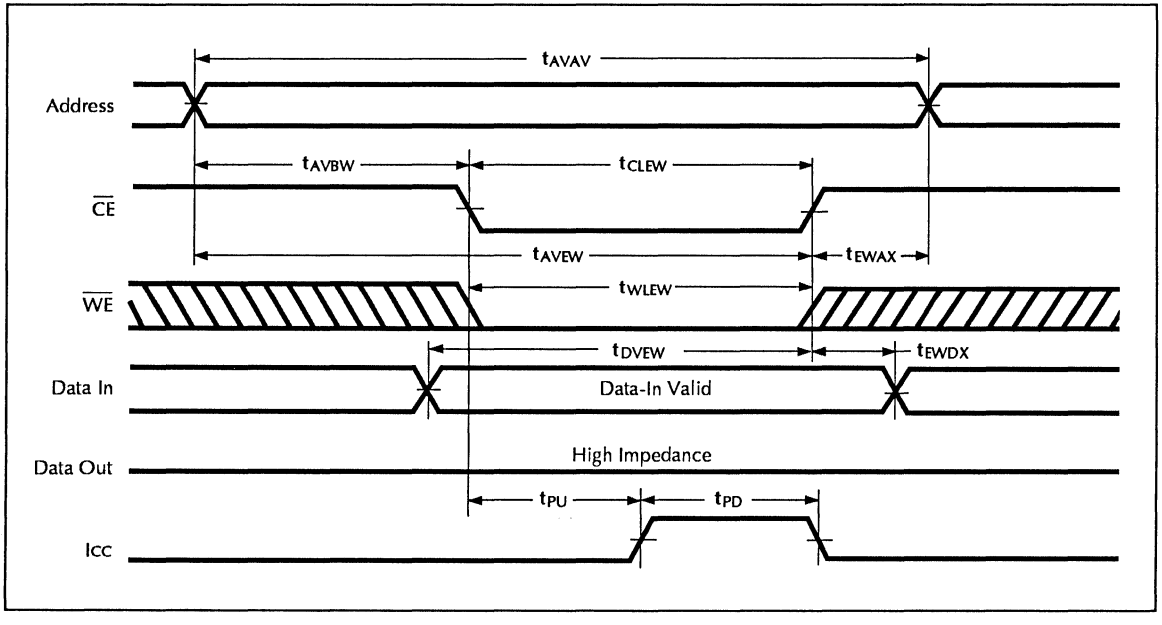
Read Cycle — $\overline{CE}$ Controlled *(Notes 13, 15)*



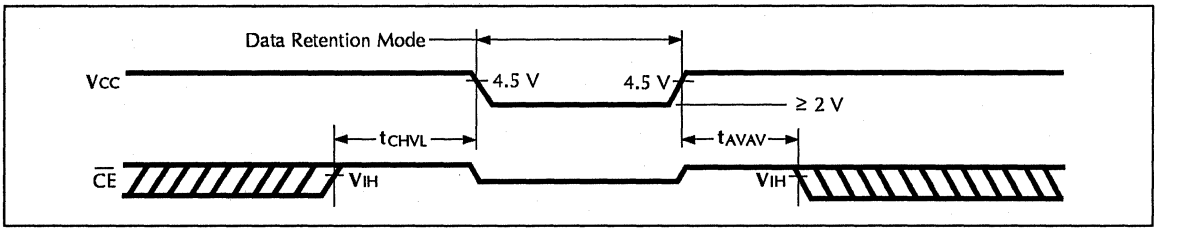
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

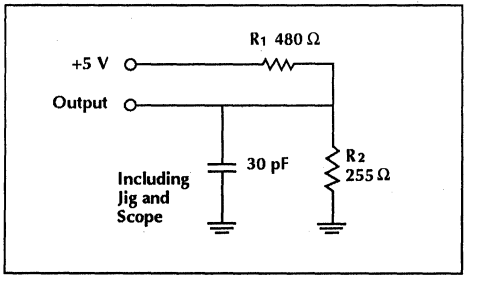


Figure 1b

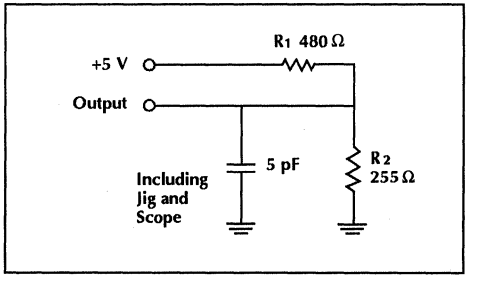
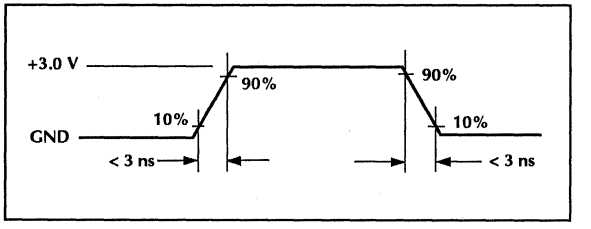


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	35 ns	25 ns	20 ns	15 ns	12 ns
20-pin Plastic DIP (0.3") — P6	L7C167PC85	L7C167PC35	L7C167PC25	L7C167PC20	L7C167PC15	L7C167PC12
20-pin Sidebraze (0.3") Hermetic DIP — D7	L7C167DC85	L7C167DC35	L7C167DC25	L7C167DC20	L7C167DC15	L7C167DC12
20-pin Plastic SOIC — U3	L7C167UC85	L7C167UC35	L7C167UC25	L7C167UC20	L7C167UC15	L7C167UC12
20-pin Plastic SOJ — W3	L7C167WC85	L7C167WC35	L7C167WC25	L7C167WC20	L7C167WC15	L7C167WC12
20-pin CerDIP (0.3") — C2	L7C167CC85	L7C167CC35	L7C167CC25	L7C167CC20	L7C167CC15	L7C167CC12
20-pin Ceramic LCC — K6	L7C167KC85	L7C167KC35	L7C167KC25	L7C167KC20	L7C167KC15	L7C167KC12

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	35 ns	25 ns	20 ns	15 ns	
20-pin Sidebraze (0.3") Hermetic DIP — D7	L7C167DM85 L7C167DME85 L7C167DMB85	L7C167DM35 L7C167DME35 L7C167DMB35	L7C167DM25 L7C167DME25 L7C167DMB25	L7C167DM20 L7C167DME20 L7C167DMB20	L7C167DM15 L7C167DME15 L7C167DMB15	
20-pin CerDIP (0.3") — C2	L7C167CM85 L7C167CME85 L7C167CMB85	L7C167CM35 L7C167CME35 L7C167CMB35	L7C167CM25 L7C167CME25 L7C167CMB25	L7C167CM20 L7C167CME20 L7C167CMB20	L7C167CM15 L7C167CME15 L7C167CMB15	
20-pin Ceramic LCC — K6	L7C167KM85 L7C167KME85 L7C167KMB85	L7C167KM35 L7C167KME35 L7C167KMB35	L7C167KM25 L7C167KME25 L7C167KMB25	L7C167KM20 L7C167KME20 L7C167KMB20	L7C167KM15 L7C167KME15 L7C167KMB15	

Pin Assignments *(P6, D7, C2, K6, U3, W3)*

Pin	Function	Pin	Function
1	A_0	11	$\overline{CE}$
2	A_1	12	D_{IN}
3	A_2	13	A_7
4	A_3	14	A_8
5	A_4	15	A_9
6	A_5	16	A_{10}
7	A_6	17	A_{11}
8	D_{OUT}	18	A_{12}
9	$\overline{WE}$	19	A_{13}
10	GND	20	V_{CC}

628 East Evelyn Avenue • Sunnyvale, CA 94086 • Telephone 408-720-8630 • FAX 408-733-7690

Features

- 4K by 4 Static RAM with common I/O, output enable (L7C170 only)
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 15 ns worst case
- Low Power Operation
  Active: 170 mW typical at 45 ns
  Standby: 12.5 µW typical
- Data retention at 2 V for battery backup
- Plug-compatible with IDT 6168 and Cypress CY7C168/170
- Package styles available:
  - 20/22-pin Plastic DIP
  - 20/22-pin Sidebraze, Hermetic DIP
  - 20/22-pin CerDIP
  - 20-pin Ceramic LCC
  - 20-pin Plastic SOIC (Gull-Wing)
  - 20-pin Plastic SOJ (J-Lead)

Description

The **L7C168** and **L7C170** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C170 version adds and active-low Output Enable input. Parts are available in six speed categories with worst-case access times from 15 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 170 mW (typical) when being operated at 45 ns. Dissipation drops to 20 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C168 and L7C170 consumes only 1 µW (typical) at 2 V, for effective battery back-up operation.

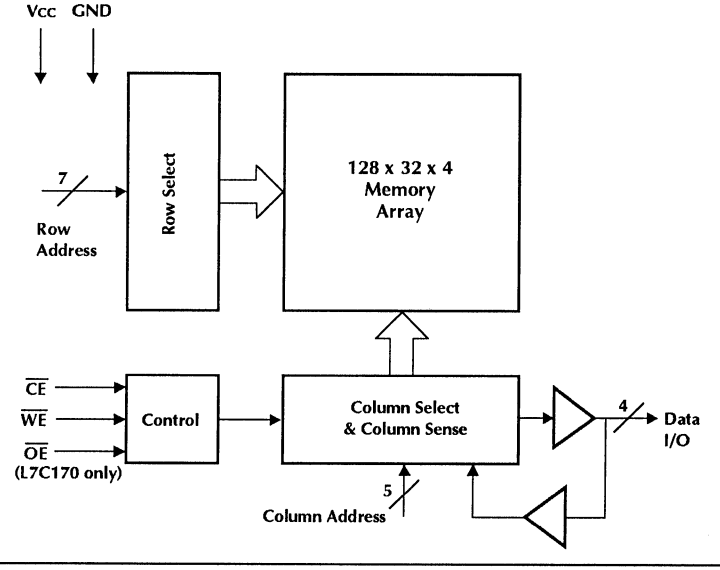
The L7C168 and L7C170 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{11}. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C168 and L7C170 can withstand an injection current of up to 200 mA on any pin without damage.

L7C168/170 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latch-up current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	−3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			−350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		4.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		0.5	10	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		5	500	nA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C168/170-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	25	45	55	75	95	120	mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 21, 22, 23, 24)*

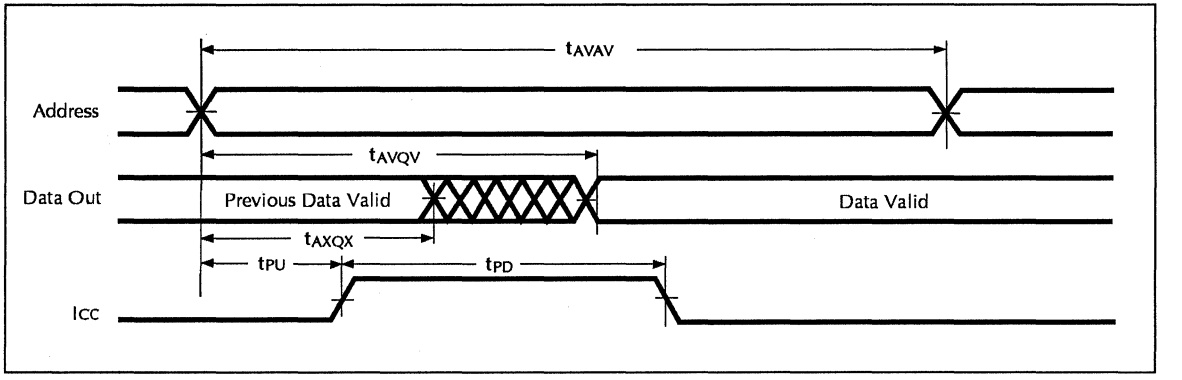
		L7C168/170-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		30		15		15		10		10		8
tOLQV	Output Enable Low to Output Valid		35		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
tOHQZ	Output Enable High to Output High Z (20, 21)		30		15		12		10		8		8
tPU	$\overline{CE}$ or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

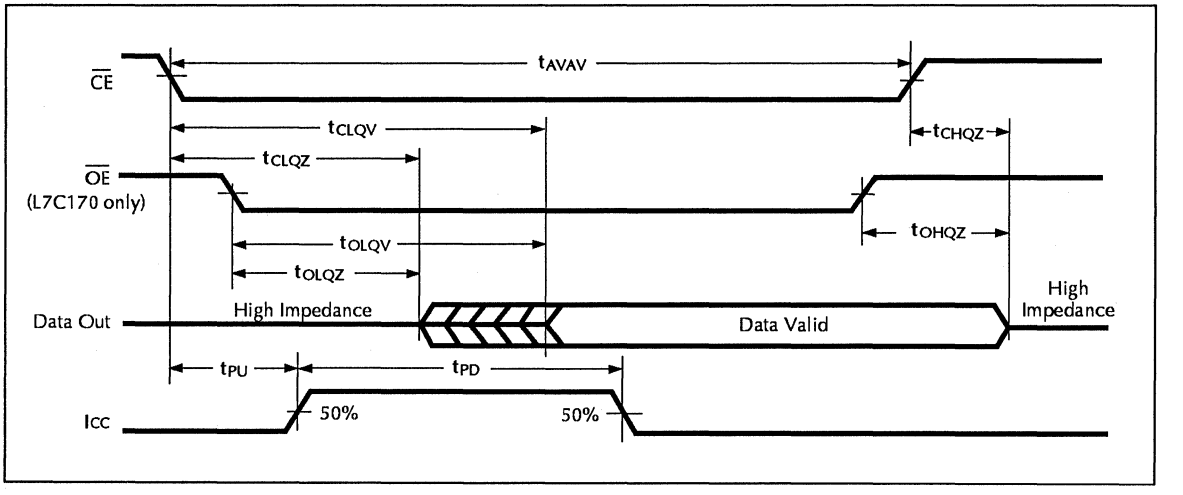
		L7C168/170-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		17		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		25		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

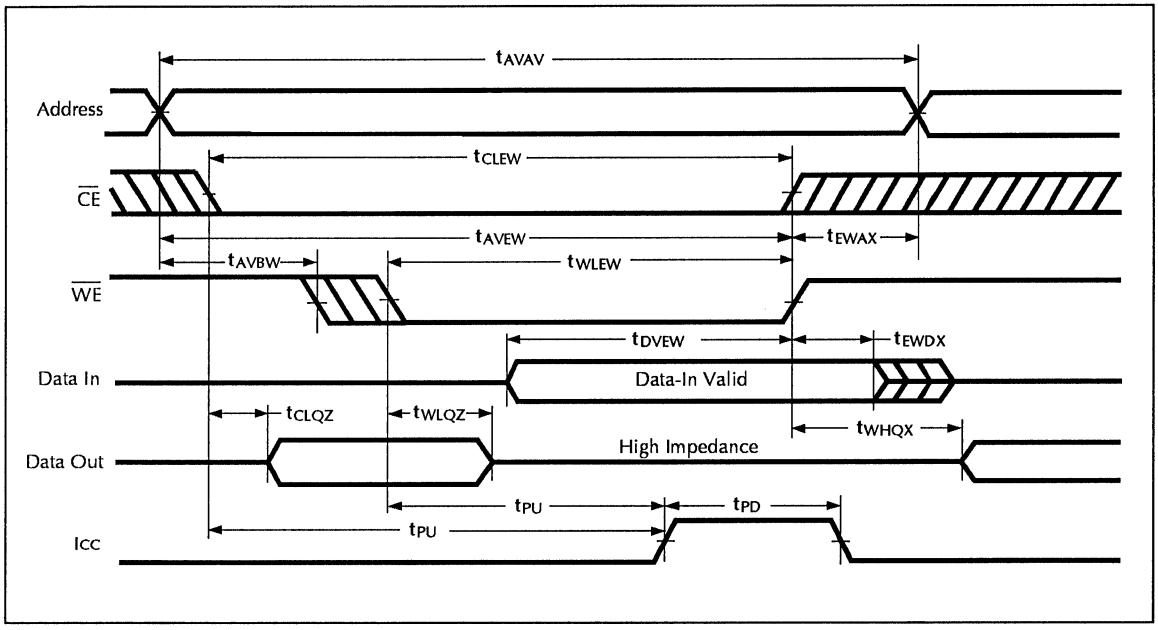
Read Cycle — Address Controlled *(Notes 13, 14)*



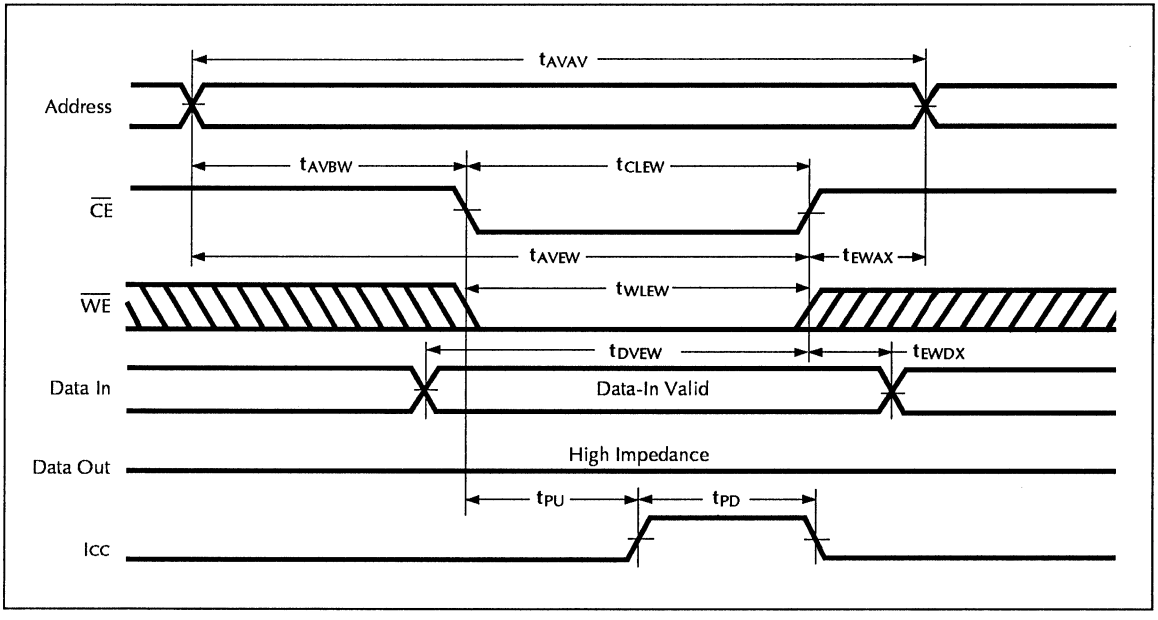
Read Cycle — $\overline{CE}/\overline{OE}$ Controlled *(Notes 13, 15)*



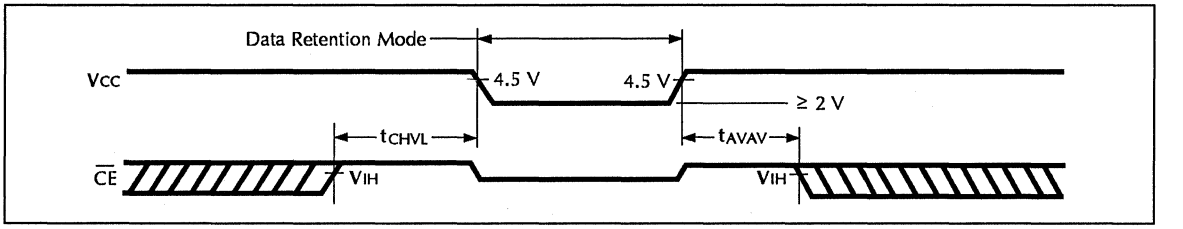
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

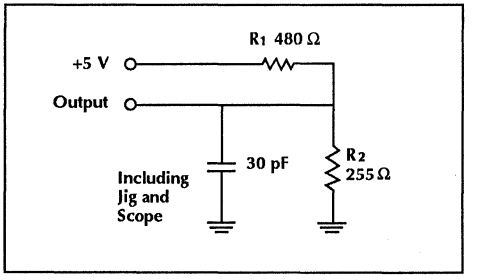


Figure 1b

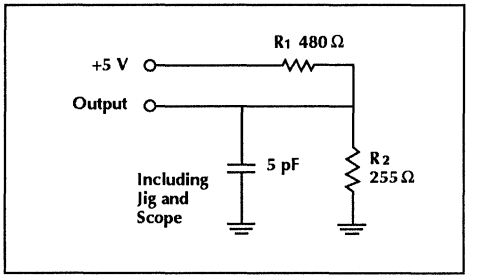
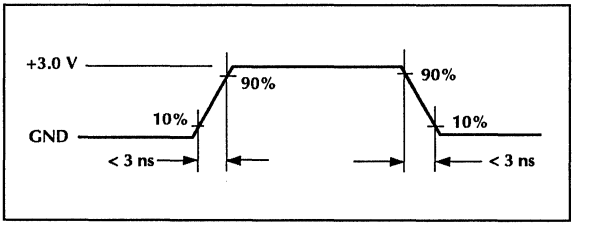


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
L7C168						
20-pin Plastic DIP (0.3") — P6	L7C168PC85	L7C168PC45	L7C168PC35	L7C168PC25	L7C168PC20	L7C168PC15
20-pin Sidebraze (0.3") Hermetic DIP — D7	L7C168DC85	L7C168DC45	L7C168DC35	L7C168DC25	L7C168DC20	L7C168DC15
20-pin Plastic SOIC — U3	L7C168UC85	L7C168UC45	L7C168UC35	L7C168UC25	L7C168UC20	L7C168UC15
20-pin Plastic SOJ — W3	L7C168WC85	L7C168WC45	L7C168WC35	L7C168WC25	L7C168WC20	L7C168WC15
20-pin CerDIP (0.3") — C2	L7C168CC85	L7C168CC45	L7C168CC35	L7C168CC25	L7C168CC20	L7C168CC15
20-pin Ceramic LCC — K6	L7C168KC85	L7C168KC45	L7C168KC35	L7C168KC25	L7C168KC20	L7C168KC15
L7C170						
22-pin Plastic DIP (0.3") — P8	L7C170PC85	L7C170PC45	L7C170PC35	L7C170PC25	L7C170PC20	L7C170PC15
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C170DC85	L7C170DC45	L7C170DC35	L7C170DC25	L7C170DC20	L7C170DC15
22-pin CerDIP (0.3") — C3	L7C170CC85	L7C170CC45	L7C170CC35	L7C170CC25	L7C170CC20	L7C170CC15

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
L7C168						
20-pin Sidebraze (0.3") Hermetic DIP — D7	L7C168DM85 L7C168DME85 L7C168DMB85	L7C168DM45 L7C168DME45 L7C168DMB45	L7C168DM35 L7C168DME35 L7C168DMB35	L7C168DM25 L7C168DME25 L7C168DMB25	L7C168DM20 L7C168DME20 L7C168DMB20	
20-pin CerDIP (0.3") — C2	L7C168CM85 L7C168CME85 L7C168CMB85	L7C168CM45 L7C168CME45 L7C168CMB45	L7C168CM35 L7C168CME35 L7C168CMB35	L7C168CM25 L7C168CME25 L7C168CMB25	L7C168CM20 L7C168CME20 L7C168CMB20	
20-pin Ceramic LCC — K6	L7C168KM85 L7C168KME85 L7C168KMB85	L7C168KM45 L7C168KME45 L7C168KMB45	L7C168KM35 L7C168KME35 L7C168KMB35	L7C168KM25 L7C168KME25 L7C168KMB25	L7C168KM20 L7C168KME20 L7C168KMB20	
L7C170						
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C170DM85 L7C170DME85 L7C170DMB85	L7C170DM45 L7C170DME45 L7C170DMB45	L7C170DM35 L7C170DME35 L7C170DMB35	L7C170DM25 L7C170DME25 L7C170DMB25	L7C170DM20 L7C170DME20 L7C170DMB20	
22-pin CerDIP (0.3") — C3	L7C170CM85 L7C170CME85 L7C170CMB85	L7C170CM45 L7C170CME45 L7C170CMB45	L7C170CM35 L7C170CME35 L7C170CMB35	L7C170CM25 L7C170CME25 L7C170CMB25	L7C170CM20 L7C170CME20 L7C170CMB20	

L7C168 Pin Assignments *(P6, D7, C2, K6, U3, W3)*

Pin	Function	Pin	Function
1	A_0	11	$\overline{WE}$
2	A_1	12	I_0/O_0
3	A_2	13	I_1/O_1
4	A_3	14	I_2/O_2
5	A_4	15	I_3/O_3
6	A_5	16	A_8
7	A_6	17	A_9
8	A_7	18	A_{10}
9	$\overline{CE}$	19	A_{11}
10	GND	20	V_{CC}

L7C170 Pin Assignments *(P8, D8, C3)*

Pin	Function	Pin	Function
1	A_0	12	$\overline{WE}$
2	A_1	13	I_0/O_0
3	A_2	14	I_1/O_1
4	A_3	15	I_2/O_2
5	A_4	16	I_3/O_3
6	A_5	17	*NC*
7	A_6	18	A_8
8	A_7	19	A_9
9	$\overline{CE}$	20	A_{10}
10	$\overline{OE}$	21	A_{11}
11	GND	22	V_{CC}

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Features

- 4K by 4 Static RAM with separate I/O, transparent write (L7C171), or high impedance write (L7C172)
- Auto-PowerDown™ design
- Advanced CMOS technology
- High speed — to 15 ns worst case
- Low Power Operation
  Active: 170 mW typical at 45 ns
  Standby: 12.5 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 71681/71682, Cypress CY7C171/172
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 28-pin Ceramic LCC

Description

The **L7C171** and **L7C172** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out are separate. Parts are available in five speed categories with worst-case access times from 15 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 170 mW (typical) when operating at 45 ns. Dissipation drops to 20 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-PowerDown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C171 and L7C172 consumes only 1 µW (typical) at 2 V, allowing effective battery back-up operation.

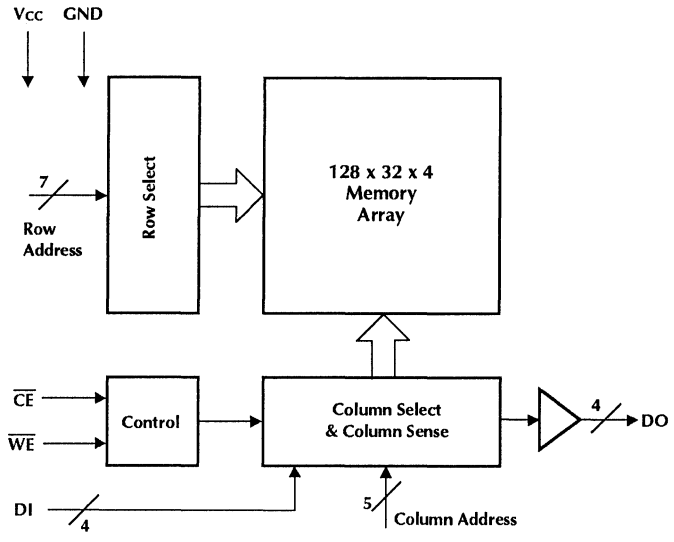
The L7C171 and L7C172 provides asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state output bus output with a bus control line simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{11}. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while Write remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is low (L7C172 only) or $\overline{CE}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Each of these signals may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C171 and L7C172 can withstand an injection current of up to 100 mA on any page without damage.

L7C171/172 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	−3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			−350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		4.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		0.5	10	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		5	500	nA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C171/172-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	25	45	55	75	95	120	mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle (Notes 11, 12, 22, 23, 24)

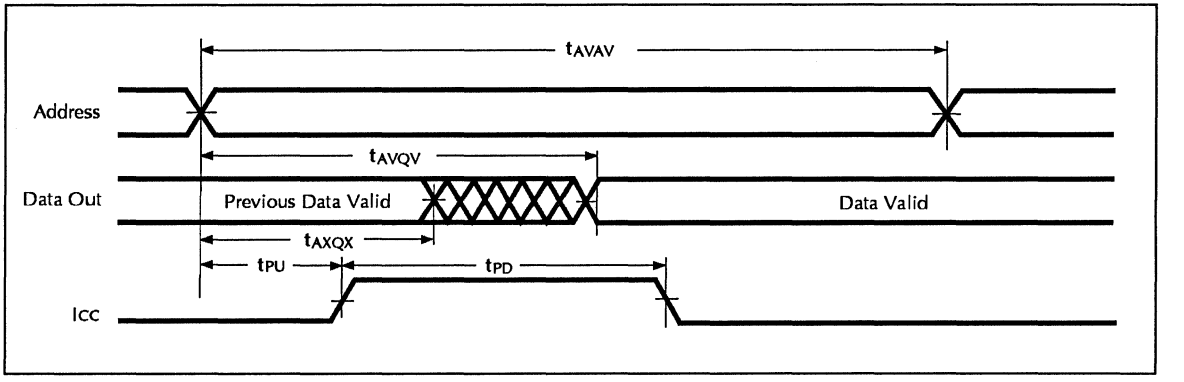
		L7C171/172-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		30		15		15		10		8		8
tPU	CE or WE Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle (Notes 11, 12, 21, 22, 23, 24)

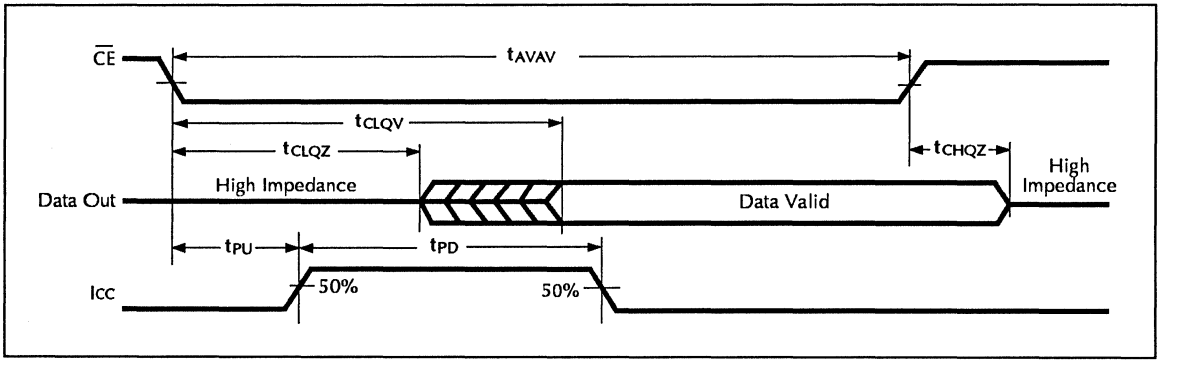
		L7C171/172-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		17		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	65		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	
tWLQV	Write Enable Low to Output Valid		50		35		30		20		15		15
tDVQV	Data Valid to Output Valid		50		35		30		20		15		15

Switching Waveforms

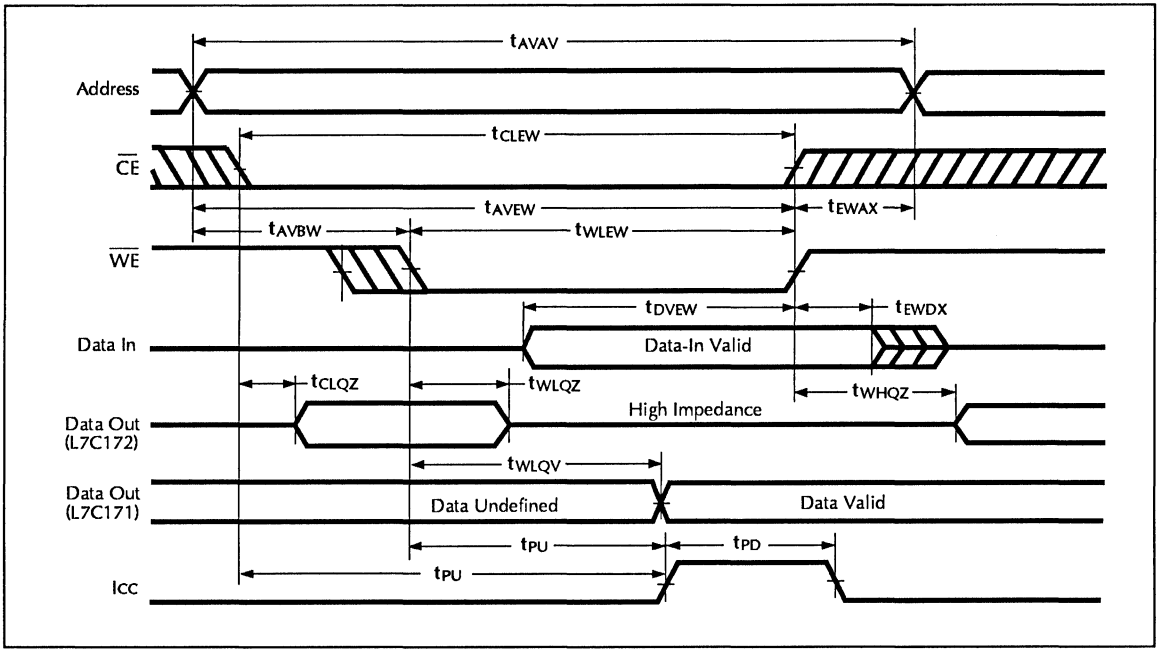
Read Cycle — Address Controlled *(Notes 13, 14)*



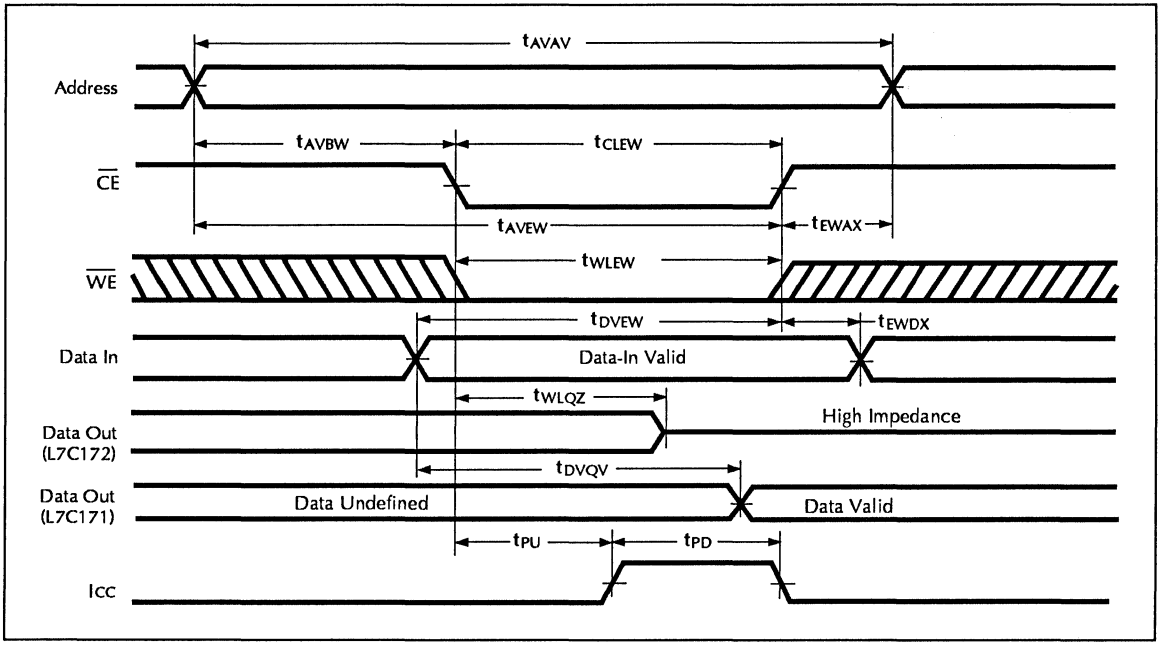
Read Cycle — $\overline{CE}$ Controlled *(Notes 13, 15)*



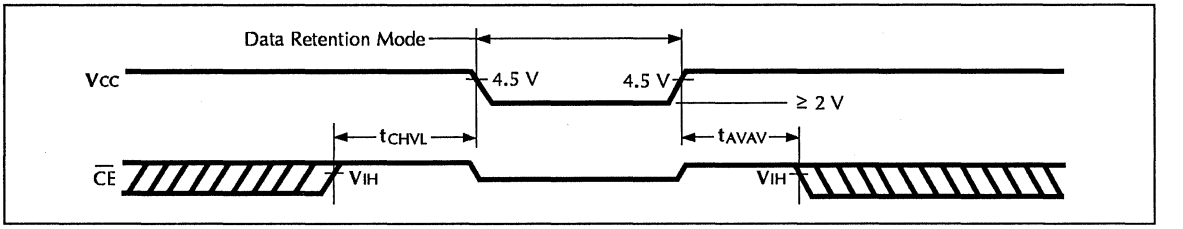
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

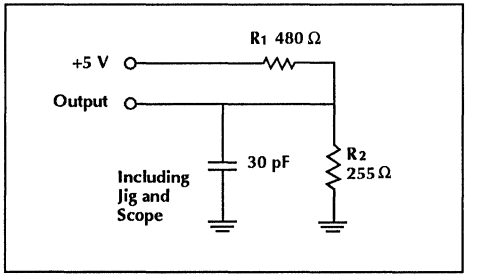


Figure 1b

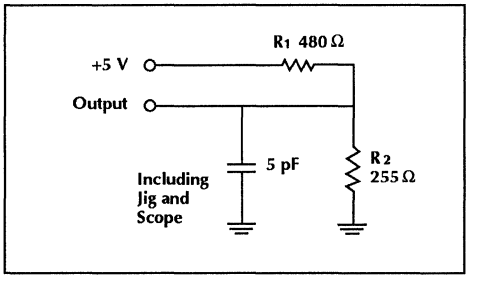
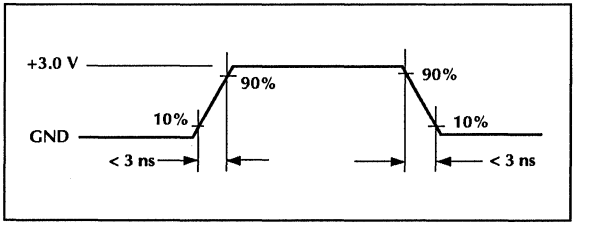


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
L7C171						
24-pin Plastic DIP (0.3") — P2	L7C171PC85	L7C171PC45	L7C171PC35	L7C171PC25	L7C171PC20	L7C171PC15
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C171DC85	L7C171DC45	L7C171DC35	L7C171DC25	L7C171DC20	L7C171DC15
24-pin CerDIP (0.3") — C1	L7C171CC85	L7C171CC45	L7C171CC35	L7C171CC25	L7C171CC20	L7C171CC15
28-pin Ceramic LCC — K7	L7C171KC85	L7C171KC45	L7C171KC35	L7C171KC25	L7C171KC20	L7C171KC15
L7C172						
24-pin Plastic DIP (0.3") — P2	L7C172PC85	L7C172PC45	L7C172PC35	L7C172PC25	L7C172PC20	L7C172PC15
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C172DC85	L7C172DC45	L7C172DC35	L7C172DC25	L7C172DC20	L7C172DC15
24-pin CerDIP (0.3") — C1	L7C172CC85	L7C172CC45	L7C172CC35	L7C172CC25	L7C172CC20	L7C172CC15
28-pin Ceramic LCC — K7	L7C172KC85	L7C172KC45	L7C172KC35	L7C172KC25	L7C172KC20	L7C172KC15

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
L7C171						
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C171DM85 L7C171DME85 L7C171DMB85	L7C171DM45 L7C171DME45 L7C171DMB45	L7C171DM35 L7C171DME35 L7C171DMB35	L7C171DM25 L7C171DME25 L7C171DMB25	L7C171DM20 L7C171DME20 L7C171DMB20	
24-pin CerDIP (0.3") — C1	L7C171CM85 L7C171CME85 L7C171CMB85	L7C171CM45 L7C171CME45 L7C171CMB45	L7C171CM35 L7C171CME35 L7C171CMB35	L7C171CM25 L7C171CME25 L7C171CMB25	L7C171CM20 L7C171CME20 L7C171CMB20	
28-pin Ceramic LCC — K7	L7C171KM85 L7C171KME85 L7C171KMB85	L7C171KM45 L7C171KME45 L7C171KMB45	L7C171KM35 L7C171KME35 L7C171KMB35	L7C171KM25 L7C171KME25 L7C171KMB25	L7C171KM20 L7C171KME20 L7C171KMB20	
L7C172						
24-pin Sidebraze (0.3") Hermetic DIP — D2	L7C172DM85 L7C172DME85 L7C172DMB85	L7C172DM45 L7C172DME45 L7C172DMB45	L7C172DM35 L7C172DME35 L7C172DMB35	L7C172DM25 L7C172DME25 L7C172DMB25	L7C172DM20 L7C172DME20 L7C172DMB20	
24-pin CerDIP (0.3") — C1	L7C172CM85 L7C172CME85 L7C172CMB85	L7C172CM45 L7C172CME45 L7C172CMB45	L7C172CM35 L7C172CME35 L7C172CMB35	L7C172CM25 L7C172CME25 L7C172CMB25	L7C172CM20 L7C172CME20 L7C172CMB20	
28-pin Ceramic LCC — K7	L7C172KM85 L7C172KME85 L7C172KMB85	L7C172KM45 L7C172KME45 L7C172KMB45	L7C172KM35 L7C172KME35 L7C172KMB35	L7C172KM25 L7C172KME25 L7C172KMB25	L7C172KM20 L7C172KME20 L7C172KMB20	

Pin Assignments

(24-pin — P2, D2, C1)

Pin	Function	Pin	Function
1	A0	13	$\overline{WE}$
2	A1	14	O0
3	A2	15	O1
4	A3	16	O2
5	A4	17	O3
6	A5	18	I2
7	A6	19	I3
8	A7	20	A8
9	I0	21	A9
10	I1	22	A10
11	$\overline{CE}$	23	A11
12	GND	24	VCC

Pin Assignments

(28-pin — K7)

Pin	Function	Pin	Function
1	A0	15	$\overline{WE}$
2	A1	16	O0
3	A2	17	O1
4	A3	18	O2
5	A4	19	O3
6	A5	20	I2
7	*NC*	21	*NC*
8	*NC*	22	*NC*
9	A6	23	I3
10	A7	24	A8
11	I0	25	A9
12	I1	26	A10
13	$\overline{CE}$	27	A11
14	GND	28	VCC

628 East Evelyn Avenue • Sunnyvale, CA 94086 • Telephone 408-720-8630 • FAX 408-733-7690

Features

- 2K by 8 Static RAM with chip select powerdown, output enable
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 20 ns worst case
- Low Power Operation
  Active: 260 mW typical at 45 ns
  Standby: 12.5 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT6116, Cypress CY7C128/CY6116
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 24-pinPlastic SOIC(Gull-Wing)
  - 24-pin Plastic SOJ (J-Lead)
  - 28-pin Ceramic LCC

Description

The **L6116** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. Parts are available in five speeds with worst-case access times from 20 ns to 85 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 260 mW (typical) when being operated at 45 ns. Dissipation drops to 20 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 consumes only 1 µW at 2 V (typical), for effective battery back-up operation.

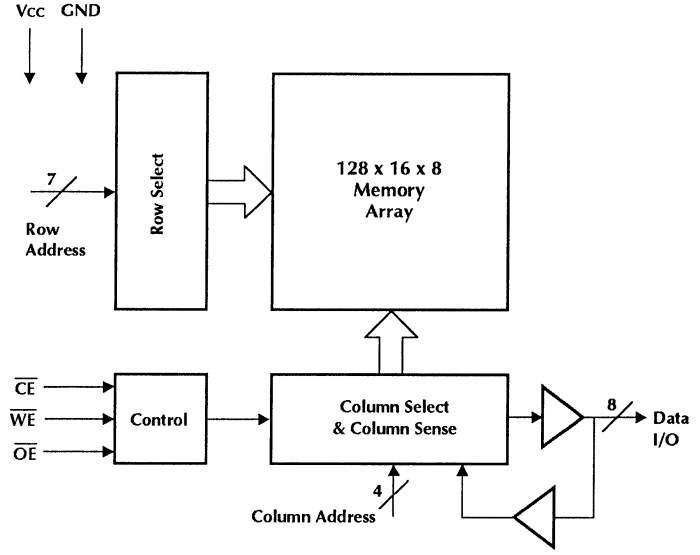
The L6116 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A10. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$, $\overline{OE}$, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 can withstand an injection current of up to 200 mA on any pin without damage.

L6116 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	Note 3	–3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4			–350	mA
I_{CC2}	V_{CC} Current, Inactive	Notes 5, 7		4.0	20	mA
I_{CC3}	V_{CC} Current, Standby	Note 8		0.5	10	µA
I_{CC4}	V_{CC} Current, DR Mode	V_{CC} = 2.0 V, Note 9		5	500	nA
C_I	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

Symbol	Parameter	Test Condition	L6116- 85	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	Notes 5, 6	25	70	90	125	155		mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 21, 22, 23, 24)*

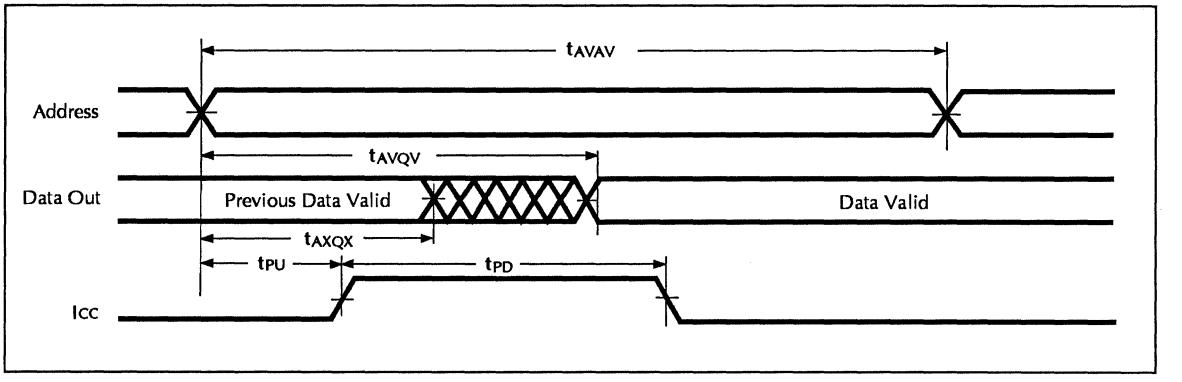
		L6116-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		30		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		35		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
tOHQZ	Output Enable High to Output High Z (20, 21)		30		15		12		10		8		8
tPU	$\overline{CE}$ or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

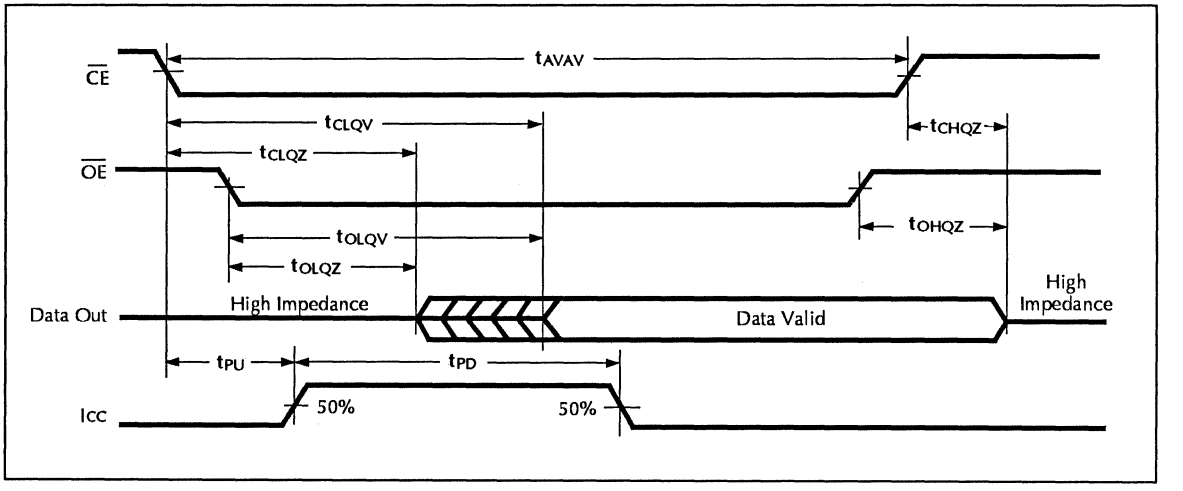
		L6116-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		17		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

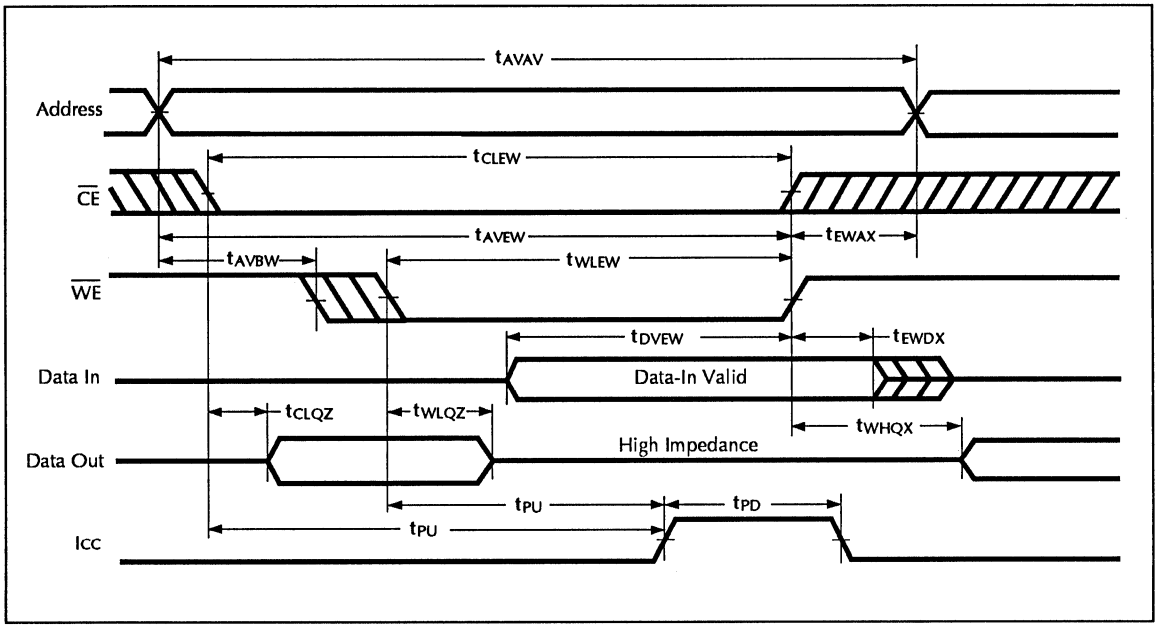
Read Cycle — Address Controlled *(Notes 13, 14)*



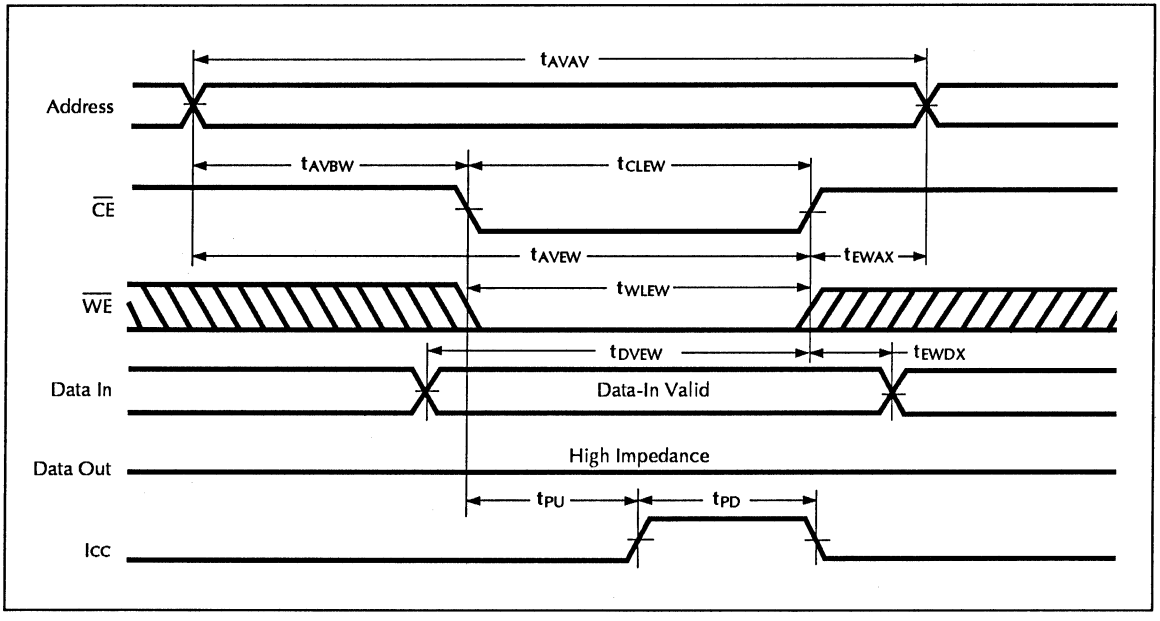
Read Cycle — $\overline{CE}/\overline{OE}$ Controlled *(Notes 13, 15)*



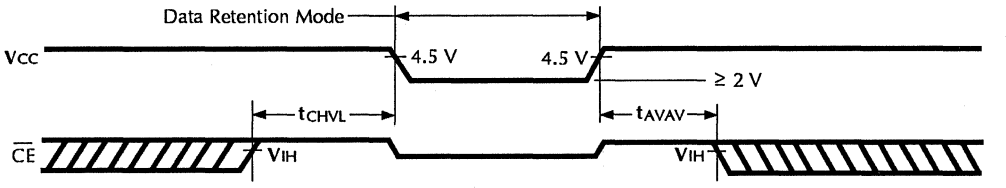
Write Cycle — $\overline{WE}$ Controlled *(Notes 16, 17, 18, 19)*



Write Cycle — $\overline{CE}$ Controlled *(Notes 16, 17, 18, 19)*



Data Retention



Test Loads and Transition Times

Figure 1a

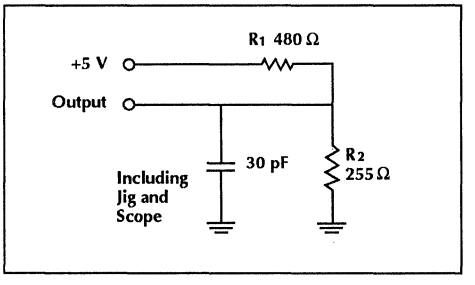


Figure 1b

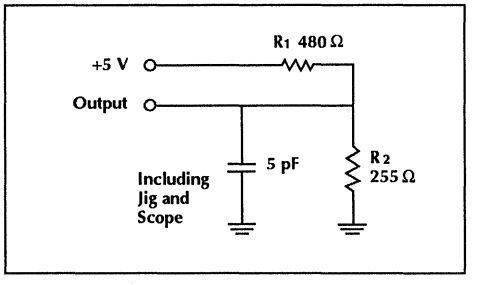
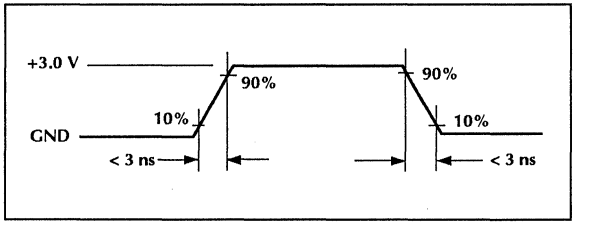


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
24-pin Plastic DIP (0.3") — P2	L6116PC85	L6116PC45	L6116PC35	L6116PC25	L6116PC20	
24-pin Plastic DIP (0.6") — P1	L6116NC85	L6116NC45	L6116NC35	L6116NC25	L6116NC20	
24-pin SOIC — U1	L6116UC85	L6116UC45	L6116UC35	L6116UC25	L6116UC20	
24-pin SOIC — U1	L6116WC85	L6116WC45	L6116WC35	L6116WC25	L6116WC20	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L6116DC85	L6116DC45	L6116DC35	L6116DC25	L6116DC20	
24-pin Sidebraze (0.6") Hermetic DIP — D1	L6116HC85	L6116HC45	L6116HC35	L6116HC25	L6116HC20	
24-pin CerDIP (0.3") — C1	L6116CC85	L6116CC45	L6116CC35	L6116CC25	L6116CC20	
24-pin CerDIP (0.6") — C4	L6116IC85	L6116IC45	L6116IC35	L6116IC25	L6116IC20	
28-pin Ceramic LCC — K7	L6116KC85	L6116KC45	L6116KC35	L6116KC25	L6116KC20	

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L6116DM85 L6116DME85 L6116DMB85	L6116DM45 L6116DME45 L6116DMB45	L6116DM35 L6116DME35 L6116DMB35	L6116DM25 L6116DME25 L6116DMB25		
24-pin Sidebraze (0.6") Hermetic DIP — D1	L6116HM85 L6116HME85 L6116HMB85	L6116HM45 L6116HME45 L6116HMB45	L6116HM35 L6116HME35 L6116HMB35	L6116HM25 L6116HME25 L6116HMB25		
24-pin CerDIP (0.3") — C1	L6116CM85 L6116CME85 L6116CMB85	L6116CM45 L6116CME45 L6116CMB45	L6116CM35 L6116CME35 L6116CMB35	L6116CM25 L6116CME25 L6116CMB25		
24-pin CerDIP (0.6") — C4	L6116IM85 L6116IME85 L6116IMB85	L6116IM45 L6116IME45 L6116IMB45	L6116IM35 L6116IME35 L6116IMB35	L6116IM25 L6116IME25 L6116IMB25		
28-pin Ceramic LCC — K7	L6116KM85 L6116KME85 L6116KMB85	L6116KM45 L6116KME45 L6116KMB45	L6116KM35 L6116KME35 L6116KMB35	L6116KM25 L6116KME25 L6116KMB25		

Pin Assignments

(P1, P2, D1, D2, C1, C4, U1, W1)

Pin	Function	Pin	Function
1	A7	13	I3/O3
2	A6	14	I4/O4
3	A5	15	I5/O5
4	A4	16	I6/O6
5	A3	17	I7/O7
6	A2	18	$\overline{CE}$
7	A1	19	A10
8	A0	20	$\overline{OE}$
9	I0/O0	21	$\overline{WE}$
10	I1/O1	22	A9
11	I2/O2	23	A8
12	GND	24	VCC

Pin Assignments

(K7)

Pin	Function	Pin	Function
1	A7	15	I3/O3
2	A6	16	I4/O4
3	A5	17	I5/O5
4	A4	18	I6/O6
5	A3	19	I7/O7
6	A2	20	$\overline{CE}$
7	*NC*	21	*NC*
8	*NC*	22	*NC*
9	A1	23	A10
10	A0	24	$\overline{OE}$
11	I0/O0	25	$\overline{WE}$
12	I1/O1	26	A9
13	I2/O2	27	A8
14	GND	28	VCC

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LOGIC

DEVICES INCORPORATED

Contents

Product Selection Guide

Part No.	Description	Maximum Speed (ns) Commercial	Maximum Speed (ns) Military	Power (mW)	Pins	Packages Available
MULTIPLIERS						
LMU08	8 x 8 Signed	35	45	40	40/44	DIP, LCC, PLCC
LMU8U	8 x 8 Unsigned					
LMU557	8 x 8 Latched Output	60	70	85	40	DIP
LMU558	8 x 8 Unregistered					
LMU12	12 x 12	35	45	60	64/68	DIP, Pin Grid Array
LMU112	12 x 12 Reduced Pinout	50	60	50	48	DIP
LMU16	16 x 16	45	55	60	64/68	DIP, Pin Grid Array
LMU216	16 x 16	45	55	60	68	LCC, PLCC
LMU17	16 x 16 Microprogrammable	45	55	60	64/68	DIP, Pin Grid Array
LMU217	16 x 16 Surface Mount	45	55	60	68	LCC, PLCC
LMU18	16 x 16/32 Outputs	35	45	150	84	Pin Grid Array, PLCC
MULTIPLIER ACCUMULATORS						
LMA1009	12 x 12	45	55	60	64/68	DIP, Pin Grid Array
LMA2009	12 x 12 Surface Mount	45	55	60	68	LCC, PLCC
LMA1010	16 x 16	45	55	60	64/68	DIP, Pin Grid Array
LMA2010	16 x 16 Surface Mount	45	55	60	68	LCC, PLCC
MULTIPLIER SUMMER						
LMS12	12 x 12 x 26 FIR	40	50	75	84	Pin Grid Array, PLCC
PIPELINE REGISTERS						
L29C520	4 x 8-Bit, Variable Delay, 1–4 Stages	22	24	50	24/28	DIP, LCC, PLCC
L29C521	4 x 8-Bit, Variable Delay, 1–4 Stages					Flat Pack
LPR520	4 x 16-Bit, Variable Delay, 1–4 Stages	22	24	50	40/44	DIP, LCC, PLCC
LPR521	4 x 16-Bit, Variable Delay, 1–4 Stages					
L29C524	14 x 8-Bit, Variable Delay, 0–14 Stages		Call Factory		28	DIP, LCC
L29C525	16 x 8-Bit, Variable Delay, 0–16 Stages		Call Factory		28	
L10C11	18 x 8-Bit, Variable Delay, 3–18 Stages		Call Factory		24	DIP
L29C818	Shadow Register		Call Factory		24	DIP
REGISTER FILES						
LRF07	8 x 8, 3 Independent Port	35	35	40	40	DIP, LCC
LRF08	8 x 8, 5 Independent Port	35	35	60	64/68	DIP, LCC, PLCC, Pin Grid Array
ARITHMETIC LOGIC UNITS						
L4C381	16-Bit, Add/Sub	26	30	60	68	Pin Grid Array, LCC, PLCC
L29C101	16-Bit Slice, Quad 2901	35	45	75	64/68	DIP, LCC, Pin Grid Array
SPECIAL FUNCTIONS						
LSH32	32-Bit Barrel Shifter	32	40	60	68	Pin Grid Array, LCC, PLCC
L10C23	64 x 1 Digital Correlator	20	20	125	24/28	DIP, LCC

Cross Reference Guide

LOGIC DEVICES		TRW	Analog Dev	IDT	Cypress	AMD	Weitek
LMU08	8 X 8 MULT	MPY008	ADSP1080				
LMU8U	8 X 8 MULT	MPY08U	ADSP1081				
LMU557	8 X 8 MULT					AM25S557 SN54557 SN74557	
LMU558	8 X 8 MULT					AM25S558 SN54558 SN74558	
LMU12	12 X 12 MULT	MPY012	ADSP1012	IDT7212			
LMU112	12 X 12 MULT	MPY112					
LMU16/ LMU216	16 X 16 MULT	MPY016 TMC216	ADSP1016	IDT7216	CY7C516	AM29516 AM29C516	WTL1016 WTL1516
LMU17/ LMU217	16 X 16 MULT		ADSP1017	IDT7217	CY7C517	AM29517 AM29C517	
LMA1009/ LMA2009	12 X 12 MAC	TDC1009 TMC2009 TMC2109	ADSP1009	IDT7209			
LMA1010/ LMA2010	16 X 16 MAC	TDC1010 TMC2010 TMC2110 TMC2210	ADSP1010	IDT7210	CY7510	AM29510 AM29C510	WTL1010 WTL2010

LOGIC DEVICES		AMD	Performance	Wafer Scale	Intersil	IDT
L29C520-1	PIPELINE REGISTER	AM29520A 29C520CNS	P29PCT520	WS59520	ISP9520	IDT29FCT520A
L29C521-1	PIPELINE REGISTER	AM29521A	P29PCT521	WS59521	ISP9521	IDT29FCT521A

LOGIC DEVICES		TRW	IDT	Cypress	AMD
L29C101	16-BIT ALU		IDT49C401	CY7C9101	AM29C101
L10C23	CORRELATOR	TDC1023J			

8 x 8-bit Parallel Multiplier — LMU08/LMU8U

Features

- 35 ns worst-case multiply time
- Low-power CMOS technology
- LMU08 replaces TRW MPY008H
- LMU8U replaces TRW MPY08HU
- Two's complement (LMU08), or unsigned (LMU8U) operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead (LMU08 only)
  - 44-pin Ceramic LCC (Type C)

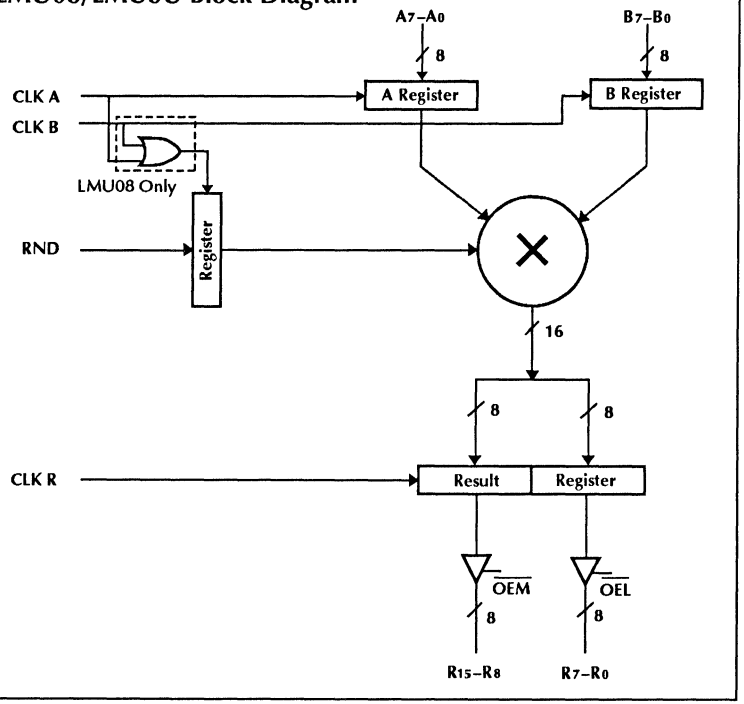
Description

The **LMU08** and **LMU8U** are 8-bit parallel multipliers which feature high speed with low power consumption. They are pin-for-pin equivalents with TRW MPY08H and MPY008HU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

LMU08/LMU8U Block Diagram



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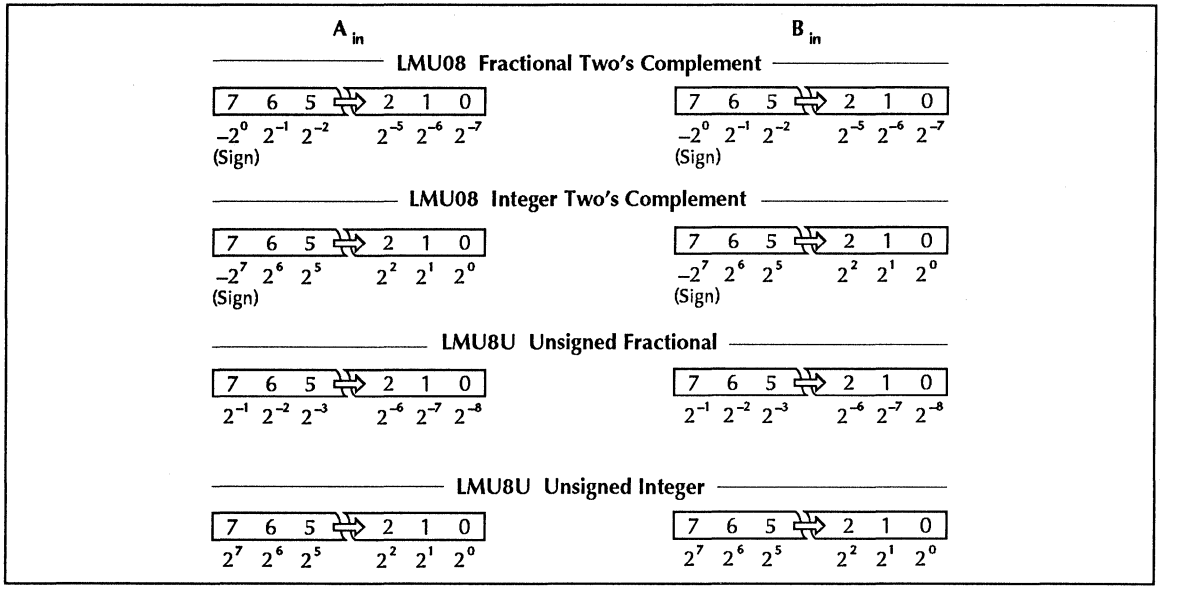
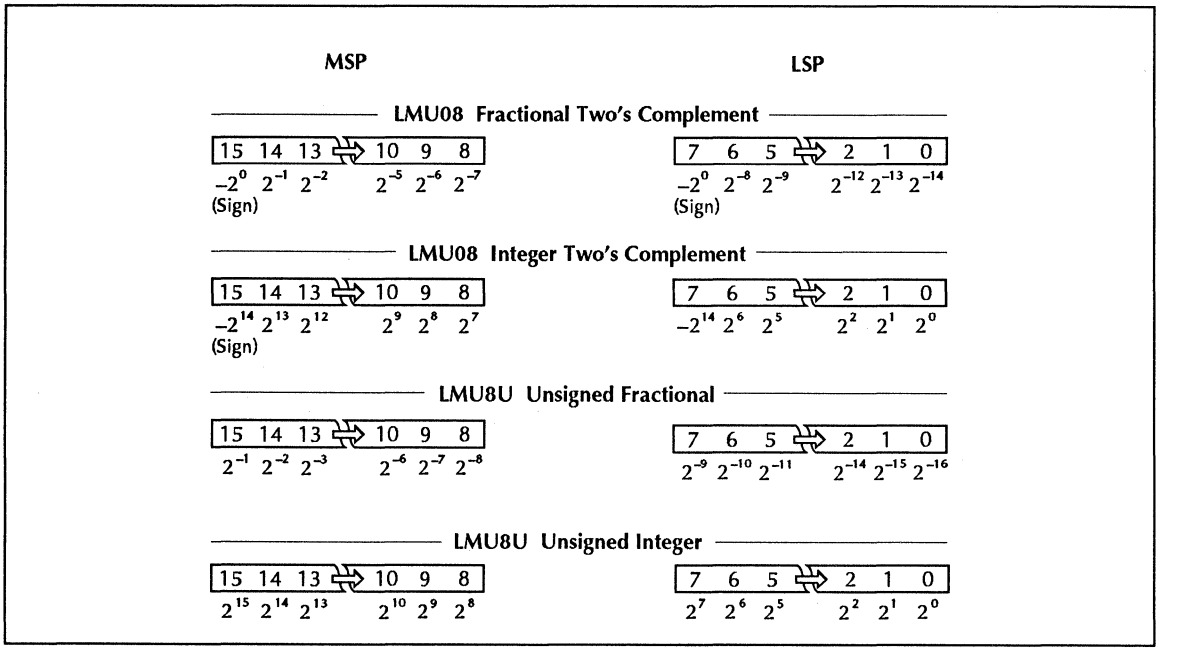
Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		8	24	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

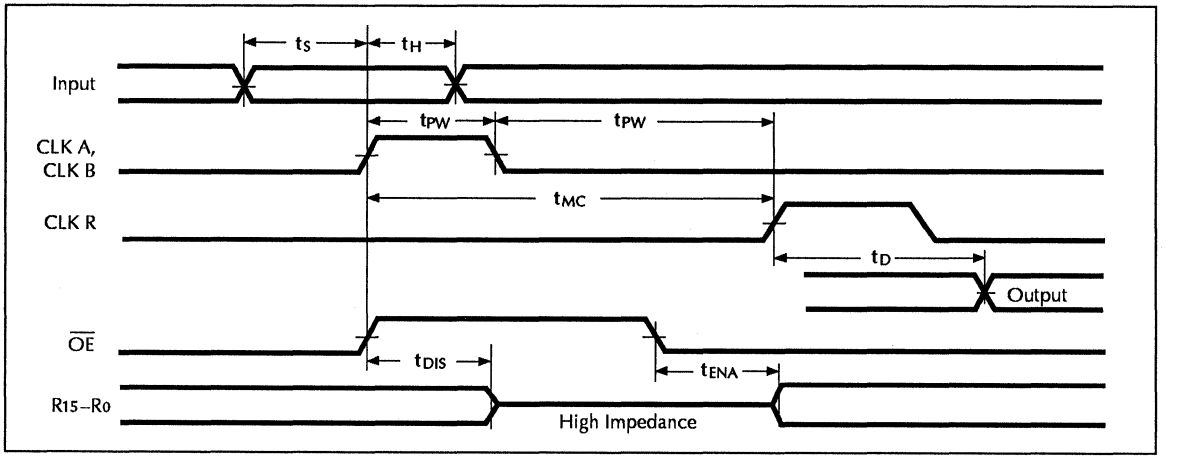
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU08/8U-70		LMU08/8U-50		LMU08/8U-35	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		70		50		35
t_D	Output Delay		25		18		16
t_{ENA}	Output Enable Time (Note 11)		20		18		18
t_{DIS}	Output Disable Time (Note 11)		18		17		17
t_{PW}	Clock Pulse Width	20		20		10	
t_H	Input Register Hold Time	4		0		0	
t_S	Input Register Setup Time	12		12		12	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU08/8U-90		LMU08/8U-60		LMU08/8U-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		90		60		45
t_D	Output Delay		35		20		20
t_{ENA}	Output Enable Time (Note 11)		35		20		20
t_{DIS}	Output Disable Time (Note 11)		35		18		18
t_{PW}	Clock Pulse Width	25		20		15	
t_H	Input Register Hold Time	5		0		0	
t_S	Input Register Setup Time	20		12		12	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	70 ns	50 ns	35 ns	
LMU08				
40-pin Plastic DIP (0.6") — P3	LMU08PC70	LMU08PC50	LMU08PC35	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU08DC70	LMU08DC50	LMU08DC35	
44-pin Plastic LCC, J-Lead — J1	LMU08JC70	LMU08JC50	LMU08JC35	
44-pin Ceramic LCC — K2	LMU08KC70	LMU08KC50	LMU08KC35	
LMU8U				
40-pin Plastic DIP (0.6") — P3	LMU8UPC70	LMU8UPC50	LMU8UPC35	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU8UDC70	LMU8UDC50	LMU8UDC35	
44-pin Ceramic LCC — K2	LMU8UKC70	LMU8UKC50	LMU8UKC35	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	90 ns	60 ns	45 ns	
LMU08				
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU08DM90 LMU08DME90 LMU08DMB90	LMU08DM60 LMU08DME60 LMU08DMB60	LMU08DM45 LMU08DME45 LMU08DMB45	
LMU8U				
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU8UDM90 LMU8UDME90 LMU8UDMB90	LMU8UDM60 LMU8UDME60 LMU8UDMB60	LMU8UDM45 LMU8UDME45 LMU8UDMB45	

Pin Assignments

Pin		Function	Pin		Function
D,P	J,K		D,P	J,K	
1	1	R10	23	25	CLK A
2	2	R9	24	26	CLK B
3	3	R8	25	27	RND
4	4	CLK R	26	29	B0
5	5	$\overline{OEM}$	27	30	B1
6	7	$\overline{OEL}$	28	31	B2
7	8	R7 (RSL)	29	32	B3
8	9	R6	30	33	Vcc
9	10	R5	31	34	B4
10	11	R4	32	35	GND
11	12	R3	33	36	B5
12	13	R2	34	37	B6
13	14	R1	35	38	B7 (BS)
14	15	R0	36	40	R15 (RSM)
15	16	A0	37	41	R14
16	18	A1	38	42	R13
17	19	A2	39	43	R12
18	20	A3	40	44	R11
19	21	A4		6	*NC*
20	22	A5		17	*NC*
21	23	A6		28	*NC*
22	24	A7 (AS)		39	*NC*

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8 x 8-bit Parallel Multiplier

LMU557/558

Features

- 60 ns worst-case multiply time
- Low-power CMOS technology
- Replaces Am25S557/558, 54S557/558
- Fully combinatorial, no clocks required
- Two's complement, unsigned, or mixed operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP

Description

The **LMU557** and **LMU558** are 8-bit parallel multipliers with high speed and low power operation. They are pin for pin equivalents with 54S557 and 54S558 type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

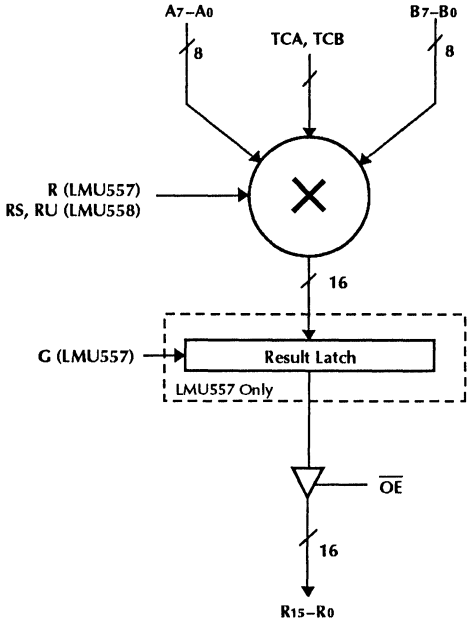
Both the LMU557 and LMU558 produce the 16-bit product of two 8-bit signed or unsigned numbers in a single unclocked operation. Assertion of control inputs TCA and TCB indicate that the corresponding input value is in two's complement notation.

Provision is made for proper rounding for any combination of signed or unsigned inputs. The RU input to the LMU557 causes the product to be rounded to 8 bits of precision for unsigned or mixed mode multiplication. For multiplication of two signed operands, the RS input is used for rounding, and the most significant bit of the product is discarded. [It will be identical to the sign bit for all except the $(-2^8)*(-2^8)$ case, which will cause overflow if the result MSB is not considered.]

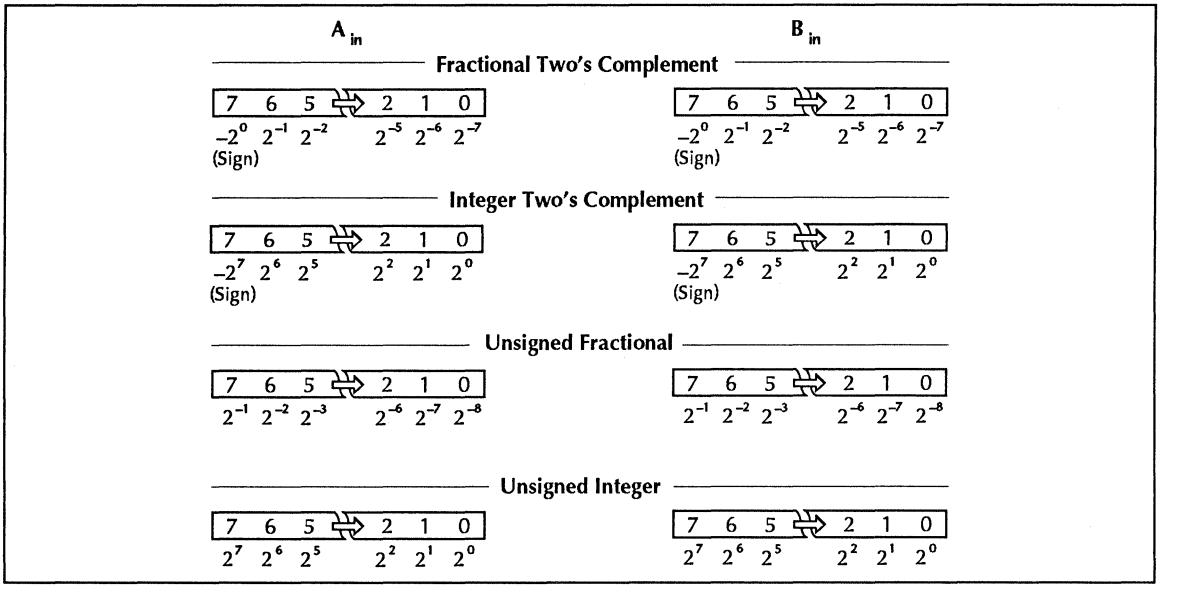
The LMU558 internally produces the RU and RS controls from a single round input, denoted R. With R asserted, RS rounding occurs if either TCA or TCB is asserted, while RU rounding is implemented for TCA and TCB not asserted. This implementation frees a pin for control of the transparent output latch in the LMU557 via the G input.

Both the LMU557 and LMU558 offer three-state output buffers controlled by the $\overline{OE}$ input. The LMU557 has a 16-bit transparent latch between the multiplier array and the output drivers for flexibility in implementing pipelined systems. This latch is transparent when G is high, and holds its state when G is low. In addition both polarities of the result MSB (R_{15}) are available as separate output pins to allow simple expansion to longer word lengths in signed multiplication.

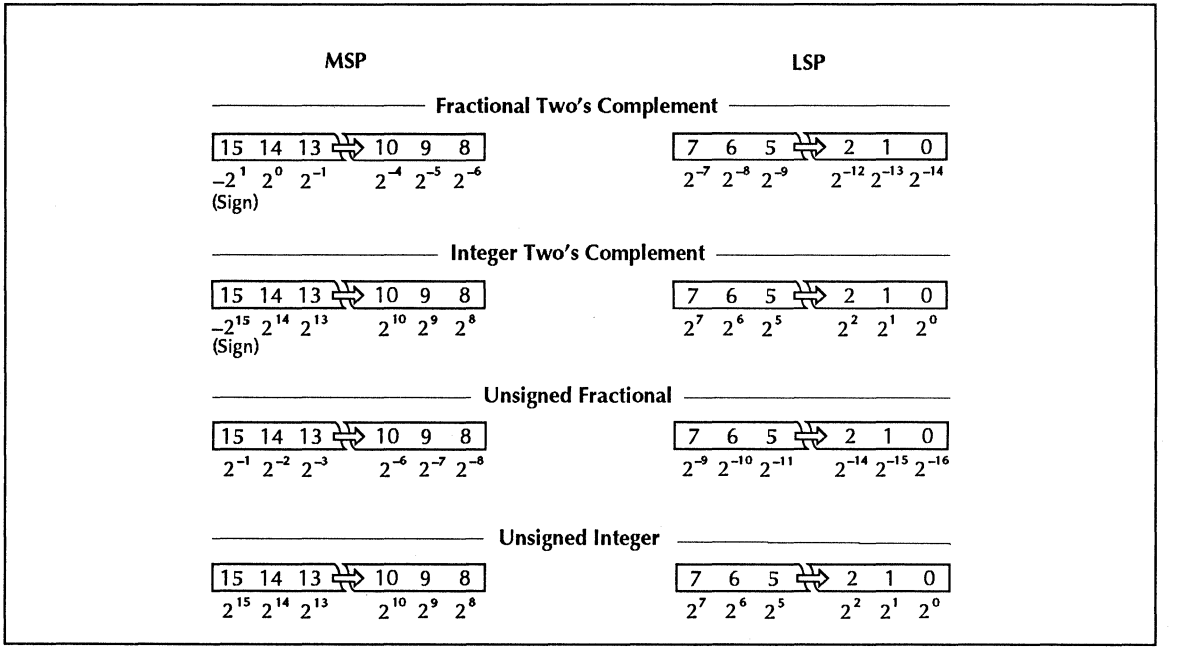
LMU557/558 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

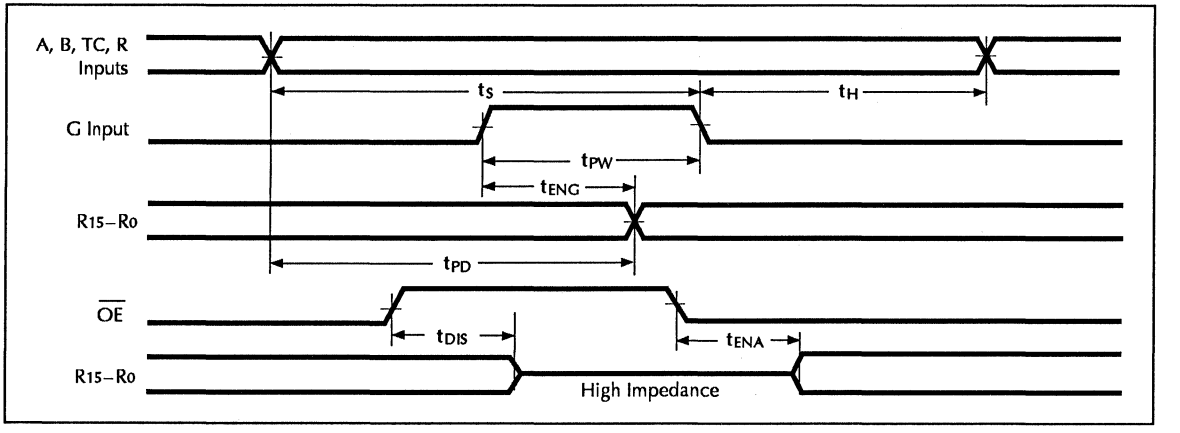
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU557/558-60 Min	LMU557/558-60 Max
t_{PD}	A, B, TC, R Inputs to R15–R8, $\overline{R15}$		60
t_{PD}	A, B, TC, R Inputs to R7–R0		55
t_{ENG}	G Enable to Result		30
t_{ENA}	Output Enable Time (Note 11)		25
t_{DIS}	Output Disable Time (Note 11)		20
t_{PW}	G Pulse Width	15	
t_H	G to A, B, TC, R Hold Time	0	
t_S	A, B, TC, R, Inputs to G Setup Time	45	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU557/558-70 Min	LMU557/558-70 Max
t_{PD}	A, B, TC, R Inputs to R15–R8, $\overline{R15}$		70
t_{PD}	A, B, TC, R Inputs to R7–R0		60
t_{ENG}	G Enable to Result		35
t_{ENA}	Output Enable Time (Note 11)		30
t_{DIS}	Output Disable Time (Note 11)		25
t_{PW}	G Pulse Width	20	
t_H	G to A, B, TC, R Hold Time	0	
t_S	A, B, TC, R, Inputs to G Setup Time	55	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance 60 ns
LMU557	
40-pin Plastic DIP (0.6") — P3	LMU557PC60
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU557DC60
LMU558	
40-pin Plastic DIP (0.6") — P3	LMU558PC60
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU558DC60

Military Operating Range (–55°C to +125°C)

Package Style	Performance 70 ns
LMU557	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU557DM70 LMU557DME70 LMU557DMB70
LMU558	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LMU558DM70 LMU558DME70 LMU558DMB70

Pin Assignments

Pin	Function	Pin	Function
1	A_0	21	$\overline{OE}$
2	A_1	22	$\overline{R15}$
3	A_2	23	R_{15}
4	A_3	24	R_{14}
5	A_4	25	R_{13}
6	A_5	26	R_{12}
7	A_6	27	R_{11}
8	A_7	28	R_{10}
9	RS/R	29	R9
10	V_{CC}	30	GND
11	RU/G	31	R_8
12	B_0	32	R_7
13	B_1	33	R_6
14	B_2	34	R_5
15	B_3	35	R_4
16	B_4	36	R_3
17	B_5	37	R_2
18	B_6	38	R_1
19	B_7	39	R_0
20	TCB	40	TCA

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12 x 12-bit Parallel Multiplier — LMU12

Features

- 35 ns worst-case multiply time
- Low-power CMOS technology
- Replaces TRW MPY12HJ
- Two's complement, unsigned, or mixed operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Pin Grid Array

Description

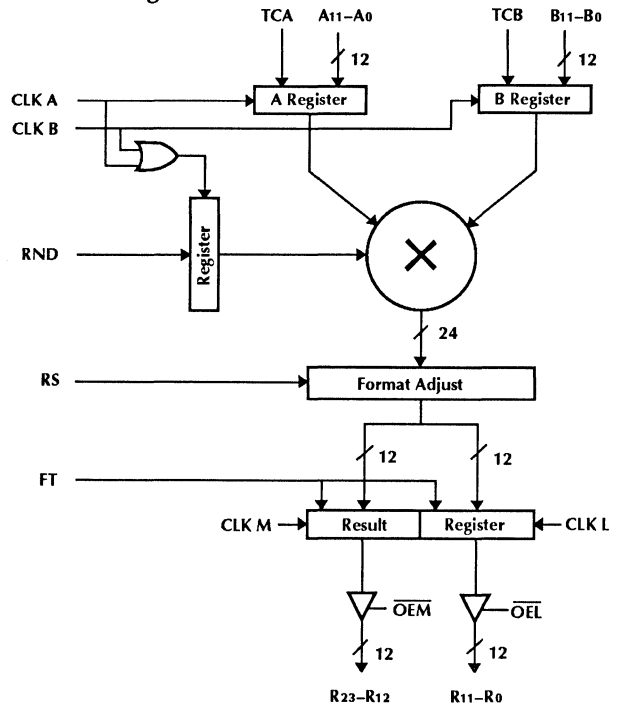
The **LMU12** is a 12-bit parallel multiplier with high speed and low power consumption. It is pin and functionally compatible with TRW MPY12HJ devices. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU12 produces the 24-bit product of two 12-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded by CLK B. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

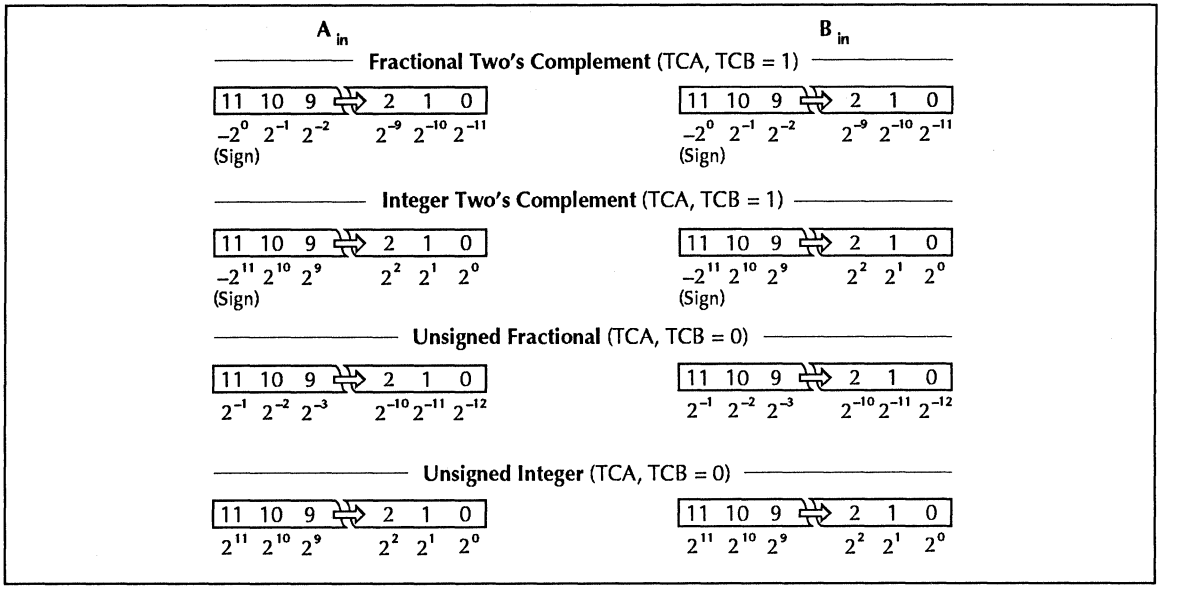
At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. Rs high gives a full 32-bit product. Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

LMU12 Block Diagram

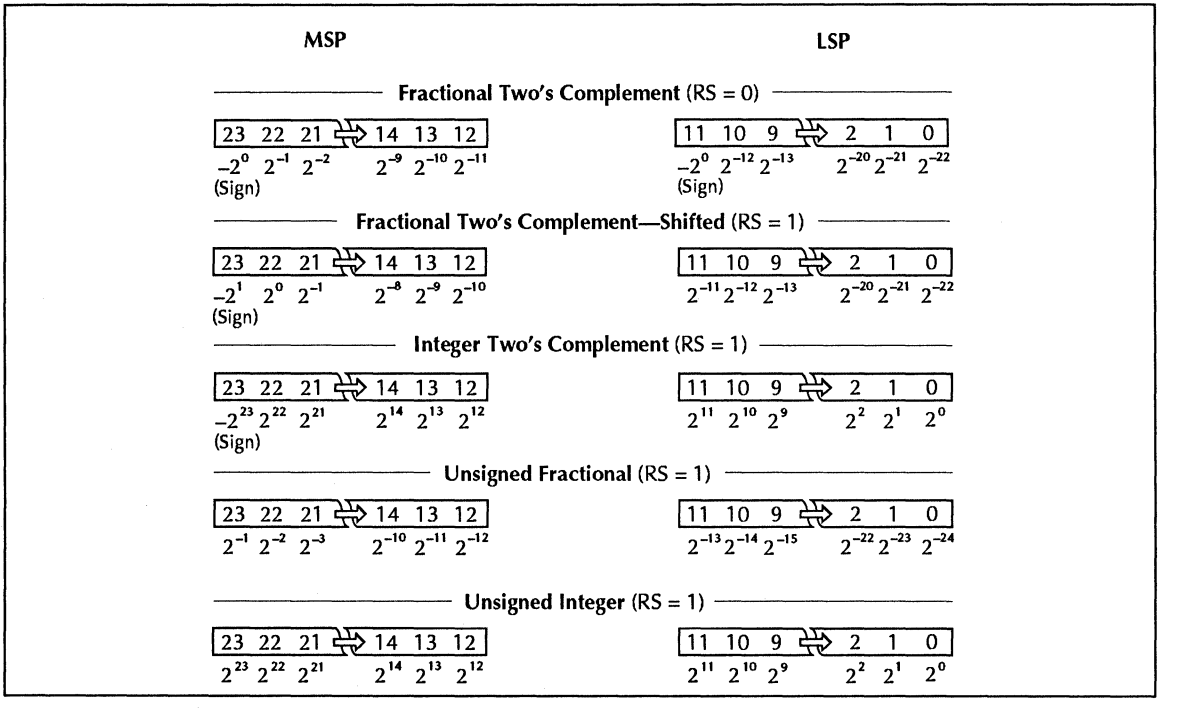


3

Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

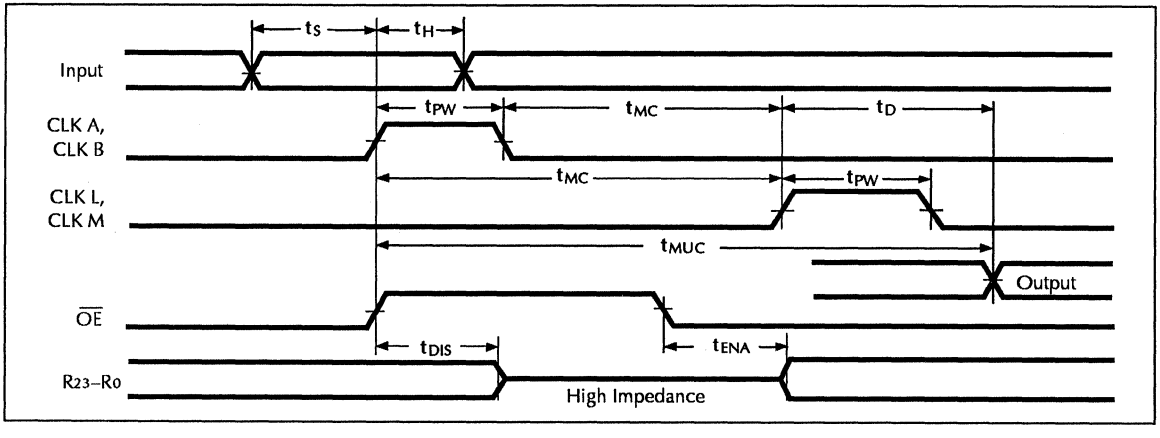
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU12-65		LMU12-45		LMU12-35	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		45		35
t_{MUC}	Unclocked Multiply Time		95		65		55
t_D	Output Delay		26		25		25
t_{ENA}	Output Enable Time (Note 11)		22		22		20
t_{DIS}	Output Disable Time		20		20		18
t_{PW}	Clock Pulse Width	25		15		15	
t_H	Input Register Hold Time	0		0		0	
t_S	Input Register Setup Time	15		15		12	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU12-75		LMU12-55		LMU12-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_{MUC}	Unclocked Multiply Time		110		75		65
t_D	Output Delay		30		30		25
t_{ENA}	Output Enable Time (Note 11)		26		26		24
t_{DIS}	Output Disable Time		24		24		22
t_{PW}	Clock Pulse Width	25		20		15	
t_H	Input Register Hold Time	0		0		0	
t_S	Input Register Setup Time	18		15		12	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	45 ns	35 ns	
64-pin Plastic DIP (0.9") — P4	LMU12PC65	LMU12PC45	LMU12PC35	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU12DC65	LMU12DC45	LMU12DC35	
68-pin Pin Grid Array — G2	LMU12GC65	LMU12GC45	LMU12GC35	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	75 ns	55 ns	45 ns	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU12DM75 LMU12DME75 LMU12DMB75	LMU12DM55 LMU12DME55 LMU12DMB55	LMU12DM45 LMU12DME45 LMU12DMB45	
68-pin Pin Grid Array — G2	LMU12GM75 LMU12GME75 LMU12GMB75	LMU12GM55 LMU12GME55 LMU12GMB55	LMU12GM45 LMU12GME45 LMU12GMB45	

Pin Assignments

Pin		Function	Pin		Function
P,D	G		P,D	G	
1	F02	A7	35	G10	R18
2	F01	A6	36	G11	R19
3	E02	A5	37	H10	R20
4	E01	A4	38	H11	R21
5	D02	A3	39	J10	R22
6	D01	A2	40	J11	R23
7	C02	A1	41	K10	TCB
8	C01	A0	42	L10	B11
9	B02	R0	43	K09	B10
10	A02	R1	44	L09	B9
11	B03	R2	45	K08	B8
12	A03	R3	46	L08	B7
13	B04	R4	47	K07	B6
14	A04	R5	48	L07	VCC
15	B05	R6	49	K06	VCC
16	A05	R7	50	L06	VCC
17	B06	R8	51	K05	B5
18	A06	R9	52	L05	B4
19	B07	R10	53	K04	B3
20	A07	R11	54	L04	B2
21	B08	$\overline{OEL}$	55	K03	B1
22	A08	$\overline{OEM}$	56	L03	B0
23	B09	GND	57	K02	TCA
24	A09	GND	58	K01	RND
25	B10	FT	59	J02	CLK B
26	B11	RS	60	J01	CLK A
27	C10	CLK L	61	H02	A11
28	C11	CLK M	62	H01	A10
29	D10	R12	63	G02	A9
30	D11	R13	64	G01	A8
31	E10	R14		A10	*NC*
32	E11	R15		K11	*NC*
33	F10	R16		L02	*NC*
34	F11	R17		B01	*NC*

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LOGIC DEVICES INCORPORATED

12 x 12-bit Parallel Multiplier LMU112

Features

- 50 ns worst-case multiply time
- Low-power CMOS technology
- Replaces TRW MPY112K
- Two's complement or unsigned operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-lead

Description

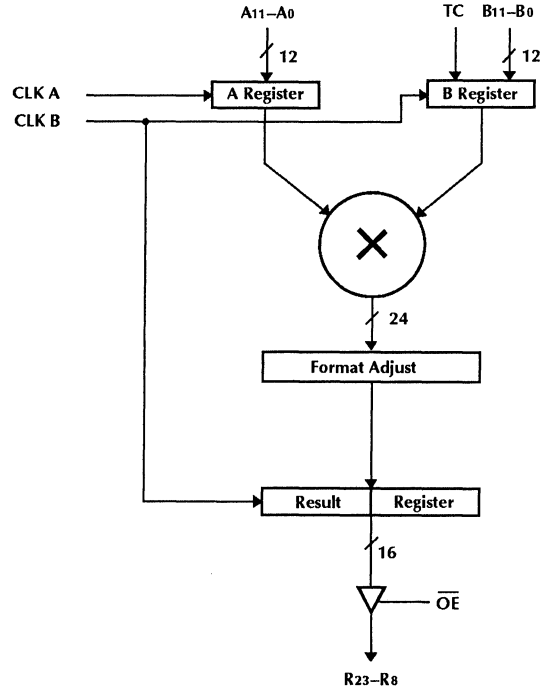
The **LMU112** is a high-speed, low power, 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with TRW's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit, TC, which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is de-asserted. Mixed mode operation is not allowed.

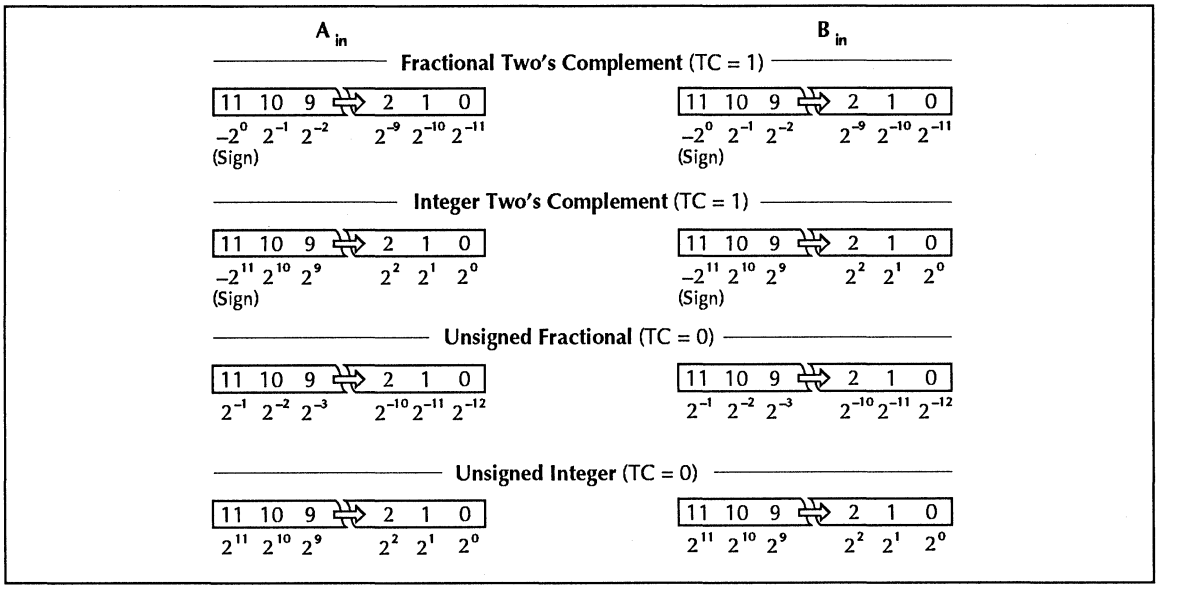
For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs (R_{23}–R_8) are in the high impedance state.

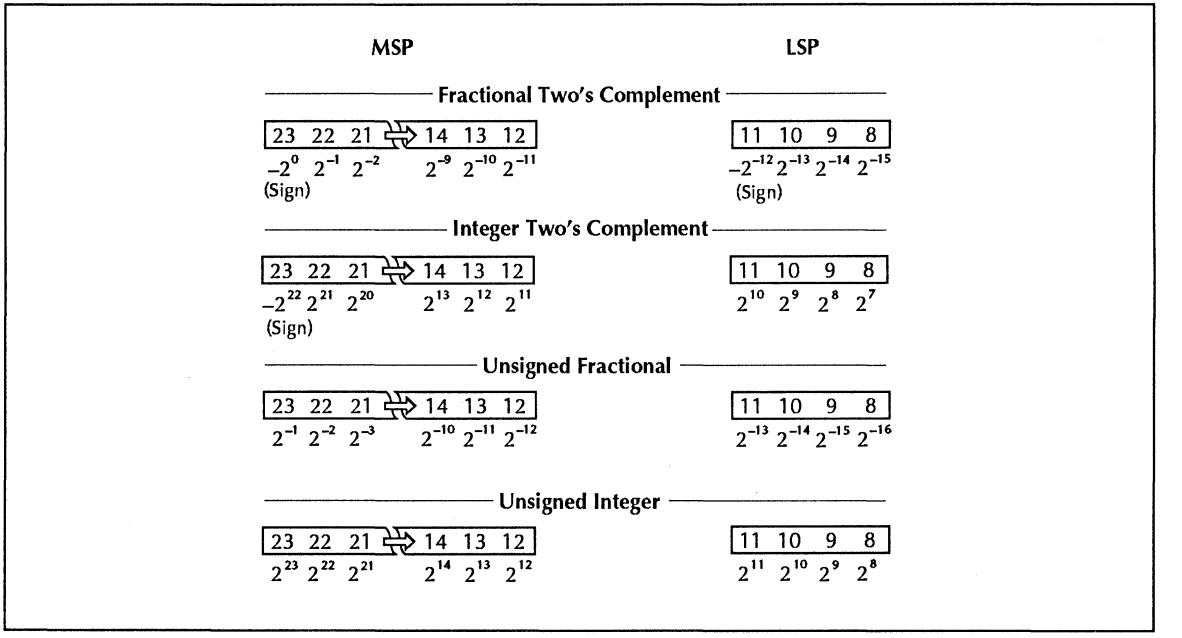
LMU112 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		10	20	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

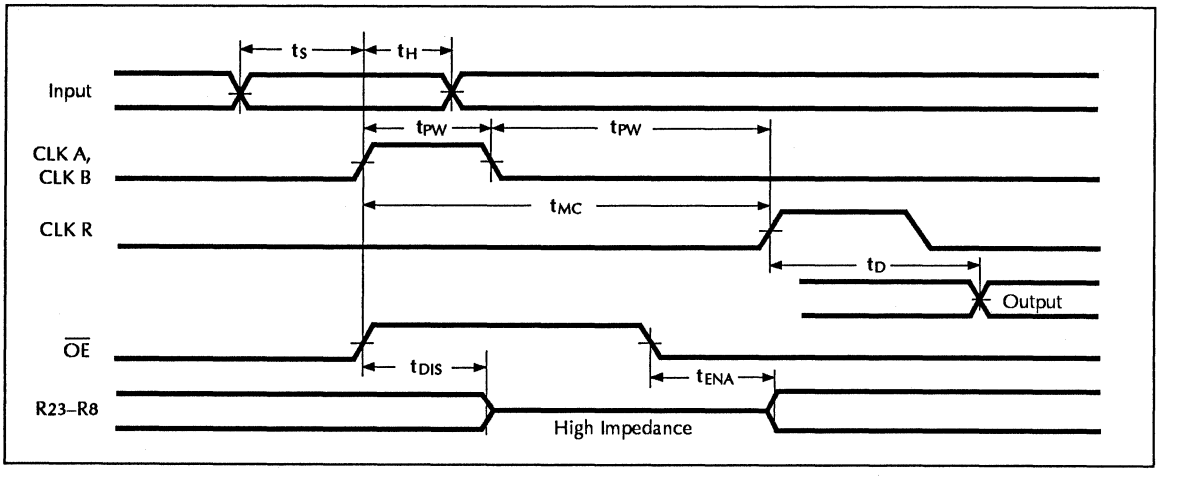
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU112-60		LMU112-50	
		Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		60		50
t_D	Output Delay		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25
t_{PW}	Clock Pulse Width	15		15	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU112-65		LMU112-55	
		Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55
t_D	Output Delay		30		30
t_{ENA}	Output Enable Time (Note 11)		30		30
t_{DIS}	Output Disable Time (Note 11)		30		30
t_{PW}	Clock Pulse Width	20		20	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance	
	60 ns	50 ns
48-pin Plastic DIP (0.6") — P5	LMU112PC60	LMU112PC50
48-pin Sidebraze (0.6") Hermetic DIP — D5	LMU112DC60	LMU112DC50
52-pin Plastic LCC, J-Lead (J5)	LMU112JC60	LMU112JC50

Military Operating Range (–55°C to +125°C)

Package Style	Performance	
	65 ns	55 ns
48-pin Sidebraze (0.6") Hermetic DIP — D5	LMU112DM65 LMU112DME65 LMU112DMB65	LMU112DM55 LMU112DME55 LMU112DMB55

Pin Assignments

P, D	J	Function	P, D	J	Function
1	1	A10	27	29	R16
2	2	A11	28	30	R15
3	3	B0	29	31	R14
4	4	B1	30	32	R13
5	5	B2	31	34	R12
6	6	B3	32	35	R11
7	8	B4	33	36	R10
8	9	B5	34	37	R9
9	10	B6	35	38	R8
10	11	B7	36	39	GND
11	12	B8	37	40	GND
12	13	Vcc	38	41	CLK A
13	14	Vcc	39	42	A0
14	15	B9	40	43	A1
15	16	B10	41	44	A2
16	17	B11	42	45	A3
17	18	TC	43	47	A4
18	19	CLK B	44	48	A5
19	21	$\overline{OE}$	45	49	A6
20	22	R23	46	50	A7
21	23	R22	47	51	A8
22	24	R21	48	52	A9
23	25	R20		7	*NC*
24	26	R19		20	*NC*
25	27	R18		33	*NC*
26	28	R17		46	*NC*

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16 x 16-bit Parallel Multiplier LMU16/216

Features

- 45 ns worst-case multiply time
- Low-power CMOS technology
- Replaces TRW MPY016HJ and AMD Am29516
- Two's complement, unsigned, or mixed operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **LMU16** and **LMU216** are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with TRW MPY016HJ and AMD Am29516 devices. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded by CLK B. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

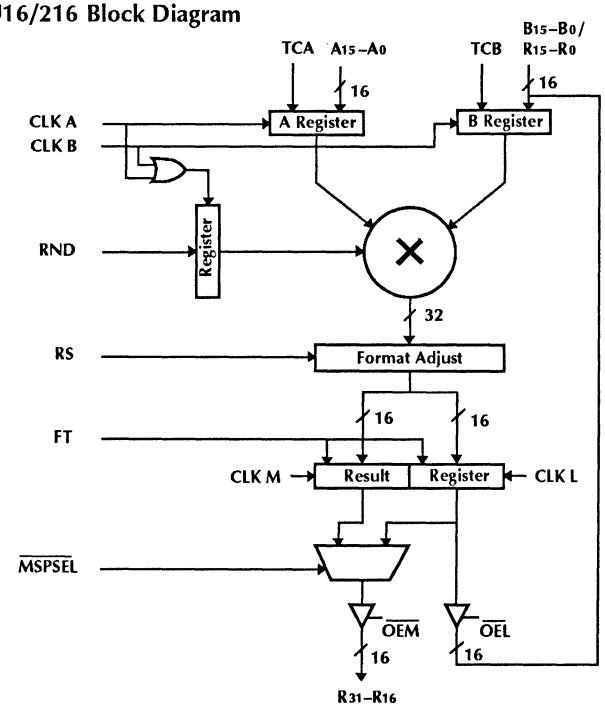
RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

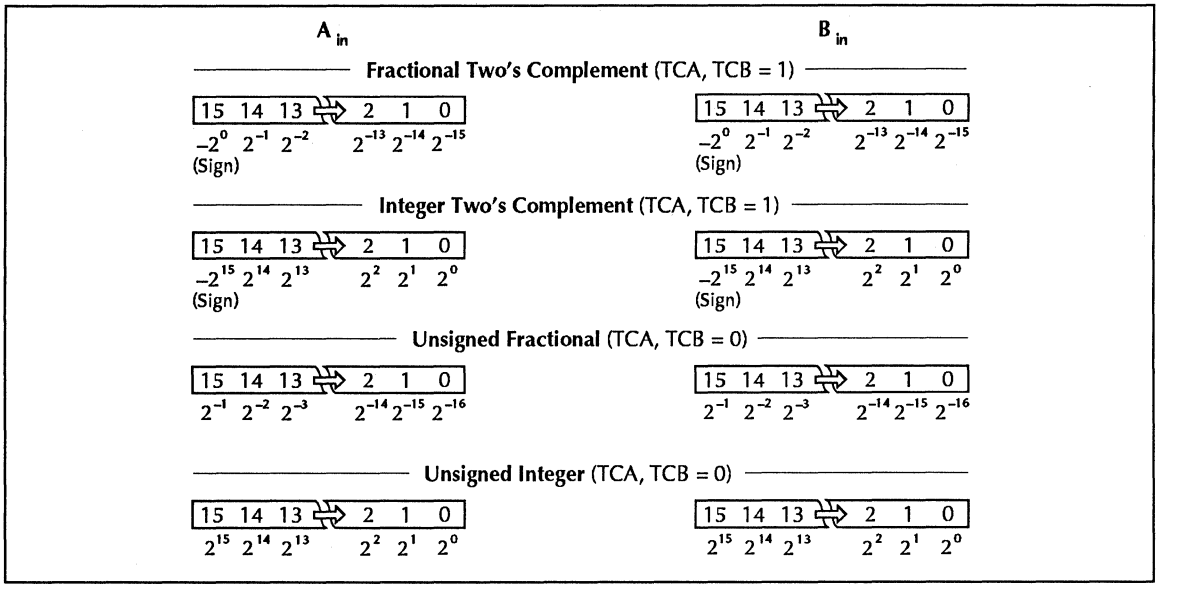
The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{\text{MSPSEL}}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{\text{MSPSEL}}$ high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

The output multiplexer control $\overline{\text{MSPSEL}}$ uses a pin which is a supply ground in the TRW MPY16HJ. When this control is LOW (GND) the function is that of the MPY16HJ, thus allowing full compatibility.

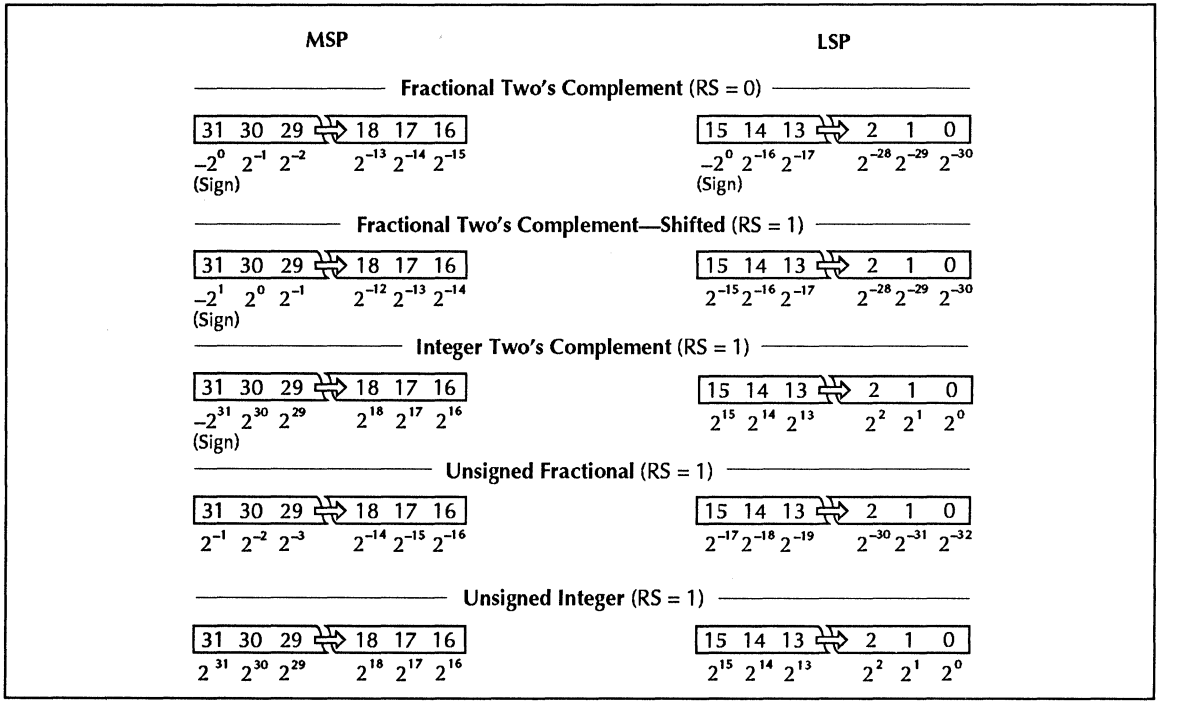
LMU16/216 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		12	25	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

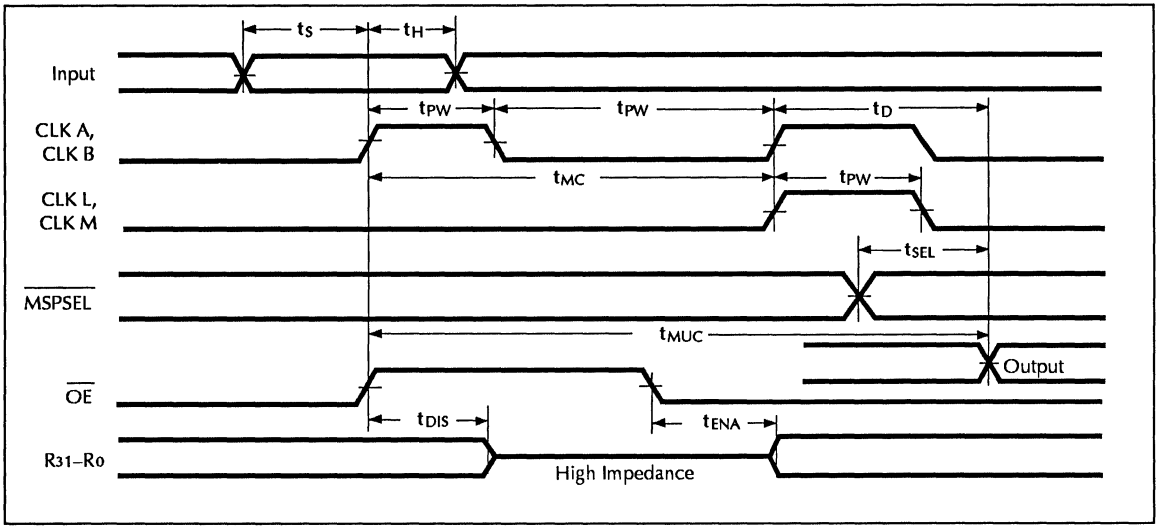
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU16/216-65		LMU16/216-55		LMU16/216-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	1		1		1	
t_S	Input Register Setup Time	15		15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU16/216-75		LMU16/216-65		LMU16/216-55	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	2		2		2	
t_S	Input Register Setup Time	15		15		15	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	55 ns	45 ns	
LMU16				
64-pin Plastic DIP (0.9") — P4	LMU16PC65	LMU16PC55	LMU16PC45	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU16DC65	LMU16DC55	LMU16DC45	
68-pin Pin Grid Array — G2	LMU16GC65	LMU16GC55	LMU16GC45	
LMU216				
68-pin Plastic LCC, J-Lead — J2	LMU216JC65	LMU216JC55	LMU216JC45	
68-pin Ceramic LCC — K3	LMU216KC65	LMU216KC55	LMU216KC45	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	75 ns	65 ns	55 ns	
LMU16				
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU16DM75 LMU16DME75 LMU16DMB75	LMU16DM65 LMU16DME65 LMU16DMB65	LMU16DM55 LMU16DME55 LMU16DMB55	
68-pin Pin Grid Array — G2	LMU16GM75 LMU16GME75 LMU16GMB75	LMU16GM65 LMU16GME65 LMU16GMB65	LMU16GM55 LMU16GME55 LMU16GMB55	
LMU216				
68-pin Ceramic LCC — K3	LMU216KM75 LMU216KME75 LMU216KMB75	LMU216KM65 LMU216KME65 LMU216KMB65	LMU216KM55 LMU216KME55 LMU216KMB55	

Pin Assignments

LMU16		216		LMU16		216	
P,D	G	J,K	Function	P,D	G	J,K	Function
1	F02	51	A4	35	G10	15	R26
2	F01	50	A3	36	G11	14	R27
3	E02	49	A2	37	H10	13	R28
4	E01	48	A1	38	H11	12	R29
5	D02	47	A0	39	J10	11	R30
6	D01	46	$\overline{OEL}$	40	J11	10	R31
7	C02	45	CLK L	41	K10	8	CLK M
8	C01	44	CLK B	42	L10	7	$\overline{OEM}$
9	B02	42	R0,B0	43	K09	6	RS
10	A02	41	R1,B1	44	L09	5	FT
11	B03	40	R2,B2	45	K08	4	$\overline{MSPSEL}$
12	A03	39	R3,B3	46	L08	3	GND
13	B04	38	R4,B4	47	K07	2	GND
14	A04	37	R5,B5	48	L07	1	Vcc
15	B05	36	R6,B6	49	K06	68	Vcc
16	A05	35	R7,B7	50	L06	67	TCB
17	B06	34	R8,B8	51	K05	66	TCA
18	A06	33	R9,B9	52	L05	65	RND
19	B07	32	R10,B10	53	K04	64	CLK A
20	A07	31	R11,B11	54	L04	63	A15
21	B08	30	R12,B12	55	K03	62	A14
22	A08	29	R13,B13	56	L03	61	A13
23	B09	28	R14,B14	57	K02	59	A12
24	A09	27	R15,B15	58	K01	58	A11
25	B10	25	R16	59	J02	57	A10
26	B11	24	R17	60	J01	56	A9
27	C10	23	R18	61	H02	55	A8
28	C11	22	R19	62	H01	54	A7
29	D10	21	R20	63	G02	53	A6
30	D11	20	R21	64	G01	52	A5
31	E10	19	R22		A10	43	*NC*
32	E11	18	R23		K11	26	*NC*
33	F10	17	R24		L02	9	*NC*
34	F11	16	R25		B01	60	*NC*

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Features

- 45 ns worst-case multiply time
- Low-power CMOS technology
- Replaces AMD Am29517
- Single clock architecture with register enables
- Two's complement, unsigned, or mixed operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **LMU17** and **LMU217** are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with AMD Am29517 devices. The LMU17 and LMU217 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

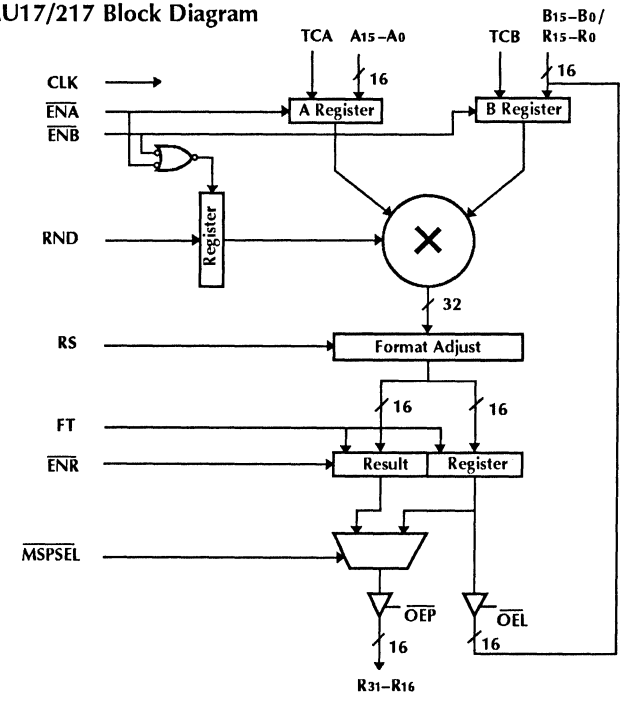
The LMU17 and LMU217 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are low. RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

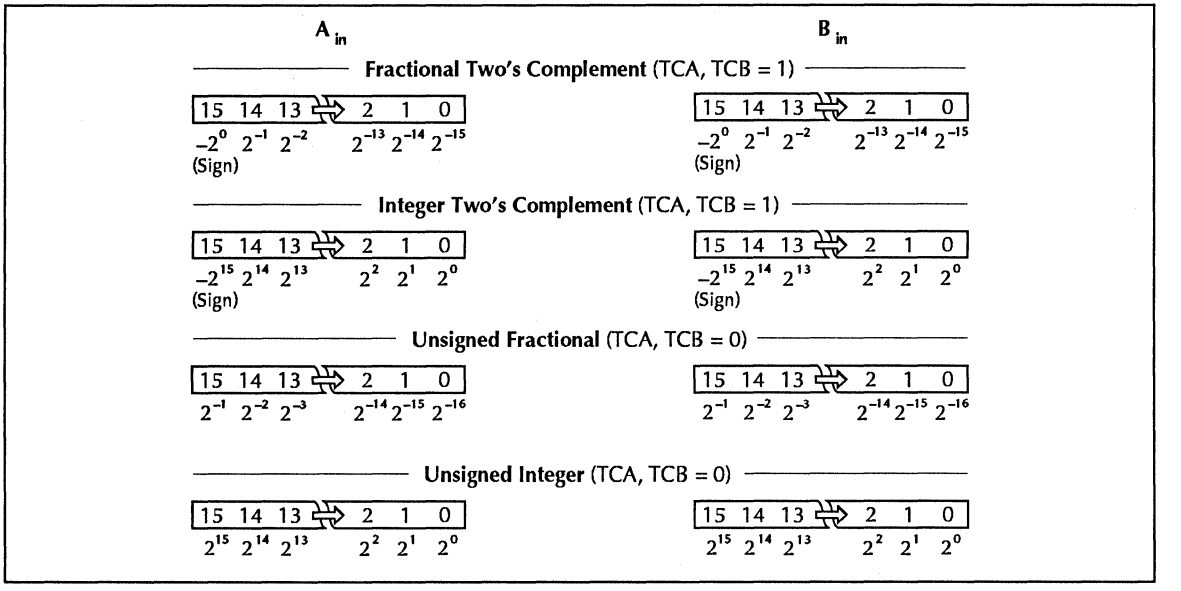
At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

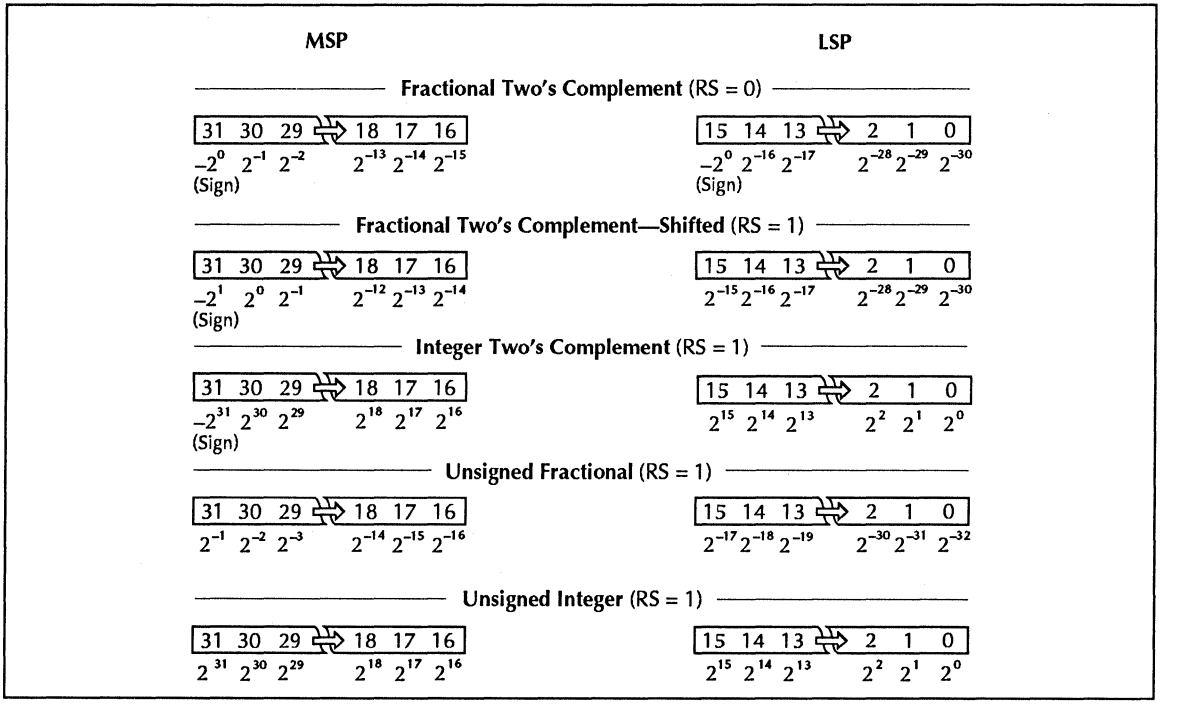
LMU17/217 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		12	25	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

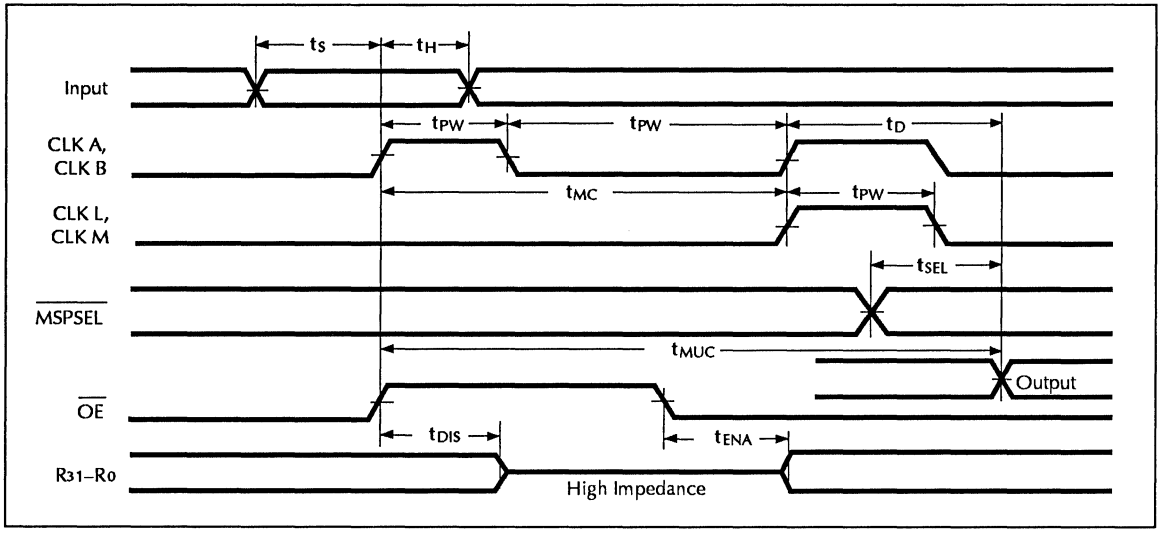
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU17/217-65		LMU17/217-55		LMU17/217-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU17/217-75		LMU17/217-65		LMU17/217-55	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	55 ns	45 ns	
LMU17				
64-pin Plastic DIP (0.9") — P4	LMU17PC65	LMU17PC55	LMU17PC45	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU17DC65	LMU17DC55	LMU17DC45	
68-pin Pin Grid Array — G2	LMU17GC65	LMU17GC55	LMU17GC45	
LMU217				
68-pin Plastic LCC, J-Lead — J2	LMU217JC65	LMU217JC55	LMU217JC45	
68-pin Ceramic LCC — K3	LMU217KC65	LMU217KC55	LMU217KC45	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	75 ns	65 ns	55 ns	
LMU17				
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMU17DM75 LMU17DME75 LMU17DMB75	LMU17DM65 LMU17DME65 LMU17DMB65	LMU17DM55 LMU17DME55 LMU17DMB55	
68-pin Pin Grid Array — G2	LMU17GM75 LMU17GME75 LMU17GMB75	LMU17GM65 LMU17GME65 LMU17GMB65	LMU17GM55 LMU17GME55 LMU17GMB55	
LMU217				
68-pin Ceramic LCC — K3	LMU217KM75 LMU217KME75 LMU217KMB75	LMU217KM65 LMU217KME65 LMU217KMB65	LMU217KM55 LMU217KME55 LMU217KMB55	

Pin Assignments

LMU17		217		LMU17		217	
P,D	G	J,K	Function	P,D	G	J,K	Function
1	F02	51	A4	35	G10	15	R26
2	F01	50	A3	36	G11	14	R27
3	E02	49	A2	37	H10	13	R28
4	E01	48	A1	38	H11	12	R29
5	D02	47	A0	39	J10	11	R30
6	D01	46	$\overline{OEL}$	40	J11	10	R31
7	C02	45	CLK	41	K10	8	$\overline{ENR}$
8	C01	44	$\overline{ENB}$	42	L10	7	$\overline{OEM}$
9	B02	42	R0,B0	43	K09	6	RS
10	A02	41	R1,B1	44	L09	5	FT
11	B03	40	R2,B2	45	K08	4	$\overline{MSPSEL}$
12	A03	39	R3,B3	46	L08	3	GND
13	B04	38	R4,B4	47	K07	2	GND
14	A04	37	R5,B5	48	L07	1	Vcc
15	B05	36	R6,B6	49	K06	68	Vcc
16	A05	35	R7,B7	50	L06	67	TCB
17	B06	34	R8,B8	51	K05	66	TCA
18	A06	33	R9,B9	52	L05	65	RND
19	B07	32	R10,B10	53	K04	64	$\overline{ENA}$
20	A07	31	R11,B11	54	L04	63	A15
21	B08	30	R12,B12	55	K03	62	A14
22	A08	29	R13,B13	56	L03	61	A13
23	B09	28	R14,B14	57	K02	59	A12
24	A09	27	R15,B15	58	K01	58	A11
25	B10	25	R16	59	J02	57	A10
26	B11	24	R17	60	J01	56	A9
27	C10	23	R18	61	H02	55	A8
28	C11	22	R19	62	H01	54	A7
29	D10	21	R20	63	G02	53	A6
30	D11	20	R21	64	G01	52	A5
31	E10	19	R22		A10	43	*NC*
32	E11	18	R23		K11	26	*NC*
33	F10	17	R24		L02	9	*NC*
34	F11	16	R25		B01	60	*NC*

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16 x 16-bit Parallel Multiplier — LMU18

Features

- 35 ns worst-case multiply time
- Low-power CMOS technology
- Full 32-bit output port — no multiplexing required
- Two's complement, unsigned, or mixed operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Pin Grid Array

Description

The **LMU18** is a 16-bit parallel multiplier featuring high speed and low power consumption. The LMU18 is an 84-pin device which provides simultaneous access to all outputs. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

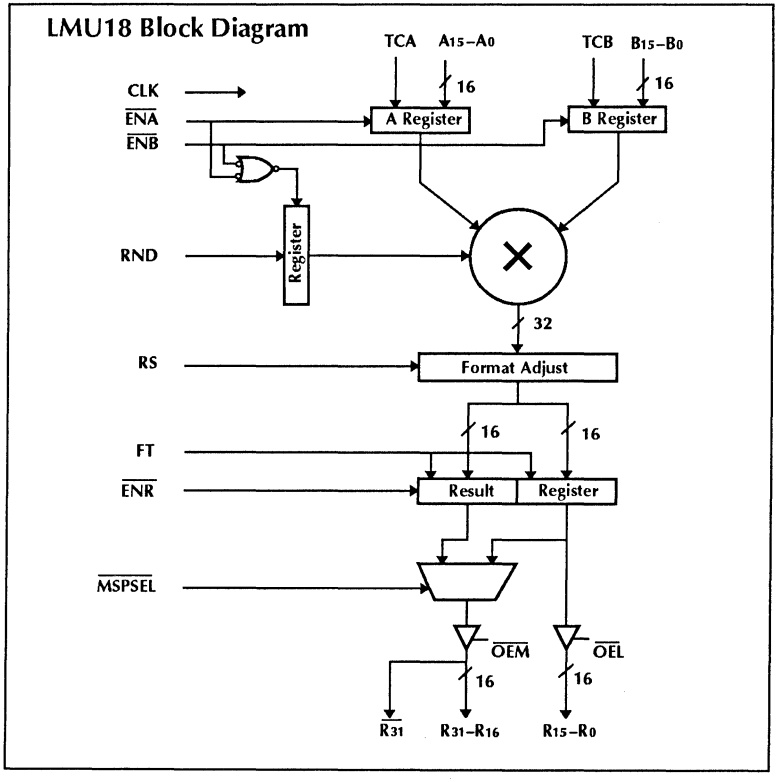
The LMU18 produces the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are low. RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

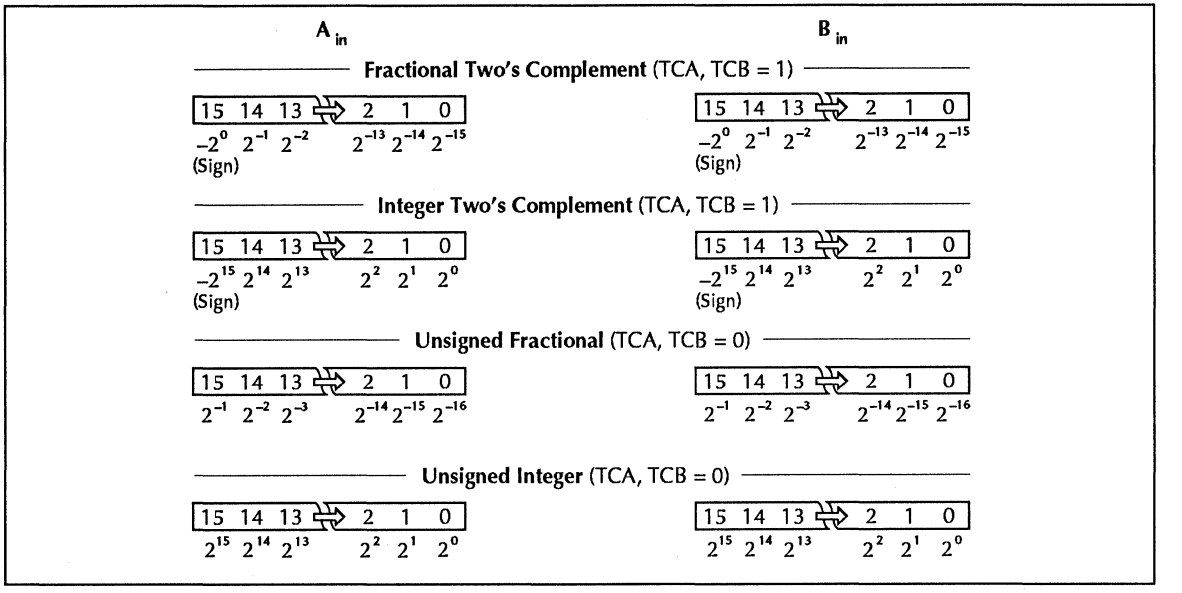
At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ high routes the least significant half of the result to the MSP pins. The MSB of the result is available in both true and complemented form to aid implementation of higher precision multipliers.

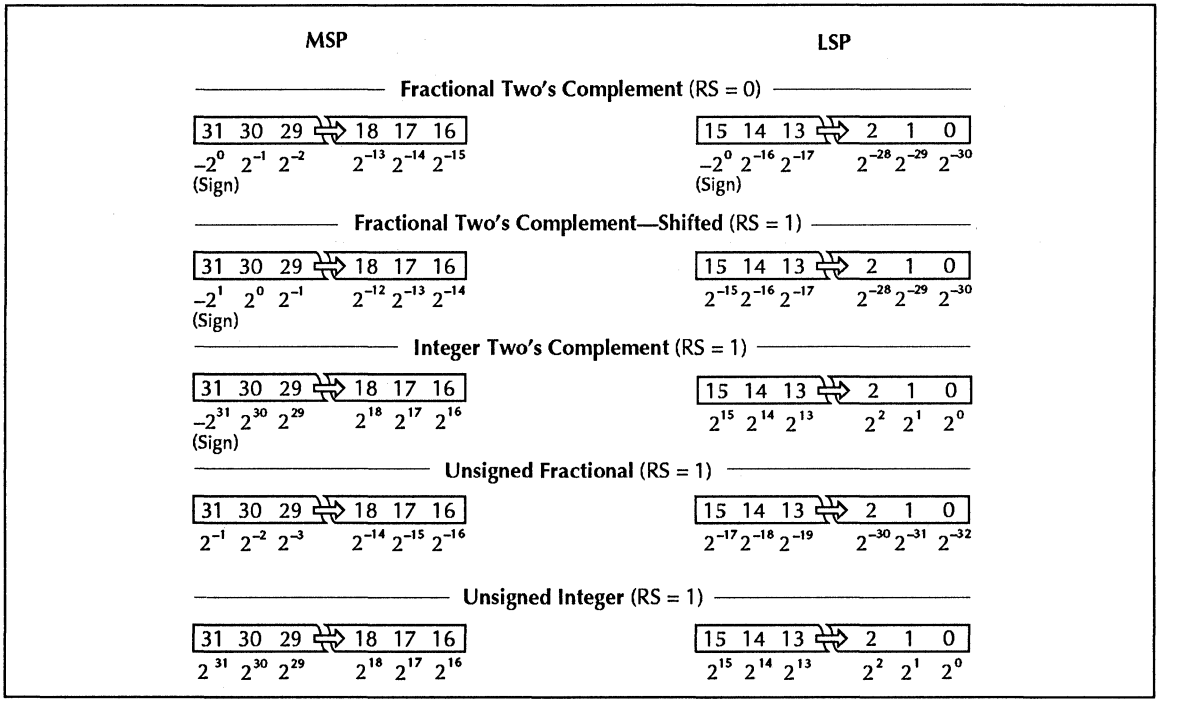
LMU18 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		25	45	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

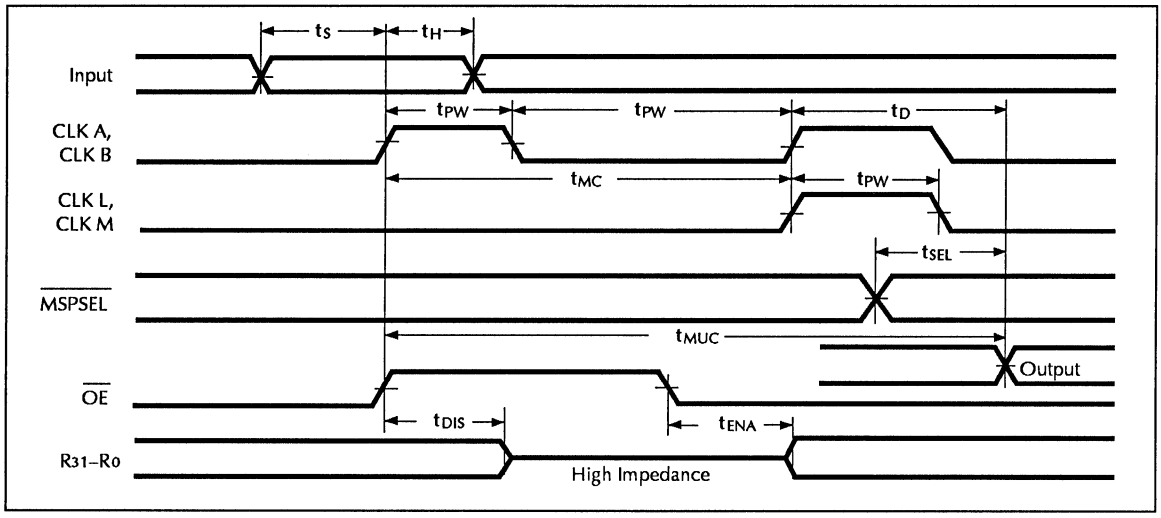
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU18-65		LMU18-45		LMU18-35	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		45		35
t_{MUC}	Unclocked Multiply Time		85		65		55
t_D	Output Delay		30		30		25
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		20		20
t_{DIS}	Output Disable Time (Note 11)		24		20		20
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	5		5		5	
t_S	Input Register Setup Time	15		15		12	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU18-75		LMU18-55		LMU18-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_{MUC}	Unclocked Multiply Time		95		85		65
t_D	Output Delay		35		35		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		20		20
t_{DIS}	Output Disable Time (Note 11)		24		20		20
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	5		5		5	
t_S	Input Register Setup Time	15		15		12	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	45ns	35 ns	
84-pin Plastic LCC, J-Lead — J3	LMU18JC65	LMU18JC45	LMU18JC35	
84-pin Pin Grid Array — G3	LMU18GC65	LMU18GC45	LMU18GC35	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	75 ns	55 ns	45 ns	
84-pin Pin Grid Array — G3	LMU18GM75 LMU18GME75 LMU18GMB75	LMU18GM55 LMU18GME55 LMU18GMB55	LMU18GM45 LMU18GME45 LMU18GMB45	

Pin Assignments

Pin		Function	Pin		Function
J	G		J	G	
1	F03	A_0	43	F09	R_{18}
2	E03	B_0	44	F11	R_{19}
3	E01	B_1	45	G11	R_{20}
4	E02	B_2	46	G10	R_{21}
5	F01	B_3	47	G09	R_{22}
6	D01	B_4	48	H11	R_{23}
7	D02	B_5	49	H10	R_{24}
8	C01	B_6	50	J11	R_{25}
9	B01	B_7	51	K11	R_{26}
10	C02	B_8	52	J10	R_{27}
11	A01	B_9	53	L11	R_{28}
12	B02	B_{10}	54	K10	R_{29}
13	B03	B_{11}	55	K09	R_{30}
14	A02	B_{12}	56	L10	R_{31}
15	A03	B_{13}	57	L09	$\overline{R_{31}}$
16	B04	B_{14}	58	K08	$\overline{ENR}$
17	A04	B_{15}	59	L08	$\overline{OEM}$
18	B06	$\overline{ENB}$	60	J07	RS
19	B05	CLK	61	K07	FT
20	A05	$\overline{OEL}$	62	L07	$\overline{MSPSEL}$
21	C05	GND	63	K06	GND
22	C06	V_{CC}	64	J06	GND
23	A06	R_0	65	J05	V_{CC}
24	A07	R_1	66	L05	TCB
25	B07	R_2	67	K05	TCA
26	C07	R_3	68	L06	RND
27	A08	R_4	69	L04	$\overline{ENA}$
28	B08	R_5	70	K04	A_{15}
29	A09	R_6	71	L03	A_{14}
30	A10	R_7	72	L02	A_{13}
31	B09	R_8	73	K03	A_{12}
32	A11	R_9	74	L01	A_{11}
33	B10	R_{10}	75	K02	A_{10}
34	C10	R_{11}	76	J02	A_9
35	B11	R_{12}	77	K01	A_8
36	C11	R_{13}	78	J01	A_7
37	D10	R_{14}	79	H02	A_6
38	D11	R_{15}	80	H01	A_5
39	F10	V_{CC}	81	G03	A_4
40	E10	GND	82	G02	A_3
41	E11	R_{16}	83	G01	A_2
42	E09	R_{17}	84	F02	A_1

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Features

- 45 ns worst-case multiply-accumulate time
- Low-power CMOS technology
- Replaces TRW TDC1009
- Two's complement, unsigned, or mixed operands
- Accumulator performs load, accumulate, subtract
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **LMA1009** and **LMA2009** are 12-bit CMOS multiplier-accumulators. They are pin for pin equivalent to the TRW TDC1009 bipolar multiplier-accumulator. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1009 and LMA2009 produce the 24-bit product of two 12-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 27-bit precision with the multiplier product sign extended as appropriate.

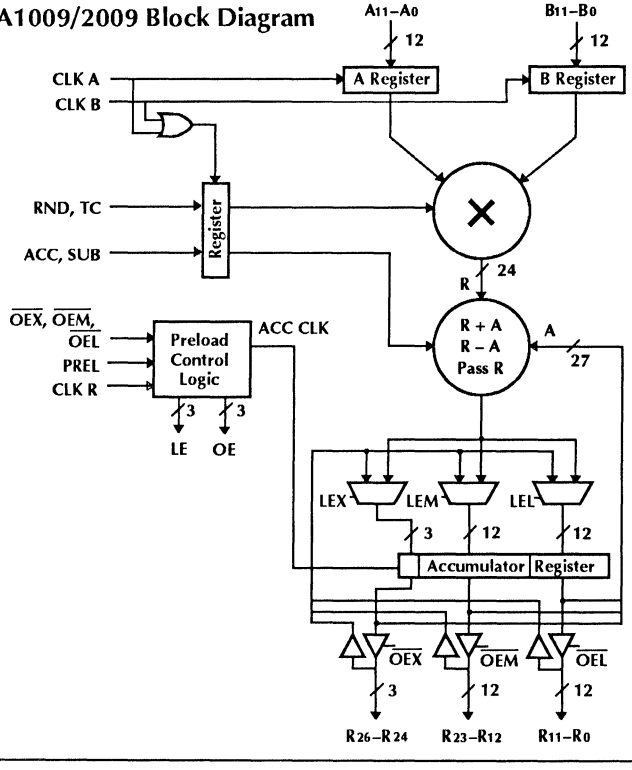
Data present at the A and B input registers (12-bits) is latched in on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the input as two's complement (TC high) or as unsigned magnitude (TC low). RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

The LMA1009 and LMA2009 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 12 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in the preload truth table.

LMA1009/2009 Block Diagram

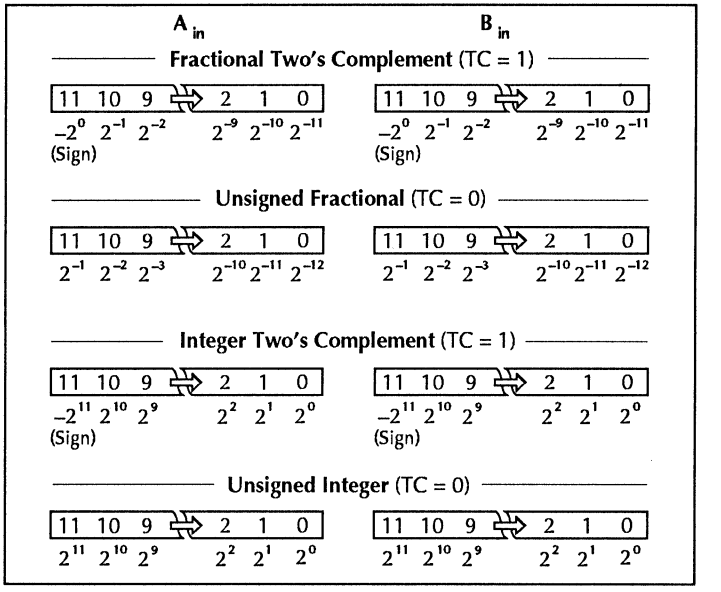


Preload Truth Table

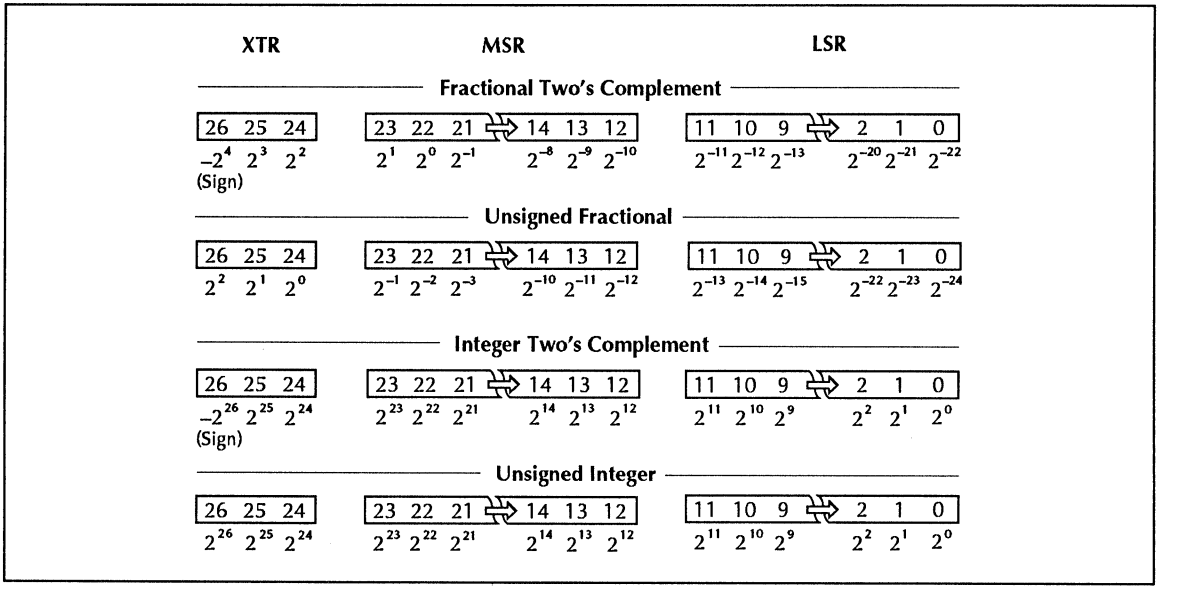
PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

OUT = Register available on output pins
Z = High impedance state
PREL = Data can be preloaded to appropriate register

Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
Vcc supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			−250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		12	25	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

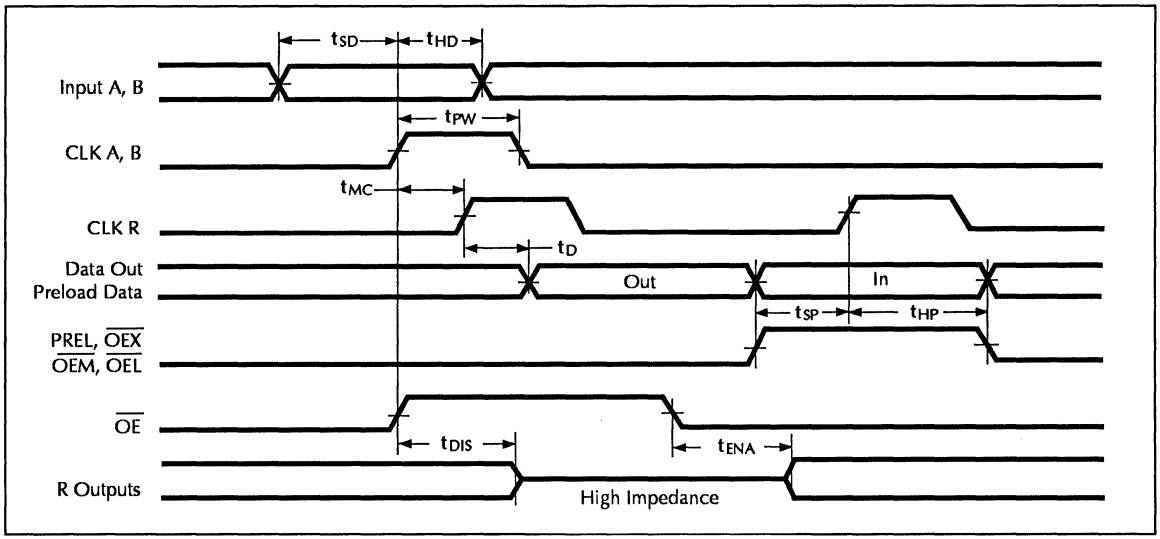
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMA1009/2009-75		LMA1009/2009-55		LMA1009/2009-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_D	Output Delay		30		25		25
t_{ENA}	Output Enable Time (Note 11)		30		30		25
t_{DIS}	Output Disable Time		25		25		25
t_{HD}	Input Register Hold Time	2		2		2	
t_{HP}	Preload Hold Time	2		2		2	
t_{SD}	Input Register Setup Time	15		15		12	
t_{SP}	Preload Setup Time	15		15		12	
t_{PW}	Clock Pulse Width	15		15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMA1009/2009-95		LMA1009/2009-65		LMA1009/2009-55	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		95		65		55
t_D	Output Delay		35		30		25
t_{ENA}	Output Enable Time (Note 11)		35		35		30
t_{DIS}	Output Disable Time		30		30		30
t_{HD}	Input Register Hold Time	2		2		2	
t_{HP}	Preload Hold Time	2		2		2	
t_{SD}	Input Register Setup Time	20		20		15	
t_{SP}	Preload Setup Time	20		20		15	
t_{PW}	Clock Pulse Width	20		20		15	

Switching Waveforms



3

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	75 ns	55 ns	45 ns	
LMA1009				
64-pin Plastic DIP (0.9") — P4	LMA1009PC75	LMA1009PC55	LMA1009PC45	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMA1009DC75	LMA1009DC55	LMA1009DC45	
68-pin Pin Grid Array — G2	LMA1009GC75	LMA1009GC55	LMA1009GC45	
LMA2009				
68-pin Plastic LCC, J-Lead — J2	LMA2009JC75	LMA2009JC55	LMA2009JC45	
68-pin Ceramic LCC — K3	LMA2009KC75	LMA2009KC55	LMA2009KC45	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	95 ns	65 ns	55 ns	
LMA1009				
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMA1009DM95 LMA1009DME95 LMA1009DMB95	LMA1009DM65 LMA1009DME65 LMA1009DMB65	LMA1009DM55 LMA1009DME55 LMA1009DMB55	
68-pin Pin Grid Array — G2	LMA1009GM95 LMA1009GME95 LMA1009GMB95	LMA1009GM65 LMA1009GME65 LMA1009GMB65	LMA1009GM55 LMA1009GME55 LMA1009GMB55	
LMA2009				
68-pin Ceramic LCC — K3	LMA2009KM95 LMA2009KME95 LMA2009KMB95	LMA2009KM65 LMA2009KME65 LMA2009KMB65	LMA2009KM55 LMA2009KME55 LMA2009KMB55	

Pin Assignments

LMA1009		2009		LMA1009		2009	
P,D	G	J,K	Function	P,D	G	J,K	Function
1	F02	52	A4	35	G10	16	R21
2	F01	51	A3	36	G11	15	R22
3	E02	50	A2	37	H10	14	R23
4	E01	49	A1	38	H11	13	R24
5	D02	48	A0	39	J10	12	R25
6	D01	47	ACC	40	J11	11	R26
7	C02	46	SUB	41	K10	10	$\overline{OEX}$
8	C01	45	RND	42	L10	9	TC
9	B02	44	$\overline{OEL}$	43	K09	8	B11
10	A02	43	R0	44	L09	7	B10
11	B03	42	R1	45	K08	6	B9
12	A03	41	R2	46	L08	5	B8
13	B04	40	R3	47	K07	4	B7
14	A04	39	R4	48	L07	3	B6
15	B05	38	R5	49	K06	2,68	VCC
16	A05	37,36	GND	50	L06	67	B5
17	B06	35	R6	51	K05	66	B4
18	A06	33	R7	52	L05	65	B3
19	B07	32	R8	53	K04	64	B2
20	A07	31	R9	54	L04	63	B1
21	B08	30	R10	55	K03	62	B0
22	A08	29	R11	56	L03	61	CLK B
23	B09	28	CLK R	57	K02	60	CLK A
24	A09	27	PREL	58	K01	59	A11
25	B10	26	$\overline{OEM}$	59	J02	58	A10
26	B11	25	R12	60	J01	57	A9
27	C10	24	R13	61	H02	56	A8
28	C11	23	R14	62	H01	55	A7
29	D10	22	R15	63	G02	54	A6
30	D11	21	R16	64	G01	53	A5
31	E10	20	R17		A10	1	*NC*
32	E11	19	R18		K11	34	*NC*
33	F10	18	R19		L02		*NC*
34	F11	17	R20		B01		*NC*

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Features

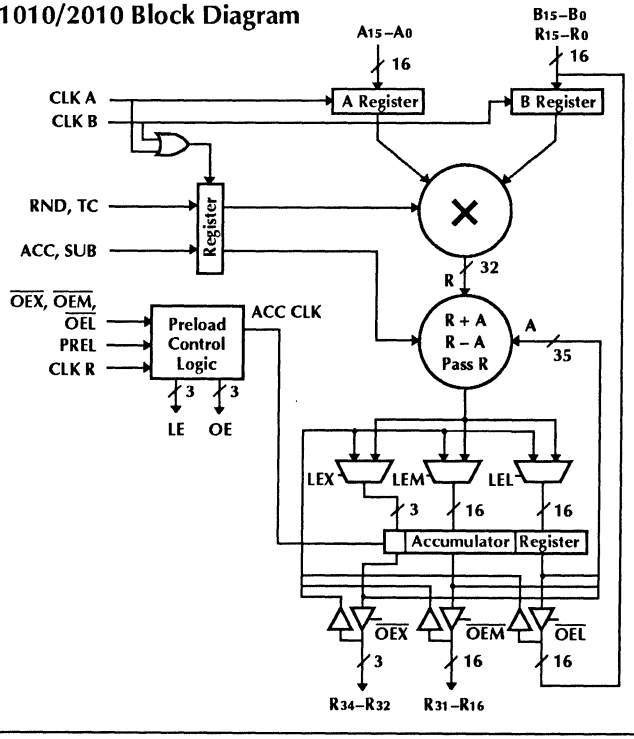
- 45 ns worst-case multiply-accumulate time
- Low-power CMOS technology
- Replaces TRW TDC1010 and AMD Am29510
- Two's complement, unsigned, or mixed operands
- Accumulator performs load, accumulate, subtract
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, HermeticDIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **LMA1010** and **LMA2010** are high speed, low power multiplier-accumulators (MACs). They are pin for pin equivalent to the TRW TDC1010 and the AMD AM29510 bipolar multiplier accumulators. The LMA1010 and LMA2010 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is achieved with advanced CMOS technology.

The LMA1010 produces the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

LMA1010/2010 Block Diagram



Data present at the A and B inputs is loaded into the input registers on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are loaded on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the input as two's complement (TC high) or unsigned magnitude (TC low). RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

The LMA1010 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is 3 bits long. The LSR output pins are multiplexed with the B input pins.

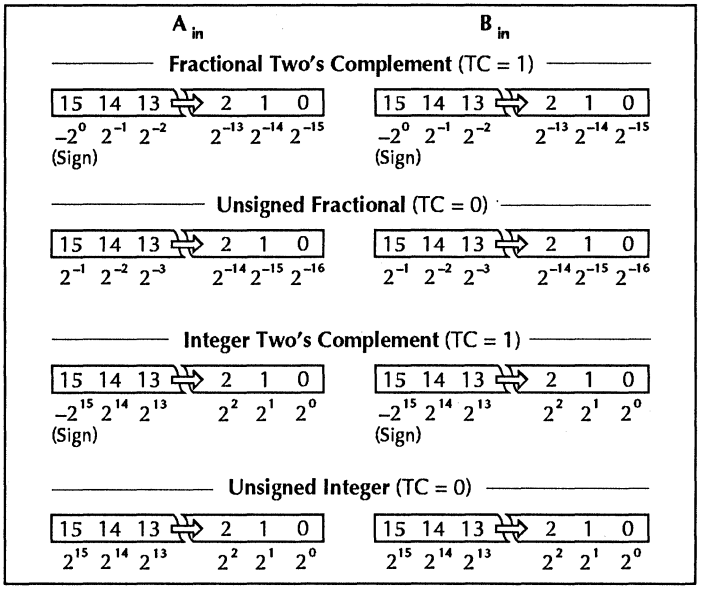
Each output register has an independent output enable control. In addition to providing three-state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of PREL and enable controls is summarized in the preload truth table.

Preload Truth Table

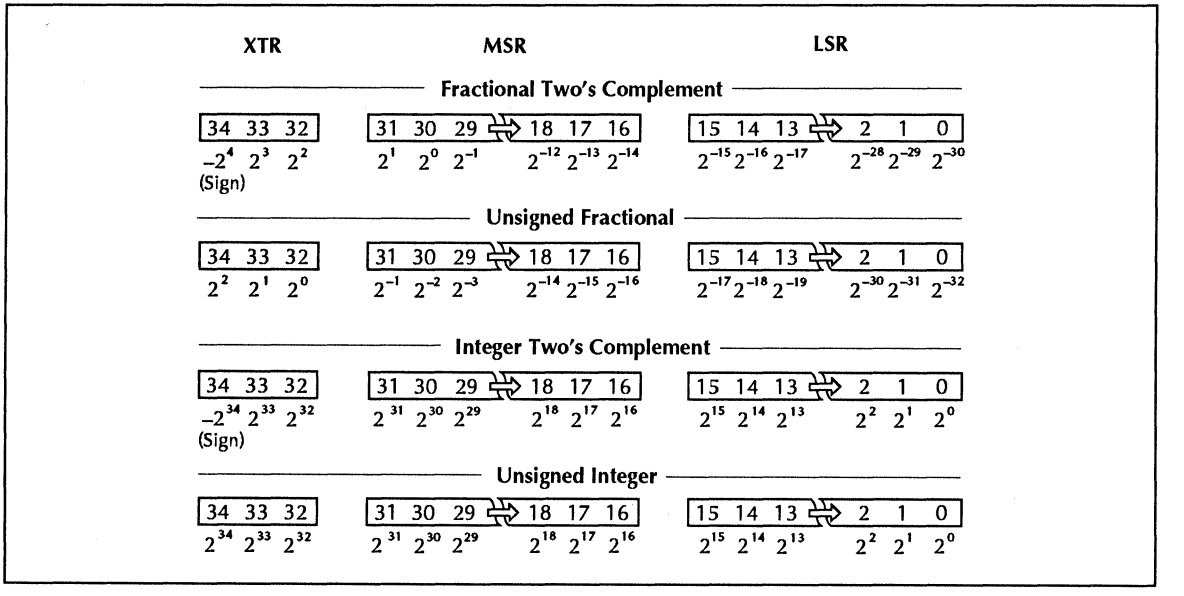
PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

OUT = Register available on output pins
Z = High impedance state
PREL = Data can be preloaded to appropriate register

Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

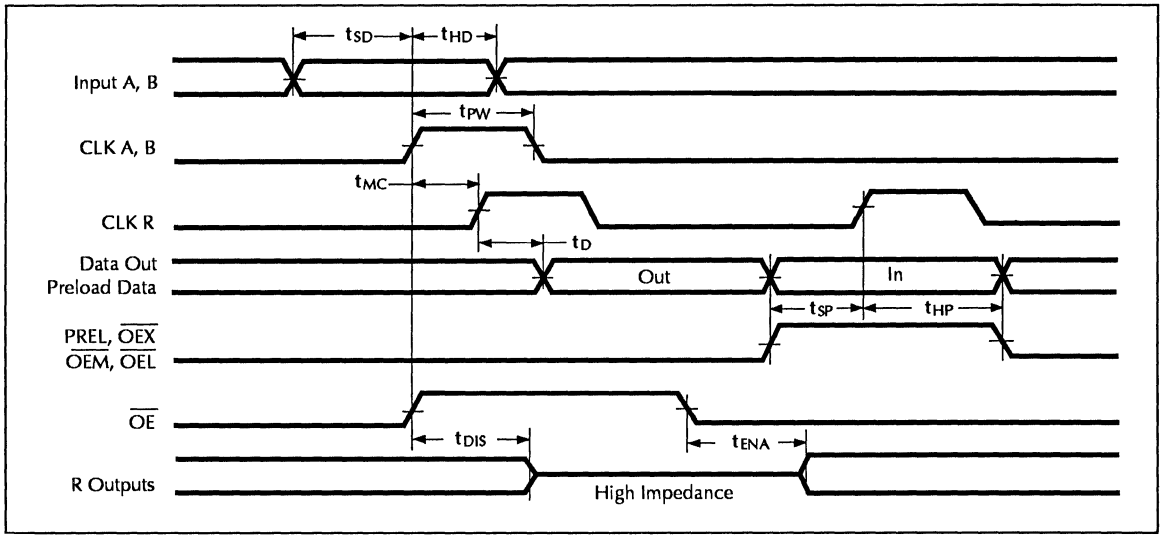
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMA1010/2010-65		LMA1010/2010-55		LMA1010/2010-45	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_D	Output Delay		30		25		25
t_{ENA}	Output Enable Time (Note 11)		30		30		30
t_{DIS}	Output Disable Time (Note 11)		30		25		25
t_{HD}	Input Register Hold Time	0		0		0	
t_{HP}	Preload Hold Time	0		0		0	
t_{SD}	Input Register Setup Time	15		15		12	
t_{SP}	Preload Setup Time	15		15		12	
t_{PW}	Clock Pulse Width	15		15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMA1010/2010-75		LMA1010/2010-65		LMA1010/2010-55	
		Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_D	Output Delay		35		30		30
t_{ENA}	Output Enable Time (Note 11)		35		30		30
t_{DIS}	Output Disable Time (Note 11)		35		25		25
t_{HD}	Input Register Hold Time	0		0		0	
t_{HP}	Preload Hold Time	0		0		0	
t_{SD}	Input Register Setup Time	20		15		12	
t_{SP}	Preload Setup Time	20		15		12	
t_{PW}	Clock Pulse Width	20		15		15	

Switching Waveforms



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Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	55 ns	45 ns	
LMA1010				
64-pin Plastic DIP (0.9") — P4	LMA1010PC65	LMA1010PC55	LMA1010PC45	
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMA1010DC65	LMA1010DC55	LMA1010DC45	
68-pin Pin Grid Array — G2	LMA1010GC65	LMA1010GC55	LMA1010GC45	
LMA2010				
68-pin Plastic LCC, J-Lead — J2	LMA2010JC65	LMA2010JC55	LMA2010JC45	
68-pin Ceramic LCC — K3	LMA2010KC65	LMA2010KC55	LMA2010KC45	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	75 ns	65 ns	55 ns	
LMA1010				
64-pin Sidebraze (0.9") Hermetic DIP — D6	LMA1010DM75 LMA1010DME75 LMA1010DMB75	LMA1010DM65 LMA1010DME65 LMA1010DMB65	LMA1010DM55 LMA1010DME55 LMA1010DMB55	
68-pin Pin Grid Array — G2	LMA1010GM75 LMA1010GME75 LMA1010GMB75	LMA1010GM65 LMA1010GME65 LMA1010GMB65	LMA1010GM55 LMA1010GME55 LMA1010GMB55	
LMA2010				
68-pin Ceramic LCC — K3	LMA2010KM75 LMA2010KME75 LMA2010KMB75	LMA2010KM65 LMA2010KME65 LMA2010KMB65	LMA2010KM55 LMA2010KME55 LMA2010KMB55	

3

Pin Assignments

LMA1010	2010			LMA1010	2010	
P,D	G	J,K	Function	P,D	G	J,K	Function
1	F02	1	A6	35	G10	34	R26
2	F01	68	A5	36	G11	33	R27
3	E02	67	A4	37	H10	32	R28
4	E01	66	A3	38	H11	31	R29
5	D02	65	A2	39	J10	30	R30
6	D01	64	A1	40	J11	29	R31
7	C02	63	A0	41	K10	28	R32
8	C01	62	R0,B0	42	L10	27	R33
9	B02	61	R1,B1	43	K09	26	R34
10	A02	60	R2,B2	44	L09	25	CLK R
11	B03	59	R3,B3	45	K08	24	$\overline{OEM}$
12	A03	58	R4,B4	46	L08	23	PREL
13	B04	57	R5,B5	47	K07	22	$\overline{OEX}$
14	A04	56	R6,B6	48	L07	21	TC
15	B05	55	R7,B7	49	K06	20,19,18,17	Vcc
16	A05	54,53	GND	50	L06	16	CLK B
17	B06	52	R8,B8	51	K05	15	CLK A
18	A06	51	R9,B9	52	L05	14	ACC
19	B07	50	R10,B10	53	K04	13	SUB
20	A07	49	R11,B11	54	L04	12	RND
21	B08	48	R12,B12	55	K03	11	$\overline{OEL}$
22	A08	47	R13,B13	56	L03	10	A15
23	B09	46	R14,B14	57	K02	9	A14
24	A09	45	R15,B15	58	K01	8	A13
25	B10	44	R16	59	J02	7	A12
26	B11	43	R17	60	J01	6	A11
27	C10	42	R18	61	H02	5	A10
28	C11	41	R19	62	H01	4	A9
29	D10	40	R20	63	G02	3	A8
30	D11	39	R21	64	G01	2	A7
31	E10	38	R22		A10		*NC*
32	E11	37	R23		K11		*NC*
33	F10	36	R24		L02		*NC*
34	F11	35	R25		B01		*NC*

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LOGIC DEVICES INCORPORATED

Features

- 12 × 12-bit multiplier with pipelined 26-bit output summer
- Summer has 26-bit input port fully independent from multiplier inputs
- Cascadable to form video rate FIR filter with 3-bit headroom
- A, B, and C input registers separately enabled for maximum flexibility
- 25 MHz data rate for FIR filtering applications
- High speed, low power CMOS technology
- Package styles available:
  - 84-pin Plastic LCC J-Lead
  - 84-pin Grid Array

Description

The **LMS12** is a high speed 12 × 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

Architecture

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

Multiplier

The A11–A0 and B11–B0 inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input register, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 × 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in 2's complement format. The multiplication result forms the input to the 24-bit product register.

Summer

The C25–C0 inputs to the LMS12 form a 26-bit 2's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the (sign extended) contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

Output Multiplexer

The FTS input controls a multiplexer which selects the data to be output on the S25–S0 lines. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, the multiplexer selects the S register for output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 Block Diagram

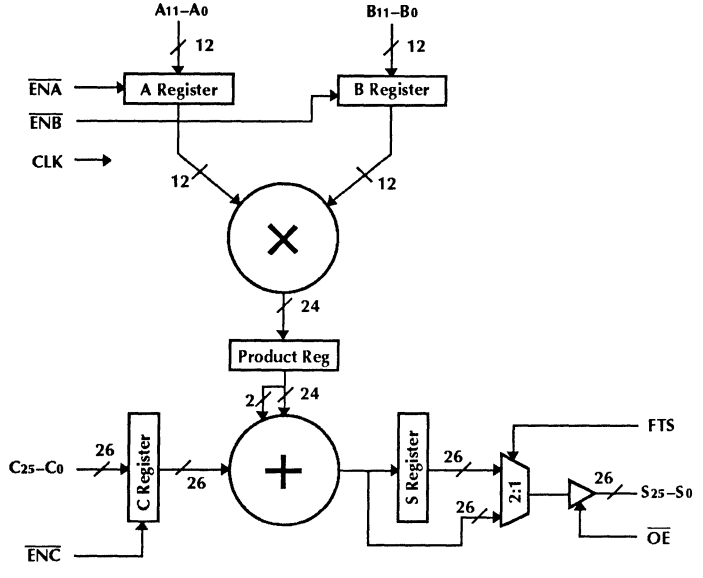
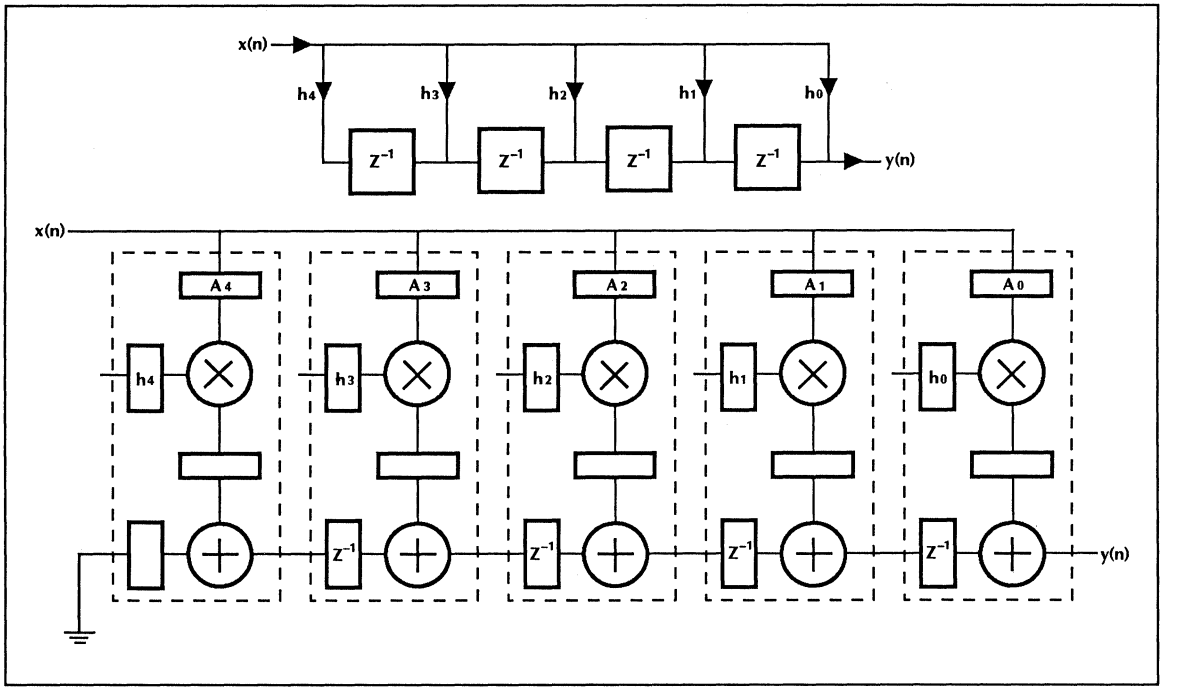


Figure 2. Flow diagram for 5-tap FIR filter.



Applications

The LMS12 is designed specifically for high speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Fig. 2.

The operation of the 5-tap FIR filter implementation of Fig. 2 is depicted in Table 1. The filter weights h_4–h_0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A-register contents and Sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S_0 is produced by the rightmost device, which has h_0 as its filter weight and A_0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

Table 1. Timing example for 5-tap nondecimating FIR filter.

CLK Cycle	1	2	3	4	5	6	7	8	9
X(n)	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A3 Register Sum 3		X_n	X_{n+1} h_3X_n $+ h_4X_{n-1}$	X_{n+2} h_3X_{n+1} $+ h_4X_n$	X_{n+3} h_3X_{n+2} $+ h_4X_{n+1}$	X_{n+4} h_3X_{n+3} $+ h_4X_{n+2}$	X_{n+5} h_3X_{n+4} $+ h_4X_{n+3}$	X_{n+6} h_3X_{n+5} $+ h_4X_{n+4}$	X_{n+7} h_3X_{n+6} $+ h_4X_{n+5}$
A2 Register Sum 2		X_n	X_{n+1} h_2X_n $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+2} h_2X_{n+1} $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+3} h_2X_{n+2} $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+4} h_2X_{n+3} $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+5} h_2X_{n+4} $+ h_3X_{n+3}$ $+ h_4X_{n+2}$	X_{n+6} h_2X_{n+5} $+ h_3X_{n+4}$ $+ h_4X_{n+3}$	X_{n+7} h_2X_{n+6} $+ h_3X_{n+5}$ $+ h_4X_{n+4}$
A1 Register Sum 1		X_n	X_{n+1} h_1X_n $+ h_2X_{n-1}$ $+ h_3X_{n-2}$ $+ h_4X_{n-3}$	X_{n+2} h_1X_{n+1} $+ h_2X_n$ $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+3} h_1X_{n+2} $+ h_2X_{n+1}$ $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+4} h_1X_{n+3} $+ h_2X_{n+2}$ $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+5} h_1X_{n+4} $+ h_2X_{n+3}$ $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+6} h_1X_{n+5} $+ h_2X_{n+4}$ $+ h_3X_{n+3}$ $+ h_4X_{n+2}$	X_{n+7} h_1X_{n+6} $+ h_2X_{n+5}$ $+ h_3X_{n+4}$ $+ h_4X_{n+3}$
A0 Register Sum 0		X_n	X_{n+1} h_0X_n $+ h_1X_{n-1}$ $+ h_2X_{n-2}$ $+ h_3X_{n-3}$ $+ h_4X_{n-4}$	X_{n+2} h_0X_{n+1} $+ h_1X_n$ $+ h_2X_{n-1}$ $+ h_3X_{n-2}$ $+ h_4X_{n-3}$	X_{n+3} h_0X_{n+2} $+ h_1X_{n+1}$ $+ h_2X_n$ $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+4} h_0X_{n+3} $+ h_1X_{n+2}$ $+ h_2X_{n+1}$ $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+5} h_0X_{n+4} $+ h_1X_{n+3}$ $+ h_2X_{n+2}$ $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+6} h_0X_{n+5} $+ h_1X_{n+4}$ $+ h_2X_{n+3}$ $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+7} h_0X_{n+6} $+ h_1X_{n+5}$ $+ h_2X_{n+4}$ $+ h_3X_{n+3}$ $+ h_4X_{n+2}$

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		15	25	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

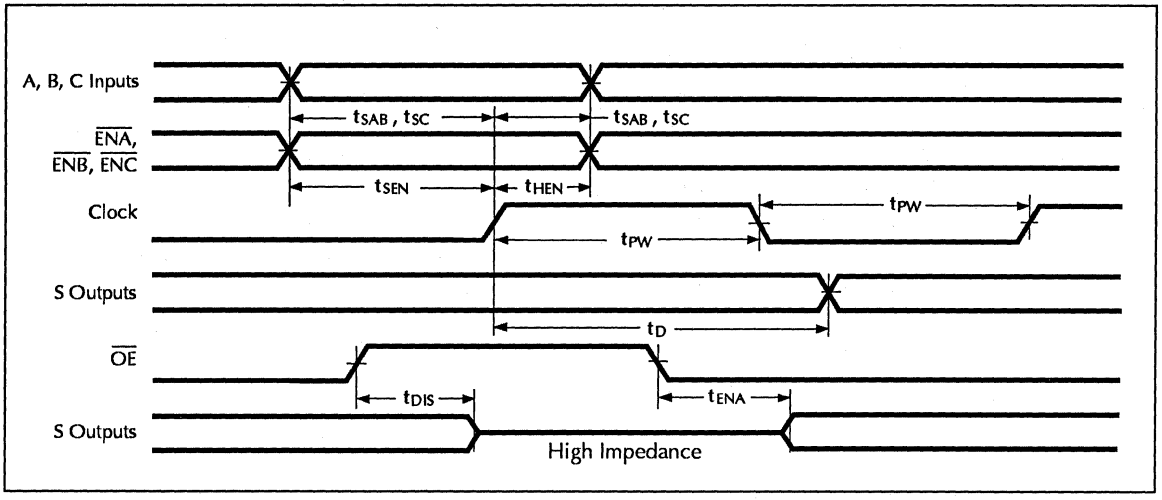
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMS12-65		LMS12-50		LMS12-40	
		Min	Max	Min	Max	Min	Max
t_{CP}	Clock Period		40		35		30
t_D	Clock to S–FT = 1		50		40		35
	Clock to S–FT = 0		25		25		25
t_{SC}	C Data Setup Time	15		10		5	
t_{SAB}	A, B Data Setup Time	15		10		10	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		10		10	
t_{HC}	C Data Hold Time	5		5		5	
t_{HAB}	A, B Data Hold Time	5		5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
t_{PW}	Clock PulseWidth	15		15		12	
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		22		22		22

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMS12-65		LMS12-50	
		Min	Max	Min	Max
t_{CP}	Clock Period		40		35
t_D	Clock to S–FT = 1		50		40
	Clock to S–FT = 0		25		25
t_{SC}	C Data Setup Time	15		10	
t_{SAB}	A, B Data Setup Time	15		10	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		10	
t_{HC}	C Data Hold Time	5		5	
t_{HAB}	A, B Data Hold Time	5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5	
t_{PW}	Clock PulseWidth	15		15	
t_{ENA}	Output Enable Time (Note 11)		25		25
t_{DIS}	Output Disable Time (Note 11)		22		22

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

3

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance			
	65 ns	50 ns	40 ns	
84-pin Plastic LCC, J-Lead — J3	LMS12JC65	LMS12JC50	LMS12JC40	
84-pin Pin Grid Array — G3	LMS12GC65	LMS12G50	LMS12GC40	

Military Operating Range (–55°C to +125°C)

Package Style	Performance			
	65 ns	50 ns		
84-pin Pin Grid Array — G3	LMS12GM65 LMS12GME65 LMS12GMB65	LMS12GM50 LMS12GME50 LMS12GMB50		

Pin Assignments

Pin		Function	Pin		Function
J,K	G		J,K	G	
1	F03	A_4	43	F09	S_9
2	E03	A_5	44	F11	S_8
3	E01	A_6	45	G11	S_7
4	E02	A_7	46	G10	S_6
5	F01	A_8	47	G09	S_5
6	D01	A_9	48	H11	S_4
7	D02	A_{10}	49	H10	S_3
8	C01	A_{11}	50	J11	S_2
9	B01	$\overline{ENA}$	51	K11	S_1
10	C02	B_0	52	J10	S_0
11	A01	B_1	53	L11	C_{25}
12	B02	B_2	54	K10	C_{24}
13	B03	B_3	55	K09	C_{23}
14	A02	B_4	56	L10	C_{22}
15	A03	CLK	57	L09	C_{21}
16	B04	B_5	58	K08	C_{20}
17	A04	B_6	59	L08	C_{19}
18	B06	B_7	60	J07	C_{18}
19	B05	B_8	61	K07	C_{17}
20	A05	B_9	62	L07	C_{16}
21	C05	B_{10}	63	K06	C_{15}
22	C06	B_{11}	64	J06	C_{14}
23	A06	$\overline{ENB}$	65	J05	C_{13}
24	A07	S_{25}	66	L05	C_{12}
25	B07	S_{24}	67	K05	C_{11}
26	C07	S_{23}	68	L06	C_{10}
27	A08	S_{22}	69	L04	C_9
28	B08	S_{21}	70	K04	C_8
29	A09	S_{20}	71	L03	C_7
30	A10	$\overline{OE}$	72	L02	C_6
31	B09	FTS	73	K03	C_5
32	A11	V_{CC}	74	L01	GND
33	B10	S_{19}	75	K02	C_4
34	C10	S_{18}	76	J02	C_3
35	B11	S_{17}	77	K01	C_2
36	C11	S_{16}	78	J01	C_1
37	D10	S_{15}	79	H02	C_0
38	D11	S_{14}	80	H01	$\overline{ENC}$
39	F10	S_{13}	81	G03	A_0
40	E10	S_{12}	82	G02	A_1
41	E11	S_{11}	83	G01	A_2
42	E09	S_{10}	84	F02	A_3

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Multilevel Pipeline Register — L29C520/521

Features

- Four 8-bit registers
- Implements double 2-stage pipeline or single 4-stage pipeline register
- Hold, Shift, Load instructions
- Separate data in and data out pins
- High-speed, low-power CMOS technology
- Three-state outputs
- Available 100% screened to MIL-STD-883, Class B
- Plug-compatible with AMD AM29520 and AM29521
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC (Type C)

Description

The Logic Devices **L29C520** and **L29C521** are pin for pin compatible with the Advanced Micro Devices AM29520 and AM29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the L29C520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The L29C521 devices differ from the L29C520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

Table 1

I_1	I_0	L29C520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

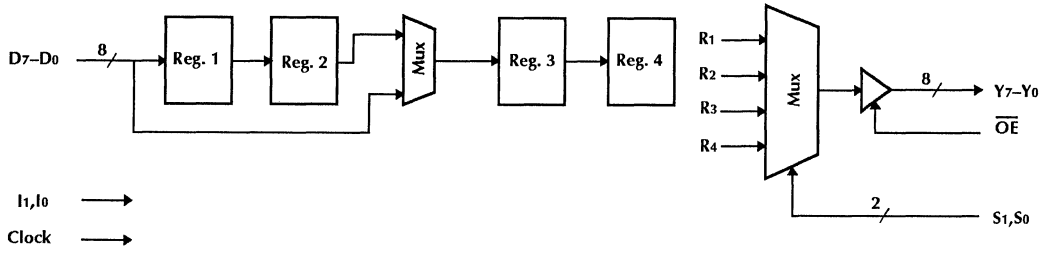
Table 2

I_1	I_0	L29C521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

Table 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

L29C520/521 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6.5 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8	–20		–100	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		10	15	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

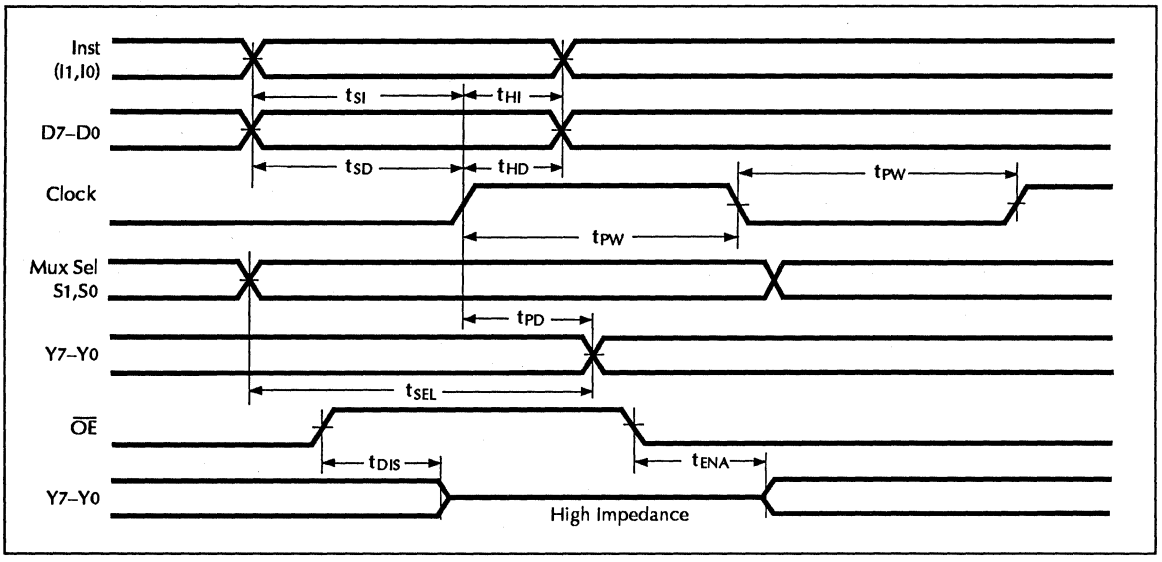
Symbol	Parameter	L29C52x-25		L29C52x-22	
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0		25		22
t_{SEL}	S_1,S_0 to Y_7–Y_1		25		20
t_{SD}	D_7–D_0 to CLK Setup	13		10	
t_{HD}	CLK to D_7–D_0 Hold	3		3	
t_{SI}	I_1,I_0 to CLK Setup	13		10	
t_{HI}	CLK to I_1,I_0 Hold	3		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21
t_{PW}	Clock Pulse Width	10		10	

3

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	L29C52x-30		L29C52x-24	
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0		30		24
t_{SEL}	S_1,S_0 to Y_7–Y_0		30		22
t_{SD}	D_7–D_0 to CLK Setup	15		10	
t_{HD}	CLK to D_7–D_0 Hold	5		3	
t_{SI}	I_1,I_0 to CLK Setup	15		10	
t_{HI}	CLK to I_1,I_0 Hold	5		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22
t_{PW}	Clock Pulse Width	15		10	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance		
	25 ns	22 ns	
L29C520			
24-pin Plastic DIP (0.3") — P2	L29C520PC25	L29C520PC22	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L29C520DC25	L29C520DC22	
24-pin CerDIP (0.3") — C1	L29C520CC25	L29C520CC22	
28-pin Plastic LCC, J-Lead — J4	L29C520JC25	L29C520JC22	
28-pin Ceramic LCC — K1	L29C520KC25	L29C520KC22	
L29C521			
24-pin Plastic DIP (0.3") — P2	L29C521PC25	L29C521PC22	
24-pin Sidebraze (0.3") Hermetic DIP — D2	L29C521DC25	L29C521DC22	
24-pin CerDIP (0.3") — C1	L29C521CC25	L29C521CC22	
28-pin Plastic LCC, J-Lead — J4	L29C521JC25	L29C521JC22	
28-pin Ceramic LCC — K1	L29C521KC25	L29C521KC22	

Pin Assignments

Pin		Function	Pin		Function
P,D,C,F	J,K		P,D,C,F	J,K	
1	1	I_0	15	17	Y_6
2	2	I_1	16	19	Y_5
3	3	D_0	17	20	Y_4
4	5	D_1	18	21	Y_3
5	6	D_2	19	22	Y_2
6	7	D_3	20	23	Y_1
7	8	D_4	21	24	Y_0
8	9	D_5	22	26	S_1
9	10	D_6	23	27	S_0
10	12	D_7	24	28	V_{CC}
11	13	CLK		4	*NC*
12	14	GND		11	*NC*
13	15	$\overline{OE}$		18	*NC*
14	16	Y_7		25	*NC*

Ordering Information

Military Operating Range (–55°C to +125°C)

Package Style	Performance		
	30 ns	24 ns	
L29C520			
24-pin Sidebraze (0.3") Hermetic DIP — D2	L29C520DM30 L29C520DME30	L29C520DM24 L29C520DME24 L29C520DMB24	
24-pin CerDIP (0.3") — C1	L29C520CM30 L29C520CME30	L29C520CM24 L29C520CME24 L29C520CMB24	
24-pin Ceramic Flatpack — F1	L29C520FM30 L29C520FME30	L29C520FM24 L29C520FME24 L29C520FMB24	
28-pin Ceramic LCC — K1	L29C520KM30 L29C520KME30	L29C520KM24 L29C520KME24 L29C520KMB24	
L29C521			
24-pin Sidebraze (0.3") Hermetic DIP — D2	L29C521DM30 L29C521DME30	L29C521DM24 L29C521DME24 L29C521DMB24	
24-pin CerDIP (0.3") — C1	L29C521CM30 L29C521CME30	L29C521CM24 L29C521CME24 L29C521CMB24	
24-pin Ceramic Flatpack — F1	L29C521FM30 L29C521FME30	L29C521FM24 L29C521FME24 L29C521FMB24	
28-pin Ceramic LCC — K1	L29C521KM30 L29C521KME30	L29C521KM24 L29C521KME24 L29C521KMB24	

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Multilevel Pipeline Register — LPR520/521

Features

- Four 16-bit registers
- Implements double 2-stage pipeline or single 4-stage pipeline register
- Hold, Shift, Load instructions
- Separate data in and data out pins
- High-speed, low-power CMOS technology
- Three-state outputs
- Available 100% screened to MIL-STD-883, Class B
- Package styles available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC (Type C)

Description

The Logic Devices **LPR520** and **LPR521** are functionally compatible with the Advanced Micro Devices AM29520 and AM29521 but are 16 bits wide. They are implemented in low power CMOS.

The LPR520 and LPR521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the LPR520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The LPR521 devices differ from the LPR520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

Table 1

I_1	I_0	LPR520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

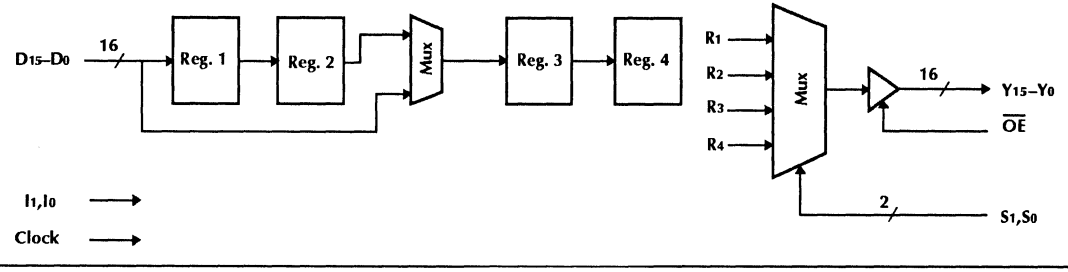
Table 2

I_1	I_0	LPR521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

Table 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

LPR520/521 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8	–20		–100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	25	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

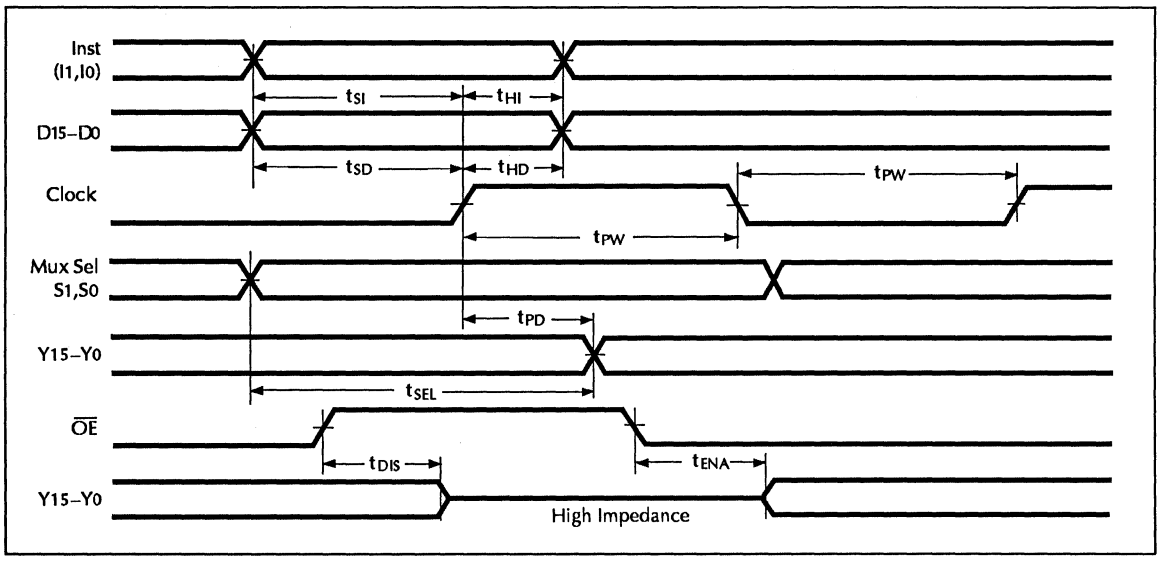
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LPR52x-25		LPR52x-22	
		Min	Max	Min	Max
t_{PD}	CLK to Y_{15}–Y_0		25		22
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		25		20
t_{SD}	D_{15}–D_0 to CLK Setup	13		10	
t_{HD}	CLK to D_{15}–D_0 Hold	3		3	
t_{SI}	I_1,I_0 to CLK Setup	13		10	
t_{HI}	CLK to I_1,I_0 Hold	3		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21
t_{PW}	Clock Pulse Width	10		10	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LPR52x-30		LPR52x-24	
		Min	Max	Min	Max
t_{PD}	CLK to Y_{15}–Y_0		30		24
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		30		22
t_{SD}	D_{15}–D_0 to CLK Setup	15		10	
t_{HD}	CLK to D_{15}–D_0 Hold	5		3	
t_{SI}	I_1,I_0 to CLK Setup	15		10	
t_{HI}	CLK to I_1,I_0 Hold	5		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22
t_{PW}	Clock Pulse Width	15		10	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

3

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance		
	25 ns	22 ns	
LPR520			
40-pin Plastic DIP (0.6") — P3	LPR520PC25	LPR520PC22	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LPR520DC25	LPR520DC22	
44-pin Plastic LCC, J-Lead — J1	LPR520JC25	LPR520JC22	
44-pin Ceramic LCC — K2	LPR520KC25	LPR520KC22	
LPR521			
40-pin Plastic DIP (0.6") — P3	LPR521PC25	LPR521PC22	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LRP521DC25	LPR521DC22	
44-pin Plastic LCC, J-Lead — J1	LRP521JC25	L29C521JC22	
44-pin Ceramic LCC — K2	LPR521KC25	LPR521KC22	

Military Operating Range (–55°C to +125°C)

Package Style	Performance		
	30 ns	24 ns	
LPR520			
40-pin Sidebraze (0.6") Hermetic DIP — D3	LPR520DM30 LPR520DME30	LPR520DM24 LPR520DME24 LPR520DMB24	
44-pin Ceramic LCC — K2	LPR520KM30 LPR520KME30	LPR520KM24 LPR520KME24 LPR520KMB24	
LPR521			
40-pin Sidebraze (0.6") Hermetic DIP — D3	LPR521DM30 LPR521DME30	LPR521DM24 LPR521DME24 LPR521DMB24	
44-pin Ceramic LCC — K2	LPR521KM30 LPR521KME30	LPR521KM24 LPR521KME24 LPR521KMB24	

Pin Assignments

Pin		Function	Pin		Function
P,D	J		P,D	J	
1	1	I_0	23	25	Y_{14}
2	2	I_1	24	26	Y_{13}
3	3	D_0	25	27	Y_{12}
4	4	D_1	26	29	Y_{11}
5	5	D_2	27	30	Y_{10}
6	7	D_3	28	31	Y_9
7	8	D_4	29	32	Y_8
8	9	D_5	30	33	Y_7
9	10	D_6	31	34	Y_6
10	11	D_7	32	35	Y_5
11	12	D_8	33	36	Y_4
12	13	D_9	34	37	Y_3
13	14	D_{10}	35	38	Y_2
14	15	D_{11}	36	40	Y_1
15	16	D_{12}	37	41	Y_0
16	18	D_{13}	38	42	S_1
17	19	D_{14}	39	43	S_0
18	20	D_{15}	40	44	V_{CC}
19	21	CLK		6	*NC*
20	22	GND		17	*NC*
21	23	$\overline{OE}$		28	*NC*
22	24	Y_{15}		39	*NC*

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Dual Pipeline Register

L29C524/525

Features

- Pipeline Registers — dual 7-deep (L29C524) or dual 8-deep (L29C525)
- Configurable to single 14-deep and single 16-deep
- Hold, Shift, Load instructions
- Separate data in and data out pins
- High-speed, low-power CMOS technology
- Three-state outputs
- Available 100% screened to MIL-STD-883, Class B
- Plug-compatible with AMD AM29524 and AM29525
- Package styles available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP

Description

The Logic Devices **L29C524** and **L29C525** are high performance, low power CMOS pipeline registers. They are pin-for-pin compatible with the Advanced Micro Devices Am29524 and Am29525. The products can be configured as two independent, 7-level (or 8-level) pipelines or as single 14-level (or 16-level) pipelines. The configuration implemented is determined by the instruction code (I_1,I_0) as shown in Table 2.

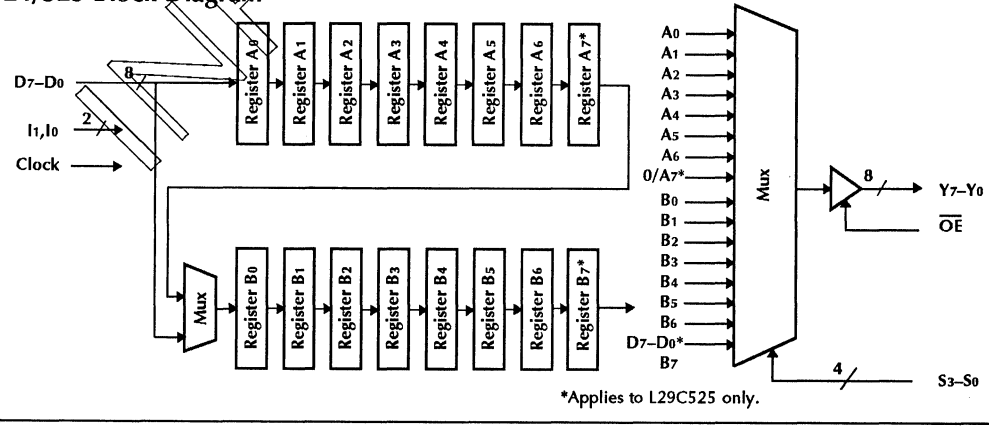
The I_1,I_0 instruction code controls the internal routing of data and loading of each register. For instruction $I_1,I_0 = 00$ (Push A & B), data applied at the D_7–D_0 inputs is loaded into register A_0 at the rising edge of the Clock. The contents of A_0 simultaneously moves to register A_1, A_1 moves to A_2, and so on. The contents of the last register on the "A" side (A_6 for the L29C524, A_7 for the L29C525) are wrapped back to register B_0. The registers on the B side are similarly shifted, with the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) lost.

Instruction $I_1,I_0 = 01$ (Push B) acts similarly to the Push A & B instruction, except that only the B side registers are shifted. The input data is applied to register B_0, and the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) are lost. The contents of the A side registers are unaffected. Instruction $I_1,I_0 = 10$ (Push A) is identical to the Push B instruction, except that A side registers are shifted and B side registers are unaffected.

Instruction $I_1,I_0 = 11$ (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

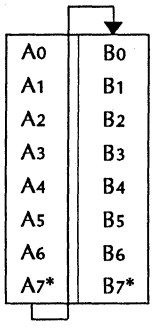
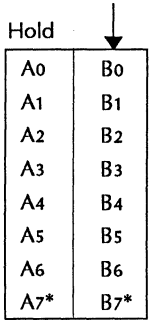
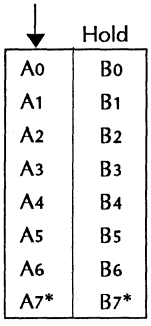
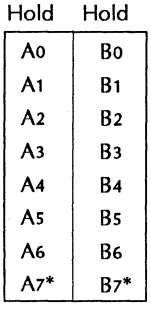
The contents of any of the registers is selectable at the output through the use of the S_3–S_0 control inputs. On the L29C524, the input pins D_7–D_0 may also be selected to drive the output, and all output pins may be forced to zero. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_3–S_0 controls is given in Table 3.

L29C524/525 Block Diagram



*Applies to L29C525 only.

Table 1. Register Load Operations (See Table 2 for instruction codes.)

Single 14/16 Level	Dual 7/8 Level		
Push A & B	**Push B**	**Push A**	**No-Op**
			

* A7 and B7 registers apply only to L29C525

Table 2. Instruction Set Descriptions

Mnemonic	Inputs		Description
	I_1	I_0	
Shift	0	0	Push A & B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	No-Op

Table 3. Select Operation Descriptions

S_3	S_2	S_1	S_0	Y_7–Y_0
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	1	A6
0	1	1	1	0 (L29C524) A7 (L29C525)
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	1	D7–D0 (L29C524) B7 (L29C525)

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –15.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–100	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		10	15	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

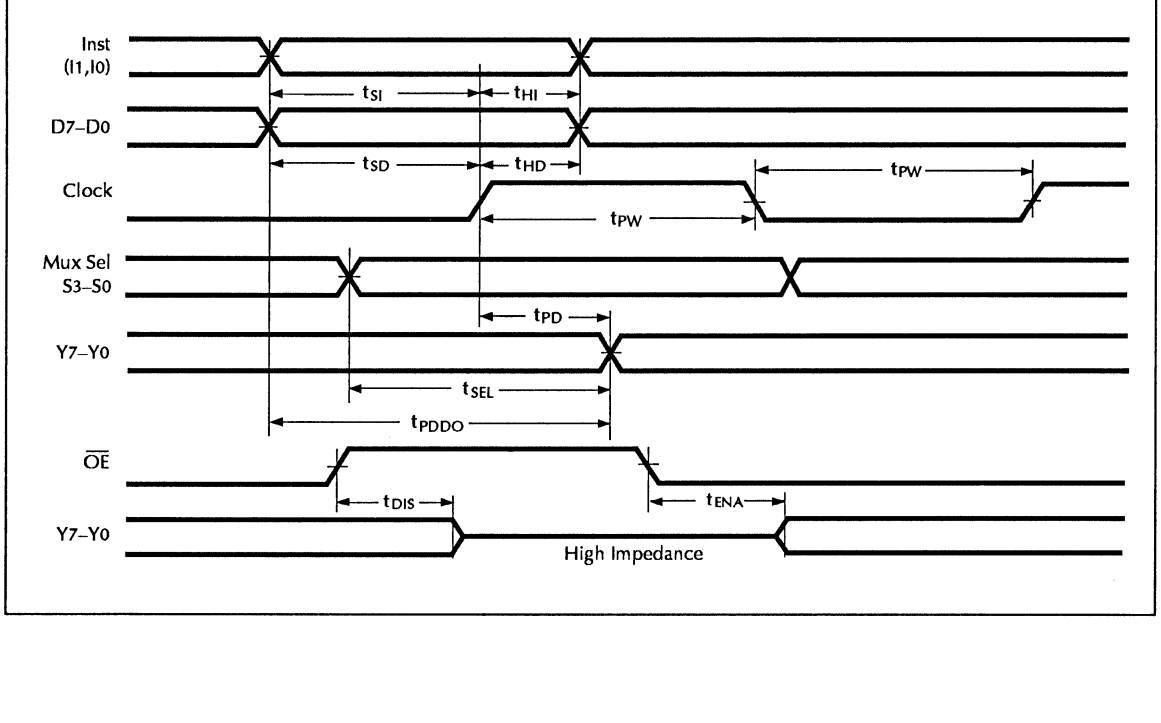
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter				
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0				
t_{SEL}	S_3–S_0 to Y_7–Y_0				
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)				
t_{SD}	D_7–D_0 to CLK Setup				
t_{HD}	CLK to D_7–D_0 Hold				
t_{SI}	I_1,I_0 to CLK Setup				
t_{HI}	CLK to I_1,I_0 Hold				
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)				
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)				
t_{PW}	Clock Pulse Width				

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter				
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0				
t_{SEL}	S_3–S_0 to Y_7–Y_0				
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)				
t_{SD}	D_7–D_0 to CLK Setup				
t_{HD}	CLK to D_7–D_0 Hold				
t_{SI}	I_1,I_0 to CLK Setup				
t_{HI}	CLK to I_1,I_0 Hold				
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)				
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)				
t_{PW}	Clock Pulse Width				

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Contact Factory

Pin Assignments

Pin	Function	Pin	Function
1	S_1	15	I_1
2	S_0	16	Y_7
3	D_0	17	Y_6
4	D_1	18	Y_5
5	D_2	19	Y_4
6	D_3	20	$\overline{OE}$
7	V_{CC}	21	GND
8	GND	22	V_{CC}
9	D_4	23	Y_3
10	D_5	24	Y_2
11	D_6	25	Y_1
12	D_7	26	Y_0
13	I_0	27	S_3
14	CLK	28	S_2

3

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Variable Length Shift Register

L10C11

Features

- Variable length 4 or 8 bit-wide shift register
- Selectable length from 3 to 18 stages
- Hold, Shift, Load instructions
- Separate data in and data out pins
- High-speed, low-power CMOS technology
- Plug-compatible with TRW TDC1011
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebraze, Hermetic DIP

Description

The **L10C11** consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock. Both shift registers can be programmed together to any length from 3 to 18 stages inclusive, or one register can be fixed at 18 stages of delay while the other is variable. The configuration implemented is determined by the Length code (L_3–L_0) and MODE line as shown in Table 1.

Each input is applied to a chain of registers which are clocked on the rising edge of the common CLK input. These registers are numbered R1 through R17 and R1' to R17', corresponding to the D3–D0 and D7–D4 data fields, respectively. A multiplexer serves to route the contents of any of registers R2 through R17 to the output register, denoted R18. A similar multiplexer operates on the contents of R2' through R17' to load R18'. Note that the minimum-length path from data inputs to outputs is R1 to R2 to R18, consisting of three stages of delay.

The MODE control input is registered, and determines whether one or both of the internal shift registers have variable length. When MODE=0, both D3–D0 and D7–D4 are delayed by an amount which is controlled by the Length inputs. When MODE=1, the D7–D4 field is delayed by 18 stages independent of the Length setting.

The Length code controls the number of stages of delay applied to the D inputs, as shown in Table 1. When the Length register contains 0, the inputs are delayed by 3 clock periods. When the Length register contains 1, the delay is 4 clock periods, and so forth. The Length control field (L3–L0) and the MODE input are registered at the rising edge of the Clock. Both the length and MODE values may be changed at any time without affecting the contents of registers R17–R1.

L10C11 Block Diagram

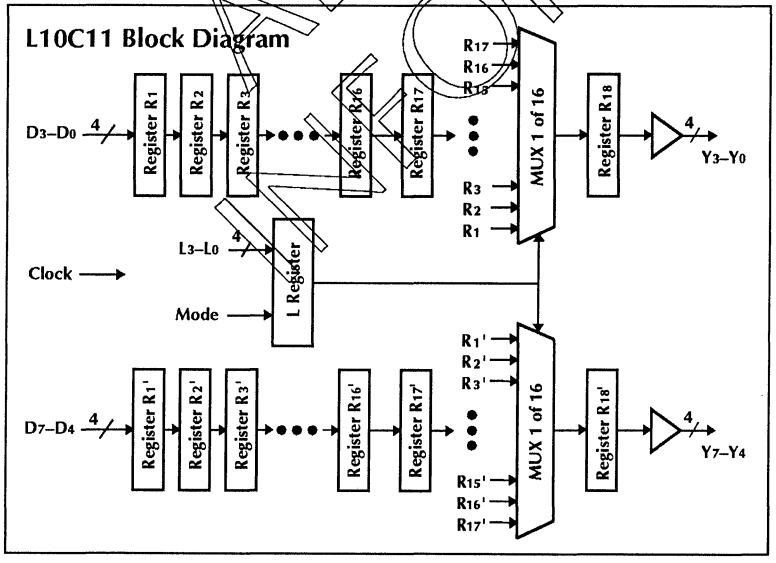


Table 1. Control Encoding

Input Code				Mode=0 Delay		Mode=1 Delay	
L_3	L_2	L_1	L_0	Y3–0	Y7–4	Y3–0	Y7–4
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –15.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

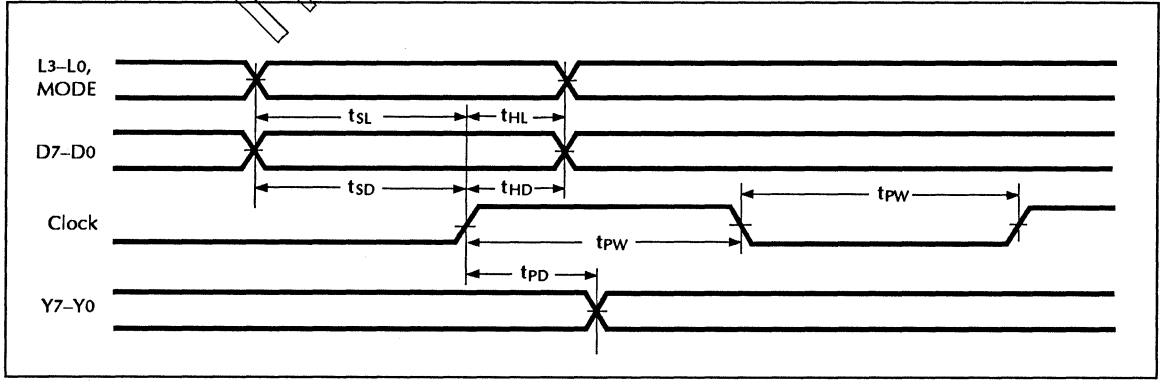
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter				
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0				
t_{SD}	D_7–D_0 to CLK Setup				
t_{HD}	CLK to D_7–D_0 Hold				
t_{SL}	L_3–L_0, MODE to CLK Setup				
t_{HL}	CLK to L_3–L_0, MODE Hold				
t_{PW}	Clock Pulse Width				

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter				
		Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0				
t_{SD}	D_7–D_0 to CLK Setup				
t_{HD}	CLK to D_7–D_0 Hold				
t_{SL}	L_3–L_0, MODE to CLK Setup				
t_{HL}	CLK to L_3–L_0, MODE Hold				
t_{PW}	Clock Pulse Width				

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Call Factory

Pin Assignments

Pin	Function	Pin	Function
1	D_0	13	Y_0
2	D_1	14	Y_1
3	D_2	15	Y_2
4	D_3	16	Y_3
5	L_0	17	L_2
6	L_1	18	L_3
7	Vcc	19	GND
8	CLK	20	MODE
9	D_4	21	Y_4
10	D_5	22	Y_5
11	D_6	23	Y_6
12	D_7	24	Y_7

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Serial Scan Register

L29C818

Features

- Octal register with additional 8-bit shiftable shadow register
- Serial load/verify of writable control store RAM
- Serial stimulus/observation of sequential logic
- High-speed, low-power CMOS technology
- Available 100% screened to MIL-STD-883, Class B
- Plug compatible with AMD Am29818
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC

Description

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

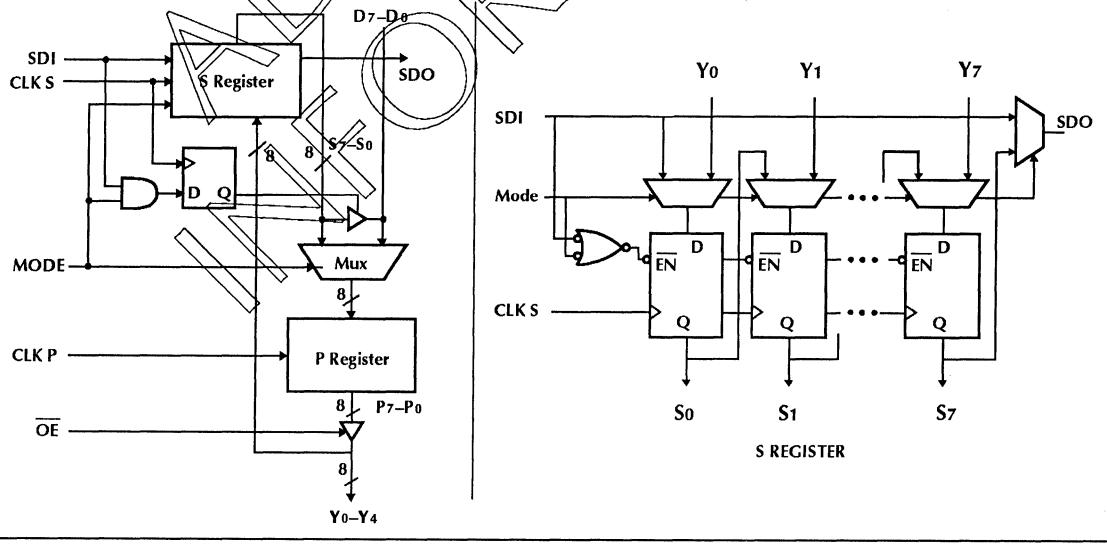
The L29C818 consists of an octal register (the "P" register), internally connected to an 8-bit shift register (the "S" register). Each has its own corresponding clock pin, and the P register has a three-state output control.

An input control signal MODE, in combination with the S register serial data input pin SDI controls data routing within the L29C818. When the MODE input is low, indicating normal operation, data present on the D7–D0 pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y7–Y0 when the $\overline{OE}$ control line is low.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right shift operation, with the contents of each bit position replaced by the value in the next least significant location. The value in S7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is low, the operation of the P and S registers are completely independent, and no timing relationship is enforced between CLK P and CLK S.

When MODE is high, the internal multiplexers route data between the S and P registers, and the Y port. The contents of the S register are loaded into the P register on the rising edge of CLK P. In diagnostic applications,

L29C818 Block Diagram



this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is high, CLK S causes a parallel rather than serial load of the S register. In this mode, the S register is loaded from the Y_7–Y_0 pins at the rising edge of CLK S. This is useful in writable control store applications for readback of the control store via the serial path.

When MODE is high, the SDI pin is used as a control input to enable or disable the loading of the S register, and it also affects routing of the S register contents onto the D_7–D_0 outputs. When SDI is low, the S register is enabled for loading as above. When SDI is high however, CLK S is prevented from reaching the S register, and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is high, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_7–D_0 port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_7–D_0 pins. This is accomplished when MODE and SDI are high, and a CLK S rising edge occurs. Note from above that with SDI high, no loading of the S register occurs. However, a flip-flop is set which syncronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is low. Thus to load a control store RAM, data would be shifted in with MODE low. When an entire control store word was present in the serial S registers, the SDI and MODE pins are brought high for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE high with SDI low. Then, the S register contents are scanned out serially by returning MODE to low and applying CLK S pulses.

Table 1. Function table.

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_7–Y_0	D_7–D_0	SDO
0	X	↑	X	N/A	SHIFT	Normal	Hi-Z	S_7
0	X	X	↑	LOAD D	N/A	Normal	Input	S_7
1	0	↑	X	N/A	LOAD Y	Input*	Hi-Z	SDI
1	1	↑	X	N/A	HOLD	Normal	Output	SDI
1	X	X	↑	LOAD S	N/A	Normal	Hi-Z	SDI

* If $\overline{OE}$ is 0, the D register value will be loaded into the S register. If $\overline{OE}$ is 1, a value may be applied externally to the Y_7–Y_0 pins.

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −15.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			−100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

Switching Characteristics

Symbol	Parameter				
		Min	Max	Min	Max
t_{PD}	CLK P to Y_7–Y_0				
	MODE to SDO				
	SDI to SDO				
	CLK S to SDO				
t_S	D_7–D_0 to CLK P Setup				
	MODE to CLK P Setup				
	Y_7–Y_0 to CLK S Setup				
	MODE to CLK S Setup				
	SDI to CLK S Setup				
	CLK S to CLK P Setup				
	CLK P to CLK S Setup				
t_H	CLK P to D_7–D_0 Hold				
	CLK P to MODE Hold				
	CLK S to Y_7–Y_0 Hold				
	CLK S to SDI Hold				
t_{PW}	CLK S Pulsewidth (High and Low)				
	CLK P Pulsewidth (High and Low)				
t_{ENA}	$\overline{OE}$ to Y_7–Y_0 Enable				
	CLK S to D_7–D_0 Enable				
t_{DIS}	$\overline{OE}$ to Y_7–Y_0 Disable				
	CLK S to D_7–D_0 Disable				

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

3

Ordering Information

Call Factory

Pin Assignments

Pin		Function	Pin		Function
P,D	K		P,D	K	
1	2	$\overline{OE}$	15	18	Y7
2	3	CLK S	16	19	Y6
3	4	D0	17	20	Y5
4	5	D1	18	21	Y4
5	6	D2	19	23	Y3
6	7	D3	20	24	Y2
7	9	D4	21	25	Y1
8	10	D5	22	26	Y0
9	11	D6	23	27	MODE
10	12	D7	24	28	Vcc
11	13	SDI		1	*NC*
12	14	GND		8	*NC*
13	16	CLK P		15	*NC*
14	17	SDO		22	NC

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Features

- 8-word × 8-bit three port memory
- Independently addressable ports: 1 input, 1 output, 1 bidirectional
- High-speed, low-power CMOS technology
- Internally-latched control bits
- High-speed scratchpad memory with overlapped data fetch/store
- Fully TTL compatible
- 60 mW typical power dissipation
- Package styles available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Ceramic LCC (Type C)

Description

The **LRF07** is an 8 word × 8 bit expandable register file with three independently addressable ports, designated A, B, and C. Each port has eight data lines, three address lines and a port enable control. All address and control lines are registered to facilitate instruction pipelining in microprogrammed systems. All ports may be used simultaneously in any clock cycle.

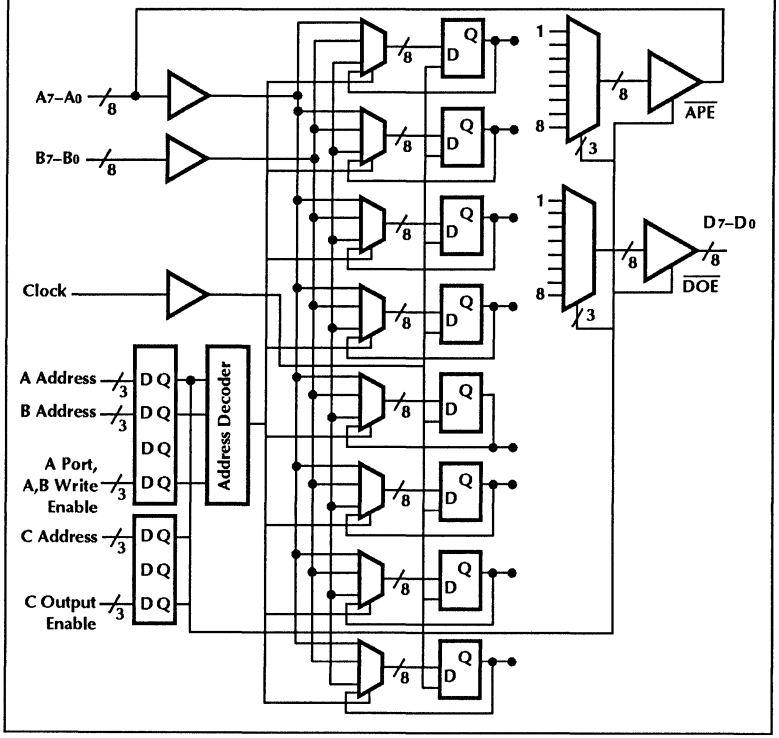
The C port is a read only port. C port address lines (CA_2–CA_0) are latched at the rising edge of the clock. The data indicated by the respective port address will be presented on the output lines one TACC following the clock edge on which the address is latched. If the same register is simultaneously addressed for writing from a different port, the data presented to the outputs is the contents of the register prior to the write operation.

The B port is a write port. B port address lines (BA_2–BA_0) are latched at the rising edge of the clock. The contents of the B address register are decoded to control data routing multiplexers. These supply data from the input pins to the desired register. Data meeting the setup time is latched into the addressed register on the clock edge following the one which latched the address. Simultaneous writes to the same register from multiple ports result in storage of the logical 'OR' of the input data.

The A port is a bidirectional port. The A Read/Write control AR/$\overline{W}$ is latched along with the address lines (AA_2–AA_0) and determines whether the A port acts as an input or an output during any clock period. When AR/$\overline{W}$ is a '1' at the clock edge, the A port presents the addressed data on the A_7–A_0 data lines. A port read operations are thus performed identically to C port reads. When AR/$\overline{W}$ is a '0' at the clock edge, A port writes are executed in the same manner as B port writes, with the data latched on the clock edge following application of the corresponding address.

All ports have associated port enable inputs. These inputs are internally registered and are applied simultaneously with the corresponding port address. In the case of the C port, the $\overline{COE}$ input is a three state output control. A '1' at these inputs places the corresponding data lines in a high impedance state beginning one TDIS following the clock edge. The B port enable $\overline{BWE}$ serves as a registered write enable input. A '1' latched on these inputs disables write operations from the port on the following clock edge. The A port enable $\overline{APE}$, serves the dual function of write enable or three state enable depending on the direction of the A port.

LRF07 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 150 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8	–20		–100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

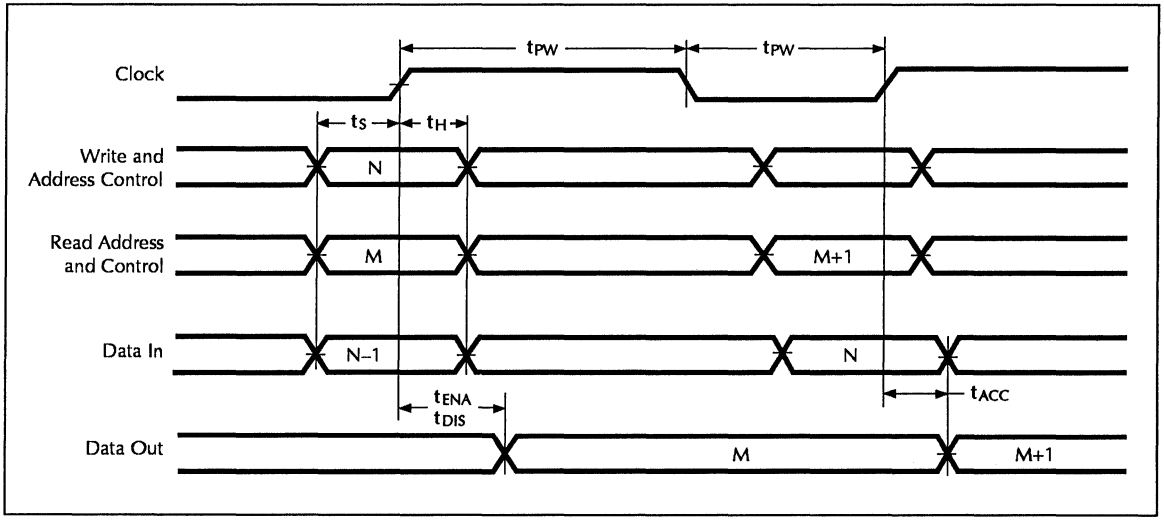
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LRF07-35 Min	LRF07-35 Max
t_{ACC}	CLK to Output		35
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LRF07-35 Min	LRF07-35 Max
t_{ACC}	CLK to Output		35
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance 35ns
LRF07	
40-pin Plastic DIP (0.6") — P3	LRF07PC35
40-pin Sidebraze (0.6") Hermetic DIP — D3	LRF07DC35
44-pin Ceramic LCC — K2	LRF07KC35

Military Operating Range (–55°C to +125°C)

Package Style	Performance 35ns
LRF07	
40-pin Sidebraze (0.6") Hermetic DIP — D3	LRF07DM35 LRF07DME35 LRF07DMB35
44-pin Ceramic LCC — K2	LRF07KM35 LRF07KME35 LRF07KMB35

Pin Assignments

Pin P,D	Pin K	Function	Pin P,D	Pin K	Function
1	1	B_3	23	25	C_5
2	2	B_2	24	26	C_6
3	3	B_1	25	27	C_7
4	4	B_0	26	29	CA_2
5	5	A_0	27	30	CA_1
6	7	A_1	28	31	CA_0
7	8	A_2	29	32	CLK
8	9	A_3	30	33	AA_2
9	10	A_4	31	34	AA_1
10	11	A_5	32	35	AA_0
11	12	A_6	33	36	$\overline{BWE}$
12	13	A_7	34	37	BA_2
13	14	GND	35	38	BA_1
14	15	V_{CC}	36	39	BA_0
15	16	$\overline{APE}$	37	41	B_7
16	17	$AR/\overline{W}$	38	42	B_6
17	19	$\overline{COE}$	39	43	B_5
18	20	C_0	40	44	B_4
19	21	C_1		6	*NC*
20	22	C_2		18	*NC*
21	23	C_3		28	*NC*
22	24	C_4		40	*NC*

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Features

- 8-word × 8-bit five port memory
- Independently addressable ports: 2 input, 2 output, 1 bidirectional
- High-speed, low-power CMOS technology
- Internally-latched control bits
- High-speed scratchpad memory with overlapped data fetch/store
- Available 100% screened to MIL-STD-883, Class B
- Fully TTL compatible
- 60 mW typical power dissipation
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array

Description

The **LRF08** is an 8 word × 8 bit expandable register file with five independently addressable ports, designated A through E. Each port has eight data lines, three address lines and a port enable control. All address and control lines are registered to facilitate instruction pipelining in microprogrammed systems. All ports may be used simultaneously in any clock cycle.

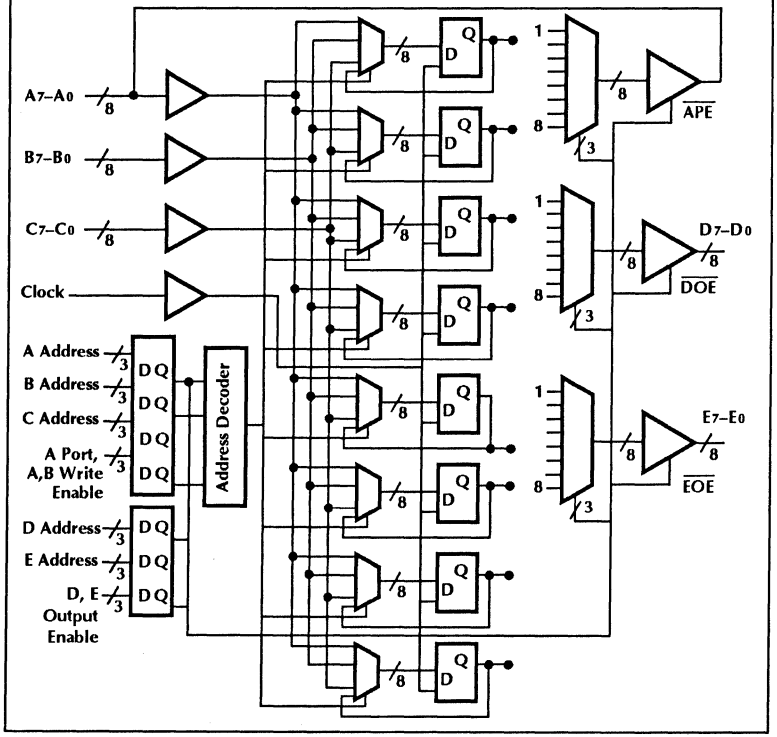
The D and E ports are read only ports. D and E address lines (DA_2–DA_0 and EA_2–EA_0) are latched at the rising edge of the clock. The data indicated by the respective port address will be presented on the output lines one TACC following the clock edge on which the address is latched. If the same register is simultaneously addressed for writing from a different port, the data presented to the outputs is the contents of the register prior to the write operation.

The B and C ports are write ports. B and C address lines (BA_2–BA_0 and CA_2–CA_0) are latched at the rising edge of the clock. The contents of the B and C address registers are decoded to control data routing multiplexers. These supply data from the input pins to the desired register. Data meeting the set-up time is latched into the addressed register on the clock edge following the one which latched the address. Simultaneous writes to the same register from multiple ports result in storage of the logical 'OR' of the input data.

The A port is a bidirectional port. The A Read/Write control AR/$\overline{W}$ is latched along with the address lines (AA_2–AA_0) and determines whether the A port acts as an input or an output during any clock period. When AR/$\overline{W}$ is a '1' at the clock edge, the A port presents the addressed data on the A_7–A_0 data lines. A port read operations are thus performed identically to D and E port reads. When AR/$\overline{W}$ is a '0' at the clock edge, A port writes are executed in the same manner as B and C port writes, with the data latched on the clock edge following application of the corresponding address.

All ports have associated port enable inputs. These inputs are internally registered and are applied simultaneously with the corresponding port address. In the case of the D and E ports, the $\overline{DOE}$ and $\overline{EOE}$ inputs are three state output controls. A '1' at these inputs places the corresponding data lines in a high impedance state beginning one TDIS following the clock edge. The B and C port enables $\overline{BWE}$ and $\overline{CWE}$ serve as registered write enable inputs. A '1' latched on these inputs disables write operations from the port on the following clock edge. The A port enable $\overline{APE}$, serves the dual function of write enable or three state enable depending on the direction of the A port.

LRF08 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 150 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8	–20		–100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	45	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

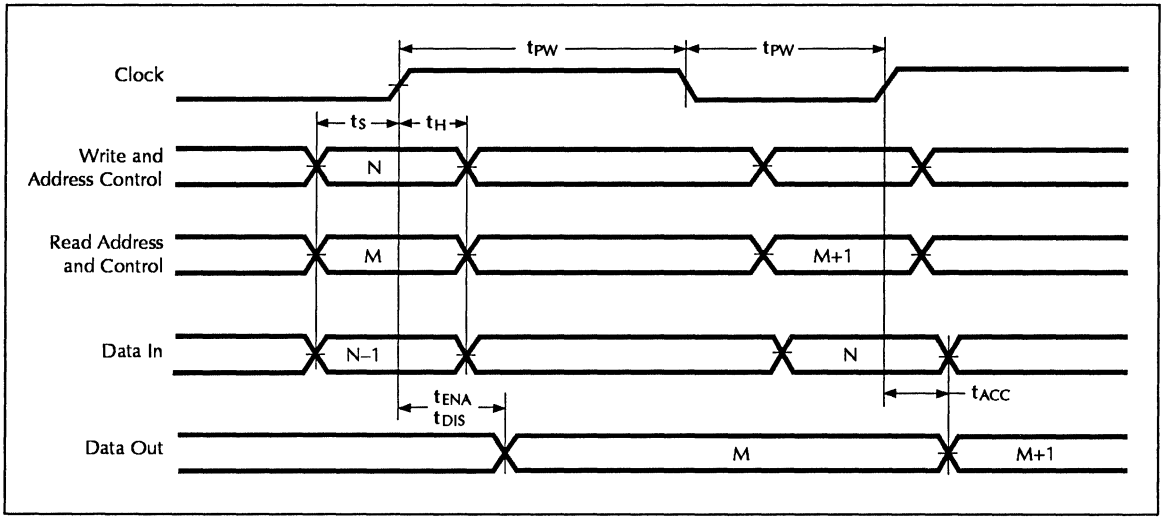
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LRF08-35 Min	LRF08-35 Max
t_{ACC}	CLK to Output		35
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LRF08-35 Min	LRF08-35 Max
t_{ACC}	CLK to Output		35
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance 35 ns
LRF08	
64-pin Plastic DIP — P4	LRF08PC35
64-pin Sidebraze Hermetic DIP — D4	LRF08DC35
68-pin Plastic LCC, J-Lead — J2	LRF08JC35
68-pin Pin Grid Array — G1	LRF08GC35
68-pin Ceramic LCC — K3	LRF08KC35

Military Operating Range (–55°C to +125°C)

Package Style	Performance 35 ns
LRF08	
64-pin Sidebraze Hermetic DIP — D4	LRF08DM35 LRF08DME35
68-pin Pin Grid Array — G1	LRF08GM35 LRF08GME35

Pin Assignments

Pin P,D	Pin J,K	Pin G	Function	Pin P,D	Pin J,K	Pin G	Function
1	1	G01	C_1	35	37	G10	D_2
2	2	F02	C_0	36	38	G11	D_3
3	3	F01	B_7	37	39	H10	D_4
4	4	E02	B_6	38	40	H11	D_5
5	5	E01	B_5	39	41	J10	D_6
6	6	D02	B_4	40	42	J11	D_7
7	7	D01	B_3	41	44	K10	EA_2
8	8	C02	B_2	42	45	L10	EA_1
9	9	C01	B_1	43	46	K09	EA_0
10	10	B01	B_0	44	47	L09	DA_2
11	11	B02	A_0	45	48	K08	DA_1
12	12	A02	A_1	46	49	L08	DA_0
13	13	B03	A_2	47	50	K07	CLK
14	14	A03	A_3	48	51	L07	AA_2
15	15	B04	A_4	49	52	K06	AA_1
16	16	A04	A_5	50	53	L06	AA_0
17	17	B05	A_6	51	54	K05	$\overline{CWE}$
18	18	A05	A_7	52	55	L05	CA_2
19	19,20	B06	GND	53	56	K04	CA_1
20	21,22	A06	V_{CC}	54	57	L04	CA_0
21	23	B08	$\overline{APE}$	55	58	K03	$\overline{BWE}$
22	24	A08	$AR/\overline{W}$	56	59	L03	BA_2
23	25	B09	$\overline{EOE}$	57	61	L02	BA_1
24	26	A09	$\overline{DOE}$	58	62	K02	BA_0
25	27	B10	E_0	59	63	K01	C_7
26	28	B11	E_1	60	64	J02	C_6
27	29	C10	E_2	61	65	J01	C_5
28	30	C11	E_3	62	66	H02	C_4
29	31	D10	E_4	63	67	H01	C_3
30	32	D11	E_5	64	68	G02	C_2
31	33	E10	E_6		43	A07	*NC*
32	34	E11	E_7		60	B07	*NC*
33	35	F10	D_0			A10	*NC*
34	36	F11	D_1			K34	*NC*

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16-bit Cascadable ALU

L4C381

Features

- High-speed (26 ns), low power 16-bit cascadable ALU
- Implements add, subtract, accumulate, 2's complement, pass, and logic operations
- All registers have a bypass path for complete flexibility
- Available in MIL-STD-883 compliant version
- Package styles available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **L4C381** is a flexible, high-speed, cascadable 16-bit Arithmetic and Logic Unit implemented in CMOS technology. It combines four 381-type 4-bit ALUs, a lookahead-carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high-speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

Architecture

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

ALU Operations

The S0–S2 lines specify the operation to be performed. The ALU functions and their select codes are shown below.

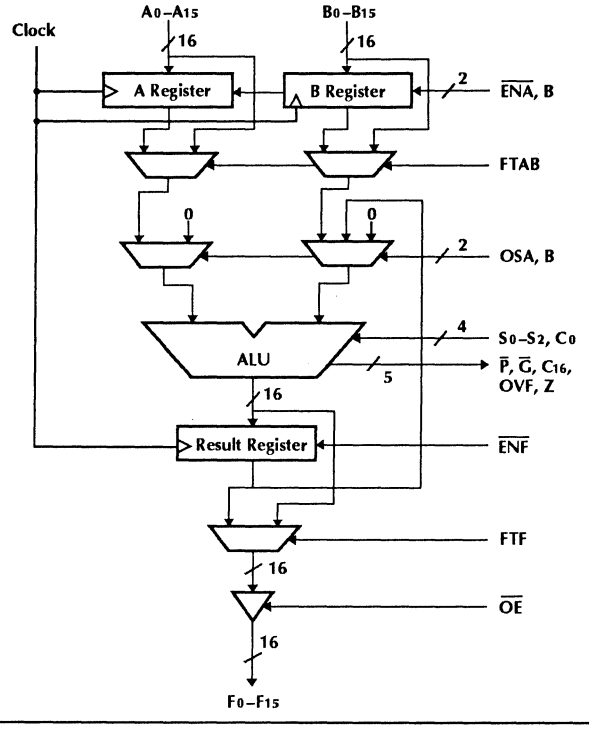
S2	S1	S0	Function
0	0	0	CLEAR (F=00 ... 0)
0	0	1	NOT (A) + B
0	1	0	A + NOT (B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F=11 ... 1)

The functions B minus A and A minus B can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

ALU Status

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are

L4C381 Block Diagram



zero. The Generate, Propagate, C16, and OVF flags for the A + B operation are defined in Table 1. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing Ai and Bi respectively in Table 1.

Table 1. ALU Status Flags

Bit Carry Generate = gi = AiBi,	for i = 0 ... 15
Bit Carry Propagate = pi = Ai + Bi,	for i = 0 ... 15
P0 = p0	for i = 1 ... 15
Pi = pi (Pi–1)	for i = 1 ... 15
and	
G0 = g0	
Gi = gi + pi (Gi–1)	for i = 1 ... 15
Ci = Gi–1 + Pi–1 (C0)	for i = 1 ... 15
then	
$\overline{G}$ = NOT (G15)	
$\overline{P}$ = NOT (P15)	
C16 = G15 + P15C0	
OVF = C15 XOR C16	

Operand Registers

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. Each register is independently enabled by control signals $\overline{ENA}$ and $\overline{ENB}$.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted, data is routed around the A and B input registers; however, they continue to function normally via the $\overline{ENA}$ and $\overline{ENB}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

Output Register

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. The output register is enabled by the $\overline{ENF}$ control signal. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{OE}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal. When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{ENF}$ control. The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (high) the L4C381 is functionally identical to four cascaded 54S381-type devices.

Operand Selection

The two operand select lines OSA and OSB control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F-register feedback to the B input. Table 2 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU (FTF = true). The output register continues to function, however, and provides the ALU B operand source.

Table 2. Operand Selection Control

OSB	OSA	Operand B	Operand A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

Switching Characteristics

Over Commercial Operating Range (Notes 9, 10)

***Guaranteed Maximum Combinational Delays** (ns)*

To Output / From Input	L4C381-55				L4C381-40				L4C381-26			
	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	28	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_0–A_{15}, B_0–B_{15}	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_0–A_{15}, B_0–B_{15}	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA,B=0)	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

***Guaranteed Minimum Setup and Hold Times With Respect to Clock Rising Edge** (ns)*

Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_0–A_{15}, B_0–B_{15}	8	0	35	0	6	0	28	0	6	0	16	0
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_0–S_2, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	8	2	8	2	6	2	6	2	6	2	6	2

***Three State Enable/Disable Times** (ns) (Note 11)*

	L4C381-55	L4C381-40	L4C381-26
t_{EN}	20	18	16
t_{DIS}	20	18	16

***Clock Cycle Time and Pulse Width** (ns)*

	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

Switching Characteristics

Over Military Operating Range (Notes 9, 10)

Guaranteed Maximum Combinational Delays (ns)

To Output / From Input	L4C381-65				L4C381-45				L4C381-30			
	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_0–S_2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_0–S_2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A_0–A_{15}, B_0–B_{15}	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_0–S_2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A_0–A_{15}, B_0–B_{15}	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA,B=0)	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_0–S_2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

Guaranteed Minimum Setup and Hold Times With Respect to Clock Rising Edge (ns)

Input	L4C381-65				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_0–A_{15}, B_0–B_{15}	10	0	43	0	8	0	33	0	8	0	20	0
C_0	25	0	25	0	20	0	20	0	12	0	12	0
S_0–S_2, OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	10	2	10	2	8	2	8	2	8	2	8	2

Three State Enable/Disable Times (ns) (Note 11)

	L4C381-65	L4C381-45	L4C381-30
t_{EN}	22	20	18
t_{DIS}	22	20	18

Clock Cycle Time and Pulse Width (ns)

	L4C381-65	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Cascading the L4C381

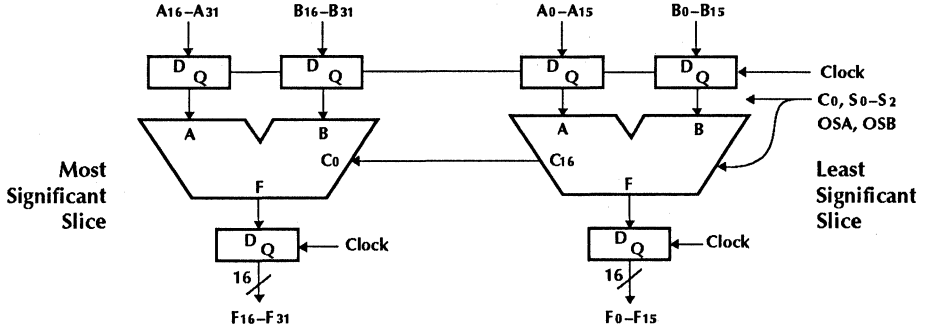
Cascading the L4C381 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most significant slice. The S_0–S_2, OSA, OSB, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figure 4.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path. A faster method is to use an external carry-lookahead generator. The $\overline{P}$ and $\overline{G}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C_0 inputs for each slice except the least significant. The C_{16} outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C_0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{P}$, $\overline{G}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C_0 to output time of the most significant slice.

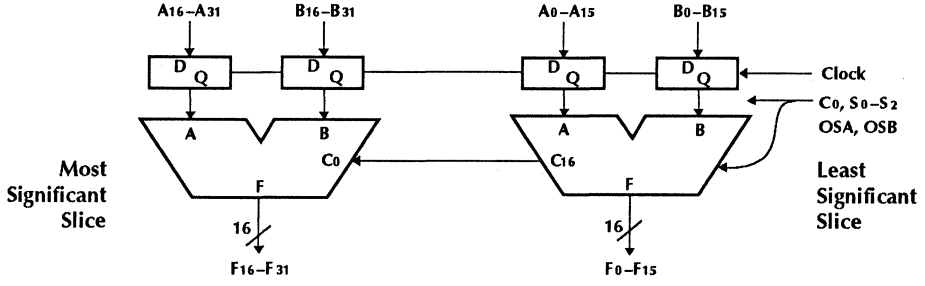
FTAB = 0
FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	Same as 16-bit case
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + C0 Setup
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C16) + (C0 Setup time)



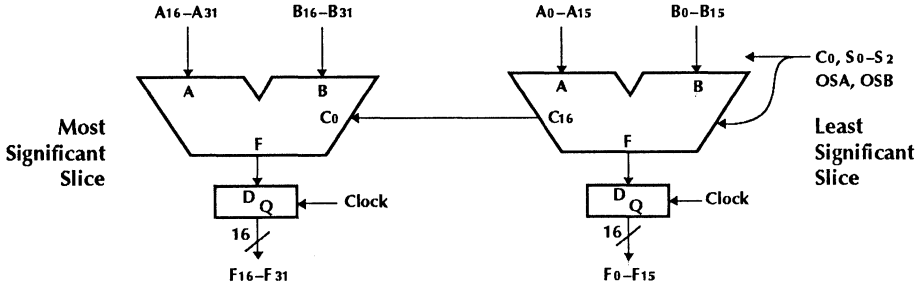
FTAB = 0
FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C16) + (C0 → F)
Clock	→ Other	=	(Clock → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ F	=	(S0–S2, OSA, OSB → C16) + (C0 → F)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	Same as 16-bit case
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C16) + (C0 Setup time)



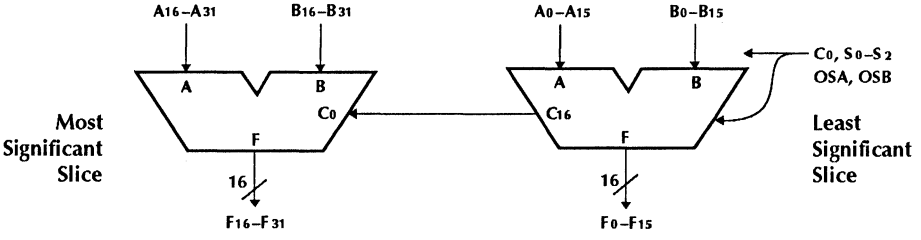
FTAB = 1
FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)



FTAB = 1
FTF = 1

From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C16) + (C0 → F)
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ F	=	(S0–S2, OSA, OSB → C16) + (C0 → F)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)



Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance		
	55 ns	40 ns	26 ns
L4C381			
68-pin Plastic LCC, J-Lead — J2	L4C381JC55	L4C381JC40	L4C381JC26
68-pin Pin Grid Array — G1	L4C381GC55	L4C381GC40	L4C381GC26
68-pin Ceramic LCC — K3	L4C381KC55	L4C381KC40	L4C381KC26

Military Operating Range (–55°C to +125°C)

Package Style	Performance		
	65 ns	45 ns	30 ns
L4C381			
68-pin Pin Grid Array — G1	L4C381GM65 L4C381GME65	L4C381GM45 L4C381GME45 L4C381GMB45	L4C381GM30 L4C381GME30 L4C381GMB30
68-pin Ceramic LCC — K3	L4C381KM65 L4C381KME65	L4C381KM45 L4C381KME45 L4C381KMB45	L4C381KM30 L4C381KME30 L4C381KMB30

Pin Assignments

Pin		Function	Pin		Function
J,K	G		J,K	G	
1	F02	A_0	35	F10	F_8
2	F01	A_1	36	F11	F_7
3	E02	A_2	37	G10	F_6
4	E01	A_3	38	G11	F_5
5	D02	A_4	39	H10	F_4
6	D01	A_5	40	H11	F_3
7	C02	A_6	41	J10	F_2
8	C01	A_7	42	J11	F_1
9	B01	A_8	43	K11	F_0
10	B02	A_9	44	K10	C_0
11	A02	A_{10}	45	L10	S_0
12	B03	A_{11}	46	K09	S_1
13	A03	A_{12}	47	L09	S_2
14	B04	A_{13}	48	K08	OSA
15	A04	A_{14}	49	L08	OSB
16	B05	A_{15}	50	K07	FTAB
17	A05	CLK	51	L07	$\overline{ENB}$
18	B06	V_{CC}	52	K06	$\overline{ENA}$
19	A06	GND	53	L06	B_0
20	B07	C_{16}	54	K05	B_1
21	A07	$\overline{P}$	55	L05	B_2
22	B08	$\overline{G}$	56	K04	B_3
23	A08	ZERO	57	L04	B_4
24	B09	OVF	58	K03	B_5
25	A09	$\overline{ENF}$	59	L03	B_6
26	A10	FTF	60	L02	B_7
27	B10	$\overline{OE}$	61	K02	B_8
28	B11	F_{15}	62	K01	B_9
29	C10	F_{14}	63	J02	B_{10}
30	C11	F_{13}	64	J01	B_{11}
31	D10	F_{12}	65	H02	B_{12}
32	D11	F_{11}	66	H01	B_{13}
33	E10	F_{10}	67	G02	B_{14}
34	E11	F_9	68	G01	B_{15}

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Features

- Four-wide 2901 ALU plus carry look-ahead logic and full 16-bit data paths
- High speed, low power CMOS technology
- Fast: 35 ns Commercial, 45 ns Military clock period
- Available 100% screened to MIL-STD-883, Class B
- Functionally equivalent to Am29C101 from AMD and to similar IDT and Cypress devices
- Package styles available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The **L29C101** is a high- performance, expandable, 16-bit Arithmetic Logic Unit slice manufactured using CMOS technology. Completely code compatible with its 4-bit predecessors, the part can be used to implement the arithmetic section of central processors or many types of programmable controllers.

The microinstruction set of the L29C101 is straightforward, yet versatile enough so that the part can be used to emulate the ALU operations of most digital computers.

The L29C101 is comprised of functions equivalent to four 2901 bit-slice ALU's plus the 2902 carry-look-ahead logic, all in a single 64-pin device. Included are a 16-word by 16-bit dual-port register file, a 16-bit 8-function ALU, 16-bit shifters, and all the necessary decoding and control logic.

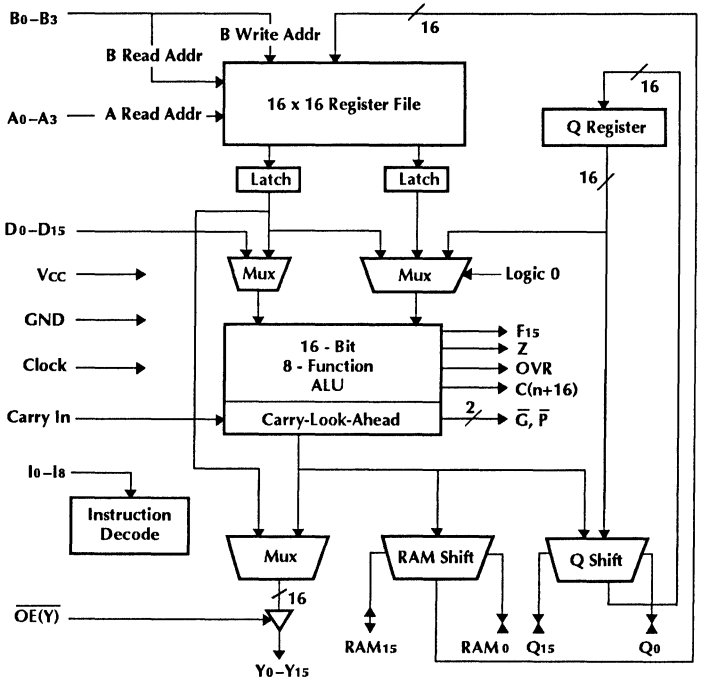
All status, shift linkage, and carry functions are cascadable to allow construction of architectures wider than 16-bits if desired. Expanded designs can take advantage of full carry-look-ahead for improved performance.

The L29C101 is fully pin and function compatible with the Am29C101.

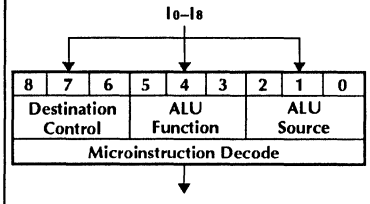
The L29C101 is available in High-Rel versions that are fully compliant with MIL-STD-883C, class B.

3

L29C101 Block Diagram



L29C101 Instruction Decoding

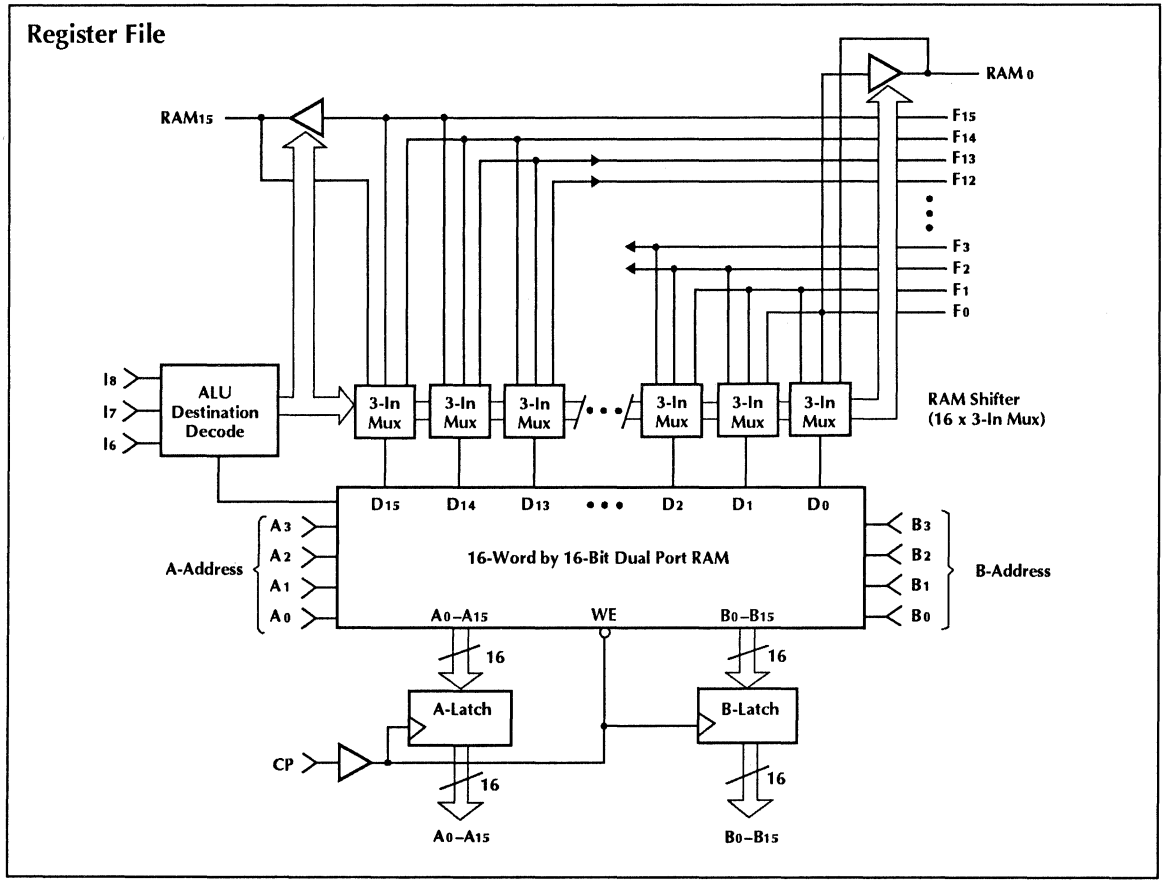


L29C101 Architecture

A typical execution cycle for the L29C101 consists of reading two operands simultaneously from the two-port register file, performing an ALU operation on these operands, and returning the result to the file. This entire operation can be completed in a single clock cycle, providing high performance and simple microcode. Optionally, the ALU operands may be sourced by the external data port, an auxiliary register denoted the Quotient or "Q" register, or forced to zero under instruction control. Also, the data returned to the register file and the Q register may be shifted one bit in either direction to aid multiplication and division operations.

Register File

The two-port register file has a capacity of 16 words of 16 bits each. The A-port address (A_0–A_3) specifies the register to be read from the A-port, and the B-port address (B_0–B_3) specifies the register to the read from the B-port. Both A and B addresses may be the same, in which case identical data will appear at both A and B ports. In addition, the B-port address can specify a register location for writing. Data from the locations indicated by the A and B addresses are read from the register file during the low period of the clock. The data is applied to two latches which are transparent during the clock low period, and hold their state during the clock high period. The purpose of these latches is to hold the A and B ALU operands constant while a computation result is written back to the register file at the B address. This allows for a read-modify-write cycle, which is useful in applications such as accumulation. Under control of the Result Destination Field (I_6, I_8), data to be written to the register file is stored into the register addressed by the B field on the rising edge of the clock.



ALU Control

The ALU is capable of performing eight operations. These functions are described in Table 2. The control inputs I_3–I_5 select one of three arithmetic or five logical operations to be performed on the input operands. The integral carry-lookahead circuitry across all 16 ALU bits is functionally equivalent to the 2902 carry-lookahead unit and provides significant speed advantages.

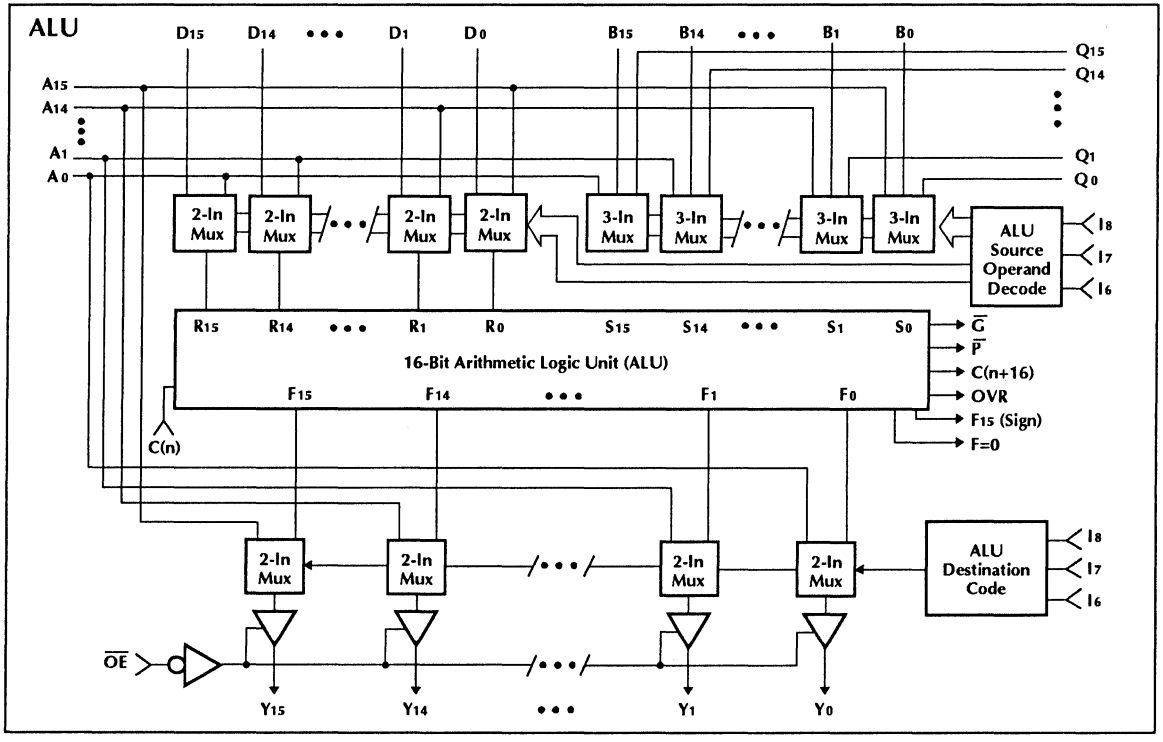
In the arithmetic mode, the ALU result is also a function of the Carry In input. When executing ALU Add or Subtract instructions, setting the C(n) input to '1' causes the addition of '1' to the result. Thus for 2's complement operations, C(n) of the least significant slice would be set to zero for addition, and to '1' for subtraction. This is because the L29C101 ALU naturally implements 1's complement subtraction, that is, a bitwise complement of one of the operands. In order to achieve a 2's complement result, a '1' must be added in the least significant position. This is accomplished using C(n). PASS and Negate operations are also available by combining arithmetic instructions (Add, Subtract) with any of the operand source options which set one operand to zero. Tables 5 and 6 show the detailed ALU logic and arithmetic functions and the operands selected. Table 5 includes ALU function selection.

Operand Source Control

As shown in the figure below, each of the ALU operands is supplied by a multiplexer, which allows significant flexibility in the selection of the operand source. The two 16-bit ALU inputs are denoted R and S. The R operand may be sourced by the A read port of the register file, from the D input pins, or may be forced to zero. The S operand may be sourced by the B read port of the register file, the A read port, (when the R operand is D or zero), the Q register, or forced to zero. Control of the operand selection multiplexers is encoded into control field I_2–I_0, as described in Table 1.

Result Destination Control

The instruction field I_6–I_8 is encoded to control the routing of the ALU result field, denoted F, and the Q register contents. The encoding is defined in Table 3. Under instruction control, the ALU result can be stored in the register file, the Q register, or both. A No Operation capability is also provided during which the result is not stored in either location. This field also controls the value presented at the Y_0–Y_{15} outputs. These outputs generally reflect the ALU result F, but for one of the instruction decodes are



driven by the A port value read from the register file. This provides the capability to read data from the register file while simultaneously performing an ALU operation. This is useful in applications such as postincrement address generation, for example.

In addition to destination control, up or down shifting of both the register file and Q register load values are controlled by the I6–I8 field. Each can be up or down shifted one position prior to storing in the destination register. The RAM0 or Q0 pins output the least significant bit of the value being stored for downshifts, and accept the bit to be stored in the least signficant position for upshifts. Similarly, the RAM15 or Q15 pins output the most significant bit for upshifts, and accept the bit to be stored in the most significant position for downshifts. Table 3 gives the various shift actions and data destinations controlled by the I6–I8 inputs.

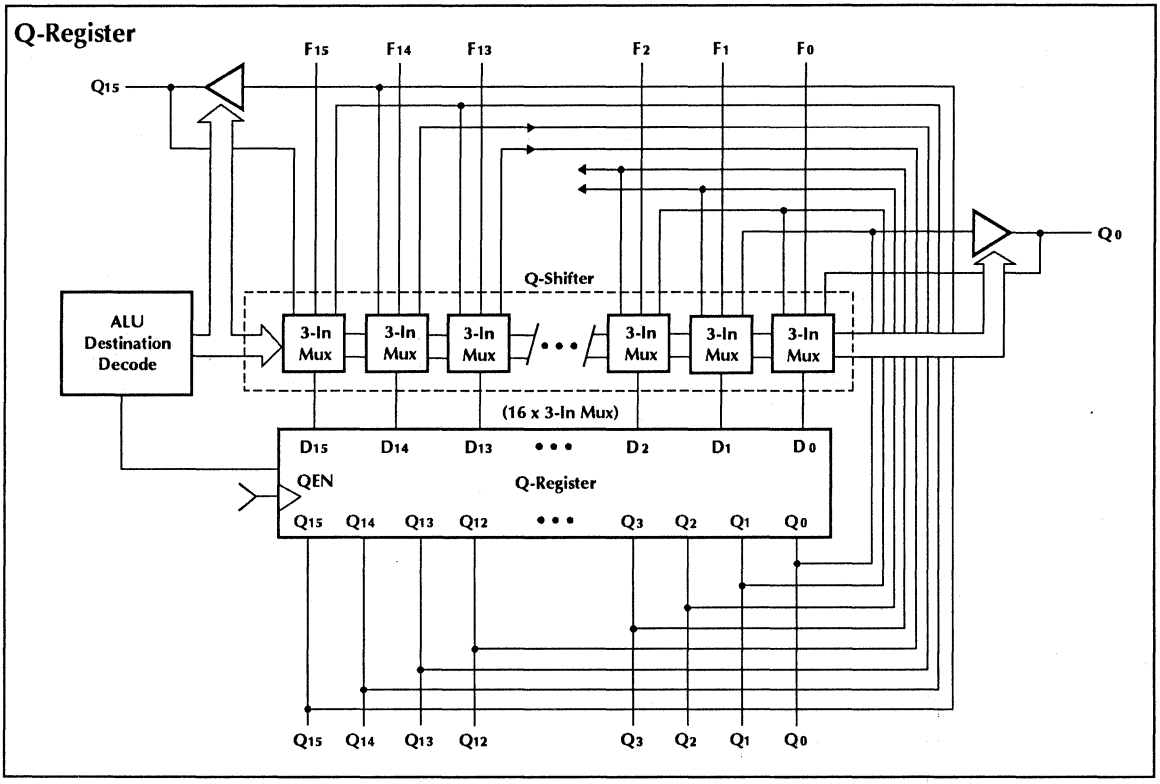
Q-Register

The Q-register is intended primarily for use as a separate working register for multiplication and division routines but it also serves as an accumulator or for temporary storage. The Q register is loaded via a multiplexer, which allows either up or downshift of the Q register contents, or an unshifted load of the Q register with the ALU result.

Status Outputs

The $\overline{G}$ and $\overline{P}$ outputs are low-true Carry Generate and Carry Propagate signals. They are used in conjunction with an external carry-lookahead generator when cascading L29C101 slices beyond 32 bits. The C(n+16) is the Carry Out signal, which can be directly connected to the C(n) input of another L29C101 to implement a 32-bit system. The OVR output indicates 2's complement overflow for addition and subtraction. The logical definitions of the $\overline{G}$, $\overline{P}$, C(n+16), and OVR signals are given in Table 7.

The MSB of the ALU result (F15) is provided so that the sign bit may be examined easily. The Z output is used for zero detection and is high when all of the F output bits are low. It is an open drain output which may be wire OR'ed across multiple slices.



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125° C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

Table 1. ALU Source Operand Control

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	$\overline{R}$ OR S	
AND	H	L	L	4	R AND S	
NOTRS	H	L	H	5	R AND S	
EXOR	H	H	L	6	R EX-OR S	
EXNOR	H	H	H	7	R EX-NOR S	

Table 3. ALU Destination Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_{15}	X	Q_{15}

Table 4. Source Operand and ALU Function Matrix

	I210 Octal	0	1	2	3	4	5	6	7
Octal I543	ALU Source / ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C(n) = L R plus S C(n) = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C(n) = L S minus R C(n) = H	Q – A – 1 Q – A	B – A – 1 B – A	Q – 1 Q	B – 1 B	A – 1 A	A – D – 1 A – D	Q – D – 1 Q – D	– D – 1 – D
2	C(n) = L R minus S C(n) = H	A – Q – 1 A – Q	A – B – 1 A – B	– Q – 1 – Q	– B – 1 – B	– A – 1 – A	D – A – 1 D – A	D – Q – 1 D – Q	D – 1 D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	$\overline{A}$∧Q	0	0	0	$\overline{D}$∧A	$\overline{D}$∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	A∧B	Q	B	A	D∧A	D∧Q	0
6	R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

Table 5. ALU Logic Mode Functions

Octal I543, I210	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee A$
60	EX – OR	$A \forall Q$
61		$A \forall B$
65		$D \forall A$
66		$D \forall Q$
70	EX – NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{R}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	ZERO	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I543, I210	C(n) = 0 (Low)		C(n) = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD Plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q – 1	PASS	Q
13		B – 1		B
14		A – 1		A
27		D – 1		D
22	1's Comp.	– Q – 1	2's Comp. (Negate)	– Q
23		– B – 1		– B
24		– A – 1		– A
17		– D – 1		– D
10	Subtract (1's Comp.)	Q – A – 1	Subtract (2's Comp.)	Q – A
11		B – A – 1		B – A
15		A – D – 1		A – D
16		Q – D – 1		Q – D
20		A – Q – 1		A – Q
21		A – B – 1		A – B
25		D – A – 1		D – A
26		D – Q – 1		D – Q

Table 7. Logic Functions for Carry and Overflow Conditions

I_{543}	Function	P	G	C(n+16)	OVR
0	R + S	$\overline{P_0 \bullet P_1 \cdots P_{15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots}$	C_{16}	$C_{16} \forall C_{15}$
1	S – R	← Same as R + S equations, but substitute $\overline{R_i}$ for Ri in definitions →			
2	R – S	← Same as R + S equations, but substitute $\overline{S_i}$ for Si in definitions →			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$R \wedge S$				
6	$\overline{R} \forall S$				
7	$\overline{R \forall S}$				

3

Switching Characteristics
Over Commercial Operating Range (Note 9)

Output Enable/Disable Times (Note 11)

Device	Input	Output	t_{EN}	t_{DIS}
L29C101–35	$\overline{OE}$	Y	20	17

Cycle Time and Clock Characteristics

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	35 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	30 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	20 ns

Combinational Propagation Delays (Note 12)

To Output / From Input	Y	F_{15}	C(n+16)	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}
A,B Address	46	43	35	37	49	41	40	—
D	34	34	27	27	40	29	33	—
C(n)	27	24	20	—	28	23	28	—
I_0, I_1, I_2	40	40	33	30	42	32	35	—
I_3, I_4, I_5	41	38	32	28	40	36	38	—
I_6, I_7, I_8	20	—	—	—	—	—	26	26
A bypass ALU (I = 2XX)	26	—	—	—	—	—	—	—
Clock	38	34	30	30	36	32	34	25

Set-Up and Hold Times Relative to Clock Input (Note 12)

Input	Setup Time Before H→L	Hold Time After H→L	Setup Time Before L→H	Hold Time After L→H
A,B Source Address (Note 14, 15)	24	3	35	—
B Destination Address (Note 13)	24	←Do Not Change→		0
D	—	—	26	0
C(n)	—	—	16	0
I_0, I_1, I_2	—	—	30	0
I_3, I_4, I_5	—	—	31	0
I_6, I_7, I_8 (Note 13)	10	←Do Not Change→		0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	12	0

Switching Characteristics
Over Military Operating Range (Note 9)

Output Enable/Disable Times (Note 11)

Device	Input	Output	tEN	tDIS
L29C101–45	$\overline{OE}$	Y	23	20

Cycle Time and Clock Characteristics

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	25 MHz
Minimum Clock LOW Time	20 ns
Minimum Clock HIGH Time	20 ns

3

Combinational Propagation Delays (Note 12)

To Output / From Input	Y	F15	C(n+16)	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM15	Q0 Q15
A,B Address	52	50	40	38	48	46	43	—
D	37	36	30	32	40	32	35	—
C(n)	30	28	24	—	29	27	30	—
I0, I1, I2	44	43	36	34	46	38	41	—
I3, I4, I5	47	44	35	35	45	44	45	—
I6, I7, I8	22	—	—	—	—	—	30	30
A bypass ALU (I = 2XX)	27	—	—	—	—	—	—	—
Clock	44	39	32	32	40	36	34	28

Set-Up and Hold Times Relative to Clock Input (Note 12)

Input	Setup Time Before H→L	Hold Time After H→L	Setup Time Before L→H	Hold Time After L→H
A,B Source Address (Note 14, 15)	22	3	40	—
B Destination Address (Note 13)	22	←Do Not Change→		0
D	—	—	30	0
C(n)	—	—	20	0
I0, I1, I2	—	—	37	0
I3, I4, I5	—	—	36	0
I6, I7, I8 (Note 13)	10	←Do Not Change→		0
RAM0, RAM15, Q0, Q15	—	—	12	2

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 volts. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turnon/turnoff times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition for t_{EN} is measured ±200 mV from steady-state voltage with specified loading.

12. A dash indicates a propagation delay or set-up time constraint that does not exist.

13. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

14. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.

15. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance 35 ns
L29C101	
64-pin Plastic DIP (0.9") — P4	L29C101PC35
64-pin Sidebraze (0.9") Hermetic DIP — D4	L29C101DC35
68-pin Ceramic LCC — K3	L29C101KC35
68-pin Pin Grid Array — G1	L29C101GC35

Military Operating Range (–55°C to +125°C)

Package Style	Performance 45 ns
L29C101	
64-pin Sidebraze (0.9") Hermetic DIP — D4	L29C101DM45 L29C101DME45 L29C101DMB45
68-pin Ceramic LCC — K3	L29C101KM45 L29C101KME45 L29C101KMB45
68-pin Pin Grid Array — G1	L29C101GM45 L29C101GME45 L29C101GMB45

Pin Assignments

Pin	Function	Pin	Function
1	I_4	33	I_6
2	I_5	34	Q_0
3	$\overline{P}$	35	RAM_0
4	$\overline{G}$	36	CP
5	C(n+16)	37	B_3
6	OVR	38	B_2
7	F_{15}	39	B_1
8	Y_{15}	40	B_0
9	Y_{14}	41	D_0
10	Y_{13}	42	D_1
11	Y_{12}	43	D_2
12	Y_{11}	44	D_3
13	Y_{10}	45	D_4
14	Y_9	46	D_5
15	Y_8	47	D_6
16	GND	48	D_7
17	$\overline{OE}$	49	V_{CC}
18	Y_7	50	D_8
19	Y_6	51	D_9
20	Y_5	52	D_{10}
21	Y_4	53	D_{11}
22	Y_3	54	D_{12}
23	Y_2	55	D_{13}
24	Y_1	56	D_{14}
25	Y_0	57	D_{15}
26	F=0	58	A_0
27	C_{IN}	59	A_1
28	I_2	60	A_2
29	I_1	61	A_3
30	I_0	62	RAM_{15}
31	I_8	63	Q_{15}
32	I_7	64	I_3

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LOGIC DEVICES INCORPORATED

32-bit Cascadable Barrel Shifter LSH32

Features

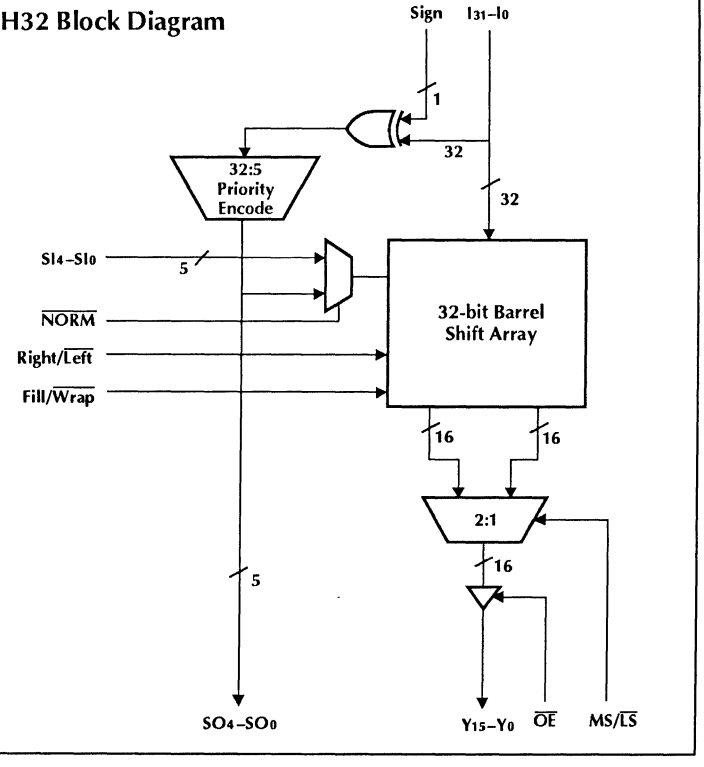
- 32-bit input, 32-bit output multiplexed to 16 lines
- Full 0–31 position barrel shift capability
- Integral priority encoder for 32-bit floating point normalization
- Sign-magnitude or two's complement mantissa representation
- 32-bit linear shifts with sign or zero fill
- Independent priority encoder outputs for block floating point
- Package styles available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC (Type C)
  - 68-pin Pin Grid Array

Description

The **LSH32** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

The major features of the LSH32 architecture are discussed in the following paragraphs.

LSH32 Block Diagram



Shift Array

The 32 inputs to the LSH32 are applied to a 32-bit shift array. The 32 outputs of this array are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH32 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH32 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the Right/$\overline{\text{Left}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

Table 1. Wrap mode shift code definitions

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	I_{31}
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	I_{29}	I_{30}
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•	I_0	I_{31}	•	•	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_{13}	I_{12}	I_1	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	I_2	I_1	I_0	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	I_1	I_0	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	I_0	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 2. Fill mode shift code definitions (Left shift)

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	0
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	0	0
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	0	0
10000	I_{15}	I_{14}	I_{13}	•	I_0	0	•	•	0	0
10001	I_{14}	I_{13}	I_{12}	•	0	0	•	•	0	0
10010	I_{13}	I_{12}	I_{11}	•	0	0	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_3	I_2	I_1	•	0	0	•	•	0	0
11101	I_2	I_1	I_0	•	0	0	•	•	0	0
11110	I_1	I_0	0	•	0	0	•	•	0	0
11111	I_0	0	0	•	0	0	•	•	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH32 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

Output Multiplexer

The shift array outputs are applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

Priority Encoder

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs;

Table 3. Fill mode shift code definitions (Right shift)

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	S	S	•	•	S	S	•	•	S	S
00001	S	S	•	•	S	S	•	•	S	I_{31}
00010	S	S	•	•	S	S	•	•	I_{31}	I_{30}
00011	S	S	•	•	S	S	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	S	S	S	•	S	S	•	•	I_{18}	I_{17}
10000	S	S	S	•	S	I_{31}	•	•	I_{17}	I_{16}
10001	S	S	S	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	S	S	S	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	S	S	S	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	S	S	S	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	S	S	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	S	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 4. Priority encoder function table

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}	•••	I_0	Shift Code
1	X	X	•••	X	X	X	•••	X	00000
0	1	X	•••	X	X	X	•••	X	00001
0	0	1	•••	X	X	X	•••	X	00010
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	1	X	X	•••	X	01111
0	0	0	•••	0	1	X	•••	X	10000
0	0	0	•••	0	0	1	•••	X	10001
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	0	0	0	•••	1	11111
0	0	0	•••	0	0	0	•••	0	11111

the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

Normalize Multiplexer

The $\overline{\text{NORM}}$ input, when asserted results in the priority encoder output driving the internal shift code inputs directly. It is exactly equivalent to routing the SO_4–SO_0 outputs back to the SI_4–SI_0 inputs. The $\overline{\text{NORM}}$ input provides faster normalization of 32-bit data by avoiding the delay associated with routing the shift code off chip. When using the $\overline{\text{NORM}}$ function, the LSH32 should be placed in fill mode, with the R/$\overline{\text{L}}$ input low.

Applications Examples

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH32. The $\overline{\text{NORM}}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{\text{LS}}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH32 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{\text{LS}}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

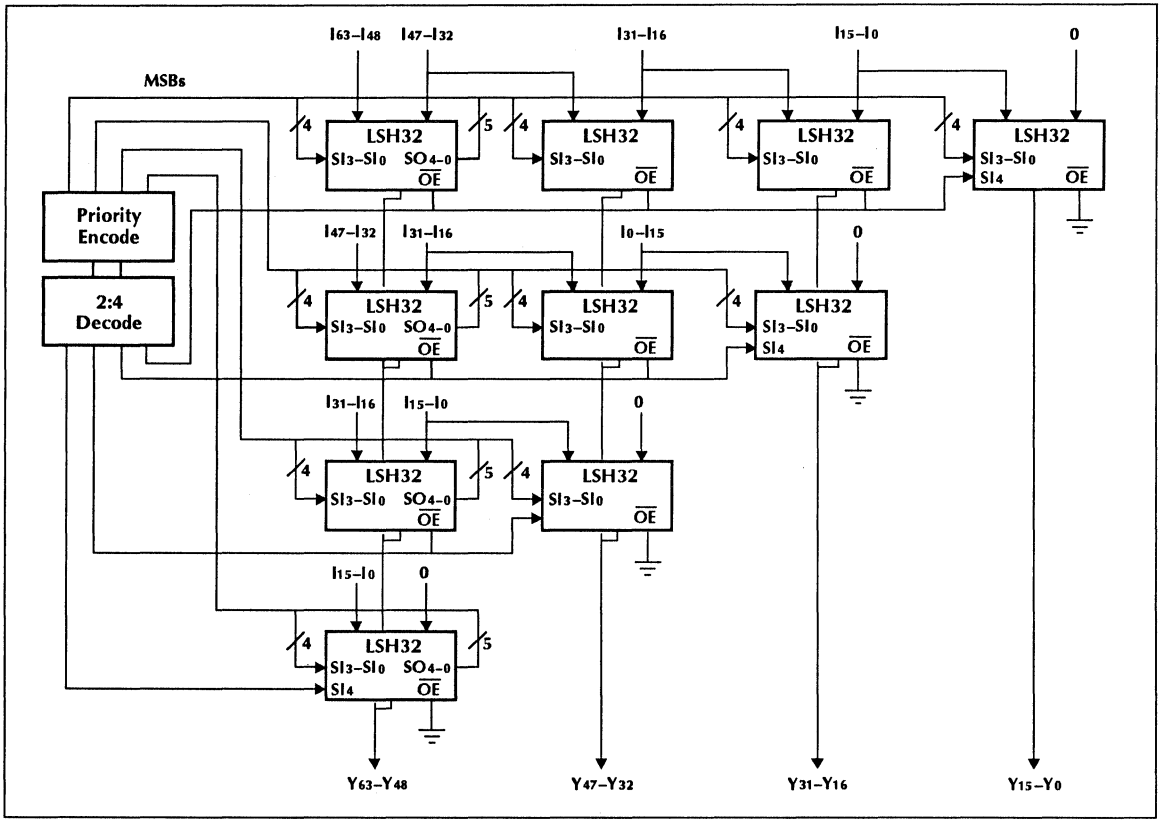
Long-Word Normalization (Multiple Cycles)

Normalization of floating point mantissas longer than 32 bits can be accomplished by cascading LSH32 units. When cascading for normalization, the device inputs are overlapped such that each device lower in priority than the first shares 16 inputs with its more significant neighbor. Fill mode and left shift are selected, however, internal normalization ($\overline{NORM}$) is not used. The most significant result half of each device is enabled to the output. The shift out (SO_4–SO_0) lines of the most significant slice are connected to the shift in lines of all slices, including the first. The exception is that all SI_4 lines are grounded, limiting the shift distance to 16 positions. The shift distance required for normalization is produced by the priority encoder in the most significant slice. The priority encoder will produce the shift code necessary to normalize the input word if the leading non-zero digit is found in the upper 16 bits. If this is the case, the number of shift positions necessary to accomplish normalization is placed on the SO_4–SO_0 outputs for use by all slices, and the appropriate 0–15 bit shift is accomplished. If the upper 16 bits are all zero, then the maximum shift of 15 places is executed. Single clock normalization requiring shifts longer than 16 bits can be accomplished by a bank-select technique described below.

Single Cycle Long-Word Normalization

An extension of the above concept is a single clock normalization of long words (potentially requiring shifts of more than 15 places). The arrangement of LSH32s required is shown in Figure 1. Cascading of LSH32 units is accomplished by connecting the SI_3–SI_0 input lines of each unit to the SO_3–SO_0 outputs of the most significant device in the row as before. Essentially the LSH32s are arranged in multiple rows or banks such that the

Figure 1. Single cycle long-word normalization using LSH32s



inputs to successive rows are left-shifted by 16 positions. The outputs of each row are multiplexed onto a three-state bus. The normalization problem then reduces to selecting from among the several banks that one which has the first non-zero bit of the input value among its 16 most significant positions. If the most significant one in the input file was within the upper 16 locations of a given bank, the SO_4 output of the most significant slice in that bank will be low. Single clock normalization can thus be accomplished simply by enabling onto the three-state output bus the highest priority bank in which this condition is met. In this way the input word will be normalized regardless of the number of shift positions required to accomplish this. The number of shift positions can be determined simply by concatenation of the SO_3–SO_0 outputs of the most significant slice in the selected row with the encoded Output Enable-bits determining the row number. Note that lower rows need not be fully populated. This is because they represent left shifts in multiples of 16 positions, and the lower bits of the output word will be zero filled. In order to accomplish this zero fill, the least significant device in each row is always enabled, and the row select is instead connected to the SI_4 input. This will force the shift length of the least significant device to a value greater than 15 whenever the row containing that device is not selected. This results in zero fill being accomplished by the equivalently positioned slice in a higher bank, as shown in the diagram.

Block Floating Point

With a small amount of external logic, block floating point operations are easily accomplished by the LSH32. Data resulting from a vector operation are applied to the LSH32 with the $\overline{NORM}$-input deasserted. The SO_4–SO_0 outputs fill then represent the normalization shift distance for each vector element in turn. By use of an external latch and comparator, the maximum shift distance encountered across all elements in the vector is saved for use in the next block operation (or block normalization). During this subsequent pass through the data, the shift code saved from the previous pass is applied uniformly across all elements of the vector. Since the LSH32 is not used in the internal normalize mode, this operation can be pipelined, thereby obtaining the desired shift distance for the next pass while simultaneously applying the normalization required from the previous pass.

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 150 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3			0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8	–20		–100	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

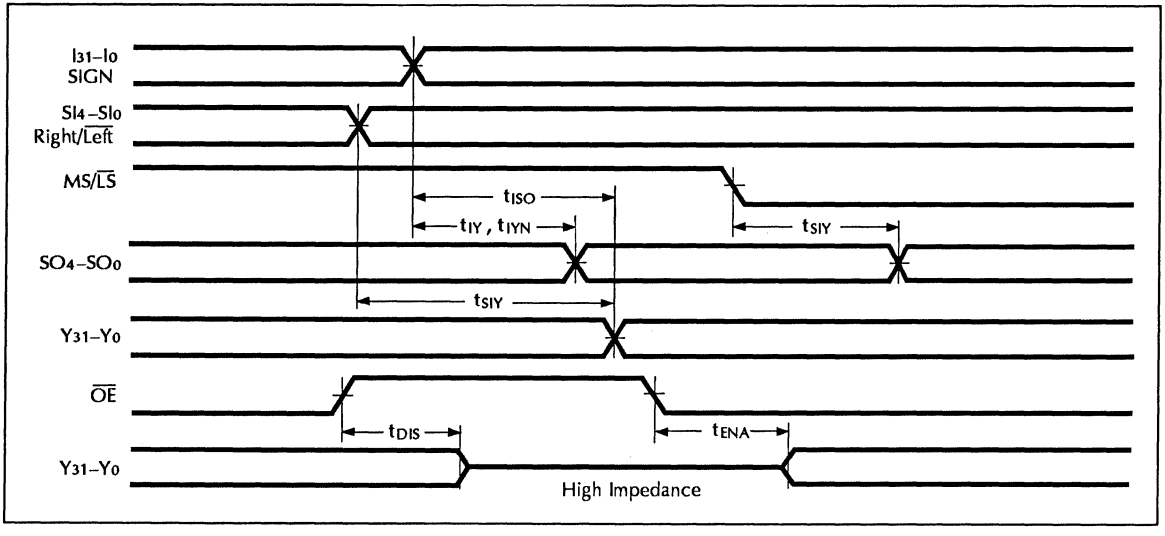
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LSH32-42		LSH32-32	
		Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		42		32
t_{ISO}	I, SIGN Inputs to SO Outputs		55		42
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		75		60
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		52		40
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		28		24
t_{DIS}	$\overline{\text{OE}}$ to Output Disable (Note 11)		20		20
t_{ENA}	$\overline{\text{OE}}$ to Output Enable (Note 11)		20		20

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LSH32-50		LSH32-40	
		Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		50		40
t_{ISO}	I, SIGN Inputs to SO Outputs		65		52
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		85		75
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		62		52
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		32		26
t_{DIS}	$\overline{\text{OE}}$ to Output Disable (Note 11)		22		20
t_{ENA}	$\overline{\text{OE}}$ to Output Enable (Note 11)		22		20

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance	
	42 ns	32 ns
LSH32		
68-pin Plastic LCC, J-Lead — J2	LSH32JC42	LSH32JC32
68-pin Pin Grid Array — G1	LSH32GC42	LSH32GC32
68-pin Ceramic LCC — K3	LSH32KC42	LSH32KC32

Military Operating Range (–55°C to +125°C)

Package Style	Performance	
	50 ns	40 ns
LSH32		
68-pin Pin Grid Array — G1	LSH32GM50 LSH32GME50	LSH32GM40 LSH32GME40
68-pin Ceramic LCC — K3	LSH32KM50 LSH32KME50	LSH32KM40 LSH32KME40

Pin Assignments

Pin J,K	Pin G	Function	Pin J,K	Pin G	Function
1	F02	I_{21}	35	F10	Y_{22}/Y_6
2	F01	I_{22}	36	F11	Y_{21}/Y_5
3	E02	I_{23}	37	G10	Y_{20}/Y_4
4	E01	I_{24}	38	G11	Y_{19}/Y_3
5	D02	I_{25}	39	H10	Y_{18}/Y_2
6	D01	I_{26}	40	H11	Y_{17}/Y_1
7	C02	I_{27}	41	J10	Y_{16}/Y_0
8	C01	I_{28}	42	J11	$\overline{OE}$
9	B01	I_{29}	43	K11	MS/$\overline{LS}$
10	B02	I_{30}	44	K10	V_{CC}
11	A02	I_{31}	45	L10	V_{CC}
12	B03	SIGN	46	K09	I_0
13	A03	SO_4	47	L09	I_1
14	B04	SO_3	48	K08	I_2
15	A04	SO_2	49	L08	I_3
16	B05	SO_1	50	K07	I_4
17	A05	SO_0	51	L07	I_5
18	B06	$\overline{NORM}$	52	K06	I_6
19	A06	SI_4	53	L06	I_7
20	B07	SI_3	54	K05	I_8
21	A07	SI_2	55	L05	I_9
22	B08	SI_1	56	K04	I_{10}
23	A08	SI_0	57	L04	I_{11}
24	B09	R/$\overline{L}$	58	K03	I_{12}
25	A09	F/$\overline{W}$	59	L03	I_{13}
26	A10	Y_{31}/Y_{15}	60	L02	GND
27	B10	Y_{30}/Y_{14}	61	K02	GND
28	B11	Y_{29}/Y_{13}	62	K01	I_{14}
29	C10	Y_{28}/Y_{12}	63	J02	I_{15}
30	C11	Y_{27}/Y_{11}	64	J01	I_{16}
31	D10	Y_{26}/Y_{10}	65	H02	I_{17}
32	D11	Y_{25}/Y_9	66	H01	I_{18}
33	E10	Y_{24}/Y_8	67	G02	I_{19}
34	E11	Y_{23}/Y_7	68	G01	I_{20}

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LOGIC DEVICES INCORPORATED

Features

- High-speed (50 MHz), low power (125 mW), CMOS 64-bit Digital Correlator
- Functionally and pin compatible with the TRW TDC1023J
- Bits can be selectively masked
- Three-state outputs
- Available 100% screended to MIL-STD-883, Class B
- Package styles available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC (Type C)

Description

The **L10C23** is a high speed CMOS 64-bit digital correlator. It is pin-for-pin equivalent to the TDC1023 bipolar correlator. The L10C23 operates over the full military ambient temperature range using advanced CMOS technology.

The L10C23 produces the 7-bit correlation score of two input words of up to 64 bits, denoted A and B. The A and B inputs are serially shifted into two independently clocked 64-bit registers. The A register is clocked on the rising edge of CLK A, and the B register is clocked on the rising edge of CLK B.

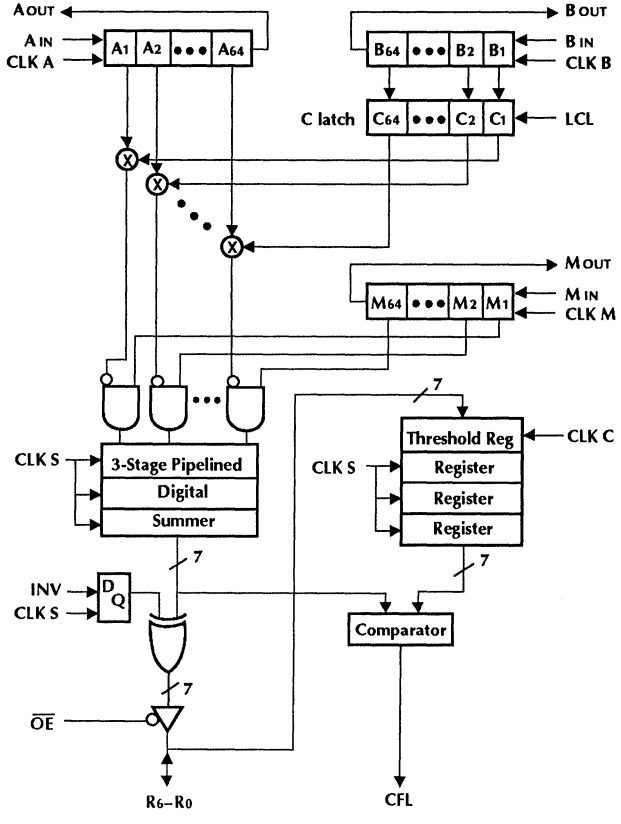
The outputs of the B register drive a 64-bit transparent latch, denoted the C latch. The C latch is controlled by the LCL (Load C Latch) input. A high level on the LCL input causes the C latch to be transparent, allowing the contents of the B register to be applied directly to the correlator array. When the LCL input is low, the data in the C latch is held, so that the B input may be loaded with a new correlation reference without affecting the current reference value stored in C.

Each bit in the A register is exclusive NOR'ed with the corresponding bit in the C latch, implementing a single bit multiplication at each bit position.

The mask register, denoted by M, is a third 64-bit register, which is serially loaded from the M input on the rising edge of CLK M. Bit positions in the M register which are set to zero mask the corresponding bits in the A and C registers from participating in the correlation score. This can be used to reduce the effective length of the correlation, or to correlate against only one channel of a bit-multiplexed datastream without deinterleaving the data.

The output of the masking process is a 64-bit vector which contains ones in the locations in which A and B data match, and which are unmasked (M register contains a 1). This 64-bit vector is applied to a pipelined digital summer which calculates the total number of ones in the vector (the correlation score). The summer network contains three pipeline stages, which

L10C23 Block Diagram



are clocked on the rising edge of CLK S. Calculation of a correlation score therefore requires three clock cycles, but a new result can be obtained on each cycle once the pipeline is filled.

Because a portion of the summer logic is located between the input registers and the first pipeline register, some timing restrictions exist between CLK S and CLK A, CLK B, or CLK M. CLK S may be tied to an input clock (usually CLK A) to obtain a continuously updated correlation score, delayed by three cycles from the data. Under this condition, CLK S may be skewed later than CLK A by no more than t_{SK} to assure that the A register outputs have not changed before the S clock occurs.

Alternatively, CLK S may be asynchronous to the input clocks, as long as data is stable at the pipeline register inputs prior to the CLK S rising edge. This condition can be met by assuring that CLK S occurs at least t_{PS} after the input clock.

The summer output represents a count of the number of matching positions in the input data streams. This 7-bit result can be inverted (one's-complemented) by loading a '1' into the INV register.

Correlation values which exceed a predetermined threshold can be detected via the Threshold register and Comparator. The Threshold register is loaded with a 7-bit value via the R_6–R_0 pins at the rising edge of CLK C and while $\overline{OE}$ is logic high. To achieve synchronization with the digital summer, the Threshold register contents are fed into pipeline registers clocked by CLK S. The compare flag output (CFL) goes high when the summer output is equal to or greater than the contents of the Threshold register.

Cascading the L10C23 devices for longer correlation lengths and more bits of reference or data precision is easily accomplished. The A, B, and M registers have serial outputs to directly drive the corresponding inputs of succeeding devices. The correlation scores of multiple devices in such a system should be added together to obtain the overall correlation score.

Correlation on data exceeding one bit of precision can be accomplished by first calculating single-bit correlation scores at each bit position, then adding the results after weighting them appropriately. Thus, one L10C23 would be used for each bit of precision in the data.

Logic Devices' L4C381 16-bit ALU can be used to assist in adding the outputs of several L10C23 correlators. When adding several 7-bit correlation scores, advantage can be taken of the fact that the sum of two 7-bit numbers will not exceed 8 bits. Thus the L4C381 can simultaneously perform *two* 7-bit additions. The first two operands are applied to A_6–A_0 and B_6–B_0, with the result appearing on F_7–F_0. The second pair of operands are applied to A_{14}–A_8 and B_{14}–B_8, with the result appearing in F_{15}–F_8. The unused inputs are tied to ground. If it can be guaranteed that at least one of the input scores will not reach its maximum value of 64, then this technique can also be applied in the second tier of adders. In this case, while the inputs have 8 bits of precision, the maximum value their sum can assume is 255, which is expressable in 8 bits.

Alternatively, when performing long correlations on relatively slow datastreams, one L4C381 can be configured using its feedback mode to accumulate the correlation scores of a number of L10C23s. To accomplish this, the outputs of all the correlators are tied together on a three-state bus. Each one is sequentially enabled and clocked into the L4C381, which accumulates the total resulting score.

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		25	100	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			0.5	mA

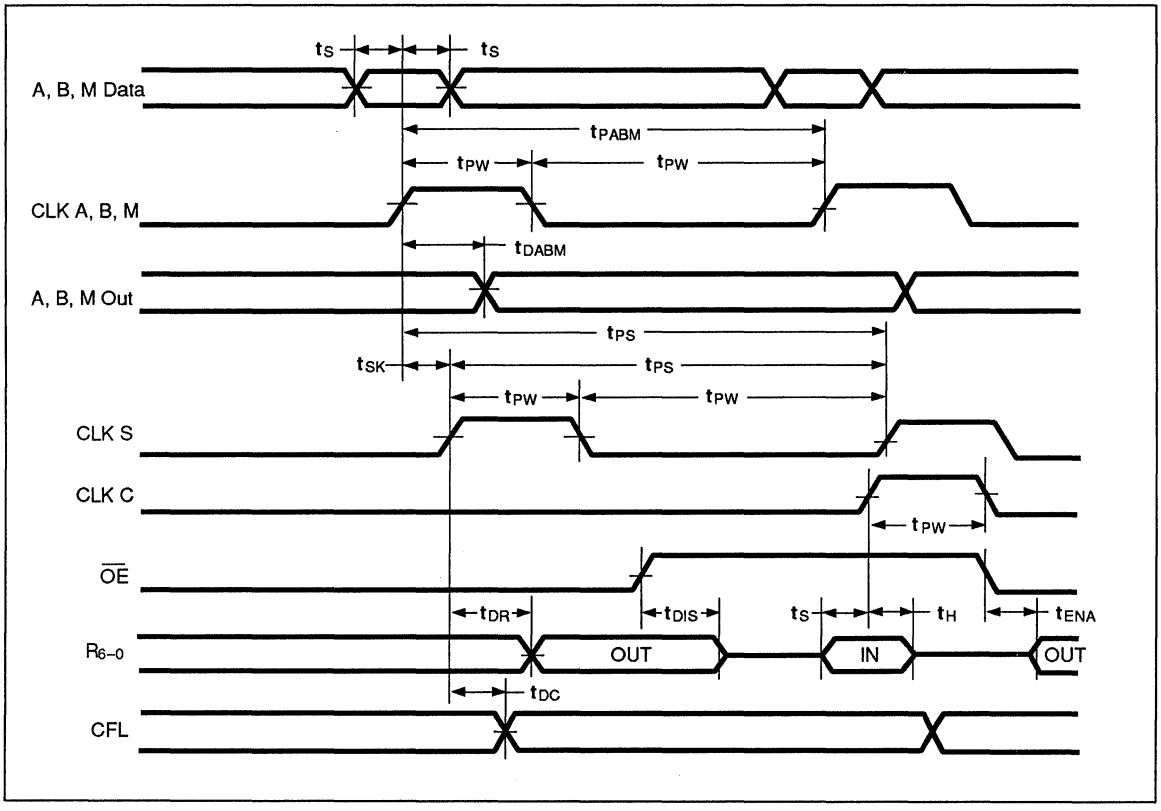
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	L10C23-50		L10C23-30		L10C23-20	
		Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	50		28		20	
t_S	Input Data Setup Time	20		8		8	
t_H	Input Data Hold Time	0		0		0	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		12		8	
t_{DABM}	A, B, M Clock to A, B, M Out		25		20		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	50		28		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_6–R_0		35		30		22
t_{DC}	S Clock to CFL		25		20		18
t_{DIS}	Output Disable Time (Note 11)		35		16		14
t_{ENA}	Output Enable Time (Note 11)		30		18		16

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	L10C23-60		L10C23-35		L10C23-20	
		Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	58		33		20	
t_S	Input Data Setup Time	22		10		10	
t_H	Input Data Hold Time	0		0		0	
t_{PW}	A, B, M, S Clock Pulse Width	20		14		8	
t_{DABM}	A, B, M Clock to A, B, M Out		30		23		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	58		33		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_6–R_0		40		35		25
t_{DC}	S Clock to CFL		30		23		18
t_{DIS}	Output Disable Time (Note 11)		40		18		16
t_{ENA}	Output Enable Time (Note 11)		35		20		18

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance		
	50 ns	30 ns	20 ns
24-pin Plastic DIP (0.3") — P2	L10C23NC50	L10C23NC30	L10C23NC20
24-pin Plastic DIP (0.6") — P1	L10C23PC50	L10C23PC30	L10C23PC20
24-pin Sidebraze (0.3") Hermetic DIP — D2	L10C23HC50	L10C23HC30	L10C23HC20
24-pin Sidebraze (0.6") Hermetic DIP — D1	L10C23DC50	L10C23DC30	L10C23DC20

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Military Operating Range (–55°C to +125°C)

Package Style	Performance		
	60 ns	35 ns	20 ns
24-pin Sidebraze (0.3") Hermetic DIP — D2	L10C23HM60 L10C23HME60 L10C23HMB60	L10C23HM35 L10C23HME35 L10C23HMB35	L10C23HM20 L10C23HME20 L10C23HMB20
24-pin Sidebraze (0.6") Hermetic DIP — D1	L10C23DM60 L10C23DME60 L10C23DMB60	L10C23DM35 L10C23DME35 L10C23DMB35	L10C23DM20 L10C23DME20 L10C23DMB20
24-pin Ceramic LCC — K1	L10C23KM60 L10C23KME60 L10C23KMB60	L10C23KM35 L10C23KME35 L10C23KMB35	L10C23KM20 L10C23KME20 L10C23KMB20

Pin Assignments

Pin			Pin		
P,D,H	K	Function	P,D,H	K	Function
1	1,2	V_{CC}	13	14	R_2
2	3	M IN	14	16	R_1
3	4	A IN	15	17	R_0
4	6	B IN	16	19,20	GND
5	7	CLK C	17	21	CFL
6	8	CLK S	18	22	B OUT
7	9	INV	19	23	A OUT
8	10	$\overline{OE}$	20	24	M OUT
9	11	R_6	21	25	LCL
10	12	R_5	22	26	CLK A
11	13	R_4	23	27	CLK M
12	14	R_3	24	28	CLK B
				5	*NC*
				18	*NC*

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LOGIC DEVICES INCORPORATED

Contents

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Product Selection /Cross Reference Guide

Product Selection

Part No.	Description	Speed (ns) Com.	Speed (ns) Mil.	Power (mW)	Pins	Packages Available
L5380	SCSI Controller	4 Mbytes/s	2 Mbytes/s	50	40/44	DIP, PLCC
L53C80	SCSI Controller	4 Mbytes/s	2 Mbytes/s	50	48/44	DIP, PLCC

Product Cross Reference

LOGIC DEVICES		AMD	NCR	National
L5380	SCSI	AM5380	NCR5380 NCR5380-40	DP5380
L53C80	SCSI	AM53C80	NCR53C80	

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Features

- Asyncronous transfer rate up to 4 Mbytes/sec
- Pin and functionally compatible with NCR5380, but 2.5× faster
- Low-power CMOS technology
- On-chip SCSI bus drivers
- Supports arbitration, selection/re-selection, initiator or target roles
- Programmed or DMA I/O, handshake or wait state DMA interlock
- Package styles available:
  - 40/48-pin Plastic DIP
  - 40/48-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead

Description

The **L5380/ L53C80** are very high performance CMOS controllers which support the physical layer of the SCSI (Small Computer System Interface) bus as defined by the ANSI X3T9.2 committee. It is pin and functionally compatible with the NMOS NCR5380, while offering up to a 2.5× performance improvement, 10× power reduction, and lower cost. Replacement of the NMOS 5380 by the LOGIC Devices L5380/L53C80 will result in an immediate transfer rate improvement due to $\overline{REQ}/\overline{ACK}$ and DRQ/$\overline{DACK}$ handshake response times up to 5 times faster than previous devices.

While remaining firmware compatible with the NCR5380, the L5380/L53C80 provides bug fixes and state machine enhancements allowing even larger throughput gains for new designs.

The L5380/L53C80 supports asyncronous data transfer between initiator and target at up to 4 Mbytes/sec. It operates in either initiator or target roles, and offers a choice of programmed I/O (direct microprocessor manipulation of handshake) or any of several DMA modes (autonomous handshake and data transfer operations). The L5380/L53C80 has

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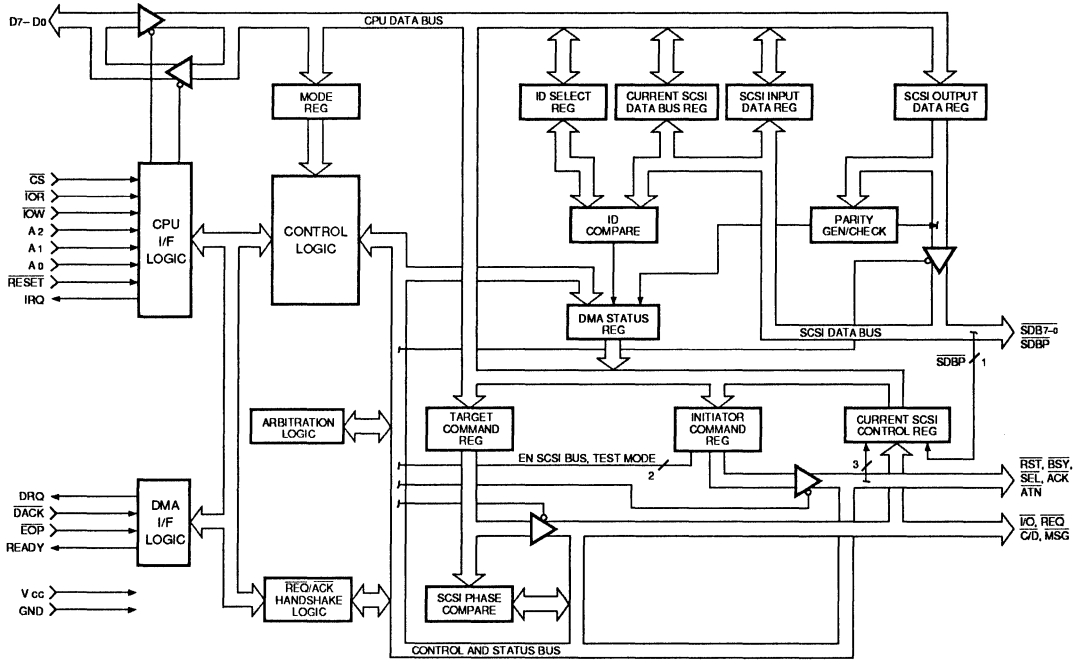
L5380/L53C80 Function Diagram



internal hardware to support arbitration, and can monitor and generate interrupts for a variety of error conditions. It provides extensive bus status monitoring features, and includes buffers capable of directly driving a terminated SCSI bus for a compact implementation.

PIN DEFINITION

A. SCSI Bus

$\overline{SDB}_{7-0}$ — SCSI DATA BUS 7–0: Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. $\overline{SDB7}$ is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; $\overline{SDB7}$ represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

$\overline{SDBP}$ — SCSI DATA BUS PARITY: Bidirectional/Active low. $\overline{SDBP}$ is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

$\overline{SEL}$ — SELECT: Bidirectional/Active low. $\overline{SEL}$ is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

$\overline{BSY}$ — BUSY: Bidirectional/Active low. $\overline{BSY}$ is asserted to indicate that the SCSI bus is active.

$\overline{ACK}$ — ACKNOWLEDGE: Bidirectional/Active low. $\overline{ACK}$ is asserted by the initiator, during any information transfer phase, in response to assertion of $\overline{REQ}$ by the target. Similarly, $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of $\overline{ACK}$ for target receive operations.

$\overline{ATN}$ — ATTENTION: Bidirectional/Active low. $\overline{ATN}$ is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to $\overline{ATN}$ by entering the MESSAGE OUT phase.

Pin Assignments

L5380 Pin Assignment

Pin P,D	Pin J,K	Function	Pin P,D	Pin J,K	Function
1	2	D0	23	26	$\overline{IRQ}$
2	3	$\overline{SDB7}$	24	27	$\overline{IOR}$
3	4	$\overline{SDB6}$	25	28	READY
4	5	$\overline{SDB5}$	26	29	$\overline{DACK}$
5	6	$\overline{SDB4}$	27	30	$\overline{EOP}$
6	7	$\overline{SDB3}$	28	31	$\overline{RESET}$
7	8	$\overline{SDB2}$	29	32	$\overline{IOW}$
8	9	$\overline{SDB1}$	30	33	A0
9	10	$\overline{SDB0}$	31	35	Vcc
10	11	$\overline{SDBP}$	32	36	A1
11	12	GND	33	37	A2
12	14	$\overline{SEL}$	34	38	D7
13	15	$\overline{BSY}$	35	39	D6
14	16	$\overline{ACK}$	36	40	D5
15	17	$\overline{ATN}$	37	41	D4
16	18	$\overline{RST}$	38	42	D3
17	19	$\overline{I/O}$	39	43	D2
18	20	$\overline{C/D}$	40	44	D1
19	21	$\overline{MSG}$		13	GND
20	22	$\overline{REQ}$		1	*NC*
21	24	$\overline{CS}$		23	*NC*
22	25	DRQ		34	*NC*

P,D = L5380PC
L5380DC

J,K = L5380JC
L5380KC

L53C80 Pin Assignment

Pin P,D	Pin J,K	Function	Pin P,D	Pin J,K	Function
1	1	$\overline{SDB7}$	27	25	D3
2	2	$\overline{RST}$	28	26	D2
3	3	GND	29	27	D1
4	4	$\overline{BSY}$	30	28	D0
5	5	$\overline{SEL}$	32	29	$\overline{MSG}$
6	6	$\overline{ATN}$	33	30	$\overline{C/D}$
8	7	$\overline{RESET}$	34	31	GND
9	8	IRQ	35	32	$\overline{I/O}$
10	9	DRQ	36	33	$\overline{ACK}$
11	10	$\overline{EOP}$	37	34	$\overline{REQ}$
12	11	$\overline{DACK}$	38	35	$\overline{SDBP}$
13	12	GND	39	36	GND
14	13	READY	40	37	$\overline{SDB0}$
15	14	A0	41	38	$\overline{SDB1}$
16	15	A1	43	39	$\overline{SDB2}$
17	16	A2	44	40	$\overline{SDB3}$
19	17	$\overline{CS}$	45	41	$\overline{SDB4}$
20	18	$\overline{IOW}$	46	42	GND
21	19	$\overline{IOR}$	47	43	$\overline{SDB5}$
22	20	D7	48	44	$\overline{SDB6}$
23	21	D6	7		*NC*
24	22	D5	18		*NC*
25	23	Vcc	31		*NC*
26	24	D4	42		*NC*

P,D = L53C80PC
L53C80DC

J,K = L53C80JC
L53C80KC

$\overline{RST}$ — SCSI BUS RESET:
Bidirectional/Active low. $\overline{RST}$ when active indicates a SCSI bus reset condition.

$\overline{I/O}$ — INPUT/OUTPUT:
Bidirectional/Active low. $\overline{I/O}$ is controlled by the target and specifies the direction of information transfer. When $\overline{I/O}$ is asserted, the direction of transfer is to the initiator. $\overline{I/O}$ is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

$\overline{C/D}$ — CONTROL/DATA:
Bidirectional/Active low. $\overline{C/D}$ is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when $\overline{C/D}$ is deasserted.

$\overline{MSG}$ — MESSAGE:
Bidirectional/Active low. $\overline{MSG}$ is controlled by the target, and when asserted indicates MESSAGE phase.

$\overline{REQ}$ — REQUEST:
Bidirectional/Active low. $\overline{REQ}$ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. $\overline{REQ}$ is deasserted upon receipt of $\overline{ACK}$ from the initiator. Data is latched by the initiator on the lowgoing edge of $\overline{REQ}$ for initiator receive operations.

B. Microprocessor Bus

$\overline{CS}$ — CHIP SELECT:
Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST:
Output/Active high. This signal is used to indicate that the L5380/L53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST:
Output/Active high. The L5380/L53C80 asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

$\overline{IOR}$ — I/O READ:
Input/Active low. $\overline{IOR}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped read of a L5380/L53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA read of the SCSI input data register.

READY — READY:
Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA, and must be specifically enabled by the CPU. In blockmode DMA, data is throttled by treating the L5380/L53C80 as wait state memory. $\overline{I/O}$ (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the L5380/L53C80. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

$\overline{DACK}$ — DMA ACKNOWLEDGE:
Input/Active low. $\overline{DACK}$ is used in conjunction with $\overline{IOR}$ or $\overline{IOW}$ to enable reading or writing the SCSI Input and Output Data Registers when in DMA mode. $\overline{DACK}$ resets DRQ and must not occur simultaneously with $\overline{CS}$.

$\overline{EOP}$ — END OF PROCESS:
Input/Active low. This input is used to indicate to the L5380/L53C80 that a DMA transfer is to be concluded. The L5380/L53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$ from the DMA controller.

$\overline{RESET}$ — CPU BUS RESET:
Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the $\overline{RST}$ signal on the SCSI bus and therefore affects only the local L5380/L53C80 and not other devices on the bus.

$\overline{IOW}$ — I/O WRITE:
Input/Active low. $\overline{IOW}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped write of a L5380/L53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA write of the SCSI output data register.

A_2, A_1, A_0 — ADDRESS 2,1,0:
Inputs/Active high. These signals, in conjunction with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, address the L5380/L53C80 internal registers for CPU read/write operations.

D_{7-0} — DATA 7–0:
Bidirectional/Active high. These signals are the microprocessor data bus. D_7 is the most significant bit.

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L5380/L53C80 INTERNAL REGISTERS

Overview

The L5380/L53C80 contains registers that are directly addressed by the microprocessor. These registers allow for monitoring of SCSI bus activity, controlling the operation of the L5380/L53C80, and determining the cause of interrupts. In many cases, a read-only and a write-only register are mapped to the same address. Some addresses are dummy registers which are used to implement a control operation but do not correspond to a physical register. The state of the CPU data bus when writing or reading these dummy registers is 'don't care.' Tables 1 and 3 show the address and name of each register as well as bit definitions.

Register Descriptions

A. WRITE OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/L53C80 internal registers for write operations as shown in Table 1.

WRITE ADDRESS 0 — Output Data Register

The Output Data Register is a write-only register used for sending information to the SCSI data bus. During arbitration, the arbitrating SCSI device asserts its ID via this register. The device which wins arbitration also asserts the "OR" of its ID and the ID of the target/initiator to be selected/reselected. In programmed I/O, this register is written using $\overline{CS}$ and $\overline{IOW}$ with A_{2-0} = 000. In DMA mode, it is written when $\overline{IOW}$ and $\overline{DACK}$ are simultaneously active, irrespective of the state of the address lines. Note that a "1" written to the Output Data Register becomes a low state when asserted on the active-low SCSI bus.

WRITE ADDRESS 1 — Initiator Command Register

The Initiator Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the initiator. Some bits in this register are not readable, and these positions are mapped to status bits useful in monitoring the progress of arbitration. These, along with the initiation of systemwide reset and test functions may also be of use to the target.

R1 Bit 7 - Assert $\overline{RST}$

When this bit is set, the L5380/L53C80 asserts the $\overline{RST}$ line on the SCSI bus, initializing all devices on the bus to the reset condition. All logic and internal registers of the L5380/L53C80 are reset, except for the Assert $\overline{RST}$ bit itself, the Testmode bit (R1 bit 6) and the IRQ (interrupt request) latch. The IRQ pin becomes active indicating a SCSI bus reset interrupt. This interrupt is not maskable.

R1 Bit 6 - Testmode

When this bit is set, the L5380/L53C80 places all outputs including both SCSI and CPU signals, in a high impedance state. This effectively removes the device from the system as an aid to system diagnostics. Note that internal registers may still be written while in testmode. The L5380/L53C80 returns to normal operation when Testmode is reset. The Testmode bit is reset by writing a 0 to R1 bit 6, or via the $\overline{RESET}$ (CPU reset) pin. Testmode is not affected by the $\overline{RST}$ (SCSI bus reset) signal, or by the Assert $\overline{RST}$ bit in the Initiator Command Register (R1 bit 7).

R1 Bit 5 - Not Used

R1 Bit 4 - Assert $\overline{ACK}$

When this bit is set, $\overline{ACK}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ACK}$. Note that $\overline{ACK}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is reset, indicating that the L5380/L53C80 is acting as an initiator.

R1 Bit 3 - Assert $\overline{BSY}$

When this bit is set, $\overline{BSY}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{BSY}$. $\overline{BSY}$ is asserted to indicate that the device has been selected or reselected, and deasserting $\overline{BSY}$ causes a bus free condition.

R1 Bit 2 - Assert $\overline{SEL}$

When this bit is set, $\overline{SEL}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{SEL}$. $\overline{SEL}$ is normally asserted after a successful arbitration.

R1 Bit 1 - Assert $\overline{ATN}$

When this bit is set, $\overline{ATN}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ATN}$. $\overline{ATN}$ is asserted by the initiator to request message out phase. Note that $\overline{ATN}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is reset, indicating that the L5380/L53C80 is acting as an initiator.

R1 Bit 0 - Assert Data Bus

When this bit is set, the open drain SCSI data bus and parity drivers are enabled and the contents of the Output Data Register are driven onto the SCSI data lines. In addition to the Assert Data Bus bit, enabling of the SCSI bus drivers requires one of the following two sets of conditions:

When the L5380/L53C80 is operating as an initiator, the Targetmode bit (R2 bit 6) must be reset, the I/O pin must be negated (initiator to target transfer) and no phase mismatch condition exist. A phase mismatch occurs when the $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ bits of the Target Command Register (R3) do not match the corresponding SCSI control lines.

When the L5380/L53C80 is operating as a target, the Targetmode bit will be set, and in this case Assert Data Bus will enable the outputs unconditionally.

The Assert Data Bus bit need not be set for arbitration to occur; when the Arbitrate bit (R2 bit 0) is set, and a bus free condition is detected, the data bus will be enabled for arbitration independent of the state of the Assert Data Bus bit.

Finally, note that the Testmode bit (R1 bit 6) overrides all other controls including Assert Data Bus and Arbitrate, and disables all outputs.

WRITE ADDRESS 2 — Mode Register

The Mode register is a read/write register which provides control over several aspects of L5380/L53C80 operation. Programmed I/O or two different types of DMA transfer may be selected, initiator or target device operation is accommodated, and parity checking and interrupts may be enabled via this register. The function of each individual bit is described as follows:

R2 Bit 7 - Blockmode

This bit must be used in conjunction with DMA Mode (R2 bit 1). It is used to select the type of handshake desired between the L5380/L53C80 and the external DMA controller. See "L5380/L53C80 Data Transfers" for a complete discussion of the transfer types supported.

R2 Bit 6 - Targetmode

When this bit is set, the L5380/L53C80 will operate as a SCSI target device. This enables the SCSI signals $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, and $\overline{REQ}$ to be asserted. When Targetmode is reset, the device will operate as an initiator. This enables the SCSI signals $\overline{ATN}$ and $\overline{ACK}$ to be asserted. Targetmode also affects state machine operation for DMA transfers, and the conditions necessary for enabling the SCSI Data bus drivers. (See Assert Databus, R1 bit 0).

Table 1. WRITE Register Chart.

Address 0 — Output Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	TEST MODE		ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RUPT	ENABLE EODMA INT'RUPT	MONITOR BUSY	DMA MODE	ARBITRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C/D}$	ASSERT $\overline{I/O}$

Address 4 — ID Select Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 5 — Start DMA Send

7	6	5	4	3	2	1	0

Address 6 — Start DMA Target Receive

7	6	5	4	3	2	1	0

Address 7 — Start DMA Initiator Receive

7	6	5	4	3	2	1	0

4

R2 Bit 5 - Enable Parity Check

When this bit is set, information received on the SCSI data bus is checked for odd parity. When Enable Parity Check is set, the Parity Error latch will be set whenever data is received under DMA control or the Current SCSI Data Register (Read Register 0) is read by the CPU. The state of the parity error latch can be determined by reading R5 bit 5, and it can be reset by a read to Address 7. Note that enable parity check must be set if parity error interrupts are to be generated. This interrupt can be separately masked by the Enable Parity Interrupt bit (R2 bit 4) while retaining the state of the parity error latch for later examination by the CPU.

R2 Bit 4 - Enable Parity Interrupt

When this bit is set, the L5380/L53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a parity error. Enable Parity Check (R2 bit 5) must also be set if parity error interrupts are desired.

R2 Bit 3 - Enable End Of DMA Interrupt

When this bit is set, the L5380/L53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a valid $\overline{EOP}$ (End of Process) signal. $\overline{EOP}$ is normally generated by a DMA controller to indicate the end of a DMA transfer. $\overline{EOP}$ is valid only when coincident with $\overline{IOR}$ or $\overline{IOW}$ and $\overline{DACK}$.

R2 Bit 2 - Monitor Busy

When this bit is set, the L5380/L53C80 continuously monitors the state of the $\overline{BSY}$ signal. Absence of $\overline{BSY}$ for a period longer than 400 ns (but less than 1200 ns) will cause the L5380/L53C80 to set the BSYERR and IRQ (interrupt request) latches. In addition, the 6 least significant bits of the Initiator Command Register are reset, and all SCSI data and control outputs are disabled until the BSYERR latch is reset. This effectively disconnects the L5380/L53C80 from the SCSI bus in response to an unexpected disconnect by another device. It also allows the CPU to be interrupted when the SCSI bus becomes free in systems where arbitration is not used and an $\overline{EOP}$ signal is not available.

R2 Bit 1 - DMA Mode

When this bit is set, the L5380/L53C80's internal state machines automatically control the SCSI signals $\overline{REQ}$ and $\overline{ACK}$ (as appropriate for initiator or target operation) and the CPU signals' DRQ and READY. DMA Mode must be set prior to starting a DMA transfer in either direction. The DMA Mode bit is reset whenever a bus free condition is detected ($\overline{BSY}$ is not active). This aborts DMA operations when a loss of $\overline{BSY}$ occurs, regardless of the state of the Monitor Busy bit (R2 bit 2.) The DMA Mode bit is not reset when $\overline{EOP}$ is received, but must be specifically reset by the CPU. $\overline{EOP}$ does however inhibit additional DMA cycles from occurring.

R2 Bit 0 - Arbitrate

This bit is set to indicate a desire to arbitrate for use of the SCSI bus. Before setting the Arbitrate bit, the SCSI Output Data Register (Write Register 0) must be written with the SCSI ID assigned to the arbitrating SCSI device. The bit position of register R0 which is set represents the priority number of the SCSI device, with bit 7 the highest priority. See the section on "Arbitration" for a full discussion of the L5380/L53C80 arbitration procedure.

WRITE ADDRESS 3 — Target Command Register

The Target Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the target. In addition, this register contains a read-only status flag useful in unambiguously determining when the last byte of a DMA transfer has actually been sent over the SCSI bus.

When operating as an initiator with DMA mode set, the ASSERT $\overline{MSG}$, ASSERT $\overline{C/D}$, and ASSERT $\overline{I/O}$ bits are used as a template to compare against the corresponding SCSI control signals provided by the target. A phase mismatch interrupt will be generated on the falling edge of the $\overline{REQ}$ input if the template does not match the state of the signals. Therefore the CPU should initialize these bits to the phase of the expected data transfer. An interrupt then will signal an intent by the target to change to a new phase. The SCSI information transfer phases and their associated direction of data transfer are given in Table 2.

Table 2. SCSI Information Transfer Phases

MSG	C/D	I/O	Phase	Direction		
0	0	0	Data Out	Initiator	→	Target
0	0	1	Data In	Target	→	Initiator
0	1	0	Command	Initiator	→	Target
0	1	1	Status	Target	→	Initiator
1	0	0	Unused			
1	0	1	Unused			
1	1	0	Message Out	Initiator	→	Target
1	1	1	Message In	Target	→	Initiator

R3 Bits 7–4 - Not Used

R3 Bit 3 - Assert $\overline{REQ}$

When this bit is set, $\overline{REQ}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{REQ}$. Note that $\overline{REQ}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target.

R3 Bit 2 - Assert $\overline{MSG}$

When this bit is set, $\overline{MSG}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{MSG}$. Note that $\overline{MSG}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{MSG}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 1 - Assert $\overline{C/D}$

When this bit is set, $\overline{C/D}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{C/D}$. Note that $\overline{C/D}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{C/D}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 0 - Assert $\overline{I/O}$

When this bit is set, $\overline{I/O}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{I/O}$. Note that $\overline{I/O}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{I/O}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

WRITE ADDRESS 4 —
ID Select Register

The ID Select Register is a write-only register which is used to monitor for selection or reselection attempts to the L5380/L53C80. In arbitrating systems, an ID number is assigned to each SCSI device by setting a single bit position of the ID select register. Each SCSI data pin is inverted and compared with the corresponding bit in the ID Select Register. If any matches are found while a bus free condition exists and $\overline{SEL}$ is active, the L5380/L53C80 will generate an interrupt to indicate a selection or reselection. During selection or reselection, parity checking may be enabled by setting the Enable Parity Check bit (R2 bit 5). This interrupt may be masked by resetting all bits in this register.

WRITE ADDRESS 5 —
Start DMA Send

This is a dummy register. Writes to this location are detected and cause the L5380/L53C80 internal state machine to execute a DMA send operation. This location is used for either initiator or target DMA send. The DMAMODE bit (R2 bit 1) must be set prior to writing this location.

WRITE ADDRESS 6 —
Start DMA Target Receive

This is a dummy register. Writes to this location are detected and cause the L538/L53C80 internal state machine to execute a target DMA receive operation. The DMAMODE bit (R2 bit 1) and the TARGETMODE bit (R2 bit 6) must be set prior to writing this location.

WRITE ADDRESS 7 —
Start DMA Initiator Receive

This is a dummy register. Writes to this location are detected and cause the L5380/L53C80 internal state machine to execute an initiator DMA receive operation. The DMAMODE bit (R2 bit 1) must be set and the TARGETMODE bit (R2 bit 6) must be reset prior to writing this location.

B. READ OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/L53C80 internal registers for read operations as shown in Table 3.

READ ADDRESS 0 —
Current SCSI Data Bus

The Current SCSI Data Bus Register allows the microprocessor to monitor the SCSI data bus at any time, by asserting CS and IOR with address lines $A_{2-0} = 000$. The SCSI data lines are not actually registered, but gated directly onto the CPU bus whenever address 000 is read by the CPU. Therefore, reads of this location should only be done when the SCSI data lines are guaranteed to be stable by the SCSI protocol. For systems which implement SCSI bus arbitration, this location is read to determine whether devices having higher priorities are also arbitrating. Programmed I/O data transfer uses this location for reading data transferred on the SCSI data bus. With parity checking enabled, SCSI data bus parity checking is done at the beginning of the read cycle for fast error detection. Note that the SCSI data bus is inverted to become active high when presented to the CPU.

READ ADDRESS 1 —
Initiator Command Register

Reading bit 7 or bits 4–0 of the Initiator Command Register simply reflects the status of the corresponding bit in the register. Bits 6 and 5 are mapped to other signals as discussed below:

R1 Bit 6 - Arbitration In Progress

For this bit to be active, the ARBITRATE bit (R2 bit 0) must be set. When ARBITRATION IN PROGRESS is set, it indicates that the L5380/L53C80 has detected a bus free condition and is currently arbitrating for control of the bus. See the section on "Arbitration" for a complete discussion of the L5380/L53C80 arbitration mechanism. Resetting the ARBITRATE bit will reset ARBITRATION IN PROGRESS.

R1 Bit 5 - Lost Arbitration

For this bit to be active, the ARBITRATE bit (R2 bit 0) must be set. When LOST ARBITRATION is set, it indicates that the L5380/L53C80 has arbitrated for the SCSI bus (see R1 bit 6 above) and has detected the assertion of SEL by another (higher priority) device. The L5380/L53C80 responds to loss of arbitration by immediately discontinuing the arbitration attempt. Resetting the ARBITRATE bit will reset LOST ARBITRATION.

READ ADDRESS 2 —
Mode Register

Reading the Mode Register simply reflects the status of the bits in that register.

READ ADDRESS 3 —
Target Command Register

Reading the Target Command Register simply reflects the status of the bits in that register, except for bit 7, LAST BYTE SENT.

R3 bit 7 - Last Byte Sent

This read only bit indicates that the last byte of data loaded into the L5380/L53C80 during a DMA send operation has actually been transferred over the SCSI bus. Note that the end of process flag and the corresponding interrupt occur when this byte is loaded into the L5380/L53C80, but do not reflect whether it has actually been sent. This bit is not present in the NCR5380, but is present in the NCR53C80. Last Byte Sent is reset when the DMAMODE bit (R2 bit 1) is reset.

READ ADDRESS 4 —
Current SCSI Control Register

The Current SCSI Control Register provides a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 100 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 5 —
DMA Status Register

The DMA Status Register provides a means for the CPU to determine the status of a DMA transfer and to determine the cause of an interrupt. It also makes available the final two SCSI bus signals which are not included in the Current SCSI Control Register. The function of each individual bit is defined as follows:

R5 Bit 7 - End of DMA

When this bit is set, it indicates that a valid $\overline{EOP}$ has been received during a DMA transfer. A valid $\overline{EOP}$ occurs when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for the minimum specified time. End of DMA is reset when the DMAMODE bit (R2 bit 1) is reset.

Note that for DMA send operations, an END OF DMA status indicates only that the last byte of the transfer is loaded into the Output Data Register of the sending device, not that it has actually been transferred over the SCSI bus. For this reason, the L5380/L53C80 provides an additional status bit; LAST BYTE SENT (R3 bit 7) which indicates that this final byte has been transferred to the receiving end. This bit is not present in the NCR5380.

Also, note that the DMAMODE bit is reset automatically whenever a loss of busy condition is detected, which in turn resets END OF DMA. Therefore

the DMA Status Register should be read prior to resetting the ASSERT $\overline{BSY}$ bit (R1 bit 3) at the conclusion of a DMA transfer.

R5 Bit 6 - DMA Request

This bit reflects the state of the DRQ (DMA Request) signal. In programmed I/O, this bit can be polled by the CPU to determine whether there is a pending request for byte transfer. For DMA send operations, DMA REQUEST is reset when $\overline{DACK}$ and $\overline{IOW}$ are simultaneously asserted. For DMA receive operations, simultaneous $\overline{DACK}$ and $\overline{IOR}$ will reset DMA REQUEST. DMA REQUEST is reset unconditionally when the DMAMODE bit (R2 bit 1) is reset.

R5 Bit 5 - Parity Error

This bit can only be set if ENABLE PARITY CHECK (R2 bit 5) is set. When enabled, the PARITY ERROR bit is set if incoming SCSI data in either initiator or target mode, or during selection phase, does not correctly reflect odd parity. PARITY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 4 - Interrupt Request

This bit reflects the state of the IRQ signal. The L5380/L53C80 asserts IRQ to generate an interrupt to the CPU. See the section on "Interrupts" for further information on the possible sources of interrupts in the L5380/L53C80. INTERRUPT REQUEST can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 3 - Phase Match

When this bit is set, it indicates that the $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ lines match the state of the ASSERT $\overline{MSG}$, ASSERT $\overline{C/D}$, and ASSERT $\overline{I/O}$ bits in the Target Command Register. PHASEMATCH is not actually registered, but represents a continuous comparison of these three phase bits to the corresponding internal register

Table 3. READ Register Chart.

Address 0 — Current SCSI Data Bus

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	ARB. IN PRO-GRESS	LOST ARB.	ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RUPT	ENABLE EODMA INT'RUPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C/D}$	ASSERT $\overline{I/O}$

Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{PARITY}$

Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQUEST	PARITY ERROR	INTER-RUPT REQUEST	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Address 6 — Input Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 7 — Reset Error/Interrupt Register

7	6	5	4	3	2	1	0

locations. This bit is intended for use by the initiator to detect that the target device has changed to a different information transfer phase. When the L5380/L53C80 detects a phase mismatch, PHASEMATCH is reset, and information transfer to or from the SCSI bus is inhibited.

R5 Bit 2 - Busy Error

This bit can only be set if the MONITOR BUSY bit (R2 bit 2) is set. When set, BUSY ERROR indicates that the BSY pin has been false for a period at least equal to a bus settle delay (400 ns) When the BUSY ERROR condition is detected, all SCSI signal pins are disabled, and the DMAMODE bit (R2 bit 1) and bits 0–5 of the Initiator Command Register are reset. BUSY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bits 1, 0 - $\overline{ATN}$, $\overline{ACK}$

Like the Current SCSI Control Register, these bits provide a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 5 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 6 —
Input Data Register

This register acts as a temporary holding register for information received from the SCSI data bus during DMA transfers (DMAMODE bit, R2 bit 1 is set). In the initiator mode, the L5380/L53C80 latches the SCSI data when $\overline{REQ}$ goes active, while in the target mode data is latched when $\overline{ACK}$ goes active. The contents of this register represent the negation of the low-true SCSI data. The contents of the SCSI Input Data Register are gated onto the CPU data bus when $\overline{DACK}$ and $\overline{IOR}$ are simultaneously true, or by a CPU read of location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously, to prevent conflicting read operations. Parity may optionally be checked on the data as it is loaded into this register.

READ ADDRESS 7 —
Reset Error/Interrupt Register

This is a dummy register. Reads to this location are detected and used to reset the Interrupt Request Latch (IRQ signal) and the PARITY ERROR, INTERRUPT REQUEST, and BUSY ERROR latches (visible as bits 5, 4, and 2 of Register 5).

INTERRUPTS

The L5380/L53C80 generates interrupts to the CPU by setting the Interrupt Request Latch, which directly drives the IRQ (Interrupt Request) line. The IRQ output will reflect the state of the Interrupt Request Latch under all conditions except when TESTMODE (R1 bit 6) is active, when it is in a high impedance state. The Interrupt Request Latch may be reset by reading Address 7, the Reset Error/Interrupt Register. A read of this location also resets several error condition latches as discussed in the section on "Internal Registers."

Interrupts may be caused by any of six conditions, most of which may be masked by resetting enable bits in the appropriate registers. The following sections describe each interrupt type, its cause, and how it may be reset. Upon receiving an interrupt, the CPU may read the Current SCSI Control Register (R4) and the DMA Status Register (R5) to determine the cause of the interrupt. While the following discussions indicate the expected values of these registers following an interrupt, it is recommended that bits in these registers which are not germane to determining the cause of an interrupt be masked off in firmware prior to implementing a comparison. A typical operational sequence for an interrupt service routine is given at the end of this section.

SCSI Bus Reset Interrupt

A SCSI Bus Reset Interrupt occurs when the SCSI $\overline{RST}$ signal becomes active. This may be due to another SCSI device driving the $\overline{RST}$ line, or because the ASSERT $\overline{RST}$ bit (R1 bit 7) has been set, causing the L5380/L53C80 to drive the SCSI $\overline{RST}$ line. The value of the SCSI $\overline{RST}$ line is visible as R4 bit 7; however, this line is not latched and therefore may have changed state by the time the CPU responds to the interrupt and polls this location. For this reason a SCSI Bus Reset Interrupt should be assumed if no other interrupt condition is active when reading Registers 4 and 5.

The SCSI Bus Reset Interrupt is nonmaskable. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Selection/Reselection Interrupt

A Selection/Reselection Interrupt occurs when the SCSI $\overline{SEL}$ signal becomes active, the SCSI bus matches the bit set in the ID Select Register, and $\overline{BSY}$ has been false for at least a bus settle delay. When the $\overline{I/O}$ pin is as-serted, the interrupt should be interpreted as a reselection. The Selection/Reselection Interrupt may be masked by resetting all bits in the ID Select Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Loss of Busy Interrupt

A Loss of Busy Interrupt occurs when the SCSI $\overline{BSY}$ signal has been inactive for at least a bus settle delay (400 ns). The Loss of Busy Interrupt may be masked by resetting the MONITOR BUSY bit (R2 bit 2). Resetting MONITOR BUSY also prevents the BUSY ERROR latch (Read R5 bit 2) from being set. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Phase Mismatch Interrupt

A Phase Mismatch Interrupt occurs when the DMAMODE bit (R2 bit 1) is set, $\overline{REQ}$ is active on the SCSI bus, and the SCSI phase signals $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ do not match the corresponding bits in the Target Command Register. This interrupt is intended for use by the initiator to detect a change of phase by the target during a DMA transfer. When operating as a target, the SCSI phase lines will normally be asserted via the Target Command Register, so no phase mismatch will be generated unless another SCSI device is erroneously driving the phase lines to an unintended state.

The result of the continuous comparison of the SCSI phase lines to the Target Command Register contents is visible as the PHASE MATCH bit (Read R5 bit 3). This flag operates irrespective of the state of DMAMODE and $\overline{REQ}$. As long as a phase mismatch condition persists, the L5380/L53C80 is prevented from recognizing active $\overline{REQ}$ inputs, and SCSI output data drivers are disabled.

The Phase Mismatch interrupt is nonmaskable, however it will only occur when operating in DMAMODE. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Parity Error Interrupt

A Parity Error Interrupt occurs when incorrect parity is detected during a read of the SCSI bus. Parity checking occurs under the following conditions: Parity is checked during a programmed I/O read of the Current SCSI Data Register (Read R0), when $\overline{CS}$ and $\overline{IOR}$ are active and the A2-0

Table 4. Interrupt Read Values

Read Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{PARITY}$
SCSI Bus Interrupt							
X	0	0	0	0	0	0	0
Selection/Reselection Interrupt							
0	0	0	X	X	1=RESEL	1	X
Loss of Busy Interrupt							
0	0	0	0	0	0	0	0
Phase Mismatch Interrupt							
0	1	1	X	X	X	0	X
Parity Error Interrupt							
0	X	X	X	X	X	X	X
End of DMA Interrupt							
0	1	X	X	X	X	0	X

Read Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$
SCSI Bus Interrupt							
0	0	0	1	1	0	0	0
Selection/Reselection Interrupt							
0	0	0	1	X	0	X	0
Loss of Busy Interrupt							
0	0	0	1	X	1	0	0
Phase Mismatch Interrupt							
0	0	0	1	0	X	X	0
Parity Error Interrupt							
X	X	1	1	X	X	X	X
End of DMA Interrupt							
1	0	0	1	X	0	0	X

lines are 000. Parity is also checked during DMA read operations (DMAMODE bit, R2 bit 1 is set) when $\overline{ACK}$ is active for target receive, or $\overline{REQ}$ is active for initiator receive.

The PARITY ERROR latch is set when parity error checking is enabled and one of the above parity error conditions is encountered. This latch is visible as bit 5 of the DMA Status Register (Read R5). The Parity Error Interrupt may be masked and setting of the PARITY ERROR latch prevented by resetting the ENABLE PARITY CHECK bit (Write R2 bit 5). The PARITY ERROR latch can be reset by reading the Reset Error/Interrupt Register (Read R7). The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

End of DMA Interrupt

An End of DMA Interrupt occurs when a valid $\overline{EOP}$ (End of Process) signal is detected during a DMA transfer. $\overline{EOP}$ is valid when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously asserted for the minimum specified time. $\overline{EOP}$ inputs not occurring during I/O read or write operations are ignored.

The End of DMA latch is set whenever the DMAMODE bit (R2 bit 1) is set and a valid $\overline{EOP}$ is received. This latch is visible as bit 7 of the DMA Status Register (Read R5). The End of DMA Interrupt may be masked by resetting the ENABLE EODMA INTERRUPT bit (Write R2 bit 3). This bit does not affect the END OF DMA latch, however. The End of DMA latch can be reset by resetting the DMAMODE bit in the Mode Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

DATA TRANSFERS

The L5380/L53C80 supports programmed I/O under CPU control or DMA transfer via a DMA controller when transferring information to and from the SCSI data bus. Programmed I/O can be implemented entirely in firmware or using minimum external logic for accessing the appropriate registers. Under DMA control, the L5380/L53C80's DMA interface logic and internal state machines provide the necessary control of the $\overline{REQ}$-$\overline{ACK}$ handshake. Each type of transfer is fully described in the following sections.

Programmed I/O

Two forms of programmed I/O are supported by the L5380/L53C80. For normal programmed I/O, the SCSI handshake is accomplished by setting bits in the Initiator or Target Command registers to assert SCSI control lines, and polling the Current SCSI Control and DMA Control registers for the appropriate responses. Since for this method the control is contained in firmware, the cycle times are relatively slow. It is most appropriate for transferring small blocks of data such as SCSI command blocks or messages, where the overhead of

Table 5. Typical Interrupt Service Routine Polling Service

Read Address 5 > TEMP	: Read DMA Status Reg to variable TEMP
IF TEMP "AND" HEX (10) = 0 THEN GO TO NEXT DEVICE	: IRQ not active, so L5380/L53C80 was not the source of this interrupt
TEMP "AND" HEX (AC) → TEMP	: Mask off irrevelant bits
IF TEMP > HEX (7F) THEN GO TO EODMA	: End of DMA Interrupt
IF TEMP > HEX (1F) THEN GO TO PARERR	: Parity Error Interrupt
IF TEMP > HEX (07) THEN GO TO PHASERR	: Phase Mismatch Interrupt
IF TEMP > HEX (03) THEN GO TO BYSERR	: Loss of Busy Interrupt
Read Address 4 → TEMP	: Read Current SCSI Control Reg to variable TEMP
TEMP "AND" HEX (06) → TEMP	: Mask off irrevelant bits
IF TEMP = HEX (06) THEN GO TO RESEL	: Reselection Interrupt
IF TEMP = HEX (02) THEN GO TO SEL	: Selection Interrupt
IF TEMP = HEX (00) THEN GO TO RESET	: SCSI Bus Reset Interrupt

setting up a DMA controller could be significant.

Pseudo DMA

An alternate method of programmed I/O allows the state machines of the L5380/L53C80 to handle the SCSI handshake, thereby improving performance in systems which do not employ a hardware DMA controller. To implement Pseudo DMA, the DMAMODE bit is set. The CPU polls the DRQ bit in the DMA Control Register to determine when a byte should be written to or read from the L5380/L53C80. When reading or writing, external logic must be used to decode the L5380/L53C80 location and produce $\overline{DACK}$, since it is used by the internal state machines. Also, $\overline{CS}$ must be suppressed since it may not be asserted simultaneously with $\overline{DACK}$.

Normal DMA Mode

Normal DMA mode is obtained when the DMAMODE bit is set but the BLOCKMODE bit is reset. The DMA process is started by writing to the Start DMA Send, Start DMA Initiator Receive, or Start DMA Target Receive locations as appropriate. Once started, the internal state machines of the L5380/L53C80 manage the $\overline{REQ}$ - $\overline{ACK}$ handshake protocol, as well as the DRQ-$\overline{DACK}$ handshake with the DMA controller.

The L5380/L53C80 will assert DRQ whenever it is ready to transfer a byte to or from the DMA controller. In response to DRQ, the controller asserts $\overline{DACK}$ and $\overline{IOR}$ to read the byte, or $\overline{DACK}$ and $\overline{IOW}$ to write a byte to the L5380/L53C80. For write operations, the byte is latched at the rising edge of the logical AND of $\overline{DACK}$ and $\overline{IOW}$. The transfer can be terminated by asserting $\overline{EOP}$ during a read or write operation, or by resetting the DMAMODE bit.

Block DMA Mode

When the BLOCKMODE bit is set, the DMA handshake is no longer dependent on interlocked DRQ-$\overline{DACK}$ cycles. Instead, the DMA controller may be allowed to free-run, with data flow throttled by inserting "wait-states" in the DMA transfer to or from the L5380/L53C80. Wait-states, which are idle clock cycles inserted during the I/O read or write operation, are inserted by the DMA controller until the READY output of the L5380/L53C80 goes true, allowing the bus cycle to conclude.

The READY output will be deasserted under the following conditions: For send operations, READY will be false whenever the Output Data Register contains a byte which has not been transferred over the SCSI bus. This allows the DMA controller to access RAM to fetch the next byte, but postpones the end of the CPU bus cycle until the previous byte has been transferred, freeing the Output Data Register to receive it.

For receive operations, READY will be false whenever the Input Data Register is empty. This allows the DMA controller to address the RAM for a write operation, but postpones the end of the CPU bus cycle until the incoming byte is stored in the Input Data Register and is available on the CPU bus.

Note that when blockmode is employed, $\overline{DACK}$ may optionally remain asserted throughout the DMA transfer, since it is not used in an interlocked DMA handshake. (Its interlock function is replaced by $\overline{IOR}$ or $\overline{IOW}$.) Also, DRQ will be asserted in the normal way when operating in blockmode. To gain the abovementioned performance benefits, it should be used only to initiate the first byte transfer, with READY used to throttle succeeding transfers. This methodology is compatible with DMA controllers such as the Intel 8237 and AMD Am9516/9517.

In summary, blockmode operation offers the potential for improved transfer rates by overlapping the DMA memory access with the SCSI transfer. This is of particular value when used with DMA controllers capable of "flyby" operation, where the data is transferred directly from memory to the peripheral, and does not pass through the DMA controller itself. This transfer rate gain is achieved at the expense of locking up the CPU bus for a time equal to the SCSI transit time of the entire block. This may be strongly preferable in some systems where net disk access time is a crucial performance factor. Also, the time required to arbitrate for the CPU bus on a byte-by-byte basis may well be longer than the cycles wasted waiting for SCSI transfers to take place, especially with fast peripherals which operate from a high speed sector buffer.

Terminating DMA Transfers

DMA transfers, either normal or blockmode, may be terminated in a number of ways. The following sections describe these methods, along with providing information about correct sequencing of various signals to effect a clean exit from a DMA process.

$\overline{EOP}$ Signal

The $\overline{EOP}$ signal is usually generated by a DMA controller to indicate that its transfer counter has decremented to zero. In order to be recognized by the L5380/L53C80, it should be asserted simultaneously with the $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals corresponding to the last byte in the transfer. Note that in the case of send operations, asserting $\overline{EOP}$ indicates to the L5380/L53C80 that SCSI transfers should cease after transmission of the

byte loaded while $\overline{EOP}$ is asserted. In order to determine when this last byte has actually been sent, the LAST BYTE SENT flag in the Target Command Register may be examined. This flag is not present in the NCR implementation of the 5380, but is available in the 53C80, a non-pin-compatible variant. The $\overline{EOP}$ input does not reset the DMAMODE bit, but after transmission of the last byte causes the internal state machine to return to an idle condition, so that no further SCSI handshaking will occur until another transmission is explicitly initiated. Note that the NCR version of the 5380, upon receiving an $\overline{EOP}$, will stop asserting DRQ, but will continue to issue $\overline{ACK}$ in response to additional $\overline{REQ}$ inputs, potentially causing data loss if the target initiates another data transmission without an intervening phase change. The L5380/L53C80 prevents this spurious DMA handshake from occurring.

DMAMode Bit

Resetting the DMAMODE bit in the Mode Register causes a hard reset of the internal DMA state machines, and thus an effective termination of a DMA transfer. Since unlike the $\overline{EOP}$ case the state machine is not allowed to exit gracefully, care must be taken in the timing of DMAMODE reset.

For receive operations, the DMAMODE bit should be reset after the last DRQ is received, but prior to asserting $\overline{DACK}$ to prevent an additional $\overline{REQ}$ or $\overline{ACK}$ from occurring. For normal DMA mode, resetting this bit will cause DRQ to go inactive. However the last byte received remains in the SCSI Input Data Register and may be read either by the normal $\overline{DACK}$ and $\overline{IOR}$ DMA read or using a CPU read of Address 6. For blockmode DMA, READY will remain asserted when DMAMODE is reset, allowing the DMA controller to retrieve the last byte in the normal fashion. The NCR version of the 5380 fails to keep ready asserted when DMAMODE is reset, potentially causing deadlock on the CPU bus.

Bus Phase Mismatch

When operating in DMAMODE as an initiator, a bus phase mismatch can be used to terminate a data transfer. If the $\overline{C/D}$, $\overline{I/O}$, and $\overline{MSG}$ lines fail to match the corresponding bits in the Target Command Register, it will prevent recognition of $\overline{REQ}$, and will disable the SCSI data and parity output drivers. Also, when $\overline{REQ}$ becomes active, an interrupt will be generated. Because $\overline{REQ}$ is not recognized, the effect is to stop the DMA transfer, although the state machine does not return to idle until either DMAMODE is reset or a valid $\overline{EOP}$ is received.

One caution should be observed when using phase changes to end DMA transfers: While this method obviates the need for the initiator to keep a transfer counter, it depends on the target causing a phase change between any two consecutive information transfer phases. Since this is not required by the protocol, it must be guaranteed by the target software. Otherwise the target may begin a new information transfer without the initiator recognizing the boundary between the two.

ARBITRATION

The L5380/L53C80 contains on-chip hardware to assist in arbitrating for the SCSI bus. This arbitration logic cooperates with the host firmware to effect SCSI arbitration, as described in the following paragraphs:

The SCSI arbitration timeline begins with detection of a bus free condition at time t0. Bus free is defined as BSY and $\overline{SEL}$ inactive for at least a bus settle delay (400 ns). Following the bus settle delay, the SCSI device must wait an additional bus free delay of 800 ns, for a total of 1200 ns after t0, prior to driving any signal. Thus a minimum of 1200 ns must elapse from initial deassertion of $\overline{BSY}$ to the beginning of an arbitration attempt. A final constraint is that arbitration may not begin if more than a bus set delay (1800 ns) has elapsed since $\overline{BSY}$ became active (arbitration began), corresponding to 2200 ns after t0.

The CPU indicates a desire to arbitrate by setting the ARBITRATE bit (R2 bit 0.) When ARBITRATE is set, the L5380/L53C80 will monitor the state of $\overline{BSY}$ and $\overline{SEL}$ to detect a bus free condition. The actual implementation uses an internal delay line to provide a time reference for detection of a bus free condition. This delay is nominally 800 ns during which $\overline{BSY}$ and $\overline{SEL}$ must be inactive. This time represents the center of the window between the Bus Settle Delay (400 ns) and the Bus Free Delay (400 + 800 = 1200 ns). When Bus Free is detected, the L5380/L53C80 waits for an additional time of nominally 900 ns (1700 ns nominal since t0) and asserts $\overline{BSY}$ and the contents of the Output Data Register. This time represents the center of the 1200 ns–2200 ns window between the earliest and latest legal arbitration attempt. Since the actual delays are process and temperature dependent, they will vary in practice, but will always remain well within the specified limits.

Once arbitration has begun ($\overline{BSY}$ and the Output Data Register asserted,) the ARBITRATION IN PROGRESS bit (R1 bit 6) will be set, allowing the CPU to detect the fact that arbitration has begun. The CPU should then wait one arbitration delay (2.2 µs) before reading the bus to determine whether

arbitration has been won or lost. The LOST ARBITRATION bit (R2 bit 7) will be active if the L5380/L53C80 has detected $\overline{SEL}$ active on the SCSI bus, indicating that another SCSI device has declared itself the winner of the arbitration. $\overline{SEL}$ active also disables the SCSI output drivers, allowing the winning arbitrator to proceed with its transfer.

BUG FIXES/ENHANCMENTS

The NCR5380 and the Am5380 have some architectural bugs, both published and unpublished. The **Logic Devices L5380/L53C80** was designed to eliminate these bugs while maintaining pin and architectural compatibility. A list of these errors along with solutions implemented in the L5380/L53C80 is itemized below.

1. When executing blockmode DMA send operations, the READY signal is intended to insert memory wait states as a mechanism to throttle data transfer, with the DMA controller in a free-running loop. The NCR/Am5380 erroneously allows the contents of the Output Data Register to be overwritten by subsequent bytes prior to acknowledgment of the current byte by the SCSI receiver. This causes loss of data when operating in blockmode if the sender's DMA cycle is faster than the receiver's.

2. Assertion of $\overline{EOP}$ during blockmode DMA transfers fails to cause assertion of READY in the NCR/Am5380. This may prevent the CPU from becoming bus master and can result in lockup of the CPU bus in a not-ready state. In block DMA send mode when $\overline{EOP}$ is received, the L5380/L53C80 reasserts READY immediately after transmitting the final byte. For receive mode, READY is asserted immediately.

3. When a valid $\overline{EOP}$ is detected, the NCR/Am5380 prevents assertion of additional DRQ's, but continues to respond to SCSI handshakes. This means that additional data transmitted without phase change may be lost. The L5380/L53C80, like the NCR/Am5380 remains in DMAMODE after an $\overline{EOP}$. However, the internal state machine returns to an idle condition and does not respond to additional SCSI handshake attenpts until another data transfer is explicitly initiated.

4. When operating as an initiator in DMAMODE, the NCR/Am5380 leaves $\overline{ACK}$ asserted after receipt of a valid $\overline{EOP}$, requiring the CPU to deassert it. When a valid $\overline{EOP}$ is detected, the L5380/L53C80 deasserts $\overline{ACK}$ properly.

5. If the NCR/Am5380 is not terminated on the SCSI side, the floating $\overline{RST}$ pin will cause spurious interrupts. The L5380/L53C80 contains internal high value pullups to set unterminated SCSI pins to the inactive state.

6. During DMA send operations, when a valid $\overline{EOP}$ signal is received by the NCR/Am5380, no convenient indication exists to indicate that the last byte of data (loaded simultaneously with EOP) has in fact been successfully transmitted. The L5380/L53C80 provides LAST BYTE status bit mapped to bit 7 of the Target Command Register. This bit will be set after a valid $\overline{EOP}$ has occurred, and the final byte has been transmitted successfully.

7. During the reselection phase, the NCR/AM5380 may reset the reselection interrupt if the contents of the Target Command Register do not match the current SCSI bus phase. The L5380/L53C80 does not spuriously reset this interrupt.

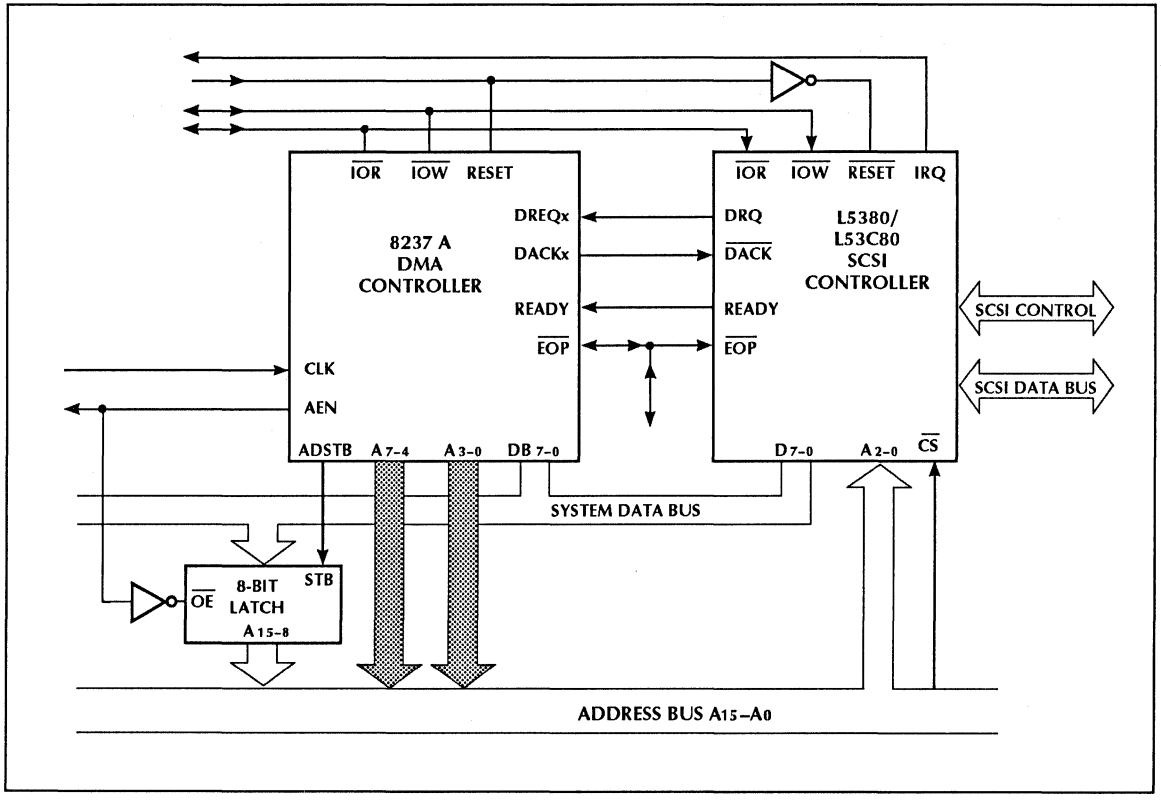
8. In the NCR/Am5380, the phase mismatch interrupt is captured in an edge triggered fashion on the active edge of $\overline{REQ}$. During reselection, this interrupt might not be generated even though a phase change has occurred. The reason for this is as follows:

- The initiator DMAMODE bit must be set in order to receive a phase-match interrupt.
- However, the DMAMODE bit cannot be set unless $\overline{BSY}$ is active.
- $\overline{BSY}$ will be driven active by the target only after the relesection has occurred.
- Once $\overline{BSY}$ has been asserted by the target, it may then assert $\overline{REQ}$ before the initiator has set the DMAMODE bit, and the initiator will then fail to generate an interrupt.

The L5380/L53C80 interrupt latch will be set if a phase mismatch condition exists when the later of $\overline{REQ}$ or DMAMODE become active. In this way, the mismatch will always be detected, even if the target asserts request before the initiator sets DMAMODE.

4

DMA Interface with 8237 A.

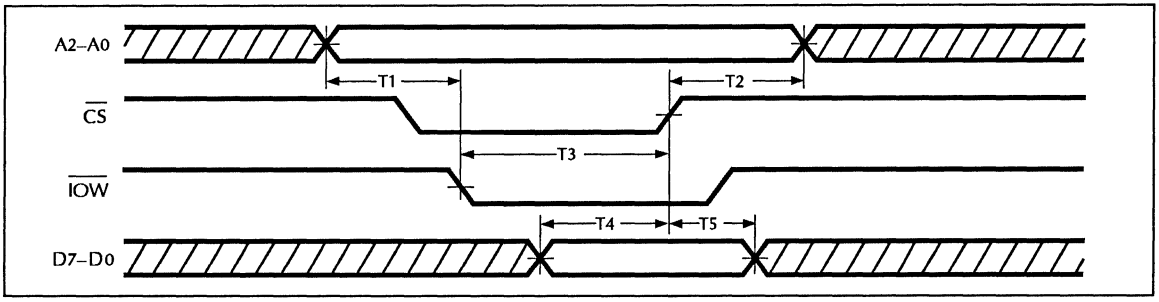


SWITCHING CHARACTERISTICS

A. CPU Write Timing —*(Units measured in ns except where noted)*

		Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
T1	Address Setup to Write Enable	10		5		10	
T2	Address Hold from End of Write Enable	0		0		0	
T3	Width of Write Enable	40		20		40	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	10		5		10	

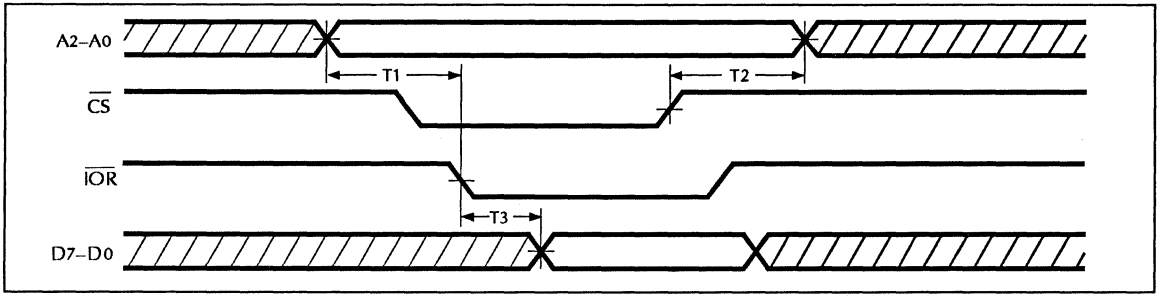
CPU Write Waveforms



B. CPU Read Timing —*(Units measured in ns except where noted)*

		Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
T1	Address Setup to Read Enable	10		5		10	
T2	Address Hold from End of Read Enable	0		0		0	
T3	Data Access Time from Read Enable		50		20		50

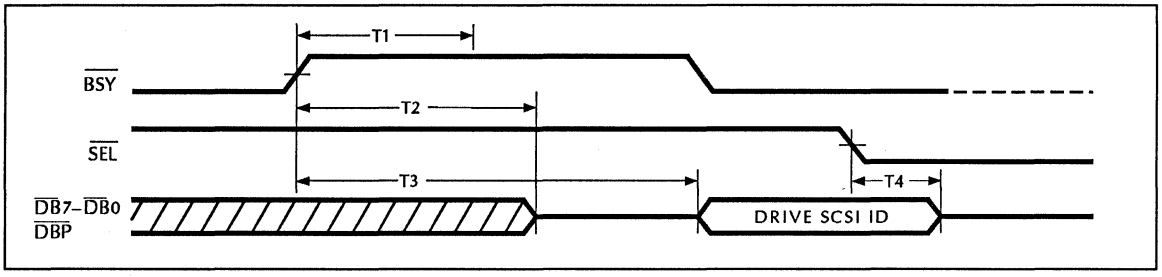
CPU Read Waveforms



C. Arbitration —*(Units measured in ns except where noted)*

Symbol	Parameter	Commercial		Military	
		Min	Max	Min	Max
T1	$\overline{BSY}$ False Duration to Detect Bus Free Condition	0.4 µs	1.1 µs	0.4 µs	1.1 µs
T2	SCSI Bus Clear (High Z) from $\overline{BSY}$ False		1.1 µs		1.1 µs
T3	Arbitrate ($\overline{BSY}$ and SCSI ID asserted) from $\overline{BSY}$ False (Bus Free Detected)	1.2 µs	2.2 µs	0.8 µs	2.4 µs
T4	SCSI Bus Clear (High Z) from $\overline{SEL}$ True (Lost Arbitration)		60		60

Arbitration Waveforms



D. DMA Write Initiator Send —*(Units measured in ns)*

Symbol	Parameter	Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
		Min	Max	Min	Max	Min	Max
The following apply for all DMA Modes							
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ & $\overline{DACK}$)		60		30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ & $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{REQ}$ False to $\overline{ACK}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		65		45		65
T14	SCSI Data Setup Time to $\overline{ACK}$ True	60		65		60	
The following apply for Normal DMA Mode only							
T7	$\overline{REQ}$ False to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{DACK}$ False)		70		35		70
The following apply for BLOCKMODE DMA only							
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{REQ}$ False to READY True		60		30		60
T12	$\overline{IOW}$ False to Ready False		70		35		70

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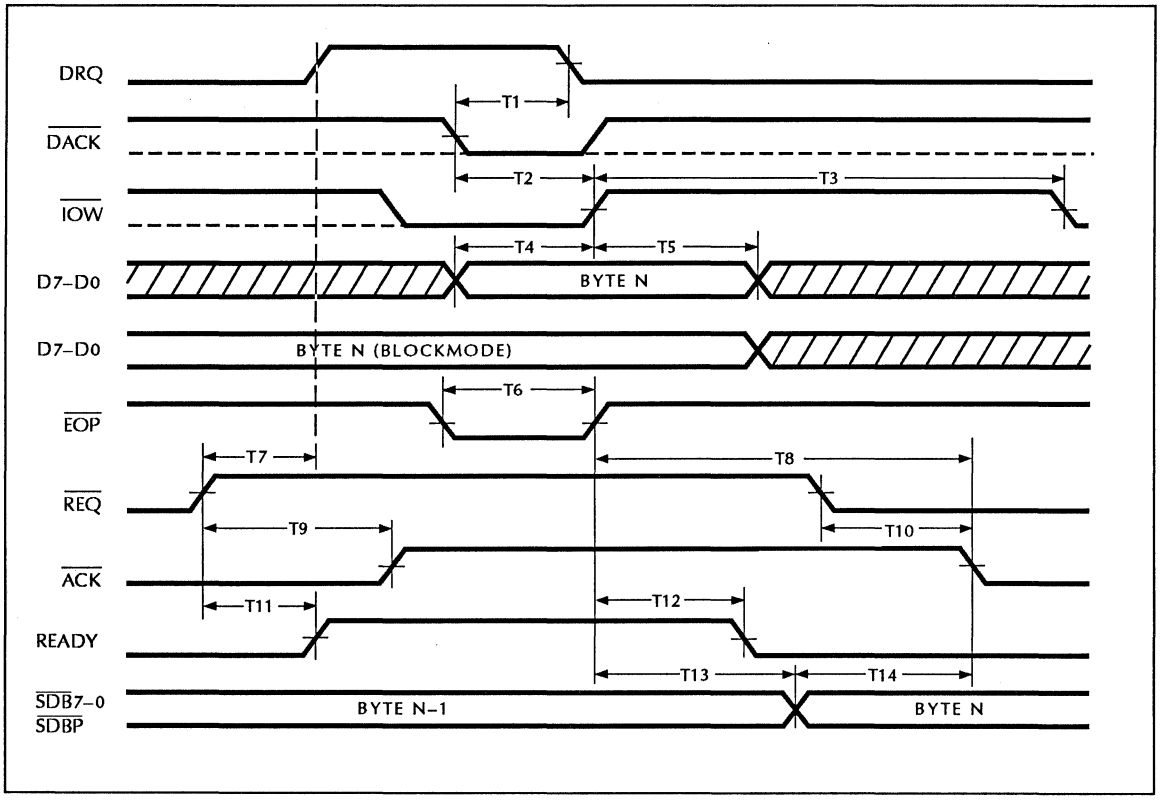
DMA Write Initiator Send Waveforms



E. DMA Read Initiator Receive —*(Units measured in ns)*

Symbol	Parameter	Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
		Min	Max	Min	Max	Min	Max
The following apply for all DMA Modes							
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ & $\overline{DACK}$		60		20		60
T4	Concurrence Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{REQ}$ True to $\overline{ACK}$ True		70		35		70
T12	SCSI Data Setup Time to $\overline{REQ}$ True	20		5		20	
T13	SCSI Data Hold Time from $\overline{REQ}$ True	15		5		15	
The following apply for Normal DMA Mode only							
T5	$\overline{REQ}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		80		45		80
The following apply for BLOCKMODE DMA only							
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{IOR}$ False)		80		45		80
T9	$\overline{REQ}$ False to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to Ready False		70		35		70

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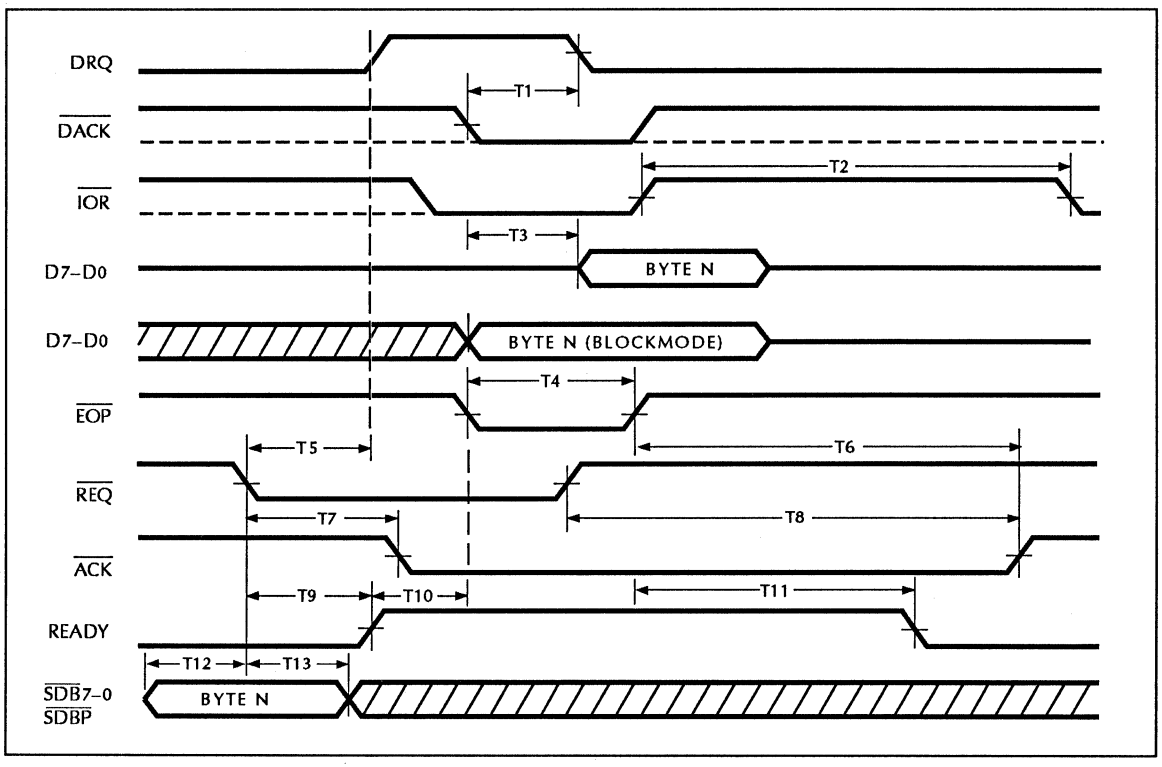
DMA Read Initiator Receive Waveforms



F. DMA Write Target Send —*(Units measured in ns)*

Symbol	Parameter	Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
		Min	Max	Min	Max	Min	Max
The following apply for all DMA Modes							
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ & $\overline{DACK}$)		60		`30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ & $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		60		45		60
T14	SCSI Data Setup Time to $\overline{REQ}$ True	60		65		60	
The following apply for Normal DMA Mode only							
T7	$\overline{ACK}$ False to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35		70
The following apply for BLOCKMODE DMA only							
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{ACK}$ True to READY True		60		30		60
T12	$\overline{IOW}$ False to Ready False		70		35		70

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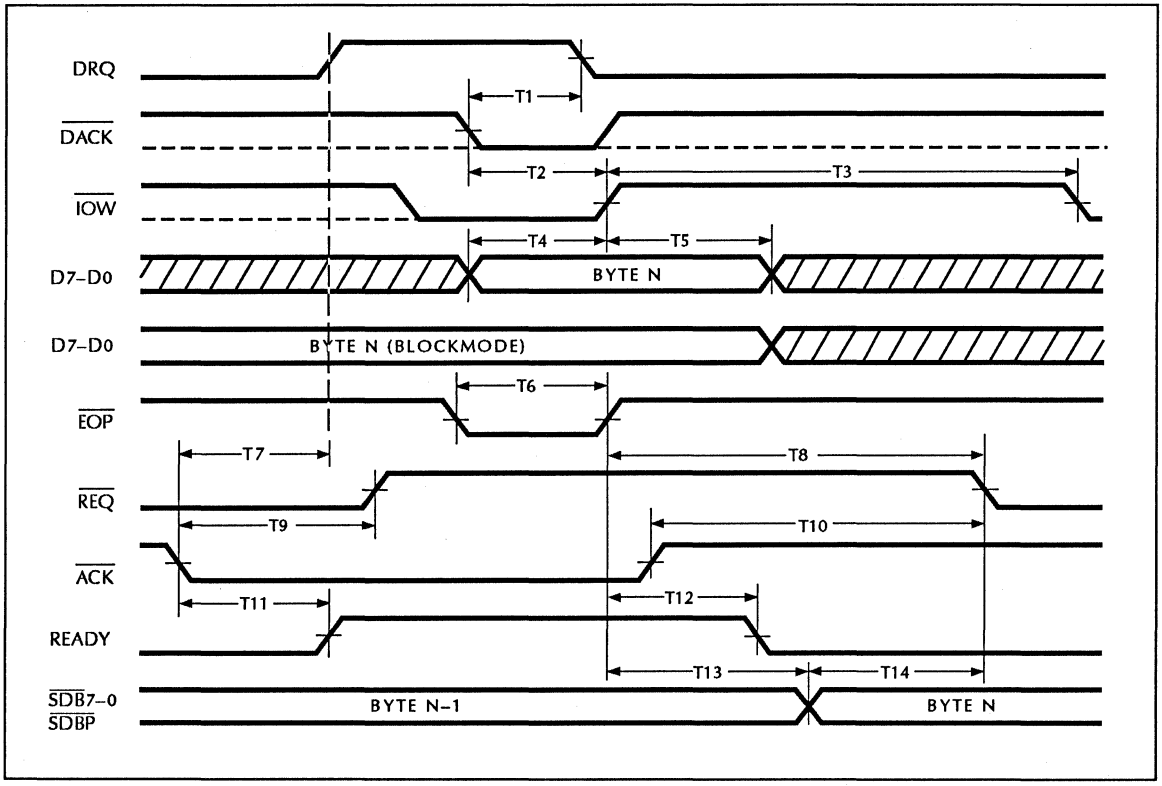
DMA Write Target Send Waveforms



G. DMA Read Target Receive —*(Units measured in ns)*

Symbol	Parameter	Commercial				Military	
		2 Mbytes/sec		4 Mbytes/sec		2 Mbytes/sec	
		Min	Max	Min	Max	Min	Max
The following apply for all DMA Modes							
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ & $\overline{DACK}$		60		20		60
T4	Concurrence Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45		90
T12	SCSI Data Setup Time to $\overline{ACK}$ True	20		5		20	
T13	SCSI Data Hold Time from $\overline{ACK}$ True	15		5		15	
The following apply for Normal DMA Mode only							
T5	$\overline{ACK}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		70		35		70
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35		70
The following apply for BLOCKMODE DMA only							
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		70		35		70
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOR}$ False)		70		35		70
T9	$\overline{ACK}$ True to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to Ready False		70		35		70

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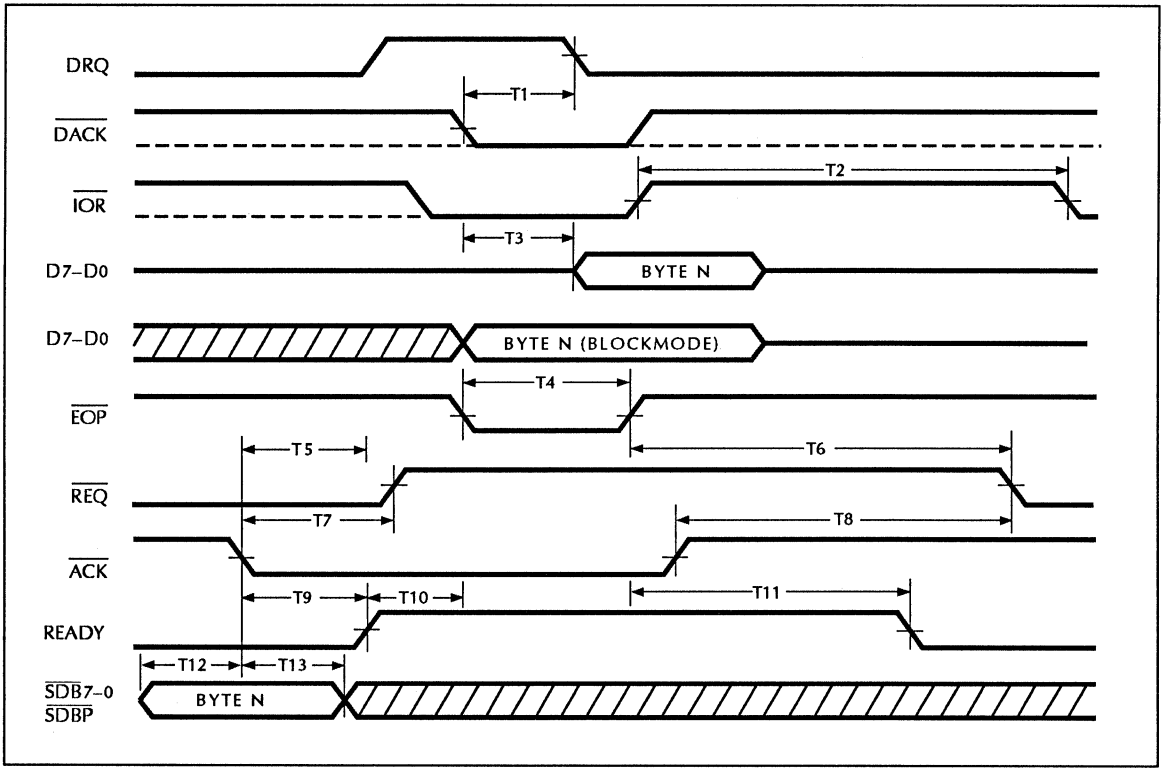
DMA Read Target Receive Waveforms



Maximum Ratings

Above which useful life may be impaired

Storage temperature	−65°C to +150°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Output voltage	0.0 to V_{CC}
Input Voltage	0.0 to 5.5 V
I_{OL} Low Level Output Current (SCSI bus)	48 mA
I_{OL} Low Level Output Current (other pins)	8 mA
I_{OH} High Level Output Current (other pins)	−4 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage		0.0		0.8	V
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{OL}	Low Level Output Voltage (SCSI bus)	V_{CC} = min, I_{OL} = 48 mA			0.5	V
V_{OL}	Low Level Output Voltage (other pins)	V_{CC} = min, I_{OL} = 8 mA			0.5	V
VOH	High Level Output Voltage (other pins)	V_{CC} = min, I_{OH} = −4 mA	3.5			V
I_I	Input Current*	V_{CC} = max, V_I = 0 – V_{CC} (SCSI bus)			65	µA
I_I	Input Current*	V_{CC} = max, V_I = 0 – V_{CC} (other pins)			20	µA
I_{CC}	Supply Current	V_{CC} = max, V_{IH} = 2.4, V_{IL} = 0.4, 4 MHz cycle, no load, no termination		10	20	mA
I_{CC}	Supply Current Quiescent	As above, inputs stable			1.0	mA

* Not tested at low temperature extreme.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance	
	4 Mbytes/sec	2 Mbytes/sec
40-pin Plastic DIP (0.6") — P3	L5380PC4	L5380PC2
40-pin Sidebraze (0.6") Hermetic DIP — D3	L5380DC4	L5380DC2
48-pin Plastic DIP (0.6") — P5	L53C80PC4	L53C80PC2
48-pin Sidebraze (0.6") Hermetic DIP — D5	L53C80DC4	L53C80DC2
44-pin Plastic LCC, J-Lead — J1	L5380JC4 L53C80JC4	L5380JC2 L53C80JC2
44-pin Ceramic LCC — K2	L5380KC4 L53C80KC4	L5380KC2 L53C80KC2

Military Operating Range (–55°C to +125°C)

Package Style	Performance
	2 Mbytes/sec
40-pin Sidebraze (0.6") Hermetic DIP — D3	L5380DM2 L5380DMB2
48-pin Sidebraze (0.6") Hermetic DIP — D5	L53C80DM2 L53C80DMB2
44-pin Ceramic LCC — K2	L5380KM2 L53C80KM2 L5380KMB2 L53C80KMB2

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LOGIC

Contents

5

Overview — Commitment to Quality

Management Commitment Statement

A successful quality program requires that every employee act as a member of the quality organization. This applies particularly to the management team who establish acceptable behavior by their actions. Bill Volz, President/CEO of Logic Devices Incorporated encourages active participation of all departments in a quality oriented operation.

At Logic Devices, the quality department strives to maintain a proactive relationship with Manufacturing, Design, Marketing, and Sales emphasizing training and procedural controls. Training and good communication allow employees to understand which practices lead to good quality and reliability and make them willing participants in the quality program. This attitude has allowed Logic Devices to continually improve the quality of its product line.

Organization

The Quality/Reliability Department reports directly to the President/CEO. The quality operation is divided into two functions:

1. Quality Administration
2. Reliability Engineering

Quality Administration performs all inspections/Q.A. monitors in assembly/test operations including incoming inspection of all direct materials. Q.A. Administration also includes the document control function.

The Reliability Engineering function is responsible for assuring that all products manufactured by Logic Devices meet our rigid standards for reliability. Activities that support this function include qualifications of new products, reliability monitor testing, failure analysis, and corrective action.

Documentation

All manufacturing and Q.A. procedures are controlled in the document control area and are available in controlled binders located in the appropriate manufacturing areas. In addition, the program plans for the quality and reliability functions are described in individual manuals:

Quality Manual. The quality function is described in the quality program plan as outlined in the Quality Manual. The program plan has been designed to the requirements of Appendix A of Mil-M-38510.

Reliability Manual. The reliability of Logic Devices' products is among the best in the industry and will continue to be. The Reliability Manual has been created to insure that we maintain high visibility of reliability data. This manual also describes the reliability function and goals at Logic Devices.

Mil-Std-883C. All products to be sold as 883C compliant are manufactured to this specification. As new revisions are released, they are evaluated and changes implemented as required.

Mil-M-38510. This document is referenced continuously by Mil-Std-883C and specifically defines program requirements for compliance to 883C programs.

Available Processing Flows

Logic Devices offers many processing flows to provide the best combination of reliability assurance and cost. Available flows are:

1. Commercial Plastic Flow.
2. Commercial Plastic Flow with 48 hr burn-in.
3. Commercial Hermetic Flow — 0° to +70°C.
4. Commercial Hermetic Flow — –55°C to +125°C.
5. Hi Rel Hermetic Flow — 0°C to +70°C with 48 hr burn-in.
6. Hi Rel 883C Flow — Per Mil-Std-883C, Methods 5004 and 5005.
7. Hi Rel Extended Flow — Per Logic Devices Flow pages 5-14 to 5-17.

Reliability Monitor Program

Logic Devices' reliability monitor program is designed for early detection of any potential reliability problems and taking appropriate actions for evaluation and correction. Data gathered from monitor testing is evaluated and utilized in a continuous effort to improve the reliability of products at Logic Devices.

Test Name	Conditions	Sample Size/Accept
Early Failure Rate	80 hrs, 125°C	77/1
Latent Failure Rate	2000 hrs, 125°C	77/1
Pressure Cooker	96 hrs, A102*	100/1
Biased Humidity Life	1000 hrs, A101*	77/1
Temperature Cycle	15 cycles, A104*	77/1

*JEDEC STD-22B Test Methods

Reliability and Failure Rate Prediction

The failure rate of semiconductor devices over time is due to a variety of mechanisms. Most of these are chemical reactions which eventually degrade device functionality beyond prescribed limits. Determining the effects of time, temperature, current flow, applied field, etc. on the rate of these reactions is central to predicting reliability of a group of semiconductor devices. If these effects can be known or approximated, then failure rates under actual use conditions can be extrapolated from data taken under accelerated stress. This is useful because the failure rate of modern semiconductor devices under commercial operating conditions is so low that an inordinate amount of time would be required to gather a statistically meaningful sample of failed devices.

The usual method of accelerating stress is to subject the devices to elevated temperature (i.e., burn-in). The electrical environment during burn-in attempts to model actual use so that the effects of current and voltage on failure rate are normalized out. If the failure rate vs time is assumed constant, then the remaining parameter of failure rate is temperature.

The expression which relates reaction rate and temperature is called the Arrhenius equation, and is given below:

$$R(t) = C\, e^{\frac{-Ea}{kT}}$$

where

R(t) = reaction rate (failure rate),

C = a constant,

Ea = activation energy, a parameter which varies with the failure mechanism but is generally between 0.3 and 1.3 eV,

k = Boltzmann's constant; 8.625×10^{-5} eV/degree K,

T = temperature in degrees K.

A more useful equation results from taking the ratio of the Arrhenius equation at the elevated stress temperature and the intended operating temperature. This will give the failure rate acceleration factor, denoted lambda (λ). λ is a measure of the increase in failure rate of the devices at the higher temperature relative to that at the lower temperature.

$$\lambda = \frac{R(T_{acc})}{R(T_{op})}$$

$$= e^{\frac{-Ea}{k}\left(\frac{1}{T_{acc}} - \frac{1}{T_{op}}\right)}$$

where

T_{acc} = accelerated temperature in degrees K

T_{op} = operating temperature in degrees K

This equation is commonly used for calculations relating to elevated-temperature burn-in. In burn-in, semiconductor devices are operated for a short period (typically 48 or 160 hours) at a temperature of 125 or 150°C. The acceleration equation is used to derive an estimate of the number of hours of high-temperature exposure necessary to produce the same number of device failures as a much longer period of operation at normal temperature.

As an example of the use of the acceleration equation, for a failure mechanism with an activation energy of 0.8 eV, a burn-in temperature of 125°C, and an expected operating junction temperature of 27°C, the failure rate acceleration with burnin would be:

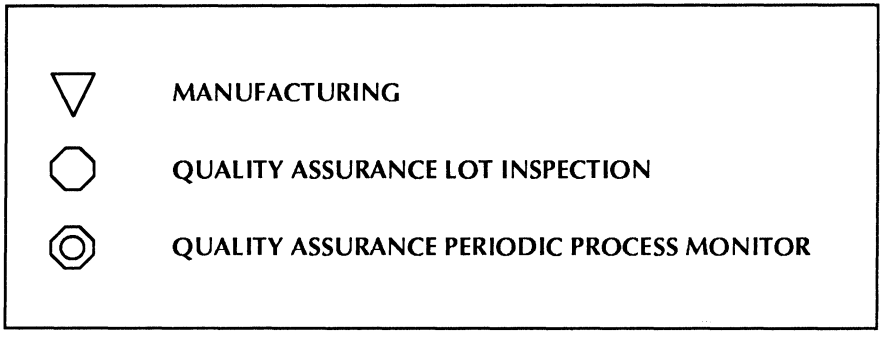
$$e^{\frac{-0.8}{8.63\times10^{-5}}\left(\frac{1}{398} - \frac{1}{300}\right)} = 2015$$

Therefore the expected failure rate under actual operating conditions would be 2015 times less than the failure rate experienced during burn-in.

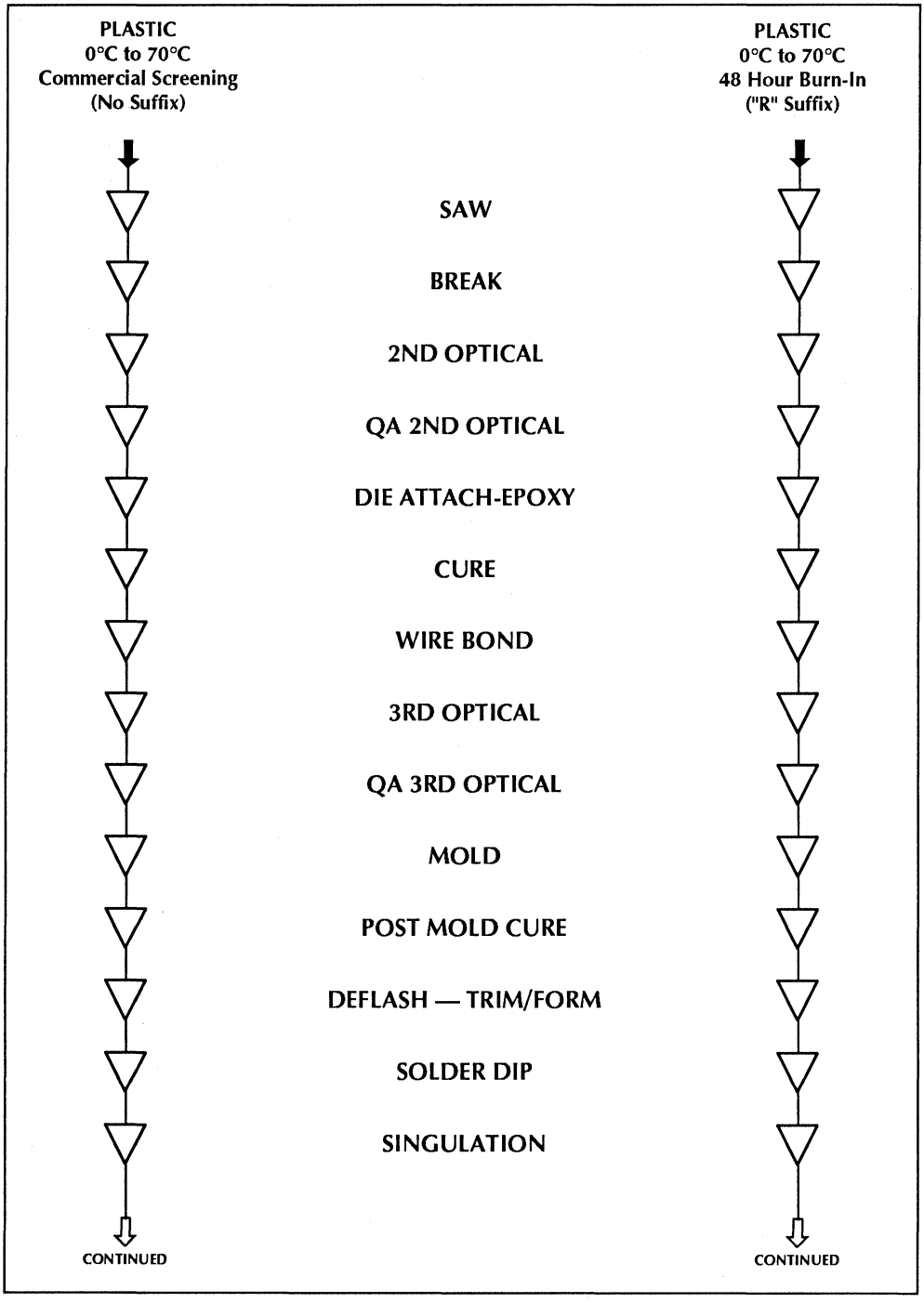
Life test data taken from representative Logic Devices products is kept on file and is available to customers. This data allows the calculation of expected failure rates over time for Logic products under given operating conditions. Contact your local Logic Devices representative for more information.

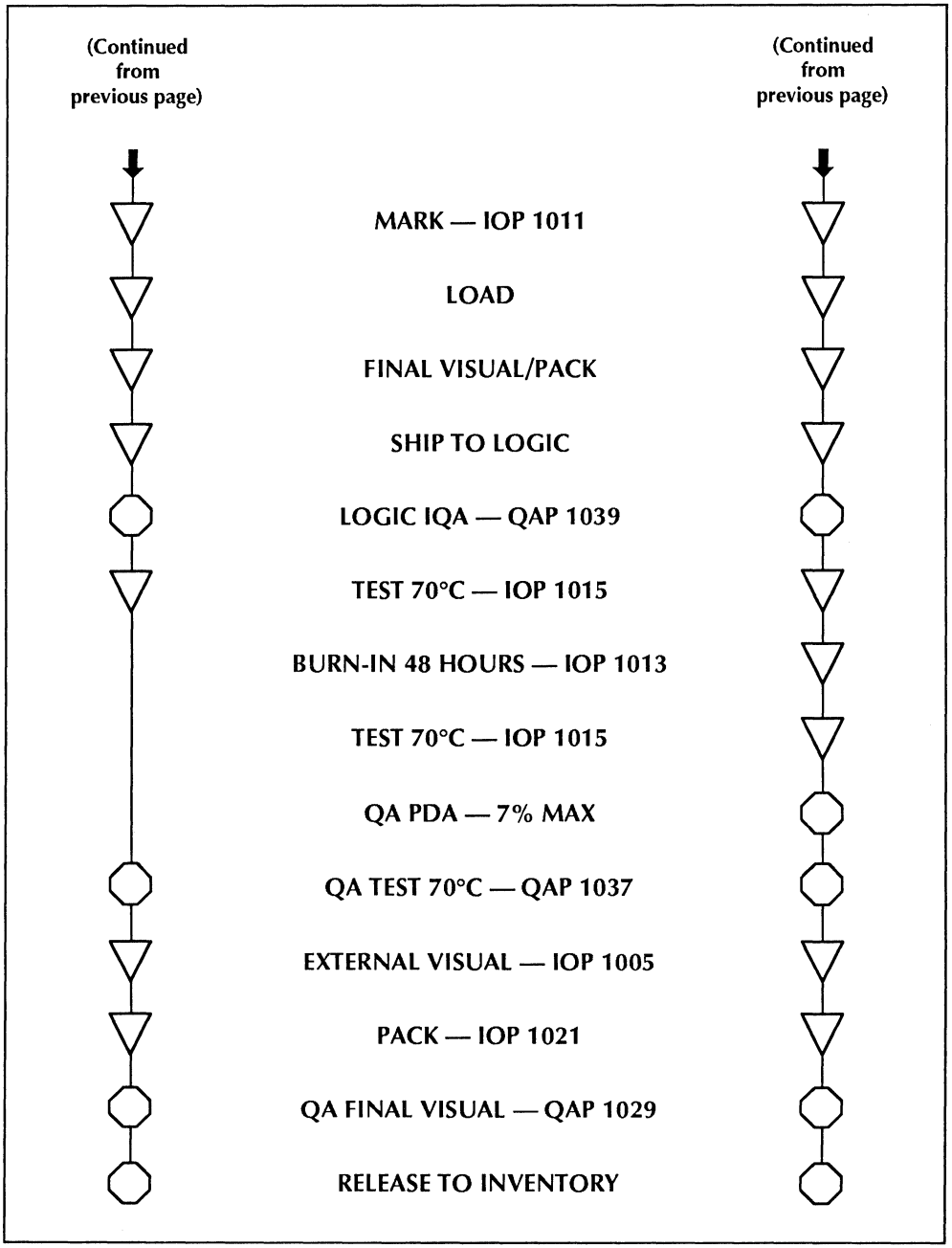
Assembly Flows

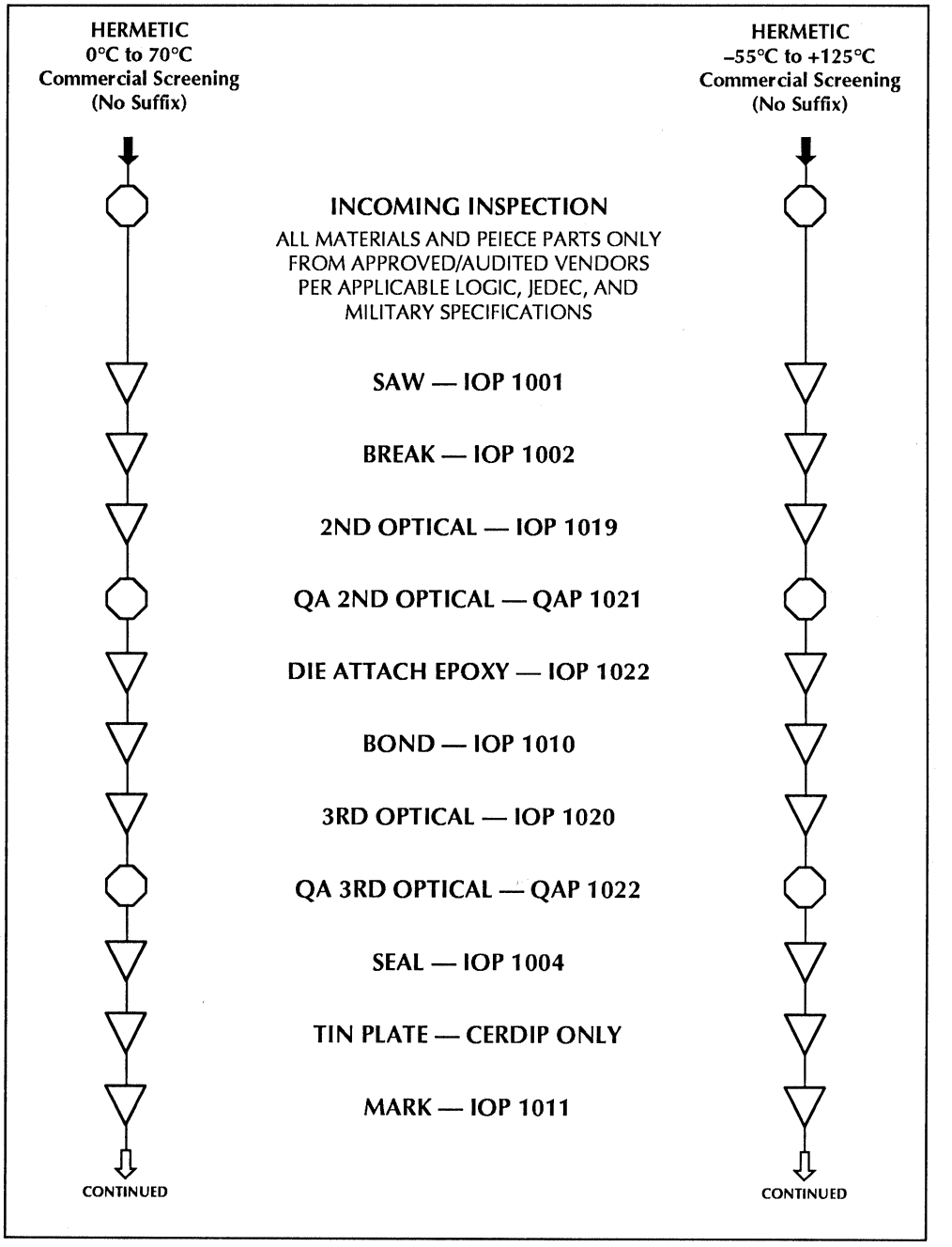
KEY:

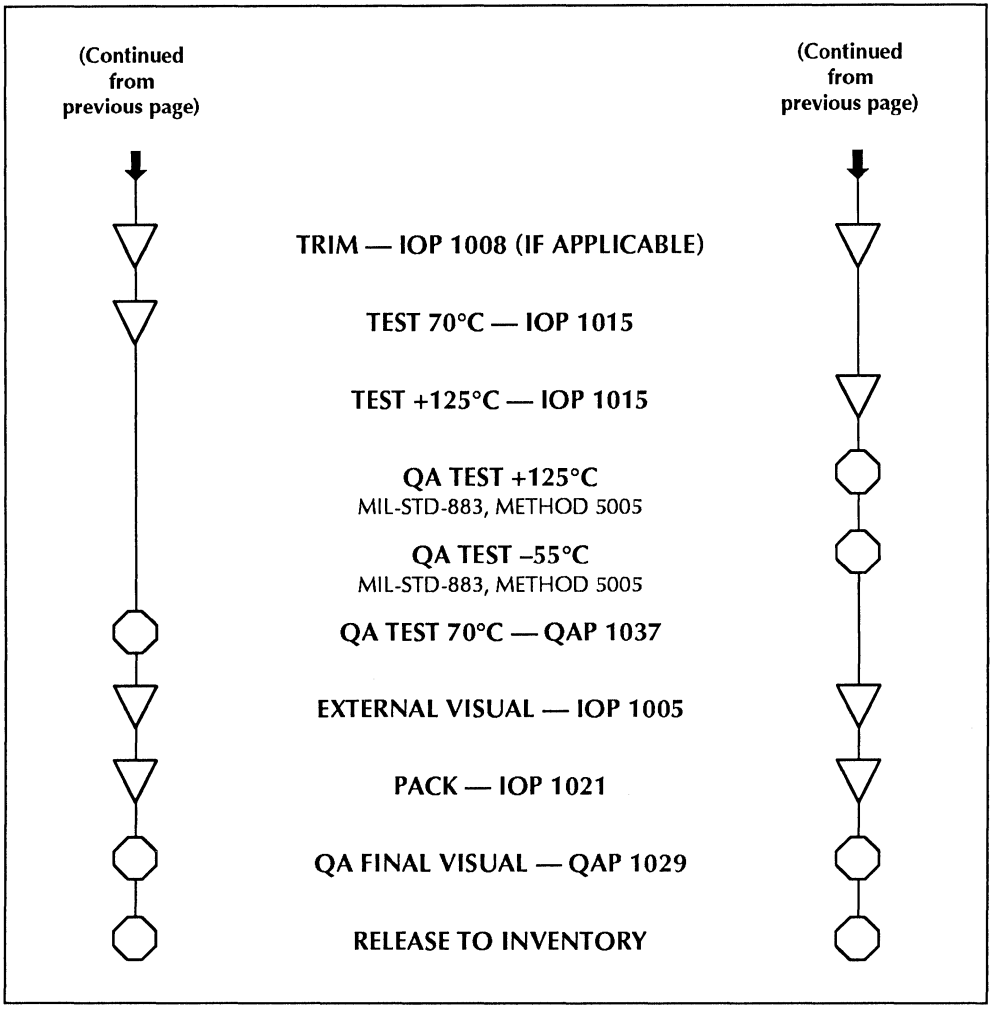


The following diagrams represent nominal process flows as of the date of issue. Specific details are available in Logic Devices Manufacturing Instructions.

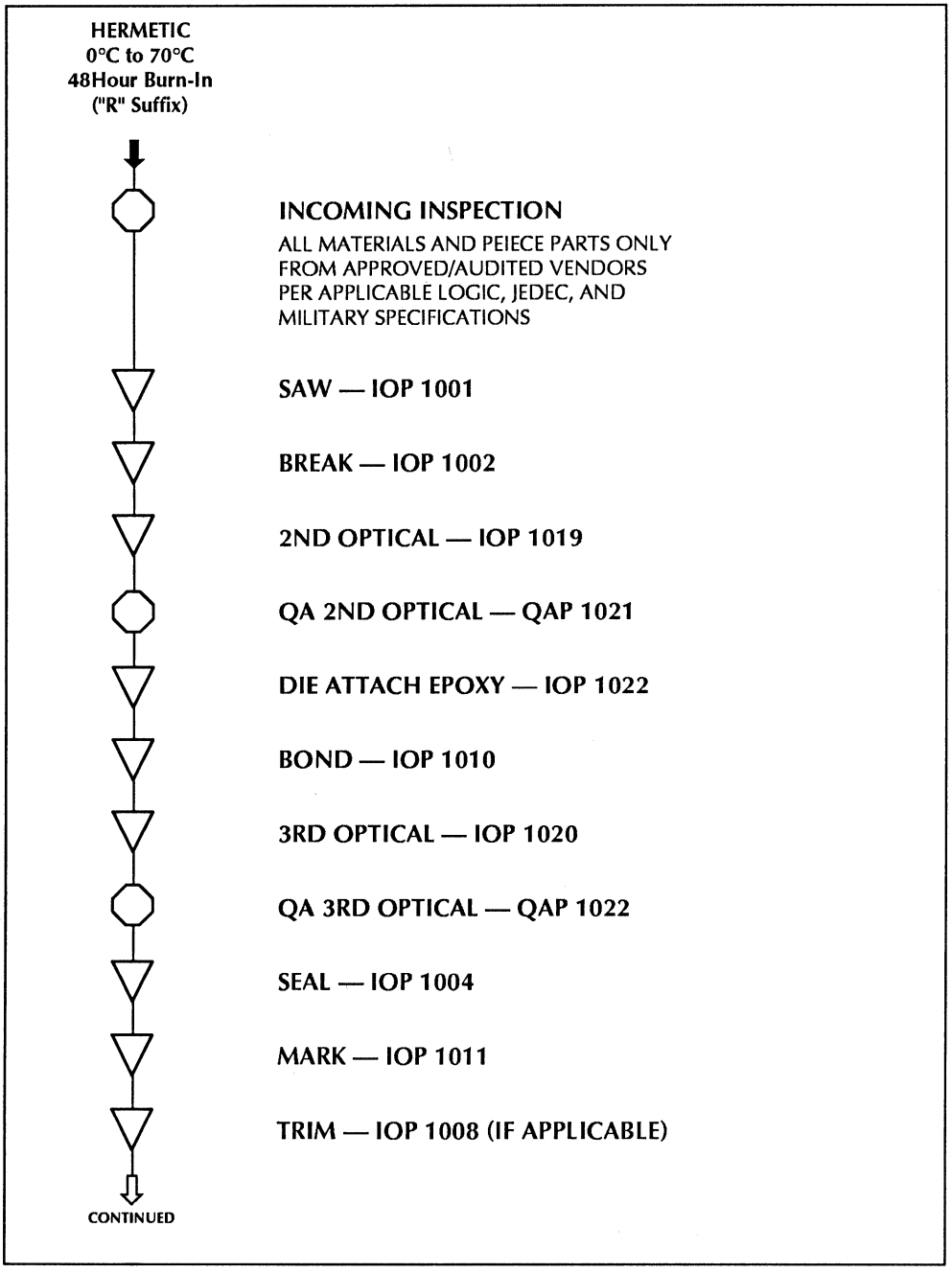

PLASTIC
0°C to 70°C
Commercial Screening
(No Suffix)
PLASTIC
0°C to 70°C
48 Hour Burn-In
("R" Suffix)
SAW
BREAK
2ND OPTICAL
QA 2ND OPTICAL
DIE ATTACH-EPOXY
CURE
WIRE BOND
3RD OPTICAL
QA 3RD OPTICAL
MOLD
POST MOLD CURE
DEFLASH — TRIM/FORM
SOLDER DIP
SINGULATION
CONTINUED
CONTINUED


(Continued from previous page)
(Continued from previous page)
MARK — IOP 1011
LOAD
FINAL VISUAL/PACK
SHIP TO LOGIC
LOGIC IQA — QAP 1039
TEST 70°C — IOP 1015
BURN-IN 48 HOURS — IOP 1013
TEST 70°C — IOP 1015
QA PDA — 7% MAX
QA TEST 70°C — QAP 1037
EXTERNAL VISUAL — IOP 1005
PACK — IOP 1021
QA FINAL VISUAL — QAP 1029
RELEASE TO INVENTORY


HERMETIC
0°C to 70°C
Commercial Screening
(No Suffix)
HERMETIC
–55°C to +125°C
Commercial Screening
(No Suffix)
INCOMING INSPECTION
ALL MATERIALS AND PEIECE PARTS ONLY
FROM APPROVED/AUDITED VENDORS
PER APPLICABLE LOGIC, JEDEC, AND
MILITARY SPECIFICATIONS
SAW — IOP 1001
BREAK — IOP 1002
2ND OPTICAL — IOP 1019
QA 2ND OPTICAL — QAP 1021
DIE ATTACH EPOXY — IOP 1022
BOND — IOP 1010
3RD OPTICAL — IOP 1020
QA 3RD OPTICAL — QAP 1022
SEAL — IOP 1004
TIN PLATE — CERDIP ONLY
MARK — IOP 1011
CONTINUED
CONTINUED


(Continued from previous page)
(Continued from previous page)
TRIM — IOP 1008 (IF APPLICABLE)
TEST 70°C — IOP 1015
TEST +125°C — IOP 1015
QA TEST +125°C
MIL-STD-883, METHOD 5005
QA TEST -55°C
MIL-STD-883, METHOD 5005
QA TEST 70°C — QAP 1037
EXTERNAL VISUAL — IOP 1005
PACK — IOP 1021
QA FINAL VISUAL — QAP 1029
RELEASE TO INVENTORY

5


HERMETIC
0°C to 70°C
48Hour Burn-In
("R" Suffix)
INCOMING INSPECTION
ALL MATERIALS AND PEIECE PARTS ONLY
FROM APPROVED/AUDITED VENDORS
PER APPLICABLE LOGIC, JEDEC, AND
MILITARY SPECIFICATIONS
SAW — IOP 1001
BREAK — IOP 1002
2ND OPTICAL — IOP 1019
QA 2ND OPTICAL — QAP 1021
DIE ATTACH EPOXY — IOP 1022
BOND — IOP 1010
3RD OPTICAL — IOP 1020
QA 3RD OPTICAL — QAP 1022
SEAL — IOP 1004
MARK — IOP 1011
TRIM — IOP 1008 (IF APPLICABLE)
CONTINUED

(Continued from previous page)

TEST 70°C — IOP 1015

BURN-IN 48 HOURS — IOP 1013

TEST 70°C — IOP 1015

QA PDA — 7% MAX

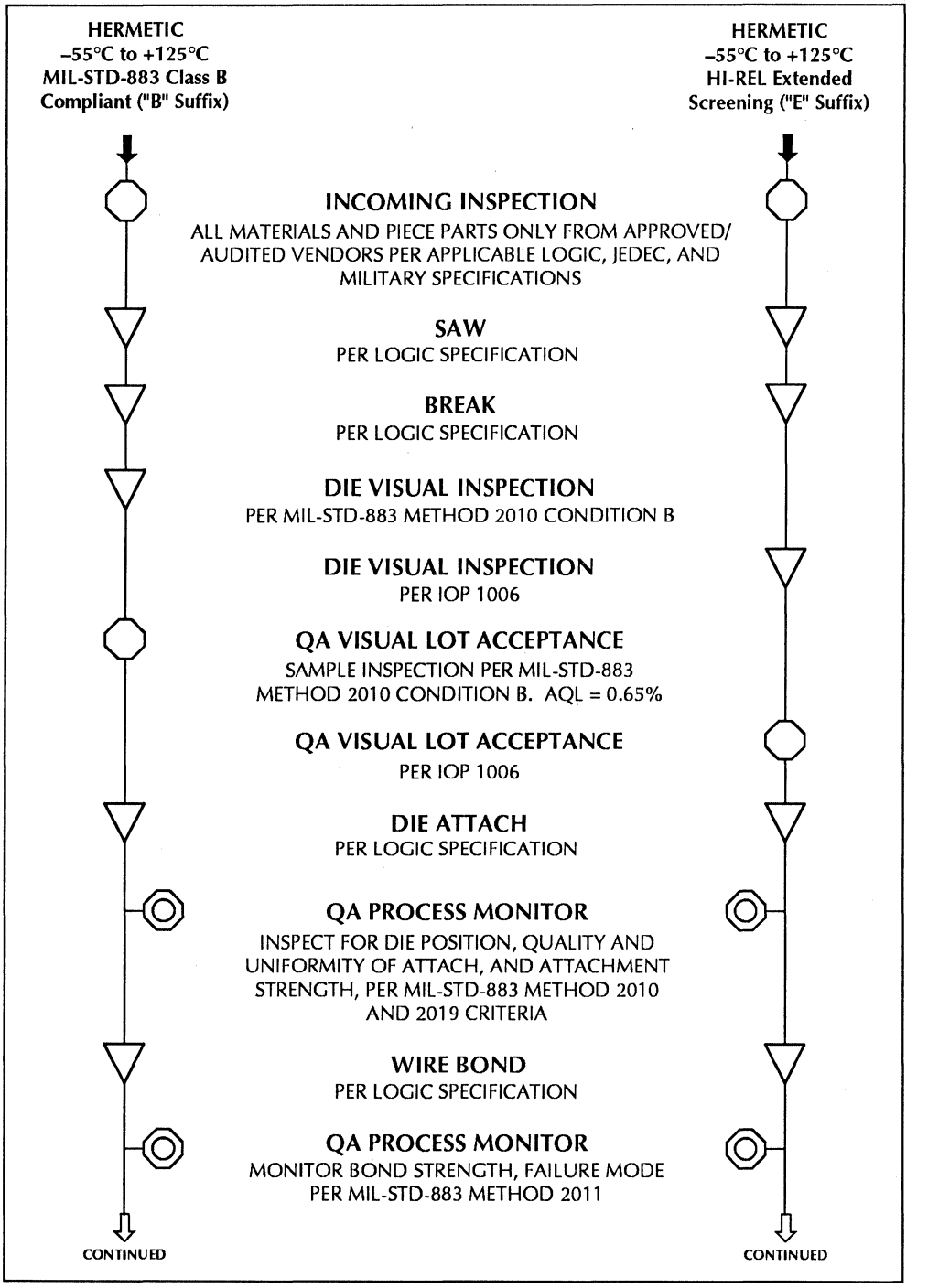
QA TEST 70°C — QAP 1037

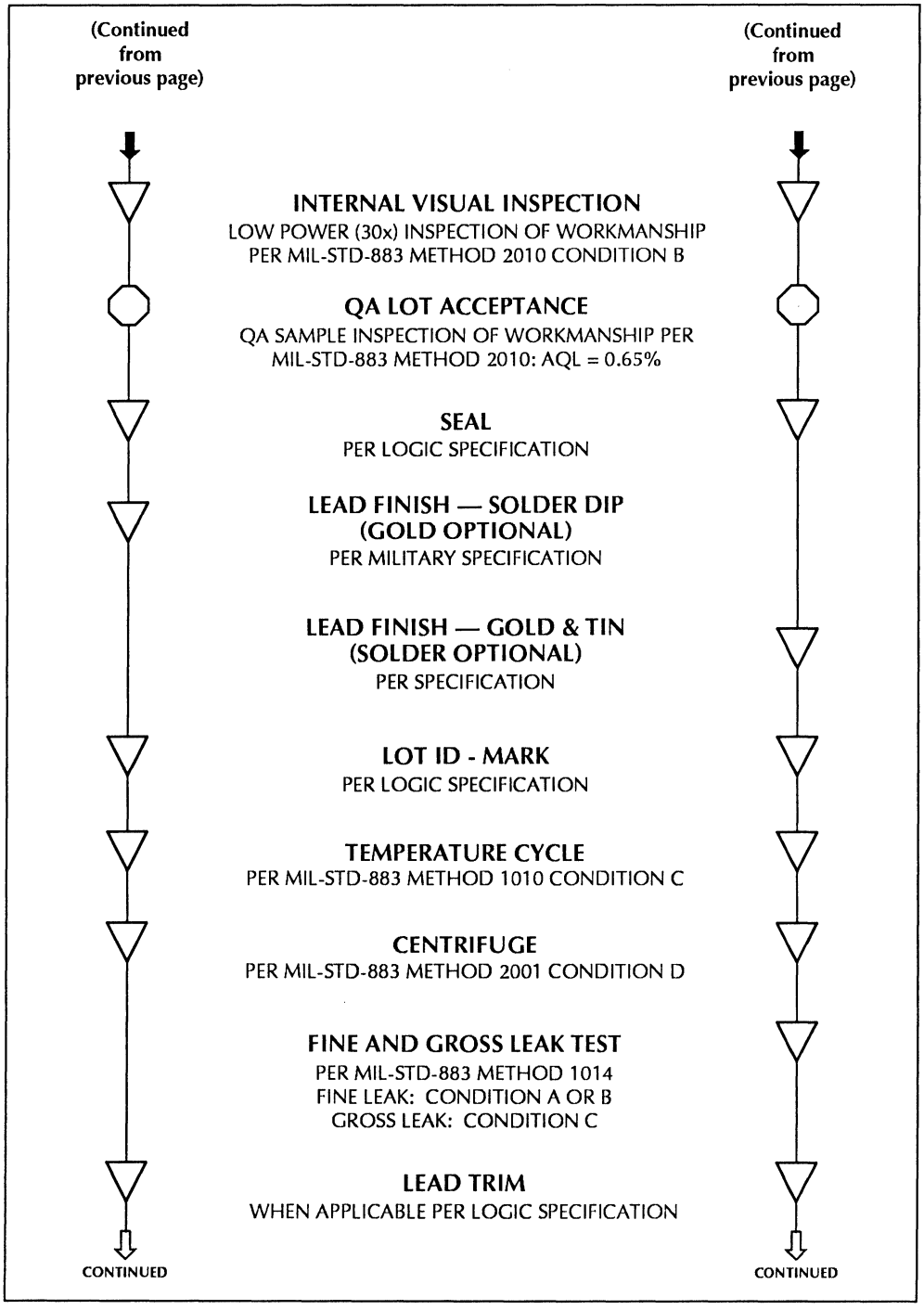
EXTERNAL VISUAL — IOP 1005

PACK — IOP 1021

QA FINAL VISUAL — QAP 1029

RELEASE TO INVENTORY


HERMETIC
–55°C to +125°C
MIL-STD-883 Class B
Compliant ("B" Suffix)
HERMETIC
–55°C to +125°C
HI-REL Extended
Screening ("E" Suffix)
INCOMING INSPECTION
ALL MATERIALS AND PIECE PARTS ONLY FROM APPROVED/ AUDITED VENDORS PER APPLICABLE LOGIC, JEDEC, AND MILITARY SPECIFICATIONS
SAW
PER LOGIC SPECIFICATION
BREAK
PER LOGIC SPECIFICATION
DIE VISUAL INSPECTION
PER MIL-STD-883 METHOD 2010 CONDITION B
DIE VISUAL INSPECTION
PER IOP 1006
QA VISUAL LOT ACCEPTANCE
SAMPLE INSPECTION PER MIL-STD-883 METHOD 2010 CONDITION B. AQL = 0.65%
QA VISUAL LOT ACCEPTANCE
PER IOP 1006
DIE ATTACH
PER LOGIC SPECIFICATION
QA PROCESS MONITOR
INSPECT FOR DIE POSITION, QUALITY AND UNIFORMITY OF ATTACH, AND ATTACHMENT STRENGTH, PER MIL-STD-883 METHOD 2010 AND 2019 CRITERIA
WIRE BOND
PER LOGIC SPECIFICATION
QA PROCESS MONITOR
MONITOR BOND STRENGTH, FAILURE MODE PER MIL-STD-883 METHOD 2011
CONTINUED
CONTINUED


(Continued from previous page)
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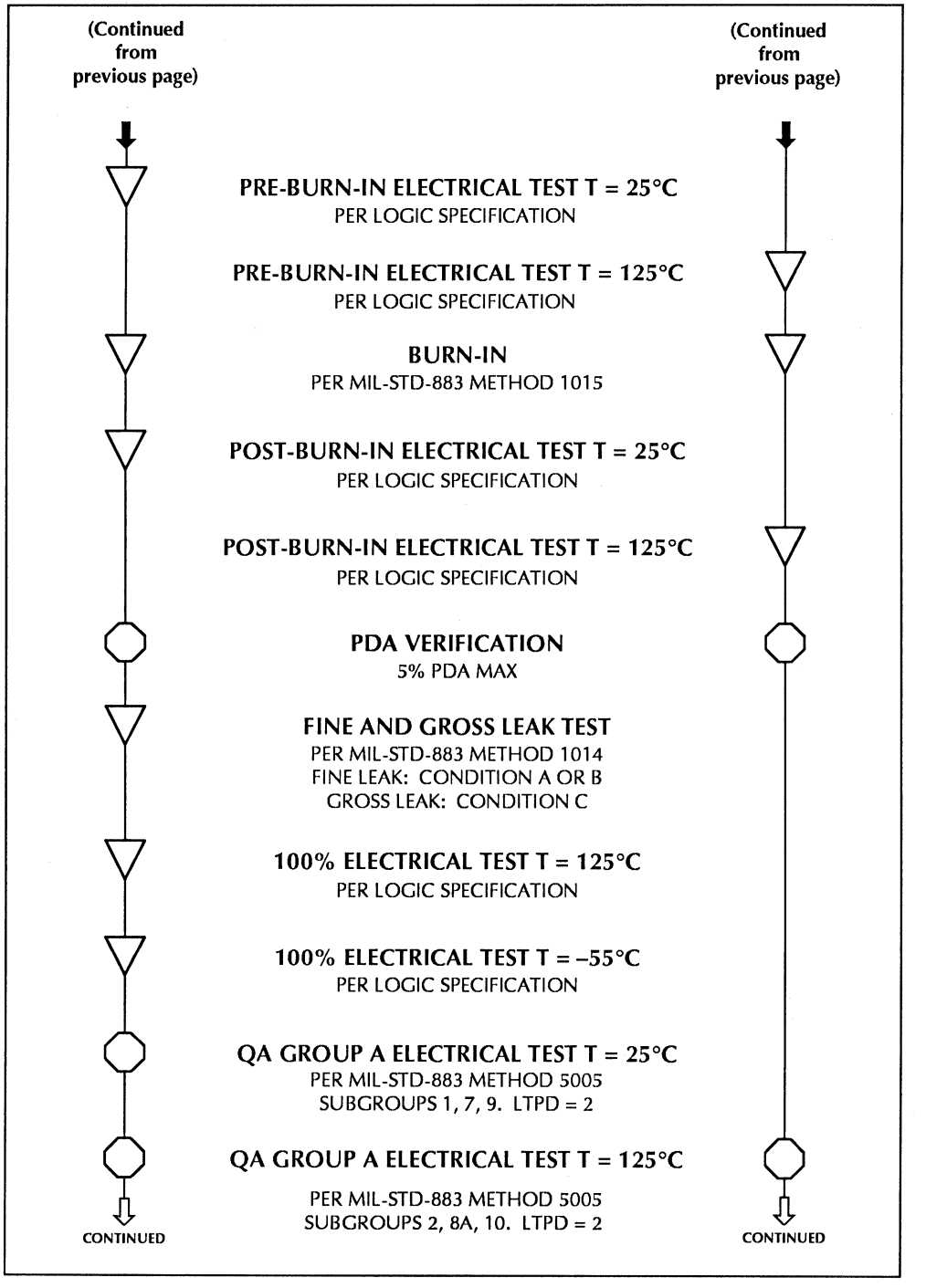
INTERNAL VISUAL INSPECTION
LOW POWER (30x) INSPECTION OF WORKMANSHIP PER MIL-STD-883 METHOD 2010 CONDITION B
QA LOT ACCEPTANCE
QA SAMPLE INSPECTION OF WORKMANSHIP PER MIL-STD-883 METHOD 2010: AQL = 0.65%
SEAL
PER LOGIC SPECIFICATION
LEAD FINISH — SOLDER DIP (GOLD OPTIONAL)
PER MILITARY SPECIFICATION
LEAD FINISH — GOLD & TIN (SOLDER OPTIONAL)
PER SPECIFICATION
LOT ID - MARK
PER LOGIC SPECIFICATION
TEMPERATURE CYCLE
PER MIL-STD-883 METHOD 1010 CONDITION C
CENTRIFUGE
PER MIL-STD-883 METHOD 2001 CONDITION D
FINE AND GROSS LEAK TEST
PER MIL-STD-883 METHOD 1014
FINE LEAK: CONDITION A OR B
GROSS LEAK: CONDITION C
LEAD TRIM
WHEN APPLICABLE PER LOGIC SPECIFICATION
CONTINUED
CONTINUED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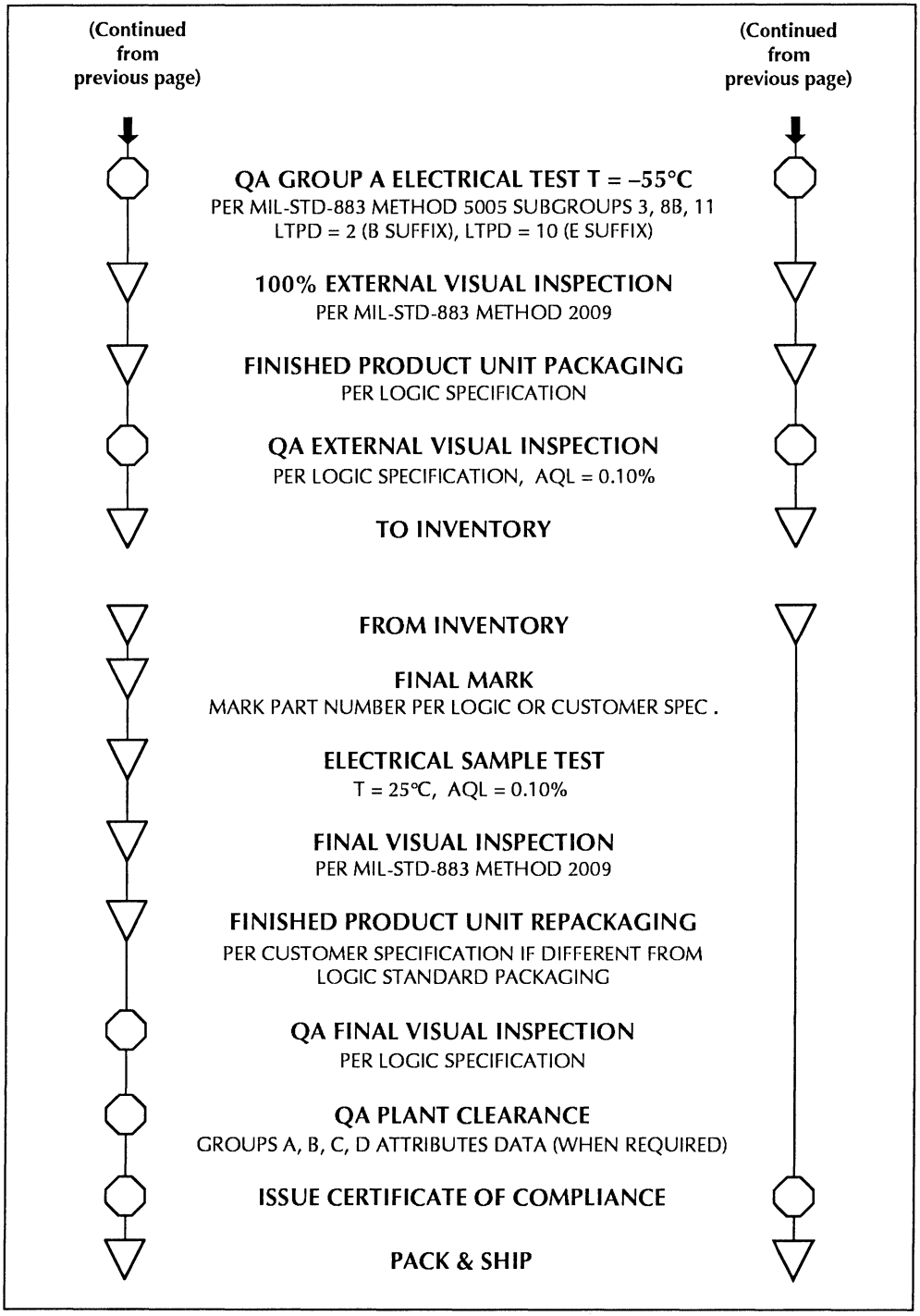
PRE-BURN-IN ELECTRICAL TEST T = 25°C
PER LOGIC SPECIFICATION
PRE-BURN-IN ELECTRICAL TEST T = 125°C
PER LOGIC SPECIFICATION
BURN-IN
PER MIL-STD-883 METHOD 1015
POST-BURN-IN ELECTRICAL TEST T = 25°C
PER LOGIC SPECIFICATION
POST-BURN-IN ELECTRICAL TEST T = 125°C
PER LOGIC SPECIFICATION
PDA VERIFICATION
5% PDA MAX
FINE AND GROSS LEAK TEST
PER MIL-STD-883 METHOD 1014
FINE LEAK: CONDITION A OR B
GROSS LEAK: CONDITION C
100% ELECTRICAL TEST T = 125°C
PER LOGIC SPECIFICATION
100% ELECTRICAL TEST T = –55°C
PER LOGIC SPECIFICATION
QA GROUP A ELECTRICAL TEST T = 25°C
PER MIL-STD-883 METHOD 5005
SUBGROUPS 1, 7, 9. LTPD = 2
QA GROUP A ELECTRICAL TEST T = 125°C
PER MIL-STD-883 METHOD 5005
SUBGROUPS 2, 8A, 10. LTPD = 2
CONTINUED
CONTINUED


(Continued from previous page)
(Continued from previous page)
QA GROUP A ELECTRICAL TEST T = –55°C
PER MIL-STD-883 METHOD 5005 SUBGROUPS 3, 8B, 11
LTPD = 2 (B SUFFIX), LTPD = 10 (E SUFFIX)
100% EXTERNAL VISUAL INSPECTION
PER MIL-STD-883 METHOD 2009
FINISHED PRODUCT UNIT PACKAGING
PER LOGIC SPECIFICATION
QA EXTERNAL VISUAL INSPECTION
PER LOGIC SPECIFICATION, AQL = 0.10%
TO INVENTORY
FROM INVENTORY
FINAL MARK
MARK PART NUMBER PER LOGIC OR CUSTOMER SPEC .
ELECTRICAL SAMPLE TEST
T = 25°C, AQL = 0.10%
FINAL VISUAL INSPECTION
PER MIL-STD-883 METHOD 2009
FINISHED PRODUCT UNIT REPACKAGING
PER CUSTOMER SPECIFICATION IF DIFFERENT FROM LOGIC STANDARD PACKAGING
QA FINAL VISUAL INSPECTION
PER LOGIC SPECIFICATION
QA PLANT CLEARANCE
GROUPS A, B, C, D ATTRIBUTES DATA (WHEN REQUIRED)
ISSUE CERTIFICATE OF COMPLIANCE
PACK & SHIP

LOGIC

Contents

6

Latchup and ESD Protection

Latchup is a destructive phenomenon which was once common in CMOS circuits but has now been largely eliminated by improved circuit design techniques. Latchup takes place because of the existence in CMOS of an inherent p/n/p/n or n/p/n/p structure between V_{CC} and ground. Either of these two can form a pair of transistors connected so as to form a positive feedback loop, with the collector of one transistor driving the base of the other. The result is a low-impedance path from V_{CC} to ground, which cannot be interrupted except by the removal of power. This condition can be destructive if the area involved is sufficiently large to dissipate excessive power. One example of the formation of such a structure is shown in Fig. 1. The equivalent circuit is shown in Fig. 2.

As shown in Fig. 1, the n+ regions which form the source and drain of an n-channel MOS transistor, also act as the emitters of a parasitic npn transistor. The p-well forms the base region, and the n-substrate is the collector. The current gain of this transistor is relatively high because it is formed vertically and therefore the base width is quite small. This is especially true of fine-geometry CMOS processes which tend to have very shallow wells to reduce sidewall capacitance. The p+ region in the well is called a well tap, and is present to form a low-resistance connection between the well and ground. The source region cannot serve this function because it forms a diode between the n+ source and the p-well.

Also shown in Fig. 1 is an additional parasitic pnp transistor. The source and drain regions of the p-channel MOS device form the emitters, the n-substrate is the base, and the p-well is the collector. This transistor is a pnp, and generally has a beta much less than 1 since it is formed laterally and the gate region is relatively large. Like the vertical npn, it can have multiple emitters. The n+ region tied to V_{CC} in the substrate functions similarly to the well tap discussed above.

Note that the base of the npn and the collector of the pnp are a common region (the p-well), and similarly the base of the pnp and the collector of the npn are common (the n-substrate). Thus, the pnpn structure necessary for latchup is formed. Also, due to the the physical distance between the well and substrate taps and the base regions which they attempt to contact, a small resistance exists between the base regions and their respective well taps, denoted R_S (substrate) and R_W (well).

Latchup begins when a perturbation causes one of the bipolar transistors to turn on. An example would be excursion of the output pad below ground or above V_{CC} due to transmission-line ringing. If the pad goes more than 0.7 V below ground, the npn will turn on since its base is at approximately ground potential. The npn's collector current will cause a voltage drop across R_S, the bulk substrate resistance. This voltage drop turns on the pnp.

The pnp transistors' collector current forces a similar voltage drop across R_W, the well resistance. This raises the base voltage of the npn above ground, and can cause the npn to continue to conduct even after the output pad returns to a normal voltage range. In this case, the current path shifts to the grounded emitter.

Note that any effect which can cause a transient turn-on of either transistor can cause the latchup process. Common causes include:

1. Ringing of unprotected I/O pins outside the ground to V_{CC} region.
2. Radiation-induced carriers generated in the base of the bipolar transistors.
3. Hot-powerup of the device, with inputs driven high before V_{CC} is applied.
4. Electrostatic discharge.

Protecting Against Latchup

Latchup, while once a severe problem for CMOS, is now a relatively well-understood phenomenon. In order for latchup to occur, the product of the current gains of the two parasitic transistors must exceed 1. Thus, the primary means for avoiding latchup is the insertion of structures known as "guard rings" around all MOS

Figure 1. Parasitic transistor structures in parallel CMOS.

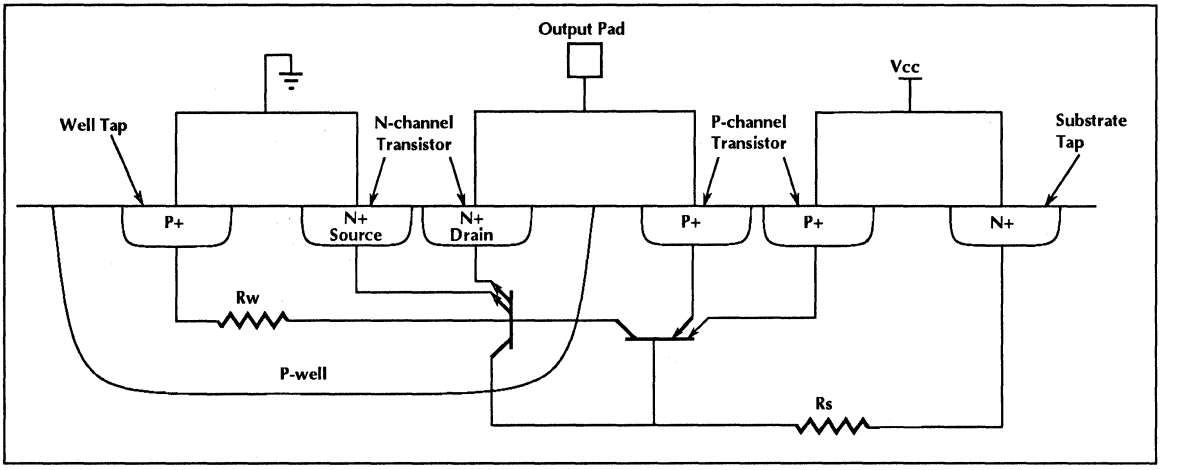
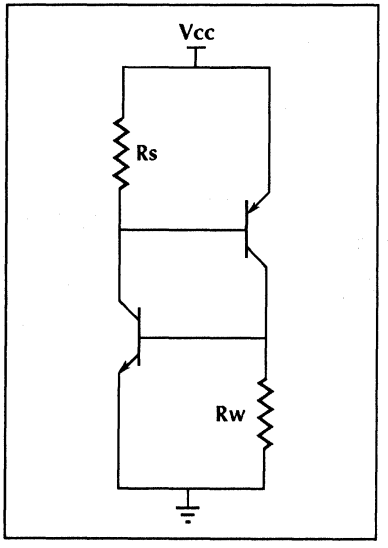


Figure 2. Equivalent circuit for Latchup path.



transistors (and other structures) likely to be subjected to latchup-causing transients. This includes output buffer transistors and any devices which form a part of the ESD protection network. These guard rings absorb current which would otherwise drive the base of the lateral device, and thus dramatically reduce its gain.

Since external electrical perturbations are the dominant cause of latchup in non-radiation environments, protecting the "periphery" of the chip is most important. Therefore, since guard rings require a lot of area, they are generally used only in critical areas such as those mentioned above.

As an additional protective measure, strict rules are enforced in the layout regarding the positioning of the substrate and well taps. They are spaced closely together throughout the die, reducing the values of Rs and Rw. This makes it more difficult to develop the base drive necessary to regenerate the latchup condition.

Measurement of susceptibility to latchup is done by connecting a current source to an input or output of the device under test. By increasing the current forced to flow into the pin and noting the point at which latchup occurs, a measure of the device's ability to resist latchup-inducing carrier injection is obtained. Note that depending on the device, the current source may require a rather large voltage compliance in order to provide an adequate test.

While early CMOS devices had a latchup trigger current of a few tens of milliamps, most current Logic Devices products typically can withstand more than 1 amp without latching. As a result, latchup is no longer a practical concern, except for extreme conditions such as driving multiple inputs high with a low-impedance source during powerup of the device.

Electrostatic Discharge

Input protection structures on CMOS devices are used to protect against damage to the gate oxides of input transistors when accumulated static charge is discharged through a device. This charge can often reach potentials of several thousand volts. The input protection network is designed to shunt this charge safely to ground or Vcc, bypassing the delicate MOS transistors.

Several features are required of a good input protection network. Since static discharge pulses exhibit very fast risetimes, it must have a very fast turnon time. It must be capable of carrying large instantaneous currents without damage. It must prevent the voltage at the circuit input from rising above about 10 V during the time when the several-thousand-volt discharge is shunted to ground. It must not create appreciable delay for fast edges which are within the 0–5 V input range. And finally, it must be well protected against latchup caused by inputs which are driven beyond the supply rails, injecting current into the substrate. Much research and experimentation has been devoted to optimizing the tradeoffs between these conflicting goals.

All Logic Devices products employ one of three input protection structures shown in Fig. 3. Most devices currently use the Type 1 input protection. This structure is designed to absorb very high static discharge energies and will draw substantial current from the input pin if driven beyond either supply rail. Hence, it provides a "hard" clamp. Besides its advantages for static protection, this clamp can effectively reduce undershoot energy, preventing oscillation of an unterminated input back above the 0.8 V Vil MAX level. This makes the circuit ideal for noisy environments and ill-behaved signals. This input structure may not be driven to a high level without power applied to the device, however. To do so would result in current flowing through the diode connected to the devices' Vcc rail, and supplying power to the entire board or system backward through the device Vcc pin. This may overstress the bond wire or device metallization, resulting in failure.

The Type 2 structure employs a series resistor prior to the two clamp diodes. This results in a "soft" clamping effect. This structure will withstand the transient application of voltages outside the supply rails for brief periods without drawing excessive current. In contrast to the Type 1 structure, this circuit will provide only a modest reduction of the energy in an undershoot pulse. It is somewhat more tolerant of power-up sequences which cause the inputs to be driven before Vcc is applied, however. In the course of routine product upgrades, devices employing this structure are being redesigned to use a Type 1 input protection.

The Type 3 structure uses a large area N-channel transistor (part of an open-drain output buffer) to protect the input. The drain-well junction of this device serves the function of a diode connected between the input and ground, protecting against negative excursions of the input. The avalanche breakdown of the output device serves to protect against positive pulses, giving the effect of a zener diode between the input and ground. This circuit is used only for inputs which are designed to have their inputs driven without power applied. The lack of a diode to Vcc prevents sourcing of power from the inputs to the Vcc supply.

Table 1 gives Latchup figures for the three input protection structures used in Logic Devices products. Table 2 indicates the input structure used for each part type.

6

Figure 3. Input protection devices.

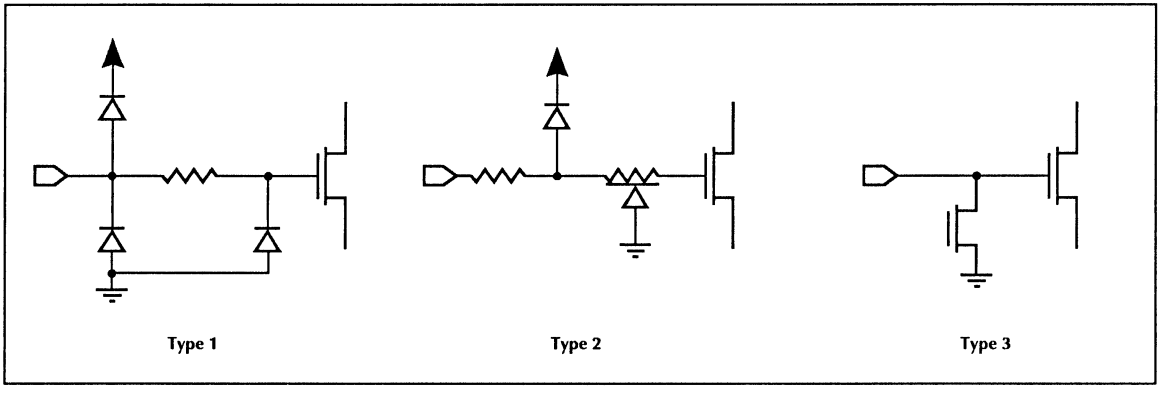


Table 1. Latchup immunity.

Structure	Latchup Current Immunity	
	Min	Typ
Type 1	400 mA	1000 mA
Type 2	150 mA	250 mA
Type 3	400 mA	1000 mA

Table 2. Input structure list by part number.

Device	Input Structure	Device	Input Structure
Multipliers/Multiplier Accumulators		**Register Files**	
LMU08/8U	Type 1	LRF07	Type 2
LMU557/558	Type 1	LRF08	Type 2
LMU12/112	Type 1	**Peripheral Products**	
LMU16/216	Type 1	L5380	Type 1,3
LMU17/217	Type 1	L53C80	Type 1,3
LMU18	Type 1	**16K Static RAMS**	
LMA1009/2009	Type 1	L7C167	Type 1
LMA1010/2010	Type 1	L7C168/170	Type 1
LMS12	Type 1	L7C171/172	Type 1
Arithmetic/Logic Units		L6116	Type 1
L4C381	Type 1	**64K Static RAMS**	
L29C101	Type 1	L7C187	Type 1
Special Functions		L7C164/165/166	Type 1
LSH32	Type 2	L7C161/162	Type 1
L10C23	Type 1	L7C185	Type 1
Pipeline Registers			
L29C520/521	Type 1		
LPR520/521	Type 2		

Power Dissipation in Logic Devices Products

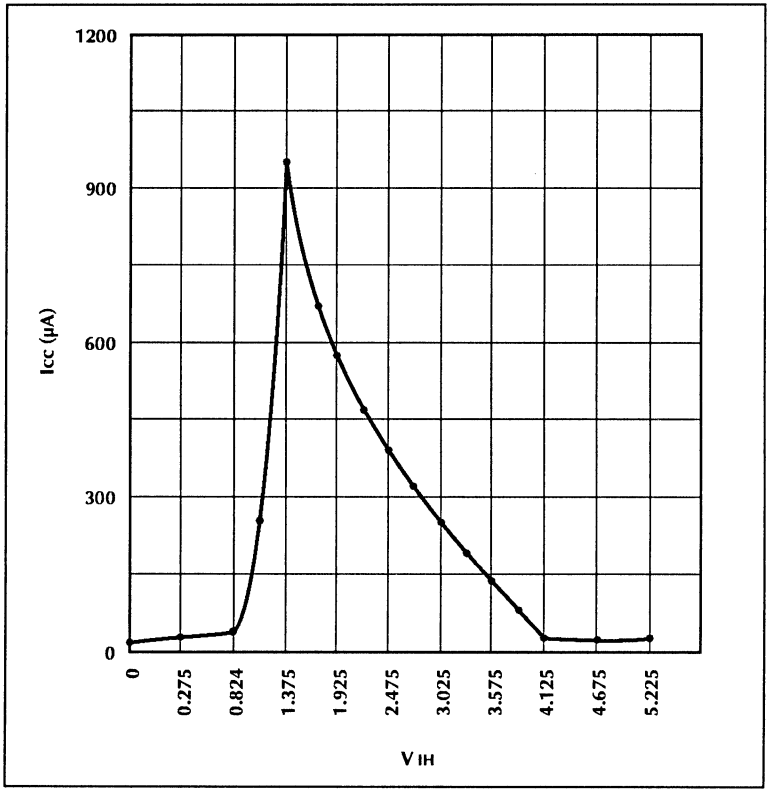
In calculating the power dissipation of Logic Devices products, attention must be given to a number of formerly second-order effects which were generally ignored when dealing with bipolar and NMOS technologies. By far the dominant contributor to power dissipation in most CMOS devices is the effective current path from the supply to ground, created by the repetitive charging and discharging of the load capacitance. This is distinct from DC loading effects, which may also consume power. The power dissipated in the load capacitance is proportional to CV^2F, where C is the load capacitance, V is the voltage swing, and F is the switching frequency. This mechanism can frequently contribute 80% or more of the total device dissipation of a truly complementary device operating at a high clock rate.

The second contributor to the power dissipation of a CMOS device is the DC current path between V_{CC} and ground present in the input level translators. These circuits are voltage amplifiers which are designed to convert worst case 0.8–2.0 V TTL-compatible input levels to 0 and 5 V internal levels. With 2.0 V applied to the input of most level translator circuits, about 1 mA will flow from the power supply to ground. A floating input will at best have similar results, and may result in oscillations which can dissipate orders of magnitude more power and cause malfunctioning of the device.

The power dissipation of input level translators exhibits a strong peak at about 1.4 V, but is reduced substantially when the input voltage exceeds 3.0 V (see Fig. 1). Fortunately, this voltage is easy to achieve in practice, even for bipolar devices with TTL I/O structures. These generally will produce a V_{OH} of at least 3.5 V if not fully loaded. As a result, dissipation in the input structures is usually negligible compared to other sources.

Two further sources of power dissipation in CMOS come from the core logic. The sources of internal power dissipation are the same as those

Figure 1.



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discussed for external nodes, namely repetitive charging of the parasitic load capacitances on each gate output, and the power drawn due to a direct current path to ground when gate input voltage levels transition through the linear region. In practice, the internal voltage waveforms are characterized by high edge rates and rail-to-rail swings. For this reason, the latter source of dissipation is usually negligible, unless NMOS or other non-complementary logic design techniques have been used.

The capacitance of typical internal nodes in CMOS logic circuits are a few femtofarads. However, there can be thousands, or tens of thousands of such nodes. As a result, the core power dissipation is strongly dependent on the average rate at which these nodes switch (the "F" in CV^2F). Fortunately, for most complex logic circuits, with non-pathological external stimulus only a small fraction of the logic nodes switch on any given cycle. For this reason, internal power is generally quite small for these device types. Exceptions include devices containing long shift registers or other structures which can exhibit high duty cycles on most internal nodes. These devices can dissipate significant power in the core logic if stimulated with alternating data patterns and clocked at a high rate.

To summarize, of the several contributors to power dissipation, the CV^2F power of the outputs is usually dominant. Because output loading is system-dependent, it is not possible for the manufacturer to accurately predict total power dissipation in actual use. As a result, Logic Devices extrapolates measured power dissipation values to a zero-load environment, and publishes the resulting value. This value includes the effects of worst-case input and power-supply voltages, temperature, and stimulus pattern, but not CV^2F. This value is weakly frequency dependent, and the frequency at which it is measured is published in the device data sheet. The maximum value is for worst-case pattern, and the typical is for a more random pattern and is therefore more representative of what would be experienced in actual practice.

A good estimate of total power dissipation in a particular system under worst-case conditions can be obtained by adding the calculated output power to the *typical* published figure. The output power is given by:

$$\frac{N}{2}\left(CV^2\frac{F}{2}\right)$$

where:

- N = the number of device outputs (divided by 2 to account for the assumption that on average half of the outputs switch on any given cycle)
- C = the output load capacitance, per pin, given in Farads
- V = the power supply voltage
- F = the clock frequency (divided by 2 to account for the fact that a registered output can at most switch at only half the clock rate).

A less pessimistic estimate, appropriate for complex devices when reasonable input voltage levels and non-pathological patterns can be expected, would neglect the published value and use only the calculated value as given above.

LOGIC DEVICES INCORPORATED

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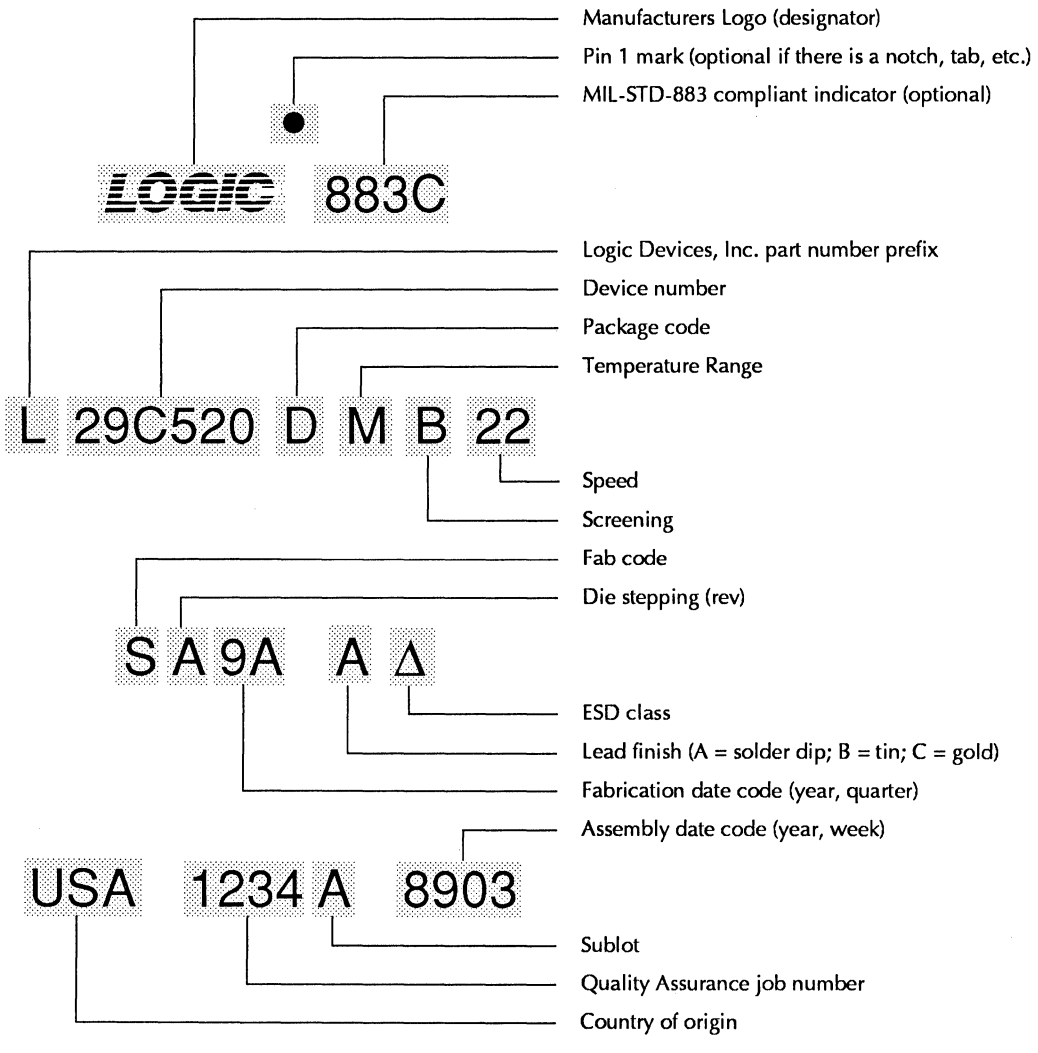
Product Marking Guide



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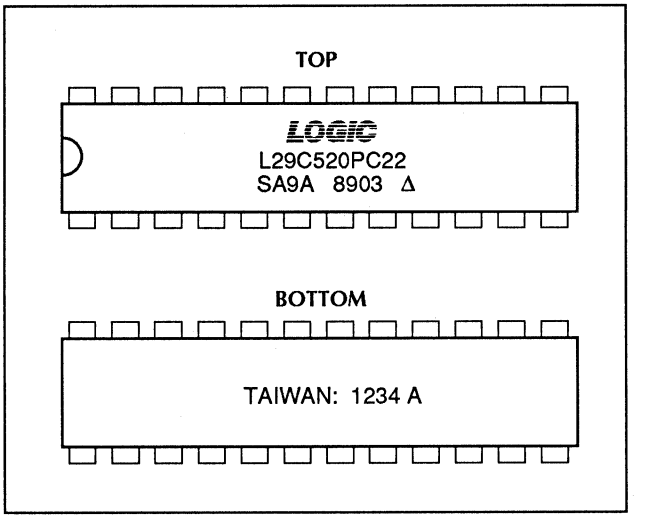
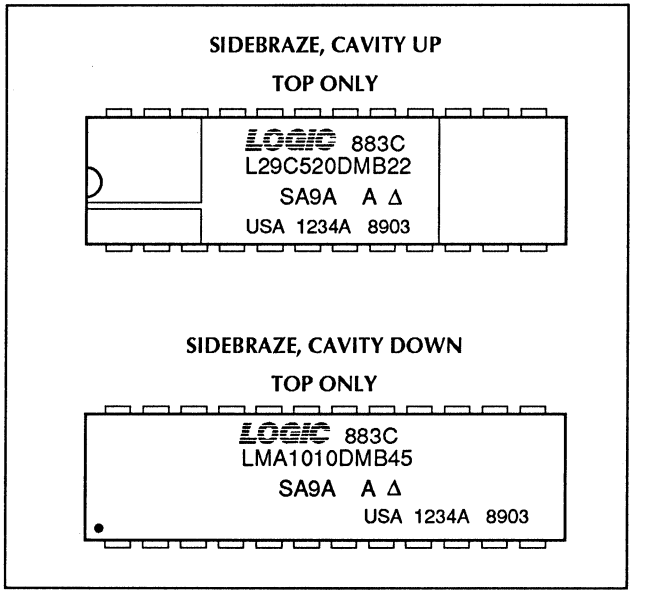
Plastic Package Marking (Plastic DIP, SOIC, SOJ, PLCC)

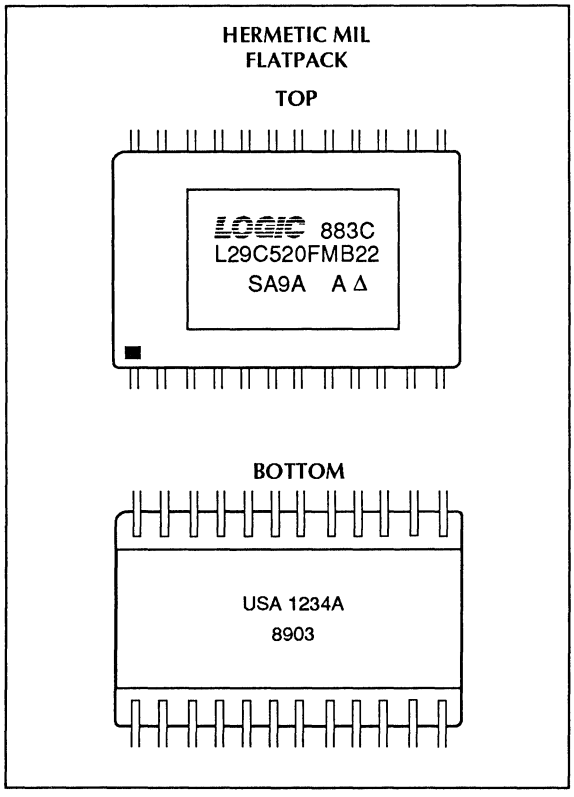


Sidebraze Hermetic Package Marking

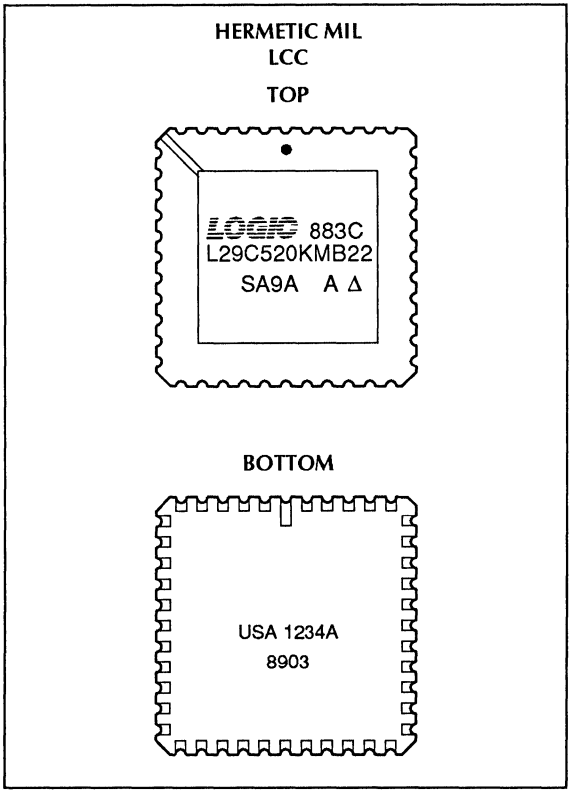


NOTE: Package marking may vary due to space limitations.

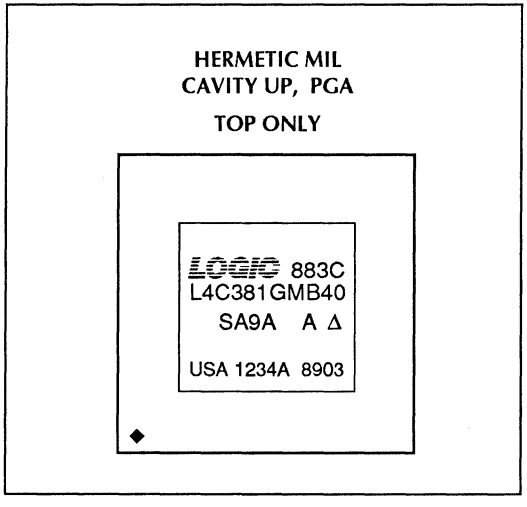
Flatpack Package Marking



Leadless Chip Carrier Package Marking



Pin Grid Array Package Marking

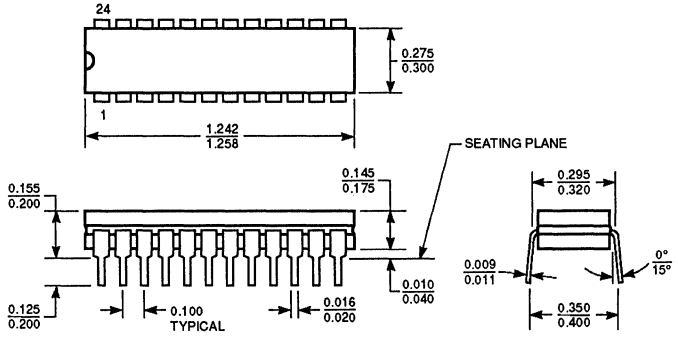


NOTE: Package marking may vary due to space limitations.

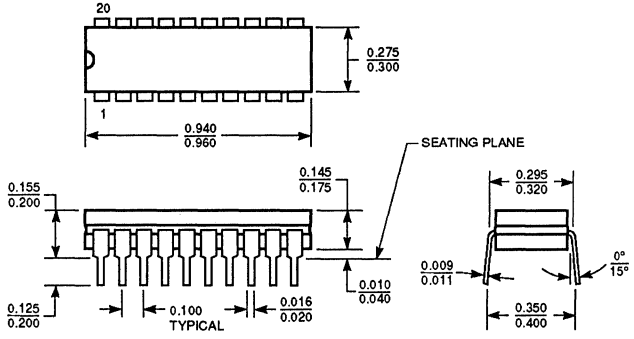
Mechanical Drawings

CerDIP — Type C

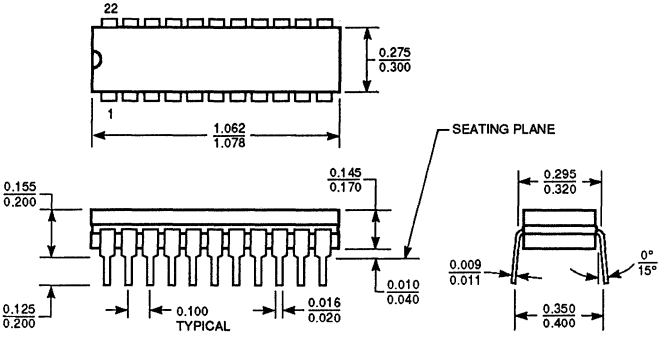
C1 — 24-Pin CerDIP



C2 — 20-Pin CerDIP

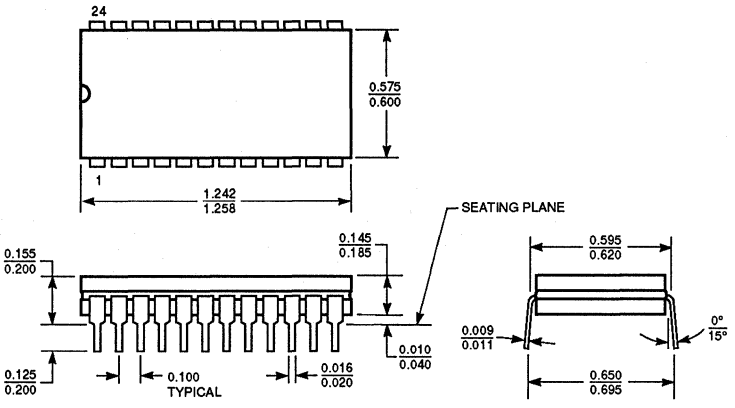


C3 — 22-Pin CerDIP

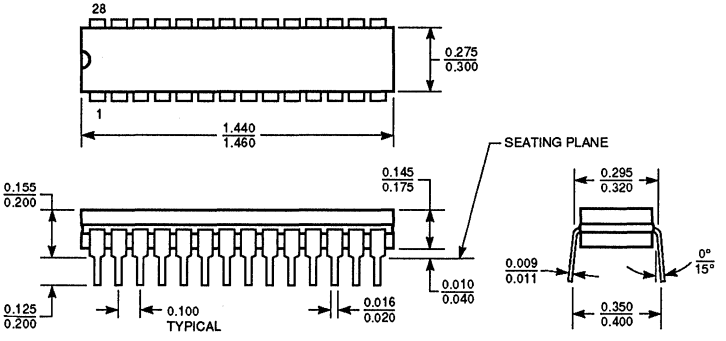


CerDIP — Type C

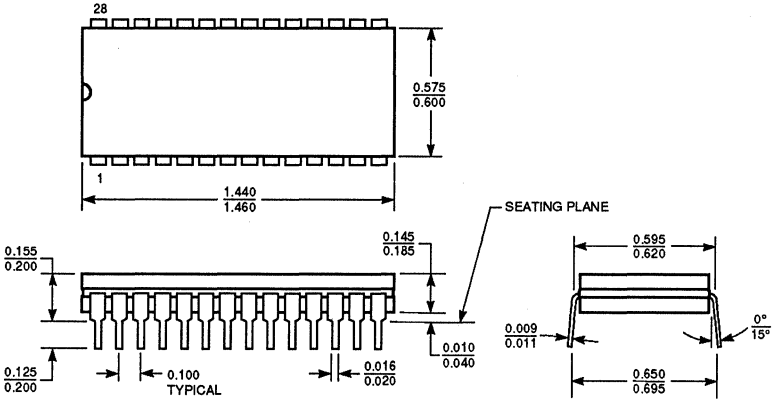
C4 — 24-Pin CerDIP



C5 — 28-Pin CerDIP

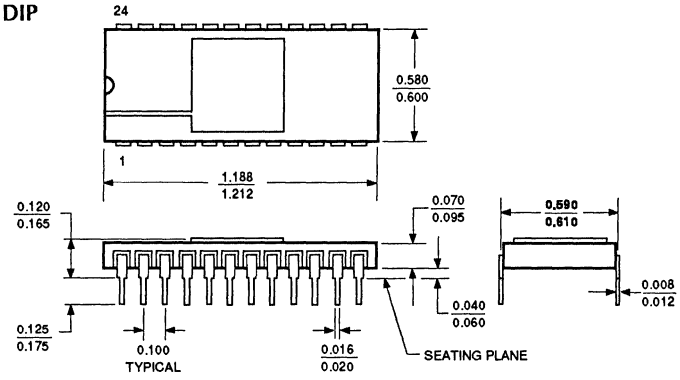


C6 — 28-Pin CerDIP

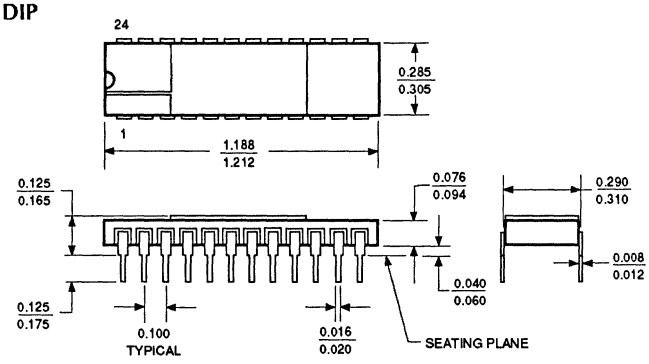


Sidebraze, Hermetic DIP — Type D

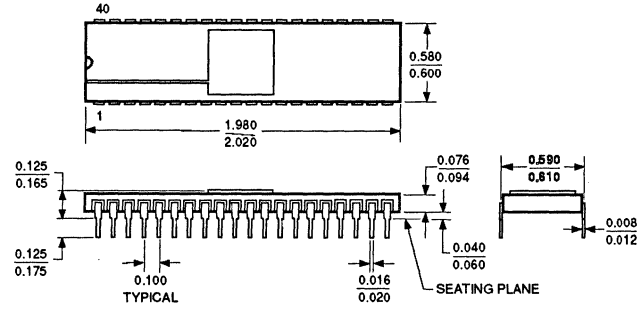
D1 — 24-Pin Hermetic DIP



D2 — 24-Pin Hermetic DIP



D3 — 40-Pin Hermetic DIP



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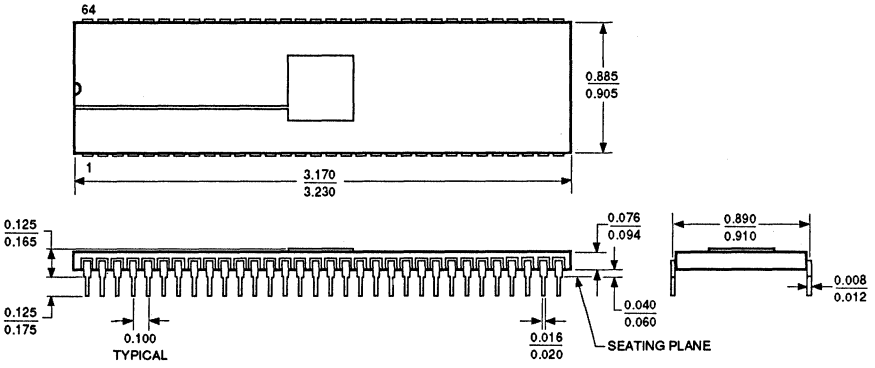
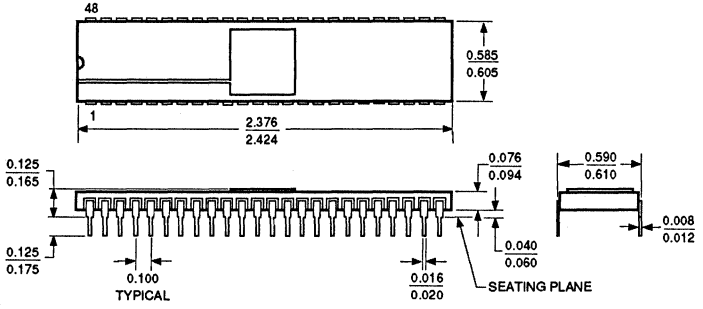
Sidebraze, Hermetic DIP — Type D

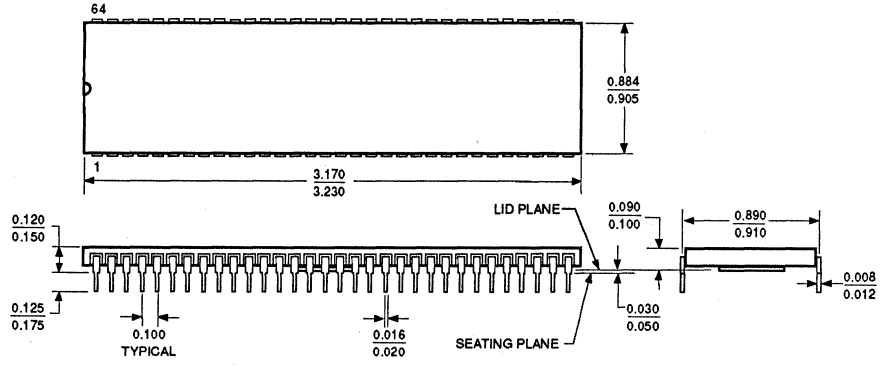
D4 — 64-Pin Hermetic DIP



D5 — 48-Pin Hermetic DIP

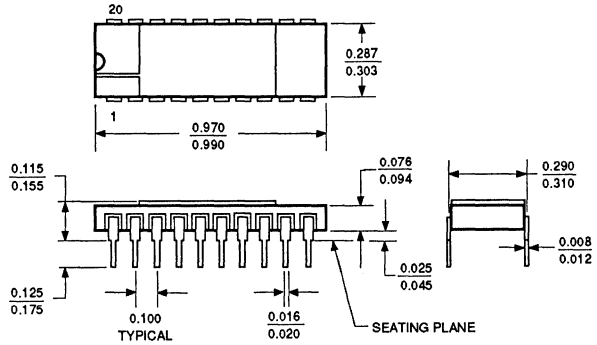


D6 — 64-Pin Hermetic DIP (Cavity Down)

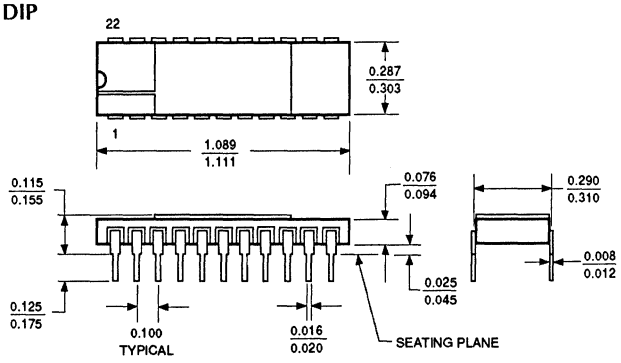


Sidebraze, Hermetic DIP — Type D

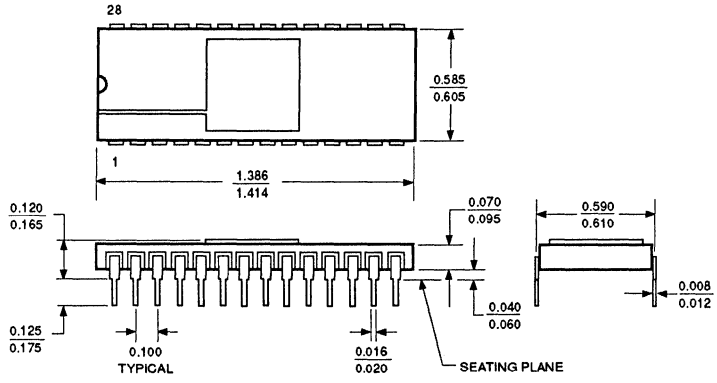
D7 — 20-Pin Hermetic DIP



D8 — 22-Pin Hermetic DIP



D9 — 28-Pin Hermetic DIP



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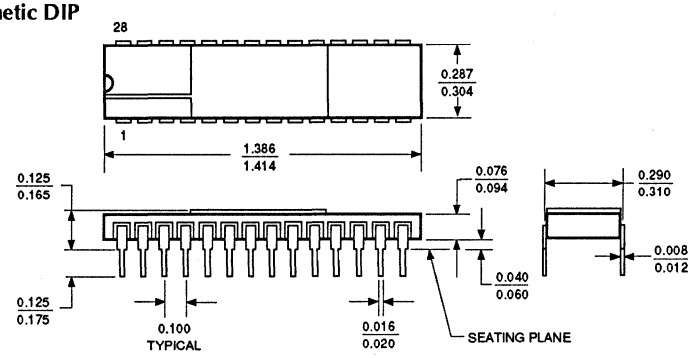
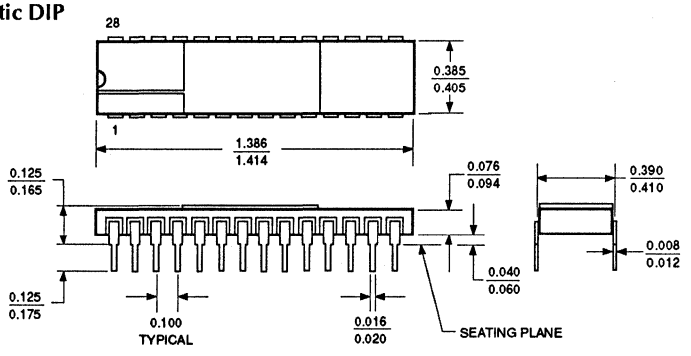
Sidebraze, Hermetic DIP — Type D

D10 — 28-Pin Hermetic DIP

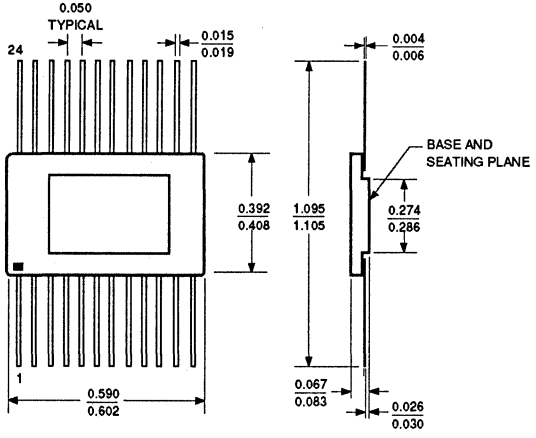


D11— 28-Pin Hermetic DIP



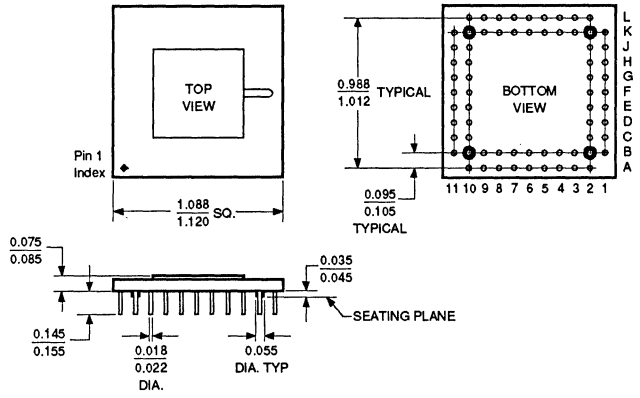
Ceramic Flat Pack — Type F

F1 — 24-Pin Ceramic Flat Pack

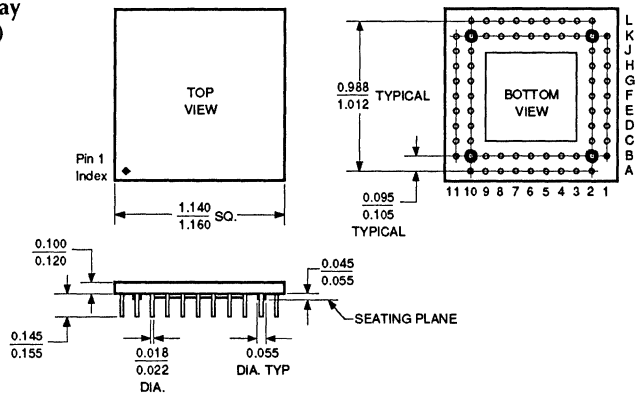


Ceramic Pin Grid Array — Type G

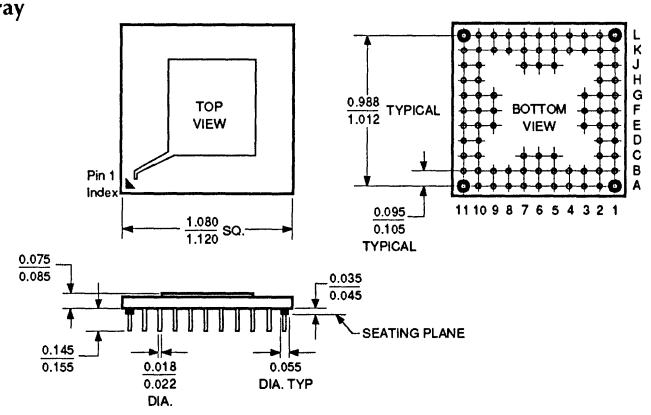
G1 — 68-Pin Grid Array



G2 — 68-Pin Grid Array (Cavity Down)



G3 — 84-Pin Grid Array



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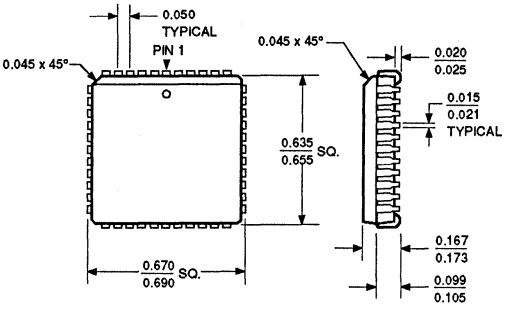
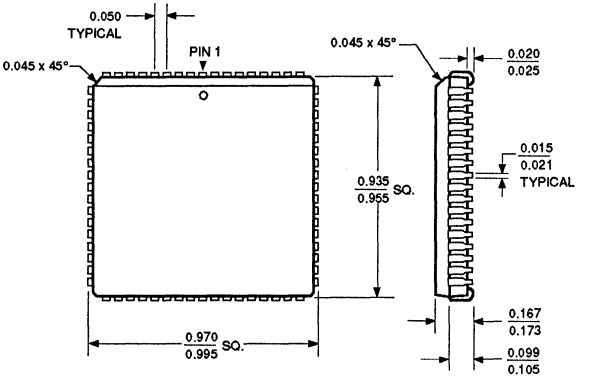
Plastic J-Lead Chip Carrier — Type J

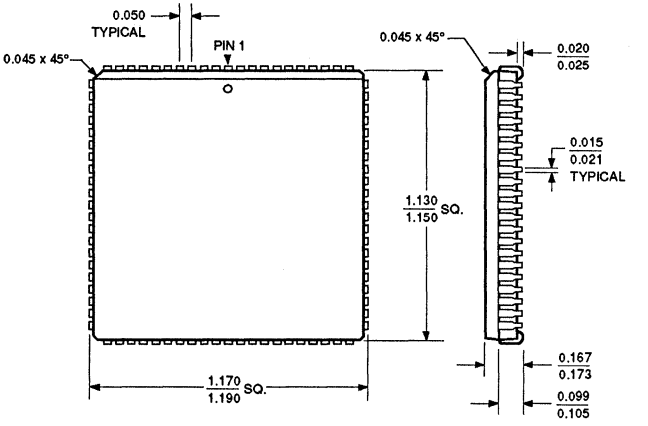
J1 — 44-Pin Plastic J-Lead



J2 — 68-Pin Plastic J-Lead

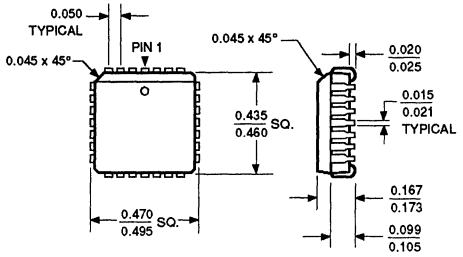


J3 — 84-Pin Plastic J-Lead

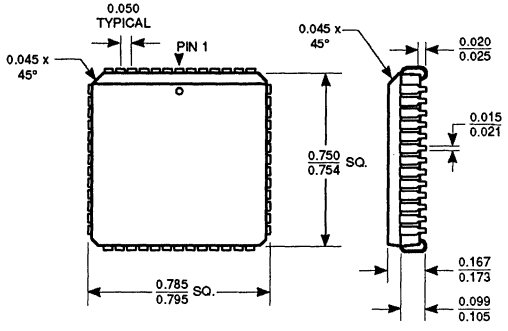


Plastic J-Lead Chip Carrier — Type J

J4 — 28-Pin Plastic J-Lead



J5 — 52-Pin Plastic J-Lead



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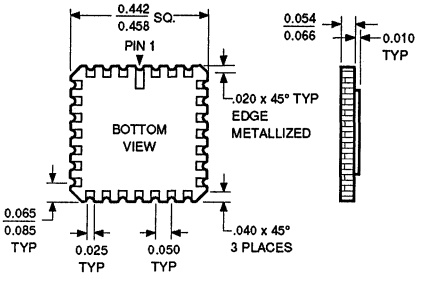
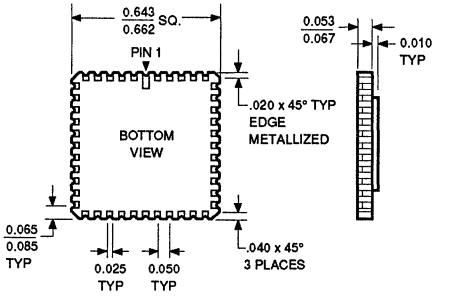
Ceramic Leadless Chip Carrier — Type K

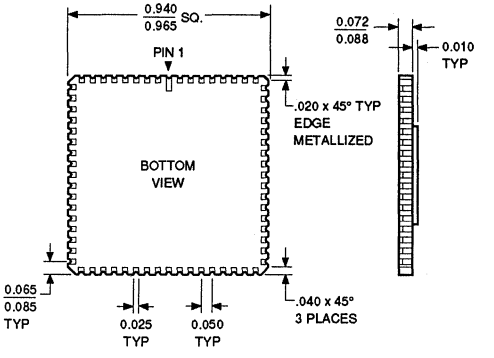
K1 — 28-Pin Ceramic LCC



K2 — 44-Pin Ceramic LCC

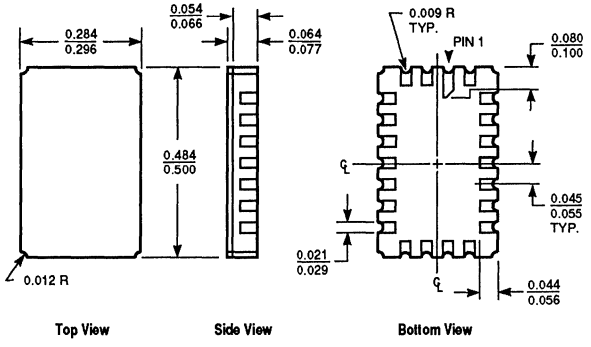


K3 — 68-Pin Ceramic LCC

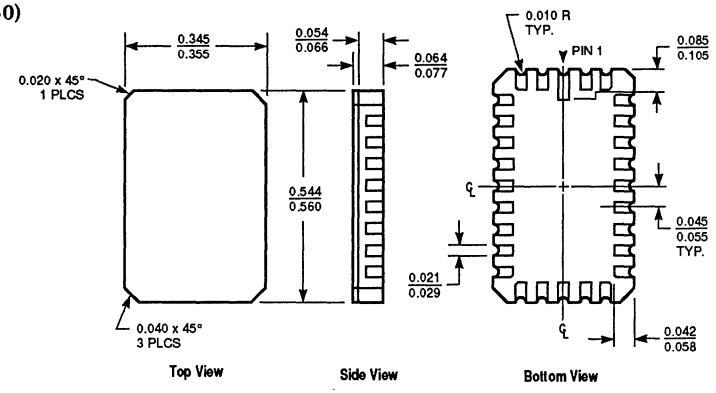


Ceramic Leadless Chip Carrier — Type K

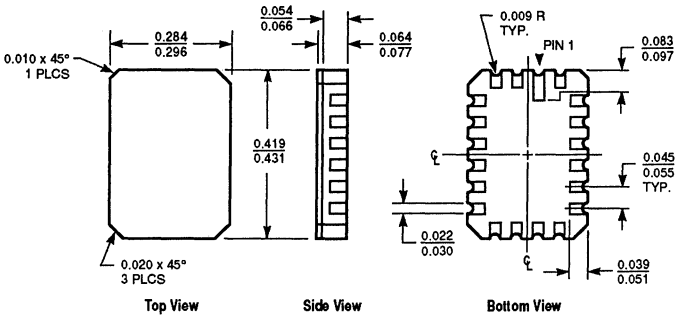
K4 — 22-Pin Ceramic LCC (290 x 490)



K5 — 28-Pin Ceramic LCC (350 x 350)



K6 — 20-Pin Ceramic LCC (290 x 425)



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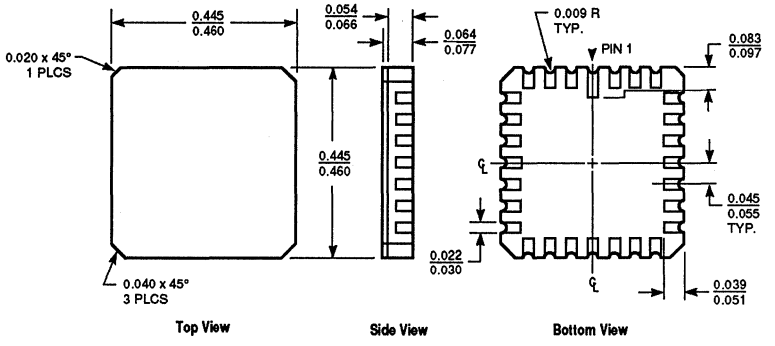
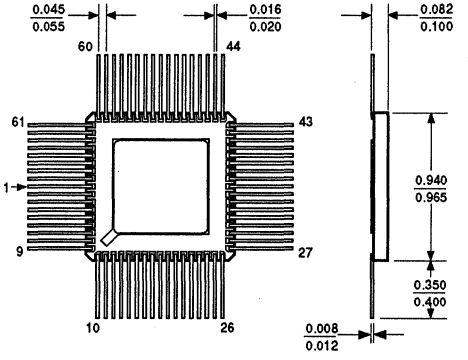
Ceramic Leadless Chip Carrier — Type K

K7 — 28-Pin Ceramic LCC (450 x 450)



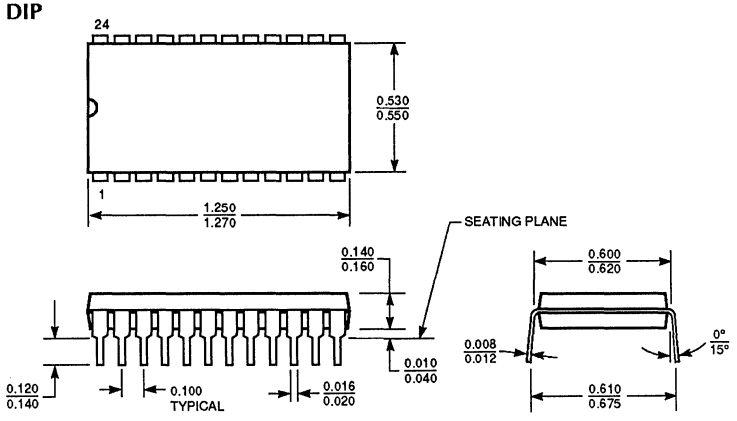
Ceramic Leaded Chip Carrier — Type L

L1 — 68-Pin Ceramic Leaded Chip Carrier

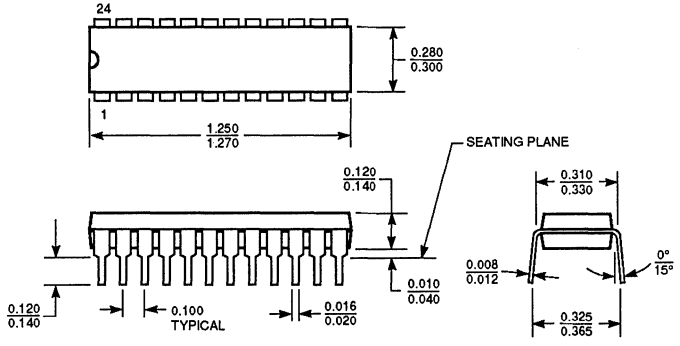


Plastic DIP — Type P

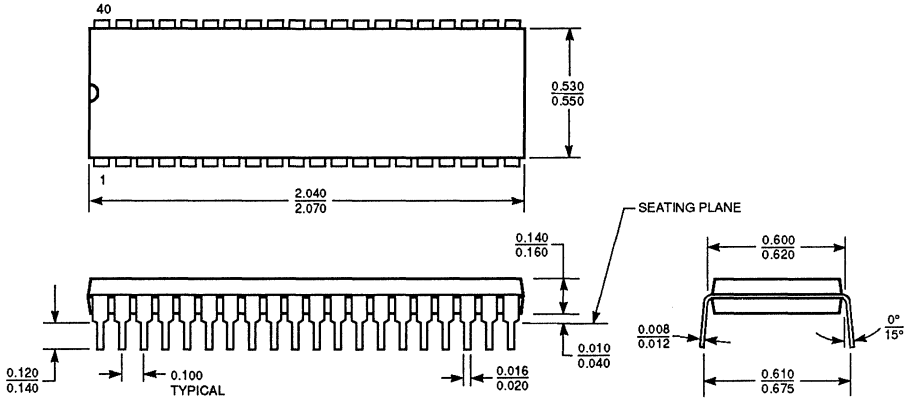
P1 — 24-Pin Plastic DIP



P2 — 24-Pin Plastic DIP



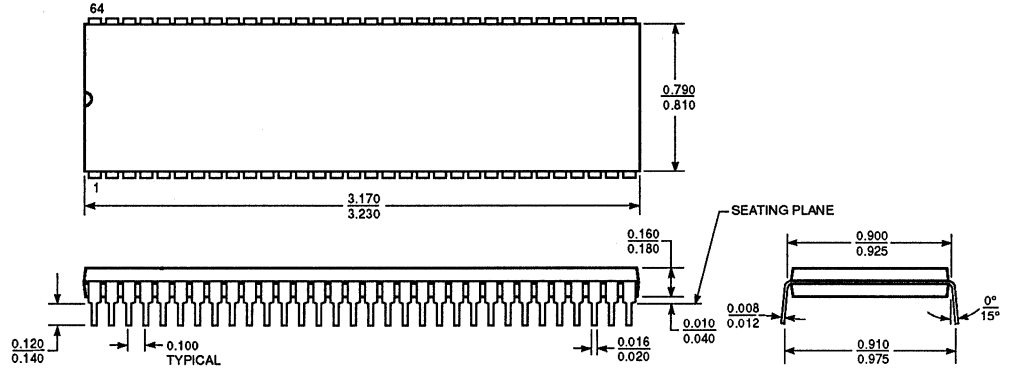
P3 — 40-Pin Plastic DIP



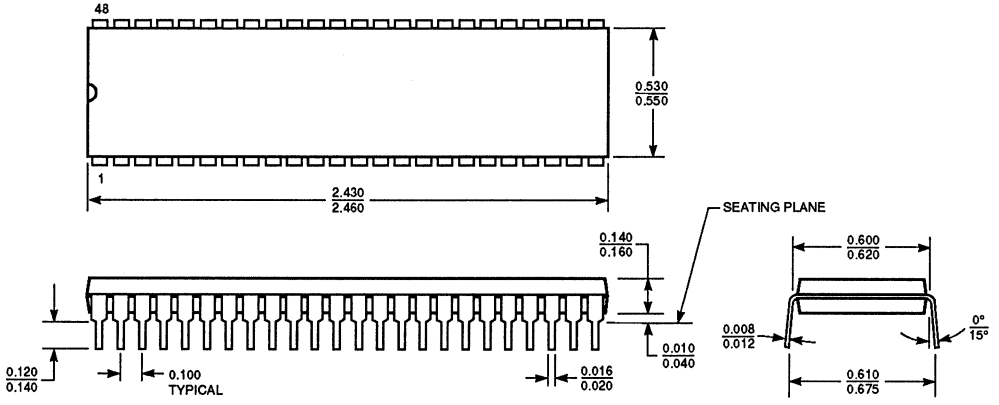
7

Plastic DIP — Type P

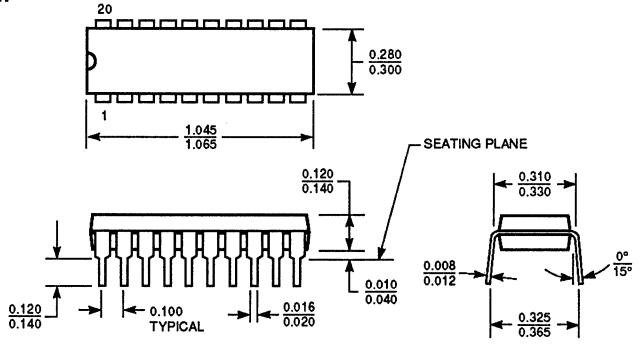
P4 — 64-Pin Plastic DIP



P5 — 48-Pin Plastic DIP

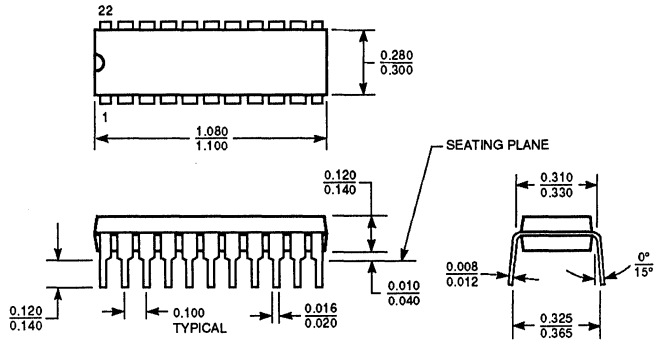


P6 — 20-Pin Plastic DIP

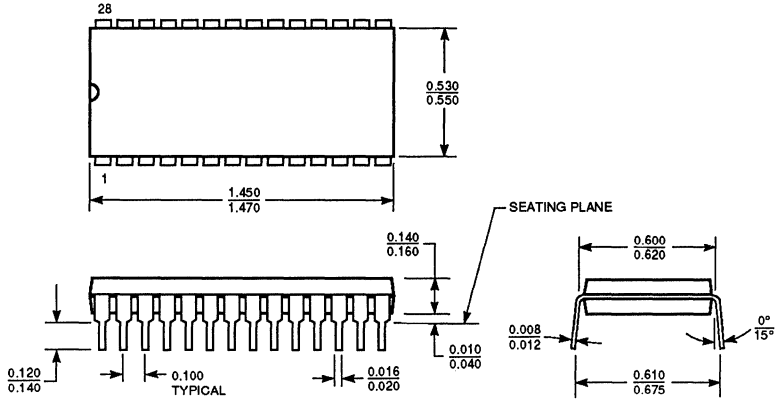


Plastic DIP — Type P

P8 — 22-Pin Plastic DIP



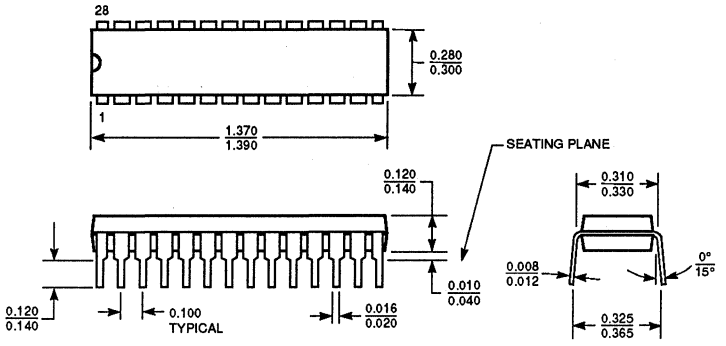
P9 — 28-Pin Plastic DIP



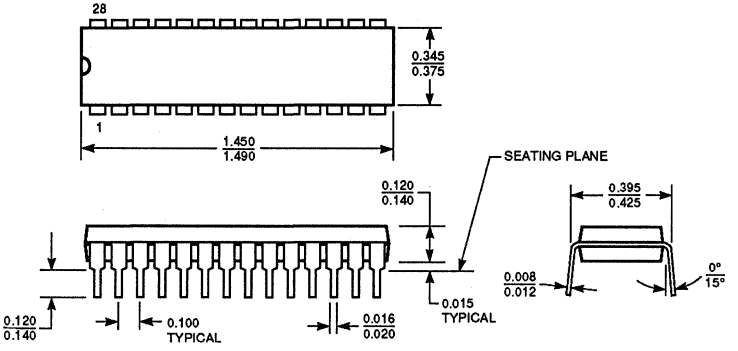
7

Plastic DIP — Type P

P10 — 28-Pin Plastic DIP

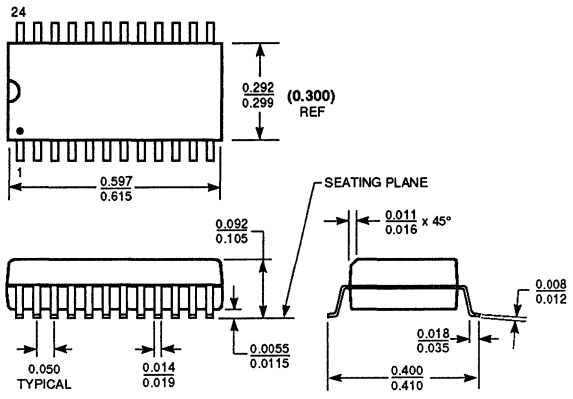


P11 — 28-Pin Plastic DIP

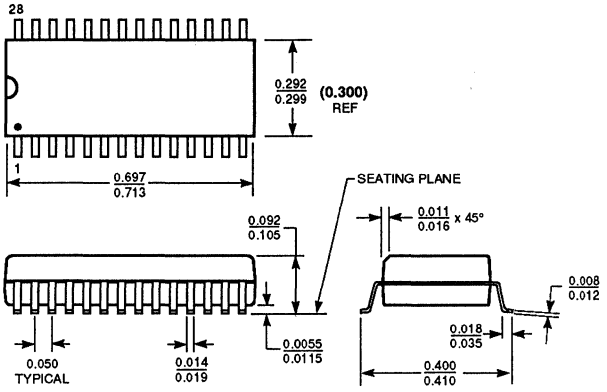


Plastic SOIC (Gull-wing) (0.300" wide) — Type U

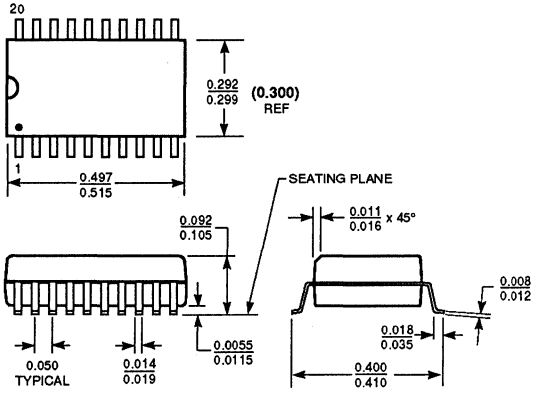
U1 — 24-pin Plastic SOIC (0.300" wide)



U2 — 28-pin Plastic SOIC (0.300" wide)



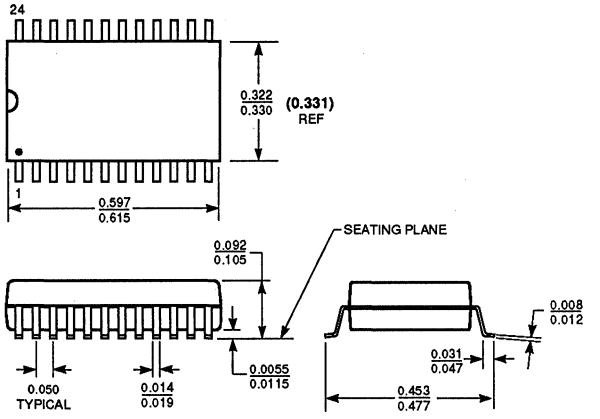
U3 — 20-pin Plastic SOIC (0.300" wide)



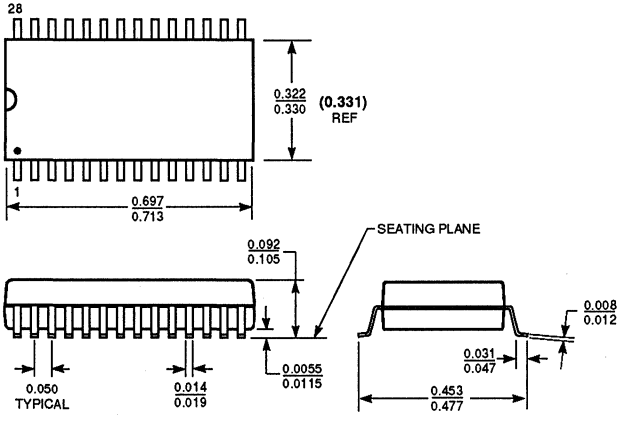
7

Plastic SOIC (Gull-wing) (0.331" wide) — Type V

V1 — 24-pin Plastic SOIC (0.331" wide)

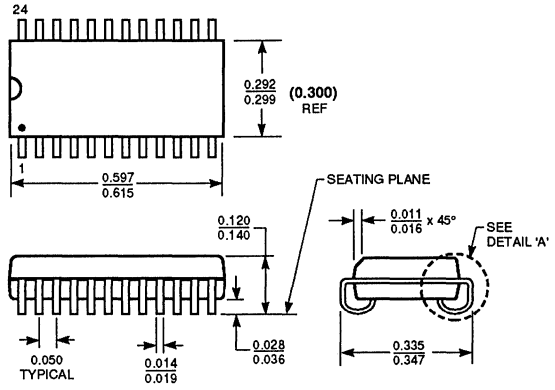


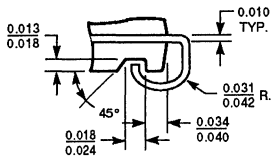
V2 — 28-pin Plastic SOIC (0.331" wide)



Plastic SOJ (J-lead) — Type W

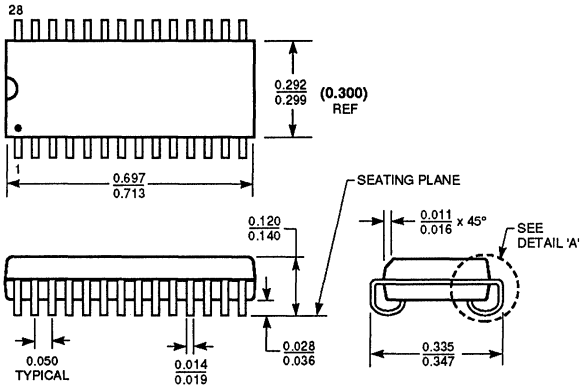
W1 — 24-pin Plastic SOJ



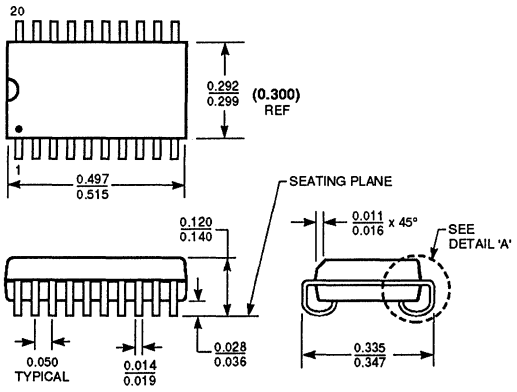


Detail A

W2 — 28-pin Plastic SOJ



W3 — 20-pin Plastic SOJ



7

Thermal Considerations

The temperature at which a semiconductor device operates is one of the primary determinants of its reliability. This temperature is often referred to as the "junction temperature", although this term is more appropriate for bipolar than MOS technologies. Heat dissipated in the device during operation escapes through a path consisting of one or more series thermal impedances terminating in the surrounding air (see Fig. 1).

The presence of this nonzero thermal impedance causes the temperature of the device to rise above that of the air. Each of the components of the overall thermal impedance causes a rise in temperature which is linearly dependent on the power dissipated in the device. The coefficient is called θ, and has the units °C/W. The θ value for each thermal impedance represents the amount of temperature rise across the impedance as a function of the power dissipation. Usually, θ is given a subscript indicating the two points between which the impedance is measured. Thus the junction temperature of an operating device is given by:

$$T_j = T_{AMB} + (Pd \bullet \theta_{JA})$$

where:

T_j = junction temperature of the device, °C,

T_{AMB} = ambient air temperature, in°C

Pd = power dissipation of the device, in W,

θ_{JA} = sum of all thermal impedances between the die and the ambient air, in °C/W.

The thermal impedance of a given device is dependent on several factors. The package type is the predominant effect; ceramic packages have much lower thermal impedances than plastic, and packages with large surface areas tend to dissipate heat faster. Another factor which is beyond the control of the device manufacturer but which is nonetheless important is the temperature and flow rate of the cooling air. Secondary effects include the size of the die, the method of attaching the die to the package, and the organization of high power dissipation elements on the die.

Because all Logic Devices products are built with low-power CMOS technology, thermal impedance is less of a concern than it would be for higher power technologies. As an example, consider a typical NMOS multiplier similar to the LMU16, packaged in a 64-pin plastic DIP. Assuming 1 W power dissipation and θ_{JA} of 50°C/W, the actual die temperature would be 50°C above the surrounding air. By contrast, the Logic Devices LMU16 has a typical power dissipation of only 60 mW. This device in the same package would operate at only 3° above the ambient air temperature. Since operating temperature has an exponential relationship to device failure rate (see Quality & Reliability, Section 5), the reduction of die temperature available with Logic Devices low-power CMOS translates to a marked increase in expected reliability.

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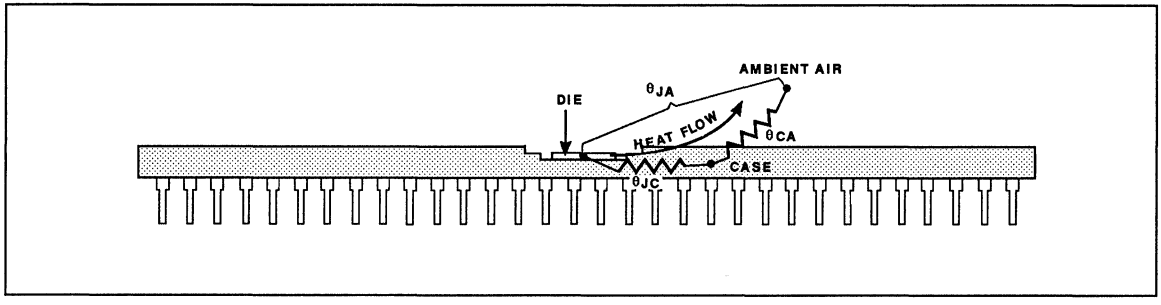
Figure 1.



To assist the user in calculating cooling requirements and in making reliability predictions based on MIL-HDBK-217, the following table of estimated θ_{JA} values for Logic Devices products is provided below:

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
Plastic Dual-Inline			
20		P6	65–80
22		P8	65–80
24	0.3	P2	60–75
24	0.6	P1	50–70
28	0.3	P10	60–80
28	0.6	P9	50–80
40		P3	50–60
48		P5	40–60
64		P4	40–60
Sidebraze, Dual-Inline			
20		D7	35–45
22		D8	35–45
24	0.3	D2	30–40
24	0.6	D1	25–40
28	0.3	D10	30–40
28	0.6	D9	25–40
40		D3	25–35
48		D5	20–40
64		D4	20–30
64	Cav. dn	D6	20–30

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
CerDIP, Dual-Inline			
20		C2	60–75
22		C3	60–75
24	0.3	C1	55–70
24	0.6	C4	40–55
28	0.3	C5	55–70
28	0.6	C6	40–55
Pin Grid Array			
68		G1	40–60
68	Cav Dn	G2	30–50
84		G3	20–40
Plastic J-Lead Chip Carrier			
28		J4	50–70
44		J1	40–60
68		J2	35–55
84		J3	35–55
Ceramic Leadless Chip Carrier			
28		K1	40–60
44		K2	35–60
68		K3	25–50
84		K4	20–40

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
Plastic SOIC (Gull-Wing)			
24		U1	65–80
28		U2	60–75
Plastic SOJ (J-Lead)			
24		W1	65–80
28		W2	60–75

LOGIC

DEVICES INCORPORATED

Contents

8

Real-Time Digital Image Transformation

by

Joel H. Dedrick

This application brief describes the design of a special effects generator for commercial broadcast television application. It demonstrates efficient realization of real-time pixel filtering, two dimensional interpolation, first order coordinate transformation, and display memory address generation. These operations are used in a variety of applications including mechanical and electrical CAD/CAM, image recognition, machine vision, RADAR/SONAR display processing, and other similar problems in which two or three dimensional data must be reformatted or manipulated for display.

Introduction

The television special effects generator is commonly used to provide a range of effects for broadcast use. These include the inclusion of reduced size, live or frozen inset pictures (e.g., "scene of the accident" shots in news programs) contained anywhere in the main video shot. Also, causing images or text (the network logo, a photograph and statistics of an athlete, etc.) to overlay the main video, and to be moved around the screen, rotated, and sized as appropriate.

The design described here can accomplish any first order translation (displacement in 2D space), rotation, and scaling (enlargement or reduction) on the input image in real time. By first order we mean that the translation, rotation, and scaling of the image is constant throughout the image for a given direction (X or Y), and thus no curvature of the image may be produced. Introducing second or higher order warping is a straightforward extension of the concepts presented. By real time, we mean that the system is capable of altering the effect generated throughout its range on a frame-by-frame basis, effectively providing for smooth progressions in the translation, rotation, and scaling operations giving the appearance of motion of the processed image around the screen.

Image Transformation — A System Overview

The image transformation system works essentially in two steps: First, the incoming image is lowpass filtered in both the vertical and horizontal directions. This is done because the effect required may include shrinking the picture. This essentially amounts to subsampling, or extracting every "n^{th}" pixel sample from the input image to form the output image. Subsampling the input image without filtering would result in aliasing, since the new spatial sample rate may be insufficient to meet the Nyquist criterion. (The Nyquist criterion for calculating the required sample rate in a sampled data system states that the sampling frequency must be at least twice that of the highest frequency component in the signal. Aliasing is the term for the type of distortion which occurs if this condition is not met.)

It is important to note that the cutoff frequency for the lowpass filters should be selected so that the above criterion is met, but a lower cutoff frequency than necessary results in loss of information (a "smearing" of the output image). For this reason, the cutoff frequency, and therefore the coefficients, of this filter must be adjusted according to the amount of scaling desired. This is done independently in the horizontal (X) and vertical (Y) directions.

The second step in the transformation process is to extract the individual pixels in the input image in the specific sequence required to form the output image.

Simple Transformation Examples

Some examples of the transformation process will illustrate the steps required:

For a simple shrink of an image by a factor of two in each direction, (Figs. 1 and 2) every other pixel (PIcture ELement) of the image would be extracted to form a scan line in the output image. Since this results in only half the number of pixels required on the scanline for television, the remaining pixels are blanked. Similarly, in the

vertical direction every other scanline is skipped, effecting a similar shrink along the Y axis.

The capability of moving the input image around the output image plane, called translation, is accomplished during the creation of the output image. By controlling on a line-by-line basis, when the sampling of the input image begins, and by blanking all pixels which map to coordinates outside the input image, translation can be accomplished. In addition to scaling, Fig. 2 shows translation of the (reduced size) input image to the center of the output image.

A more complex example arises when the image must be reduced in size as above, and also rotated 45° (Fig. 3). In this case, the scan direction (order in which pixels are displayed to produce an image) has changed between the input and output image, as shown by the arrows in Fig. 3. Because the in-put image is now being scanned at an angle rather than in the normal horizontal direction, the desired sample points will generally fall in between the actual locations of available pixels (Fig. 4). Note that this will also occur with simple scaling when the scale factor is not an integer. Because of this phenomenon, some type of interpolation will be required

Figure 1. Normal TV image.

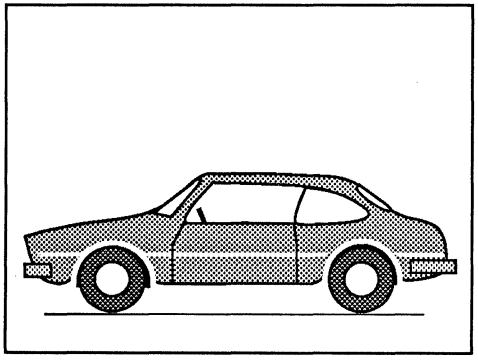


Figure 2. Same image after 2:1 shrink in both axes, and translation to center of output frame.

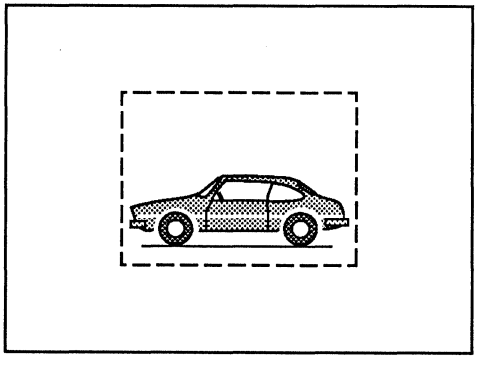


Figure 3. Addition of 45° rotation to the scaled image. The arrows show the scan directions in the input (small arrow) and output coordinate frames.

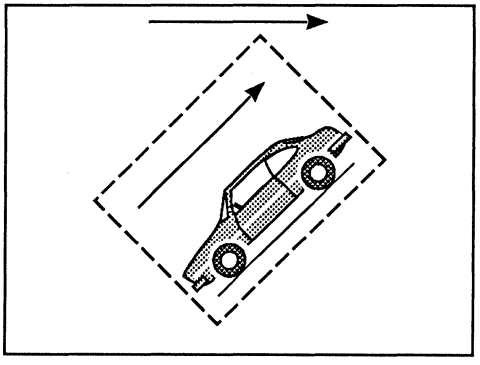
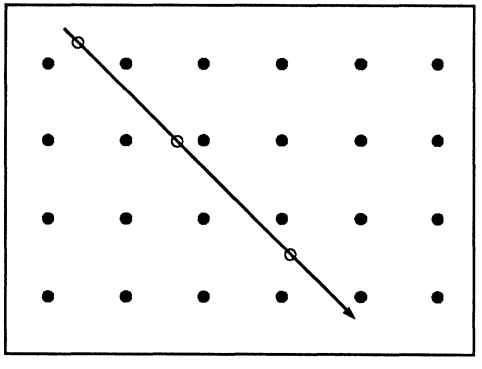


Figure 4. Sample points on one scanline through the input to form the result in Fig. 3. The black dots are the input (normal) image samples, the white dots are the desired sample points for the scaled and rotated output. The sample rate is reduced (spacing increased) to shrink the image, and the scan angle causes rotation.



to calculate the value of a point which does not fall exactly on a pixel location. For the system under discussion, bilinear interpolation is used for this calculation.

Image Transformation System-Implementation

The video effects generator block diagram is shown in Fig. 5. Television signals are expressed digitally as three channels of data. One channel, containing luminance or brightness information, is sampled at 14.3 MHz. The other two channels together express the chrominance or color of the image, and the aggregate of these also represents a 14.3 MHz data stream. It is common practice to split the datapath into two halves, one operating on the luminance channel, and the other operating in an interleaved fashion on the chrominance channel, with control information common between the two. The diagram represents a single such channel easily capable of sustaining a 14.3 MHz datarate.

Display Memory, Display Address Counter

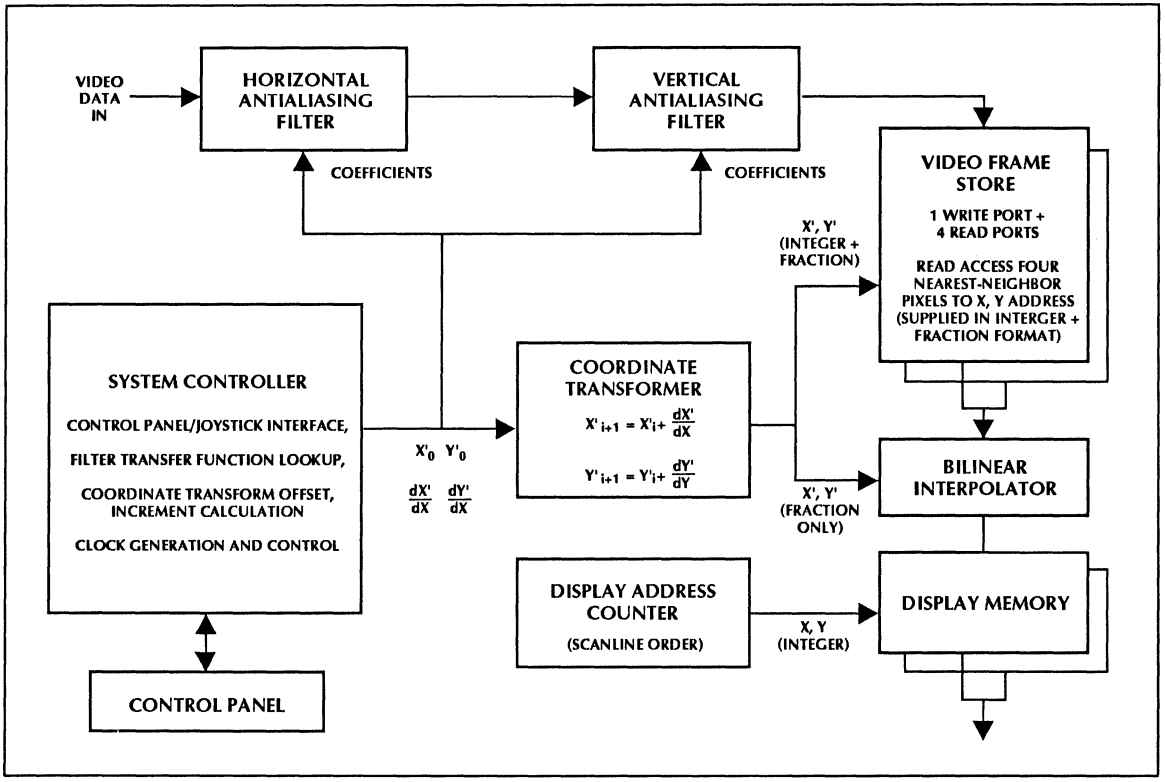
The system is composed of several major blocks as shown in Fig. 5. The Display Memory contains the output video image. The address sequence for this memory is provided by a Display Address Counter, which counts in a fixed sequence, scanning the pixels within a line from left to right, and sequential lines from the top to the bottom of the image. The address provided to this memory uniquely selects an individual pixel in the output image, and is denoted by (X,Y), respectively the horizontal and vertical displacement from the upper left corner.

Coordinate Transformer

The Coordinate Transformer calculates the address of the pixel location in the input image, denoted by (X',Y'), corresponding to the location currently addressed by the Display Address Counter. A general first order transformation from one 2D coordinate space to another can be implemented as:

$$X' = aX + bY + c$$
$$Y' = dX + eY + f \qquad (1)$$

Figure 5. Video special effects generator block diagram.



By appropriate choice of the six coefficients a–f, this set of equations can map any point in the X,Y (output) image plane to the corresponding point in the X',Y' plane if the two images are related by any combination of translation, rotation, and scaling.

However, since the Display Memory (X,Y) is always scanned in a fixed order, a generalized transformation as given above is not required. Significant hardware savings can be realized by taking advantage of the fact that once the input image point corresponding to the first pixel on an output image scan line is known, the locations of successive input points are related to the first by fixed offsets in X' and Y'. This is true because while the input image may be scanned at any angle, the path through the input image corresponding to an output scan line is always a straight line (for first order transformations). Thus, generating addresses in the X',Y' space is reduced to a simple recursion formula requiring only two additions and no multiplications. This formula takes the form:

$$X'_{i+1} = X'_i + dX'/dX$$

$$Y'_{i+1} = Y'_i + dY'/dX \qquad (2)$$

Note here that dX'/dX and dY'/dX are constants, so a simple programmable accumulator suffices to calculate input image addresses once the starting point for a given scanline is known.

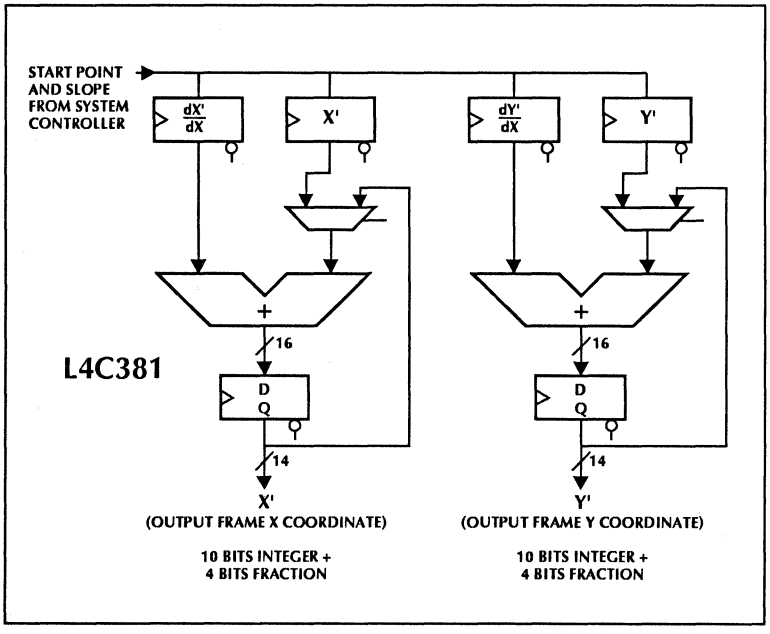
Figure 6 shows the coordinate transformer implemented with two Logic Devices L4C381 ALU's. The operand select function of the L4C381 is used to feed back the contents of the output register to the B input, implementing a programmable-rate increment function. By allocating one ALU for X' and one for Y', the recursions in Eq. (2) are implemented in only two devices. The B operand register of the ALUs holds the starting value for the next scanline, which is passed to the F register to initialize it. The A operand register holds the increment value dX'/dX or dY'/dX which is added to the accumulator (F register) contents on each cycle.

As discussed above, the desired pixel location in general does not correspond to the actual location of a pixel in the Frame Store. As a result, the X',Y' address must provide much finer resolution than the actual pixel grid used in the image. This is accomplished by providing both an integer and a fraction part of the X' and Y' displacements. For example, if 10 bits of integer and 4 bits of fraction (14 bits each for X' and Y') then a 1024 × 1024 image could be addressed to a spatial resolution of one sixteenth of a pixel. This fine resolution is required to produce adequate interpolation of the pixel value which is stored in the Display Memory. The L4C381 implementation of the coordinate transformer easily meets this requirement: In implementing a 16-bit accumulator for both X' and Y, the L4C381 provides two additional bits of resolution so that the address increments in X' and Y' directions can be specified to a full 16 bits of precision, even though only 14 bits are actually used. This is important because in a recursion formula, small errors in the desired increment accumulate with each cycle. The net effect is quantization error in the desired angle of rotation. The additional bits provide finer control over the desired angle.

Video Frame Store

The Video Frame Store is a RAM bank which stores the filtered input image. It is designed to execute four simultaneous read operations per clock cycle. For each address (X',Y') of the desired location provided by the Coordinate Transformer, the

Figure 6. Coordinate Transformer. The L4C381 ALU is used as an address counter with programmable step size.



Frame Store outputs the values of the *four stored pixel values closest to the addressed point.* In order to accomplish this, only the integer part of the X',Y' address need be considered. If I(X') is taken to mean the integer part of X', and similarly with Y', then for an input address X',Y' the desired four pixel locations are:

I(X'), I(Y') I(X')+1, I(Y')

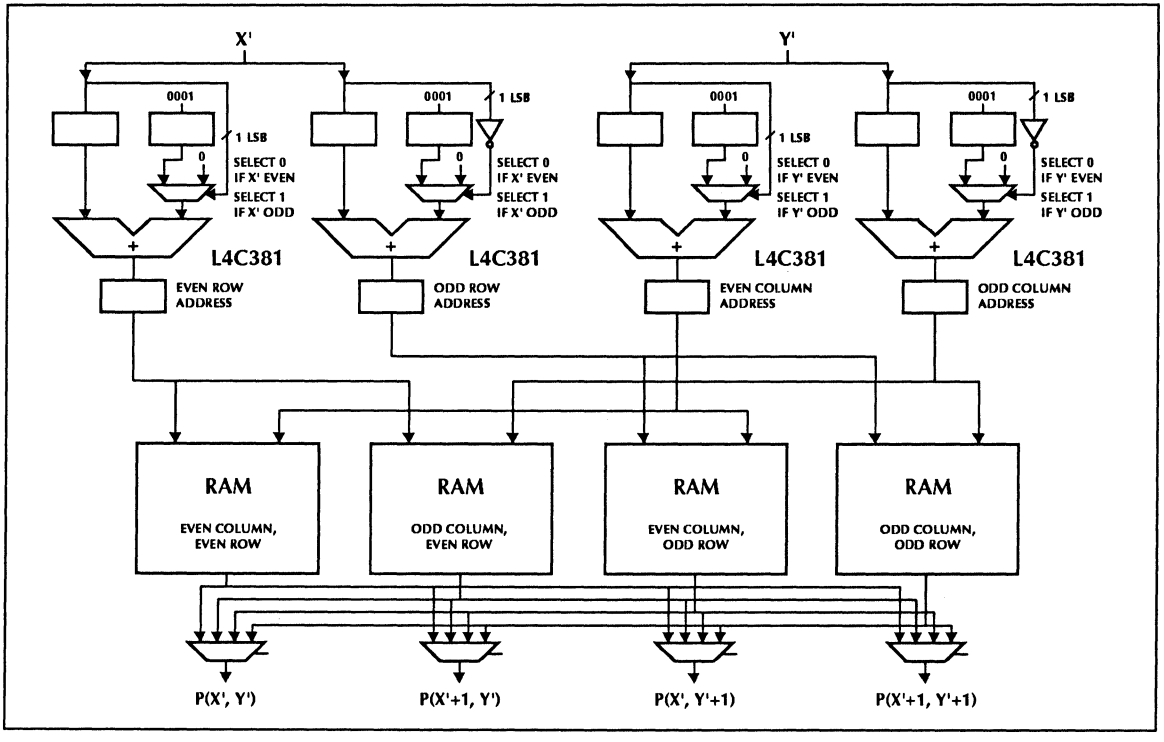
I(X'), I(Y')+1 I(X')+1, I(Y')+1

The organization of a memory capable of executing these simultaneous read operations is shown in Fig. 7. Pixel data is assigned to four internal RAM banks in such a way that adjacent pixels are never stored in the same bank, i.e., one bank is assigned to even row numbers and even column numbers only, etc.

The X' and Y' addresses are processed by a set of L4C381 ALU devices in order to generate internal addresses used to access the four RAM banks. The input X' and Y' addresses are each applied to a pair of ALU's configured so as to selectively increment the address depending on whether it is even or odd. For example, if the Y' address (row number) is even, then the RAM banks containing data for even row numbers should be supplied with this address directly, and those containing odd row numbers should be supplied with Y'+1. Conversely, if Y' is odd, it will be incremented for presentation to the even row RAM, and passed directly to the odd RAM. As an aside, note that since the data for any row is distributed between two RAM banks, the least significant bit of the address generated above will be discarded. This is so that data elements are stored in contiguous locations in the RAM banks, fully utilizing the available storage. As a result, the actual address supplied to the even and odd row data may be the same, or may differ by one.

The X' address is similarly modified to produce internal addresses for even and odd column numbers, and the resulting four addresses are combined to access the four RAM banks. The assumption here is that a row and column address can be concatenated

Figure 7. Video Frame Store. This special purpose memory accepts a desired sample location (X and Y Address) and reads the four pixel values closest to the desired point.



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to address a RAM bank, i.e., the internal plane sizes are integral powers of 2. Once these addresses are formed, four memory accesses are executed in parallel. Finally, multiplexers route the appropriate data to the four output ports, with selection of these muxes again determined by whether X' and Y' are even or odd.

Bilinear Interpolation

The four pixel values read from the Frame Store on each clock cycle are processed by the Bilinear Interpolator to produce the actual value written to the Display Memory. Bilinear interpolation is a means for interpolating a value between sample points in a two dimensional grid. It operates as shown in Fig. 8.

The four shaded points P1–P4 in the figure represent actual pixel values in the Frame Store. These are the four closest pixels to the desired point, denoted by P. P represents location of the point addressed by (X',Y'). As discussed above, X' and Y' have both an integer and fractional part, with the fractional part of each representing offsets in the horizontal and vertical direction *between pixels in the Frame Store.* The interpolator is presented with the four pixel values P1–P4, and the fractional parts of X' and Y', denoted dX' and dY'. The interpolation process can then be derived as follows:

First, the value of an imaginary pixel located between P1 and P2 is determined. This point, labeled P' in Fig. 8, is offset from P1 by dX', the same horizontal offset as the output point P. Unlike P, however, P' has the same vertical value as P1 and P2, so it represents interpolation in the X direction only. P' can be seen in Eq. 3 to be a weighted sum of P1 and P2, with the weights inversely proportional to the distance of P' from P1 and P2.

$$P' = P1(1 - dX') + P2(dX') \qquad (3)$$

Note that the weights applied to P1 and P2, namely (1 – dX') and (dX') sum to one, resulting in no net amplitude gain through this process.

In a similar way, a point P'' can be determined which is a horizontal axis interpolation between P3 and P4 (Eq. 4).

$$P'' = P3(1 - dX') + P4(dX') \qquad (4)$$

Having determined P' and P'', the final step is to interpolate between these two to determine the desired point P, with the fractional part of the Y axis address dY' used as the weighting factor (Eq. 5).

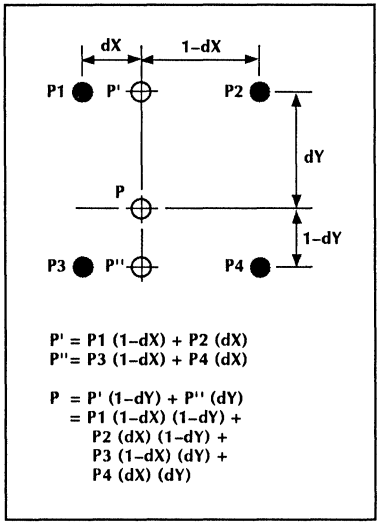
$$P = P'(1 - dY') + P''(dY') \qquad (5)$$

By substituting Eqs. (1) and (2) into (3), the following is obtained:

$$\begin{aligned} P = {} & P1(1 - dX')(1 - dY') + \\ & P2(dX')(1 - dY) + \\ & P3(1 - dX')(dY') + \\ & P4(dX')(dY') \end{aligned} \qquad (6)$$

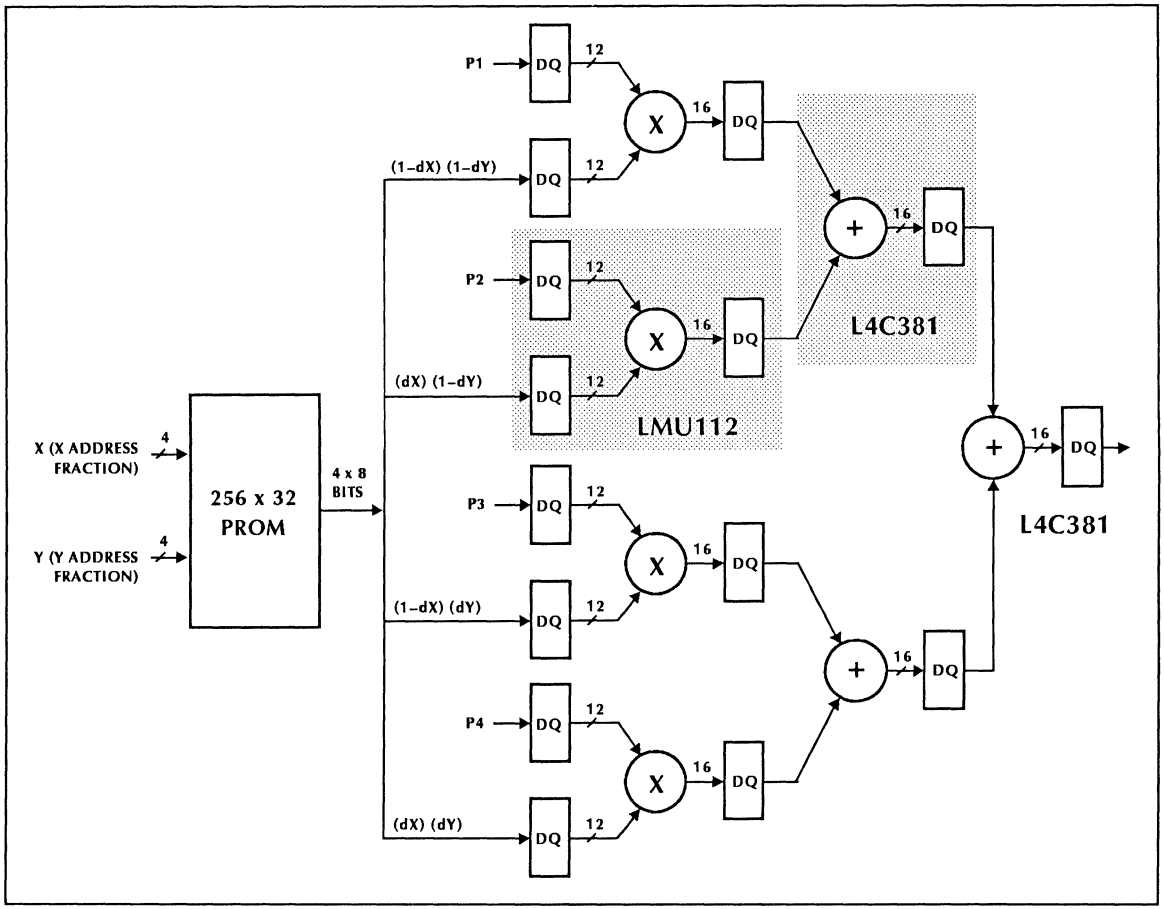
Figure 9 shows the implementation of the bilinear interpolator. The inputs are dX' and dY'; the fractional parts of the coordinate transform address. Each of these fractions is 4 bits, for a total of 8 bits. A 256 word lookup table PROM is used to derive the four weights required for the interpolation in parallel. Four LMU112 multipliers apply these weights to the four pixel values P1–P4 in parallel. The LMU112 is a 12 × 12 multiplier which is available in a 48-pin package, due to the fact that only the 16 most significant outputs are brought out. Since 16 bits of information is more than sufficient for video, it is an appropriate choice to save space over the more typical 64-pin implementations of 12 × 12 multipliers. The four weighted pixel values are then summed using a network of three L4C381 ALU devices. These provide the 16-bit add function required, as well as integrating the pipeline registers necessary to maintain the desired clock rate.

Figure 8. Bilinear Interpolation. Bilinear interpolation involves first executing linear interpolations between two pairs of adjacent points on successive scanlines, resulting in P' and P''. Then, a final linear interpolation is performed between these two intermediate results to form an approximation of the image value at the desired location P.



One final function is performed by the interpolator: The transformations available on the input image may result in portions of the output display which contain no video data. A simple instance occurs when the input image is reduced in size, in which case the remaining portions of the display must be blanked. Also, since the amount of size reduction can be changed in real time, the pixels to be blanked must also be set on a scanline-by-scanline basis. This requirement is conveniently met by the L4C381, since its instruction set contains a force-to-zero function. By

Figure 9. Bilinear Interpolator. LMU112 12 x 12 multipliers and L4C381 ALUs form a compact implementation of the equations in Fig. 8. The coefficients are precomputed and stored in PROM.



setting the function control lines of the last ALU stage to 000 (force-to-zero instruction) when writing the nonimage areas of the display memory, the pixel data stored in these locations is blanked. This instruction control is provided by the system controller.

Horizontal/Vertical Anti-aliasing Filters

Prior to any operation on the data which involves resampling, a lowpass filtering pass must be applied to the data to avoid aliasing distortion. The filter chosen here is a Finite Impulse Response (FIR) type.

Figure 10 shows the conventional flow diagram for an FIR filter. The data is applied to a delay network, the length of which corresponds to the desired filter length. Each delay element output is weighted (multiplied) by the appropriate coefficient, and the results are summed to form the filter output.

Figure 11 shows an alternate, but equivalent implementation of the same flow diagram. In this implementation (known as the transpose form,) the delay elements are distributed through the summation or output path, with the input data distributed simultaneously to all of the weighting operators. This form of the flow graph is more convenient for implementation in LSI form, since it results in a series of identical functional blocks, each of which performs

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a multiply, add, and delay function. The dotted line in Fig. 11 illustrates the repeated function, and Fig. 12 shows an implementation of the flow diagram for the horizontal filter using the LOGIC Devices LMS12.

The LMS12 is a filter building block especially suited to the transpose form FIR structure. It provides a 12×12 bit multiplication, and addition of a third input of 26 bits to the result. Thus the FIR structure under consideration can be implemented with no external logic using this device, saving considerable real estate over more conventional implementations using multipliers and discrete external adders and delay elements.

The vertical (Y dimension) filter is formed in a similar way (Fig. 13) except that a delay equal to the length of each horizontal scanline is inserted between each LMS12 and its neighbor. In this way, the input pixels contributing to a given output sample are vertically adjacent, i.e., separated in the input datastream by a number of samples equal to one less than the length of one scanline. Since this filter implementation makes available all of the coefficient registers independently, they can be loaded at any time by the system controller with coefficients appropriate for the cutoff frequency desired.

Figure 10. F.I.R. Filter (Canonical Form).

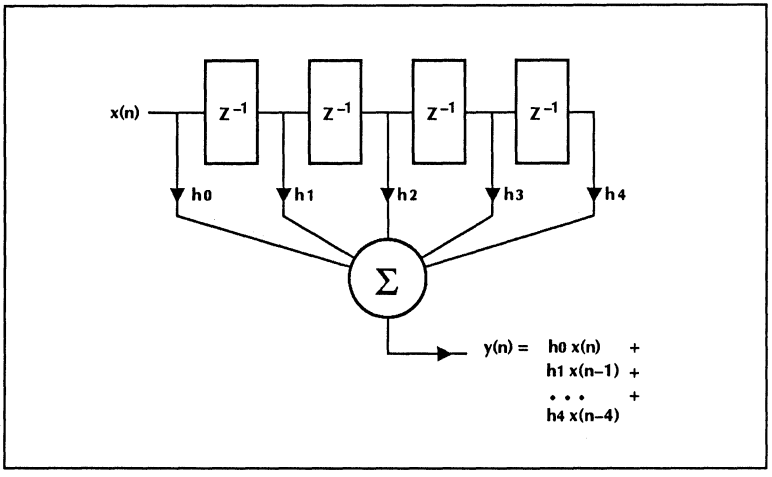


Figure 11. F.I.R. Filter (Transpose Form).
An alternate formulation of the equation in Fig. 10 allowing implementation by cascading identical functional blocks. The summation is now distributed across the filter delay and is therefore inherently pipelined.

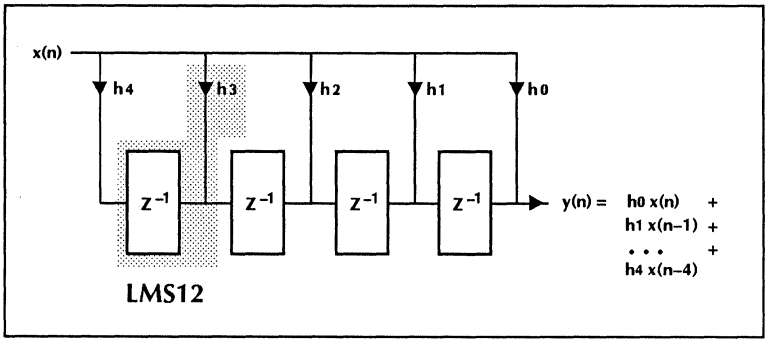


Figure 12. Horizontal Anti-aliasing Filter.
This realization of the transfer function in Fig. 11 uses the LMS12 filter building block. it is capable of exceeding 25 MHz data rates for any filter length, while allowing instantaneous coefficient changes.

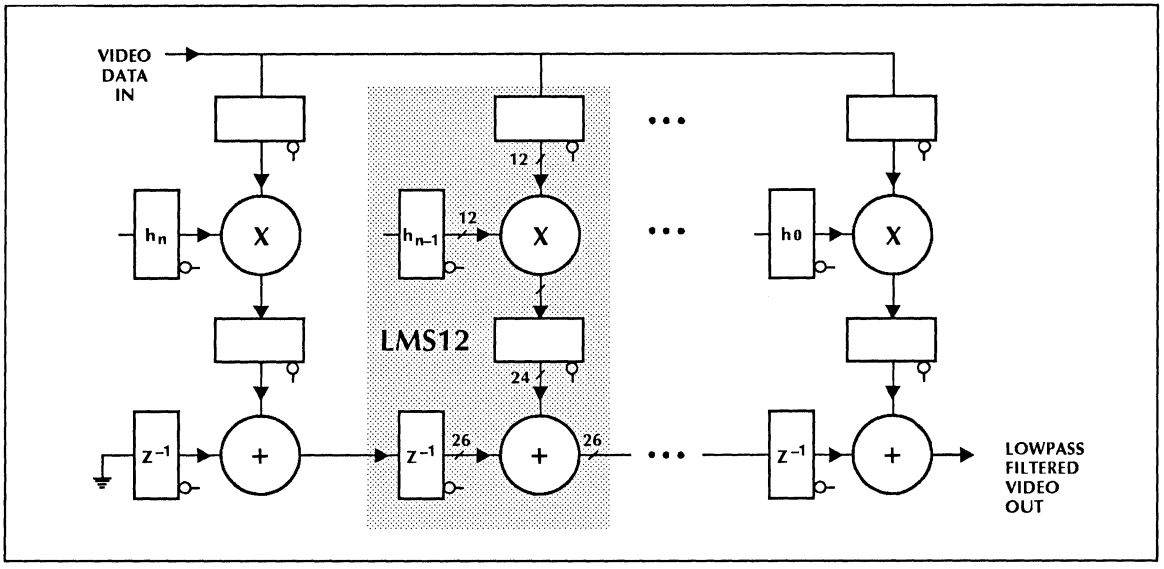
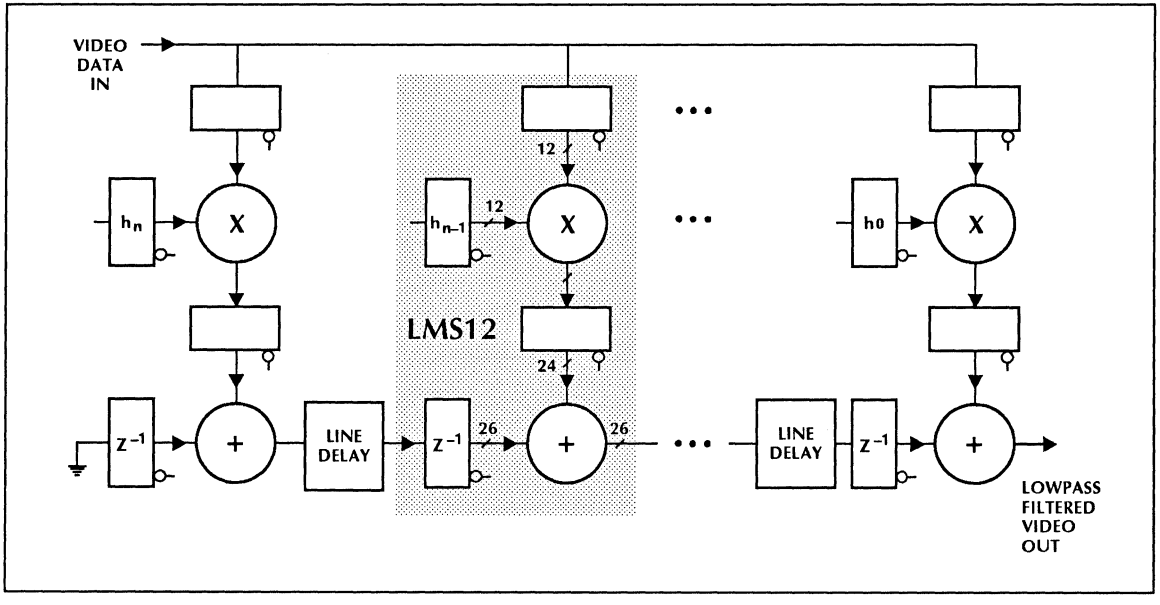


Figure 13. Vertical Anti-aliasing Filter.
A modification of Fig. 12 allows filtering in the vertical direction by inserting a delay equal to the length of a scanline between each pair of filter taps.



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Ultra-High Performance FFT Using DSP 'Designer Chips'

by
Edgar R. Macachor and
Joel H. Dedrick

New high-speed CMOS building blocks provide a clean implementation of the FFT for applications where single-chip DSP microprocessors cannot provide the necessary throughput.

Introduction

As single-chip microprocessors for DSP mature, digital spectrum analysis for low to medium bandwidth application has become widely available at reasonably low cost. For many real-time applications however, the single-chip units do not have the throughput to do the job. This article shows how to determine when you've outgrown a single-chip solution, and gives implementation details for an FFT engine which is 10 to 100 times faster than the single-chip units studied.

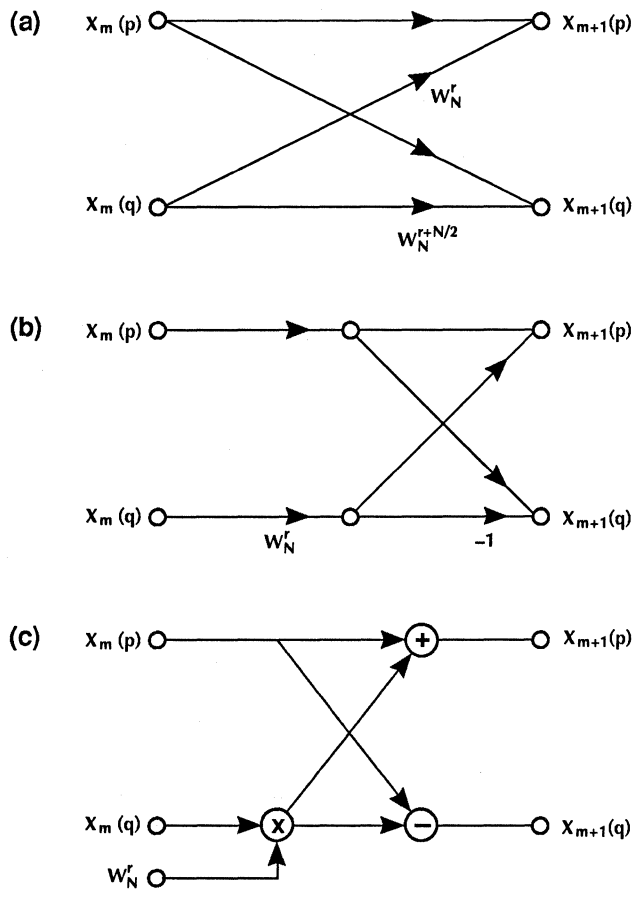
The FFT and Current Single-Chip DSP Microprocessors

In digital signal processing (DSP), the Fast Fourier Transform (FFT) is used to evaluate the Discrete Fourier Transform (DFT) of a signal. Typically, the signal is continuous and periodic in the time domain. To obtain the DFT of a continuous signal, the FFT is necessary to reduce the computation time. For example, if the original signal is represented as having real and imaginary components and sampled N times during its full period it takes $4N^2$ multiplications and N(4N–2) additions to compute the DSP directly. In contrast, the FFT, in particular the decimation-in-time algorithm, only requires $(N/2)\log_2 N$ stages of multiplications and additions. Each stage is defined by the basic cell of the FFT, the butterfly flow graph, and shown in Fig. 1(a) using the notation of Ref. 1. By taking advantage of the symmetric property of the W_N^r term, Fig. 1(b) allows for better computational efficiency. Figure 1(c) is further obtained to serve as the working model and shows that four multiplications, three additions and three subtractions are required per butterfly. The additions and subtractions are combined with the multiplications via a multiplier/accumulator (subtractor) unit.

The FFT butterfly computation can be accomplished using presently available single-chip DSP units. These current third-generation products can be categorized into two groups. The first group contains some on-chip memory to hold the executable instructions and the data to be processed. The TI TMS32010/20 and the NEC μPD77230 belong to this group. The architecture of these devices allows the process to be "optimized" if both program and data are in the on-chip memory at all times throughout the whole process. However, the computational throughput is still slow since only two data elements can be operated on at any given cycle. Another drawback is that, if the number of sample data points to be processed exceeds the on-chip memory capacity, then data need to be stored externally. As a result, additional cycles to fetch data from external memory further degrade the computational throughput. Still another factor is the increase in software overhead. Since data is now fetched from external memory, instructions that would have enabled parallel processing cannot be taken advantage of anymore. Therefore, one has to resort to straight-line coding to get maximum performance at the expense of increasing the code size.

The second group of "single-chip" DSP units require external memory for program and data storage. The National LM32900 and the Analog Devices ADSP2100 belong in this category. Their architecture allows for efficient access to both program and data memory via independent busses. However, these DSP units still can only process one set of operands at

Figure 1. Butterfly Cell working models



$$X_{m+1}(p) = X_m(p) + X_m(q)\,W_N^r$$
$$= \{Re[X_m(p)] + (A-D)\} + \{Im[X_m(p)] + (B+C)\}$$

$$X_{m+1}(q) = X_m(p) - X_m(q)\,W_N^r$$
$$= \{Re[X_m(p)] - (A-D)\} + \{Im[X_m(p)] - (B+C)\}$$

$A = Re[X_m(q)] \cdot Re[W_N^r]$ $\quad C = Re[X_m(q)] \cdot Im[W_N^r]$

$B = Re[W_N^r] \cdot Im[X_m(q)]$ $\quad D = Im[X_m(q)] \cdot Im[W_N^r]$

any given cycle. For FFTs involving 32-bit complex data, external memory fetch cycles degrade the computational throughput. One method of improving the performance is by operating two devices in parallel to handle two sets of operands at a time. In this case, however, the user is faced with issues regarding synchronization and control of the two devices.

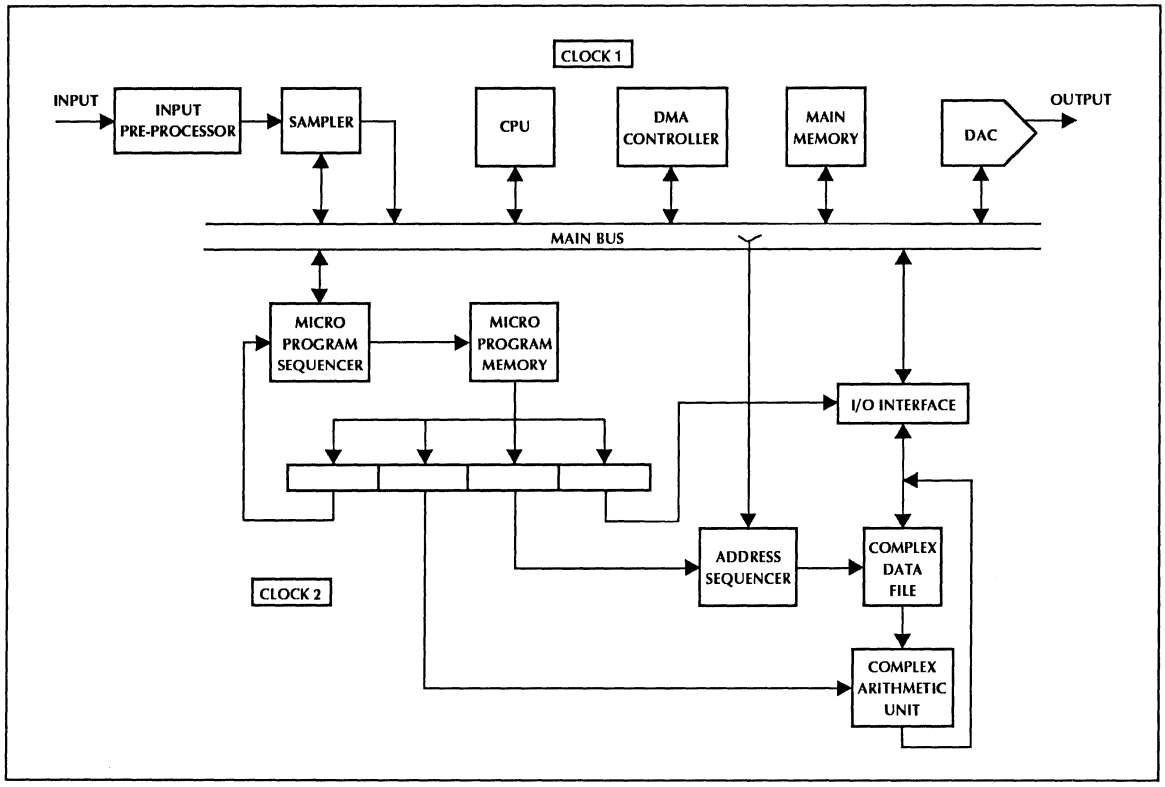
Building Block Approach

The "functional building block" architecture overcomes the limitations of the "single-chip" DSP units. This method allows the user flexibility in achieving the high-throughput requirement by minimizing the number of machine cycles per butterfly computation. The only penalty is the typical increase in the number of components used. However, this penalty is more than offset by the increased performance. An efficient functional building block architecture for high-speed DSP is shown in the block diagram of Fig. 2. The architecture achieves 2 machine cycles per butterfly, pipelined for 32-bit complex data FFT. The detailed implementation of the butterfly cell is shown in Fig. 3. The architecture is described as follows.

In the block diagram of Fig. 2, the butterfly cell is embedded in the system, under microprogram control, to handle the FFT computation. The overall architecture utilizes both a general purpose CPU, i.e., a Motorola 68000 or equivalent and functional building blocks to serve as the FFT coprocessor. The architecture allows for the execution of four phases to obtain the DFP. The four phases are: sampling, data formatting, computation, and outputting the DFP via the DAC.

The analog input signal is first fed into a pre-processor where it is band-limited via an anti-aliasing filter. The input signal can also be split into its quadrature components at this stage

Figure 2. A representative system block diagram DSP



or this may occur as a result of other operations such as heterodyning implemented digitally. The SAMPLER converts the analog signal into its equivalent digital data representation. The sampling process can be controlled either by the CPU or the DMA controller. Reference 2 shows that the controlling element also determines the maximum throughput rate of the sampling process; hence, the maximum input signal bandwidth. After sampling, or at the conclusion of other DSP processes, each of the real and imaginary data samples is assumed to be stored in contiguous memory locations in main memory. Therefore, real data can be stored in even address and imaginary data in odd addresses.

Data Formatting

Assume that in the 16-bit system of Fig. 1 the analog input signal is sampled 1024 times to represent one sample period. Furthermore, if all the samples are real numbers and storage is to begin at address 0000H, then the normal data storage sequence is such that the consecutive samples are stored in contiguous memory locations in main memory. This is particularly true in the case where the sampling process is treated as a data block transfer under CPU or DMA control. However, to be able to execute an in-place computation of the decimation-in-time FFT algorithm, the original data sequence obtained during the sampling phase must be restructured. This process involves address-bit reversal and is illustrated in Fig. 4.

An algorithm for generating the addresses in the bit-reverse order is discussed in Ref. 3. As pointed out, a highly flexible FFT Address Sequencer is sometimes required if the data buffer is not located at address 0000H, or if the FFT size is variable, due to the different sizes and fields of the address bits that need to undergo bit-reversal. Further complications are encountered when X(N) data is complex. As shown in Fig. 2, the 16-bit real and 16-bit imaginary data in main memory is to be mapped into a 32-bit field in the COMPLEX DATA RAM. A general purpose FFT Address Sequencer can be efficiently implemented with the combination of Logic

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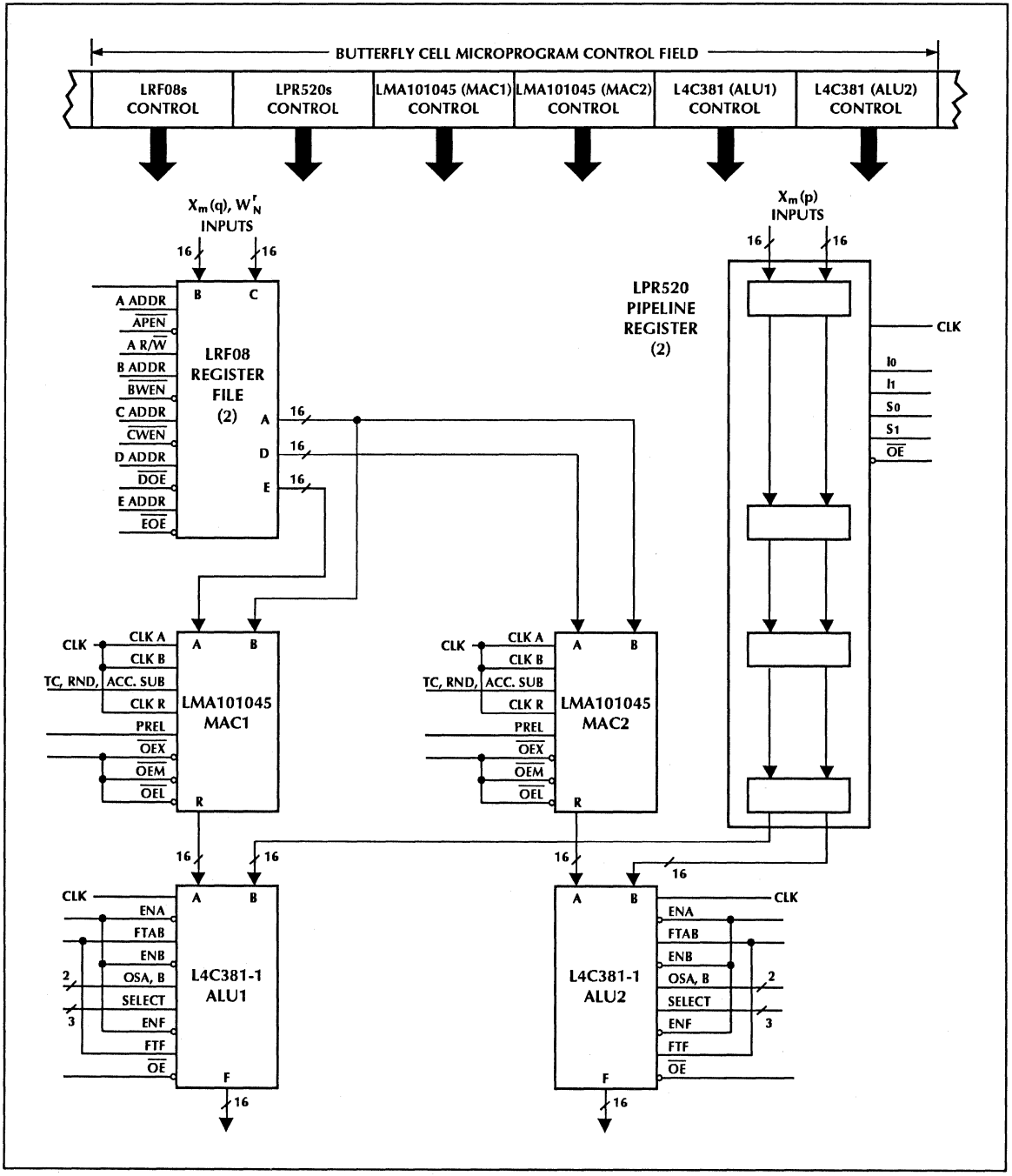
Figure 3. Detailed Butterfly Cell implementation with the control field.



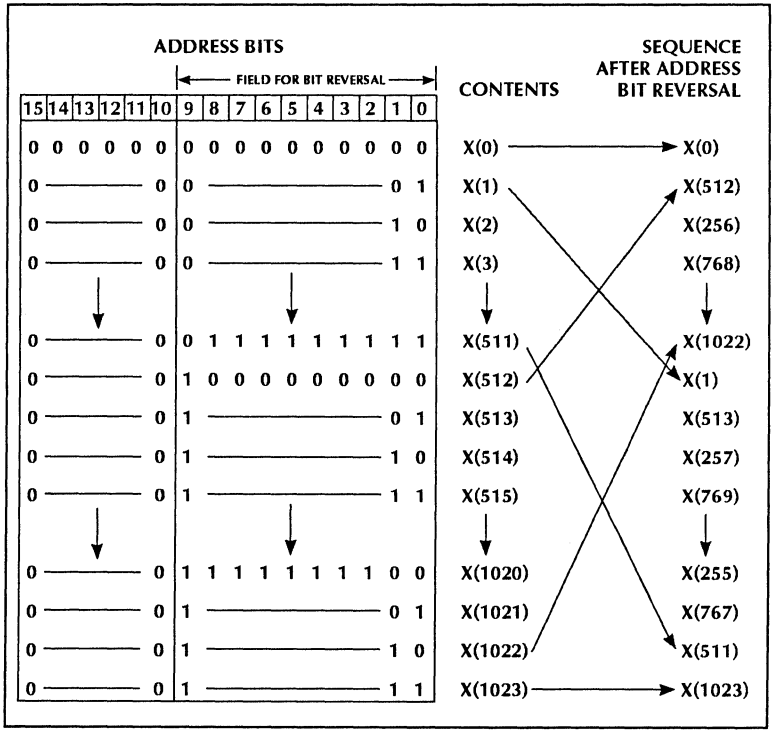
Devices' LRF08 multiport register file and L4C381 16-bit ALU. Because of their ability to be controlled by microcode, these two high-speed CMOS LSI devices provide the flexibility required of the FFT Address Sequencer. Also, the overhead time required to pre-sort the complex data sequence prior to the computation phase is reduced.

Handling the Computation

In Figure 1, the butterfly operands $X_m(p)$, $X_m(q)$, and W_N^r are all complex variables. The results of the computations $X_{m+1}(p)$ and $X_{m+1}(q)$ are also complex variables. W_N^r are known coefficients and stored in a read-only memory device as part of the COMPLEX DATA FILE in Fig. 2. The other part of the COMPLEX DATA FILE consist of the input data samples stored in COMPLEX DATA RAM in sorted order as defined by the bit-reversal process. The elements of the COMPLEX DATA FILE are 32 bits wide to accommodate the 16-bit real and 16-bit imaginary components.

The computation phase starts with the CPU generating a code for the MICROSEQUENCER. The MICROSEQUENCER interprets this code to access the first microinstruction in the MICROPROGRAM MEMORY and stores it in the MICROINSTRUCTION REGISTER. The microinstruction is horizontally organized so that different processing blocks can be controlled simultaneously; thus executing one microinstruction in one cycle of CLOCK2. The microinstruction field for controlling the butterfly cell is shown in Fig. 3 along with the detailed hardware implementation of the butterfly which consist of Logic Devices' LRF08 multiport register file (2), LPR520 pipeline register (2), LMA1010 16-bit multiplier/accumulator (2) and L4C381 16-bit ALU (2). The operands $X_m(q)$ and W_N^r are to be held in the register file temporarily while the $X_m(p)$ is passed down the pipeline register. The computations are done in a pipelined fashion and facilitated by the internal pipeline registers of the LMA1010s and L4C381s. The results of the computations can then be stored back into the COMPLEX DATA RAM to be used in the next iteration. This is really the essence of the in-place computation of the decimation-in-time FFT algorithm. The status of the components comprising the butterfly cell is outlined in the state matrix of Fig. 5.

Figure 4. Normal data sequence during sampling phase and result of re-structuring via address bit reversal. The new data sequence is stored in the complex data RAM.



Digging into the Microcode

During state SO, the Address for storing one of the first set of operands, $X_m(q)$ is loaded into the B and C Address Port register of the LRF08s. Since $X_m(q)$ is composed of 16-bit real, $Re[X_m(q)]$, and 16-bit imaginary data, $Im[X_m(q)]$, the LRF08s' registers are set up such that $Re[X_m(q)]$ will be stored in register R0 and $Im[X_m(q)]$ in R1. This is easily done by setting up the microcode to take advantage of the simultaneous register access capability of the LRF08. In this case, the address bits are $B_2B_1B_0 = 000$ and $C_2C_1C_0 = 001$ respectively. During S1, $X_m(q)$ is written into the LRF08s via the B and C input ports and at the same time the address for storing the real and imaginary part of W_N^r, $Re[W_N^r]$ and $Im[W_N^r]$ respectively, are also written into the B and C Address Port registers. This time the address bits are $B_2B_1B_0 = 010$ and $C_2C_1C_0 = 011$. This will allow storage of $Re[W_N^r]$

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Figure 5. Butterfly computation state matrix.

DEVICE	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
LRF08 REGISTER FILE	LOAD $X_m(q0)$. WRITE ADR.	WRITE $X_m(q0)$. LOAD $[W_N^r]0$ WRITE ADR.	WRITE $[W_N^r]0$. READ $Im[X_m(q0)]$ & $[W_N^r]0$. LOAD $X_m(q1)$ WRITE ADR.	WRITE $X_m(q1)$ LOAD $[W_N^r]1$ WRITE ADR. READ $[W_N^r]0$	WRITE $[W_N^r]1$. READ $Im[X_m(q1)]$ & $[W_N^r]1$ LOAD $X_m(q2)$ WRITE ADR.	S3	S4	S3	S4	S3	S4
LRP520 PIPELINE REGISTER			$X_m(p0) \rightarrow R1$	$X_m(p0) \rightarrow R2$ $X_m(p1) \rightarrow R1$	$X_m(p0) \rightarrow R3$ $X_m(p1) \rightarrow R2$ $X_m(p2) \rightarrow R1$	$X_m(p0) \rightarrow R4$ $X_m(p1) \rightarrow R3$ $X_m(p2) \rightarrow R2$	HOLD	$X_m(p1) \rightarrow R4$ $X_m(p2) \rightarrow R3$	HOLD	$X_m(p2) \rightarrow R4$	HOLD
LMA1010 MAC1				LOAD $Im[W_N^r]0$ & $Im[X_m(q0)]$	$Im[X_m(q0)] \times Im[W_N^r] = D$ LOAD $Re[W_N^r]0$ & $Re[X_m(q0)]$	$\{Re[X_m(q0)] \times Re[W_N^r]0\} - D = Re[X']$. S3 LOAD.	OUTPUT $Re[X']$. EVALUATE "NEW" D.	S5	S6	S5	S6
LMA1010 MAC2				LOAD $Re[W_N^r]0$ & $Im[X_m(q0)]$	$Im[X_m(q0)] \times Re[W_N^r] = B$ LOAD $Im[W_N^r]0$ & $Re[X_m(q0)]$	$\{Re[X_m(q0)] \times Im[W_N^r]0\} + B = Im[X']$. S3 LOAD.	OUTPUT $Im[X']$. EVALUATE "NEW" B.	S5	S6	S5	S6
L4C381 ALU1							$Re[X_m(p0)] - Re[X'] = Re[X_{m+1}(q0)]$	$Re[X_m(p0)] - Re[X'] = Re[X_{m+1}(p0)]$	S6	S7	S6
L4C381 ALU2							$Im[X_m(p0)] - Im[X'] = Im[X_{m+1}(q0)]$	$Im[X_m(p0)] - Im[X'] = Im[X_{m+1}(p0)]$	S6	S7	S6
								$X_{m+1}(q0)$	$X_{m+1}(p0)$	$X_{m+1}(q1)$	$X_{m+1}(q1)$

into register R2 and $Im[W_N^r]$ into R3 of the LRF08s. During S2, W_N is written via the B and C input ports and simultaneously read out via the D and E output ports. The imaginary part of $X_m(q)$ is also read out of the bi-directional A-port. In addition, the address for storing a "new" $X_m(q)$ is written into the B and C Address Port registers. $X_m(p)$ is also loaded into the LPR520 pipeline register. Note that during this state two sets of complex operands, W_N^r and $X_m(p)$, are simultaneously accessed from the COMPLEX DATA FILE. During this state all the complex data operands for the first FFT butterfly computation are available in the working registers. For a 1024-point FFT, the first set of operands correspond to

$X_m(p) = X(0)$, the first sample

$X_m(q) = X(512)$, the 513th sample

$W_N^r = W_N^o = 1$

The operands $Im[W_N^r]$, $Re[W_N^r]$ and $Im[W_N^r]$ are latched into the LMA1010s input registers during S3. From Fig. 1(c), note that the $Im[X_m(q)]$ term is common to the expressions for B and D. Therefore, B and D can be simultaneously evaluated during S4 and the result stored in the corresponding LMA1010's accumulator. During S6, ALU1 and ALU2 control bits are set so that both L4C381s will act as subtractors. The contents of the MAC1 and MAC2 output registers are shifted into the input registers of the L4C381s. The other operands are the real and imaginary components of $X_m(p)$, $Re[X_m(p)]$ and $Im[X_m(p)]$ respectively, which has been shifted down the LPR520 pipeline registers during states S2, S3, S4 and S5. Referring to Figs. 1(c), 4, and 5, the real component of $X_{m+1}(q)$ is evaluated by ALU1 while the imaginary component is evaluated in ALU2. A new set of D and B values are also evaluated. The new D and B values correspond to the new set of $X_m(q)$ and W_N^r operands loaded into the MAC1 and MAC2 input registers

during S5. The real and imaginary components of $X_{m+1}(p)$ are evaluated in ALU1 and ALU2 respectively during S7. By holding the contents of the LPR520s, all the operands needed to obtain $X_{m+1}(q)$ during S6 are also available to obtain $X_{m+1}(p)$ during S7. The in-place computation is realized by storing $X_{m+1}(q)$, during S7, into the location in COMPLEX DATA FILE occupied by $X_m(q)$. In the same manner, $X_{m+1}(p)$ is loaded into $X_m(p)$ during S8.

From the state matrix of Fig. 5, note that a steady state condition occurs after, the state S6 such that a butterfly computation is completed every two cycles after an initial overhead of only 6 cycles. The efficient handling of the computation is largely aided by the flexibility of the LRF08 multiport register file. A good example is illustrated during state S3 when the real and imaginary components of a new $X_m(q)$ are written into register R4 and R5 via the B and C data input ports and at the same time "previous" $Re[X_m(q)]$, $RE[W_N^r]$ and $Im[W_N^r]$ are read out of register R0, R1 and R3 via the output ports A, D and E respectively.

Dealing with Overflow, Underflow and Precision

Overflow can occur at the front end when the input signal exceeds the full-scale range of the ADC. Depending upon the application, this can be prevented by using an automatic gain control (AGC) stage within the INPUT SIGNAL PROCESSOR or a hard limiting circuit to limit the maximum excursion of ADC. Another overflow condition involves exceeding the dynamic range of the fractional number representation. If the operands $X_m(p)$, $X_m(q)$ and W_N^r are fractions in fractional 2's-complement form, then the product of any of two operands is always a fraction. However, the FFT also involves accumulation of the product terms and the addition of two large positive fractions could result in an integer and a fraction. In this case the highest fractional number represented is exceeded and an overflow condition occurs.

From Fig. 3, the output of the LMA1010s are rounded to a 16-bit, single precision value and applied to the ALUs. However, the internal accumulation/subtraction process uses the full 35-bit double precision value. Overflow occurs when the MAC1/MAC2 operands are both –1.0, i.e., 8000H, and the product is added to an accumulator containing +1.0. One way of handling this is to provide a fixed divide-by-two scale factor by using the R31–R16 output bits of the MACs. Since the bits have the significance of 2^1 to 2^{-14}, the dynamic range is reduced by 1 bit, which might be unacceptable in certain applications. Another method is to limit the most negative number representation of the coefficient, W_N^r, to be –1.0 + 1 LSB (8001H). This guarantees the result of the multiplication/accumulation to be less than 2.0. In this case, the MACs R30–R15 output bits having the significance 2^0 to 2^{-15} are used and the dy-namic range is improved by 1 bit. Another potential source of overflow is at the ALU1 and ALU2 when the MACs outputs are added with the operands at the output of the LPR520s.

The modified butterfly cell, shown in Fig. 6, implements block-floating-point arithmetic to handle the potential overflows by means of the LSH32 32-bit Barrel Shifter/Normalizer. In this configuration, for a given stage of the FFT the ALU's outputs are fed into the SHIFT ENCODER LOGIC block. If either one or both the ALU's output is greater than 0.5, a shift code corresponding to the maximum output of either ALU is generated and latched. This is done because if either ALU's outputs is equal to or greater than 0.5 for the current FFT stage, then an overflow could occur during the next stage. To avoid this possibility, the shift code that is latched during the current stage is fed into the S14–S0 inputs of the LSH32s. Then during the next stage all the input operands are uniformly scaled down by shifting right.

Underflow can occur when two large negative fractions produce a result less than the most negative fractional number that can be represented by the system. The hardware that handles the overflow condition at the $X_{m+1}(p)$ output can be replicated and used to handle the underflow condition at the $X_{m+1}(q)$ output.

The addition of the LSH32 for input scaling certainly adds flexibility to the system at the expense of additional hardware. However, it may not be needed in applications where it is known that overflow or underflow cannot possibly occur. In this situation, only the sign bit (R31) and the 15 most significant fractional parts (R30–R16) at the LMA1010s outputs are applied to the input of the L4C381s. Regardless of the presence or absence of the LSH32s, the conversion to single precision result is obtained by rounding up the accumulator contents of the LMA1010s. Rounding up is done automatically by asserting the RND control bit of the LMA1010s. The performance rating of the Logic Devices' "functional building block" architecture is shown in Fig. 7 along with the single-chip DSP units. Note that although the instruction cycle time is approximately the same, the Logic Devices' architecture is close to an order of magnitude faster. It is also important to note that the 100 ns cycle time of the Logic Devices' architecture using high-speed CMOS components is comparable to architectures implemented with bipolar components with an added advantage of much lower power dissipation.

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Figure 6. Modified Butterfly Cell implements block-floating-point arithmetic to handle potential overflows.

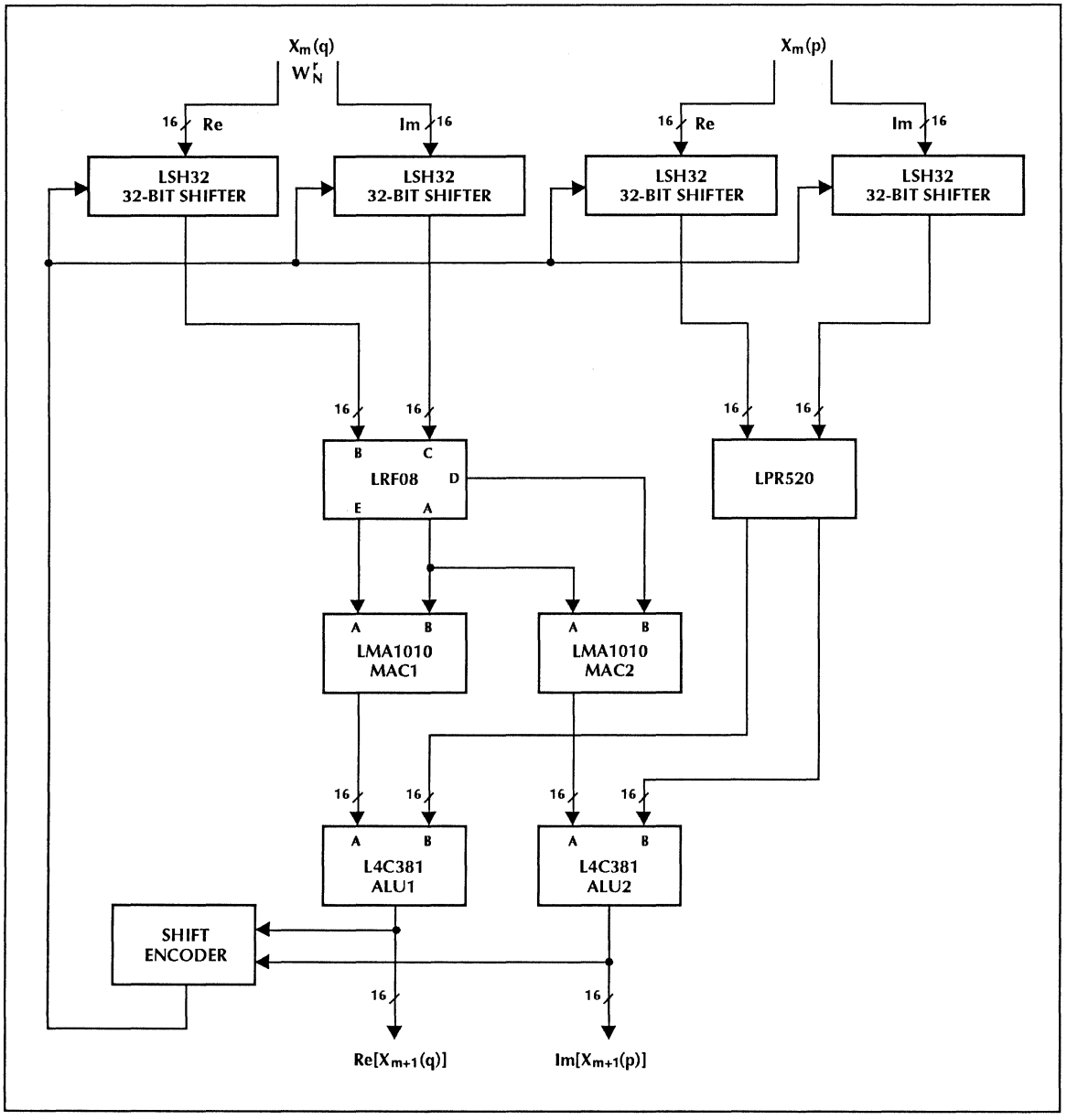

Figure 7. Performance ratings for different DSP units based on execution time of 1024-point, complex FFT.

DSP UNIT	MEMORY (1)	INSTRUCTION CYCLE TIME	1024-POINT COMPLEX FFT	SAMPLING RATE (MAX)
TMS32010 (TI)	144 x 16 -D -RAM 1536 x 16 -P -ROM	200 ns	75.9 ms (2)	13.1 kHz
µPD77230 (NEC)	2-512 x 32 -D -RAM 1K x 32 -D -ROM 1K x 32 -P -ROM	150 ns	10.75 ms (3)	100 kHz
LM32900 (NNational)	EXTERNAL	100 ns	13.42 ms (3)	78 kHz
ADSP2100 (Analog Dev.)	EXTERNAL	125 ns	7.2 ms (3)	142 kHz
LOGIC DEVICES (Fig. 3) BUILDING BLOCKS	EXTERNAL	50 ns	0.5 ms	2 MHz

References:

1. A. V. Oppenheim and R. W. Schafer, *Digital Signal Processing*, Prentice-Hall, Englewood Cliffs, NJ, 1975.

2. E. Macachor and G. McGlinchey, *Logic and Interfacing Aspects of High-Speed A/D Converters*, Wescon/81 Technical Paper.

3. J. H. Dedrick, *Multiport Register File Streamlines Signal Processing*, EDN, November 15, 1984.

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Multiport register file simplifies and speeds digital signal processing

A byte-wide eight-register chip with five independent ports overcomes bit-slice barriers and puts digital data into registers simultaneously with processing operations.

Bit-slice processors have achieved broad acceptance in digital signal processing. However, inflexibility and a small memory-to-register bandwidth limit their effectiveness for many applications.

For example, the transfer of data between registers and memory cannot often occur simultaneously with ALU processing.

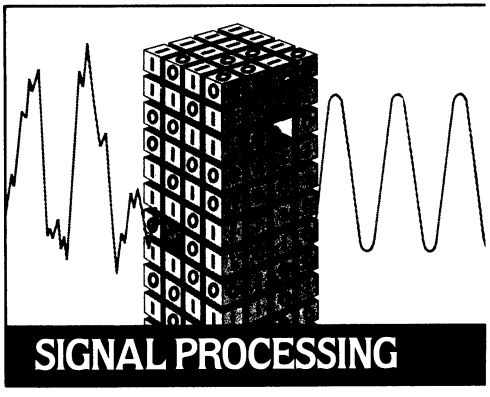
These limitations can be overcome with a multiport CMOS register file IC that not only increases signal-processing bandwidths, but also adds a new dimension of flexibility.

The file, the LFR08, contains eight registers of eight bits each and is easily expandable to more registers and wider words. The device has five independent parallel ports, each of which may be individually addressed to access any of the eight internal registers on a given clock cycle.

Two of the five ports, B and C, are write-only memory ports. Two, D and E, are read-only ports; and the fifth, A, is bidirectional. With so many ports, microprogrammable digital signal-processing systems take on new flexibility.

A closer look

Each of the five parallel ports has an 8-bit data bus, three address lines, and one or two control lines (Fig. 1). All address and control-line inputs are latched on the rising edge of the clock signal. During the following clock period, the addressed data is available at the read ports. Input data is latched on the rising



Joel H. Dedrick, Logic Devices Inc.

Joel H. Dedrick, director of product development, joined Logic Devices in Sunnyvale, Calif., in January. Earlier he worked with Texas Instruments, where he helped develop CMOS LSI signal processors and other digital signal-processing systems for military use. He earned his BSEE from the University of Nebraska and his MSEE from Southern Methodist University.

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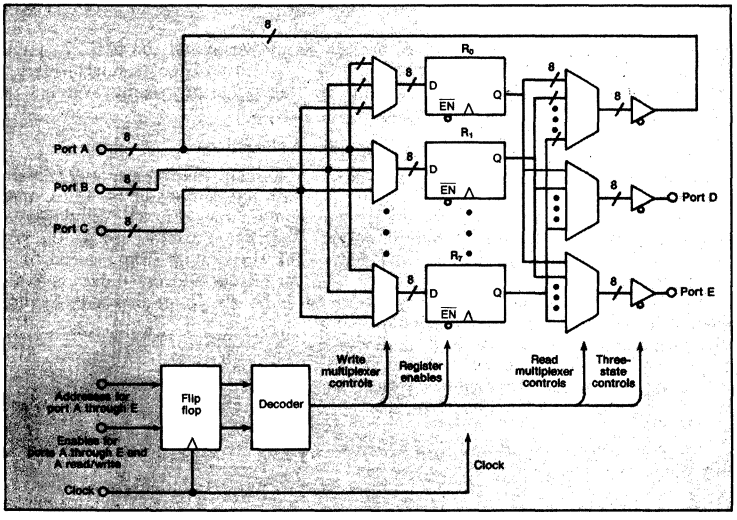
edge following application of the address. This timing allows for efficient use of the LRF08 in horizontally microcoded architectures with pipelining.

A logic low on the enable lines of ports D and E enables the corresponding three-state outputs, which in turn allows these ports to produce the contents of the register selected by address lines 0 through 2.

Input ports B and C are enabled in the same way. A logic low on their enable lines allows the selection of the target register for the write operation on the next rising clock signal after addressing. The addressing is similarly performed by B and C port address lines 0 through 2.

Because it is bidirectional, port A is served not only by address lines 0 through 2 and an enable line, but also a read/write line. The last line is latched with all other control lines to determine when port A will be used for reading or writing. When the read/write line is high, the A port is in the read mode, and its enable line functions as a three-state control line. When the read/write line goes low, the A port is in the write mode. Here its enable line functions the same as the port B and C enable lines for write clock cycles.

The five independent ports of the LRF08 also allow data to be transferred between the register file and external system memory. The transfer occurs while arithmetic operations



1. Five independently accessible ports that address eight 8-bit registers make the LRF08 multiport register file an extremely flexible chip in digital signal-processing circuits. The two output ports, D and E, are for reading only; the two input ports B and C, are for writing only; and the A port is bidirectional.

are being performed on data in the file and while the results are being returned to the file. If a register addressed for reading is the target of a write operation during the same clock period, the data at the output port will be the register contents prior to the write operation. Since the user can write to and read from any register during the same clock cycle, any of the eight registers can be used as accumulators for arithmetic operations.

With this five-port, eight-register flexibility, a word-slice approach to digital signal processing is available. It is superior to the traditional bit-slice approach, embodied in such parts as those in the Am2900 family, and a closer examination of the two architectures will show why.

In the bit-slice architecture of the Am2903, for example, each chip has a slice of the ALU and register file memory (Fig. 2a). The registers are in a three-port RAM—two read ports and one write. The read ports supply operands to the ALU, and the ALU feeds back results to the write port for storage.

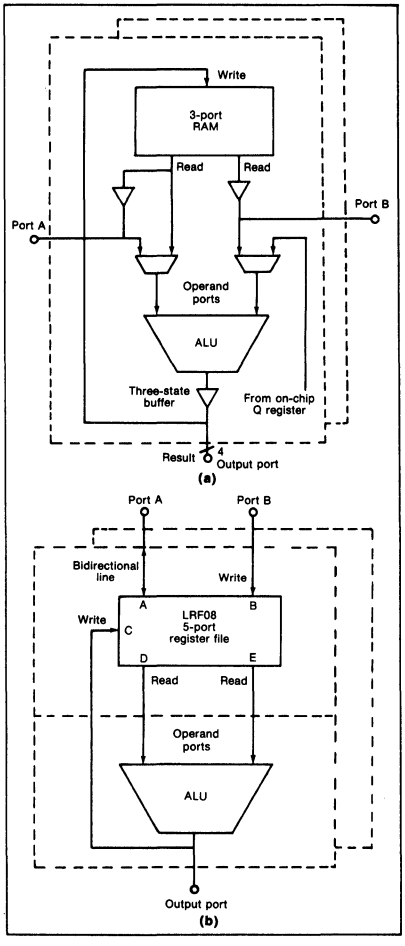
Writing external data to the registers of a bit-slice system can be performed in two ways. The ALU's output port can be disabled by use of an off-chip, three-state enable circuit. This allows the user to write in external data to the RAM through the feedback line.

Alternatively, off-chip multiplexers can be used to allow external data into the system through the two operand ports, A and B. Data is passed through the ALU and stored through the feedback line in the three-port RAM.

In many cases, the ALU's operation must be suspended, with resulting computational delays, while the external data is brought in.

As for reading data from a bit-slice system, it can be done at the output of the ALU or at the ALU's operand ports. In the latter case, ALU results are read out at the A and B ports simultaneously with ALU operations. This operation is useful for such applications as address generation for vector processing. Here, the address is read to the A port from the RAM and is simultaneously incremented by the ALU. The result is stored in the RAM in place of the old address.

The word-slice system, in contrast, is divided along functional boundaries, with the



2. The bit-slice architecture of processors like the Am2903 (a) limits the memory-to-ALU bandwidth and leads to delays when outside data is introduced, because the ALU's operation may have to be suspended while the external data is written into the three-port RAM. Using the LRF08 allows complete overlap of an ALU operand and result transfers with external read/write of the register set (b).

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register file and the ALU partitioned into separate chips (Fig. 2b).

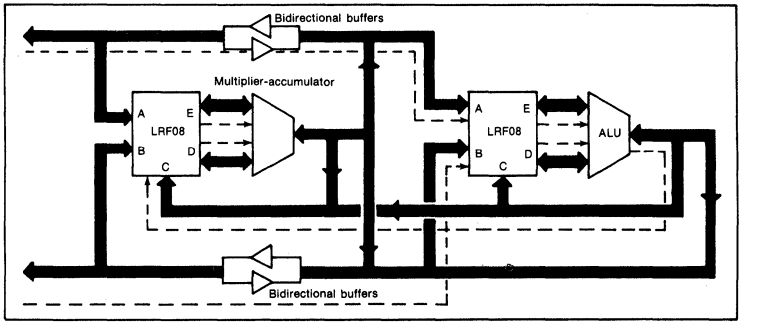
In the circuit shown, the data flow for dyadic operations (those that require two operands) is the same as that in the bit-slice system: Two operands are sent from the register file to the ALU, and the result is fed back to the register file through a write port. But there is a significant difference in the way data enters and leaves the circuit.

The most obvious difference in I/O organization is the fact that reading into and writing out of the register file can now be done simultaneously with ALU processing. In the bit-slice approach, the memory buses used for I/O are the same as those used for ALU operations. Thus unless the data is immediately used as an operand, ALU no-op instructions must be inserted to prevent register file read/write operations and ALU processes from conflicting.

With complex signal-processing algorithms, fetching data with the correct sequence and timing to avoid these no-op cycles is difficult, since only a limited number of independent address generators are available. True, the no-op states can be held down by the use of wide-word or complex (real plus imaginary) memory organizations, but then additional circuitry is needed to store the data temporarily, perhaps even rearrange it, for the ALU. With the completely independent I/O ports in the LRF08, all these problems are eliminated.

A more subtle advantage of the word-slice approach results from timing considerations in the design of the processor-memory interface. When data is multiplexed into the ALU at the operand ports in the bit-slice approach, provision must be made for sufficient setup time so that data can propagate through the ALU before the next rising edge of the clock signal.

Depending on the complexity of the instruction being executed, this setup time can range from 100 ns upward. Since many digital signal-processing system clock periods are 150 ns or less, a staging register is required be-



3. Used in a pipeline processor, the multiport register file makes reconfiguration easy. The large number of independent ports allows data routing through the system to be software controlled. The dotted lines show system data flow for a finite-impulse-response filter algorithm.

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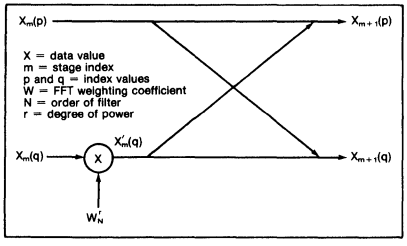
tween the external system memory and the ALU. The LRF08 essentially performs the function of such a staging register, reducing effective memory data setup time to 15 ns.

A reconfigurable pipeline processor

Consider the utility of the LRF08 in a reconfigurable pipeline processor, where two of the multiport register file ICs are paired with an ALU and a multiplier-accumulator (Fig. 3). The outputs of the ALU and multiplier-accumulator are fed back to their associated register files, and they may also be selectively gated onto auxiliary data buses running the length of the pipeline.

Bidirectional buffers on the data buses make them reconfigurable. System memory, which is accessed through ports A and B of each register file, can also be reconfigured for greater I/O bandwidth by the addition of memory ports to the buses. Likewise, the number of arithmetic elements, like the ALU and multiplier-accumulator, can be increased by a simple extension of each bus.

A typical application of the circuit shown is



4. In a radix-two decimation-in-time butterfly, the basic unit of the fast Fourier transform, four real multiplications and six real additions take place.

the finite-impulse-response (FIR) filter algorithm, frequently encountered in digital signal processing. For a nonrecursive Nth-order filter algorithm, each output sample consists of the sum of the past N points, each weighted by the appropriate filter coefficient. This can be expressed as follows:

$$Y_n = \sum_{k=0}^{N-1} h_k(x_{n-k})$$

where:

Y_n = the nth output sample
n = the data index
k = the coefficient index
N = order of filter
h_k = the kth coefficient
x = the input sample
x_{n-k} = input sample delayed by k sample periods

A key feature of the FIR filter algorithm is its linear-phase transfer characteristic. A necessary and sufficient condition for linear phase is that the coefficients of the filter be symmetric or antisymmetric about the center of the impulse response. Thus, for a filter with N coefficients, where the first coefficient has the value h_0, coefficient h_{N-1} must equal $\pm h_0$, and so on, from h_1 through $h_{(N/2)-1}$, with N being an even number. Such a filter can be expressed as:

$$Y_n = \sum_{k=0}^{(N/2)-1} h_k(x_{n-k} + x_{n-N+k+1})$$

The symmetry of the filter coefficients offers the possibility of computational shortcuts. By adding the input points corresponding to coefficients that are equal prior to weighting, the designer can reduce the total number of multiplications required for each output point to N/2. Although this reduction comes at the expense of an extra addition for each pair of input points, it offers the advantage of a 2:1 adder-to-multiplier ratio, typical of many signal-processor architectures.

The flow of data to implement the FIR filter is shown by dotted lines in Fig. 3. It is assumed that the filter coefficients are stored in the multiplier register file prior to entering the kernel (the smallest processing loop or itera-

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tion). Data enters the system from the memory ports and is placed in the ALU register file.

Points corresponding to a single coefficient are assumed to be read from memory simultaneously. If memory limitations preclude simultaneous readings, the designer can obtain an equivalent throughput by doubling the kernel length from one to two clock periods and processing input points four at a time. In this way adjacent points can be fetched from memory by a single address generator and a double-width memory organization.

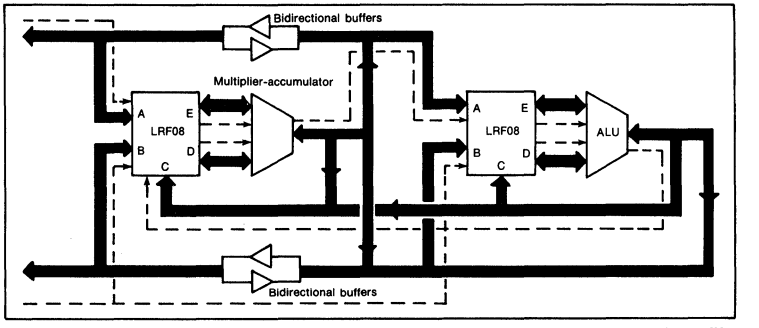
The addition of the two input values is accomplished in the ALU, and the result is fed back to the multiplier-accumulator register file. The file performs weighting and accumulation and holds the result until all pertinent input points have been processed.

Taking on the FFT

Yet another illustration of the flexibility of the LRF08 is its use for calculating fast Fourier transforms, a type of algorithm encountered frequently in digital signal processing. The fundamental unit of the FFT, the butterfly, is of interest. One of several common forms is the radix two, decimation-in-time butterfly (Fig. 4).

For complex (real plus imaginary) input data, the decimation-in-time butterfly requires four real multiplications and six real additions. The multiplications and two of the additions are used in the complex multiplication which phase-rotates the lower input, $x_m(q)$. The remaining four additions combine the upper input, $x_m(p)$, with the weighted lower input to produce the pair of complex output points, $x_{m+1}(p)$ and $x_{m+1}(q)$.

For this example, the weighting coefficients, W, are assumed to be stored in the multiplier-accumulator register file of Fig. 5 at kernel entry. In practice, the kernel is usually four or eight butterflies long. It takes advantage of the extensive symmetry in the weighting coefficients ($\pm 90°$ and $\pm 180°$ rotations, and reflections about the 45° axes). Thus, given one coefficient, three others may



5. The LRF08 multiport register file allows reconfiguration of the pipeline architecture for a different algorithm, in this case, the complex decimation-in-time FFT butterfly (Fig. 4).

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be calculated by sign changes in the real and imaginary parts of the complex input data. In this way the butterfly can be computed efficiently without the need for a memory dedicated to storage of the complex weights.

The data flow of the decimation-in-time butterfly in the figure is heavily pipelined. It has a net throughput of one complex output pair for every four clock pulses. The total pipeline delay is 12 clock periods. The table (below) shows a symbolic listing of the various data movements and arithmetic operations.

During the first two clocks of every four-clock iteration, the real and imaginary parts of $x_m(p)$ are read from memory to the multiplier-accumulator register file. This transfer of data occurs through the lower I/O port. The last two clocks are used for reading the real and imaginary parts of $x_m(q)$ from memory to the ALU register file. The paths of the data flowing from memory to the register are represented by dotted lines in the figure.

The second column in the table shows the complex multiplication of the weighting coefficient and the $x_m(q)$ input from the previous iteration. Results are passed to the ALU register file, where the additions needed to produce the real parts of the output values occur during the latter half of the iteration. This transfer of data is accomplished over the upper bus in the figure, a bus isolated from the memory port by bidirectional buffers.

The last column in the table shows the final iteration, when the imaginary portions of the results are calculated. These results are returned to the multiplier register file through the C port bus. Finally, the results stored in the multiplier file are sent out to the upper memory bus, one word during each of the four clocks of the iteration.□

How useful?	Circle
Immediate design application	556
Within the next year	557
Not applicable	558

Symbolic listing of operations for an FFT decimation-in-time butterfly iteration

	Multiplier $Re[X_m(p)] \rightarrow$ register file	$Re[X_m(q)] + Re[W_n'] \rightarrow$ accumulator	$Re[X_{m+1}(t)] \rightarrow$ output $Im[X_m(s)] + Im[X_m'(t)] \rightarrow$ multiplier register file
	Multiplier $Im[X_m(p)] \rightarrow$ register file	Accumulator $- Im[X_m(s)]^* \rightarrow$ ALU $Im[W_m'] \rightarrow$ register file	$Im[X_{m+1}(t)] \rightarrow$ output $Im[X_m(s)] - Im[X_m'(t)] \rightarrow$ multiplier register file
	ALU $Re[X_m(q)] \rightarrow$ register file	$Re[X_m(s)^* Im[W_n'] \rightarrow$ accumulator $Re[X_m(r)] + Re[X_m'(s)] \rightarrow$ multiplier register file	$Re[X_{m+1}(U)] \rightarrow$ output
	ALU $Im[X_m(q)] \rightarrow$ register file	Accumulator $+ Im[X_m(s)]^*$ $Re[W_n'] \rightarrow$ ALU register file $Re[X_m(r)] - Re[X_m(s)] \rightarrow$ multiplier register file	$Im[X_{m+1}(U)] \rightarrow$ output

Multiport register file streamlines signal processing

A register-file IC that incorporates five access ports and allows simultaneous use of its eight registers increases flexibility and throughput in signal-processing applications. But effective use of the part requires attention to new design concepts.

Joel H Dedrick, *Logic Devices Inc*

You can simplify signal- and image-processing system design by using a 5-port, 8-register IC. The LRF08 lets you design digital filters that you can reconfigure by reprogramming rather than by rewiring. Because it allows simultaneous use of its five ports, the LRF08 eliminates interference between I/O or memory transfers and arithmetic operations (see **box,** "Independent I/O ports yield flexibility").

The simultaneous use of ports is the LRF08's key feature. For example, while two read ports source operands to an ALU or multiplier, and a third write port records the result, the remaining two ports allow unimpeded data movement to external memory. These external data accesses don't interfere with arithmetic operations, so you don't need the Wait states or No Op cycles commonly found in less flexible architectures. You can thus increase throughput by as much as a factor of two for some algorithms. In addition, you can expand the device's eight 8-bit registers for greater word width or memory depth.

In contrast, most horizontally microprogrammed systems dedicate independent subsystems to memory-address and data calculations. Although memory addressing and data processing have different arithmetic requirements, both require that the calculations overlap efficiently with data storage and retrieval. To provide efficient overlap, such systems, especially those requiring data-dependent addressing, often use address generators to calculate a new data address on nearly every cycle while simultaneously storing or retrieving variables from system memory.

The LRF08's multiport write capability simplifies address generation, but it's not limited to that task: It's equally well suited to the data-handling and I/O portions of programmable-signal or image processors. Applications such as multiprocessor interfacing and shared-resource protection can also benefit from the LRF08's high bandwidth and flexible port structure.

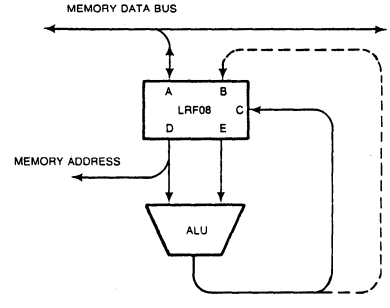

Fig 1—A pipeline address generator *comprising the LRF08 register file and an ALU uses the file's bidirectional A port for data transfers. The D port supplies the memory address as well as one of the ALU inputs. The E port supplies the remaining ALU operand while the ALU results return to the register file through the C port.*

To understand the concepts involved in application of the register-file IC, consider a data-address generator used in signal- or image-processing systems (**Fig 1**). The address generator, comprising an ALU and LRF08, uses the register file's D and E ports to source ALU operands. The ALU result returns via the C port. The bidirectional A port then serves as a data port for transferring register-file values to or from memory.

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Multiport register file requires new design techniques

Further, the A port's 3-state capability lets you wire this port directly to the system data bus. The D port, in addition to being used as an operand source, supplies the memory address.

The typical sequence for simple indexing operations (such as those required for vector addition and subtraction) is this: The system sources the accumulator register contents to the D port and the increment value (eg, 1) to the E port; the ALU performs an addition and returns the result to the accumulator. (Note that the register file's read-before-write operation allows you to use any register as the accumulator.) Thus, the effective address presented to memory is the accumulator value prior to the increment. The address increment occurs simultaneously with the memory access.

Now consider the addressing requirement that results when you apply an N×N space-invariant filter to 2-dimensional-image data stored in a linear memory. Such filtering helps to remove high-frequency noise from image data. The filtering algorithm consists of replacing each output-image pixel with the weighted sum of its neighboring pixels in the input image. In this case, define a pixel's neighbors as the pixels contained in a square, centered on the target pixel, with N pixels on each side (N odd). You can express this filtering operation as:

$$g(x, y) = \sum_{j=-\frac{(N-1)}{2}}^{\frac{N-1}{2}} \sum_{i=-\frac{(N-1)}{2}}^{\frac{N-1}{2}} h(i, j) f(x + i, y + j),$$

where g(x,y) is the output image, f(x,y) is the input

Independent I/O ports yield flexibility

The LRF08 high-speed CMOS multiport register file suits signal- and image-processing systems; it contains eight 8-bit registers accessible via five parallel ports **(figure).** Designated A through E, these ports each have eight data lines, three address inputs, and either one or two port-control lines. All address and control signals are latched on the clock's rising edge, so device activity is pipelined by one cycle (reads or writes occur one cycle following the cycle when corresponding controls are applied). This pipelining eliminates the need for discrete registers on microcontrol ROM outputs for microprogrammed applications.

The register file's D_0 to D_7 and E_0 to E_7 lines are output ports; DA_0 to DA_2 and EA_0 to EA_2 are their corresponding address inputs. An address applied to these inputs is latched at the clock's rising edge, and corresponding register contents appear on the data lines. $\overline{DOE}$ and $\overline{EOE}$ are the output-enable controls for the D and E ports, respectively; they control 3-state output drivers on the D_0 to D_7 and E_0 to E_7 lines. Asserting these inputs enables the corresponding port for output following the clock's next rising edge.

Write operations are processed in much the same way as read operations. B_0 to B_7 and C_0 to C_7 are input ports that write data to the LRF08's internal registers. You dictate the destination register for write operations with port-address lines BA_0 to BA_2 and CA_0 to CA_2. The address presented on these lines at the clock's rising edge gets latched and determines the destination register for a write operation on the next clock.

Port-enable inputs $\overline{BPE}$ and $\overline{CPE}$ allow selective control of B- and C-port write operations. To write to any port, you assert the corresponding port-enable control while presenting the write address. The control are latched along with the address lines, and an inactive port control causes the device to ignore the corresponding address input and suspend the write operation on that port during the next clock period.

The A port forms an interface to a bidirectional 3-state bus. The bidirectional A_0 to A_7 lines operate in conjunction with three address lines (AA_0 to AA_2), a port-enable control ($\overline{APE}$), and a read/write control (AR/$\overline{W}$). The AR/$\overline{W}$ input controls whether this port operates as a read or write port during the next clock cycle: Making this signal Low causes the A port to operate identically to the B and C ports, and you use the address lines and port-enable control to handle the write; a High input on AR/$\overline{W}$ makes it an output port with the $\overline{APE}$ line controlling the 3-state drivers on the A_0 to A_7 data lines similarly to the D- and E-port enables.

All ports are independent; the only usage restriction is that two ports can't write to the same register simultaneously. Two or more output ports can read a register simultaneously, though, and any other combination of address values and port enables is allowed. A final feature is useful for read-modify-write operations: When you read a register to an output port during the same cycle in which you write to it from an input port, the output data is the register contents prior to the write.

For further information on the LRF08 multiport register file.

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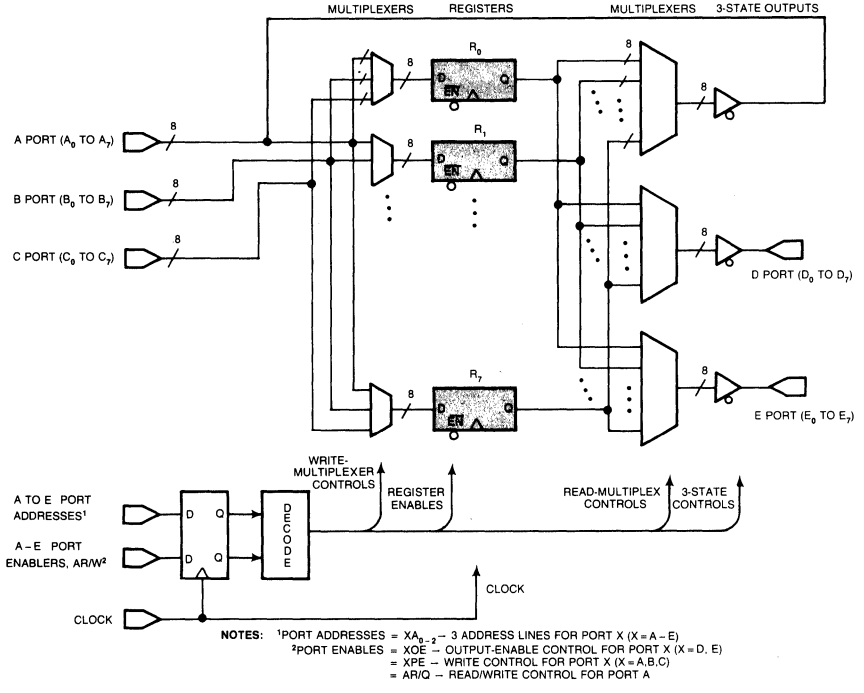
image, and h(i,j) is the filter's N×N impulse response.

Next, assume that the input image f(x,y) is stored in memory such that the increasing memory addresses scan left to right across the image, with the rightmost pixel of one row followed by the leftmost pixel of the row below it. Thus, to find the address of a pixel directly below a target pixel in an n-row×m-column image, you need only an address increment of m. Assume also that the input image f(x,y) is padded with (N-1)/2 Zero pixels around each border, corresponding to half the filter impulse response (**Fig 2**). This padding provides orderly filter calculations for elements near the image's edge.

Fig 3 gives a symbolic listing of the algorithm that implements the spatial filter. The left side of the Action column gives the required instruction words in a typical microprogrammed image-processing system. Looping and subsequent program flow control occurs simultaneously with data manipulation and doesn't require a separate microinstruction.

In this example, several assumptions have been made. First, assume that for every output-image point g (denoted G_{CENTER}), the filter function h(i,j) is centered over the corresponding input pixel F_{CENTER}, and all pixels covered by h are fetched in a left-to-right, top-to-bottom sequence. Also assume that the filtering functions operating on these points execute in a separate processing element, and that **Fig 4** shows only address-calculation operations. Finally, assume that the filter coefficients h(i,j) are stored in a separately addressed coefficient ROM (the algorithm could fetch them from RAM with some loss in throughput).



Five independent access ports *in the LRF08 register file direct data to and from eight registers upon proper manipulation of port-address and port-enable signals. The A port is bidirectional.*

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All five ports operate independently

The first two instructions (**Fig 3**) initialize the variables F_{CENTER} and G_{CENTER} to point to the upper left pixel in the input and output images, respectively. To accomplish this task, an offset is added to the F buffer's base address to account for the zero padding.

After initialization, the algorithm loops over all elements in the output image. For each new point in g, instruction 3 initializes a temporary index, k, to the filter function's upper left corner. This address is related to F_{CENTER} by the constant offset $-[(N-1)(N+m)/2]$. To fetch successive input-image pixels from memory, the system increments k by one at each step and applies the old value as the memory address. This process repeats for N cycles, where N corresponds to the number of pixels along the top of the filter impulse response h(i,j). When that row is completed, instruction 5 increments k by the image's width (m) to wrap processing back to the left edge of the impulse response area, on the next line down. This sequence of operations repeats for the impulse response's N rows until the output pixel's processing is complete.

After the algorithm has calculated a particular output pixel, instruction 6 stores the result in g while G_{CENTER} gets updated for the next pass. The LRF08 allows you to overlap address modification with memory operations by simultaneously reading and writing the G_{CENTER} register. Instruction 7 implements the corresponding update of F_{CENTER}. The process repeats for each pixel in a row of output array g. When all elements in the output rows have been processed, instruction 8 adds the offset $(N-1)$ to correct F_{CENTER} for input-image padding; this procedure wraps F_{CENTER} into the next line's first image pixel.

CYCLE	ACTION
1	$F_{CENTER} - F_{BASEADDR} + \frac{(N-1)(N+m)}{2}$
2	$G_{CENTER} - G_{BASEADDR}$ LOOP OVER n ROWS in g
3	LOOP OVER m PIXELS IN 1 ROW OF g $k - F_{CENTER} - [(N-1)(N+m)/2]$ LOOP OVER N ROWS IN h
4	LOOP OVER N PIXELS IN 1 ROW OF h FETCH f(k), $k - k + 1$
5	END LOOP $k - k + m$
6	END LOOP STORE g (G_{CENTER}), $G_{CENTER} - G_{CENTER} + 1$
7	$F_{CENTER} - F_{CENTER} + 1$ END LOOP
8	$F_{CENTER} - F_{CENTER} + (N-1)$ END LOOP

Fig 3—A symbolic listing of the spatial filter algorithm *shows that looping and other program flow control is performed simultaneously with data manipulation and doesn't require a separate microinstruction.*

In this application, data is efficiently accessed through the manipulation of multiple addressing variables, including several preloaded offsets and base addresses. The simultaneous use and updating of data pointers also improves throughput.

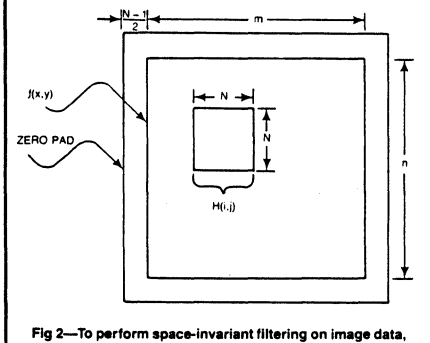

Fig 2—To perform space-invariant filtering on image data, *replace each pixel in the input image (f(x,y)) with the sum of its neighboring pixels (centered in an N×N square) weighted by h(i,j), the filter's impulse response.*

Bit reversal complicates FFTs

Now that you're familiar with the LRF08's basic operation, consider a specific application. To evaluate a fast Fourier transform (FFT) using a decimation-in-time algorithm, for example, a system must presort input data into bit-reversed order. "Bit reversed" refers to the following transformation: For an N-bit binary word A defined as

$$A = A_{n-1}2^{n-1} + A_{n-2}2^{n-2} + \ldots + A_1 2^1 + A_0 2^0,$$

you construct the bit-reversed word A by reversing the coefficients such that the new coefficient for 2^k is A_{n-1-k}:

$$A = A_0 2^{n-1} + A_1 2^{n-2} + \ldots + A_{n-2} 2^1 + A_{n-1} 2^0.$$

Thus, for this type of FFT algorithm, the system must provide data to working storage in bit-reversed order or perform the bit-reversal operation after the algorithm.

In either case, you can see the necessity for the efficient generation of bit-reversed addresses. You could accomplish bit reversal by hardwiring the conductors for each bit in reversed sequence (eg, at register inputs). But this rudimentary technique isn't generally the most efficient for two reasons: First, the FFT buffer doesn't usually require the entire machine address space. Instead, the algorithm uses only a small portion of a larger memory with the effective address consisting of the buffer base address plus an offset. This

factor complicates matters because only the offset portion must undergo bit reversal, while the base address remains in its usual form.

The second problem stems from the fact that most systems are required to execute FFTs of varying length. This flexibility requires the number of offset bits in the bit-reversal operation to be variable also. In addition, each offset bit's resulting position in the effective address word changes with the FFT's length.

Bit reversal with the LRF08

You can implement bit reversal with the LRF08, but note that the algorithm used is not widely known, so it deserves some explanation. The following notation defines desired operations:

- Base=base address of the FFT buffer.
- Offset=offset from base address to obtain effective address.
- Increment=increment used in indexing through the buffer (usually 1).
- W=bits in the machine address word.
- B=bits in the offset portion of the address ($B \leq W$).
- $BR_W(x)$=bit-reversal operation over W bits applied to x.
- $BR_B(x)$=bit-reversal operation on x applied over only the B least significant bits.
- $\bar{}A$=the variable A that has undergone the bit-reversal operation.

Using these definitions, the desired effective address becomes

$$\text{ADDRESS} = BR_B\,(\text{OFFSET}_B + \text{INCREMENT}_{n-1}) + \text{BASE}. \quad (1)$$

As noted, the difficulty with this form is that the $BR_B(x)$ operation is difficult to implement when x can vary. An easier-to-handle form of **Eq 1** is

$$\text{ADDRESS} = BR_w\,[BR_w\,(\text{OFFSET}_{n-1}) + BR_w\,\{BR_B\,(\text{INCREMENT})\}] + \text{BASE}. \quad (2)$$

In this form, the only occurrence of the bit-reversal operation not applied over the entire address word has a constant (the increment value) as its argument. In fact, the result of the BR_B operation becomes the argument of a full-width reversal. The resulting value is also a constant, which serves as a new increment for an indexing operation carried out in the upper end of the word. Note also that you generally map variables into hardware registers, so this operation's accumulator is represented by the first term inside the square brackets in **Eq 2** ($BR_W OFFSET_{n-1}$). The increment that's added to this accumulator comes from $BR_W(BR_B(\text{INCREMENT}))$, which equals $2(W-B)-1$ for an increment of 1.

CYCLE #	ACTION	MEMORY ADDRESS
1		$INADDR_n$
2	$\sim INADDR_n + \sim K \rightarrow INADDR_{n+1}$; $\rightarrow INADDR_{n+1}$	
3	$OUTADDR_n + 1 \rightarrow OUTADDR_{n+1}$	

Fig 4—A bit-reversed addressing operation *operates in a pipeline fashion. The memory address column shows the results of the calculations from the previous iteration of the action column.*

Now simplify **Eq 2** by using $\bar{}K$ to represent the new increment value and $\bar{}INADDR$ to represent the accumulator.

$$\text{ADDRESS}_{n-1} = BR_w\,[\bar{}INADDR_n + \bar{}K] + \text{BASE}. \quad (3)$$

This relationship establishes an equivalence between the accumulation of prereversed (over B bits) offset values as in **Eq 1**, and the accumulation of a corresponding constant increment value with full-width bit reversal of the result. **Eq 2** gives the origin of the new increment value.

A final note about computational efficiency: If the FFT buffer's base address resides on a 2^B boundary, you don't have to add the buffer base address because the base and offset fields are disjoint. In such a case, the desired base address undergoes a full-width bit reversal to become the initial input accumulator value $\bar{}INADDR_0$, and each successive iteration of **Eq 3** automatically produces the correct base+offset value.

Special hardware eases bit reversals

The previous discussion demonstrates the need for a flexible address generator in implementing efficient FFT designs. With one minor modification, you can adapt the LRF08-based architecture shown in **Fig 1** to calculate bit-reversed addresses efficiently for an arbitrary-length FFT buffer, starting at an arbitrary position within the machine space.

To implement this architecture, have the bit-reversed ALU output source the register file's B port. Note that the system applies the bit reversal over the full width of the address-generator word. As previously discussed, **Fig 4** is a symbolic listing of the bit-reversed addressing operation for the special case where the input buffer resides on a 2^B boundary. Each row represents all operations active during a given clock cycle, with the algorithm kernel requiring three clocks; the

Space-invariant image filter removes high-frequency noise

columns describe the action of the ALU and resulting memory addresses.

A key factor of **Fig 4** is that it gives a cycle-by-cycle description of the system, which performs two functions at once: It calculates a memory address in the middle column and then performs a memory read or write using that value in the next cycle while calculating the next required address. The system cycles repeatedly through these three steps.

Look at each cycle in detail. During the first clock period, the input address calculated during the previous iteration is sent to memory. The value comes from the D port (**Fig 1**) with no ALU operation executed, and a new input value is fetched.

During the second clock period, the register file adds the input-address accumulator $^{-}INADDR_n$) to the increment value (^{-}K), where those values follow the notation in **Eq 3**. The unit then stores the result simultaneously in two registers. The updated bit-reverse accumulator ($^{-}INADDR_{n-1}$) is stored in its original memory location via the B port. Finally, to effect the required bit-reversal operation, the register file produces the effective input address, $BR_W[^{-}INADDR_n + ^{-}K]$, by storing the sum in a different register via the C port.

In the last clock period, the register file simultaneously increments the non-bit-reversed accumulator $OUTADDR_n$ and supplies it as the output buffer address. As with the input address, the system should initialize this accumulator to the buffer's base address.

EDN

Author's biography

Joel H Dedrick is director of product planning for Logic Devices Inc (Sunnyvale, CA). Before joining that firm, he worked at Texas Instruments, where he helped to develop several signal-processing systems for radar and sonar applications as well as CMOS LSI devices for military signal-processing systems. He earned his BSEE degree from the University of Nebraska (Lincoln) and his MSEE from Southern Methodist University (Dallas, TX). Joel enjoys woodworking, snow skiing, and entertaining his baby daughter.

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