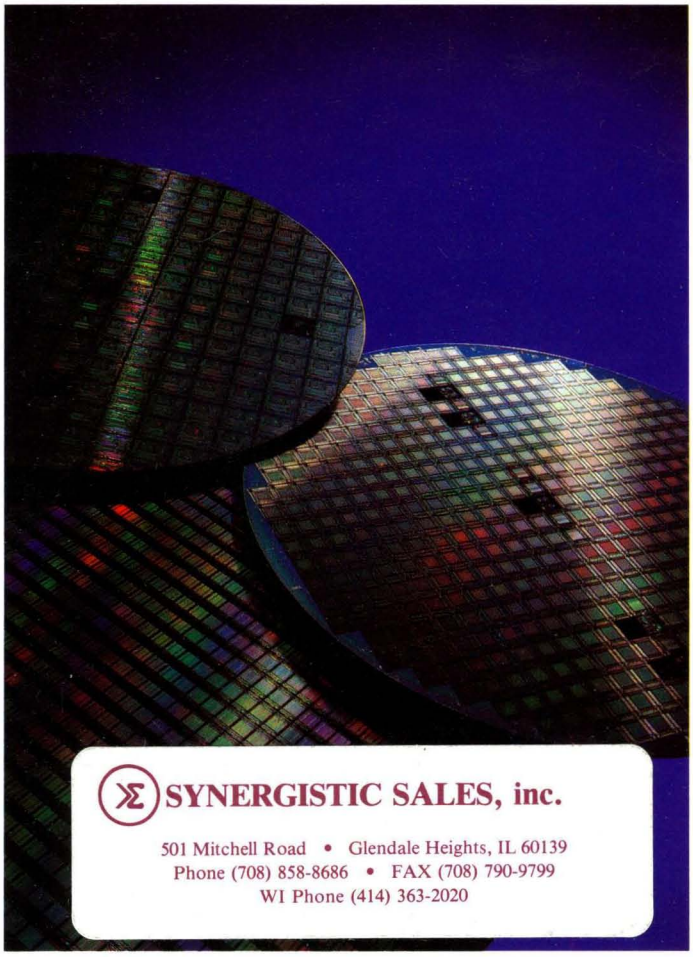
MEMORIES



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1990

MHS

MEMORIES

MHS

GENERAL INFORMATION

MHS BACKGROUND

MATRA MHS was formed in 1979 as a joint venture company beetween MATRA of France and HARRIS Corporation of the United States. Its charter was to develop a leading CMOS design and manufacturing operation in Europe.

In the early 80's, MHS reached its objectives and became a pioneer with several novative products, especially CMOS static memories.

Then, several other agreements contributed to MHS development.

In 1981, MHS signed an agreement with Intel Corp. covering the manufacture of NMOS circuits in Nantes, France and the establishment of a joint design facility for telecom chips and video controllers (82716).

Resultingly, MHS manufactured Intel's 8086, 8088, 8051 and 8052, as well as Harris' 80C86/88.

MHS was also entitled to desing CMOS versions of the 8051 MCU family. The 80C51 and its derivates have become one of MHS major successes, while fabrication of 16 bit MPU and NMOS devices was stopped, to concentrate on CMOS MCU.

In 1985, a joint venture was created between MHS and SGS Microelettronica to develop a fully automated assembly and test line for integrated circuits.

In a deal with Cypress, MHS received licensing rights to manufacture Cypress fast 16 K, 64 K and 256 K CMOS SRAMs and utilize Cypress fast 1.2 and 0.8 micron processes for MHS designs as well.

With France's national Telecom research labs (CNET), MHS developed an advanced sub-micron process, named Super-CMOS, to combine speed and low power consumption *(see page 4)*. This process is in production at MHS since 1988, while most new devices are designed to run on it.

Recently, MHS and NEC also signed a second-source agreement covering mutual manufacture and design rights of NEC's 78312A 16 bit microcontroller family.

MHS INDUSTRIAL CAPABILITY

MHS plant in Nantes (western France) includes a 2,000 m^2, class 10 wafer fab which is capable to produce 100,000 125 mm wafers per year.

Around 15 million integrated circuits are shipped every year by MHS.

The Nantes operation also has its own assembly and test lines, as well as R & D and Quality departments.

This factory has been fully qualified by most major military and space agencies according to their highest standards ; its quality has also been praised by some of the world's most demanding I.C. users.

MHS SALES NETWORK

MHS has its own worldwide sales and distribution network, with direct subsidiaries in Paris, Munich, London, Milan, Stockolm, Santa-Clara, and Hong-Kong.

These locations also have a technical center to ensure local support for MHS' expertise inintegration and ASIC design.

MHS PRODUCT OFFERING

MHS offering includes four main product lines, all in CMOS ; most circuits are available in commercial, indusrtrial, and military temperature ranges.

MHS is also a leading European manufacturer of Hi-Rel devices for military, aeronautics and space applications : its factory has been certified AQAP-1 and a variety of products have been listed by the corresponding agencies.

MICROCONTROLLERS

The 8051 family in CMOS, with a complete palette of options :

- ROM capacity from 4 K to 32 Kbytes : 80C51, 80C52, 83C154, 83C154D.
- Low-voltage (2.7 V), fuse-protected "secret ROM", high-speed (20 MHz) versions.
- Quick ROM service : three weeks for ROM code customization.
- and a specific single-chip keyboard controller : 80C752.

STATIC RAMs

- **fast** 16 K & 64 K devices : HM65728/767/768 (down to 15 ns) & HM65764/787-790 and a fast 8 K x 9 : HM65779, and 256 K devices 65756/65797/65798
- **very low-power** 16 K and 64 K memories (6 transistors per cell) : HM65162/262 and HM65641 (8K x 8, 55 ns, 1 µA)
- **"ultimate"** 64 K SRAM, such as HM65664/65687/65688 : 35 ns, 1 µA
- application-specific memories.
- ECL SRAM 256 x 4 and 1 K x 4 in BICMOS process technology. Access time : 3 ns.

DATACOM PRODUCTS

- a family of combo devices (HC3054/57) compatible with a market standard
- specific chips for modem applications, the 29C42 error correction circuit for V42/LAP M Modems, the HC55421 X21 interface, etc.

MHS is introducing a range of circuits dedicated to ISDN applications : rate adaptators (29C93), HDLC and ECMA102 multiplexed controllers, video codecs...

These products can be used in Terminal Equipments or at the Network Termination end.

They are targeted for the upcoming generation of equipment requiring powerful, flexible and low-cost components.

CMOS ASIC

- Five **gate-array** families, with gate-counts from 250 up to 55,000 gates, ultra-fast CMOS arrays, proprietary and standard software tools running on VAX, SUN, or turnkey systems such as DAISY, MENTOR, VALID, HP.
- Two families of **Composite arrays** mixing optimized blocks (RAM, ROM, & others) with regular arrays of gates.
- Specific **smart software** for system analysis and logical synthetisis.
- Digital and/or analog **custom designs** capabilities using standard software from Silicon Compilers Systems Corp. : GDT and genesil.
- Field technical centers in most of its subsidiaries.

MHS DIFFERENTIATION

After having successfully proved its ability to provide the electronic market with quality CMOS standard products as well as ASICs, MHS has decided to offer additional and newer solutions for system integration.

We named it : "THE TOOLBOX".

It combines our best strengthes :

- A unique sub-micron process : the Super-CMOS.
- A proven experience in making microcontrollers, SRAM, ASIC and Telecom chips which results in our mastering several of the most frequent functionalities needed in modern electronic systems.
- A design methodology based the availability of the above functions in a building block form, and a set of advanced design tools - including silicon compilation - which allows to mix them on a single I.C. as required.
- The total flexibility of these tools, which offers the possibility to develop most specific product in gate-array, composite array, or optimized silicon, according to our customer needs, expressed in terms of time-to-market, prototype cost, and production price.
- A team of very capable system and device architects, fully dedicated to analyze and discuss our customers' needs, in order to choose with them the best suited architecture and mean of integration to completely satisfy their specific requirements.

The above concept has been working so well that we have developped priviledged relations with our customers. As a result, we are able to move with them through the frontier between standard and user specific I.C. We are diluting this frontier ; our customer's experience has fertilized our tool box, and MHS's constantly richer tool box allows us to propose more and smarter solutions every day.

With our customers, we became :

A CONSULTANT IN INTEGRATION
and
AN EXPERT IN INTEGRATION

ALTERNATIVES FOR SYSTEM INTEGRATION

Each of the below criteria come from one or several different departments of our customers : marketing, design, manufacturing, and purchasing or finance. Program managers will evaluate the appropriate trade-offs, depending on the context of each program, including technical, market, and other specific factors.

This will help in choosing with MHS the best suitable solution and planning, taking into account possibilities offered by MHS to shift or evolve from one solution to another one at a further program stage.

SAMPLE OF CRITERIA	STANDARD CIRCUITS & PLD, GATE-ARRAYS	FULL CUSTOM CIRCUITS	COMPOSITE ARRAYS	OPTIMIZED* PARTITION
Breadboarding	++	–	–	+
Fast redesign	++	–	++	+
Level of integration	–	++	+	+
Complex systems	–	+	+/–	++
Flexibility	++	–	+	++
Technical risks	+	–	+	+
Test & emulation	++	–	+	++
Development cost	++	–	+	+
First production cost	–	–/+	+	+
Mature production cost	–	++	+	+
Second source	++	–	+	+
Confidentiality	–/+	++	+	+

(+ = satisfactory ; – = poor)

* **Note :** the optimized partition is a multi-chip solution based on standard circuits and composite arrays, for which the balance of criteria is often more favorable than solutions using custom circuits.

MHS SCMOS PROCESS

1. MHS COMMITMENT TO CMOS

For development and fabrication of the most advanced integrated circuits in both the ASIC and standard product fields MHS has made and stick to the choice of CMOS technology. A lot of developments and progress have been made from the initial 4 µm CMOS process, back in 1980, to the most recent processes bearing on materials, device physics or lithography which allow now the new technology to provide speed and high integration density on top of the traditionnal virtues of CMOS : low power consumption, wide voltage and temperature operating range or high noise immunity.

These continuous efforts made by the company in a very focused way around CMOS led MHS to the introduction in 1988 of the Super CMOS (SCMOS) technology on which most of the new MHS integrated circuits are now built or developed.

One single process however cannot fulfill all product requirements, and for this purpose complementary developments have been performed to derivate from a generic technology process varieties more suited to particular needs as presented below.

2. THE SCMOS PROCESS

Co-developed with the France's National Telecom Research Laboratory (CNET) the SCMOS goal has been to offer a generic process as described here before with submicronic minimum features to provide a very high speed potential as well as maximum integration capability. Such advantages however should not be gained against reliability characteristics which are of prime importance in highly integrated system especially for avionics or space application. For all these reasons special options have been taken in building up the process as can be viewed on the cross section of the double metal version of SCMOS. Let's review the key points of that construction :

THE SUBSTRATE

The latch-up phenomenon has always been a major concern of CMOS technology, that triggers parasitic thyristor which can generate very high current flows resulting in circuit non functionnality of destruction. By using special electrical structure on circuits I/O's and adopting careful layout rules inside the chips, accuity of the problem has been greatly reduced on MHS products. However, shrinking down the dimensions requires new solutions. Building the devices in a shallow high resistive layer epitaxially grown on very low resitivity substrate has proven its efficiency in killing the latch-up phenomenon. By using such P+ epitaxial wafers in SCMOS, voltage drops, induced by current injection in the substrate, are greatly reduced, while chance of triggering the parasitic SCR is close to zero, resulting in potential latch-up free circuits.

THE DEVICES

To guarantee high operation frequency of products, it is necessary to move toward submicronic transistor size in new processes. SCMOS emphasizes this trend as 0.8 micron drawn devices reach electrical channel length as low as 0.65 micron for the N channel transistor thus conferring high speed potential to the circuits.

Short channels - however - have several drawbacks that needed to be considered in SCMOS to guarantee reliable operation and keep high performance :

- To prevent punchthrough effects, such as voltage limitations and subthreshold currents degrading the circuit standby power consumption, in-depth study and optimization of transistor ion implant have been carried out.
- When going to short channel length, very high electrical fields are applied to electrons in the devices and the chance for those carriers to get enough energy to be injected in gate oxide becomes significant. This "hot electron" effect creates voltage and transconductance shifts that degrade device and circuit reliability. To counter this threat on SCMOS, both P and N channel transistors are built with LDD structures. This "Lightly Doped Drain" structure reduces the electrical fields in the devices drain vicinity thus lowering the probability of hot electron emission.

These two examples illustrate, among other actions, the particular care that was taken in designing the SCMOS devices to get the best performances without giving up any in reliability.

THE GATE MATERIAL

Used to build the transistor gates and being the first interconnection layer, this level has to have as low resistivity as possible. The SCMOS technology achieves that goal by replacing the polysilicon material by a bilayer of polysilicon which keeps the transistor threshold voltage characteristics, and Titanium Silicide which provides the low resistance. A tenfold improvement has been obtained through this solution, lowering typical value of this layer from 30 ohm/square down to 3 ohm/square. A great benefit results for all product performances and especially for memory, for which long word lines use to be realized with the gate level.

THE DOUBLE METAL SYSTEM

More and more circuits now require an enhanced routing capability, either to achieve higher integration density (memories), or to allow automation in placement and routing tasks (ASIC). If multilayer interconnection is a necessity, several limitations however have to be overcome to implement it efficiently in very dense technology. Among the concerns of double metal systems let us mention the silicon metal interface, the metal step coverage, the risk of hillock formation generating shorts

between metal layers, contact filling, intermetal dielectric planarization, via-contact stacking constrain, and electromigration.

Here again, with SCMOS, an innovative solution has been chosen to address most of these problems : it stands in the utilization of Tungsten as the first metal material, followed by a planarized intermetal dielectric before deposition of the 2nd metal layer using aluminium material.

Among other properties, Tungsten can be deposited by chemical vapor deposition technique which leads to better topology coverage, and offers the possibility of contact filling by an autoplanarization mechanism. Advantage is taken of this characteristic in allowing the stacking of vias and contact to interconnect the 2 metal layers. Such a possibility autorizes tighter metal pitches thus saving area in repetitive structures and interconnections.

Other advantages come with tungsten utilization, including better reliability resulting from the very good electromigration endurance of this material.

Through these specific developments, adding to the basic works in new techniques around lithography (direct stepping on wafers) or material deposition and etching as well as manufacturing engineering works, MHS as been able to master this advanced CMOS process.

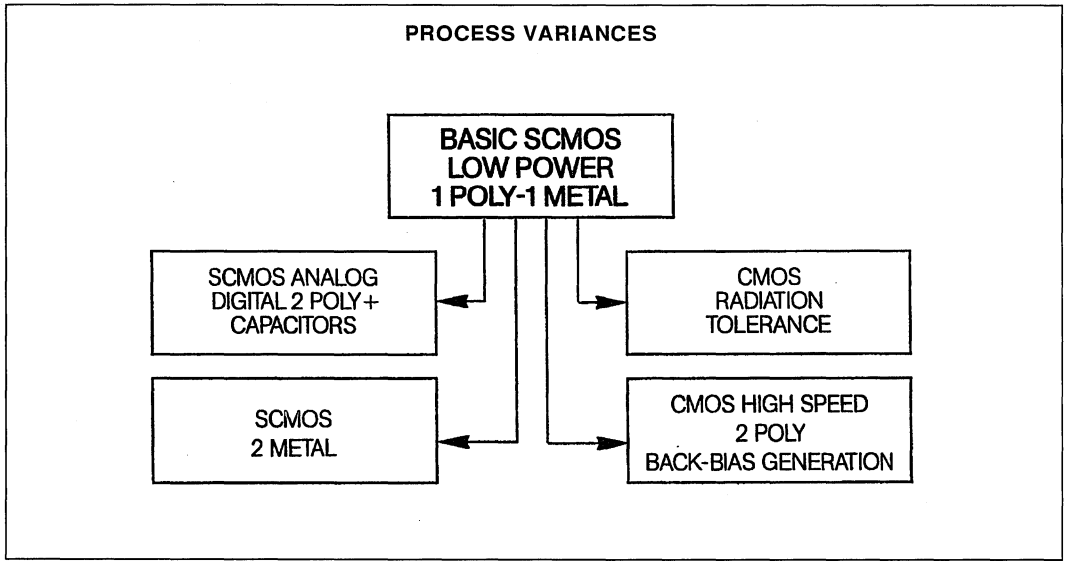
With its characteristics, of which an abstract is given in *table 1*, the SCMOS appears as a key technology for the next 5 years. Thanks to innovative options that were made, it also bears the basics for future enhancements : it is already prepared for an analog version of the same process and for even smaller lithographies (0.7 and 0.5 µm).

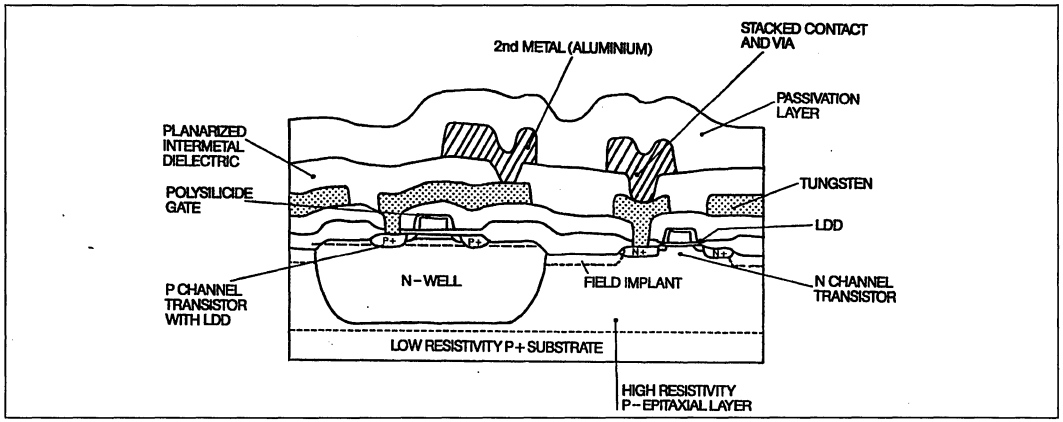
Gate oxide thickness	200 A
Electrical channel length • NMOS transistor • PMOS transistor	 0.65 µm 0.9 µm
Minimum drawn features	0.8 µm
Metal 1 pitch	2.9 µm
Metal 2 pitch	3.4 µm
Propagation delay	120 ps/gate
Integration density	25000 transistor/mm^2 (RAM)

Table 1.

PRODUCT REQUIREMENTS

PRODUCTS	NEEDS	PROCESS
MICROCONTROLLER OR COMPLEX LOGIC	Digital high density	CMOS
DATACOM	Mixed analog digital	CMOS analog
MEMORIES	High density High speed	CMOS High speed
ASIC	Flexibility routeability	CMOS multilayer





MHS LITTERATURE

In order to provide our customers with a more exhaustive and regularly updated information, MHS has now split its data book into several handbooks.

Following volumes are available :

MICROS - MEMORIES - DATACOM - ASIC - GRAPHIC - HI-REL.

Each volume includes all data pertinent to its topic : data-sheets, application and technical notes, software/progamming manuals, as well as a cross-reference guide to common industry equivalents, if any.

Last chapters deal with general information : quality and reliability, dice/wafer form products, dice geometry index, package selection & dimensions guides, and sales network.

Separate documents, as well as updated information, can be obtained through MHS sales network.

DATA SHEET CLASSIFICATION

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview	Formative or design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information	Sampling or pre-production	This is advanced information, and specifications are subject to change without notice.
Preliminary	First production	Additional data may be published at a later date. MHS reserves the right to make changes at any time without notice, to improve design and supply the best possible product.

PRODUCT INDEX

HANDBOOK	TOPIC
8 BIT MICROCONTROLLERS	80C51/C31 ; 80C51-L/C31-L ; 80C51F ; 80C51S/C31S ; 80C52/32 ; 83C154 ; 83C154D ; 80C732/752.
16 BIT MICROCONTROLLER	78312/310 78312A/310A.
MEMORIES	HM 65687/688/664/767/768/770/772/728/787/788/789/790/791/764/779/797/798/799/795/796/756/162/262/641/161/6116L/6207/65231.
DATACOM	29C93/94/95, 29C42/43, 29C80/82/84. HC 55421/5570A/3052/3053/3054/3057.
ASIC	MA, MB, MAF, MC/MCR, MBM, MCM, CMOS Foundry, Macrocell 6402/I2C, Macrocells in Development, MA & MB Summary, Daisy, Mentor, Valid, Hewlett Packard, Gateaid II Vax, Superdesigner, Gasp.

MHS : A WORLD LEADER IN 80C51 FAMILY OF MICROCONTROLLERS

In 1985, MHS became a pioneer in CMOS microcontroller by introducing the CMOS version of the popular 8051.

Beyond the well-known advantages of CMOS such as low-power consumption, MHS design offered a fully static core, allowing chip operation down to zero MHz clock without data loss.

MHS kept on leading the way by continuoulsy introducing innovative versions :

1986 : - a low-voltage version (80C51-L) operating with V_{CC} down to 2.7 V,

1987 : - a "secret ROM" version (80C51F) with which simply blowing a fuse allows to protect ROM content from being read or dumped by any mean,

- the first CMOS version of 8052 : 8 K ROM and three timers.

1988 : - 16 K bytes of ROM and additional features with the 83C154,

- the "Quick ROM" service : a precious advantage providing our customers with customized ROM parts in less than 3 weeks (80C51 and 80C52),

- the long awaited 20 MHz version : 80C51S,

- a complete keyboard controller, integrated in one single I.C. : 80C752.

All above devices have been successful around the world in a wide variety of applications : over 8 million parts have been shipped.

MHS has more versions, more packages, more temperature ranges and screening levels than any other vendor on this family of microcontroller, for which MHS is by far the first european source.

1989 : - for software-greedy applications : at last a 32 K ROM device : 83C154D,

- piggy-back circuits 80C51 PX

- and a very clever solution for integrated systems...

If your already know most of all this, we will still surprize you. If you did not so far, trying MHS might help you to catch-up with those who know !

PRODUCT INDEX

PRODUCT INDEX

ULTIMATE CMOS SRAM (high speed & low power)

FORMAT	PART NUMBER	COMMERCIAL	INDUSTRIAL	MILITARY	PAGE
64 K x 1	**HM 65687**	35-45 ns	45-55 ns	45-55 ns	3-3
16 K x 4	**HM 65688**	35-45 ns	45-55 ns	45-55 ns	3-13
8 K x 8	**HM 65664**	35-45 ns	45-55 ns	45-55 ns	3-23

HIGH SPEED CMOS SRAM

FORMAT	PART NUMBER	ACCESS TIME/GRADE			PAGE
		COMMERCIAL 0 – 70°C	INDUSTRIAL – 40, + 85°C	MILITARY – 55, + 125°C	
16 K x 1	**HM 65767 (A)**	15-55 ns	–	25-55 ns	4-3
4 K x 4	**HM 65768 (A)**	15-55 ns	–	25-55 ns	4-11
4 K x 4 with $\overline{OE}$	**HM 65770**	20-45 ns	–	25-45 ns	4-21
4 K x 4 with Sep I/O	**HM 65772**	20-45 ns	–	25-45 ns	4-29
2 K x 8	**HM 65728 (A)**	20-55 ns	–	35-55 ns	4-37
64 K x 1	**HM 65787**	20-55 ns	25-55 ns	25-55 ns	4-47
16 K x 4	**HM 65788**	20-55 ns	25-55 ns	25-55 ns	4-57
16 K x 4 with $\overline{OE}$	**HM 65789**	20-55 ns	25-55 ns	25-55 ns	4-65
16 K x 4 with Sep I/O	**HM 65790**	25-55 ns	35-55 ns	35-55 ns	4-75
16 K x 4 with Sep I/O Transparent Write	**HM 65791**	25-55 ns	35-55 ns	35-55 ns	4-85
8 K x 8	**HM 65764**	25-55 ns	35-55 ns	35-55 ns	4-95
8 K x 9	**HM 65779**	25-55 ns	35-55 ns	35-55 ns	4-105
32 K x 8	**HM 65756**	35-45 ns	35-55 ns	35-55 ns	4-115
256 K x 1	**HM 65797**	25-45 ns	35-55 ns	35-55 ns	4-123
64 K x 4	**HM 65798**	25-45 ns	35-55 ns	35-55 ns	4-131
64 K x 4 with $\overline{OE}$	**HM 65799**	25-45 ns	35-55 ns	35-55 ns	4-139
64 K x 4 with Sep I/O	**HM 65795**	25-45 ns	35-55 ns	35-55 ns	4-147
64 K x 4 with Sep I/O & Transparent Write	**HM 65796**	35-55 ns	45-55 ns	45-55 ns	4-149

ECL SRAM

FORMAT	PART NUMBER	COMMERCIAL	INDUSTRIAL	MILITARY	PAGE
256 x 4	MM 10E422	3-7 ns	–	–	5-3
256 x 4	MM100E422	3-7 ns	–	–	5-3
1024 x 4	MM 10E474	3-7 ns	–	–	5-9
1024 x 4	MM100E474	3-7 ns	–	–	5-9

VERY LOW POWER CMOS SRAM

FORMAT	PART NUMBER	COMMERCIAL	INDUSTRIAL	MILITARY	PAGE
2 K x 8	**HM 65162**	55-70 ns	70-85 ns	70-85 ns	6-3
16 K x 1	**HM 65262**	55-70 ns	70-85 ns	70-85 ns	6-13
8 K x 8	**HM 65641**	55-70 ns	70-85 ns	70-85 ns	6-23

GENERAL PURPOSE CMOS SRAM

FORMAT	PART NUMBER	COMMERCIAL	INDUSTRIAL	MILITARY	PAGE
2 K x 8	**HM 6116**	120 ns	120 ns	CS*	7-3
2 K x 8	**HM 65161**	70 ns	80 ns	CS*	7-11

* Consult sales.

1

SMART MEMORIES

FORMAT	PART NUMBER	COMMERCIAL	INDUSTRIAL	MILITARY	PAGE
Dual Port RAM Controller	**HMC 6207**	–	–	–	8-5
Dual Port RAM 2 K x 8	**HM 65231**	–	–	–	8-3

2

CROSS REFERENCE

CROSS REFERENCE

Following data only reflect MHS's best interpretation of available industry literature, and might include some errors, for which MHS cannot be held responsible.

MEASURE CONDITIONS

PARAMATER	CONDITIONS	
Access time		All figures are max at 70 dec. C
Stand-by current	CS = V_{CC} – 0.3 V V_{IN} < V_{CC} – 0.2 V or < 0.2 V	
Operating current	V_{CC} max Iout = 0 mA Duty cycle 100 % Freq. max V_{IN} = V_{CC} or Gnd	

FORMAT	VENDOR		MIL (1)	MHS PRODUCT	MIL (1)	MHS ADVANTAGES
16 K x 1			Yes	**HM 65767**	Yes	Equivalent Performance
	Fujitsu	MB81C67	Yes	**HM 65767**	Yes	Faster, Lower Consumption
	Harris	HM65262	Yes	**HM 65262**	Yes	Faster, Eq. Consumption
	Hitachi	HM6167L	No	**HM 65262**	Yes	Faster, Lower Consumption
	IDT	IDT6167SA	Yes	**HM 65767**	Yes	Equivalent Performances
	NEC	µPD431	No	**HM 65262**	Yes	Faster, Lower Consumption
	Thomson	MK41H67	No	**HM 65262**	Yes	Lower Consumption
4 K x 4			Yes	**HM 65788**	Yes	Equivalent Performance
	Fujitsu	MB81C68A	Yes	**HM 65768**	Yes	Faster, Lower Consumption
	Hitachi	HM6168HL	No	**HM 65768**	Yes	Faster
	Inmos	IMS1420/21	No	**HM 65768**	Yes	Faster, Lower Consumption
	IDT	IDT6168LA	Yes	**HM 65768**	Yes	
	NEC	µPD4314	No	**HM 65768**	Yes	Faster
	Thomson	MK41H68	No	**HM 65768**	Yes	Faster
	Toshiba	TMM2068AD	No	**HM 65768**	Yes	Faster, Lower Consumption
4 K x 4 SEP I/O			Yes	**HM 65772**	CS(2)	Faster, Eq. Performances
	IDT	61682LA	Yes	**HM 65772**	CS	Faster
4 K x 4 with OE	Cypress	CY7C170	Yes	**HM 65770**		Faster, Lower Consumption
	Toshiba	TMM2078AD	No	**HM 65770**		Faster, Eq. Consumption
2 K x 8			Yes	**HM 65728**	Yes	Faster, Eq. Consumption
			Yes	**HM 65728**	Yes	Faster, Eq. Consumption
	Harris	HM65162	Yes	**HM 65162**	Yes	Lower Consumption
	IDT	6116SA	Yes	**HM 65162**	Yes	Lower Consumption
	Toshiba	TMM2018AD	No	**HM 65728**	CS	Faster, Eq. Consumption
	Fujitsu	MB8418L	No	**HM 6116B**	CS	Faster, Lower Consumption
	Fujitsu	MB8417/18	No	**HM 6116B**	CS	Faster, Lower Consumption
	Hitachi	HM6116L	No	**HM 6116B**	CS	Faster, Lower Consumption
	NEC	µPD446-L	No	**HM 6116B**	CS	Faster, Lower Consumption
	Toshiba	TC5516	–	**HM 6116B**	CS	Faster, Eq. Consumption
	Vitalic	V6C16L	No	**HM 6116B**	CS	Faster, Lower Consumption

(1) Also available in military temp. range.
(2) Consult sales.

CROSS REFERENCE (continued)

FORMAT	VENDOR		MIL (1)	MHS PRODUCT	MIL (1)	MHS ADVANTAGES
64 K x 1			Yes	**HM 65787**	Yes	Equivalent Performances
	Fujitsu	MB81C71	No	**HM 65787**	Yes	Faster, Eq. Consumption
	Toshiba	TC5561	No	**HM 65687**	Yes	Faster, Lower Consumption
	Toshiba	TC5562	No	**HM 65787**	Yes	Faster, Lower Consumption
	Hitachi	HM6287L	No	**HM 65687**	Yes	Lower Consumption
	IDT	IDT7187L	Yes	**HM 65687**	Yes	Lower Consumption
	NEC	µPD3461C	No	**HM 65687**	Yes	Faster, Lower Consumption
	Thomson	MK71H87	No	**HM 65687**	Yes	Lower Consumption
	Mitsubishi	M5M5187	No	**HM 65687**	Yes	Lower Consumption
16 K x 4			Yes	**HM 65788**	Yes	Equivalent Performances
	Fujitsu	MB81C74	No	**HM 65788**	Yes	Faster, Eq. Consumption
	AMD	AMD99C164	Yes	**HM 65788**	Yes	Faster, Eq. Consumption
	IDT	IDT7188	Yes	**HM 65688**	Yes	Lower Consumption
	NEC	µPD4362C	No	**HM 65688**	Yes	Faster, Lower Consumption
	Hyundai	HY62C88L	No	**HM 65688**	Yes	Lower Consumption
	Mitsubishi	M5M5188	No	**HM 65688**	Yes	Lower Consumption
	Vitelic	V61C62	No	**HM 65688**	Yes	Faster, Lower Consumption
16 K x 4 with OE			Yes	**HM 65789**	No	Equivalent Performances
	IDT	IDT6198L	Yes	**HM 65789**	No	
	NEC	µPD4363C	No	**HM 65789**	No	Faster, Eq. Consumption
16 K x 4 SEP I/O			Yes	**HM 65790**	No	Equivalent Performances
	IDT	IDT6198L	Yes	**HM 65790**	No	
8 K x 8			Yes	**HM 65764**	Yes	Equivalent Performances
	Harris	HM65642	Yes	**HM 65664**	Yes	Faster, Lower Consumption
	IDT	7164S	Yes	**HM 65764**	Yes	Faster, Eq. Consumption
	Toshiba	TC5563APL	No	**HM 65664**	Yes	Faster, Lower Consumption
	Fujitsu	MB8464	No	**HM 65664**	Yes	Faster, Lower Consumption
	Hitachi	HM6264L	No	**HM 65664**	Yes	Faster, Lower Consumption
	NEC	µPD4364C	No	**HM 65664**	Yes	Faster, Lower Consumption
	Thomson	MK48H64	Yes	**HM 65664**	Yes	Lower Consumption
	Fujitsu	MB81C78	No	**HM 65764**	–	Faster, Eq. Consumption
8 K x 9	Fujitsu	MB81C79	–	**HM 65779**	–	Faster, Eq. Consumption
	Toshiba	TMM2089	–	**HM 65779**	–	Equivalent Performances

(1) Also available in military temp. range.

3

ULTIMATE STATIC RAM

High Speed and Low Power

MHS

DATA SHEET

HM 65687

64 k x 1
ULTIMATE CMOS SRAM

3

FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 45/55 ns (max)
  COMMERCIAL : 35/45 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 175.0 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55 TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

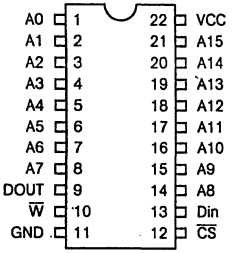
DESCRIPTION

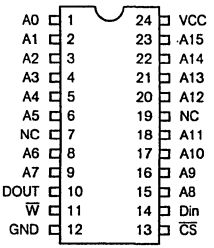
The HM 65687 is a very low power CMOS static RAM organized as 65536 x 1 bit. It is manufactured using the MHS high performance CMOS technology named super CMOS.
With this process, MHS is the first to bring the solution for applications where fast computing is a mandatory as low consumption, such as the aerospace electronics, the portable instruments or PC's.
Utilising an array of six transistors (6T) memory cells, the HM 65687 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.
The HM 65687 is processed following the test methods of MIL STD 883C.

PACKAGES

Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.
SOIC & SOJ* 300 mils, 24 pins DIL
LCC, 22 pins.

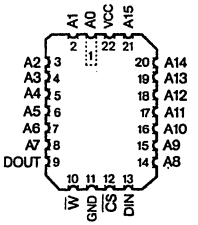
Pinout DIL 22/24 pins (top view)



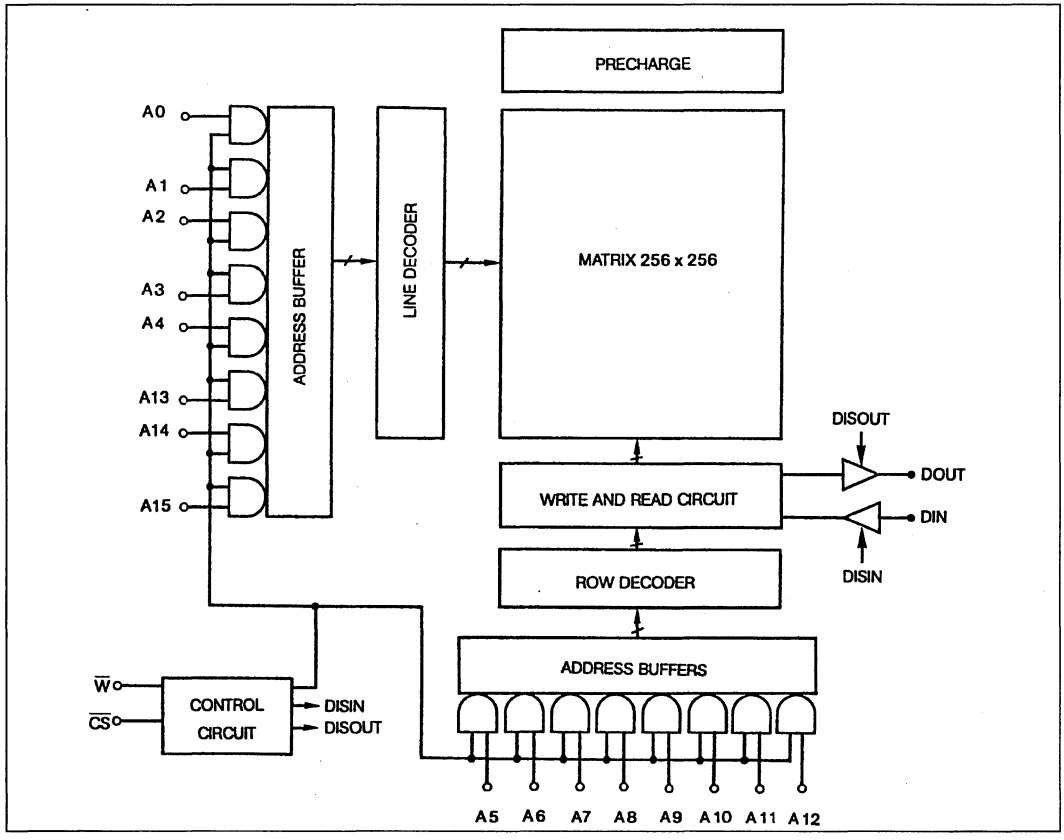


* preliminary

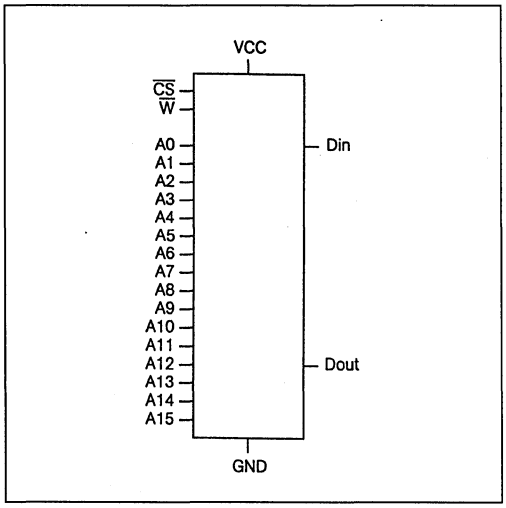
Pinout LCC 22 pins (top view)



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0–A15	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	V_{CC}	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = High impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	V_{CC} ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	V_{CC} ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	V_{CC} ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc		Supply Voltage	4.5	5.0	5.5	V
Gnd		Ground	0.0	0.0	0.0	V
VIL	(1)	Input Low Voltage	– 0.3	0.0	0.8	V
VIH		Input High Voltage	2.2	–	VCC + 0.3 V	V

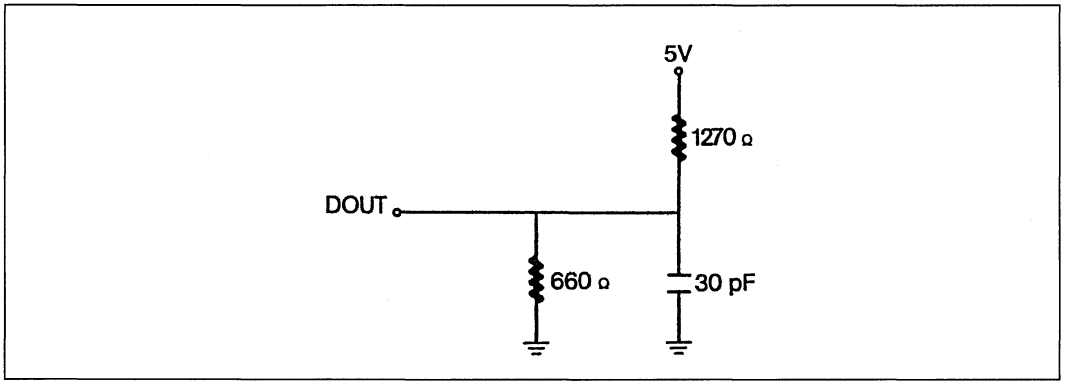
Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(2)	Input capacitance	–	–	5	pF
Cout	(2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

OUTPUT LOAD



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65687 B-5	65687 S-5	65687 -5	65687 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	10	15	10	15	mA	max
ICCSB1	(6)	Standby supply current	1.0	100.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	10	15	10	15	mA	max
ICCOP	(8)	Operating supply current	50	75	50	75	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65687 B-9	65687 S-9	65687 -9	65687 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65687 B-2	65687 S-2	65687 -2	65687 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

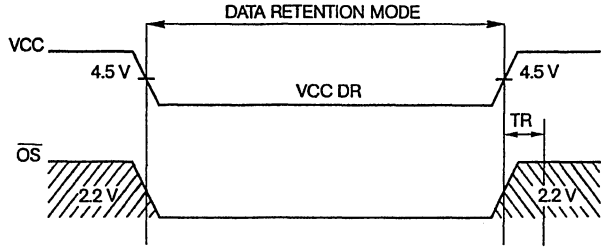
Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA.
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V
2. $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions
3. The RAM can begin operation > 35 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselected to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	@ 2.0 V : HM-65687 (B)-5	–	0.1	1.0	µA
	HM-65687 (B)-9	–	0.1	3.0	µA
	HM-65687 (B)-2	–	0.1	20.0	µA
	HM-65687S/C-5	–	0.1	30.0	µA
	HM-65687S/C-9	–	0.1	30.0	µA
	HM-65687S/C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-65687 (B)-5	–	0.3	1.0	µA
	HM-65687 (B)-9	–	0.3	3.0	µA
	HM-65687 (B)-2	–	0.3	30.0	µA
	HM-65687S/C-5	–	0.3	50.0	µA
	HM-65687S/C-9	–	0.3	50.0	µA
	HM-65687S/C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 30 pF

WRITE CYCLE : Commercial specification

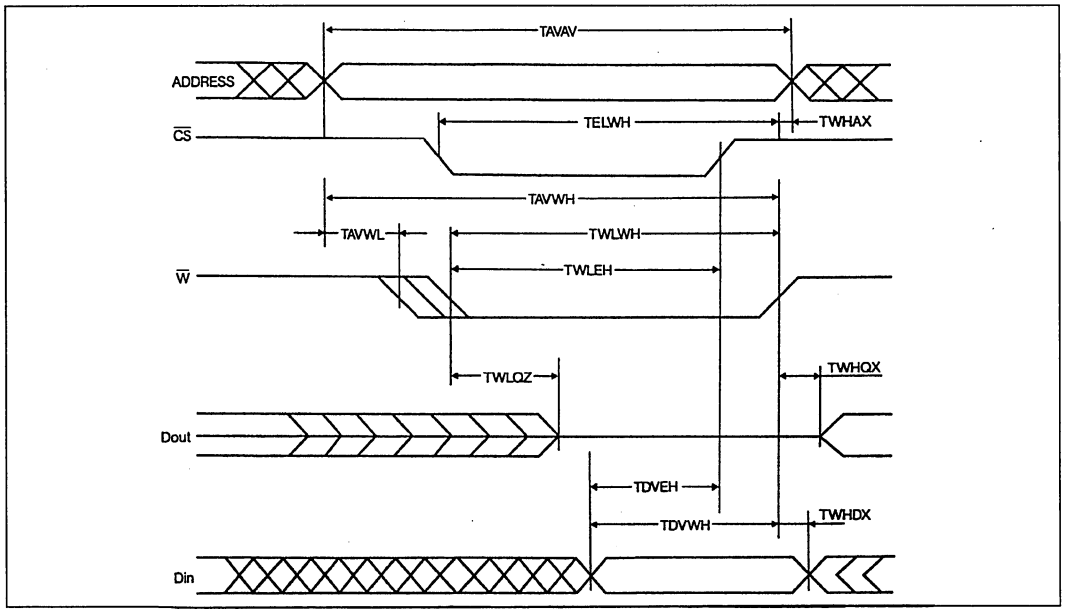
SYMBOL	PARAMETER	65687 B-5	65687 S-5	65687 -5	65687 C-5	UNIT	VALUE
TAVAV	Write cycle time	35	35	45	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	35	35	45	45	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	35	35	45	45	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	30	30	40	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

WRITE CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65687 B-9/2	65687 S-9/2	65687 -9/2	65687 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE



Note : The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE : Commercial specification

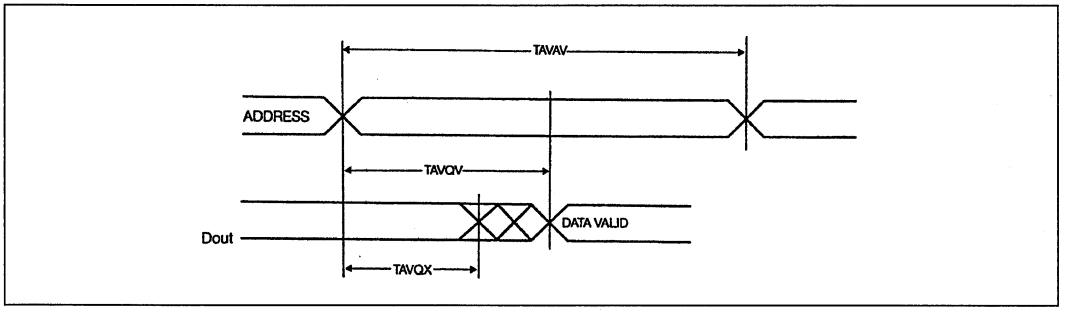
SYMBOL	PARAMETER	65687 B-5	65687 S-5	65687 -5	65687 C-5	UNIT	VALUE
TAVAV	Read cycle time	35	35	45	45	ns	min
TAVQV	Address access time	35	35	45	45	ns	max
TAVQX	Address Valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	40	40	50	50	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQZ	$\overline{CS}$ high to high Z	35	35	45	45	ns	max

3

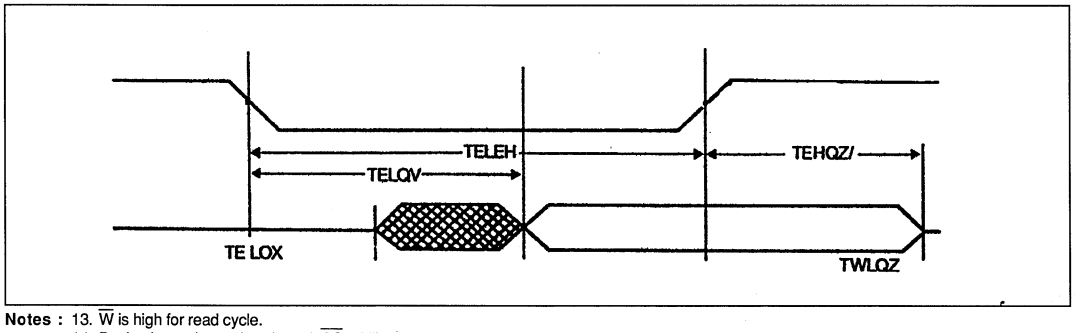
READ CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65687 B-9/2	65687 S-9/2	65687 -9/2	65687 C-9/2	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address Valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	50	50	65	65	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQZ	$\overline{CS}$ high to high Z	45	45	55	55	ns	max

READ CYCLE nb 1 (notes 13, 14)



READ CYCLE nb 2 (notes 13, 15)



Notes : 13. $\overline{W}$ is high for read cycle.
14. Device is continuously selected, $\overline{CS}$ = VIL.
15. Address valid prior to or coincident with CS transitive.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65687	B	– 5
0 - Chip form 1 - Ceramic 22 pins 3 - Plastic 22 pins - 300 mils 4 - LCC 22 pins T - SOIC 24 pins U* - SOJ 24 pins	64 k x 1 Ultimate CMOS static RAM	B - high speed/low current S : high speed/standard current Blank : standard speed/low current C : standard	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

* preliminary

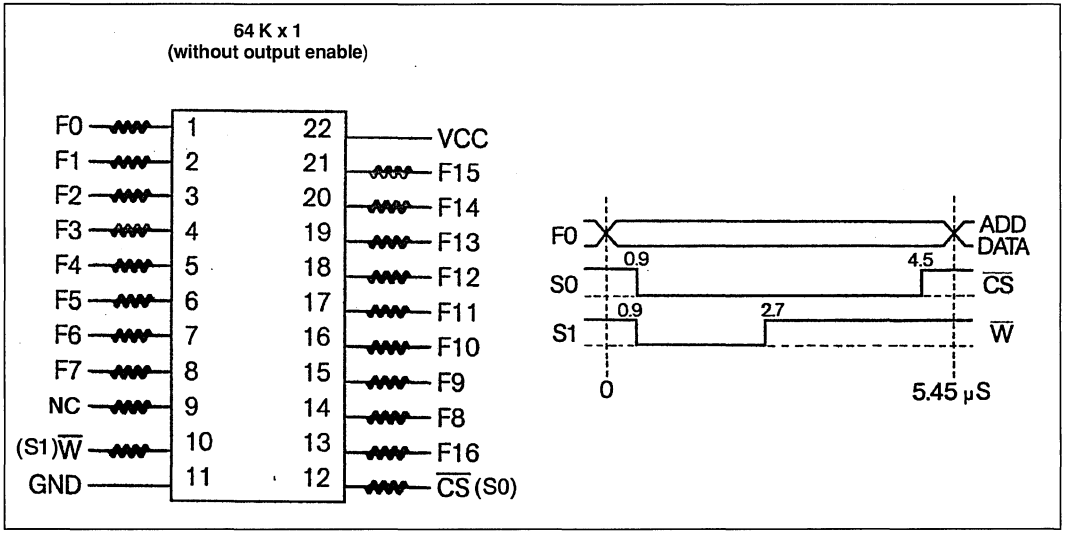
3

PACKAGE OUTLINE

For the packaging information, refer to chapter 10

Package reference : Plastic DIL, 300 mils, 22 pins : X41
Ceramic DIL, 300 mils, 22 pins : forthcoming
SOIC DIL, 300 mils, 24 pins : TBD
LCC rectangular, 22 pins : L16.

BURN-IN SCHEMATICS



VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin

F0 = 91.6 KHz ± 20 %
Fn = 1/2 F n-1

S0 & S1 : programmable signals for write / read cycles

NC = Non connected.

DATA SHEET

HM 65688

16 k x 4
ULTIMATE CMOS SRAM

3

FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 45/55 ns (max)
  COMMERCIAL : 35/45 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 175.0 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55 TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

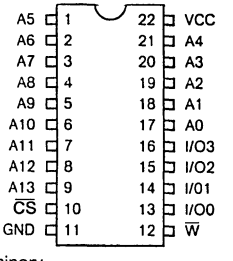
DESCRIPTION

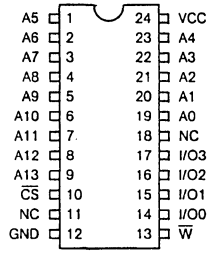
The HM 65688 is a very low power CMOS static RAM organised as 16384 x 4 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.
With this process, MHS is the first to bring the solution for applications where fast computing as mandatory as low consumption, such as the aerospace electronics, the portable instruments or PC's.
Utilising an array of six transistors (6T) memory cells, the HM 65688 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The HM-65688 is processed following the test methods of MIL STD 883C.

PACKAGES

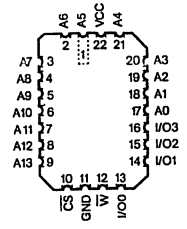
Plastic 300 mils, 22 pins, DIL
Ceramic 300 mils, 22 pins, DIL
SOIC & SOJ* 300 mils, 24 pins, DIL
LCC, 22 pins

Pinout DIL 22/24 pins (top view)



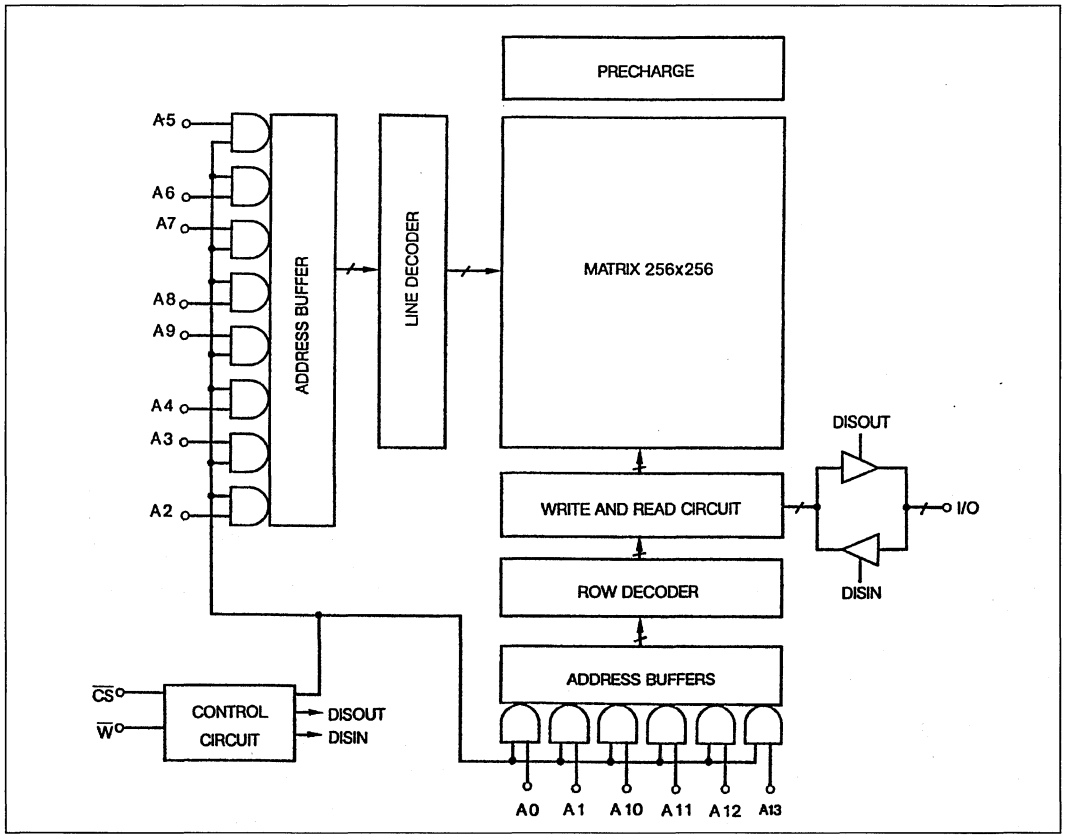


Pinout LCC 22 pins (top view)

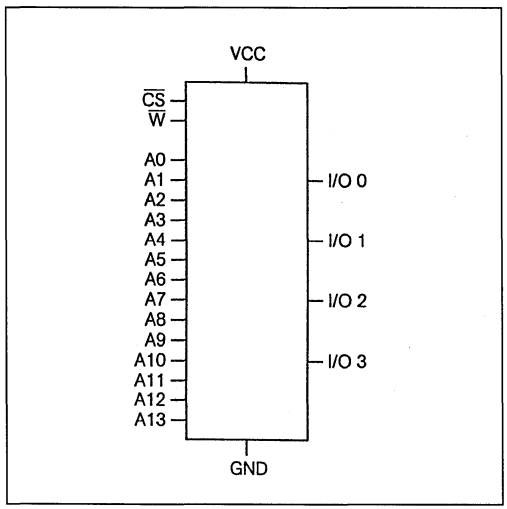


* preliminary

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A13 : Address inputs	GND : Ground
I/O0-I/O3 : Inputs/Outputs	$\overline{CS}$: Chip-Select
Vcc : Power	$\overline{W}$: Write Enable

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial (– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial (– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3V	V

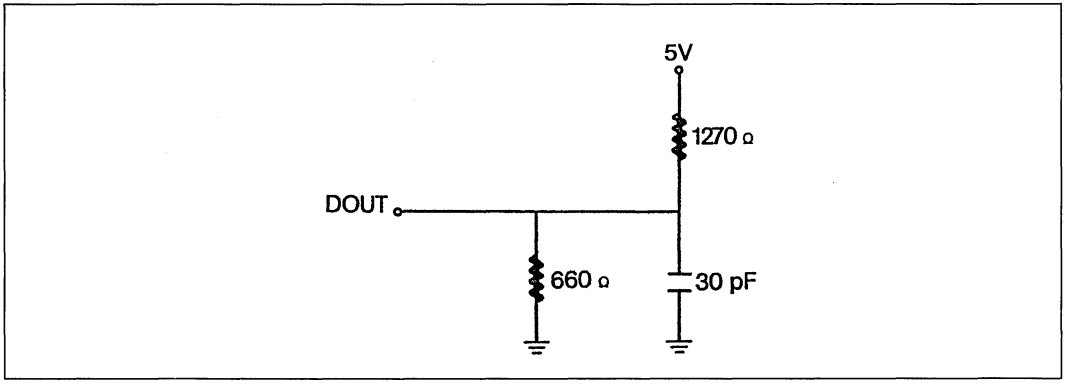
Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	5	pF
Cout (2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

OUTPUT LOAD



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65688 B-5	65688 S-5	65688 -5	65688 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	10	15	10	15	mA	max
ICCSB1	(6)	Standby supply current	1.0	100.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	10	15	10	15	mA	max
ICCOP	(8)	Operating supply current	50	75	50	75	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65688 B-9	65688 S-9	65688 -9	65688 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65688 B-2	65688 S-2	65688 -2	65688 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

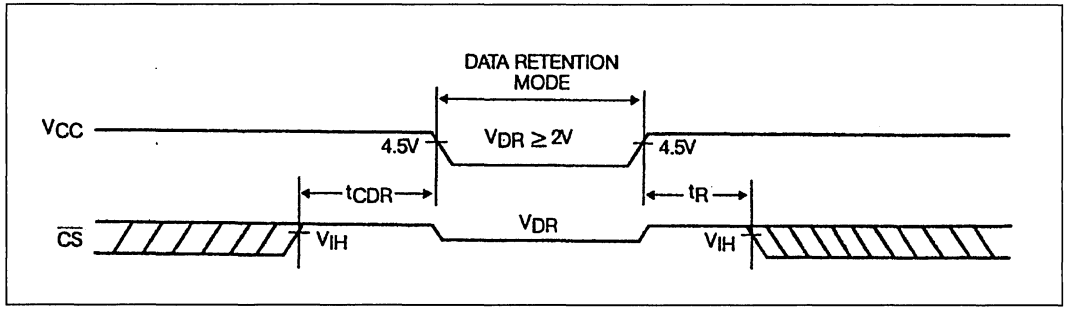
Notes : 5. $\overline{CS} \geq VIH$.
6. $\overline{CS} \geq Vcc - 0.3$ V, Iout = 0 mA.
7. $\overline{CS} \leq VIL$, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3V.
2. $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
3. The RAM can begin operation > 35 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselected to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (10)	Data retention current				
	@ 2.0 V : HM-65688(B)-5	–	0.1	1.0	µA
	HM-65688(B)-9	–	0.1	3.0	µA
	HM-65688(B)-2	–	0.1	20.0	µA
	HM-65688S/C-5	–	0.1	30.0	µA
	HM-65688S/C-9	–	0.1	30.0	µA
	HM-65688S/C–2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-65688(B)-5	–	0.3	1.0	µA
	HM-65688(B)-9	–	0.3	3.0	µA
	HM-65688(B)-2	–	0.3	30.0	µA
	HM-65688S/C-5	–	0.3	50.0	µA
	HM-65688S/C-9	–	0.3	50.0	µA
	HM-65688S/C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 30 pF

WRITE CYCLE : Commercial specification

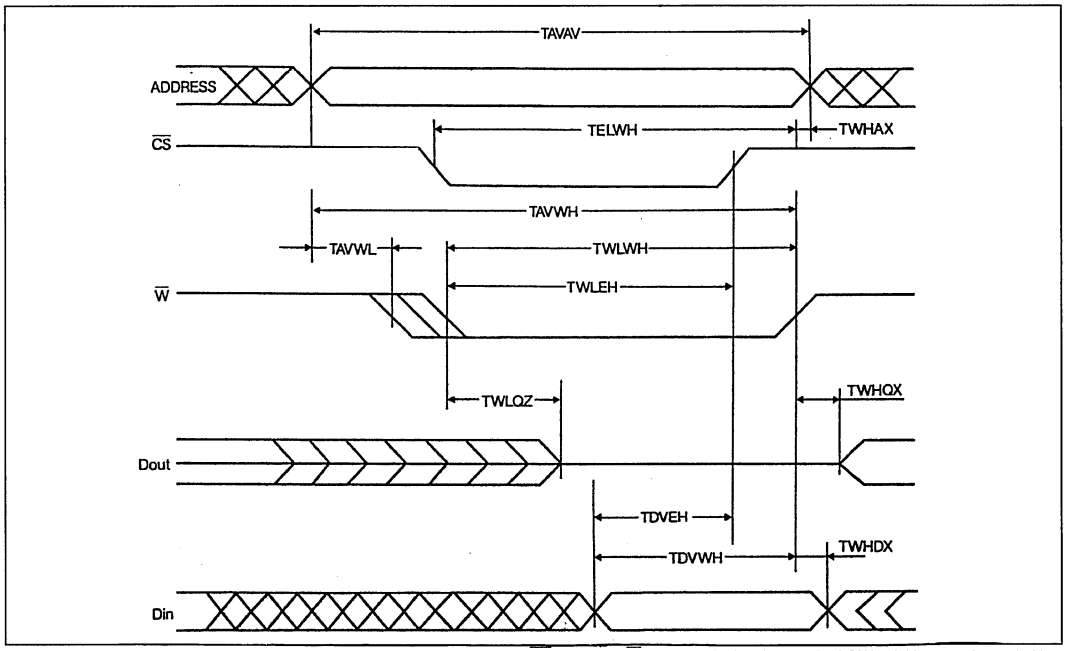
SYMBOL	PARAMETER	65688 B-5	65688 S-5	65688 -5	65688 C-5	UNIT	VALUE
TAVAV	Write cycle time	35	35	45	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	35	35	45	45	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	35	35	45	45	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	30	30	40	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

WRITE CYCLE : Industrial and Military Specification

SYMBOL	PARAMETER	65688 B-9/2	65688 S-9/2	65688 -9/2	65688 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE



Note : The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE : Commercial specification

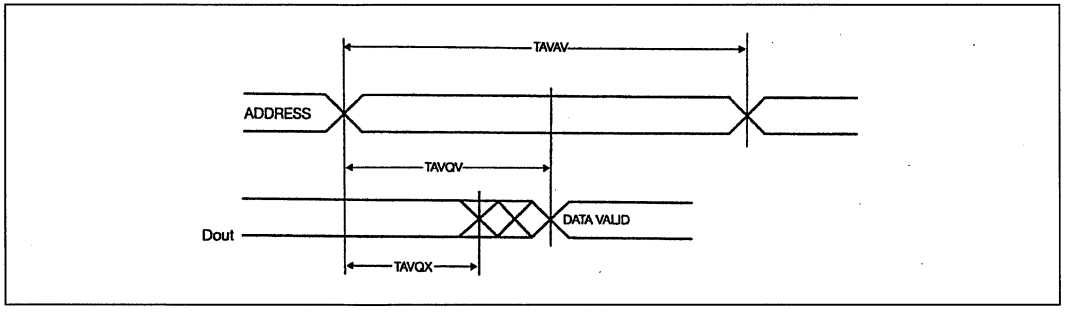
SYMBOL	PARAMETER	65688 B-5	65688 S-5	65688 -5	65688 C-5	UNIT	VALUE
TAVAV	Read cycle time	35	35	45	45	ns	min
TAVQV	Address access time	35	35	45	45	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	40	40	50	50	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQZ	$\overline{CS}$ high to high Z	35	35	45	45	ns	max

3

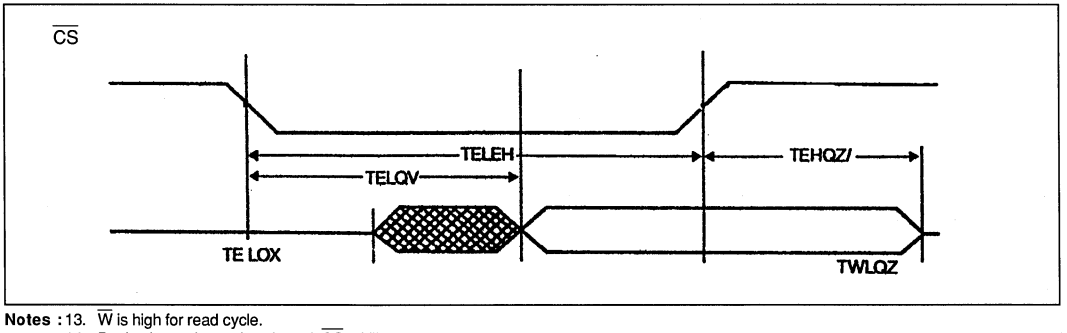
READ CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65688 B-9/2	65688 S-9/2	65688 -9/2	65688 C-9/2	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address Valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	50	50	65	65	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQX	$\overline{CS}$ high to high Z	45	45	55	55	ns	max

READ CYCLE nb 1 (notes 13, 14)



READ CYCLE nb 2 (notes 13, 15)



Notes : 13. $\overline{W}$ is high for read cycle.
14. Device is continuously selected, $\overline{CS}$ = VIL.
15. Address valid prior to or coincident with $\overline{CS}$ transitive low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65688	B	– 5
0 - Chip form 1 - Ceramic 22 pins 3 - Plastic 22 pins 300 mils 4 - LCC 22 pins T - SOIC 24 pins U* - SOJ 24 pins	16 k x 4 Ultimate CMOS static RAM	B - high speed/low current S : high speed/standard current Blank : standard speed/low current C : standard	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

* preliminary

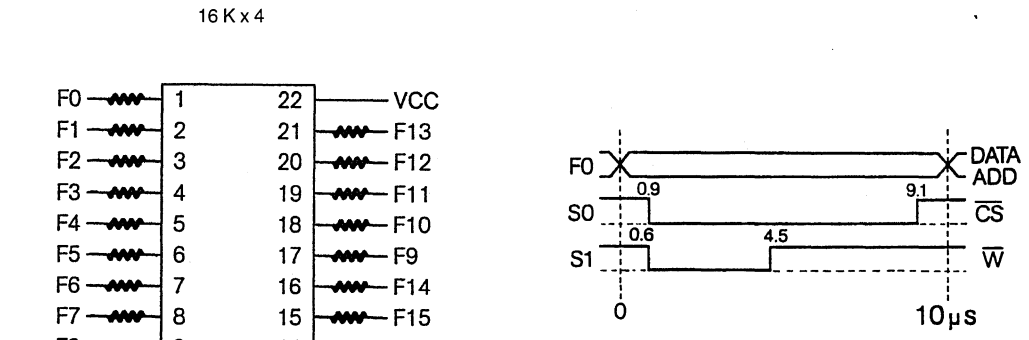
3

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins : X41
Ceramic DIL, 300 mils, 22 pins : TBD
SOIC DIL, 300 mils, 24 pins : N02
LCC rectangular, 22 pins : L16.

BURN-IN SCHEMATICS



VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %
Fn = 1/2 Fn-1

S0 et S1 : programmable signals for write / read cycles

DATA SHEET

HM 65664

8 K x 8
ULTIMATE CMOS SRAM

FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 45/55 ns (max)
  COMMERCIAL : 35/45 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 175.0 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

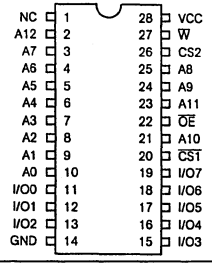
DESCRIPTION

The HM 65664 is a very low power CMOS static RAM organized as 8192 x 8 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.
With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics or the portable instruments PC's.
Utilising an array of six transistors (6T) memory cells, the HM 65664 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The HM 65664 is processed following the test methods of MIL STD 883C.

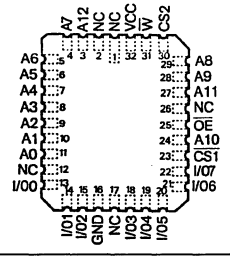
PACKAGES

Plastic 300 & 600 mils, 28 pins, DIL. SOIC&SOJ 300 mils, 28 pins, DIL.
Ceramic 300 & 600 mils, 28 pins, DIL. LCC, 32 pins.

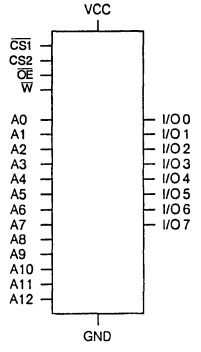
Pinout DIL 28 pins (top view)



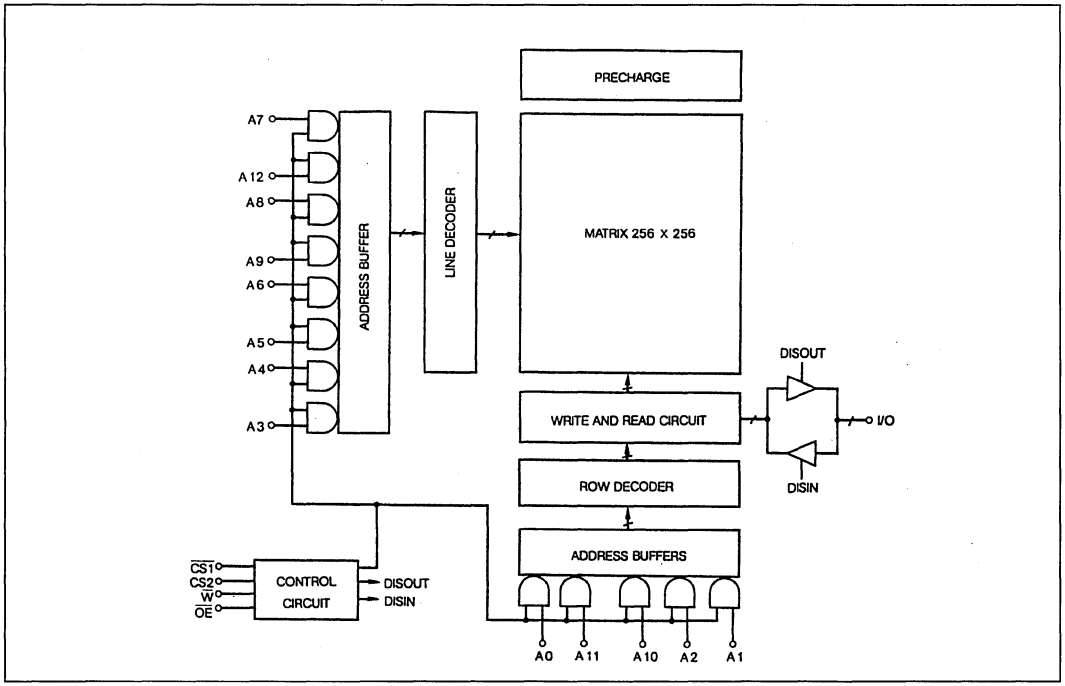
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A12	: Address inputs	$\overline{CS1}$	: Chip-select 1
I/O0-I/O7	: Input/Output	CS2	: Chip-select 2
Vcc	: Power	$\overline{OE}$	: Output Enable
Gnd	: Ground	$\overline{W}$	: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3 V	V

Note : 1. VIL min = - 0.3 V or - 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	– 1.0	–	10.0	µA
IOZ (3)	Output leakage current	– 1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL	PARAMETER	65664 B-5	65664 S-5	65664 -5	65664 C-5	UNIT	VALUE
ICCSB (5)	Standby supply current	10	15	10	15	mA	max
ICCSB1 (6)	Standby supply current	1.0	100.0	1.0	100.0	µA	max
ICC (7)	Operating supply current	10	15	10	15	mA	max
ICCOP (8)	Operating supply current	50	75	50	75	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL	PARAMETER	65664 B–9	65664 S-9	65664 -9	65664 C-9	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC (7)	Operating supply current	15	20	15	20	mA	max
ICCOP (8)	Operating supply current	75	100	75	100	mA	max

Consumption for Military specification (– 2) :

SYMBOL	PARAMETER	65664 B-2	65664 S-2	65664 -2	65664 C-2	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC (7)	Operating supply current	15	20	15	20	mA	max
ICCOP (8)	Operating supply current	75	100	75	100	mA	max

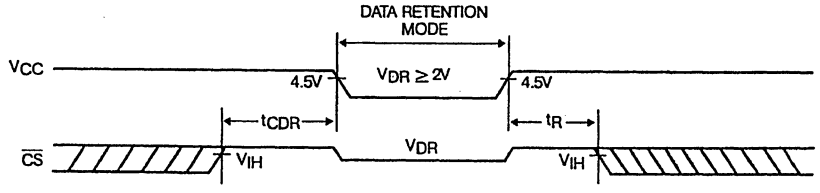
Notes : 5. $\overline{CS1} \geq$ VIH, CS2 $\leq$ VIL.
6. $\overline{CS1} \geq$ Vcc - 0.3V, CS2 $\leq$ 0.3 V, Iout = 0 mA.
7. $\overline{CS1} \geq$ VIL, CS2 $\leq$ VIH, Iout = 0 mA, Vin = Gna/Vcc.
8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begin operation > 45 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	@ 2.0 V : HM-65664(B)-5	–	0.1	1.0	µA
	HM-65664(B)-9	–	0.1	3.0	µA
	HM-65664(B)-2	–	0.1	20.0	µA
	HM-65664S/C-5	–	0.1	30.0	µA
	HM-65664S/C-9	–	0.1	30.0	µA
	HM-65664S/C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-65664(B)-5	–	0.3	1.0	µA
	HM-65664(B)-9	–	0.3	3.0	µA
	HM-65664(B)-2	–	0.3	30.0	µA
	HM-65664S/C-5	–	0.3	50.0	µA
	HM-65664S/C-9	–	0.3	50.0	µA
	HM-65664S/C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 30 pF

WRITE CYCLE : Commercial specification

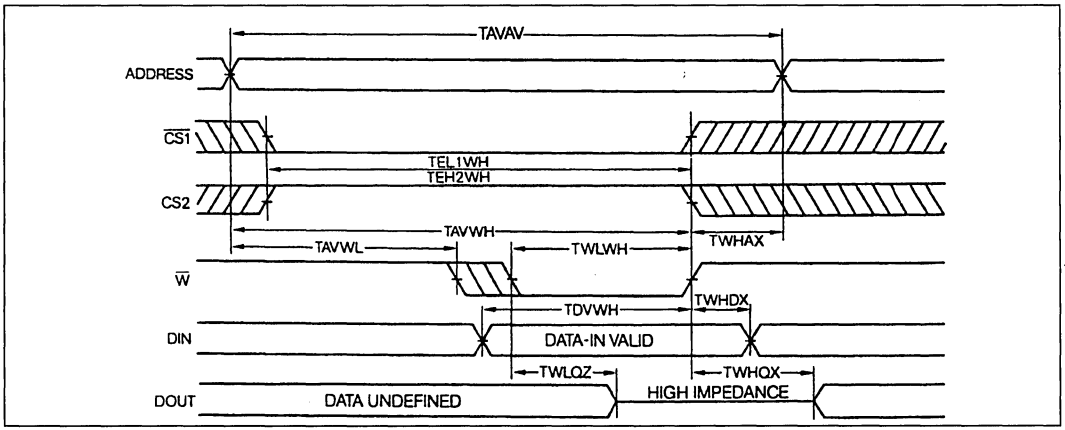
SYMBOL	PARAMETER	65664 B-5	65664 S-5	65664 -5	65664 C-5	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	45	45	55	55	ns	min
TEH2WH	CS2 low to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

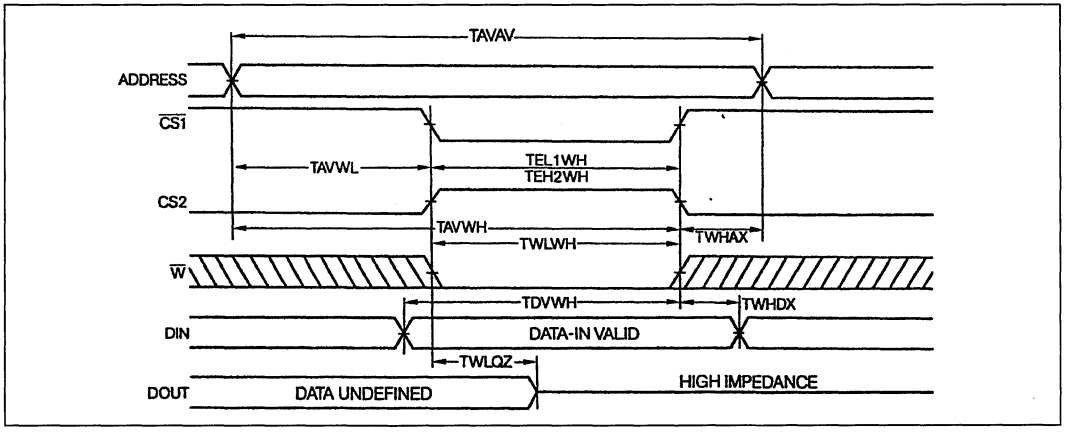
SYMBOL	PARAMETER	65664 B-9/2	65664 S-9/2	65664 -9/2	65664 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	45	45	55	55	ns	min
TEH2WH	CS2 low to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 13)



WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

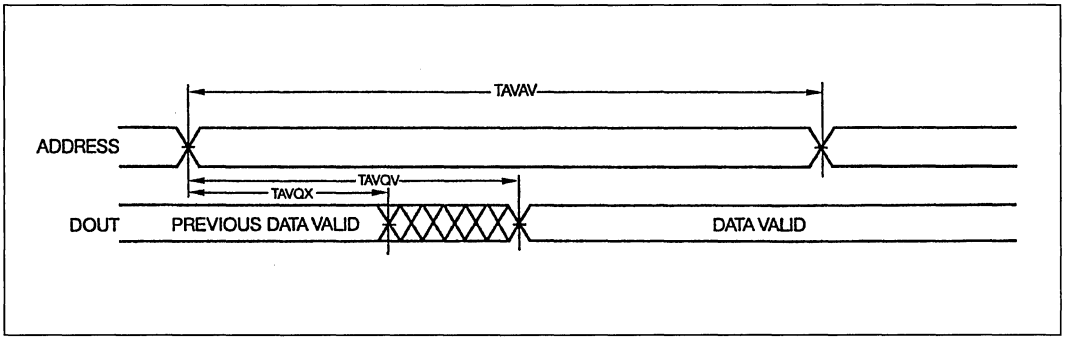
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65664 B-5	65664 S-5	65664 -5	65664 C-5	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	50	50	65	65	ns	max
TEH2QV	Chip-select 2 access time	50	50	65	65	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	max
TEH2QX	CS2 to low Z	5	5	5	5	ns	max
TEH1QZ	$\overline{CS1}$ high to high Z	45	45	55	55	ns	max
TEL2QZ	CS2 low to high Z	45	45	55	55	ns	max
TGLQV	Output Enable access time	15	15	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	10	20	20	ns	max

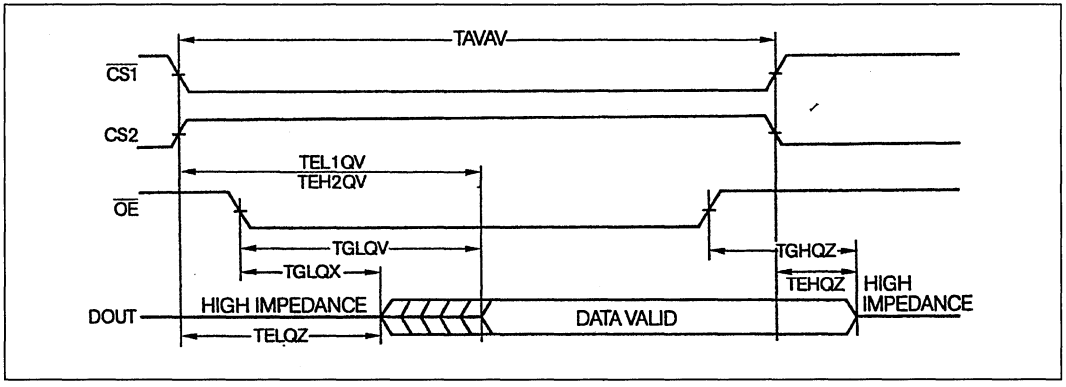
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65664 B-9/2	65664 S-9/2	65664 -9/2	65664 C–9/2	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address saccess time	45	45	55	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	50	50	65	65	ns	max
THL2QV	Chip-select 2 access time	50	50	65	65	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	max
TEH2QX	CS2 high to low Z	5	5	5	5	ns	max
TEH1QZ	$\overline{CS1}$ high to high Z	45	45	55	55	ns	max
TEL2QZ	CS2 low to high Z	45	45	55	55	ns	max
TGLQV	Output Enable access time	15	15	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	10	20	20	ns	max

READ CYCLE nb 1 (notes 16, 17)



READ CYCLE nb 2 (notes 16, 18)



Notes : 16. $\overline{W}$ is high for read cycle
17. Device is continuously selected, $\overline{CS1}$ & $\overline{OE}$ = VIL and CS2 = VIH
18. Address valid prior to or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65664	B	– 5
0 - Chip form 1 - Ceramic 28 pins 300 mils 1E - Ceramic 28 pins 600 mils 3 - Plastic 28 pins 300 mils 3E - Plastic 28 pins 600 mils 4 - LCC 32 pins T - SOIC 28 pins U* - SOJ 28 pins	8 k x 8 Ultimate CMOS static RAM	B = high speed/low current S = high speed/standard current Blank : standard speed/low current C : standard	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

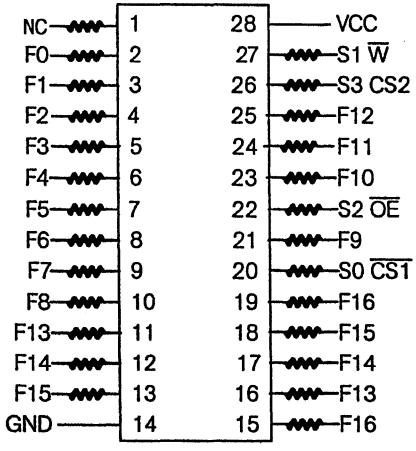
* preliminary

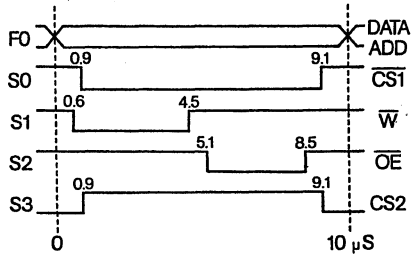
PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins : X49
Plastic DIL, 600 mils, 28 pins : X32
Ceramic DIL, 600 mils, 28 pins : C32
SOIC DIL, 300 mils, 28 pins : TBD
LCC rectangular, 32 pins : L19.

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
Fo = 50 KHz ± 20 %

Fn = 1/2 F n-1
S0 to S3 : programmable signals for write / read cycles
NC = Not connected

4

HIGH SPEED CMOS SRAM

MHS

DATA SHEET

HM 65767

16 K x 1
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25*/35/45/55 ns (max)
  COMMERCIAL : 15*/20*/25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 275 mW (typ)
  STANDBY : 55 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

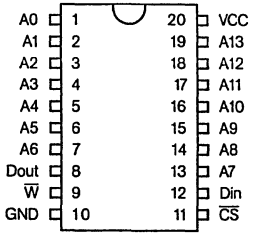
DESCRIPTION

The HM 65767 is a high speed CMOS static RAM organized as 16384x1 bit. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65767 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 70 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.
All inputs and outputs of the HM 65767 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65767 is processed following the test methods of MIL STD 883C.

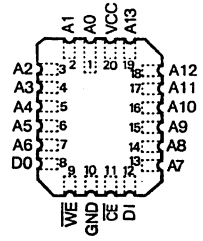
PACKAGES

Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
Tape and Reel Service.
SOIC 300 mils, 20 pins, DIL.
LCC 20 pins.

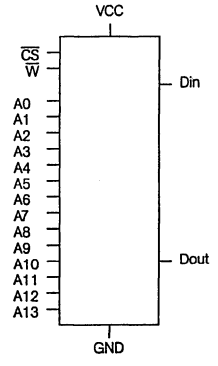
Pinout DIL 20 pins (top view)



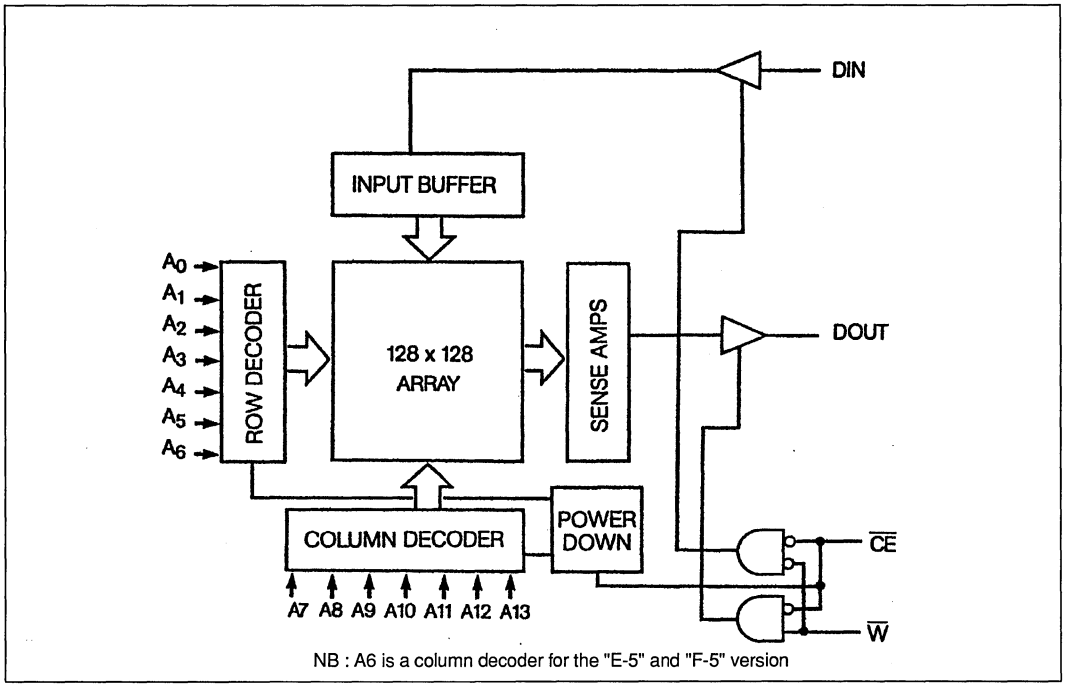
Pinout LCC 20 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



NB : A6 is a column decoder for the "E-5" and "F-5" version

PIN NAMES

A0-A13	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low - H = high - X = H or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	5.5	V

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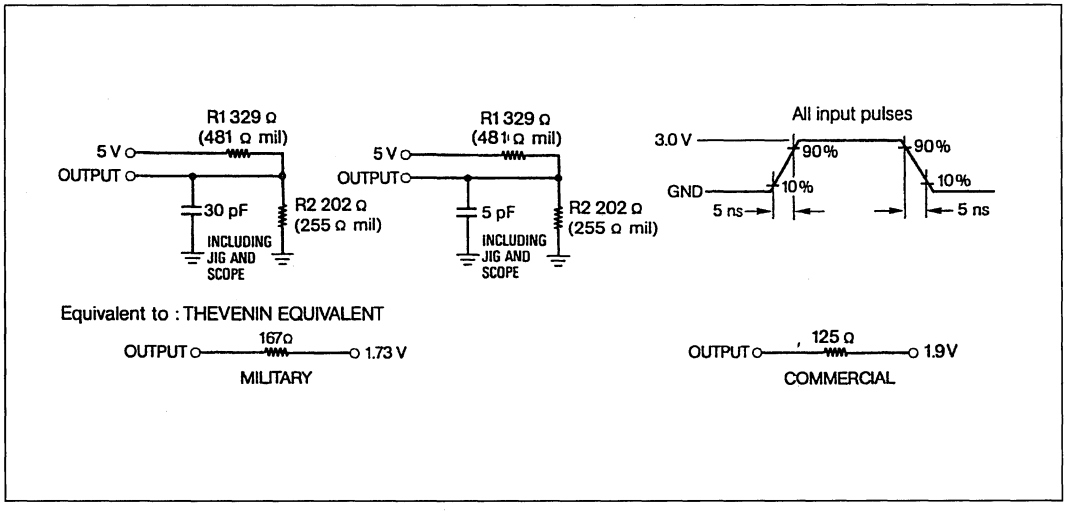
CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output capacitance	–	–	7	pF
C CS	(1)	CS capacitance	–	–	5	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 50.0	–	50.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
4. Vcc min, IOL = 12.0 mA (commercial) 8.0 mA (military).
5. Vcc min, IOH = – 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65767A E-5*	65767A F-5*	65767 H-5	65767 K-5	65767 M-5	65767 N-5	UNIT	VALUE
ICCSB (6)	Standby supply current	30	30	20	20	20	30	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	70	90	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65767A H-2*	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
ICCSB (6)	Standby supply current	30	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	80	70	70	70	mA	max

Notes : 6. $\overline{CS} \leq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary specification.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH : + 30 pF

WRITE CYCLE : Commercial specification

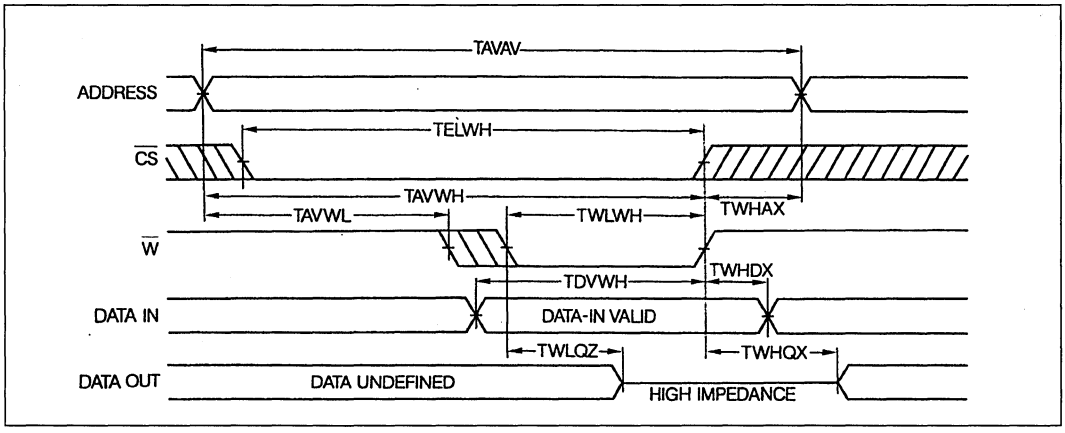
SYMBOL	PARAMETER	65767A E-5*	65767A F-5*	65767 H-5	65767 K-5	65767 M/N-5	UNIT	VALUE
TAVAV	Write Cycle time	15	20	25	30	40	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	25	30	40	ns	min
TDVWH	Data set-up time	10	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	25	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	10	25	30	20	ns	max
TWLWH	Write pulse width	15	15	15	20	20	ns	min
TWHAX	Address hold to end of write	0	0	0	0	0	ns	min
TWDHX	Data hold time	0	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	0	0	0	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65767A H-2*	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
TAVAV	Write cycle time	25	30	40	40	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	25	30	40	40	ns	min
TDVWH	Data set-up time	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	40	40	ns	min
TWLQZ (8)	Write low to high Z	15	20	20	20	ns	max
TWLWH	Write pulse width	15	20	20	20	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	0	0	0	ns	min

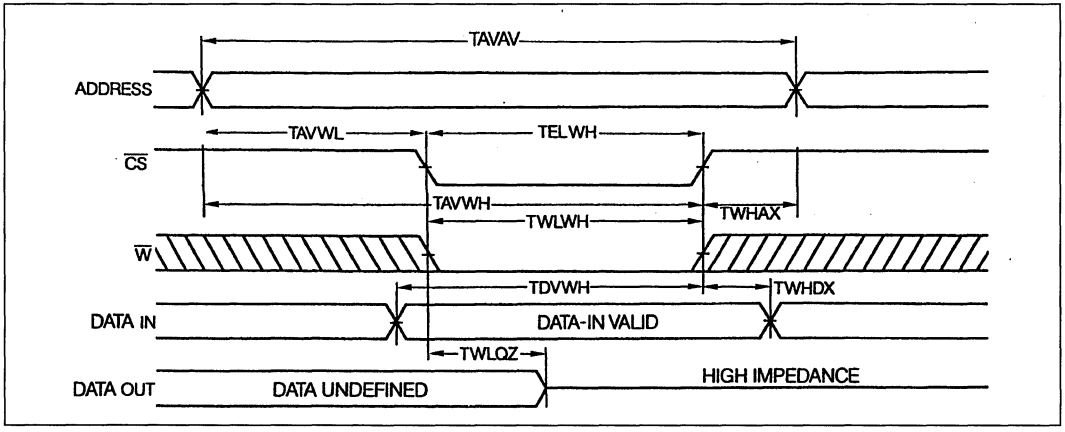
Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
* Preliminary specification.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



4

WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65767A E-5*	65767A F-5*	65767 H-5	65767 K-5	65767 M-5	65767 N-5	UNIT	VALUE
TAVAV	READ cycle time	15	20	25	30	40	50	ns	min
TAVQV	Address access time	15	20	25	30	40	50	ns	max
TAVQX	Address valid to low Z	2	2	3	3	3	3	ns	min
TELQV	Chip-select access time	15	20	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	10	20	20	25	30	30	ns	max

* Preliminary specification.

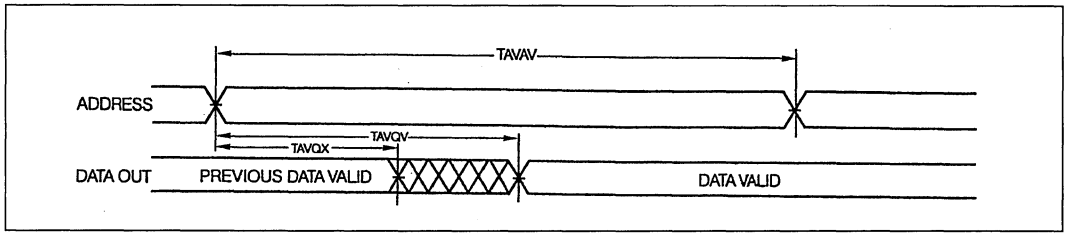
READ CYCLE : Military specification

SYMBOL	PARAMETER	65767A H-2*	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	40	50	ns	min
TAVQV	Address access time	25	35	40	50	ns	max
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	30	ns	max

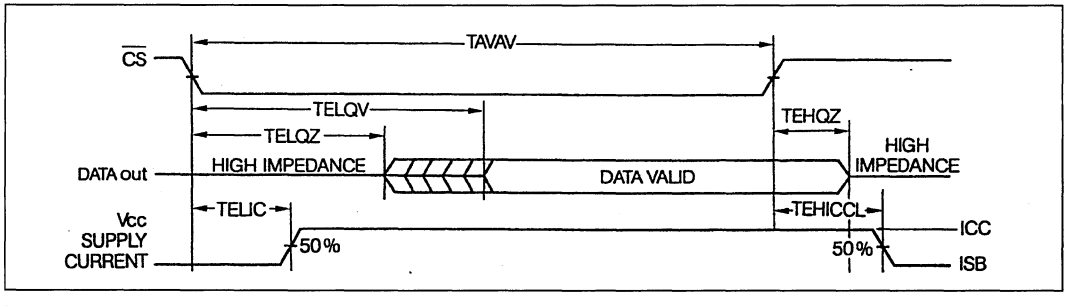
* Preliminary specification.

4

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65767 (A)	H	– 5 : R

- Package: 0 - Chip form; 1 - Ceramic 20 pins; 3 - Plastic 20 pins 300 mils; 4 - LCC 20 pins; T - SOIC 20 pins
- Device type: 16 k x 1 high speed power static RAM
- Grade: E = 15 ns; F = 20 ns; H = 25 ns; K = 35 ns; M = 45 ns; N = 55 ns
- Level: – 5 : Commercial; – 5+ : Commercial with B.I.; – 2 : Military; – 8 : Military with B.I. (B.I. = Burn-In)
- Tape and Reel Service

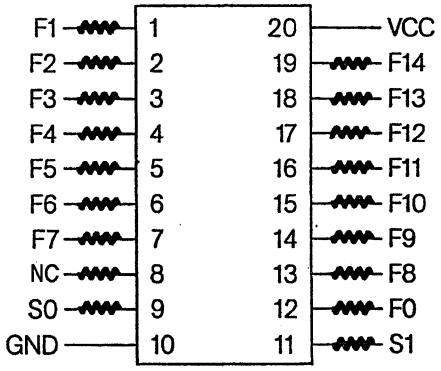
4

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 20 pins : 034
SOIC DIL, 300 mils, 20 pins : N01
Ceramic, 300 mils, 20 pins : C23
LCC rectangular, 20 pins : L20.

BURN-IN SCHEMATICS



R = 220 Ω per row
FO = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

Vcc = 5.5 V

NC = Not connected

DATA SHEET

HM 65768

4 K x 4
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25*/35/45/55 ns (max)
  COMMERCIAL : 15*/20*/25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 200 mW (typ)
  STANDBY : 35 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

DESCRIPTION

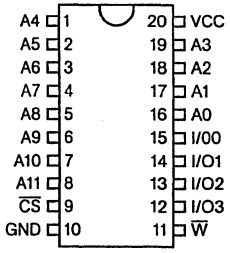
The HM 65768 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65768 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 77 % when the circuit is deselected.

Each memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.
All inputs and outputs of the HM 65768 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65768 is processed following the test methods of MIL STD 883C.

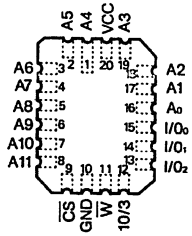
PACKAGES

Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
Tape and Reel Service
SOIC 300 mils, 20 pins, DIL.
LCC 20 pins.

Pinout DIL 20 pins (top view)

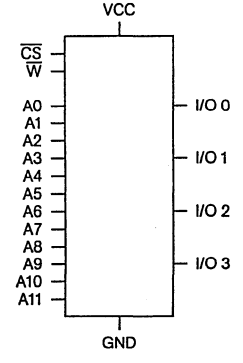


Pinout LCC 20 pins (top view)

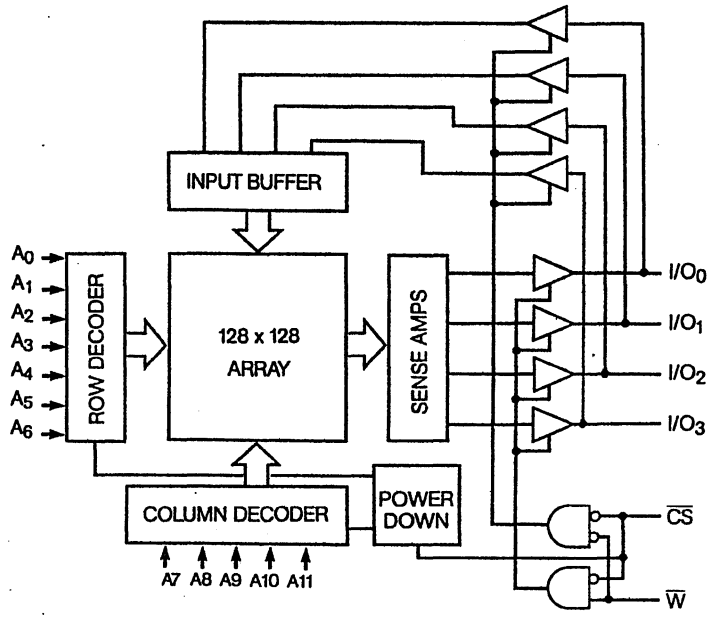


* preliminary specification

LOGIC SYMBOL



BLOCK DIAGRAM



A6 is a column decoder for the "E - 5" and "F - 5" versions

PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I/O0-I/O3	: Input/Output	$\overline{W}$	: Write enable
Vcc	: Power		
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	5.5	V

4

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V.

AC TEST LOADS WAVEFORMS

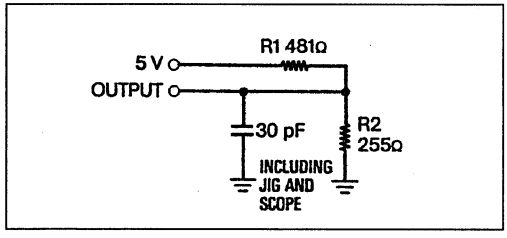


Fig. 1a.

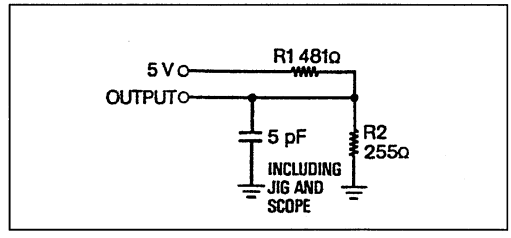
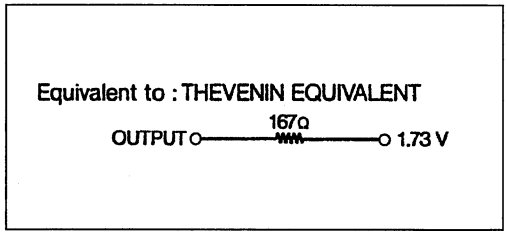


Fig. 1b.



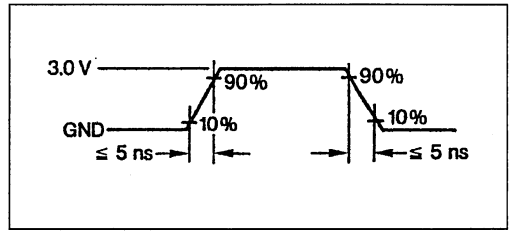


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 50.0	–	50.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA .
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65768A E-5*	65768A F-5*	65768 H-5	65768 K-5	65768 M-5	65768 N-5	UNIT	VALUE
ICCSB (6)	Standby supply current	30	30	15	15	15	30	mA	max
ICCSB1(7)	Standby supply current	30	30	11	11	11	30	mA	max
ICCOP (8)	Dynamic operating current	70	70	70	70	70	90	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65768A H-2*	65768 K-2	65768 M-2	65768 N-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCSB1(7)	Standby supply current	30	20	20	20	mA	max
ICCOP (8)	Dynamic operating current	120	90	90	90	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. CS ≥ Vcc - 300 mV.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary specification.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) : +30 pF

WRITE CYCLE : Commercial specification

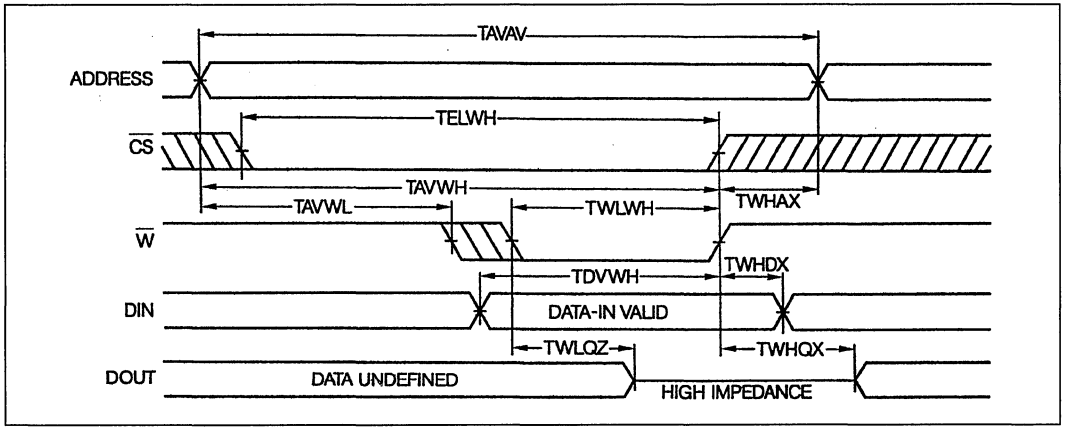
SYMBOL	PARAMETER	65768A E-5*	65768A F-5*	65768 H-5	65768 K-5	65768 M/N-5	UNIT	VALUE
TAVAV	Write Cycle time	15	20	25	35	40	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	15	20	30	35	ns	min
TDVWH	Data set-up time	10	10	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	15	15	25	35	35	ns	min
TWLQZ (9)	Write low to high Z	10	10	10	15	20	ns	max
TWLWH	Write pulse width	15	15	20	30	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	3	3	ns	min
TWHQX (9)	Write high to low Z	3	3	6	6	6	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65768A H-2*	65768 K-2	65768 M-2	65768 N-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	40	40	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	35	35	ns	min
TDVWH	Data set-up time	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	35	35	35	ns	min
TWLQZ (9)	Write low to high Z	10	15	20	20	ns	max
TWLWH	Write pulse width	20	30	35	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	3	3	ns	min
TWHQX (9)	Write high to low Z	3	6	6	6	ns	min

Note : 9. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
* Preliminary specification.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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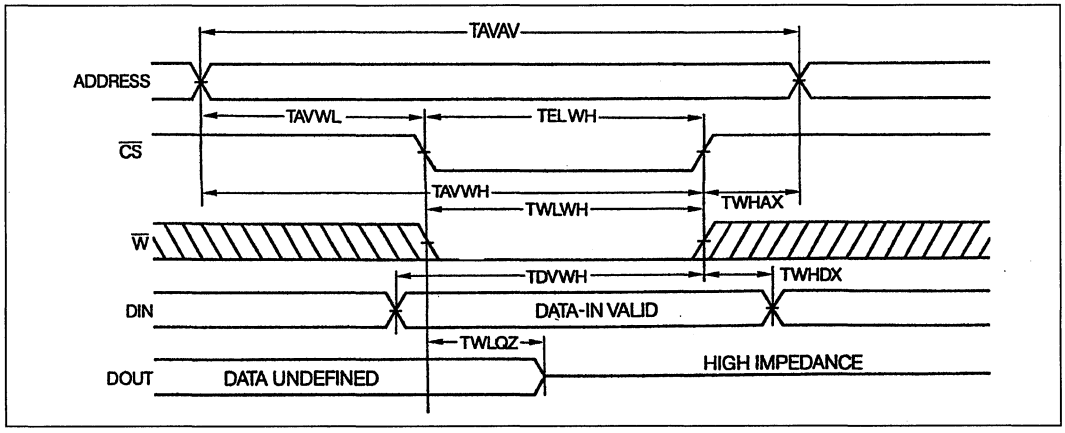
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65768A E-5*	65768A F-5*	65768 H-5	65768 K-5	65768 M-5	65768 N-5	UNIT	VALUE
TAVAV	READ cycle time	15	20	25	35	45	55	ns	min
TAVQV	Address access time	15	20	25	35	45	55	ns	max
TAVQX	Address valid to low Z	2	2	3	3	3	3	ns	min
TELQV	Chip-select access time	15	20	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	15	25	25	25	30	30	ns	max

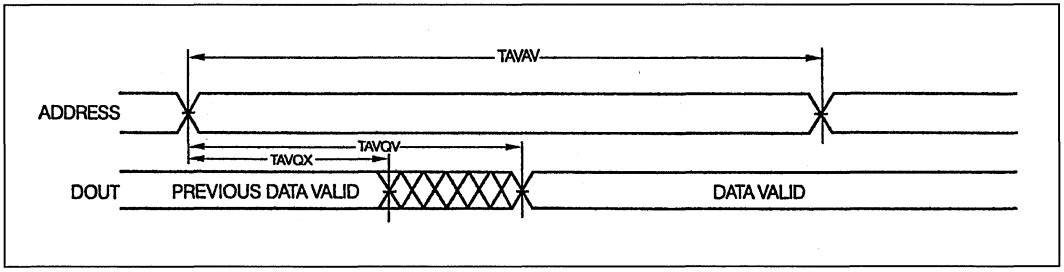
* Preliminary specification.

READ CYCLE : Military specification

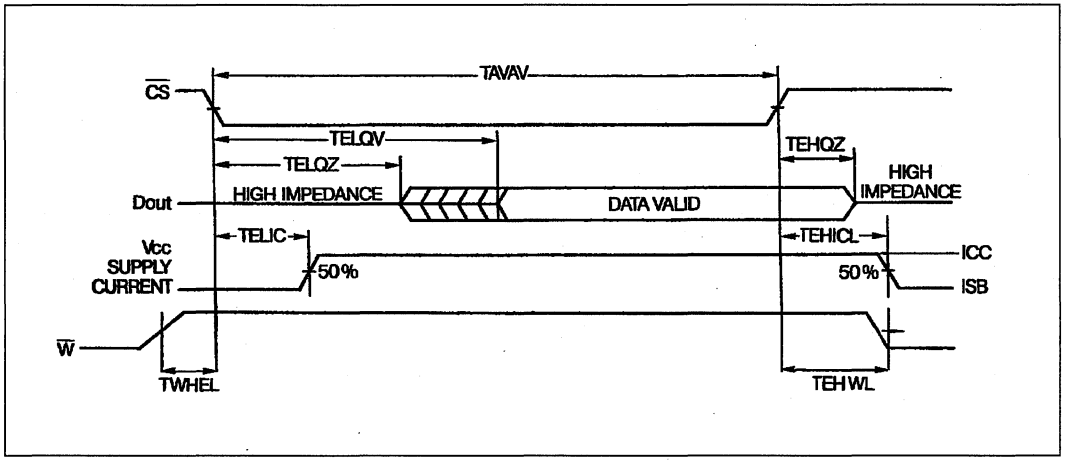
SYMBOL	PARAMETER	65768A H-2*	65768 K-2	65768 M-2	65768 N-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	5	25	30	30	ns	max

* Preliminary specification.

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package
HM1
- 0 - Chip form
- 1 - Ceramic 20 pins
- 3 - Plastic 20 pins
- 4 - LCC 20 pins
- T - SOIC 20 pins

Device type
65768 (A)
- 4 k x 4 high speed static RAM

Grade
H
- E = 15 ns
- F = 20 ns
- H = 25 ns
- K = 35 ns
- M = 45 ns
- N = 55 ns

Level
– 5 : R
- – 5 : Commercial
- – 5+ : Commercial with B.I.
- – 2 : Military
- – 8 : Military with B.I.

(B.I. = Burn-In)

R : Tape and Reel Service

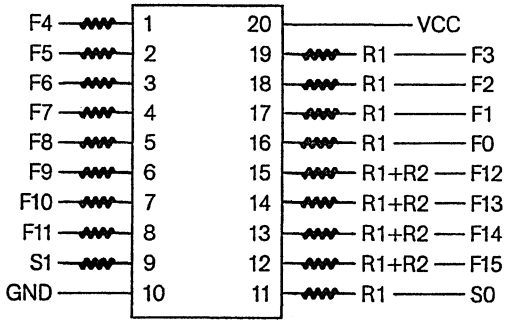
4

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 20 pins : 034
SOIC DIL, 300 mils, 20 pins : N01
Ceramic, 300 mils, 20 pins : C23
LCC rectangular, 20 pins : L20.

BURN-IN SCHEMATICS



R1 = 300 Ω per row
R2 = 2 KΩ per driver
FO = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

DATA SHEET

HM 65770

4 K x 4
HIGH SPEED CMOS SRAM
WITH OUTPUT ENABLE

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25/35/45 ns (max)
  COMMERCIAL : 20/25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (max)
  STANDBY : 27.5 mW (max)
- **WIDE TEMPERATURE RANGE :**
  - 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **OUTPUT ENABLE**

4

DESCRIPTION

The HM 65770 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65770 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 90 % when the circuit is deselected.

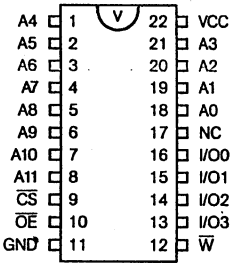
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65770 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65770 is processed following the test methods of MIL STD 883C.

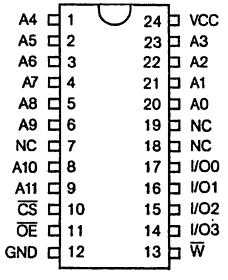
PACKAGES

Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.

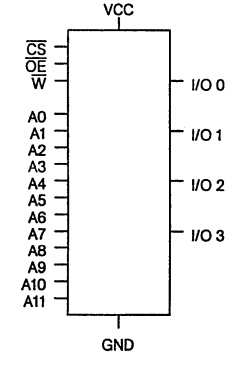
SO 300 mils, 24 pins, DIL.

Pinout DIL 22/24 pins (top view)

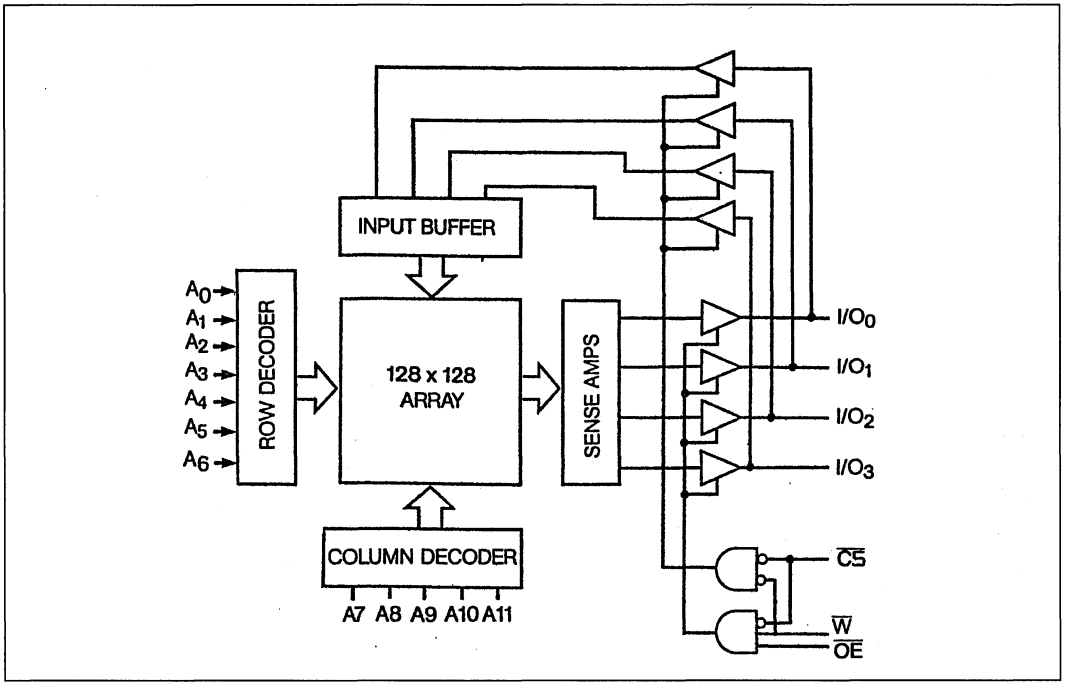




LOGIC SYMBOL



BLOCK DIAGRAM



4

PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I/O0–I/O3	: Input/Output	$\overline{W}$	: Write enable
Vcc	: Power	$\overline{OE}$	: Output enable
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial (– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	VCC	V

4

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input capacitance	–	–	4	pF
Cout (1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V. These parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

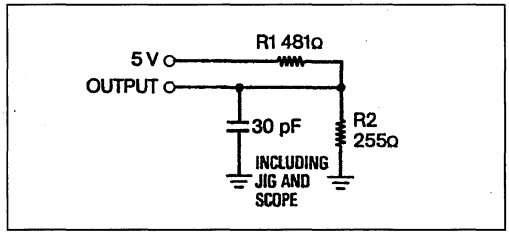


Fig. 1a.

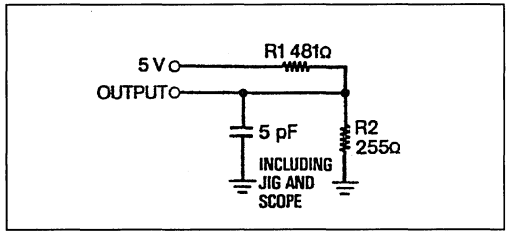
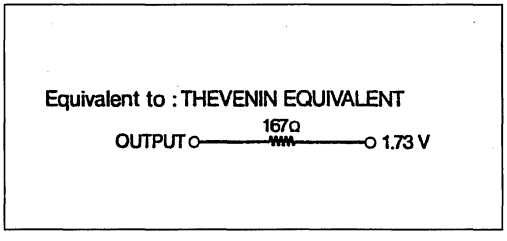


Fig. 1b.



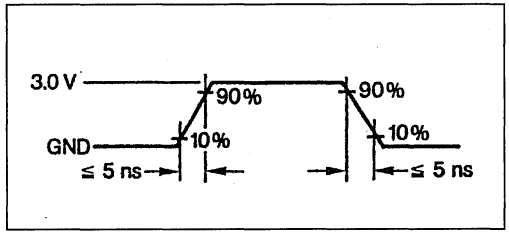


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 50.0	–	50.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA .
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	90	90	90	90	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65770 H-2	65772 K-2	65770 M-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	120	120	120	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

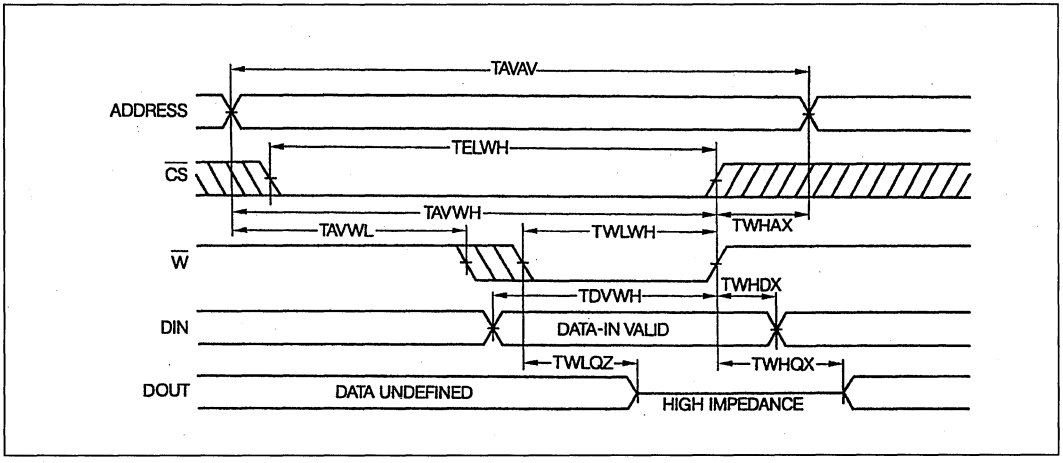
SYMBOL	PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	30	35	ns	min
TDVWH	Data set-up time	10	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	35	35	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	20	ns	max
TWLWH	Write pulse width	15	20	30	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	3	ns	min
TWHQX (8)	Write high to low Z	3	6	6	6	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65770 H-2	65770 K-2	65770 M-2	UNIT	VALUE
TAVAV	Write cycle time	25	35	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	35	ns	min
TDVWH	Data set-up time	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	35	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	20	30	35	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	3	ns	min
TWHQX (8)	Write high to low Z	6	6	6	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ Controlled (note 9)



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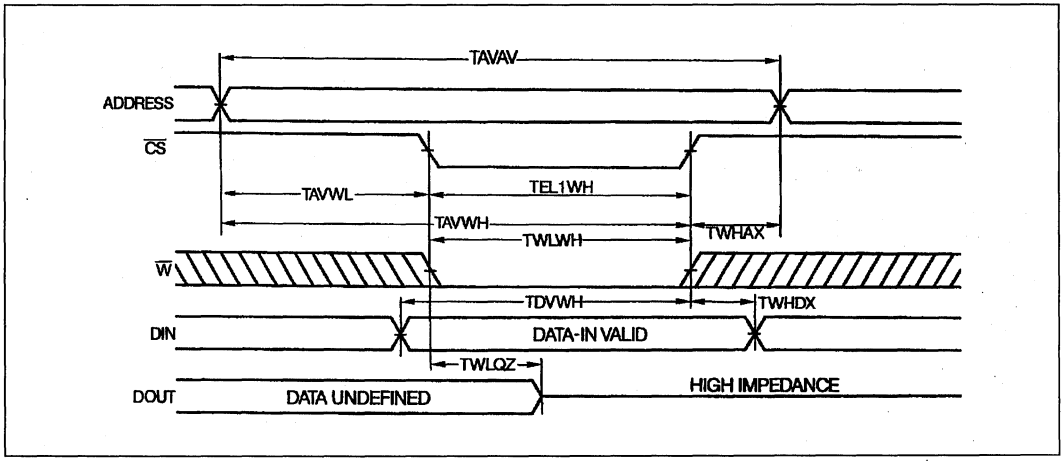
WRITE CYCLE 2 $\overline{CS}$ Controlled (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

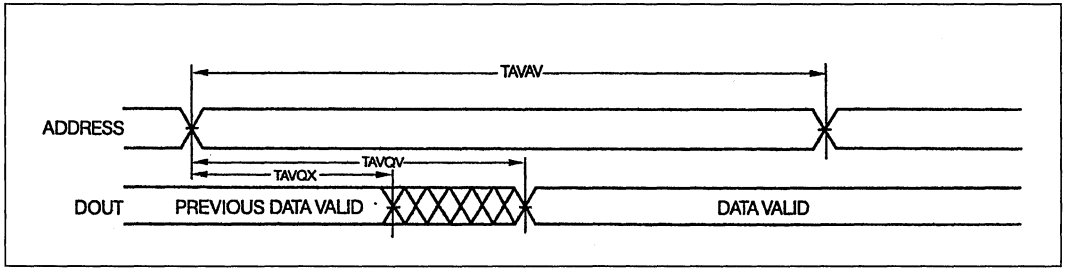
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	max
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	15	15	25	30	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	25	30	ns	max
TGLQV	Output Enable access time	12	15	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	2	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	12	15	15	15	ns	max

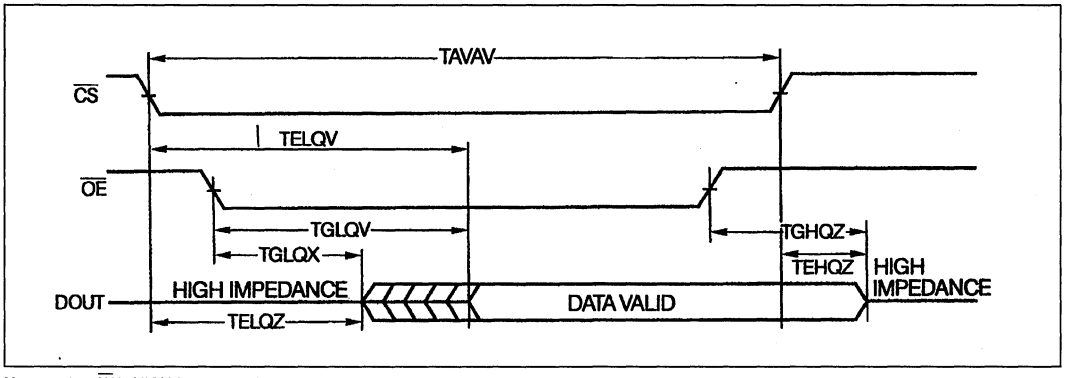
READ CYCLE : Military specification

SYMBOL	PARAMETER	65770 H-2	65770 K-2	65770 M-2	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	ns	max
TGLQV	Output Enable access time	15	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	20	ns	max

READ CYCLE nb 1 : (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL and $\overline{OE}$ = VIL.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65770	K	– 5
0 - Chip form 1 - Ceramic 22 pins 3 - Plastic 22 pins T - SO 24 pins	4 k x 4 high speed static RAM with Output Enable	F = 20 ns H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins : X41
Ceramic, 300 mils, 20 pins : C33
SOIC DIL 300 mils, 24 pins : TBD.

DATA SHEET

HM 65772

4 k x 4 HIGH SPEED CMOS SRAM SEPARATE I/O

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25/35/45 ns (max)
  COMMERCIAL : 20/25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (max)
  STANDBY : 27.5 mW (max)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUT/OUTPUT**

DESCRIPTION

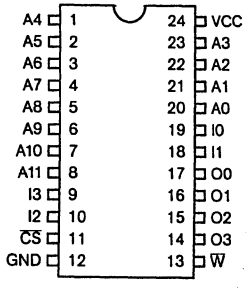
The HM 65772 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65772 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 10 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$), four separate input/output buffers and three state drivers.
All inputs and outputs of the HM 65772 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65772 is processed following the test methods of MIL STD 883C.

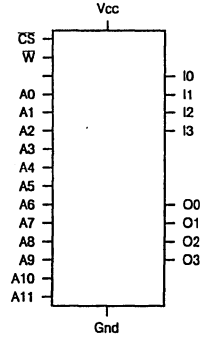
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
SO 300 mils, 24 pins, DIL.
L = low, H = high, X = H

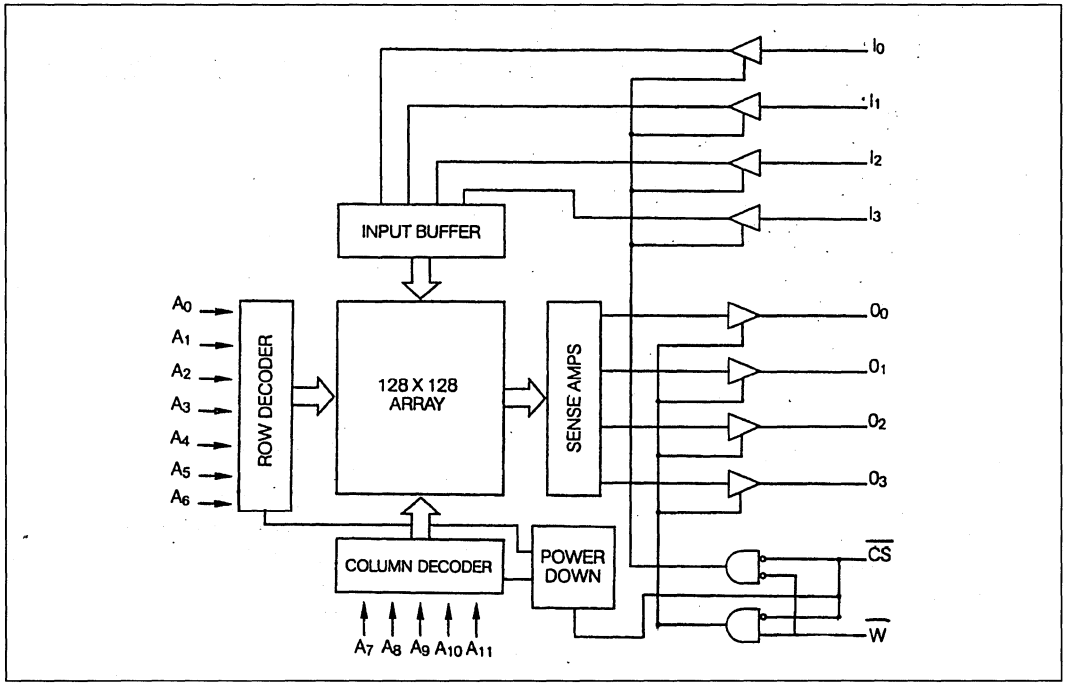
Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I0–I3	: Inputs	VCC	: Power
O0–O3	: Outputs	GND	: Ground
$\overline{W}$	: Write enable		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output Capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

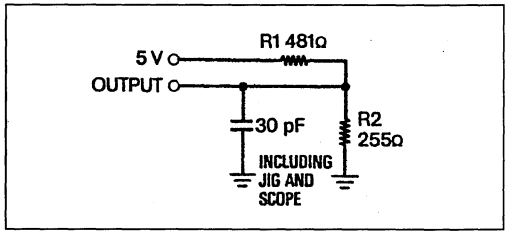


Fig. 1a.

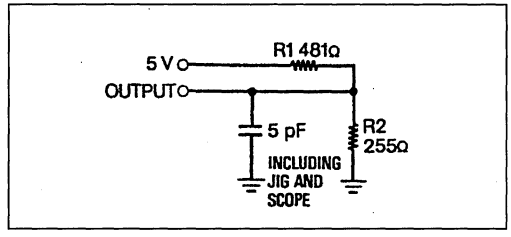
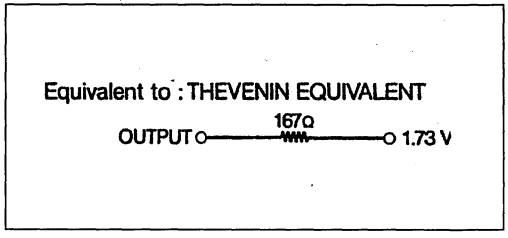


Fig. 1b.



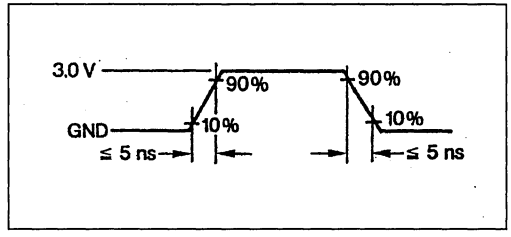


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 15.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output High voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Operating supply current	80	70	70	70	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	mA	max
ICCOP (7)	Operating supply current	90	90	90	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels :1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

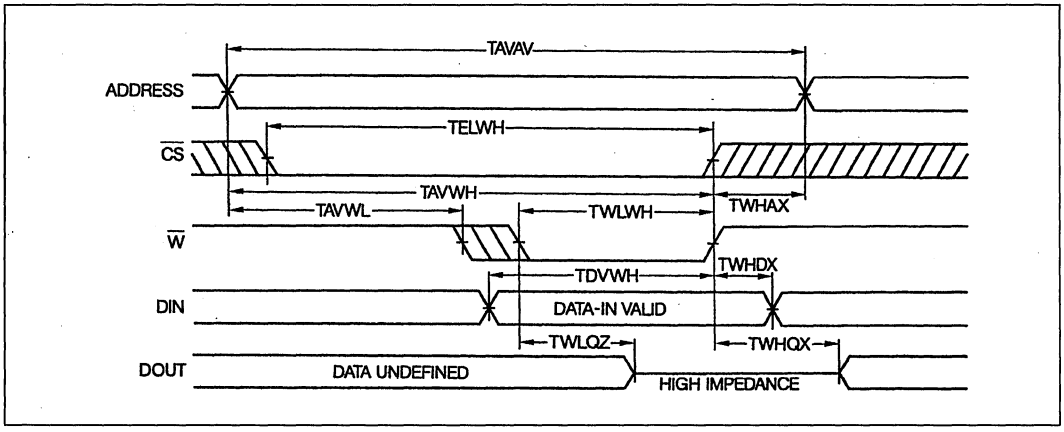
SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
TAVAV	Write Cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	30	40	ns	min
TDVWH	Data set-up time	10	15	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	20	ns	max
TWLWH	Write pulse width	15	20	30	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWDHX	Data hold time	0	0	0	3	ns	min
TWHQX (8)	Write high to low Z	3	6	6	6	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	25	30	40	ns	min
TDVWH	Data set-up time	20	20	20	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	20	30	40	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWDHX	Data hold time	0	0	3	ns	min
TWHQX (8)	Write high to low Z	6	6	6	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 10)



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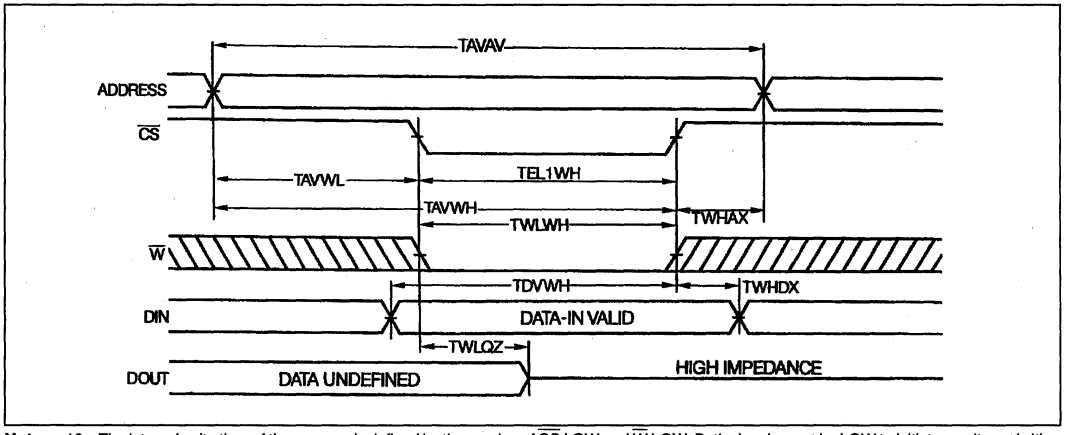
WRITE CYCLE 2 $\overline{CS}$ CONTROLLED (note 10)



Note : 10. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

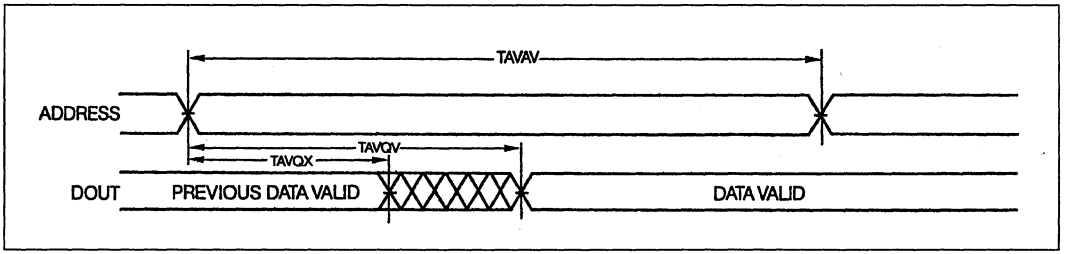
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
TAVAV	READ Cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	min
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	20	15	25	30	ns	min
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	25	30	ns	max

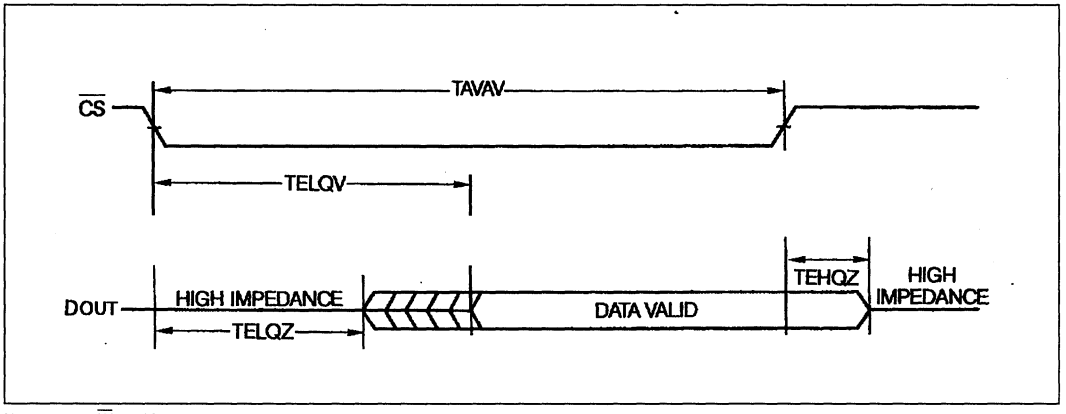
READ CYCLE : Military specification

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	min
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	ns	min
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	25	30	ns	max

READ CYCLE nb1 : (notes 11, 12)



READ CYCLE nb2 : (notes 11, 13)



Note : 11. $\overline{W}$ is HIGH for Read cycle.
Notes : 12. Device is continuously selected, $\overline{CS}$ = VIL.
13. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65772	K	– 5
0 - Chip form 1 - Ceramic 28 pins 3 - Plastic 28 pins T - SOIC 24 pins	4 k x 4 high speed static RAM with separate I/O	F = 20 ns H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins : 043
Ceramic DIL, 300 mils, 24 pins : C25
SOIC DIL, 300 mils, 24 pins : TBD.

DATA SHEET

HM 65728

2 k x 8
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 20*/25*/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 310 mW (typ)
  STANDBY : 55 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

DESCRIPTION

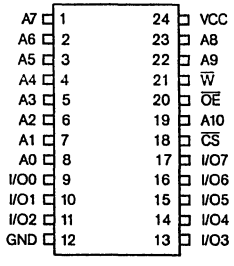
The HM 65728 is a high speed CMOSstatic RAM organized as 2048 x 8 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 20 ns are available with maximum power consumption of only 600 mW.
The HM 65728 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65728 are TTL compatible and operate from single 5V supply thus simplifying system design.
The HM 65728 is processed following the test methods of MIL STD 883C.

PACKAGES

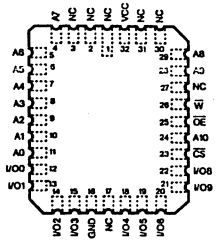
Plastic 300 & 600 mils, 24 pins, DIL
SO 300 mils, 24 pins, DIL
Tape and Reel Service

Ceramic 300 mils, 24 pins, DIL
LCC, 32 pins

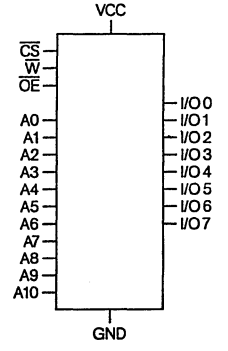
Pinout DIL 24 pins (top view)



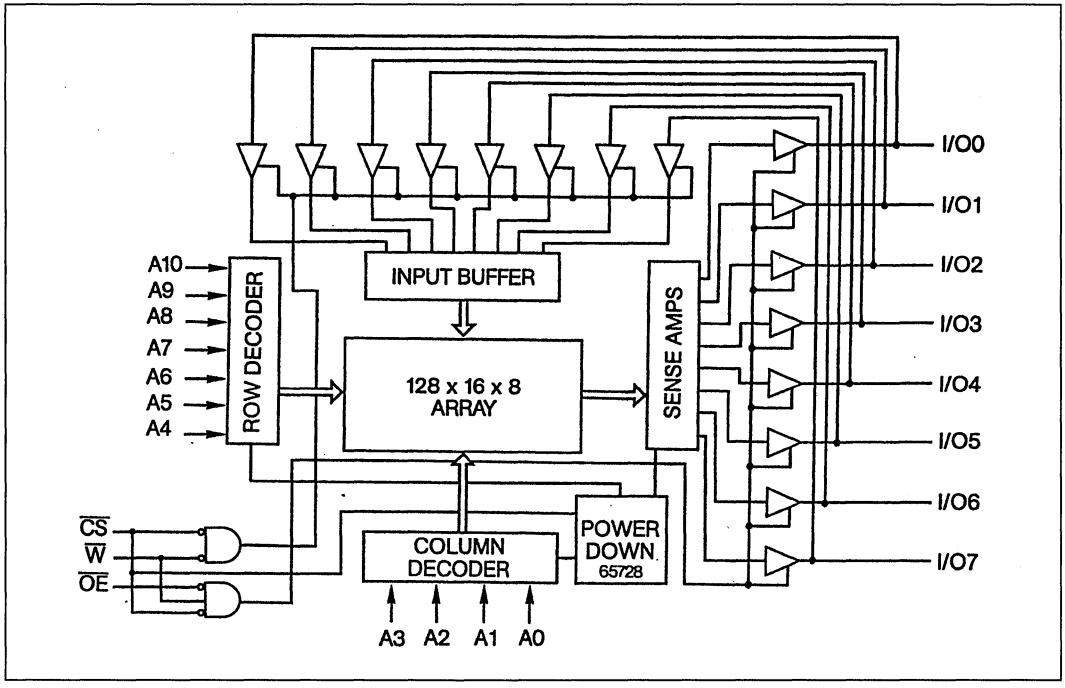
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A10	: Address inputs	$\overline{CS}$	: Chip Select
I/O0–I/O7	: Input/Output	$\overline{OE}$	: Output Enable
Vcc	: Power	$\overline{W}$	: Write enable
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial (– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	5.5	V

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CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input capacitance	–	–	5	pF
Cout (1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25C, f = 1MHz, Vcc = 5.0V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

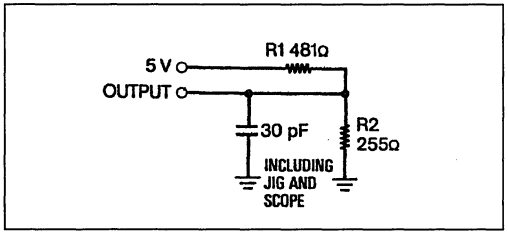


Fig. 1a.

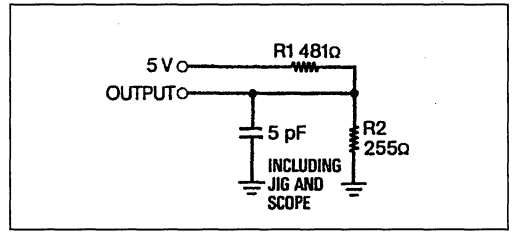
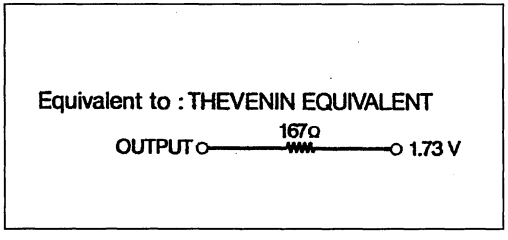


Fig. 1b.



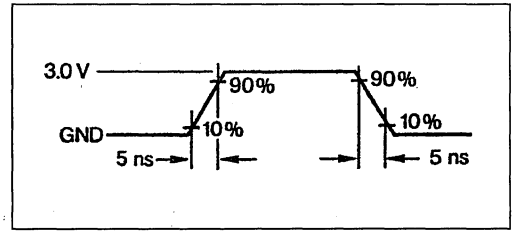


Figure 2 : All Input Pulses.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 40.0	–	40.0	µA
IOS (3)	Output short circuit current	–	–	– 300.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65728A F-5*	65728A H-5*	65728 K-5	65728 M-5	65728 N-5	UNIT	VALUE
ICCSB (6)	Standby supply current	40	20	20	20	30	mA	max
ICCOP (7)	Dynamic Operating current	100	100	100	100	100	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65728A H-2*	65728 K-2	65728 M-2	65728 N-2	UNIT	VALUE
ICCSB (6)	Standby supply current	40	30	30	30	mA	max
ICCOP (7)	Dynamic Operating current	120	120	120	120	mA	max

Notes : 6. $\overline{CS} \geq VIH$, a pull up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary specification.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) : + 30 pF

WRITE CYCLE : Commercial Specification

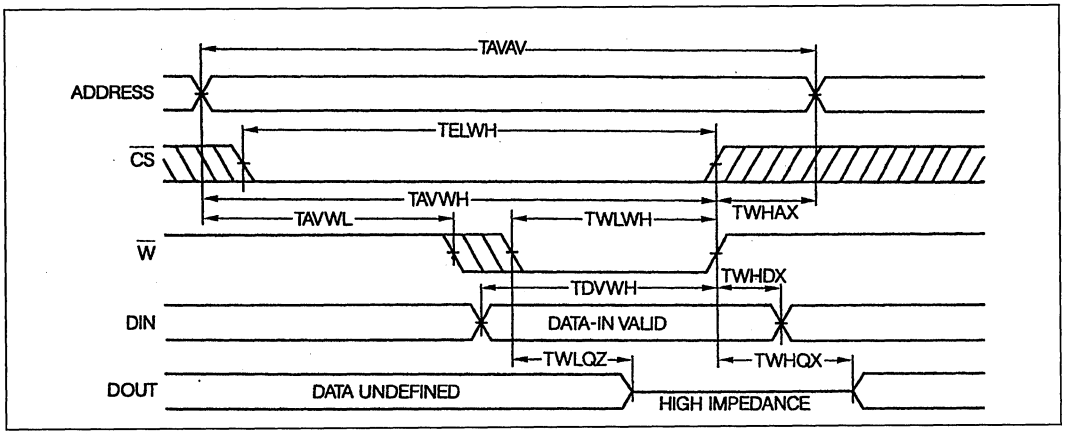
SYMBOL	PARAMETER	65728A F-5*	65728A H-5*	65728 K-5	65728 M-5	65728 N-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	20	30	40	50	ns	min
TDVWH	Data set-up time	15	15	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	15	20	ns	max
TWLWH	Write pulse width	15	20	20	20	30	ns	min
TWHAX	Address hold to end of write	0	2	5	5	5	ns	min
TWHDX	Data hold time	0	0	0	0	5	ns	min
TWHQX (8, 9)	Write high to low Z	3	3	0	0	0	ns	min

Notes : 8. The data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.
* Preliminary specification.

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65728A H-2*	65728 K-2	65728 M-2	65728 N-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	10	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	10	15	15	20	ns	max
TWLWH	Write pulse width	20	20	25	30	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	5	5	5	5	ns	min

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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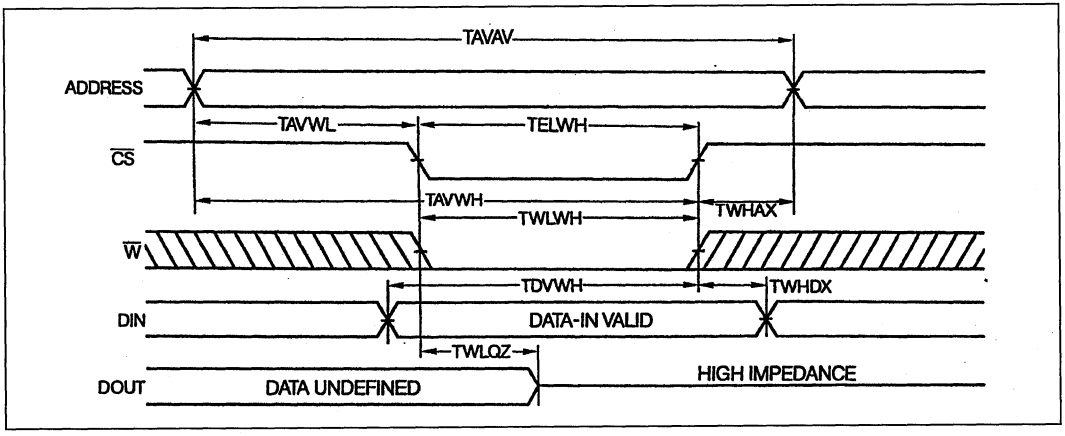
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE : Commercial specification

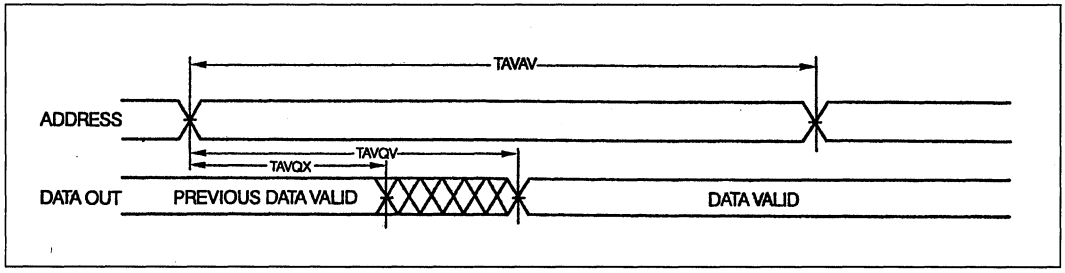
SYMBOL	PARAMETER	65728A F-5*	65728A H-5*	65728 K-5	65728 M-5	65728 N-5	UNIT	VALUE
TAVAV	Read cycle time	20	25	35	45	55	ns	min
TAVQV	Address access time	20	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	5	5	5	ns	min
TELQV	Chip-select access time	20	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	12	12	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	15	15	20	25	25	ns	max
TGLQV	Output enable access time	10	15	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	2	2	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	10	15	15	20	ns	max

* Preliminary specification

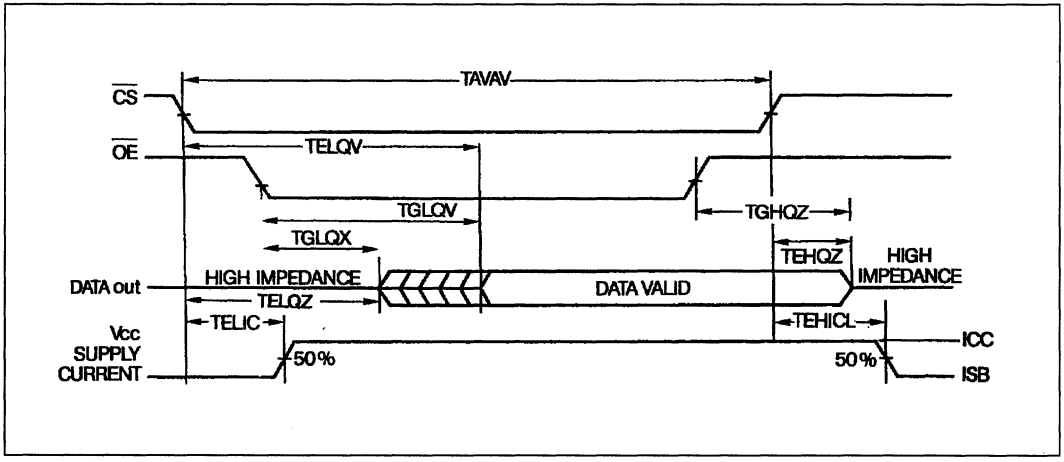
READ CYCLE : Military specification

SYMBOL	PARAMETER	65728A H-2*	65728 K-2	65728 M-2	65728 N-2	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	12	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	0	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	12	15	15	20	ns	max

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65728 (A)	H	– 5 : R

Package:
0 - Chip form
1 - Ceramic 24 pins
3 - Plastic 24 pins 300 mils
3E - Plastic 24 pins 600 mils
4 - LCC 32 pins
T - SOIC 24 pins

Device type:
2 k x 8 high speed static RAM

Grade:
F = 20 ns
H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

Level:
– 5 : Commercial
– 5+ : Commercial with B.I.
– 2 : Military
– 8 : Military with B.I.
(B.I. = Burn-In)

: R — Tape and Reel Service

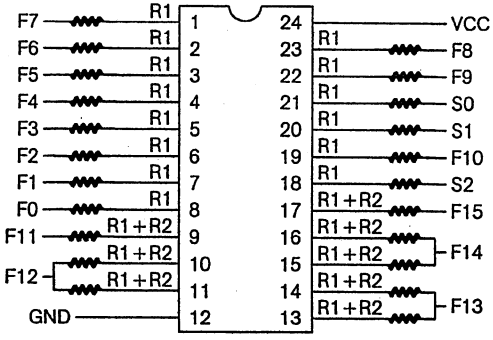
4

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

The reference are : Plastic DIL, 300 mils, 24 pins : 043
Plastic DIL, 600 mils, 24 pins : 03
SOIC DIL, 300 mils, 24 pins : N02
Ceramic, 300 mils, 24 pins : C25
LCC rectangular, 32 pins : L17.

BURN-IN SCHEMATICS



R1 = 220 Ω per row

R2 = 2.2 K Ω per driver

FO = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write/read cycles

VCC = 5.5 V

DATA SHEET

HM 65787

64 K x 1
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 25/35/45/55 ns
  COMMERCIAL : 20/25/35/45 ns
- **LOW POWER CONSUMPTION**
  ACTIVE : 320 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM 65787 is a high speed CMOS static RAM organized as 65536 x 1 bit. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 20 ns are available with maximum power consumption of only 385 mW.

The HM 65787 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

All inputs and outputs of the HM 65787 are TTL compatible and operate from single 5 V supply thus simplifying system design.

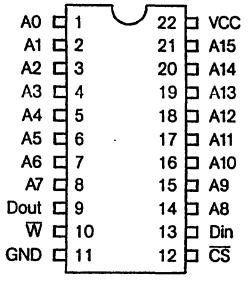
The HM 65787 is processed following the test methods of MIL STD 883C.

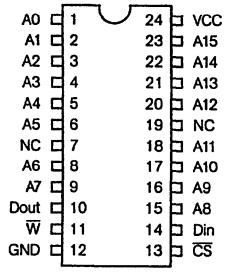
PACKAGES

Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.
Tape and Reel Service

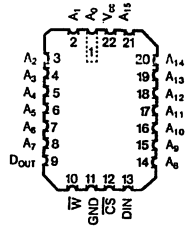
SOIC & SOJ 300 mils, 24 pins, DIL.
LCC 22 pins.

Pinout DIL 22/24 pins (top view)

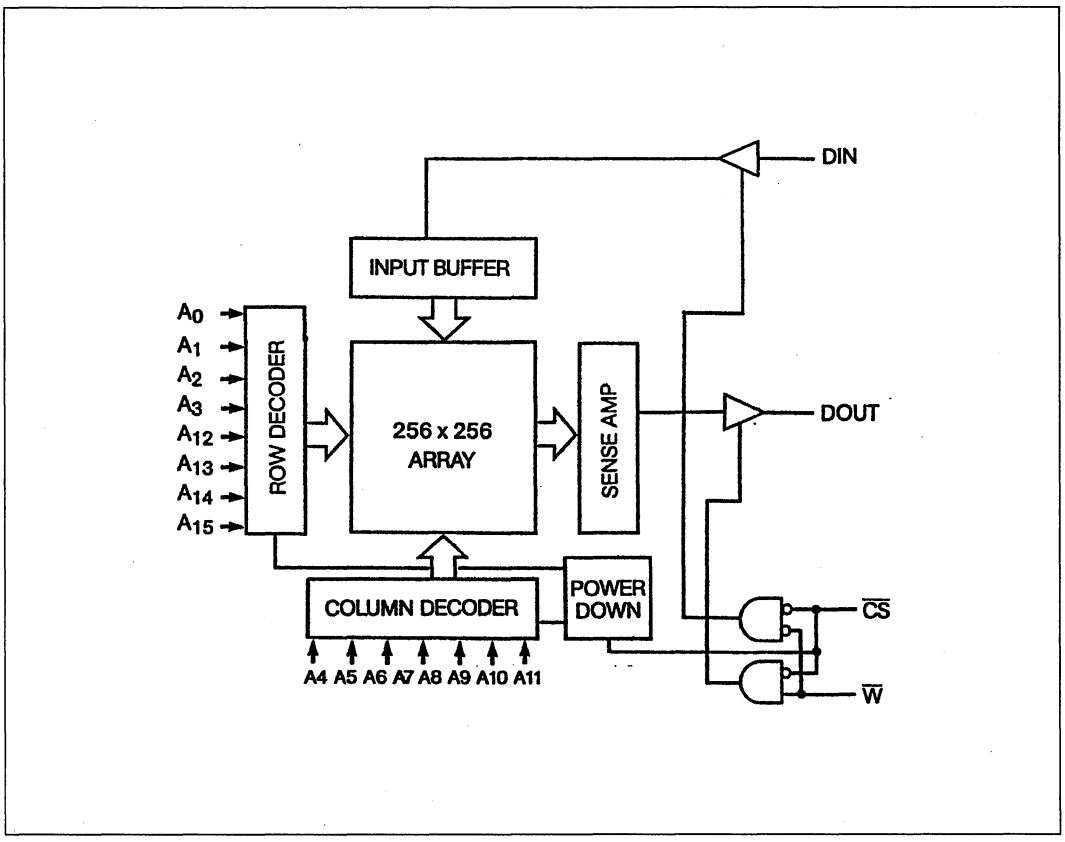




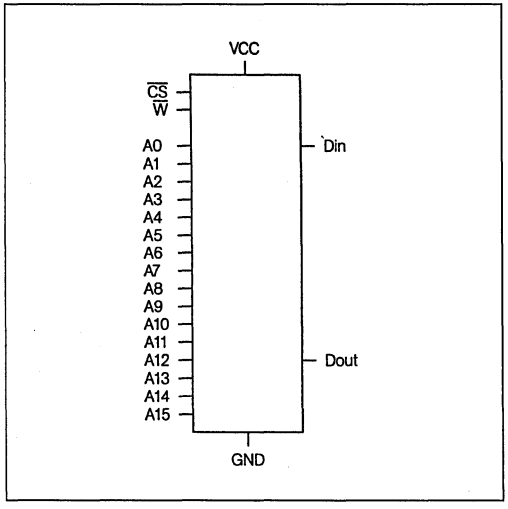
Pinout LCC 22 pins (top view)



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A15	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 0.3 V to + 7.0 V
DC output voltge in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

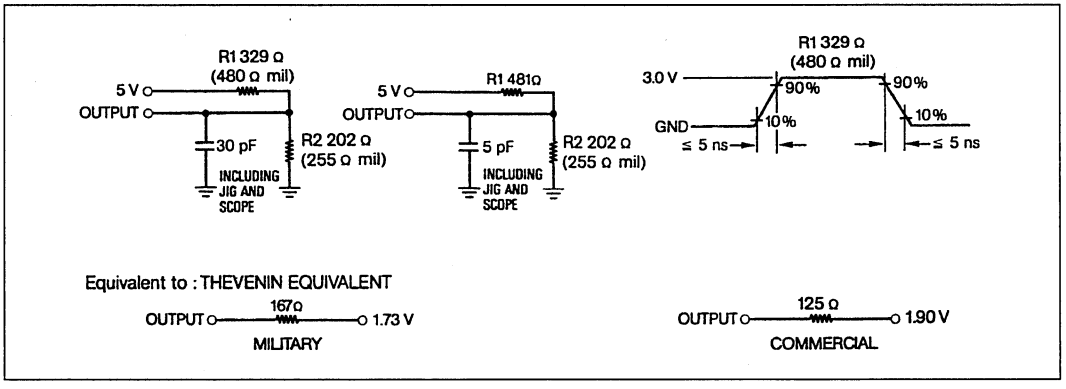
PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
VCC	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	5.5	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, VCC = 5.0 V.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 10.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	

Note : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
4. Vcc min, IOL = 12.0 mA (commercial) 8.0 mA (military).
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL	PARAMETER	65787 F-5	65787 H-5	65787 K-5	65787 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	mA	max

Consumption for Industrial (— 9) and Military specification (— 2) :

SYMBOL	PARAMETER	65787 H-9/-2	65787 K-9/2	65787 N-9/2	65787 N-9/2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) :+ 30 pF

WRITE CYCLE : Commercial specification

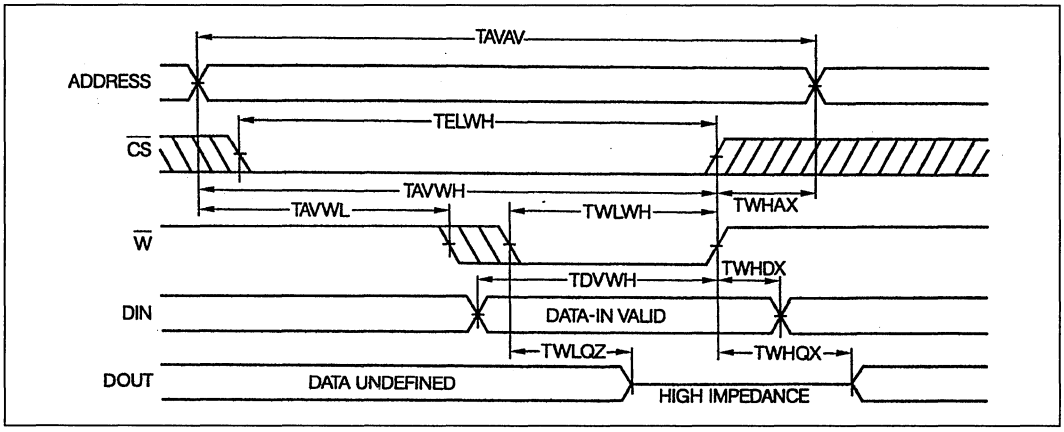
SYMBOL	PARAMETER	65787 F-5	65787 H-5	65787 K-5	65787 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	30	40	ns	min
TDVWH	Data set-up time	15	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	20	ns	max
TWLWH	Write pulse width	15	20	25	25	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	0	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65787 H-9/-2	65787 K-9/-2	65787 M-9/-2	65787 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	30	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	20	20	ns	max
TWLWH	Write pulse width	20	25	25	25	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	0	0	0	0	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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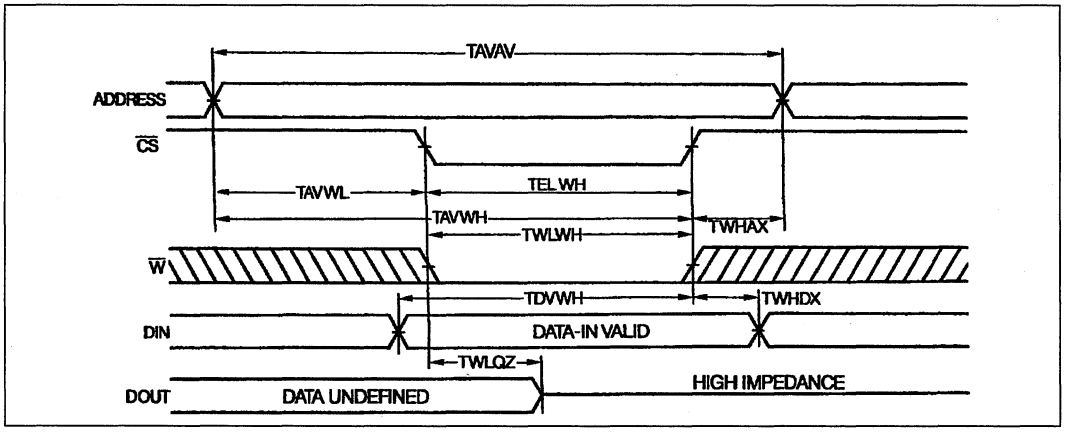
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



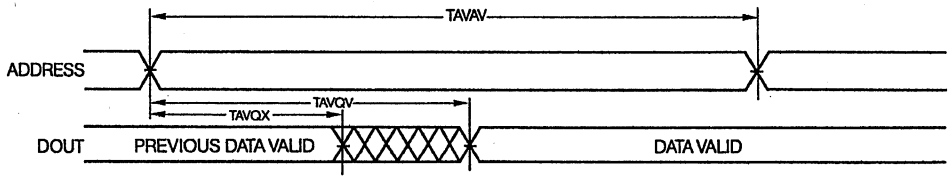
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65787 F-5	65787 H-5	65787 K-5	65787 M-5	UNIT	VALUE
TAVAV	Read cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	20	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	30	ns	max

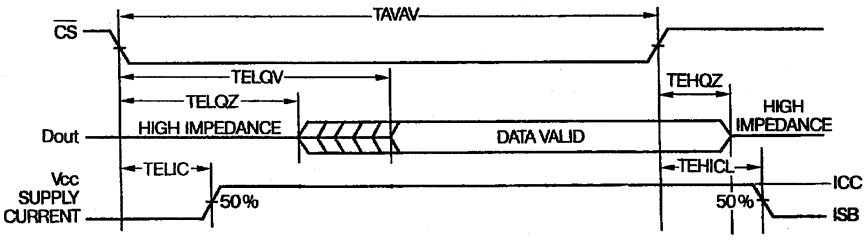
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65787 H-9/-2	65787 K-9/2	65787 M-9/2	65787 N-9/2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	min
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	min
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	25	ns	min
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	30	ns	max

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package	Device	Grade	Type Level
HM1	65787	F	–5 : R

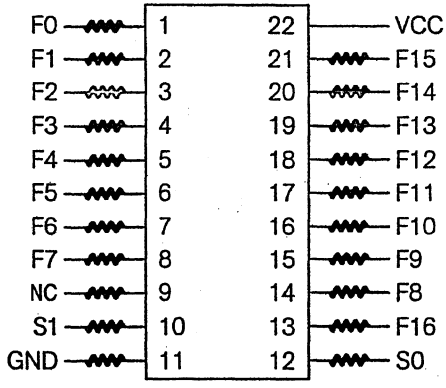
- Package: 0 - Chip form; 1 - Ceramic 22 pins; 3 - Plastic 22 pins; 4 - LCC 22 pins; T - SOIC 24 pins; U - SOJ 24 pins
- Device: 64 k x 1 high speed static RAM
- Grade: F = 20 ns; H = 25 ns; K = 35 ns; M = 45 ns; N = 55 ns
- Type Level: –5 : Commercial; –5+ : Commercial with B.I.; –9 : Industrial; –9+ : Industrial with B.I.; –2 : Military; –8 : Military with B.I.; (B.I. = Burn-In)
- Tape and Reel Service

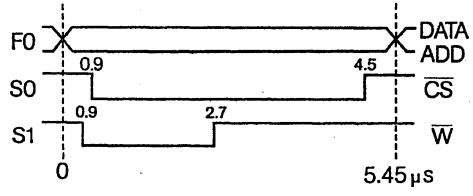
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins : X41
SOIC DIL, 300 mils, 24 pins : TBD
Ceramic, 300 mils, 22 pins : C33
LCC rectangular, 22 pins : L16.

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %
Fn = 1/2 F n-1

S0 & S1 : programmable signals for write/read cycles

NC = Non connected.

DATA SHEET

HM 65788

16 K x 4
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 25/35/45/55 ns
  COMMERCIAL : 20*/25/35/45 ns
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

DESCRIPTION

The HM 65788 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 20 ns are available with maximum power consumption of only 385 mW.

The HM 65788 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

All inputs and outputs of the HM 65788 are TTL compatible and operate from single 5 V supply thus simplifying system design.

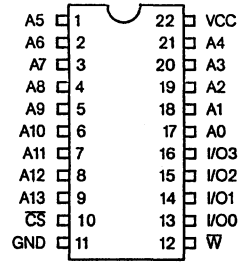
The HM 65788 is processed following the test methods of MIL STD 883C.

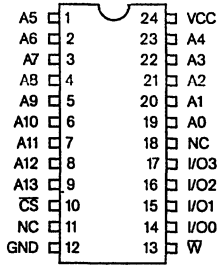
PACKAGES

Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.
Tape and Reel Service.

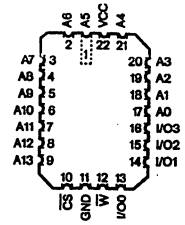
SOIC & SOJ 300 mils, 24 pins, DIL.
LCC 22 pins.

Pinout DIL 22/24 pins (top view)



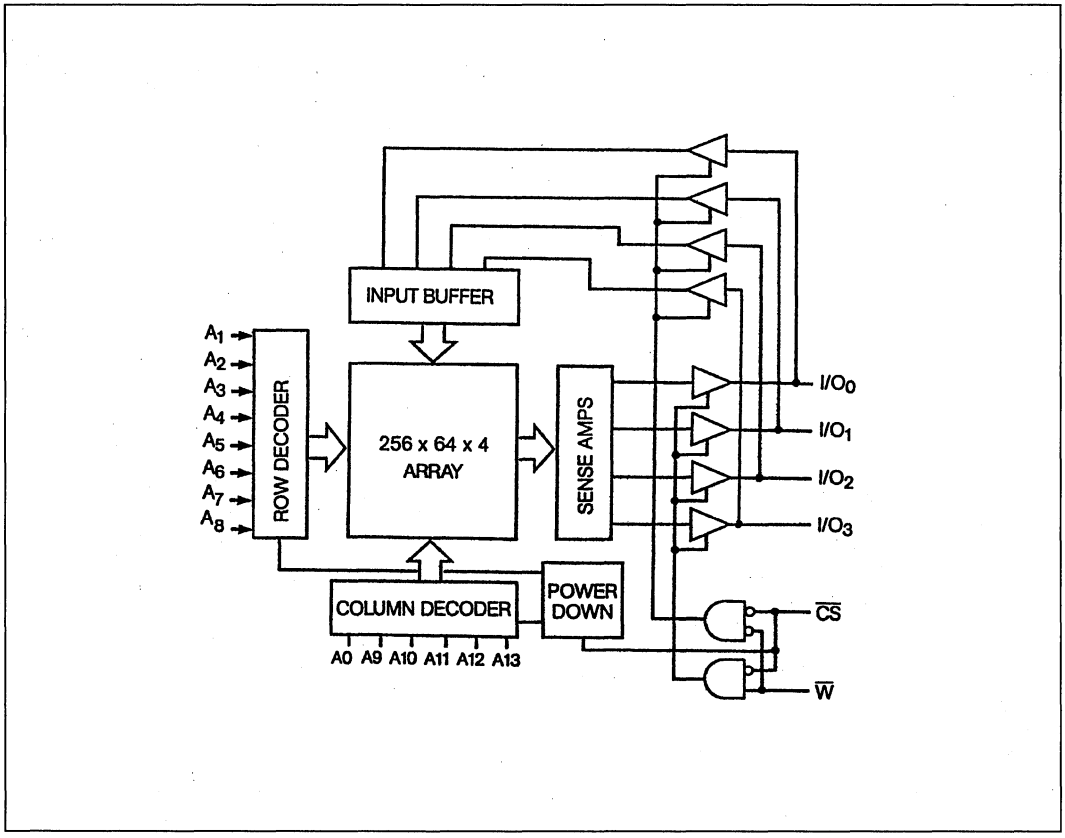


Pinout LCC 22 pins (top view)

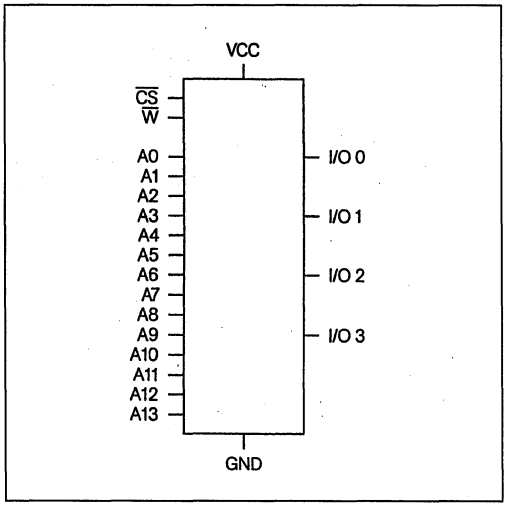


* preliminary

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A13	: Address inputs	GND	: Ground
I/O0-I/O3	: Inputs/Outputs	$\overline{CS}$	: Chip select
VCC	: Power	$\overline{W}$	: Write enable

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 0.3 V to + 7.0 V
DC output voltge in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

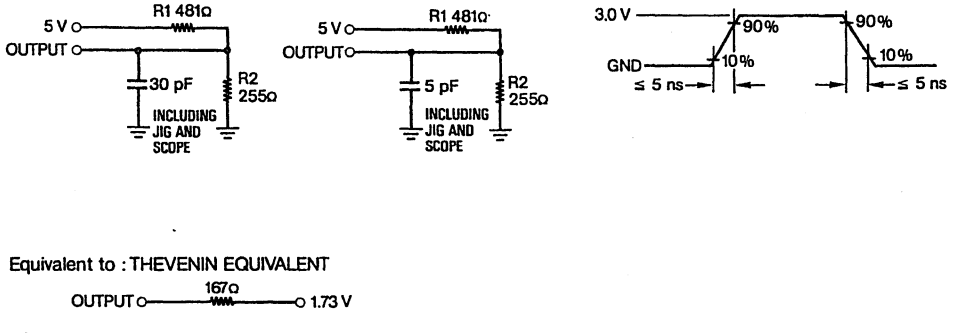
PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, VCC = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 10.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL	PARAMETER	65788 F-5	65788 H-5	65788 K-5	65788 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	mA	max

Consumption for Industrial (– 9) and Military specification (– 2) :

SYMBOL	PARAMETER	65788 K-9/2	65788 M-9/2	65788 N-9/-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) : + 30

WRITE CYCLE : Commercial specification

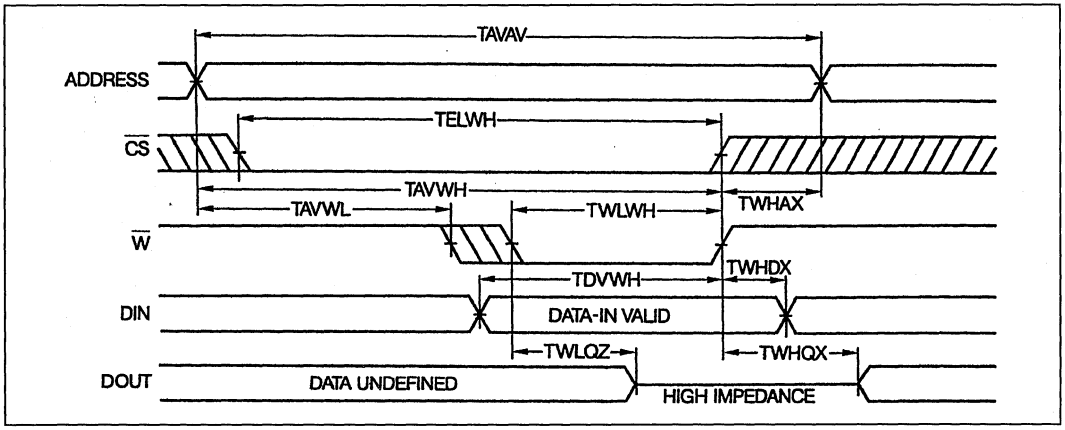
SYMBOL	PARAMETER	65788 F-5	65788 H-5	65788 K-5	65788 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	25	35	ns	min
TDVWH	Data set-up time	13	13	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	30	35	ns	min
TWLQZ (9)	Write low to high Z	7	7	10	15	ns	max
TWLWH	Write pulse width	15	20	25	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	5	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65788 K-9/2	65788 M-9/2	65788 N-9/2	UNIT	VALUE
TAVAV	Write cycle time	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	25	35	45	ns	min
TDVWH	Data set-up time	15	20	30	ns	min
TELWH	$\overline{CS}$ low to write end	30	35	45	ns	min
TWLQZ (8)	Write low to high Z	10	15	25	ns	max
TWLWH	Write pulse width	25	35	45	ns	min
TWHAX	Address hold from end of write	0	0	0	ns	min
TWHDX	Data hold time	0	5	5	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



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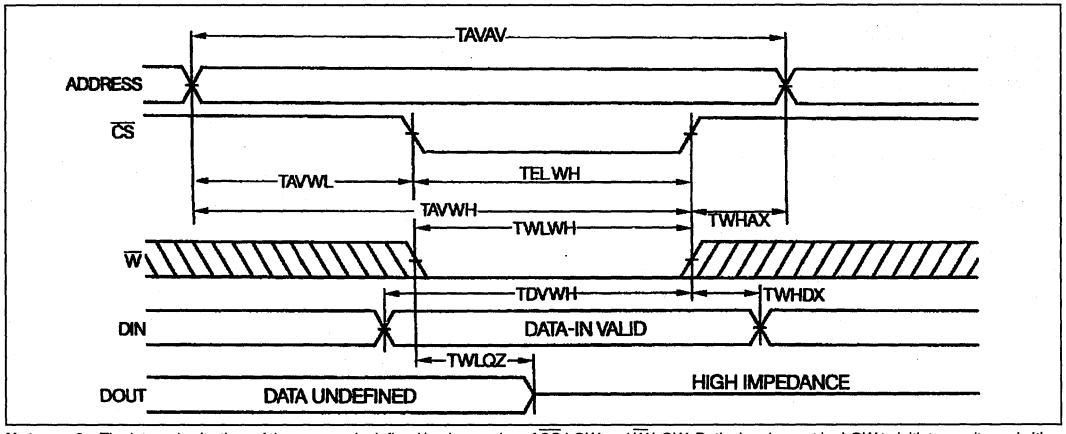
WRITE CYCLE 2 $\overline{CS}$ CONTROLLED (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65788 F-5	65788 H-5	65788 K-5	65788 M-5	UNIT	VALUE
TAVAV	Read cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	20	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	10	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	35	45	ns	max

READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65788 K-9/2	65788 M-9/2	65788 N-9/2	UNIT	VALUE
TAVAV	Read cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	35	45	55	ns	max

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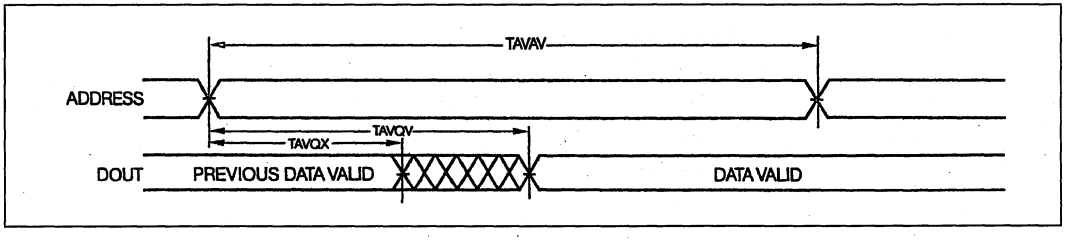
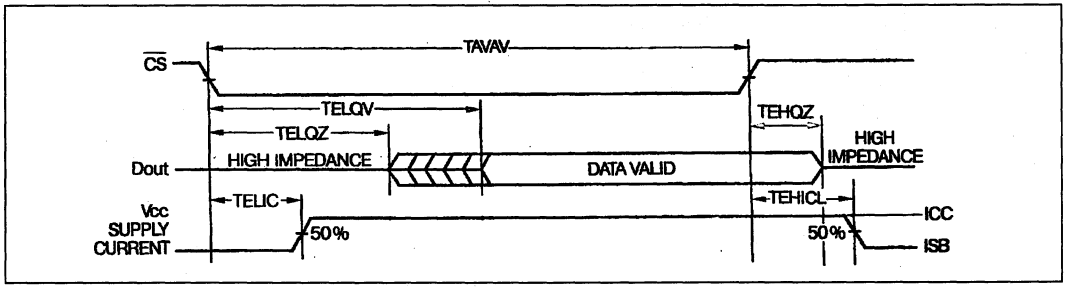
READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65788	F	– 5 : R

- Package: 0 - Chip form; 1 - Ceramic 22 pins; 3 - Plastic 22 pins; 4 - LCC 22 pins; T - SOIC 24 pins; U - SOJ 24 pins
- Device type: 16 k x 4 High speed static RAM
- Grade: F = 20 ns; H = 25 ns; K = 35 ns; M = 45 ns; N = 55 ns
- Level: – 5 : Commercial; – 5+ : Commercial with B.I.; – 9 : Industrial; – 9+ : Industrial with B.I.; – 2 : Military; – 8 : Military with B.I. (B.I. = Burn-In)
- Tape and Reel Service

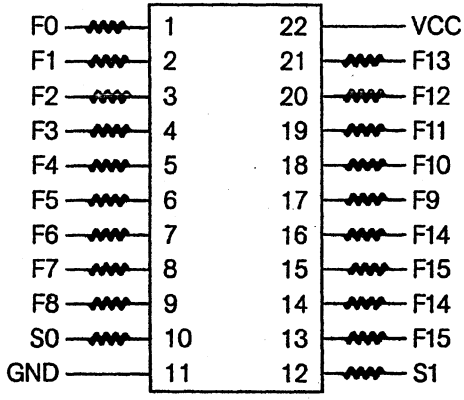
4

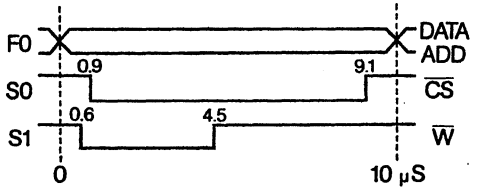
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins : 041
SOIC DIL, 300 mils, 24 pins : NO2
Ceramic, 300 mils, 22 pins : C33
LCC rectangular, 22 pins : L23.

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %
Fn = 1/2 F n-1

S0 & S1 : programmable signals for write/read cycles

NC = Non connected.

DATA SHEET

HM 65789

16 K x 4
HIGH SPEED CMOS SRAM
WITH OUTPUT ENABLE

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns
  COMMERCIAL : 20*/25/35/45 ns
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **OUTPUT ENABLE**

DESCRIPTION

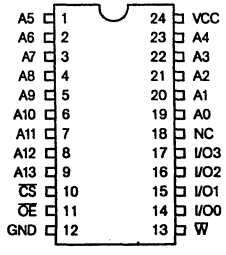
The HM 65789 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 20 ns are available with maximum power consumption of only 385 mW.
The HM 65789 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65789 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65789 is processed following the test methods of MIL STD 883C.

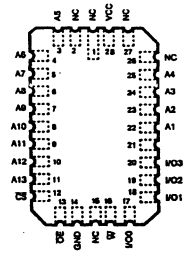
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
Tape and Reel Service.
SOIC & SOJ 300 mils, 24 pins, DIL.
LCC 28 pins.

Pinout DIL 24 pins (top view)



Pinout LCC 28 pins (top view)



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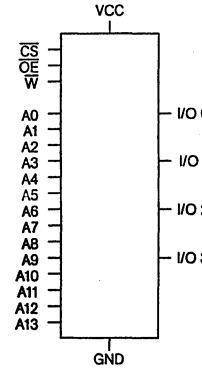
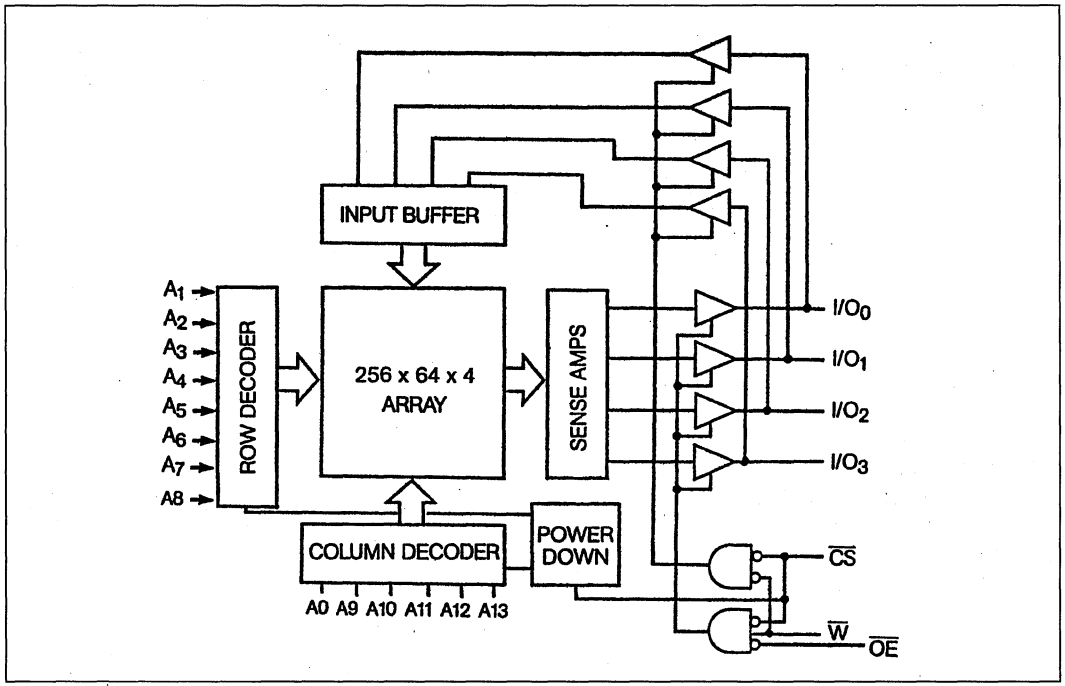
LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13	: Address inputs	$\overline{CS}$	: Chip-select
I/O0-I/O3	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	X	L	Valid	Z	Write

L = low - H = high - X = H or L-Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

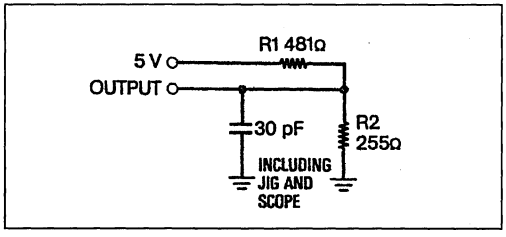


Fig. 1a.

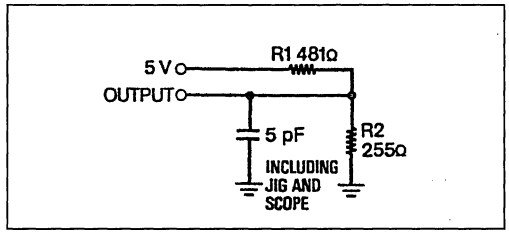
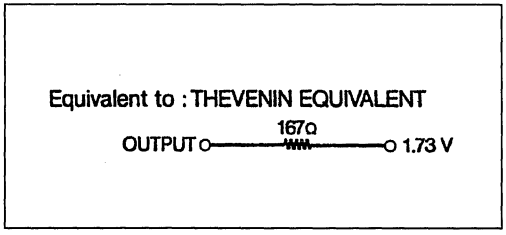


Fig. 1b.



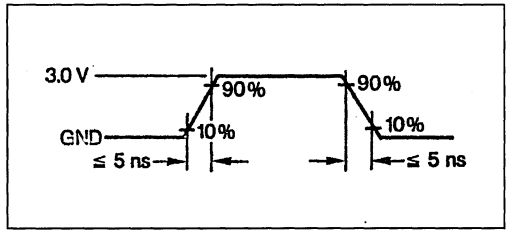


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 10.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65789 K-9/-2	65789 M-9/2	65789 N-9/-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : + 30 pF

WRITE CYCLE : Commercial specification

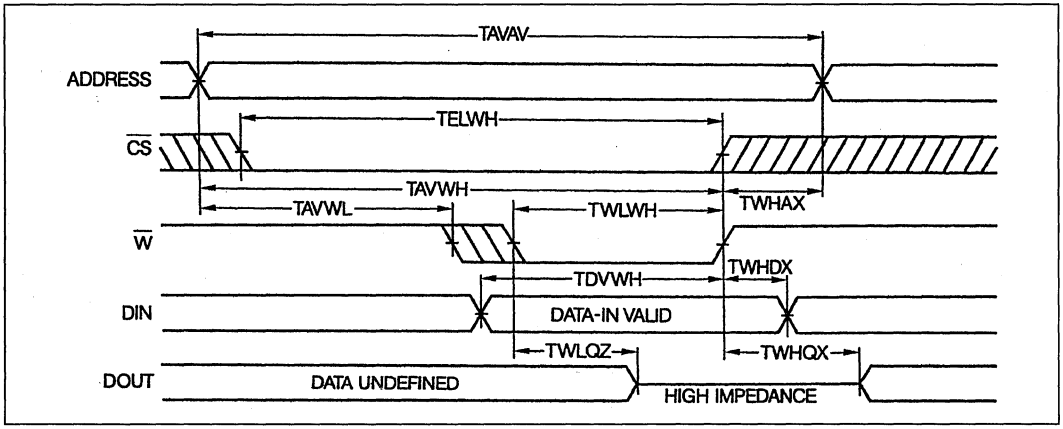
SYMBOL	PARAMETER	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	25	35	ns	min
TDVWH	Data set-up time	10	13	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	30	35	ns	min
TWLQZ	Write low to high Z	7	7	10	15	ns	max
TWLWH	Write pulse width	15	20	25	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65789 K-9/-2	65789 M-9/-2	UNIT	VALUE
TAVAV	Write cycle time	35	45	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	25	35	ns	min
TDVWH	Data set-up time	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	30	35	ns	min
TWLQZ (8)	Write low to high Z	10	15	ns	max
TWLWH	Write pulse width	25	35	ns	min
TWHAX	Address hold from end of write	0	0	ns	min
TWHDX	Data hold time	0	5	ns	min
TWHQX (8)	Write high to low Z	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 9)



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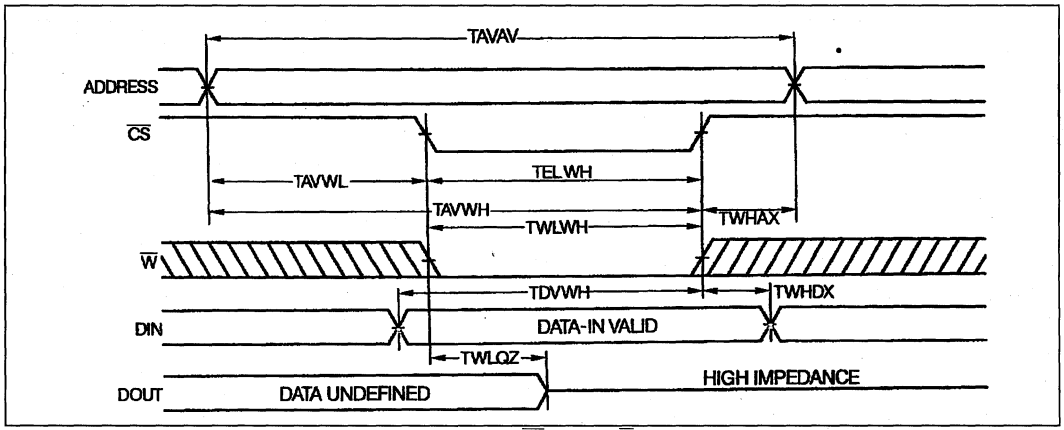
WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a writee by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out will be high impedance if $\overline{OE}$ = VIH.

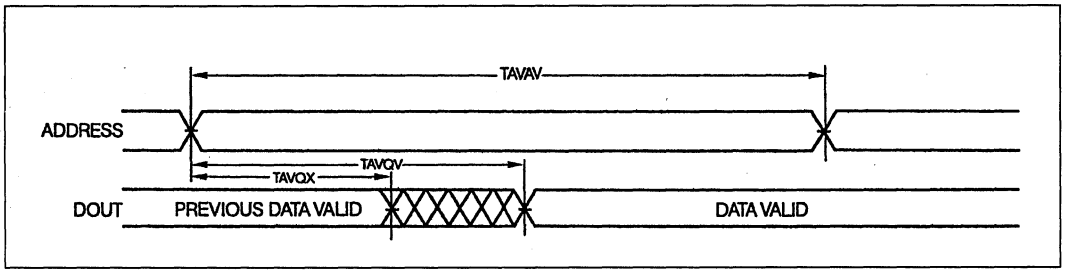
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
TAVAV	Read cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	20	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	10	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	35	45	ns	max
TGLQV	Output enable access time	10	15	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	15	15	15	ns	max

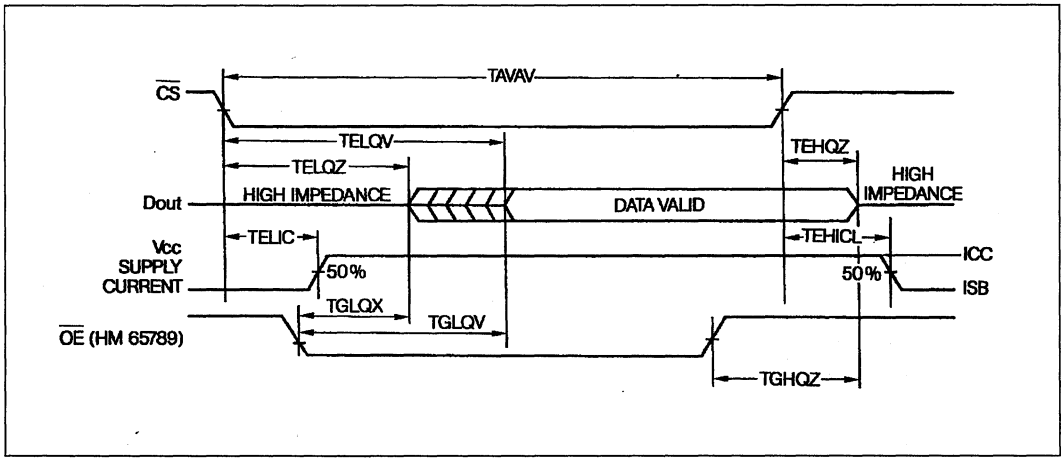
READ CYCLE : Military specification

SYMBOL	PARAMETER	65789 K9/2	65789 M9/2	65789 N-9/2	UNIT	VALUE
TAVAV	Read cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	35	45	55	ns	max
TGLQV	Output enable access time	25	30	40	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	15	ns	max

READ CYCLE nb 1 : (notes 10, 11)



READ CYCLE nb 2 : (notes 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package
HM1
0 - Chip form
1 - Ceramic 24 pins
3 - Plastic 24 pins
4 - LCC 28 pins
T - SOIC 24 pins
U - SOJ 24 pins

Device type
65767
16 k x 4 high speed static RAM with output enable

Grade
F
F = 20 ns
H = 25 ns
K = 35 ns
M = 45 ns

Level
– 5 : R
Tape and Reel Service
– 5 : Commercial
– 5+ : Commercial with B.I.
– 9 : Industrial
– 9+ : Industrial with B.I.
– 2 : Military
– 8 : Military with B.I.
(B.I. = Burn-In)

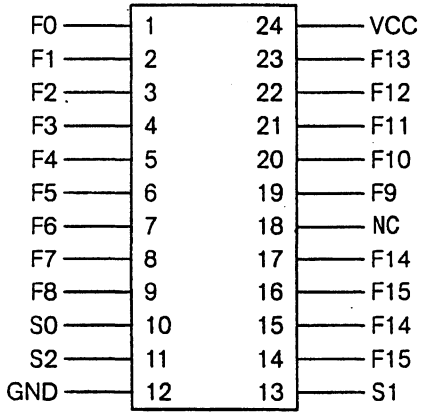
4

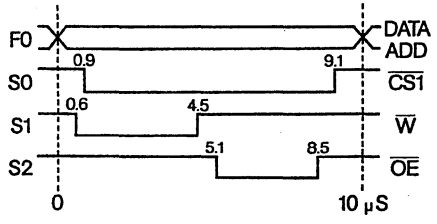
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins :
SOIC DIL, 300 mils, 24 pins :
Ceramic, 300 mils, 24 pins :
LCC rectangular, 28 pins :

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
FO = 50 KHz ± – 20 %
Fn = 1/2 Fn – 1
S0 to S2 = programmable signals for write/read cycles
NC = Non connected

DATA SHEET

HM 65790

16 K x 4
HIGH SPEED CMOS SRAM
SEPARATE I/O

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 35/45 ns (max)
  COMMERCIAL : 25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUTS/OUTPUTS**
- **OUTPUT ENABLE**

DESCRIPTION

The HM 65790 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 385 mW.
The HM 65790 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

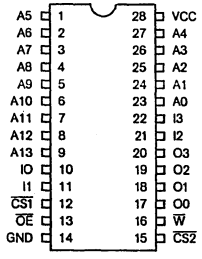
Easy memory expansion is provided by two active low chip select (CS1, CS2), an active low output enable (OE) and three state drivers.
All inputs and outputs of the HM 65790 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65790 is processed following the test methods of MIL STD 883C.

PACKAGES

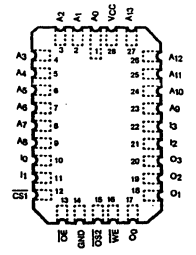
Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
Tape and Reel Service.

SOIC & SOJ 300 mils, 28 pins, DIL.
LCC 28 pins.

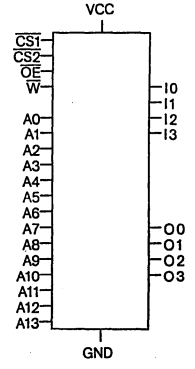
Pinout DIL 28 pins (top view)



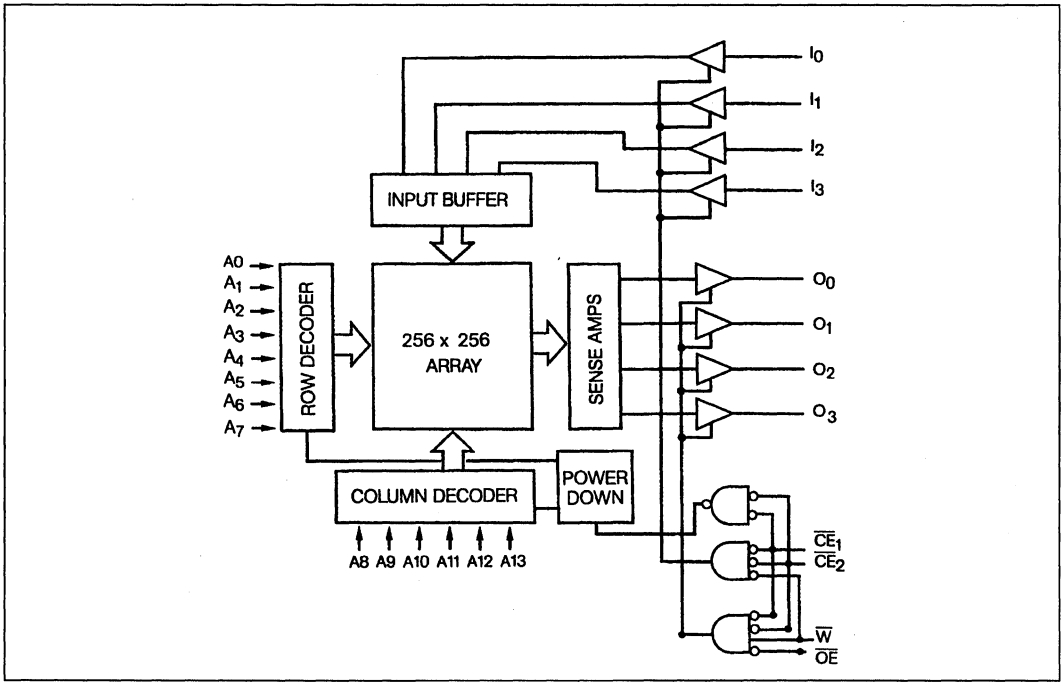
Pinout LCC 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A13	: Address inputs	$\overline{CS1}$-$\overline{CS2}$	: Chip Select
I0-I3	: Inputs	$\overline{OE}$	: Output enable
O0-O3	: Outputs	$\overline{W}$	: Write enable
VCC	: Power	GND	: Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	X	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

4

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

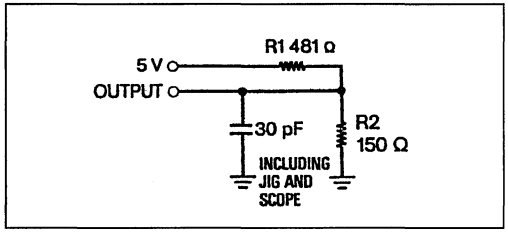


Fig. 1a.

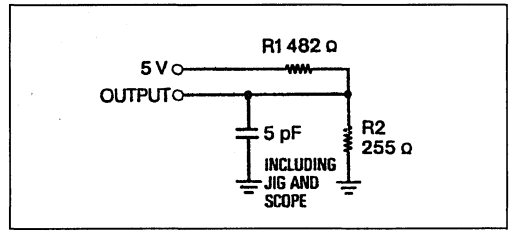
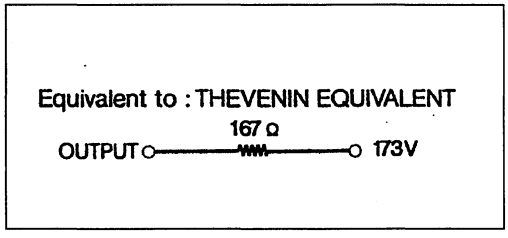


Fig. 1b.



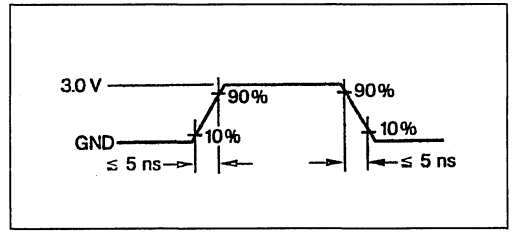


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL		PARAMETER	65790 H-5	65790 K-5	65790 M-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	70	70	70	mA	max

Consumption for Military specification :

SYMBOL		PARAMETER	65790 K-2	65790 M-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	mA	max
ICCOP	(7)	Dynamic operating current	70	70	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input risqe : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) : + 30 pF

WRITE CYCLE : Commercial specification

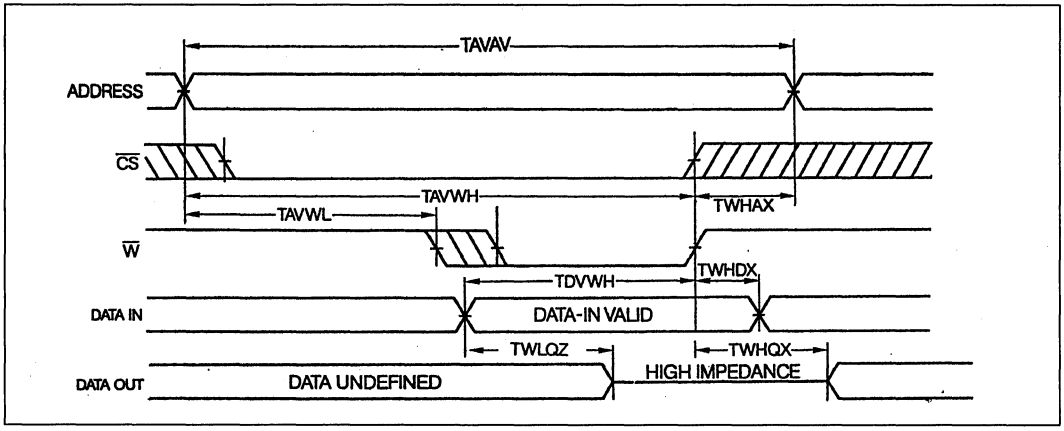
SYMBOL	PARAMETER	65790 H-5	65790 K-5	65790 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	30	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	35	ns	min
TDVWH	Data set-up time	13	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	35	ns	min
TWLQZ	Write low to high Z	7	10	15	ns	max
TWLWH	Write pulse width	20	25	35	ns	min
TWHAX	Address hold from end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65790 K-2	65790 M-2	UNIT	VALUE
TAVAV	Write cycle time	30	40	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address Valid to end of write	25	35	ns	min
TDVWH	Data set-up time	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	30	35	ns	min
TWLQZ (8)	Write low to high Z	10	15	ns	max
TWLWH	Write pulse width	25	35	ns	min
TWHAX	Address hold from end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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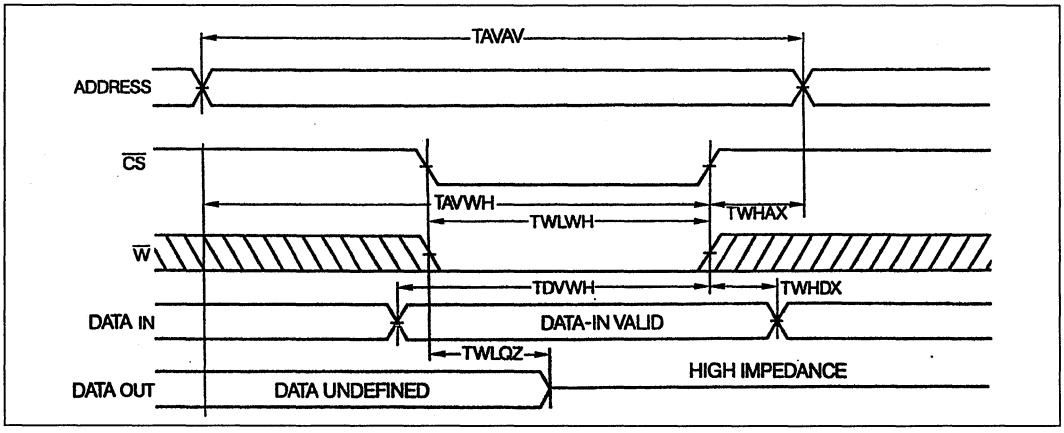
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



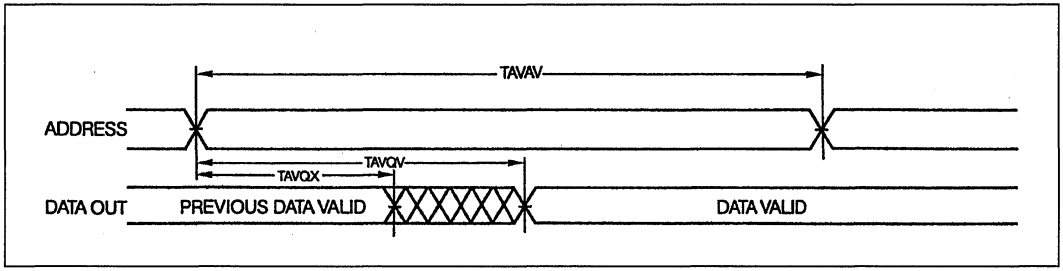
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65790 H-5	65790 K-5	65790 M-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	35	45	ns	max
TGLQV	Output enable access time	15	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQX	$\overline{OE}$ high to high Z	15	15	15	ns	max

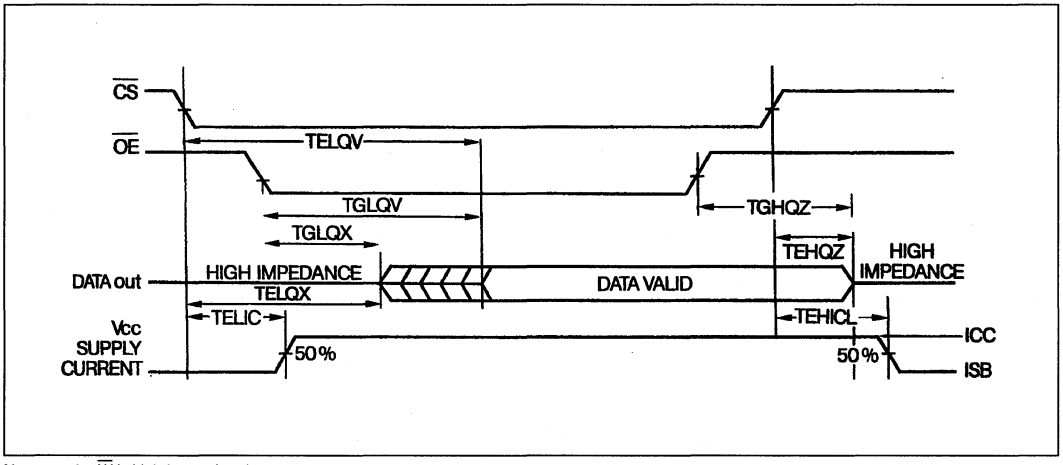
READ CYCLE : Military specification

SYMBOL	PARAMETER	65790 K-2	65790 M-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	ns	min
TAVQV	Address access time	35	45	ns	max
TAVQX	Address valid to low Z	3	3	ns	min
TELQV	Chip-select access time	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	35	45	ns	max
TGLQV	Output enable access time	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	ns	min

READ CYCLE nb 1 (notes 9, 10)



READ CYCLE nb 2 (notes 9, 11)



Notes : 9. $\overline{W}$ is high for read cycle.
10. Device is continuously selected, $\overline{CS_1}$, $\overline{CS_2}$ = VIL.
11. Address valid prior to or coincider with $\overline{CS_1}$, $\overline{CS_2}$ transition low.

ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65790	H	– 5
0 - Chip form 1 - Ceramic 28 pins 3 - Plastic 28 pins 4 - LCC 28 pins T - SOIC 28 pins U - SOJ 28 pins	16 k x 4 high speed static RAM with separate I/O	H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

4

PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins : 049.
SOIC DIL, 300 mils, 28 pins : N10.
Ceramic, 300 mils, 28 pins : C31.
LCC rectangular, 32 pins : L32.

DATA SHEET

HM 65791

16 K x 4
HIGH SPEED CMOS SRAM
SEPARATE I/O AND TRANSPARENT WRITE

FEATURES

- **FAST ACCESS TIME**
  MILITARY : 35/45 ns (max)
  COMMERCIAL : 25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUTS/OUTPUTS**
- **TRANSPARENT WRITE**
- **OUTPUT ENABLE**

DESCRIPTION

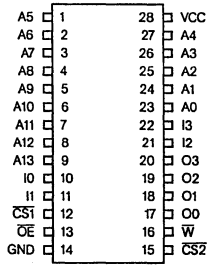
The HM 65791 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 385 mW.
The HM 65791 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip select (CS1, CS2), an active low output enable (OE) and three state drivers.
All inputs and outputs of the HM 65791 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65791 is processed following the test methods of MIL STD 883C.

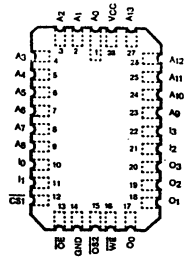
PACKAGES

Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
Tape and Reel Service.
SOIC & SOJ 300 mils, 28 pins, DIL.
LCC 28 pins.

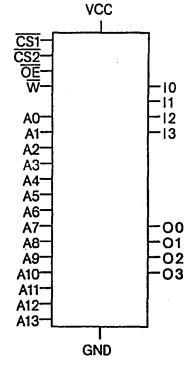
Pinout DIL 28 pins (top view)



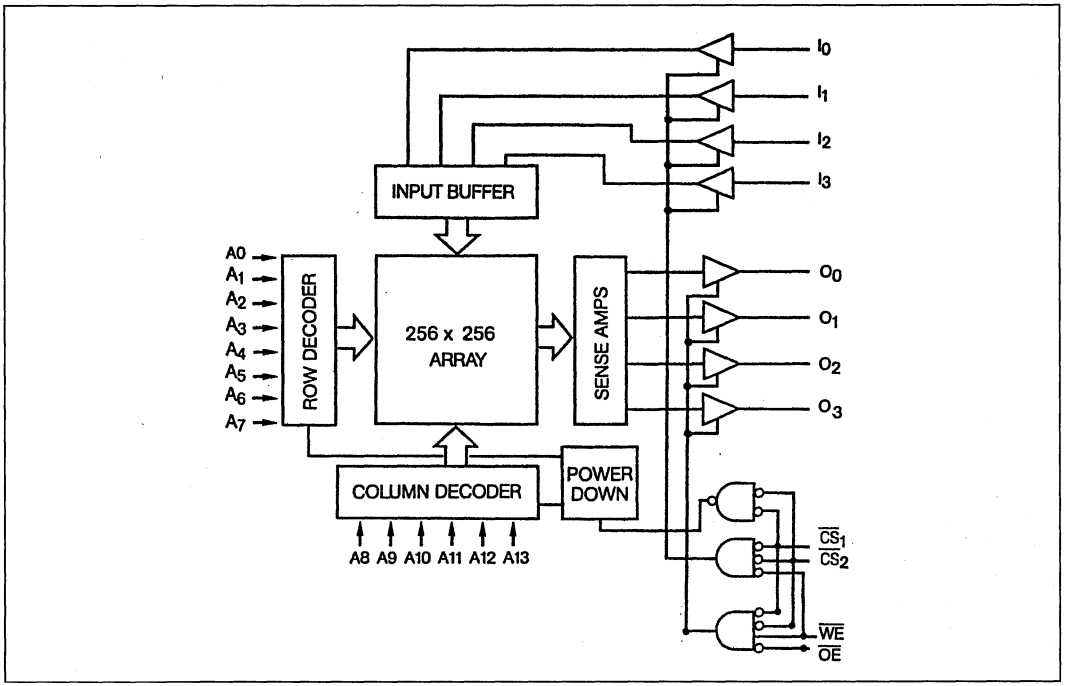
Pinout LCC 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A13 : Address inputs	CS1-CS2 : Chip-Select
I0-I3 : Inputs	OE : Output enable
O0-O3 : Outputs	W : Write enable
VCC : Power	GND : Ground

TRUTH TABLE

CS	OE	W	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Valid	Write
L	L	L	Valid	Valid	Write

L = low, H = high, or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

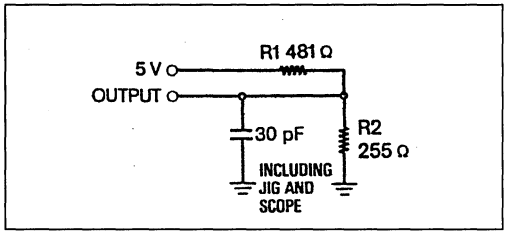


Fig. 1a.

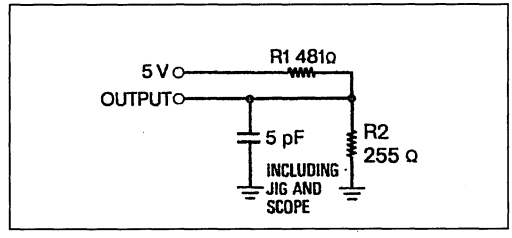
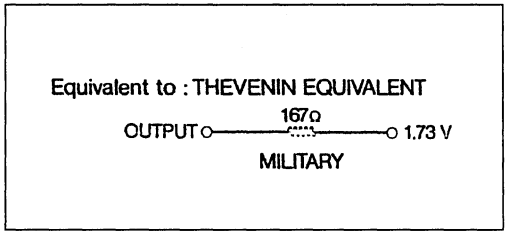


Fig. 1b.



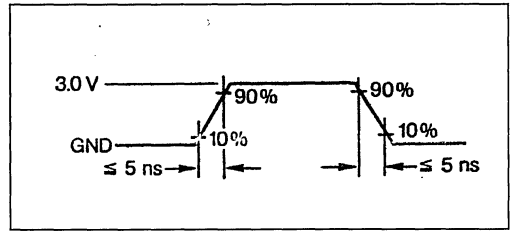


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic Operating current	70	70	70	mA	max

Consumption for Industrial (– 9) and Military specification (2) :

SYMBOL		PARAMETER	65791 K-9/2	65791 M-9/2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	mA	max
ICCOP	(7)	Dynamic operating current	70	70	mA	max

Notes : 6. $\overline{CS} \geq$ VIH.
7. Vcc max, Output current = 0mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise - : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : + 30 pF

WRITE CYCLE : Commercial specification

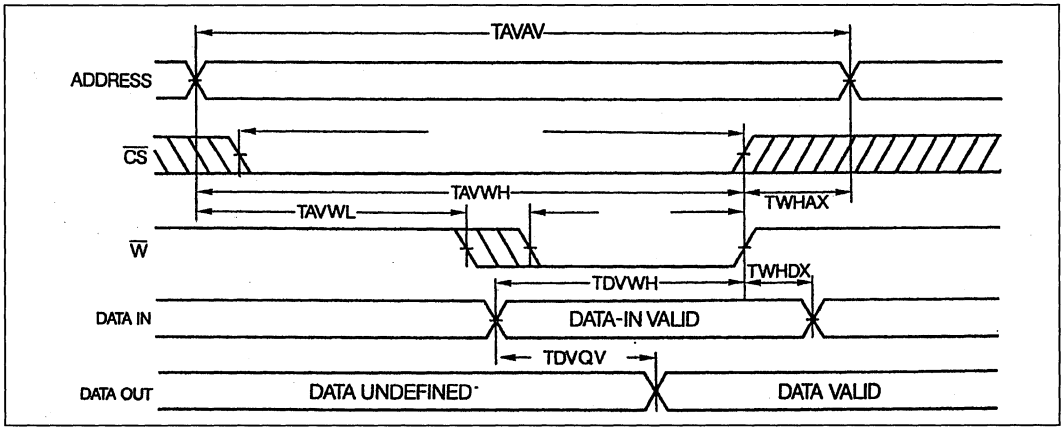
SYMBOL	PARAMETER	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	30	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address Valid to end of write	20	25	35	ns	min
TDVWH	Data set-up time	13	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	35	ns	min
TWLQZ	Write low to high Z	7	10	15	ns	max
TWLWH	Write pulse width	20	25	35	ns	min
TWHAX	Address hold from end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWLQV	$\overline{W}$ low to data valid	25	30	35	ns	max
TDVQV	Data valid to output valid	20	30	35	ns	max

WRITE CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65791 K-9/2	65791 M-9/2	UNIT	VALUE
TAVAV	Write cycle time	30	40	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	25	35	ns	min
TDVWH	Data set-up time	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	30	35	ns	min
TWLQZ (8)	Write low to high Z	10	15	ns	max
TWLWH	Write pulse width	25	35	ns	min
TWHAX	Address hold from end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWLQV	$\overline{W}$ low to data valid	30	35	ns	max
TDVQV	Data valid to output valid	30	35	ns	max

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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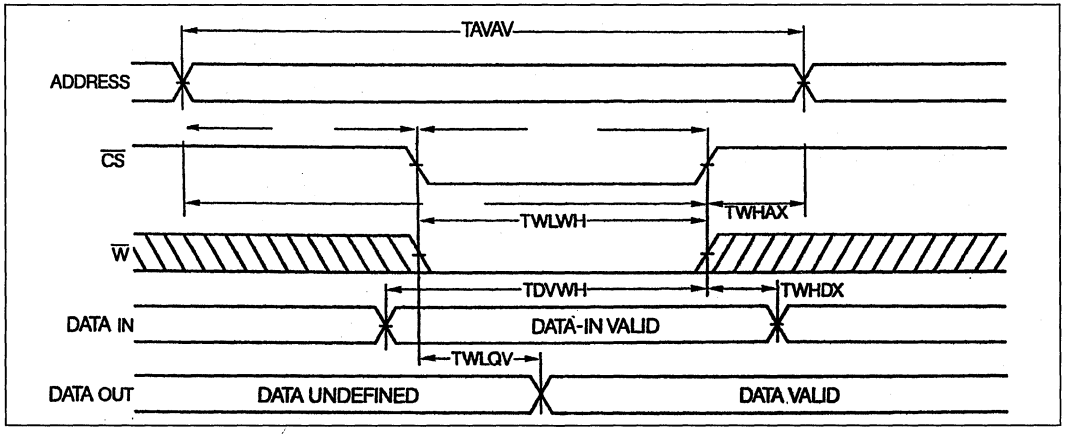
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



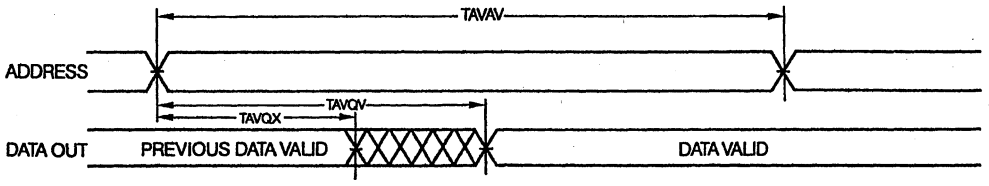
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	max
TAVQX	Address Valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	35	45	ns	max
TGLQV	Output enable access time	15	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	15	ns	max

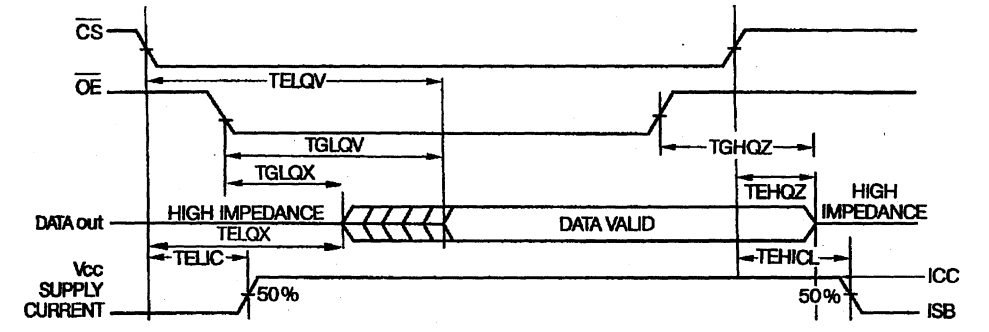
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65791 K-9/2	65791 M-9/2	UNIT	VALUE
TAVAV	READ cycle time	35	45	ns	min
TAVQW	Address access time	35	45	ns	max
TAVQX	Address Valid to low Z	3	3	ns	min
TELQV	Chip-select access time	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	35	45	ns	max
TGLQV	Output enable access time	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	ns	min

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65791	H	– 5
0 - Chip form 1 - Ceramic 24 pins 3 - Plastic 28 pins 4 - LCC 28 pins T - SOIC 28 pins U - SOJ 28 pins	16 k x 4 high speed static RAM with separate I/O and transparent write	H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

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PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins : 049
SOIC DIL, 300 mils, 28 pins : N10
Ceramic, 300 mils, 28 pins : C31
LCC rectangular, 28 pins : C32

DATA SHEET

HM 65764

8 k x 8
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 380 mW (typ)
  STANDBY : 110mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

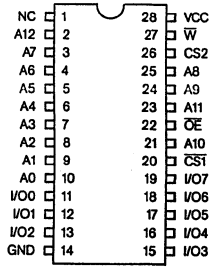
DESCRIPTION

The HM 65764 is a high speed CMOS static RAM organized as 8192x8 bits. It is manufactured using MHS high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 550 mW.
The HM 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.
Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65764 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65764 is processed following the test methods of MIL STD 883C.

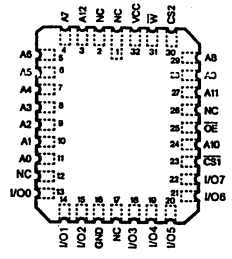
PACKAGES

Plastic 300 & 600 mil, 28 pins, DIL.
Ceramic 300 mils, 600 mils, 28 pins, DIL
SOIC & SOJ 300 mils, 28 pins, DIL.
LCC 32 pins.

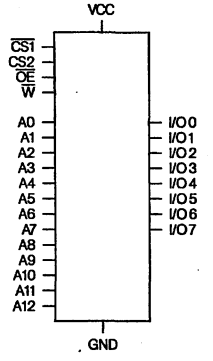
Pinout DIL 28 pins (top view)



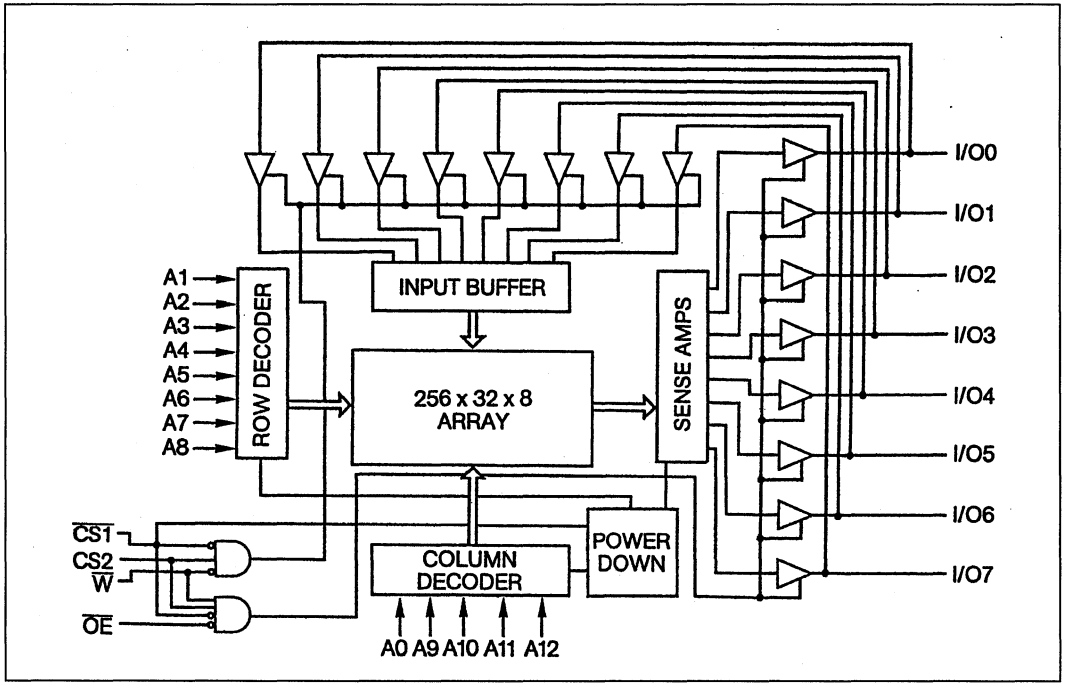
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A13 : Address inputs	$\overline{CS1}$: Chip Select 1
I/O0-I/O7 : Inputs/Outputs	CS2 : Chip Select 2
VCC : Power	$\overline{OE}$: Output enable
GND : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low - H = high - X = H or L-Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

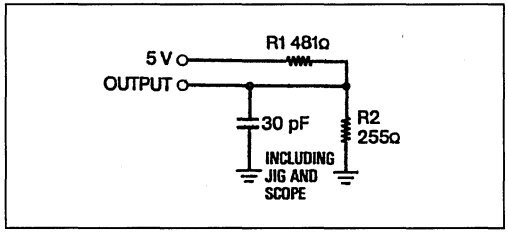


Fig. 1a.

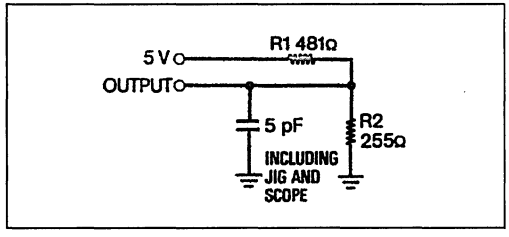
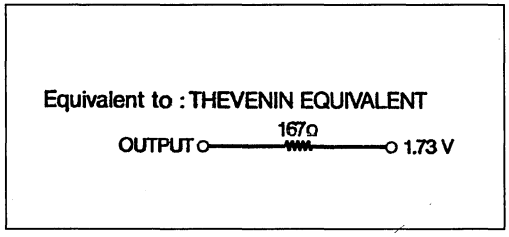


Fig. 1b.



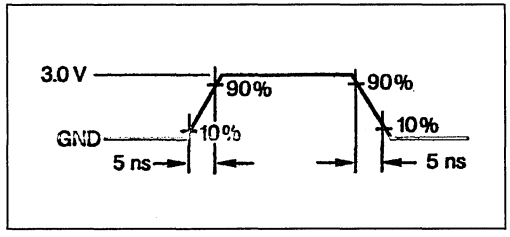


Fig. 2

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	25	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current		100	100	100	mA	max

Consumption for Industrial (– 9) and Military specification (2) :

SYMBOL		PARAMETER	65764 K-9/2	65764 M-9/2	65764 N-9/2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Operating supply current	100	100	100	mA	max

Notes : 6. $\overline{CS1} \geq VIH$, $CS2 \leq VIL$.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 10 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1 and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

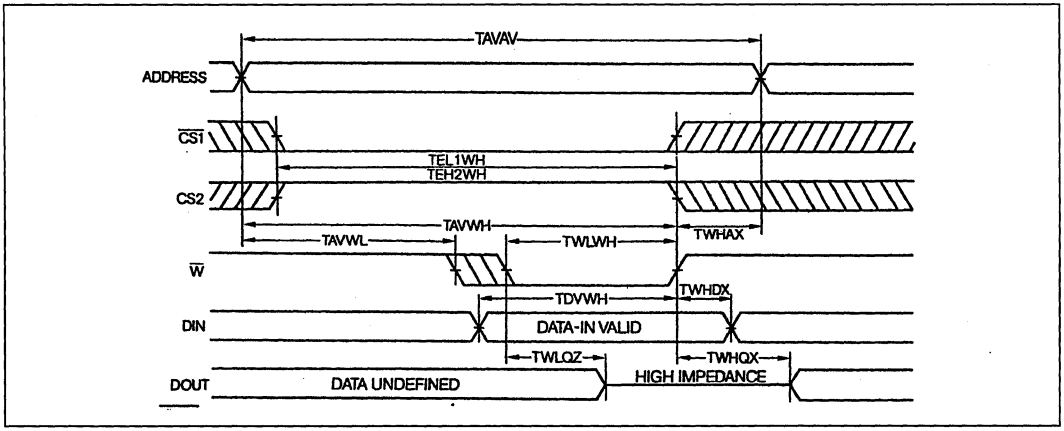
SYMBOL	PARAMETER	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	10	15	20	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	25	30	40	50	ns	min
TEH2WH	CS2 high to write end	20	20	25	30	ns	min
TWLQZ (9)	Write low to high Z	15	15	20	25	ns	max
TWLWH	Write pulse width	20	20	25	30	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65764 K-9/-2	65764 M-9/-2	65764 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	30	40	50	ns	min
TEH2WH	CS2 high to write end	20	25	30	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	ns	min
TWHAX	Address hold to end from write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



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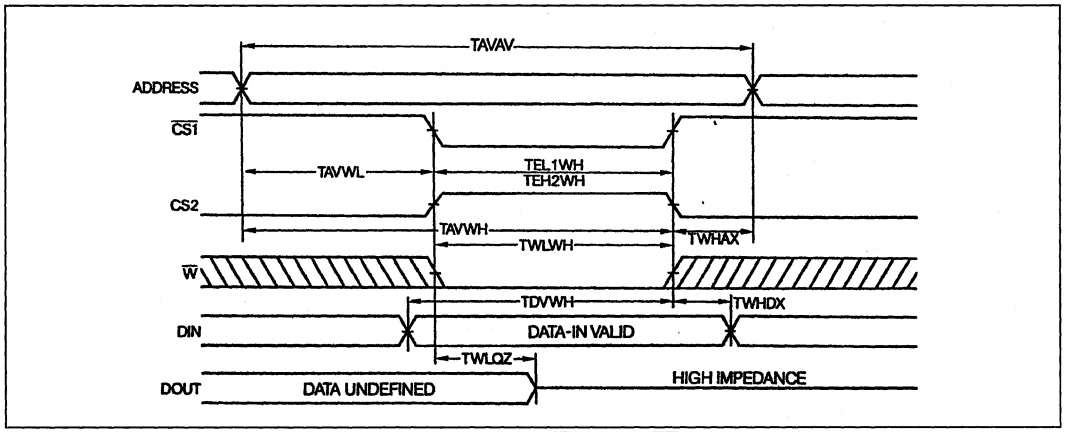
WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE}$ = VIH.

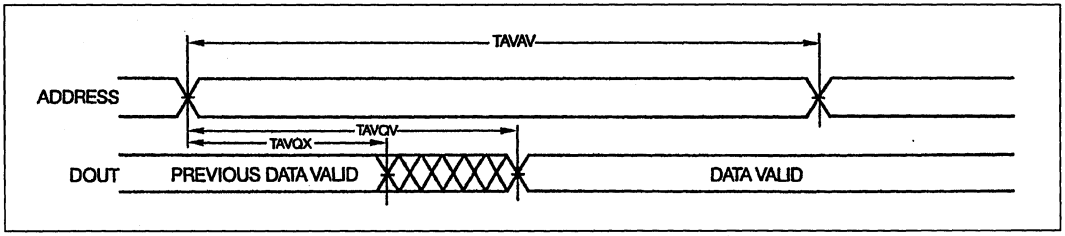
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	15	15	20	20	ns	max
TEL2QZ (11)	CS2 low to high Z	15	15	20	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEL1ICCL	CS1 high to power up	20	20	25	25	ns	max
TGLQV	Output enable access time	15	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	20	25	30	ns	max

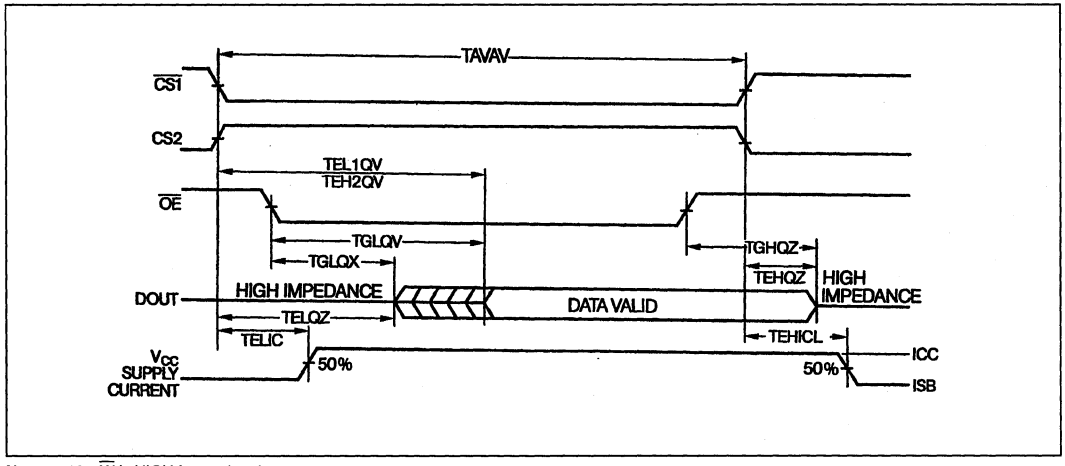
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65764 K-9/-2	65764 M-9/-2	65764 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	15	20	20	ns	max
TEL2QZ (11)	CS2 high to high Z	15	20	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	ns	min
TEH1ICCL	CS1 high to power down	20	25	25	ns	max
TGLQV	Output enable access time	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	20	25	30	ns	min

READ CYCLE nb 1 (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{CS_1}$ & $\overline{OE}$ = VIL and CS_2 = VIH.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package
HM1
0 - Chip form
1 - Ceramic 28 pins 300 mils
1E - Ceramic 28 pins 600 mils
3 - Plastic 28 pins 300 mils
3E - Plastic 28 pins 600 mils
4 - LCC 32 pins
T - SOIC 28 pins
U - SOJ 28 pins

Device type
65764
8 k x 4 High speed static RAM

Grade
H
H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

Level
– 5 : R
Tape and Reel Service
– 5 : Commercial
– 5+ : Commercial with B.I.
– 9 : Industrial
– 9+ : Industrial with B.I.
– 2 : Military
– 8 : Military with B.I.
(B.I. = Burn-In)

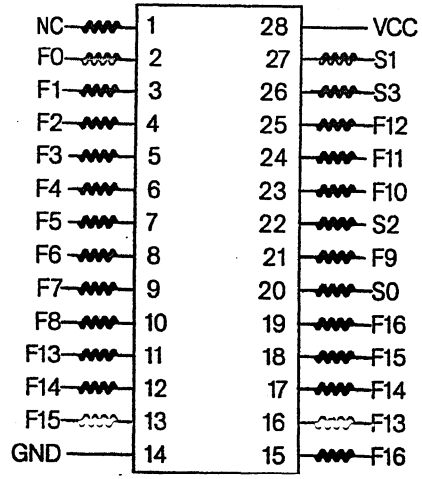
4

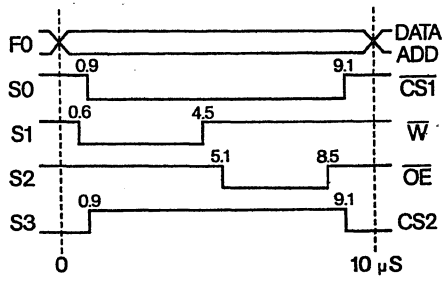
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins : 049
Plastic DIL, 600 mils, 28 pins : 050
SOIC DIL, 300 mils, 28 pins : N10
Ceramic, 300 mils, 28 pins : C31
LCC rectangular, 32 pins : L32

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
FO = 50 KHz ± 20 %

Fn = 1/2 F n-1
S0 to S3 : programmable signals for write / read cycles
NC = Not connected

DATA SHEET

HM 65779

8 K x 9
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  COMMERCIAL : 35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 850 mW (max)
  STANDBY : 125 mW (max)
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

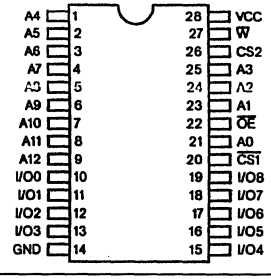
DESCRIPTION

The HM 65779 is a high speed CMOS static RAM organized as 8192 x 9 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 35 ns are available with maximum power consumption of only 850 mW.
The HM 65779 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 68 % when the circuit is deselected. Easy memory expansion is provided by an active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65779 are TTL compatible and operate from a single 5 V supply thus simplifying system design.
The HM-65779 is processed following the test methods of MIL STD 883C.
The HM 65779 is cache memory application oriented. It can be used either as cache disk (RAM disk) or cache memory in the main frame.

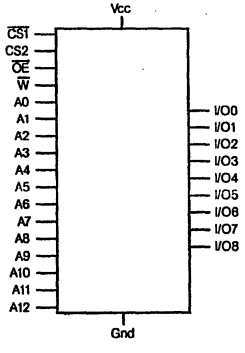
PACKAGES

Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
SOIC 300/330 mils and SOJ 300 mils, 28 pins, DIL.
Tape and Reel Service.

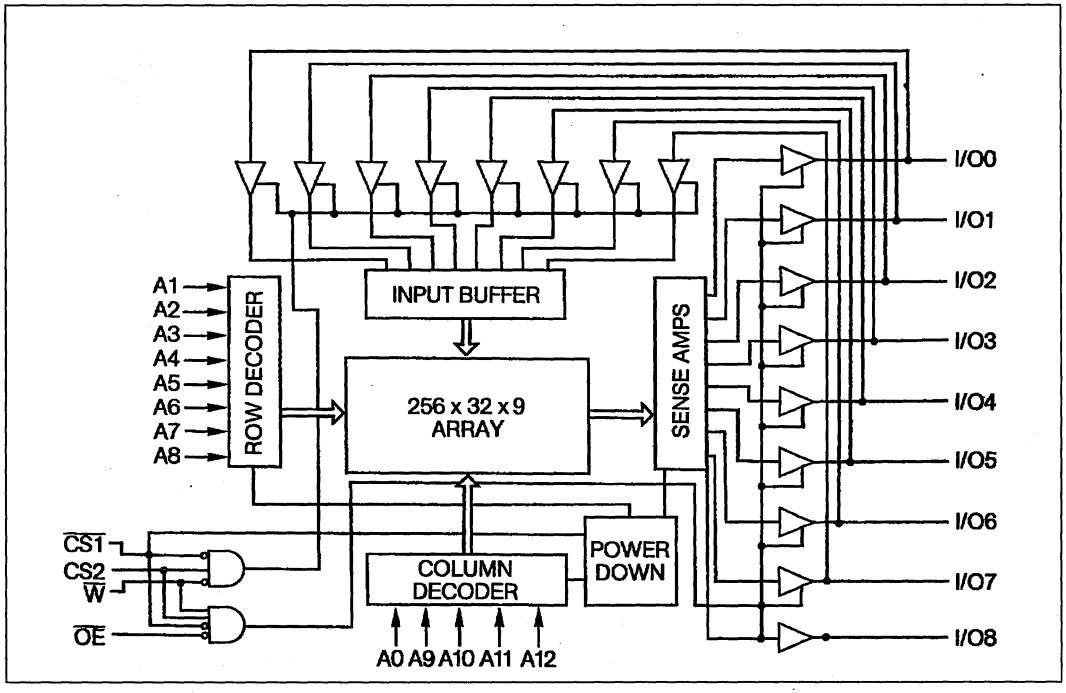
Pinout DIL 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13 : Address inputs	$\overline{CS1}$: Chip Select 1
I/O0-I/O8 : Inputs/Outputs	CS2 : Chip Select 2
VCC : Power	$\overline{OE}$: Output Enable
GND : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect (power down)
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable
X	L	X	X	Z	Z	Deselect

L = low - H = high - X = H or L - Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro Static Discharge voltage > 2000 V (MIL STD 883C method 3015.)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C
Military	(– 2/– 8)	5 V ± 10 %	– 55°C to + 125°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

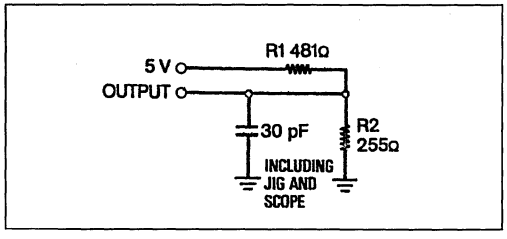


Fig. 1a.

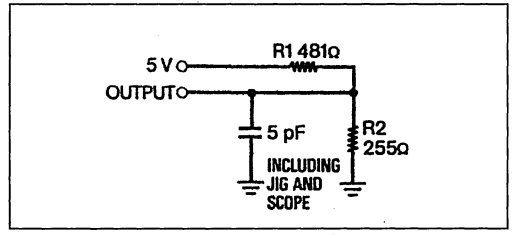
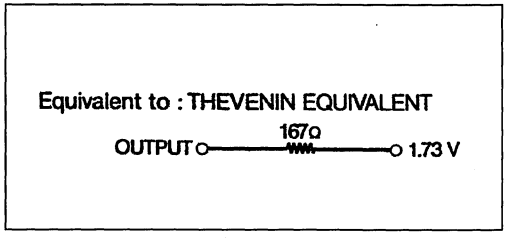


Fig. 1b.



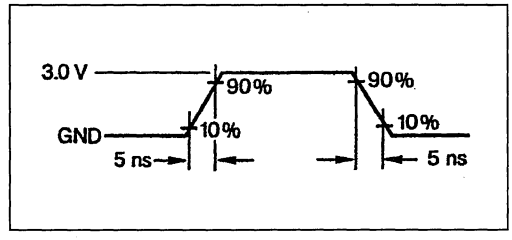


Figure 2 : All Input Pulses.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL		PARAMETER	65779 H-5*	65779 K-5	65779 M-5	65779 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	100	100	100	100	mA	max

Consumption for Military (–2) specification :

SYMBOL		PARAMETER	65779 K-2	65779 M-2	65779 N-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	100	100	100	mA	max

Notes : 6. $\overline{CS1} \geq VIH$, $CS2 \leq VIL$, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to skeep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH : + 30 pF

WRITE CYCLE : Commercial specification

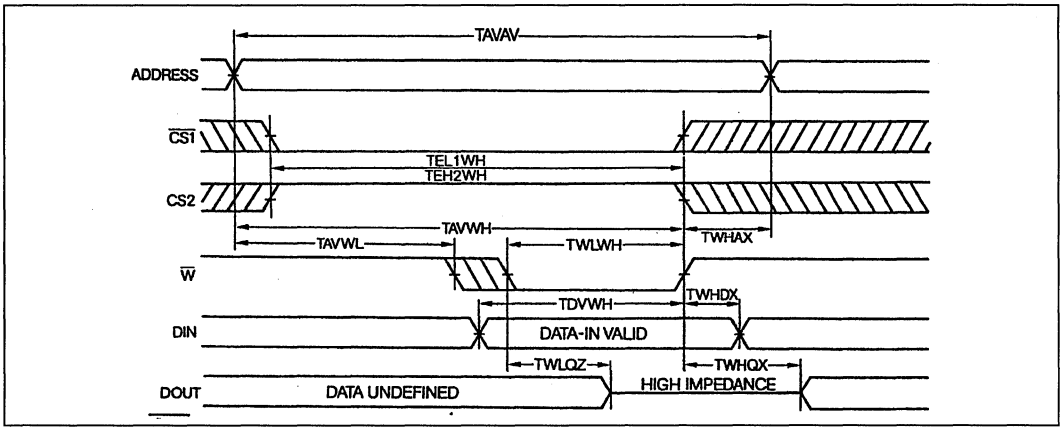
SYMBOL	PARAMETER	65779 H-5*	65779 K-5	65779 M-5	65779 N-5	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	30	ns	min
TEL1WH	$\overline{CS1}$ low to write end	20	30	40	50	ns	min
TEH2WH	CS2 high to write end	20	30	40	50	ns	min
TWLQZ (9)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	35	ns	min
TWHAX	Address hold from end of write	5	5	5	5	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65779 K-2	65779 M-2	65779 N-2	UNIT	VALUE
TAVAV	Write cycle time	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	20	25	30	ns	min
TEL1WH	$\overline{CS1}$ low to write end	30	40	50	ns	min
TEH2WH	CS2 high to write end	30	40	50	ns	min
TWLQZ (9)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	25	30	35	ns	min
TWHAX	Address hold to end of write	5	5	5	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. Tese parameters are sampled and not 100 % tested.

WRITE CYCLE 1 W CONTROLLED (note 10)



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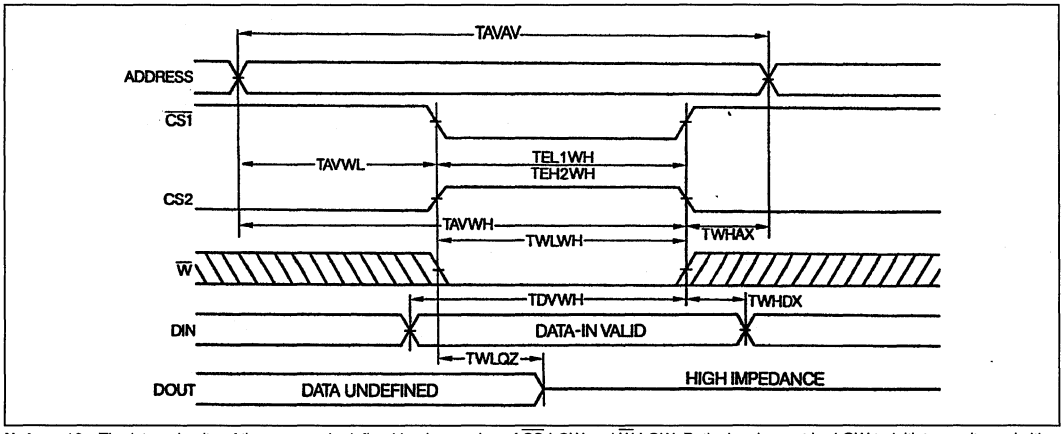
WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 10)



Note : 10. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out is HIGH impedance if $\overline{OE}$ = VIH.

READ CYCLE : Commercial specification

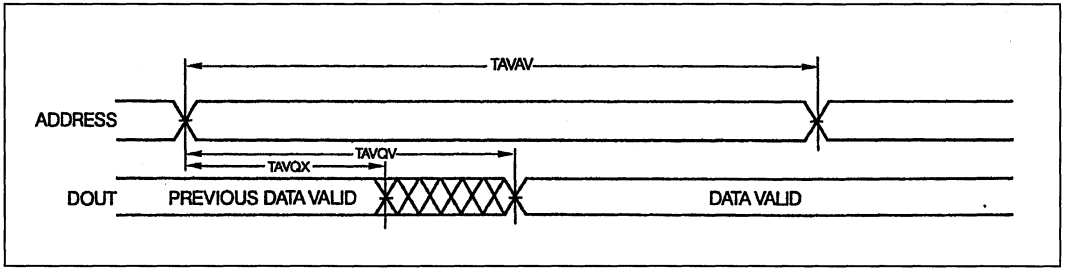
SYMBOL	PARAMETER	65779 H-5*	65779 K-5	65779 M-5	65779 N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	35	45	55	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to low Z	5	5	5	5	ns	min
TEH1QZ(10)	$\overline{CS1}$ high to high Z	20	20	25	25	ns	max
TEL2QZ (10)	CS2 high to high Z	20	20	25	25	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEH1ICCL	$\overline{CS1}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	15	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	20	20	25	30	ns	max

READ CYCLE : Military specification

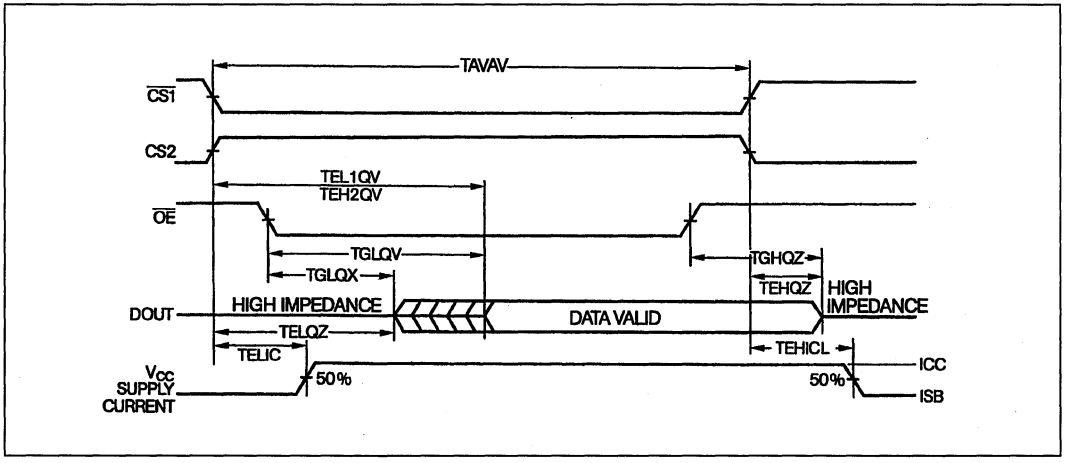
SYMBOL	PARAMETER	65779 K-2	65779 M-2	65779 N-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	35	45	55	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	ns	min
TEH2QX	CS2 high to low Z	5	5	5	ns	min
TEH1QZ(10)	$\overline{CS1}$ high to high Z	20	25	25	ns	max
TEL2QZ (10)	CS2 high to high Z	20	25	25	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	ns	min
TEH1ICCL	$\overline{CS1}$ high to power down	20	25	25	ns	max
TGLQV	Output enable access time	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	20	25	30	ns	max

Note : 10. TEHQZ and TWLQZ are specified with C1 = 5 pF. Transition is measured ± 500 mV from steady state voltage.

READ CYCLE nb 1 (notes 12, 13)



READ CYCLE nb 2 (note 12,14)



Notes : 12. $\overline{w}$ is high for read cycle.
13. Device is continuously selected, $\overline{CS_1}$/$\overline{OE}$, = VIL, CS_2 = VIH.
14. Address valide prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65779	H	– 5 : R

Tape and Reel Service

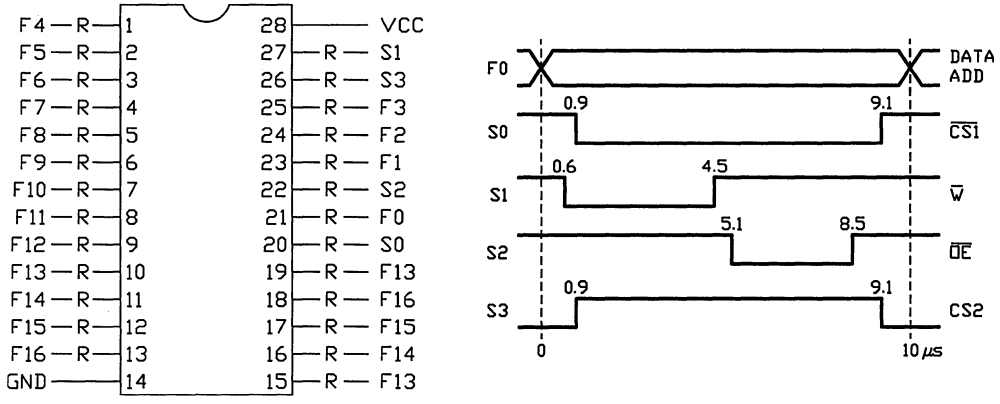
8 k x 9 high speed static RAM

1 - Ceramic 28 pins, 300 mils.
3 - Plastic 28 pins, 300 mils.
T - SO 300 mils, 28 pins.
TP - SO 330 mils, 28 pins.
U - SOJ 300 mils, 28 pins.

H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

– 5 : Commercial
– 5+ : Commercial with B.I.
– 2 : Military
– 8 : Military with B.I.
(B.I. = Burn-In)

BURN-IN SCHEMATICS



VCC = + 5 V (– 0, + 0.5)
R = 1 KΩ per pin
F0 = 50 KHz ± 20 %
Fn = 1/2 Fn – 1
S0 to S3 = Programmable signal for read/write cycles.

DATA SHEET

HM 65756

32 K x 8 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 45//55 ns (max)
  COMMERCIAL : 35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 500 mW (Typ)
  STANDBY : 110 mW (Typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **OUTPUT ENABLE**
- **SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM-65756 is a high speed CMOS static RAM organised as 32,768 X 8 bits. It is manufactured using MHS's high performance CMOS technology.

Access time as fast as 35 ns are available with maximum power consumption of only 550 mW.

The HM-65756 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) an active low output enable ($\overline{OE}$), and three state drivers.

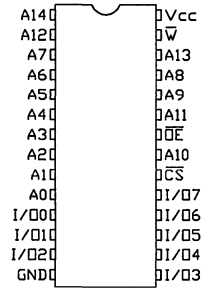
All inputs or outputs of the HM-65756 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65756 is processed following the test methods of MIL STD 883C.

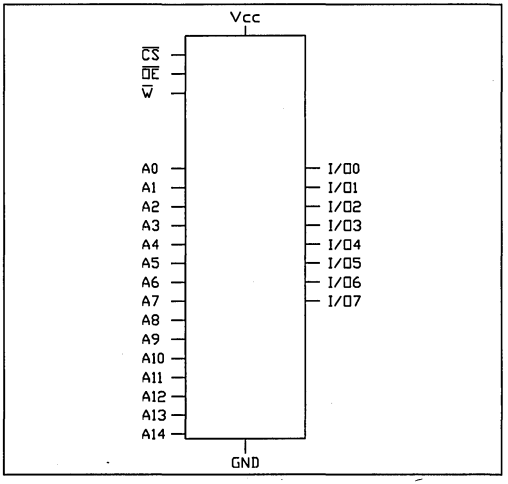
PACKAGES

Plastic 300 and 600 mils, 28 pins, DIL.
Ceramic 300 and 600 mils, 28 pins, DIL.
SO/SOJ 300 and 330 mils, 28 pins, DIL.
LCC 32 pins.
Tape and Reel Service.

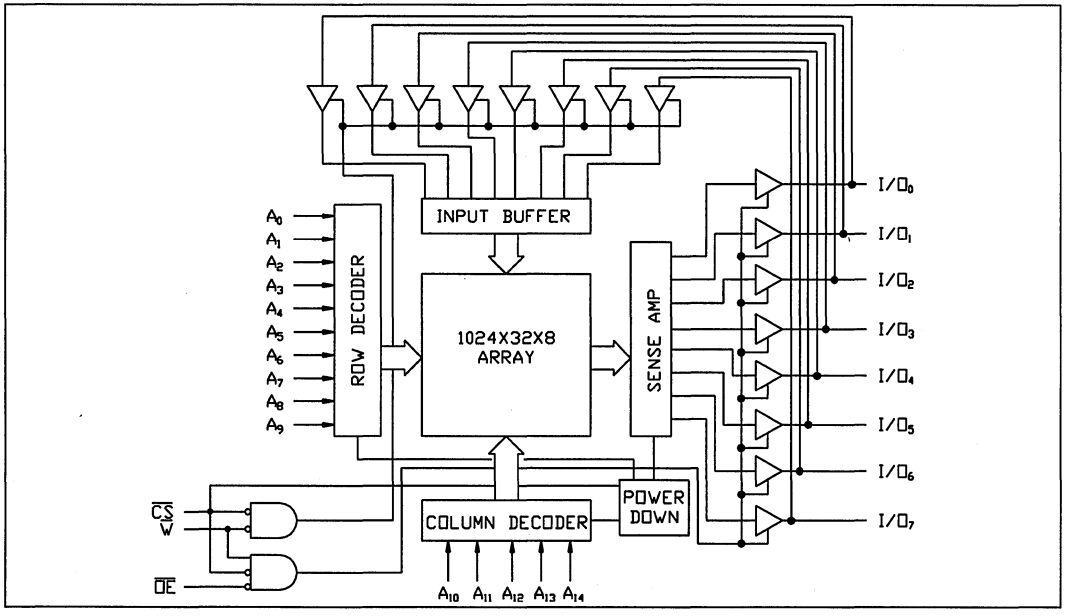
Pinout DIL 28 pins



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A14	: Address inputs	$\overline{CS}$	: Chip Select
I/00-I/07	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	X	L	Valid	Z	Write
L	H	H	Z	Z	Output disable

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
DC output voltage in high Z state .... – 0.5 V to + 7.0 V
Storage temperature ..... – 65°C to + 150°C
Output current into outputs (low) ..... 20 mA
Electro static discharge voltage ..... 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS

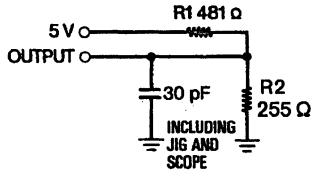


Figure 1a

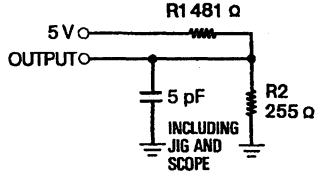


Figure 1b

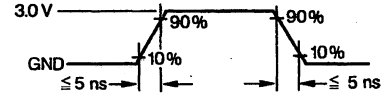
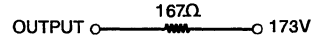


Figure 2

Equivalent to : THEVENIN EQUIVALENT



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65756 K-5	65756 M-5	65756 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	110	110	110	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (- 2) SPECIFICATION :

SYMBOL		PARAMETER	65756 M-9/-2	65756 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	mA	max
ICCOP	(7)	Dynamic operating current	120	120	mA	max

Notes : 6. $\overline{CS} \geq VIH$
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels	Gnd to 3.0 V	Input timing reference levels	1.5 V
Input rise	5 ns	Output loading IOL/IOH (see figure 1a and 1b)	+ 30 pF

WRITE CYCLE : Commercial specification

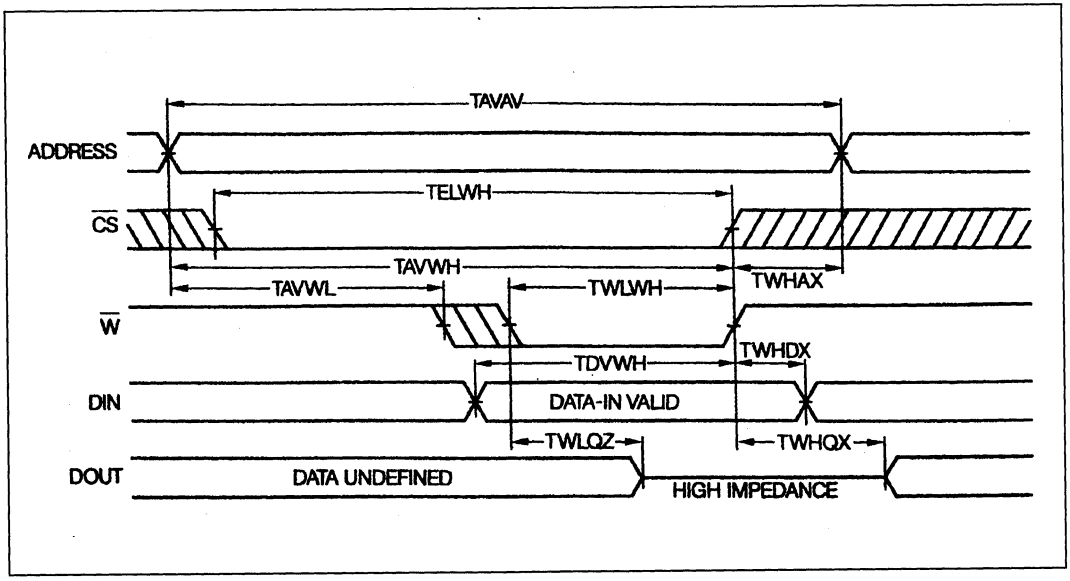
SYMBOL	PARAMETER	65756 K-5	65756 M-5	65756 N-5	UNIT	VALUE
TAVAV	Write cycle time	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address Valid to write end	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	ns	min
TWHAX	Address hold from write end	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

WRITE CYCLE : Industrial and military specifications

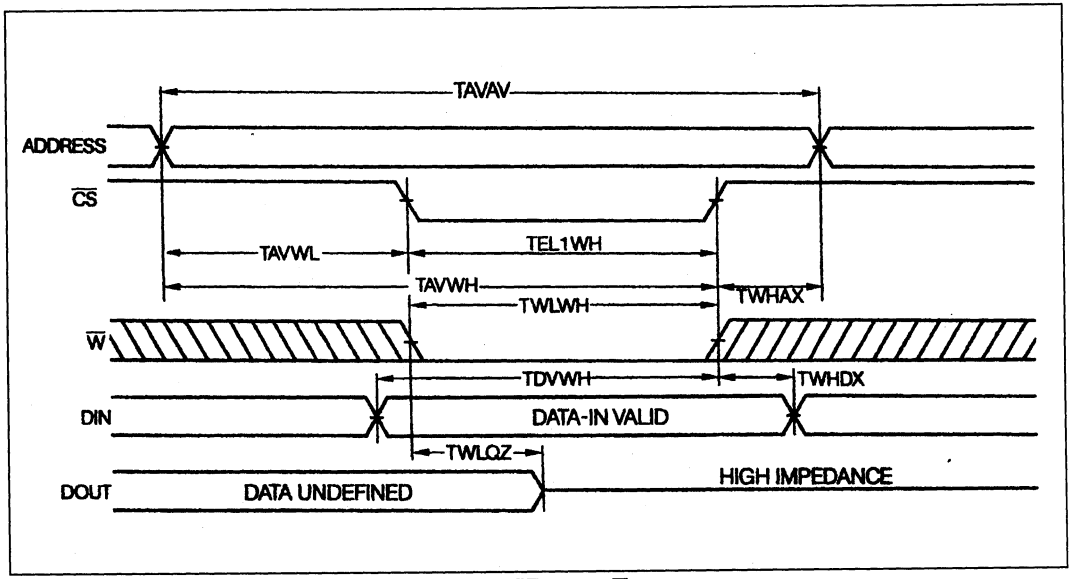
SYMBOL	PARAMETER	65756 M-9/-2	65756 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	45	50	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	40	50	ns	min
TDVWH	Data set-up time	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	40	50	ns	min
TWLQZ (8)	Write low to high Z	20	25	ns	max
TWLWH	Write pulse width	25	30	ns	min
TWHAX	Address hold from write end	2	2	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if $\overline{OE}$ = VIH.

READ CYCLE : Commercial specification

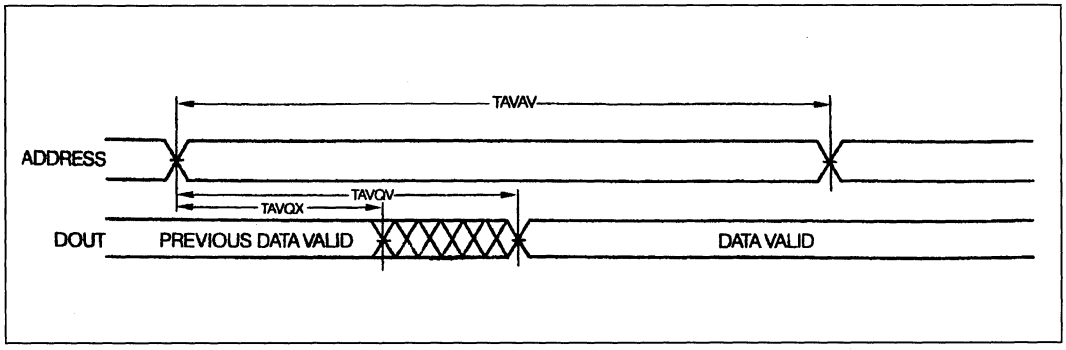
SYMBOL	PARAMETER	65756 K-5	65756 M-5	65756 N-5	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address Valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	25	ns	max
TGLQV	Output enable access time	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	20	25	30	ns	max

READ CYCLE : Industrial and Military specifications

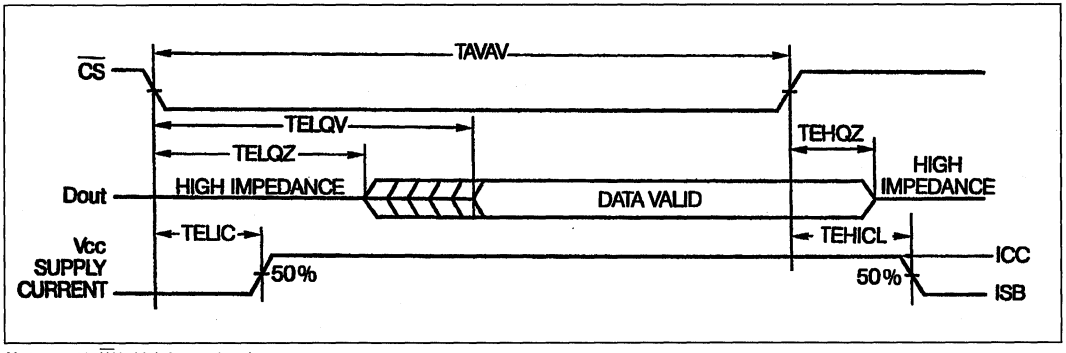
SYMBOL	PARAMETER	65756 M-9/-2	65756 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	45	55	ns	min
TAVQV	Address access time	45	55	ns	max
TAVQX	Address Valid to low Z	3	3	ns	min
TELQV	Chip-select access time	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	20	20	ns	max
TEL1IC	$\overline{CS}$ low to power up	0	0	ns	min
TEH1ICCL	$\overline{CS}$ high to power down	25	25	ns	max
TGLQV	Output enable access time	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	25	30	ns	min

4

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65756	K	– 5 : R
	32 k x 8 high speed static RAM		Tape & Reel Service
0 - Chip form		K = 35 ns	– 5 : Commercial
1 - Ceramic 28 pins 300 mils		M = 45 ns	– 5+ : Commercial with B.I
1E - Ceramic 28 pins 600 mils		N = 55 ns	– 9 : Industrial
3 - Plastic 28 pins 300 mils			– 9+ : Industrial with B.I
3E - Plastic 28 pins 600 mils			– 2 : Military
4 - LCC 32 pins			– 8 : Military with B.I
T - SOIC 28 pins 300 mils			
TP - SOIC 28 pins 330 mils			(B.I : Burn-In)
U - SOJ 28 pins			

DATA SHEET

HM 65797

256 K x 1 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCES TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (Typ)
  STANDBY : 100 mW (Typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM-65797 is a high speed CMOS static RAM organised as 262, 144 X 1 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25ns are available with maximum power consumption of only 330mW.

The HM-65797 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 67 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

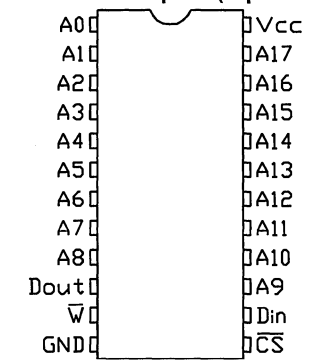
All inputs and outputs of the HM-65797 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65797 is 100 % processed following the test methods of MIL STD 883C.

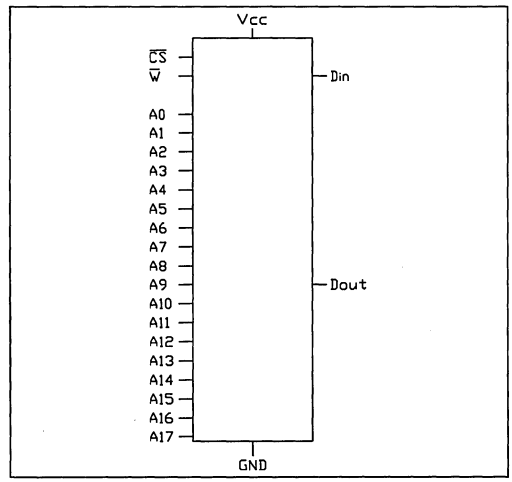
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
SO/SOJ 300 and 330 mils, 24 pins, DIL.
Tape and Reel Service

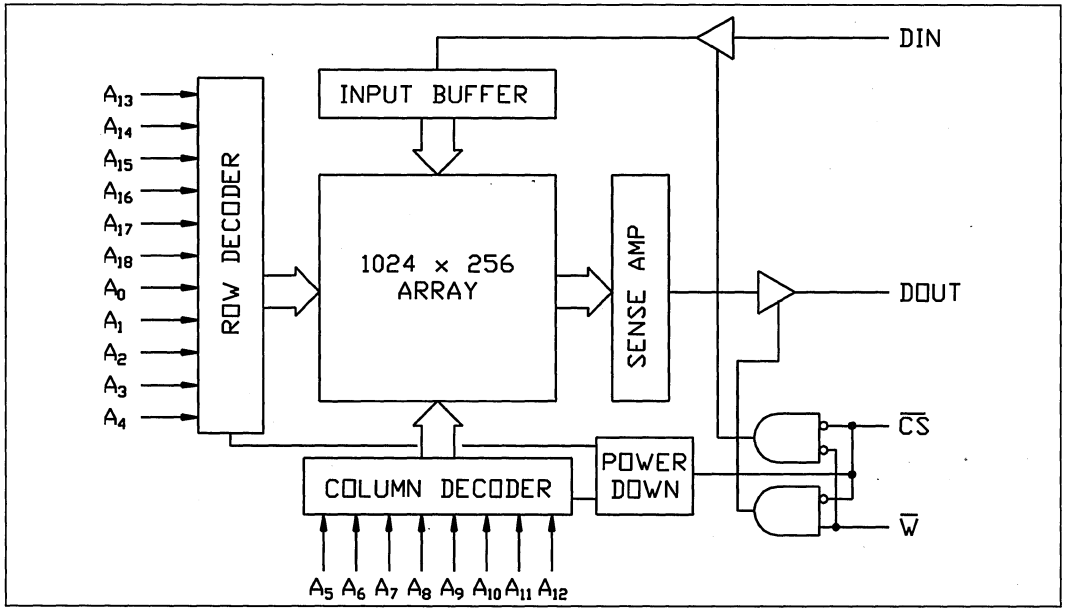
Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A17	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	INPUT/OUTPUTS	MODE
H	X	High Z	Deselect/Power down
L	H	Data Out	Read
L	L	Data In	Write

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
DC output voltage in high Z state..... – 0.5 V to + 7.0 V
Storage temperature..... – 65°C + 150°C
Output current into outputs (low)..... 20 mA
Electro static discharge voltage ..... > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

4

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS

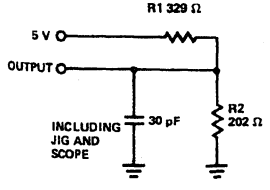


Figure 1a

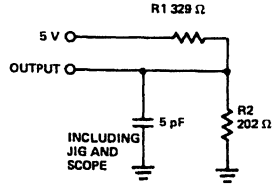


Figure 1b

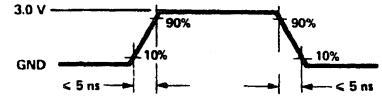
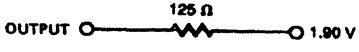
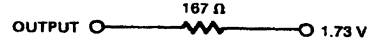


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Commercial



Military

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 50.0	–	50.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA (military), IOL = 12.0 mA (commercial)
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65797 H-5	65797 K-5	65797 M-5	65797 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	70	70	70	70	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (-2) SPECIFICATION :

SYMBOL		PARAMETER	65797 K-9/-2	65797 M-9/-2	65797 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	80	80	80	mA	max

Notes : 6. $\overline{CS} \geq VIH$
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

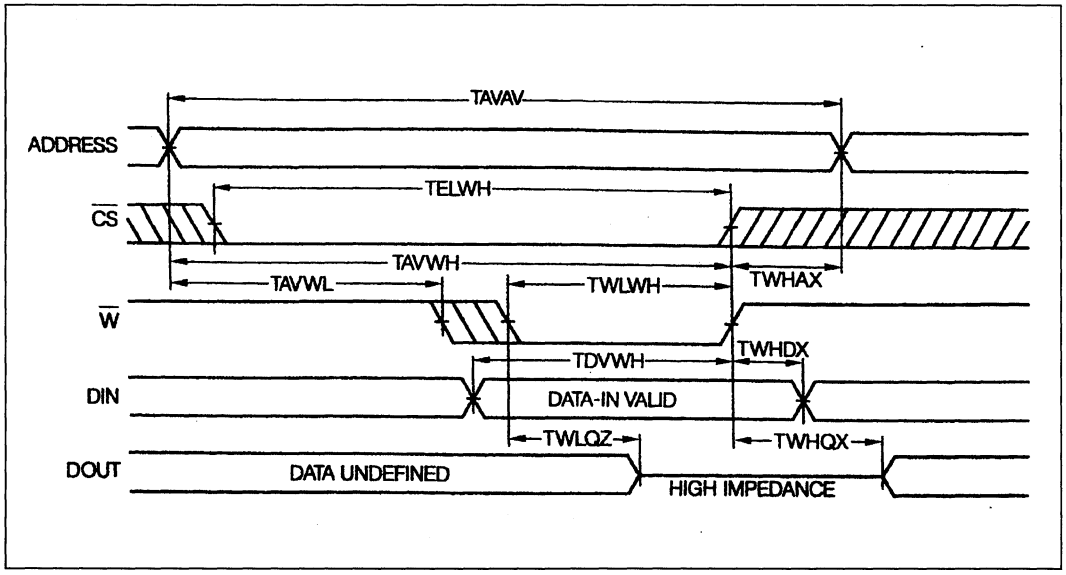
SYMBOL	PARAMETER	65797 H-5	65797 K-5	65797 M-5	65797 N-5	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to write end	20	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	30	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	30	ns	max
TWLWH	Write pulse width	20	25	25	30	ns	min
TWHAX	Address hold from write end	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Industrial and Military specifications

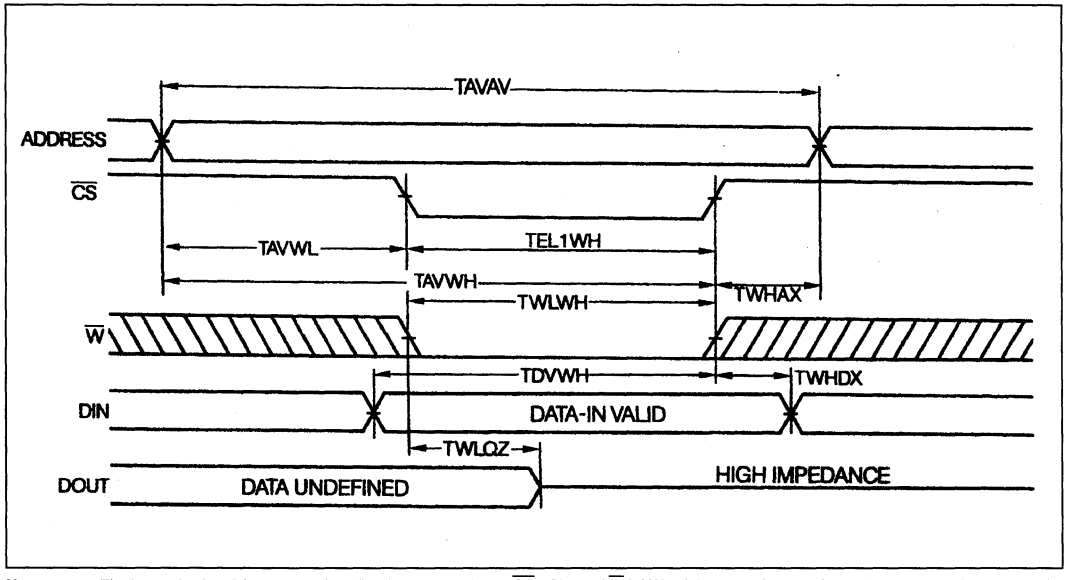
SYMBOL	PARAMETER	65797 K-9/-2	65797 M-9/-2	65797 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	ns	min
TWHAX	Address hold to Write end	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

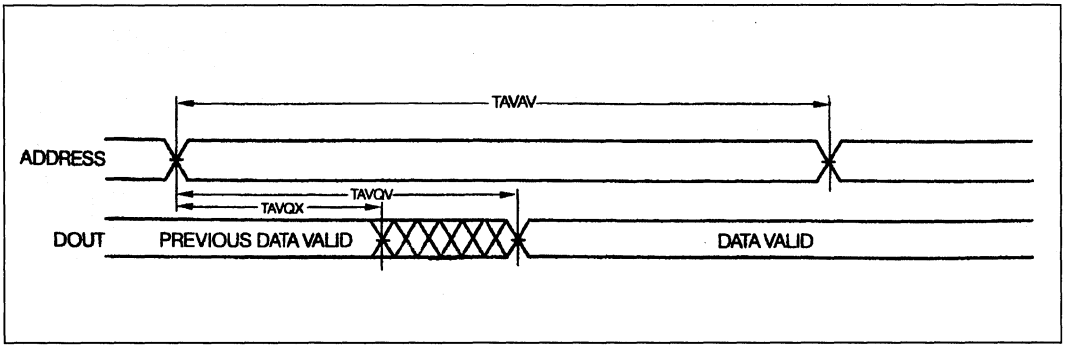
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65797 H-5	65797 K-5	65797 M-5	65797 N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power up	20	25	30	35	ns	max

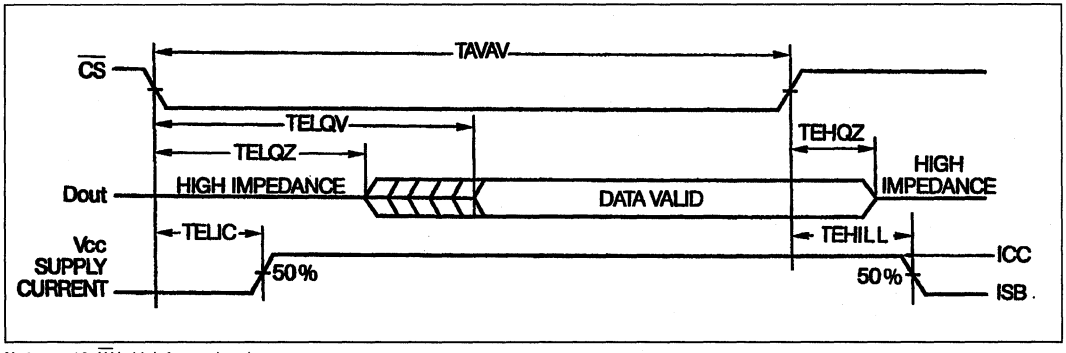
READ CYCLE : Industrial and Military specifications

SYMBOL	PARAMETER	65797 K-9/-2	65797 M-9/-2	65797 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	30	35	ns	max

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65797	H	– 5 : R

– 5 : R — Tape & Reel Service

256 x 1 high speed static RAM

0 - Chip form
1 - Ceramic 24 pins 300 mils
3 - Plastic 24 pins 300 mils
T - SOIC 24 pins 300 mils
TP - SOIC 24 pins 330 mils
U - SOJ 24 pins

H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

– 5 : Commercial
– 5+ : Commercial with B.I
– 9 : Industrial
– 9+ : Industrial with B.I
– 2 : Military
– 8 : Military with B.I

(B.I : Burn In)

DATA SHEET

HM 65798

64 K x 4 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOWER POWER CONSUMPTION**
  ACTIVE : 385 mW (Typ)
  STANDBY : 100 mW (Typ)
- **WIDE TEMPERATURE RANGE :**
  - 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM-65798 is a high speed CMOS static RAM organised as 65,536 X 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW.

The HM-65798 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

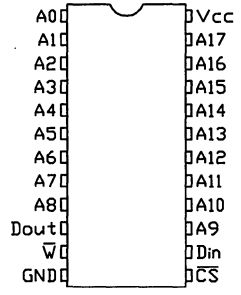
All inputs and outputs of the HM-65798 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65798 is 100 % processed following the test methods of MIL STD 883C.

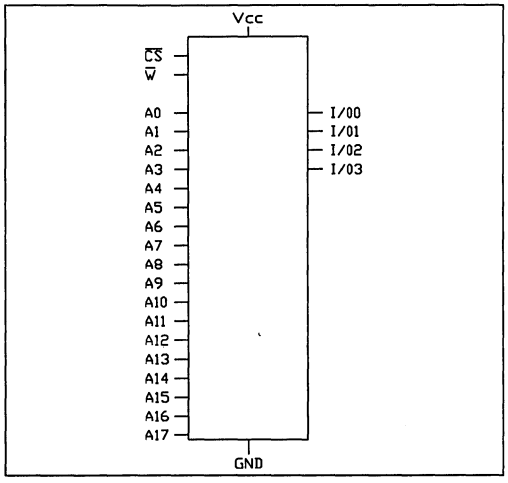
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
SO/SOJ 300 and 330 mils, 24 pins, DIL.
Tape and Reel Service

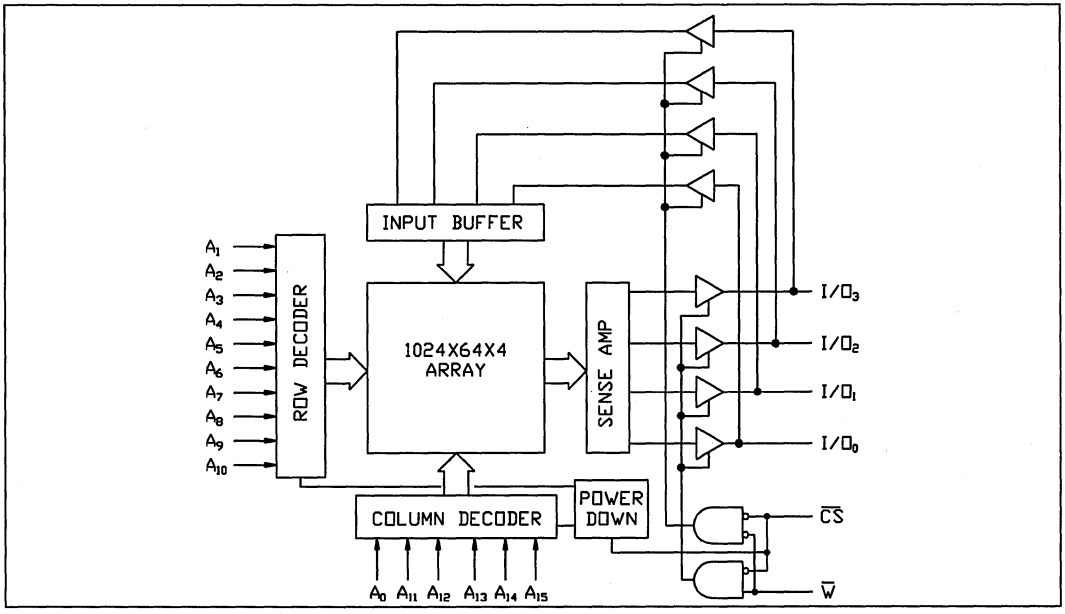
Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A15	: Address inputs	$\overline{W}$	: Write enable
I/00-I/03	: Input/Output	Vcc	: Power
$\overline{CS}$	: Chip Select	GND	: Ground

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	INPUT/OUTPUTS	MODE
H	X	High Z	Deselect/Power down
L	H	Data Out	Read
L	L	Data In	Write

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
CD output voltage in high Z state .... – 0.5 V to + 7.0 V
Storage temperature ..... – 65°C to + 150°C
Output current into outputs (low) 20mA
Electro static discharge voltage ..... > 2000V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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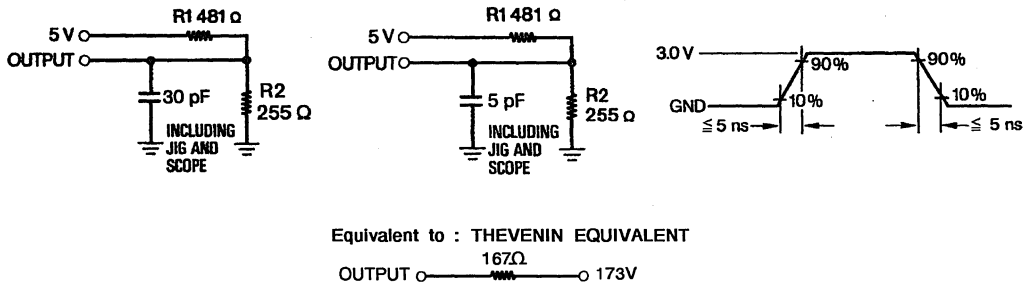
CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65798 H-5	65798 K-5	65798 M-5	65798 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	80	80	80	80	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (-2) SPECIFICATION :

SYMBOL		PARAMETER	65798 K-9/-2	65798 M-9/-2	65798 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	90	90	90	mA	max

Notes : 6. $\overline{CS} \geq VIH$
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels	Gnd to 3.0 V	Input timing reference levels	1.5 V
Input rise	5 ns	Output loading IOL/IOH (see figure 1a and 1b)	+ 30 pF

WRITE CYCLE : Commercial specification

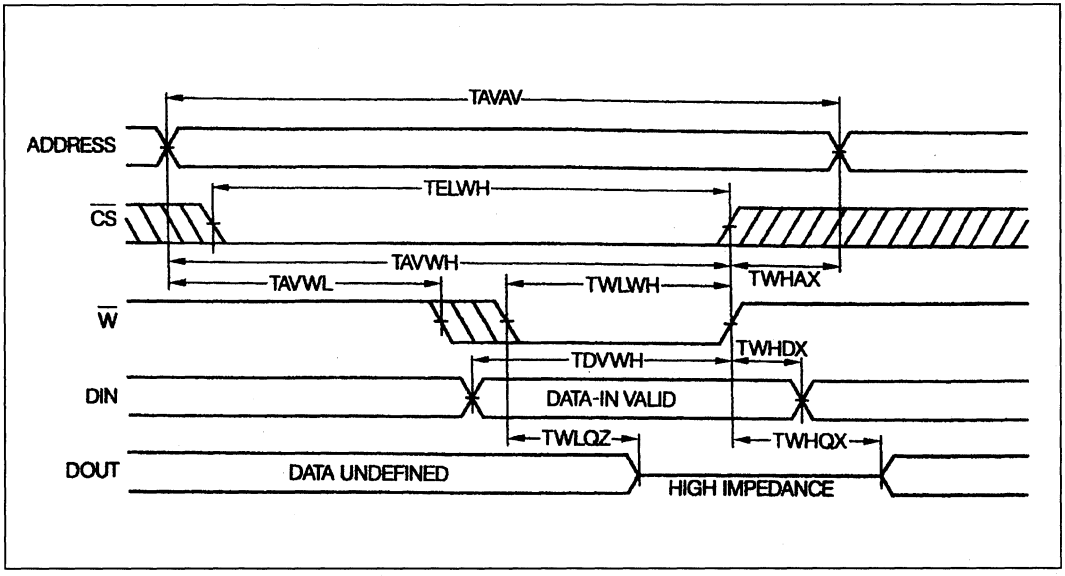
SYMBOL	PARAMETER	65798 H-5	65798 K-5	65798 M-5	65798 N-5	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to write end	20	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	30	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	30	ns	max
TWLWH	Write pulse width	20	25	25	30	ns	min
TWHAX	Address hold from write end	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Industrial and Military specifications

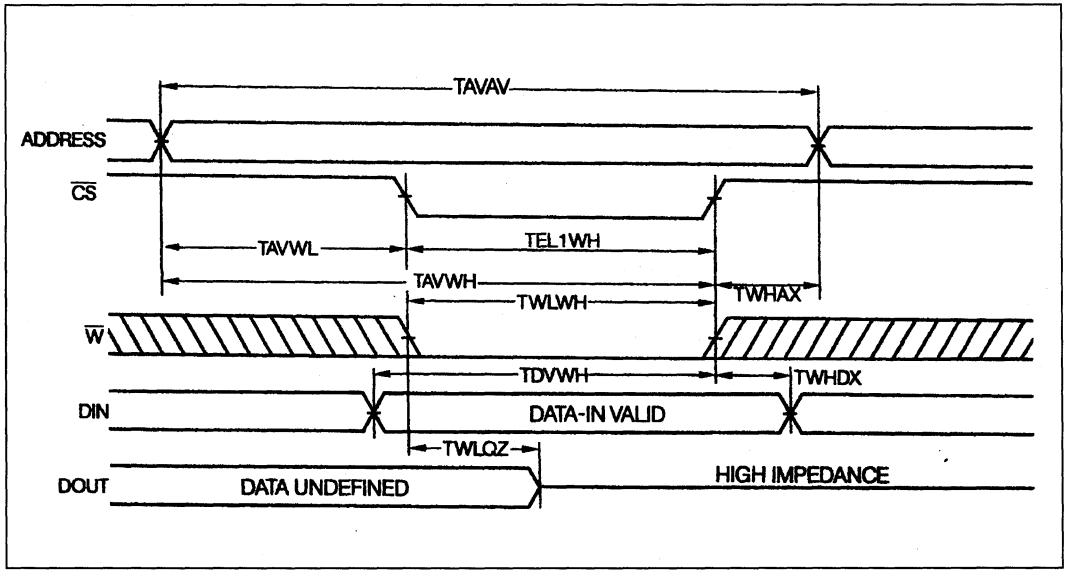
SYMBOL	PARAMETER	65798 K-9/-2	65798 M-9/-2	65798 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	15	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	ns	min
TWHAX	Address hold from Write end	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if $\overline{OE}$ = VIH.

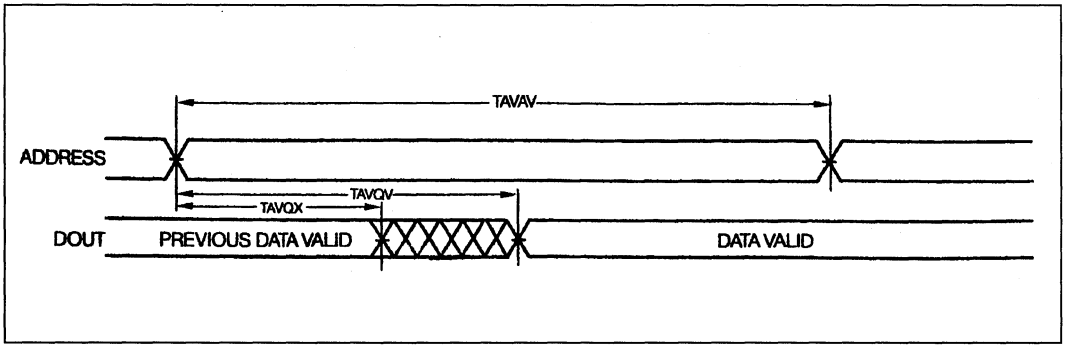
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65798 H-5	65798 K-5	65798 M-5	65798 N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	min
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	35	ns	max

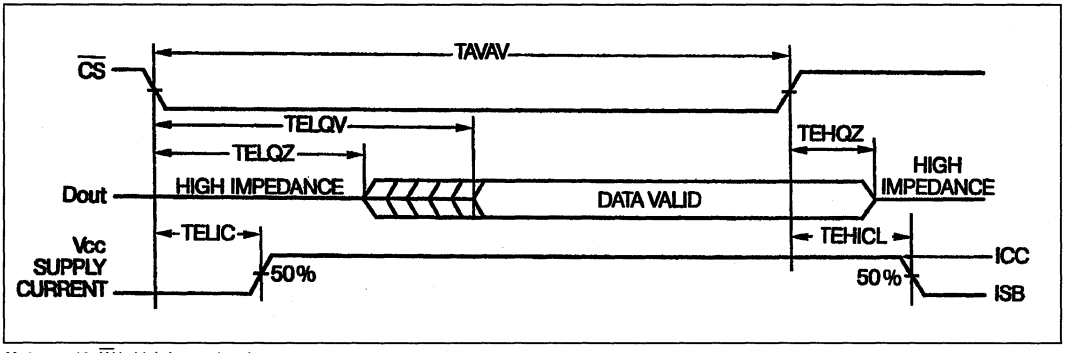
READ CYCLE : Industrial and Military specifications

SYMBOL	PARAMETER	65798 K-9/-2	65798 M-9/-2	65798 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	30	35	ns	max

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65798	H	– 5 : R
	64 k x 4 high speed static RAM		– 5 : Commercial – 5+ : Commercial with B.I – 9 : Industrial – 9+ : Industrial with B.I – 2 : Military – 8 : Military with B.I
0 - Chip form 1 - Ceramic 24 pins 300 mils 3 - Plastic 24 pins 300 mils T - SOIC 24 pins 300 mils TP - SOIC 24 pins 330 mils U - SOJ 24 pins		H = 25 ns K = 35 ns M = 45 ns N = 55 ns	Tape & Reel Service (B.I : Burn-In)

DATA SHEET

HM 65799

64 K x 4 WITH $\overline{OE}$ HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (Typ)
  STANDBY : 100 mW (Typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **OUTPUT ENABLE**
- **SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM-65799 is a high speed CMOS static RAM organised as 65,536 X 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW.

The HM-65799 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip selects ($\overline{CS1}$, $\overline{CS2}$), an active low output enable ($\overline{OE}$) and three state drivers.

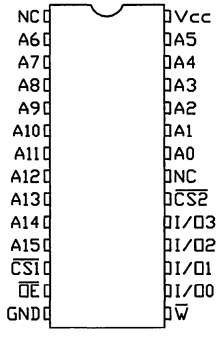
All inputs and outputs of the HM-65799 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65799 is processed following the test methods of MIL STD 883C.

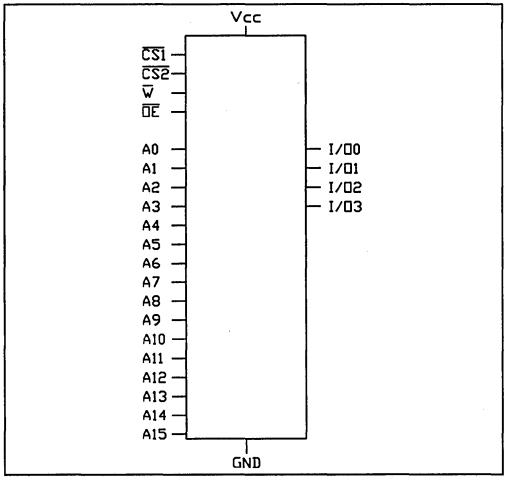
PACKAGES

Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
SO/SOJ 300 and 330 mils, 28 pins, DIL.
Tape and Reel Service

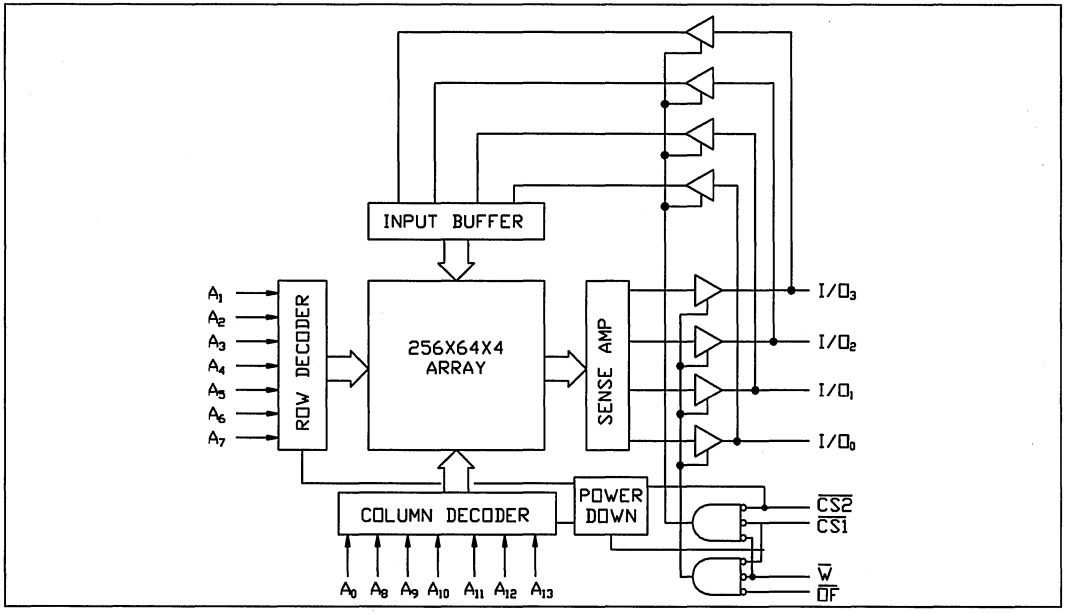
Pinout DIL 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A15	: Address inputs	$\overline{OE}$	: Output Enable
I/00-I/03	: Input/Output	$\overline{W}$	: Write enable
$\overline{CS1}$	: Chip select 1	Vcc	: Power
$\overline{CS2}$	: Chip Select 2	GND	: Ground

TRUTH TABLE

$\overline{CS1}$	$\overline{CS2}$	$\overline{W}$	$\overline{OE}$	INPUT/ OUTPUTS	MODE
H X	X H	X X	X X	High Z	Deselect/Power Down
L	L	H	L	Data Out	Read
L	L	L	X	Data In	Write
L	L	H	H	High Z	Deselect

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
DC output voltage in high Z state..... – 0.5 V to + 7.0 V
Storage temperature..... – 65°C to + 150°C
Output current into outputs (low)..... 20 mA
Electro static discharge voltage ..... > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

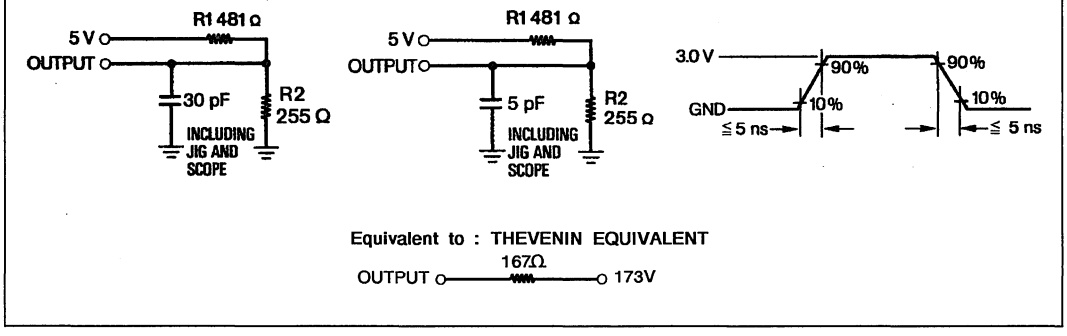
4

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65799 H-5	65799 K-5	65799 M-5	65799 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	80	80	80	80	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (-2) SPECIFICATION :

SYMBOL		PARAMETER	65799 K-9/-2	65799 M-9/-2	65799 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	90	90	90	mA	max

Notes : 6. $\overline{CS} \geq VIH$
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels	Gnd to 3.0 V	Input timing reference levels	1.5 V
Input rise	5 ns	Output loading IOL/IOH (see figure 1a and 1b)	+ 30 pF

WRITE CYCLE : Commercial specification

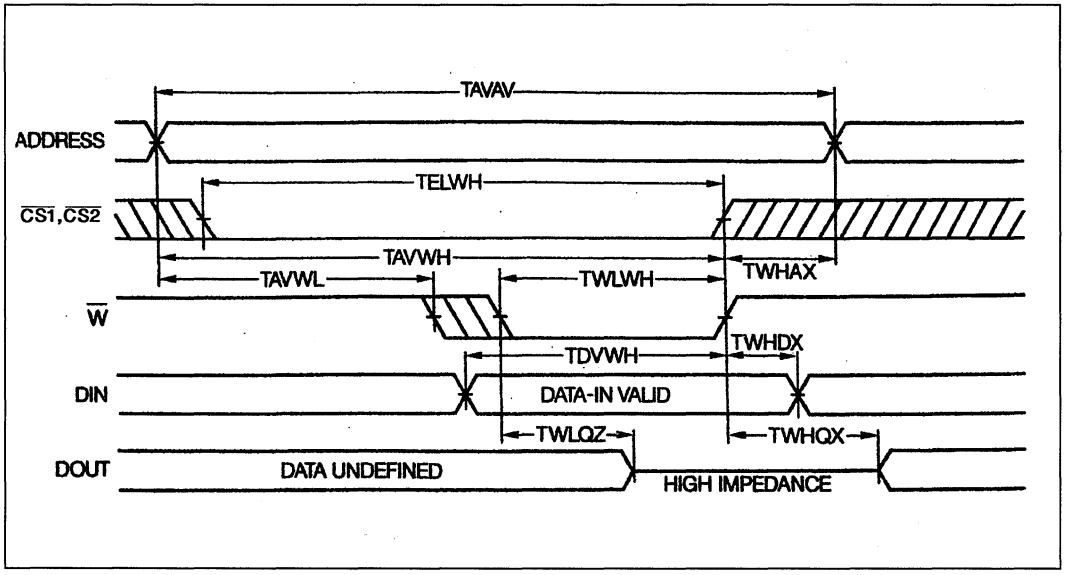
SYMBOL	PARAMETER	65799 H-5	65799 K-5	65799 M-5	65799 N-5	UNIT	VALUE
TAVAV	Write cycle time	20	30	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to write end	20	30	35	40	ns	min
TDVWH	Data set-up time	10	15	20	25	ns	min
TELWH	$\overline{CS1}$, $\overline{CS2}$ low to write end	20	30	35	45	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	20	ns	max
TWLWH	Write pulse width	20	25	35	45	ns	min
TWHAX	Address hold from write end	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

WRITE CYCLE : Industrial and Military specifications

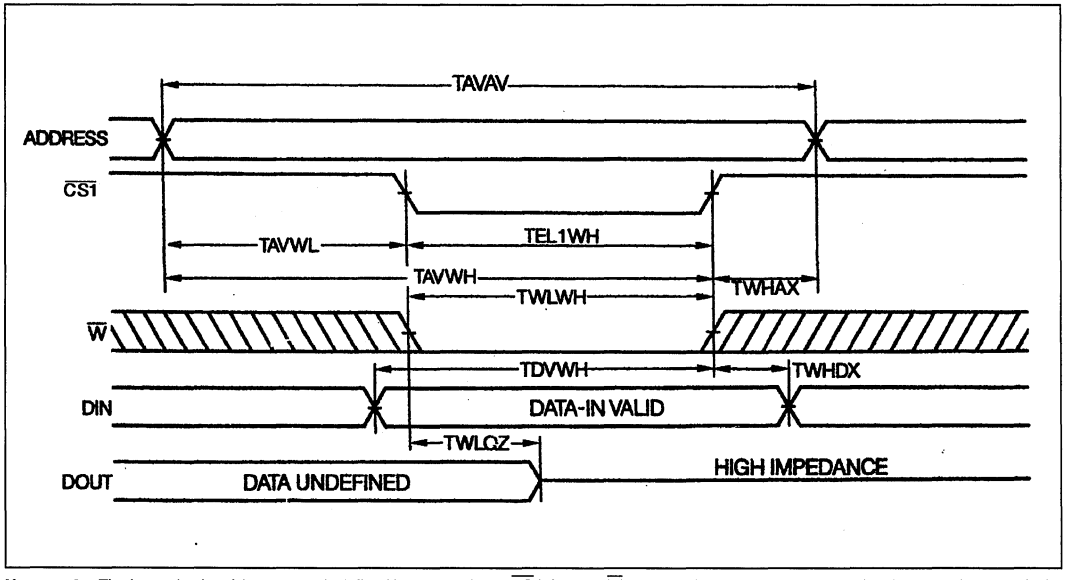
SYMBOL	PARAMETER	65799 K-9/-2	65799 M-9/-2	65799 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	30	40	50	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	35	45	ns	min
TDVWH	Data set-up time	15	20	25	ns	min
TELWH	$\overline{CS1}$, $\overline{CS2}$ low to write end	30	35	45	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	25	35	45	ns	min
TWHAX	Address hold from Write end	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if $\overline{OE}$ = VIH.

READ CYCLE : Commercial specification

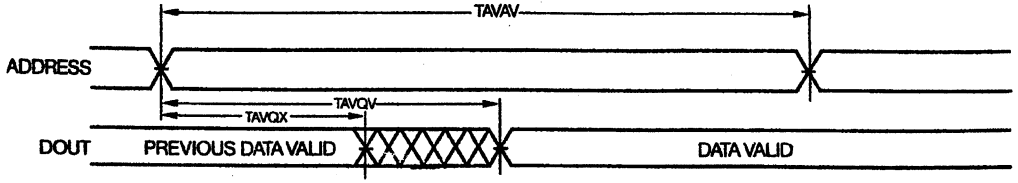
SYMBOL	PARAMETER	65799 H-5	65799 K-5	65799 M-5	65799 N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	min
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	$\overline{CS1}$ and $\overline{CS2}$ access time	25	35	45	55	ns	max
TELQX	$\overline{CS1}$ and $\overline{CS2}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS1}$ and $\overline{CS2}$ high to high Z	15	20	20	20	ns	max
TGLQV	$\overline{OE}$ access time	15	25	35	40	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	35	ns	max

READ CYCLE : Industrial and Military specifications

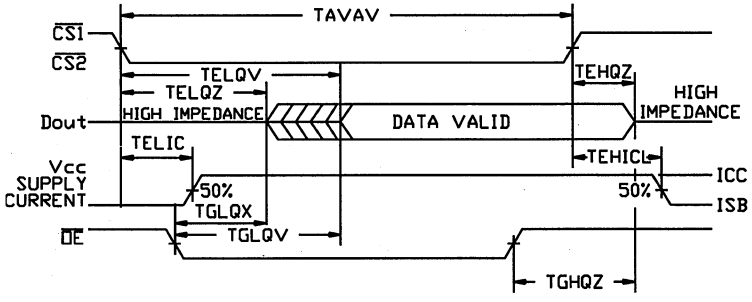
SYMBOL	PARAMETER	65799 K-9/-2	65799 M-9/-2	65799 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	min
TAVQX	Address valid to low Z	3	3	3	ns	min
TELQV	$\overline{CS1}$ and $\overline{CS2}$ access time	35	45	55	ns	min
TELQX	$\overline{CS1}$ and $\overline{CS2}$ low to low Z	3	3	3	ns	min
TEHQZ	$\overline{CS1}$ and $\overline{CS2}$ high to high Z	20	20	20	ns	max
TGLQV	Output Enable access time	25	35	40	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	30	35	ns	max

4

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS1}$ = VIL, $\overline{CS2}$ = VIL, $\overline{OE}$ = VIL
12. Address valid prior or coincident with CS1, CS2 transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65799	H	– 5 : R
	64 k x 4 high speed static RAM with $\overline{OE}$		Tape & Reel Service
0 - Chip form 1 - Ceramic 28 pins 300 mils 3 - Plastic 28 pins 300 mils T - SOIC 28 pins 300 mils TP - SOIC 28 pins 330 mils U - SOJ 28 pins		H = 25 ns K = 35 ns M = 45 ns N = 55 ns	– 5 : Commercial – 5+ : Commercial with B.I – 9 : Industrial – 9+ : Industrial with B.I – 2 : Military – 8 : Military with B.I (B.I : Burn In)

DATA SHEET

HM 65795

64 K x 4 WITH SEPARATE I/O HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (typ)
  STANDBY : 100 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SEPARATE INPUTS/OUTPUTS**
- **SINGLE 5 VOLT SUPPLY**

4

DESCRIPTION

The HM-65795 is a high speed CMOS static RAM organised as 65,536 x 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW.

The HM-65795 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

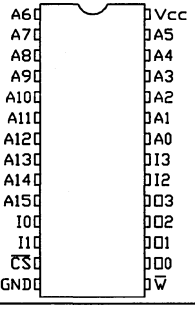
All inputs and outputs of the HM-65795 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65795 is processed following the test methods of MIL STD 883C.

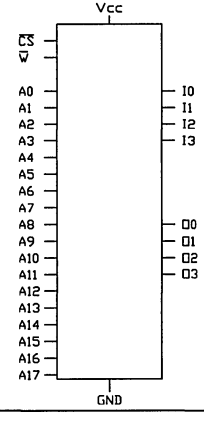
PACKAGES

Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
SO/SOJ 300 and 330 mils, 28 pins, DIL.
Tape and Reel Service

Pinout DIL 28 pins (top view)



LOGIC SYMBOL



DATA SHEET

HM 65796

64 K x 4 WITH SEPARATE I/O HIGH SPEED CMOS SRAM AND TRANSPARENT WRITE

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (typ)
  STANDBY : 100 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SEPARATE INPUTS/OUTPUTS**
- **TRANSPARENT WRITE**
- **SINGLE 5 V SUPPLY**

4

DESCRIPTION

The HM-65796 is a high speed CMOS static RAM organised as 65,536 x 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW

The HM-65796 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

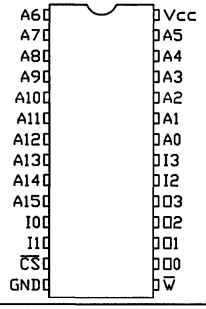
All inputs and outputs of the HM-65796 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65796 is processed following the test methods of MIL STD 883C.

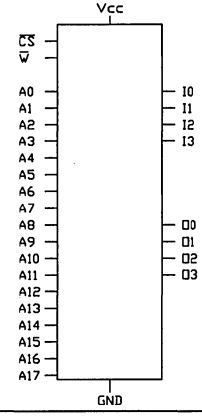
PACKAGES

Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
SO/SOJ 300 and 330 mils, 28 pins, DIL.
Tape and Reel Service

Pinout DIL 28 pins (top view)



LOGIC SYMBOL



ECL SRAM

5

MHS

DATA SHEET

MM10E422/MM100E422

256 x 4 ECL STATIC RAM

FEATURES

- **256 X 4 BITS ORGANIZATION**
- **ULTRA HIGH SPEED/STANDARD POWER**
  - **t_{AA} = 3 ns, t_{ABS} = 2 ns**
  - **I_{EE} = 220 mA**
- **LOW POWER VERSION**
  - **t_{AA} = 5 ns**
  - **I_{EE} = 150 mA**
- **BOTH 10 KH/10 K AND 100 K COMPATIBLE I/O VERSIONS**
- **ON CHIP VOLTAGE COMPENSATION FOR IMPROVED NOISE MARGIN**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **INDUSTRY STANDARD PINOUT**

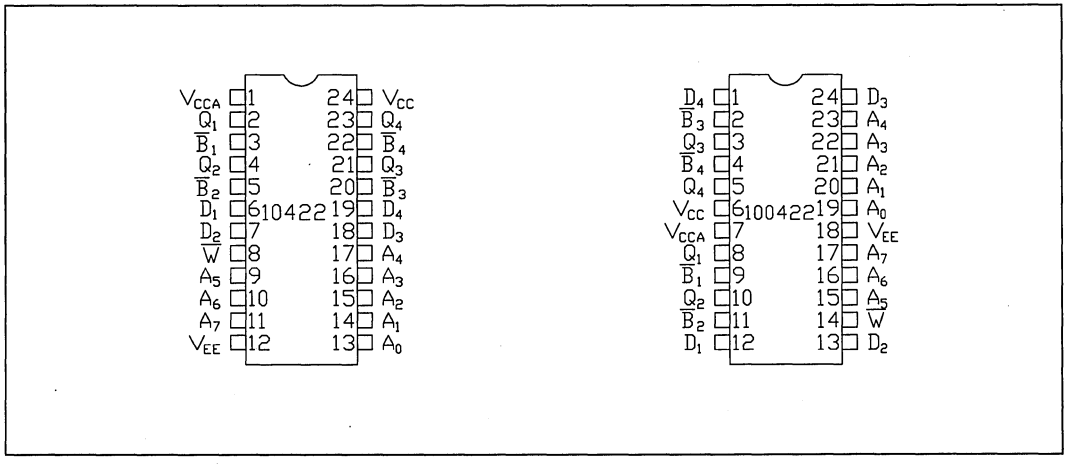
5

DESCRIPTION

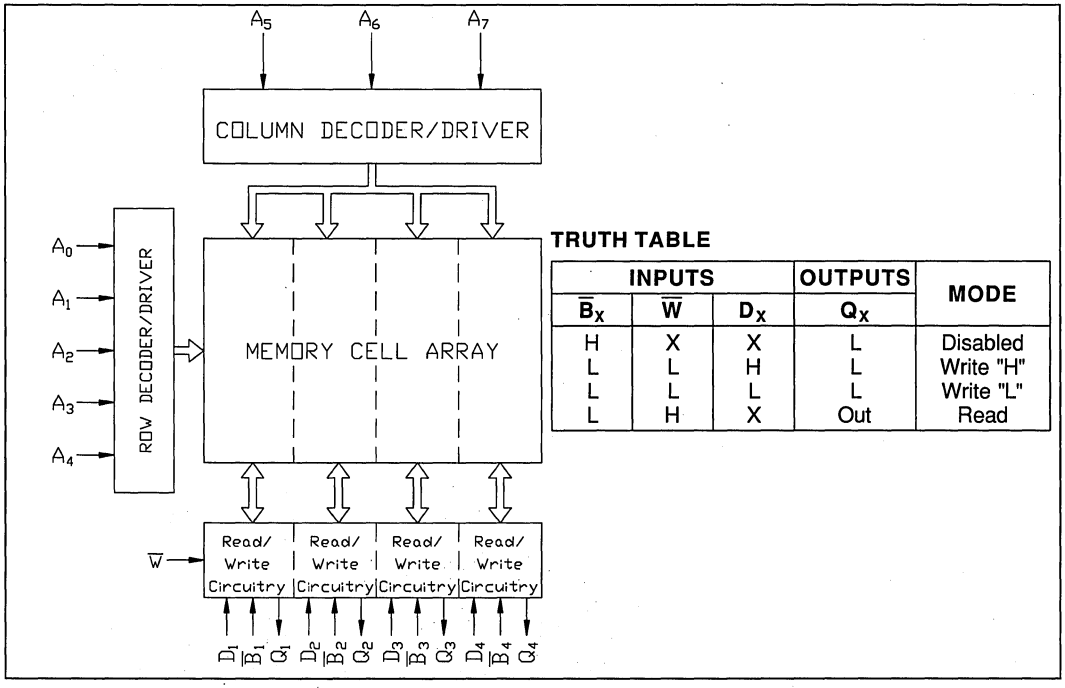
The MHS MM10E422 and MM100E422 are 256 x 4 ECL RAMs designed for scratch pad, control and Buffer Storage applications. These RAMs are developed by Aspen Semiconductor Corporation. Both parts are fully decoded random access memories organized as 256 words by 4 bits. The CY10E422 is 10 KH/10 K compatible. The MM100E422 is 100 K compatible.

The four independent active LOW block select ($\overline{B}$) inputs control memory selection and allow for memory expansion and reconfiguration. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{B}_x$ LOW, the corresponding data at D_x is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{B}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand or reconfigure the memory.

PIN CONFIGURATIONS



LOGIC BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	MODE
$\overline{B}_X$	$\overline{W}$	D_X	Q_X	
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	Out	Read

5

SELECTION GUIDE

		10E422-3 100E422-3	10E422-5 100E422-5	10E422-7 100E422-7
Maximum Access Time (ns)		3	5	7
I_{EE} Max. (mA)	Commercial	220	220	
	"L" (Low Power)		150	150

MAXIMUM RATINGS

Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage V_{EE} to V_{CC} ..... – 7.0 to + 0.5 V

Input Voltage ..... V_{EE} to + 0.5 V

Output Current ..... 50 mA

OPERATING RANGE referenced to V_{CC}

RANGE	I/O	AMBIENT TEMPERATURE	V_{EE}
Commercial (Standard, "L")	10KH/ 10K	0°C to 75°C	– 5.2 V ± 5 %
Commercial (Standard, "L")	100K	0°C to 85°C	– 4.5 V ± 0.3 V

ELECTRICAL CHARACTERISTICS

PARAMETERS	DESCRIPTION	TEST CONDITIONS	TEMPERATURE[1]	MIN.	MAX.	UNIT
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50 Ω to – 2 V V_{EE} = – 5.2 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	– 1000	– 840	mV
			T_A = + 25°C	– 960	– 810	mV
			T_A = + 75°C	– 900	– 735	mV
		100K R_L = 50 Ω to – 2 V V_{EE} = – 4.5 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	– 1025	– 880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50 Ω to – 2 V V_{EE} = – 5.2 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	– 1870	– 1665	mV
			T_A = + 25°C	– 1850	– 1650	mV
			T_A = + 75°C	– 1830	– 1625	mV
		100K R_L = 50 Ω to – 2 V V_{EE} = – 4.5 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	– 1810	– 1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = – 5.2 V	T_A = 0°C	– 1170	– 840	mV
			T_A = + 25°C	– 1130	– 810	mV
			T_A = + 75°C	– 1070	– 720	mV
		100K V_{EE} = – 4.5 V	T_A = 0°C to 85°C	– 1165	– 880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = – 5.2 V	T_A = 0°C	– 1950	– 1480	mV
			T_A = + 25°C	– 1950	– 1480	mV
			T_A = + 75°C	– 1950	– 1450	mV
		100K V_{EE} = – 4.5 V	T_A = 0°C to 85°C	– 1810	– 1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{B}$ inputs	0.5	170	µA
			All other inputs	– 50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial "L" (Low Power)			– 150	mA
		Commercial Standard			– 220	mA

Notes : 1. Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.
2. 10E specifications support both 10 K and 10 KH compatibility.

CAPACITANCE [3]

PARAMETERS	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance		4	10	pF
C_{OUT}	Output Capacitance		6	12	pF

Notes : 3. Tested initially and after any design or process changes that may affect these parameters.

AC TEST LOADS AND WAVEFORMS (5, 6, 7, 8, 9, 10)

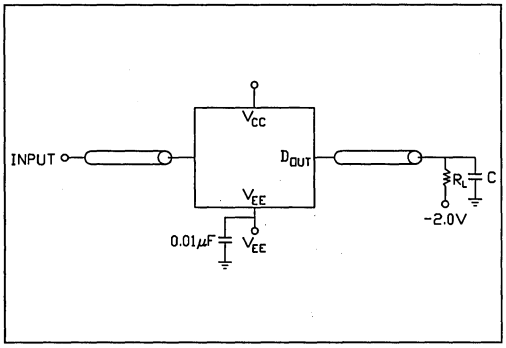


Figure 1.

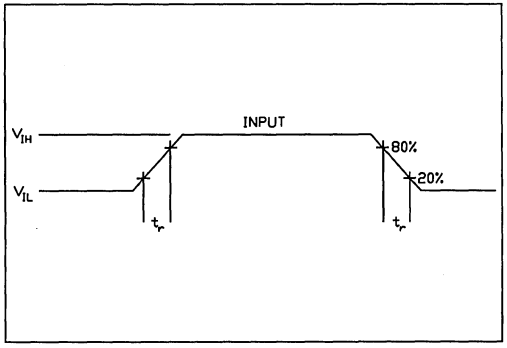


Figure 2.

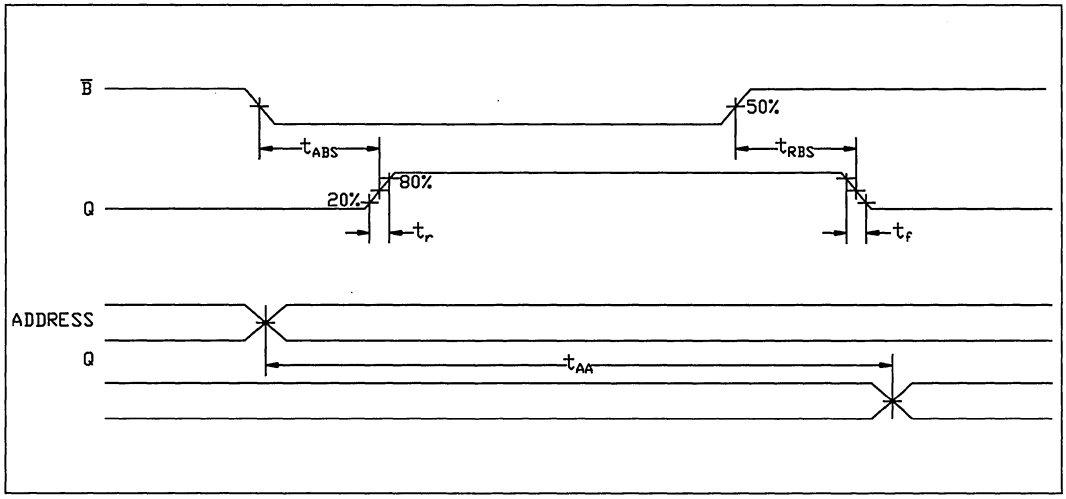
Notes :
5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = – 1.7 V, V_{IH} = – 0.9 V on 100 K version.
7. R_L = 50 Ω, C < 5 pF (3 ns grade) or < 30 pF (5, 7 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be 50 Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. t_r = t_f = 0.7 ns.
10. All timing measurements are made from the 50 % point of all waveforms.

5

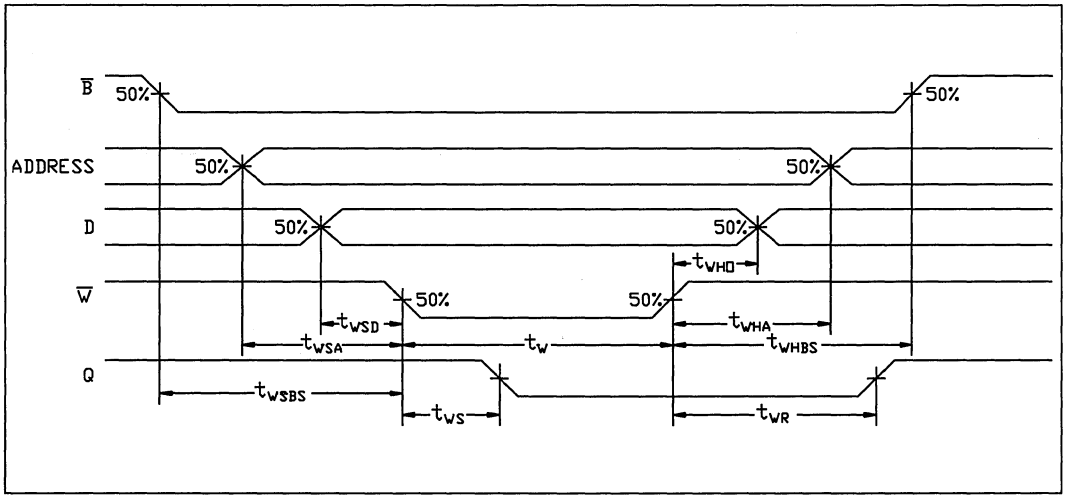
SWITCHING CHARACTERISTICS Over Operating Range

PARAMETERS	DESCRIPTION	10E422-3 100E422-3		10E422-5 100E422-5		10E422-7 100E422-7		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ABS}	Block Select to Output Delay		2.0		3.0		4.0	ns
t_{RBS}	Block Select Recovery		2.0		3.0		4.0	ns
t_{AA}	Address Access Time		3.0		5.0		7.0	ns
t_W	Write Pulse Width	3.0		3.0		5.0		ns
t_{WSD}	Data Setup to Write	0.5		1.0		1.0		ns
t_{WHD}	Data Hold to Write	0.5		1.0		1.0		ns
t_{WSA}	Address Setup/Write	0.5		1.0		1.0		ns
t_{WHA}	Address Hold/Write	0.5		1.0		1.0		ns
t_{WSBS}	Block Select Setup/Write	0.5		1.0		1.0		ns
t_{WHBS}	Block Select Hold/Write	0.5		1.0		1.0		ns
t_{WS}	Write Disable		2.0		3.0		4.0	ns
t_{WR}	Write Recovery		3.5		6.0		8.0	ns
t_r	Output Rise Time	0.7	1.5	0.7	2.5	1.0	2.5	ns
t_f	Output Fall Time	0.7	1.5	0.7	2.5	1.0	2.5	ns

SWITCHING WAVEFORMS



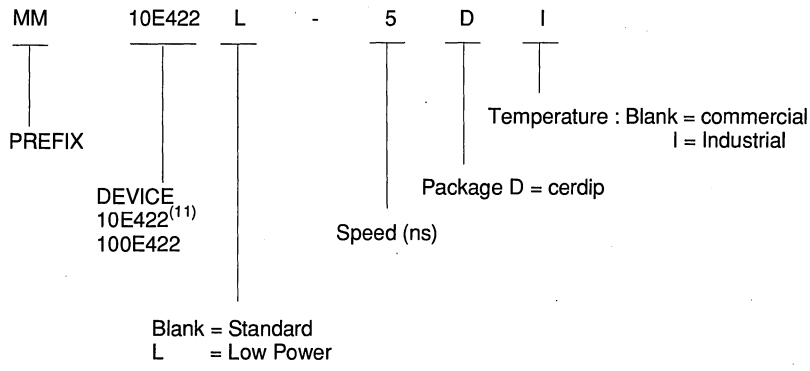
Read Mode



Write Mode

5

ORDERING INFORMATION

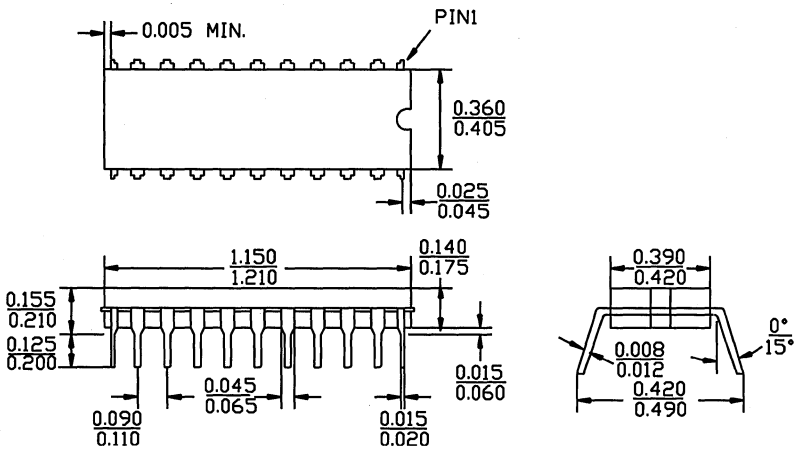


Note : 11. 10E specifications support both 10 K and 10 KH compatibility.

5

PACKAGE DIAGRAMS

24 LEAD (400 MIL) CERDIP



INCH Dimension

DATA SHEET

MM10E474/MM100E474

1024 x 4 ECL STATIC RAM

FEATURES

- **1024 x 4 BITS ORGANIZATION**
- **ULTRA HIGH SPEED/STANDARD POWER**
  - **t_{AA} = 3 ns, t_{ACS} = 2 ns**
  - **I_{EE} = 275 mA**
- **LOW POWER VERSION**
  - **t_{AA} = 5 ns**
  - **I_{EE} = 190 mA**
- **BOTH 10 KH/10 K AND 100 K COMPATIBLE I/O VERSIONS**
- **ON CHIP VOLTAGE COMPENSATION FOR IMPROVED NOISE MARGIN**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **INDUSTRY STANDARD PINOUT**

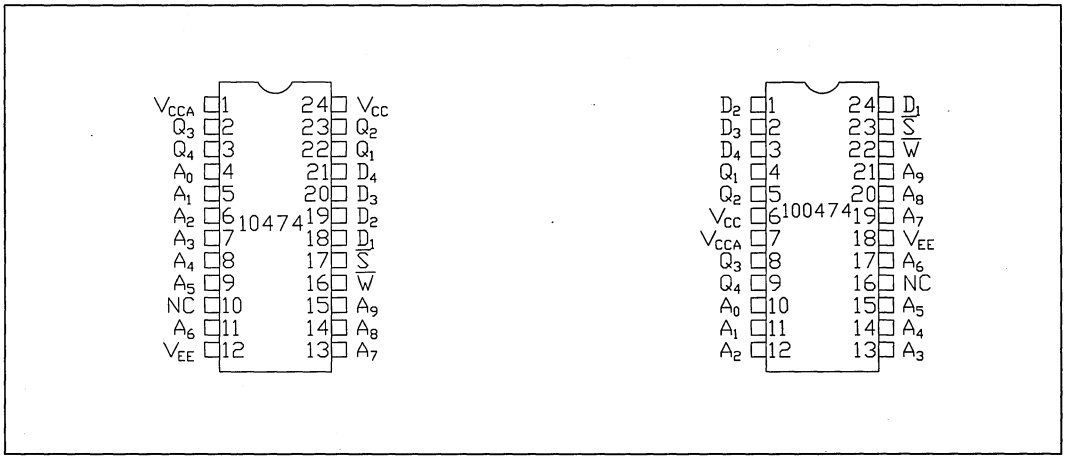
5

DESCRIPTION

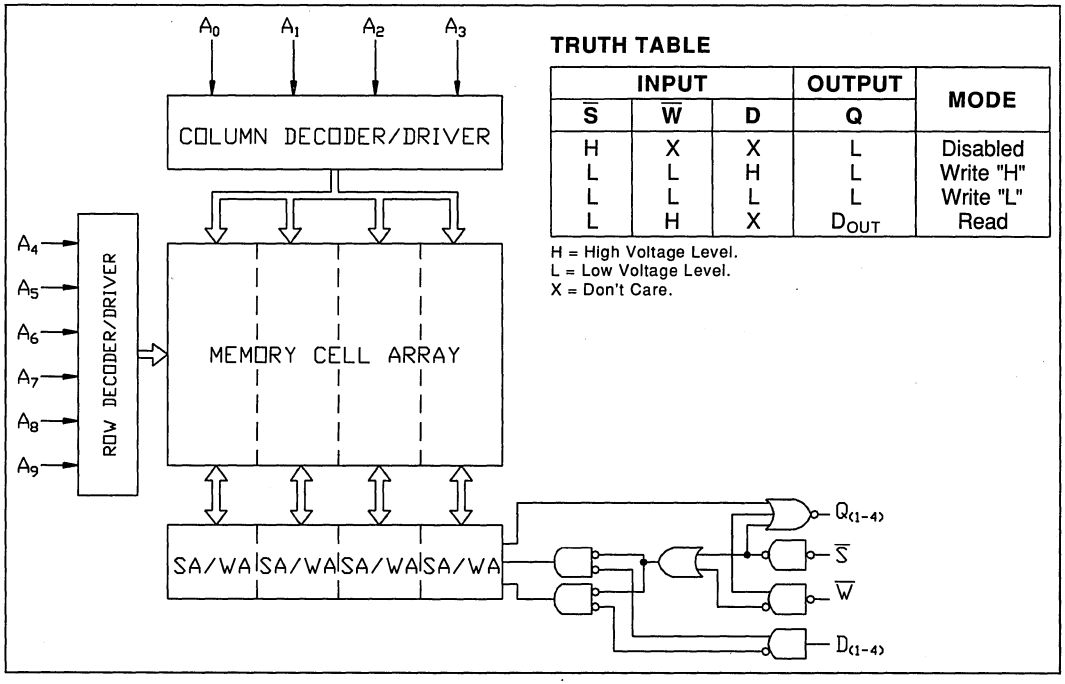
The MHS MM10E474 and MM100E474 are 1 K x 4 ECL RAMs designed for scratch pad, control and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation. Both parts are fully decoded random access memories organized as 1024 words by 4 bits. The MM10E474 is 10 KH/10 K compatible. The MM100E474 is 100 K compatible.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at D(1-4) is written into the addressed location. To read $\overline{W}$ is held HIGH, while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

PIN CONFIGURATIONS



LOGIC BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D	Q	
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level.
L = Low Voltage Level.
X = Don't Care.

5

SELECTION GUIDE

		10E474-3 100E474-3	10E474-5 100E474-5	10E474-7 100E474-7
Maximum Access Time (ns)		3	5	7
I_{EE} Max. (mA)	Commercial	−275	−275	
	"L"		−190	−190

MAXIMUM RATINGS

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... −7.0 to +0.5 V

Input Voltage ..... VEE to +0.5 V

Output Current ..... −50 mA

OPERATING RANGE referenced to V_{CC}

RANGE	I/O	AMBIENT TEMPERATURE	V_{EE}
Commercial (Standard, "L")	10KH/ 10K	0°C to 75°C	−5.2 V ±5 %
Commercial (Standard, "L")	100K	0°C to 85°C	−4.5 V ±0.3 V

ELECTRICAL CHARACTERISTICS

PARAMETERS	DESCRIPTION	TEST CONDITIONS	TEMPERATURE(1)	MIN.	MAX.	UNIT
V_{OH}	Output HIGH Voltage	10E(2) R_L = 50 Ω to – 2 V V_{EE} = – 5.2 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	– 1000	– 840	mV
			T_A = + 25°C	– 960	– 810	mV
			T_A = + 75°C	– 900	– 735	mV
		100K R_L = 50 Ω to – 2 V V_{EE} = –4.5 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	– 1025	– 880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50 Ω to – 2 V V_{EE} = – 5.2 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	– 1870	– 1665	mV
			T_A = + 25°C	– 1850	– 1650	mV
			T_A = + 75°C	– 1830	– 1625	mV
		100K R_L = 50 Ω to – 2 V V_{EE} = – 4.5 V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	– 1810	– 1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = – 5.2 V	T_A = 0°C	– 1170	– 840	mV
			T_A = + 25°C	– 1130	– 810	mV
			T_A = + 75°C	– 1070	– 720	mV
		100K V_{EE} = – 4.5 V	T_A = 0°C to 85°C	– 1165	– 880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = – 5.2 V	T_A = 0°C	– 1950	– 1480	mV
			T_A = + 25°C	– 1950	– 1475	mV
			T_A = + 75°C	– 1950	– 1450	mV
		100K V_{EE} = – 4.5 V	T_A = 0°C to 85°C	– 1810	– 1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	– 50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial "L" (Low Power)		– 190		mA
		Commercial Standard		– 275		mA

Notes : 1. Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.
2. 10E specifications support both 10 K and 10 KH compatibility.

CAPACITANCE (3)

PARAMETERS	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Pin Capacitance		4	10	pF
C_{OUT}	Output Pin Capacitance		6	12	pF

Notes : 3. Tested initially and after any design or process changes that may affect these parameters.

AC TEST LOADS AND WAVEFORMS (5, 6, 7, 8, 9, 10)

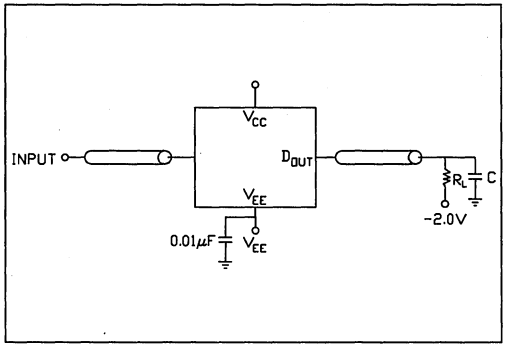


Figure 1.

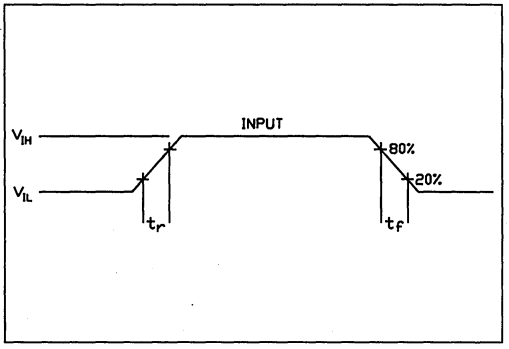


Figure 2.

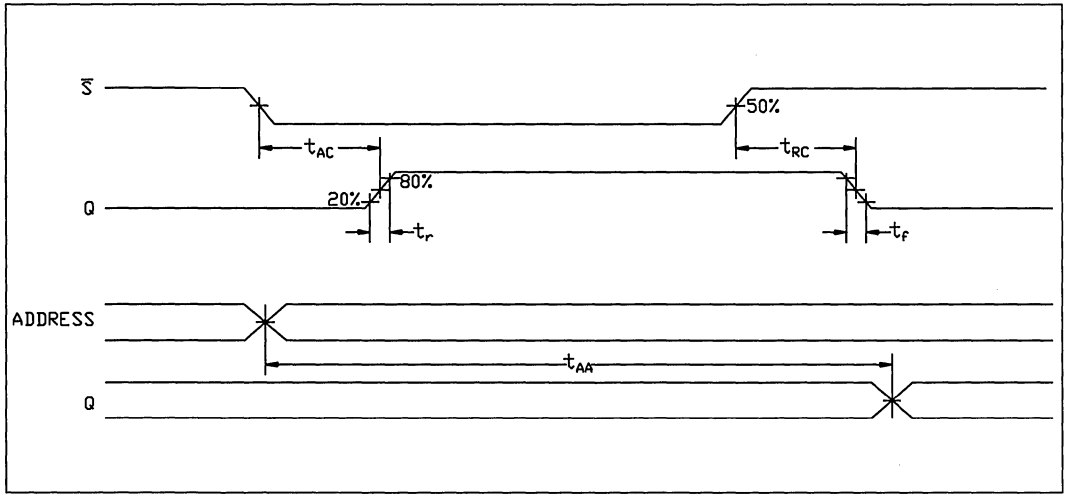
Notes :
5. $V_{IL} = V_{IL}$ Min., $V_{IH} = V_{IH}$ Max. on 10E version.
6. $V_{IL} = -1.7$ V, $V_{IH} = -0.9$ V on 100 K version.
7. $R_L = 50\ \Omega$, C < 5 pF (3 ns grade) or < 30 pF (5, 7 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be 50 Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. $t_r = t_f = 0.7$ ns.
10. All timing measurements are made from the 50 % point of all

5

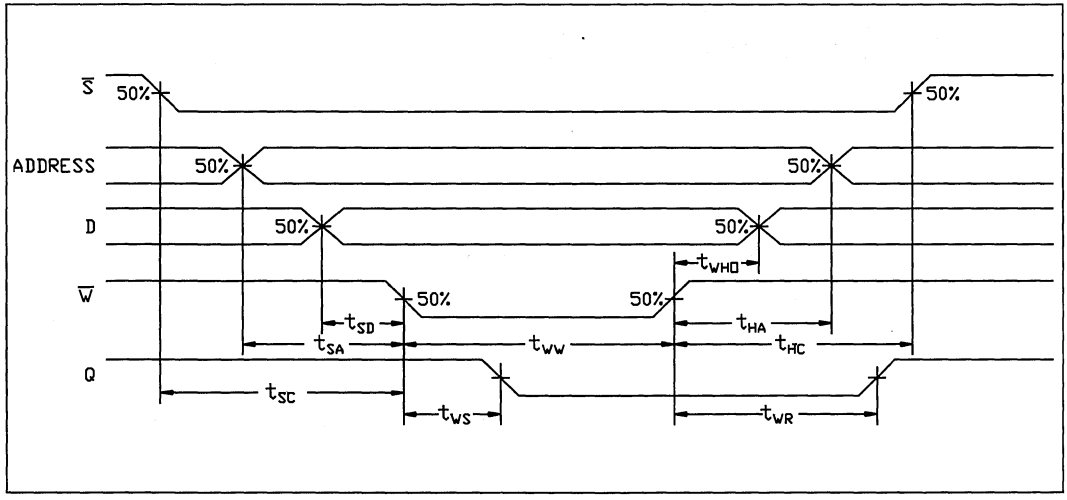
SWITCHING CHARACTERISTICS Over Operating Range

PARAMETERS	DESCRIPTION	10E474-3 100E474-3		10E474-5 100E474-5		10E474-7 100E474-7		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		2.0	0.5	3.0	0.5	5.0	ns
t_{RC}	Chip Select Recovery		2.0	0.5	3.0	0.5	5.0	ns
t_{AA}	Address Access Time		3.0	1.2	5.0	1.2	7.0	ns
t_{WW}	Write Pulse Width	3.0		5.0		5.0		ns
t_{SD}	Data Setup to Write	0.5		0.0		0.0		ns
t_{HD}	Data Hold to Write	0.5		0.0		1.0		ns
t_{SA}	Address Setup/Write	0.5		0.0		1.0		ns
t_{HA}	Address Hold/Write	0.5		0.0		1.0		ns
t_{SC}	Chip Select Setup/Write	0.5		0.0		0.0		ns
t_{HC}	Chip Select Hold/Write	0.5		0.0		1.0		ns
t_{WS}	Write Disable		2.0	0.3	3.0	0.3	6.5	ns
t_{WR}	Write Recovery		3.5	0.5	5.0	0.5	7.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	2.5	1.0	2.5	ns
t_f	Ooutput Fall Time	0.35	1.5	0.35	2.5	1.0	2.5	ns

SWITCHING WAVEFORMS



Read Mode



Write Mode

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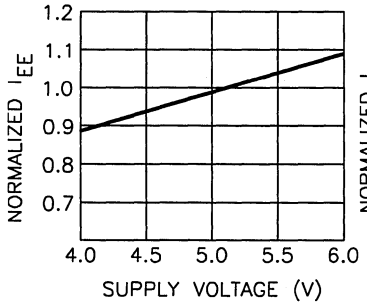
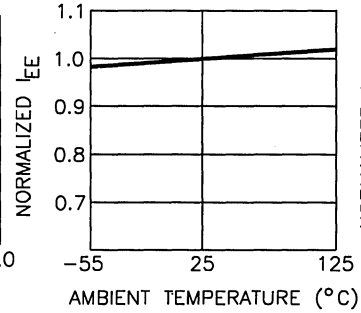
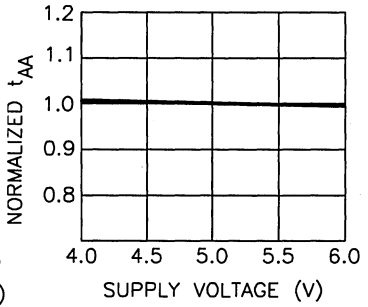
NORMALIZED SUPPLY VOLTAGE vs. SUPPLY CURRENT



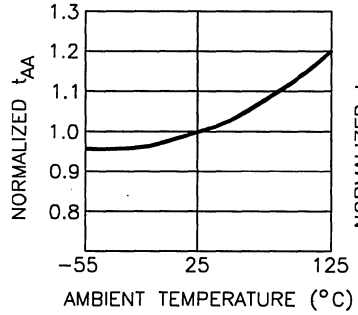
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



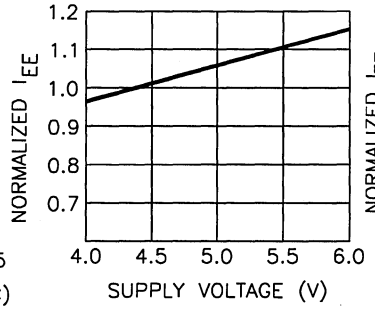
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



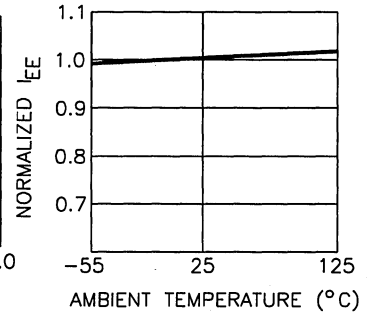
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



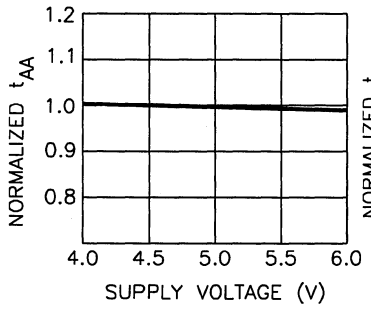
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



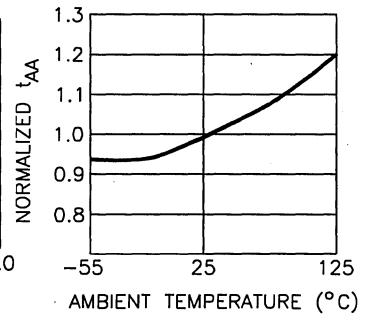
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



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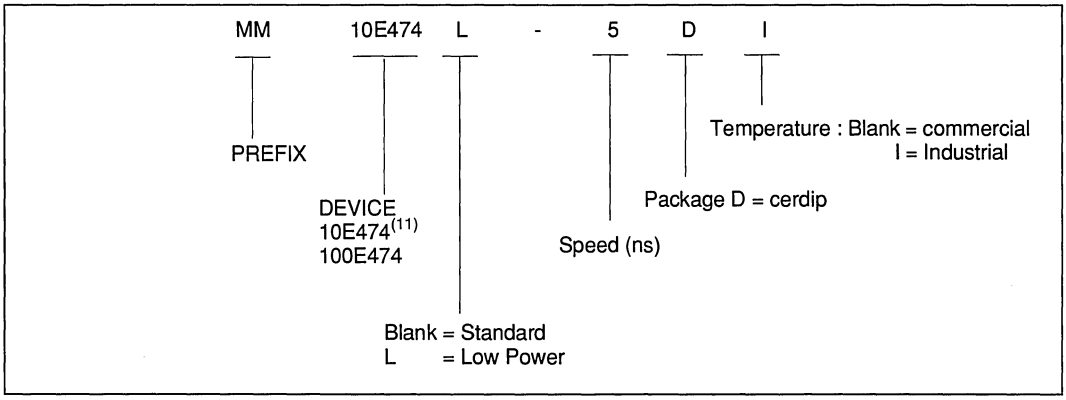
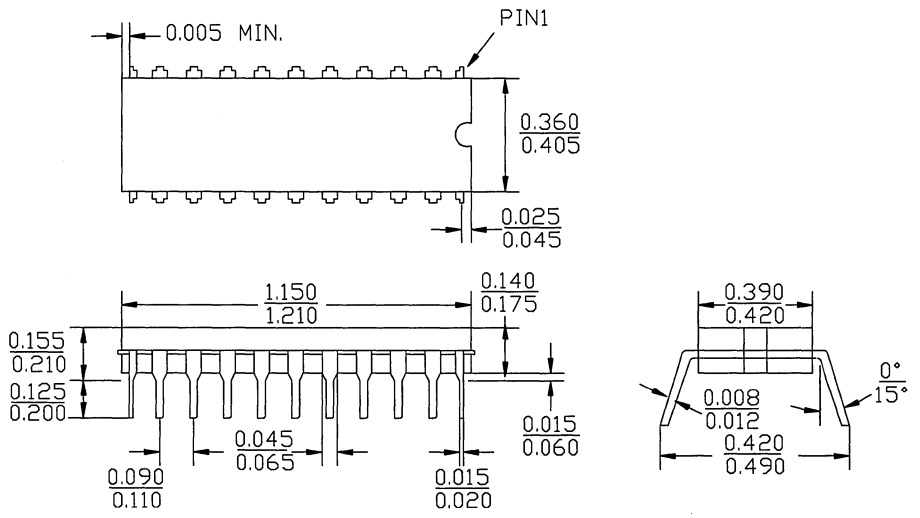
ORDERING INFORMATION



Note : 11. 10E specifications support both 10 K and 10 KH compatibility.

PACKAGE DIAGRAMS

24 LEAD (400 MIL) CERDIP



VERY LOW POWER CMOS SRAM

6

DATA SHEET

HM 65162

2 k x 8
VERY LOW POWER CMOS SRAM

FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 70/85 ns (max)
  COMMERCIAL : 55/70 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 240 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE : – 55 TO + 125°C**
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

6

DESCRIPTION

The HM 65162 is a very low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
The HM 65162 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1 µa) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

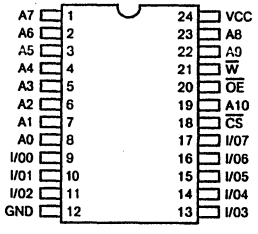
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM-65162 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65162 is processed following the test methods of MIL STD 883C.

PACKAGES

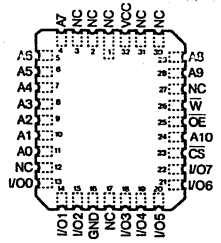
Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

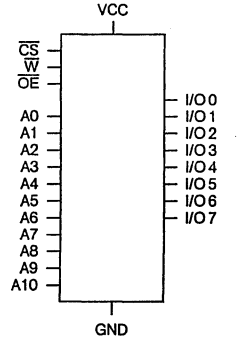
Pinout DIL 24 pins (top view)



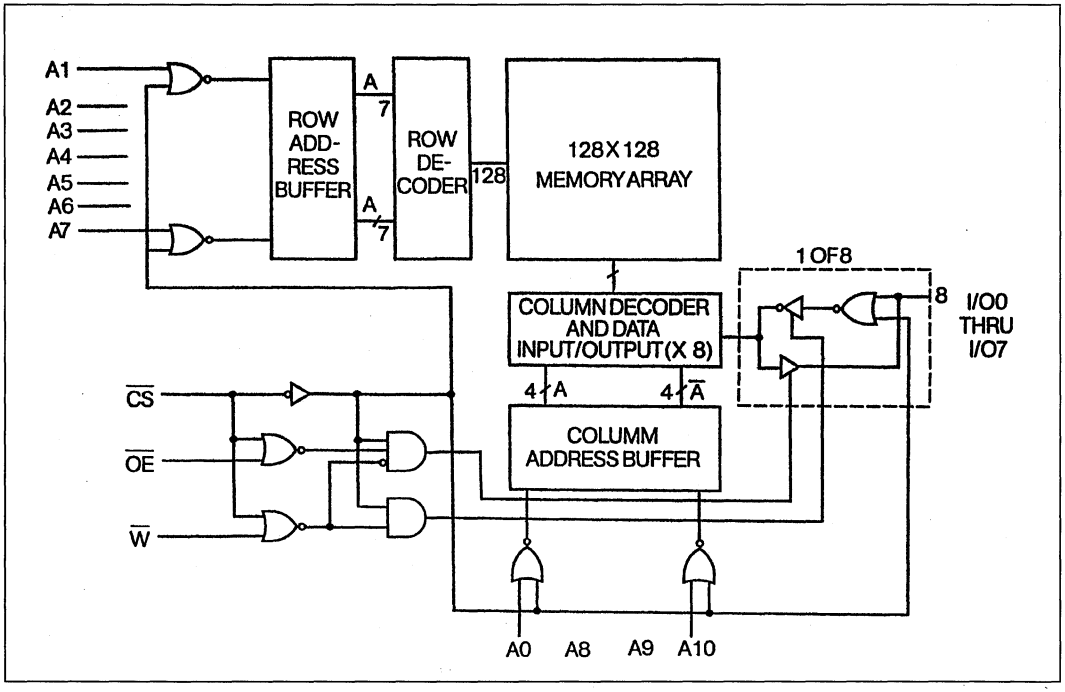
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



6

PIN NAMES

A0-A10	: Address inputs	$\overline{CS}$	: Chip Select
I/O0-I/O7	: Input/Output	$\overline{OE}$	: Output Enable
Vcc	: Power	$\overline{W}$	: Write enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	– 0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3 V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	5	pF
Cout (2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100% tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < VIN < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4.0mA, IOH = - 1.0mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	70.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65162 B-9	65162 -9	65162 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	3.0	3.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	70.0	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65162 B-2	65162 -2	65162 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	5.0	5.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	70.0	mA	max

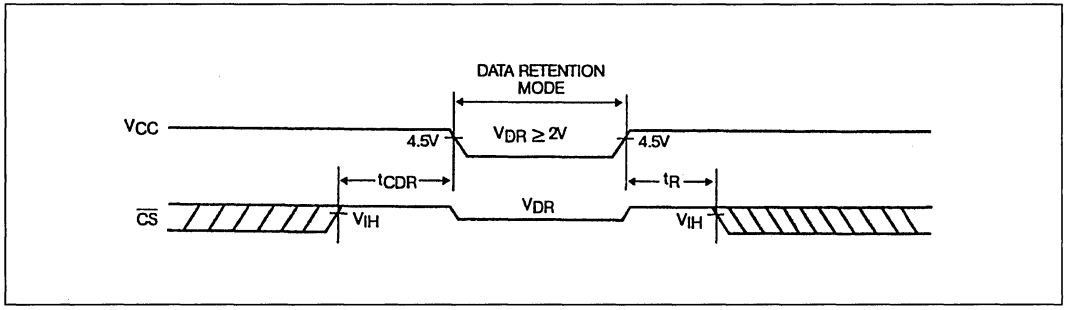
Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA..
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70% of Vcc during the power up and power down transitions.
4. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	2.0 V : HM-65162(B)-5	–	0.1	1.0	µA
	HM-65162(B)-9	–	0.1	3.0	µA
	HM-65162(B)-2	–	0.1	20.0	µA
	HM-65162C-5	–	0.1	30.0	µA
	HM-65162C-9	–	0.1	30.0	µA
	HM-65162C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	3.0 V : HM-65162(B)-5	–	0.3	1.0	µA
	HM-65162(B)-9	–	0.3	3.0	µA
	HM-65162(B)-2	–	0.3	30.0	µA
	HM-65162C-5	–	0.3	50.0	µA
	HM-65162C-9	–	0.3	50.0	µA
	HM-65162C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Commercial specification

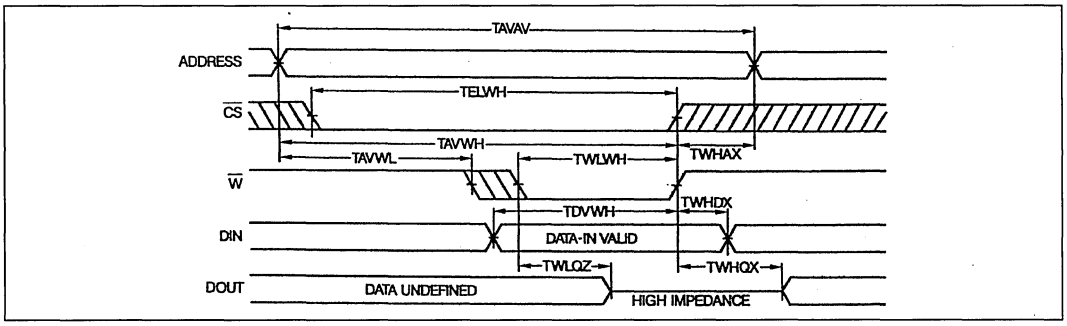
SYMBOL	PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
TAVAV	Write cycle time	55	70	70	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	45	50	50	ns	min
TDVWH	Data set-up time	25	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	40	45	45	ns	min
TWLQZ (12)	Write low to high Z	35	40	40	ns	max
TWLWH	Write pulse width	35	40	40	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

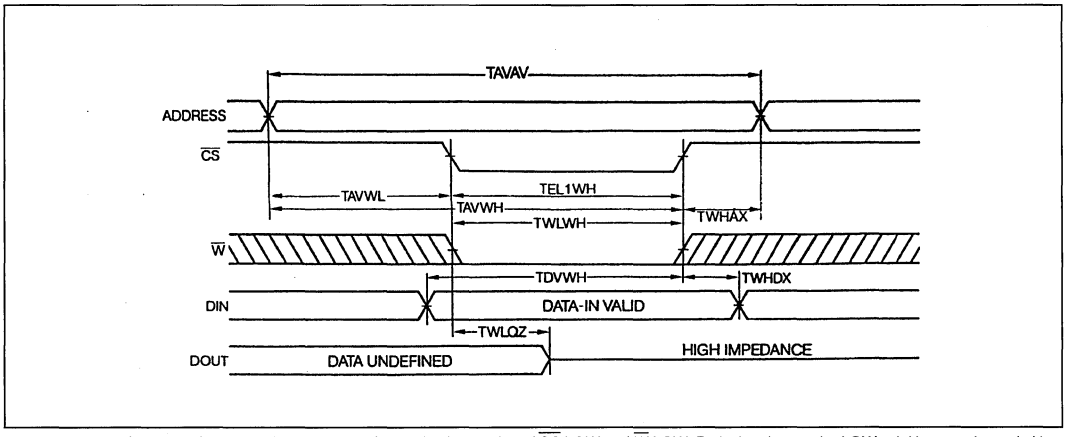
SYMBOL	PARAMETER	65162 B-9/2	65162 -9/2	65162 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	65	65	ns	min
TDVWH	Data set-up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	40	50	50	ns	max
TWLWH	Write pulse width	40	55	55	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.

6

READ CYCLE : Commercial specification

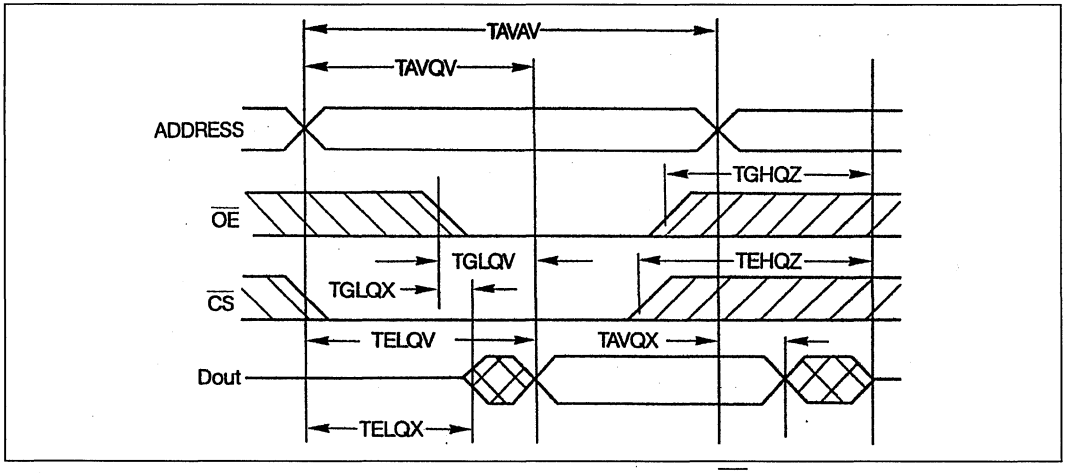
SYMBOL	PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
TAVAV	READ cycle time	55	70	70	ns	min
TAVQV	Address access time	55	70	70	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	55	70	70	ns	max
TELQZ	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output enable access time	40	50	50	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	max

READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65162 B-9/2	65162 -9/2	65162 C-9/2	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output Enable access time	50	65	65	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	min

6

READ CYCLE

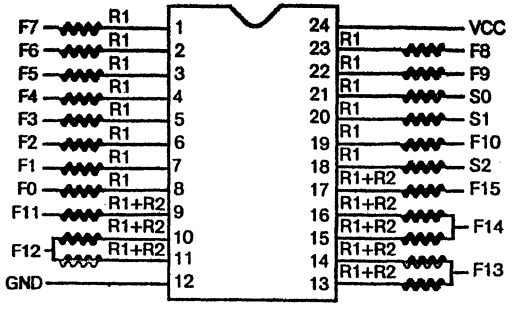


Addresses must remain stable for the duration of the read cycle. To read $\overline{OE}$ and $\overline{CS}$ must be < VIL and W VIH. The output buffers can be controlled independently by $\overline{OE}$ while $\overline{CS}$ is low. To execute consecutive read cycles. $\overline{CS}$ may be tied low continuously until all desired locations are accessed. When $\overline{CS}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65162	B	– 5
0 - Chip form 1 - Ceramic 24 pins 600 mils 3 - Plastic 24 pins 600 mils 4 - LCC 32 pins	2 k x 8 very low power static RAM	B = high speed/low current Blank : standard speed/low current C : standard	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

BURN-IN SCHEMATICS



R1 = 1 KΩ
R2 = 2.2 KΩ

Fo = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write / read cycles

VCC = 5.5 V

6

DATA SHEET

HM 65262

16 k x 1
VERY LOW POWER CMOS SRAM

FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 70/85 ns (max)
  COMMERCIAL : 55/70 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 110 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE : – 55 TO + 125°C**
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

6

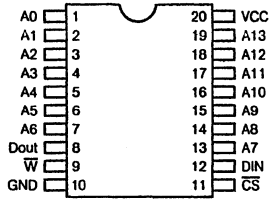
DESCRIPTION

The HM 65262 is a very low power CMOS static RAM organized as 16384 x 1 bit. It is manufactured using the MHS high performance CMOS technology.
The HM 65262 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1 µA) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65262 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65262 is processed following the test methods of MIL STD 883C.

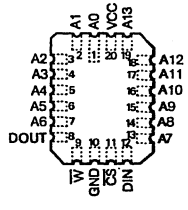
PACKAGES

Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
LCC, 20 pins.

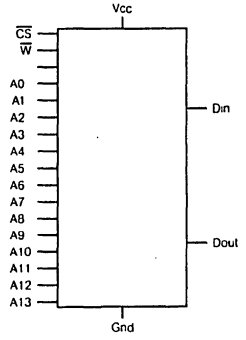
Pinout DIL 20 pins (top view)



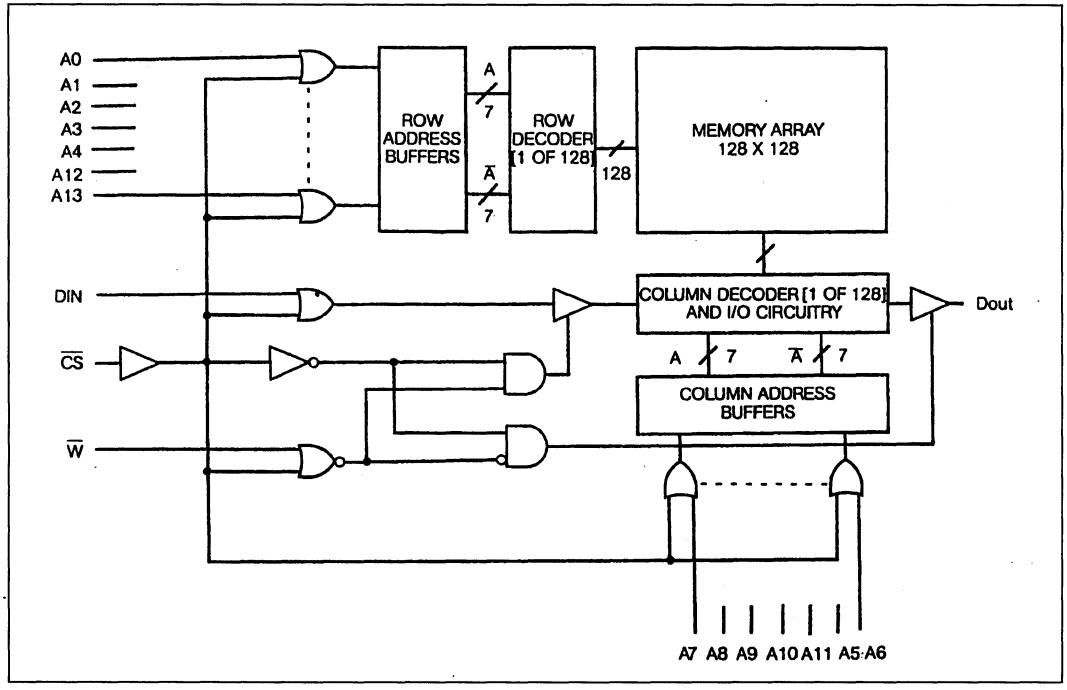
Pinout LCC 20 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



6

PIN NAMES

A0-A13	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	VCC	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	– 0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3 V	V

Note : 1. VIL min = – 0.3 V or - 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 8.0 mA, IOH = – 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65262 B-9	65262 -9	65262 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	3.0	3.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65262 B-2	65262 -2	65262 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	5.0	5.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

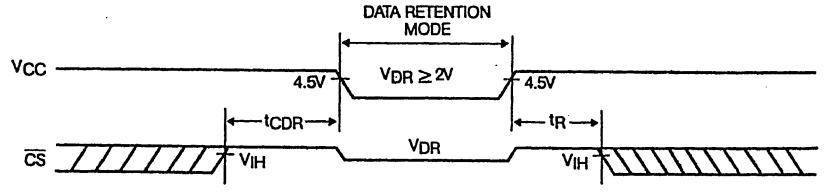
Notes : 5. $\overline{CS} \geq VIH$.
6. $\overline{CS} \geq Vcc - 0.3V$, Iout = 0 mA.
7. $\overline{CS} \leq VIL$, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
3. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	@ 2.0 V : HM-65262(B)-5	–	0.1	1.0	µA
	HM-65262(B)-9	–	0.1	3.0	µA
	HM-65262(B)-2	–	0.1	20.0	µA
	HM-65262C-5	–	0.1	30.0	µA
	HM-65262C-9	–	0.1	30.0	µA
	HM-65262C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-65262(B)-5	–	0.3	1.0	µA
	HM-65262(B)-9	–	0.3	3.0	µA
	HM-65262(B)-2	–	0.3	30.0	µA
	HM-65262C-5	–	0.3	50.0	µA
	HM-65262C-9	–	0.3	50.0	µA
	HM-65262C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Commercial specification

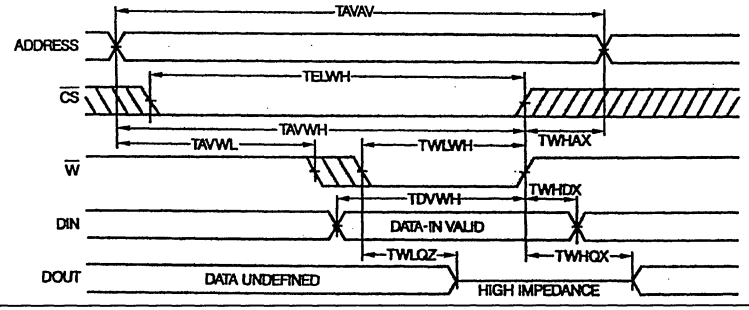
SYMBOL	PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
TAVAV	Write cycle time	55	70	70	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	55	55	ns	min
TDVWH	Data set-up time	35	40	40	ns	min
TELWH	$\overline{CS}$ low to write end	50	55	55	ns	min
TWLQZ (12)	Write low to high Z	35	40	40	ns	max
TWLWH	Write pulse width	50	55	55	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

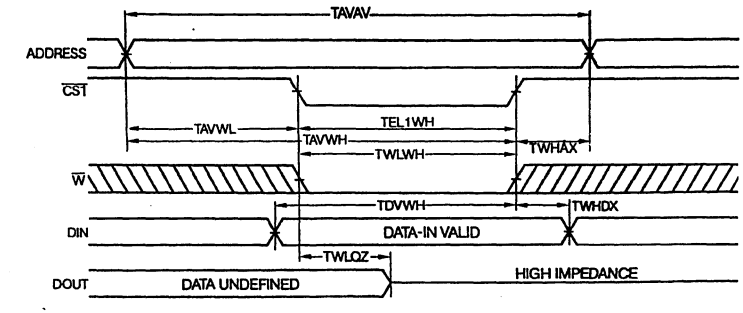
SYMBOL	PARAMETER	65262 B-9/2	65262 -9/2	65262 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	55	65	65	ns	min
TDVWH	Data set-up time	40	45	45	ns	min
TELWH	$\overline{CS}$ low to write end	55	65	65	ns	min
TWLQZ (12)	Write low to high Z	50	50	50	ns	max
TWLWH	Write pulse width	55	65	65	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

6

READ CYCLE : Commercial specification

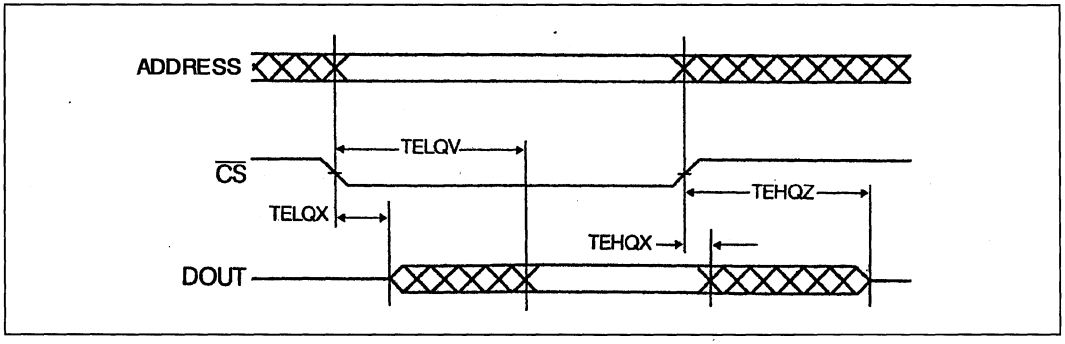
SYMBOL	PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
TAVAV	READ cycle time	55	70	70	ns	min
TAVQV	Address access time	55	70	70	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	55	70	70	ns	max
TELQZ	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	40	40	ns	max

READ CYCLE : Industrial and Military specification

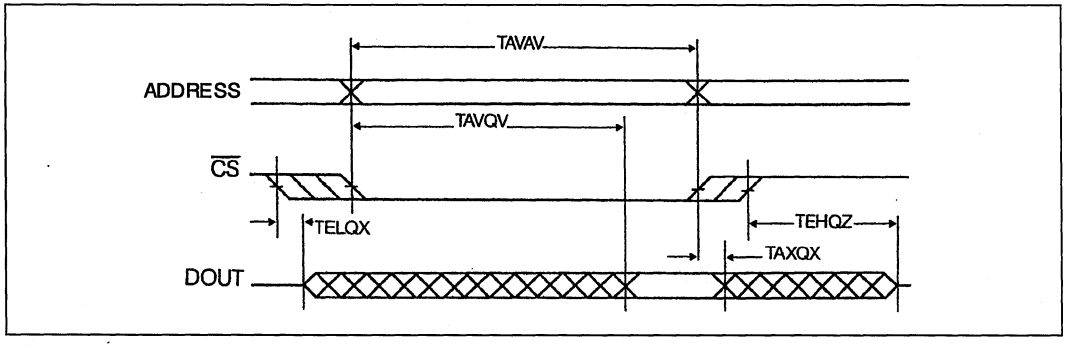
SYMBOL	PARAMETER	65262 B-9/2	65262 -9/2	65262 C-9/2	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	40	40	ns	max

6

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

Package
HM1
- 0 - Chip form
- 1 - Ceramic 20 pins 300 mils
- 3 - Plastic 20 pins 300 mils
- 4 - LCC 20 pins

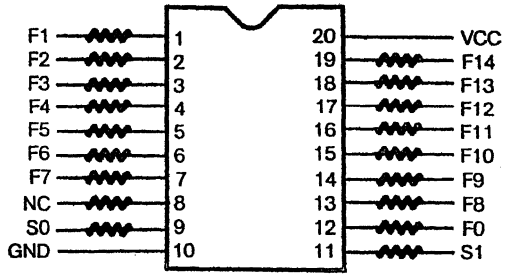
Device Type
65262
- 16 k x 1 very low power static RAM

Grade
B
- B = high speed/low current
- Blank : standard speed/low current
- C : standard

Level
– 5
- – 5 : Commercial
- – 5+ : Commercial with B.I.
- – 9 : Industrial
- – 9+ : Industrial with B.I.
- – 2 : Military
- – 8 : Military with B.I.

(B.I. = Burn-in)

BURN-IN SCHEMATICS



R = 1 KΩ
Fo = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

VCC = 5.5 V

NC = Not connected

6

DATA SHEET

HM 65641

8 k x 8
VERY LOW POWER CMOS SRAM

FEATURES

- **FAST ACCES TIME**
  MILITARY/INDUSTRIAL : 70/85 ns (max)
  COMMERCIAL : 55/70 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 125 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE : – 55 TO + 125°C**
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**
- **LATCH UP IMMUNE**
- **RADIATION TOLERANT**

6

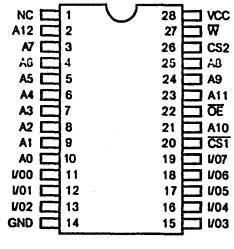
DESCRIPTION

The HM-65641 is a very low power CMOS static RAM organized as 8192 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
The HM-65641 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting an extremely low standby supply current (typical value = 0.1 µA) over the full temperature range. The high stability of the 6T cell provides an excellent protection against soft errors due to noise. Easy memory expansion is provided by an active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM-65641 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65641 is processed following the test methods of MIL STD 883C.

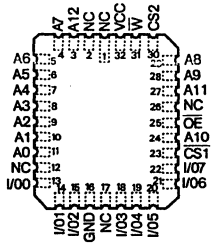
PACKAGES

Plastic 600 mils, 28 pins, DIL.
Ceramic 600 mils, 28 pins, DIL.
LCC, 32 pins.

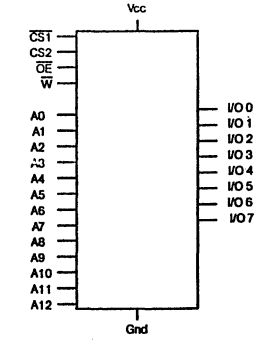
Pinout DIL 28 pins (top view)



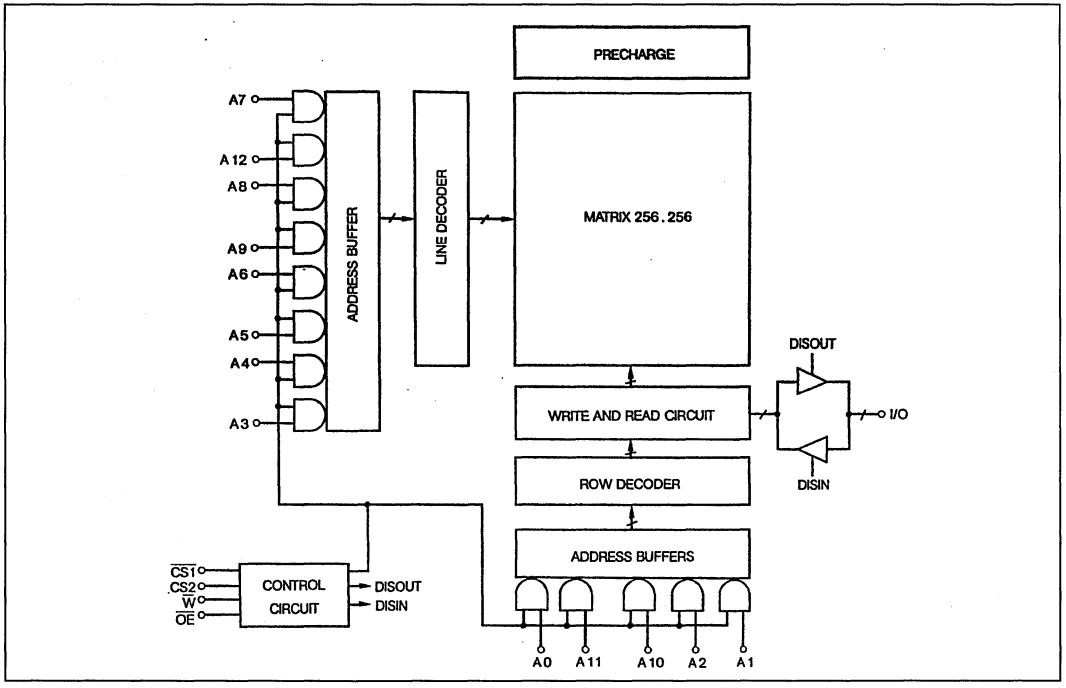
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



6

PIN NAMES

A0-A12 : Address inputs	$\overline{CS1}$: Chip Select 1
I/O0-I/O7 : Input/Output	CS2 : Chip Select 2
Vcc : Power	$\overline{OE}$: Output Enable
Gnd : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	– 0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	3.5	Vcc + 0.3 V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < VIN < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65641 B-5	65641 S-5	65641 -5	65641 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	8.0	10.0	8.0	10.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	100.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	8.0	12.0	8.0	12.0	mA	max
ICCOP	(8)	Operating supply current	135.0	135.0	125.0	125.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65641 B-9	65641 S-9	65641 -9	65641 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	8.0	10.0	8.0	10.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	8.0	12.0	8.0	12.0	mA	max
ICCOP	(8)	Operating supply current	135.0	135.0	125.0	125.0	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65641 B-2	65641 S-2	65641 -2	65641 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	8.0	10.0	8.0	10.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	8.0	12.0	8.0	12.0	mA	max
ICCOP	(8)	Operating supply current	135.0	135.0	125.0	125.0	mA	max

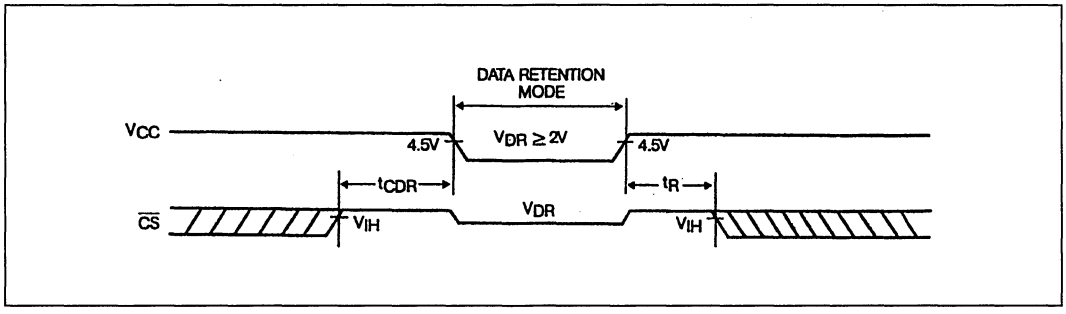
Notes : 5. $\overline{CS1} \geq$ VIH, CS2 ≤ VIL.
6. $\overline{CS1} \geq$ Vcc – 0.3 V, CS2 ≤ 0.3 V, Iout = 0 mA.
7. CS1 ≤ VIL, CS2 ≤ VIH, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	2.0 V : HM-65641 (B)-5	–	0.1	1.0	µA
	HM-65641 (B)-9	–	0.1	3.0	µA
	HM-65641 (B)-2	–	0.1	20.0	µA
	HM-65641S/C-5	–	0.1	30.0	µA
	HM-65641S/C-9	–	0.1	30.0	µA
	HM-65641S/C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	3.0 V : HM-65641 (B)-5	–	0.3	1.0	µA
	HM-65641 (B)-9	–	0.3	3.0	µA
	HM-65641 (B)-2	–	0.3	30.0	µA
	HM-65641S/C-5	–	0.3	50.0	µA
	HM-65641S/C-9	–	0.3	50.0	µA
	HM-65641S/C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

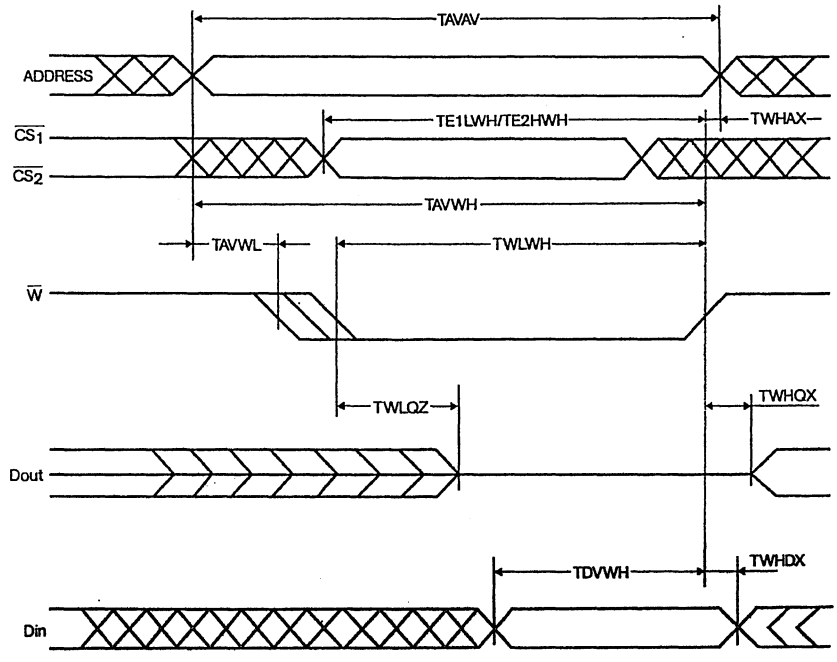
WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65641 B-5	65641 S-5	65641 -5	65641 C-5	UNIT	VALUE
TAVAV	Write cycle time	55	55	70	70	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	50	50	55	55	ns	min
TEH2WH	$\overline{CS2}$ high to write end	50	50	55	55	ns	min
TWLQZ (12)	Write low to high Z	25	25	30	30	ns	max
TWLWH	Write pulse width	45	45	55	55	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	5	5	5	5	ns	min
TWHQX (12)	Write high to low Z	5	5	5	5	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65641 B-9/2	65641 S-9/2	65641 -9/2	65641 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	70	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	55	55	70	70	ns	min
TDVWH	Data set-up time	25	25	30	30	ns	min
TEL1WH	$\overline{CS1}$ low to write end	55	55	70	70	ns	min
TEH2WH	CS2 high to write end	55	55	70	70	ns	min
TWLQZ (12)	Write low to high Z	30	30	40	40	ns	max
TWLWH	Write pulse width	55	55	70	70	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	5	5	5	5	ns	min
TWHQX (12)	Write high to low Z	5	5	5	5	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



The internal write time of the memory is defined by the overlap of $\overline{CS_1}$ LOW, $\overline{CS_2}$ HIGH and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE}$ = VIH.

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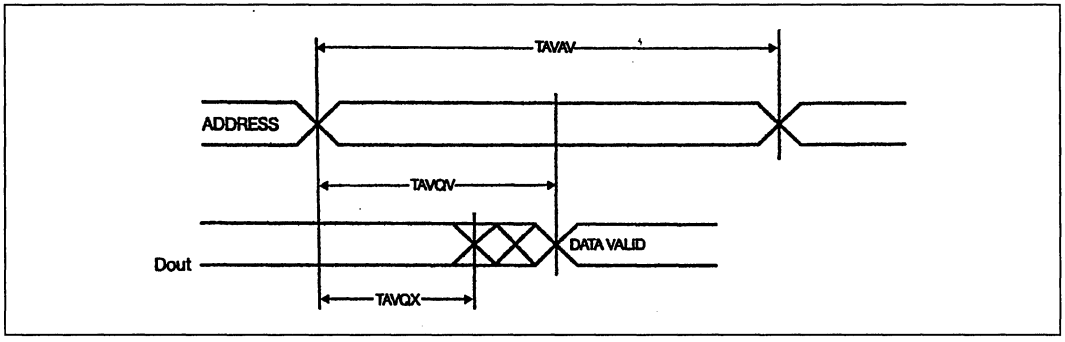
READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65641 B-5	65641 S-5	65641 -5	65641 C-5	UNIT	VALUE
TAVAV	Read cycle time	55	55	70	70	ns	min
TAVQV	Address access time	55	55	70	70	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	55	55	70	70	ns	max
TEH2QV	Chip-select 2 access time	55	55	70	70	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	max
TEH2QX	CS2 high to low Z	5	5	5	5	ns	max
TEH1QZ	$\overline{CS1}$ high to high Z	25	25	30	30	ns	max
TEL2QZ	CS2 low to high Z	25	25	30	30	ns	max
TGLQV	Ouptut Enable access time	25	25	30	30	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	25	25	30	30	ns	max

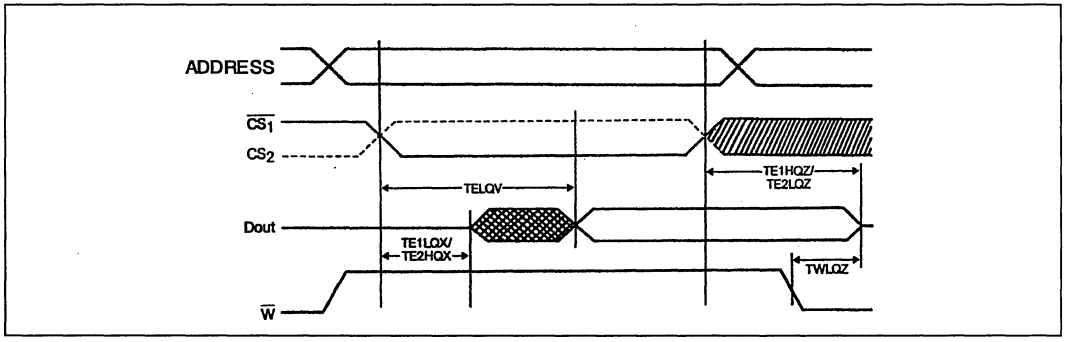
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65641 B-9/2	65641 S-9/2	65641 -9/2	65641 C-9/2	UNIT	VALUE
TAVAV	Read cycle time	70	70	85	85	ns	min
TAVQV	Address access time	70	70	85	85	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	70	70	85	85	ns	max
TEH2QV	Chip-select 2 access time	70	70	85	85	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	max
TEH2QX	CS2 high to low Z	5	5	5	5	ns	max
TEH1QZ	CS1 high to high Z	30	30	40	40	ns	max
TEL2QZ	CS2 LOW to high Z	30	30	40	40	ns	max
TGLQV	Ouptut Enable access time	30	30	40	40	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	30	30	40	40	ns	max

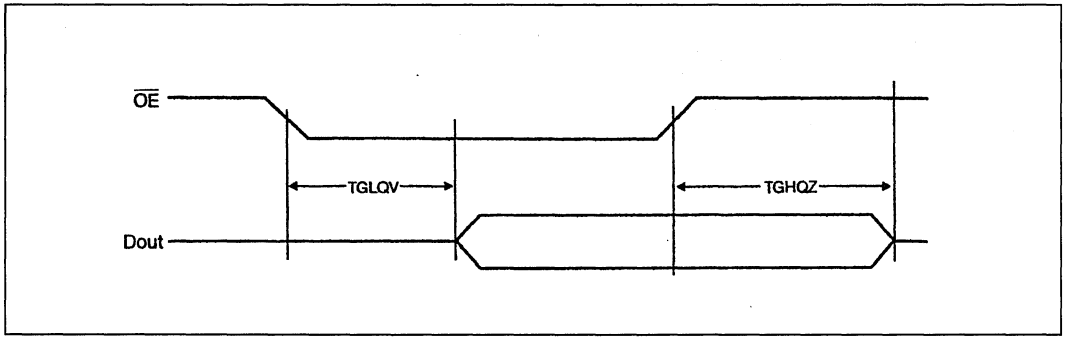
READ CYCLE nb 1



READ CYCLE nb 2



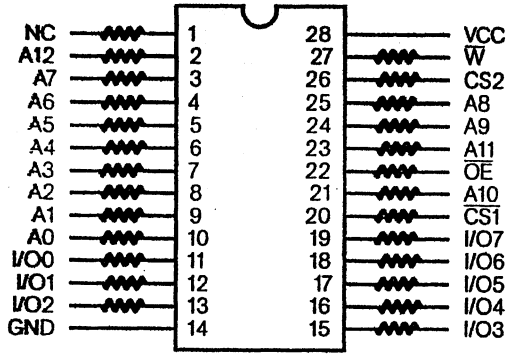
READ CYCLE nb 3



ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65641	B	– 5
0 - Chip form 1 - Ceramic 28 pins 600 mils 3 - Plastic 28 pins 600 mils 4 - LCC 32 pins	8 k x 8 very low power static RAM	B = high speed/low current S = high speed/standard current Blank : standard speed/low current C : standard	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

BURN-IN SCHEMATICS



R = 1 KΩ
FO = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2, S3, S4 : programmable signals for write / read cycles

VCC = 5.5 V

NC = Not connected

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GENERAL PURPOSE CMOS SRAM

7

MHS

DATA SHEET

HM 6116

2 k x 8
GENERAL PURPOSE CMOS SRAM

FEATURES

- **ACCESSS TIME**
  MILITARY : 120 ns (max)
  INDUSTRIAL : 120 ns (max)
  COMMERCIAL : 120 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 240 mW (typ)
  STANDBY : 25 µW (typ)
  DATA RETENTION : 4 µW (typ)
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **NO CLOCK AND STROBES REQUIRED**
- **GATED INPUTS**
- **WIDE TEMPERATURE RANGE : – 55 TO + 125 °C**

DESCRIPTION

The HM 6116 is a low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
120 ns access time for commercial temperature range is available with a maximum power consumption of only 385 mW.
The HM 6116 features fully static operation requiring no external clocks or timing strobes. Thanks to the special input buffer "gated inputs", the circuit stays in stand by mode when the $\overline{CS}$ goes to an intermediate level (VIH). Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
The HM 6116 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 6116 is processed following the test methods of MIL STD 883C.

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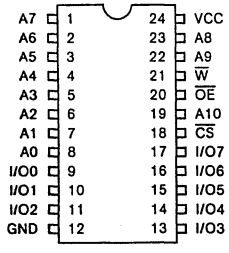
PACKAGES

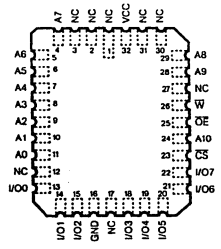
Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

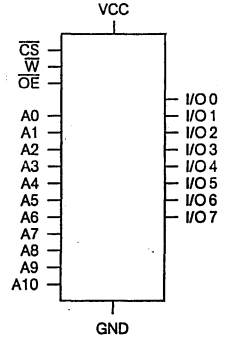
Pinout DIL 24 pins (top view)



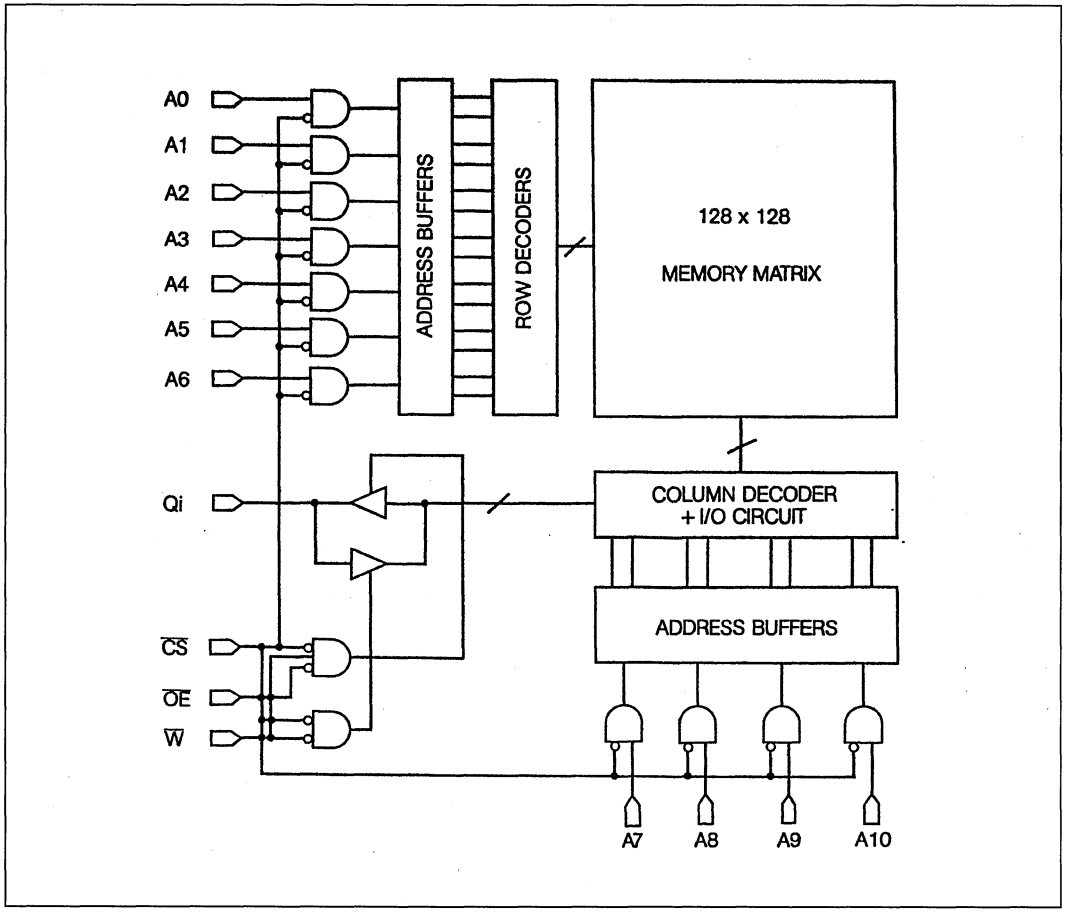
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A10	: Address inputs	$\overline{CS}$	: Chip Select
I/O0-I/O7	: Input/Output	$\overline{OE}$	: Output enable
Vcc	: Power	$\overline{W}$	: Write Enable
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc		Supply voltage	4.5	5.0	5.5	V
Gnd		Ground	0.0	0.0	0.0	V
VIL	(1)	Input low voltage	– 0.3	0.0	0.8	V
VIH		Input high voltage	2.2	–	V_{CC} + 0.3V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(2)	Input capacitance	–	–	8	pF
Cout	(2)	Output capacitance	–	–	10	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

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ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	– 5.0	–	5.0	µA
IOZ (3)	Output leakage current	– 5.0	–	5.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled specified to ± 10 µA for the HM 6116 2.
4. Vcc min, IOL = 3.2 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL	PARAMETER	6116 -5	6116 L-5	6116 B-5	UNIT	VALUE
ICCSB (5)	Standby supply current	3.0	2.0	2.0	mA	max
ICCSB1 (6)	Standby supply current	2000.0	100.0	1.0	µA	max
ICC (7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP (8)	Operating supply current	70.0	70.0	70.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL	PARAMETER	6116 -9	6116 L-9	6116 B-9	UNIT	VALUE
ICCSB (5)	Standby supply current	4.5	4.0	4.0	mA	max
ICCSB1 (6)	Standby supply current	2000.0	500.0	5.0	µA	max
ICC (7)	Operating supply current	80.0	80.0	80.0	mA	max
ICCOP (8)	Operating supply current	80.0	80.0	80.0	mA	max

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Consumption for Military specification (– 2) :

SYMBOL	PARAMETER	6116 -2	6116 L-2	UNIT	VALUE
ICCSB (5)	Standby supply current	5.0	4.5	mA	max
ICCSB1 (6)	Standby supply current	3000.0	1500.0	µA	max
ICC (7)	Operating supply current	85.0	85.0	mA	max
ICCOP (8)	Operating supply current	85.0	85.0	mA	max

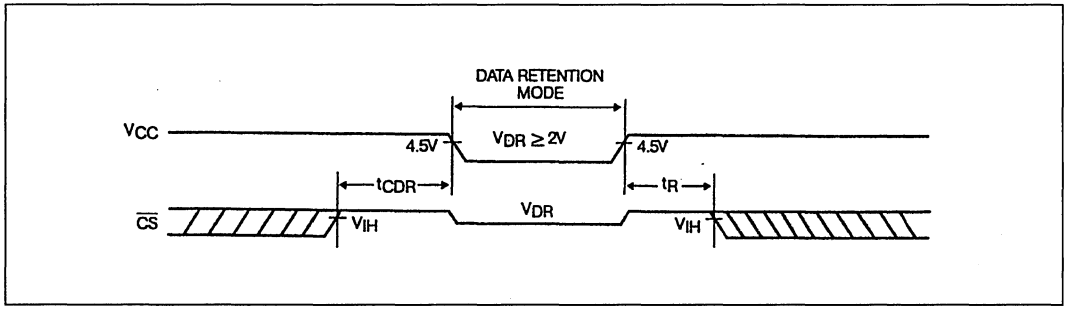
Notes : 5. $\overline{CS} \leq$ VIH.
6. $\overline{CS} \leq$ Vcc – 0.3 V, Iout = 0 mA.
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retenti on time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	–
ICCDR1 (11)	Data retention current				
	@ 2.0 V : HM-6116B -5	–	0.1	1.0	µA
	HM-6116B -9	–	0.1	5.0	µA
	HM-6116L -5	–	2.0	30.0	µA
	HM-6116L -9	–	2.0	200.0	µA
	HM-6116L -2	–	2.0	600.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-6116B -5	–	0.3	1.0	µA
	HM-6116B -9	–	0.3	7.0	µA
	HM-6116L -5	–	3.0	45.0	µA
	HM-6116L -9	–	3.0	300.0	µA
	HM-6116L -2	–	3.0	900.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

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ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

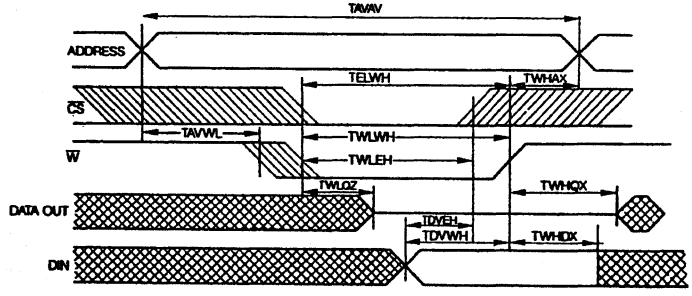
Input pulse levels : Gnd to 3.0 V
Input rise : 10 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE

SYMBOL	PARAMETER	6116 (B)(L) -5/ -9/ -2	UNIT	VALUE
TAVAV	Write cycle time	120	ns	min
TAVWL	Address set-up time	0	ns	min
TAVWH	Address valid to end of write	105	ns	min
TDVWH	Data set-up time	35	ns	min
TELWH	$\overline{CS}$ low to write end	70	ns	min
TWLQZ (12)	Write low to high Z	50	ns	max
TWLWH	Write pulse width	70	ns	min
TWHAX	Address hold to end of write	10	ns	min
TWHDX	Data hold time	10	ns	min
TWHQX (12)	Write high to low Z	5	ns	min

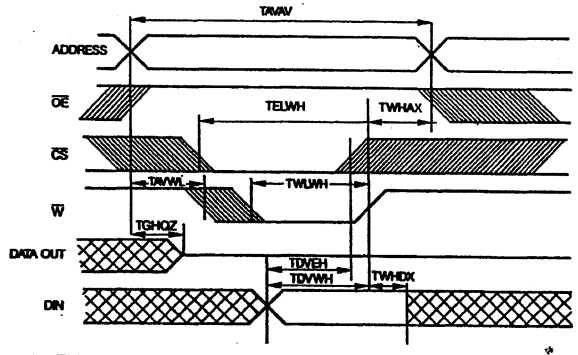
Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1



$\overline{OE}$ = VIH during this write cycle. This write cycle is recommended for continuous writing.

WRITE CYCLE 2

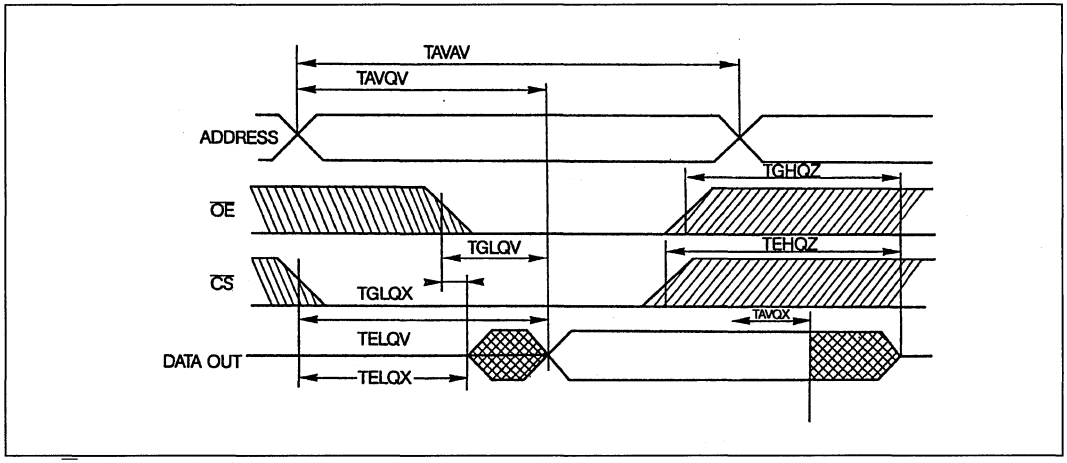


$\overline{OE}$ is low throughout write cycle. This write cycle time way be used for write and read in the same cycle (write followed by read).

READ CYCLE

SYMBOL	PARAMETER	6116 (B)(L) -5/ -9/ -2	UNIT	VALUE
TAVAV	Write cycle time	120	ns	min
TAVQV	Address access time	120	ns	max
TAVQX	Address valid to low Z	10	ns	min
TELQV	Chip-select access time	120	ns	max
TELQX	$\overline{CS}$ low to low Z	10	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	ns	max
TGLQV	Output Enable access time	80	ns	max
TGLQX	$\overline{OE}$ low to low Z	10	ns	min
TGHQZ	$\overline{OE}$ high to high Z	40	ns	max

READ CYCLE



Note : $\overline{W}$ high for a read cycle.

ORDERING INFORMATION

Package

HM1

- 0 - Chip form
- 1 - Ceramic 24 pins
- 3 - Plastic 24 pins
- 4 - LCC 32 pins

Device Type

6116

2 k x 8 general purpose static RAM

L

- L = Low power
- Blank = Standard
- B = very Low Power (only for – 5/– 9 version)

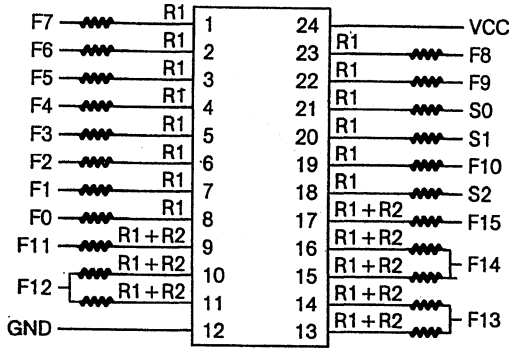
Level

– 5

- – 5 : Commercial
- – 5+ : Commercial with B.I.
- – 9 : Industrial
- – 9+ : Industrial with B.I.
- – 2 : Military
- – 8 : Military with B.I.

(B.I. : Burn-in)

BURN-IN SCHEMATICS



R1 = 220 Ω per row or 1 KΩ per pin
R2 = 2.2 KΩ per driver

Fo = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write / read cycles

VCC = 5.5 V

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DATA SHEET

HM 65161

2 k x 8
GENERAL PURPOSE CMOS SRAM

FEATURES

- **ACCESS TIME**
  MILITARY: 90 ns (max)
  INDUSTRIAL : 80 ns (max)
  COMMERCIAL : 70 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 240 mW (typ)
  STANDBY : 25 µW (typ)
  DATA RETENTION : 4 µW (typ)
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **NO CLOCK AND STROBES REQUIRED**
- **GATED INPUTS**
- **WIDE TEMPERATURE RANGE : – 55 TO + 125°C**

DESCRIPTION

The HM 65161 is a low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
70 ns access time for commercial temperature range is available with a maximum power consumption of only 385mW.
The HM 65161 features fully static operation requiring no external clocks or timing strobes. Thanks to the special input buffer "gated inputs", the circuit stays in stand by mode when the $\overline{CS}$ goes to an intermediate level (VIH).
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
The HM 65161 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65161 is processed following the test methods of MIL STD 883C.

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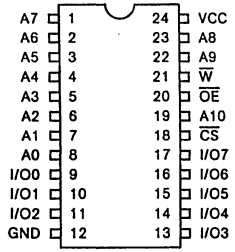
PACKAGES

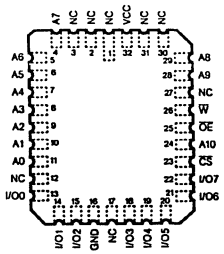
Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

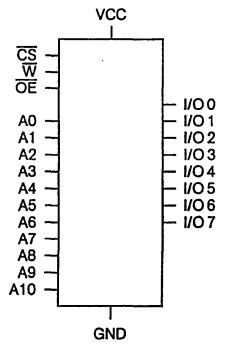
Pinout DIL 24 pins (top view)



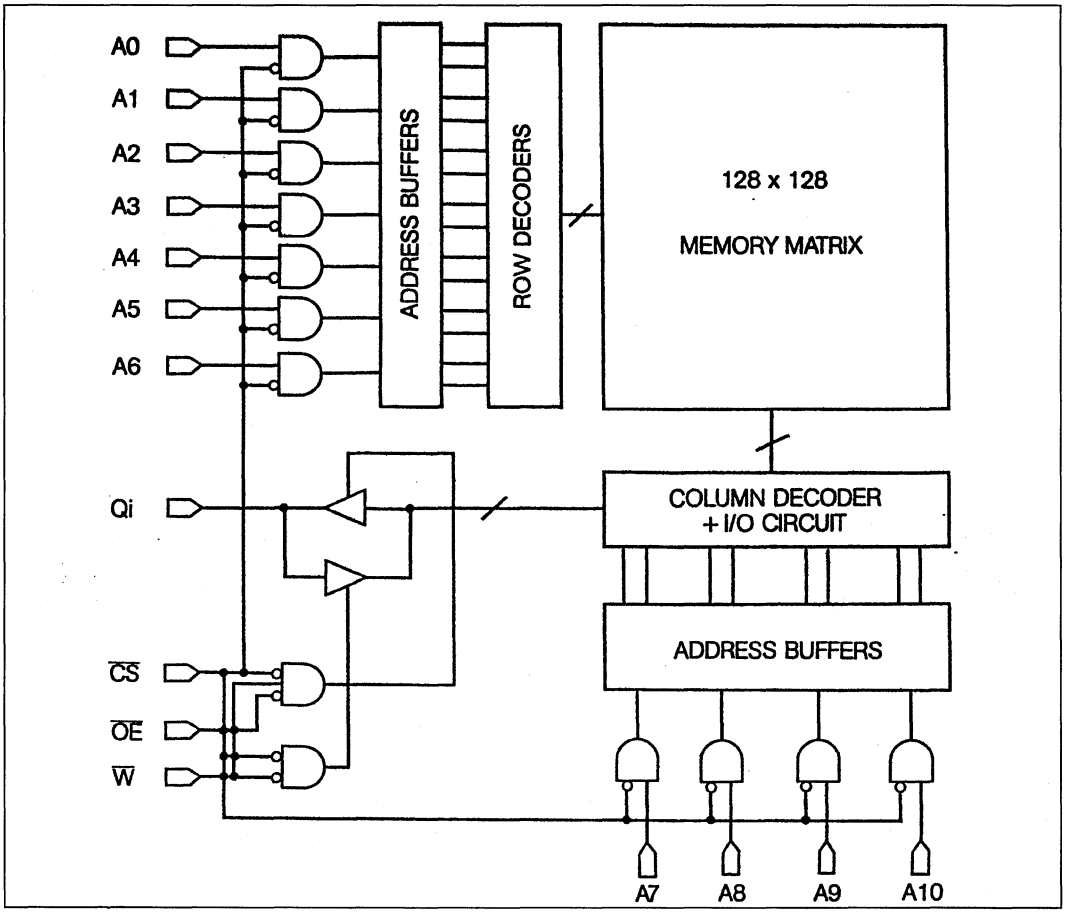
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A10 : Address inputs	I/O0-I/O7 : Input/Output
Vcc : Power	$\overline{CS}$: Chip Select
$\overline{OE}$: Output enable	$\overline{W}$: Write Enable

TRUTH TABLE

$\overline{CS1}$	$\overline{OE}$	W	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	3.5	V_{CC} + 0.3V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	10	pF

Note : 2. TA = 25°C, f = 1 MHz, VCC = 5.0 V, these parameters are not 100 % tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0*	–	1.0*	µA
IOZ	(3)	Output leakage current	– 1.0*	–	1.0*	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
* Specified to ± 2 µA for the HM-65161
4. Vcc min, IOL = 3.2 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65161-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	mA	max
ICCSB1	(6)	Standby supply current	100.0	µA	max
ICC	(7)	Operating supply current	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65161-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	mA	max
ICCSB1	(6)	Standby supply current	350.0	µA	max
ICC	(7)	Operating supply current	80.0	mA	max
ICCOP	(8)	Operating supply current	80.0	mA	max

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Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65161-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	4.0	mA	max
ICCSB1	(6)	Standby supply current	1000.0	µA	max
ICC	(7)	Operating supply current	85.0	mA	max
ICCOP	(8)	Operating supply current	85.0	mA	max

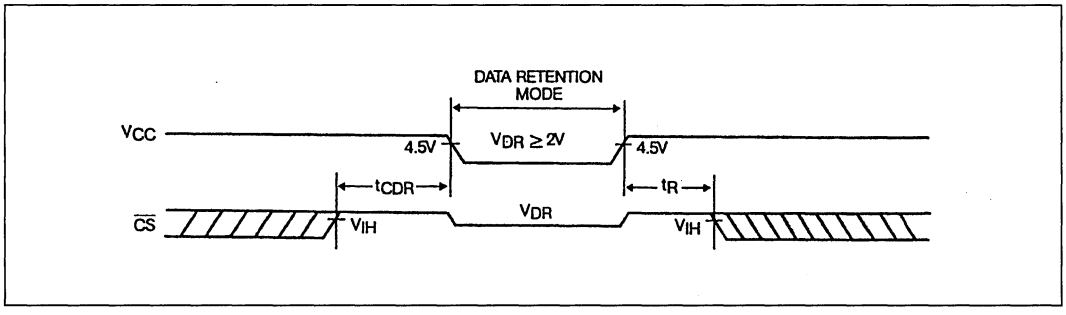
Notes : 5. $\overline{CS} \geq VIH$
6. $\overline{CS} \geq Vcc - 0.3$ V, Iout = 0 mA
7. $\overline{CS} \leq VIL$, Iout = 0 mA, Vin = Gnd/Vcc
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation
3. $\overline{CS}$ and $\overline{OE}$ must kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65161-5	–	2.0	30.0	µA
	HM-65161-9	–	2.0	140.0	µA
	HM-65161-2	–	2.0	400.0	µA
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65161-5	–	3.0	45.0	µA
	HM-65161-9	–	3.0	210.0	µA
	HM-65161-2	–	3.0	600.0	µA

Notes : 9. TA = 25°C
10. TAVAV = Read cycle time
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

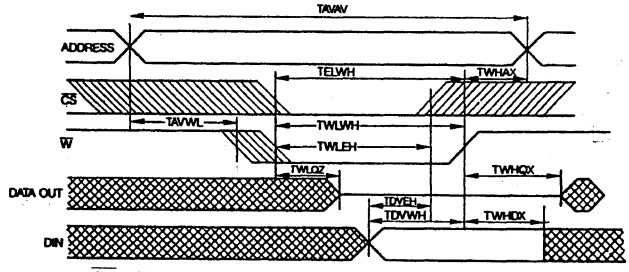
Input pulse levels	: Gnd to 3.0 V	Input timing reference levels	: 1.5 V
Input rise	: 10 ns	Output load	: 1 TTL gate + 100 pF

WRITE CYCLE

SYMBOL	PARAMETER	65161 -5	65161 -9	65161 -2	UNIT	VALUE
TAVAV	Write cycle time	70	80	90	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	65	65	65	ns	min
TDVWH	Data set-up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	65	65	65	ns	min
TWLQZ (12)	Write low to high Z	35	35	35	ns	max
TWLWH	Write pulse width	65	65	65	ns	min
TWHAX	Address hold to end of write	5	5	5	ns	min
TWHDX	Data hold time	5	5	5	ns	min
TWHQX (12)	Write high to low Z	5	5	5	ns	min

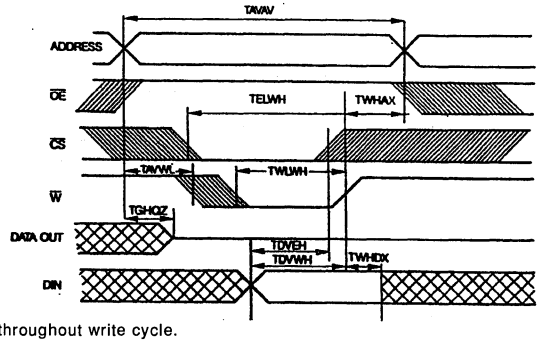
Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1



$\overline{OE}$ = VIH during this write cycle.
This write cycle is recommended for continuous writing.

WRITE CYCLE 2

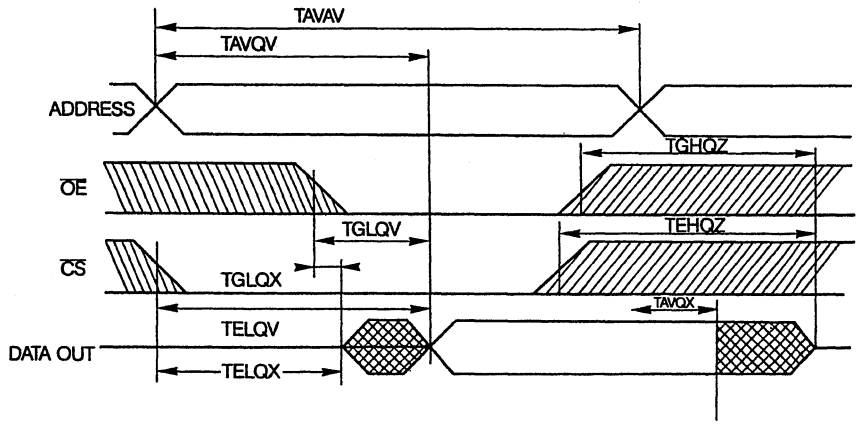


Note : $\overline{OE}$ is low throughout write cycle.
This write cycle time way be used for write and read in the same cycle (write followed by read).

READ CYCLE

SYMBOL	PARAMETER	65161 -5	65161 -9	65161 -2	UNIT	VALUE
TAVAV	READ cycle time	70	80	90	ns	min
TAVQV	Address access time	70	80	90	ns	max
TAVQX	Address valid to low Z	10	10	10	ns	min
TELQV	Chip-select access time	70	80	90	ns	max
TELQX	$\overline{CS}$ low to low Z	10	10	10	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	35	35	ns	max
TGLQV	Ouptut Enable access time	40	40	60	ns	max
TGLQX	$\overline{OE}$ low to low Z	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	35	35	ns	max

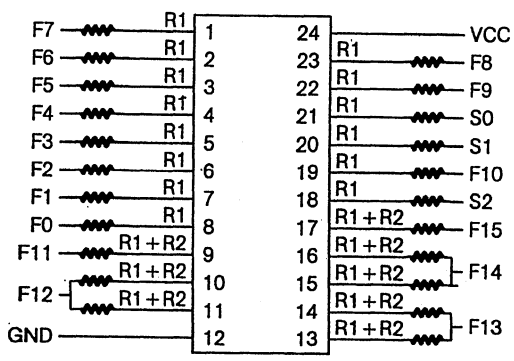
READ CYCLE



ORDERING INFORMATION

Package	Device type	Level
HM1	65161	– 5
0 - Chip form 1 - Ceramic 24 pins 3 - Plastic 24 pins 4 - LCC 32 pins	2 k x 8 general purpose static RAM	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

BURN-IN SCHEMATICS



R1 = 220 Ω per row
R2 = 2.2 KΩ per driver

Fo = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write / read cycles

VCC = 5.5 V

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SMART MEMORIES

8

MHS

DATA SHEET

HM 65231

2K x 8 CMOS DUAL PORT RAM

FEATURES

- **HIGH SPEED, FAST ACCESS TIME :**
  COMMERCIAL : 80 ns max
  INDUSTRIAL : 100 ns max
  MILITARY : 120 ns max
- **STANDBY CURRENT : 3 mA**
- **OPERATING SUPPLY CURRENT : 60 mA max**
- **BATTERY BACK UP OPERATION :**
  2V DATA RETENTION
- **ONE SEPARATE ADDRESS/DATA PORT,**
  ONE MULTIPLEXED ADDRESS/DATA PORT
- **3 PROGRAMMABLE ARBITRATION MODES ON CHIP**
- **INT AND BUSY OUTPUTS**
- **FULLY STATIC OPERATION**
- **TTL COMPATIBLE INPUT/OUTPUT**
- **SINGLE 5V +/ - 10 % POWER SUPPLY**

DESCRIPTION

The HM 65231 is a CMOS 2K x 8 high-speed Dual Port Static RAM. This state of the art technology used to fabricate it, combined with innovative circuit design techniques provides high speed access times together with excellent low power performance.

The HM 65231 provides two ports with controls, address and I/O. Port X is compatible with general purpose buses with separate address and data ; Port Y is directly compatible with a CPU providing multiplexed address and data. It is then possible to interconnect a CPU (type 8088 or 6809) or a microcontroller (type 8051) with a general purpose bus or a local bus without additional logic. Due to input buffers with gated inputs, the CE control pin permits the respective port to go into a standby mode when not selected (CE high).

Three programmable arbitration modes are available to resolve any contention with the maximum of efficiency. This allows the interconnection of two buses using READY signals or a bus with a READY signal to a bus without wait state capability (8051-). In both cases, the access arbitration is totality software transparent.

The third mode is a general purpose mode based on a software controlled flag.

Dependin upon the programmed mode, the memory locations 7FE and 7FF are defined as standard memory words or as two 8-bit flag registers. It is then possible to implement up to 16 concurrent communication channels with error free handshaking.

Two internal interrupt request flags are provided. Each flag is set or reset when memory locations 7FE or 7FF are accessed.

LITERATURE

Data sheets, application notes (ref. : AN1033, AN1034) and user's manuals are available upon request. Contact your sales office or representative.

DATA SHEET

HMC-6207

CMOS DUAL-PORT RAM CONTROLLER

FEATURES

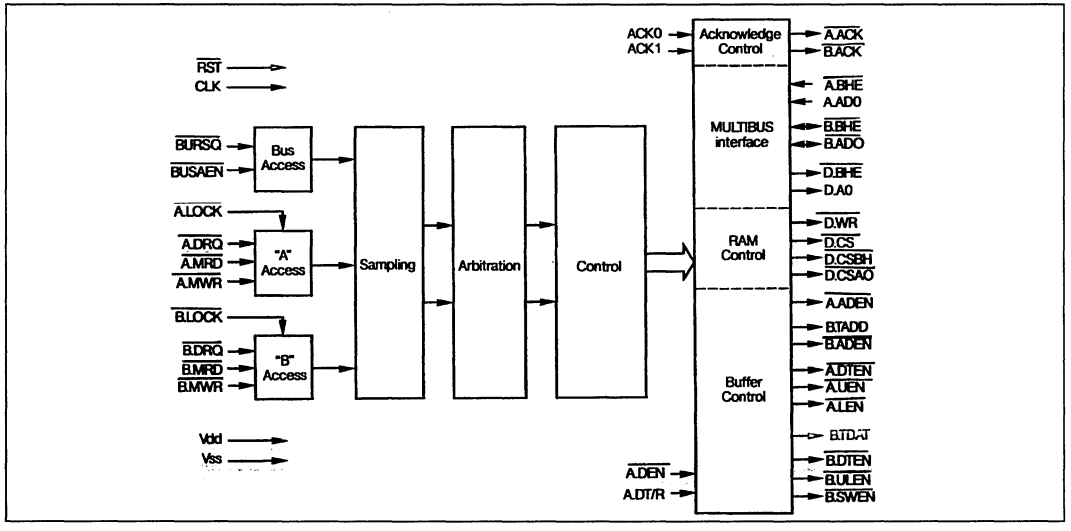
- MANAGES RAM ACCESSES FROM TWO INDEPENDENT PROCESSORS
- RAM SIZE MAY BE 8 OR 16-BITS IRRESPECTIVE OF PROCESSORS
- DIRECT INTERFACING TO 80C86, 80C88 MICROPROCESSOR FAMILY
- PROCESSOR WORD SIZES MAY BE MIXED, 8 OR 16-BITS
- CONTROL OF ALL ADDRESS/DATA BUFFERS FOR BOTH PROCESSORS
- GENERATION OF SEPARATE ACKNOWLEDGE SIGNALS
- RAM BYPASS MODE OPTIMISED FOR USE WITH MULTIBUS SYSTEMS
- FABRICATED USING MHS HIGH-SPEED LOW-POWER CMOS TECHNOLOGY

DESCRIPTION

The Dual-Port RAM Controller from Matra-MHS Semiconductor allows the configuration of a block of memory shared between two independent processors.

The controller manages all accesses to this memory, carrying out both arbitration and priority assignment. Once an access is in progress, the controller generates all signals for the address and data bus buffers and the RAM selection, according to the access type, either 8 or 16-bits. When the data becomes available the controller sends an acknowledge signal to processor to complete the access.

FUNCTIONAL DIAGRAM



LITERATURE

Data sheets and application notes (ref : AN1029) are available upon request. Contact your sales office or representative.

APPLICATION NOTES

9

MHS

APPLICATION NOTE **AN1006**

CMOS STATIC RAM
TTL - CMOS INPUT - OUTPUT COMPATIBILITY

One of the feature of our CMOS static RAM is TTL compatibility. The inputs of CMOS Memories are not the same as the inputs found on TTL devices that most digital designers are familiar with.

If we look at our DC electrical characteristics,a parameter like VOH = 2.4 V min., seems too high. The goal of this note is to define a method of interfacing for customer application.

TTL GATE CHARACTERISTICS

Figure 1 shows the electrical schematifc of TTL and TTLG/S and TTL/S gates.

We shall mainly analyse TTL/CMOS interfacing : the approach for other families will be the same.

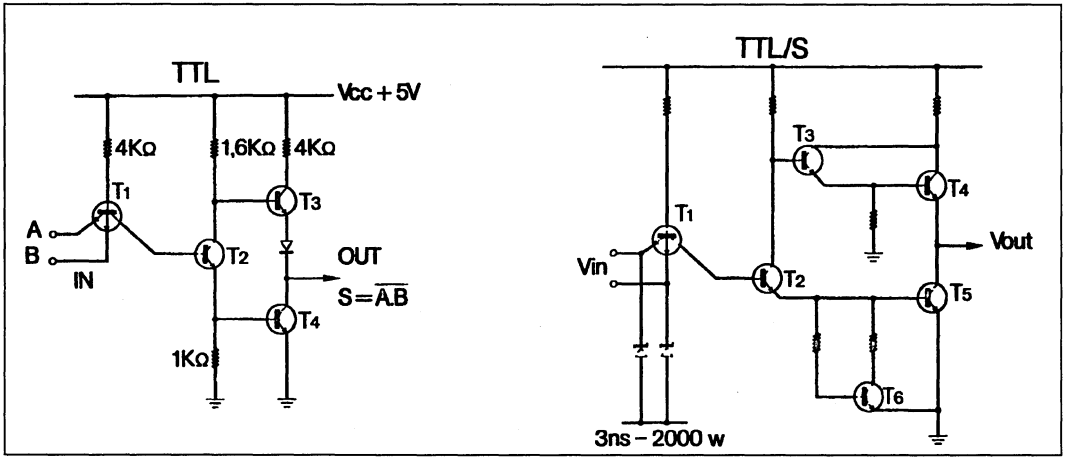


Figure 1.

1. INPUT CHARACTERISTICS

1.1 HIGH LEVEL (1) :

VIH min = 2 V.
If we look at *(figure 2)*, the only consumption is the emitter-base current of transistor T1. This I_{IH} current is in the range of 40 µA.

1.2. LOW LEVEL (0) :

VIL max = 0.8 V.
Transistor T1 is now conducting and the consumption is in the range of 1.6 mA.

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2. OUTPUT CHARACTERISTICS

(fig. 2) shows two series TTL gate.

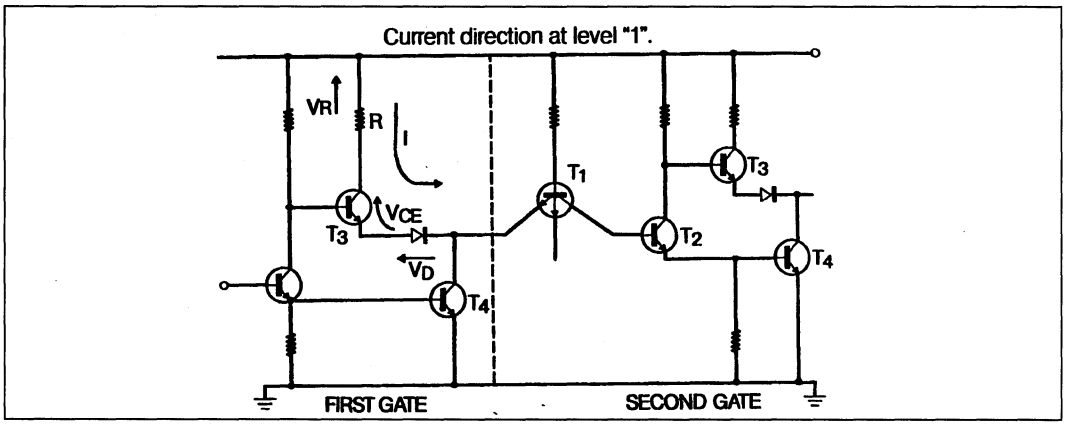


Figure 2.

2.1 HIGH LEVEL (VOH)

Transistor T4 is biased off. The only consumption is the reverse junction current consumed by the emitter of T1. This current is in the range of 40 µA. T3 can dissipate a current of about 800 µA.

We can write : VOH = Vcc – Vr – Vce – Vd

and VOH = Vcc – Ri – Vce – Vd

We see that VOH is directly proportional to the current consumed by the next row.

The higher the current, the closer VOH will be to 2.4 V (VOH min.).

2.2 LOW LEVEL (VOL)

Transistor T4 is saturated (fig 3)g. The only current is that delivered by T1 of the next row ; value is again in the range of 1.6 mA.

Transistor T4 sinks 16 mA (fan-out of 10). The Vce sat of T4 is about 0.4 V.

In fact VOL is equal to saturation voltage of T4 : 0.4 V.

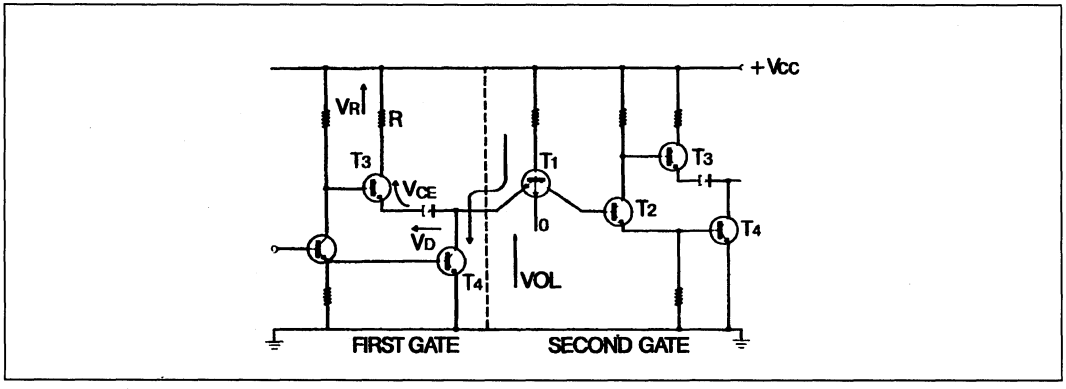


Figure 3.

3. OTHERS CHARACTERISTICS

Following the analysis of input/output characteristics seen above, we can easily calculate :

- the minimum noise immunity voltage
- the maximum fan-out.

3.1 NOISE IMMUNITY

High level : VIH = 2 V min. VOH = 2.4 V min. noise immunity : 0.4 V

Low level : VIL = 0.8 V max. VOL = 0.4 V max. noise immunity : 0.4 V

NOISE IMMUNITY IS 400 mV min. IN TTL MODE.

3.2 FAN-OUT

High level : If we look again at *fig. 3* we can see that the reversed bias of T1 can absorb 40 µA and T3 can deliver a current 1/3 800 µA.

Fanout at high level $1/3 \frac{800}{40}$ 1/3 20

Low level : T1 can deliver 1.6 mA, T4 can absorb 16 mA.

Fan-out at low level $= \frac{16}{1.6} = 10$

THE FAN-OUT OF A TTL GATE IS 10.

Table 2.

SERIES	LOGIC LEVEL	INPUT CURRENT	OUTPUT CURRENT
54/74	H L	40 µA 1.6 mA	400/800 µA 16 mA
54 H/74 H	H L	50 µA 2 mA	500 µA 20 mA
54 L/74 L	H L	10 µA 0.18 mA	100 µA 2 mA
54 LS/74 LS 54 LS 74 LS	H L L	20 µA 0.36 mA 0.36 mA	400 µA 5 mA 8 mA
54 S/74 S	H L	50 µA 2 mA	1000 µA 20 mA

CMOS GATE CHARACTERISTICS

(Fig. 4) shows a standard CMOS inverter.

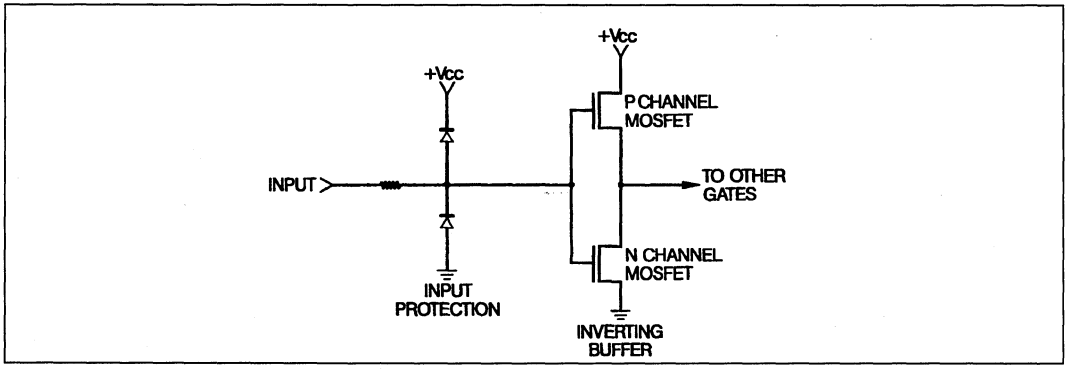


Figure 4.

9

Table 1.

CHARACTERISTICS	54 S/74 S	54 H/74 H	54/74	54 LS/74 LS	54 L/74 L	DTL	UNIT
Power Supply	5	5	5	5	5	5	V
High Level Input VIH Min	2	2	2	2	2	1.8	V
Low Level Input VIL Max	0.8	0.8	0.8	0.8	0.7	1.1	V
High Level Output VOH Min for IOH Max	2.7	2.4	2.4	2.7	2.4	2.5	V
Low Level Output VOL Max for IOL Max	0.5	0.4	0.4	0.5	0.3	0.5	V
Lowest Noise Immunity (high level)	700	400	400	700	400	500	mV
Highest Noise Immunity (low level)	300	400	400	300	400	450	mV
Fan-out	10	10	10	10	10	8	
Maximum Power Dissipation (25°) with 50% Duty Cycle	19	23	10	2	1	8	mW
Transition Time from Low to High Level	3	8	2	8	35	60	ns
Transition Time from High to Low Level	3	6	8	10	31	20	ns
Propagation Delay (average value)	3	6	10	10	33	25	ns
Signal Rise Time	3	9	18	22	70		ns
Signal Fall Time	3	5	6	8	20		ns
Quality Factor	57	138	100	20	33	200	pJ

The input circuit on CMOS devices is an inverting buffer stage with a protection network added against electrostatic discharge. A representative input buffer is shown in fig. 4. The FETs are both enhancement mode devices, which means that there is no current flow from the drain to the source unless the gate voltage is above threshold. With on P-FET and one N-PET in this complementary configuration, the output of the inverter is switched between Vcc and ground, but there is no current path from Vcc to groud because when one device is conducting the other device is biased off.

The input protection network protects the MOSFET gate dielectric from static damage. The purpose of the diodes is to clamp the input voltage of the gate. The gates are capacitive, so the resistor will cause an RC delay time to slow the rise of an applied potential and give the diodes the time to turn on and protect the gates. The inverter will not allow any current to flow from Vcc to ground (except leakage current) because of the complementary design. With a low input voltage, VIL, the N-FET is biased off and the P-FET is on. The output is pulled high by the P-FET but no current flows directly from Vcc to ground. The opposite condition occurs with a high input. The N-FET is on the P-FET is off the output is pulled low, but there is still no direct current path from Vcc to ground. When an input is taken to an inter-mediate voltage, between 1.5 V and 3.5 V, both the N-FET and the P-FET will be partially conducting. There will be a dc path from Vcc to ground until the input is taken either high enough to fully bias off the P-FET, or low enough to turn off the N-FET.

1. INPUT CHARACTERISTICS

Like described above, whatever the level (high or low), there is no conduction between the gate and the source of a CMOS transistor.
The only consumption is a leakage current due to parasitic current caused by parasitic capacitance. The value of this current is very low : < 1 µA.
Whatever the temperature range and Vcc value we can say :

VIH min. = Vcc 2 V
VIL max. = 0.8 V

2. OUTPUT CHARACTERISTICS

2.1. HIGH LEVEL

We can compare a MOS transistor in a saturated state to a resistor. The resistance depends on the structure of the channel. *(fig. 5)*
The schematic of Fig. 5 shows the equivalent output circuit in a high state : VOH = $V_{CC} - R_{DS1} \times I$. Transistor T2 is biased off. The total current will depend on the value of R_{DS1}.

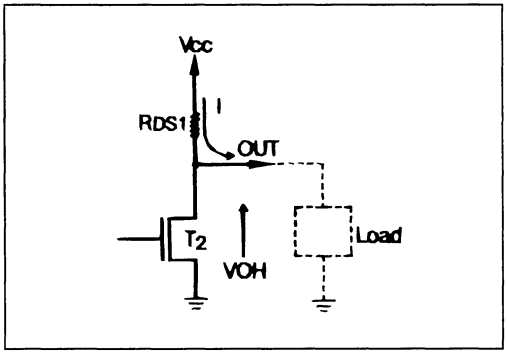


Figure 5.

If we look at the DC characteristics of a CMOS RAM (ex. 6514) for VCC = 4.5 V.
VOH = 2.4 V for IO = 1 mA (load current).
We can easily deduce the value of R_{DS1} :

$$VOH = VCC - RDS1 \times IO$$

and

$$RDS1 = \frac{VCC - VOH}{IO} = \frac{4.5 - 2.4}{10-3} = 2.1\ k\Omega$$

R_{DS1} = 2.1 KΩ

Conditions when the loads is an other CMOS circuit
The only current that flows through R_{DS1} is the input leakage current of the second circuit : ≈ 1 µA.
We can write :;
$V = R_{DS1} \times I = 2.1 \times 10^3 \times 10^{-6} = 2.1$ mV and
$VOH = 4.5 - 2.1 \times 10^3 = 4.4979$ V

VOH ≈ 4.50 V

VIH condition is : ≥ Vcc– 2 V (≥ 2.5 V).
Conclusion : no problem for CMOS interfacing at high level.
Conditions when the load is a TTL circuit
The current that flows through R_{DS1} will be the reverse junction current of T1 (≥ 40 µA).
We can write :
$V = R_{DS1} \times I = 2.1 \times 10^3 \times 40.10^{-6} = 84$ mV
and $VOH = 4.5 - 84 \times 10^{-3} = 4.416$ V

VOH ≈ 4.40 V

VIH condition is : ≥ 2 V.
Conclusion : no problem for TTL interfacing at high level. TTL noise immunity will not create any problems En > 400 mV (4.416 – 2 = 2.416 V).

2.2 LOW LEVEL

The schematic of *fig.6* shows the equivalent output circuit in a low stat. VOL = $R_{DS2} \times I$.
Transistor T1 is biased off; no current will flow through R_{DS2}, unless the load supplies this current.

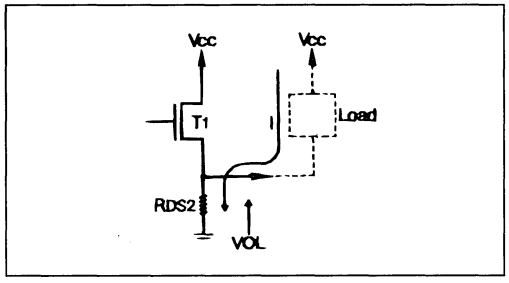


Figure 4.

If we look at the DC characteristic of CMOS RAM (6514 for example), for VCC = 4.5 V, we have :
VOL = 0.45 V for IO = 2 mA and

$$R_{DS2} = \frac{0.45}{2 \,.\, 10-3} = 225\ \Omega$$

Conditions when the load is an other CMOS circuit
The only current that flows through RDS2 is the leakage current of the second circuit : ≈ 1 µA.

DC ELECTRICAL CHARACTERISTICS (6514)

SYMBOL	PARAMETER	TEMP. & V_{CC} OPERATING RANGE		TEMP. = 25°C1 V_{CC} = 5.0 V	UNIT	TEST CONDITIONS
		MIN.	MAX.	TYPICAL		
ICCSB	Standby Supply Current		50	1.0	µA	IO = 0 VI = V_{CC} or GND
ICCOP	Operating Supply Current 2		7	5	mA	f = 1 MHz, IO = 0 VI = V_{CC} or GND
ICCDR	Data Retention Supply Current		25	0.1	µA	V_{CC} = 2.0,IO = 0 VI = V_{CC} or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
II	Input Leakage Current	– 1.0	+ 1.0	0.0	µA	GND ≤ VI ≤ V_{CC}
IIOZ	Input/Output Leakage Current	– 1.0	+ 1.0	0.0	µA	GND ≤ VIO ≤ V_{CC}
VIL	Input Low Voltage	– 0.3	0.8	2.0	V	
VIH	Input High Voltage	V_{CC} – 2.0	V_{CC} + 0.3	2.0	V	
VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0 mA
VOH	Output High Voltage	2.4		4.0	V	IO = – 1.0 mA
CI	Input Capacitance 3		8.0	5.0	pF	VI = V_{CC} or GND : = 1 MHz
CIO	Input/Output Capacitance 3		10.0	6.0	pF	VIO = V_{CC} or GND : = 1 MHz

We can write :

$VOL = R_{DS2} \times I = 225.10^6$

VOL ≈ 0,2 mV (negligible).

VOL condition is ≤ 0.8 V.

Conclusion : no problem for CMOS interfacing at low level.

Conditions when the load is a TTL circuit

The current that flows through R_{DS2} will be the T1 transistor current *(see fig. 6)* of the TTL circuit. This current is in the range of ≈ 1.6 mA.

We can write :

$VOL = R_{DS2} \times I = 225 \times 1.6.10 = 360$ mV

VOL = 360 mV.

VIL condition is ≤ 0.8 V

Conclusion : no problem for TTL interfacing at low level with a noise immunity > 400 mV (800 360 = 440 mV).

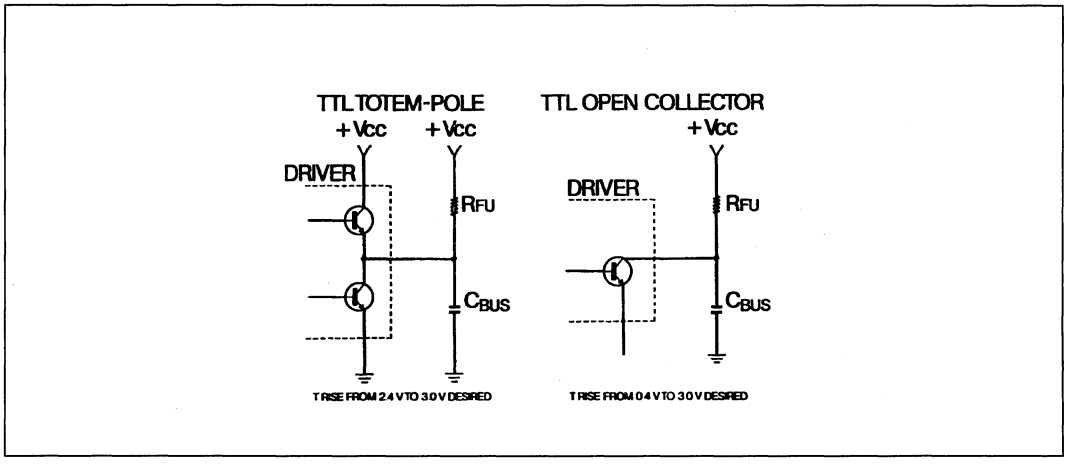
9

The CMOS static RAMS from MHS are :
- CMOS input/output, compatible with a CMOS noise immunity > 30% Vcc.
- TTL output compatible with a TTL noise immunity ≈ 400 mV.
- TTL input compatible with pull-up resistors.

To guarantee high logic levels and noise margins, TTL buffers require external pull-up resistors. The value of the resistor is chosen by an RC based decision. The bus capacitance, and the allowable time for reaching VIH, determine the resistor value. If the system speed is very slow, the pull-up resistor can be chosen to supply the bus leakage currents while maintaining a VIH of at least 3.0 volts (Vcc 2.0 volts). *Figure 7* shows the basic circuit models and equation used.

Another possible choise for array bus driver is open collector TTL buffers. As in the case of standard totem pole bus drivers, the pull-up resistor is chosen by an RC and time based equation. The difference is that the open collector pull-up, must pull up from a low logic level ; where the totem pole resistor pull-up, only pulls from the TTL output high level, up to the CMOS input high level. The pull-up speed is slower with open collector than with standard TTL. Due to the slower pull-up open collector than with standard TTL. Due to the slower pull-up, open collector TTL drivers are normally used only in systems having separate power supplies for the TTL and CMOS sections of the systems.

(Fig. 7) - Choosing bus pull-up resistors.



9

BATTERY BACK-UP SOLUTION AND APPLICATION

SUMMARY

- USING A BATTERY WITH A VOLTAGE LESS THAN THAT OF THE MAIN POWER SUPPLY.
- BATTERY CHARGER USING A CONSTANT CURRENT SUPPLY WITH AUTOMATIC CUT-OFF AT FULLCHARGE.
- PROTECTION AGAINST MAIN POWER SUPPLY FAILURE.

I - DESCRIPTION OF BATTERY BACK-UP SYSTEM

1.1 BLOCK DIAGRAM

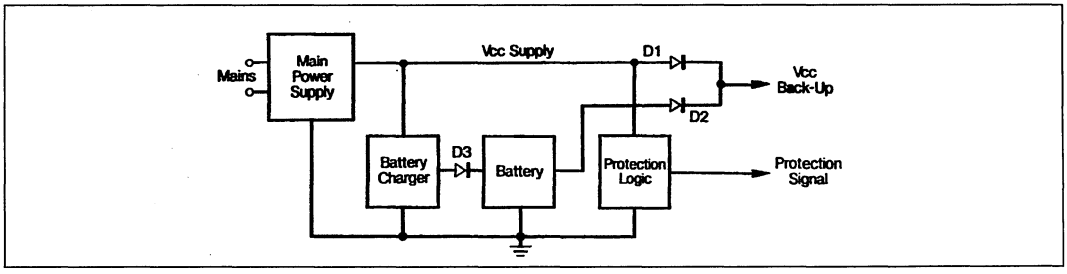


Figure 1.

1.2 BATTERY CHARGER

A - DESCRIPTION

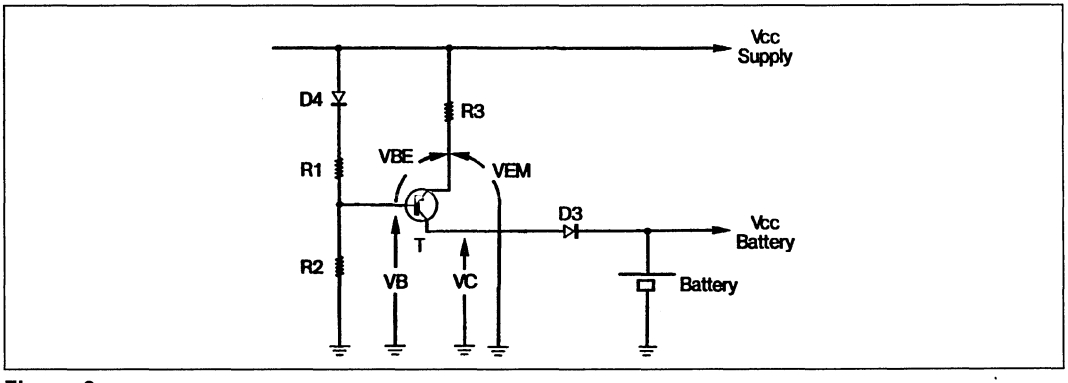


Figure 2.

B - OPERATION

The charger is composed of a current generator formed by the transistor T (PNP) and its biasing components. The diode (D4) and resistors (R1, R2) fix the base voltage (VB) to the output voltage of the battery. The current that flows in the chain is of the order of 5 mA.
The emitter voltage of the transistor (VE) :
VE = VBE + VB (VBE = 0.6 V).
Resistor R3 determines the charging current which, in turn, is dependent upon the battery characteristics. The diode (D4) compensates for Δ VBE of the transistor with temperature changes.
The battery charges until VC ≈ VE, where cut-off occurs.
The germanium diode, D3 (having a low voltage-drop), isolates the battery from the charger.
Diodes D1 and D2 (also germanium), isolate the battery and the main power supply from each other.

1.3 PROTECTION AGAINST POWER-OFF AND POWER-ON

A - OVERVIEW

• **Poweroff**

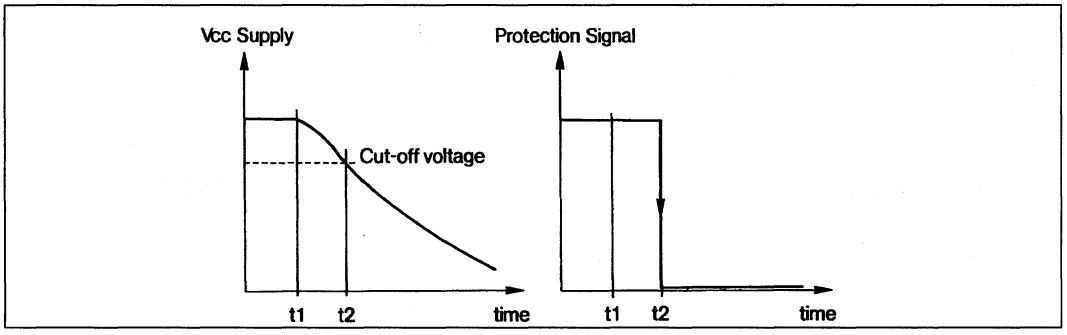


Figure 3.

During power-off conditions the protection signal must be active from the time the main power supply voltage drops below the limiting threshold, which is fixed by the cut-off circuitry. This will depend upon the components used.

• **Power-on**

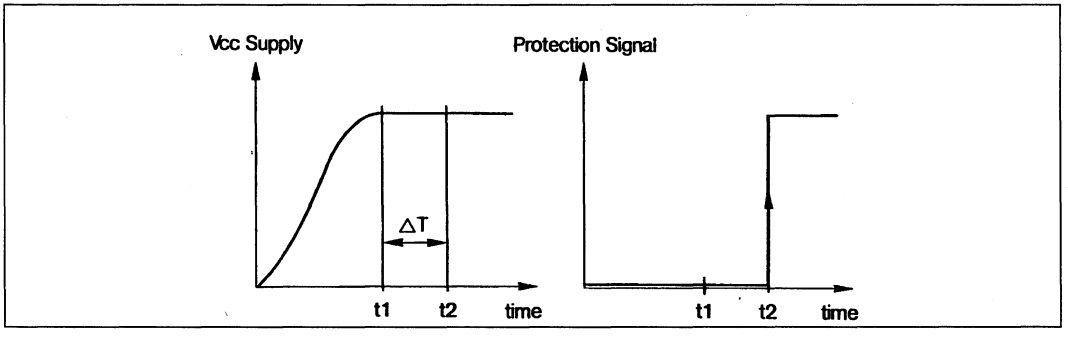


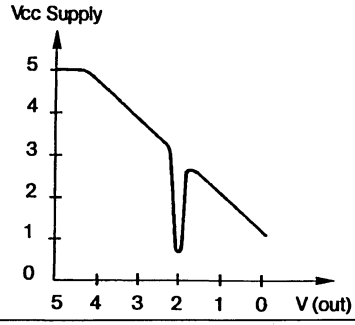
Figure 4.

At power-on the protection signal must be active until the main power supply is stable. Any random functioning must be avoided. The time ΔT allows a safety margin.

• **Introduction**

The only stable reference during power supply transitions is ground, hence the protection signal is active low.
The protection logic is not powered by the battery so as to reduce the current drawn to a minimum.
The protection logic must have a good noise immunity (CMOS advised) so that it is not affected by any disturbances.

The threshold value must not be too close the power supply voltage (to allow voltage fluctuations) nor too close to ground to cause failure of circuits that are not adequately supplied.



Behaview of decored output as a fonction ofpower supply (type 745 138)

Figure 5.

B - CIRCUIT OVERVIEW

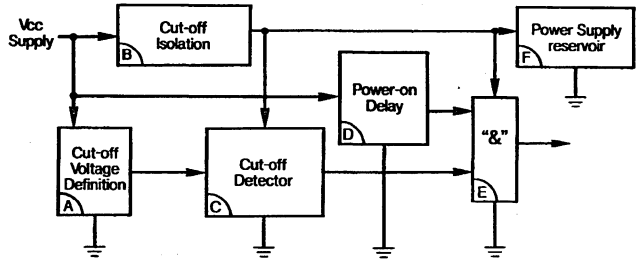


Figure 6.

The system is constructed around a Schmidt trigger (c) built using PNP transistors. This triggers around the cutoff voltage defined by circuitry (A). A power supply reservoir (F) allows the detector to continue operating under normal conditions. The supply isolation (B) stops the rest of the circuitry from draining the supply reservoir (F) when the power is cut-off. The protection signal is obtained by an "AND" (E) between the signals provided by the cutoff detector (C) and the power-on delay (D). This is a low power CMOS gate.

C - CIRCUIT DIAGRAM

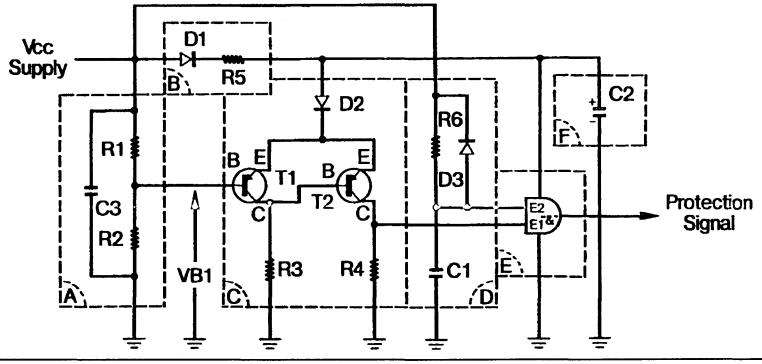


Figure 7.

• Normal operation

Transistor T1 is cut-off, its base voltage being higher than its switching threshold.

Switching threshold = VCC Supply – VD1 – VD2 – VBE1
= VCC Supply – 0,9 V

The quiescent base voltage, VB1, is fixed around the limiting power supply voltage during power-off (cut-off voltage : VCP).

So that :

$$VB1 = \frac{VCC\ Supply\ (VCC\ Supply - VEB1 - VD2 - VD1)}{VCP}$$

Since T1 is not conducting, the base of T2 is pulled towards ground accross R3, hence the transistor T2 turns on and becomes saturated.

VE2 – VCC – VD1 – VD2
VB2 – VE2 – VBE2
VR4 ≈ VCC Supply – VD1 – VD2 – VCE2

• Power off

VCC Supply falls and reaches the limiting voltage VCP. The trigger threshold is reached so that T1 saturates. VR3 increases cutting off T2. The input E1 of the "AND" gate is at logic zero so that the protection signal becomes active. The supply reservoir, C2, maintains the emitter voltage levels until cut-off detection. It discharges across the equivalent resistance Req.

$$Req = \frac{VC2}{IC1} \quad \text{where } IC1 \approx IE1 \approx IE2$$

• Power on

The protection signal depends only upon the network formed by R6 and C1. (R6.C1 ≥ risetime of the power supply, VCC Supply). This network intro duces a delay.

= R6.C1 = 5.tLH of VCC Supply

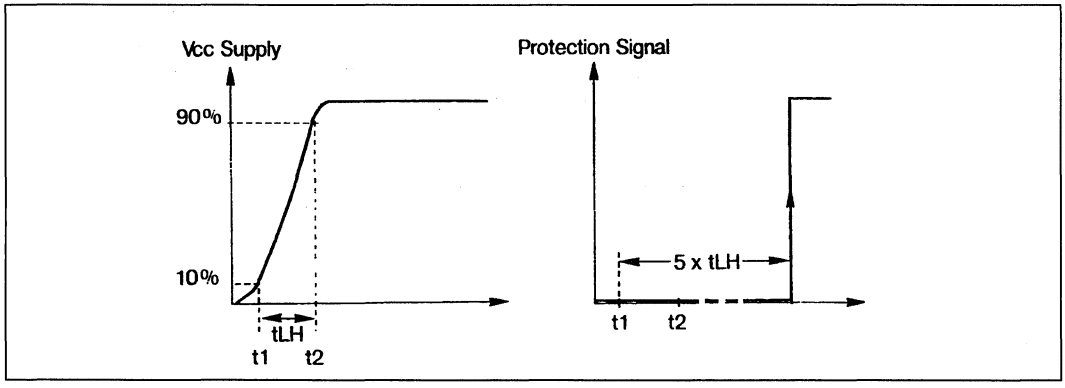


Figure 8.

The diode in parallel with R6 (D3) discharges C1 during power-off. It also the system to react efficiently whenever the power-off period is less than the time constant R6.C1.

9

II - APPLICATION USING A 16K BYTE MEMORY BLOCK WITH BATTERY BACK-UP

2.1 PRESENTATION

This application allows :
- Selection of a single 2Kx8 RAM of a 16K byte block located in a 64K byte page.
- Access time of 140 nS (time between a read request and the data).
- Decoder protection during power-on and power-off.
- Constant current battery charger with automatic cu-toff at full charge.
- Data retention of one month with a battery of 100 mAH.

2.2COMPONENTS USED

A - MEMORY

2K byte static asynchonous CMOS RAMs, ref. HM651615 *(see appendix 2).*

B - MEMORY DECODER

3.8 CMOS decoder, ref. HD-6440 *(see appendix 2).*

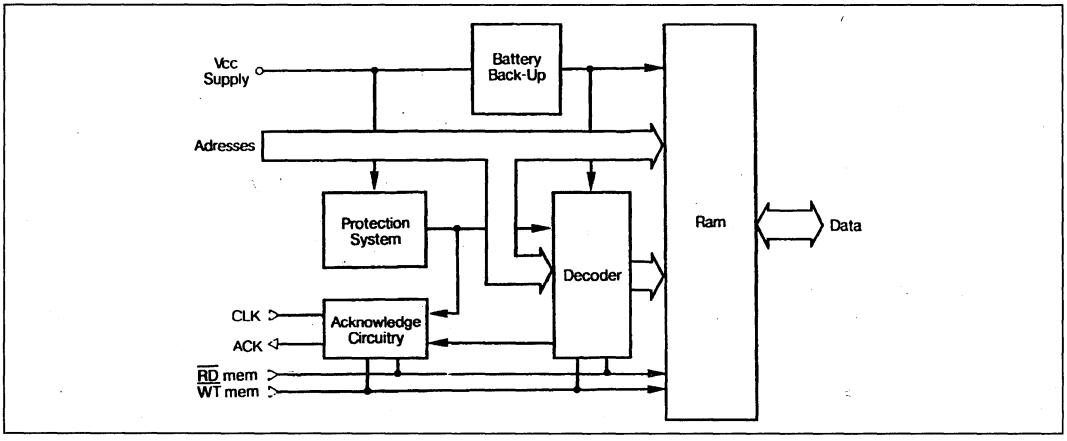


Figure 9.

C - BATTERY Capacity 100 mAh
Charge current 4 mA Voltage output 2 ↔ 4.65 V

2.3 BATTERY BACK-UP SYSTEM

A - CIRCUIT DIAGRAM

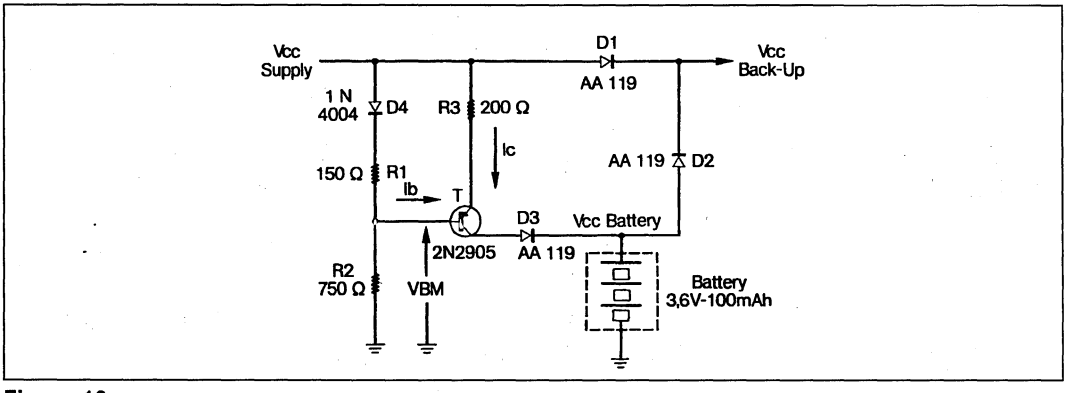


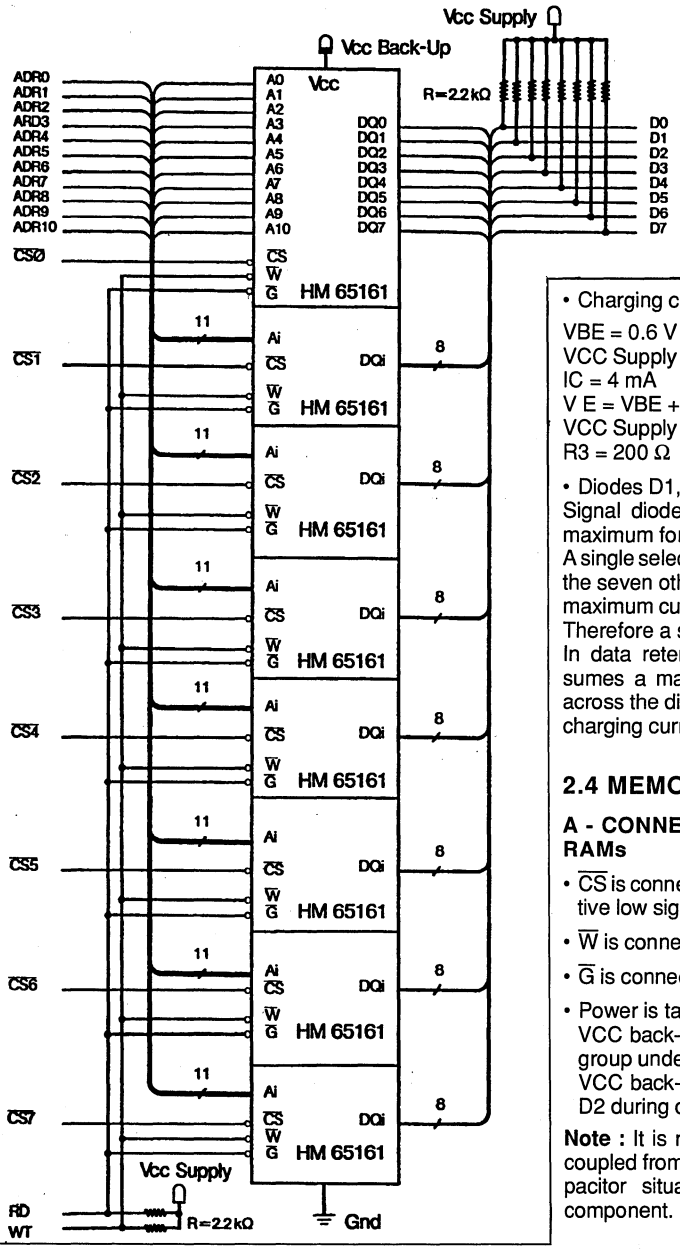
Figure 10.

B - OPERATION

• Biasing of transitor (type 2N2905)

VB = battery E.M.F. = 3.6 V
Ip = 5 mA (current necessary in D4)
Diode voltage drop = 0.6 V (type 1N4004)

VCC Supply = 5 V
VCC Supply = VD + (R1 + R2), Ip (IB negligeable)
VB = R2.Ip
R2 = 750 W R1 = 150 W



• Charging current

VBE = 0.6 V
VCC Supply = 5 V
IC = 4 mA
V E = VBE + VB
VCC Supply = R3.IC + VE
R3 = 200 Ω

• Diodes D1, D2, D3.
Signal diodes (germanium) type AA119, with a maximum forward current of 100 mA.
A single selected memory circuit consumes 60 mA, the seven others consume 7 x 100 µA, so that the maximum current across the diode D1 is 60.7 mA. Therefore a single AA119 is sufficient.
In data retention mode the memory bank consumes a maximum of 8 x 100 µA, which flows across the diode D2. The current across D3 is the charging current which is a maximum of 4 mA.

2.4 MEMORY BANK

A - CONNECTION OF THE HM-65161-5 RAMs

- $\overline{CS}$ is connectd to one of the decoder outputs, active low signal.
- $\overline{W}$ is connected to the write signal, active low.
- $\overline{G}$ is connected to the read signal, active low.
- Power is taken from VCC back-up.
  VCC back-up = BCC Supply – VD of the diode group under normal conditions.
  VCC back-up = VCC Battery – VD of the diode D2 during data retention.

Note : It is recommended that each RAM is decoupled from the power supply using a 100 nF capacitor situated as close as possible to the component.

B - MEMORY BANK PROTECTION

- A study of the architecture of the HM-65161-5 RAM indicates that the CS signal must be protected during the switch from normal operation and back-up operation.
- The G and W inputs do not require any special attention.

C - RISING EDGE IMPROVEMENT

- The data bus and the read/write lines are pulled up to VCC Supply by resistors.

Capacitive load on these lines : 8 x 5 pF = 40 pF
Pull-up resistor value : 2.2 kΩ
(Application Note : 1006)

- The addresses appear earlier than the oter signals, so pull-up resistors are not necessary on these lines.

2.5 DECODING

A - USING THE HD-6440 DECODER

- The latch ($\overline{L1}$, $\overline{L2}$) is not used. So that $\overline{L1}$ = '0' and L2 = 1.
- The outputs of the decoder are used to select the RAMs ($\overline{CS}$), therefore it is sufficient to disable the decoder to deselect the memory bank. To do this protection signal is connected to the G3 input of the decoder ; it is also necessary to safeguard the decoder power supply.
- The ground (logic zero level) being the only reference for the two supplies (VCC Supply, VCC Battery), it is sufficient to apply this signal to the G3 input to deselect both the decoder and the RAM.
- $\overline{G2}$ = Selection (active low) of the memory bank.

B - SELECTION OF A MEMORY BANK WITHIN A 64K BYTE PAGE

- Using a 2 → 4 line decoder (type 74-S-139)
- Selection of memory bank address within a 64K byte page by jumpers.
- Selection of the decoder if the RAM valid signal is active.

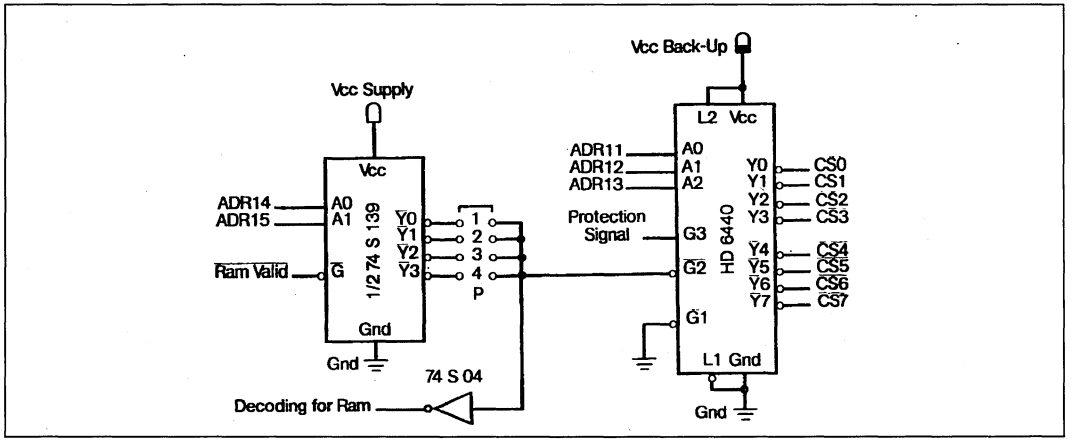


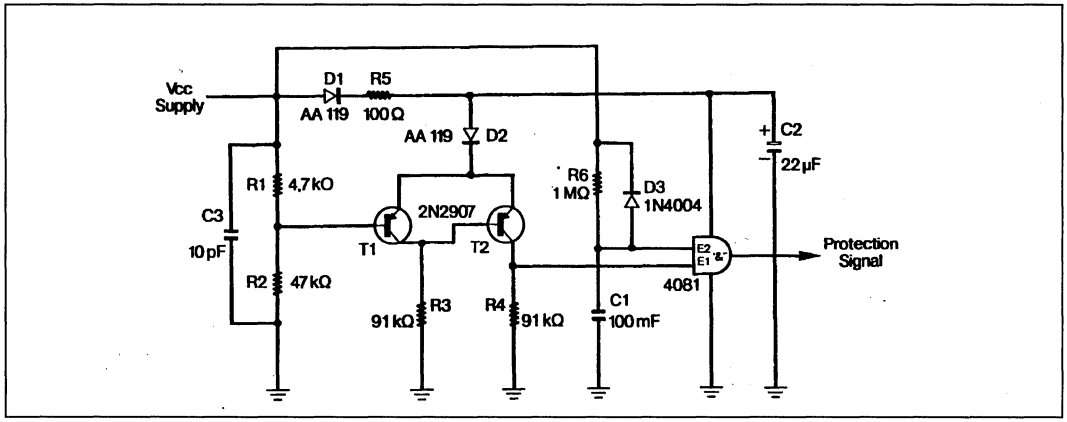
Figure 12.

2.6 PROTECTION SYSTEM

A - CHARACTERISTICS OF THE CONSTRUCTED SYSTEM

- VCC Supply = 5 V ± 5 %
- During power-off the time for the voltage to fall between VCC Supply and 37 % of this value is 240 mS.
- During power-on the risetime between 10 % to 90 % of VCC Supply is 20 mS.
- The cut-off voltage was chosen to be 4.5 V.

B - CIRCUIT DIAGRAM



C - OPERATION

- Input stage, (T1, R1, R2, R3, D1, D2, D5) D1 and D2 fix the potential VE of transistor T1 (VR5 negligeable VE = VCC Supply VD1 VD2 = 4.7 V
  The current IC1 of T1 is chosen to be small, IC1 ≈ 50 µA, to have low power consumption and to obtain a small value of C2, the reservoir capacitor. The chain R1 and R2 fixes the threshold of the trigger.

$$VB1 = \frac{VCC\ Supply\ (VCC\ Supply - VD1 - VD2 - VBE1)}{VCP}$$

$= 4.55\ V$

The current across R1 and R2 must be greater than IB1.
IR1 ≈ 100 IB1 ⇒ IR1 ≈ IR2
IB1 ≈ 1 µA ⇒ IR1 ≈ 100 µA

Note : If IR1 ≥ IB1 the noise immunity will be greater because the circuit is voltage sensitive. The capacitor C3 permits filtering of VB1.

- $R1 + R2 = \frac{VCC\ Supply}{IR1} = \frac{5}{100 \times 10^{-6}}$ R1 + R2 = 50 KΩ

- $R2 = \frac{VB1}{IR2} = \frac{4.5}{100 \times 10^{-6}} = 45.5\ k\Omega$

R2 = 45.5 kΩ standardised to 47 kΩ
R1 = 4.5 kΩ standardised to 4.7 kΩ

- $R3 = \frac{VE - VCE1}{IC1} = \frac{4.7 - 0.2}{50 \times 10^{-6}} = 90\ kW$

R3 = 90 kΩ, standardised to 91 kΩ.

Capacitor C3 serves as a small filter and has a value of 10 pF.

Resistor R5 limits the current through diode D1 that charges C2.

R5 = 100 Ω

- Operation of the output stage (R4).
  The current IC2 of transistor T2 is also small to keep consumption low and limit the value of C2. IC2 ≈ 50 µA.

$$R4 = \frac{VE - VCE2}{IC2} = \frac{4.7 - 0.2}{50 \times 10^{-6}} = 90\ k\Omega$$

R4 = 90 kΩ, standardised to 91 KΩ.
Under normal operation : VR4 ≈ R4. IC2 = 4.5 V
Therefore VR4 effectively correcponds to a logic one level for the E2 input of the 'AND' gate.

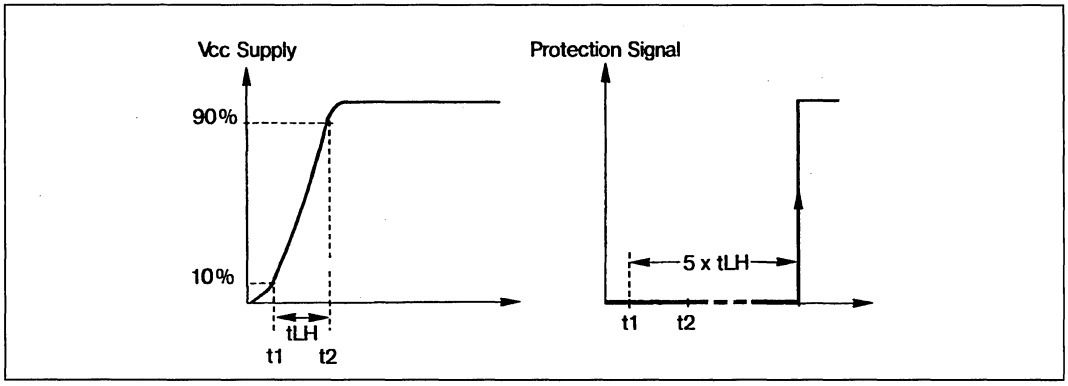
- Voltage reservoir operation.
  Capacitor C2 charges via D1 and R5. Whenever VCC Supply falls, C2 supplies power for the system. Diode D1 cuts off and isolates C2 from the main power supply. C2 discharges across T1 and R3, other components drawing a negligeable current.
  τ = time constant for the power supply cut-off (τ = 240 mS).
  VE = VCC Supply VD1 VD2 = 4,7 V
  VCP = 4,5 V
  IC1 = 50 µA
  VEB = 0,6 V

$$C2 = \frac{0.9\ \tau\ IC1\ (1 - \frac{VCP}{VCC})}{VE - VBE - 0.9\ VCP}$$

C2 = 20.9 µF, standardised to 22 µF

9

• **Poweron delay operation**



tLH = 20 mS => Δt = 100 mS
VB : Logic one level, guaranteed for a 4081 AND gate, of 2.75 V.
VSS : Power supply for R6, C1
VSS = VCC Supply VD1 = 4.85 V.

$$VB = VSS \quad (I - e^{\frac{\Delta T}{R6 \cdot C1}})$$

$$R6 \cdot C1 = \frac{\Delta T}{\text{Log}_e \left(\frac{VSS}{VSS - VB} \right)} = 0.12\ S$$

If C1 = 100 nF, R6 = 1 MΩ.

The discharge current of C1 having a large peak, D3 must be of the type 1N4004.

D MODIFICATIONS FOR IMPROV ED TEMPERATURE STABILITY

The circuit, as it is at present, can have temperature related problems which show themselves by a shift of ≈ 180 mV of VCP (cut-off voltage) at 50 °C.
In this case a greater precision is necessary for VCP, the initial cirduit must be modified.

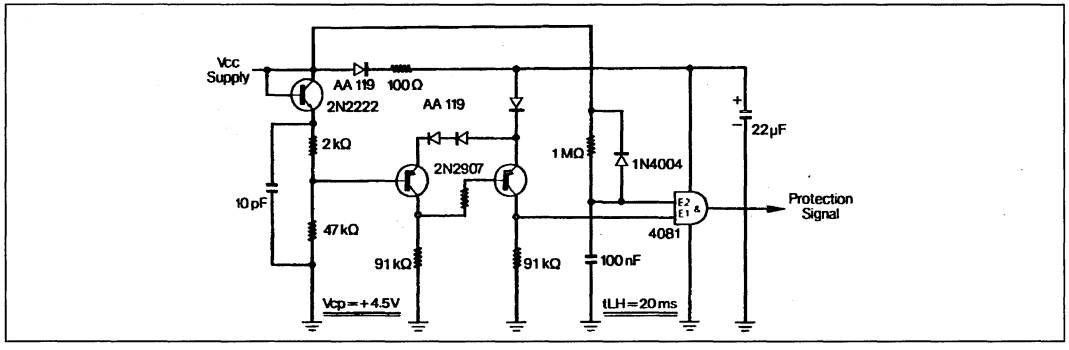


Figure 14.

2.7 RAM ACCESS ACKNOWLEDGE

A - NECESSARY CONDITIONS

- To have decoded the memory address
- To be in read or write operation
- To be not in the state where RAM is disabled and/or protected

The signal obtained must be sent to the bus line ($\overline{ACK}$), allowing the system controller to complete the cycle.

B - DELAY OF ACKNOWLEDGE

If compatible slow memories are used (HM-6516) it may be necessary to delay the ACK signal with certain high-speed microprocessors.

3. CONCLUSION

The method used may also be applied to other CMOS memories and other decoding systems.

The application of a 16K byte memory block an be extended to have greater capacity for 8,16 or 32 bit data buses. A recalculation of certain parameters will be necessary.

To delay the sending of $\overline{ACK}$ a counter is used in conjuction with CLK. The counter is enabled whenever a read or write to memory occurs.

The use of a non-rechargeable battery (such as lithium cells) is also possible, having a life of several years. In this case the circuit becomes simpler because the charger is no longer required.

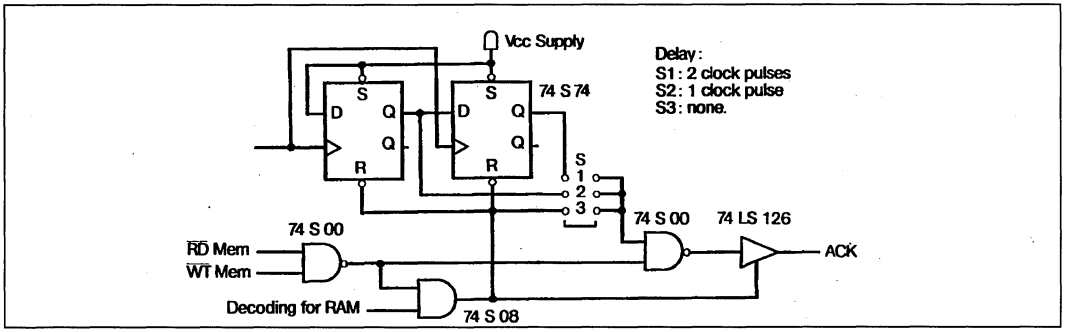


Figure 15.

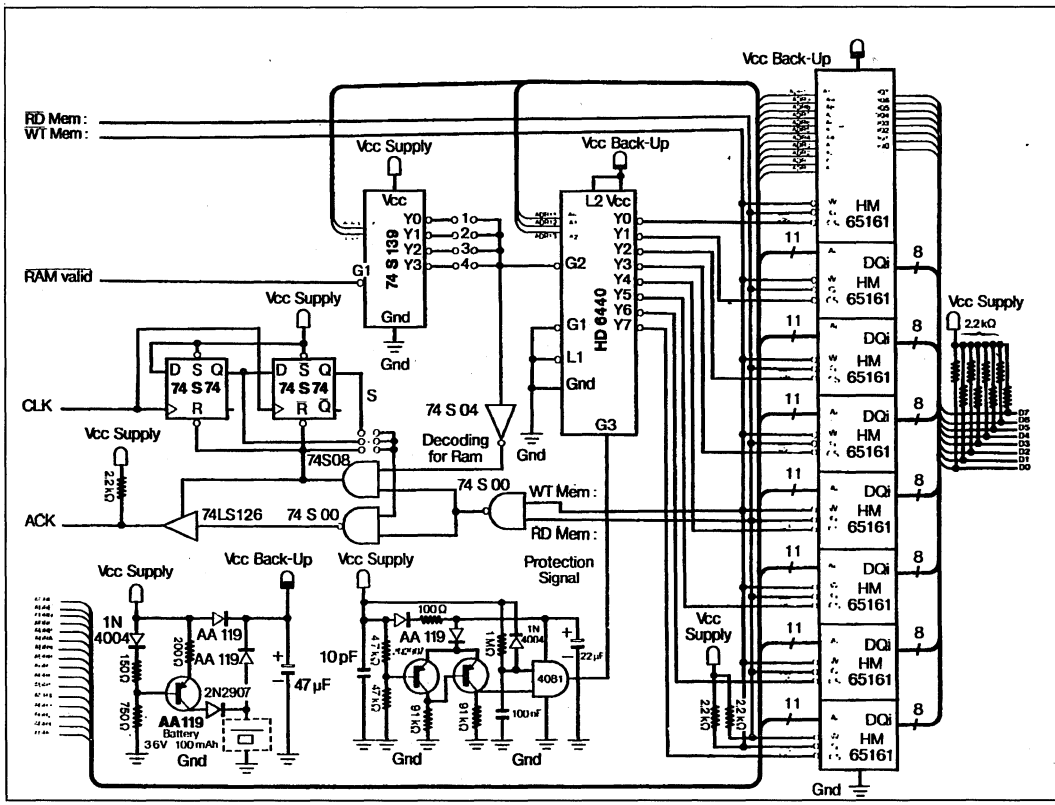


Figure 16.

PACKAGING

10

MHS

PRODUCT REFERENCES

DEVICE TYPE	PINS COUNT	PDIL 300 MILS	PDIL 600 MILS	CDIL 300 MILS	CDIL 600 MILS	SOIC	LCC	PLCC	SOJ
65687	22p	054	–	C33	–	*	*	–	*
65688	22p	054	–	C33	–	*	*	–	*
65664	28p	051	033	C31	C32	N10	L32	–	P03
65767	20p	034	–	C23	–	N01	L20	–	–
65768	20p	034	–	C23	–	N01	L20	–	–
65770	22p	053	–	C33	–	N02	–	–	–
65772	24p	043	–	C29	–	N02	–	–	–
65728	24p	043	03	C25	–	N02	L17	–	–
65787	22p	041	–	C33	–	N02	L23	–	P02
65788	22p	041	–	C33	–	N02	L23	–	P02
65789	24p	044	–	C29	–	N02	L15	–	P02
65790	28p	049	–	C31	–	N10	L15	–	*
65791	28p	049	–	C31	–	N10	L15	–	*
65764	28p	049	050	C31	C32	N10	L32	–	P03
65779	28p	049	–	–	–	N10	–	–	P03
65262	20p	X8	–	C1	–	–	L22	–	–
65162	24p	–	X3	–	5F	–	L17	–	–
65641	28p	–	X33	–	C20	–	L32	–	–
6116	24p	–	X3	–	5F	–	LU	–	–
65161	24p	–	X3	–	5F	–	LU	–	–
6207	40p	–	3J	–	5H	–	L09	K04	–
65231	48p	–	036	–	C21	–	L04	K01	–
65797	24p	*	–	*	–	*	*	–	*
65798	24p	*	–	*	–	*	*	–	*
65799	28p	*	–	*	–	*	*	–	*
65795	28p	*	–	*	–	*	*	–	*
65796	28p	*	–	*	–	*	*	–	*
65756	28p	*	*	*	*	*	*	–	*

* Contact your sales office.

STANDARD NOTES FOR PLASTIC D.I.L.

1 - Controlling dimensions : inches
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.

2 - Dimensioning and tolerancing per ansi y 14.5M-1982.

3 - Dimensioning A.A1. and L are measured with the package seated in jedec seatind plane gauge GS-3.

4 - D and E1 dimensions do not include mold flash or protusions. Mold flash or protusions shall not exceed .010 inch (0.25 mm).

5 - E and eA measured at the leads contrained to be perpendicular to the base plane.

6 - eB is measured at the lead tips with the leads uncontrained.

7 - Corner leads may be configured as shown in figure 2.

STANDARD NOTES OR CERAMIC D.I.L.

1 - Controlling dimensions : inches.
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.

2 - Dimensioning and tolerancing per ansi y 14.5M-1982.

3 - Dimensions A.A1. and L are measured with the package seated in jedec seatind plane gauge GS-3.

4 - E and eA measured at the leads contrained to be perpendicular to the base plane.

5 - eB is measured at the lead tips with the leads uncontrained.

6 - Corner leads may be configured as shown in figure 2.

7 - Leads within 0.127 radius of true position at gauge plane with MMC (maximum material condition) and unit installed.

STANDARD NOTES FOR PLCC

1 - Controlling dimensions : inches.
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.

2 - Dimensioning and tolerancing per ansi y 14.5M-1982.

3 - D and E1 dimensions do not include mold flash or protusions. Mold flash or protusins shall not exceed 0.25 mm (.010 inch).

STANDARD NOTES FOR S.O.

1 - Controlling dimensions : mm.

2 - Dimensioning and tolerancing per ansi y 14.5M-1982.

3 - D is a reference datum.

4 - A and B are reference datums and do not include mold flash or protusion. Mold flash and protusions shall not exceed 0.15 mm (.0086 inch).

5 - The chmfer h on the body is optional.

STANDARD NOTES FOR SO TYPE J

1 - Controlling dimensions : inches.

2 - Dimensioning and tolerancing per ansi y 14.5M-1982.

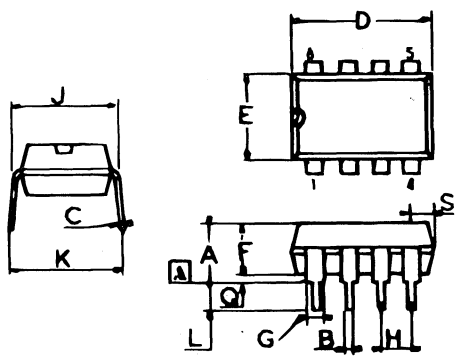
3 - Dim eA to be determine at seating plane .DATUM C.

4 - D and E dimensions do not include mod flash or protusions. Mold flash or protusions shall not exceed 0.15 mm (.006 inch).

PLCC PACKAGE DRAWING

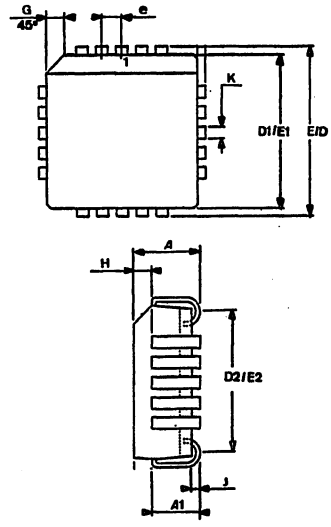
CODE : X39 8 PIN PLASTIC DIL

	MM dimens.		IN dimens.	
	min	max	min	max
A	3.81	5.08	1.50	.200
B	0.41	0.508	.016	.020
C	0.20	0.30	.008	.012
D	9.39	9.90	.370	.390
E (300)	6.22	6.73	.245	.265
F	3.25	3.94	.128	.155
G	1.27	1.78	.050	.070
H	2.29	2.79	.090	.110
J	7.37	7.87	.290	.310
K	7.62	9.65	.290	.380
L	2.92	3.81	.115	.150
Q	0.51	1.65	.020	.065
S	1.65	2.16	.065	.085



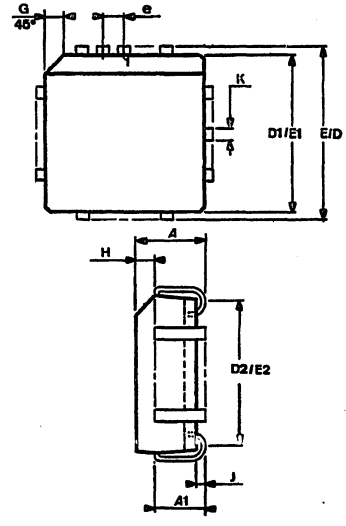
CODE : K04 44 PIN PLCC **REV : C**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	0.120
D	17.40	17.65	.685	.695
D1	16.51	16.66	.650	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.51	16.66	.650	.656
E2	14.99	16.00	.590	.630
e	1.27 B.S.C.		.050 B.S.C.	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	.0.51	–	.020	–
K	.0.33	.0.53	.013	.021
	PKG STD : 00			



CODE : K01 68 PIN PLCC **REV : E**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	0.13
D	25.02	25.27	.985	.995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
E	25.02	25.27	.985	.995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
e	1.27 B.S.C		.050 B.S.C.	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
	PKG STD : 00			



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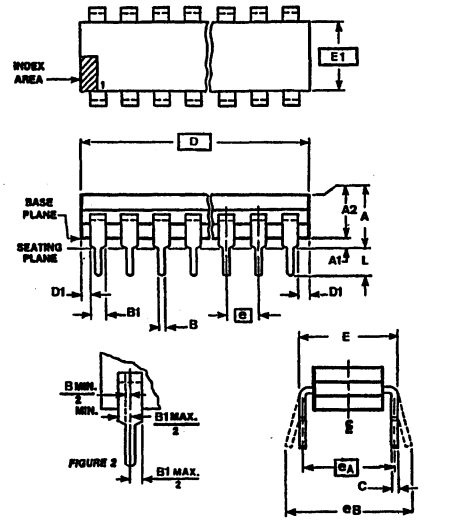
CERDIP DUAL IN LINE

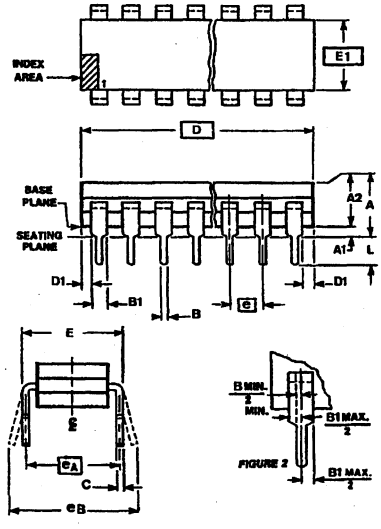
CODES : C1 - C23 20 PINS CERDIP.300 **REV : C**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.32	5.71	.170	.225
A1	0.18	0.74	.007	.029
A2	4.14	5.03	.163	.198
B	0.38	0.58	.015	.023
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	23.87	24.63	.940	.970
D1	0.13	–	.005	–
E	8.00	8.38	.315	.330
E1	7.24	7.87	.285	.310
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.90 B.S.C.		.311 B.S.C.	
eB	8.08	10.82	.318	.426
L	3.17	3.81	.125	.150
PKG STD : 01				



CODE : C33 22 PINS CERDIP.300

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.47	5.84	.176	.230
A1	0.51	–	.020	–
A2	3.17	4.95	.125	.195
B	0.36	0.58	.014	.023
B1	0.89	1.78	.035	.070
C	0.20	0.38	.008	.015
D	26.92	28.19	1.060	1.110
D1	0.13	–	.005	–
E	7.82	8.00	.308	.315
E1	7.24	9.91	.285	.310
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.82	–	.426
L	3.05	5.08	.125	.200
PKG STD : 01				



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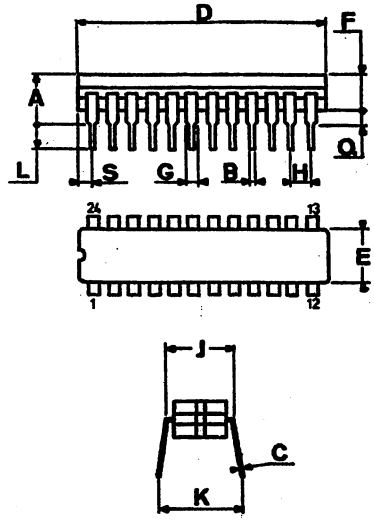
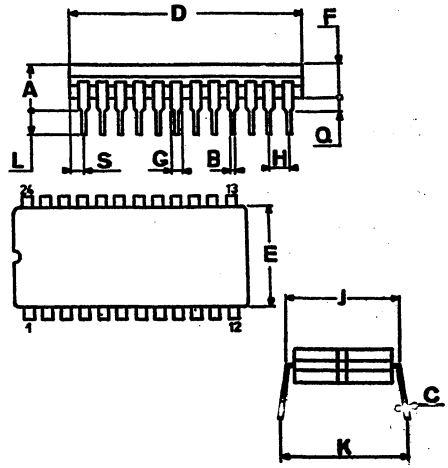
CODES : C25 - C29 CERDIP 24 PINS.300 **REV : B**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
B	0.36	0.58	.014	.023
C	0.20	0.38	.008	.015
D	31.50	32.26	1.240	1.270
E	7.24	7.87	.285	.310
F	3.81	4.57	.150	.180
G	0.76	1.78	.030	.070
H	2.54 TYP		.100 TYP	
J	8.00	8.38	.315	.330
K	8.25	10.16	.325	.400
L	3.17	5.08	.125	.200
Q	0.50	1.52	.020	.060
S	0.76	2.54	.030	.100
PKG STD : 00				



CODE : 5F **CERDIP 24 PINS.600** **REV : B**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
B	0.36	0.58	.014	.023
C	0.20	0.38	.008	.015
D	31.50	32.51	1.240	1.280
E	13.05	13.66	.514	.538
F	3.81	4.57	.150	.180
G	1.27	1.78	.050	.070
H	2.54 TYP		.100 TYP	
J	15.24	15.75	.600	.620
K	15.24	17.78	.600	.700
L	3.17	5.08	.125	.200
Q	0.51	1.52	.020	.060
S	1.52	2.29	.060	.090
PKG STD : 00				



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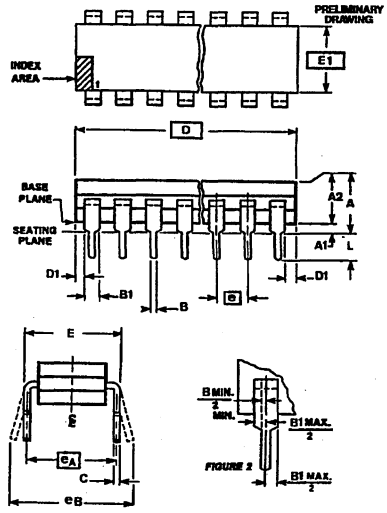
CODE : C31 28 PINS CERDIP.300

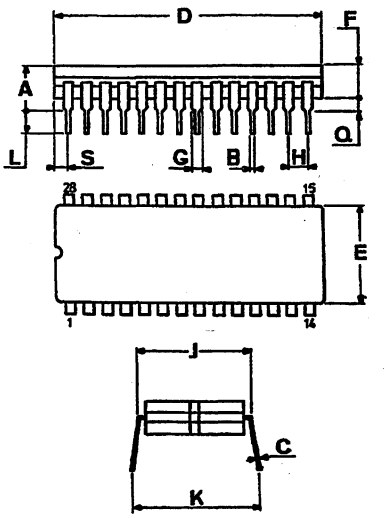
	MM dimens.		IN dimens.	
	min	max	min	max
A	3.30	5.84	.130	.230
A1	0.38	–	.015	–
A2	2.92	4.95	.115	.195
B	0.36	.058	.014	.023
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	29.97	32.64	1.180	1.285
D1	0.13	–	.005	–
E	7.62	8.25	.300	.325
E1	6.10	7.87	.240	.310
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	11.43	–	.450
L	3.05	5.08	.125	.200
PKG STD : 01				



CODE : C32 CERDIP 28 PINS.600

REV : B

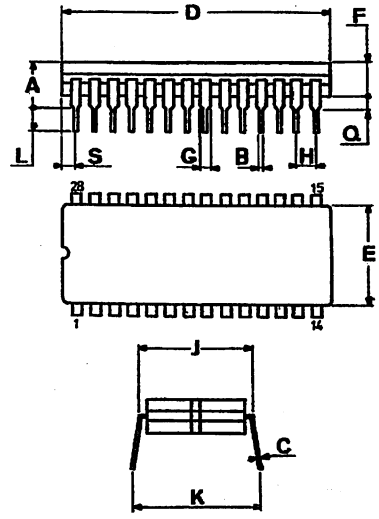
	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
B	0.36	0.58	.014	.023
C	0.20	0.38	.008	.015
D	36.58	37.85	1.440	1.490
E	13.05	13.66	.514	.538
F	3.81	4.57	.150	.180
G	1.27	1.78	.050	.070
H	2.54 TYP		.100 TYP	
J	15.24	15.75	.600	.620
K	15.24	17.78	.600	.700
L	3.17	5.08	.125	.200
Q	0.51	1.52	.020	.060
S	1.52	2.29	.060	.090
PKG STD : 00				



10

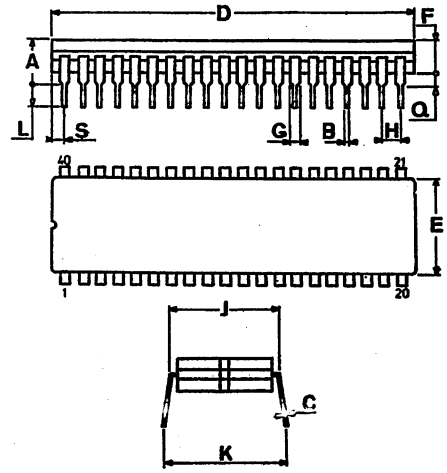
CODE : C20 CERDIP 28 PINS.600 **REV : B**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
B	0.36	0.58	.014	.023
C	0.20	0.38	.008	.015
D	36.58	37.85	1.440	1.490
E	14.50	15.11	.571	.595
F	3.81	4.57	.150	.180
G	1.27	1.78	.050	.070
H	2.54 TYP		.100 TYP	
J	15.24	15.75	.600	.620
K	15.24	17.78	.600	.700
L	3.17	5.08	.125	.200
Q	0.51	1.52	.020	.060
S	1.52	2.29	.060	.090
PKG STD : 00				



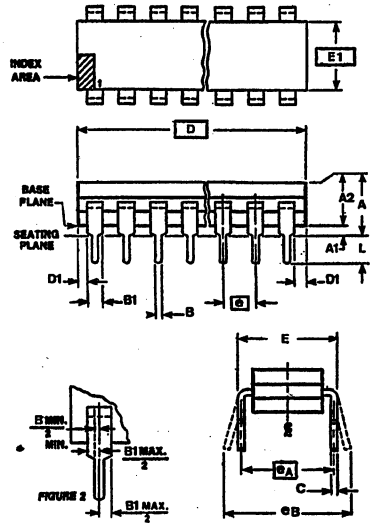
CODE : 5H CERDIP 40 PINS.600 **REV : B**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
B	0.36	0.58	.014	.023
C	0.20	0.38	.008	.015
D	51.69	52.83	2.035	2.080
E	13.05	13.66	.514	.538
F	3.81	4.57	.150	.180
G	1.27	1.78	.050	.070
H	2.54 TYP		.100 TYP	
J	15.24	15.75	.600	.620
K	15.24	17.78	.600	.700
L	3.17	5.08	.125	.200
Q	0.51	1.52	.020	.060
S	1.52	2.29	.060	.090
PKG STD : 00				



CODE : C21 48 PINS CERDIP.600 **REV : D**

	MM dimens.		IN dimens.	
	min	max	min	max
A	4.31	5.71	.170	.225
A1	0.51	1.52	.020	.060
A2	3.81	4.57	.150	.180
B	0.36	0.58	.014	.023
B1	1.27	1.78	.050	.070
C	0.20	0.38	.008	.015
D	62.23	63.65	2.440	2.506
D1	0.13	–	.005	–
E	15.70	15.85	.618	.624
E1	14.78	15.39	.582	.606
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	3.17	3.94	.125	.155
PKG STD : 01				

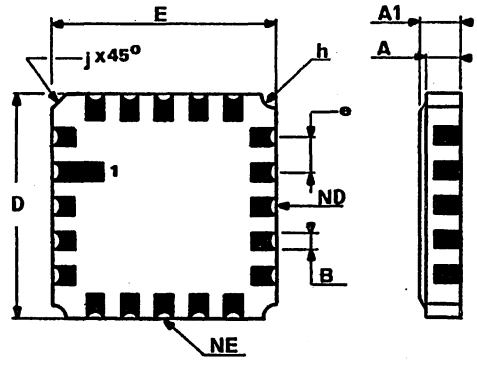


10

CHIP CARRIER

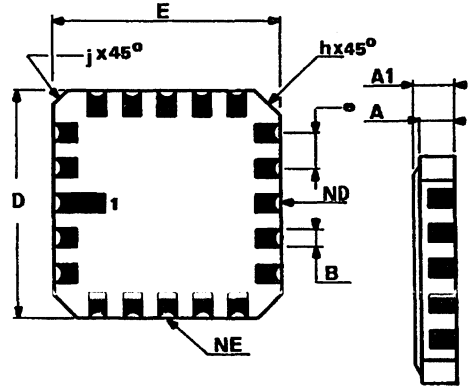
CODE : L04 48 LDS.040 CENTER LEADLESS SQUARE CHIP CARRIER REV : C

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.47	1.83	.058	.072
A1	1.73	2.26	.068	.089
B	0.43	0.58	.017	.023
D	14.10	14.53	.555	.572
E	14.10	14.53	.555	.572
e	1.016 B.S.C.		.040 B.S.C.	
h	0.19 R.A.D.		.0075 R.A.D.	
j	0.51		.020	
ND	12		12	
NE	12		12	
PKG STD : 01				



CODE : L09 48 LDS.050 CENTER LEADLESS SQUARE CHIP CARRIER REV : C

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.47	1.83	.058	.072
A1	1.73	2.26	.068	.089
B	0.635 TYP		.025 TYP	
D	16.33	16.82	.643	.662
E	16.33	16.82	.643	.662
e	1.27 B.S.C.		.050 B.S.C.	
h	1.016		.040	
j	0.51		.020	
ND	11		11	
NE	11		11	
PKG STD : 01				



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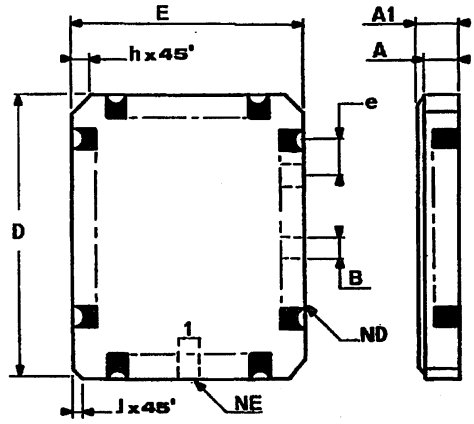
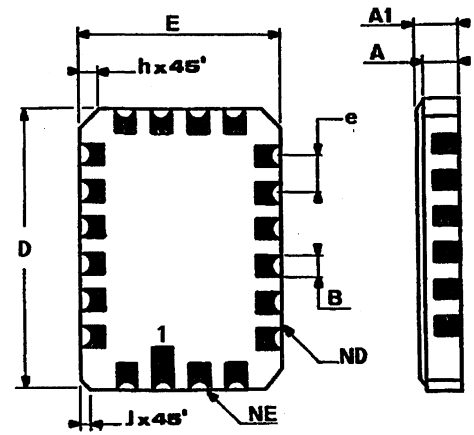
CODE : L15 28 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : O

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.37	1.60	.054	.063
A1	1.62	1.98	.064	.078
B	0.56	0.71	.022	.028
D	13.81	14.12	.544	.556
E	8.74	9.04	.344	.356
e	1.27 B.S.C.		.050 B.S.C.	
h	1.016 T.Y.P.		.040 T.Y.P.	
j	0.51 T.Y.P.		.020 T.Y.P.	
ND	9		9	
NE	5		5	
PKG STD : 01				



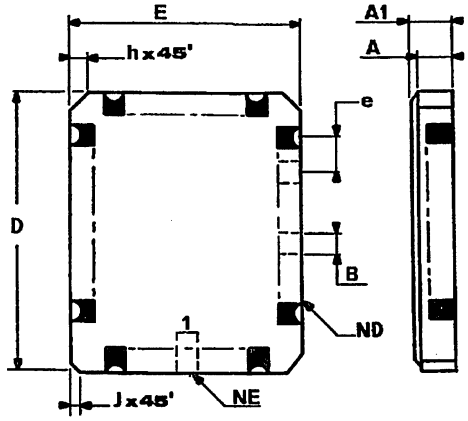
CODE : L20 20 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : C

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.37	1.68	.054	.066
A1	1.62	1.98	.064	.078
B	0.53	0.76	.021	.030
D	10.64	10.94	.419	.431
E	7.21	7.52	.284	.296
e	1.27 B.S.C.		.050 B.S.C.	
h	0.51 T.Y.P.		.020 T.Y.P.	
j	0.25 T.Y.P.		.010 T.Y.P.	
ND	6		6	
NE	4		4	
PKG STD : 02				



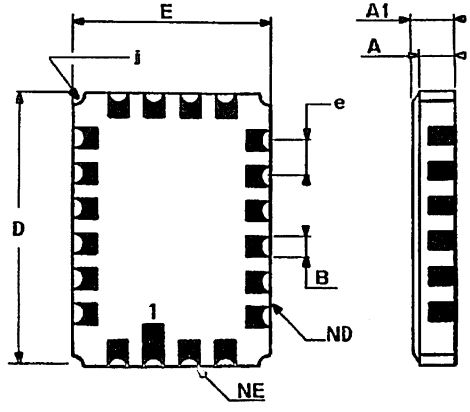
CODES : LU, L17, L32, L19 32 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : G

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.62	1.88	.064	.074
A1	1.88	2.18	.074	.086
B	0.635 T.Y.P.		.025 T.Y.P.	
D	13.81	14.22	.544	.560
E	11.30	11.63	.445	.458
e	1.27 B.S.C.		.050 B.S.C.	
h	1.016		.040	
j	0.51		.020	
ND	9		9	
NE	7		7	
PKG STD : 01				



CODE : L22 20 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : C

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.37	1.68	.054	.066
A1	1.62	1.98	.064	.078
B	0.53	0.76	.021	.030
D	10.64	10.94	.419	.431
E	7.46	7.52	.294	.296
e	1.27 B.S.C.		.050 B.S.C.	
h				
j	0.30 R.A.D.		.010 R.A.D.	
ND	6		6	
NE	4		4	
PKG STD : 02				



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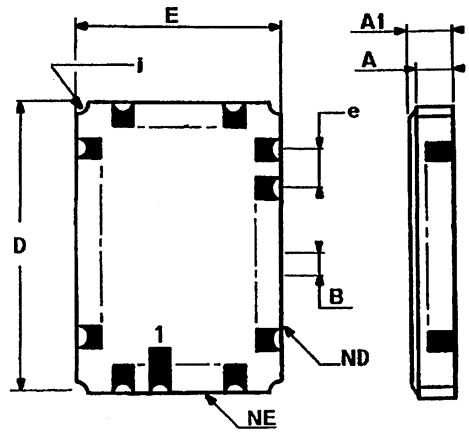
CODE : L23, L16 22 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : A

	MM dimens.		IN dimens.	
	min	max	min	max
A	1.52	1.73	.055	.068
A1	1.78	2.03	.070	.080
B	0.15	–	.006	–
D	12.31	12.57	.485	.495
E	7.24	7.49	.285	.295
e	1.27 B.S.C.		.050 B.S.C.	
h				
j	0.30 R.A.D.		0.12 R.A.D.	
ND	7		7	
NE	4		4	
PKG STD : 00				



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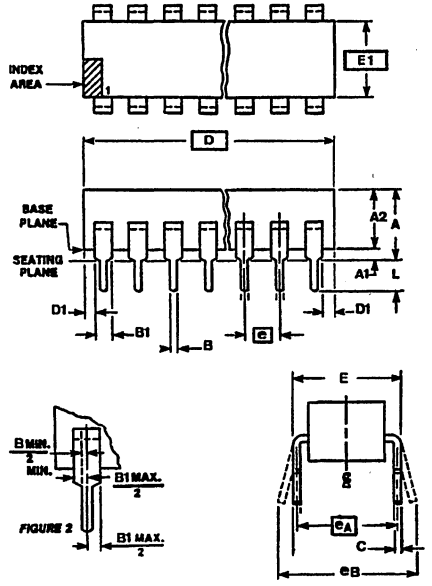
PLASTIC DUAL IN LINE

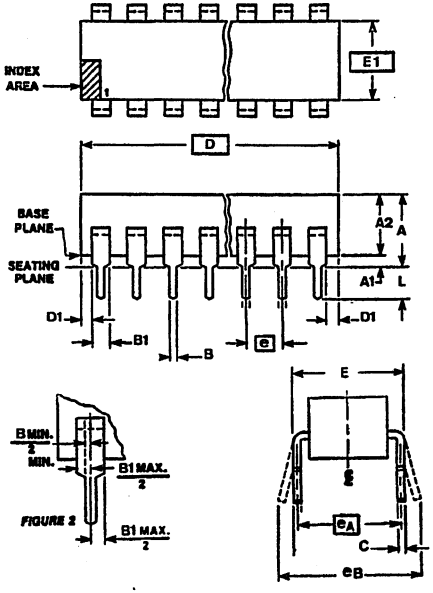
CODES : X8 - O34 **20 PINS PLASTIC.300** **REV : G**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	5.33	–	.210
A1	0.39	–	.015	–
A2	2.92	4.95	.115	.195
B	0.36	–	.014	–
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	23.50	26.90	.925	1.060
E	7.62	8.25	.300	.325
E1	6.10	7.11	.240	.280
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.92	–	.430
L	2.92	4.06	.115	.160
D1	0.13	–	.005	–
PKG STD :				



CODES : O41, O53, O54 **22 PINS PLASTIC.300** **REV : A**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	5.33	–	.210
A1	0.39	–	.015	–
A2	2.92	4.95	.115	.195
B	0.36	–	.014	–
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	26.67	28.45	1.050	1.120
E	7.62	8.25	.300	.325
E1	6.10	7.11	.240	.280
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.92	–	.430
L	2.92	4.06	.115	.160
D1	0.13	–	.005	–
PKG STD : 00				



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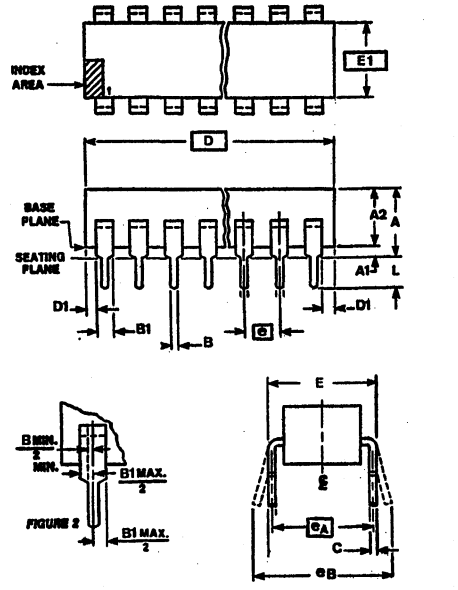
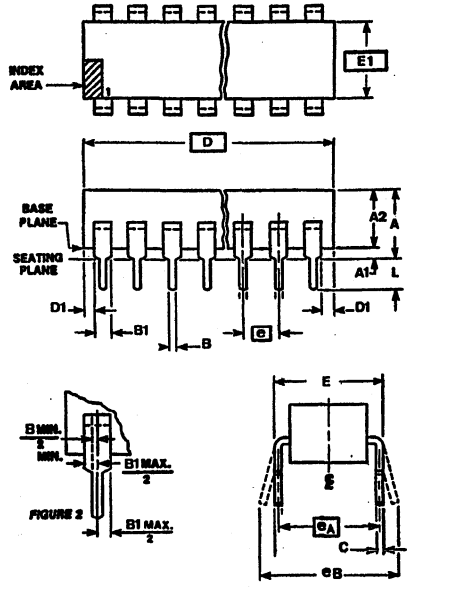
CODES : O43, O44 **24 PINS PLASTIC.300** **REV : G**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	5.33	–	.210
A1	0.39	–	.015	–
A2	2.92	4.95	.115	.195
B	0.36	–	.014	–
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	28.60	32.30	1.125	1.275
E	7.62	8.25	.300	.325
E1	6.10	7.10	.240	.280
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.92	–	.430
L	2.92	4.06	.115	.160
D1	0.13	–	.005	–
PKG STD : 02				



CODES : O3, X3, X40 **24 PINS PLASTIC.300** **REV : D**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	6.35	–	.250
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	29.21	32.77	1.150	1.290
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	5.08	.115	.200
D1	0.13	–	.005	–
PKG STD : 02				



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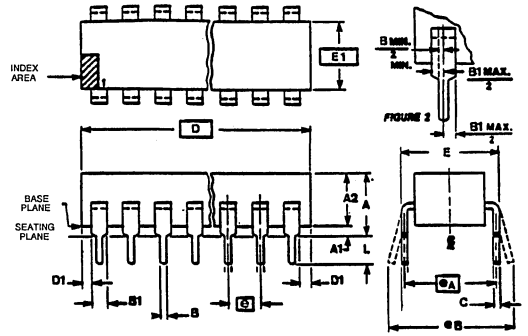
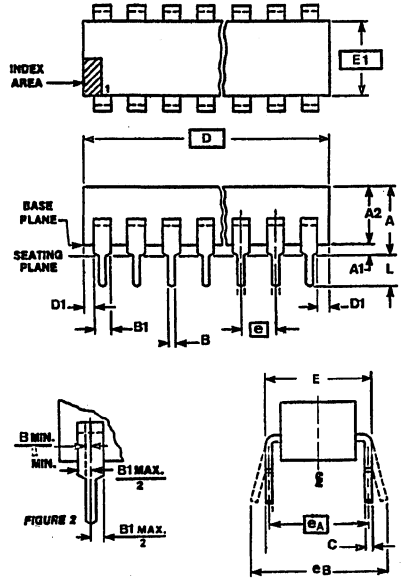
CODES : O49, O51 **28 PINS PLASTIC.300**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	4.57	–	.180
A1	0.51	–	.020	–
A2	–	3.30	–	.130
B	0.36	–	.014	–
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	34.54	34.80	1.360	1.370
E	7.62	8.25	.300	.325
E1	7.11	7.62	.280	.300
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.92	–	.430
L	3.18	3.43	.125	.135
D1	0.71	0.97	.028	.038
PKG STD : 00				



CODES : X33, O50, O33 **28 PINS PLASTIC.600** **REV : C**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	6.35	–	.250
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	35.05	39.75	1.380	1.565
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	5.08	.115	.200
D1	0.13	–	.005	–
PKG STD : 02				



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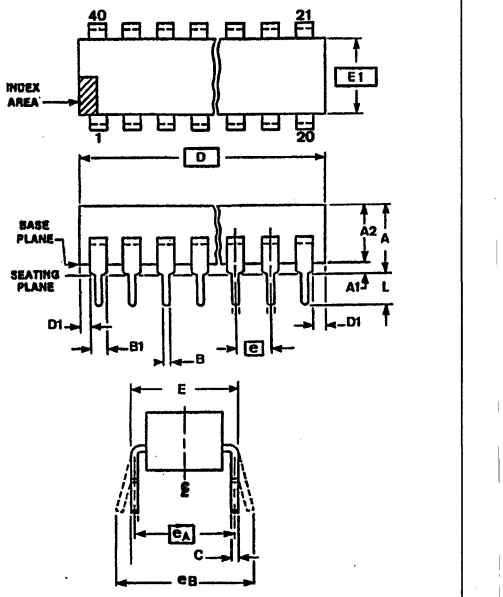
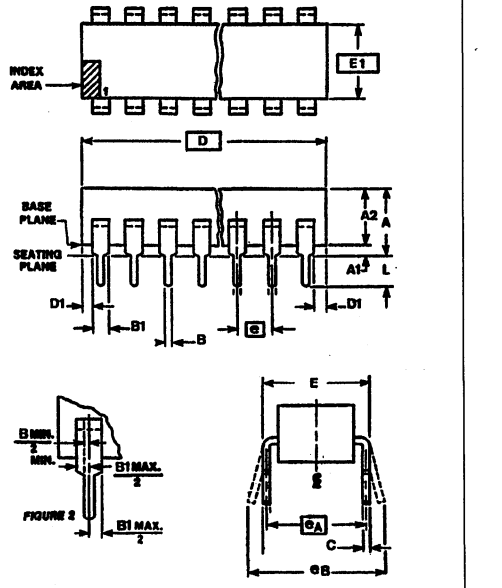
CODE : 3J **40 PINS PLASTIC.600** **REV : C**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	6.35	–	.250
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	5.08	.115	.200
D1	0.13	–	.005	–
PKG STD : 02				



CODES : O36 **48 PINS PLASTIC.600** **REV : C**

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	6.35	–	.250
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	61.98	62.48	2.440	2.460
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	5.08	.115	.200
D1	0.13	–	.005	–
PKG STD : 01				



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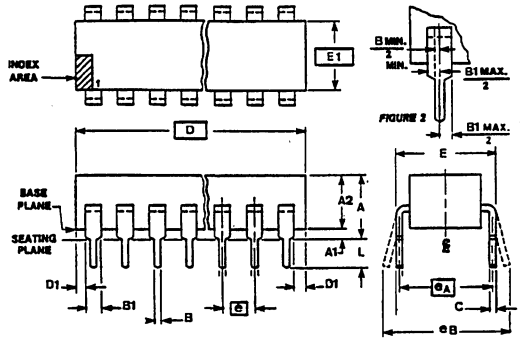
CODES : O49, O51 28 PINS PLASTIC.300

	MM dimens.		IN dimens.	
	min	max	min	max
A	–	4.57	–	.180
A1	0.51	–	.020	–
A2	–	3.30	–	.130
B	0.36	–	.014	–
B1	1.14	1.78	.045	.070
C	0.20	0.38	.008	.015
D	34.54	34.80	1.360	1.370
E	7.62	8.25	.300	.325
E1	7.11	7.62	.280	.300
e	2.54 B.S.C.		.100 B.S.C.	
eA	7.62 B.S.C.		.300 B.S.C.	
eB	–	10.92	–	.430
L	3.18	3.43	.125	.135
D1	0.71	0.97	.028	.038
PKG STD : 00				



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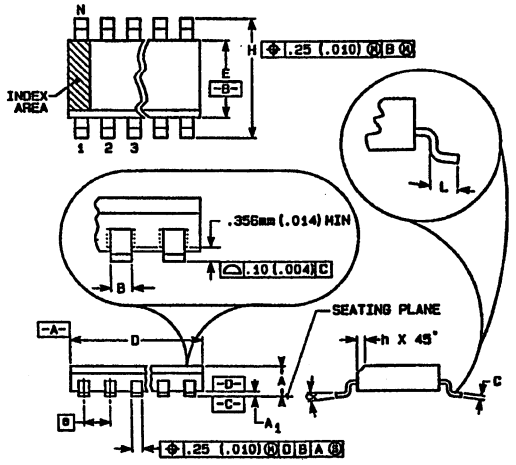
SMALL OUTLINE

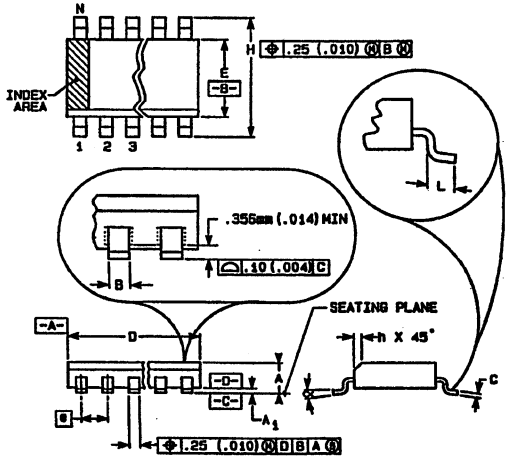
CODES : N01 20 PINS S.O. (.300) **REV : F**

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.35	2.65	.0926	.1043
A1	0.10	0.30	.0040	.0118
B	0.35	0.49	.0138	.0192
C	0.23	0.32	.0091	.0125
D	12.60	13.00	.4961	.5118
E	7.40	7.60	.2914	.2992
e	1.27 B.S.C.		.050 B.S.C.	
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	20		20	
α	0*		8*	
PKG STD : 01				



CODES : N02 24 PINS S.O. (.300) **REV : F**

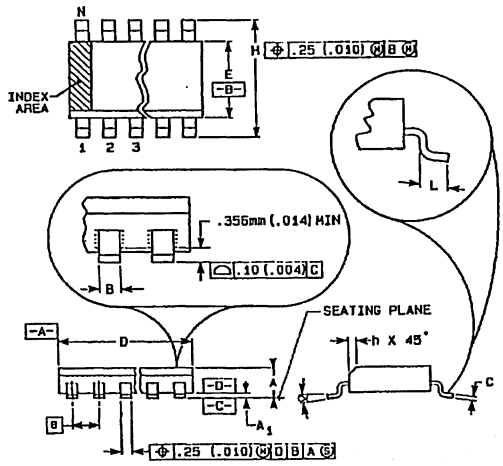
	MM dimens.		IN dimens.	
	min	max	min	max
A	2.35	2.65	.0926	.1043
A1	0.10	0.30	.0040	.0118
B	0.35	0.49	.0138	.0192
C	0.23	0.32	.0091	.0125
D	15.20	15.60	.5985	.6141
E	7.40	7.60	.2914	.2992
e	1.27 B.S.C.		.050 B.S.C.	
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	24		24	
α	0*		8*	
PKG STD : 01				



10

CODE : N10 28 PINS S.O.(300) **REV : F**

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.35	2.65	.0926	.1043
A1	0.10	0.30	.0040	.0118
B	0.35	0.49	.0138	.0192
C	0.23	0.32	.0091	.0125
D	17.70	18.10	.6969	.7125
E	7.40	7.60	.2914	.2992
e	1.27 B.S.C.		.050 B.S.C.	
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	28		28	
α	0*		8*	
PKG STD : 01				

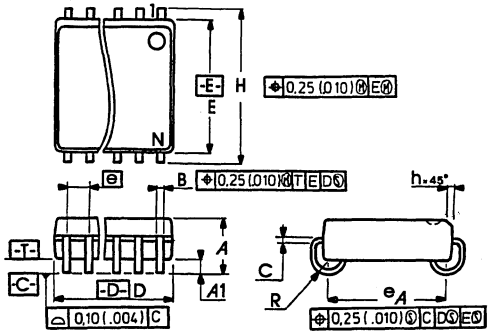


10

SOJ PACKAGES

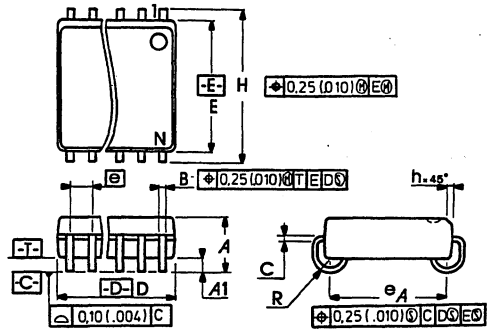
CODES : P02 24 PINS S.O.J.(.300)

	MM dimens.		IN dimens.	
	min	max	min	max
A	3.05	3.56	.120	.140
A1	0.71	0.91	.028	.036
B	0.35	0.48	.014	.019
C	0.254		.010	
D	15.29	15.54	.602	.612
E	7.42	7.59	.292	.299
e	1.27 B.S.C.		.050 B.S.C.	
H	8.51	8.81	.335	.347
h	0.25	0.41	.010	.016
eA	6.65	6.91	.262	.272
N	24		24	
R	0.79	1.07	.031	.042
PKG STD : 01				



CODES : P03 28 PINS S.O.J.(.300)

	MM dimens.		IN dimens.	
	min	max	min	max
A	3.05	3.56	.120	.140
A1	0.71	0.91	.028	.036
B	0.35	0.48	.014	.019
C	0.254		.010	
D	17.81	18.06	.701	.711
E	7.42	7.59	.292	.299
e	1.27 B.S.C.		.050 B.S.C.	
H	8.51	8.81	.335	.347
h	0.25	0.41	.010	.016
eA	6.65	6.91	.262	.272
N	28		28	
R	0.79	1.07	.031	.042
PKG STD : 01				

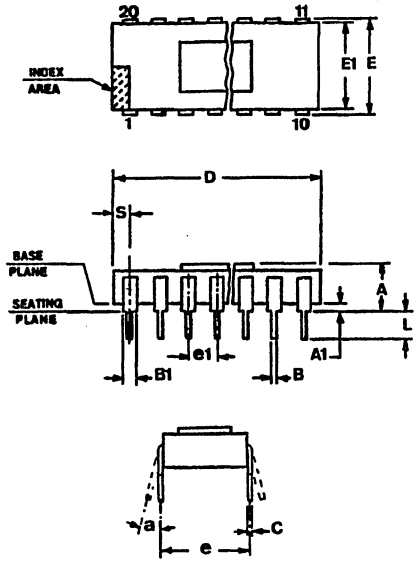


10

SIDE BRAZE

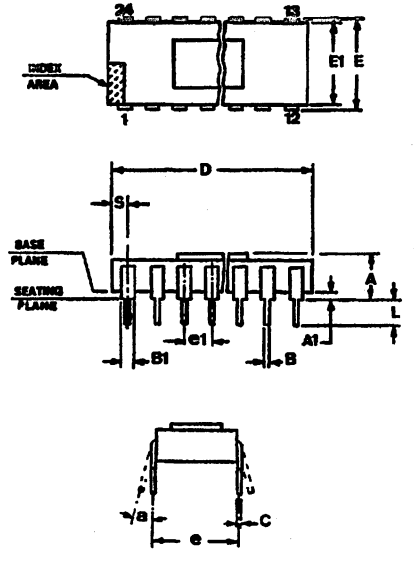
CODES : S15, S25 20 LEAD (.300) SIDE BRAZE **REV : O**

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.82	3.94	.111	.155
B	0.38	0.53	.015	.021
C	0.20	0.30	.008	.012
D	25.14	25.65	.990	1.010
E1	7.49 R.E.F		.295 R.E.F.	
B1	1.22	1.32	.048	.052
e1	2.54 T.Y.P.		.100 T.Y.P.	
E	7.37	8.25	.290	.325
L	3.18	4.44	.125	.175
A1	0.63	1.14	.025	.045
S	2.41	2.67	.095	.105
a	0*	15*	0*	15*
PKG STD : 00				



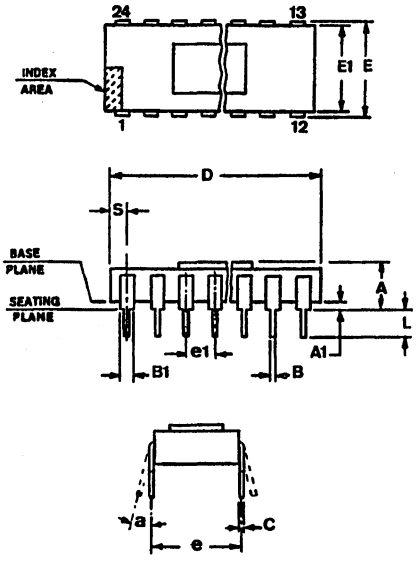
CODE : S31 24 LEAD (.300) SIDE BRAZE **REV : O**

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.67	4.44	.105	.175
B	0.38	0.58	.015	.023
C	0.20	0.30	.008	.012
D	28.39	30.78	1.188	1.212
E1	7.29	8.26	.287	.325
B1	0.97	1.52	.038	.060
e1	2.54 T.Y.P.		.100 T.Y.P.	
E	7.37	8.25	.290	.325
e	7.62 T.Y.P.		.300 T.Y.P.	
L	3.18	4.44	.125	.175
A1	0.64	1.39	.025	.055
S	2.11	2.97	.083	.117
e	0*	15*	0*	15*
PKG STD : 00				



10

CODE : 6H **24 LEAD (.600) SIDE BRAZE** **REV : D**



	MM dimens.		IN dimens.	
	min	max	min	max
A	1.90	3.18	.075	.125
B	0.41	0.51	.016	.020
C	0.22	0.30	.009	.012
D	30.10	31.10	1.185	1.224
E	14.75	15.25	.580	.600
F				
G	1.27 TYP		.050 TYP	
H	2.27	2.79	.090	.110
J				
K	14.99	15.49	.590	.610
L	3.18	5.08	.125	.200
Q	1.02	1.52	.040	.060
S	1.02	1.52	.040	.060
PKG STD : OBSOLETE				

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.20	4.80	.085	.190
B	0.38	0.58	.015	.023
C	0.20	0.30	.008	.012
D	29.88	30.98	1.180	1.220
E1	14.61	15.49	.575	.610
B1	0.97	1.52	.038	.060
e1	2.54 T.Y.P.		.100 T.Y.P.	
E	15.12	15.87	.595	.625
e	15.24 T.Y.P.		.600 T.Y.P.	
L	3.18	4.44	.125	.175
A1	0.51	1.77	.020	.070
S	0.77	1.65	.030	.065
e	0*	15*	0*	15*
PKG STD : 01				

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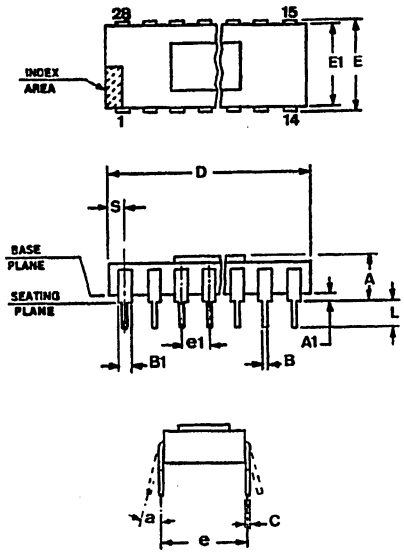
CODES : S21, S30 28 LEAD (.600) SIDE BRAZE **REV : C**



	MM dimens.		IN dimens.	
	min	max	min	max
A	1.90	3.18	.075	.125
B	0.41	0.51	.016	.020
C	0.22	0.30	.009	.012
D	35.20	36.20	.380	.420
E	14.75	15.25	.580	.600
F				
G	1.27 TYP		.050 TYP	
H	2.27	2.79	.090	.110
J				
K	14.99	15.49	.590	.610
L	3.18	5.08	.125	.200
Q	1.02	1.52	.040	.060
S	1.02	1.52	.040	.060
PKG STD : OBSOLETE				

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.20	4.80	.085	.190
B	0.38	0.58	.015	.023
C	0.20	0.30	.008	.012
D	35.06	36.22	1.180	1.220
E1	14.74	15.49	.580	.610
B1	0.97	1.52	.038	.060
e1	2.54 T.Y.P.		.100 T.Y.P.	
E	15.12	15.87	.595	.625
e	15.24 T.Y.P.		.600 T.Y.P.	
L	3.18	4.44	.125	.175
A1	0.51	1.77	.020	.070
S	0.77	1.65	.030	.065
e	0*	15*	0*	15*
PKG STD : 01				

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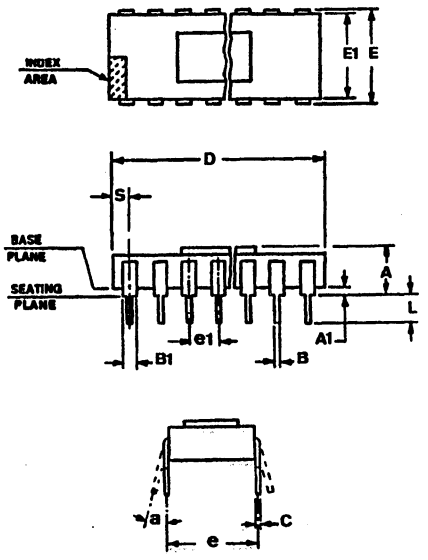
CODE : S01 **40 LEAD (.600) SIDE BRAZE** **REV : D**



	MM dimens.		IN dimens.	
	min	max	min	max
A	1.90	3.18	.075	.125
B	0.41	0.51	.016	.020
C	0.22	0.30	.009	.012
D	50.29	51.31	1.980	2.020
E	14.75	15.25	.580	.600
F				
G	1.27 TYP		.050 TYP	
H	2.27	2.79	.090	.110
J				
K	14.99	15.49	.590	.610
L	3.18	5.08	.125	.200
Q	1.02	1.52	.040	.060
S	1.02	1.52	.040	.060
PKG STD : OBSOLETE				

	MM dimens.		IN dimens.	
	min	max	min	max
A	2.20	4.80	.085	.190
B	0.38	0.58	.015	.023
C	0.20	0.30	.008	.012
D	50.30	51.56	1.980	2.030
E1	14.74	15.49	.580	.610
B1	0.97	1.52	.038	.060
e1	2.54 T.Y.P.		.100 T.Y.P.	
E	15.12	15.87	.595	.625
e	15.24 T.Y.P.		.600 T.Y.P.	
L	3.18	4.44	.125	.175
A1	0.51	1.77	.020	.070
S	0.77	1.65	.030	.065
e	0*	15*	0*	15*
PKG STD : 01				

10

QUALITY

11

QUALITY

1 - INTRODUCTION

1.1 - STATEMENT OF SCOPE

This section establishes the detail requirements for MATRA MHS' circuits screened and tested under the Quality Assurance Program.

Included in this section are the Quality standards and screening methods for commercial parts which must perform reliable in the field.

1.2 - APPLICABLE DOCUMENTS

The following documents form a part of this section to the extent referenced herein and provide the foundation of Matra MHS Quality Program :

MIL-M-38510G	"General Specification of Microcircuits"
MIL-STD-883C	"Test Methods and Procedures for Microelectronics"
ESA/SCC9000	"European Space Agency Specification for Microelectronics"

The MHS Quality Assurance Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the MATRA MHS facilities and survey the deployment of the Quality function.

MATRA MHS maintains a Quality Assurance Program (QAP) using the above defined documents as a guide. This program assures compliance with the requirements and quality standard of control drawings and the requirements of this specification.

The special military and space programs will also be found useful by those MATRA MHS customers who must generate their own procurement specifications *(see hi-rel databook).*

Use of the enclosed MATRA MHS standard test tables, test parameters and burn-in circuits will aid in reducing specification negociation time.

1.3 - QUALITY AND RELIABILITY AT MATRA MHS

Our Quality Division strives to assure that the quality and reliability of products shipped to customers are high quality level and consistent with customer's requirements.

To achieve these requirements, MATRA MHS has started in early 1988 a Quality Improvement Program. The objective of this program is to call for continuous Progress and committment of every employee to total Quality.

The reliability approach at MATRA MHS is based on designing in reliability rather than testing for reliability only. The latter is applied to check and confirm that sound design with quality and reliability ground rules are observed and correctly executed in a new product design.

Reliability engineering becomes involved as early as concept review of a new product and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability layout guidelines are invoked to insure an all around reliable design. This concept is reflected by the MATRA MHS reliability procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Both maximum rated and accelerated stress conditions are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device's stress limitation.

PPM PROGRAM

- For standard and volume products, MHS proposes to his customers a PPM program. Cooperation agreement could be established with customer willing to engage such an improvement program.
- PPM programs are already existing and we expect an optimum of 2 or 3 customers agreements by product. It is obvious that the upgrade of the quality level achieved is effective for all customers.

1.4 - AGENCIES QUALIFICATIONS

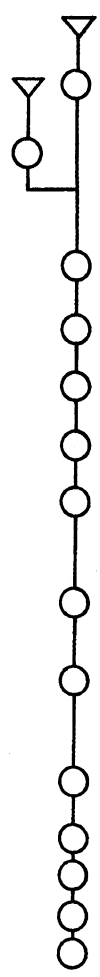
As part of specific qualification on military or space programs, MATRA MHS received several agreements from french agencies.

In 1986, MHS received the RAQ 1 certification (RAQ 1/ AQAP 1 Regulation quality assurance level 1) from the SIAR (service de surveillance industrielle de l'armement).

The RAQ1 means that MATRA MHS quality assurance procedures satisfy design, manufacturing and delivery of MOS products and on customer support on custom design.

The major MHS technologies and products are agreed by french telecommunication agency (CNET). These products are in qualified list (LNZ).

2 - QUALITY CONTROL

FLOW	PROCESS	TYPICAL ITEM	FREQUENCY	REQUIREMENTS
	Silicon wafers Incoming Inspection	• Resistivity • Bow–particles • Flatness • Taper • Oxygen content • Dimensions • Appearance	Every manufactured lot	25 Wafers/LOT
	Masks Incoming Inspection	• Defects • Dimensions • Registration • Conformity	Every mask	
	Oxidize	Thickness	Every run	3 Wafers/run 5 points/wafer
	Implant	Resistivity Thersal wave	Every run	2 Wafers/run 5 points/wafer
	Diffuse	Resistivity Thickness	Every run	3 Wafers/lot 5 points/wafer
	Silicon nitride	Thickness Critical dimensions (*)	Every run	3 Wafers/run 5 points/wafer
	Gate oxide	Thickness Defect rates VFBDVFB	Every run	3 Wafers/lot 5 points/wafer
	Polysilicon	• Resistivity • Thickness • Critical dimensions (*) • Sem Inspection	Every run Periodical	3 Wafers/lot 5 points/wafer
	Metallization	• Resistivity • Thickness • Critical dimensions (*) • Sem Inspection	Every run Periodical	1 Wafer/run
	Passivation	• Doping • CVD Thickness • Sem Inspection	Every run Periodical	3 points/wafer
	Test site	Electrical charact.	Every Wafer	5 PCM/wafer
	Blacklap	Thickness	Every lot	1 wafer/lot
	QC visual gate	Visual	Sampling	5 wafer/lot
	Wafer sort	Electrical charact.	100 % chips	

* All Critical Dimensions (After etching) : Every lot - 3 wafers/lot
- 5 points/wafer.

Table 1 : Quality flow chart of wafer processing.

2.1 - PROCESS CONTROLS

As shown by table 1 each integrated circuit is constructed by manufacturing processes which are under the surveillance of MATRA MHS Quality Control Department. The processes are monitored and controlled by use of statistical techniques and computerization in accordance with published specifications and procedures. MATRA MHS prepares and maintains suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process specification. The customer may verify, with the permission of and in the company of MATRA MHS's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by MATRA MHS is made available to the customer or its representative only with the written permission of MATRA MHS.

Process control is recognized as being vital to the concept of "built-in" quality. The process control program includes a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis is defined in a Quality & Reliability Assurance document.

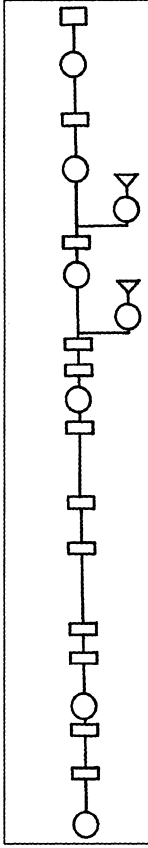
FLOW	PROCESS MATERIALS	INSPECTION	METHOD	FREQUENCY
	Scribing	Visual	2010 Cond B	Monitor
	2 Nd Optical	Visual	2010 Cond B	100 %
	Scribing	Visual	2010 Cond B	100 %
	QC Inspection	Visual	2010 Cond B	Every lot
	Lead Frame, base (incoming inspection)			
	Die Bonding			
	QC Inspection	Appearance		Every lot
	Wire (incoming inspection)			
	Wire Bonding	Bond sirength	2011	Every lot
	Praseal inspection	Visual		100 %
	QC Inspection	Visual		Every lot
	Prestabilization sealing			
	Temperature Cycling		1010 Condition C	100 %
	Centrifuge		2001 Condition E	100 %
	Lead cut			
	Plating			
	Plating inspection	Appearance thickness		Every lot
	Marking	Permanency	2015	Every lot
	Fine leak		1014 Condition A or B	100 %
	Gross leak		1014 Condition C	100 %
	QA monitoring		All QC inspection	

Table 2 : QC Ceramic flow charts of assembly process (1).

2.1 - CONTROL OF PROCUREMENT SOURCES

MATRA MHS is responsible for assuring that all supplies and services conform to this specification, the detail specification and MHS's procurement requirements.

A - MATRA MHS/supplier convention

Prior to use in production, MATRA MHS verifies the capability of the supplier QA, manufacturing engineering and services to deliver material conform to specification and kept under control. Formal agreement is established between the two partners.

B - Receiving inspection

Purchased supplies are subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration is given to the controls exercised by the procurement source and evidence of substained quality conformance.

C - MATRA MHS initiates corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

COMMERCIAL TEMP. RANGE 0°C to 70°C			INDUSTRIAL TEMP. RANGE – 40°C to + 85°C			AUTOMOTIVE – 40°C to 110°C	MILITARY TEMP. RANGE – 55°C to + 125°C		
Family	STD	STD + B.I.	**Family**	STD	STD + B.I.	**Family**	**Family**	STD	STD + B.I.
Memory suffix	– 5	– 5 +	**Memory suffix**	– 9	– 9 +		**Memory**	– 2	– 8
Micro's prefix		Q	**Micro's prefix**	I	L	**Micro's prefix A**	**Micro's**		M---/B
Gate array suffix	– 5	– 5 +	**Gate array suffix**	– 9	– 9 +		**Gate array**	– 2	– 8

Table 1 : PROCESS FLOWS INFORMATION

	COMMERCIAL		INDUSTRIAL		AUTOMOTIVE	MILITARY	
	STD	**STD + B.I.**	**STD**	**STD + B.I.**		**STD**	**STD + B.I.**
QA Wafer visual inspection	Monitor	Monitor	Monitor	Monitor	Monitor	Monitor	Monitor
Electrical test and probe 25°C	100%	100%	100%	100%	100%	100%	100%
Assembly (see table 2 and 3)	100%	100%	100%	100%	100%	100%	100%
Pre Burn–in test		100%		100%	100%		100%
Burn–in		100% (1)		100% (1)	100% (1)		100% (1)
Post Burn–in test		100%		100%	100%		100%
P.D.A (percentage defective allowable)		5% (2)		5% (2)	5% (2)		5% (2)
Final electrical test (per MHS specification)	100% high temp. Low temp. optional	idem	idem	idem	idem	idem	idem
Marking (lot number + branding week code, per MATRA MHS specification)	100%	100%	100%	100%	100%		100%
Lead Straigthen	100%	100%	100%	100%	100%	100%	100%
MATRA MHS Quality final acceptance electrical	(3)	(3)	(3)	(3)	(3)	(3)	(3)
mechanical (visual)	100%	100%	100%	100%	100%	100%	100%

Notes : 1) Burn-in is performed as 24 h, 125°C (or equivalent) minimum.
2) If a lot fails the 5 % PDA, but is < 10 %, the lot may be submitted to burn-in on time only to the same time and temperature condition.
3) MHS quality final acceptance is performed following quality dispositions to assure 200 ppm. Average Outgoing Quality.

3 - RELIABILITY RESULTS

The objective failure rate at 55°C, 60 % UCL is in any case lower than 100 fits. Details about data base are available upon request in Reliability Reports, written for each product or product family.

4 - MILITARY HI-REL PRODUCTS

A broad choice of quality grades is available.

CB : CECC program according to level B of CECC 90000.

MB : military program according to class B of MIL-STD 883C.

SB : space program according to level B of SCC 9000 (LAT 1, 2, 3).

SC : space program according to level C or SCC9000 (LAT 1, 2, 3).

DB : dice military program with qualification flow.

(refer to MATRA MHS high reliability Data-book)

5 - DICE/WAFER FORM

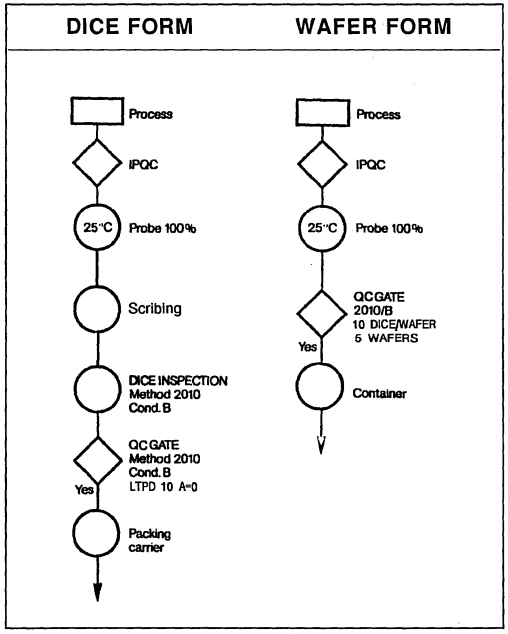
MATRA MHS Memory, Gate Arrays and Microcontroller products are available in chip form and wafer form to the hybrid microcircuit designer. Table 1 gives the different flows used for Military and Standard levels with the production operations and QC gates.

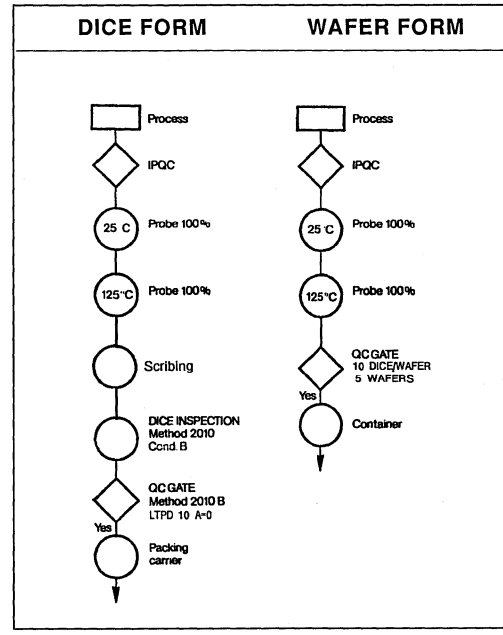
So as to respond to specific requirements of the hybrid industry, MATRA MHS has several additionnal options to table 1 as electrical qualification lots for military dice, available upon request at extra cost.

PROCESS FLOWS INFORMATION (Table 1)

STANDARD FLOW		
FAMILY	**DICE FORM**	**WAFER FORM**
MEMORY	HM0–65162-6	HMW–65162-6
MICRO'S	XX–80C31	XW–80C31
GATE ARRAY	MA0–250A69-6	MAW–250A69-6

MILITARY FLOW		
FAMILY	**DICE FORM**	**WAFER FORM**
MEMORY	HM0–65162-2	HMW–65162-2
MICRO'S	–80C31	XW–80C31
GATE ARRAY	MA0–250A69-2	MAW–250A69-2





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M.H.S.
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7973-B WASHINGTON WOOD DRIVE
DAYTON, OH 45459
Tel. : (513) 433-5551
Fax : (513) 461-4329

749 MINER ROAD
CLEVELAND, OH 44143
Tel. : (216) 461-4700
Fax : (216) 461-4329

620 ALPHA DRIVE
PITTSBURGH, PA 15238
Tel. : (412) 963-6202
Fax : (412) 963-6210

FALCON ELECTRONICS INC.

5 HIGGINS DRIVE
MILFORD, CT 06460
Tel. : (203) 878-5272
Fax : (203) 877-2010

CATON RESEARCH CENTER,
SUITE Q
1520 CATON CENTER DRIVE
BALTIMORE, MD 21227
Tel. : (301) 247-5800
Fax : (301) 247-5893

1383 VETERAN'S MEMORIAL HWY.
HAUPPAGE, NY 11788
Tel. : (516) 724)-0980
(800) 528-0016
Fax : (516) 724-0993

HAMMOND ELECTRONICS, INC.

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HUNTSVILLE, AL 35816
Tel. : (205) 830-4764
Fax : (205) 830-4287

6600 N.W. 21ST AVE., 8AY D
FT. LAUDERDALE, FL 33309
Tel. : (305) 973-7103
(FT LAUDERDALE)
Fax : (305) 973-7601

2923 PACIFIC AVE.
GREENBORO, NC 27420
Tel. : (919) 275-6391

1230 WEST CENTRAL BLVD.
ORLANDO, FL 32802
Tel. : (407) 841-1010 (ORLANDO)
Fax : (407) 648-8584

5680 OAKBROOK PKWY., SUITE 160
NORCROSS, GA 30093
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(800) 241-5437
Fax : (404) 424-9834

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151 ANDOVER ST.
DANVERS, MA 01923
Tel. : (617) 777-8800
Fax : (617) 777-8806

6000 NEW HORIZONS BLVD.
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Tel. : (516) 226-6000
Fax : (516) 226-6262

39 U.S. ROUTE 46
PINE BROCK, NJ 07058
Tel. : (201) 882-8300
Fax : (201) 882-8398

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CAMPUS
MARLTON, NJ 08053
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Fax : (609) 596-0612

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EACH ROCHESTER, NY 1445
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(203) 265-0162
Fax : (716) 248-9132

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CANADA L3R 424
Tel. : (416) 475-3922
Fax : (416) 475-4158

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OTTAWA, ONTARIO
CANADA K2C OR3
Tel. : (613) 727-8325
Fax : (613) 727-9489

8563 GOVERNMENT ST.
BURNABY, B.C.
CANADA V3N 4S9
Tel. : (604 420-9889
Fax : (604) 420-0124

243 PLACE FRONTENAC
POINTE CLAIRE, PQ
CANADA H9R 4Z7
Tel. : (514) 694-0860
Fax : (514) 694-0965

6120 THIRD ST., SE UNIT #G
CALGARY, ALBERTA
CANADA T2H 1K4
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