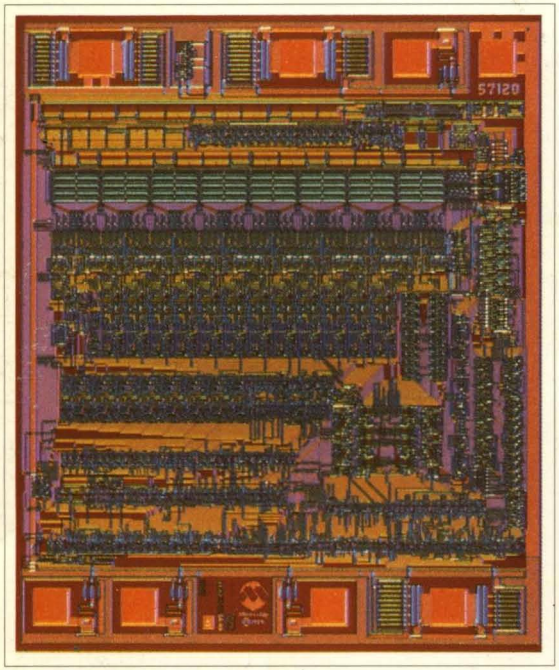
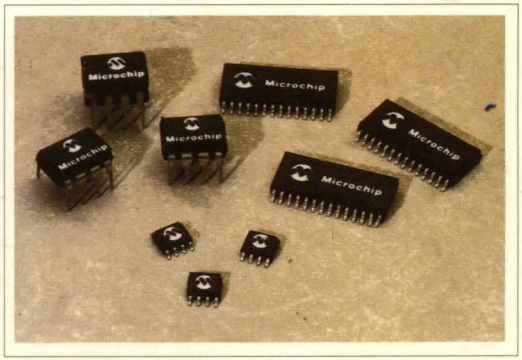
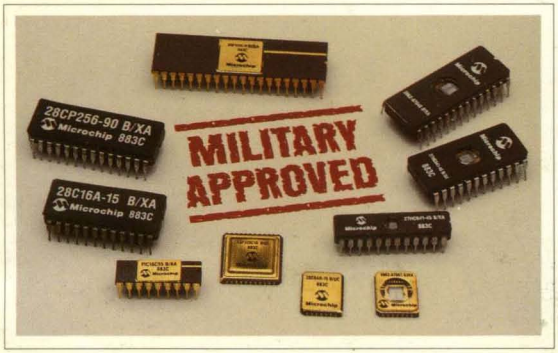
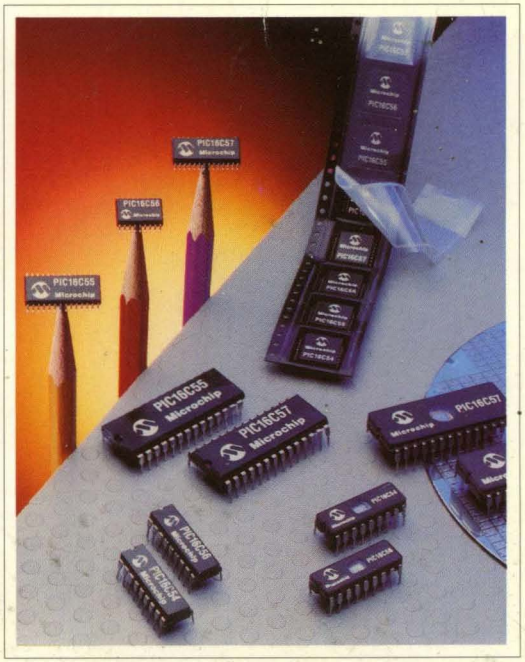
MICROCHIP DATA BOOK









Microchip

Microchip Data Book

Second Edition

For Military devices, please refer to the "MILITARY DATA BOOK"

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MICROCHIP TECHNOLOGY INCORPORATED

Company Profile

FEATURES

- Fully integrated manufacturing
- A global network of plants and facilities
- A history of innovation
- Strategic marketing focus
- A product family of shared strengths
- Quality without compromise
- Research and development of high performance products
- Performance alliance with customers
- A solid executive team with an eye towards innovation

BUSINESS SCOPE

Microchip Technology manufactures and markets very large scale integrated circuits (VLSI). The Company's strong experience in CMOS nonvolatile memories, programmable microcontrollers and peripheral devices has positioned the firm as a leading supplier to manufacturers of computer peripheral, automotive, consumer, military and telecommunication products.

Company headquarters in Chandler, Arizona; executive offices, R & D, and two wafer fabrication units occupy this 142,000 square-foot facility.

GUIDING VALUES

Customers Are Our Focus

We establish successful customer partnerships by exceeding customer expectations for products, services and attitude. We earn our credibility through meeting commitments and producing quality products and services in a timely fashion. We believe each employee must effectively serve their internal customers in order for Microchip's external customers to be properly served.

Quality Comes First

We will perform correctly the first time, maintain customer satisfaction and measure our quality against requirements. We practice effective and standardized improvement methods, such as statistical process control to anticipate problems and implement root cause solutions. We believe that when quality comes first, reduced costs follow.

Continuous Improvement Is Essential

We utilize the concept of "Vital Few" to establish our priorities. We concentrate our resources on continuously improving the Vital Few while empowering each employee to make continuous improvements in their area of responsibility. We strive for constructive and honest self-criticism to identify improvement opportunities.

Employees Are Our Greatest Strength

We design jobs and provide opportunities in a fashion which clearly promotes pride in work, integrity, trust, teamwork, creativity, employee involvement and development, fairness, and productivity. We base recognition, advancement and compensation on an employee's achievement of excellence in team and individual performance. We provide for employee health and welfare by offering a competitive, comprehensive employee benefits program.

Shareholders Are The Owners Of Our Business

We understand that shareholders have invested in the Microchip team and will be provided with continuously increasing company net worth.

Technology Is Our Foundation

We commit to ongoing investments and advancements in the design and development of our manufacturing process, device and circuit technologies, which are the basis for our products.

Products Are The Result Of Our Efforts

We develop technologies which provide reliable, innovative, and cost effective products to support current and future market opportunities. We understand that customers primarily view Microchip through the quality, service, cost, and technological leadership of our products.

Total Cycle Times Are Competitive

We focus resources to optimize cycle times to our customers by empowering employees to achieve efficient cycle times in their area of responsibility. We believe that cycle time reduction is achieved by streamlining processes through the systematic removal of barriers to productivity.

Safety Is Never Compromised

We place our concern for safety of our community and employees at the forefront of our decisions, policies and actions. Each employee is responsible for safety.

Profits Provide For Everything We Do

We strive to maintain competitive pretax profits as they allow continued investments and future growth, and indicate the overall success of Microchip.

Communication Is Vital

We encourage open, honest, constructive, and ongoing communication in all company and community relationships to resolve issues, exchange information and share knowledge.

Suppliers, Representatives, And Distributors Are Our Partners

We maintain mutually beneficial partnerships with suppliers, representatives and distributors who are an integral link in the achievement of our mission and guiding values.

Professional Ethics Are Practiced

We manage our business and treat customers, employees, shareholders, investors, suppliers, distributors, representatives, community and government in a manner that exemplifies our honesty, ethics and integrity. We recognize our responsibility to the community and are proud to serve as an equal opportunity employer.

MICROCHIP:
A FULLY INTEGRATED COMPANY
SERVING A GLOBAL MARKET

Propelled by customer requirements....

"Microchip Technology draws its impetus from the technology expectations of a large base of longstanding customers. Microchip is small enough to respond quickly with technology to equate the customer's need. Moreover, as a fully integrated IC Manufacturer, Microchip deploys its panoply of resources to act timely and efficiently, and on a worldwide scale: Design, Technology Development, Mask Shop, Wafer Fabrication, Assembly and Test, Customer Support.

...and powered by continuous improvement...

"World-wide competition leaves no room for divergence or mediocrity. Therefore, Microchip Technology is committed to focus and to continuously improve all the vital aspects of its business. To improve performance, our employees are encouraged to analyze their methods continually. Personal empowerment trespasses the limits of personal responsibility to act in anticipation.

...upfront the wave of technological change.

"Our industry's life-line is innovation. The fast pace of technological change is inherent in our industry. Microchip Technology has accelerated the rate of change of its technology and products to the forefront of the economical feasibility.

"Change is our ally. Driving and managing change is our winning strategy."

Steve Sanghi

President

Microchip Technology Incorporated

A PRODUCT FAMILY OF SHARED STRENGTHS

Microchip's product focus is CMOS nonvolatile memories and programmable microcontrollers. These product lines include EEPROMs, High Speed EPROMs, Flash EPROMs, and PIC® microcontrollers in a broad range of product densities, speeds and packages.

Microchip is quick to capitalize on advances in one product line by incorporating those breakthroughs into other product families. The possibility of enhancing the performance levels of each Microchip product family is explored with every innovation.

MICROCONTROLLERS

Microcontrollers from Microchip combine high performance, low cost, and small package size. They offer the best price/performance ratio in the industry. Large numbers of these devices are used in computer peripherals, data entry, office automation, automotive control systems, security, and cost-sensitive consumer products, such as remote controls and appliances.

The widely accepted PIC16XX (over 75 million shipped) and PIC16CXX series are the industry's only 8-bit based microcontrollers using a high speed RISC architecture. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency. The CMOS PIC16CXX is in volume production, and has achieved over one thousand design wins.

The PIC family is supported by a range of user-friendly development systems, including simulators and in-circuit emulators.

Future CMOS PIC generations will include advanced features, such as higher speed, additional I/O, sophisticated timers, embedded A/D, extended instruction/data memory and inter-processor communication,

SERIAL EEPROMs

Serial EEPROM devices are available in 256 bit, 1K, 2K, 4K, and 16K bit densities. Endurance is greater than 100,000 erase/write cycles. These EEPROMs are ESD protected for greater than 4 kV and operate over a temperature range from -40 °C to +85 °C. They are available in SOIC packages conforming to JEDEC and Japanese standards. The main markets are automotive and consumer products, such as entertainment and telecommunication electronics and appliances.

EEPROMs

The 1.2* micron CMOS EEPROM devices from Microchip are available in 4K, 16K, and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 write and erase cycles. Data retention is over 10 years. Short write times are less than 200 µsec. These EEPROMs work reliably under demanding conditions and have been proven to operate efficiently at temperatures from -55 °C to +125 °C.

* All EEPROMs 4K and greater utilize a 1.2 micron CMOS process.

Common applications include computer peripherals, engine control, pattern recognition and telecommunications.

EPROMs

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. High Speed EPROMs have access times range as low as 45 nano-seconds. Microchip's process flow uniqueness lies in its simplicity. A minimum number of steps allow to offer a reliable family of commodity EPROMs, single metal EPROMs, and double metal EPROMs. Typical applications include computer peripheral, military, instrumentation, and automotive devices.

Microchip's expertise in Plastic Packaging, combined with its previous leadership in the ROM market, led to the development of the Plastic OTP EPROM market where Microchip the #1 supplier today.

MILITARY PRODUCTS

Microchip delivers military devices that conscientious engineers can use with confidence. Our 883C compliant parts cover all quality fronts: DESC standard military drawing approval, high speed performance and quick turn availability.

Microchip's military products include CMOS memories, CMOS/NMOS digital signal processors and microcontrollers - all with high reliability, fast access times and proven retention. Endurance is guaranteed in both dual in-line cerdip packages and leadless chip carriers.

OTHER MICROCHIP PRODUCTS

Other Microchip products, such as DSPs, ICs for serial data communications and sound generation, are mature products with proven track record, and a large, repeat customer base.

Microchip provides a wide package selection of single-chip DSPs that can be programmed for a wide variety of applications. Several variants of the industry standard 32010 and 320C10 are offered at speeds up to 25 MHz. The 320 DSP family is often found in commercial and military applications were medium and high performance parts are required.

The Company's reputation as a quality supplier of DSPs is evidenced by a license agreement with Texas Instruments to second-source the TMS 32010 and TMS 320C10.

Microchip Technology Incorporated

FULLY INTEGRATED MANUFACTURING

Microchip delivers fast turnaround through total control over all phases of production. Design, product development, mask making, wafer fabrication, assembly and quality assurance testing are conducted at facilities owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of statistical process control, continuous improvement and implementation of root cause fixes, has brought forth tight product consistency levels and high yields which enable Microchip to compete successfully in world markets.

A GLOBAL NETWORK OF PLANTS AND FACILITIES

Microchip is a global competitor providing local service to the world's technology centers. The Company's focal point is the design and technology advancement facility in Chandler, Arizona. Most military and high performance parts emanate from here, as well as front end wafer fabrication and electrical probing.

Microchip's assembly and test facility in Kaohsiung, Taiwan houses the technology and modern assembly methods necessary for plastic and ceramic packaging. Select quality conscious firms who fabricate wafers in the Pacific Rim use our Kaohsiung plant for assembly.

Sales and application offices are located in key cities throughout the Western Hemisphere, Pacific Rim and Europe. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical support, purchasing information and failure analysis.

A HISTORY OF INNOVATION

Microchip's history of innovation in the semiconductor industry is as old as the industry itself. For over a quarter century Microchip and its former parent company General Instruments have been developers of cost-effective logic and memory technology and products.

Microchip is credited with a number of firsts: The Metal-Oxide-Silcon (MOS) Integrated Circuit, DRAM, serial EEPROM, Reduced Instruction Set Computer (RISC) microcontroller product family, UART, CMOS 64K EEPROM, and CMOS single chip DSP are all innovations that were originally developed and introduced by our engineers.

STRATEGIC MARKETING FOCUS

Microchip targets selected markets where our advanced designs, progressive process technology and industry leading operating speeds enable us to deliver decidedly superior performance. The firm has recently positioned itself to play a dominant role as a supplier of high performance reprogrammable microcontrollers, and CMOS nonvolatile memories.

FUTURE PRODUCTS

New process technology is constantly being developed for EEPROM, High Speed EPROM, and microcontroller products. Many advanced process technology modules are being developed that will be integrated into our present product lines to achieve a range of compatible processes. Current production technology is attaining 1.2 micron densities. Substantial progress

toward 1 micron and submicron technologies are under development, as well as new CMOS EEPROM, High Speed CMOS EPROM and advanced CMOS RISC-based microcontroller products.

QUALITY WITHOUT COMPROMISE

Product reliability is designed into Microchip products at the outset. Design margins are established to guarantee that every product can be produced easily, error-free and within the tolerances of the manufacturing process.

All our quality assurance tests are run tighter than customer specifications. Products are tested at least two machine tolerances higher than those specified by the customer.

Every new product is measured under accelerated stress testing. Test samples encompass the full range of processed tolerances at each step. Data sheets detailing these processes enable customers to reach accurate decisions based on known quantitative values.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at each process step. In-process controls are performed by operators in the wafer fabrication division and immediate corrective action is taken if they deem a process is out of control. Products are also sampled weekly through a variety of carefully monitored stress and accelerated life tests.

Microchip's positive documentation control program assures the correct document is always available at the point of use. Active documents are serialized and stamped to eliminate the possibility of performing a job from obsolete or incorrect instructions.

Individuals in all departments are required to analyze the methods employed at their positions and formulate plans to improve performance. The evaluation process is never exhausted. Screening efforts alone are never considered enough. In all areas of our business, everyone is expected to make continuous improvement.

RESEARCH AND DEVELOPMENT OF PERFORMANCE PRODUCTS

Microchip's research and development activities, include exploring new process technologies and products that have industry leadership potential. Particular emphasis is placed on products that can be put to work in high performance niche markets.

Equipment is continually updated to bring the most sophisticated process, CAD and testing tools on line. Cycle times for new technology development are continuously reduced by using a pilot line within the manufacturing facility.

FORMING A PERFORMANCE ALLIANCE WITH CUSTOMERS

Microchip works in tangent with customers to establish mutual programs to improve the performance of our products in their systems. We go beyond the incoming inspection level and specification by extending our quality responsibility to the point where the customer ships the system. Microchip's quality programs ensure that our products can be used with such impunity, a customer can implement improvement programs centered on us as a supplier.

NOTES:

SECTION 1
SERIAL EEPROM PRODUCT SPECIFICATIONS

Microchip

24C01A

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

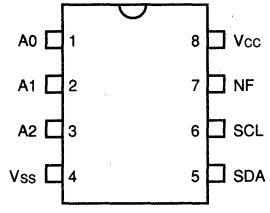
- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

DESCRIPTION

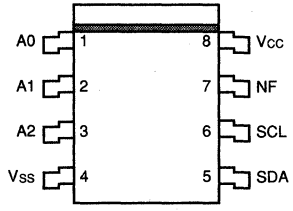
The Microchip Technology Inc 24C01A is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 24C01As may be connected to the two wire bus. The 24C01A is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

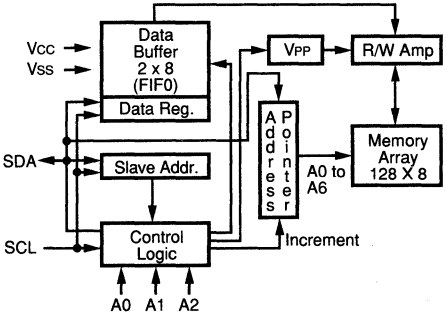
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ....+300°C
ESD protection on all pins .....4 kV

***Notice**: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NF	No Function
VCC	+5 V Power Supply

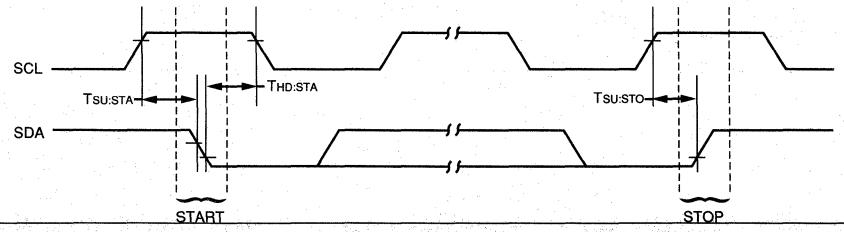
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = 0°C to 70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = (I) and (E)
program cycle	ICCW		7.0	mA	VCC = 5 V, Tamb = 0°C to +70°C
			8.5	mA	VCC = 5 V, Tamb= (I) and (E)
read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

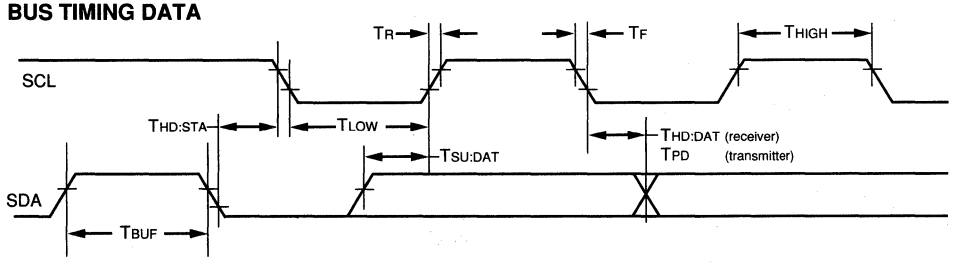


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C01A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 24C01A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

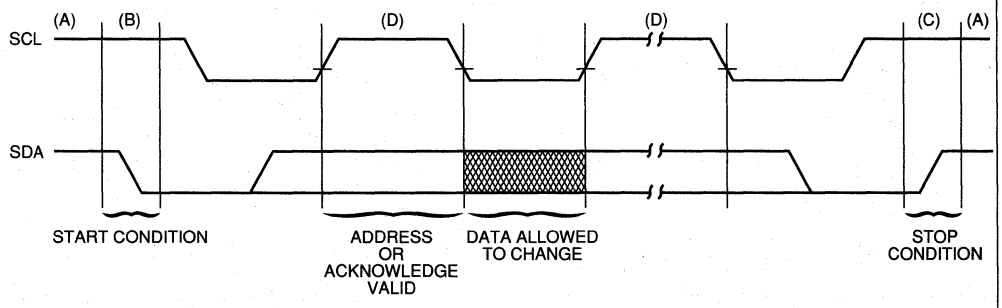
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

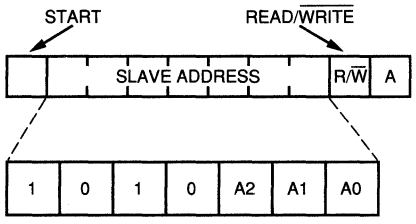
The chip address inputs A0, A1 and A2 of each 24C01A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A a unique 3-bit address. Up to eight 24C01As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C01A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A. (See Figure2.)

The 24C01A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 24C01A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A. The most significant bit of the word address is a "Do Not Care" value for the 24C01A. After receiving the acknowledge of the 24C01A, the master device transmits the data word to be written into the addressed memory location. The 24C01A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A. (See Figure 3).

PAGE PROGRAM MODE

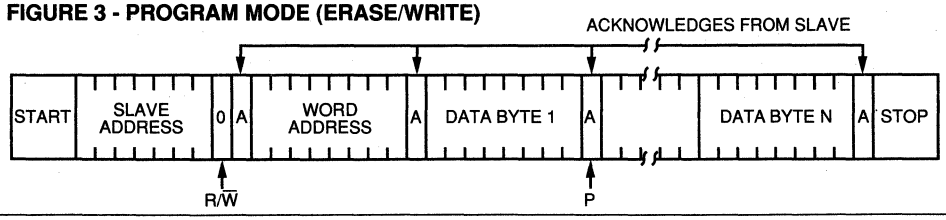
To program the 24C01A, the master sends addresses and data to the 24C01A which is the slave, (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One do not care bit and seven address bits.) The 24C01A will generate an acknowledge after every 8-bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C01A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 24C01A.

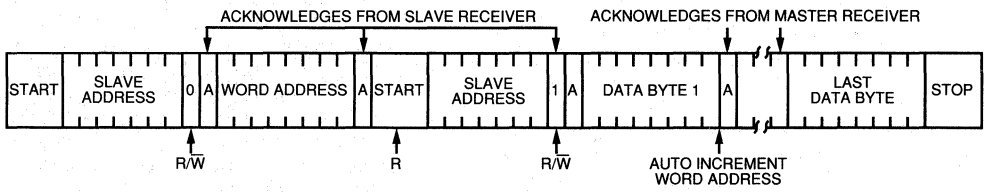
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C01A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will automatically increment from the end of the memory block (128 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C01As can be connected to the bus.

These inputs must be connected to either V_{SS} or V_{CC}.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NF No Function

Must be connected to either V_{SS} or V_{CC}.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C01A page is 2 bytes long.

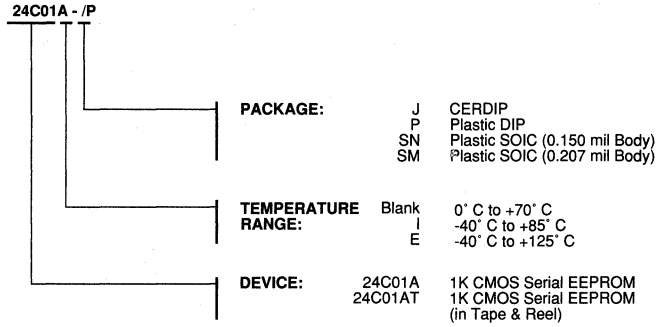
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C01A has only one block (128 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



24C01A

DICE FORM

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

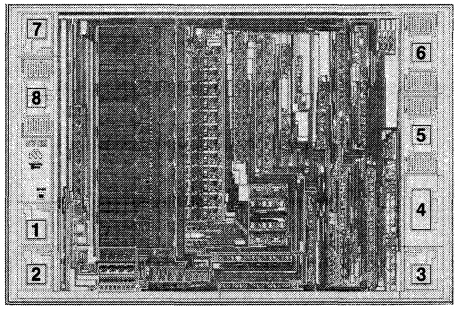
- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 24C01A is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 24C01As may be connected to the two wire bus. The 24C01A dice are available in wafer or wafflepack package.

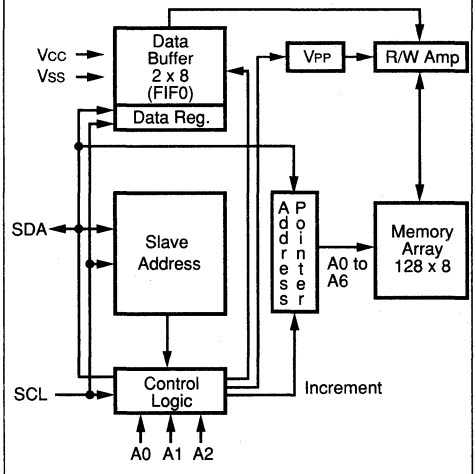
DIE CONFIGURATION

Die Size: 106 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	NF
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3V to +7V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

***Notice**: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NF	No Function
VCC	+5 V Power Supply

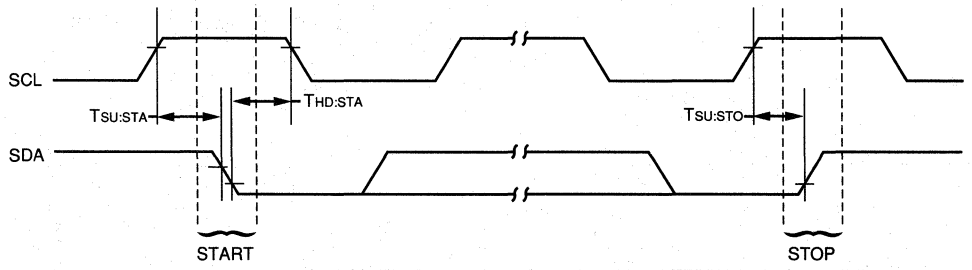
DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V,
program cycle	ICCW		7.0	mA	VCC = 5 V
read cycle	ICCR		750	µA	VCC = 5 V
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

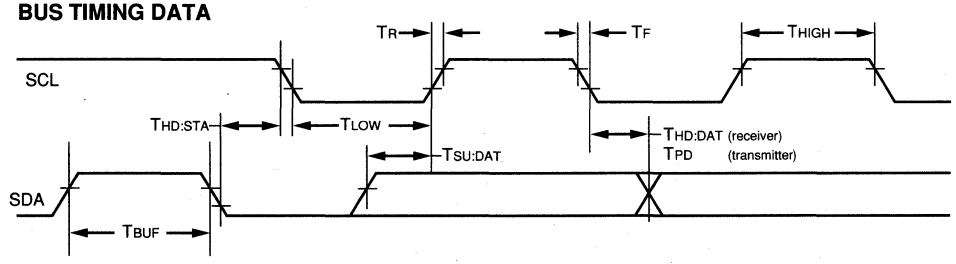


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock Frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C01A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 24C01A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

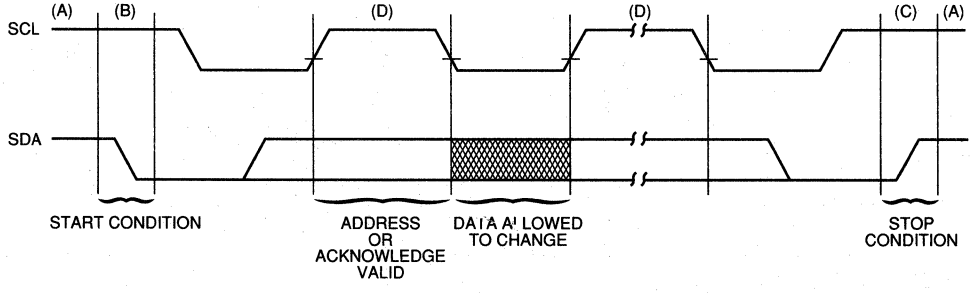
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER ON THE SERIAL BUS



SLAVE ADDRESS

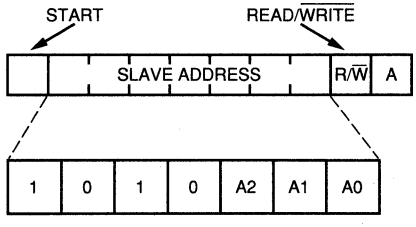
The chip address inputs A0, A1 and A2 of each 24C01A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A a unique 3-bit address. Up to eight 24C01As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C01A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A. (See Figure 2.)

The 24C01A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C01A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A. The most significant bit of the word address is a "Do Not Care" value for the 24C01A. After receiving the acknowledge of the 24C01A, the master device transmits the data word to be written into the addressed memory location. The 24C01A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A. (See Figure 3.)

PAGE PROGRAM MODE

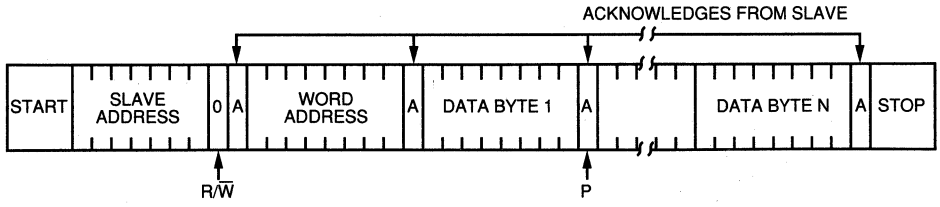
To program the 24C01A, the master sends addresses and data to the 24C01A which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One do not care bit and seven address bits.) The 24C01A will generate an acknowledge after every 8-bits received and store them consecutively in a 2- byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C01A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

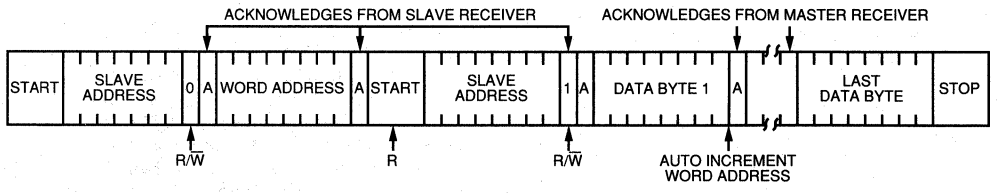
This mode illustrates master device reading data from the 24C01A.

As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C01A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C01As can be connected to the bus.

These inputs must be connected to either V_{SS} or V_{CC}.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NF No Function

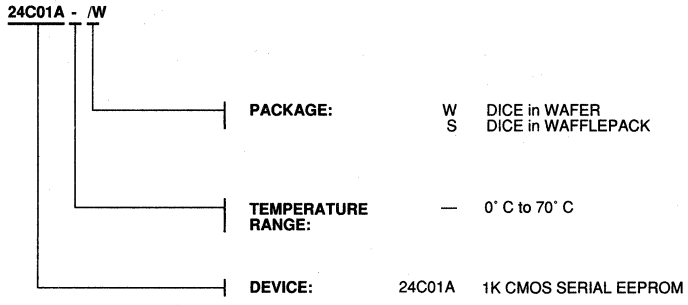
Must be connected to either V_{SS} or V_{CC}.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24C02A

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

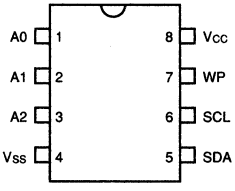
- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Hardware write protect for upper 1K (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

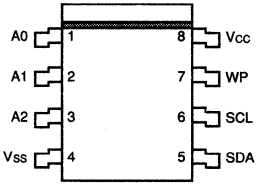
The Microchip Technology Inc. 24C02A is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 1K (128 x 8). The 24C02A also has a page-write capability for up to 2 bytes of data. Up to eight 24C02As may be connected to the two wire bus. The 24C02A is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

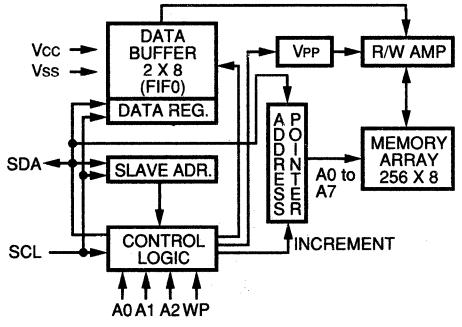
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+5 V Power Supply

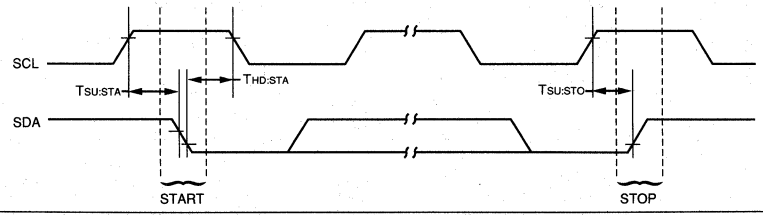
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) TAMB = 25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V, Tamb = 0°C to 70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V, Tamb = (I) and (E)
program cycle	ICCW		7.0	mA	Vcc = 5 V, Tamb = 0°C to +70°C
			8.5	mA	Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb = (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

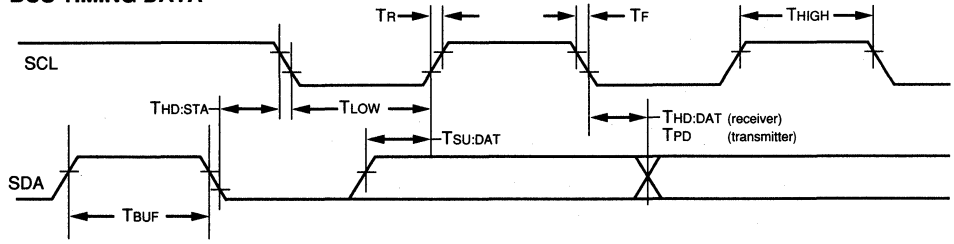


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C02A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C02A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C02As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 24C02A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

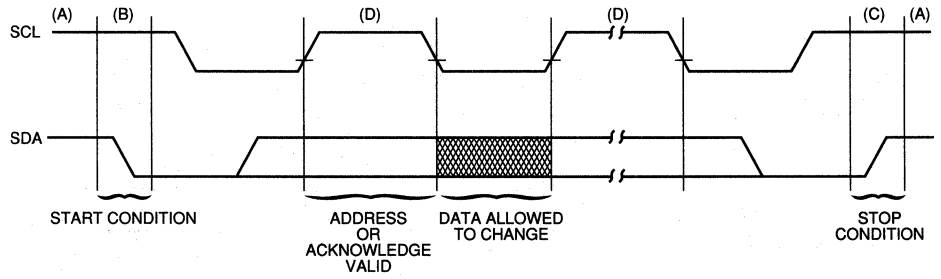
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C02A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

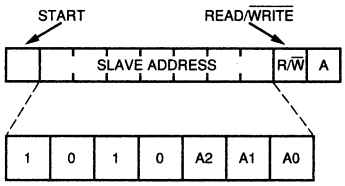
The chip address inputs A0, A1 and A2 of each 24C02A must be externally connected to either Vcc or ground (Vss), assigning to each 24C02A a unique 3-bit address. Up to eight 24C02As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24C02A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C02A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C02A. (See Figure 2.)

The 24C02A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 24C02A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C02A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C02A. After receiving the acknowledge of the 24C02A, the master device transmits the data word to be written into the addressed memory location. The 24C02A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C02A. (See Figure 3.)

PAGE PROGRAM MODE

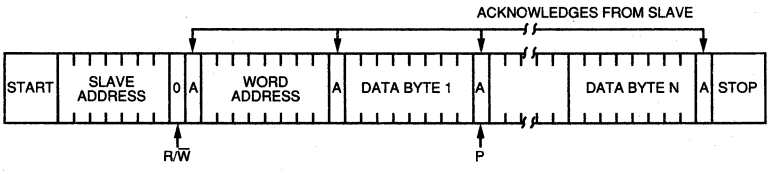
To program the 24C02A, the master sends addresses and data to the 24C02A which is the slave. (See Figure 3.) This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C02A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 24C02A will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C02A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A is connected to Vcc (+5 V). The 24C02A will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C02A.

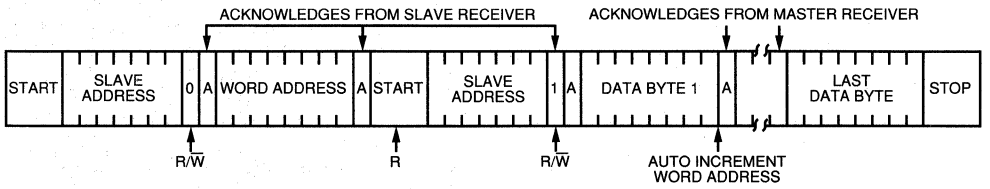
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: although this is a read mode the address pointer must be written to.) During this period the 24C02A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C02As can be connected to the bus. These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pin must be connected to either Vss or Vcc.

If tied to Vcc, PROGRAM operations onto the upper half of memory (addresses 080—0FF) will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000—0FF).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C02A page is 2 bytes long.

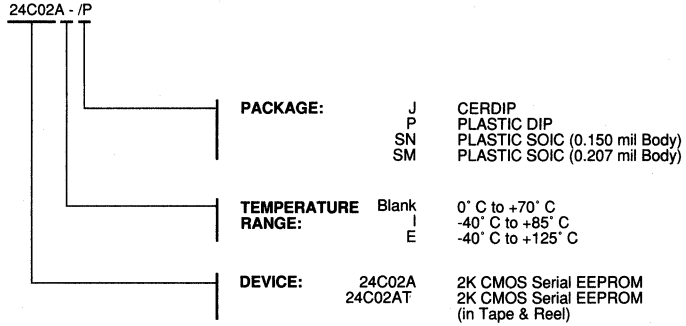
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C02A has only one block (256 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24C02A

DICE FORM

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

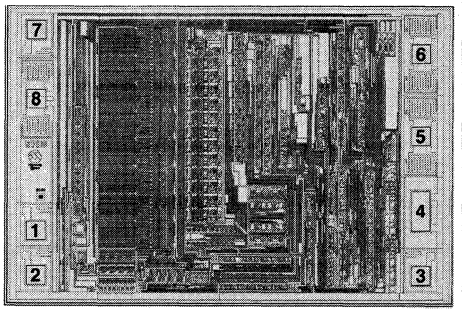
- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Hardware write protect for upper 1k (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc 24C02A is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 1k (128 x 8). The 24C02A also has a page-write capability for up to 2 bytes of data. Up to eight 24C02As may be connected to the two wire bus. The 24C02A dice are available in wafer or wafflepack package.

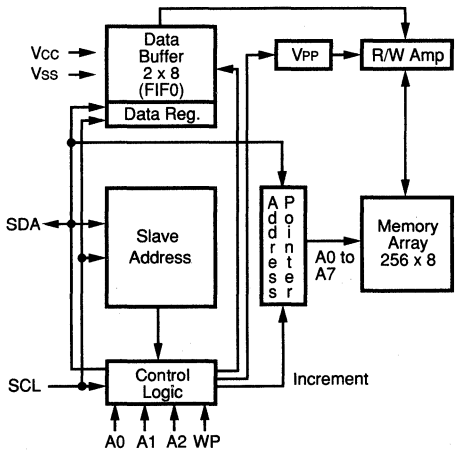
DIE CONFIGURATION

Die Size: 106 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	WP
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

All inputs and outputs w.r.t. Vss .....-0.3V to +7V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+5 V Power Supply

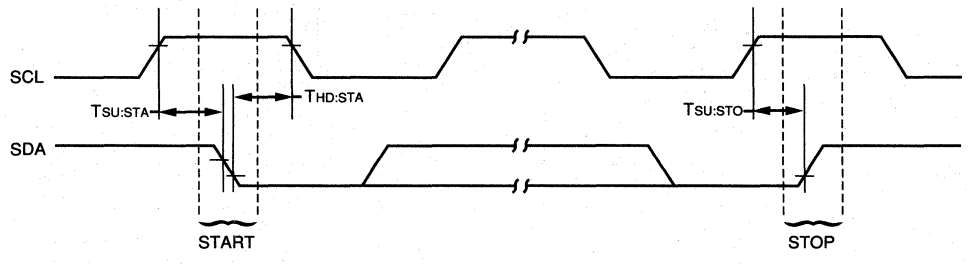
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V,
program cycle	ICCW		7.0	mA	Vcc = 5 V
read cycle	ICCR		750	µA	Vcc = 5 V
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

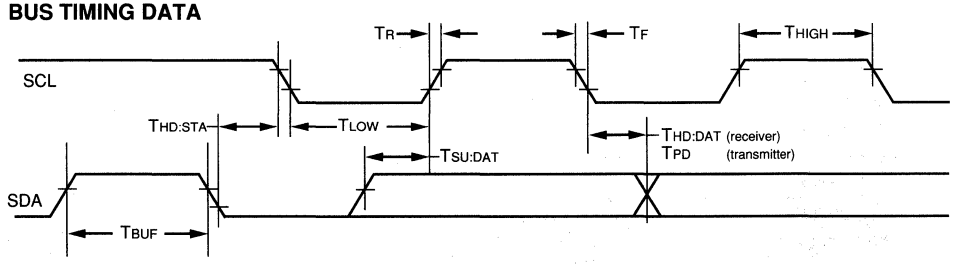


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C02A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C02A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C02As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 24C02A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During the data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOPp condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

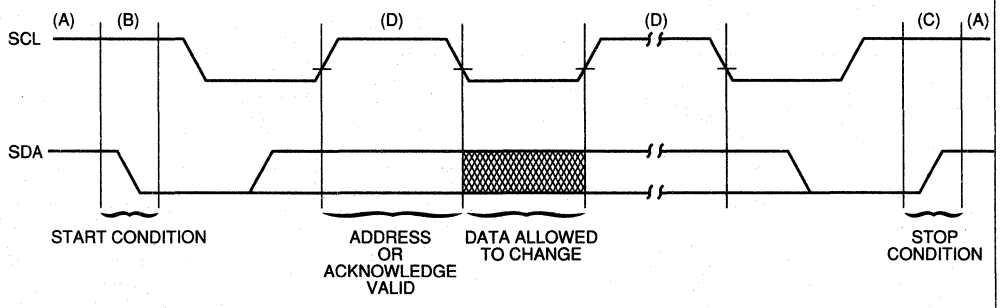
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C02A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

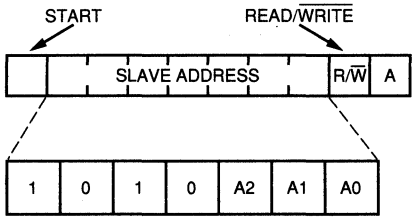
The chip address inputs A0, A1 and A2 of each 24C02A must be externally connected to either Vcc or ground (Vss), assigning to each 24C02A a unique 3-bit address. Up to eight 24C02As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24C02A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C02A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C02A. (See Figure 2.)

The 24C02A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C02A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C02A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C02A. After receiving the acknowledge of the 24C02A, the master device transmits the data word to be written into the addressed memory location. The 24C02A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C02A. (See Figure 3.)

PAGE PROGRAM MODE

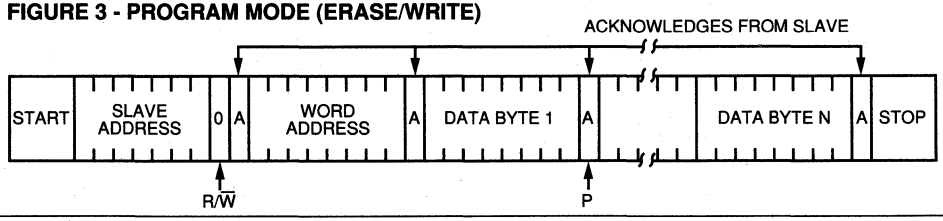
To program the 24C02A, the master sends addresses and data to the 24C02A which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C02A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 24C02A will generate an acknowledge after every 8-bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C02A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 2) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pad of the 24C02A is connected to Vcc (+5 V). The 24C02A will accept slave and word addresses but if the memory accessed is write protected by the WP pad, the 24C02A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C02A.

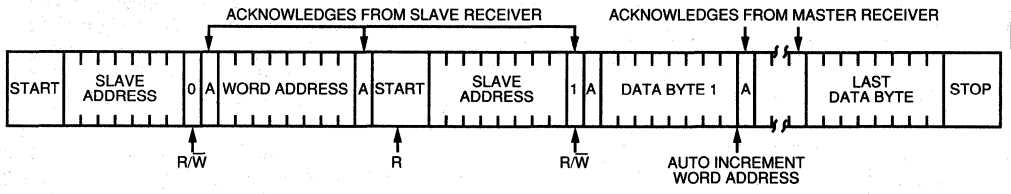
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C02A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 bytes) back to the first location in that block.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C02As can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pad must be connected to either VCC or VSS.

If tied to Vcc, PROGRAM operations onto the upper memory page (addresses 080—0FF) will not be executed. READ operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000—0FF).

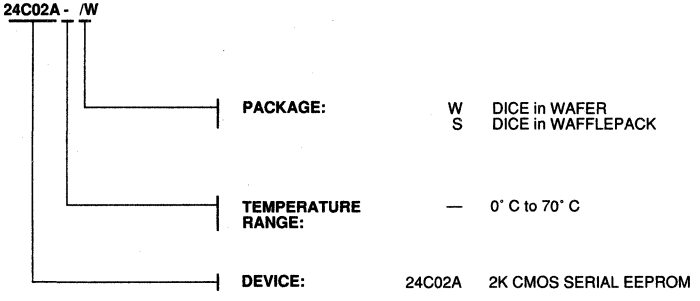
This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24C04A

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

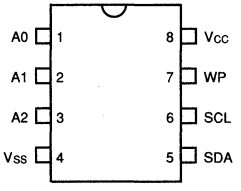
- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Hardware write protect for upper block
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +85°C

DESCRIPTION

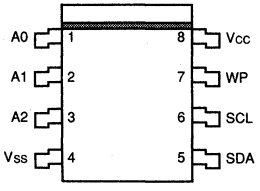
The Microchip Technology Inc. 24C04A is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 256 byte block. The 24C04A also has a page-write capability for up to 8 bytes of data. Up to four 24C04As may be connected to the two wire bus. The 24C04A is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

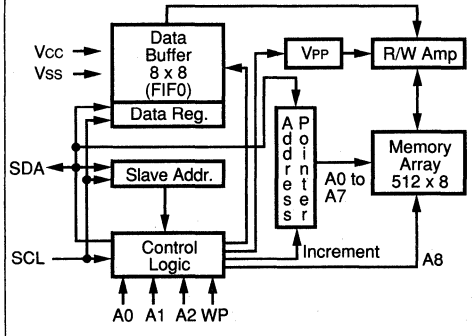
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

***Notice**: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	No Function, Must be connected to VCC or VSS
A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+5 V Power Supply

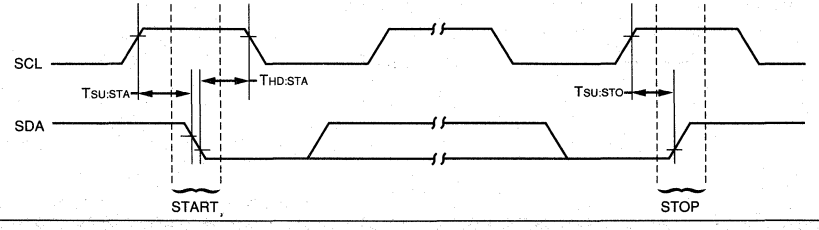
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive: (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = (I) and (E)
program cycle	ICCW		7.0	mA	VCC = 5 V, Tamb = 0°C to +70°C
			8.5	mA	VCC = 5 V, Tamb= (I) and (E)
read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

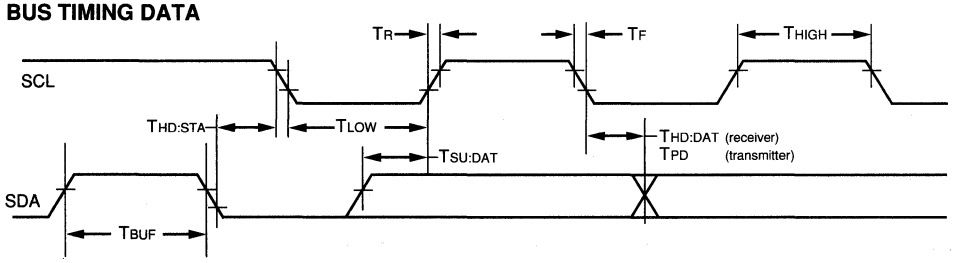


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C04A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C04As can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to VCC or VSS. Other devices can be connected to the bus but require different device codes than the 24C04A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

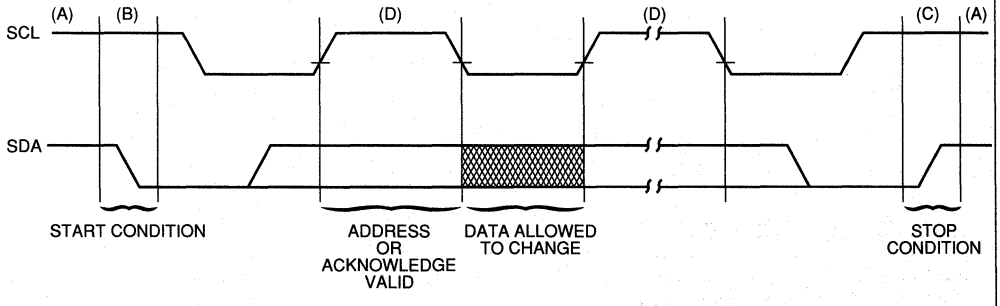
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

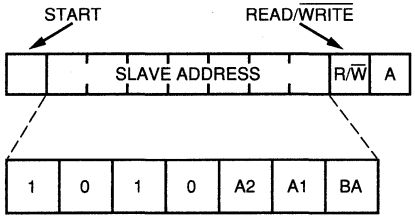
The chip address inputs A1 and A2 of each 24C04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C04A a unique2-bit address. Up to four 24C04As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C04A. A0 is not used and must be connected to either Vcc or Vss.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C04A, followed by the chip address bits A1 and A2. The seventh bit of that byte (BA) is used to select the upper block (addresses 100—1FF) or lower page (addresses 000—0FF) of the 24C04A.

The eighth bit of slave address determines if the master device wants to read or write to the 24C04A. (See Figure 2.)

The 24C04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C04A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C04A. After receiving the acknowledge of the 24C04A, the master device transmits the data word to be written into the addressed memory location. The 24C04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C04A. (See Figure 3.)

PAGE PROGRAM MODE

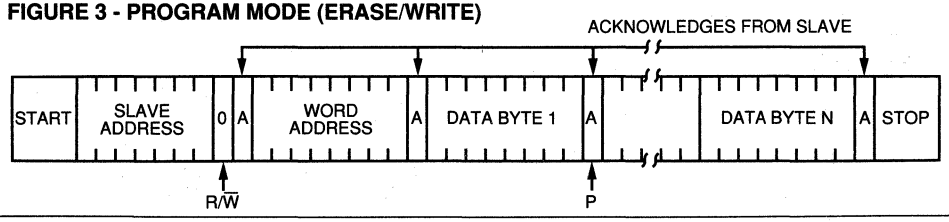
To program the 24C04A, the master sends addresses and data to the 24C04A which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The BA bit transmitted with the slave address is the ninth bit of the address pointer.) The 24C04A will generate an acknowledge after every 8-bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 24C04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to eight) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C04A is connected to Vcc (+5 V). The 24C04A will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C04A.

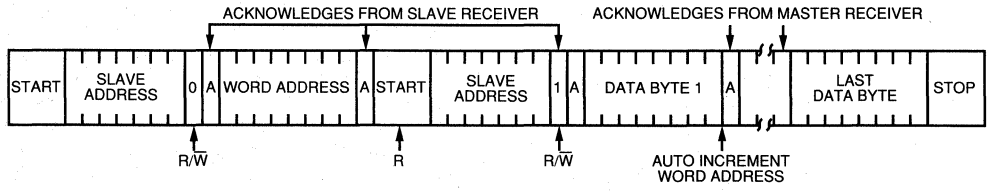
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0

This pin must be connected to either Vcc or Vss.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 24C04As can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pin must be connected to either Vcc or Vss.

If tied to Vcc, PROGRAM operations onto the upper memory block (addresses 100—1FF) will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000—1FF).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long.

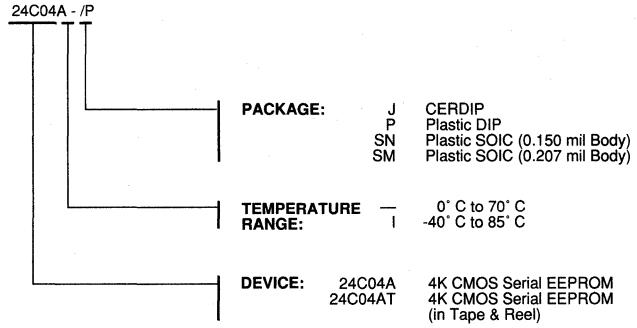
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



24C04A

DICE FORM

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

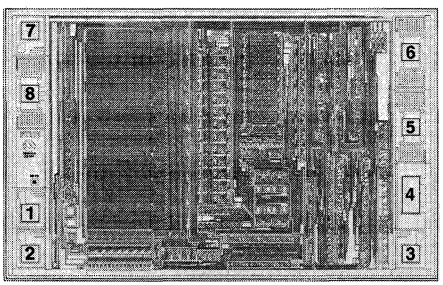
- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Hardware write protect for upper block
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 24C04A is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 256 byte block. The 24C04A also has a page-write capability for up to 8 bytes of data. Up to four 24C04As may be connected to the two wire bus. The 24C04A dice are available in wafer or wafflepack package.

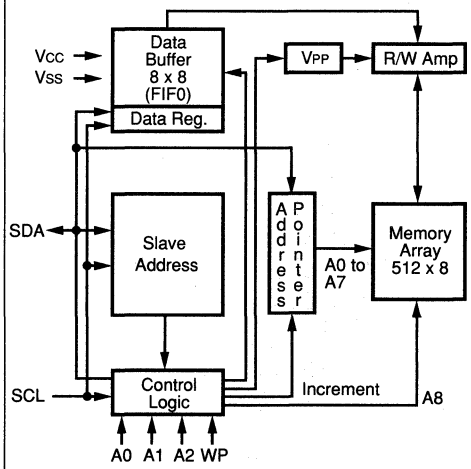
DIE CONFIGURATION

Die Size: 113 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	WP
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+5 V Power Supply

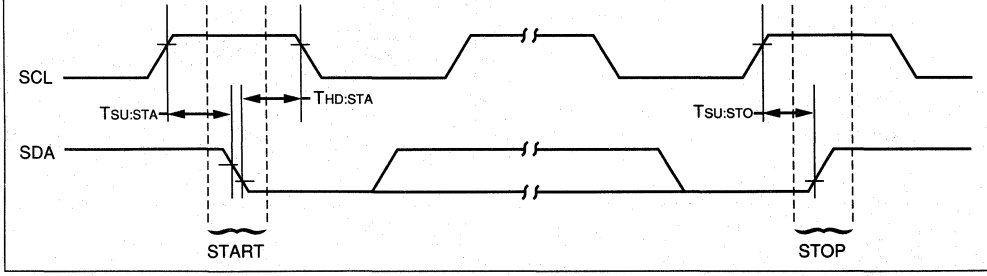
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V,
program cycle	ICCW		7.0	mA	VCC = 5 V
read cycle	ICCR		750	µA	VCC = 5 V
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

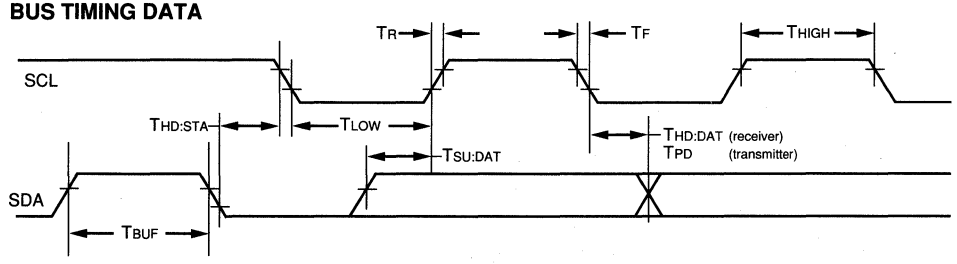
BUS TIMING START/STOP



AC CHARACTERISTICS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C04A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C04A can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to VCC or VSS. Other devices can be connected to the bus but require different device codes than the 24C04A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Tansfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

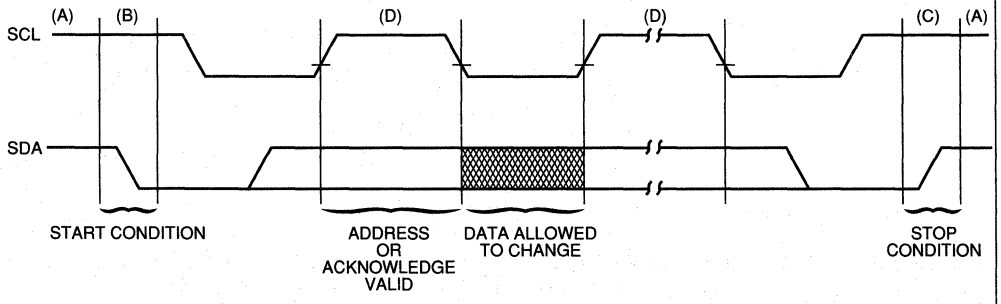
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE



SLAVE ADDRESS

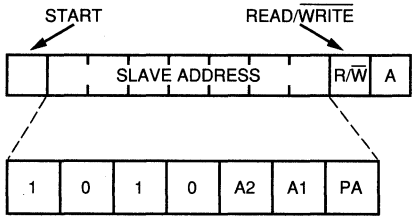
The chip address inputs A1 and A2 of each 24C04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C04A a unique 2-bit address. Up to four 24C04As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C04A. A0 is not used and must be connected to Vcc or Vss.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C04A, followed by the chip address bits A1 and A2. The seventh bit of that byte (PA) is used to select the upper page (addresses 100—1FF) or lower page (addresses 000—0FF) of the 24C04A.

The eighth bit of slave address determines if the master device wants to read or write to the 24C04A. (See Figure 2.)

The 24C04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 24C04A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C04A. After receiving the acknowledge of the 24C04A, the master device transmits the data word to be written into the addressed memory location. The 24C04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C04A. (See Figure 3.)

PAGE PROGRAM MODE

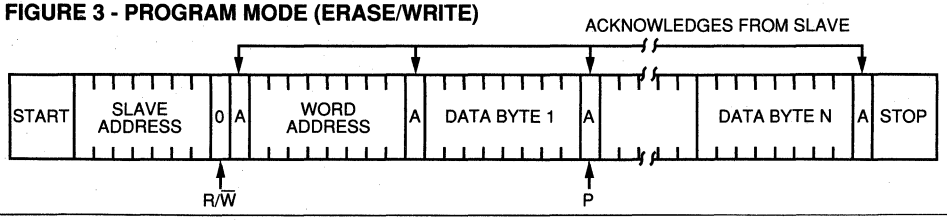
To program the 24C04A, the master sends addresses and data to the 24C04A which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The PA bit transmitted with the slave address is the ninth bit of the address pointer.) The 24C04A will generate an acknowledge after every 8-bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 24C04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to eight) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pad of the 24C04A is connected to VCC (+5 V). The 24C04A will accept slave and word addresses but if the memory accessed is write protected by the WP pad, the 24C04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C04A.

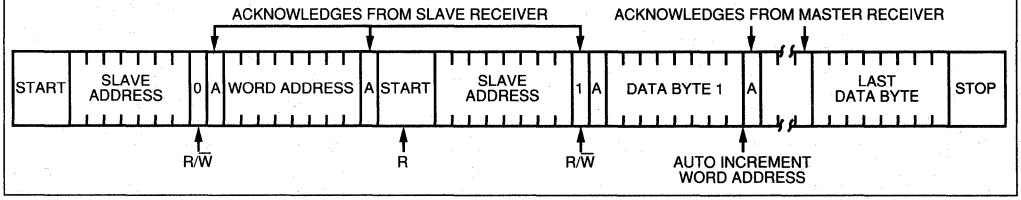
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will never automatically increment through a block (256 byte) boundary but will rotate back to the first location in that block.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0

This pad must be connected to either VCC or VSS.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 24C04As can be connected to the bus.

These inputs must be connected to either VSS or VCC.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pad must be connected to either VCC or VSS.

If tied to VCC, PROGRAM operations onto the upper memory block (addresses 100—1FF) will not be executed. Read operations are possible.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000—1FF).

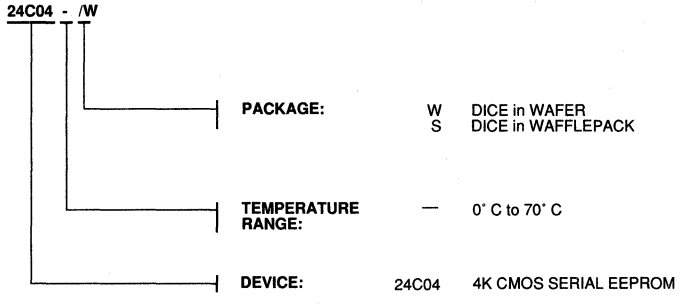
This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



59C11

1K (128 x 8 or 64 x 16) CMOS Serial Electrically Erasable PROM

FEATURES

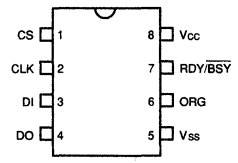
- Low power CMOS technology
- Pin selectable memory organization
  - — 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/$\overline{BSY}$ status information during WRITE
- Power on/off data protection circuitry
- 100,000 ERASE/WRITE cycles
- Data Retention > 10 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

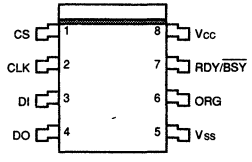
The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

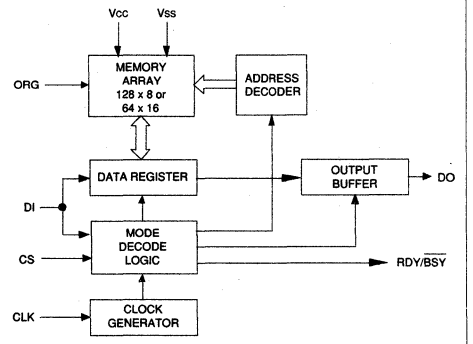
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7.0 V
Storage temperature .....-65°C to +150°C
Ambient temperature with
power applied .....65°C to +125°C
Soldering temperature of leads (10 seconds) ....+300°C
ESD protection on all pins .....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
ORG	Memory Array Organization
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Status
VCC	+5 V Power Supply

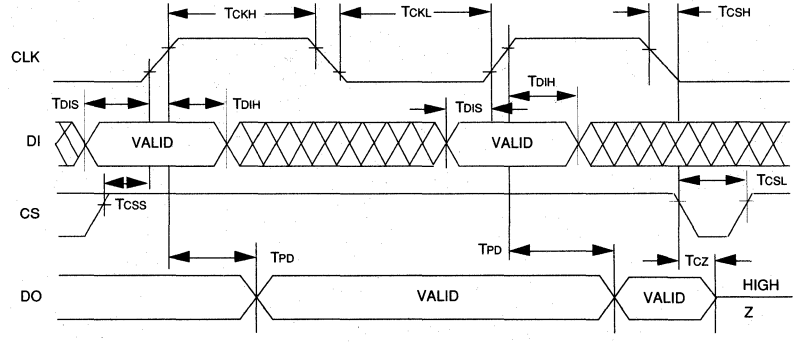
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	ICCO		4	mA	FCLK = 1 MHz, VCC =5.5 V
Standby current	ICCS		100	µA	CS = 0 V, VCC = 5.5 V

Note 1: Internal resister pull-up at Pin 6. Active output at Pin 7.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCS	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/$\overline{\text{BSY}}$ delay time	TRBD		400	ns	
Program cycle time (Auto Erase & Write)	TWC		1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (TCSL) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (TCKH) and clock low time (TCKL)). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become "Don't Care" inputs until CS is brought LOW for at least chip select low time (TCSL) and brought HIGH again and a WRITE cycle (if any) is completed.

Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

Ready/Busy (RDY/$\overline{BSY}$)

Pin 7 provides RDY/$\overline{BSY}$ status information. RDY/$\overline{BSY}$ is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

DATA PROTECTION

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.8 V and 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when VCC has fallen below the voltage range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed.

INSTRUCTION SET — **64 X 16 MODE, ORG=1**

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15 – D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15 – D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15 – D0	High-Z	27

128 X 8 MODE, ORG=0

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7 – D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7 – D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D15 – D0	High-Z	20

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note: CS must go LOW between consecutive instructions.

DI/DO Pins

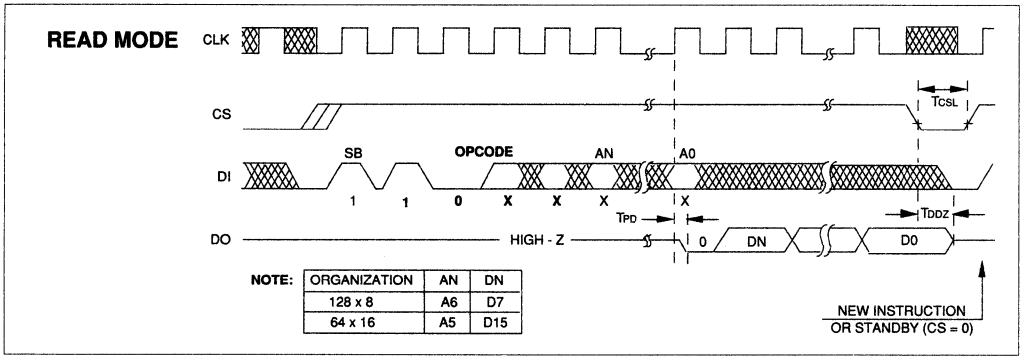
It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).

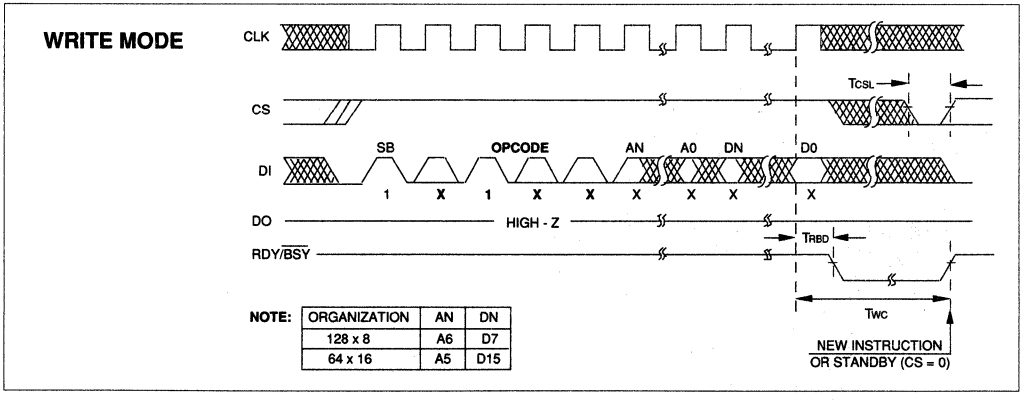


NOTE:	ORGANIZATION	AN	DN
	128 x 8	A6	D7
	64 x 16	A5	D15

WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms max for 8-bit mode and 2 ms max for 16-bit mode.

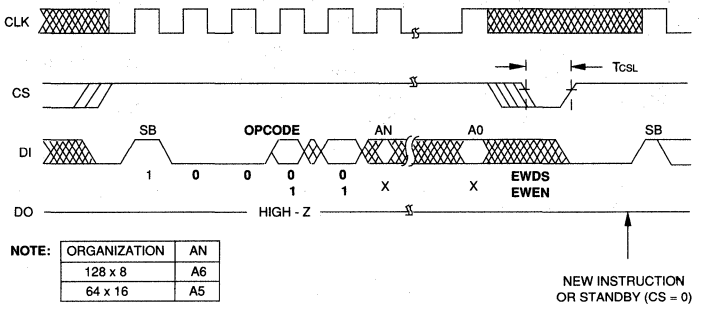


NOTE:	ORGANIZATION	AN	DN
	128 x 8	A6	D7
	64 x 16	A5	D15

ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device.

ERASE/WRITE ENABLE AND DISABLE

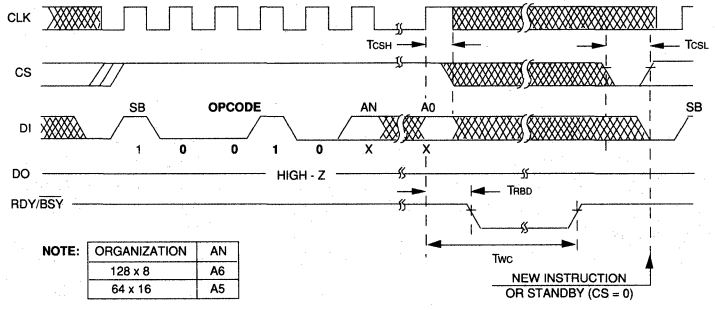


NOTE:	ORGANIZATION	AN
	128 x 8	A6
	64 x 16	A5

ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms max.

ERASE ALL (CHIP ERASE)



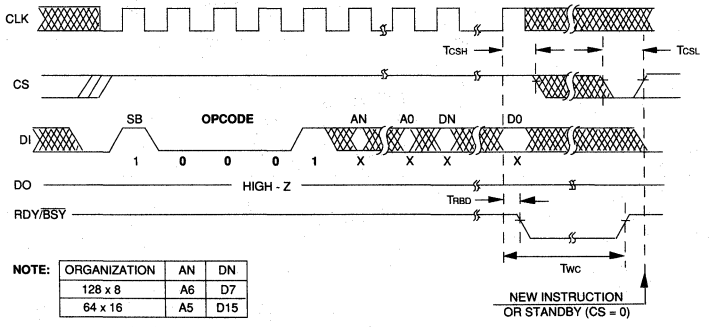
NOTE:	ORGANIZATION	AN
	128 x 8	A6
	64 x 16	A5

WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

WRITE ALL



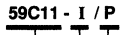
NOTE:	ORGANIZATION	AN	DN
	128 x 8	A6	D7
	64 x 16	A5	D15

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package:	J	CERDIP
	P	Plastic DIP
	SN	Plastic SOIC (0.150 mil Body)
	SM	Plastic SOIC (0.207 mil Body)
Temperature Range:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
Device:	59C11	1K CMOS Serial EEPROM
	59C11T	1K CMOS Serial EEPROM (in Tape & Reel)

Microchip

59C11

DICE FORM

1K (128 x 8 or 64 x 16) CMOS Serial Electrically Erasable PROM

FEATURES

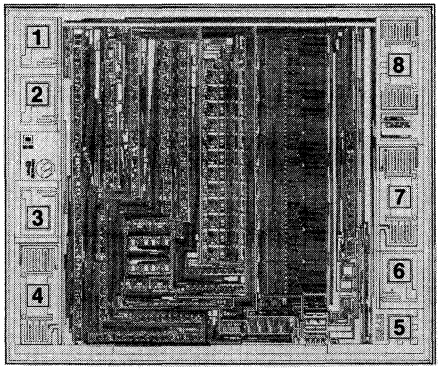
- Low power CMOS technology
- Pad selectable memory organization
  — 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self-timed write, ERAL and WRAL cycles
- Automatic erase before write
- RDY/$\overline{BSY}$ status information during write
- Power on/off data protection circuitry
- Available in wafer or wafflepack
- Temperature range:
  — Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pad ORG. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 59C11 dice are available in wafer or wafflepack.

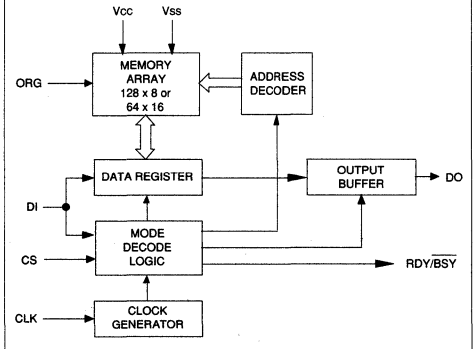
DIE CONFIGURATION

Die Size: 88 x 78 mils.



1. CS
2. CLK
3. DI
4. DO
8. Vcc
7. RDY/BSY
6. ORG
5. Vss

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
ORG	Memory Array Organization
RDY/BSY	Ready/Busy Status
Vcc	+5 V Power Supply

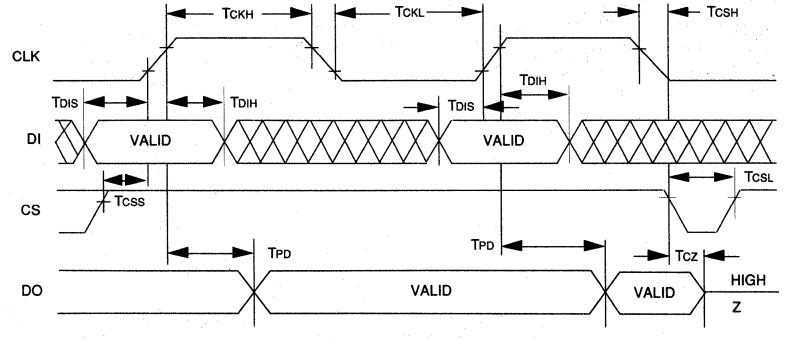
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, Vcc = 5.5 V
Standby current	ICCS		100	uA	CS = 0 V, Vcc = 5.5 V

Note 1: Internal resistor pull-up at Pin 6. Active output at Pin 7.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCS	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/$\overline{\text{BSY}}$ delay time	TRBD		400	ns	
Program cycle time (Auto Erase & Write)	TWC		1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

PAD DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (TCSL) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL)). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a start condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e. auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become don't care inputs until CS is brought LOW for at least chip select low time (TCSL) and brought HIGH again and a WRITE cycle (if any) is completed.

Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

Organization (ORG)

This input selects the memory array organization. When the ORG pad is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pad is left unconnected, then an internal pullup device will select the 64 x 16 organization.

Ready/Busy (RDY/BSY)

Pad 7 provides RDY/BSY status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH, the internal self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

DATA PROTECTION

During power-up all modes of operation are inhibited until Vcc has reached a level of between 2.8 Vand 4.5 V. During power-down the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the voltage range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed.

INSTRUCTION SET — **64 X 16 MODE, ORG=1**

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15 – D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15 – D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15 – D0	High-Z	27

128 X 8 MODE, ORG=0

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7 – D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7 – D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7 – D0	High-Z	20

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become "don't care" bits until a new start condition is detected.

Note:

CS must go LOW between consecutive instructions.

DI/DO Pads

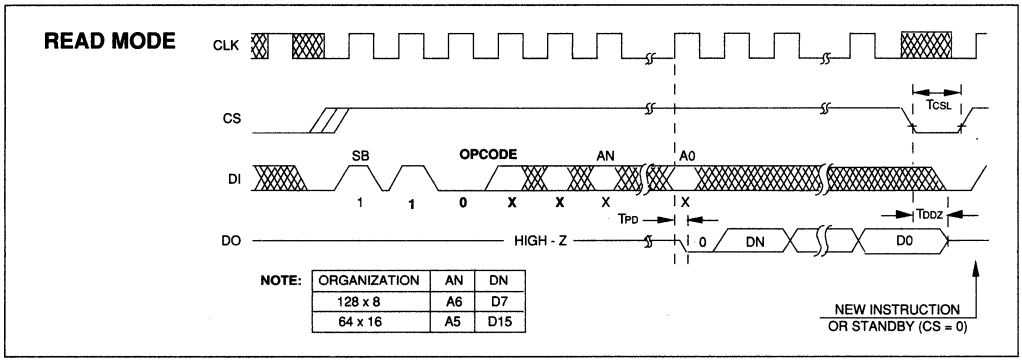
It is possible to connect the Data In and Data Out pads together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pad.

READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pad. A dummy bit (logical 0) precedes the 8/16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).



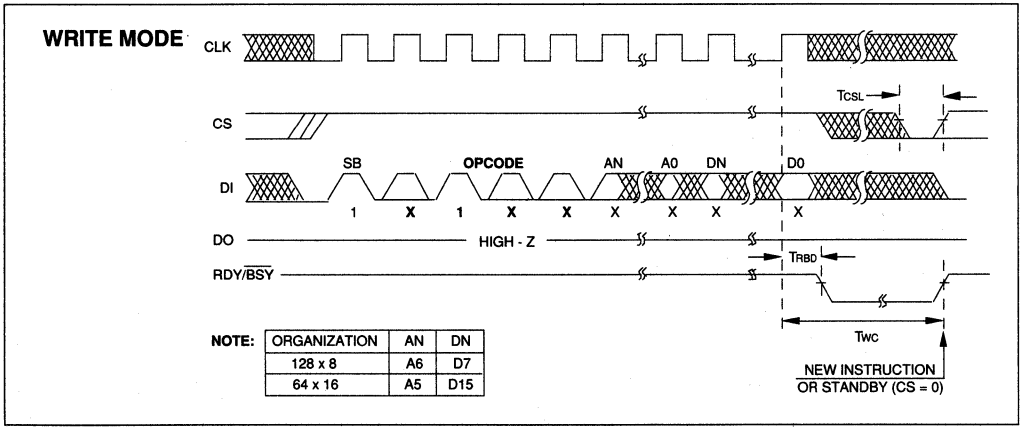
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

WRITE Mode

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the last data bit (D0) has been clocked in.

The WRITE cycle takes 1 ms for 8-bit mode and 2 ms for 16-bit mode max.



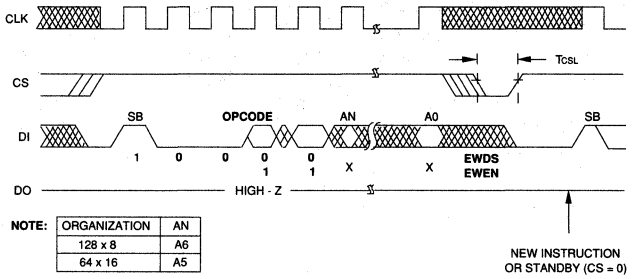
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

ERASE/WRITE Enable/Disable (EWEN,EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device.

ERASE/WRITE ENABLE AND DISABLE



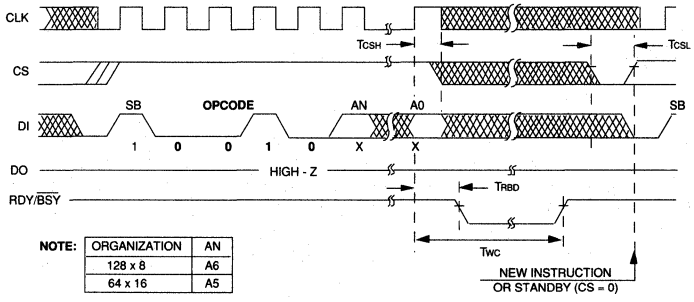
NOTE:	ORGANIZATION	AN
	128 x 8	A6
	64 x 16	A5

ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode.

The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in. ERAL takes 15 ms max in both 8-bit and 16-bit modes.

ERASE ALL (CHIP ERASE)



NOTE:	ORGANIZATION	AN
	128 x 8	A6
	64 x 16	A5

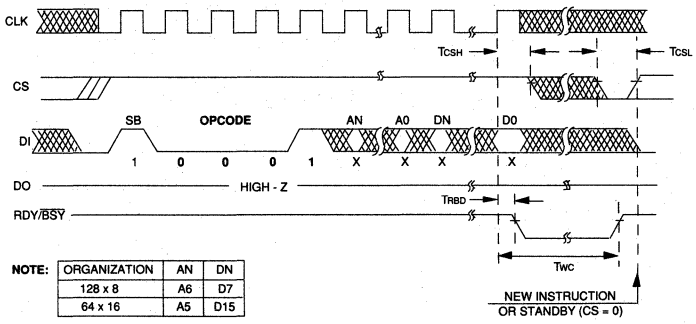
WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max in both 8-bit and 16-bit modes.

Note: The WRAL does not include an automatic erase cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

WRITE ALL



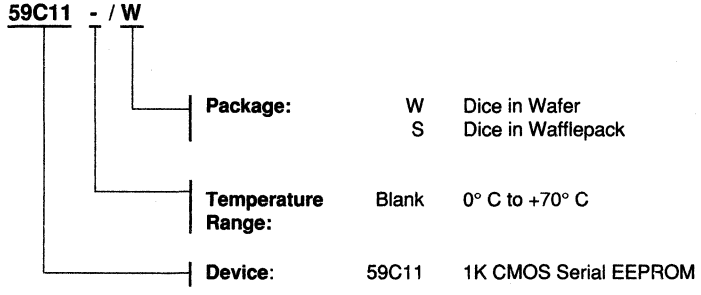
NOTE:	ORGANIZATION	AN	DN
	128 x 8	A6	D7
	64 x 16	A5	D15

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C72

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

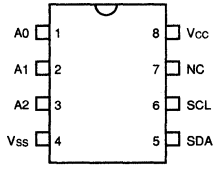
- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

DESCRIPTION

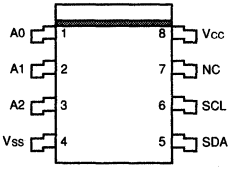
The Microchip Technology Inc. 85C72 is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 85C72s may be connected to the two wire bus. The 85C72 is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

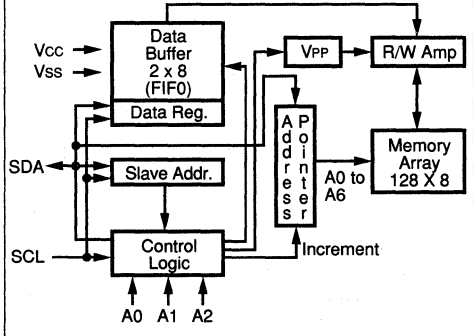
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4.0 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NC	No Connect
VCC	+5 V Power Supply

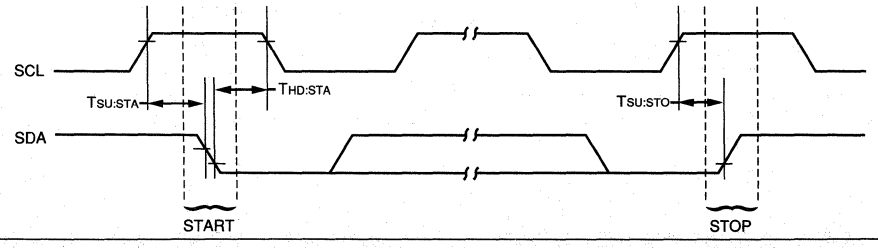
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = (I) and (E)
Program cycle	ICCW		7.0	mA	VCC = 5 V, Tamb = 0°C to +70°C
			8.5	mA	VCC = 5 V, Tamb= (I) and (E)
Read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

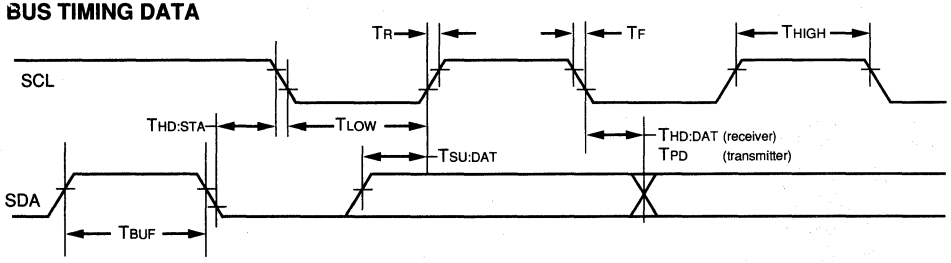


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C72 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the start and STOP conditions, while the 85C72 works as slave.

Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 85C72s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C72 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

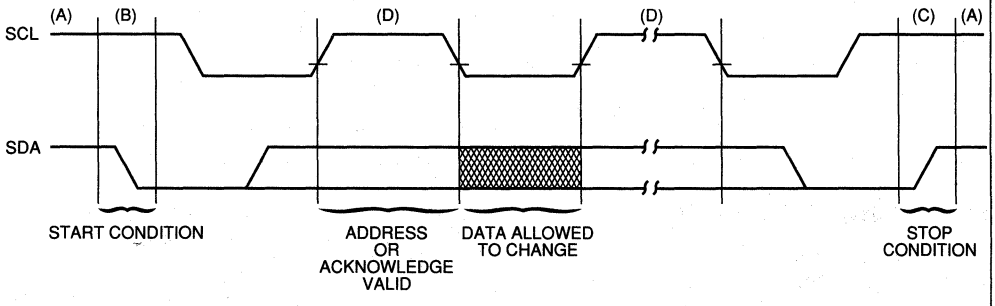
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

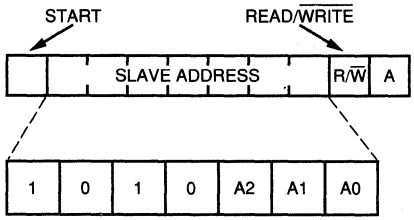
The chip address inputs A0, A1 and A2 of each 85C72 must be externally connected to either VCC or ground (VSS), assigning to each 85C72 a unique 3-bit address. Up to eight 85C72s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C72.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72. (See Figure 2.)

The 85C72 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 85C72.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72. The most significant bit of the word address is a "Do Not Care" value for the 85C72. After receiving the acknowledge of the 85C72, the master device transmits the data word to be written into the addressed memory location. The 85C72 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72. (See Figure 3.)

PAGE PROGRAM MODE

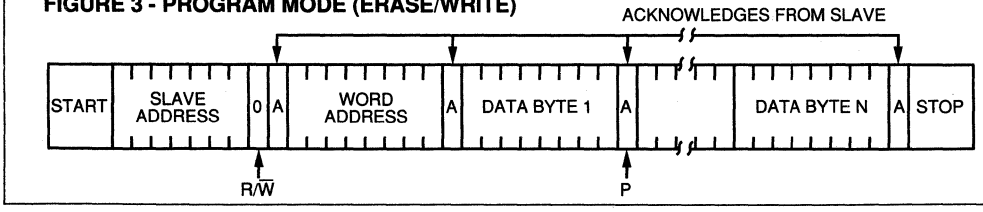
To program the 85C72, the master sends addresses and data to the 85C72 which is the slave. (See Figure 3.) This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One " Do Not Care" bit and seven address bits.) The 85C72 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C72.

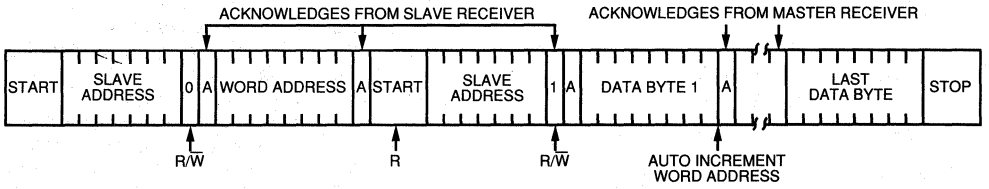
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode the address pointer must be written to.) During this period the 85C72 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will automatically increment from the end of the memory block (128 bytes) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C72s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C72 page is 2 bytes long.

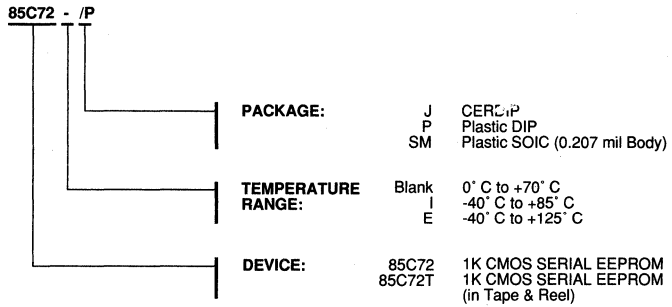
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C72 has only one block (128 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C72

DICE FORM

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

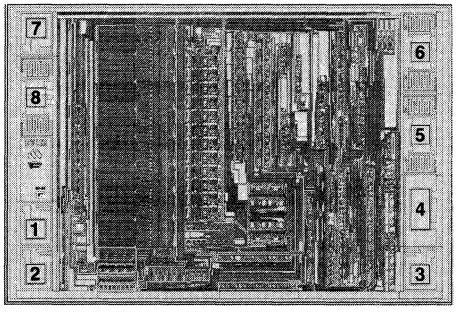
- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1 ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 85C72 is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 85C72s may be connected to the two wire bus. The 85C72 dice are available in wafer or wafflepack.

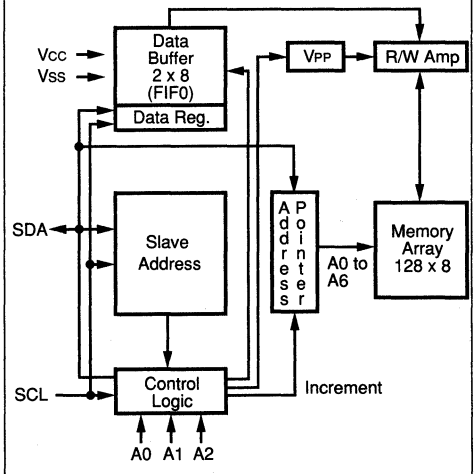
DIE CONFIGURATION

Die Size: 106 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	NF
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NF	No Function
Vcc	+5 V Power Supply

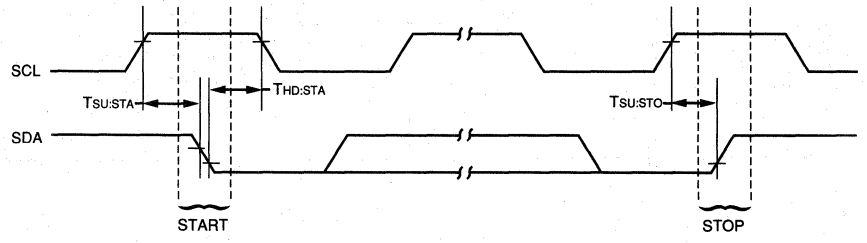
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V,
program cycle	ICCW		7.0	mA	Vcc = 5 V
read cycle	ICCR		750	µA	Vcc = 5 V
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

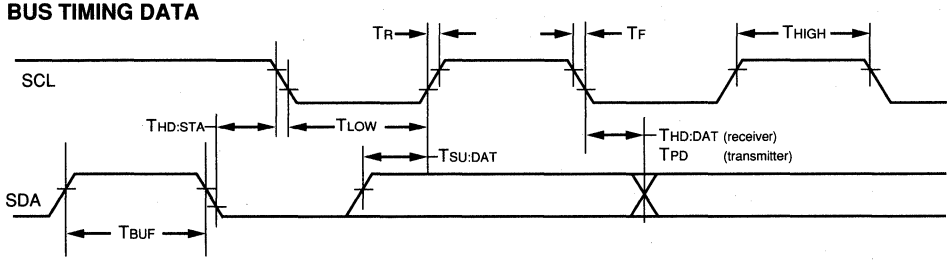


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C72 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C72 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 85C72s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 85C72 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

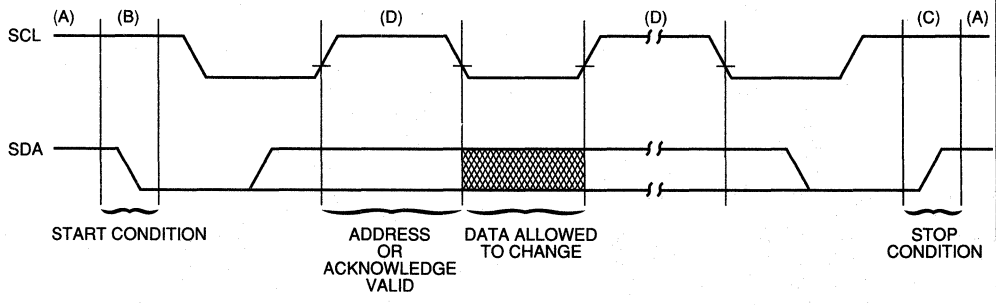
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL



SLAVE ADDRESS

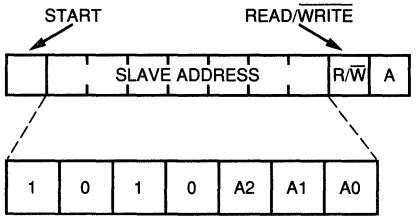
The chip address inputs A0, A1 and A2 of each 85C72 must be externally connected to either Vcc or ground (Vss), assigning to each 85C72 a unique 3-bit address. Up to eight 85C72s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C72.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72. (See Figure 2.)

The 85C72 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 85C72.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72. The most significant bit of the word address is a "Do Not Care" value for the 85C72. After receiving the acknowledge of the 85C72, the master device transmits the data word to be written into the addressed memory location. The 85C72 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72. (See Figure 3.)

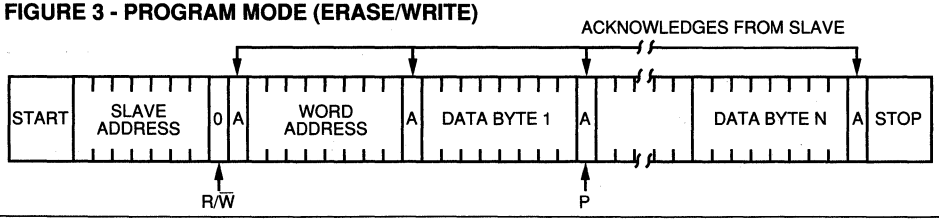
PAGE PROGRAM MODE

To program the 85C72, the master sends addresses and data to the 85C72 which is the slave (see Figure 3). This is done by supplying a start condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One do not care bit and seven address bits) The 85C72 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 2) data bytes will be written in a serial manner.

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

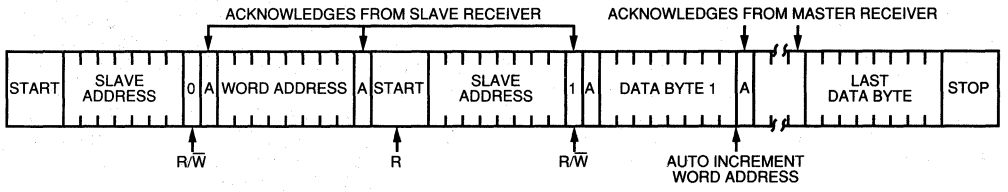
This mode illustrates master device reading data from the 85C72.

As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode the address pointer must be written to.) During this period the 85C72 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another start condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a stop condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C72s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NF No Function

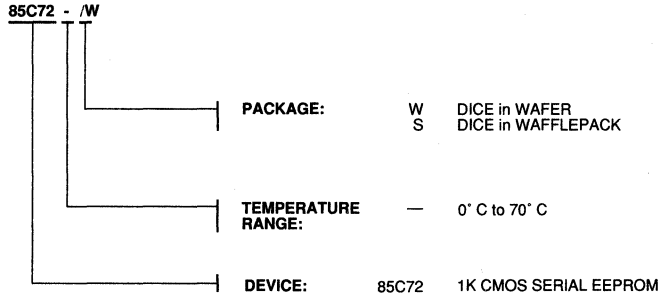
This pad must be connected to Vss for normal operation.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C82

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

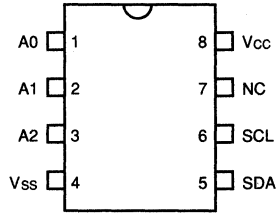
- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

DESCRIPTION

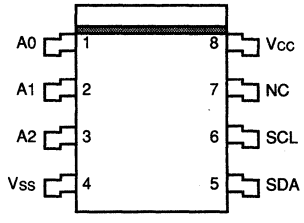
The Microchip Technology Inc. 85C82 is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C82 also has a page-write capability for up to 2 bytes of data. Up to eight 85C82s may be connected to the two wire bus. The 85C82 is available in standard 8-pin DIP and surface mount SOIC package.

PIN CONFIGURATION

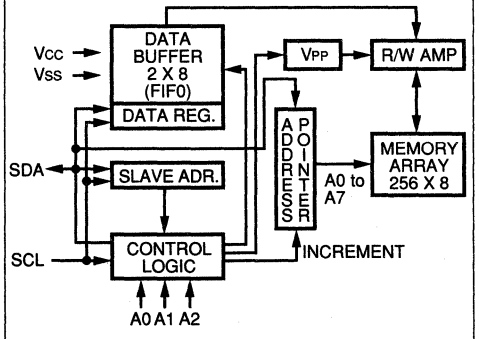
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data Input/Output
SCL	Serial Clock
NC	No Connect
VCC	+5 V Power Supply

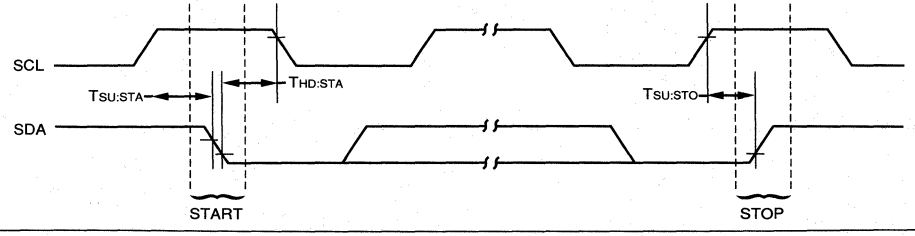
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = (I) and (E)
program cycle	ICCW		7.0	mA	VCC = 5 V, Tamb = 0°C to +70°C
			8.5	mA	VCC = 5 V, Tamb= (I) and (E)
read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V(no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

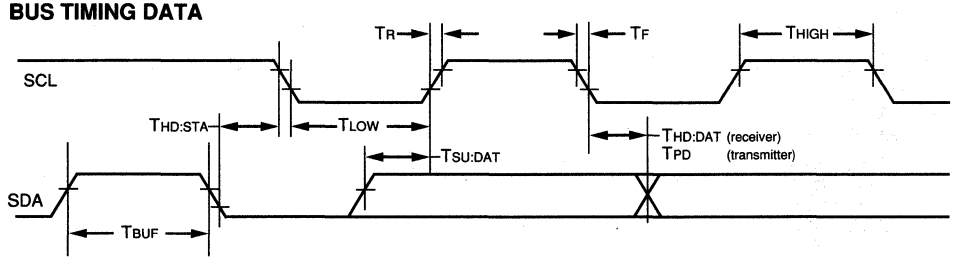


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C82 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C82 works as slave. Both, master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Up to eight 85C82s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C82 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

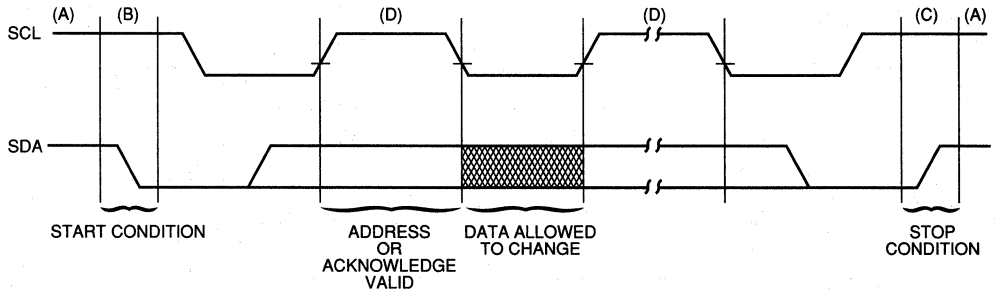
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C82 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

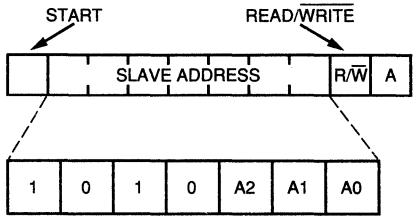
The chip address inputs A0, A1 and A2 of each 85C82 must be externally connected to either Vcc or ground (Vss), assigning to each 85C82 a unique 3-bit address. Up to eight 85C82s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C82.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C82, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C82. (See Figure 2.)

The 85C82 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C82.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C82 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C82. After receiving the acknowledge of the 85C82, the master device transmits the data word to be written into the addressed memory location. The 85C82 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C82. (See Figure 3.)

PAGE PROGRAM MODE

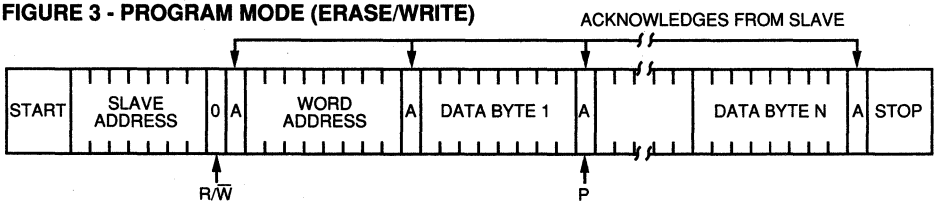
To program the 85C82, the master sends addresses and data to the 85C82 which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C82, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C82 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C82 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C82.

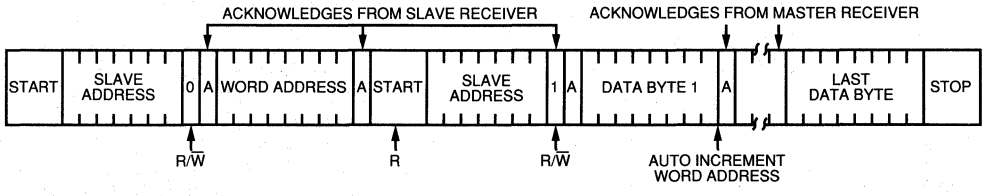
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 85C82 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C82s can be connected to the bus.

These inputs must be connected to either V_{SS} or V_{CC}.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C82 page is 2 bytes long.

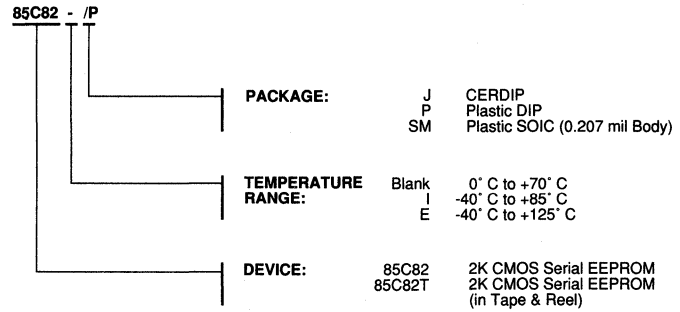
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C82 has only one block (256 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C82

DICE FORM

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

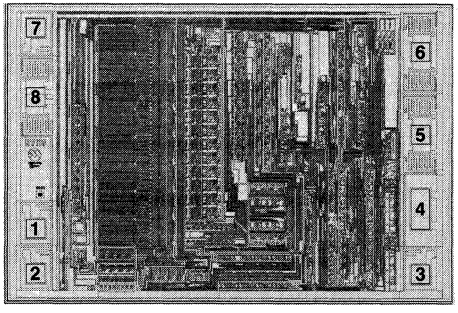
- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 85C82 is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C82 also has a page-write capability for up to 2 bytes of data. Up to eight 85C82s may be connected to the two wire bus. The 85C82 dice are available in wafer or wafflepack.

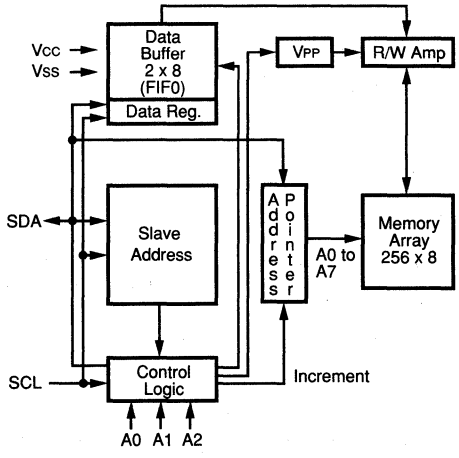
DIE CONFIGURATION

Die Size: 106 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	NF
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0,A1,A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NF	No Function
Vcc	+5 V Power Supply

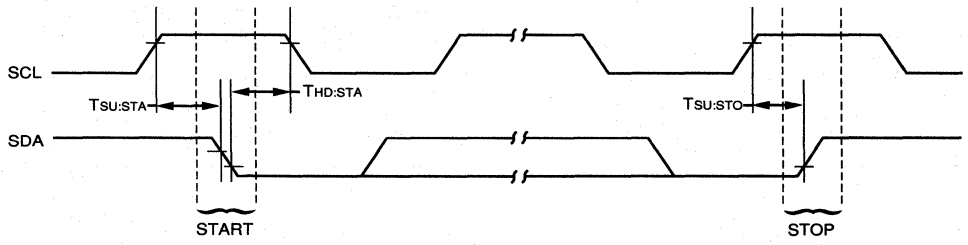
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V,
program cycle	ICCW		7.0	mA	Vcc = 5 V
read cycle	ICCR		750	µA	Vcc = 5 V
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

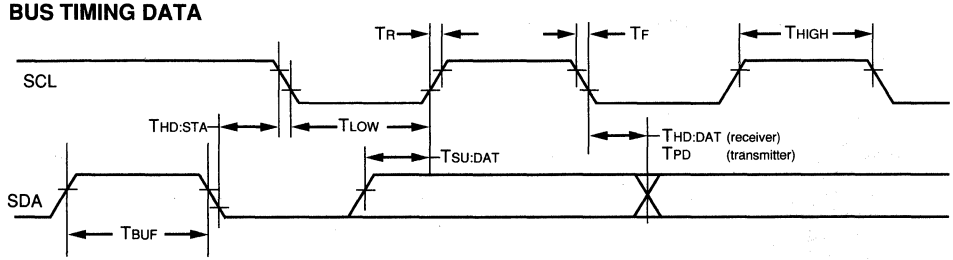


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C82 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C82 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 85C82s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 85C82 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

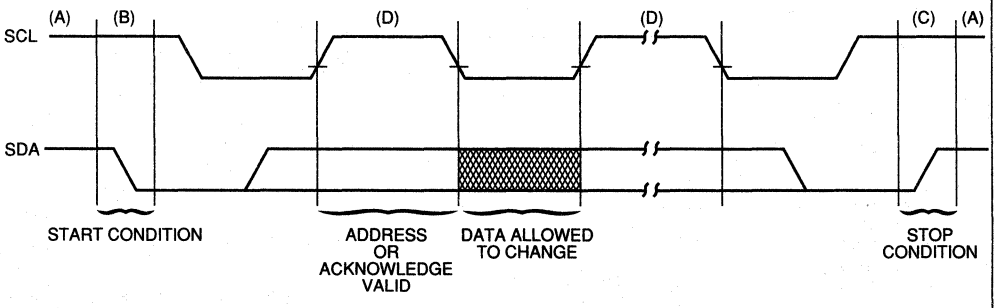
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C82 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS BUS



SLAVE ADDRESS

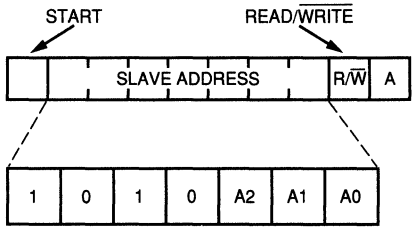
The chip address inputs A0, A1 and A2 of each 85C82 must be externally connected to either Vcc or ground (Vss), assigning to each 85C82 a unique 3-bit address. Up to eight 85C82s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C82.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C82, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C82. (See Figure 2.)

The 85C82 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C82.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C82 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C82. After receiving the acknowledge of the 85C82, the master device transmits the data word to be written into the addressed memory location. The 85C82 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C82. (See Figure 3.)

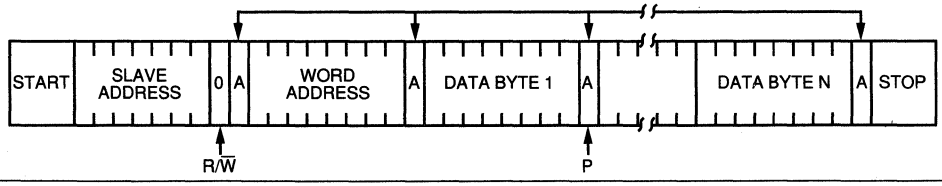
PAGE PROGRAM MODE

To program the 85C82, the master sends addresses and data to the 85C82 which is the slave (see Figure 3). This is done by supplying a start condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C82, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C82 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C82 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 2) data bytes will be

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C82.

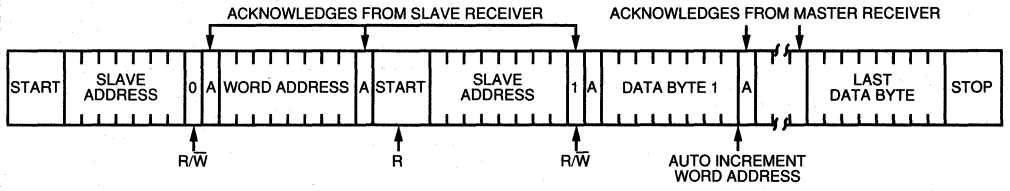
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: although this is a read mode the address pointer must be written to.) During this period the 85C82 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 bytes) back to the first location in that block.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C82s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NF No Function

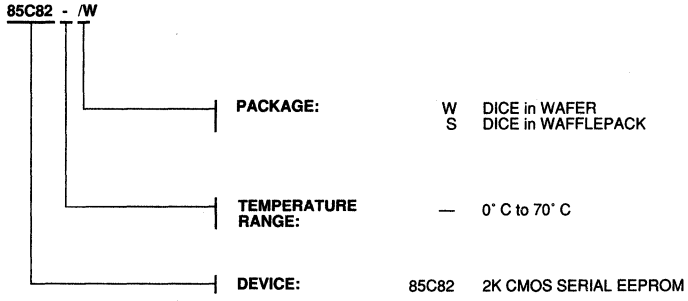
This pad must be connected to Vss for normal operation.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C92

4K (512 x 8) CMOS Serial Electrically Erasable PROM

1

FEATURES

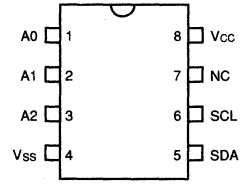
- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

DESCRIPTION

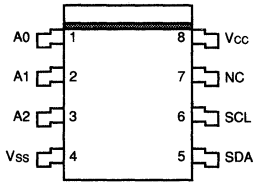
The Microchip Technology Inc. 85C92 is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C92 also has a page-write capability for up to 8 bytes of data. Up to four 85C92s may be connected to the two wire bus. The 85C92 is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

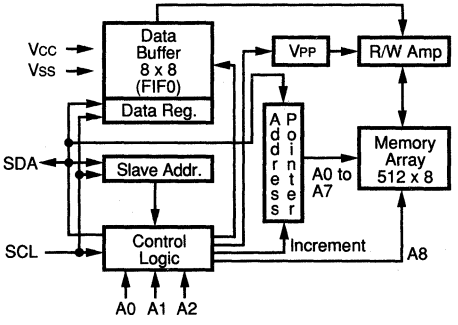
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	No function. Must be connected to VCC or VSS
A1, A2	Chip address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NC	No Connect
VCC	+5 V Power Supply

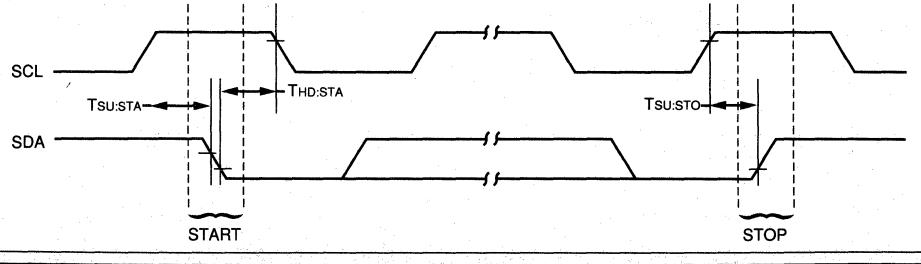
DC CHARACTERISTICS

VCC = + 5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) TAMB = 25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 2 ms, VCC = 5 V, Tamb = (I) and (E)
program cycle	ICCW		7.0	mA	VCC = 5 V, Tamb = 0°C to +70°C
			8.5	mA	VCC = 5 V, Tamb= (I) and (E)
read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

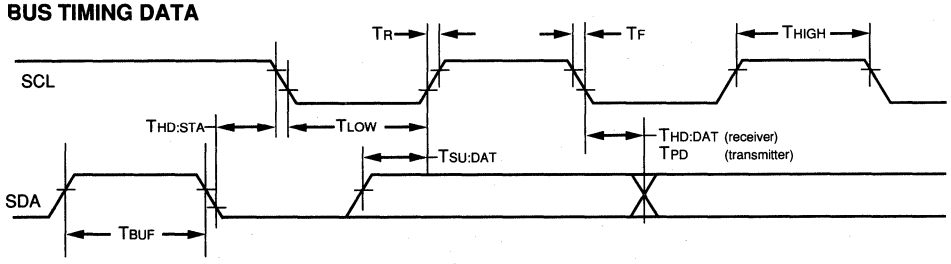


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C92 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 85C92s can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to VCC or VSS. Other devices can be connected to the bus but require different device codes than the 85C92 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

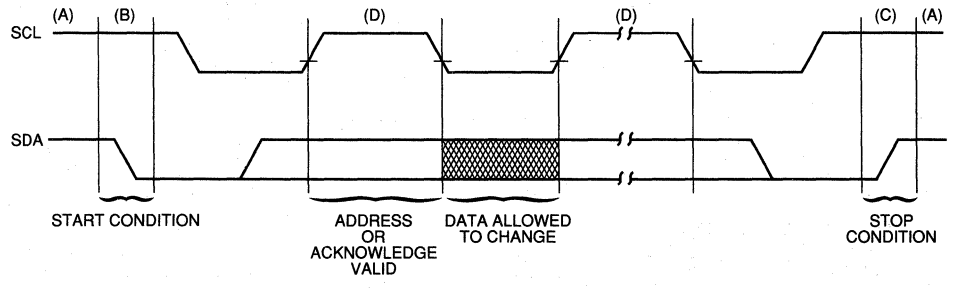
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

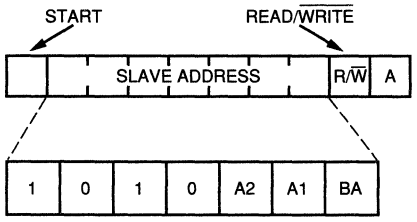
The chip address inputs A1 and A2 of each 85C92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C92 a unique 2-bit address. Up to four 85C92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C92. A0 is not used and must be connected to either Vcc or Vss.

After generating a start condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C92, followed by the chip address bits A1 and A2. The seventh bit of that byte (BA) is used to select the upper block (addresses 100—1FF) or lower page (addresses 000—0FF) of the 85C92.

The eighth bit of slave address determines if the master device wants to read or write to the 85C92. (See Figure 2.)

The 85C92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C92. After receiving the acknowledge of the 85C92, the master device transmits the data word to be written into the addressed memory location. The 85C92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C92. (See Figure 3.)

PAGE PROGRAM MODE

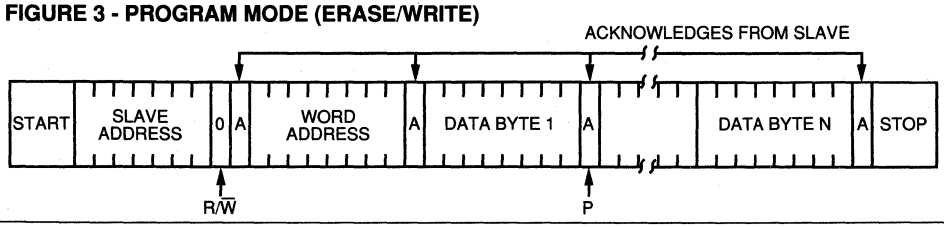
To program the 85C92, the master sends addresses and data to the 85C92 which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The BA bit transmitted with the slave address is the ninth bit of the address pointer.) The 85C92 will generate an acknowledge after every 8 bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 85C92 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 8) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C92.

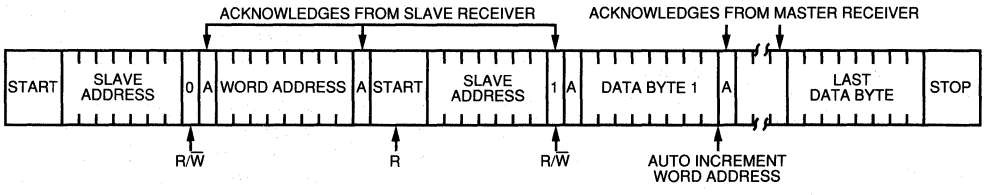
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 85C92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will not increment through a block (256 byte) boundary but will wrap around to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0

This pin must be connected to either Vcc or Vss.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 85C92s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C92 page is 8 bytes long.

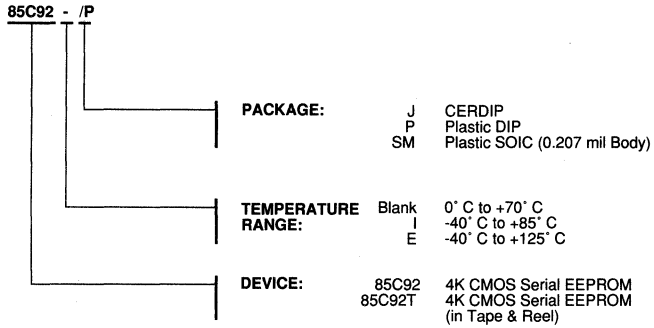
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C92 has two blocks, 256 bytes each.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C92

DICE FORM

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

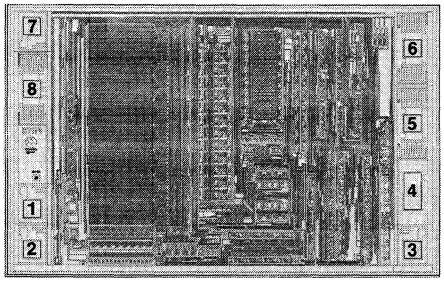
- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- Available in wafer or wafflepack
- Temperature range:
  —Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 85C92 is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C92 also has a page-write capability for up to 8 bytes of data. Up to four 85C92s may be connected to the two wire bus. The 85C92 dice are available in wafer or wafflepack package.

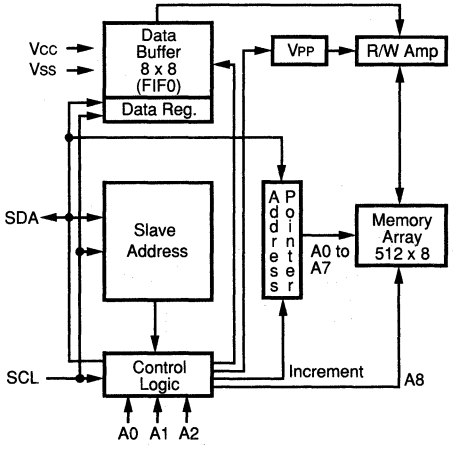
DIE CONFIGURATION

Die Size: 113 x 76 mils



1.	A0	8.	Vcc
2.	A1	7.	NF
3.	A2	6.	SCL
4.	Vss	5.	SDA

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NF	No Function
Vcc	+5 V Power Supply

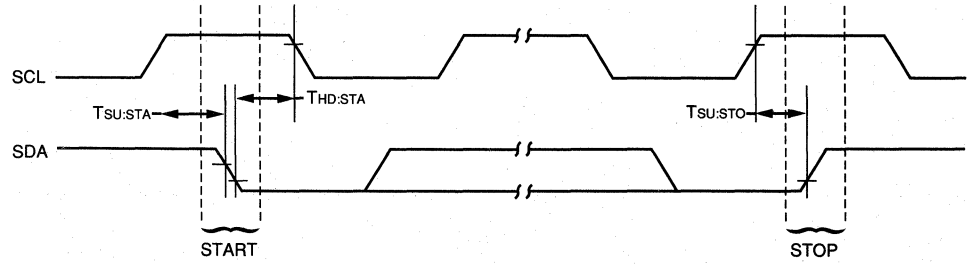
DC CHARACTERISTICS

Vcc = +5V (±10%)
Commercial: Tamb = 0° C to +70° C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 2 ms, Vcc = 5 V,
program cycle	ICCW		7.0	mA	Vcc = 5 V
read cycle	ICCR		750	µA	Vcc = 5 V
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP

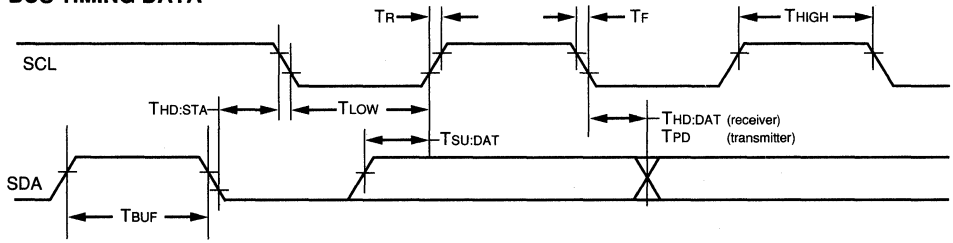


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Noise suppression time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C92 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 85C92s can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to VCC or VSS. Other devices can be connected to the bus but require different device codes than the 85C92 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of the data bytes transferred between the start and stop conditions is determined by the master device and is theoretically unlimited.

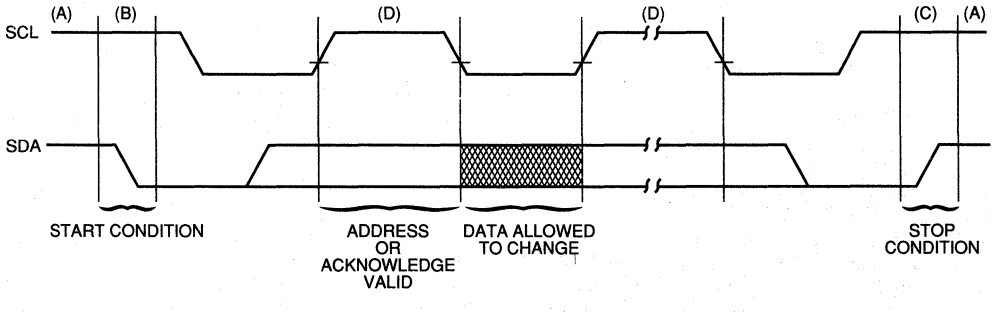
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

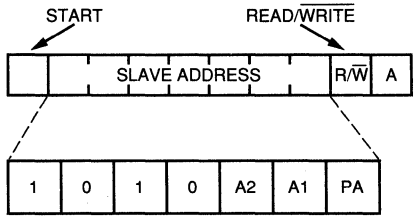
The chip address inputs A1 and A2 of each 85C92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C92 a unique 2-bit address. Up to four 85C92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C92. A0 is not used and must be connected to Vcc or Vss.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C92, followed by the chip address bits A1 and A2. The seventh bit of that byte (PA) is used to select the upper page (addresses 100—1FF) or lower page (addresses 000—0FF) of the 85C92.

The eighth bit of slave address determines if the master device wants to read or write to the 85C92. (See Figure 2.)

The 85C92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C92. After receiving the acknowledge of the 85C92, the master device transmits the data word to be written into the addressed memory location. The 85C92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C92. (See Figure 3.)

PAGE PROGRAM MODE

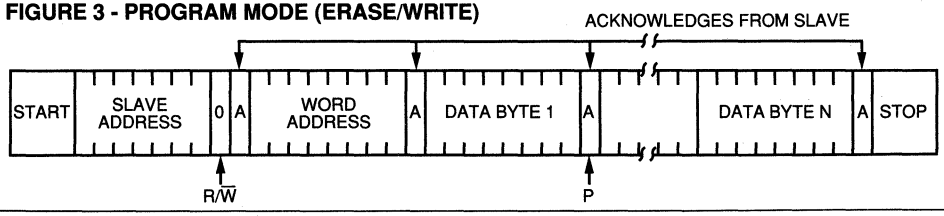
To program the 85C92, the master sends addresses and data to the 85C92 which is the slave (see Figure 3). This is done by supplying a start condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The PA bit transmitted with the slave address is the ninth bit of the address pointer.) The 85C92 will generate an acknowledge after every 8 bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 85C92 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 8) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C92.

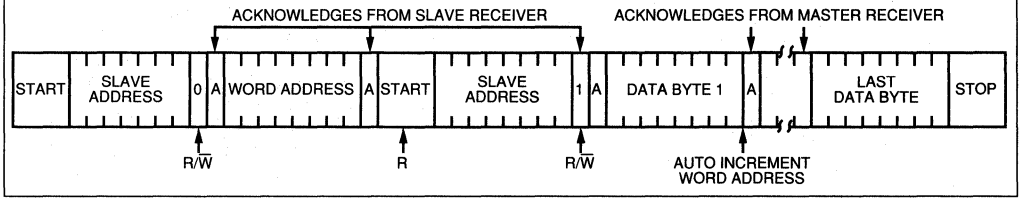
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: although this is a read mode the address pointer must be written to.) During this period the 85C92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pad, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will never automatically increment through a block (256 byte) boundary but will rotate back to the first location in that block.

FIGURE 4 - READ MODE



PAD DESCRIPTION

A0

This pad must be connected to either VCC or VSS.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 85C92s can be connected to the bus.

These inputs must be connected to either VCC or VSS.

SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NF No Function

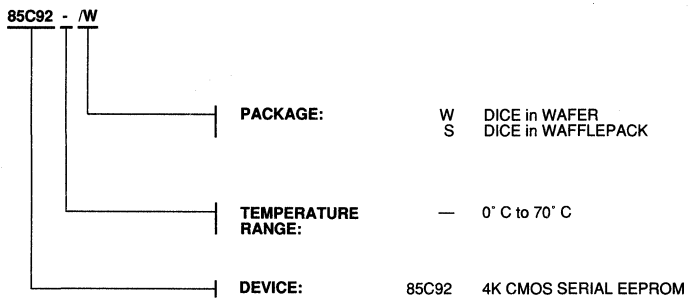
This pad must be connected to Vss for normal operation.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C06

256 Bits (16 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

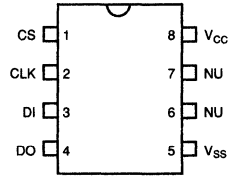
- Low power CMOS technology
- 16 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 100,000 ERASE/WRITE cycles
- Data Retention > 10 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

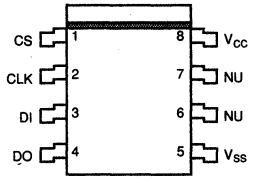
The Microchip Technology Inc. 93C06 is a 256 bit serial Electrically Erasable PROM. The device memory is configured as 16 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C06 is available in the standard 8-pin DIP and a surface mount SOIC package.

PIN CONFIGURATION

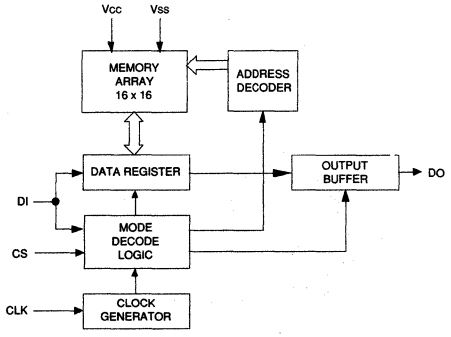
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7.0 V
Storage temperature .....-65°C to +150°C
Ambient temperature with
power applied .....-65°C to +125°C
Soldering termperature of leads (10 seconds)...+300°C
ESD protection on all pins .....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
NU	Not Utilized. No Connection
VCC	+5 V Power Supply

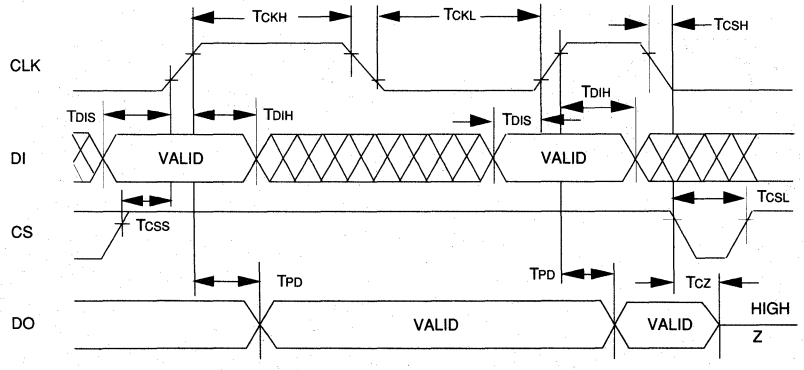
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Automotive: Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, F = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, VCC = 5.5 V
Standby current	ICCS		100	µA	CS = VSS, VCC = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = Low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC		1	ms	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e,. auto ERASE/WRITE) cycle.

After detection of a START condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a Start bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during ERASE and WRITE cycles if the READY/$\overline{\text{BUSY}}$ status information is output by the 93C06.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	0	0	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	0	0	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1	1	0	0	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{\text{BSY}}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The start bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is High, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection and Noise Immunity

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.8 Vand 4.5 V.

During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE, or WRITE instruction can be executed.

READ Mode

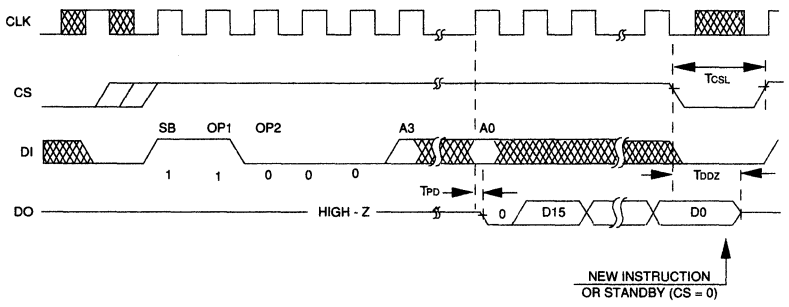
The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a "1".

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).

READ MODE

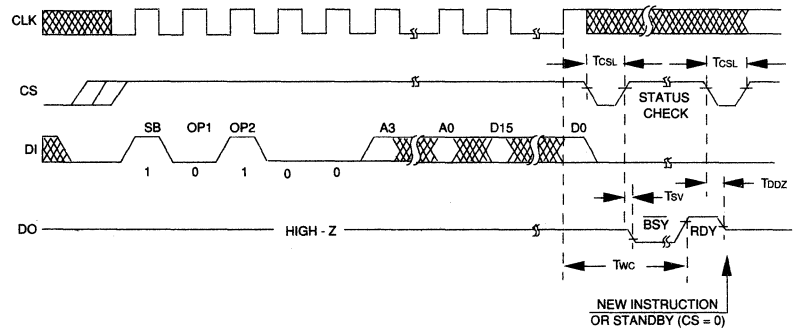


WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 2 ms max.

WRITE MODE

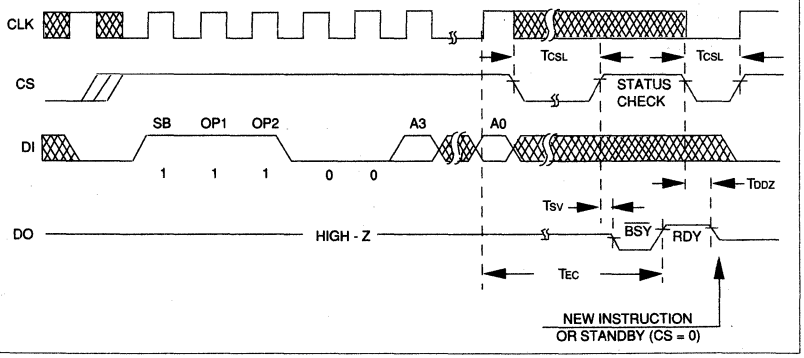


ERASE Mode

The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

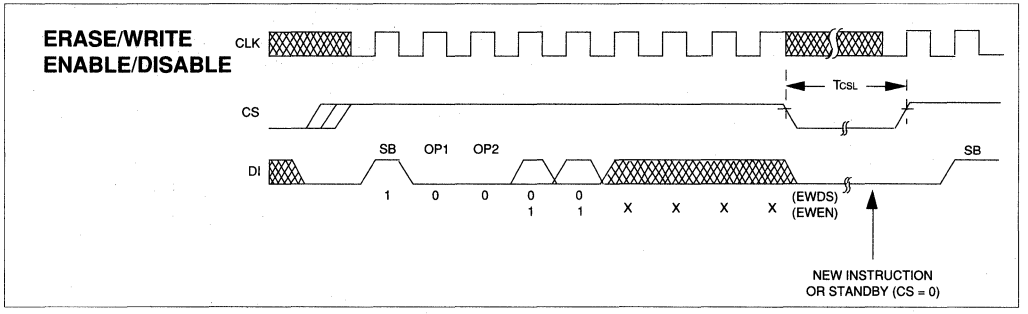
The ERASE cycle takes 1 ms max.

ERASE MODE



ERASE/WRITE Enable/Disable (EWEN, EWDS)

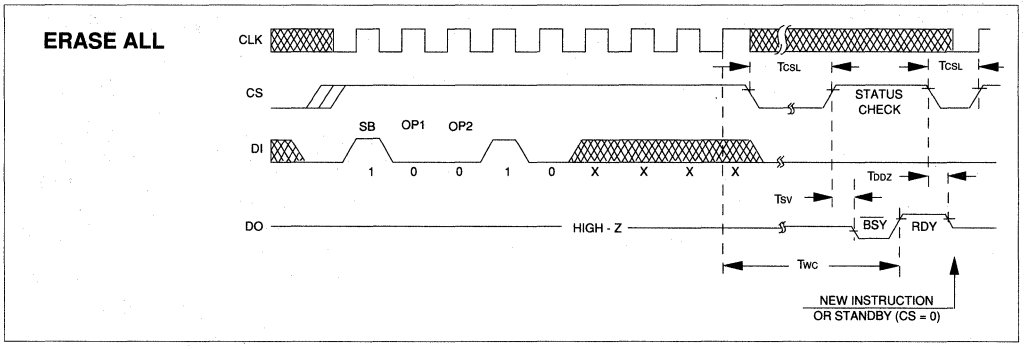
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device.



ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

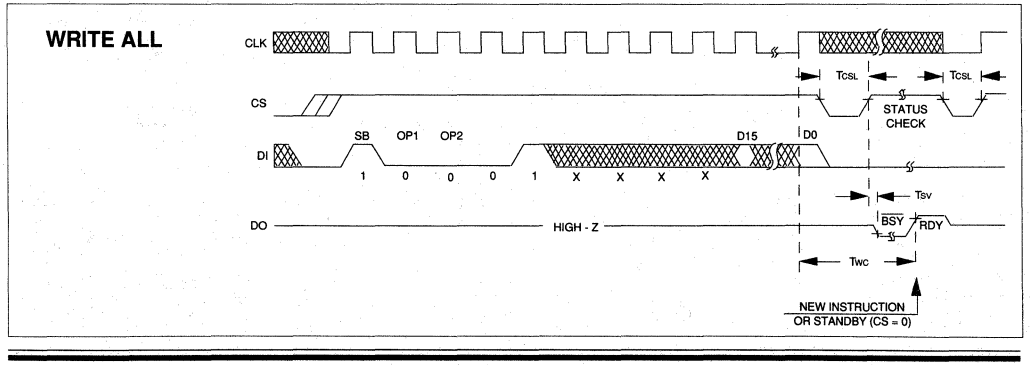


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic erase cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.



NOTES:

SALES AND SUPPORT

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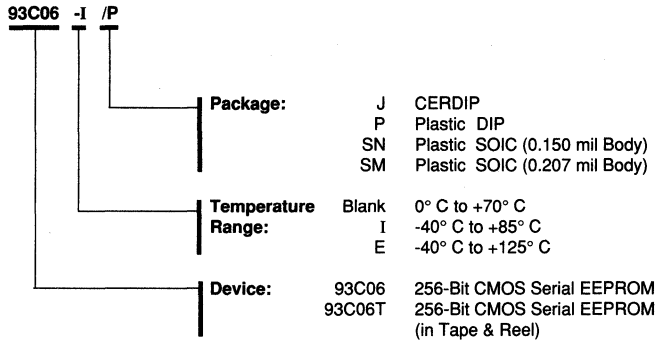
PART NUMBERS



Microchip

93C06

DICE FORM

256 Bits (16 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

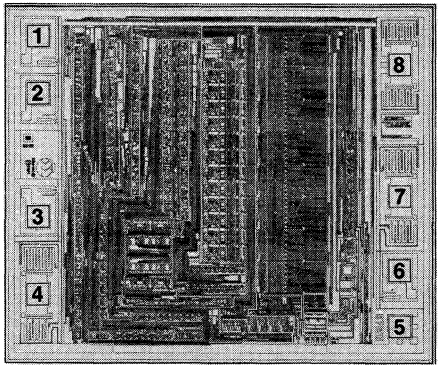
- Low power CMOS technology
- 16 x 16 bit memory organization
- Single 5V only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Available in wafer or waffle pack
- Temperature range:
  — Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 93C06 is a 256 bit serial Electrically Erasable PROM. The device memory is configured as 16 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C06 dice are available in wafer or wafflepack package.

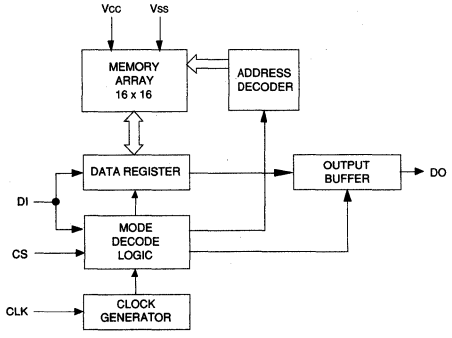
DIE CONFIGURATION

Die Size: 88 x 78 mils.



1. CS	8. Vcc
2. CLK	7. NU
3. DI	6. NU
4. DO	5. Vss

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t VSS ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering termperature of leads
(10 seconds) ..... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
NU	Not Utilized. No Connection
VCC	+5 V Power Supply

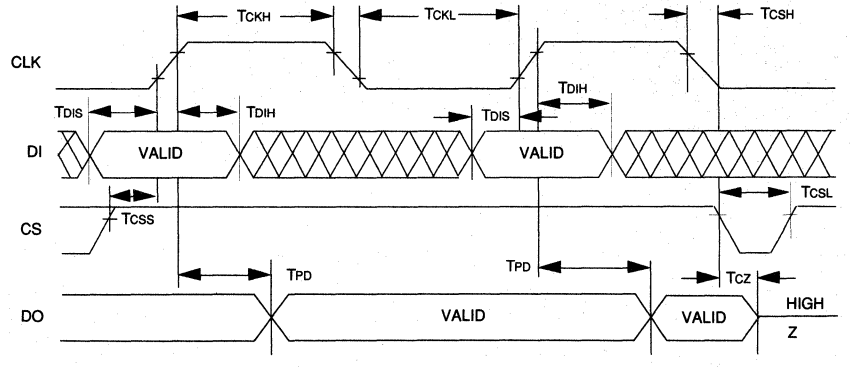
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, F = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, VCC = 5.5 V
Standby current	ICCS		100	µA	CS = 0 V, VCC = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = Low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	 for ERAL and WRAL
Erase cycle time	TEC		1	ms	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e. auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pad also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pad if CS is brought HIGH after being LOW for minimum chip select low time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases, DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during ERASE and WRITE cycles if the READY/BUSY status information is output by the 93C06.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	0	0	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	0	0	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	0	0	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

Start Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pads together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pad.

Data Protection

During power-up, all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 V and 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE, or WRITE instruction can be executed.

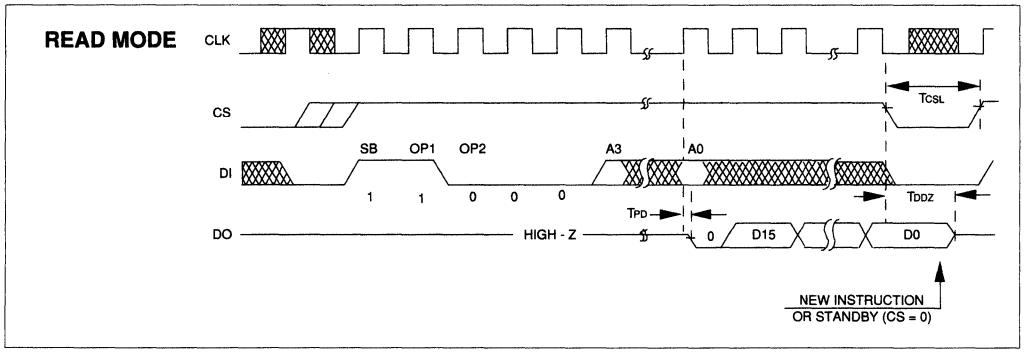
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output T_{PD} after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a "1".

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

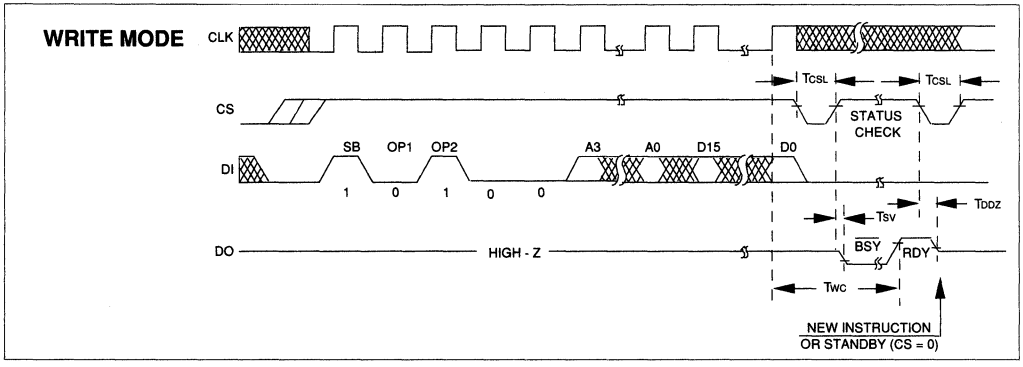
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).



WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the last data bit (D0) has been clocked in.

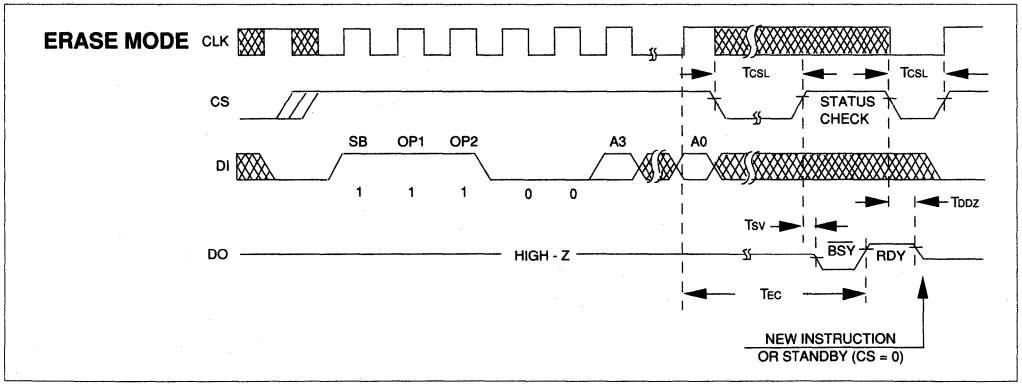
The WRITE cycle takes 2 ms max.



ERASE Mode

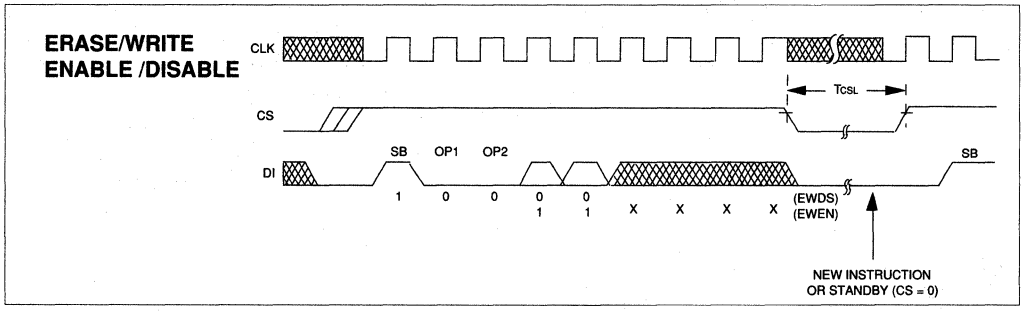
The ERASE instruction forces the data bits of the specified address all to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms max.



ERASE/WRITE Enable/Disable (EWEN, EWDS)

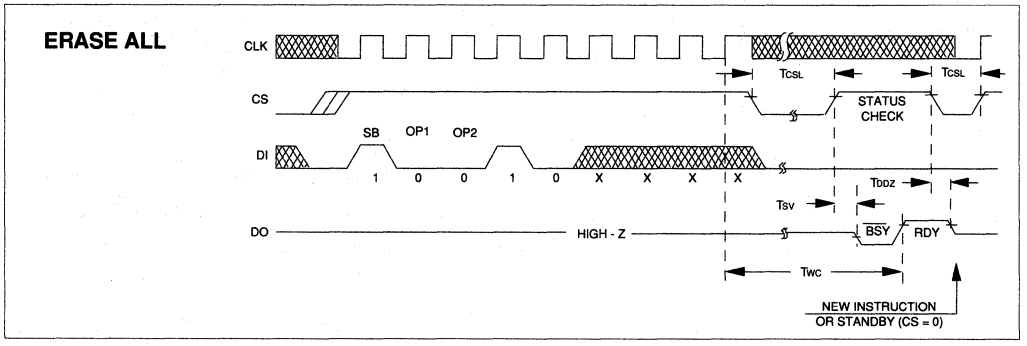
The device is automatically in the ERASE/WWRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device.



ERASE All (ERAL)

The entire chip will erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

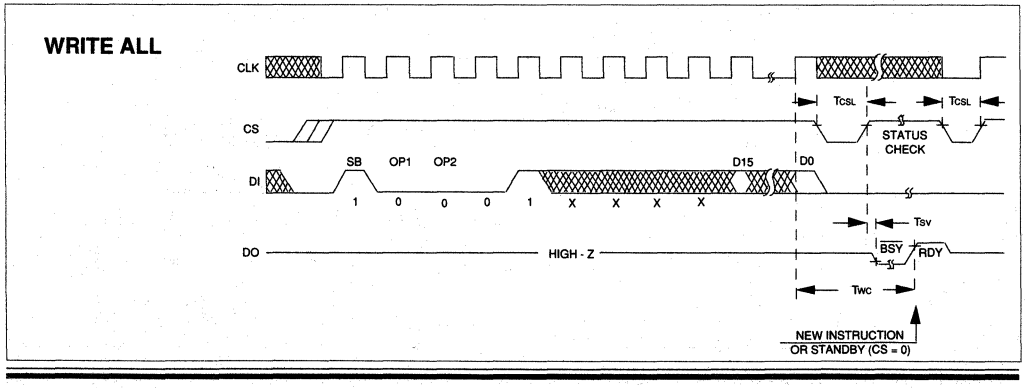


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic erase cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

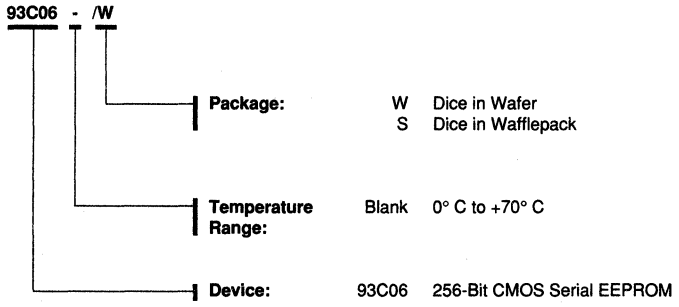


NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C46

1K (64 X 16) CMOS Serial Electrically Erasable PROM

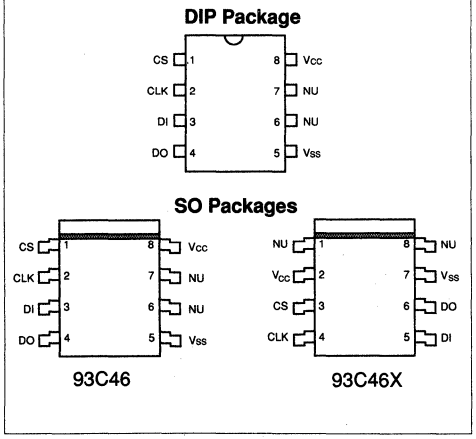
FEATURES

- Low power CMOS technology
- 64 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 100,000 ERASE/WRITE cycles
- Data Retention > 10 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

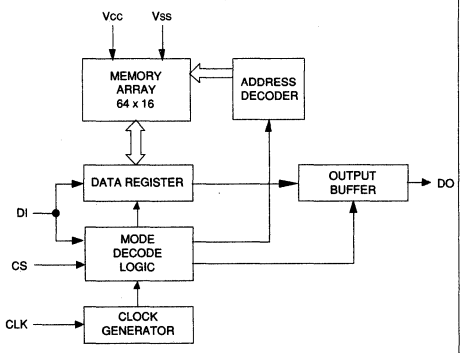
DESCRIPTION

The Microchip Technology Inc. 93C46 is a 1K bit serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C46 is available in the standard 8-pin DIP and a surface mount SOIC package. The 93C46X comes as SOIC only.

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. V_{SS} ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125C
Soldering termperature of leads (10 seconds) ... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
V_{SS}	Ground
NU	Not Utilized. No Connection
V_{CC}	+5 V Power Supply

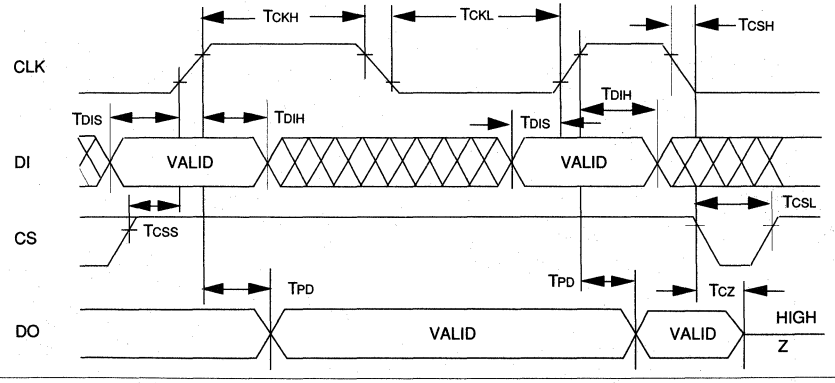
DC CHARACTERISTICS

V_{CC} = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
V_{CC} detector threshold	V_{TH}	2.8	4.5	V	
High level input voltage	V_{IH}	2.0	V_{CC} + 1	V	
Low level input voltage	V_{IL}	-0.3	0.8	V	
High level output voltage	V_{OH}	2.4		V	I_{OH} = -400 µA
Low level output voltage	V_{OL}		0.4	V	I_{OL} = 3.2 mA
Input leakage current	I_{LI}		10	µA	V_{IN} = 0 V to V_{CC} (Note 1)
Output leakage current	I_{LO}		10	µA	V_{OUT} = 0 V to V_{CC} (Note 1)
Internal capacitance (all inputs/outputs)	C_{INT}		7	pF	V_{IN}/V_{OUT} = 0 V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	I_{CC0}		4	mA	F_{CLK} = 1 MHz, V_{CC} = 5.5 V
Standby current	I_{CCS}		100	µA	CS = 0 V, V_{CC} = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC		1	ms	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out o the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but STARTcondition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., autoERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/BUSY status information is outputted by the 93C46.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	A5	A4	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.8 Vand 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

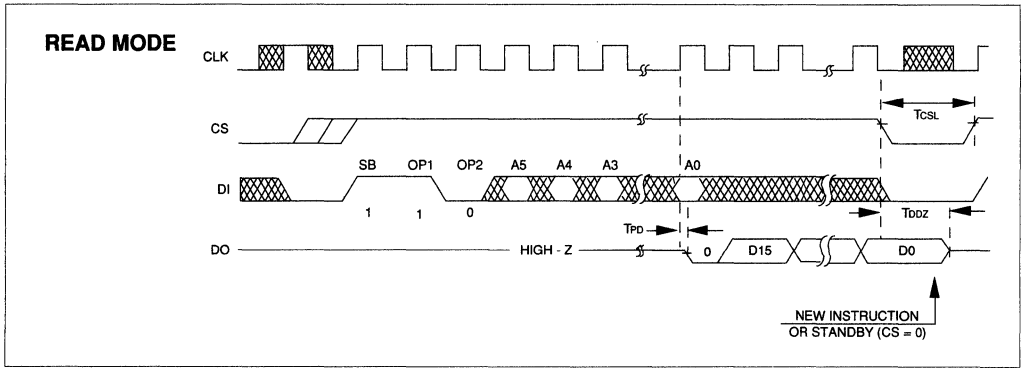
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

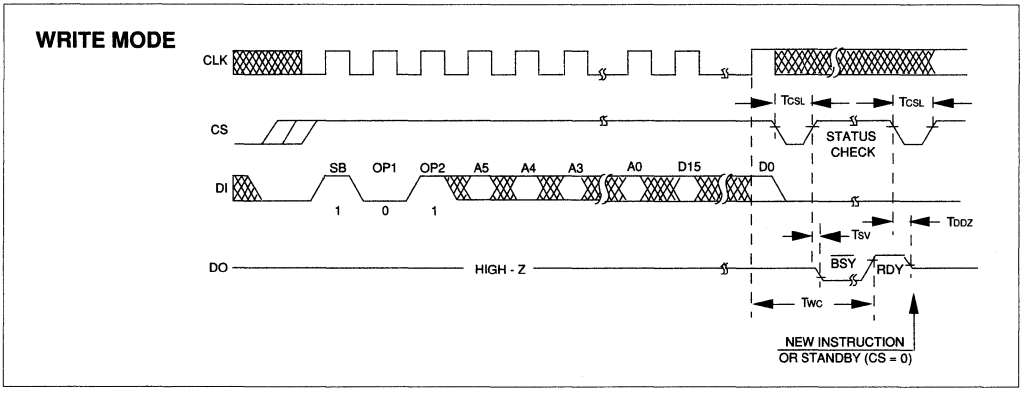
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).



WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

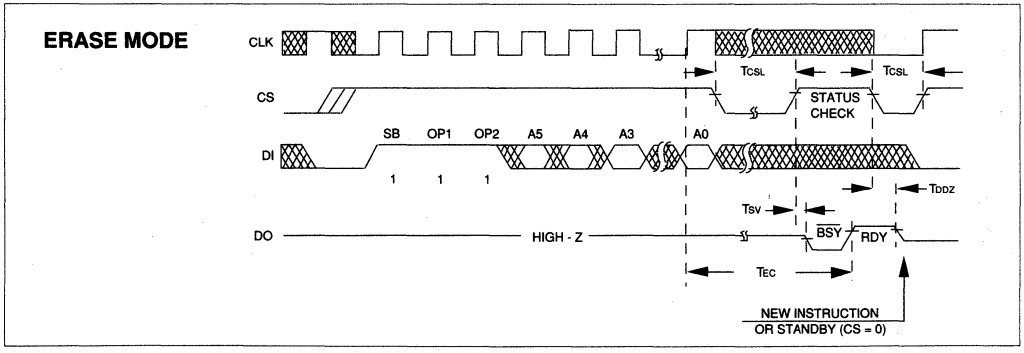
The WRITE cycle takes 2 ms max.



ERASE Mode

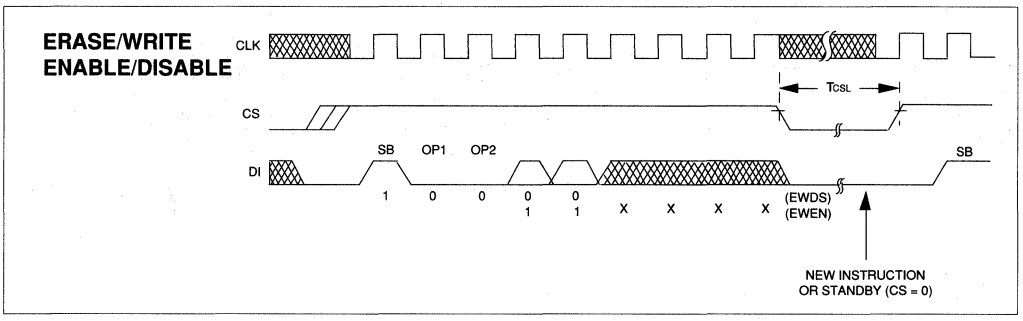
The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms max.



ERASE/WRITE Enable/Disable (EWEN, EWDS)

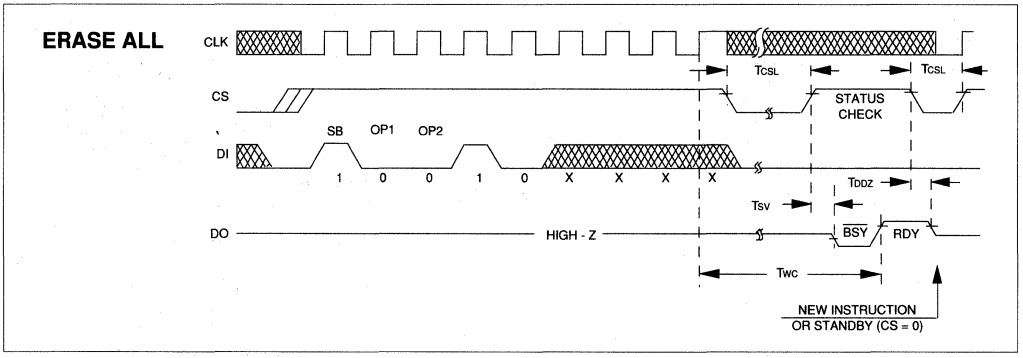
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device.



ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

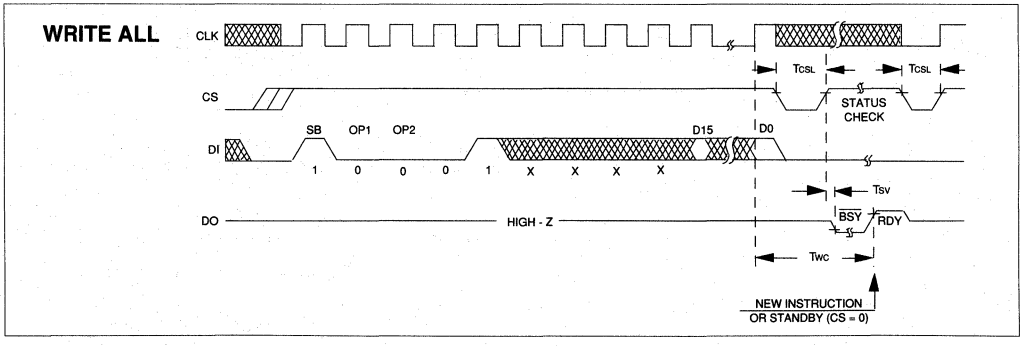


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms max.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

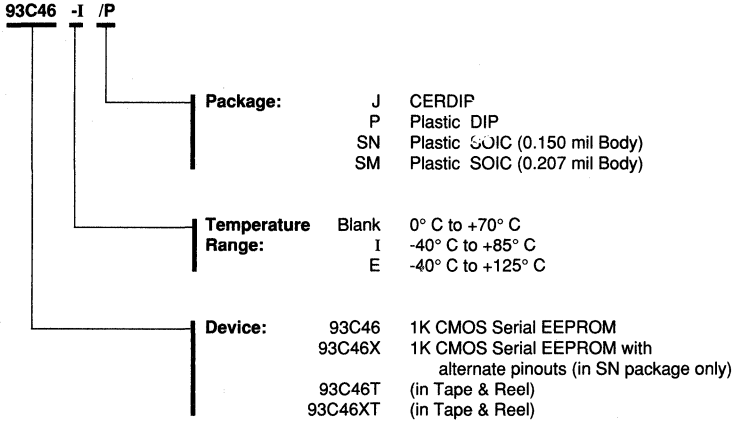


NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C46

DICE FORM

1K (64 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

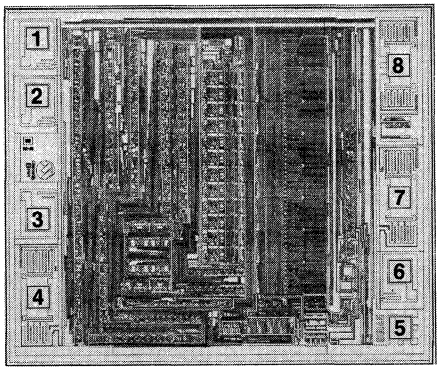
- Low power CMOS technology
- 64 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Available in wafer or waffle pack
- Temperature range:
  — Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 93C46 is a 1K bit serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C46 dice are available in wafer or wafflepack.

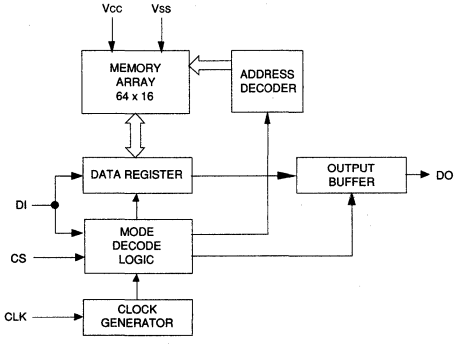
DIE CONFIGURATION

Die Size: 88 x 78 mils.



1. CS
2. CLK
3. DI
4. DO
8. Vcc
7. NU
6. NU
5. Vss

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t Vss ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering termperature of leads
(10 seconds) ..... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PAD FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
NU	Not Utilized. No Connection
Vcc	+5 V Power Supply

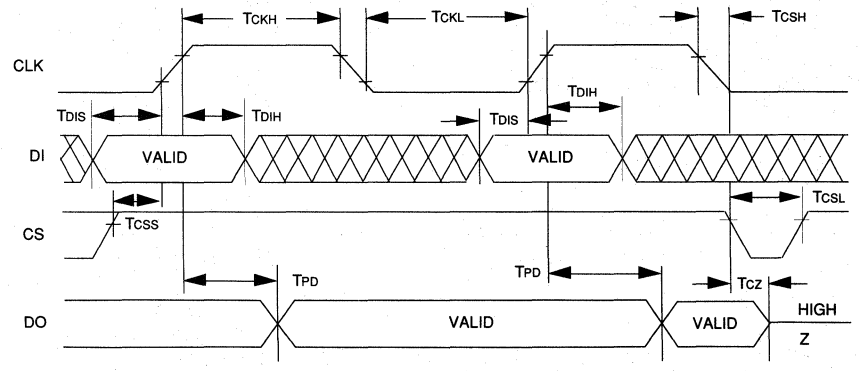
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, F = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, Vcc = 5.5 V
Standby current	ICCS		100	µA	CS = 0 V, Vcc = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = Low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	 for ERAL and WRAL
Erase cycle time	TEC		1	ms	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (TCKH) and Clock Low Time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but STARTcondition has been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pad also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pad if CS is brought high after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in

the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during ERASE and WRITE cycles if the READY/BUSY status information is outputted by the 93C46.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	A5	A4	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a start condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pads together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level.

Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pad.

Data Protection

During power-up, all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 V and 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

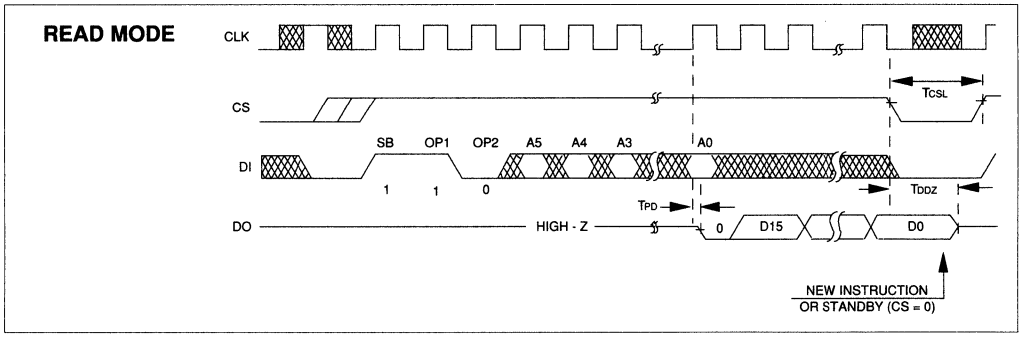
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output T_{PD} after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a "1".

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

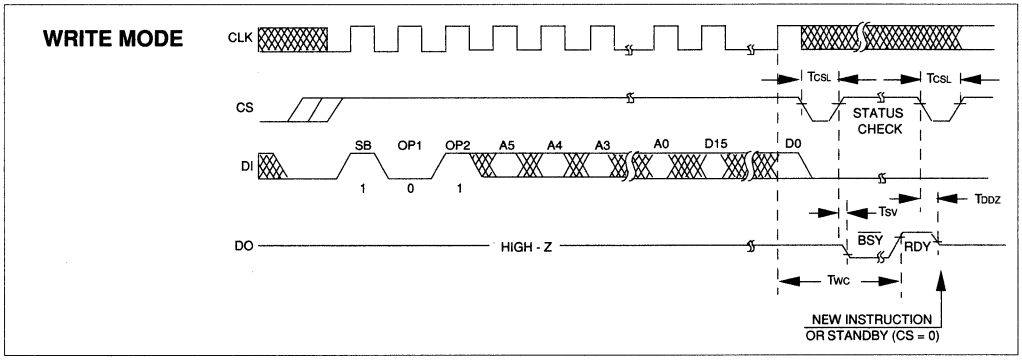
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).



WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the last data bit (D0) has been clocked in.

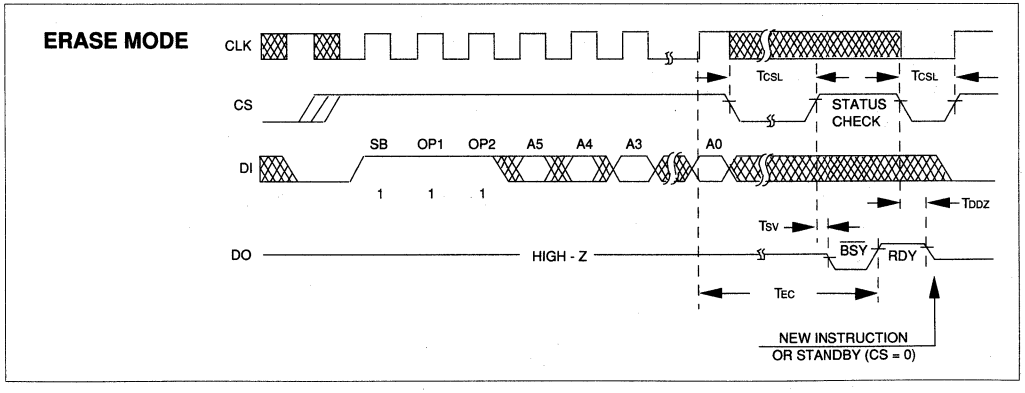
The WRITE cycle takes 2 ms max.



ERASE Mode

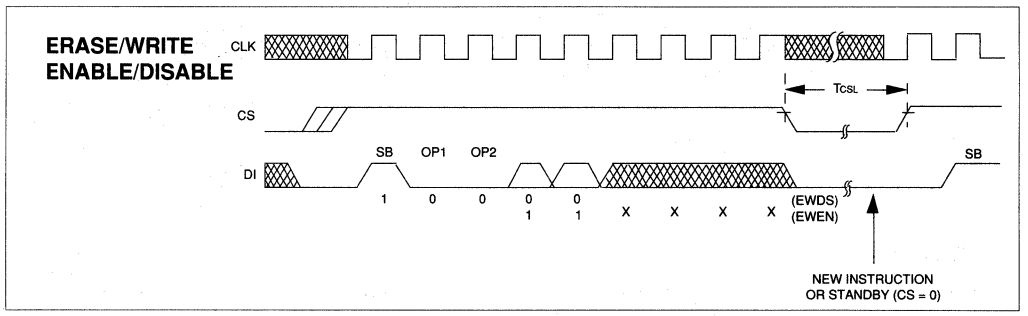
The ERASE instruction forces the data bits of the specified address all to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms max.



ERASE/WRITE Enable/Disable (EWEN, EWDS)

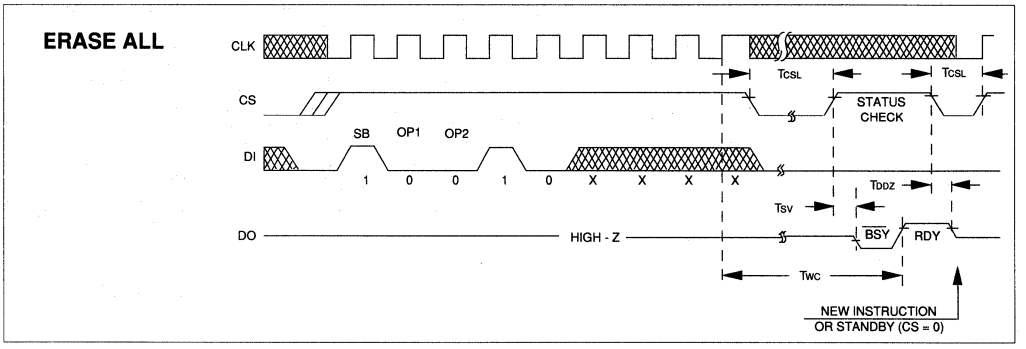
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device.



ERASE All (ERAL)

The entire chip will erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

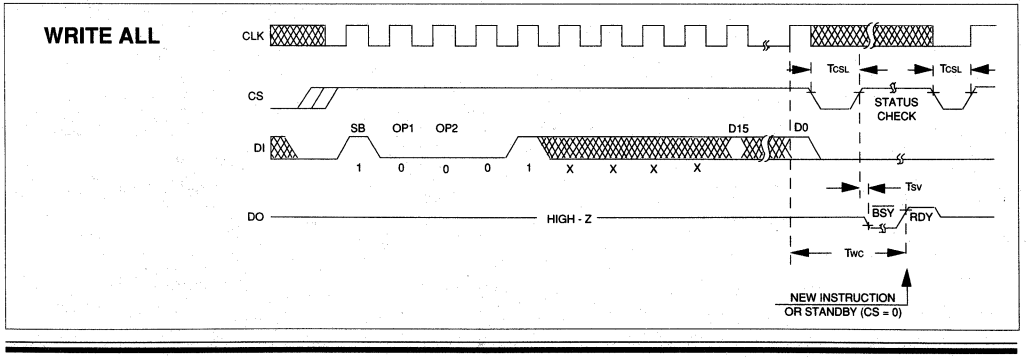


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic erase cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

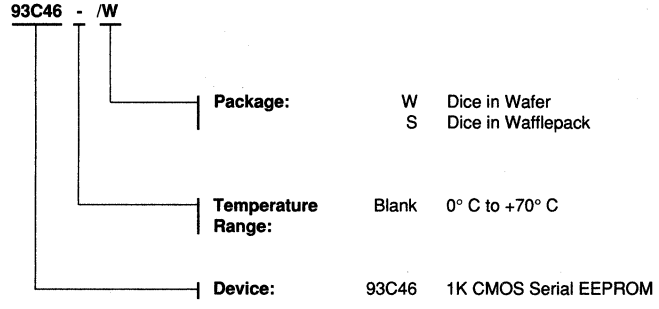


NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



24CXX / 85CXX TO MICROCONTROLLER COMMUNICATION

Two Wire Bus Interface to PIC16C54

Introduction

The Microchip Technology Inc.'s 24Cxx and 85Cxx serial EEPROMs feature a two wire serial interface bus. The bus protocol is I2C compatible. Interface to a serial port with I2C bus protocol in a microcontroller is trivial. This application note is intended for design engineers who want to develop their software programs to communicate a microcontroller with a two wire bus serial EEPROM through a general purpose I/O port.

Unlike other 3-wire bus serial E2PROMs, the 24Cxx/85Cxx communicate with any microcontroller only by a serial data I/O line (SDA) and a serial clock (SCL). Chip select is not required. Data transfer may be initiated only when the bus is not busy. During such transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line while the clock line is high are interpreted as a START or STOP condition. A typical transfer format is shown in Figure 1.

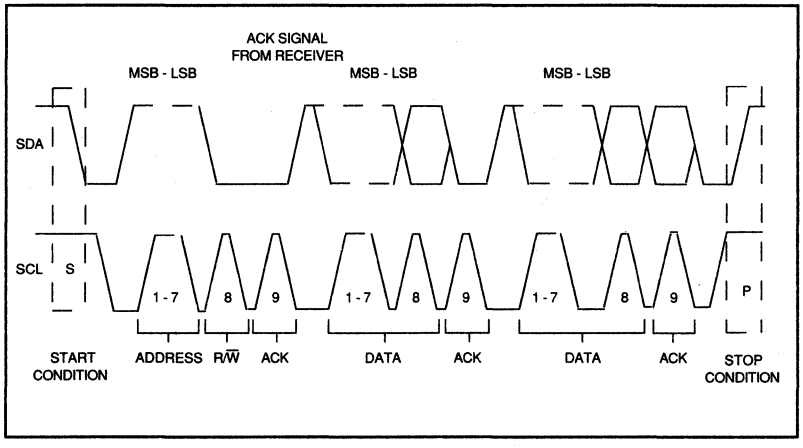


Fig. 1 Transfer Format

After the START condition, a slave address is sent. This address is 7-bits long, the eighth bit is a data direction bit (R/$\overline{W}$) - a logical '0' indicates a transmission WRITE, a logical '1' represents a request for data READ. A data transfer is always terminated by a STOP condition generated by the master controller. However, if a master still wishes to communicate on the bus, it can generate another START condition, and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such transfer.

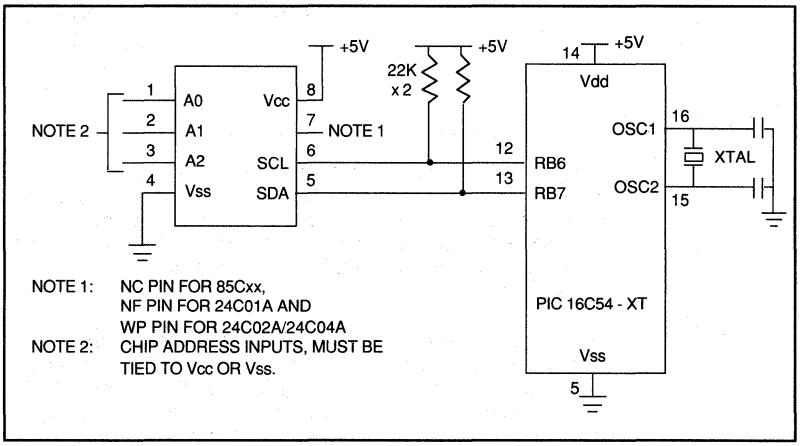


Fig. 2 A Simple Hardware Connection

An example program has been provided in Appendix A containing all PIC16C54 routines needed to exercise a 24Cxx or 85Cxx device. A simple hardware connection is illustrated in Figure 2. A maximum of 8 24C01A/24C02A/85C72/85C82s or 4 24C04A/85C92s can be addressed by a microcontroller on the same two wire bus without additional interfaces. Each device is identified by its Chip Address and will only respond to a correct slave address of a serial communication. A detailed bus flow is shown in Figure 3.

Figure 3 as shown below describes how the bit stream is set up for READ and WRITE mode in the microcomputer programming software prior to sending it on the two wire serial bus.

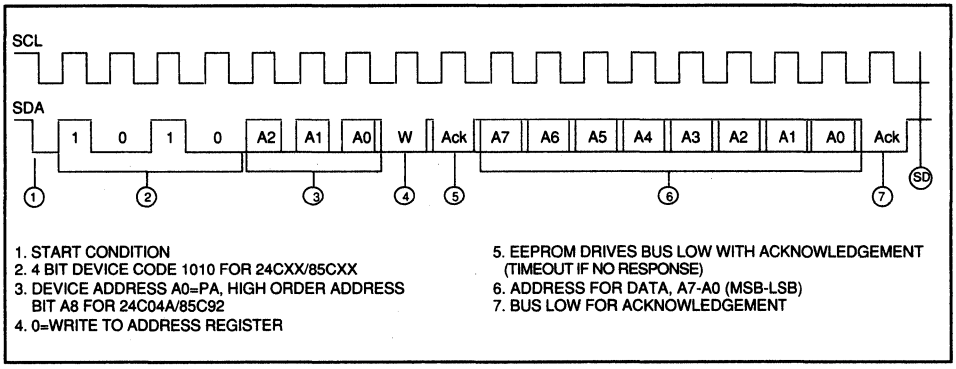


Fig. 3A Setting The Internal Word Address Of The 24Cxx/85Cxx

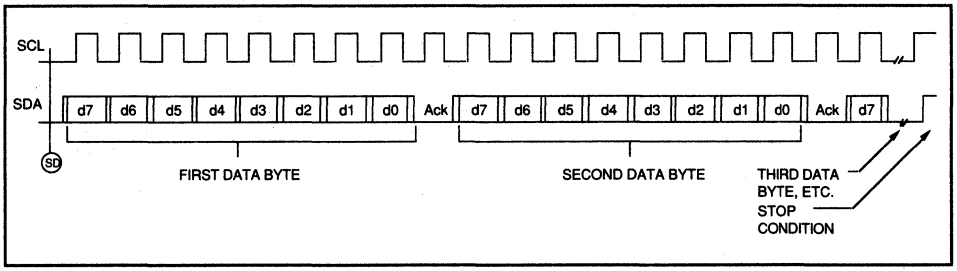


Fig. 3B Byte Write Sequence

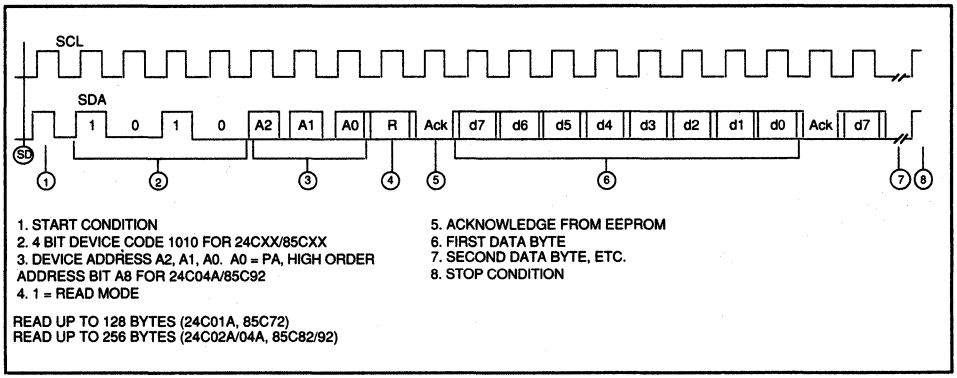


Fig. 3C Read Mode Sequence

The stop condition after write starts the internal self-timed write cycle which may last up to 6 milliseconds (.7 ms per byte). Acknowledge signal should be monitored during this period.

Appendix A:

```
PICALC CROSS ASSEMBLER   2.00   d:\seeprom\appnotes\i2cbus.asm
Apr 11 15:36:02 1990  PAGE 1

TWO WIRE/I2C BUS INTERFACE WITH PIC16C5x

0001            TITLE "TWO WIRE/I2C BUS INTERFACE WITH PIC16C5x"
0002      ;
0003            LIST    P=16C54
0004      ;
0005      ;*****************************************************
0006      ;**  Two wire/I2C Bus READ/WRITE Sample Routines
                ;   of Microchip's 24Cxx/85Cxx serial CMOS
0007      ;**  EEPROM interfacing to a PIC16C54 8-bit CMOS
0008      ;**  single chip microcomputer
0009      ;**
0010      ;**  Part use = PIC16C54-XT/JW
0011      ;**  Note: 1) All timings are based on a
                ;   reference crystal frequency of 2 MHz which
                ;   is equivalent to an instruction cycle
0012      ;**  time of 2 usec.
0013      ;**  2) Address and literal values are read
                ;      in octal unless otherwise specified.
                ;   3) The following sample program is
                ;      intended to interface a two wire/I2C
                ;      serial EEPROM with a PIC16C54 on a
                ;      stand-alone application only.
                ;      In the case where the two wire bus is
                ;      multiplexing with other circuitry, it is
                ;      recommended to check the 24Cxx/85Cxx in
                ;      standby mode to avoid bus contention.
0014      ;**
0015      ;*****************************************************
0016      ;
0017      ;-----------------------------------------------------
0018      ;   Files Assignment
0019      ;-----------------------------------------------------
0020      ;
0021  0002     PC       EQU     2       ; Program counter
0022  0004     FSR      EQU     4       ; File Select Register
0023  0005     RA       EQU     5       ; Port A use to select
                                         ; device address
0024  0006     RB       EQU     6       ; RB7 = SDA, RB6 = SCL
0025      ;
0026  0010      STATUS  EQU     10      ; Status register
0027  0011     FLAG     EQU     11      ; Common flag bits
                                         ; register
0028  0012     EEPROM   EQU     12      ; Bit buffer
0029  0013     ERCODE   EQU     13      ; Error code (to indicate
                                         ; bus status)
0030  0020     ADDR     EQU     20      ; Address register
0031  0021     DATAI    EQU     21      ; Stored data input
                                         ; register
0032  0022     DATAO    EQU     22      ; Stored data output
                                         ; register
0033  0023     SLAVE    EQU     23      ; Device address
                                               ; (1010xxx0)
0034  0024     TXBUF    EQU     24      ; TX buffer
0035  0025     RXBUF    EQU     25      ; RX buffer
0036  0026     COUNT    EQU     26      ; Bit counter
0037      ;
0038  0030     TIMER0   EQU     30      ; Delay timer0
0039  0031     TIMER1   EQU     31      ; Delay timer1
0040      ;
0041      ;
```



```
0042      ;-------------------------------------------------------
0043      ;                       Bit Assignments
0044      ;-------------------------------------------------------
0045      ;
0046      ;    FLAG Bits
0047      ;
0048  0000  ERROR   EQU     0       ; Error flag
0049      ;
0050      ;    EEPROM Bits
0051      ;
0052  0007  DI      EQU     7       ; EEPROM input
0053  0006  DO      EQU     6       ; EEPROM output
0054      ;
0055      ;    I2C Device Bits
0056      ;
0057  0007  SDA     EQU     7       ; RB7, data in/out
0058  0006  SCL     EQU     6       ; RB6, serial clock
0059      ;
0060      ;    END FILES/BITS EQUATE
0061      ;
0062      ;
0063      ;-------------------------------------------------------
0064      ;    Two wire/I2C - CPU communication error status table
          ;    and subroutine
0065      ;-------------------------------------------------------
0066      ;  input  :  W-reg           = error code
0067      ;  output :  ERCODE          = error code
0068      ;            FLAG(ERROR)     = 1
0069      ;
0070      ;       code      error status mode
0071      ;    -------      ---------------------------------------
0072           ;        1   :    SCL locked low by device (bus is
still                                busy)
0073      ;         2    :  SDA locked low by device (bus is still
                             busy)
0074      ;         3    :  No acknowledge from device (no
                             handshake)
0075      ;         4    :  SDA bus not released for master to
                             generate STOP bit
0076      ;-------------------------------------------------------
0077      ;
0078      ; Subroutine to identify the status of the serial clock
          ; (SCL) and serial data
0079      ; (SDA) condition according to the error status table.
0080      ; Codes generated are useful for bus/device diagnosis.
0081      ;
0082      ERR
0083  0000  3411 BTFSS   FLAG,ERROR       ; Remain as first error
                                          ; encountered
0084  0001  0053 MOVWF   ERCODE           ; Save error code
0085  0002  2411 BSF     FLAG,ERROR       ; Set error flag
0086  0003  4000 RETLW   0
0087      ;
0088      ;-------------------------------------------------------
0089      ;    START bus communication routine
0090      ;-------------------------------------------------------
0091      ;    input    : none
0092      ;    output   : initialize bus communication
0093      ;-------------------------------------------------------
0094      ;
0095      ; Generate START bit (SCL is high while SDA goes from
          ; high to low transition) and check status of the
0096      ; serial clock.
0097      BSTART
0098  0004  6077 MOVLW   B'00111111'      ; Put SCL, SDA line in
                                          ; output state
```

```
0099 0005 0006 TRIS     RB
0100 0006 2706 BSF      RB,SCL          ; Set clock high
0101 0007 6001 MOVLW    1               ; Ready error status
                                        ; code 1
0102 0010 3706 BTFSS    RB,SCL          ; Locked?
0103 0011 4400 CALL     ERR             ; SCL locked low by device
0104 0012 2346      BCF     RB,SDA      ; SDA goes low during SCL
                                        ; high
0105 0013 0000      NOP                 ; Timing adjustment
0106 0014 0000      NOP
0107 0015 0000      NOP
0108 0016 2306      BCF     RB,SCL      ; Start clock train
0109 0017 4000      RETLW   0
0110      ;
0111      ;END SUB
0113      ;
0114      ;-----------------------------------------------------
0115      ;   STOP bus communication routine
0116      ;-----------------------------------------------------
0117      ;   Input     :   None
0118      ;   Output    :   Bus communication, STOP condition
0119      ;-----------------------------------------------------
0120      ;
0121      ; Generate STOP bit (SDA goes from low to high during
          ; SCL high state)
0122      ; and check bus conditions.
0123      ;
0124      BSTOP
0125 0020 2346      BCF     RB,SDA      ; Return SDA to low
0126 0021 0000      NOP
0127 0022 0000      NOP
0128 0023 2706      BSF     RB,SCL      ; Set SCL high
0129 0024 6001      MOVLW   1           ; Ready error code 1
0130 0025 3706      BTFSS   RB,SCL      ; High?
0131 0026 4400      CALL    ERR         ; No, SCL locked low by
                                        ; device
0132 0027 2746      BSF     RB,SDA      ; SDA goes from low to
                                        ; high during SCL high
0133 0030 6004      MOVLW   4           ; Ready error code 4
0134 0031 3746      BTFSS   RB,SDA      ; High?
0135 0032 4400      CALL    ERR         ; No, SDA bus not release
                                        ; for STOP
0136 0033 4000      RETLW   0
0137      ;
0138      ;END SUB
0139      ;
0140      ;-----------------------------------------------------
0141      ;   Serial data send from PIC to serial EEPROM,
          ;   bit-by-bit subroutine
0142      ;-----------------------------------------------------
0143      ;   Input :    None
0144      ;   Output     :   To (DI) of serial EEPROM device
0145      ;-----------------------------------------------------
0146      ;
0147      BITIN
0148 0034 6277      MOVLW   B'10111111' ; Force SDA line as input
0149 0035 0006      TRIS    RB
0150 0036 2746      BSF     RB,SDA      ; Set SDA for input
0151 0037 2352      BCF     EEPROM,DI
0152 0040 2706      BSF     RB,SCL      ; Clock high
0153 0041 6001      MOVLW   1
0154 0042 3306      BTFSC   RB,SCL      ; Skip if SCL  is high
0155 0043 5047      GOTO    BIT1
0156 0044 3411      BTFSS   FLAG,ERROR  ; Remain as first error
                                        ; encountered
0157 0045 0053      MOVWF   ERCODE      ; Save error code
```

```
0158 0046 2411      BSF     FLAG,ERROR    ; Set error flag
0159          BIT1
0160 0047 3346      BTFSC   RB,SDA        ; Read SDA pin
0161 0050 2752      BSF     EEPROM,DI     ; DI = 1
0162 0051 0000      NOP                   ; Delay
0163 0052 2306      BCF     RB,SCL        ; Return SCL to low
0164 0053 4000      RETLW   0
0165
0166      ;END SUB
0168      ;
0169      ;-----------------------------------------------------
0170      ;  Serial data receive from serial EEPROM to PIC,
          ;  bit-by-bit subroutine
0171      ;-----------------------------------------------------
0172      ;  Input :   EEPROM file
0173      ;  Output    :  From (DO) of serial EEPROM device
          ;               to PIC
0174      ;-----------------------------------------------------
0175      ;
0176      BITOUT
0177 0054 6077      MOVLW   B'00111111'   ; Set SDA, SCL as outputs
0178 0055 0006      TRIS    RB
0179 0056 3712      BTFSS   EEPROM,DO
0180 0057 5070      GOTO    BIT0
0181 0060 2746      BSF     RB,SDA        ; Output bit 0
0182 0061 6002      MOVLW   2
0183 0062 3346      BTFSC   RB,SDA        ; Check for error code 2
0184 0063 5074      GOTO    CLK1
0185 0064 3411      BTFSS   FLAG,ERROR    ; Remain as first error
                                          ; encountered
0186 0065 0053      MOVWF   ERCODE        ; Save error code
0187 0066 2411      BSF     FLAG,ERROR    ; Set error flag
0188 0067 5074      GOTO    CLK1          ; SDA locked low by device
0189          ;
0190          BIT0
0191 0070 2346      BCF     RB,SDA        ; Output bit 0
0192 0071 0000      NOP                   ; Delay
0193 0072 0000      NOP
0194 0073 0000      NOP
0195          CLK1
0196 0074 2706      BSF     RB,SCL
0197 0075 6001      MOVLW   1             ; Error code 1
0198 0076 3306      BTFSC   RB,SCL        ; SCL locked low?
0199 0077 5103      GOTO    BIT2          ; No.
0200 0100 3411      BTFSS   FLAG,ERROR    ; Yes.
0201 0101 0053      MOVWF   ERCODE        ; Save error code
0202 0102 2411      BSF     FLAG,ERROR    ; Set error flag
0203          BIT2
0204 0103 0000      NOP
0205 0104 0000      NOP
0206 0105 2306      BCF RB,SCL            ; Return SCL to low
0207 0106 4000      RETLW   0
0208          ;
0209          ;END SUB
0211          ;
0212          ;
0213          ;-----------------------------------------------------
0214          ;     RECEIVE DATA subroutine
0215          ;-----------------------------------------------------
0216          ;     Input   :     None
0217          ;     Output  :     RXBUF = Receive 8-bit data
0218          ;-----------------------------------------------------
0219          ;
0220          RX
0221 0107 6010      MOVLW   .8            ; 8 bits of data
0222 0110 0066      MOVWF   COUNT
```

```
0223 0111 0165      CLRF    RXBUF
0224          ;
0225          RXLP
0226 0112 1565      RLF     RXBUF          ; Shift data to buffer
0227 0113           SKPC
0228 0113 3403  +   BTFSS   3,0
0228 0114 2025      BCF     RXBUF,0        ; carry ---> f(0)
0229 0115           SKPNC
0230 0115 3003  +   BTFSC   3,0
0230 0116 2425      BSF     RXBUF,0
0231 0117 4434      CALL    BITIN
0232 0120 3352      BTFSC   EEPROM,DI
0233 0121 2425      BSF     RXBUF,0        ; Input bit =1
0234 0122 1366      DECFSZ  COUNT          ; 8 bits?
0235 0123 5112      GOTO    RXLP
0236 0124 2712      BSF     EEPROM,DO      ; Set acknowledge bit = 1
0237 0125 4454      CALL    BITOUT         ; to STOP further input
0238 0126 4000      RETLW   0
0239          ;
0240          ;END SUB
0241          ;
0242          ;-------------------------------------------------
0243          ;     TRANSMIT DATA subroutine
0244          ;-------------------------------------------------
0245          ;     Input   :    TXBUF
0246          ;     Output  :    Data X'mitted to EEPROM device
0247          ;-------------------------------------------------
0248          ;
0249          TX
0250 0127 6010      MOVLW   .8
0251 0130 0066      MOVWF   COUNT
0252          ;
0253          TXLP
0254 0131 2312      BCF     EEPROM,DO      ; Shift data bit out.
0255 0132 3364      BTFSC   TXBUF,7        ; If shifted bit=0, data
                                           ; bit = 0
0256 0133 2712      BSF     EEPROM,DO      ; Otherwise data bit = 1
0257 0134 4454      CALL    BITOUT         ; Serial data out
0258 0135 1564      RLF     TXBUF          ; Rotate TXBUF left
0259 0136           SKPC                   ; f(6) ---> f(7)
0260 0136 3403  +   BTFSS   3,0
0260 0137 2024      BCF     TXBUF,0        ; f(7) ---> carry
0261 0140           SKPNC                  ; carry ---> f(0)
0262 0140 3003  +   BTFSC   3,0
0262 0141 2424      BSF     TXBUF,0
0263 0142 1366      DECFSZ  COUNT          ; 8 bits done?
0264 0143 5131      GOTO    TXLP           ; No.
0265 0144 4434      CALL    BITIN          ; Read acknowledge bit
0266 0145 6003      MOVLW   3
0267 0146 3352      BTFSC   EEPROM,DI      ; Check for
                                           ; acknowledgement
0268 0147 4400      CALL    ERR            ; No acknowledge from
                                           ; device
0269 0150 4000      RETLW   0
0270          ;
0271          ;END SUB
0273          ;
0274          ;-------------------------------------------------
0275          ;     BYTE-WRITE, write one byte to EEPROM device
0276          ;-------------------------------------------------
0277          ;     Input   :    DATAO = data to be written
0278          ;                  ADDR = destination address
0279          ;                  SLAVE = device address (1010xxx0)
0280          ;     Output  :    Data written to EEPROM device
0281          ;-------------------------------------------------
0282          ;
```

```
0283 0200            ORG     200          ; The location for BYTE-
                                          ; WRITE routine can be
0284                                      ; assigned anywhere
                                          ; between (377- 777)
                                          ; octal.
0285           WRBYTE
0286 0200 1023       MOVF    SLAVE,W      ; Get SLAVE address
0287 0201 0064       MOVWF   TXBUF        ; to TX buffer
0288 0202 4404       CALL    BSTART       ; Generate START bit
0289 0203 4527       CALL    TX           ; Output SLAVE address
0290 0204 1020       MOVF    ADDR,W       ; Get WORD address
0291 0205 0064       MOVWF   TXBUF        ; into buffer
0292 0206 4527       CALL    TX           ; Output WORD address
0293 0207 1022       MOVF    DATAO,W      ; Move DATA
0294 0210 0064       MOVWF   TXBUF        ; into buffer
0295 0211 4527       CALL    TX           ; Output DATA and detect
                                          ; acknowledgement
0296 0212 4420       CALL    BSTOP        ; Generate STOP bit
0297           ;
0298           ;
0299           ;
0300           ;-------------------------------------------------
0301           ;     BYTE-READ, read one byte from serial EEPROM
               ;     device
0302           ;-------------------------------------------------
0303           ;     Input   :    ADDR  = source address
0304           ;                 SLAVE = device address (1010xxx0)
0305           ;     Output  :   DATAI = data read from serial
                                  EEPROM
0306           ;-------------------------------------------------
0307           ;
0308 0300            ORG     300          ; The location for BYTE-
                                          ; READ routine can be
                                          ; assigned anywhere
0309           ;                          ; between (377-777) octal.
0310           RDBYTE
0311 0300 1023       MOVF    SLAVE,W      ; Move SLAVE address
0312 0301 0064       MOVWF   TXBUF        ; into buffer (R/W = 0)
0313 0302 4404       CALL    BSTART       ; Generate START bit
0314 0303 4527       CALL    TX           ; Output SLAVE address.
                                          ; Check ACK.
0315 0304 1020       MOVF    ADDR,W       ; Get WORD address
0316 0305 0064       MOVWF   TXBUF
0317 0306 4527       CALL    TX           ; Output WORD address.
                                          ; Check ACK.
0318 0307 4404       CALL    BSTART       ; START READ (if only one
                                          ; device
0319 0310 1023       MOVF    SLAVE,W      ; is connected to the I2C
                                          ; bus)
0320 0311 0064       MOVWF   TXBUF
0321 0312 2424       BSF     TXBUF,0      ; Specify READ mode
                                          ; (R/W = 1)
0322 0313 4527       CALL    TX           ; Output SLAVE address
0323 0314 4507       CALL    RX           ; READ in data and
                                          ; acknowledge
0324 0315 4420       CALL    BSTOP        ; Generate STOP bit
0325 0316 1065       MOVF    RXBUF        ; Save data from buffer
0326 0317 0061       MOVWF   DATAI        ; to DATAI file.
0327           ;
0328           ;
0329           ;
0330           END

%ASM-I, No Errors, No Warnings
```

NOTES:

ER59256/93C06 AND NMC9306/NMC93C06 COMPATIBILITY ISSUE

Introduction

The ER59256 and 93C06 are 256 bits (16 x 16) serial EEPROM currently offered by Microchip. ER59256 is fabricated in N-channel SNOS technology and 93C06 in advanced CMOS. There are some uncertainties in the field regarding the compatibility between Microchip's 256 bits serial EEPROM and National. Namely NMC9306 and NMC93C06. This report highlights the differences.

Software Differences

	Microchip ER59256			Microchip 93C06				National NMC9306/NMC93C06			
INSTRUCTION	SB	OPCODE	ADDRESS	DATA	SB	OPCODE	ADDRESS	DATA	SB	OPCODE	ADDRESS	DATA
READ	1	1000	A3A2A1A0	-	1	1000	A3A2A1A0	-	1	10XX	A3A2A1A0	-
WRITE	1	0100	A3A2A1A0	D15 - D0	1	0100	A3A2A1A0	D15 - D0	1	01XX	A3A2A1A0	D15 - D0
ERASE	1	1100	A3A2A1A0	-	1	1100	A3A2A1A0	-	1	11XX	A3A2A1A0	-
EWEN	1	0011	0000	-	1	0011	XXXX	-	1	0011	XXXX	-
EWDS	1	0000	0000	-	1	0000	XXXX	-	1	0000	XXXX	-
ERAL	1	0010	0000	-	1	0010	XXXX	-	1	0010	XXXX	-
WRAL	NOT SPECIFIED				1	0001	XXXX	D15 - D0	1	0001	XXXX	D15 - D0

Note: EWEN ..... Erase/Write Enable
EWDS ..... Erase/Write Disable
ERAL ..... Erase All
WRAL .... Write All

From the instruction sets shown, the address bits on EWEN, EWDS, ERAL and WRAL are "don't care" for 9306/93C06 and all logical 0's for ER59256. The WRAL instruction is not specified for ER59256. The two LSB of the opcode are "0 0" for Microchip's ER59256/93C06 and "don't care" for National's NMC9306/NMC93C06. In order to make software fully compatible to all parts, it is recommended to design program with all logical 0's in place of the "don't care" bits.

Polling is available on the 93C06 and NMC93C06. The soft polling can be done by checking the status signal on the DO line (pin 4). A low busy signal ($\overline{BSY}$) indicates the device is still in the programming mode and a high level (RDY) represents the device is ready to receive new instruction. ER59256 and NMC9306 however, do not provide this feature.

Hardware Differences

	Microchip		National	
PARAMETER	ER59256	93C06	NMC9306	NMC93C06
PIN 6	NC	NC	NC	NC
PIN 7	TEST	NC	NC	NC
CLOCK FREQ	250 KHZ	1 MHZ	250 KHZ	1 MHZ
CLK DUTY CYCLE	25% - 75%	not specified	not specified	not specified
CLK HIGH TIME min.	not specified	500 ns	1 us	250 ns
CLK LOW TIME min.	not specified	500 ns	1 us	250 ns
CS LOW TIME min.	not specified	100 ns	1 us	250 ns
ENDURANCE	10K	100K	40K	40K
ESD RATING	1.0 KV	4.0 KV	2.0 KV	2.0 KV
E/W TIME	10 - 30 ms	2 ms	10 - 30 ms	10 ms
ACTIVE CURRENT	10 mA	4 mA	10 mA	3 mA
STANDBY CURRENT	3 mA	100 uA	3 mA	50 uA

Pin 6 and 7 configuration -

Microchip uses the pin 6 and 7 of ER59256 for factory internal test purposes. Pin 6 is used to monitor the on-chip charge pump which generates the required internal high programming voltage (>20 volts) during the ERASE and WRITE cycles. Any circuitry connects to this pin will force to reduce the data retention of the device or even no programming will take place. Signal on pin 7 can force the device into its internal test modes resulting in overprogramming all memory locations. It is therefore recommended that pin 6 should be left open and pin 7 tied to Vss for normal operation.

Microchip's 93C06 and National's NMC9306/NMC93C06 have their pin 6 and 7 physically not utilized. To make ER59256 compatible, the TEST pin (pin 7) can be left floating but must be kept "clean" (noise-free).

Clock high time, clock low time -

For a clock frequency of 250 kHz, both ER59256 and NMC9306 specify the same electrical parameters:

250 kHz equals 4 us clock cycle time
25% of the clock period (4 us) = 1 us (clock high time)
75% of the clock period (4 us) = 3 us (clock low time = 4 - 3 us =1 us)

For slower clock frequencies, the ER59256 spec would restrict the user regarding clock low and high times:

A clock frequency of	100 k Hz	= 10 us cycle time
would result in clock low	= 75% of 10 us	= 7.5 us
and	clock high = 25% of 10 us	= 2.5 us.

In reality, Microchip's ER59256 can fulfill National's NMC9306 spec regarding SK low and SK high equal to 1 usec over all operating frequencies as 250 kHz is the maximium allowable frequency and is therefore the worst case.

Chip select low time -

All parts require a chip select (CS) input goes low between any two instructions. Programming of the part (ER59256, NMC9306,NMC93C06) begins at the falling edge of the CS. Microchip's 93C06 however, starts self-programming at the rising edge of the last data clocked bit. CS goes low and high with a minimium of chip select low time (Tcsl) during programming can be used for polling purpose as discribed in 2.

NOTES:

24C01A COMPATIBILITY ISSUE AND ITS MOBILITY FOR MEMORY UPGRADE

Introduction

The 24C01 is a 1K (128 x 8) serial EEPROM which is currently offered by Microchip and Xicor. There are several important differences between the two devices which are discussed in this report. This report refers to the Microchip part as the 24C01A and the Xicor part as the X24C01. It is intended to assist in designing a board which is compatible with either device.

Compatibility Issues

There are three major differences between Microchip 24C01A and Xicor X24C01 as detailed in the following paragraphs.

2.1 PAGE MODE DIFFERENCES

The 24C01A was originally designed to work in the same socket as the PCD8572 which has a two-byte page mode. Its page is therefore two bytes deep. The X24C01 has a page mode of four bytes depth.

If more than two bytes are transmitted to the 24C01A during a page programming cycle, the 24C01A will terminate the write cycle.

In many applications where serial EEPROMs are used and speed is not a key issue, the byte write mode can be used without any loss of system performance. If only the byte write mode is used, there is no compatibility problem (other than the slave address software differences discussed in 2.2).

If the page write feature must be used, two different page mode algorithms can be transmitted by the master depending upon whose device is being used. The master will have to first do a polling routine to determine if it is interfacing with a 24C01A or X24C01. This polling technique is discussed in 2.2.

Interestingly, the 24C01A actually updates faster in the page mode even though it has one-half the page depth of the X24C01. This is due to the faster write cycle time of the 24C01A. The two devices are compared below:

	Microchip	*Xicor*
Max byte program time	1 ms	10 ms
Max page program time	2 ms (2 bytes)	10 ms (4 bytes)
Max time to program 4 bytes	4 ms	10 ms
Max time to rewrite device	128 ms	320 ms

2.2 SOFTWARE DIFFERENCES

Microchip's 24C01A is designed to share a 2-wire bus on which it resides with other devices. To support this, the first byte of each command sequence from the master to the 24C01A must be a slave address. The 24C01A monitors the 2-wire bus for its slave address and "wakes-up" from standby mode if the address transmitted matches its address as defined by the voltage level (Vss or Vcc) on pins 1, 2 and 3. X24C01 does not support a multiple device bus and will always "wake-up" if a start condition is detected.

A slave address must be transmitted to the 24C01A at certain points during reading and writing. This slave address is not required by the X24C01. Transmitting a slave address to X24C01 will result in erroneous operation. This problem can be solved by having the master transmit the the proper serial bit pattern to the slave, but first the master has to be ascertained which 24C01 it is communicating with.

The master can do a simple polling routine before beginning serial communication with 24C01A or X24C01 to determine which device it is working with. The proper serial protocol for both devices must be contained in the master controller's firmware. Once the master knows which 24C01 is on the bus, it can execute the proper serial commands.

The polling consists of the pattern like the one shown below:

SDA LINE: | START BIT | 00000001 | ACKNOWLEDGE BIT | DATA 7...0 |

If a X24C01 is used on the 2-wire bus, an acknowledge bit and eight data bits will be returned whereas 24C01A will issue no response and will ignore the command.

2.3 HARDWARE DIFFERENCES

As described earlier, the 24C01A is designed to share a 2-wire bus with other devices while the X24C01 is not. Chip address bits are included in the slave address for the 24C01A, and are incorporated into pins 1, 2 and 3 of the device. They must be connected to Vcc or Vss for proper operation. Since pins 1, 2 and 3 of the Xicor part are NC (no connect) pins and they are not internally connected, they can be tied high or low.

Another hardware difference involves pin 7 which *MUST* be connected to Vss on X24C01. The 24C01A can have pin 7 connected to Vss or Vcc.

If only one device is planned for the 2-wire bus, the board can be made compatible for either device by connecting pins 1, 2 and 3 to either Vss or Vcc and tieing pin 7 to Vss.

Mobility For Memory Upgrade And Expansion

In system applications where the master device needs to address more than one serial EEPROM on a 2-wire bus, Microchip's 24C01A offers the flexibility. Up to eight 24C01As can be connected to the 2-wire bus. More than one Xicor X24C01 connecting to the bus may result in bus contention.

If memory upgrade is required, Microchip's 24C01A can be upgraded to 24C02A (256 x 8) or 24C04A (512 x 8) on the same IC socket with *NO change* in hardware. Using Xicor X24C01 will have to reconfigure both software and hardware to accomodate the changes.

NOTES:

SECTION 2
EEPROM PRODUCT SPECIFICATIONS

Microchip

28C04A

4K (512 x 8) CMOS Electrically Erasable PROM

FEATURES

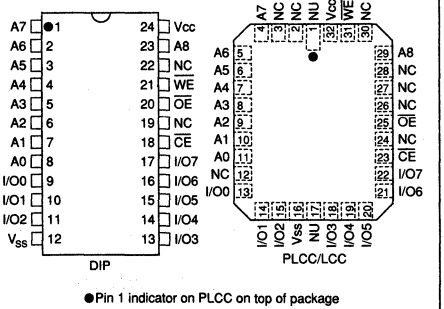
- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  —30mA Active
  —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  —Internal Control Timer
  —Auto-Clear Before Write Operation
  —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  —V_{CC} Detector
  —Pulse Filter
  —Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  —24 Pin Dual-In-Line Package
  —32 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C

DESCRIPTION

The Microchip Technology Inc 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

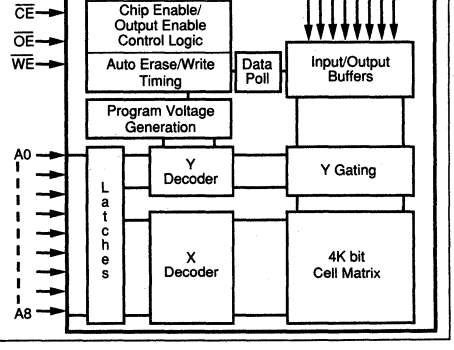
PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V
Output Voltage w.r.t. Vss .....-0.6V to Vcc+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied .....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 85° C) CE = Vcc-0.3 to Vcc+1

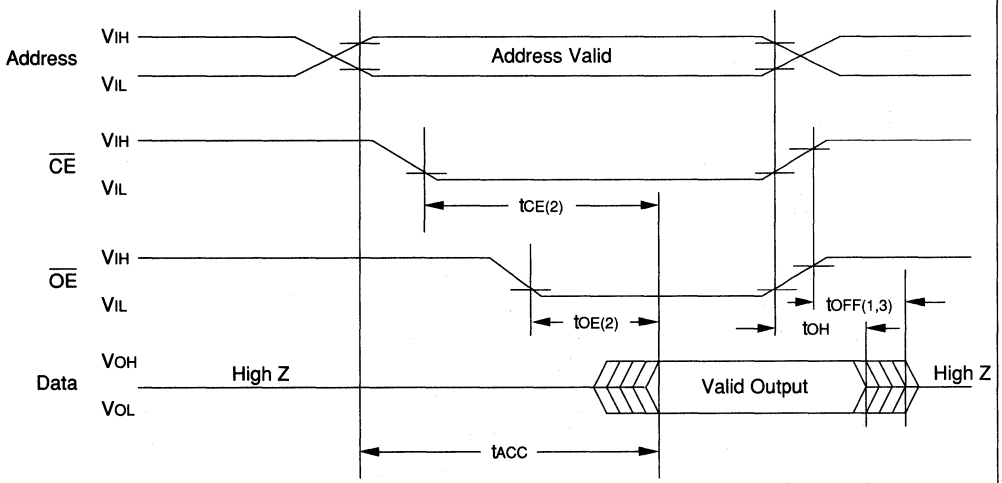
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C04A-15		28C04A-20		28C04A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

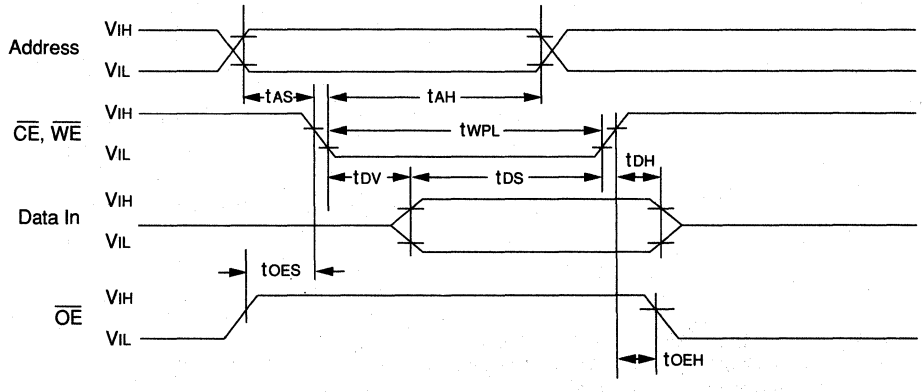
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

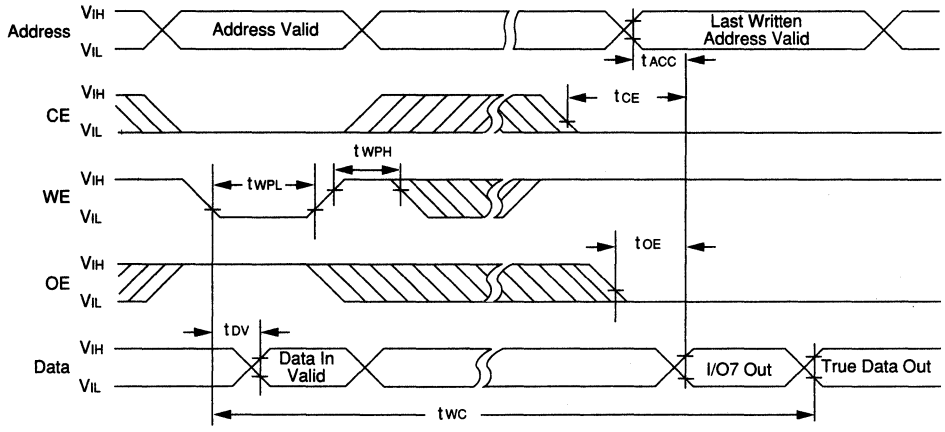
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

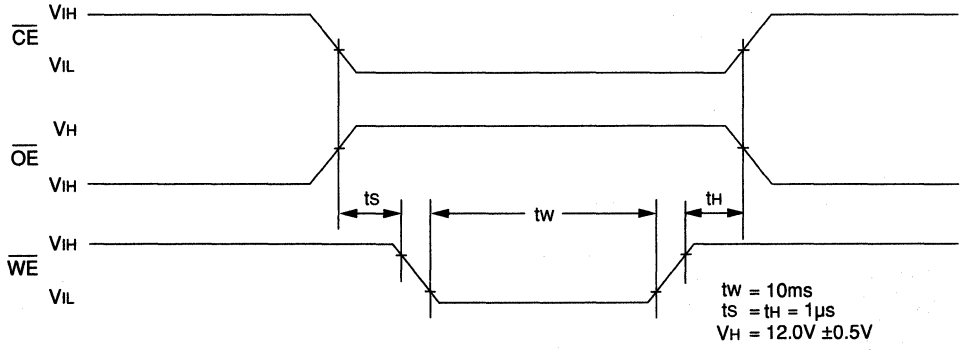
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



DEVICE OPERATION

The Microchip Technology Inc 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

$\overline{\text{Data}}$ Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Optional Chip Clear

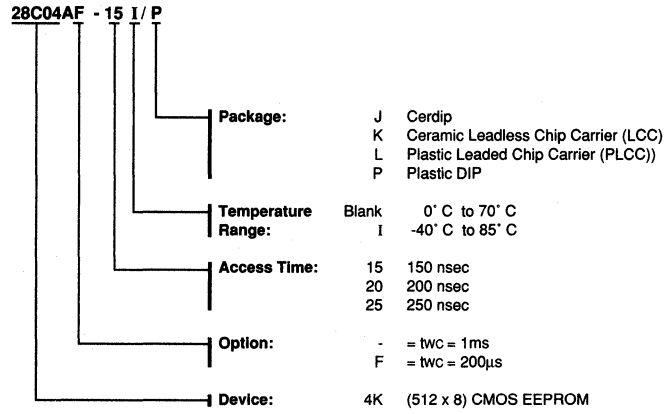
All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

28C16A

16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100μA Standby
- Fast Byte Write Time—200μs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ polling
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - —24 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Military *: -55° C to 125° C

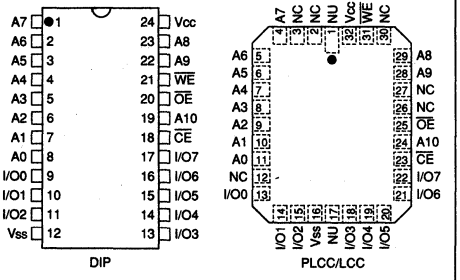
DESCRIPTION

The Microchip Technology Inc 28C16A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

* See military data sheet DS60036.

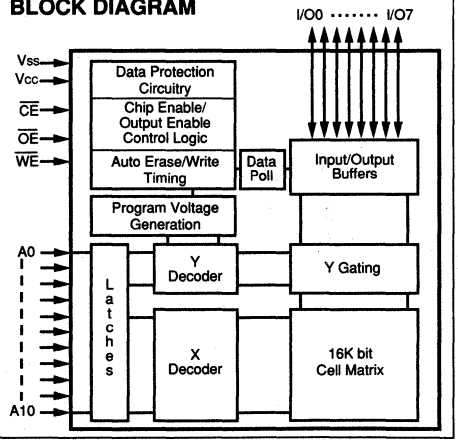
PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V
Voltage on A9 w.r.t. Vss .....-0.6V to +13.5V
Output Voltage w.r.t. Vss .....-0.6V to Vcc+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 85° C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

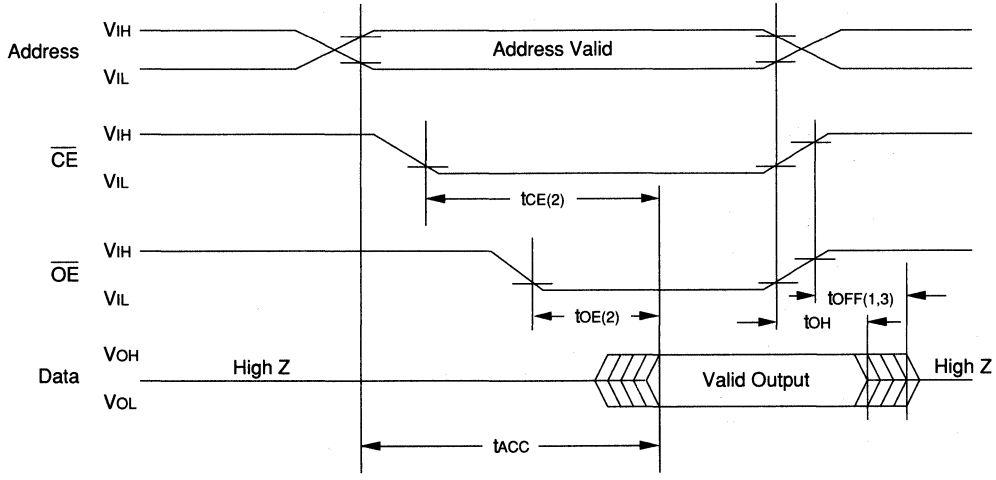
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C16A-15		28C16A-20		28C16A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

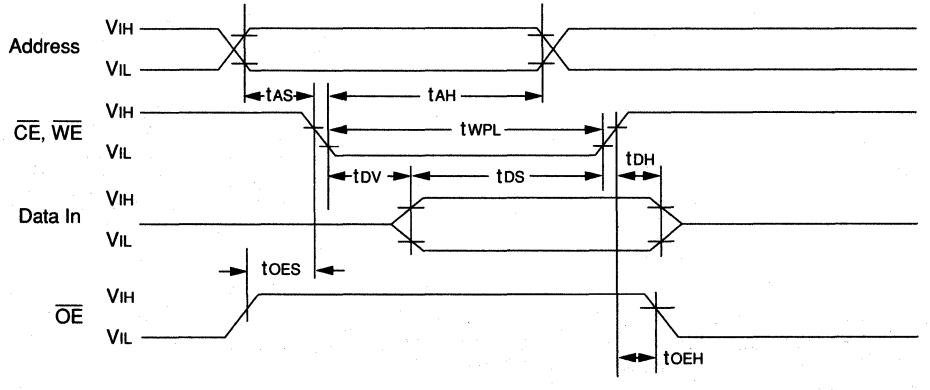
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

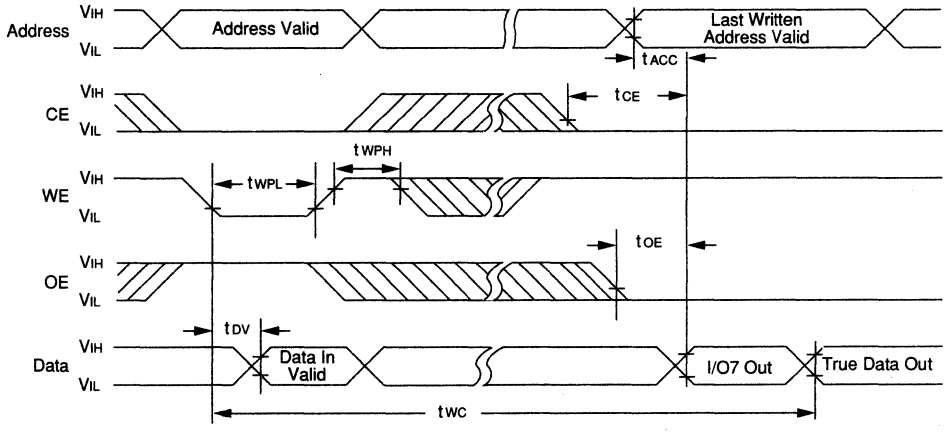
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C16A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

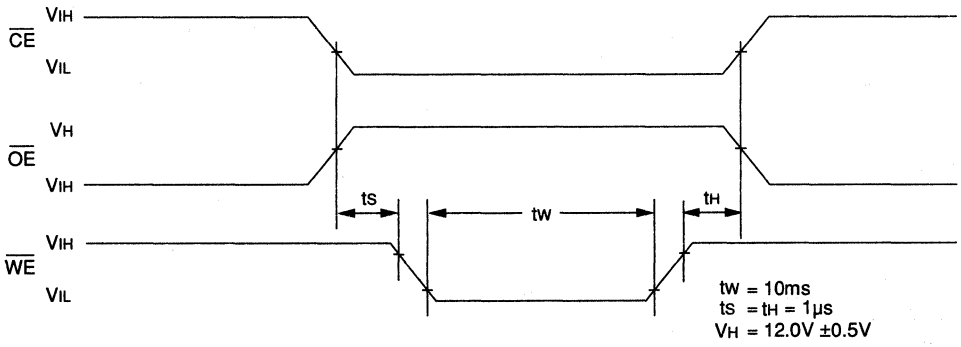
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

$\overline{Data}$ Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C16AF - 15 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier (LCC)
	L	Plastic Leaded Chip Carrier (PLCC))
	P	Plastic DIP
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	15	150 nsec
	20	200 nsec
	25	250 nsec
Option:	-	= twc = 1ms
	F	= twc = 200µs
Device:	16K	(2K x 8) CMOS EEPROM

28C17A

16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

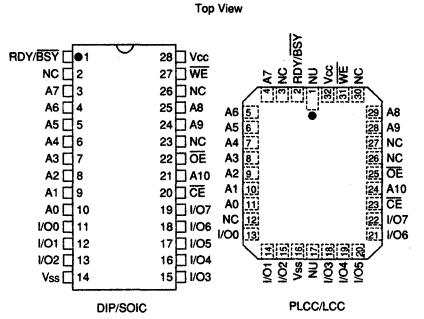
- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Ready/$\overline{\text{Busy}}$
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - —28 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Military *: -55° C to 125° C

DESCRIPTION

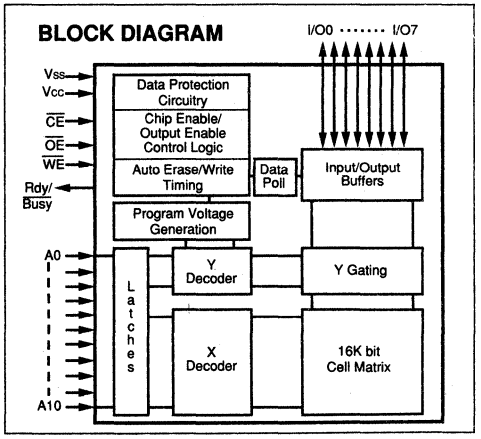
The Microchip Technology Inc 28C17A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{Data}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

* See military data sheet DS60036.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

V_{CC} and input voltages w.r.t. V_{SS} .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. V_{SS} .....-0.6V to +13.5V
Voltage on A9 w.r.t. V_{SS} .....-0.6V to +13.5V
Output Voltage w.r.t. V_{SS} .....-0.6V to V_{CC}+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

V_{CC} = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN}= -0.1V to V_{CC}+1
Input Capacitance		C_{IN}		10	pF	V_{IN} = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
Output Leakage		I_{LO}	-10	10	µA	V_{OUT} = -0.1V to V_{CC}+0.1V
Output Capacitance		C_{OUT}		12	pF	V_{IN} = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	I_{CC}		30	mA	f = 5 MHz (Note 1) V_{CC} = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$		2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0° C to 70° C) $\overline{CE}$ = V_{IH} (-40° C to 85° C) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1

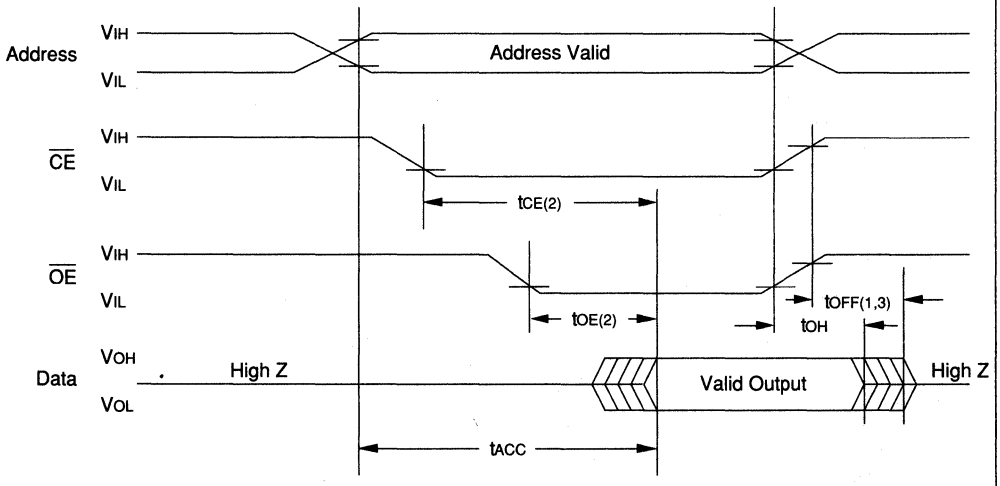
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C17A-15		28C17A-20		28C17A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

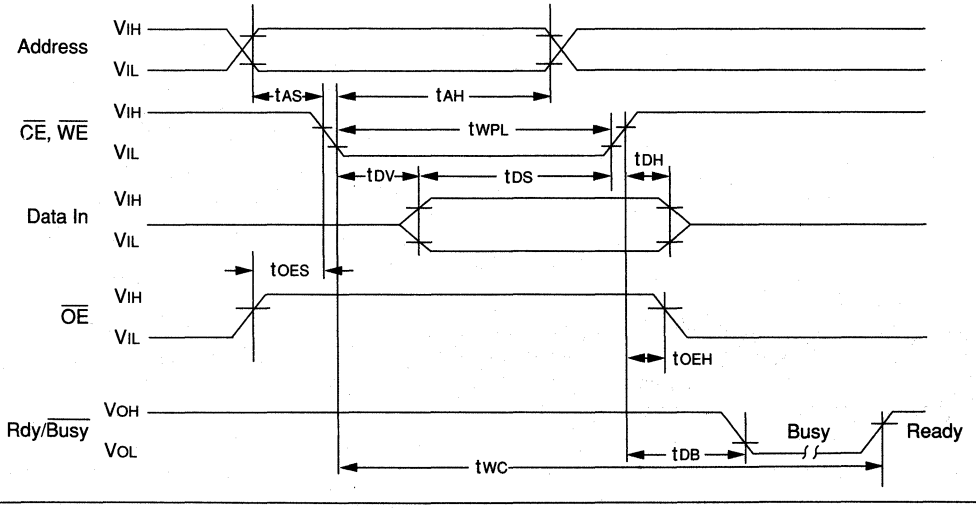
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

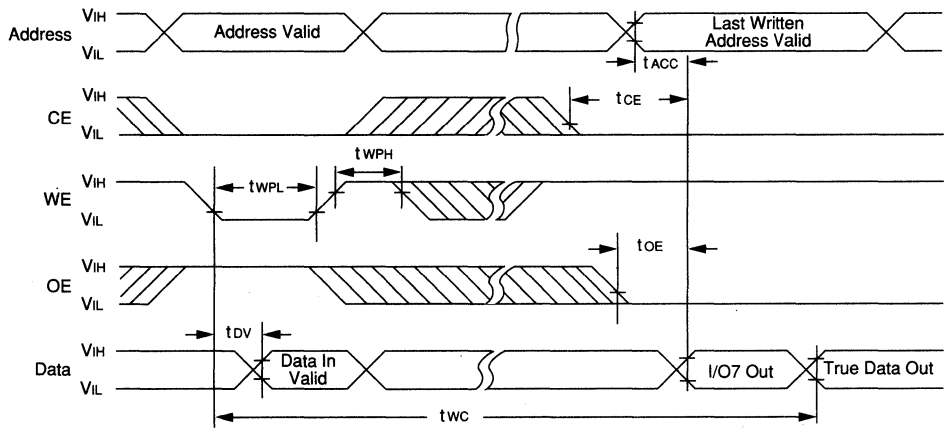
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Time to Device Busy	t_{DB}		50	ns	
Write Cycle Time (28C17A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C17AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

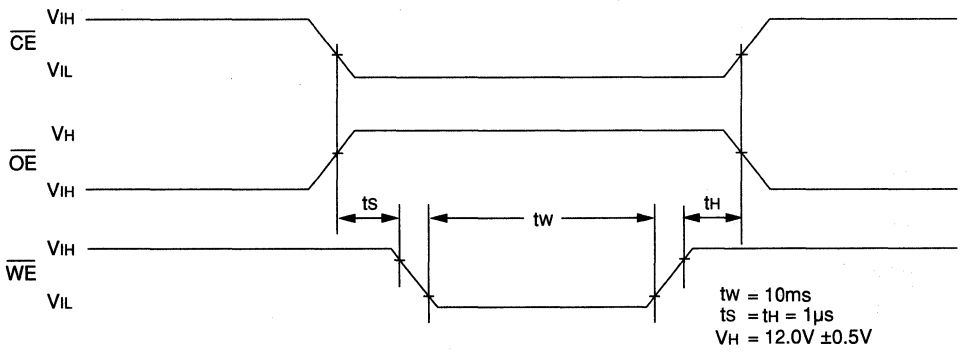
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

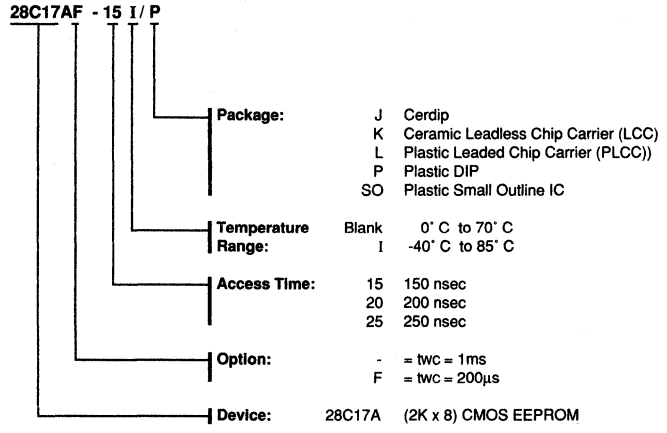
All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



28C17A

DICE FORM

16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

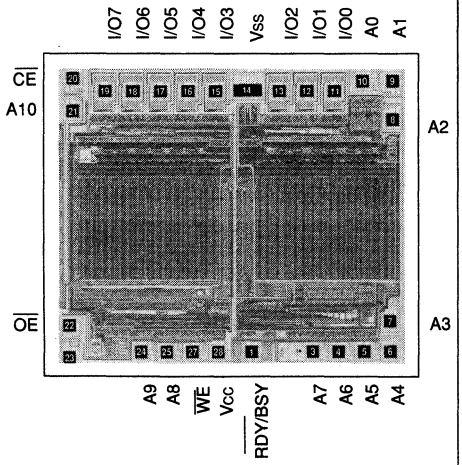
- 250ns Access Time
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100μA Standby
- Fast Byte Write Time—1ms
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Ready/$\overline{\text{Busy}}$
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Commercial Temperature Range:
  - — 0° C to 70° C
- Available in Wafer Form or Waffle Pack

DESCRIPTION

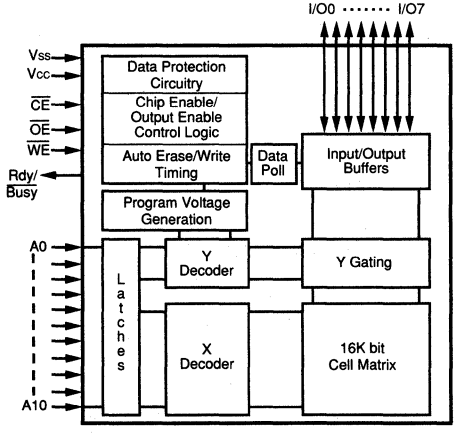
The Microchip Technology Inc 28C17A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{Data}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required.

DIE CONFIGURATION

Die Size: 137 x 117 sq. mils



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V
Voltage on A9 w.r.t. Vss .....-0.6V to +13.5V
Output Voltage w.r.t. Vss .....-0.6V to Vcc+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial: Tamb= 0° C to 70° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input CMOS input	ICC(S)TTL ICC(S)CMOS		2 100	mA µA	$\overline{CE}$ = VIH $\overline{CE}$ = Vcc-0.3 to Vcc+1

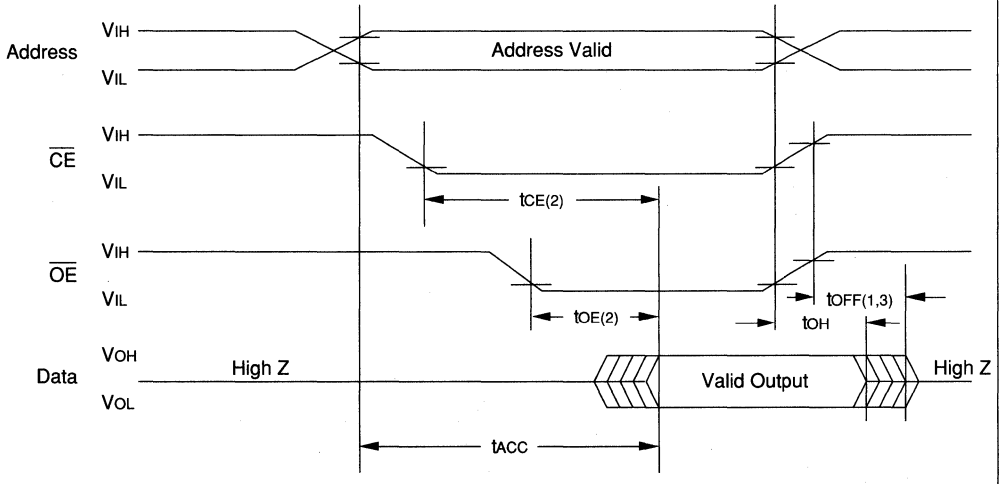
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C

Parameter	Sym	28C17A-25		Units	Conditions
		Min	Max		
Address to Output Delay	t_{ACC}		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

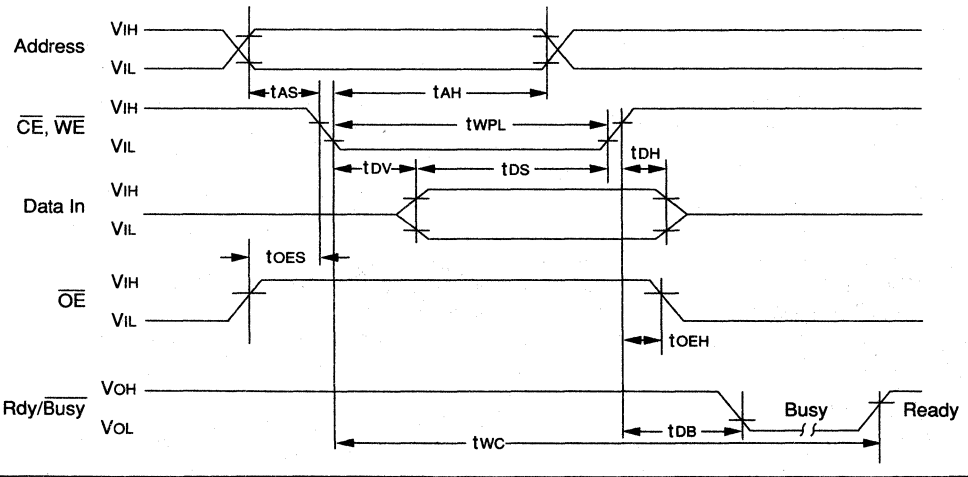
BYTE WRITE AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial: Tamb = 0°C to 70°C

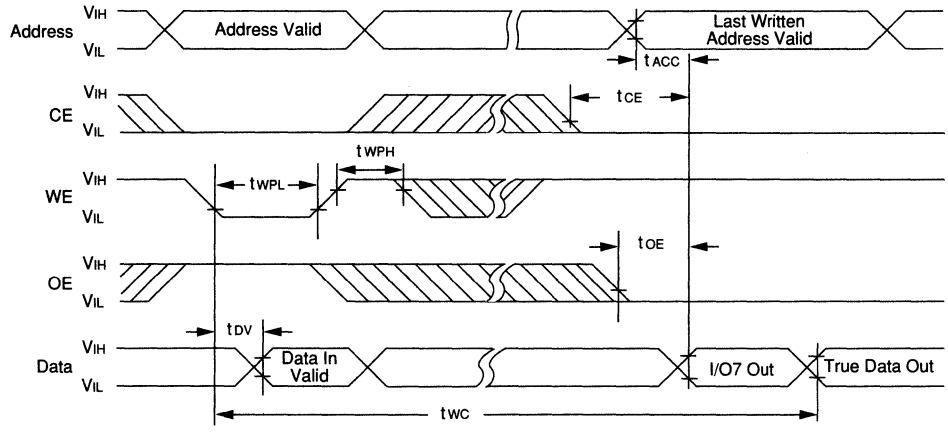
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-up Time	t_{AS}	50		ns	
Address Hold Time	t_{AH}	100		ns	
Data Set-Up Time	t_{DS}	100		ns	
Data Hold Time	t_{DH}	50		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}	-	1000	ns	Note 2
Time to Device Busy	t_{DB}	-	50	ns	
Write Cycle Time (28C17A)	t_{WC}	-	1	ms	0.5 ms typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

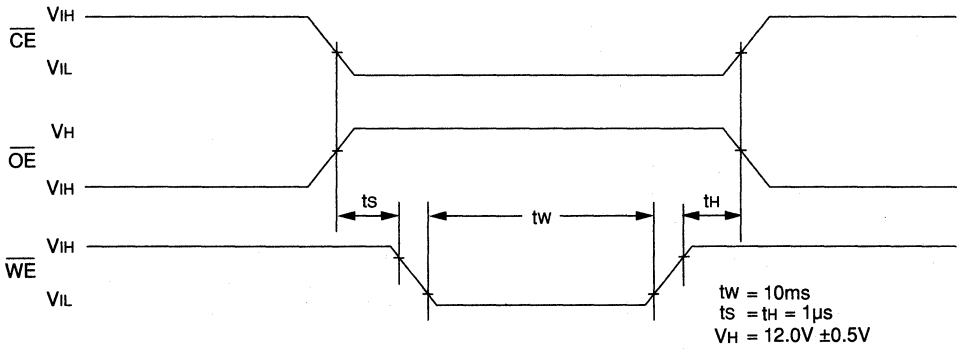
PROGRAMMING Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C17A - 25 - / W

Package:	W	Dice in Wafer Form
	S	Dice in Waffle Pack
Temperature Range:	Blank	0° C to 70° C
Access Time:	25	250 nsec
Device:	28C17A	(2K x 8) CMOS EEPROM

Microchip

28C64A

64K (8K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100μA Standby
- Fast Byte Write Time—200μs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - —28 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Military**: -55° C to 125° C

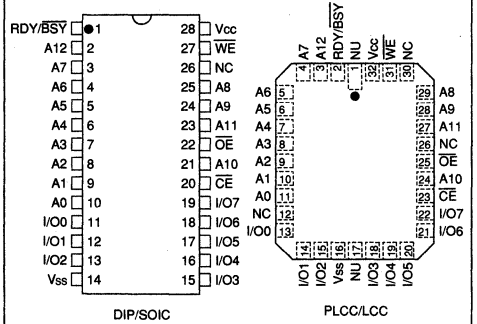
DESCRIPTION

The Microchip Technology Inc 28C64A is a CMOS 64K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

** See Military Data Sheet DS60003

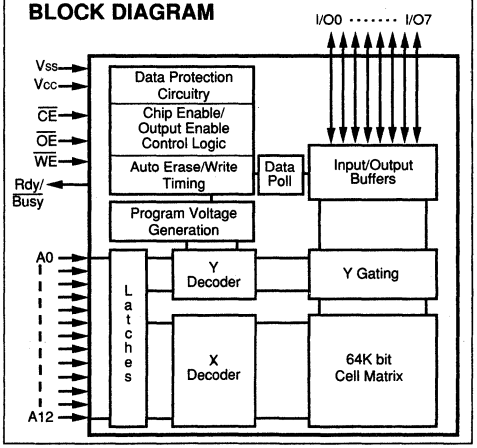
PIN CONFIGURATION

Top View



● Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
VCC	+5V Power Supply
VSS	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. VSS .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. VSS .....-0.6V to +13.5V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output Voltage w.r.t. VSS .....-0.6V to VCC+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN= -0.1V to VCC+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT= -0.1V to VCC+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) VCC = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 85° C) $\overline{CE}$ = VCC-0.3 to VCC+1

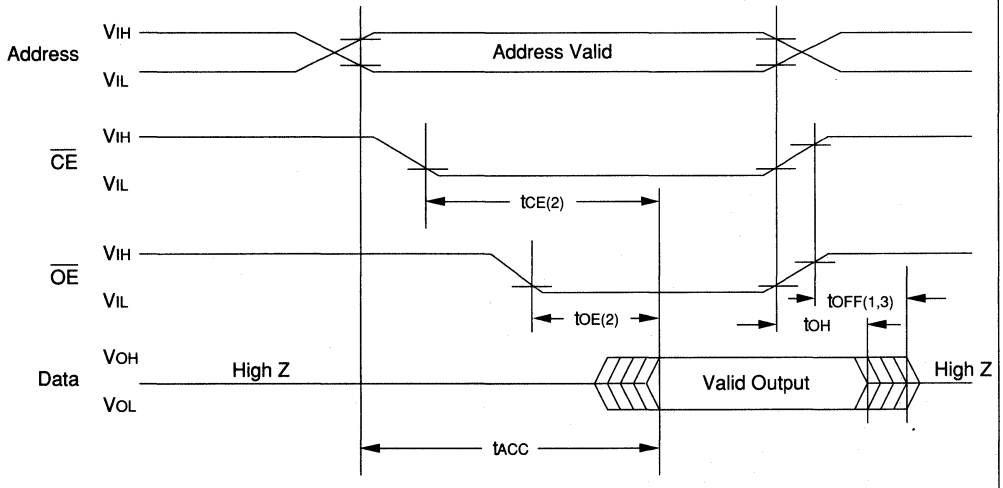
Note: (1) AC power supply current above 5 MHz: 2 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

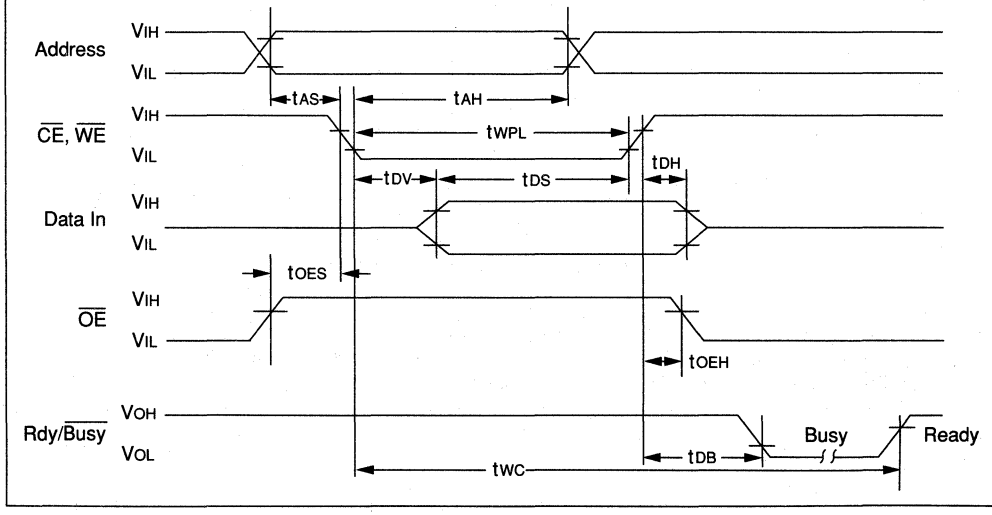
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

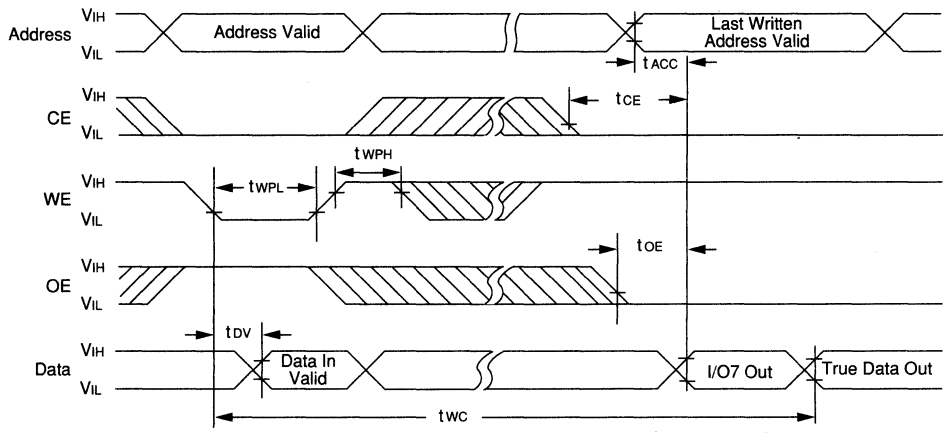
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Time to Device Busy	t_{DB}		50	ns	
Write Cycle Time (28C64A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

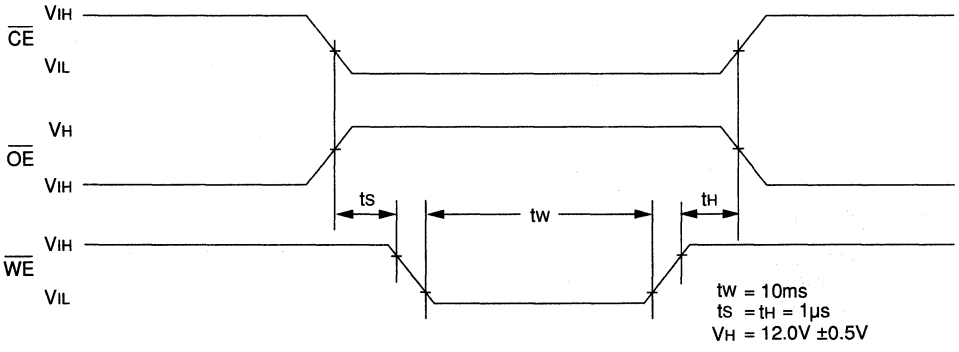
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FE0 to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C64AF - 15 I / P

Package:		J	Cerdip
		K	Ceramic Leadless Chip Carrier (LCC)
		L	Plastic Leaded Chip Carrier (PLCC))
		P	Plastic DIP
		SO	Plastic Small Outline IC
Temperature Range:		Blank	0° C to 70° C
		I	-40° C to 85° C
Access Time:		15	150 nsec
		20	200 nsec
		25	250 nsec
Option:		-	= twc = 1ms
		F	= twc = 200µs
		X	Pin 1 NC (Pin 2 PLCC), twc = 1ms
Device:		64K	(8K x 8) CMOS EEPROM

Microchip

28C64A

DICE FORM

64K (8K x 8) CMOS Electrically Erasable PROM

FEATURES

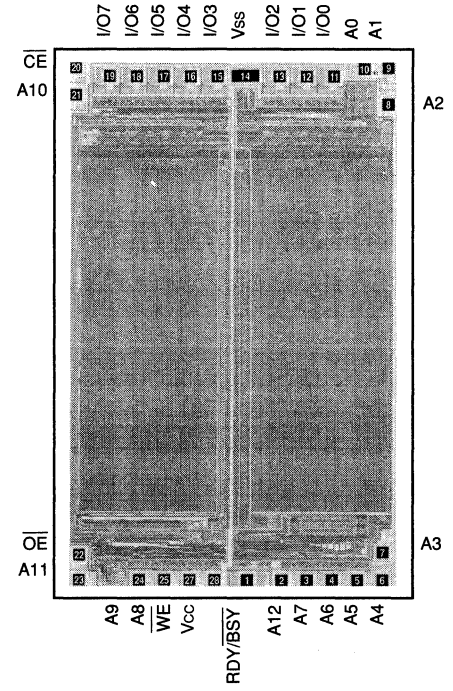
- 250ns Access Time
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—1ms
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Commercial Temperature Range:
  - — 0° C to 70° C
- Available in Wafer Form or Waffle Pack

DESCRIPTION

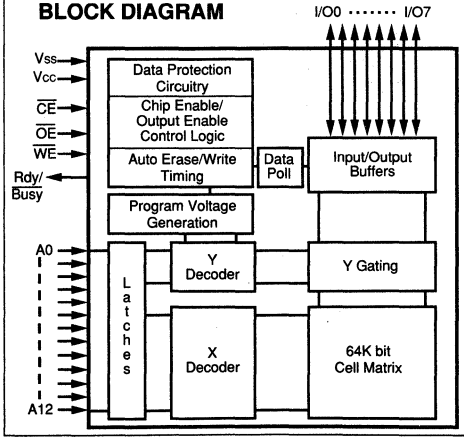
The Microchip Technology Inc 28C64A is a CMOS 64K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required.

DIE CONFIGURATION

Die Size: 134 x 206 sq. mils



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
VCC	+5V Power Supply
VSS	Ground
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. VSS .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. VSS .....-0.6V to +13.5V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output Voltage w.r.t. VSS .....-0.6V to VCC+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to VCC+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to VCC+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) VCC = 5.5V;
Power Supply Current, Standby	TTL input CMOS input	ICC(S)TTL ICC(S)CMOS		2 100	mA µA	$\overline{CE}$ = VIH $\overline{CE}$ = VCC-0.3 to VCC+1

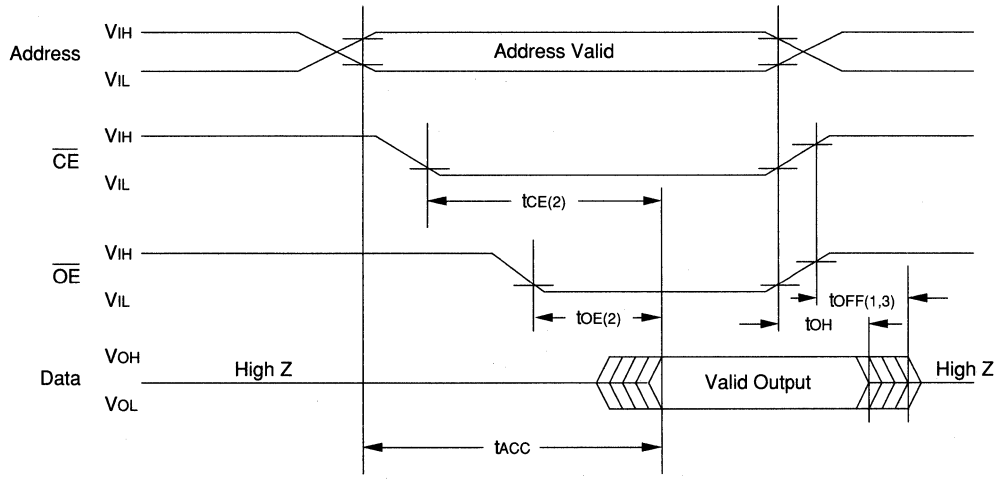
Note: (1) AC power supply current above 5 MHz: 2 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial: Tamb = 0°C to 70°C

Parameter	Sym	28C64A-25		Units	Conditions
		Min	Max		
Address to Output Delay	t_{ACC}		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

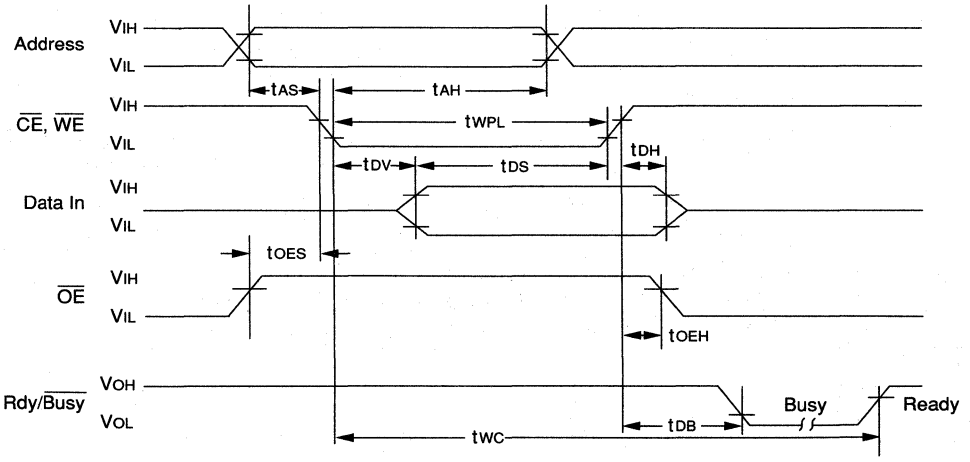
BYTE WRITE AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial: Tamb = 0°C to 70°C

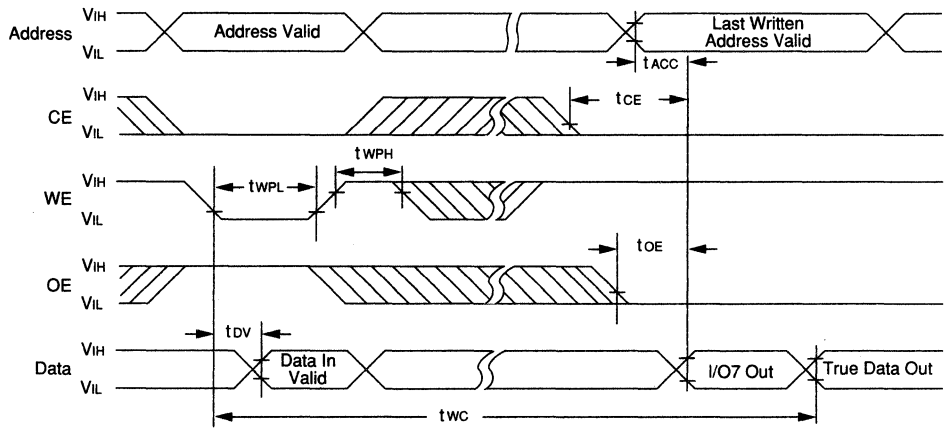
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-up Time	t_{AS}	50		ns	
Address Hold Time	t_{AH}	100		ns	
Data Set-Up Time	t_{DS}	100		ns	
Data Hold Time	t_{DH}	50		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}	-	1000	ns	Note 2
Time to Device Busy	t_{DB}	-	50	ns	
Write Cycle Time (28C64A)	t_{WC}	-	1	ms	0.5 ms typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of CE or WE, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of WE or CE, whichever occurs first.

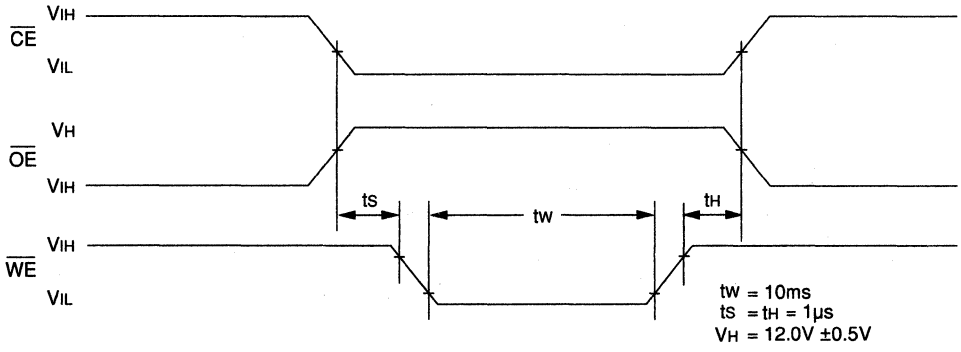
PROGRAMMING Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FE0 to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C64A - 25 - / W

Package:	W	Dice in Wafer Form
	S	Dice in Waffle Pack
Temperature Range:	Blank	0° C to 70° C
Access Time:	25	250 nsec
Device:	28C64A	(8K x 8) CMOS EEPROM

Microchip

SECTION 3
EPROM PRODUCT SPECIFICATIONS

3

Microchip

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS Technology for low power consumption
  —20mA Active current
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Automotive: -40° C to 125° C
  —Military** (B): -55° C to 125° C

DESCRIPTION

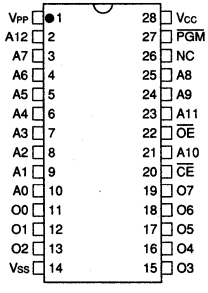
The Microchip Technology Inc 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. U.V. erasable versions are also available.

3

PIN CONFIGURATIONS

Top View



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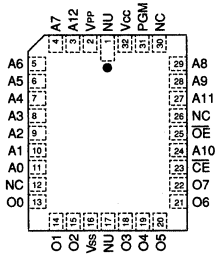
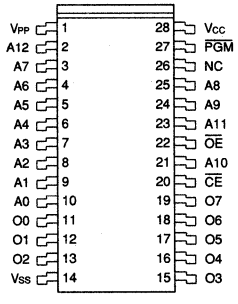


PLCC/LCC



SOIC

** See 27C64 Military Data sheet DS60011

PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

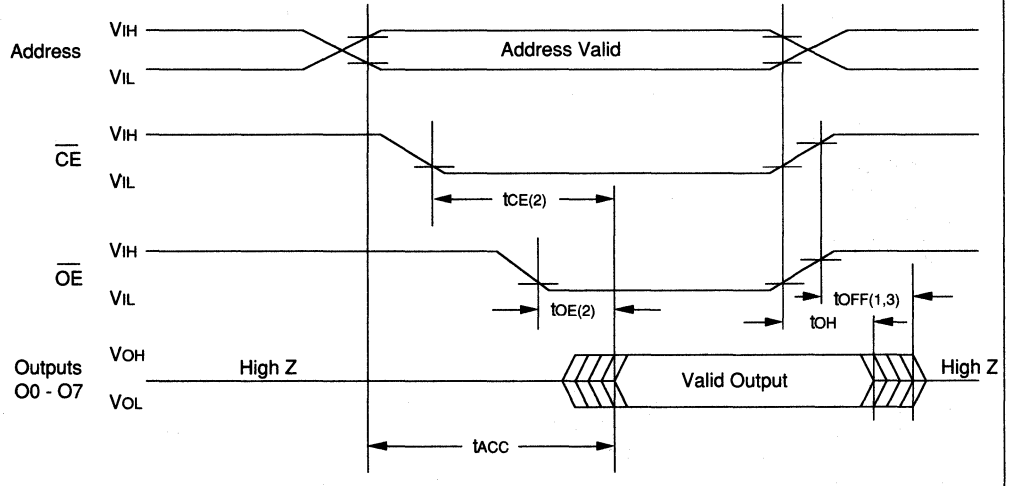
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 8mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C64-12		27C64-15		27C64-17		27C64-20		27C64-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		120		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0		0		0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current,program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

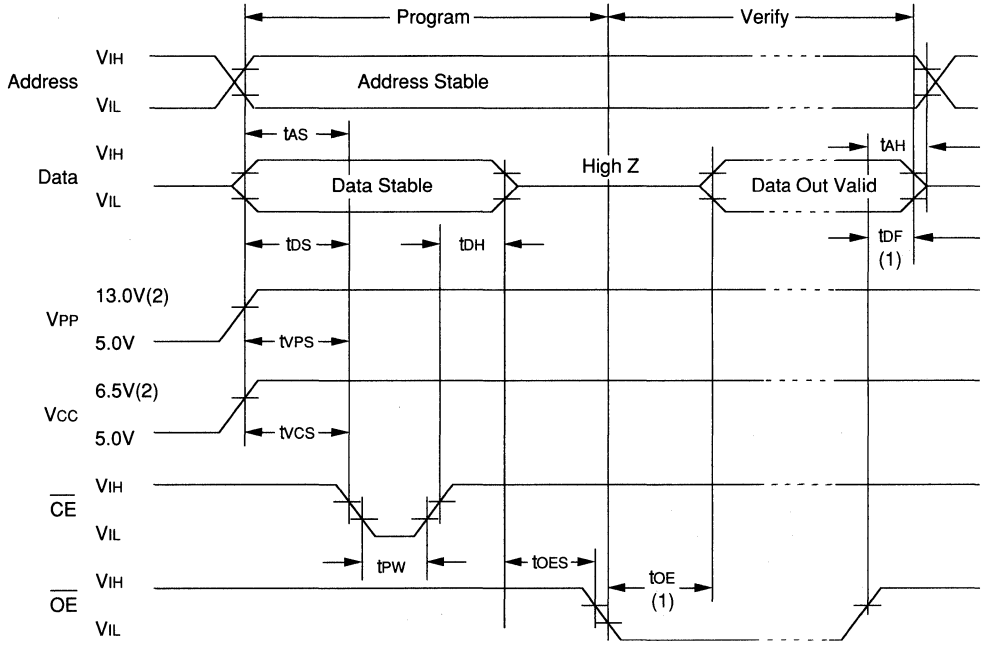
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100μA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

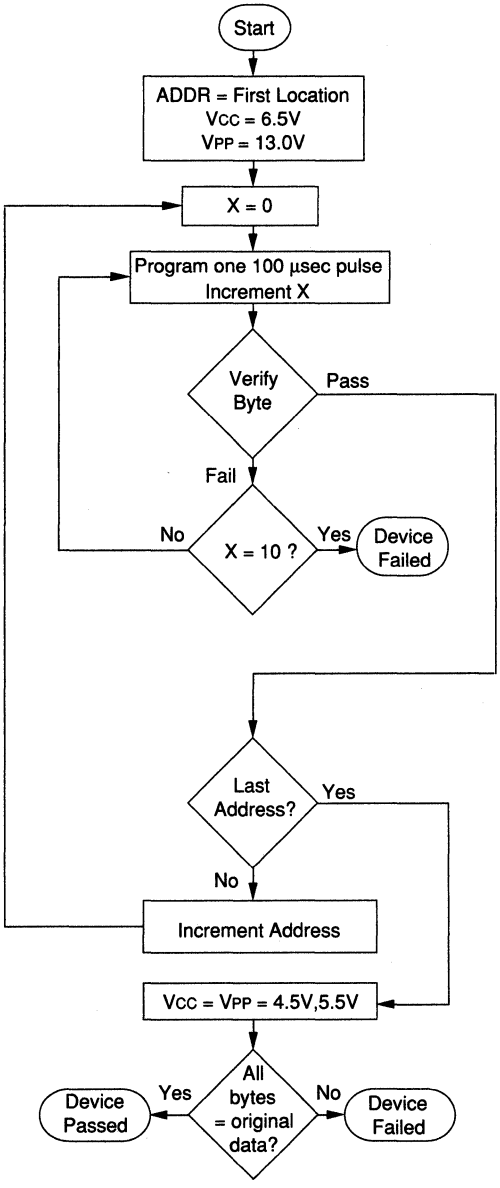
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

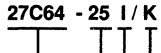
Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	12	120 nsec
	15	150 nsec
	17	170 nsec
	20	200 nsec
	25	250 nsec
Device:	27C64	64K (8K x 8) CMOS EPROM

Microchip

27C128

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —120ns Maximum access time
- CMOS Technology for low power consumption
  - —20mA Active current
  - —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —Tape and reel
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C
  - —Military**(B): -55° C to 125° C

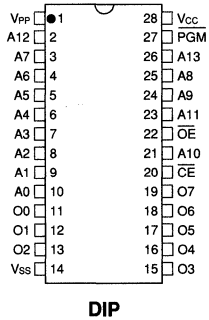
DESCRIPTION

The Microchip Technology Inc 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

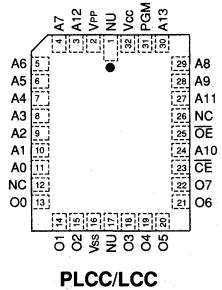
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

3

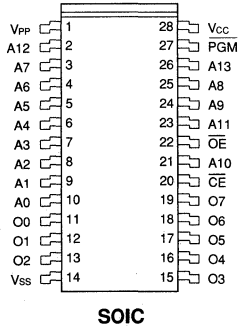
PIN CONFIGURATIONS
Top View



DIP



PLCC/LCC



SOIC

** See 27C128 Military Data sheet DS60012

PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

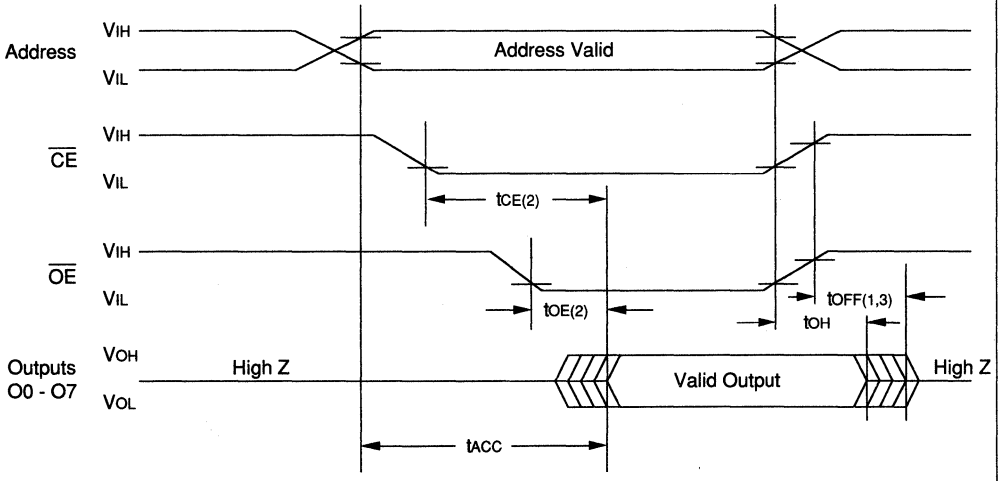
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 8mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		120		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0		0		0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current,program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

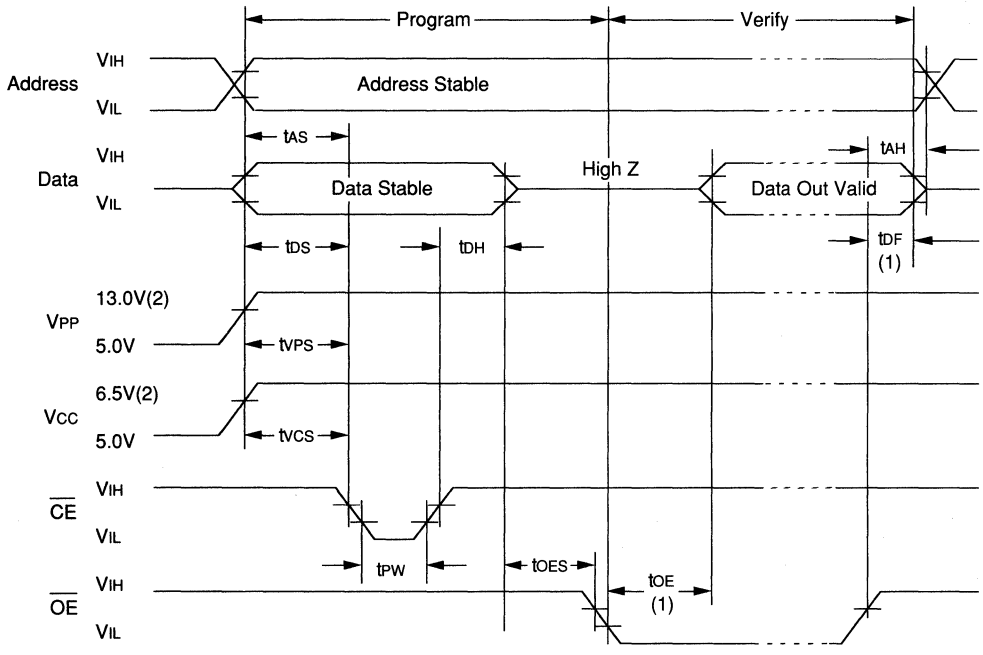
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.5 V ±0.25 V, V_{PP} = V_H = 13.0 V ±0.25 V for express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100µA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure1.

Programming takes place when:

a) V_{CC} is brought to proper voltages,
b) V_{PP} is brought to proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

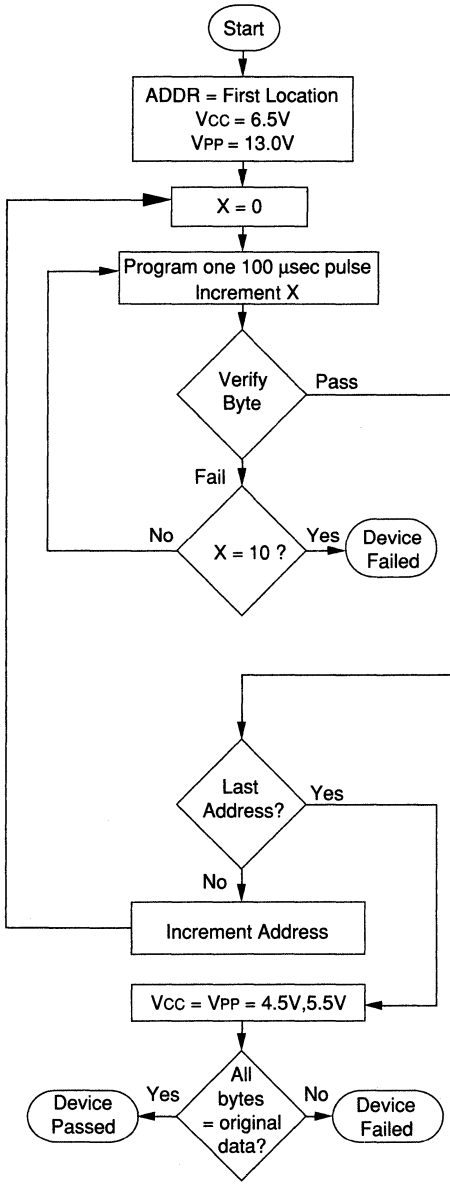
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	0	0	1	1	83

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
Tamb = 25° C ±5° C
VCC = 6.5 ±0.25V
VPP = 13.0 ±0.25V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C128 - 25 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	12	120 nsec
	15	150 nsec
	17	170 nsec
	20	200 nsec
	25	250 nsec
Device:	27C128	128K (16K x 8) CMOS EPROM

Microchip

27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS Technology for low power consumption
  —20mA Active current
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Automotive: -40° C to 125° C
  —Military** (B): -55° C to 125° C

DESCRIPTION

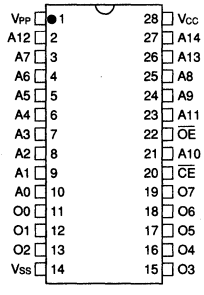
The Microchip Technology Inc 27C256 is a CMOS 256K bit (electrically) Programmable Read Only Memory. The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

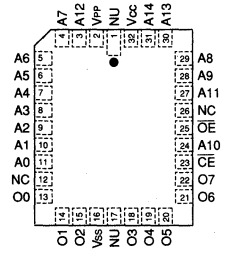
3

PIN CONFIGURATIONS

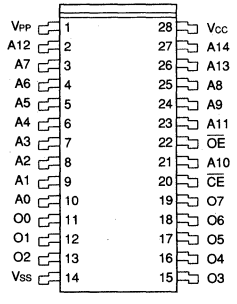
Top View



DIP



PLCC/LCC



SOIC

** See 27C256 Military Data sheet DS60013

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

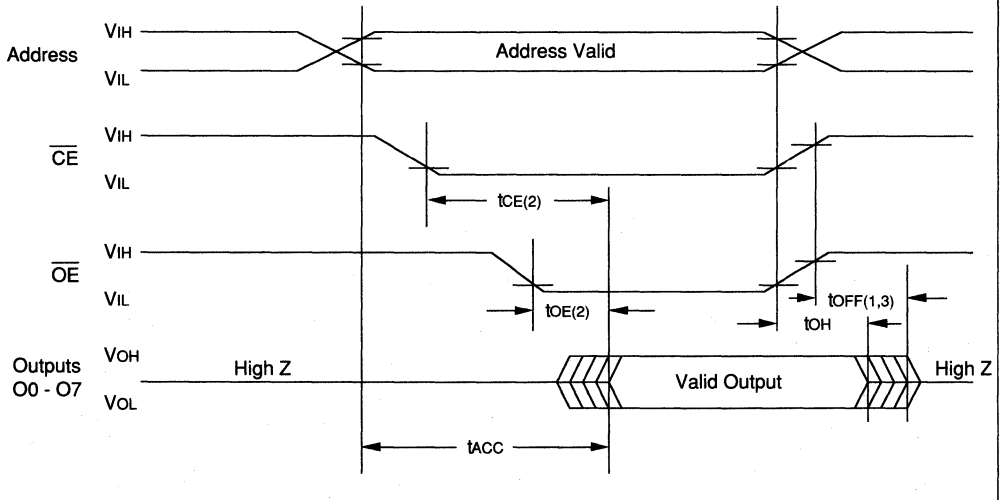
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 5mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C256-12		27C256-15		27C256-17		27C256-20		27C256-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		120		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		50		60		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	35	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current, program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

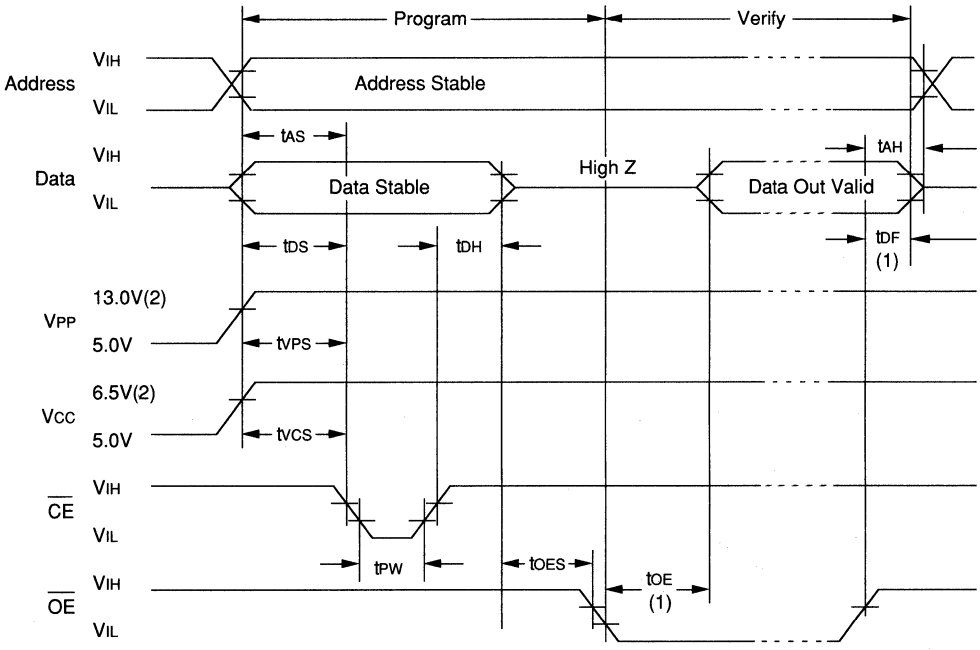
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for express algorithm

3

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100μA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

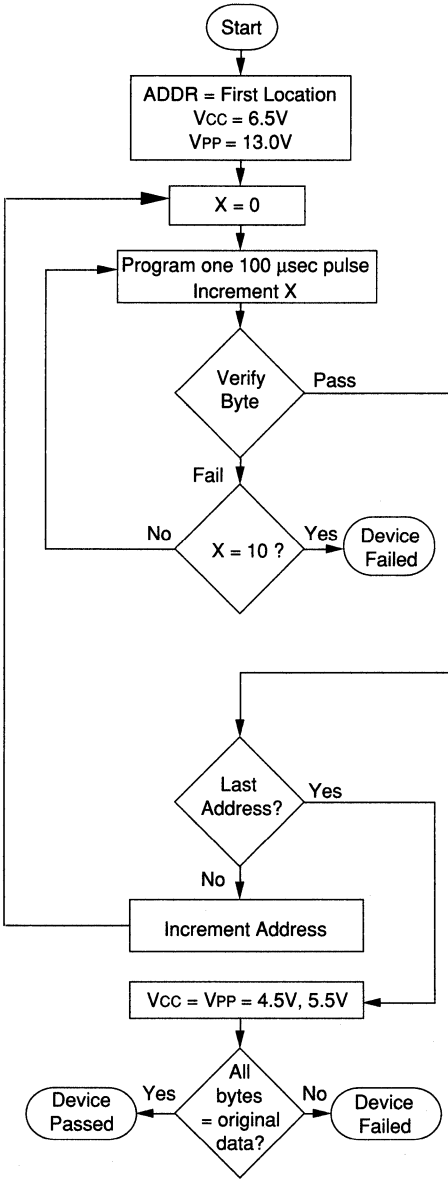
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C256 - 25 I / P

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	12	120 nsec
	15	150 nsec
	17	170 nsec
	20	200 nsec
	25	250 nsec
Device:	27C256	256K (32K x 8) CMOS EPROM

Microchip

27C512

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —120ns access time available
- CMOS Technology for low power consumption
  - —35mA Active current
  - —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- High speed "express" programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —Tape and reel
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C
  - —Military** (B): -55° C to 125° C

DESCRIPTION

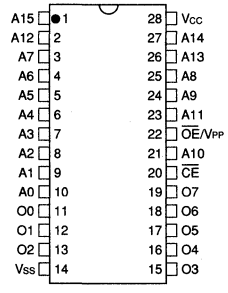
The Microchip Technology Inc 27C512 is a CMOS 512K bit (electrically) Programmable Read Only Memory. The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexability in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages. U.V. erasable versions are also available.

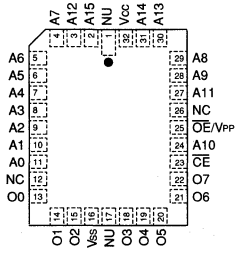
3

PIN CONFIGURATIONS

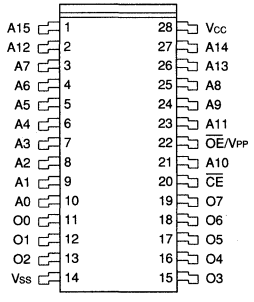
Top View



DIP



PLCC/LCC



SOIC

**See 27C512 Military Data Sheet DS60014

PIN FUNCTION TABLE

Name	Function
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN= 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT= 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC ICC		35 45	mA mA	VCC = 5.5V f = 1MHz; $\overline{OE}$/VPP= $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC;
Power Supply Current, Standby	S X S	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 2mA/MHz.

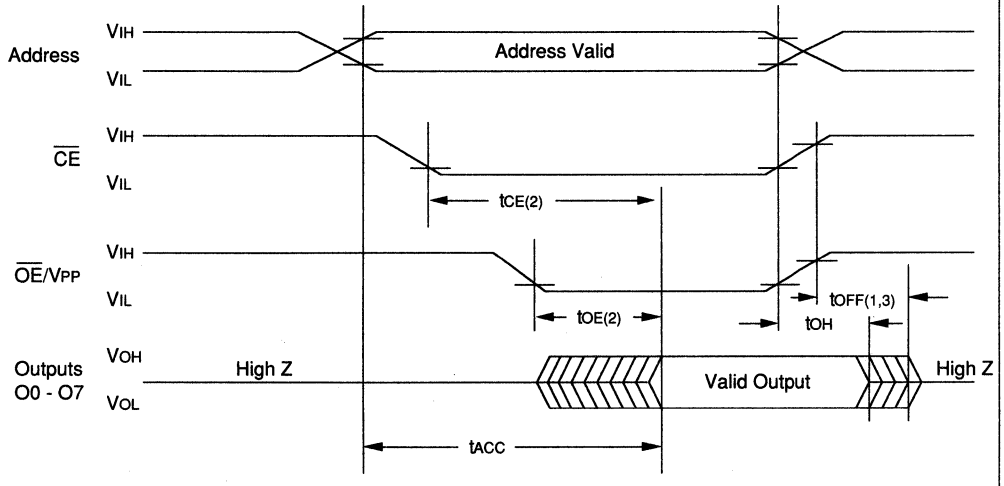
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0 V and V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C512-12*		27C512-15		27C512-17		27C512-20		27C512-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		120		150		170		200		250	ns	$\overline{OE}/V_{PP}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occured first	t_{OH}	0		0		0		0		0		ns	

*27C512-12 is only available in commercial temperature range

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	V_{CC}+1	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Current (all inputs)		I_{IL}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1"	V_{OH}	2.4		V	I_{OH} = -400µA
	Logic "0"	V_{OL}		0.45	V	I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		35	mA	
$\overline{OE}/V_{PP}$ Current, program		I_{PP2}		25	mA	$\overline{CE}$ = V_{IL}
A9 Product Identification		V_{ID}	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

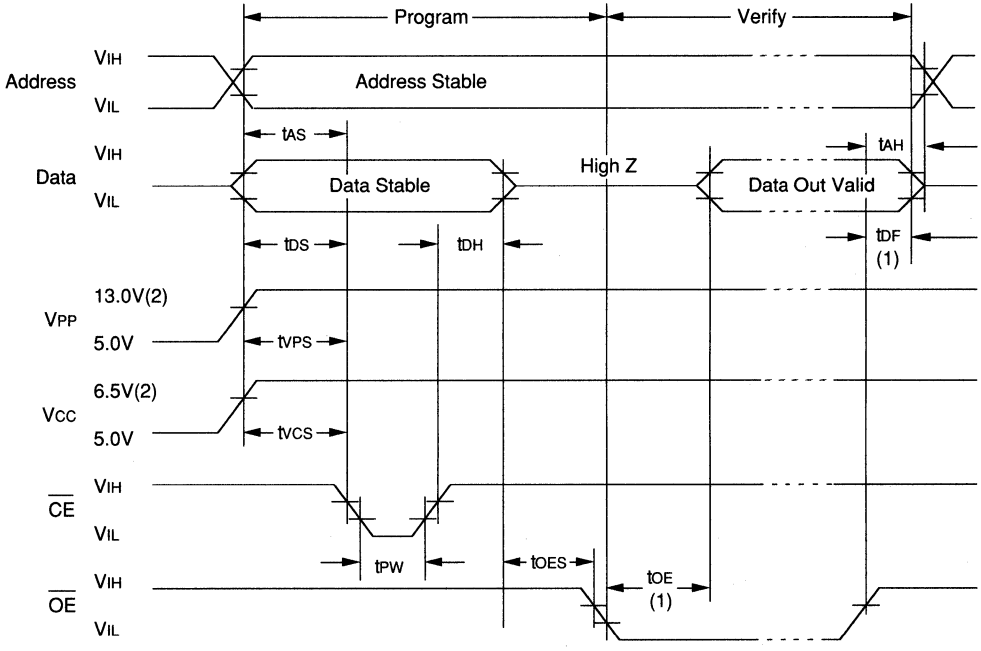
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
$\overline{OE}$ Hold Time	t_{OEH}	2		µs	
$\overline{OE}$ Recovery Time	t_{OR}	2		µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50		ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ± 5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.5 V ±0.25 V, V_{PP} = V_H = 13.0 V ±0.25 V for express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

When this condition is met, the supply current will drop from 35mA to 100μA.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprcessor systems and the outputs go to high impedance when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"'s state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

Identity Mode

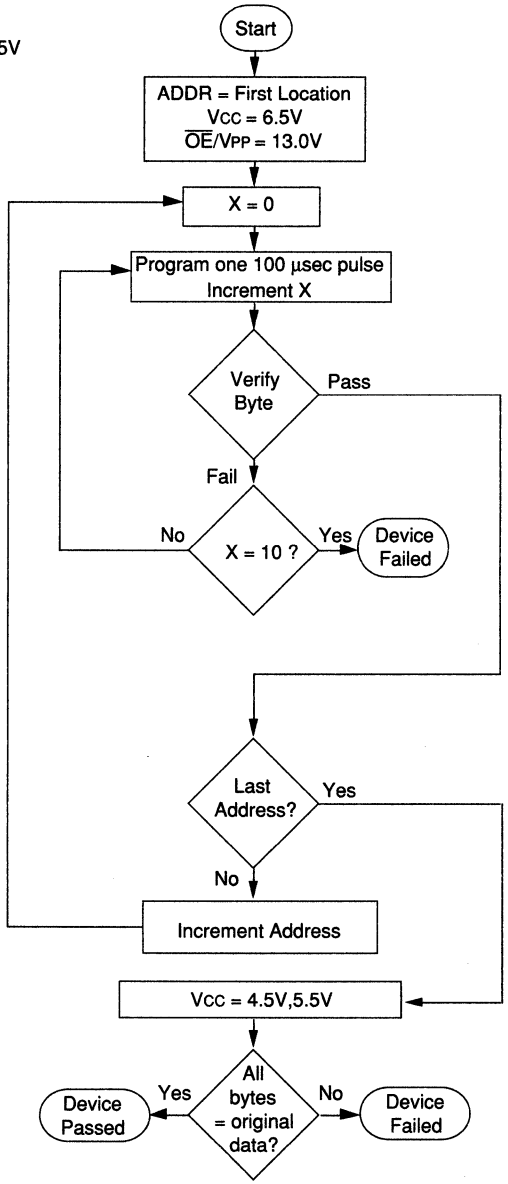
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
$\overline{OE}/V_{PP}$ = 13.0 ±0.25V



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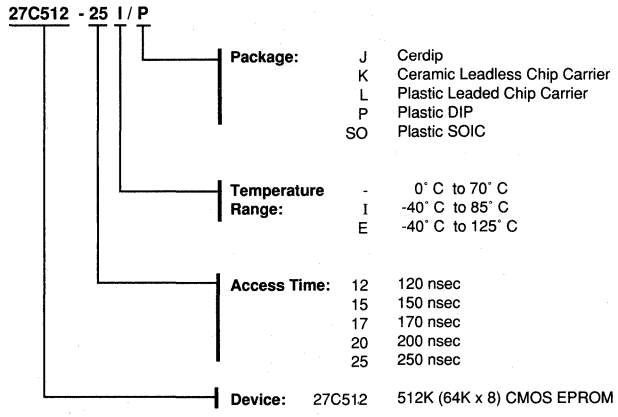
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

27HC64

64K (8K x 8) High Speed CMOS UV Erasable PROM

FEATURES

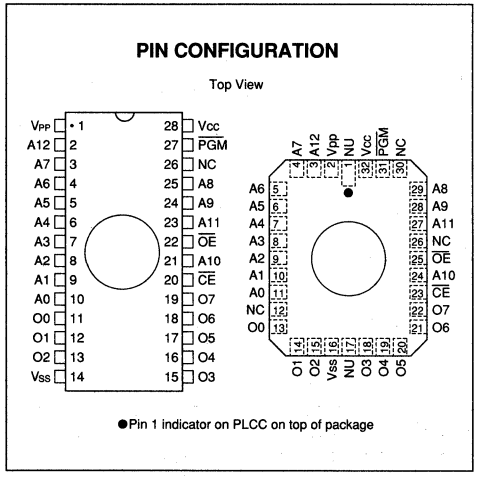
- Bipolar Performance
  - — 40ns Maximum Access Time
- CMOS Technology For Low Power Consumption
  - — 80mA Active Current
  - — 100µA Standby Current (Low Power Option)
- OTP (One Time Programming) Available
- Auto-Insertion-Compatible Plastic Packages
- Auto ID™ Aids Automated Programming
- Separate Chip Enable and Output Enable Controls
- Two Programming Algorithms Allow Improved Programming Times
  - — Fast Programming
  - — Express
- Organized 8K x 8: JEDEC Standard Pinouts
  - — 28 Pin Dual in Line Package
  - — 32 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - — Commercial: 0° C to 70° C
  - — Industrial: -40° C to 85° C
  - — Military**: -55° C to 125° C

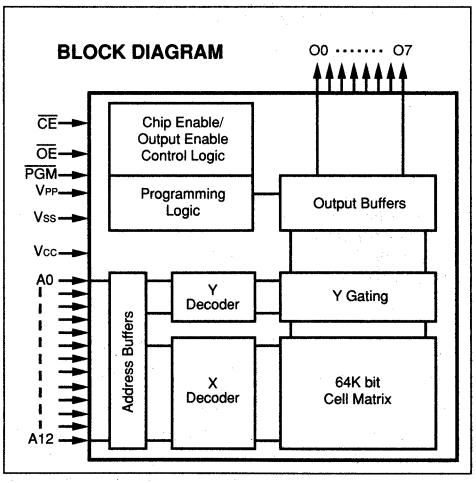
DESCRIPTION

The Microchip Technology Inc 27HC64 is a CMOS 64K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design allows bipolar speed with a significant reduction in power over bipolar PROMs. A low power option (L) allows further standby power reduction to 100µA. The 27HC64 is configured in a standard 64K EPROM pinout, which allows an easy upgrade for 27C64 sockets. This very high speed device allows digital signal processors (DSP) or other sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. One Time Programming (OTP) is available for low cost (plastic) applications.

3





** See 27HC64 Military Data sheet DS60006

PIN FUNCTION TABLE	
Name	**Function**
$\overline{A0}$ - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS ... -0.6V to + 7.25V
VPP voltage w.r.t. VSS during programming ... -0.6V to + 14V
Voltage on A9 w.r.t. VSS ... -0.6V to +13.5V
Output voltage w.r.t. VSS ... -0.6V to VCC +1.0V
Storage temperature ... -65° C to 150° C
Ambient temp. with power applied -65° C to 125° C
ESD protection on all pins ... 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 4mA IOL = 16mA
Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S,L SX,LX	TTL input TTL input	ICC1 ICC2		80 90	mA mA	VCC = 5.5V; VPP = VCC $\overline{f}$ = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		40 50	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2 MHz: 3mA/MHz for standard part; 5 mA/MHz for industrial temperature range part.
(2) VCC must be applied before (or simultaneously with VPP), and be removed after (or simultaneously with) VPP.

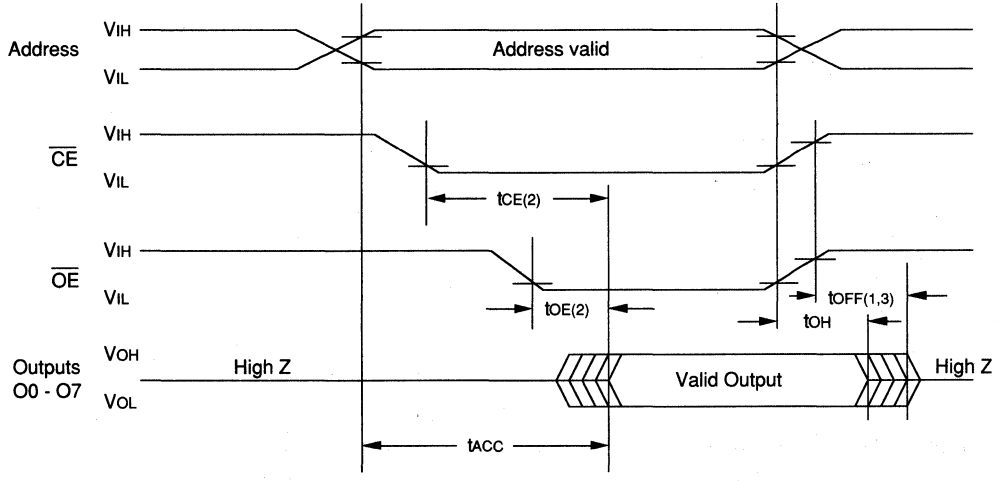
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Part*	Sym	27HC64-40		27HC64-45		27HC64-55		27HC64-70		Units	Conditions
			Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		40		45		55		70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}		40 30		45 30		55 35		70 45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}		25		25		25		25	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	20	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0		0		0		0		ns	

* Parts: S = Standard Power; L = Low Power
** 27HC64-40 is only available in commercial temperature range

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
For V_{PP} and V_{CC} Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = OV to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4mA I_{OL} = 16mA
V_{CC} Current, program & verify		I_{CC}		80	mA	Note 1
V_{PP} Current,program		I_{PP}		40	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

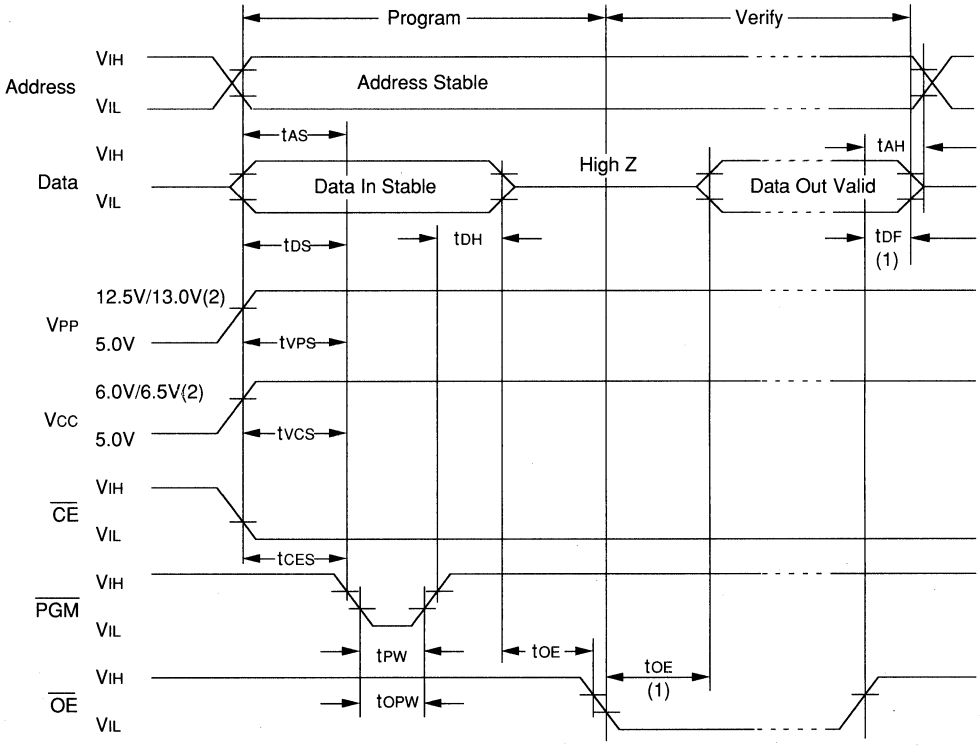
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
For V_{PP} and V_{CC} Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Overprogram Pulse Width (2)	t_{OPW}	2.85	78.75	ms	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.0 V ±0.25 V, VPP = VH = 12.5 V ±0.25 V for fast programming algorithm
VCC = 6.5 V ±0.25 V, VPP = VH = 13.0V ±0.25 V for Express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations on the low powered version, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). A faster $\overline{CE}$ access time (tCE) is available on the standard part to provide the additional time for decoding of the $\overline{CE}$ signal. Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}).

When this condition is met, the supply current will drop from 80mA to 100μA on the low power part and to 40mA on the standard part.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the Express algorithm is shown in Figure 2.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device in conjunction with the $\overline{PGM}$ line low, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

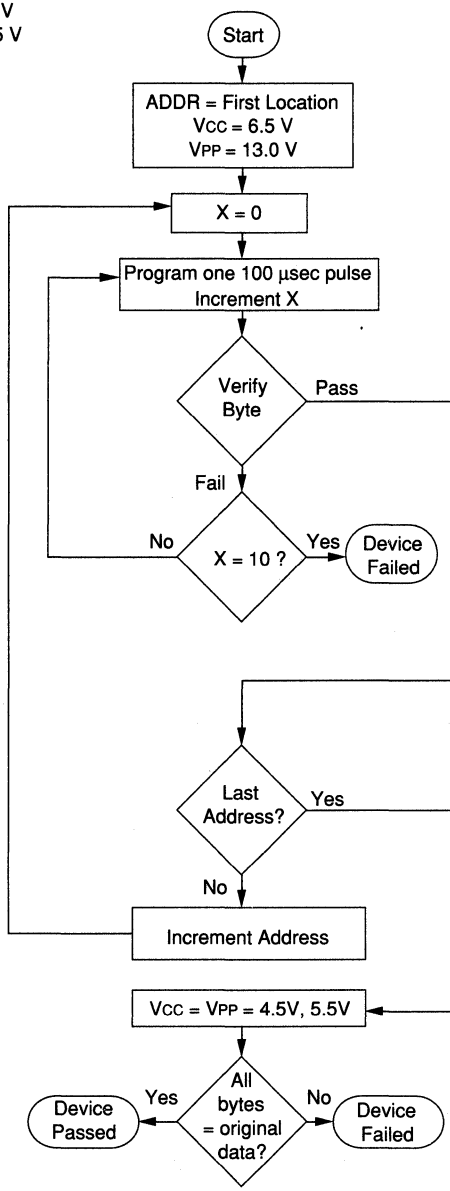
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc., and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	0	0	1	91

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

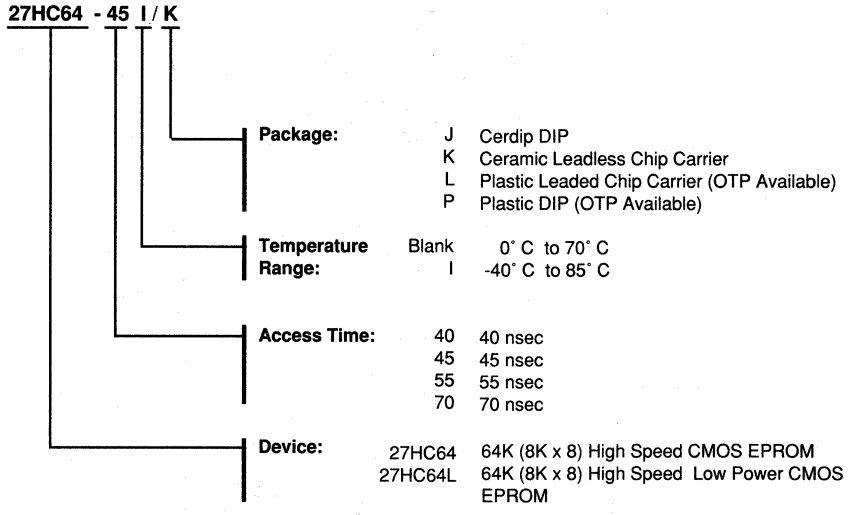
Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25 V
V_{PP} = 13.0 ±0.25 V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

27HC256

256K (32K x 8) High Speed CMOS EPROM

FEATURES

- High speed performance
  —55ns access time available
- CMOS technology for low power consumption
  —55mA active current
  —100μA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Organized in 32K x 8 - JEDEC Standard Pinouts
  —28-pin Dual-in-line and SOIC package
  —32-pin Chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial: 0° C to +70° C
  —Industrial: -40° C to +85° C
  —Automotive: -40° C to +125° C
  —Military**: -55° C to +125° C

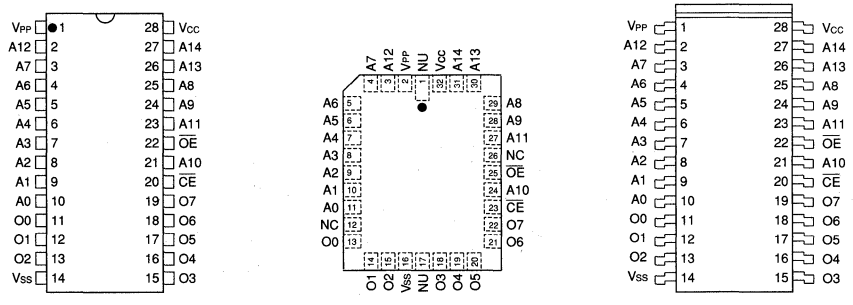
DESCRIPTION

The Microchip Technology Inc 27HC256 is a CMOS 256K bit (electrically) Programmable Read Only Memory. The device is organized into 32K words of 8 bit each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100μA. The 27HC256 is configured in a standard 256K EPROM pinout which allows an easy upgrade for present 27C256 users. A complete family of packages are offered to provide the utmost flexibility. The 27HC256 allows high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing makes this part suitable for applications where reliability and reduced power consumption are essential.

3

PIN CONFIGURATIONS

TOP VIEW



**See 27HC256 Military Data Sheet DS60009A

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Temperature under bias ..... -65° C to 125° C
Storage temperature ..... -65° C to 150° C
Maximum exposure to UV 7258Wsec/cm²
ESD protection on all pins 2.0kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%

Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1V to VCC +1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4mA IOL = 16mA
Output Leakage	all		ILO	-10	10	µA	VOUT = -0.1V to VCC +0.1V
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb = 25°C; f = 1MHz
Power Suppy Current, Active	S,L X	TTL input TTL input	ICC1 ICC2		55 65	mA mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		35 40	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC -0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial and Automotive Temp. Ranges;
Notes: (1) AC Power component above 2 MHz: 3mA/MHz for standard part; 5 mA/MHz for extended temperature range part.
(2) VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP.

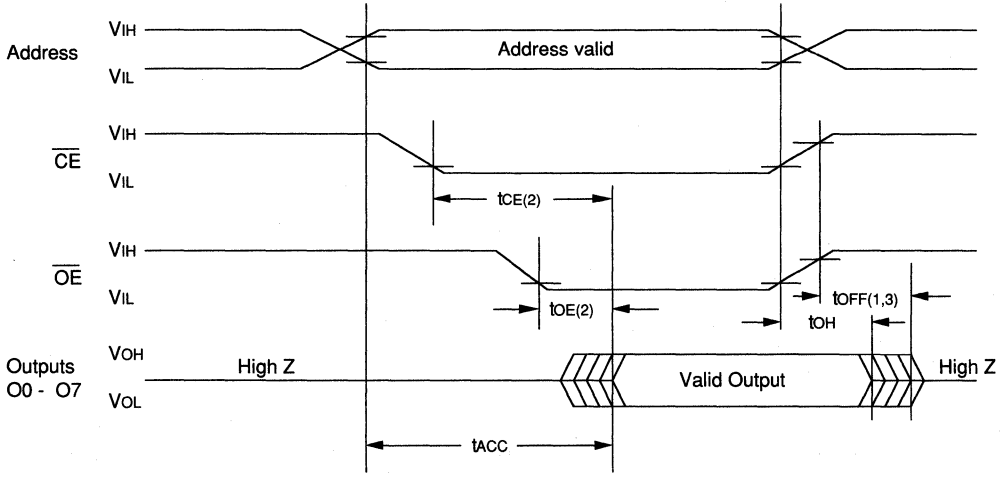
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Part*	Sym	27HC256-55**		27HC256-70		27HC256-90		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	tACC		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	tCE1 tCE2		55 45		70 45		90 50	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	tOE		30		35		40	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to O/P High Impedance	all	tOFF	0	25	0	30	0	35	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	tOH	0		0		0		ns	

* Parts: S = Standard Power; L = Low Power
** 27HC256-55 is only available in commercial temperature range

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

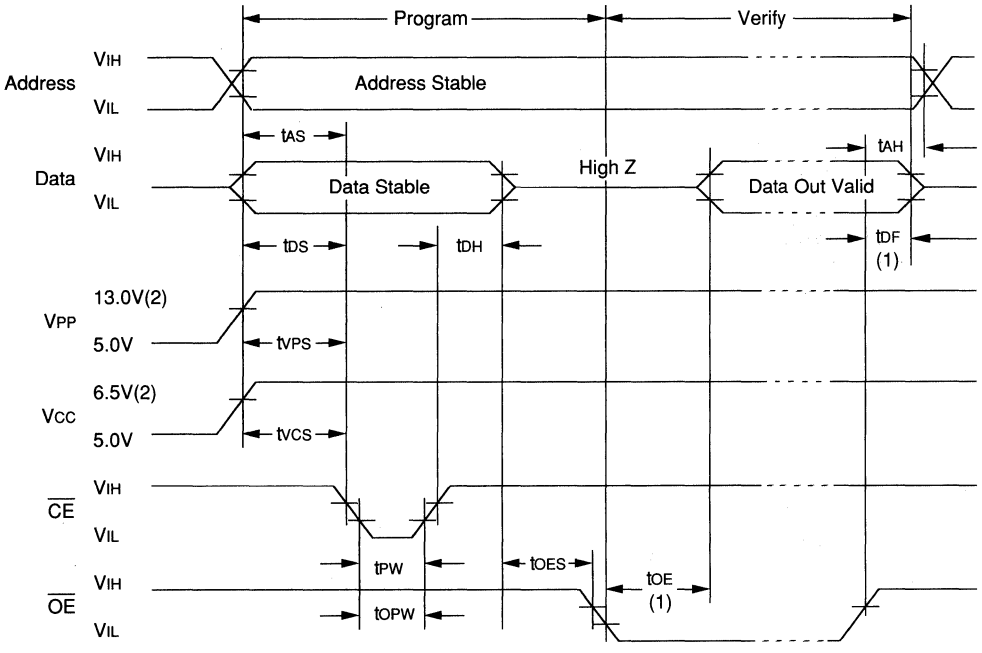
PROGRAMMING DC Characteristics		Ambient Temperature: Tamb = 25° C ±5° C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = OV to VCC
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4mA IOL = 16mA
VCC Current, program & verify		ICC		55	mA	
VPP Current, program		IPP		30	mA	Note 1
A9 Product Identification		VH	11.5	12.5	V	

Note: (1) VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH = 2.4V and VIL = 0.45V; VOH = 2.0V; VOL = 0.8V Output Load: 1 TTL Load + 100 pF Ambient Temperature: Tamb = 25° C ±5° C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2		µs	
Data Set-Up Time	tDS	2		µs	
Data Hold Time	tDH	2		µs	
Address Hold Time	tAH	0		µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2		µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{OE}$ Set-Up Time	tOES	2		µs	
VPP Set-Up Time	tVPS	2		µs	
Data Valid from $\overline{OE}$	tOE		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC256 has the following functional modes:

—Operation: The 27HC256 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC256 must be programmed. Both a program and program/verify procedure is available. It can be programmed with Fast or Rapid Pulse algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Operation

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC256's memory data is accessed when

— the chip is enabled by setting the $\overline{CE}$ pin low.
— the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and a program mode is not defined. When these conditions are met, the supply current will drop from 55mA to 100µA on the low power part, and to 35mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming Algorithms

The express algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure1.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A14, and the data is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{CE}$ needs to be under seperate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies ths manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	1	0	0	1	0	1	0	0	94

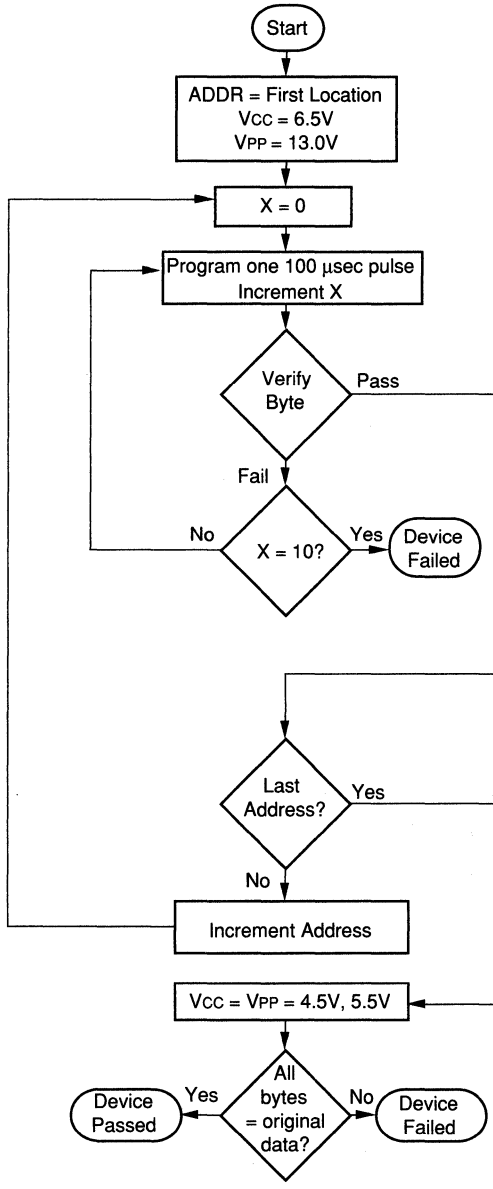
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelenghts ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - Figure 1
Express Algorithm

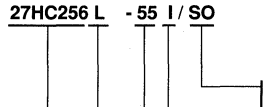
Conditions:
T_{amb} = 25+/-5C
V_{CC} = 6.5+/-0.25V
V_{PP} = 13.0+/-0.25V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing, or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package:	J	Cerdip DIP
	K	Ceramic Leadless Chip Carrier
	L	PLCC
	P	Plastic DIP
	SO	Plastic SOIC
Temperature Range:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to + 125° C
Access Time:	55	55 nsec
	70	70 nsec
	90	90 nsec
Power Type:	-	Standard Power
	L	Low Power
Device:	27HC256	256K (32K x 8) High Speed EPROM

27HC1616

256K (16K x 16) High Speed CMOS UV Erasable PROM

FEATURES

- High speed performance
  —45ns Maximum access time
- CMOS Technology for low power consumption
  —90mA Active current
  —100µA Standby current (low power option)
- OTP (one time programming) available
- WordWide architecture offers space saving over Bytewide memories
- Two programming algorithms allow improved programming times
  —Fast programming
  —Express
- Organized 16K x 16: JEDEC standard pinouts
  —40-Pin dual in line package
  —44-Pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Military**: -55° C to 125° C

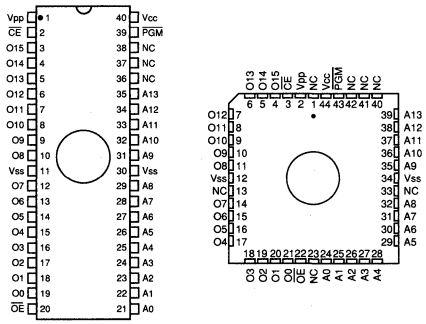
DESCRIPTION

The Microchip Technology Inc. 27HC1616 is a CMOS 256K bit (ultraviolet light) Erasable (electrically) Programmable Read Only Memory. The device is organized as 16K words of 16 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further standby power reduction to 100µA. The 27HC1616 is configured in the JEDEC WordWide pinout which allows a two for one package savings over Bytewide memories along with a significant PC board savings. This very high speed single chip solution is ideal for 16/32 bit digital signal processors (DSP) or other sophisticated microprocessors. A complete family of packages is offered to provide the utmost flexibility. One Time Programming (OTP) is available for low cost (plastic) applications.

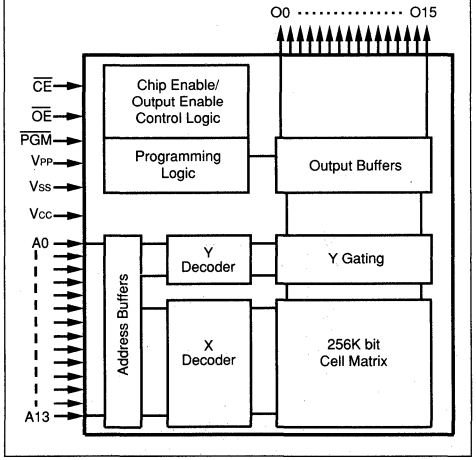
3

PIN CONFIGURATION

Top View



BLOCK DIAGRAM



** See 27HC1616 Military Data sheet DS60038

PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V
Temperature under bias .....-65°C to 125° C
Storage temperature .....-65°C to 150° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2mA IOL = 8mA
Output Leakage	all		ILO	-10	10	µA	VOUT = -0.1 to VCC + 1.0V
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	all	TTL input	ICC1		90	mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S,SX		ICC(S)1		50	mA	
Power Supply Current, Standby	L, LX L, LX	TTL input CMOS input	ICC(S)2		3 100	mA µA	$\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2MHz: 2mA/MHz.
(2) VCC must be applied simultaneously or before VPP and be removed simultaneously or after VPP.

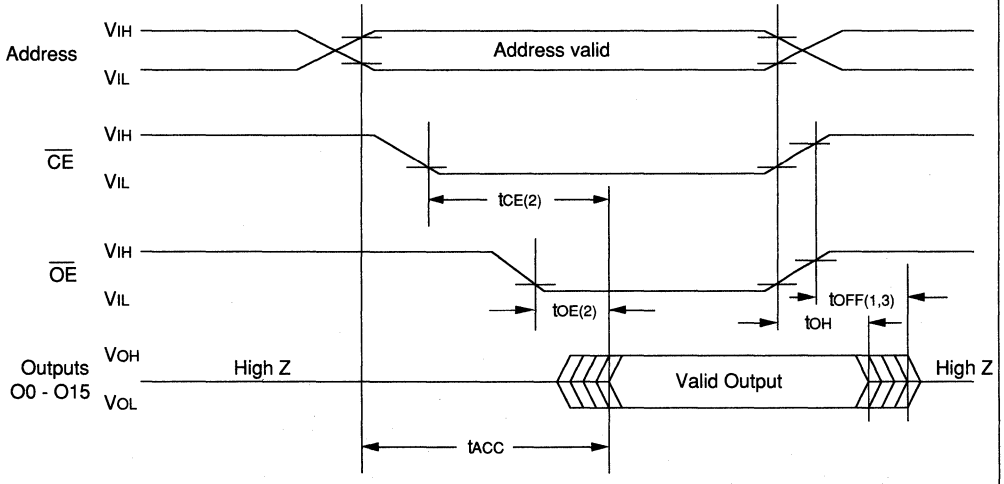
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0 V and V_{IL} = 0.0 V; V_{OH} = V_{OL} = 1.5 V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Sym	27HC1616-45		27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		45		55		70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}		45 30		55 35		70 45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}		25		30		35	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	all	t_{OH}	0		0		0		ns	

* Parts: S = Standard Power; L = Low Power

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

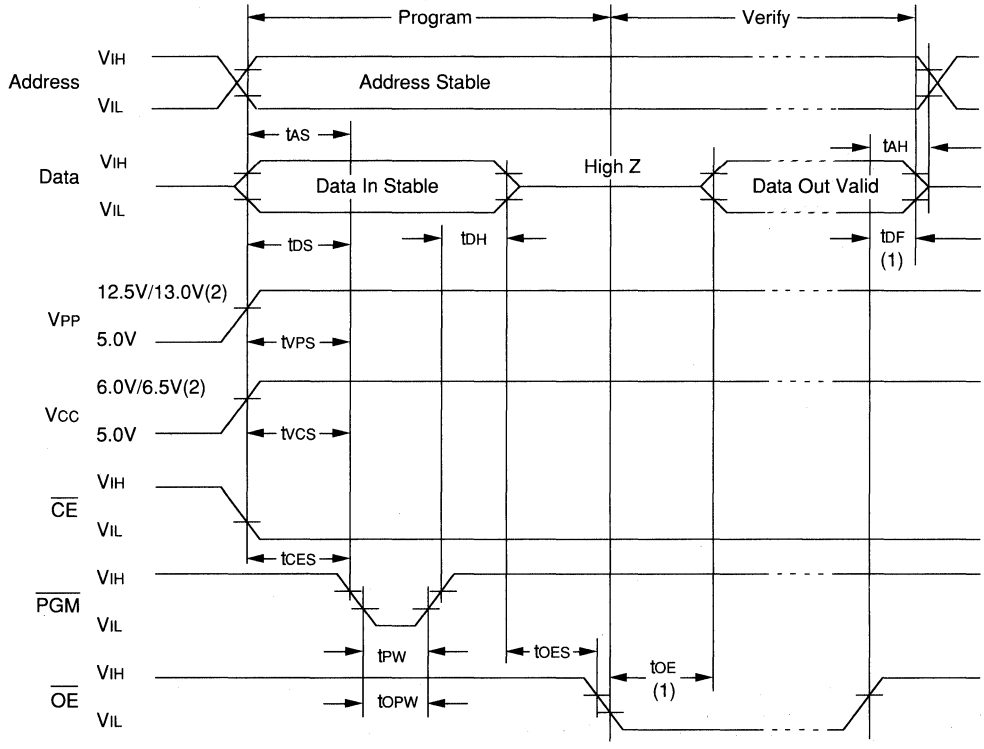
PROGRAMMING DC Characteristics	Ambient Temperature: 25° C ±5° C For V_{PP} and V_{CC} Voltages refer to Programming Algorithms					
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = -.1V to V_{CC} + 1.0V
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 2mA I_{OL} = 8mA
V_{CC} Current, program & verify		I_{CC}		90	mA	Note 1
V_{PP} Current,program		I_{PP}		50	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V and V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Ambient Temperature: 25° C ±5° C For V_{PP} and V_{CC} Voltages, refer to Programming Algorithms				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Overprogram Pulse Width (2)	t_{OPW}	2.85	78.75	ms	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.0V ±0.25V, V_{PP} = V_H = 12.5V ±0.5V for fast programming algorithm
V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

—Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. It can be programmed with Fast or Express algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O15
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{out}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{in}
Program Verify	V_{IH}	V_{IL}	V_{IH}	V_H	X	D_{out}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care
V_H = 12.0 ±0.5V

OPERATION

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

—the chip is enabled by setting the $\overline{CE}$ pin low.
—the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90mA to 100µA on the low power part, and to 50mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithms

Two programming algorithms are available: fast programming and express.

The fast programming algorithm is the industry standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the algorithm is shown in Figure 1.

The express algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ pin is pulsed low.

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin ⟶	Input	Output*								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

*Code subject to change.
Note: O15 - O8 are 00 for the manufacturer and device type code.

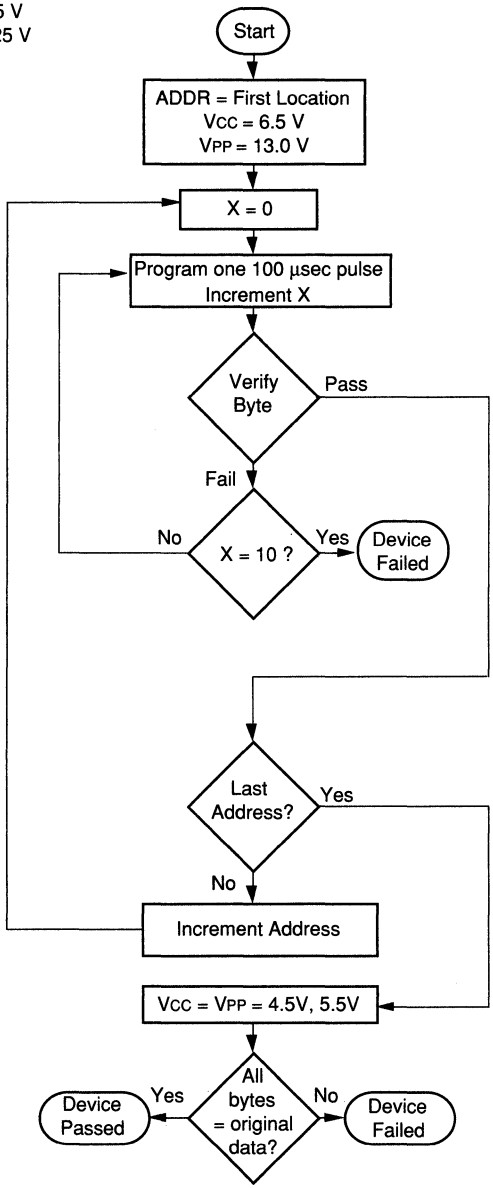
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

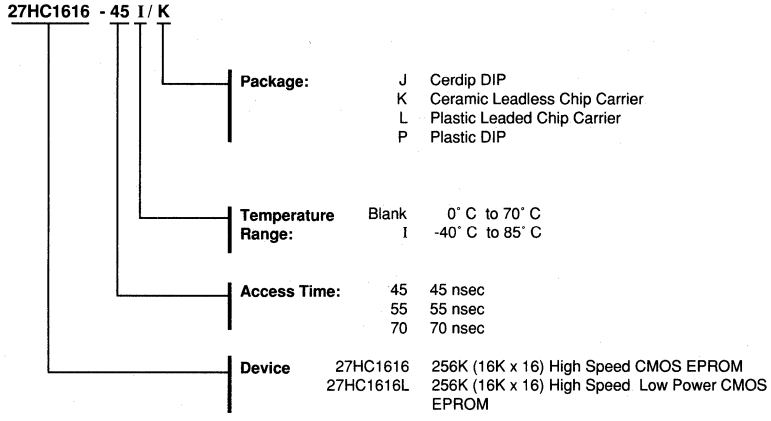
Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25 V
V_{PP} = 13.0 ±0.25 V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



27HC641

64K (8K x 8) High Speed CMOS UV Erasable PROM

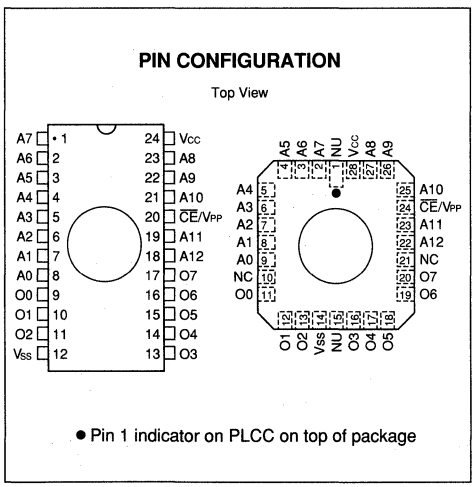
FEATURES

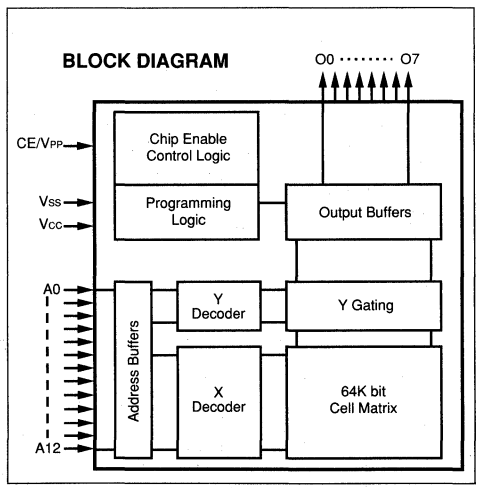
- Bipolar Performance
  - — 40ns Maximum Access Time
- CMOS Technology For Low Power Consumption
  - — 80mA Active Current
  - — 100µA Standby Current (Low Power Option)
- OTP (One Time Programming) Available
- Auto-Insertion-Compatible Plastic Packages
- Auto ID™ Aids Automated Programming
- Two Programming Algorithms Allow Improved Programming Times
  - — Fast Programming
  - — Express
- Organized 8K x 8: Bipolar PROM Pinouts
  - — 24 Pin Dual in Line Package
  - — 28 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - — Commercial: 0° C to 70° C
  - — Industrial: -40° C to 85° C
  - — Military**: -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27HC641 is a CMOS 64K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design allows bipolar speed with a significant reduction in power over bipolar PROMs. A low power option (L) allows further standby power reduction to 100µA. The 27HC641 is configured in a standard 64K bipolar PROM pinout, which allows an easy upgrade for PROM sockets. This very high speed device allows digital signal processors (DSP) or other sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the utmost flexibility in applications. Skinny Cerdip (300 mil) and Skinny Plastic are available. One Time Programming (OTP) is available for low cost (plastic) applications.





**See 27HC641 Military Data Sheet DS60007A

PIN FUNCTION TABLE	
Name	**Function**
$\overline{A0}$ - A12	Address Inputs
$\overline{CE}$/VPP	Chip Enable/VPP Pin
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to + 7.25V
$\overline{CE}$/VPP voltage w.r.t. VSS during programming ..... -0.6V to + 14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC+1.0V
Storage temperature ..... -65° C to 150° C
Ambient temperature with power applied ..... -65° C to 125° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 4mA IOL = 16mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25°C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT= 0V;Tamb = 25°C; f = 1MHz
Power Suppy Current, Active	S,L SX,LX	TTL input TTL input	ICC1 ICC2		80 90	mA mA	VCC = 5.5V; $\overline{CE}$/VPP = VIL f = 2MHz; Iout = 0mA; VIL = -0.1V to 0.8 V; VIH = 2.0V to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		40 50	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	 $\overline{CE}$/VPP = VCC ±0.2V

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2 MHz: 3mA/MHz for standard part; 5 mA/MHz for industrial temperature range part.

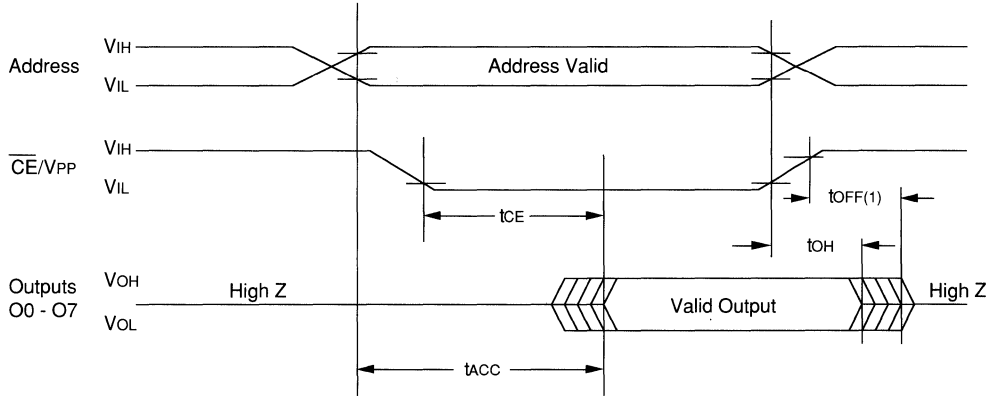
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Part*	Sym	27HC641-40**		27HC641-45		27HC641-55		27HC641-70		Units	Conditions
			Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		40		45		55		70	ns	
$\overline{CE}/V_{PP}$ to Output Delay	L S	t_{CE1} t_{CE2}		40 30		45 35		55 35		70 45	ns	
$\overline{CE}/V_{PP}$ to O/P High Impedance	all	t_{OFF}	0	25	0	25	0	30	0	35	ns	
Output Hold from Address or $\overline{CE}/V_{PP}$, whichever goes first	all	t_{OH}	0		0		0		0		ns	

* Parts: S = Standard Power; L = Low Power
** 27HC641-40 is only available in commercial temperature range

READ WAVEFORMS



Note: (1) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
For $\overline{CE}$/V_{PP} and V_{CC} Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = OV to V_{CC}
Output Voltages during verification	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4mA I_{OL} = 16mA
V_{CC} Current, program & verify		I_{CC}		80	mA	
V_{PP} Current, program		I_{PP}		40	mA	
A9 Product Identification		V_H	11.5	12.5	V	

PROGRAMMING
AC Characteristics

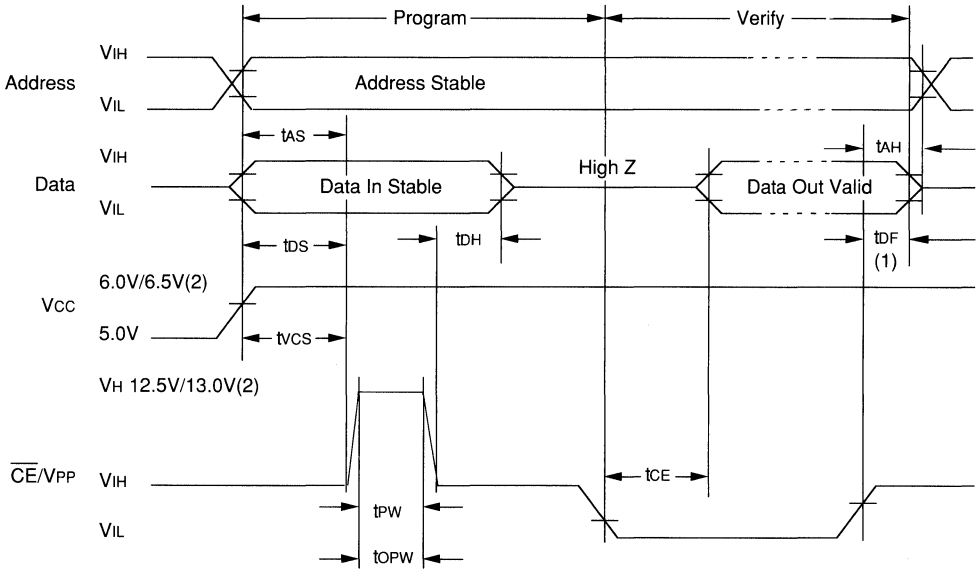
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
For $\overline{CE}$/V_{PP} and V_{CC} Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
Overprogram Pulse Width (2)	t_{OPW}	2.85	78.75	ms	
$\overline{CE}$ to Output Delay	t_{CE}		100	ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING Waveforms



Notes: (1) tDF is a characteristics of the device but must be accomodated by the programmer
(2) VCC = 6.0V ±0.25V, CE/VPP = VH=12.5V ±0.5V for fast programming algorithm
VCC = 6.5V ±0.25V, CE/VPP = VH=13.0V ±0.25V Express programming algorithm

MODES

Operating Modes	CE/VPP	A9	O0 - O7
Read/Program Verify	VIL	X	DOUT
Program	VH	X	DIN
Standby/Program Inhibit	VIH	X	High Z
Identify	VIL	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

the CE/VPP pin is low to power up (enable) the chip

For Read operations on the low powered version, if the addresses are stable, the address access time (tACC) is equal to the delay from CE/VPP to output (tCE). A faster CE/VPP access time (tCE) is available on the standard part to provide the additional time for decoding for the CE/VPP signal.

Standby Mode

The standby mode is defined when the $\overline{CE}/V_{PP}$ pin is high (V_{IH}).

When this condition is met, the supply current will drop from 80mA to 100µA on the low power part and to 40mA on the standard part.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"'s state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the Express algorithm is shown in Figure 2.

The $\overline{CE}/V_{PP}$ is a multifunction pin that controls the programming of the 27HC641.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) the $\overline{CE}/V_{PP}$ pin is pulsed at the proper V_H level.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A12 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a high voltage pulse (V_H) on the $\overline{CE}/V_{PP}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) the $\overline{CE}/V_{PP}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}/V_{PP}$ needs to be under separate control to each device. By pulsing the $\overline{CE}/V_{PP}$ line to a V_H on a particular device, that device will be programmed; all other devices with $\overline{CE}/V_{PP}$ held high (V_{IH}) will not be programmed with the data, although address and data will be available on their input pins (i.e., when a level (V_{IH}) is present on $\overline{CE}/V_{PP}$) and the device is inhibited from programming.

Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc., and the device type. This mode is entered when Pin A9 is taken to V_H (11.5V - 12.5V).

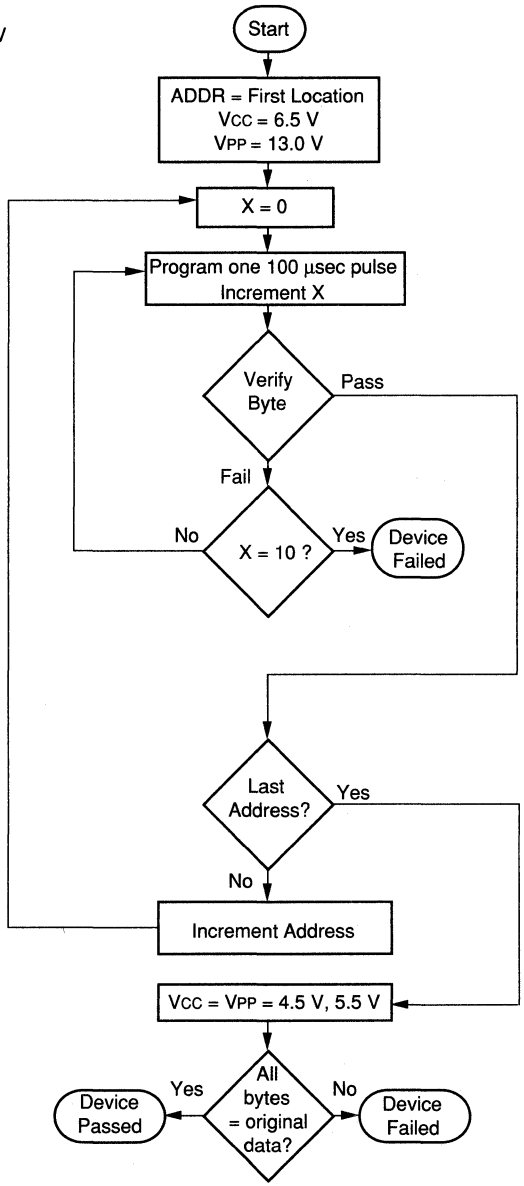
The $\overline{CE}/V_{PP}$ line must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	0	0	0	1	0	0	0	0	10

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25 V
V_{PP} = 13.0 ±0.25 V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC641 - 45 I / K

Package:		J	Cerdip DIP
		K	Ceramic Leadless Chip Carrier
		L	Plastic Leaded Chip Carrier (OTP Available)
		P	Plastic DIP (OTP Available)
		SJ	SKINNY CERDIP
		SP	SKINNY PLASTIC (OTP Available)
Temperature Range:		Blank	0° C to 70° C
		I	-40° C to 85° C
Access Time:		40	40 nsec
		45	55 nsec
		55	55 nsec
		70	70 nsec
Device:	27HC641		64K (8K x 8) High Speed CMOS EPROM
	27HC641L		64K (8K x 8) High Speed Low Power CMOS EPROM

27Cxxx EPROM FAMILY PROGRAMMING ALGORITHM

Overview

Microchip Technology Inc supports three programming algorithms for its CMOS EPROM Family. The selection of an algorithm is an important consideration and will impact the programming time, programming yield and programming margins of the EPROM.

Fast Programming Algorithm

This is the old industry standard programming algorithm with up to 25 1-msec programming pulses and a three times overprogramming pulse. It is a very stable algorithm to use, with its major draw back being an increase in throughput time especially at the larger densities.

Rapid Pulse Programming Algorithm

The Rapid Pulse algorithm provides an alternative to the Fast algorithm. The slight increase in V_{CC} and V_{PP} during programming allows the use of a narrower 100 usec programming pulse and the removal of the overprogramming pulse associated with the Fast Programming. This translates into a decrease in programming times of nearly 40 to 1 and an increase in throughput of nearly 10 to 1. (Throughput is heavily influenced by the machine cycle time of the programmer during the pre-programming blank check, and the post-programming verification. It also varies from programmer to programmer.)

Express Programming Algorithm

The Express algorithm is an improvement on the Rapid Pulse algorithm. While it exhibits the same excellent throughput as the Rapid Pulse algorithm, its advantage lies in the additional increase in V_{PP} and V_{CC} applied during programming. The higher V_{PP} and V_{CC} voltages provide additional charge to the floating gate during programming. After each programming pulse, the cell is verified against V_{CC} (6.5 Volts for Express, 6.25 volts for Rapid Pulse). This verification step with a higher V_{CC} ensures improvement in programming margins over the Rapid Pulse algorithm.

Algorithm Selection

The optimization of programmer throughput is a concern to all EPROM users in a production environment. A major contributor to increasing throughput is shorter programming times. The Express algorithm has been developed to minimize programming times. In addition, sufficient programming margins must be developed to insure EPROM functionality over the full range of voltage and temperature variations. The higher Vcc and Vpp voltages generate this increased margin and provide additional guardband against the effects of aging hardware.

Programming Times (sec)			
Memory Size	**Fast**	**Rapid**	**Express**
64K	32.8	0.819	0.819
128K	131.1	1.64	1.64
256K	93/32	3.28	3.28
512K	262.2	6.55	6.55

Note: Actual throughput time depends on the machine cycle time of the programmer during pre-programming blank check, and the post-programming verification.

Microchip Programming Algorithm Recommendations

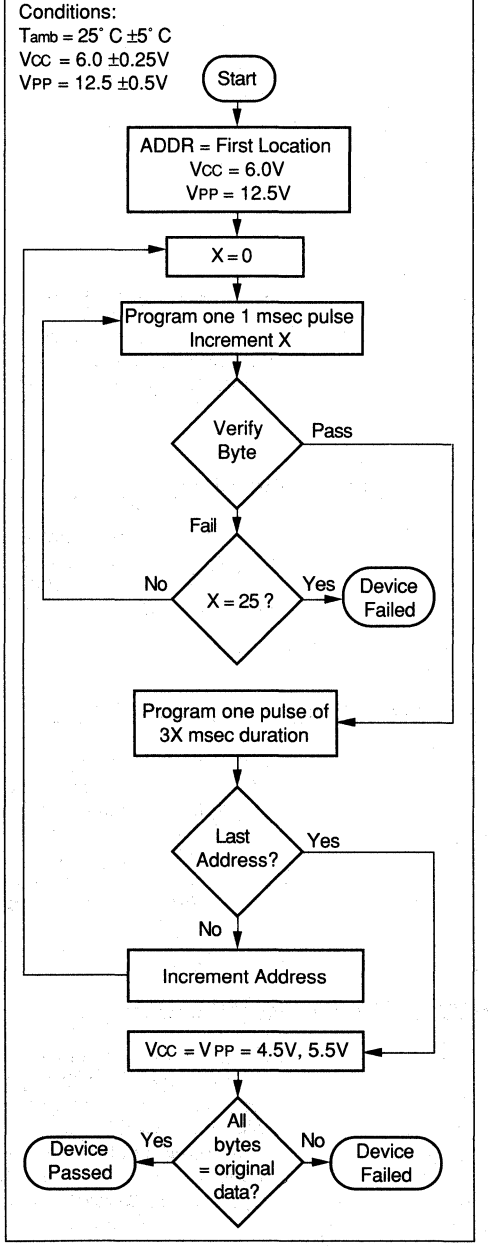
Microchip recommends that the Express algorithm be used on all commercial/industrial EPROMs (when available).

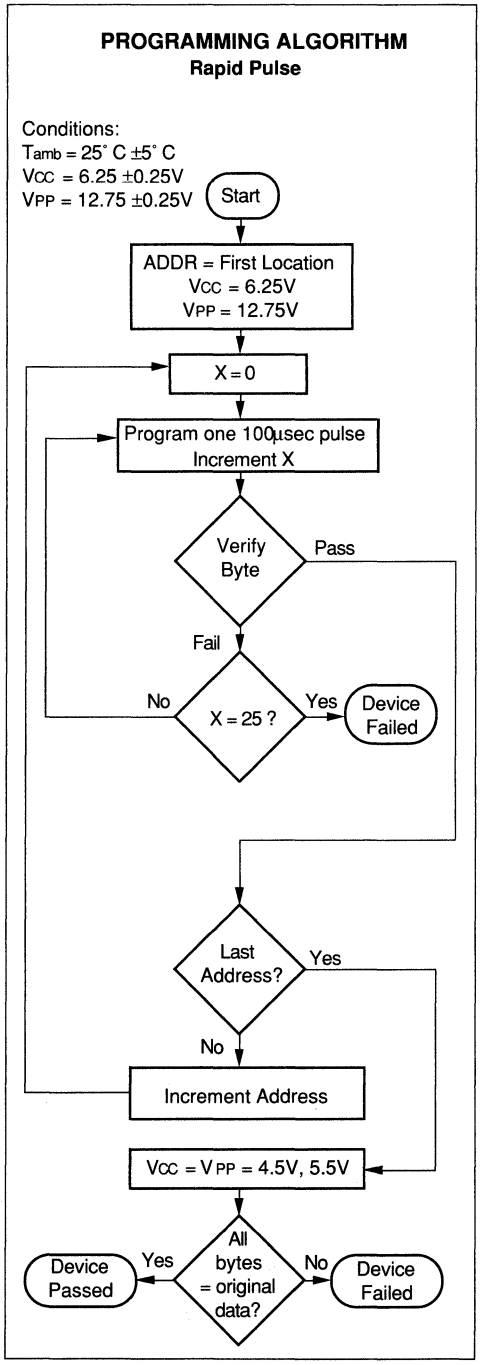
The Fast Programming algorithm should be your second choice for the 64K and the 128K EPROMs, with Rapid Pulse being the second choice for the 256K and 512K EPROMs. The remaining algorithm should be your third choice. This recommendation is based on the maximization of programmer throughput and cell margins. At the smaller density (when Express is not available) the increased margins supplied by the Fast Programming far outweigh the small increase in throughput of Rapid Pulse. As you increase density, programming throughput becomes the dominant criteria.

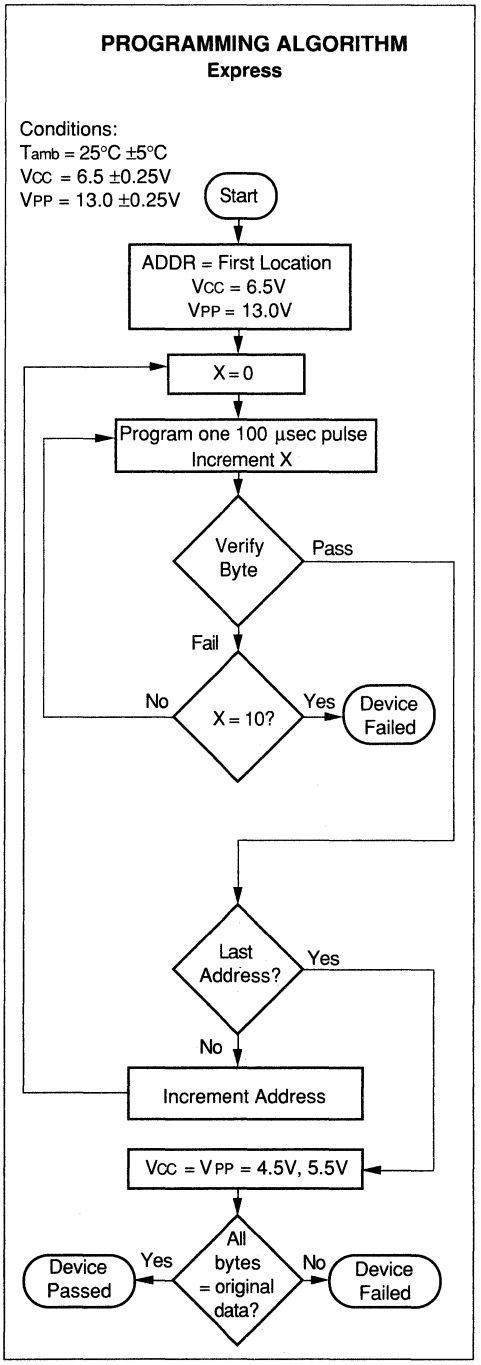
Data I/O Family Code and Pin-Outs*				
Device	**Size**	**Fast**	**Rapid**	**Express**
27C64	64K	93/33	5C/33	115/033
27C128	128K	93/51	5C/51	115/051
27C256	256K	93/32	5C/32	115/032
27C512	512K	4B/A4	5E/A4	116/0A4

* DIP Packages

PROGRAMMING ALGORITHM
Fast Algorithm




PROGRAMMING ALGORITHM
Rapid Pulse
Conditions:
Tamb = 25° C ±5° C
VCC = 6.25 ±0.25V
VPP = 12.75 ±0.25V
Start
ADDR = First Location
VCC = 6.25V
VPP = 12.75V
X = 0
Program one 100µsec pulse
Increment X
Verify Byte
Pass
Fail
No
X = 25 ?
Yes
Device Failed
Last Address?
Yes
No
Increment Address
VCC = VPP = 4.5V, 5.5V
All bytes = original data?
Yes
Device Passed
No
Device Failed


PROGRAMMING ALGORITHM
Express
Conditions:
Tamb = 25°C ±5°C
VCC = 6.5 ±0.25V
VPP = 13.0 ±0.25V
Start
ADDR = First Location
VCC = 6.5V
VPP = 13.0V
X = 0
Program one 100 µsec pulse
Increment X
Verify Byte
Pass
Fail
No
X = 10?
Yes
Device Failed
Last Address?
Yes
No
Increment Address
VCC = VPP = 4.5V, 5.5V
All bytes = original data?
Yes
Device Passed
No
Device Failed

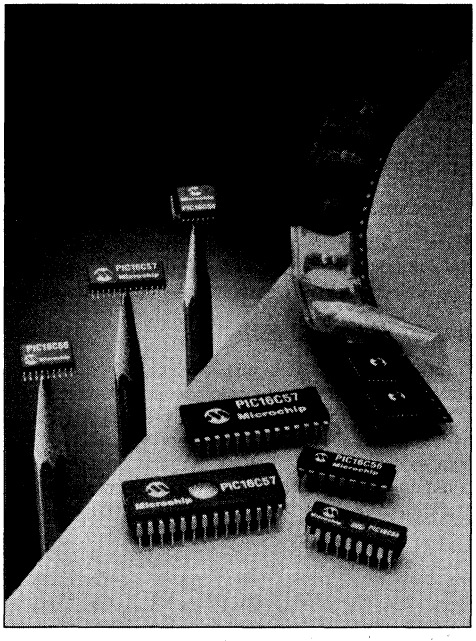
NOTES:

SECTION 4
MICROCONTROLLER PRODUCT SPECIFICATIONS

Microchip

PIC® 16XXX SERIES

PIC 16xxx Series Microcontroller Family



THE PIC FAMILY

A History of Innovation and Success

Microchip's history of innovation and its strong commitment to develop and market leading edge products, is best exemplified by its popular 8-Bit Microcontroller families. Microchip is the first semiconductor company to introduce RISC-like features and offer the time saving flexibility of one-time-programmable (OTP) EPROM 8-Bit MCUs. These new design concepts and the integration of advanced CMOS EPROM technology overcomes three major user barriers, namely: efficiency/performance; time to market; and affordability. The benefits of PIC® microcontroller technology are being shared by hundreds of customers worldwide with over 80 million CMOS and NMOS PIC microcontrollers in use.

FEATURES

PIC EPROM Technology

PIC's OTP EPROM technology offers a low cost alternative to using competitive ROM based devices for high volume production. EPROM technology also offers several important cost saving advantages namely:

Time-To-Market: Since the financial success of a product is often determined by its time-to-market, through user programmability PIC offers an immediate solution to lengthy market entry delays. Our off-the shelf products eliminate the 10-18 week lead times experienced with conventional ROM based MCU suppliers.

EPROM Flexibility: Means decisions to change codes "on-the-fly" while in development or in mid-production no longer carry a financial or time penalty in the event of error. System performance enhancements which may be critical to market success can now be achieved quickly, effortlessly and cost effectively. Another demonstration of EPROM flexibility is the ability to perform in-circuit-programming. This allows for product variants to be developed cost effectively. Participation in high profit custom business becomes economically feasible with OTP PICs.

Off-The-Shelf: EPROM technology benefits the user by eliminating the need for substantial inventories and limits exposure to product obsolescence; typical of ROM devices. OTP parts also ensure an immediate supply from a variety of worldwide stocking locations. High volume quick-turn-production (QTP) programming services are also available from Microchip for customers who chose not to perform high volume programming themselves.

PIC's RISC Architecture

PIC's RISC Architecture sets a new standard in performance in the 8-Bit MCU marketplace. The highly efficient and powerful instruction set which supports this architecture requires only 33 single cycle instructions to learn versus 60 to 110 multi-byte instructions common to competitive CISC MCU architectures. Benchmarks have demonstrated that the efficiency of this instruction set provides the user with **up to a 2:1 code compaction advantage over competitive products.** It has also been demonstrated that this level of efficiency can also **reduce code development time by up to 30 percent.**

PIC® is a registered trademark of Microchip Technology Inc.

The PIC's single cycle instructions and RISC architecture facilitates up to five million instructions per second execution throughput. This provides the designer with up to a 5:1 speed advantage over competitive products. This advanced rate of code execution rivals many 16-Bit MCU designs and opens new real-time, high performance application opportunities. Also, memory inefficient, engineering intensive and inaccurate look-up tables can now be replaced with PIC's high level algorithmic processing speed. Applications such as efficient motor control, high speed I/O and high speed data bit stream manipulation now becomes a reality in the 8-Bit domain.

A new design concept of user definable oscillators allows the chip to execute instructions in four speed ranges from DC to 200ns.

PIC's CMOS Design

The PIC employs a fully static CMOS design allowing for reliable low power operation. PIC incorporates on-chip POR and Watchdog Timer circuitry thus eliminating expensive off-chip support components.

Bit manipulation is one of PIC's strongest suits. The designer can now utilize very powerful bit manipulation instructions capable of setting, clearing and testing any bit in any register (including I/O registers) in one instruction cycle. This allows the PIC to efficiently interface to external circuitry and be used as a powerful I/O controller. The I/O is software definable bi-directional. Under software control, each pin of a port can be individually time multiplexed between input and output or can be programmed into a high impedance state thus supporting multi-chip common bus configurations.

The PIC's small die size and Microchip's advanced CMOS technology support a wide performance range but also allow low operating and standby current. These low currents will make long-life battery dependent projects possible.

PIC's Small Packaging

Microchip has also engineered the world's smallest 8-bit microcontroller package. For highly integrated designs, 300 mil. wide 18 pin PDIP, SOIC and PLCC surface mount packages are available. Tape and reel packaging is also offered for automatic high speed surface mount placement.

PIC Temperature Ranges

The PIC16C5X family is currently available in commercial and industrial temperatures. There are plans to offer this family in automotive and military temperatures.

Upward Migration Path

Future CMOS PIC generations will provide a family of products with embedded analog capabilities, additional I/O, sophisticated timers, increased memory and industry leading CPU power. The capability to address off-chip extended RAM/EPROM memory and inter-chip communication is currently under development.

PIC FAMILY PRODUCT GUIDE

High Performance CMOS Microcontrollers...

where performance and power efficiency is prime consideration.

PIC16C5X CMOS MICROCONTROLLER

Part Number	Pins	I/O	RAM	ROM	EPROM	Oscillator Range	Min.Instr.Cycle	Available
PIC16C54	18	12	32 x 8	-	512 x 12	25kHz-20MHz	200ns	NOW
PIC16C55	28	20	32 x 8	-	512 x 12	25kHz-20MHz	200ns	NOW
PIC16C56	18	12	32 x 8	-	1024 x 12	25kHz-20MHz	200ns	NOW
PIC16C57	28	20	80 x 8	-	2048 x 12	25kHz-20MHz	200ns	NOW

Low-Cost NMOS Microcontrollers...

for highly cost sensitive applications where the superior performance of the PIC16C5X series is not required.

PIC16XXX NMOS MICROCONTROLLER

Part Number	Pins	I/O	RAM	ROM	EPROM	Oscillator Range	Min.Instr.Cycle	Available
PIC1654S	18	12	32 x 8	512 x 12	-	-	2µs	NOW
PIC1655	28	20	32 x 8	512 x 12	-	-	4µs	NOW
PIC1670	40	32	64 x 8	1024 x 13	-	-	2µs	NOW

PC-HOSTED SYSTEMS SIMPLIFY SOFTWARE DEVELOPMENT

Two advanced PC-hosted systems, the PIC-ICE™ and PIC PAK™, are available to help users develop applications software and program PIC16C5X devices quickly and easily. Both operate with IBM PC, XT, AT, or compatibles.

PIC-ICE

The PIC-ICE system provides low-cost in-circuit emulation and debugging and includes an 18-pin and 28-pin EPROM PIC programmer. This low profile module has a handy carrying case and comes with an external power supply, ribbon cabling, cross assembler, PIC16C5X EPROM product samples and a users manual. Key features include a DC to 20MHz operating range, a built-in disassembler, breakpoints and a symbolic debugger.

PIC PAK

The PIC PAK (PIC Applications Kit) is a powerful yet low-cost software development tool that combines assembler and simulator software to compile, execute, debug and analyze microcode in a non-real time environment. An EPROM PIC programmer (PIC PRO) and PIC16C5X EPROM product samples are included for code verification.

PICALC Cross Assembler

The PIC Cross Assembler PICALC is available for several host computer platforms, including IBM PC. Macro assembly and conditional assembly are just a few of the capabilities of PICALC. Besides the PIC16C5x and PIC167x family members. PICALC can generate various object code formats to support Microchip's proprietary development tools as well as third party systems.

PICSIM Software Simulator

The software simulator PICSIM allows PIC16C5x code development on IBM PCs without any additional hardware. It simulates the PIC16C5x series on instruction level. Software trace, break-points, symbolic debugging, and stimulus file generation are just a few of the features available. PICSIM is particularly useful in the early development stages of an application, or when real-time and/or in-circuit emulation are not necessary for the code development.

PICPRO EPROM Programmer

PICPRO is a low volume EPROM programmer for the PIC16C5x series. It allows downloading and programming of PIC object code generated with PICALC from any host computer system providing a serial interface (RS232).

QUALITY FROM THE TOP DOWN AND THE BOTTOM UP

Microchip's sole ownership of its facilities ensures our quality control standards remain consistent throughout all manufacturing steps. Continuous improvement programs are active at every operations level. Equipment for simulation, product testing and failure analysis is constantly updated to the most current levels of sophistication. Our customer support reaches out to the point when a customer ships his product.

To ensure product quality, Microchip conducts accelerated mechanical tests, temperature tests and memory retention tests to explore the many ways failures might occur. Stresses carefully applied over time, guarantee the effective operation of Microchip products. Comprehensive 1,000-hour qualification tests such as high temperature reverse bias, high temperature retention bake, latchup tests and operating life provide precise quality and reliability data. An electrostatic discharge sensitivity test is also conducted in accordance with MIL-STD 883-C, method 5005.

Microchip PIC microcontrollers have demonstrated their reliability in several demanding applications such as high noise, high temperature under-hood automotive applications, NASA space shuttle missions and missile safe-arm fuse control.

CMOS PIC16C5X MICROCONTROLLER RELIABILITY DATA (Failures/Sample Size)

TEST: 125°C DYNAMIC LIFE

24HR.	168 HR.	500 HR.	1000 HR.	Fits
4/2344	5/2340	0/2331	1/2331	**117 Fits**

TEST: 150°C HIGH TEMPERATURE REVERSE BIAS

0/162	0/162	0/162	0/162	**16 Fits**

TEST: 150°C RETENTION EPROM BAKE

0/1710	1/1710	1/1709	3/1708	**31 Fits**

Failure analysis available upon request.

EXACTING SOLUTIONS FOR DEMANDING APPLICATIONS.....

Smallest Packaging

For highly integrated insertion or surface mount modules, Microchip produces the smallest microcontroller devices in the world. An 18 pin DIP, SOIC or PLCC package makes space limited applications a design reality, such as:

- Handheld devices
- Automotive modules
- Small PC peripherals
- Consumer products

For even further integration, PIC's in dice form will also be available for Hybrid or COB packaging.

Fastest Operating Speed

For "High Performance" applications, the PIC's 5 million instruction per second architecture offers a very unique solution. With PIC, system designers are now able to replace inaccurate predetermined look-up table values with high precision, real time, algorithmic processing.

PIC can solve several real-time problems often found in designs of:

- Disk Drives
- Pointing Devices/Scanners
- Motor/Compressor Controls
- I/O Processors
- "Glue" Logic Replacement

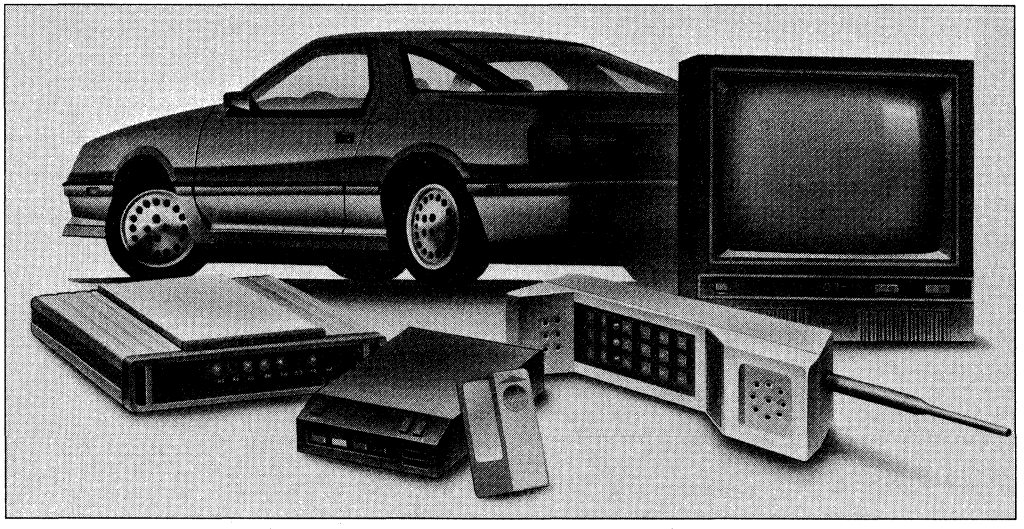
Lowest Power Consumption

The PIC16C5X families possess one of the lowest standby and operating currents in the industry, opening new design opportunities for battery, solar and remotely powered applications, such as

- Cordless Telephones
- Mobile Telephones
- Automobile Electronic Locks
- Secure Access Remote Control
- Consumer Remote Controls
- Remote Smart Sensors
- Cordless Radar Detectors

A GLOBAL COMMITMENT TO CUSTOMER SUPPORT

Microchip's commitment to microcontroller breakthrough technology is superseded only by our attention to customer support. Through a worldwide network of manufacturing facilities, sales offices and field applications support, Microchip delivers total customer service worldwide.



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PIC®16C5x Series

EPROM-Based 8-Bit CMOS Microcontroller Series

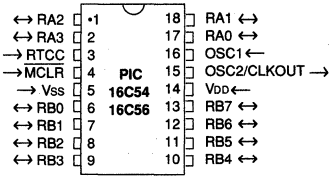
FEATURES

- Low power, high speed CMOS EPROM technology
- Wide variety of EPROM and RAM sizes, oscillator types, frequency ranges and I/O configurations
- Fully static chip design
- Operating Frequency Range:
  - DC - 8 MHz (20 MHz future release)
- Operating voltage range:
  - Standard: 4.0V to 5.5V
- Low power consumption:
  - < 2 mA (4 MHz, 5V, XTAL oscillator)
  - <10 μA standby
- Available in temp ranges:
  - Commercial = 0°C to +70°C
  - Industrial = -40°C to +85°C
- Wide selection of 18 and 28 lead packaging options: PDIP, SOIC, PLCC, or CERDIP Window
- 512 to 2048 words of 12-bit program EPROM
- 32 to 80 words of 8-bit data RAM
- Only 33 single 12-bit-word instructions to learn
- 8 bit ALU
- 12 or 20 bidirectional tristate I/O's
- 2 level stack for subroutine nesting
- Direct, indirect, immediate, and relative addressing modes for data and instructions
- 8 bit real time clock/counter (RTCC) with selectable signal source and trigger edge
- Free running on-chip watchdog timer
- 8 bit prescaler, assignable to RTCC or watchdog timer
- Oscillator start up timer
- Security EPROM fuse for code protection
- QTP (factory programming) available

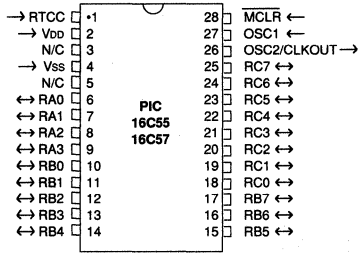
4

FIGURE 1: PIN CONFIGURATIONS

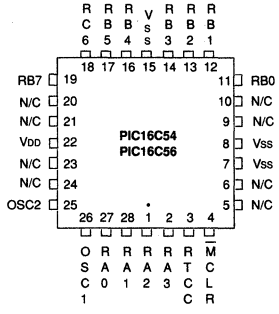
PDIP, SOIC
CERDIP Window



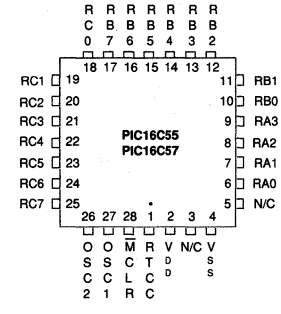
PDIP, SOIC
CERDIP Window



PLCC



PLCC



GENERAL DESCRIPTION

The Microchip Technology PIC16C5x series is based on the proven architecture of the PIC165x NMOS 8-bit microcontroller family. Using Microchip's low-power, high-speed CMOS EPROM technology, the PIC16C5x offers additional features like on-chip watchdog timer, tristate I/O, power-down mode, and several prescaler options.
The advantages of the user programmable CMOS EPROM technology allow extremely flexible applications, as well as reduced development costs and turn-around time compared to mask programmable ROM versions.

APPLICATIONS

The PIC16C5x series fits perfectly for applications from high speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecom processors. The EPROM technology allows customizing of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low cost, high performance, ease of use, and I/O flexibility make the PIC16C5x series very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

PIN FUNCTION TABLE

Name	Function
RA0 - RA3	I/O PORT A
RB0 - RB7	I/O PORT B
RC0 - RC7	I/O PORT C
RTCC	Real Time Clock/Counter
MCLR	Master Clear
OSC1	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
VSS	Ground
N/C	No (internal) Connection

ARCHITECTURAL DESCRIPTION

HARVARD ARCHITECTURE

The PIC16C5x single-chip microcomputers are low-power, high-speed, full static CMOS devices containing EPROM, RAM, I/O, and a central processing unit on a single chip.

The firmware architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8 bits wide while the program bus and program memory (EPROM) have a width of 12 bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16C5x series is given in Figure 2.

DATA REGISTER FILE

The 8 bit data bus connects two basic functional elements together: the Register File composed of up to 80 addressable 8 bit registers including the I/O Ports, and an 8 bit wide Arithmetic Logic Unit. 32 bytes of RAM are directly addressable while a "banking" scheme, with banks of 16 bytes each, is employed to address larger data memories (Figure 3). Data can be addressed direct, or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.
The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.
In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

ARCHITECTURAL DESCRIPTION (CONT.)

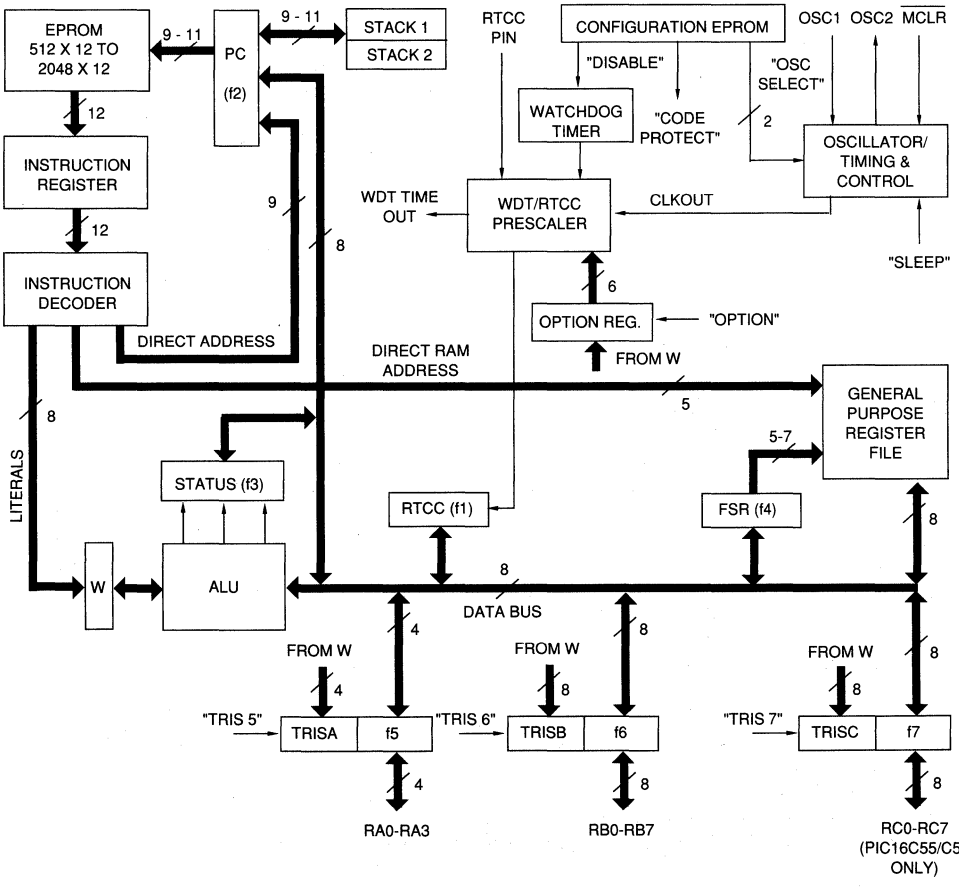
ARITHMETIC/LOGIC UNIT (ALU)

The 8 bit wide ALU contains one temporary working register (W Register) and gating to perform Boolean functions between data held in the W Register and any file register.

PROGRAM MEMORY

Up to 512 words of 12 bit wide on-chip program memory (EPROM) can be directly addressed. Larger program memories can be addressed by selecting one of up to four available pages with 512 words each (Figure 4). Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

FIGURE 2: PIC16C5x SERIES BLOCK DIAGRAM



PIC16C5X SERIES OVERVIEW

A wide variety of EPROM and RAM sizes, number of I/O pins, oscillator types, frequency ranges, and packaging options is available. Depending on application and production requirements the proper device option can be selected using the following information and tables. When placing orders, please use the "PIC16C5x Product Identification System" on page 32 of this data sheet to specify the correct part number.

UV ERASABLE DEVICES

Four different device versions, as listed in Table 1, are available to accommodate the different EPROM, RAM , and I/O configurations. These devices are optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", or "HS". An erased device is configured as "RC" type by default. Depending on the selected oscillator type and frequency, the operating supply voltage must be within the same range as a OTP/QTP part would be specified for.

The PIC development programmer, "PICPRO", can program all members of the PIC16C5x family for prototyping and small-volume production. See page 4-32 for high-volume programming support.

ONE-TIME-PROGRAMMABLE (OTP) DEVICES

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices have the oscillator type pre-configured by the factory, and they are tested only for this special configuration (including voltage and frequency ranges, current consumption). Table 2 below gives an overview about devices available now and planned for future release.

The program EPROM is erased, allowing the user to write his application code into it. In addition, the watchdog timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. The sixteen special EPROM bits for ID code storage are also user programmable.

QUICK-TURNAROUND-PRODUCTION (QTP) DEVICES

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices (see Table 2) but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

TABLE 1: OVERVIEW UV-ERASABLE DEVICES

Part #	EPROM	RAM	I/O**	Supply Voltage	Osc.Freq.Range	Package Options
PIC16C54	512 x 12	32 x 8	13	4.0* - 5.5 V	DC - 8 MHz ***	18 ld. Windowed CERDIP
PIC16C55	512 x 12	32 x 8	21	4.0* - 5.5 V	DC - 8 MHz ***	28 ld. Windowed CERDIP
PIC16C56	1K x 12	32 x 8	13	4.0* - 5.5 V	DC - 8 MHz ***	18 ld. Windowed CERDIP
PIC16C57	2K x 12	80 x 8	21	4.0* - 5.5 V	DC - 8 MHz ***	28 ld. Windowed CERDIP

* Frequencies above 4 MHz and/or operation in the industrial temperature range (-40 to +85°C) require that V_{DD} is greater than 4.75 V.

** Includes RTCC pin

*** Device operation is currently guaranteed up to 8 MHz oscillator frequency.
Please contact Microchip Technology Inc. for expected release dates of 20 MHz devices.

TABLE 2: OVERVIEW OTP AND QTP DEVICES

Part #	EPROM	RAM	I/O*	Supply*** Voltage	Osc. Type	Freq. Range	Package Options (Note)
PIC16C54RC	512 x 12	32 x 8	13	4.0 - 5.5 V	RC	DC - 4 MHz	DIP-18, SOIC-18, PLCC-28
PIC16C54XT	512 x 12	32 x 8	13	4.0 - 5.5 V	XTAL, Ext.	0.4 - 4 MHz	DIP-18, SOIC-18, PLCC-28
PIC16C54HS	512 x 12	32 x 8	13	4.5 - 5.5 V	XTAL, Ext.	4 - 8 MHz **	DIP-18, SOIC-18, PLCC-28
PIC16C55RC	512 x 12	32 x 8	21	4.0 - 5.5 V	RC	DC - 4 MHz	DIP-28, SOIC-28, PLCC-28
PIC16C55XT	512 x 12	32 x 8	21	4.0 - 5.5 V	XTAL, Ext.	0.4 - 4 MHz	DIP-28, SOIC-28, PLCC-28
PIC16C55HS	512 x 12	32 x 8	21	4.5 - 5.5 V	XTAL, Ext.	4 - 8 MHz **	DIP-28, SOIC-28, PLCC-28
PIC16C56RC	1K x 12	32 x 8	13	4.0 - 5.5 V	RC	DC - 4 MHz	DIP-18, SOIC-18, PLCC-28
PIC16C56XT	1K x 12	32 x 8	13	4.0 - 5.5 V	XTAL, Ext.	0.4 - 4 MHz	DIP-18, SOIC-18, PLCC-28
PIC16C56HS	1K x 12	32 x 8	13	4.5 - 5.5 V	XTAL, Ext.	4 - 8 MHz	DIP-18, SOIC-18, PLCC-28
PIC16C57RC	2K x 12	80 x 8	21	4.0 - 5.5 V	RC	DC - 4 MHz	DIP-28, SOIC-28, PLCC-28
PIC16C57XT	2K x 12	80 x 8	21	4.0 - 5.5 V	XTAL, Ext.	0.4 - 4 MHz	DIP-28, SOIC-28, PLCC-28
PIC16C57HS	2K x 12	80 x 8	21	4.5 - 5.5 V	XTAL, Ext.	4 - 8 MHz	DIP-28, SOIC-28, PLCC-28

* Including RTCC pin

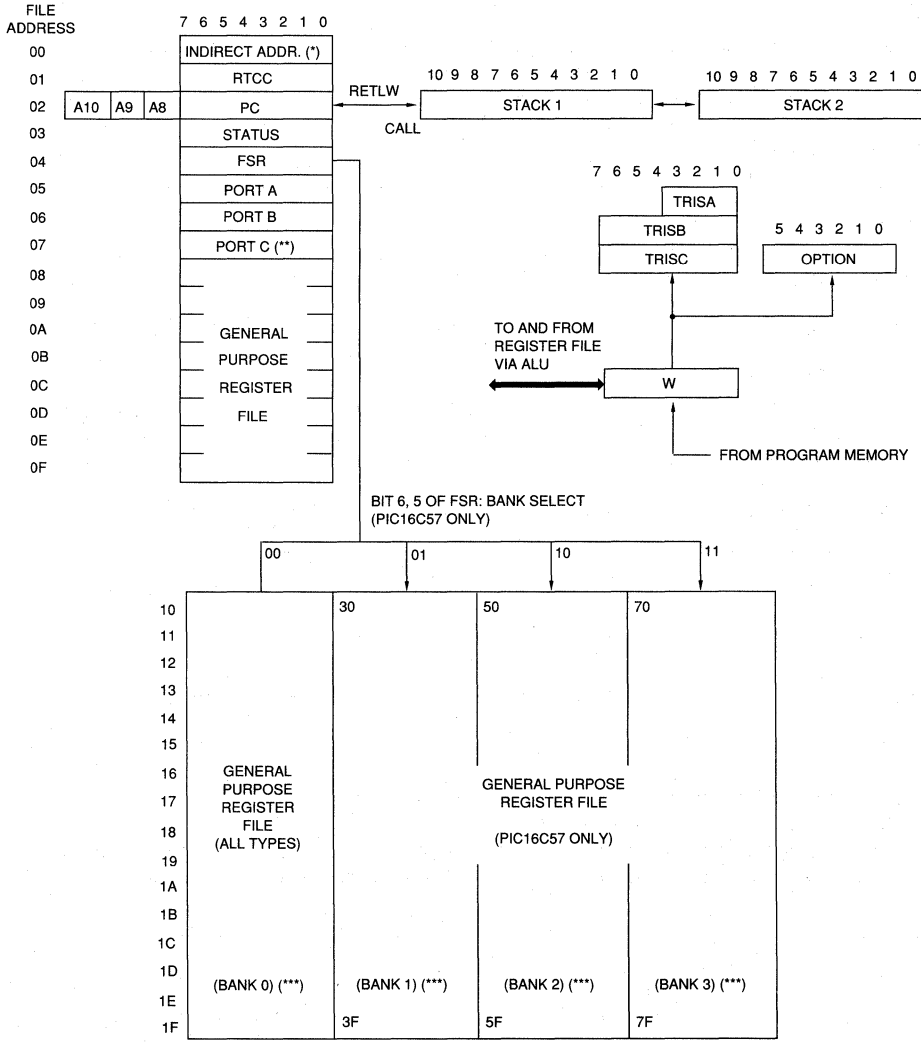
** Device operation is currently guaranteed up to 8 MHz oscillator frequency.
Please contact Microchip Technology for expected release dates of 20 MHz devices.

*** Minimum supply voltage for industrial temperature range is 4.5V for XT and RC, and 4.75V for HS versions.
Devices operating at supply voltages below 4.0V or 4.5V respectively, are under development.

4

REGISTER FILE ARRANGEMENT

FIGURE 3: PIC16C5x DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER. SEE SECTION "OPERATIONAL REGISTER FILES" FOR DETAILS
(**) FILE f7 IS A GENERAL PURPOSE REGISTER ON THE PIC16C54/C56
(***) BANK 0 IS AVAILABLE ON ALL MICROCONTROLLERS WHILE BANK 1 TO BANK 3 ARE ONLY AVAILABLE ON THE PIC16C57. (SEE SECTION "FILE SELECT REGISTER" FOR DETAILS)

OPERATIONAL REGISTER FILES

f0 INDIRECT DATA ADDRESSING

Not a physically implemented register. f0 calls for the contents of the File Select Register to be used to select a file register. f0 is useful as indirect address pointer. For example, the instruction ADDWF f0, W will add the contents of the register pointed to by the FSR (f4) to the content of the W Register and place the result in W .

f1 REAL TIME CLOCK/COUNTER REGISTER (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4).

An 8 bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. If the prescaler is assigned to the RTCC, instructions writing to f1 (e.g. CLRF 1, or BSF1,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if f1 is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. However, the RTCC pin must be tied to VDD or VSS, whatever is convenient, to prevent unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), f1 keeps incrementing and just rolls over when the value "0FF16" is reached. All increment pulses for f1 are delayed by two instruction cycles. After writing to f1, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before f1 is incremented.

OPERATIONAL REGISTER FILES (CONT.)

f2 PROGRAM COUNTER

The program counter generates the addresses for the up to 2048 x 12 on-chip EPROM cells containing the program instruction words (Figure 4).

Depending on the device type, the program counter and its associated two-level hardware stack is 9 - 11 bits wide.

TABLE 3: PROGRAM COUNTER/STACK WIDTH

Part #	PC width	Stack width
PIC16C54/PIC16C55	9 bit	9 bit
PIC16C56	10 bit	10 bit
PIC16C57	11 bit	11 bit

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower 9 program counter bits.
b) "CALL" instructions load the lower 8 bit of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack.
c) "RETLW" instructions load the program counter with the top of stack contents.
d) "MOVWF 2" allows the loading of computed addresses from the W register into the program counter.
e) "ADDWF 2" allows adding of relative addresses to the current PC contents. In this case the PC will also be incremented. That is, adding "000" to f2 results in the PC value PC + 1.

In the cases d) and e), the ninth bit of the PC will always be cleared to "0". Thus, indexed addressing is only possible within the lower half of a program memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF).

Program Memory Page Select (PIC16C56/ PIC16C57 Only):

The most significant program counter bit(s) will be loaded with the contents of the page preselect bits in the status register f3 upon execution of a "GOTO", "CALL", "ADDWF 2", or "MOVWF 2" instruction.

Incrementing the program counter when it is pointing to the last address of a selected memory page is also possible and will cause the program to continue in the next higher page. However, the page pre-select bits in f3 will not be changed, and the next "GOTO", "CALL", "ADDWF 2", "MOVWF 2" instruction will return to the previous page, unless the page pre-select bits have been updated under program control. For example, a "NOP" at location "1FF"(page 0) increments the PC to "200" (page 1). A "GOTO xxx" at "200" will return the program to address "xxx" on page "0" (assuming that the page preselect bits in f3 are "0".
Upon a RESET condition, page 0 is pre-selected while the program counter addresses the last location in the last page. Thus, a "GOTO" instruction at this location will automatically cause the program to continue in page 0.

Stack

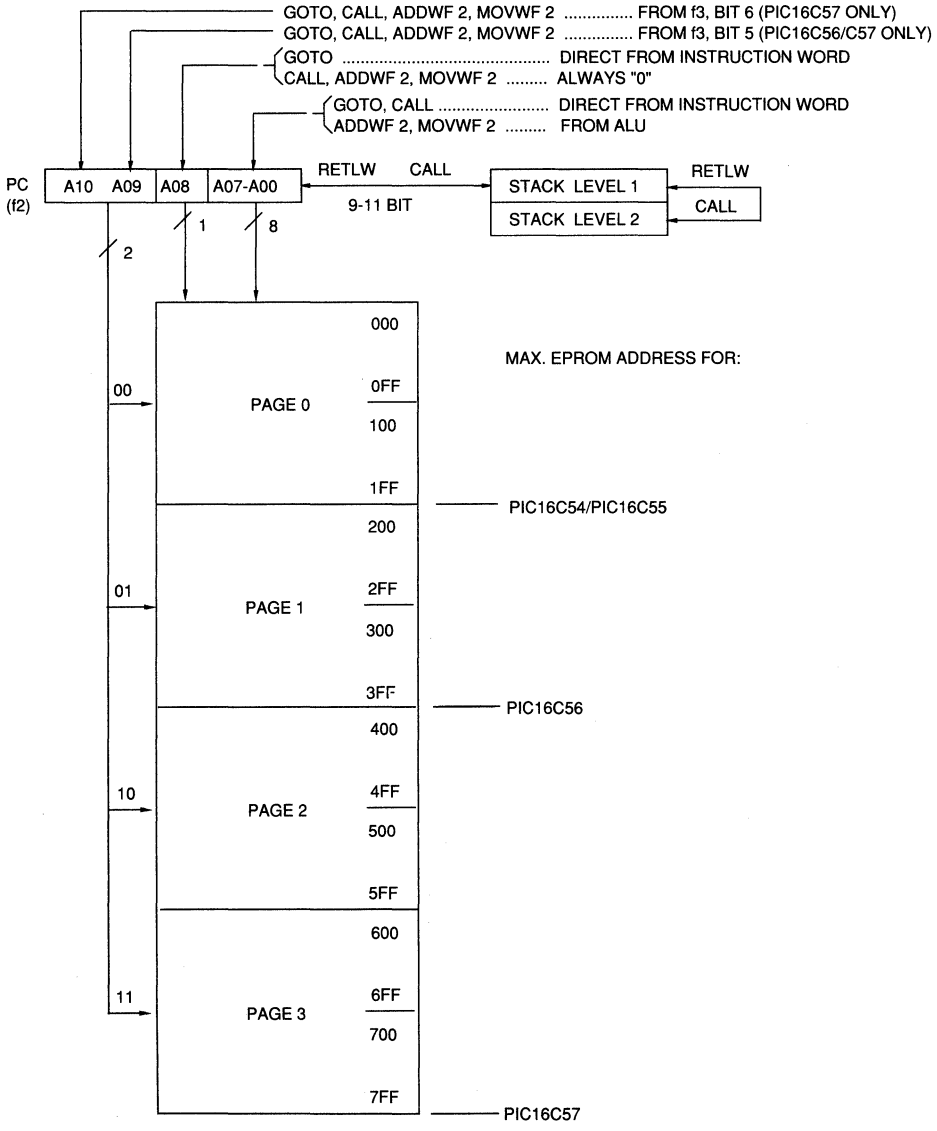
The PIC16C5x series employs a two level hardware push/pop stack (Figure 4).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.
For the PIC16C56 and PIC16C57, the page preselect bits of f3 will be loaded into the most significant bits of the program counter. The ninth bit is always cleared to "0" upon a CALL instruction. This means that subroutine entry addresses have to be located always within the lower half of a memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF). However, as the stack has always the same width as the PC, subroutines can be called from anywhere in the program.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than 2 subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. For the PIC16C56 and PIC16C57, the return will be always to the page from where the subroutine was called, regardless of the current setting of the page pre-select bits in file register f3. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is in particular useful for the implementation of "data" tables within the program memory.

OPERATIONAL REGISTER FILES (CONT.)

FIGURE 4: PROGRAM MEMORY ORGANIZATION



4

OPERATIONAL REGISTER FILES (CONT.)

f3 STATUS WORD REGISTER

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for larger program memories than 512 words (PIC16C56, PIC16C57).

f3 can be altered under program control only via bit set, bit clear, or MOVWF 3 instructions except for the "TO" and "PD" bits.

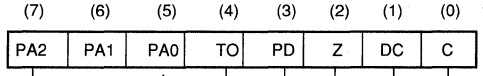
For other instructions, affecting any status bits, see section "Instruction Set Summary."

Time out and power down status bits (TO, PD)

The "TO" and "PD" bits in the status register f3 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or $\overline{\text{MCLR}}$ pin.

These status bits are only affected by events listed in Table 4.

STATUS WORD REGISTER f3



CARRY BIT:
For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY BIT:
For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is reset to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is reset to "0" by a watchdog timer time out.

PIC16C54/C55 : Two general purpose read/write bits

PIC16C56 : BIT 5 ... Page preselect bit
0 = Page 0 (000 - 1FF)
1 = Page 1 (200 - 3FF)

BIT 6 ... General purpose read/write bit

PIC16C57 : Two page preselect bits
00 = Page 0 (000 - 1FF)
01 = Page 1 (200 - 3FF)
10 = Page 2 (400 - 5FF)
11 = Page 3 (600 - 7FF)

BIT 7: General purpose read/write bit (reserved for future use)

OPERATIONAL REGISTER FILES (CONT.)

TABLE 4: EVENTS AFFECTING PD/TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 5 reflects the status of PD and TO after the corresponding event.

TABLE 5: PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on $\overline{MCLR}$ input

Note: The PD and TO bit maintain their status (X) until an event of Table 4 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the PD and TO status bits.

Program Page Preselect (PIC16C56, PIC16C57 ONLY)

Bits 5-6 of the STATUS register are defined as PAGE address bits PA0 - PA1, and are used to preselect a program memory page. When executing a GOTO, CALL, MOVWF 2, or ADDWF 2 instruction, PA0 - PA1 are loaded into bit A9-A10 of the program counter, selecting one of the available program memory pages. The direct address specified in the instruction is only valid within this particular memory page.
RETLW instructions do not change the page preselect bits.
Upon a RESET condition, PA0-PA2 are cleared to "0"s.

f4 FILE SELECT REGISTER (FSR)

PIC16C54/C55/C56

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file f0 in any of the file oriented instructions).
Bits 5-7 of the FSR are read-only and are always read as "one"s.
If no indirect addressing is used, the FSR can be used as a 5 bit wide general purpose register.

PIC16C57 ONLY

Bit 5 and 6 of the FSR select the current data memory bank (Figure 3).
The lower 16 bytes of each bank are physically identical and are always selected when bit 4 of the FSR (in case of indirect addressing) is "0", or bit 4 of the direct file register address of the currently executing instruction is "0" (e.g. MOVWF 08).
Only if bit 4 in the above mentioned cases is "1", bits 5 and 6 of the FSR select one of the four available register banks with 16 bytes each.
Bit 7 is read-only and is always read as "one."

4

I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF 6,W) read always the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB, TRISC) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

f5 (PORT A)

4-bit I/O register. Low order 4 bits only are used (RA0 - RA3). Bit 4 - 7 are defined as "zeros."

f6 (PORT B)

8-bit I/O register.

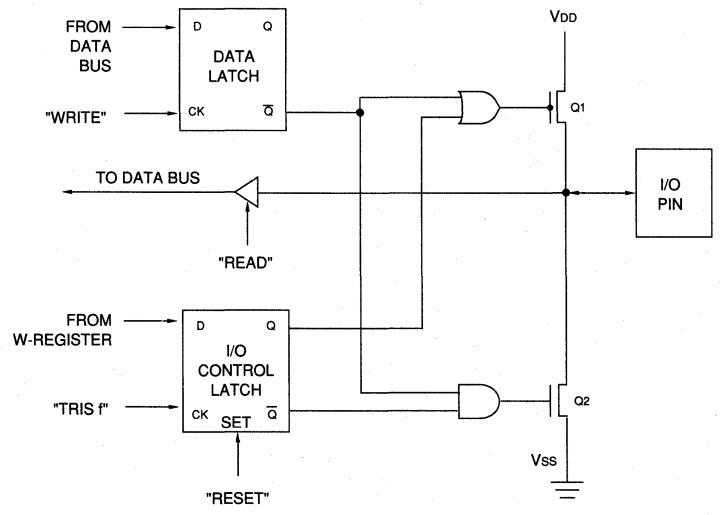
f7 (PORT C)

PIC16C55/C57 : 8-bit I/O register
PIC16C54/C56 : General purpose register.

I/O INTERFACING

The equivalent circuit for an I/O port bit is shown in Figure 5. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF 6, W). The outputs are latched and remain unchanged until the output latch is rewritten. For use as an output, the I/O control register (TRISA,TRISB, TRISC) must be zero in order to enable the output buffer. For use as an input the I/O control register must be "one" in order to allow an external device to drive the port high or low. This principle is the same whether operating on individual pins or the entire port. Any I/O pin can be programmed individually as input, output or bidirectional pin.

FIGURE 5: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



I/O PROGRAMMING HINTS

BIDIRECTIONAL I/O PORTS

a) Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. As an example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode , no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may disturb an otherwise clean power supply, and proper device functionality is not guaranteed.
For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).

SUCCESSIVE OPERATIONS ON I/O PORTS

Writing to an I/O port happens always at the end of an instruction cycle, while for reading, the data have to be valid as shown in Figure 20.
Therefore, care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

OPERATION IN NOISY ENVIRONMENT

In noisy application environments, for example keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes.
The on-chip watchdog timer will take care of all situations involving program sequence "lock-ups." However, if a I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lock-up" situation without leading to a watchdog timer timeout. Thus, it is recommended to redefine all I/O pins in regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading or putting data out.

GENERAL PURPOSE REGISTERS

PIC16C54/C55/C56 :

f08$_{16}$ - f1F$_{16}$: are general purpose register files.

PIC16C57 ONLY:

f08$_{16}$ - f0F$_{16}$: are general purpose register files which are always selected, independent of bank select.
f10$_{16}$ - f1F$_{16}$: general purpose register files in memory bank 0
f20$_{16}$ - f2F$_{16}$: physically identical to f00 - f0F
f30$_{16}$ - f3F$_{16}$: general purpose register files in memory bank 1
f40$_{16}$ - f4F$_{16}$: physically identical to f00 - f0F
f50$_{16}$ - f5F$_{16}$: general purpose register files in memory bank 2
f60$_{16}$ - f6F$_{16}$: physically identical to f00 - f0
f70$_{16}$ - f7F$_{16}$: general purpose register files in memory bank 3

SPECIAL PURPOSE REGISTERS

W WORKING REGISTER

Holds second operand in two operand instructions and/or supports the internal data transfer.

TRISA I/O CONTROL REGISTER FOR PORT A (f5)

Bit 0 - 3 only available. The corresponding I/O port (f5) is only 4 bit wide.

TRISB I/O CONTROL REGISTER FOR PORT B (f6)

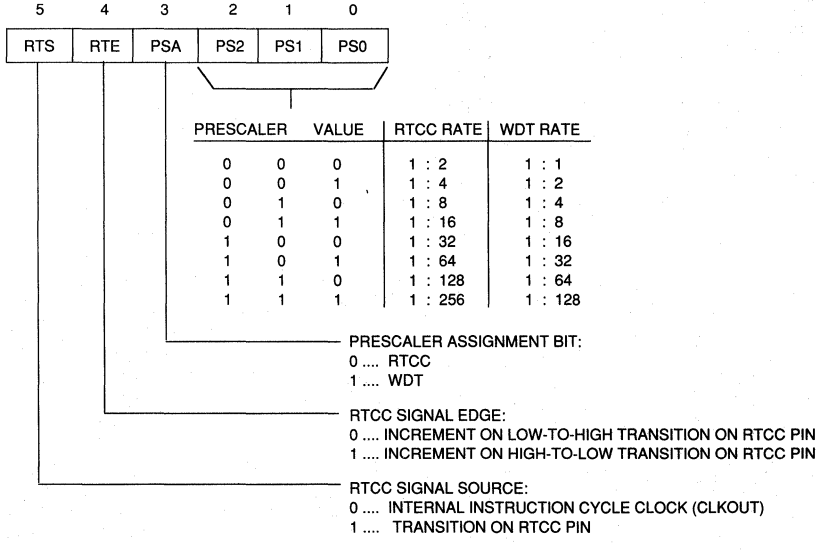
TRISC I/O CONTROL REGISTER FOR PORT C (f7)

The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register f5, f6, or f7 , respectively, out on the selected I/O pins.
These registers are "write-only" and are set to all "ones" upon a RESET condition.

OPTION PRESCALER/RTCC OPTION REGISTER

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide. By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register will be set to all "ones."

OPTION REGISTER



RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low", or by a Watchdog Timer Timeout. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the MCLR input is "low."

During a RESET condition the PIC function is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP)
- All I/O port pins (RA0 - RA3, RB0 - RB7, RC0 - RC7) are put into the high-impedance state (tri-stated) by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones"
- The OPTION register is set to all "ones"
- The Watchdog Timer and prescaler are cleared
- The upper three bits (page select bits) in the Status Register (f3) are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

PRESCALER

An 8-bit counter is available as prescaler for the RTCC, or as post-scaler for the watchdog timer, respectively (Figure 6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watch dog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and ratio.

The prescaler will be cleared whenever the circuit to which it is assigned is being written to. That is, when assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler.

PRESCALER PROGRAMMING CAUTIONS

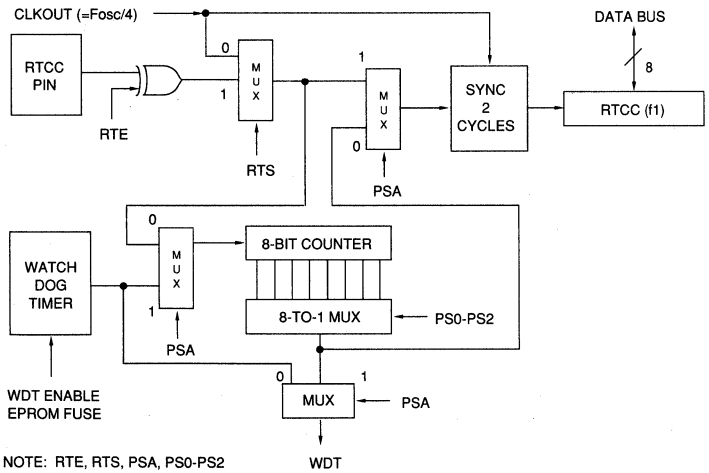
The prescaler assignment is fully under software control. Thus, it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence has to be executed when changing the prescaler assignment from RTCC to WDT:

```
1.MOVLW  B'xxx00xxx'   ;Select internal RTCC clock
2.OPTION               ;
3.CLRF 1               ;Clear RTCC and prescaler
4.MOVLW  B'xxxx1x10'   ;
5.OPTION               ;Select WDT prescaler with
                        ratio ≥ 1:4
```

Step 1 and 2 are only required if an external RTCC source is used with a clock period less than TCY +20ns. In all other cases, only steps 3-5 are necessary.

No precaution is required when changing the prescaler assignment from WDT to RTCC.

FIGURE 6: BLOCK DIAGRAM RTCC/WDT PRESCALER



BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC instruction set summary in Table 6 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. For the PIC16C57, bit 5 and 6 in the FSR determine the selected register bank.
The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.
For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

NOTES TO TABLE 6

Note1: The 9th bit of the program counter will be forced to a "zero" by CALL , MOVWF 2 , or ADDWF 2 instructions.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, a tristated pin which data latch is "1" but is driven low by an external device, will be relatched in the low state.

Note 3: The instruction "TRIS f" , where f = 5 or 6 or 7 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 6: INSTRUCTION SET SUMMARY

BYTE -ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0000 0000 0000	000	No Operation	**NOP**		-	None	
0000 001f ffff	02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0100 0000	040	Clear W	**CLRW**	-	0 → W	Z	
0000 011f ffff	06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 10df ffff	08f	Substract W from f	**SUBWF**	f, d	f - W → d [f + W + 1 → d]	C, DC, Z	1,2,4
0000 11df ffff	0Cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0001 00df ffff	10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0001 01df ffff	14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0001 10df ffff	18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4
0001 11df ffff	1Cf	Add W and f	**ADDWF**	f, d	W + f → d	C, DC, Z	1,2,4
0010 00df ffff	20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0010 01df ffff	24f	Complement f	**COMF**	f, d	f → d	Z	2,4
0010 10df ffff	28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0010 11df ffff	2Cf	Decrement f,Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0011 00df ffff	30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0011 01df ffff	34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 10df ffff	38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0011 11df ffff	3Cf	Increment f,Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4

BIT- ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary	(Hex)	Name	Mnemonic,Operands		Operation	Status affected	Notes
0100 bbbf ffff	4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff	5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff	6bf	Bit Test f,Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff	7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary	(Hex)	Name	Mnemonic,Operands		Operation	Status affected	Notes
0000 0000 0010	002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
0000 0000 0011	003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	TO, PD	
0000 0000 0100	004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	TO, PD	
0000 0000 0fff	00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1000 kkkk kkkk	8kk	Return,place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
1001 kkkk kkkk	9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
101k kkkk kkkk	Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1100 kkkk kkkk	Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
1101 kkkk kkkk	Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1110 kkkk kkkk	Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1111 kkkk kkkk	Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into a special EPROM fuse which is not part of the normal program memory EPROM. The PIC development tools "PIC-ICE" and "PICPRO" provide special commands to program this fuse.

WDT PERIOD

The WDT has a time-out period of approx. 18 ms. If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and may also vary from unit to unit due to variations in the manufacturing process. Please refer to the ELECTRICAL CHARACTERISTICS section and Figures 21, 22 for more details.

SPECIAL WDT PROGRAMMING CAUTIONS:

1. PIC16C54/C55:
   If no prescaler is assigned to the WDT, its typical time-out period is 18 ms. However, a CLRWDT or SLEEP instruction has to occur before 1/2 of the time-out period (i.e. 9 ms) is over . Otherwise, the CLRWDT or SLEEP instruction itself will cause a device RESET. If the WDT has a prescaler assigned, the full WDT period is available for a CLRWDT instruction.
   This precaution is not necessary for the PIC16C56 and PIC16C57.
2. In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.
   It should also be taken in account that under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

OSCILLATOR CIRCUITS

OSCILLATOR TYPES

The PIC16C5x series is available with 4 different oscillator circuits. On windowed devices, a particular oscillator circuit can be selected by programming the configuration EPROM accordingly. The PIC development tools (e.g. PIC-ICE, PICPRO) provide special commands to select the desired oscillator configuration.

On OTP and QTP devices, the oscillator configuration is determined by the factory and the parts are tested only to the according specifications.

CRYSTAL OSCILLATOR

The PIC16C5x-XT, -HS needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Fig. 7). Note that the series resistor Rs is only required for the "HS" oscillator.

RC OSCILLATOR

For timing uncritical applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition, there will be variation from unit to unit due to normal process variation. Figure 9 shows how the R/C combination is connected to the PIC16C5x. Some typical values for the oscillator frequency at given R and C values and supply voltages are listed in Table 7. For Rext values below 2.2 kOhm, the oscillator operation will become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise and humidity. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

TABLE 7: RC OSCILLATOR FREQUENCIES

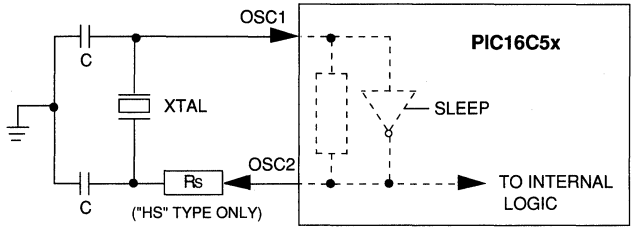
Rext	Cext	V_{DD}	F_{osc}	t = 25° C
5 kOhm	0 pF	5.0 V	4.0 MHz	
5 kOhm	20 pF	6.0 V	2.2 MHz	
5 kOhm	20 pF	3.5 V	2.5 MHz	
10 kOhm	130 pF	5.0 V	480 kHz	
10 kOhm	290 pF	5.0 V	245 kHz	
100 kOhm	300 pF	3.5 V	30 kHz	

Rext. min. = 2.2 kOhm, Cext. min. = 0 pF (see text)

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons.
Figure 10 shows the typical dependency of the oscillator frequency from VDD for given Rext/Cext values. Figure 11 shows the frequency as a typical function of the operating temperature with given R, C, and VDD values. Note that this graph is normalized to 25° C.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Fig. 20 for timing).

FIGURE 7: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT TYPES ONLY)



TYPICAL VALUES FOR C: 20 pF (CRYSTAL 4 MHz)
30 pF (CERAMIC RESONATOR 4 MHz)
Rs IS ONLY REQUIRED FOR "HS" DEVICES (100Ω < Rs < 1KΩ)

FIGURE 8: EXTERNAL CLOCK INPUT OPERATION (HS, XT TYPES ONLY)

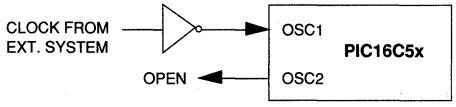


FIGURE 9: R/C OSCILLATOR (RC TYPE ONLY)

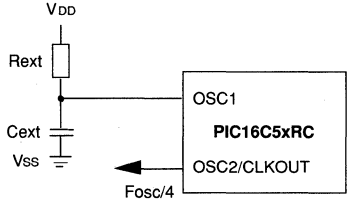


FIGURE 10: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

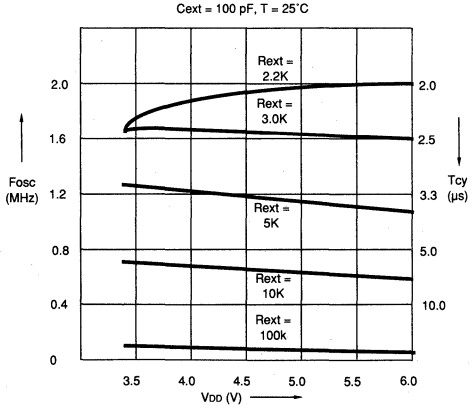
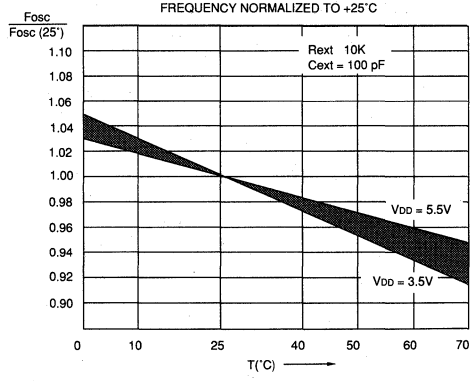


FIGURE 11: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE



OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approx. 18 ms after the voltage on the $\overline{MCLR}$ pin has reached the V_{IHMC} input level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.
The OST will also be triggered upon a watchdog timer timeout. This is in particular important for applications using the WDT to awake the PIC16C5x from SLEEP mode automatically.

POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.
When enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f3) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (High, Low, Hi-Z).
For lowest current consumption in this mode, all I/O pins should be either at V_{DD}, or V_{SS}, with no external circuitry drawing current from the I/O pin. If the I/O pins are in the High-Z mode they must be pulled high or low externally in order to avoid switching currents caused by floating inputs.
The $\overline{MCLR}$ pin must be at V_{IHMC}. The RTCC pin must be at V_{ILRT} or V_{IHRT}.

WAKE-UP

The device can be awakened by a watchdog timer timeout (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases the PIC will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on $\overline{MCLR}$ or WDT timeout) before normal program execution resumes.

The "PD" bit in the STATUS register, which is set to one during power on , but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 5). The TO bit in the Status register can be used to determine, if the "wake up" was caused by an external $\overline{MCLR}$ signal or a watchdog timer time out.

NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator startup times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC will be in RESET only for the oscillator start-up timer period.

CONFIGURATION EPROM

The configuration EPROM consists of four EPROM fuses which are not part of the normal EPROM for program storage.
Two are for the selection of the oscillator type (program only on parts in package with window), one is the watchdog timer enable fuse, and one is the code protection fuse.
The PIC development tools allow the setting of these fuses with special commands.
OTP or QTP devices have the oscillator configuration programmed by the factory and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC", "HS" following the part number to identify the oscillator type and operating range.

CUSTOMER ID CODE

The PIC16C5x series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution. The PIC16C5x programmers (PICPRO) provide special commands to read or write these ID bits.

CODE PROTECTION

The program code written into the EPROM can be protected by programming the code protection fuse with "0".
If the code protection logic is activated, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040_{16} and above are protected against programming.
It is still possible to program locations 000_{16} - $03F_{16}$, the 16 ID bits, the watchdog timer disable fuse, and, for windowed parts only, the oscillator configuration.
Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient temperature under bias .....-55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) .....-0.6V to VDD +0.6V
Voltage on VDD with respect to Vss .....0 to +9.5 V
Voltage on MCLR with respect to Vss
(Note 2) .....0 to +14 V
Total power Dissipation (Note 1) .....800 mW
Max. Current out of Vss pin .....150 mA
Max. Current into VDD pin .....50 mA
Max. Output Current sinked by any I/O pin .....25 mA
Max. Output Current sourced by any I/O pin .....20 mA
Max. Output Current sourced by a single
I/O port (Port A, B, or C) .....40 mA
Max. Output Current sinked by a single
I/O port (Port A, B, or C) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \Sigma Ioh\} + \Sigma\{(VDD-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$
2. Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the MCLR pin rather than pulling this pin directly to Vss.

PIN DESCRIPTIONS

Name	Function	Observation
RA0 - RA3	I/O PORT A	4 input/output lines
RB0 - RB7	I/O PORT B	8 input/output lines
RC0 - RC7	I/O PORT C	8 input/output lines, (PIC16C55/C57 only)
RTCC	Real Time Clock/Counter	Schmitt Trigger Input Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input A "Low" voltage on this input generates a RESET condition for the PIC16C5x microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

4

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions PIC16C5x Operating temperature 0 ≤ TA ≤ +70°C PIC16C5xI Operating temperature -40 ≤ TA ≤ +85°C, unless otherwise stated						
Characteristic	**Sym**	**Min PIC 16C5x**	**Min PIC 16C5xI**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage							
PIC16C5xXT (Note 3)	VDDxt	4.0	4.5		5.5	V	Fosc = 4 MHz
PIC16C5xRC (Note 3)	VDDrc	4.0	4.5		5.5	V	Fosc = 4 MHz
PIC16C5xHS (Notes 3,8)	VDDhs	4.5			5.5	V	Fosc = 8 MHz
PIC16C5xHS (Notes 3,8)	VDDhs		4.75		5.25	V	Fosc = 8 MHz
RAM Data Retention Voltage (Notes 3, 4)	VDR			1.5		V	Device in SLEEP mode
Power-on trip voltage to set 'TO" and "PD" status bit	VPOR			1.2		V	at VDD pin (Note 7), MCLR pin tied to VDD
Supply Current (Notes 2, 3)							
PIC16C5xXT	IDDxt			1.8	3.3	mA	Fosc = 4 MHz, VDD=5.5V, T = -40°C
PIC16C5xRC (Note 6)	IDDrc			1.8	3.3	mA	Fosc = 4 MHz , VDD=5.5V, T = -40°C
PIC16C5xHS (Note 8)	IDDhs			4.8	10.0	mA	Fosc = 8 MHz, VDD=5.5V, T = -40°C
Power Down Current (Notes 3, 5)							
PIC16C5x	IPD1			10	TBD	µA	SLEEP, All I/Os at VDD or VSS. VDD = 3.5V, WDT enabled, @25°C
	IPD2			5	TBD	µA	SLEEP, All I/Os at VDD or VSS. VDD = 3.5V, WDT disabled, @25°C

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, MCLR = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: Data include PIC16C54/PIC16C55 only.

Note 4: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 5: The power down current in SLEEP mode does not depend on the oscillator type. Maximum values will be available when characterization of all product variants is complete.

Note 6: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 7: On the rising edge of VDD, when VDD exceeds VPOR the device will be in RESET until the oscillator start-up timer times out.

Note 8: 20 MHz for future release.

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions Operating temperature -40 < TA < +85°C, unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin "tristated"
MCLR	VILMC	VSS		0.15 VDD	V	
RTCC	VILRT	VSS		0.15 VDD	V	
OSC1	VILOSC	VSS		0.15 VDD	V	PIC16C5xRC only! (Note 6)
OSC1	VILOSC	VSS	0.3 VDD		V	Driven with external clock. Not PIC16C5xRC.
Input High Voltage						
I/O ports	VIH	2.0		VDD	V	Pin "tristated"
MCLR	VIHMC	VDD-0.2		VDD	V	
RTCC	VIHRT	VDD-0.2		VDD	V	
OSC1	VIHOSC	VDD-0.2		VDD	V	PIC16C5xRC only ! (Note 6)
OSC1	VIHOSC		0.7 VDD	VDD	V	Driven with external clock. Not PIC16C5xRC.
Input Leakage Current (Notes 3, 4)						
I/O ports	IIL	-1		+1	µA	VSS < VPIN <VDD, Pin "tristated"
MCLR	IILMCL	-5			µA	VPIN = VSS + 0.25V
MCLR	IILMCH		+1	+5	µA	VPIN = VDD
RTCC	IILRT	-3	+-1	+3	µA	VSS < VPIN <VDD
OSC1	IILOSC1	-3	+-1	+3	µA	" " " , Not PIC16C5xRC
Output Low Voltage						
I/O Ports	VOL	-	-	0.6	V	IOL = 9.2 mA, VDD = 5.5V
OSC2/CLKOUT (PIC16C5xRC)	VOL	-	0.1 VDD		V	IOL = TBD
Output High Voltage						
I/O Ports (Note 4, 5)	VOH	VDD-0.7V	-	-	V	IOH = -3.4 mA, VDD = 5.5V
OSC2/CLKOUT (PIC16C5xRC)	VOH		0.9 VDD	-	V	IOH = TBD

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

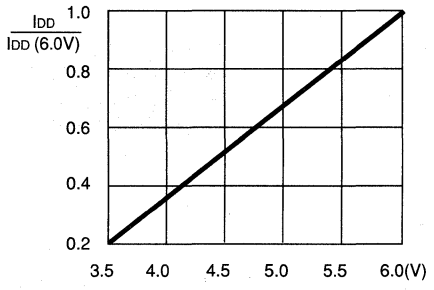
Note 4 : Negative current is defined as coming out of the pin.

Note 5 : The maximum currents per I/O pin, port, or total device under normal operating conditions must not exceed 80% of the "Absolute Maximum Ratings."

Note 6 : For PIC16C5xRC devices, the OSC1 pin is a Schmitt trigger input.

TYPICAL DC CHARACTERISTICS GRAPHS (PIC16C5x-XT, PIC16C5x-RC)

FIGURE 12: IDD vs. VDD (NORMALIZED)



NOTE: The following graphs are based on characterization data and are for design guidance only. Most graphs are normalized to the worst case conditions to allow easy extrapolation for different operating conditions. For example, IDD max at 2.0 MHz, 5.0V can be derived from 3.3 mA • 0.7 • 0.65 ≈ 1.5 mA.

FIGURE 13: IDD vs. FREQUENCY (NORMALIZED)

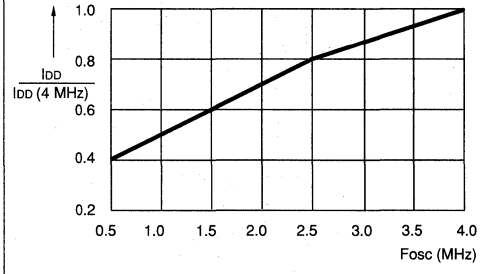
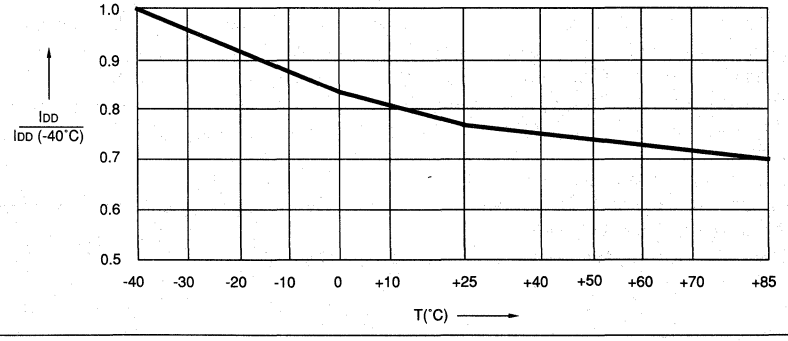


FIGURE 14: IDD vs. Temperature (NORMALIZED)



TYPICAL DC CHARACTERISTICS GRAPHS (PIC16C5x-XT, PIC16C5x-RC) (Cont.)

FIGURE 15: IDD vs. VDD (SLEEP MODE)

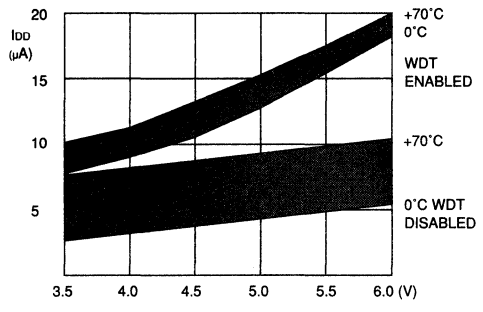


FIGURE 16: IOL vs. VOL

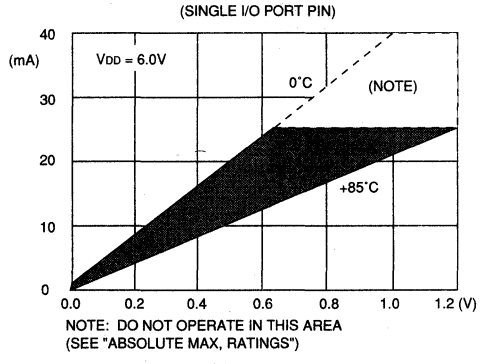
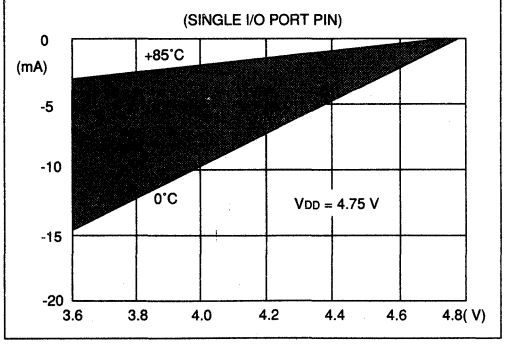


FIGURE 17: IOH vs. VOH



4

AC CHARACTERISTICS

AC CHARACTERISTICS						Standard Conditions (unless otherwise noted) Operating temperature TA = -40 to +85°C
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Instruction cycle time	TCYXT	1.0	-	10	usec	PIC16C5xXT, (Note 2) VDD within VDDXT specification
	TCYRC	1.0	-	DC	usec	PIC16C5xRC, (Note 2) VDD within VDDRC specification
	TCYHS	0.5	-	1.0	usec	PIC16C5xHS, (Note 2, 4) VDD within VDDHS specification
RTCC Input Timing						
Period	TRT	(TCY+20)/N	-	-	nsec	external RTCC input (N = selected prescaler ratio) Note 3
High Pulse Width	TRTH	TCY/2N	-	-	nsec	
Low Pulse Width	TRTL	TCY/2N	-	-	nsec	
Prescaler Toggling Freq.	FPMAX	-	32	-	MHz	Note 3
Watchdog timer period/ Oscillator start-up timer period (no prescaler)	TWDT/ TOST	TBD -	18 -	TBD -	msec -	VDD = 5.0V, Temp. = +25° C -

Note 1: Data in the column labeled "Typical" is based on characterization results at 25° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

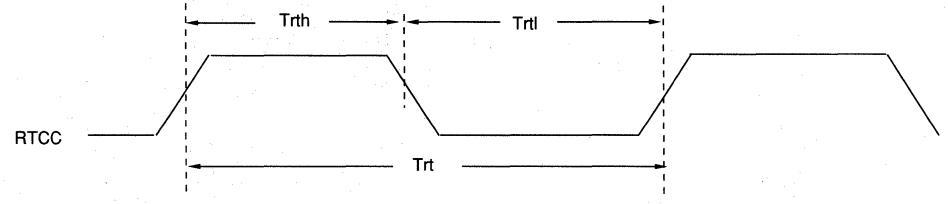
Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these spec. limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external oscillator is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: The prescaler is designed as a simple ripple counter. Its maximum input frequency is theoretically only limited by the maximum toggling frequency of the first counter stage. However, as the prescaler output has to be synchronized before fed into the RTCC, FPMAX is also a function of TCY and the number of selected prescaler stages (N). Thus, the relationship

$$\frac{1}{T_{RT}} = \frac{N}{T_{CY} + 20} < F_{PMAX}$$ must be obeyed.

Note 4: TCYHS min. = 0.2µs for 20 MHz oscillator (future release).

FIGURE 18: RTCC TIMING



AC CHARACTERISTICS (CONT.)

FIGURE 19: OSCILLATOR START-UP TIMING (PIC16C5xRC*)

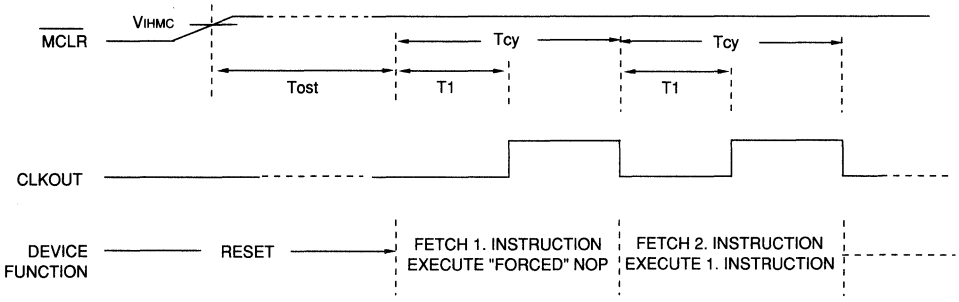
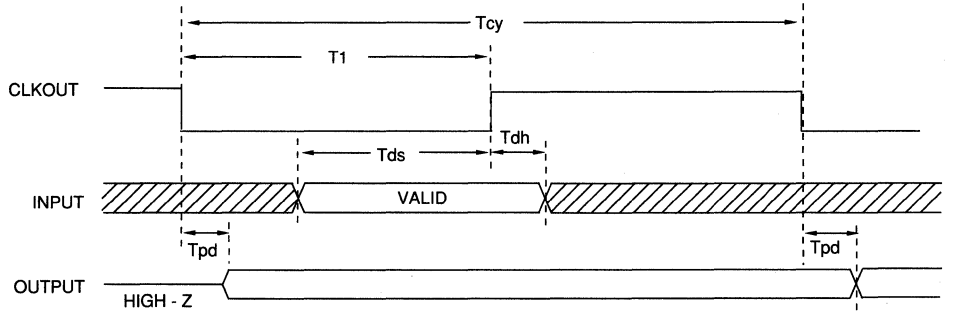


FIGURE 20: INPUT/OUTPUT TIMING FOR I/O PORTS (PIC16C5xRC*)



T1 = 1/2 TCY + 20 ns
Tds = 1/4 TCY + TBD ns
Tdh = 0 ns
Tpd = TBD ns

* The oscillator start-up timing and the input/output timing is for all PIC16C5x devices the same. However, the CLKOUT signal is only available at PIC16C5xRC devices.

FIGURE 21: TYPICAL WDT PERIOD vs. TEMP. (NORMALIZED TO +25°C)

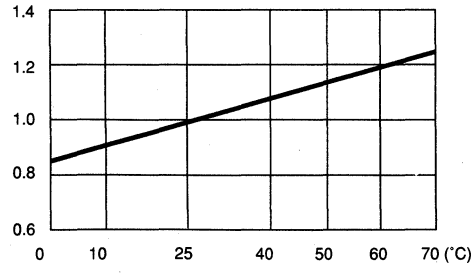
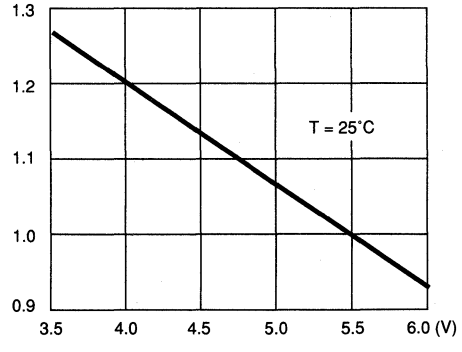


FIGURE 22: TYPICAL WDT PERIOD vs. VDD (NORMALIZED TO +5.5V)



DEVELOPMENT SUPPORT

PIC-ICE™

The PIC-ICE In-Circuit Emulation System from Microchip allows real time emulation of all chip functions with frequencies up to 20 MHz. Symbolic debugging, hardware breakpoints, software tracing, sample programming are just a few of the capabilities of this IBM PC hosted development system. Please contact your nearest sales office for details.

PICPAK DEVELOPMENT KIT

PICPAK is a low-cost PIC Applications and development Kit, consisting of PICALC, PICSIM, PICPRO, and PIC16C54/PIC16C55 samples.

PICALC CROSS-ASSEMBLER

The PIC Cross Assembler **PICALC** is available for several host computer platforms, including IBM PC. Macro assembly and conditional asssembly are just a few of the capabilities of PICALC. Besides the PIC16C5x Series, PICALC can also generate code for all of Microchip's NMOS PIC1600 microcontrollers, including the PIC165x and PIC167x family members. PICALC can generate various object code formats to support Microchip's proprietary development tools as well as third party systems.

PICSIM SOFTWARE SIMULATOR

The software simulator **PICSIM** allows PIC16C5x code development on IBM PCs without any additional hardware. It simulates the PIC16C5x series on instruction level. Software trace, breakpoints, symbolic debugging, and stimulus file generation are just a few of the features available. PICSIM is particularly useful in the early development stages of an application, or when real-time and/or in-circuit emulation are not necessary for the code development.

PICPRO EPROM PROGRAMMER

PICPRO is a low volume EPROM programmer for the PIC16C5x series. It allows downloading and programmming of PIC object code generated with PICALC from any host computer system providing a serial interface (RS232).

EPROM PROGRAMMING

PROTOTYPE PROGRAMMERS

Microchip's proprietary PIC16C5x series Development System and PICPRO, were not designed for high volume production programming but were designed strictly to support engineering development level programming of PIC16C5x EPROM and OTP units. Microchip assumes no responsibility for the replacement of programming rejects when these development tools are used to support high volume production level programming.

VOLUME PROGRAMMERS

High volume programming by the customer should be supported by production quality programmers from approved third party sources. Currently the approved sources are Data I/O "Unisite (Site 48)" model and Logical Devices' "ALLPRO" model.

Microchip assumes no responsibility for replacing defective units related to mechanical and/or electrical problems of any third party programming equipment or the improper use of such equipment.

Programming of the code protection bit (also called "security bit" or "security fuse") implies that the contents of the PIC16C5x EPROM can no longer be verified, thus making programming related failure analysis an impossibility.

Microchip warrants that PIC16C5x units will not exceed a programming failure rate of 1% of shipment quality. Programming related failures beyond this level can be returned for replacement, again, if the security bit has not been programmed.

FACTORY PROGRAMMING

High volume factory programming (QTP) is an available service from Microchip Technology. A small price adder and minimum quantity requirements apply.

CURRENT PRODUCT AVAILABILITY

The following selections are currently available (for the Part-Number coding, refer to the back-page):

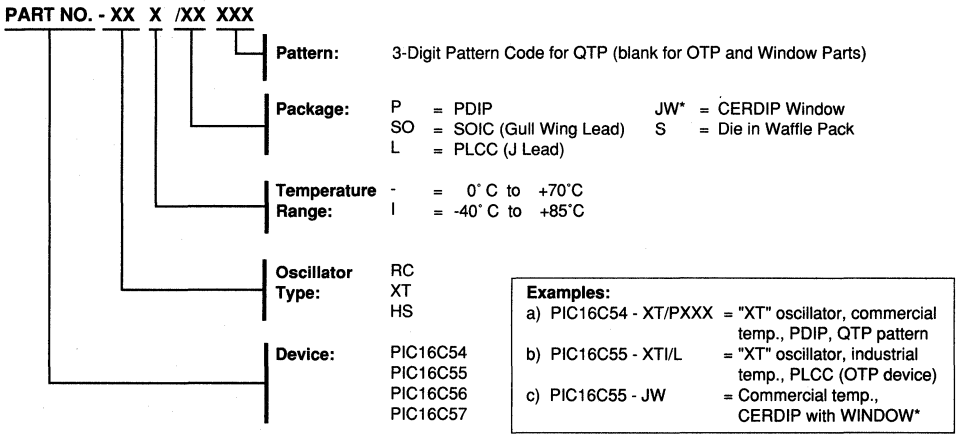
Oscillator Type	Temp/ Package	Descriptions
RC,XT or HS	/P	PDIP, 0°C to +70°C
RC,XT or HS	I/P	PDIP, -40°C to +85°C
RC,XT or HS	/SO	SOIC, 0°C to +70°C
RC,XT or HS	I/SO	SOIC, -40°C to +85°C
RC,XT or HS	/L	PLCC, 0°C to +70°C
RC,XT or HS	I/L	PLCC, -40°C to +85°C
(Fuse-Programmed)*	/JW	Window CERDIP, 0°C to +70°C

* JW has UV erasable fuses which determine oscillator types RC, XT or HS.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. For the *currently available code-combinations*, refer to previous page.



Notes: * For UV-erasable devices, the oscillator type is RC by default (= erased device). The user can select XT or HS oscillators by programming the according fuses with PICPRO.

Microchip

PIC1654S

8-Bit Microcontroller

FEATURES

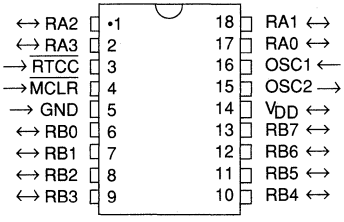
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self contained oscillator for crystal or ceramic resonator
- Access to RAM registers inherent to instruction
- Available in three temperature ranges: 0° to 70°C, -40° to 85°C and -40° to 110°C
- 18 pin package
- 2 level stack for subroutine nesting
- Open drain option on all I/O lines
- 12 bi-directional I/O lines
- 2 μsec instruction execution time

PIN CONFIGURATION

18 Lead Dual In Line

18 Lead SOIC

Top View



4

DESCRIPTION

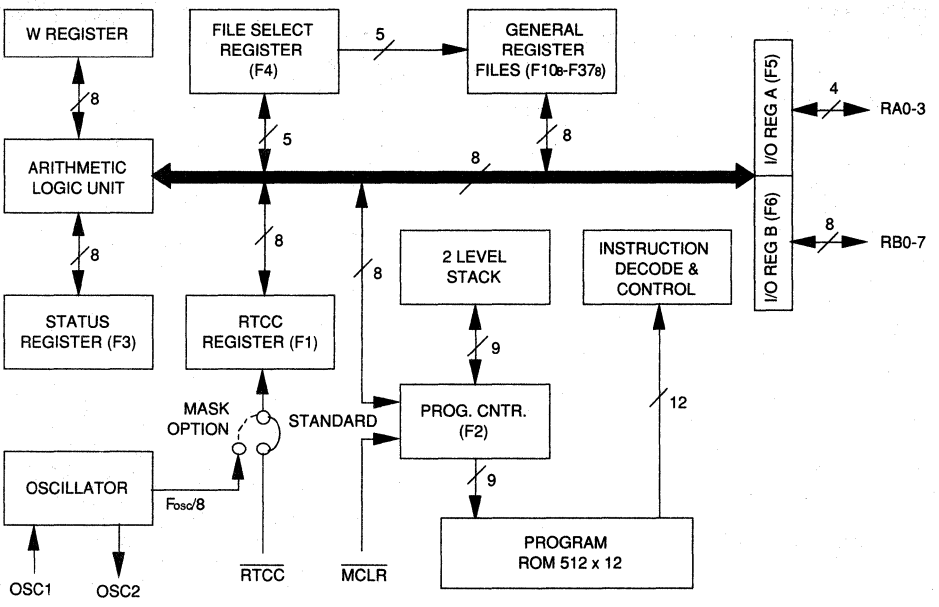
The PIC1654S microcontroller is a MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities for motor control, telecommunication equipment, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1654S is fabricated with N-Channel Silicon Gate technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal or ceramic resonator to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, a powerful macroassembler. PICALC is available in various versions that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PICES II real time In-Circuit Emulation System, PIC Field Demo boards (PFD), and the ROM-less version of the PIC1654S, the PIC1664, provide all required development and debugging tools.

PIC1654S BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcontroller is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock/Counter (RTCC), the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTION TABLE

Signal	Definition
OSC1 (Input), OSC2 (Output)	These pins are the time base inputs to which a crystal, ceramic resonator, or external single phase clock may be connected. The frequency of oscillation is 8 times the instruction cycle frequency.
$\overline{\text{RTCC}}$ (Input)	Real Time Clock/Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock/Counter Register increments on falling edges applied to this pin. This register (F1) can be loaded and read by the program. This is a Schmitt trigger input. A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock counter register. In this mode, transitions in the $\overline{\text{RTCC}}$ pin will be disregarded. However, the pin must be tied to either VSS or VDD to avoid unintended test mode activation.
RA0-3 (Input/Output)	4 user programmable I/O lines (F5). The four MSB's are always read as logic 0's. All inputs and outputs are under direct control of the program. A mask option will allow any I/O pin at the time of ROM pattern definition to be open drain.
RB0-7 (Input/Output)	8 user programmable I/O lines (F6). All inputs and outputs are under direct control of the program. A mask option will allow any I/O pin at the time of ROM pattern definition to be open drain.
$\overline{\text{MCLR}}$ (Input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high. Should be held low 10 - 75ms past the time when $V_{DD} \geq 4.5V$ depending on the crystal start up time. This is a Schmitt trigger input.
VDD	Power supply.
VSS	Ground pin.

4

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W + F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock/Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on high-to-low transitions on the RTCC input. However, if data is being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The nine bit wide PC is automatically incremented during each instruction cycle, unless it is written into under program control (MOVWF F2, GOTO, CALL, ADDWF F2, RETLW). CALL, MOVWF2, ADDWF2 instructions write only the 8 low order bits of the PC, while the MSB is made to zero. Only the 8 low order bits of F2 can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction. (7) (6) (5) (4) (3) (2) (1) (0) 1 1 1 1 1 Z DC C C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source. DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant. Note that a subtraction os always executed as an addition of the two's complement of the second operand. Z (Zero): Set if the result of an Arithmetic operation is zero. Bits: 3-7 These bits are defined as logic ones.
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (RA0-RA3) (RA4 - RA7 defined as zeros).
F6	I/O Register B (RB0-RB7).
F7-F37$_8$	General Purpose Registers.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code that specifies the instruction type and one or more operands specifying the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit oriented instructions, "b" represents a bit field designator that selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight- or nine-bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 2 µsec, unless a conditional test is true or the program counter is changed as a result of an instruction*. In these two cases, the instruction execution time is 4 µsec.

* (GOTO, CALL, RETLW, MOVWF2, ADDWF2).

BYTE-ORIENTED FILE REGISTER

For d = 0, f → W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f → f (if d is omitted, assembler assigns d = 1).

(11-6)	(5)	(4-0)
OP CODE	d	f(FILE #)

Instruction-Binary (Octal)					Name	Mnemonic, Operands		Operation	Status Affected
000	000	000	000	(0000)	No Operation	NOP	-	-	None
000	000	1ff	fff	(0040)	Move W to f (Note 1)	MOVWF	-	W→f	None
000	001	000	000	(0100)	Clear W	CLRW	-	0→W	Z
000	001	1ff	fff	(0140)	Clear f	CLRF	f	0→f	Z
000	010	dff	fff	(0200)	Subtract W from f	SUBWF	f,d	f-W→d [f + $\overline{W}$ + 1→d]	C,DC,Z
000	011	dff	fff	(0300)	Decrement f	DECF	f,d	f-1→d	Z
000	100	dff	fff	(0400)	Inclusive OR W and f	IORWF	f,d	W∨f→d	Z
000	101	dff	fff	(0500)	ANDbW and f	ANDWF	f,d	W•f→d	Z
000	110	dff	fff	(0600)	Exclusive OR W and f	XORWF	f,d	W⊕f→d	Z
000	111	dff	fff	(0700)	Add W and f	ADDWF	f,d	W + F→d	C,DC,Z
001	000	dff	fff	(1000)	Move f	MOVF	f,d	f→d	Z
001	001	dff	fff	(1100)	Complement f	COMF	f,d	f→d	Z
001	011	dff	fff	(1200)	Increment f	INCF	f,d	f + 1→d	Z
001	011	dff	fff	(1300)	Decrement f, Skip to Zero	DECFSZ	f,d	f - 1→d, skip if Zero	None
001	100	dff	fff	(1400)	Rotate Right f	RRF	f,d	f(n)→d(n-1), C→d(7), f(0)→C	C
001	101	dff	fff	(1500)	Rotate Left f	RLF	f,d	f(n)→d(n + 1), C→d(0), f(7)→C	C
001	110	dff	fff	(1600)	Swap halves f	SWAPF	f,d	f(0-3)↔f(4-7)→d	None
001	111	dff	fff	(1700)	Increment f, Skip if Zero	INCFSZ	f,d	f + 1→d, skip if Zero	None

4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f(FILE #)

Instruction-Binary (Octal)					Name	Mnemonic, Operands		Operation	Status Affected
010	0bb	bff	fff	(2000)	Bit Clear f	BCF	f,b	0→f(b)	None
010	1bb	bff	fff	(2400)	Bit Set f	BSF	f,b	1→f(b)	None
011	0bb	bff	fff	(3000)	Bit Test f, skip if Clear	BTFSC	f,b	Bit Test f(b): skip if clear	None
011	1bb	bff	fff	(3400)	Bit Test f, skip if Set	BTFSS	f,b	Bit Test f(b): skip if set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)					Name	Mnemonic, Operands		Operation	Status Affected
100	0kk	kkk	kkk	(4000)	Return and place Literal in W	RETLW	k	k→w, Stack→PC	None
100	1kk	kkk	kkk	(4400)	Call subroutine (Note 1)	CALL	k	PC+1-Stack, k→PC	None
101	kkk	kkk	kkk	(5000)	Go to address (k is 9 bits)	GOTO	k	k→PC	None
110	0kk	kkk	kkk	(6000)	Move Literal to W	MOVLW	k	k→W	None
110	1kk	kkk	kkk	(6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111	0kk	kkk	kkk	(7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111	1kk	kkk	kkk	(7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377₈. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3.0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

SUPPLEMENTAL INSTRUCTION SET SUMMARY

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Operation	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	-
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	-
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	-
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	-
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	-
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	-
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	-
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC3, 0	-
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	-
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3,1	-
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	-
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC3, 2	-
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140)	Negate File	NEGF f,d	COMF f, 1	
001 010 dff fff (1200)			NCFf,d	Z
011 000 000 011 (3003)	Add Carry to File	ADDCF f,d	BTFSC 3,0	
001 010 dff fff (1200)			INCF f,d	Z
011 000 000 011 (3003)	Subtract Carry from File	SUBCF f,d	BTFSC 3, 0	
000 011 dff fff (0300)			DECF f,d	Z
011 000 100 011 (3043)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3, 1	
001 010 dff fff (1200)			INCF f,d	Z
011 000 100 011 (3043)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3, 1	
000 011 dff fff (0300)			DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	-
011 000 000 011 (3003)	Branch on Carry	BC k	BTFSC 3, 0	
101 kkk kkk kkk (5000)			GOTO k	-
011 100 000 011 (3403)	Branch on No Carry	BNC k	BTFSS 3, 0	
101 kkk kkk kkk (5000)			GOTO k	-
011 100 100 011 (3043)	Branch on Digit Carry	BDC k	BTFSC 3, 1	
101 kkk kkk kkk (5000)			GOTO k	-
011 001 000 011 (3443)	Branch on No Digit Carry	BNDC k	BTFSS 3, 1	
101 kkk kkk kkk (5000)			GOTO k	-
011 101 000 011 (3103)	Branch on Zero	BZ k	BTFSC 3, 2	
101 kkk kkk kkk (5000)			GOTO k	-
011 101 000 011 (3503)	Branch on No Zero	BNZ k	BTFSS 3, 2	
101 kkk kkk kkk (5000)			GOTO k	-

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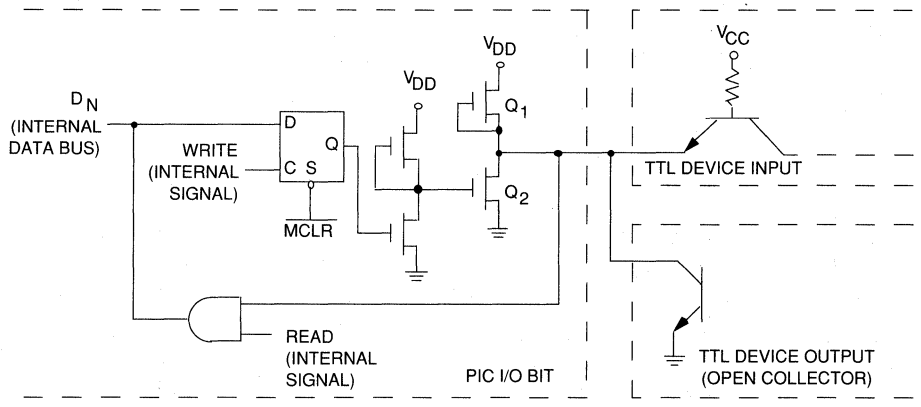
I/O INTERFACING

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100µA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



NOTE: TRANSISTOR Q_1 CAN BE REMOVED PER MASK OPTION TO FORM AN OPEN-DRAIN OUTPUT.

PROGRAMMING CAUTIONS

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

BIDIRECTIONAL I/O PORTS

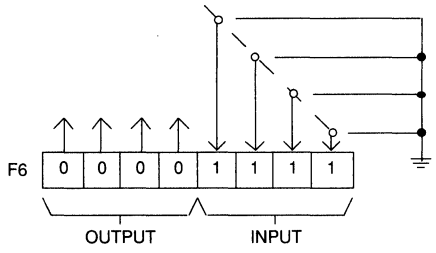
The bidirectional ports may be used for both inut and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output latch must be set in the high state. Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F6 (port RB) will cause all eight bits of F6 to be read into the CPU. Then the BSF operation takes place on bit 5 and F6 is re-output to the output latches. If another bit of F6 is used as an inut (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples on the next page.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if tpd (See I/O Timing Diagram) is greater than 1/4tcy (min). When in doubt, it 's better to separate these instructions with a NOP or other instruction.

EXAMPLE 1

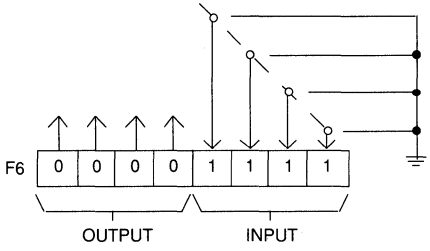


What is thought to be happening:
BSF 6,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F6:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2



What could happen if an input were low:
BSF 6,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F6:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature under bias..... 125°C
Storage Temperature ..... - 55°C to +150°C
Voltage on any pin with respect to VSS (except open drain) ..... -0.3V to + 9.0V
Voltage on any pin with respect to VSS (open drain) ..... -0.3V to + 13V
Power Dissipation (Note 1) 800mW

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS - PIC16C54S

Operating temperature TA = 0°C to + 70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Power Supply Voltage	VDD	4.5	-	7.0	V	
Primary Supply Current	IDD	-	30	50	mA	All I/O pins @ VDD (See Primary Supply Current Chart for additional information).
Input Low Voltage	VIL	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	VIH	2.4	-	VDD	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	VIH2	VDD - 1	-	VDD	V	(Note 4)
Output High Voltage	VOH	2.4	-	VDD	V	IOH = -100µA provided by internal pullups (Note 2)
Output Low Voltage (I/O only)	VOL1	-	-	0.45	V	IOL = -1.6mA, (Note 3)
Input $\overline{RTCC}$ Current	IRTCC	-	7	20	µA	VSS ≤ VIN ≤ VDD
Input Leakage Current ($\overline{MCLR}$)	IIC	- 5	-	+ 5	µA	VSS ≤ VIN ≤ VDD
Output Leakage Current (open drain pins)	IOL	-	-	10	µA	VSS ≤ VPIN ≤ 12V
Input Low Current (all I/O ports)	IIL	- 0.2	-	-1.6	mA	VIL = 0.4V (internal pullup)
Input High Current (all I/O ports)	IIH	- 0.1	-0.4	-	mA	VIH = 2.4V

† Typical data is at TA = 25°C, VDD = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   PD = (VDD) (IDD) + Σ(VDD - VIL) (IIOHI) + Σ(VOL) (IOL).
   The term I/O refers to all interface pins; input, output or I/O.
2. Positive current indicates current into pin.
   Negative current indicates current out of pin.
3. Total IOL for all output pins must not exceed 175 mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed VDD + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application it must be tied to VSS or VDD.

DC CHARACTERISTICS-PIC1654S-I

Operating temperature T_A = -40°C to + 85°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	-	7.0	V	
Primary Supply Current	I_{DD}	-	30	54	mA	All I/O pins @ V_{DD} (See Primary Supply Current Chart for additional information).
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH2}	V_{DD} - 1	-	V_{DD}	V	(Note 4)
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA provided by internal pullups (Note 2)
Output Low Voltage (I/O only)	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA (Note 3)
Input $\overline{RTCC}$ Current	I_{RTCC}	-	7	20	µA	$V_{SS} \le V_{IN.} \le V_{DD}$
Input Leakage Current ($\overline{MCLR}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN.} \le V_{DD}$
Output Leakage Current (open drain pins)	I_{OL}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 9V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-	-1.6	mA	V_{IL} = 0.4V(internal pullup) T_A = 0°C to 85°C
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{ILI}) + \Sigma(V_{DD} - V_{OH})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins must not exceed 175 mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed V_{DD} + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application, it must be tied to V_{SS} or V_{DD}.

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DC CHARACTERISTICS - PIC1654S-H

Operating temperature T_A = -40°C to + 110°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	-	5.5	V	
Primary Supply Current	I_{DD}	-	35	58	mA	All I/O pins @ V_{DD} (See Primary Supply Current Chart for additional information).
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH2}	V_{DD} - 1	-	V_{DD}	V	(Note 4)
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA provided by internal pullups (Note 2)
Output Low Voltage (I/O only)	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA (Note 3)
Input $\overline{RTCC}$ Current	I_{RTCC}	-	7	20	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Input Leakage Current ($\overline{MCLR}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OL}	-	-	20	µA	$V_{SS} \le V_{PIN} \le 9V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-	-1.6	mA	V_{IL} = 0.4V(internal pullup) T_A = 0°C to 110°C
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{ILI}) + \Sigma(V_{DD} - V_{OH})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins must not exceed 17 5mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed V_{DD} + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application, it must be tied to V_{SS} or V_{DD}.

AC CHARACTERISTICS - PIC1654S

Operating temperature T_A = 0°C to + 70°C

-40°C to +85°C and -40°C to + 110°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	2	-	10	µs	0.8 MHz - 4.0MHz external time base (Notes 1 and 2)
$\overline{\text{RTCC}}$ Input						
Period	t_{RT}	t_{CY} = 0.2µs-	-	-	-	Note 3
High Pulse Width	t_{RTH}	1/2 t_{RT}	-	-	-	
Low Pulse Width	t_{RTL}	1/2 t_{RT}	-	-	-	

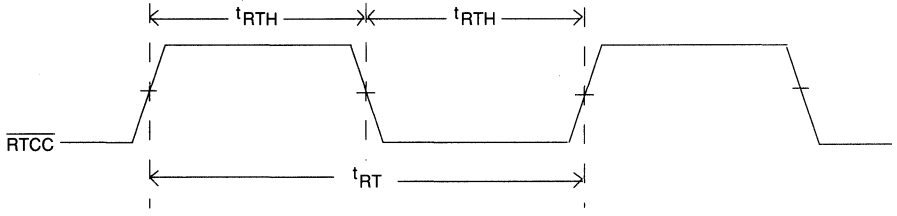
NOTES:

1. Instruction cycle period (t_{CY}) equals eights times the input oscillator time base period.
2. The oscillator frequency may deviate to 4.08MHz to allow for tolerance of a crystal or ceramic resonator time base element.
3. The maximum frequency which may be input to the $\overline{\text{RTCC}}$ pin is calculated as follows:

$$f(max) = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

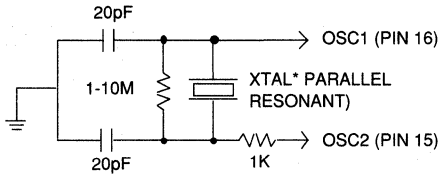
For example: if t_{CY} = 4µs, $f(max) = \frac{1}{4.2\mu s}$ = 238KHz.

RTCC TIMING



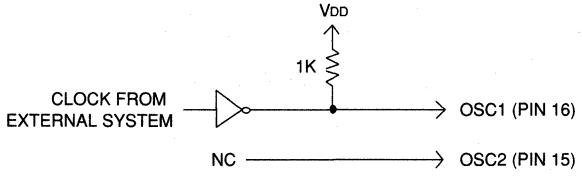
OSCILLATOR OPTIONS (TYPICAL CIRCUITS) (Cont.)

CRYSTAL INPUT OPERATION



* Or ceramic resonator

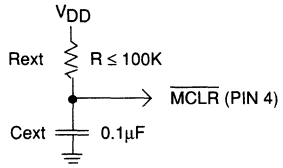
EXTERNAL CLOCK INPUT OPERATION



PRIMARY SUPPLY CURRENT AT SELECTED TEMPERATURES

		PIC1654S PIC1654S-I		PIC1654S-H			
Characteristic	**Sym**	**Typ**	**Max**	**Typ**	**Max**	**Units**	**Conditions**
Primary Supply Current	IDD	40	54	48	58	mA	-40°C, All I/O pins at VDD
		35	50	44	54	mA	0°C, All I/O pins at VDD
		24	45	39	49	mA	70°C, All I/O pins at VDD
		22	42	36	46	mA	85°C, All I/O pins at VDD
		-	-	30	40	mA	110°C, All I/O pins at VDD

MASTER CLEAR (TYPICAL CIRCUIT)

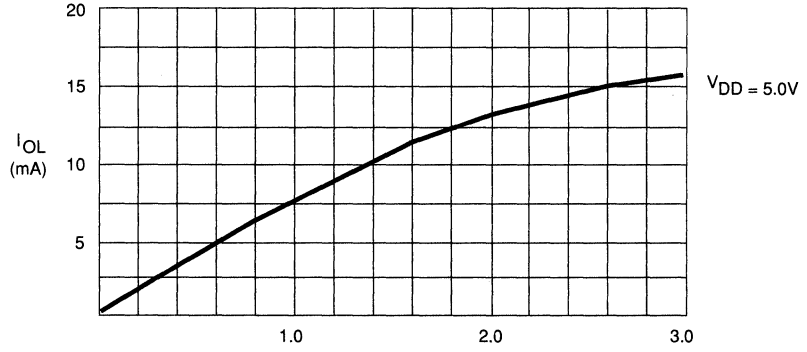


Typical Values
R = 100K
C = 0.1µf

The $\overline{MCLR}$ pin must be pulsed low for a minimum of one complete instruction cycle (t_{CY}) for the master clear function to be guaranteed, assuming that power is applied and the oscillator is running. For initial power application, a delay is required for the external oscillator time base element to start up before $\overline{MCLR}$ is brought high. To achieve this, an external RC configuration, as shown, can be used. This provides approximately a 10ms delay (assuming V_{DD} is applied as a step function), which may be insufficient for some time base elements. Consult the manufacturer of the time base element for the specific start-up times.

4

OUTPUT SINK CURRENT GRAPH (TYPICAL)



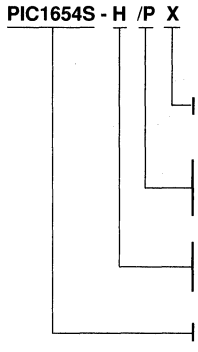
I_{OL} VS V_{OL}

$T_A = 25°C$, $V_{DD} = 5.0V$

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Pattern	3-Digit	Pattern Code
Package	P	Plastic DIP
	*SO	SOIC (Gull Wing Lead)
	*L	PLCC (J Lead)
Temperature Range	Blank	0°C to +70°C
	I	-40°C to +85°C
	H	-40°C to +110°C
Device	PIC1654S	

Notes: *SOIC and PLCC available in Commercial Temperature (0°C to +70°C) only

PIC1655

8-Bit Microcontroller

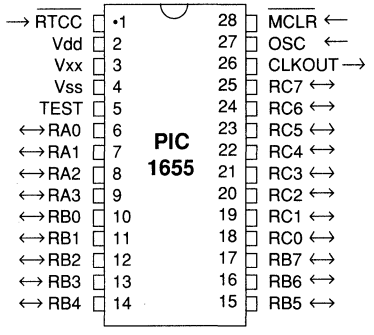
FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- External or RC input oscillator mask option
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in three temperature ranges: 0° to 70°C, -40° to 85°C and -40° to 110°C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting

PIN CONFIGURATION

28 LEAD DUAL INLINE

Top View



DESCRIPTION

The PIC®1655 microcontroller is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities for motor controls, telecommunication equipment, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1655 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, a powerful macroassembler. PICALC is available in a MS-DOS version that can be run on an IBM PC or compatible computer system. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROMless PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROM's. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-along mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

4

ARCHITECTURAL DESCRIPTION

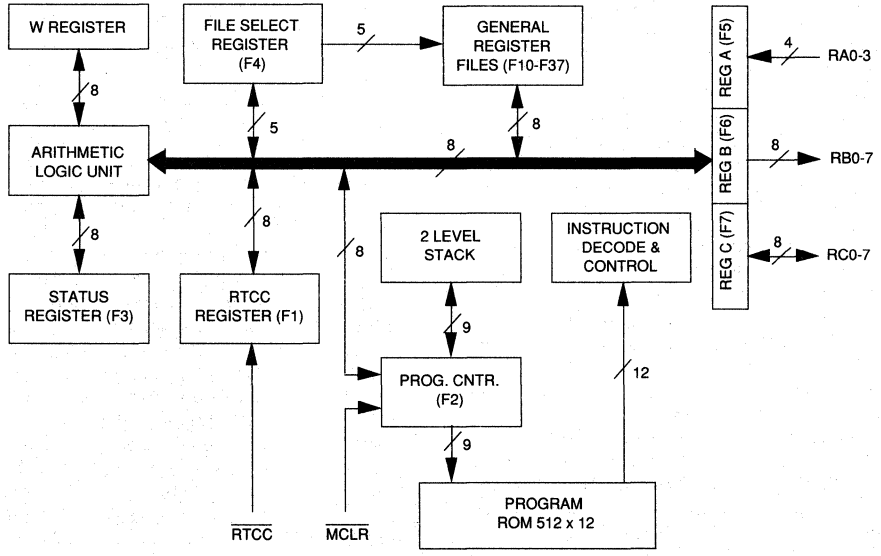
The firmware architecture of the PIC series microcontroller is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the ROM program to address 777$_8$.

PIC1655 BLOCK DIAGRAM



PIN FUNCTION TABLE

Name	Function
OSC1 (Input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
RTCC (Input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-3 (input)	4 input lines.
RB0-7 (output)	8 output lines.
RC0-7 (input/output)	8 user programmable input/output lines.
MCLR (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1 ms past the time when the power supply is valid. This is a Schmitt trigger input. RAM registers are not initialized by Master Clear
CLKOUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground.

4

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W + F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input RTCC. However, if data is being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction. (7) (6) (5) (4) (3) (2) (1) (0) 1 1 1 1 1 Z DC C C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source. DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant. Z (Zero): Set if the result of an Arithmetic operation is zero. Bits: 3-7 These bits are defined as logic ones.
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4 - A7 defined as zeros).
F6	Output Registers B (B0-B7).
F7	I/O Register C (C0-C7).
F10$_8$-F37$_8$	General Purpose Registers.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code that specifies the instruction type and one or more operands specifying the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit oriented instructions, "b" represents a bit field designator that selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight- or nine-bit constant or literal value.

For an oscillator frequency of 1 MHz the instruction execution time is 4 µsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these cases, the instruction execution time is 8 µsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

For d = 0, f → W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f → f (if d is omitted, assembler assigns d = 1).

(11-6)	(5)	(4-0)
OP CODE	d	f(FILE #)

INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
000	000	000	000	(0000)	No Operation	NOP	-	-	None
000	000	1ff	fff	(0040)	Move W to f (Note 1)	MOVWF	-	W→f	None
000	001	000	000	(0100)	Clear W	CLRW	-	0→W	Z
000	001	1ff	fff	(0140)	Clear f	CLRF	f	0→f	Z
000	010	dff	fff	(0200)	Subtract W from f	SUBWF	f,d	f-W→d [f + $\overline{W}$ + 1→d]	C,DC,Z
000	011	dff	fff	(0300)	Decrement f	DECF	f,d	f-1→d	Z
000	100	dff	fff	(0400)	Inclusive OR W and f	IORWF	f,d	Wvf→d	Z
000	101	dff	fff	(0500)	ANDbW and f	ANDWF	f,d	W•f→d	Z
000	110	dff	fff	(0600)	Exclusive OR W and f	XORWF	f,d	W ⊕ f→d	Z
000	111	dff	fff	(0700)	Add W and f	ADDWF	f,d	W + F→d	C,DC,Z
001	000	dff	fff	(1000)	Move f	MOVF	f,d	f→d	Z
001	001	dff	fff	(1100)	Complement f	COMF	f,d	f→d	Z
001	011	dff	fff	(1200)	Increment f	INCF	f,d	f + 1→d	Z
001	011	dff	fff	(1300)	Decrement f, Skip to Zero	DECFSZ	f,d	f - 1→d, skip if Zero	None
001	100	dff	fff	(1400)	Rotate Right f	RRF	f,d	f(n)→d(n-1), C→d(7), f(0)→C	C
001	101	dff	fff	(1500)	Rotate Left f	RLF	f,d	f(n)→d(n + 1), C→d(0), f(7)→C	C
001	110	dff	fff	(1600)	Swap halves f	SWAPF	f,d	f(0-3) ↔ f(4-7)→d	None
001	111	dff	fff	(1700)	Increment f, Skip if Zero	INCFSZ	f,d	f + 1→d, skip if Zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f(FILE #)

INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
010	0bb	bff	fff	(2000)	Bit Clear f	BCF	f,b	0→f(b)	None
010	1bb	bff	fff	(2400)	Bit Set f	BSF	f,b	1→f(b)	None
011	0bb	bff	fff	(3000)	Bit Test f, skip if Clear	BTFSC	f,b	Bit Test f(b): skip if clear	None
011	1bb	bff	fff	(3400)	Bit Test f, skip if Set	BTFSS	f,b	Bit Test f(b): skip if set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

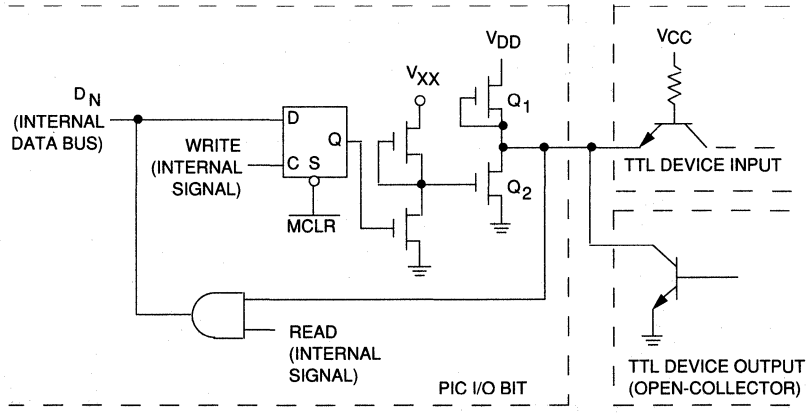
INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
100	0kk	kkk	kkk	(4000)	Return and place Literal in W	RETLW	k	k→w, Stack→PC	None
100	1kk	kkk	kkk	(4400)	Call subroutine (Note 1)	CALL	k	PC + 1→Stack, k→PC	None
101	kkk	kkk	kkk	(5000)	Go to address (k is 9 bits)	GOTO	k	k→PC	None
110	0kk	kkk	kkk	(6000)	Move Literal to W	MOVLW	k	k→W	None
110	ikk	kkk	kkk	(6400)	Inclusive OR Literal and W	IORLW	k	k v W→W	Z
111	okk	kkk	kkk	(7000)	AND Literal and W	ANDLW	k	k • W→W	Z
111	1kk	kkk	kkk	(7400)	Exclusive OR Literal and W	XORLW	k	k ⊕ W→W	Z

NOTES:
1. The 9th bit of the program counter in the PIC is zero or a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377₈. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state. See example 2 on page 7.

I/O INTERFACING

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q2, allowing the TTL open collector device to drive the pad, pulled up by Q1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Note: Q1 can be disconnected via mask option to form an "open drain" pin.

Bidirectional I/O Ports

The bidirectional ports may be used for both inut and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output latch must be set in the high state. Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an inut (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655 consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeros. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5. Also, file register instructions which leave the results in W can be used.

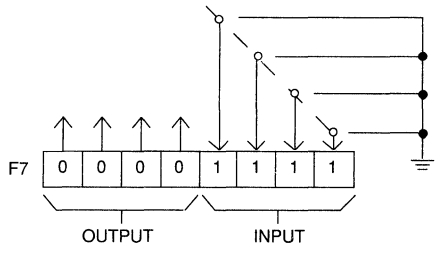
Output Only Port: (Port RB)

The output only port of the PIC1655 consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if tpd (See I.O Timing Diagram) is greater than 1/4tcy (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:

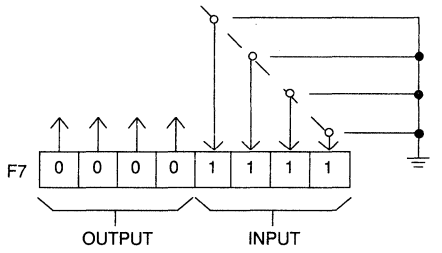


What is thought to be happening:
BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:
BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

4

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature under bias..... 125°C
Storage Temperature ..... - 55°C to +150°C
Voltage on any pin with respect
to V_{SS} ..... -0.3V to + 10.0V
Power Dissipation (Note 1) 1000mW

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS/PIC1655 Operating temperature T_A = 0°C to + 70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{CC}	4.5	-	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	65	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
		3.5	-	V_{DD}	V	I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current (MCLR, RTCC)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (open drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.4	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

DC CHARACTERISTICS/PIC1655I Operating temperature T_A = -40°C to + 85°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	70	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
						I_{OH} = 0
Output Low Voltage	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
(I/O only)		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.8	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.8	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

DC CHARACTERISTICS/PIC1655H Operating temperature T_A = -40°C to + 110``°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	5.5	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	70	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
						I_{OH} = 0
Output Low Voltage	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
(I/O only)		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (open drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.8	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.8	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

AC CHARACTERISTICS/PIC1655, PIC1655I AND PIC1655H

Operating temperature T_A = 0°C to + 70°C
-40°C to +85°C and -40°C to + 110°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	-	20	µs	0.2 MHz - 1.0MHz external time base (Notes 1, 2 and 5)
RTCC Input						
Period	t_{RT}	t_{CY} = 0.2µs-	-	-		
High Pulse Width	t_{RTH}	1/2 t_{RT}	-	-	-	
Low Pulse Width	t_{RTL}	1/2 t_{RT}	-	-	-	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	-	-	1/4t_{CY} - 125	ns	
Data Input Hold Time	t_H	0	-	-	ns	
Data Output Propagation Delay	t_{PD}	-	600	1000	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	V_{OSC} = 5V Applies to external
External Input Impedance Low	R_{OSCL}	-	10^6	-	Ω	V_{OSC} = 0.4V OSC drive only

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:
1. Instruction cycle period (t_{CY}) equals four times the inut oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the RTCC input.
3. The maximum frequency which may be input to the RTCC pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

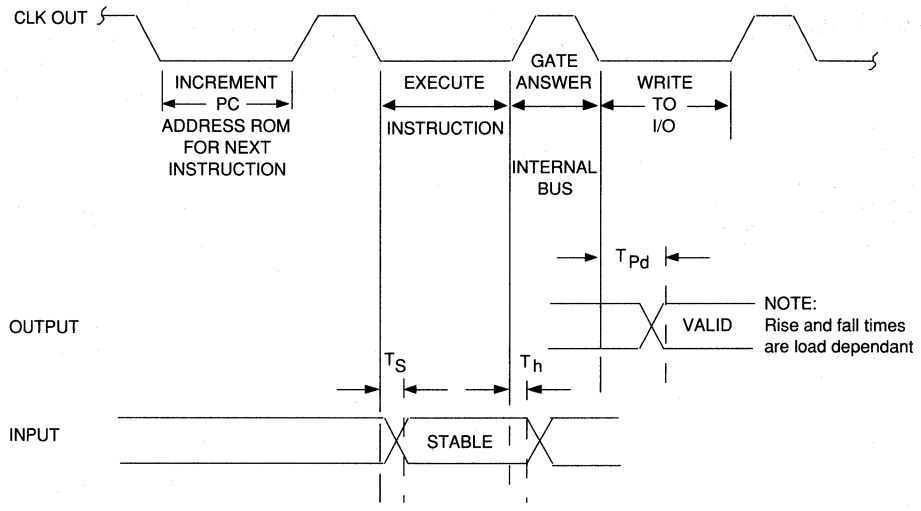
For example: if t_{CY} = 4µs, $f_{(max)} = \frac{1}{4.2\mu s}$ = 238KHz.

4. Caution must be exercised to allow for unit to unit variation of oscillator frequency when using RC option. (See RC Option Operation Graph).

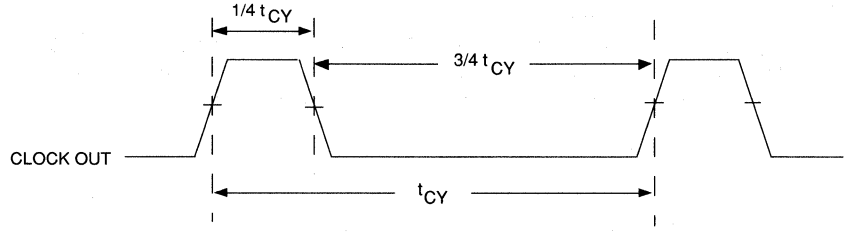
PRIMARY SUPPLY CURRENT AT SELECTED TEMPERATURES: PIC1655, PIC1655I, PIC1655H

Characteristic	Sym	Max	Units	Conditions
Primary Supply Current	I_{DD}	70	mA	-40°C, All I/O pins at V_{DD}
		65	mA	0°C, All I/O pins at V_{DD}
		48	mA	70°C, All I/O pins at V_{DD}
		45	mA	85°C, All I/O pins at V_{DD}
		42	mA	110°C, All I/O pins at V_{DD}

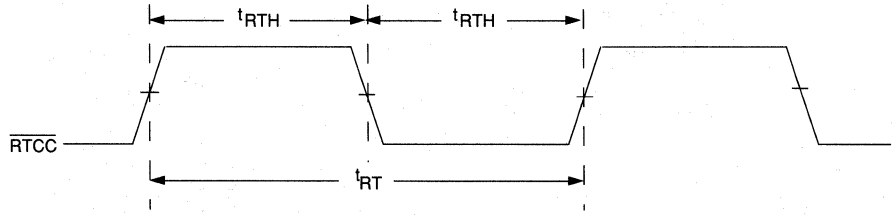
I/O TIMING



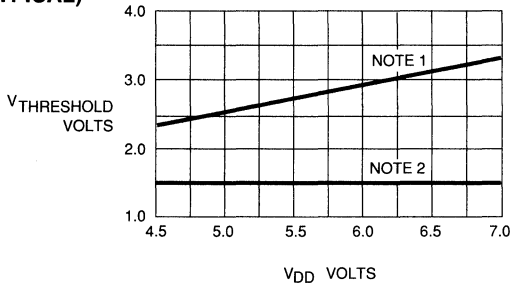
CLOCK OUT TIMING



RTCC TIMING

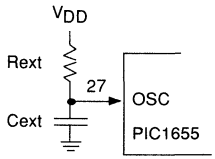


SCHMITT TRIGGER CHARACTERISTICS (RTCC, MCLR AND OSC PINS)
TA =25°C (TYPICAL)

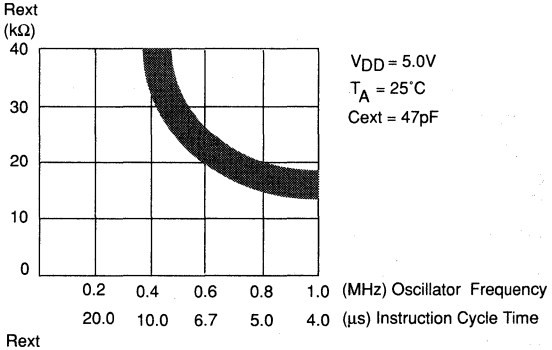


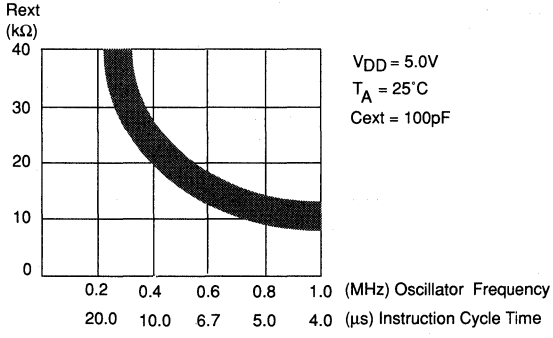
NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

RC OPTION OPERATION



TYPICAL RC OSCILLATOR FREQUENCY RANGE

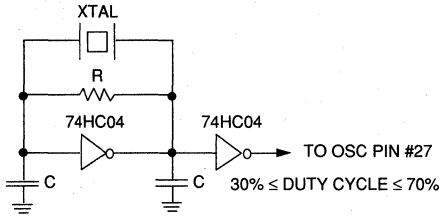




Unit to Unit Variation @ 5.0V, 25°C is ±25%
Variation from V_{DD} = 4.5V - 7.0V referenced to 5.0V is -3%, +9%
Variation from T_A = 0°C - 70°C referenced to 25°C is +3%, -5%

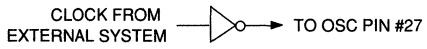
4

BUFFERED CRYSTAL INPUT OPERATION

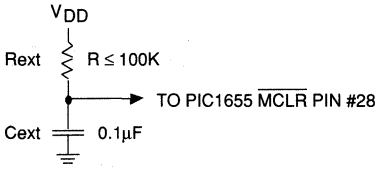


The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION

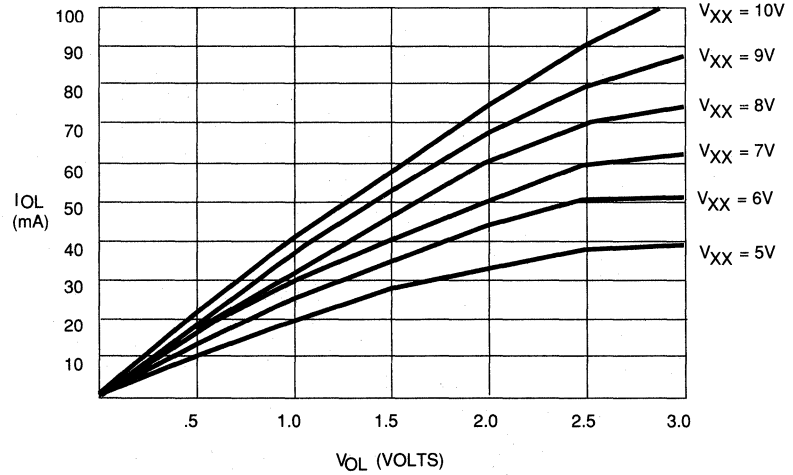


MASTER CLEAR (TYPICAL CIRCUIT)

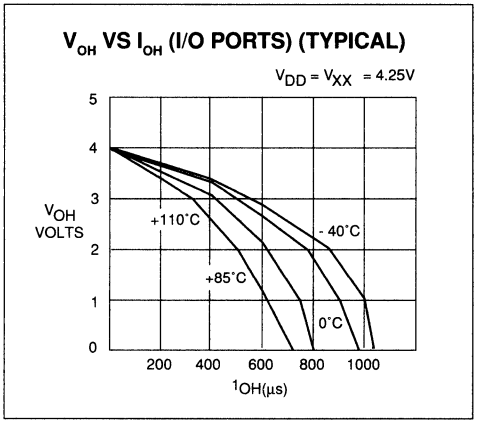


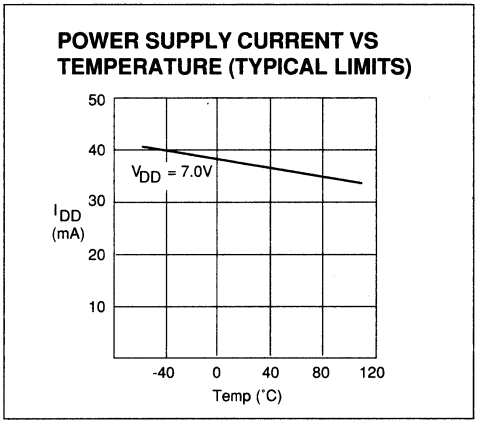
Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

OUTPUT SINK CURRENT GRAPH



The Output Sink Current is dependent on the VXX supply and the output load. This chart shows the typical curves used to express the output drive capability.





PIC1655 EMULATION CAUTIONS

When emulating a PIC1655 using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1655 mode. (Refer to the PICES Manual). The PIC1655 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{\text{MCLR}}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application the MCLR input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

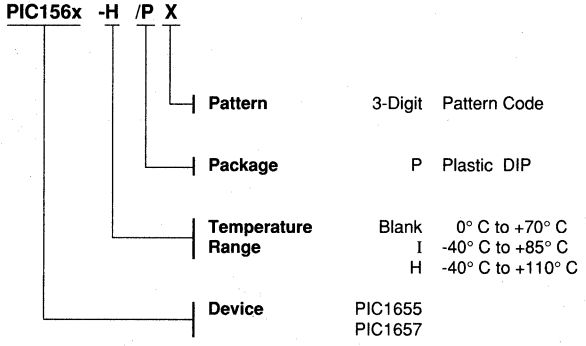
F. If an oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1655.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the sales offices. For the *currently available code-combinations*, refer to previous page.

PART NUMBERS



Microchip

PIC1670

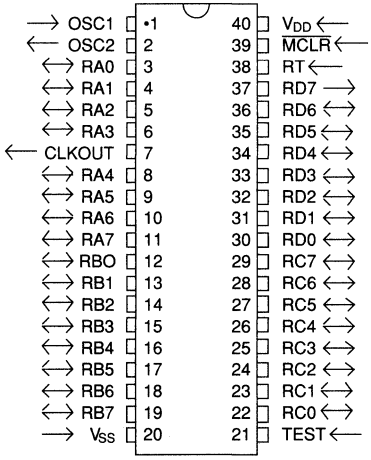
8 Bit Microcontroller

FEATURES

- 1024 x 13-bit Program ROM
- 64 x 8-bit RAM (16 special purpose registers)
- Arithmetic Logic Unit
- Sophisticated interrupt structure
- 6 level pushdown stack
- Versatile self contained oscillator
- 2.0μs instruction execution time
- Wide power supply operating range (4.5-5.5 volts)
- 4 sets of 8 user defined TTL compatible I/O lines
- Available in two temperature ranges: 0°C to 70°C and -40°C to 85°C

PIN CONFIGURATION
40 Lead Dual In Line

Top View



DESCRIPTION

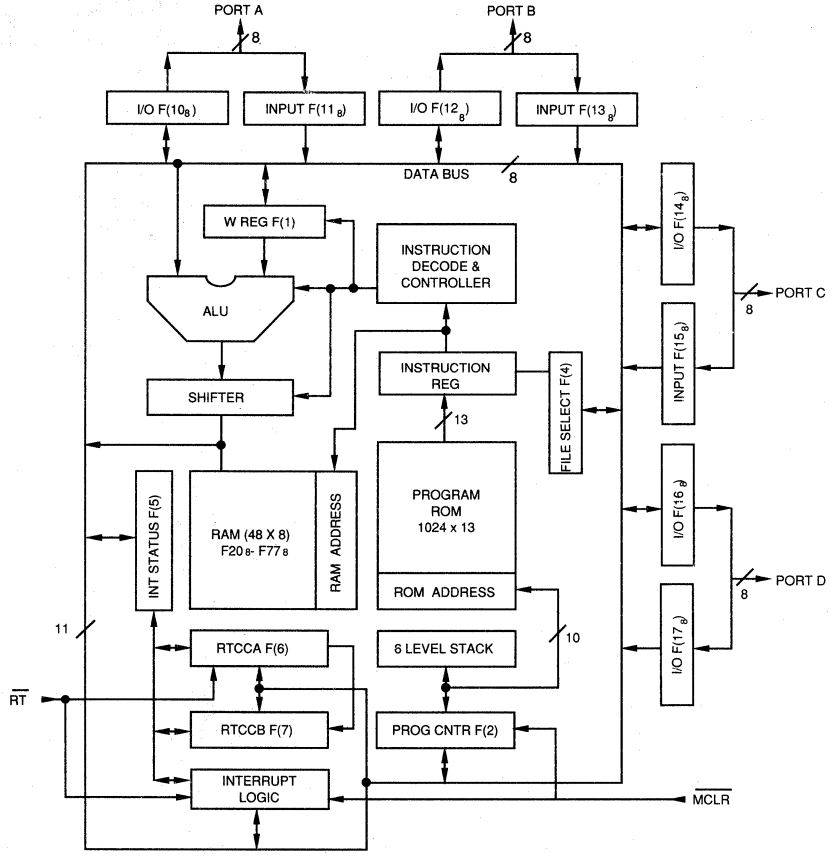
The PIC1670 microcontroller is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 13-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1670 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product. Only a single wide range power supply is required for operation. An on-chip oscillator provides the operating clock with an external crystal or ceramic resonator to establish the frequency. Inputs and outputs are TTL-compatible, with open-drain option available.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, eliminating the burden of coding with ones and zeros. Once the application program is developed, several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1665. The PIC1665 is a ROM-less PIC1670 microcontroller with additional pins to connect external EPROM or RAM and to accept HALT commands. The PFD 1020 Field Demo System is available containing a PIC1665 with sockets for erasable PROMS. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

PIC1670 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1670 microcontroller is based on a register file concept with simple yet powerful instruction commands designed to optimize the code for bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the functional blocks of the PIC1670 are connected by an 8-bit bidirectional bus: the 64 8-bit registers of which the first 16 are special purpose, an Arithmetic Logic Unit, and a user defined program ROM composed of 1024 x 13 words. The register file is divided into two functional groups: operational registers and general purpose registers. The first sixteen are the operational registers and they include the Real Time Clock Counter A and B, four I/O registers, two Status registers, a Program Counter and a File Select Register. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register (W Register), an adder, and hardware for decimal adjust. Manipulation between data in the working register and any other register can be performed.

The Program ROM contains the user defined application program and is supported by an instruction decoder and instruction register. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. The Program Counter is modified by bit test, jump, call or branch instructions and the lower 8-bits can be modified for computed addresses by file register instructions. In addition, an on-chip six level stack is employed to push and pull the contents of the program counter. This provides easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power-up initializes the ROM program to address 1777$_8$.

REGISTERS

REGISTER FILE ARRANGEMENT

File	Function
F0$_8$	Not a physical register. F0 calls for contents of the FSR (F4) to be used to select a file register. F4 is used as an indirect address pointer.
F1$_8$	W Register: The working register.
F2$_8$	Program Counter: Points to the next program ROM address to be executed (8 lower bits only).
F3$_8$	Arithmetic Status Register
F4$_8$	File Select Register: The FSR is used in generating effective file register addresses under program control.
F5$_8$	Interrupt Status Register: Used to control interrupts and registers F6 and F7. (See "Interrupt System")
F6$_8$, F7$_8$	RTCCA and RTCCB: Real Time Clock Counters A & B respectively can be configured as a single 16 bit counter, an 8 bit counter and an 8 bit general purpose register or two general purpose registers when no external counting is required. The RTCC registers can be loaded and read by the program, as well as count negative transitions on the $\overline{RT}$ pin or count at 1/8 the frequency of the oscillator . If data are being stored into RTCCA simultaneous with a negative transition on the $\overline{RT}$ pin (and CNTE = 1 and CNTS = 1), RTCCA will contain the new stored value and the external transition will be ignored by the microcomputer. (See "Real Time Clock Interrupt" for further details about the RTCC).
F10$_8$, 11$_8$	I/O Port A
F12$_8$, 13$_8$	I/O Port B
F14$_8$, 15$_8$	I/O Port C
F16$_8$, 17$_8$	I/O Port D
F20$_8$, 77$_8$	General Purpose Registers: Used for temporary and general purpose storage during program execution time.

Note: F10$_8$, 12$_8$, 14$_8$ & 16$_8$ are the I/O registers and F11$_8$, 13$_8$, 15$_8$ & 17$_8$ are used for reading the actual pin levels.

ARITHMETIC STATUS REGISTER F3

7	6	5	4	3	2	1	0
1	1	A9	A8	OV	Z	DC	C

Bit	Name	Function
0	C	Bit 0 is the carry flag and is usually the carry from the A.L.U., also used as a borrow subtract instructions.
1	DC	Bit 1 is the half carry (decimal carry) and is used to indicate a carry from bit 3 in the A.L.U. as the result of an addition (byte). This bit is used in the decimal adjust instruction to allow B.C.D. decimal addition.
2	Z	Bit 2 is the zero flag and is set to a one if the results of the previous operation was identically zero.
3	OV	Bit 3 is the overflow flag and is set to a one by operations which cause a signed two's complement arithmetic overflow. The bit is set when the carry from the MSB in the A.L.U. is opposite to the carry from the MSB-1 bit.
4	A8	Bit 4 is the 9th bit of the program counter. This bit is a read only bit.
5	A9	Bit 5 is the 10th bit of the program counter. This bit is a read only bit.

INTERRUPT STATUS REGISTER F5

7	6	5	4	3	2	1	0
0	CNTE	AVB	CNTS	RTCIR	XIR	RTCIE	XIE

BASIC INSTRUCTION SET AND PIN FUNCTIONS

Each PIC instruction is a 13-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed if "d" is zero. The result is placed in the W register if "d" is one. The result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4 MHz the instruction execution time is 2.0µsec unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 4.0µsec.

BYTE ORIENTED FILE REGISTER OPERATIONS

(12 - 7)	(6)	(5 - 0)
OPCODE	d	f(FILE #)

Instruction-Binary					(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0	000	000	000	100	(00004)	Decimal adjust W	DAW	-	(Note 1)	C
0	000	001	fff	fff	(00100)	Move W to file	MOVWF	f	W→ f	-
0	000	1d	fff	fff	(00200)	Subtract W from file w/borrow	SUBBWF	f,d	f + $\overline{W}$ + c→ d	OV,C,DC,Z
0	000	10d	fff	fff	(00400)	Subtract W from file	SUBWF	f,d	f + $\overline{W}$ + 1→ d	OV,C,DC,Z
0	000	11d	fff	fff	(00600)	Decrement file	DECF	f,d	f - 1→ d	OV,C,DC,Z
0	001	00d	fff	fff	(01000)	Inclusive or W with file	IORWF	f,d	WVf → d	Z
0	001	01d	fff	fff	(01200)	And W with file	ANDWF	f,d	W • 1→ d	Z
0	001	10d	fff	fff	(01400)	Exclusive OR W with file	XORWF	f,d	W ⊕ f → d	Z
0	001	11d	fff	fff	(01500)	Add W with file	ADDWF	f,d	W + f → d	OV,C,DC,Z
0	010	00d	fff	fff	(02000)	Add W to file with carry	ADCWF	f,d	W + f + c → d	OV,C,DC,Z
0	010	01d	fff	fff	(02200)	Complement file	COMPF	f,d	$\overline{f}$ → d	Z
0	010	10d	fff	fff	(02400)	Increment file	INCF	f,d	f + 1 → d	OV,C,DC,Z
0	010	11d	fff	fff	(02600)	Decrement file, skip if zero	DECFSZ	f,d	f • 1 → d, skip if zero	-
0	011	00d	fff	fff	(03000)	Rotate file right through carry	RRCF	f,d	f(n)→d(n - 1), c→d(7), f(0)→c	C
0	011	01d	fff	fff	(03200)	Rotate file left through carry	RLCF	f,d	f(n)→d(n + 1), c→d(0), f(7)→c	C
0	011	01d	fff	fff	(03400)	Swap upper and lower nibble of file	SWAPF	f,d	f(0-3) ↔ (4-7)→d	-
0	011	11d	fff	fff	(03600)	Increment file, skip if zero	INCFSZ	f,d	f + 1 → d, skip if zero	-
1	000	000	fff	fff	(0004)	Move file to W	MOVFW	f	f → W	Z
1	000	001	fff	fff	(00100)	Clear file	CLRF	f	0 → f	Z
1	000	010	fff	fff	(00200)	Rotate file right/no carry	RRNCF	f	f(n) → d(n-1), f(0) → f(7)	-
1	000	011	fff	fff	(00300)	Rotate file left/nocarry	RLNCF	f	f(n)→d(n + 1), f(7)→f(0)	-
1	000	100	fff	fff	(00400)	Compare file to W, skip if F < W	CPFSLT	f	f - W, skip if C = 0	-
1	000	101	fff	fff	(00500)	Compare file to W skip if F = W	CPFSEO	f	f - W, skip if Z = 1	-
1	000	110	fff	fff	(00800)	Compare file to W, skip if F> W	CPFSGT	f	f - W, skip if Z • C = 1	-
1	000	111	fff	fff	(01000)	Move file to itself	TESTF	f	f - 1	Z

Note 1: The DAW instruction adjusts the eight bit number in the W register to form two valid BCD (binary coded decimal) digits, one in the lower and in the upper nibble. (The results will only be meaningful if the number in W to be adjusted is the result of adding together two valid two digit BCD numbers). The adjustment obeys the following two step algorithm.

1. If the lower nibble is greater than 9 or the digit carry flag (DC) is set, 06 is added to the W register.
2. Then, if the upper nibble is greater than 9 or the carry from the original or step 1 addition is set, 60 is added to the W register. The carry bit is set if there is a carry from the original step 1 or step 2 addition.

BIT ORIENTED FILE REGISTER OPERATIONS

(12 - 9)	(8 - 6)	(5 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary					(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0	100	bbb	fff	fff	(04000)	Bit clear file	BCF	f,b	0 → f(b)	-
0	101	bbb	fff	fff	(05000)	Bit set file	BSF	f,b	1 → f(b)	-
0	110	bbb	fff	fff	(06000)	Bit test, skip if clear	BTFSC	f,b	Bit Test f(b),skip if clear	-
0	111	bbb	fff	fff	(07000)	Bit test,skip if set	BTFSS	f,b	Bit Test f(b), skip if set	-

LITERAL AND CONTROL OPERATIONS

(12 -8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary					(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0	000	000	000	000	(00000)	No Operation	NOP	-	-	-
0	000	000	000	010	(00002)	Return from interrupt	RETFI	-	Stack → PC	-
0	000	000	000	011	(00003)	Return from Subroutine	RETFS	-	Stack → PC	-
1	001	0kk	kkk	kkk	(11000)	Move Literal tro W	MOVLW	k	k → W	-
1	001	1kk	kkk	kkk	(11400)	Add Literal to W	ADDLW	k	k + W → W	OV,C,DC,Z
1	010	0kk	kkk	kkk	(12000)	Inclusive OR Literal to W	IORLW	k	kVW →- W	Z
1	010	1kk	kkk	kkk	(02400)	And Literal and W	ANDLW	k	k • W → W	Z
1	011	0kk	kkk	kkk	(13000)	Exclusive OR Literal to W	XCRLW	k	k W → W	Z
1	011	1kk	kkk	kkk	(13400)	Return and load literal in W	RETLW	k	k ⊕ W, Stack - PC	-
1	10k	kkk	kkk	kkk	(14000)	Go to address	GOTO	k	k → PC	-
1	11k	kkk	kkk	kkk	(16000)	Call Subroutine	CALL	k	PC + 1 → Stack, k → PC	-

PIN FUNCTIONS

Signal Name	Signal Type	Function
OSC1, OSC2	Input Output	Oscillator pins. The on-board oscillator can be driven by an external crystal ceramic resonator or an external clock via these pins.
$\overline{RT}$	Input	Real Time Input. Negative transitions on this pin increment the RTCC (F6) register. This pin can also be used for an interrupt input. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
RA0-7, RB-7, RC0-7, RD0-7	Input Output	User programmable input/output lines. These lines can be used as inputs and/ or outputs and are under direct control of the program.
$\overline{MCLR}$	Input	Master Clear: Used to initialize the internal ROM program to address 1777_8 latch all I/O registers high, and disables the interrupts. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
TEST	Input	Test pin. This pin is used for testing purposes only. It must be grounded for normal operation.
V_{DD}	-	Power supply pin.
V_{SS}	-	Ground pin.
CLKOUT	Output	Clock Output: A signal derived from the internal oscillator. May be used by external circuitry to synchronize with PIC1670 timing.

INTERRUPT SYSTEM

The interrupt system of the PIC1670 is comprised of an external interrupt and a real-time clock counter interrupt. These have different interrupt vectors, enable bits and status bits. Both interrupts are controlled by the status register (F5) shown below.

7	6	5	4	3	2	1	0
0	CNTE	A/B	CNTS	RTCIR	XIR	RTCIE	XIE

Notes: 1. Bit 7 is unused and is read as zero.
2. The Status Register F5 will power up to all zeroes.

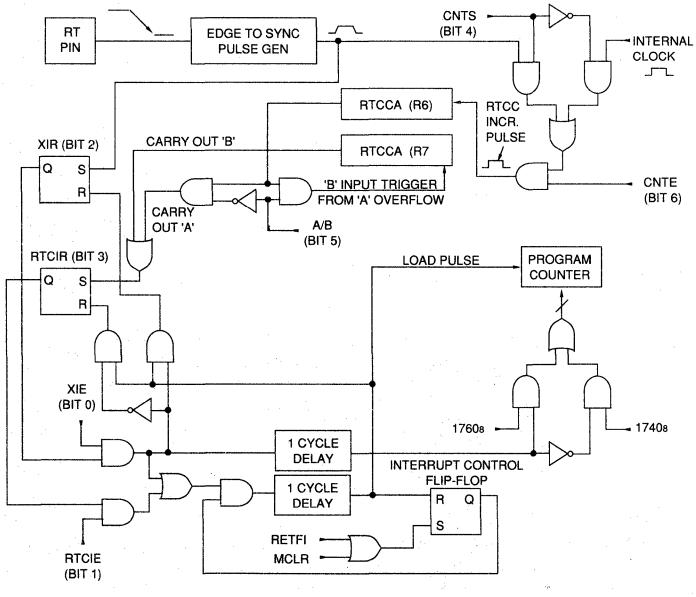
External Interrupt

On any high to low transition of the $\overline{RT}$ pin the external interrupt request (XIR) bit will be set. This request will be serviced if the external interrupt enable (XIE) bit is set or if it is set at a later point in the program. The latter allows the processor to store a request (without interrupting) while a critical timing routine is being executed. Once external interrupt service is initiated, the processor willclear the XIR bit, delay one cycle (to execute the current instruction), then push the current program counter onto the stack and execute the instruction at location 1760_8. It takes three to four instruction cycles from the transition on the $\overline{RT}$ pin until the instruction at 1760_8 is executed. No new interrupts can be serviced until a return from interrupt (RETFI) instruction has been executed.

Real-Time Clock Interrupt

The real-time clock counter (RTCCA & RTCCB, file registers F6 and F7) have a similar mechanism of interrupt service. The RTCCA register will increment if the count enable (CNTE) bit is set: If this bit is not set the RTCCA & RTCCB will maintain their present contents and can therefore be used as general purpose RAM registers. The count source (CNTS) bit selects the clocking source for RTCCA. If CNTS is cleared to a '0', then RTCCA will use the internal instruction clock and increment at 1/8 the frequency present on the OSC pins. If CNTS is set to a '1', then RTCCA will increment on each high to low transition of the RT pin. RTCCB can only be incremented when RTCCA makes a transition from 377_8 to 0 and the A/B status bit is set. This condition links the two eight bit registers together to form one sixteen bit counter. An interrupt request under these conditions will occur when the combined registers make a transition from 177777_8 to 0. If, however, the A/B bit is not set, then RTCCA will be the only incrementing register and an interrupt request will occur when RTCCA makes a transition from 377_8 to 0. (In this setup the RTCCB register will not increment and can be used as a general purpose RAM register). Once a request has come from the real-time clock counter, the real-time clock interrupt request (RTCIR) bit will be set. At this point, the request can either be serviced immediately if the real-time clock interrupt enable (RTCIE) bit is set or be stored if RTCIE is not set. The latter allows the

INTERRUPT SYSTEM BLOCK DIAGRAM



Interrupt System (Cont.)

processor to store a real-time clock interrupt while a critical timing routine is being executed. Once interrupt service is initiated, the processor will clear the RTCIR bit, delay one cycle (to execute the current instruction), then push the present program counter onto the stack and execute the instruction at location 1740$_8$. It takes three instruction cycles from when the RTCC(A or B) overflows until the instruction 1740$_8$ is executed. No new interrupts can be serviced until a RETFI instruction has been executed.

The RETFI instruction (00002$_8$) must be used to return from any interrupt service routine if any pending interrupts are to be serviced. External interrupts have priority over RTCC driven interrupt in the event both types occur simultaneously. Interrupts cannot be nested but will be serviced sequentially. The existance of any pending interrupts can be tested via the state of the XIR (bit 2) and RTCIR (bit 1) in the status word F5.

INPUT/OUTPUT CAPABILITY

The PIC1670 provides four complete quasi-bidirectional input/output ports. A simplified schematic of an I/O pin is shown below. The ports occupy address locations in the register file space of the PIC1670. Thus, any instruction that can operate on a general purpose register can operate on an I/O port. Two locations in the register file space are allocated for each I/O port. Port RA0-7 is addressable as either F10$_8$ or F11$_8$. Port RB0-7 is addressable as either F12$_8$ or F13$_8$. Port RC0-7 is addressable as either F14$_8$ or F15$_8$. An I/O port READ on its odd-numbered location will interrogate the chip pins while an I/O port READ on its even-numbered location will interrogate the internal latch in that I/O port. This simplifies programming in cases where a portion of a single port is used for inputting only while the remainder is used for outputting as illustrated in the following example.

Here, the low 3 bits of port RA are used as output-only, while the high 5 bits are used as input-only. During power on reset ($\overline{MCLR}$ low), the latches in the I/O ports will be set high, turning off all pull down transistors as represented by Q 2 in the figure below. During program execution if we wish to interrogate an input pin, then, for example,

```
BTFSS 11,6
```

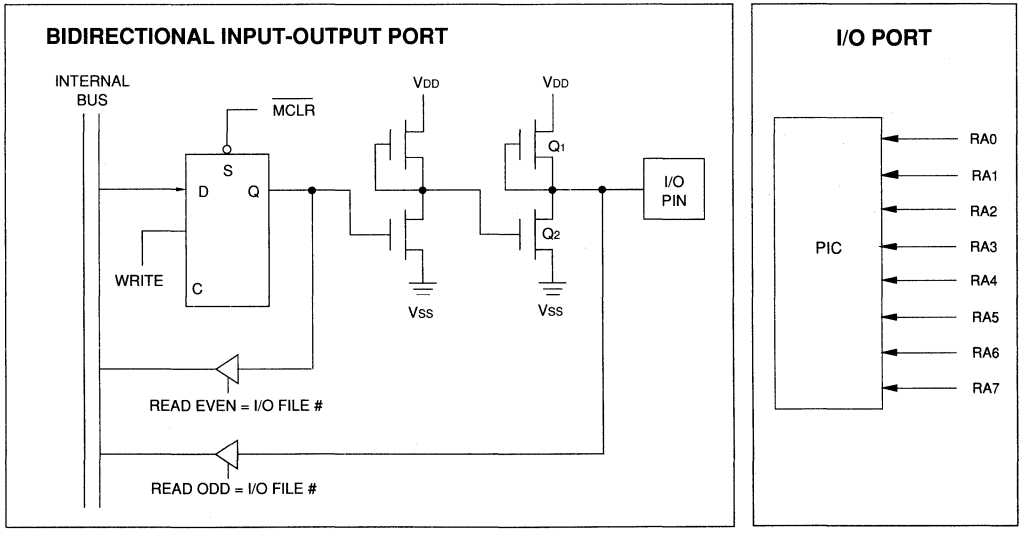
will test pin RA6 and skip the next instruction if that pin is set. If we wish to modify a single output, then, for example,

```
BCF 10, 2
```

will force RA2 to zero because its internal latch will be cleared to zero. This will turn on Q2 and pull the pin to zero.

The way this instruction operates internally is the CPU reads file 10 into the A.L.U., modifies the bit and re-outputs the data to file 10. If the pins were read instead, any input which was grounded externally would cause a zero to be read on that bit. When the CPU re-outputted the data to the file, that bit would be cleared to zero, no longer useful as an input until set high again.

During program execution, the latches in bits 3-7 should remain in the high state. This will keep Q2 off, allowing external circuitry full control of pins RA3-RA7, which are being used here as input.



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... - 55°C to +150°C
Voltage on any pin with
respect to Vss ..... -0.3V to +10.0V
Power Dissipation 1000mW

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Operating temperature:
- Commercial: T_A = 0 °C to + 70 °C
- Industrial: T_A = -40 °C to + 85 °C

Characteristic	Sym	Min	Typ*	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	-	5.5	V	
Primary Supply Current	I_{DD}	-	-	100	mA	All I/O pins high
Input Low Voltage (except $\overline{MCLR}$ & $\overline{RT}$)	V_{IL}	V_{SS}	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH1}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH2}	V_{DD}-1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} - 100 µA provided by internal pullups (Note 2)
Output Low Voltage (I/O and CLK OUT)	V_{OL}	-	-	0.45	V	I_{OL} = 1.6mA
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$, OSC1)	I_{LC}	-5	-	+5	µA	$V_{SS} = V_{IN} - V_{DD}$
Input Low Current (All I/O ports)	I_{IL}	-0.2	-0.6	-2.0	mA	V_{IL} = 0.4V internal pullup
Input High Current (All I/O ports)	I_{IH}	-0.1	-0.4	-	mA	V_{IH} = 2.4V

* Typical data is at T_A = 25°C, V_{DD} = 0V.

Notes: 1. Total power dissipation for the package is calculated as follows:
$P_O = (V_{DD})(I_{DD}) + \Sigma\{(V_{DD} - V_{IL}) \cdot |V_{IL}|\} + \Sigma\{(V_{DD} - V_{OH}) \cdot |I_{OH}|\} + \Sigma\{(V_{OL}) \cdot I_{OL}\}$.
2 Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pin (I/O ports plus CLK OUT) must not exceed 175mA.

AC CHARACTERISTICS

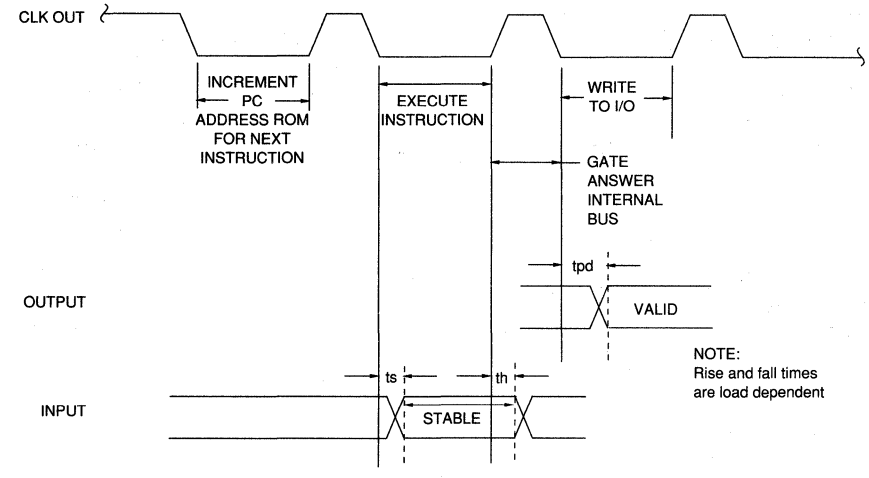
Operating temperature:
- Commercial: T_A = 0 °C to + 70 °C
- Industrial: T_A = -40 °C to + 85 °C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	2.0	-	8	µs	4 MHz external time base (Notes 1, 2, 4))
$\overline{RT}$ input						(Note 3)
Period - Commercial	t_{RT}	t_{CY}+175ns	-	-	-	Commercial: T_A = 70°C
Period -Industrial	t_{RT}	t_{CY}+200ns	-	-	-	Industrial: T_A = 85°C
High Pulse Width	t_{RTH}	1/2t_{RT}	-	-	-	Commercial: T_A = 70°C
Low Pulse Width	t_{RTL}	1/2t_{RT}	-	-	-	Commercial: T_A = 70°C
I/O Ports						
Data Input Setup Time	t_R	-	-	1/4t_{CY} - 125	ns	
Data Input Hold Time	t_H	0	-	-	ns	
Data Output Propagation Delay	t_{RT}	-	500	800	ns	Capacitance load = 50pF

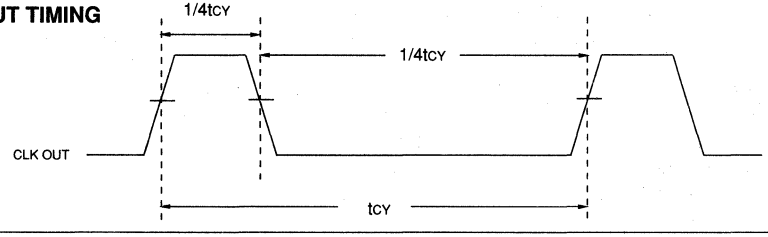
Notes:
1. Instruction cycle period (t_{CY}) equals eight times the oscillator time base period.
2. The oscillator frequency may deviate to 4.08 MHz to allow for tolerance of the time base element (LC, crystal, or ceramic resonator).
3. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input. The minimum times specified represent theoretical limits.
4. The maximum frequency which may be input to the $\overline{RT}$ pin is calculated as follows: $f_{max} = \frac{1}{t_{RTmin}} = \frac{1}{t_{CYmin}+\delta}$
   where: ∂=175 ns for Commercial
   ∂=200 ns for Industrial
   Examples: Commercial: if t_{CY} = 2µs, $f_{(max)}$ = 1/2.175 µs = 460 KHz
   Industrial: if t_{CY} = 2µs, $f_{(max)}$ = 1/2.2µs = 455 KHz.

4

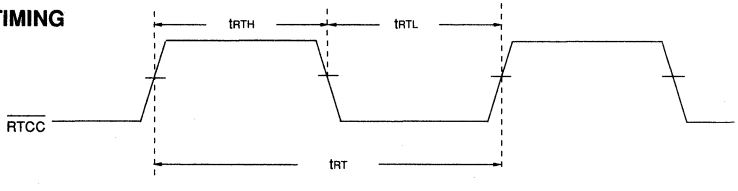
I/O TIMING



CLK OUT TIMING

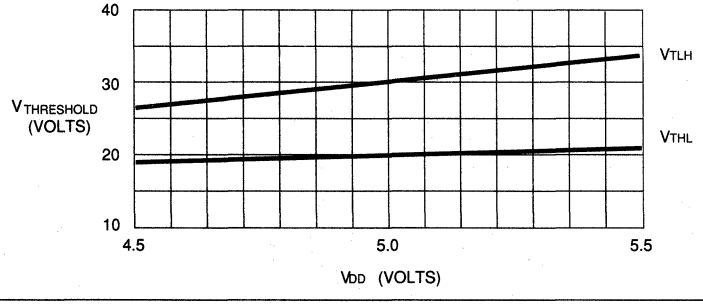


$\overline{\text{RTCC}}$ TIMING



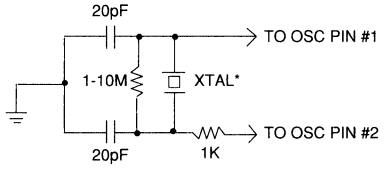
SCHMITT TRIGGER CHARACTERISTICS (TYPICAL)

(RT, MCLR) T_A = 25°C



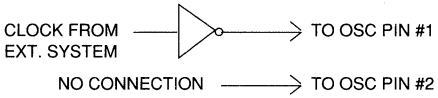
TYPICAL OSCILLATOR CIRCUITS

CRYSTAL INPUT OPERATION

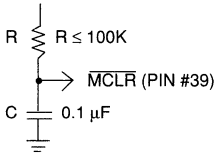


* OR CERAMIC RESONATOR,
PARALLEL RESONANT
(1.0 - 4.0 MHz)

EXT. INPUT OPERATION

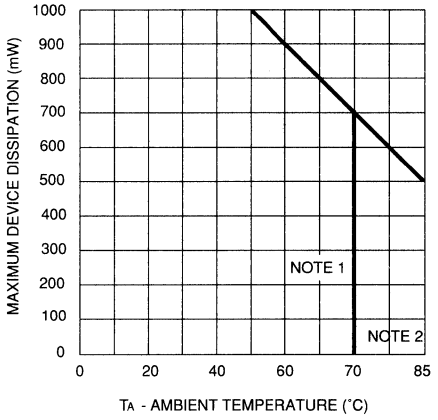


MASTER CIRCUIT (TYPICAL)



Note: The $\overline{MCLR}$ pin must be pulsed low for a minimum of one complete instruction cycle (tCY) for the master clear function to be guaranteed, assuming that power is applied and the oscillator is running. For initial power application, a delay is required for the external oscillator time base element to start up before $\overline{MCLR}$ is brought high. To achieve this, an external RC configuration as shown can be used. This provides approximately a 10 ms delay (assuming VDD is applied as a step function), which may be insufficient for some time base elements. Consult the manufacturer of the time base element for specific start-up times.

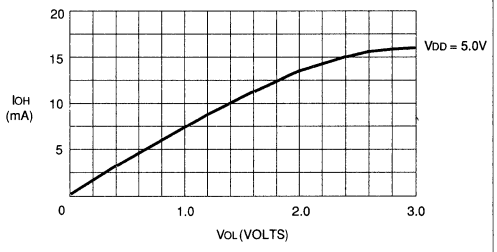
POWER DISSIPATION DERATING GRAPH



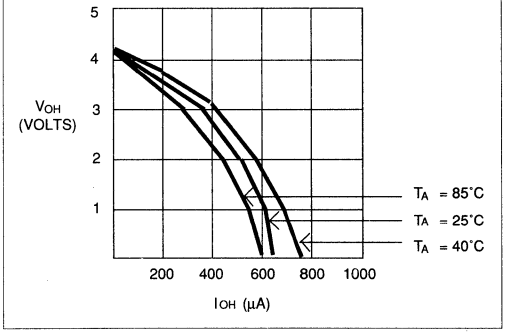
Notes: 1. 70°C is the maximum operating temperature for standard parts.

2. 85°C is the maximum operating temperature for "I" suffix parts.

OUTPUT SINK CURRENT GRAPH



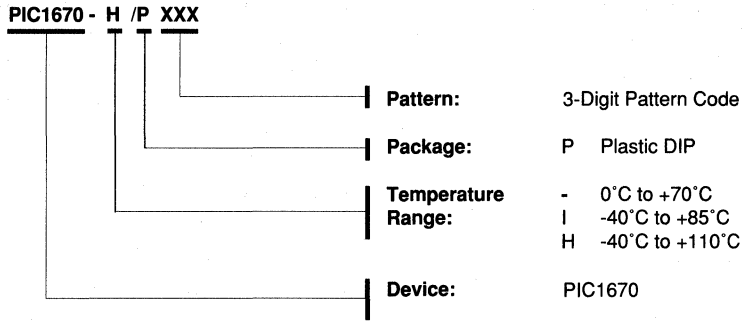
VOH VS IOH (I/O PORTS) (TYPICAL)



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



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SECTION 5
LOGIC PRODUCT SPECIFICATIONS

Microchip

AY2661

Enhanced Programmable Communication Interface

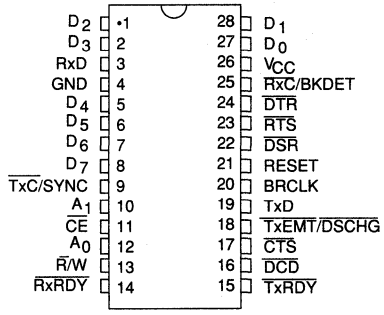
FEATURES

- Synchronous and Asynchronous full or half duplex operation
- On-chip baud rate generator - 3 standards
- Double buffering of data
- TTL compatible
- Single +5 volt power supply
- Compatible with SC2661, COM2661

PIN CONFIGURATION

28 LEAD DUAL INLINE

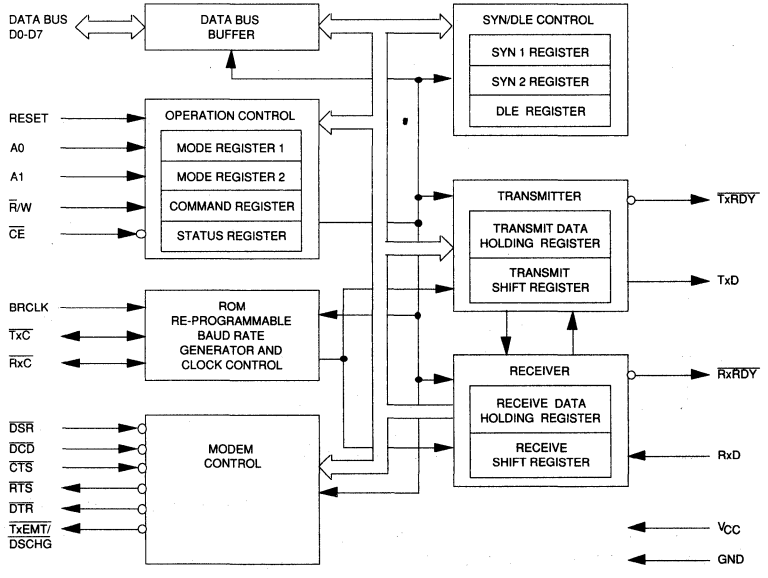
Top View



DESCRIPTION

The AY2661 is a universal synchronous /asynchronous receiver/transmitter designed for microcomputer system data communications. It may be programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including Bi-Sync. The AY2661 receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the device will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The AY2661 will signal the processor when it has completely received or transmitted a character and requires service. Complete status information including data format errors and control signals is available to the processor at any time.

AY2661 BLOCK DIAGRAM



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PIN FUNCTIONS

Pin Name	Function
BRCLK	Clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{\text{R x C}}$/BKDET	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
$\overline{\text{T x C}}$/XSYNC	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a1X/16X clock output for an external jam synchronization input.
R x D	Serial data input to the receiver. "Mark" is high, "space" is low.
T x D	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{\text{DSR}}$	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. It causes a low output on $\overline{\text{TxEMT/DSCHG}}$ when its state changes and CR2 or CR0 = 1.
$\overline{\text{DCD}}$	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{\text{TxEMT/DSCHG}}$ when its state changes and CR2 or CR0 = 1. If $\overline{\text{DCD}}$ goes high while receiving, the R x C is internally inhibited.
$\overline{\text{CTS}}$	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{\text{DTR}}$	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{\text{RTS}}$	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. If the transmit shift register is not empty when CR5 is reset (1 to 0), then $\overline{\text{RTS}}$ will go high one T x C time after the last serial bit is transmitted.
RESET	A high on this input performs a master reset on the AY2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1 - A_0	Address lines used to select internal EPCI registers.
$\overline{\text{R/W}}$	Read command when low, write command when high.
$\overline{\text{CE}}$	Chip enable command. When low, indicates that control and data lines to the EPCI are valid and that the operation specified by the $\overline{\text{R/W}}$, A_1 and A_0 inputs should be performed. When high, places the D_0 - D_7 lines in the three-state condition.

PIN FUNCTIONS (CONTINUED)

Pin Name	Function
D_7 - D_0	8-bit, three-state data bus used to transfer commands, data and status between EPCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{T \times RDY}$	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{R \times RDY}$	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT/DSCHG}$	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occured. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

AY2661 OPERATION

The functional operation of the AY2661 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc.

Receiver

The AY2661 is conditioned to receive data when the DCD input is low and RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the Receive Data Holding Register, the $\overline{RxRDY}$ bit in the status register is set, and the RxRDY output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the AY2661 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set.

Otherwise, the AY2661 returns to the hunt mode. (note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been acheived, the AY2661 continues to assemble charac-

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ters and transfers them to the Holding Register. The RxRDY status bit is set and the $\overline{\text{RxRDY}}$ output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Transmitter

The AY2661 is conditioned to transmit when the $\overline{\text{CTS}}$ input is low and the TxEN command register bit is set. The AY2661 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{\text{TxRDY}}$ output. When the processor writes a character into the Transmit Data Holding Register, the $\overline{\text{TxRDY}}$ status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT/DSCHG}}$ output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the AY2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity if commanded) are generated by the AY2661 unless the processor fails to send a new character to the AY2661 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the AY2661 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, and SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

AY2661 Programming

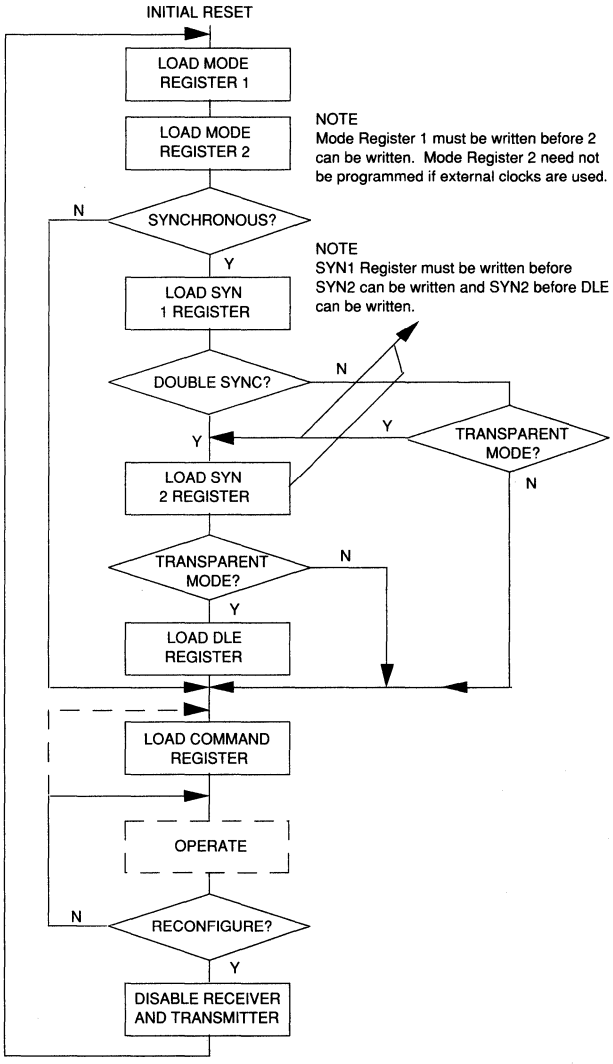
Prior to initiating data communications, the AY2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The AY2661 can be reconfigured at any time during program execution. A flow chart of the initialization process follows.

The internal registers of the AY2661 are accessed by applying specific signals to the $\overline{\text{CE}}$, $\overline{\text{R}}$/W A1 and A0 inputs. The conditions necessary to address each register are shown in Fig. 3.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and $\overline{\text{R}}$/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1 and subsequent operation addressed Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The AY2661 register formats are summarized in Tables 6, 7, 8 and 9. Mode Registers 1 and 2 define the general operational characteristics of the AY2661, while the Command Register controls the operation within this basic framework. The AY2661 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

AY2661 INITIALIZATION FLOW CHART



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AY2661 REGISTER ADDRESSING

CE	A1	A0	R/W	Function
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1 and 2
0	1	0	1	Write mode registers 1 and 2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

MODE REGISTER 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop Bit Length 00 = Invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double Syn 1 = Single Syn	**Sync: Transparency Control** 0 = Normal 1 = Transparent						

NOTE
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected.

MODE REGISTER 2 (MR2)

MR27 - MR24					MR23 - MR20					
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	Sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	Async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	Sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	Async	See baud rates in baud rate standards
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	Sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	Async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	Sync	
0111	I	I	16X	16X	1110	I	I	16X	BKDET	Async	

NOTES
1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-2, and DLE-SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs

COMMAND REGISTER (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request To Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic echo mode Sync: SYN and/ or DLE stripping mode 10 = Local loop back 11 = Remote loop back		0 = Force $\overline{RTS}$ output high one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, OE, PE/DLE detect).	Async: Force break 0 = Normal 1 = Force break Sync: Send DLE 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable	0 = Force $\overline{DIR}$ output high 1 = Force $\overline{DIR}$ output low	0 = Disable 1 = Enable

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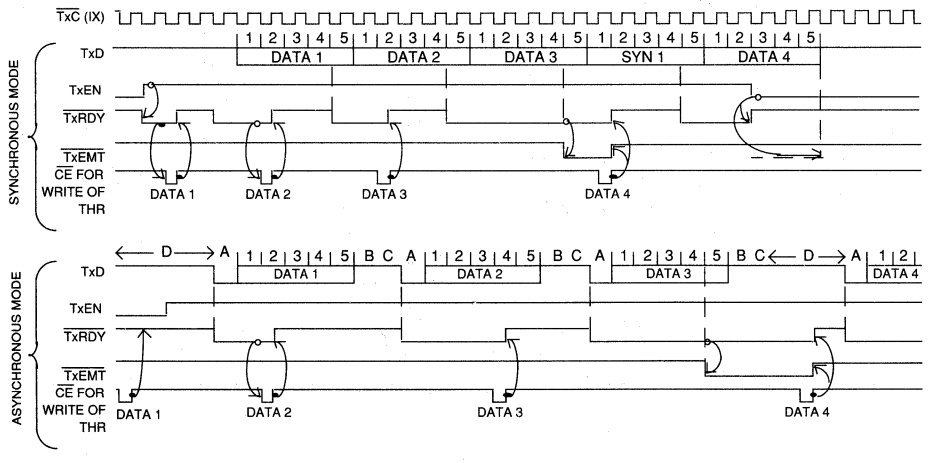
STATUS REGISTER (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/ DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	Async: 0 = Normal 1 = Framing Error	0 = Normal 1 = Overrun Error	Async: 0 = Normal 1 = Parity Error	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty
		Sync: 0 = Normal 1 = SYN CHAR detected		Sync: 0 = Normal 1 = Parity error or DLE received			

TIMING DIAGRAMS

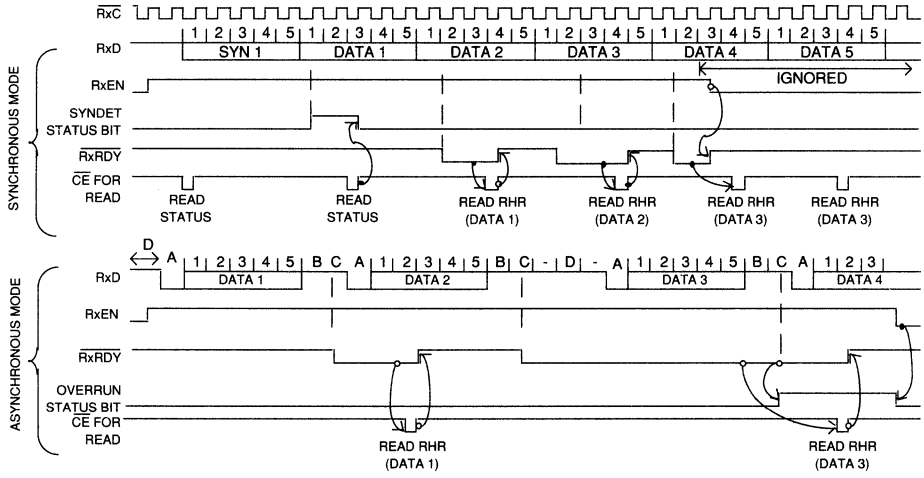
TxRDY, TxEMT (shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode]



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit or if parity is enabled at the beginning of the parity bit

TIMING DIAGRAMS (Cont.)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

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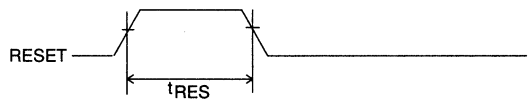
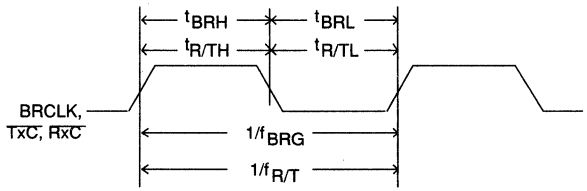
TIMING DIAGRAMS (Cont.)

RESET

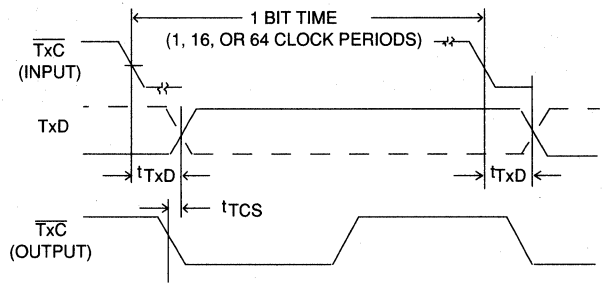


CLOCK

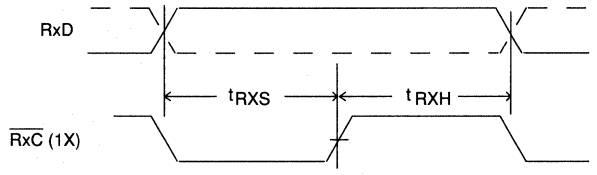


TIMING DIAGRAMS (Cont.)

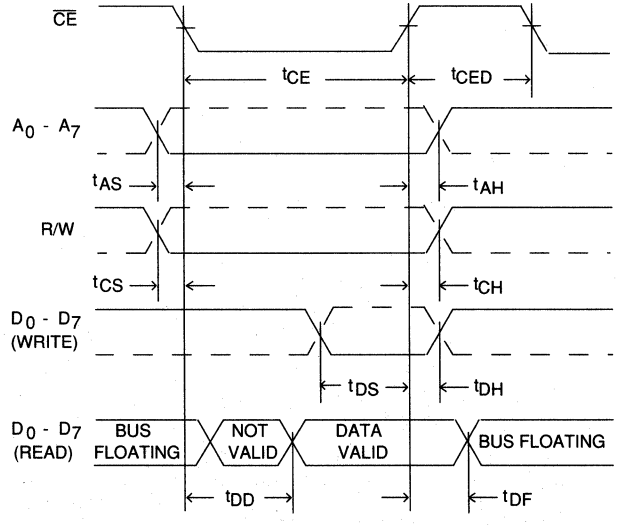
TRANSMIT



RECEIVE

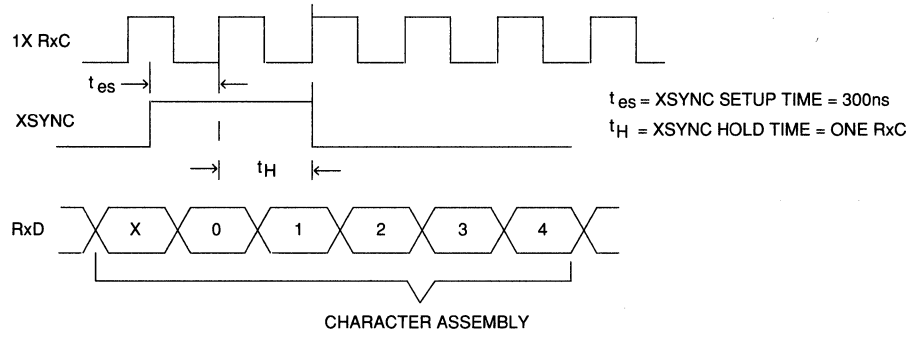


READ AND WRITE

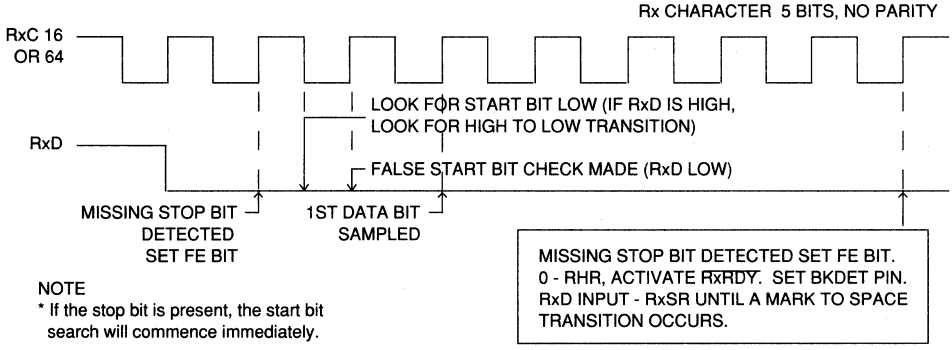


TIMING DIAGRAMS (Cont.)

EXTERNAL SYNCHRONIZATION WITH XSYNC



BREAK DETECTION TIMING



NOTE
* If the stop bit is present, the start bit search will commence immediately.

ELECTRICAL CHARACTERISTICS

Maximum Guaranteed Ratings*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... - 55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin,
with respect to ground ..... +18.0V
Negative Voltage on any Pin,
with respect to ground ..... -0.3V

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Operating temperature T_A = 0°C to + 70°C, V_{CC} = 5.0V +5%

Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Input Voltage						
Low	V_{IL}	-	-	0.8	V	
High	V_{IH}	2.0	-	-	-	
Output voltage						
Low	V_{OL}	-	-	0.4	V	I_{OL} = 2.2mA
High	V_{OH}	2.4	-	-	-	I_{OH} = 400µA
Input leakage current	I_{IL}	-	-	10	µA	V_{IN} = 0 to 5.5V
Output leakage current						
Data bus high	I_{LH}	-	-	10	µA	V_O = 4.0V
Data bus low	I_{LL}	-	-	10	µA	V_O = 0.45V
Power supply current	I_{CC}	-	-	150	mA	
Capacitance						
Input	C_{IN}	-	-	20	pF	fc = 1MHz
Output	C_{OUT}	-	-	20	pF	Unmeasured pins tied
Input/Output	C_{IO}	-	-	20	pF	to ground

AC CHARACTERISTICS

Operating temperature T_A = -0°C to +70°C, V_{CC} = 5.0V +5%

Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
Pulse Width						
Reset	t_{RES}	1000	-	-	ns	
Chip enable	t_{CE}	250	-	-	ns	
Setup and hold time						
Address setup	t_{AS}	10	-	-	ns	
Address hold	t_{AH}	10	-	-	ns	
R/W control setup	t_{CS}	10	-	-	ns	
R/W control hold	t_{CH}	10	-	-	ns	
Data setup for write	t_{DS}	150	-	-	ns	
Data hold for write	t_{DH}	0	-	-	ns	
Rx data setup	t_{RXS}	300	-	-	ns	
Rx data hold	t_{RXH}	350	-	-	ns	
Data delay time for read	t_{DD}	-	-	200	ns	C_L = 150pF
Data bus floating time for read	t_{DF}	-	-	100	ns	C_L = 150pF
CE to CE delay	t_{CED}	600	-	-	ns	
Input clock frequency						
Baud rate generator (2661-1, -2)	f_{BRG}	1.0	4.9152	4.9202	MHz	
Baud rate generator (2661-3)	f_{BRG}	1.0	5.0688	5.0738	MHz	
TxC or RxC	f_{RT} [1]	dc	-	1.0	MHz	
Clock width						
Baud rate high (2661-1, -2)	t_{BRH}	75	-	-	ns	f_{BRG} = 4.915MHz; measured at V_{IH}
Baud rate high (2661-3)	t_{BRH}	70	-	-	ns	f_{BRG} = 5.0688MHz; measured at V_{IH}
Baud rate low (2661-1, -2)	t_{BRL}	75	-	-	ns	f_{BRG} = 4.915MHz; measured at V_{IL}
Baud rate low (2661-3)	t_{BRL}	70	-	-	ns	f_{BRG} = 5.0688MHz; measured at V_{IL}
TxC or RxC high	t_{RTH1}	480	-	-	ns	
TxC or RxC low	t_{RTL}	480	-	-	ns	
TxD delay from falling edge of TxC	t_{TXD}	-	-	650	ns	C_L = 150pF
Skew between TxD changing and falling edge of TxC output	t_{TCS}	-	0	-	ns	C_L = 150pF

NOTE:

1. f_{RT} and t_{RTL} shown for all modes except Local Loopback. For Local Loopback mode f_{RT} = 0.7MHz and t_{RTL} = 700ns min.

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BAUD RATE STANDARDS

AY2661-A
(BRCLK = 4.9152MHz)

MR23-20	Baud Rate	Actual Frequency 16X Clock	Percent Error	Divisor
0000	50	0.8kHz	-	6144
0001	75	1.2	-	4096
0010	110	1.7598	-0.01	2793
0011	134.5	2.152	-	2284
0100	150	2.4	-	2048
0101	200	3.2	-	1536
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	-	256
1010	1800	28.7438	-0.19	171
1011	2000	31.9168	-0.26	154
1100	2400	38.4	-	128
1101	4800	76.8	-	64
1110	9600	153.6	-	32
1111	19200	307.2	-	16

AY2661-B
(BRCLK = 4.9152MHz)

MR23-20	Baud Rate	Actual Frequency 16X Clock	Percent Error	Divisor
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	-	6144
0010	75	1.2	-	4096
0011	110	1.7598	-0.01	2793
0100	134.5	2.152	-	2284
0101	150	2.4	-	2048
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1200	19.2	-	256
1001	1800	28.7438	-0.19	171
1010	2000	31.9168	-0.26	154
1011	2400	38.4	-	128
1100	4800	76.8	-	64
1101	9600	153.6	-	32
1110	19200	307.2	-	16
1111	38400	614.4	-	8

BAUD RATE STANDARDS (CONT.)

AY2661-C
(BRCLK = 5.0688MHz)

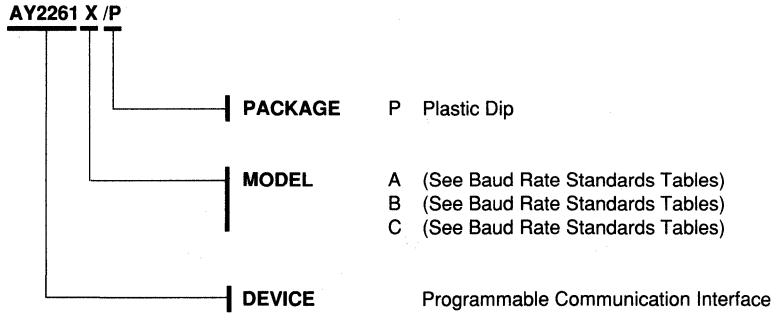
MR23-20	Baud Rate	Actual Frequency 16X Clock	Percent Error	Divisor
0000	50	0.8kHz	-	6336
0001	75	1.2	-	4224
0010	110	0.76	-	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	-	2112
0101	300	4.8	-	1056
0110	600	9.6	-	528
0111	1200	19.2	-	264
1000	1800	28.8	-	176
1001	2000	32.081	-0.253	158
1010	2400	38.4	-	132
1011	3600	57.6	-	88
1100	4800	76.8	-	66
1101	7200	115.2	-	44
1110	9600	153.6	-	33
1111	19200	316.8	3.125	16

NOTE
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



AY31015D

UAR/T: UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

FEATURES

- DTL and TTL compatible - no interfacing circuits required - drives one TTL load
- Fully Double Buffered - eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation - can handle multiple bauds (receiving - transmitting) simultaneously
- Start Bit Verification - decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs - bus structure capability
- Low Power - minimum power requirements
- Input Protected - eliminates handling problems
- Single Supply Operation: +4.75V to +5.25V
- 1 1/2 stop bit mode
- External reset of all registers except control bits register
- N-channel Ion Implant Process
- 0 to 25K baud
- Pull-up resistors to Vcc on all inputs

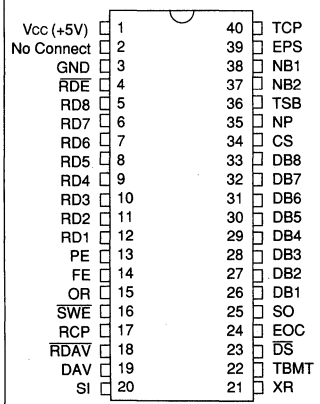
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, 1, 1-1/2, or 2 stop bit capability, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

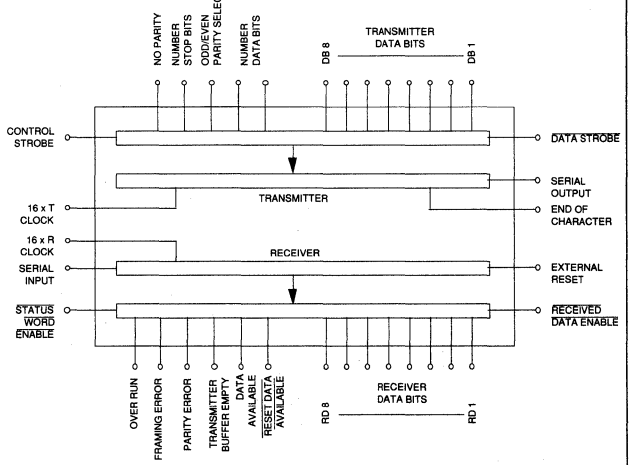
PIN CONFIGURATION

40 LEAD DUAL INLINE

Top View



AY31015D BLOCK DIAGRAM



PIN FUNCTIONS

Pin Number	Signal Name	Input/ Output	Function
1	VCC	I	VCC Power Supply: +5V Supply
2	N.C.	-	(Not Connected)
3	Ground	-	Ground
4	$\overline{RDE}$		$\overline{Received\ Data\ Enable}$: A logic "0" on this input places the received data onto the output lines (RD8..RD1).
5-12	RD8..RD1	I	Received Data Bits: These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{RDE}$ is "0" and a high impedence state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	PE	O	Parity Error: This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state when $\overline{SWE}$ (pin 16) is "1".
14	FE	O	Framing Error: This line goes to a logic "1" if the received character has no valid stop bit. Tri-state when $\overline{SWE}$ (pin 16) is "1".
15	OR	O	Over-Run: This line goes to a logic "1"if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state when $\overline{SWE}$ (pin 16) is "1".
16	$\overline{SWE}$	I	$\overline{Status\ Word\ Enable}$: A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. A logic "1" puts the status word bit outputs into a high impedance state.
17	RCP	I	Receiver Clock: This input line requires a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAV}$	I	$\overline{Reset\ Data\ Available}$: A logic "0" will reset the DAV line. The DAV F/F is the only thing that is reset.
19	DAV	O	Data Available: This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state when $\overline{SWE}$ (pin 16) is "1". Fig. 8.
20	SI	I	Serial Input: This line accepts the serial bit input stream. A marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 7, 8.
21	XR	I	External Reset: Resets all registers. Sets S0, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.

PIN FUNCTIONS (CONT.)

Pin Number	Signal Name	Input/ Output	Function
22	TBMT	O	Transmitter Buffer Empty: The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 14, 16. Tristate when $\overline{SWE}$ (pin 16) is "1".
23	$\overline{DS}$	I	$\overline{Data\ Strobe}$: A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	EOC	O	End of Character: This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 13, 15.
25	SO	O	Serial Output: This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.
26..33	DB1..DB8	I	Data Bit Inputs: There are up to 8 data bit input lines available.
34	CS	I	Control Strobe: A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	NP	I	No Parity: A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	TSB	I	Number of Stop Bits: This lead will select the number of stop bits, 1 or 2 to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1 1/2 stop bits.
37-38	NB2, NB1	I	Number of Bits/Character: These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	EPS	I	Odd/Even Parity Select: The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even partiy.
40	TCP	I	Transmitter Clock: This input line requires a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc(with Respect to GND) ..... -0.3 to +16V
Storage Temperature..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) .....+330°C

Standard Conditions

(unless otherwise noted)
Vcc .....+4.75V to +5.25V
Operating Temperature (TA) .....0°C to +70°C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

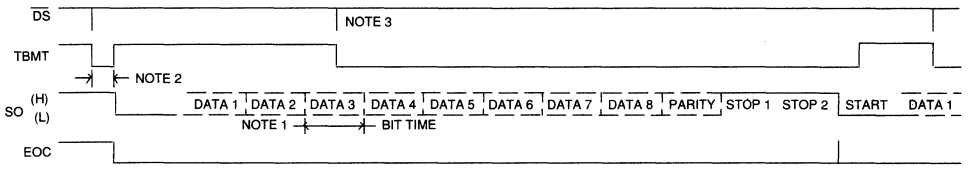
Characteristics	Min	Typ	Max	Units	Conditions
Input Logic Levels (AY31015D)					
Logic 0	0	-	0.8	Volts	
Logic 1	2.0	-	V_{CC}+0.3	Volts	Has internal pull-up resistors to V_{CC}
Input Capacitance					
All inputs	-	-	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Hi-Impedance Outputs	0.5	-	-	M ohms	V_{IN} = 5V
Data Output Levels					
Logic 0	-	-	0.8	Volts	I_{OL} = 1.6mA (sink)
Logic 1	2.4	-	-	Volts	I_{OL} = 40 µA (source) - at V_{CC} = +5V
Output Capacitance	-	10	15	pF	
Power Supply Current					
I_{CC} at V_{CC} = +5V	-	10	15	mA	

AC CHARACTERISTICS

Characteristics	Min	Typ	Max	Units	Conditions	Remarks
Clock Frequency	DC	-	400	kHz	at V_{CC} = +4.75V	All AC testing
Baud	0	-	25	kbaud	at V_{CC} = +4.75V	waveforms at:
Pulse Width						V_{IH} = 2.4V
Clock Pulse	1.0	-	-	µs	See Fig. 5	V_{IL} = 0.8V
Control Strobe	200	-	-	ns	See Fig. 11	V_{OH} = 2.0V
Data Strobe	200	-	-	ns	See Fig. 10	V_{OL} = 0.8V
External Reset	500	-	-	ns	See Fig. 9	
Status Word Enable	500	-	-	ns	See Fig. 17	
Reset Data Available	200	-	-	ns	See Fig. 18	
Received Data Enable	500	-	-	ns	See Fig. 17	
Set Up & Hold Time						
Input Data Bits	20	-	-	ns	See Fig. 10	
Input Control Bits	20	-	-	ns	See Fig. 11	
Output Propagation Delay						
TPD0	-	-	500	ns	See Figs. 17 and 20	
TPD1	-	-	500	ns	See Figs. 17 and 20	

TIMING DIAGRAMS

FIG. 1 UAR/T - TRANSMITTER TIMING



NOTES: SEE FIGURES 2, 3, 4 FOR DETAILS
TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM.
SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE SO 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

DETAIL:

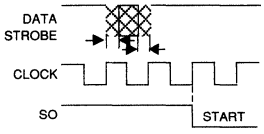


FIG. 2 TRANSMITTER AT START BIT NOT A TEST POINT

TRANSMITTER INACTIVE
TRANSMIT BUFFER LOADED WHEN EOC HIGH

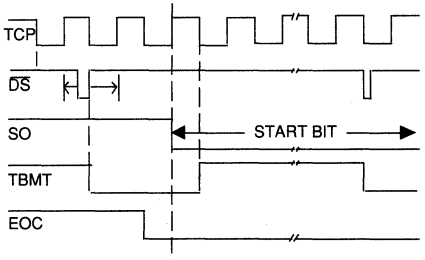


FIG. 3 TRANSMITTER AT START BIT

TRANSMITTER ACTIVE
TRANSMIT BUFFER LOADED WHEN EOC LOW

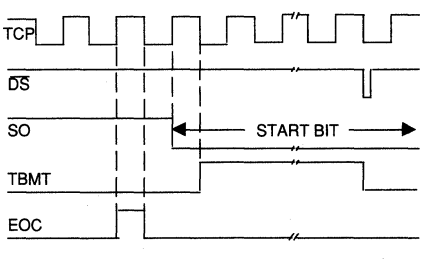
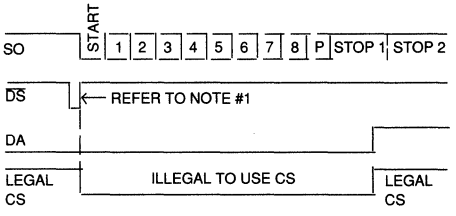


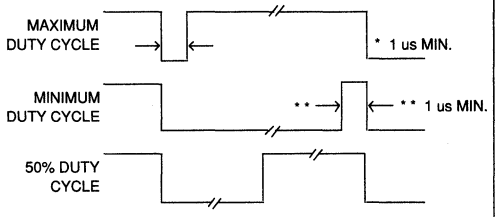
FIG. 4 ALLOWABLE POINTS TO USE



NOTE 1:
DS AND CS MAY OCCUR SIMULTANEOUSLY WHEN TRANSMITTER INACTIVE.

NOTE:
IF CONTROL STROBE IS HARDWIRED TO "1". THEN THE CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME.

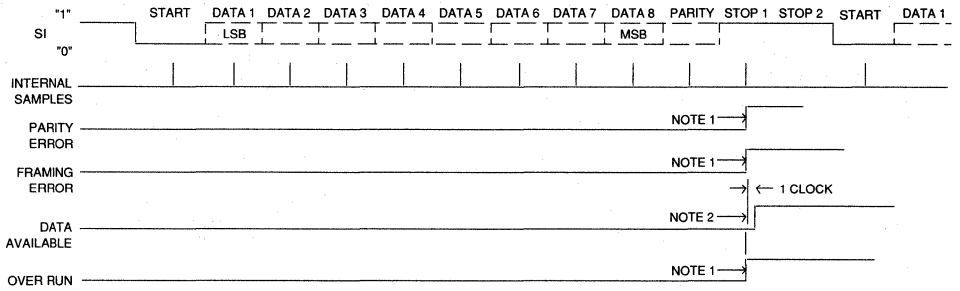
FIG. 5 ALLOWABLE TCP, RCP



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

TIMING DIAGRAMS (CONT.)

FIG. 6 UAR/T - RECEIVER TIMING



NOTES:
1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA AND PE, FE, OR HAVE BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTERS UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 BIT CODE WITH PARITY AND TWO STOP BITS. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE, THE DATA IN THE HOLDING REGISTER IS RIGHT JUSTIFIED, THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

FIG. 7 TRUE RECEIVER CENTER SAMPLING

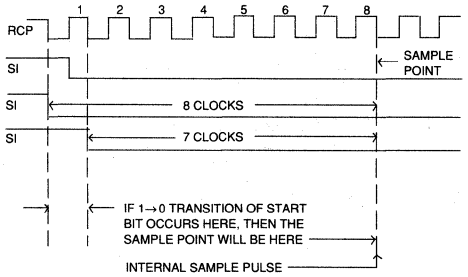


FIG. 8 RECEIVER DURING 1ST STOP BIT

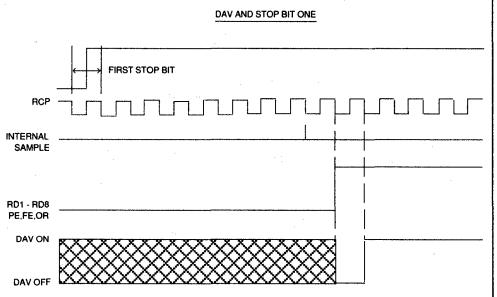
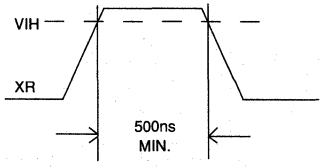


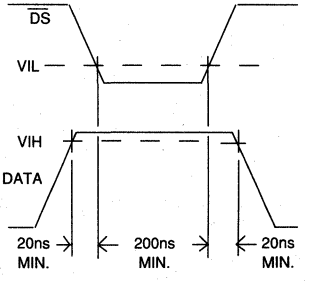
FIG. 9 XR PULSE



WHEN NOT IN USE, XR MUST BE HELD AT GND.

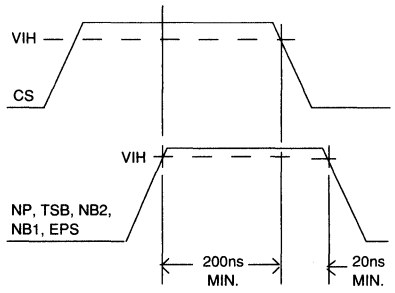
XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT EOC ARE RESET TO LOGIC "1" , ALL OTHER OUTPUTS RESET TO LOGIC "0".

FIG. 10 $\overline{DS}$



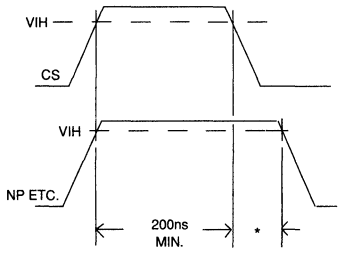
TIMING DIAGRAMS (CONT.)

FIG. 11A CS



CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

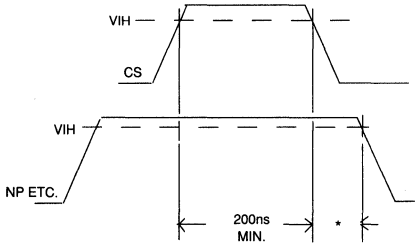
FIG. 11B



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM.

*20ns MIN.

FIG. 12



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

*20ns MIN.

FIG. 13 EOC TURN - ON

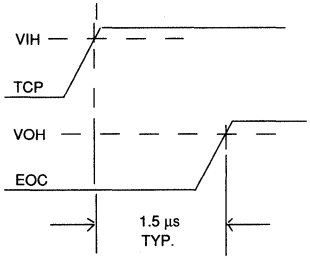


FIG. 14 TBMT TURN - OFF

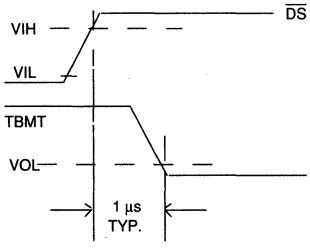
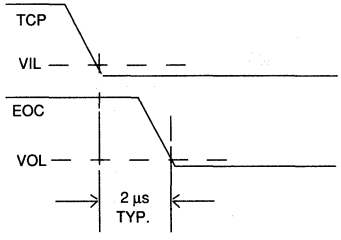


FIG. 15 EOC TURN - OFF



5

TIMING DIAGRAMS

FIG. 16 TBMT TURN - ON

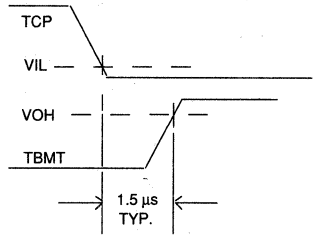


FIG. 17 $\overline{RDE}$, $\overline{SWE}$

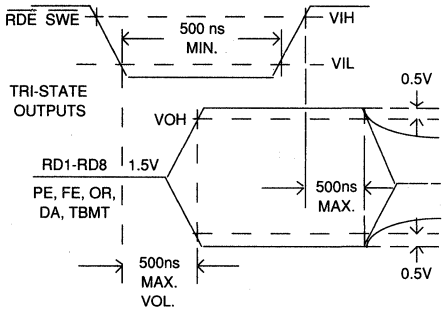


FIG. 18 RDAV

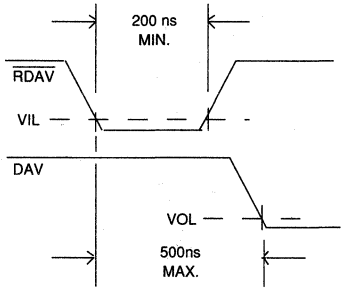


FIG. 19 SHORT CIRCUIT OUTPUT CURRENT

(only 1 output may be shorted at a time)

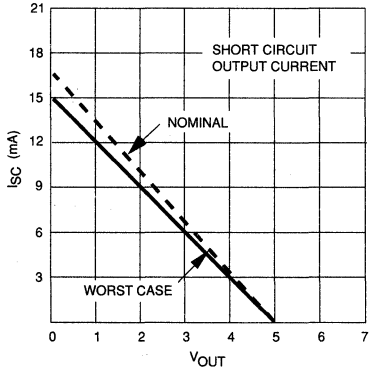


FIG. 20 RD1 - RD8, PE, FE, OR, TBMT, DAV

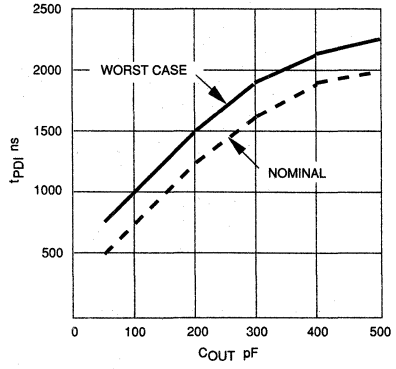


FIG. 21 +5 VOLT SUPPLY CURRENT

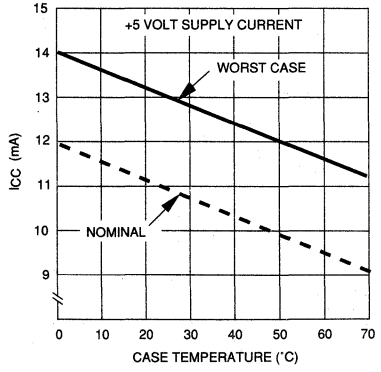
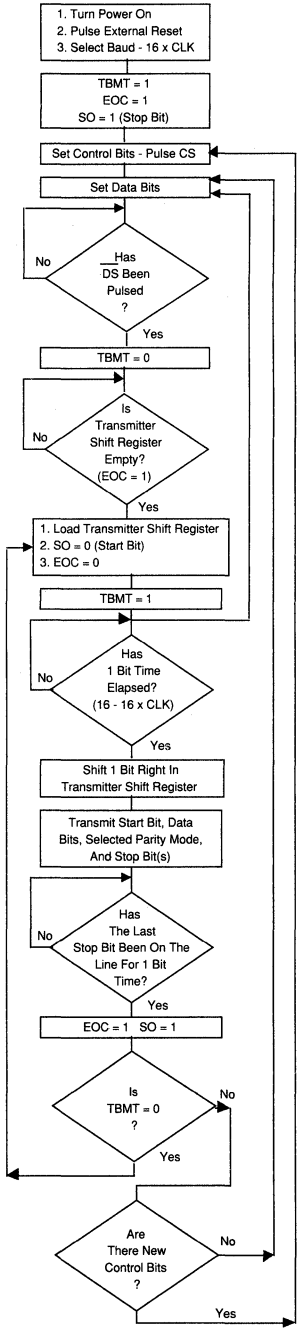


FIG. 22 TRANSMITTER OPERATION



TRANSMITTER

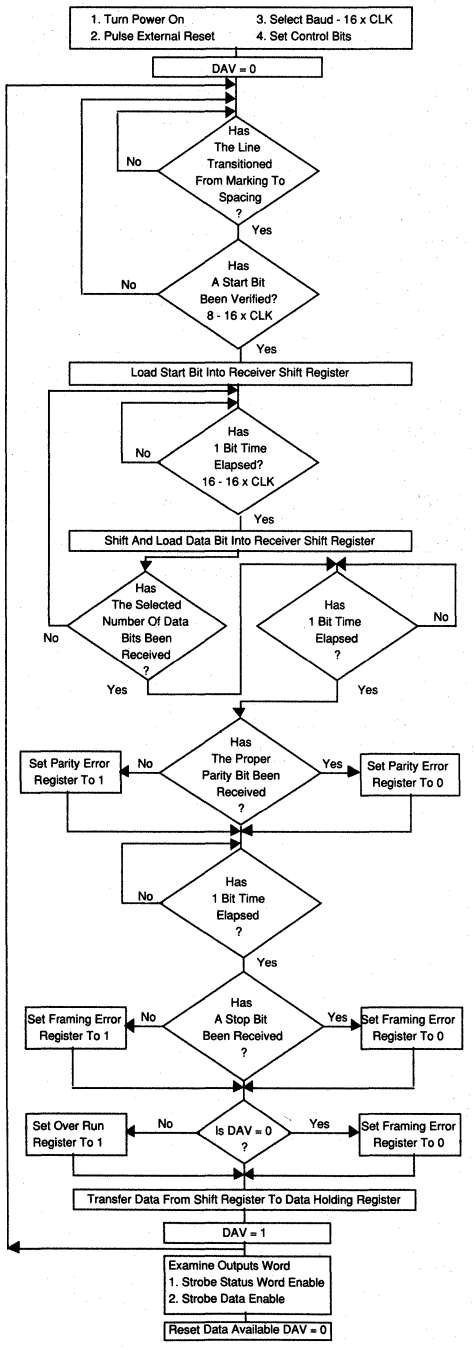
Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initialization is complete, user may set control bits and data bits. Control bits selection should occur before data bit selection, however, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0" and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss of transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

5

FIG. 23 RECEIVER OPERATION



RECEIVER

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "0".

After initialization is complete, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0"state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s) reception proceeds in an orderly manner.

While receiving parity and stop bit(s), the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected, the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been read out. If the DAV signal is at a logic "1", the receiver will assume data has not been read out and the over run flip-flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0", the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

FIG. 24 TRANSMITTER BLOCK DIAGRAM

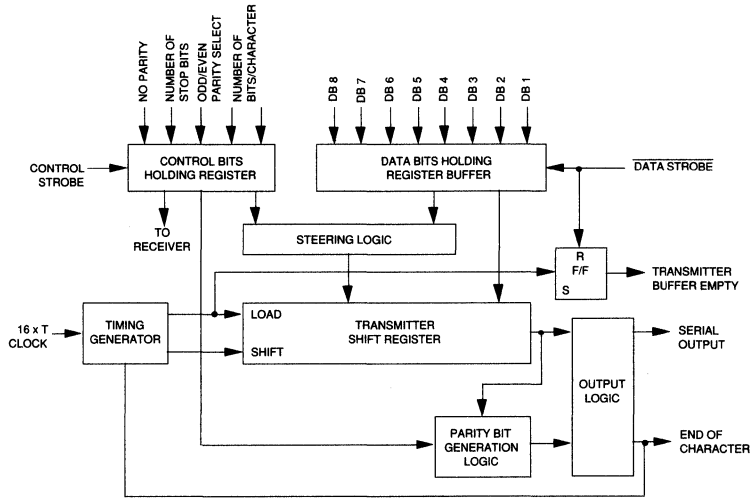
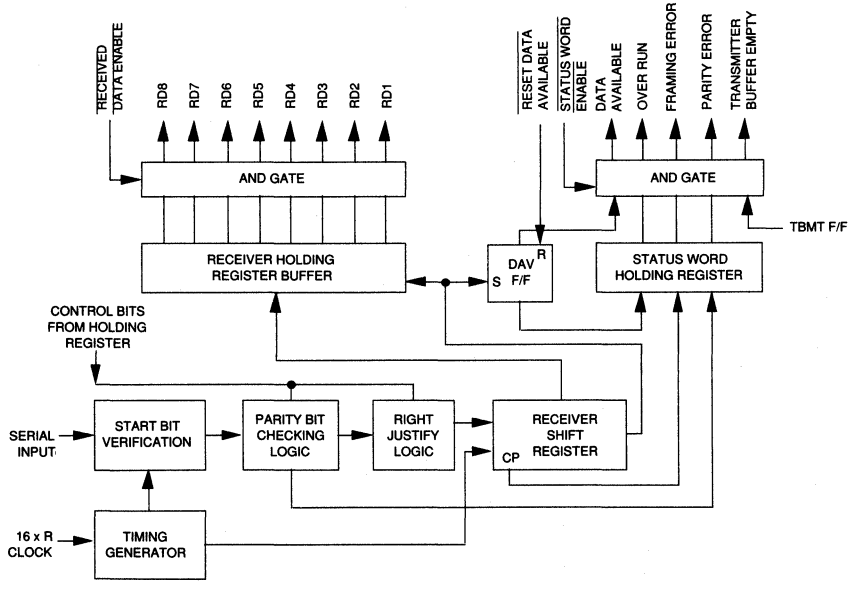


FIG. 25 RECEIVER BLOCK DIAGRAM

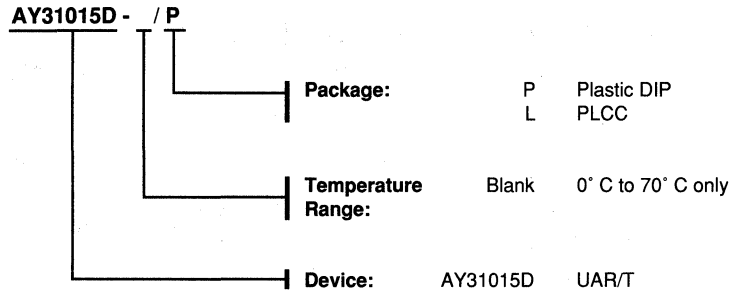


5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



AY58116/8116T
AY58136/8136T

Dual Baud Rate Generator

FEATURES

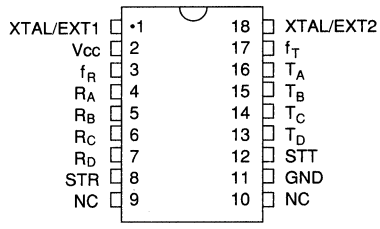
- Single +5V power supply
- On-chip crystal oscillator 8116/8136 or external frequency input 8116/8116T/8136/8136T
- Direct compatibility with UART/USRT
- Dual selectable 16x clock outputs
- High frequency reference output (Available only on 8136/8136T)
- Reprogrammable ROM allowing generation of non-standard frequencies
- TTL, MOS compatibility
- Pin for pin and functionally compatible with SMC's COM 8116/8116T/8136/8136T
- Microchip Technology Advanced N-Channel Silicon Gate Process

PIN CONFIGURATIONS

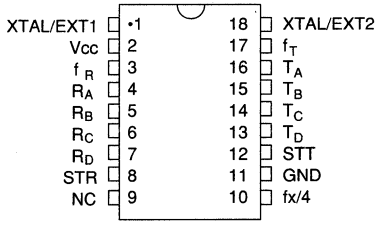
18 LEAD DUAL INLINE

AY58116/8116T

Top View



Top View



DESCRIPTION

The Microchip Technology AY58116/8136 Series is a very versatile family of Dual Baud Rate Generators. The AY58116/8116T and AY58136/8136T are pin for pin functionally equivalent to SMC's COM 8116/8116T and COM 8136/8136T, respectively.

The AY58116/8136 is designed to generate the full spectrum of 16 asynchronous /synchronous data communication frequencies for use with 16x and 32x UART/USRT devices.

An on-chip crystal oscillator available on the 8116 and 8136 is capable of providing a master reference frequency. Alternatively, complimentary TTL level clock signals can be input to pins 1 and 18. The 8116T and 8136T are only suitable for this external TTL reference. When using TTL outputs to drive the XTAL/EXT inputs, they should not be used to drive other TTL inputs due to excessive loading which may result in a reduction of noise immunity.

Dividers are used on the output of the oscillator/buffer which generate the output frequencies f_t and f_R. These dividers can divide any integer from 6 to $2^{19} + 1$, inclusive. When using an even divisor, the output will be square; an odd divisor will cause the output to be high longer than it is low by one clock period ($1/f_x$). The clock frequency (f_x) is used by the 8136/8136T to provide a high frequency output ($f_x/4$).

The 8116/8136 family allows generation of other frequencies with the use of its two divisor ROMs which contain 16 divisors, each 19 bits wide, allowing for up to 32 different divisors on custom parts.

Externally strobed data latches are used to hold the divisor select bits, R_A- R_D and T_A-T_D. The strobe inputs, STR or STT, allow data to pass directly through the data latch when in the high state. A new frequency is initiated within 3.5 µsec of a change in any of the four divisor select bits read by the device. Pull-up resistors are provided on the divisor select inputs which are not present on the strobe inputs.

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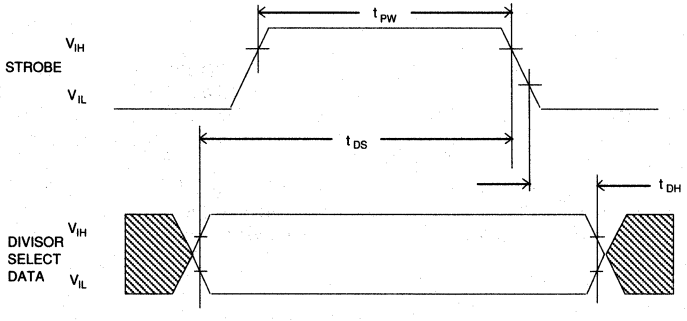
PIN FUNCTIONS

Pin Number	Signal	Function
1	XTAL/EXT1	Input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Positive power supply - normally +5V.
3	f_R	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A,R_B,R_C,R_D	These inputs, as shown in Table 1, select the receiver output frequency, f_R.
8	STR	A high level input strobe loads the receiver data (R_A,R_B,R_C,R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	
10	NC or $f_x/4$	NC (8116/8116T), $f_x/4$ (8136/8136T).
11	GND	Ground.
12	STT	A high level inut strobe loads the transmitter data (T_A,T_B,T_C,T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D,T_C,T_B,T_A	These inputs, as shown in Table 1, select the transmitter output frequency, f_T.
17	f_T	This output runs at a frequency selected by the transmitter divisor select data bits.
18	XTAL/EXT2	This input is either the other pin of the crystal package or the other polarity of the external input.

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Positive Voltage on any Pin,
with respect to ground ..... +8.0V
Negative Voltage on any Pin,
with respect to ground ..... -0.3V

Standard Conditions (unless otherwise noted):
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Voltage Levels						
Low Level	V_{IL}	-	-	0.8	V	
High Level	V_{IH}	2.0	-	-	V	excluding XTAL inputs
Output Voltage Levels						
Low Level	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA, for $f_X/4$,
		-	-	0.4	V	I_{OL} = 3.2mA, for f_R, f_T
High Level	V_{OH}	3.5	-	-	V	I_{OH} = -100µA
Input Current						
Low Level	I_{IL}	-	-	-0.1	mA	V_{IN} = GND, R_A-R_D & T_A-T_D only
Input Capacitance All inputs		-	5	10	pF	V_{IN} = GND, excluding XTAL inputs
Power Supply Current	I_{CC}	-	-	50	mA	

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Clock Frequency	f_X	0.01	-	5.1	MHz	XTAL/EXT, 50% Duty Cycle ±5%
Strobe Pulse Width	t_{PW}	150	-	DC	ns	
Input Set-up Time	t_{DS}	200	-	-	ns	
Input Hold Time	t_{DH}	50	-	-	ns	
Strobe to new Frequency Delay		-	-	3.5	µs	@f_X = 5.0 MHz

CRYSTAL SPECIFICATIONS

Temperature range 0°C to +70°C
Series resistance ≤50Ω
Series resonant
Overall tolerance ± 0.01%

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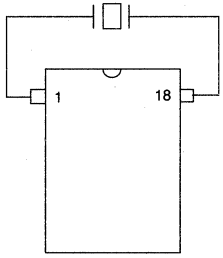
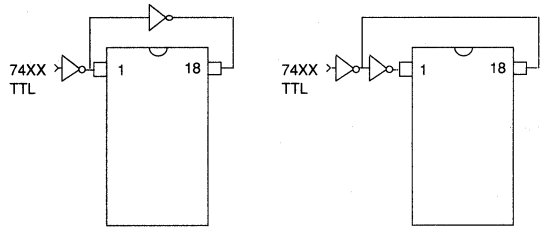
CRYSTAL OPERATION AY58116/8136



EXTERNAL INPUT OPERATION AY58116/8116T/8136/8136T



74XX - TOTEM POLE OR OPEN COLLECTOR OUTPUT (EXTERNAL PULL-UP RESISTOR REQUIRED)

BLOCK DIAGRAM: AY58116/8116T/8136/8136T

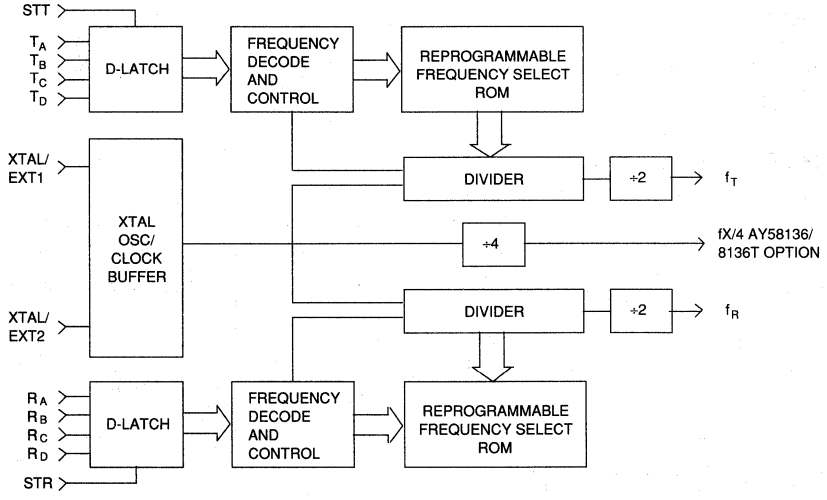


Table 1 Output Frequency AY58116/8116T/8136/8136T

REFERENCE FREQUENCY = 5.068800 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
0011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
0100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
1001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
1010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
1011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
1100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
1110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

Table 1 (Cont.) Output Frequency AY58116/8116T/8136/8136T-005

REFERENCE FREQUENCY = 4.915200 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6144	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4096	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2793	109.93	1.758983	0.0100%
0011	134.50	16X	2.15200	2284	134.50	2.152000	0.0000%
0100	150.00	16X	2.40000	2048	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1024	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	512	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	256	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	171	1796.49	28.743859	0.1949%
1001	2000.00	16X	32.00000	154	1994.81	31.916883	0.2597%
1010	2400.00	16X	38.40000	128	2400.00	32.000000	0.0000%
1011	3600.00	16X	57.60000	85	3614.11	57.825882	0.3921%
1100	4800.00	16X	76.80000	64	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	43	7144.19	114.306976	0.7751%
1110	9600.00	16X	153.60000	32	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19200.00	307.200000	0.0000%

Table 1 (Cont.) Output Frequency AY58116/8116T/8136/8136T-006

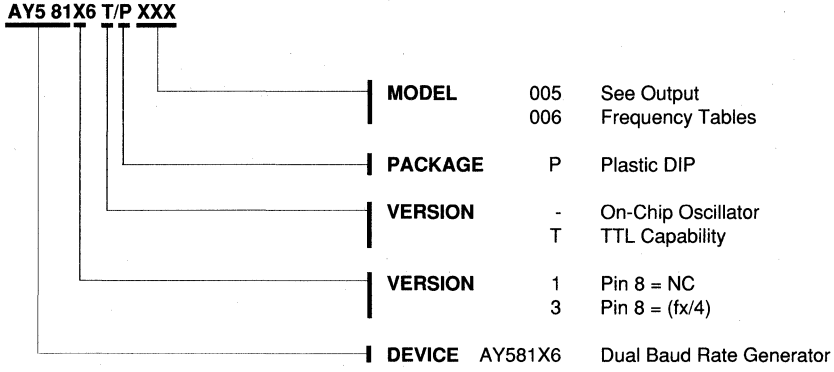
REFERENCE FREQUENCY = 5.068800 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	32X	1.60000	3168	50.00	1.60000	0.0000%
0001	75.00	32X	2.40000	2112	75.00	2.40000	0.0000%
0010	110.00	32X	3.52000	1440	110.00	3.52000	0.0000%
0011	134.50	32X	4.30400	1177	134.52	4.30600	0.0600%
0100	150.00	32X	4.80000	1056	150.00	4.80000	0.0000%
0101	200.00	32X	6.40000	792	200.00	6.40000	0.0000%
0110	300.00	32X	9.60000	528	300.00	9.60000	0.0000%
0111	600.00	32X	19.20000	264	600.00	19.20000	0.0000%
1000	1200.00	32X	38.40000	132	1200.00	38.40000	0.0000%
1001	1800.00	32X	57.60000	88	1800.00	57.60000	0.0000%
1010	2400.00	32X	76.80000	66	2400.00	76.80000	0.0000%
1011	3600.00	32X	115.20000	44	3600.00	115.20000	0.0000%
1100	4800.00	32X	153.60000	33	4800.00	153.60000	0.0000%
1101	7200.00	32X	230.40000	22	7200.00	230.40000	0.0000%
1110	9600.00	32X	307.20000	16	9900.00	316.80000	3.1250%
1111	19200.00	32X	614.40000	8	19800.00	633.60000	3.1250%

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



AY58126/8126T
AY58146/8146T

SINGLE BAUD RATE GENERATOR

FEATURES

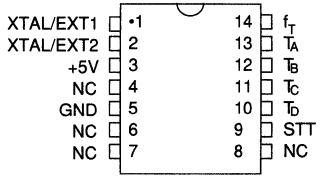
- Single +5V power supply
- On-chip crystal oscillator 8126/8146 or external frequency input 8126/8126T/8146/8146T
- Direct compatibility with UART/USRT
- Choice of 16x clock outputs
- High frequency reference output (Available only on 8146/8146T)
- Reprogrammable ROM allowing generation of non-standard frequencies
- TTL, MOS compatibility
- Pin for pin and functionally compatible with SMC's COM 8126/8126T/8146/8146T
- Microchip Technology Advanced N-Channel Silicon Gate Process

PIN CONFIGURATIONS

14 LEAD DUAL INLINE

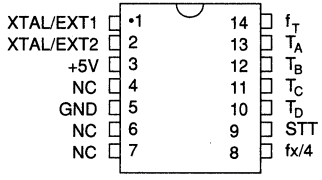
AY58126/8126T

Top View



AY58146/8146T

Top View



DESCRIPTION

The Microchip Technology AY58126/8146 Series is a very versatile family of Single Baud Rate Generators. The AY58126/8126T and AY58146/8146T are pin for pin functionally equivalent to SMC's COM 8126/8126T and COM 8146/8146T, respectively.

The AY58126/8146 is designed to generate the full spectrum of 16 asynchronous /synchronous data communication frequencies for use with 16x and 32x UART/USRT devices.

An on-chip crystal oscillator available on the 8126 and 8146 is capable of providing a master reference frequency. Alternatively, complimentary TTL level clock signals can be input to pins 1 and 2. The 8126T and 8146T are only suitable for this external TTL reference. When using TTL outputs to drive the XTAL/EXT inputs, they should not be used to drive other TTL inputs due to excessive loading which may result in a reduction of noise immunity.

Dividers are used on the output of the oscillator/buffer which generate the output frequency f_T. This divider can divide any integer from 6 to $2^{19} + 1$, inclusive. When using an even divisor, the output will be square; an odd divisor will cause the output to be high longer than it is low by one clock period ($1/f_x$). The clock frequency (f_x) is used by the 8146/8146T to provide a high frequency output ($f_x/4$).

The 8126/8146 family allows generation of other frequencies with the use of its two divisor ROMs which contain 16 divisors, each 19 bits wide, allowing for up to 32 different divisors on custom parts.

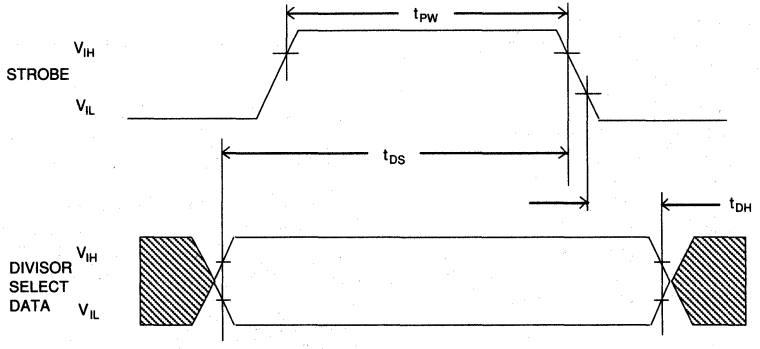
Externally strobed data latches are used to hold the divisor select bit T_A-T_D. The strobe input STT allows data to pass directly through the data latch when in the high state. A new frequency is initiated within 3.5 usec of a change in any of the four divisor select bits read by the device. Pull-up resistors are provided on the divisor select inputs which are not present on the strobe inputs.

5

PIN FUNCTIONS

Pin Number	Signal	Function
1	XTAL/EXT1	Input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Positive power supply - normally +5V.
4	NC	
5	GND	Ground.
6-7	NC	
8	NC or $f_X/4$	NC (8126/8126T), $f_X/4$ (8146/8146T).
9	STT	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
10-13	T_D,T_C,T_B,T_A	These inputs, as shown in the Tables p.5 ff, select the transmitter output frequency, f_T.
14	f_T	This output runs at a frequency selected by the transmitter divisor select data bits.

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Positive Voltage on any Pin,
with respect to ground ..... +8.0V
Negative Voltage on any Pin,
with respect to ground ..... -0.3V

Standard Conditions

(unless otherwise noted):
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Voltage Levels						
Low Level	V_{IL}	-	-	0.8	V	
High Level	V_{IH}	2.0	-	-	V	excluding XTAL inputs
Output Voltage Levels						
Low Level	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA, for $f_X/4$,
		-	-	0.4	V	I_{OL} = 3.2mA, for f_R, f_T
High Level	V_{OH}	3.5	-	-	V	I_{OH} = -100µA
Input Current						
Low Level	I_{IL}	-	-	-0.1	mA	V_{IN} = GND, T_A-T_D only
Input Capacitance All inputs		-	5	10	pF	V_{IN} = GND, excluding XTAL inputs
Power Supply Current	I_{CC}	-	-	50	mA	

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Clock Frequency	f_X	0.01	-	5.1	MHz	XTAL/EXT, 50% Duty Cycle ±5%
Strobe Pulse Width	t_{PW}	150	-	DC	ns	
Input Set-up Time	t_{DS}	200	-	-	ns	
Input Hold Time	t_{DH}	50	-	-	ns	
Strobe to new Frequency Delay		-	-	3.5	µs	@f_X = 5.0 MHz

CRYSTAL SPECIFICATIONS

Temperature range 0°C to +70°C
Series resistance ≤ 50Ω
Series resonant
Overall tolerance ± 0.01%

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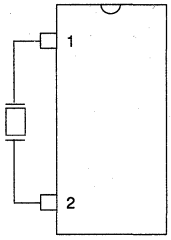
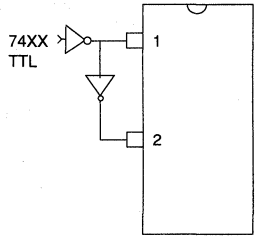
CRYSTAL OPERATION

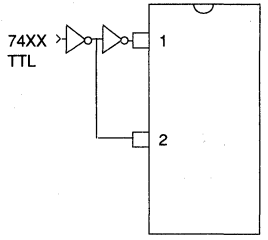
AY58126/8146



EXTERNAL INPUT OPERATION

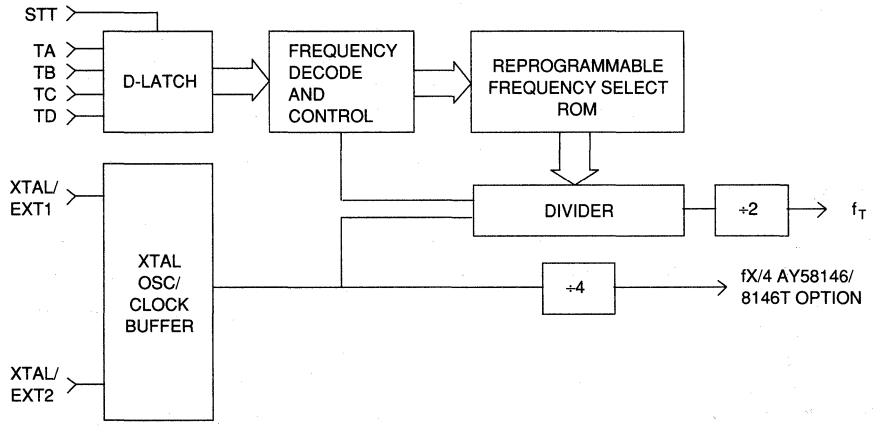
AY58126/8126T/8146/8146T





74XX - TOTEM POLE OR OPEN COLLECTOR OUTPUT (EXTERNAL PULL-UP RESISTOR REQUIRED)

BLOCK DIAGRAM: AY58126/8126T/8146/8146T



OUTPUT FREQUENCY

AY58126/8126T/8146/8146

Reference Frequency = 5.068800 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
0011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
0100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
1001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
1010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
1011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
1100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
1110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

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OUTPUT FREQUENCY

AY58126/8126T/8146/8146T-005 Reference Frequency = 4.915200 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6144	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4096	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2793	109.93	1.758983	0.0636%
0011	134.50	16X	2.15200	2284	134.50	2.152000	0.0000%
0100	150.00	16X	2.40000	2048	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1024	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	512	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	256	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	171	1796.49	28.743859	0.1949%
1001	2000.00	16X	32.00000	154	1994.81	31.916883	0.2597%
1010	2400.00	16X	38.40000	128	2400.00	38.400000	0.0000%
1011	3600.00	16X	57.60000	85	3614.11	57.825882	0.3921%
1100	4800.00	16X	76.80000	64	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	43	7144.19	114.306976	0.7751%
1110	9600.00	16X	153.60000	32	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19200.00	307.200000	0.0000%

OUTPUT FREQUENCY

AY58126/8126T/8146/8146T-006 Reference Frequency = 5.068800 MHz

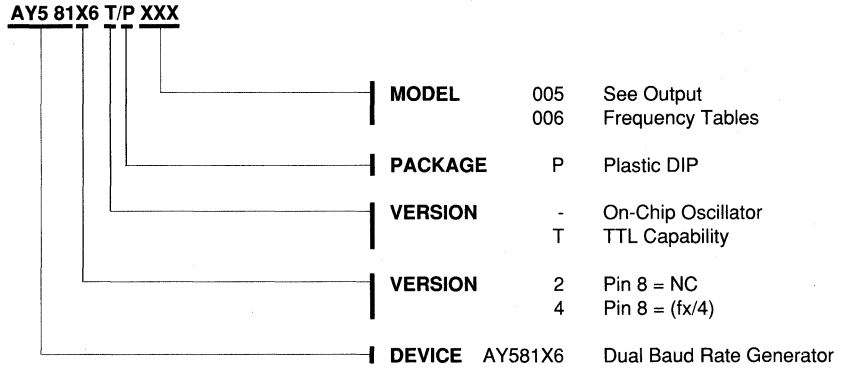
Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	32X	1.60000	3168	50.00	1.60000	0.0000%
0001	75.00	32X	2.40000	2112	75.00	2.40000	0.0000%
0010	110.00	32X	3.52000	1440	110.00	3.52000	0.0000%
0011	134.50	32X	4.30400	1177	134.52	4.30600	0.0600%
0100	150.00	32X	4.80000	1056	150.00	4.80000	0.0000%
0101	200.00	32X	6.40000	792	200.00	6.40000	0.0000%
0110	300.00	32X	9.60000	528	300.00	9.60000	0.0000%
0111	600.00	32X	19.20000	264	600.00	19.20000	0.0000%
1000	1200.00	32X	38.40000	132	1200.00	38.40000	0.0000%
1001	1800.00	32X	57.60000	88	1800.00	57.60000	0.0000%
1010	2400.00	32X	76.80000	66	2400.00	76.80000	0.0000%
1011	3600.00	32X	115.20000	44	3600.00	115.20000	0.0000%
1100	4800.00	32X	153.60000	33	4800.00	153.60000	0.0000%
1101	7200.00	32X	230.40000	22	7200.00	230.40000	0.0000%
1110	9600.00	32X	307.20000	16	9900.00	316.80000	3.1250%

5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



AY38910A
AY38912A

PROGRAMMABLE SOUND GENERATOR

FEATURES

- Industry standard programmable sound generator
- Register oriented architecture for ease of use
- Full software control of sound generation
- Easily interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmable analog outputs
- One or two 8-bit I/O ports
- Single 5 volt supply
- 0° to 70° C operation
- 40 pin or 28 pin package option

APPLICATIONS

- Arcade games
- Warning alarms
- Special effects
- Personal computers
- Music synthesis

DESCRIPTION

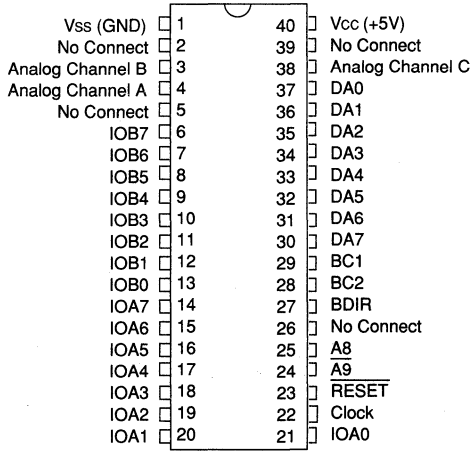
The AY38910A/38912A Programmable Sound Generator (PSG) is an LSI circuit which can produce a wide variety of complex sounds under software control. The AY38910A/38912A is manufactured in Microchip Technologys N-Channel Ion Implant Process. Operation requires a single +5V power supply, a compatible clock, and a microprocessor controller, such as the PIC series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signaling, and personal computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one component is satisfied by the three independently controllable analog sound output channels can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

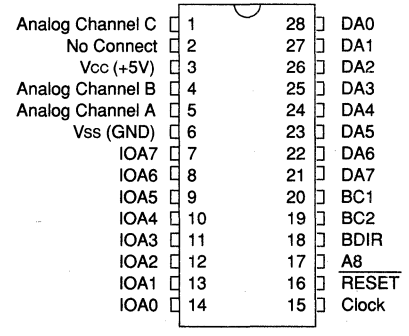
5

PIN CONFIGURATION
Top View

40 LEAD DUAL INLINE - AY38910A



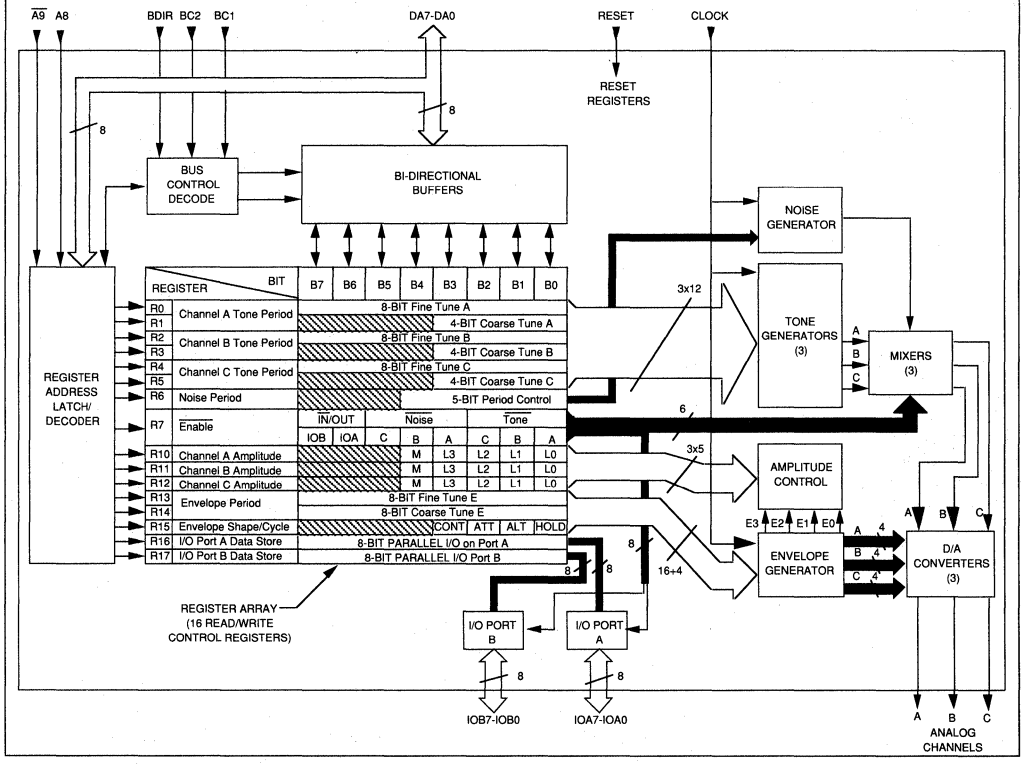
28 LEAD DUAL INLINE - AY38912A



DESCRIPTION (CTD.)

All circuit control signals are digital in nature and may be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction.

AY389XXA BLOCK DIAGRAM



PIN FUNCTIONS

DA7-DA0 (Input /Output/High Impedence)

Data/Address Bits 7-0: Pins 30-37 (AY38910A)
Pins 21-28 (AY38912A)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the address mode, DA3-DA0 select the internal register address ($0\text{-}17_8$) and DA7-DA4 in conjunction with address inputs $\overline{A9}$ and A8, form the chip select function. When the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedence state.

$\overline{\text{Address 9}}$, Address 8

A8 (input): Pin 25 (AY38910A)
Pin 17 (AY38912A)

$\overline{A9}$ (input): Pin 24 (AY38910A)
Not available (AY38912A)

High order address bits $\overline{A9}$ and A8 are fixed to recognize a "01"code. They may be left unconnected as each is provided with either an on chip pull-down ($\overline{A9}$) or pull-up (A8) resistor. In noisy environments, however, it is recommended that $\overline{A9}$ and A8 be tied to external ground and +5V respectively if they are not to be used.

RESET (Input)

Pin 23 (AY38910A)
Pin 16 (AY38912A)

For initialization/power-on purposes, applying a low level input to the RESET pin will reset all registers to 0s. The RESET pin is provided with an on-chip pull-up resistor.

CLOCK (Input)

Pin 22 (AY38910A)
Pin 15 (AY38912A)

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

BDIR, BC2, BC1 (Inputs)

Pins 27,28,29 (AY38910A)
Pins 18,19,20 (AY38912A)

The Bus DIRection, Bus Control 2 and Bus Control 1 are used to control the PSG.

For example, if these bus control signals are generated directly by a microprocessor to control all bus operations internal and external to the PSG, then the following Bus Control Function Table applies.

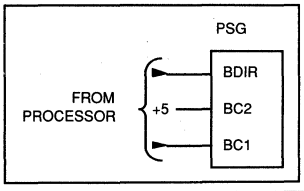
Interfacing to a processor simply requires simulating the decoding shown in the Function Table. The redundancies in the PSG functions vs. bus control signals can be used as an advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could reduce the programming of the bus control signals to the following Simplified Bus Control Function Table which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V).

BUS CONTROL FUNCTION TABLE

Inputs BDIR	BC2	BC1	Microprocessor Function	PSG Function
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7-DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7-DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7-DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7-DA0 are in the input mode.

SIMPLIFIED BUS CONTROL FUNCTION TABLE

Inputs BDIR	BC2	BC1	PSG Function
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



Analog Channel A, B, C (Outputs)

Pins 4,3,38 (AY38910A)
Pins 5,4,1 (AY38912A)

Each of these signals is the output of its corresponding digital to analog converter and provides 1V peak-peak (max) signal representing the complex sound waveshape generated by the PSG.

No Connect

Pins 2,5,26,39 (AY38910A)
Pins 2 (AY38912A)

These pins are for Microchip Technology test purposes only and should be left open. Do not use as tie-points.

Vcc

Pins 40 (AY38910A)
Pin 3 (AY38912A)

Nominal +5 Volt power supply to the PSG.

Vss

Pin 1 (AY38910A)
Pin 6 (AY38912A)

Ground reference for the PSG.

ARCHITECTURE

The AY38910A/AY38912A is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values. All functions of the PSG are controlled through the 16 registers which, once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

Register Array

The principle element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits) are decoded as follows:

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THROUGH									
0	1	0	0	0	0	1	1	1	1

HIGH ORDER (Chip Select) — LOW ORDER (Register No.)

The four low order address bits select one of the 16 registers ($R0_8$-$R17_8$). The six high order address bits function as chip selects to control the tri-state bidirectional buffers (when the high order address bits are incorrect, the bidirectional buffers are forced to a high impedance state). High order address bits A9, A8 are fixed in the PSG design to recognize a "01" code; high order address bits DA7-DA4 are programmed to recognize only a "0000" code. All addresses are latched internally. This internally latched address is updated and modified on every latch address signal presented to the PSG via the BDIR, BC2 and BC1 inputs. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (Inactive, Latch Address, Write Data) is accomplished by the Bus Control Decode block.

Sound Generating Blocks

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	Produce the basic square wave tone frequencies for each channel (A, B, C).
Noise Generator	Produces a pulse width modulated pseudo-random square wave output.
Mixers	Combine the outputs of the Tone Generators and the Noise Generator; per channel (A,B,C).
Envelope Generator	Produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
Amplitude Control	Provides the D/A Converters with either a fixed or variable amplitude pattern. Fixed amplitude is under direct CPU control. Variable amplitude is accomplished via the output of the Envelope Generator.
D/A Converters	The three D/A Converters each produce a 16 level (max) output signal as determined by the Amplitude Control.

OPERATION

Since all PSG functions are processor controlled by writing to the internal registers (see table). A detailed description of the PSG operation may best be accomplished by relating each PSG function to control of the corresponding register. The function of creating or programming a specific sound effect logically follows the control sequence shown in the figure below.

Tone Generator Control (R0 - R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained by first dividing the input clock by 16 then by further dividing the result by the programmed 12 bit Tone Period value. Each 12-bit tone period value is obtained by combining the contents of the respective Coarse and Fine Tune registers, as illustrated.

INTERNAL REGISTERS

Operation	Register	Function
Tone Generator Control	R0-R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and/or noise on selected channels
Amplitude Control	$R10_8$-$R12_8$	Select fixed or variable (envelope) amplitudes
Envelope Generator Control	$R13_8$-$R15_8$	Program envelope period, select envelope pattern

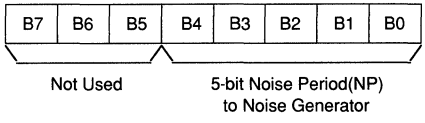
TUNE REGISTERS

Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2

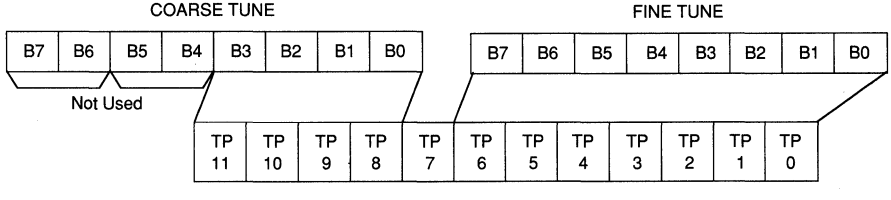
Noise Generator Control (R6)

The frequency of the noise source is obtained by dividing the input clock by 16, then by further dividing the result by the programmed 5 bit Noise Period value. This 5 bit value consists of the lower 5 bits (B4-B0) of register R6, as illustrated:

NOISE PERIOD REGISTER (R6)



CONTROL SEQUENCE



12-bit Tone Period (TP) to Tone Generator

Notes:
1. The period of the output of the tone generator is therefore determined by: 16 x TP x P where P = the period of the input clock.
2. If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, ie., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

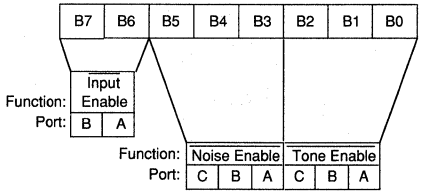
Mixer Control - I/O Enable (R7)

Register R7 is a multi-function ENABLE register which controls the three Noise/Tone Mixers.

The mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5-B0 of register R7, as illustrated.

The direction (input or output) of the general purpose I/O ports (I/OA and I/OB) is determined by the state of bits B7 and B6 of R7, as illustrated.

MIXER CONTROL REGISTER (R7)



NOISE ENABLE TRUTH TABLE

R7 Bits B5 B4 B2	Noise Enabled on Channel
0 0 0	C B A
0 0 1	C B -
0 1 0	C - A
0 1 1	C - -
1 0 0	- B A
1 0 1	- B -
1 1 0	- - A
1 1 1	- - -

TONE ENABLE TRUTH TABLE

R7 Bits B2 B1 B0	Tone Enabled on Channel
0 0 0	C B A
0 0 1	C B -
0 1 0	C - A
0 1 1	C - -
1 0 0	- B A
1 0 1	- B -
1 1 0	- - A
1 1 1	- - -

I/O PORT TRUTH TABLE

R7 bits B7 B6	I/O Port Status I/OB	I/OA
0 0	Input	Input
0 1	Input	Output
1 0	Output	Input
1 1	Output	Output

NOTE: Disabling noise and tone does not turn off a channel. Turning a channel off can only be accomplished by writing all zeros into the corresponding Amplitude Control Register.

Amplitude Control ($R10_8$,$R11_8$,$R12_8$)

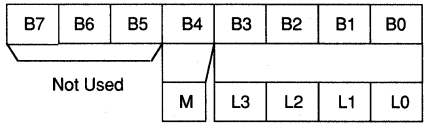
The amplitude of the signals generated by each of the three D/A Converters (one each for Channels A,B, and C) is determined by the content of the lower bits (B4-B0) of registers $R10_8$, $R11_8$, and $R12_8$ as illustrated.

These five bits consist of a 1-bit mode select ("M" bit) and a 4-bit "fixed" amplitude level (L3-L0). When the M bit is low, the output level of the analog channel is defined by the 4-bit "fixed" amplitude level of the Amplitude Control Register. This amplitude level is fixed in the sense that the amplitude

CHANNEL CONTROL

Register	Channel
$R10_8$	A
$R11_8$	B
$R12_8$	C

AMPLITUDE CONTROL BITS



AMPLITUDE CONTROL REGISTER

Amplitude Mode	4 bit fixed Amplitude Level	Note
0	0 0 0 0	Amplitude Defined By L0-L3
'	' ' '	
'	' ' '	
'	' ' '	
0	1 1 1 1	
1	X X X X	Amplitude Defined By E0-E3

is under direct control of the system processor. When the M bit is high, the output level of the analog channel is defined by the 4-bits of the Envelope Generator (bits E3-E0). The amplitude mode bit can also be thought of as an "envelope enable" bit.

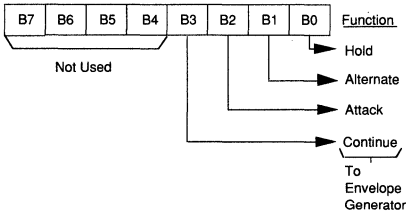
Envelope Generator Control

To accomplish the generation of complex envelope patterns, two independent methods of control are provided: first, it is possible to vary the frequency of the envelope using registers $R13_8$ and $R14_8$; second, the relative shape and cycle pattern of the envelope can be varied using register $R15_8$. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control. (See Figure 1 and 2).

Envelope Period Cotrol ($R13_8$,$R14_8$)

The frequency of the envelope is obtained by first dividing the input clock by 256, then by further dividing the result by the programmed 16 bit Envelope Period value. This 16 bit value is obtained by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated:

ENVELOPE SHAPE/CYCLE CONTROL REGISTER (R15)



Envelope Shape/Cycle Control ($R15_8$)

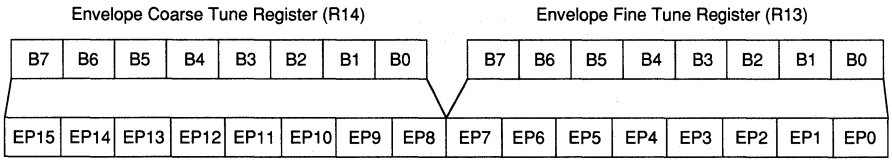
The Envelope Generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern of the 4-bit counter. (See Figure 4 and 5).

This envelope shape/cycle control is contained in the lower 4 bits (B3-B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated:

ENVELOPE SHAPE/CYCLE CONTROL

Bit	Signal	Function
0	HOLD	When this is set high (logic 1) the envelope is limited to one cycle, the value of the envelope at the end of the cycle being held.
1	ALTERNATE	When set high (logic 1) the envelope counter reverses direction at end of each cycle (i.e. performs as an up/down counter).
2	ATTACK	When set high (logic 1) the envelope counter will count up (attack). When set low (logic 0) the counter will count down (decay).
3	CONTINUE	When set high (logic 1) the cycle pattern will be defined by the HOLD bit . When set low (logic 0) the envelope counter will reset to 0000 after one cycle and hold that value.

16-BIT ENVELOPE PERIOD (EP) TO ENVELOPE GENERATOR



Refer to Programmable Sound Generator Data Manual for calculation example.

NOTE: If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

D/A Converter

Since the primary use of the PSG is to produce sound for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4 bit outputs of the Amplitude Control block while the Mixer outputs provide the base signal frequency (Noise and/or Tone). (See Fig. 3).

FIG. 1 ENVELOPE SHAPE /CYCLE OPERATION

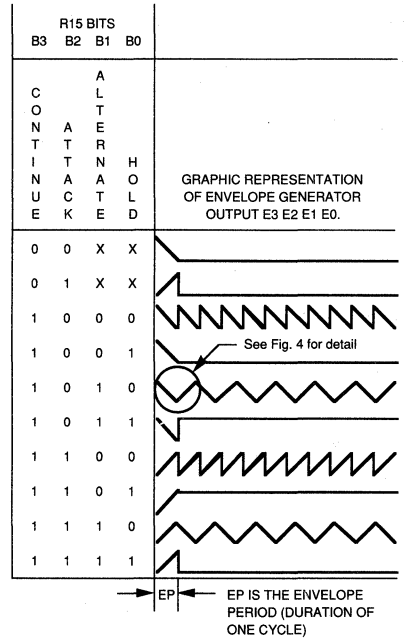


FIG. 2 DETAIL OF TWO CYCLES (REF. WAVEFORM "1010" IN FIG. 1)

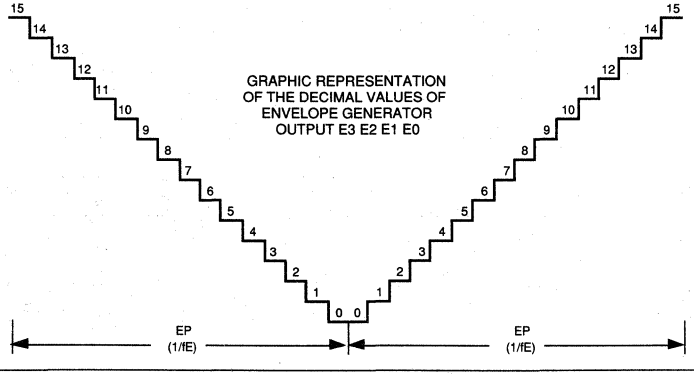


FIG. 3 D/A CONVERTER OUTPUT

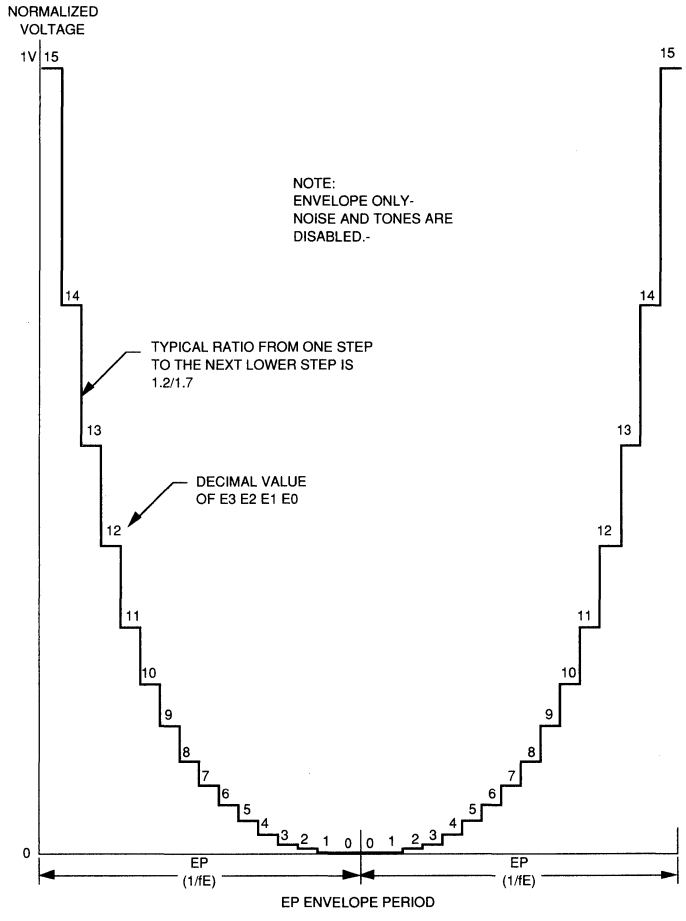


FIG. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

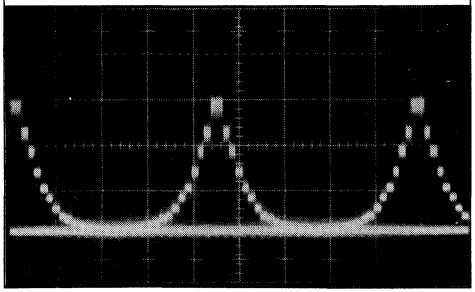
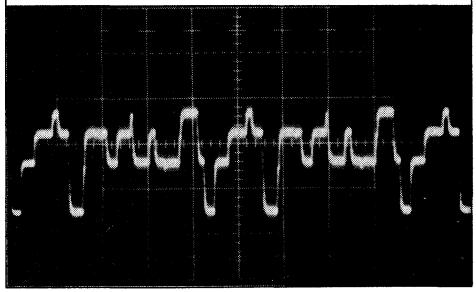


FIG. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature.....-55°C to +150°C
Operating Temperature.....0°C to +70°C
Vcc and all other Input/Output
Voltages with Respect to Vss.....-0.3V to +8.0V

Standard Conditions

Vcc = +5V ± 5%
Vss = GND
Operating Temperature = 0°C to +70°C
(Unless otherwise noted)

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS	Sym	Min	Typ**	Max	Units	Conditions
All Inputs						
Low Level	V_{IL}	-0.2	-	0.8	V	
High Level	V_{IH}	2.2	-	Vcc	V	
Data Bus (DA7-DA0) Output Levels						
Low Level	V_{OL}	0	-	0.4	V	I_{OL} = 1.6mA, 150pF
High Level	V_{OH}	2.4	-	Vcc	V	I_{OH} = 100 A, 150pF
Data Bus(DA7-DA0)						
Input Leakage	I_{IAL}	-10	-	10	A	V_{IN} = 0.4V to Vcc
Analog Channel Outputs						
Output Volume	V_o	0	-	60	dB	Test Circuits: Fig. 6
Power Supply Current	Icc	-	70	90	mA	
Max. Current (per channel)	-	0.4	2.0	-	mA	V_{OUT} = 0.7V, Amplitude Control Set to F
I/O Ports						
Pull Up Current Low	I_{IL}	20	-	200	A	V_{IN} = 0.4V, Outputs disabled
Pull Up Current High	I_{IH}	10	-	100	A	V_{IN} = 3.5V
- as Outputs (A7-A0, B7-B0)						
Low Level	V_{OL}	0	-	0.5	V	I_{IL} = 1.6mA
High Level	V_{OHh}	3.5	-	Vcc	V	I_{OHh} = 10 A See
	V_{OH1}	2.4	-	Vcc	V	I_{OH1} = 85 A Note 1
- as Inputs (A7-A0,B7-B0)						
Low Level	V_{IL}	0	-	0.8	V	
High Level	V_{IH}	2.4	-	Vcc	V	
- $\overline{A8}$ and Reset Input						
Pull up Current	I_{ILpu}	-10	-	-100	A	V_{IN} = 0.4V
	I_{IHpu}	-10	-	-50	A	V_{IN} = 2.4V
- A9						
Pull down Current	I_{IHpd}	10	-	100	A	V_{IN} = 2.4V
- BC1,BDIR, Clock Inputs						
Input Leakage	I_{ICL}	-10	-	10	A	V_{IN} = 0.4V to Vcc

**Typical values are at +25°C and nominal voltages.

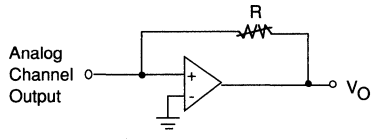
Note 1: The active pull-up during an output operation will achieve a logic 1 of 2.4 volts in a time of typically 1 microsecond. However, from 2.4 volts to the high level of 3.5 volts the available pull up current will reduce significantly and further edge transition will be highly dependent upon load capacitance.

AC CHARACTERISTICS	Sym	Min	Typ**	Max	Units	Conditions
Clock Input						
Frequency	fc	1	-	2	MHz	
Rise Time	tr	-	-	50	ns	Fig. 7
Fall Time	tf	-	-	50	ns	
Duty Cycle	-	40	50	60	%	
Bus Signals (BDIR, BC2, BC1)						
Associate Delay Time	tBD	-	-	40	ns	
Reset						
Reset Pulse Width	tRW	500	-	-	ns	Fig. 8
$\overline{A9}$, A8, DA7-DA0 (Address Mode)						
Address Setup Time	tAS	300	-	-	ns	
Address Hold Time	tAH	65	-	-	ns	Fig. 9
DA7-DA0 (Write Mode)						
Write Data Pulse Width	tDW	500	-	10,000	ns	
Write Data Setup Time	tDS	300	-	-	ns	Fig. 10
Write Data Hold Time	tDH	65	-	-	ns	
DA7-DA0 (Read Mode)						
Data Access Time from DTB	tDA	-	-	200	ns	Fig. 11
DA7-DA0 (Inactive Mode)						
Tri-state Delay Time from DTB	tTS	-	-	100	ns	
I/O Ports (A7-A0, B7-B0)						
Pull up Recovery Time	tPN	-	-	50	µsec	V_{OH} = 3.5V C_{LOAD} = 100pF See Note 2

**Typical values are at +25°C and nominal voltages

NOTE 2: Pull up recovery time is defined as the time required for any I/O pin A7-A0 or B7-B0 to change up to a 100pf capacitor load from 0.0 volts to 3.5 volts. This recovery time is conditional on the output function of Port A or Port B being deselected via Bits B7 and B6 of register R10.

Fig. 6 ANALOG CHANNEL OUTPUT TEST CIRCUIT



(OP AMP Must Not Saturate)

TIMING CONDITIONS FOR AC CHARACTERISTICS

FIG. 7 CLOCK AND BUS SIGNAL TIMING

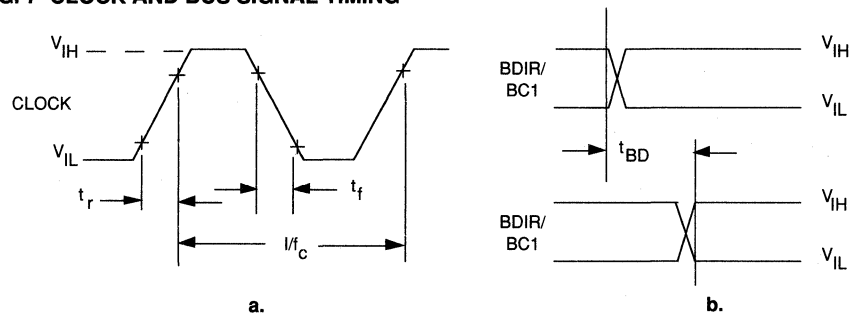


FIG. 8 RESET TIMING

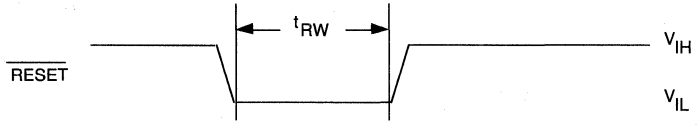


FIG. 9 LATCH ADDRESS TIMING

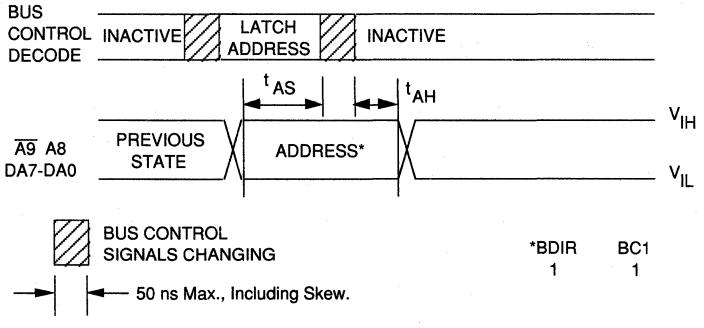


FIG. 10 WRITE DATA TIMING

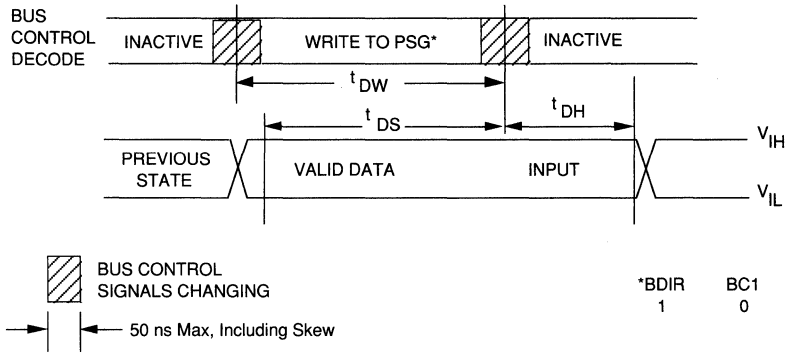
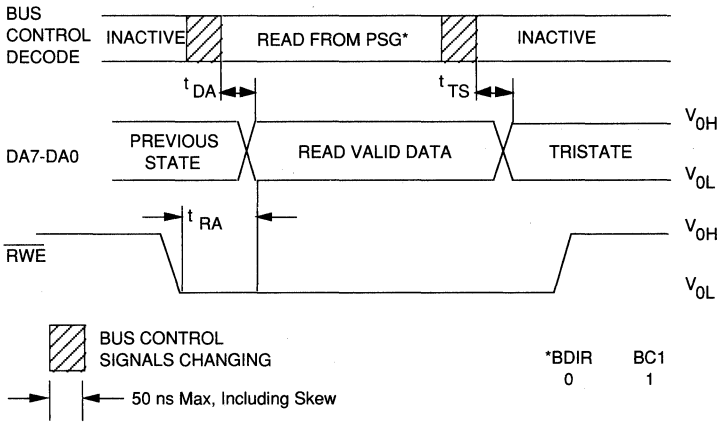


FIG. 11 READ DATA TIMING



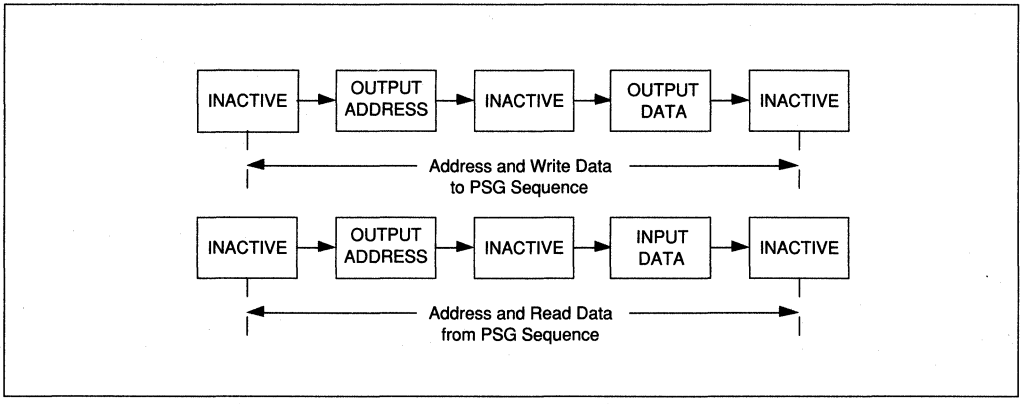
5

TIMING DIAGRAMS

State Timing

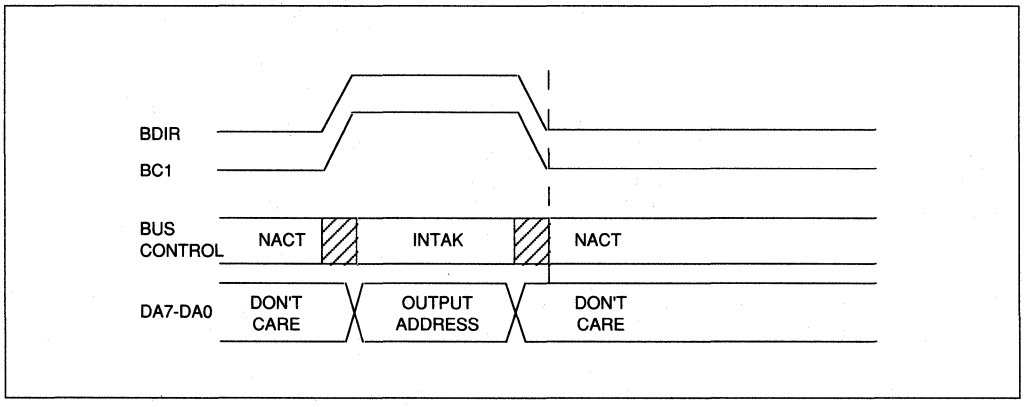
While the state flow for many microprocessors can be somewhat involved for certain operations, the sequence of events necessary to control the PSG is simple and straightforward. Each of the three major state sequences (Latch Address, Write to PSG, and Read from PSG) consists of several operations (indicated below by rectangular blocks) defined by the pattern of bus control signals (BDIR, BC1).

The functional operation and relative timing of the PSG control sequences are described in the following sections.



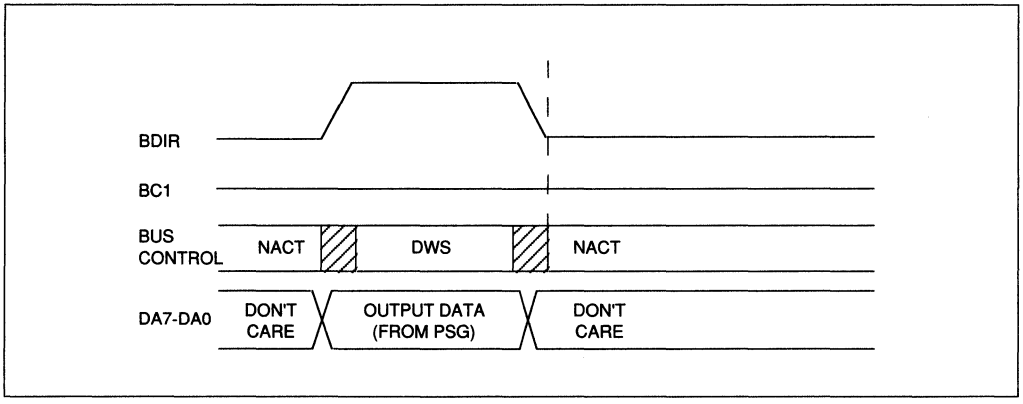
Address PSG Register Sequence

The Latch Address sequence is normally an integral part of the write or read sequences but for simplicity is illustrated here as in individual sequence. Depending upon the processor used, the program sequence will normally require four principal microstates: (1) send NACT (inactive); (2) send INTAK (latch address): (3) put address on bus; (4) send NACT (inactive).



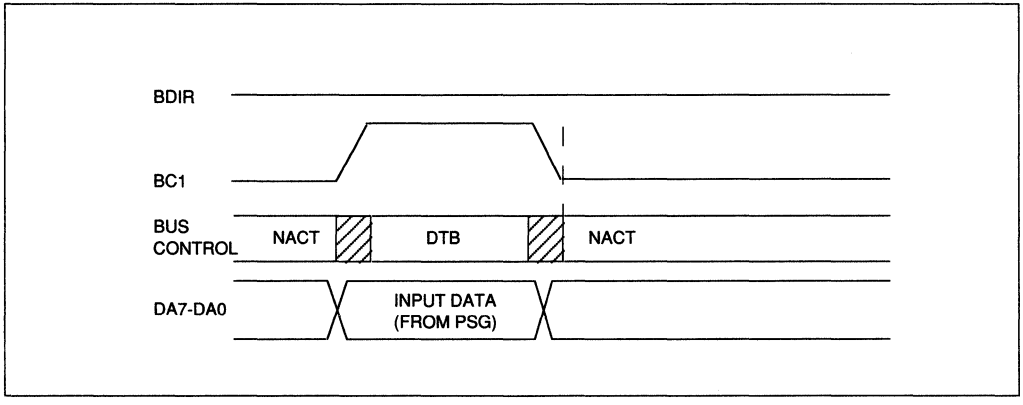
Write Data to PSG Sequence

The Write to PSG sequence, which would normally follow immediately after an address sequence, requires four principal microstates: (1) send NACT (inactive);(2) put data on bus; (3) send DWS (write to PSG); (4) send NACT (inactive).



Read Data From PSG Sequence

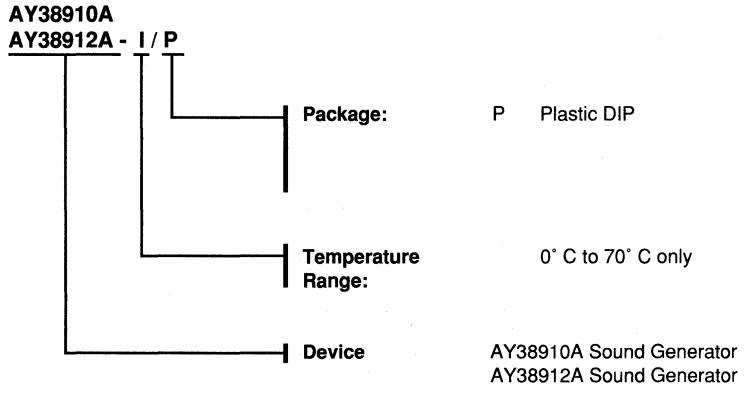
As with the Write to PSG sequence, the READ from PSG sequence would also normally follow immediately after an address sequence. The four principal microstates of the read sequence are: (1) send NACT (inactive); (2) send DTB (read from PSG); (3) read data on bus; (4) send NACT (inactive).



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

AY8930

Enhanced Programmable Sound Generator

FEATURES

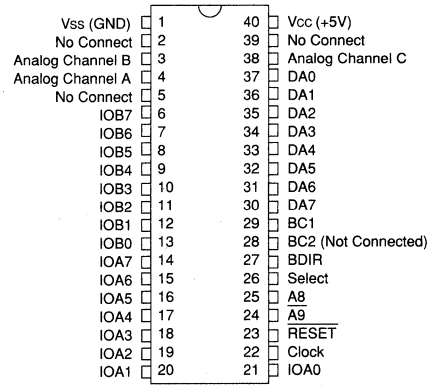
- Two Modes Available On-Chip
  - AY8930 Expanded Mode
  - AY38910A-Compatible Mode
- Improved Frequency Range
- Three Independently Programmable Analog Output Channels with Separate Frequency, Duty Cycle and Envelope Controls for Each Channel
- 5 Bits of Logarithmic Digital-to-Analog Conversion Per Channel
- Bus Interface Independent of Clock Frequency
- Input Clock Frequency: 2 or 4MHz
- Two 8-Bit General Purpose I/O Ports

PIN CONFIGURATION

40 LEAD DUAL INLINE

AY8930

Top View



DESCRIPTION

The AY8930 Enhanced Programmable Sound Generator (EPSG) is an LSI circuit that can produce a wide variety of complex sounds under software control. The AY8930 is manufactured in the Microchip Technology Inc. n-channel silicon gate process. The AY8930 is an enhanced version of the company's industry standard AY38910A sound generator. Enhanced features include improved frequency range and noise synthesis and independent control of each channel's envelope and duty cycle.

The PSG is easily interfaced to any bus-oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling, and personal computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable analog sound output channels available in the device. These analog sound output channels can each provide five bits of logarithmic digital-to-analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and can be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub- audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

DEVICE ARCHITECTURE

The AY8930 is a register oriented PSG. Communication between the microprocessor and the PSG is based on the concept of memory mapped I/O. Control commands are issued to the PSG by writing to these memory mapped registers . Each of the registers within the PSG is readable so that the microprocessor can determine, as necessary, present states or stored data values.

5

PIN FUNCTIONS

DA7-DA0 (Input /Output/High Impedance)
Data/Address Bits 7-0: Pins 30-37

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG, and to receive data from the PSG. In the address mode, DA3-DA0 select the internal register address (0-Fn) and DA7-DA4 in conjunction with address inputs $\overline{A9}$ and A8, form the chip select function. When the high order address bits are "incorrect," the bidirectional buffers are forced to a high impedance state.

$\overline{\text{Address 9}}$, Address 8
A8 (input): Pin 25
$\overline{A9}$ (input): Pin 24

High order address bits $\overline{A9}$ and A8 are fixed to recognize a "01" code. They may be left unconnected, as each is provided with either an on chip pull-down ($\overline{A9}$) or pull-up (A8) resistor. In noisy environments, however, it is recommended that $\overline{A9}$ and A8 be tied to external ground and +5V respectively, if they are not to be used.

RESET (Input): Pin 23

For initialization/power-on purposes, applying a low level input to the $\overline{\text{RESET}}$ pin will reset all registers to 0. (See following table). The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor.

Register (in Hex)	B7	B6	B5	B4	B3	B2	B1	B0
R0/R0A	0	0	0	0	0	0	0	0
R1/R1A	0	0	0	0	0	0	0	0
R2/R2A	0	0	0	0	0	0	0	0
R3/R3A	0	0	0	0	0	0	0	0
R4/R4A	0	0	0	0	0	0	0	0
R5/R5A	0	0	0	0	0	0	0	0
R6/R6A	0	0	0	0	0	0	0	0
R7/R7A	0	0	0	0	0	0	0	0
R8/R8A	#	#	0	0	0	0	0	0
R9/R9A	#	#	0	0	0	0	0	0
RA/RAA	#	#	0	0	0	0	0	0
RB/RBA	0	0	0	0	0	0	0	0
RC/RCA	0	0	0	0	0	0	0	0
RD/RDA/RDB	0	0	0	0	0	0	0	0
RE/REA	0	0	0	0	0	0	0	0
RF/RFA	0	0	0	0	0	0	0	0
R0B	0	0	0	0	0	0	0	0
R1B	0	0	0	0	0	0	0	0
R2B	0	0	0	0	0	0	0	0
R3B	0	0	0	0	0	0	0	0
R4B	#	#	#	#	X	X	X	X
R5B	#	#	#	#	X	X	X	X
R6B	#	#	#	#	X	X	X	X
R7B	#	#	#	#	X	X	X	X
R8B	#	#	#	#	X	X	X	X
R9B	0	0	0	0	0	0	0	0
RAB	X	X	X	X	X	X	X	X
RFB	0	0	0	0	0	0	0	0

- X indicates a don't care.
- # indicates that there is no physical memory element for a bit; if read, a 0 will be returned.
- All counter work registers will be initialized to zeros.
- The noise generator 17-bit shift register will be initialized to ones.
- The noise value register will be initialized to zeros.

CLOCK (Input): Pin 22

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

CLOCK DIVIDE - SELECT (Input): Pin 26

Select = 0 Input Clock = 4 MHz max.
(Divided internally by 2)
Select = 1 Input Clock = 2 MHz max.
The select pin is provided with an internal pull-up resistor such that the pin default condition is Select = 1.

BDIR, BC2, BC1 (Inputs): Pins 27, 28, 29

Bus Direction, Bus Control 2*, Bus Control 1
* Not connected

Analog Channel A, B, C (Outputs): Pins 4, 3, 38

Each of these signals is the output of its corresponding digital-to-analog converter, and provides 1V peak-peak (max) signal representing the complex sound wave-shape generated by the PSG.

No Connect: Pins 2, 5, 39

These pins are for Microchip Technology test purposes only and should be left open. Do not use as tie-points.

Vcc: Pin 40, Nominal +5 Volt power supply to the PSG.

Vss: Pin 1, Ground reference for the PSG.

INPUT CONTROL SIGNALS

Interfacing to the AY8930 requires the generation of only two of the three AY38910A input control signals, BDIR and BC1. BC2 is shown on the pinout diagram for reference only; the pin is not internally connected.

INPUT CONTROL SIGNALS

BDIR	BC1	Function
0	0	INACTIVE: The PSG/CPU bus is inactive. DA7-DA0 are in a high impedance state.
0	1	READ FROM PSG: This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7-DA0 are in the output mode.
1	0	WRITE TO PSG: This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7-DA0 are in the input mode.
1	1	LATCH ADDRESS: This signal indicates that the bus contains a register address which should be latched by the PSG. DA7- DA0 are in the input mode.

5

REGISTER ARRAY

The principal element of the AY8930 is an array of 27 control registers arranged in one bank of 16 and one bank of 11 registers. These registers occupy 16 address locations of the 1,024-word memory space in which the PSG resides.

The configuration of this register array is shown on the following pages. Note the two modes of operation: 8910A-compatibility mode and 8930 expanded mode.

The registers are addressed via the combination of the bidirectional data bus (DA0-DA7) and address input pins A8 and $\overline{A9}$.

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	X	X	X	X

DA0-DA3 These four low-order address bits are used to select one of the internal registers within a bank.

DA4-DA7, A8, $\overline{A9}$ These six high-order address bits function as chip selects and are used to position the register bank(s) within the 1,024-word memory space. In the deselected state, the data bus is in the high impedance state.

The address enable code for bits DA4-DA7 is all zeros.

Inputs A8 and $\overline{A9}$ are enabled by a high on A8 and a low on $\overline{A9}$; all other input level combinations result in a deselected condition. Pins A8 and $\overline{A9}$ have an on-chip pull-up and pull-down resistor, respectively, and will assume the correct logic level if left unconnected.

Address bits DA7-DA0 are latched internally. This internally latched address is updated and modified on every "latch address" signal presented to the PSG via the BDIR and BC1 control lines.

The AY8930 initializes in the AY38910A-compatibility mode. To utilize the expanded features of the AY8930, an access code must be input to register R15 upon program initialization.

Entering a "101" code in bits B7-B5 of register R15 selects the 8930 expanded mode. In the 8930 expanded mode, bit B4 = 0 (R15) selects BANK A and B4 = 1 selects BANK B. All other bit selections are defined as 8910A-compatibility mode. Registers R15A and R15B are mapped into the same physical register.

Switching modes causes loss of all register data from the previous mode. All registers will be initialized except for the Mode Select code of R15.

Shown on the next page is the register configuration for the AY8930. Note that Bank A of the expanded mode is virtually identical to the single register array of the 8910A-compatibility mode.

AY8930 REGISTER ARRAY: AY38910A-COMPATIBILITY MODE

Register			Bit							
Hex	Octal	Function	B7	B6	B5	B4	B3	B2	B1	B0
R0	R0	Channel A	8-Bit Fine Tune							
R1	R1	Tone Period					4-Bit Coarse Tune			
R2	R2	Channel B	8-Bit Fine Tune							
R3	R3	Tone Period					4-Bit Coarse Tune			
R4	R4	Channel C	8-Bit Fine Tune							
R5	R5	Tone Period					4-Bit Coarse Tune			
R6	R6	Noise Period				5-Bit Period Control				
			IN/OUT		NOISE			TONE		
R7	R7	$\overline{\text{Enable}}$	IOB	IOA	C	B	A	C	B	A
R8	R10	Channel A Amplitude				M	L3	L2	L1	L0
R9	R11	Channel B Amplitude				M	L3	L2	L1	L0
RA	R12	Channel C Amplitude				M	L3	L2	L1	L0
RB	R13	Envelope Period	8-Bit Fine Tune							
RC	R14		8-Bit Coarse Tune							
RD	R15	Envelope Shape/Cycle	MODE SELECT				CONT.	ATT.	ALT.	HOLD
RE	R16	I/O Port A	8-Bit Parallel I/O on Port A							
RF	R17	I/O Port B	8-Bit Parallel I/O on Port B							

5

AY8930 REGISTER ARRAY: EXPANDED CAPABILITY MODE - BANK A

Register			Bit							
Hex	Octal	Function	B7	B6	B5	B4	B3	B2	B1	B0
R0A	R0A	Channel A	8-Bit Fine Tune							
R1A	R1A	Tone Period	8-Bit Coarse Tune							
R2A	R2A	Channel B	8-Bit Fine Tune							
R3A	R3A	Tone Period	8-Bit Coarse Tune							
R4A	R4A	Channel C	8-Bit Fine Tune							
R5A	R5A	Tone Period	8-Bit Coarse Tune							
R6A	R6A	Noise Period	8-Bit Noise Period							
			IN/OUT		NOISE			TONE		
R7A	R7A	$\overline{\text{Enable}}$	IOB	IOA	C	B	A	C	B	A
R8A	R10A	Channel A Amplitude			M	L4	L3	L2	L1	L0
R9A	R11A	Channel B Amplitude			M	L4	L3	L2	L1	L0
RAA	R12A	Channel C Amplitude			M	L4	L3	L2	L1	L0
RBA	R13A	Channel A	8-Bit Fine Tune							
RCA	R14A	Envelope Period	8-Bit Coarse Tune							
RDA	R15A	Bank A/B: Envelope A	1	0	1	0	CONT.	ATT.	ALT.	HOLD
REA	R16A	I/O Port A	8-Bit Parallel I/O on Port A							
RFA	R17A	I/O Port B	8-Bit Parallel I/O on Port B							

AY8930 REGISTER ARRAY: EXPANDED CAPABILITY MODE - BANK B

Register			Bit							
Hex	Octal	Function	B7	B6	B5	B4	B3	B2	B1	B0
R0B	R0B	Channel B	8-Bit Fine Tune							
R1B	R1B	Envelope Period	8-Bit Coarse Tune							
R2B	R2B	Channel C	8-Bit Fine Tune							
R3B	R3B	Envelope Period	8-Bit Coarse Tune							
R4B	R4B	Envelope Shape/Cycle B					CONT.	ATT.	ALT.	HOLD
R5B	R5B	Envelope Shape/Cycle C					CONT.	ATT.	ALT.	HOLD
R6B	R6B	Channel A Duty Cycle					4-Bit			
R7B	R7B	Channel B Duty Cycle					4-Bit			
R8B	R10B	Channel C Duty Cycle					4-Bit			
R9B	R11B	Noise "And" Mask	8-Bit							
RAB	R12B	Noise "Or" Mask	8-Bit							
RBB	R13B*									
RBC	R14B*									
RBD	R15B	Bank A/B: Envelope A	1	0	1	1	CONT.	ATT.	ALT.	HOLD
RBC	R16B*									
RBF	R17B*	TEST	NOT TO BE ACCESSED BY THE USER							

* Not accessible in AY8930 mode.

NOTE: All unused bits will be read back as "0".

5

SOUND GENERATING BLOCKS

The basic blocks in the PSG that produce the programmed sounds include:

Tone Generators - Produce the basic pulse tone frequencies for each channel (A, B, C).

Noise Generator - Produces a frequency modulated pseudorandom noise output.

Mixers - Combine the outputs of the tone generators and the noise generator. One for each channel (A, B, C).

Amplitude Control - Provides the D/A converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the envelope generators, one for each channel (A, B, C).

Envelope Generators - Produce an envelope pattern that can be used to amplitude modulate the output of the mixer, one for each channel (A, B, C).

D/A Converters - The three D/A converters each produce up to a 32-level output signal as determined by the amplitude control.

OPERATION

Since all functions of the PSG are controlled by a host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers*	Function
Tone Generator Control	R0A-R5A	Program tone periods
Duty Cycle Control	R6B-R8B	Select duty cycle
Noise Generator Control	R6A, R9B-RAB	Program noise period
Mixer Control	R7A	Enable tone/noise on selected channels
Amplitude Control	R8A-RAA	Select "fixed" or "variable" amplitudes
Envelope Generator Control	RBA-RDA, R0B-R5B	Program envelope period and envelope pattern
D/A Converters		Produces a 32-bit output signal

*All registers referenced are for the AY8930 Expanded Mode.

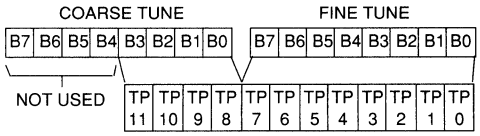
TONE GENERATOR CONTROL

Each analog output channel has associated with it two registers which specify the tone period for that channel, the coarse tune and the fine tune registers. The tone period for each channel is obtained by combining the coarse and fine tune registers as shown.

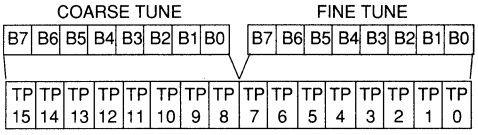
Note that the value programmed in the combined coarse and fine tune registers is a *period* value- the higher the value in the registers, the lower the resultant frequency.

Coarse Tune Registers	Channel	Fine Tune Register
R1A	A	R0A
R3A	B	R2A
R5A	C	R4A

12-BIT TONE PERIOD (TP) VALUE: AY38910A-COMPATIBILITY MODE



16-BIT TONE PERIOD (TP) VALUE: AY8930 EXPANDED MODE



PERIOD OF OUTPUT = 16 x TP x P
WHERE P = PERIOD OF INPUT CLOCK AND
TP = DECIMAL EQUIVALENT OF TONE PERIOD BITS TP15-TP0

If the coarse and fine tune registers are both set to 00h, the resulting period will be minimum, i.e. the generated tone period will be as if the coarse tune register were set to 00h and the fine tune register were set to 01h. The counter will count the period value down to zero. When zero is reached, the period value will be reloaded into the counter.

DUTY CYCLE CONTROL

The duty cycle of each pulse generated by the three tone generators is controlled by an associated 4-bit duty cycle register (R6B, R7B, and R8B).

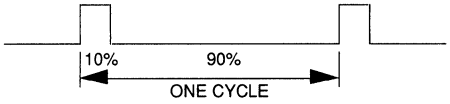
The following duty cycles are selectable:

% Duty Cycle	Duty Cycle	Register Value
3.125%	0	0000
6.25 %	1	0001
12.50%	2	0010
25.00%	3	0011
50.00%	4	0100
75.00%	5	0101
87.50%	6	0110
93.75%	7	0111
96.875%	8*	1000

* NOTE: Any value greater than 8_{10} decodes as an 8_{10}.

NOTE:

The percent duty cycles refers to the high (logic high) portion of the duty cycle. The low portion is then 100% duty cycle. For example, a 10% duty cycle is then 10% up and 90% down, as shown below.



In AY8910A-compatibility mode, the duty cycle is fixed at 50%. The capability for a variable duty cycle exists only in the expanded AY8930 mode.

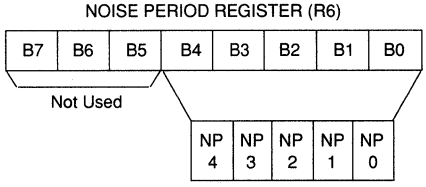
In order to change a duty cycle, the appropriate duty cycle register must be updated. The new duty cycle will then remain constant at this value until the duty cycle register is modified. The new duty cycle value will take effect immediately. This may result in one period with a "random" duty cycle at the time the register is updated.

NOISE GENERATOR CONTROL

AY38910A-COMPATIBILITY MODE:

Noise is generated by a 17-bit polynominal shift register. The period of the clock to this shift register is specified by the 8-bit binary value NP.

The noise period value is derived from the lower five bits (B4-B0) of the noise period register (R6) as shown.



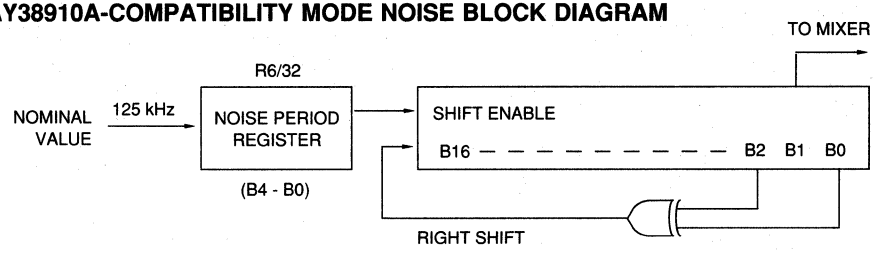
5 BIT NOISE PERIOD (NP) VALUE

NOTE:

As with the tone period, the lowest period value is 01h (divide by 1), an entry of 00h will have the same value as 01h; the highest period value is 1Fh (divide by 31_{10}).

5

AY38910A-COMPATIBILITY MODE NOISE BLOCK DIAGRAM



AY8930 EXPANDED MODE:

In the AY8930 expanded mode, noise is generated using a 17-bit polynomial shift register, an "AND" mask, an "OR" mask, and an 8-bit noise period value. The least significant byte of the polynomial shift register is logically AND'ed with the "AND" mask specified in Register 11B, then logically OR'ed with the "OR" mask specified in Register 12B. The result is stored in a temporary register which is clocked each time the counter associated with the 8-bit noise period register (R6A) reaches zero. When the noise value reaches zero, a new value is fetched from the polynomial shift register and the process is repeated. The noise output is toggled each time the noise value reaches zero.

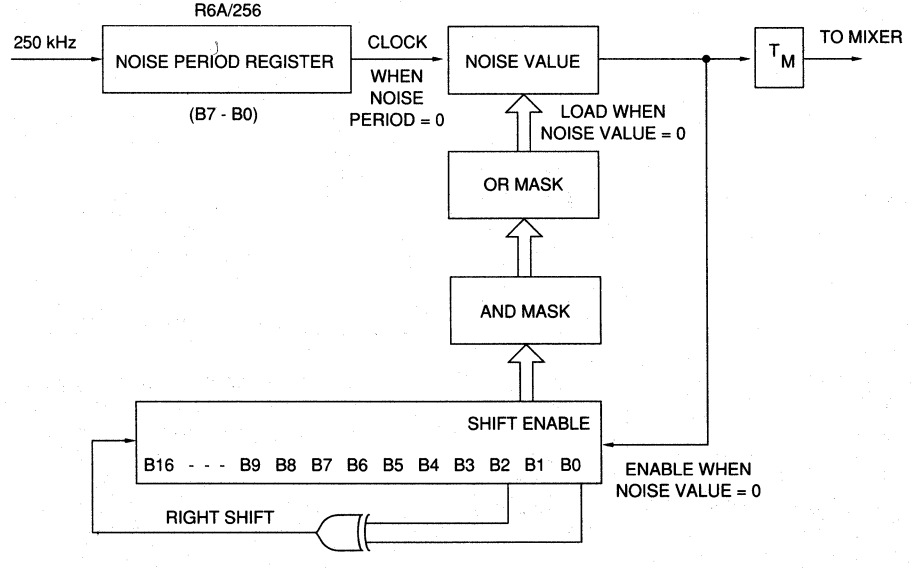
NOISE PERIOD REGISTER (R6A)

B7	B6	B5	B4	B3	B2	B1	B0
NP 7	NP 6	NP 5	NP 4	NP 3	NP 2	NP 1	NP 0

8 BIT NOISE PERIOD (NP) VALUE

The lowest period value is 01h (divide by 1), an entry 00h will have the same value as 01h; the highest period value is FFh (divide by 255_{10}.)

AY8930 EXPANDED MODE NOISE BLOCK DIAGRAM



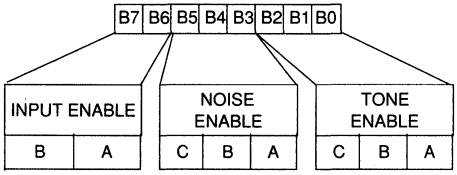
MIXER CONTROL - I/O ENABLE

Register 7A is a multi-function $\overline{\text{Enable}}$ register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports. The mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5-B0 of R7A.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7A.

These functions are illustrated in the following:

MIXER CONTROL - I/O ENABLE REGISTER (R7A)



Noise Enable Truth Table

R7A Bits B5	B4	B3	Noise Enabled On Channel		
0	0	0	C	B	A
0	0	1	C	B	-
0	1	0	C	-	A
0	1	1	C	-	-
1	0	0	-	B	A
1	0	1	-	B	-
1	1	0	-	-	A
1	1	1	-	-	-

Tone Enable Truth Table

R7A Bits B2	B1	B0	Tone Enabled On Channel		
0	0	0	C	B	A
0	0	1	C	B	-
0	1	0	C	-	A
0	1	1	C	-	-
1	0	0	-	B	A
1	0	1	-	B	-
1	1	0	-	-	A
1	1	1	-	-	-

The direction of the I/O Port(s) is determined as follows:

I/O Port Truth Table

R7A Bits B7	B6	I/O Direction IOB	IOA
0	0	In	In
0	1	In	Out
1	0	Out	In
1	1	Out	Out

Note: The Mixer - I/O Control function is identical in both modes of operation.

Disabling noise and tone does not turn off a channel. Turning off a channel can only be accomplished by writing all zeros into corresponding amplitude control register.

I/O PORT DATA STORE

Registers REA and RFA function as intermediate data storage registers between the PSG/CPU data bus (DA0-DA7) and the two I/O ports (IOA0-IOA7, IOB0-IOB7). Both I/O ports are available on the AY8930.

Using registers REA and RFA for the transfer of I/O data has no effect on sound generation.

To output data from the CPU Bus to a peripheral device connected to I/O port A:

1. Address the enable register (R7A).
2. Set the port A direction bit to output (write "1" to bit B6 of R7A).
3. Address the I/O port A register (REA).
4. Write data to I/O port A register. The data will pass through the PSG I/O port A register to the I/O port bus.

To input data from I/O port A to the CPU bus:

1. Address the enable register (R7A).
2. Set the port A direction bit to input (write a "0" to bit B6 of R7A).
3. Address the I/O port A register (REA). The contents of the port register will follow the signals applied to the I/O port.
4. Read data from I/O port A register. The data will be transferred from the PSG I/O port A register to the CPU bus as in a normal read operation.

If a logic 1 has been written to any bit position of register REA or register RFA and the corresponding I/O pins of port A or port B are externally pulled below the logic 0, (V_{IL}) level, a subsequent CPU read instruction of registers REA or RFA will actually contain a logic 0 in the pulled down bit positions. The output pins will return to logic 1 if the pull down condition is removed.

If a logic 0 has been written to any bit position of the I/O registers and the external world wishes to pull these pins to a 1, the user should be aware that an impedence conflict will exist between the pull down transistor and the external driver.

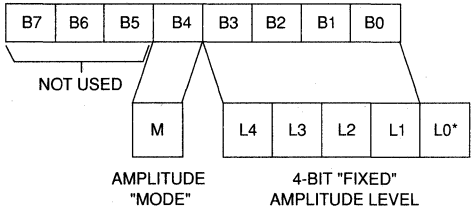
5

AMPLITUDE CONTROL

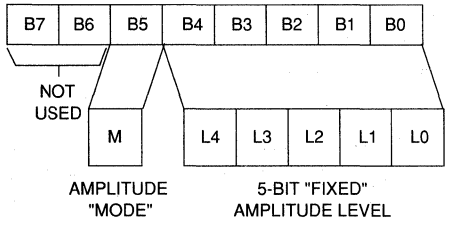
The amplitudes of the signals generated by each of the three D/A converters (one each for channels A, B, and C) are determined by the contents of the amplitude control registers as illustrated in the following:

Amplitude Control Register #	Channel
R8A	A
R9A	B
RAA	C

AY38910A-COMPATIBILITY MODE:



AY8930 EXPANDED MODE:



The amplitude "mode" (bit M) selects either fixed level amplitude (M = 0) or variable level amplitude (M = 1). It follows that bits L4 - L0, defining the value of a "fixed" level amplitude, are only active when M = 0. The amplitude is only "fixed" in the sense that the amplitude level is under the direct control of the system processor via an address latch/write data sequence.

When "variable amplitude" is selected (M = 1), the amplitude of each channel is determined by the envelope pattern as defined by the envelope generators 5-bit output (E4 - E0). The amplitude "mode" bit (bit M) can also be thought of as an envelope enable bit, i.e. when M = 1, the envelope is enabled.

The following is a chart describing all combinations of the 6-bit Amplitude Control.

M	L4	L3	L2	L1	L0	
0	0	0	0	0	0*	The amplitude is fixed at 1 of 31 levels as determined by L4, L3, L2, L1, L0.
0	0	0	0	0	1*	
•	•	•	•	•	•	
•	•	•	•	•	•	
0	1	1	1	1	1	
1	X	X	X	X	X	The amplitude is variable at 31 levels as determined by the output of the Envelope Generator.

(X = Don't care)

NOTE:

In the AY38910A-compatibility mode, the externally driven "fixed" amplitude is limited to a total of 16 possible levels determined by amplitude bits L4-L1.

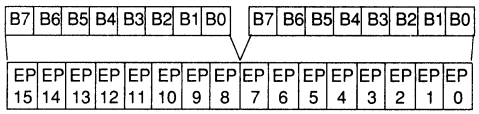
ENVELOPE GENERATOR CONTROL

ENVELOPE PERIOD CONTROL

The period of the sound envelope, in the AY38910A-compatibility mode, is controlled by two 8-bit registers, RB and RC (the envelope fine and coarse tune, respectively). In the 8930 expanded mode, each analog output channel has its own independent sound envelope. Changes to the envelope period counter will occur at envelope period boundary or when envelope shape/cycle register is loaded.

Coarse Tune Register	Channel	Fine Tune Register
RCA	A	RBA
R1B	B	R0B
R3B	C	R2B

16-BIT ENVELOPE PERIOD TO ENVELOPE GENERATOR



Note that the value programmed in the combined coarse and fine tune registers is a period value - the higher the value in the registers, the lower the resultant frequency.

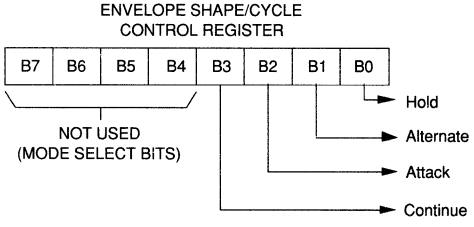
Note also, that as with the tone period, the lowest period value is 0001h (divided by 1); the highest period value is FFFFh (divided by $65{,}535_{10}$).

ENVELOPE SHAPE/CYCLE CONTROL

The AY8930 envelope generator further counts down the envelope frequency by 32, producing a 32-state per cycle envelope pattern defined by its 5-bit counter output, E4, E3, E2, E1, and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/ count down) of the 5-bit counter and by defining a single cycle repeat-cycle pattern. The AY38910A mode envelope generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0.

Loading of the envelope shape/cycle control register will reset the associated counter to the appropriate initial state and reset the envelope period counter for that channel.

The envelope shape/cycle control is contained in the lower 4 bits (B3-B0) of the respective envelope control registers. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:



The definition of each function is as follows:

Hold - When set to logic "1" in AY38910A mode, limits the envelope to one cycle, holding the last count of the envelope counter (E3 - E0 = 0000 or 1111, depending on whether the envelope counter was in a count-down or count-up mode, respectively).

Alternate - When set to logic "1", the envelope counter reverses count direction (up-down) after each cycle.

NOTE: When both the hold bit and the alternate bit are ones, the envelope counter is reset to its initial count before holding.

Attack - When set to logic "1" in AY38910A mode, the envelope counter will count up (attack) from E3, E2, E1, E0 = 0000 to E3, E2, E1, E0 = 1111; when set to logic "0", the envelope counter will count down (decay) from 1111 to 0000.

Continue - When set to logic "1", the cycle pattern will be as defined by the hold bit; when set to logic "0", the envelope generator will be reset to 0000 after one cycle and hold at that count.

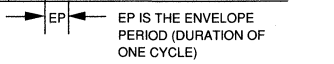
Further description of the above functions could be accomplished by numerous charts of the binary count sequence of E3, E2, E1, E0 for each combination of hold, alternate, attack and continue. However, since these ouputs are used (when selected by the amplitude control registers) to amplitude modulate the output of the mixers, a better understanding of their effect can be accomplished via a graphic representation of their value for each condition selected, as illustrated in the Envelope Shape/Cycle Control figure to the right and the Detail of Two Cycles figure below.

For AY8930 mode, hold, alternate, attack and continue is the same, however the pattern is defined by 5 bits (E4, E3, E2, E1, E0.)

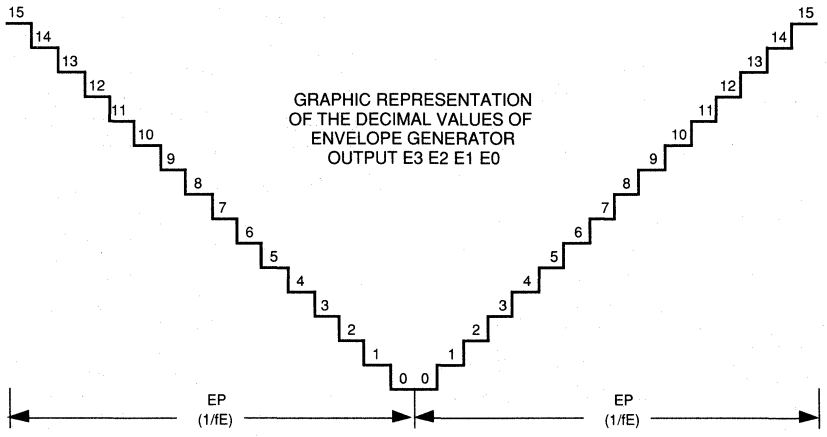
5

ENVELOPE SHAPE/CYCLE CONTROL

RD BITS				AY38910A MODE
B3	B2	B1	B0	
CONTINUE	ATTACK	ALTERNATE	HOLD	GRAPHIC REPRESENTATION OF ENVELOPE GENERATOR OUTPUT E3 E2 E1 E0.
0	0	X	X	
0	1	X	X	
1	0	0	0	
1	0	0	1	(SEE FIG. BELOW FOR DETAIL)
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



DETAIL OF TWO CYCLES - AY38910A MODE

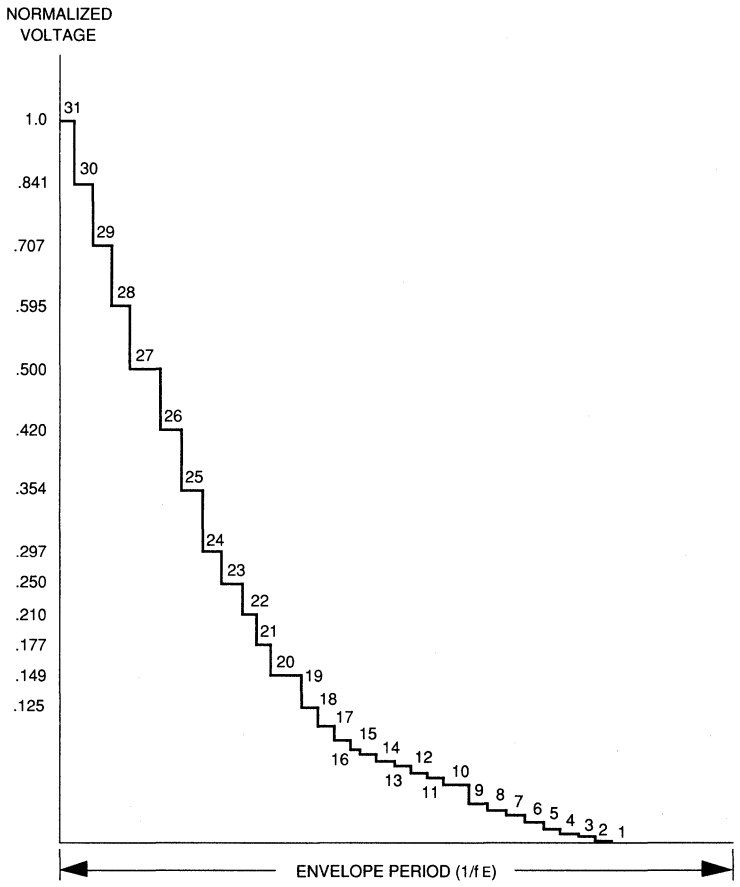


DIGITAL TO ANALOG CONVERTER

The Digital to Analog conversion is performed in logarithmetic steps with a normalized voltage range of 0V to 1.0V. The specified amplitude of each converter is controlled by a 5-bit word from either the amplitude control register* or the envelope generator. The signal of the output is the Noise/Tone specified for that channel.

* Except in the 8910A-compatibility mode, which only allows for 4 bits of external amplitude control.

D/A CONVERTER OUTPUT - AY8930 EXPANDED MODE



THIS FIGURE ILLUSTRATES THE D/A CONVERTER OUTPUT WHICH WOULD RESULT IF NOISE AND TONES WERE DISABLED AND AN ENVELOPE CONTROLLED VARIABLE AMPLITUDE WERE SELECTED.

NOTE: THE RESET CONDITION IS ZERO CURRENT.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage temperature.....-55°C to +150°C
Maximum temperature under bias ..... +125°C
V_{DD} and all other input/output
voltages with respect to V_{SS}.....-0.3V to +7.0V

Standard Conditions (Unless otherwise noted)
Free air ambient operating
temperature ..... 0°C to +70°C
V_{DD} ..... +4.5V to +5.5V
V_{SS} ..... 0.0V (Ground)

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Logic Levels						
Logic 0	V_{IL}	-0.3	-	+0.4	Volts	
Logic 1	V_{IH}	+ 2.4		V_{DD}	Volts	
Input Leakage						
Clock	-	-	-	10	µA	
BC1, BDIR	-	-	-	10	µA	
Inputs with Pullups	I_{IL}	10	-	100	µA	V_{IN} = +0.4V
A8, RESET, Select						
Inputs with Pulldowns	I_{IH}	10	-	50	µA	V_{IN} = +2.4V
A9						
I/O with Pullups						
A7-A0, B7-B0	I_{IL}	20	-	150	µA	V_{IN} = +0.4V
	V_{OH}	+2.4	-	V_{DD}	Volts	I_{OH} = 100 µA w/100pF
	V_{OL}	0.0	-	+0.4	Volts	I_{OL} = 1.6 mA w/100pF
Data/Address						
DA7-DA0	V_{OH}	+2.4	-	V_{DD}	Volts	I_{OH} = 100 µA w/100pF
	V_{OL}	0.0	-	+0.4	Volts	I_{OL} = 1.6 mA w/100pF
Power Supply	I_{DD}	-	-	85	mA	All inputs and outputs tied to V_{SS} or V_{DD}.

AC CHARACTERISTICS *

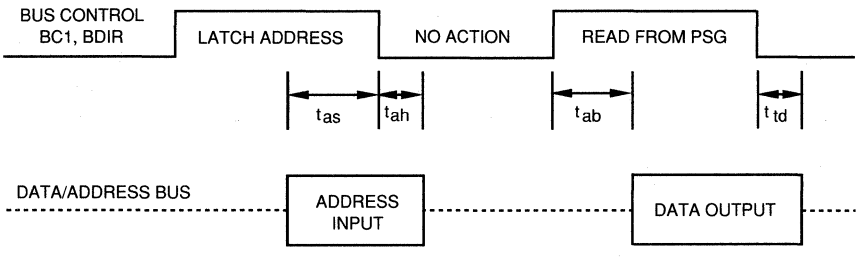
Parameters	Sym	Min	Typ	Max	Units	Conditions
Clock Input						
Frequency	-	1	-	4	MHz	40/60 asymmetry
Rise/Fall Time	tr, tf	0	-	50	ns	allowed
Master Reset						
RESET	tms	*	-	-	ns	*Two Clock Periods
Control Signals						
BC1, BC2, BDIR						
Skew	tcs	-	-	40	ns	
Valid	tccs	300	-	-	ns	
Data Address Bus						
DA7-DA0, A8, A9						
Address Setup Time	tas	300	-	-	ns	
Address Hold Time	tah	65	-	-	ns	
Read Mode						
Data Setup Time	tab	-	-	200	ns	
Data Hold Time	ttd	20	-	100	ns	
Write Mode						
Data Setup Time	tds	300	-	-	ns	
Data Hold Time	tdh	65	-	-	ns	
Input/Output Port						
IOA7-IOA0, IOB7-IOB0						
Output Mode						
Data Setup Time	tpw	500	-	-	ns	
Input Mode						
Data Setup Time	tprs	200	-	-	ns	
Data Hold Time	tprh	65	-	-	ns	

* The address/data read cycle is latch address followed by an inactive state then the read command. The address/data write cycle would be the same with the substitution of the write command in place of the read. An inactive state is required between each cycle (or active command).

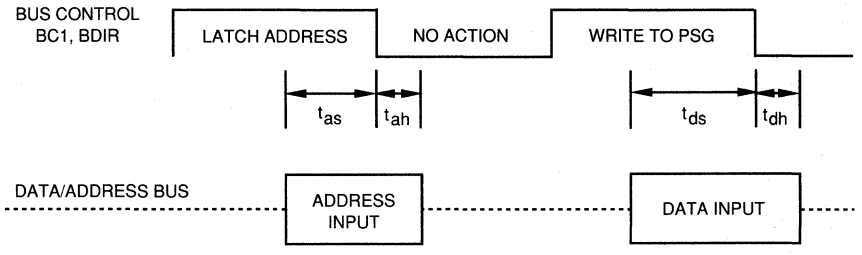
5

TIMING DIAGRAMS

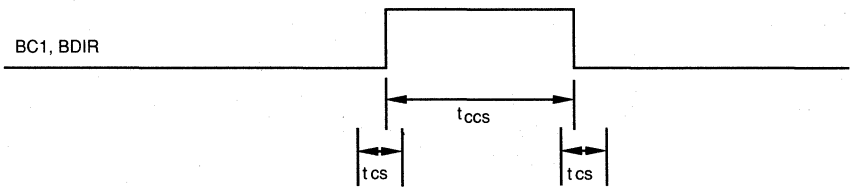
READ MODE



WRITE MODE

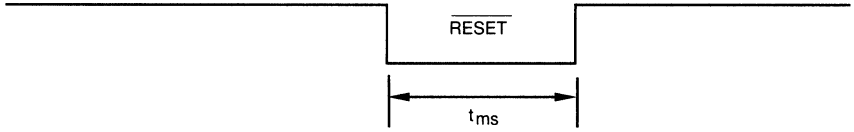


BUS CONTROL SIGNALS

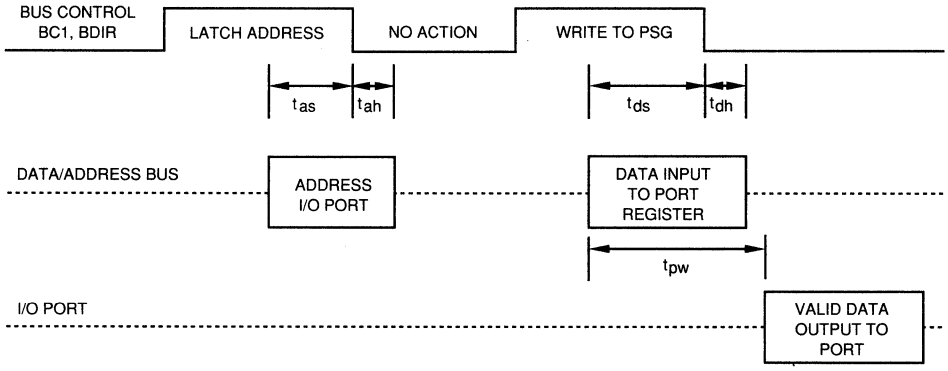


TIMING DIAGRAMS (Cont.)

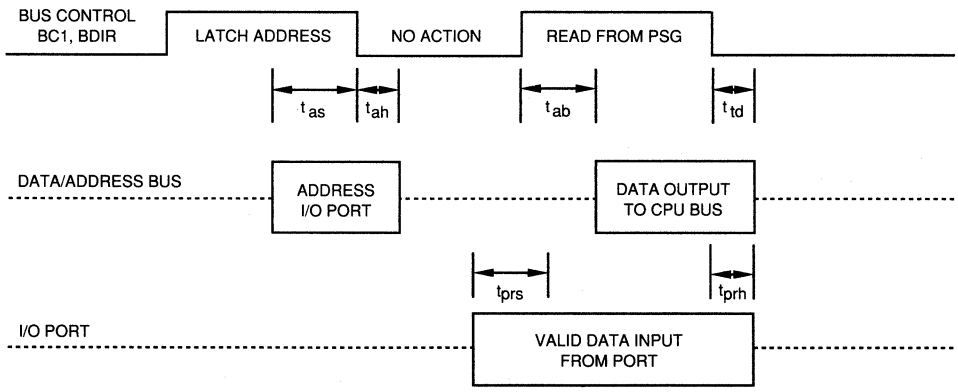
MASTER RESET



I/O PORT OUTPUT MODE: WRITE DATA FROM CPU BUS TO I/O PORT*



I/O PORT INPUT MODE: WRITE DATA FROM I/O PORT TO CPU BUS*

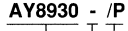


* Assume the direction of the I/O port has already been determined via a write to the Enable register (R7A).

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package	P	40-Pin Plastic DIP
Temperature Range	Blank	0° C to 70° C
Device	AY8930	Enhanced Programmable Sound Generator

AY0438-I

32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low power operation, high noise immunity, wide temperature range
- CMOS, NMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines
- Can be used to drive relays, solenoids, print head drives, etc.

APPLICATIONS

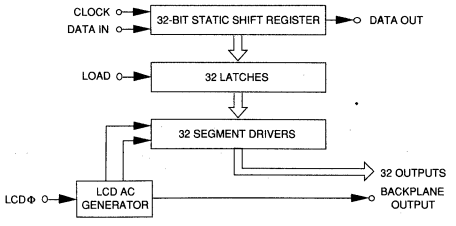
- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

The AY0438-I is a CMOS LSI circuit that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438-I can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14-, or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438-I devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

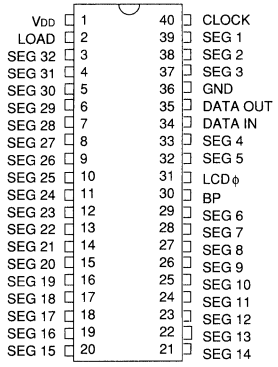
BLOCK DIAGRAM



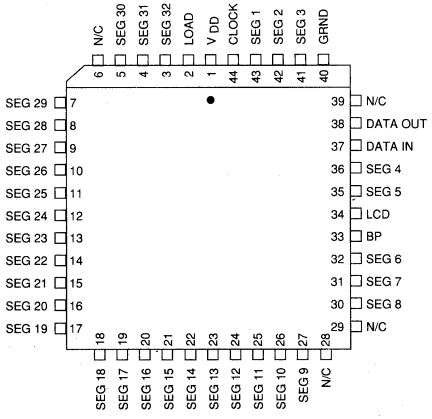
PIN CONFIGURATION

40 LEAD DUAL INLINE

Top View



44 PLCC



The device also acts as a versatile peripheral, able to drive displays, motors, relays, and solenoids within its output limitations.

The AY0438-I is available in 40 lead dual-in-line ceramic and plastic packages. Unpackaged dice are also available.

PIN DESCRIPTION

Pin #	Name	Direction	Description
1	V_{DD}		Supply voltage
2	Load	Input	Latch data from registers
3-29, 32, 33, 37-39	Seg 1-32	Output	Direct drive outputs
30	BP	Output	Backplane drive output
31	LCDΦ	Input	Backplane drive input
34	Data In	Input	Data input to shift register
35	Data Out	Output	Data output from shift register
36	V_{SS}	Ground	Ground
40	Clock	Input	System clock input

FIGURE 1 TIMING DIAGRAM

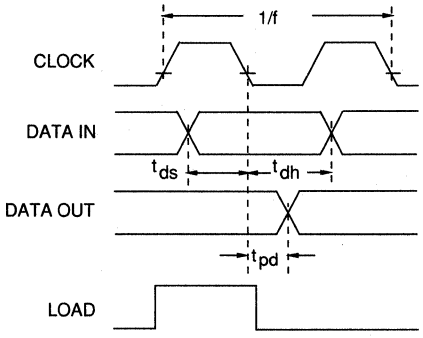
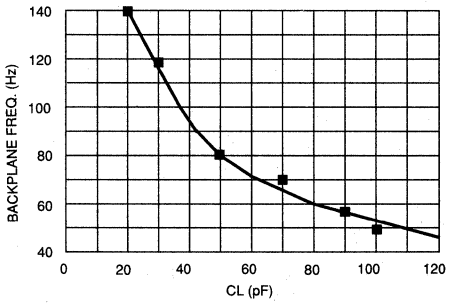


FIGURE 2 OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of the clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers.
4. If LCDΦ is driven, it is in phase with the backplane output.
5. To cascade units, either connect backplane of one circuit to LCDΦ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. If the former is chosen, tie just one backplane to the LCD and use a different backplane output to drive the LCDΦ inputs. The data can be loaded to all circuits in parallel or else Data Out can be connected to Data In to form a long serial shift register.
6. The supply voltage of the AY04381 is equal to half the peak driving voltage of the LCD.
7. The LCDΦ pin can be used in two modes, driven or oscillating. If LCDΦ is driven, the circuit will sense this condition and pass the LCDΦ input to the backplane output. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD drivingwaveforms have a frequency 2^8 slower than the oscillator itself. The relationship is shown graphically (see Figure 2). The frequency is nearly independent of supply voltage. If LCDΦ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCDΦ be as large as is practical.
8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when the clock is falling, and (2) changing Load when the clock is falling.
9. The number of a segment corresponds to how many pulses have occurred since its data was present at the input. For example, the data on SEG 17 was input 17 clock pulses earlier.
10. It is acceptable to tie the load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, clock and Data In.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} ..... -0.3V to +12V
Inputs (CLK, Data In, Load) ..... V_{CC} to V_{DD} +0.3V
LCDΦ Input ..... -0.3V to V_{DD} +0.3V
Power Dissipation 250mW
Storage Temperature ..... -65°C to +125°C
Operating Temperature Industrial ..... -40°C to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

V_{DD} = +5V unless otherwise noted
T_A = -40°C to +85°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	+3.0	-	+10.5	V	
Supply Current	I_{DD}	-	25	60	µA	LCDΦ OSC < 15 kHz
		-	13	30	µA	LCDΦ OSC < 100Hz
Input High Level	V_{IH}	0.5V_{DD}	-	V_{DD}	V	
Input Low Level Clock,	V_{IL1}	0	-	+0.6	V	V_{DD} = +3.0V
Data,	V_{IL2}	0	-	+1.0	V	V_{DD} = +10.5V
Input Leakage Current Load	I_L	-	0.01	±10	µA	V_{IN} = 0V and +5.0V
Input Capacitance	C_I	-	-	5.0	pF	V_{DD} = +5.0V
Segment Output Voltage	V_{OH}	0.8V_{DD}	-	V_{DD}	V	I_{OH} = -100µA
	V_{OL}	0	-	0.1V_{DD}	V	I_{OL} = 100µA
LCDΦ Input High Level	V_{IN}	0.9V_{DD}	-	V_{DD}	V	
LCDΦ Input Low Level	V_{IL}	0	-	0.1V_{DD}	V	
LCDΦ Input Leakage Current Level	I_L	-	-	10	µA	V_{IN} = 0V and +5.0V V_{DD} = +5.0V

AC CHARACTERISTICS

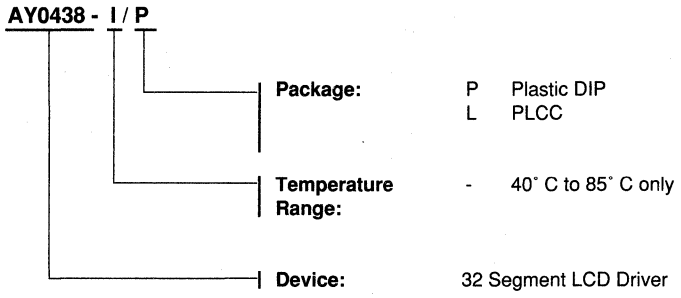
Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Rate	f	DC	-	1.5	MHz	50% duty cycle
Data Set-up Time	t_{ds}	150	-	-	nsec	Data change to Clk falling edge
Data Hold Time	t_{dh}	50	-	-	nsec	
Load Pulse Width	t_{pw}	175	-	-	nsec	
Data Out Prop. Delay	t_{pd}	-	-	500	nsec	C_L = 55pF

5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



SECTION 6
DIGITAL SIGNAL PROCESSING PRODUCT SPECIFICATIONS

6

DSP Product Portfolio

COMMERCIAL DSP (0° TO 70°)

CMOS DSP - COMMERCIAL (0° TO 70°)				
Microchip Part Number	**Speed (MHz) / TI Part Number**	**Maximum Instruction Cycle Time (ns)**	**Internal Mask ROM Version Available**	**Package**
DSP320C10-32/P	15.0 to 32.8	122	X	40L Plastic DIP
DSP320C10-32/L	15.0 to 32.8	122	X	44L PLCC
DSP320C10-25/P	15.0 to 25.6/ TMS320C10NL-25	156	X	40L Plastic DIP
DSP320C10-25/L	15.0 to 25.6/ TMS320C10FNL-25	156	X	44L PLCC
DSP320C10/P	6.7 to 20.5/ TMS320C10NL	195	X	40L Plastic DIP
DSP320C10/L	6.7 to 20.5/ TMS320C10FNL	195	X	44L PLCC
DSP320C10-14/P	6.7 to 14.4/ TMS320C10NL-14	277	X	40L Plastic DIP
DSP320C10-14/L	6.7 to 14.4	277	X	44L PLCC

INDUSTRIAL DSP (-45° TO +85°C)

CMOS DSP - INDUSTRIAL (-45° TO +85°C)				
Microchip Part Number	**Speed (MHz) / TI Part Number**	**Maximum Instruction Cycle Time (ns)**	**Internal Mas ROM Version Available**	**Package**
DSP320C10-32I/P	15.0 to 32.8	122	X	40L Plastic DIP
DSP320C10-32I/L	15.0 to 32.8	122	X	44L PLCC
DSP320C10-25I/P	15.0 to 25.6/ TMS320C10NA-25	156	X	40L Plastic DIP
DSP320C10-25I/L	15.0 to 25.6/ TMS320C10FNA-25	156	X	44L PLCC
DSP320C10I/P	6.7 to 20.5/ TMS320C10NA	195	X	40L Plastic DIP
DSP320C10I/L	6.7 to 20.5/ TMS320C10FNA	195	X	44L PLCC

MILITARY DSP (-55° TO +110°C)

Please refer to the "MILITARY DATA BOOK"

CMOS DSP - MILITARY (-55° TO +125°C)

Microchip	DESC SMD Part Number	Speed (MHz) Part Number Number	Maximum TI Part Cycle Time (ns)	Package Instruction	Lead Finish	Internal Masked ROM Version
DSP320C10-B/QA	5962-8763301QA	6.7 to 20.5 SMJ320C10JDM	195	40L Ceramic Side-Braze	Solder	-
DSP320C10-B/QC	5692-8763301QC	6.7 to 20.5	195	40L Ceramic Side-Braze	Gold	-
DSP320C10-B/UA	5962-8763301XA	6.7 to 20.5 SMJ320C10FDM	195	44 Terminal LCC	Solder	-
DSP320C10-B/UC	5692-8763301XC	6.7 to 20.5	195	44 Terminal LCC	Gold	-
DSP320C10-25B/QA	5962-8763302QA	15.0 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320C10-25B/QC	5962-8763302QC	15.0 to 25.6	156	40L Ceramic Side-Braze	Gold	-
DSP320C10-25B/UA	5692-8763302XA	15.0 to 25.6	156	44 Terminal LCC	Solder	-
DSP320C10-25B/UC	5962-8763302XC	15.0 to 25.6	156	44 Terminal LCC	Gold	-
DSP320CF10-25B/QA	5962-8763305QA	6.7 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320CF10-25B/QC	5962-8763305QC	6.7 to 25.6	156	40L Ceramic Side-Braze	Gold	-
DSP320CF10-25B/UA	5962-8763305XA	6.7 to 25.6	156	44 Terminal LCC	Solder	-
DSP320CF10-25B/UC	5962-8763305XC	6.7 to 25.6	156	44 Terminal LCC	Gold	-
DSP320CM10-B/QA	5962-8763303QA X	6.7 to 20.5	195	40L Ceramic Side-Braze	Solder	-
DSP320CM10-B/QC	5962-8763303QC	6.7 to 20.5	195	40L Ceramic Side-Braze	Gold	X
DSP320CM10-B/UA	5962-8763303XA X	6.7 to 20.5	195	44 Terminal LCC	Solder	-
DSP320CM10-B/UC	5962-8763303XC	6.7 to 20.5	195	44 Terminal LCC	Gold	X
DSP320CM10-25B/QA	5962-8763304QA X	15.0 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320CM10-25B/QC	5962-8763304QC	15.0 to 25.6	156	40L Ceramic Side-Braze	Gold	X
DSP320CM10-25B/UA	5962-8763304XA X	15.0 to 25.6	156	44 Terminal LCC	Solder	-
DSP320CM10-25B/UC	5962-8763304XC	15.0 to 25.6	156	44 Terminal LCC	Gold	X

MILITARY DSP (-55° TO +110°C) (CONT.)

NMOS DSP - MILITARY (-55° TO +110°C)

Microchip Part Number	DESC SMD Part Number	Speed (MHz) TI Part Number	Maximum Instruction Cycle Time (ns)	Package	Lead Finish
DSP32010-B/QA	5962-8405301QA	6.7 to 20.0	200	40L Ceramic Side-Braze	Solder
DSP32010-B/QC	5692-8405301QC	6.7 to 20.0	200	40L Ceramic Side-Braze	Gold
DSP32010-B/UA	5962-8405301ZA	6.7 to 20.0	200	44 Terminal LCC	Solder
DSP32010-B/UC	5692-8405301ZX	6.7 to 20.0	200	44 Terminal LCC	Gold

PART NUMBERS - MILITARY (see next page for Commercial and Industrial Parts)

DSP320x10 - 32 I / Q A

Lead Finish:		A	Solder Dip
		C	Gold
Case Outline:		Q	44 Pin Side Braze DIL
		U	40 Terminal LCC
Screening Level*:		B	MIL-STD-883C Compliant (-55° C to 125° C)
Frequency:		-	20.5 MHz
		25	25.6 MHz
Device:	DSP32010		NMOS DSP
	DSP320C10		CMOS DSP
	DSP320CF10		CMOS DSP, 6.7 to 25.6 MHz
	DSP320C10		CMOS DSP, ROM Version

***Note:** 32010 = TE (Thermally Enhanced LCC); 320C10 = NTE (Non-Thermally Enhanced LCC)

PART NUMBERS - DESC SMD

5xx2 87633 30x Q A

Lead Finish:	A	Solder Dip
	C	Gold
Case Outline*:	X	Ceramic Dual-in-line (28 lead)
	Q	Ceramic Side Braze DIL(40 lead)
	Z	Flat pack
Version:	301	6.7 to 20.5 MHz
	302	15.0 to 25.6 MHz
	303	6.7 to 20.5 MHz, ROM Version
	304	15.0 to 25.6 MHz, ROM Version
	305	6.7 to 25.6 MHz
Device:	5962	CMOS DSP
	5692	NMOS DSP

***Note:** The Case Outline Code is used for order entry only and will not be marked on device

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NOTES:

DSP320C10

CMOS Digital Signal Processor

FEATURES

- 122ns instruction cycle
- 144 word on-chip data RAM
- ROM-less version — DSP320C10
- 1.5K word on-chip program ROM—DSP320CM10
- External memory expansion to a total of 4K words at full speed
- 16-bit instruction/data word
- 32-bit ALU/Accumulator
- 16 x 16-bit multiply in 122ns
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 16-bit bidirectional data bus with a 65Mbps transfer rate
- Interrupt with a full context save
- Signed two's complement fixed-point arithmetic
- CMOS technology
- Single 5 volt supply
- Four versions available:

—DSP320C10-14	14.4MHz Clock
—DSP320C10	20.5MHz Clock
—DSP320C10-25	25.6MHz Clock
—DSP320C10-32	32.8MHz Clock

DESCRIPTION

The DSP320C10 is the first low power CMOS member of the Microchip Technology DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor.

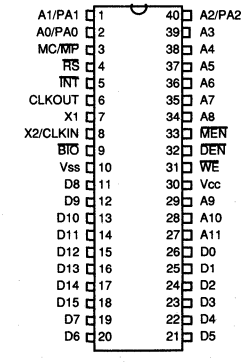
The processor has been enhanced to make the Data RAM static with respect to the Reset. Also, the address hold time has been improved to a non-negative value.

This 16/32 bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor thereby offering an inexpensive alternative to multichip bit-slice processors. The DSP320 family contains MOS microcomputers capable of executing eight million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DSP) algorithms.

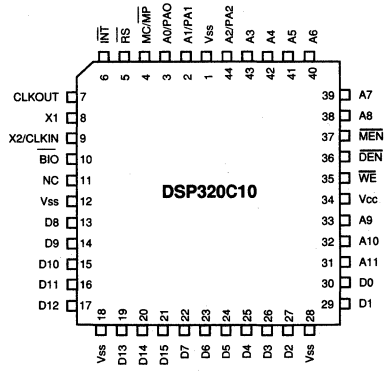
The DSP320 family's unique versatility and power give the design engineer solutions to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the DSP320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.

PIN CONFIGURATION
Top View

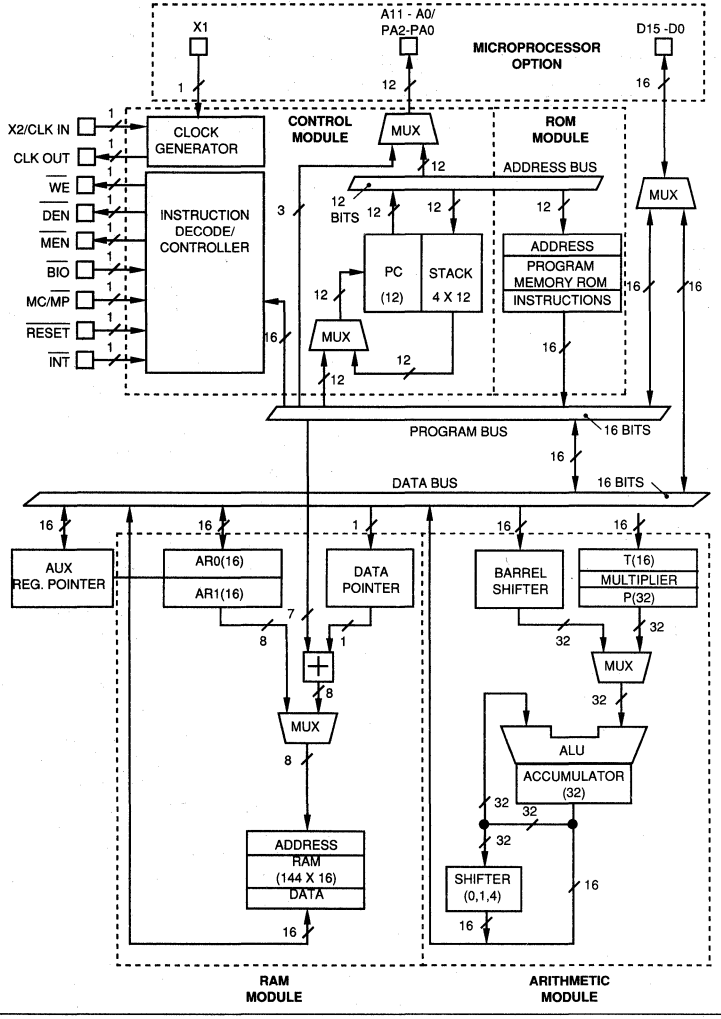
40 LEAD DIP



44 PIN PLCC



DSP320C10 BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	I/O	Definition	Name	I/O	Definition
A11-A0/ PA2-PA0	OUT	External address bus. I/O port address multiplexed over PA2-PA0.	MC/$\overline{MP}$	IN	Memory mode select: High selects microcomputer, low selects microprocessor mode.
$\overline{BIO}$	IN	External polling input for bit test and jump operations.	$\overline{MEN}$	OUT	Memory enable indicates that D15-D0 will accept external memory instruction.
CLKOUT	OUT	System clock output, 1/4 crystal CLKIN frequency.	$\overline{RS}$	IN	Reset used to initialize device.
D15-D0	I/O	16-bit data bus.	VCC	IN	Power.
DEN	OUT	Data enable indicates the processor accepting input data on D15-D0.	VSS	IN	Ground.
$\overline{INT}$	IN	Interrupt.	$\overline{WE}$	OUT	Write enable indicates valid data on D15-DO.
			X1	IN	Crystal input.
			X2/CLKIN	IN	Crystal input or external clock input.

ARCHITECTURE

The DSP320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The DSP320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

The DSP320C10 utilizes hardware to implement functions that other processors typically perform in software. For example, this device contains a hardware multiplier to perform a multiplication in a single 122ns cycle. There is also a hardware barrel shifter for shifting data on its way into the ALU. Finally, extra hardware has been included so that auxiliary registers, which provide indirect data RAM addresses, can be configured in an auto increment/decrement mode for single-cycle manipulation of data tables. This hardware-intensive approach gives the design engineer the type of power previously unavailable on a single chip.

32-bit ALU/Accumulator

The DSP320C10 contains a 32-bit ALU and accumulator that support double-precision arithmetic. The ALU operates on 16-bit words taken from the data RAM or derived from immediate instructions. Besides the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

Shifters

A barrel shifter is available for left-shifting data 0 to 15 places before it is loaded into, subtracted from, or added to the accumulator. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's complement arithmetic A second shifter left-shifts the upper half of the accumulator 0, 1, or 4 places while it is being stored in the data RAM. Both shifters are very useful for scaling and bit extraction.

16 x 16-bit Parallel Multiplier

The DSP320C10's multiplier performs a 16 x 16-bit, two's complement multiplication in one 122ns instruction cycle. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit result. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the DSP320C10 to perform such fundamental operations as convolution, correlation, and filtering at a very high rate.

Program Memory Expansion

The DSP320C10 is equipped with a 1536-word ROM which can be mask-programmed at the factory with a customer's program. It can also execute from an additional 2560 words of off-chip program memory at full speed. This memory expansion capability is especially useful for those situations where a customer has a number of different applications that share the same subroutines. In this case, the common subroutines can be stored on-chip while the application specific code is stored off-chip.

The DSP 320C10 can operate in either of the following memory modes via the MC/$\overline{MP}$ pin:

Microcomputer Mode (MC)—Instruction addresses 0-1535 fetched from on-chip ROM. Those with addresses 1536-4095 fetched from off-chip memory at full speed.

Microprocessor Mode ($\overline{MP}$)—Full speed execution from all 4096 off-chip instruction addresses.

The ability of the DSP320C10 to execute at full speed from off-chip memory provides important benefits:

- Easier prototyping and development work than is possible with a device that can address only on-chip ROM
- Purchase of a standard off-the-shelf product rather than a semi-custom mask-programmed device
- Ease of updating code
- Execution from external RAM
- Downloading of code from another microprocessor
- Use of off-chip RAM to expand data storage capability

Input/Output

The DSP320C10's 16-bit parallel data bus can be utilized to perform I/O functions at burst rates of 65 million bits per second. Available for interfacing to peripheral devices are 128 input and 128 output bits consisting of eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. In addition, a polling input for bit test and jump operations (BIO) and an interrupt pin ($\overline{INT}$) have been incorporated for multi-tasking.

Interrupts and Subroutines

The DSP320C10 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the DSP320C10's complete context. The instructions, PUSH stack from accumulator, and POP stack to accumulator permit a level of nesting restricted only by the amount of available RAM. The interrupts used in the DSP320C10 are maskable.

INSTRUCTION SET

The DSP320C10's comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general purpose operations, such as high-speed control. The instruction set, explained in Tables 1 and 2, consists primarily of single-cycle single-word instructions, permitting execution rates of up to eight million instructions per second. Only infrequently used branch and I/O instructions are multicycle.

The DSP320C10 also contains a number of instructions that shift data as part of an arithmetic operation. These all execute in a single cycle and are very useful for scaling data in parallel with other operations.

Three main addressing modes are available with the DSP320C10 instruction set: direct, indirect, and immediate addressing.

Direct Addressing

In direct addressing, seven bits of the instruction word concatenated with the data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words and the second page contains 16 words. In a typical application, infrequently accessed variables, such as those used for servicing an interrupt, are stored on the second page. The instruction format for direct addressing is shown below.

15 14 13 12 11 10 9 8	7	6 5 4 3 2 1 0
OPCODE	0	DMA

Bit 7 = 0 defines direct addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain data memory address.

The seven bits of the data memory address (DMA) field can directly address up to 128 words (1 page) of data memory. Use of the data memory page pointer is required to address the full 144 words of data memory.

Direct addressing can be used with all instructions requiring data operands except for the immediate operand instructions.

Indirect Addressing

Indirect addressing forms the data memory from the least significant eight bits of one of two auxiliary registers, AR0 and AR1. The auxiliary register pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. The instruction format for indirect addressing is as follows:

15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
OPCODE	1	0	INC	DEC	NAR	0	0	ARP

Bit7 = 1 defines indirect addressing mode. The opcode is contained in bits 15 through 8. Bits 7 through 0 contain indirect addressing control bits.

Bit 3 and bit 0 control the Auxiliary Register Pointer (ARP). If bit 3 = 0, then the content of bit 0 is loaded into the ARP. If bit 3 = 1, then content of ARP remain unchanged. ARP = 0 defines the contents of AR0 as memory address. ARP = 1 defines the contents of AR1 as memory address.

Bit 5 and bit 4 control the auxiliary registers. If bit 5 = 1, then the ARP defines which auxiliary register is to be incremented by 1. If bit 4 = 1, then the ARP defines which auxiliary register is to be decremented by 1. If bit 5 or bit 4 are zero, then neither auxiliary register is incremented or decremented. Bits 6, 2 and 1 are reserved and should always be programmed to zero.

Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

Immediate Addressing

The DSP320C10 instruction set contains special "immediate" instructions. These instructions derive data from part of the instruction word rather than from the data RAM. Some very useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

INSTRUCTION SET SUMMARY

TABLE 1 - INSTRUCTION SYMBOLS

Symbol	Meaning
ACC	Accumulator
D	Data memory address field
I	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

TABLE 2 - ACCUMULATOR INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0
ADD	Add to accumulator with shift	1	1	0	0	0	0	←		S	→	I	←			D			→
ADDH	Add to high-order accumulator bits	1	1	0	1	1	0	0	0	0	0	I	←			D			→
ADDS	Add to accumulator with no sign extension	1	1	0	1	1	0	0	0	0	1	I	←			D			→
AND	AND with accumulator	1	1	0	1	1	1	1	0	0	1	I	←			D			→
LAC	Load accumulator with shift	1	1	0	0	1	0	←		S	→	I	←			D			→
LACK	Load accumulator immediate	1	1	0	1	1	1	1	1	1	0	←				K			→
OR	OR with accumulator	1	1	0	1	1	1	1	0	1	0	I	←			D			→
SACH	Store high-order accumulator bits with shift	1	1	0	1	0	1	1	←	X	→	I	←			D			→
SACL	Store low-order accumulator bits	1	1	0	1	0	1	0	0	0	0	I	←			D			→
SUB	Subtract from accumulator with shift	1	1	0	0	0	1	←		S	→	I	←			D			→
SUBC	Conditional subtract (for divide)	1	1	0	1	1	0	0	1	0	0	I	←			D			→
SUBH	Subtract from high-order	1	1	0	1	1	0	0	0	1	0	I	←			D			→
SUBS	Subtract from accumulator with no sign extension	1	1	0	1	1	0	0	0	1	1	I	←			D			→
XOR	Exclusive OR with accumulator	1	1	0	1	1	1	1	0	0	0	I	←			D			→
ZAC	Zero accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1
ZALH	Zero accumulator and load high-order bits	1	1	0	1	1	0	0	1	0	1	I	←			D			→
ZALS	Zero accumulator and load low-order bits with no sign extension	1	1	0	1	1	0	0	1	1	0	I	←			D			→

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INSTRUCTION SET SUMMARY (CONT.)

TABLE 2 (CONT.) - AUXILIARY REGISTER AND DATA PAGE POINTER INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAR	Load auxiliary register	1	1	0	0	1	1	1	0	0	R	I	←			D			→
LARK	Load auxiliary register immediate	1	1	0	1	1	1	0	0	0	R	←				K			→
LARP	Load auxiliary register pointer immediate	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	K
LDP	Load data memory page pointer	1	1	0	1	1	0	1	1	1	1	I	←			D			→
LDPK	Load data memory page pointer immediate	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	K
MAR	Modify auxiliary register and pointer	1	1	0	1	1	0	1	0	0	0	I	←			D			→
SAR	Store auxiliary register	1	1	0	0	1	1	0	0	0	R	I	←			D			→

TABLE 2 (CONT.) - BRANCH INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	2	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BANZ	Branch on auxiliary register not zero	2	2	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BGEZ	Branch if accumulator ≥ 0	2	2	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BGZ	Branch if accumulator > 0	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BIOZ	Branch on $\overline{BIO}$ = 0	2	2	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BLEZ	Branch if accumulator ≤ 0	2	2	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BLZ	Branch if accumulator < 0	2	2	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BNZ	Branch if accumulator ≠ 0	2	2	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BV	Branch on overflow	2	2	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
BZ	Branch if accumulator = 0	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
CALA	Call subroutine from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
CALL	Call subroutine immediately	2	2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS							→	
RET	Return from subroutine or interrupt routine	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1

INSTRUCTION SET SUMMARY (CONT.)

TABLE 2 (CONT.) - T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APAC	Add P register to accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
LT	Load T register	1	1	0	1	1	0	1	0	1	0	I	←			D			→
LTA	LTA combines LT and APAC into one instruction	1	1	0	1	1	0	1	1	0	0	I	←			D			→
LTD	LTD combines LT, APAC, and DMOV into one instruction	1	1	0	1	1	0	1	0	1	1	I	←			D			→
MPY	Multiply with T register, store product in P register	1	1	0	1	1	0	1	1	0	1	I	←			D			→
MPYK	Multiply T register with immediate operand; store product in P register	1	1	1	0	0	←						K						→
PAC	Load accumulator from P register	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0
SPAC	Subtract P register from accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0

TABLE 2 (CONT.) - CONTROL INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DINT	Disable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0
LST	Load status register	1	1	0	1	1	1	1	0	1	1	I	←			D			→
NOP	No operation	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
POP	POP stack to accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1
PUSH	PUSH stack from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	0
ROVM	Reset overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1
SOVM	Set overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1
SST	Store status register	1	1	0	1	1	1	1	1	0	0	I	←			D			→

TABLE 2 (CONT.) - I/O AND DATA MEMORY OPERATIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMOV	Copy contents of data memory	1	1	0	1	1	0	1	0	0	1	I	←			D			→
IN	Input data from port	2	1	0	1	0	0	0	←	PA	→	I	←			D			→
OUT	Output data to port	2	1	0	1	0	0	1	←	PA	→	I	←			D			→
TBLR	Table read from program memory to data RAM	3	1	0	1	1	0	0	1	1	1	I	←			D			→
TBLW	Table write from data RAM to program (external only)	3	1	0	1	1	1	1	1	0	1	I	←			D			→

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Over specified temperature range (unless otherwise noted)**

Supply voltage, V_{CC} ..... -0.3V to 7V
All input voltages ..... -0.3V to 7V
Output voltage ..... -0.3V to 7V

Continuous power dissipation:

DSP320C10 (0° to +70°C) 0.3W
DSP320C10I (-40° to +85°C) 0.36W
DSP320C10-25 (0° to +70°C) 0.35W
DSP320C10I-25 (-40° to +85°C) 0.4W

Air temperature range above operating device:

– Commercial ..... 0° C to 70° C
– Industrial ..... -40° C to 85° C

Storage Temperature Range ..... -55° C to 150° C
Junction Temperature (TJ) ..... 165° C

**Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

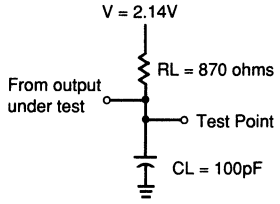
DC CHARACTERISTICS

*V_{CC} = 5V, TA = 25° C

Characteristics	DSP320C10			DSP320C10-14			DSP320C10-25			DSP320C10-32			Unit	Conditions
	Min	Nom*	Max	Min	Nom*	Max	Min	Nom*	Max	Min	Nom*	Max		
Supply voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V	
Supply voltage, V_{SS}	—	0	—	—	0	—	—	0	—	—	0	—	V	
High-level input voltage, V_{IH}														
- All inputs except CLKIN	2.0	—	—	2.0	—	—	2.0	—	—	2.0	—	—	V	
- CLKIN	.65Vcc	—	—	.65Vcc	—	—	.65Vcc	—	—	.65Vcc	—	—	V	
Low-level input voltage, V_{IL} (all inputs)	—	—	0.8	—	—	0.8	—	—	0.8	—	—	0.8	V	
High-level output voltage V_{OH}	Vcc-.4	—	—	Vcc-.4	—	—	Vcc-.4	—	—	Vcc-.4	—	—	V	I_{OH} = 20µA
	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	I_{OH} = 300µA
Low-level output voltage, V_{OL}	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	I_{OL} = 2mA
Off-state output current, I_{OZ}	—	—	20	—	—	20	—	—	20	—	—	20	µA	V_{CC} = 5.5V
	—	—	-20	—	—	-20	—	—	-20	—	—	-20	µA	V_O = V_{CC} - .4V
Input current, I_I	—	—	±50	—	—	±50	—	—	±50	—	—	±50	µA	
Supply current, I_{CC} (tested w/clocks running & part in reset)	—	—	50	—	—	50	—	—	55	—	—	65	mA	V_{CC} = 5.5V
Input capacitance, C_I														f = 1MHz, all other pins 0V
- Data bus	—	25	—	—	25	—	—	25	—	—	25	—	pF	
- All others	—	15	—	—	15	—	—	15	—	—	15	—	pF	
Output capacitance, C_O														
- Data bus	—	25	—	—	25	—	—	25	—	—	25	—	pF	
- All others	—	10	—	—	10	—	—	10	—	—	10	—	pF	

PARAMETER MEASUREMENT INFORMATION

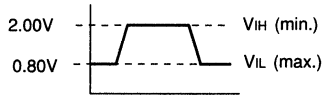
FIGURE 2 - TEST LOAD CIRCUIT



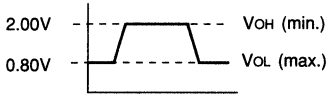
TTL Load Condition

FIGURE 3 - AC TIMING VOLTAGE REFERENCE LEVELS

a. Inputs, TTL compatible



b. Outputs, TTL compatible



6

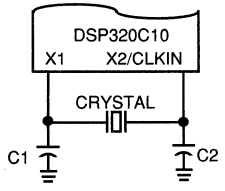
CLOCK

The DSP320C10 can use either its internal oscillator or an external frequency source for a clock.

INTERNAL CLOCK OPTION

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (See Figure 1) . The frequency of CLKOUT is one-fourth the crystal fundamental frequency.

FIGURE 1 - INTERNAL CLOCK OPTION



The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

EXTERNAL CLOCK OPTION

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected.

The external frequency injected must conform to the specifications listed in the table below.

CLOCK FREQUENCIES

Characteristics	Sym	Min	Nom	Max	Unit	Temperature Range Conditions
DSP320C10 Crystal frequency	fx	6.7	—	20.5	MHz	I, C
DSP320C10-14 Crystal frequency	fx	6.7	—	14.4	MHz	I, C
DSP320C10-25 Crystal frequency	fx	6.7	—	25.6	MHz	I, C
DSP320C10-32 Crystal frequency	fx	6.7	—	32.8	MHz	I, C
C1,C2		—	10	—	pf	I, C

CLOCK (CONT.)

CLOCK AC CHARACTERISTICS

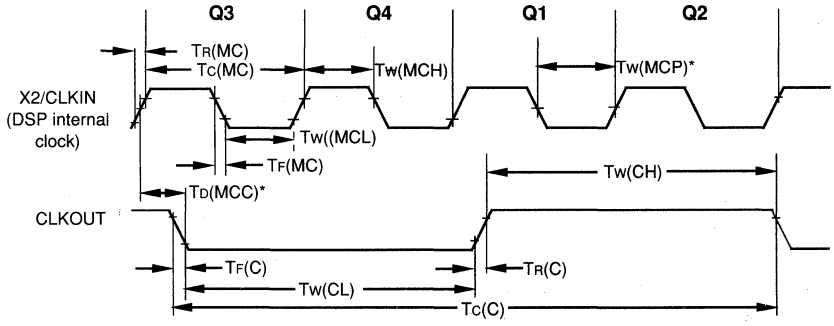
Timing requirements/Switching Characteristics over Recommended Operating Conditions

T_A (Commercial) = 0° to 70° C
T_A (Industrial) = -40° to 85° C
V_{CC} = 5V + 10%, V_{SS} = 0V

		DSP320C10			DSP320C10-14			DSP320C10-25			DSP320C10-32				
Characteristics	**Sym**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Unit**	**Conditions**
Master clk cycle time	$T_{C(MC)}$	48.78	—	150	69.50	—	150	39	—	150	30.5	—	150	ns	Note 1
Rise time mast. clk in.	$T_{R(MC)}$	—	5	10*	—	5	10*	—	4	8*	—	3	6*	ns	
Fall time mast. clk in.	$T_{F(MC)}$	—	5	10*	—	5	10*	—	4	8*	—	3	6*	ns	
Pulse dur. mast. clk low, $T_{C(MC)}$ = 70ns	$T_{W(MCL)}$	14*	20	—	14*	20	—	12*	16	—	8*	12	—	ns	
Pulse dur. mast clk high, $T_{C(MC)}$ = 70ns	$T_{W(MCH)}$	14*	20	—	14*	20	—	12*	16	—	8*	12	—	ns	
Pulse dur. mast clk	$T_{W(MCP)}$	0.4$T_{C(C)}$*	—	0.6$T_{C(C)}$*	0.4$T_{C(C)}$*	—	0.6$T_{C(C)}$*	0.45$T_{C(C)}$*	—	0.55$T_{C(C)}$*	0.45$T_{C(C)}$*	—	0.55$T_{C(C)}$*	ns	
CLKOUT cycle time	$T_{C(C)}$	195.12	—	—	277.80	—	—	156	—	—	122	—	—	ns	
CLKOUT rise time	$T_{R(C)}$	—	10	—	—	10	—	—	10	—	—	4	—	ns	
CLKOUT fall time	$T_{F(C)}$	—	8	—	—	8	—	—	8	—	—	7	—	ns	
Pls. dur., CLKOUT low	$T_{W(CL)}$	—	92	—	—	131	—	—	74	—	—	57	—	ns	See Fig 2
Pls. dur., CLKOUT high	$T_{W(CH)}$	—	90	—	—	129	—	—	72	—	—	54	—	ns	
Delay time to CLKIN↑ to CLKOUT↓ (Note 2)	$T_{D(MCC)}$	10	—	60	10	—	60	10	—	50	10	—	50	ns	

Note: (1) TC(C) is the cycle time of CLKOUT. i.e., 4*TC(MC) (4 times CLKIN cycle time if an external oscillator is used)
(2) **These values were derived from characterization data and are not tested or guaranteed.*

CLOCK TIMING



* TD(MCC) and TW(MCP) are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

MEMORY AND PERIPHERAL INTERFACE TIMING

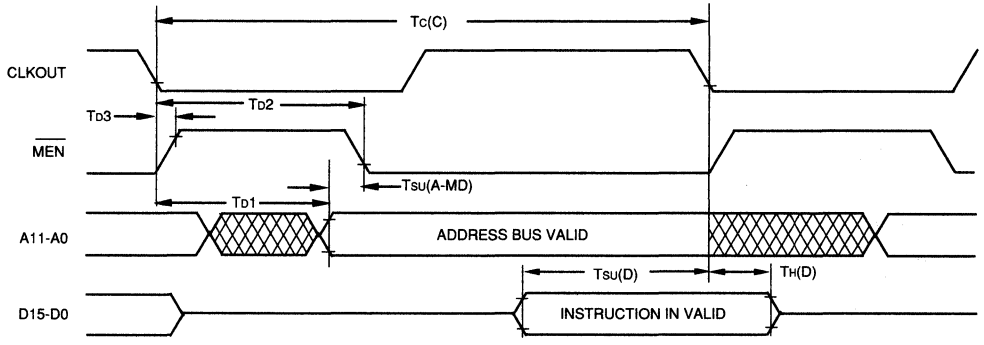
MEMORY AND PERIPHERAL INTERFACE - AC CHARACTERISTICS
Over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Delay time CLKOUT↓ to address bus valid (see note)	Td1	10*	—	38	ns	See Figure 2
Delay time CLKOUT↓ to $\overline{MEN}$↓	Td2	1/4Tc(C) -5*	—	1/4Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{MEN}$↑	Td3	-8*	—	12	ns	
Delay time CLKOUT↓ to $\overline{DEN}$↓	Td4	1/4Tc(C) -5*	—	1/4Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{DEN}$↑	Td5	-8*	—	12	ns	
Delay time CLKOUT↓ to $\overline{WE}$↓	Td6	1/2Tc(C) -5*	—	1/2Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{WE}$↑	Td7	-8*	—	12	ns	
Delay time CLKOUT↓ to data bus OUT valid	Td8	—	—	1/4Tc(C) +40	ns	
Time after CLKOUT↓ that data bus starts to be driven	Td9	1/4Tc(C) - 5*	—	—	ns	
Time after CLKOUT↓ that data bus stops being driven	Td10	—	—	1/4Tc(C) +30*	ns	
Data bus OUT valid after CLKOUT↓	Tv	1/4Tc(C) - 10	—	—	ns	
Delay time $\overline{DEN}$↑, $\overline{MEN}$↑ and $\overline{WE}$↑ from $\overline{RS}$↓	Td11	–	—	Tc(C) + 50*	ns	
Setup time data bus valid prior to CLKOUT↓	Tsu(D)	38	—	—	ns	
Hold time data bus held valid after CLKOUT↓	Th(D)	0	—	—	ns	
Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓	Tsu (A-MD)	1/4Tc(C) -35	—	—	ns	
Address bus hold after $\overline{WE}$↑, $\overline{MEN}$↑ or $\overline{DEN}$↑	Th(A-WMD)	5	—	—	ns	
Address bus setup time prior to $\overline{WE}$↓	Tsu(A-WE)	1/2Tc(C) -34	—	—	ns	
Data bus setup time prior to $\overline{WE}$↓	Tsu(D-WE)	1/4Tc(C) -32	—	—	ns	
Data bus hold after $\overline{WE}$↑	Th(D-WE)	1/4Tc(C) -18	—	—	ns	
External memory access time	Tacc	—	—	Tc(C) - 69	ns	
External memory output enable time	Toe	—	—	3/4 Tc(C) - 40	ns	

*These values were derived from characterization data and are not tested.
Note: 1. Address bus will be valid upon $\overline{WE}$↑, $\overline{DEN}$↑, or $\overline{MEN}$↑.
2. Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓

MEMORY AND PERIPHERAL INTERFACE TIMING (CONT.)

MEMORY READ TIMING DIAGRAM

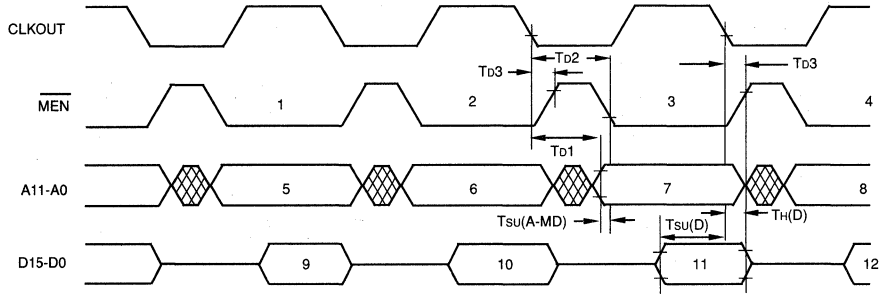


Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

INSTRUCTION TIMING DIAGRAMS (CONT.)

TBLR INSTRUCTION TIMING DIAGRAM

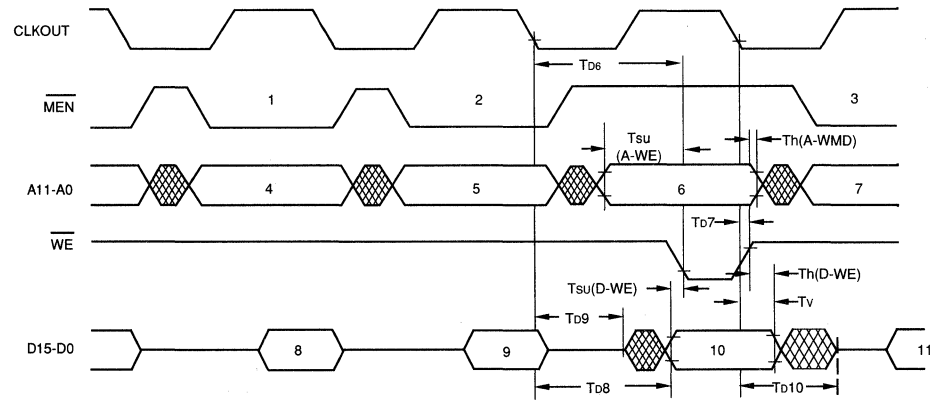


Legend:

1. TBLR INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. DATA FETCH
4. NEXT INSTRUCTION PREFETCH
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. ADDRESS BUS VALID
9. INSTRUCTION IN VALID
10. INSTRUCTION IN VALID
11. DATA IN VALID
12. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

TBLW INSTRUCTION TIMING DIAGRAM



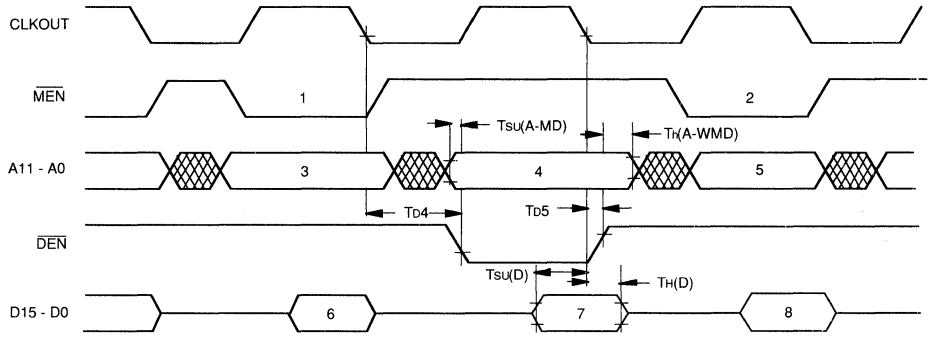
Legend:

1. TBLW INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. NEXT INSTRUCTION PREFETCH
4. ADDRESS BUS VALID
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. INSTRUCTION IN VALID
9. INSTRUCTION IN VALID
10. DATA OUT VALID
11. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

INSTRUCTION TIMING DIAGRAMS (CONT.)

IN INSTRUCTION TIMING DIAGRAM

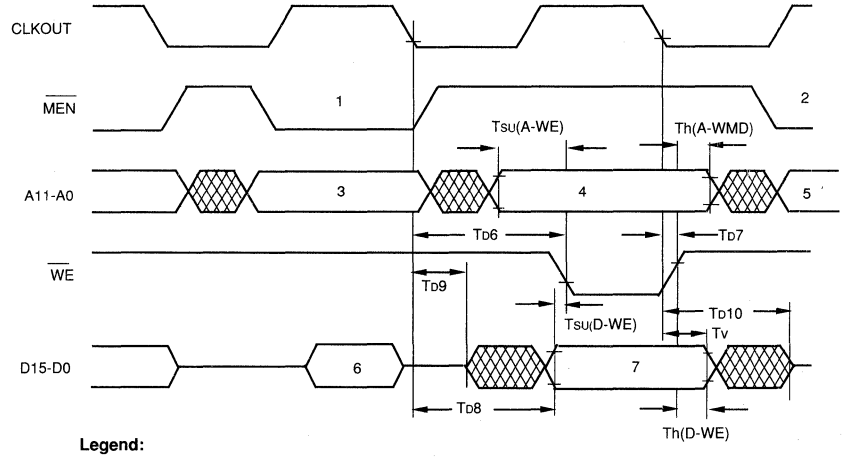


Legend:

1. IN INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA IN VALID
8. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

OUT INSTRUCTION TIMING DIAGRAM



Legend:

1. OUT INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA OUT VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

RESET (RS) TIMING

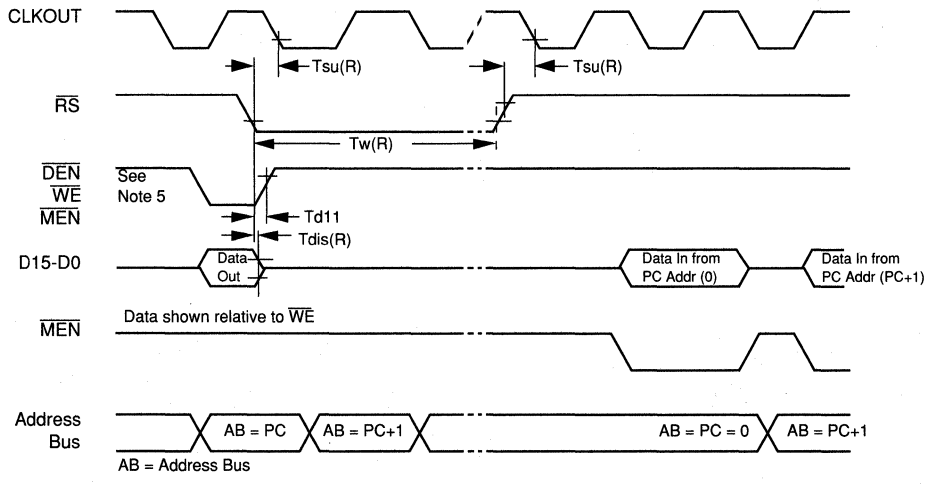
RESET TIMING AC CHARACTERISTICS

Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Reset ($\overline{RS}$) setup time prior to CLKOUT. See notes 1-4. DSP320C10-32	$T_{su}(R)$	38	—	—	ns	See Figure 2
$\overline{RS}$ pulse duration	$T_w(R)$	$5T_c(C)$	—	—	ns	
Delay time $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}\downarrow$	Td11	—	—	$T_c(C) + 50^*$	ns	
Data bus disable time after $\overline{RS}$	$T_{dis}(R)$	—	—	$3/4T_c(C) + 120^*$	ns	

Note: RS can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.
*These values were derived from characterization data and are not tested.

FIGURE 4 - RESET TIMING



Notes:

1. $\overline{RS}$ forces $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ high and tristates data bus DO through D15. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\downarrow$.
2. $\overline{RS}$ must be maintained for a minimum of five clock cycles.
3. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.
4. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.
5. Diagram shown is for definition purpose only. $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ are mutually exclusive.
6. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
7. During a write cycle, $\overline{RS}$ may produce an invalid write address.

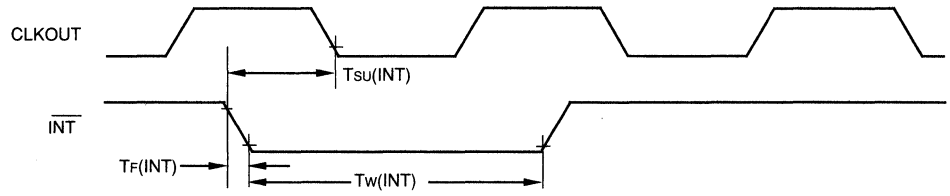
INTERRUPT (INT) TIMING

INTERRUPT TIMING AC CHARACTERISTICS

Timing requirements over recommended operating conditions * These values are not tested

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Fall time $\overline{INT}$	$T_f(INT)$	—	—	15*	ns	
Pulse duration $\overline{INT}$	$T_w(INT)$	$T_c(C)$	—	—	ns	
Setup time $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	$T_{su}(INT)$	38	—	—	ns	

INTERRUPT TIMING DIAGRAM



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

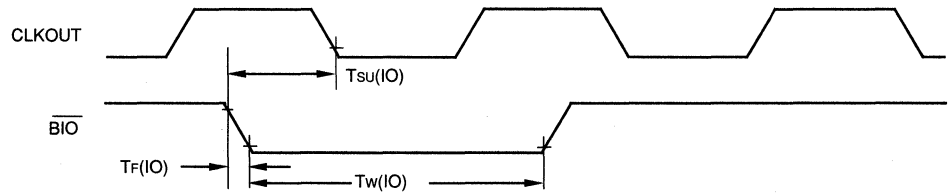
I/O (BIO) TIMING

I/O (BIO) AC CHARACTERISTICS

Timing requirements over recommended operating conditions * These values are not tested

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Fall time $\overline{BIO}$	$T_f(IO)$	—	—	15*	ns	
Pulse duration $\overline{BIO}$	$T_w(IO)$	$T_c(C)$	—	—	ns	
Setup time $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	$T_{su}(IO)$	38	—	—	ns	

I/O (BIO) TIMING DIAGRAM



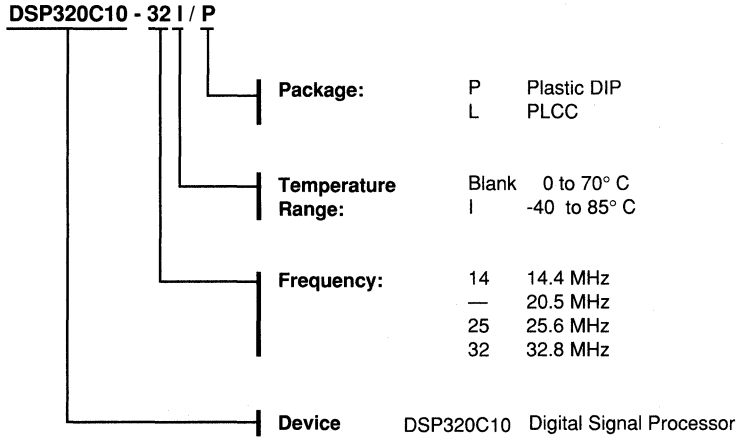
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



DSP320C10 DIGITAL SIGNAL PROCESSOR SUPPORT TOOLS

Introduction

The following information relates to the support tools available for Microchip's DSP320C10 Digital Signal Processor. A brief description of each tool is provided along with the availability and prices. A part number is assigned for each product and this number should be used when ordering.

For more information, please contact your local Microchip sales office. Microchip reserves the rights to change the specifications of each system without notice.

Systems & Tools

Hardware Tools:

Please contact your local sales office or factory for a list of third party support products. These include in-circuit emulators, EVM boards and other plug in modules.

Software Tools:

Product	Function
C10ASM	A cross assembler and linker with macro capabilities for DSP320C10. Various computer systems are supported.
C10SIM	A software instruction level simulator of DSP320C10. Available on various computer systems.

Please contact your local sales office or factory for a list of third party support products. These include assemblers/linkers, filter design packages and other DSP libraries.

C10ASM (ASSEMBLER/LINKER)

Description

This is a cross assembler which converts the source code to object code for Microchip's DSP320C10 series of 16-bit digital signal processors. A linker is also provided for combining separately assembled modules into one or more object modules. Multiple object code format is provided and supports formats required by all other Microchip's development systems. One of the output format is 8 bit Intel hex format. Under this format two separate files with high bytes in one and low bytes in another file are produced. This eases programming 8 bit wide EPROMs.

Functional Features

- Absolute and Relocatable addressing.
- Conditional assembly.
- Macro capability.
- External Symbol Reference.
- Multiple Object code formats.
- Combines separately assembled modules into one or more object modules.
- External Symbol resolution.
- ROM/RAM partitioning.
- Object code libraries and Multiple Object code formats.

Minimum Host Requirements :

- MS-DOS -- 512k RAM.
- VAX/VMS.

Part Number & Ordering Information

• C10ASM-DS	C10 Assembler/Linker for MS-DOS systems/IBM compatibles
• C10ASM-VS	C10 Assembler/Linker for DEC VAX/VMS

C10SIM (SIMULATOR)

Description

This is a software simulator simulating the DSP320C10 series. The simulator accepts any object code format generated by Microchip's cross assembler, and aids in debugging and testing microcode. Algorithms and software development can be executed without waiting for silicon and other hardware. Since the simulator is totally under software control, the user has a lot more control in execution of his code through complex breakpoints, trace, single stepping, viewing/modifying. Various signals, memory locations and registers can be viewed very easily. Signals can be injected or captured from/to files by redirecting the I/O port to files, and then be analyzed by other software.

Functional Features

- Instruction Boundary Simulation
- Three execution modes (execute until break condition, trace and single stepping).
- Flexible breakpoints : On Instruction acquisition, error conditions, data conditions and maskable memory read/write.
- Watch/modify registers and memory locations.
- 128 instruction trace buffer (can be output to a file).
- Continuous trace mode
- Symbolic debug and symbolic disassembler.
- File associated port I/O.
- Programmable interrupts.
- Friendly user interface that can constantly display registers and memory on screen.
- Input/Output Radix can be Hex, decimal or Octal.

Part Number & Ordering Information

- C10SIM-DS C10 Simulator for MS-DOS systems/IBM compatibles
- C10SIM-VS C10 Simulator for DEC VAX/VMS

6

NOTES:

Microchip

SECTION 7
QUALITY AND RELIABILITY

7

Microchip

Quality Without Compromise

A CORPORATE COMMITMENT

Raising the quality level of Microchip's products and services is a performance alliance built with customers and suppliers.

Total quality improvement and quality awareness is powered by company-wide participation.

Meeting a customer's expectations is where quality commitment begins. The resolve to continuously improve as a supplier never ends.

THE CHALLENGE OF COMPLEXITY

Integrating An Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down the President and CEO actively leads and audits programs to ensure continuous improvement is a perpetual process. Quality teams work from the bottom up to improve performance at every department level. Incorporating quality improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination To Be The Best

Through statistical management and the use of statistical tools, a framework is built for becoming a continuously improving supplier. The programs put in place are to become the foundation for success.

PROCESS TECHNOLOGY

EEPROM Technology

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a guaranteed endurance of $> 10^4$ which can be erased automatically and byte written in-situ in a system, all in 1 ms.

EPROM Technology

The CMOS EPROM technology produces a non-volatile memory cell by storing or removing charge from a self-aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region, and are removed by radiation from a high intensity UV source. This memory cell is guaranteed to have an endurance of >100. Programming is done off-line using an EPROM programmer and block erasing accomplished with a high intensity UV source through the package window.

SNOS Technology

Microchip's SNOS EEPROM technology produces a non-volatile memory cell which stores or removes charge from the nitrite/oxide interface by electron tunneling through a sub-5 nm oxide under the nitride. This cell is guaranteed to have an endurance $>10^4$. Individual bytes can be written in-situ in a system at 30 ms but due to layout design constraints, a circuit can only be block erased.

Microcontroller and Logic

Logic Products use an N-well CMOS technology. Depending on functionality and/or performance requirements, however, different variations of the CMOS process are used. These include ROM, EPROM or EEPROM and use of single or double level metallization. Two levels of polysilicon are used for EPROM, EEPROM or capacitors (in analog circuits).

Oxide spacers are used to obtain DDD (Double Diffused Drains) and titanium is used for polycide formation for low resistance poly lines. The process uses a 250 Å gate-oxide thickness and 550 Å interpoly oxide thickness. Boron and Phosphorous plugs are used for N-contacts and P-contacts to prevent junction spiking.

QUALITY

Design For Quality And Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Design committee members representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Documentation And Procurement Specifications

Microchip's positive documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These positive document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls And Process Assessment

Product integrity is assured by samplings and inspection plans performed in line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans follow MIL-STD-883C procedures where applicable.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is assured and data to guide continuous improvement is generated. (See Appendix A - Controls)

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B - Material Controls)

Testing For Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an out going quality assurance program, most products are tested at least two machine tolerances tighter than those specified by the customer. Margin testing accounts for normal tolerances of any particular test system and provides customers with the assurance that Microchip's products meet a customer's specifications.

Variation From Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Presently Microchip uses electrical screens to help eliminate short term failures. The long term program of total quality improvement emphasizes continuous improvement.

Individuals in all departments are encouraged to analyze the methods employed at their positions and formulate plans to improve performance. Because a customer could receive part of every mistake, definitive programs are continuously formulated at all working levels, designed to eliminate mistakes and contain error.

Outgoing Quality

Quality Control samples all outgoing product from Microchip final testing.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. Engineers labor under strict guidelines to ensure tests of sample lots are precise and reliable. Exacting internal specifications demand every product used to qualify a process endure an accelerated life test. EPROMs, EEPROMs, and Logic Products are stressed beyond normal use limits when undergoing high temperature reverse bias, operating life, and retention bake tests.

Package Qualification

Package qualification measures a component's ability to withstand thermal and mechanical shock, temperature cycles and moisture. Stresses applied to products exceed normal parts use. All products are stressed to high level military or industrial specifications to ensure reliability.

Ongoing Sampling Of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data gleaned from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for longer periods of circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The number of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods of failure rate statements are commonly used:

* Percent failures per thousand circuit-hours, (represented as ^), or
* Absolute failures per 10^9 circuit-hours, or Fits.

Note that a failure rate of 0.0001%/1000 hours and 1 Fit are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time To) and decreases as time goes on.

Time T1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T_1 and T_2. This long period of time is distinguished by a nearly constant and very low failure rate. After T2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate by higher environmental stress levels, the incidence of the failure modes encountered under normal conditions. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used is known as the Arrhenius Equation. It is as follows:

$$AF = e^x, \text{ Where: } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828....(non-dimensional constant)

E_A = Activation energy level (electron volts)

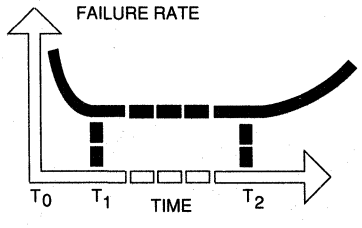
k = Boltzmann's constant = $8.6172754 * 10^{-5}$ (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T_1 under temperature T_N can be compressed by the amount T_1 divided by AF at the accelerated temperature T_A. Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

FIGURE 1: BATHTUB CURVE



Activation Energy Level

The dependent variable AF in the Arrhenius Equation is a function of several variables. T_N and T_A are specified for the situation under consideration. E_A is a function of the particular mode of failure, and can be viewed as the minimum energy required for a particular failure to occur.

Activation energy levels in semiconductors generally are in the 0.4 - 1.1 electron-volt range. Each failure mode that is accelerated has its own activation energy level. Some typical examples are:

FAILURE MECHANISM	E_A(eV)
Oxide/Dielectric Defects	0.3
Chemical, Galvanic, or Electrolytic Corrosion Silicon Defect	0.3
	0.5
Electromigration	0.5 to 0.7
Unknown	0.7
Broken Bonds	0.7
Lifted Die	0.7
Surface Related Contamination	1.0
Induced Shifts/ Lifted Bonds (Au-A1 Interface)	1.0
Charge Injection	1.3
Floating Gate Charge Loss	0.6
Hot Electron Trapping	-.06
Tunnel Dielectric Breakdown	0.13

A compromise value of 0.7 electron-volts is often used when there are no specific a prior facts relating to the failure modes being accelerated.

There is however, a continous reliability program at Microchip structured to validate E_A values in use and to categorize new failure mechanisms.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked like a typical application and outputs are loaded in the same way as a typical application. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 24, 168, 500 and 1,000 hours. Early hour failures are usually associated with test escapes, manufacturing defects or otherwise marginal material. Longer term failures are typically caused by metal migration, ionic contamination, and oxide breakdowns.

High Temperature Reverse Bias (HTRB)

Microchip employs the High Temperature Reverse Bias test on floating gate devices to accelerate any charge gain onto the floating gate due to oxide defects and to accelerate threshold shifts due to ionic contamination. The test is conducted by putting the device into a special test mode whereby 7.0 volts is applied to all poly 2 structures with all source, drain and substrate held at ground. The test is conducted at +150°C and is normally conducted for 1,000 hours with readouts at 24, 168, 500 and 1,000 hours.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate and SNOS devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a programmable device can be programmed and erased. Normally the test is conducted at worse case programming conditions and is followed by a retention bake.

Temperature Cycle

The Temperature Cycle test simulates systems that are subject to power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is normally 1,000 cycles for plastic and 100 cycles for ceramic packages. Endpoint criteria is both electrical and mechanical.

RELIABILITY TESTS (CONT.)

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid which simulates rapid environment changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C and the number of cycles are typically 15.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate to the die surface. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating gate devices usually happen before a corrosion mechanism develops.

Temperature Humidity Test

The Temperature Humidity test determines the survivability of devices in molded plastic packages functioning in a humid environment. By convention, test conditions are 85°C and 85% relative humidity. The parts are biased to lend themselves to electrochemical corrosion. The duration of the test is usually 1,000 hours or more. The test checks the adequacy of the die surface protection and the plastic's lack of ionic impurities. The applied bias may be 5 volts on alternating pins or set up for minimum power to reduce internal heating and consequent moisture evaporation on the device. Similar to the Autoclave test, charge loss on floating gate devices is a principle failure mechanism.

QUALIFICATION CATEGORIES

Qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Qualification applies to the following changes:

I. New technology

II. Start-up of Fab or Assembly

III. Transfer of fab or assembly to another location

IV. Major process changes:

- A. Process scaling (shrink conversion)
- B. Change in vendor or material source
- C. New equipment that affects reliability

V. New die configurations:

- A. New structures
- B. New packaging material
- C. Design rule changes
- D. Existing package revision (dimensional or layout)

QUALIFICATION PROGRAMS

Qualifications guarantee new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequency on each process family include:

A. 168 hour operating life - weekly

B. 1,000 hour operating life - annually

C. Endurance test - weekly

D. Data retention test - weekly

E. Temperature cycle - weekly

F. Temperature humidity - annually

G. Long term retention - annually

H. Mechanical tests - annually

APPENDIX A - IN-LINE CONTROLS

CONTROLS - PLASTIC PACKAGE ASSEMBLY

PROCESS STEP	REJECT PARAMETER LIMITS	SAMPLE PLAN	FUNCTION QC	FUNCTION PROD	MIL STD REP
Die Visual Inspection	Reject For Any Defect	100%		X	883C Method 2010 B
Wafer Saw	Report Failure Modes	1 Slice Per Lot Visual	X		883C Method 2010
Die Attach Inspection	Machine Shut Down	5/Shift Each Machine	X		883C Method 2019
Wire Bond Inspection	Report Failure Mode Machine Shut Down	1% AQL Each Half Shift	X		883C Method 2011 D 2010
Post Wire Bond Visual Inspect	Reject For Any Defect	100%		X	883C Method 2010
Mould Press Visual	Machine Shut Down	LTPD 15% A=0	X		X-Ray Monitor
Package Visual	Report Defects 100% Screen For Major Defects	LTPD 2% A=0	X		N/A
Trim & Form Visual	Report Defects 100% Screen For Major Defects	LTPD 2% A=0	X		883C Method 2016
External Final Visual Inspection - Run Ticket Verification - Marking Legibility - Package Outline Check - Solderability Monitor - Package Form	Major Defects 100% Screen	LTPD 2% A=0	X		883C Method 2009

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CONTROLS - CERAMIC PACKAGE ASSEMBLY

PROCESS STEP	REJECT PARAMETER	SAMPLE PLAN LIMITS	FUNCTION QC	FUNCTION PROD	MIL STD REP
Die Visual Inspection	Reject For Any Defect	100%		X	883C Method 2010 B
Wafer Saw Inspection	Machine Shut Down	1 Slice/ Lot Visual	X		883C Method 2010
Die Attach Inspection	Machine Shut Down	Non-destruct Each 2 hrs Destruct Each Shift	X		883C Method 2019
Wire Bond Inspection	Report Failure Mode Machine Shut Down	1% AQL Each Half Shift	X		883C Method 2011 D 2010
Preseal Visual Inspection	Reject For Any Defect	LTPD 15% A=0		X	883C Method 2010 B
Package Seal Inspection	Machine Shut Down	LTPD 15% A=0	X		883C Method 1014
Fine Leak Test	Screen 100%	LTPD 5% A=0	X		883C Method 1014
Gross Leak Test	Screen 100%	LTPD 5% A=0	X		883C Method 2014
Lead Trim Visual	Screen 100%	LTPD 2% A=0	X		883C Method 2016
Package Mark Inspection	Machine Shut Down	LTPD 10% A=1	X		883C Method 2015
Environmental Inspection	Machine Shut Dow	LTPD 5% A=0	X		883C Methods 1010C 2001E, 1014
External Package Visual	Screen 100%	LTPD 10% A=1	X		883C Method 2009

APPENDIX B - MATERIAL CONTROLS

MATERIAL CONTROLS - PLASTIC PACKAGE ASSEMBLY			
PROCESS STEP	**REJECT PARAMETER LIMITS**	**SAMPLE PLAN**	
Lead Frame Inspection	Reject For Any Failure	Visual Functional	LTPD 2% A=0 LTPD 10% A=0
Die Mount Epoxy Inspect	Functional Test-Reject Any Failure		3 Sample Runs
Gold Wire Inspection	Reject For Any Defect		2 Spools Per Lot A=0
Mould Compound Inspection	Storage Temp 5°C Pellet Weight ±5 GMS Functional Test Any Failure		3 Sample Runs

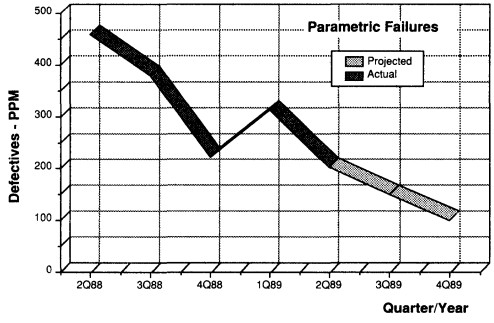
MATERIAL CONTROLS - CERAMIC PACKAGE ASSEMBLY

PROCESS STEP	REJECT PARAMETER LIMITS	SAMPLE PLAN		FUNCTION QC	FUNCTION PROD	MIL STD REP
Package Inspection - Mechanical Visual - Hermeticity - Plating Thickness - Bake Visual	Reject For Any Defect		LTPD % 10 A=0 15 A=0 10 A=0 15 A=0	X		N/A
Preform Inspection	Reject For Any Defect	Visual Functional	LTPD % 10 A=0 15 A=0	X		N/A
Bond Wire Inspection	Reject For Any Defect		2 Spools Per Lot A=0	X		N/A
Lid Inspection	Reject For Any Defect	Visual Functional	LTPD % 7 A=0 10 A=0	X		N/A

Plastic Package Reliability Bulletin

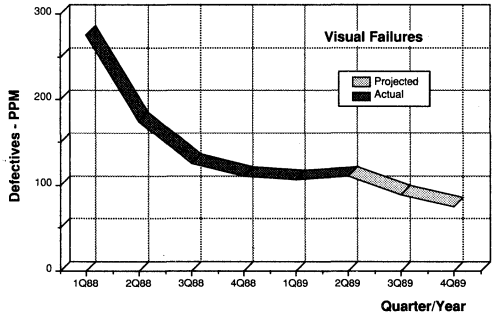
AVERAGE OUTGOING QUALITY OF PLASTIC EPROMS

Microchip Technology Inc.'s organized data on outgoing quality of plastic EPROMs tracks parametric failures such



as speed, power and device leakage. Its present level has reached 200 ppm after programming, with a goal of 100 ppm.

As plastic parts have extremely high impact resistance, visual/mechanical failure rate is expected to run half the expected failure rate of ceramic parts.



OVERVIEW

Microchip Technology Inc.'s Plastic EPROM products provide competitive leadership in quality and reliability, with demonstrated performance of less than 170 FITs (Failures in Time) operating life. The designed-in reliability of Microchip Technology Inc.'s Plastic EPROMs is supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip Technology Inc.'s quality and reliability system, and the EPROM product data demonstrate its results.

The customer's quality requirements are Microchip Technology Inc.'s top priority: Ongoing customer feedback and device performance monitoring drive Microchip Technology Inc.'s manufacturing and design process, leading to continuing improvements in the long-term quality and reliability of Microchip Technology Inc.'s products.

PRODUCT SCOPE

Subject of this Product Reliability Bulletin are the Plastic Packages of Microchip Technology Inc.'s EPROM Product Family:

27C64-XX/YY	64K (8Kx8) CMOS EPROM
27C128-XX/YY	128K (16Kx8) CMOS EPROM
27C256-XX/YY	256K (32Kx8) CMOS EPROM
27C512-XX/YY	512K (64Kx8) CMOS EPROM

These EPROMs are available in a range of access times designated by the XX parameter: 120, 150, 170, 200 and 250 ns. Available plastic packages are identified by the YY parameter: Plastic DIP, PLCC, and SOIC.

RELIABILITY DATA

Microchip Technology Inc.'s EPROMs in plastic were produced to offer the customer the flexibility of using the plastic device as a direct substitution for a Cerdip EPROM in one-time-programming applications. Failure Rate Predictions/Operating Life data for plastic EPROMs at 125°C proves to be equivalent to the data of ceramic EPROMs (refer to page 8), opening the way for package substitution for cost savings and inventory reduction.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology Inc. agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology Inc., an activation energy of 0.7 eV has been shown to be most representative of typical failures on operating life, while 0.6 eV is representative of charge gain or loss failures. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

EPROM products have an early failure rate (infant mortality) of less than 0.05% and thus, a production burn-in should not be necessary. For all products shown, the early and the intermediate failure rates are combined and expressed as a single failure rate.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball bond chip-out Cracked die or surface cracks Bond pad corrosion
Biased-Humidity/	Internal circuit corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss from EPROM cell
High Temp. Reverse Bias	Charge gain to EPROM cell Parameter drift/shift

DEFINITIONS

AOQ (Average Outgoing Quality): The amount of defective product in a population, usually expressed in terms of parts per million (PPM).

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Biased-Humidity: Moisture and bias are used to accelerate corrosion-type failures in plastic packages. The conditions include 85°C ambient temperature with 85% relative humidity. Typical bias voltage is +5 volts and ground on alternating pins.

Autoclave (pressure cooker): Using a pressure of one atmosphere above normal pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock: Consists of extreme temperature cycling of devices from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C Temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM.

High Temperature Reverse Bias (HTRB): A special test mode which subjects the entire EPROM array to a high voltage level and is used to measure charge gain and/or threshold shifts.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

DESIGN AND DEVELOPMENT → **QUALIFICATION** → **RELIABILITY CONTROL**

Specify:
- Design objectives/specifications
- Testability goals
- Reliability requirements
- Process/packaging requirements
- Design guidelines

Design:
- Functional models
- Logic design & verification
- Circuit design & verification
- Layout design & verification
- Prototype verification
- Performance characterization

Develop (as required):
- Wafer fabrication processes
- Package/packaging technology

Confirm design objectives using qualification tests:
- Operating life, 125°C ambient
- Temp-cycle, -65°/150°C
- Thermal shock, -65°/150°C
- ESD resistance, ± 2000 V
- Latch-up (CMOS devices)
- Biased-humidity, 85°C/85%
- Autoclave (pressure cooker) retention bake
- HTRB

Assure Outgoing Quality Level:
- Design release document
- Baseline wafer fabrication process
- Baseline assembly process
- Qualification release
- Enter device to specification system
- Wafer-level reliability controls
- Assembly reliability controls
- Early failure rate sampling
- Reliability monitoring
- Statistical process control feedback
- Audit specifications
- Analyze returned failures
- Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement, and new package types.

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Plastic EPROM Reliability Bulletin

RELIABILITY DATA SUMMARY

INTRODUCTION

This section provides a reliability summary of Microchip Technology Inc.'s plastic EPROMs. Included is plastic packaging information and reliability data obtained to date for the 27C64, 27C128, 27C256, and 27C512 EPROM plastic devices.

EPROMs have become a viable quick turn solution for providing new ROM pattern capability without the typical long turn around time associated with mask programmable ROMs. The speed capability of EPROMs has also improved, making them competitive with traditional ROM products.

With this capability, it is possible and practical for the customer to keep an inventory of blank EPROMs on hand and do custom programming on an as needed basis.

Units are also available from Microchip Technology Inc. utilizing the QTP (Quick Turn Product) approach. Microchip Technology Inc. will provide pre-programmed EPROM units to customers using the customers defined pattern. This approach eliminates the traditional delay time involved in processing a mask programmable ROM.

PLASTIC PACKAGE CHARACTERISTICS

Plastic packaging utilized for the EPROM products uses a silver filled epoxy adhesive for die attach. Bonding technology is gold wire thermosonic bonding. The lead frame pedestal and finger tips are silver plated. The epoxy molding compound used is a Shinitsu compound KMC-140-3 which meets the safety rating requirements of UL 94 VO 1/8 in/min. External lead finish is electroplated tin lead 90/10 percent. The package code table below lists the plastic packages covered by the reliability data in this document.

As part of an on going product improvement program, Microchip Technology Inc. will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques.

PLASTIC PACKAGE IDENTIFICATION CODES

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP

ELECTRICAL CHARACTERISTICS

Microchip Technology Inc.'s EPROMs packaged in plastic are tested to the same electrical characteristics as devices assembled in Cerdip packages. This testing covers the full commercial range of 0-70°C. Performance characteristics are the same as for Cerdip packaging with speeds to 120ns available.

QUALITY/RELIABILITY TESTING RESULTS

Reliability and programming tests were performed on EPROM devices in plastic packages. Data from these qualification tests are displayed throughout this document.

PROGRAMMABILITY

Programmability is measured by sample data taken from production lots. Devices are programmed with a Diagonal FF which exercises 98% of the EPROM cell array. This rigorous patterning combined with Microchip Technology Inc.'s FAST programming algorithm greatly enhances the ability to meet specific customer applications. Large volume beta site programming results for plastic EPROMs indicate an expected yield of 98.7% using Fast Mode programming under normal production conditions. This means customer programming, using a recommended Express programming algorithm, should be higher than 99% on the smaller EPROM arrays.

PROGRAMMABILITY DATA (12 months period)

Time Period	No. of Sample Units	No. of Non-Programmable Units	Fraction Defective
1989	10019	258	.026

Note: Derated to typical customer programming, the defective fraction should be 0.009

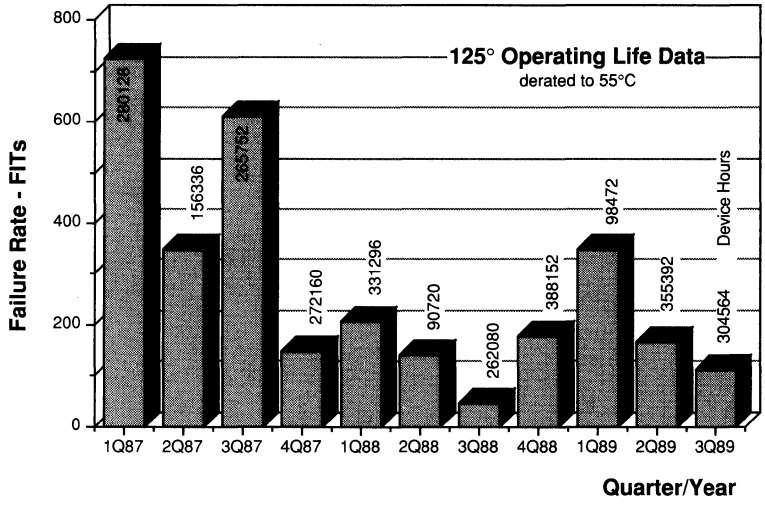
PACKAGE CODE

Package Code	SP	P	L	Gull Wing
Package Type	**300 Mil P Dip**	**600 Mil P Dip**	**J Lead PLCC**	**300 mil body SOIC**
Lead Count: 24	F	A		F
28		A	A	F
32		F	A	
40		F		
44			F	

(A) Available - (F) Future Release Planned

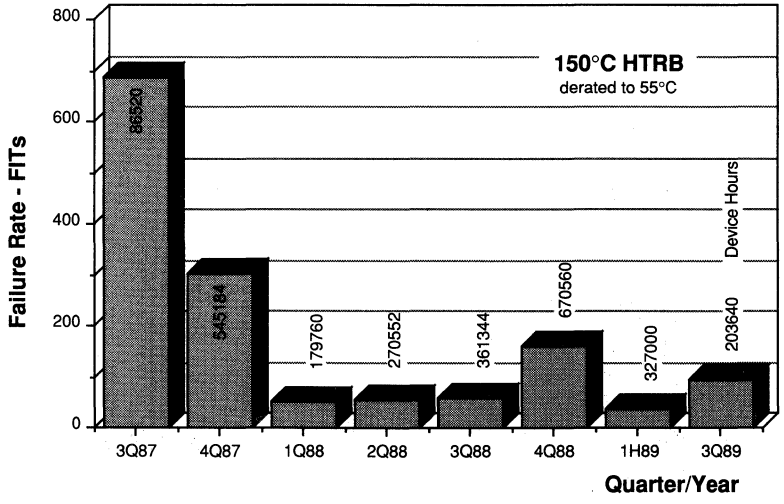
HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

High temperature dynamic life testing accelerates random failure modes which would occur in a users application. Voltage bias and address signals are used to exercise the device in a manner similar to the users system.



HIGH TEMPERATURE REVERSE BIAS (150°C/7 Volts)

Microchip Technology Inc.'s EPROMs are designed for enhanced reliability by having a special test mode which allows all gates on the array to be simultaneously placed at a high voltage stress level in reference to the rest of the circuitry. This test is used to create a high voltage stress on the memory oxide. An additional acceleration of three times is gained from the 7V level based on experimental data. This is calculated into the failure rates below. Failures which will be detected with this type of stress are: pin holes in the oxide, thin oxide layers, and charge gain failures.



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MOISTURE RESISTANCE TESTING

Moisture resistance evaluation of Microchip Technology Inc. plastic EPROMs includes both autoclave testing (121°C, 15 PSI) and temperature humidity testing (85°C/ 85% relative humidity with bias). Moisture resistance could not be obtained by the industry standard so a layered passivation utilizing an Oxy-Nitride film to provide a moisture block while allowing unblocked UV transmission is used.

The autoclave accelerates any moisture penetration through the plastic package material or around the metal leadframe and plastic to leadframe interface. The objective of this testing is to accelerate failure of the device as a result of any moisture contamination on the surface of the die. Failure mechanisms such as passivation defects (pinholes, cracking, lifting), corrosion of bondpads or surface metal through passivation defects, leakage and surface contamination as well as charge loss failures may be identified. The predominant failure mechanism for EPROMs is data loss.

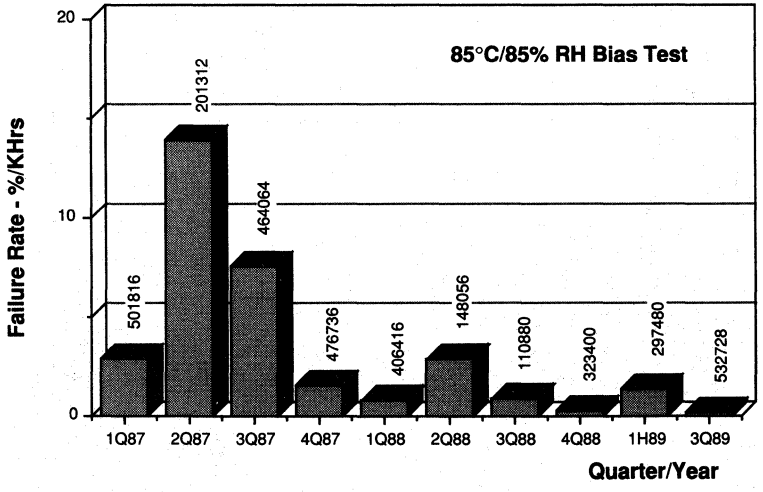
AUTOCLAVE (121°C/15 PSI)

Product	Failures/Sample Size		
	24 Hrs	96 Hrs	168Hrs
27C256/L	0/723	0/766	1/766[1]
27C64/P	1/767[1]	0/380	1/766[1]
27C128/P	0/380	1/444[1]	2/443[1]
27C256/P	0/444	1/450[1]	3/449[1]
27C512/P	0/450	3/723[1]	9/720[1]
27Cxxx/X (discounted for charge loss)	0/2764	0/2763	0/2758

[1] - Failures due to charge loss on EPROM cell

HUMIDITY BIAS - 85°C/85%RH

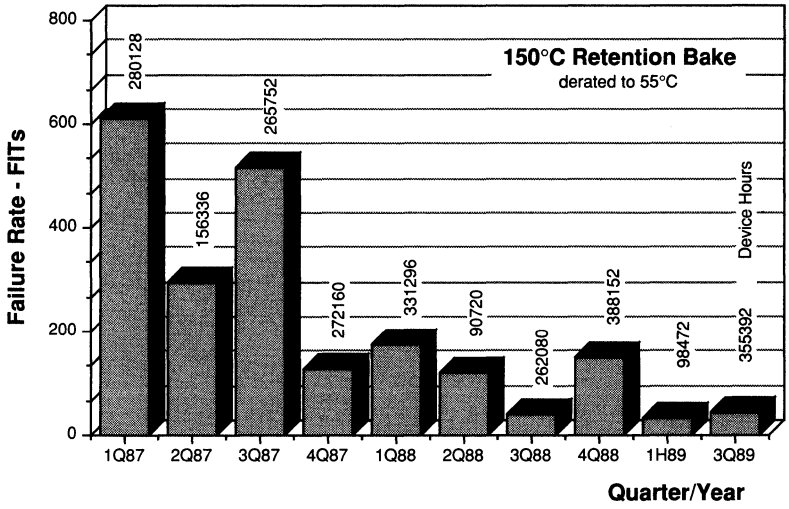
Temperature humidity testing is utilized to accelerate failures through electrolytic corrosion. This is accomplished by subjecting devices to a high temperature and high humidity atmosphere with bias applied to the device. The combination of moisture penetration through the plastic package and interaction of the moisture with any contaminates on the surface of the device and the applied voltage to the unit, will result in electrolytic corrosion and failure of the device.



DATA RETENTION BAKE

Data storage in EPROMs is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in loss of data. In order to detect this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell.

This added screen for detecting infant mortality charge loss allows Microchip Technology Inc.'s plastic product to duplicate the excellent data retention characteristics of the ceramic EPROM packages.



TEMPERATURE CYCLING (-65°C TO +150°C)

This stress is used to evaluate the mechanical integrity of the plastic package and the assembly process. Temperature cycling consists of cycling the devices between -65°C and +150°C at the rate of 4 cycles per hour. This stress will identify failure mechanisms such as plastic package cracking, die attach problems, and wire bonds lifting.

Product	Failures/ Sample Size	
	100 Cycles	500 Cycles
27C64/L	0/34	0/0
27C256/L	0/102	0/0
27C64/P	0/374	0/340
27C256/P	0/68	0/68

THERMAL SHOCK (-55°C TO + 125°C)

This stress is used to evaluate the mechanical integrity of the plastic package. It consists of rapid immersion of devices into liquids of -55°C and +125°C respectively.

Product	Failures/ Sample Size
	15 cycles
27C64/P	0/170
27C256/L	0/34
27C256/P	0/68

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PRODUCT RELIABILITY DATA

1988/89 FAILURE RATES AT 60% CONFIDENCE

Reliability Test	Product	Failures/Sample Size at 24 Hrs	168 Hrs	500 Hrs	1000 Hrs	FITs
125°C Operating Life	27C64	0/871	2/871	0/198	0/45	170
	27C128	3/393	1/390	0/216	0/172	301
	27C256	2/1243	2/1241	2/882	0/880	100
	27C512	4/954	1/949	0/948	0/948	85
150°C HTRB	27C64	1/749	1/748	2/154	0/0	84
	27C128	3/225	0/222	0/45	0/45	157
	27C256	1/902	3/901	1/586	0/585	27
	27C512	2/411	4/409	2/405	0/284	77
150°C Retention Bake	27C64	1/1074	0/1073	0/813	0/813	9
	27C128	0/1562	0/1562	0/1562	0/1562	4
	27C256	1/1670	2/1669	1/1509	0/1508	29
	27C512	2/477	2/475	0/397	0/397	108
Failure Modes	Operating Life: (5) Metal Migration, (10) Oxide Breakdown, (2) Poly Shorts HT Reverse Bias: (12) Oxide Breakdown, (8) Charge Gain Retention Bake: (9) Charge Loss					

SECTION 8
PACKAGING

Microchip

PACKAGING

Commercial/Industrial Outlines and Parameters

COMMERCIAL AND INDUSTRIAL PARTS

Part Number Suffix Designations:

XXXXXXXXXX - XX X / XX XXX

ROM Code or Special Requirements

Case Outline

P	= Plastic Dual In-Line
J	= Cerdip (with window if EPROM) - all product except Microcontrollers
D	= Ceramic Side Brazed Dual In-Line
L	= PLCC (Plastic Leaded Chip Carrier)
W	= Die in Wafer Form
S	= Die in Waffle Pack
K	= LCC (Ceramic Leadless Chip Carrier, not thermally enhanced)
SP	= Skinny Plastic Dual In-Line
SJ	= Skinny Cerdip
SN	= Small Outline Narrow Plastic Gull Wing (150 mil Body)
SM	= Small Outline Medium Plastic Gull Wing (207 mil Body)
SO	= Small Outline Wide Plastic Gull Wing (300 mil Body)
CB	= COB (Chip-On-Board)
IC	= IC Card
JW	= Cerdip, windowed - for Microcontrollers only

Process Temperature

Blank	= 0°C to +70°C
I	= -40°C to +85°C
H	= -40°C to +110°C
E	= -40°C to +125°C

Speed (EPROM / High Density EEPROM)	**Frequency** (DSP)	**Crystal Designation** (PIC)
-35 = 35 ns	Blank = 20.5 MHz	LP = 4 µs
-40 = 40 ns	-14 = 14.4 MHz	RC = 1 µs
-45 = 45 ns	-25 = 25.6 MHz	XT = 1 µs
-55 = 55 ns	-32 = 32.8 MHz	HS = 200 ns
-70 = 70 ns		
-90 = 90 ns		
-10 = 100 ns		
-12 = 120 ns		
-15 = 150 ns		
-17 = 170 ns		
-20 = 200 ns		
-25 = 250 ns		

Device Type (Up To 10 Digits)

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TABLE OF CONTENTS

SECTION 1: HERMETIC

A. Ceramic Side Brazed Dual In-line Package ("D" Case Outlines)

B. Ceramic Cerdip Dual In-iine Package ("J, JW, SJ" Case Outlines)

C. Ceramic Flatpack

D. Ceramic Leadless Chip Carrier (Surface Mount Package, "K" Case Outlines)

TABLE OF CONTENTS (Cont'd)

SECTION 2: PLASTIC

Packaging Diagrams and Parameters

Ceramic Side Brazed Dual In-line Family

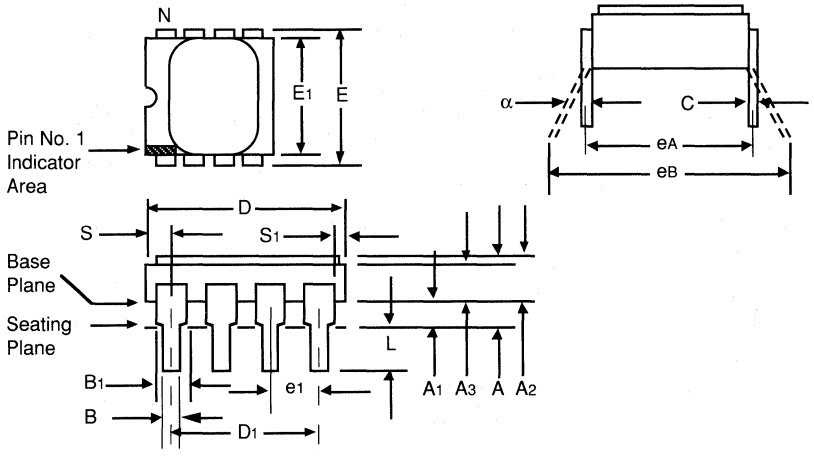
Symbol List for Ceramic Side Brazed Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

Packaging Diagrams and Parameters

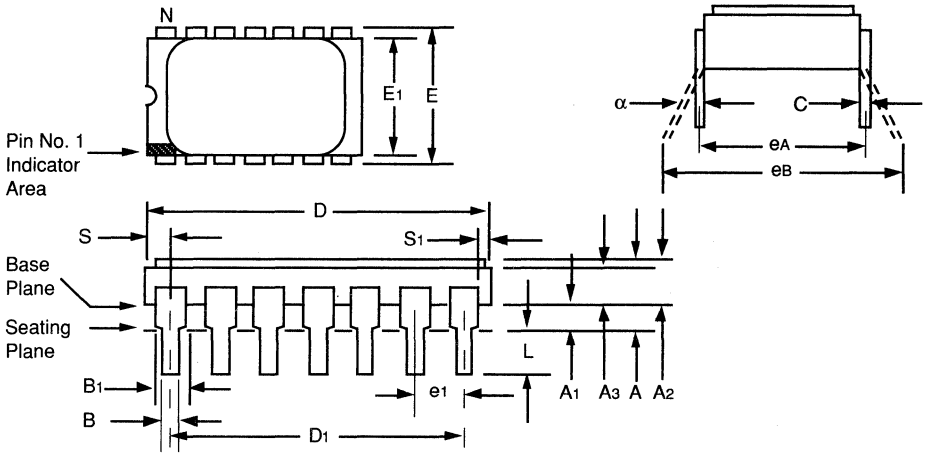
Package Type: 8-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	3.937		0.130	0.155	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	Typical	0.054	0.054	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	13.0048	13.4112		0.512	0.528	
D1	7.4168	7.8232	Reference	0.292	0.308	Reference
E	7.5692	8.2296		0.298	0.324	
E1	7.112	7.620		0.280	0.300	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.620	9.652		0.300	0.380	
L	3.302	3.810		0.130	.150	
N	8	8		8	8	
S	2.540	3.048		0.100	0.120	
S1	0.127	–		.005	–	

Packaging Diagrams and Parameters

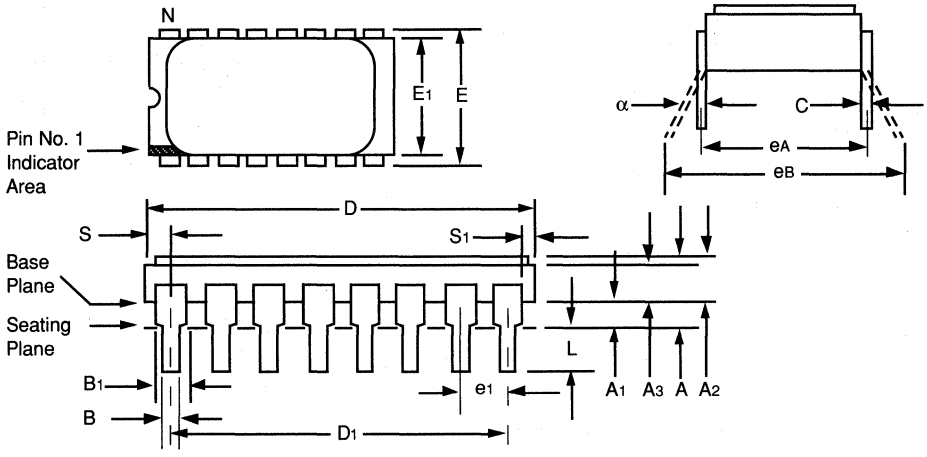
Package Type: 14-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.3048	**Typical**	0.008	0.012	**Typical**
D	18.796	19.2278		0.740	0.757	
D1	15.0368	15.4432	**Reference**	0.592	0.608	**Reference**
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.3622	2.7432	**Typical**	0.093	0.108	**Typical**
eA	7.366	7.874	**Reference**	0.290	0.310	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	14	14		14	14	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

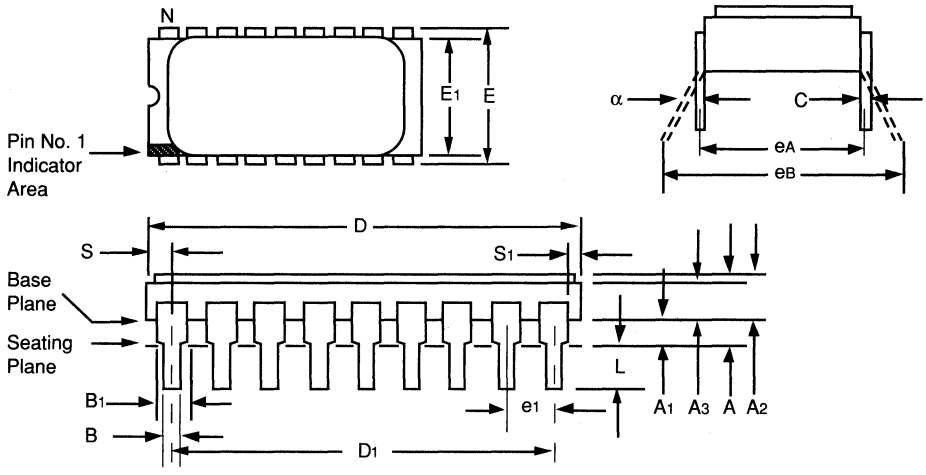
Package Type: 16-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	**Typical**	0.054	0.054	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	19.812	20.574		0.780	0.810	
D1	17.653	17.907	**Reference**	0.695	0.705	**Reference**
E	7.620	8.382		0.300	0.330	
E1	7.1628	7.4676		0.282	0.294	
e1	2.413	2.667	**Typical**	0.095	0.105	**Typical**
eA	7.366	7.874	**Reference**	0.290	0.310	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	16	16		16	16	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

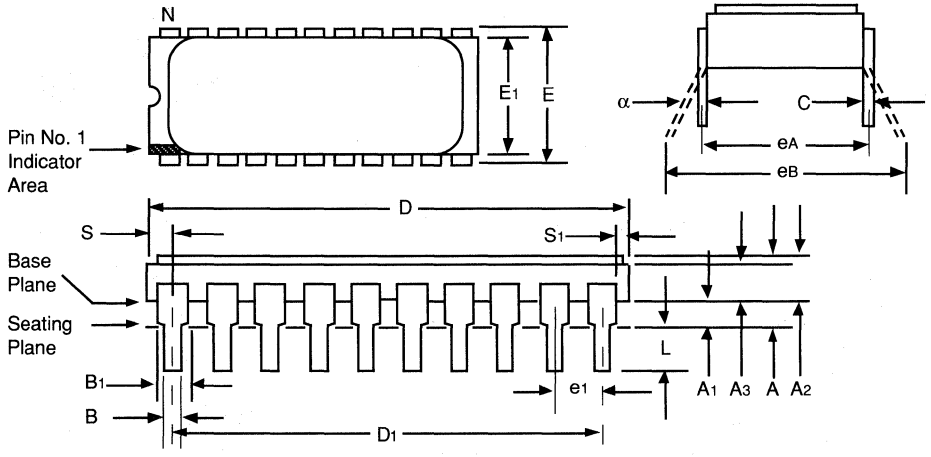
Package Type: 18-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	Typical	0.054	0.054	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	22.352	23.114		0.880	0.910	
D1	20.193	20.447	Reference	0.795	0.805	Reference
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.413	2.667	Typical	0.095	0.105	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	18	18		18	18	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

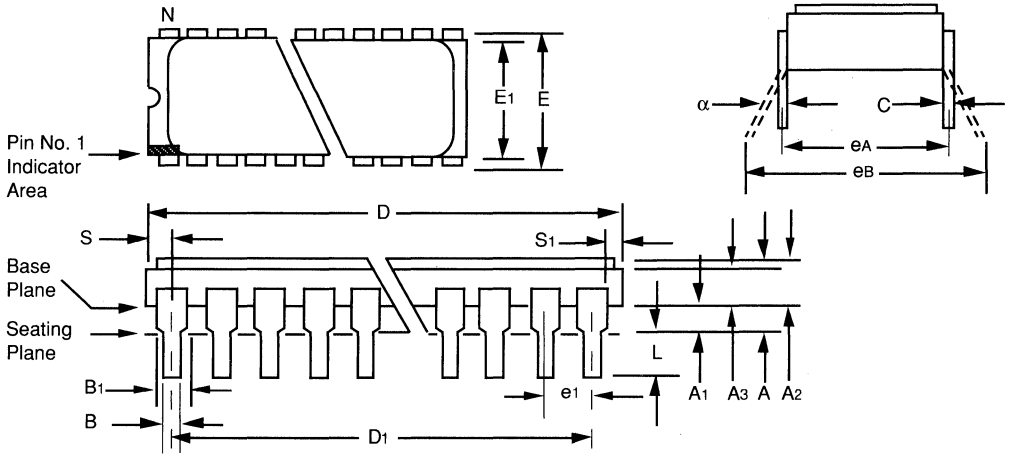
Package Type: 20-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	0.508		–	0.200	
A1	0.381	1.778		0.015	0.070	
A2	–	–		–	–	
A3	3.81	4.445		0.150	0.175	
B	0.355	0.584		0.014	0.023	
B1	1.27	1.27	**Typical**	0.050	0.050	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	23.876	24.892		0.940	0.980	
D1	22.86	22.86	**Reference**	0.900	0.900	**Reference**
E	7.62	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.54	2.54	**Typical**	0.100	0.100	**Typical**
eA	7.62	7.62	**Reference**	0.300	0.300	**Reference**
eB	7.62	10.16		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	20	20		20	20	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

Package Type: 22-Lead Ceramic Side Brazed Dual In-line (.400 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.667	4.064		0.105	0.160	
A1	0.7112	1.2192		0.028	0.048	
A2	2.032	3.302		0.080	0.130	
A3	1.778	2.921		0.070	0.115	
B	0.4318	0.5842		0.017	0.023	
B1	1.016	1.016	**Typical**	0.040	0.040	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	27.1526	27.8638		1.069	1.091	
D1	25.2968	25.6032	**Reference**	0.992	1.008	**Reference**
E	10.160	10.922		0.400	0.430	
E1	9.7282	9.9822		0.383	0.393	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	9.906	10.414	**Reference**	0.390	0.410	**Reference**
eB	10.160	12.192		0.400	0.480	
L	3.175	4.191		0.125	0.165	
N	22	22		22	22	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

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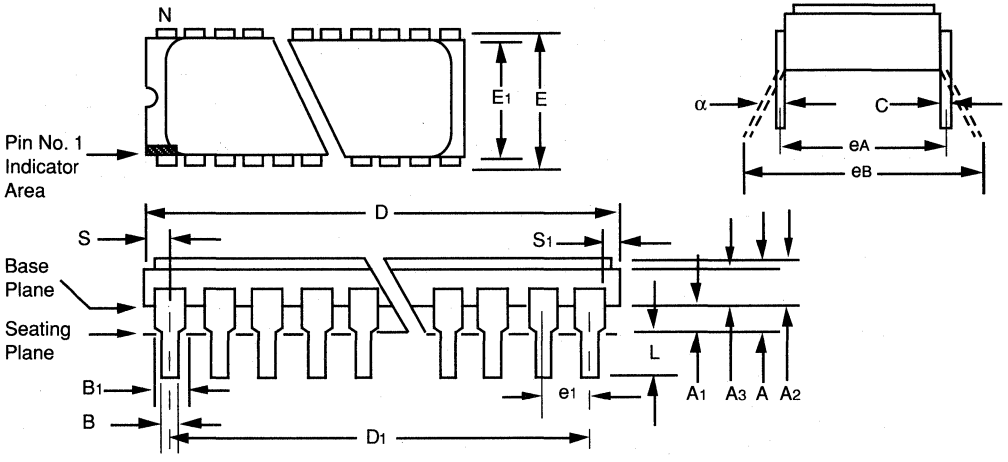
Packaging Diagrams and Parameters

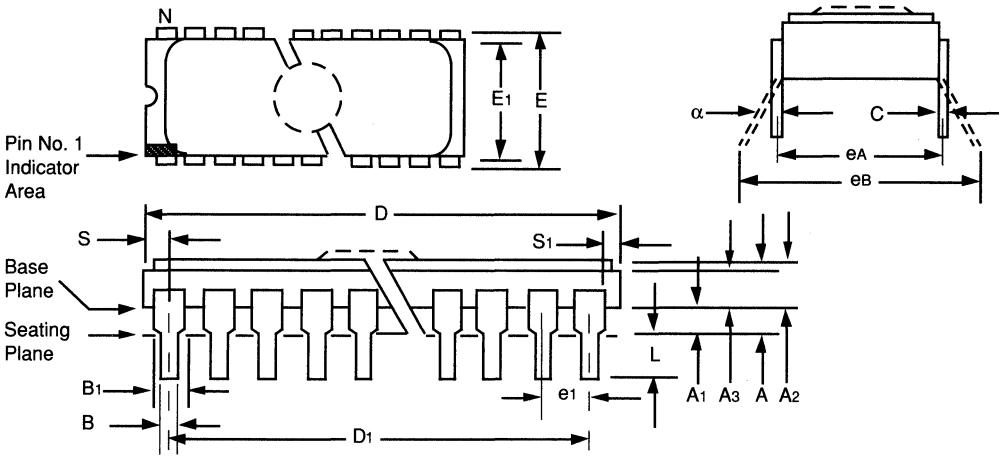
Package Type: 24-Lead Ceramic Side Brazed Dual In-line (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A_1	1.016	1.524		0.040	0.060	
A_2	2.032	2.921		0.080	0.115	
A_3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B_1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	30.1752	30.7848		1.188	1.212	
D_1	27.7368	28.1432	**Reference**	1.092	1.108	**Reference**
E	14.986	16.002		0.590	0.630	
E_1	14.7828	14.9352		0.582	0.588	
e_1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
e_A	14.986	15.748	**Reference**	0.590	0.620	**Reference**
e_B	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S_1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

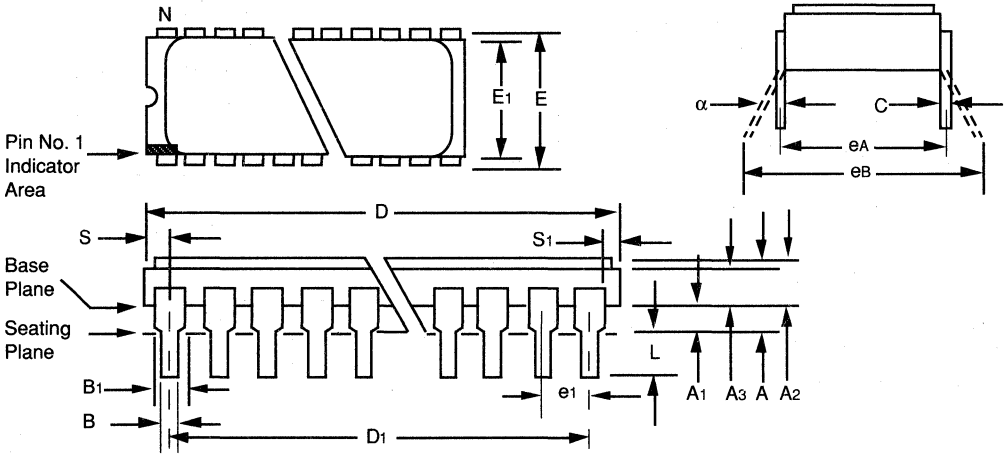
Package Type: 24-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	30.1752	30.7848		1.188	1.212	
D1	27.7368	28.1432	**Reference**	1.092	1.108	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	14.9352		0.582	0.588	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	14.986	15.748	**Reference**	0.590	0.620	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

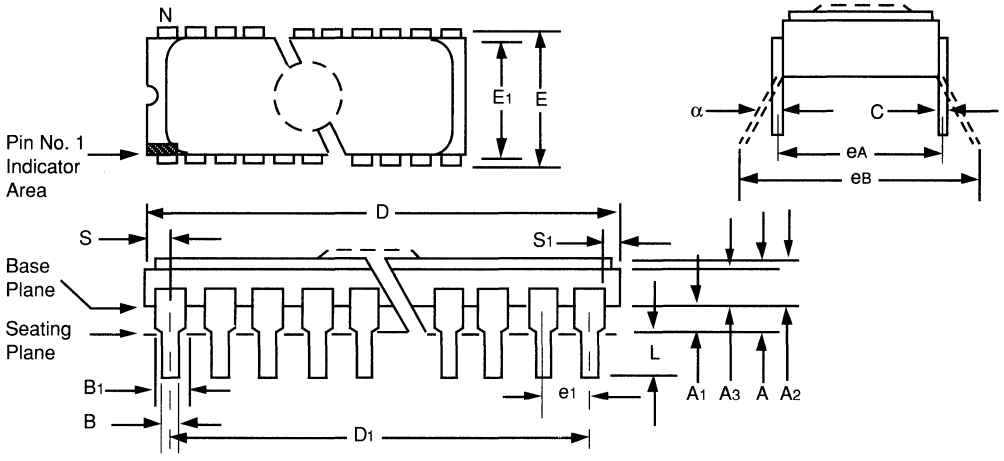
Package Type: 28-Lead Ceramic Side Brazed Dual In-line (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

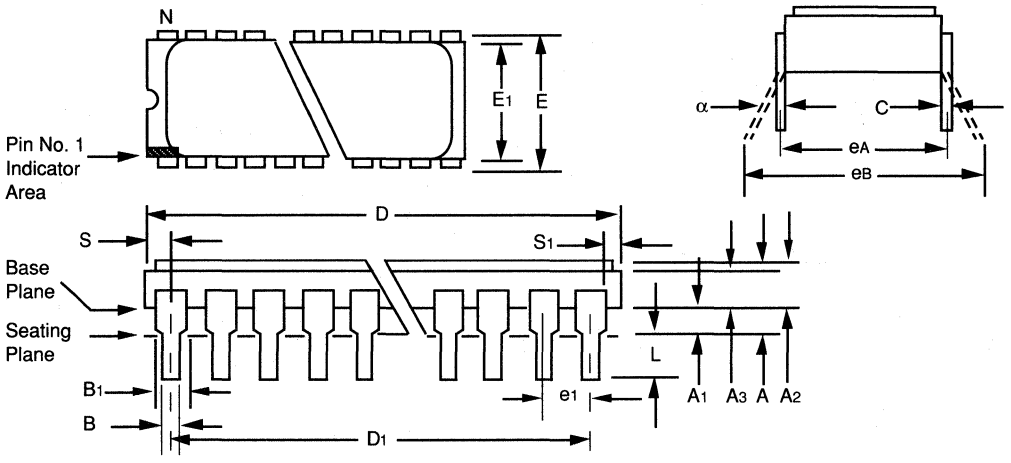
Package Type: 28-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

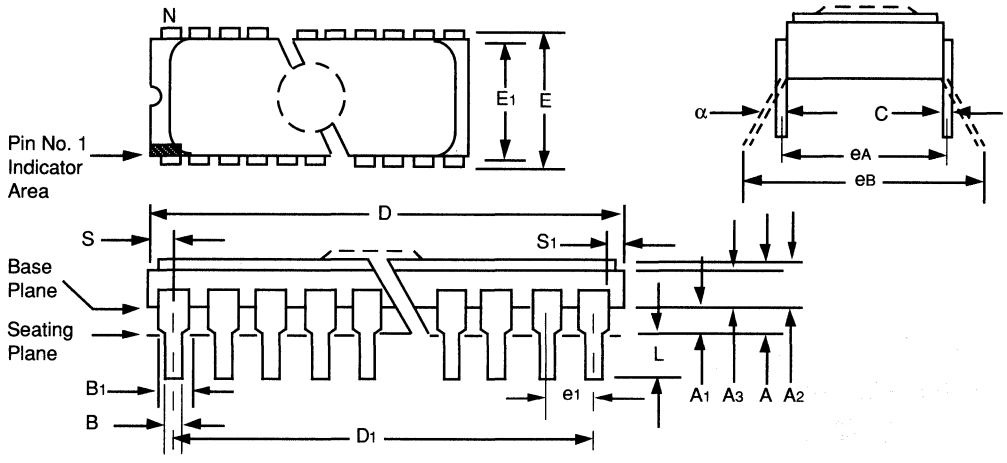
Package Type: 40-Lead Ceramic Side Brazed Dual In-line (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

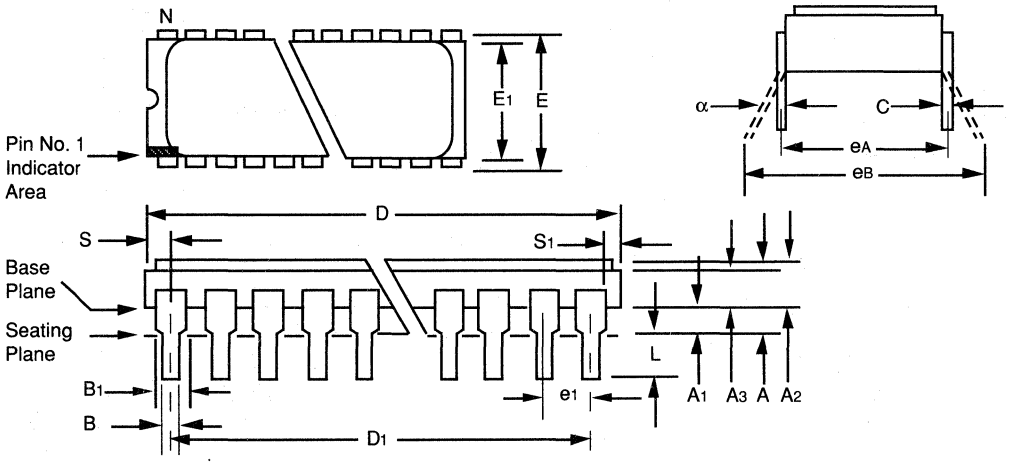
Package Type: 40-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Ceramic Side Brazed Dual In-line (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		0.072	0.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	60.3504	61.5696		2.376	2.424	
D1	58.2168	58.6232	**Reference**	2.292	2.308	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.290	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	48	48		48	48	
S	–	2.4892		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Ceramic Cerdip Dual In-line Family

Symbol List for Ceramic Cerdip Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

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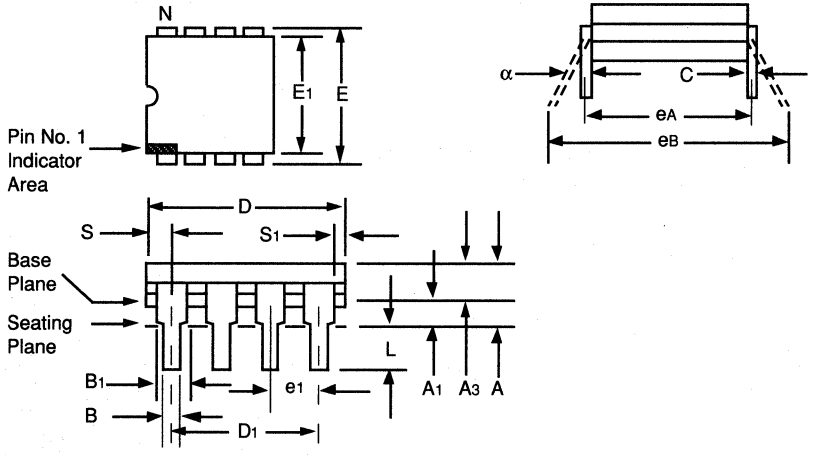
Packaging Diagrams and Parameters

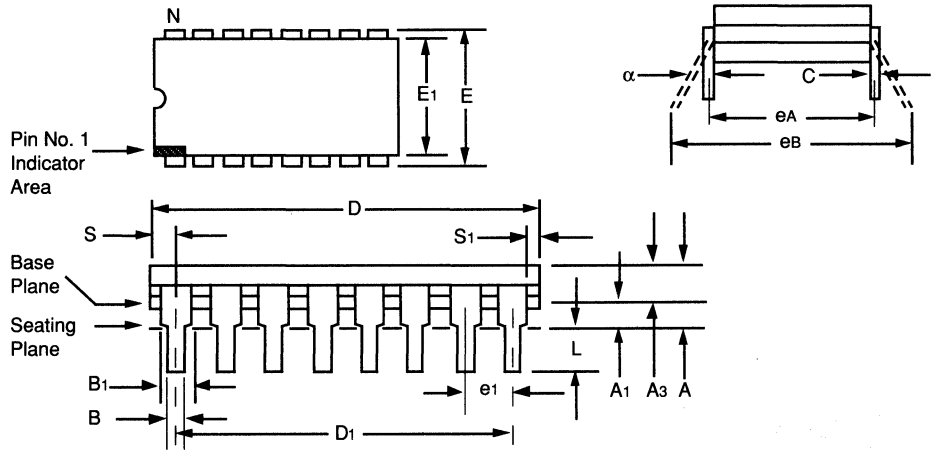
Package Type: 8-Lead Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	9.398	10.287		0.370	0.405	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Referemce	0.290	0.320	Reference
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	8	8		8	8	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

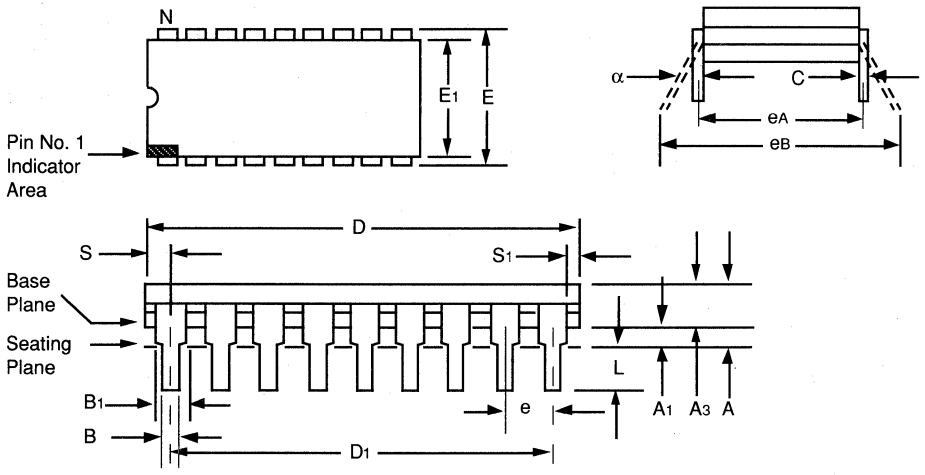
Package Type: 16-Lead Ceramic Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.191	5.080		0.165	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	19.050	20.320		0.750	0.800	
D1	17.780	17.780	Reference	0.700	0.700	Reference
E	7.493	8.255		0.295	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	16	16		16	16	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

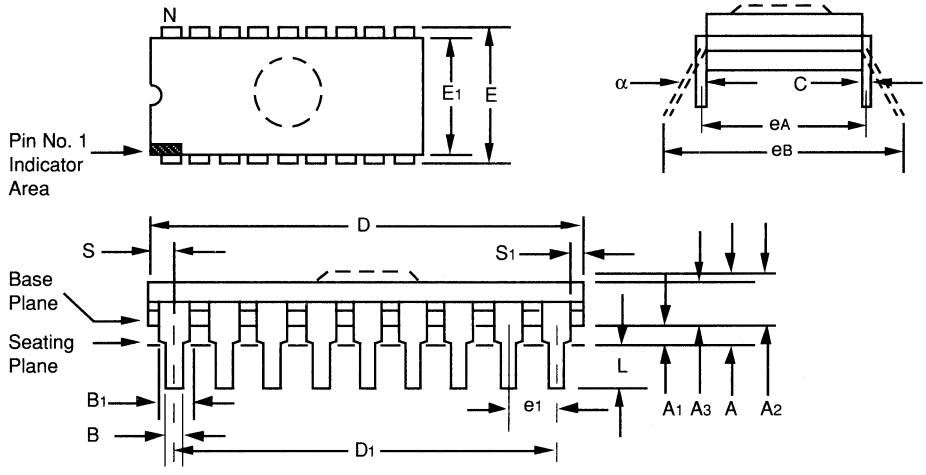
Package Type: 18-Lead Ceramic Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

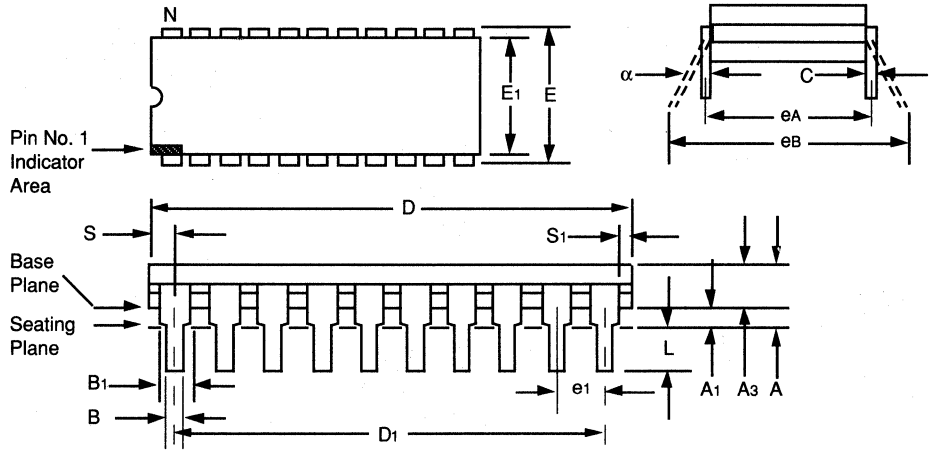
Package Type: 18-Lead Cerdip Dual In-line with Window (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	**Reference**	0.800	0.800	**Reference**
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.366	8.128	**Reference**	0.290	0.320	**Reference**
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

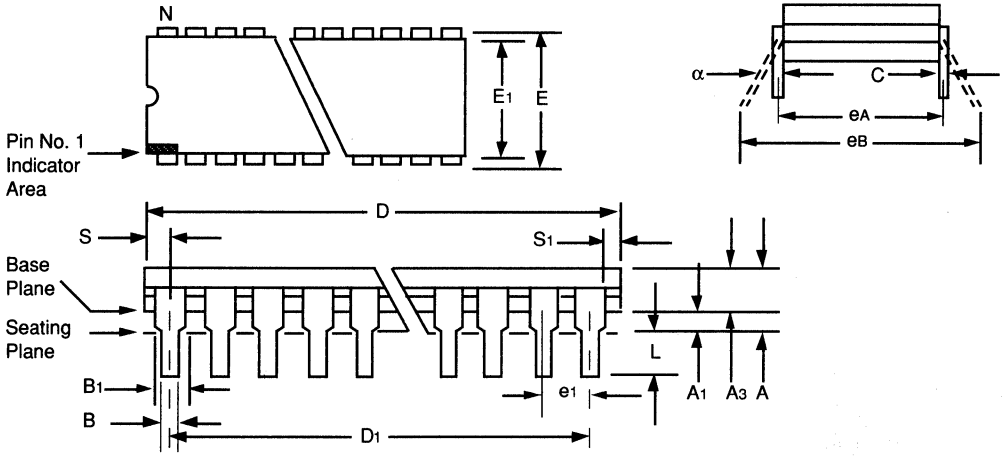
Package Type: 20-Lead Ceramic Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	.508		—	0.200	
A1	0.381	1.778		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.81	4.445		0.150	0.175	
B	0.355	0.584		0.014	0.023	
B1	1.27 typ	1.27 typ	Typical	0.050 typ	0.050 typ	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	23.876	24.892		0.940	0.980	
D1	22.86	22.86	Reference	0.900	0.900	Reference
E	7.62	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.54	2.54	Typical	0.100	0.100	Typical
eA	7.62	7.62	Reference	0.300	0.300	Reference
eB	7.62	10.16		0.300	0.400	
L	3.175	3.81		0.125	0.150	
N	20	20		20	20	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.27		0.015	0.050	

Packaging Diagrams and Parameters

Package Type: 22-Lead Ceramic Cerdip Dual In-line (.400 mil)

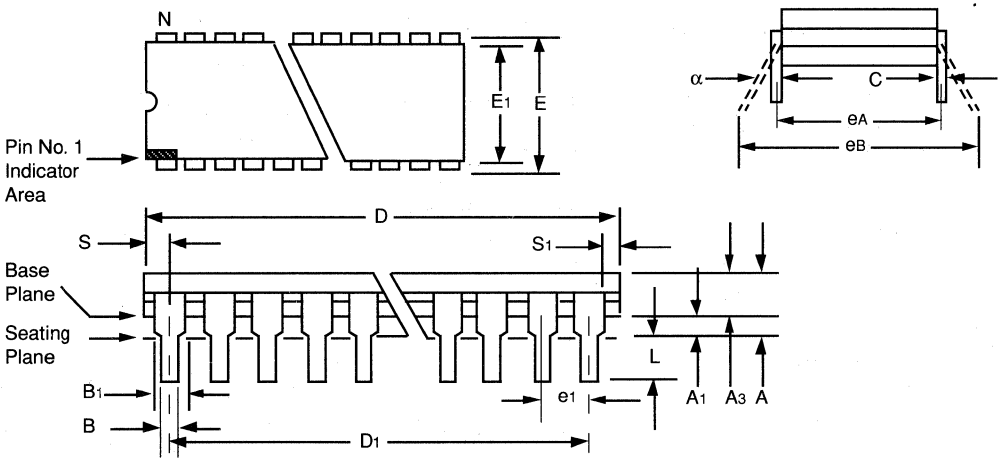


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	26.670	27.940		1.050	1.100	
D1	25.400	25.400	Reference	1.000	1.000	Reference
E	10.160	10.922		0.400	0.430	
E1	8.890	10.414		0.350	0.410	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	9.906	10.668	Reference	0.390	0.420	Reference
eB	10.160	12.700		0.400	0.500	
L	3.175	3.810		0.125	0.150	
N	18	18		22	22	
S	—	1.270		—	0.050	
S1	0.127	1.270		0.005	0.050	

8

Packaging Diagrams and Parameters

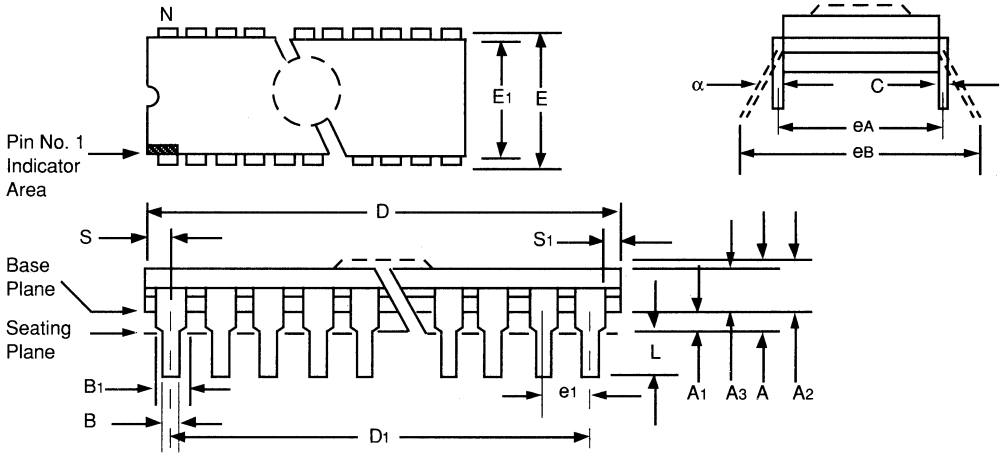
Package Type: 24-Lead Ceramic Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.894		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

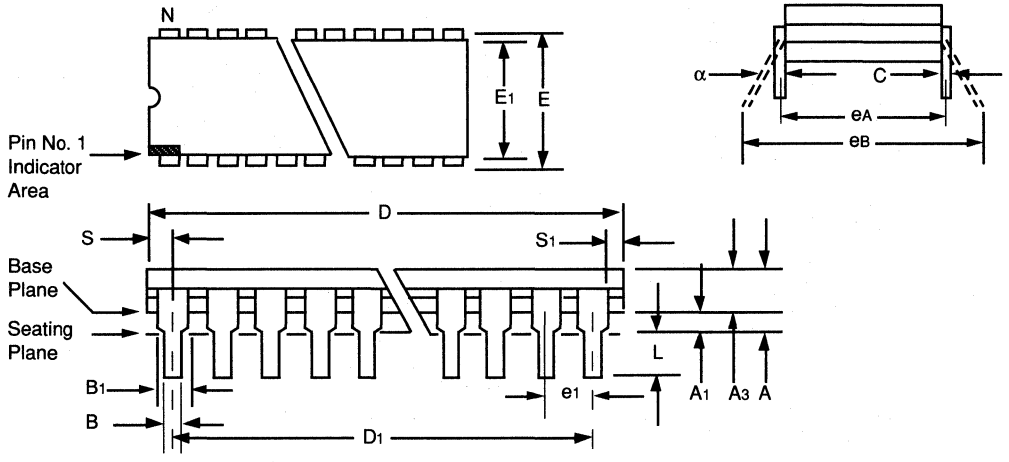
Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	7.62	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.366	8.128	**Reference**	0.290	0.320	**Reference**
eB	7.62	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

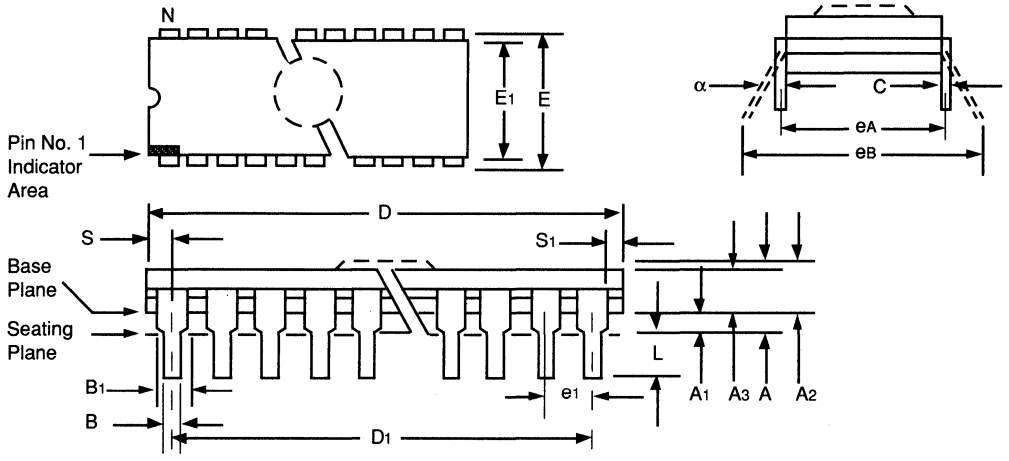
Package Type: 24-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.127	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	15.748	**Reference**	0.590	0.620	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.127	1.778		0.015	0.070	

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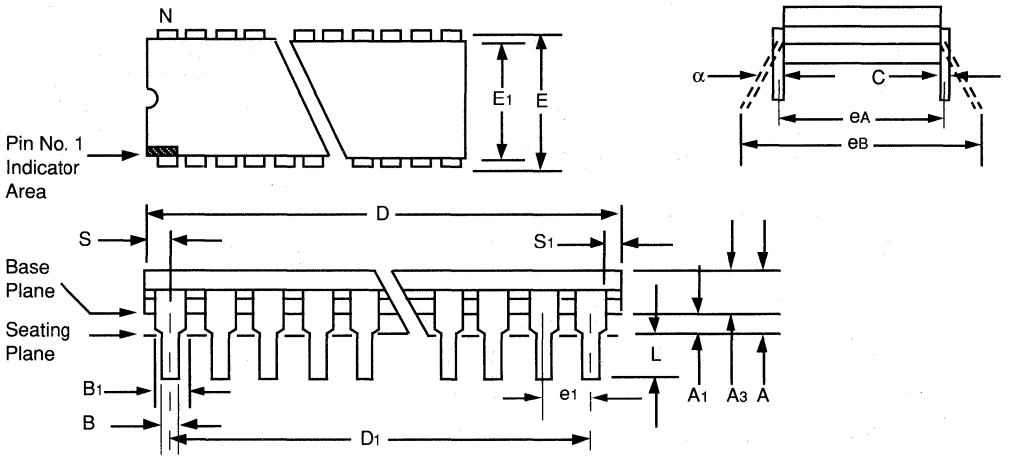
Packaging Diagrams and Parameters

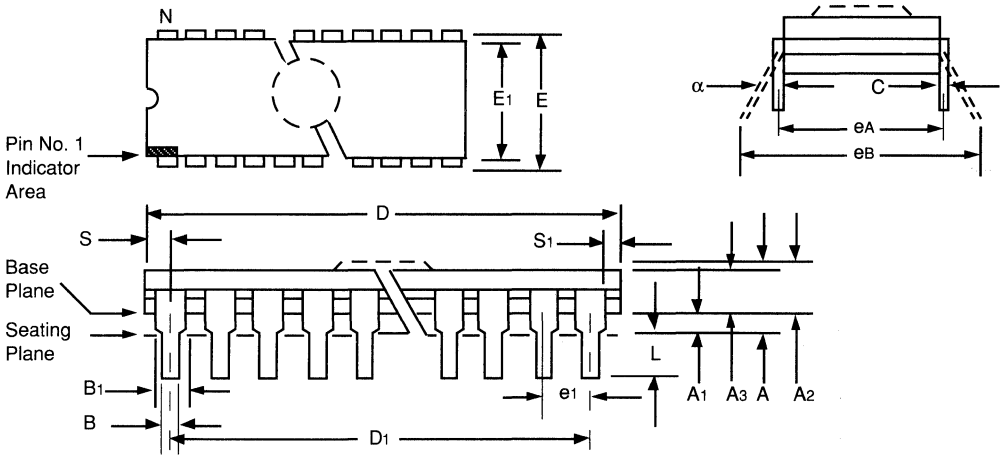
Package Type: 28-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	36.195	36.195		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	8.128	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)

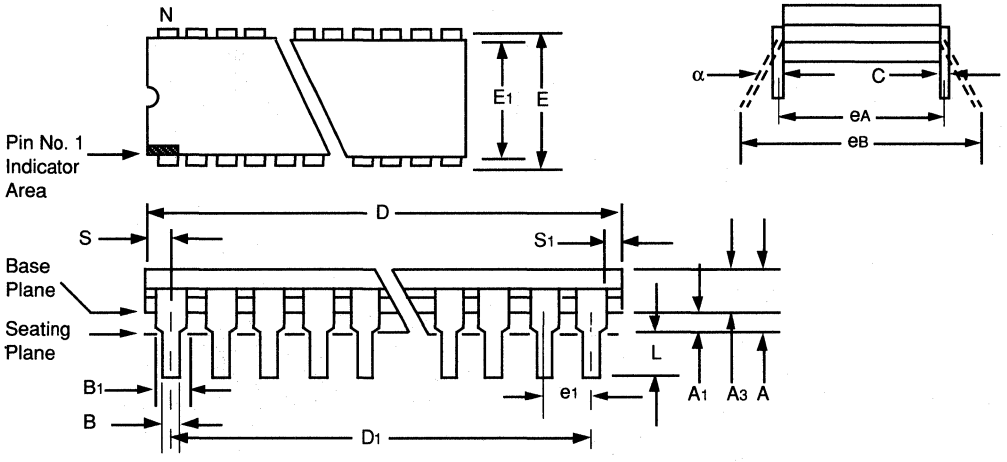


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	36.195	36.195		1.425	1.475	
D1	33.020	33.020	**Reference**	1.300	1.300	**Reference**
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	8.128	**Reference**	0.590	0.620	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

8

Packaging Diagrams and Parameters

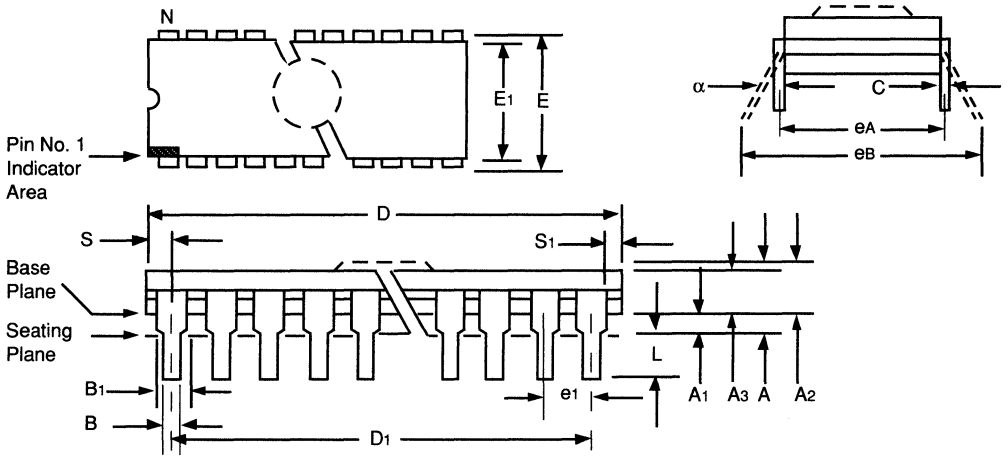
Package Type: 40-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	–	–	Ref. A3	–	–	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	16.002	Reference	0.590	0.630	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699	Ref. A3	0.150	0.185	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	16.002	Reference	0.590	0.630	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

8

Packaging Diagrams and Dimensions

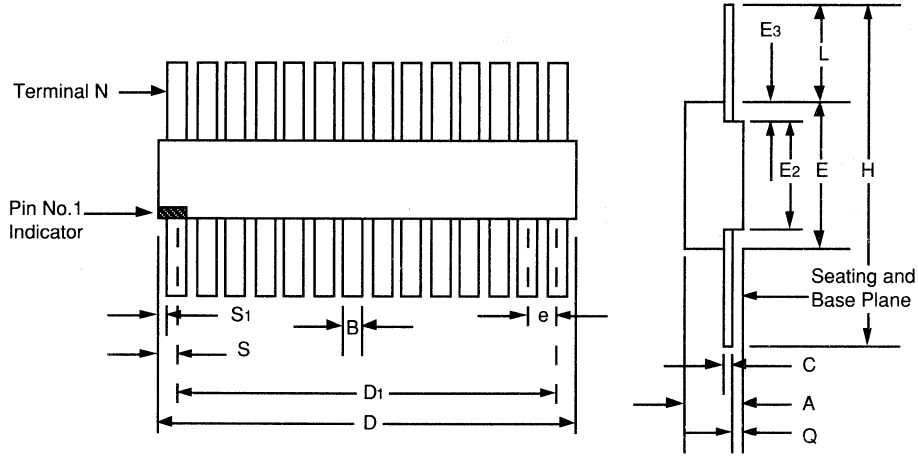
Ceramic Flatpack Family

Symbol List for Ceramic Flatpack Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_2, E_3	Body width parameters not including leads
e	Linear spacing between center lines of body standoffs (terminal leads)
H	Other package width parameter
L	Distance from package body to end of lead
N	Total number of potentially useable lead positions
Q	Distance between seating plane and lead
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameters "B" and "C" are nominal.

Packaging Diagrams and Dimensions

Package Type: 28-Lead Ceramic Flatpack



Package Group: Ceramic Flatpack (CFPK)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.286	3.302		0.090	0.130	
B	0.381	0.4826		0.015	0.019	Typical
C	0.0762	0.1524		0.003	0.006	Typical
D	17.780	18.796		0.700	0.740	
D_1	16.307	16.713		0.642	0.658	Reference
E	9.652	10.668		0.380	0.420	
E_2	9.756	–		0.180	–	
E_3	0.762	–		0.030	–	
e	1.270	1.270		0.050	0.050	Typical
H	22.352	29.464		0.880	1.160	
L	6.350	9.398		0.250	0.370	
N	28	28		28	28	
Q	0.660	1.143		0.026	0.045	
S	0.889	1.016		0.035	0.040	
S_1	0.254	0.381		0.010	0.015	

Packaging Diagrams and Parameters

Ceramic Leadless Chip Carrier Family

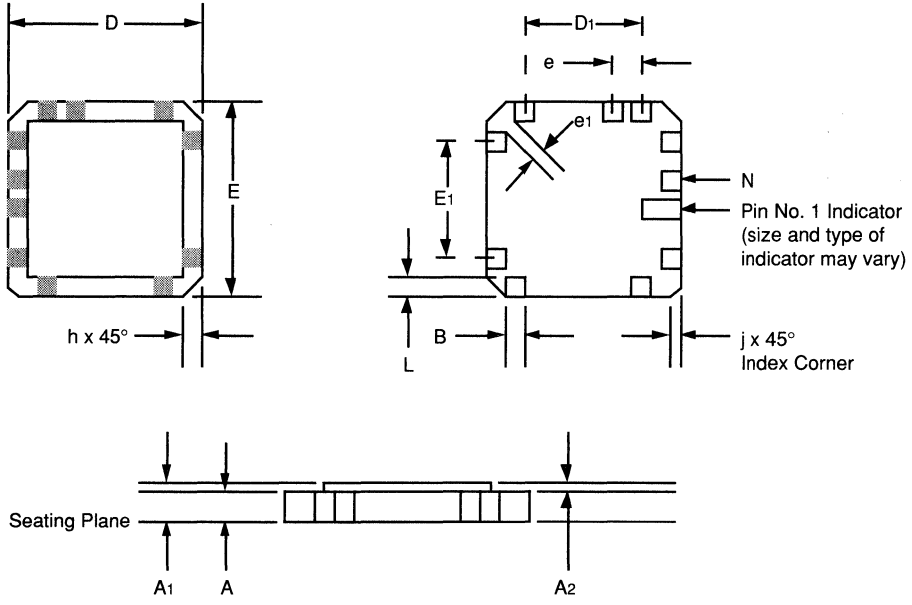
Symbol List for Ceramic Leadless Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Thickness of base body
A_1	Total package height
A_2	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package dimension of length
D_1, E_1	Body length dimension - end lead center to end lead center
E	Largest overall package dimension of width
e	Linear spacing
e_1	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	Total number of potentially useable lead positions

Notes:

1. Controlling dimension: inches.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by PC board hole size.
4. Dimension "B" is nominal.
5. Corner configuration optional.

Packaging Diagrams and Parameters

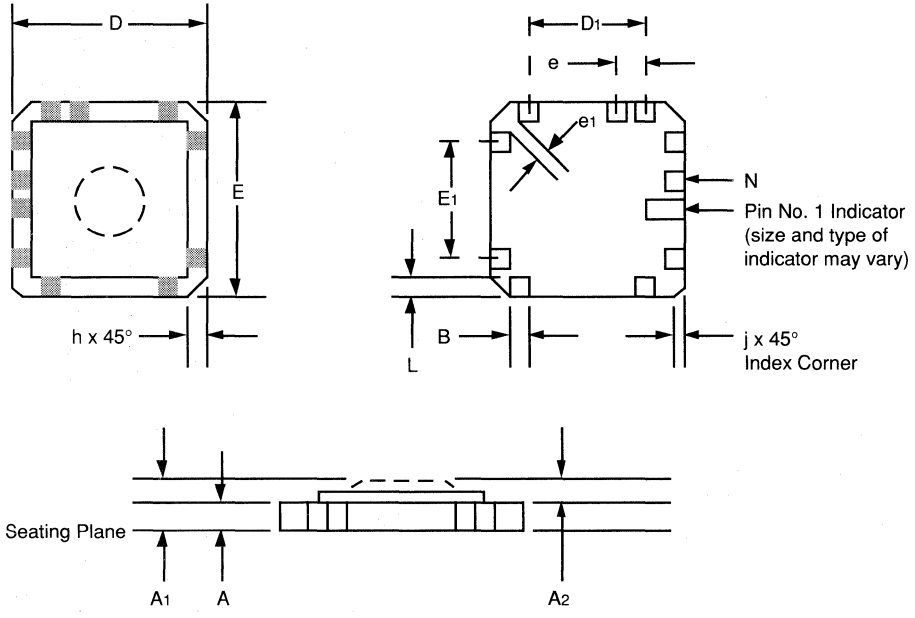
Package Type: 28-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	1.651	2.540		0.065	0.100	
A2	0.254	0.381		0.010	0.015	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	Reference	0.300	0.300	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

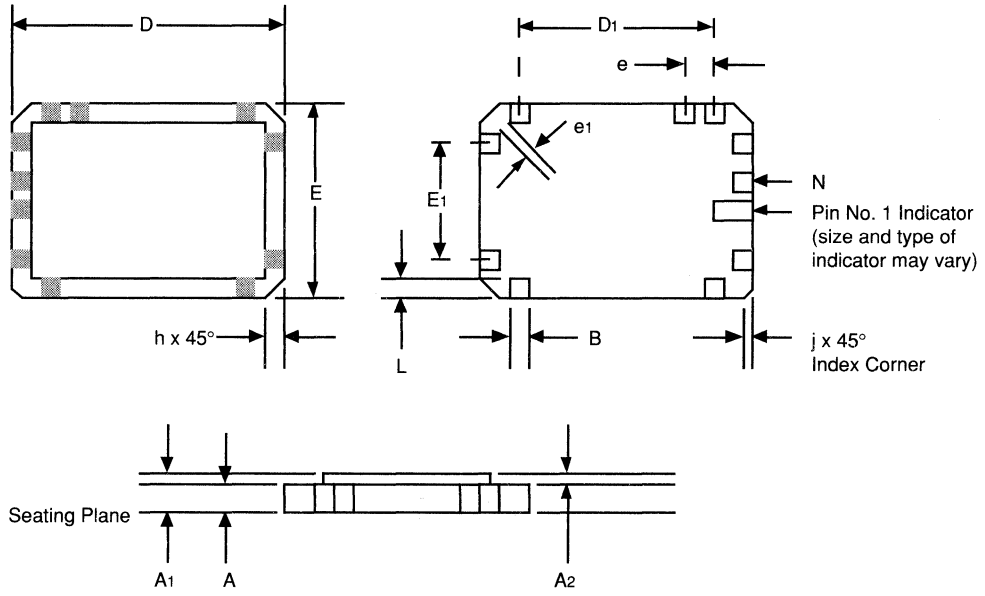
Package Type: 28-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.100	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	**Typical**	0.022	0.028	**Typical**
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
e	1.270	1.270	**Typical**	0.050	0.050	**Typical**
e1	0.38	–	**Typical**	0.015	–	**Typical**
h	1.02	1.02	**Reference**	0.040	0.040	**Reference**
j	0.51	0.51	**Reference**	0.020	0.020	**Reference**
L	1.143	1.397	**Typical**	0.045	0.055	**Typical**
N	28	28		28	28	

Packaging Diagrams and Parameters

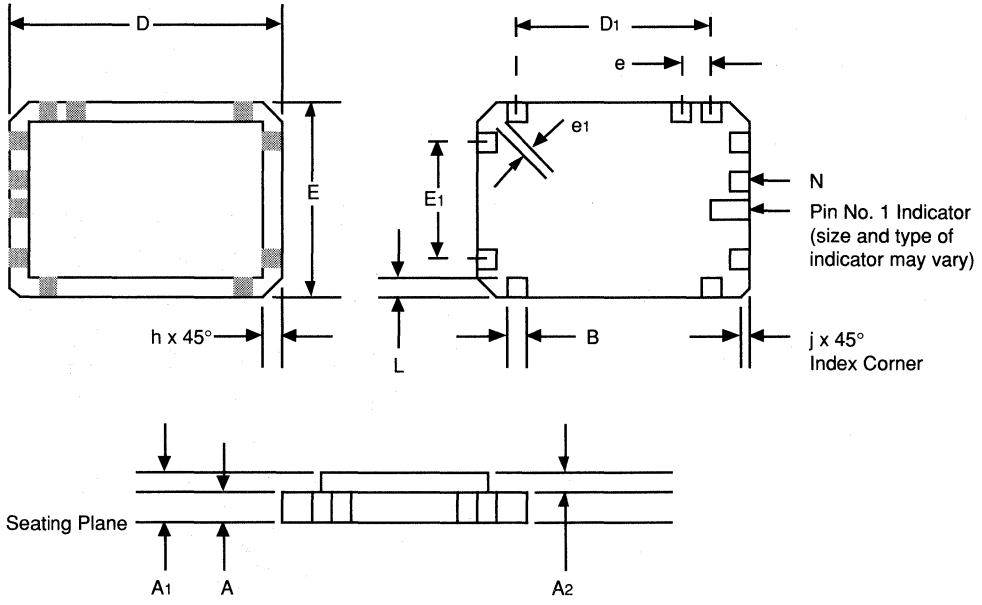
Package Type: 32-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.54	3.048		0.100	0.120	
A2	0.254	0.381		0.010	0.015	
B	0.635	0.7112	Typical	0.025	0.026	Typical
D	13.716	14.224		0.540	0.560	
D1	9.98	10.34	Reference	0.393	0.407	Reference
E	11.2268	11.684		0.442	0.458	
E1	7.442	7.80	Reference	0.293	0.307	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

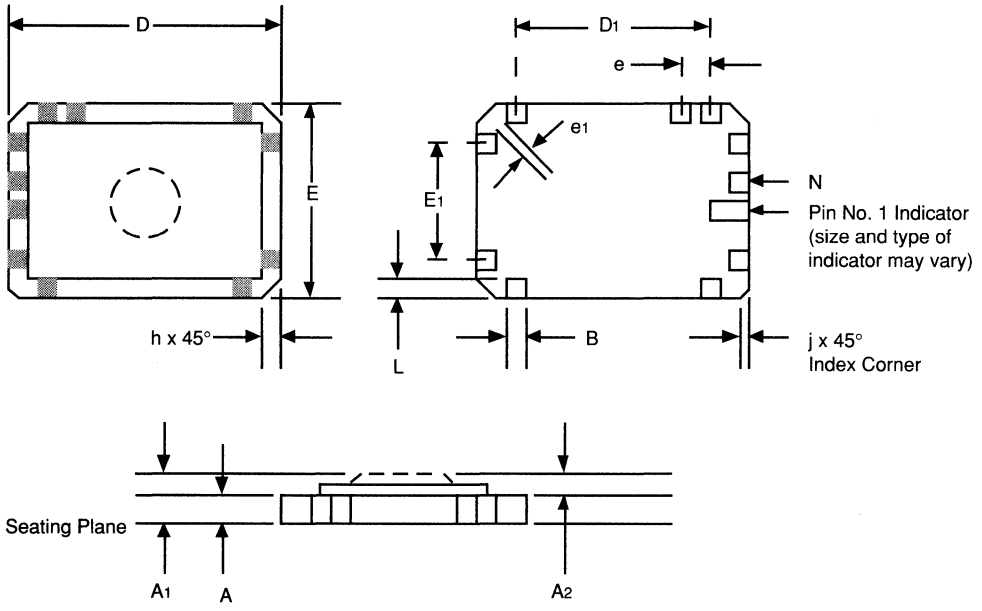
Package Type: 32-Lead Ceramic Leadless Chip Carrier - FRIT



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A_1	2.286	3.302		0.090	0.130	
A_2	0.635	1.143		0.025	0.045	
B	0.5588	0.7112	**Typical**	0.022	0.028	**Typical**
D	13.716	14.224		0.540	0.560	
D_1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
E	11.2268	11.6332		0.442	0.458	
E_1	10.160	10.160	**Reference**	0.400	0.400	**Reference**
e	1.270	1.270	**Typical**	0.050	0.050	**Typical**
e_1	0.38	–	**Typical**	0.015	–	**Typical**
h	1.02	1.02	**Reference**	0.040	0.040	**Reference**
j	0.51	0.51	**Reference**	0.020	0.020	**Reference**
L	1.143	1.397	**Typical**	0.045	0.055	**Typical**
N	32	32		32	32	

Packaging Diagrams and Parameters

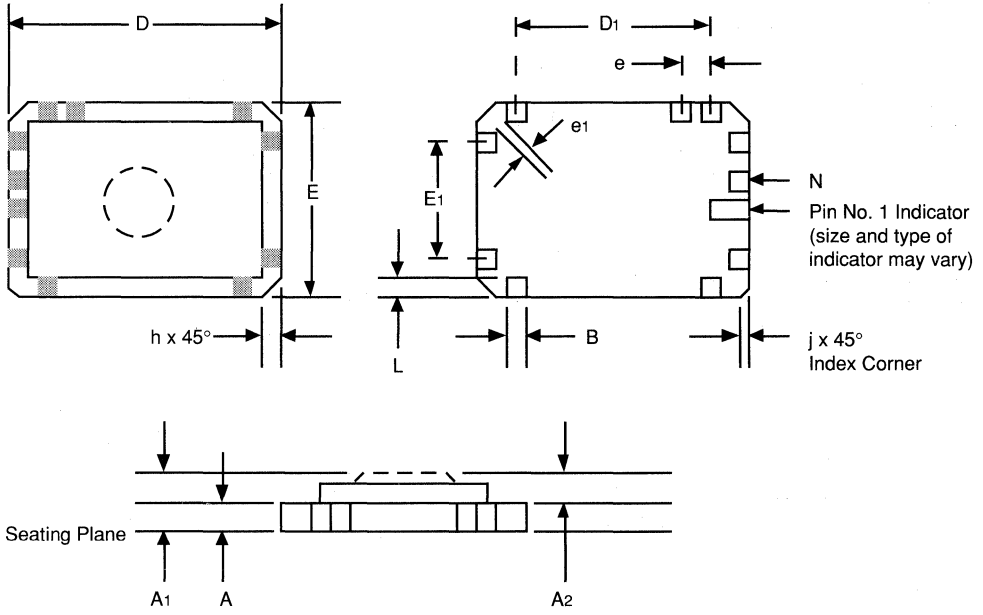
Package Type: 32-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	1.02	1.02	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

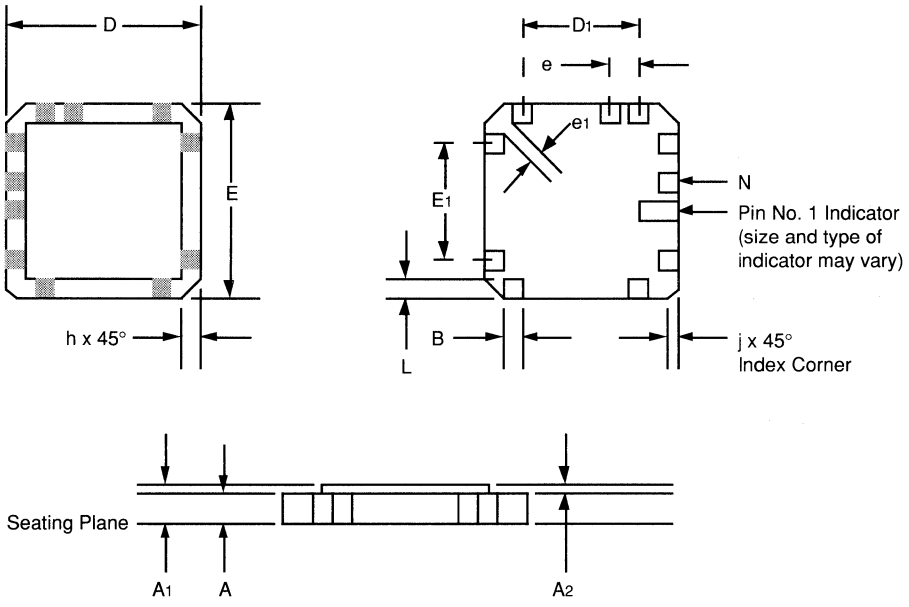
Package Type: 32-Lead Ceramic Leadless Chip Carrier with FRIT Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A_1	2.286	3.302		0.090	0.130	
A_2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	**Typical**	0.022	0.028	**Typical**
D	13.716	14.224		0.540	0.560	
D_1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
E	11.2268	11.6332		0.442	0.458	
E_1	10.160	10.160	**Reference**	0.400	0.400	**Reference**
e	1.270	1.270	**Typical**	0.050	0.050	**Typical**
e_1	0.38	–	**Typical**	0.015	–	**Typical**
h	1.02	1.02	**Reference**	0.040	0.040	**Reference**
j	0.51	0.51	**Reference**	0.020	0.020	**Reference**
L	1.143	1.397	**Typical**	0.045	0.055	**Typical**
N	32	32		32	32	

Packaging Diagrams and Parameters

Package Type: 44-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.37	2.082		0.054	0.082	
A1	1.778	3.048		0.070	0.120	
A2	0.254	1.143		0.010	0.045	
B	0.584	0.7112	Typical	0.023	0.028	Typical
D	16.256	16.8148		0.640	0.662	
D1	12.700	12.700	Reference	0.500	0.500	Reference
E	16.256	16.8148		0.640	0.662	
E1	12.700	12.700	Reference	0.500	0.500	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	44	44		44	44	

Packaging Diagrams and Parameters

Packaging Diagrams and Dimensions

Plastic Dual In-line Family

Symbol List for Plastic Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.
5. Details of pin No. 1 identifier are optional.

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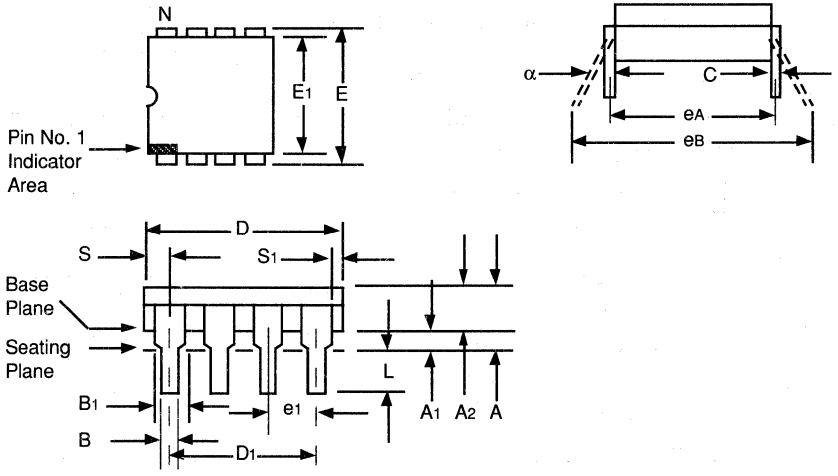
Packaging Diagrams and Dimensions

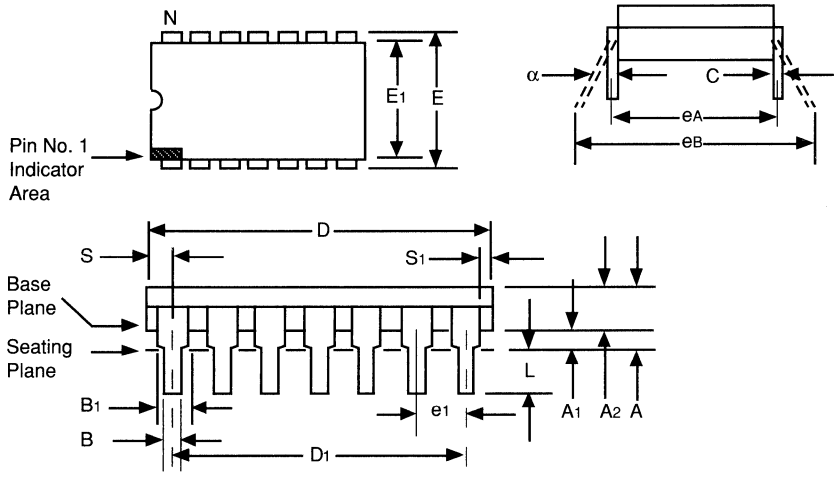
Package Type: 8-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	9.144	10.922		0.360	0.430	
D1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	8	8		8	8	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

Package Type: 14-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	18.415	19.431		0.725	0.765	
D1	15.240	15.240	**Reference**	0.600	0.600	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	14	14		14	14	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

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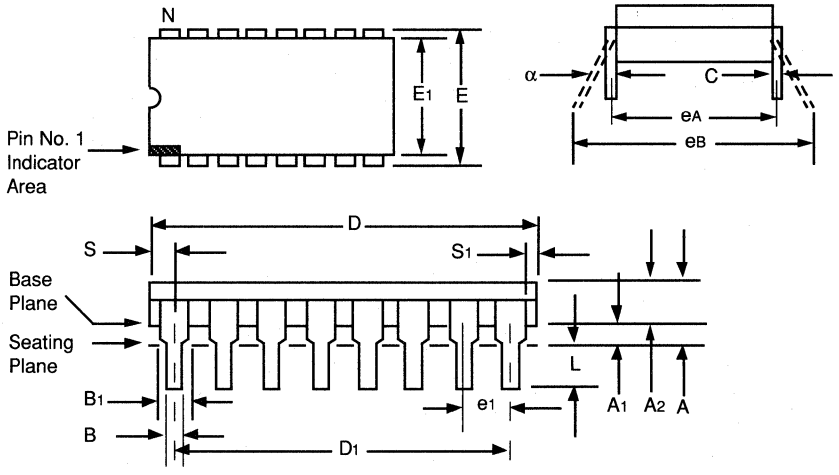
Packaging Diagrams and Dimensions

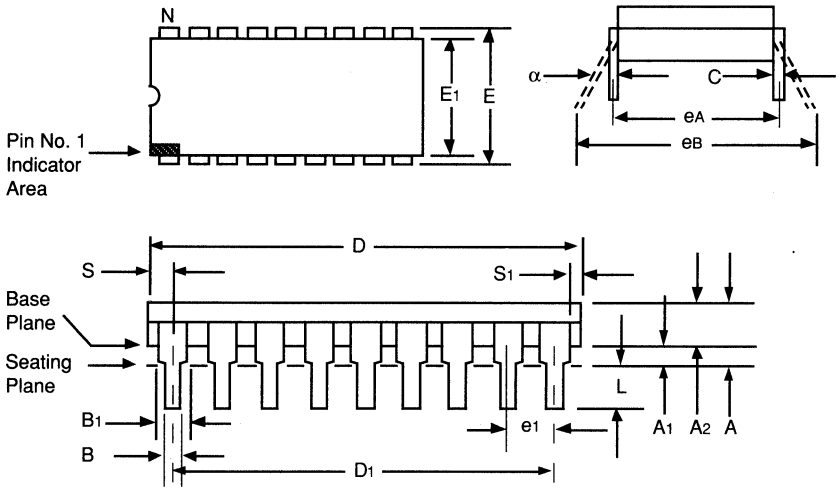
Package Type: 16-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	18.923	19.939		0.745	0.785	
D1	17.780	17.780	**Reference**	0.700	0.700	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.0480	3.556		0.120	0.140	
N	16	16		16	16	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

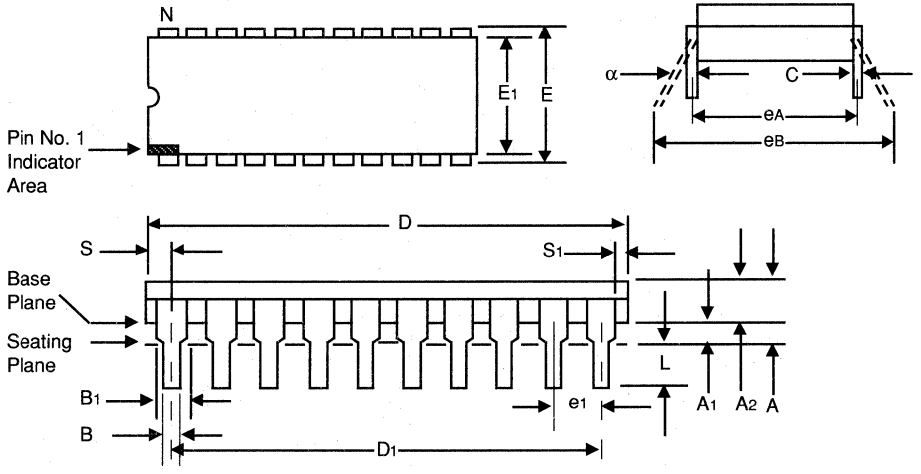
Package Type: 18-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	**Reference**	0.800	0.800	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

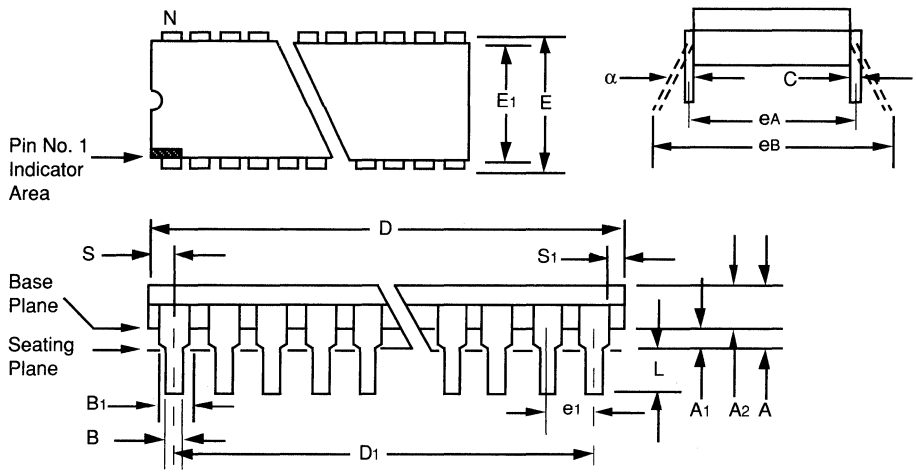
Package Type: 20-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.558		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	24.892	26.924		0.980	1.060	
D1	22.86	22.86	**Reference**	0.900	0.900	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	20	20		20	20	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

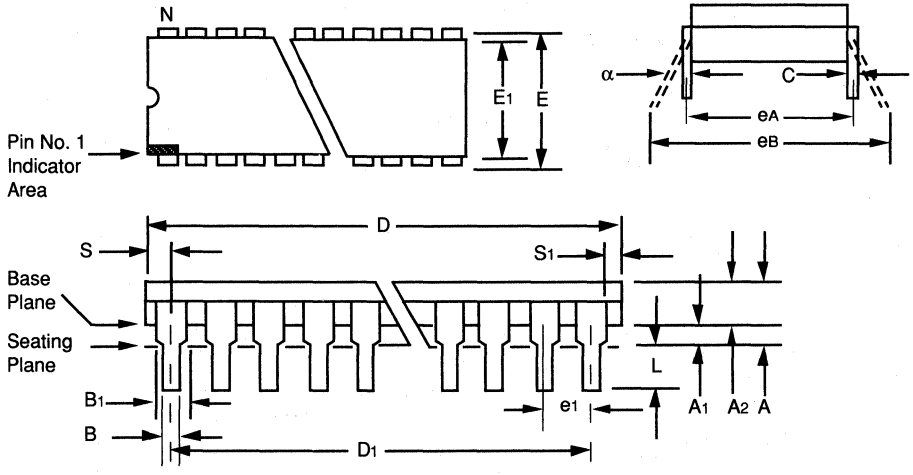
Package Type: 22-Lead Plastic Dual In-line (.400 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	.180		–	.180	
A_1	0.381	–		0.015	–	
A_2	3.175	3.810		0.125	0.150	
B	0.356	0.559		0.014	0.022	
B_1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	26.670	28.448		1.050	1.120	
D_1	25.400	25.400	**Reference**	1.000	1.000	**Reference**
E	9.906	10.795		0.390	0.425	
E_1	8.382	9.398		0.330	0.370	
e_1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
e_A	10.160	10.160	**Reference**	0.400	0.400	**Reference**
e_B	10.160	12.192		0.400	0.480	
L	3.048	3.556		0.120	0.140	
N	22	22		22	22	
S	0.889	–		0.035	–	
S_1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

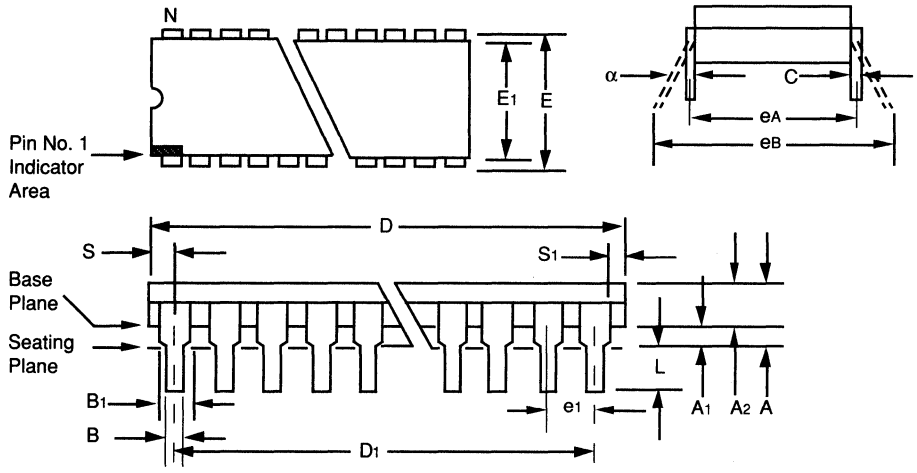
Package Type: 24-Lead Plastic Dual In-line (.600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	30.353	32.385		1.195	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.827	14.224		0.505	0.560	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.494	17.272		0.610	0.680	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Dimensions

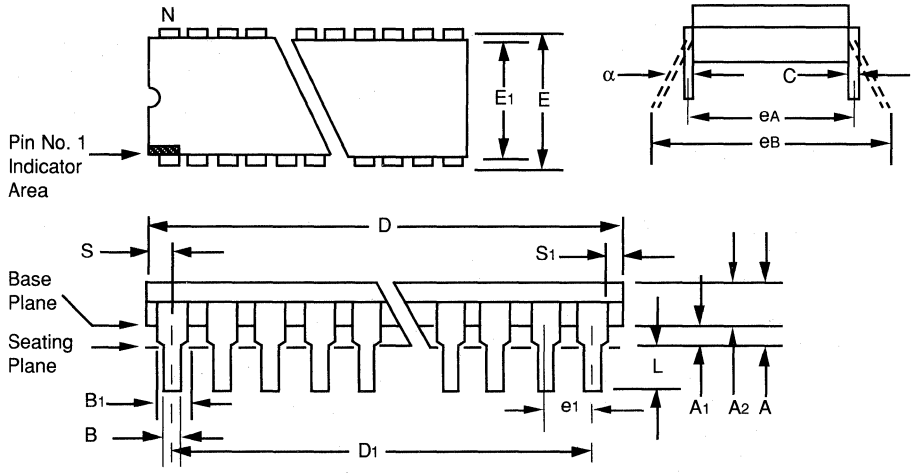
Package Type: 24-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line Package (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	Typical	0.060	0.060	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	31.242	32.258		1.230	1.270	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.381	–		0.015	–	

Packaging Diagrams and Dimensions

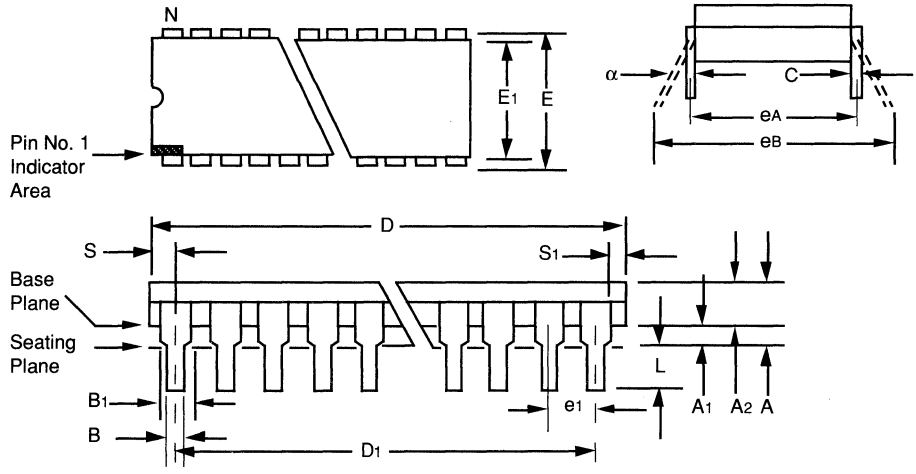
Package Type: 28-Lead Dual In-line Plastic (.600 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.778	**Typical**	0.050	0.070	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	35.560	37.084		1.400	1.460	
D1	33.020	33.020	**Reference**	1.300	1.300	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	28	28		28	28	
S	0.889	–		0.035	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Dimensions

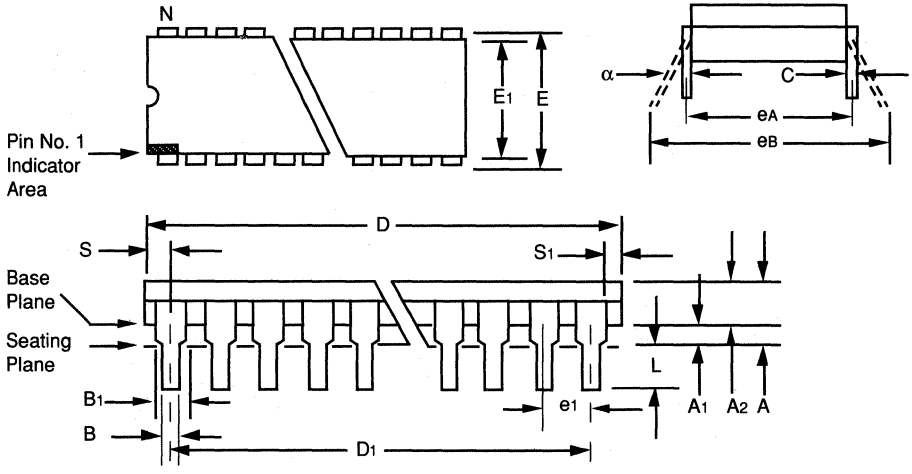
Package Type: 40-Lead Plastic Dual In-line (.600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.778	**Typical**	0.050	0.070	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	**Reference**	1.900	1.900	**Reference**
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Dimensions

Package Type: 48-Lead Plastic Dual In-line (.600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	61.468	62.230		2.420	2.450	
D1	58.420	58.420	**Reference**	2.300	2.300	**Reference**
E	15.240	15.875		0.600	0.625	
E1	13.716	14.224		0.540	0.560	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	48	48		48	48	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Plastic Leaded Chip Carrier Family

Symbol List for Plastic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance from seating plane to highest point of body
A_1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D_1/E_1	Plastic body dimension
D_2/E_2	Footprint
D_3/E_3	Footprint
LT	Lead thickness
N	Total number of potentially useable lead positions
N_d	Total number of leads on short side (rectangular)
N_e	Total number of leads on long side (rectangular)

Notes:

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.

2 Datum plane -H- located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.

3 Datums D–E and F–G to be determined where center leads exit plastic body at datum plane -H-.

4 To be determined at seating plane -C-.

5 Transition is optional.

6 Plastic body details between leads are optional.

7 Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is .254 mm/.010 in. per side. Dimensions D and E include mold mismatch and are dtermined at parting line.

8 Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated.
Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.

9 Location to datums -A- and -B- to be determined at plane -H-.

10 All dimensions and tolerances include lead trim offset and lead finish.

11 These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.

12 Controlling dimension: inches.

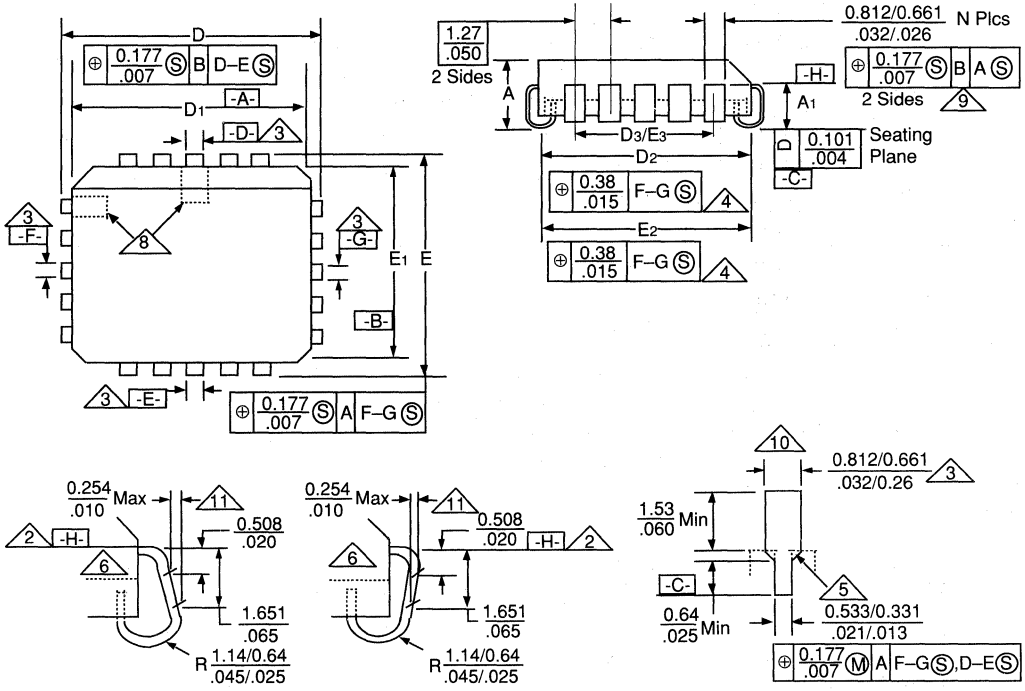
X Sum of dam bar protrusions to be 0.17 (.007) max per lead.

Y Feature is not required, but is optional at manufacturer's discretion.

8

Packaging Diagrams and Parameters

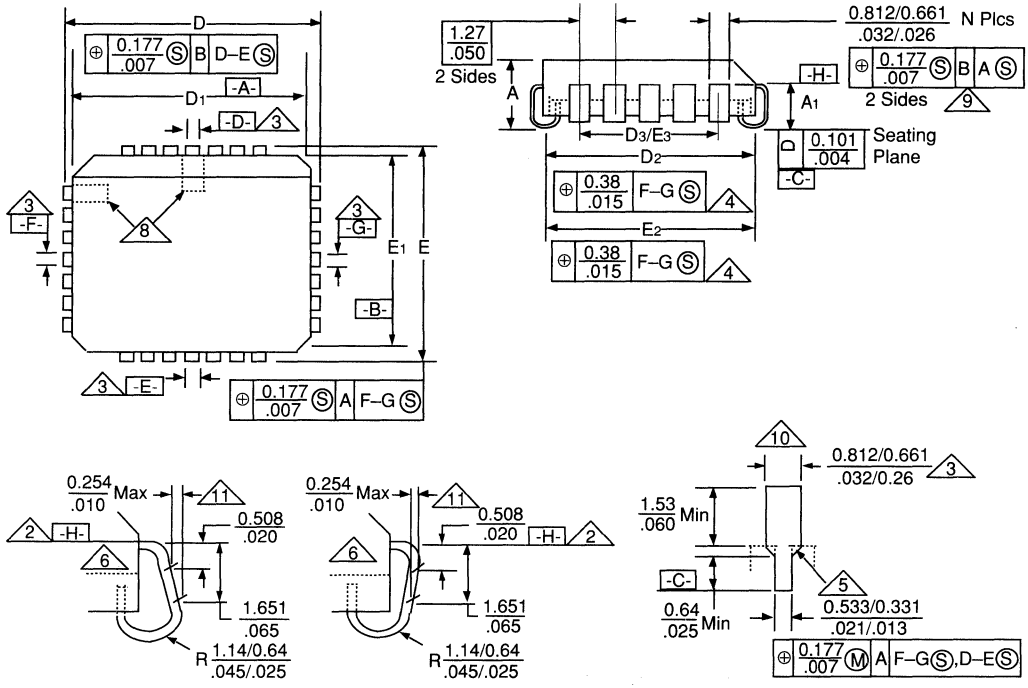
Package Type: 20-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	9.779	10.033		0.385	0.395	
D1	8.890	9.042		0.350	0.356	
D2	7.493	8.255		0.295	0.325	
D3	5.080	5.080	Reference	0.200	0.200	Reference
E	9.779	10.033		0.385	0.395	
E1	8.890	9.042		0.350	0.356	
E2	7.493	8.255		0.295	0.325	
E3	5.080	5.080	Reference	0.200	0.200	Reference
N	20	20		20	20	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

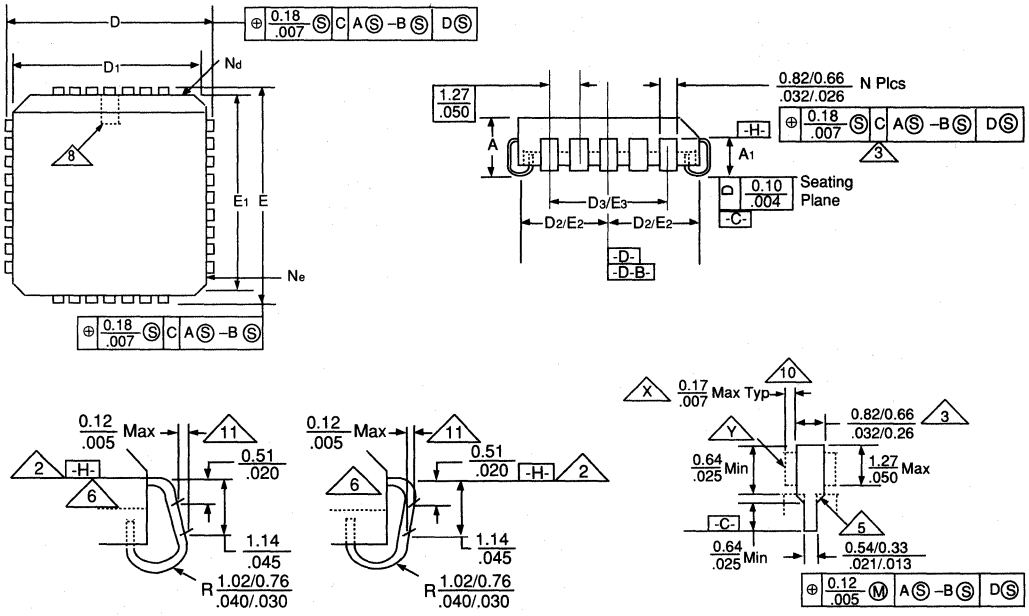
Package Type: 28-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	12.319	12.573		0.485	0.495	
D1	11.430	11.582		0.450	0.456	
D2	10.414	10.922		0.410	0.430	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	12.319	12.573		0.485	0.495	
E1	11.430	11.582		0.450	0.456	
E2	10.414	10.922		0.410	0.430	
E3	7.620	7.620	Reference	0.300	0.300	Reference
N	28	28		28	28	
. CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

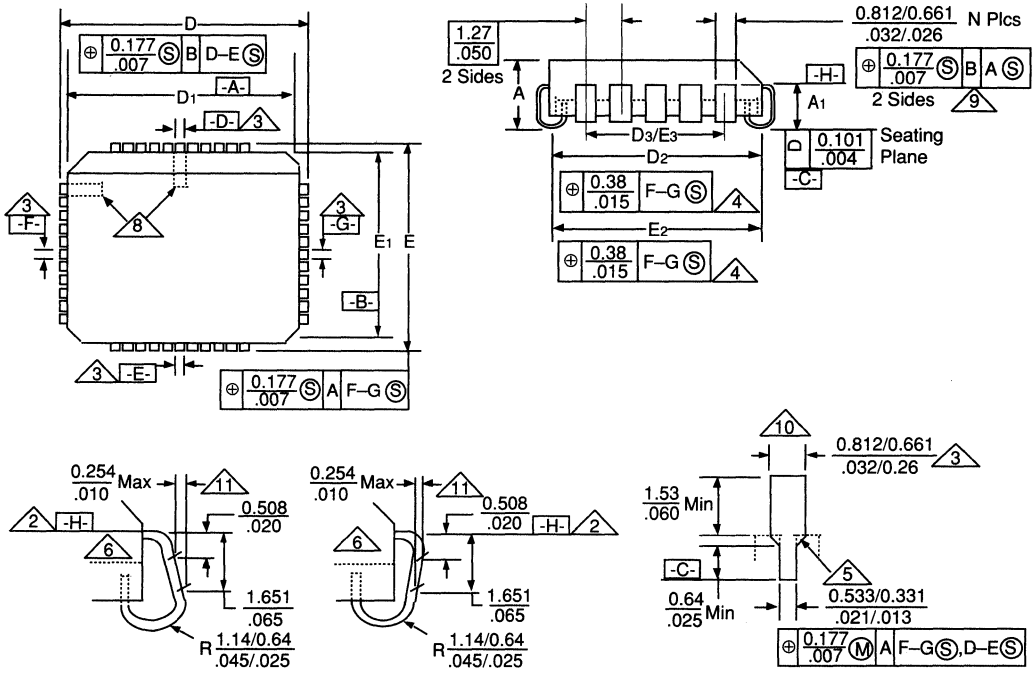
Package Type: 32-Lead Plastic Leaded Chip Carrier (Rectangle)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.048	3.556		0.120	0.140	
A1	1.905	2.413		0.075	0.095	
D	12.319	12.573		0.485	0.495	
D1	11.35	11.506		0.447	0.453	
D2	4.826	5.334		0.190	0.210	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	14.859	15.113		0.585	0.595	
E1	13.893	14.046		0.547	0.553	
E2	6.096	6.858		0.240	0.270	
E3	10.160	10.160	Reference	0.400	0.400	Reference
N	32	32		32	32	
Nd	7	7		7	7	
Ne	9	9		9	9	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D1	16.510	16.662		0.650	0.656	
D2	15.494	16.002		0.610	0.630	
D3	12.700	12.700	**Reference**	0.500	0.500	**Reference**
E	17.399	17.653		0.685	0.695	
E1	16.510	16.662		0.650	0.656	
E2	15.494	16.002		0.610	0.630	
E3	12.700	12.700	**Reference**	0.500	0.500	**Reference**
N	44	44		44	44	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

8

Packaging Diagrams and Parameters

Plastic Small Outline Family

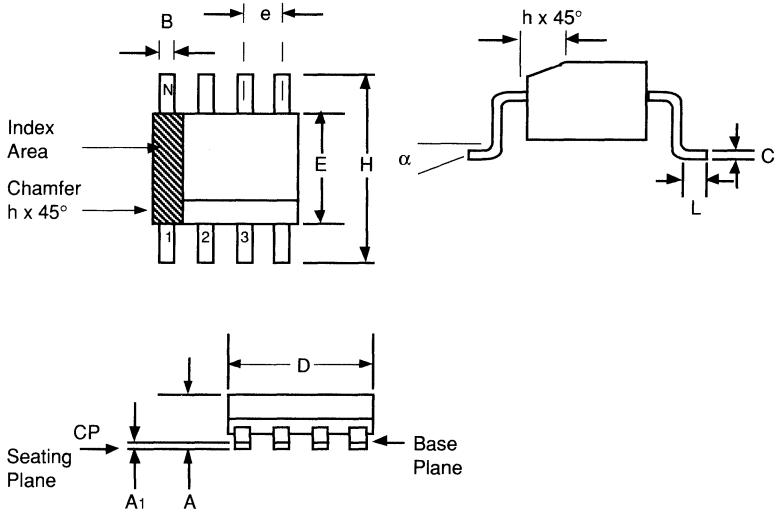
Symbol List for Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spaciing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead postions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.0086 inches).
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

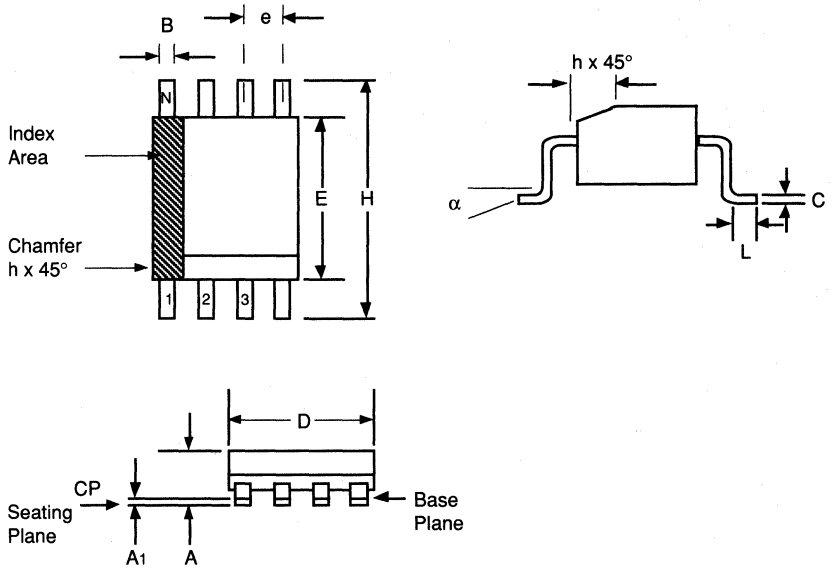
Package Type: 8-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	4.8006	4.9784		0.189	0.196	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	8	8		8	8	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

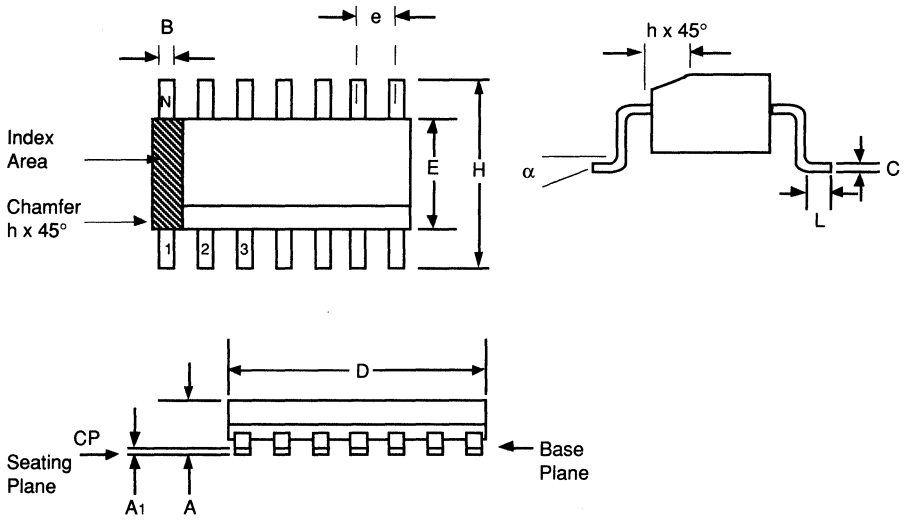
Package Type: 8-Lead Plastic Surface Mount (SOIC - Medium, 200 mil Body)



Package Group: Plastic SOIC (SM)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.778	2.032		0.070	0.080	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	5.08	5.334		0.200	0.210	
E	5.156	5.410		0.203	0.213	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	7.62	8.382		0.300	0.330	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	14	14		14	14	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

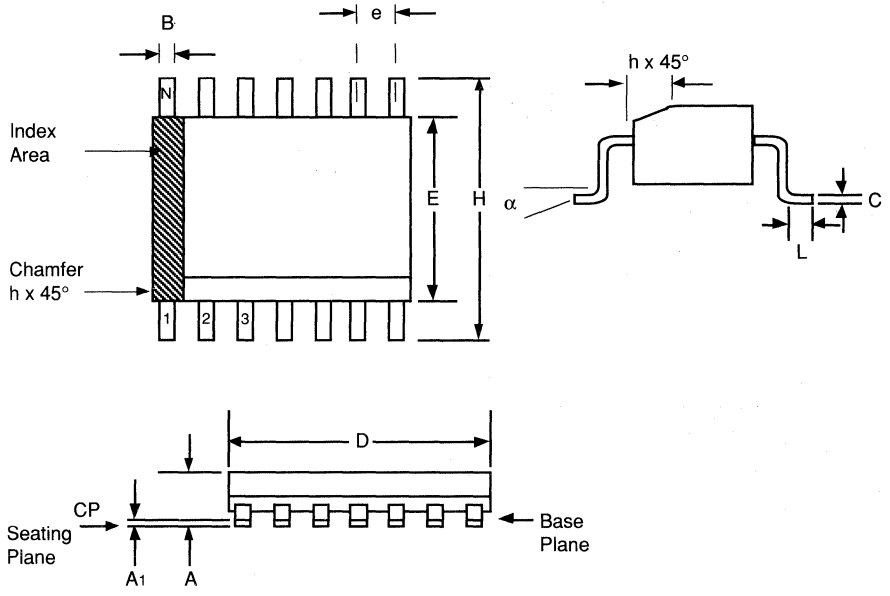
Package Type: 14-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	5.08	5.334		0.387	0.393	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	14	14		16	16	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

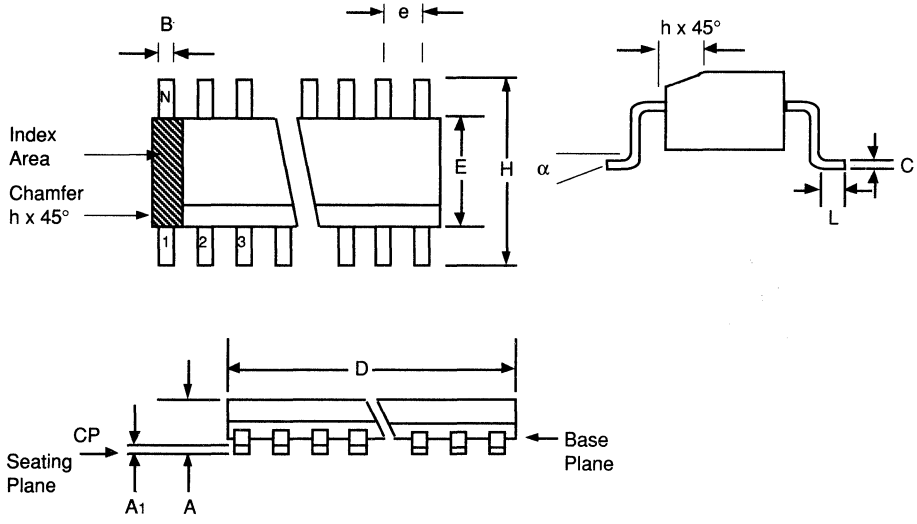
Package Type: 14-Lead Plastic Surface Mount (SOIC - Wide. 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	0.8763	9.271		0.345	0.365	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	14	14		14	14	
cp	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

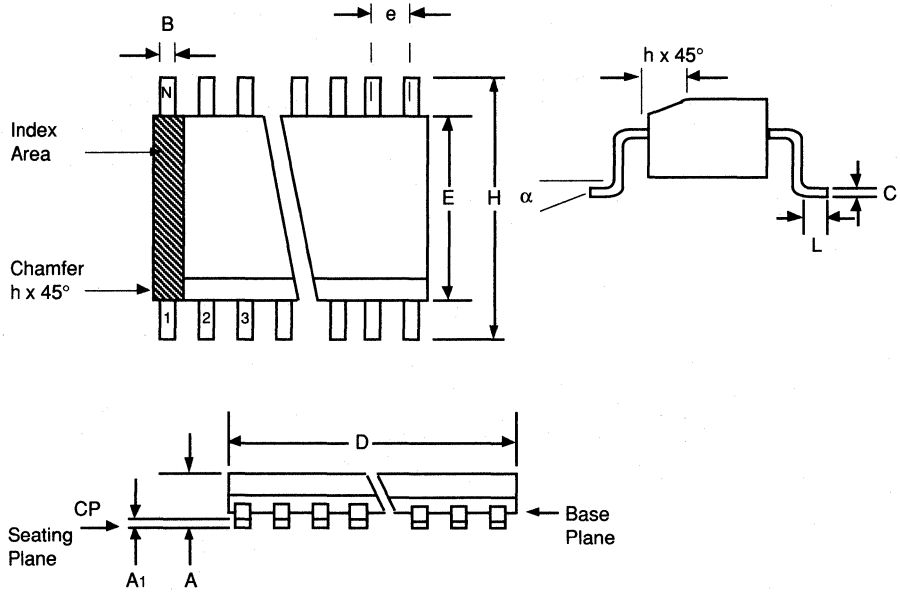
Package Type: 16-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	5.08	5.334		0.387	0.393	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	14	14		16	16	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

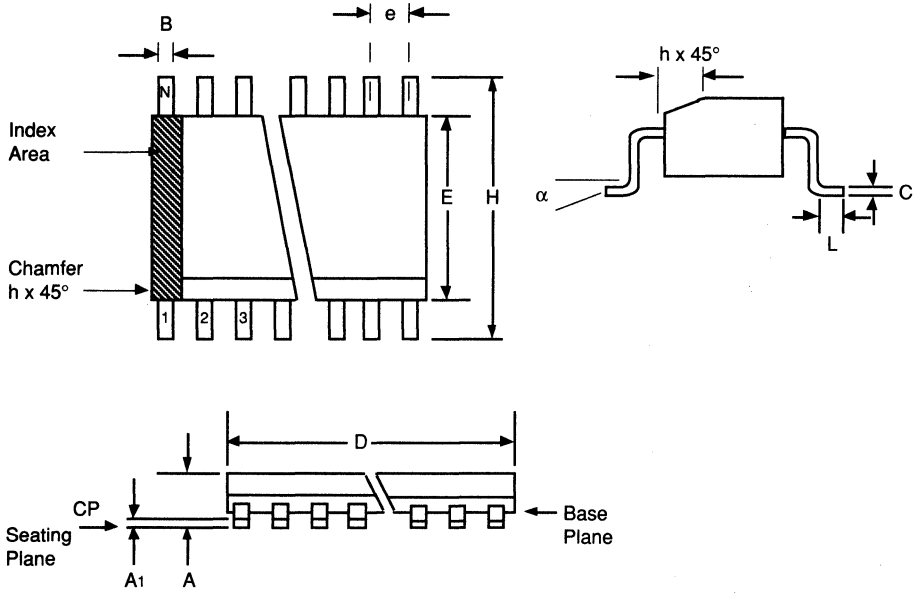
Package Type: 16-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	10.1092	10.4902		0.398	0.413	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	16	16		16	16	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

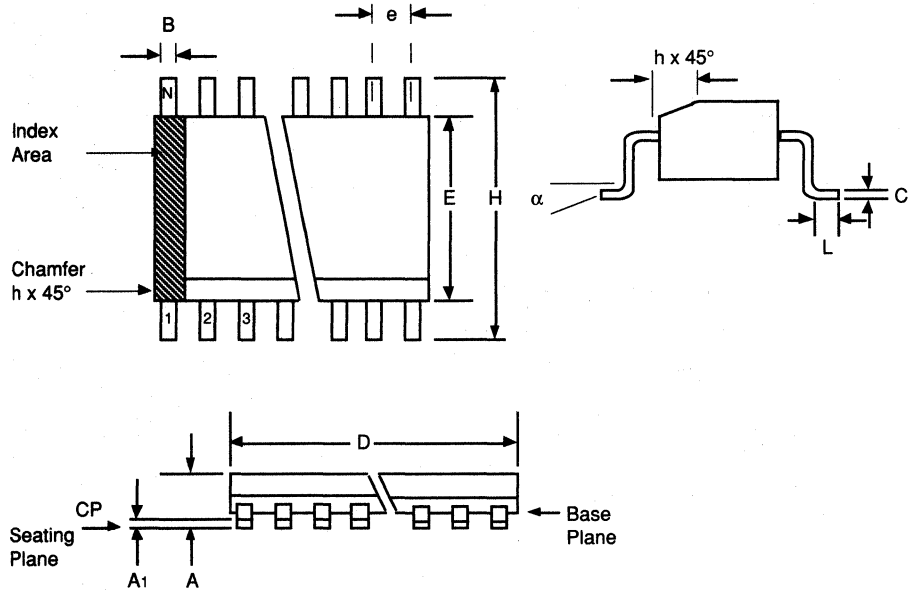
Package Type: 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

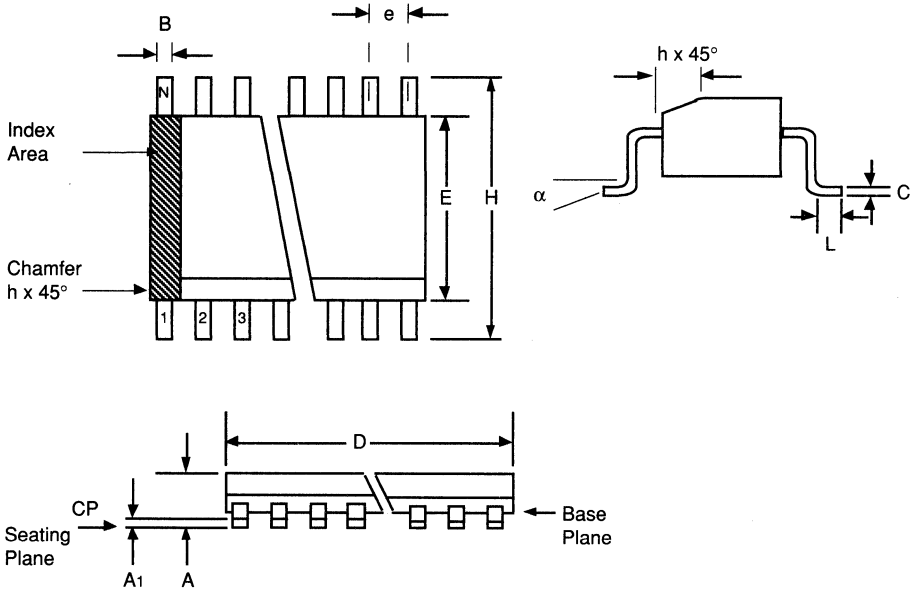
Package Type: 20-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	12.5984	13.0048		0.496	0.512	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	20	20		20	20	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

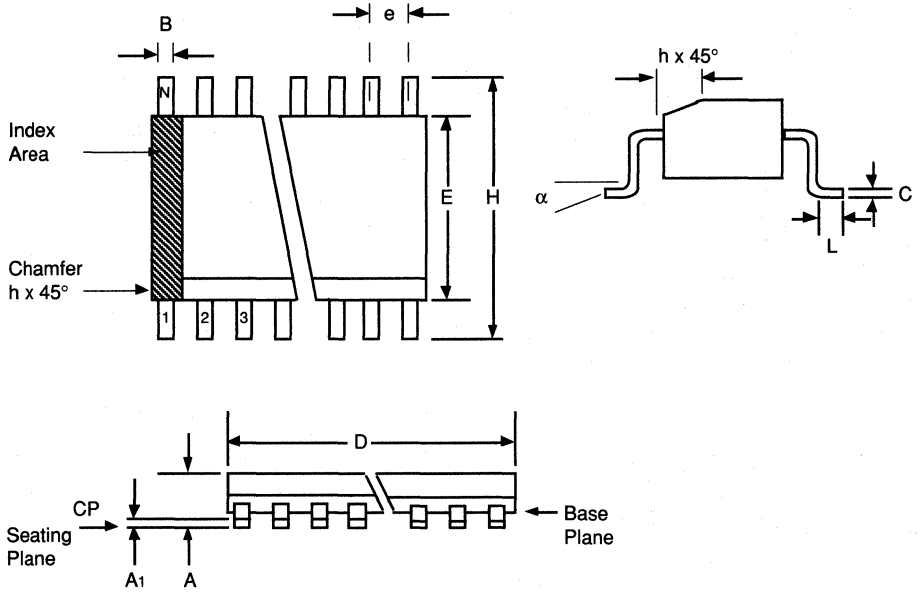
Package Type: 24-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	15.2146	15.5956		0.599	0.614	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	24	24		24	24	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	17.7038	18.0848		0.697	0.712	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

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