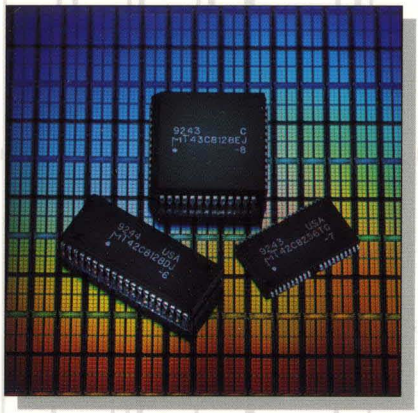
SPECIALTY DRAM

GRAPHICS/COMMUNICATIONS 1993 DATA BOOK



MICRON

SEMICONDUCTOR, INC.

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SPECIALTY DRAM DATA BOOK

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ABOUT THE COVER:

Front — A variety of features highlights Micron's Specialty DRAM product line, shown here against a circuitry backdrop rendered from a scanning electron microscope. Pictured are Micron's 1 Meg Triple-Port DRAM in a PLCC package (top), 1 Meg VRAM in an SOJ package (lower left) and 2 Meg VRAM in a TSOP package (lower right).

Back — Micron's Boise, Idaho, headquarters.

IMPORTANT NOTICE

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductors are appropriate for any application by a customer.

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MICRON'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRON SEMICONDUCTOR, INC., AS USED HEREIN:

A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

Dear Customer:

Micron Semiconductor, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly reliable memory components. Our corporate mission is:

"To be a world class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce. All components shipped have been through the AMBYX burn-in system.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And when you have a design or application question, you can get the answers you need from one of Micron's applications engineers. They can be reached at (208) 368-3950.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Semiconductor brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on customer expectations, including just in time (JIT) programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron entered the memory market in 1978, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and triple-port DRAM), and a variety of other memory products.

As we bring progressive memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple-Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. In 1990, Micron's Triple-Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Micron Triple-Port tradition. Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install, 88-pin IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and GEL-PAK®.

CUSTOM MANUFACTURING SERVICES

For complete project management of system-level products, Micron offers value-added services, including turnkey services covering all phases of production, and standard contract manufacturing services such as design, assembly, custom-kitted assembly and comprehensive quality testing or shipping. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with each Micron shipment. That's because we believe that quality must be internalized consistently at each level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX® intelligent burn-in and test system** gives Micron a unique edge in product reliability.

*See NOTE, page v.
**For more information on AMBYX®, see Section 6.

ABOUT THIS BOOK

CONTENT

The 1993 *Specialty DRAM Data Book* from Micron Semiconductor provides complete specifications on specialty and derivative products based on our DRAM production process. These products include our Wide DRAMs, Video RAMs (VRAMs), Triple-Port DRAMs, and VRAM Modules.

The *Specialty DRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes, currently available, include our *SRAM Data Book* and *DRAM Data Book.*

SECTION ORGANIZATION

Micron's 1993 *Specialty DRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The *Data Book* is organized into eight sections:

- **Sections 1–4:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 5:** Application/Technical notes.
- **Section 6:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX® intelligent burn-in and test system.*
- **Section 7:** Packaging information.
- **Section 8:** Sales information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the VRAM section begins with the 256K x 4 followed by 128K x 8 and all other x8 configurations in order of ascending depth. Next come the x16 products.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary or Production. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of each page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature for you.

For more information on Micron product literature, or to order additional copies of this publication, contact

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01-208-368-3410 (Intl.)

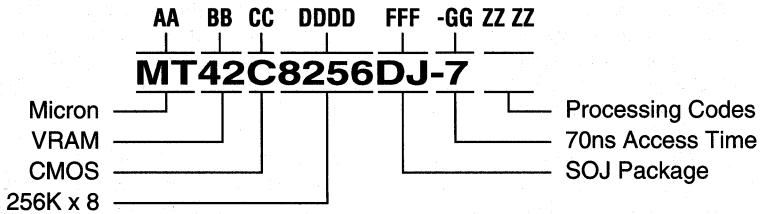
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Production)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. These specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Production) is a new addition since the data book's last printing.

NOTE: Micron's Data Books use acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
JEIDA—Japanese Electronics Industry Development Association
PCMCIA—Personal Computer Memory Card International Association

*Micron's detailed *Quality/Reliability Handbook* is available by calling (208) 368-3900.

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
VRAM 42
TPDRAM 43
SRAM 5
FIFO 52
Cache Data SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low-Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM ..... Width, Density
VRAM ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
CACHE ..... Density, Width
Latched SRAM ..... Total Bits, Width
FIFO ..... Width, Total Bits
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC
- DIP ..... Blank
- DIP (Wide Body) ..... W
- ZIP ..... Z
- LCC ..... EJ
- SOP/SOIC ..... SG

FFF – PACKAGE CODES (continued)

- QFP ..... LG
- TSOP (Type II) ..... TG
- TSOP (Reversed) ..... RG
- TSOP (Longer) ..... TL
- SOJ ..... DJ
- SOJ (Skinny) ..... SJ
- SOJ (Reversed) ..... DR
- SOJ (Longer) ..... DL

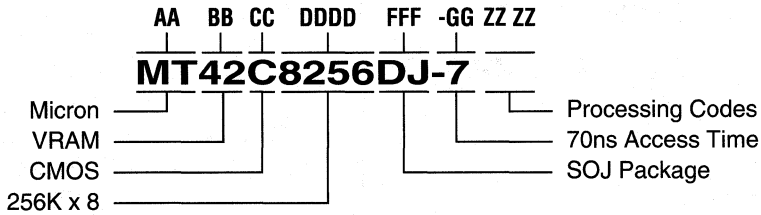
DIE
- Die ..... XDC
- Wafer ..... XWC
- Military Die ..... XD
- Military Wafer ..... XW

Ceramic
- DIP C
- DIP (Narrow Body) ..... CN
- DIP (Wide Body) ..... CW
- LCC ..... EC
- LCC (Narrow Body) ..... ECN
- LCC (Wide Body) ..... ECW
- SOP/SOIC ..... CG
- SOJ ..... DCJ
- PGA ..... CA
- FLAT PACK ..... F

GG – ACCESS TIME

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

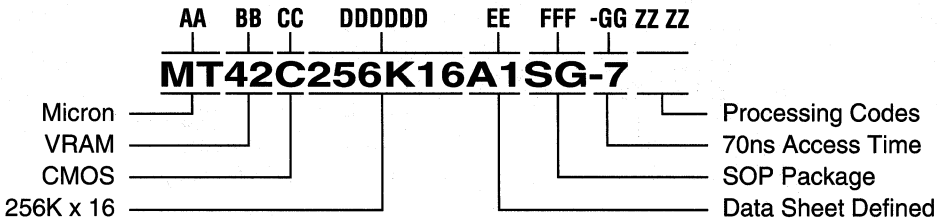
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (SELF REFRESH)	S
Low Voltage, Low Power (SELF REFRESH)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP

ZZ ZZ – PROCESSING CODES (continued)

Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



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Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
VRAM 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
FIFO 52
Latched SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG

FFF – PACKAGE CODES (continued)

QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Skinny) ..... SJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

DIE
Die ..... XDC
Wafer ..... XWC
Military Die ..... XD
Military Wafer ..... XW

CERAMIC
DIP C
DIP (Narrow Body) ..... CN
DIP (Wide Body) ..... CW
LCC (Narrow Body) ..... ECN
LCC ..... EC
LCC (Wide Body) ..... ECW
SOP/SOIC ..... CG
SOJ ..... DCJ
PGA ..... CA
FLAT PACK ..... F

GG – ACCESS TIME

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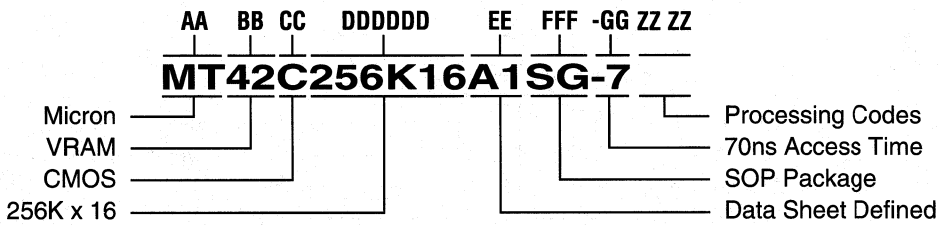
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-45 ..... 45ns
-50 (SRAM only) 50ns
-53 ..... 53ns
-55 ..... 55ns
-70 (SRAM only) 70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

Interim I
Low Voltage V
DRAMs
- Low Power (Extended Refresh) L
- Low Voltage, Low Power (Extended Refresh) VL
- Low Power (SELF REFRESH) ..... S
- Low Voltage, Low Power (SELF REFRESH) ..... VS

SRAMs
- Low Volt Data Retention L
- Low Power ..... P

ZZ ZZ – PROCESSING CODES (continued)

- Low Power, Low Volt Data Retention ..... LP
- Low Voltage, Low Power ..... VP
- Low Voltage, Low Volt Data Retention VL
- Low Voltage, Low Volt Data Retention, Low Power ..... VB

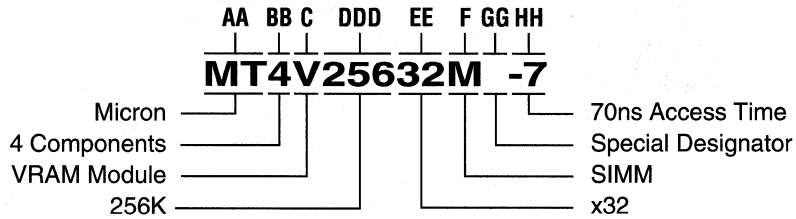
EPI Wafer ..... E
Commercial Testing
- 0°C to +70°C ..... Blank
- -40°C to +85°C ..... IT
- -40°C to +125°C ..... AT
- -55°C to +125°C ..... XT

MIL-STD-883C Testing
- -55°C to +125°C 883C
- -55°C to +110°C (DRAMs) 883C
- 0°C to +70°C M070

Special Processing
- Engineering Sample ..... ES
- Mechanical Sample ..... MS
- Sample Kit* ..... SK
- Tape-and-Reel* ..... TR
- Bar Code* ..... BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D
- VRAM V

DDD – DEPTH

EE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- Gold Plate ..... G
- ZIP ..... Z
- SIP ..... N
- SIMM ..... M

GG – SPECIAL DESIGNATOR
- Low Power L

HH – ACCESS TIME
- -10 ..... 10ns or 100ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns
- -45 ..... 45ns
- -6 ..... 60ns
- -7 ..... 70ns
- -8 ..... 80ns

WIDE DRAMS

FP ..... FAST-PAGE-MODE
LP ..... Low Power, Extended Refresh
DW ..... Dual WE
2KR ..... 2,048-Row Refresh
S ..... SELF REFRESH
EDO ..... Extended Data-Out
SC ..... STATIC-COLUMN
WPB ..... WRITE-PER-BIT
DC ..... Dual CAS
4KR ..... 4,096-Row Refresh
ASY ..... Asymmetrical Addressing

VRAMS

FP ..... FAST-PAGE-MODE
DW ..... Dual WE
DC ..... Dual CAS
EDO ..... Extended Data-Out

TRIPLE-PORT DRAMS

VRAM MODULES

APPLICATION/TECHNICAL NOTES

PRODUCT RELIABILITY

PACKAGE INFORMATION

SALES INFORMATION PAGE

NUMERICAL INDEX

Part #, MT:

NUMERICAL INDEX (continued)

Part #, MT:

WIDE DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number*	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins			Page
				Standby	Active	ZIP	SOJ	TSOP	
512K x 8	FP	MT4C8512	60, 70, 80	3mW	350mW	28	28	28	1-1
512K x 8	FP, WPB	MT4C8513	60, 70, 80	3mW	350mW	28	28	28	1-1
512K x 8	FP, LP	MT4C8512 L	60, 70, 80	1mW	350mW	28	28	28	1-17
512K x 8	FP, WPB, LP	MT4C8513 L	60, 70, 80	1mW	350mW	28	28	28	1-17
512K x 8	FP, LP, S	MT4C8512 S	70, 80	1mW	350mW	28	28	28	1-33
512K x 8	FP, WPB, LP, S	MT4C8513 S	70, 80	1mW	350mW	28	28	28	1-33
256K x 16	FP, DW	MT4C16256	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DC	MT4C16257	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DW, WPB	MT4C16258	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DC, WPB	MT4C16259	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DW, LP	MT4C16256 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DC, LP	MT4C16257 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DW, WPB, LP	MT4C16258 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DC, WPB, LP	MT4C16259 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DW, LP, S	MT4C16256 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DC, LP, S	MT4C16257 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DW, WPB, LP, S	MT4C16258 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DC, WPB, LP, S	MT4C16259 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	EDO, DC	MT4C16270	70, 80	3mW	500mW	40	40	40/44	1-119
256K x 16	EDO, DC, WPB	MT4C16271	70, 80	3mW	500mW	40	40	40/44	1-119
256K x 16	FP, ASY, DW	MT4C16260	70, 80	1mW	500mW	40	40	40/44	1-137
256K x 16	FP, WPB, ASY	MT4C16261	70, 80	1mW	500mW	40	40	40/44	1-137

FP = FAST-PAGE-MODE, SC = STATIC-COLUMN, LP = Low Power, Extended Refresh; WPB = WRITE-PER-BIT, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing
*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions

VRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins				Page
				Standby	Active	SOJ	SOP	TSOP	ZIP	
256K x 4	FP	MT42C4256	60, 70, 80	15mW	275mW	28	-	-	28	2-1
128K x 8	FP	MT42C8128	60, 70, 80	15mW	275mW	40	-	-	-	2-37
256K x 8	FP, DW	MT42C8254	70, 80	10mW	300mW	40	-	40/44	-	2-75
256K x 8	FP	MT42C8255	70, 80	10mW	300mW	40	-	40/44	-	2-107
256K x 8	FP, EDO	MT42C8256	60, 70, 80	10mW	300mW	40	-	40/44	-	2-139
256K x 8	FP	MT42C8257	60, 70, 80	10mW	300mW	40	-	40/44	-	2-181
256K x 16	FP, EDO, DW	MT42C256K16A1	60, 70, 80	TBD	TBD	-	64	70	-	2-221
256K x 16	FP, DW	MT42C256K16C1	60, 70, 80	TBD	TBD	-	64	70	-	2-265
256K x 16	FP, DC	MT42C256K16C2	60, 70, 80	TBD	TBD	-	64	70	-	2-267

FP = FAST-PAGE-MODE, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS

TRIPLE-PORT DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins				Page
				Standby	Active	SOJ	SOG	TSOP	PLCC	
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	3-1
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44	-	3-1
256K x 4	FP, BW, QSF pin	MT43C4257A	70, 80	15mW	500mW	40	-	40/44	-	3-3
256K x 4	FP, BW, SSF pin	MT43C4258A	70, 80	15mW	500mW	40	-	40/44	-	3-3
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	3-49
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	3-49
128K x 8	FP, BW, QSF pin	MT43C8128A	70, 80	15mW	550mW	-	-	-	52	3-51
128K x 8	FP, BW, SSF pin	MT43C8129A	70, 80	15mW	550mW	-	-	-	52	3-51
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW	-	64	-	-	3-97

FP = FAST-PAGE-MODE, BW = BLOCK WRITE

VRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins	Page
				Standby	Active	SIMM	
256K x 32	FP, BW	MT4V25632	70, 80	40mW	1,200mW	104	4-1

FP = FAST-PAGE-MODE, BW = BLOCK WRITE

APPLICATION/TECHNICAL NOTE PRODUCT SELECTION GUIDE

Technical Note	Title	Page
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TN-00-02	Tape-and-Reel Procedures	5-3
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AN-43-02	Use of TPDRAM for Smarter/Faster Network Applications	5-63

MICRON
SEMICONDUCTOR, INC.

WIDE DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number*	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins			Page
				Standby	Active	ZIP	SOJ	TSOP	
512K x 8	FP	MT4C8512	60, 70, 80	3mW	350mW	28	28	28	1-1
512K x 8	FP, WPB	MT4C8513	60, 70, 80	3mW	350mW	28	28	28	1-1
512K x 8	FP, LP	MT4C8512 L	60, 70, 80	1mW	350mW	28	28	28	1-17
512K x 8	FP, WPB, LP	MT4C8513 L	60, 70, 80	1mW	350mW	28	28	28	1-17
512K x 8	FP, LP, S	MT4C8512 S	70, 80	1mW	350mW	28	28	28	1-33
512K x 8	FP, WPB, LP, S	MT4C8513 S	70, 80	1mW	350mW	28	28	28	1-33
256K x 16	FP, DW	MT4C16256	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DC	MT4C16257	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DW, WPB	MT4C16258	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DC, WPB	MT4C16259	60, 70, 80	3mW	500mW	40	40	40/44	1-51
256K x 16	FP, DW, LP	MT4C16256 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DC, LP	MT4C16257 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DW, WPB, LP	MT4C16258 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DC, WPB, LP	MT4C16259 L	60, 70, 80	1mW	500mW	40	40	40/44	1-73
256K x 16	FP, DW, LP, S	MT4C16256 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DC, LP, S	MT4C16257 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DW, WPB, LP, S	MT4C16258 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	FP, DC, WPB, LP, S	MT4C16259 S	60, 70, 80	1mW	500mW	40	40	40/44	1-95
256K x 16	EDO, DC	MT4C16270	70, 80	3mW	500mW	40	40	40/44	1-119
256K x 16	EDO, DC, WPB	MT4C16271	70, 80	3mW	500mW	40	40	40/44	1-119
256K x 16	FP, ASY, DW	MT4C16260	70, 80	1mW	500mW	40	40	40/44	1-137
256K x 16	FP, WPB, ASY	MT4C16261	70, 80	1mW	500mW	40	40	40/44	1-137

FP = FAST-PAGE-MODE, SC = STATIC-COLUMN, LP = Low Power, Extended Refresh; WPB = WRITE-PER-BIT, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing
*(L)C means device is available in both 5V V_{CC} (MT4CXXXXX) and 3/3.3V V_{CC} (MT4LCXXXXX) versions

WIDE DRAM

512K x 8 DRAM

FAST-PAGE-MODE

FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: ten row-addresses, nine column-addresses
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)

OPTIONS

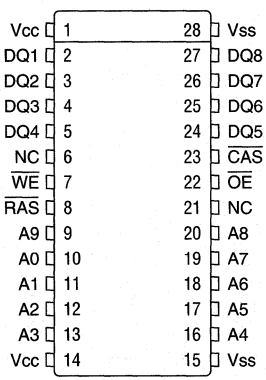
	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• MASKED WRITE	
Not available	8512
Available	8513
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (375 mil)	Z

- Part Number Example: MT4C8512TG-7

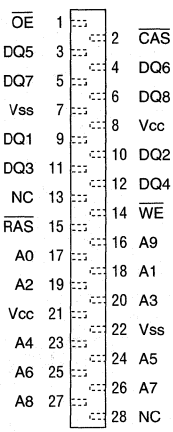
*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

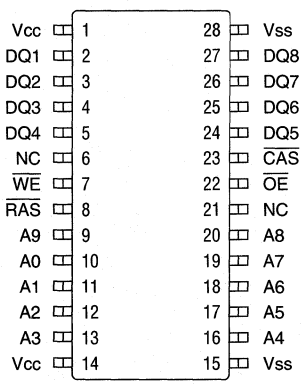
28-Pin SOJ (SDB-1)



28-Pin ZIP (SDA-1)



28-Pin TSOP (SDE-1)

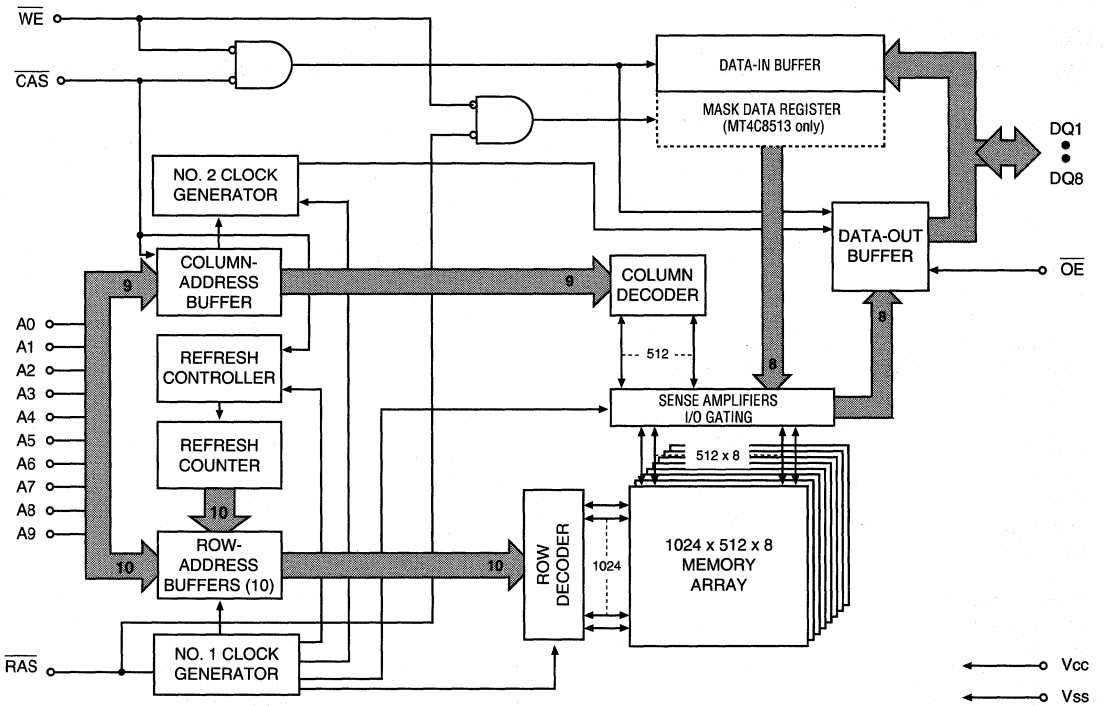


GENERAL DESCRIPTION

The MT4C8512/3 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 only).
23	2	$\overline{CAS}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
7	14	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C8513).
22	1	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	V_{CC}	Supply	Power Supply: +5V ±10%
15, 28	7, 22	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First, $\overline{RAS}$ is used to latch 10 bits (A0-A9) then, $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

MASKED WRITE ACCESS CYCLE (MT4C8513 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTANT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

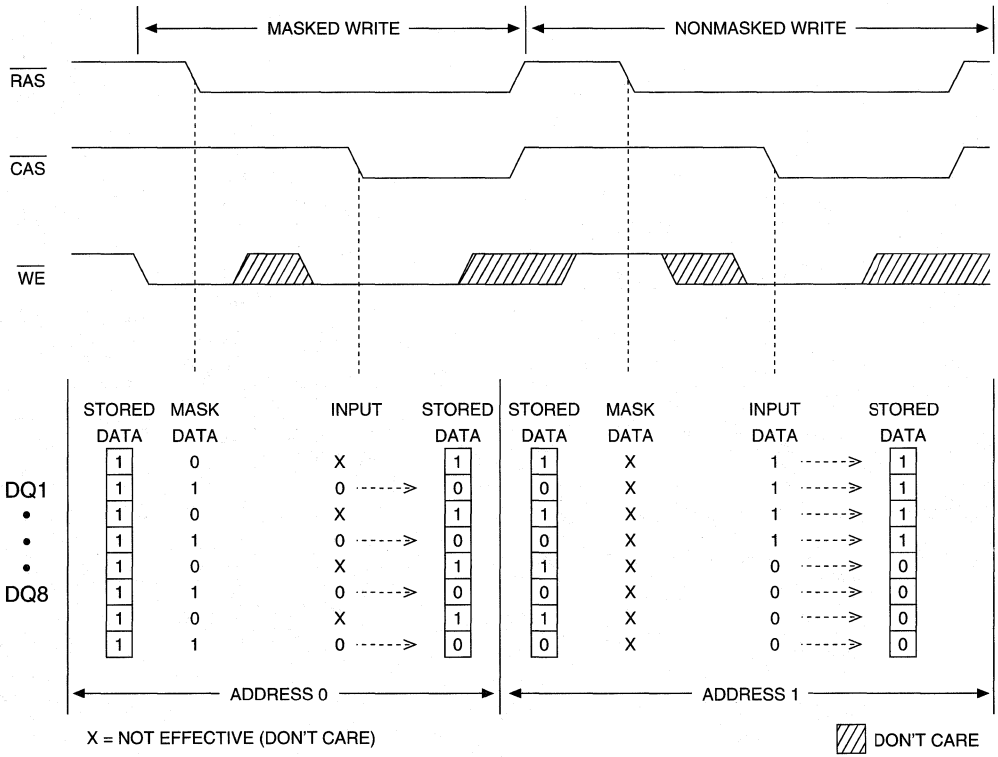


Figure 1
MT4C8513 MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided (MT4C8513 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6**	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	100	mA	3, 4, 30
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	80	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	100	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	90	mA	3

**60ns specifications may be limited to a V_{CC} range of ±5%.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable time	^tOE		15		20		20	ns	
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	31

*60ns specifications may be limited to a Vcc range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

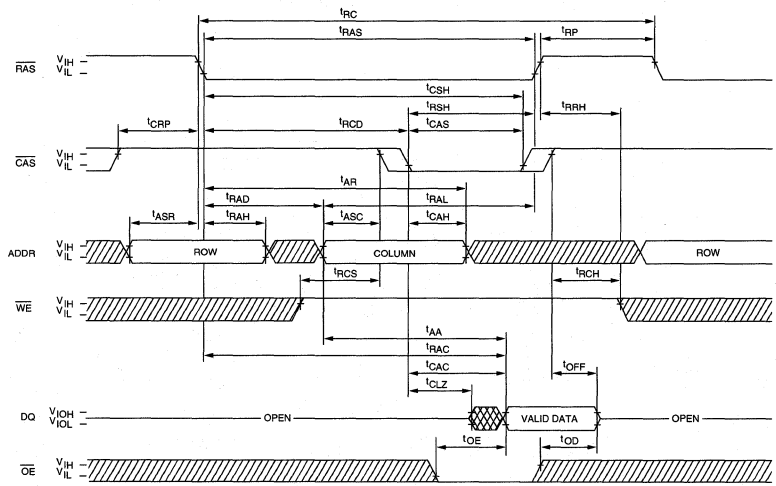
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 29, 31
Output disable time	^tOD	3	15	3	15	3	15	ns	29, 31
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26
$\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE	^tWRH	10		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

*60ns specifications may be limited to a Vcc range of ±5%.

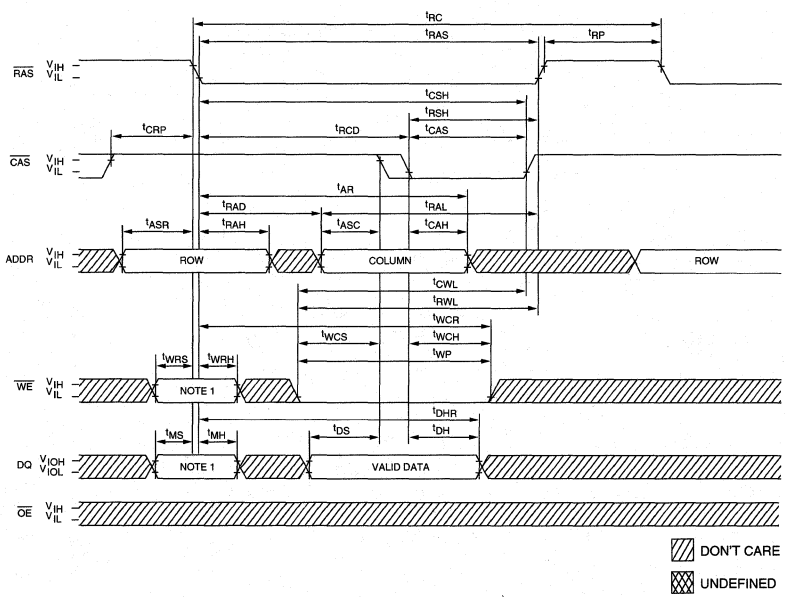
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit conzdition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
31. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE

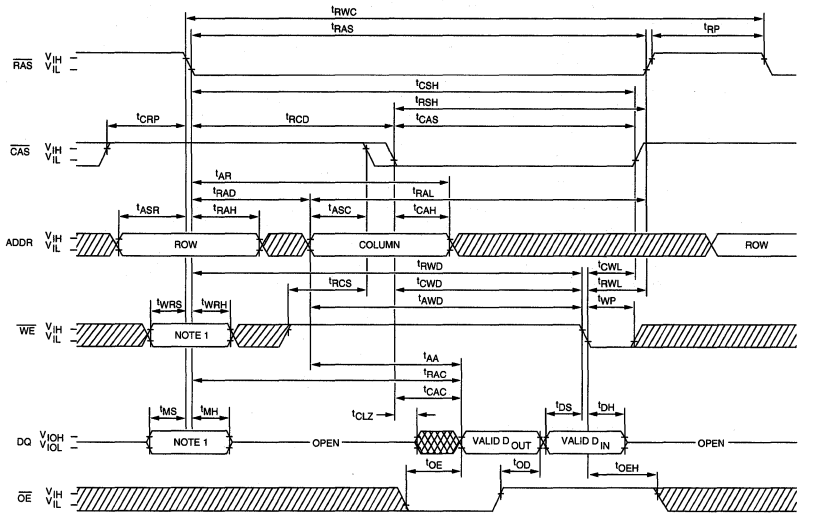


EARLY-WRITE CYCLE

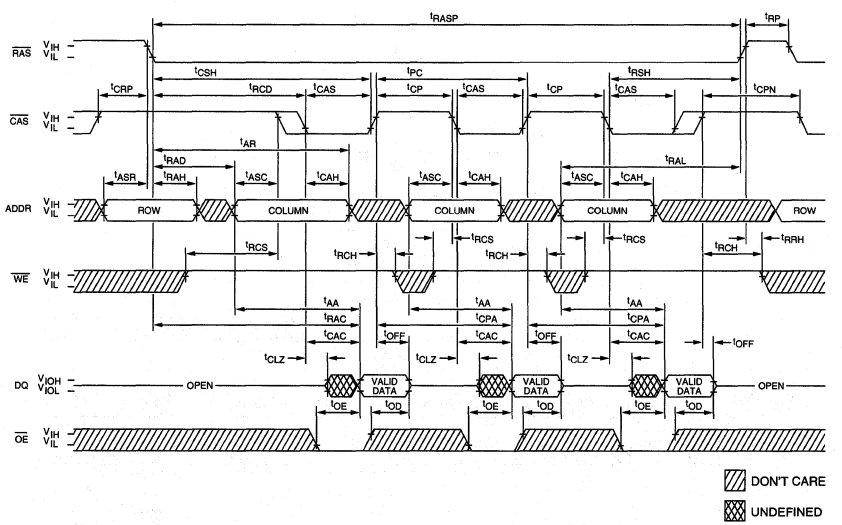


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

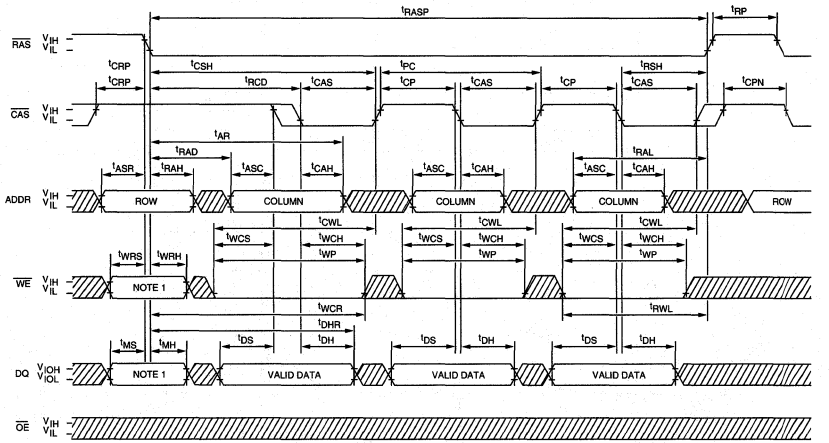


FAST-PAGE-MODE READ CYCLE

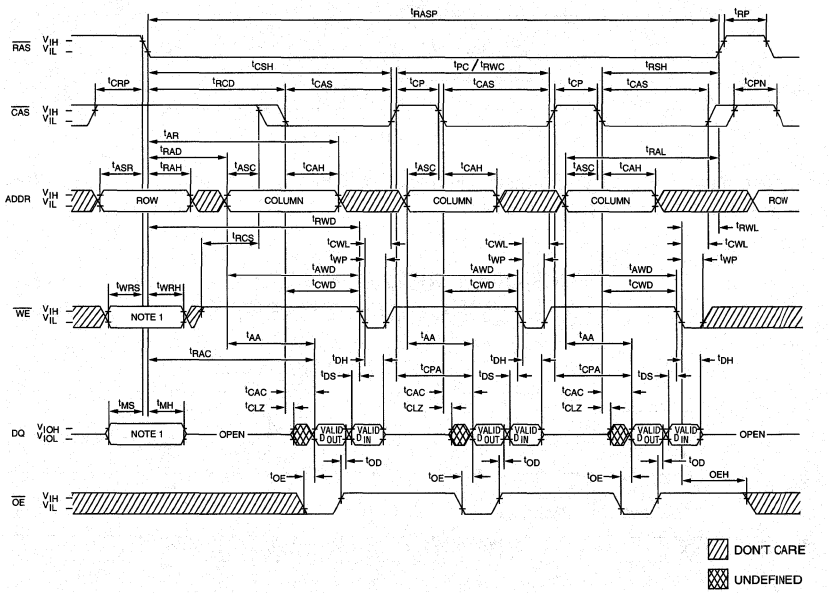


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

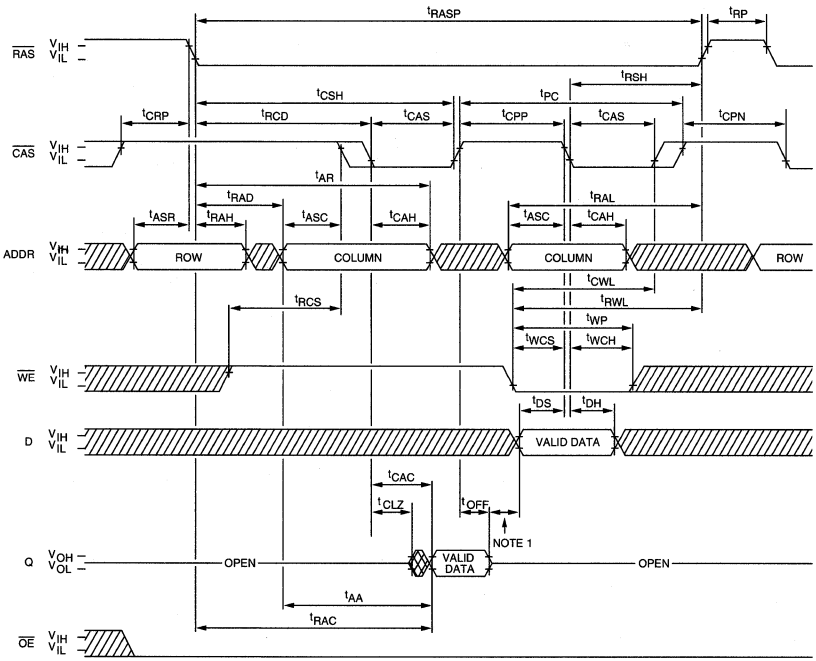


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



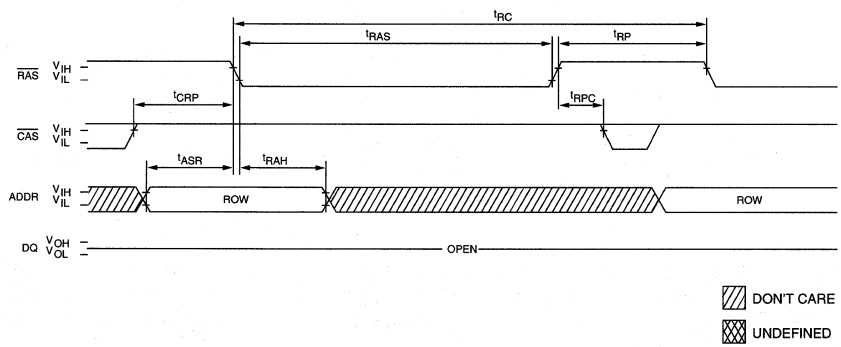
NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

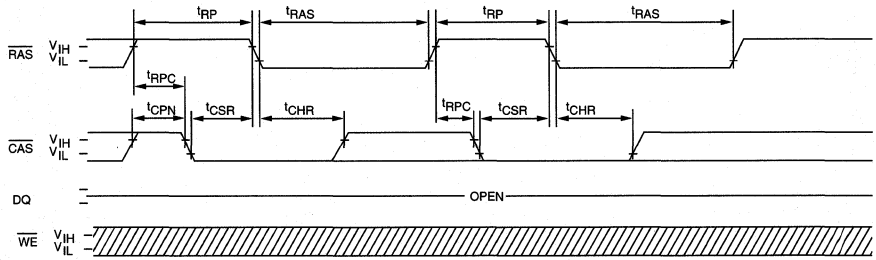


NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

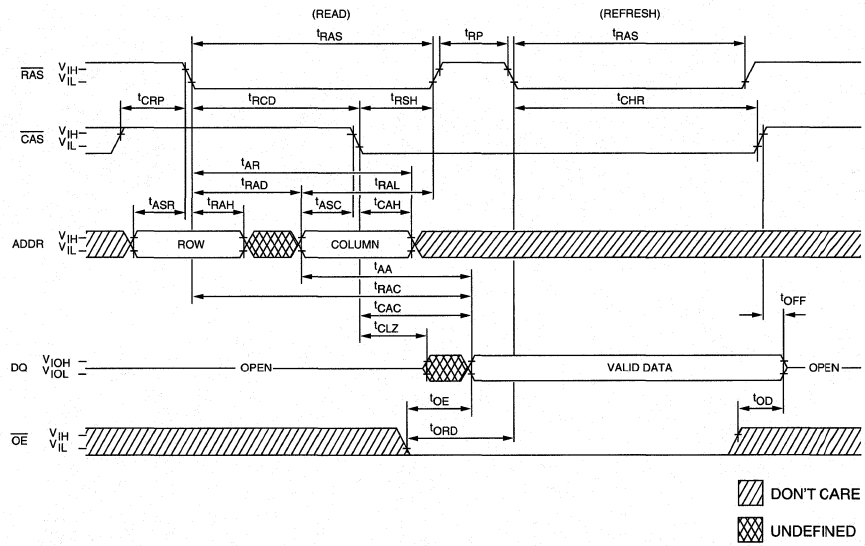
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

512K x 8 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: ten row-addresses, nine column-addresses
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)
- 1,024-cycle refresh distributed accross 128ms
- Low-power, 1mW standby; 350mW active, typical

OPTIONS

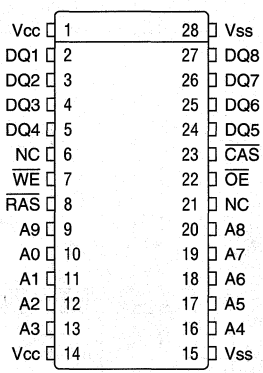
	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• MASKED WRITE	
Not available	8512 L
Available	8513 L
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (375 mil)	Z

• Part Number Example: MT4C8512DJ-7 L

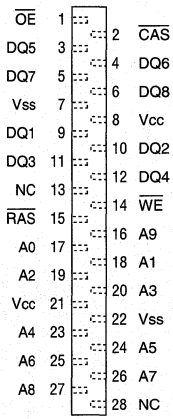
*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

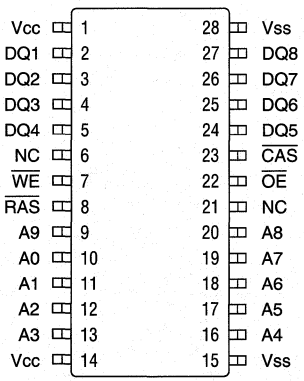
28-Pin SOJ (SDB-1)



28-Pin ZIP (SDA-1)



28-Pin TSOP (SDE-1)

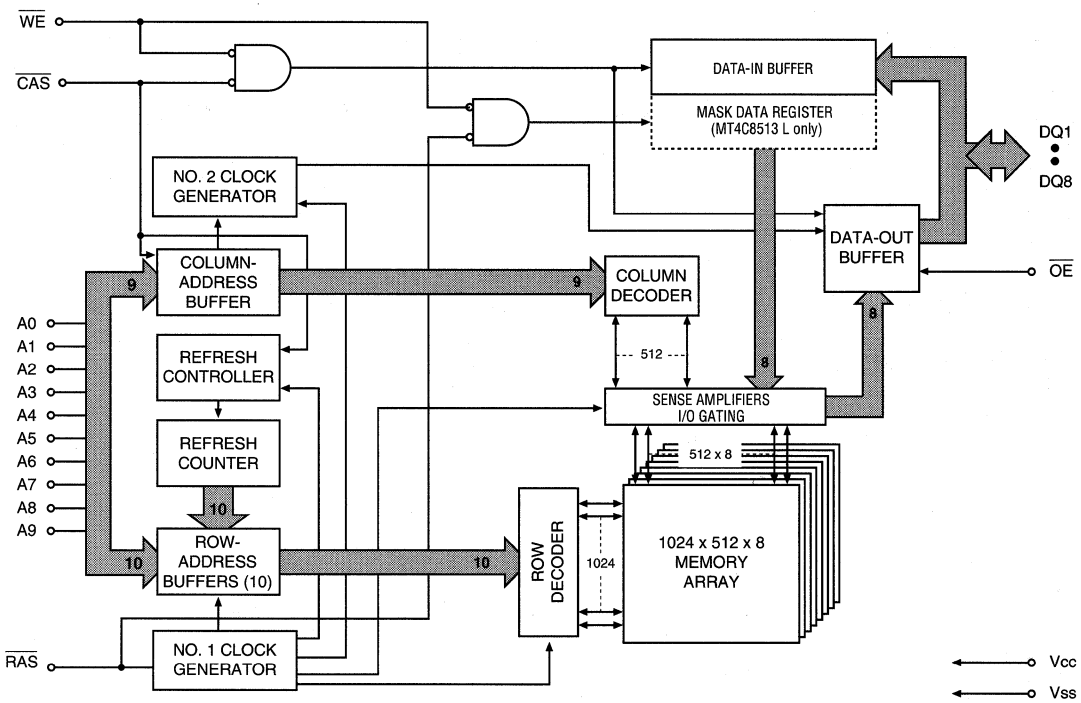


GENERAL DESCRIPTION

The MT4C8512/3 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 L has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 L only).
23	2	$\overline{CAS}$	Input	Column-address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
7	14	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C8513 L).
22	1	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	Vcc	Supply	Power Supply: +5V ±10%
15, 28	7, 22	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 10 bits (A0-A9) then, $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU MODE is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

MASKED WRITE ACCESS CYCLE (MT4C8513 L ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTANT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

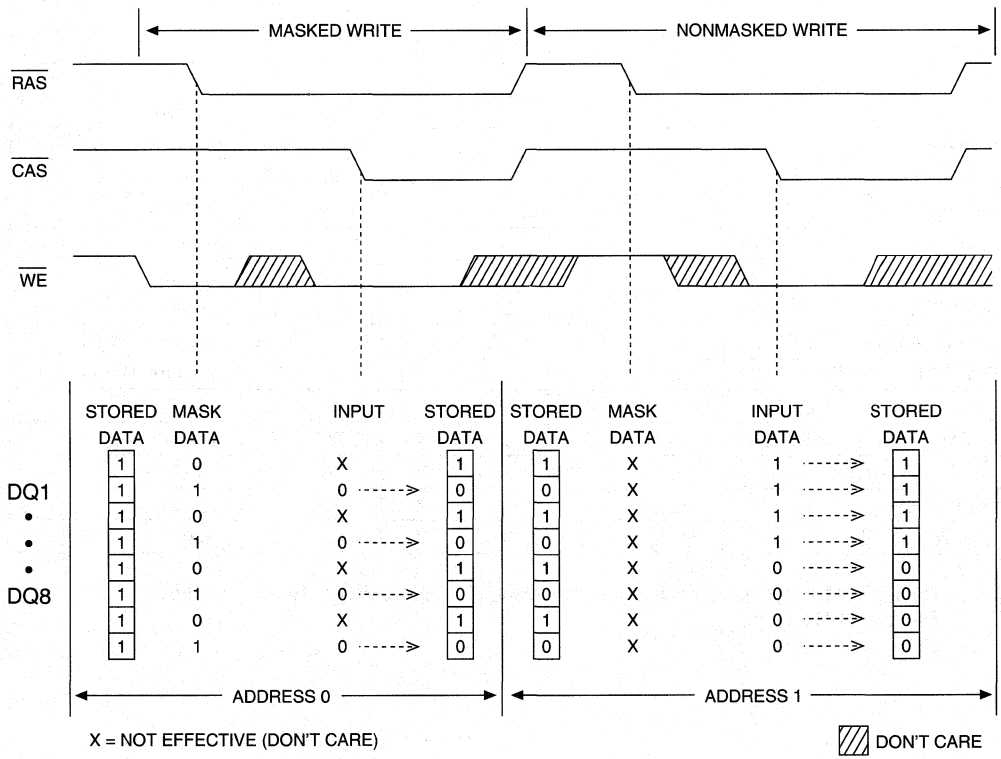


Figure 1
MT4C8513 L MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	High-Z	
BBU REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided (MT4C8513 L only). Refer to Figure 1.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6**	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	100	mA	3, 4, 31
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	80	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	100	mA	3, 31
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	90	mA	3
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 5, 30

**60ns specifications may be limited to a V_{CC} range of ±5%.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable time	^tOE		15		20		20	ns	
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	32

*60ns specifications may be limited to a Vcc range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

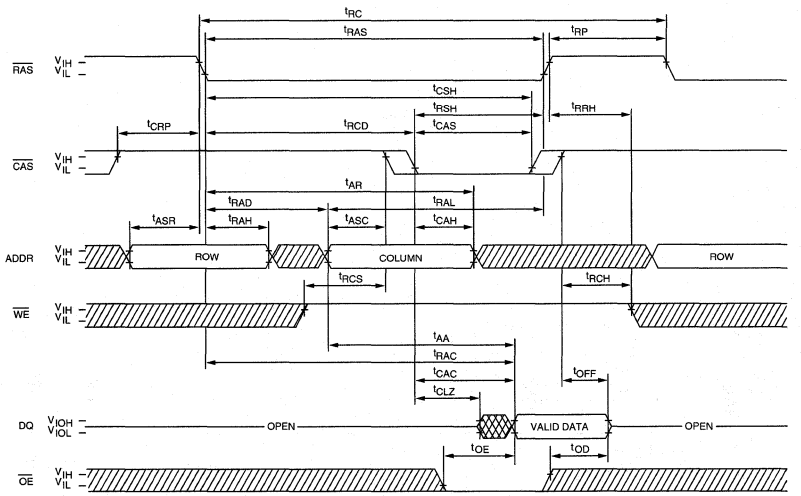
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 29, 32
Output disable time	^tOD	3	15	3	15	3	15	ns	29, 32
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26
$\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE	^tWRH	10		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

*60ns specifications may be limited to a Vcc range of ±5%.

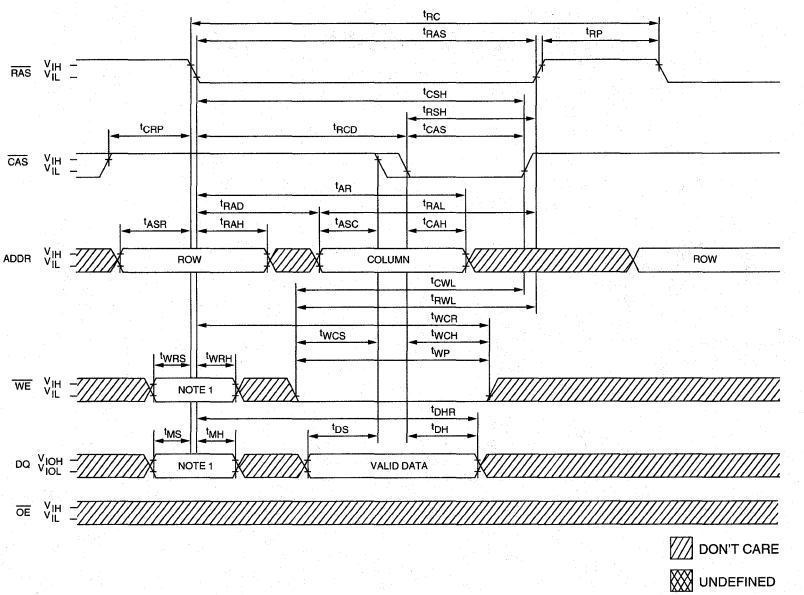
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 L only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
31. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
32. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE

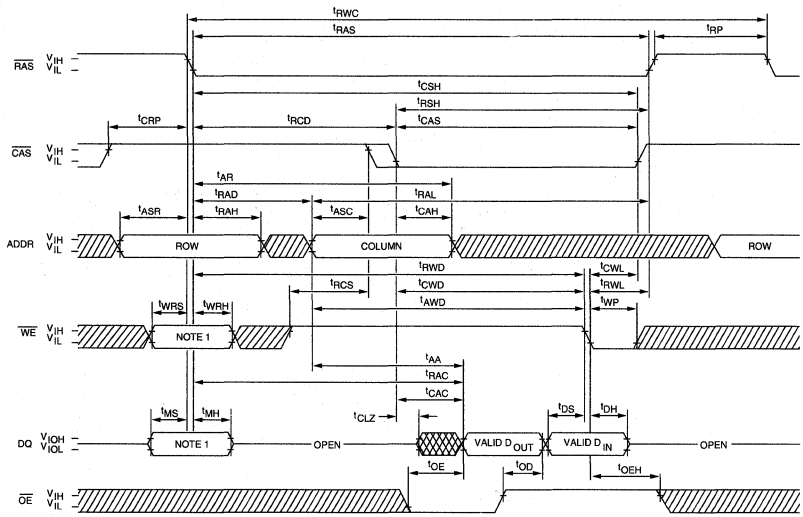


EARLY-WRITE CYCLE

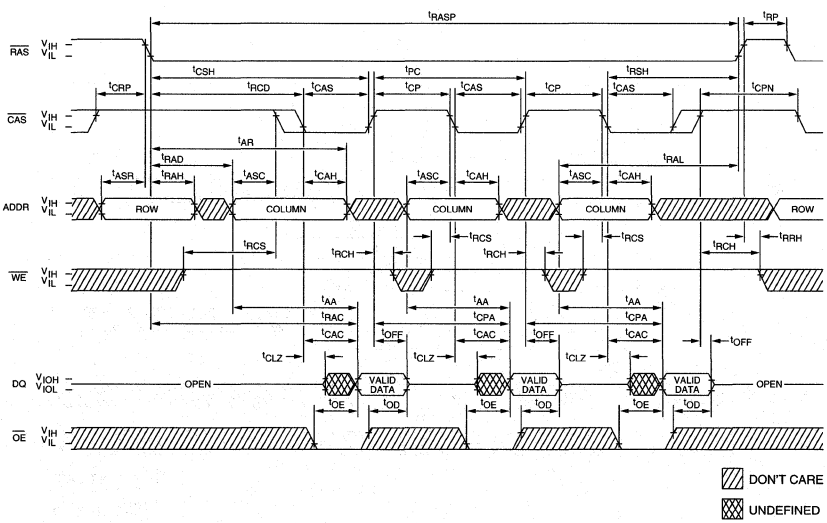


NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

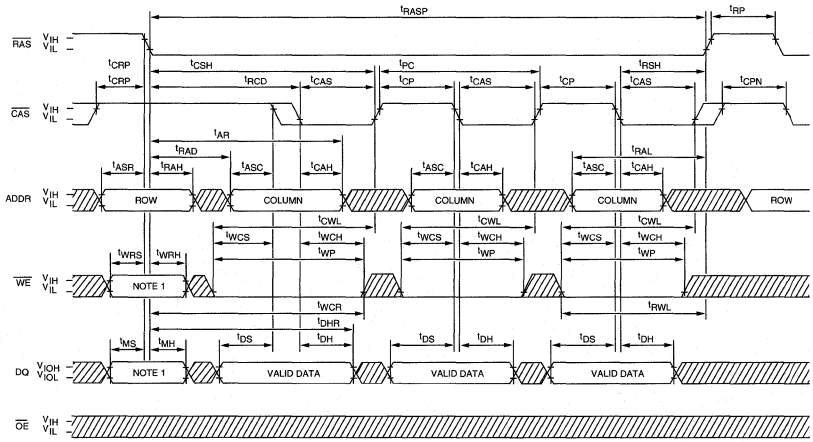


FAST-PAGE-MODE READ CYCLE

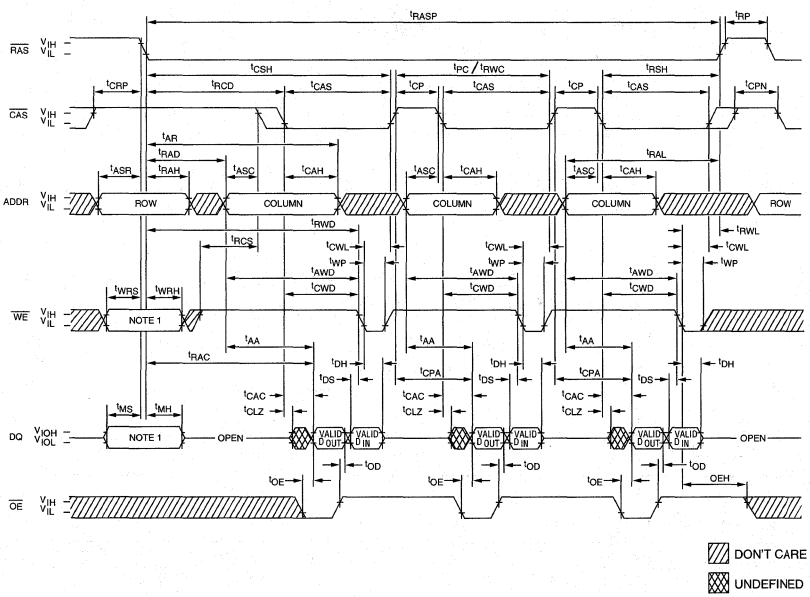


NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

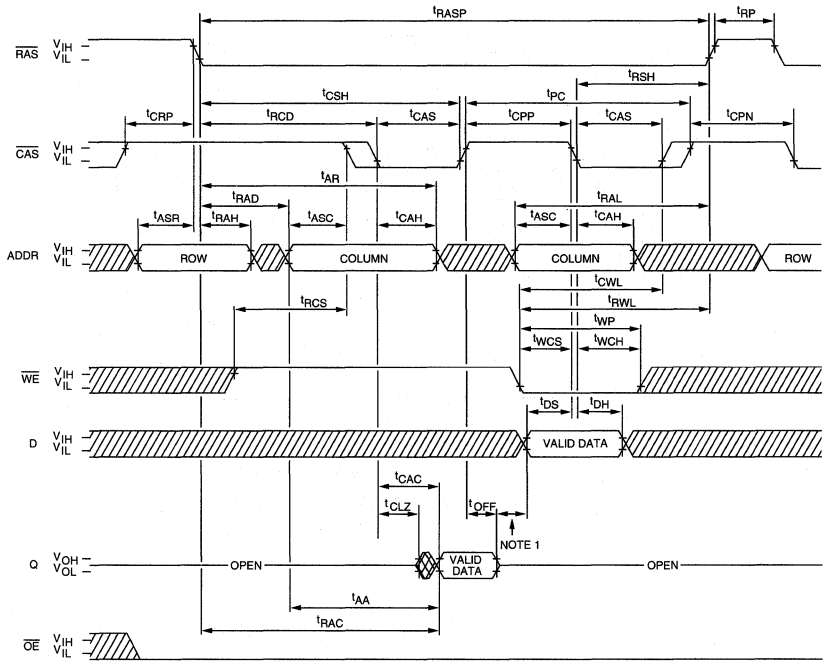


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



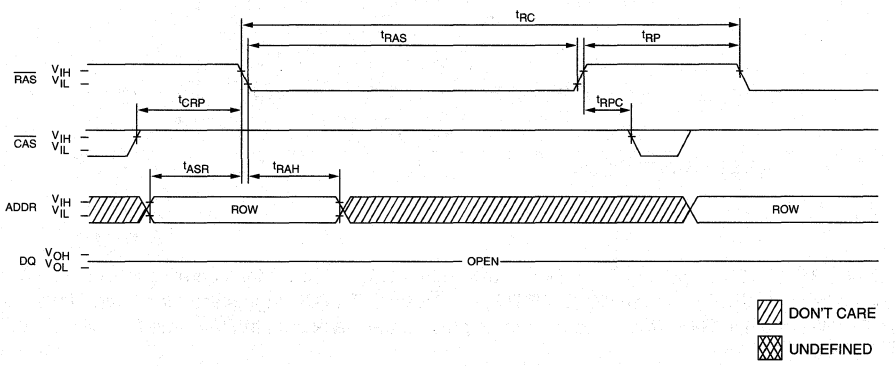
NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

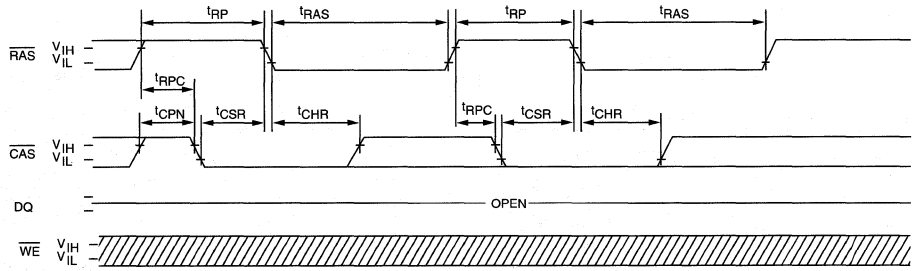


NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

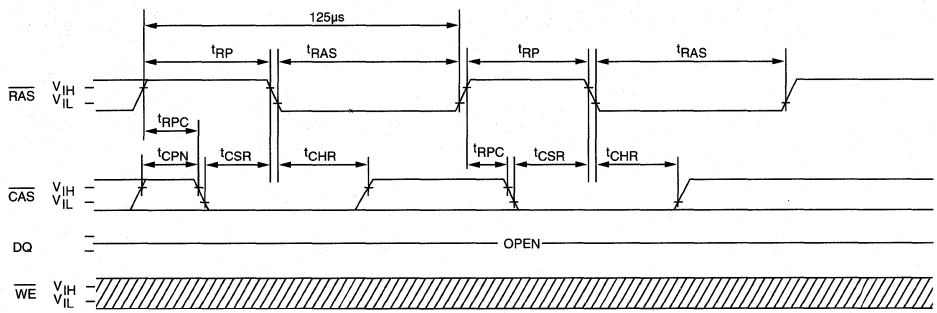
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)



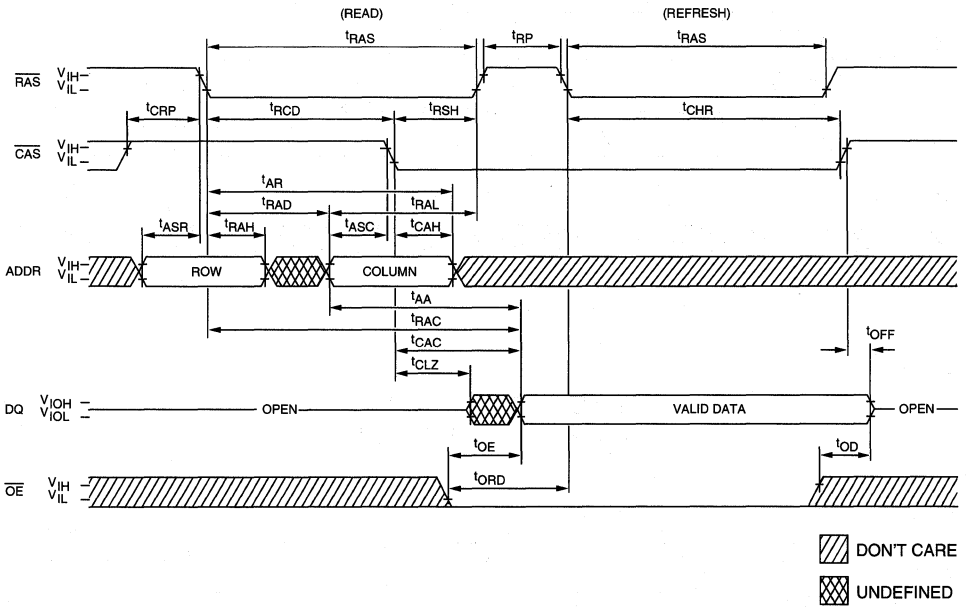
BBU REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

512K x 8 DRAM

EXTENDED REFRESH
SELF REFRESH

FEATURES

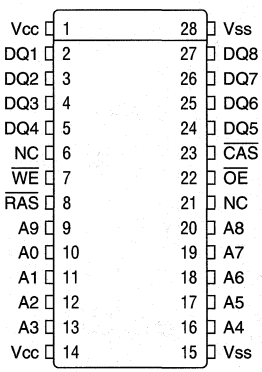
- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: ten row-addresses, nine column-addresses
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN, BATTERY BACKUP (BBU), and SELF
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 S only)
- 1,024-cycle refresh distributed accross 128ms
- Low-power, 1mW standby; 350mW active, typical

OPTIONS — MARKING

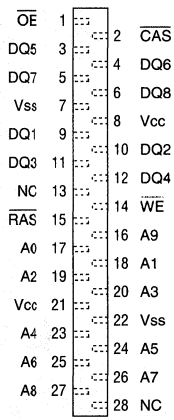
- Timing
  - 70ns access — -7
  - 80ns access — -8
- MASKED WRITE
  - Not available — 8512 S
  - Available — 8513 S
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (375 mil) — Z
- Part Number Example: MT4C8512DJ-7 S

PIN ASSIGNMENT (Top View)

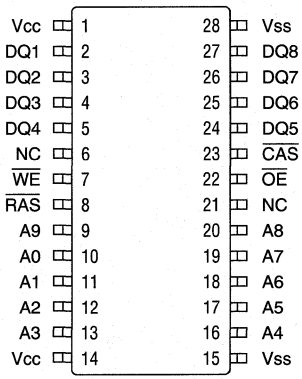
28-Pin SOJ (SDB-1)



28-Pin ZIP (SDA-1)



28-Pin TSOP (SDE-1)

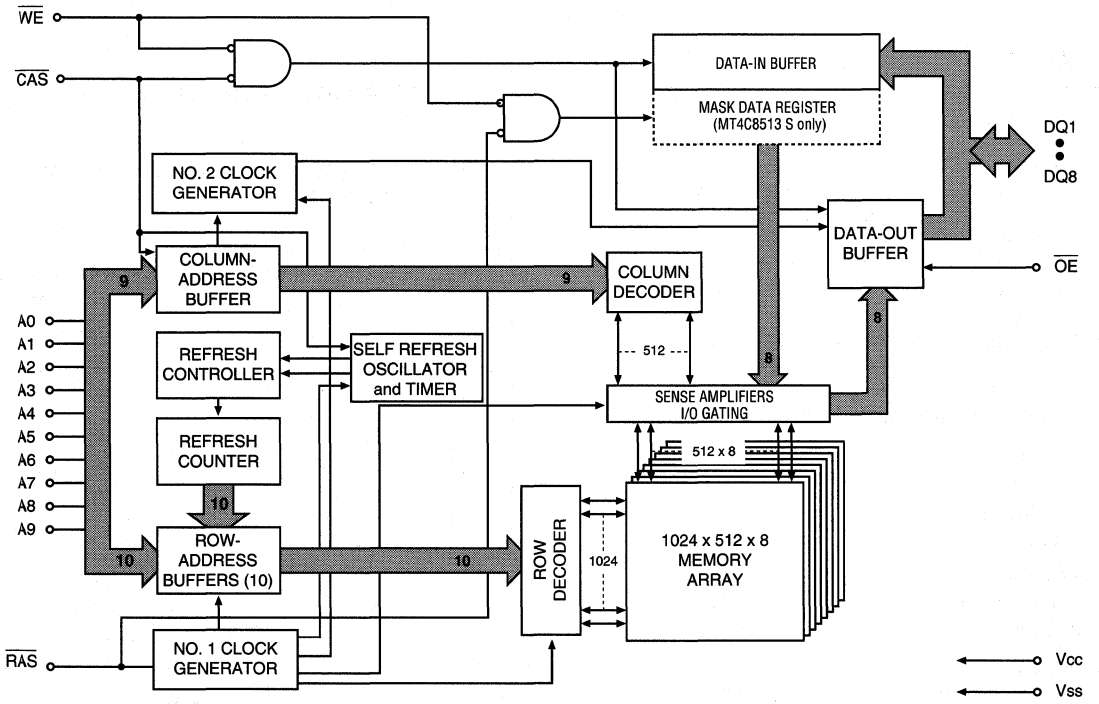


GENERAL DESCRIPTION

The MT4C8512/3 S are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 S has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 S only).
23	2	$\overline{CAS}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
7	14	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C8513 S).
22	1	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	V_{CC}	Supply	Power Supply: +5V ±10%
15, 28	7, 22	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First, $\overline{RAS}$ is used to latch 10 bits (A0-A9) then, $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during sleep mode. Thus, an external clock is not required, which provides additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (^{t}RASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for 600µs (^{t}CHD), $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care." $\overline{CAS}$ is a "don't care" until ^{t}CHS, at which time $\overline{CAS}$ must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically 200ns (^{t}RPS). Once the SELF REFRESH mode has been terminated, accesses to the DRAM can begin immediately, as long as the system uses distributed CBR refresh as the standard refresh. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three external refresh rate periods. The external refresh rate is typically 125µs per row-address. This immediate access is possible because Micron employs a distributed CBR SELF REFRESH scheme internally.

The alternative approach when exiting SELF REFRESH mode is to perform a refresh of all rows within the time of the external refresh rate prior to active use of the DRAM. This burst must be done if anything other than distributed CBR refresh is used as the standard refresh. Once this burst has been completed, the DRAM may be used in the functional mode with a burst or distributed refresh, such as CBR or $\overline{RAS}$ only.

Micron's devices allow you to access the DRAM as soon as SELF REFRESH is exited, while other maufacturers' devices may require a full burst when exiting, regardless of the type of refresh used. To prevent possible compatibility problems, you may want to design the controller to perform the burst when exiting SELF REFRESH.

MASKED WRITE ACCESS CYCLE (MT4C8513 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data

will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 S MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

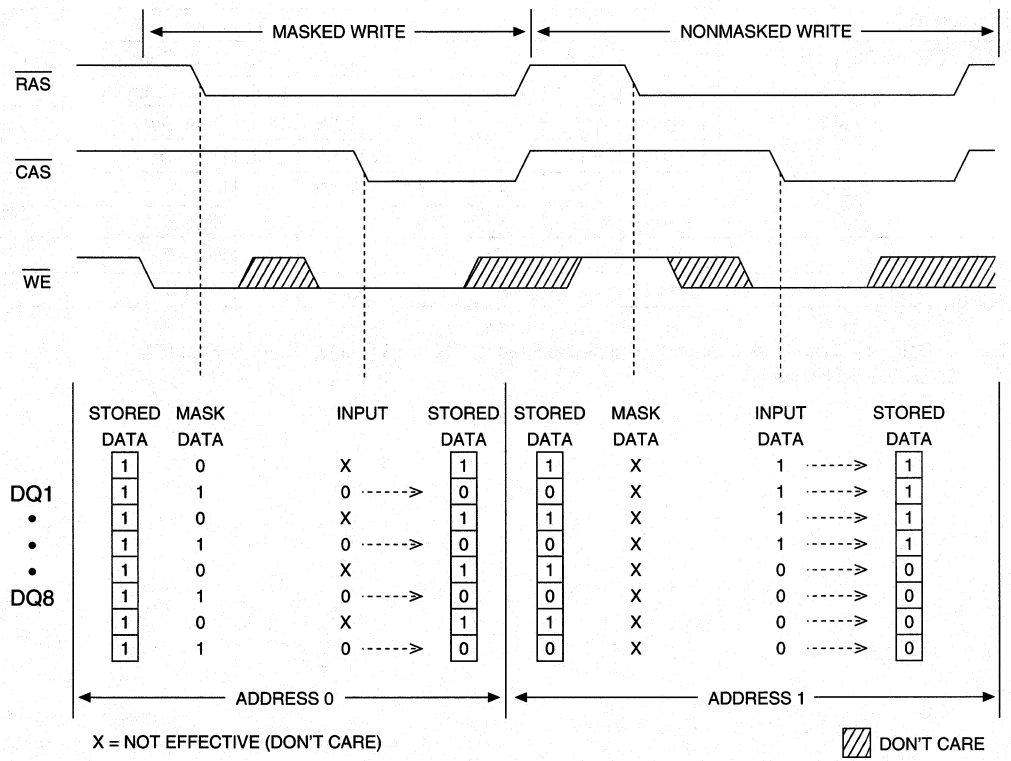


Figure 1
MT4C8513 S MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	High-Z	
BBU REFRESH		H→L	L	X	X	X	X	High-Z	
SELF REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided (MT4C8513 S only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	**SYMBOL**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	mA	3, 4, 31
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	mA	3, 31
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	100	90	mA	3
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	µA	3, 5, 30
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A8 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	400	400	µA	5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		ns	
READ-WRITE cycle time	t_{RWC}	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20	ns	15
Output Enable time	t_{OE}		20		20	ns	
Access time from column-address	t_{AA}		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		ns	16
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	t_{CP}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Row-address hold time	t_{RAH}	10		10		ns	
$\overline{RAS}$ to column-address delay time	t_{RAD}	15	35	15	40	ns	18
Column-address setup time	t_{ASC}	0		0		ns	
Column-address hold time	t_{CAH}	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		ns	
Column-address to $\overline{RAS}$ lead time	t_{RAL}	35		40		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	ns	20, 29, 33
Output disable time	^tOD	3	15	3	15	ns	29, 33
Write command setup time	^tWCS	0		0		ns	21, 26
Write command hold time	^tWCH	10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	26
Write command pulse width	^tWP	10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	26
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		ns	26
$\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE)	^tWRH	15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		us	32
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	150		150		ns	32
$\overline{CAS}$ hold time during SELF REFRESH cycle	^tCHS	-70		-70		ns	32
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	600		600		us	29

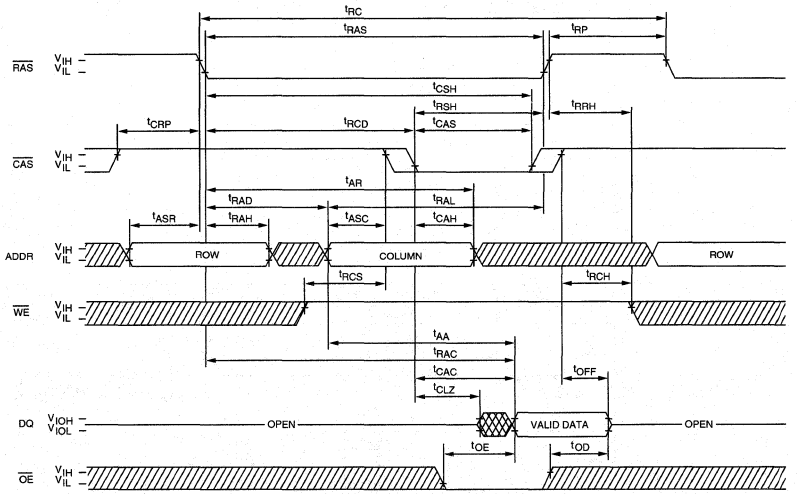
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

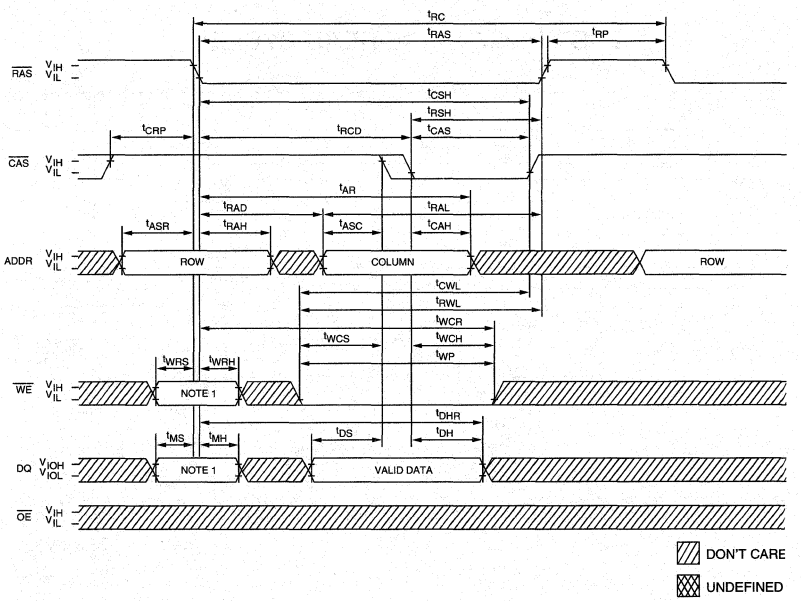
NOTES (continued)

30. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during BBU cycle.
31. Column-address changed once while $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
32. When exiting the SELF REFRESH mode, one CBR REFRESH must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distibuted CBR REFRESH is used in the active mode.
33. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE

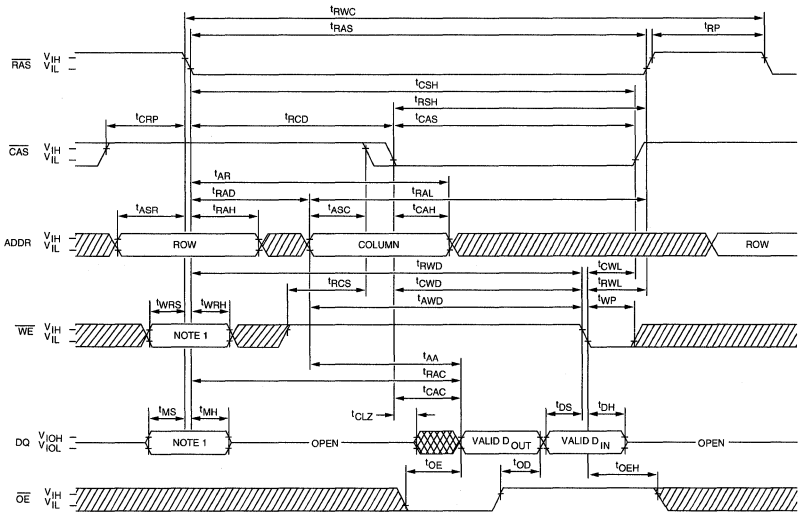


EARLY-WRITE CYCLE

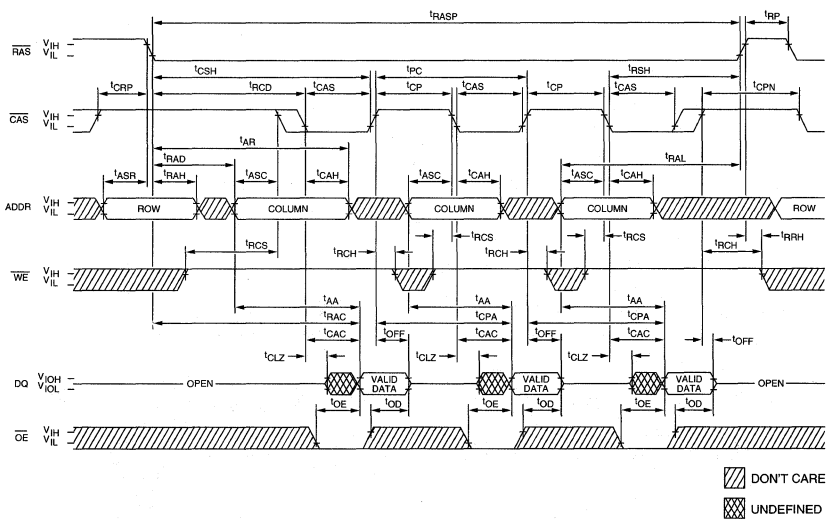


NOTE: 1. Applies to MT4C8513 S only; $\overline{WE}$ and DQ inputs on MT4C8512 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

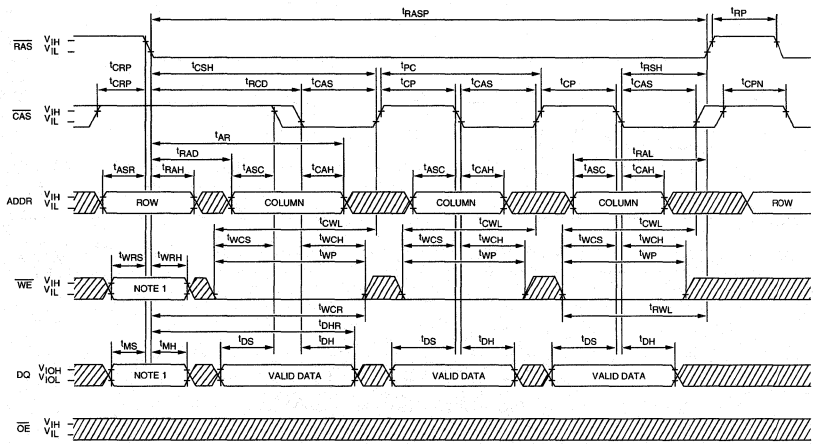


FAST-PAGE-MODE READ CYCLE

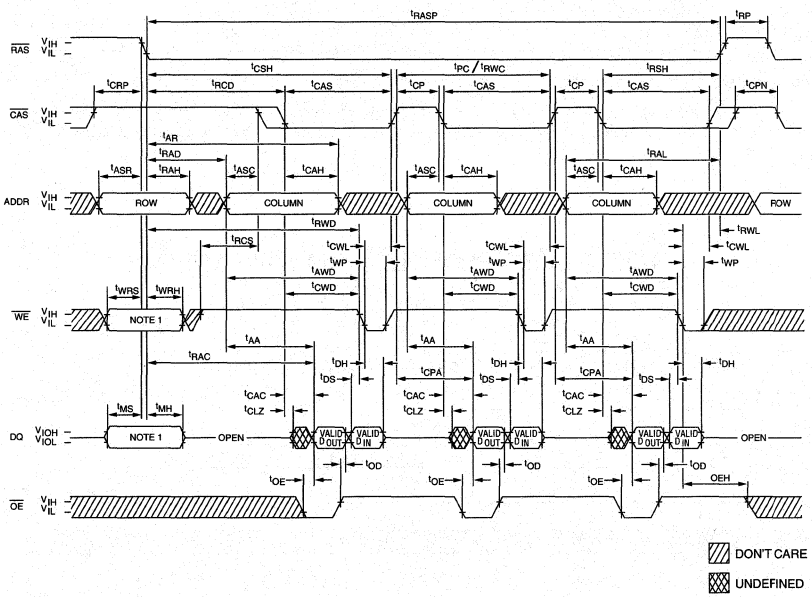


NOTE: 1. Applies to MT4C8513 S only; $\overline{WE}$ and DQ inputs on MT4C8512 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

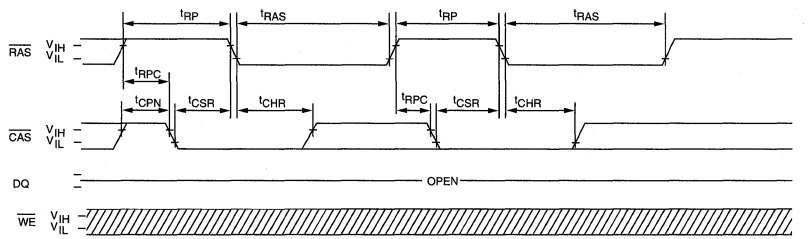


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

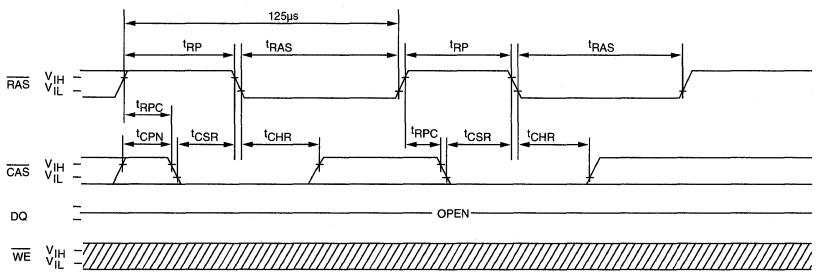


NOTE: 1. Applies to MT4C8513S only; $\overline{WE}$ and DQ inputs on MT4C8512 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

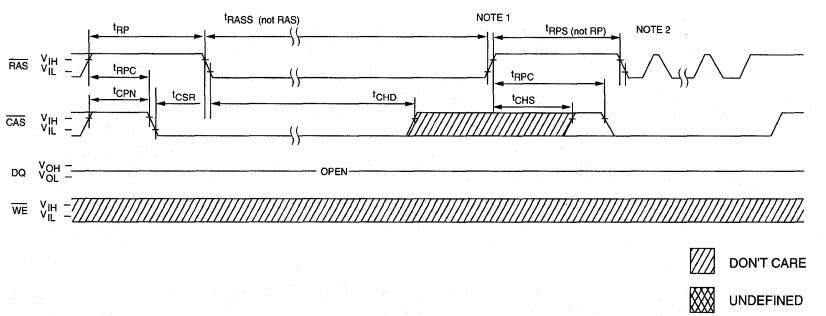
CBR REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)



BBU REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)

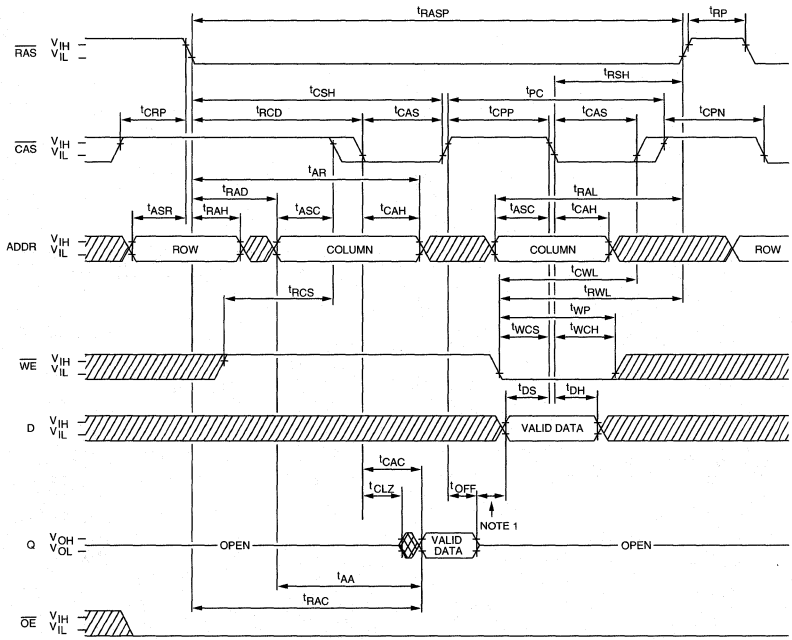


SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A9; $\overline{OE}$ = DON'T CARE)



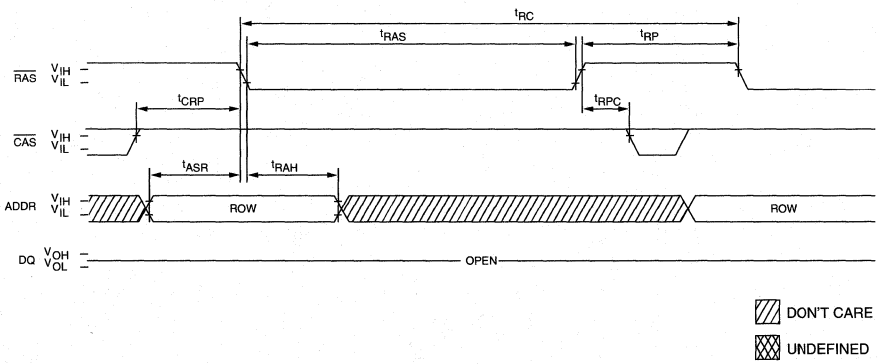
NOTE: 1. Once tRASS (MIN) is met, and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisified, a complete burst of all rows should be executed.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

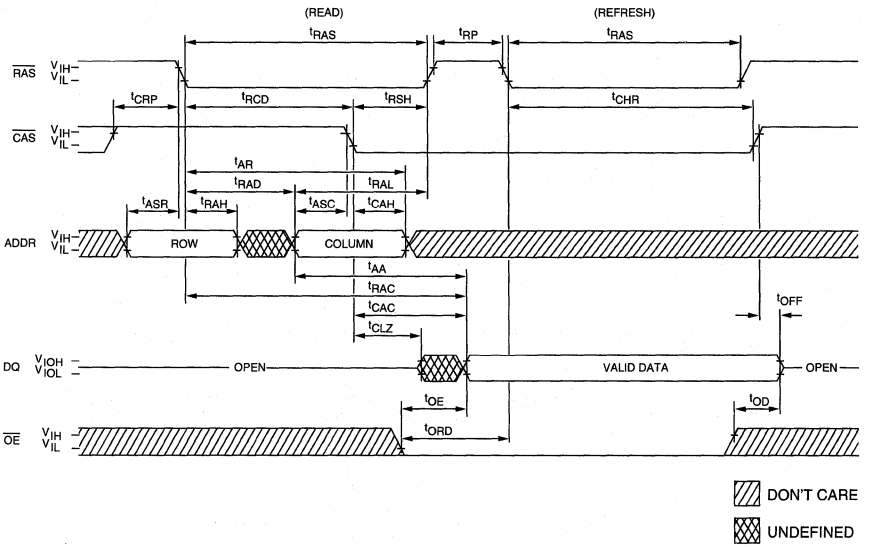


NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

256K x 16 DRAM

FAST-PAGE-MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 only)

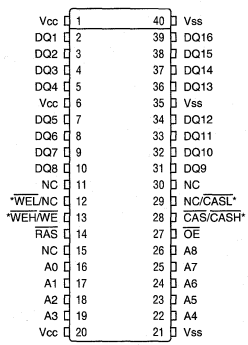
OPTIONS — MARKING

- Timing
  - 60ns access — -6*
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via $\overline{WE}$ (nonmaskable) — 16256
  - BYTE or WORD via $\overline{CAS}$ (nonmaskable) — 16257
  - BYTE or WORD via $\overline{WE}$ (maskable) — 16258
  - BYTE or WORD via $\overline{CAS}$ (maskable) — 16259
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z
- Part Number Example: MT4C16256DJ-7

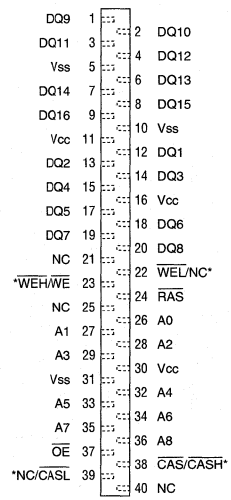
*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

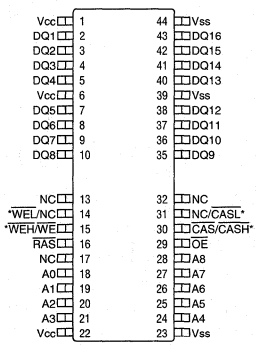
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-2)



40-Pin TSOP (SDE-2)



*MT4C16256/8 / MT4C16257/9

GENERAL DESCRIPTION

The MT4C16256/7/8/9 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 and MT4C16258 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 and MT4C16259 have both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The MT4C16258 and MT4C16259 are also able to perform WRITE-PER-BIT accesses.

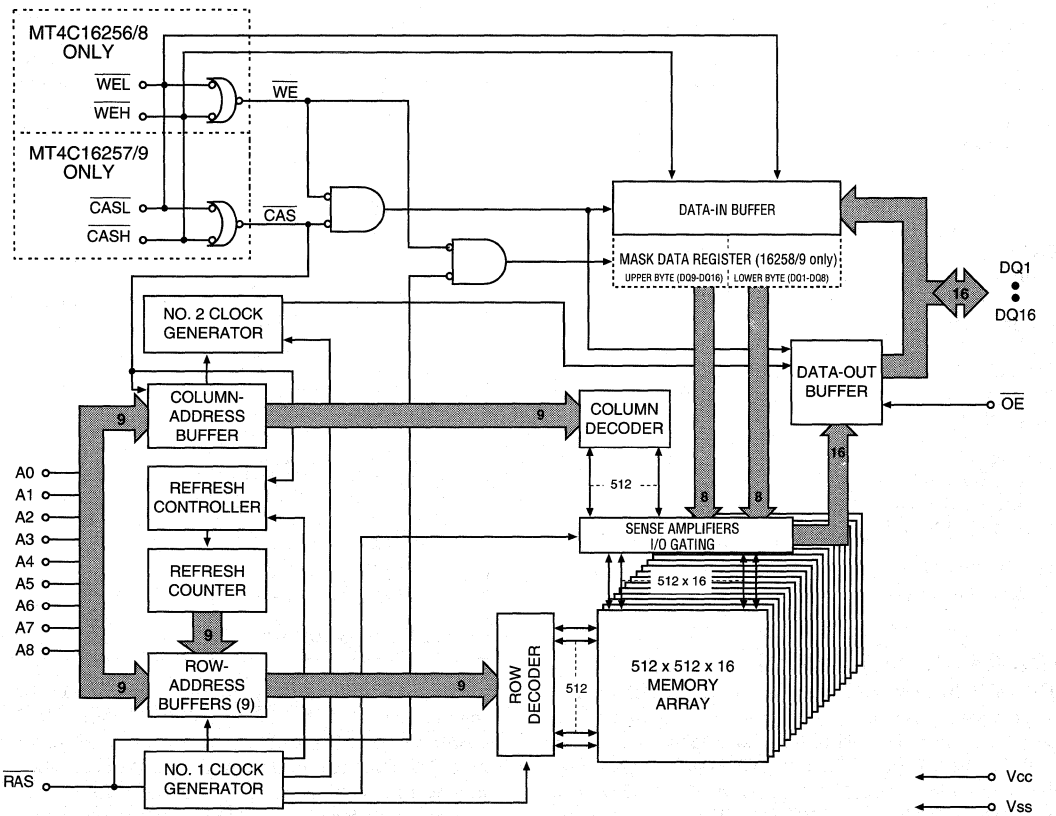
The MT4C16256 and MT4C16257 function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C16256 and $\overline{CASL}$ and $\overline{CASH}$ on MT4C16257 control the selection of byte WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C16256 $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257.

The MT4C16258 and MT4C16259 function in the same manner as MT4C16256 and MT4C16257, respectively; they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C16258 and MT4C16259 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 and MT4C16259 only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column-Address Strobe: $\overline{CAS}$ (MT4C16256/8) is used to latch-in the 9 column-address bits and enable the DRAM output buffers and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column-Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{WE}$ (MT4C16257/9) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C16256/8) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9) controls DQ1 through DQ16inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 also use $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column-Address Strobe Lower Byte: $\overline{CASL}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8). The MT4C16257/9 allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C16256 and MT4C16258 each have one $\overline{CAS}$ control while the MT4C16257 and MT4C16259 have two, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 and MT4C16259 $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 and MT4C16259 both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 or MT4C16259 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the $\overline{WE}$ on the MT4C16256 or MT4C16258. The MT4C16256 and MT4C16258 $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 and MT4C16258) or $\overline{WE}$ (MT4C16257 and MT4C16259).

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256, MT4C16257, MT4C16258 and MT4C16259 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 ONLY)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 and MT4C16257 do not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated , even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 MASKED WRITE operation and Figure 5 illustrates the MT4C16259 MASKED WRITE operation.

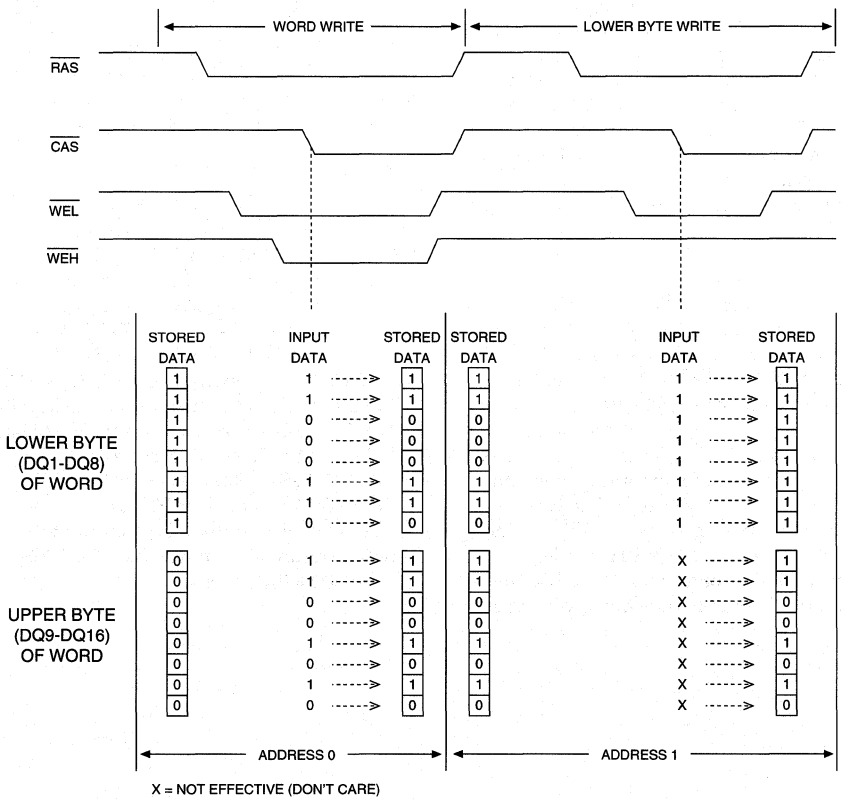


Figure 1
MT4C16256/8 WORD AND BYTE WRITE EXAMPLE

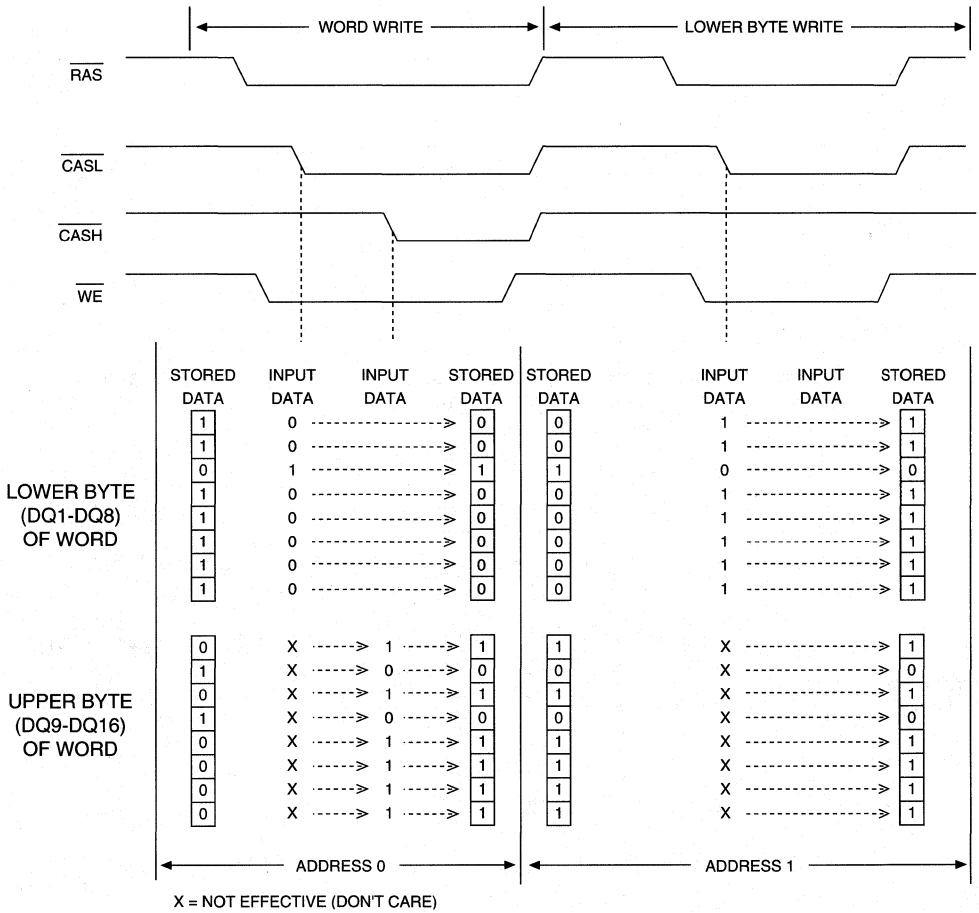


Figure 2
MT4C16257/9 WORD AND BYTE WRITE EXAMPLE

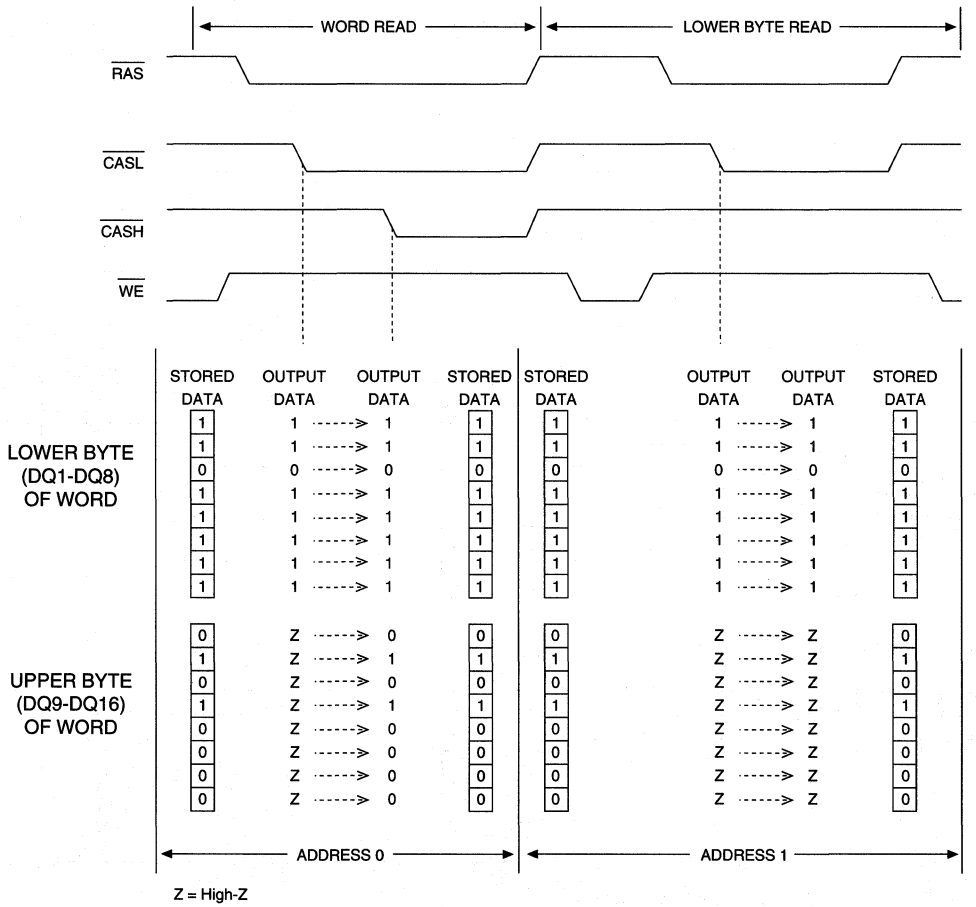


Figure 3
MT4C16257/9 WORD AND BYTE READ EXAMPLE

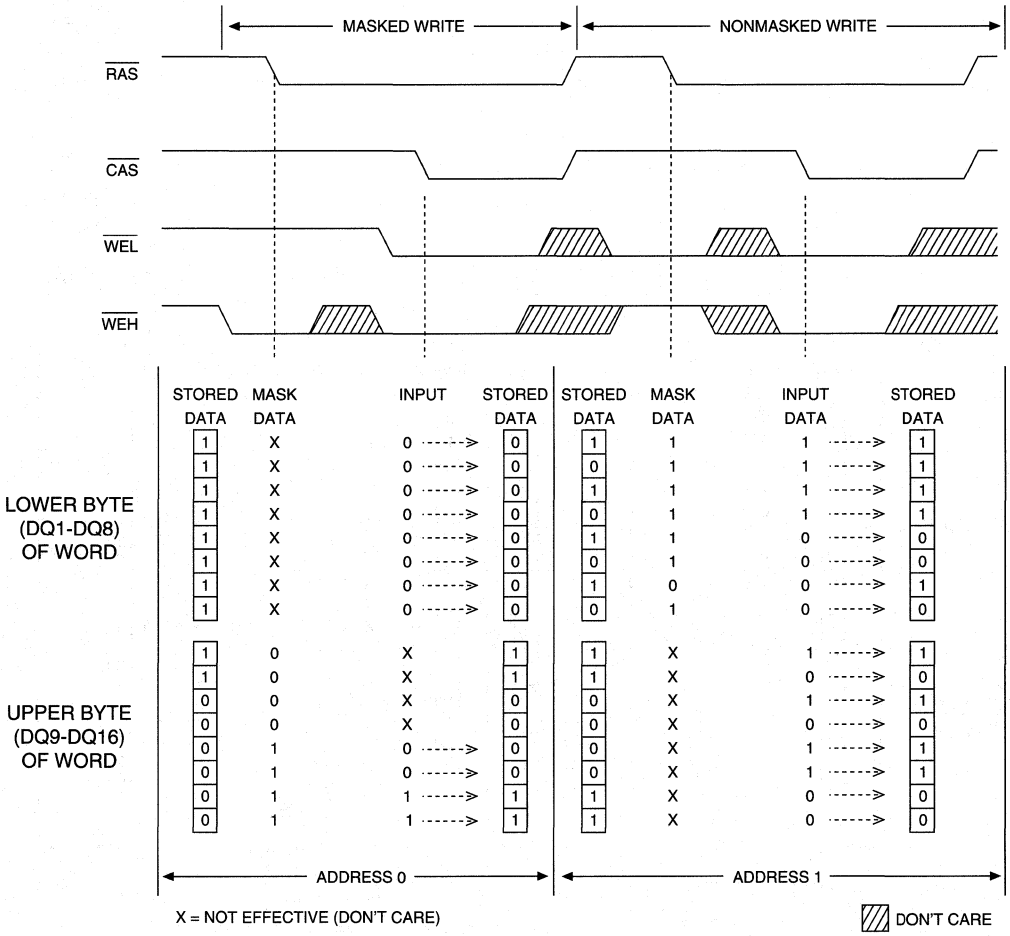


Figure 4
MT4C16258 MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

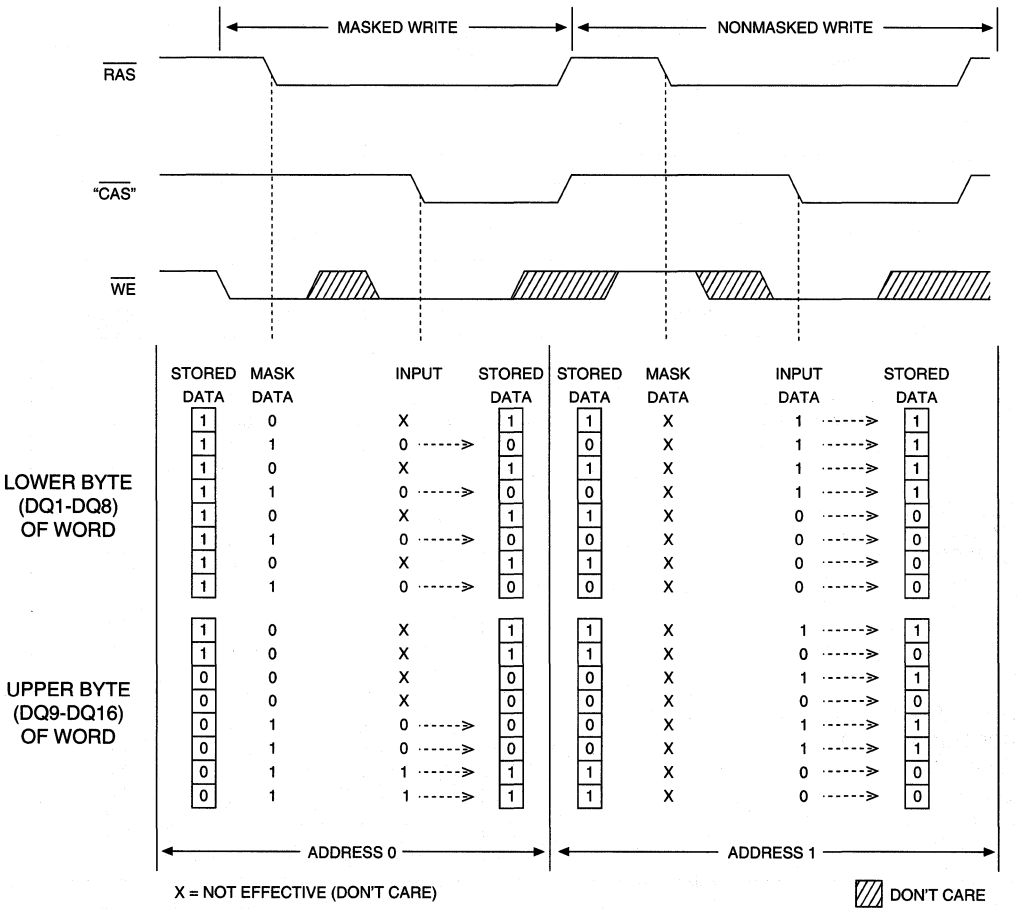


Figure 5
MT4C16259 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS signals must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C16259 only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6**	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	190	170	150	mA	3, 4, 42
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 42
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	190	170	150	mA	3, 5, 42
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	160	140	mA	3, 5

**60ns specifications may be limited to a V_{CC} range of ±5%.

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable time	^tOE		15		20		20	ns	33
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	32
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	31
Column-address hold time	^tCAH	10		15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	33

*60ns specifications may be limited to a V_{CC} range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 29, 33
Output disable time	^tOD	3	15	3	15	3	15	ns	29, 41
Write command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		10		10		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE)	^tWRH	10		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	34

*60ns specifications may be limited to a Vcc range of ±5%.

NOTES

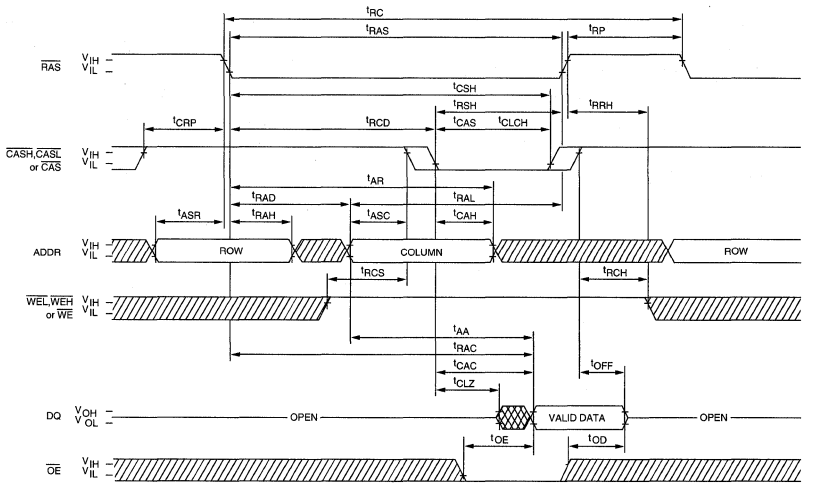
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.80 and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.*
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9.
27. MT4C16258/9 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

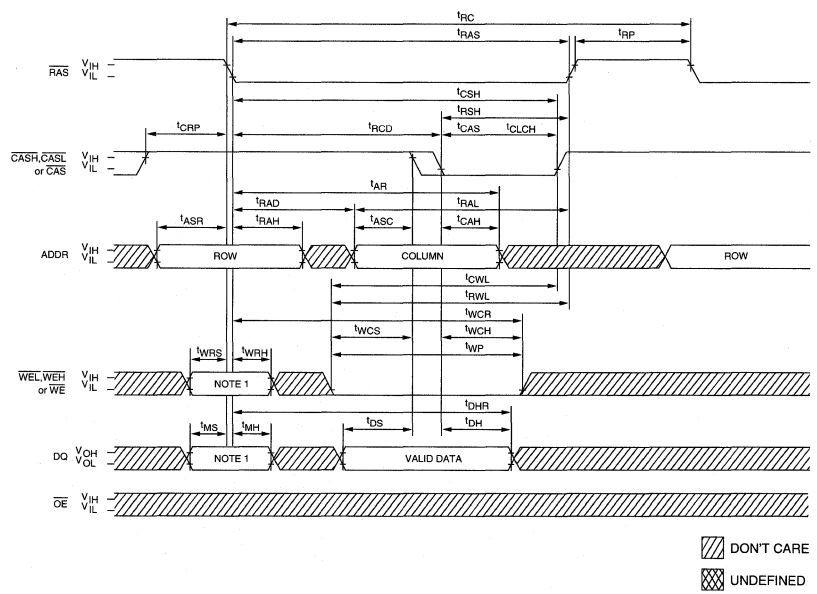
NOTES (continued)

30. Notes 31 through 41 apply to MT4C16257/9 only.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

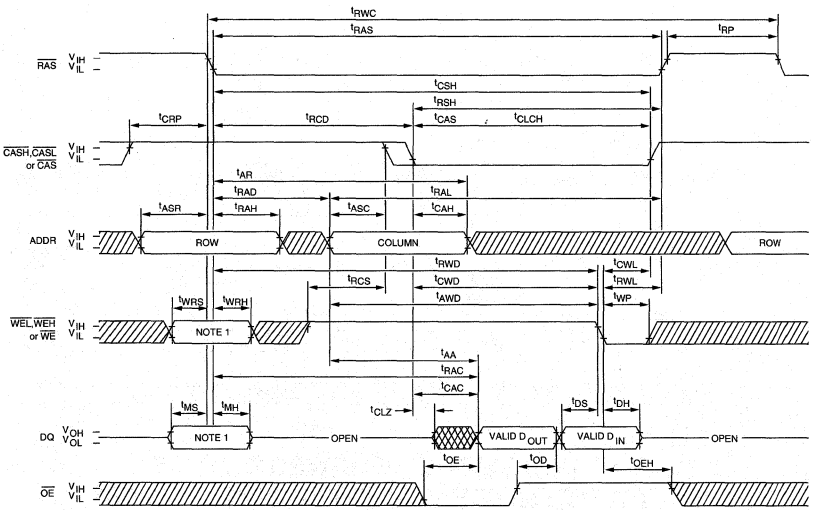


EARLY-WRITE CYCLE

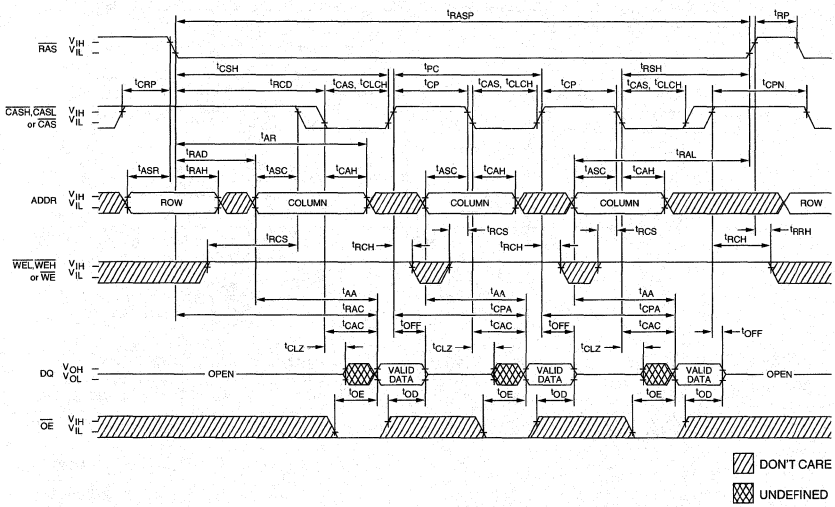


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

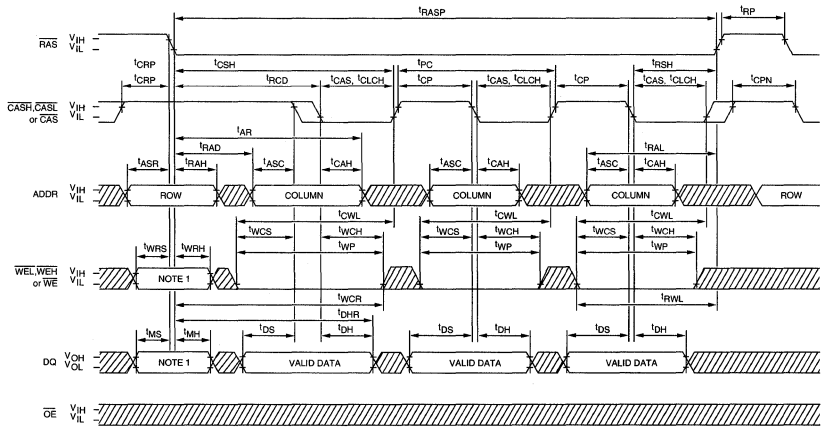


FAST-PAGE-MODE READ CYCLE

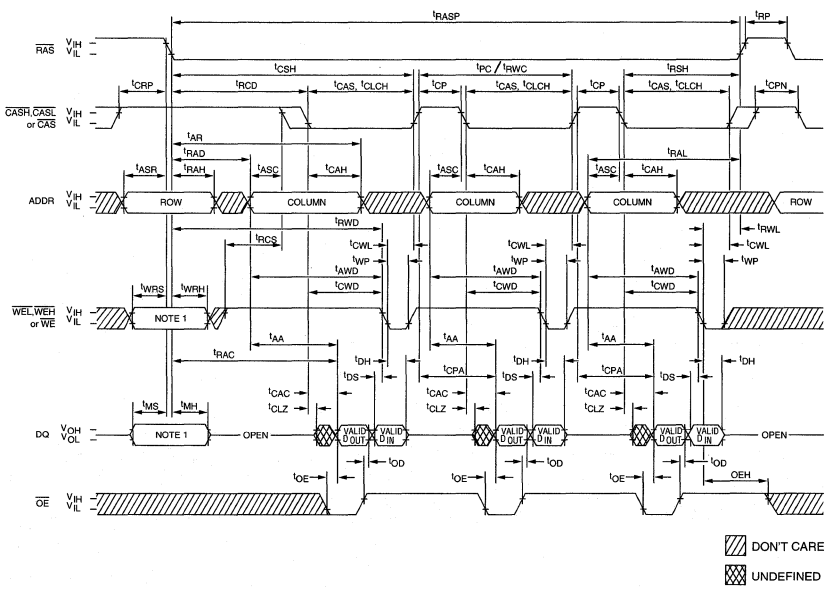


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

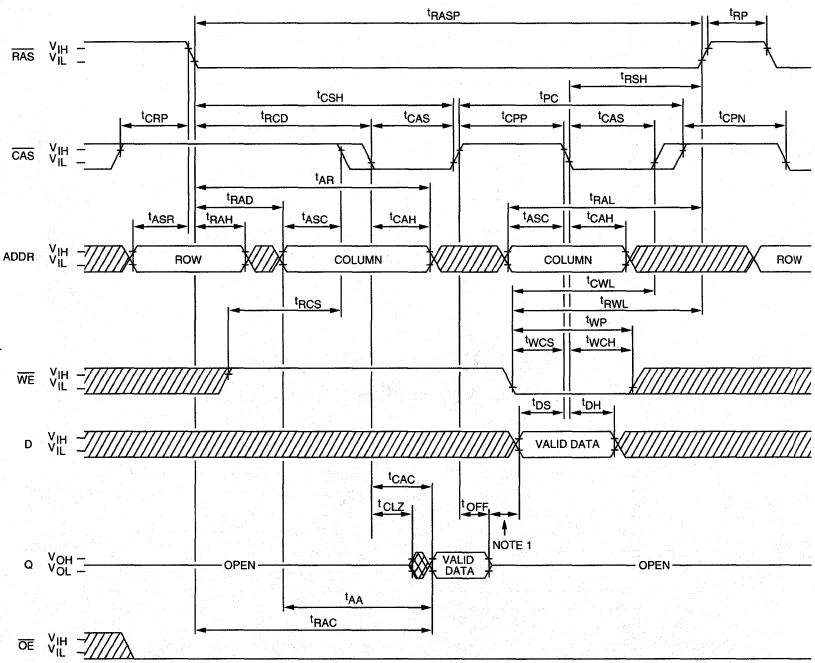


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



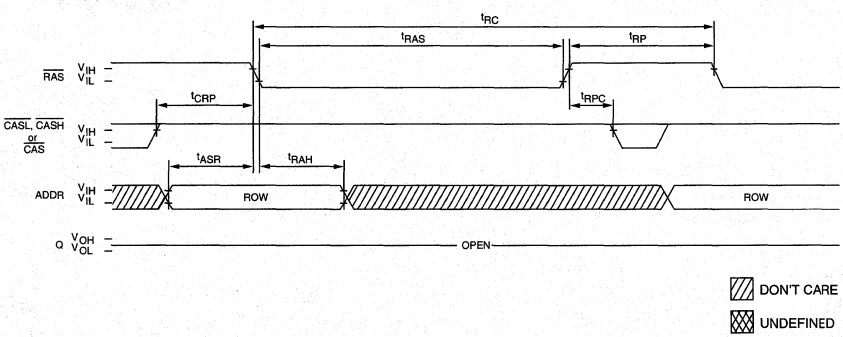
NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

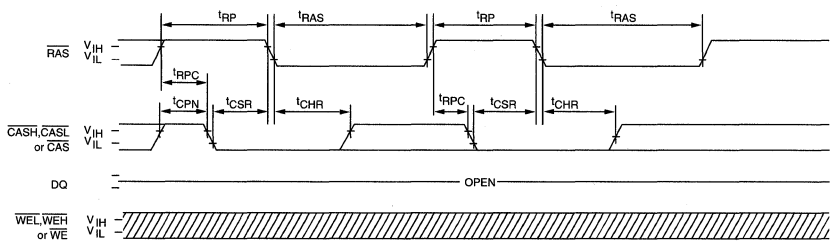


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

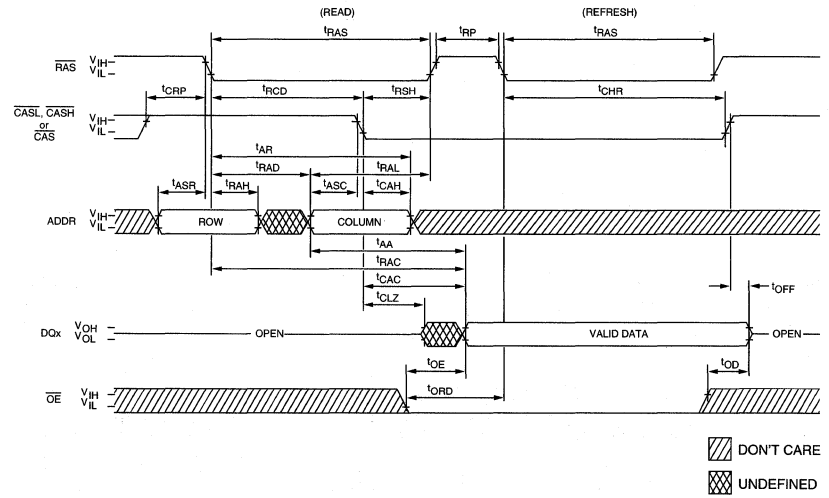
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

256K x 16 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST-PAGE-MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 L only)
- 512-cycle refresh distributed across 64ms
- Low power, 1mW standby; 500mW active, typical

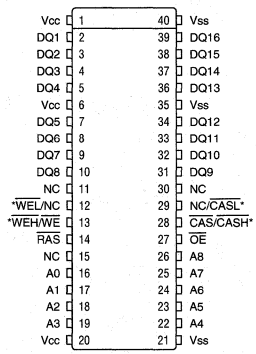
OPTIONS — MARKING

- Timing
  - 60ns access — -6*
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via WE (nonmaskable) — 16256 L
  - BYTE or WORD via CAS (nonmaskable) — 16257 L
  - BYTE or WORD via WE (maskable) — 16258 L
  - BYTE or WORD via CAS (maskable) — 16259 L
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z
- Part Number Example: MT4C16256DJ-7 L

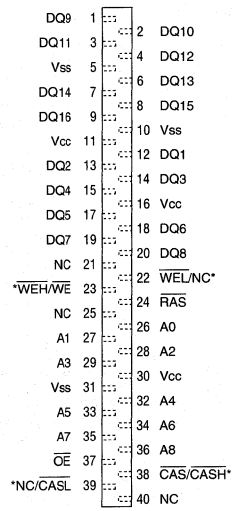
*60ns specifications are limited to a Vcc range of ±5%.

PIN ASSIGNMENT (Top View)

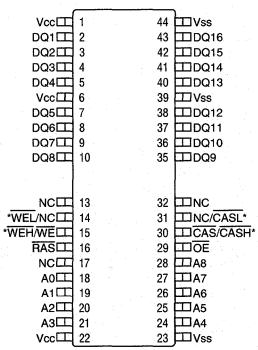
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-2)



40-Pin TSOP (SDE-2)



*MT4C16256/8 L / MT4C16257/9 L

GENERAL DESCRIPTION

The MT4C16256/7/8/9 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 L and MT4C16258 L have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 L and MT4C16259 L have both BYTE WRITE and WORD WRITE access cycles via two CAS pins. The MT4C16258 L and MT4C16259 L are also able to perform WRITE-PER-BIT accesses.

The MT4C16256 L and MT4C16257 L function in the same manner except that WEL and WEH on MT4C16256 L and CASL and CASH on MT4C16257 L control the selection of byte WRITE access cycles. WEL and WEH function in an

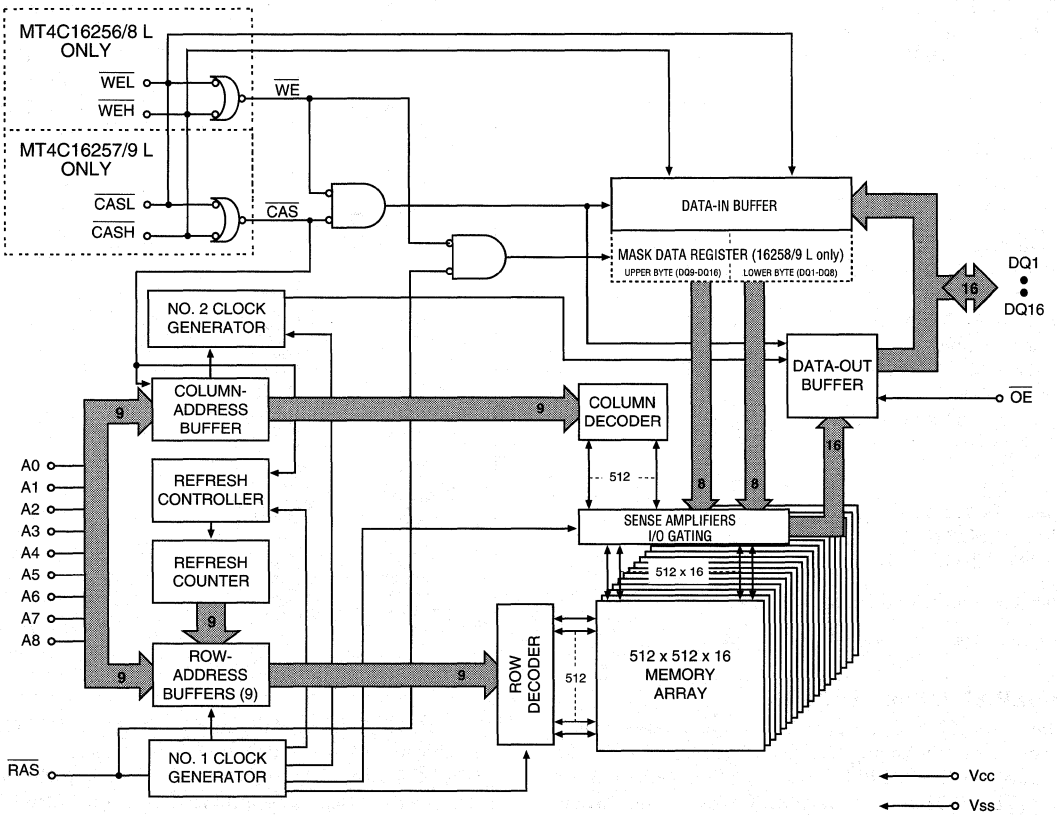
identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C16256 L $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 L $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257 L.

The MT4C16258 L and MT4C16259 L function in the same manner as MT4C16256 L and MT4C16257 L, respectively; they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C16258 L and MT4C16259 L to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 L and MT4C16259 L only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column-Address Strobe: $\overline{CAS}$ (MT4C16256/8 L) is used to latch-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column-Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9 L) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8 L) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9 L) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8 L) or $\overline{WE}$ (MT4C16257/9 L) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1625L6/8 L) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9 L) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 L also use $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8 L) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column-Address Strobe Lower Byte: $\overline{CASL}$ (MT4C16257/9 L) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8L) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8L) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8L). The MT4C16257/9L allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C16256 L and MT4C16258 L each have one $\overline{CAS}$ control while the MT4C16257 L and MT4C16259 L have two, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 L and MT4C16259 L $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 L and MT4C16259 L both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 L or MT4C16259 L are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the $\overline{WE}$ on the MT4C16256L or MT4C16258 L. The MT4C16256 L and MT4C16258 L $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 L and MT4C16258 L) or $\overline{WE}$ (MT4C16257 L and MT4C16259 L).

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address (A0-A8) defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256 L, MT4C16257 L, MT4C16258 L and MT4C16259 L can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 L BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 L BYTE WRITE and WORD WRITE cycles.

The MT4C16257 L also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 L BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 L ONLY)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 L and MT4C16257 L do not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 L MASKED WRITE operation and Figure 5 illustrates the MT4C16259 L MASKED WRITE operation.

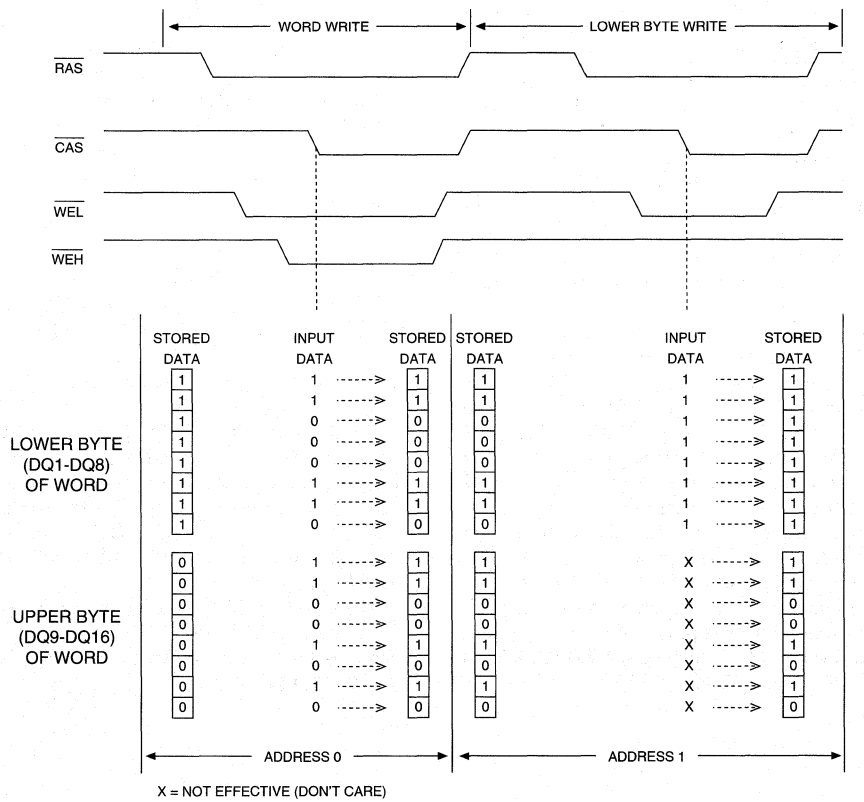


Figure 1
MT4C16256/8 L WORD AND BYTE WRITE EXAMPLE

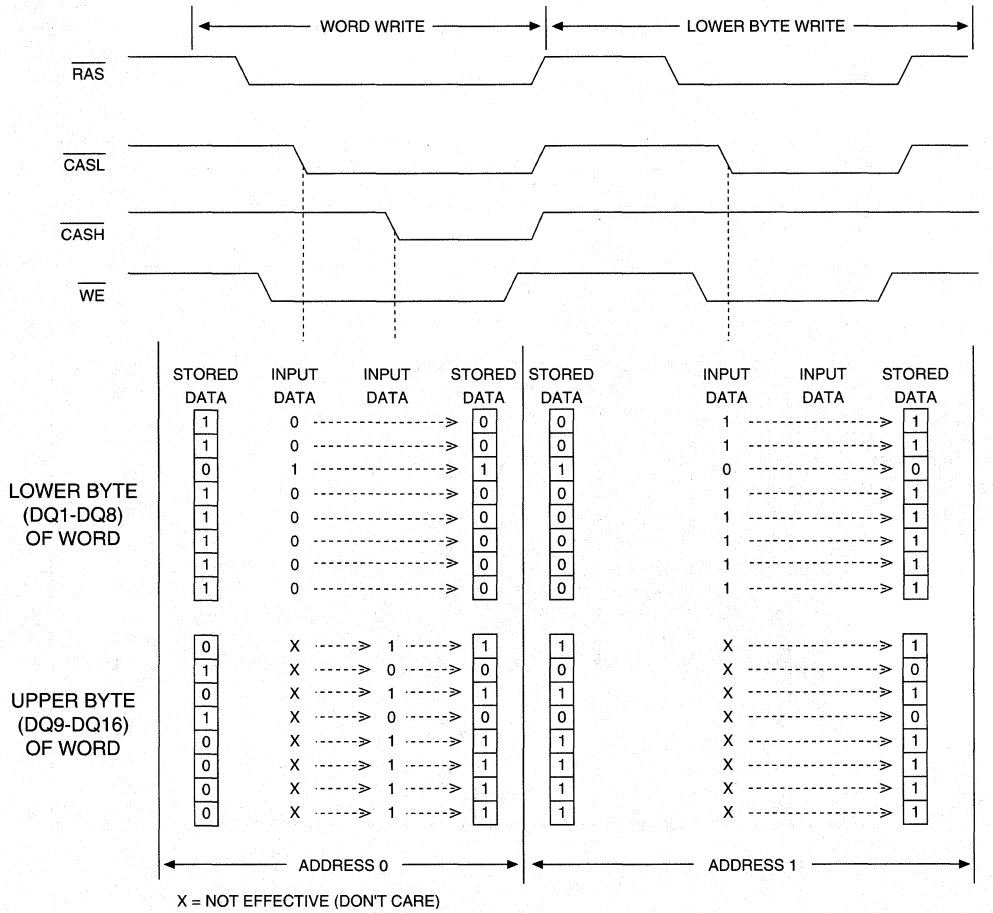


Figure 2
MT4C16257/9 L WORD AND BYTE WRITE EXAMPLE

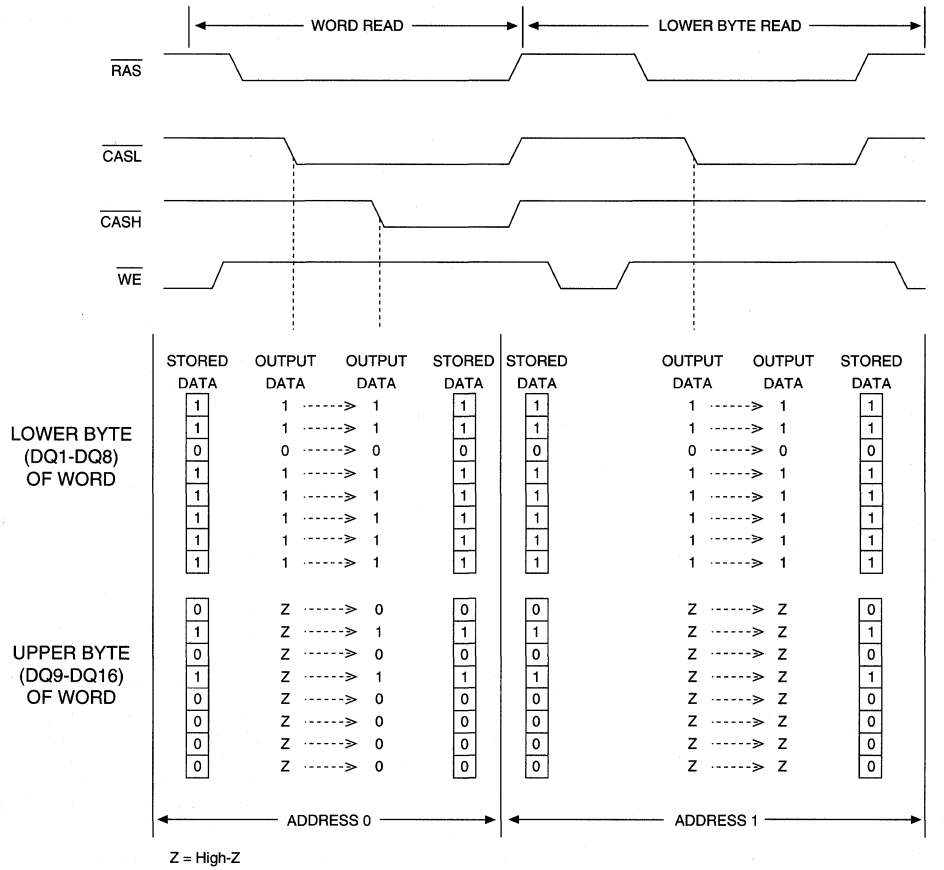


Figure 3
MT4C16257/9 L WORD AND BYTE READ EXAMPLE

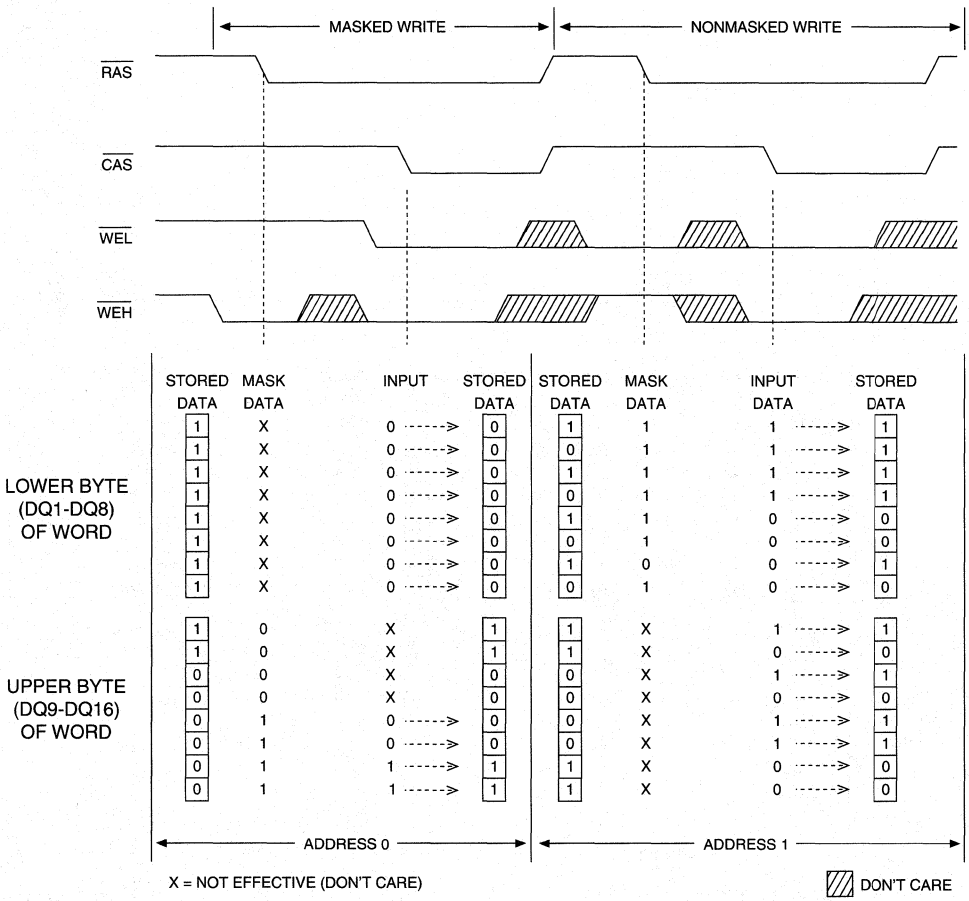


Figure 4
MT4C16258 L MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

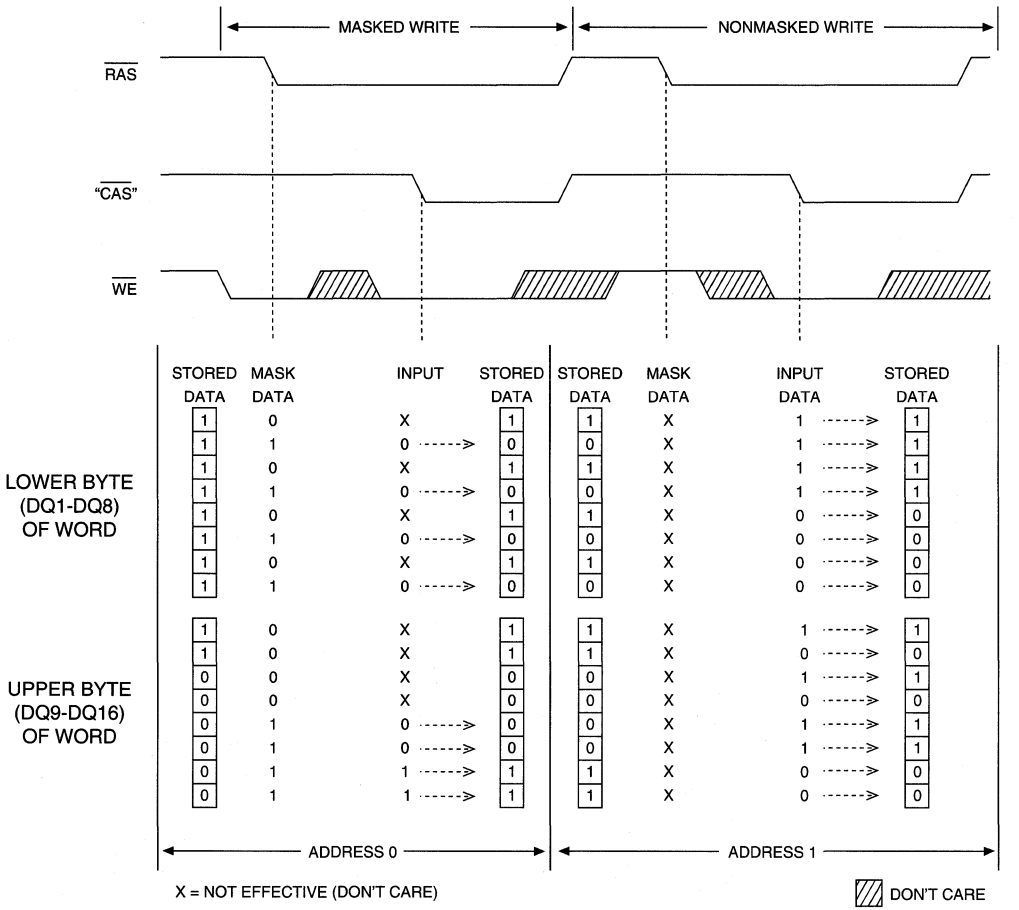


Figure 5
MT4C16259 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8 L

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	
BBU REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 L only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9 L

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4
BBU REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS signals must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C16259 L only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6**	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	190	170	150	mA	3, 4, 43
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 43
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	190	170	150	mA	3, 5, 43
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	160	140	mA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	300	300	300	µA	3, 5, 42

**60ns specifications may be limited to a V_{CC} range of ±5%.

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150			
READ-WRITE cycle time	^tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable time	^tOE		15		20		20	ns	33
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	32
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	31
Column-address hold time	^tCAH	10		15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	33

*60ns specifications may be limited to a Vcc range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 29, 33
Output disable time	^tOD	3	15	3	15	3	15	ns	29, 41
Write command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		10		10		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		7ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64		64	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE)	^tWRH	10		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	34

*60ns specifications may be limited to a Vcc range of ±5%.

NOTES

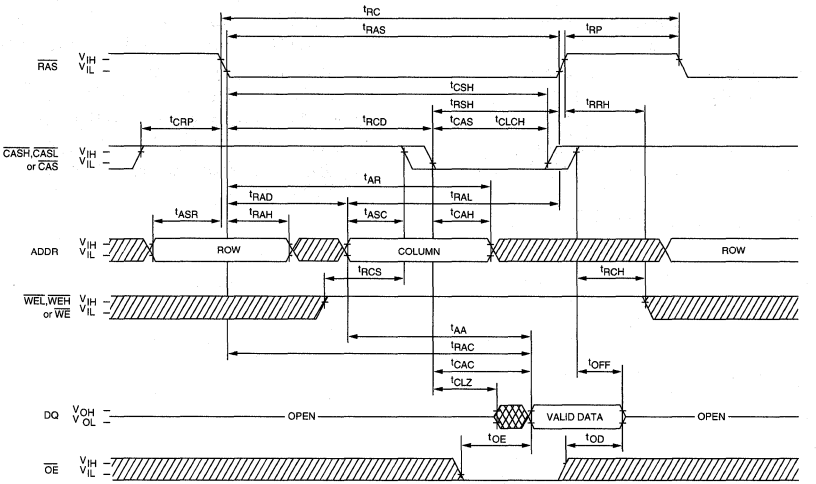
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.*
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8 L. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9 L.
27. MT4C16258/9 L only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the OE. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

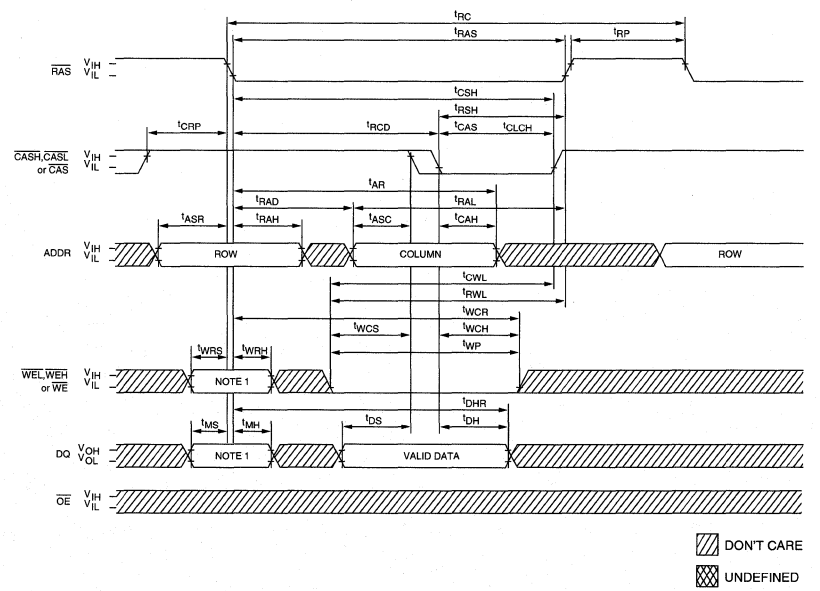
NOTES (continued)

30. Notes 31 through 41 apply to MT4C16257/9 L only.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.
43. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

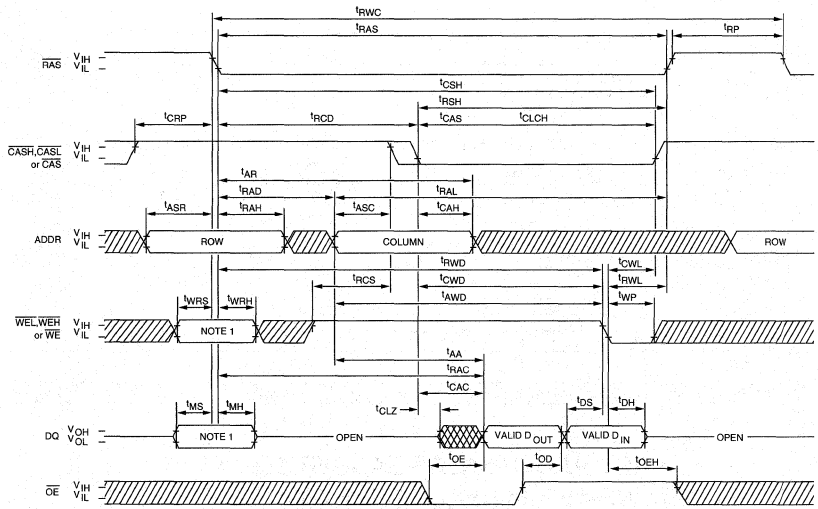


EARLY-WRITE CYCLE

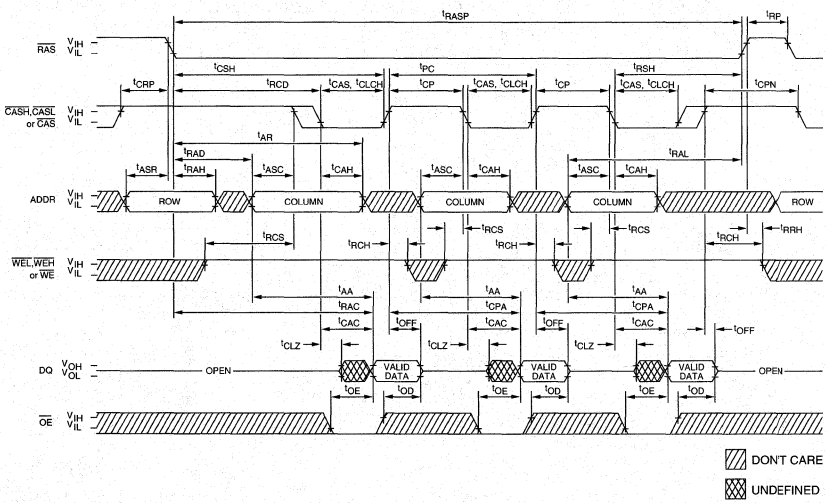


NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

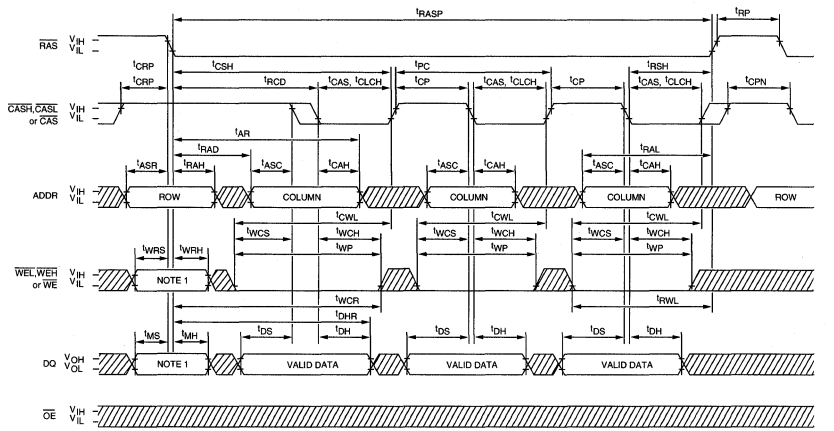


FAST-PAGE-MODE READ CYCLE

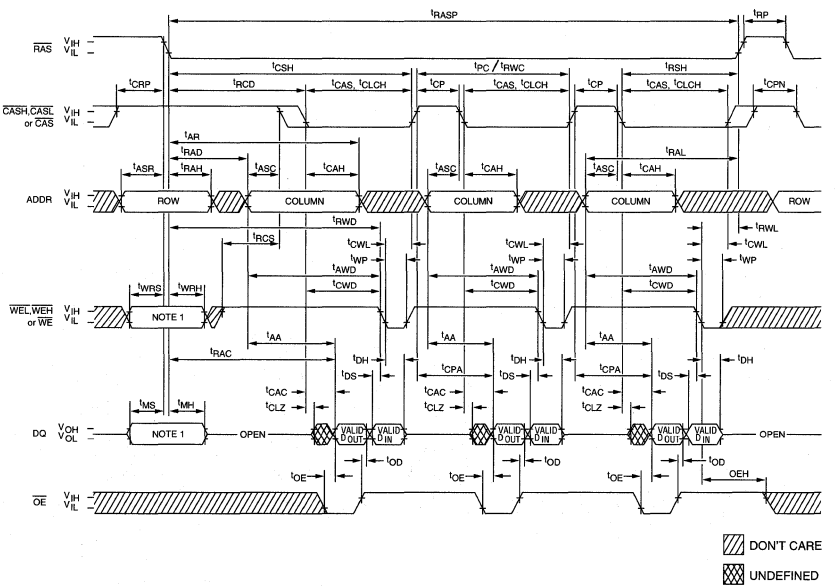


NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

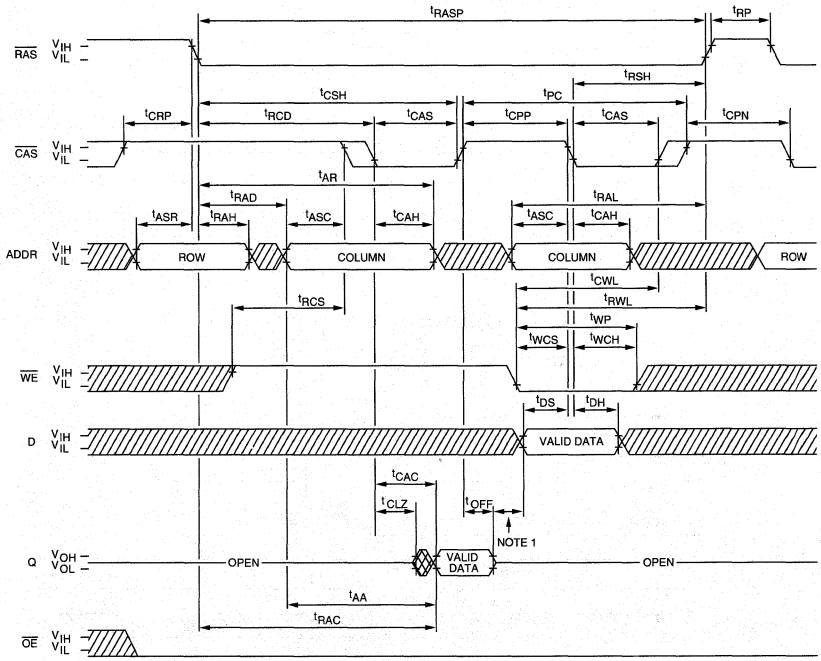


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



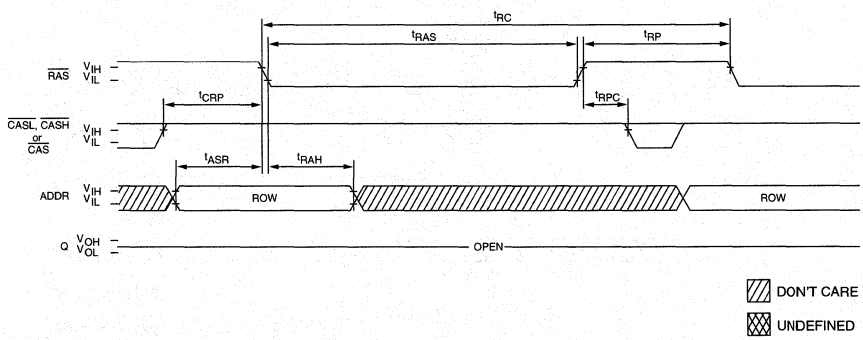
NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

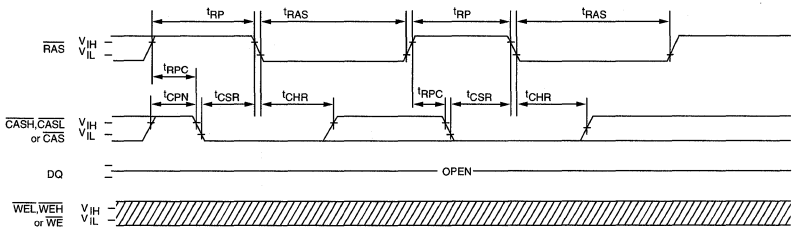


NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

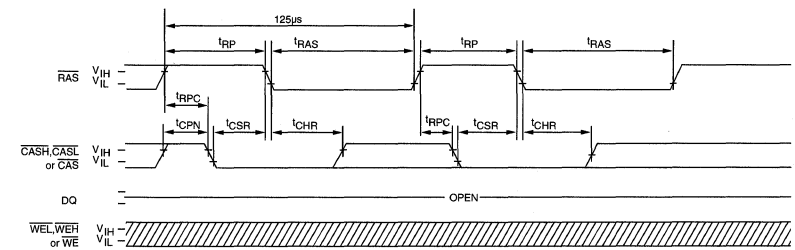
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



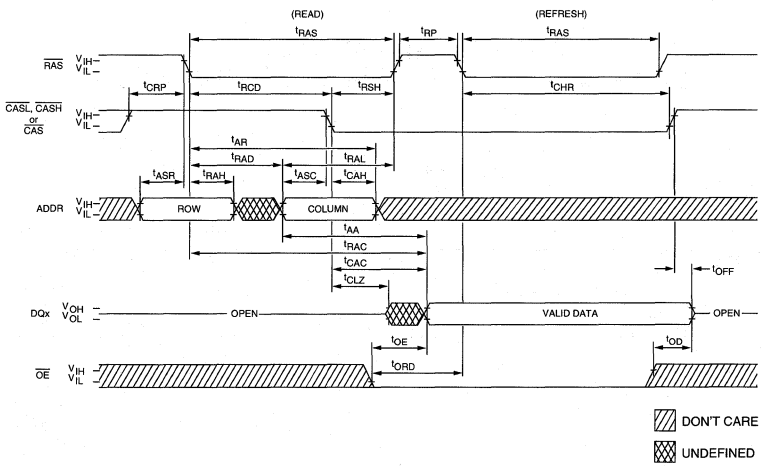
CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



BBU REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

256K x 16 DRAM

FAST-PAGE-MODE SELF REFRESH

FEATURES

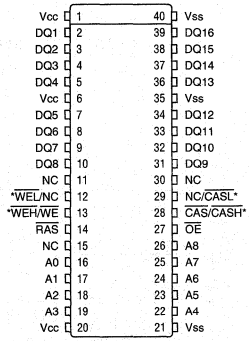
- SELF REFRESH, or "Sleep Mode"
- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 1mW standby; 500mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 64ms (nine rows and nine columns)
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) HIDDEN, and BATTERY BACKUP (BBU)
- Optional FAST-PAGE-MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 S only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 S only)

OPTIONS — MARKING

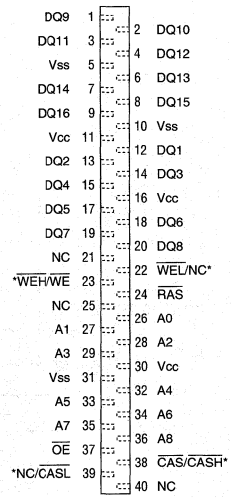
- Timing
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via $\overline{\text{WE}}$ (nonmaskable) — 16256 S
  - BYTE or WORD via $\overline{\text{CAS}}$ (nonmaskable) — 16257 S
  - BYTE or WORD via $\overline{\text{WE}}$ (maskable) — 16258 S
  - BYTE or WORD via $\overline{\text{CAS}}$ (maskable) — 16259 S
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z
- Part Number Example: MT4C16256DJ-7 S

PIN ASSIGNMENT (Top View)

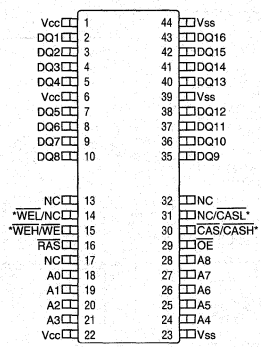
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-1)



40-Pin TSOP (SDE-2)



*MT4C16256/8 S / MT4C16257/9 S

GENERAL DESCRIPTION

The MT4C16256/7/8/9 S are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 S and MT4C16258 S have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 S and MT4C16259 S have both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. The MT4C16258 S and MT4C16259 S are also able to perform WRITE-PER-BIT accesses.

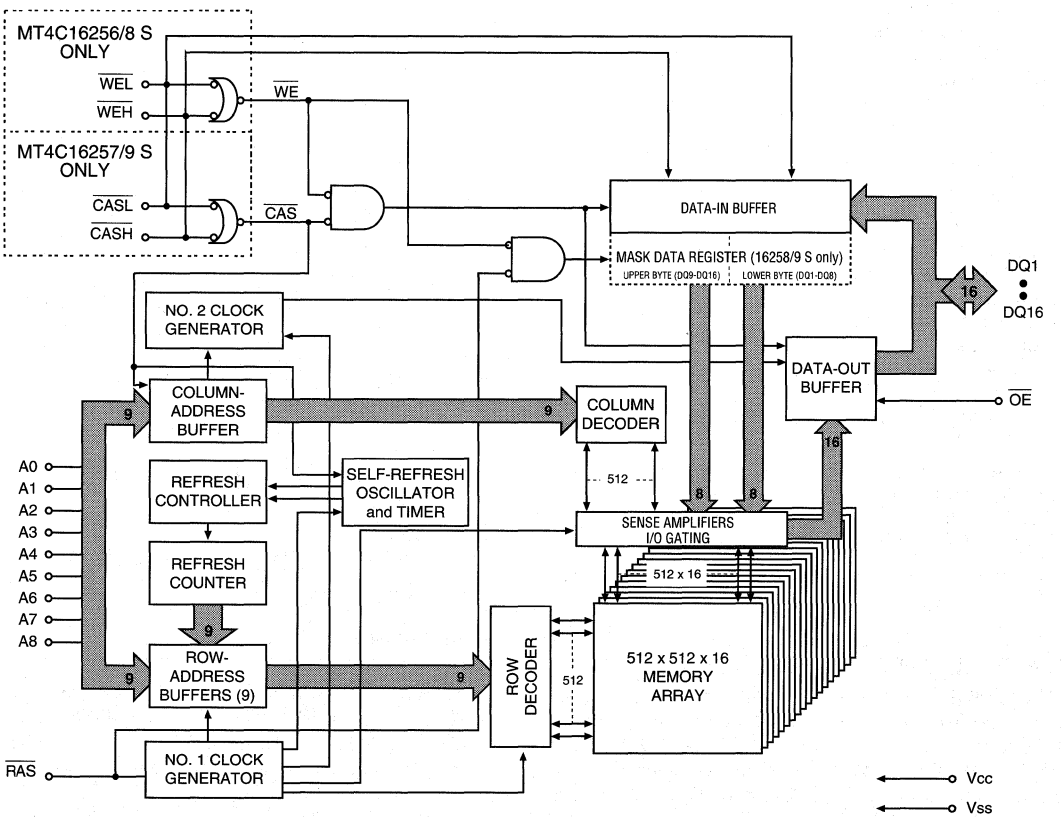
The MT4C16256 S and MT4C16257 S function in the same manner except that $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ on MT4C16256 S and $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ on MT4C16257 S control the selection of byte WRITE access cycles. $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ function in an identical manner to $\overline{\text{WE}}$ in that either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ will generate an internal $\overline{\text{WE}}$. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ function in an identical manner to $\overline{\text{CAS}}$ in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate an internal $\overline{\text{CAS}}$.

The MT4C16256 S $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 S $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$)to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257 S.

The MT4C16258 S and MT4C16259 S function in the same manner as MT4C16256 S and MT4C16257 S, respectively; they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C16258 S and MT4C16259 S to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 S and MT4C16259 S only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column-Address Strobe: $\overline{CAS}$ (MT4C16256/8 S) is used to latch-in the 9 column-address bits and enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column-Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9 S) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9 S) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8 S) or $\overline{WE}$ (MT4C16257/9 S) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C16256/8 S) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9 S) controls DQ1 through DQ16inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 S also use $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8 S) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column-Address Strobe Lower Byte: $\overline{CASL}$ (MT4C16257/9 S) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8 S) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C16256/8 S). The MT4C16257/9 S allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. Both the MT4C16256 S and MT4C16258 S have one $\overline{CAS}$ control while the MT4C16257 S and MT4C16259 S have two, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is that each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 S and MT4C16259 S $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 S and MT4C16259 S both byte READ and byte WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 S or MT4C16259 S are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the $\overline{WE}$ on the MT4C16256 S or MT4C16258 S. The MT4C16256 S and MT4C16258 S $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 S and MT4C16258 S) or $\overline{WE}$ (MT4C16257 S and MT4C16259 S).

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. Only one of the $\overline{CAS}$ signals ($\overline{CASL}$ or $\overline{CASH}$) is required to transition LOW in order to perform a CBR REFRESH cycle. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during sleep mode. Thus, an external clock is not required, which provides additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (^{t}RASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for 600µs (^{t}CHD), $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care." $\overline{CAS}$ is a "don't care" until ^{t}CHS, at which time $\overline{CAS}$ must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically 200ns (^{t}RPS). Once the SELF REFRESH mode has been terminated, accesses to the DRAM can begin immediately, as long as the system uses distributed CBR REFRESH as the standard refresh. The first CBR pulse should occur within the time of the EXTERNAL REFRESH rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three EXTERNAL REFRESH rate periods. The EXTERNAL REFRESH rate is typically 125µs per row-address. This immediate access is possible because Micron employs a distributed CBR SELF REFRESH scheme internally.

The alternative approach when exiting SELF REFRESH mode is to perform a refresh of all rows within the time of the EXTERNAL REFRESH rate prior to active use of the DRAM. This burst must be done because anything other than distributed CBR REFRESH is used as the standard refresh. Once this burst has been completed, the DRAM may be used in the functional mode with burst or distributed refreshes such as CBR or $\overline{RAS}$-ONLY.

Micron's devices allow you to access the DRAM as soon as SELF REFRESH is exited, while other manufacturers' devices may require a full burst when exiting, regardless of the type of refresh used. To prevent possible compatibility problems, you may want to design the controller to perform the burst when exiting SELF REFRESH.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256 S, MT4C16257 S, MT4C16258 S and MT4C16259 S can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 S BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 S BYTE WRITE and WORD WRITE cycles.

The MT4C16257 S also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 S BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 S Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 S and MT4C16257 S do not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 S MASKED WRITE operation and Figure 5 illustrates the MT4C16259 S MASKED WRITE operation.

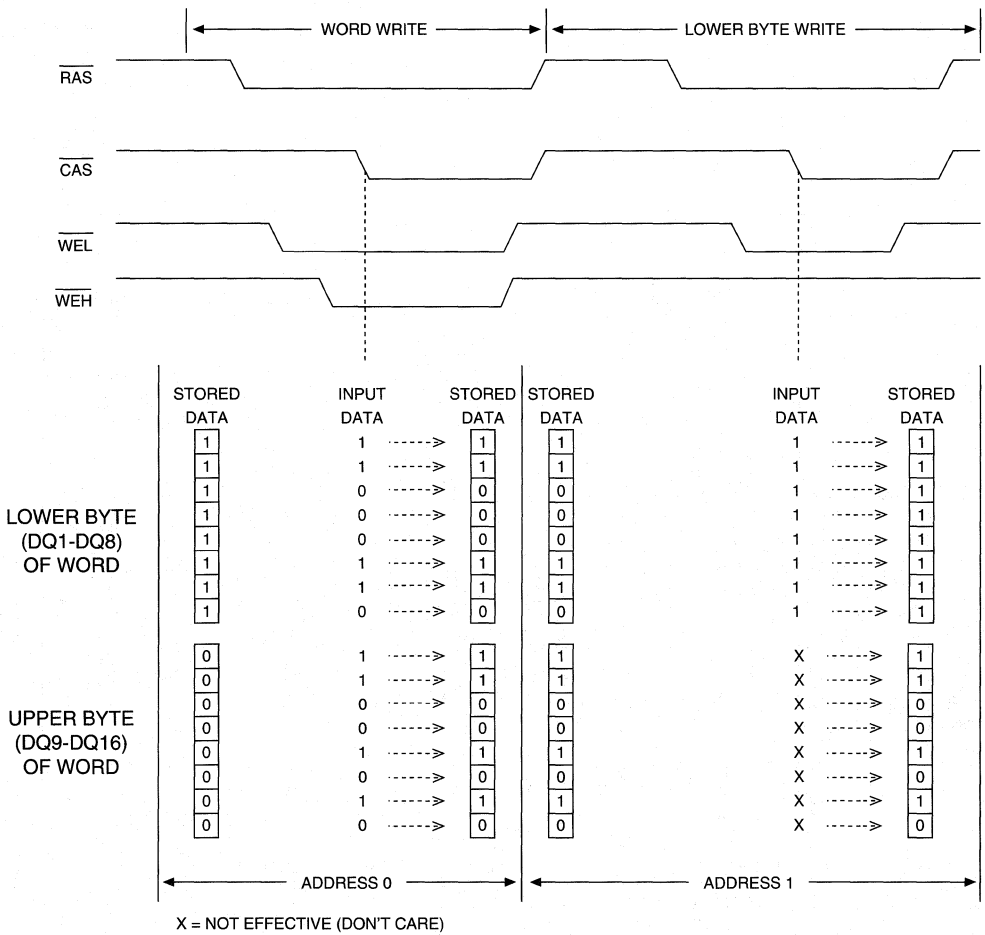


Figure 1
MT4C16256/8 S WORD AND BYTE WRITE EXAMPLE

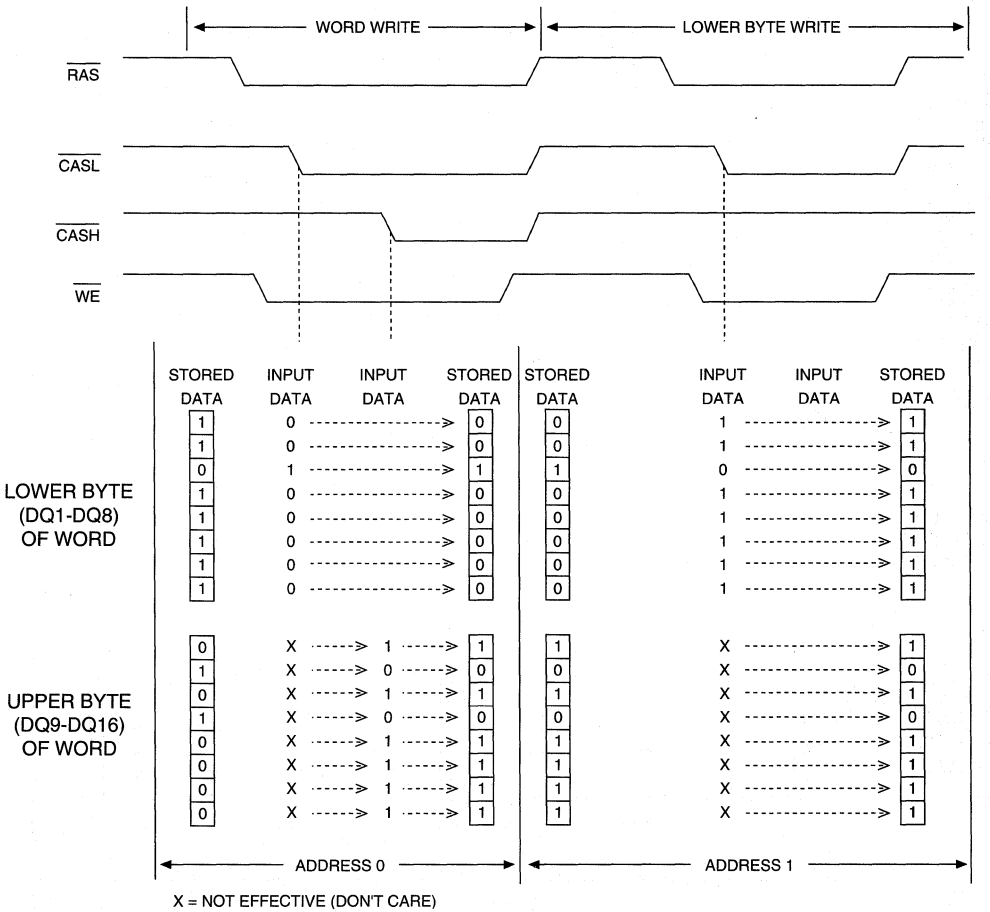


Figure 2
MT4C16257/9 S WORD AND BYTE WRITE EXAMPLE

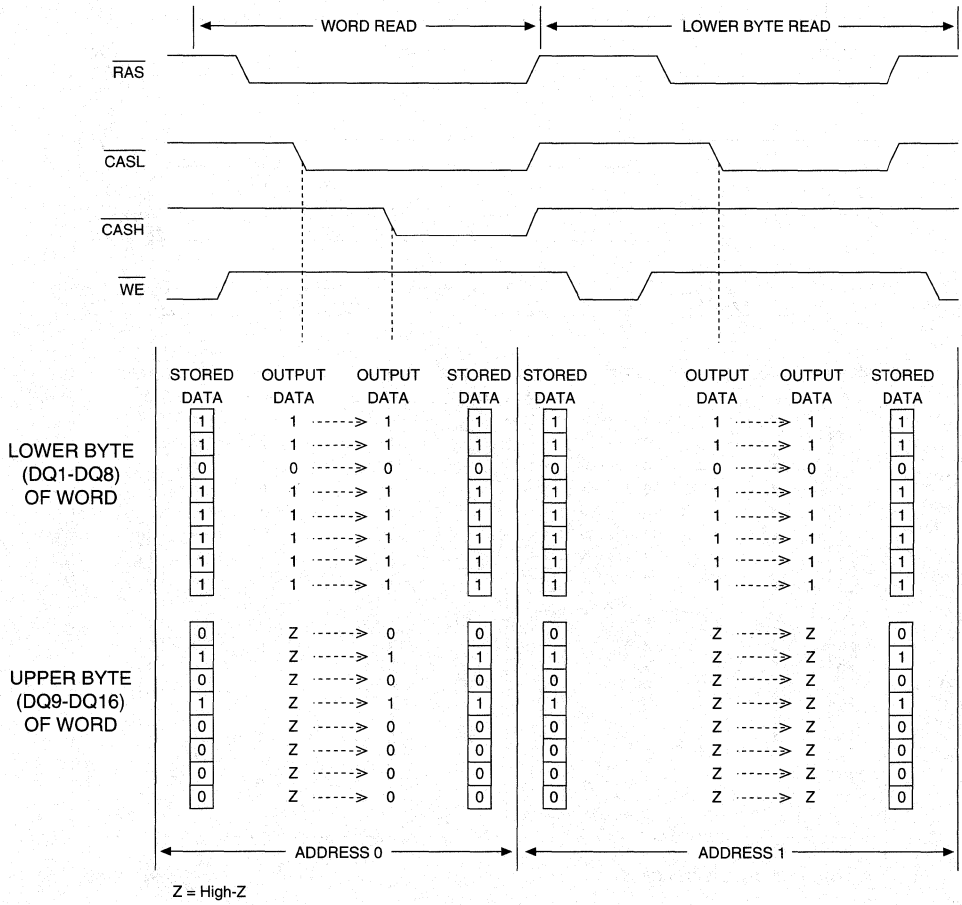


Figure 3
MT4C16257/9 S WORD AND BYTE READ EXAMPLE

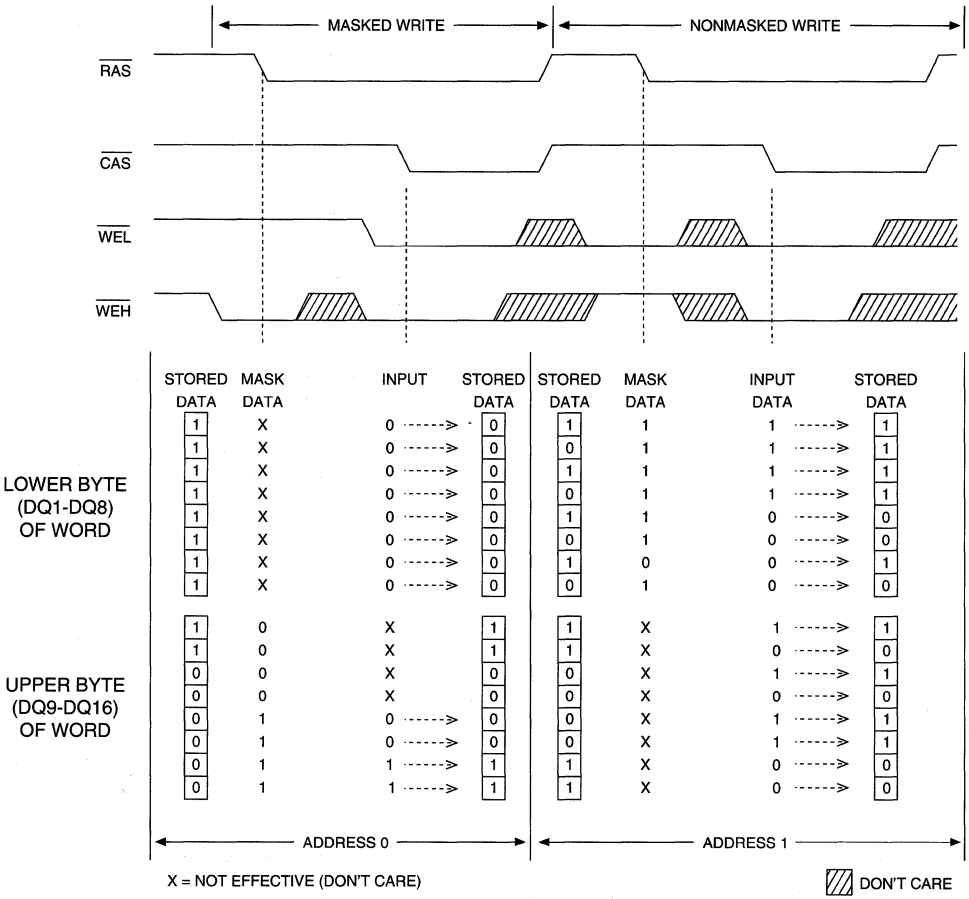


Figure 4
MT4C16258 S MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

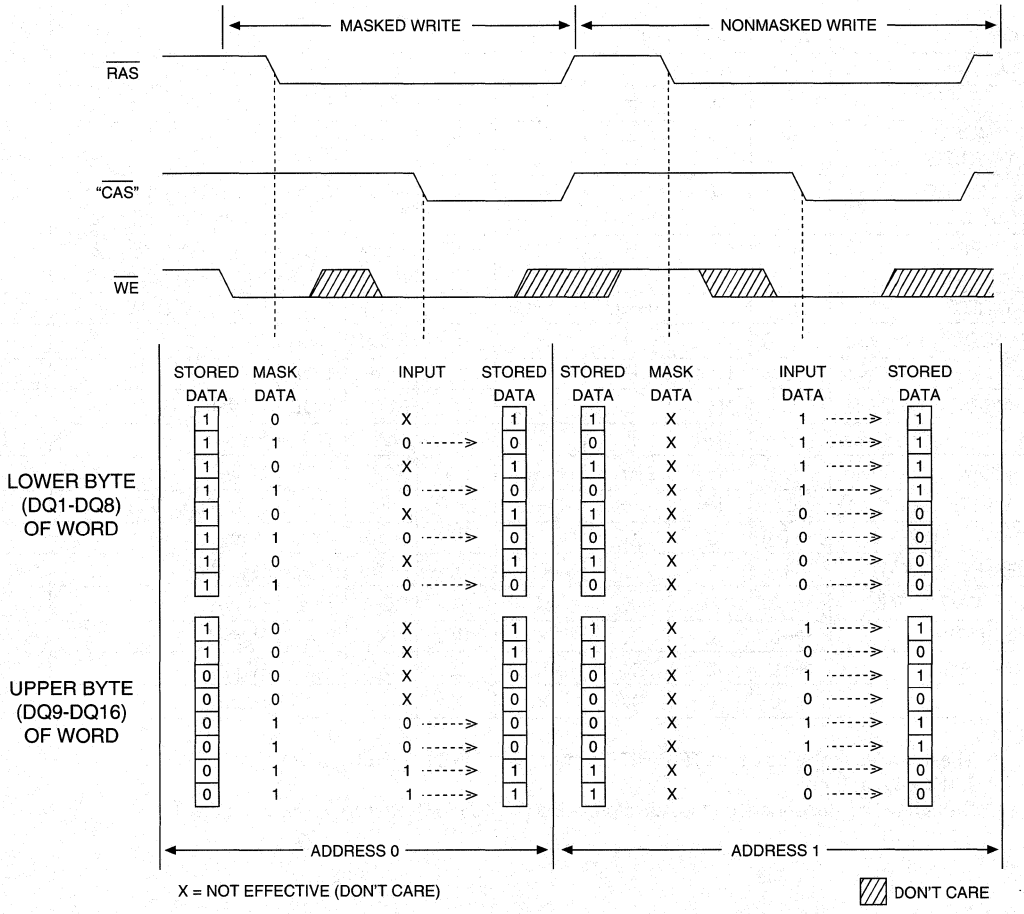


Figure 5
MT4C16259 S MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8 S

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	
BBU REFRESH		H→L	L	X	X	X	X	X	High-Z	
SELF REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 S only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9 S

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4
BBU REFRESH		H→L	L	H	X	X	X	X	High-Z	4
SELF REFRESH		H→L	L	H	X	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C16259 S only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	uA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	150	mA	3, 4, 43
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	110	100	mA	3, 4, 43
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	170	150	mA	3, 5, 43
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	160	140	mA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A8 and D_{IN} = Vcc - 0.2V (D_{IN} may be left open); ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	300	300	µA	3, 5,42
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A8 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	400	400	µA	5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15, 33
Output Enable time	^tOE		20		20	ns	33
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	32
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	31
Column-address hold time	^tCAH	15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	ns	20, 29, 33
Output disable time	^tOD	3	15	3	15	ns	29, 41
Write command setup time	^tWCS	0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		10		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	26
Write command pulse width	^tWP	10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	26, 32
Data-in setup time	^tDS	0		0		ns	22, 33
Data-in hold time	^tDH	15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE and CBR REFRESH)	^tWRH	15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		ns	34
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		us	44
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	150		150		ns	44
$\overline{CAS}$ hold time during SELF REFRESH cycle	^tCHS	-70		-70		ns	44
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	600		600		us	29

NOTES

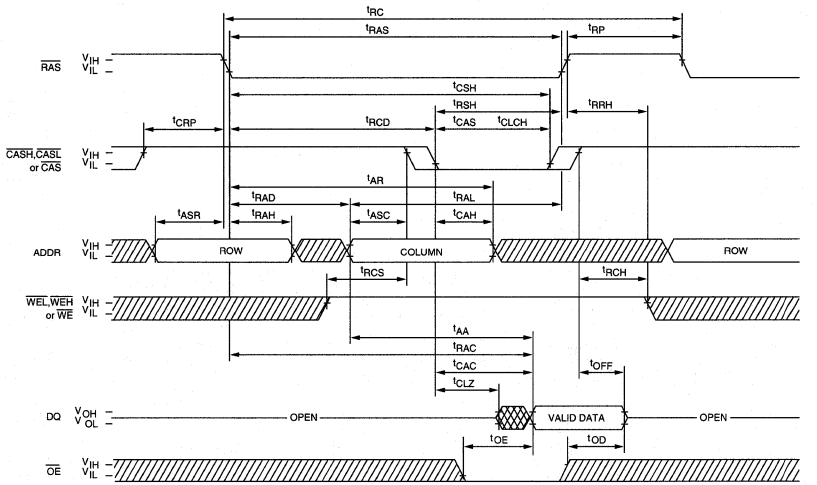
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; is it not a reference to V_{OH} or V_{OL}.*
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8 S. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9 S.
27. MT4C16258/9 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the OE. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

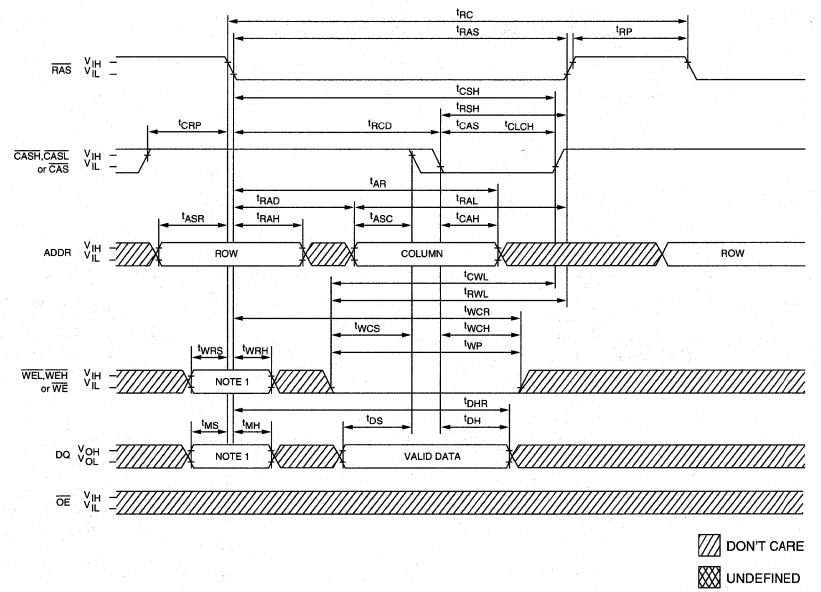
NOTES (continued)

30. Notes 31 through 41 apply to MT4C16257/9 S only.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during BBU cycle.
43. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
44. When exiting the SELF REFRESH mode, one CBR REFRESH must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.

READ CYCLE

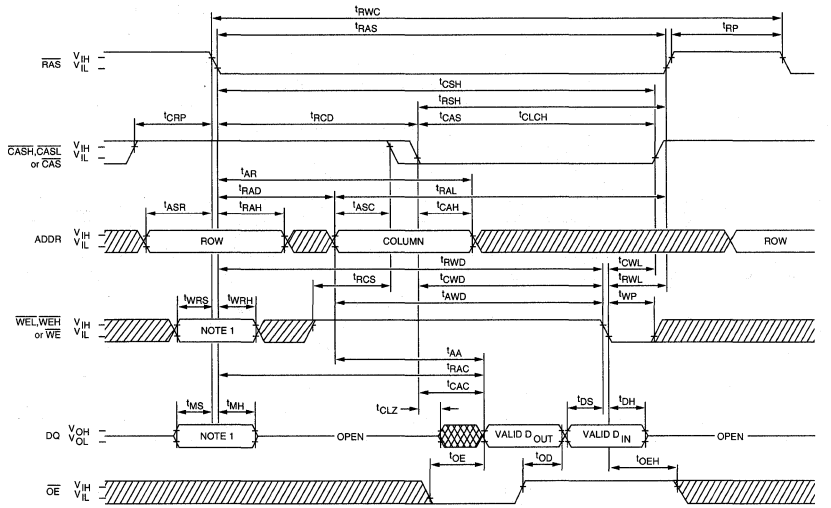


EARLY-WRITE CYCLE

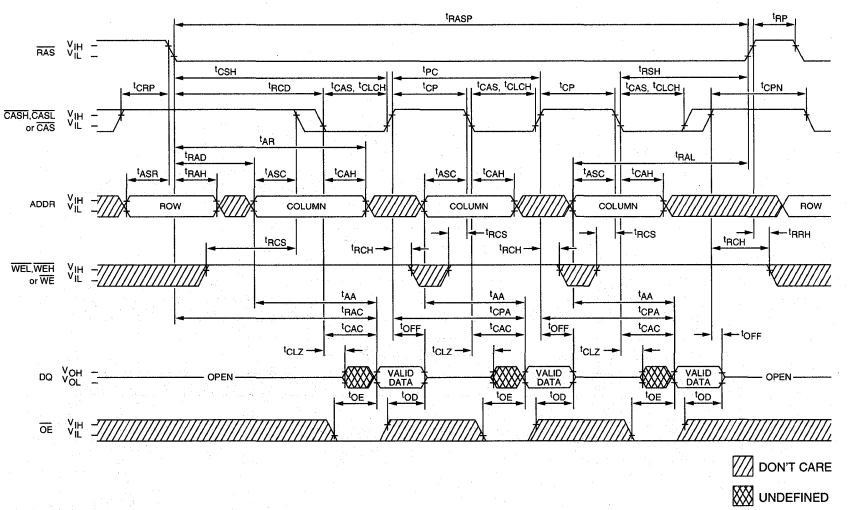


NOTE: 1. Applies to MT4C16258 S and MT4C16259 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 S and MT4C16257 S are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

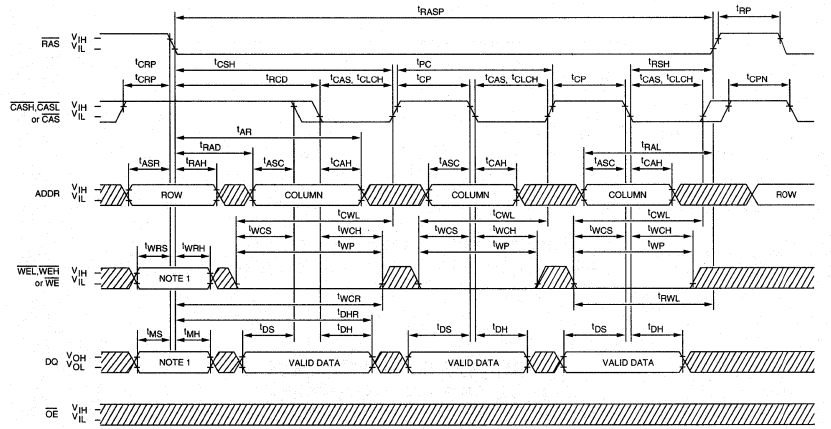


FAST-PAGE-MODE READ CYCLE

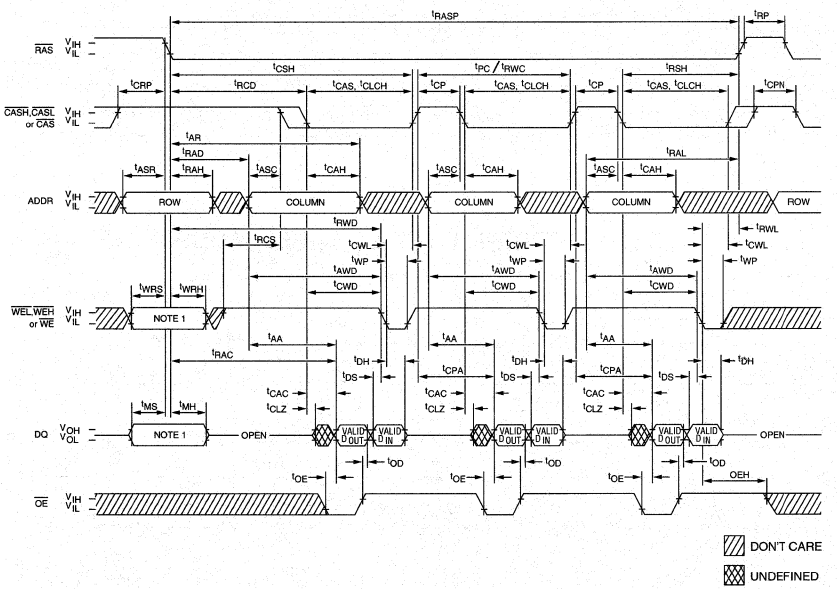


NOTE: 1. Applies to MT4C16258 S and MT4C16259 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 S and MT4C16257 S are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

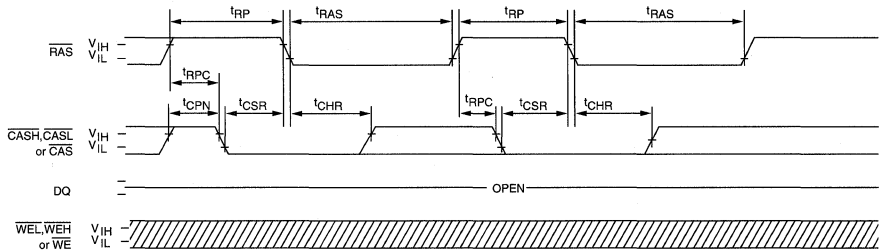


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

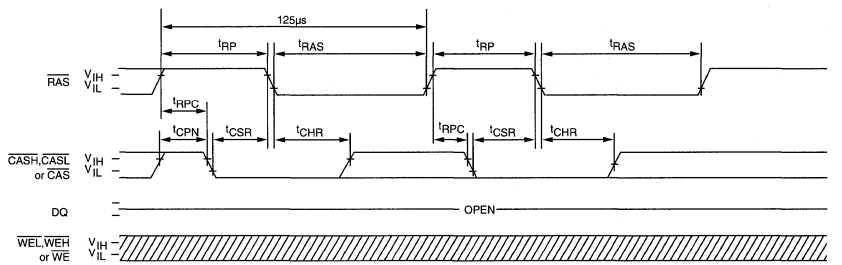


NOTE: 1. Applies to MT4C16258 S and MT4C16259 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 S and MT4C16257 S are "don't care" at $\overline{RAS}$ time.

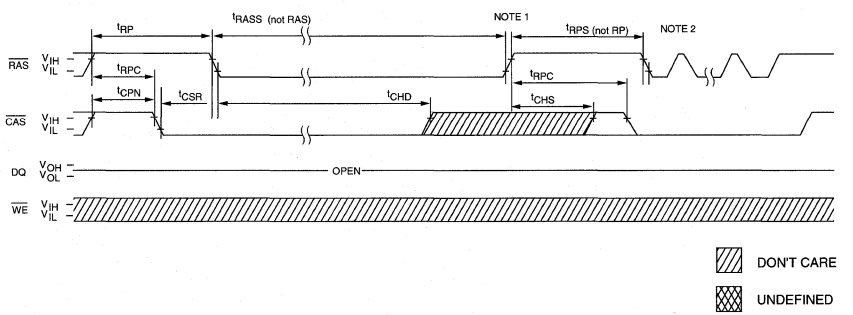
CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



BBU REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)

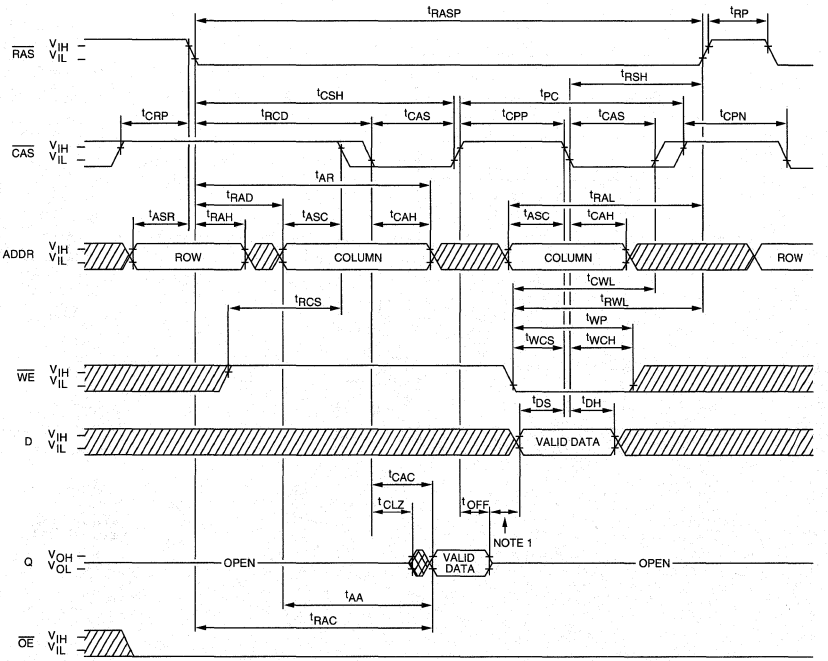


SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A8; $\overline{OE}$ = DON'T CARE)



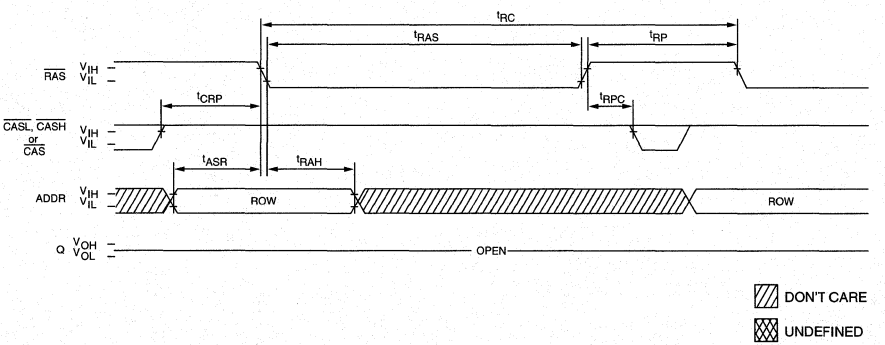
NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



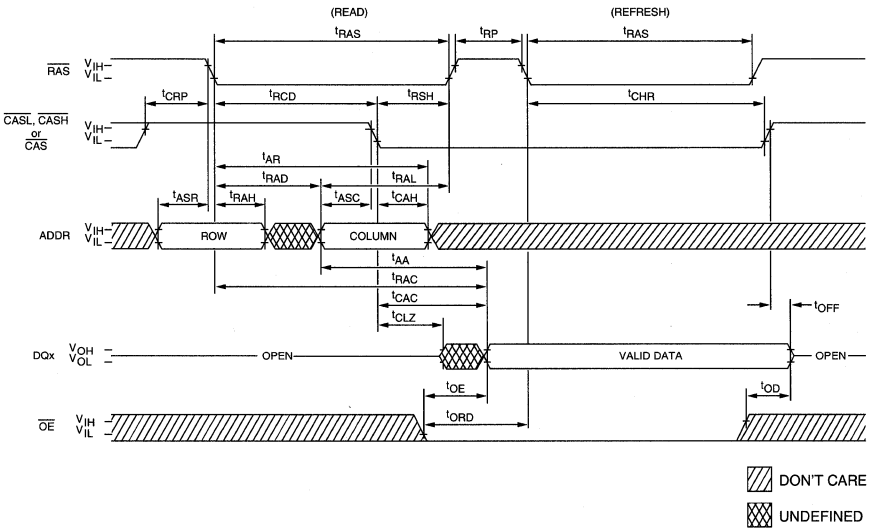
NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



WIDE DRAM

256K x 16 DRAM

FAST-PAGE-MODE WITH EXTENDED DATA-OUT

FEATURES

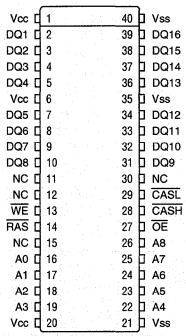
- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE with EXTENDED DATA-OUT access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C16271 only)

OPTIONS — MARKING

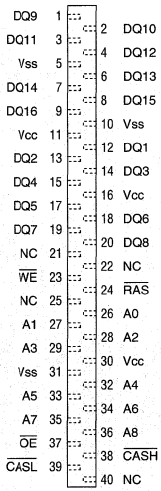
- Timing
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via $\overline{CAS}$ (nonmaskable) — 16270
  - BYTE or WORD via $\overline{CAS}$ (maskable) — 16271
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z
- Part Number Example: MT4C16270DJ-7

PIN ASSIGNMENT (Top View)

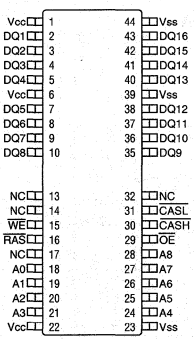
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-2)



40-Pin TSOP (SDE-2)



GENERAL DESCRIPTION

The MT4C16270/1 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 and MT4C16271 have both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The MT4C16271 is also able to perform WRITE-PER-BIT accesses.

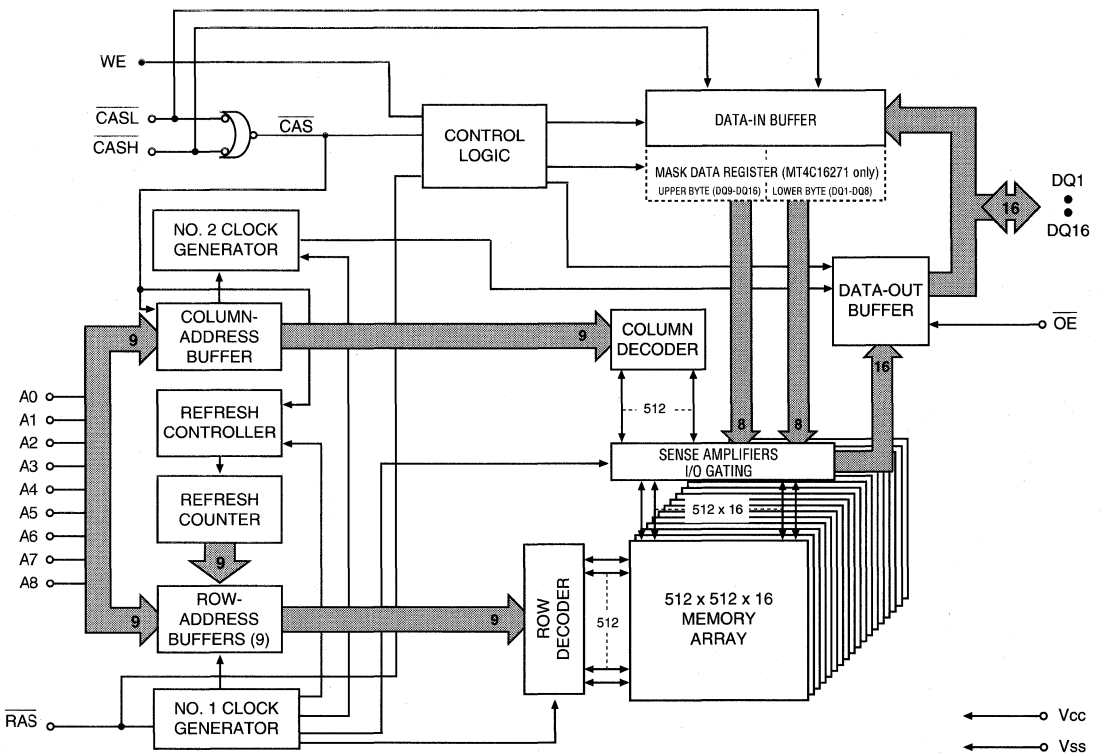
Both the MT4C16270 and MT4C16271 offer an accelerated FAST-PAGE-MODE cycle through a feature called EXTENDED DATA-OUT.

The MT4CMT4C16270/1 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE

cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner.

The MT4C16271 functions in the same manner as MT4C16270; it has NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C216271 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16271only).
28	30	38	$\overline{CASH}$	Input	Column-Address Strobe Upper Byte: $\overline{CASH}$ is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CASL}$ / $\overline{CASH}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16271 also uses $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
29	31	39	$\overline{CASL}$	Input	Column-Address Strobe Low Byte: $\overline{CASL}$ is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CASL}$ / $\overline{CASH}$ to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{CASL}$ / $\overline{CASH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. The MT4C16270/1 allow for BYTE READ cycles.
11, 12, 15, 30	13, 14, 17, 32	21, 22, 25, 40	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	V_{CC}	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter nine bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. Both the MT4C16270 and MT4C16271 have two $\overline{CAS}$ controls, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is that each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$ and $\overline{RAS}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16270/1 $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16270/1 both byte READ and byte WRITE cycle capabilities.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WE}$ and $\overline{RAS}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

EXTENDED DATA-OUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4C16270/1 offer an accelerated FAST-PAGE-MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EXTENDED DATA-OUT and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and FAST-PAGE-MODE READ waveforms).

EXTENDED DATA-OUT operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ is LOW. If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. During cycles other than PAGE-MODE READ, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16270/1 can be viewed as two 256K x 8 DRAMS which have common input controls. Figure 1 illustrates the MT4C16270 BYTE WRITE and WORD WRITE cycles.

The MT4C16270/1 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 2 illustrates the MT4C16270 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16271 only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C216270 does not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port

and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 3 illustrates the MT4C16271 MASKED WRITE operation.

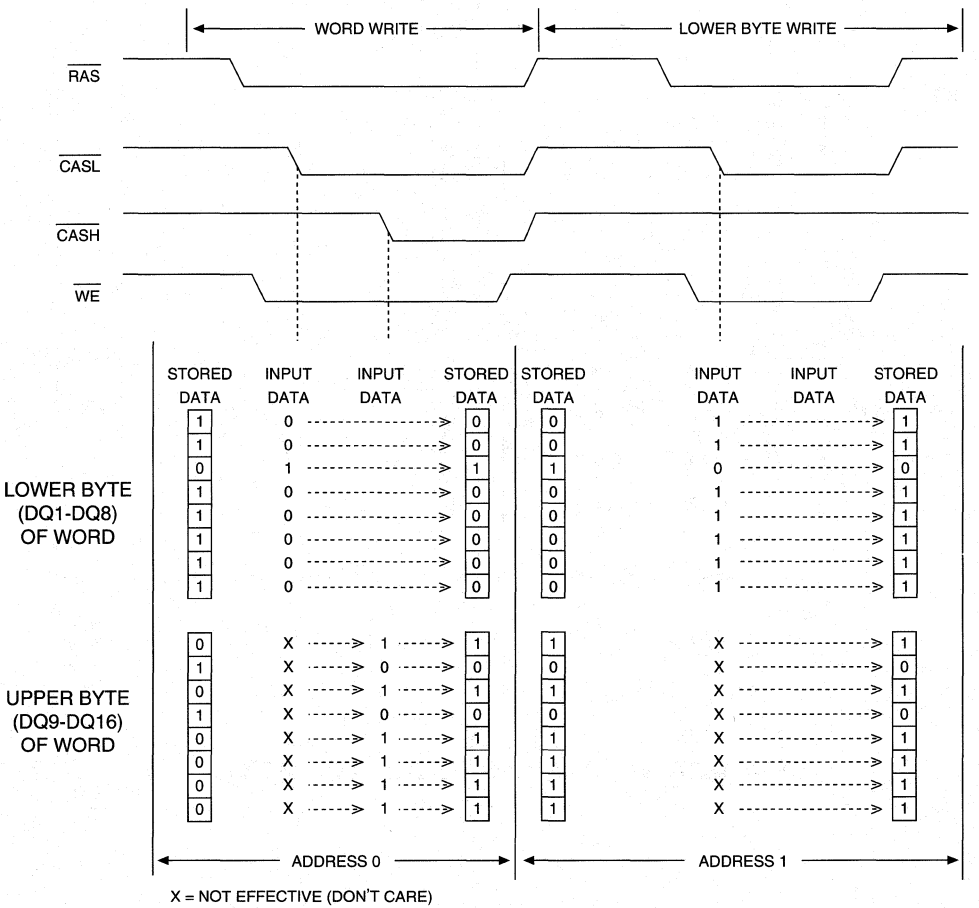


Figure 1
MT4C16270 WORD AND BYTE WRITE EXAMPLE

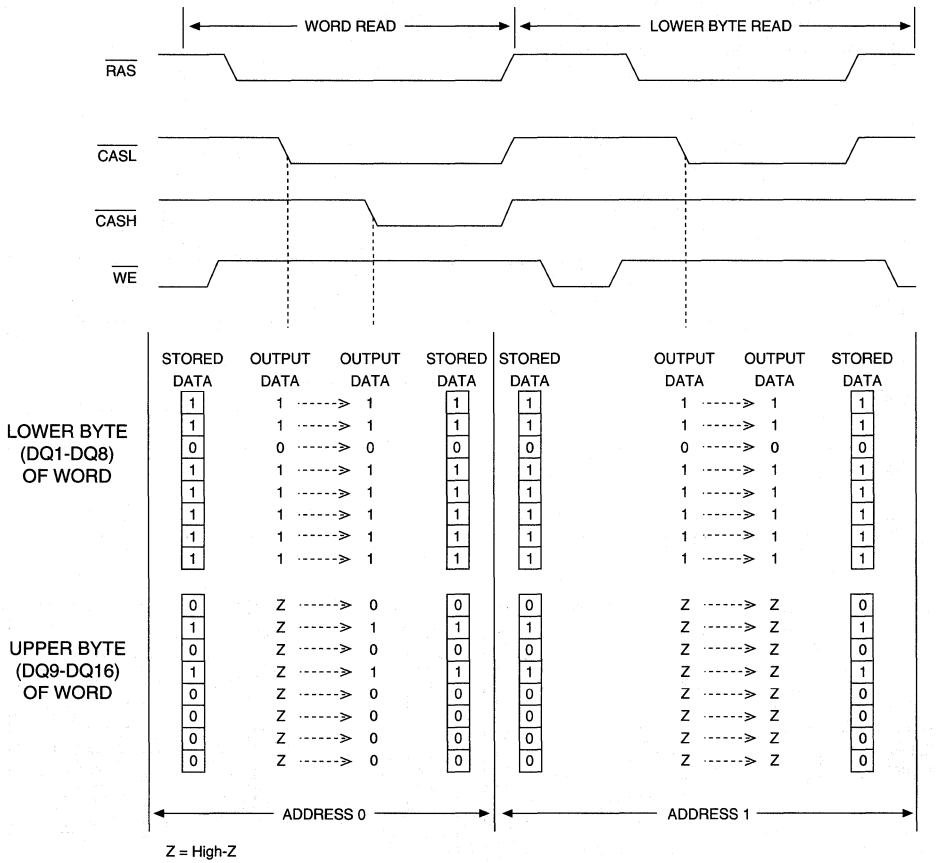


Figure 2
MT4C16270 WORD AND BYTE READ EXAMPLE

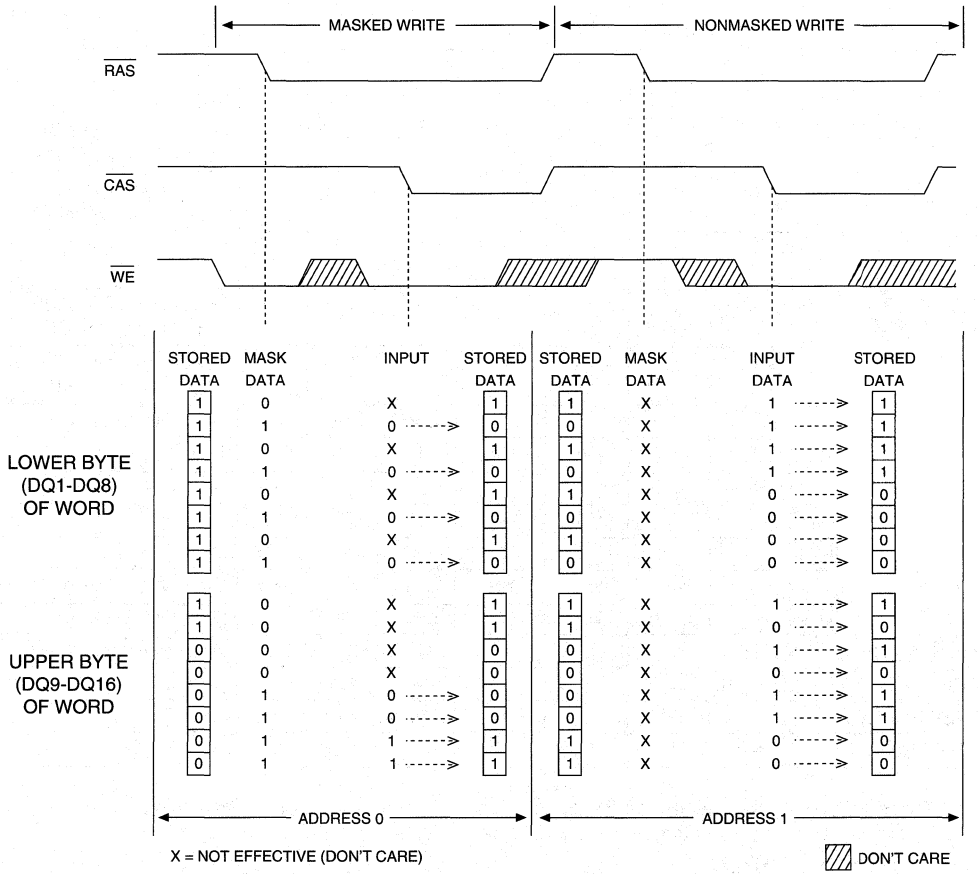


Figure 3
MT4C16271 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16270/1

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS signals must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C256K16E5 only). Refer to Figure 3.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	150	mA	3, 4, 41
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	110	100	mA	3, 4, 41
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	170	150	mA	3, 5, 41
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	160	140	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		ns	34
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15, 32
Output Enable time	^tOE		20		20	ns	23, 32
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	32
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	39
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	15	100,000	ns	38
$\overline{CAS}$ hold time	^tCSH	70		80		ns	31
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16, 35
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	10		10		ns	35
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17, 30
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	31
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	30
Column-address hold time	^tCAH	15		15		ns	30
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	26, 30
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19, 26, 31
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	32, 42

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	tOFF	3	15	3	15	ns	20, 29, 32, 42
Output disable time	tOD	3	15	3	15	ns	29, 40, 42
Write command setup time	tWCS	0		0		ns	21, 26, 30
Write command hold time	tWCH	10		10		ns	26, 39
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		ns	26
Write command pulse width	tWP	10		10		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		ns	26, 31
Data-in setup time	tDS	0		0		ns	22, 32
Data-in hold time	tDH	15		15		ns	22, 32
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	95		105		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		ns	21, 30
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8	ns	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		ns	5, 30
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		10		ns	5, 31
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE)	tWRH	15		15		ns	26
Mask data to $\overline{RAS}$ setup time	tMS	0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	tCLCH	10		10		ns	33
Data output hold after $\overline{CAS}$ LOW	tCOH	5		5		ns	

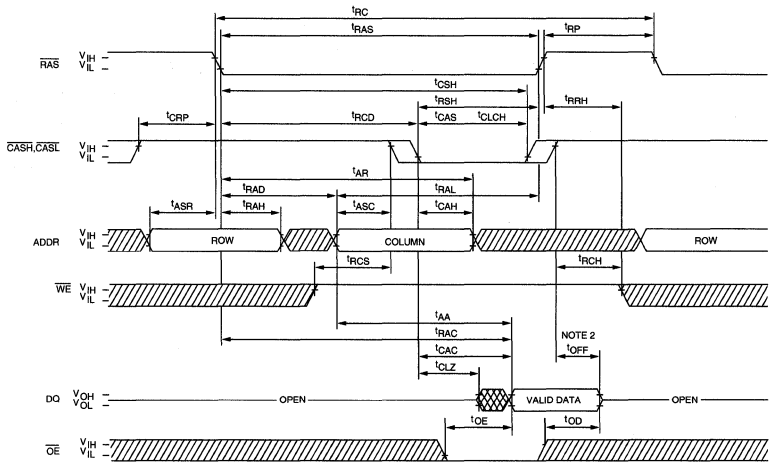
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C16271 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met.
29. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.

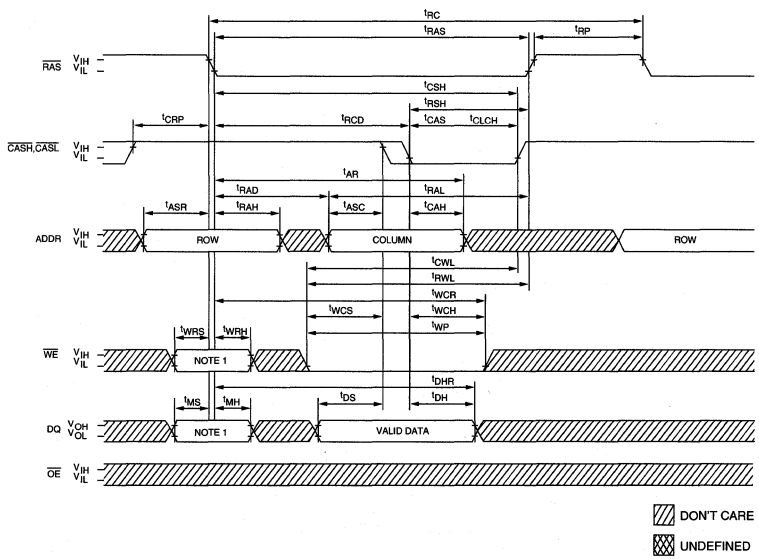
NOTES (continued)

30. The first $\overline{CAS}$x edge to transition LOW.
31. The last $\overline{CAS}$x edge to transition HIGH.
32. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
33. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
36. First DQs controlled by the first $\overline{CAS}$x to go LOW.
37. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
38. Each $\overline{CAS}$x must meet minimum pulse width.
39. Last $\overline{CAS}$x to go LOW.
40. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
41. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
42. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE



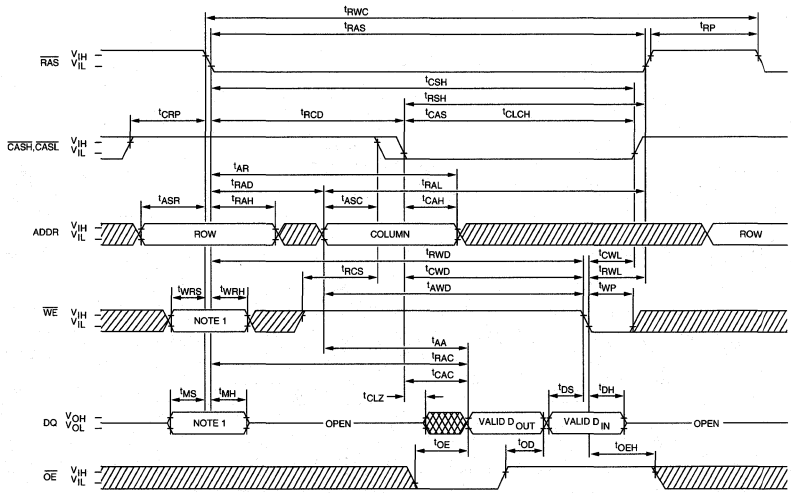
EARLY-WRITE CYCLE



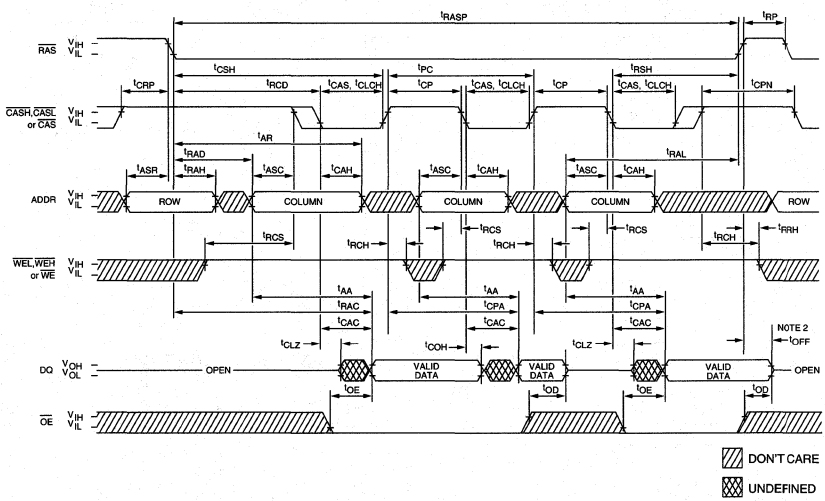
NOTE: 1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.

2. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

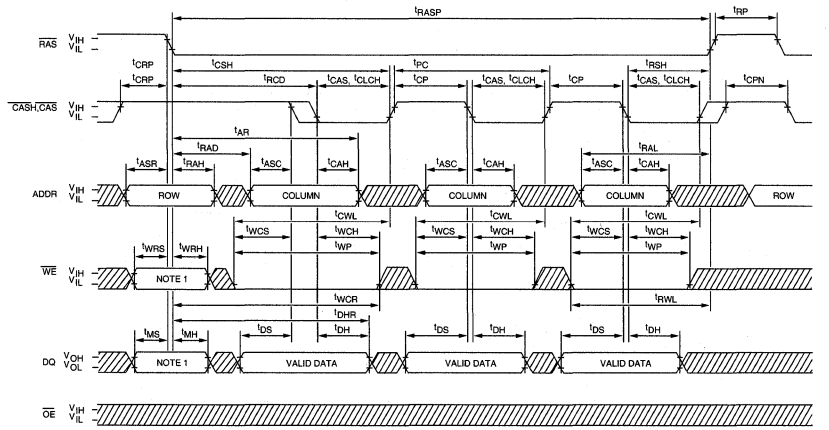


FAST-PAGE-MODE READ CYCLE with EXTENDED DATA-OUT

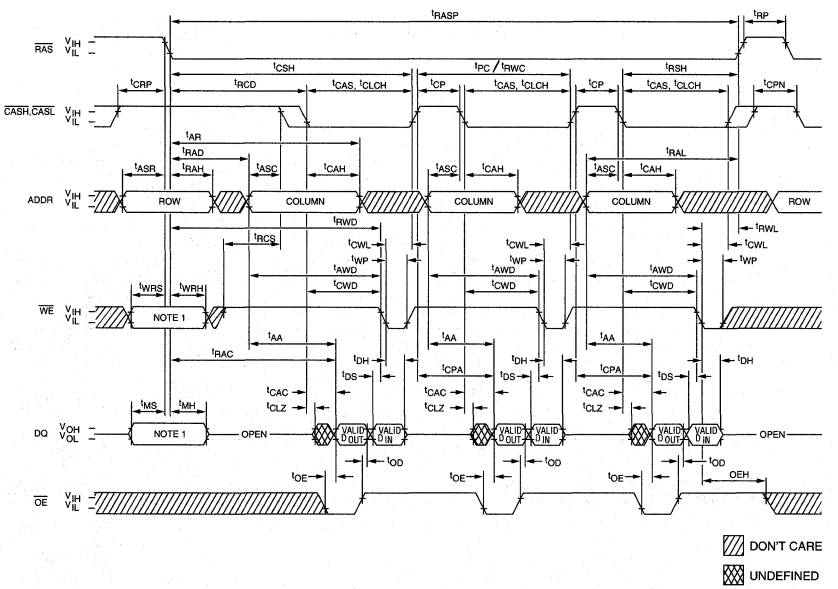


NOTE:
1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.
2. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

FAST-PAGE-MODE EARLY-WRITE CYCLE

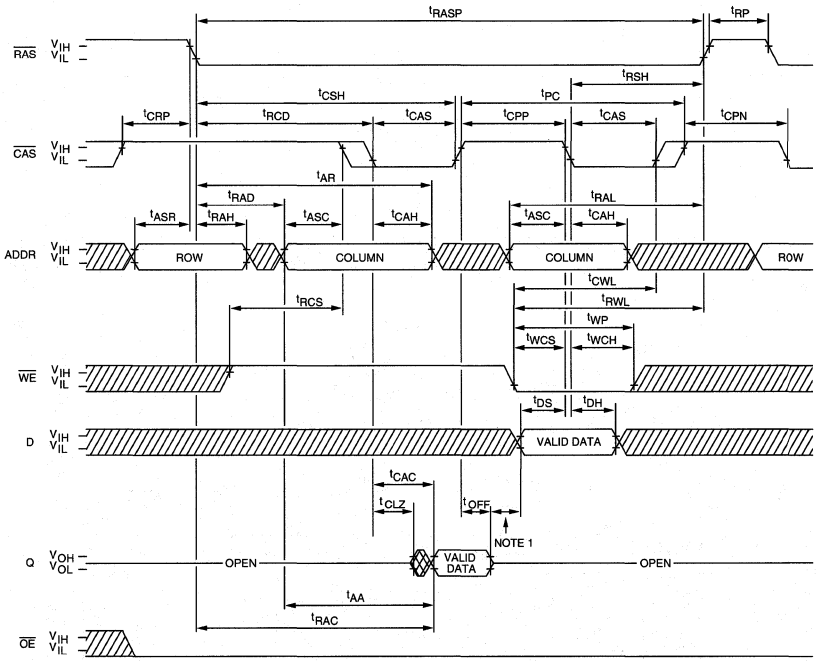


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



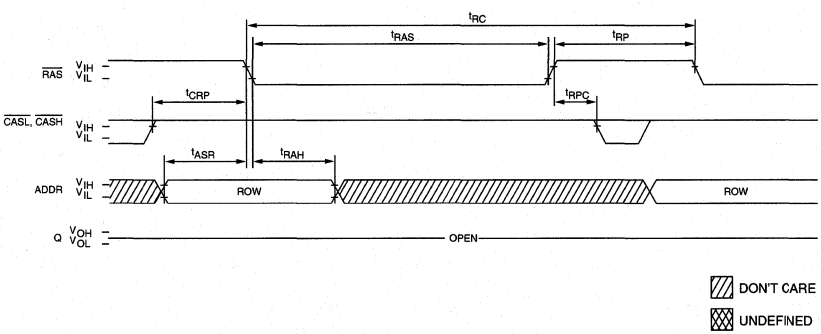
NOTE: 1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

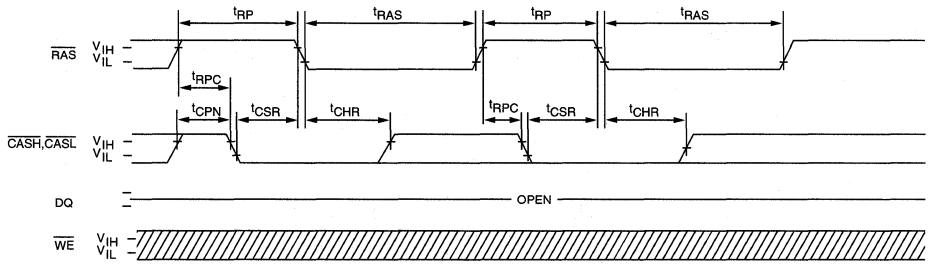


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

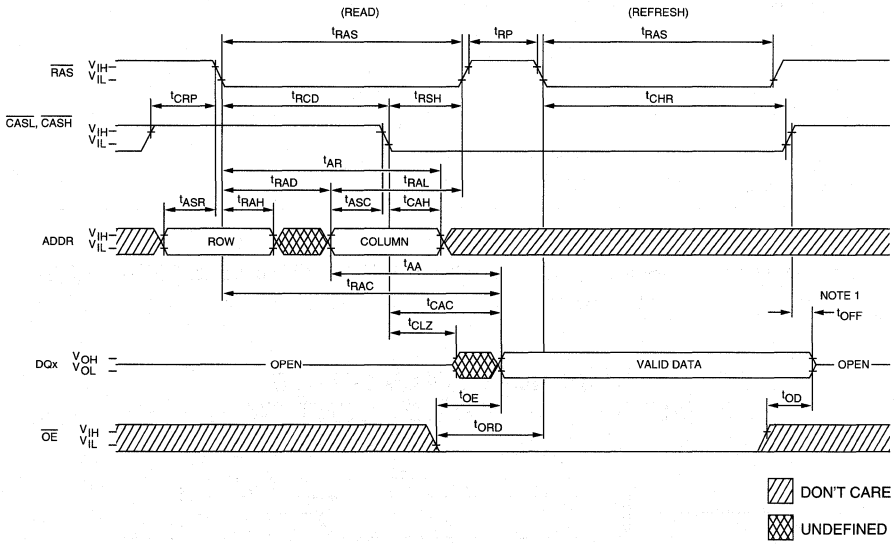
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

WIDE DRAM

256K x 16 DRAM

ASYMMETRICAL, FAST-PAGE-MODE

FEATURES

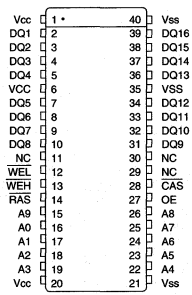
- Industry-standard x16 pinouts, timing, functions and packages
- Address entry: ten row-addresses, eight column-addresses
- High-performance CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle, 256 locations wide
- BYTE WRITE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C16261 only)

OPTIONS — MARKING

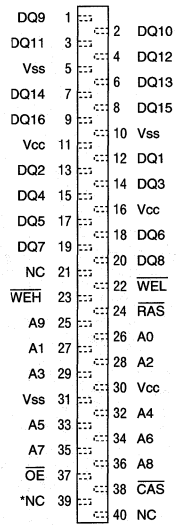
- Timing
  - 70ns access — -7
  - 80ns access — -8
- MASKED WRITE
  - Not Available — 16260
  - Available — 16261
- Packages
  - Plastic SOJ (400mil) — DJ
  - Plastic TSOP (400mil) — TG
  - Plastic ZIP (475mil) — Z
- Part Number Example: MT4C16260DJ-7

PIN ASSIGNMENT (Top View)

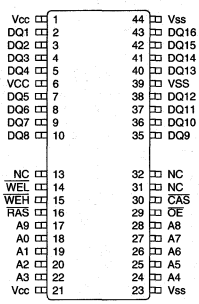
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-2)



40-Pin TSOP (SDE-2)



GENERAL DESCRIPTION

The MT4C16260 and MT4C16261 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. Each word or byte is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) first, 8 bits second (A0-A7). $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 8 bits.

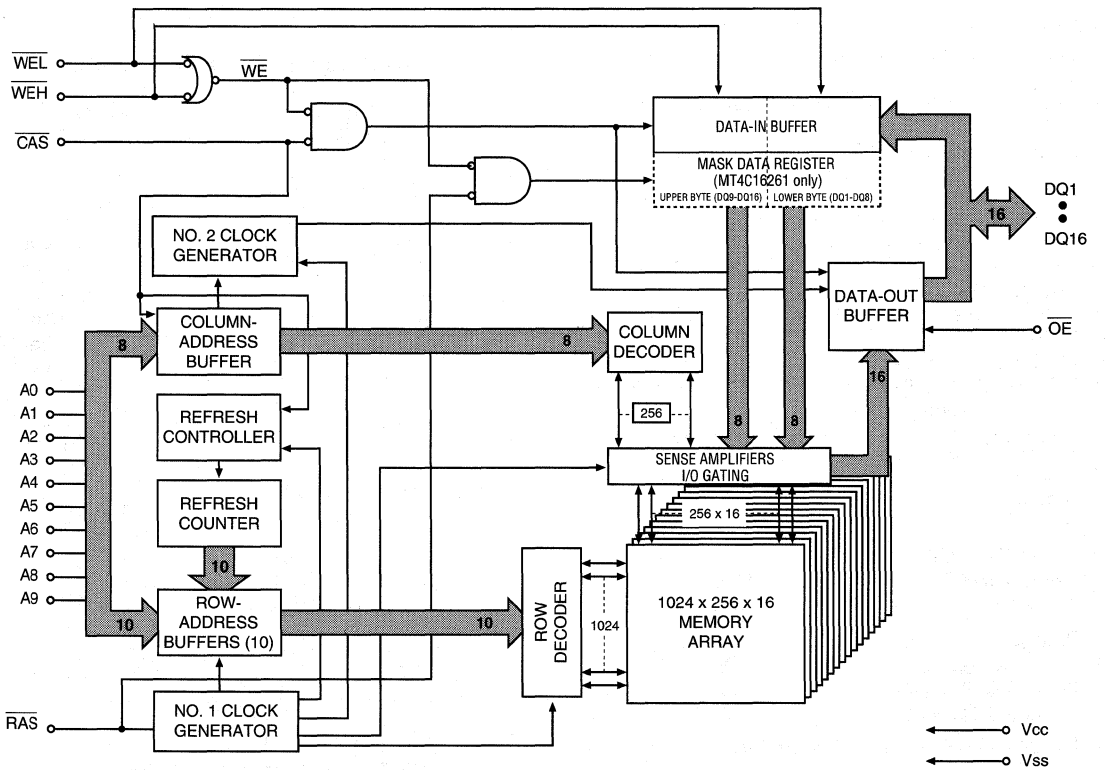
The MT4C16260 and MT4C16261 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16261 is able to perform WRITE-PER-BIT accesses.

The MT4C16260 and MT4C16261 function in the same manner in that $\overline{WEL}$ and $\overline{WEH}$ control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function identically to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$.

The $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16261 has NONPERSISTENT, MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option.
28	30	38	$\overline{CAS}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ / $\overline{WEH}$ HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$	Input	Write Enable Upper Byte: $\overline{WEH}$ is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16261, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
12	14	22	$\overline{WEL}$	Input	Write Enable Lower Byte: $\overline{WEL}$ is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16261, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles.
11, 15, 30, 29	13, 17, 31	21, 25, 40, 39	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	V_{CC}	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. $\overline{RAS}$ is used to latch the first 10 bits (A0-A9) and $\overline{CAS}$ the latter 8 bits (A0-A7).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

A READ or WRITE cycle is selected with either $\overline{WEL}$ or $\overline{WEH}$ performing the $\overline{WE}$ function. The $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower byte WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ will select an upper byte WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a word WRITE cycle.

The MT4C16260/1 may be viewed as two 256K x 8 DRAMS that have common input controls, with the exception of the $\overline{WE}$ inputs. Figure 1 illustrates the MT4C16260/1 BYTE and WORD WRITE cycles.

MASKED WRITE ACCESS CYCLE (MT4C16261 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

For NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 2 illustrates the MT4C16261 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

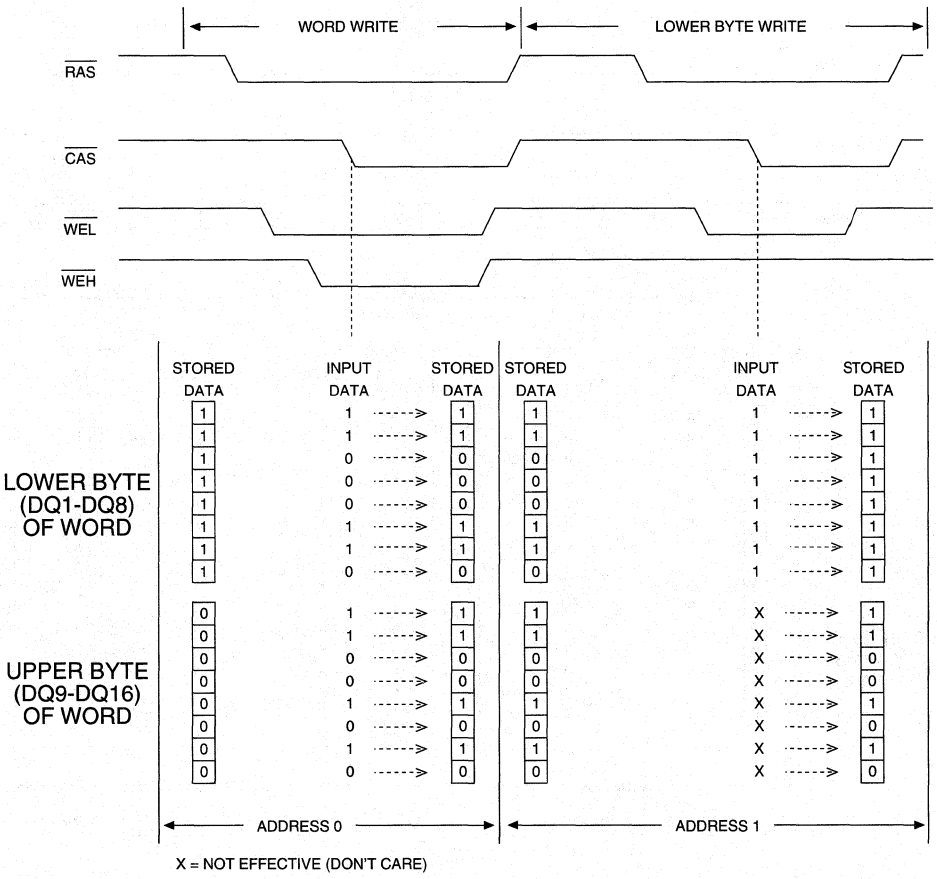


Figure 1
MT4C16260/1 WORD AND BYTE WRITE EXAMPLE

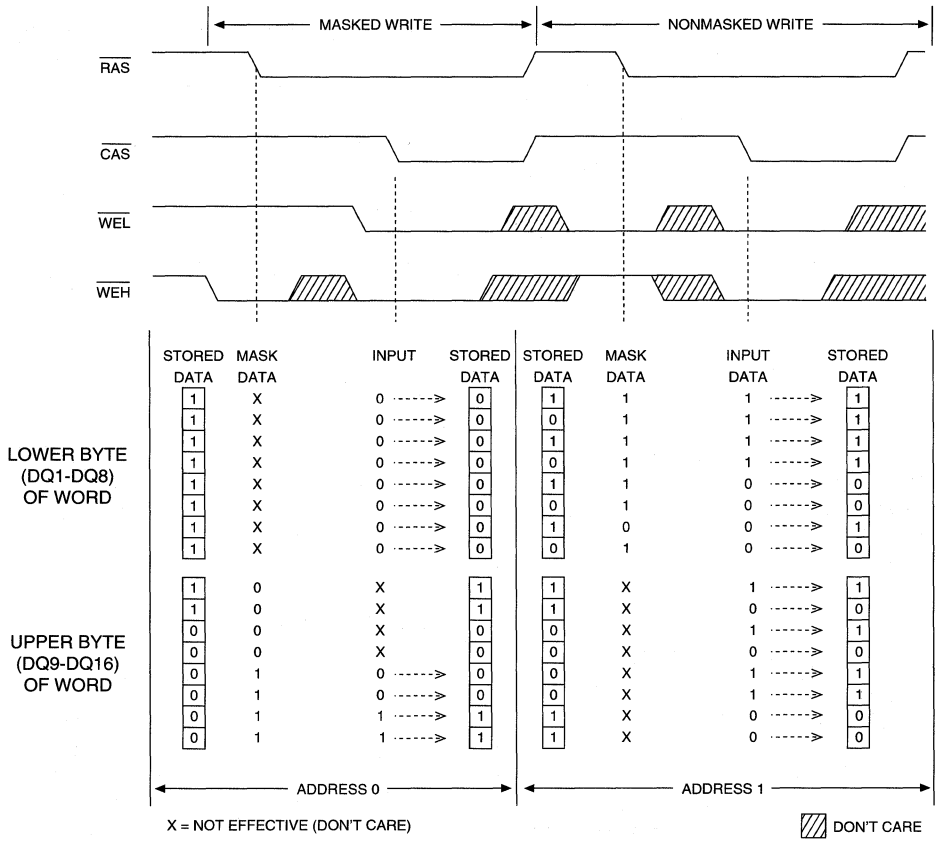


Figure 2
MT4C16261 MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

TRUTH TABLE: MT4C16260/1

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
FAST-PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16261 only). Refer to figure 2.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0 V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	140	130	mA	3, 4, 30
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	140	130	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	140	130	mA	3

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15
Output Enable time	^tOE		20		20	ns	
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	31

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

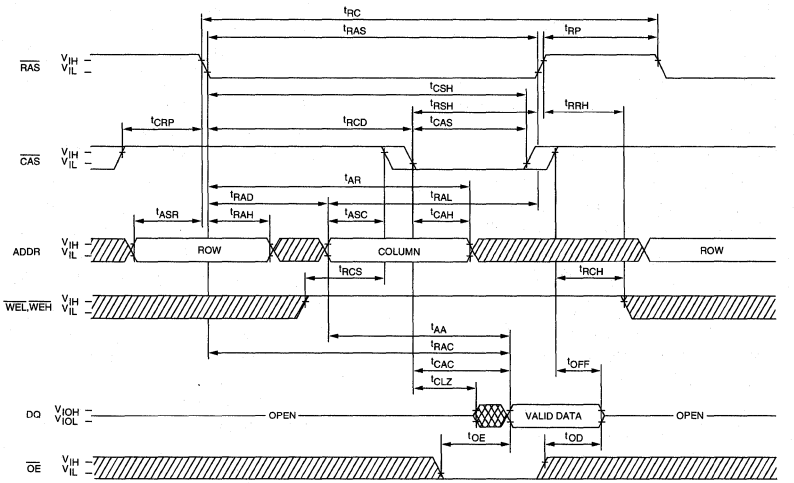
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	3	15	3	15	ns	20, 29, 31
Output disable time	^tOD	3	15	3	15	ns	29, 31
Write command setup time	^tWCS	0		0		ns	21, 26
Write command hold time	^tWCH	10		10		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	26
Write command pulse width	^tWP	10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	26
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		7ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE)	^tWRH	15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Last $\overline{CAS}$ going low to first $\overline{CAS}$ returning high	^tCLCH	10		10		ns	

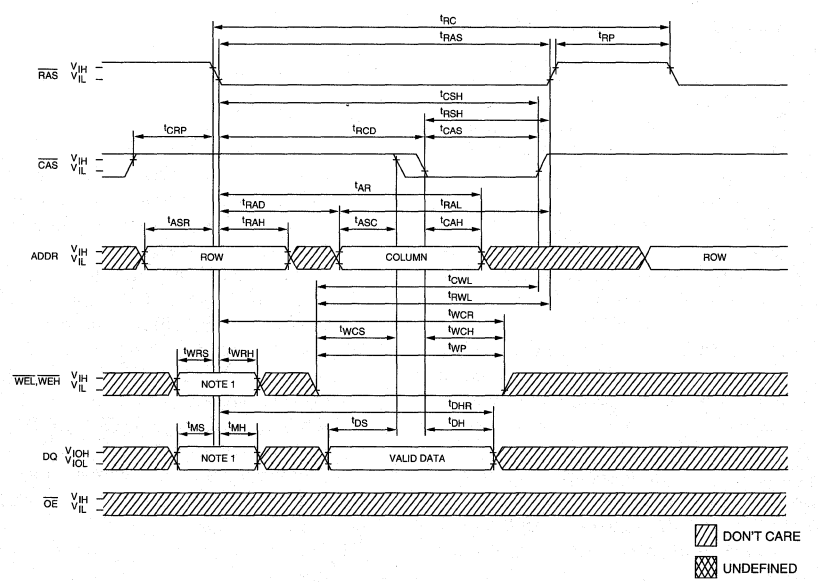
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or $\overline{CBR}$) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tRAF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate. $\overline{WE}$ determines either EARLY-WRITE (WCS), LATE-WRITE (RWD, AWD and CWD) or an indeterminate (WCS or RWD, AWD and CWD not met) cycle when $\overline{WE}$ goes LOW in reference to $\overline{CAS}$ going LOW.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW.
27. MT4C16261 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of OE. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
31. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE

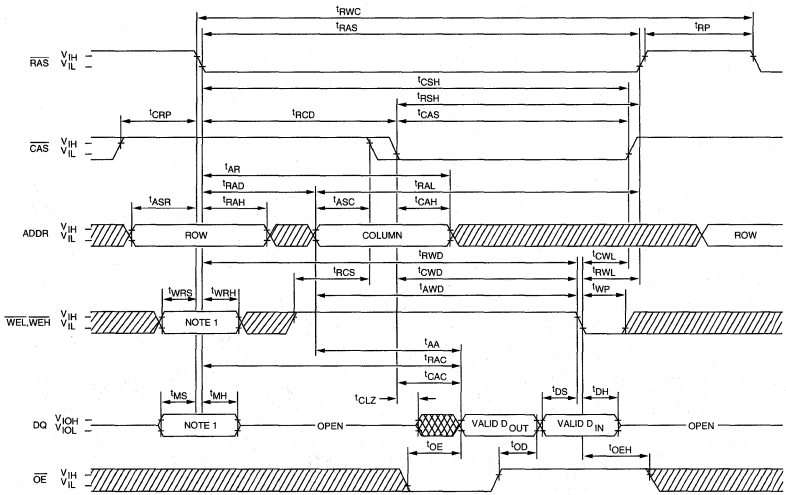


EARLY-WRITE CYCLE

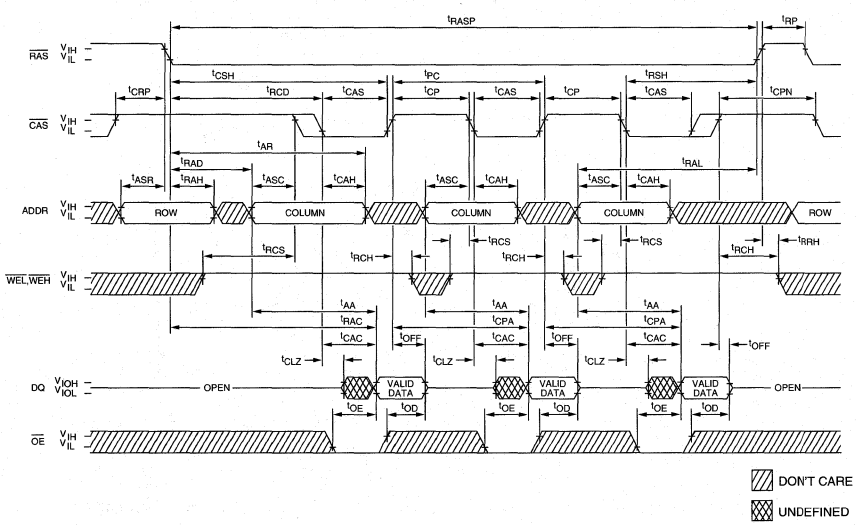


NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

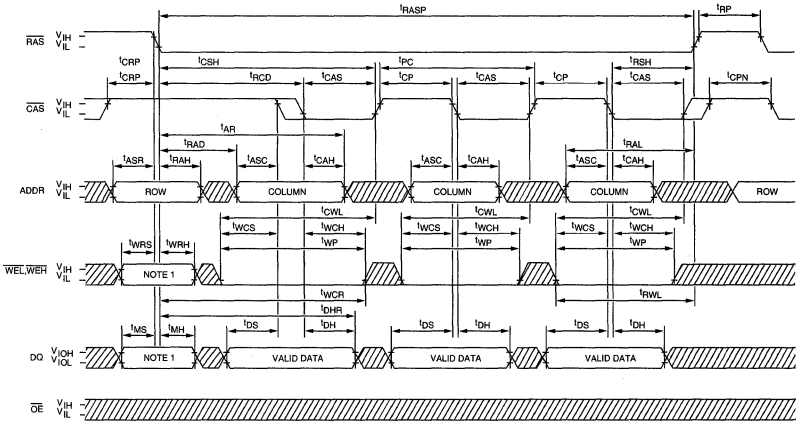


FAST-PAGE-MODE READ CYCLE

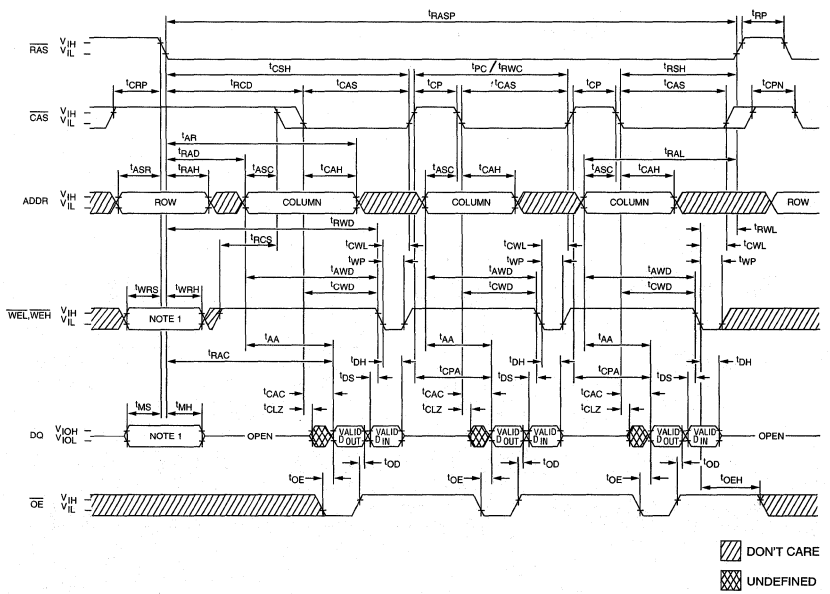


NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

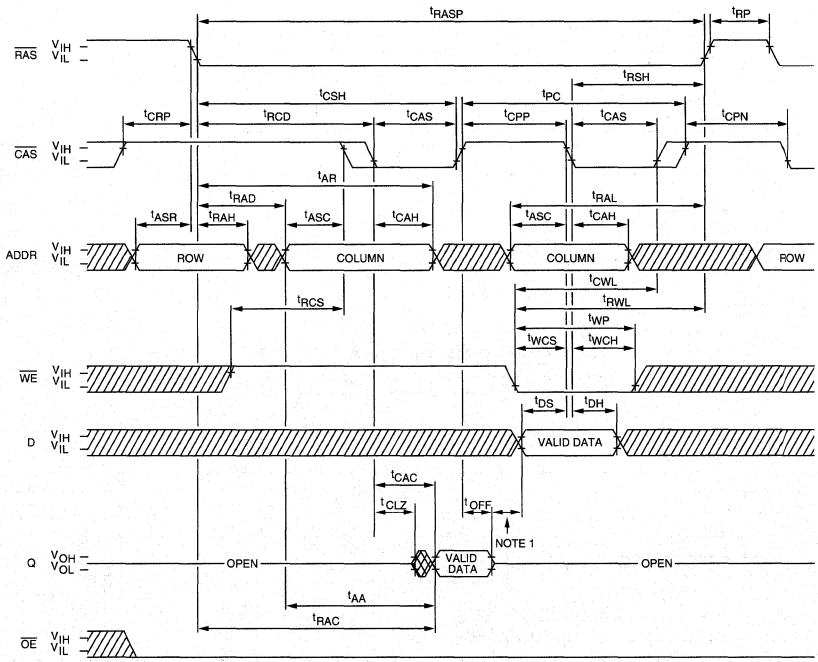


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



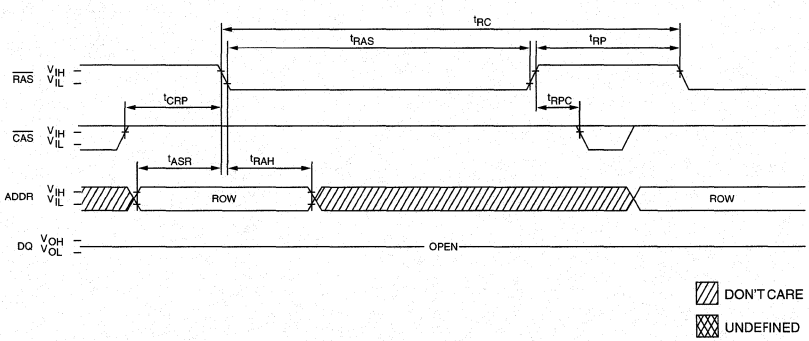
NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

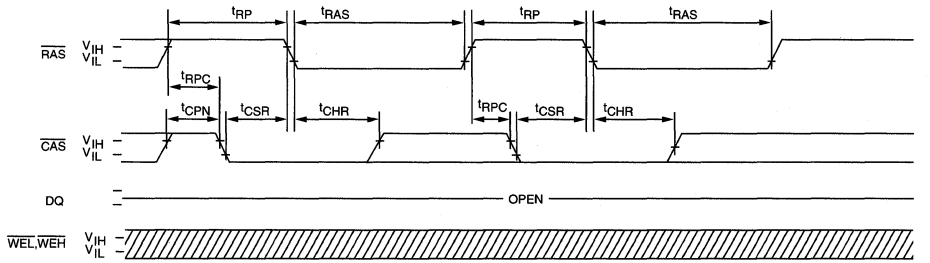


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

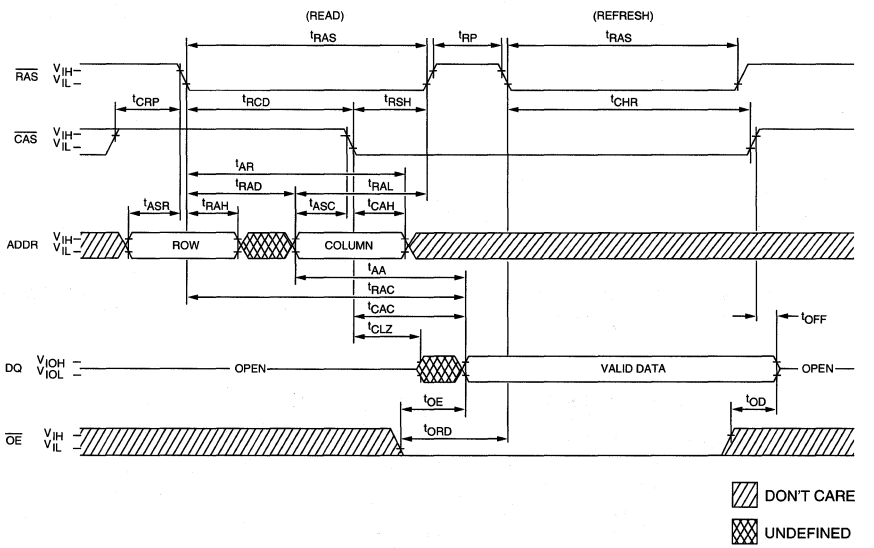
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9, OE; WEL and WEH = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ = HIGH; $\overline{OE}$=LOW)



MICRON
SEMICONDUCTOR, INC.

VRAM SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins				
				Standby	Active	SOJ	SOP	TSOP	ZIP	Page
256K x 4	FP	MT42C4256	60, 70, 80	15mW	275mW	28	-	-	28	2-1
128K x 8	FP	MT42C8128	60, 70, 80	15mW	275mW	40	-	-	-	2-37
256K x 8	FP, DW	MT42C8254	70, 80	10mW	300mW	40	-	40/44	-	2-75
256K x 8	FP	MT42C8255	70, 80	10mW	300mW	40	-	40/44	-	2-107
256K x 8	FP, EDO	MT42C8256	60, 70, 80	10mW	300mW	40	-	40/44	-	2-139
256K x 8	FP	MT42C8257	60, 70, 80	10mW	300mW	40	-	40/44	-	2-181
256K x 16	FP, EDO, DW	MT42C256K16A1	60, 70, 80	TBD	TBD	-	64	70	-	2-221
256K x 16	FP, DW	MT42C256K16C1	60, 70, 80	TBD	TBD	-	64	70	-	2-265
256K x 16	FP, DC	MT42C256K16C2	60, 70, 80	TBD	TBD	-	64	70	-	2-267

FP = FAST-PAGE-MODE, EDO = Extended Data-Out, DW = Dual WE, DC = Dual CAS

VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- Optional FAST-PAGE-MODE access cycles
- Dual-port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times: 70ns random, 22ns serial
  60ns random, 18ns serial*

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

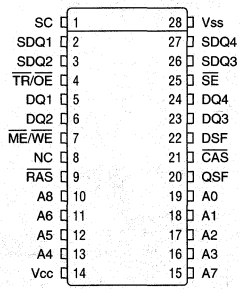
OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])
  60ns, 18ns/18ns -6*
  70ns, 22ns/22ns -7
  80ns, 25ns/25ns -8
- Packages
  Plastic SOJ (400 mil) DJ
  Plastic ZIP (375 mil) Z
- Part Number Example: MT42C4256DJ-7

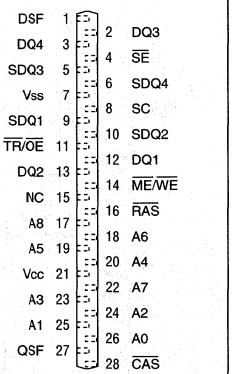
*60ns (-6) specifications are preliminary; consult factory for availability.

PIN ASSIGNMENT (Top View)

28-Pin SOJ (SDB-1)



28-Pin ZIP (SDA-1)



GENERAL DESCRIPTION

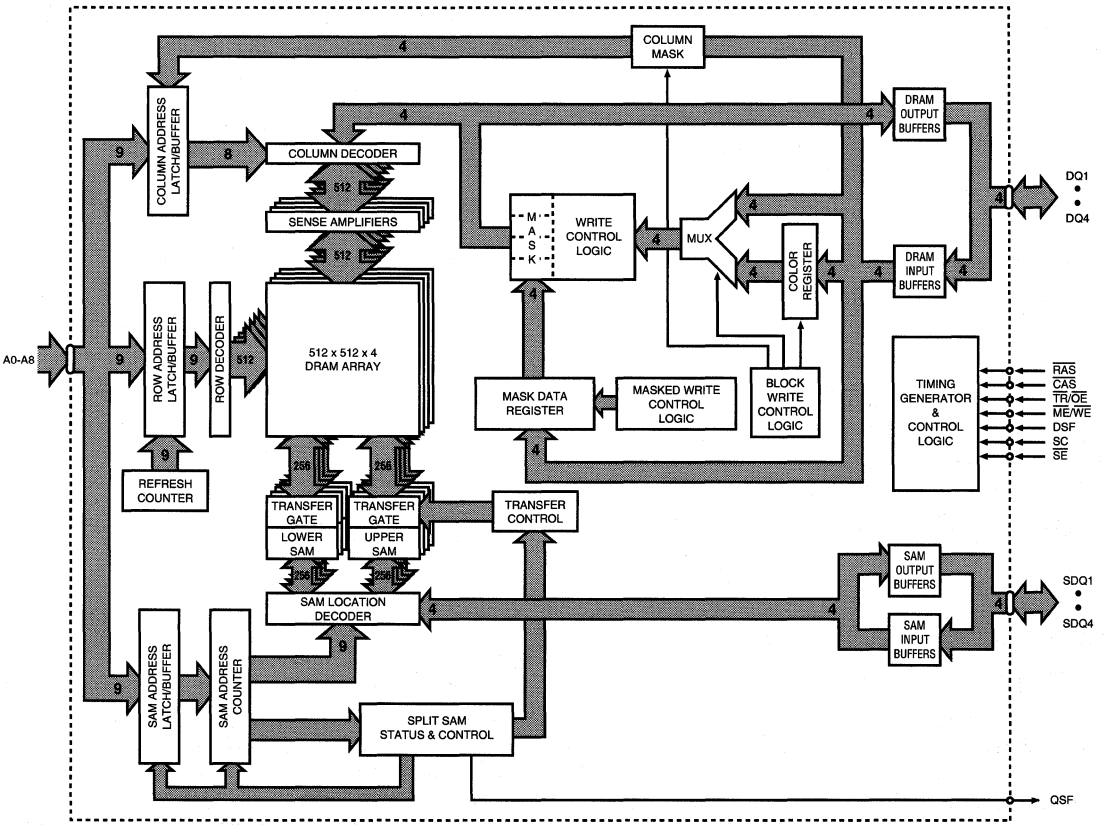
The MT42C4256 is a high-speed, dual-port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed by a 4-bit-wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is similar to the MT4C4256 (256K x 4 DRAM). Four 512-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths; the 4-bit random access I/O port, the four internal 512-bit-wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. Refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data used in raster graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable and must fall for initiation of any DRAM or TRANSFER cycle.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1-SDQ4	Input/ Output	Serial Data I/O: Input, output, or High-Z.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed: LOW if address is 0-255, HIGH if address is 256-511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	V_{CC}	Supply	Power Supply: +5V ±10%
28	7	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 may be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C4256 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C4256 supports CBR, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY refresh cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR refresh cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C4256 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

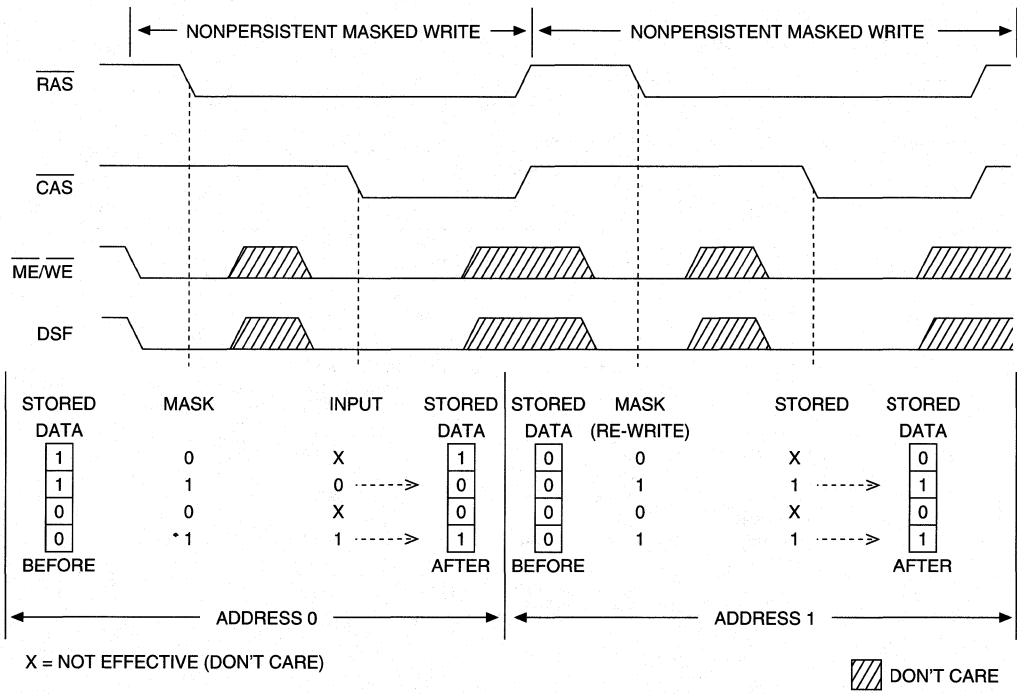


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations may be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

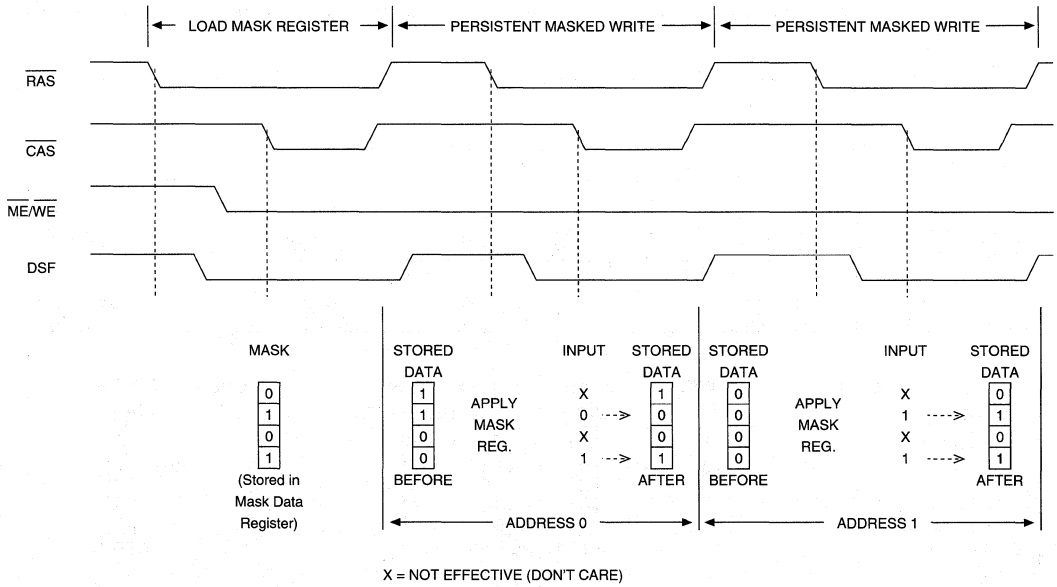


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

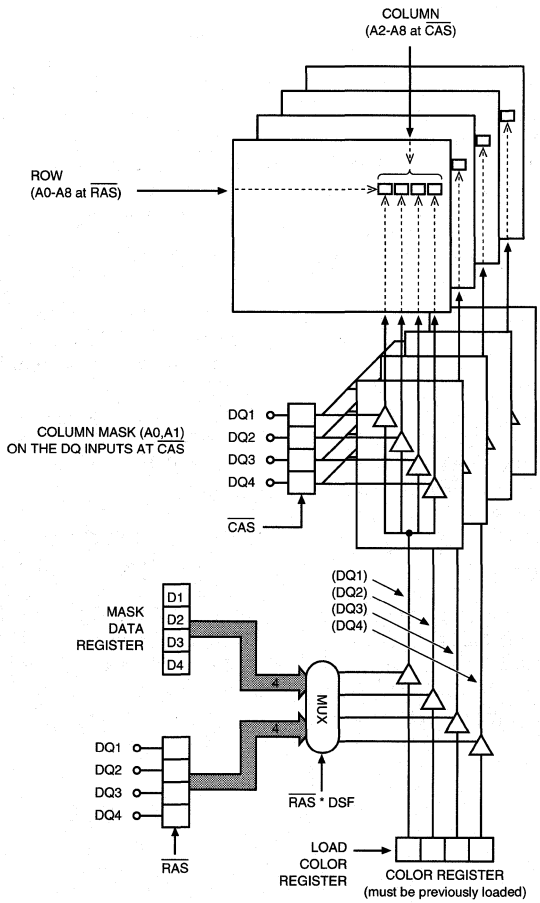


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE, except that the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASKED cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform the NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes or column locations may be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

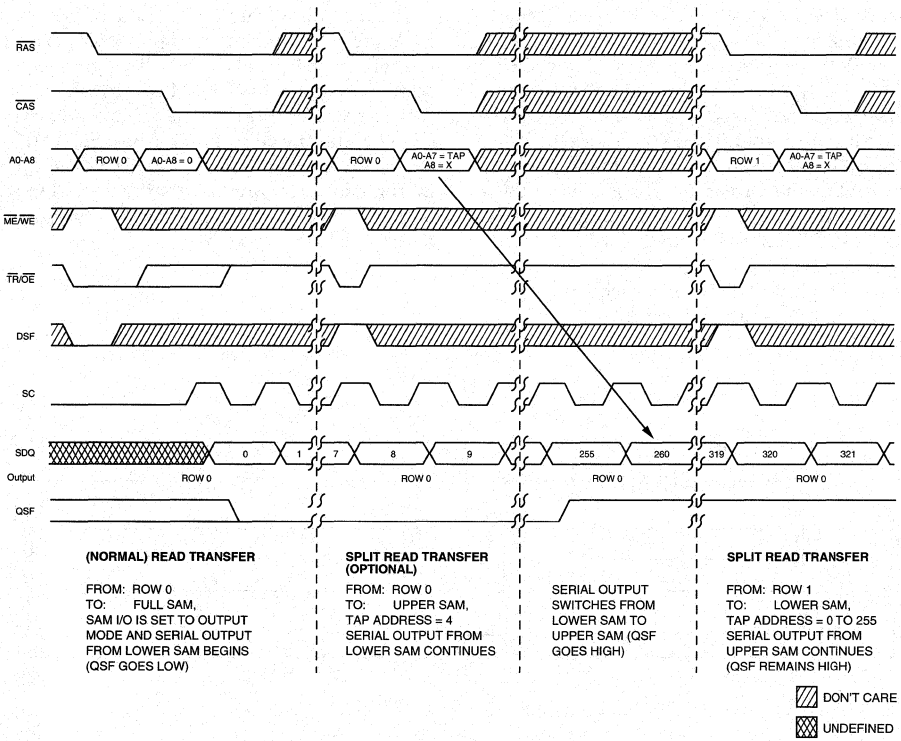


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. An SRT does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SRT cycles to set SAM I/O direction and provide a reference to which half of the SAM the access will begin. Then SRTs may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need be done only if the Tap for the upper half is $\neq 0$. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1), the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half a Tap address of "0" will be used. Access will start at 0 if going to the lower half, or 256 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

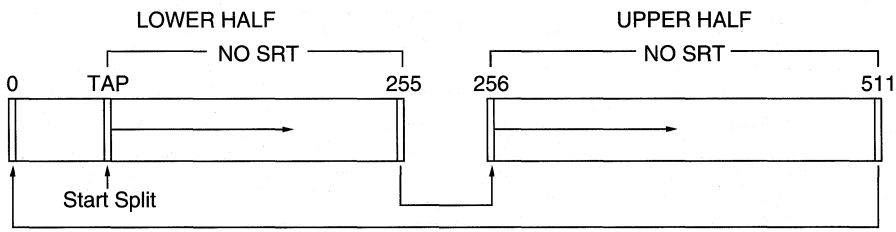


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C4256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ4[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS,WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CBR REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE and LOAD COLOR REGISTER), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	105	95	85	mA	3, 4 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC2}	95	85	75	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	105	95	85	mA	3, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	105	95	85	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	115	105	95	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC9}	170	150	130	mA	3, 4, 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC10}	160	140	120	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	65	55	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC12}	170	150	130	mA	3, 4, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	170	150	130	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	190	160	130	mA	3, 4

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	148		170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	83		90		95		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	18	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	42	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	12		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	40		45		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer turn-off delay	tOFF	3	12	3	12	3	15	ns	20, 23
Output disable	tOD	3	10	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		10		10		ns	25
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	tROH	0		0		0		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		45		55		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	18		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	18		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	12		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	50		55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	38		40		45		ns	21
Transition time (rise or fall)	^tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	tRTH	65	10,000	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	tCTH	25		25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	tTSL	5		5		5		ns	
$\overline{TR}/(\overline{OE})$ to $\overline{RAS}$ HIGH hold time	tTRD	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	tTRW	15		20		20		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	tTSD	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	tREH	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	12		15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	12		15		15		ns	
SC to QSF delay time	tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	tRQD		70		75		75	ns	
DSF to $\overline{RAS}$ hold time	tFHR	40		45		55		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	12		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		25		25		25	ns	
$\overline{CAS}$ to QSF delay time	tCQD		30		35		35	ns	
$\overline{RAS}$ to first SC delay	tRSD	70		80		80		ns	
$\overline{CAS}$ to first SC delay	tCSD	25		30		30		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

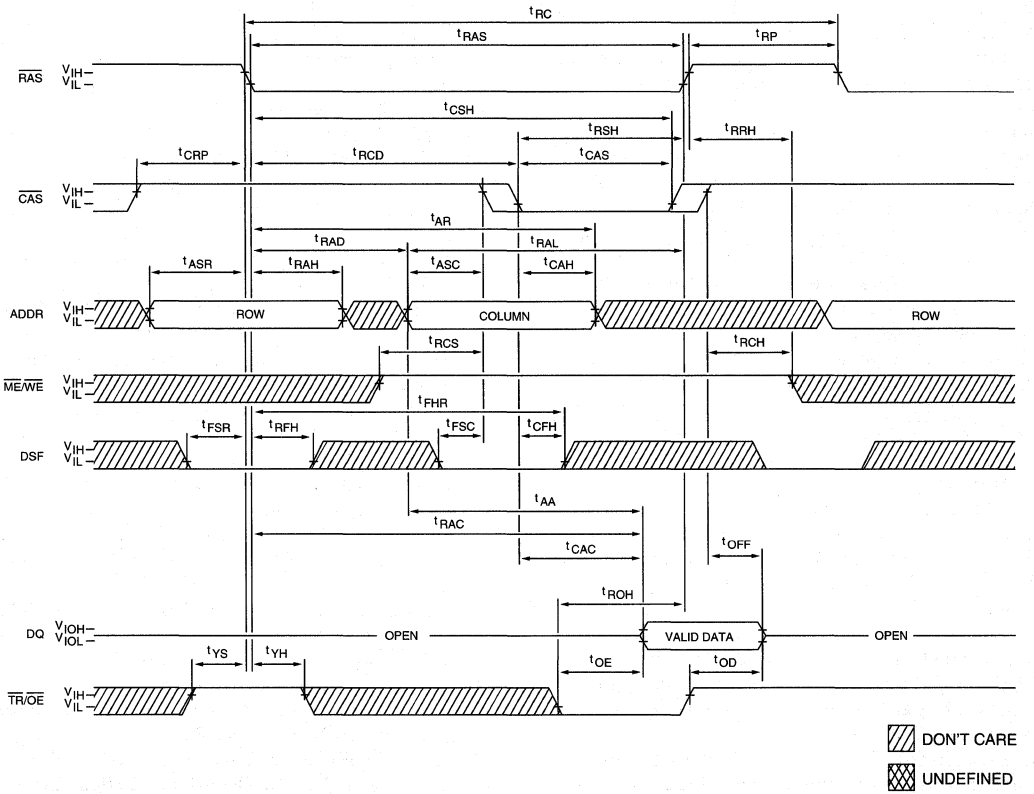
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	18		22		25		ns	
Access time from SC	^tSAC		18		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	7		8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		10		ns	
Access time from $\overline{SE}$	^tSEA		12		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		10		ns	
$\overline{SE}$ pulse width	^tSE	7		8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	10	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	9		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

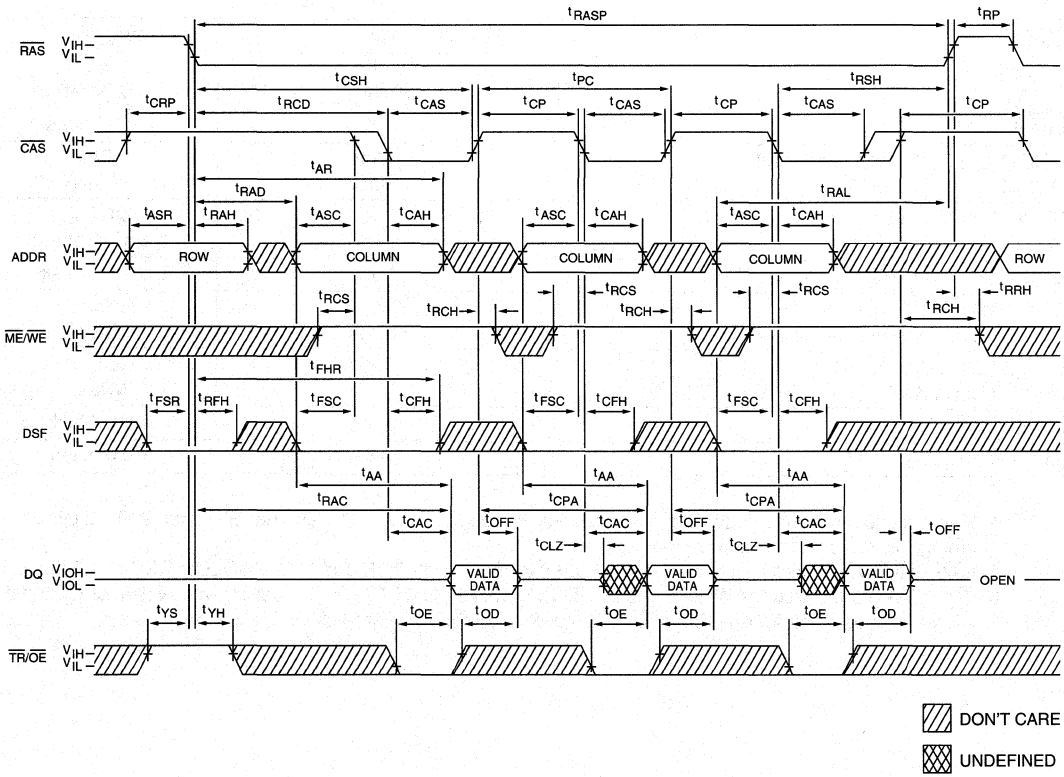
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ4) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OD, ^{t}OFF and ^{t}SEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^{t}WCS \leq {}^{t}WCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^{t}OD and ^{t}OEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. ^{t}OD and ^{t}OEH must be met in LATE-WRITE and READ-MODIFY-WRITE cycles ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^{t}SAC is MAX at 70° C and 4.5V Vcc; ^{t}SOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^{t}SOH = ^{t}SAC - output transition time; this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



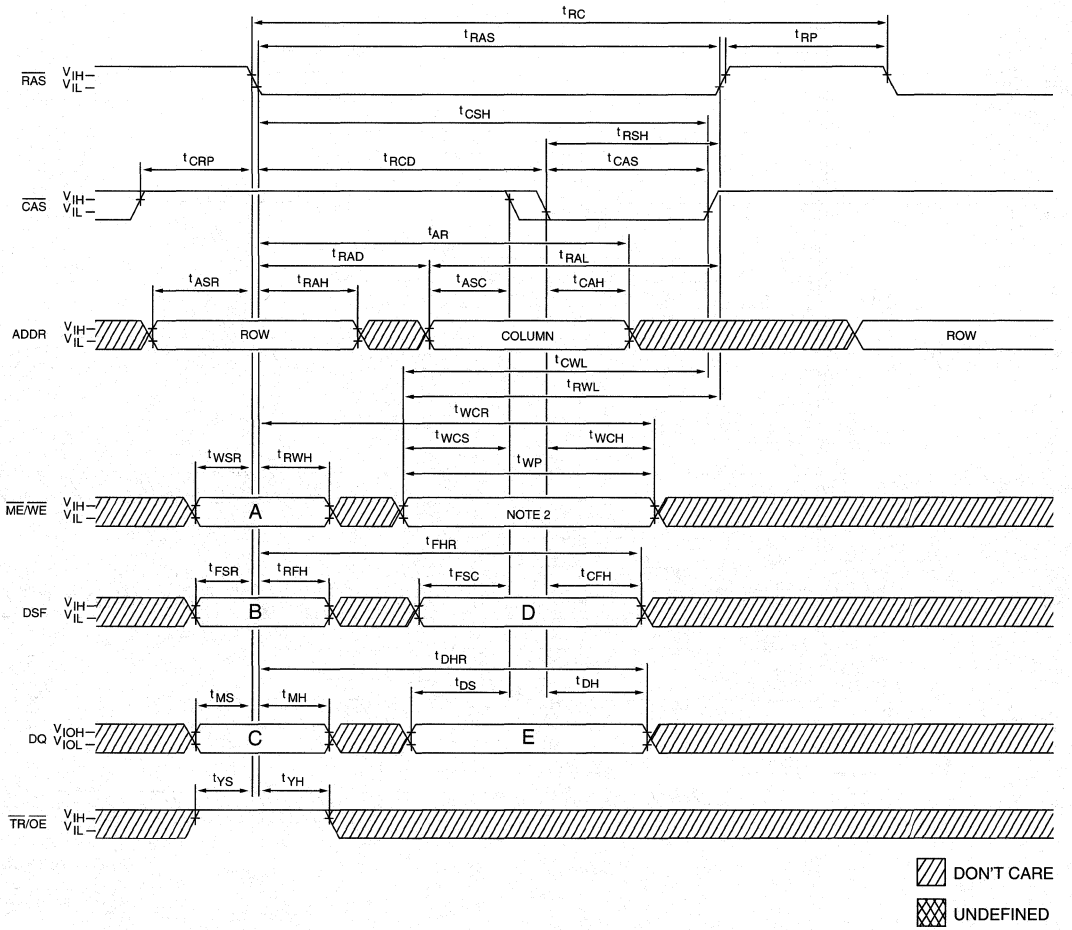
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later (Except for BLOCK WRITE and LOAD COLOR REGISTER).
3. $\overline{WE}$ = "don't care" BLOCK WRITE and LOAD COLOR REGISTER. The DQ column-mask data or color data will be latched at the falling edge of $\overline{CAS}$, regardless of the state of $\overline{ME}/\overline{WE}$.

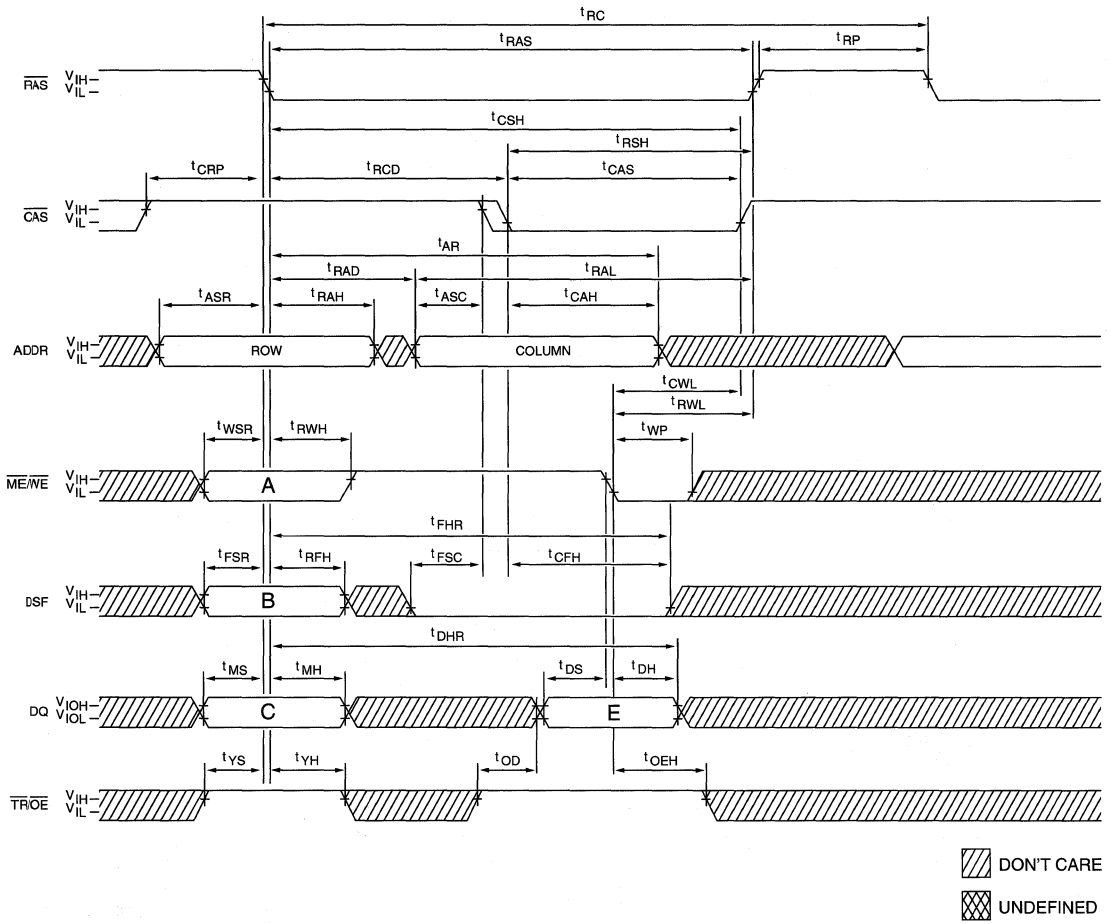
DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For Block Write, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

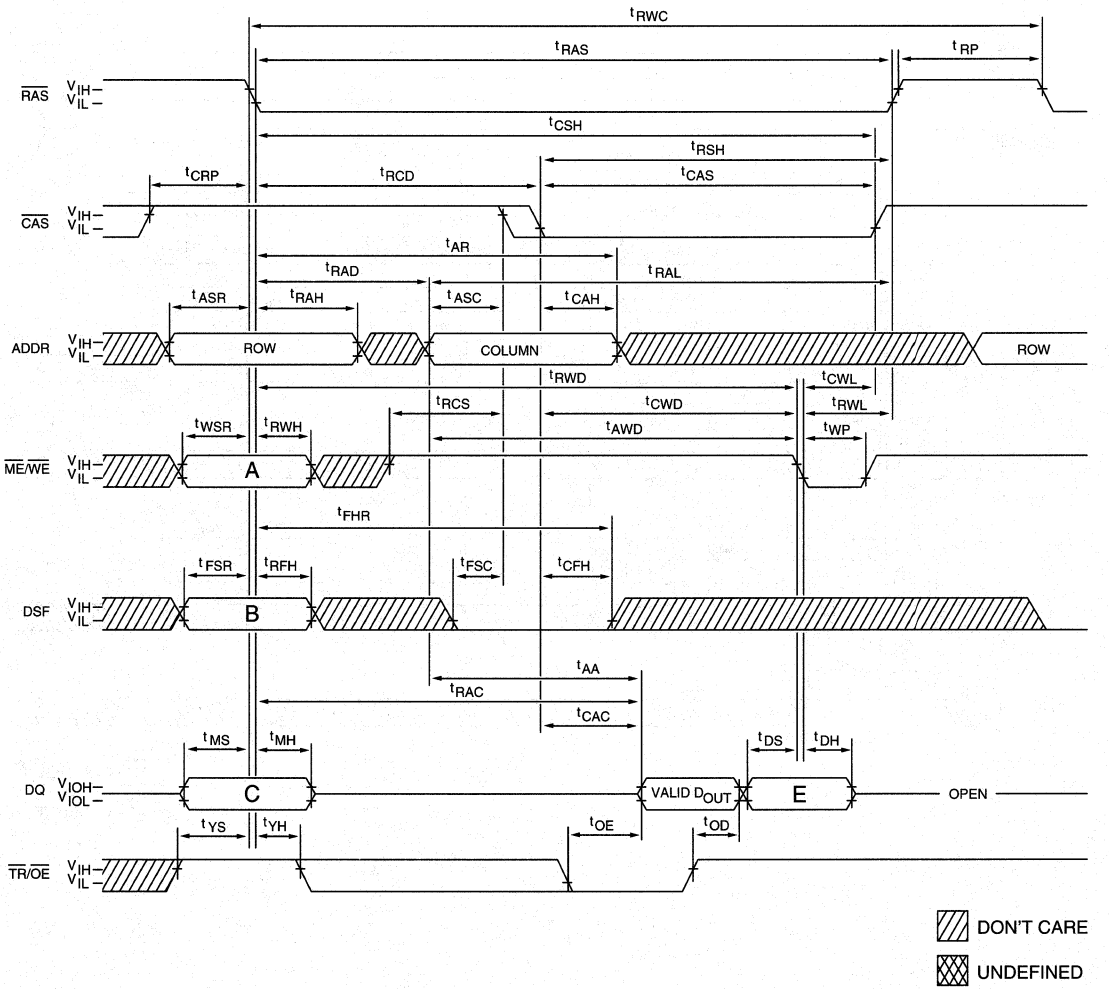
VRAM

DRAM LATE-WRITE CYCLE [1]



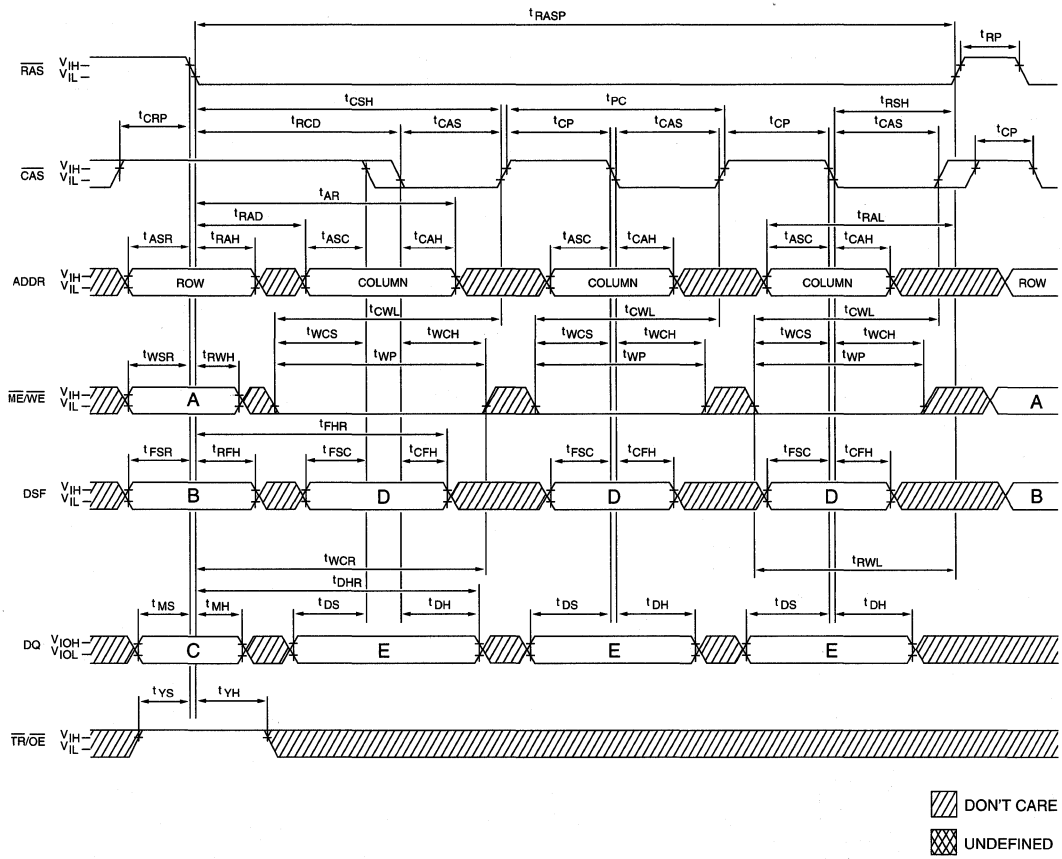
NOTE: 1. The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



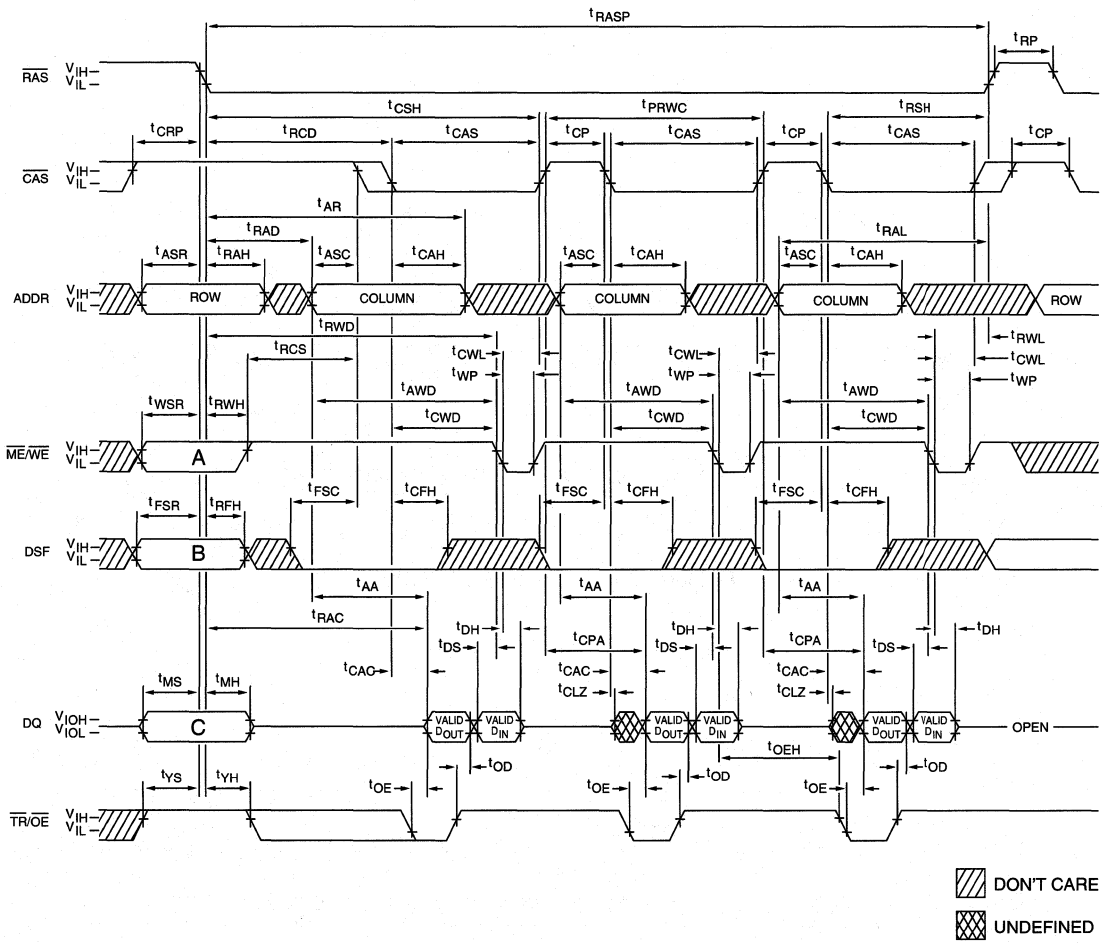
NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



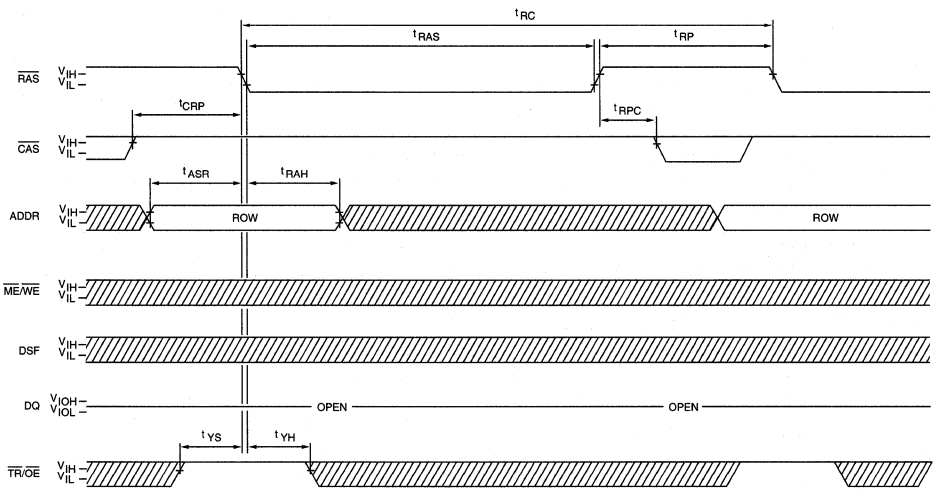
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

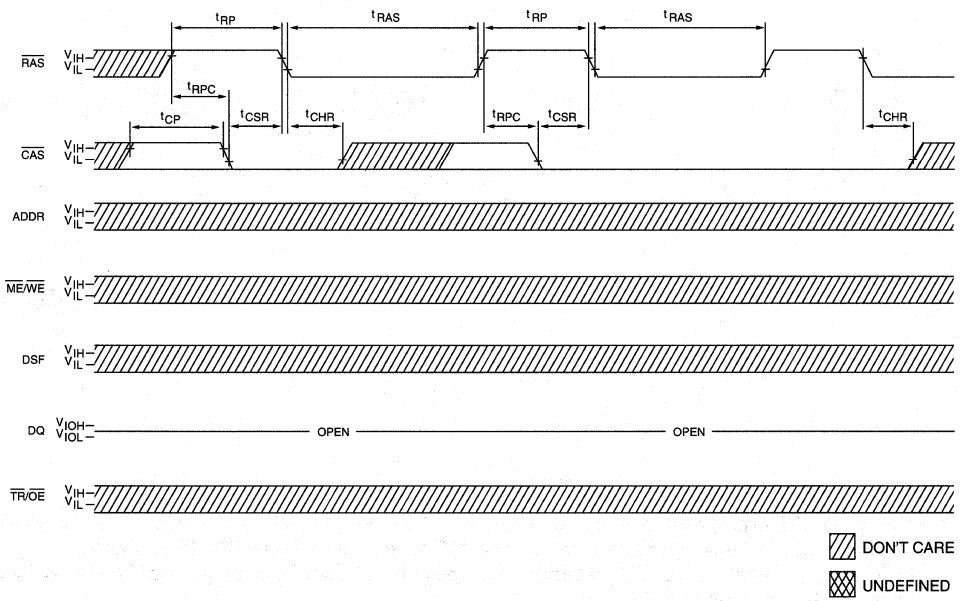


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

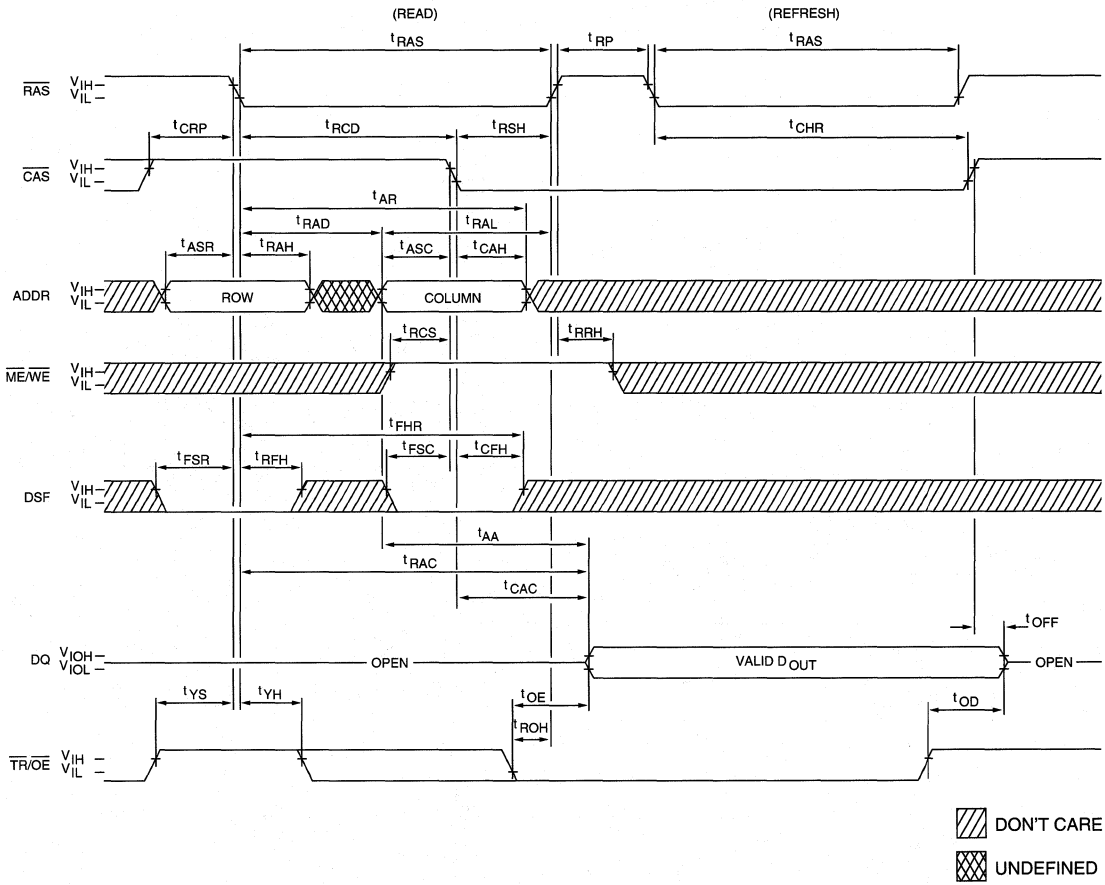
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



DRAM CBR REFRESH CYCLE

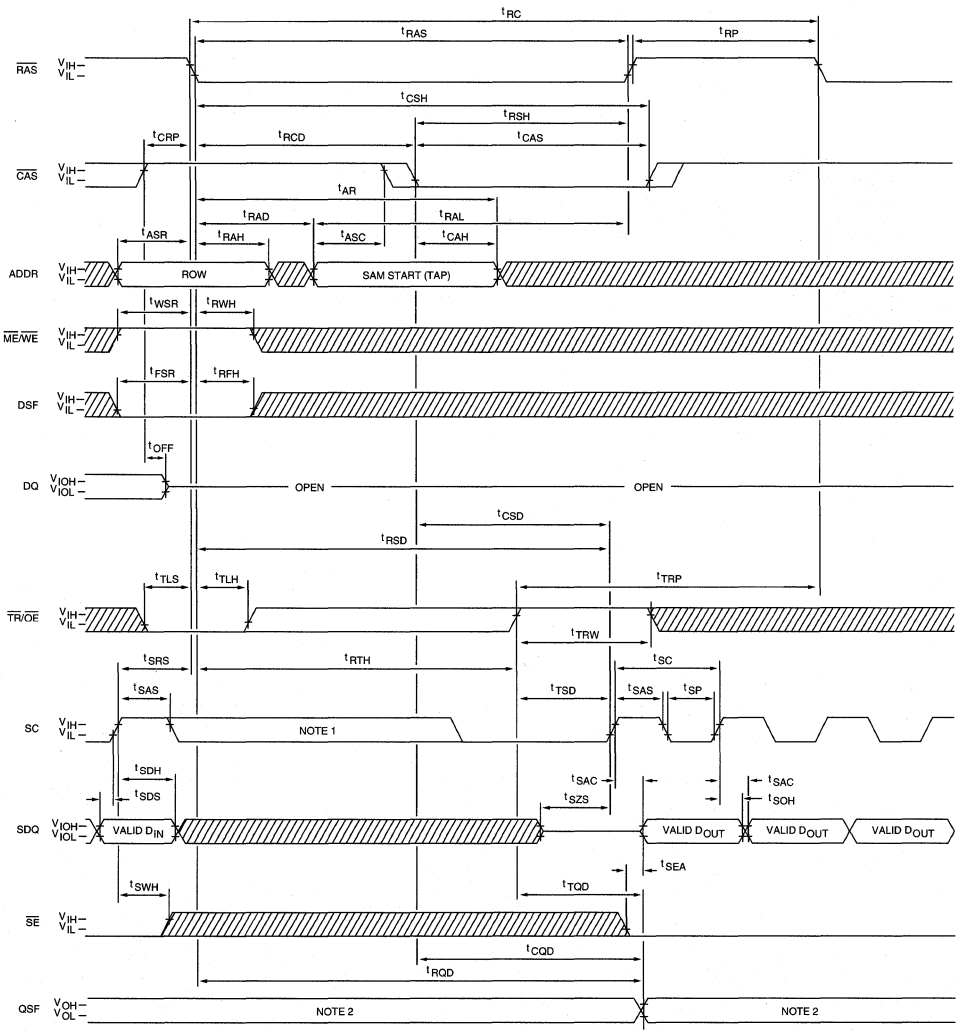


DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

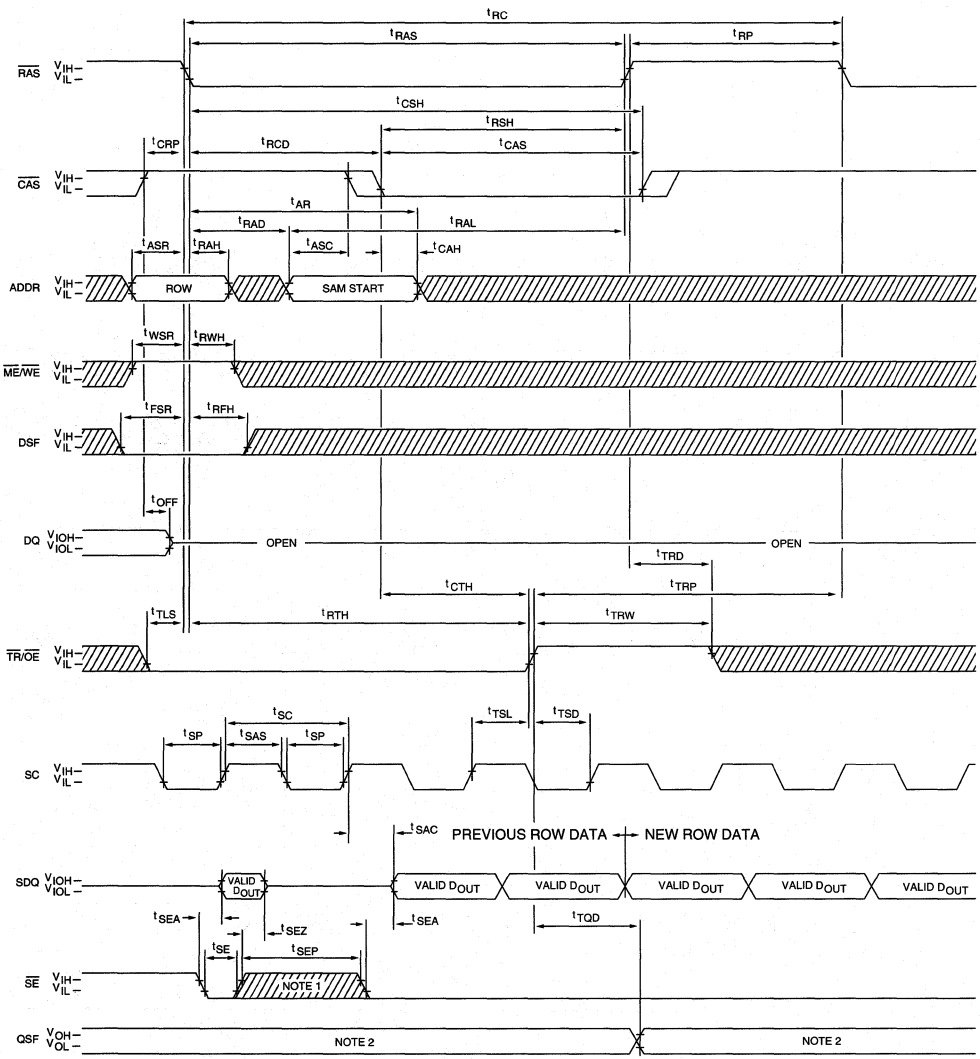
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ^{t}TSD must be met.

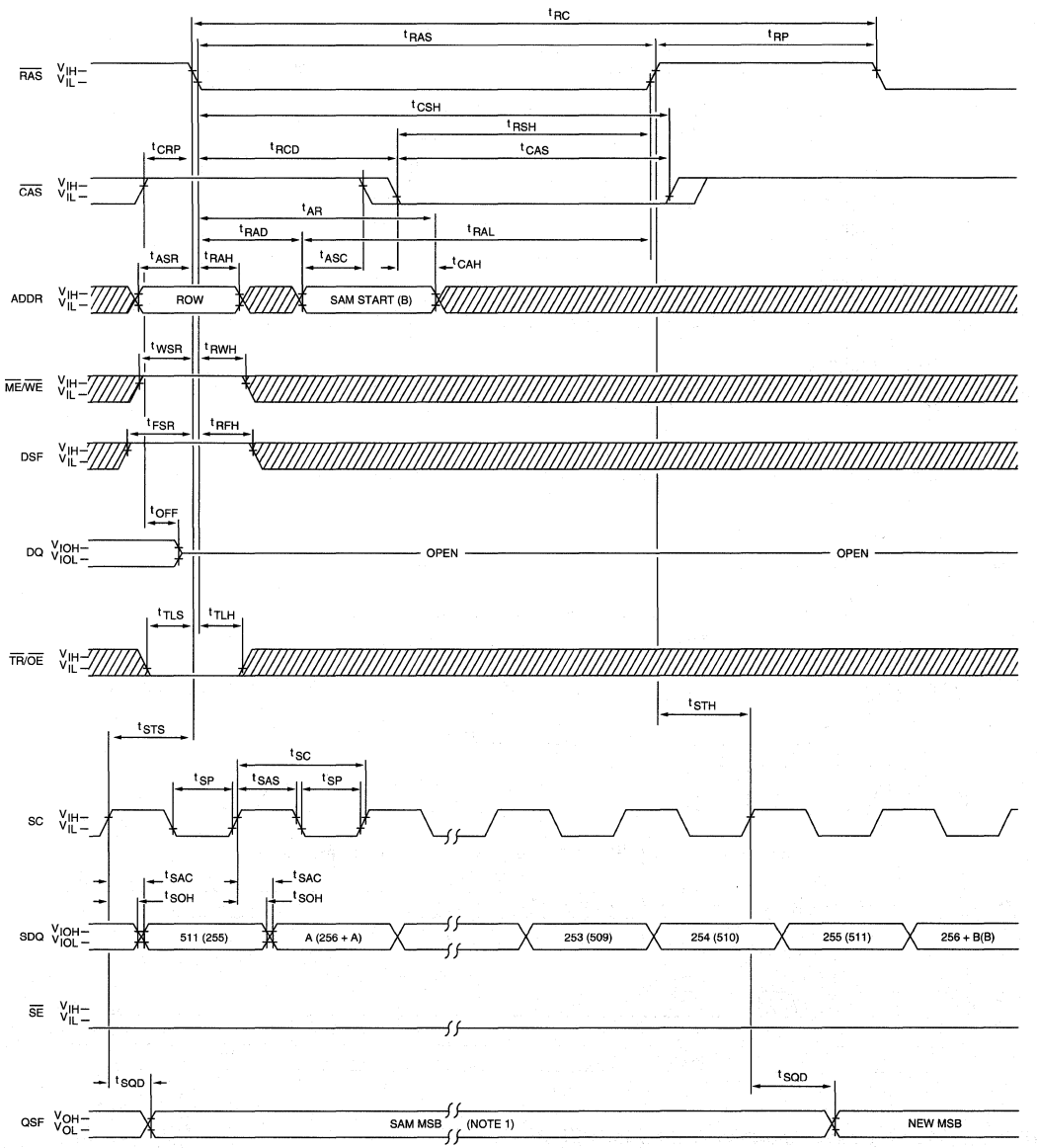
REAL-TIME READ-TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)

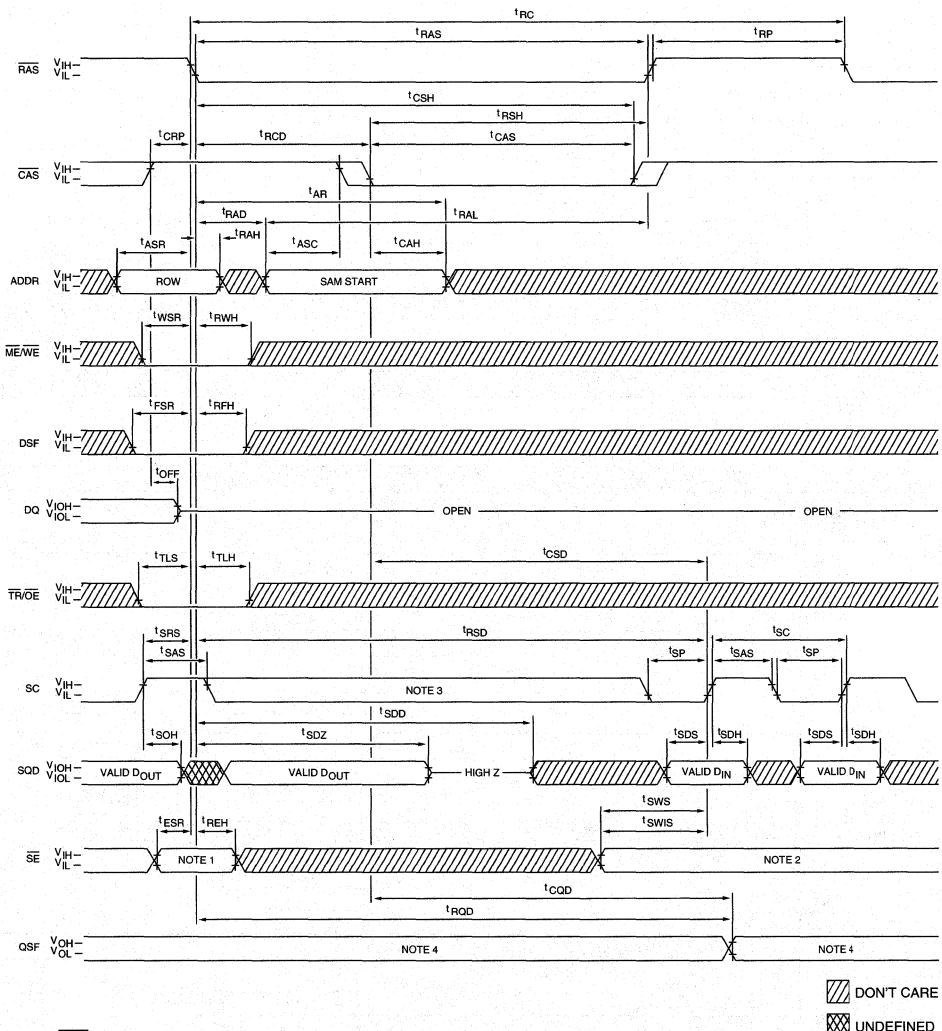


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

▨ DON'T CARE
▩ UNDEFINED

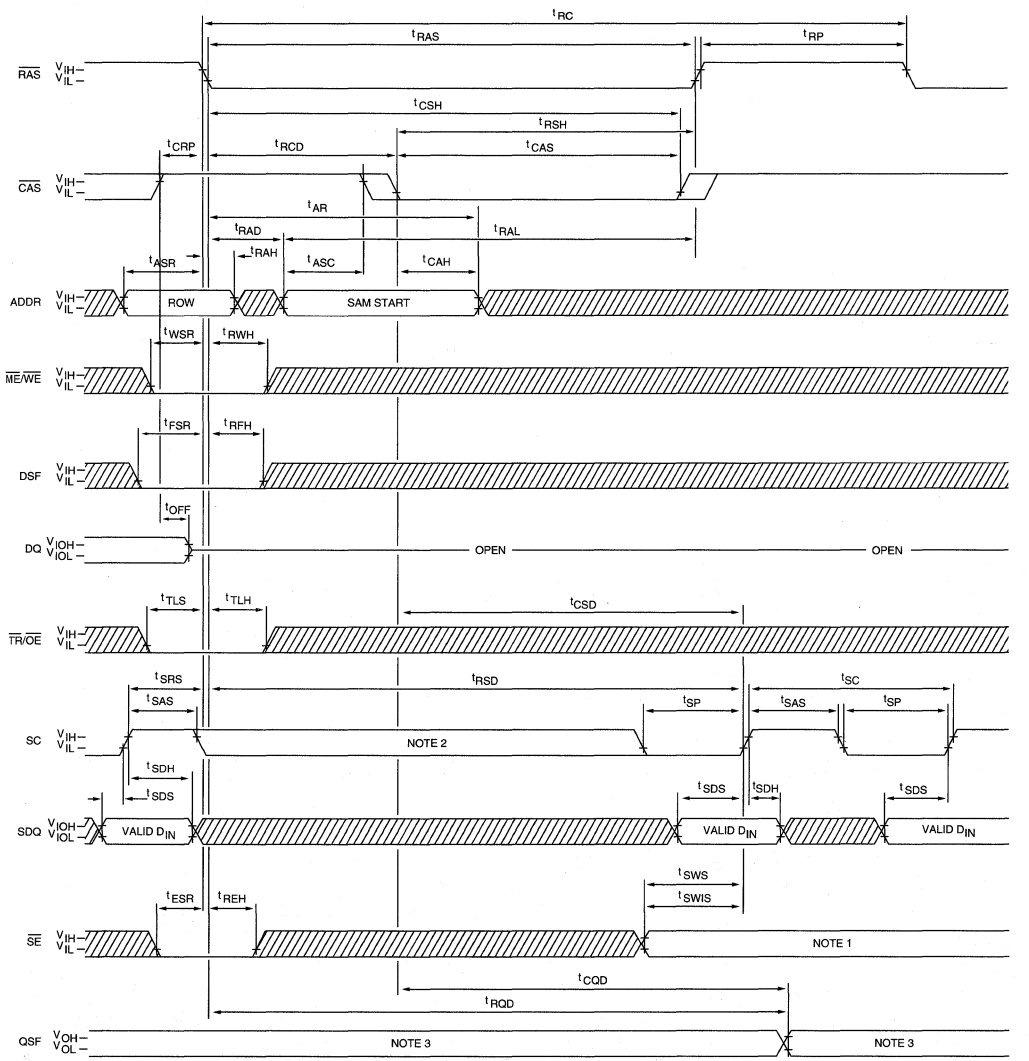
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)

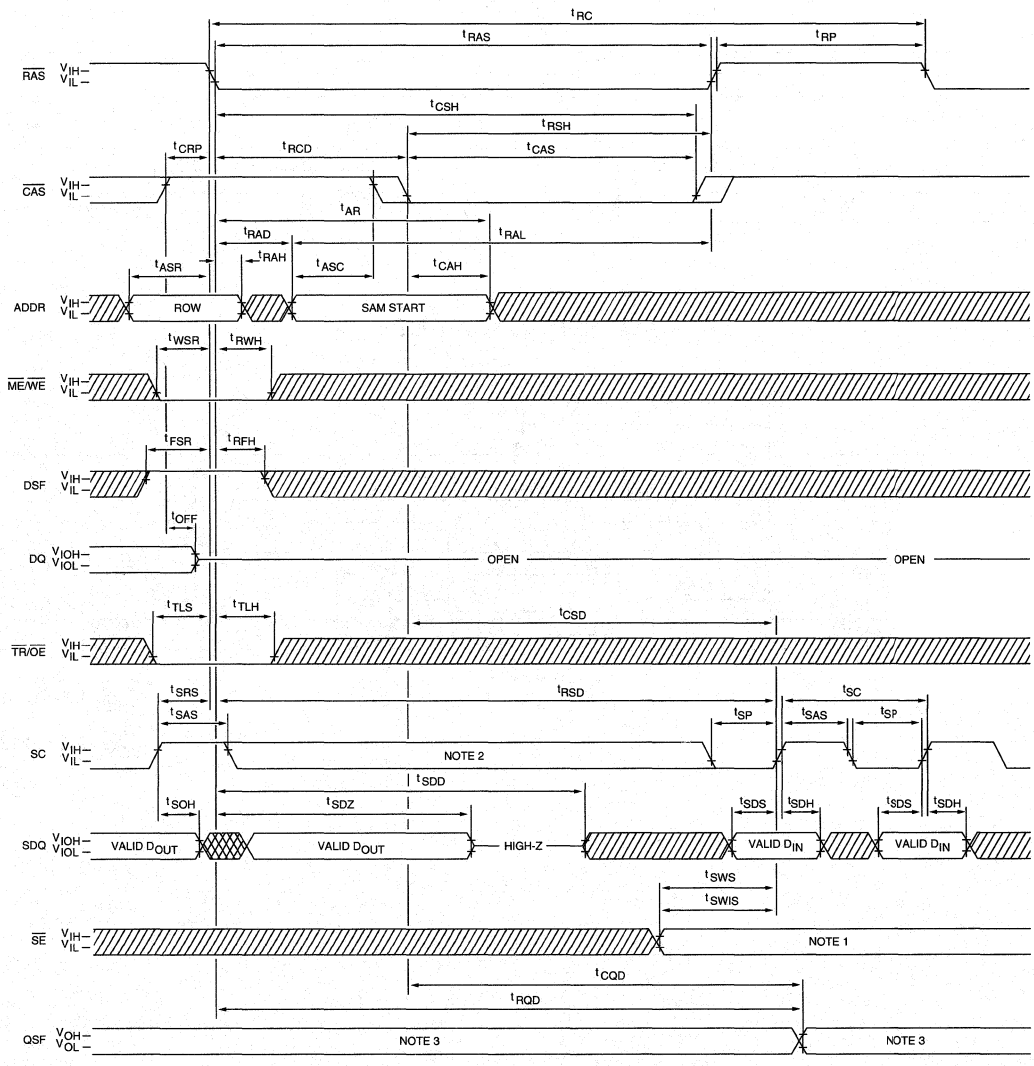


DON'T CARE

UNDEFINED

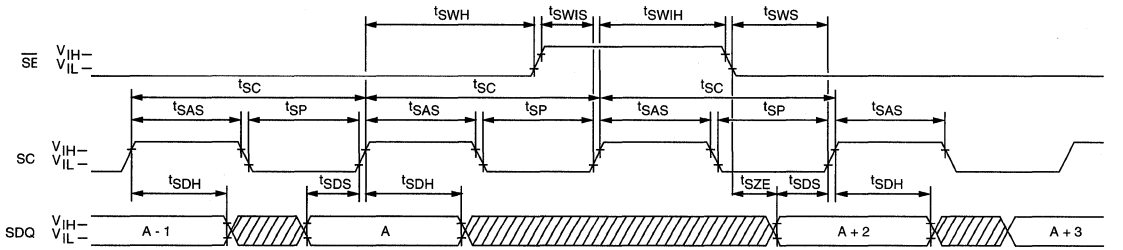
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

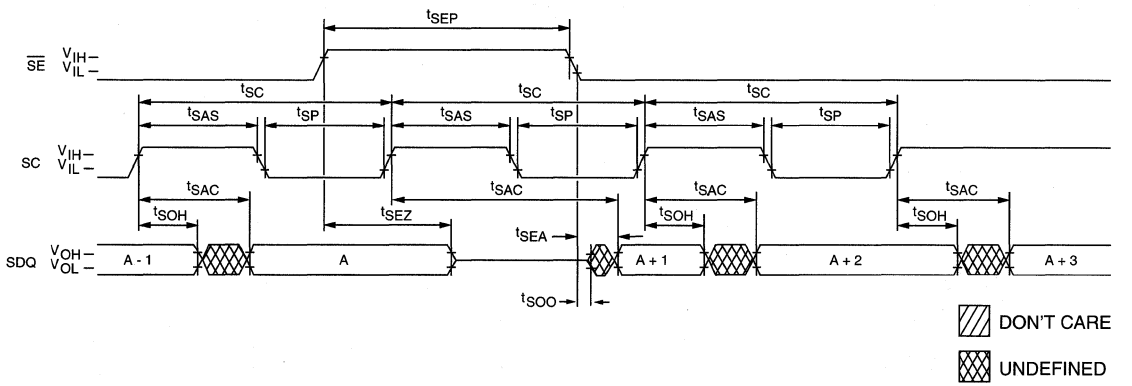


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power: 15mW standby; 275mW active, typical
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- No refresh required for serial access memory
- Optional FAST-PAGE-MODE access cycles
- Dual-port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- Fast access times: 70ns random, 22ns serial
  60ns random, 18ns serial*

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

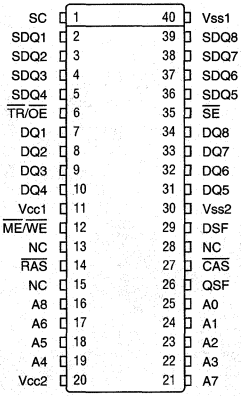
OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])
  60ns, 18ns/18ns -6*
  70ns, 22ns/22ns -7
  80ns, 25ns/25ns -8
- Packages
  Plastic SOJ (400 mil) DJ
- Part Number Example: MT42C8128DJ-7

*60ns (-6) specifications are preliminary; consult factory for availability.

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(SDB-3)



GENERAL DESCRIPTION

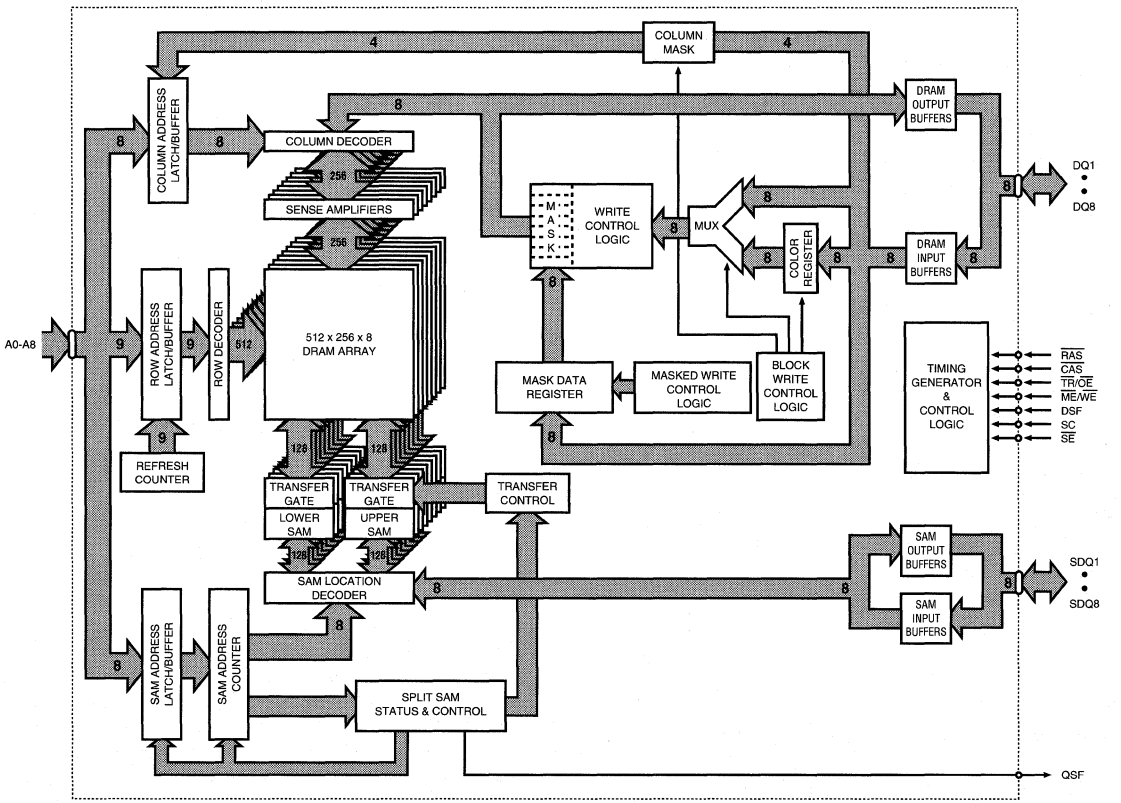
The MT42C8128 is a high-speed, dual-port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit-wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is similar to the MT4C4256 (256K x 4 DRAM). Eight 256-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256-bit-wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and requires no refresh.

The operation and control of the MT42C8128 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE, allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
12	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It acts as master chip enable, and must fall to initiate any DRAM or TRANSFER cycle.
27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe the DSF input.
25, 24, 23, 22, 19, 18, 17, 21, 16	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when during SPLIT TRANSFER.

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7, 8, 9, 10, 31, 32, 33, 34	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 4, 5, 36, 37, 38, 39	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-127, HIGH if address is 128-255.
15, 28	NC	–	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	Vcc	Supply	Power Supply: +5V ±10%
30, 40	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 may be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8128 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C8128 supports CBR, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 8 column address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH; all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFERcycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. To enable the DRAM output port, the $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within an 8-bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$ and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

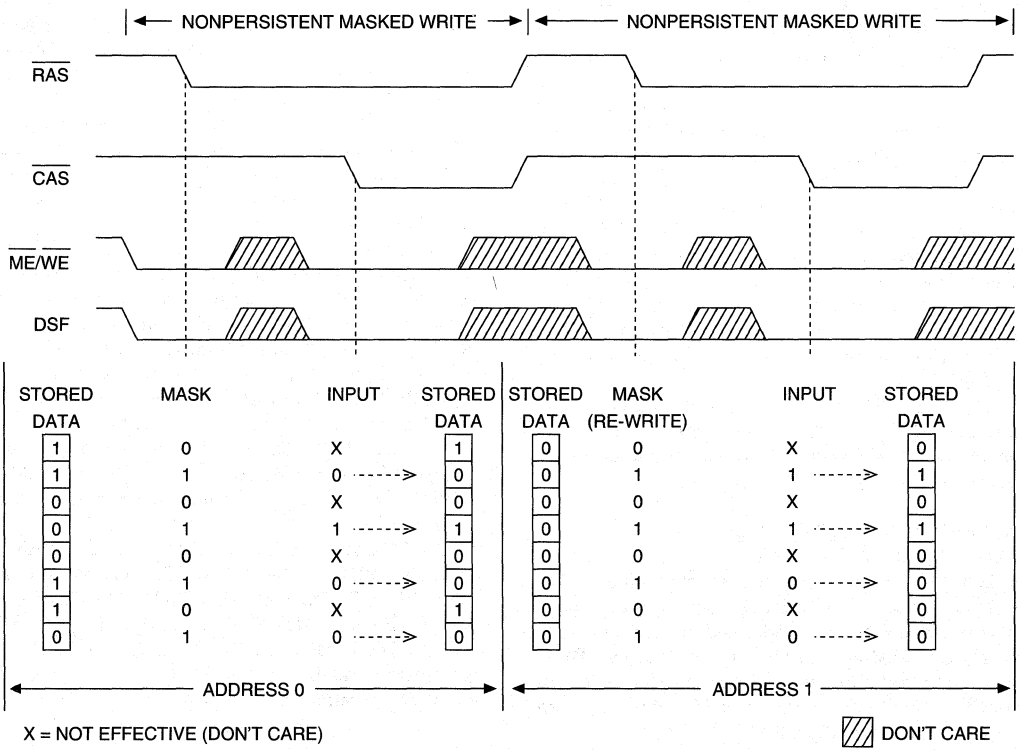


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

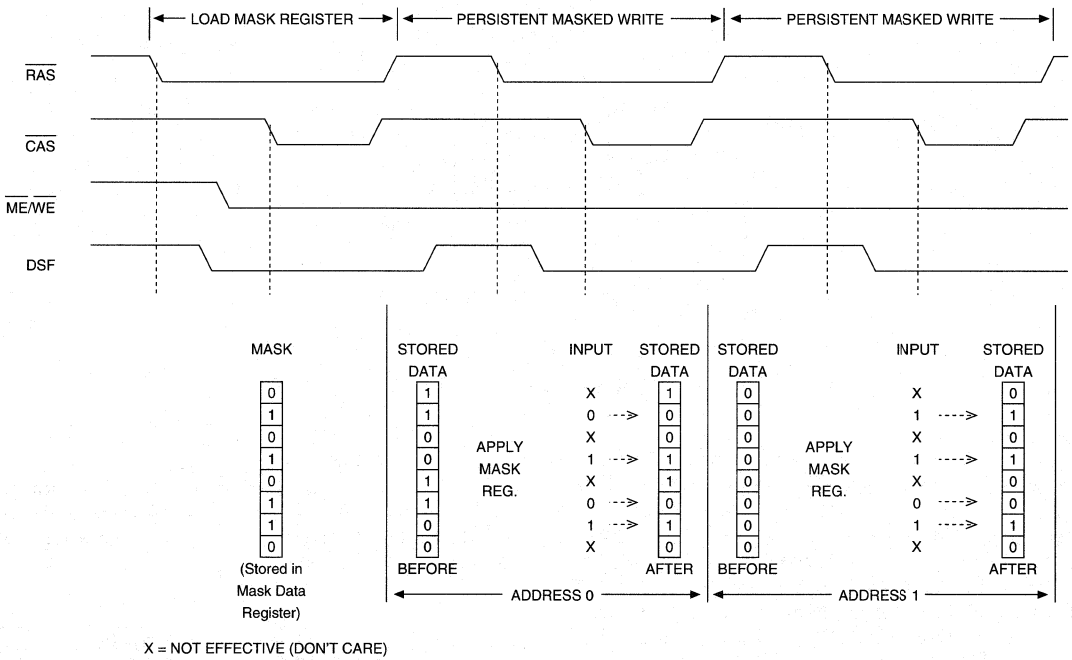


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

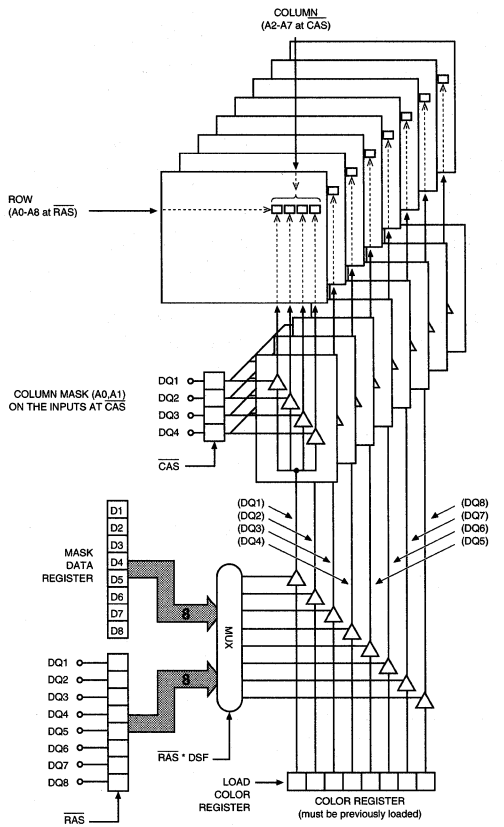


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. Using the column mask input and MASKED WRITE function allows any combination of the eight bit planes or four column locations to be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The mask data register contents will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

The LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

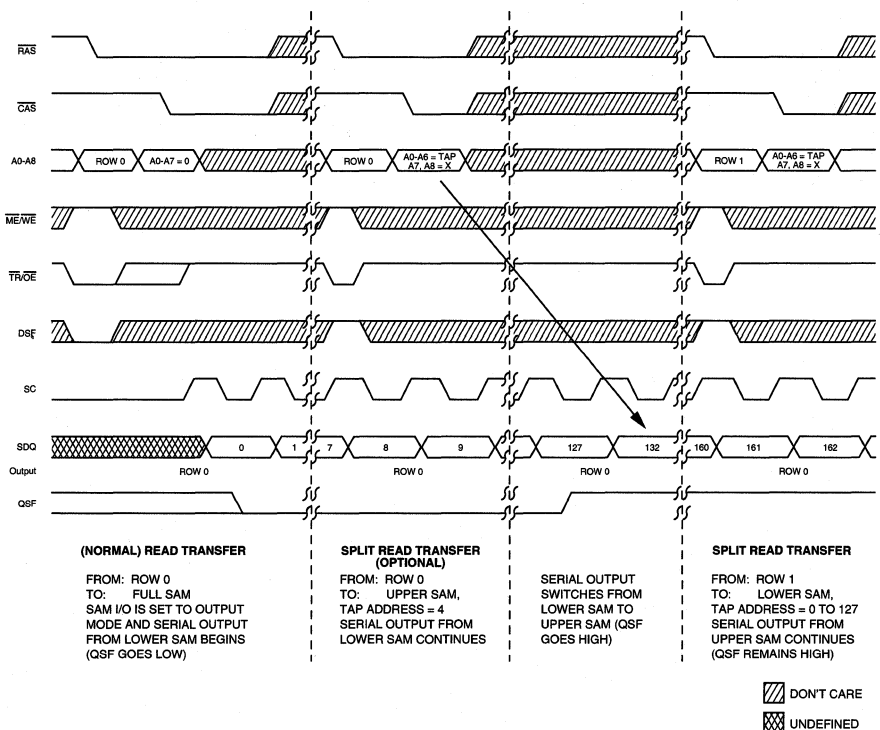


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin, and to set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pin A7 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, it is only needed if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 127 ("A7" = 0, A0-A6 = 1) the new Tap address is loaded for the next half ("A7" = 1, A0-A6 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached, before an SRT is done for the half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, and 128 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to that of the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QSF is LOW if access is to the lower half of the SAM, and HIGH if to access the upper half.

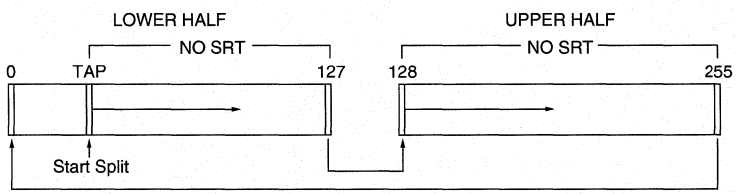


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and ($\overline{ME}$)/$\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SRT cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = ($\overline{TR}$)/$\overline{OE}$ ≥ V_{IH} during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8128 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS, A8=X	RAS	CAS, WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CBR REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE and LOAD COLOR REGISTER), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for the lower half, 255 for the upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	
OUTPUT LEVELS	VOH	2.4		V	1
Output High Voltage (IOUT = -2.5mA) Output Low Voltage (IOUT = 2.5mA)	VOL		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	CI2		7	pF	2
Input/Output Capacitance: DQ, SDQ	CI/O		9	pF	2
Output Capacitance: QSF	CO		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ [MIN])	I_{CC1}	105	95	85	mA	3, 4 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ [MIN])	I_{CC2}	95	85	75	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC5}	105	95	85	mA	3, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	105	95	85	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	115	105	95	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ [MIN])	I_{CC9}	170	150	130	mA	3, 4, 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ [MIN])	I_{CC10}	160	140	120	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	65	55	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC12}	170	150	130	mA	3, 4, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	170	150	130	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	190	160	130	mA	3, 4

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	148		170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	83		90		95		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	18	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	42	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	12		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	40		45		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer turn-off delay	tOFF	3	12	3	12	3	15	ns	20, 23
Output disable	tOD	3	10	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		10		10		ns	25
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	tROH	0		0		0		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		45		55		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	18		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	18		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	12		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	50		55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	38		40		45		ns	21
Transition time (rise or fall)	^tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	tRTH	65	10,000	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	tCTH	25		25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	tTSL	5		5		5		ns	
$\overline{TR}/(\overline{OE})$ to $\overline{RAS}$ HIGH hold time	tTRD	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	tTRW	15		20		20		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	tTSD	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	tREH	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	12		15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	12		15		15		ns	
SC to QSF delay time	tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	tRQD		70		75		75	ns	
DSF to $\overline{RAS}$ hold time	tFHR	40		45		55		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	12		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		25		25		25	ns	
$\overline{CAS}$ to QSF delay time	tCQD		30		35		35	ns	
$\overline{RAS}$ to first SC delay	tRSD	70		80		80		ns	
$\overline{CAS}$ to first SC delay	tCSD	25		30		30		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

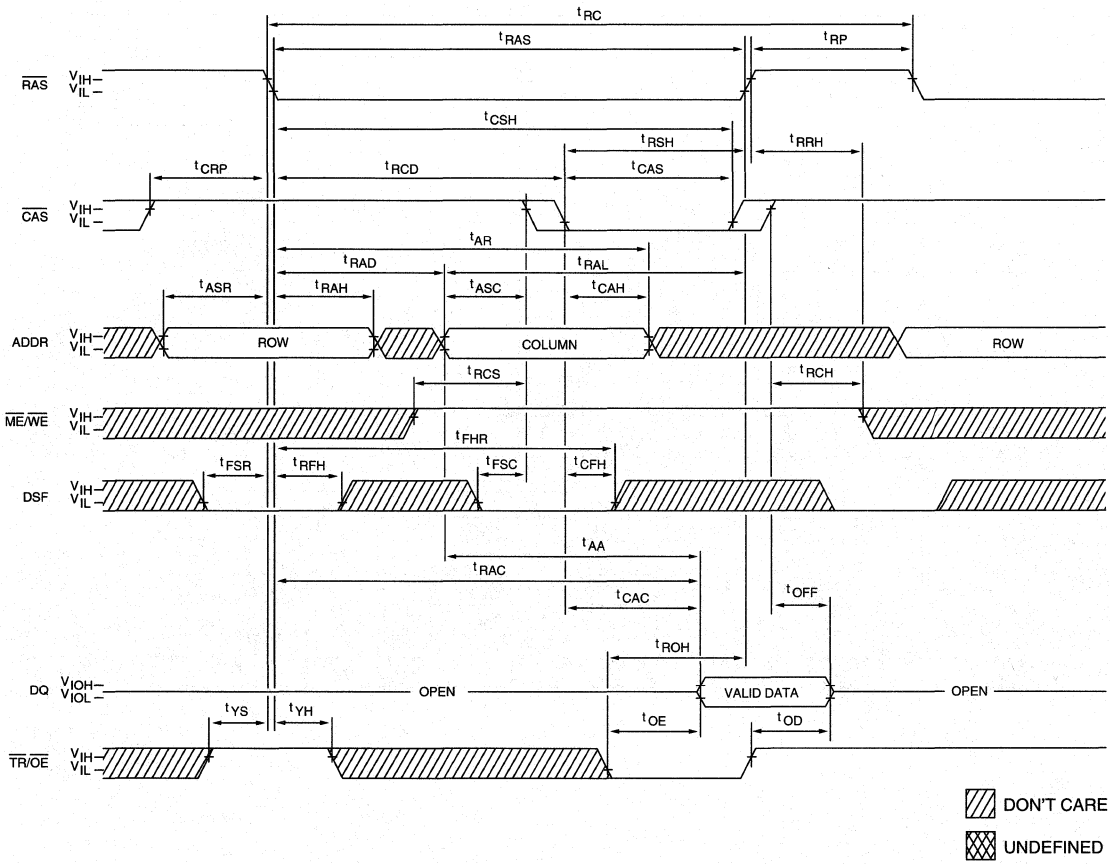
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	18		22		25		ns	
Access time from SC	^tSAC		18		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	7		8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		10		ns	
Access time from $\overline{SE}$	^tSEA		12		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		10		ns	
$\overline{SE}$ pulse width	^tSE	7		8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	10	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	9		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

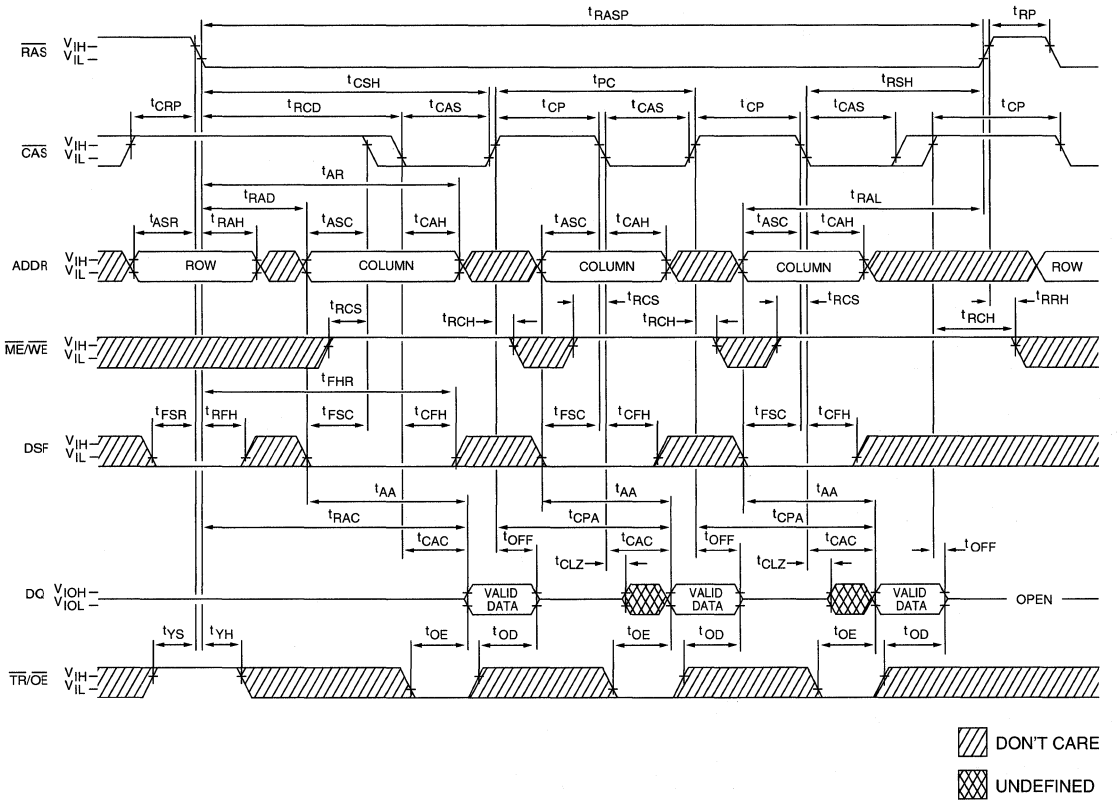
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16.7ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature $^tSOH = ^tSAC$ - output transition time, this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



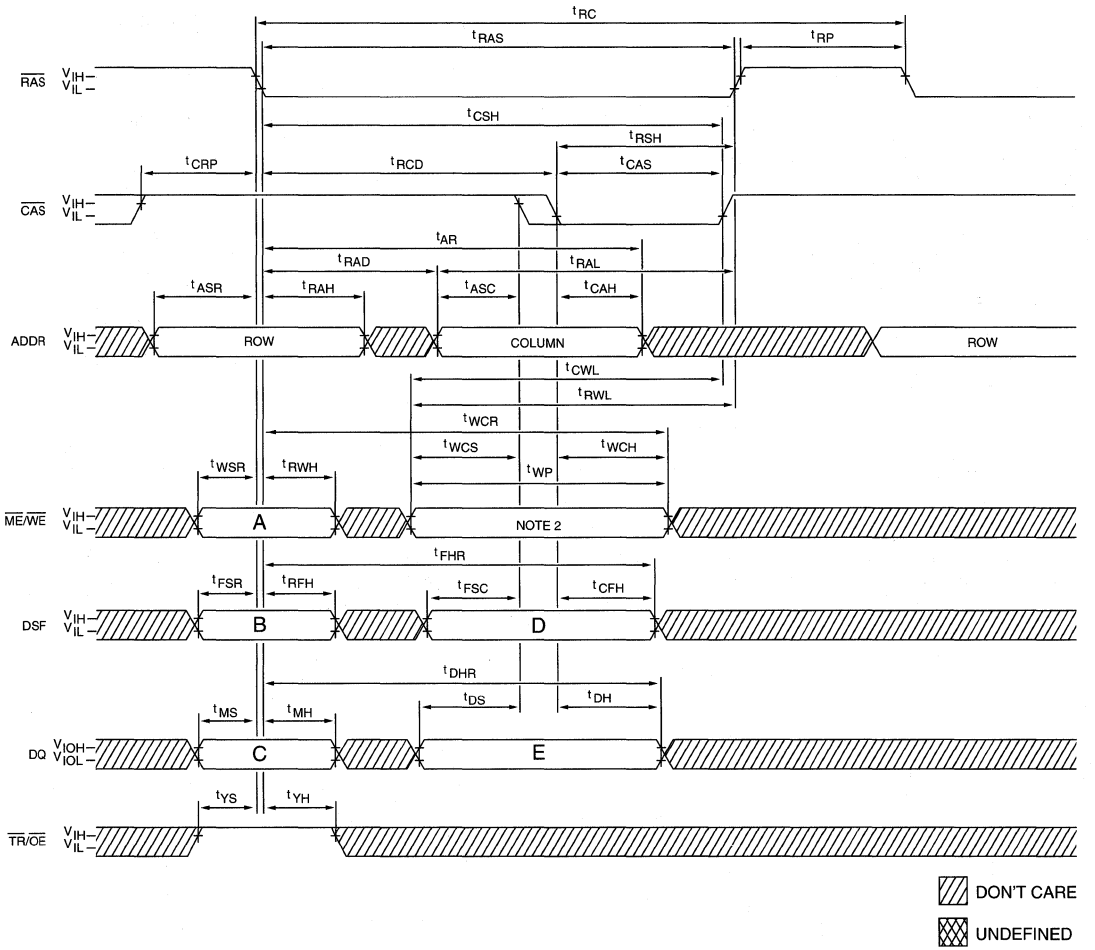
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE (or READ)	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

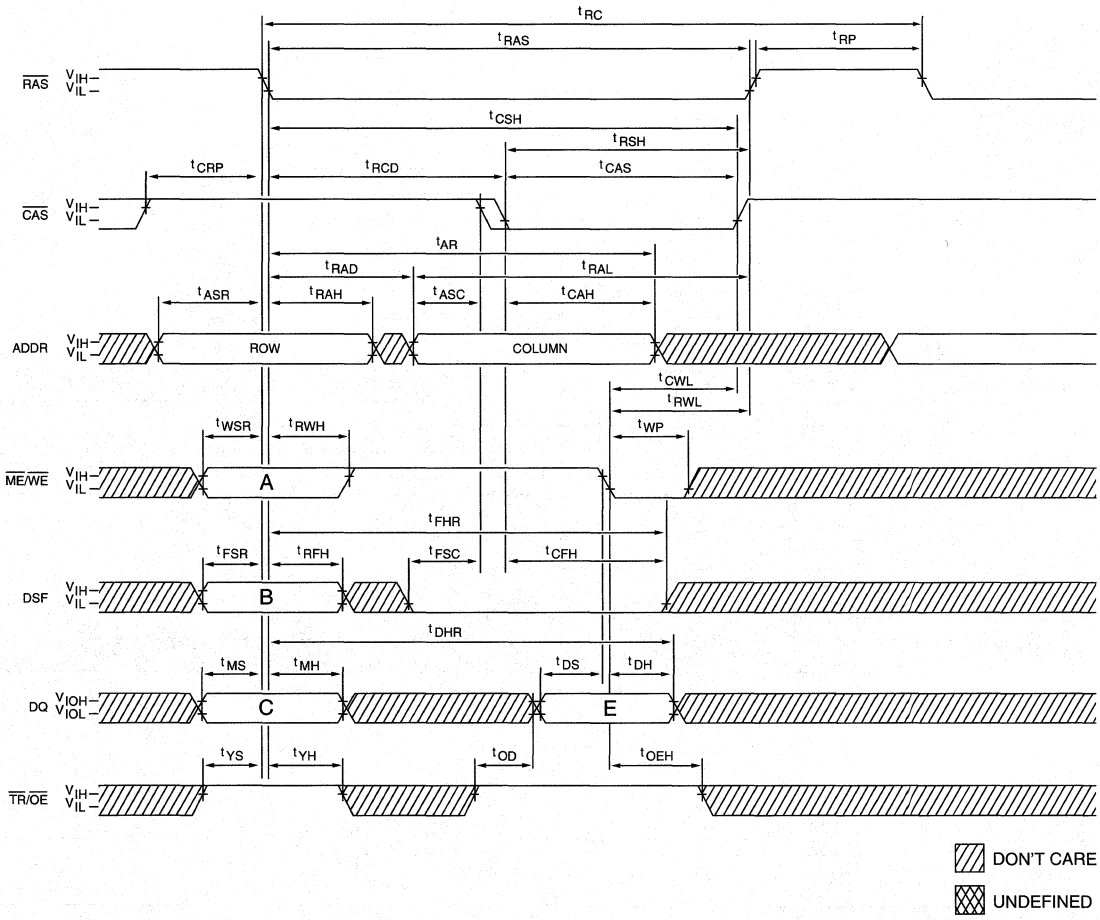
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later (except for BLOCK WRITE and LOAD COLOR REGISTER).
3. $\overline{WE}$ = "don't care" for BLOCK WRITE and LOAD COLOR REGISTER. The DQ column-mask data or color data will be latched at the falling edge of $\overline{CAS}$, regardless of the state of $\overline{ME}/\overline{WE}$.

DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For BLOCK WRITE, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

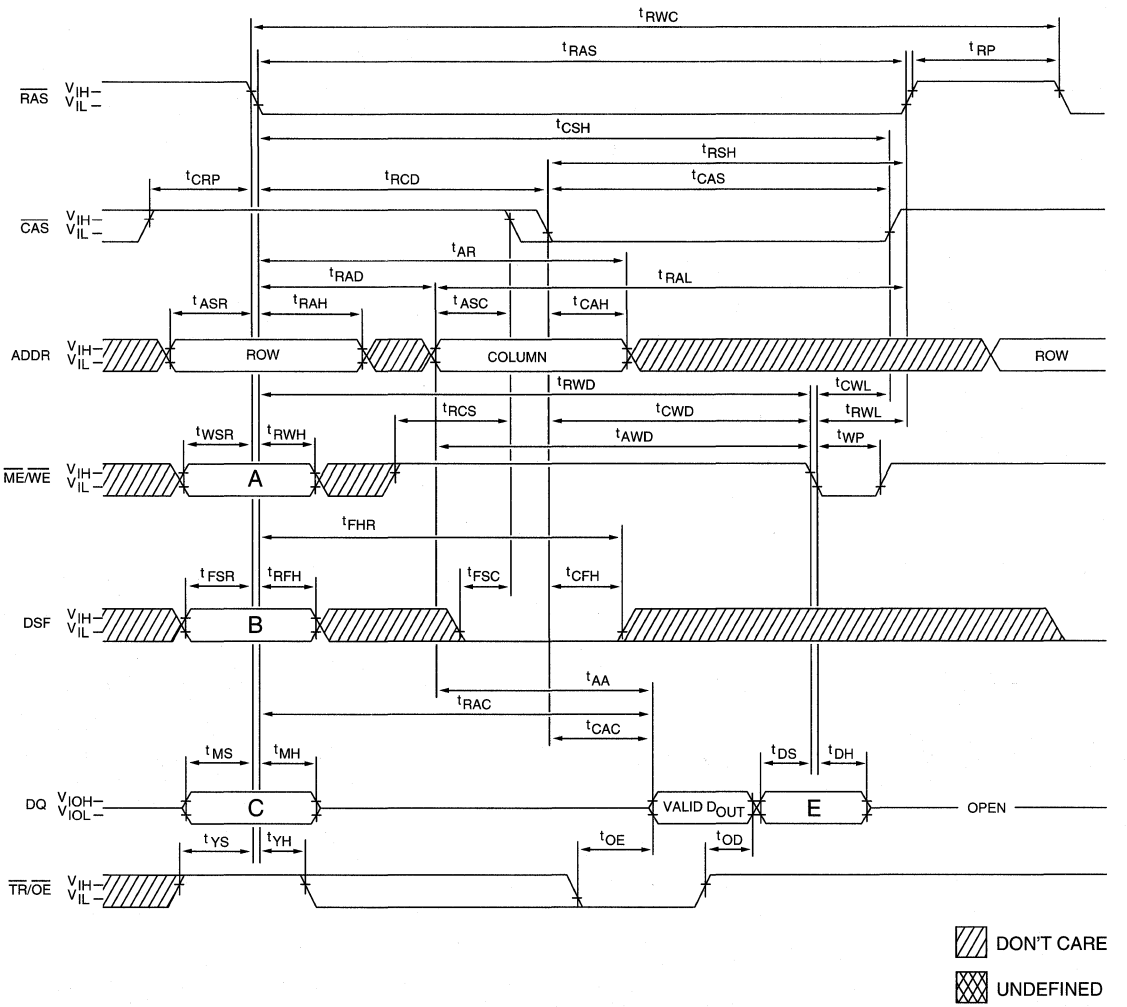
DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

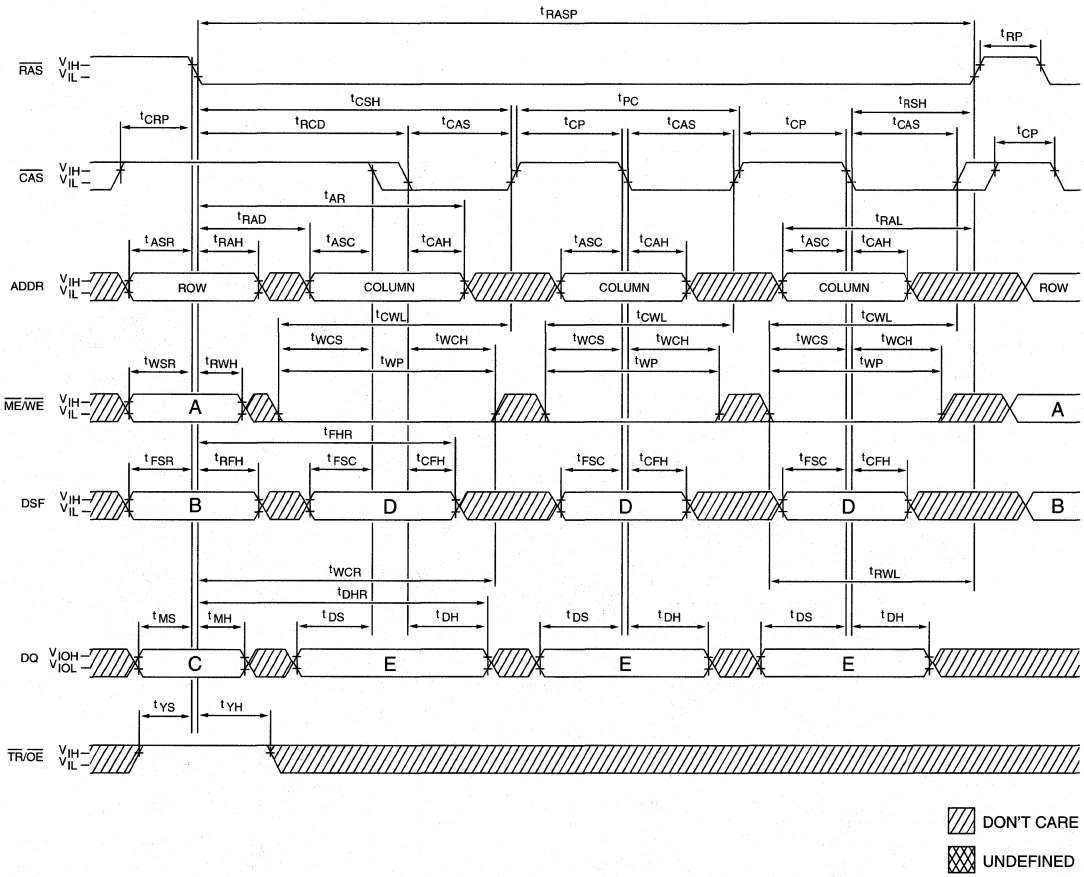
VRAM

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



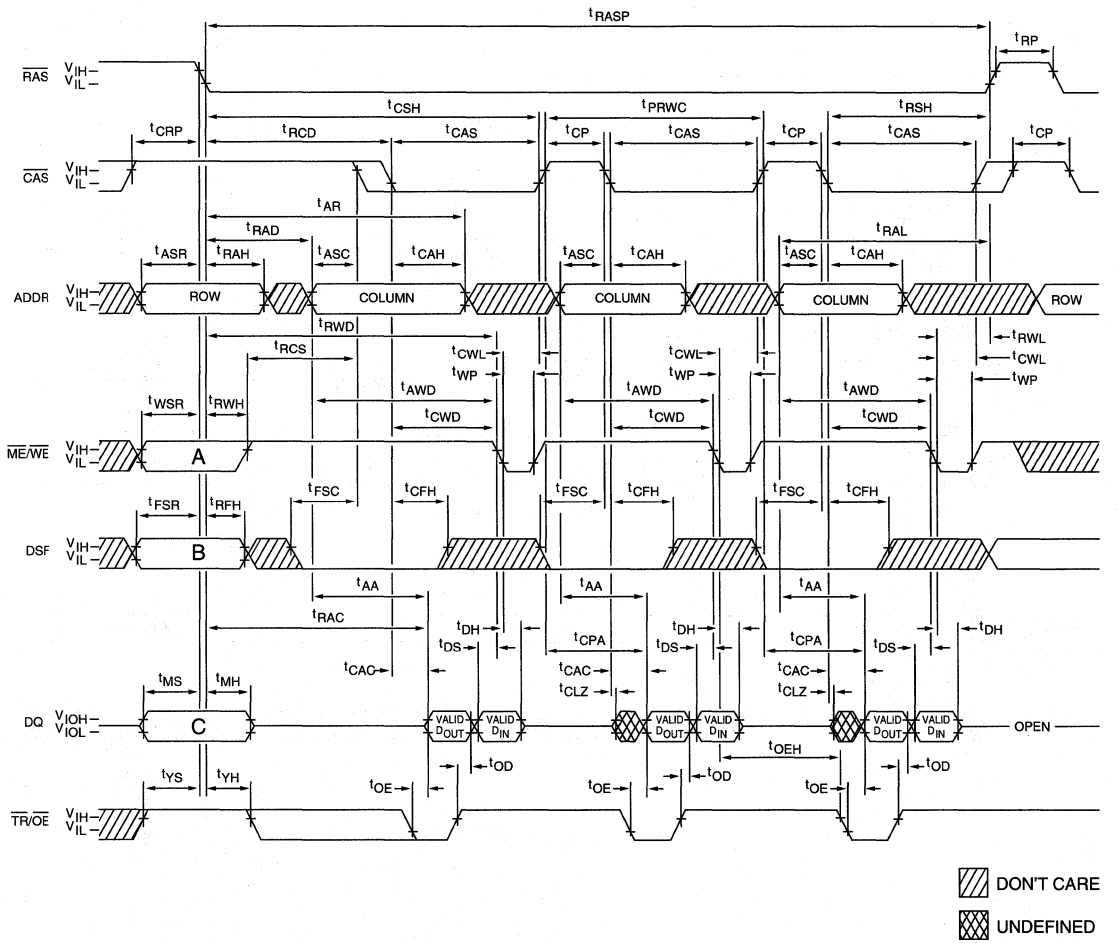
NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



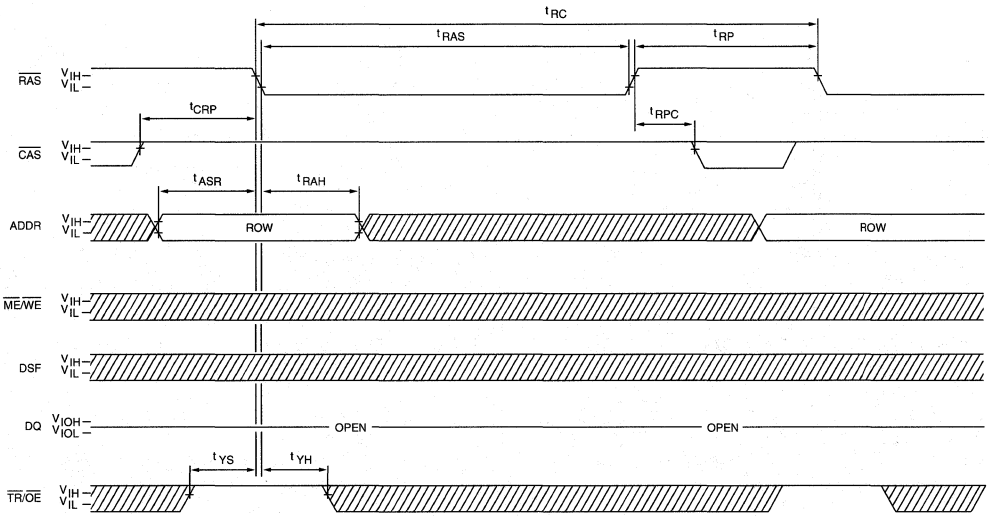
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

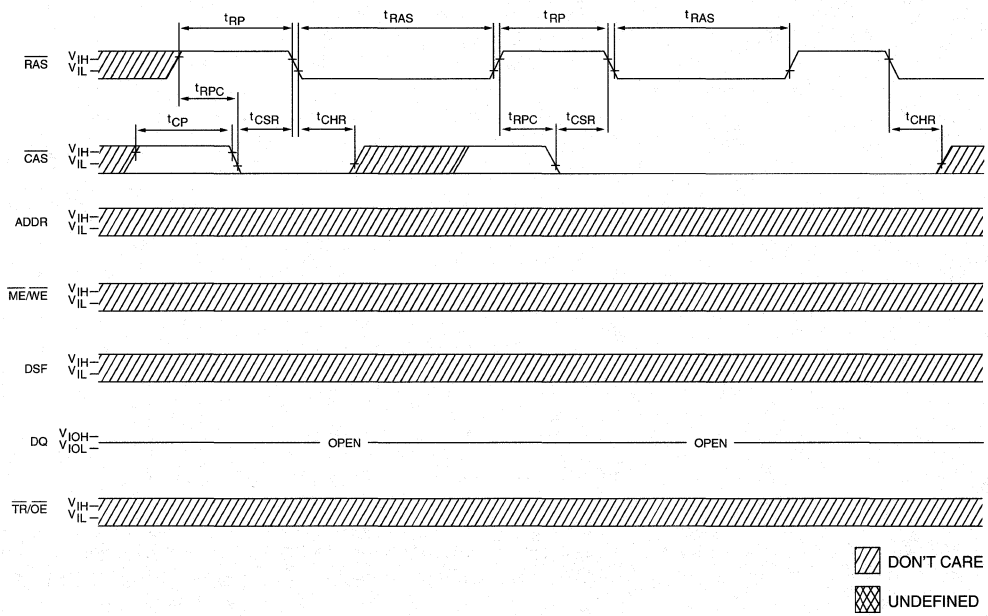


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

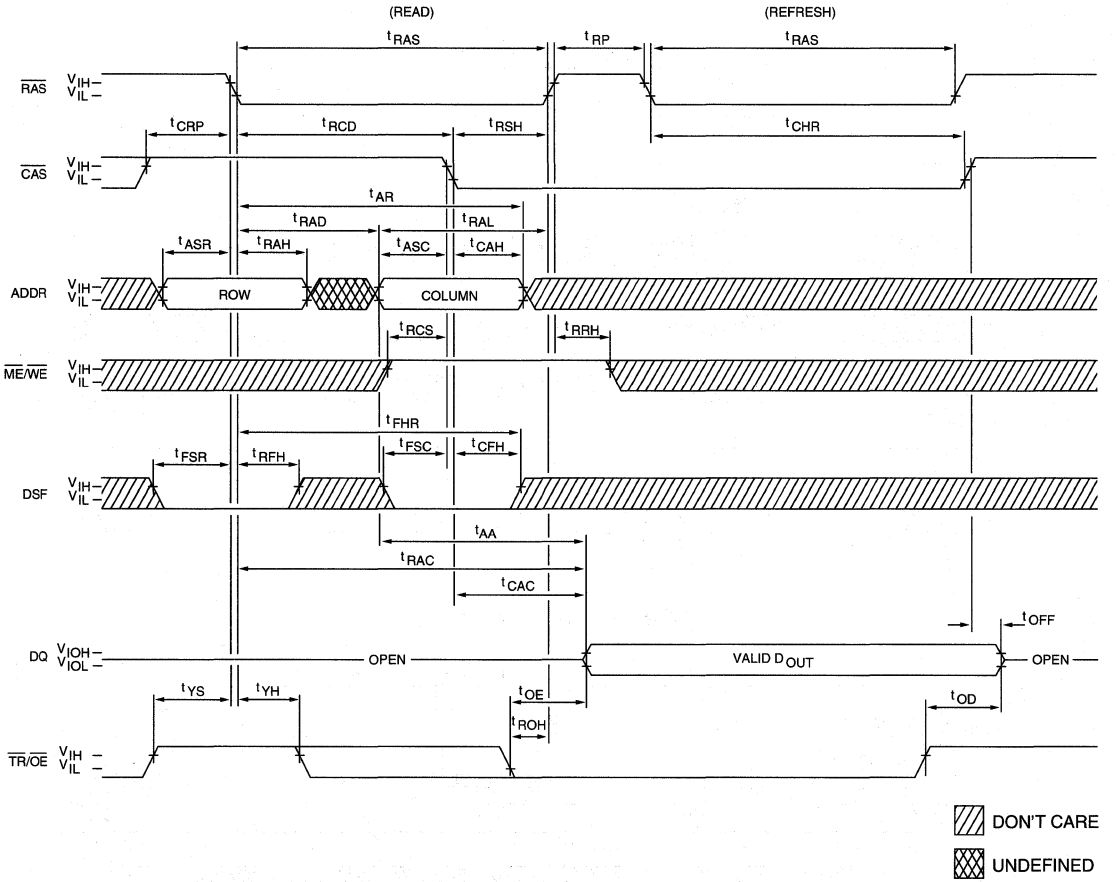
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CBR REFRESH CYCLE

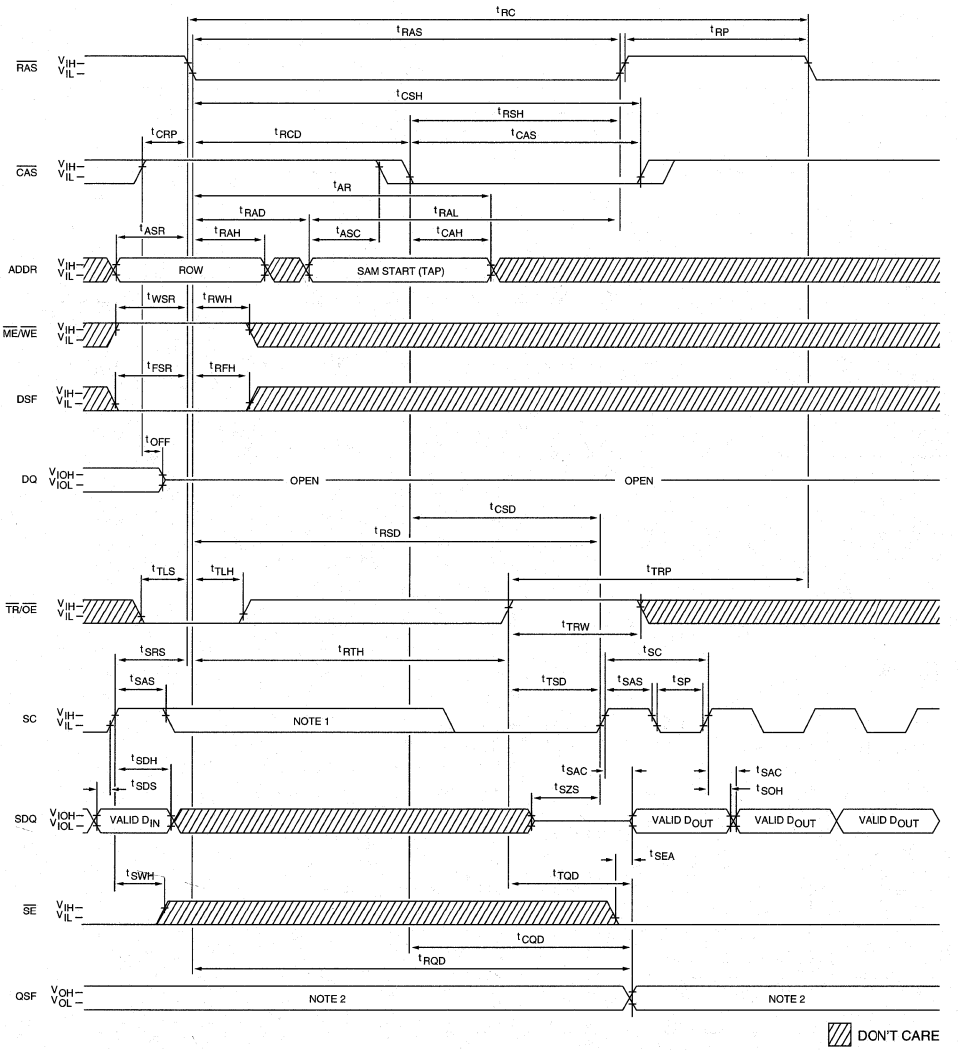


DRAM HIDDEN-REFRESH CYCLE



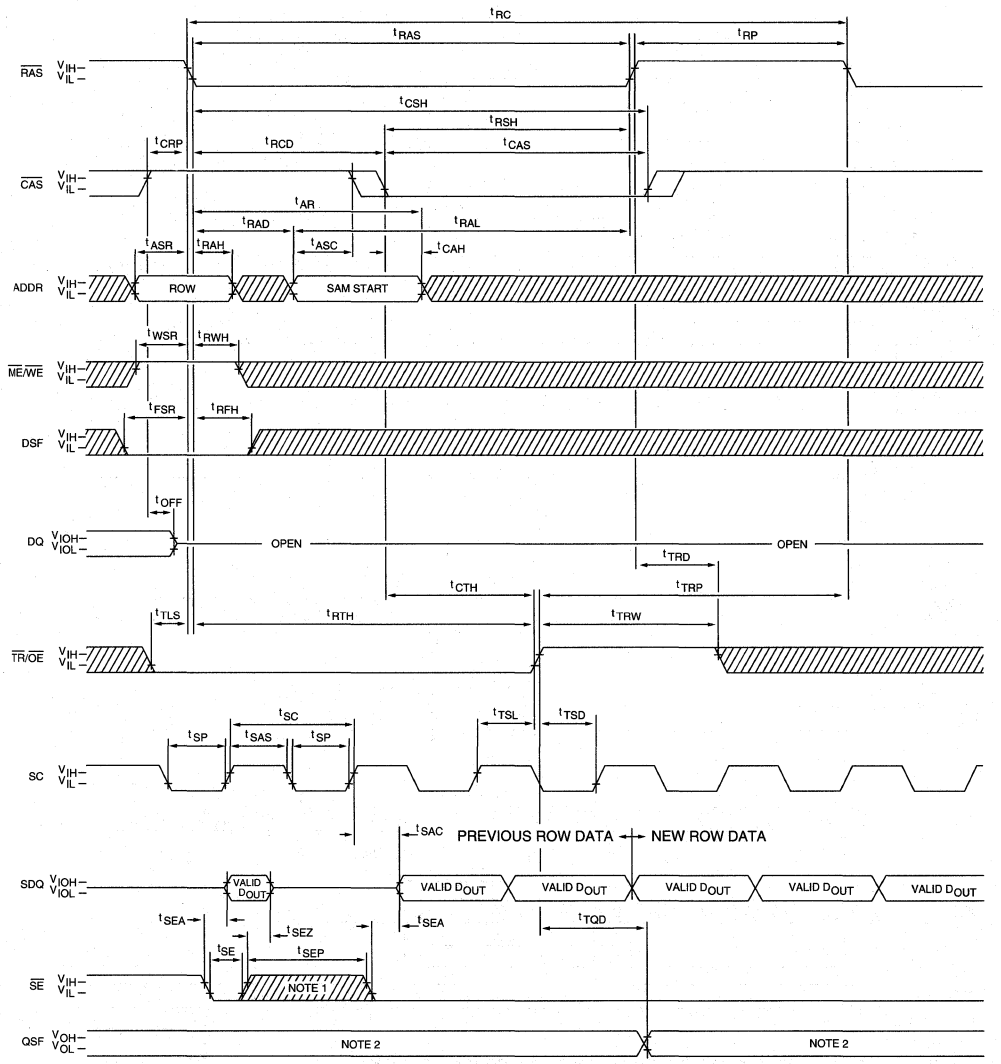
NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)



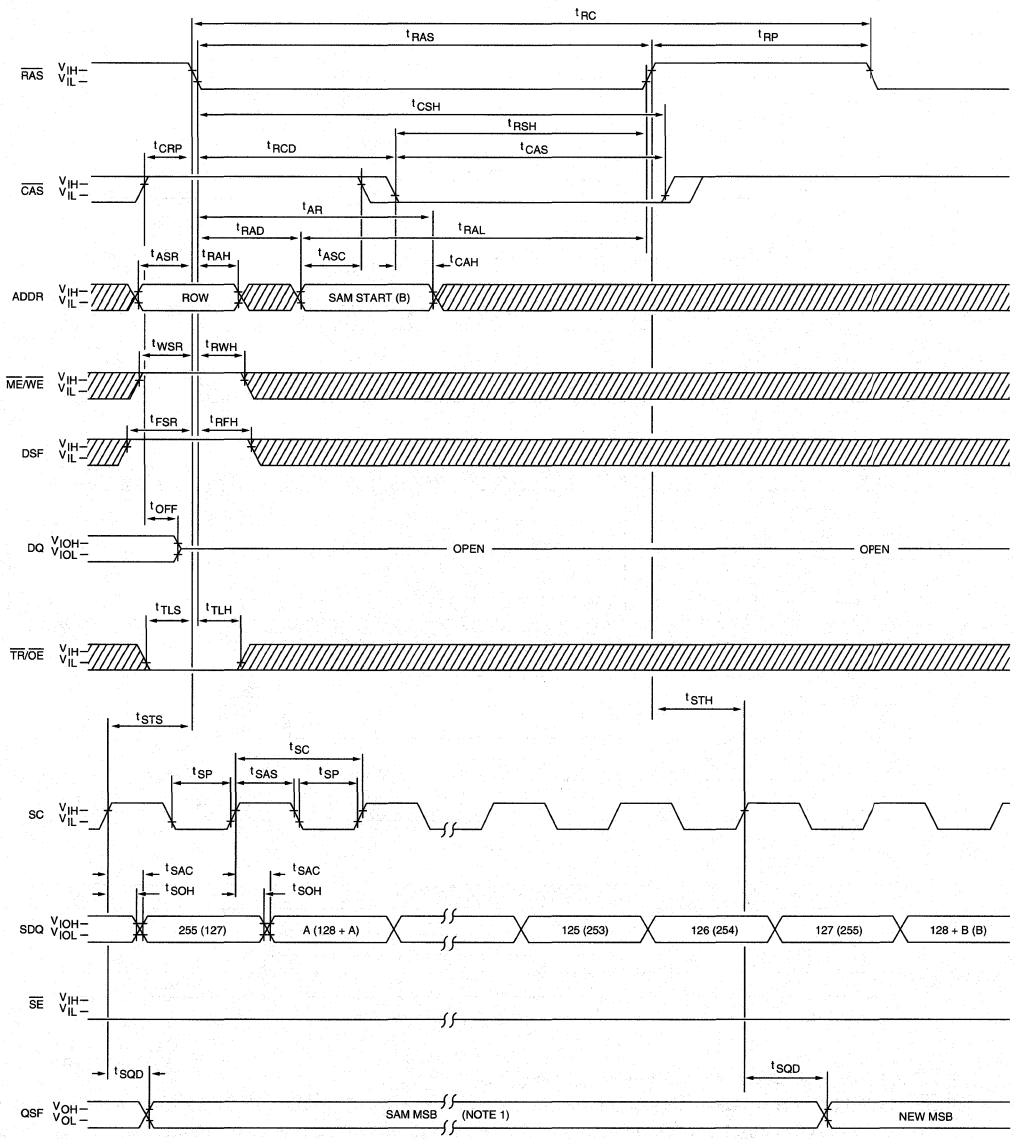
NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ^{t}TSD must be met.

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

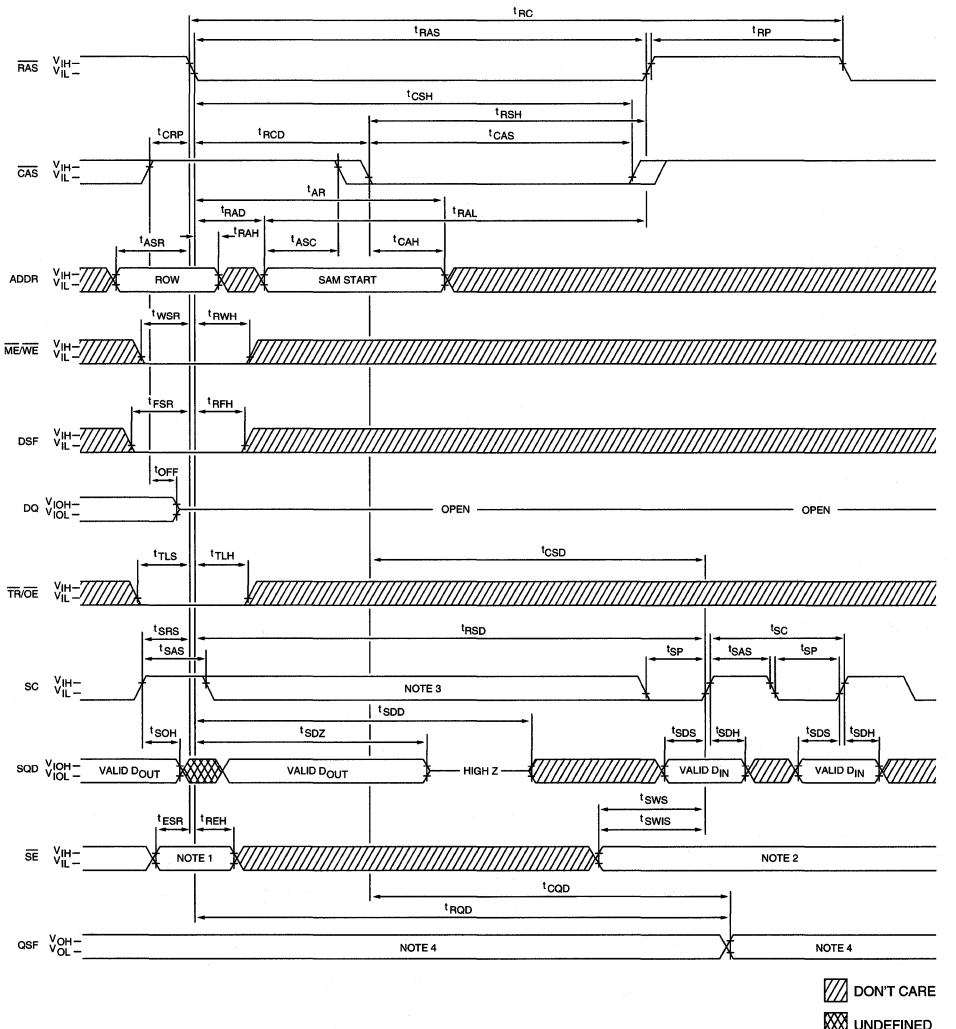
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

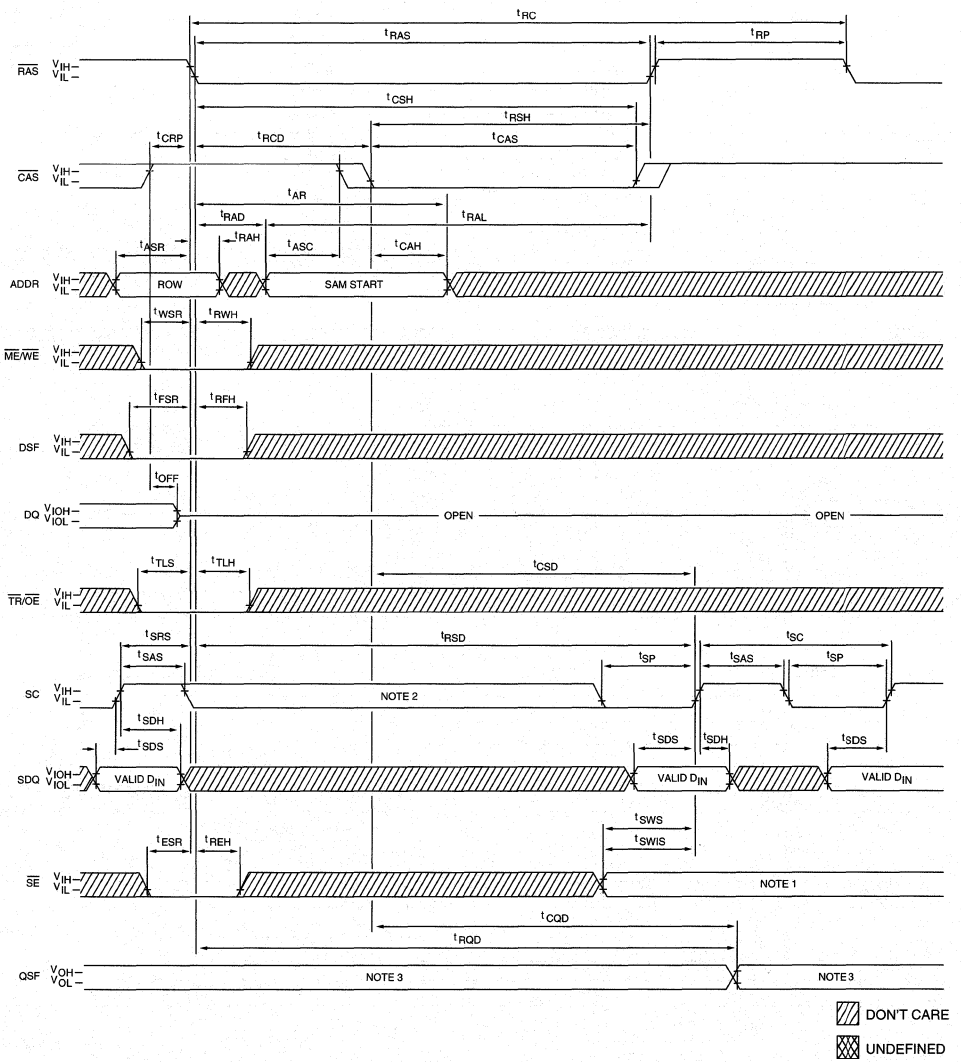
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



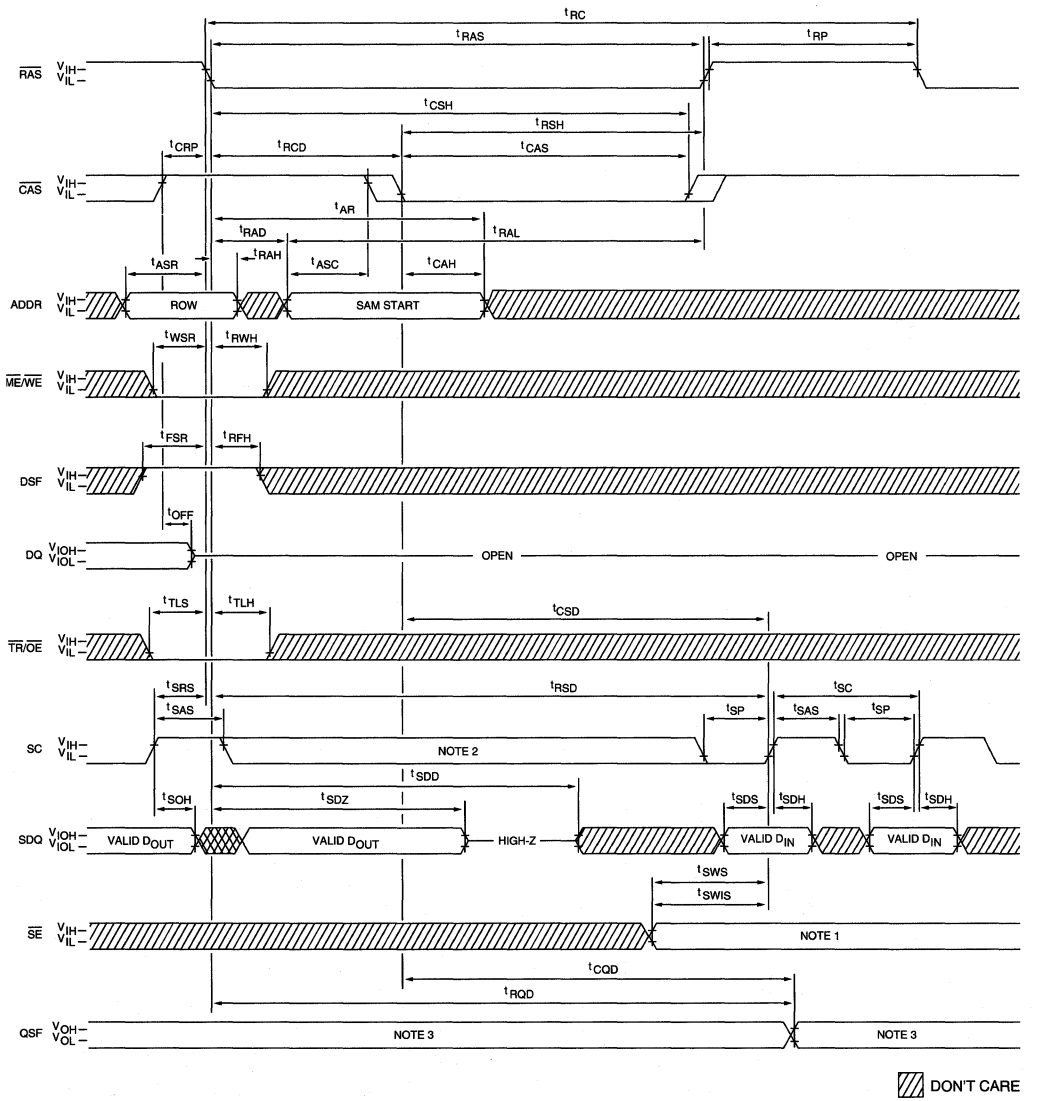
NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



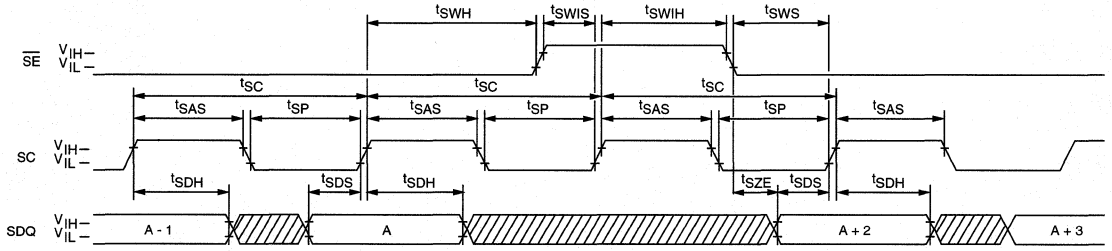
NOTE: 1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

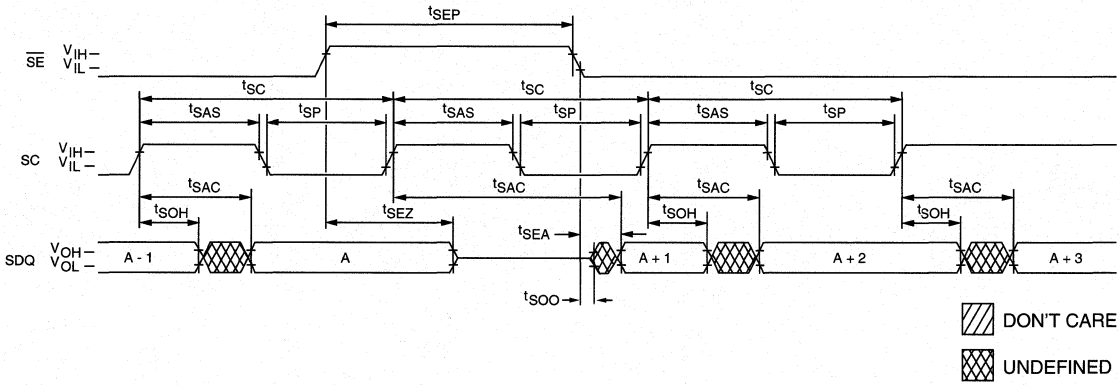


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



NEW VRAM

VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry-standard pinout, timing and functions
- NIBBLE (4-bit) WRITE and MASKED WRITE access cycles
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE
- Dual-port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times: 70ns random, 22ns serial

SPECIAL FUNCTIONS

- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS — MARKING

- Timing (DRAM, SAM [cycle/access])
  70ns, 22/22ns — -7
  80ns, 25/25ns — -8
- Packages
  Plastic SOJ (400 mil) — DJ
  Plastic TSOP (400 mil) — TG*
  Plastic TSOP (400 mil) reverse pinout — RG*
- Part Number Example: MT42C8254-7DJ

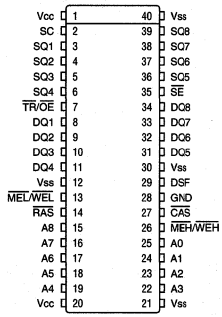
GENERAL DESCRIPTION

The MT42C8254 is a dual $\overline{ME}/\overline{WE}$ version of the MT42C8255, high-speed, dual-port CMOS dynamic random access memory or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit-wide DRAM port or by a 512 x 8-bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM.

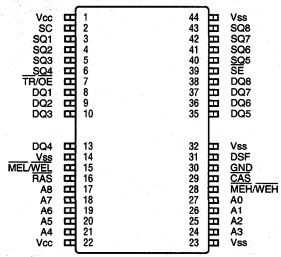
The DRAM portion of the VRAM is functionally similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate data paths: the 8-bit

PIN ASSIGNMENT (Top View)

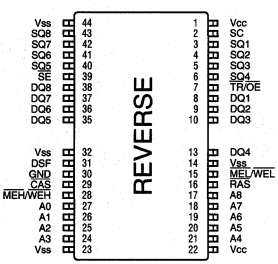
40-Pin SOJ (SDB-3)



40/44-Pin TSOP* (SDE-2)



40/44-Pin TSOP* (SDE-2)



*Consult factory for availability.

NEW VRAM

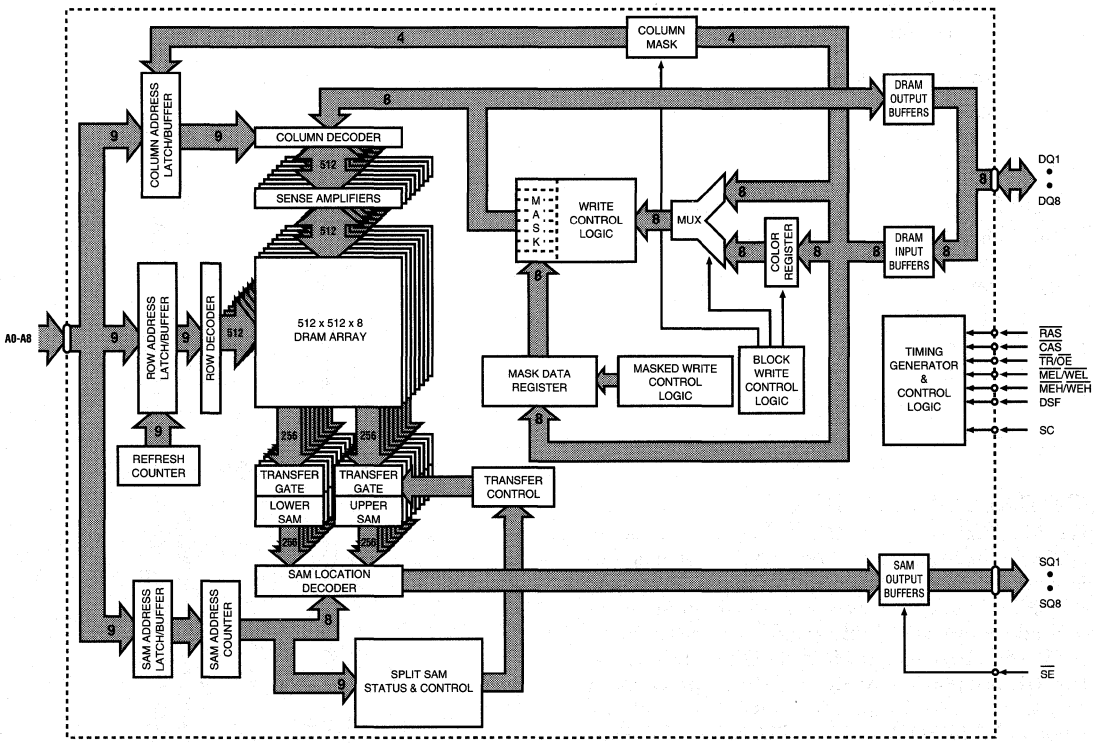
random access I/O port, the eight internal 512-bit-wide paths between the DRAM and the SAM, and the 8-bit serial output port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The MT42C8254 $\overline{WE}$ function and timing are determined by the first NIBBLE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a NIBBLE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower NIBBLE (DQ1-DQ4) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper NIBBLE (DQ5-DQ8).

The operation and control of the MT42C8254 are optimized for high performance graphics using off-the-shelf Super VGA controllers/accelerators. NIBBLE WRITE capability simplifies 16-color VGA modes. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
7	7	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
26 13	28 15	$\overline{MEH/WEH}$ $\overline{MEL/WEL}$	Input	Mask Enable: If $\overline{MEH/WEH}$ or $\overline{MEL/WEL}$ are LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{MEH,L/WEH,L}$ are also used to select a READ ($\overline{MEH,L/WEH,L}$ = H) or WRITE ($\overline{MEH,L/WEH,L}$ = L) cycle when accessing the DRAM and READ TRANSFER ($\overline{MEH,L/WEH,L}$ = H) to the SAM. $\overline{MEL/WEL}$ controls DQ4-DQ1. $\overline{MEH/WEH}$ controls DQ8-DQ5. When performing BLOCK WRITE, both $\overline{ME/WE}$ pins must be LOW. NIBBLE BLOCK WRITE is not supported.
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial output buffers and allows a serial READ operation to occur; otherwise, the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits and strobe the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0-A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles; these pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SQ1-SQ8	Output	Serial Data Out: Output or High-Z.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	Vcc	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	Vss	Supply	Ground

NEW VRAM

FUNCTIONAL DESCRIPTION

The MT42C8254 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/(OE) pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8254 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C8254 supports CBR, RAS-ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8254 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the nine column-address bits are set up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, MEH,L/WEH,L, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For standard single-port DRAMS, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if (MEH,L)/WEH,L are HIGH when CAS goes LOW and remain HIGH until CAS goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH to LOW sometime after RAS falls in order to enable the DRAM output port.

For standard single-port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions: write mask enable and data write enable. ME/(WE) is used when RAS goes LOW to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The NIBBLE WRITE signals MEH/WEH and MEL/WEL can be used together or singly to perform a write mask enable and data write enable. Using one performs a NIBBLE WRITE; using both performs a BYTE WRITE. The WE function is determined by the first NIBBLE WRITE signal to transition LOW and the last to transition HIGH.

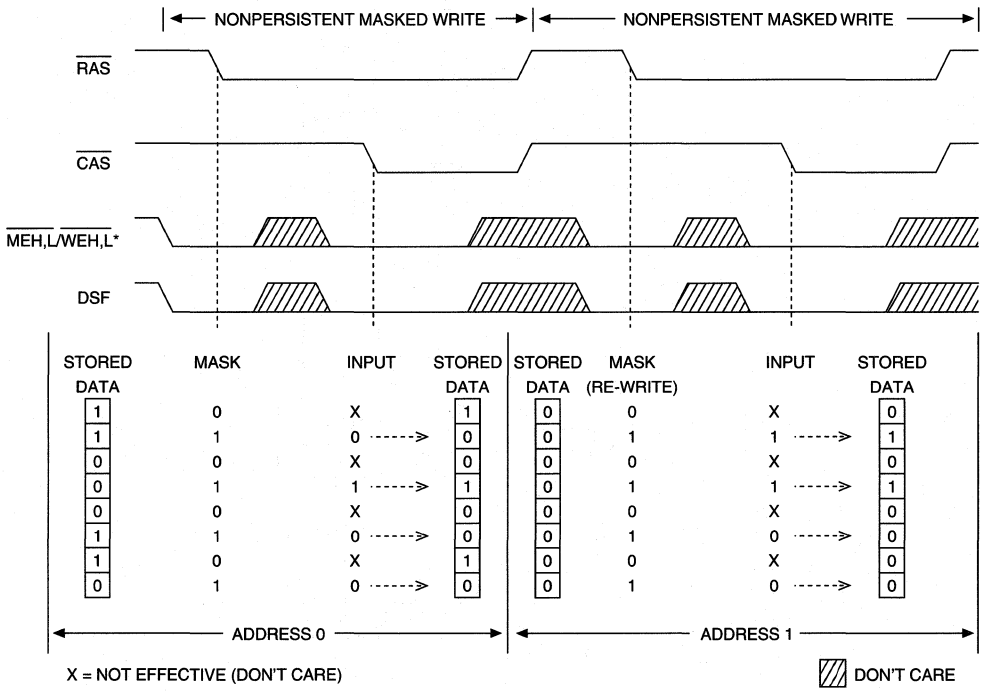
The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (late or early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. When $\overline{MEL}$/($\overline{WEL}$), $\overline{MEH}$/($\overline{WEH}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed. MASKED WRITE can be executed as a NIBBLE or BYTE MASKED WRITE.

The MT42C8254 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). DQ1-DQ4 or DQ5-DQ8 may be written independently during NIBBLE MODE. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.



* One or two write enables are active, depending upon whether a NIBBLE or BYTE MASKED WRITE is to be performed.

Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NEW VRAM

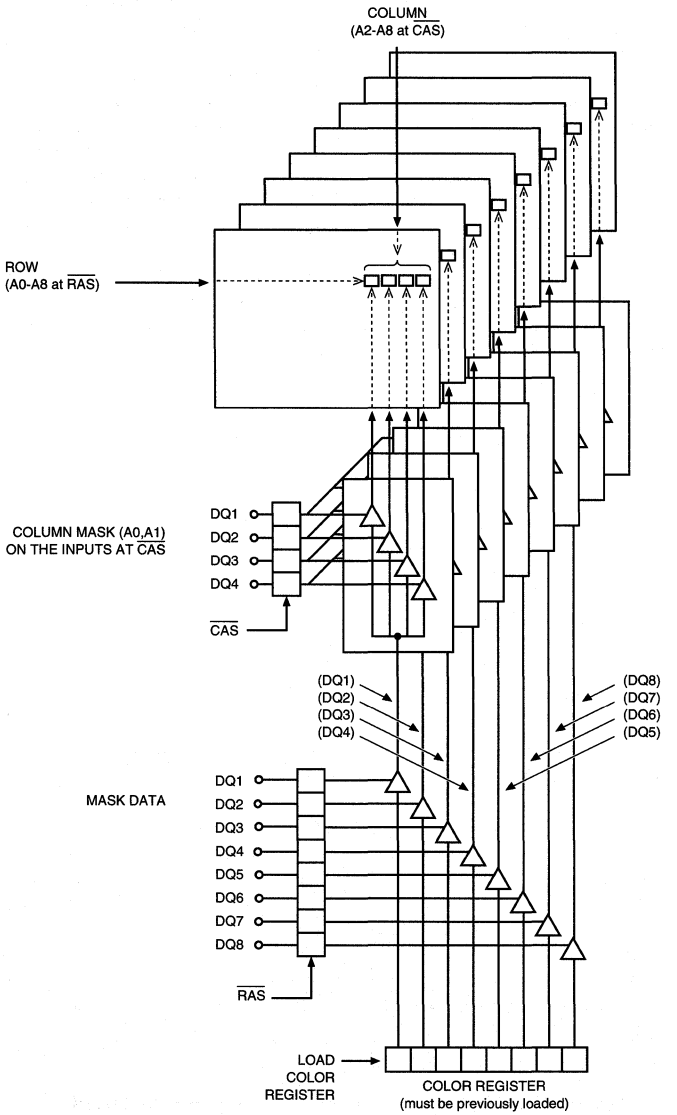


Figure 2
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8254 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3 and 4) are then used to determine what combination of the four column locations will be changed (see Table 1). The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

BLOCK WRITE can only be executed as a byte BLOCK WRITE. Both $\overline{MEL}/\overline{WEL}$ and $\overline{MEH}/\overline{WEH}$ must be "active" for any BLOCK WRITE cycle.

MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the eight bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. Any combination of the eight bit-planes may be masked, along with any combination of the four column locations, by using both the column mask input and the MASKED WRITE function of BLOCK WRITE. MASKED BLOCK WRITE can only be executed on a byte basis; nibble MASKED BLOCK WRITE is not allowed.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except that DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles. Both $\overline{ME}/\overline{WE}$ pins must be in the same state when loading the color register; only byte loads are allowed.

Table 1
DQ Masking of Columns (at $\overline{CAS}$ falling)

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

TRANSFER OPERATIONS

The MT42C8254 provides two TRANSFER operations. These TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW and both $\overline{MEH}/\overline{WEH}$, and $\overline{MEL}/\overline{WEL}$ are HIGH at the falling edge of $\overline{RAS}$. DSF at the falling edge of $\overline{RAS}$ selects between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER

A TRANSFER operation with DSF LOW when $\overline{RAS}$ goes LOW is a READ TRANSFER cycle. The row-address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every RT in order to load a valid Tap address.

An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal nine-bit register. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$.

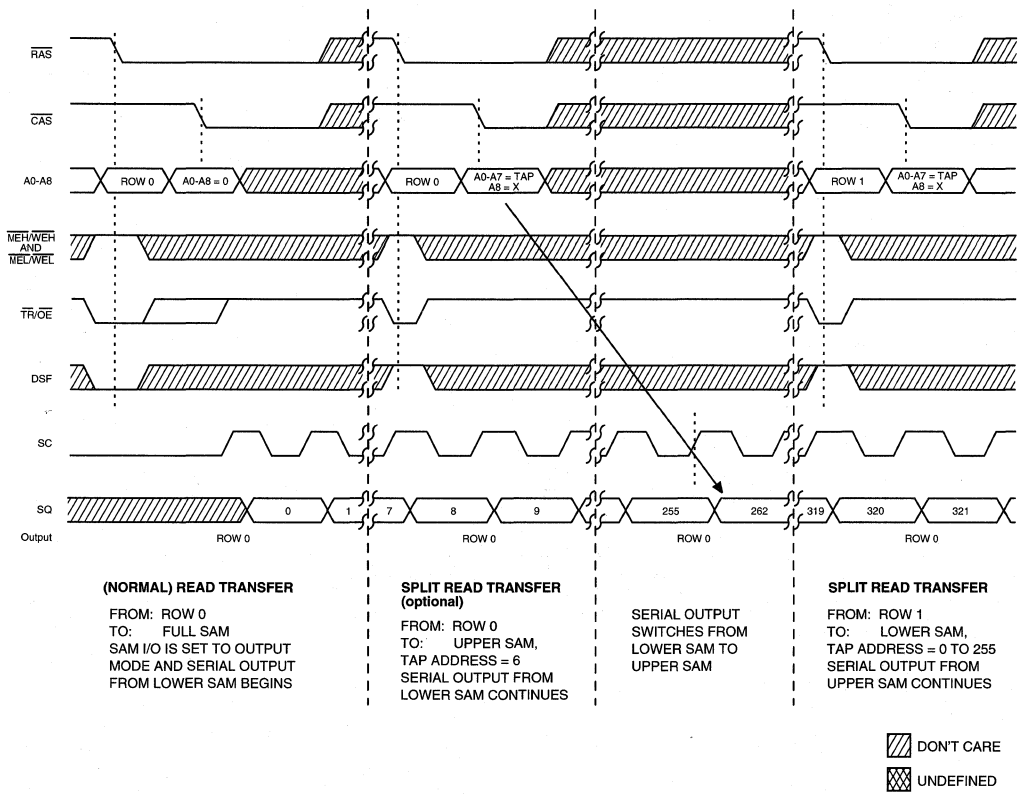


Figure 3
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER must occur between the last clock of "old" data and first clock of "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputting data.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, making it independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference as to which half of the SAM the access will begin. Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As with nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address (at the HIGH-to-LOW transition of $\overline{CAS}$). Address pin A8 is a "don't care" when the Tap address is loaded. A8 is generated internally and automatically selects the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need be done only if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1), and an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. For example, in Figure 3, the next step would be to wait until row one data shifts out of the lower SAM and executes an SRT of the upper half of row one to the upper SAM. If the half boundary is reached before an SRT is completed for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half, or at zero if going to the lower half (see Figure 4).

SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial output buffers.

Serial output of the SAM contents will begin at the serial start address that was loaded in the SAM address counter during a READ or SRT cycle. The SC input increments the address counter and presents the contents of the next SAM location to the eight-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. The address count will wrap around (after count 511) to Tap address zero if in the "full" SAM modes.

POWER-UP and INITIALIZATION

After V_{CC} is at specified operating conditions for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = \overline{TR}/\overline{OE} \geq V_{IH}$ during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8254 is completely static in operation and does not require refresh or initialization. The SAM port will power up with the output pins (SQs) in High- Z regardless of the state of $\overline{SE}$. The color register will contain random data after power-up.

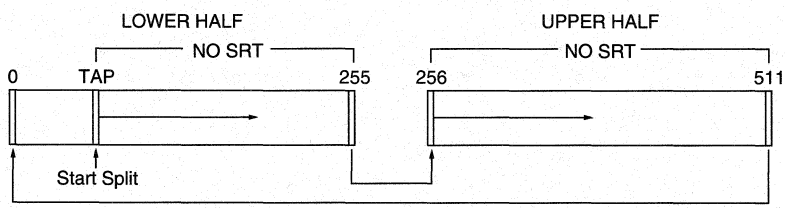


Figure 4
SPLIT SAM TRANSFER

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTER
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE[3]	COLOR
	DRAM OPERATIONS										
CBR	CBR REFRESH	0	X	1[6]	1[6]	—	X	X	—	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0[7]	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1[8]	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0[8]	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1[8]	1	1	ROW[4]	X	X	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1[8]	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1[8]	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is last. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is last. During a NIBBLE WRITE (no BLOCK WRITE), only one of the two WEs is used.
4. The ROW that is addressed will be refreshed, but a ROW address is not required.
5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).
6. The MT42C8254 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.
7. If a NIBBLE MASKED WRITE is to be executed, only one of the two write enables needs to be LOW at the RAS falling edge.
8. Both ME/WEs must be at the same state during these cycles; only byte-wide operations are supported.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input ($0V \le V_{IN} \le V_{CC}$); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SQ	$C_{I/O}$		9	pF	2

NEW VRAM

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	125	110	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC2}	115	100	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	10	10	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	125	110	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	125	110	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	135	120	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	175	160	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC8}	165	150	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤V_{IL})	I_{CC9}	60	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	175	160	mA	3, 4, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	175	160	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	185	170	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	90		95		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		20		20	ns	
Access time from column-address	tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	
Row address setup time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		ns	
Column-address hold time	tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$	tOFF	3	20	3	20	ns	20,23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	tOD	3	10	3	10	ns	20,23
Output disable hold time from start of WRITE	tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	tROH	0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ to $\overline{RAS}$ HIGH hold time	^tTRD	15		15		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
SPLIT TRANSFER setup time	^tSTS	25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	45		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	30		30		ns	

NEW VRAM

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

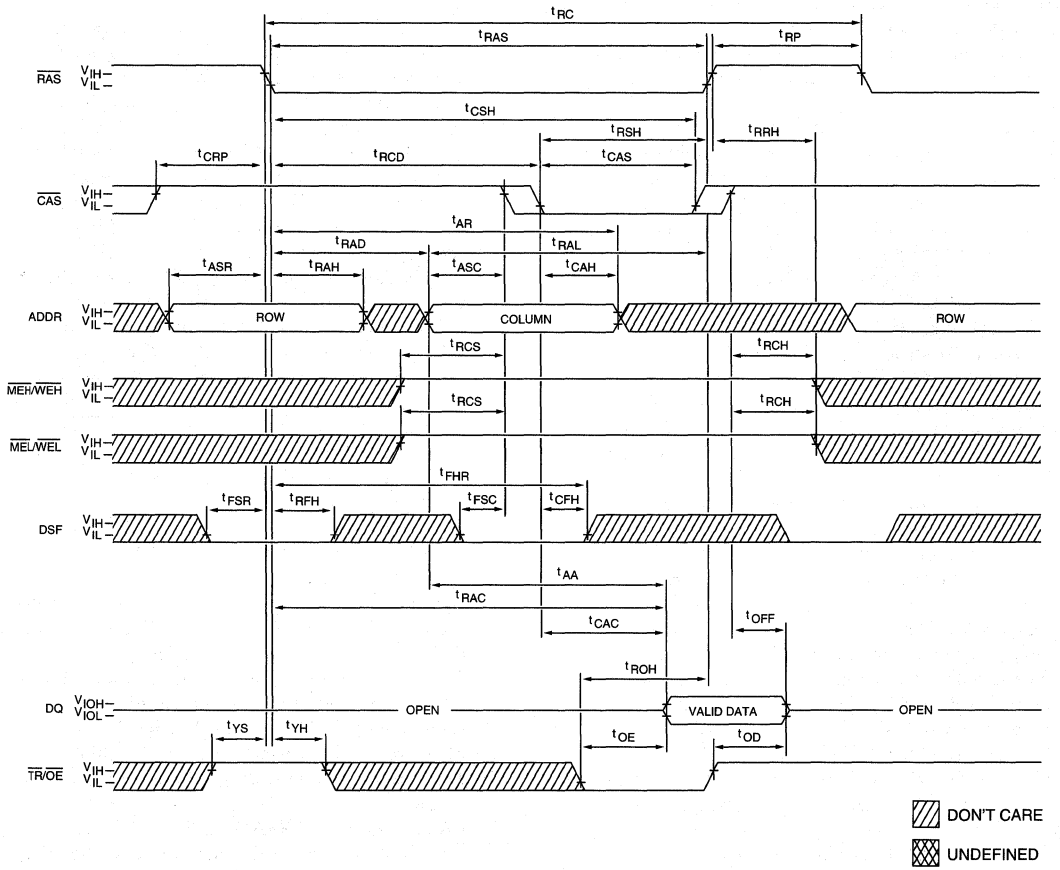
AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	22		25		ns	
Access time from SC	^tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	8		10		ns	
$\overline{SE}$ pulse width	^tSE	8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16.7ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from zero to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing is measured with a load equivalent to one TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV; V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate, but the WRITE will be valid if ^tOD and ^tOEH are met. (See the LATE-WRITE AC Timing diagram.)
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW, then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to one TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Measured with two address changes while $\overline{RAS}$ = V_{IL}.
26. Measured with one address change while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. (^tSOH = ^tSAC - output transition time); this is guaranteed by design.

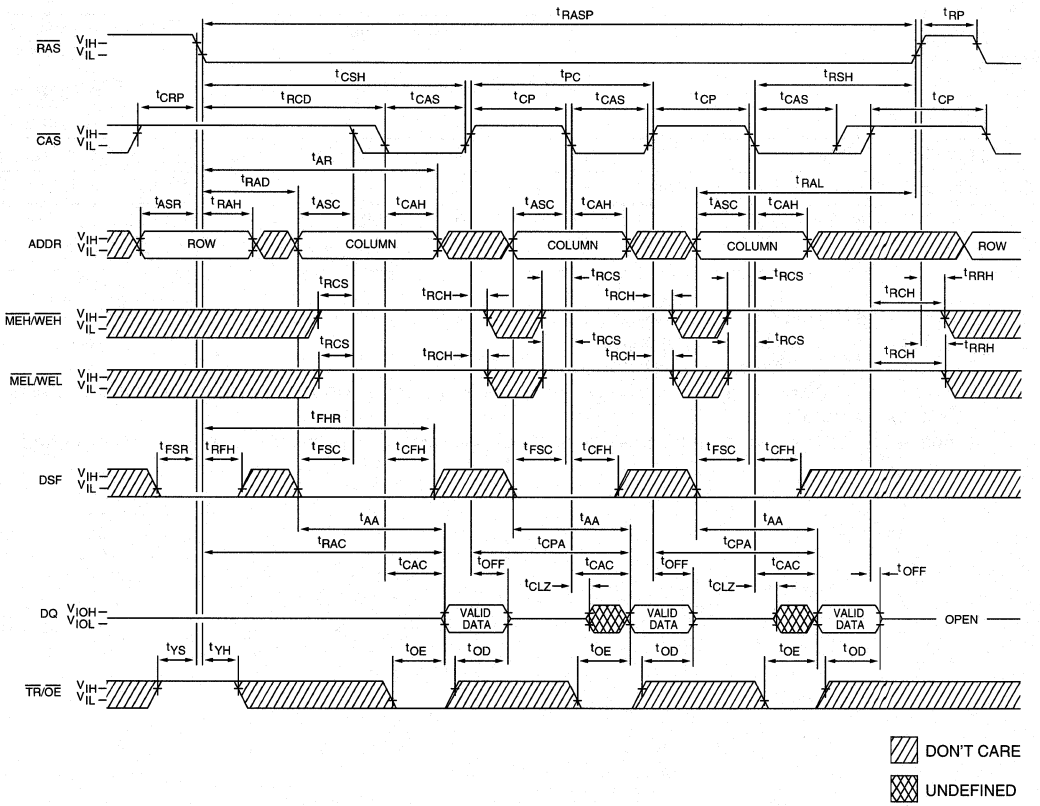
NEW VRAM

DRAM READ CYCLE



NEW VRAM

DRAM FAST-PAGE-MODE READ CYCLE



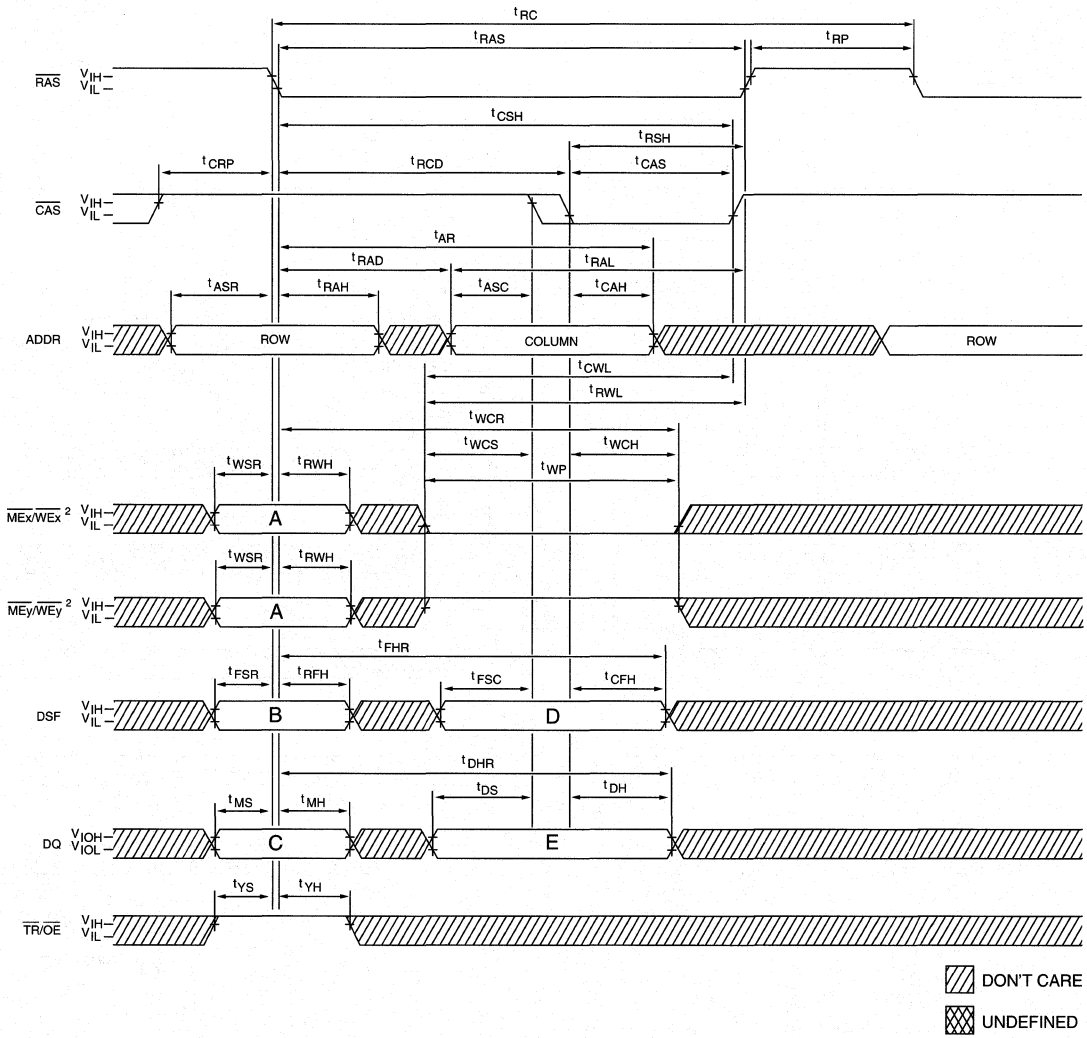
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0[3]	0	Write Mask	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1[4]	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0[4]	0	Write Mask	1	Column Mask
Load Color Register	1[4]	1	X	1	Color Data

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs last.
3. If a NIBBLE MASKED WRITE is to be performed, only one of the two write enables needs to be LOW at the $\overline{RAS}$ falling edge.
4. Both $\overline{ME}/\overline{WE}$s must be at the same state during these cycles; only byte-wide operations are supported.

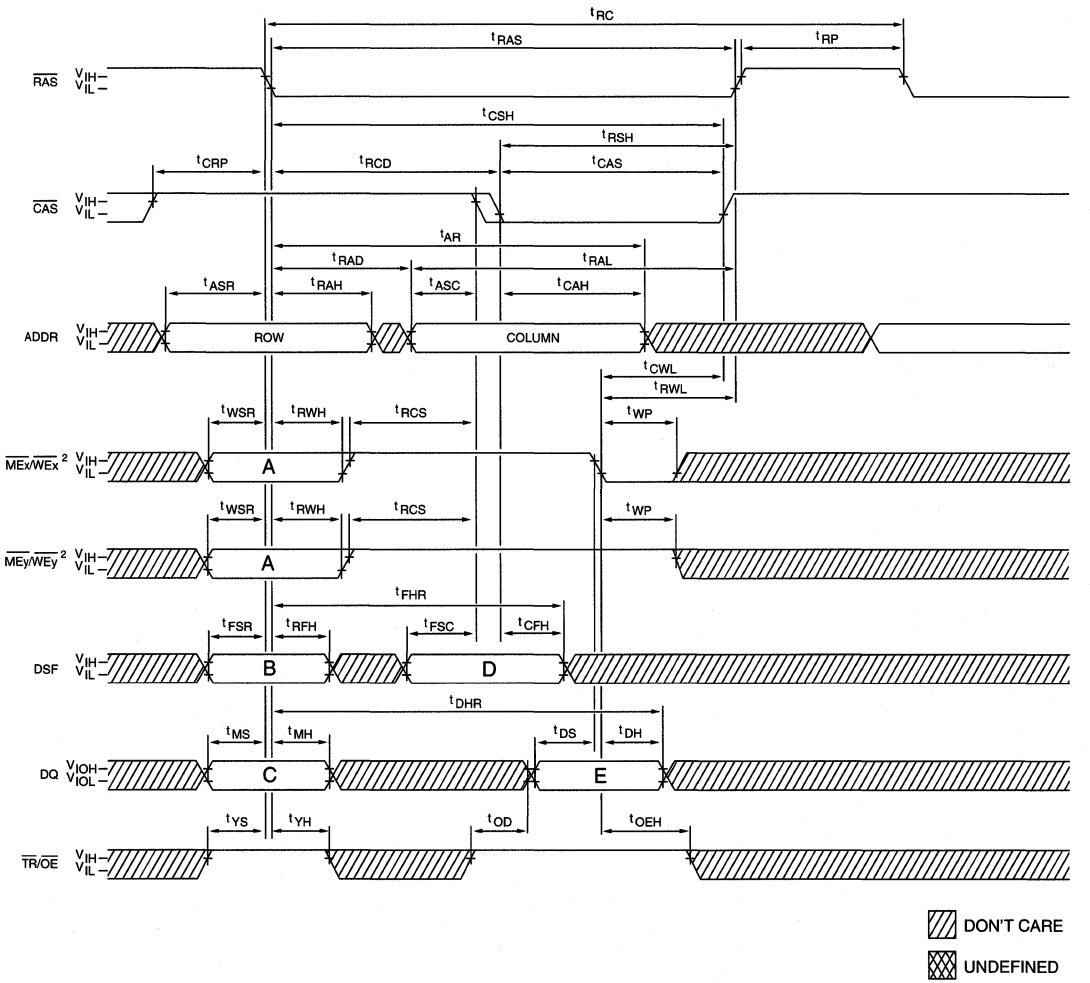
DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. $\overline{WEH}$ and $\overline{WEL}$ apply to the $\overline{WEx}$ waveform if the corresponding nibble participates in the WRITE; if not, apply the $\overline{WEy}$ waveform.

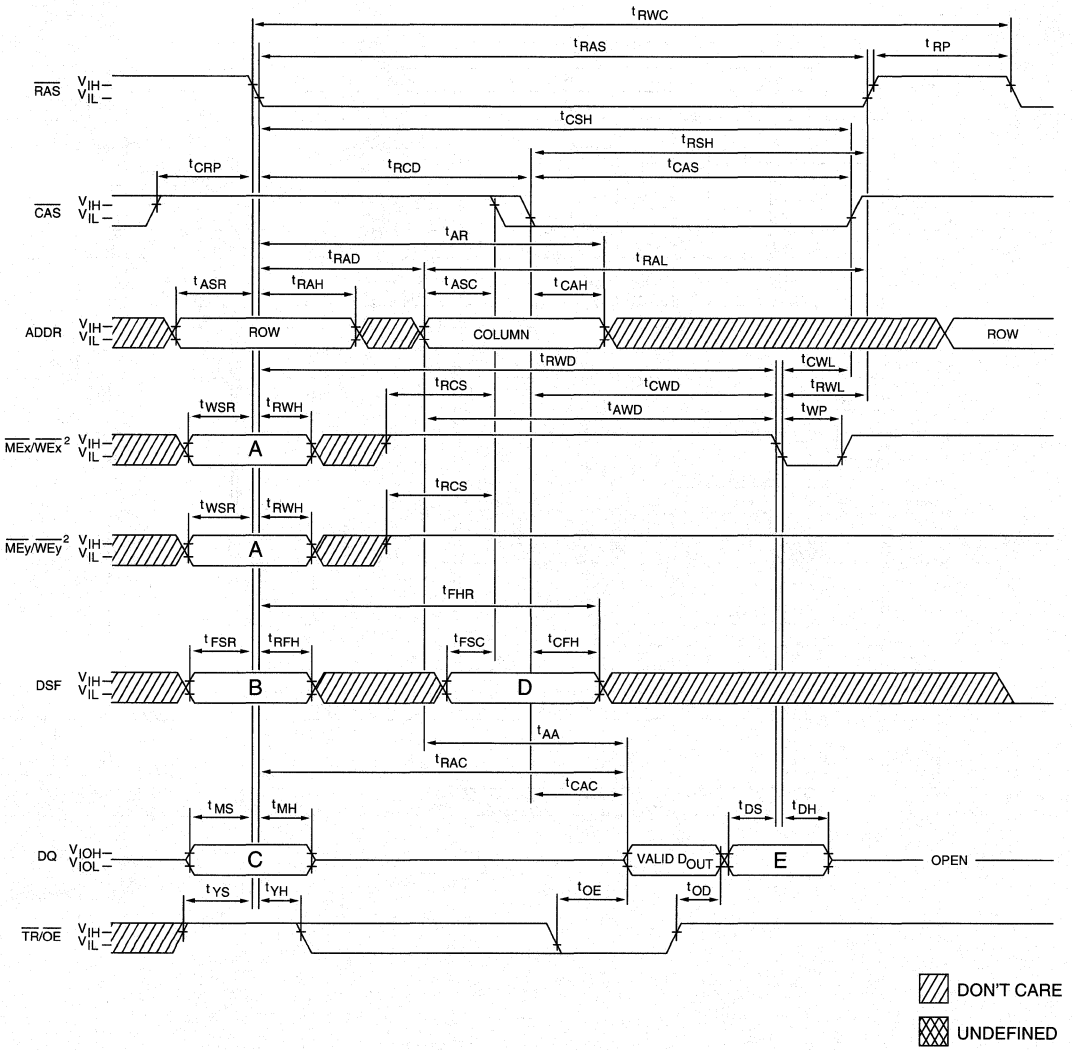
NEW VRAM

DRAM LATE-WRITE CYCLE



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. $\overline{WEH}$ and $\overline{WEL}$ apply to the $\overline{WEx}$ waveform if the corresponding nibble participates in the WRITE; if not, apply the $\overline{WEy}$ waveform.

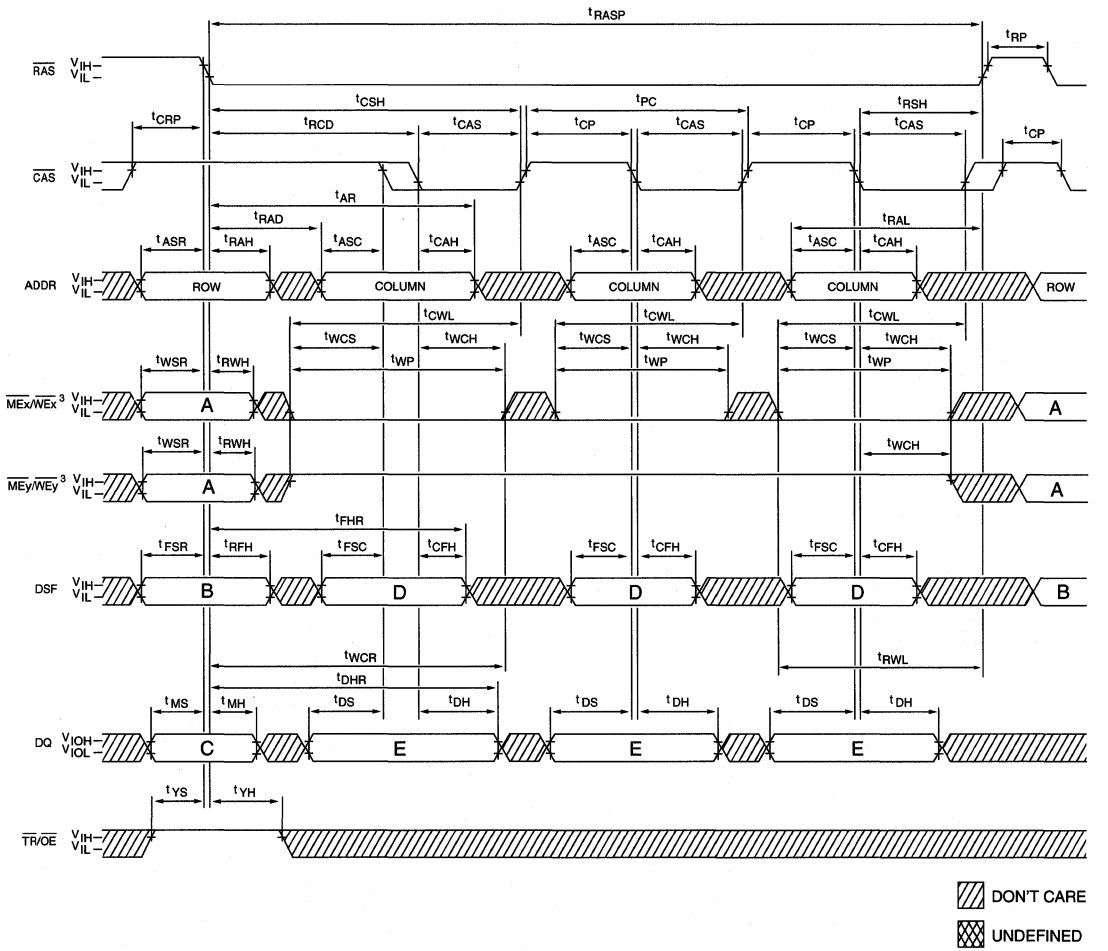
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. $\overline{WEH}$ and $\overline{WEL}$ apply to the $\overline{WEx}$ waveform if the corresponding nibble participates in the WRITE; if not, apply the $\overline{WEy}$ waveform.

NEW VRAM

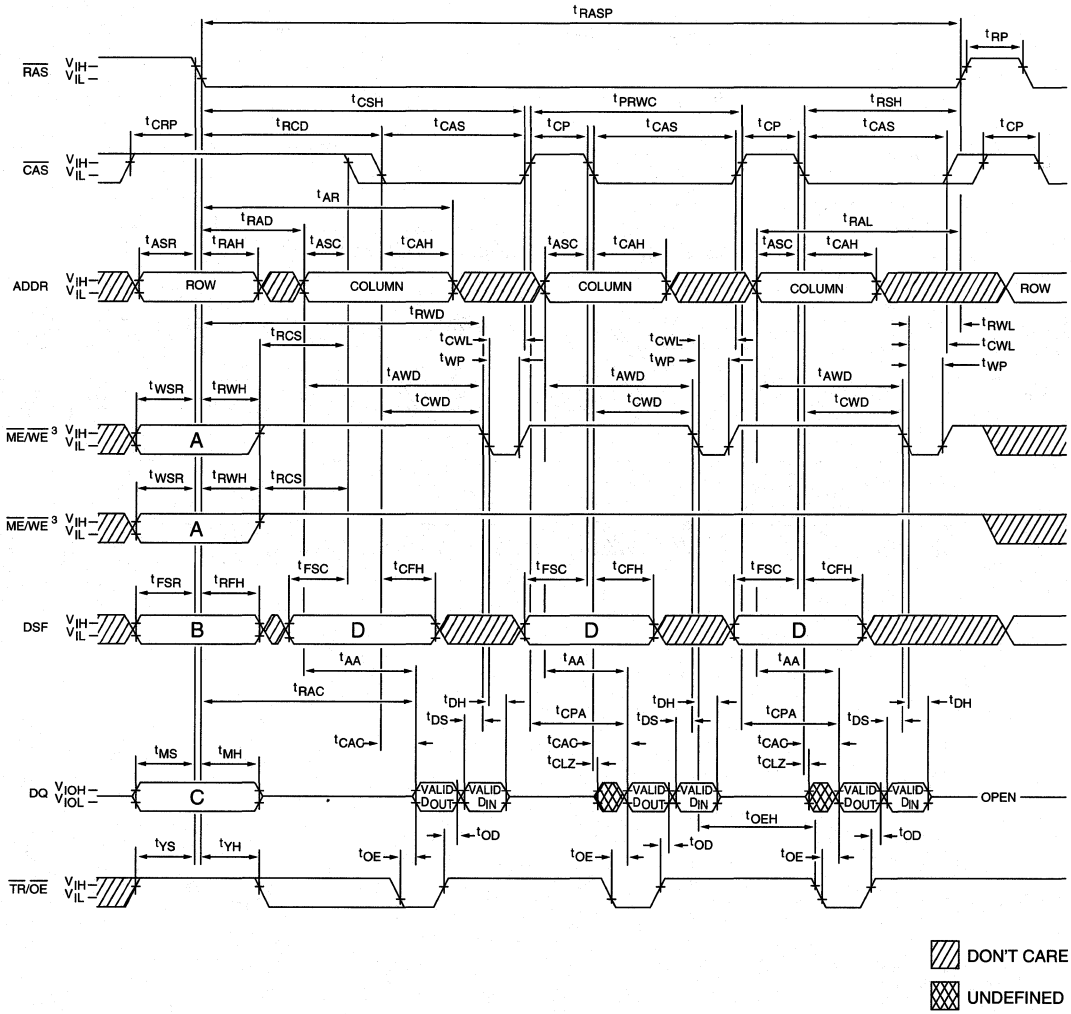
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
3. $\overline{WEH}$ and $\overline{WEL}$ apply to the $\overline{WEx}$ waveform if the corresponding nibble participates in the WRITE; if not, apply the $\overline{WEy}$ waveform.

NEW VRAM

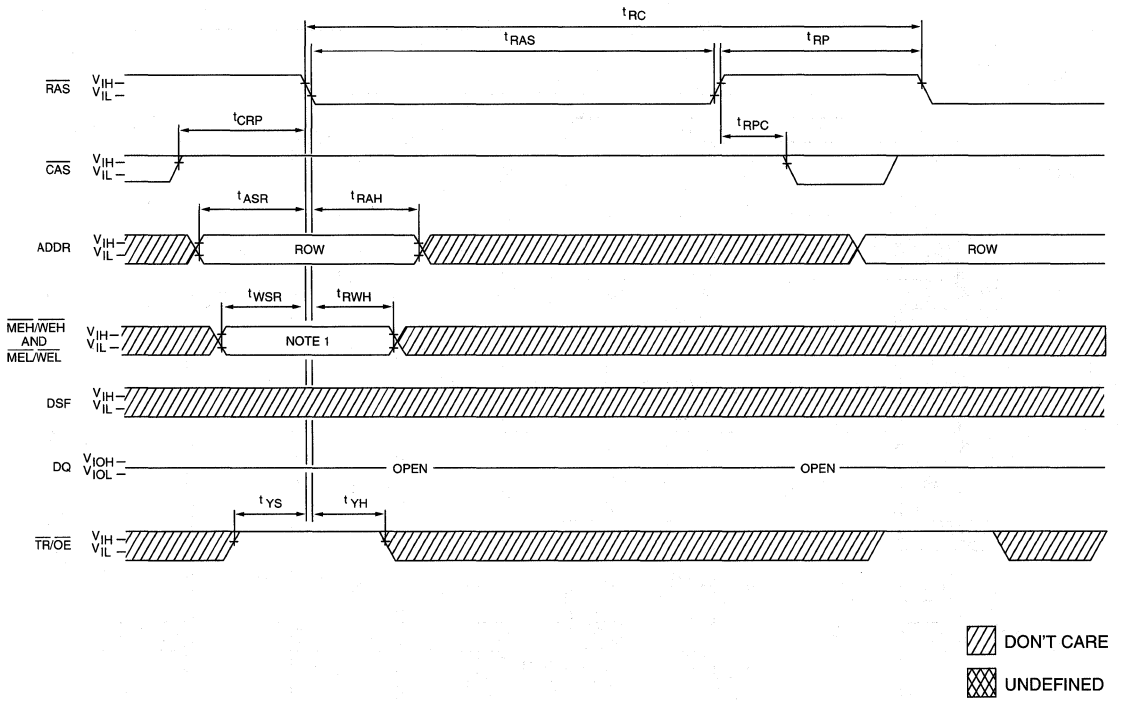
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B", "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
3. $\overline{WEH}$ and $\overline{WEL}$ apply to the $\overline{WEx}$ waveform if the corresponding nibble participates in the WRITE; if not, apply the $\overline{WEy}$ waveform.

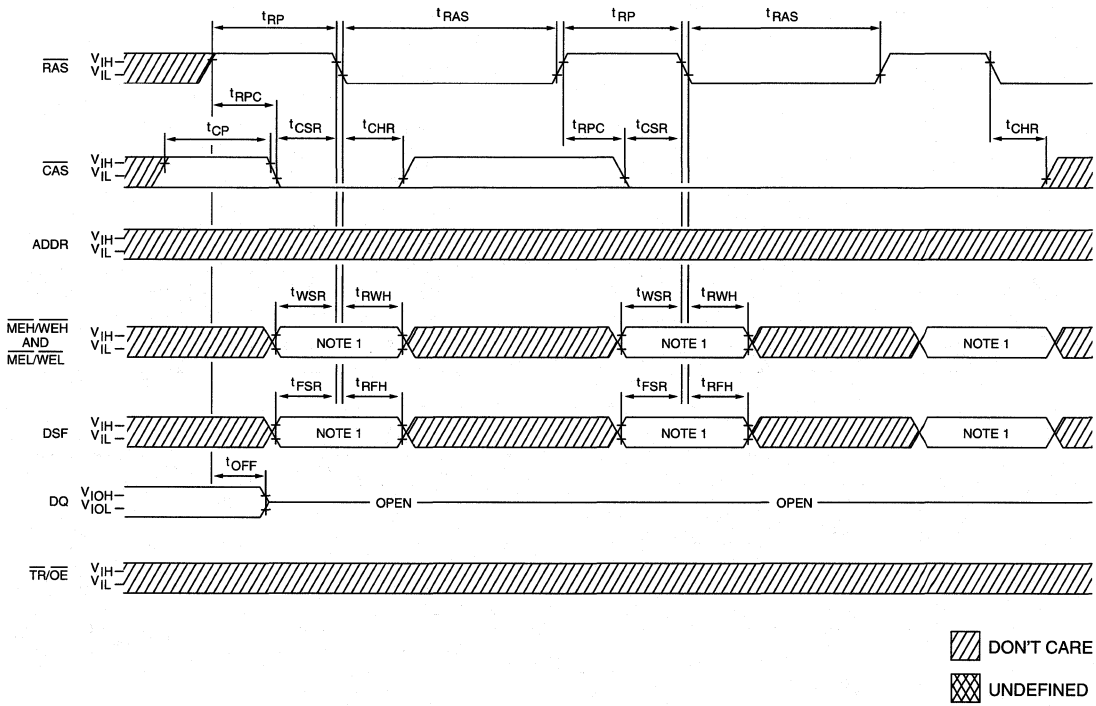
NEW ■ VRAM

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



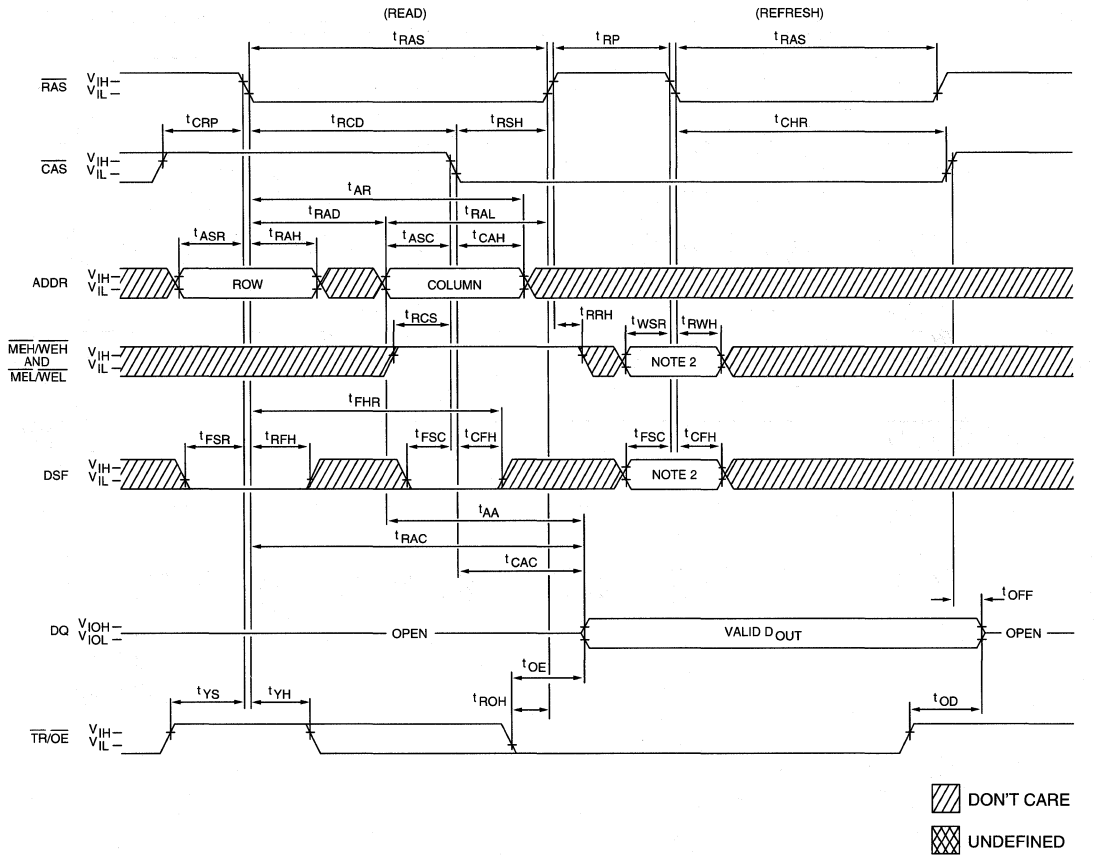
NEW VRAM

CBR REFRESH CYCLE



NOTE: 1. The MT42C8254 operates properly with $\overline{ME}/\overline{WE}$ and DSF = "don't care", but to ensure compatibility with all 2 Meg VRAM feature sets, Micron recommends that they be HIGH ("1").

DRAM HIDDEN-REFRESH CYCLE

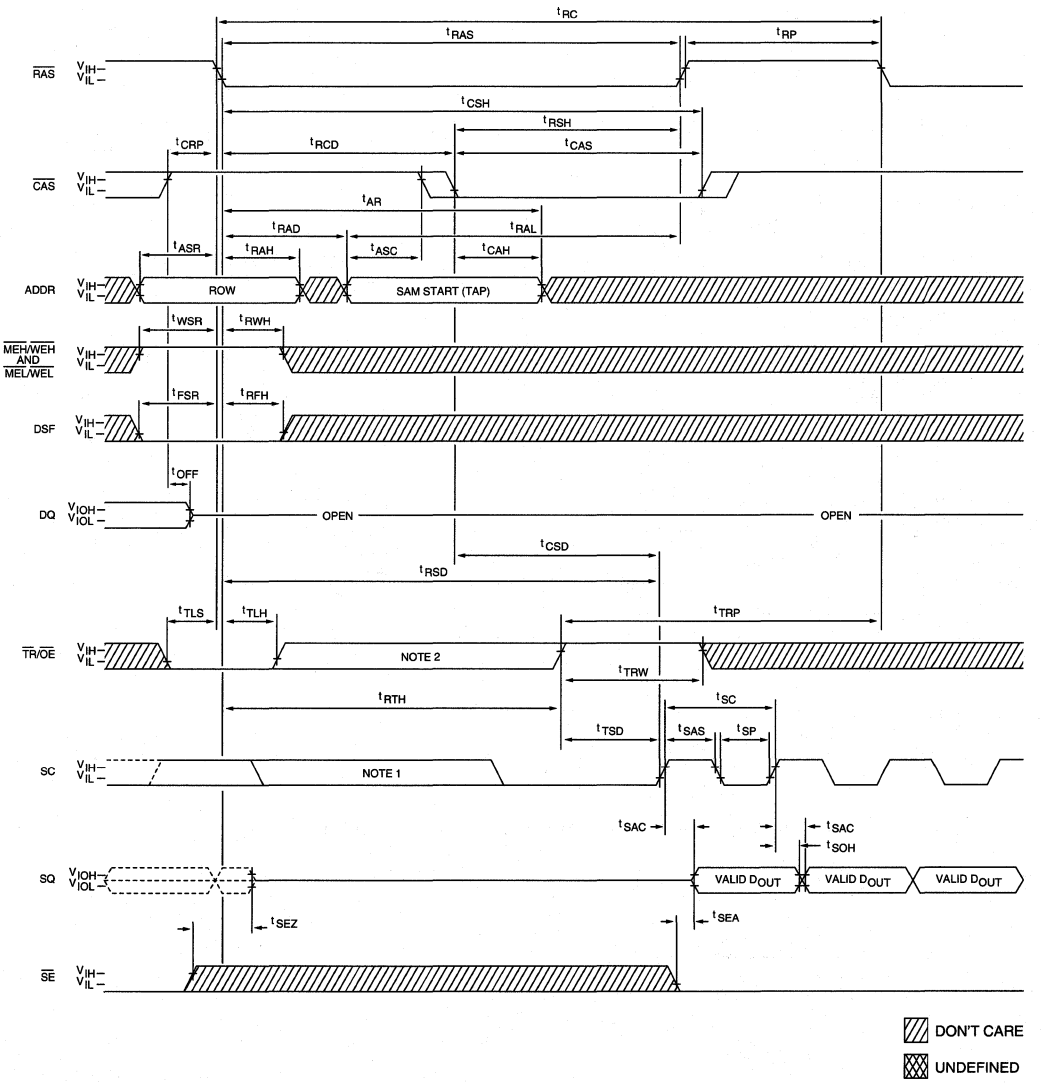


NOTE: 1. A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

2. The MT42C8254 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care", but to ensure compatibility with all 2 Meg VRAM feature sets, Micron recommends that they be HIGH ("1").

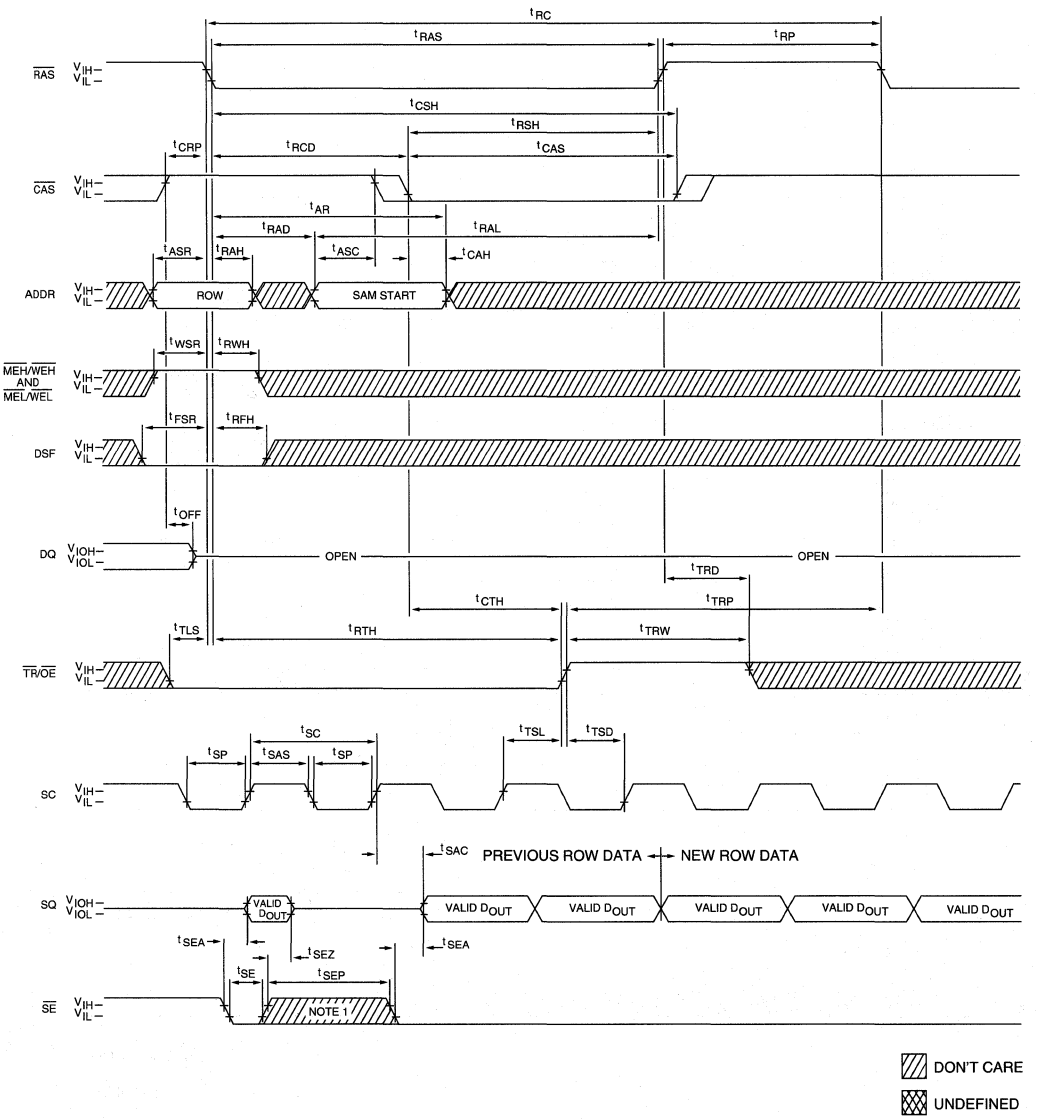
NEW VRAM

READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When serial part was previously High-Z or SC idle)



NOTE: 1. There must be no rising edges on the SC input during this time period.
2. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge, and tTSD must be met.

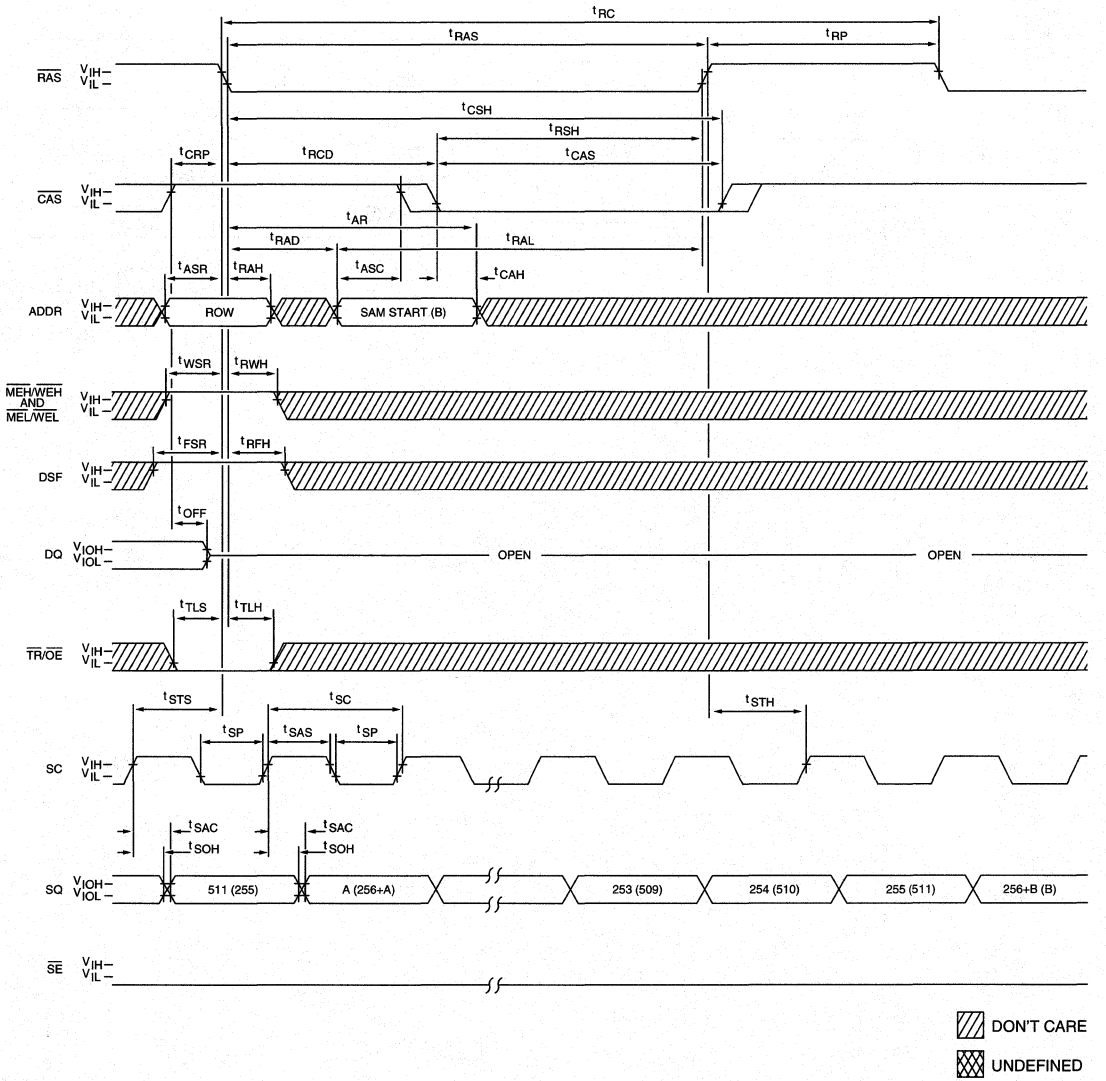
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

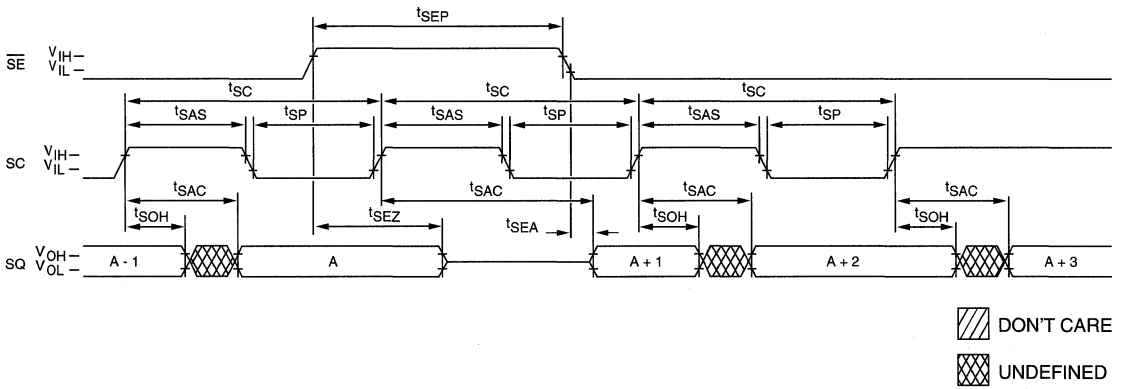
NEW VRAM

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NEW VRAM

SAM SERIAL OUTPUT



VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE
- Dual-port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times: 70ns random, 22ns serial

SPECIAL FUNCTIONS

- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])
  70ns, 22/22ns -7
  80ns, 25/25ns -8

- Packages
  Plastic SOJ (400 mil) DJ
  Plastic TSOP (400 mil) TG*
  Plastic TSOP (400 mil) reverse pinout RG*

- Part Number Example: MT42C8255DJ-7

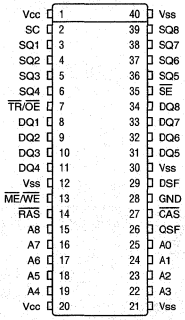
GENERAL DESCRIPTION

The MT42C8255 is a high-speed, dual-port CMOS dynamic random access memory or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit-wide DRAM port or by a 512 x 8 bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM.

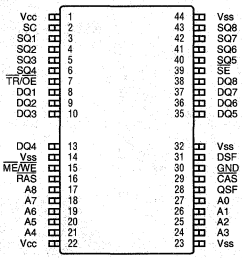
The DRAM portion of the VRAM is functionally similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer

PIN ASSIGNMENT (Top View)

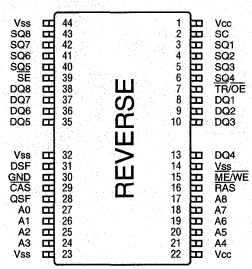
40-Pin SOJ (SDB-3)



40/44-Pin TSOP (SDE-2)



40/44-Pin TSOP* (SDE-2)



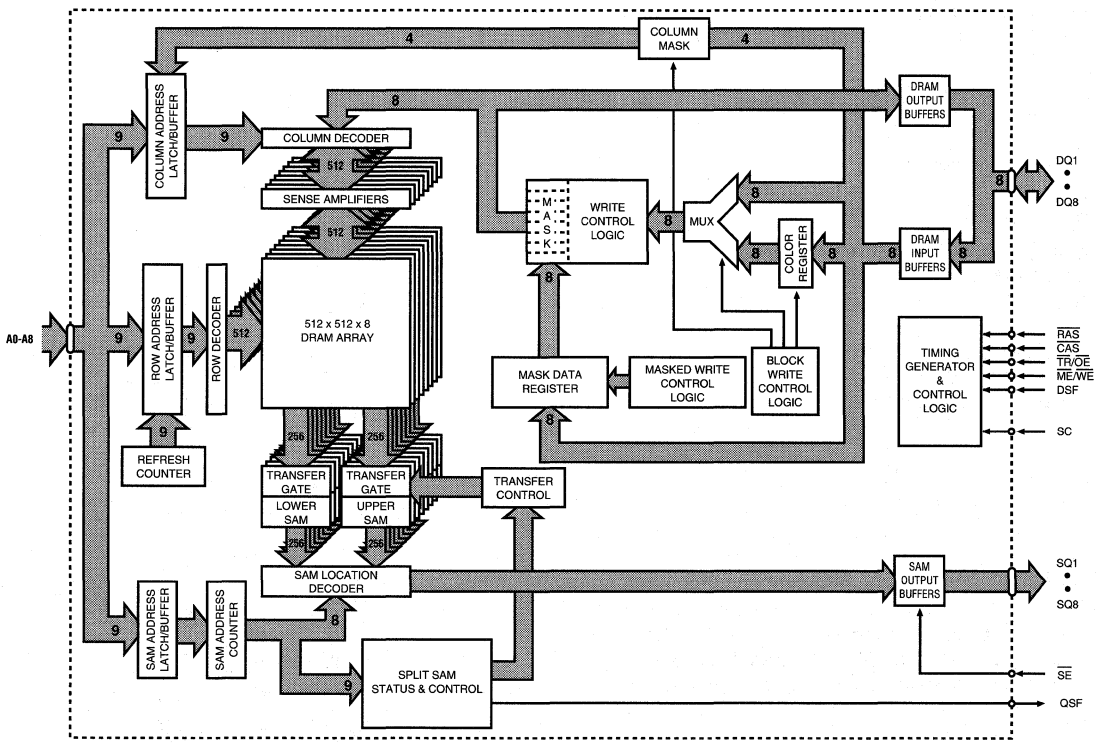
*Consult factory for availability.

are accomplished using three separate data paths: the 8-bit random access I/O port, the eight internal 512-bit-wide paths between the DRAM and the SAM, and the 8-bit serial output port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8255 are optimized for high performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
7	7	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
13	15	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM and READ TRANSFER ($\overline{ME/WE}$ = H) to the SAM.
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial output buffers and allows a serial READ operation to occur; otherwise, the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits and strobe the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SQ1-SQ8	Output	Serial Data Out: Output or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	Vcc	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8255 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8255 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C8255 supports CBR, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8255 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW and remains HIGH until $\overline{CAS}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/\overline{WE}$ performs two functions; write mask enable and data write enable. $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any nonmasked DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE

The MASKED WRITE (RWM) feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. When $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8255 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST-PAGE-MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

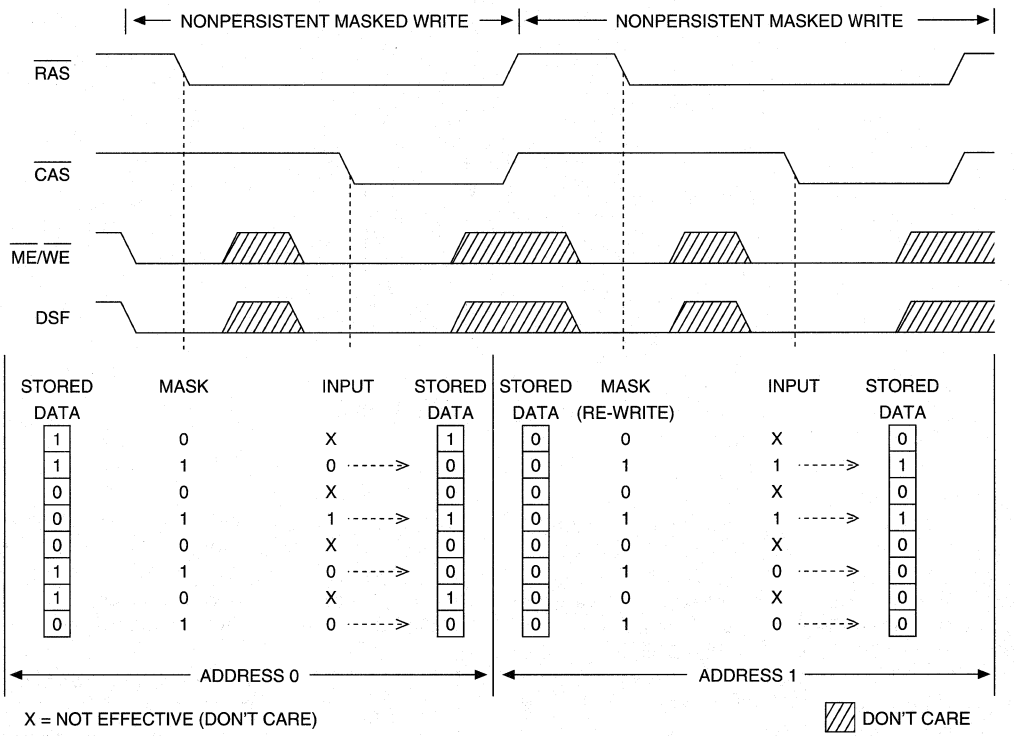


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

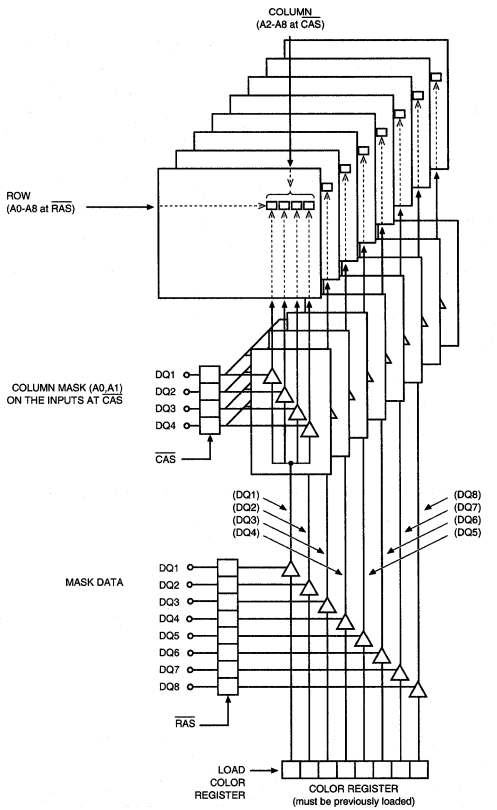


Figure 2
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8255 will perform a BLOCK WRITE (BW) cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE (BWM) operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of 4 column locations instead of just one column location.

The combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the eight bit planes may be masked, along with any combination of the four column locations.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER (LCR) cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

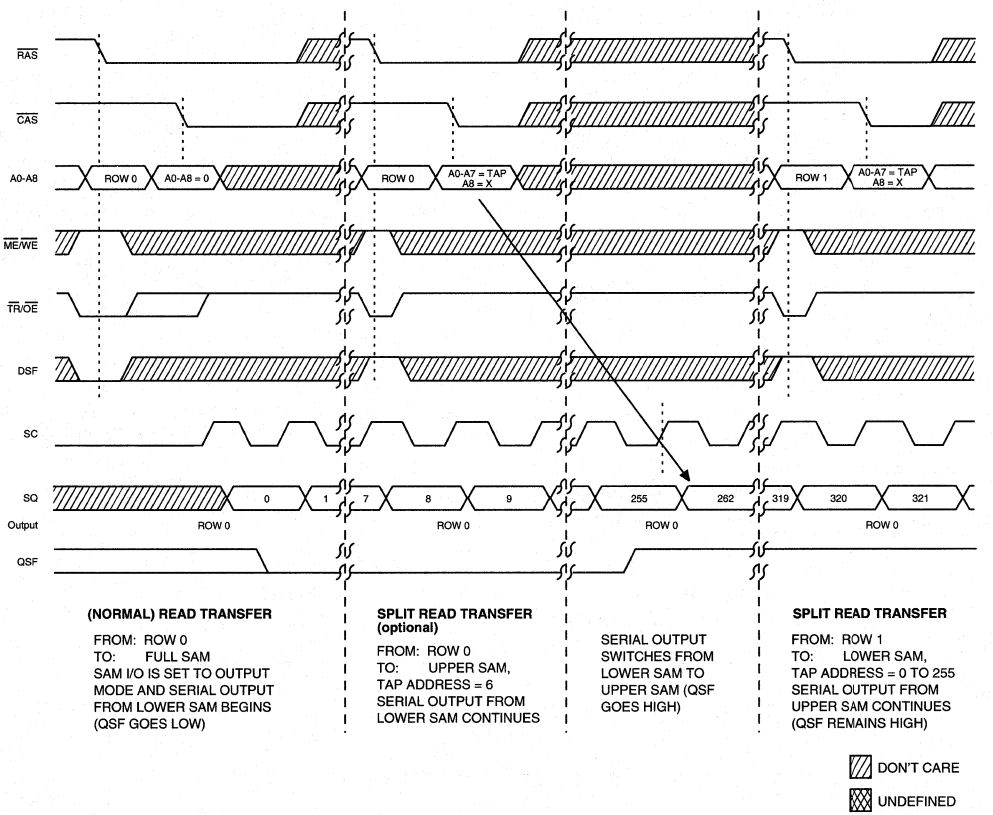


Figure 3
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

READ TRANSFER

If $\overline{ME}/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER (RT) cycle is selected. The row-address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every RT in order to load a valid Tap address. An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$.

SPLIT READ TRANSFER

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputing data.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF). Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is ≠0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1) the QSF output goes HIGH, and if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 3 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 4).

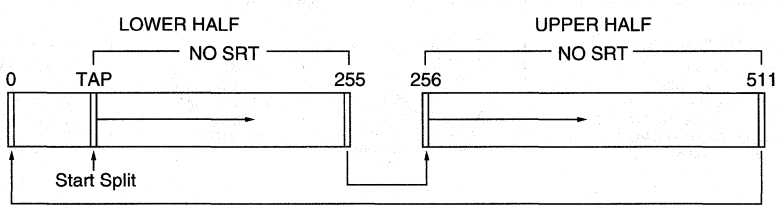


Figure 4
SPLIT SAM TRANSFER

SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SRT cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

POWER-UP and INITIALIZATION

After V_{CC} is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = \overline{TR}/\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8255 is completely static in operation and does not require refresh or initialization. The SAM port will power-up with the Output pins (SQs) in High-Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTER
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE[3]	COLOR
	DRAM OPERATIONS										
CBR	CBR REFRESH	0	X	1[6]	1[6]	—	X	X	—	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[4]	X	X	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but a ROW address is not required.
5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).
6. The MT42C8255 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME/WE}$, $\overline{TR/OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	125	110	mA	3, 4 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC2}	115	100	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	10	10	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	125	110	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	125	110	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	135	120	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	175	160	mA	3, 4 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC8}	165	150	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤V_{IL})	I_{CC9}	60	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	175	160	mA	3, 4 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	175	160	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	185	170	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	^tRWC	170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	90		95		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		20	ns	
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$	^tOFF	3	20	3	20	ns	20,23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	^tOD	3	10	3	10	ns	20,23
Output disable hold time from start of WRITE	^tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	^tROH	0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ to $\overline{RAS}$ HIGH hold time	^tTRD	15		15		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
SC to QSF delay time	^tSQD		25		30	ns	
SPLIT TRANSFER setup time	^tSTS	25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	45		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		75		75	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	30		30		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

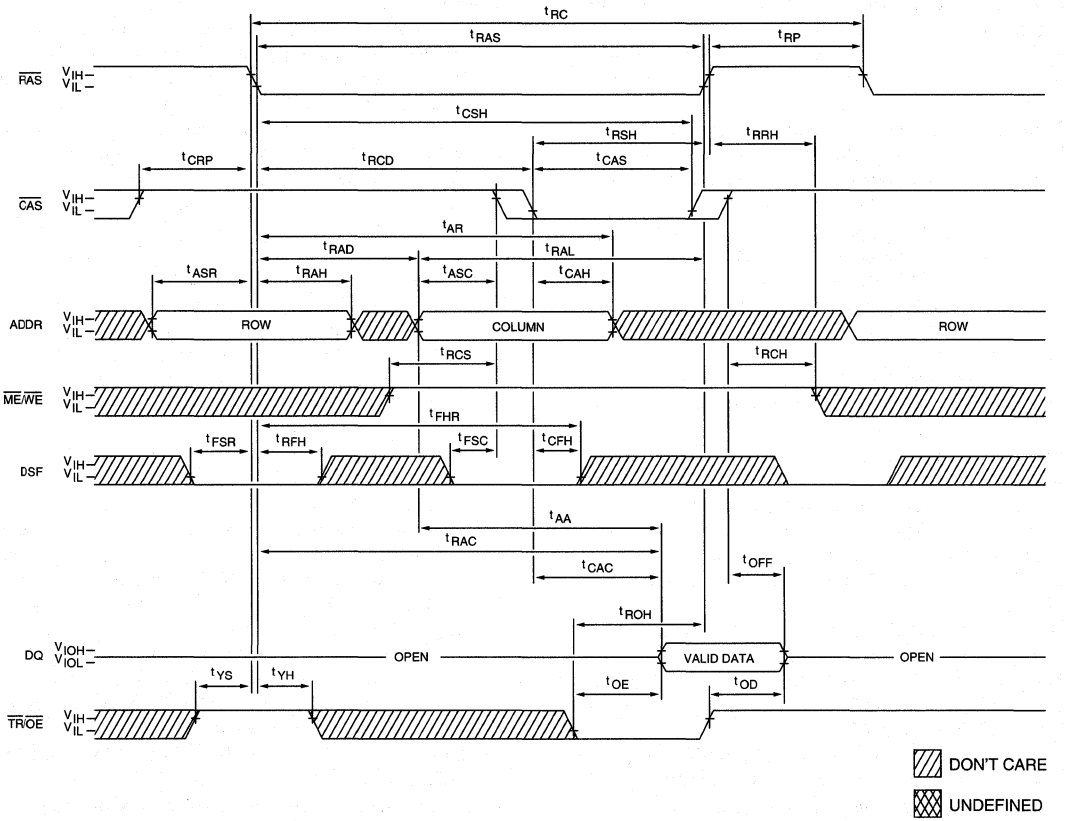
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	22		25		ns	
Access time from SC	^tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	8		10		ns	
$\overline{SE}$ pulse width	^tSE	8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24

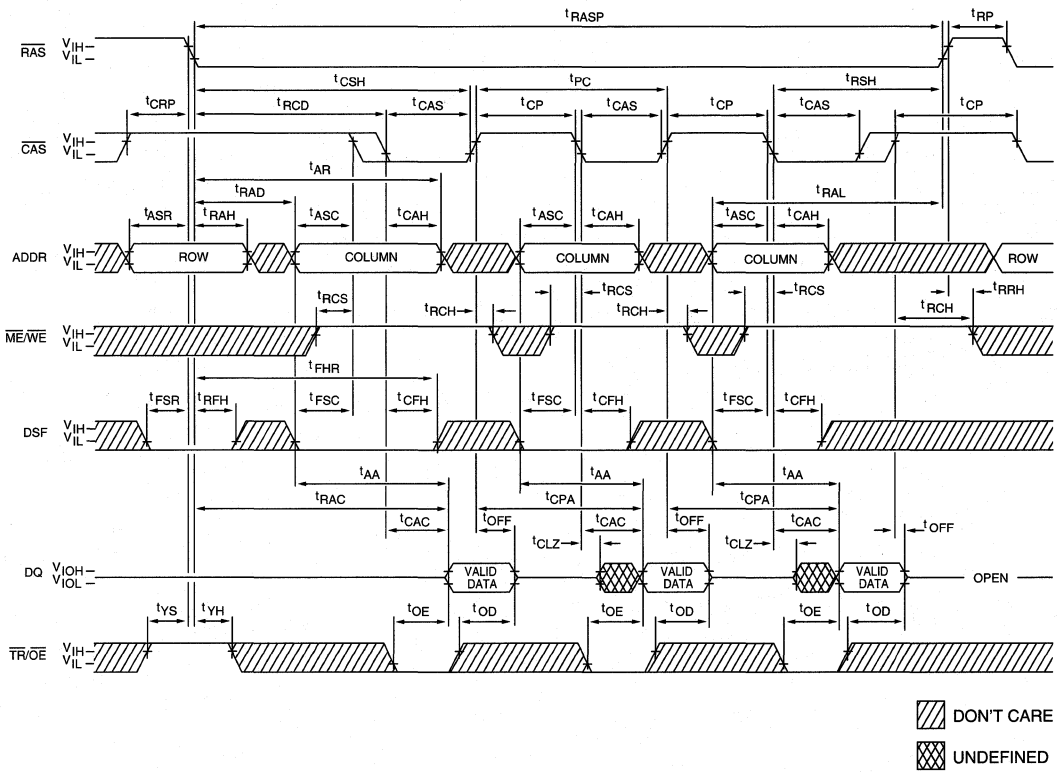
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16.7ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ($^tSOH = ^tSAC$ - output transition time); this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



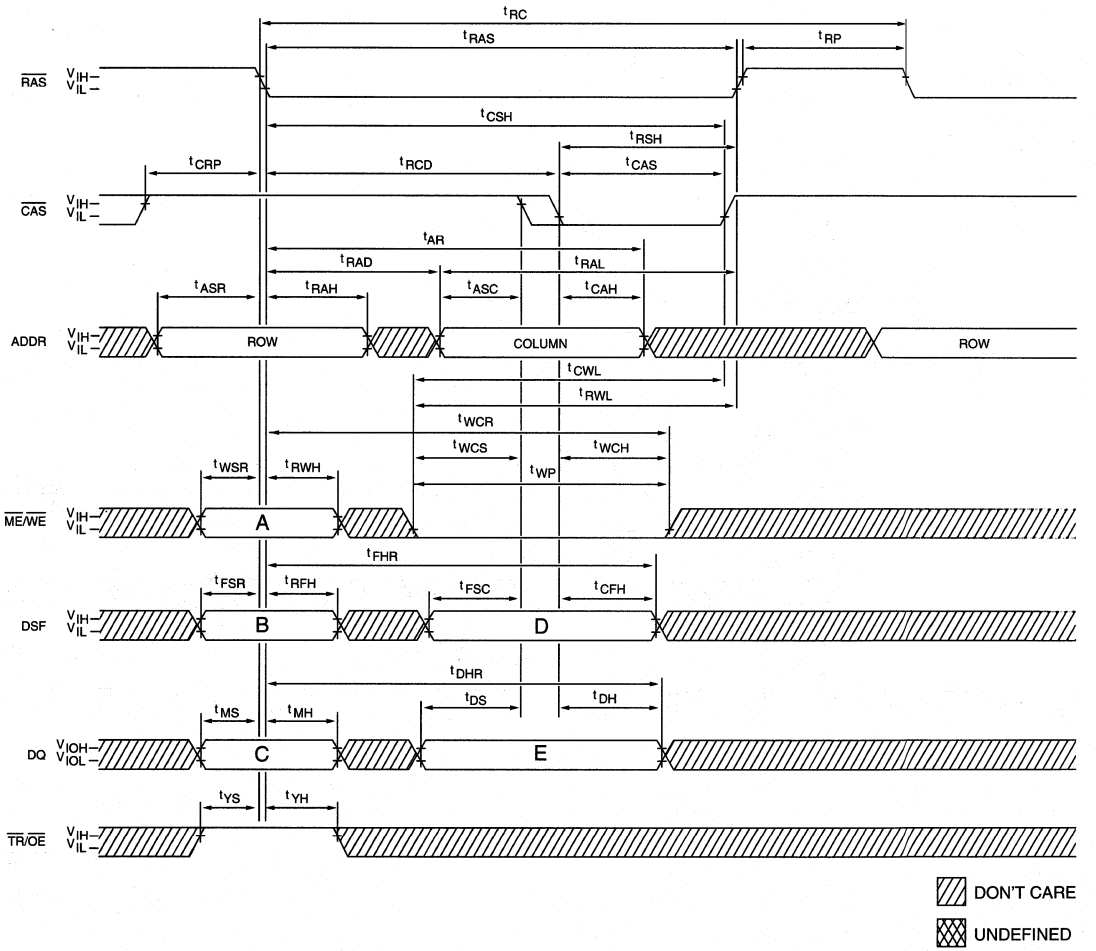
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask
Load Color Register	1	1	X	1	Color Data

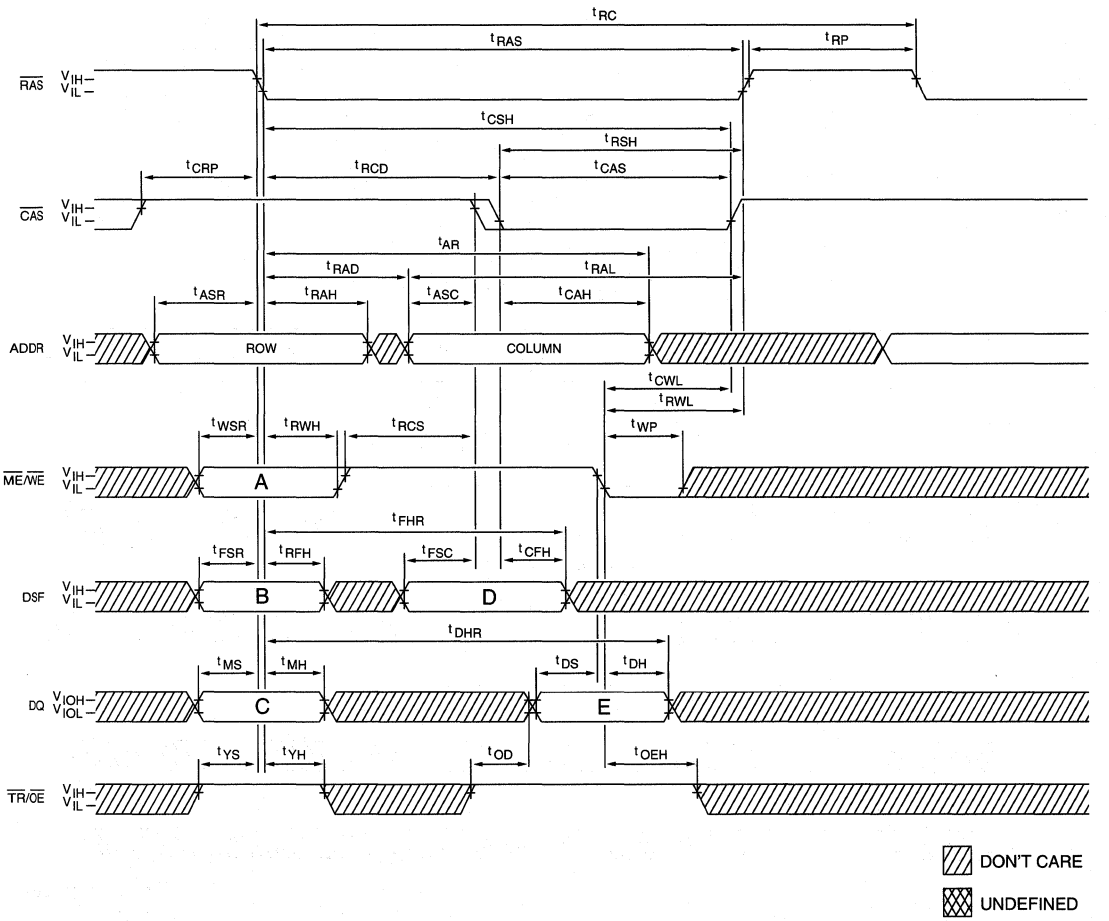
NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs later.

DRAM EARLY-WRITE CYCLE [1]



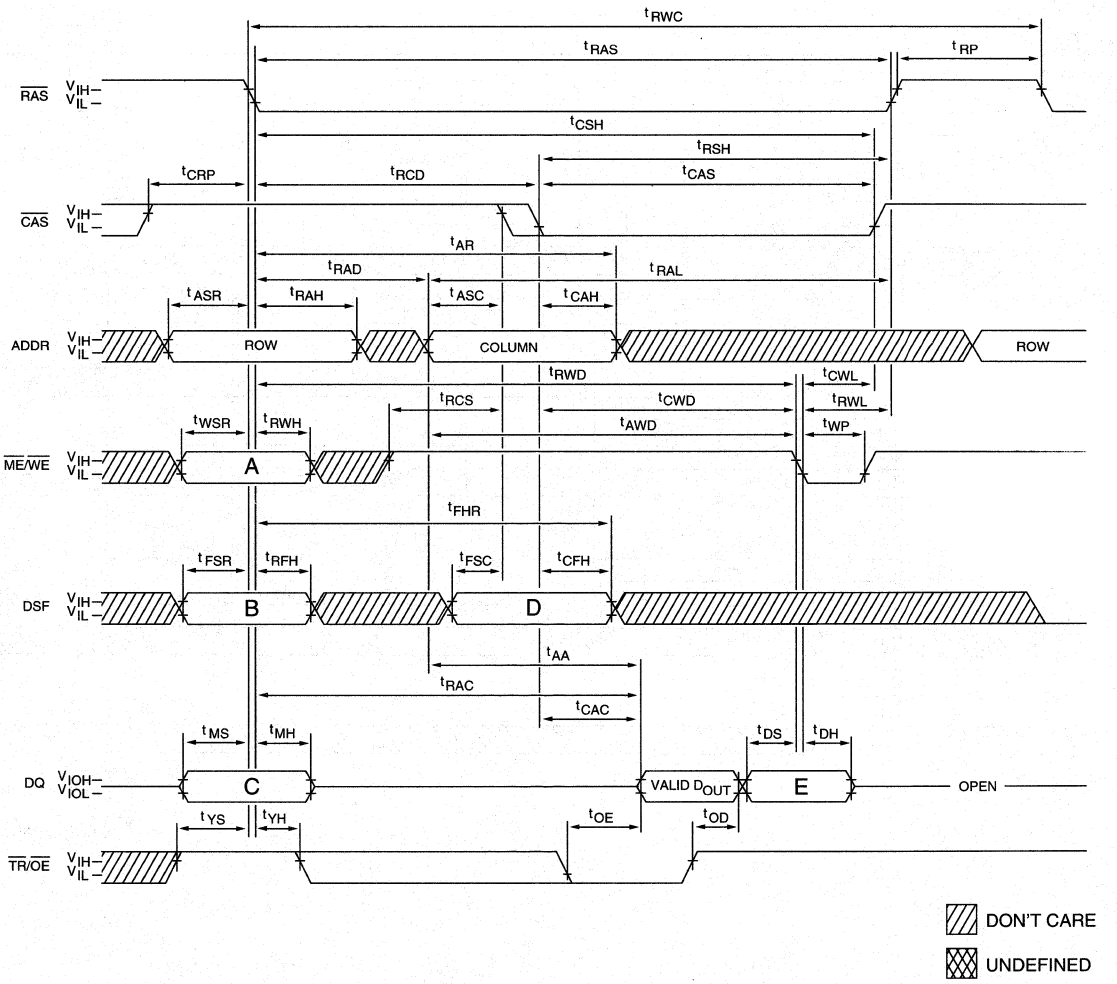
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

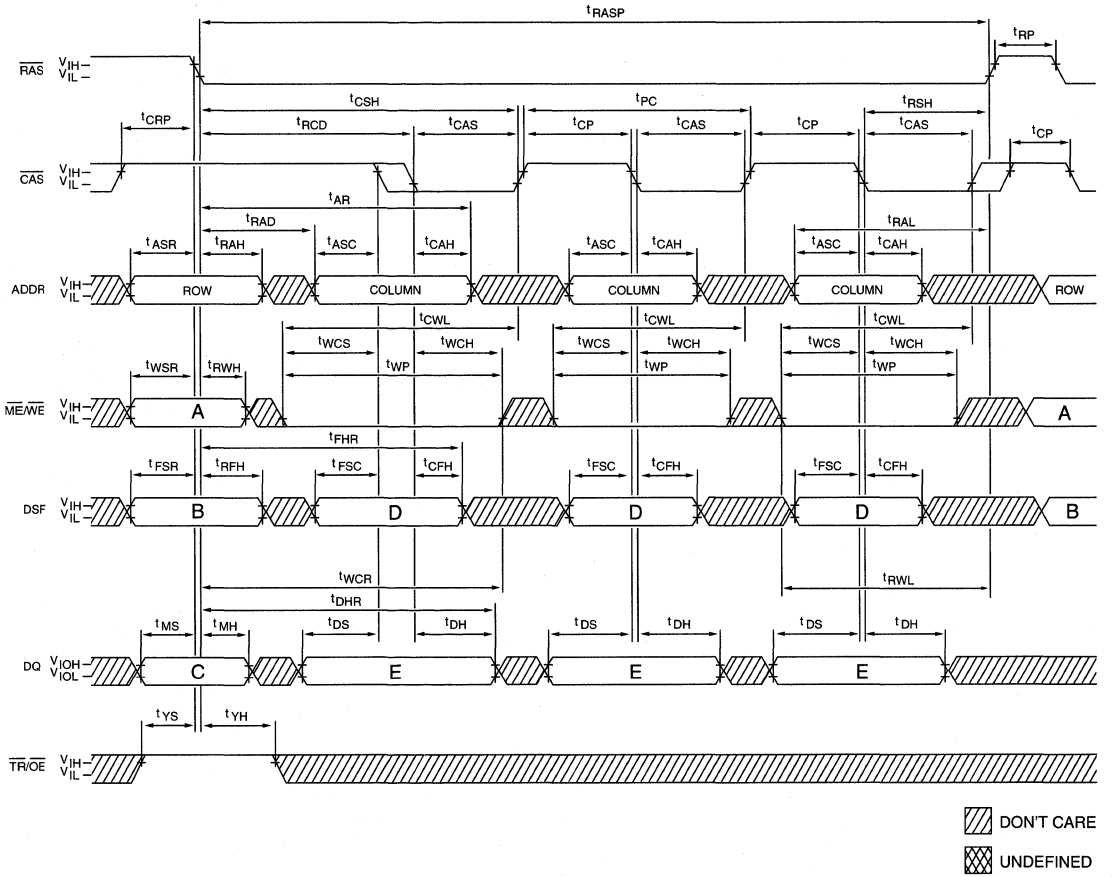
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

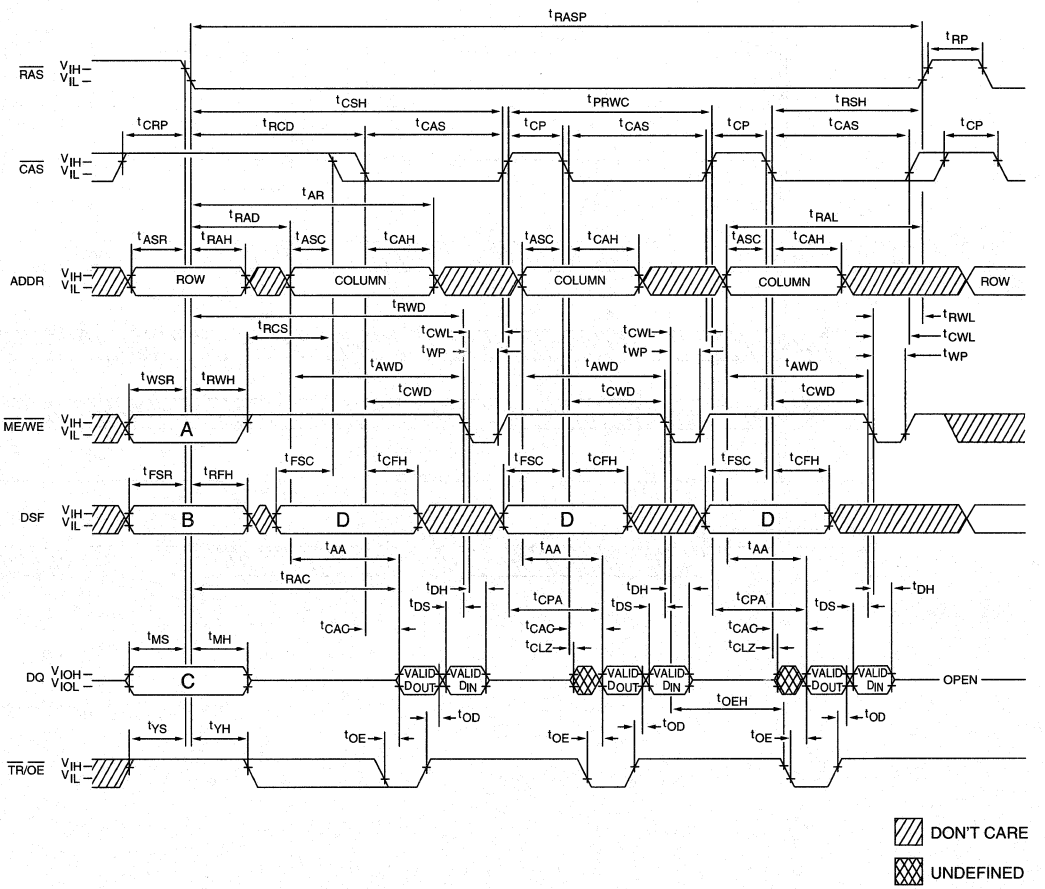
VRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



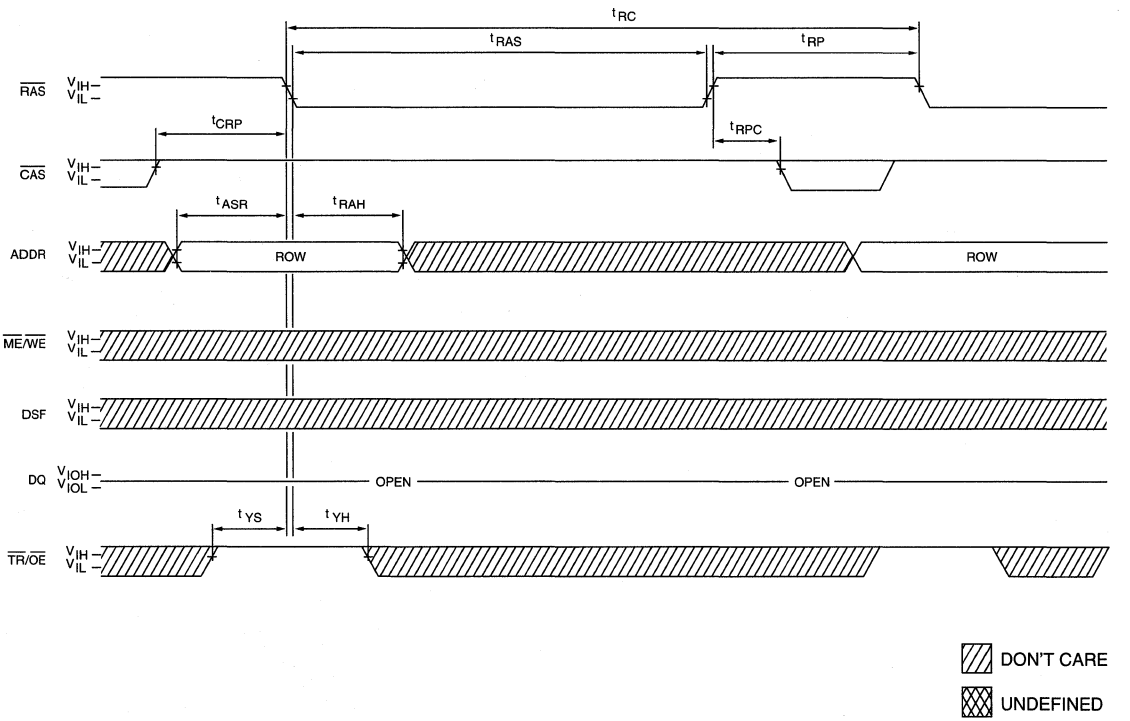
NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

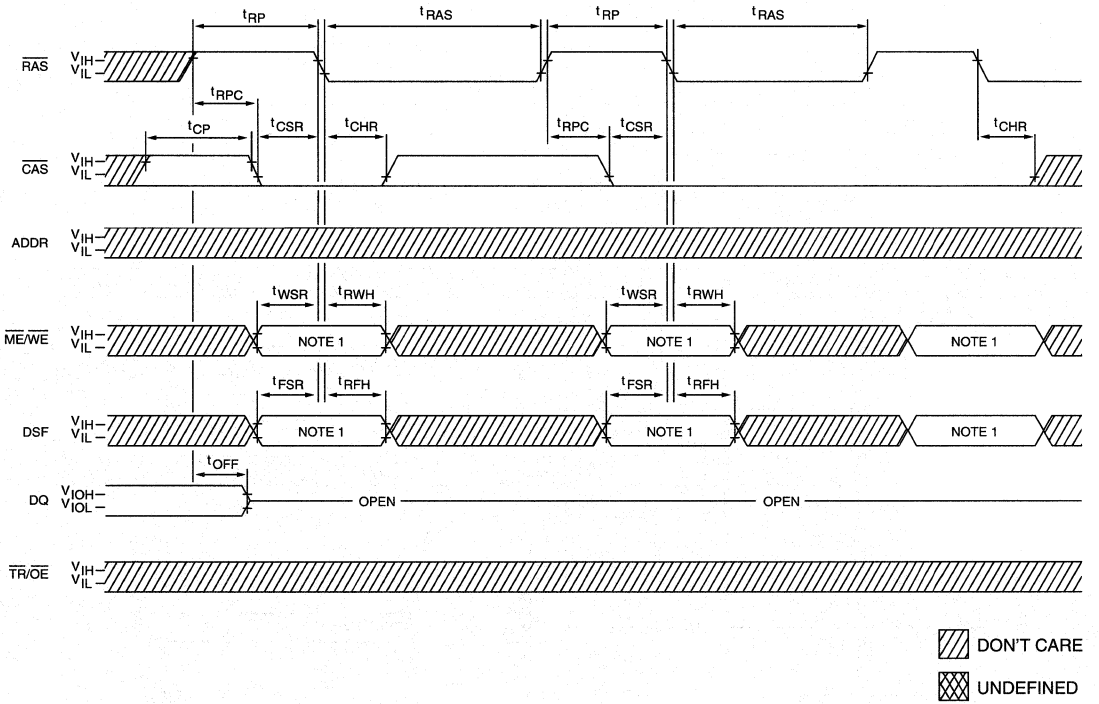


NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

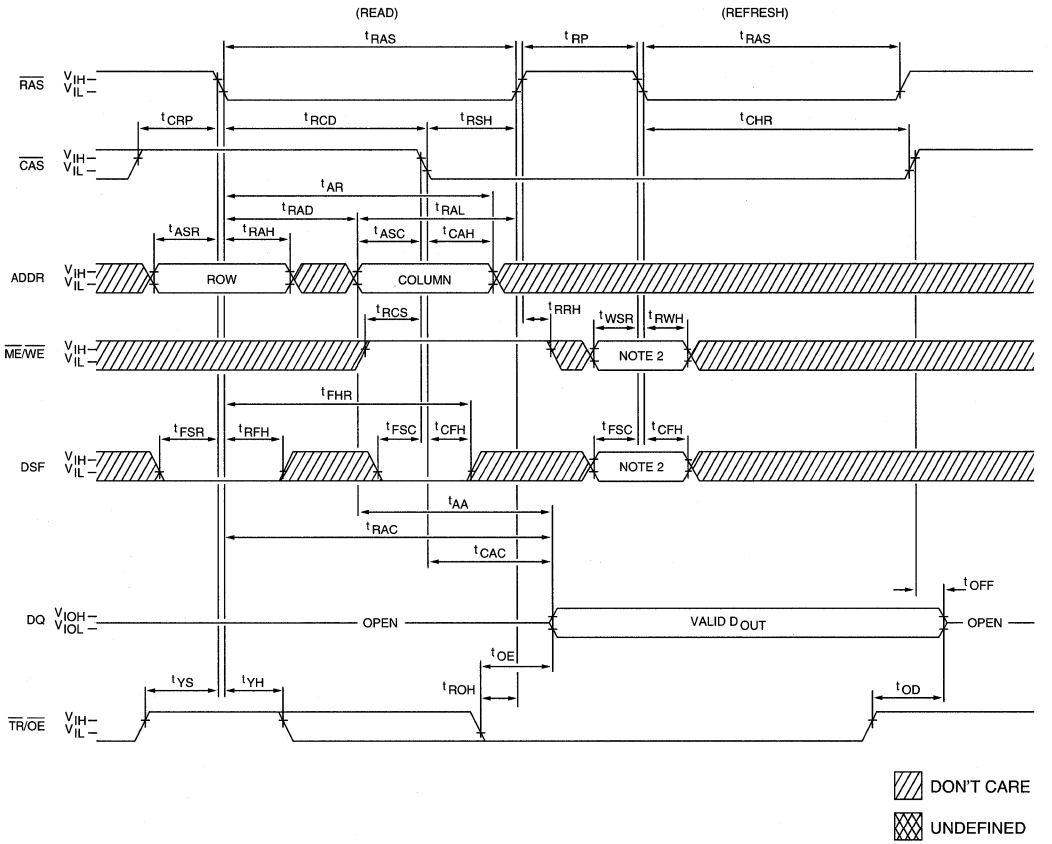


CBR REFRESH CYCLE



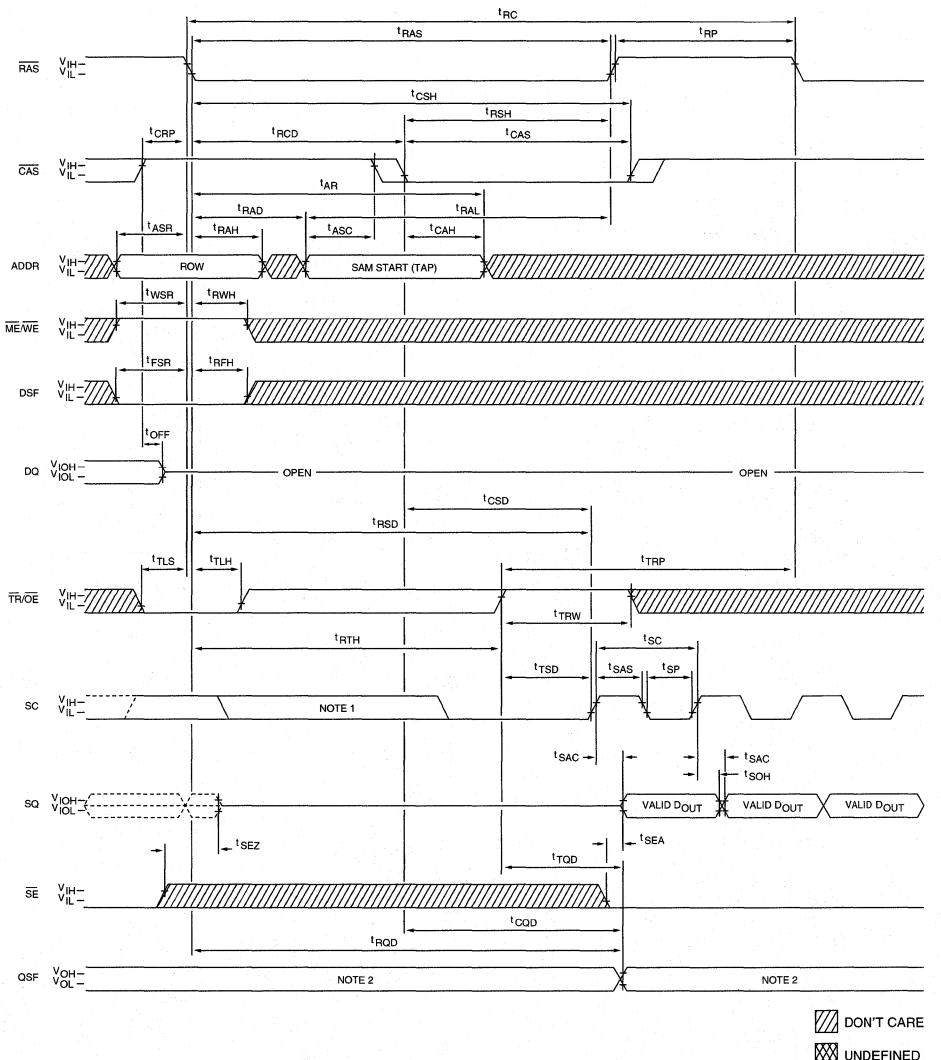
NOTE: 1. The MT42C8255 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

DRAM HIDDEN-REFRESH CYCLE



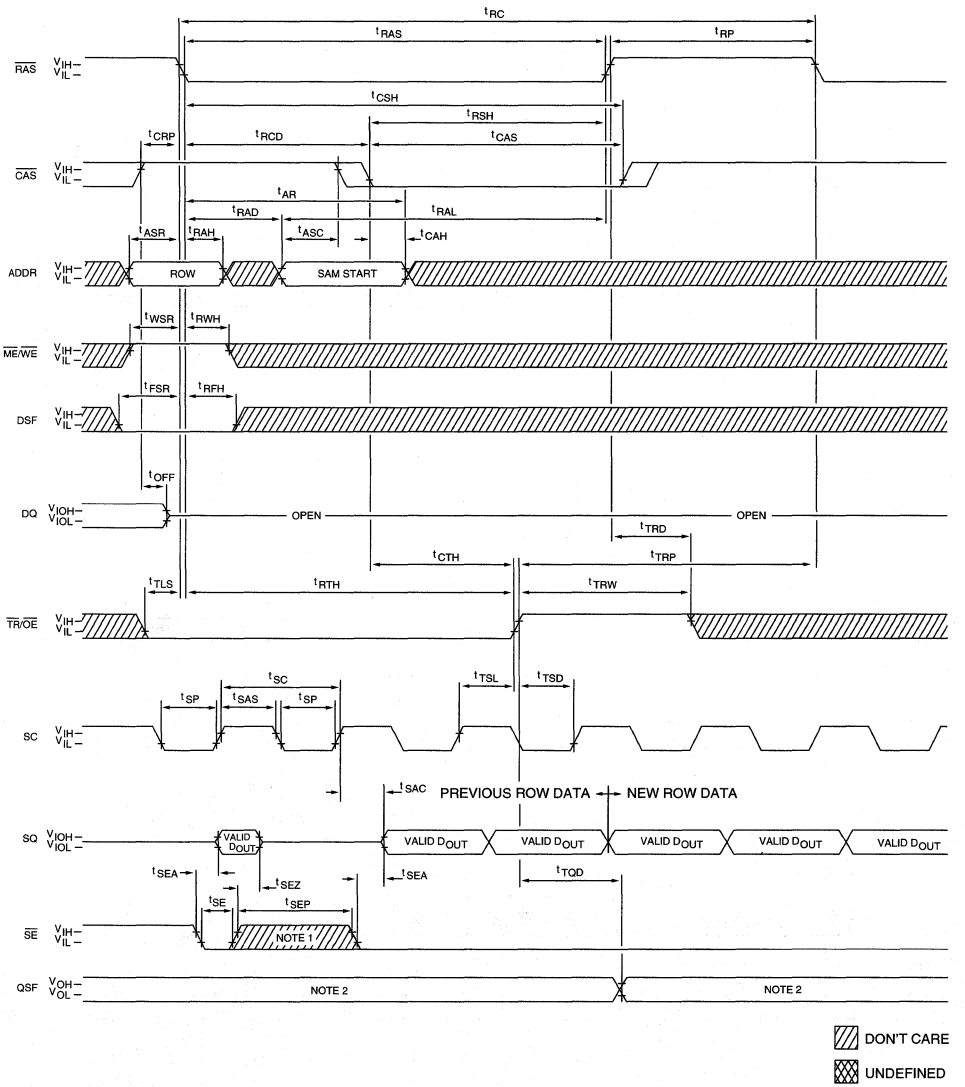
NOTE:
1. A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The MT42C8255 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When serial part was previously High-Z or SC idle)



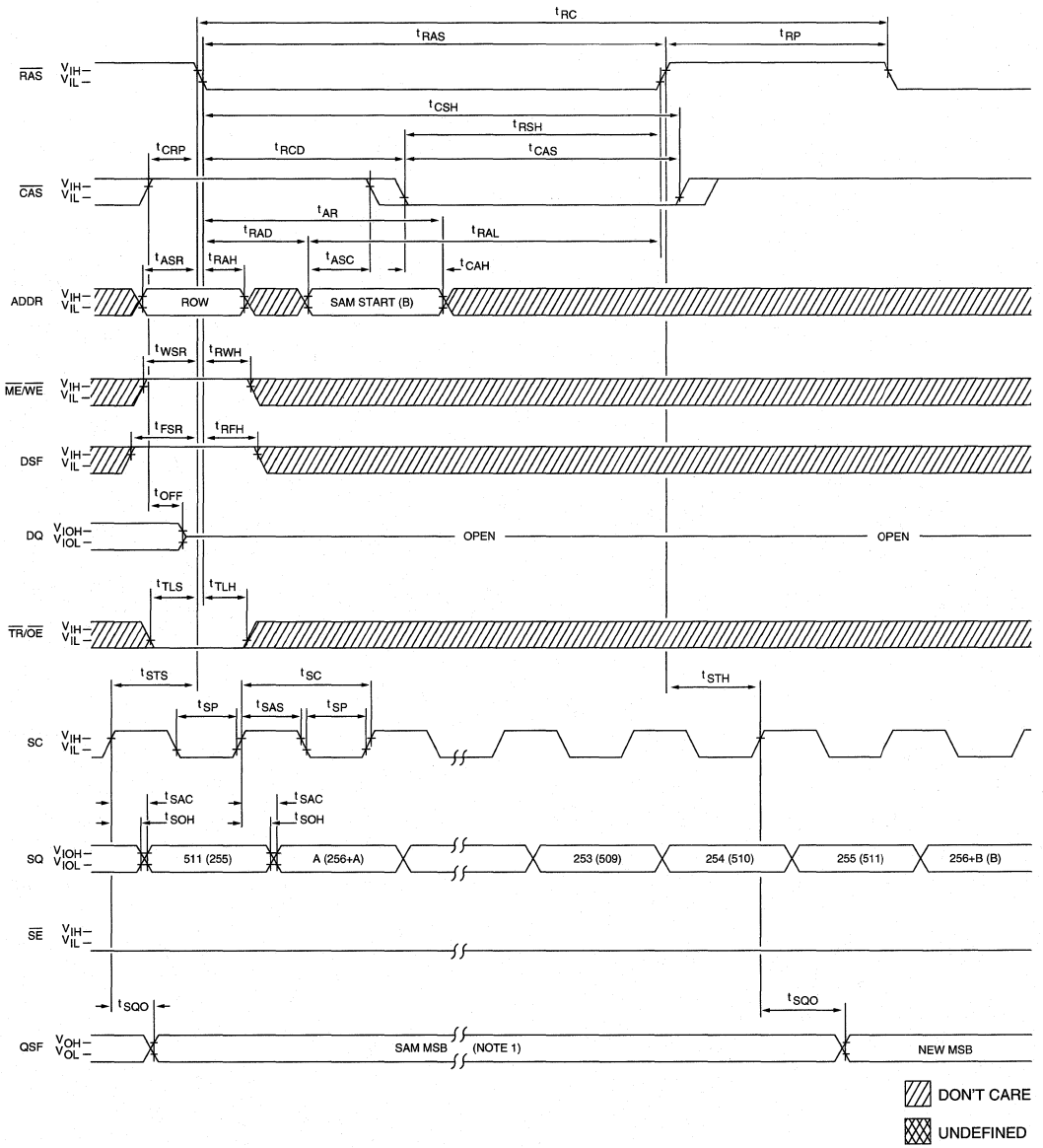
NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)



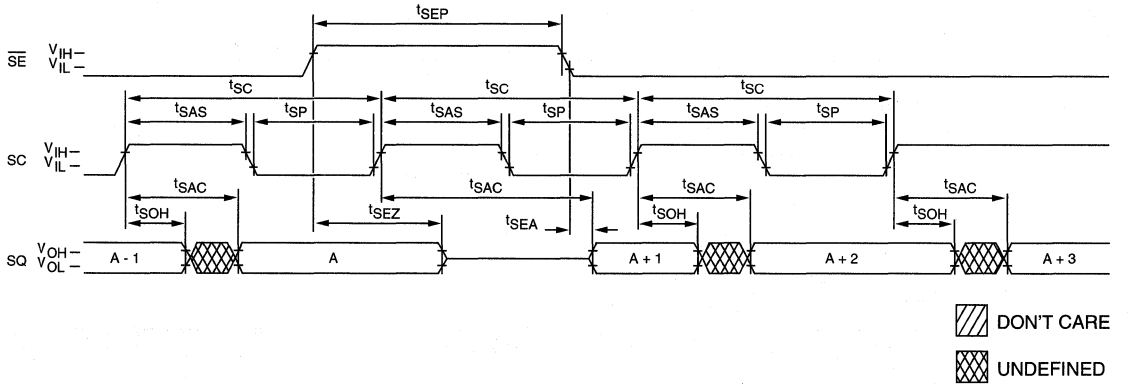
NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL OUTPUT



VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
  (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- EXTENDED-DATA-OUT FAST-PAGE-MODE access
- Dual-port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times: 70ns random, 17ns serial
  60ns random, 15ns serial†

SPECIAL FUNCTIONS

- JEDEC-Standard Mandatory Function set
- PERSISTENT MASKED WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- PROGRAMMABLE SPLIT SAM

OPTIONS — MARKING

- Timing (DRAM, SAM [cycle/access])
  - 60ns, 18/15ns — -6†
  - 70ns, 20/17ns — -7
  - 80ns, 22/20ns — -8
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG*
  - Plastic TSOP (400 mil) reverse pinout — RG*

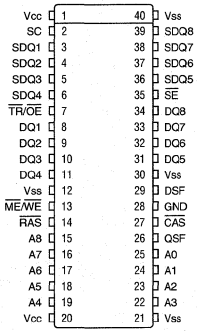
†60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

GENERAL DESCRIPTION

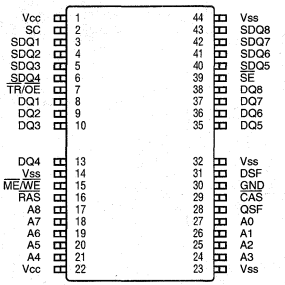
The MT42C8256 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

PIN ASSIGNMENT (Top View)

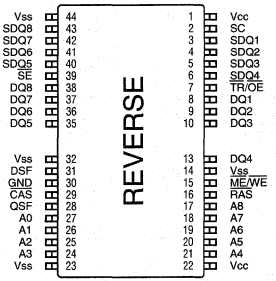
40-Pin SOJ (SDB-3)



40/44-Pin TSOP* (SDE-2)



40/44-Pin TSOP* (SDE-2)



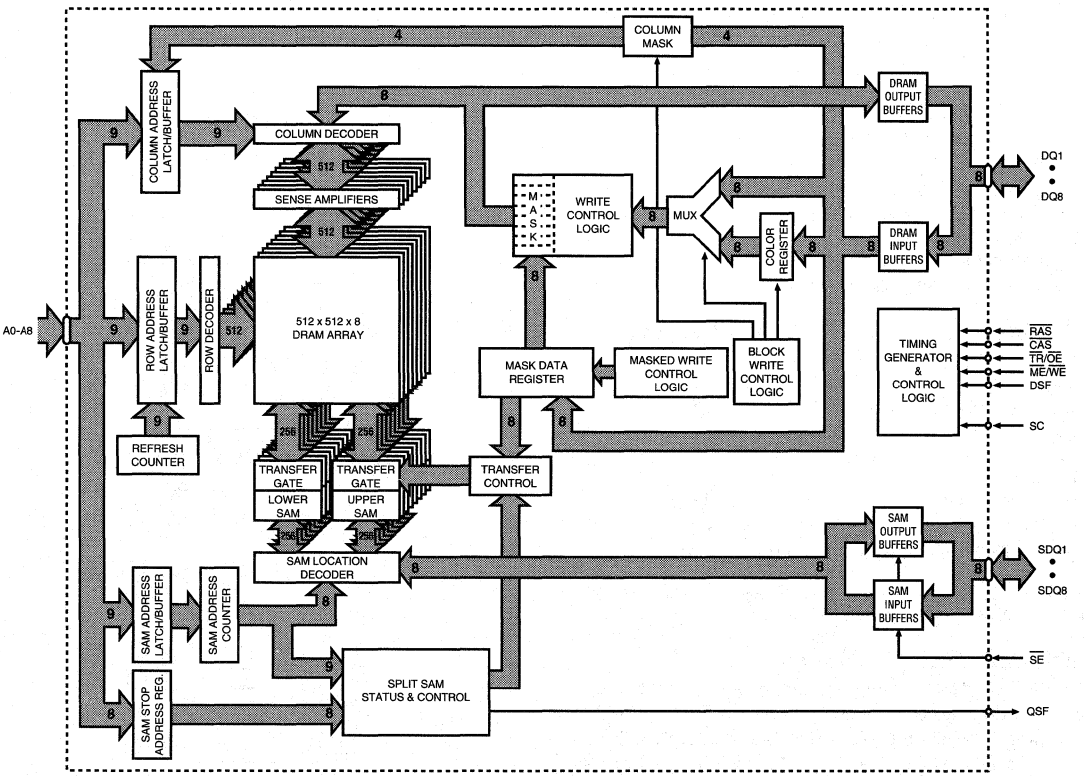
*Consult factory for availability.

The DRAM portion of the VRAM is similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 512-bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address-decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8256 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT TRANSFERs, extended data-out FAST-PAGE-MODE and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter and data latch for the SAM registers.
7	7	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, FLASH WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and strobe for $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycles.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits and as a strobe for the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT TRANSFERs.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Mask and Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	V_{CC}	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8256 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8256 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C8256 supports CBR, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and must simply perform 512 CBR cycles within the 16.7ms time period. CBR cycles are also used to reset MASKED WRITE and PROGRAMMABLE SPLIT SAM operating modes. There are three CBR cycles defined for the MT42C8256: CBR No Reset (CBRN), CBR Reset Stop Address (CBRS), and CBR Reset All Options (CBRR). To perform these functions, two additional pins are defined for CBR cycles, $\overline{ME}/\overline{WE}$ and DSF1. These operations are described in detail in the MASKED WRITE and SPLIT READ/WRITE TRANSFER sections of the functional description.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8256 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles or resets will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW and remains HIGH until $\overline{CAS}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/\overline{WE}$ performs two functions, write mask enable and data write enable. When $\overline{RAS}$ goes LOW, $\overline{ME}/(\overline{WE})$ is used to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ (with EXTENDED-DATA-OUT), FAST-PAGE-MODE WRITE (late or early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

EXTENDED DATA OUTPUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ goes HIGH, and $\overline{OE}$ is LOW (active), the output buffers will be disabled. The MT42C8256 offers an accelerated FAST PAGE MODE (FPM) cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called extended data-out, and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see DRAM READ and DRAM FAST-PAGE-MODE READ waveforms).

Extended data-out operates as any DRAM READ or FPM READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $(\overline{TR})/\overline{OE}$ are LOW. If the DQ outputs from multiple banks are wired together, $(\overline{TR})/\overline{OE}$ must be used to select and deselect the appropriate banks. During non-PAGE-MODE READ cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs later.

MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. The MT42C8256 supports two types of MASKED WRITE cycles, nonpersistent MASKED WRITE and persistent MASKED WRITE. When $\overline{ME}/(\overline{WE})$ and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8256 initializes in the nonpersistent mode. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle.

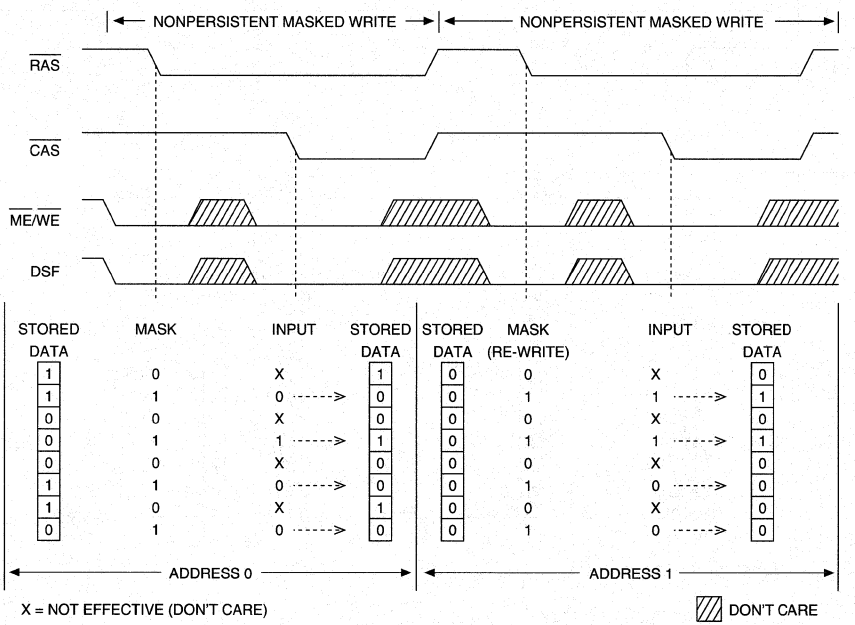


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

The selection of persistent or nonpersistent MASKED WRITE is done by performing a LOAD MASK REGISTER (LMR) cycle (see LMR description). If an LMR is done, all ensuing MASKED WRITEs are persistent and the mask data will be provided by the mask data register (see Figure 2). The mask data is applied in the same manner as in nonpersistent mode.

To reset the device back to the nonpersistent mode, a CBR RESET All Options (CBRR) cycle must be performed. This cycle is defined as a CBR with DSF LOW when $\overline{RAS}$ falls; WE is "don't care." To preserve the persistent mode of MASKED WRITE, while using CBR REFRESH, a CBRN cycle is used. This cycle will perform a refresh of the internally addressed row of DRAM but will not reset the MASKED WRITE mode.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3 and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH;

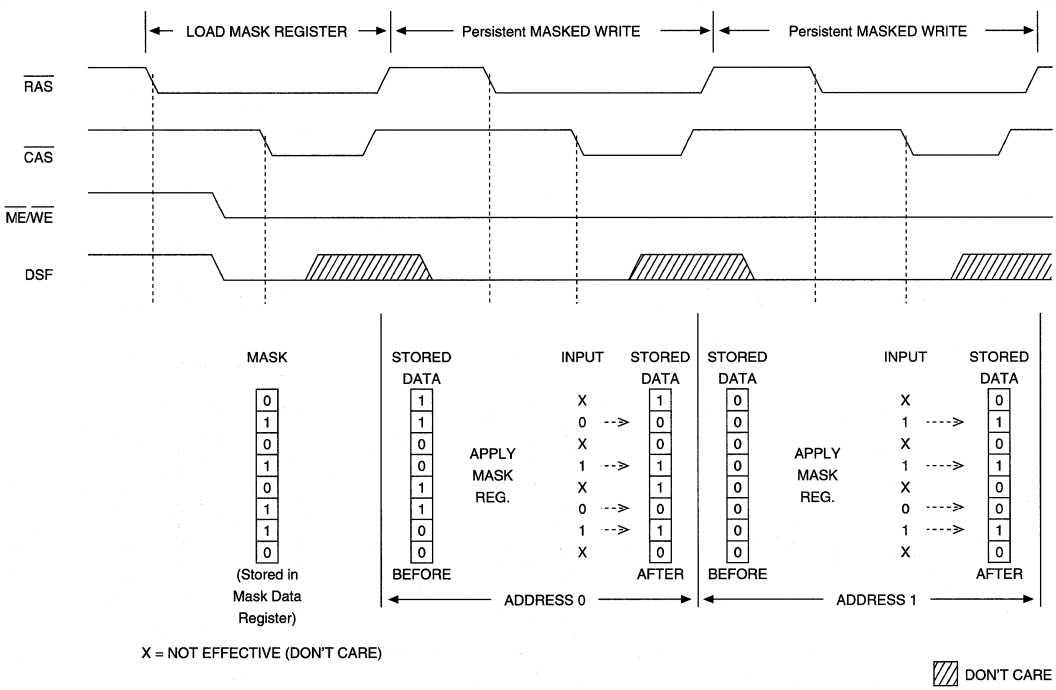


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

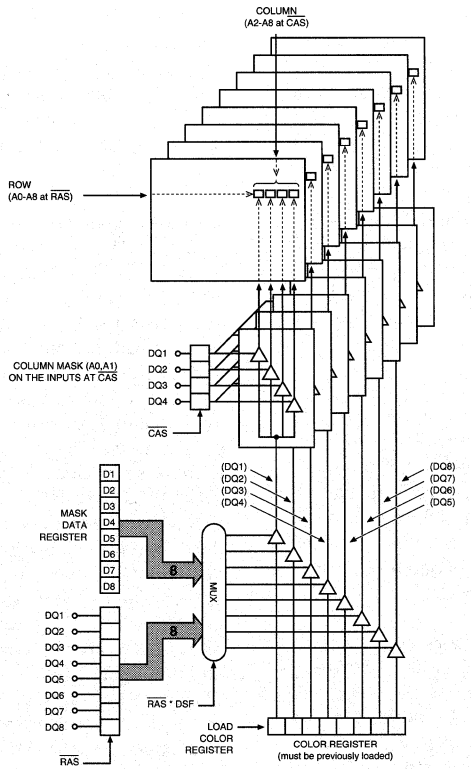


Figure 3
BLOCK WRITE EXAMPLE

a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

MASKED BLOCK WRITE

The MASKED WRITE functions may also be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BLOCK WRITE (BW), any combination of the eight bit planes may be masked, along with any combination of the four column locations.

The MASKED BLOCK WRITE will be nonpersistent (new mask) at device power-up. To enter persistent mode (old mask) a LOAD MASK REGISTER cycle is performed. All MASKED BLOCK WRITEs will be persistent after the LOAD MASK REGISTER (LMR). To reset to nonpersistent mode, a CBRR (reset all) cycle must be performed.

INPUTS	COLUMN ADDRESS CONTROLLED	
	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

MASKED FLASH WRITE

The MASKED FLASH WRITE cycle is similar to the MASKED BLOCK WRITE cycle in that it uses the color register to accelerate the writing of a select color to the DRAM memory array. Instead of writing to four adjacent column locations in one DRAM cycle (BLOCK WRITE), FWM writes the contents of the color register to all column locations on an addressed row in one cycle.

The FWM cycle is selected by taking $\overline{TR}/(\overline{OE})$ and DSF HIGH and $\overline{ME}/(\overline{WE})$ LOW at the falling edge of $\overline{RAS}$. DSF is "don't care" at the falling edge of $\overline{CAS}$. The DQ plane mask applies as it does for all masked write cycles; if the mask register has been loaded, the mask is persistent; if it has not, the mask is nonpersistent.

LOAD MASK REGISTER

The LOAD MASK REGISTER (LMR) operation loads the data present on the DQ pins into the 8-bit mask data Register at the falling edge of $\overline{CAS}$ or $(\overline{ME})/\overline{WE}$. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $(\overline{ME})/\overline{WE}$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle.

Note: *LOAD MASK REGISTER cycles also enable the persistent MASKED WRITE mode. All ensuing MASKED WRITEs (including MASKED WRITE and MASKED SPLIT WRITE TRANSFER) will be masked with data from the mask register. A CBRR has to be done to reset back to nonpersistent mode.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

During persistent operation, the mask data register contents are used for MASKED WRITE, MASKED BLOCK WRITE, MASKED FLASH WRITE, and MASKED WRITE and SPLIT WRITE TRANSFER cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER (LCR) cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE and FLASH WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER (RT) cycle is selected. The row-address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

SPLIT READ TRANSFER

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and is not synchronized with the serial clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM I/O port.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF), and to set SAM I/O direction. Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 (A8= 0, A0-A7=1) the QSF output goes HIGH and, if an SRT was done for the upper half, the new Tap address is loaded for the next half (A8 = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that Row 1 data is shifting out of the lower SAM) and execute an SRT of the upper half of Row 1 to the upper SAM. If the half-boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 5).

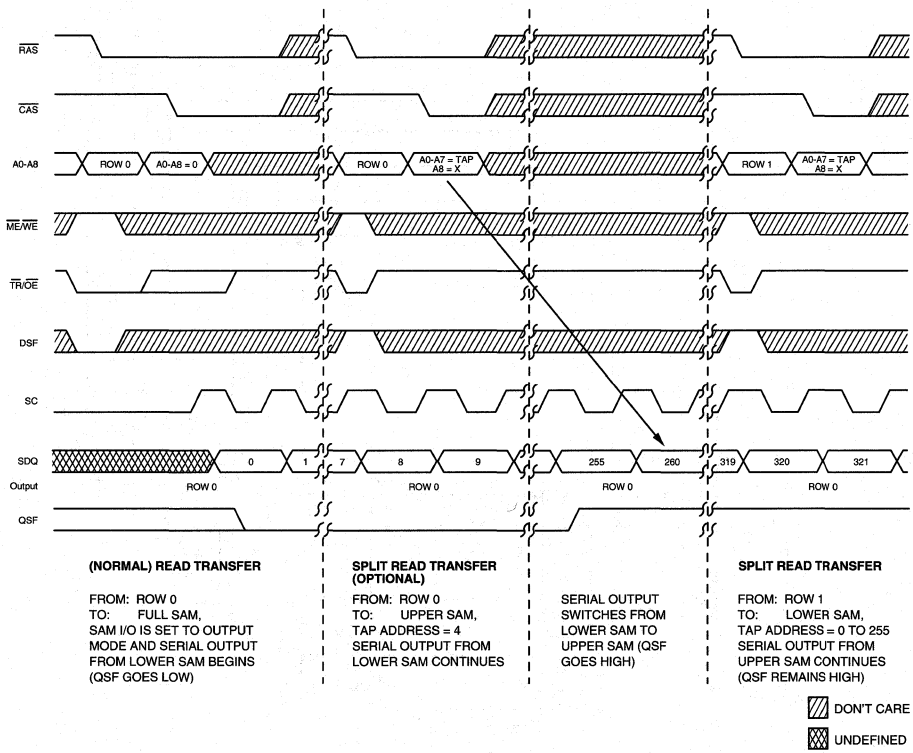


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

The stop address of the SAM half (the point at which access will change to the next half) is programmable on the MT42C8256. This function is described in the PROGRAMMABLE SPLIT SAM section of the functional description.

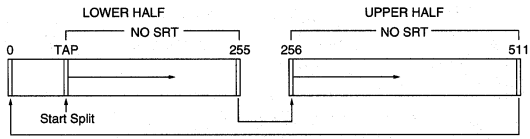


Figure 5
SPLIT SAM TRANSFER

MASKED WRITE TRANSFER

The operation of the MASKED WRITE TRANSFER (MWT) is identical to that of the READ TRANSFER described previously except ($\overline{ME}$)/$\overline{WE}$ is LOW and a DQ plane mask is applied when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A DQ mask must be applied to all MWTs as shown in Figure 6. This may be done using persistent or nonpersistent modes. When using persistent mode, the mask will be supplied by the mask register. When in nonpersistent mode, the DQ pins are used to input a bit plane mask at the falling edge of $\overline{RAS}$. An MWT changes the direction of the SAM I/O buffers to the input mode. To change the SAM I/O buffers to input mode without SAM data being transferred to the DRAM, a mask of all zeros must be presented on the DQ pins when $\overline{RAS}$ falls. QSF is LOW if serial input is to the lower half of the SAM, and HIGH if it is to the upper.

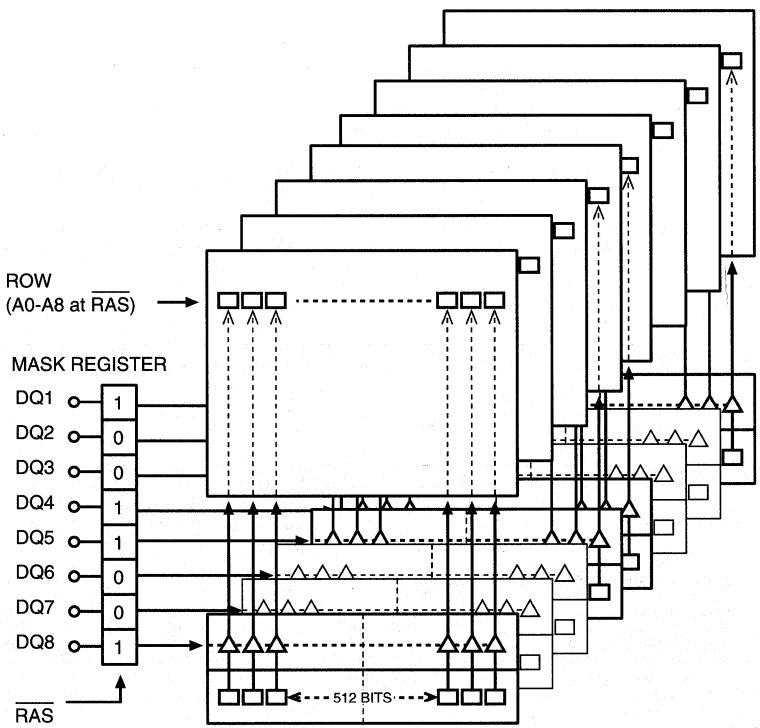


Figure 6
DQ MASKED WRITE TRANSFER

MASKED SPLIT WRITE TRANSFER

The MASKED SPLIT WRITE TRANSFER (MSWT) cycle allows serial input data to be transferred to the DRAM without interrupting the serial clock. Operation of the SWT cycle is very similar to the SPLIT READ TRANSFER cycle. It will transfer the idle half of the SAM to the DRAM and set the Tap address to where the new serial data will be loaded in that half. Selection of the MSWT cycle is the same as that of the MASKED WRITE TRANSFER with the exception of the state of DSF. When DSF is HIGH at the falling edge of $\overline{RAS}$, an MSWT will occur. The initiation sequence for MSWT is shown in Figure 7. An MSWT will not change the direction of the SAM I/O buffers.

PROGRAMMABLE SPLIT SAM

Programmable Split SAM operation is an extension of the Split SAM mode. This mode optimizes SAM performance by allowing user-programmable stop points to be defined in the split SAM. The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the loaded Tap address). The locations of the stop points are programmable in power-of-two increments. The stop points and size of the resulting partitions are shown in Figure 8, along with an example.

The stop points are set by performing a CBR RESET STOP (CBRS) address cycle. A CBRS cycle is a CBR with $\overline{ME}/\overline{WE}$ LOW and DSF HIGH at the $\overline{RAS}$ HIGH-to-LOW transition.

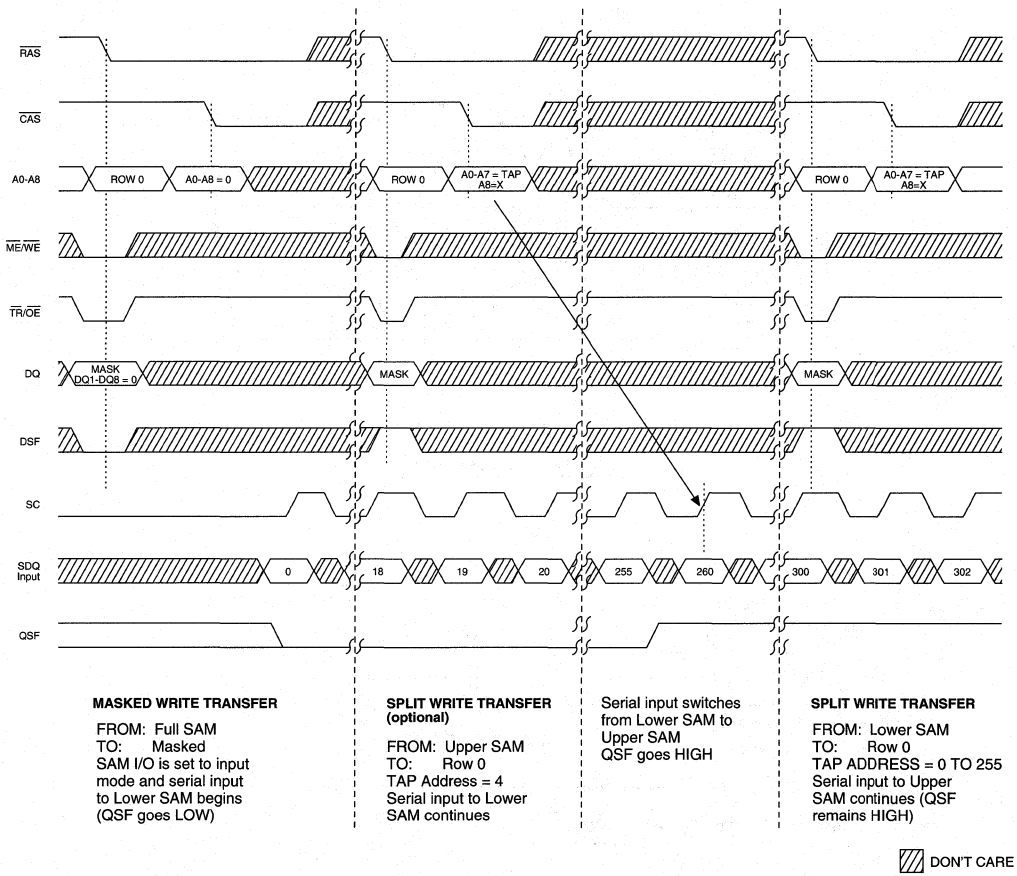


Figure 7
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

This is a special CBR refresh cycle that, in addition to refreshing the DRAM, will sample the address pins (A4-A8) and set the stop point partition to the addressed value (See Figure 8). The programmable stop points will not become valid until a Split Transfer (READ or WRITE) is done, following the CBRS. Both halves of the SAM will be programmed simultaneously to the same partition lengths and stop points.

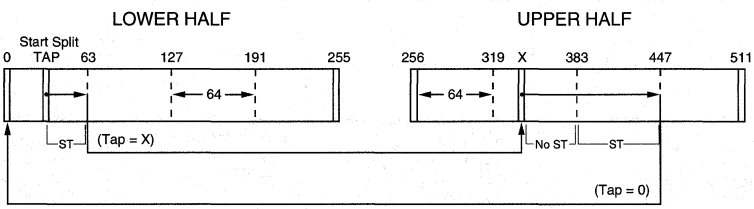
Access will progress from the Tap address to the end of the programmable partition into which the Tap fell. When the end of the "addressed" partition is reached, the access will jump to the tap address of the next half, provided that a SPLIT TRANSFER (READ or WRITE) was done before the partition boundary was reached. If a SPLIT TRANSFER (ST) is not done prior to the terminal count of the partition, the partition is not recognized and the address count will continue in the same half (this is shown Figure 8 at stop address 383). The count will continue in the same half until a SPLIT TRANSFER (READ or WRITE) occurs or the SAM half boundary is reached. In Figure 8, an ST occurs some time between addresses 383 and 447 and the boundary is recognized at 447. The programmable stop points may be reprogrammed at any time by performing another CBRS cycle, the new stop points will not be valid until an ST is performed.

Disabling the programmable split SAM requires a CBRR. This is as CBR cycle with DSF LOW at the $\overline{RAS}$ HIGH-to-LOW transition. The CBRR will take effect immediately; it does not require an ST to become active valid.

Number Stop Points/Half	Address @ $\overline{RAS}$ LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

EXAMPLE
(four stop points)



Programmed Partition (A4-A8) = 000111111
MSB....LSB

Figure 8
PROGRAMMABLE SPLIT SAM OPERATION

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the SERIAL INPUT/OUTPUT buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address zero if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the SERIAL INPUT mode. As in the serial output operation, the contents of the SAM address counter (loaded when the SERIAL INPUT mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for SERIAL INPUT data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP and INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data, and the nonpersistent MASKED WRITE mode is enabled.

The SAM portion of the MT42C8256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the SERIAL INPUT mode (MASKED WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The mask and color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS											
CBRR	CBR REFRESH (RESET ALL OPTIONS)	0	X	X	0	—	X	X	—	X	X	X
CBRS	CBR REFRESH (RESET STOP ADDRESS)	0	X	0	1	—	STOP[7]	X	—	X	X	X
CBRN	CBR REFRESH (NO RESET)	0	X	1	1	—	X	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X	X
RWM	MASKED WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK[4]	VALID DATA	USE[4]	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWM	MASKED BLOCK WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK[4]	COLUMN MASK	USE[4]	USE
FWM	MASKED FLASH WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	1	X	ROW	X	WRITE MASK[4]	X	USE[4]	USE
	REGISTER OPERATIONS											
LMR	LOAD MASK REGISTER	1	1	1	1	0	ROW[5]	X	X	REG DATA	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[5]	X	X	REG DATA	X	LOAD
	TRANSFER OPERATIONS											
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[6]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[6]	X	X	X	X
MWT	MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	0	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X
MSWT	MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NEW OR OLD MASK)	1	0	0	1	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is last. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is last.
4. After an LMR cycle, all masked WRITEs use the mask register (old mask). Data on the DQs at RAS falling edge will be ignored. A CBRR will reset to new mask state and mask data must be presented on the DQs at every RAS falling edge.
5. The ROW that is addressed will be refreshed, but a ROW address is not required.
6. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half or programmable stop address boundary).
7. Defines the column addresses where access moves to the next half; see Programmable Split SAM functional description.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	1
Output Low Voltage (IOUT = 2.5mA)	VOL		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SC, $\overline{SE}$, DSF	CI2		8	pF	2
Input/Output Capacitance: DQ, SDQ	CI/O		9	pF	2
Output Capacitance: QSF	CO		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	165	155	145	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC2}	110	100	90	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	165	155	145	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	165	155	145	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	185	175	165	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6*	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	215	205	190	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC8}	160	150	135	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC9}	50	50	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	215	205	190	mA	3, 4, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	215	205	190	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	220	210	195	mA	3, 4

*60ns (-6) specifications are preliminary and are specified for V_{CC} = 5V ±5%. Please consult factory for availability.

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	148		170		190		ns	
FAST-PAGE-MODE READ or EARLY WRITE cycle time (Extended Data Out (READ))	tPC	24		27		30		ns	
FAST-PAGE-MODE LATE WRITE, MASKED WRITE or BLOCK WRITE cycle time.	tPC	30		35		40		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	83		90		95		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	15, 28
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width (FAST-PAGE-MODE READ or EARLY WRITE cycles only)	tCAS	10	100,000	10	100,000	12	100,000	ns	
$\overline{CAS}$ pulse width (All other cycles)	tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	12		12		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
$\overline{CAS}$ HIGH to $\overline{RAS}$ HIGH lead time	tCRL	0		0		0		ns	
$\overline{RAS}$ HIGH to $\overline{CAS}$ HIGH lead time	tRCL	0		0		0		ns	
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	tOFF	3	20	3	20	3	20	ns	20, 23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	tOD	3	10	3	10	3	10	ns	20, 23
Output enable delay from ($\overline{TR}$)/$\overline{OE}$	tOELZ	3		3		3		ns	
Output disable delay from ($\overline{ME}$)/$\overline{WE}$	tWHZ	3	10	3	10	3	10	ns	
Output disable hold time from start of WRITE	tOEH	10		10		10		ns	27
Output Enable to $\overline{RAS}$ delay	tORD	0		0		0		ns	
Data output hold after $\overline{CAS}$ LOW	tCOH	5		5		5		ns	28

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	12		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	18		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	18		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	12		12		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	50		55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		40		ns	21
Transition time (rise or fall)	^tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	tRTH	60	10,000	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	tCTH	15		20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	50		50		50		ns	
$\overline{TR}/(\overline{OE})$ precharge time	tTRW	15		20		25		ns	
$\overline{TR}/(\overline{OE})$ LOW to last SC hold time	tTSL	5		5		5		ns	11
$\overline{TR}/(\overline{OE})$ HIGH to first SC setup time	tTSD	50		50		50		ns	11
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	tSZS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	15		15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	15		15		15		ns	
SC to QSF delay time	tSQD		20		25		30	ns	
SPLIT TRANSFER setup time	tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	tSTH	10		10		10		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	tFHR	45		55		60		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	15		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		30		30		30	ns	
$\overline{RAS}$ to QSF delay time	tRQD		70		75		75	ns	
$\overline{CAS}$ to QSF delay time	tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	tRSD	95		105		115		ns	
$\overline{CAS}$ to first SC delay	tCSD	50		55		55		ns	

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

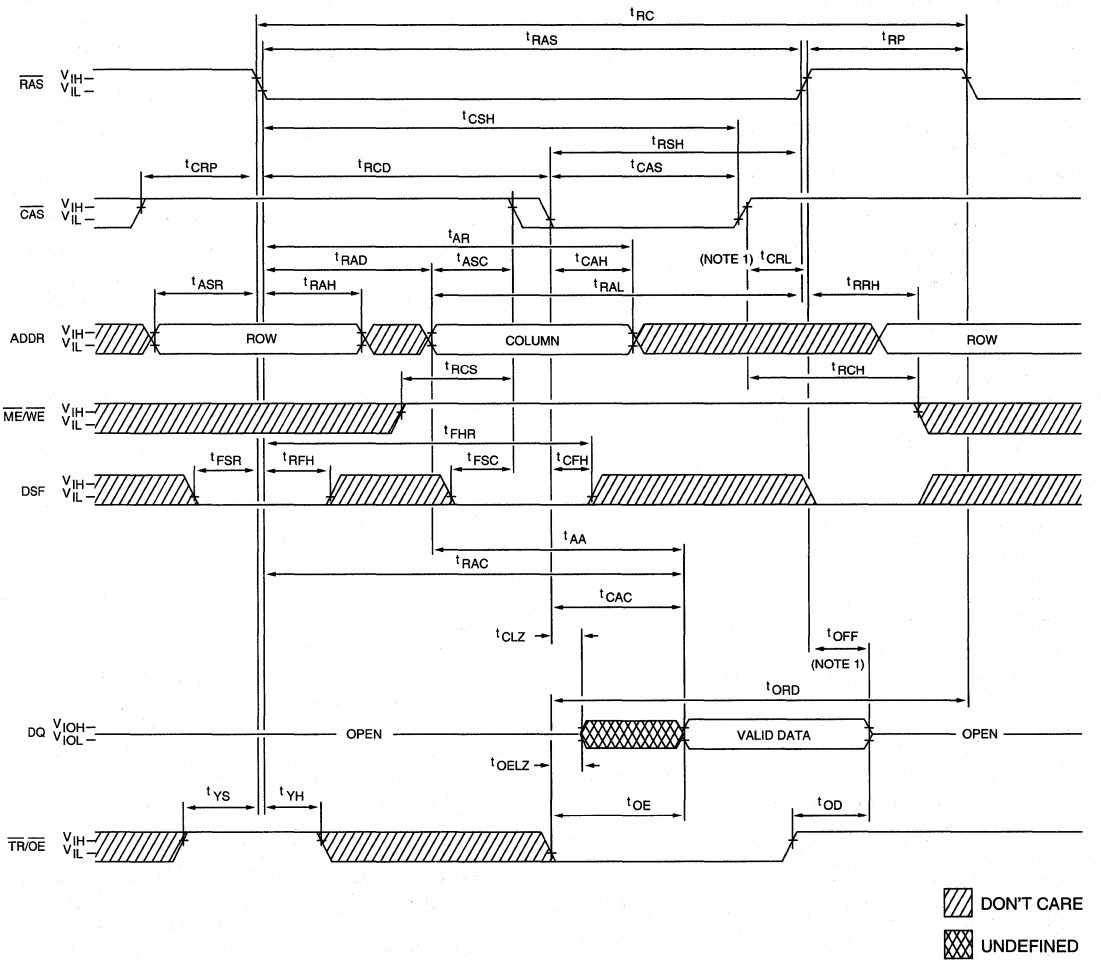
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	18		20		22		ns	
Access time from SC	^tSAC		15		17		20	ns	24, 28
SC precharge time (SC LOW time)	^tSP	7		8		9		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		9		ns	
Access time from $\overline{SE}$	^tSEA		12		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		9		ns	
Serial data-out hold time after SC high	^tSOH	3		3		3		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial output buffer turn-on delay from $\overline{SE}$	^tSOO	3		3		3		ns	
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

NOTES

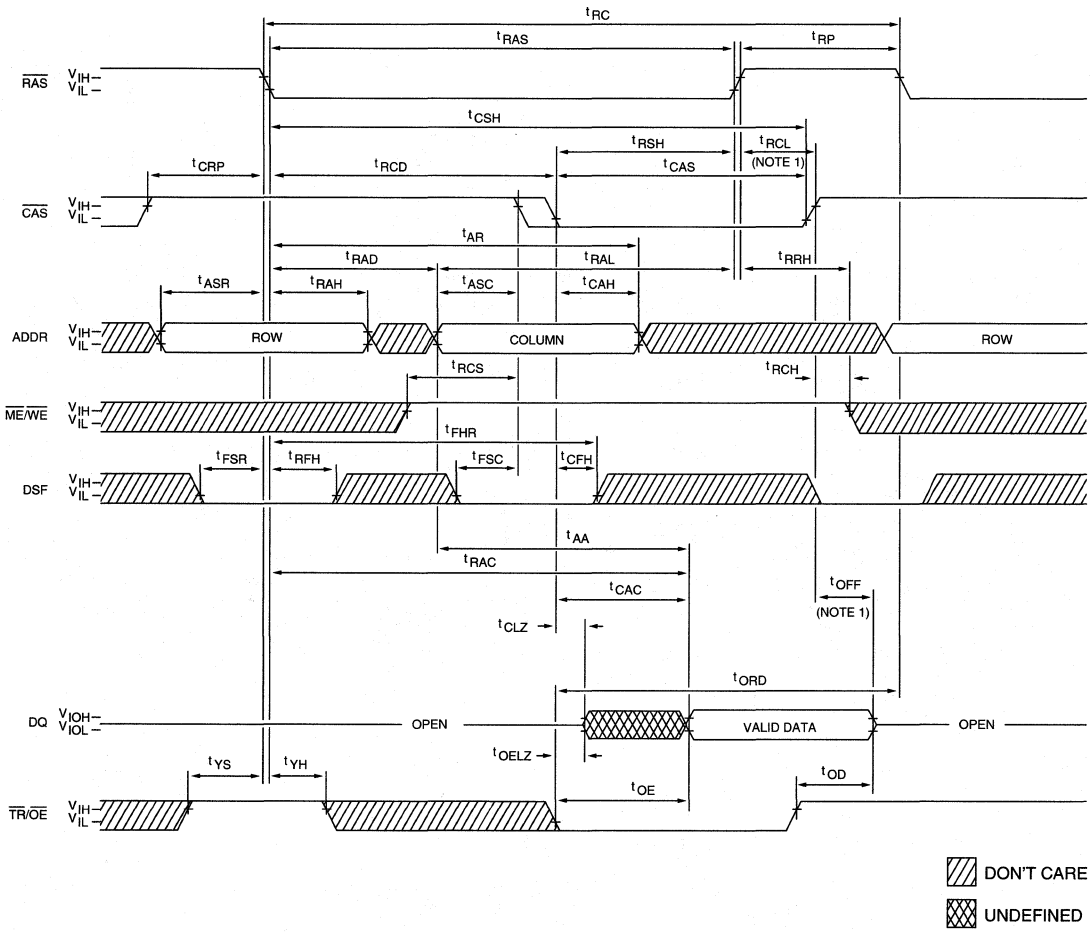
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. The "last" SC edge causes the last data from the previous row to appear on the SDQ pins. The "first" SC causes the first data from the new row to appear.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to one TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OD, ^{t}OFF and ^{t}SEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^{t}WCS ≤ ^{t}WCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until ^{t}OD is met) is indeterminate, but the WRITE will be valid if ^{t}OD and ^{t}OEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ HIGH or when $\overline{RAS}$ and $\overline{CAS}$ go HIGH, whichever occurs first.
24. SAM output timing is measured with a load equivalent to one TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^{t}OEH is met. If $\overline{CAS}$ and $\overline{RAS}$ go HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^{t}SAC/^{t}CAC are MAX at 70° C and 4.5V Vcc; ^{t}SOH/^{t}COH are MIN at 0° C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. This is guaranteed by design (^{t}SOH = ^{t}SAC - output transition time; ^{t}COH = ^{t}CAC - output transition time).

DRAM READ CYCLE [1]
(Outputs controlled by $\overline{RAS}$)



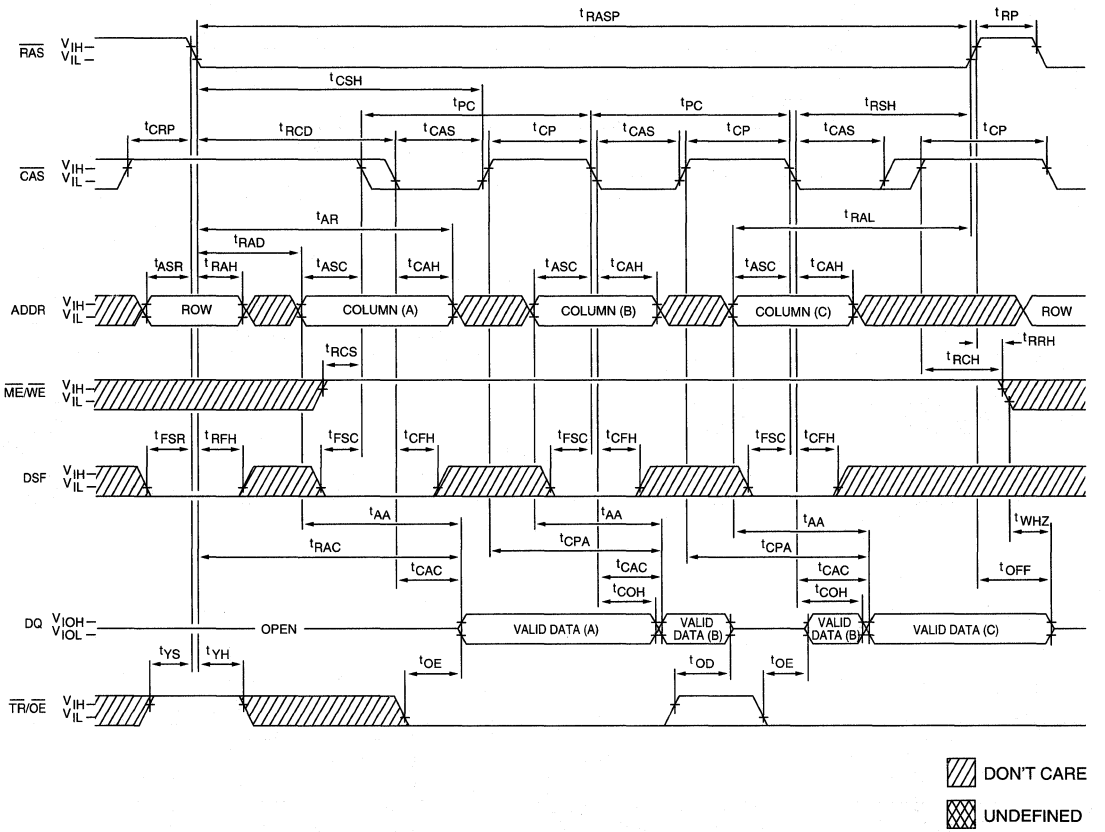
NOTE: 1. tCRL is a reference parameter. If $\overline{CAS}$ = HIGH tCRL before $\overline{RAS}$, tOFF is referenced from the rising edge of $\overline{RAS}$.

DRAM READ CYCLE [1]
(Outputs controlled by $\overline{CAS}$)



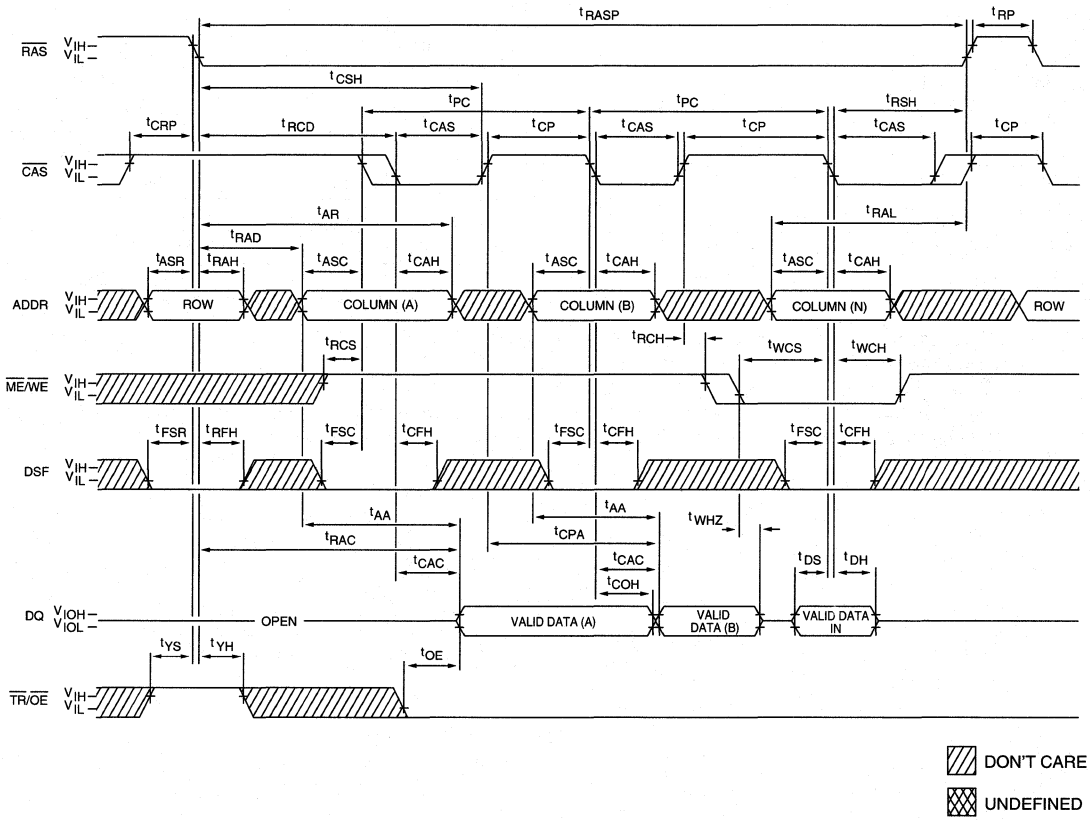
NOTE: 1. ^{t}RCL is a reference parameter. If $\overline{RAS}$ = HIGH ^{t}RCL before $\overline{CAS}$, ^{t}OFF is referenced from the rising edge of $\overline{CAS}$.

DRAM FAST-PAGE-MODE READ CYCLE
(Extended Data-Out)



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

DRAM FAST-PAGE-MODE READ/WRITE CYCLE
(Extended Data-Out)

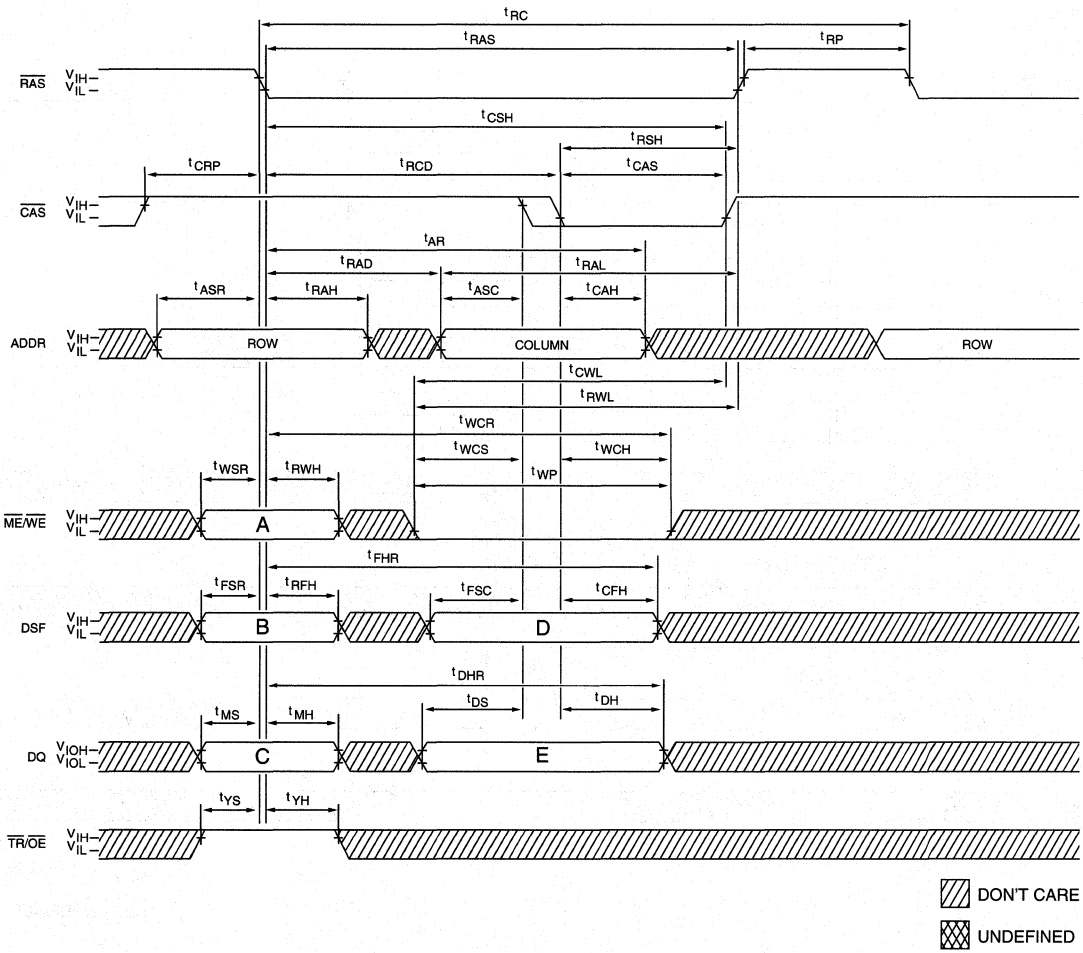


WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask[3]	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask[3]	1	Column Mask
MASKED FLASH WRITE to DRAM	0	1	Write Mask[3]	X	X
Load Mask Data Register	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

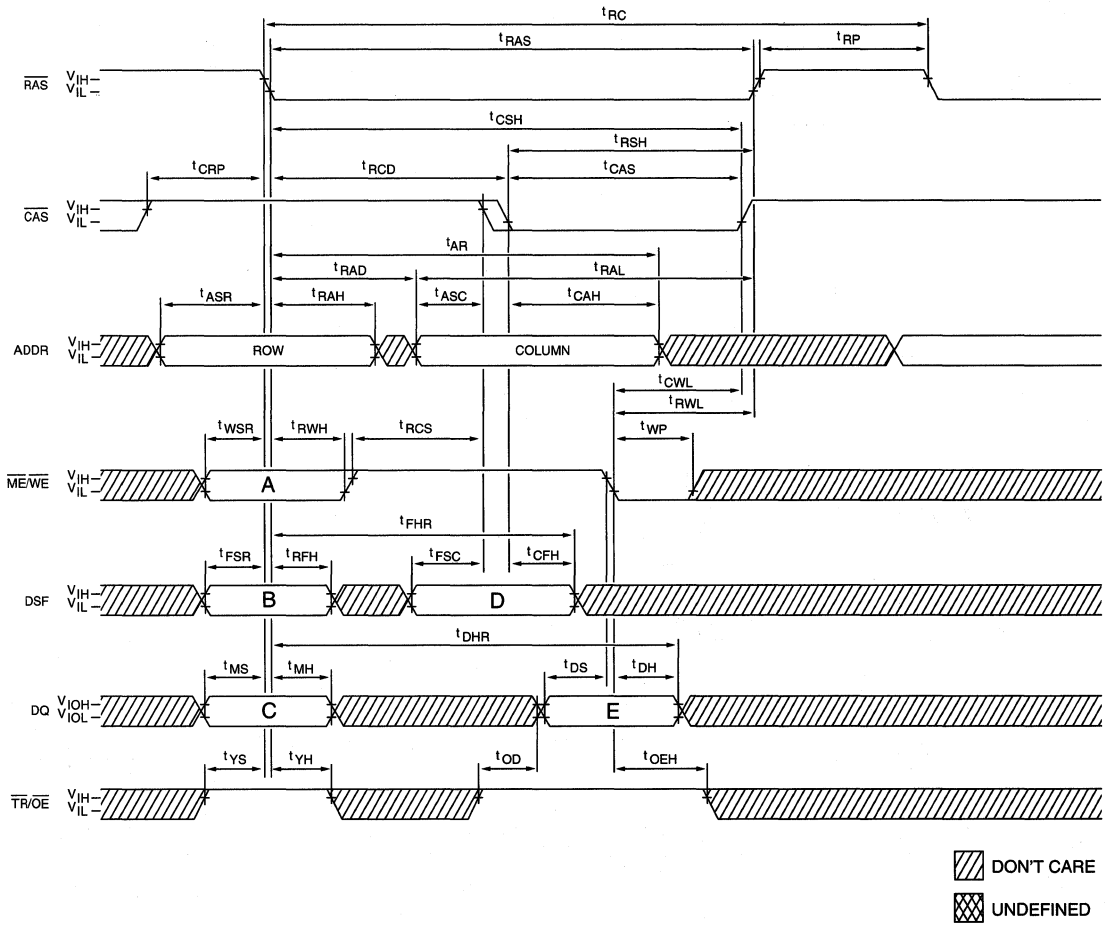
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs last.
3. Mask Data is loaded at $\overline{RAS}$ falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the Mask Data Register and the DQs are "don't care" at the $\overline{RAS}$ falling edge.

DRAM EARLY-WRITE CYCLE [1]



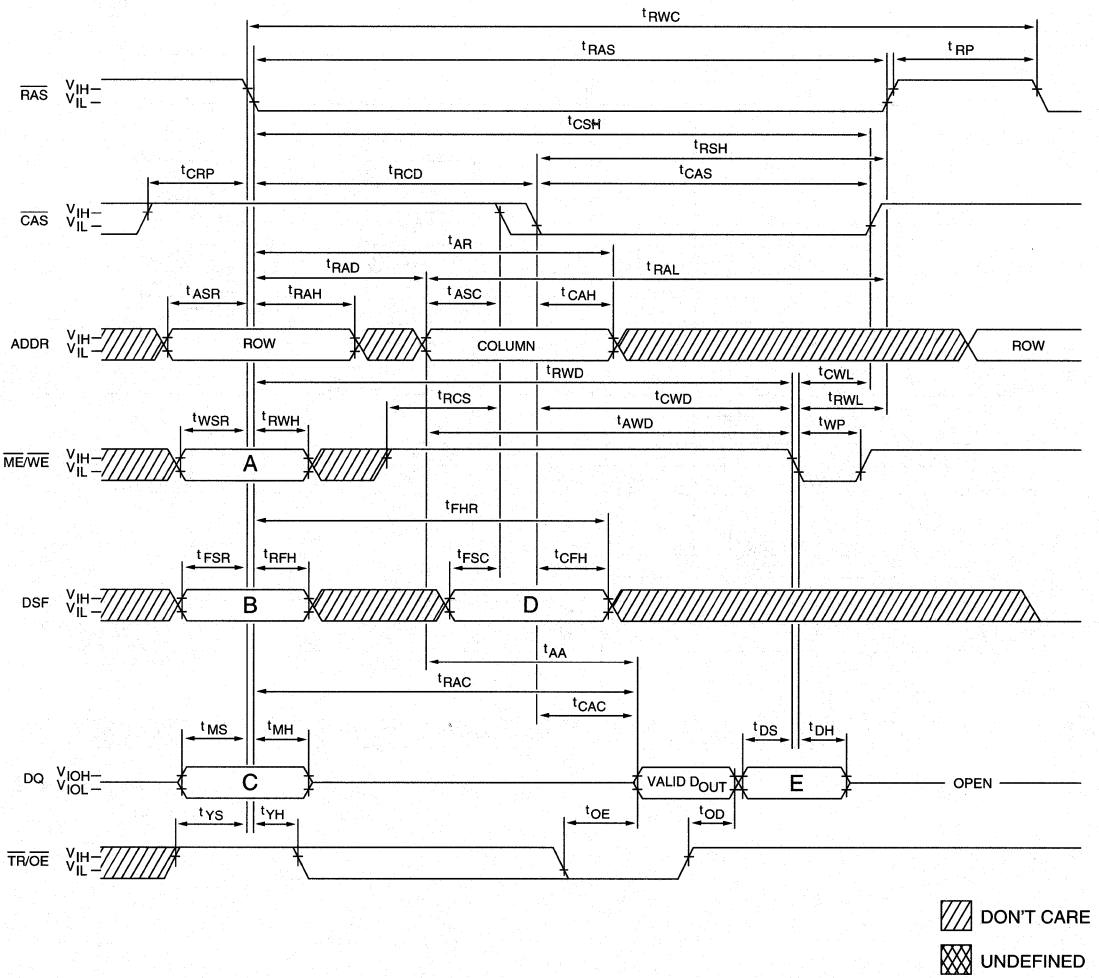
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



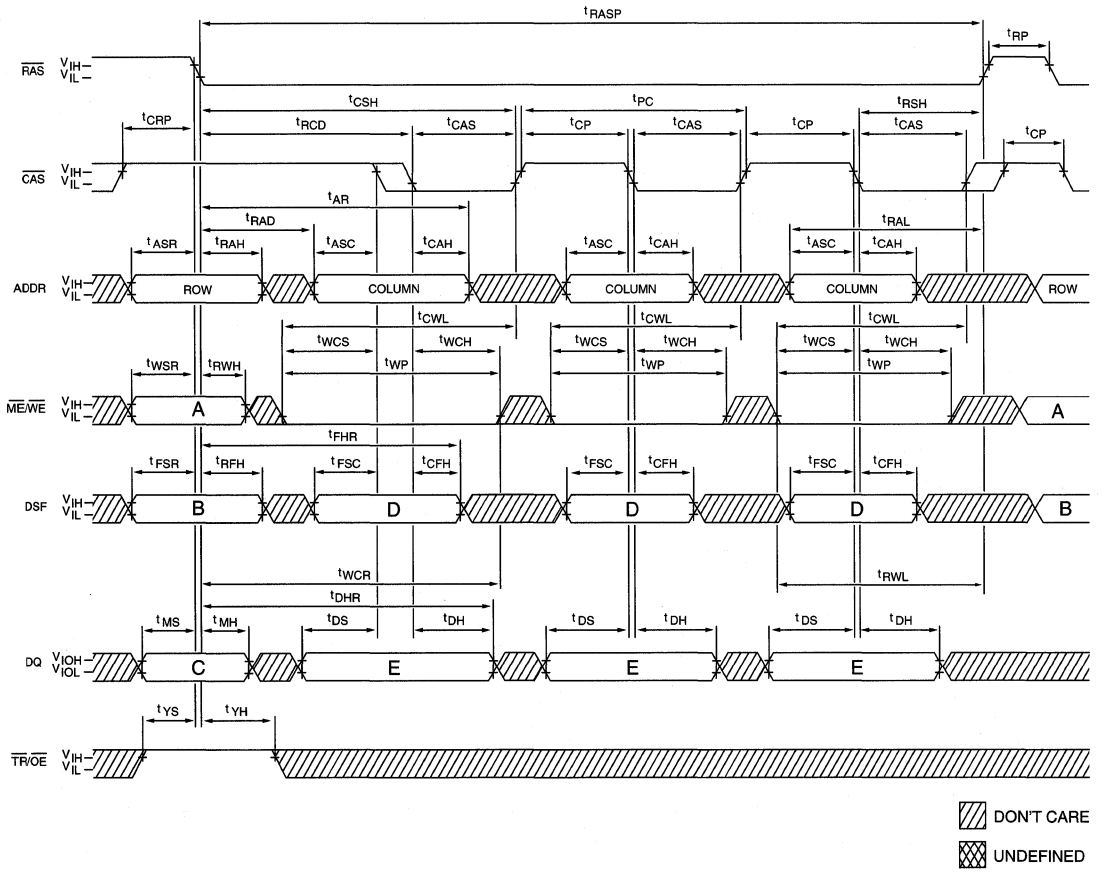
NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



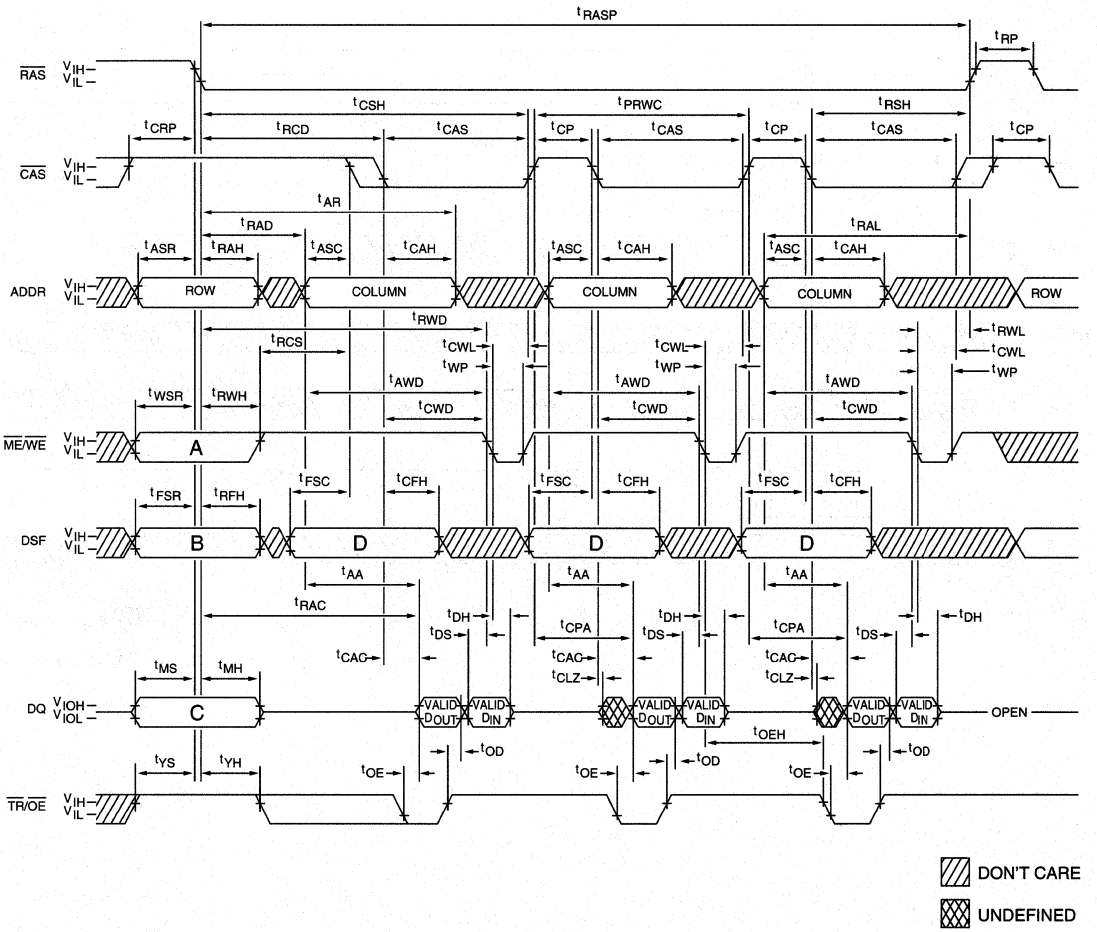
NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



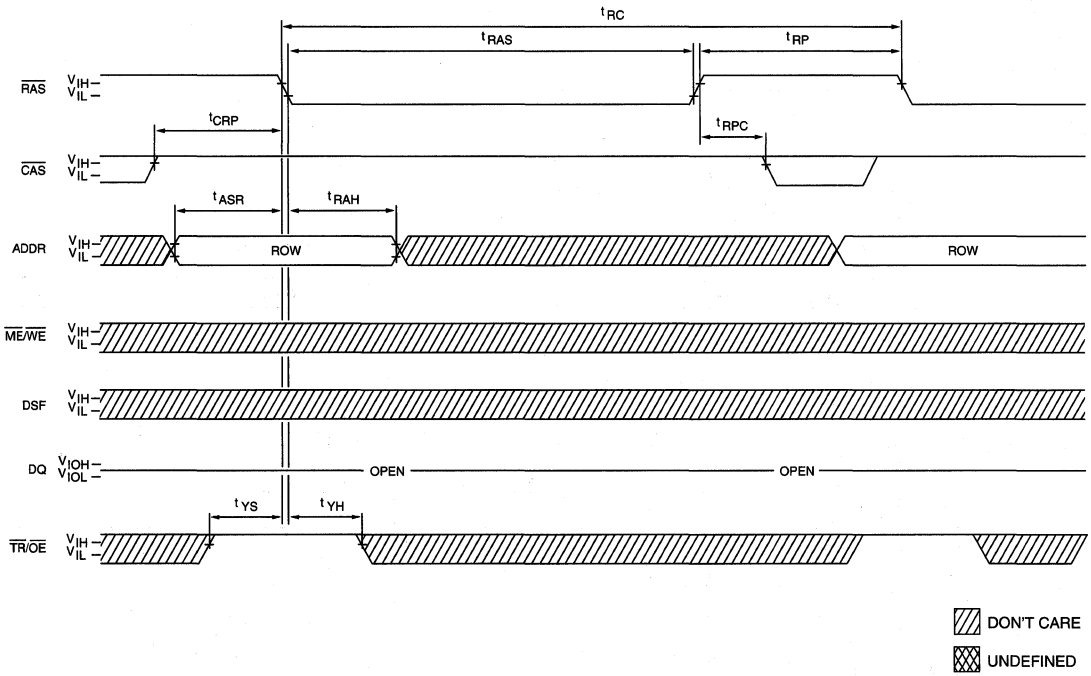
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE [1, 2]
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B", "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

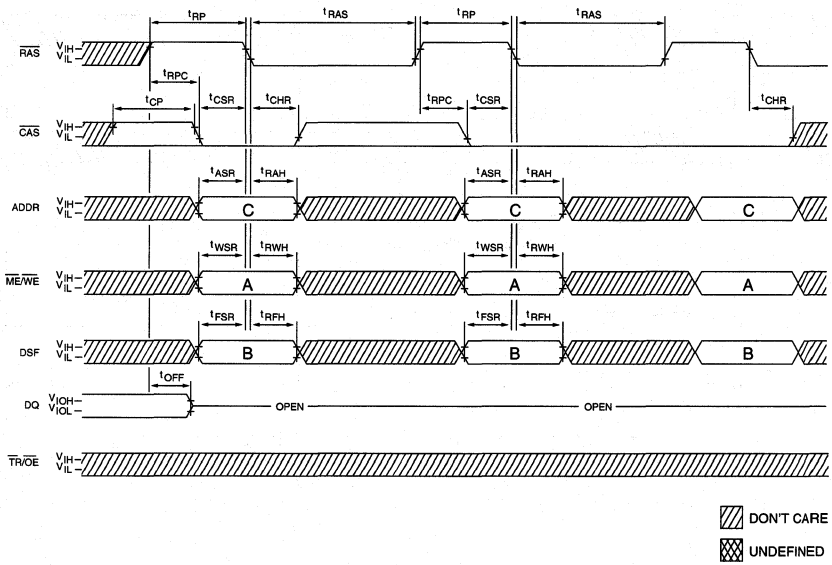
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CBR CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		RAS Falling Edge (CAS = LOW)		
		A ME/WE	B DSF	C A0-A8
CBR REFRESH (Reset All Options)	CBRR	X	0	X
CBR REFRESH (Set/Reset Stop Address)	CBRS	0	1	STOP ADDRESS[1]
CBR REFRESH (No Reset)	CBRN	1	1	X

CBR REFRESH CYCLE [2]



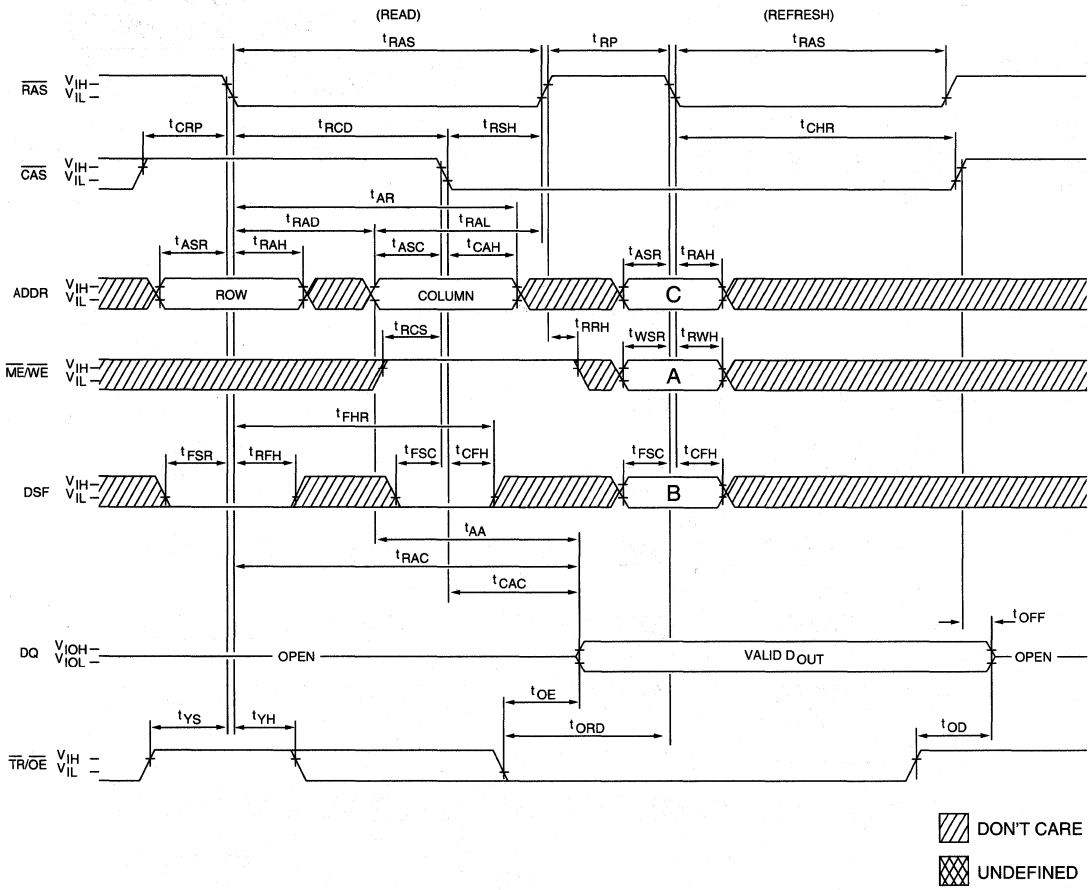
NOTE: 1. Programmable Stop Point column addresses:

Number Stop Points/Half	Address @ RAS LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

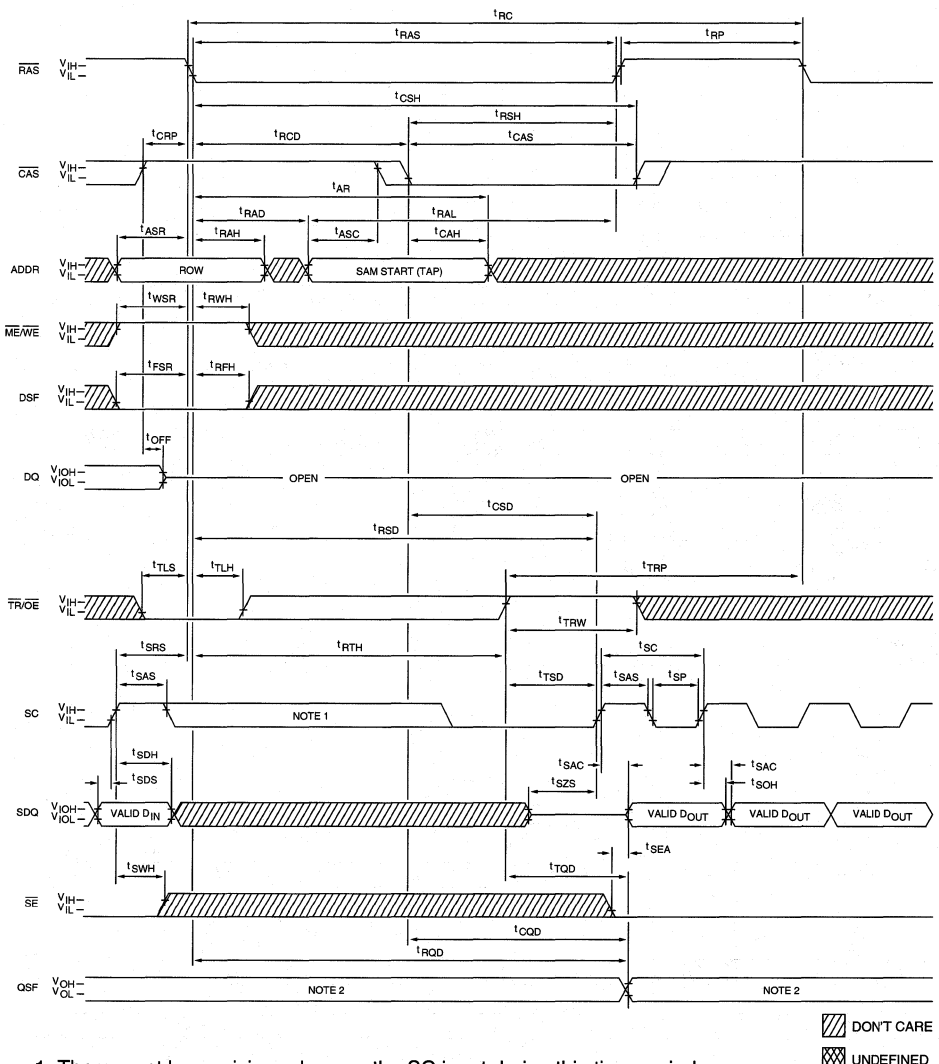
2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

DRAM HIDDEN-REFRESH CYCLE [1, 2]



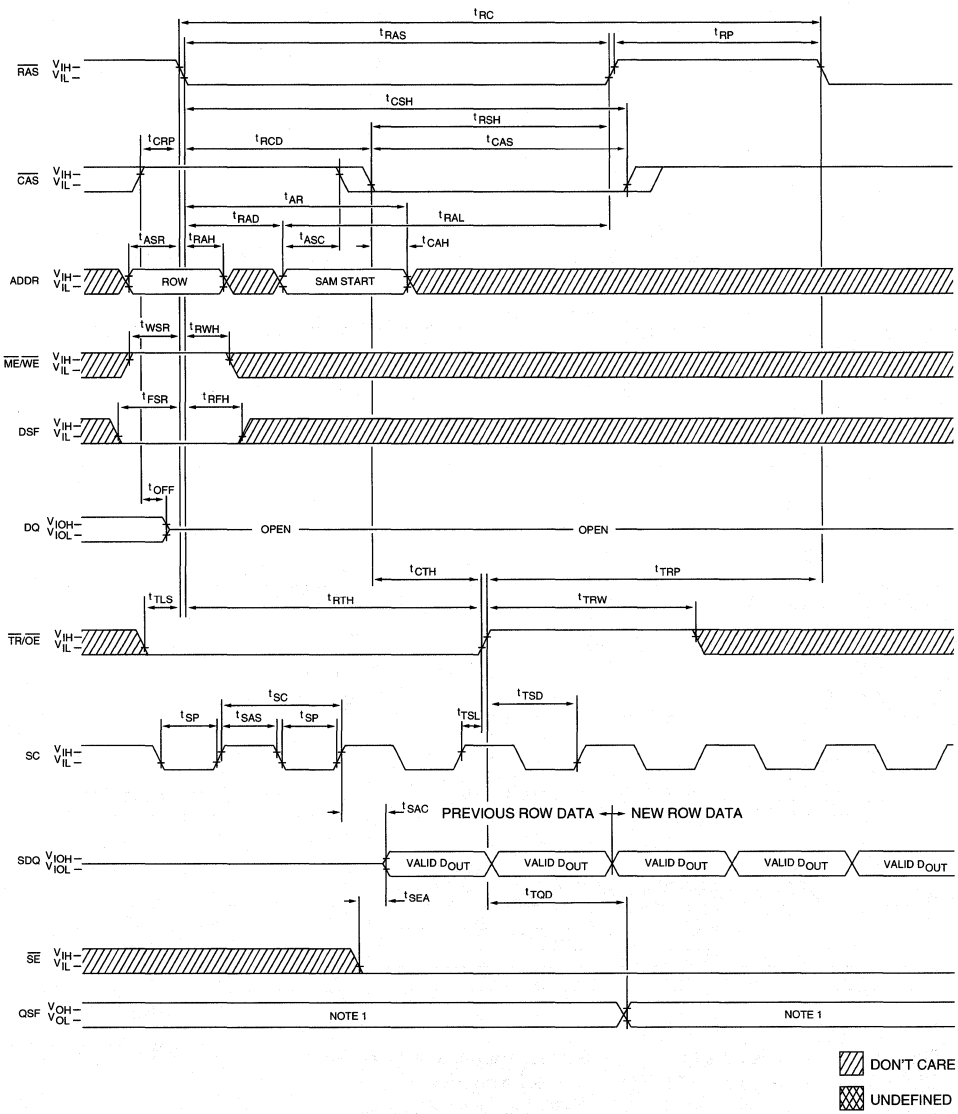
NOTE:
1. A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode, or SC idle)



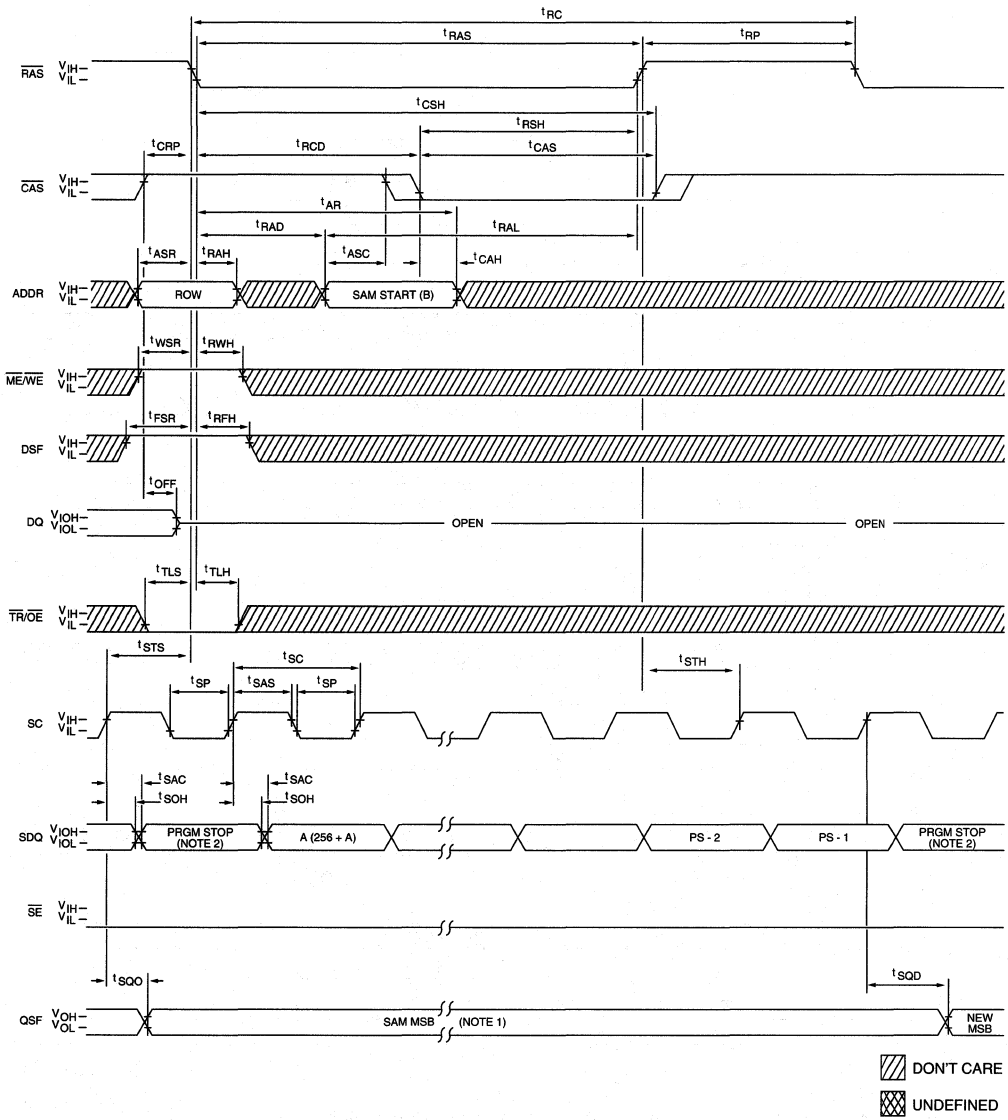
NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}$/($\overline{OE}$) rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}$/($\overline{OE}$) rising edge, the transfer is done off of the $\overline{TR}$/($\overline{OE}$) rising edge and ^{t}TSD must be met.

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



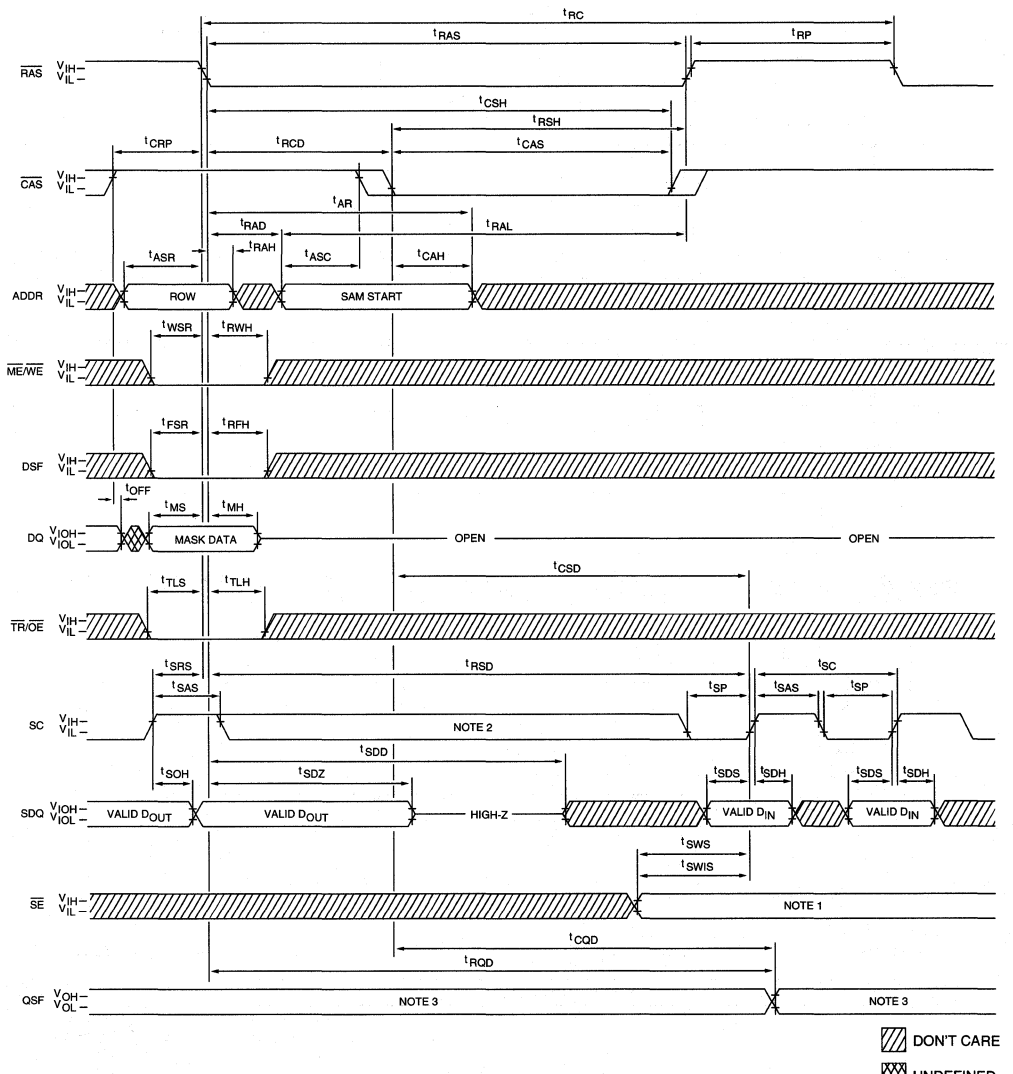
NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



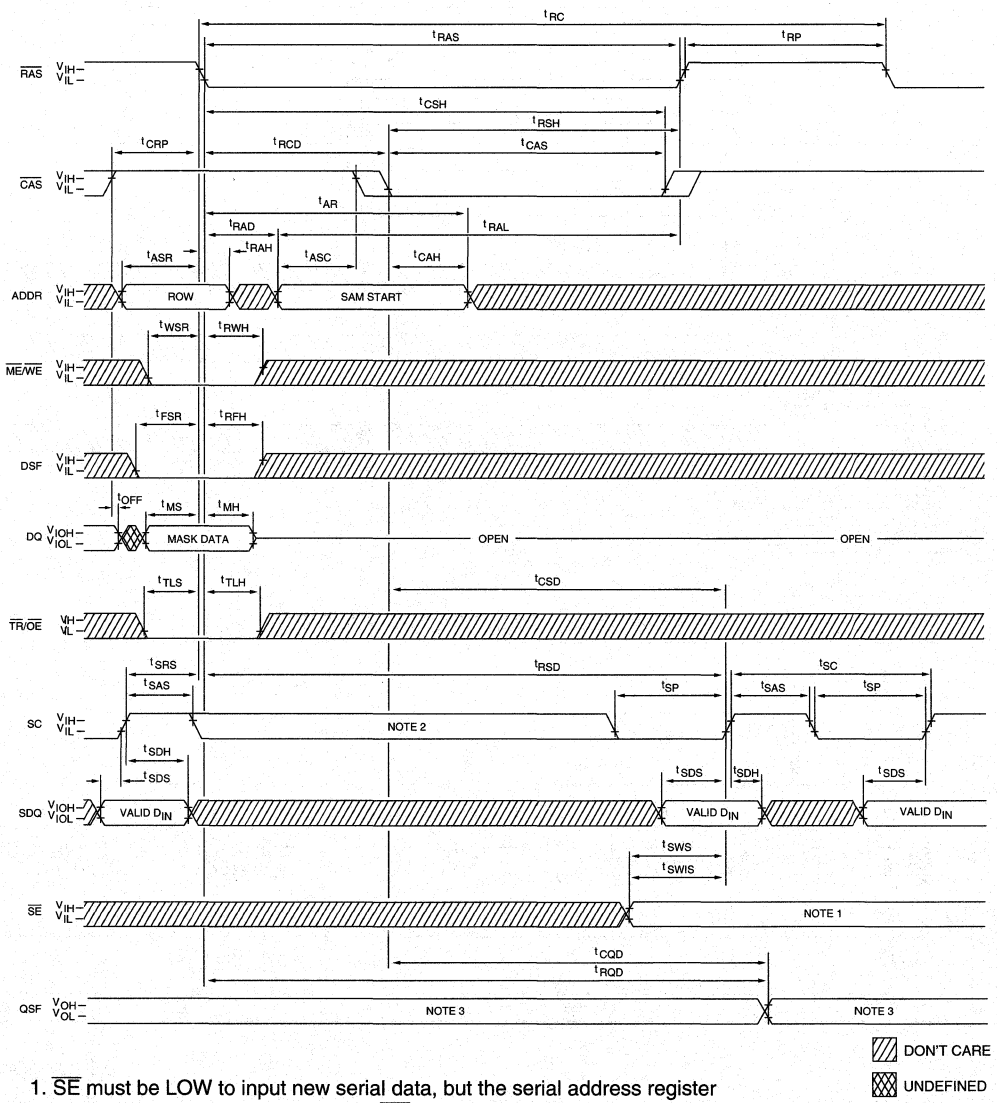
NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



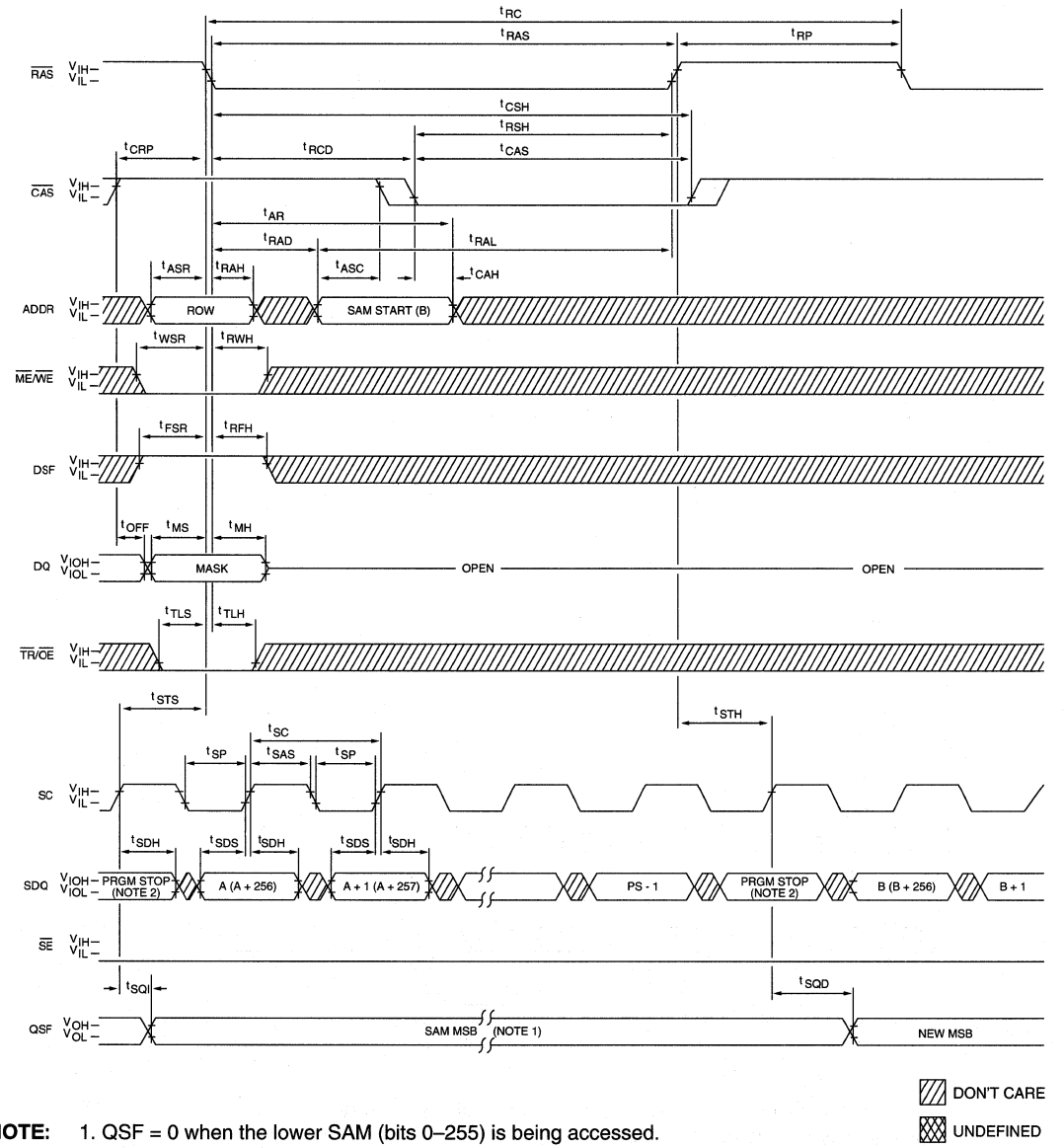
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.

MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



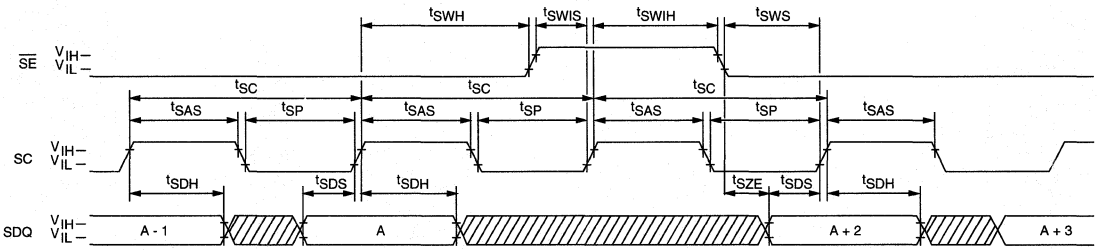
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 255–511) is being accessed.

MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

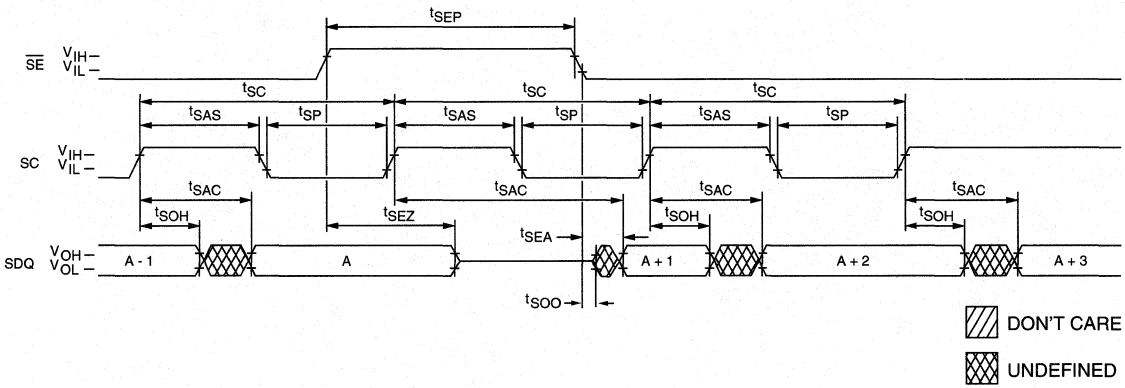


NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



NEW VRAM

VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- Dual port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times: 70ns random, 17ns serial
  60ns random, 15ns serial†

SPECIAL FUNCTIONS

- JEDEC-Standard Mandatory Function set
- PERSISTENT MASKED WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- PROGRAMMABLE SPLIT SAM

OPTIONS — MARKING

- Timing (DRAM, SAM [cycle/access])

60ns, 18/15ns	-6†
70ns, 20/17ns	-7
80ns, 22/20ns	-8

- Packages

Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG*
Plastic TSOP (400 mil) reverse pinout	RG*

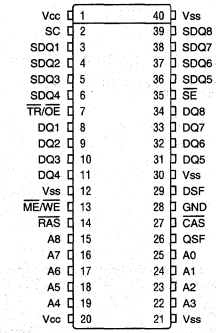
†60ns (-6) specifications are preliminary andare specified for Vcc = 5V ±5%. Please consult factory for availability.

GENERAL DESCRIPTION

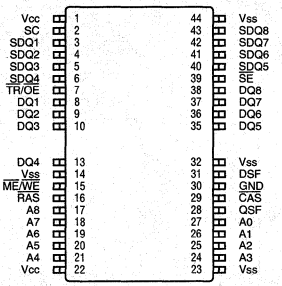
The MT42C8257 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

PIN ASSIGNMENT (Top View)

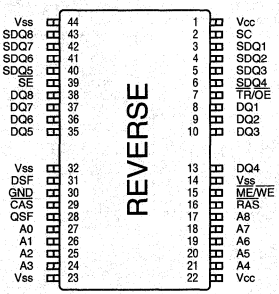
40-Pin SOJ (SDB-3)



40/44-Pin TSOP* (SDE-2)



40/44-Pin TSOP* (SDE-2)



*Consult factory for availability.

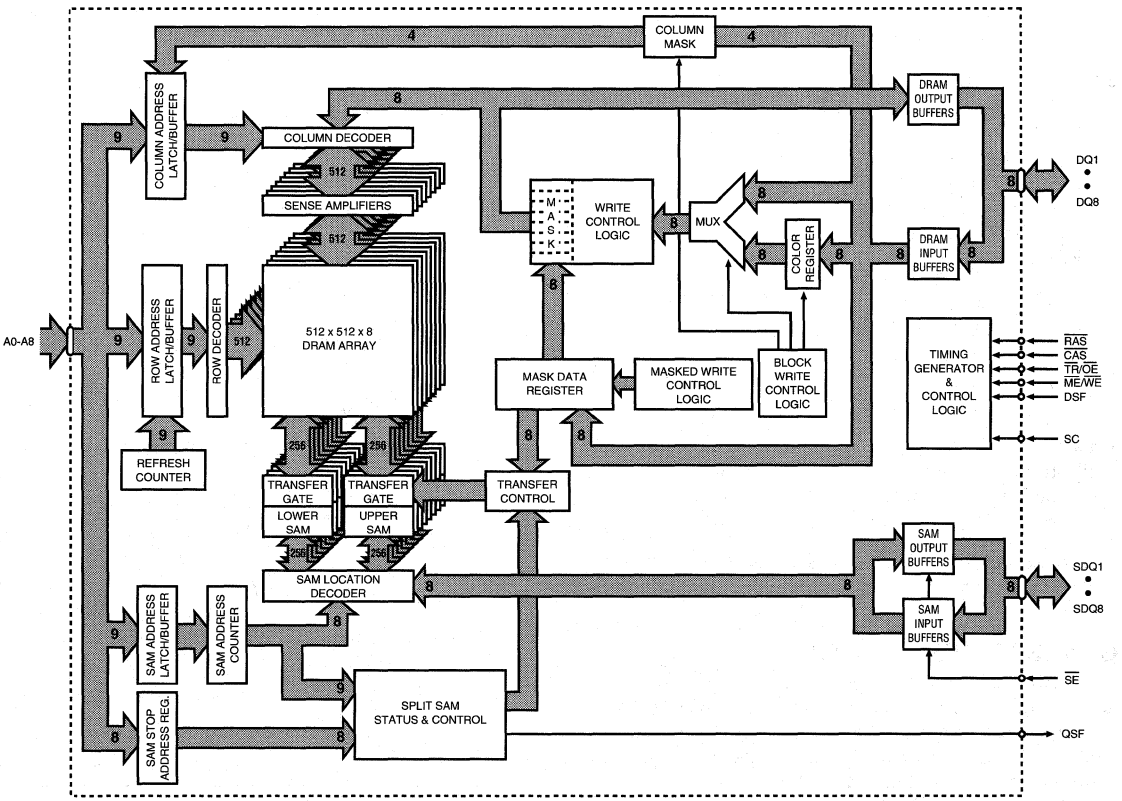
NEW VRAM

The DRAM portion of the VRAM is similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 512-bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8257 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter and data latch for the SAM registers.
7	7	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, FLASH WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and strobe for $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycles.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits and as a strobe for the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW), and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT TRANSFERs.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Mask and Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	V_{CC}	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8257 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8257 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C8257 supports CBR, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and must simply perform 512 CBR cycles within the 16.7ms time period. CBR cycles are also used to reset MASKED WRITE and PROGRAMMABLE SPLIT SAM operating modes. There are three CBR cycles defined for the MT42C8257: CBR No Reset (CBRN), CBR Reset Stop Address (CBRS), and CBR Reset All Options (CBRR). To perform these functions, two additional pins are defined for CBR cycles, $\overline{ME}/\overline{WE}$ and DSF1. These operations are described in detail in the MASKED WRITE and SPLIT READ/WRITE TRANSFER sections of the functional description.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8257 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the nine column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles or resets will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW and remains HIGH until $\overline{CAS}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/\overline{WE}$ performs two functions, write mask enable and data write enable. When $\overline{RAS}$ goes LOW, $\overline{ME}/(\overline{WE})$ is used to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (late or early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. The MT42C8257 supports two types of MASKED WRITE cycles, nonpersistent MASKED WRITE and persistent MASKED WRITE. When $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8257 initializes in the nonpersistent mode. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle.

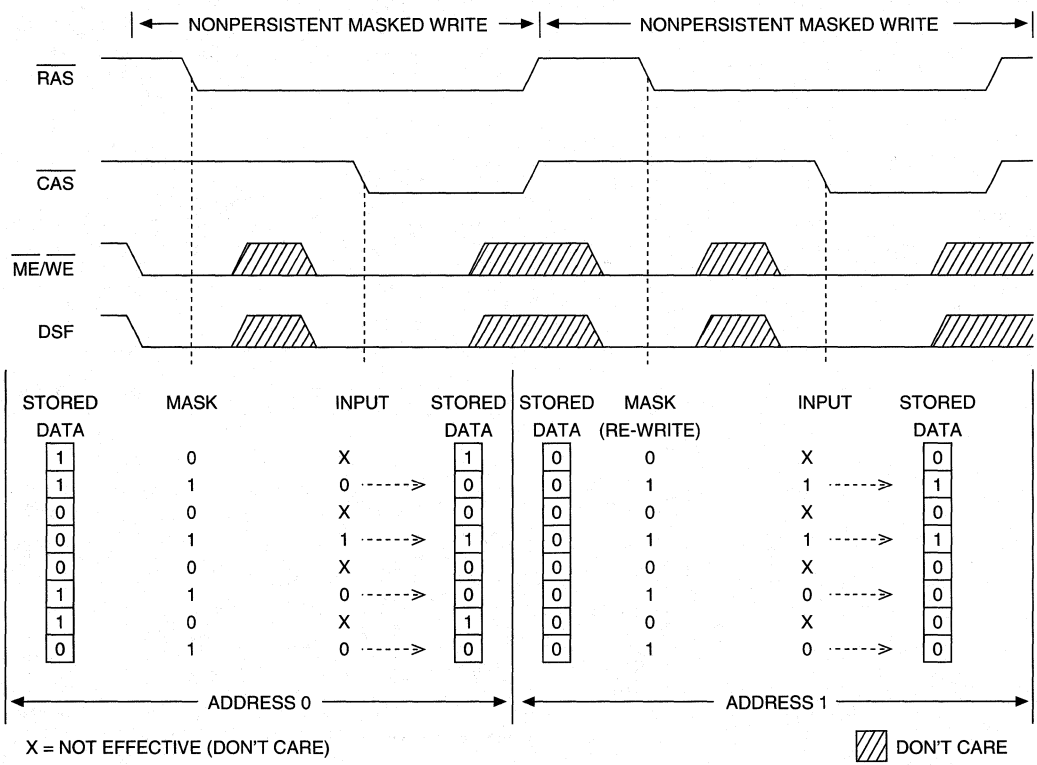


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

The selection of persistent or nonpersistent MASKED WRITE is done by performing a LOAD MASK REGISTER (LMR) cycle (see LMR description). If an LMR is done, all ensuing MASKED WRITEs are persistent and the mask data will be provided by the Mask Data Register (see Figure 2). The mask data is applied in the same manner as in nonpersistent mode.

To reset the device back to the nonpersistent mode, a CBR RESET All Options (CBRR) cycle must be performed. This cycle is defined as a CBR with DSF LOW when $\overline{RAS}$ falls; WE is "don't care." To preserve the persistent mode of MASKED WRITE, while using CBR REFRESH, a CBRN cycle is used. This cycle will perform a refresh of the internally addressed row of DRAM but will not reset the MASKED WRITE mode.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8257 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3 and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH;

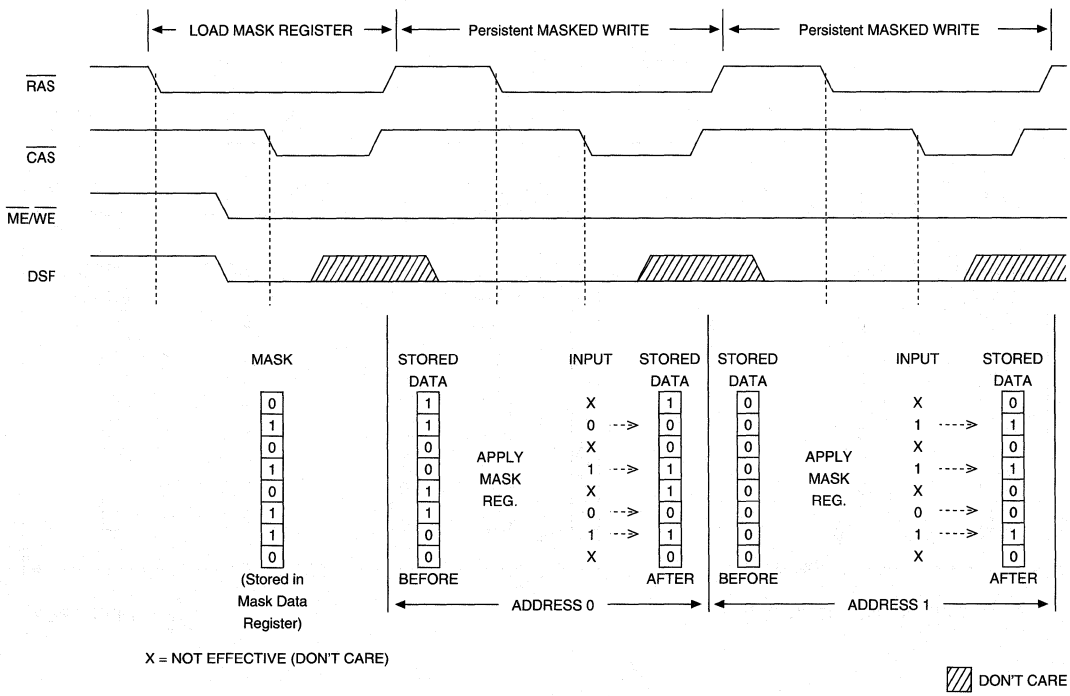


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

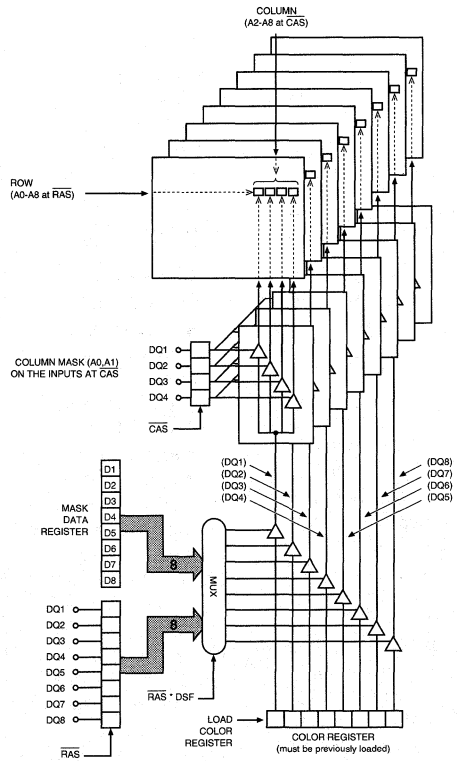


Figure 3
BLOCK WRITE EXAMPLE

a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

MASKED BLOCK WRITE

The MASKED WRITE functions may also be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BLOCK WRITE (BW), any combination of the eight bit planes may be masked, along with any combination of the four column locations.

The MASKED BLOCK WRITE will be nonpersistent (new mask) at device power-up. To enter persistent mode (old mask) a LOAD MASK REGISTER cycle is performed. All MASKED BLOCK WRITEs will be persistent after the LOAD MASK REGISTER (LMR). To reset to nonpersistent mode, a CBRR (reset all) cycle must be performed.

INPUTS	COLUMN ADDRESS CONTROLLED	
	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NEW VRAM

MASKED FLASH WRITE

The MASKED FLASH WRITE cycle is similar to the MASKED BLOCK WRITE cycle in that it uses the color register to accelerate the writing of a select color to the DRAM memory array. Instead of writing to four adjacent column locations in one DRAM cycle (BLOCK WRITE), FWM writes the contents of the color register to all column locations on an addressed row in one cycle.

The FWM cycle is selected by taking $\overline{TR}/(\overline{OE})$ and DSF HIGH and $\overline{ME}/(\overline{WE})$ LOW at the falling edge of $\overline{RAS}$. DSF is "don't care" at the falling edge of $\overline{CAS}$. The DQ plane mask applies as it does for all masked write cycles; if the mask register has been loaded, the mask is persistent; if it has not, the mask is nonpersistent.

LOAD MASK REGISTER

The LOAD MASK REGISTER (LMR) operation loads the data present on the DQ pins into the 8-bit mask data register at the falling edge of $\overline{CAS}$ or $(\overline{ME})/\overline{WE}$. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $(\overline{ME})/\overline{WE}$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle.

Note: *LOAD MASK REGISTER cycles also enable the persistent MASKED WRITE mode. All ensuing MASKED WRITEs (including MASKED WRITE and MASKED SPLIT WRITE TRANSFER) will be masked with data from the mask register. A CBRR has to be done to reset back to nonpersistent mode.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

During persistent operation, the mask data register contents are used for MASKED WRITE, MASKED BLOCK WRITE, MASKED FLASH WRITE, and MASKED WRITE and SPLIT WRITE TRANSFER cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER (LCR) cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE and FLASH WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER (RT) cycle is selected. The row-address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

SPLIT READ TRANSFER

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and is not synchronized with the serial clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM I/O port.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF), and to set SAM I/O direction. Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 (A8= 0, A0-A7=1) the QSF output goes HIGH and, if an SRT was done for the upper half, the new Tap address is loaded for the next half (A8 = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that Row 1 data is shifting out of the lower SAM) and execute an SRT of the upper half of Row 1 to the upper SAM. If the half-boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 5).

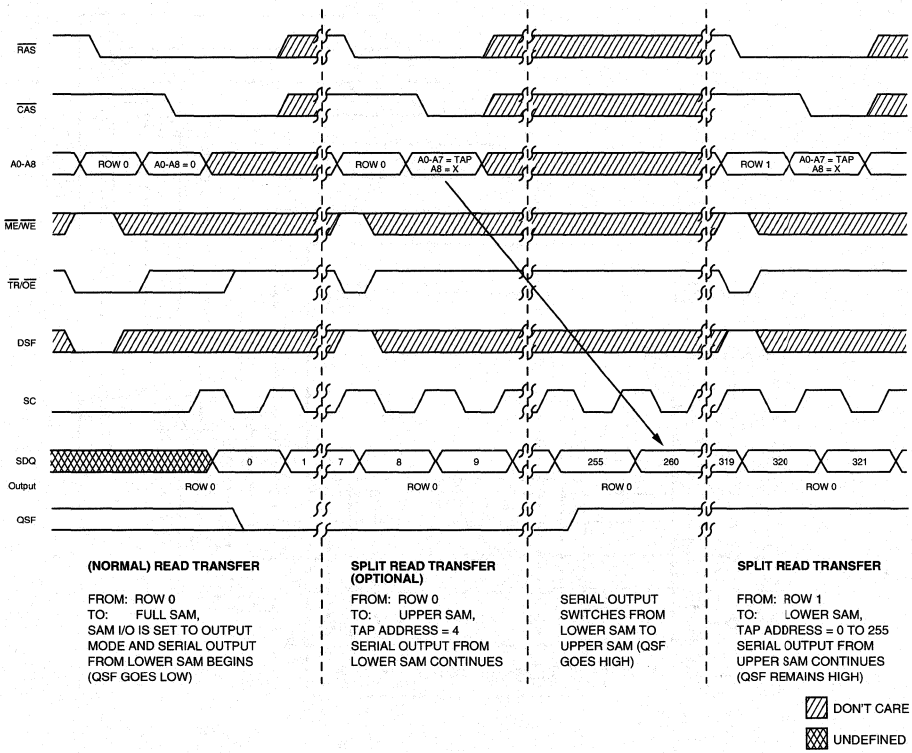


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

NEW VRAM

The stop address of the SAM half (the point at which access will change to the next half) is programmable on the MT42C8257. This function is described in the PROGRAMMABLE SPLIT SAM section of the functional description.

MASKED WRITE TRANSFER

The operation of the MASKED WRITE TRANSFER (MWT) is identical to that of the READ TRANSFER described previously except ($\overline{ME}$)/$\overline{WE}$ is LOW and a DQ plane mask is applied when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A DQ mask must be applied to all MWTs as shown in Figure 6. This may be done using persistent or nonpersistent modes. When using persistent mode, the mask will be supplied by the mask register. When in nonpersistent mode, the DQ pins are used to input a bit plane mask at the falling edge of $\overline{RAS}$. An MWT changes the direction of the SAM I/O buffers to the input mode. To change the SAM I/O buffers to input mode without SAM data being transferred to the DRAM, a mask of all zeros must be presented on the DQ pins when $\overline{RAS}$ falls. QSF is LOW if serial input is to the lower half of the SAM, and HIGH if it is to the upper.

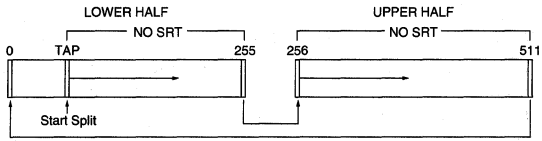


Figure 5
SPLIT SAM TRANSFER

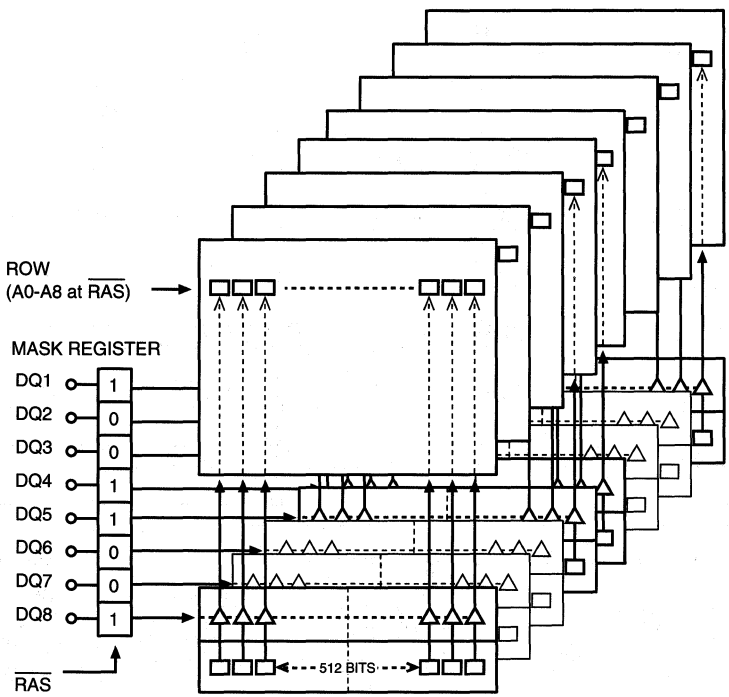


Figure 6
DQ MASKED WRITE TRANSFER

MASKED SPLIT WRITE TRANSFER

The MASKED SPLIT WRITE TRANSFER (MSWT) cycle allows serial input data to be transferred to the DRAM without interrupting the serial clock. Operation of the SWT cycle is very similar to the SPLIT READ TRANSFER cycle. It will transfer the idle half of the SAM to the DRAM and set the Tap address to where the new serial data will be loaded in that half. Selection of the MSWT cycle is the same as that of the MASKED WRITE TRANSFER with the exception of the state of DSF. When DSF is HIGH at the falling edge of $\overline{RAS}$, an MSWT will occur. The initiation sequence for MSWT is shown in Figure 7. An MSWT will not change the direction of the SAM I/O buffers.

PROGRAMMABLE SPLIT SAM

Programmable Split SAM operation is an extension of the Split SAM mode. This mode optimizes SAM performance by allowing user-programmable stop points to be defined in the split SAM. The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the loaded Tap address). The locations of the stop points are programmable in power-of-two increments. The stop points and size of the resulting partitions are shown in Figure 8, along with an example.

The stop points are set by performing a CBR RESET STOP (CBRS) address cycle. A CBRS cycle is a CBR with $\overline{ME}/\overline{WE}$ LOW and DSF HIGH at the $\overline{RAS}$ HIGH-to-LOW transition.

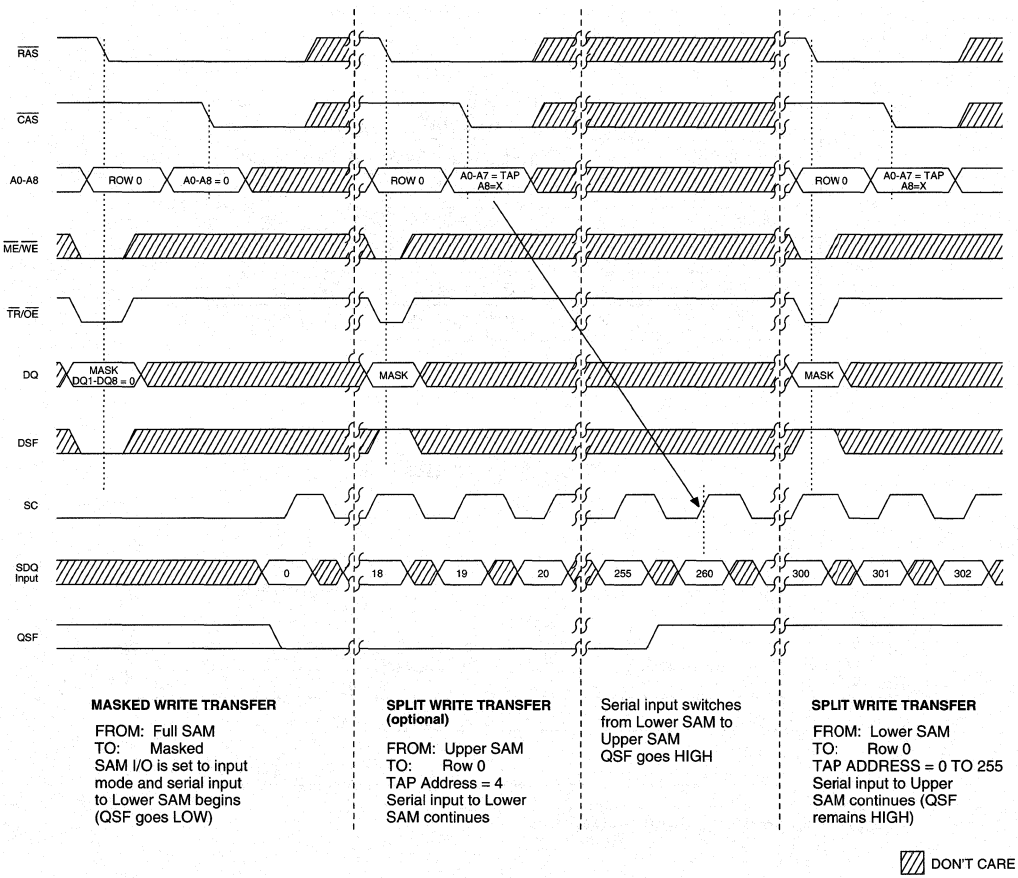


Figure 7
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

NEW VRAM

This is a special CBR refresh cycle that, in addition to refreshing the DRAM, will sample the address pins (A4-A8) and set the stop point partition to the addressed value (See Figure 8). The programmable stop points will not become valid until a Split Transfer (READ or WRITE) is done, following the CBRS. Both halves of the SAM will be programmed simultaneously to the same partition lengths and stop points.

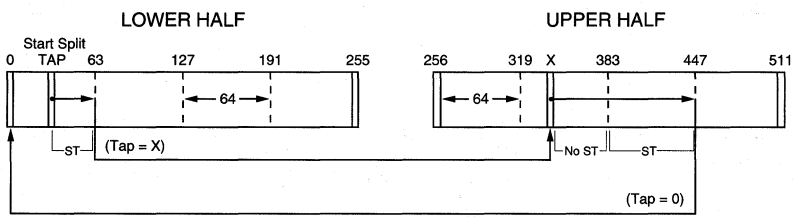
Access will progress from the Tap address to the end of the programmable partition into which the Tap fell. When the end of the "addressed" partition is reached, the access will jump to the tap address of the next half, provided that a SPLIT TRANSFER (READ or WRITE) was done before the partition boundary was reached. If a SPLIT TRANSFER (ST) is not done prior to the terminal count of the partition, the partition is not recognized and the address count will continue in the same half (this is shown Figure 8 at stop address 383). The count will continue in the same half until a SPLIT TRANSFER (READ or WRITE) occurs or the SAM half boundary is reached. In Figure 8, an ST occurs some time between addresses 383 and 447 and the boundary is recognized at 447. The programmable stop points may be reprogrammed at any time by performing another CBRS cycle, the new stop points will not be valid until an ST is performed.

Disabling the programmable split SAM requires a CBRR. This is a CBR cycle with DSF LOW at the $\overline{RAS}$ HIGH-to-LOW transition. The CBRR will take effect immediately; it does not require an ST to become active valid.

Number Stop Points/Half	Address @ $\overline{RAS}$ LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

EXAMPLE
(four stop points)



Programmed Partition (A4-A8) = 000111111
MSB....LSB

Figure 8
PROGRAMMABLE SPLIT SAM OPERATION

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the SERIAL INPUT/OUTPUT buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address zero if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the SERIAL INPUT mode. As in the serial output operation, the contents of the SAM address counter (loaded when the SERIAL INPUT mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for SERIAL INPUT data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP and INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data, and the nonpersistent MASKED WRITE mode is enabled.

The SAM portion of the MT42C8257 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the SERIAL INPUT mode (MASKED WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The mask and color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS											
CBRR	CBR REFRESH (RESET ALL OPTIONS)	0	X	X	0	—	X	X	—	X	X	X
CBRS	CBR REFRESH (RESET STOP ADDRESS)	0	X	0	1	—	STOP[7]	X	—	X	X	X
CBRN	CBR REFRESH (NO RESET)	0	X	1	1	—	X	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X	X
RWM	MASKED WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK[4]	VALID DATA	USE[4]	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWM	MASKED BLOCK WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK[4]	COLUMN MASK	USE[4]	USE
FWM	MASKED FLASH WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	1	X	ROW	X	WRITE MASK[4]	X	USE[4]	USE
	REGISTER OPERATIONS											
LMR	LOAD MASK REGISTER	1	1	1	1	0	ROW[5]	X	X	REG DATA	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[5]	X	X	REG DATA	X	LOAD
	TRANSFER OPERATIONS											
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[6]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[6]	X	X	X	X
MWT	MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	0	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X
MSWT	MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NEW OR OLD MASK)	1	0	0	1	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is last. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is last.
4. After an LMR cycle, all masked WRITEs use the mask register (old mask). Data on the DQs at RAS falling edge will be ignored. A CBRR will reset to new mask state and mask data must be presented on the DQs at every RAS falling edge.
5. The ROW that is addressed will be refreshed, but a ROW address is not required.
6. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half or programmable stop address boundary).
7. Defines the column addresses where access moves to the next half; see Programmable Split SAM functional description.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6***	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	165	155	145	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC2}	110	100	90	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	165	155	145	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	165	155	145	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	185	175	165	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6***	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	215	205	190	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC8}	160	150	135	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC9}	50	50	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	215	205	190	mA	3, 4, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	215	205	190	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	220	210	195	mA	3, 4

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	148		170		190		ns	
FAST-PAGE-MODE READ, WRITE, MASKED WRITE or BLOCK WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	83		90		95		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	15, 28
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	12		12		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	tOFF	3	20	3	20	3	20	ns	20, 23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	tOD	3	10	3	10	3	10	ns	20, 23
Output enable delay from ($\overline{TR}$)/$\overline{OE}$	tOELZ	3		3		3		ns	
Output disable delay from ($\overline{ME}$)/$\overline{WE}$	tWHZ	3	10	3	10	3	10	ns	
Output disable hold time from start of WRITE	tOEH	10		10		10		ns	27
Output Enable to $\overline{RAS}$ delay	tORD	0		0		0		ns	
Data output hold after $\overline{CAS}$ LOW	tCOH	5		5		5		ns	28

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

NEW VRAM

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	12		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	18		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	18		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	12		12		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		100		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	50		55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	35		40		40		ns	21
Transition time (rise or fall)	tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	tRWH	15		15		15		ns	
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	tRTH	60	10,000	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	tCTH	15		20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	50		50		50		ns	
$\overline{TR}/(\overline{OE})$ precharge time	tTRW	15		20		25		ns	
$\overline{TR}/(\overline{OE})$ LOW to last SC hold time	tTSL	5		5		5		ns	29
$\overline{TR}/(\overline{OE})$ HIGH to first SC setup time	tTSD	50		50		50		ns	29
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	tSZS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	15		15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	15		15		15		ns	
SC to QSF delay time	tSQD		20		25		30	ns	
SPLIT TRANSFER setup time	tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	tSTH	10		10		10		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	tFHR	45		55		60		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	15		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		30		30		30	ns	
$\overline{RAS}$ to QSF delay time	tRQD		70		75		75	ns	
$\overline{CAS}$ to QSF delay time	tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	tRSD	95		105		115		ns	
$\overline{CAS}$ to first SC delay	tCSD	50		55		55		ns	

*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	18		20		22		ns	
Access time from SC	^tSAC		15		17		20	ns	24, 28
SC precharge time (SC LOW time)	^tSP	7		8		9		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		9		ns	
Access time from $\overline{SE}$	^tSEA		12		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		9		ns	
Serial data-out hold time after SC high	^tSOH	3		3		3		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial output buffer turn-on delay from $\overline{SE}$	^tSOO	3		3		3		ns	
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

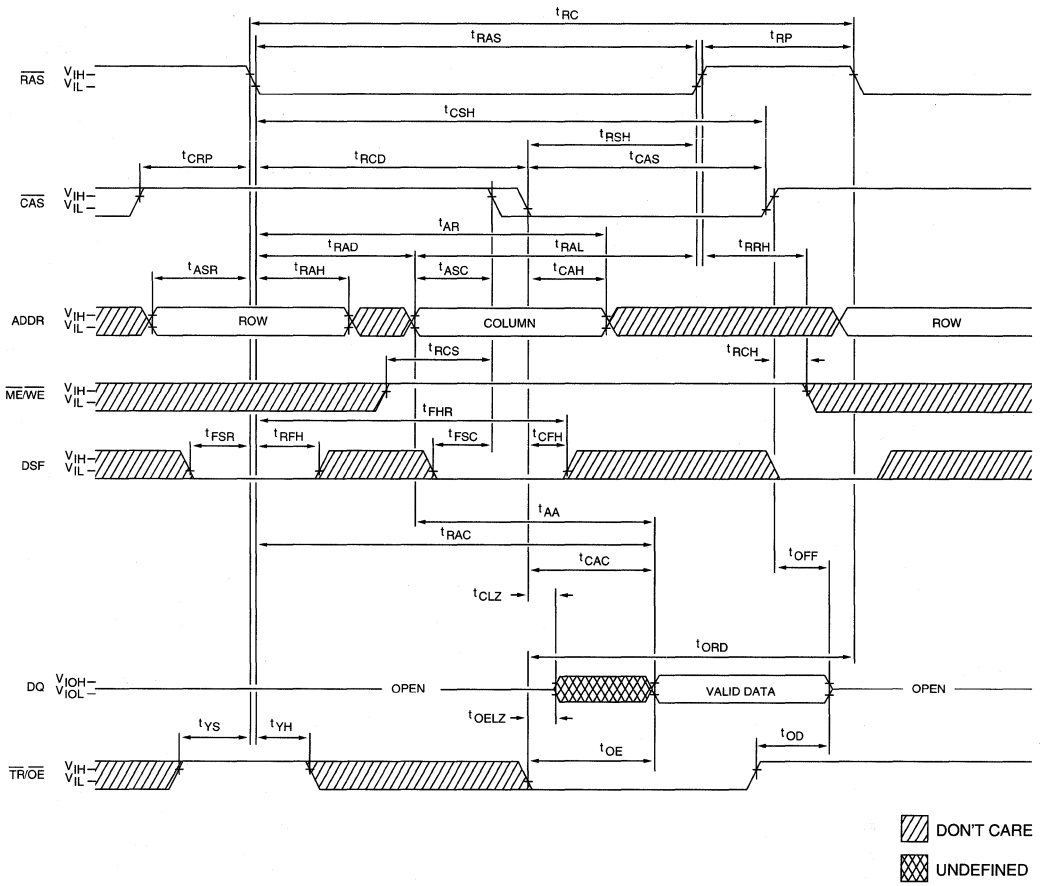
*60ns (-6) specifications are preliminary and are specified for Vcc = 5V ±5%. Please consult factory for availability.

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to one TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq ^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OD, ^{t}OFF and ^{t}SEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq ^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^{t}WCS \leq ^{t}WCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^{t}RWD \geq ^{t}RWD$ (MIN), $^{t}AWD \geq ^{t}AWD$ (MIN) and $^{t}CWD \geq ^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate, but the WRITE will be valid if ^{t}OD and ^{t}OEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to one TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. $^{t}SAC/^{t}CAC$ are MAX at 70° C and 4.5V Vcc; $^{t}SOH/^{t}COH$ are MIN at 0° C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. This is guaranteed by design ($^{t}SOH = ^{t}SAC$ - output transition time; $^{t}COH = ^{t}CAC$ - output transition time).
29. The "last" SC edge causes the last data from the previous row to appear on the SDQ pins. The "first" SC causes the first data from the new row to appear.

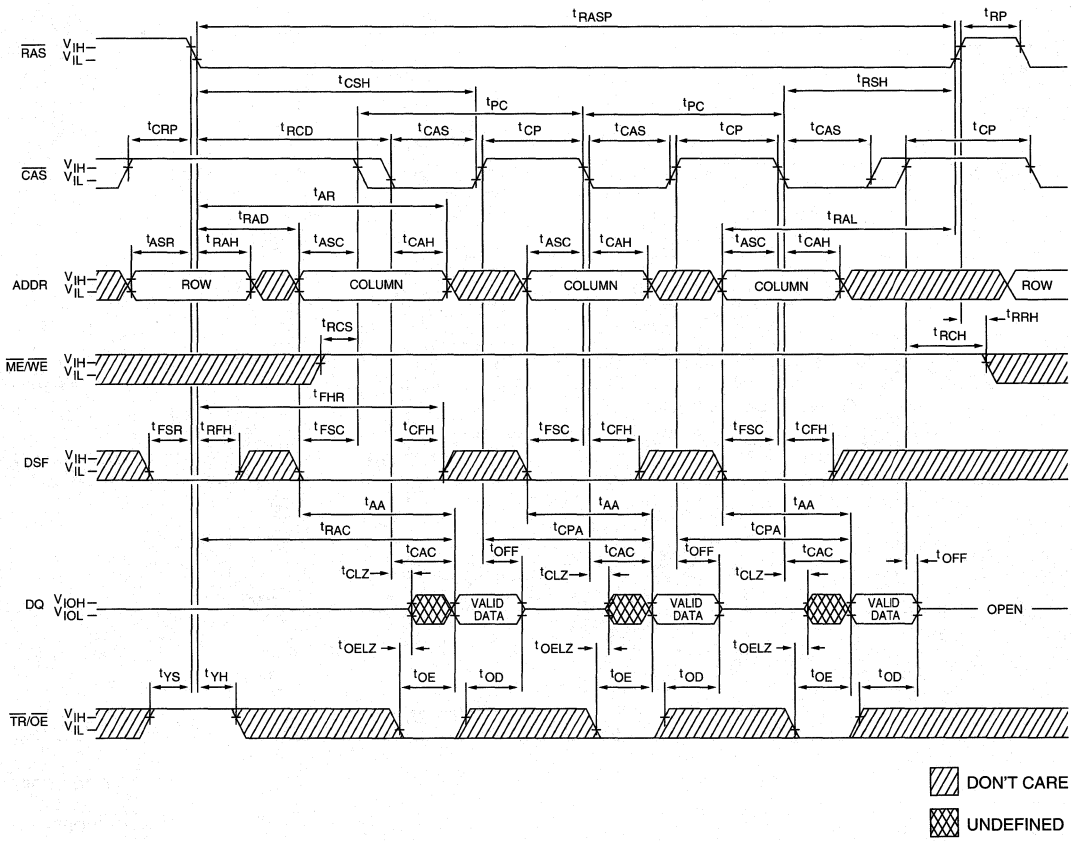
NEW VRAM

DRAM READ CYCLE



NEW VRAM

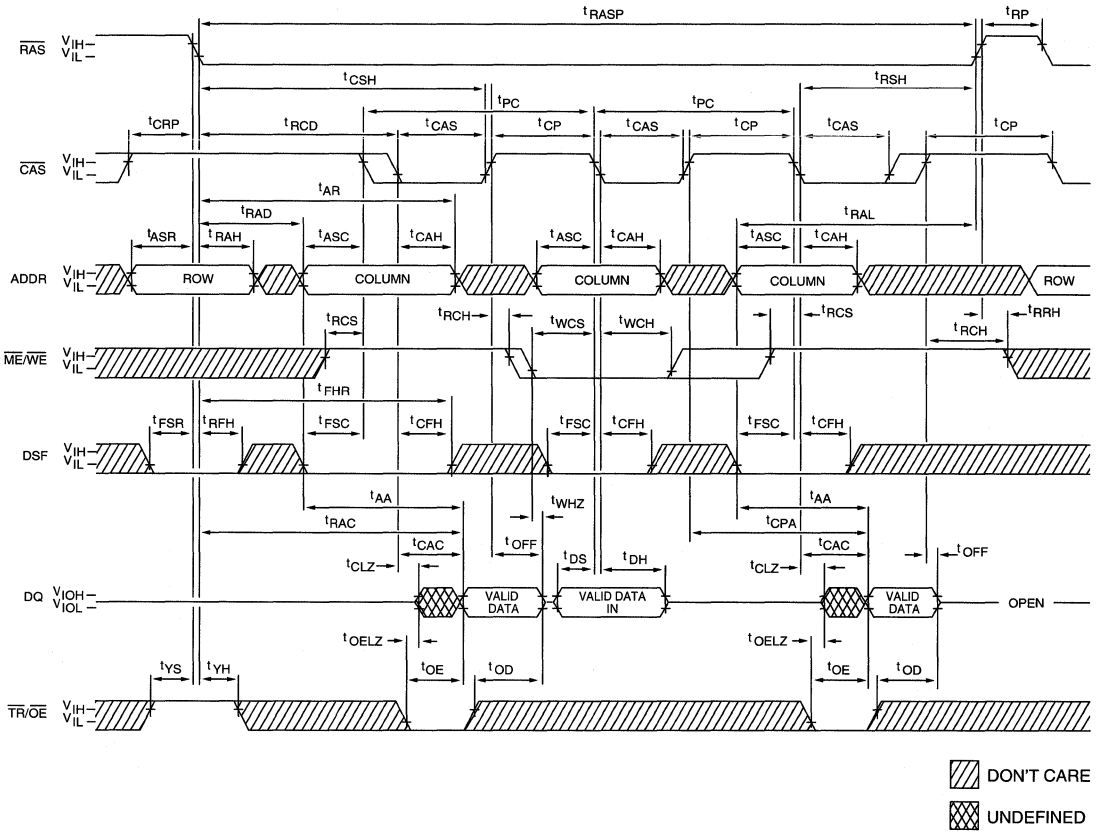
DRAM FAST-PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

NEW VRAM

DRAM FAST-PAGE-MODE READ/WRITE CYCLE



NOTE: Any one of the following signals: (TR)/OE, (ME)/WE or CAS, can be used to disable the data outputs before presenting input data. The controlling parameter would then be tOD, tWHZ or tOFF, respectively, or the first to be met when more than one parameter is applicable.

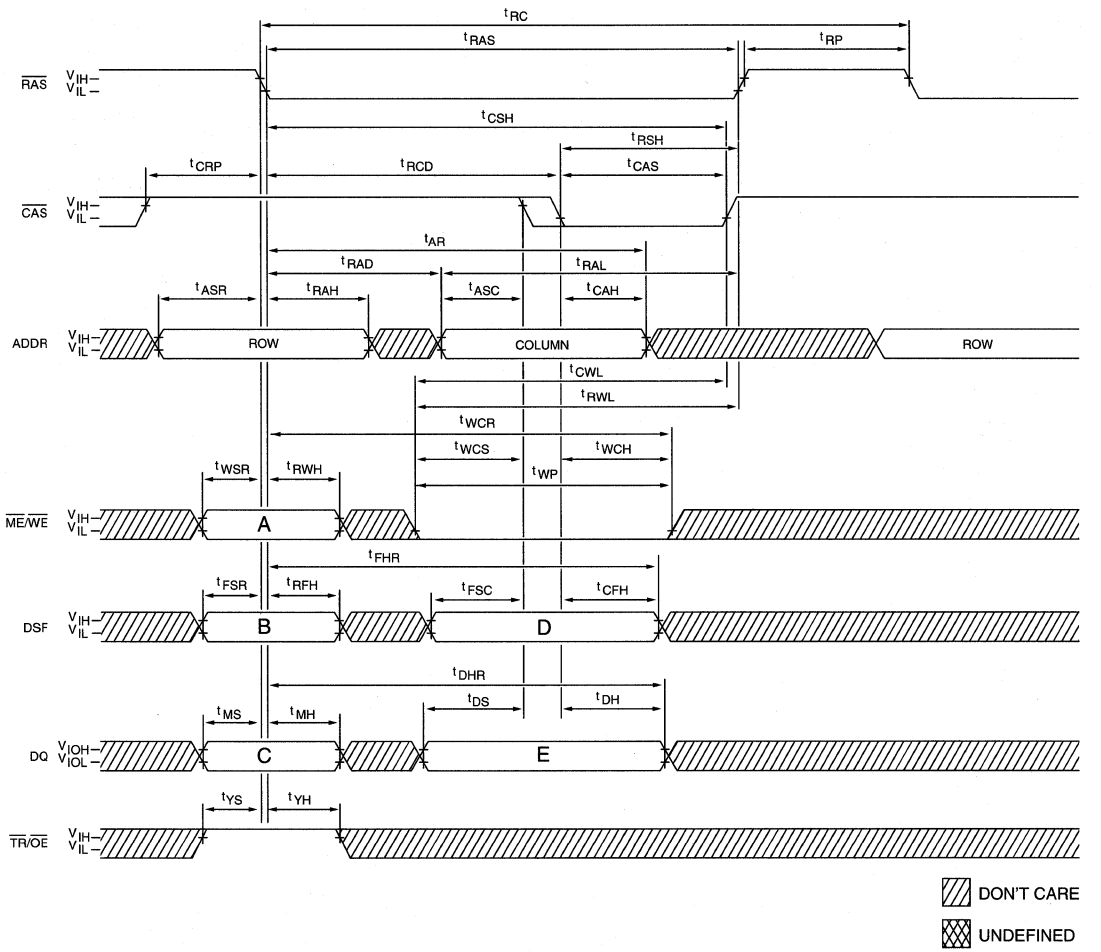
WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask[3]	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask[3]	1	Column Mask
MASKED FLASH WRITE to DRAM	0	1	Write Mask[3]	X	X
Load Mask Data Register	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs last.
3. Mask Data is loaded at $\overline{RAS}$ falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the Mask Data Register and the DQs are "don't care" at the $\overline{RAS}$ falling edge.

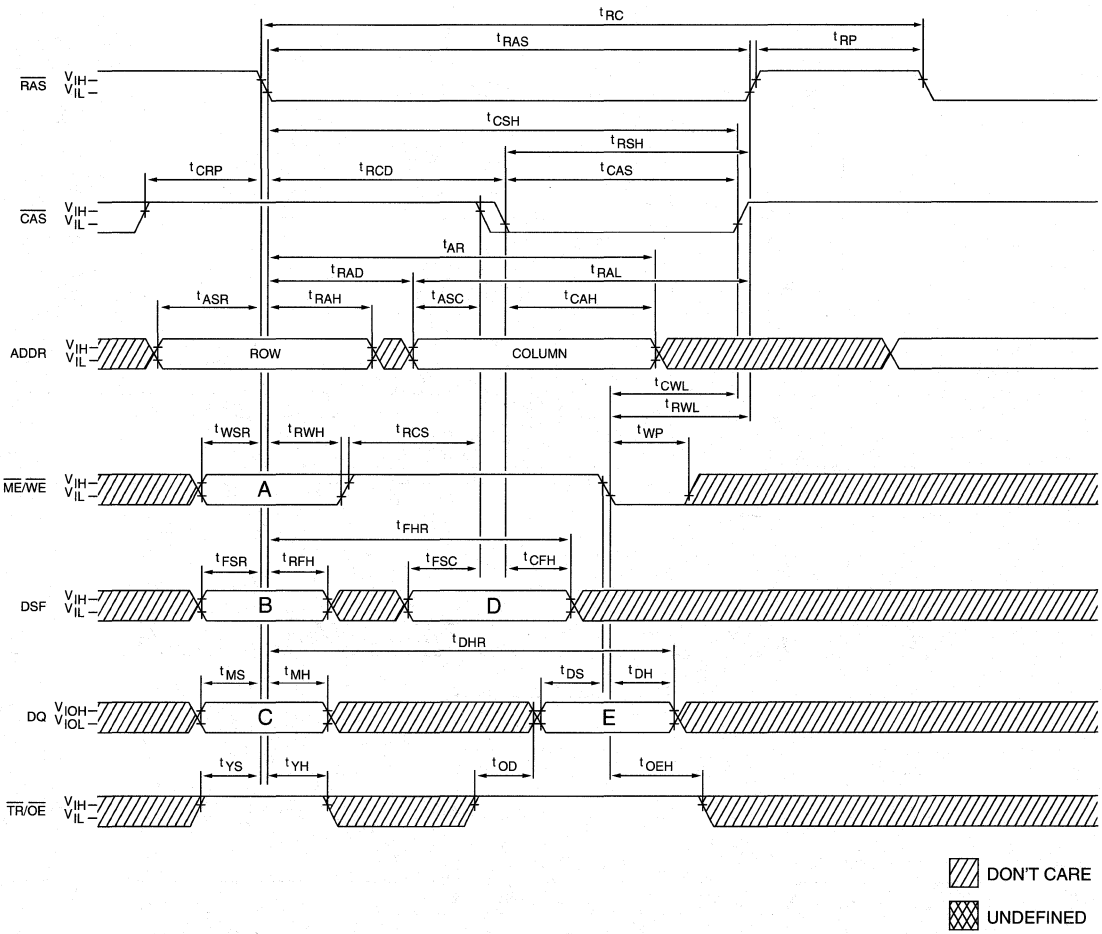
NEW VRAM

DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

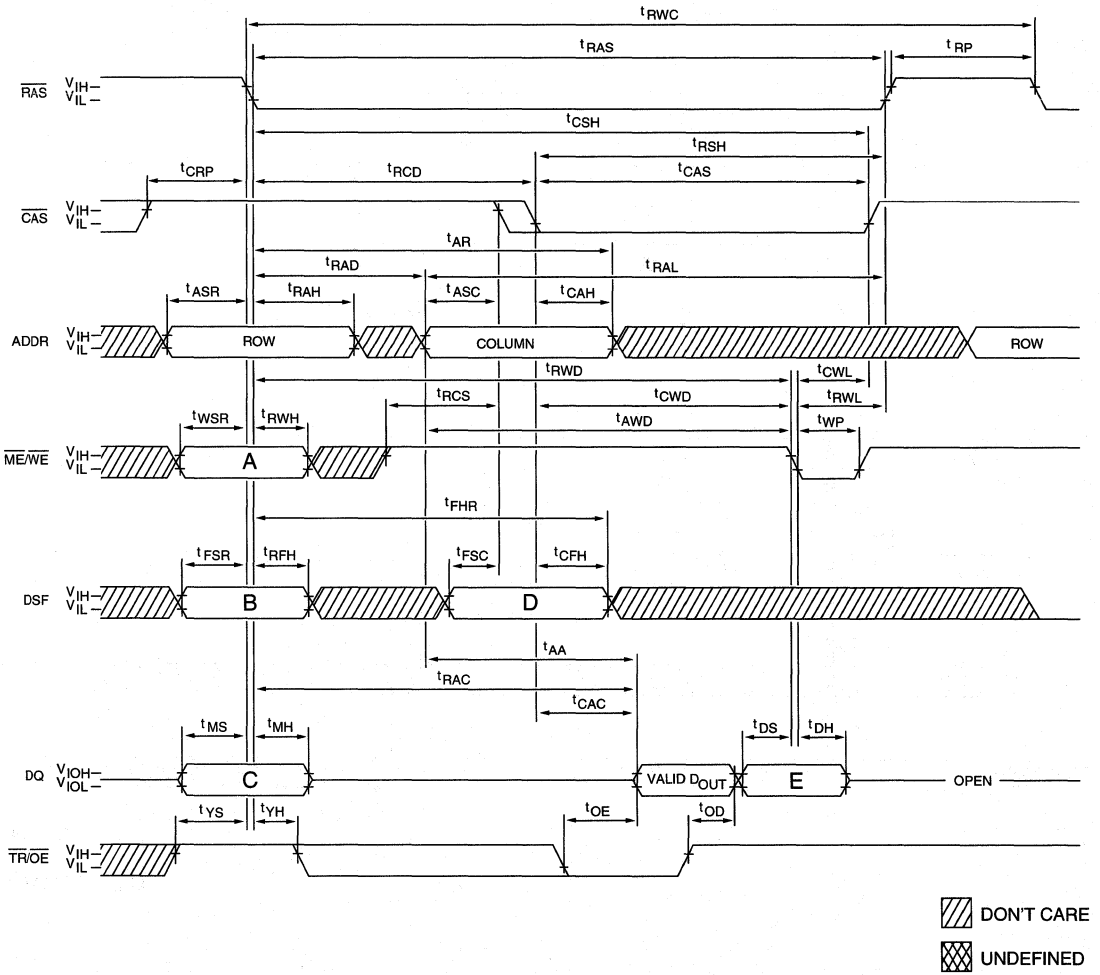
DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

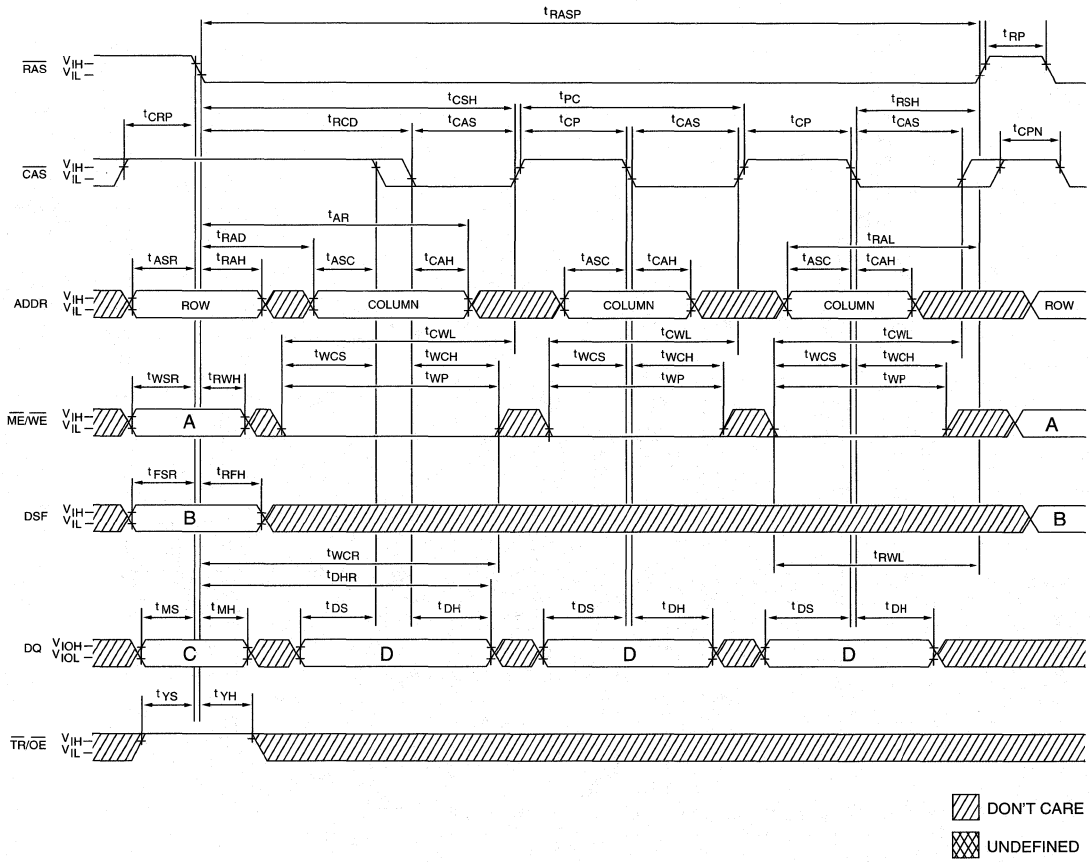
NEW VRAM

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

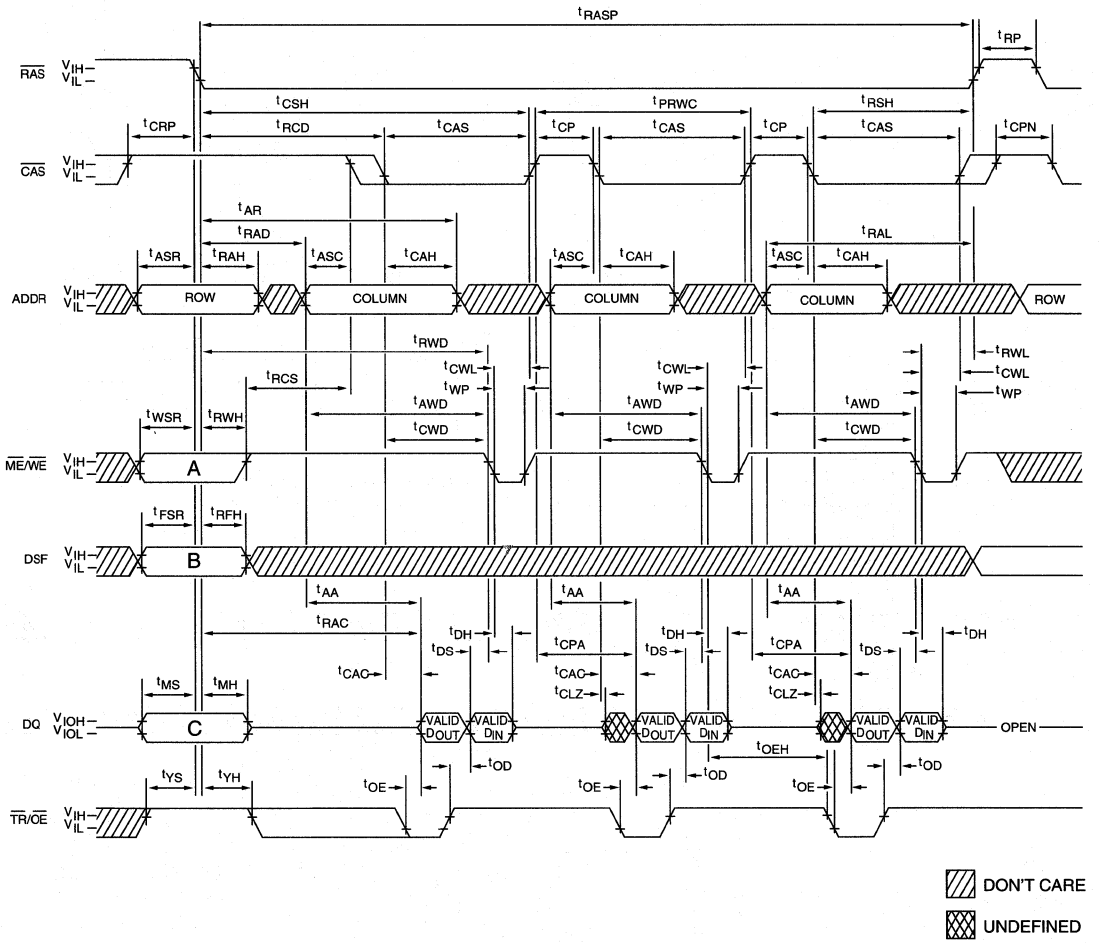
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW VRAM

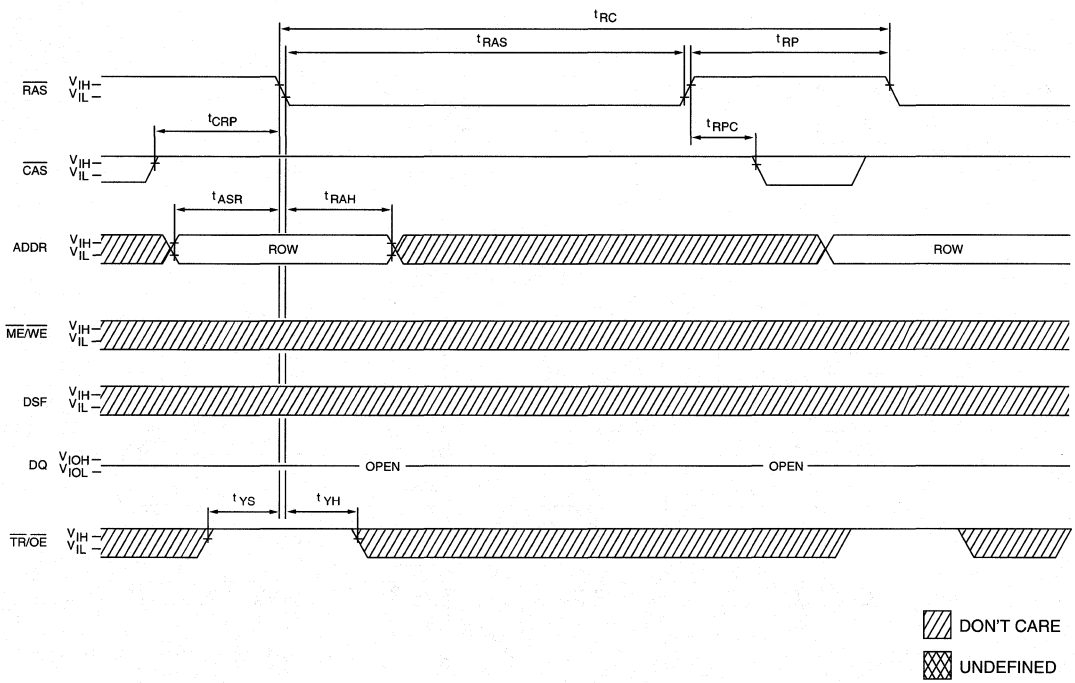
DRAM FAST-PAGE-MODE READ-WRITE CYCLE [1, 2]
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW VRAM

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

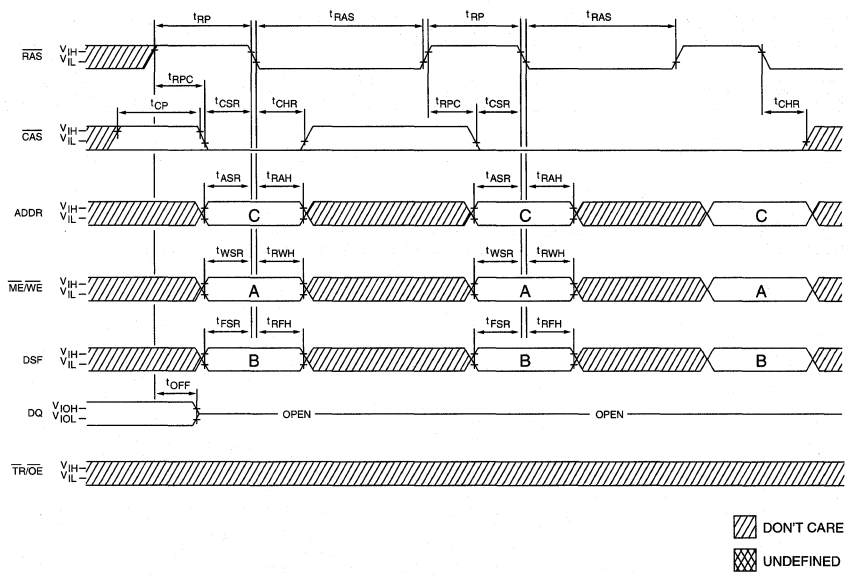


NEW VRAM

CBR CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		RAS Falling Edge (CAS = LOW)		
		A ME/WE	B DSF	C A0-A8
CBR REFRESH (Reset All Options)	CBRR	X	0	X
CBR REFRESH (Set/Reset Stop Address)	CBRS	0	1	STOP ADDRESS[1]
CBR REFRESH (No Reset)	CBRN	1	1	X

CBR REFRESH CYCLE [2]



NOTE: 1. Programmable Stop Point column addresses:

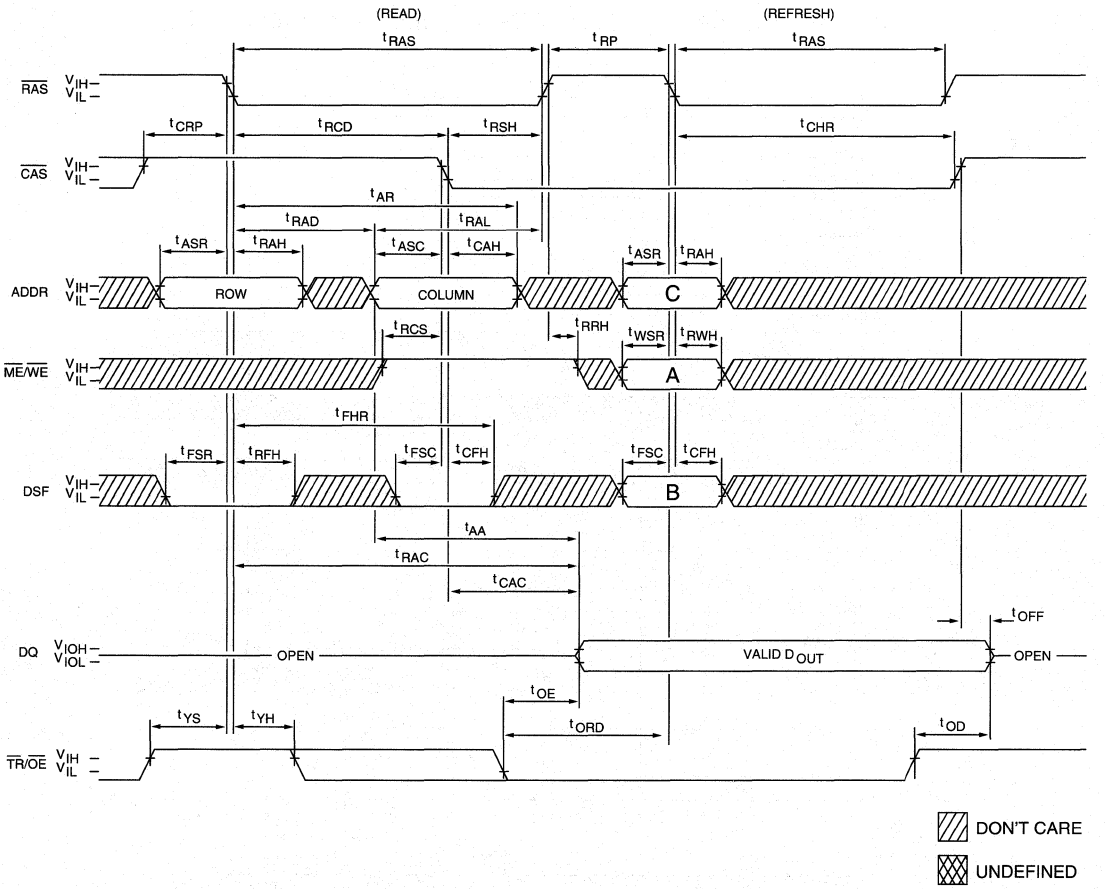
Number Stop Points/Half	Address @ RAS LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

NEW VRAM

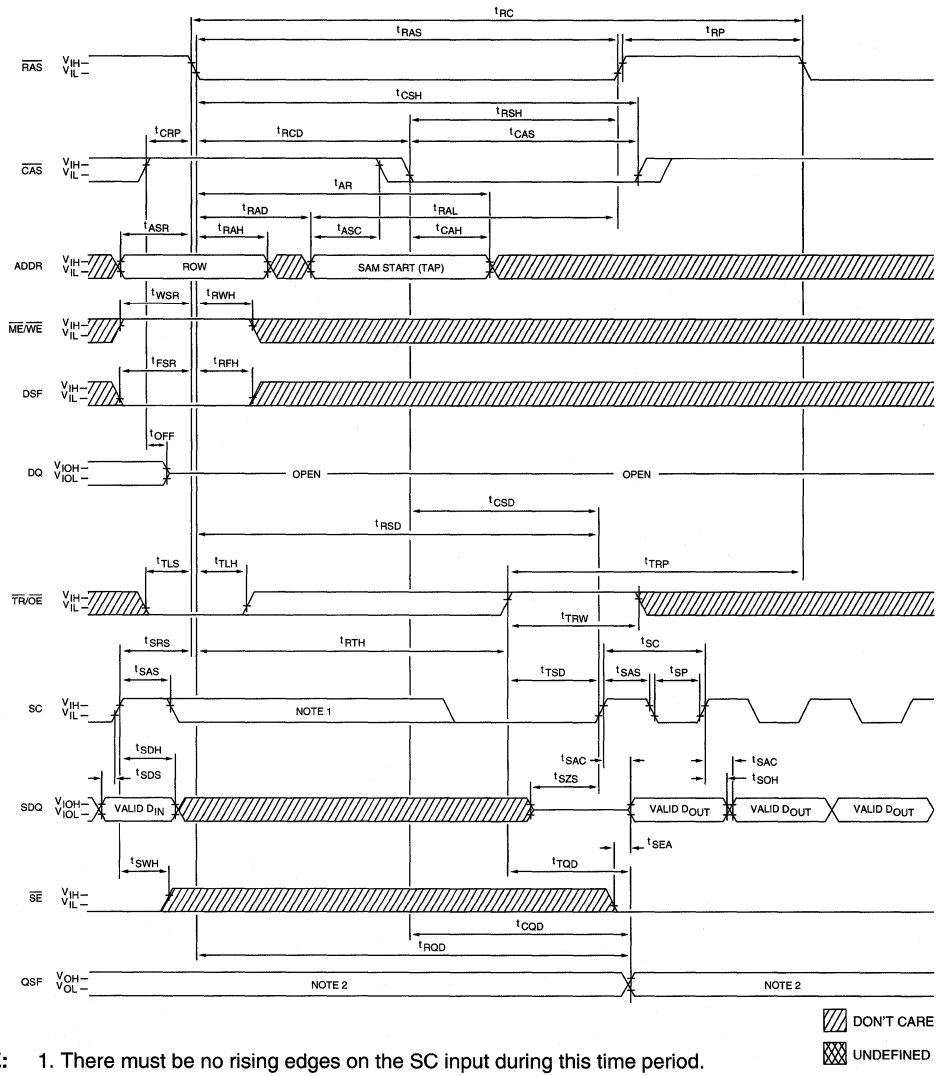
DRAM HIDDEN-REFRESH CYCLE [1, 2]



NOTE:
1. A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

NEW VRAM

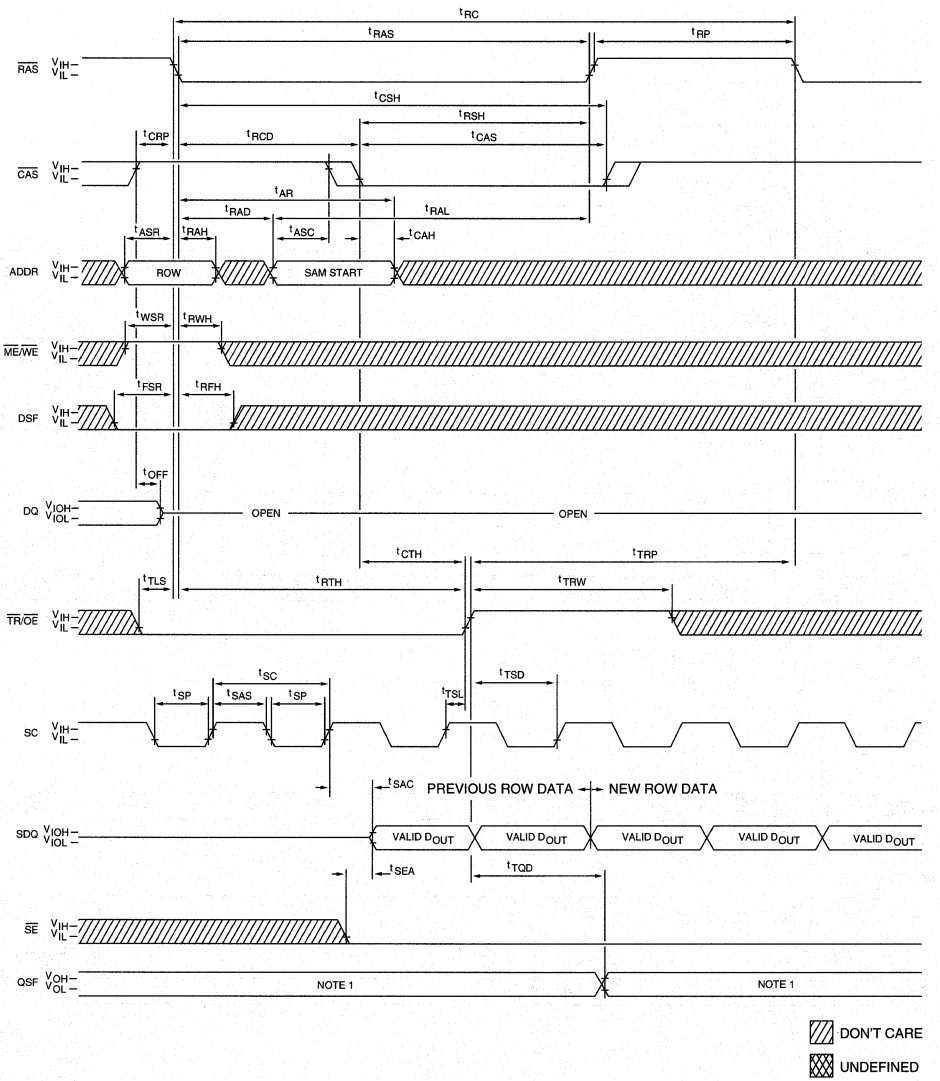
READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode, or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ^{t}TSD must be met.

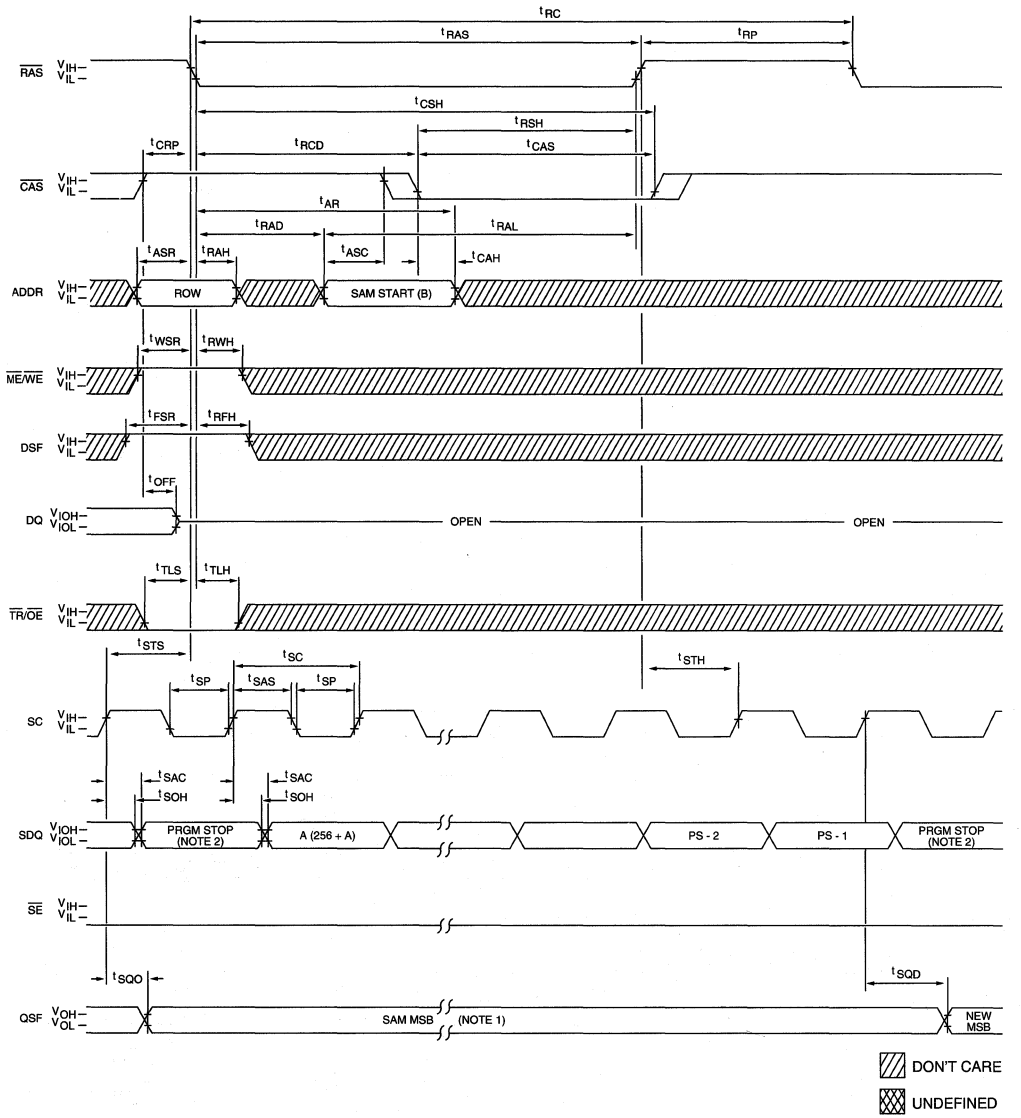
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



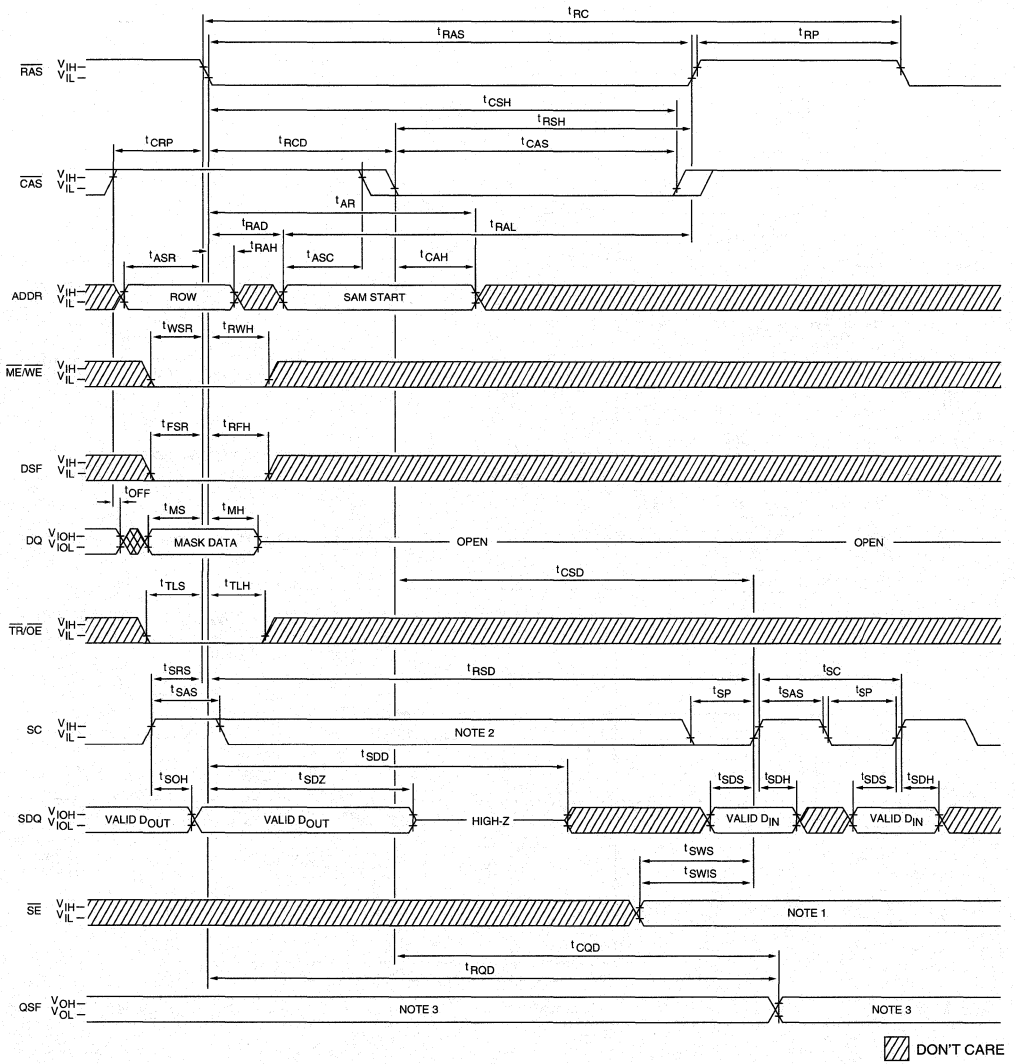
NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

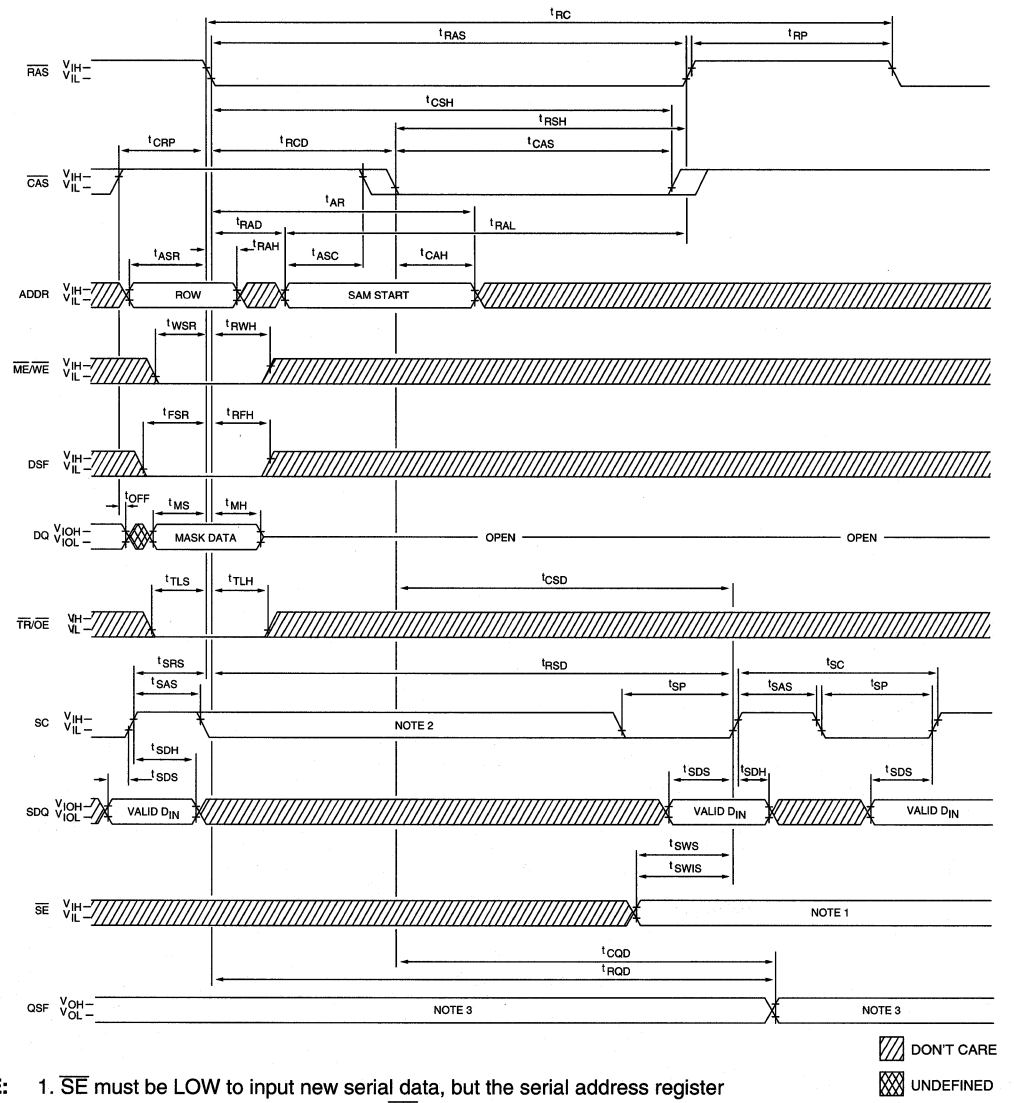
MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.

NEW VRAM

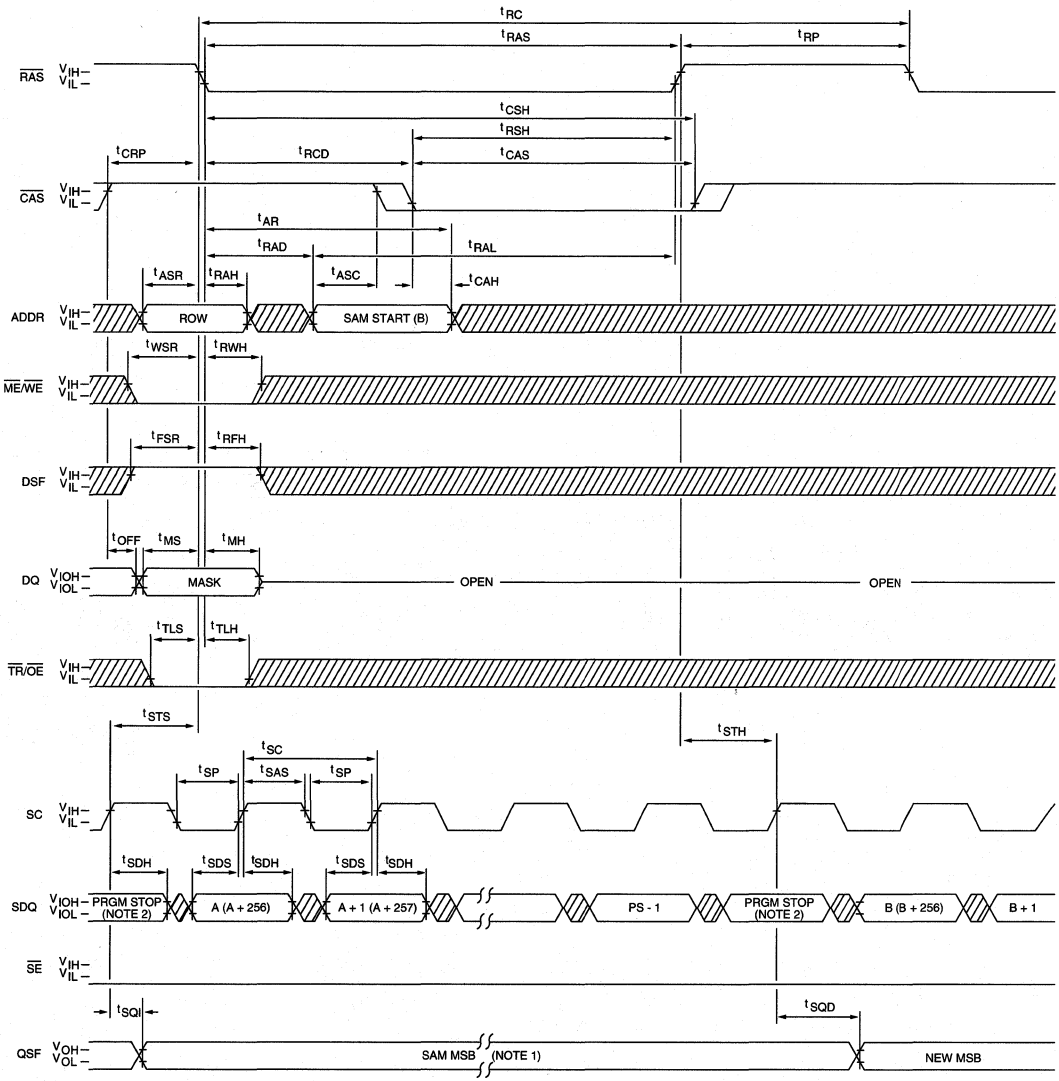
MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 255–511) is being accessed.

NEW VRAM

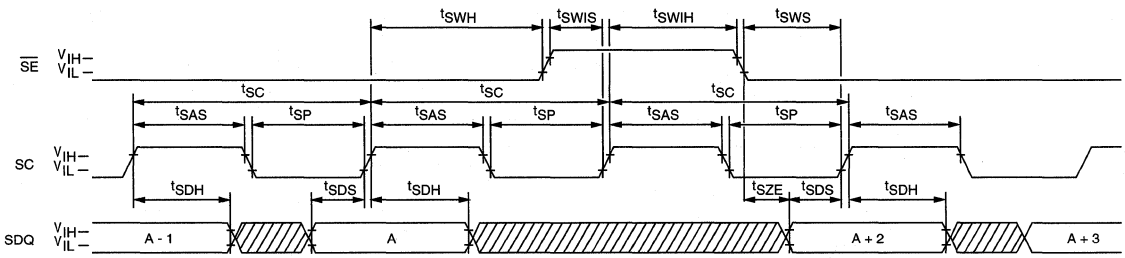
MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



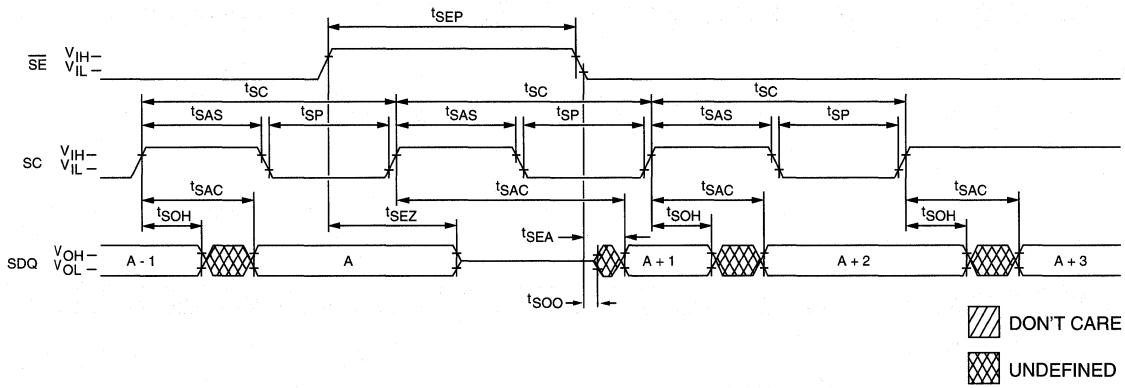
NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

NEW VRAM

SAM SERIAL INPUT



SAM SERIAL OUTPUT



MICRON SEMICONDUCTOR, INC.

MT42C256K16A1
256K x 16 VRAM

VRAM

256K x 16 DRAM WITH 512 x16 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
  (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE access with Extended Data-Out
- Upper and lower byte $\overline{WE}$ control
- Dual-port organization: 256K x 16 DRAM port
  512 x 16 SAM port
- No refresh required for serial access memory
- Fast access times: 70ns random, 17ns serial
  60ns random, 15ns serial*

SPECIAL FUNCTIONS

- JEDEC Basic Feature Set, plus:
- PERSISTENT MASKED WRITE
- EIGHT COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

OPTIONS MARKING

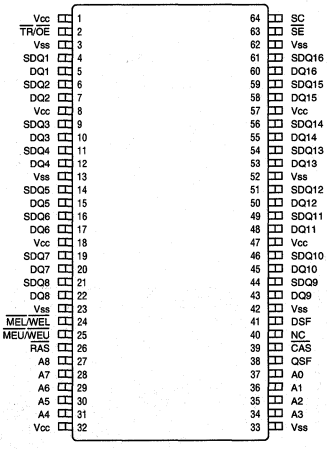
- Timing (DRAM, SAM [cycle/access])
  60ns, 18/15ns -6*
  70ns, 20/17ns -7
  80ns, 22/20ns -8
- Packages
  Plastic SOP (12 mm) SG
  Plastic TSOP (400 mil) TG*
- Part Number Example: MT42C256K16A1SG-7

GENERAL DESCRIPTION

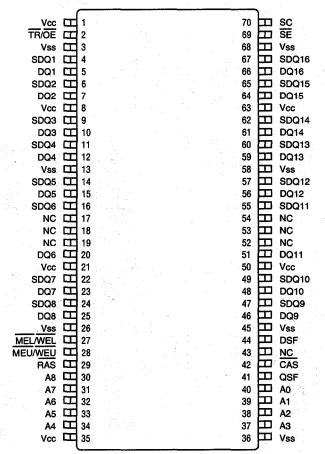
The MT42C256K16A1 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by a 16-bit-wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

PIN ASSIGNMENT (Top View)

64-Pin SOP (SDC-1)



70-Pin TSOP* (SDE-4)



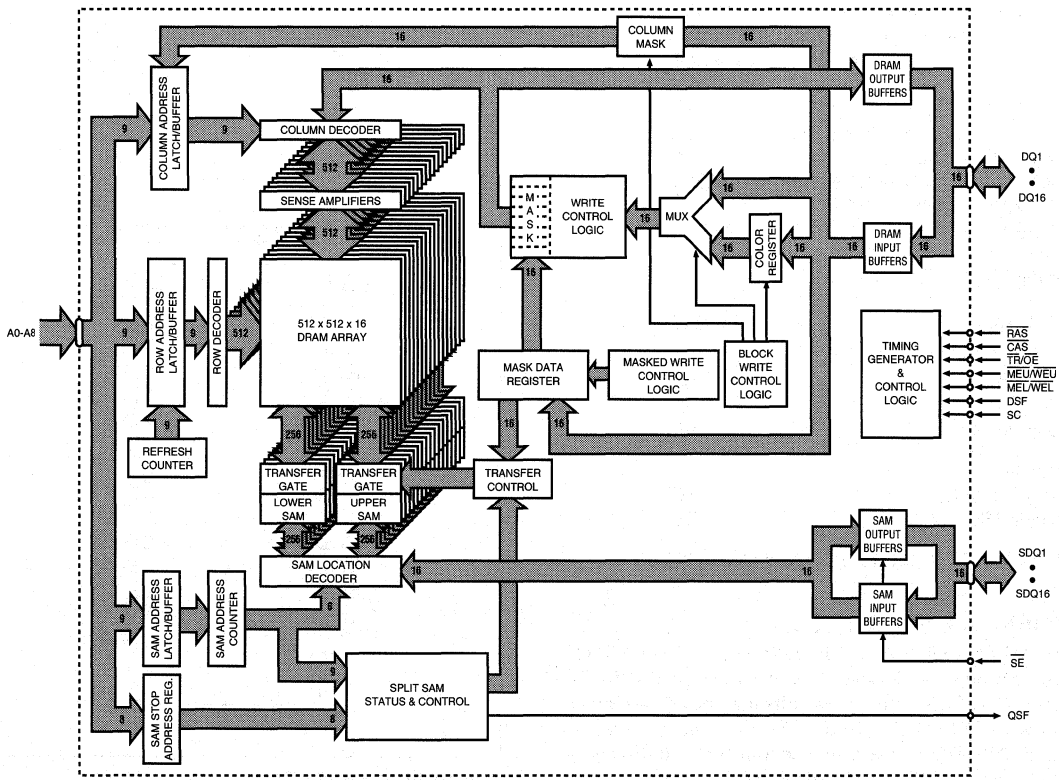
*Consult factory for availability.

The DRAM portion of the VRAM is similar to the MT4C16256 (256K x 16-bit DRAM), with the addition of BLOCK WRITE and FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512-bit-wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16A1 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, extended data-out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
64	70	SC	Input	Serial Clock: Clock input to the serial address counter and data latch for the SAM registers.
2	2	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
24,25	27,28	$\overline{MEL}$/$\overline{WEL}$, $\overline{MEU}$/$\overline{WEU}$	Input	Mask Enable: If $\overline{MEU}$/$\overline{WEU}$ or $\overline{MEL}$/$\overline{WEL}$ are LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{MEL,U}$/$\overline{WEL,U}$ are also used to select a READ or READ TRANSFER CYCLE ($\overline{MEL,U}$/$\overline{WEL,U}$ = H) or WRITE or WRITE TRANSFER CYCLE ($\overline{MEL,U}$/$\overline{WEL,U}$ = L). $\overline{MEL}$/$\overline{WEL}$ controls writes on DQ1-DQ8. $\overline{MEU}$/$\overline{WEU}$ controls writes on DQ9-DQ16.
63	69	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC, regardless of the state of $\overline{SE}$.
41	44	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, FLASH WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
26	29	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the nine row-address bits and strobe for $\overline{MEL,U}$/$\overline{WEL,U}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycles.
39	42	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the nine column-address bits and as a strobe for the DSF input.
37, 36, 35 34, 31, 30 29, 28, 27	40, 39, 38 37, 34, 33 32, 31, 30	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT TRANSFERs.
5,7,10,12, 15,17,20,22, 43,45,48,50, 53,55,58,60	5,7,10,12, 15,20,23,25, 46,48,51,56, 59,61,64,67	DQ1- DQ16	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Mask and Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
4,6,9,11,14,16 19,21,44,46,49 51,54,56,59,61	4,6,9,11,14,16 22,24,47,49,55 57,60,62,65,67	SDQ1- SDQ16	Input/ Output	Serial Data I/O: Input, output, or High-Z.
38	41	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
40	17,18,19,43, 52,53,54	NC	–	No Connects. SOP pin 40/ TSOP pin 43 should be tied LOW to allow for upward functional compatibility with future VRAM feature sets.
1,8,18,32,47,57	1,8,21,35,50,63	Vcc	Supply	Power Supply: +5V ±10%
3,13,23,33 42, 52, 62	3,13,26,36, 45,58,68	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C256K16A1 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C256K16A1 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C256K16A1 supports CBR, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CBR cycles within the 16.7ms time period. CBR cycles are also used to reset MASKED WRITE and PROGRAMMABLE SPLIT SAM operating modes. There are three CBR cycles defined for the MT42C256K16A1; CBR No Reset (CBRN), CBR Reset Stop Address (CBRS), and CBR Reset All Options (CBRR). To perform these functions, three additional pins are defined for CBR cycles, $\overline{MEL}/\overline{WEL}$, $\overline{MEU}/\overline{WEU}$ and DSF. These operations are described in detail in the MASKED WRITE and SPLIT READ/WRITE TRANSFER sections of the functional description.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C256K16A1 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES (RW)

The DRAM portion of the VRAM is similar to standard 256K x 16 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 16-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{MEL}/\overline{WEL}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles or resets will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are HIGH when $\overline{CAS}$ goes LOW and remain HIGH until $\overline{CAS}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ16 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ perform two functions; write mask enable and data write enable. $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If either $\overline{MEL}/\overline{WEL}$ or $\overline{MEU}/\overline{WEU}$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If either $\overline{MEL}/\overline{WEL}$ or $\overline{MEU}/\overline{WEU}$ is

LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed. If either MEL/WEL or MEU/WEU goes LOW after CAS go LOW, a DRAM LATE WRITE operation is performed (refer to the AC timing diagrams).

The BYTE WRITE signals MEU/WEU and MEL/WEL are used together to perform a write mask enable and separately for data write enable. For write maske enables, the WE function is determined by the first BYTE WRITE signal to transition LOW and the last to transition HIGH. Using one for data writes performs a BYTE WRITE; using both performs a WORD WRITE.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ (with Extended Data Out), FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE- MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

EXTENDED DATA OUTPUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. The MT42C256K16A1 offers an accelerated FAST PAGE MODE (FPM) cycle by eliminating output disable from CAS HIGH. This option is called Extended Data Out, and it allows CAS precharge time (^{t}CP) to occur without the output data going invalid (see DRAM READ and DRAM FAST-PAGE-MODE READ waveforms).

Extended Data Out operates as any DRAM READ or FPM READ, except data will be held valid after CAS goes HIGH, as long as (TR)/OE and RAS are LOW. If the DQ outputs from multiple banks are wired together, (TR)/OE must be used in conjunction with CAS to select and deselect the appropriate banks. During non-PAGE-MODE READ cycles, the outputs are disabled at ^{t}OFF time after RAS and CAS are HIGH. The ^{t}OFF time is referenced from the rising edge of RAS or CAS, whichever occurs later.

MASKED WRITE (RWM)

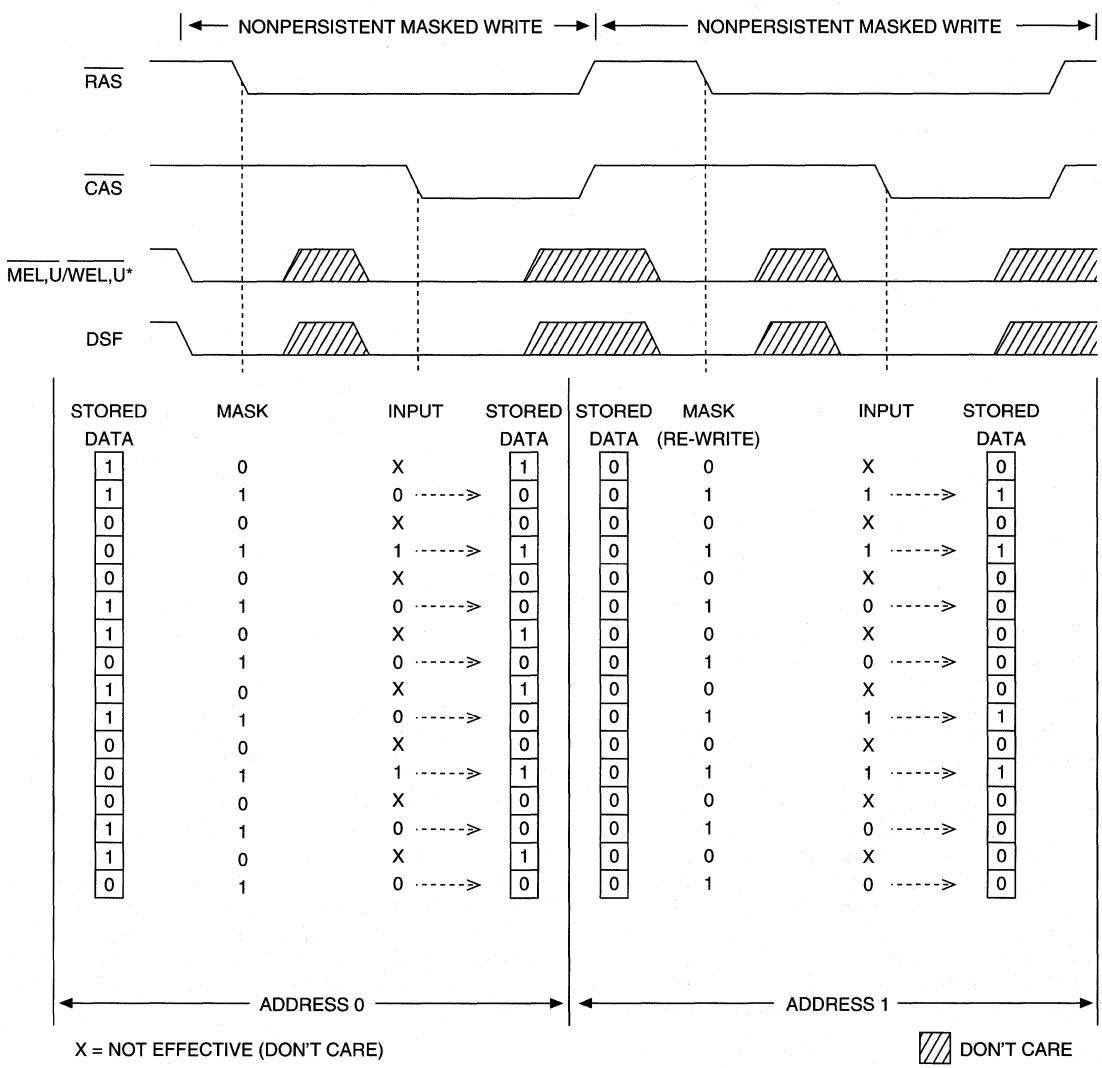
The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing individual bits within the 16-bit word. The MT42C256K16A1 supports two types of MASKED WRITE cycles, nonpersistent MASKED WRITE and persistent MASKED WRITE. When DSF and either MEL/WEL or MEU/WEU are LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C256K16A1 initializes in the nonpersistent mode. In this mode, mask data must be entered with every RAS falling edge. The data (mask data) present on the DQ1-DQ16 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the sixteen DQ1-DQ16 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that CAS is still HIGH. When CAS goes LOW, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle.

The selection of persistent or nonpersistent MASKED WRITE is done by performing a LOAD MASK REGISTER (LMR) cycle (see LMR description). If an LMR is done, all ensuing MASKED WRITEs are persistent and the mask data will be provided by the Mask Data Register (see Figure 2). The mask data is applied in the same manner as in nonpersistent mode.

To reset the device back to the nonpersistent mode, a CBR, Reset All Options (CBRR) cycle must be performed. This cycle is defined as a CBR with DSF LOW when RAS falls, MEL,U/WEL,U are "don't care." To preserve the persistent mode of MASKED WRITE, while using CBR REFRESH, a CBRN cycle is used. This cycle will perform a refresh of the internally addressed row of DRAM but will not reset the MASKED WRITE mode.

FAST-PAGE-MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE RAS cycle.

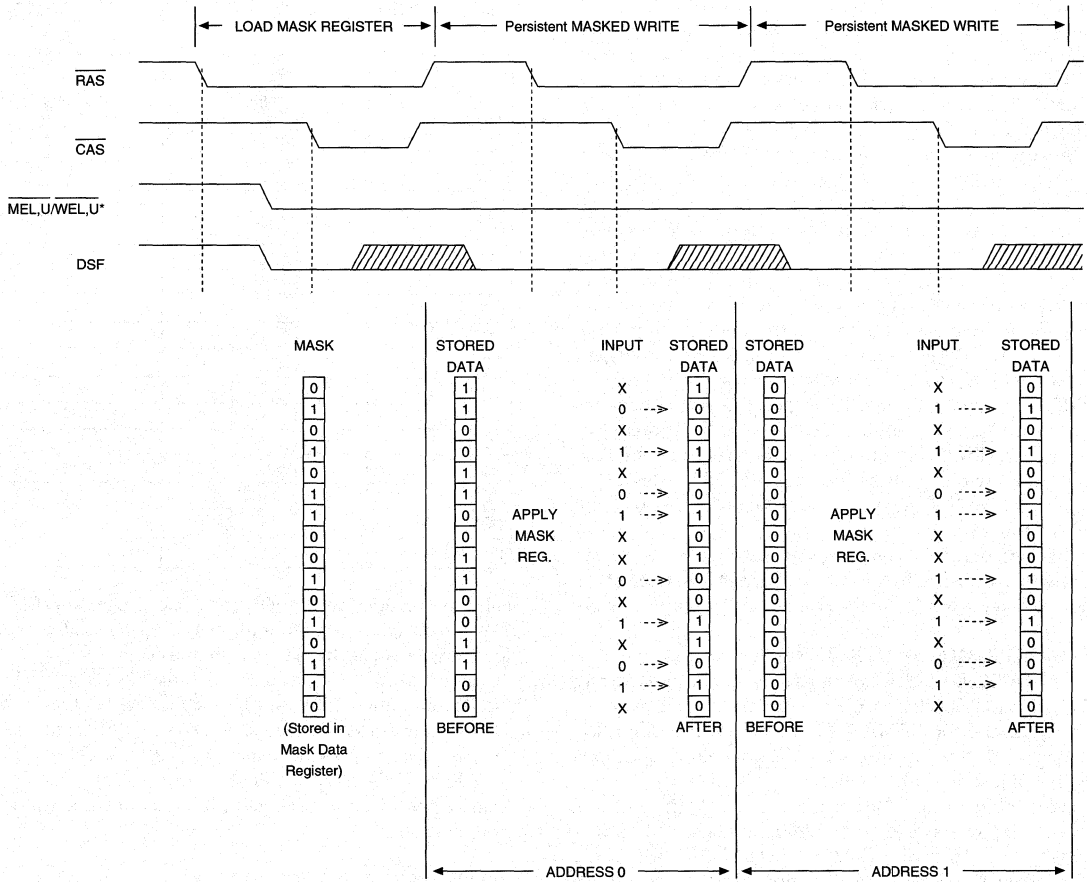


STORED DATA	MASK	INPUT	STORED DATA
1	0	X	1
1	1	0	0
0	0	X	0
0	1	1	1
0	0	X	0
1	1	0	0
1	0	X	1
0	1	0	0
1	0	X	1
1	1	0	0
0	0	X	1
0	1	1	1
0	0	X	0
1	1	0	0
1	0	X	1
0	1	0	0

STORED DATA	MASK (RE-WRITE)	INPUT	STORED DATA
0	0	X	0
0	1	1	1
0	0	X	0
0	1	1	1
0	0	X	0
0	1	0	0
0	0	X	0
0	1	0	0
0	0	X	0
0	1	1	1
0	0	X	0
0	1	1	1
0	0	X	0
0	1	0	0
0	0	X	0
0	1	0	0

* One or two write enables are active, depending upon whether a BYTE or WORD MASKED WRITE is to be performed.

Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE



X = NOT EFFECTIVE (DON'T CARE)

* One or two write enables are active, depending upon whether a BYTE or WORD MASKED WRITE is to be performed.

Figure 2
PERSISTENT MASKED WRITE EXAMPLE

BLOCK WRITE (BW)

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C256K16A1 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to eight adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A3-A8 inputs are used. A3-A8 specify the "block" of eight adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the eight column locations will be changed. Two separate 8-bit column masks are provided on the DQ inputs, one for the lower byte portion (DQ1-8) of the block, and one for the upper byte portion (DQ9-16). The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{MEL,U}/\overline{WEL,U}$, whichever occurs later (see the WRITE cycle waveforms). Table 1 on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column/byte locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the enabled column/byte locations; each DQ location of the color register is written to the corresponding DQ bit plane.

MASKED BLOCK WRITE (BWM)

The MASKED WRITE functions may also be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 16 bit-planes of eight column locations instead of just one column location.

The combination of DSF and either $\overline{MEL}/\overline{WEL}$ or $\overline{MEU}/\overline{WEU}$ LOW when $\overline{RAS}$ goes LOW initiates a MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the sixteen bit planes may be masked, along with any combination of the eight column locations for each byte portion of the block.

The MASKED BLOCK WRITE will be nonpersistent (new mask) at device power-up. To enter persistent mode (old mask) a LOAD MASK REGISTER cycle is performed. All MASKED BLOCK WRITEs will be persistent after the LMR. To reset to nonpersistent mode, a CBRR (reset all) cycle must be performed.

MASKED FLASH WRITE (FWM)

The MASKED FLASH WRITE cycle is similar to the MASKED BLOCK WRITE cycle in that it uses the color register to accelerate the writing of a select color to the DRAM memory array. Instead of writing to eight adjacent column locations in one DRAM cycle (BLOCK WRITE), FWM writes the contents of the color register to all column locations on an addressed row in one cycle.

The FWM cycle is selected by taking $\overline{TR}/(\overline{OE})$ and DSF HIGH and either $\overline{MEL}/\overline{WEL}$ or $\overline{MEU}/\overline{WEU}$ LOW at the falling edge of $\overline{RAS}$. DSF is "don't care" at the falling edge of $\overline{CAS}$. The DQ plane mask applies as it does for all MASKED WRITE cycles; if the mask register has been loaded, the mask is persistent; if it has not, the mask is nonpersistent.

Table 1
DQ Masking of Columns (at $\overline{CAS}$ falling)

DQ INPUTS	COLUMN ADDRESS CONTROLLED			DQ PLANES CONTROLLED
	A2	A1	A0	
DQ1	0	0	0	1-8
DQ2	0	0	1	1-8
DQ3	0	1	0	1-8
DQ4	0	1	1	1-8
DQ5	1	0	0	1-8
DQ6	1	0	1	1-8
DQ7	1	1	0	1-8
DQ8	1	1	1	1-8
DQ9	0	0	0	9-16
DQ10	0	0	1	9-16
DQ11	0	1	0	9-16
DQ12	0	1	1	9-16
DQ13	1	0	0	9-16
DQ14	1	0	1	9-16
DQ15	1	1	0	9-16
DQ16	1	1	1	9-16

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation loads the data present on the DQ pins into the 16-bit mask data register at the falling edge of $\overline{CAS}$ or $(\overline{MEL,U})/\overline{WEL,U}$. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{MEL}/\overline{WEL}$, $\overline{MEU}/\overline{WEU}$ and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle.

Note: *LOAD MASK REGISTER cycles also enable the persistent MASKED WRITE mode. All ensuing MASKED WRITEs (including MASKED WRITE and MASKED SPLIT WRITE TRANSFER) will be masked with data from the mask register. A CBRR is required to reset back to nonpersistent mode.*

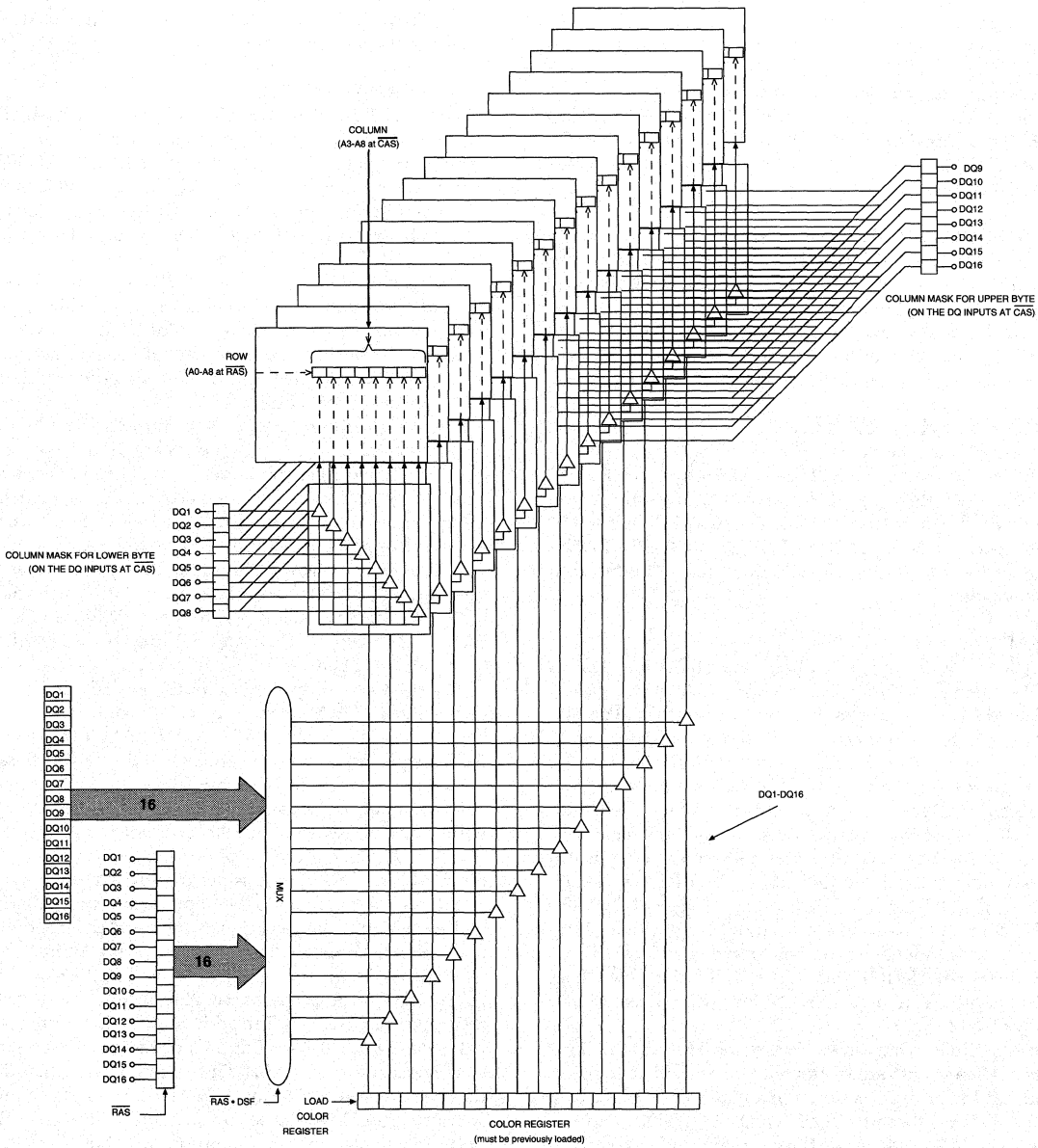


Figure 3
BLOCK WRITE EXAMPLE

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

During persistent operation, the mask data register contents are used for MASKED WRITE, MASKED BLOCK WRITE, MASKED FLASH WRITE, MASKED WRITE TRANSFER and SPLIT WRITE TRANSFER cycles to selectively enable writes to the sixteen DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 16-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE and FLASH WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{MEL},\overline{U})/\overline{WEL},\overline{U}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER (RT)

If $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row-address bits indicate which sixteen 512-bit DRAM row planes are transferred to the sixteen SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 8,192 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

SPLIT READ TRANSFER

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and is not synchronized with the serial clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles. An SRT does not change the direction of the SAM I/O port.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF), and to set SAM I/O direction. Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is $\neq 0$. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7=1), the QSF output goes HIGH; if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 5).

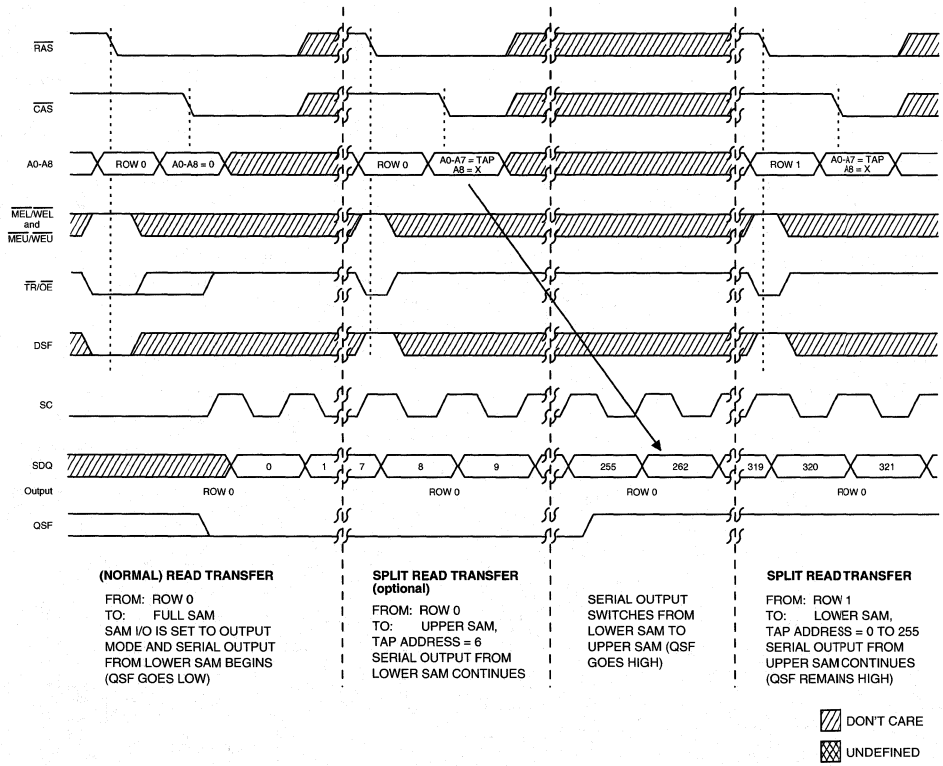


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

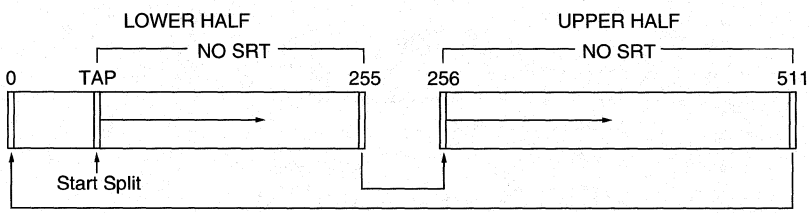


Figure 5
SPLIT SAM TRANSFER

The stop address of the SAM half (the point at which access will change to the next half) is programmable on the MT42C256K16A1. This function is described in the PROGRAMMABLE SPLIT SAM section of the Functional Description.

MASKED WRITE TRANSFER (MWT)

The operation of the MASKED WRITE TRANSFER (MWT) is identical to that of the READ TRANSFER described previously except either $\overline{MEL}$/$\overline{WEL}$ or $\overline{MEU}$/$\overline{WEU}$ is LOW and a DQ plane mask is applied when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A DQ mask must be applied to all MWTs as shown in Figure 6. This may be done using persistent or nonpersistent modes. When using persistent mode, the mask will be supplied by the mask register. When in nonpersistent mode, the DQ pins are used to input a bit plane mask at the falling edge of $\overline{RAS}$. An MWT changes the direction of the SAM I/O buffers to the input mode. To change the SAM I/O buffers to input mode without SAM data being transferred to the DRAM, a mask of all 0's must be presented on the DQ pins when $\overline{RAS}$ falls. QSF is LOW if serial input is to the lower half of the SAM, and HIGH if it is to the upper half.

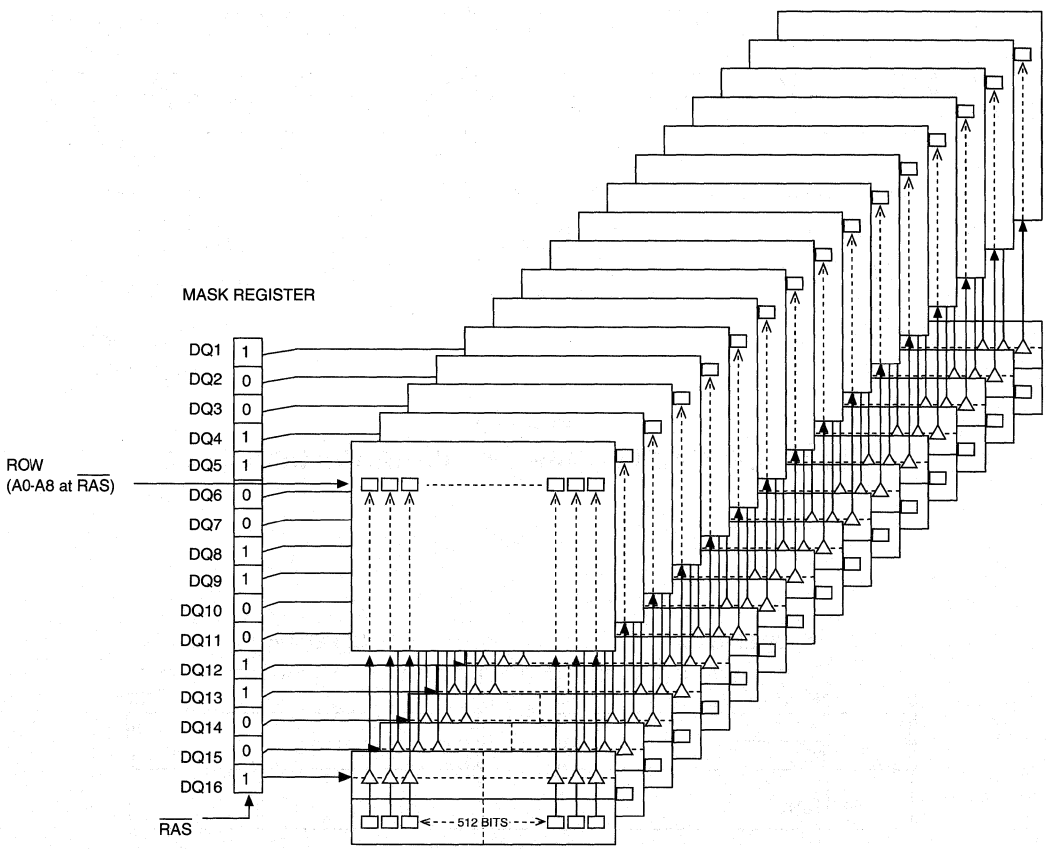


Figure 6
DQ MASKED WRITE TRANSFER

MASKED SPLIT WRITE TRANSFER (MSWT)

The MASKED SPLIT WRITE TRANSFER (MSWT) cycle allows serial input data to be transferred to the DRAM without interrupting the serial clock. Operation of the SWT cycle is very similar to the SPLIT READ TRANSFER cycle. It will transfer the idle half of the SAM to the DRAM and set the Tap address to where the new serial data will be loaded in that half. Selection of the MSWT cycle is the same as that of the MASKED WRITE TRANSFER with the exception of the state of DSF. When DSF is HIGH at the falling edge of $\overline{RAS}$, an MSWT will occur. The initiation sequence for MSWT is shown in Figure 7. An MSWT will not change the direction of the SAM I/O buffers.

PROGRAMMABLE SPLIT SAM

Programmable split SAM operation is an extension of the split SAM mode. This mode optimizes SAM performance by allowing user-programmable stop points to be defined in the split SAM. The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the loaded Tap address). The locations of the stop points are programmable in power-of-two increments. The stop points and size of the resulting partitions are shown in Figure 8, along with an example.

The stop points are set by performing a CBR (Reset Stop Addrs) cycle (CBRS). A CBRS cycle is a CBR with either $\overline{MEL}/\overline{WEL}$ or $\overline{MEU}/\overline{WEU}$ LOW and DSF HIGH at the

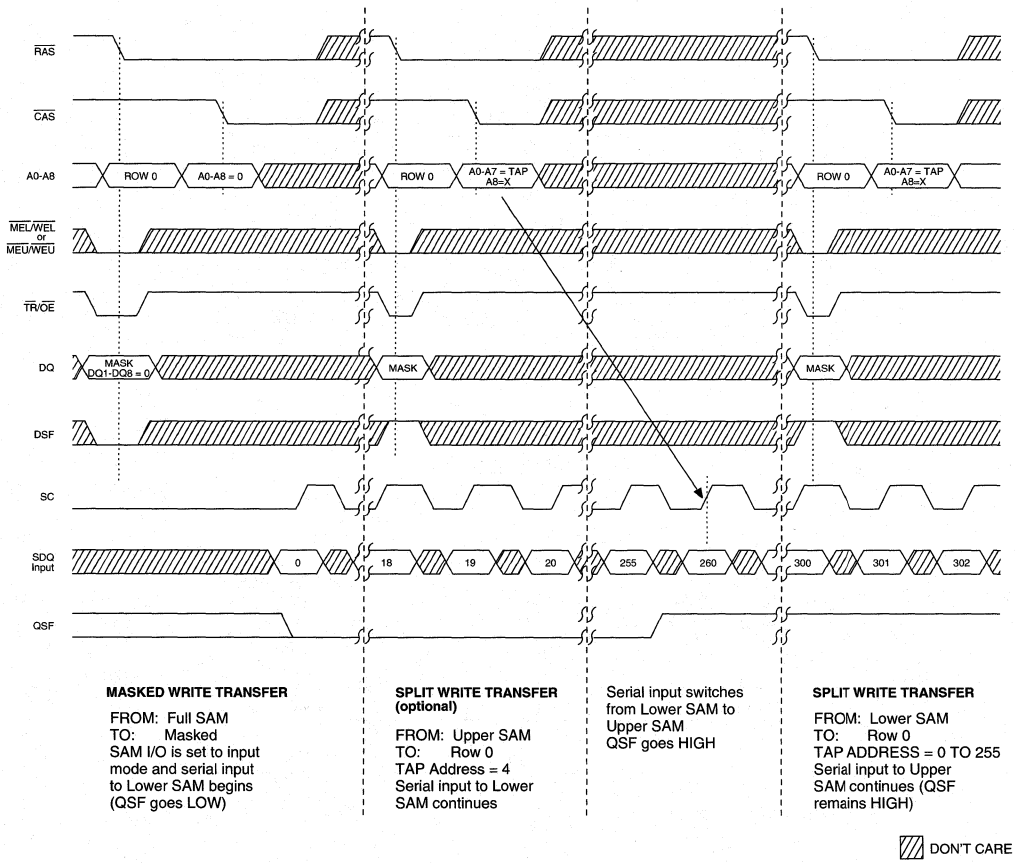


Figure 7
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

$\overline{RAS}$ HIGH-to-LOW transition. This is a special CBR refresh cycle that, in addition to refreshing the DRAM, will sample the address pins (A4-A8) and set the stop point partition to the addressed value (See Figure 8). The programmable stop points will not become valid until a SPLIT TRANSFER (READ or WRITE) is done, following the CBRS. Both halves of the SAM will be programmed simultaneously to the same partition lengths and stop points.

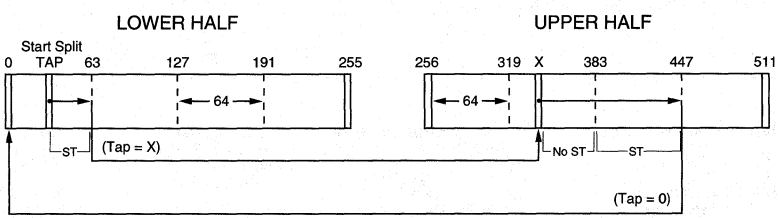
Access will progress from the Tap address to the end of the programmable partition into which the Tap fell. When the end of the "addressed" partition is reached, the access will jump to the Tap address of the next half, provided that a SPLIT TRANSFER (READ or WRITE) was done before the partition boundary was reached. If a SPLIT TRANSFER (ST) is not done prior to the terminal count of the partition, the partition is not recognized and the address count will continue in the same half (this is shown Figure 8 at stop address 383). The count will continue in the same half until a SPLIT TRANSFER (READ or WRITE) occurs or the SAM half boundary is reached. In Figure 8, an ST occurs some time between addresses 383 and 447 and the boundary is recognized at 447. The programmable stop points may be reprogrammed at any time by performing another CBRS cycle, the new stop points will not be valid until an ST is performed.

Disabling the programmable split SAM requires a CBRR. This is a CBR cycle with DSF LOW at the $\overline{RAS}$ HIGH-to-LOW transition. The CBRR will take effect immediately; it does not require an ST to become active valid.

Number Stop Points/Half	Address @ $\overline{RAS}$ LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

EXAMPLE
(4 stop points)



Programmed Partition (A4-A8) = 000111111
MSB....LSB

Figure 8
PROGRAMMABLE SPLIT SAM OPERATION

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 16-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 16-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = ($\overline{TR}$)/$\overline{OE}$ ≥ V_{IH} during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data, and the nonpersistent MASKED WRITE mode is enabled.

The SAM portion of the MT42C256K16A1 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (MASKED WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The mask and color register will contain random data after power-up.

VRAM

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE[8]	DSF	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS											
CBRR	CBR REFRESH (RESET ALL OPTIONS)	0	X	X	0	—	X	X	—	X	X	X
CBRS	CBR REFRESH (RESET STOP ADDRESS)	0	X	0	1	—	STOP[7]	X	—	X	X	X
CBRN	CBR REFRESH (NO RESET)	0	X	1	1	—	X	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X	X
RWM	MASKED WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK[4]	VALID DATA	USE[4]	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A3-A8)	X	COLUMN MASK	X	USE
BWM	MASKED BLOCK WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	1	ROW	COLUMN (A3-A8)	WRITE MASK[4]	COLUMN MASK	USE[4]	USE
FWM	MASKED FLASH WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	1	X	ROW	X	WRITE MASK[4]	X	USE[4]	USE
	REGISTER OPERATIONS											
LMR	LOAD MASK REGISTER	1	1	1	1	0	ROW[5]	X	X	REG DATA	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[5]	X	X	REG DATA	X	LOAD
	TRANSFER OPERATIONS											
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[6]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[6]	X	X	X	X
MWT	MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	0	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X
MSWT	MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NEW OR OLD MASK)	1	0	0	1	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X

NOTE:

1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ16 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or MEL,U/WEL,U, whichever is later. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. After an LMR cycle, all masked WRITEs use the mask register (old mask). Data on the DQs at RAS falling edge will be ignored. A CBRR will reset to new mask state and mask data must be presented on the DQs at every RAS falling edge.
5. The ROW that is addressed will be refreshed, but a ROW address is not required.
6. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half or Programmable Stop Address boundary).
7. Defines the column addresses where access moves to the next half, see Programmable Split SAM functional description.
8. ME/WE = 1 if both MEL/WEL and MEU/WEU are HIGH at the falling edge of RAS. ME/WE = 0 if either or both of those signals is LOW at that time.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{MEL,U}$/$\overline{WEL,U}$, $\overline{TR/OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

VRAM

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	180	170	160	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC2}	130	120	110	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	180	170	160	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	180	170	160	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	180	170	160	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	220	210	195	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC8}	170	160	145	mA	3, 4, 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after eight $\overline{RAS}$ cycles [MIN])	I_{CC9}	50	50	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	220	210	195	mA	3, 4, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	220	210	195	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	220	210	195	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	^tRWC	150		175		195		ns	
FAST-PAGE-MODE READ or EARLY WRITE cycle time (Extended Data-Out (READ))	^tPC	24		27		30		ns	
FAST-PAGE-MODE LATE WRITE, MASKED WRITE or BLOCK WRITE cycle time.	^tPC	30		35		40		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	85		90		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		18		20	ns	11,15
Access time from $\overline{(TR)}/\overline{OE}$	^tOE		15		20		20	ns	
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		18		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width (FAST-PAGE-MODE, READ or EARLY WRITE cycles only)	^tCAS	10	100,000	10	100,000	12	100,000	ns	
$\overline{CAS}$ pulse width (All other cycles)	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	52	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	12		12		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	
$\overline{CAS}$ HIGH to $\overline{RAS}$ HIGH lead time	^tCRL	0		0		0		ns	
$\overline{RAS}$ HIGH to $\overline{CAS}$ HIGH lead time	^tRCL	0		0		0		ns	

*Consult factory for availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	^tOFF	3	20	3	20	3	20	ns	20, 23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	^tOD	3	15	3	15	3	15	ns	20, 23
Output enable delay from ($\overline{TR}$)/$\overline{OE}$	^tOELZ	3		3		3		ns	
($\overline{TR}$)/$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	10		10		10		ns	
($\overline{TR}$)/$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	
Output disable delay from ($\overline{ME}$)/$\overline{WE}$	^tWHZ	3	10	3	10	3	10	ns	
Output disable hold time from start of WRITE	^tOEH	10		10		10		ns	27
Output Enable to $\overline{RAS}$ delay	^tORD	0		0		0		ns	
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		5		ns	11
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	12		12		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	18		18		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	18		18		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	12		12		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		43		45		ns	21
Transition time (rise or fall)	^tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	

*Consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	60	10,000	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	15		20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		50		50		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	15		20		25		ns	
$\overline{TR}/(\overline{OE})$ LOW to last SC hold time	^tTSL	5		5		5		ns	28
$\overline{TR}/(\overline{OE})$ HIGH to first SC setup time	^tTSD	50		50		50		ns	28
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	^tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode Enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode Enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		15		ns	
SC to QSF delay time	^tSQD		20		25		30	ns	
SPLIT TRANSFER setup time	^tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	^tSTH	10		10		10		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	45		55		60		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		30		30		30	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		70		75		75	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	^tRSD	95		105		115		ns	
$\overline{CAS}$ to first SC delay	^tCSD	50		55		55		ns	

*Consult factory for availability.

VRAM

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

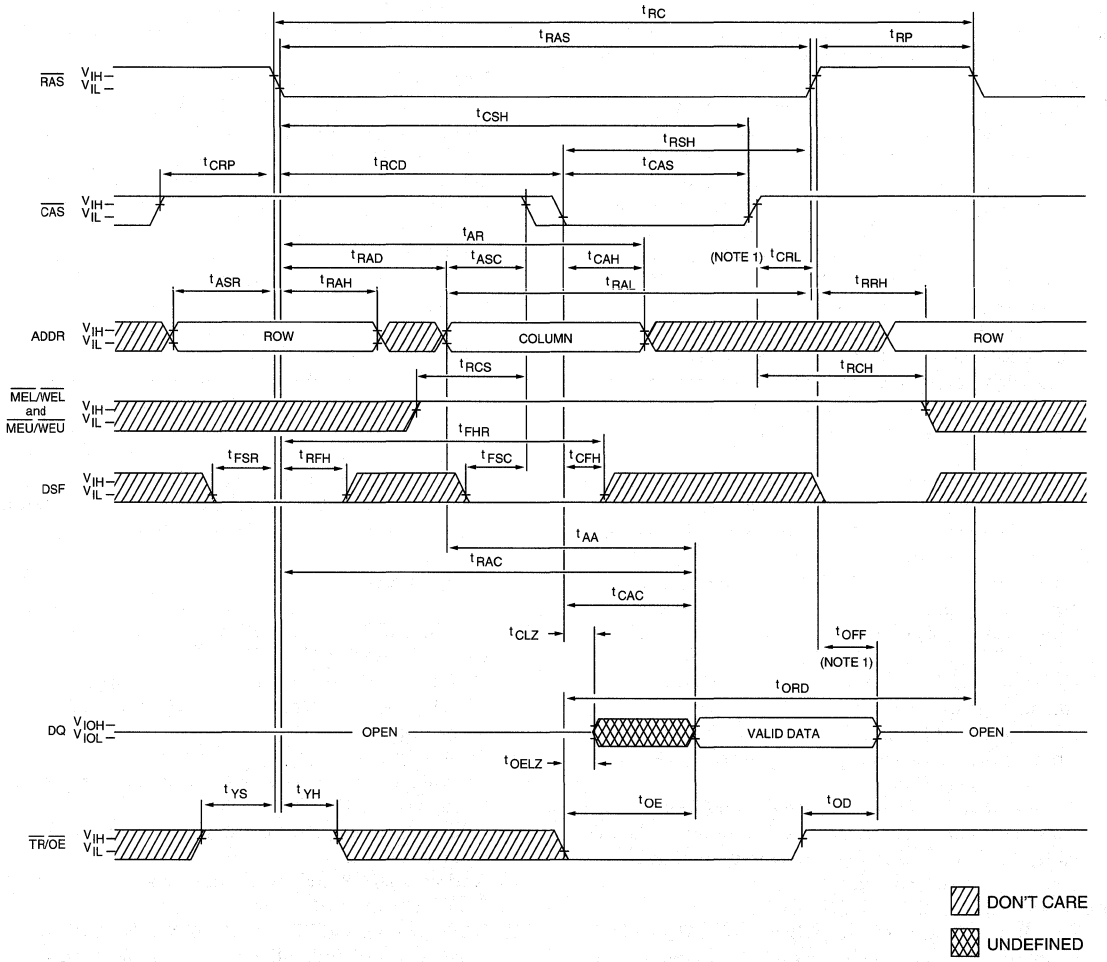
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	18		20		22		ns	
Access time from SC	^tSAC		15		17		20	ns	11,24
SC precharge time (SC LOW time)	^tSP	7		8		9		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		9		ns	
Access time from $\overline{SE}$	^tSEA		12		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		9		ns	
Serial data-out hold time after SC high	^tSOH	3		3		3		ns	11,24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial output buffer turn-on delay from $\overline{SE}$	^tSOO	3		3		3		ns	
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	3		3		3		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	3		3		3		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

*Consult factory for availability.

NOTES

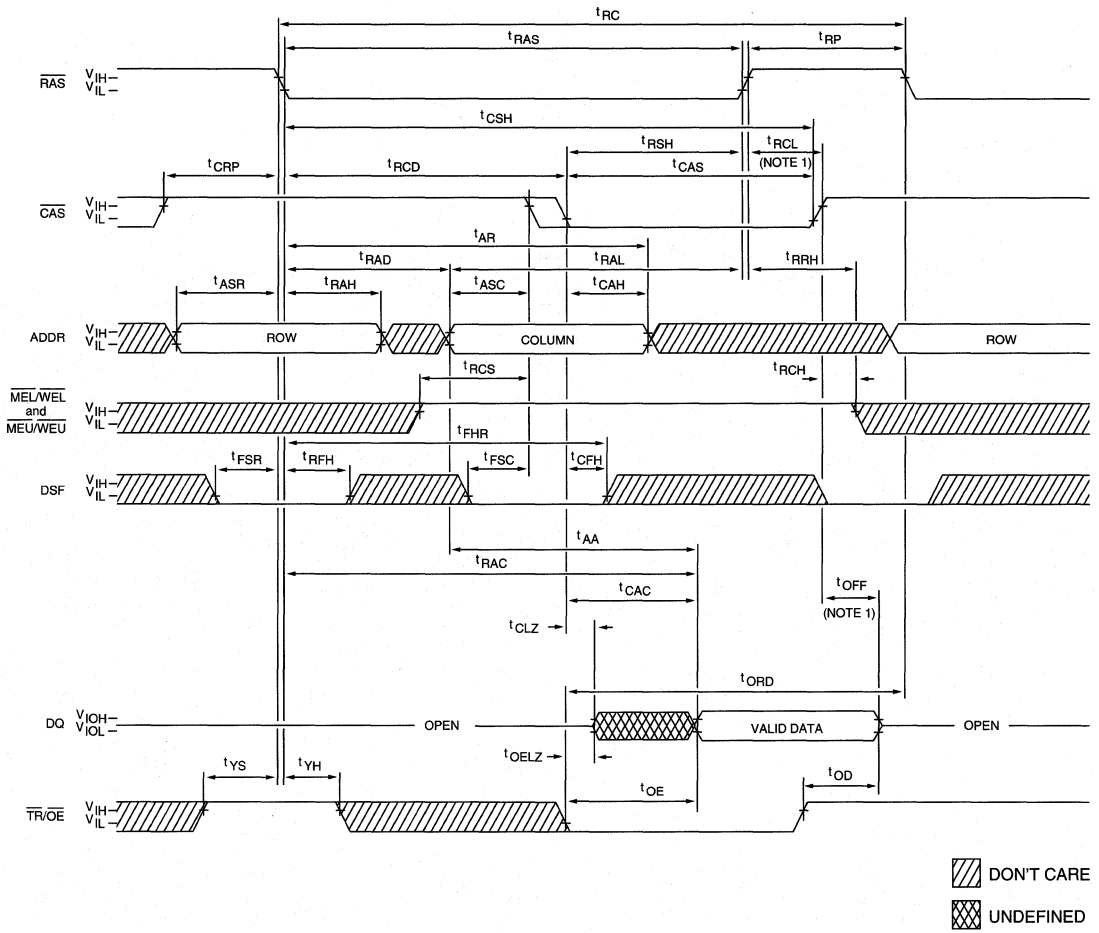
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. $^tSAC/^tCAC$ are MAX at 70° C and 4.5V Vcc; $^tSOH/^tCOH$ are MIN at 0° C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. This is guaranteed by design ($^tSOH/^tCOH = ^tSAC/^tCAC$ - output transition time).
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ16) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gates and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until ^tOD is met) is indeterminate, but the WRITE will be valid if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{MEL}, \overline{U}/\overline{WEL}, \overline{U}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ HIGH or when $\overline{RAS}$ and $\overline{CAS}$ go HIGH, whichever occurs first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ and $\overline{RAS}$ go HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The "last" SC edge causes the last data from the previous row to appear on the SDQ pins. The "first" SC, the first data from the new row.

DRAM READ CYCLE [1]
(Outputs controlled by $\overline{RAS}$)



NOTE: 1. ^{t}CRL is a reference parameter. If $\overline{CAS}$ = HIGH ^{t}CRL before $\overline{RAS}$, ^{t}OFF is referenced from the rising edge of $\overline{RAS}$.

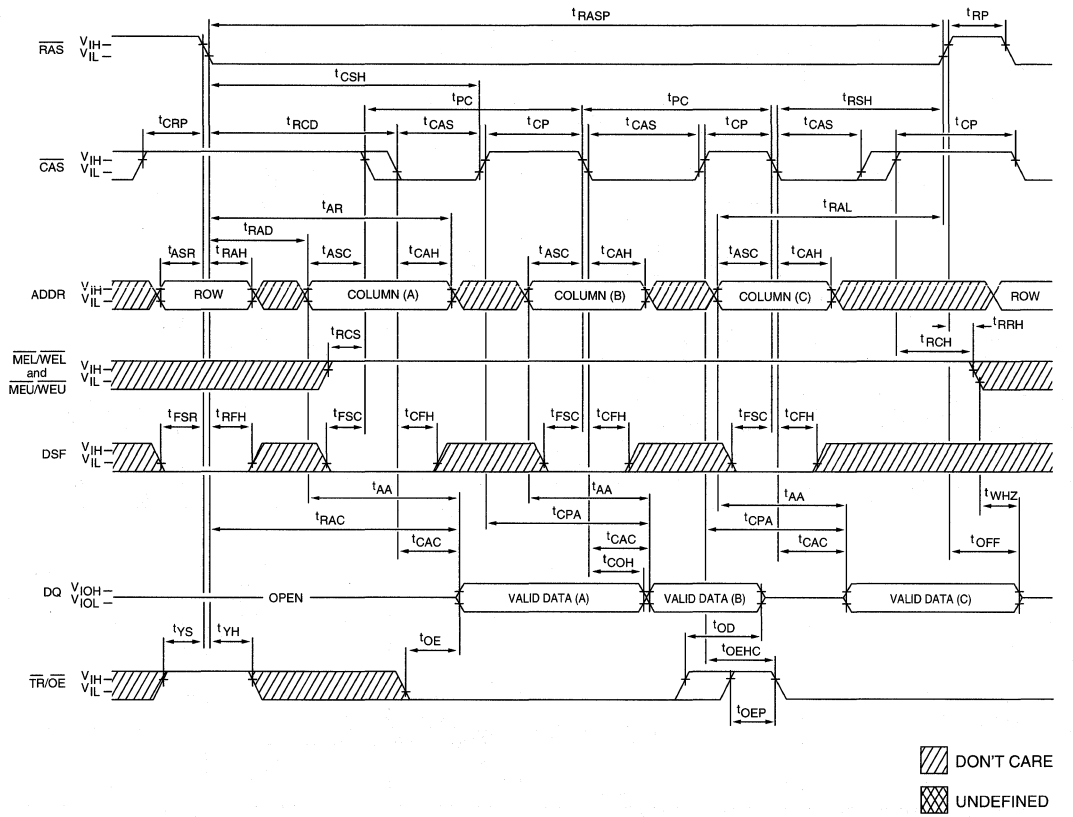
DRAM READ CYCLE [1]
(Outputs controlled by $\overline{CAS}$)



NOTE: 1. ^{t}RCL is a reference parameter. If $\overline{RAS}$ = HIGH ^{t}RCL before $\overline{CAS}$, ^{t}OFF is referenced from the rising edge of $\overline{CAS}$.

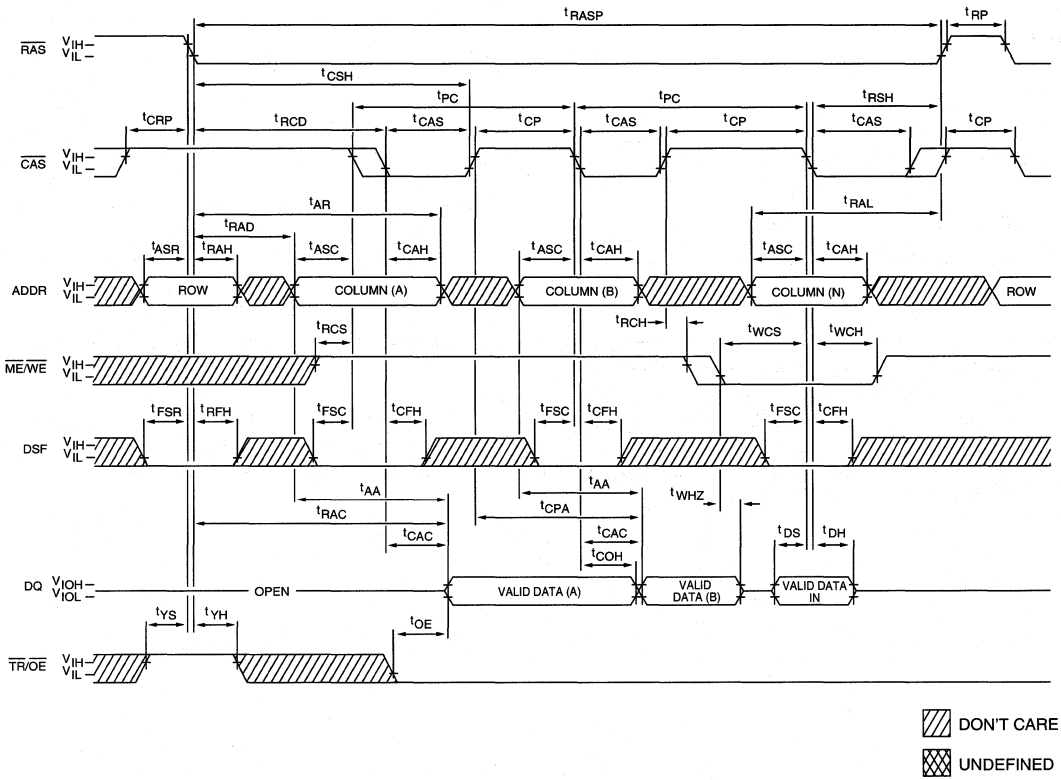
VRAM

DRAM FAST-PAGE-MODE READ CYCLE
(Extended Data-Out)



NOTE: 1. WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.
2. If ^{t}OEHC and ^{t}OEP are met, the DQs will remain in High-Z (even if $\overline{TR/OE}$ goes LOW again) until the next $\overline{CAS}$ cycle.

DRAM FAST-PAGE-MODE READ/WRITE CYCLE
(Extended Data-Out)



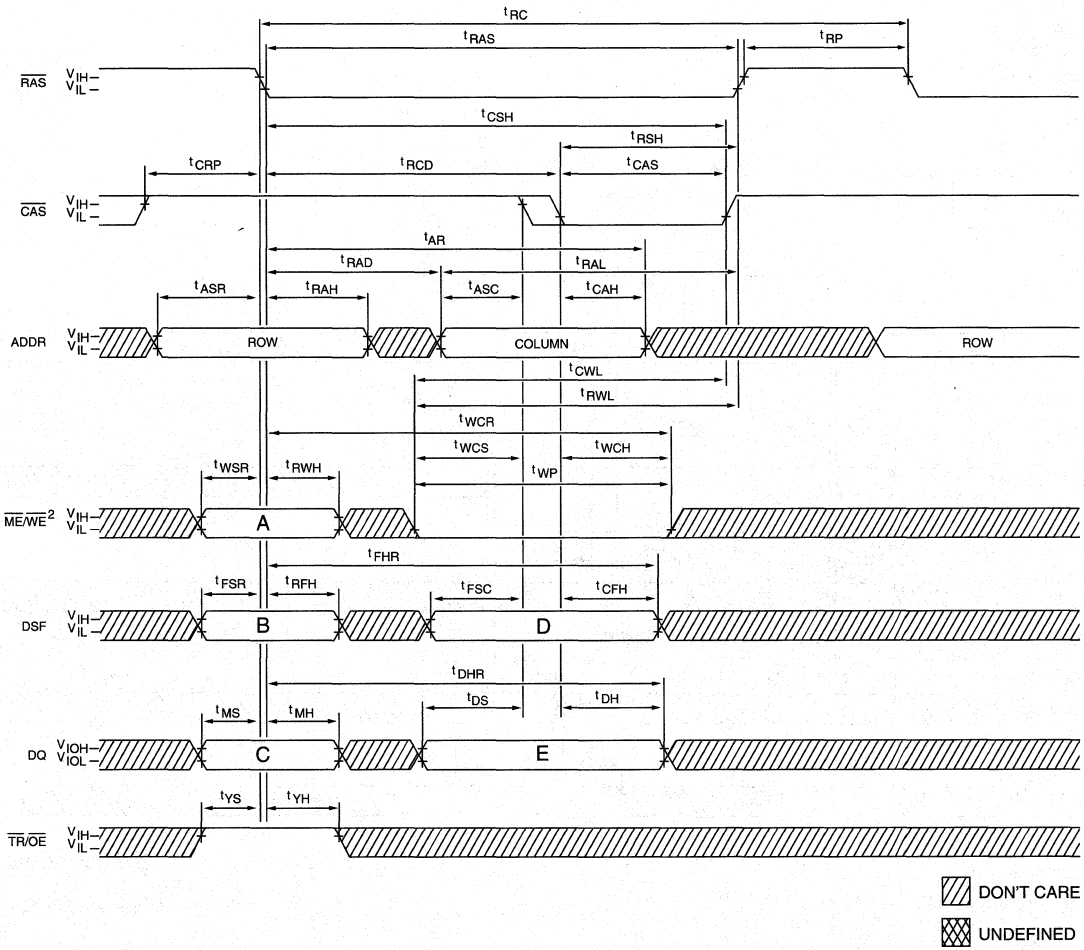
NOTE: $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are both HIGH for READs; either or both are LOW for WRITEs.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$ [4]	B DSF	C DQ (Input)	D DSF	E [2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask [3]	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask [3]	1	Column Mask
MASKED FLASH WRITE to DRAM	0	1	Write Mask [3]	X	X
Load Mask Data Register	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{MEL}, \overline{U}/\overline{WEL}, \overline{U}$ falling edge, whichever occurs last.
3. Mask data is loaded at $\overline{RAS}$ falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the mask data register and the DQs are "don't care" at the $\overline{RAS}$ falling edge.
4. $\overline{ME}/\overline{WE}$ = 1 if both $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are HIGH at the falling edge of RAS. $\overline{ME}/\overline{WE}$ = 0 if either or both of those signals is LOW at that time.

DRAM EARLY-WRITE CYCLE [1]

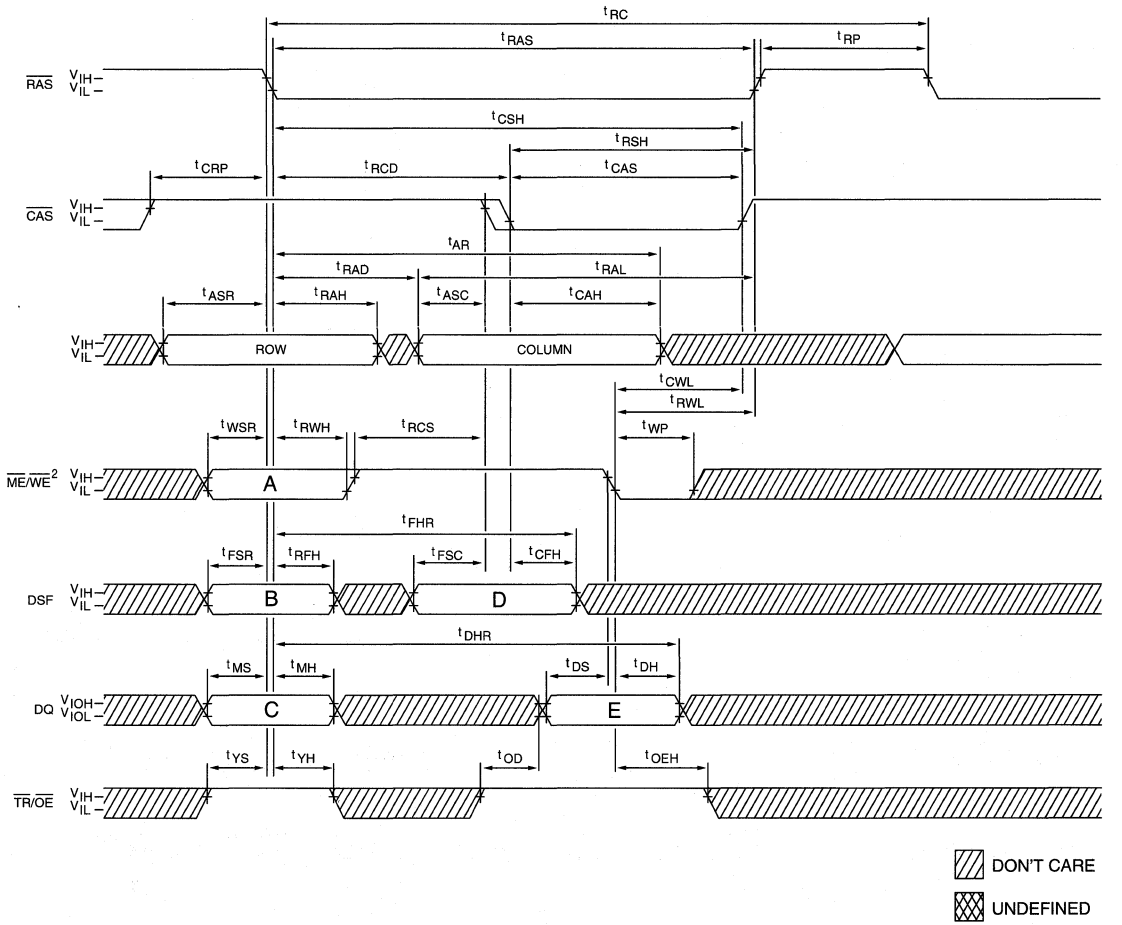


NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

2. Either or both of $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ may be LOW at the $\overline{CAS}$ falling edge. If one is LOW a BYTE WRITE is performed; if both are LOW a WORD WRITE is performed.

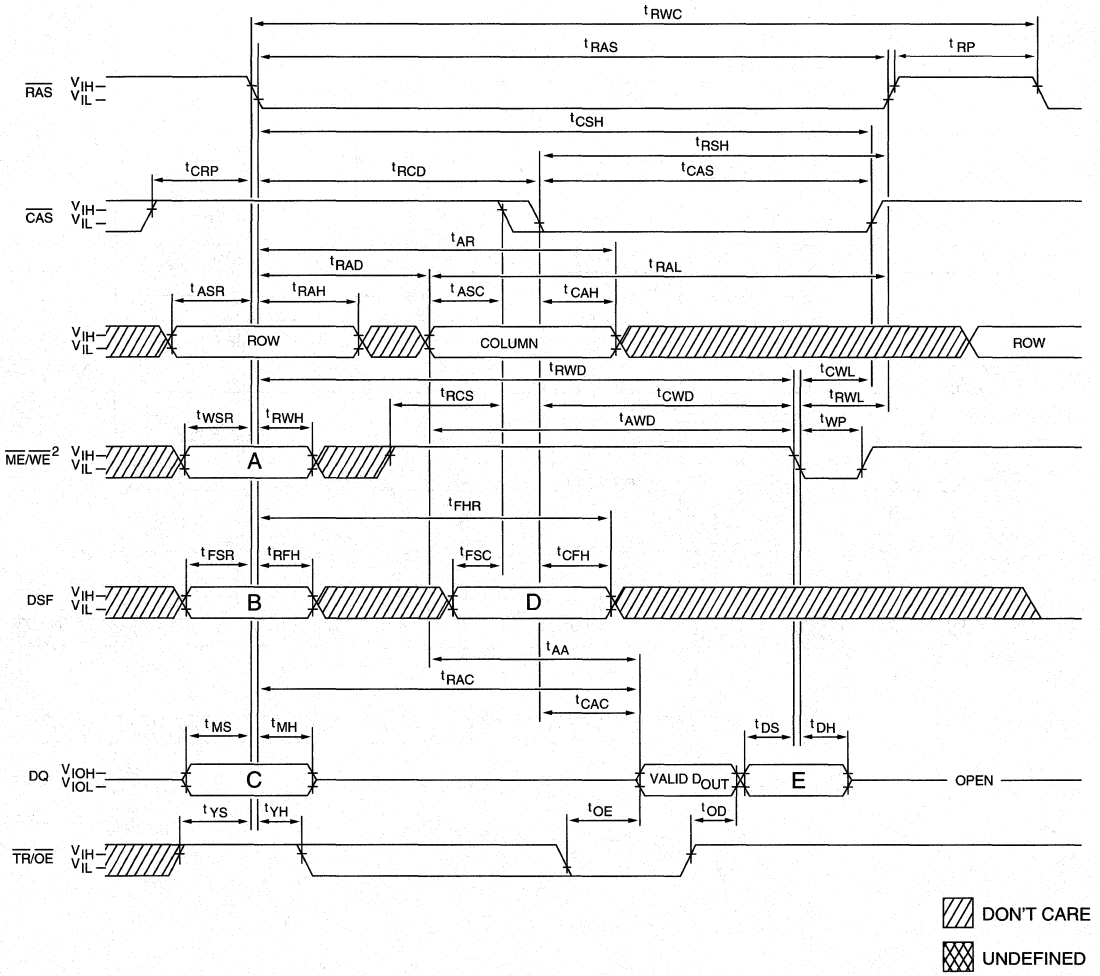
VRAM

DRAM LATE-WRITE CYCLE



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. Either or both of $\overline{\text{MEL}}/\overline{\text{WEL}}$ and $\overline{\text{MEU}}/\overline{\text{WEU}}$ may go LOW while $\overline{\text{CAS}}$ is LOW. If one goes LOW, a BYTE WRITE is performed; if both go LOW, a WORD WRITE is performed.

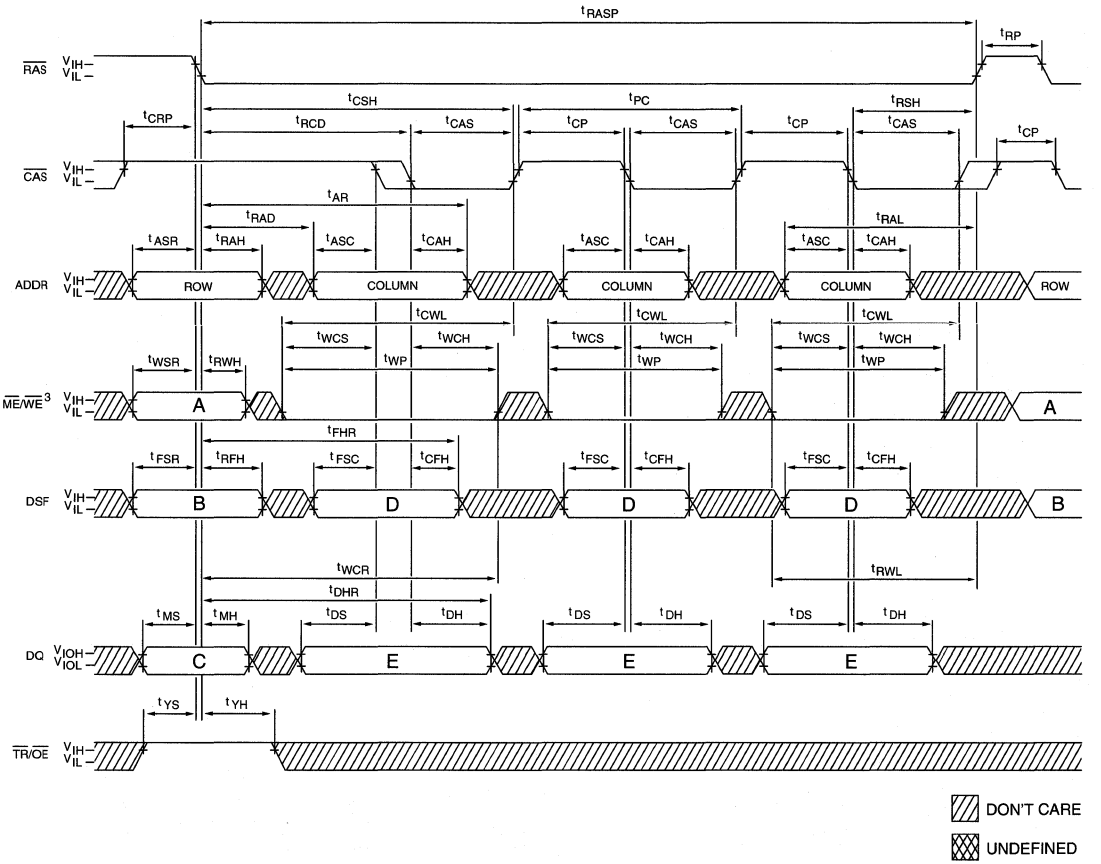
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. Either or both of $\overline{\text{MEL}}/\overline{\text{WEL}}$ and $\overline{\text{MEU}}/\overline{\text{WEU}}$ may go LOW while $\overline{\text{CAS}}$ is LOW. If one goes LOW, a BYTE WRITE is performed; if both go LOW, a WORD WRITE is performed.

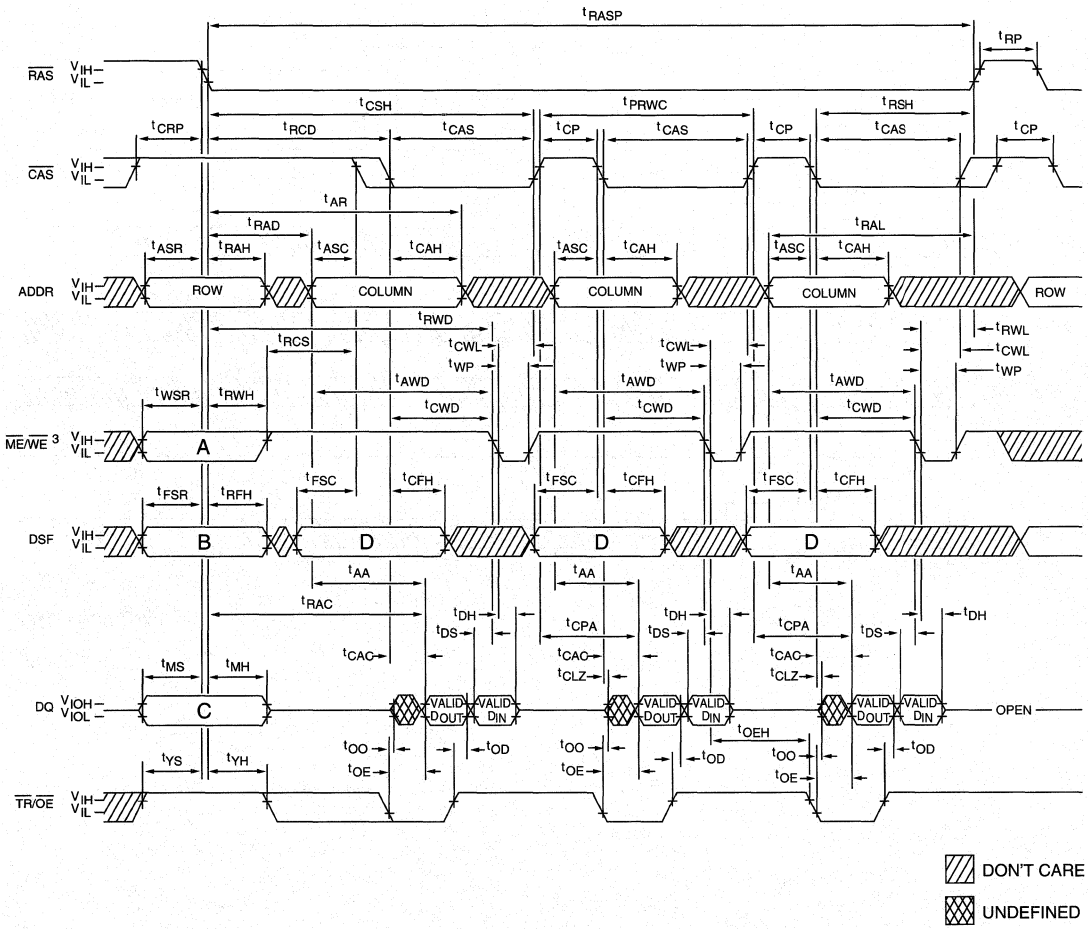
VRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
3. Either or both of $\overline{\text{MEL}}/\overline{\text{WEL}}$ and $\overline{\text{MEU}}/\overline{\text{WEU}}$ may be LOW at the $\overline{\text{CAS}}$ falling edge. If one is LOW a BYTE WRITE is performed; if both are LOW a WORD WRITE is performed.

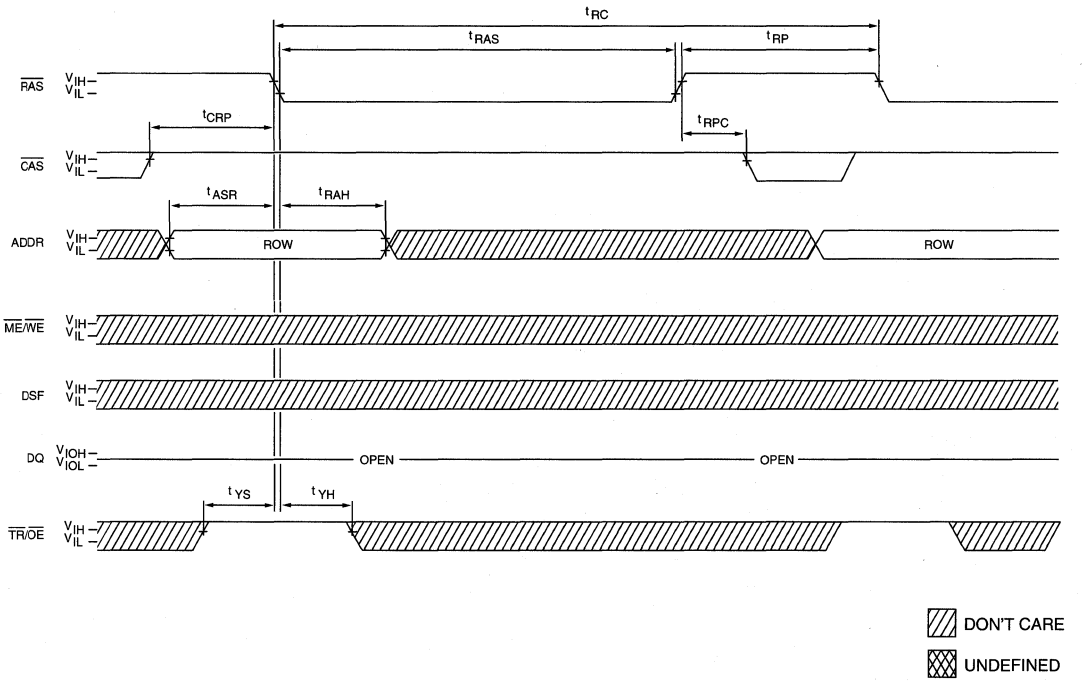
DRAM FAST-PAGE-MODE READ-WRITE CYCLE [1, 2]
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
3. Either or both of $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ may be LOW while $\overline{CAS}$ is LOW. If one goes LOW, a BYTE WRITE is performed; if both go LOW, a WORD WRITE is performed.

VRAM

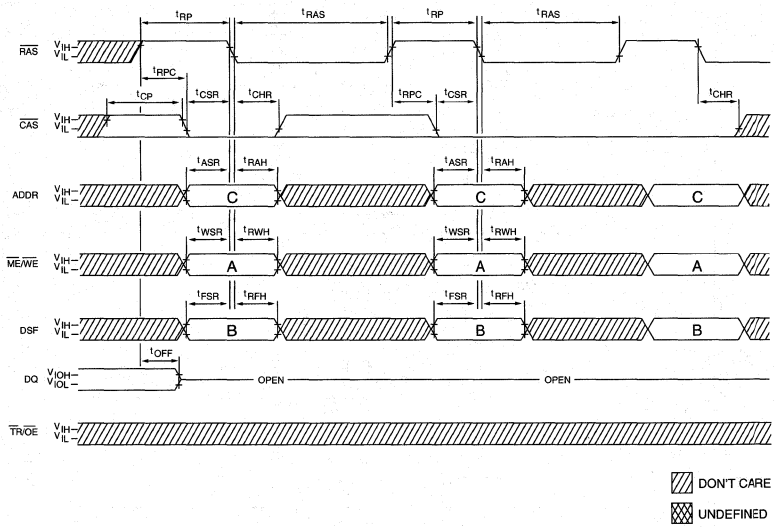
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CBR CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		RAS Falling Edge (CAS = LOW)		
		A[1] ME/WE	B DSF	C A0-A8
CBR REFRESH (Reset All Options)	CBRR	X	0	X
CBR REFRESH (Set/Reset Stop Address)	CBRS	0	1	STOP ADDRESS[2]
CBR REFRESH (No Reset)	CBRN	1	1	X

CBR REFRESH CYCLE [3]



NOTE: 1. $\overline{ME}/\overline{WE}$ = 1 if both $\overline{MEL}/\overline{WEL}$ and $\overline{MEU}/\overline{WEU}$ are HIGH at the falling edge of RAS. $\overline{ME}/\overline{WE}$ = 0 if either or both of those signals is LOW at that time.

2. Programmable Stop Point column addresses:

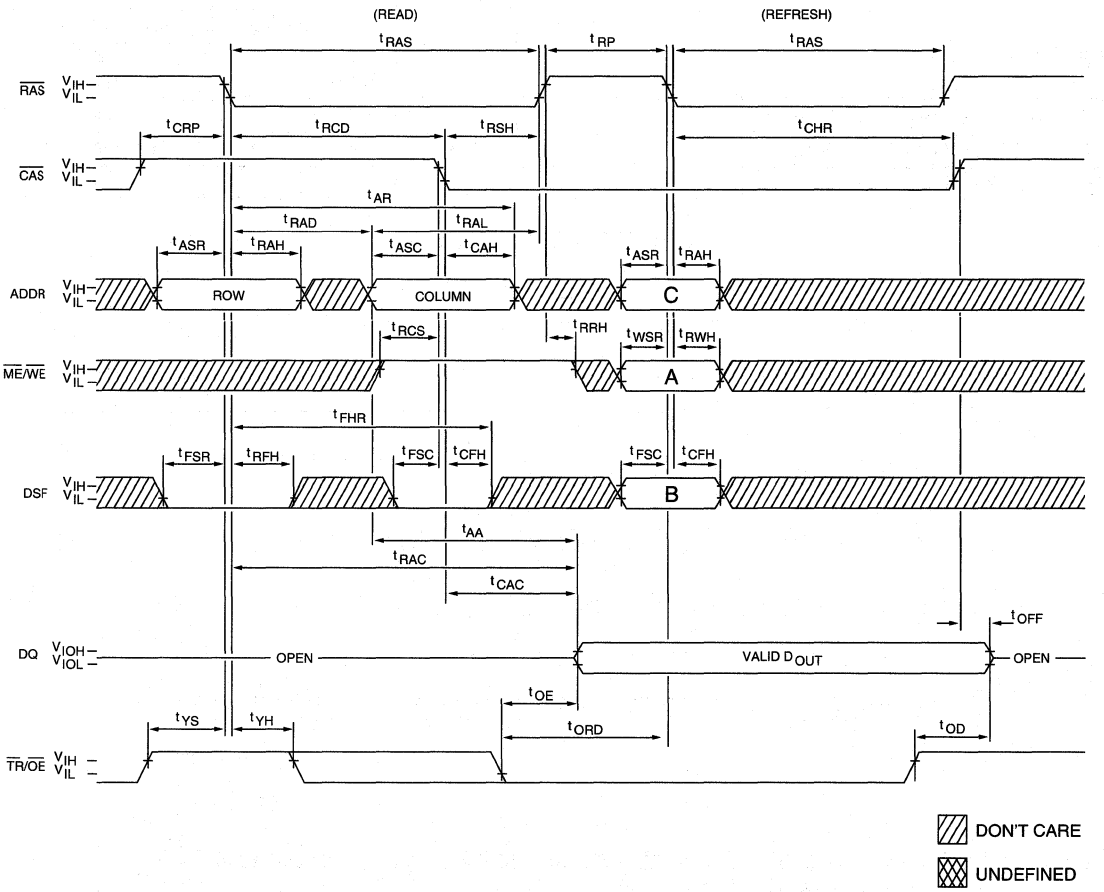
Number Stop Points/Half	Address @ RAS LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

3. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

VRAM

DRAM HIDDEN-REFRESH CYCLE [1, 2]

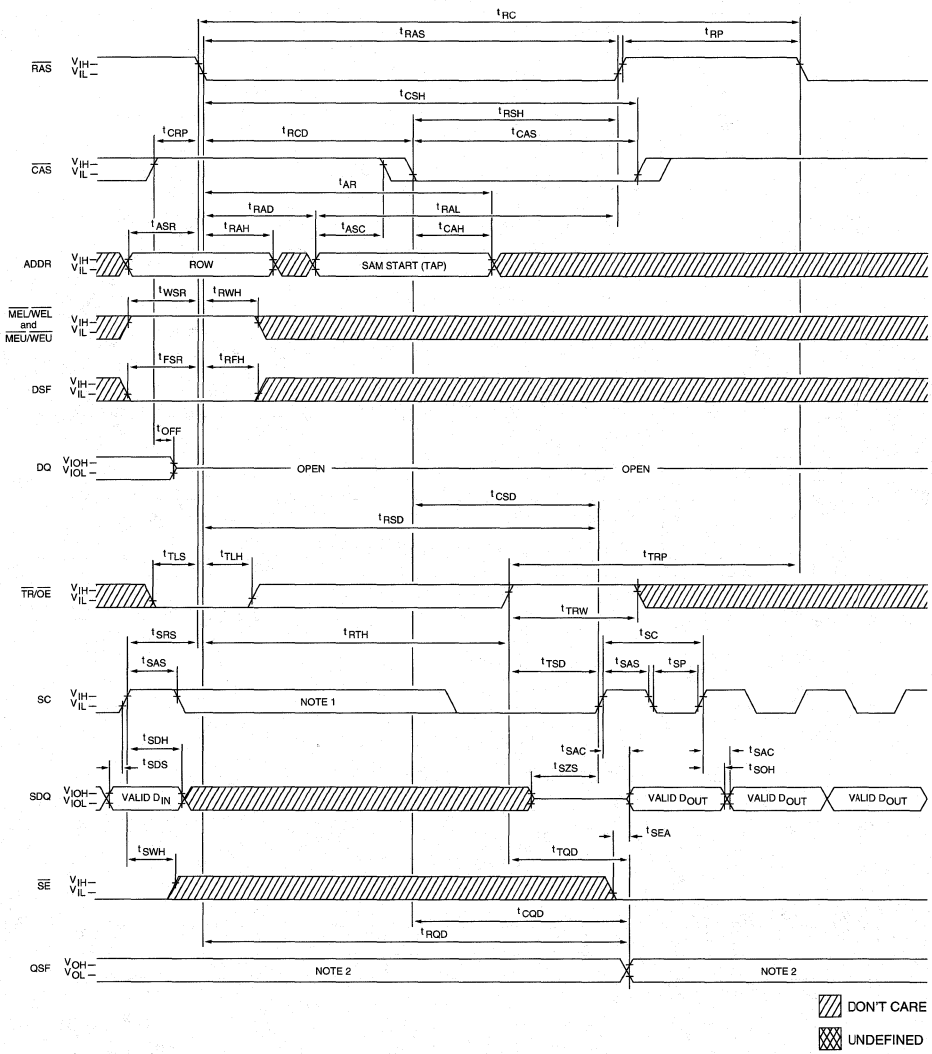


NOTE: 1. A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{MEL}$,$\overline{U}$/$\overline{WEL}$,$\overline{U}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}$/$\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}$/$\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}$/$\overline{OE}$.

2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode, or SC idle)

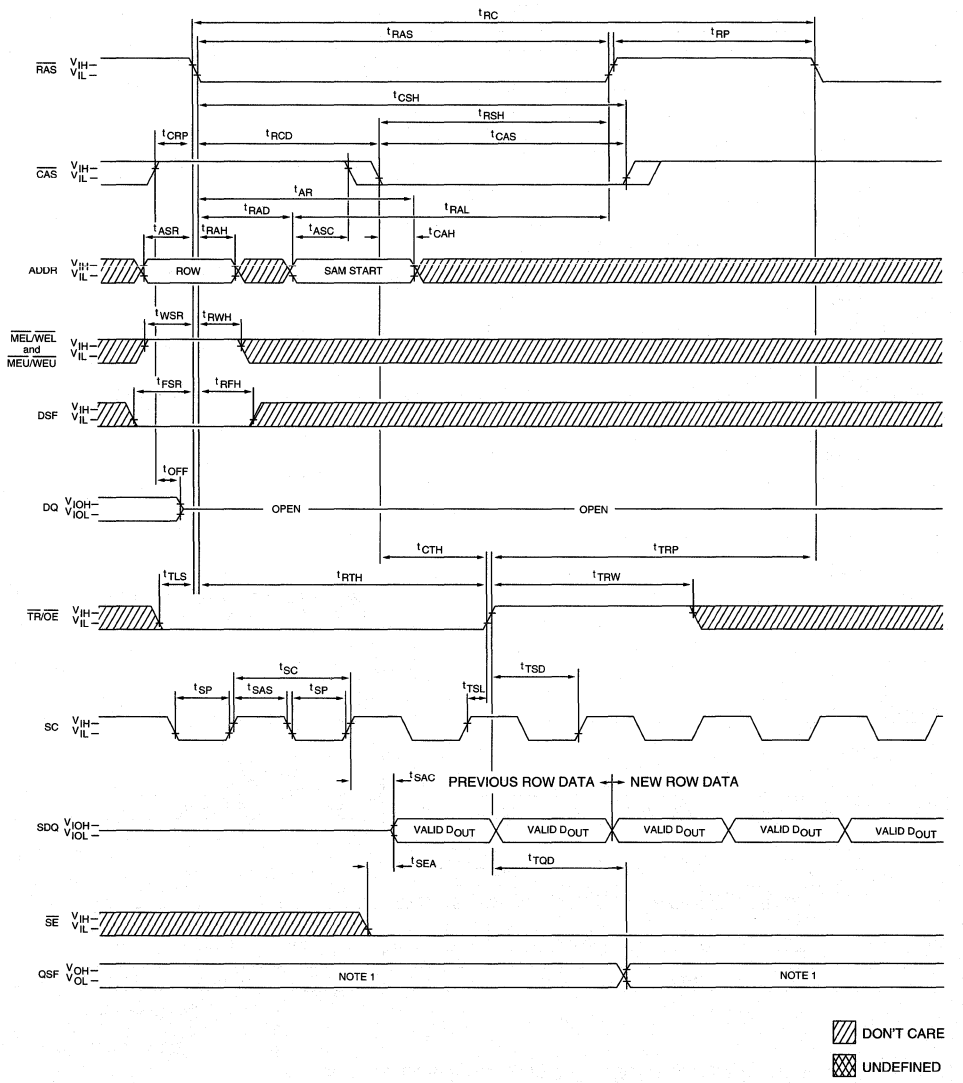


NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}$/($\overline{OE}$) rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}$/($\overline{OE}$) rising edge, the transfer is done off of the $\overline{TR}$/($\overline{OE}$) rising edge and ^{t}TSD must be met.

VRAM

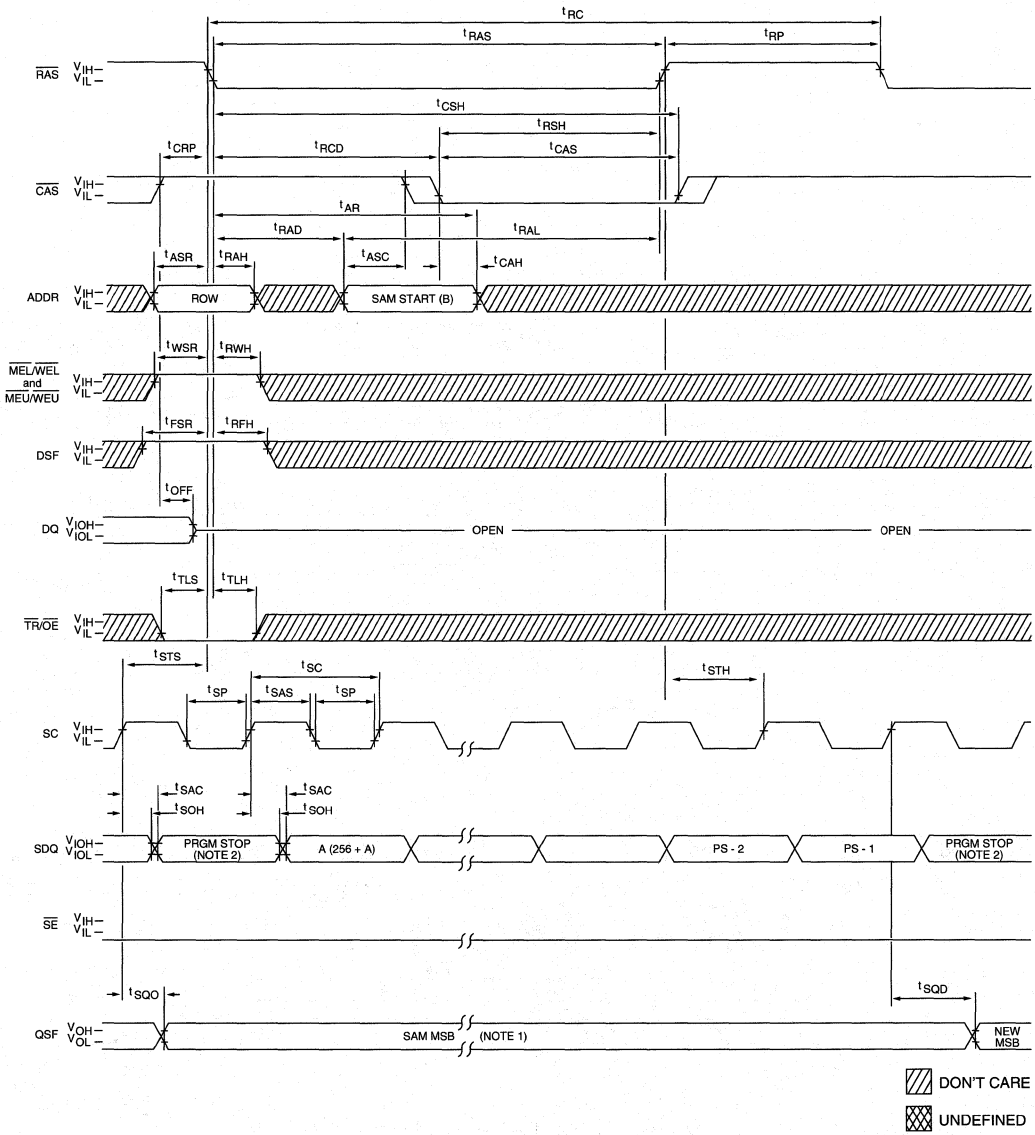
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.

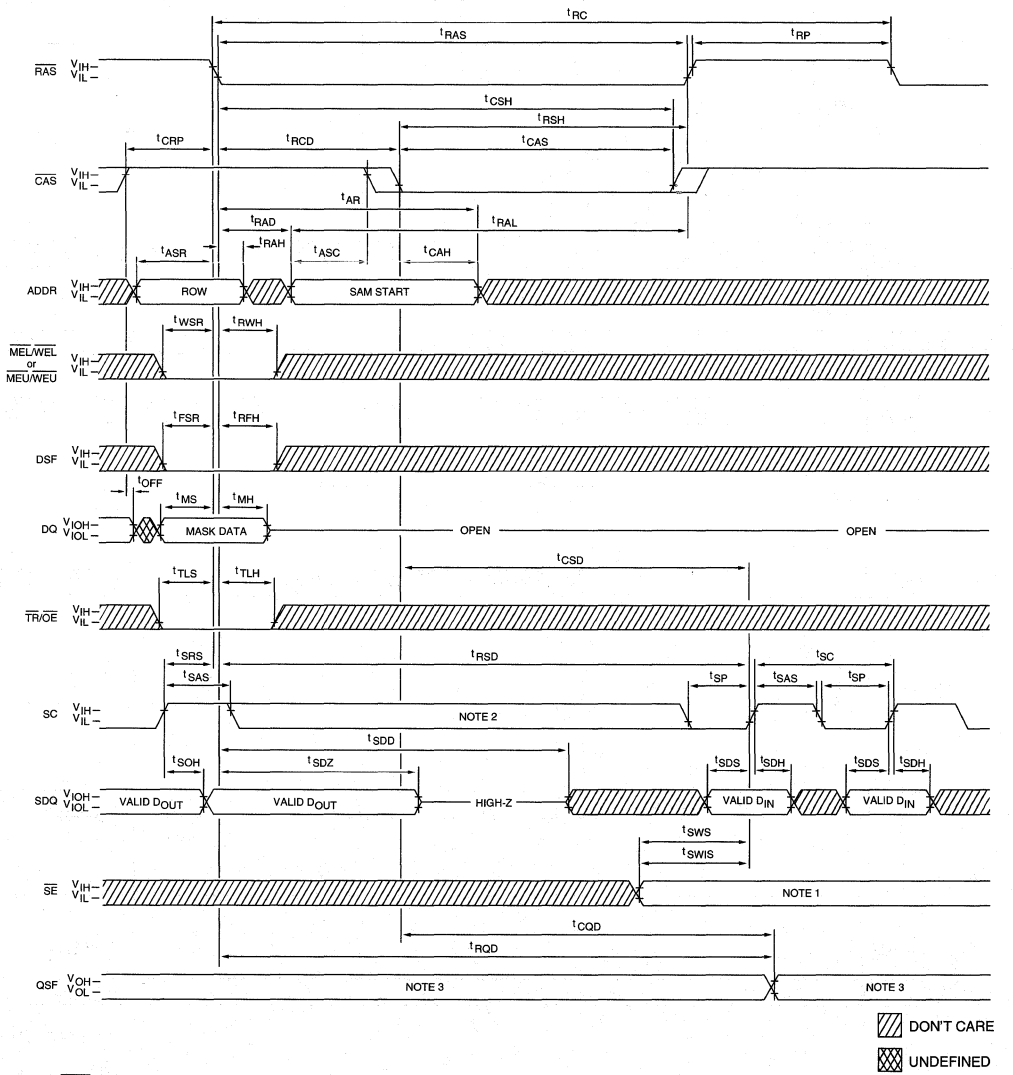
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the programmable split SAM functional description for detail.

VRAM

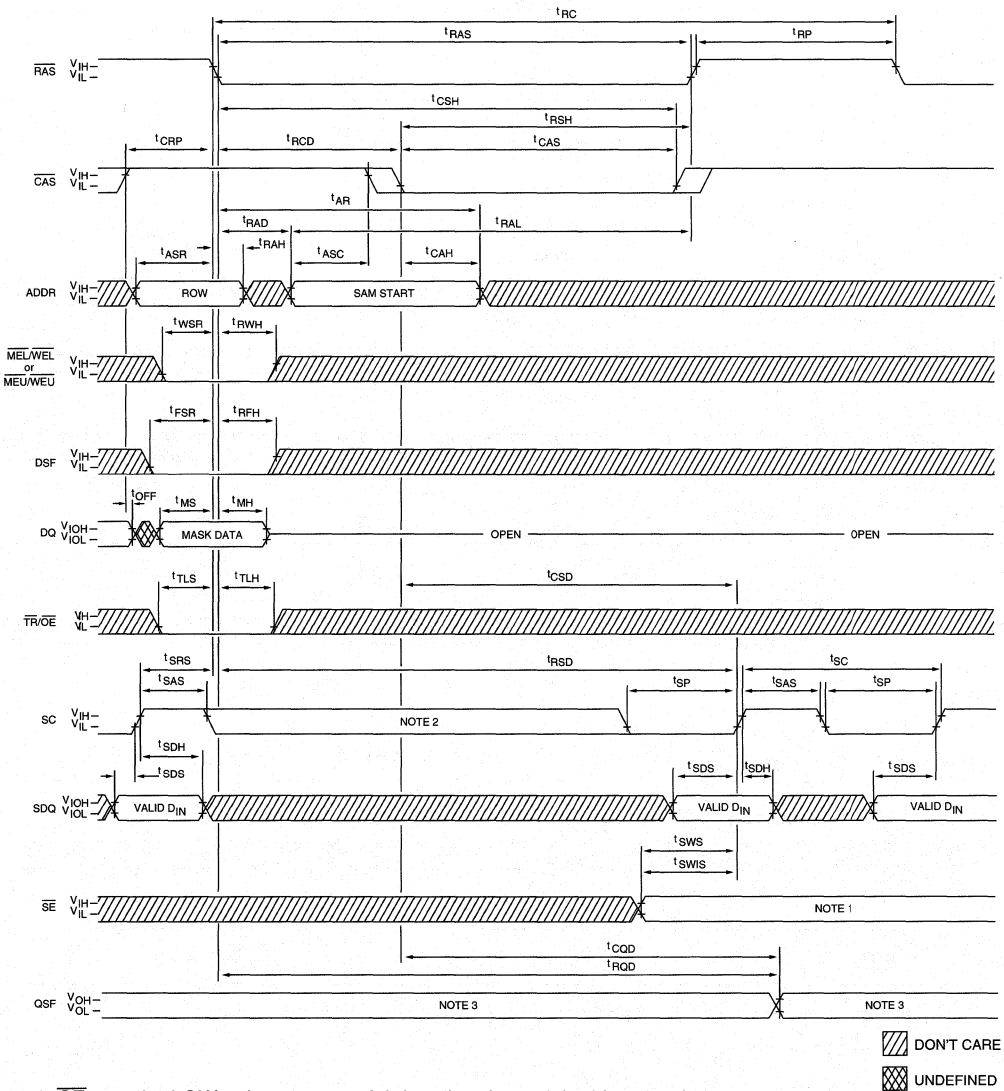
MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.

MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)

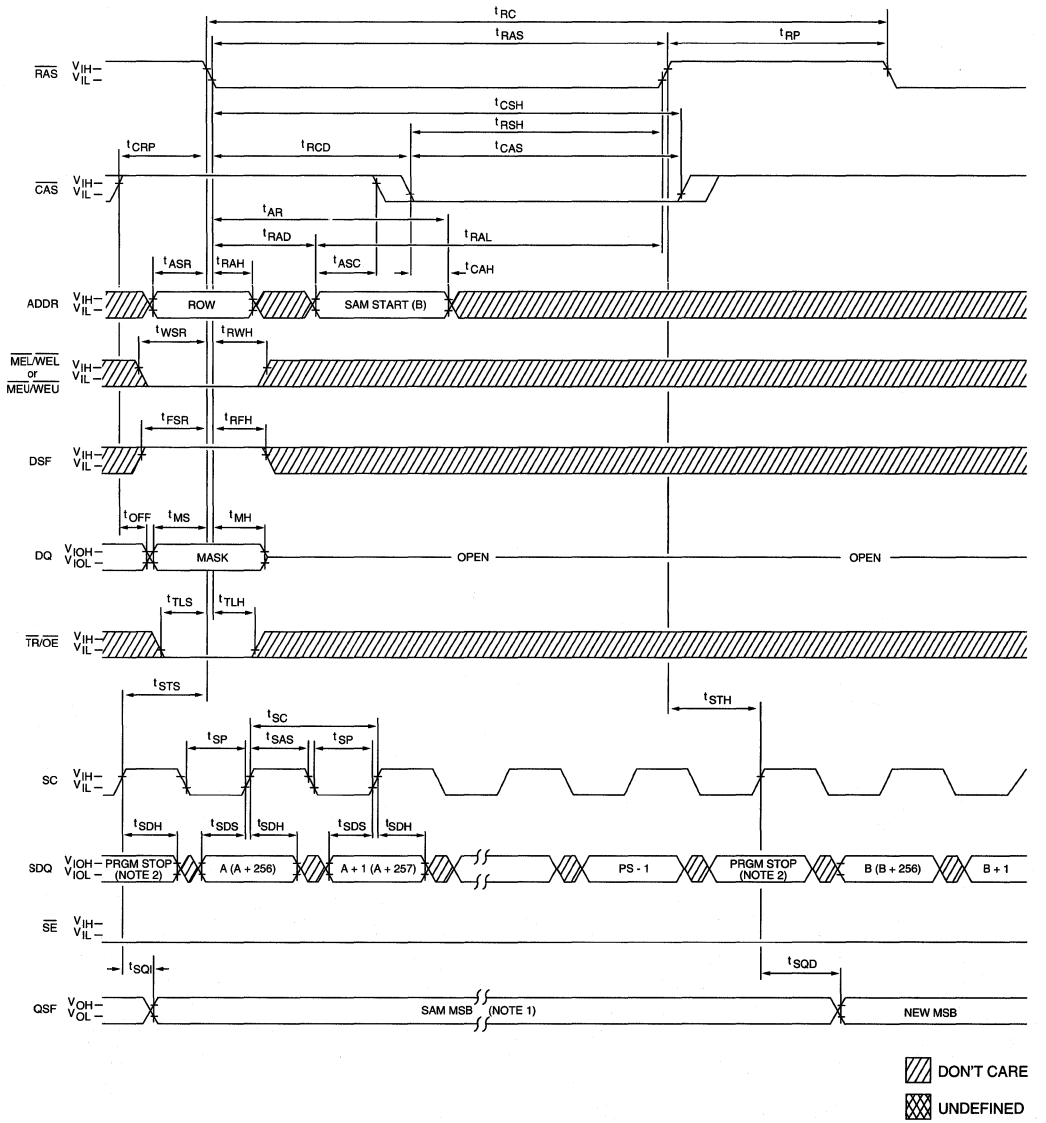
(When part was previously in the SERIAL INPUT mode)



NOTE: 1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 255–511) is being accessed.

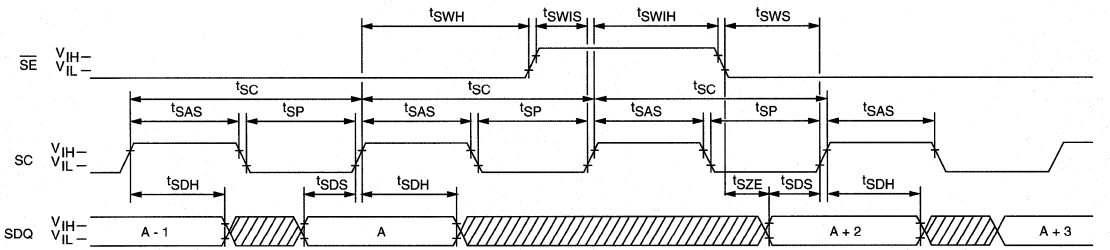
VRAM

MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

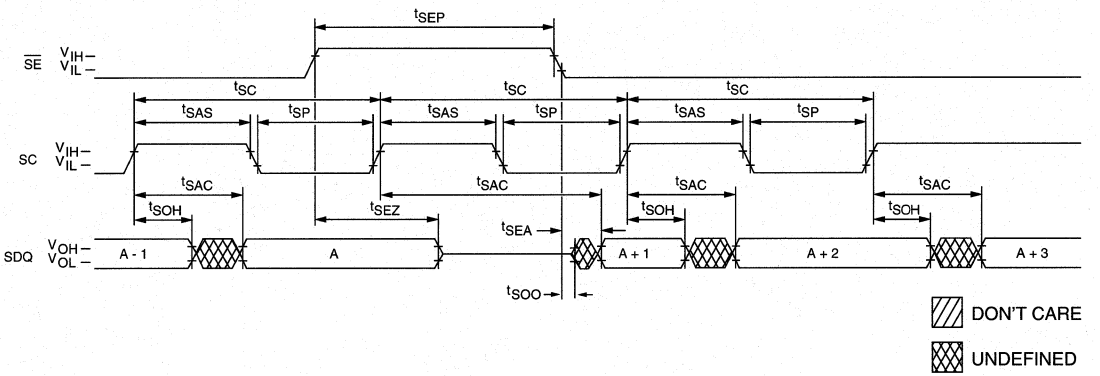


NOTE: 1. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the programmable split SAM functional description for detail.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



NEW VRAM

VRAM

256K x 16 DRAM WITH 512 x16 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE access
- Upper and lower byte $\overline{WE}$ control
- Dual-port organization: 256K x 16 DRAM port
  512 x 16 SAM port
- No refresh required for serial access memory
- Fast access times: 70ns random, 17ns serial
  60ns random, 15ns serial*

SPECIAL FUNCTIONS

- JEDEC Basic Feature Set, plus:
- PERSISTENT MASKED WRITE
- EIGHT COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])

60ns, 18/15ns	-6*
70ns, 20/17ns	-7
80ns, 22/20ns	-8

- Packages

Plastic SOP (12 mm)	SG
PLASTIC TSOP (400mil)	TG*

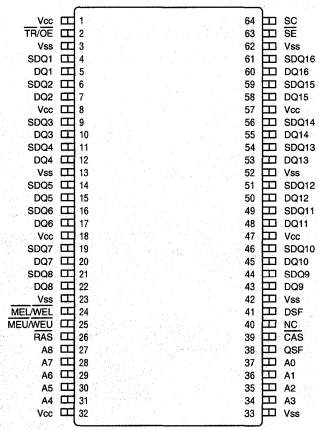
- Part Number Example: MT42C256K16C1SG-7

GENERAL DESCRIPTION

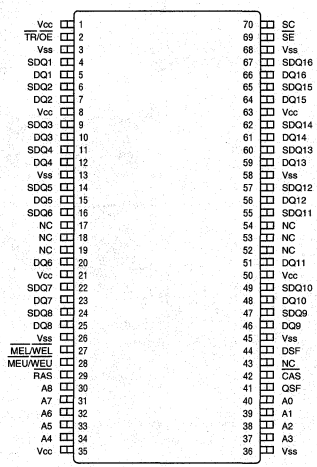
The MT42C256K16C1 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by a 16-bit-wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

PIN ASSIGNMENT (Top View)

64-Pin SOP (SDC-1)



70-Pin TSOP* (SDE-4)



*Consult factory for availability.

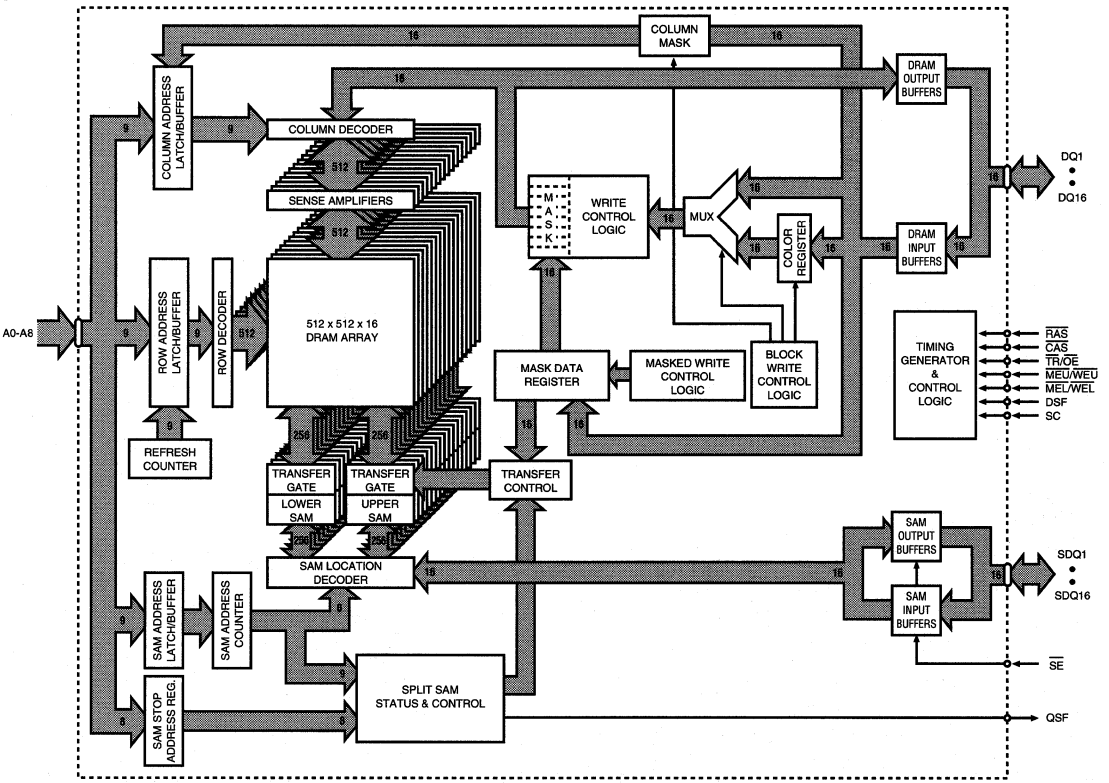
NEW VRAM

The DRAM portion of the VRAM is similar to standard 256K x 16-bit DRAMs, with the addition of BLOCK WRITEand FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512-bit-wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16C1 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, extended data-out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



NEW VRAM

VRAM

256K x 16 DRAM WITH 512 x16 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE access
- Upper and lower byte $\overline{CAS}$ control
- Dual-port organization: 256K x 16 DRAM port
  512 x 16 SAM port
- No refresh required for serial access memory
- Fast access times: 70ns random, 17ns serial
  60ns random, 15ns serial*

SPECIAL FUNCTIONS

- JEDEC Basic Feature Set, plus:
- PERSISTENT MASKED WRITE
- EIGHT COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

OPTIONS — MARKING

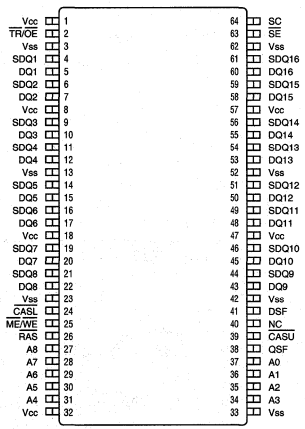
- Timing (DRAM, SAM [cycle/access])
  - 60ns, 18/15ns — -6*
  - 70ns, 20/17ns — -7
  - 80ns, 22/20ns — -8
- Packages
  - Plastic SOP (12 mm) — SG
  - Plastic TSOP(400mil) — TG*
- Part Number Example: MT42C256K16C2SG-7

GENERAL DESCRIPTION

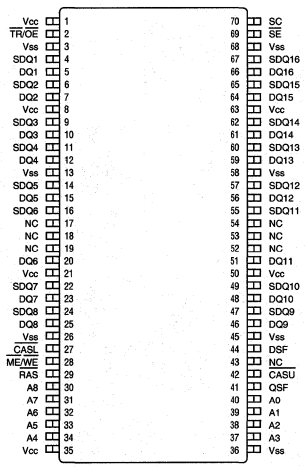
The MT42C256K16C2 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by a 16-bit-wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

PIN ASSIGNMENT (Top View)

64-Pin SOP (SDC-1)



70-Pin TSOP* (SDE-4)



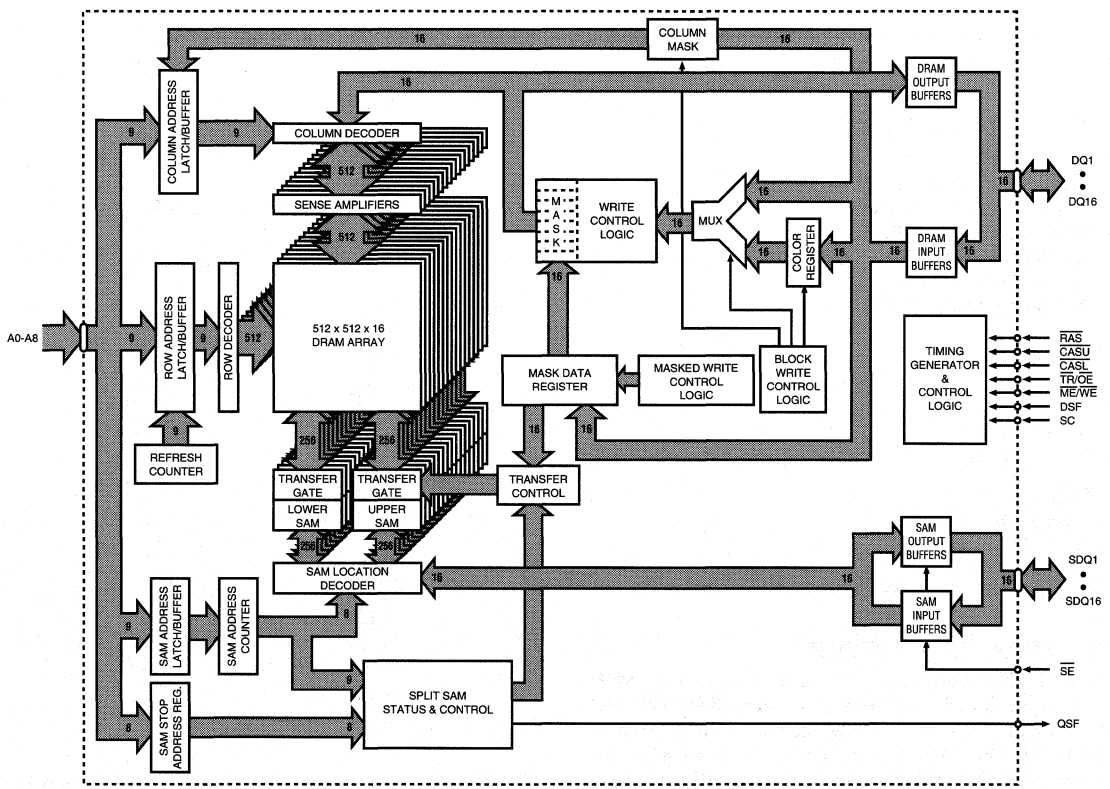
*Consult factory for availability.

The DRAM portion of the VRAM is similar to standard 256K x 16-bit DRAMs, with the addition of BLOCK WRITE and FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512-bit-wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16C2 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, extended data-out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



MICRON
SEMICONDUCTOR, INC.

TRIPLE-PORT DRAM SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins				Page
				Standby	Active	SOJ	SOG	TSOP	PLCC	
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	3-1
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44	-	3-1
256K x 4	FP, BW, QSF pin	MT43C4257A	70, 80	15mW	500mW	40	-	40/44	-	3-3
256K x 4	FP, BW, SSF pin	MT43C4258A	70, 80	15mW	500mW	40	-	40/44	-	3-3
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	3-49
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	3-49
128K x 8	FP, BW, QSF pin	MT43C8128A	70, 80	15mW	550mW	-	-	-	52	3-51
128K x 8	FP, BW, SSF pin	MT43C8129A	70, 80	15mW	550mW	-	-	-	52	3-51
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW	-	64	-	-	3-97

FP = FAST-PAGE-MODE, BW = BLOCK WRITE

TRIPLE-PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 500mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST-PAGE-MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

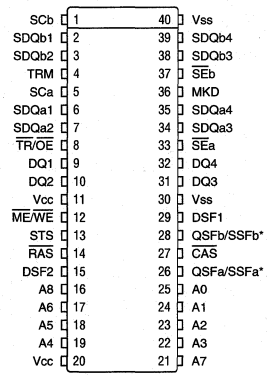
OPTIONS

	MARKING
• Timing (DRAM, SAMs [cycle/access])	
80ns, 28ns/25ns	- 8
100ns, 30ns/27ns	-10
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
• Functionality	
QSF output	MT43C4257
(indicates SAM-half accessed)	
SSF input	MT43C4258
(Split SAM special function, stop count)	

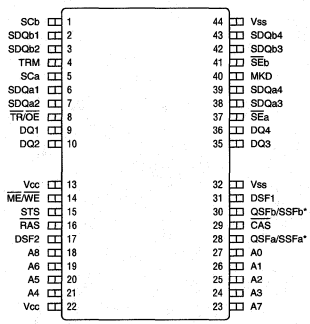
- Part Number Example: MT43C4257DJ-8

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(SDB-3)



40/44-Pin TSOP**
(SDE-2)



*MT43C4257/MT43C4258
**Consult factory for TSOP availability.

GENERAL DESCRIPTION

The MT43C4257/8 are high-speed, triple-port CMOS dynamic random access memories (TPDRAMs) containing 1,048,576 bits. Data may be accessed by a 4-bit-wide DRAM port or by either of two independently clocked 512 x 4-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and either SAM.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048-bit-

wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

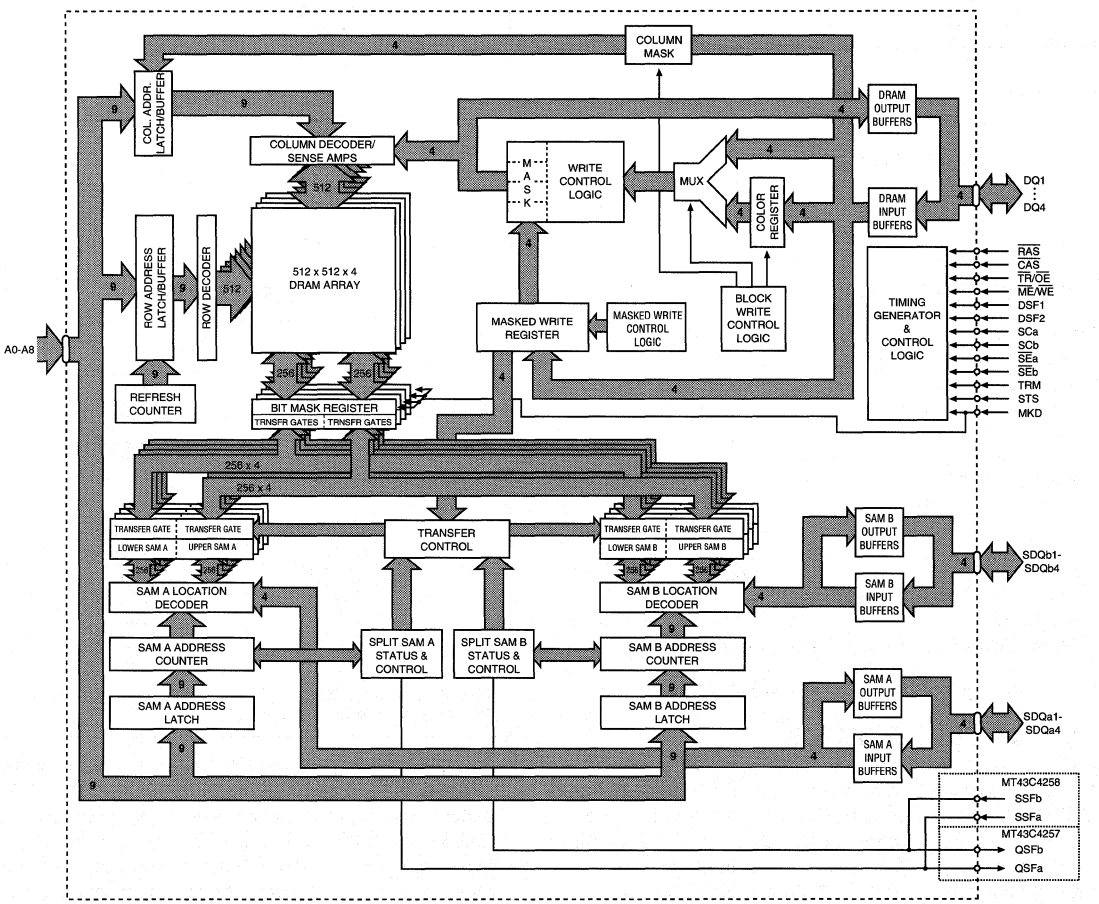
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit bit mask data register can be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257/8 are optimized for high performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



TRIPLE-PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

NEW TRIPLE-PORT DRAM

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 70ns random, 22ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 500mW active, typical
- 512-cycle refresh within 16.7ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST-PAGE-MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

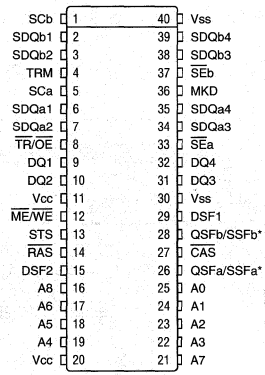
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS — MARKING

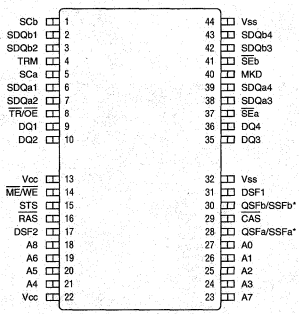
- Timing (DRAM, SAMs [read cycle/write cycle])
  - 70ns, 22ns/20ns — -7
  - 80ns, 25ns/20ns — -8
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Functionality
  - QSF output (indicates SAM-half accessed) — MT43C4257A
  - SSF input (Split SAM special function, stop count) — MT43C4258A
- Part Number Example: MT43C4257ADJ-7

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(SDB-3)



40/44-Pin TSOP**
(SDE-2)



*MT43C4257A/MT43C4258A
**Consult factory for TSOP availability.

GENERAL DESCRIPTION

The MT43C4257A/8A are high-speed, triple-port CMOS dynamic random access memories (TPDRAMs) containing 1,048,576 bits. Data may be accessed by a 4-bit-wide DRAM port or by either of two independently clocked 512 x 4-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and either SAM.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048-bit-

NEW TRIPLE-PORT DRAM

wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

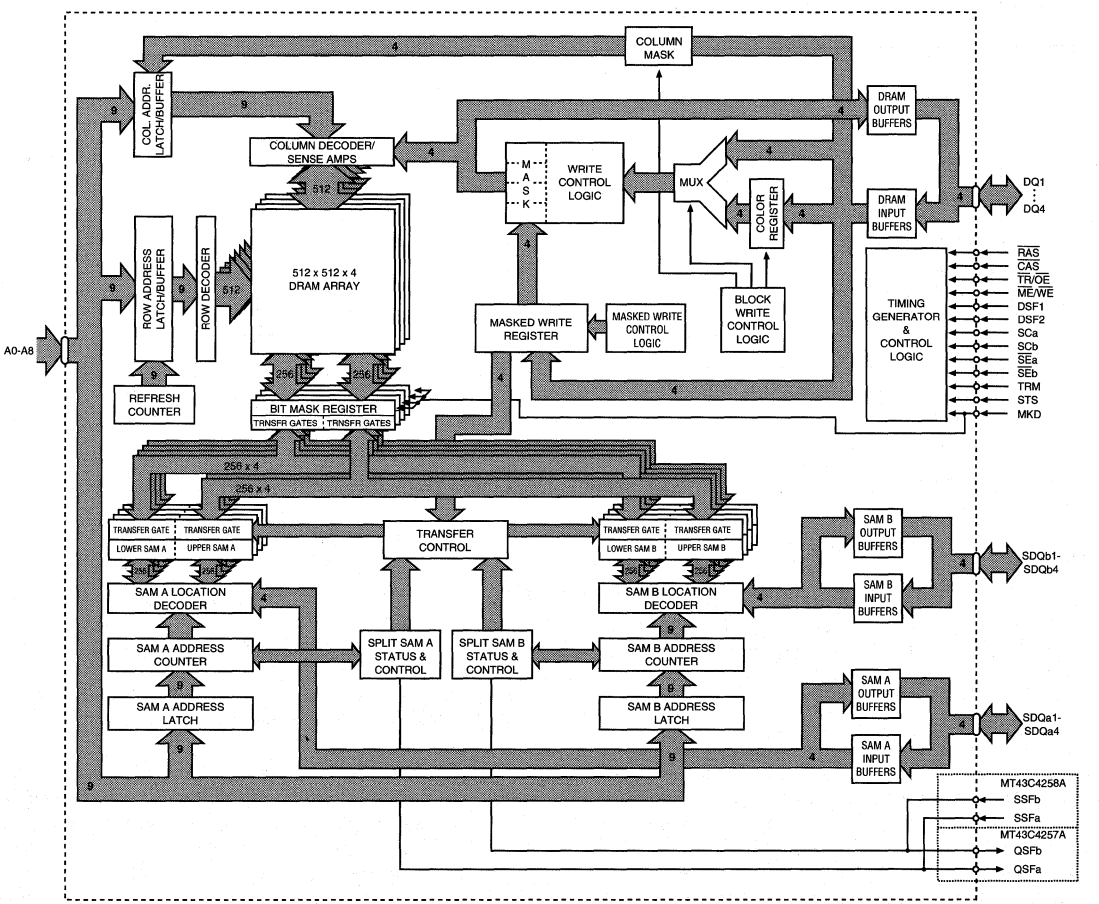
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit bit mask data register may be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257A/8A are optimized for high-performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5	5	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
8	8	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
12	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
33	37	$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
37	41	$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
29	31	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
15	17	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the control and data inputs.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe control inputs and data inputs.

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
13	15	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
36	40	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
4	4	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
9, 10, 31, 32	9, 10, 35, 36	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
6, 7, 34, 35	6, 7, 38, 39	SDQa1-SDQa4	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 38, 39	2, 3, 42, 43	SDQb1-SDQb4	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
26	28	QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C4257A): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C4258A): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
28	30	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C4257A): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C4258A): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±5%
30, 40	32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C4257A/8A may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, the TR/(OE) pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C4257A/8A TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT43C4257A/8A support CBR, RAS ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row-addresses are generated and stored in an internal address counter. The user need not supply any address data but must simply perform 512 CBR cycles within the 16.7ms time period.

For RAS-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the RAS-ONLY and CBR cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling RAS (while keeping CAS LOW) after a READ or WRITE cycle. This performs CBR REFRESH cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C4257A/8A are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 18 address bits used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS, and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

Note: *RAS also acts as a "master" chip enable for the TPDRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single-port DRAMS, the OE pin is a "don't care" when RAS goes LOW. For the TPDRAM, TR/(OE) is used when RAS goes LOW to select between DRAM and TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH to LOW transition for all DRAM operations.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transition from HIGH to LOW some time after RAS falls to enable the DRAM output port.

For single-port DRAMs, WE is a "don't care" when RAS goes LOW. For the TPDRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW when CAS goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

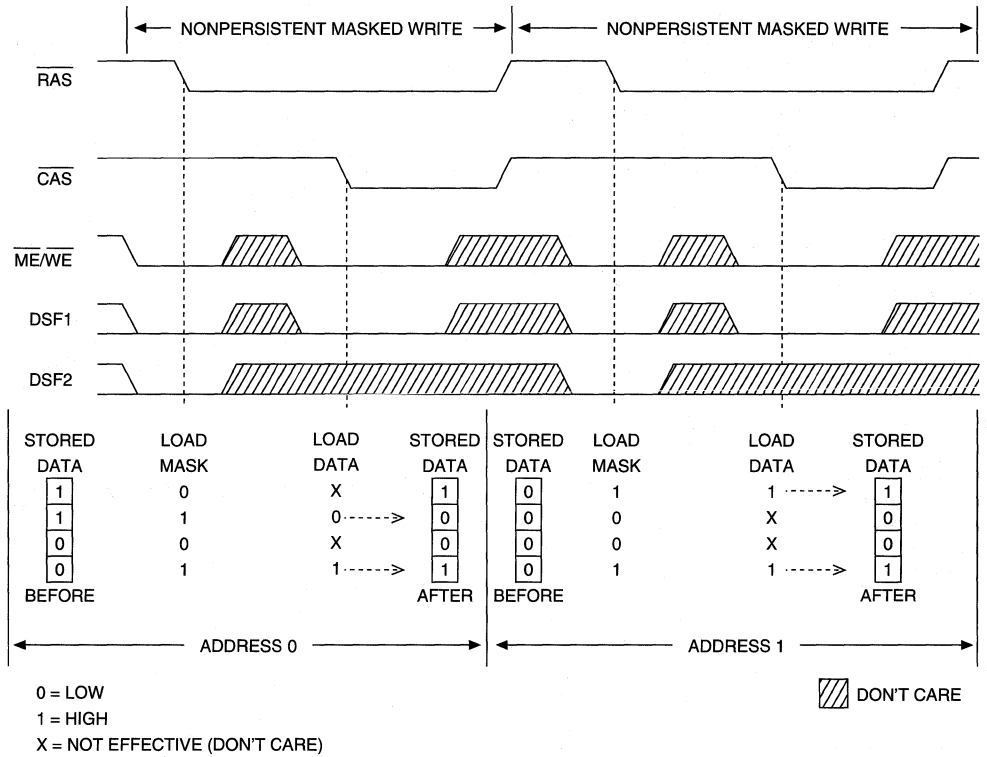


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a 4-bit word. The MT43C4257A/8A support two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH- to-LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C4257A/8A. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ or $(\overline{ME})/\overline{WE}$ go LOW, the bits present on the DQ1-DQ4 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST-PAGE-MODE can be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

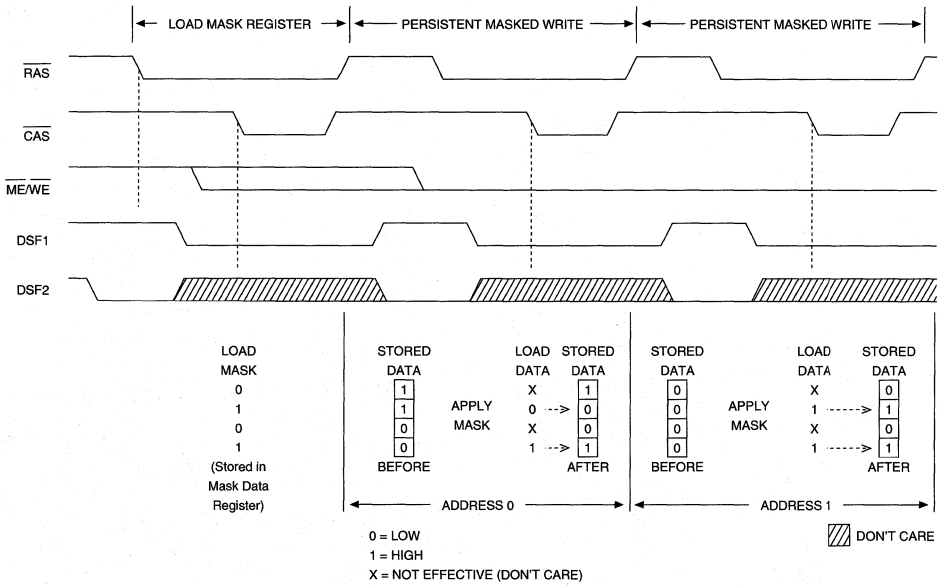


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description). PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW, and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs.

Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST-PAGE-MODE.

BLOCK WRITE (BW)

The MT43C4257A/8A will perform a BLOCK WRITE cycle if DSF1 is HIGH when $\overline{CAS}$ goes LOW. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 16 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" (out of the 128 possible) of four adjacent column locations that will be accessed. When the latter of $\overline{ME}/\overline{WE}$ and $\overline{CAS}$ go LOW, the DQ inputs are latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color

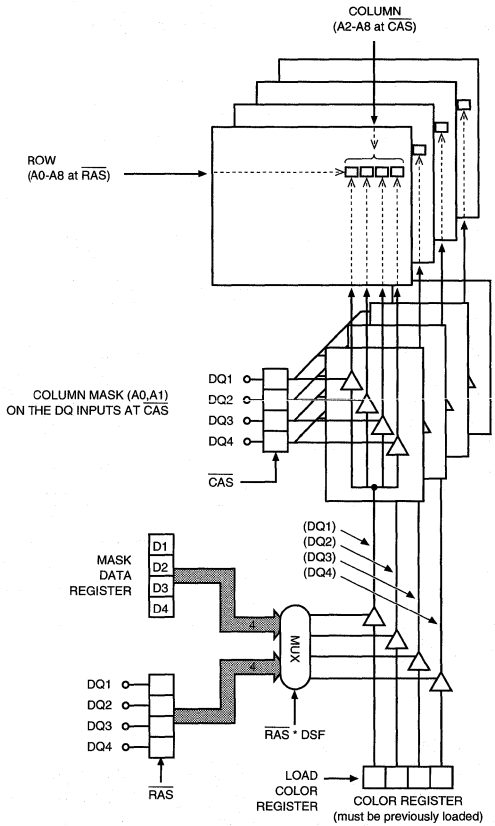


Figure 3
BLOCK WRITE EXAMPLE

register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C4257A/8A contain two 4-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE LOAD MASK REGISTER cycles are performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable WRITEs to the four DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A WRITE is referenced to the DRAM array and a READ is referenced from the array.

Note: *The three ports of the TPDRAM are independent of, and asynchronous to, one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C4257A/8A include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a transfer operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C4257A/8A support all of the popular transfer cycles available on Micron's 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{ME})/\overline{WE}$ is HIGH, DSF1, DSF2 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row-address bits indicate the four 512-bit DRAM rows that are to be transferred to the four SAM data registers. The column-address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW if the lower half, HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAM's I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the ^{t}RSD and ^{t}CSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 9-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (non-split) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT can be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half

that receives the transfer. When $\overline{CAS}$ falls, address pins A0-A7 determine the Tap address for the SAM-half selected; A8 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half ≠ 0. For the MT43C4257A, serial access continues, and when the SAM address counter reaches 255 ("A8" = 1, A0-A7 = 0), the QSF output for that SAM goes HIGH. Then the Tap address for the upper half is automatically loaded. Since the serial access has switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C4258A. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (255; lower, 511; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

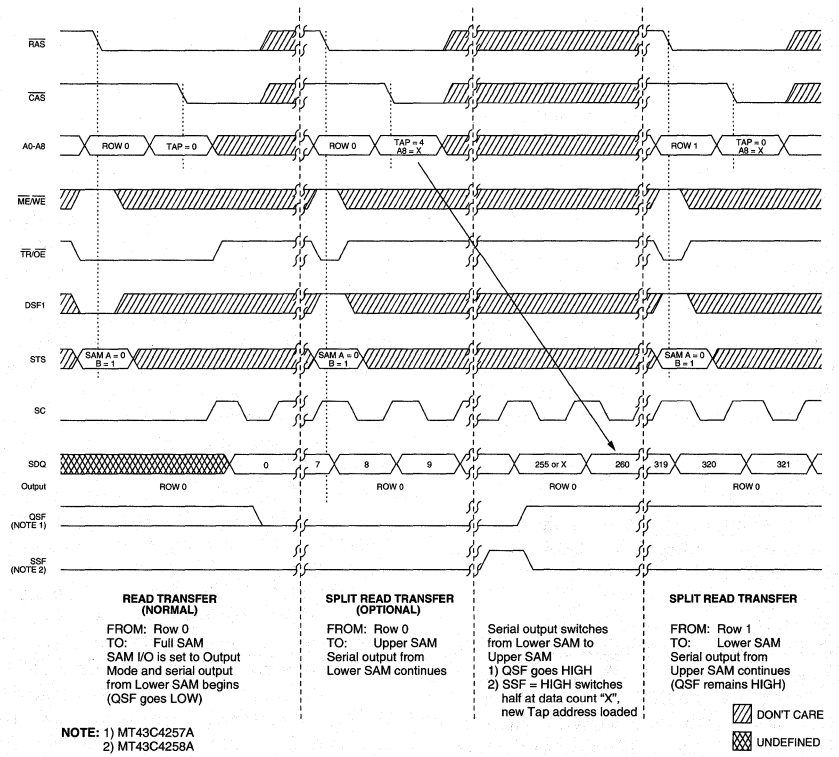


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

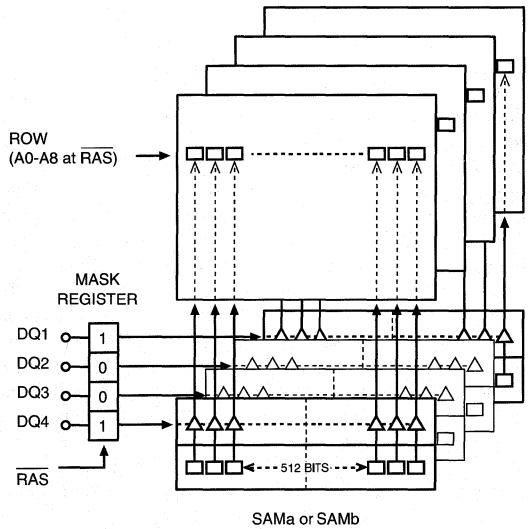


Figure 5
DQ MASKED WRITE TRANSFER

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the four DQ planes (see Figure 5). The MWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The DQ MASKED SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, an MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all four of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every MSWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the four DRAM DQ planes. For example, DQ1, at $\overline{RAS}$ time, during a MASKED WRITE enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A7) for the other half is loaded when $\overline{CAS}$ falls (A8 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A7, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C4257A) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C4258A in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (255 or 511). If SSF is HIGH at SC before an MSWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C4257A.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, $\overline{SE}$a,b and SSFa,b (MT43C4258A). The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

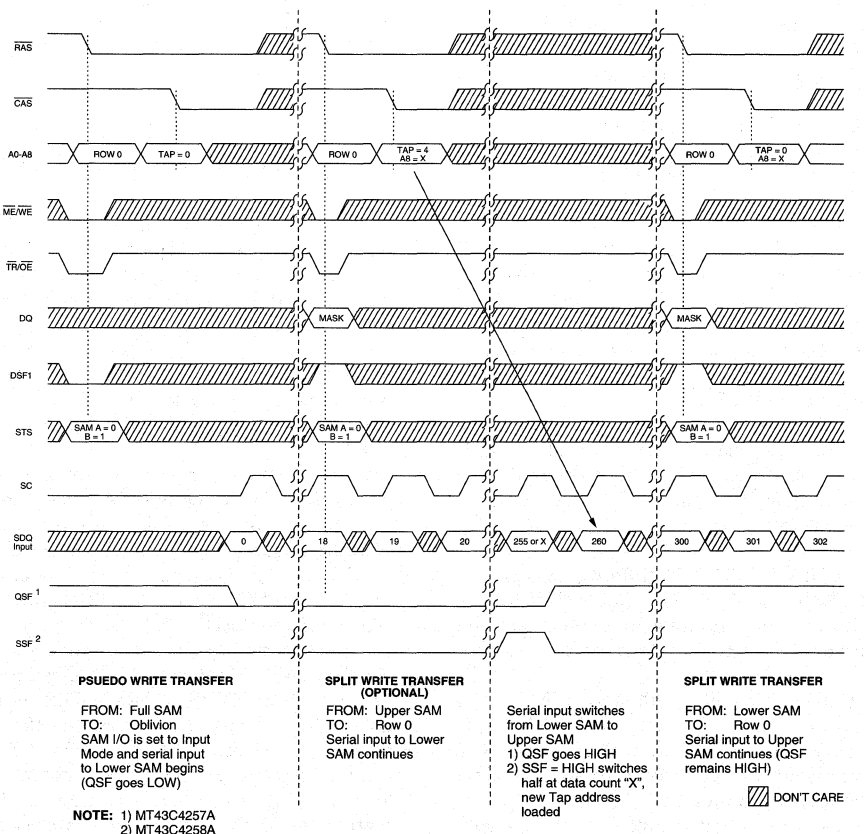


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

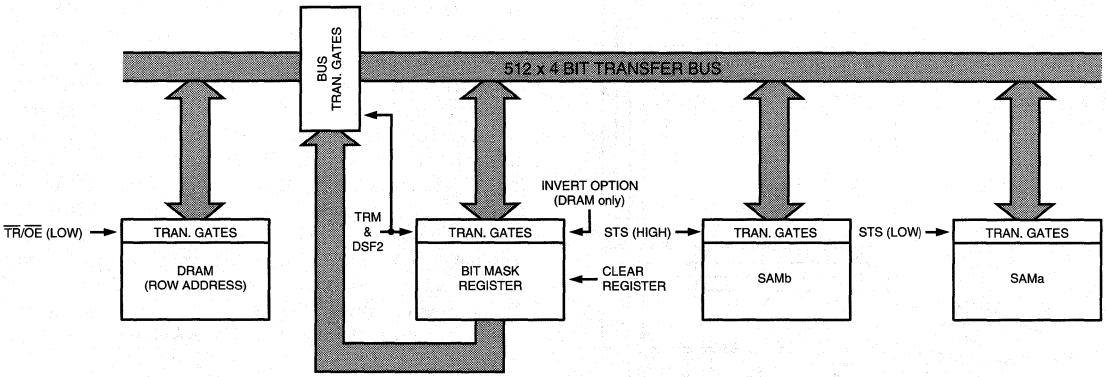


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial Tap address that was loaded in the SAMa,b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C4257A, the address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. The address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

For the MT43C4258A, the address count will wrap as it does for the MT43C4257A, or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input. The operation of SSF (MT43C4258A) is the same as described for serial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONS, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 512 x 4 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

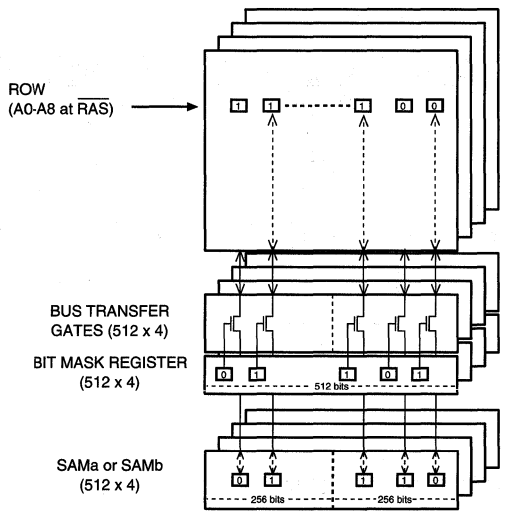


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH to select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 256 SAM bits for that row half will be masked by the corresponding 256 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

DQ MASKED BIT MASKED WRITE TRANSFER (BMWT-DQM)

The BMWT-DQM cycle is nearly identical to the BIT MASKED WRITE TRANSFER, except TRM is LOW and DSF1 is HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMWT-DQM operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 512 SAM bits for that DQ plane will be transferred to the DRAM row selected. If a DQ input is HIGH, the 512 SAM bits for that row will be masked by the corresponding 512 mask register bits when written to the selected DRAM row. The remaining control timing is identical to the requirements for a normal WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR contents. Data may be inverted when being transferred between the BMR and DRAM also.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the BMR by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}$/($\overline{OE}$) is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the serial mask input (SMI) feature is enabled (see the Functional Truth

Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). When $\overline{RAS}$ falls, MKD is LOW to disable SMI, or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the four bit-planes, the data on the MKD pin is written to each bit plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. To select a write transfer from the BMR, $(\overline{ME})/\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM, instead of the DRAM, is the source of the data. $(\overline{ME})/\overline{WE}$ is used to indicate the direction of the transfer, and must be LOW when $\overline{RAS}$ falls for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, the ROW-address present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The $(\overline{ME})/\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bits LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/(\overline{OE})$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are HIGH when $\overline{RAS}$ falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the serial mask input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a

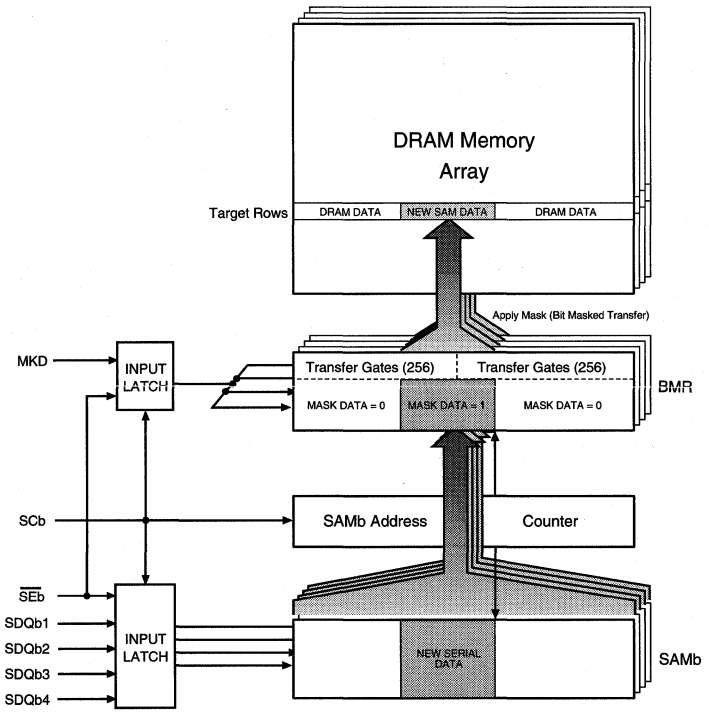


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all four of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR; the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at $\overline{RAS}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all four planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER or DQ-MASKED BIT-MASKED-WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER or DQ-MASKED BIT-MASKED-WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear only half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be

written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 16.7ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (MIN), eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of ($\overline{TR}$)/$\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power-up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQs) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C4257A) outputs power up in a LOW state. The SAMs, as well as the bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE [1]

		$\overline{RAS}$ FALLING EDGE									$\overline{CAS}$ FALL	A0-A8[2]		DQ1-DQ4[3]		REGISTERS	
CODE	FUNCTION	$\overline{CAS}$	$\overline{TR}$/$\overline{OE}$	$\overline{ME}$/$\overline{WE}$[10]	DSF1	DSF2	$\overline{SEa}$, $\overline{SEb}$	TRM	MKD	STS	DSF1	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$,$\overline{WE}$[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	0	X	1[11]	X	X	X	X	X	X	X	X	X	X	X	—	—
ROR	$\overline{RAS}$-ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	—	—
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	—	—
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	—
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	—
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	—	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	—
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	—	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
MSWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH DQ MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

TRUTH TABLE [1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ4[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	—	—
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
BMWT-DQM	DQ/BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	1	1	X	0	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

NOTE:

1. 0 = LOW (V_{IL}); 1 = HIGH (V_{IH}); X = "don't care;" — = "not applicable."
2. These columns show what must be present on the A0-A8 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
3. These columns show what must be present on the DQ1-DQ4 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
4. With WRITE cycles, the input data is latched at the falling edge of $\overline{CAS}$ or $\overline{ME/WE}$, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of $\overline{CAS}$ or $\overline{TR/OE}$, whichever is later.
5. The ROW that is addressed will be refreshed, but no particular row address is required.
6. Tap address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A8 is a "don't care" for SPLIT TRANSFERs.
7. The serial mask input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE, DQ MASKED BIT MASKED WRITE TRANSFER or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and DQ MASKED BIT MASKED WRITE TRANSFERs or BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
9. SPLIT TRANSFERs do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of $\overline{ME/WE}$ at $\overline{RAS}$ time. If $\overline{ME/WE}$ is LOW, then the selected SAM is an input; if $\overline{ME/WE}$ is HIGH, then the SAM is an output (except for SPLIT TRANSFERs).
11. The MT43C4257A/8A operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they be driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ VOUT ≤ Vcc).	IOZ	-10	10	µA	
OUTPUT LEVELS					
Output High Voltage (IOUT = -2.5mA, SDQs; -5mA all other outputs)	VOH	2.4		V	1
Output Low Voltage (IOUT = 2.5mA, SDQs; 5mA all other outputs)	VOL		0.4	V	

CAPACITANCE

($T_A = 25°C$)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD, $\overline{SE}$a,b, DSF1,2, STS	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SCa,b SSFa,b	CI2		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	CI/O		9	pF	2
Output Capacitance: QSFa,b	CO		9	pF	2

TSOP THERMAL CONSIDERATIONS (preliminary)

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	øJA	85	°C/W	
Thermal resistance - Junction to Case	øJC	15	°C/W	
Maximum Case Temperature	TC	110	°C	

NEW ■ TRIPLE-PORT DRAM

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

		MAX			
PARAMETER/CONDITION	**SYMBOL**	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC [MIN])	I_{CC1}	100	90	mA	3, 4 25
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC [MIN])	I_{CC2}	95	85	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles [MIN])	I_{CC3}	8	8	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs ≥ Vcc -0.2V or ≤ Vss +0.2V	I_{CC4}	2	2	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	105	90	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	105	90	mA	3, 5 25
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	100	90	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

		MAX			
PARAMETER/CONDITION	**SYMBOL**	**-7**	**-8**	**UNITS**	**NOTES**
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; ^tSC = ^tSC [MIN]; $\overline{SE}a/\overline{SE}b$ = V_{IL})	I_{CC8}	40	35	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^tSC = ^tSC [MIN]; $\overline{SE}b$ = V_{IL})	I_{CC9}	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = V_{IH} or V_{IL}; $\overline{SE}a/\overline{SE}b$ = V_{IH})	I_{CC10}	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = V_{IH} or V_{IL}; $\overline{SE}b$ = V_{IH})	I_{CC11}	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC1-7}) + SAMa CURRENT (I_{CC8} or I_{CC10}) + SAMb CURRENT (I_{CC8} or I_{CC10}) + SMI CURRENT (I_{CC9} or I_{CC11}) (+ 10mA [If DRAM CURRENT = I_{CC3} or I_{CC4}])

Example 1:
Operating current (-8) with DRAM operating in FAST-PAGE-MODE, SAMa active, SAMb and SMI inactive:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC2}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC10}) + SMI CURRENT (I_{CC11}) [+ 0] = 85 + 35 + 0 + 0 = 120mA (MAX)

Example 2:
Operating current (-7) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC4}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC8}) + SMI CURRENT (I_{CC9}) [+ 10] = 2 + 40 + 40 + 20 + 10 = 112mA (MAX)

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	^tRWC	170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	90		95		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14, 17
Access time from $\overline{CAS}$	^tCAC		17		20	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		20	ns	
Access time from column address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	70	20,000	80	20,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	10		12		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	17	40	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	12		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	ns	20, 23
Output disable	^tOD	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	^tOEH	10		15		ns	27
Output Enable to $\overline{RAS}$ delay	^tORD	0		0		ns	

NEW ■ TRIPLE-PORT DRAM

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		60		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		40		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR refresh)	^tCHR	10		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	60		70		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		25		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	7	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
$\overline{RAS}$ to SD buffer turn on time	^tSRO	10		10		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		60		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	55		60		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
SC to QSF delay time	^tSQD		20		20	ns	28
$\overline{RAS}$ to QSF delay time	^tRQD		65		65	ns	28
$\overline{CAS}$ to QSF delay time	^tCQD		35		35	ns	28
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25	ns	28
SPLIT TRANSFER setup time	^tSTS	25		30		ns	28
SPLIT TRANSFER hold time	^tSTH	0		0		ns	28

NEW TRIPLE-PORT DRAM

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

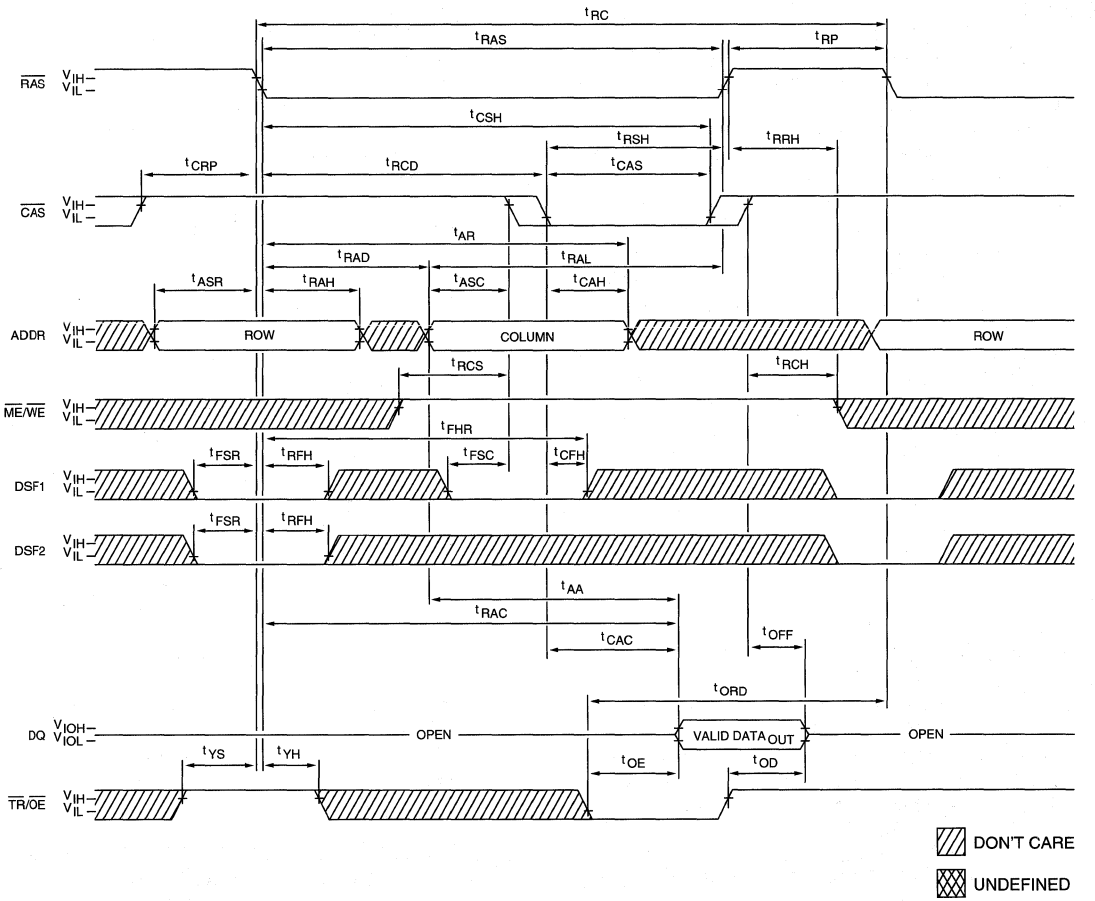
AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time (Read)	^tSCR	22		25		ns	
Serial clock cycle time (Write)	^tSCW	20		20		ns	
Access time from SC	^tSAC		22		25	ns	24, 30
SC precharge time (SC LOW time)	^tSP	7		7		ns	
SC pulse width (SC HIGH time)	^tSAS	7		7		ns	
Access time from $\overline{SE}$	^tSEA		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	10		10		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		ns	24, 30
Serial output buffer turn off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24
Serial data in setup time	^tSDS	0		0		ns	24
Serial data in hold time	^tSDH	10		10		ns	24
Serial mask data in setup time	^tMDS	0		0		ns	
Serial mask data in hold time	^tMDH	10		10		ns	
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	10		15		ns	
SERIAL INPUT (Write) disable setup time	^tSWIS	0		0		ns	
SERIAL INPUT (Write) disable hold time	^tSWIH	10		15		ns	
SSF to SC setup time	^tSFS	0		0		ns	29
SSF to SC hold time	^tSFH	10		15		ns	29
SSF LOW to SC HIGH delay	^tSFD	5		5		ns	29

NOTES

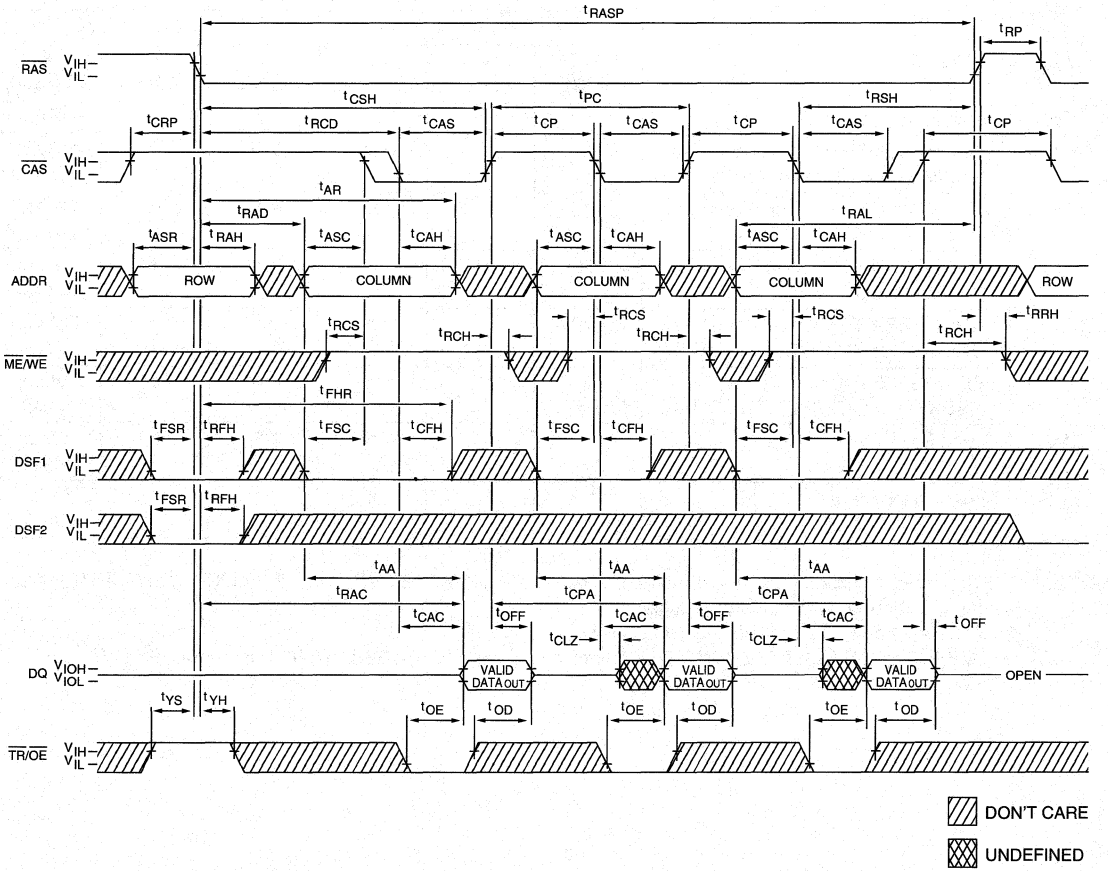
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±5%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 3 to 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data outputs (DQ1-DQ4) are High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data outputs (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^tWCS ≤ ^tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Addresses (A0-A8) change two times or less while $\overline{RAS}$ = V_{IL}.
26. Addresses (A0-A8) change once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. Applies to the MT43C4257A only.
29. Applies to the MT43C4258A only.
30. ^tSAC is MAX at 70° C and 4.75V Vcc; ^tSOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^tSOH = ^tSAC - output transition time, this is guaranteed by design.

NEW ■ TRIPLE-PORT DRAM

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE

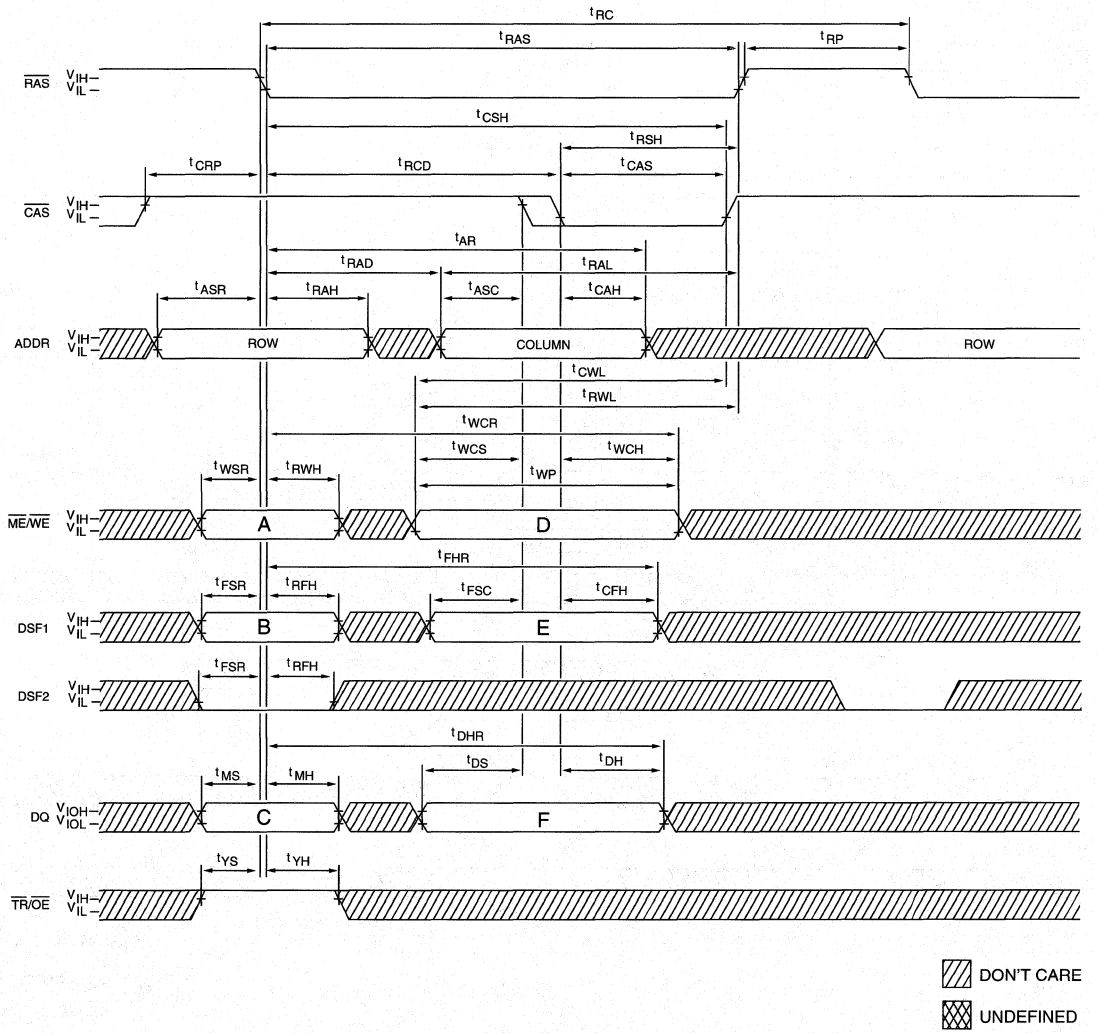


WRITE CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES[2]					
		RAS Falling Edge			CAS Falling Edge		
		A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1[3]	0	DRAM (Masked)
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1[3]	0	DRAM (Masked)
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	X	0/1[3]	1	Column Mask
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1[3]	1	Column Mask
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	0/1[3]	1	Column Mask
LMR	Load Mask Data Register	1	1	X	0/1[3]	0	Write Mask
LCR	Load Color Register	1	1	X	0/1[3]	1	Color Mask

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2. TRM, MKD and STS are "don't care" for all WRITE cycles.
3. If $\overline{ME}/\overline{WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME}/\overline{WE}$ falls after $\overline{CAS}$.

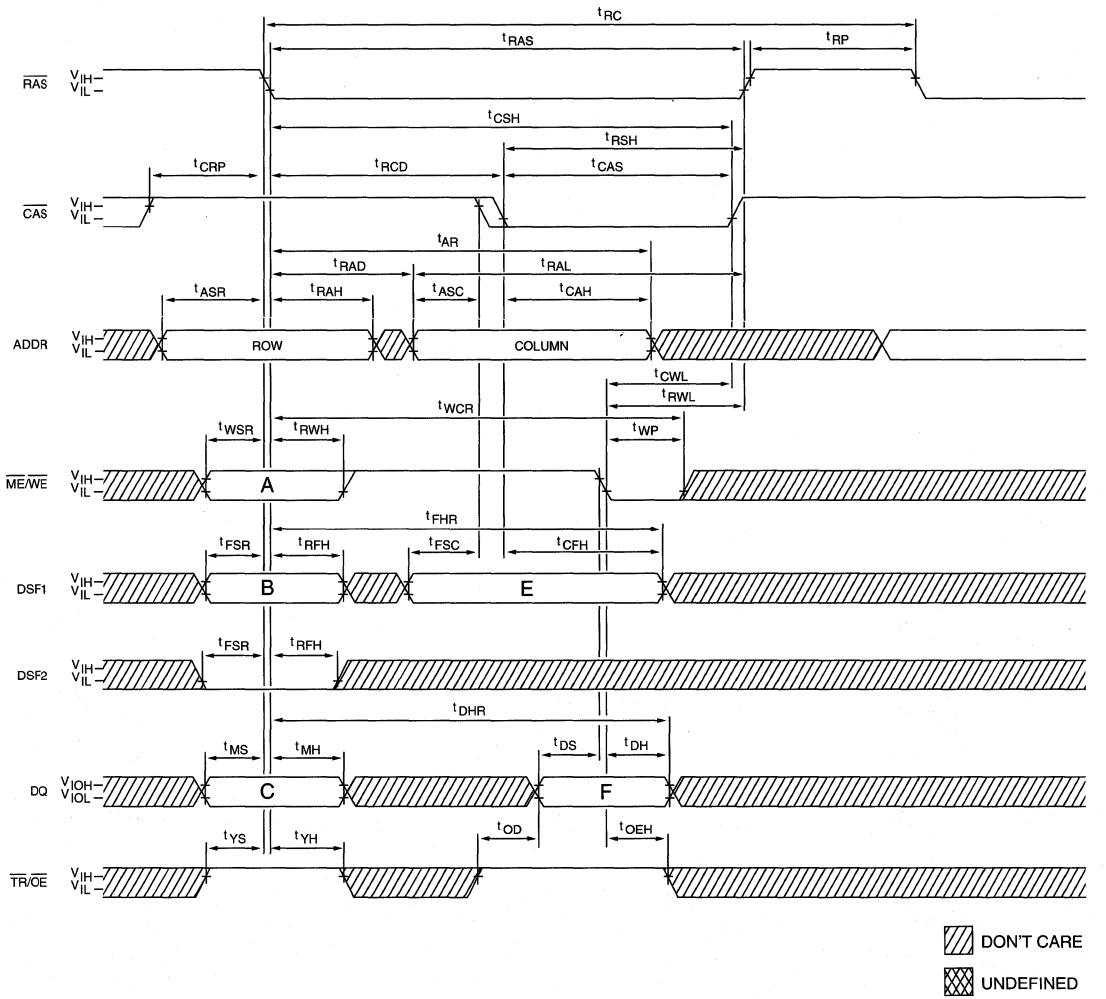
DRAM EARLY-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

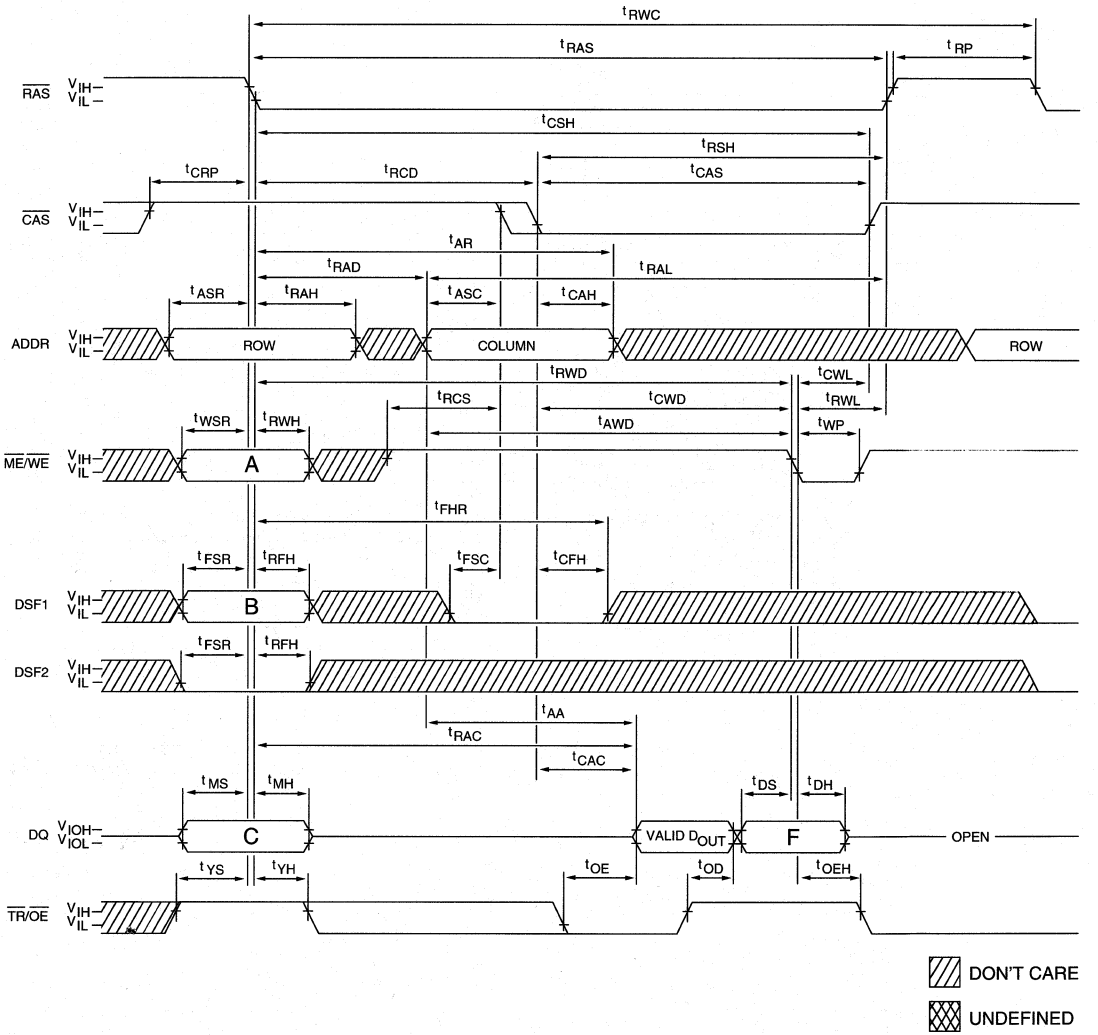
NEW TRIPLE-PORT DRAM

DRAM LATE-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

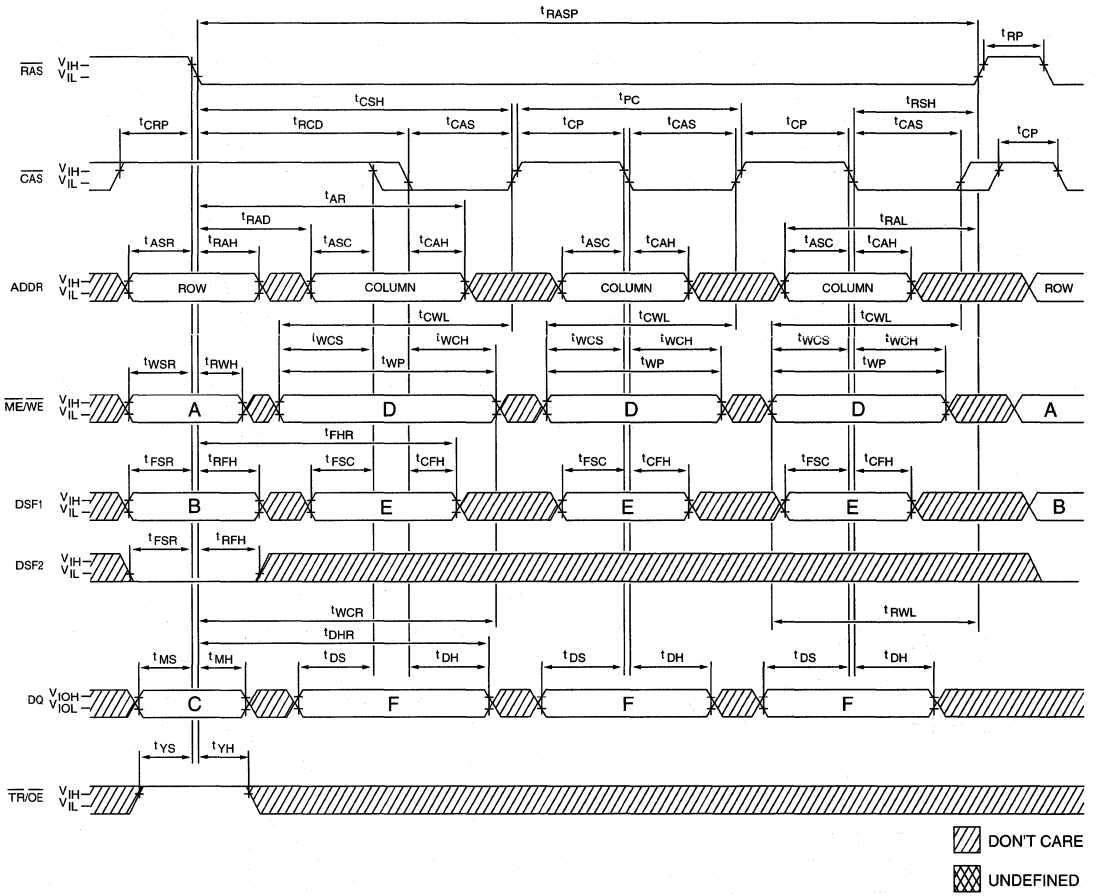
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW ■ TRIPLE-PORT DRAM

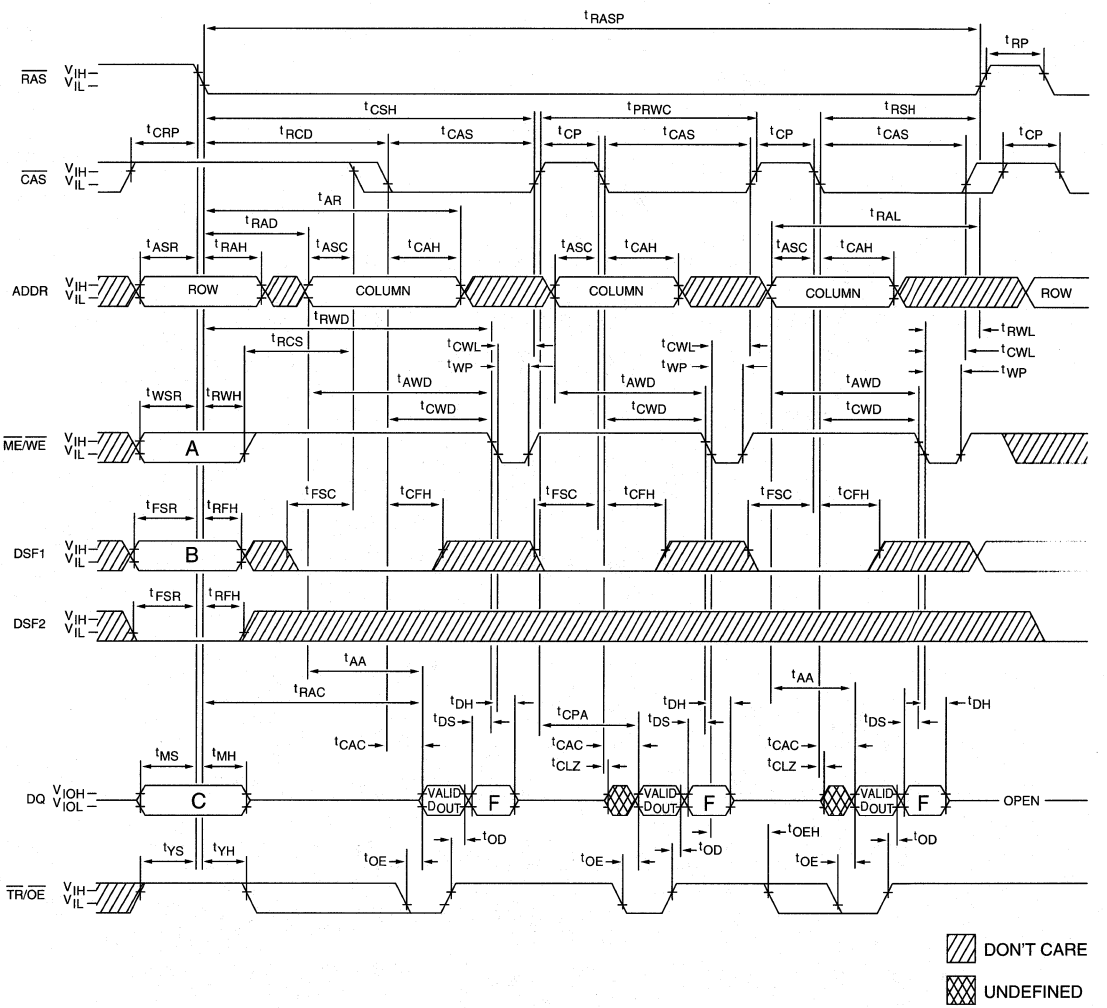
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST-PAGE-MODE.

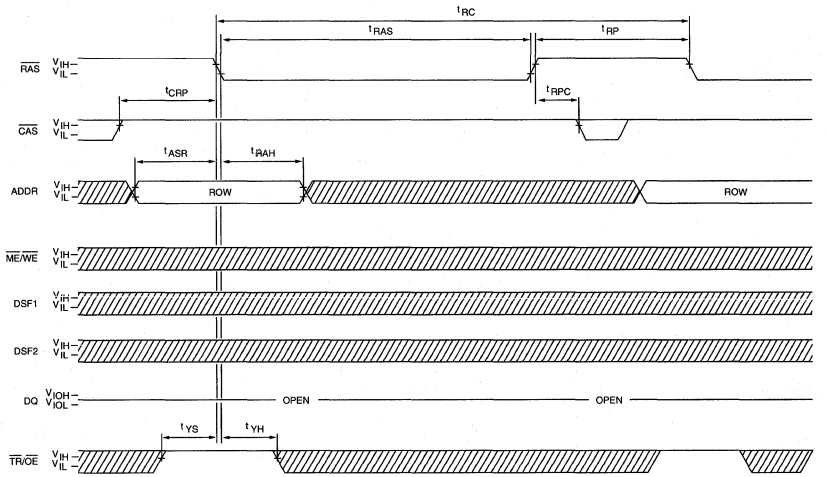
2. The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

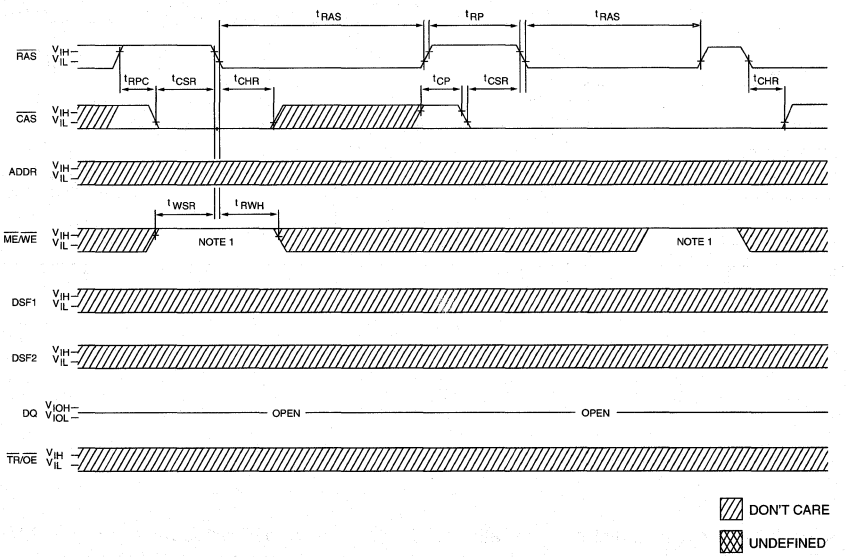


NOTE: 1. READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2. The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

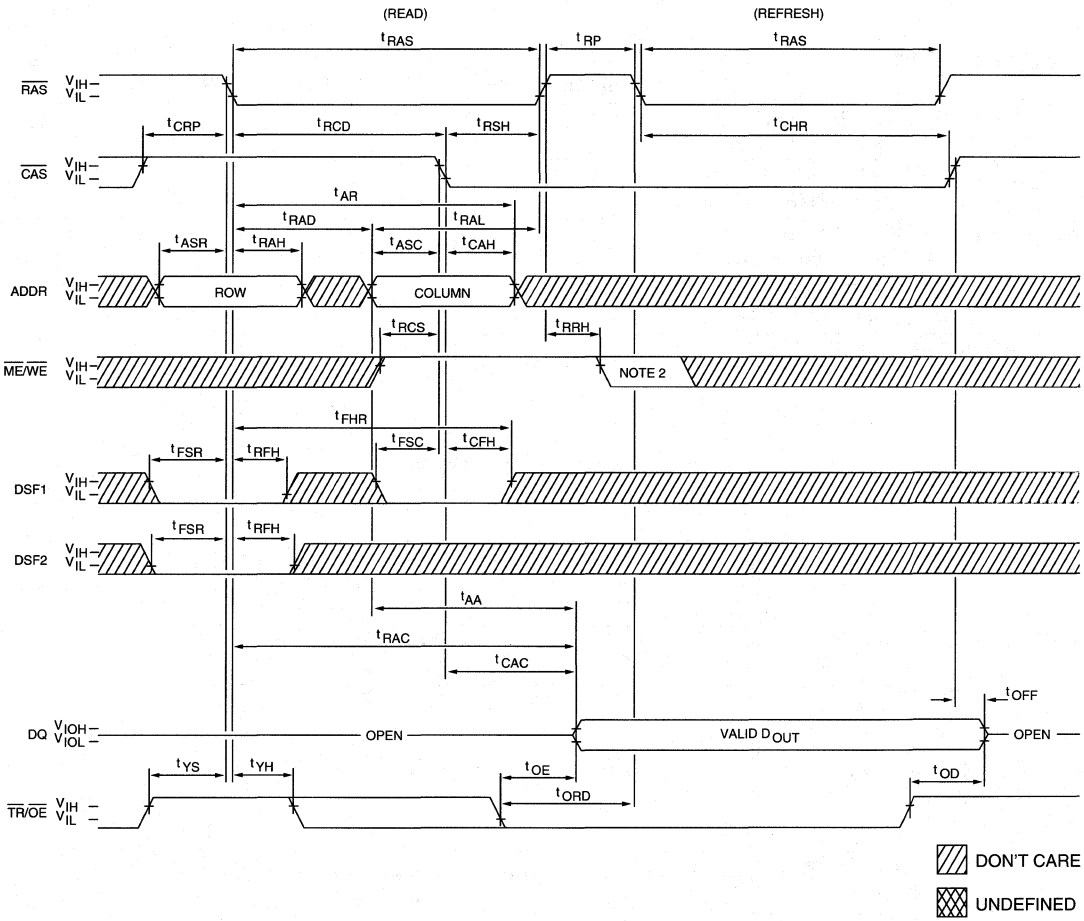


CBR REFRESH CYCLE



NOTE: 1. The MT43C4257A/8A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

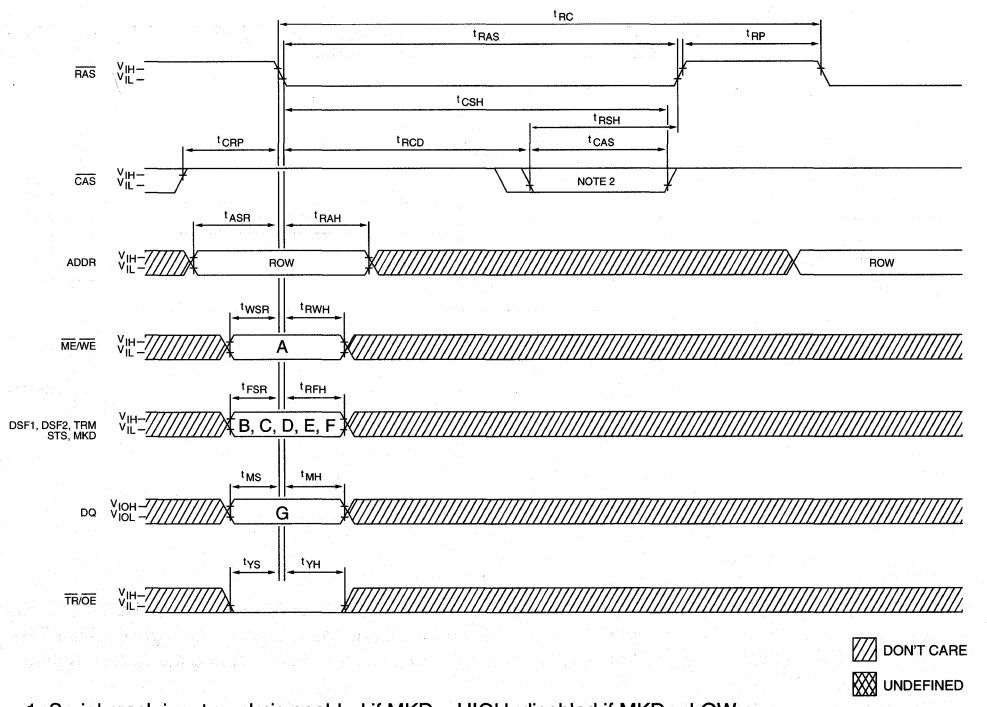


NOTE:
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The MT43C4257A/8A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES						
		RAS Falling Edge						
		A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/1[1]	X
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/1[1]	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/1[1]	Mask
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/1[1]	Mask
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	X	0/1[1]	X

DRAM/BMR TRANSFERS



NOTE: 1. Serial mask input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.

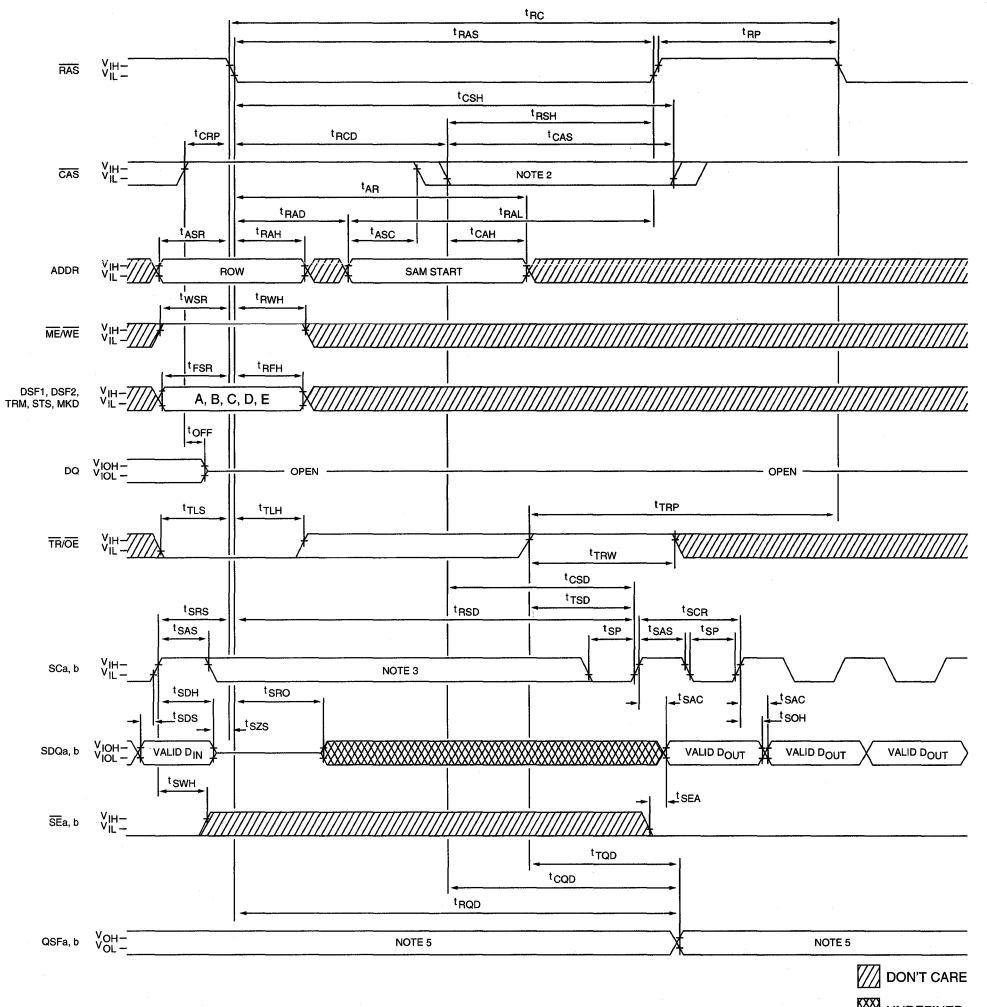
READ TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES				
		$\overline{RAS}$ Falling Edge				
		A DSF1	B DSF2	C TRM	D STS	E MKD
RW	READ TRANSFER	0	0	0	0/1[2]	X
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/1[2]	X
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/1[2]	X
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1	1	0/1[2]	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/1[2]	0/1[3]

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
3. Serial mask input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

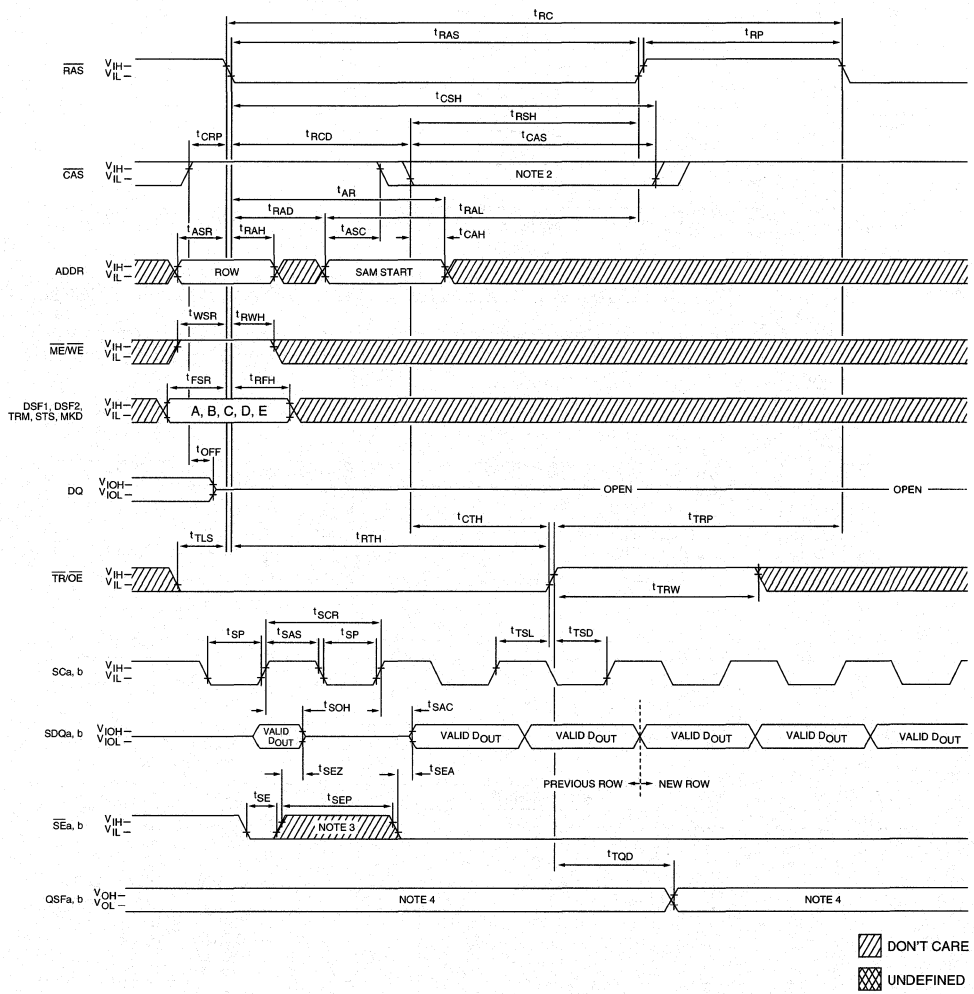
NEW TRIPLE-PORT DRAM

READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. SSFa, b = "don't care" (MT43C4258A).
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.

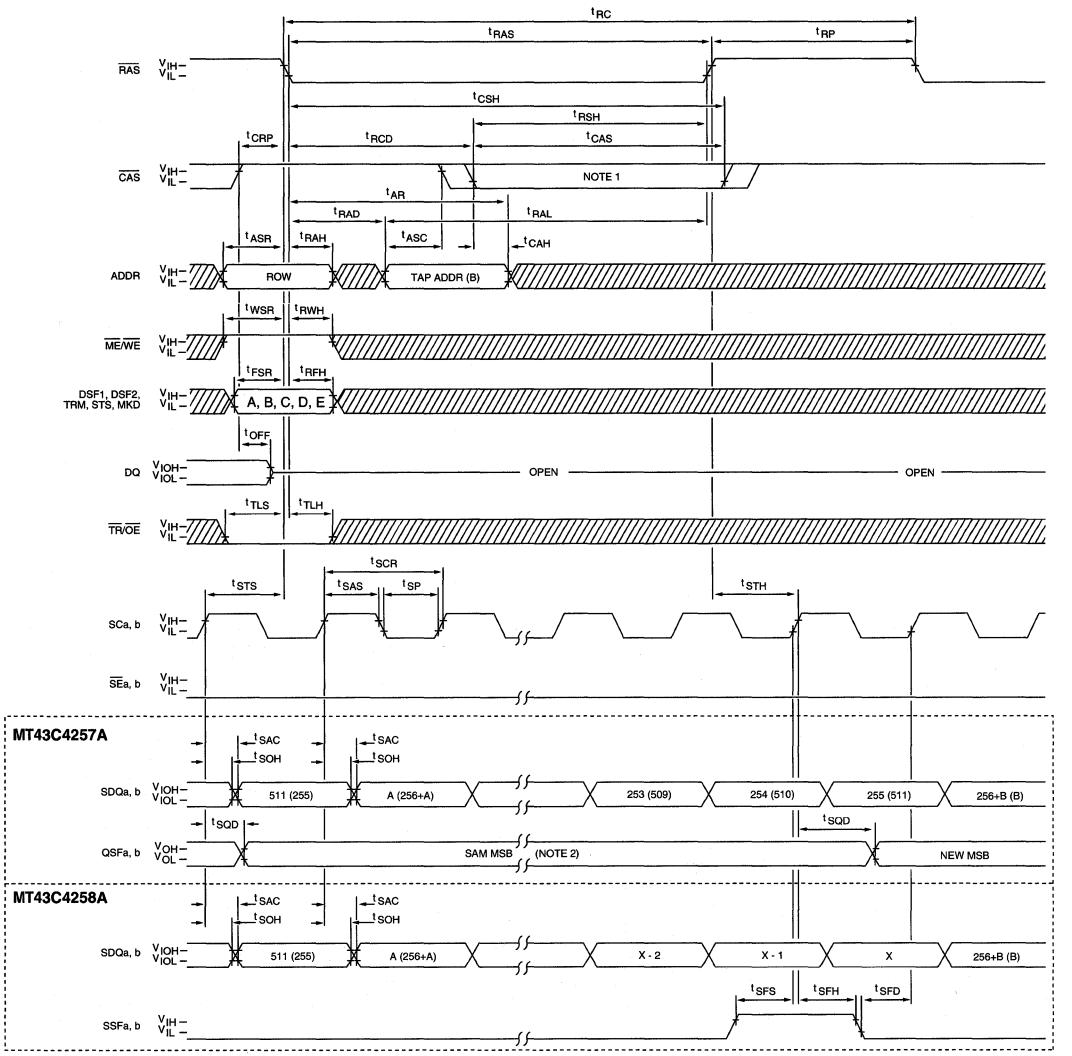
REAL-TIME READ TRANSFER [1, 5]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. SSFa, b = "don't care" (MT43C4258A).
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed.
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
5. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

NEW TRIPLE-PORT DRAM

SPLIT READ TRANSFER [3]
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

WRITE TRANSFER CYCLE FUNCTION TABLE [1]

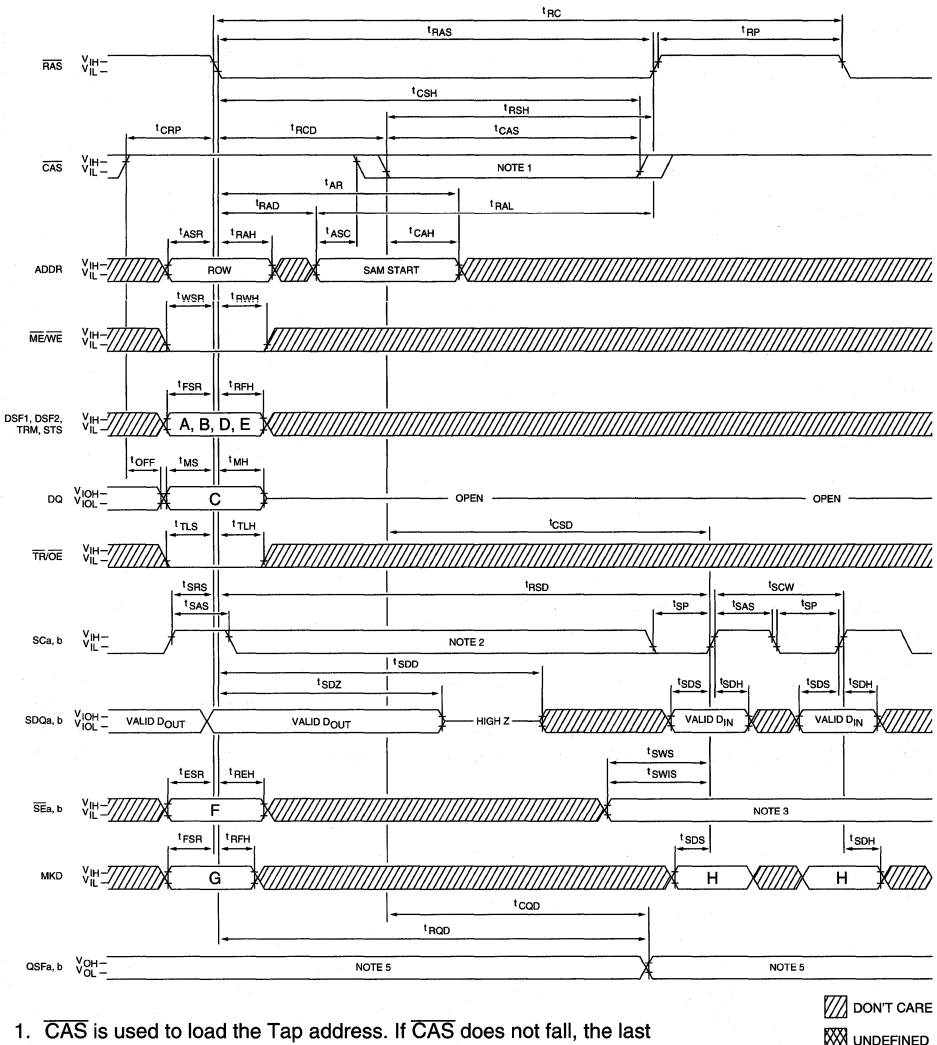
CODE	FUNCTION	LOGIC STATES							
		$\overline{RAS}$ Falling Edge							SC
		A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	X	0	0/1[2]	0	X	-
PWT	PSEUDO WRITE TRANSFER	0	0	X	0	0/1[2]	1	X	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/1[2]	X	X	-
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/1[2]	X	X	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	X	1	0/1[2]	X	X	0/1[4]
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/1[2]	X	X	0/1[4]
SAM-BMR	(SAM→BMR) TRANSFER	1	0	X	1	0/1[2]	X	0/1[3]	-
BMWT-DQM	DQ/BIT MASKED WRITE TRANSFER (SAM→DRAM)	1	1	Mask	0	0/1[2]	X	X	0/1[4]

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" , "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
3. Serial mask input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

NEW TRIPLE-PORT DRAM

WRITE TRANSFER [4]

(When part was previously in the SERIAL OUTPUT mode)

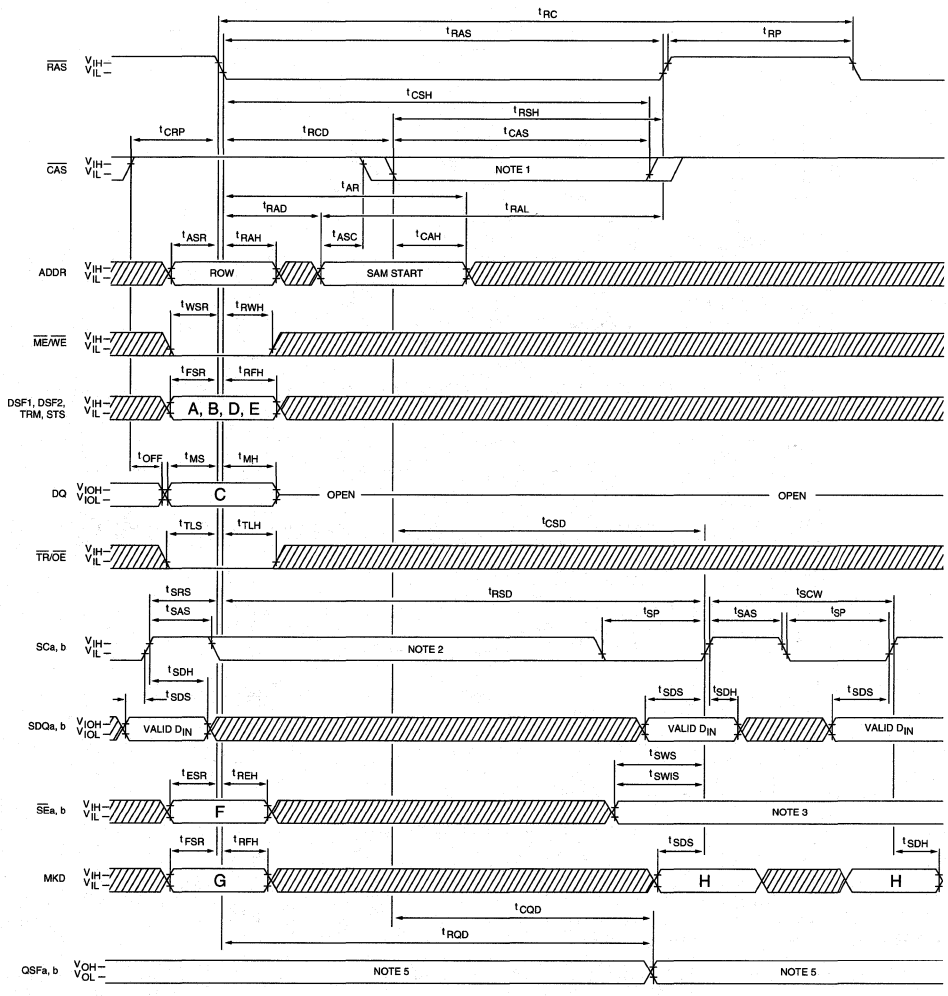


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258A).

WRITE TRANSFER [4]

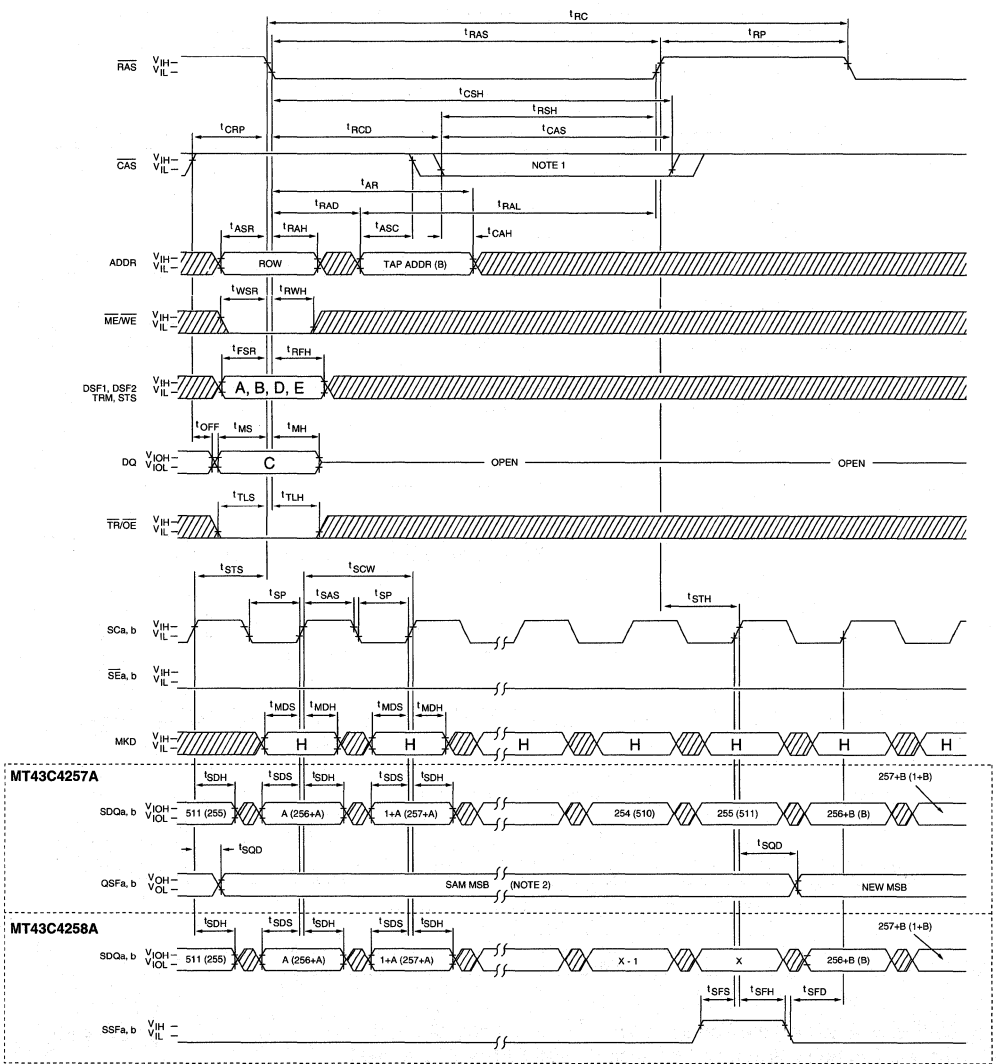
(When part was previously in the SERIAL INPUT mode)



NOTE:

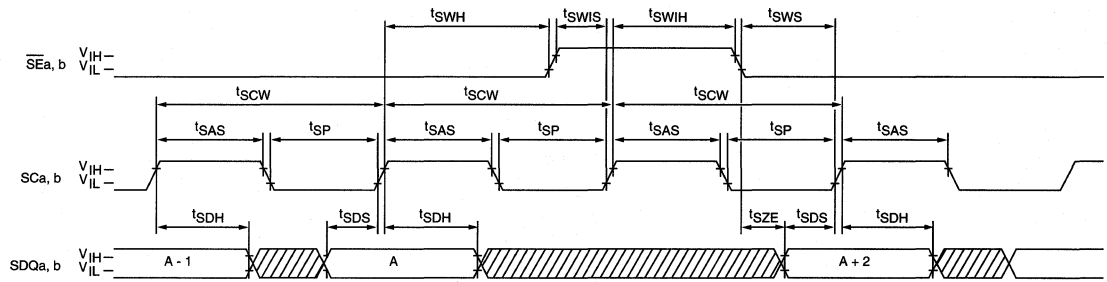
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258A).

SPLIT WRITE TRANSFER [3]
(SPLIT SAM-TO-DRAM TRANSFER)

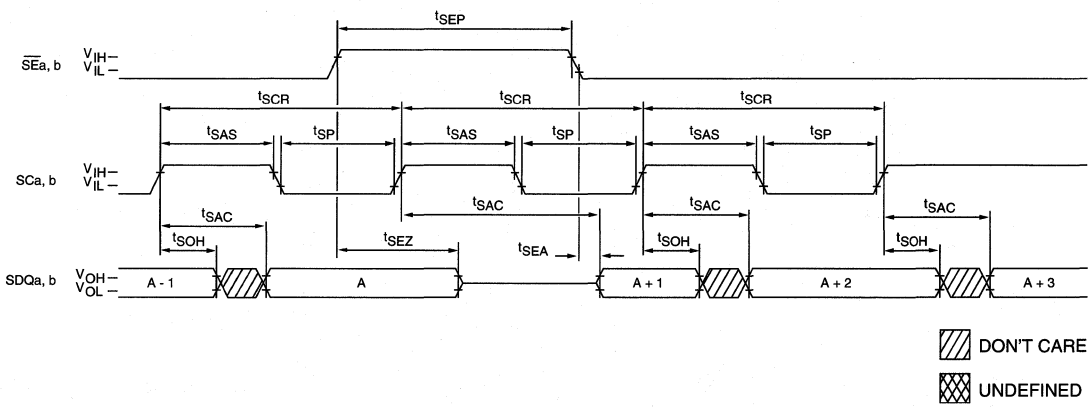


NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE : $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

TRIPLE-PORT DRAM

128K x 8 DRAM WITH DUAL 256 x 8 SAMS

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMs
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 550mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST-PAGE-MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

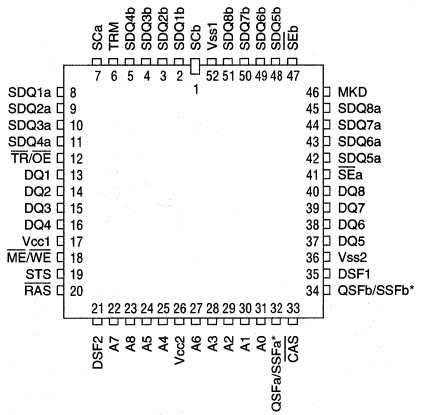
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS — MARKING

- Timing (DRAM, SAMs [cycle/access])
  80ns, 28ns/25ns — -8
  100ns, 30ns/27ns — -10
- Packages
  Plastic LCC (750 mil) — EJ
- Functionality
  QSF output — MT43C8128
  (indicates SAM half accessed)
  SSF input — MT43C8129
  (Split SAM special function, stop count)
- Part Number Example: MT43C8128EJ-8

PIN ASSIGNMENT (Top View)

52-PIN PLCC
(SDD-1)



*MT43C8128/MT43C8129

GENERAL DESCRIPTION

The MT43C8128/9 are high-speed, triple-port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048-bit-wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

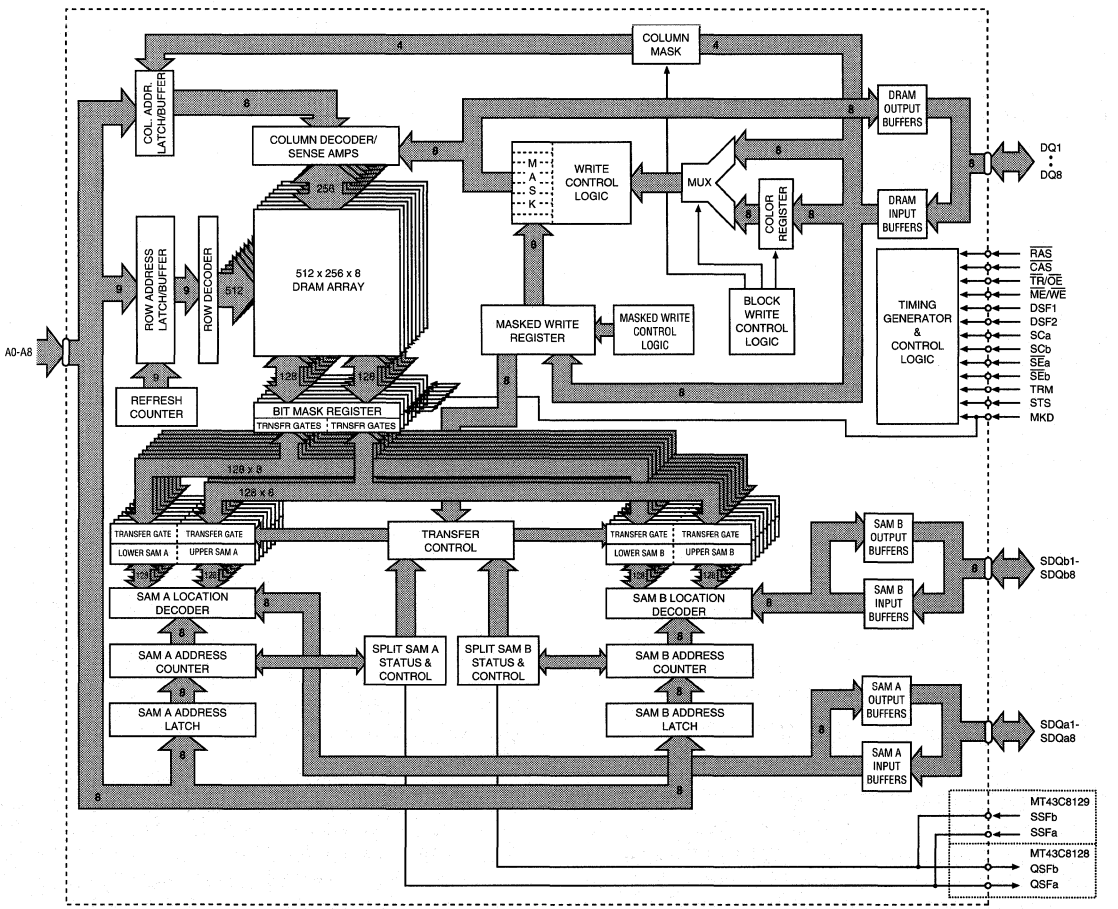
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit bit mask data register may be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128/9 are optimized for high performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, video windowing, serial/parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



TRIPLE-PORT DRAM

128K x 8 DRAM WITH DUAL 256 x 8 SAMS

NEW ■ TRIPLE-PORT DRAM

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times: 70ns random, 22ns serial
- Operation and control compatible with 1 Meg VRAMs
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 550mW active, typical
- 512-cycle refresh within 16.7ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST-PAGE-MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS MARKING

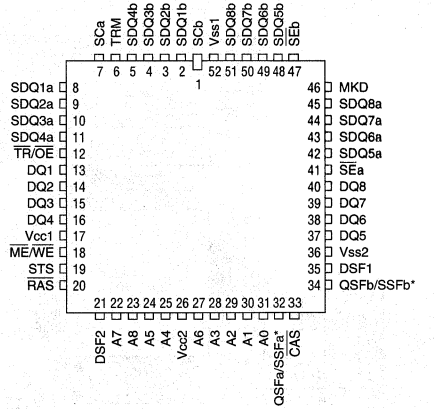
- Timing (DRAM, SAMs [read cycle/write cycle])
  70ns, 22ns/20ns -7
  80ns, 25ns/20ns -8
- Packages
  Plastic LCC (750 mil) EJ
- Functionality
  QSF output MT43C8128A
  (indicates SAM half accessed)
  SSF input MT43C8129A
  (Split SAM special function, stop count)
- Part Number Example: MT43C8128AEJ-7

GENERAL DESCRIPTION

The MT43C8128A/9A are high-speed, triple-port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

PIN ASSIGNMENT (Top View)

52-PIN PLCC
(SDD-1)



*MT43C8128A/MT43C8129A

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048 bit wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

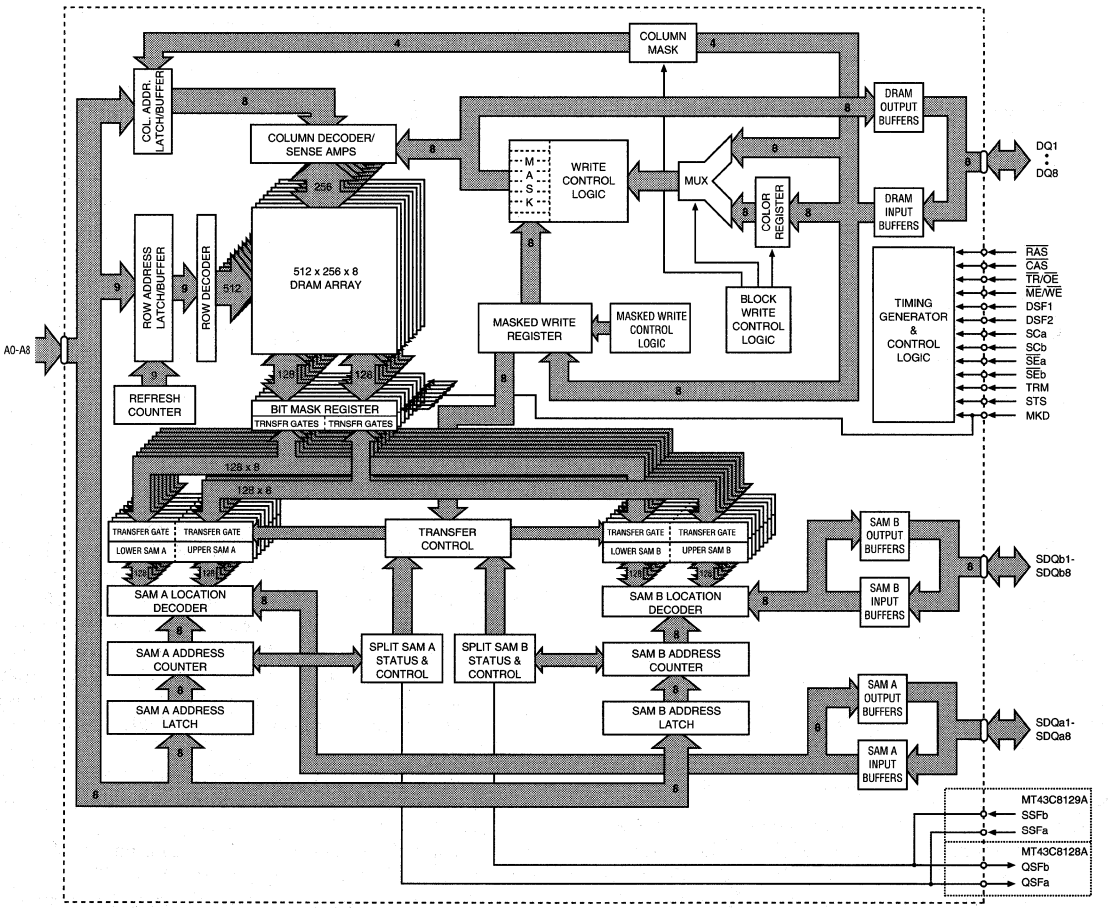
Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit bit mask data register may be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

NEW ■ TRIPLE-PORT DRAM

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128A/9A are optimized for high-performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, video windowing, serial/parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
7	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
12	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
18	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME}/\overline{WE}$ is also used to select a READ ($\overline{ME}/\overline{WE}$ = H) or WRITE ($\overline{ME}/\overline{WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME}/\overline{WE}$ = H) or WRITE TRANSFER ($\overline{ME}/\overline{WE}$ = L).
41	$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
47	$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
35	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
21	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
20	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the control and data inputs.
33	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR}/\overline{OE}$), and strobe control inputs and data inputs.

NEW ■ TRIPLE-PORT DRAM

PIN DESCRIPTIONS (continued)

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
31, 30, 29, 28, 25, 24, 27, 22, 23	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
19	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
46	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
6	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
13, 14, 15, 16, 37, 38, 39, 40	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
8, 9, 10, 11, 42, 43, 44, 45	SDQa1-SDQa8	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 4, 5, 48, 49, 50, 51	SDQb1-SDQb8	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
32	QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C8128A): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C8129A): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
34	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C8128A): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C8129A): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
17, 26	Vcc	Supply	Power Supply: +5V ±5%
52, 36	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C8128A/9A may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C8128A/9A TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT43C8128A/9A support CBR, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data but must simply perform 512 CBR cycles within the 16.7ms time period.

For $\overline{RAS}$-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the $\overline{RAS}$ ONLY and CBR cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling $\overline{RAS}$ (while keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C8128A/9A are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column-address bits (A0-A7) are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the TPDRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{TR}/(\overline{OE})$ is used when $\overline{RAS}$ goes LOW to select between DRAM and TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

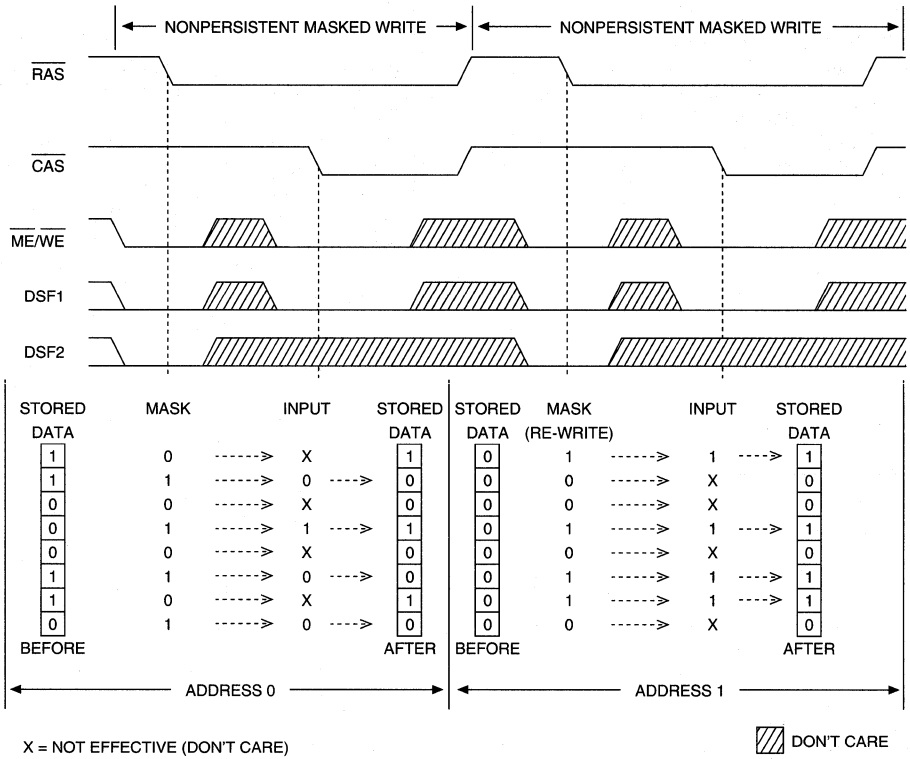


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an 8-bit word. The MT43C8128A/9A support two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C8128A/9A. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ or ($\overline{ME}$)/$\overline{WE}$ go LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST-PAGE-MODE may be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

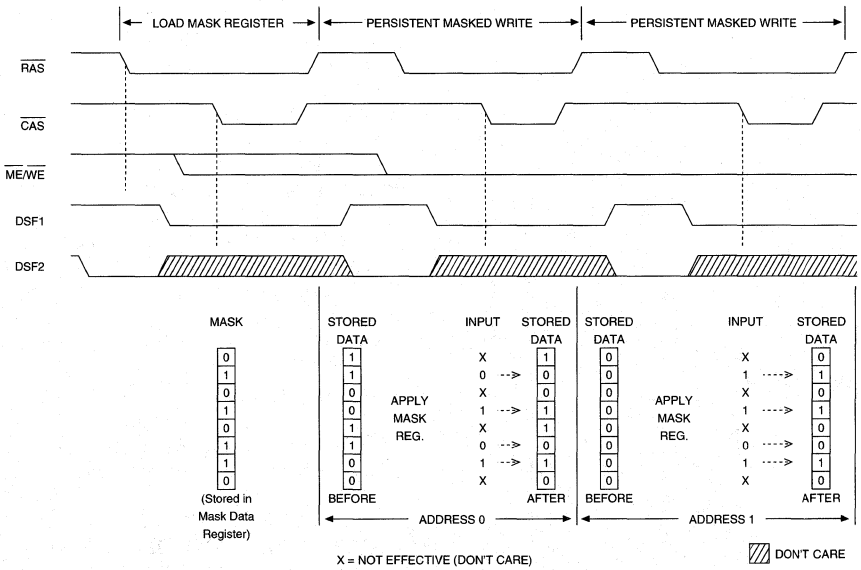


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description). PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs.

Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST-PAGE-MODE.

BLOCK WRITE (BW)

If DSF1 is HIGH when $\overline{CAS}$ goes LOW, the MT43C8128A/9A will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 32 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" (out of the 64 possible) of four adjacent column locations that will be accessed. When the latter of $\overline{ME}/\overline{WE}$ and $\overline{CAS}$ go LOW, the DQ inputs latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color

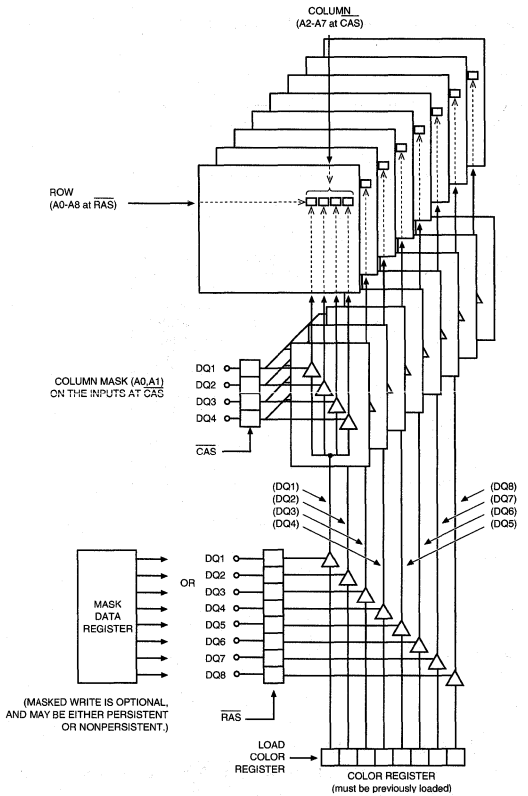


Figure 3
BLOCK WRITE EXAMPLE

register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the eight column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C8128A/9A contain two 8-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable WRITEs to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A WRITE is referenced to the DRAM array and a READ is referenced from the array.

Note: *The three ports of the TPDRAM are independent of, and asynchronous to, one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C8128A/9A include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a TRANSFER operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C8128A/9A support all of the popular transfer cycles available on Micron's 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{ME})/\overline{WE}$ is HIGH, and DSF1, DSF2 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row-address bits indicate the eight 256-bit DRAM rows that are to be transferred to the eight SAM data registers. The column-address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW if the lower half; HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAMs I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ-TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the ^{t}RSD and ^{t}CSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 8-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (nonsplit) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT may be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that

receives the transfer. When $\overline{CAS}$ falls, address pins A0-A6 determine the Tap address for the SAM-half selected; A7 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is ≠ 0. For the MT43C8128A, serial access continues, and when the SAM address counter reaches 127 ("A7" = 1, A0-A6 = 0), the QSF output for that SAM goes HIGH. Then the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C8129A. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (127; lower, 255; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–127) is being accessed. QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

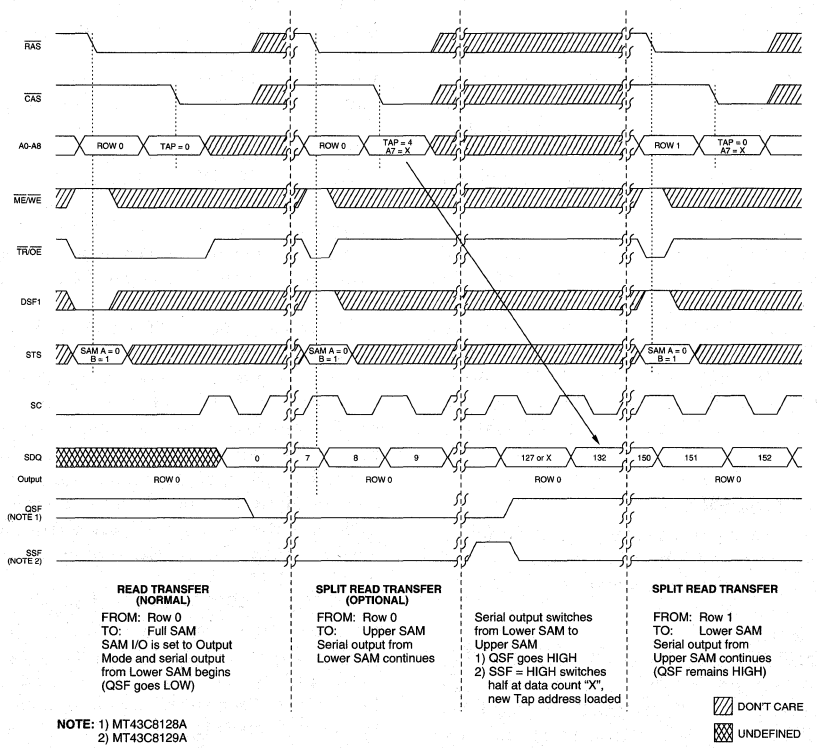


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the eight DQ planes (see Figure 5). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, an MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM

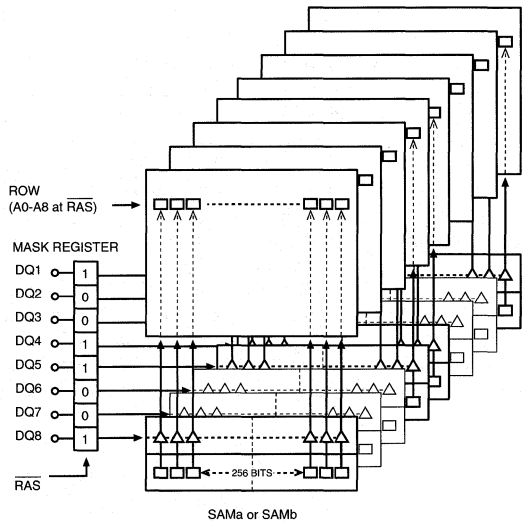


Figure 5
DQ MASKED WRITE TRANSFER

may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all eight of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, and it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every SWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the eight DRAM DQ planes. For example, DQ1, at $\overline{RAS}$ time, during a DQ1 MASKED WRITE, enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A6) for the other half is loaded when $\overline{CAS}$ falls (A7 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A6, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C8128A) indicate which half of SAMa or SAMb, respectively, is currently accepting

data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C8129A in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked-in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (127 or 255). If SSF is HIGH at SC before an MSWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not preceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C8128A.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, $\overline{SE}$a,b and SSFa,b (MT43C8128A). The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

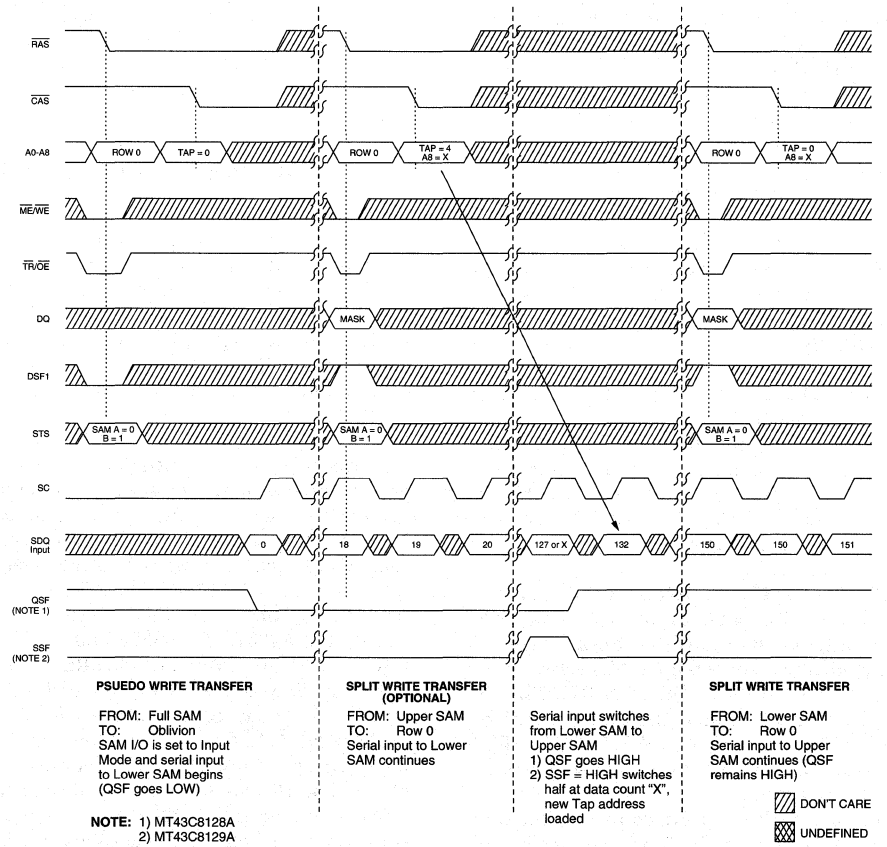


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

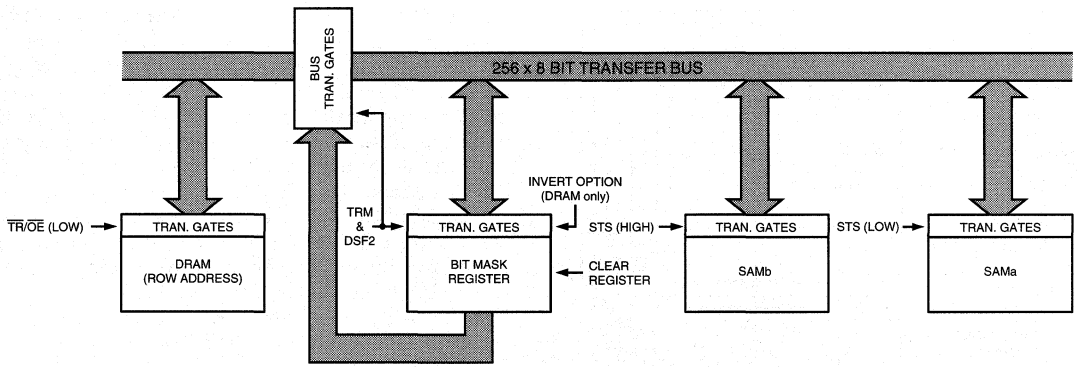


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial Tap address that was loaded in the SAMa,b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C8128A, the address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes. For the MT43C8129A, the address count will wrap as it does for the MT43C8128A or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a WRITE ENABLE for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input. The operation of SSF (MT43C8129A) is the same as described for serial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONs, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 256 x 8 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

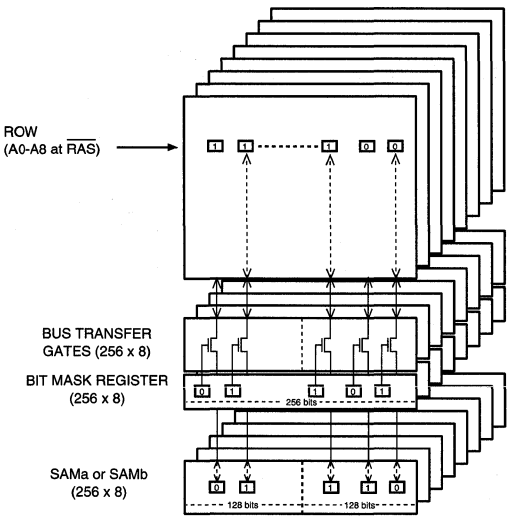


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 128 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 128 SAM bits for that row-half will be masked by the corresponding 128 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

DQ MASKED BIT MASKED WRITE TRANSFER (BMWT-DQM)

The BMWT-DQM cycle is nearly identical to the BIT MASKED WRITE TRANSFER, except TRM is LOW and DSF1 is HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMWT-DQM operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row selected. If a DQ input is HIGH, the 256 SAM bits for that row will be masked by the corresponding 256 mask register bits when written to the selected DRAM row. The remaining control timing is identical to the requirements for a normal WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR's contents. Data may be inverted when being transferred between the BMR and DRAM also.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the bit mask register by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}/(\overline{OE})$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the Serial Mask

Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when $\overline{RAS}$ falls to disable SMI, or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the eight bit-planes, the data on the MKD pin is written to each bit-plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. To select a write transfer from the BMR, $(\overline{ME})/\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. $(\overline{ME})/\overline{WE}$ is used to indicate the direction of the transfer, and must be LOW when $\overline{RAS}$ falls for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, the ROW address present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The $(\overline{ME})/\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bits LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/(\overline{OE})$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are HIGH when RAS falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal

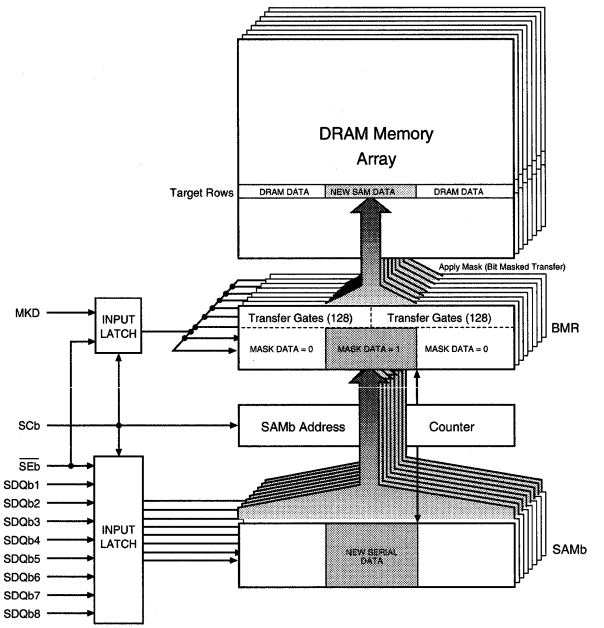


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all eight of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR; the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at $\overline{RAS}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all eight planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER or DQ MASKED BIT MASKED WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER or DQ-MASKED BIT-MASKED-WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear on half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interupted for more than 16.7ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight $\overline{RAS}$ cycles must be executed to initalize the dynamic memory array. When the device is initialized,the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of ($\overline{TR}$)/$\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQ's) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C8128A) outputs power up in a LOW state. Both SAMs as well as bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE [1]

CODE	FUNCTION	$\overline{RAS}$ FALLING EDGE									$\overline{CAS}$ FALL	A0-A8[2]		DQ1-DQ8[3]		REGISTERS	
		$\overline{CAS}$	$\overline{TR}$/$\overline{OE}$	$\overline{ME}$/$\overline{WE}$[10]	DSF1	DSF2	$\overline{SE}$a,$\overline{SE}$b	TRM	MKD	STS	DSF1	$\overline{RAS}$	$\overline{CAS}$, A8=X	$\overline{RAS}$	$\overline{CAS}$,$\overline{WE}$[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	CBR REFRESH	0	X	1[11]	X	X	X	X	X	X	X	X	X	X	X	—	—
ROR	$\overline{RAS}$-ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	—	—
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	—	—
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	—
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	—
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	—	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	—
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	—	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
MSWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER DQ WITH MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

TRUTH TABLE[1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ8[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa,SEb	TRM	MKD	STS	DSF1	RAS	CAS,A8=X	RAS	CAS,WE[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	—	—
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
BMWT-DQM	DQ/BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	1	1	X	0	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

NOTE:

1. 0 = LOW (V_{IL}); 1 = HIGH (V_{IH}); X = "don't care;" – = "not applicable."
2. These columns show what must be present on the A0-A8 inputs when $\overline{RAS}$ falls and A0-A7 when $\overline{CAS}$ falls.
3. These columns show what must be present on the DQ1-DQ8 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
4. With WRITE cycles, the input data is latched at the falling edge of $\overline{CAS}$ or $\overline{ME/WE}$, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of $\overline{CAS}$ or $\overline{TR/OE}$, whichever is later.
5. The row that is addressed will be refreshed, but no particular row address is required.
6. Tap address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A7 is a "don't care" for SPLIT TRANSFERs.
7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE, DQ MASKED BIT MASKED WRITE TRANSFER or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs or DQ MASKED BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
9. SPLIT TRANSFERs do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of $\overline{ME/WE}$ at $\overline{RAS}$ time. If $\overline{ME/WE}$ is LOW, then the selected SAM is an input; if $\overline{ME/WE}$ is HIGH, then the SAM is an output (except for SPLIT TRANSFERs).
11. The MT43C8128A/9A operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they be driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input ($0V \le V_{IN} \le V_{CC}$); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD, $\overline{SE}$a,b, DSF1,2, STS	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SCa,b SSFa,b	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	$C_{I/O}$		9	pF	2
Output Capacitance: QSFa,b	C_O		9	pF	2

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC [MIN])	I_{CC1}	105	95	mA	3, 4 25
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC [MIN])	I_{CC2}	100	90	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles [MIN])	I_{CC3}	8	8	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs ≥ V_{CC} -0.2V or ≤ V_{SS} +0.2V	I_{CC4}	2	2	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	110	95	mA	3, 25
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	110	95	mA	3, 5 25
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	105	95	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; ^tSC = ^tSC [MIN]; $\overline{SE}a/\overline{SE}b$ = V_{IL})	I_{CC8}	45	40	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^tSC = ^tSC [MIN]; $\overline{SE}b$ = V_{IL})	I_{CC9}	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = V_{IH} or V_{IL}; $\overline{SE}a/\overline{SE}b$ = V_{IH})	I_{CC10}	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = V_{IH} or V_{IL}; $\overline{SE}b$ = V_{IH})	I_{CC11}	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC1-7}) + SAMa CURRENT (I_{CC8} or I_{CC10}) + SAMb CURRENT (I_{CC8} or I_{CC10}) + SMI CURRENT (I_{CC9} or I_{CC11}) (+ 10mA [If DRAM CURRENT = I_{CC3} or I_{CC4}])

Example 1:
Operating current (-8) with DRAM operating in FAST-PAGE-MODE, SAMa active, SAMb and SMI inactive:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC2}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC10}) + SMI CURRENT (I_{CC11}) [+ 0] = 90 + 40 + 0 + 0 = 130mA (MAX)

Example 2:
Operating current (-7) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC4}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC8}) + SMI CURRENT (I_{CC9}) [+ 10] = 2 + 45 + 45 + 20 + 10 = 122mA (MAX)

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	90		95		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	14, 17
Access time from $\overline{CAS}$	tCAC		17		20	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		20		20	ns	
Access time from column address	tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	70	20,000	80	20,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		ns	
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	
Row address setup time	tASR	0		0		ns	
Row address hold time	tRAH	10		12		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	35	17	40	ns	18
Column address setup time	tASC	0		0		ns	
Column address hold time	tCAH	12		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	ns	20, 23
Output disable	tOD	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		15		ns	27
Output Enable to $\overline{RAS}$ delay	tORD	0		0		ns	

NEW TRIPLE-PORT DRAM

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		60		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		40		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR refresh)	^tCHR	10		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	60		70		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		25		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	7	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		10		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		60		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	55		60		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
SC to QSF delay time	^tSQD		20		20	ns	28
$\overline{RAS}$ to QSF delay time	^tRQD		65		65	ns	28
$\overline{CAS}$ to QSF delay time	^tCQD		35		35	ns	28
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25	ns	28
SPLIT TRANSFER setup time	^tSTS	25		30		ns	28
SPLIT TRANSFER hold time	^tSTH	0		0		ns	28

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

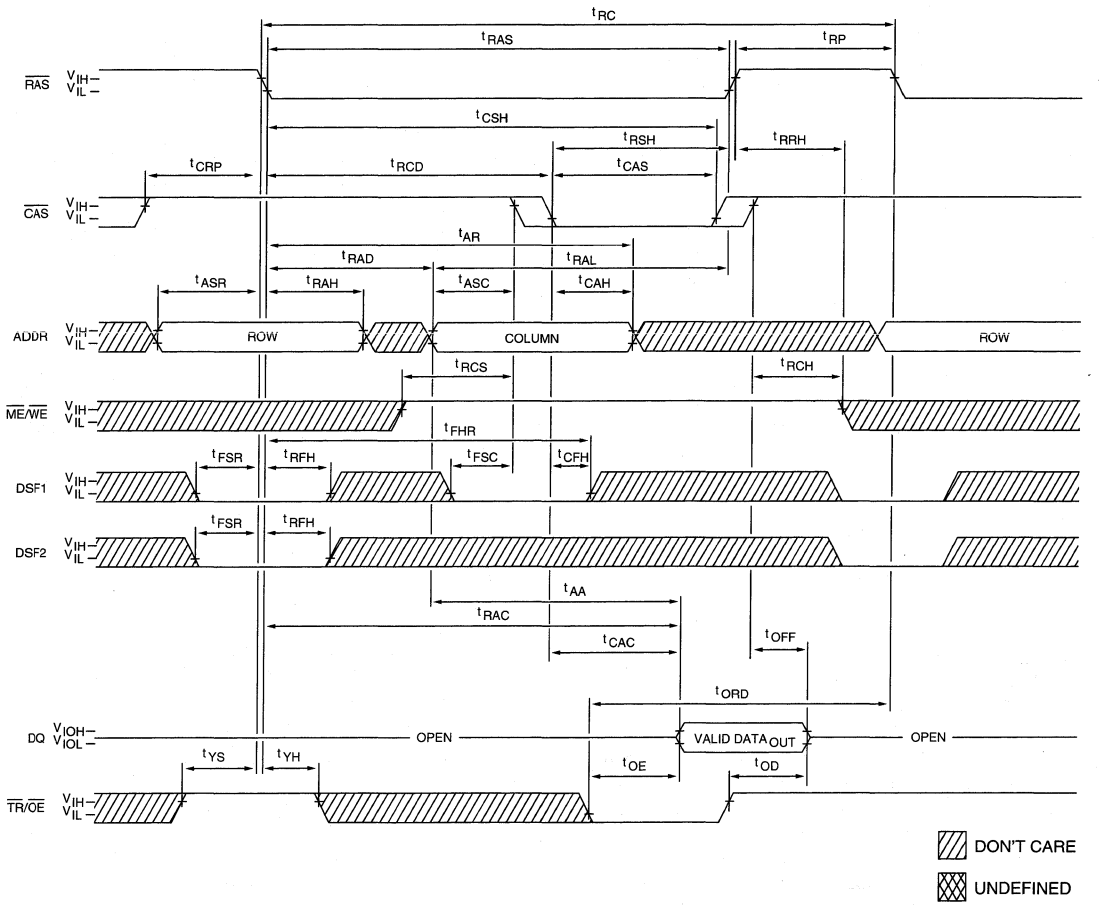
AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time (Read)	^tSCR	22		25		ns	
Serial clock cycle time (Write)	^tSCW	20		20		ns	
Access time from SC	^tSAC		22		25	ns	24, 30
SC precharge time (SC LOW time)	^tSP	7		7		ns	
SC pulse width (SC HIGH time)	^tSAS	7		7		ns	
Access time from $\overline{SE}$	^tSEA		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	10		10		ns	
$\overline{SE}$ pulse width	^tSE	10		10		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		ns	24, 30
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24
Serial data in setup time	^tSDS	0		0		ns	24
Serial data in hold time	^tSDH	10		10		ns	24
Serial mask data in setup time	^tMDS	0		0		ns	
Serial mask data in hold time	^tMDH	10		10		ns	
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	10		15		ns	
SERIAL INPUT (Write) disable setup time	^tSWIS	0		0		ns	
SERIAL INPUT (Write) disable hold time	^tSWIH	10		15		ns	
SSF to SC setup time	^tSFS	0		0		ns	29
SSF to SC hold time	^tSFH	10		15		ns	29
SSF LOW to SC HIGH delay	^tSFD	5		5		ns	29

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±5%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 3 to 5ns.
9. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data outputs (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data outputs (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^tWCS ≤ ^tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Addresses (A0-A8) change two times or less while $\overline{RAS}$ = V_{IL}.
26. Addresses (A0-A8) change once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. Applies to the MT43C8128A only.
29. Applies to the MT43C8129A only.
30. ^tSAC is MAX at 70° C and 4.75V Vcc; ^tSOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature ^tSOH = ^tSAC - output transition time; this is guaranteed by design.

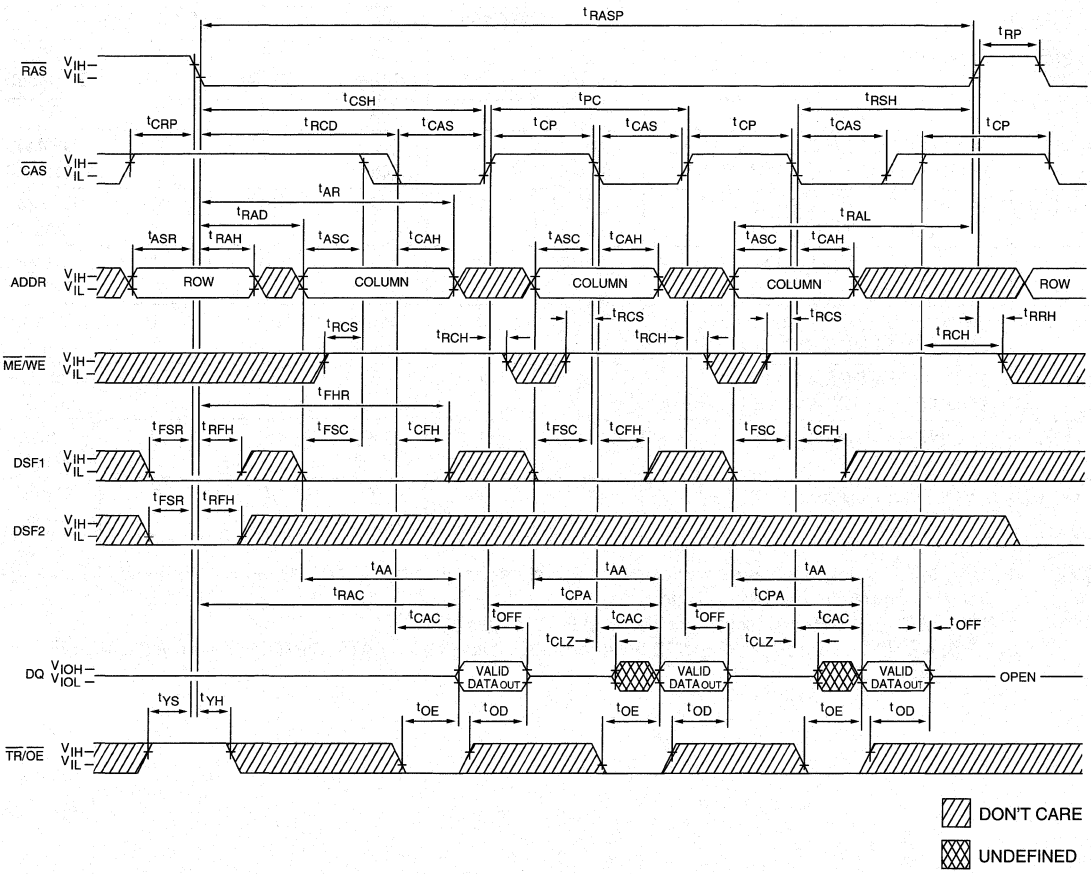
NEW TRIPLE-PORT DRAM

DRAM READ CYCLE



NEW TRIPLE-PORT DRAM

DRAM FAST-PAGE-MODE READ CYCLE

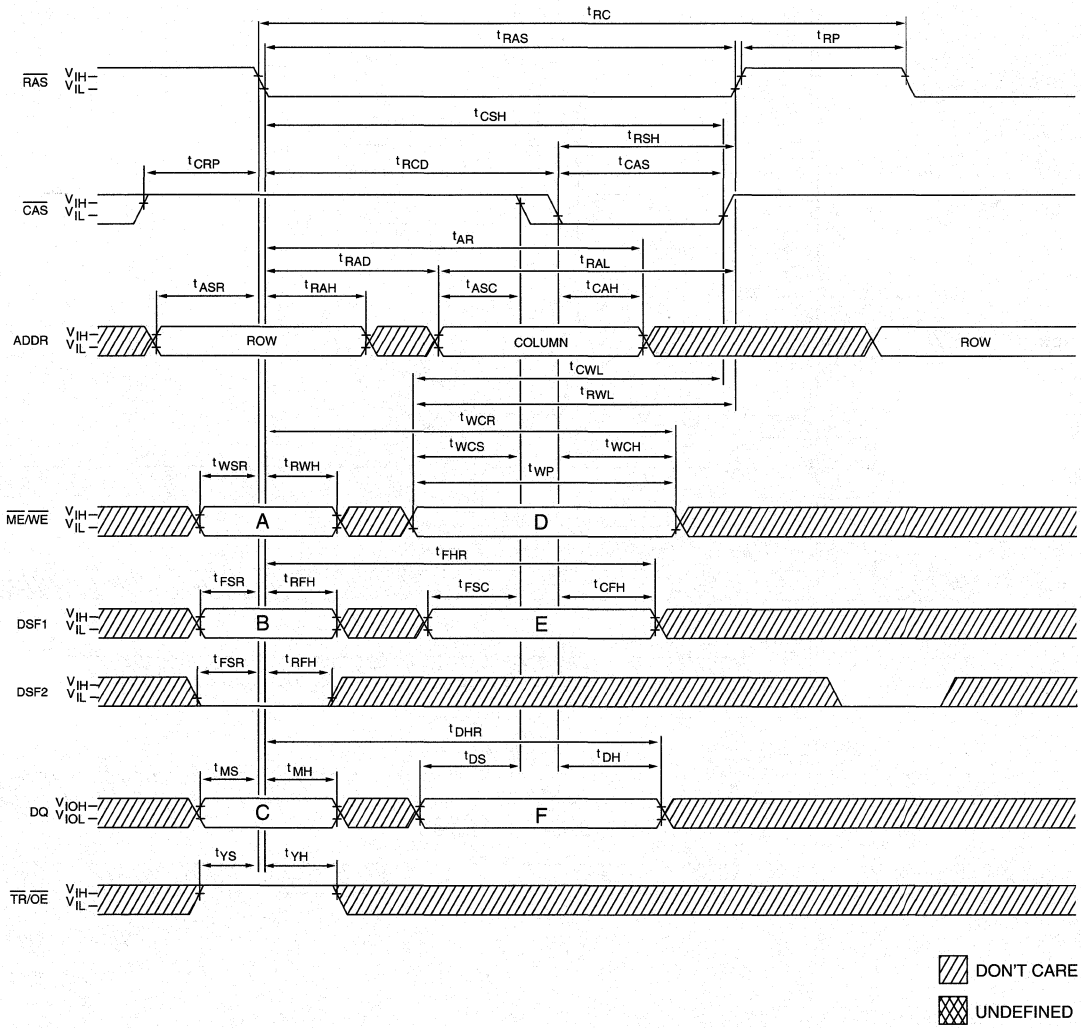


WRITE CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES[2]					
		RAS Falling Edge			CAS Falling Edge		
		A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1[3]	0	DRAM (Masked)
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1[3]	0	DRAM (Masked)
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	X	0/1[3]	1	Column Mask
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1[3]	1	Column Mask
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	0/1[3]	1	Column Mask
LMR	Load Mask Data Register	1	1	X	0/1[3]	0	Write Mask
LCR	Load Color Register	1	1	X	0/1[3]	1	Color Mask

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2. TRM, MKD and STS are "don't care" for all WRITE cycles.
3. If $\overline{ME}/\overline{WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME}/\overline{WE}$ falls after $\overline{CAS}$.

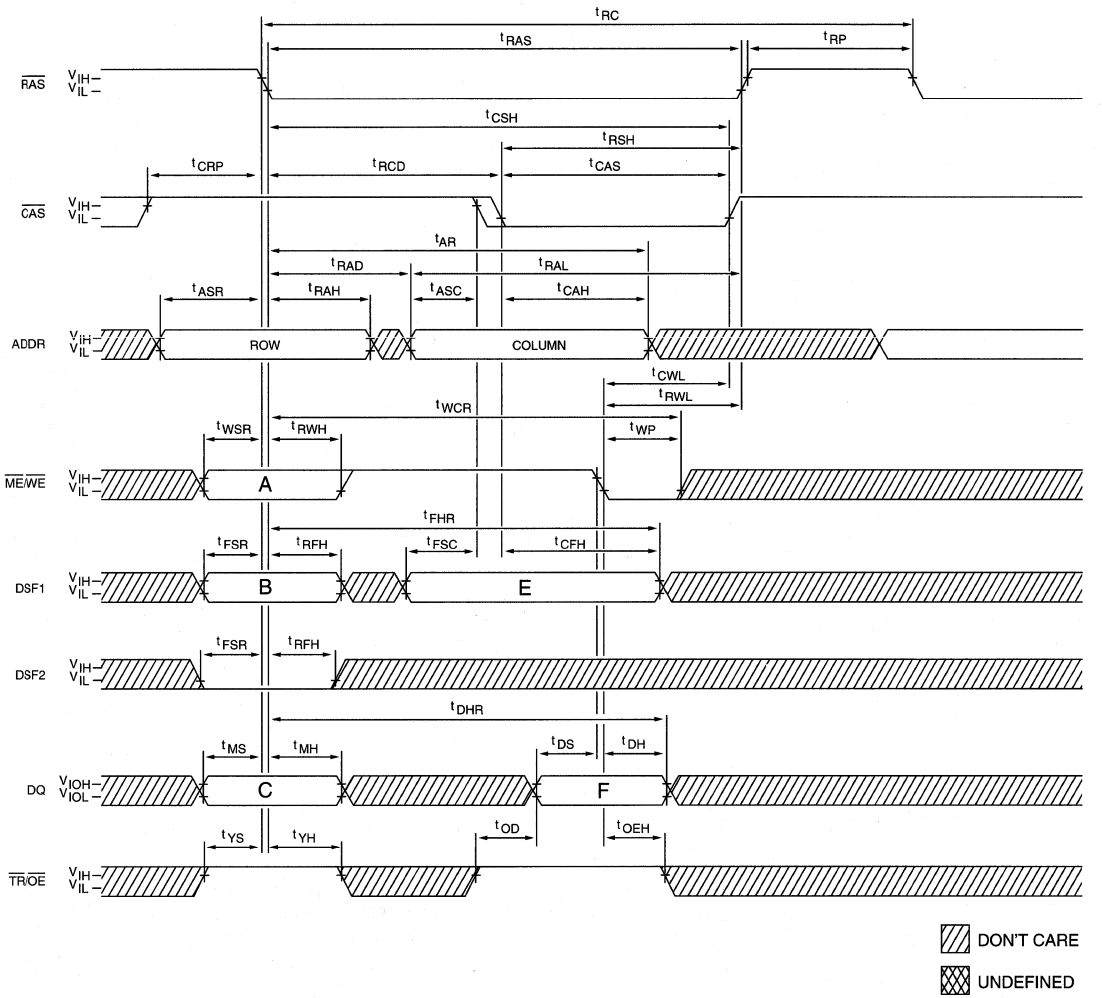
DRAM EARLY-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the WRITE Cycle Function Table for a detailed description.

NEW TRIPLE-PORT DRAM

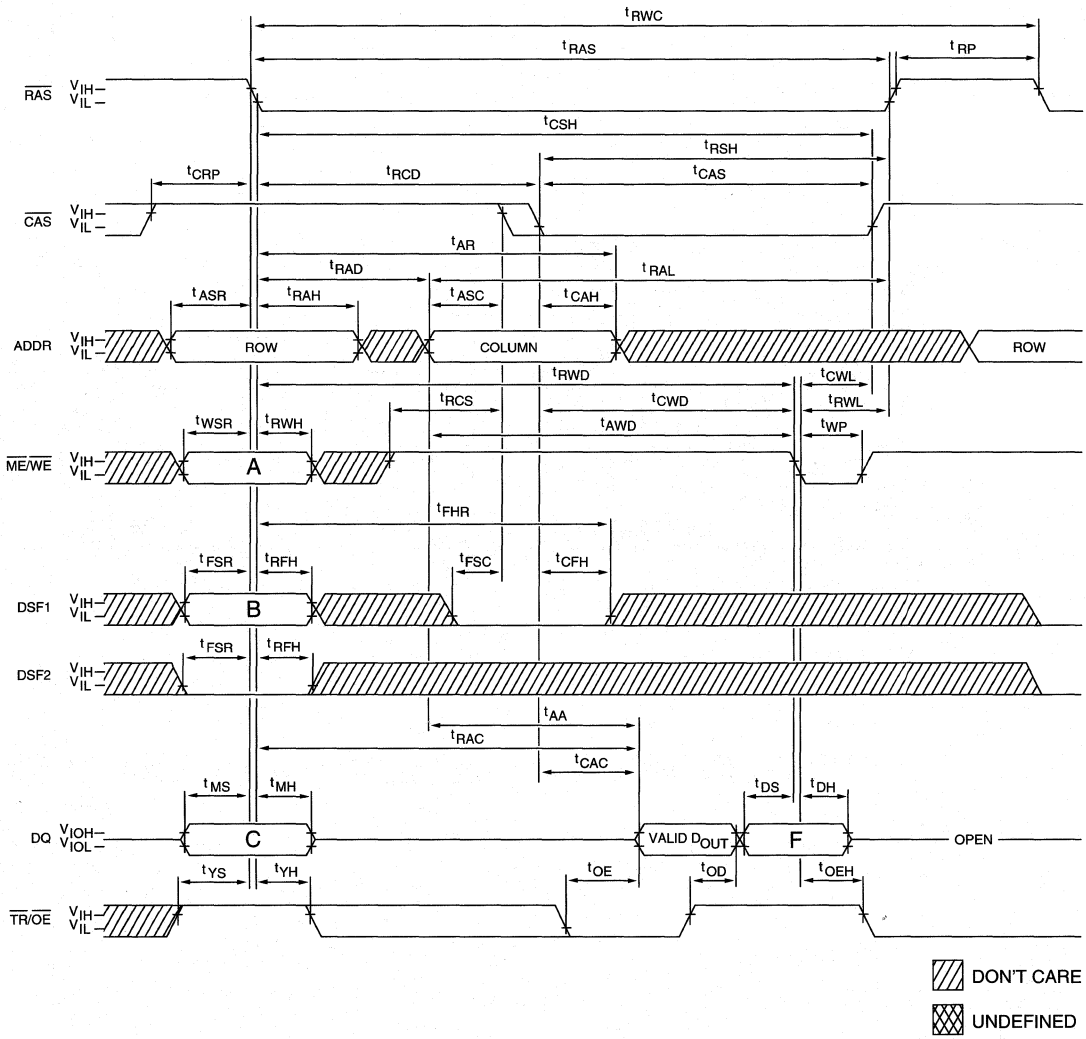
DRAM LATE-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW TRIPLE-PORT DRAM

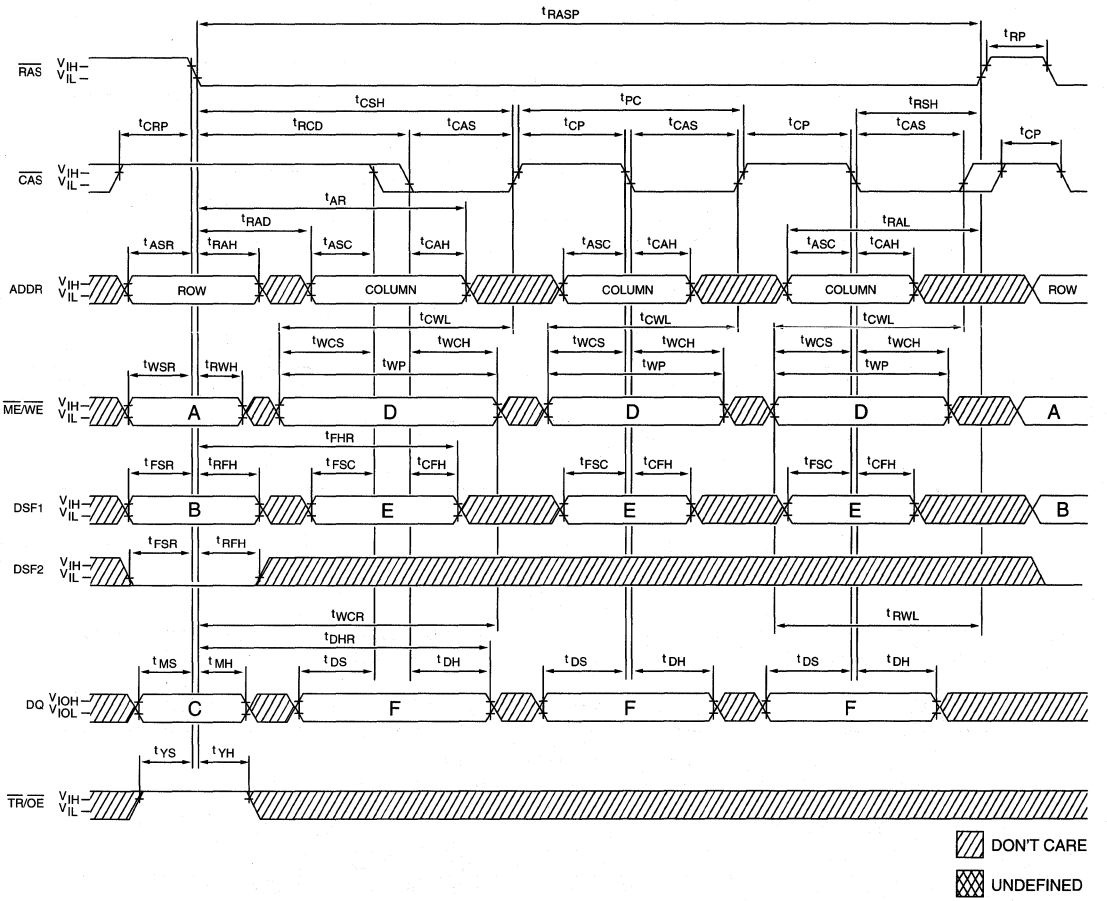
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

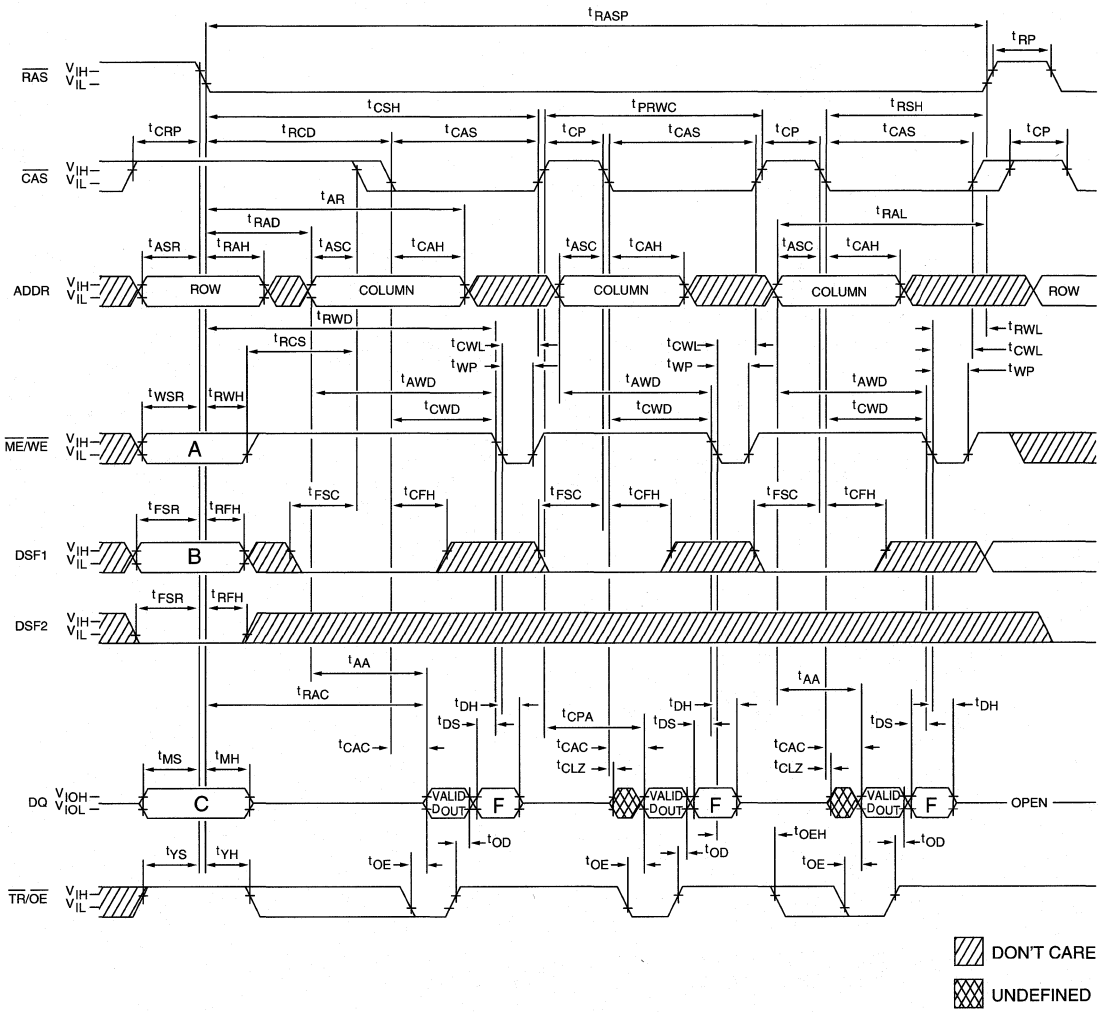
NEW ■ TRIPLE-PORT DRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



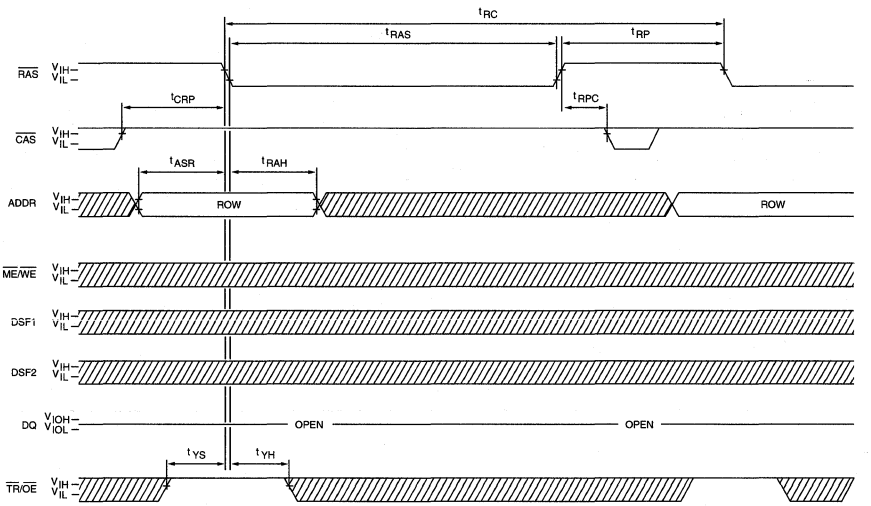
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

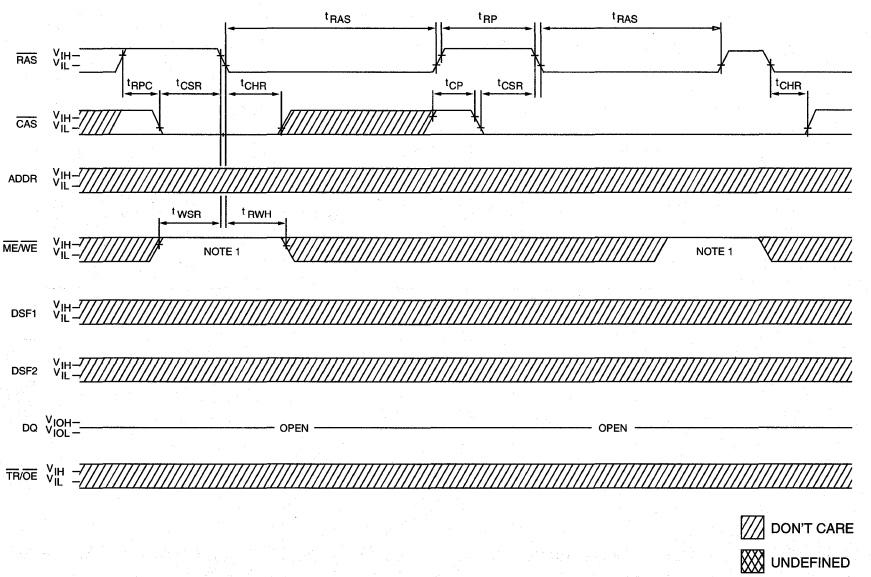


NOTE: 1. READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

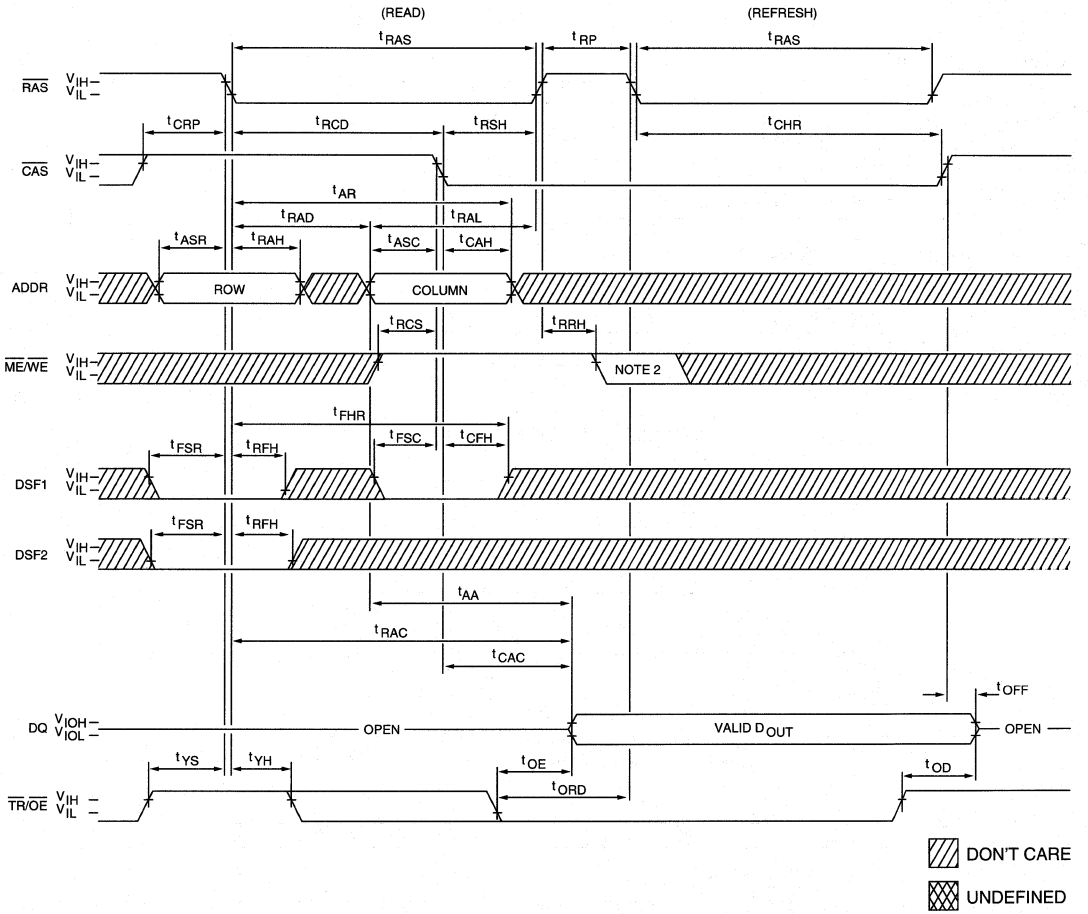


CBR REFRESH CYCLE



NOTE: 1. The MT43C8128A/9A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

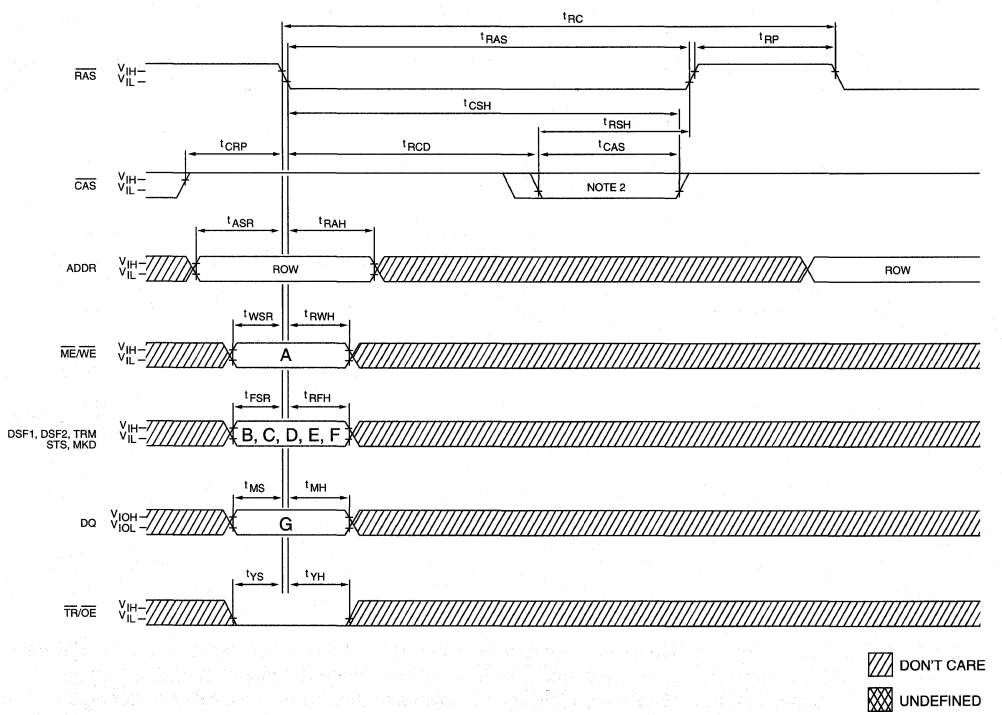


NOTE:
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay HIGH-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The MT43C8128A/9A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES						
		RAS Falling Edge						
		A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/1[1]	X
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/1[1]	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/1[1]	Mask
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/1[1]	Mask
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	X	0/1[1]	X

DRAM/BMR TRANSFERS



NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.

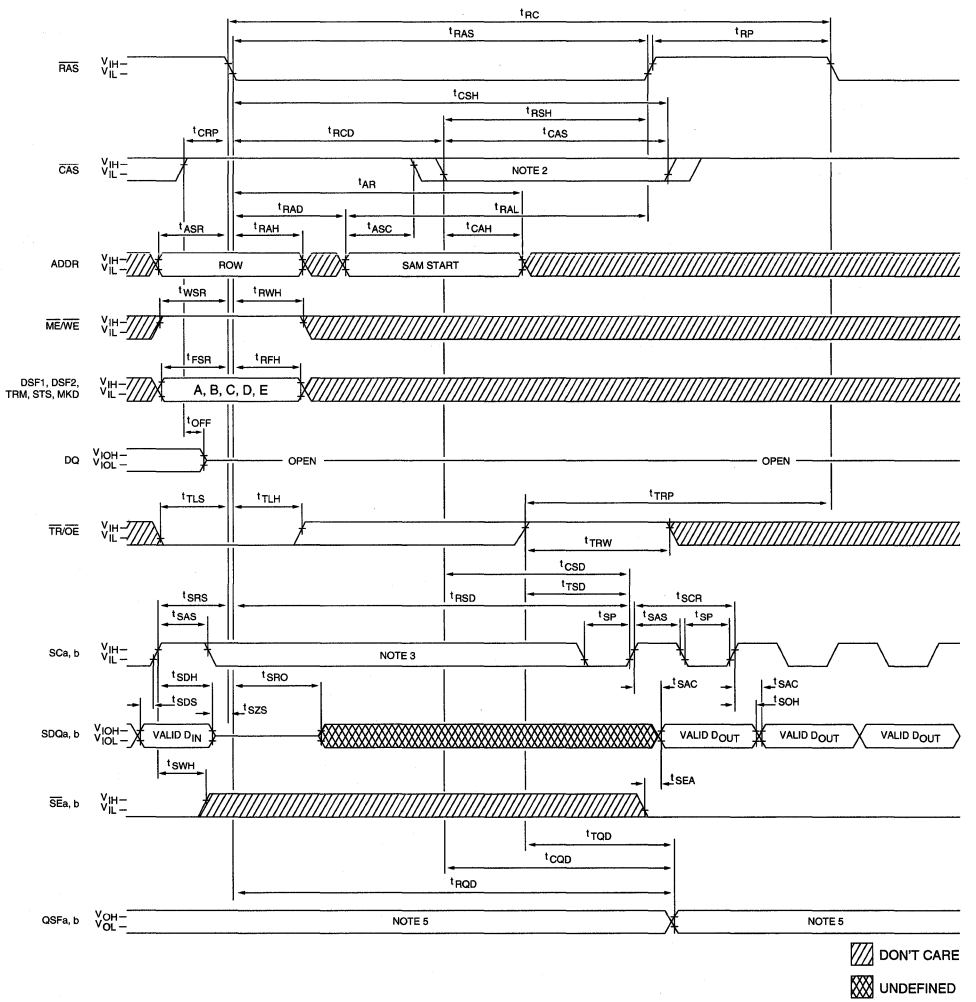
READ TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES				
		$\overline{RAS}$ Falling Edge				
		A DSF1	B DSF2	C TRM	D STS	E MKD
RW	READ TRANSFER	0	0	0	0/1[2]	X
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/1[2]	X
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/1[2]	X
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1	1	0/1[2]	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/1[2]	0/1[3]

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
3. Serial mask input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

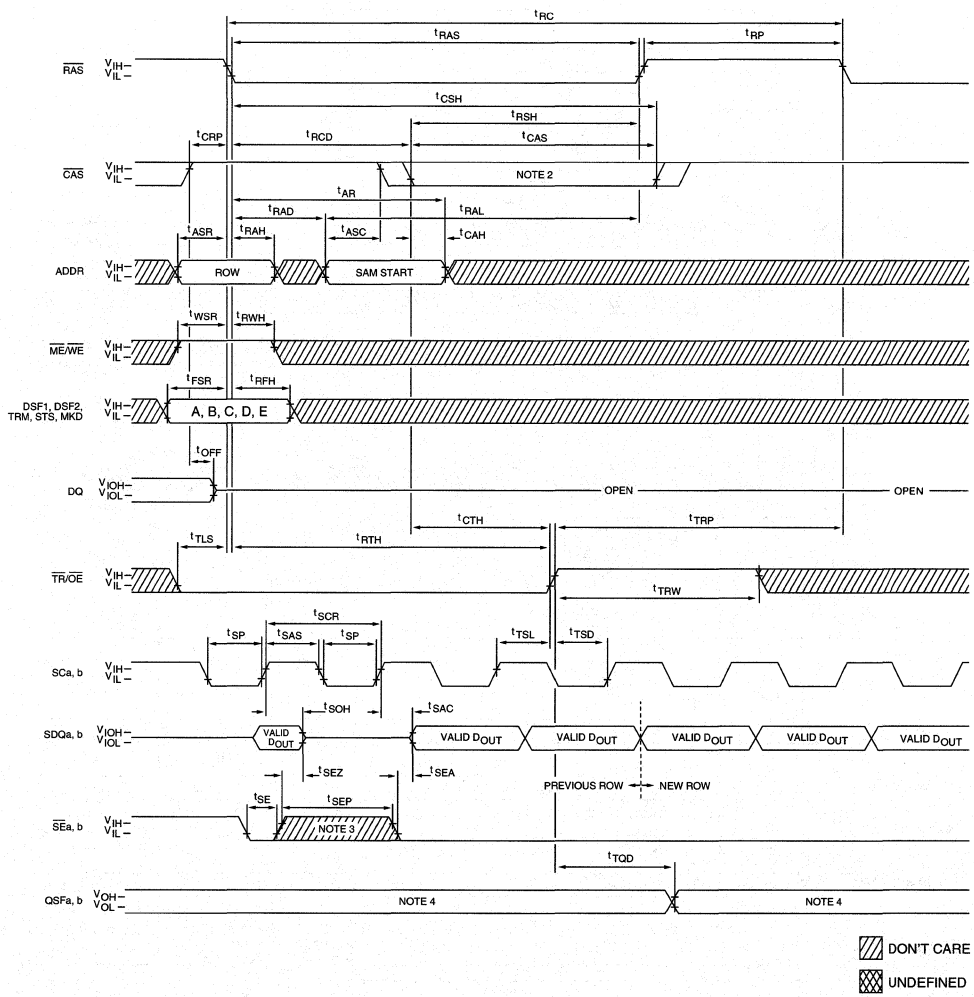
NEW ■ TRIPLE-PORT DRAM

READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. SSFa, b = "don't care" (MT43C8129A)
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed.

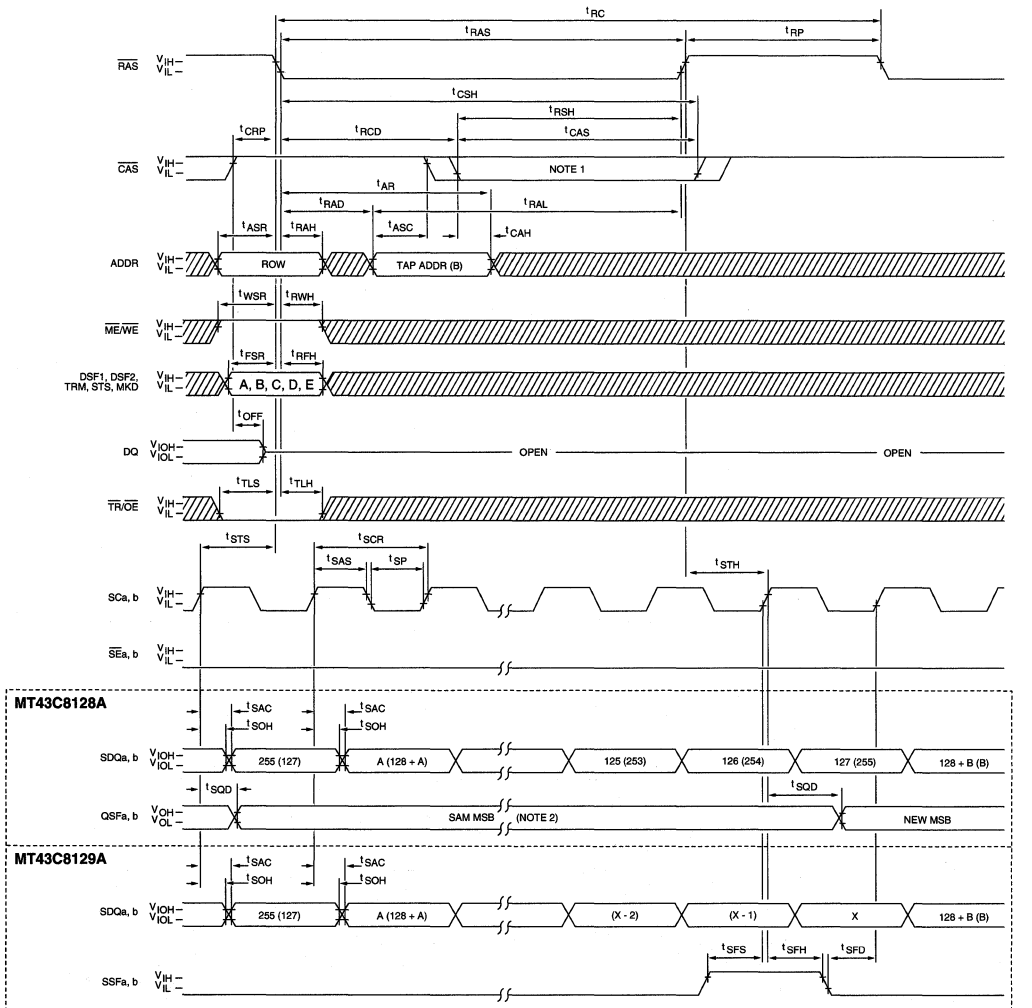
REAL-TIME READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. SSFa, b = "don't care" (MT43C8129A)
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed.
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed.

NEW TRIPLE-PORT DRAM

SPLIT READ TRANSFER [3]
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

WRITE TRANSFER CYCLE FUNCTION TABLE [1]

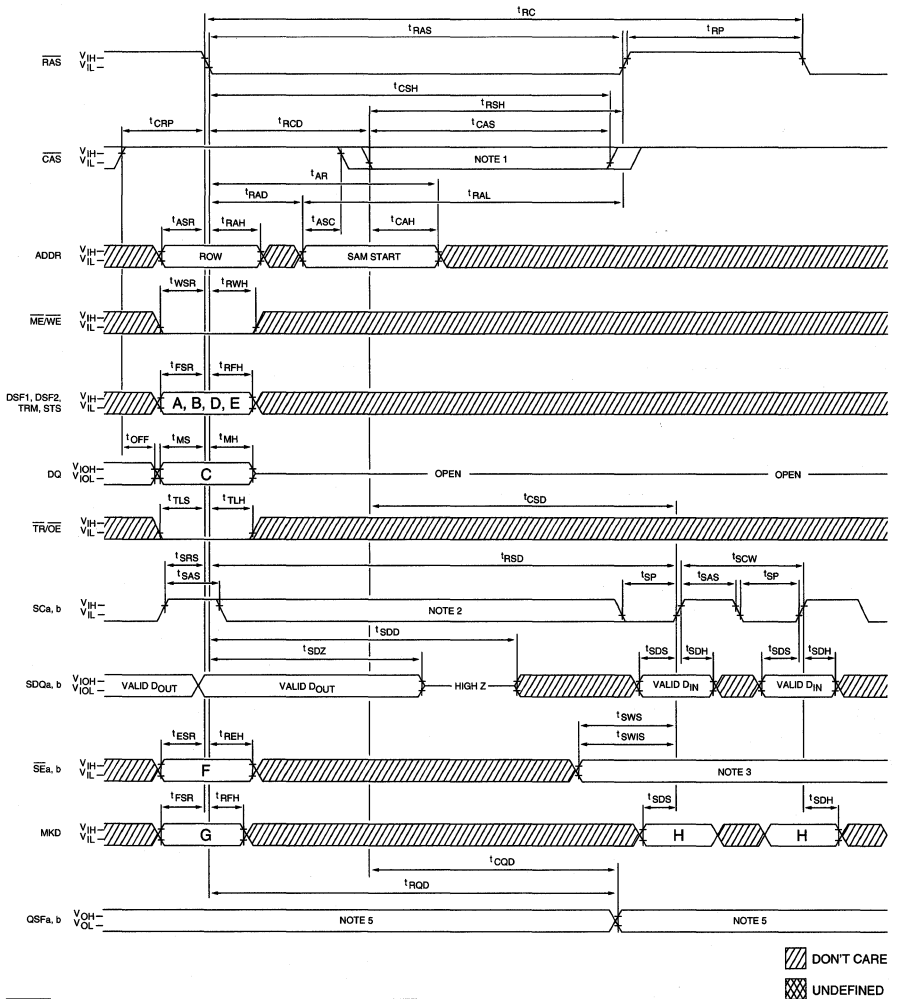
CODE	FUNCTION	LOGIC STATES							
		RAS Falling Edge							SC
		A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	X	0	0/1[2]	0	X	-
PWT	PSEUDO WRITE TRANSFER	0	0	X	0	0/1[2]	1	X	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/1[2]	X	X	-
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/1[2]	X	X	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	X	1	0/1[2]	X	X	0/1[4]
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/1[2]	X	X	0/1[4]
SAM-BMR	(SAM→BMR) TRANSFER	1	0	X	1	0/1[2]	X	0/1[3]	-
BMWT-DQM	DQ/BIT MASKED WRITE TRANSFER (SAM→DRAM)	1	1	Mask	0	0/1[2]	X	X	0/1[4]

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G" and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
3. Serial mask input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through all the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

NEW TRIPLE-PORT DRAM

WRITE TRANSFER [4]

(When part was previously in the SERIAL OUTPUT mode)

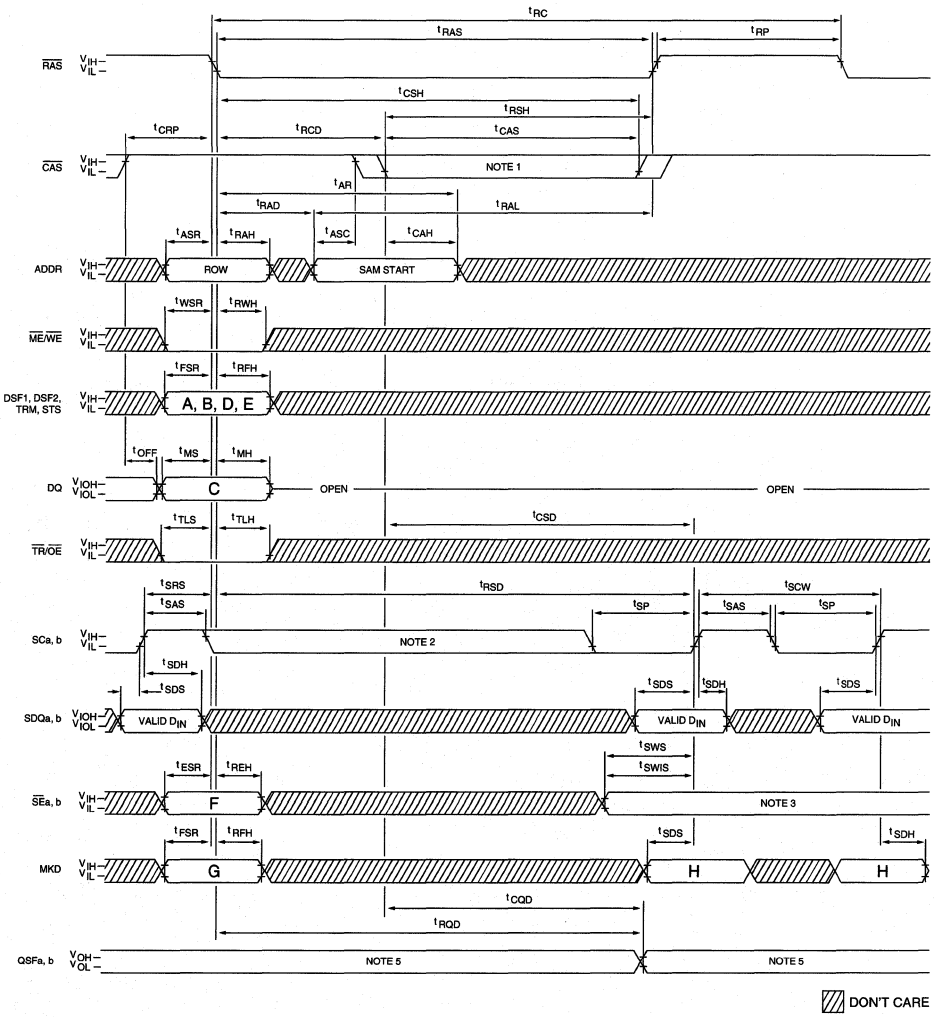


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129A).

WRITE TRANSFER [4]

(When part was previously in the SERIAL INPUT mode)

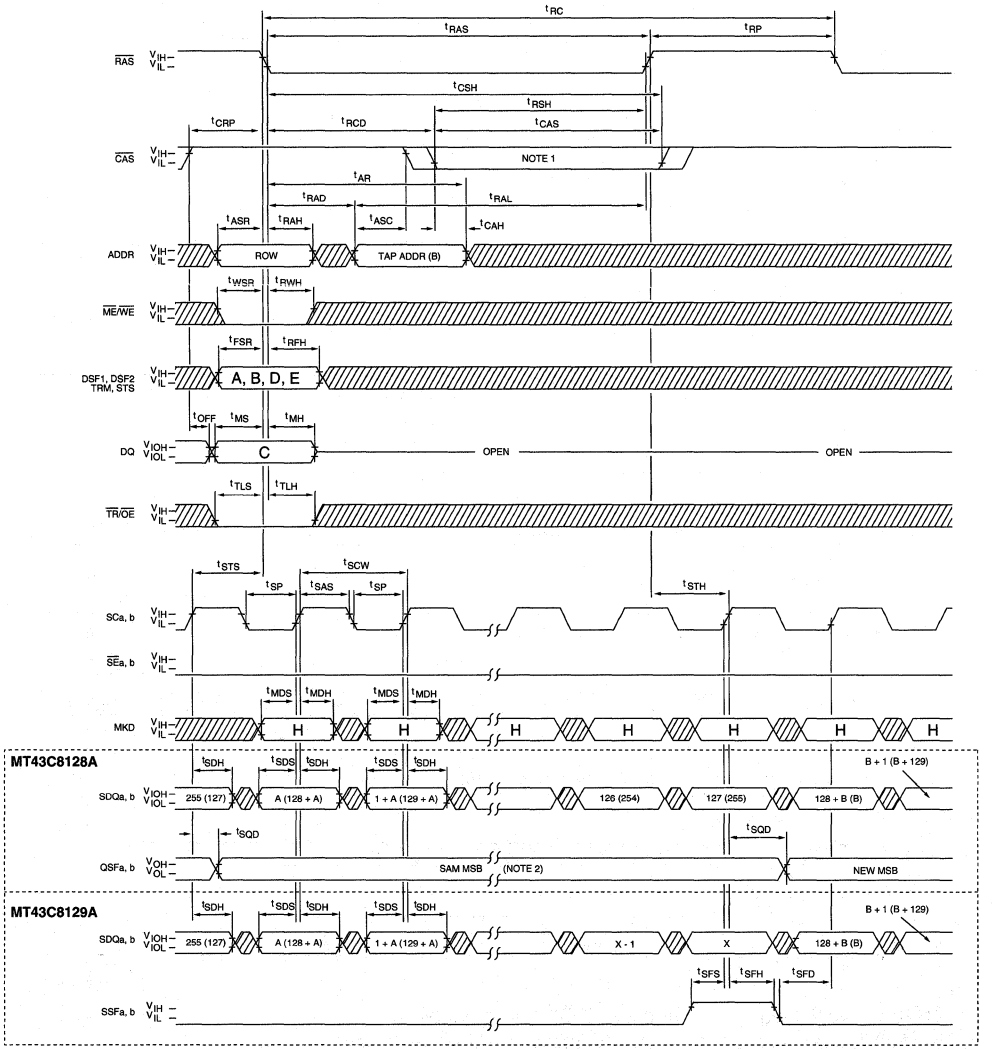


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129A).

NEW TRIPLE-PORT DRAM

SPLIT WRITE TRANSFER [3]
(SPLIT SAM-TO-DRAM TRANSFER)

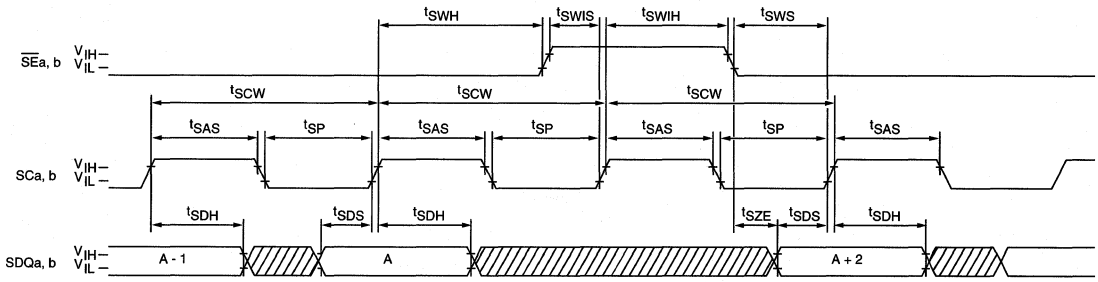


DON'T CARE

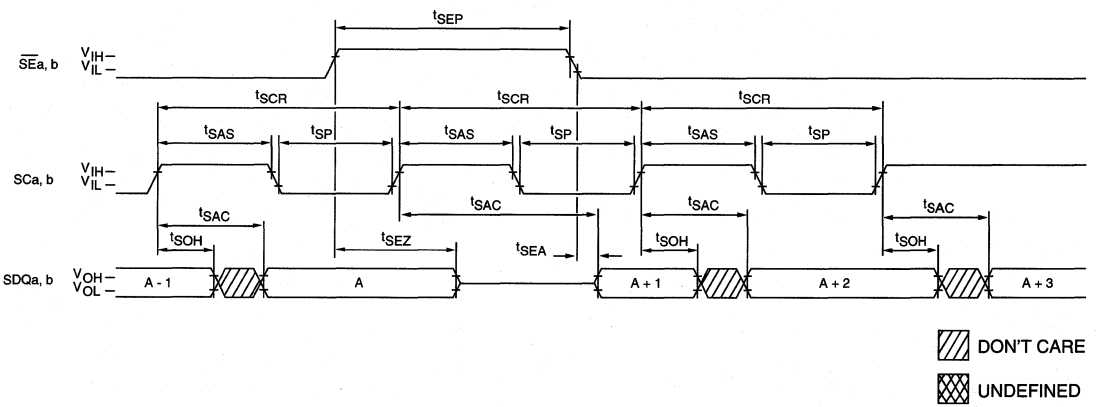
UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. QSF = 0 when the lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE: $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

MICRON SEMICONDUCTOR, INC.

MT43C8128A/9A
128K x 8 TRIPLE-PORT DRAM

TRIPLE-PORT DRAM

256K x 8 DRAM WITH DUAL 512 x 8 SAMS

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 60ns random, 15ns serial
- Operation and control compatible with 2 Meg VRAMs
- High-performance, CMOS silicon-gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 16.7ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST-PAGE-MODE with Extended Data-Out (^tPC = 30ns)
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 4,096-bit Transfer Mask Register

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- BLOCK WRITE
- SPLIT READ and SPLIT WRITE TRANSFERs
- PROGRAMMABLE SPLIT SAMs
- BIT MASKED TRANSFERs
- SERIAL MASK DATA INPUT mode

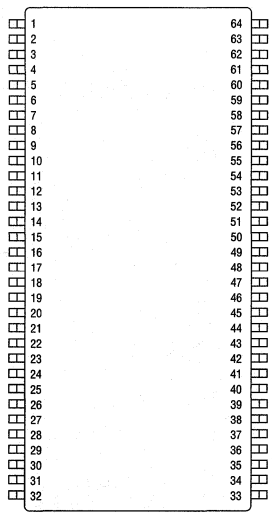
OPTIONS

OPTIONS	MARKING
• Timing (DRAM, SAMs [cycle/access])	
60ns, 20ns/15ns	-6
70ns, 25ns/20ns	-7
80ns, 28ns/25ns	-8
• Packages	
Plastic SOP (12mm)	SG

- Part Number Example: MT43C256K8A1SG-7

PIN ASSIGNMENT (Top View)

64-Pin SOP*
(SDC-1)



*Pinouts to be determined

GENERAL DESCRIPTION

The MT43C256K8A1 is a high-speed, triple-port CMOS dynamic random access memory (TPDRAM) containing 2,097,152 bits. Data may be accessed by an 8-bit-wide DRAM port or by either of two independently clocked 512 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048-bit-wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

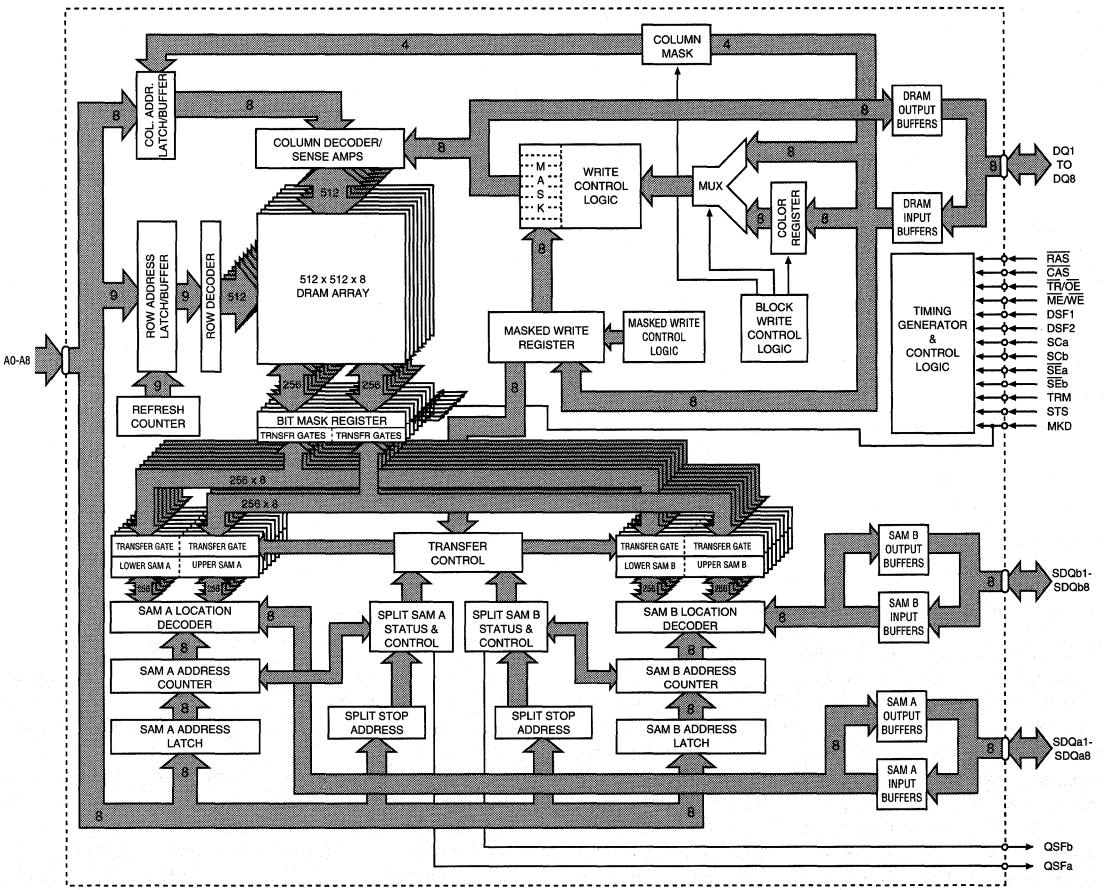
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 4,096 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 8-bit, bit mask data register may be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C256K8A1 are optimized for high-performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, video windowing, serial and parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERS and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



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VRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins	
				Standby	Active	SIMM	Page
256K x 32	FP, BW	MT4V25632	70, 80	40mW	1,200mW	104	4-1

FP = FAST-PAGE-MODE, BW = BLOCK WRITE

VRAM MODULE

256K x 32 DRAM WITH 512 x 32 SAM

FEATURES

- Proposed industry-standard pinout in a 104-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Low power, 40mW standby; 1,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Dual-port organization: 256K x 32 DRAM port
  512 x 32 SAM port
- 512-cycle refresh distributed across 16.7ms
- FAST-PAGE-MODE access cycle
- No refresh required for serial access memory

SPECIAL FUNCTIONS

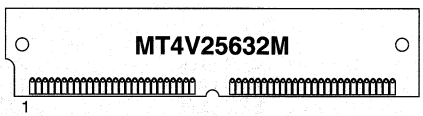
- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])
  70ns, 22/22ns -7
  80ns, 25/25ns -8
- Packages
  Leadless 104-pin SIMM M
- Part Number Example: MT4V25632M-7

PIN ASSIGNMENT (Top View)

104-Pin SIMM
(SDF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	27	SQ8	53	DQ18	79	A7
2	QSF0	28	Vss	54	DQ19	80	A8
3	$\overline{RAS0}$	29	NC	55	DQ20	81	NC
4	PRD0	30	NC	56	DQ21	82	Vss
5	$\overline{CAS1}$	31	$\overline{CAS2}$	57	DQ22	83	DQ25
6	PRD1	32	DQ9	58	DQ23	84	DQ26
7	DSF	33	DQ10	59	DQ24	85	DQ27
8	DQ1	34	DQ11	60	Vcc	86	DQ28
9	DQ2	35	DQ12	61	SQ17	87	DQ29
10	DQ3	36	DQ13	62	SQ18	88	DQ30
11	DQ4	37	DQ14	63	SQ19	89	DQ31
12	DQ5	38	DQ15	64	SQ20	90	DQ32
13	DQ6	39	DQ16	65	SQ21	91	Vcc
14	DQ7	40	Vcc	66	SQ22	92	SQ25
15	DQ8	41	SQ9	67	SQ23	93	SQ26
16	$\overline{TR/OE}$	42	SQ10	68	SQ24	94	SQ27
17	$\overline{SE0}$	43	SQ11	69	NC	95	SQ28
18	SC	44	SQ12	70	$\overline{CAS4}$	96	SQ29
19	Vcc	45	SQ13	71	Vss	97	SQ30
20	SQ1	46	SQ14	72	A0	98	SQ31
21	SQ2	47	SQ15	73	A1	99	SQ32
22	SQ3	48	SQ16	74	A2	100	Vss
23	SQ4	49	Vss	75	A3	101	PRD2
24	SQ5	50	$\overline{ME/WE}$	76	A4	102	PRD3
25	SQ6	51	$\overline{CAS3}$	77	A5	103	PRD4
26	SQ7	52	DQ17	78	A6	104	PRD5

GENERAL DESCRIPTION

The MT4V25632 is a high-speed, multiport CMOS dynamic random access memory module containing 262,144 words organized in a x32 configuration. The module may be accessed either by a 32-bit wide DRAM port or by a 512 x 32-bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM. The module consists of four 256K x 8, dual-port dynamic RAMs mounted on a 104-pin SIMM, FR4 printed circuit board.

The DRAM portion of the VRAM components is functionally similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Thirty two 512-bit data registers make up the serial access memory portion on the VRAM module. Data I/O and internal data transfer are accomplished using three separate data paths for each component on the module: the 32-bit random access I/O port, the eight internal 512-bit-wide paths between the DRAM and the SAM, and the 32-bit serial output port for the SAM.

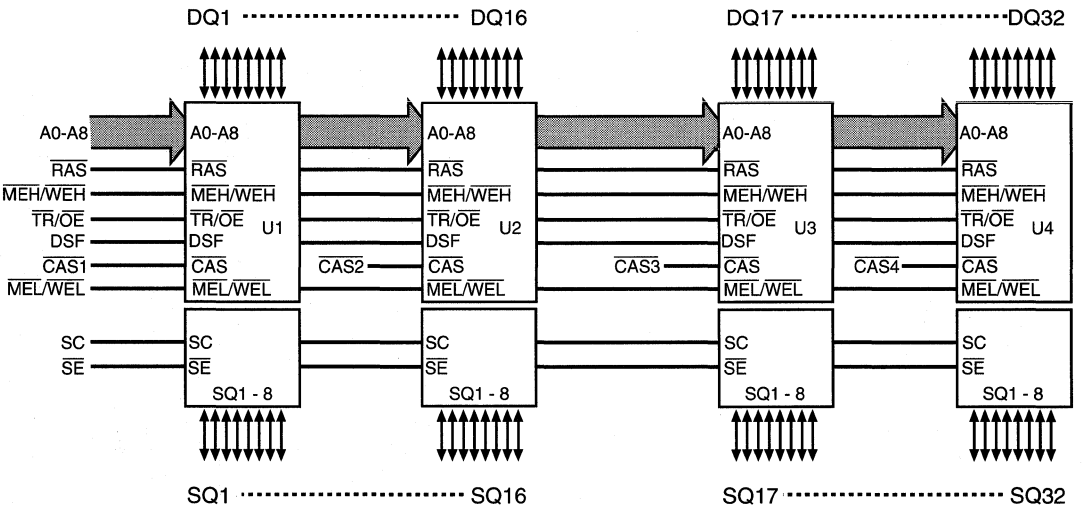
Each port may be operated asynchronously and independently of the other except when data is being transferred internally to each component. As with all DRAM modules, the VRAM module must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh

cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT4V25632 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enchancements to system performance.

NEW VRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1 - U4 = MT42C8255DJ

PRESENCE DETECT

SYMBOL	-7	-8
PRD0	Vss	Vss
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	Vss	NC
PRD4	NC	NC
PRD5	NC	NC

PIN DESCRIPTIONS

MODULE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
18	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
16	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
50	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM and READ TRANSFER ($\overline{ME/WE}$ = H) to the SAM.
17	$\overline{SE0}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial output buffers and allows a serial READ operation to occur; otherwise, the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
7	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
3	$\overline{RAS0}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
5, 31, 51, 70	$\overline{CAS1-4}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits and strobe the DSF input (BLOCK WRITE only).
72-80	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 32-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8-15, 32-39, 52-59,83-90	DQ1-DQ32	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
20-27, 41-48, 61-68, 92-99	SQ1-SQ32	Output	Serial Data Out: Output or High-Z.
2	QSF0	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
19, 40, 60, 91	V_{CC}	Supply	Power Supply: +5V ±10%
1, 28, 49, 71, 82, 100	V_{SS}	Supply	Ground

NEW VRAM MODULE

FUNCTIONAL DESCRIPTION

The MT4V25632 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory module, the MT4V25632 VRAM module must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT4V25632 supports CBR, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT4V25632 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM module is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits used to select an 32-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the VRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For standard single-port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW and remains HIGH until $\overline{CAS}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ32 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For standard single-port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/\overline{WE}$ performs two functions; write mask enable and data write enable. $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE

The MASKED WRITE (RWM) feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within a 32-bit word. When $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT4V25632 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ32 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ32 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ32 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

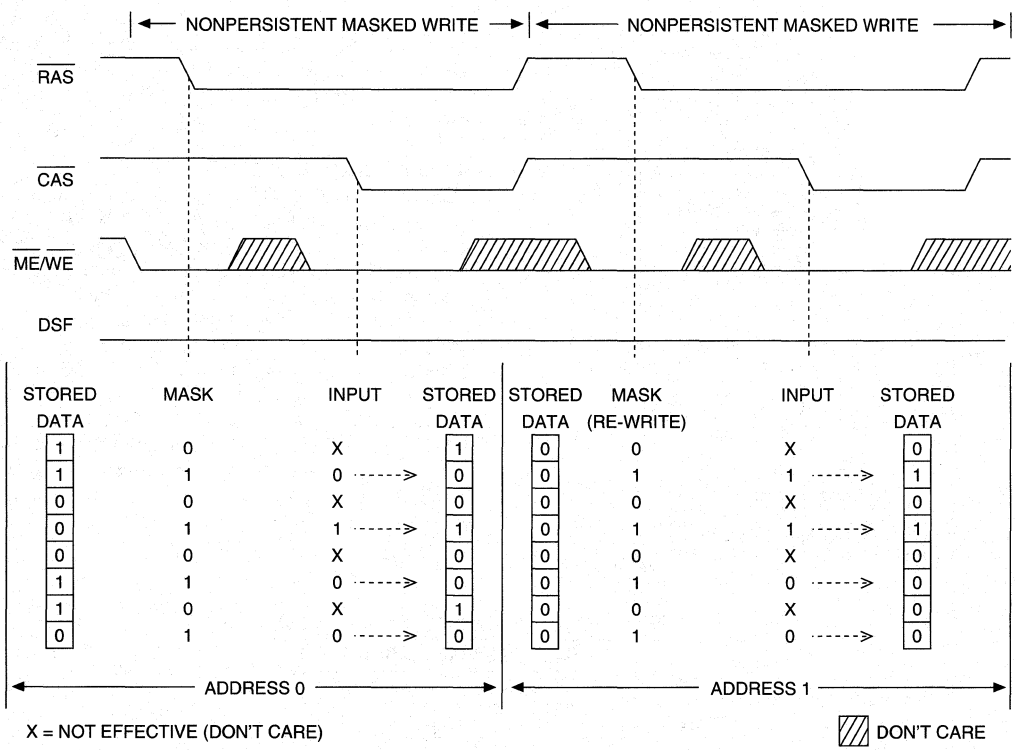


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE
(PER VRAM COMPONENT)

NEW VRAM MODULE

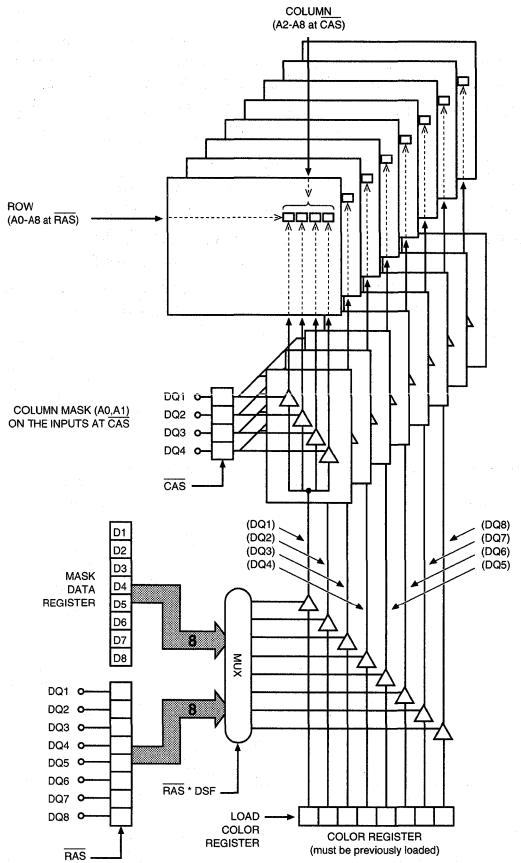


Figure 2
BLOCK WRITE EXAMPLE
(PER VRAM COMPONENT)

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT4V25632 will perform a BLOCK WRITE (BW) cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE (BWM) operates exactly like the normal MASKED WRITE except the mask is now applied to the 32 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BLOCK WRITE, any combination of the 32 bit-planes may be masked, along with any combination of the four column locations.

	COLUMN ADDRESS CONTROLLED	
INPUTS	**A0**	**A1**
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

LOAD COLOR REGISTER

A LOAD COLOR REGISTER (LCR) cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 32-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of theTRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER (RT) cycle is selected. The row-address bits indicate which 32 of the 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every RT in order to load a valid Tap address. An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data

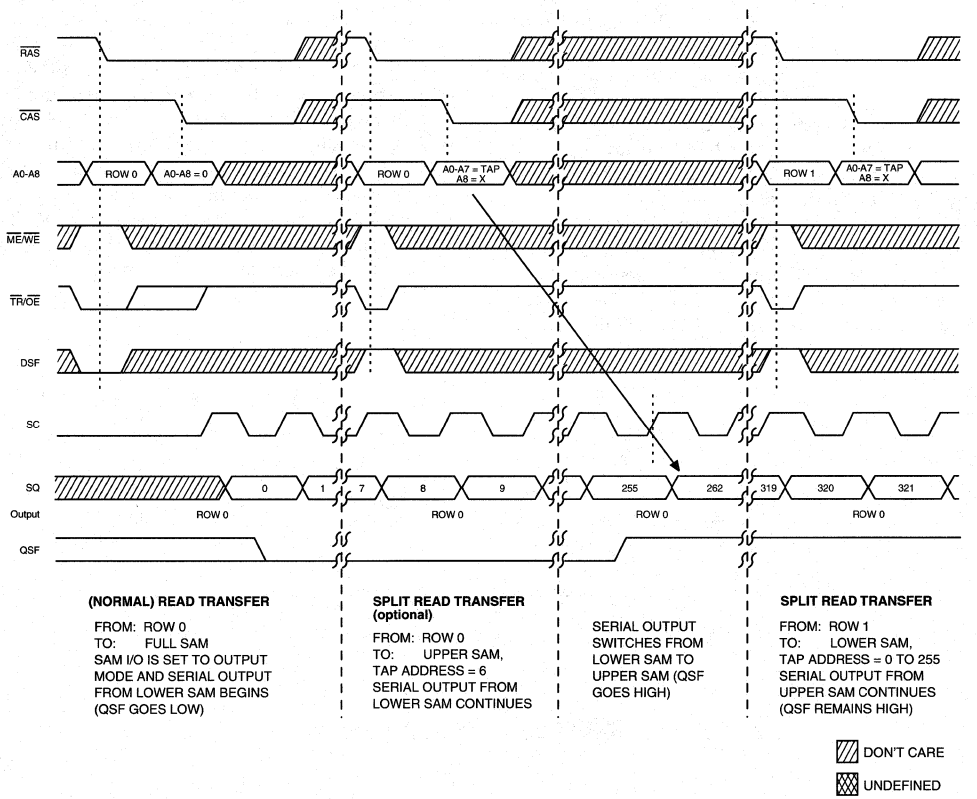


Figure 3
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers, and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER must occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputting data.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and, therefore, is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF). Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is $\neq 0$. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1) the QSF output goes HIGH. If an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 3 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode. The access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 4).

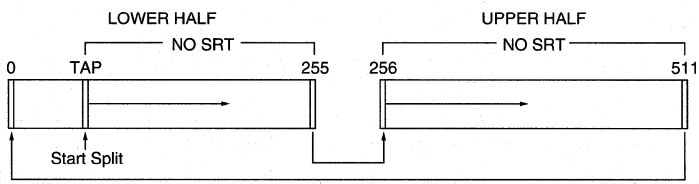


Figure 4
SPLIT SAM TRANSFER

SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SRT cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 32-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

POWER-UP and INITIALIZATION

After V_{CC} is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = $\overline{TR}$/ $\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT4V25632 module is completely static in operation and does not require refresh or initialization. The SAM port will power-up with the output pins (SQs) in High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ32[2]		REGISTER
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE[3]	COLOR
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	1[6]	1[6]	—	X	X	—	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[4]	X	X	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ32 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but a ROW address is not required.
5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).
6. The MT4V25632 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-40	40	µA	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		24	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		32	pF	2
Input Capacitance: $\overline{CAS}$1-4	C_{I3}		8	pF	2
Input/Output Capacitance: DQ1-32, SQ1-32	$C_{I/O}$		10	pF	2
Output Capacitance: QSF	C_O		10	pF	2

CURRENT DRAIN, SAM IN STANDBY

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = ^tRC$ [MIN])	I_{CC1}	500	440	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = ^tPC$ [MIN], other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC2}	460	400	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	40	40	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC4}	500	440	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	500	440	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	135	120	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = ^tRC$ [MIN])	I_{CC7}	700	640	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = ^tPC$ [MIN])	I_{CC8}	660	600	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤V_{IL})	I_{CC9}	240	240	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC10}	700	640	mA	3, 4 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	700	640	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	185	170	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	^tRWC	175		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	90		95		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		20	ns	
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$	^tOFF	3	20	3	20	ns	20,23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	^tOD	3	10	3	10	ns	20,23
Output disable hold time from start of WRITE	^tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	^tROH	0		0		ns	

NEW VRAM MODULE

NEW VRAM MODULE

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
SC to QSF delay time	^tSQD		25		30	ns	
SPLIT TRANSFER setup time	^tSTS	25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	45		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		75		75	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	30		30		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

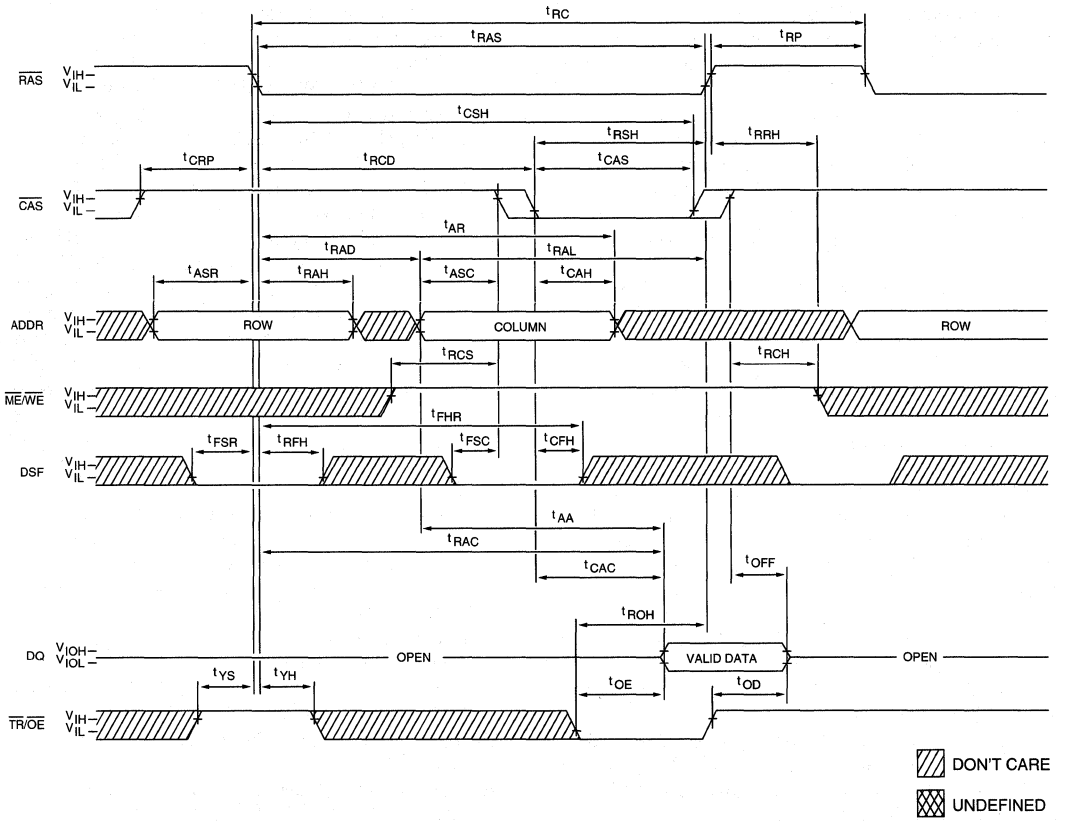
AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	22		25		ns	
Access time from SC	^tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	8		10		ns	
$\overline{SE}$ pulse width	^tSE	8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24

NOTES

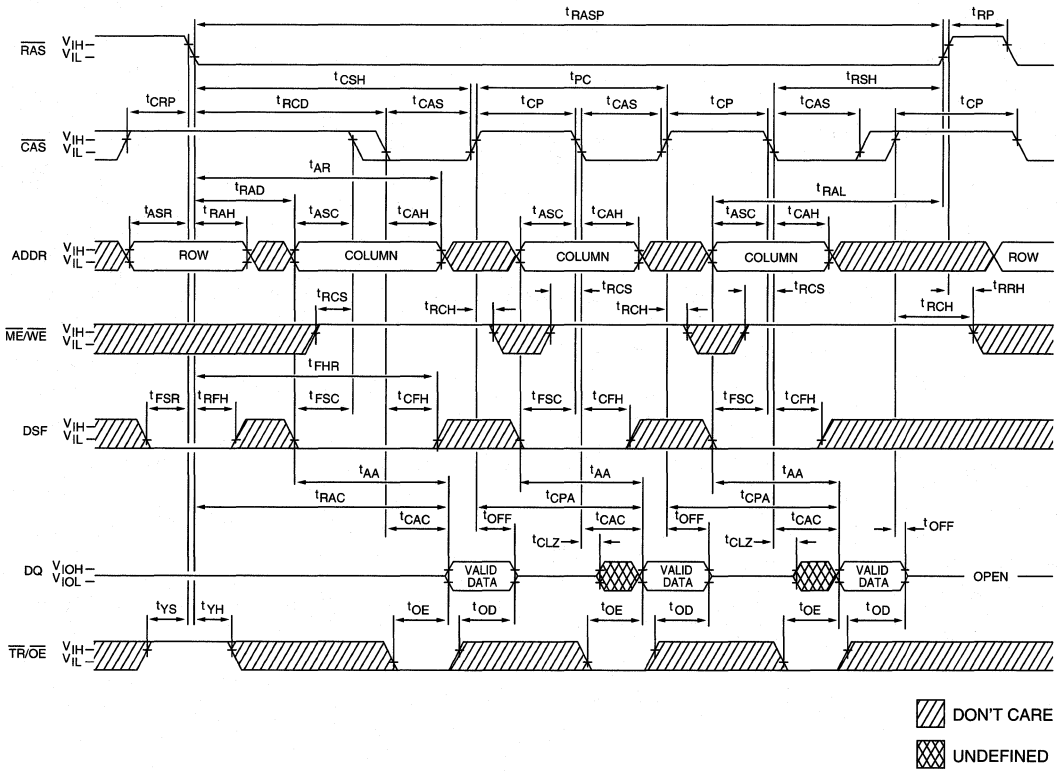
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16.7ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ32) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ32) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. (^tSOH = ^tSAC - output transition time); this is guaranteed by design.

NEW VRAM MODULE

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



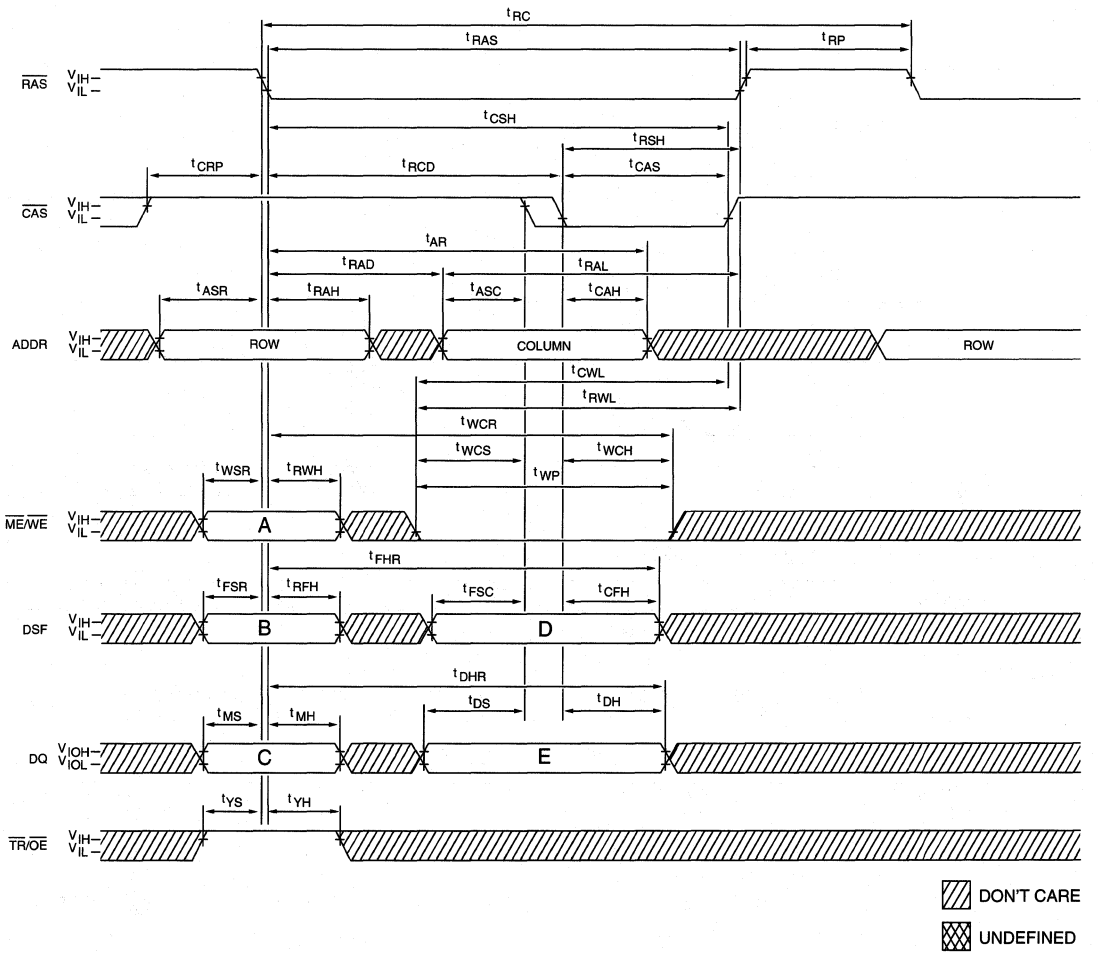
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask
Load Color Register	1	1	X	1	Color Data

NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs later.

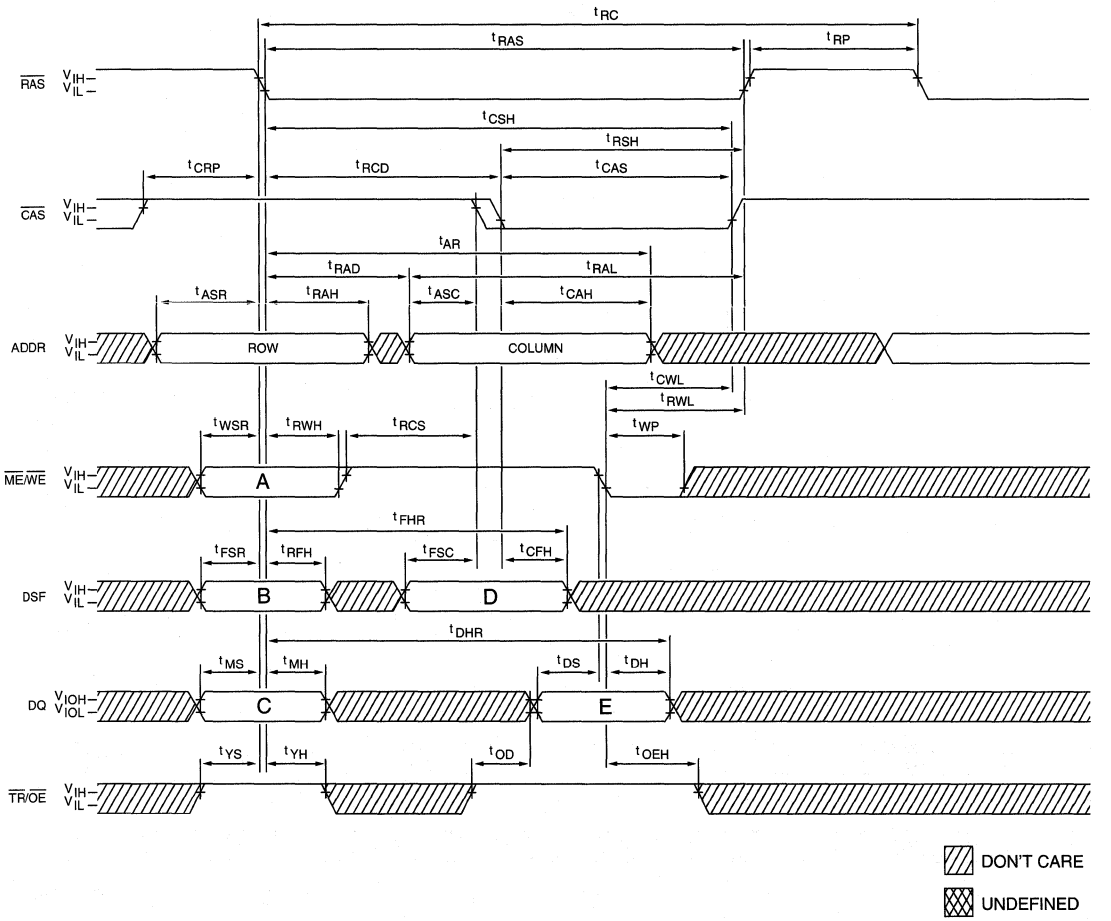
DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

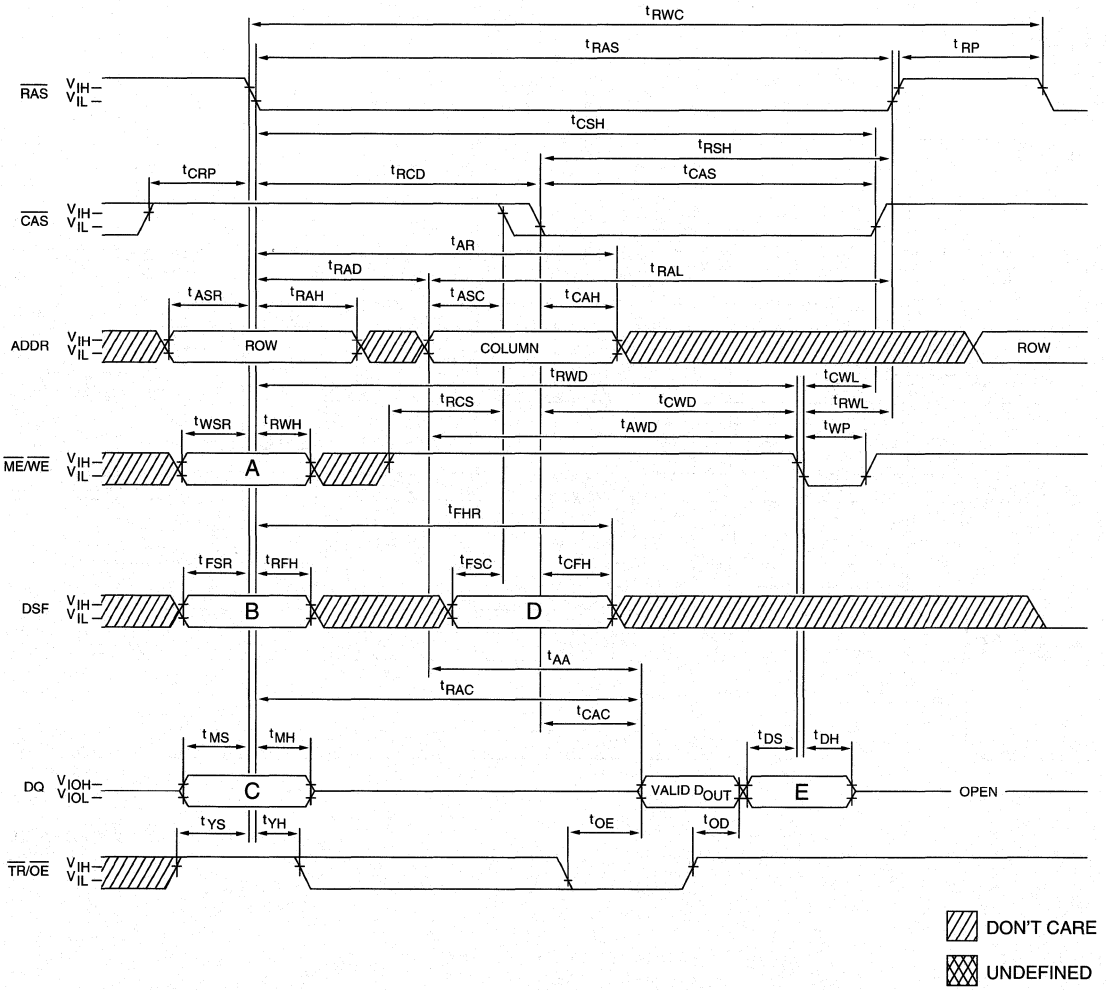
NEW VRAM MODULE

DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

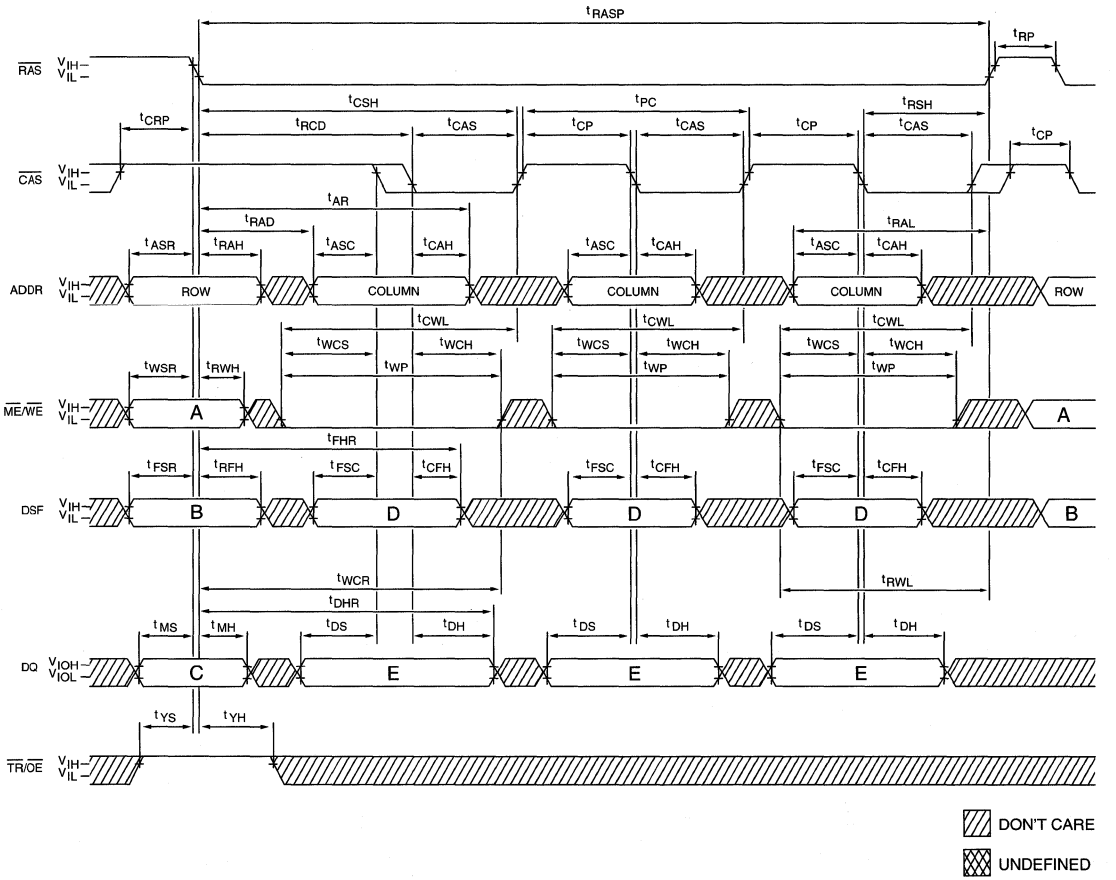
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW VRAM MODULE

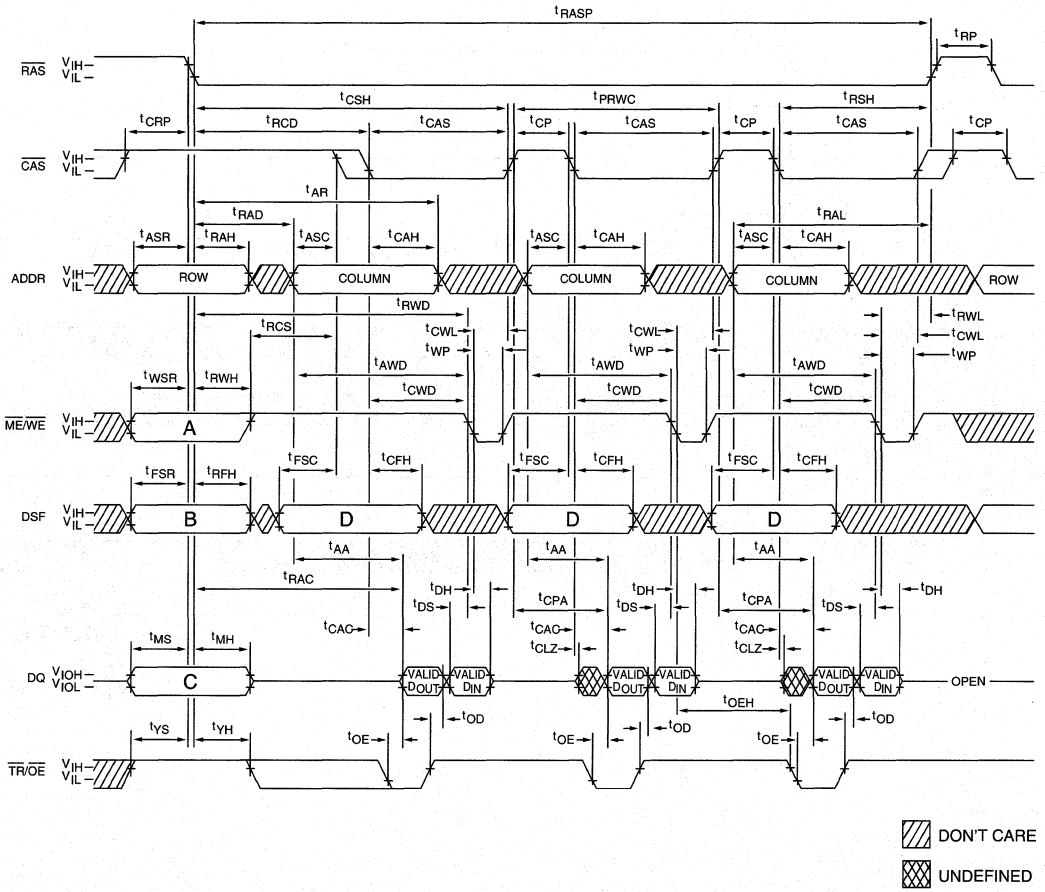
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.

2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

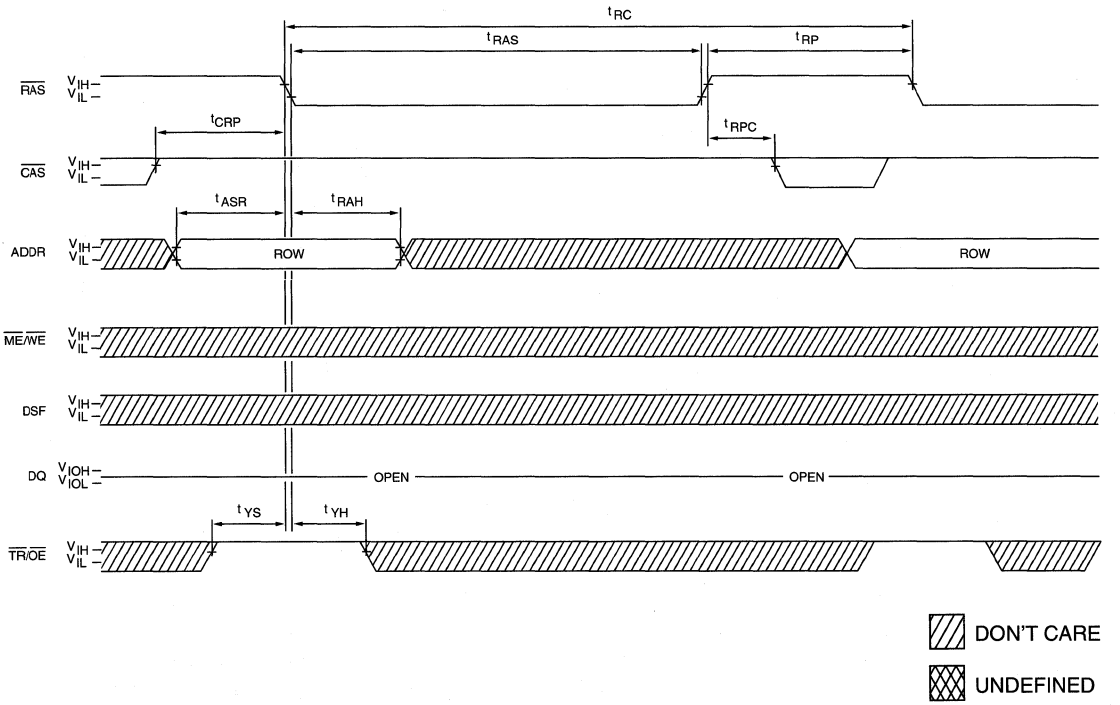
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



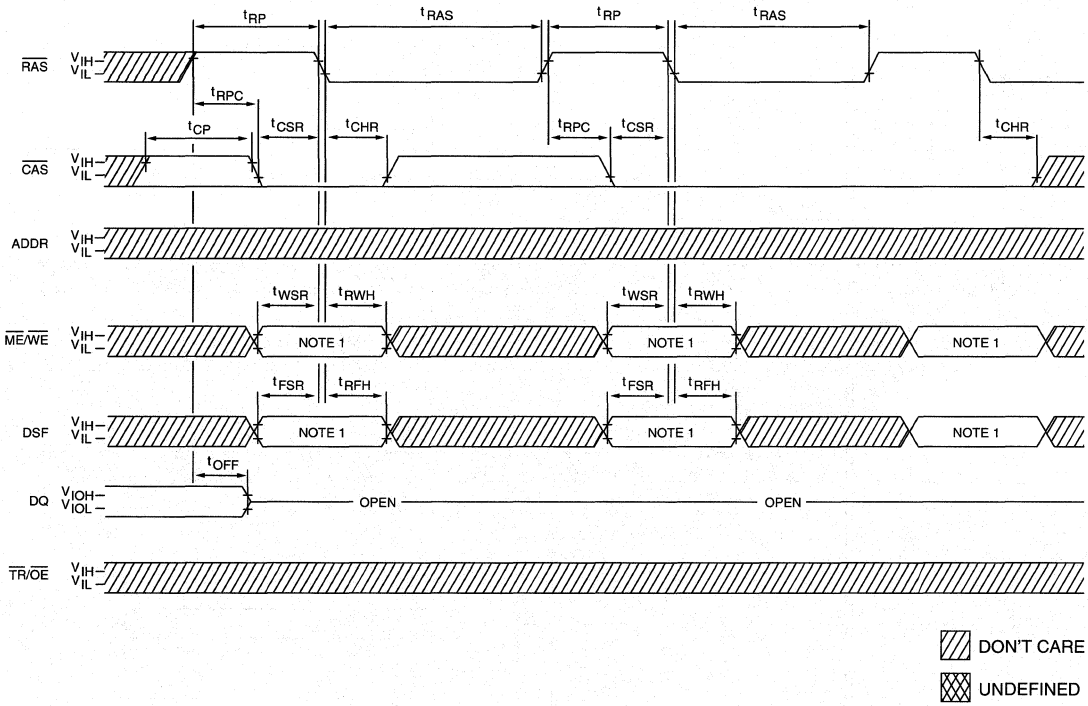
NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW VRAM MODULE

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CBR REFRESH CYCLE

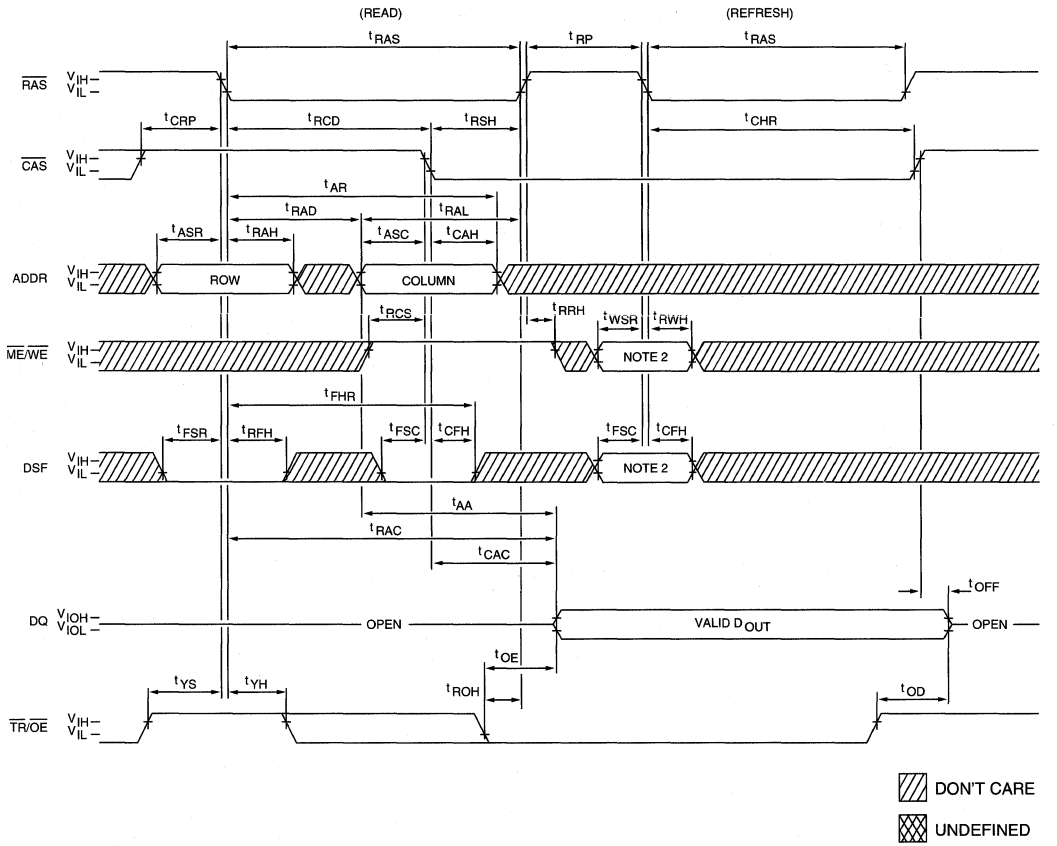


NOTE: 1. The MT4V25632 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

NEW VRAM MODULE

NEW VRAM MODULE

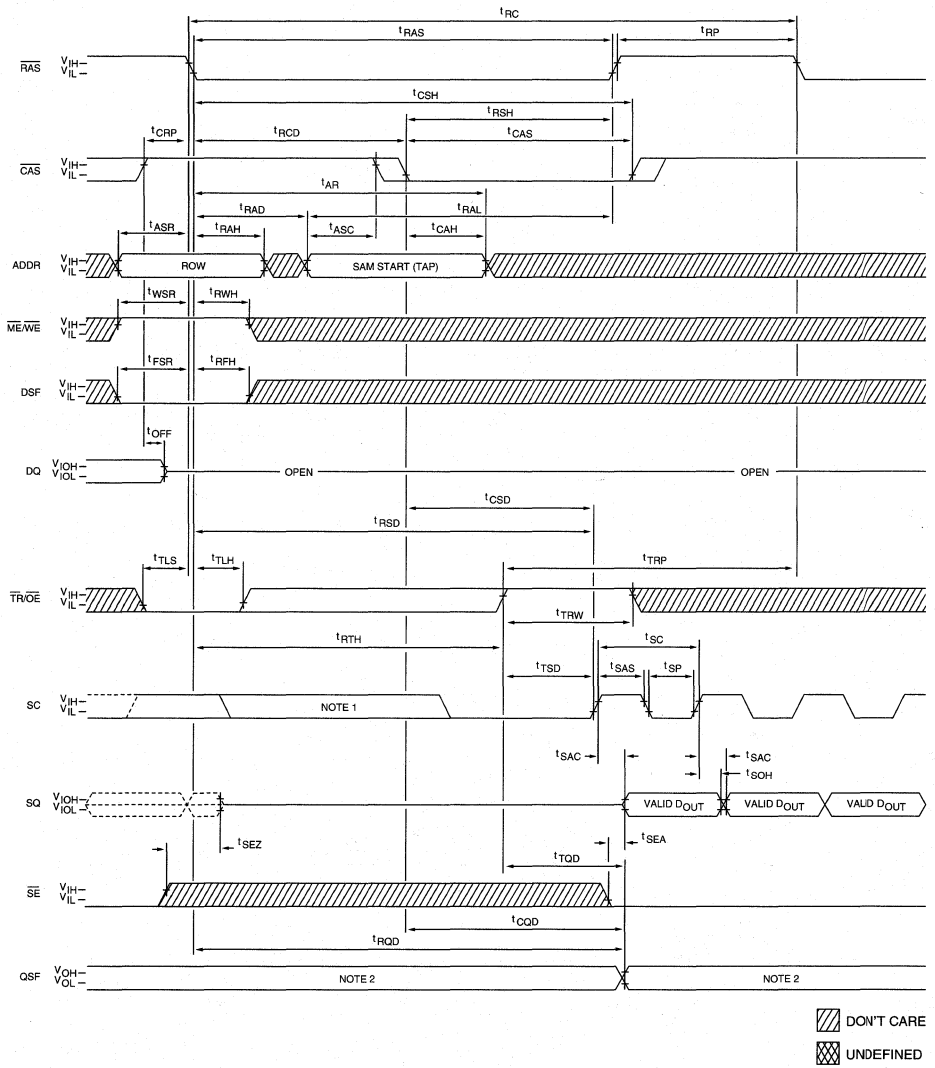
DRAM HIDDEN-REFRESH CYCLE



NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

2. The MT4V25632 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

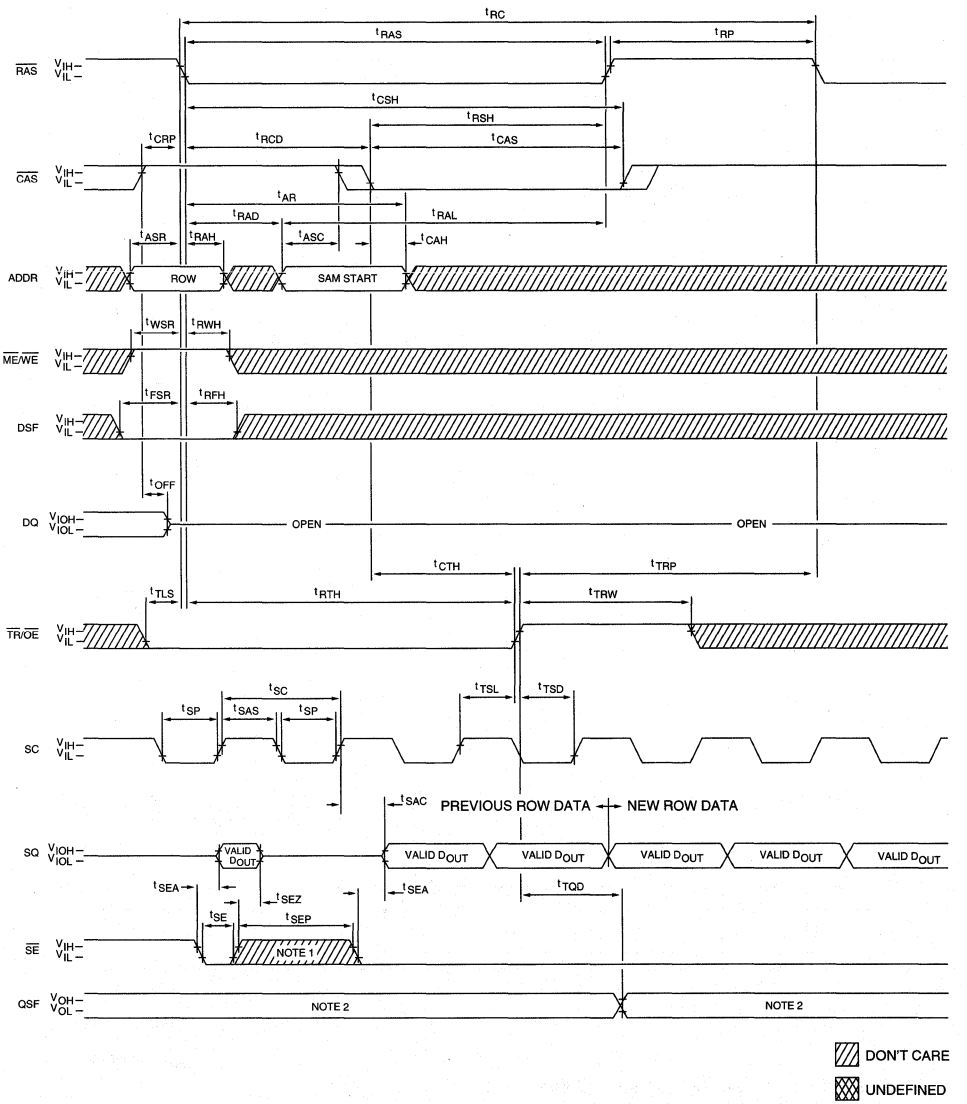
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When serial part was previously High-Z or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ^{t}TSD must be met.

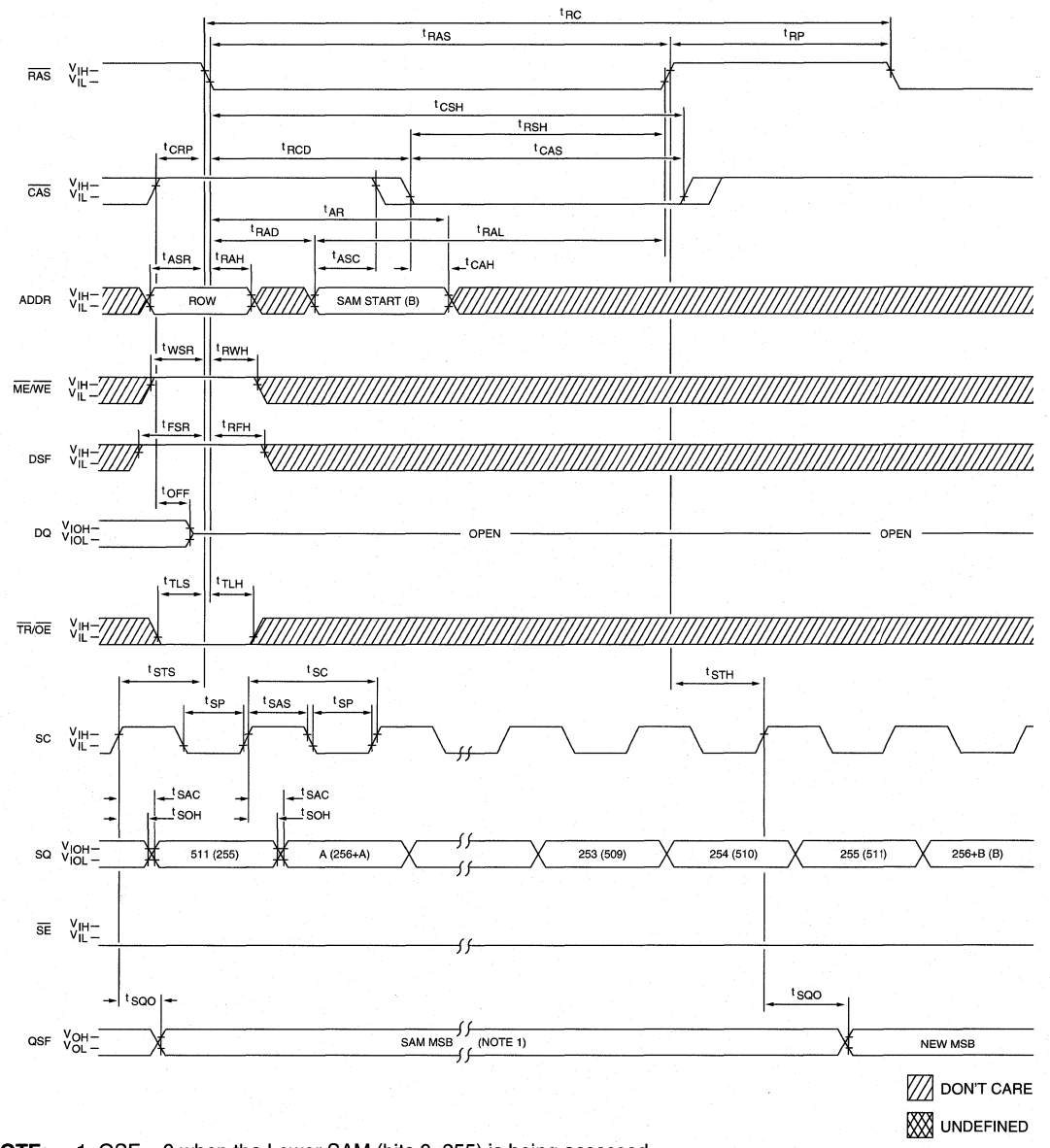
NEW VRAM MODULE

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

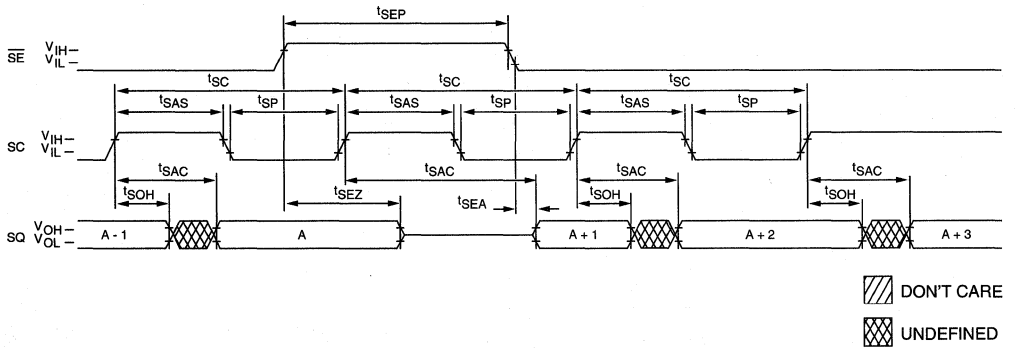
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

NEW VRAM MODULE

SAM SERIAL OUTPUT



MICRON
SEMICONDUCTOR, INC.

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated-circuit packages have a tendency to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks which might not be harmful initially could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron's customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year, and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K., et al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et al.: 26th Annual Proceeding, Reliability Physics, 1988.

TECHNICAL NOTE

TAPE-AND-REEL PROCEDURES

GENERAL DESCRIPTION

Tape-and-reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape-and-reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
52 Pin	32	16	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500

*These are examples of tape-and-reel sizes available. Please contact Micron for all available options.

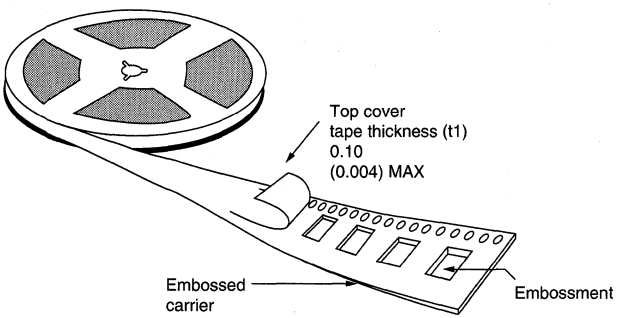


Figure 1
REEL

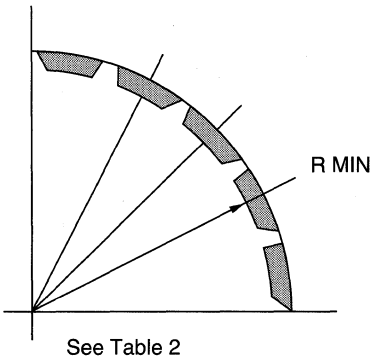
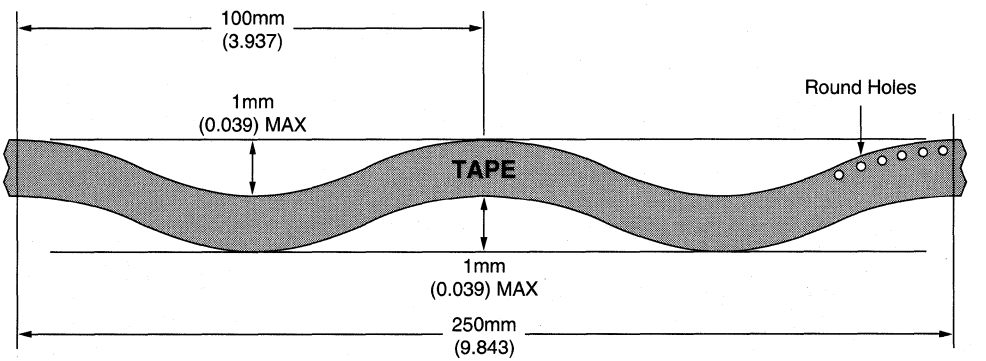


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

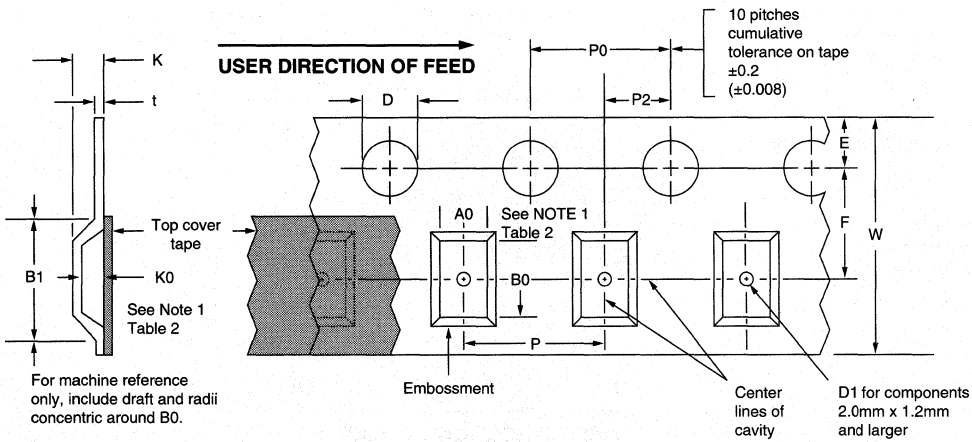


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	Note 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters, (inches).

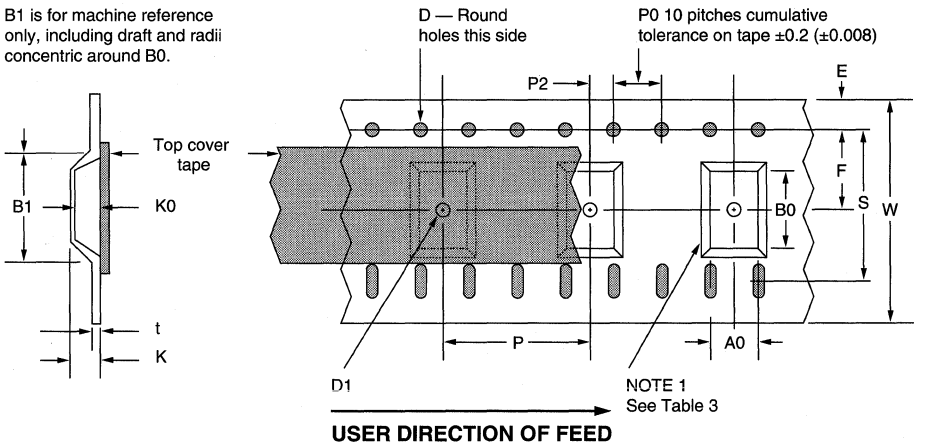


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm tape only)

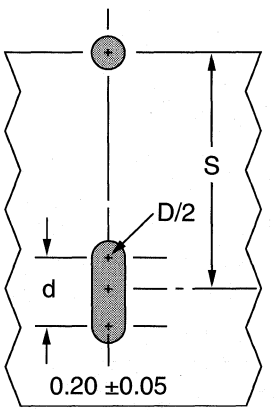


Figure 6
DETAIL ELONGATED HOLE

Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

TECHNICAL NOTE

REDUCE DRAM CYCLE TIMES WITH EXTENDED DATA-OUT

INTRODUCTION

As system speeds increase, DRAM manufacturers are developing methods to decrease the cycle times of DRAMs. The most common versions of DRAMs are FAST-PAGE (FP) and STATIC-COLUMN (SC) but the addition of a feature known as extended data-out (EDO) may become more common because it allows shorter page cycle times with only a minor functional change from FP. Because the device with EDO doesn't turn off the output drivers when $\overline{CAS}$ goes HIGH, it can have a shorter cycle time than FP.

EDO OFFERS ADVANTAGES

- It has a shorter PAGE READ cycle time than either FP or SC devices.
- Data is valid on the falling edge of $\overline{CAS}$, so the designer can use that edge to strobe data.
- A 70ns EDO device has the same PAGE READ cycle time as a 40ns DRAM.
- Implementing EDO in place of FP devices in a system can be as easy as knowing when the bus needs to be deactivated and using $\overline{OE}$ instead of $\overline{CAS}$ to accomplish it.

This article first covers some basic differences between FP, SC, and EDO during a PAGE READ cycle. Then a comparison of cycle times between FP and EDO is done, followed by a few examples under different address setup conditions. When moving from a PAGE READ into a PAGE WRITE, the timing differs slightly between FP and EDO; this difference is discussed. Finally, the issues involved when replacing an FP device with an EDO device are addressed.

BASIC DESCRIPTION

FP, SC and EDO all allow fast data operations within a row. The differences are in the latching of the column-

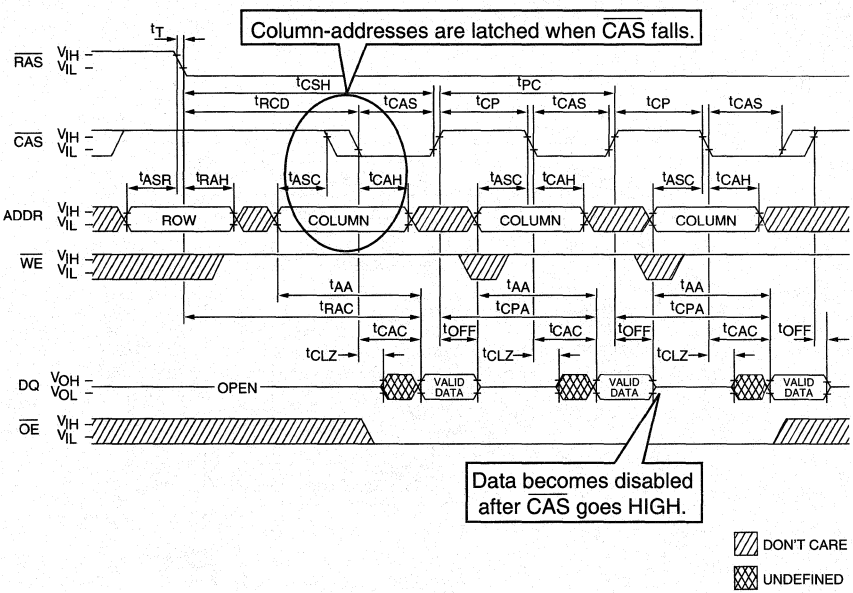


Figure 1
FP READ CYCLE

NEW APPLICATION/TECHNICAL NOTE

address and deactivating data-out when $\overline{CAS}$ goes HIGH. The following section highlights differences between the FP, SC and EDO when reading within a page.

FP MODE

Characteristics:

- The column-address is latched when $\overline{CAS}$ falls.
- The output drivers are turned off when $\overline{CAS}$ goes HIGH.
- Minimum FP READ cycle time is ${}^{t}PC = {}^{t}CPA + {}^{t}T$, $({}^{t}CPA = {}^{t}AA + {}^{t}T)$

The cycle begins with $\overline{RAS}$ strobing-in a row address, followed by $\overline{CAS}$ strobing-in a column-address. To continue to access columns within that row, $\overline{CAS}$ is toggled as addresses change.

Figure 1 shows a typical FP READ cycle. The column-address is latched into the part when $\overline{CAS}$ falls, so column-address setup and hold times are referenced to the falling edge of $\overline{CAS}$. Notice ${}^{t}OFF$; this specification tells you that $\overline{CAS}$ going HIGH turns off the output drivers.

SC MODE

Characteristics:

- The column-address is not latched when $\overline{CAS}$ falls.
- The output drivers are turned off when $\overline{CAS}$ goes HIGH.
- Minimum SC READ cycle time is ${}^{t}SC = {}^{t}AA + {}^{t}T$.

The cycle begins the same as FP, but to continue accessing columns within a row, $\overline{CAS}$ may be left LOW with only the addresses changing. The address is not latched when $\overline{CAS}$ falls. Instead, $\overline{CAS}$ acts as a transparent latch that is enabled when $\overline{CAS}$ is LOW. As long as $\overline{CAS}$ is LOW, the column-address will flow through into the device and the part will start retrieving that address. For this reason, the address must be held valid throughout the cycle. If the address is changed before data-out becomes valid, the device will start retrieving the new address and not put out data for the previous address.

Figure 2 shows a typical SC read cycle. Notice that there are no address setup and hold times, because addresses are not latched. The address can be changed once ${}^{t}AA$ has been met and the device will hold data valid for 5ns from the address change (${}^{t}AOH$). As you can see, the SC READ cycle time would be ${}^{t}SC = {}^{t}AA + {}^{t}T$. The benefit of SC over the FP is that the cycle time is shorter by one transition (generally 5ns). The disadvantage is that the user must hold the column-address valid throughout the entire cycle.

EDO

Characteristics:

- The column-address is latched when $\overline{CAS}$ falls.
- The output drivers are not turned off when $\overline{CAS}$ goes HIGH.
- Minimum FP read cycle time is ${}^{t}PC = {}^{t}AA$.

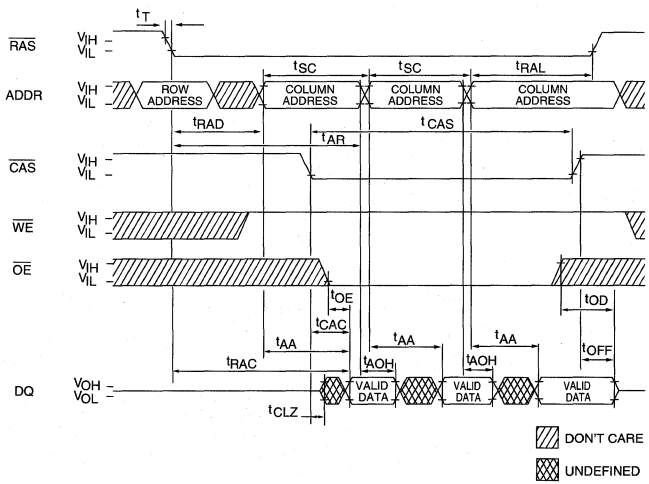


Figure 2
SC Cycle

EDO allows fast access within a row and uses $\overline{CAS}$ to latch the column-address, as does FP, but does not turn off the output when $\overline{CAS}$ goes HIGH. This last feature allows EDO to cycle faster than either FP or SC, because the user does not have to wait for valid data to appear before starting the next access. In other words, data can appear after $\overline{CAS}$ has been pulled HIGH, and it will stay valid for 5ns after $\overline{CAS}$ transitions LOW again (^{t}COH), as shown in Figure 3. Notice that there is no ^{t}OFF in the PAGE READ of the EDO diagram. The output will deactivate when both $\overline{RAS}$ and $\overline{CAS}$ are HIGH, so ^{t}OFF will now be referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

PAGE READ CYCLE TIMES

This section examines the different cycle times of FP and EDO and see how they are generated. Figure 1 shows that $\overline{CAS}$ must stay LOW until data-out becomes valid (if $\overline{CAS}$ goes HIGH before valid data, then the output buffers would turn off). The longest access time specified for the device is from $\overline{CAS}$ HIGH to data-out (^{t}CPA). $\overline{CAS}$ can't go HIGH before ^{t}CPA, or data-out will not fire. Add a transition time to pull $\overline{CAS}$ HIGH and you have the cycle time $^{t}PC_{FPM}$ = ^{t}CPA + ^{t}T.

EDO works a bit differently. ^{t}CPA is still the longest access time, but is no longer the limiting parameter in cycle time. This is because some of this access time includes $\overline{CAS}$ precharge ($\overline{CAS}$ HIGH time). In FP, you can't bring $\overline{CAS}$ HIGH before data is valid because $\overline{CAS}$ HIGH turns data off. Since $\overline{CAS}$ HIGH doesn't turn off data in the EDO device, you can bring $\overline{CAS}$ HIGH before data is valid and begin precharging $\overline{CAS}$ while you wait for data-out. This overlap of $\overline{CAS}$ precharge and getting data-out means ^{t}CPA is no longer the limiting parameter, because ^{t}CPA includes $\overline{CAS}$ precharge. Now ^{t}AA is the longest access time, so $^{t}PC_{EDO}$ = ^{t}AA. This is the shortest cycle time of the three modes.

EXAMPLES: EDO AND FP

The table below compares page READ cycles of FP and EDO under two different conditions: minimum column-address setup and maximum column-address setup time. The timing diagrams for the following examples assume that $\overline{RAS}$ is already LOW, $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW. A 70ns DRAM is used with the following timing:

DESCRIPTION	FP	EDO
^{t}PC (MIN)	45	35
^{t}CAS (MIN)	20	15
^{t}CLZ (MIN)	0	0
^{t}OFF	0-20	0-20
^{t}T	5	5

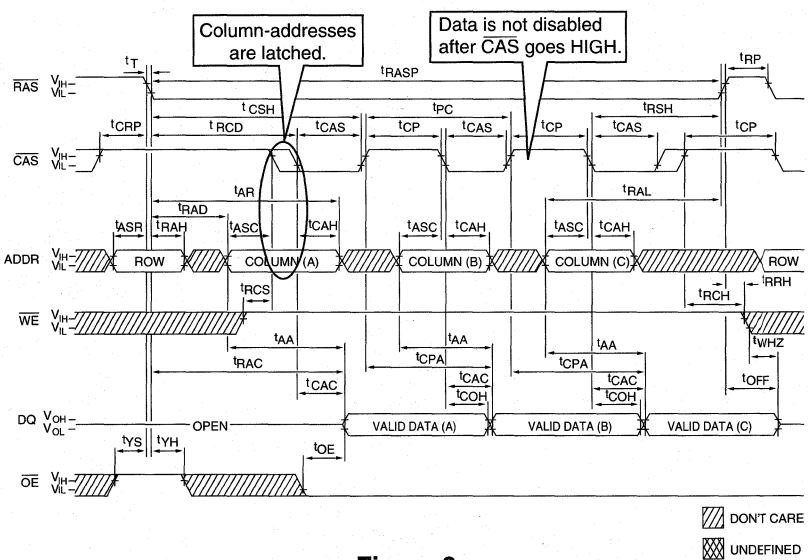


Figure 3
FP READ WITH EDO

Figures 4 and 5 show FP and EDO cycles with plenty of address setup time. On an FP device with plenty of address setup time, we can operate at ^{t}PC = 45ns (the minimum allowed), and data is valid for 5ns.

EDO under the same address setup time looks different (see Figure 5). Now the minimum cycle time is 35ns. Notice that data doesn't appear on the bus until you are already into the second access (5ns of $\overline{CAS}$ precharge for the next cycle is already completed when data appears). This is the overlap that allows the shorter cycle time. ^{t}PC is 35ns and data is valid for 15ns.

Under these conditions, EDO cuts the cycle time over an FP device by 22 percent (45ns to 35ns). In addition, even with the shorter cycle time, data-out is valid for 15ns on the EDO as opposed to only 5ns on the FP device.

Figures 6 and 7 show FP and EDO cycles with minimum address setup time. In this case, the address becomes valid coincident with $\overline{CAS}$ falling. For FP, data won't be valid for ^{t}AA(35ns), so $\overline{CAS}$ must be held LOW until that time (see Figure 6). Since the minimum $\overline{CAS}$ HIGH time is 10ns, the cycle time is 50ns (^{t}AA + ^{t}CP + ^{t}T). Data-out is valid for 5ns.

Looking at EDO under the same conditions, (Figure 7) it still takes ^{t}AA (35ns) after the addresses are valid to get valid data-out, but now you don't have to wait before pulling $\overline{CAS}$ HIGH. Notice that $\overline{CAS}$ has been pulled HIGH and precharge has been completed for the next cycle, before Data 1 appears on the bus. As data becomes valid, $\overline{CAS}$ drops and the second address is latched. Again, there is an overlap of starting one cycle and finishing the other. Now ^{t}PC = 35ns, and data-out is valid for 10ns.

In this case, EDO cycle time (35ns) is 30 percent less than the FP cycle time (50ns); EDO data is valid 5ns longer.

These examples should point out another big advantage of EDO. Not only can you operate at a shorter cycle time, but data is available longer for the system to sample. Since data is guaranteed to be valid as $\overline{CAS}$ falls, that edge may be used to sample data.

70ns EDO INSTEAD OF 40ns DRAMs

EDO can provide the FP READ speed of a 40ns DRAM. Even though a 40ns DRAM has a 40ns ^{t}RAC, the FP READ cycle time is 35ns, which is the same page READ cycle time as that of a 70ns EDO device.

EASY TO IMPLEMENT

An additional benefit of EDO is the ease of implementation. PAGE READ or WRITE cycle time is cut by 10ns, but the only difference between FP and FP with EDO is that the FP device will stop driving data-out when $\overline{CAS}$ goes HIGH

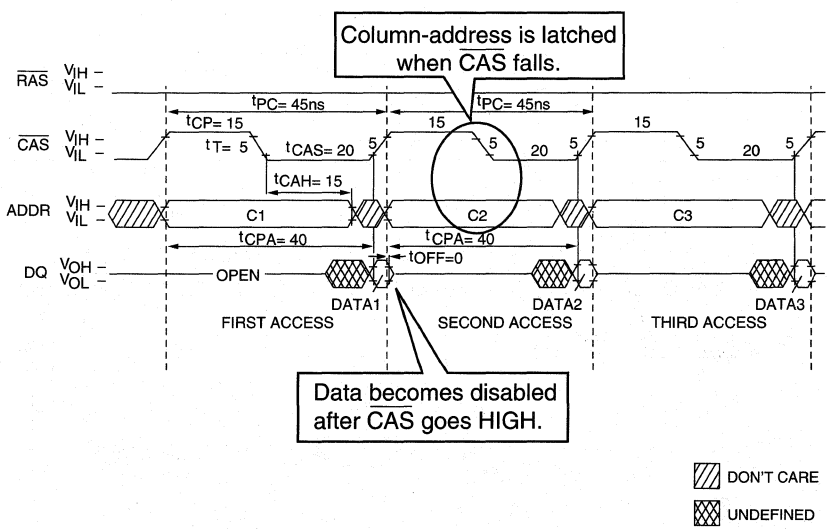


Figure 4
FP PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 45ns; DATA VALID FOR 5ns

and the EDO device must have both $\overline{CAS}$ and $\overline{RAS}$ HIGH to deactivate the output. This means that any time the designer is counting on $\overline{CAS}$ by itself to turn off the output drivers, bus contention may occur if something else tries to drive the bus. This may occur in the following situations:

- PAGE interleave memory banks
- Moving from PAGE READ directly into a PAGE WRITE (within the same page)
- Whenever anything other than the DRAM is driving the bus, and $\overline{OE}$ and $\overline{RAS}$ are LOW while $\overline{CAS}$ is HIGH

(This last case is uncommon and should not mandate a change for most systems.) Interleaved memory need only make use of $\overline{OE}$ instead of $\overline{CAS}$ when turning off the output drivers; then EDO can be used in place of FP DRAMS.

READ TO WRITE CYCLES

Since $\overline{CAS}$ doesn't turn off the output devices on an EDO device, caution should be used when turning the bus around on a shared I/O device. To demonstrate the difference, Figure 8 shows the transition from a PAGE READ to a PAGE EARLY WRITE on the same page. When using the FP version, $\overline{OE}$ can be tied LOW and $\overline{CAS}$ can be used to deactivate the output. When using the EDO version, $\overline{OE}$ must be used to deactivate the output.

SUMMARY

EDO is simply a modified FP MODE cycle and can be used in systems to increase performance. It allows system designers to improve their cycle times and system performance since data is present for a much longer time, even during short cycle times.

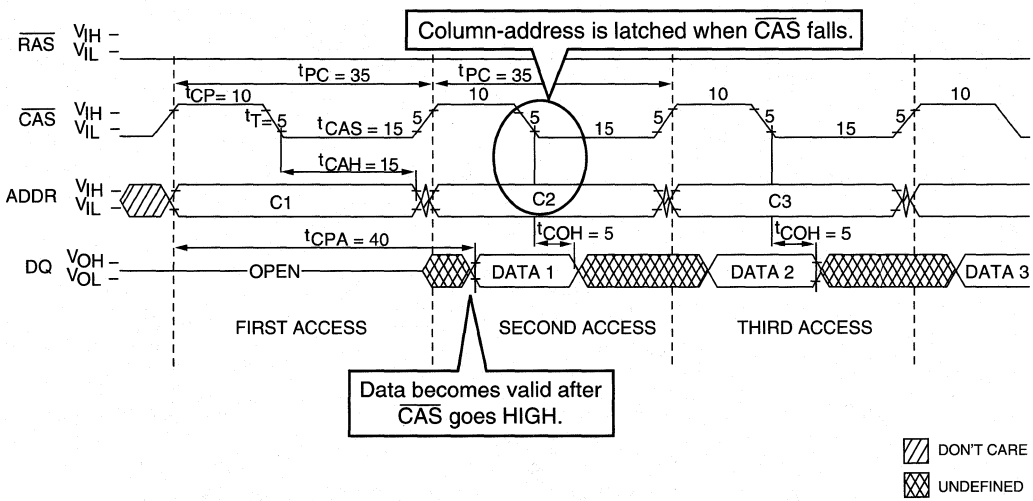


Figure 5
EDO-PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 45ns; DATA VALID FOR 15ns

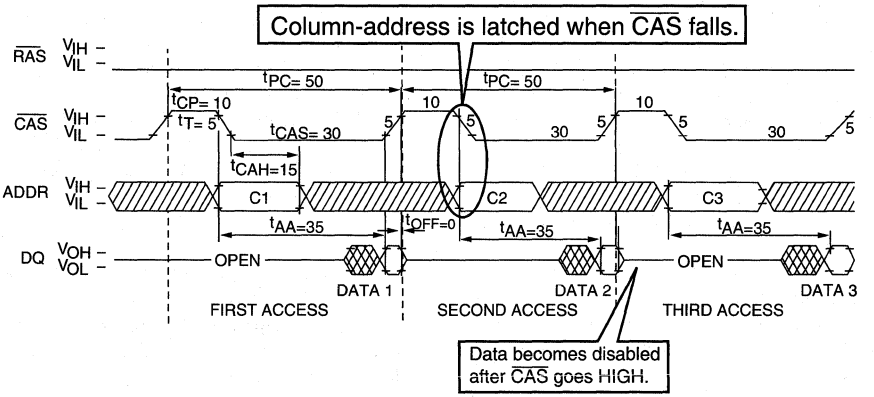


Figure 6
PAGE READ WITH MINIMUM ADDRESS SETUP
^{t}PC = 50ns; DATA VALID FOR 5ns

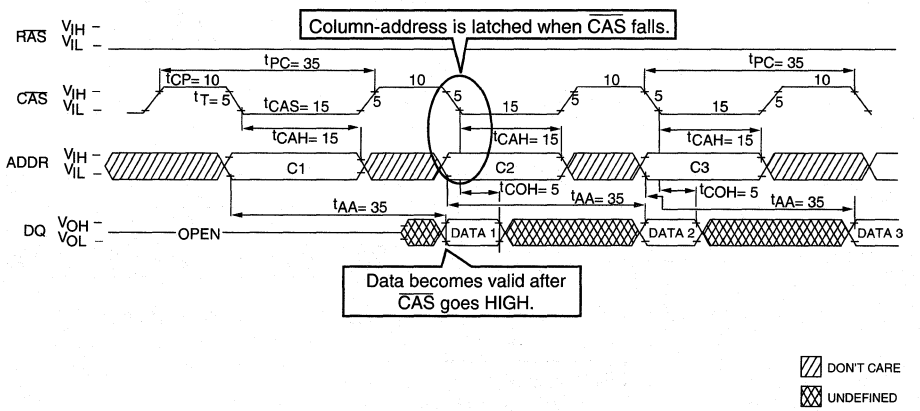


Figure 7
EDO-PAGE READ CYCLE WITH MINIMUM ADDRESS SETUP
^{t}PC = 35ns; DATA VALID FOR 10ns

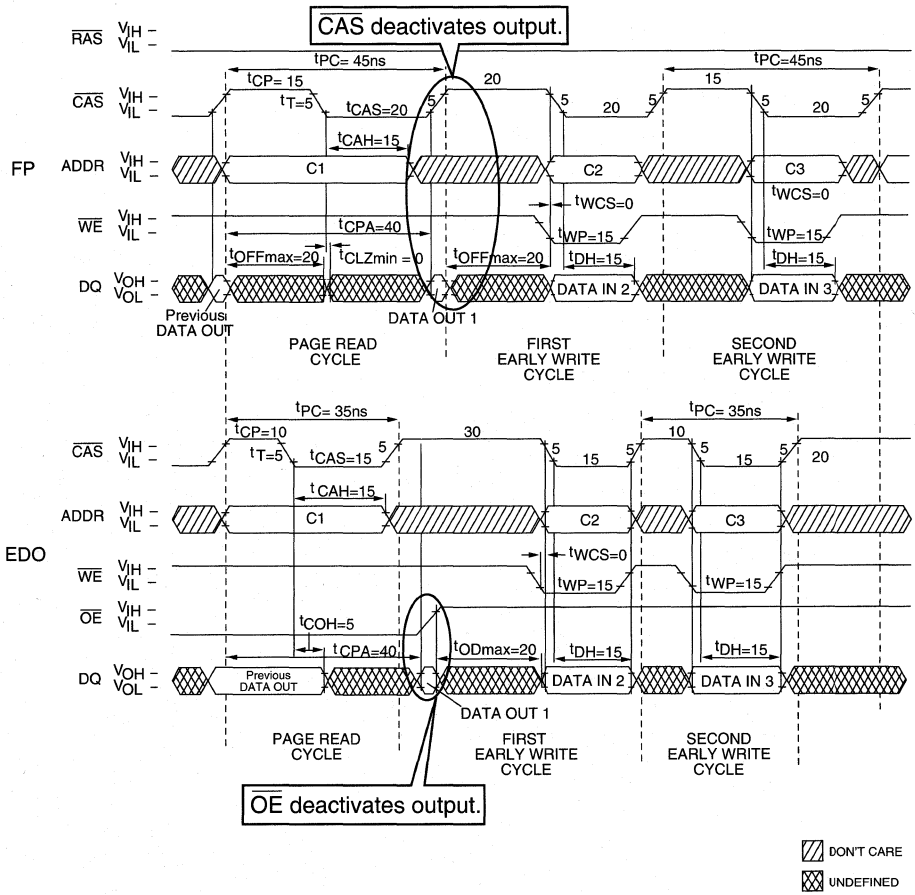


Figure 8
EXAMPLE FP AND EDO READ TO WRITE CYCLES
^{t}PC = 45ns

NEW APPLICATION/TECHNICAL NOTE

NEW APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

UPGRADING FROM 1 MEG TO 2 MEG VRAMs

INTRODUCTION

Designers of VRAM-based graphics systems are now being presented with the opportunity to switch from 1 Meg to 2 Meg VRAMs. As with any move to higher density memory devices, this allows a system to be modified to either provide the same amount of total memory while using fewer devices, or to provide additional memory without increasing the number of devices used. When the total memory size remains the same, benefits include decreased board space due to fewer components, increased reliability due to fewer connections, and lower component cost when the cost-per-bit of the higher density components falls below that of the lower density components. An additional benefit of switching from 1 Meg to 2 Meg VRAMs is the availability of a more advanced feature set at the 2 Meg level.

Micron offers four versions of the 2 Meg VRAM; each addresses different user needs and each has different design requirements. When switching from 1 Meg VRAMs, the memory configuration, the required feature set and the board layout determine which version of the 2 Meg to switch to and the design effort involved. This article covers each of these three major areas of concern. In the area of memory configuration, the effects of specific factors on the design of the graphics memory controller are discussed. These factors include whether the 1 Meg VRAMs currently used are organized as x4 or as x8, the number of VRAM banks and whether or not the total memory size will be increased. In the area of feature sets, the different sets of functions available at the 2 Meg level are compared to the functions available at the 1 Meg level. Finally, in the area of physical layout, the different packages offered at the 1 Meg and 2 Meg levels are described.

MEMORY CONFIGURATION

Based on the memory configuration factors mentioned above, there are several possible scenarios when switching to 2 Meg VRAMs, ranging from straightforward intrabank replacement transparent to the graphics memory controller, to more involved memory expansion or interbank replacement; the latter two have controller implications. The following examples illustrate the different scenarios.

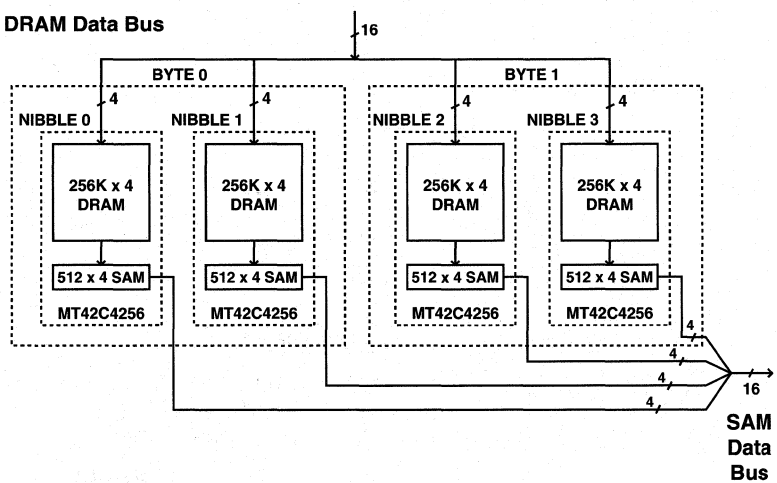


Figure 1
0.5 MB MEMORY ARRAY WITH A 16-BIT INTERFACE USING 1 MEG VRAMs

CASE 1: x4, 1 MEG VRAMS VS x8, 2 MEG VRAMs
Replacement of 4-bit-wide 1 Meg VRAMs with 8-bit-wide 2 Meg VRAMs is the most straightforward case when upgrading. This is illustrated in Examples 1 and 2.

Example 1
A 0.5 MB memory array implemented with a single bank of 4-bit-wide 1 Meg VRAMs (Micron's MT42C4256) is shown in Figure 1. The DRAM portion of the MT42C4256 is organized as 256K x 4, or 512 rows by 512 columns by 4 bits wide. The DRAM portion of 2 Meg VRAMs is organized as 256K x 8, or 512 rows by 512 columns by 8 bits wide. When the data bus interface to the DRAM side of the memory array is 16 bits wide, four 4-bit-wide 1 Meg VRAMs are required, each corresponding to one nibble of the 16-bit bus. A 16-bit data bus also exists on the SAM side.

When using 2 Meg VRAMs, only two devices are required (see Figure 2). The first corresponds to the byte formed by nibbles 0 and 1; the second, to nibbles 2 and 3. Similarly, on the SAM side, each pair of 512 x 4 SAMs (1 Meg VRAM) is replaced by a single 512 x 8 SAM (2 Meg VRAMs). Assuming that there is no need for NIBBLE READ accesses, this two-for-one replacement is transparent to the controller (NIBBLE WRITE accesses are available with the MT42C8254, if necessary, and will be covered under Feature Sets).

The examples depicted in figures 1 and 2 can be extended to wider controller-to-memory interfaces as well. (For example, in a 32-bit interface, four 2 Meg VRAMs would replace eight 1 Meg VRAMs.)

Example 2
Example 1 can also be extended to more than one bank of VRAMs simply by performing the two-for-one replacements within each bank. For example, a memory array configured as two banks of eight 1 Meg VRAMs would be replaced with two banks of four 2 Meg VRAMs (see Figures 3 and 4). In either case, the controller must include the necessary bank-select logic.

CASE 2: x8, 1 MEG VRAMs VS x8, 2 MEG VRAMs
Moving from 8-bit-wide 1 Meg VRAMs to 8-bit-wide 2 Meg VRAMs is somewhat more involved. This is shown in Examples 3 and 4.

Example 3
Figure 5 shows a 0.5 MB memory array based on 8-bit-wide 1 Meg VRAMs (Micron's MT42C8128). An equivalent memory array cannot be implemented with 2 Meg VRAMs due to the fact that four 2 Meg VRAMs are needed to form a 32-bit bus, and the resulting total memory array size then equals 1 MB. To move to 2 Meg VRAMs in this example requires a controller designed to support such memory expansion.

Example 4
On the other hand, a 1 MB memory array implemented with 8-bit-wide 1 Meg VRAMs would contain two banks (see Figure 6). Bank select logic determines which DRAMs and SAMs drive the respective busses at any given time.

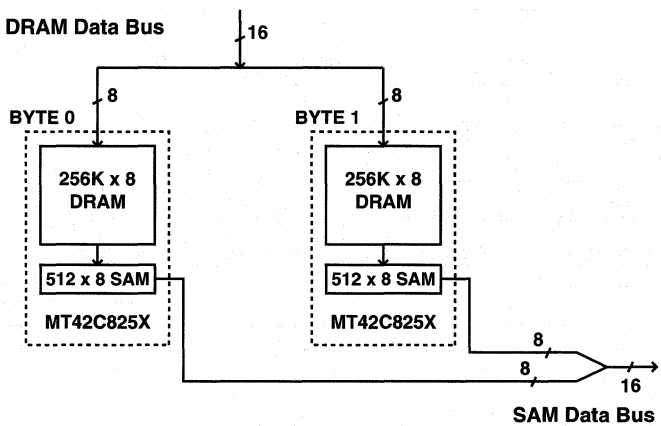


Figure 2
0.5 MB MEMORY ARRAY WITH A 16-BIT INTERFACE USING 2 MEG VRAMs

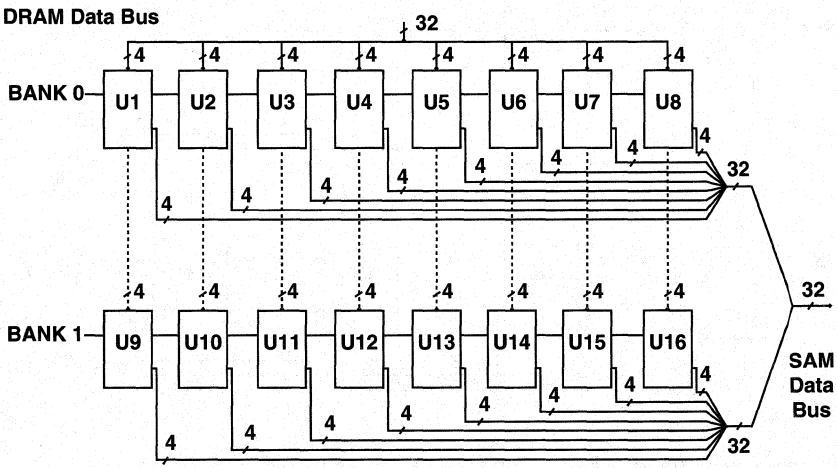
In this case, a memory array of equal size can be implemented with 2 Meg VRAMs; however, the array will consist of one bank instead of two (see Figure 7). This can be pictured as two-for-one replacements across the banks rather than within the banks. In this example, moving to 2 Meg VRAMs requires a controller that can address a second megabyte of memory through an additional column-address line rather than the bank-select logic used for the 1 Meg VRAM based implementation.

FEATURE SETS

When deciding upon the appropriate 2 Meg VRAM, there are three feature sets to consider. The first set is the one currently implemented in the 1 Meg VRAM-based design, the second and third sets are those offered by the two different categories of 2 Meg VRAMs. The first category, consisting of the Micron MT42C8254 and MT42C8255, provides standard features; the second, consisting of the MT42C8256 and MT42C8257, offers an extended feature set (see Table 1). In general, the standard features satisfy the requirements of PC graphics systems such as VGA/GUI accelerator designs, and the extended feature set addresses the needs of workstation graphics systems and communications systems.

When switching from 1 Meg VRAMs, designers will need to select an extended feature 2 Meg VRAM under any of the following conditions: 1) PERSISTENT WRITE functions were used at the 1 Meg level, 2) serial input or write transfers are required, 3) any of the functions introduced at the 2 Meg level will be supported. These additional features include the FLASH WRITE cycles, the MASKED WRITE TRANSFER cycles and the programmable split SAM. If an extended feature set 2 Meg VRAM is selected, the designer needs to be aware of some instruction decode changes between 1 Meg and 2 Meg VRAMs. Specifically, the input states which select a PERSISTENT MASKED WRITE to DRAM at the 1 Meg level are now used to select a MASKED FLASH WRITE to DRAM at the 2 Meg level. In order to support both features on one device, PERSISTENT WRITE functions are now selected automatically upon the loading of the mask register (and deselected with special $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ (CBR) cycles). Similarly, the input states that select an ALTERNATE WRITE TRANSFER at the 1 Meg level are now used to select a SPLIT WRITE TRANSFER at the 2 Meg level. The ALTERNATE WRITE TRANSFER is not offered at the 2 Meg level.

The above guidelines should be used to select the appropriate category of 2 Meg VRAMs. The next step is to determine which of the two devices within each category matches the needs of the specific application.



U1-U16: MT42C4256 VRAM (256K x 4 DRAM plus 512 x 4 SAM)

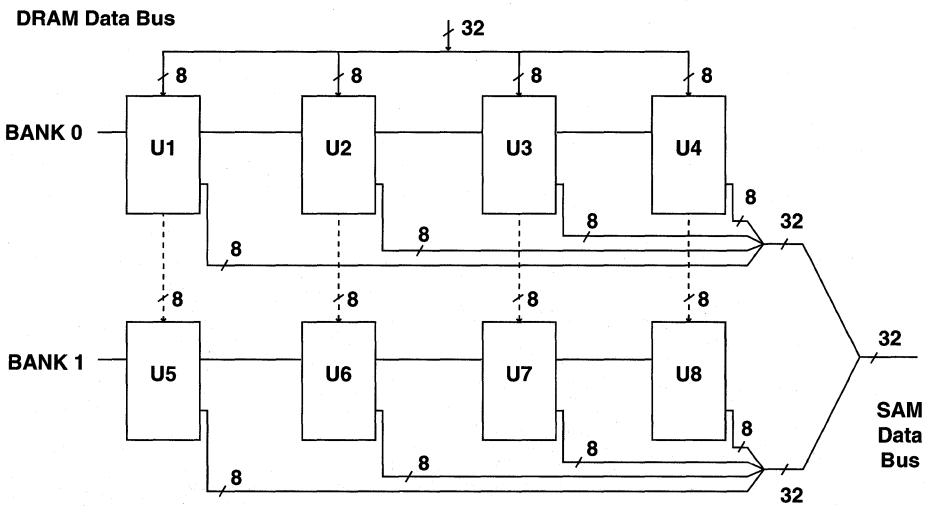
Figure 3
A 2 MB MEMORY ARRAY, WITH A 32-BIT INTERFACE, IMPLEMENTED WITH 1 MEG VRAMs

STANDARD FEATURE SET 2 MEG VRAMs: MT42C8254 VS MT42C8255

Once it is determined that a standard feature set 2 Meg VRAM is appropriate, the designer has a choice of either the MT42C8254 or the MT42C8255. The difference between the two is that the MT42C8254 provides a second WRITE ENABLE input in place of the QSF output. The second WRITE ENABLE provides NIBBLE WRITE capability. The QSF output available on the MT42C8255 indicates which half of the SAM is currently active (the half from which serial data is being read). The controller can use this information to initiate SPLIT READ TRANSFERS; however, many controllers keep track of this internally and do not require the QSF signal from the VRAM. If NIBBLE WRITE capability is required, the MT42C8254 must be used and the controller must monitor the SAM address internally. If NIBBLE WRITE capability is not required, the MT42C8255 is the appropriate choice.

EXTENDED FEATURE SET 2 MEG VRAMs: MT428256 VS MT42C8257

Similarly, once the need for an extended feature 2 Meg VRAM is established, the designer may choose either the MT42C8256 or the MT42C8257. The difference between these is that the MT42C8256 offers EXTENDED DATA-OUT on FAST-PAGE-MODE READ cycles, whereas the MT42C8257 offers standard FAST-PAGE-MODE operation. In FAST-PAGE-MODE operation with EXTENDED DATA-OUT, data being read out of the DRAM port is not disabled with the rising edge of $\overline{CAS}$ as it is in standard FAST-PAGE-MODE operation. This provides a psuedo-pipelined effect and achieves faster page mode cycle times. However, $\overline{OE}$ instead of $\overline{CAS}$ must be used to select banks in an interleaved configuration.



U1-U8: MT42C825X VRAM (256K x 8 DRAM plus 512 x 8 SAM)

Figure 4
A 2 MB MEMORY ARRAY, WITH A 32-BIT INTERFACE, IMPLEMENTED WITH 2 MEG VRAMs

PHYSICAL LAYOUT

There are no 2 Meg VRAM packages that are drop-in compatible with 1 Meg VRAM footprints. A board designed to accommodate both would have to include two sets of footprints, or a new board could be designed specifically for 2 Meg VRAM packages.

The 4-bit-wide 1 Meg VRAMs are offered in 28-lead ZIP or SOJ packages, while 2 Meg VRAMs are supplied in 40-lead SOJ or 40/44-lead TSOP packages. The 28 pins of the 1 Meg VRAM SOJ do not align with a subset of the 40 pins of the 2 Meg SOJ.

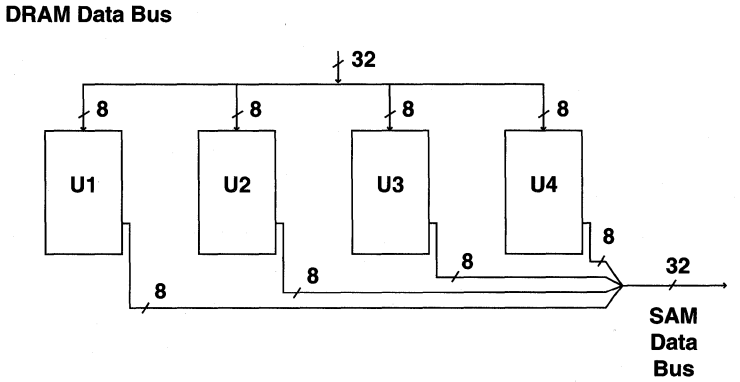
The 8-bit-wide 1 Meg VRAMs are available in 40-lead SOJ packages; however, the pin assignments do not align with those of the 2 Meg VRAM.

SUMMARY

Designers can increase system performance and reliability, while reducing board size and system costs by moving from 1 Meg VRAMs to 2 Meg VRAMs. The effort required to make this switch depends on memory configuration, required features, and physical layout. The effort might involve controller redesign, board layout redesign, or neither, if it was planned for in advance. In most cases, the added performance and reduced system costs will outweigh any forethought or redesign required.

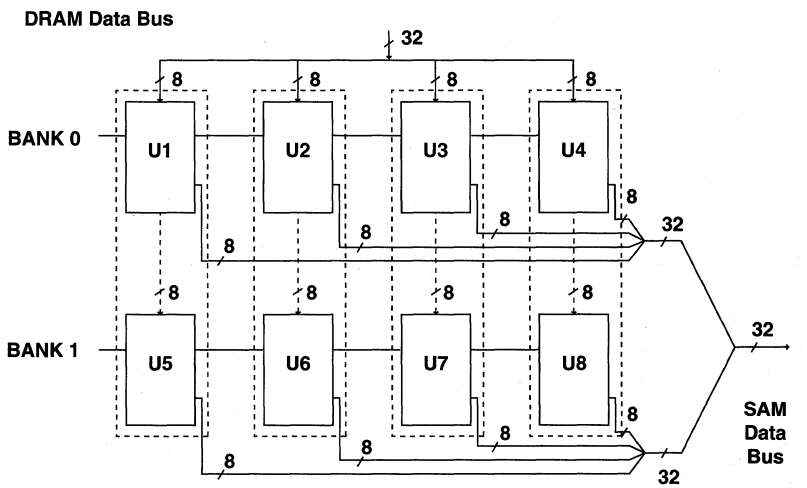
Table 1
FEATURE SETS OF 1 MEG AND 2 MEG VRAMs

Feature	1 Meg VRAM	2 Meg VRAM	
		Standard Set	Extended Set
DRAM OPERATIONS			
CBR REFRESH (RESET ALL OPTIONS)			■
CBR REFRESH (RESET STOP ADDRESS)			■
CBR REFRESH (NO RESET)	■	■	■
$\overline{\text{RAS}}$ ONLY REFRESH	■	■	■
NORMAL DRAM READ OR WRITE	■	■	■
NON PERSISTENT MASKED WRITE TO DRAM (NEW MASK)	■	■	■
PERSISTENT MASKED WRITE TO DRAM (OLD MASK)	■		■
BLOCK WRITE TO DRAM	■	■	■
NON-PERSISTENT MASKED BLOCK WRITE TO DRAM (NEW MASK)	■	■	■
PERSISTENT MASKED BLOCK WRITE TO DRAM (OLD MASK)	■		■
MASKED FLASH WRITE TO DRAM (NEW MASK)			■
MASKED FLASH WRITE TO DRAM (OLD MASK)			■
REGISTER OPERATIONS			
LOAD MASK REGISTER	■		■
LOAD COLOR REGISTER	■	■	■
TRANSFER OPERATIONS			
READ TRANSFER (DRAM-TO-SAM TRANSFER)	■	■	■
SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	■	■	■
WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NO MASK)	■		
PSEUDO WRITE TRANSFER	■		
ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	■		
MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NEW MASK)			■
MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER, OLD MASK)			■
MASKED SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER) (NEW MASK)			■
MASKED SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER) (OLD MASK)			■
PROGRAMMABLE SPLIT SAM			■



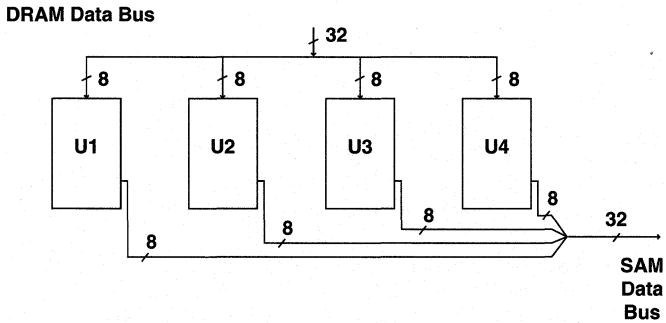
U1-U4: MT42C8128 VRAM (128K x 8 DRAM plus 256 x 8 SAM)

Figure 5
0.5 MB MEMORY ARRAY BASED ON 8-BIT-WIDE 1 MEG VRAMs



U1-U8: MT42C8128 VRAM (128K x 8 DRAM plus 256 x 8 SAM)

Figure 6
1 MB MEMORY ARRAY BASED ON 1 MEG VRAMs



U1-U4: MT42C825X VRAM (256K x 8 DRAM plus 512 x 8 SAM)

Figure 7
1 MB MEMORY ARRAY BASED ON 2 MEG VRAMs

TECHNICAL NOTE

DESIGNING WITH THE MT42C4256/8128 VRAM

INTRODUCTION

Memory buffers designed with video RAM (VRAM) will outperform similar, DRAM-based designs for a variety of applications, from graphics frame buffers to data communications and networking. Furthermore, the enhanced feature sets offered by Micron's 1 Meg VRAM can simplify and improve the performance of these designs. This note highlights the functional details of the Micron Semiconductor MT42C4256/8128 family of 1 Meg density VRAMs. All references to "VRAM" refer to the MT42C4256/8128 VRAM except where noted. The 1 Meg Triple-Port DRAMs (MT43C4257/8; 8128/9) also share common functionality with the MT42C4256/8128, all modes common between these devices are covered by this technical note.

VIDEO RAM BASICS

A VRAM is created by adding an independent static memory to a dynamic RAM (DRAM) core array. To address the bandwidth limitations of standard DRAMs, the static memory is accessed via a separate 4- or 8-bit-wide port.

The second memory buffer is referred to as a serial access memory, or SAM. It is a fully static memory equal in size to one row of the DRAM array. It is addressed in an incremental manner by an address counter/pointer that is incremented by a special clock pin, see Figure 2. This makes it well suited for high speed sequential data streams, as present in raster display graphics subsystems, network data buffers and communications.

To use the SAM as an output port, data must move internally from the DRAM array to the SAM I/O. Data written into the DRAM array from the DRAM I/O is internally moved a row at a time to the SAM by a TRANSFER cycle. The TRANSFER is facilitated by pass (transfer) gates between the DRAM column sense amplifiers and the SAM storage cells. A TRANSFER begins as any DRAM

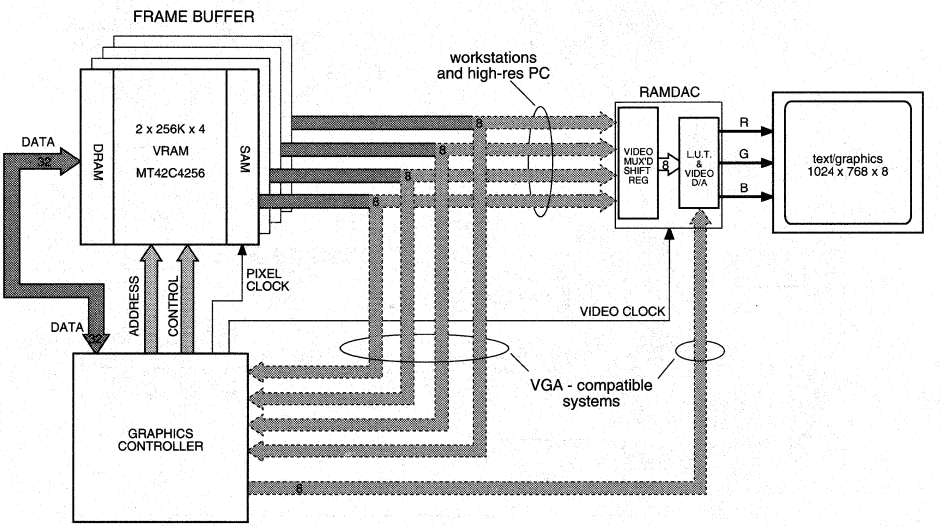


Figure 1
TYPICAL GRAPHICS APPLICATIONS FOR VRAM

access would: a row-address is selected by strobing the $\overline{RAS}$ pin. When the row is selected, the contents of all its capacitive storage elements are "read" by the column sense amplifiers. Once the data from the row is amplified ("opened"), it is ready to be sent to the output pins or overwritten from the input pins of the DRAM. A TRANSFER begins by opening a row in the same manner, but there the similarity ends. During a transfer, the data is passed (as an entire row) between the sense amps and the SAM static latches residing at the "end" of each column. Micron VRAMs incorporate bidirectional SAMs that can be configured to output data, as described above, or input data and then "write" it into a DRAM row.

Once the row is open, the DRAM access cycle selects a column-address by strobing $\overline{CAS}$. This selects the specific column sense amps that will drive a unique word to the outputs. A VRAM TRANSFER cycle does not input or output data at the DRAM I/O. Instead, the column-address is latched into a SAM "Tap" address buffer. The Tap address defines the column-address at which SAM input or output will begin.

The type of TRANSFER cycle performed determines the direction of the data flow of the SAM. Transfers are referenced from the DRAM. A READ TRANSFER means that data is read from the DRAM to the SAM and sets the SAM I/O as an output. A WRITE TRANSFER writes information from the SAM to the DRAM and sets the SAM I/O to the input direction.

Figure 1 illustrates a basic graphics frame buffer using VRAM devices. The DRAM port is accessed and controlled by a graphics controller or coprocessor. This port is used to update the display pixel data, perform DRAM refresh and control TRANSFERS from the DRAM array and the SAM. The SAM supplies the pixel data to the raster-video display circuitry. This consists of a video digital-to-analog converter (DAC) and an SRAM-based look-up table (LUT). Most systems also utilize a high-speed multiplexed shift register, or a DAC incorporating one, to increase the effective pixel rate without requiring the SAM clock to run at the video pixel, or dot clock, rate (80 MHz or more). Many video DACs also incorporate the LUT and are referred to as palette DACs or RAMDAC™s.

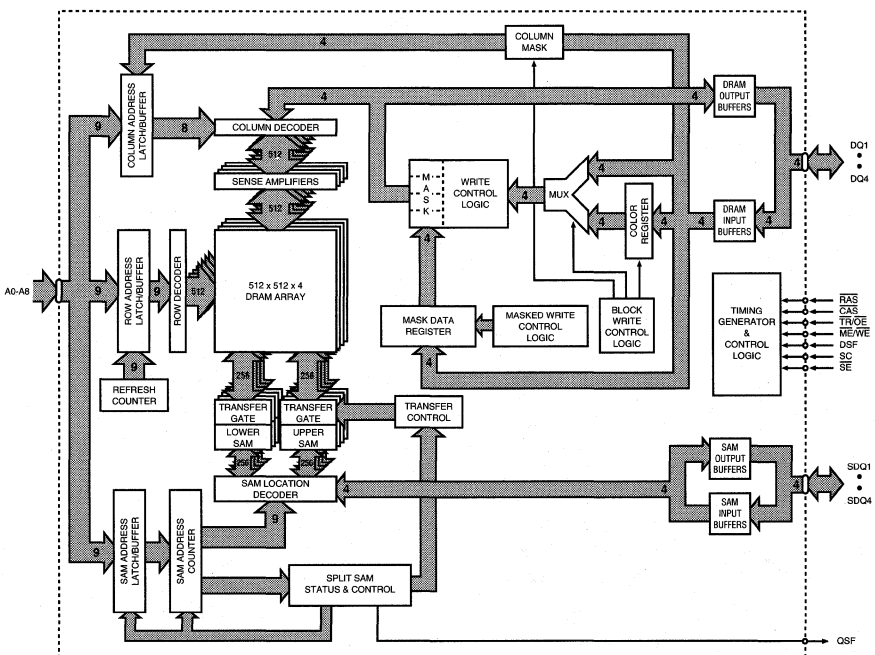


Figure 2
MT42C4256 FUNCTIONAL BLOCK DIAGRAM

In systems with VGA-compatible controllers, the SAM data is routed back through the controller. In these cases, the video multiplexer is incorporated in the controller. This reduces the cost and complexity of the DAC required. To get full advantage of the VRAM bandwidth, the VGA controller should have separate I/O for the DRAM and SAM ports.

The serial clock for the SAM is derived by dividing the pixel clock by the number of pixels accessed per SAM clock cycle. It may be generated by the controller or by the palette DAC depending on the implementation and components chosen.

ADVANTAGE OF VRAM OVER DRAM

VRAMs were developed to increase the bandwidth of raster graphic display frame buffers. If DRAM is used to build the frame buffer, it must allow access by both the host/graphics controller and the CRT refresh circuitry. The nature of raster graphics displays requires that a constant, uninterrupted flow of pixel data be available to the CRT driver circuitry. Because of this, it is the host or graphics processor that must be interrupted when a request is made by the CRT driver for a new line of pixel data (scan line). DRAM-based frame buffers suffer from data contention at the DRAM port that reduces screen redraw speed. A 1 Megabyte frame buffer designed with 70ns, single-port DRAMs would use 90 percent or more of the total memory bandwidth to perform screen refresh. This leaves 10 percent or less of the bandwidth for drawing new pixels to the display. Obviously, this will result in a noticeably slower display time when new information is to be displayed. When designed with 70ns VRAM, a similar frame buffer would only utilize two percent of the total bandwidth for screen refresh, resulting in screen redraw performance improvement of roughly an order of magnitude.

VRAM-based frame buffers are designed to give the CRT driver circuitry access to pixel data from the SAM port, thus alleviating the DRAM-port contention problem as seen with DRAM-based buffers (see Figure 1). This results in improved screen redraw performance over DRAM-based buffers when changing display information. DRAM-port accesses to the VRAM must be interrupted for READ TRANSFERs from the DRAM array to the SAM, but they occur infrequently since an entire row (page) of data is transferred per cycle. DRAM-port access is available to the graphics controller or coprocessor while screen refresh data is constantly supplied, independently, by the SAM port.

Other features of the VRAM further enhance graphics performance. These "special features" of Micron's 1 Meg VRAM include: MASKED WRITE, BLOCK WRITE, and SPLIT READ TRANSFER. These features, and the TRANSFER cycles, are detailed in the following sections, along with other features of Micron's 1 Meg VRAM.

SAM TRANSFERS

Data TRANSFERs move data between the two VRAM memory arrays. These cycles are variations of a normal DRAM $\overline{RAS}$-$\overline{CAS}$ cycle. To incorporate TRANSFERs, the VRAM's $\overline{OE}$ pin is made a dual-function pin and called Transfer Enable/Output Enable ($\overline{TR}/\overline{OE}$). At the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ is sampled; if it is LOW, the cycle will be a TRANSFER. Once a TRANSFER is selected, its direction must be defined. This also occurs at the falling edge of $\overline{RAS}$ by the level of the $\overline{ME}/\overline{WE}$ pin. When $\overline{ME}/\overline{WE}$ is LOW, a WRITE TRANSFER is selected; when $\overline{ME}/\overline{WE}$ is HIGH, a READ TRANSFER is selected. A mode-select pin called DSF is used during TRANSFERs to define variants of the standard READ and WRITE TRANSFERs. This pin is also latched at the falling edge of $\overline{RAS}$. The following sections describe the detail of all the TRANSFER variations.

Note: *All VRAM operations are defined at the falling edge of $\overline{RAS}$, with the exception of BLOCK WRITE.*

CRT REFRESH USING SERIAL OUTPUT MODE

A design using VRAM for a graphics frame buffer uses the SAM port, in the output mode, to update the CRT with pixel information. When using a VRAM in this manner, the pixel data is transferred a page at a time by READ TRANSFER cycles to the SAM. Then it is sequentially clocked out of the SAM to the DAC driving the CRT, see Figure 1.

There are three kinds of READ TRANSFERs: normal READ TRANSFER (RT), which is not synchronized with the serial clock (SC); a REAL-TIME RT (RTRT), which is synchronized to an SC cycle; and SPLIT RT (SRT), in which data is asynchronously transferred while the SAM is active.

Pixel data is stored as scan lines in the DRAM array. Each row of the array may contain all, part or many video scan lines depending on the organization and size of the frame buffer and display. Different organizations require different methods of moving data to the SAM in order to optimize performance and reduce timing requirements of the transfer cycles.

If the SAM data is loaded only during retrace time of the CRT, a normal READ TRANSFER may be performed. This will be the case when a VRAM row contains one or more complete scan lines, no partial lines. An RT allows the VRAM to time the movement of screen data from the DRAM array to the SAM internally. The pixel clock will be idle during this TRANSFER. In this case the $\overline{TR}/\overline{OE}$ pin

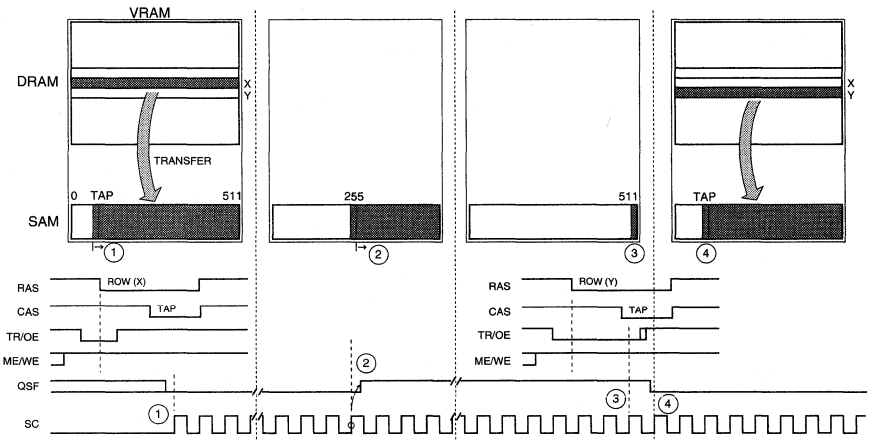


Figure 3
REAL-TIME READ TRANSFER EXAMPLE

may be taken from LOW to HIGH any time during the $\overline{RAS}$-$\overline{CAS}$ cycle. The exact timing of the internal transfer is not important, except that it be complete before the serial clock is restarted. Figures 3 and 4 illustrate this operation as the first TRANSFER cycle at state ①; here, $\overline{TR}/\overline{OE}$ is taken HIGH "early" (before $\overline{CAS}$ falls).

Note: *To implement an all-purpose VRAM design, $\overline{TR}/\overline{OE}$ should be taken HIGH before or at the same time $\overline{RAS}$ and $\overline{CAS}$ go HIGH to terminate the TRANSFER cycle.*

When screen data must be loaded into the SAM during active display time, a REAL-TIME READ TRANSFER may be performed. This allows the data output to proceed in an uninterrupted fashion required when the VRAM rows contain partial scan lines. RTRTs must be synchronized with the serial clock so that the active pixel data is not disrupted when the next portion of the scan line is moved to the SAM. The $\overline{TR}/\overline{OE}$ pin is used to control the exact moment of the transfer of data from the DRAM row to the SAM. By holding $\overline{TR}/\overline{OE}$ LOW until after $\overline{CAS}$ falls (meeting ^{t}RTH and ^{t}CTH), the transfer is "held off" until the LOW-to-HIGH transition. When $\overline{TR}/\overline{OE}$ goes HIGH, the transfer gates open and let the new row move from the sense amps to the SAM, all within a single SC cycle. This is shown from state ③ to state ④ of Figure 3.

Micron's 1 Meg VRAM introduces a transfer feature that greatly reduces the timing demands of REAL-TIME READ TRANSFERs while allowing continuous data streams out of the SAM port. By splitting the SAM and the transfer circuitry into two separately controlled halves, it is possible to transfer screen data to one half of the SAM while the other half is actively supplying screen data. This cycle is called SPLIT READ TRANSFER (SRT), and it eliminates the restriction of having to synchronize the rising $\overline{TR}/\overline{OE}$ edge

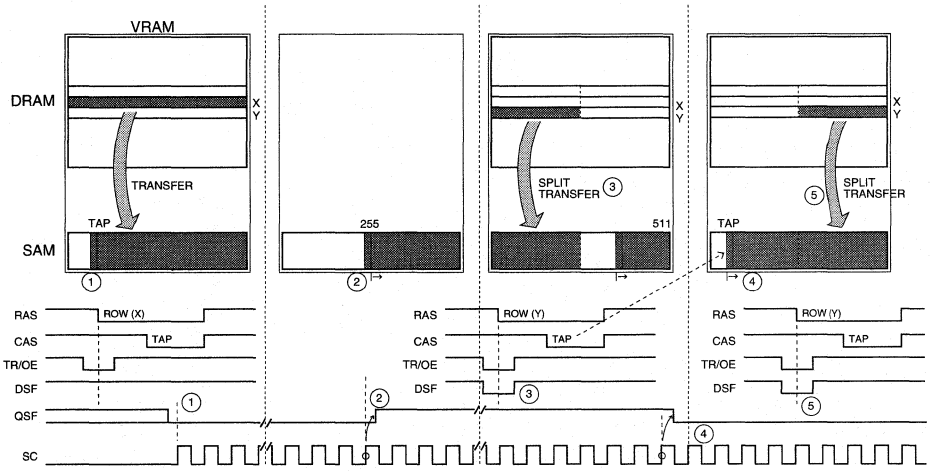


Figure 4
SPLIT READ TRANSFER EXAMPLE

with the serial clock during an RTRT cycle. Figure 4 illustrates a state sequence for split SAM operation. Before split operation can begin, the SAM must be initialized. A normal RT is used to ensure the SAM I/O is in the output state and that a known Tap address is loaded into the SAM address counter/pointer. There is no restriction regarding the initial Tap address location for the Micron VRAM. Once the RT is performed, any number of SRTs may follow. Most 1 Meg VRAMs, including Micron's, will do the SRT automatically to the "idle" half of the SAM. The most significant column-address bit latched at $\overline{CAS}$ LOW is a "don't care."

Note: *Repetitive TRANSFERs may be done regardless of the occurrence of a serial clock cycle. A READ TRANSFER may be immediately followed by a SPLIT READ TRANSFER, provided $\overline{RAS}$ precharge time is met per the specification.*

When using SRT, the system is given a window of time equal to the time needed to read a SAM-half (about 7.6µs for a 256K x 4, 80ns VRAM) to update the idle half and maintain an uninterrupted flow of data from the SAM. This is illustrated from state ② to ④ of Figure 4. The SRT is performed after the address count of the SAM moves from the "old" half (lower half, as shown at state ②) to the "new" half (upper half). State ③ of Figure 4 shows the SRT being executed a finite time after the first clock, but before the last clock, of the upper half. This delay ensures that the SAM counter has entered the new half of the SAM, ensuring that the SRT is invoked to the old half. After address 511, the SAM address counter jumps to the lower half, state ④, and to whatever Tap address was loaded during the SRT performed at state ③. Now the lower half is the active half again, and a SRT to the upper half may be done, ⑤.

The Split SAM Status (QSF) output pin is provided to indicate which half of the SAM is active. By monitoring the QSF pin, it is possible to update data in the SAM without having to externally track the SAM address. At the transition of the SAM boundary, QSF will change state (LOW for lower half, HIGH for upper). When this occurs, the controller performs an SRT to the idle half and the new screen data will be available when the next portion of the scan line is required. Using SRT will simplify the graphics controller design by reducing the control logic and critical timing associated with REAL-TIME READ TRANSFER.

USING THE SAM FOR SERIAL INPUT

An increasing number of VRAM applications require the serial port to be used as an input port. These include video capture, network data buffers and data communications (satellite, telecom, etc.). In these applications, the SAM is used to input data to be moved to the DRAM with a WRITE TRANSFER (WT) operation. All of these applications deal with sequential data, as is the case with computer graphics data. However, these applications put as much emphasis on serial input streams as graphics does on output streams.

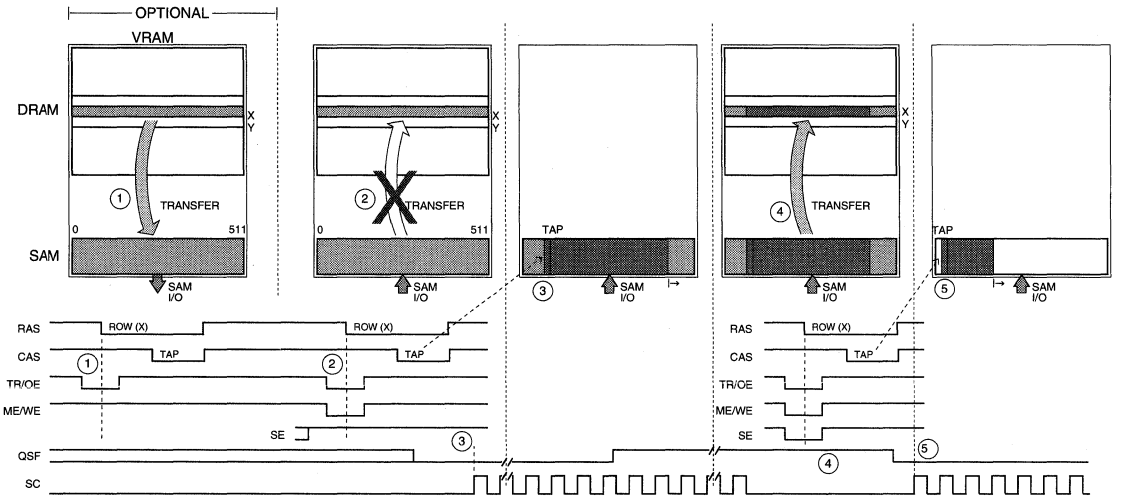


Figure 5
WRITE TRANSFER EXAMPLE

WRITE TRANSFERs are selected in a similar manner to READ TRANSFERs. To perform a WT, the $\overline{ME}/\overline{WE}$ pin must be LOW at the falling edge of $\overline{RAS}$ during the TRANSFER cycle (indicated by $\overline{TR}/\overline{OE}$ = LOW at $\overline{RAS}$), see Figure 5. Before data can be input, the SAM I/O port must be conditioned as an input port. The initial PSEUDO WRITE TRANSFER conditions the SAM I/O port as an input without actually writing data to the DRAM, this is shown in Figure 5 at state ②.

It is possible to preload a row from the DRAM array into the SAM before the PWT (see Figure 5, state ①). This will allow new serial input data to be written over a portion of an existing row in the DRAM array. To perform this operation, an RT is invoked before the PWT, followed by the normal serial input sequence.

After the PSEUDO WRITE TRANSFER has completed, the serial-input data is loaded. This starts at state ③ and progresses until ④. At this time, all the serial data has been loaded and the WRITE TRANSFER is done; the serial clock must be idle. The Tap loaded at the falling edge of $\overline{CAS}$ defines the location where the next string of serial data begins loading, ⑤. An RT and PWT may be inserted between the WT at ④ and the new serial-input at state ⑤.

Note: *The serial clock, SC, must be idle during WRITE TRANSFERs. If it is not, the Tap address will be corrupted.*

WRITE TRANSFERs may also be used to replicate rows within the DRAM. In this operation, a READ TRANSFER is done from the source row to the SAM. Then, without clocking the SAM, a WRITE TRANSFER is done to any row(s) of the DRAM. Once "full," the SAM may be transferred to any row or multiple rows by performing single or multiple WTs. This is useful in accelerating full screen clears. BLOCK WRITE may be used to "color" the source row, further enhancing the performance of this operation.

When selecting a WRITE TRANSFER, the Micron 1 Meg VRAM uses the DSF pin to invoke the ALTERNATE WRITE TRANSFER (AWT) cycle. AWT is a variation of the standard WT, differing in that the $\overline{SE}$ pin, which selects between WT and PWT, is a "don't care" when $\overline{RAS}$ falls. This will change the SAM I/O direction to input, and transfer the contents of the SAM to the addressed row of the DRAM array. The advantage of this cycle is that the SAM I/O control pins (e.g. SC and $\overline{SE}$) are not used to invoke the write transfer, separating the SAM control logic and the WT control logic.

Any of the three WRITE TRANSFER cycles will set the SAM I/O to the input direction so it is not necessary to do a PWT between successive WTs or AWTs. Once the port is set as an input, it will stay in that state until an RT is performed. The PWT cycle is only provided to give designers a way to change the I/O direction without corrupting the DRAM array data when initialing the SAM.

Some 1 Meg VRAM manufacturers use the DSF to select SPLIT WRITE TRANSFER in lieu of AWT. Micron provides SPLIT WRITE TRANSFERS on the MT42C8256/7, 2 Meg VRAM. For a description of the 2 Meg VRAM features, refer to Technical Note TN-42-01.

SAM TIMING CONSIDERATIONS

SAM timing is straightforward. Data is output from, or input to, the SAM port under the control of the serial clock (SC) and serial enable ($\overline{SE}$) pins. The serial clock performs two operations per cycle. First, on the rising edge, it outputs serial data when reading from the SAM, or it latches the serial input data when writing to the SAM. Second, shortly after the rising edge, SC increments the serial address counter/pointer, which holds the Tap address of the SAM. The address counter will increment regardless of the state of $\overline{SE}$, which is purely a data enable/disable pin.

When the SAM is conditioned as an output, the data is accessed by the rising edge of the SC pin. The incremental data will appear on the SDQ pins an access time after the rising edge. The $\overline{SE}$ pin may be used to disable the output, allowing the serial ports of multiple VRAM banks to be tied to a common data bus. QSF is always active on the Micron 1 Meg VRAM and will indicate when the address crosses the SAM-half boundaries (e.g. 255 and 511 for the 42C4256, or 127 and 255 for the 42C8128) during all SAM READ and WRITE operations. Some 1 Meg VRAMs only drive an active QSF during split SAM operation. When the device is in "full" SAM operation, QSF will be High-Z.

When data is written into the SAM, it must be stable for the setup and hold window specified by the data sheets to ensure it is latched accurately by the rising edge of the SC pin. The $\overline{SE}$ pin may be used to disable a WRITE to the SAM for any given clock cycle. When $\overline{SE}$ is disabled (HIGH) the WRITE will be inhibited but the SAM address count will increment. As the SAM is written, the QSF pin may be used as a full or half-full flag similar to those used for first-in-first-out memory devices.

Note: *The Micron 1 Meg VRAM does not use the falling edge of the SC pulse for any internal operations. This allows the clock to be idled in either state without affecting the address pointer location. This is not true of all VRAM manufacturers. To ensure compatibility, the SC should be idled in the LOW state.*

The $\overline{SE}$ pin provides a faster access time than SC and may be used to bank select. When $\overline{SE}$ goes HIGH, the SAM output drivers are designed to turn off as fast as, or two or three nanoseconds faster than, they turn on. This helps to reduce bus contention when switching banks of VRAM with $\overline{SE}$. The actual delta between turn-off and turn-on will vary lot by lot, but any lot variation will be of minor impact. Bus contention will be insignificant, if it exists all, even when using opposite polarities of a single serial enable to select between two banks of VRAM. However, systems that require a guaranteed skew between turn-on and turn-off will require additional logic to ensure that every vendor and device will not cause contention. In this case, an asynchronous state machine may be used to skew the rising and falling edges of $\overline{SE}$ to guarantee the desired separation. A skew of 5ns should yield adequate guardband between turn-off and turn-on time.

HARDWARE PIXEL MASKING

The 1 Meg VRAM supports hardware-level pixel or pixel-bit masking with the MASKED WRITE cycle. This feature can ease system design or improve performance by allowing overlay/underlay planes to be written and operations such as window clipping to be done with single WRITE, or continuous PAGE MODE WRITE cycles.

Standard DRAMs require a READ-MODIFIED-WRITE (RMW) cycle to perform a "write-per-bit" operation. During a RMW, data is read from a location in memory, changed by the processor and written back to the same memory location within the same $\overline{CAS}$ cycle.

MASKED WRITE allows individual DQ bits to be selectively overwritten during a WRITE to the DRAM port. This is done by preloading a write-mask bit for each corresponding DQ bit plane. A mask data register (4 or 8 bits for x4 or x8, respectively) inside the VRAM stores the DQ mask data. A logic 1 in the mask register will enable that bit's corresponding DQ bit (plane) when the data is written to the DRAM after $\overline{CAS}$ goes LOW. A logic 0 will mask data for that DQ plane when the DRAM WRITE is performed. See Figure 2. During non-PAGE MODE operation, MASKED WRITE is approximately 25 to 30 percent faster than an RMW; when operating in FAST-PAGE-MODE, it is at least 50 percent faster.

Two types of MASKED WRITE cycles are supported by the 1 Meg VRAM; nonpersistent and persistent. When nonpersistent MASKED WRITE is selected, mask data must be presented on the DQ pins for every new $\overline{RAS}$ cycle. When $\overline{RAS}$ falls, the data present on the DQ pins is loaded into the mask register. When the WRITE occurs at the falling edge of $\overline{CAS}$ or $\overline{WE}$, the mask is applied to the incoming write data. After $\overline{RAS}$ goes HIGH, terminating the WRITE cycle, the mask register data is lost and must be reloaded for any subsequent $\overline{RAS}$ cycles.

Some graphics processors and controllers are not able to provide mask data at the falling edge of $\overline{RAS}$. To allow these controllers to perform hardware pixel plane protect directly in the VRAM, a persistent MASKED WRITE (read/write old mask; RWOM) cycle is provided. When using this cycle, the mask data must be loaded before the WRITE cycle is done. However, once loaded, the mask register will not be

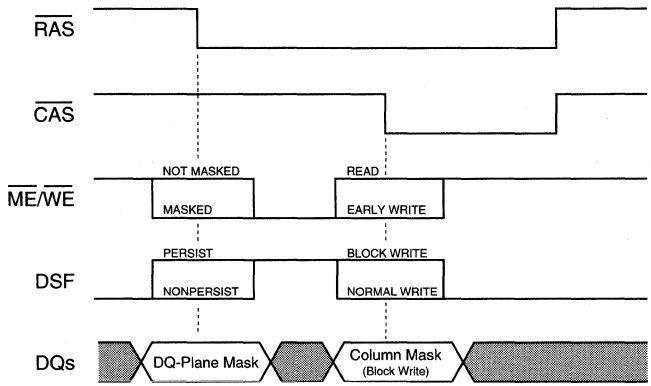


Figure 6
SPECIAL FUNCTION MODE SELECTION

erased at the end of the WRITE cycle. A LOAD MASK REGISTER cycle is performed to permanently load the mask register. During this cycle, data present on the DQ pins will be written to the mask register instead of the DRAM. This mask data will stay in the register until overwritten or until power is lost. The register is fully static and requires no refresh. When the RWOM cycle is performed, the mask is supplied by the mask register. The DQ inputs are "don't care" when $\overline{RAS}$ falls.

The control levels for the special-function DRAM access modes are shown, in a simplified form, in Figure 6. MASKED WRITE and BLOCK WRITE select options are shown. A write mask may be applied to a BLOCK WRITE in the same manner as it is to a normal WRITE. See the MT42C4256 and MT42C8128 data sheets for detailed timing of these cycles.

There is some functional variation between VRAM suppliers regarding these cycles. Some 1 Meg VRAM manufacturers support FLASH WRITE cycles in lieu of persistent MASKED WRITE. The Micron MT42C8256/7, 2 Meg VRAM includes the FLASH WRITE function, see the data sheet and TN-42-01 for more detail.

ACCELERATING WINDOW AND POLYGON FILLS WITH BLOCK WRITE

As the operating systems of workstations and PCs move toward graphical, windowed environments, the ability to quickly "fill" a window with color or text will become more important to display performance. In addition to windowed environments, demands for real-time imaging require improvement of the solid-color fill rate of drawn polygons. To satisfy these requirements, BLOCK WRITE has been added to the VRAM. This feature provides a four-times improvement of pixel drawing speed to the DRAM port of the VRAM. However, there is a penalty for this speed improvement; the pixel data is restricted to a single, preloaded "color" for each cycle. BLOCK WRITE can be used to quickly fill simple background patterns on the screen when the VRAM frame buffer contains more than one pixel per pixel-word.

The color data used during a BW is stored in the color register of the VRAM by the LOAD COLOR REGISTER cycle. This cycle must precede any BLOCK WRITE cycle

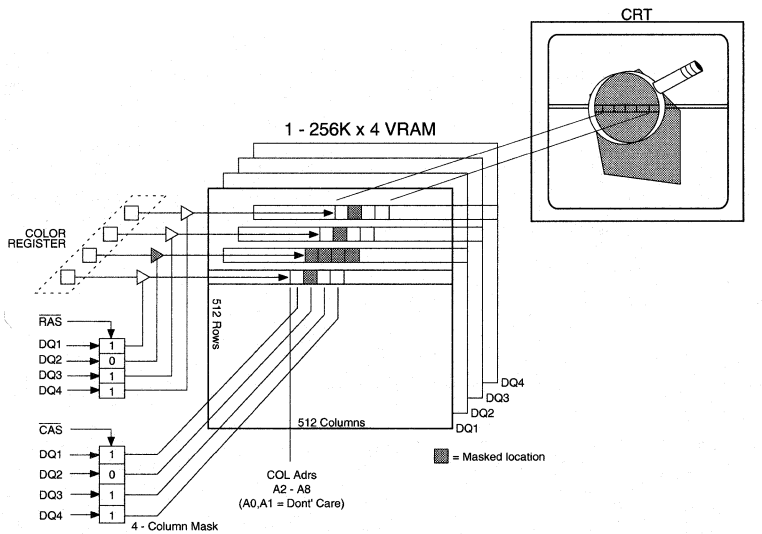


Figure 7
Block Write

because the write data is supplied by the register instead of the DQ pins.

BLOCK WRITE alters the column addressing of the DRAM array. When a BW is performed, the least significant two column-address bits (A0, A1) are ignored. This addressing selects the four-column "block" that will be written to the value stored in the color register. Each bit of the color register corresponds to its associated bit plane and is simultaneously written to all four column locations during the BW, see Figure 7.

BLOCK WRITE is selected by the DSF pin at the falling edge of $\overline{CAS}$ and is the only VRAM special function that is not selected at the falling edge of $\overline{RAS}$. It is important to note that all manufacturers of the 1 Meg VRAM do not perform BW the same way. Some manufacturers (including Micron) perform the BW only at the falling edge of $\overline{CAS}$ and allow $\overline{WE}$ to be a "don't care." The BW control and column mask (DQ pins) are latched only at the falling edge of $\overline{CAS}$. Some manufacturers allow BW to be either $\overline{CAS}$ or $\overline{WE}$ controlled (late BLOCK WRITE). For a robust design, it is recommended that all BWs be done as "early" BW ($\overline{WE}$ LOW prior to $\overline{CAS}$ LOW). A design done in this manner will accept both BW methods.

There is no need to input data at $\overline{CAS}$ time because the pixel data is already stored in the color register. Therefore, a column mask may be applied on the DQ pins when $\overline{CAS}$ falls. Data present on these pins act as separate write enables to each column location within the block, see Figure 7. The least significant DQ corresponds to the least significant column location, the second least significant to the second least column, and so on. This allows column by column addressibility of the window or polygon to be filled during the BW. For example, if the left side of the window starts at the second column location of the "block", the first column may be masked off and columns 2, 3 and 4 of the block will be written with the new color.

Note: *When using the Micron VRAM in "minimum" function applications (no MASKED WRITE, BLOCK WRITE or SPLIT READ TRANSFER), ensure that the DSF pin is grounded or held a logic 0 level.*

CONCLUSION

VRAM function sets and system implementations are very diverse. Your function set and system design may differ from what was presented here. These were typical implementation examples and are not exhaustive. The intent is to show the bandwidth advantages of the VRAM over DRAM and how to use them in a memory design. The VRAM bandwidth advantage exists when dealing with sequential data streams in particular, and longer streams in general. The special features, such as MASKED WRITE and BLOCK WRITE further advance the performance of VRAM in graphics systems. Features such as SPLIT READ TRANSFER simplify high-bandwidth continuous sequential data streams such as those seen in communications and high-bandwidth networks.

If your design question was not answered here, feel free to call Micron Application Engineering at 208-368-3905.

TECHNICAL NOTE

REGULAR, REAL-TIME AND SPLIT READ TRANSFERS

INTRODUCTION

As described in TN-42-02 "Designing with the MT42C4256/8128 VRAM," READ TRANSFER functions on VRAMs are used to perform internal transfers of data from the DRAM array to the Serial-Access-Memory (SAM) portion of the VRAM. In graphics systems, the DRAM array is used to store the data representing pixels to be displayed on the screen. This pixel data is manipulated via the DRAM I/O port, and system performance is optimized by maximizing the bandwidth of the DRAM port that is available for this manipulation. Toward that end, VRAMs include a SAM to handle the task of providing the stream of pixels to the display circuitry. The SAM acts as a buffer between the display memory (DRAM array) and the monitor (see Figure 1).

Display data is transferred, a portion at a time, to the SAM buffer. From there it is clocked out to the display circuitry which drives the monitor. To maintain a continuous flow of data to the monitor, the subsequent portion of data must be transferred to the SAM before the buffer becomes "empty."

This note describes the various forms of read-transfer functions and how each is used to feed data to the SAM buffer in different situations.

READ TRANSFERS

The vast majority of VRAMs available on the market, including all Micron VRAMs, provide a SAM buffer that is equal in size to one row of the DRAM array for that particular VRAM. For example, 2 Meg VRAMs include a DRAM array consisting of 512 rows; each row contains 512 columns of 8-bit-wide locations. Accordingly, the SAM consists of 512 8-bit locations. In "regular" READ TRANSFERs (the most fundamental form) one complete row of data from the DRAM array is copied to the SAM, thereby overwriting the entire contents of the SAM. READ TRANSFERs are used when each row in the DRAM array (and hence, the SAM) contains the pixel data for an integral number of scan lines on the monitor. In this case, the buffer will become empty at the end of a scan line and can be reloaded during the horizontal blanking time of the monitor. The READ TRANSFER cycle can easily be completed within the blanking time; and therefore the specific timing is not critical.

REAL-TIME READ TRANSFERS

In configurations where part of a scan line is stored in one row of the DRAM array and the remainder is stored in another row, the SAM buffer will become "empty" in the middle of a scan line, and a midline transfer will be required to reload the SAM. Since a read transfer overwrites the entire SAM, this transfer cannot take place until after the data from the last location has been clocked out (read). However, the transfer must also be completed prior to the next serial clock edge. (The serial clock cannot be delayed or disabled while in the middle of a scan-line, or artifacts will appear on the screen.) In other words, the actual transfer of data must take place within one serial clock cycle (the cycle between the positive edge for the last piece of "old" data and the positive edge for the first piece of "new" data). Since a transfer cycle typically spans several serial clock cycles, it is necessary to know where within the transfer cycle the data is actually transferred, and to make sure that that portion of the transfer cycle falls within the window defined between the two specific clock edges. The REAL-TIME READ TRANSFER is specified for this purpose.

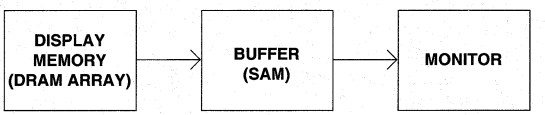


Figure 1
SAM BUFFER BETWEEN DISPLAY MEMORY AND MONITOR

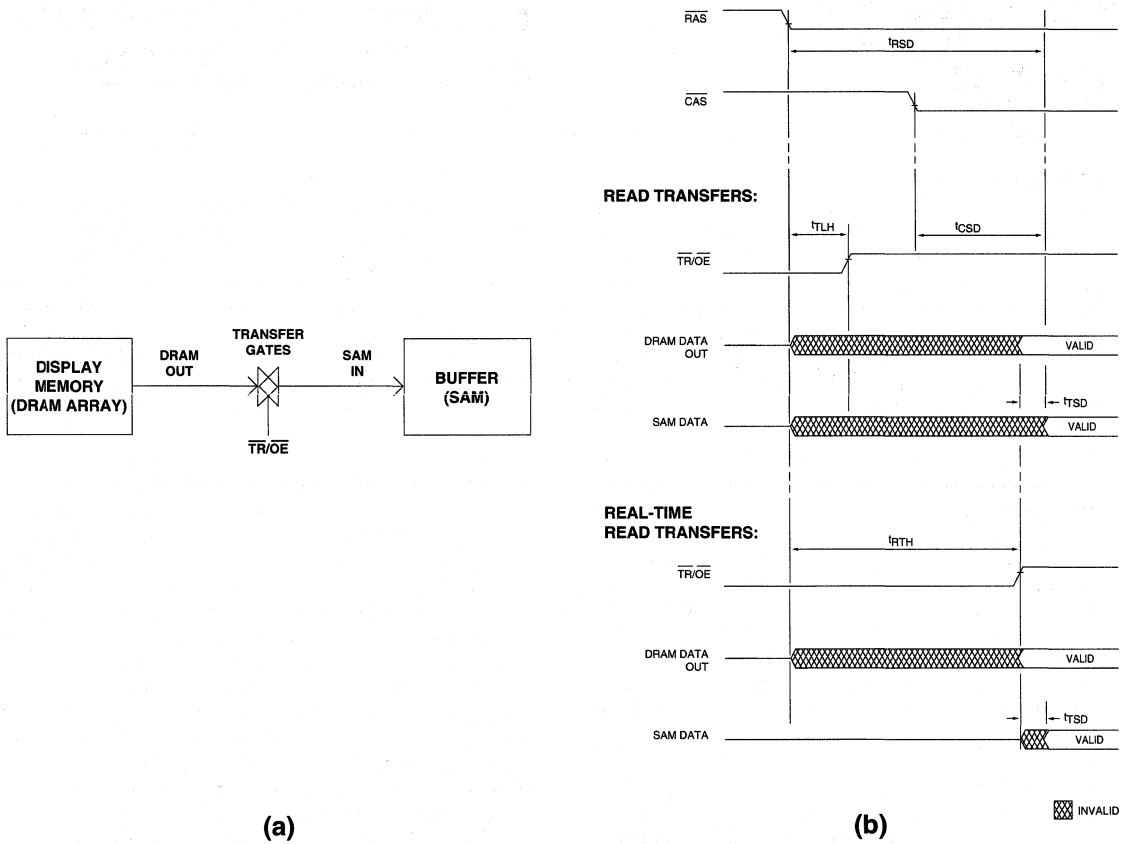


Figure 2
(a) CONTROLLING TRANSFERS BETWEEN DRAM AND SAM
(b) RELATED TIMING

Returning for a moment to "regular" READ TRANSFERs, $\overline{TR}/\overline{OE}$ goes HIGH "early" in the transfer cycle (sometime after ^{t}TLH is met, but before ^{t}RTH is met). When $\overline{TR}/\overline{OE}$ goes HIGH early in the cycle, the transfer gates between the DRAM and the SAM open before valid data has propagated completely through the DRAM circuitry (see Figure 2). So, new data reaches the SAM following the propagation delays through the DRAM circuitry and the transfer gates (^{t}RSD, ^{t}CSD and ^{t}TSD). The exact time at which new data arrives at the SAM is not specified (when $\overline{TR}/\overline{OE}$ goes HIGH before ^{t}RTH is met, the resulting transfer is sometimes referred to as "self-timed"). However, the maximum time is specified and is therefore the minimum time that should be met before supplying a positive edge on the serial clock input.

In contrast, in a REAL-TIME READ TRANSFER cycle $\overline{TR}/\overline{OE}$ goes HIGH "late" (after ^{t}RTH has been met). This way, the DRAM data is guaranteed to be at the transfer gates when they are opened and the only propagation delay is through the transfer gates (^{t}TSD), which thereby provide a shorter period of invalid SAM data. However, it is still a formidable task to fit this window within the desired clock cycle, and for this reason, SPLIT READ TRANSFERs were created.

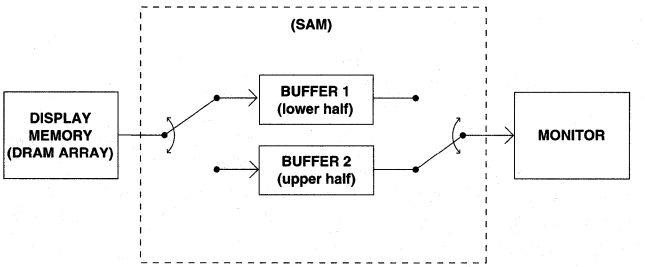


Figure 3
SPLIT BUFFER ARCHITECTURE FOR SPLIT READ TRANSFERS

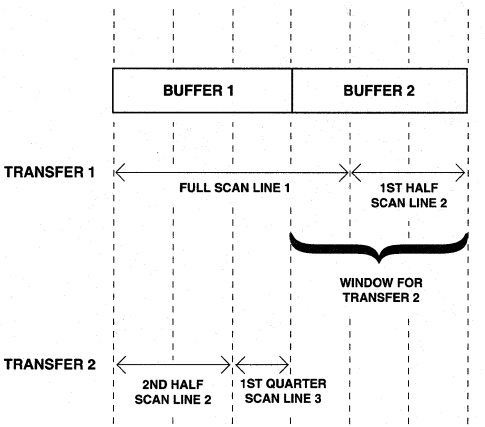


Figure 4
RELAXED TIMING CONSTRAINTS FOR SPLIT READ TRANSFERS

SPLIT READ TRANSFERS

When using SPLIT READ TRANSFERs, the SAM is effectively split into two buffers, each being half the length of the complete SAM. This provides double-buffered transfers between the DRAM and the SAM, with each buffer alternately functioning as the input buffer and the output buffer (data can be transferred into one buffer without corrupting the data being read out of the other buffer; see Figure 3).

This architecture calls for twice the number of transfer cycles, but provides less restrictive timing relative to REAL-TIME READ TRANSFERs. As an example of a case where midline transfers are required, consider a system configuration where one row in the DRAM array contains 1.5 scan lines of the display. A VRAM is always initialized for SPLIT READ TRANSFERs by executing a regular READ TRANSFER cycle first (see Transfer 1 in Figure 4). Here an entire row of the DRAM is transferred to the entire SAM. If the system continued using full READ TRANSFERS, a REAL-TIME READ TRANSFER would be required halfway through the second scan line of the display. However, with SPLIT READ TRANSFERS, the data for the remainder of the second scan line can be loaded in advance in buffer 1, thereby eliminating the seam that would otherwise exist. Specifically, one half of the next row in DRAM can be transferred to the SAM (Transfer 2 in Figure 4) any time after the SAM address counter passes from buffer 1 to buffer 2. This window is clearly much larger than the window for REAL-TIME READ TRANSFERs.

Then, after the SAM address counter wraps from the end of buffer 2 to the beginning of buffer 1, another half-row of data from the DRAM can be transferred to buffer 2. This process is continued for seamless operation of the SAM.

SUMMARY

Several types of read transfer cycles are available to transfer data from the DRAM array to the SAM portion of VRAMs. Each is suited to certain situations.

Regular READ TRANSFERs are used when each row in the DRAM array contains data for an integral number of display scan lines (or to initialize a VRAM prior to using SPLIT READ TRANSFERs). REAL-TIME READ TRANSFERs are used when midline transfers are needed (i.e. when a DRAM row contains a nonintegral number of scan lines). SPLIT READ TRANSFERs are also used when midline transfers are needed. The use of SPLIT READ TRANSFERs increases the number of transfer cycles executed, but avoids the tight timing requirements of REAL-TIME READ TRANSFERs.

TECHNICAL NOTE

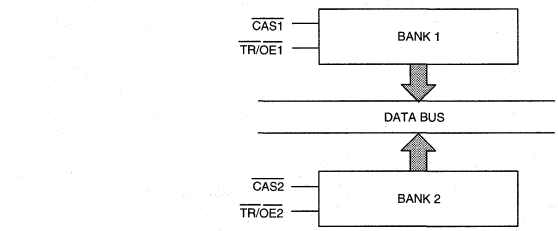
BANK INTERLEAVING WITH EXTENDED DATA-OUT VRAMs

INTRODUCTION

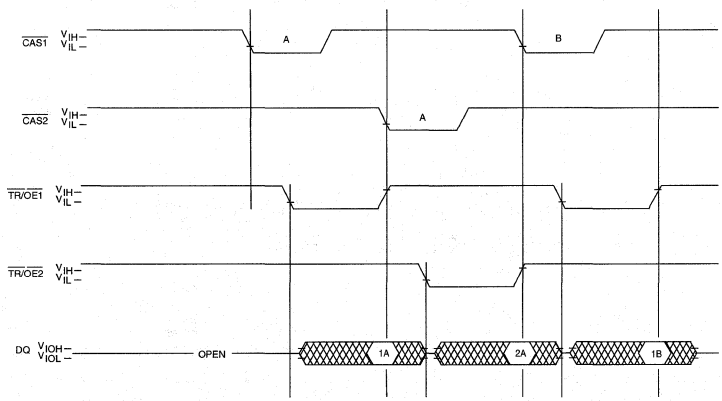
The extended data-out (EDO) functionality introduced on 2 Meg VRAMs provides faster PAGE-MODE cycle times by allowing data to remain or appear on the outputs beyond the deactivation of the related $\overline{CAS}$ signal (please refer to Technical Note TN-04-21, Reduce DRAM Cycle Times with Extended Data-Out). The tradeoff for this improved performance is that $\overline{CAS}$ alone can no longer be used to disable the data outputs. In situations where this behavior is required, such as bank-interleaved systems, the $\overline{OE}$ signal must be used to disable the data outputs.

BANK INTERLEAVED SYSTEMS

In bank-interleaved systems, the data outputs of non-selected banks must be disabled while data is being read from the selected bank. When using non-EDO parts, this can be achieved by deactivating the $\overline{CAS}$ signals of the non-selected banks. However EDO parts require that $\overline{OE}$ signals be used. For example, an interleaved design using two banks of MT42C8256 2 Meg VRAMs requires an $\overline{OE}$ signal for each bank. This configuration and related general timing are shown in Figure 1.



(a)

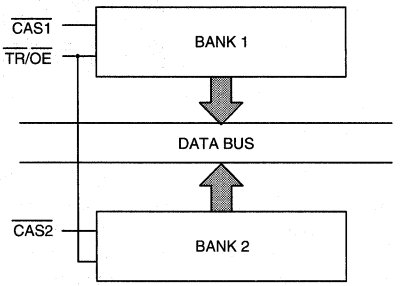


(b)

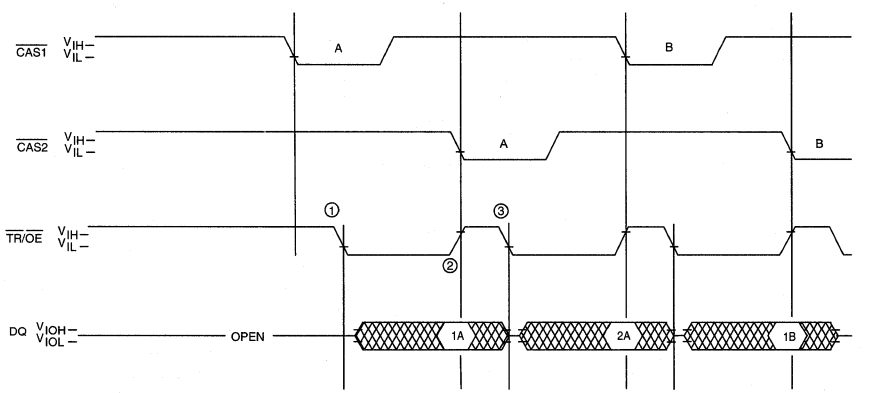
UNDEFINED

Figure 1
(a) TWO BANKS, WITH SEPARATE $\overline{OE}$s (b) RELATED GENERAL READ TIMING

NEW APPLICATION/TECHNICAL NOTE



(a)



(b)

Figure 2
(a) TWO BANKS, WITH A COMMON $\overline{OE}$
(b) RELATED GENERAL READ TIMING

For some designs, providing an $\overline{OE}$ signal for each bank may be considered undesired overhead. For this reason, the EDO operation of the Micron MT42C256K16A1 4 Meg VRAM was modified to allow bank interleaving with a single $\overline{OE}$ line common to all banks. System timing for common $\overline{OE}$ operation is shown in Figure 2. Note that edge ③ of $\overline{OE}$ causes the devices in bank 2 to drive the bus, but the outputs of the devices in bank 1 remain disabled. This reflects the modified EDO functionality provided by the MT42C256K16A1; this operation is shown in more detail in Figure 3. Initial EDO devices cannot be used as shown in Figure 2 because both banks would drive data as a result of $\overline{OE}$ edge ③. The data from bank 1 that was disabled at edge ② would simply be re-enabled at edge ③.

The "latched output-disable" functionality of modified EDO parts, such as the MT42C256K16A1, takes into account that $\overline{CAS1}$ is HIGH when $\overline{OE}$ goes HIGH at edge ②. When this occurs, the data outputs of bank 1 are disabled, and will remain disabled until $\overline{CAS1}$ goes LOW again.

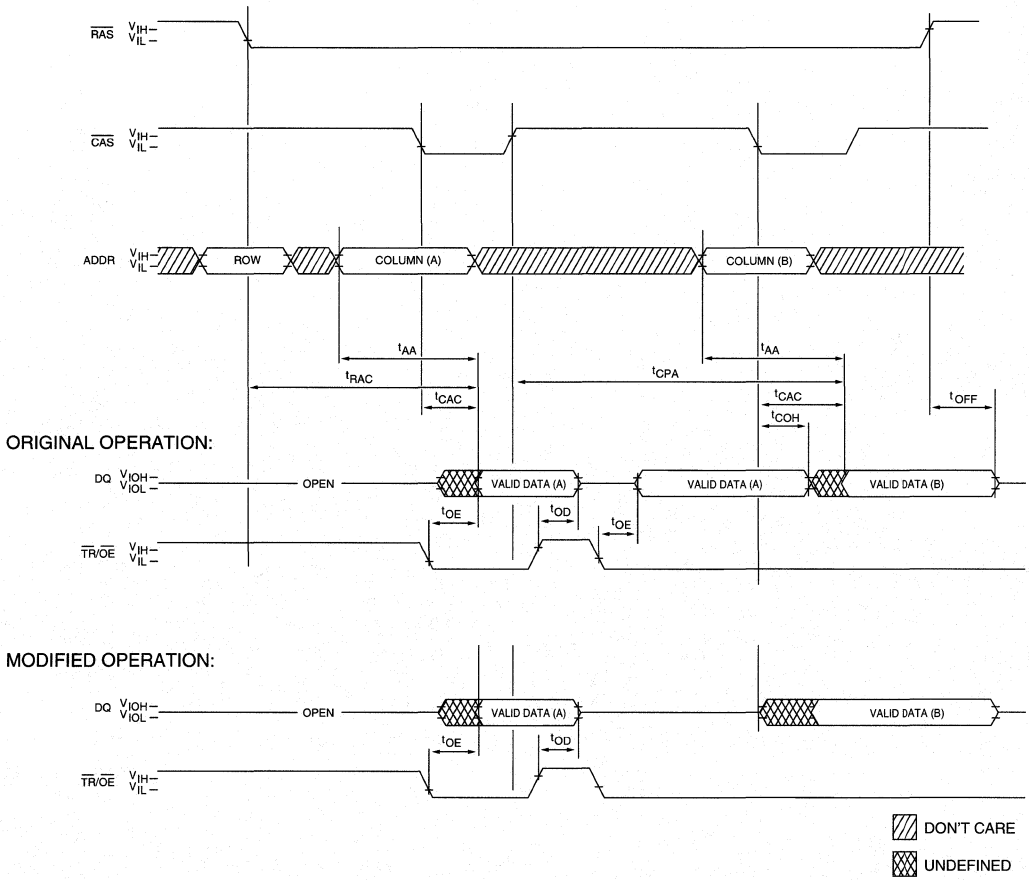


Figure 3
FAST-PAGE-MODE EDO READ CYCLE SHOWING ORIGINAL AND MODIFIED OPERATION

SUMMARY

When interleaving banks of EDO VRAMs, it is necessary to use $\overline{OE}$ signals to select the appropriate bank to drive the bus, and to deselect the other banks. The original parts that include EDO functionality require a separate $\overline{OE}$ signal for each bank. The MT42C256K16A1 4 Meg VRAM provides modified EDO operation which allows for the use of a common $\overline{OE}$ signal for all banks. The MT42C256K16A1 functions identically to previous EDO devices in all other cases.

NEW APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

FOUR-COLUMN VS EIGHT-COLUMN BLOCK WRITE

INTRODUCTION

The BLOCK WRITE feature on VRAMs allows for a single value to be written to several locations in the DRAM array in one WRITE cycle. Prior to the introduction of 4 Meg VRAMs, the BLOCK WRITE feature had been defined to apply to four column locations. This definition has been expanded to eight column locations for 4 Meg VRAMs; this expansion doubles the achievable bandwidth of BLOCK WRITEs.

This note discusses four- and eight-column BLOCK WRITEs in the context of graphics systems, where the data stored in memory represents pixels to be displayed on a screen.

BLOCK WRITE OPERATION

A BLOCK WRITE cycle affects a block of memory cells in the DRAM array. This is shown in Figures 1 and 2 for a four-bit-wide VRAM (four memory planes or DQ pins) with four-column BLOCK WRITE capability. The data to be written to the cells is stored, in advance, in an internal data register known as the COLOR REGISTER. The row-address n is provided on the address inputs at $\overline{RAS}$ time, and the column-address m, at $\overline{CAS}$ time. The two least significant column-address bits are ignored, and the four columns corresponding to the four possible combinations of those bits are all selected.

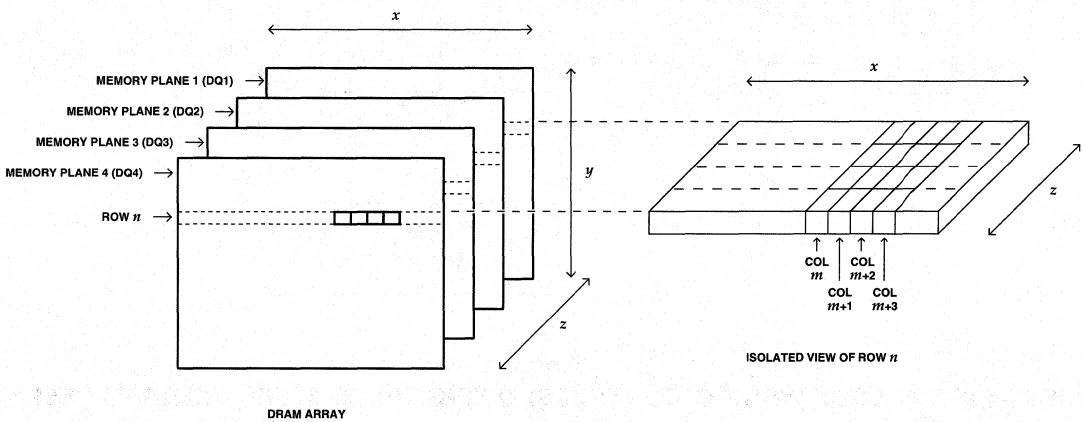


Figure 1
MEMORY CELLS AFFECTED BY BLOCK WRITE IN 4-BIT-WIDE, FOUR-COLUMN BLOCK WRITE VRAMs

NEW APPLICATION/TECHNICAL NOTE

The two-dimensional (x-z) representation of the 16 affected cells shown in Figure 2 illustrates the masking capabilities within a BLOCK WRITE cycle. The write-per-bit (WPB) mask is used to prevent the BLOCK WRITE cycle from affecting the cells associated with a particular DQ line (or lines). The WPB mask is either stored in advance in an internal mask register, or it is presented at $\overline{RAS}$ time on the DQ lines. The column mask, which is presented on the DQ lines at $\overline{CAS}$ time, is used to mask the cells in a particular column (or columns).

FOUR-COLUMN BLOCK WRITES

FOUR-BIT-WIDE VRAMs

As mentioned, when a four column BLOCK WRITE is performed in VRAMs with four-bit-wide data paths (such as the MT42C4256 1 Meg VRAM), the four-bit column mask is presented on the DQ pins at $\overline{CAS}$ time. If a 32-bit-wide array is constructed with four-bit-wide VRAMs, the total number of memory cells affected by a BLOCK WRITE cycle

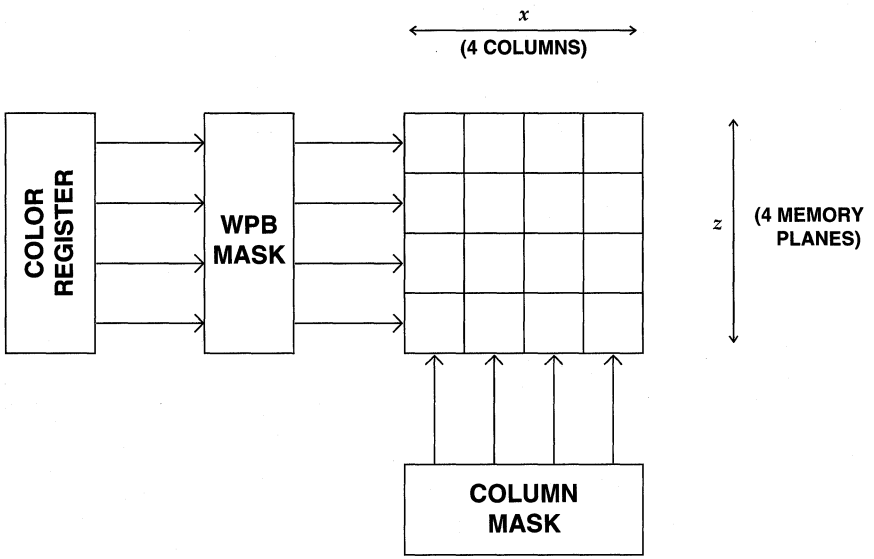


Figure 2
SIMPLIFIED BLOCK WRITE OPERATION SHOWING THE 16 AFFECTED DRAM CELLS

is 128 (32 memory planes multiplied by 4 columns). This is shown in Figure 3.

Assuming four-bit pixels in a packed-pixel implementation, each column in Figure 3 contains 8 pixels. These 4-bit pixels are shown numbered (1-32) in Figure 4(a). In this 32-bit-wide implementation, a column mask is presented on each nibble of the bus (see Figure 4[b]). This allows for single pixel granularity during area fills or color expansion operations when using four-bit pixels.

Consider an area fill operation, where a rectangle on the screen is to be filled with a single color. Assume that the left boundary of the rectangle falls on pixel 2 (i.e. pixel 1 should remain unaltered, pixels 2 through 32 should be "colored"). This would be accomplished by performing a BLOCK

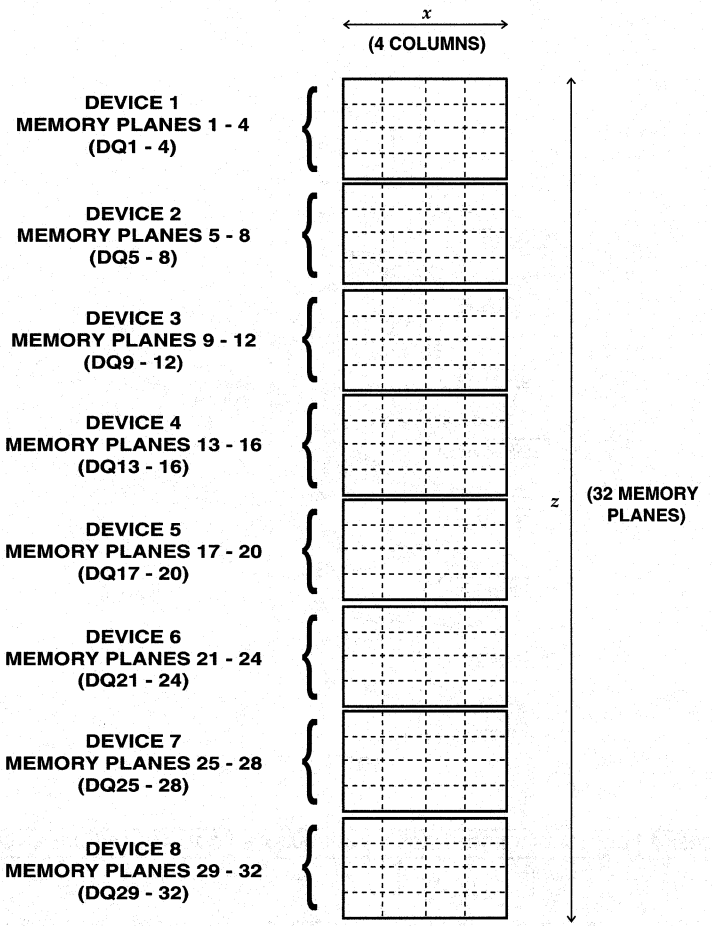


Figure 3
DRAM CELLS AFFECTED BY A BLOCK WRITE CYCLE IN A 32-BIT-WIDE ARRAY CONSISTING OF EIGHT MT42C4256 VRAMS

WRITE with column mask 1 = 0111 and column masks 2 through 8 all = 1111 (i.e at $\overline{CAS}$ time, DQ1 = 0, DQ2-32 = 1).

Assume that the above BLOCK WRITE cycle was repeated for the number of rows in the rectangle, and then BLOCK WRITEs were performed on additional columns as needed until the rectangle was completely "colored." Further, assume that this rectangle was to act as a background for text or other objects that consist of a foreground color. The text or other objects are represented by a monochrome bit map, and require color expansion. Returning to the 32 pixels represented in Figure 4, the corresponding section of the monochrome bit map contains a 1 for each of the 32 pixels that is to appear in the foreground color and a 0 for each of the pixels that is to remain as the background color. To "color" the foreground pixels, a BLOCK WRITE is performed with the foreground color value present in the color register, and with the monochrome bit-map presented as the column mask.

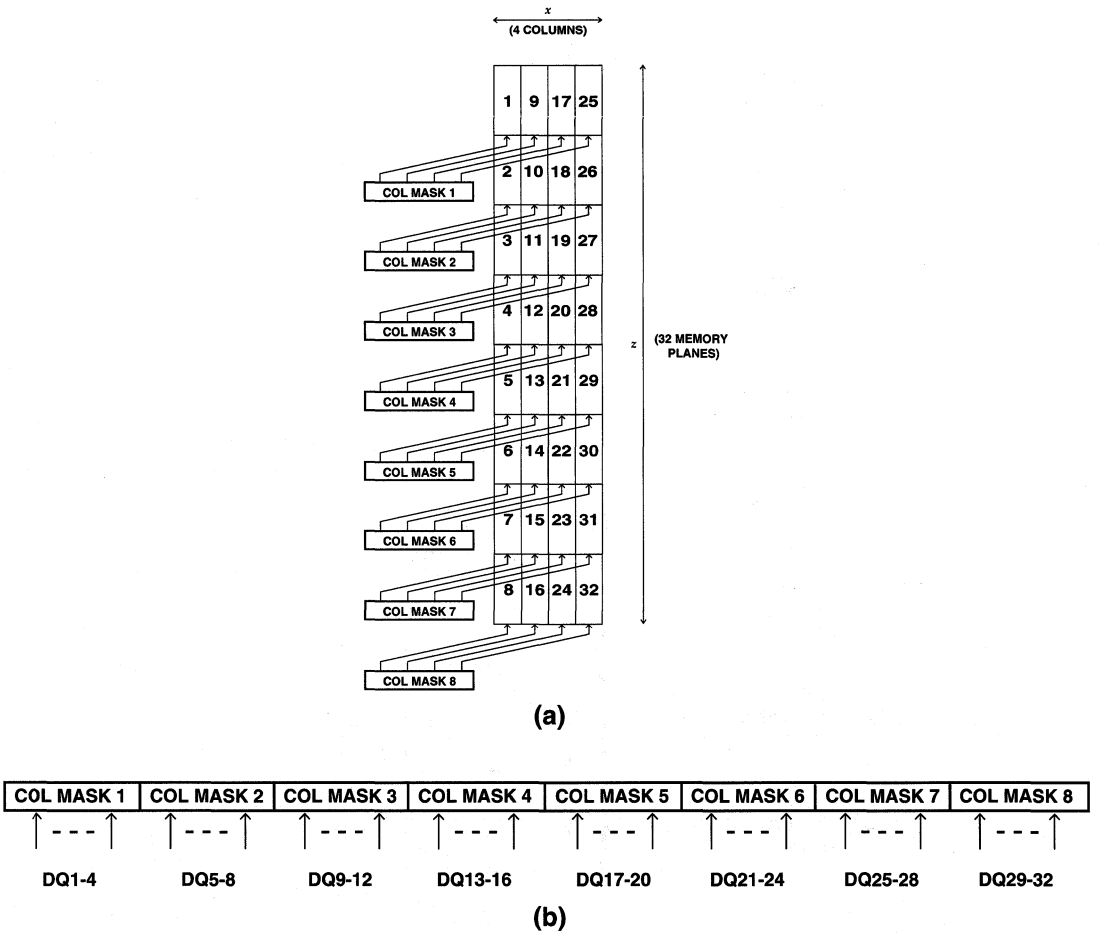


FIGURE 4
(a) 4-BIT PIXELS (1-32) STORED IN THE DRAM CELLS SHOWN IN FIGURE 3 AND THE RELATED COLUMN MASKS (b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

EIGHT-BIT-WIDE VRAMs

When four-column BLOCK WRITEs are performed in 8-bit-wide VRAMs, such as the MT42C8128 1 Meg or the MT42C8254/5/6/7 2 Meg VRAMs, the 4-bit column mask is presented on the lower nibble of the DQ pins (DQ1-DQ4). This 4-bit mask is then internally provided to both nibbles within the VRAM. Again, looking at a 32-bit array, a column mask is presented on every other nibble on the bus (see Figure 5). The result is that single-pixel resolution can be achieved on 8-, 16-, 24- or 32-bit pixels, but not for four-bit pixels.

In order to achieve the same single-pixel granularity as described previously for four-bit-wide VRAMs, it is necessary to make two passes with the BLOCK WRITE cycles, while using the WPB mask to mask alternating nibbles.

EIGHT-COLUMN BLOCK WRITES

Eight-column BLOCK WRITE is introduced on 4 Meg VRAMs such as the MT42C256K16A1, which is configured as 256K x 16. In conjunction with the expansion to eight columns, these devices also allow for two 8-bit column

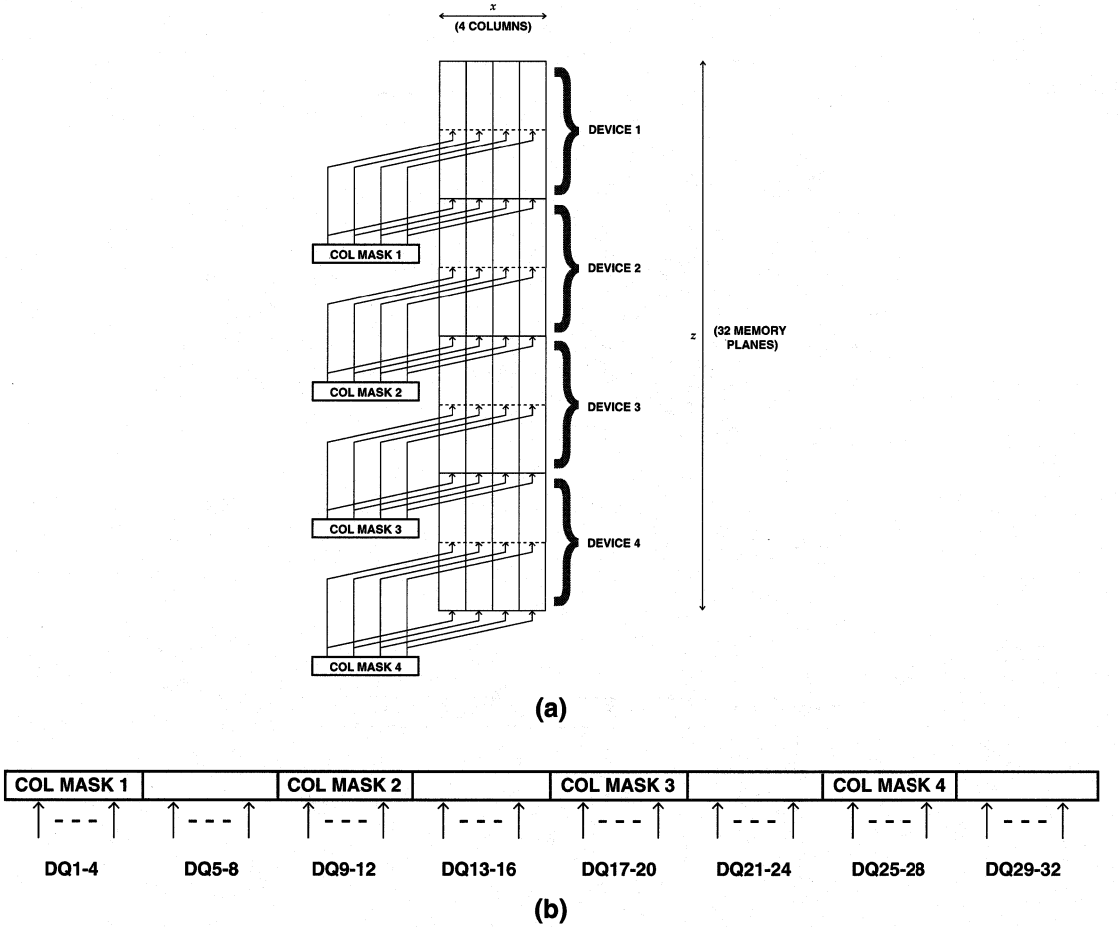


Figure 5
(a) A 32-BIT-WIDE ARRAY BASED ON 8-BIT-WIDE, 4-COLUMN BLOCK WRITE VRAMs
(b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

masks to be presented on the DQs. The 8-bit column mask for the lower byte is presented on DQ1-DQ8 and the column mask for the upper byte, on DQ9-DQ16. Again, considering a 32-bit array (see Figure 6), a column mask is provided on each byte of the bus. This preserves the single-pixel granularity that was available on 8-bit-wide devices when using 8- , 16- , 24- and 32-bit pixels. In addition, the 2x improvement in bandwidth due to eight columns being included in the BLOCK WRITE cycle negates the penalty of using two passes with four-bit pixels. Therefore, eight-column BLOCK WRITE with two eight-bit column masks is the optimal implementation overall.

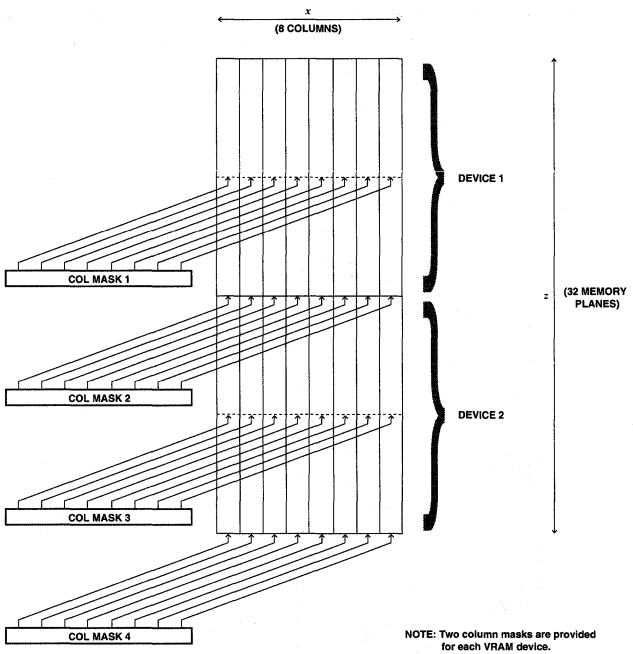


Figure 6
(a) A 32-BIT-WIDE ARRAY BASED ON 16-BIT-WIDE, 8-COLUMN BLOCK WRITE VRAMS
(b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

Table 1
COMPARISON OF BLOCK WRITE IMPLEMENTATIONS

NUMBER OF COLUMNS	VRAM WIDTH	MINIMUM PIXEL SIZE FOR SINGLE PIXEL GRANULARITY	NORMALIZED PERFORMANCE	
			4-BIT PIXELS	8-, 16-, 24-, AND 32-BIT PIXELS
4	4 BITS	4 BITS	1.0	1.0
	8 BITS	8 BITS	0.5	1.0
8	16 BITS	8 BITS	1.0	2.0

SUMMARY

BLOCK WRITE cycles allow for several locations of the DRAM array within VRAMs to be modified simultaneously. In graphics systems, this operation can improve system performance when executing area fills and/or color expansion functions.

There are several implementations of BLOCK WRITE, depending on the density and width of the VRAM. Relative to the others, the eight-column BLOCK WRITE, two-mask implementation provided by the MT42C256K16A1, 4 Meg VRAM delivers equivalent performance for four-bit pixels and twice the performance for 8-, 16-, 24- and 32-bit pixels, making it the optimal overall BLOCK WRITE implementation.

TECHNICAL NOTE

MT43C4257/MT43C4258 COMPARISON

INTRODUCTION

Micron offers its Triple-Port DRAM (TPDRAM) in two versions. The MT43C4257 supports the JEDEC split SAM status function (QSF) pin as defined for VRAMs. The MT43C4258 supports a variation of the QSF function called the split SAM special function (SSF) input function. Other than this difference, the function and performance of the two devices are identical.

MT43C4257 — QSF OUTPUT

The QSF output pin of the MT43C4257 is identical in function to the QSF pin of the MT42C4255, 256K x 4 VRAM. The QSF output pin indicates which half of the SAM is being accessed. When data is accessed from the lower half, the QSF is LOW; when data is accessed from the upper half, QSF is HIGH (see Figure 1). When using the MT43C4257 or any standard VRAM in the split SAM mode, the transition between SAM halves occurs only when the SAM-half boundary is reached by the address pointer. This is address count 255 for the lower half and 511 for the upper half. When this boundary is reached, the new Tap address for the next SAM-half is loaded ("X" for the lower, "Y" for the upper). The following SC will access data from the new half.

MT43C4258 — SSF INPUT

The MT43C4258 introduces functionality to the TPDRAM that is not available on standard VRAMs. The "QSF" pin as an input (SSF) offers a higher degree of design flexibility to the system engineer. The SSF applies only to split transfer cycles. It allows access to be switched from one half of the SAM to the other at will. If SSF is HIGH at the rising edge of the serial clock, the split SAM access will be switched to the other half of the SAM (see Figure 2).

By taking SSF HIGH for the rising edge of a serial clock (location "A" for the lower half, "B" for the upper), the access from the current half may be terminated. Data from this clock will appear on the outputs when in SERIAL OUTPUT mode or will be written if in SERIAL INPUT mode.

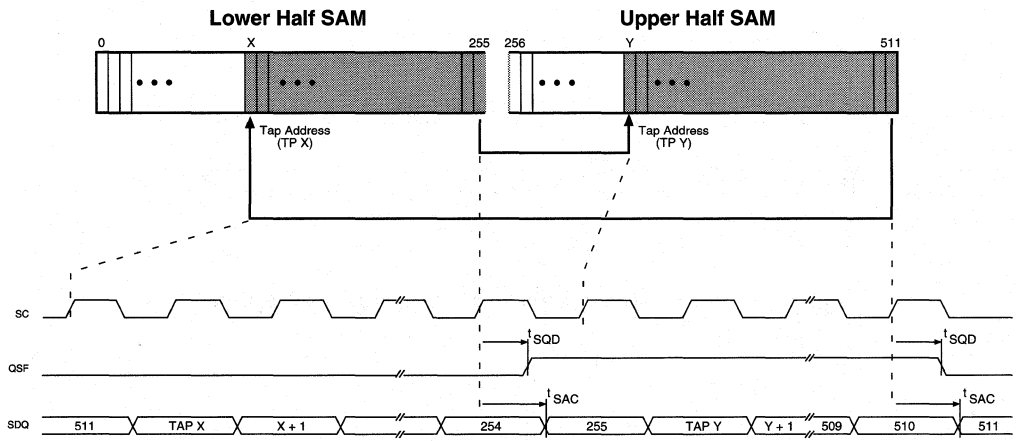


Figure 1
QSF OPERATION FOR THE MT43C4257 (SERIAL OUTPUT)

APPLICATION/TECHNICAL NOTE

The next serial clock will access data at the new Tap address ("X" for the lower, "Y" for the upper) of the next half. The SSF input acts as a "stop address" input so the designer can "force" the access from one half to the next when desired. When operating in the split SAM mode, this option allows different sized "blocks" of data to be input or output from the SAM half regardless of the Tap address and stop point. This feature is useful when performing pans, zooms and scrolling in video-graphics systems and for handling distinct packet sizes in networking or controller applications.

SUMMARY

The only difference between the MT43C4257 and MT43C4258 is the variance in the functionality of the "QSF" pin. The MT43C4258 SSF input pin allows more efficient handling, and therefore higher throughput, of input or output data in either SAM. This improves the performance of video-graphics and networking systems by providing high clock speed and no latency time between reaching the stop point of valid data in one half and the loading of the new Tap address for the next half.

The SSF functionality is also available on the x8 versions of the TPDRAM, the MT43C8128 (QSF) and MT43C8129 (SSF). Refer to the data sheets for detailed timing and functional descriptions.

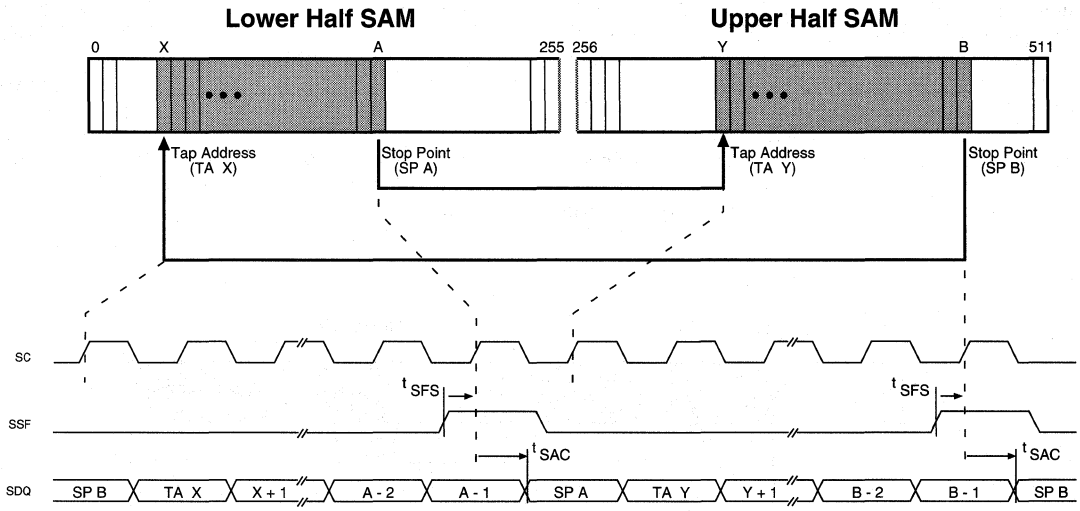


Figure 2
SSF OPERATION FOR THE MT43C4258 (SERIAL OUTPUT)

APPLICATION NOTE

ACCELERATE COMMON GUI OPERATIONS WITH A TPDRAM-BASED FRAME BUFFER

INTRODUCTION

Graphical user interface (GUI) performance is based on the ability of the graphics hardware to efficiently perform primitive graphics operations. Most of these operations rely on the movement of pixels from one area of memory to another. This operation, commonly referred to as BitBLT (short for bit-block transfer), is essential to graphics hardware performance. A BitBLT requires that before pixels are moved or copied, they must be read from one area of memory, then written back to a different area of memory. Graphics hardware that uses normal DRAM or specialized video RAM (VRAM) is forced to perform this operation in two steps because only a single port into the memory is available. Graphics hardware designed around triple-port DRAM (TPDRAM) can perform the BitBLT operation in a single step, because of the additional memory port. This ability, combined with the TPDRAM's other unique features, allows a TPDRAM-based frame buffer to give the highest BitBLT performance possible. This paper discloses a TPDRAM-based frame buffer design that accelerates GUI operations beyond DRAM- and VRAM-based solutions.

BACKGROUND

Basic GUI operation places high demands on the graphics subsystem. Central to the graphics subsystem is the graphics frame buffer. The frame buffer holds the digital representation of the display, and is typically implemented as a three-dimensional memory array. A particular frame buffer architecture must meet three demands placed on the memory bandwidth: screen refresh (supplying display pixels), DRAM refresh and random access. The display generation circuitry requires a stream of pixel data from the frame buffer in order to generate the video signals used to drive the display monitor. Screen refresh usually dominates the available bandwidth of most DRAM frame buffers and led to the development of the dual-ported VRAM. Frame buffers implemented with dynamic memories require continuous refresh cycles in order to retain seldom-accessed data. DRAM refresh usually consumes a small percentage of the available bandwidth but does complicate the frame buffer controller design. Variance in the first two bandwidth requirements will be proportionate to the display resolution. Additionally, the type of memory used will impact the efficiency of these operations. The remaining bandwidth is what is available to the graphics hardware to update the display. The amount of bandwidth available to random access must be maximized in order to achieve the greatest BitBLT performance.

Given a 72 Hz, 1,024 x 768 x 8 display (implemented as 512 x 512 x 32), 50 percent or more of the available memory bandwidth is consumed performing DRAM and screen refresh due to the single-port architecture of DRAM. An optimal DRAM frame buffer can provide approximately 40 MB/s of random access bandwidth. VRAM-based frame buffers circumvent screen refresh overhead by providing a serial access memory port dedicated to supplying pixel data to the display. This frees up the random port, allowing it to be used for random access operations. Frame buffers based on VRAM must dedicate only two percent of the available memory bandwidth to the screen- and DRAM-refresh overhead, which provides approximately 98 MB/s of random access bandwidth. BitBLT performance for VRAM- and DRAM-based frame buffers is, at best, half that of the available memory bandwidth since the BitBLT data must first be read from the frame buffer, then written back. Greater performance could be attained if the read and write operations were done concurrently.

The TPDRAM provides two serial ports and one random port. A TPDRAM-based frame buffer is similar to a VRAM-based frame buffer in that it provides a dedicated serial port for screen refresh, however it also provides an additional serial port. (The second serial port is available for other functionality. By connecting the second serial port to the random port through an alignment unit, a high performance BitBLT engine can be designed.) The TPDRAM also supports a number of features unavailable in either DRAM or VRAM that can be used to further accelerate GUI operations.

TPDRAM

The TPDRAM is currently based on the 1 megabit generation of VRAM. Internally the memory has an array that is 512 x 512 x 4 bits with two separate 512 x 4 serial access memories (SAMs) and a 512 x 4 bit mask register (BMR). The BMR can be used to mask data transfers between the memory array and each one of the SAM registers. Figure 1 provides a detailed block diagram of the TPDRAM.

The random port of the TPDRAM has the same features as the random port of a VRAM. Normal and page mode read/write cycles are supported as well as persistent and nonpersistent MASKED-WRITE operations. BLOCK-WRITE is also offered. The remaining two ports resemble the bidirectional serial port found on VRAM (with additional features). Each serial port is connected to the memory array via a 512 x 4 bus that passes through a 512 x 4 array of transfer gates. These transfer gates are controlled by the contents of the BMR. If bit-masking is enabled and a transfer between one of the SAM registers and the memory array occurs, then the transfer gates will mask those bits involved in the transfer that are not enabled in the BMR.

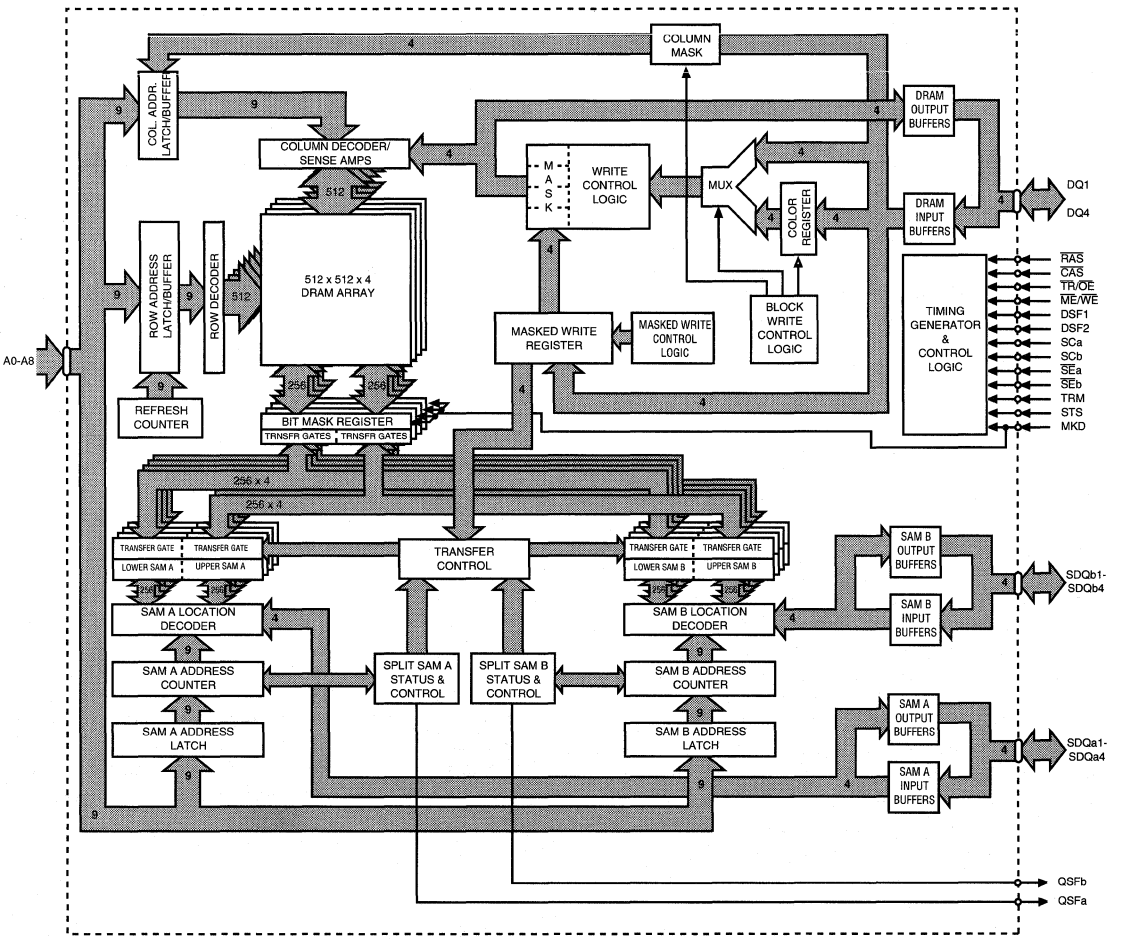


Figure 1
TPDRAM BLOCK DIAGRAM

The BMR is intended to be used for clipping operations with data into or out of the serial ports. The BMR may be loaded from a row in the memory array, cleared or inverted, or specified for each SAM cycle through a serial input pin. In addition, the BMR may also be used as a temporary register in order to implement advanced logic functions. Table 1 provides a partial truth table outlining special operations supported by the TPDRAM.

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ4[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	—	—
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

Table 1
TPDRAM PARTIAL TRUTH TABLE

A GRAPHICS DISPLAY SUBSYSTEM BASED ON A TPDRAM FRAME BUFFER DESIGN

A graphics display subsystem is usually comprised of a frame buffer memory, a frame buffer controller and video timing generator, a digital-to-analog converter, and circuitry that allows a processor or peripheral bus to access the pixel data. Implementing TPDRAM-assisted BitBLTs requires the addition of an alignment unit to the frame buffer and modification of the frame buffer controller.

A block diagram of a graphics display subsystem that uses TPDRAM for the frame buffer is shown in Figure 2. This graphics display subsystem is capable of performing unaligned BitBLTs at a rate of 100-million 8-bit pixels-per-second. Pattern fill operations and raster logic operations are performed at rates exceeding 1-billion pixels-per-second. Other graphics operations are enhanced in more subtle ways such as improved clipping performance.

The best way to describe a typical TPDRAM-assisted BitBLT operation is to consider a small pseudo-code example. In this case, a portion of a single display line is to be moved from one display line to another.

- Load SAMb (source X, source Y)
  Wait for completion
- Transfer pixels (Destination X
  Destination Y
  Number of pixels)
  Wait for completion

The command LOAD SAMb performs a DRAM to SAM transfer using the specified left-most pixel address. This will load the entire source row into SAMb and set the SAMb column pointer to the left-most pixel in the source space. Since a DRAM or screen refresh takes precedence over this operation, the controller waits for the SAM transfer to complete.

The TRANSFER PIXELS command causes the controller to specify alignment control to the alignment unit and then clock the pixels to be transferred out of SAMb, through the alignment unit and into the random port at the specified destination addresses. Pixel masking of the destination space is controlled entirely by the BitBLT control circuitry. This operation can be interrupted at any time by a screen or DRAM refresh and therefore must be polled to determine completion.

Transferring more than one row of pixels requires that the above routine be involved once for each display line.

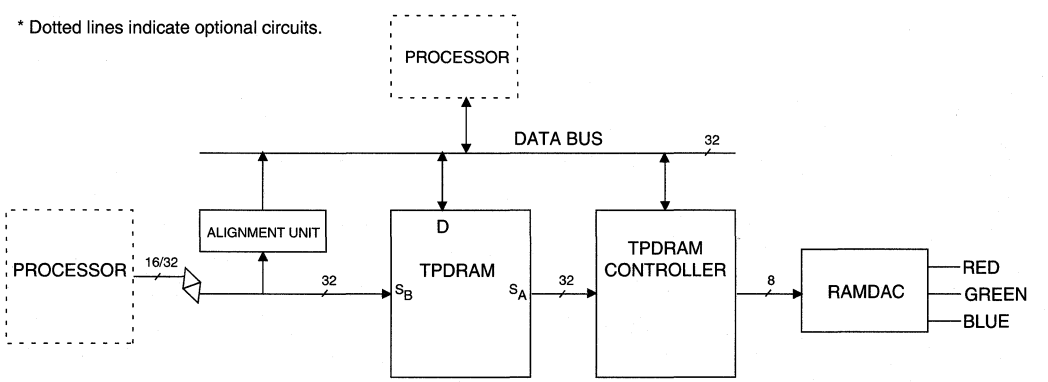


Figure 2
SYSTEM BLOCK DIAGRAM

COMPONENTS OF THE TPDRAM FRAME BUFFER

FRAME BUFFER

The TPDRAM frame buffer is required to provide two types of operation within a graphics display subsystem. The frame buffer must provide random access to allow the display to be updated, and must also be able to provide the pixel data that makes up each raster display line. The TPDRAM meets these requirements by providing two serial ports and a random port, all of which can be used to access the memory array.

SAMa provides access to the display memory to deliver pixel data to the display generation circuitry. SAMa is used because it lacks support for serial mask input (SMI) mode. SMI mode is used to specify a BMR mask when writing data into SAMb.

The random port is available to a processor or peripheral bus to support updating of the frame buffer contents. This port supports normal cycles as well as PAGE MODE READ and PAGE MODE WRITE cycles. The random port is used as the write port during BitBLTs involving the pixel alignment unit.

SAMb is used to provide bidirectional access to the display memory. SAMb is connected to the random port through the pixel alignment unit and is used as the read port during BitBLTs. The TPDRAM serial ports deliver a transfer performance rate approximately twice that of the random port during a page mode access. To take advantage of this feature, external bidirectional access into SAMb can be provided to support high bandwidth asynchronous data transfers such as those required to perform pattern-fill operations. The frame buffer is designed in a 256K x 32 array. This results in a 1,024-pixel x 1,024-pixel x 8-bit-per-pixel frame buffer. The 32-bit pixel word contains four 8-bit pixels. This configuration supports display resolutions up to 1,024 x 1,024 pixels. Each display line is mapped into memory so pixels that are vertically aligned on the screen have the same column address. This ensures that pixels are always vertically aligned both in screen coordinates and in physical memory. The BitBLT control circuitry is based on this mapping. Because of this requirement, split-mode transfer VRAM cycles are not required to load SAMa to drive the display generation circuitry.

The TPDRAM offers a number of memory cycles not found in other memory types. It supports cycles that allow powerful macro-level routines to be defined that operate on one or two display lines simultaneously. Programmable control of these additional cycle types is provided to allow the graphics programmer to make efficient use of the added functionality.

ALIGNMENT UNIT

The pixel alignment unit performs a pixel rotate based on the source and destination alignment of the pixel data being moved by a BitBLT operation. If the location of the pixel within the pixel word is different between the source and the destination, the pixel alignment unit shifts the pixels to ensure that the destination alignment requirement is met. The pixel alignment unit is designed to handle 8-bit pixels, but could be easily modified to support other pixel depths if required. The pixel alignment unit adds one pipeline delay to the BitBLT pixel data path.

CONTROLLER

The TPDRAM BitBLT controller manages the data transfer and memory control during BitBLT operations. It provides the capability to initiate most of the TPDRAM cycle types and is also responsible for controlling the entire BitBLT transfer process.

The controller is implemented as a memory-mapped device but could receive communication through a number of means depending on the graphics subsystem design. A block diagram showing the components of a TPDRAM controller is illustrated in Figure 3.

PRINCIPLES OF OPERATION

A BitBLT is defined as a transfer of pixels from one location in memory to another. The transfer can cross row and display line boundaries. The transfer can also require shifting of the pixels within the 32-bit pixel word. A BitBLT is specified by providing a source and destination starting address and the number of pixels to be transferred. It is assumed that the transfer will involve one or more horizontally aligned, adjacent pixels.

ALIGNMENT UNIT CONTROL

The TPDRAM frame buffer is 256K words deep by 32 bits wide. Given 8-bit pixels, a 32-bit pixel word contains four pixels. The source and destination addresses are pixel addresses; therefore, the two least significant bits (LSBs) of both the source and destination address are used to specify the alignment of the left-most pixel within the pixel word. The shift field required by the alignment unit can be determined by considering both the source and destination LSBs.

BITBLT TRANSFER TYPES

When the source and destination LSBs are both equal to zero and the pixel count is modulo four, the BitBLT is said to be an aligned transfer. Aligned transfers do not require any shifting of the pixel data as it is being transferred. Aligned transfers do not require any masking operations because only whole pixel words are involved in completing the BitBLT.

When either the source or destination LSBs are nonzero, or the pixel count is not modulo four (given pixel words of four pixels) then the transfer operation is said to be unaligned. Support for unaligned transfers is more complicated than that for aligned pixels. Unaligned transfers require that some form of masking be done at the start of the transfer, at the end of the transfer, or both. If the source and destination LSBs are zero but the pixel count is not modulo four, then a write enable mask is required to correctly transfer the last partial pixel word to the destination space.

MASK GENERATION

Correctly handling unaligned transfers requires several mask operations. A BitBLT involves reading pixel words from the SAMb port, passing the pixels through the alignment unit, then writing the resulting pixel data back into the frame buffer. Since not all of the pixels in a given pixel word will be updated during every cycle, a write mask on the random port is required. This write mask allows partial pixel words to be written into memory without disturbing the other pixels in the frame buffer. Because the source data resides in each SAM, a SAM shift clock mask is sometimes required. All possible combinations of source and destination alignments have to be supported. A thorough study of all possible combinations indicates that a multistage transfer operation is required to meet the requirements.

BITBLT OPERATION

Performing a BitBLT requires two actions. The first action is to perform a normal read transfer cycle into SAMb using the pixel address of the left-most pixel to be transferred. The column address pointer is specified to point at the pixel word that contains the left-most pixel to be transferred. The address bus is common to all four pixels within the pixel word and, therefore, SAMb is loaded with aligned

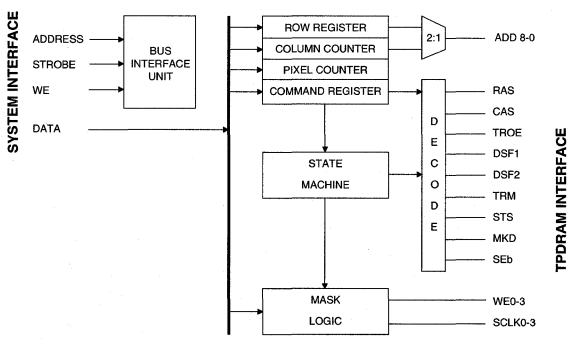


Figure 3
TPDRAM CONTROLLER

pixel data. The second action is to initialize the TPDRAM controller, indicating how many pixels are to be transferred and the destination address of the left-most pixel. The action of writing the destination address begins the BitBLT operation.

The BitBLT operation involves four separate steps to handle all possible transfer cases. The first two stages of a BitBLT are required to build the initial pixel word in the destination space. The third stage performs the transfer of all of the full pixel words required for the transfer. The fourth stage performs the writing of the final or rightmost pixel word, which is sometimes partial. All but the third stage use a write enable mask for each pixel in the pixel word. The first and second cycles also require a SAMb serial-port clock mask and a pixel-count enable mask. The value of each of these masks, based on the source and destination LSBs, is provided in Table 2.

THE FIRST CYCLE

The TPDRAM controller uses the two LSBs of the source and destination pixel addresses to form several masks that are used during the first two cycles of the BitBLT operation. As shown in the example in Figure 4, it is sometimes necessary to mask off one or more of the left-most pixels in the first pixel word to be written into the destination address. This mask operation is implemented by deasserting the write enable during the write operation to the first pixel word in the destination.

Also illustrated in the example, there exist scenarios where the first pixel word in the destination space must actually be built from both the first and second pixel words in the source space. A counter is used to generate the column portion of the destination address during a BitBLT. If the first two pixel words in the source are required to build the first pixel word in the destination space then the column pointer must be the same during the first two cycles. The COUNTEN field in Table 2 indicates which scenarios cause this to happen.

It is preferable to write full pixel words during the middle cycles. A mask is applied to the serial clocks for SAMb to keep the controller from having to build each pixel word in the destination space similar to the first two cycles of the BitBLT. By correctly masking the serial clocks, the column pointers for each pixel within the pixel word are set so that during the middle cycles, the correct pixels are identified and all pixels can be clocked simultaneously for the remainder of the transfer operation. Table 2 indicates the serial clock mask operation during the first two cycles for each of the address scenarios. Figure 4a shows the state of the destination space and SAMb after the first cycle.

SOURCE ADDRESS LSBS	DEST. ADDRESS LSBS	LEFT SHIFT	FIRST MEMORY CYCLE			SECOND MEMORY CYCLE		
			COUNT ENABLE	WRITE ENABLE MASK 0 1 2 3	SERIAL CLOCK MASK 0 1 2 3	COUNT ENABLE	WRITE ENABLE MASK 0 1 2 3	SERIAL CLOCK MASK 0 1 2 3
3	3	0 0	1	0 0 0 1	1 1 1 1	1	1 1 1 1	1 1 1 1
3	2	0 1	0	0 0 1 0	1 1 1 1	1	0 0 0 1	1 0 0 0
3	1	1 0	0	0 1 0 0	1 1 1 1	1	0 0 1 1	1 1 0 0
3	0	1 1	0	1 0 0 0	1 1 1 1	1	0 1 1 1	1 1 1 0
2	3	1 1	1	0 0 0 1	1 1 1 0	1	1 1 1 1	1 1 1 1
2	2	0 0	1	0 0 1 1	1 1 1 1	1	1 1 1 1	1 1 1 1
2	1	0 1	0	0 1 1 0	1 1 1 1	1	0 0 0 1	1 0 0 0
2	0	1 0	0	1 1 0 0	1 1 1 1	1	0 0 1 1	1 1 0 0
1	3	1 0	1	0 0 0 1	1 1 0 0	1	1 1 1 1	1 1 1 1
1	2	1 1	1	0 0 1 1	1 1 1 0	1	1 1 1 1	1 1 1 1
1	1	0 0	1	0 1 1 1	1 1 1 1	1	1 1 1 1	1 1 1 1
1	0	0 1	0	1 1 1 0	1 1 1 1	1	0 0 0 1	1 0 0 0
0	3	0 1	1	0 0 0 1	1 0 0 0	1	1 1 1 1	1 1 1 1
0	2	1 0	1	0 0 1 1	1 1 0 0	1	1 1 1 1	1 1 1 1
0	1	1 1	1	0 1 1 1	0 1 1 1	1	1 1 1 1	1 1 1 1
0	0	0 0	1	1 1 1 1	1 1 1 1	1	1 1 1 1	1 1 1 1

Table 2
MASK LOGIC TRUTH TABLE

THE SECOND CYCLE

The second cycle of the BitBLT operation is similar to the first cycle. The controller masks write-enable and serial-clock for each pixel based on the source and destination address LSBs. The column counter is allowed to advance in all cases because at the end of the second cycle, the first pixel word of the destination space, at least, has been transferred. Second cycle operation is the same as first cycle operation. Figure 4b shows how both the write enable mask and shift clock masks are used to complete the update of the first pixel word in the destination space and set up SAMb for the middle cycles.

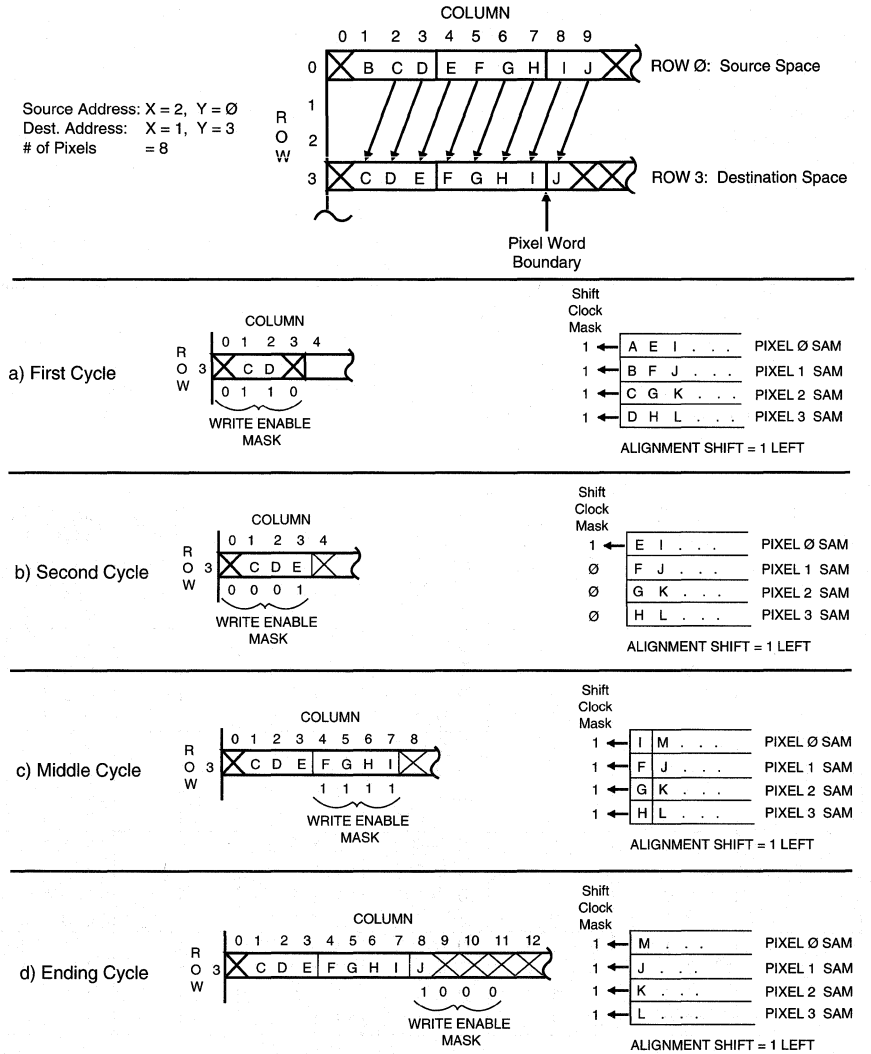


Figure 4
EXAMPLE OF BITBLT

THE MIDDLE CYCLES

The first two cycles of the BitBLT handle all of the masking required to write the first pixel word and align the SAMb pointers for each pixel within the pixel word. Under these conditions, no masking is required during the middle cycles, and the controller can transfer pixels at the full bandwidth of the TPDRAM random port. The following occur for each remaining pixel word: SAMb is clocked and the pixel word is output, aligned, and written into the random port at the destination address. This continues until the pixel counter has counted down to one, where the ending cycle begins. Figure 4c shows a typical middle cycle. Note how the alignment value affects the pixel position within the destination space.

THE ENDING CYCLE

Depending on the destination address and the number of pixels being transferred, a write-enable mask is sometimes required to correctly transfer the final pixel word into the destination space. When the pixel word counter has counted down to a value of one, the destination address LSBs and pixel count LSBs are evaluated to determine how many transfer cycles are required to complete the BitBLT operation and what the write-enable mask should be for the last pixel word. Table 3 lists the possible scenarios. Figure 4d shows how the write enable mask is used.

DESTINATION LSBS	NUMBER PIXELS MOD 4	ENDING WRITE ENABLE MASK 0 1 2 3
0 0	0	1 1 1 1
0 1	0	1 0 0 0
1 0	0	1 1 0 0
1 1	0	1 1 1 0
0 0	1	1 0 0 0
0 1	1	1 1 0 0
1 0	1	1 1 1 0
1 1	1	1 1 1 1
0 0	2	1 1 0 0
0 1	2	1 1 1 0
1 0	2	1 1 1 1
1 1	2	1 0 0 0
0 0	3	1 1 1 0
0 1	3	1 1 1 1
1 0	3	1 0 0 0
1 1	3	1 1 0 0

Table 3
ENDING CYCLE WRITE ENABLE TRUTH TABLE

ENHANCING OTHER COMMON GRAPHICS OPERATIONS

The TPDRAM can be used to enhance other primitive graphics operations. Pattern-fill operations may be improved by first loading SAMb with a pattern loaded into off-screen memory, then transferring SAMb through the BMR, which has been previously loaded with a mask. For large shapes, a significant improvement in performance may result.

Row-oriented logical operations may be improved by using the off-screen memory, SAMb and the BMR. BMR-to-DRAM transfer operations, and DRAM-to-BMR transfer operations permit inverting the transfer data. This feature, when combined with the AND operation that the BMR provides, permits complex logic functions to be constructed using a series of transfer cycles.

Additionally, a graphics display architecture can be designed to read and write serial pixel/mask streams using the SAMb serial port. This functionality can be useful for quickly loading masks, pattern data or other pixel data. This port allows for transfer rates up to 200 MB/s.

SUMMARY

The TPDRAM shows its advantage over DRAM- and VRAM-based solutions when a BitBLT circuit is defined that allows concurrent READ and WRITE operations during BitBLT operations. Performance can approach 100 million pixels-per-second BitBLT rates with logical and pattern fill operations sometimes exceeding several billion pixels-per-second. GUI operations can be modified to take advantage of the additional functionality a TPDRAM frame buffer provides, resulting in more performance and greater flexibility than DRAM- or VRAM-based designs.

NEW ■ APPLICATION/TECHNICAL NOTE

APPLICATION NOTE

USE OF TPDRAM FOR SMARTER/FASTER NETWORK APPLICATIONS

INTRODUCTION

Advanced network applications need a high bandwidth memory buffer with serial access that provides full duplex data flow for maximum flexibility and control. Current network designs address these needs with SRAM or dual-port DRAM (VRAM) devices. However, Micron Semiconductor's Triple-Port DRAM (TPDRAM) is an alternative. The 8-bit wide, MT43C8128/A and MT438129/A (including "A" versions), provide the optimum density and bandwidths required by high-end network buffers. The TPDRAM is less expensive than SRAM devices and offers higher performance. It also has uninterrupted, bidirectional capabilities, which VRAM devices do not provide. The TPDRAM may be used with all networking standards and protocols. The bandwidth of the three ports provides uninterrupted 40 MHz data flow in each of two directions and data manipulation "off line" at 22 MHz (FAST-PAGE-MODE).

The advancement and merging of network and channel architectures demands higher bandwidths and reduced system cost. The need for total system speed is the main focus of this discussion. However, the TPDRAM can increase overall system bandwidth while reducing the cost of the network/channel buffer. This paper presents the basic TPDRAM architecture, highlighting special features and discussing ideas for system implementation with a TPDRAM network buffer.

Current high-bandwidth network and channel interface boards use DRAM, VRAM or some kind of SRAM for local data buffering. These memories reduce latency in the receive/transmit capabilities of the network. They do this by storing data packets locally before they are sent over the network or forwarded to the system memory via host control or DMA moves. Existing memory solutions have been adequate for this task. However, these solutions are not able to sustain the required bandwidth of high-speed communication channels and networks because of the increasing demands of higher-speed system buses, multiprocessors, network bandwidth and increasing data volumes required by ever-more-powerful workstations. Speeds on future fiber optic networks such as ATM, Sonet, SHIPPI and Fiber Channel will be in excess of 1 Gbit/sec (Gbps).

THE TPDRAM

ARCHITECTURE

The TPDRAM was introduced by Micron Semiconductor as an evolution of the dual-port DRAM (VRAM) architecture. The device is targeted at two general applications; high-end graphics frame buffers and networking data buffers. Like the VRAM, the TPDRAM is based on a dynamic random access memory (DRAM) array. Both devices were created to enhance standard DRAM bandwidth.

A second memory and I/O port are added to a standard DRAM to make a VRAM (Figure 1). This second memory is an autonomous static RAM that is accessed in a sequential manner with its own address counter and pointer logic. Keep in mind, the data is the same width

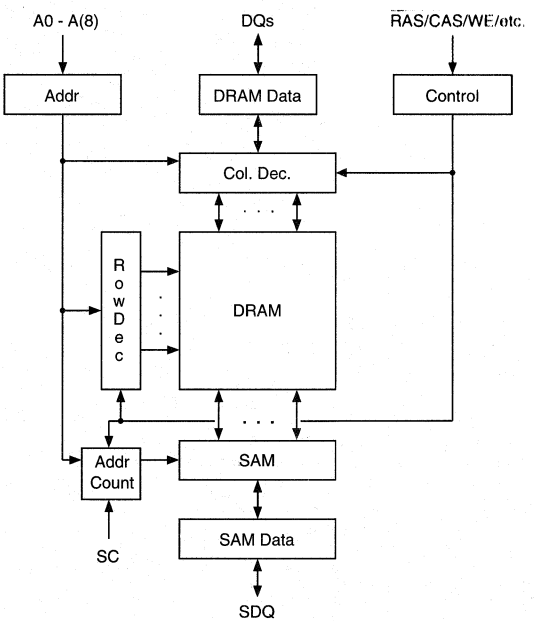


Figure 1
DUAL-PORT DRAM

NEW APPLICATION/TECHNICAL NOTE

as the DRAM port, 4 or 8 bits—not serial. Because of its serial (as opposed to random) access, this memory is commonly referred to as a serial access memory, or SAM. The SAM, which can be thought of as a FIFO, is well suited for network communication buffers. However, for full duplex communication into and out of the network data buffer, the VRAM is still a restrictive solution because the SAM can only move data one direction at a time.

The TPDRAM expands the VRAM architecture by adding a second SAM and I/O port. This new port gives the TPDRAM one DRAM port and two serially accessed memory ports (Figure 2). The control of the TPDRAM is similar to the control of a VRAM. In fact, it can be operated as a VRAM with no controller modifications.

SERIAL ACCESS MEMORY

The serial access memories in the TPDRAM are equal in length to one row of the DRAM array, and loaded internally by performing a special DRAM $\overline{RAS}$-$\overline{CAS}$ cycle. The load cycles, called "transfer(s)," load a row of DRAM into either SAM, or load either SAM into a row of DRAM, in only one DRAM cycle. The two SAMs run asynchronously and independently of each other and the DRAM, except when they are involved in a transfer (Figure 3). As a result, data can be written into the DRAM, read out of one SAM, and written into one SAM all at the same time and at different rates. The SAM ports of the TPDRAM are capable of speeds of 40 MHz, with 50 MHz planned for the future. They use two control inputs to access data: a serial enable ($\overline{SE}$) and serial clock (SC). The rising edge of the serial clock increments the address counter, and inputs or outputs the SAM data.

RANDOM (DRAM) OPERATION

The DRAM port provides the host bus interface with a bidirectional port that may be accessed randomly, and with the option of FAST-PAGE-MODE access. FAST-PAGE-MODE allows the host or local processor to access the DRAM data at a cycle time three times faster than random $\overline{RAS}$-$\overline{CAS}$ access cycles. This feature is very useful for high-speed DMA moves of data packets between the host-system main memory and the network adapter memory. When in FAST-PAGE-MODE, the access is restricted to one row (page) of the array, while the columns may be accessed randomly within the row. If the row address changes, a new $\overline{RAS}$-$\overline{CAS}$ cycle must be performed to "open" the new page.

The random port of the TPDRAM also provides a write-per-bit (MASKED WRITE) function when writing data to the memory array.

In addition, the DRAM (or random port) is used to control data transfers to the SAM ports. All internal movement of data is controlled by the $\overline{RAS}$ signal in conjunction with control pins that are latched as $\overline{RAS}$ falls. In fact, all access operations (DRAM access, Transfer, MASKED WRITE, etc.) are defined at the falling edge of $\overline{RAS}$. The only cycle that is selected at the falling edge of $\overline{CAS}$ is BLOCK WRITE, which is geared to graphics systems and not detailed here. Figure 4 illustrates the control setup for cycle definition in the TPDRAM. All function control pins (e.g. $\overline{TR}/\overline{OE}$, STS, $\overline{DSFI}$, etc.) are included in the "control" window at $\overline{RAS}$ LOW.

A transfer cycle requires a temporary interrupt of any access requests to the DRAM port and, for some transfers, will interrupt data into or out of the selected SAM. The three memory elements are independent of, and asynchronous to, each other when not involved in a data transfer.

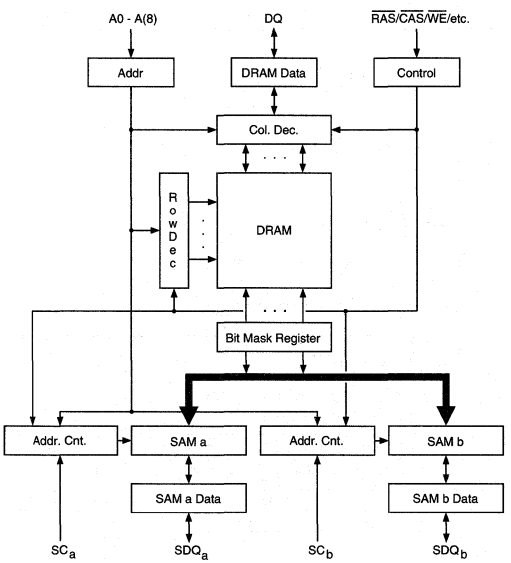


Figure 2
TRIPLE-PORT DRAM ARCHITECTURE

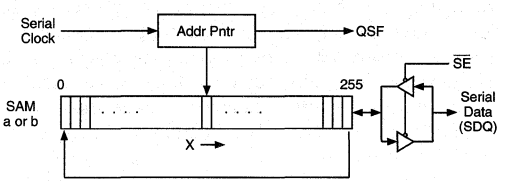


Figure 3
SAM ACCESS AND CONTROL

TRANSFER OPERATIONS

Operation of data transfers is straightforward. Six control pins are added to the typical DRAM control signals, and $\overline{OE}$ is converted to a dual function (Figure 4). Some of these pins may be permanently tied to a logic state or actively driven by control logic, depending on the functionality required by the system.

Two pins, TRM and MKD, are used to incorporate the internal BIT MASK REGISTER into the transfer (described later). They may be tied to ground to permanently disable the BMR, if it is not required.

Row data may be transferred to either SAM (but not both at once) during a transfer. The STS pin selects the SAM through which a transfer will occur. A transfer to a SAM of a page of the DRAM is called a read transfer. If the transfer is from a SAM to a page of the DRAM, it is called a write transfer.

Split transfers are provided to allow easy, uninterrupted data streams into or out of the SAM. The DSF1 pin is used to select either SPLIT READ TRANSFER or SPLIT WRITE TRANSFER. The SAMs on the TPDRAM offer an added feature that can be very beneficial to networking. Industry standard VRAMs with a split SAM provide a split SAM status pin, or QSF. This pin is LOW if the access is in the lower half address space of the SAM, and HIGH if it is in the upper half address space. Parts with this pin will access data beginning at the starting address (or Tap) of the SAM and progress through the address until they reach a SAM-half boundary. Then the access will jump to the new tap address of the new half and the QSF will change state. The MT43C8128 TPDRAM also operates this way. The function of the QSF pin changes for the MT43C8129; it is made an input and called split SAM special function (SSF). With this pin, it is possible to cease access at any location in one half of the SAM and force a jump to the tap address of the next half. Compared with standard VRAM, this can greatly improve overall bandwidth by allowing more efficient use of the serial clock. Without this function, a packet of data that did not fill the entire half of the SAM would still require enough extra clock cycles to advance the address count to the tap of the next half for a new packet to be input and stored. This would also apply to output packet data. The SSF pin allows the address to jump to the next tap and be ready for new data without adding extra clock cycles as soon as the end of a packet is reached.

BIT MASK REGISTER OPERATION

In addition to the great improvement in data flow, the TPDRAM also adds an extra dimension of memory intelligence. A bit mask is provided to allow masking of the SAM or DRAM data during transfers. To perform the masking function, an internal register that is the same size as a SAM has been added to the part. It is called the BIT MASK REGISTER (BMR). The BMR may also be used as an extra page for scratch pad memory. Data from the DRAM or either SAM may be transferred to the BMR in one $\overline{RAS}$-$\overline{CAS}$ cycle. The data stored in the BMR may be used as a mask when transferring data between the DRAM and SAMs by performing a BIT MASKED TRANS-

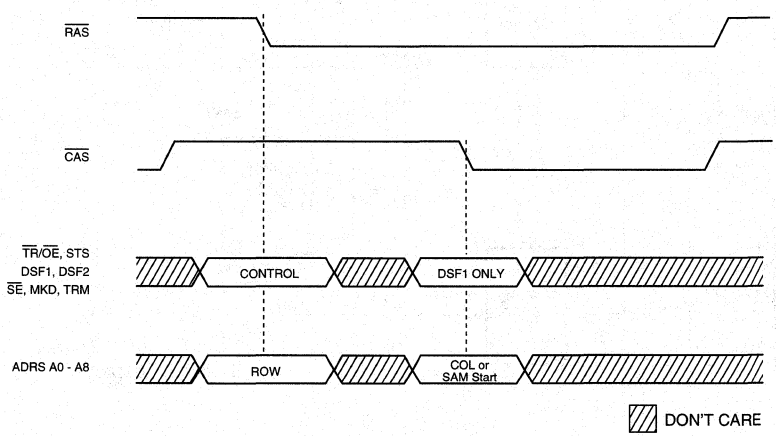


Figure 4
BASIC TPDRAM ACCESS CONTROL

FER cycle in lieu of a normal transfer. The BIT MASKED TRANSFERs can also be done as SPLIT TRANSFER.

During a BIT MASKED TRANSFER, each location in the SAM or DRAM (column location) will be masked by the corresponding location in the BMR. A logic "0" in that location will mask that bit during a BIT MASKED TRANSFER and the addressed destination location will not be changed. A logic "1" will allow the new data to be written.

The BMR may also be loaded serially by clocking-in mask data with the SCb clock pin. This mode is called the serial mask input (SMI) mode. When this mode is enabled (at $\overline{RAS}$ time), any location addressed by the SAMb address pointer will have the corresponding BMR location written to all 1's or all 0's, whichever is valid on the MKD input pin. In addition, when this mode is enabled, the contents of the BMR will be cleared automatically when a BIT MASKED WRITE TRANSFER is done from SAMb.

The BMR has been found to be useful in high-end networking applications for protecting portions of a row when transferring packets from the SAM to the DRAM. The protected areas may contain constant header and control information used by the host processor. This simplifies packing multiple packets in each DRAM row.

NETWORK APPLICATIONS

The two SAM ports of the MT43C8128/9 provide a network with full duplex input and output from the memory space without interrupting the system access to the DRAM.

In the design of high-speed networks, the overall memory bandwidth can have a great effect on the performance of the entire host system. The local data memory buffer must allow access time for the node CPU and at the same time allow the network interface logic access for incoming or outgoing data. This can tax the total system speed, slowing down the system and the network. The TPDRAM allows each part of the system to access a common memory bank simultaneously and asynchronously (Figure 5).

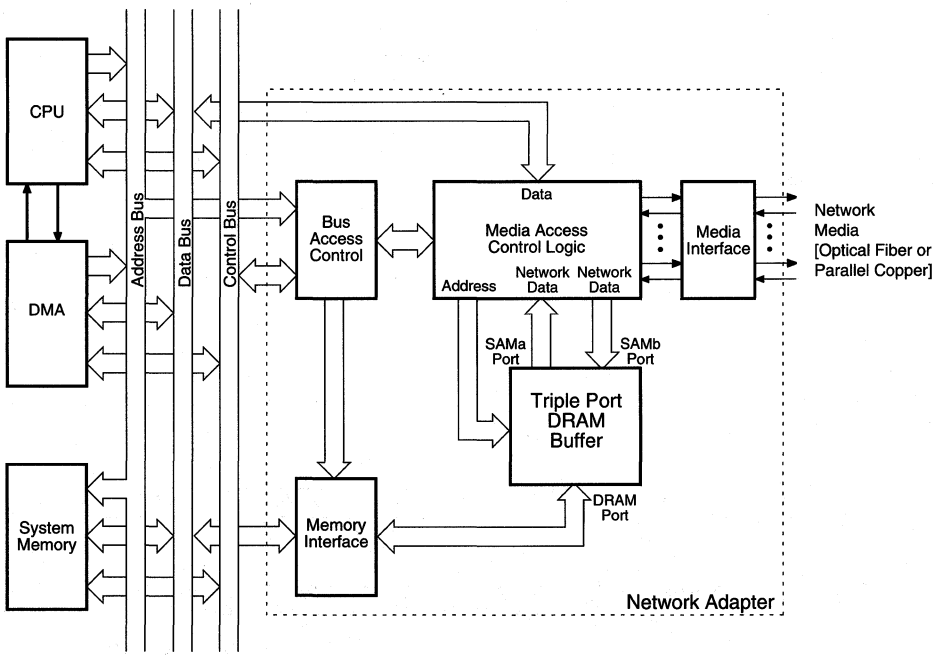


Figure 5
TYPICAL FULL DUPLEX NETWORKING APPLICATION USING TPDRAMS

NEW APPLICATION/TECHNICAL NOTE

The access time available to the node processor is as important as the bandwidth of the network port (SAMs). The local (or node) processor must have easy access to header and trailer bits to control packet flow into the system and on the network. Information to be sent on the network must be loaded quickly, either by host processor control or DMA moves. Data from the network must be rapidly routed to the appropriate processor or memory subsystem. All these operations are impacted by memory latency in the network buffer memory.

The node or local processor is allowed more time to access the data stored in the buffer by allowing the SAM ports to be the input and output ports for the network or channel. The DRAM port of the TPDRAM will typically be available for access by the system bus 97 percent of the time (Equation 1). Compare this to the single-port architecture of standard DRAM, which would only allow the node processor 40 to 60 percent of the memory bandwidth, depending on the network speed and interface card architecture.

$$\%Dav = [(^{t}max - {}^{t}tran - {}^{t}ref)/{}^{t}max] * 100 \quad (1)$$

Where:

- %Dav = Percent of time DRAM port is available for access
- ^{t}max = Maximum DRAM cycle time through memory (FAST-PAGE-MODE)
- $^{t}tran$ = Transfer time required to maintain constant data at the SAM ports
- ^{t}ref = Time required to perform refresh

The vast improvement to the DRAM bandwidth is translated into faster data throughput. Using four MT43C8128 TPDRAMs, a 128K x 32 memory array can be built with a total data rate of 160 megabytes/sec for data transceivers (SAMs) and 80 megabytes/sec for host access (FAST-PAGE-MODE rate). Futhermore, these data rates can be sustained simultaneously and in any direction.

Figure 6 illustrates how the TPDRAM would fit into a FDDI type network buffer/interface. The TPDRAM ar-

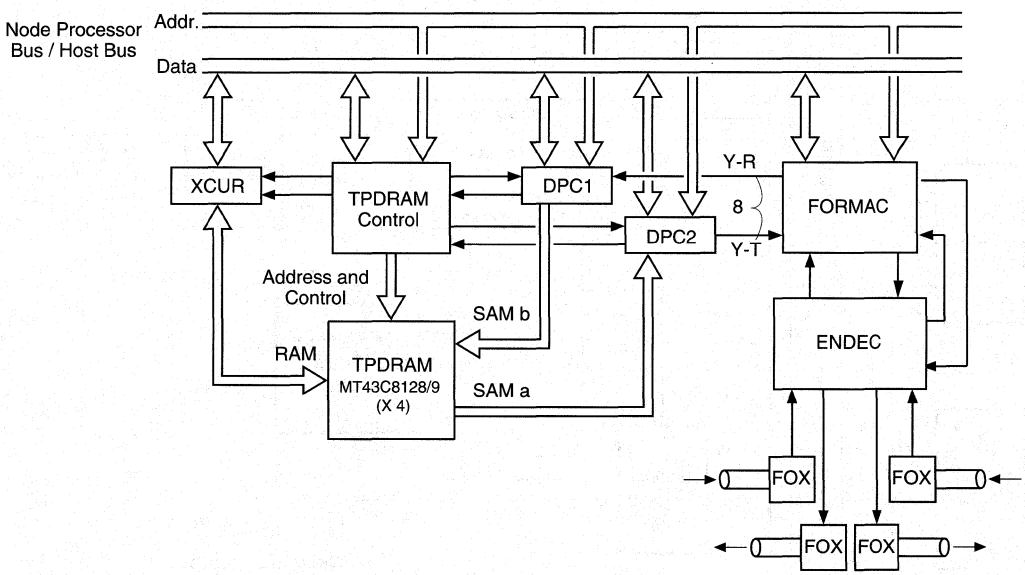


Figure 6
FDDI NETWORKING APPLICATION USING TPDRAMS

chitecture allows full duplex operation with a single bank of continuous memory. This offers flexibility in memory mapping by allowing the amount of memory space for receive and transmit data to be changed and reallocated.

The system shown in Figure 6 is based on the SUPERNET™ chipset from Advanced Micro Devices. The chip set must be modified by adding an FPLD device to perform the TPDRAM control. This would replace AMD's RAM Buffer Controller chip. A node processor handles data transfers to and from the SAM port when requested by the FORMAC/DPC chips. The data will then be routed to the DPC for byte transmission to the FORMAC and ENDEC.

The TPDRAM's flexibility means it can be used in almost any network or channel application. For example, a half-duplex system could be constructed. In this type of system, the SAMs are dedicated to the network control logic and to the host system bus. The DRAM port is solely accessed and controlled by a local node processor. This example allows faster DMA to the host than the full duplex implementation and allows half duplex access to the network (see figure 7). However, the network type is not restricted.

SUMMARY

The TPDRAM offers system designers a high density, high-bandwidth memory that reduces the chip count and the cost of network adapter boards.

Its flexibility makes the TPDRAM applicable to many network or channel architectures and protocols. The control of the device has been kept close to industry standard VRAMs. Extra features like the SSF input pin and the BIT MASK REGISTER give the TPDRAM even greater flexibility and intelligence.

This architecture can be applied to any network protocol including SONET, ATM, HIPPI, Fiber Channel and other fiber or parallel networks.

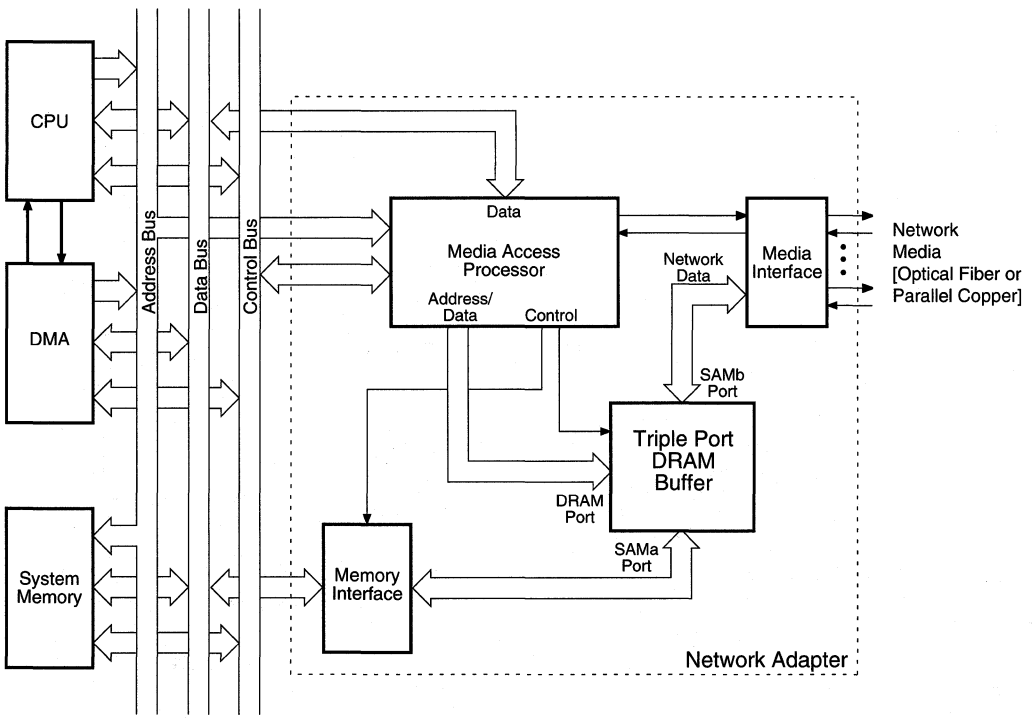


Figure 7

MICRON
SEMICONDUCTOR, INC.

OVERVIEW

Product reliability is a product's ability to function over time within given performance limits, under specified operating conditions. This section contains a brief overview of some of the issues that affect the reliability of IC devices, and a brief overview of Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's quality/reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failures and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates products using intelligent burn-in. The unique AMBYX® intelligent burn-in/test system developed by Micron is described in the following section.

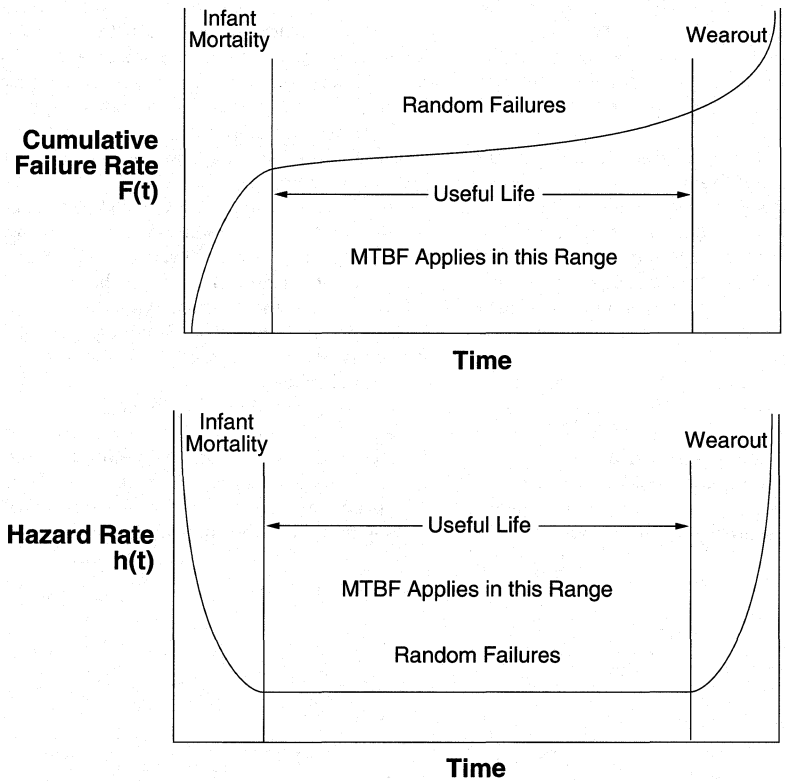


Figure 1
RELIABILITY CURVE

RELIABILITY

MICRON'S AMBYX® INTELLIGENT BURN-IN AND TEST SYSTEM

Burn-in refers to the process of accelerating failures that occur during the infant mortality phase of component life to remove the inherently weaker devices. The process has been regarded as critical for ensuring product reliability since the beginning of the semiconductor industry. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, when we were unable to find a system that met our requirements, we introduced the concept of "intelligent" burn-in and developed the AMBYX® intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots not exhibiting a stable failure rate to additional burn-in. This burn-in flow also brings to our attention the slightest variation in a product's failure rate.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then we ramp up the oven to 85°C for more functional testing. This enables us to thermal intermittent failure detection, another unique capability of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons why Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test used by IC manufacturers to compute random field failure rates. Second, we want to be sure we are not, by testing at extremely elevated conditions, introducing new failure modes unrelated to normal wearout, such as VOS.

Control charts, such as the one shown in Figure 3, alert us to trends in lot failure rates. When we detect an upward trend in a failure rate, we correlate the lots that need additional burn-in with all the variables that might be influencing the increased rate. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

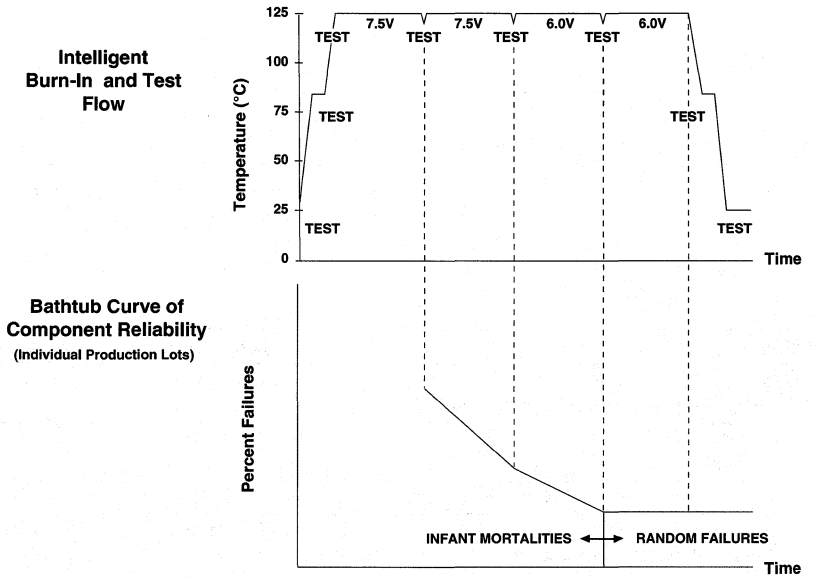


Figure 2
AMBYX BURN-IN/TEST FLOW AND TEST RESULTS

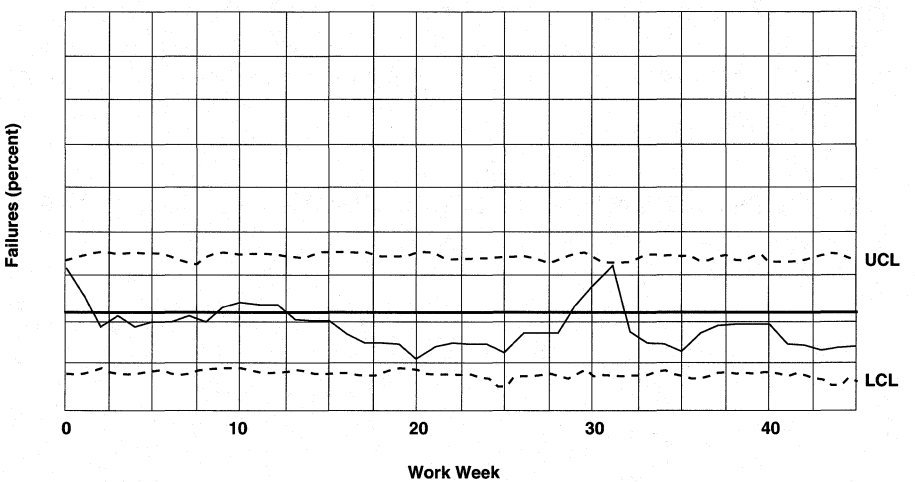


Figure 3
AMBYX FOURTH QUARTER FAILURES

RELIABILITY

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use. Figure 3 shows the conditions for these tests, known as environmental stress tests. The EPM program described in Figure 4 is for Micron's 2 Meg VRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6V, Checkerboard and Checkerboard Complement Pattern)	1,008 Hours	60 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% RH, 5.5V, Alternating Bias)	1,008 Hours	60 Devices
AUTOCLAVE (121°C, 100% RH, 15 PSI, No Bias)	96 Hours	30 Devices
LOW TEMPERATURE LIFE (-25°C, 7V, Checkerboard and Checkerboard Complement Pattern)	1,008 Hours	10 Devices
TEMPERATURE CYCLE (0°C for 15 min., +125°C for 15 min, air to air)	1,000 Cycles	30 Devices
THERMAL SHOCK (-55°C for 5 min., +125°C for 5 min., liquid to liquid)	700 Cycles	30 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	30 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	30 Devices

NOTE: Samples used in the EPM program are taken from five different lots at finished goods. Before being subjected to environmental testing, all surface-mount products are run twice through an infrared (IR) reflow furnace, reaching a peak temperature of 220°C.

Figure 4
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 2 MEG VRAM

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). Using Micron's 4 Meg DRAM as an example, the failure rate is calculated as follows:

$$\text{Failure Rate} = \frac{Pn}{\text{Device hours} \times AF}$$

where: Pn = Poisson Statistic (at a given confidence level). In our example given one device failure, Pn = 2.022 at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours). In our example, device hours equal 9.479×10^5 in an accelerated environment.

AF = acceleration factor between the stress environment and typical use conditions. For the 2 Meg VRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 56. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 2 Meg VRAM family is computed as follows:

$$\text{Failure Rate} = \frac{2.022}{(9.479 \times 10^5)(56)} = 3.809 \times 10^{-8}$$

where: total device hours at test conditions = 2.723×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 56 equals 56 $(9.479 \times 10^5) = 53 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

$$\text{Failure Rate} = (3.809 \times 10^{-8}) \times 10^5 = 0.003809\% \text{ or } 0.0038\% \text{ per 1K device hours}$$

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

$$\text{Failure Rate} = 3.809 \times 10^{-8}) \times 10^9 = 3.809 \text{ or } 38 \text{ FITs.}$$

ACCELERATION FACTOR CALCULATION

Again, using the 2 Meg VRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\left[\frac{E_a}{kT_O} - \frac{E_a}{kT_S}\right]}$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5} eV/K.

T_O and T_S = typical operating and stress temperatures, respectively, in kelvins.

E_a = activation energy in eV. (For oxide defects, which is the most common failure mechanism for the 4 Meg DRAM used in our example. The activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_V = e^{\left[\beta (V_S - V_O)\right]}$$

where:

v_S and v_O = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 2 Meg VRAM used in our example, ß equals 2).

Thus, the voltage acceleration factor for the 2 Meg VRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 7.39.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$\begin{aligned} AF_{overall} &= AF_{temperature} \times AF_{voltage} \\ &= 7.62 \times 7.39 \\ &= 56 \end{aligned}$$

RELIABILITY

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a one percent sample from each production lot. These samples are subjected to visual and electrical testing to measure the acceptable quality level (AQL) of all outgoing product. Test flows for new products that have not met required production volume and ppm levels are more comprehensive than for mature products. Over a period of time, as a product matures, the objective is to eliminate those tests devices never fail. AQL testing, although it is performed on only a small percentage of each product, is much more exhaustive. Conducted at spec conditions without guardband for every known timing, pattern and background, it is a sanity check on the production test flow. Its purpose is to detect subtle shifts in defect mechanisms which the production test flow may not catch.

Visual testing for mechanical defects consists of visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Testing is conducted at 0°C, or room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the devices are retested beginning at that point in the test flow. These are important steps to preserve the integrity of our test process.

AUTOMATED DATA CAPTURE AND ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

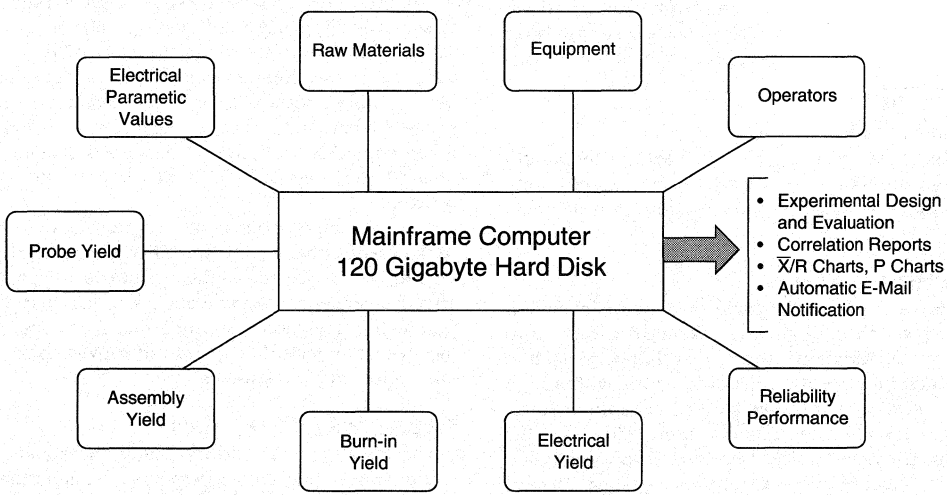


Figure 5
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\bar{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors, such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL (SPC) CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE/MULREG

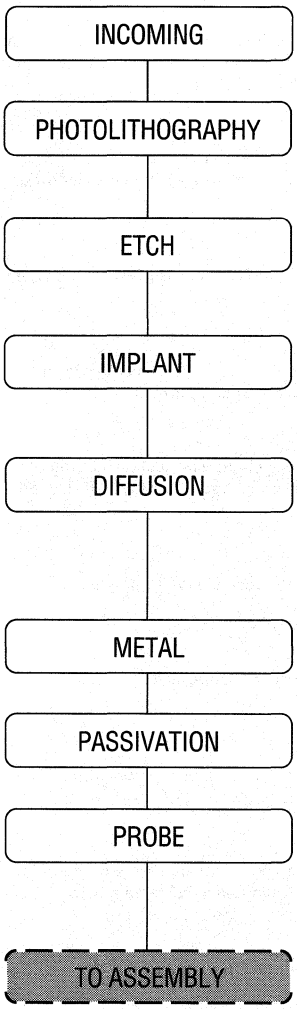
This analysis software is used for experimental design and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble-shooting. It is also used to determine the relationships between process output, probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.

GAUGE CAPABILITY STUDIES

These studies are performed on both new and existing equipment. Gauge studies help us understand the cause of variation in a measurement process and determine the amount of variation in the system.

FABRICATION*



Incoming
Verification that the starting material is clean, uniform and compliant with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping" and forms conductive regions on the wafer.

Diffusion
Silicon dioxide, nitrite and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases which either react with the silicon, causing it to oxidize and form an SiO_2 layer or react with each other, forming poly and nitrite deposits. These layers are patterned using photolithography and form the layers of the diodes, transistors and capacitors of the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

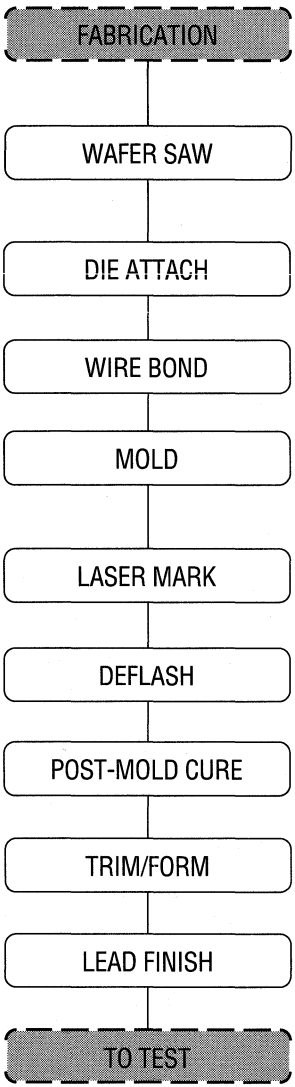
Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many die. Each individual die on the wafer is taken through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map," storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good die are packaged.

Assembly (see next page)

*This flow is general and based on DRAM products.

ASSEMBLY*



Fabrication
Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire the diameter of a human hair. These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Deflash
Prior to lead-finish processing, the leadframes are run through chemical baths to remove contaminants. This process is known as deflash.

Post-Mold Cure
Molded leadframes are placed in an oven for four and one-half hours at 175°C to complete the polymerization of the epoxy encapsulant.

Trim/Form
A press with a tool set is used to cut and form leads of the lead frame into specified shapes. Some packages have leads formed for surface-mount applications. Other packages have leads for through-hole applications.

Lead Finish
Each package is given a lead finish of tin/lead (solder) to ensure reliable application by the customer.

Test (see next page)

*This flow is general and based on DRAM products.

ASSEMBLY

HOT PREGRADE

MARKING

BURN-IN

AMBIENT POSTBURN

HOT FINAL

SCANNER

VISUAL INSPECTION

AQL

PACKAGING

FINISHED GOODS

TEST*

Assembly

Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade*

All testing (including speed sorting, parametric and functional testing) is conducted at 85°C. Parametric tests are performed to detect opens, shorts, input/output leakage, and to determine whether input/output high and low levels and standby and operating currents are within specified limits. Functional tests include low/high Vcc margin, vbump, speed sorting, dynamic and static refresh, long ^{t}RAS and ^{t}CAS lows and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single/multiple walking columns and diagonals and fast-page or static-column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Marking

Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Burn-in

Micron uses its exclusive AMBYX intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in, using checkerboard and checkerboard-complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first two intervals and 125°C, 6V Vcc for the final two intervals. During temperature ramping from 25°C to 85°C and back to 25°C, AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Ambient Postburn*

All testing is performed at 25°C. Parametric tests are performed to detect opens, shorts, input/output leakage, and to determine whether input/output high and low levels and standby and currents within specified limits. Functional tests include low/high Vcc margin, vbump, speed sorting, dynamic and static refresh, long ^{t}RAS and ^{t}CAS lows and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals and fast-page or static-column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Hot Final*

All testing (including speed grade verification and parametric and functional testing) is conducted at 78°C. Parametric tests are performed to detect opens, shorts, input/output leakage, and to dtermine whether input/output high and low levels and standby and currents within specified limits. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, long ^{t}RAS and ^{t}CAS lows and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals and fast-page or static-column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Scanner

Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection

All devices determined functional are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired, if possible. Data on the type of defects found is carefully recorded and used for improving the manufacturing processes in both assembly and test.

AQL

A quality assurance monitoring program overseas the electrical and environmental performance of all production lots. New products which have not met required production volume and ppm levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron's requirements.

Packaging

Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry-packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods

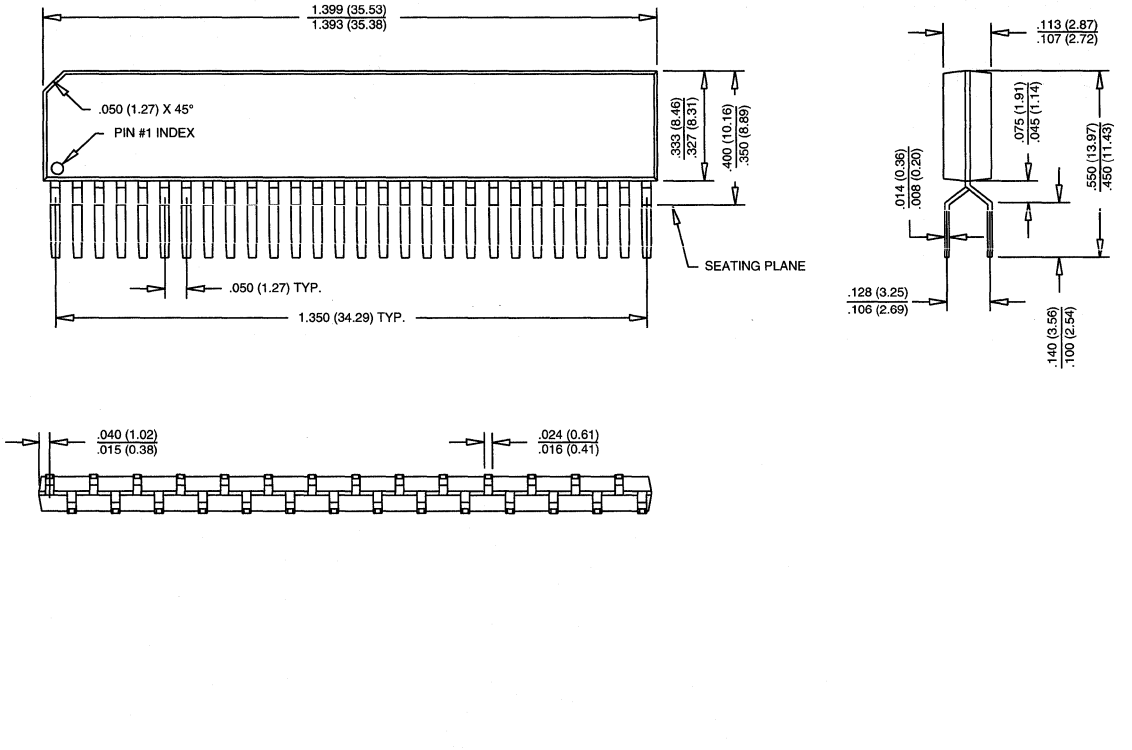
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on DRAM and VRAM products. Specific tests and temperatures are incorporated as applicable for specific products.

MICRON
SEMICONDUCTOR, INC.

28-PIN PLASTIC ZIP (375 mil)

SDA - 1

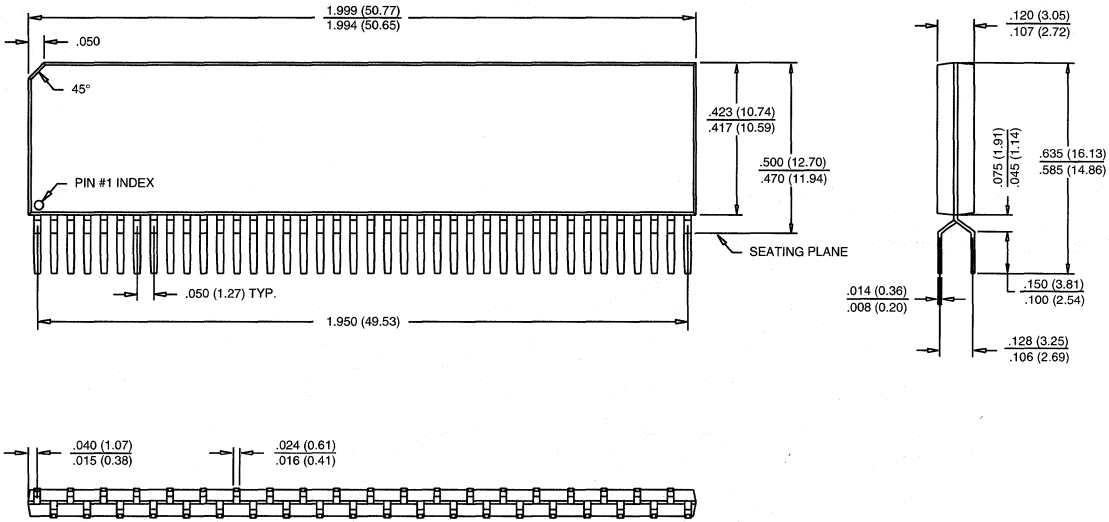


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

40-PIN PLASTIC ZIP (475 mil)

SDA - 2

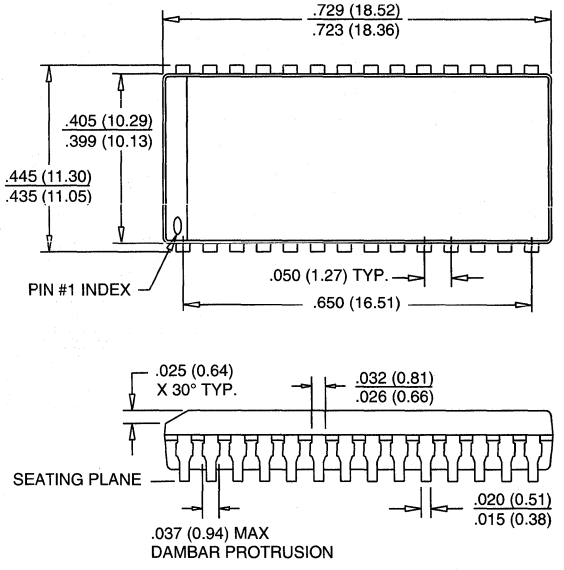


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ (400 mil)

SDB - 1

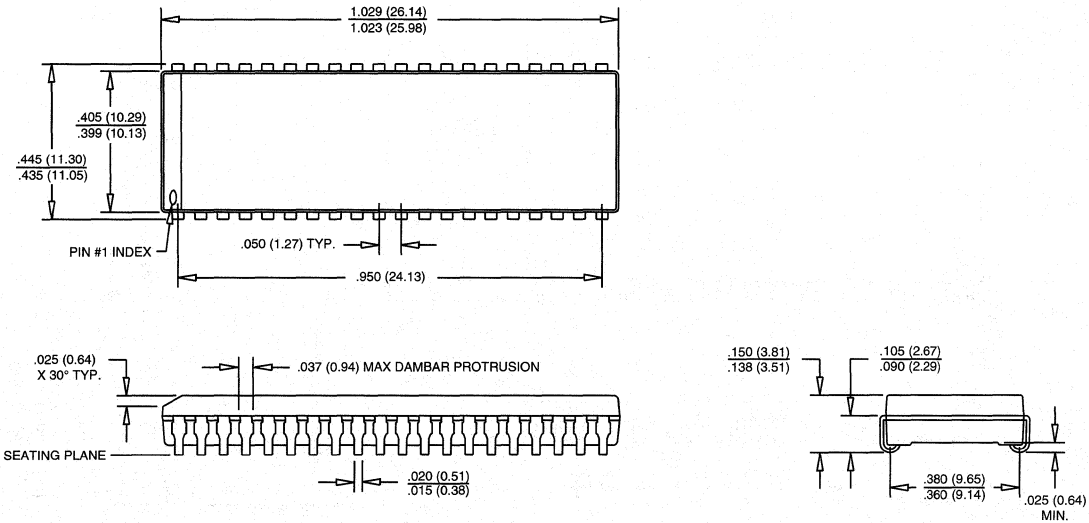


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

40-PIN PLASTIC SOJ (400 mil)

SDB - 2, 3

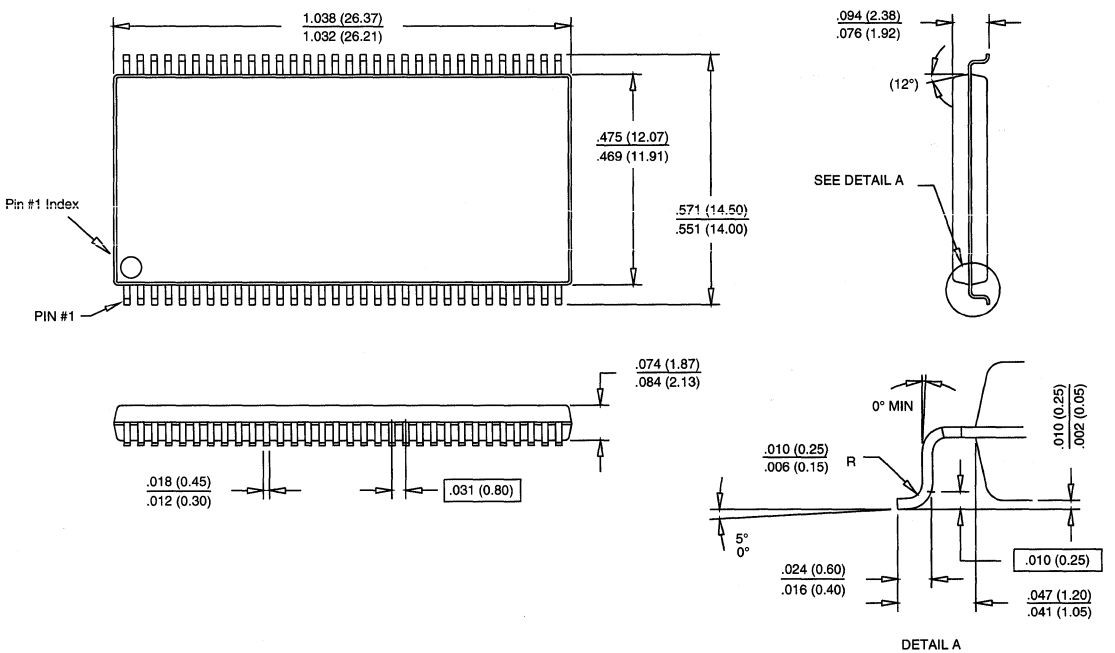


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

64-PIN PLASTIC SOP (12mm)

SDC - 1

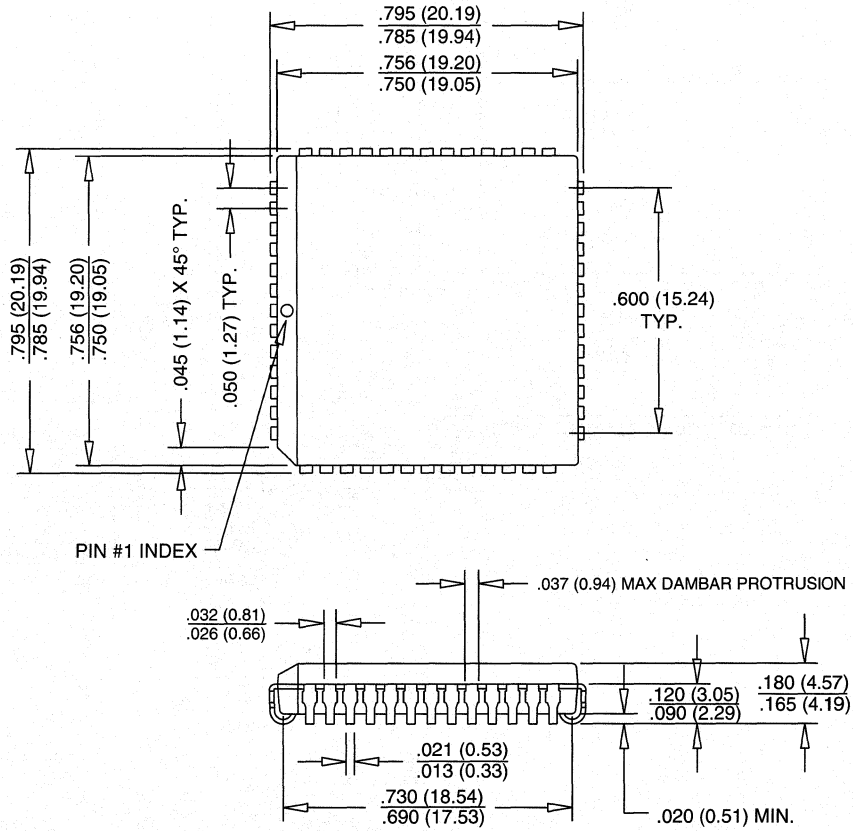


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PLASTIC PLCC

SDD - 1

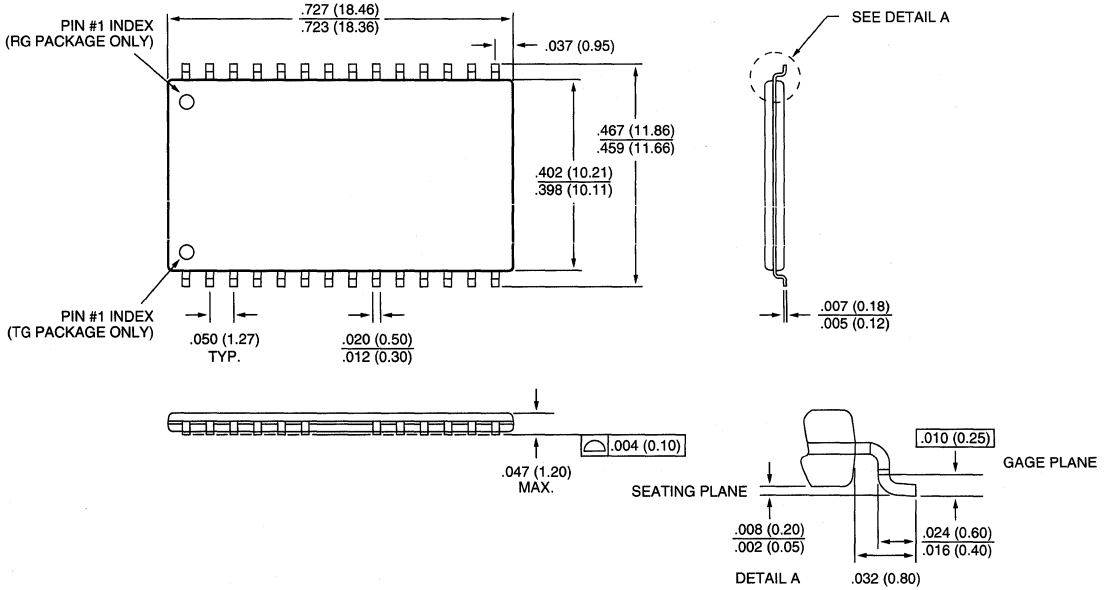


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC TSOP (400 mil)

SDE - 1

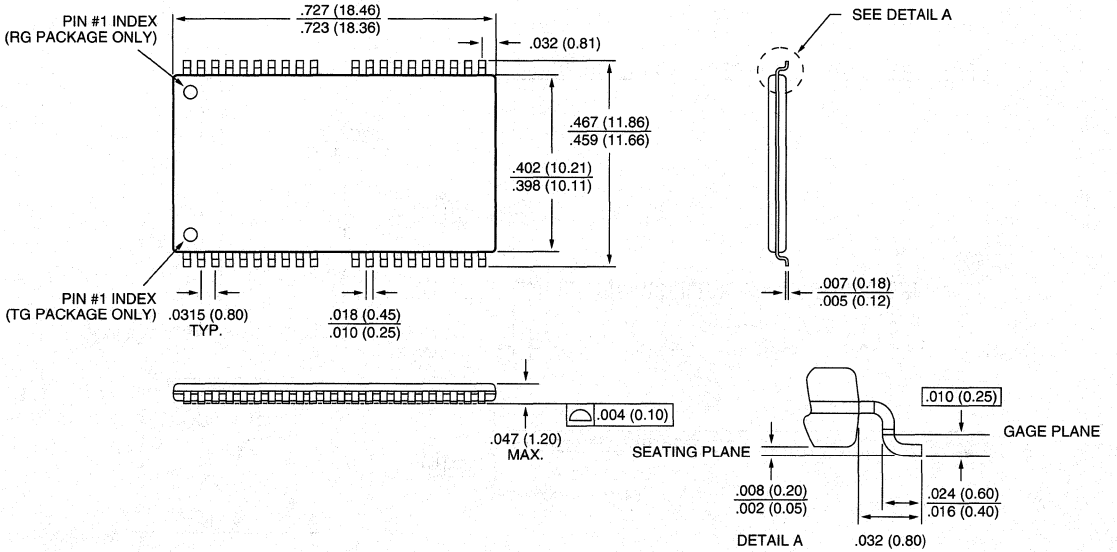


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

40/44-PIN PLASTIC TSOP (400 mil)

SDE - 2



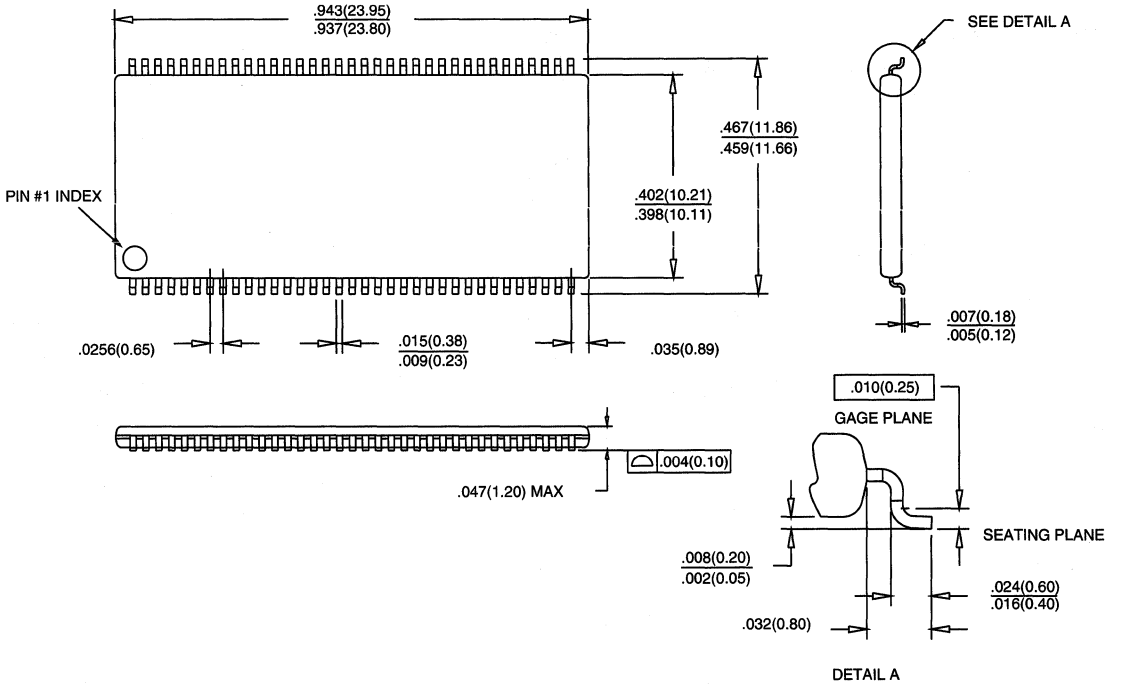
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

70-PIN PLASTIC TSOP (400 mil)

SDE - 4

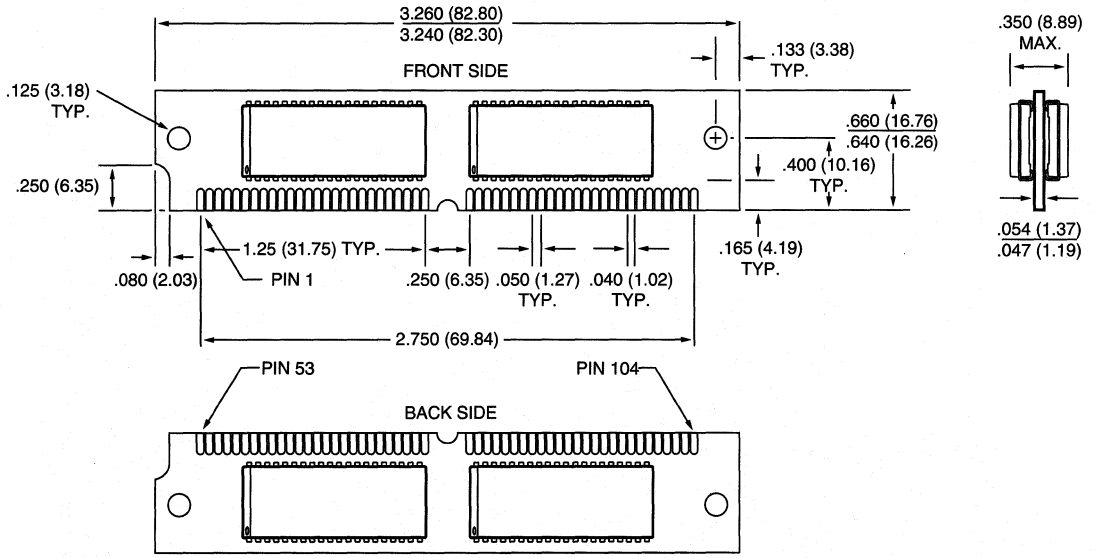


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

104-PIN MODULE SIMM

SDF - 1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON
SEMICONDUCTOR, INC.

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR-CODE LABELS

INTRODUCTION

On July 1, 1991, Micron implemented new standard bar-coding labels, which will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes have their own individual bar-code labels. The bar-code labels allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar-coding label.

BAR CODE INFORMATION

The information provided on the label is:

(4S) — Invoice/Packing Slip Number
(Q) — Quantity in master container
(Z) — Special: Individual box number and total number of boxes in the shipment (example: two of ten)
(K) — Trans ID: Customer purchase order number
(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address
Ship-From-Name: Micron name and address
Lot Date Code: Indicates date of oldest lot in the box
Human Readable: Master container package count
Package weight
Customer and supplier address

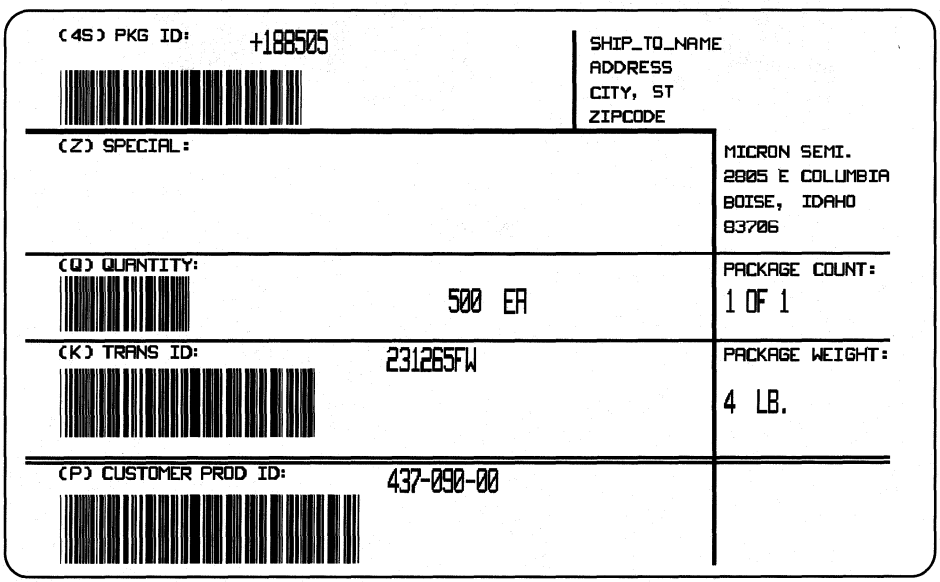


Figure 1
STANDARD BAR-CODE LABEL

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR-CODE LABELS

INTRODUCTION

Micron provides a standard bar-code label on each individual sample and tape-and-reel box. The standard bar-code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar-code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Micron part number/speed
Customer code/internal process code
Actual box number
Quantity/date code of oldest lot*
Country of origin code

Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCTS' SPC LABELS

INTRODUCTION

On November 15, 1991, Micron began providing a new SPC label on all surface-mount products. The label is attached to the static-proof bag for products packaged in tape-and-reel as well as tubes.

Figure 1 shows an example of the standard SPC label, while Figures 2 and 3 show the difference between the labels for tubed and tape-and-reel packaged products.

DATE INFORMATION

The SPC label includes the date on which the tube or reel was hermetically sealed in drypack. It also lists the ID number of the operator who sealed the product.

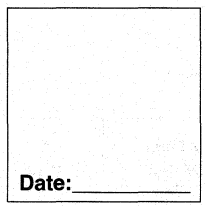


Figure 1
SURFACE-MOUNT PRODUCT SPC LABEL

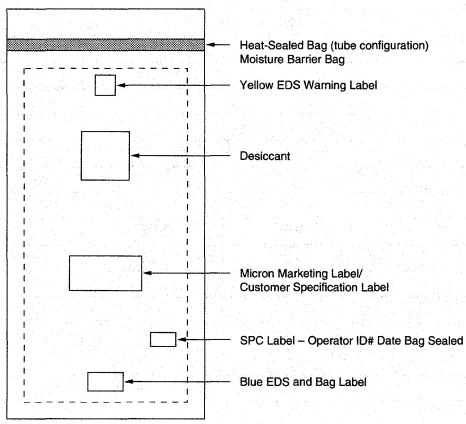


Figure 2
TUBED PRODUCT LABEL

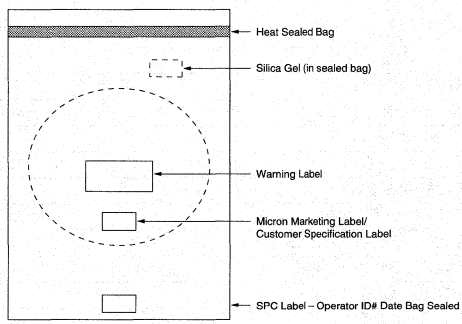


Figure 3
TAPE-AND-REEL PACKAGED PRODUCT LABEL

SALES INFORMATION

CUSTOMER SERVICE NOTE

BOX AND TAPE-AND-REEL QUANTITY AND WEIGHT CHART

INTRODUCTION

Micron encourages customers to place orders in increments of standard box, tray and reel quantities whenever possible. The chart below will help determine order quantities.

ADDITIONAL SALES INFORMATION

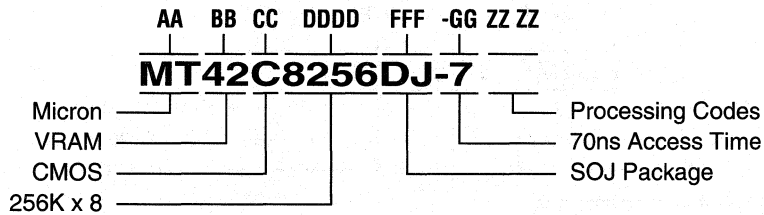
Benefits to Micron's customers by ordering in standard quantities:

1. Cost Savings—It is less expensive to send a shipment containing full boxes.
2. Process Control—Micron's production tracking system automatically checks speeds, revs, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity—Lot integrity is kept in tact when box quantities are not broken up.
4. Fewer returns—fewer errors → fewer complaints and returns.

Part Type	Quantity Per Tray	Quantity Per Box	LBS Per Box	Quantity Per Tube	Tape & Reel Quantity	LBS Per Reel
4 MEG SPECIALTY DRAMS						
*MT4C16256DJ		1500		15		
*MT4C16256Z		1000		10		
MT4C16257DJ		1500		15		
MT4C16257Z		1000		10		
MT4C16259DJ		1500		15		
MT4C16259Z		1000		10		
MT4C16260DJ		1500		15		
MT4C16261DJ		1500		15		
MT4C8512DJ		1500		15		
MT4C8512Z		1300		13		
MT4C8513DJ		1500		15		
MT4C8513Z		1300		13		
VRAM—1 MEG						
MT42C4256Z		1300	10.3	13		
MT42C 4256DJ		2000	10.3	25	500	3.5
MT42C 8128DJ		1500	11.9	15	500	3.5
VRAM—2 MEG						
MT42C8254DJ-8256DJ		1500	11.2	15	500	4.5
MT42C8254TG-8256TG	84	1000			500	
MT42C8254RG-8256RG	84	1000			500	
TRIPLE-PORT DRAM						
MT43C4257TG	84	1000				
MT43C4257RG	84	1000				
MT43C4257DJ, 4258DJ		1500	11.1	15	500	
MT43C8128EJ, 8129EJ		1500		15	500	

***Revised 3/12/93**

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
VRAM 42
TPDRAM 43
SRAM 5
FIFO 52
Cache Data SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low-Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM ..... Width, Density
VRAM ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
CACHE ..... Density, Width
Latched SRAM ..... Total Bits, Width
FIFO ..... Width, Total Bits
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG

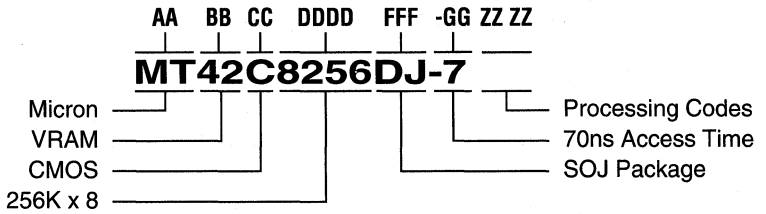
FFF – PACKAGE CODES (continued)

QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Skinny) ..... SJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL
DIE
Die ..... XDC
Wafer ..... XWC
Military Die ..... XD
Military Wafer ..... XW
Ceramic
DIP C
DIP (Narrow Body) ..... CN
DIP (Wide Body) ..... CW
LCC ..... EC
LCC (Narrow Body) ..... ECN
LCC (Wide Body) ..... ECW
SOP/SOIC ..... CG
SOJ ..... DCJ
PGA ..... CA
FLAT PACK ..... F

GG – ACCESS TIME

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: V L IT

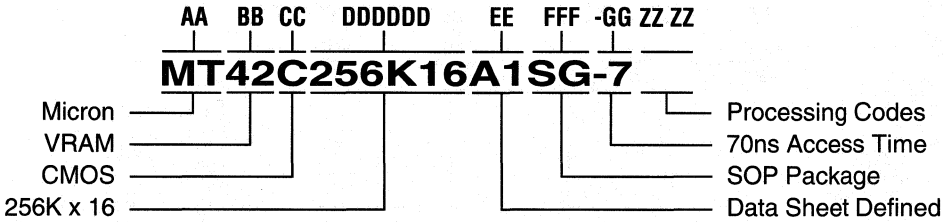
Interim	I
Low Voltage	V
DRAMS	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (SELF REFRESH)	S
Low Voltage, Low Power (SELF REFRESH)	VS
SRAMS	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP

ZZ ZZ – PROCESSING CODES (continued)

Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
VRAM 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
FIFO 52
Latched SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG

FFF – PACKAGE CODES (continued)

QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Skinny) ..... SJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

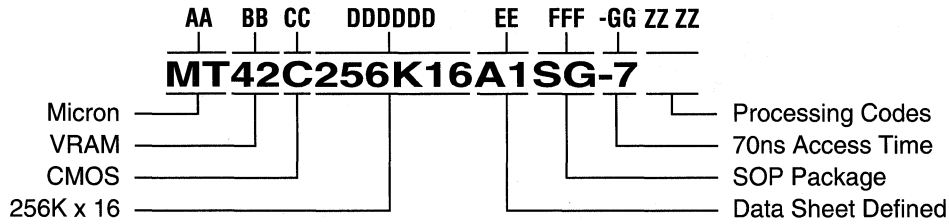
DIE
Die ..... XDC
Wafer ..... XWC
Military Die ..... XD
Military Wafer ..... XW

CERAMIC
DIP C
DIP (Narrow Body) ..... CN
DIP (Wide Body) ..... CW
LCC (Narrow Body) ..... ECN
LCC ..... EC
LCC (Wide Body) ..... ECW
SOP/SOIC ..... CG
SOJ ..... DCJ
PGA ..... CA
FLAT PACK ..... F

GG – ACCESS TIME

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

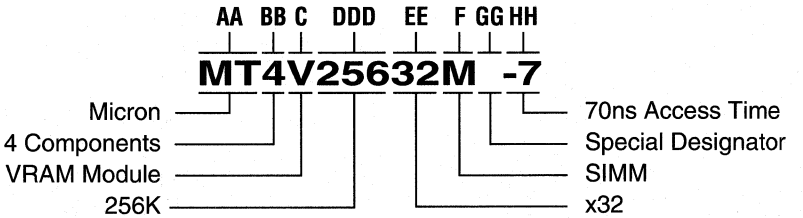
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (SELF REFRESH)	S
Low Voltage, Low Power (SELF REFRESH)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P

ZZ ZZ – PROCESSING CODES (continued)

Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D
- VRAM V

DDD – DEPTH

EE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- Gold Plate ..... G
- ZIP ..... Z
- SIP ..... N
- SIMM ..... M

GG – SPECIAL DESIGNATOR
- Low Power L

HH – ACCESS TIME
- -10 ..... 10ns or 100ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns
- -45 ..... 45ns
- -6 ..... 60ns
- -7 ..... 70ns
- -8 ..... 80ns

ORDER INFORMATION*

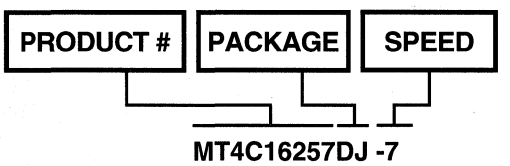
Each Micron component family is manufactured and quality controlled in the U.S.A. at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX® intelligent burn-in and test system.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributor nearest you. Micron's policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

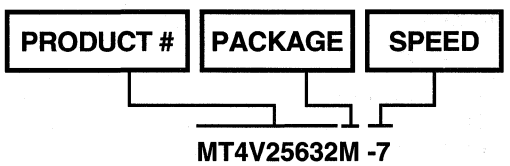
Telephone: (208) 368-3900
Fax: (208) 368-4431
Customer Comment Line:
(800) 932-4992 (U.S.A.)
01 (208) 368-3410 (Intl.)

ORDER EXAMPLES

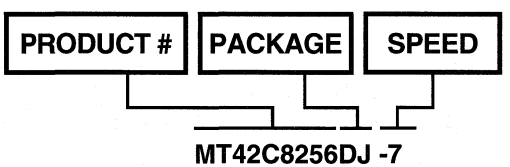
WIDE DRAM
256K x 16, 70ns in Plastic SOJ



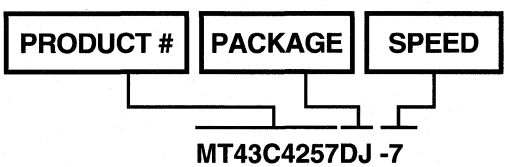
VRAM MODULE
256K x 32, 70ns in SIMM Module



VRAM
256K x 8, 70ns in Plastic SOJ



TRIPLE-PORT DRAM
256K x 4, 70ns in Plastic SOJ



*For more detailed information, refer to the product numbering charts on pages 9-5 through 9-10.

ALABAMA

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Fax - 205-534-2384

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Phone - 205-837-8700
Fax - 205-830-2565

Hamilton/Avnet Electronics
4960 Corporate Drive, Suite 135
Huntsville, AL 35805
Phone - 205-837-7211
Fax - 205-721-0356

Pioneer Technology
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Phone - 205-837-9300
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Fax - 602-820-7054

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Tempe, AZ 85281
Phone - 602-966-6600
Fax - 602-966-4826

Hamilton/Avnet Electronics
1626 South Edwards
Tempe, AZ 85281
Phone - 602-961-1211
Fax - 602-961-4555

Hall-Mark Electronics Corporation
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Fax - 602-437-2348

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