# MITSUBISHI SEMICONDUCTORS 1985

## IC MEMORIES

DATA BOOK

MITSUBISHI ELECTRIC

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## 3 NMOS STATIC RAM



## 4 CMOS STATIC RAM

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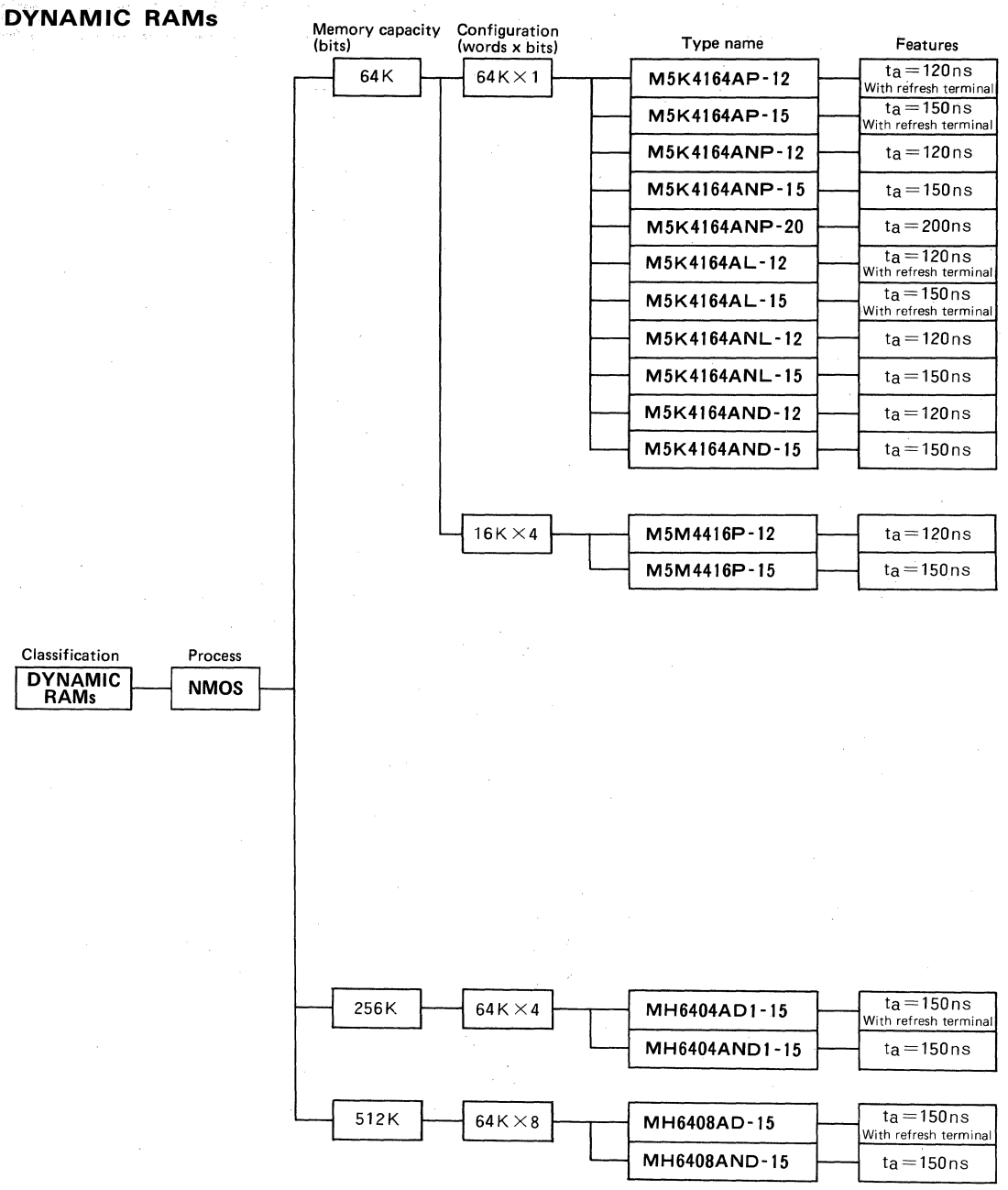
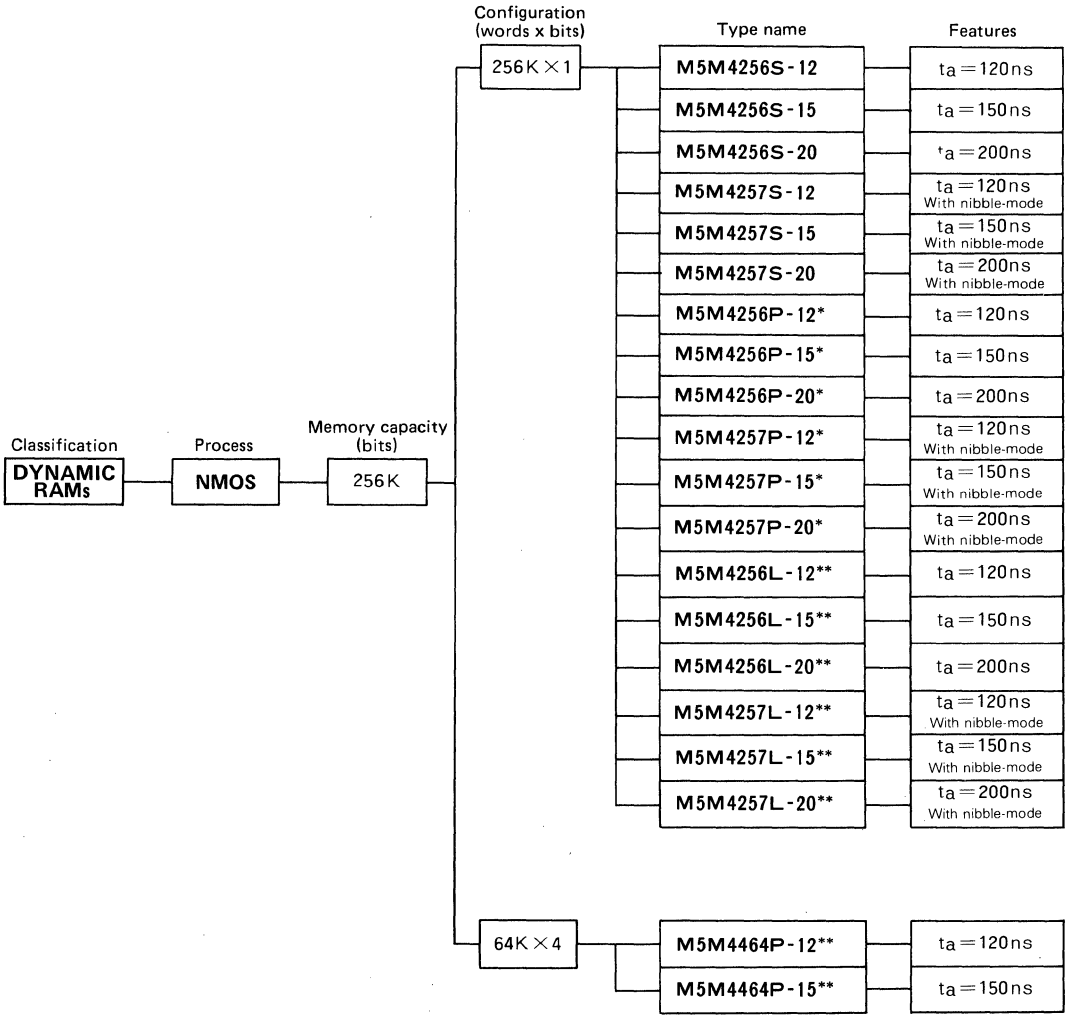
# GUIDANCE 1

## DYNAMIC RAMs



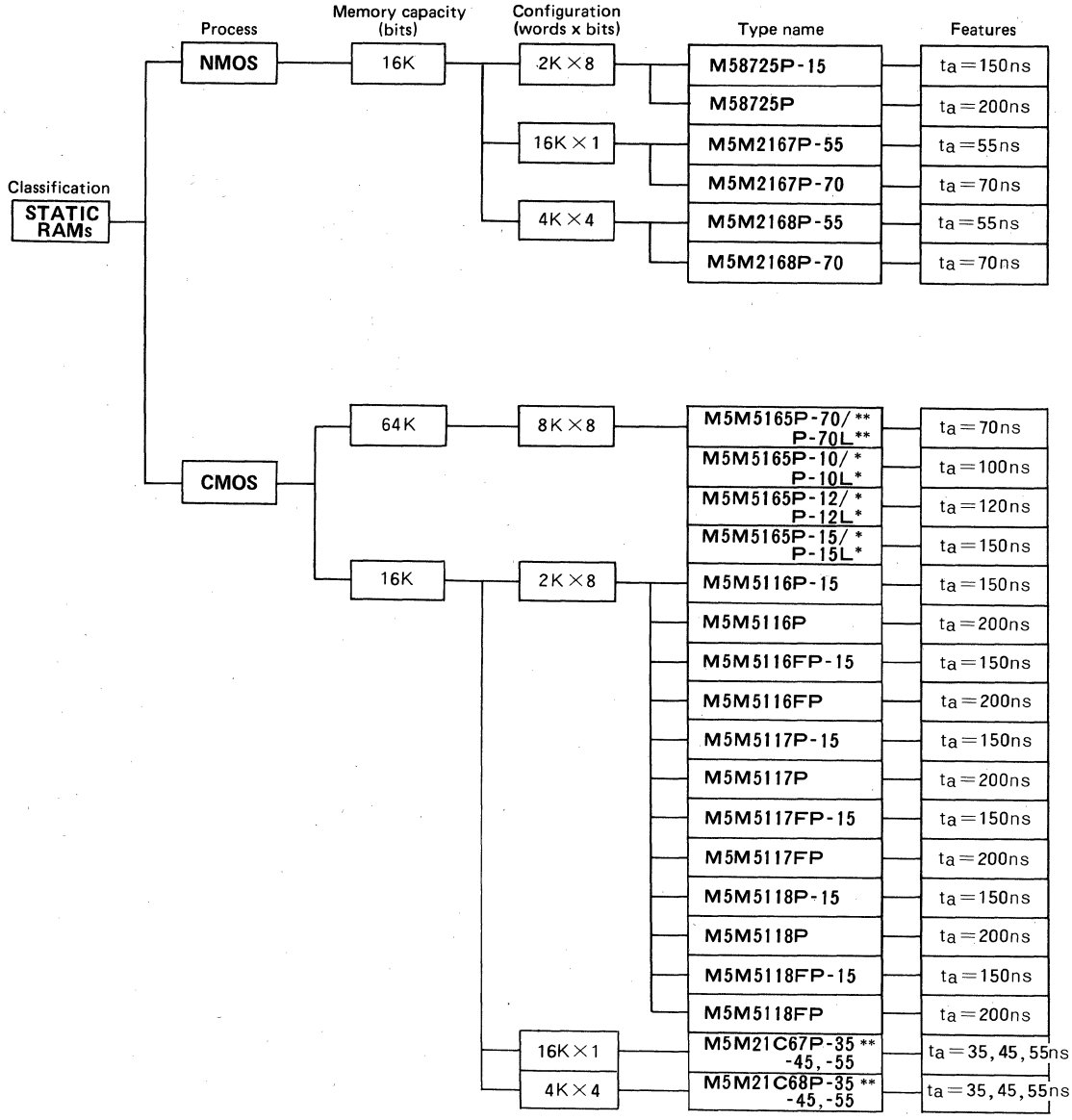
## DYNAMIC RAMs




* : New product ** : Under development

# GUIDE TO SELECTION OF IC MEMORIES

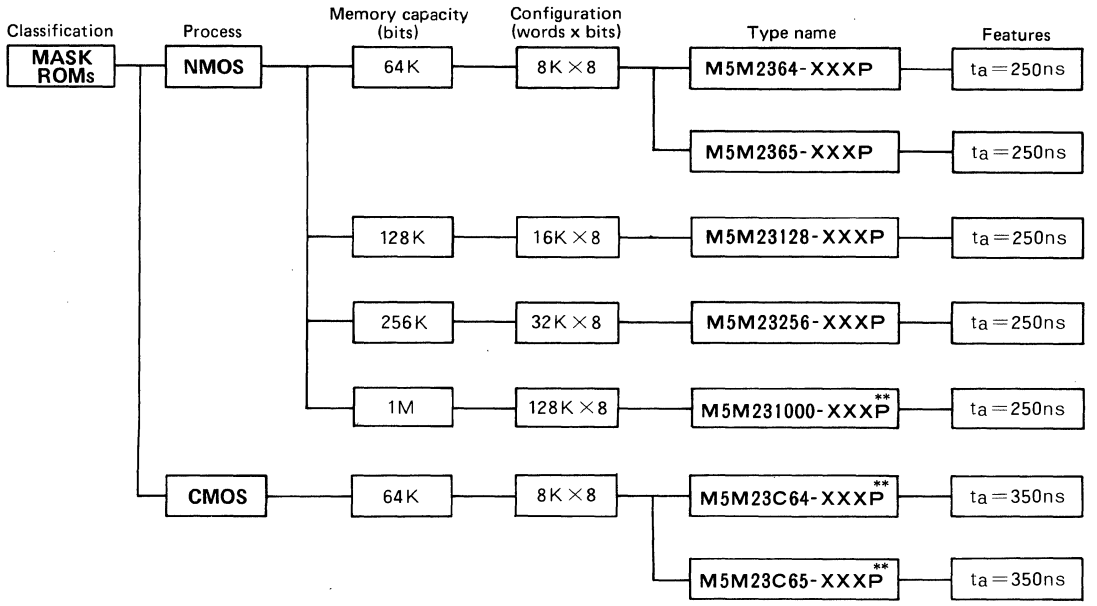
## STATIC RAMs




∗ : New product ∗∗ : Under development

# GUIDE TO SELECTION OF IC MEMORIES

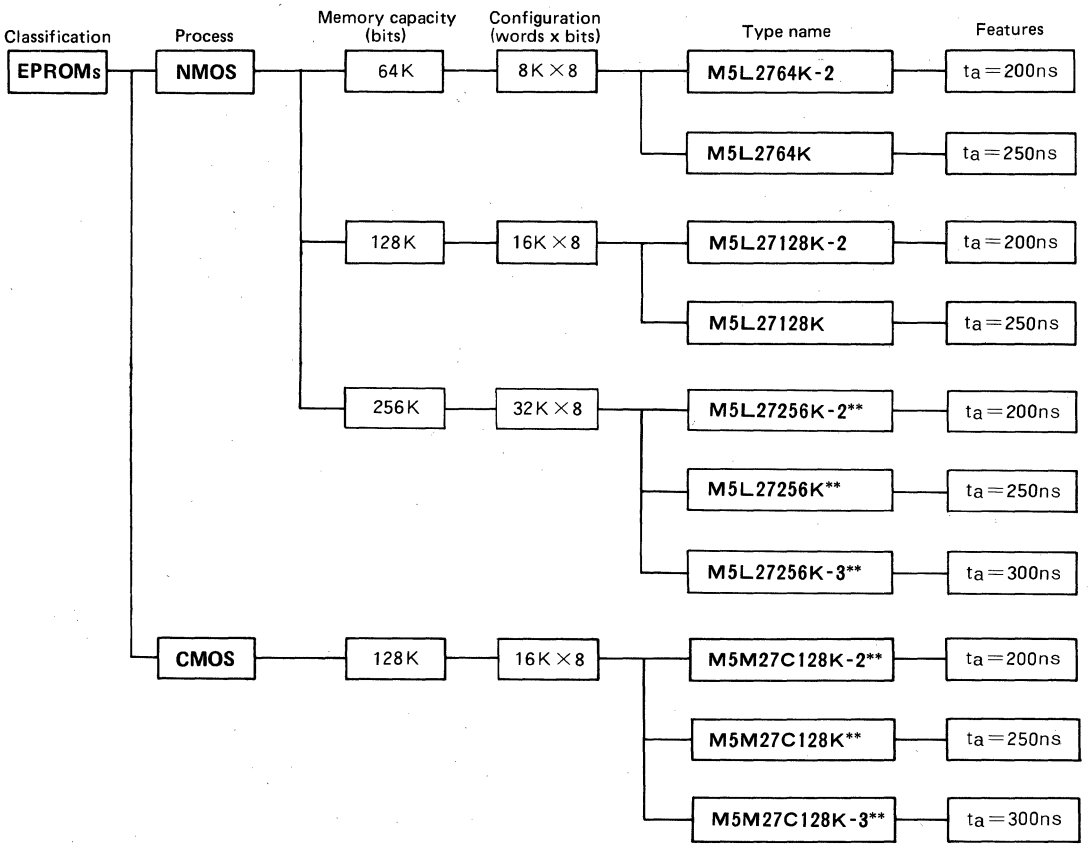
## MASK ROMs




**: Under development

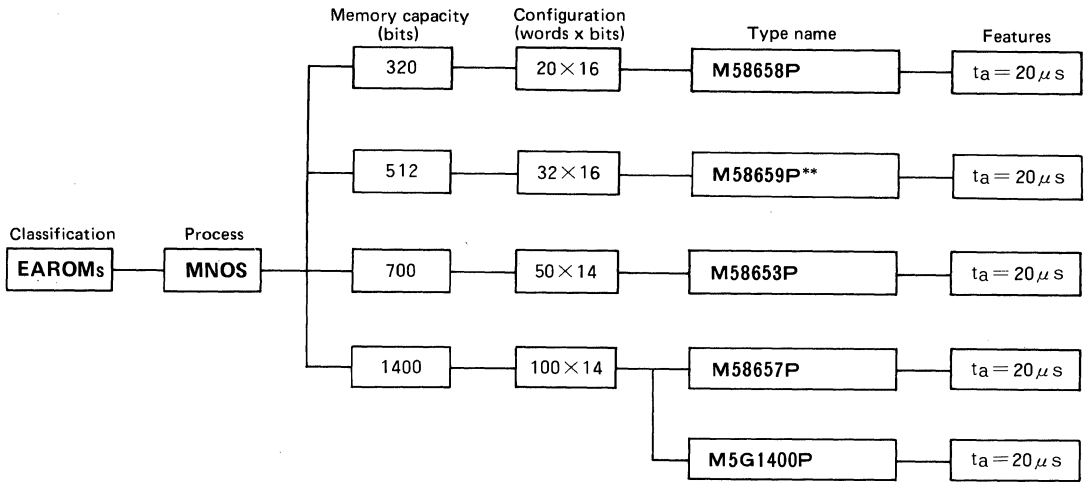
# GUIDE TO SELECTION OF IC MEMORIES

## MOS EPROMs




** : Under development

## MOS EAROMs




** : Under development

## ■64K-Bit DYNAMIC RAM

### DIL

| Type | Structure | Memory capacity (configuration) | Refresh pin | Access time Max (ns) | Cycle time Min (ns) | Power dissipation Typ (mW) | Low power dissipation Max(mW) Operating time | Specifications | Package outlines | Interchangeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **M5K4164AP-12** | NMOS | 64K (64K×1) | Yes | 120 | 220 | 175 | 275 | ●128 refresh cycles every 2ms<br>●1-pin automatic and self-refreshing capability<br>●$\overline{CAS}$ input allows hidden refresh, hidden automatic refresh, and hidden self-refresh operation. | 16P4 | See page 1-12 | 2—3 |
| **M5K4164AP-15** | | | | 150 | 260 | 150 | 250 | | 16P4 | | 2—3 |
| **M5K4164ANP-12** | | | No | 120 | 220 | 175 | 275 | ●128 refresh cycles every 2ms.<br>●$\overline{CAS}$ input allows hidden refresh operation | 16P4 | See page 1-12 | 2—14 |
| **M5K4164ANP-15** | | | | 150 | 260 | 150 | 250 | | | | |
| **M5K4164ANP-20** | | | | 200 | 330 | 125 | 225 | | | | 2—24 |
| **M5M4416P-12** | | 64K (16K×4) | | 120 | 220 | 175 | 275 | ●128 refresh cycles every 2ms<br>●4-bit configuration | 18P4 | | 2—65 |
| **M5M4416P-15** | | | | 150 | 260 | 150 | 250 | | | | |

### ZIL

| Type | Structure | Memory capacity (configuration | Refresh pin | Access time Max(ns) | Specifications | Package outlines | Interchangeable products | Page |
|---|---|---|---|---|---|---|---|---|
| **M5K4164AL-12** | NMOS | 64K (64K×1) | Yes | 120 | ●Same electrical characteristics as the M5K4164AP and ANP series.<br>●Package 16pin zig zag in-line<br>●5-pin automatic and self-refresh capability | 16P5A | — | 2—34 |
| **M5K4164AL-15** | | | | 150 | | | | |
| **M5K4164ANL-12** | | | No | 120 | ●Same electrical characteristics as the M5K4164AP and ANP series.<br>●Package: 16-pin zig-zag in-line | | — | 2—45 |
| **M5K4164ANL-15** | | | | 150 | | | | |

### Chip carrier

| Type | Structure | Memory capacity (configuration) | Refresh pin | Access time Max(ns) | Specifications | Package outlines | Interchangeable products | Page |
|---|---|---|---|---|---|---|---|---|
| **M5K4164AND-12** | NMOS | 64K (64K×1) | No | 120 | ●Same electrical characteristics as the M5K4164AP and ANP series<br>●Package: 18-pin of which two are open<br>●Lead pitch: 1.27mm<br>●External dimensions: 7.2×10.8×1.9mm | 18D0 | See page 1-12 | 2—55 |
| **M5K4164AND-15** | | | | 150 | | | | |

## SIL MODULE

| Type | Structure | Memory capacity (configuration) | Refresh pin | Access time Max(ns) | Number of chip carrier | Specifications | Package outlines | Interchangeable products | Page |
|---|---|---|---|---|---|---|---|---|---|
| **MH6404AD1-15** | NMOS | 256K (64K×4) | Yes | 150 | Four units (64K×4-bit) | ●Package: 22-pin SIL configuration<br>●External measurements: 7.6×56×3.5mm | 22S5 | — | 2—185 |
| **MH6408AD-15** | | 512K (64K×8) | | | Eight units (64K×8-bit) | ●Package: 30-pin SIL configuration<br>●External measurements: 8.4×76×7mm | 30S5 | — | 2—206 |
| **MH6404AND1-15** | | 256K (64K×4) | No | | Four units (64K×4-bit) | ●Package: 22-pin SIL configuration<br>●External measurements: 7.6×56×3.5mm | 22S5 | — | 2—196 |
| **MH6408AND-15** | | 512K (64K×8) | | | Eight units (64K×8-bit) | ●Package: 30-pin configuration<br>●External measurements: 8.4×76×7mm | 30S5 | — | 2—217 |

## ■256K-Bit DYNAMIC RAM

### DIL

| Type | Structure | Memory capacity (configuration) | Function mode | Access time Max(ns) | Cycle time Min(ns) | Power dissipation Typ (mW) | Low power dissipation Max(mW) Operating time | Specifications | Package outlines | Interchangeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **M5M4256P-12*** | NMOS | 256K (256K×1) | Page mode | 120 | 230 | 260 | 360 | ●256 refresh cycles every 4ms<br>●$\overline{CAS}$ before $\overline{RAS}$ refresh operation capability<br>●$\overline{CAS}$ input allows hidden refresh operation. | 16P4 | See page 1-12 | 2—80 |
| **M5M4256S-12** | | | | | | | 413 | | 16S1 | | 2—110 |
| **M5M4256P-15*** | | | | 150 | 260 | 230 | 330 | | 16P4 | | 2—80 |
| **M5M4256S-15** | | | | | | | 385 | | 16S1 | | 2—110 |
| **M5M4256P-20*** | | | | 200 | 330 | 190 | 275 | | 16P4 | | 2—80 |
| **M5M4256S-20** | | | | | | | 303 | | 16S1 | | 2—110 |
| **M5M4257P-12*** | | | Nibble mode | 120 | 230 | 260 | 360 | ●256 refresh cycles every 4ms.<br>●$\overline{CAS}$ before $\overline{RAS}$ refresh operation capability.<br>●$\overline{CAS}$ input allows hidden refresh operation | 16P4 | | 2—95 |
| **M5M4257S-12** | | | | | | | 413 | | 16S1 | | 2—125 |
| **M5M4257P-15*** | | | | 150 | 260 | 230 | 330 | | 16P4 | | 2—95 |
| **M5M4257S-15** | | | | | | | 385 | | 16S1 | | 2—125 |
| **M5M4257P-20*** | | | | 200 | 330 | 190 | 275 | | 16P4 | | 2—95 |
| **M5M4257S-20** | | | | | | | 303 | | 16S1 | | 2—125 |
| **M5M4464P-12**** | | 256K (64K×4) | Page mode | 120 | 230 | 260 | 360 | ●256 refresh cycles every 4ms.<br>●$\overline{CAS}$ before $\overline{RAS}$ refresh operation capability<br>●$\overline{CAS}$ input allows hidden refresh operation<br>●4-bit configuration | 18P4 | — | 2—170 |
| **M5M4464P-15**** | | | | 150 | 260 | 230 | 330 | | | | |

* : New product ** : Under development

## ZIL

| Type | Structure | Memory capacity (configu-ration) | Function mode | Access time Max(ns) | Cycle time Min(ns) | Power dissipation Typ (mW) | Low power dissipation Max(mW) Operating time | Specifications | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M5M4256L-12** | NMOS | 256K (256K×1) | Page mode | 120 | 230 | 260 | 360 | ●Same electrical characteristics as the M5M4256P and M5M4257P series. ●Package 16-pin zig-zag in line. | 16P5A | — | 2—140 |
| M5M4256L-15** | | | | 150 | 260 | 230 | 330 | | | | |
| M5M4256L-20** | | | | 200 | 330 | 190 | 275 | | | | |
| M5M4257L-12** | | | Nibble mode | 120 | 230 | 260 | 360 | | | | 2—155 |
| M5M4257L-15** | | | | 150 | 260 | 230 | 330 | | | | |
| M5M4257L-20** | | | | 200 | 330 | 190 | 275 | | | | |

## ■16K-Bit STATIC RAM

| Type | Structure | Memory capacity | Memory configuration (Word×Bit) | Supply voltage (V) | Typical power dissipation Typ(mW) | Access time Max(ns) | Cycle time Min(ns) | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| M58725P-15 | NMOS | 16K | 2K×8 | 5±10% | 250 | 150 | 150 | 24P4 | See page 1-14 | 3—3 |
| M58725P | | | | | | 200 | 200 | | | |
| M5M2167P-55 | | | 16K×1 | | 400 | 55 | 55 | 20P4 | | 3—9 |
| M5M2167P-70 | | | | | | 70 | 70 | | | |
| M5M2168P-55 | | | 4K×4 | | 500 | 55 | 55 | 20P4 | | 3—13 |
| M5M2168P-70 | | | | | | 70 | 70 | | | |
| M5M5116P-15 | CMOS | | 2K×8 | | 150 | 150 | 150 | 24P4 | See page 1-14 | 4—3 |
| M5M5116P | | | | | | 200 | 200 | | | |
| M5M5116FP-15 | | | | | | 150 | 150 | 24P2W | — | 4—8 |
| M5M5116FP | | | | | | 200 | 200 | | See page 1-14 | |
| M5M5117P-15 | | | | | | 150 | 150 | 24P4 | | 4—13 |
| M5M5117P | | | | | | 200 | 200 | | | |
| M5M5117FP-15 | | | | | | 150 | 150 | 24P2W | | 4—18 |
| M5M5117FP | | | | | | 200 | 200 | | | |
| M5M5118P-15 | | | | | | 150 | 150 | 24P4 | | 4—23 |
| M5M5118P | | | | | | 200 | 200 | | | |
| M5M5118FP-15 | | | | | | 150 | 150 | 24P2W | | 4—28 |
| M5M5118FP | | | | | | 200 | 200 | | | |
| M5M21C67P-35** | | | 16K×1 | | 200 | 35 | 35 | 20P4 | — | — |
| M5M21C67P-45** | | | | | | 45 | 45 | | | |
| M5M21C67P-55** | | | | | | 55 | 55 | | | |
| M5M21C68P-35** | | | 4K×4 | | | 35 | 35 | 20P4 | — | — |
| M5M21C68P-45** | | | | | | 45 | 45 | | | |
| M5M21C68P-55** | | | | | | 55 | 55 | | | |

## ■64K-Bit STATIC RAM

| Type | Structure | Memory capacity | Memory configuration (Word×Bit) | Supply voltage (V) | Power dissipation Operating Typ(mW) | Power dissipation Standby Max(mW) | Access time Max(ns) | Cycle time Max(ns) | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M5M5165P-70** | CMOS | 64K | 8K×8 | 5±10% | 150 | 11 | 70 | 70 | 28P4 | — | 4—33 |
| M5M5165P-10* | | | | | | | 100 | 100 | | See page 1-14 | |
| M5M5165P-12* | | | | | | | 120 | 120 | | | |
| M5M5165P-15* | | | | | | | 150 | 150 | | | |
| M5M5165P-70L** | | | | | | 0.55 | 70 | 70 | | — | |
| M5M5165P-10L* | | | | | | | 100 | 100 | | See page 1-14 | |
| M5M5165P-12L* | | | | | | | 120 | 120 | | | |
| M5M5165P-15L* | | | | | | | 150 | 150 | | | |

* : New product ** : Under development



MITSUBISHI ELECTRIC

## ■MASK ROM

| Type | Structure | Memory capacity | Memory configuration (Word×Bit) | Supply voltage (V) | Typical power dissipation Typ(mW) | Access time Max(ns) | Cycle time Min(ns) | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| **M5M2364-XXXP** | NMOS | 64K | 8K×8 | 5±10% | 200 | 250 | — | 28P4 | MK37000 | 5—3 |
| **M5M2365-XXXP** | | | | | 150 | 250 | — | 24P4 | MK36000 | 5—7 |
| **M5M23128-XXXP** | | 128K | 16K×8 | | 200 | | — | 28P4 | μPD23128 | 5—16 |
| **M5M23256-XXXP** | | 256K | 32K×8 | | | | — | | MK38000 | 5—19 |
| **M5M231000-XXXP**** | | 1M | 128K×8 | | | | — | | — | 5—22 |
| **M5M23C64-XXXP**** | CMOS | 64K | 8K×8 | | 100 | 350 | — | | — | 5—10 |
| **M5M23C65-XXXP**** | | | | | | 350 | — | 24P4 | — | 5—13 |

## ■EPROM

| Type | Structure | Memory capacity | Memory configuration (Word×Bit) | Supply voltage (V) | Typical power dissipation (mW) | Access time Max(ns) | Type of output | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| **M5L2764K-2** | NMOS | 64K | 8K×8 | 5±5% | 300 | 200 | — | 28K1 | See page1-16 | 6—3 |
| **M5L2764K** | | | | | | 250 | — | | | |
| **M5L27128K-2** | | 128K | 16K×8 | | 350 | 200 | — | 28K4 | — | 6—10 |
| **M5L27128K** | | | | | | 250 | — | | See page1-16 | |
| **M5M27C128K-2**** | CMOS | | | | 160 | 200 | — | | | 6—19 |
| **M5M27C128K**** | | | | | | 250 | — | | | |
| **M5M27C128K-3**** | | | | | | 300 | — | | | |
| **M5L27256K-2**** | NMOS | 256K | 32K×8 | | 300 | 200 | — | | | — |
| **M5L27256K**** | | | | | | 250 | — | | i27256 | |
| **M5L27256K-3**** | | | | | | 300 | — | | i27256-3 | |

## ■EAROM

| Type | Structure | Memory capacity | Memory configuration (Word×Bit) | Supply voltage (V) | Typical power dissipation (mW) | Access time Max(ns) | Cycle time Min(ns) | Package outlines | Inter-changeable products | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| **M58658P** | MNOS | 320 | 20×16 | ※1 | 200 | 20μs | — | 14P4 | — | 7—15 |
| **M58659P**** | | 512 | 32×16 | ※1 | | | — | | — | — |
| **M58653P** | | 700 | 50×14 | ※1 | | | — | | — | 7—3 |
| **M58657P** | | 1400 | 100×14 | ※1 | | | — | | — | 7—9 |
| **M5G1400P** | | | | ※2 | | | — | | ER1400 | 7—23 |

※1 $V_{GG}-V_{SS}=-35V\pm8\%$ $V_{SS}-V_{GND}=5V^{+20\%}_{-5\%}$
※2 $V_{GG}-V_{SS}=-35V\pm8\%$
** : Under development

# GUIDE TO INTERCHANGEABILITY

| | Mitsubishi Electric | AMD Advanced Micro Devices | G I General Instrument | FSC Fairchild Semiconductor | Fujitsu | Hitachi | INTEL Intel | INTERSIL Intersil |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC RAM | **M5K4116P-2** | Am9016F | | | MB8116H | HM4716A-2 | 2117-2 | |
| | **M5K4116P-3** | Am9016E | | | MB8116E | HM4716A-3 | 2117-3 | |
| | **M5K4164AP-12** | | | | MB8265A-12 | HM4865AP-12 | | |
| | **M5K4164AL-12** | | | | | | | |
| | **M5K4164AP-15** | | | | MB8265A-15 | HM4865AP-15 | | |
| | **M5K4164AL-15** | | | | | | | |
| | **M5K4164ANP-12** | | | | MB8264A-12 | HM4864AP-12 | | |
| | **M5K4164ANP-15** | | | | MB8264A-15 | HM4864AP-15 | | |
| | **M5K4164ANP-20** | | | | | | | |
| | **M5K4164ANL-12** | | | | | | | |
| | **M5K4164ANL-15** | | | | | | | |
| | **M5K4164AND-12** | | | | | | | |
| | **M5K4164AND-15** | | | | | HM4864CC-2 | | |
| | **MH6404AD1-15** | | | | | | | |
| | **MH6408AD-15** | | | | | | | |
| | **MH6404AND1-15** | | | | | | | |
| | **MH6408AND-15** | | | | | | | |
| | **M5M4416P-12** | | | | MB81416-12 | | | |
| | **M5M4416P-15** | | | | MB81416-15 | | | |
| | **M5M4256S-12** | | | | MB81256-12 | HM50256-12 | | |
| | **M5M4256S-15** | | | | MB81256-15 | HM50256-15 | | |
| | **M5M4256S-20** | | | | | HM50256-20 | | |
| | **M5M4257S-12** | | | | MB81257-12 | HM50257-12 | | |
| | **M5M4257S-15** | | | | MB81257-15 | HM50257-15 | | |
| | **M5M4257S-20** | | | | | HM50257-20 | | |
| | **M5M4256P-12** | | | | MB81256-12 | HM50256-12 | | |
| | **M5M4256P-15** | | | | MB81256-15 | HM50256-15 | | |
| | **M5M4256P-20** | | | | | HM50256-20 | | |
| | **M5M4257P-12** | | | | MB81257-12 | HM50257-12 | | |
| | **M5M4257P-15** | | | | MB81257-15 | HM50257-15 | | |
| | **M5M4257P-20** | | | | | HM50257-20 | | |
| | **M5M4256L-12** | | | | | | | |
| | **M5M4256L-15** | | | | | | | |
| | **M5M4256L-20** | | | | | | | |
| | **M5M4257L-12** | | | | | | | |
| | **M5M4257L-15** | | | | | | | |
| | **M5M4257L-20** | | | | | | | |
| | **M5M4464P-12** | | | | | | | |
| | **M5M4464P-15** | | | | | | | |

| MOSTEK Mostek | MOTOROLA Motorola Semiconductor products | NSC National Semiconductor | Nippon Electric | Oki | TI Texas Instruments | Toshiba | Remarks |
|---|---|---|---|---|---|---|---|
| MK4116-2 | MCM4116-15 | MM5290-2 | μPD416-3 | | TMS4116-15 | TMM416P-2 | |
| MK4116-3 | MCM4116-20 | MM5290-3 | μPD416-2 | | TMS4116-20 | TMM416P-3 | |
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| MK4164N-15 | | | | | | | |
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| | | | μPD4164C-12 | | | | |
| MK4564N-15 | | | μPD4164C-15 | | TMS4164-15NLJ | TMM4164P-3 | |
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| | | | | | TMS4416-15 | | |
| MK4556-12 | | | | MSM41256-12 | | TMM41256C-12 | |
| MK4556-15 | | | μPD41256C/D-15 | MSM41256-15 | | TMM41256C-15 | |
| MK4556-20 | | | μPD41256C/D-20 | MSM41256-20 | | | |
| | MCM6257-12 | | | MSM41257-12 | | | |
| | MCM6257-15 | | μPD41257C/D-15 | MSM41257-15 | | | |
| | | | μPD41257C/D-20 | MSM41257-20 | | | |
| MK4556-12 | | | | MSM41256-12 | | TMM41256C-12 | |
| MK4556-15 | | | μPD41256C/D-15 | MSM41256-15 | | TMM41256C-15 | |
| | | | μPD41256C/D-20 | MSM41256-20 | | | |
| | MCM6257-12 | | | MSM41257-12 | | | |
| | MCM6257-15 | | μPD41257C/D-15 | MSM41257-15 | | | |
| | | | μPD41257C/D-20 | MSM41257-20 | | | |
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# GUIDE TO INTERCHANGEABILITY

| | Mitsubishi Electric | AMD Advanced Micro Devices | AMI American Microsystems | FSC Fairchild Semiconductor | Fujitsu | Hitachi | INTEL Intel | INTERSIL Intersil |
|---|---|---|---|---|---|---|---|---|
| STATIC RAM | **M58725P-15** | | | | MB8128-15 | | | |
| | **M58725P** | | | | | | | |
| | **M5M2167P-55** | Am2167-55 | | | MB8167A-55 | HM6167H-55 | i2167-55 | |
| | **M5M2167P-70** | Am2167-70 | | | MB8167A-70 | HM6167H-70 | i2167-70 | |
| | **M5M2168P-55** | | | | MB8168-55 | HM6168H-55 | | |
| | **M5M2168P-70** | | | | MB8168-70 | HM6168H-70 | | |
| | **M5M5116P-15** | | | | MB8417-15 | | | |
| | **M5M5116P** | | | | MB8417-20 | | | |
| | **M5M5116FP-15** | | | | | | | |
| | **M5M5116FP** | | | | | | | |
| | **M5M5117P-15** | | | | MB8416-15 | HM6116L-3 | | |
| | **M5M5117P** | | | | MB8416-20 | HM6116L-4 | | |
| | **M5M5117FP-15** | | | | | HM6116LFP-3 | | |
| | **M5M5117FP** | | | | | HM6116LFP-4 | | |
| | **M5M5118P-15** | | | | | HM6117LP-3 | | |
| | **M5M5118P** | | | | MB8418-20 | HM6117LP-4 | | |
| | **M5M5118FP-15** | | | | | HM6117LFP-3 | | |
| | **M5M5118FP** | | | | | HM6117LFP-4 | | |
| | **M5M5165P-70 /P-70L** | | | | | | | |
| | **M5M5165P-10 /P-10L** | | | | | HM6264P-10 /LP-10 | | |
| | **M5M5165P-12 /P-12L** | | | | MB8464-12 /-12L | HM6264P-12 /LP-12 | | |
| | **M5M5165P-15 /P-15L** | | | | MB8464-15 /-15L | HM6264P-15 /LP-15 | | |

| | Mitsubishi Electric | AMD Advanced Micro Devices | AMI American Microsystems | FSC Fairchild Semiconductor | Fujitsu | Hitachi | INTEL Intel | INTERSIL Intersil |
|---|---|---|---|---|---|---|---|---|
| MASK ROM | **M5M2364-XXXP** | | | | | | | |
| | **M5M23C64-XXXP** | | | | | | | |
| | **M5M2365-XXXP** | | | | | | | |
| | **M5M23C65-XXXP** | | | | | | | |
| | **M5M23128-XXXP** | | | | | | | |
| | **M5M23256-XXXP** | | | | | | | |
| | **M5M231000-XXXP** | | | | | | | |

| MOSTEK Mostek | MOTOROLA Motorola Semiconductor products | NSC National Semiconductor | Nippon Electric | Oki | TI Texas Instruments | Toshiba | Remarks |
|---|---|---|---|---|---|---|---|
| | | | μPD4016C-3 | MSM2128-15 | | TMM2016P | |
| | | | μPD4016C-2 | MSM2128-20 | | TMM2016P-2 | |
| | | | μPD2167D-3 | | | | |
| | | | μPD2167D-2 | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | μPD447C-3 | MSM5127-15RS | | | |
| | | | μPD447C-2 | MSM5127-20RS | | TC5516AP | |
| | | | | | | | |
| | | | | | | TC5516AFP | |
| | | | μPD446C-3 | MSM5128-15RS | | | |
| | | | μPD446C-2 | MSM5128-20RS | | TC5517AP | |
| | | | | | | | |
| | | | | | | TC5517AFP | |
| | | | μPD449C-3 | MSM5129-15RS | | | |
| | | | μPD449C-2 | MSM5129-20RS | | TC5518BP | |
| | | | | | | | |
| | | | | | | TC5518BF | |
| | | | | | | | |
| | | | | | | | |
| | | | | MSM5165-12RS | | TC5565P-12 /PL-12 | |
| | | | μPD4364C-15/ C-15L(150ns) μPD4364C-20/ C-20L(200ns) | MSM5165-15RS | | TC5565P-15 /PL-15 | |

| MOSTEK Mostek | MOTOROLA Motorola Semiconductor products | NSC National Semiconductor | Nippon Electric | Oki | TI Texas Instruments | Toshiba | Remarks |
|---|---|---|---|---|---|---|---|
| MK37000 | | | | | | | |
| | | | | | | | |
| MK36000 | | | | | | | 24pin |
| | | | | | | | |
| | | | μPD23128 | | | | |
| MK38000 | | | | | | | |
| | | | | | | | 28pin |

| | Mitsubishi Electric | AMD Advanced Micro Devices | AMI American Microsystems | FSC Fairchild Semiconductor | Fujitsu | Hitachi | INTEL Intel | INTERSIL Intersil |
|---|---|---|---|---|---|---|---|---|
| EPROM | **M5L2764K-2** | | | | MBM2764-20 | | D2764-2 | |
| | **M5L2764K** | | | | MBM2764-25 | HN482764G | D2764 | |
| | **M5L27128K-2** | | | | | | | |
| | **M5L27128K** | Am27128-25 | | | MBM27128-25 | HN4827128-25 | D27128 | |
| | **M5M27C128K-2** | | | | | | | |
| | **M5M27C128K** | | | | MBM27C128-25 | | D27128 | |
| | **M5M27C128K-3** | | | | MBM27C128-30 | | | |
| | **M5L27256K-2** | | | | | | | |
| | **M5L27256K** | | | | | | D27256 | |
| | **M5L27256K-3** | | | | | | D27256-3 | |

| | Mitsubishi Electric | AMD Advanced Micro Devices | AMI American Microsystems | FSC Fairchild Semiconductor | Fujitsu | Hitachi | INTEL Intel | INTERSIL Intersil |
|---|---|---|---|---|---|---|---|---|
| EAROM | **M58653P** | | | | | | | |
| | **M58657P** | | | | | | | |
| | **M5G1400P** | | | | | | | |
| | **M58658P** | | | | | | | |
| | **M58659P** | | | | | | | |

| MOSTEK Mostek | MOTOROLA Motorola Semiconductor products | NSC National Semiconductor | Nippon Electric | Oki | TI Texas Instruments | Toshiba | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | | | TMM2764D-2 | |
| MK2764-8 | | | μPD2764D | MSM2764AS | | TMM2764D | |
| | | | μPD27128D-2 | | | TMM27128D-20 | |
| | | | μPD27128D | | | TMM27128D-25 | |
| | | | | | | | |
| | | | | | | | |
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| | | | | | | | |

| MOSTEK Mostek | MOTOROLA Motorola Semiconductor products | NSC National Semiconductor | Nippon Electric | Oki | TI Texas Instruments | Toshiba | GI General Instrument |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | ER1400 |
| | | | | | | | |
| | | | | | | | |

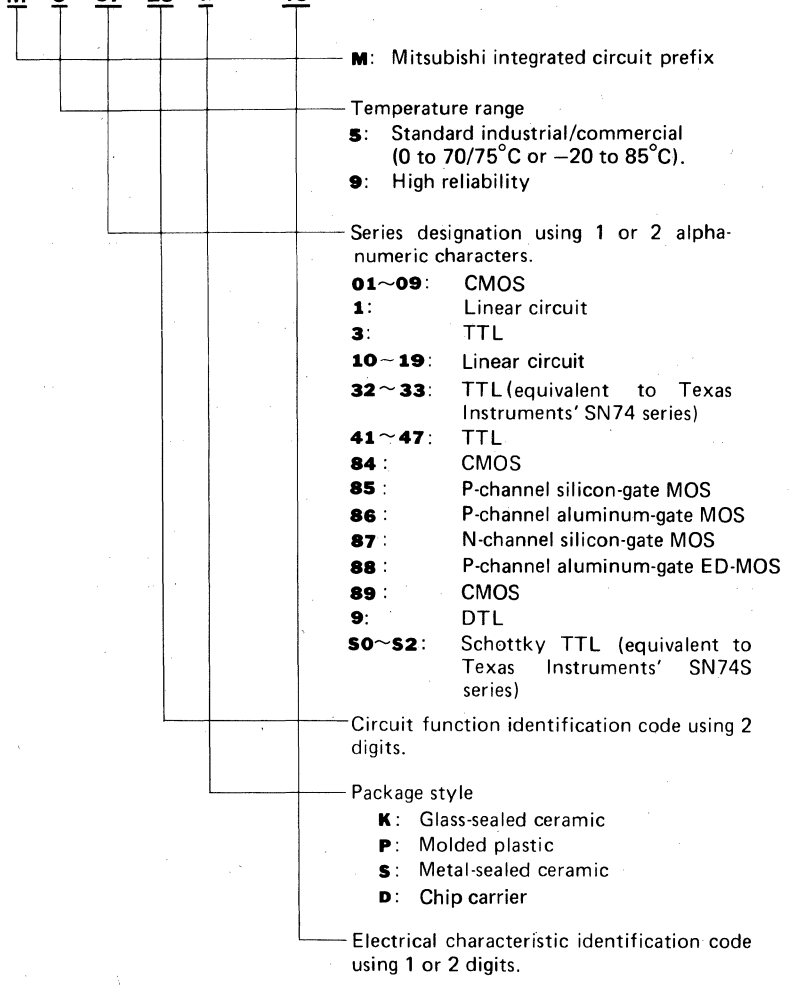
# ORDERING INFORMATION

## FUNCTION CODE

Mitsubishi integrated circuits may be ordered using the following simplified alphanumeric type-codes which define the function of the ICs and the package style.

### For Mitsubishi Original Products

Example: M 5 87 25 P – 15



**M**: Mitsubishi integrated circuit prefix

Temperature range
- **5**: Standard industrial/commercial (0 to 70/75°C or −20 to 85°C).
- **9**: High reliability

Series designation using 1 or 2 alpha-numeric characters.
- **01~09**: CMOS
- **1**: Linear circuit
- **3**: TTL
- **10~19**: Linear circuit
- **32~33**: TTL (equivalent to Texas Instruments' SN74 series)
- **41~47**: TTL
- **84**: CMOS
- **85**: P-channel silicon-gate MOS
- **86**: P-channel aluminum-gate MOS
- **87**: N-channel silicon-gate MOS
- **88**: P-channel aluminum-gate ED-MOS
- **89**: CMOS
- **9**: DTL
- **S0~S2**: Schottky TTL (equivalent to Texas Instruments' SN74S series)

Circuit function identification code using 2 digits.

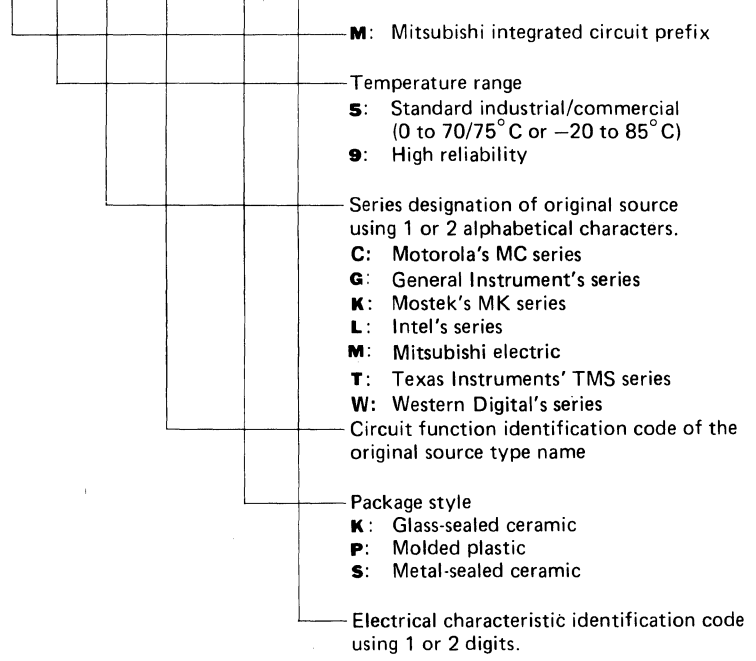
Package style
- **K**: Glass-sealed ceramic
- **P**: Molded plastic
- **S**: Metal-sealed ceramic
- **D**: Chip carrier

Electrical characteristic identification code using 1 or 2 digits.

# ORDERING INFORMATION

## For Second Source Products

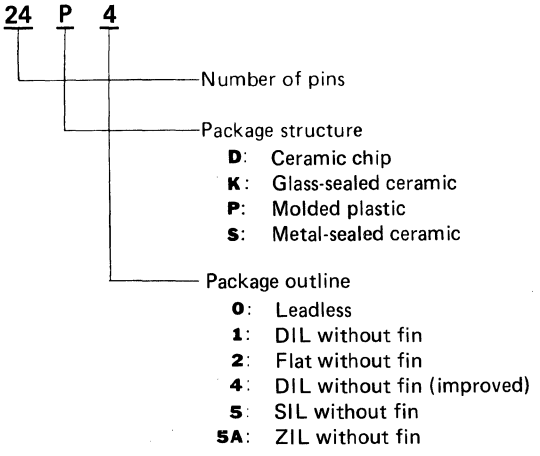
Example: M 5 M 4256 P – 12




## PACKAGE CODE

Package style may be specified by using the following simplified alphanumeric code.

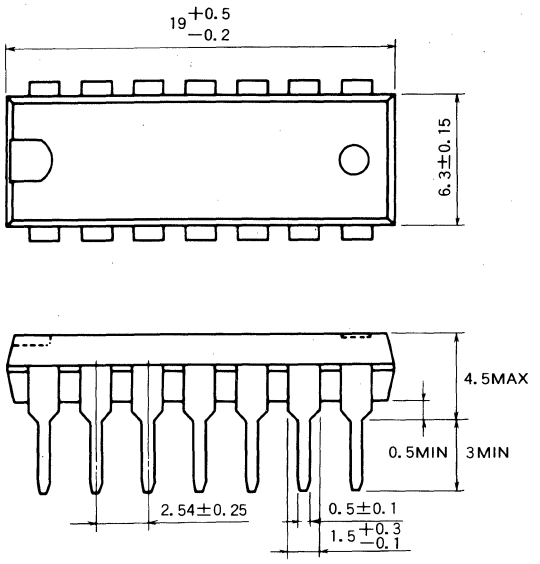
Example: 24 P 4



# PACKAGE OUTLINES

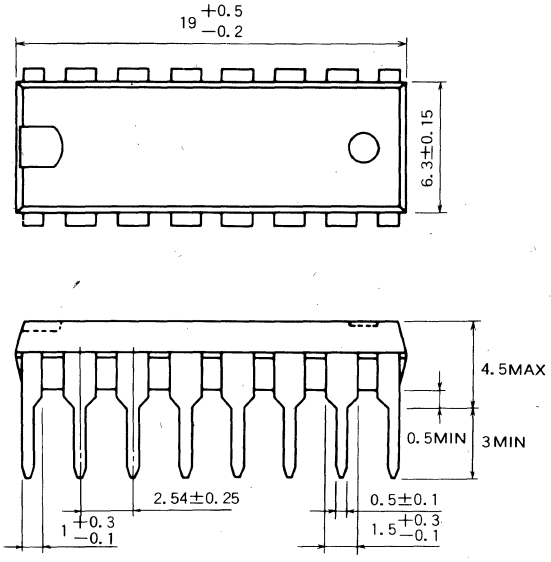
## TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimensions in mm




## TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimensions in mm

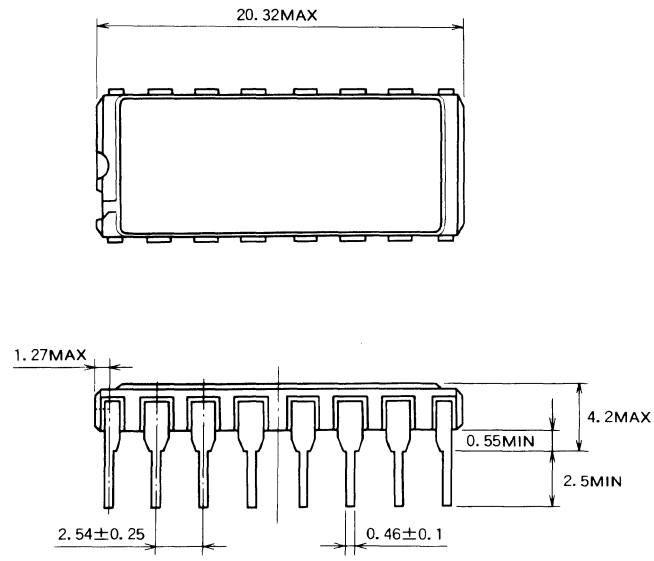





MITSUBISHI ELECTRIC

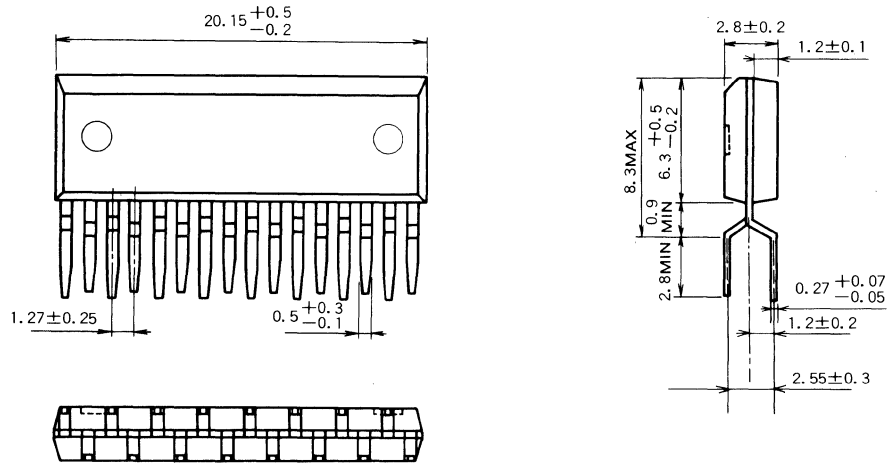
## TYPE 16S1 16-PIN METAL-SEALED CERAMIC DIL

Dimensions in mm



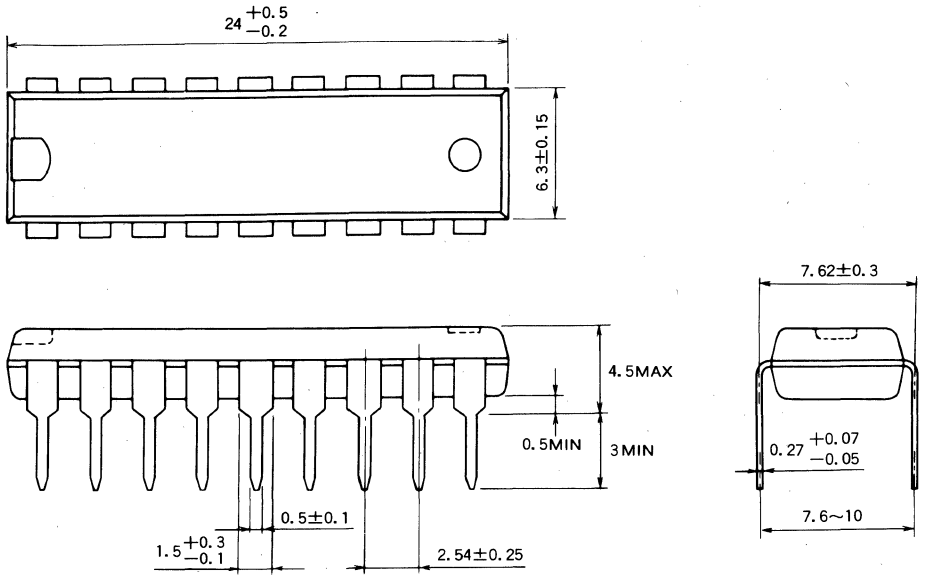

## TYPE 16P5A 16-PIN MOLDED PLASTIC ZIL

Dimensions in mm



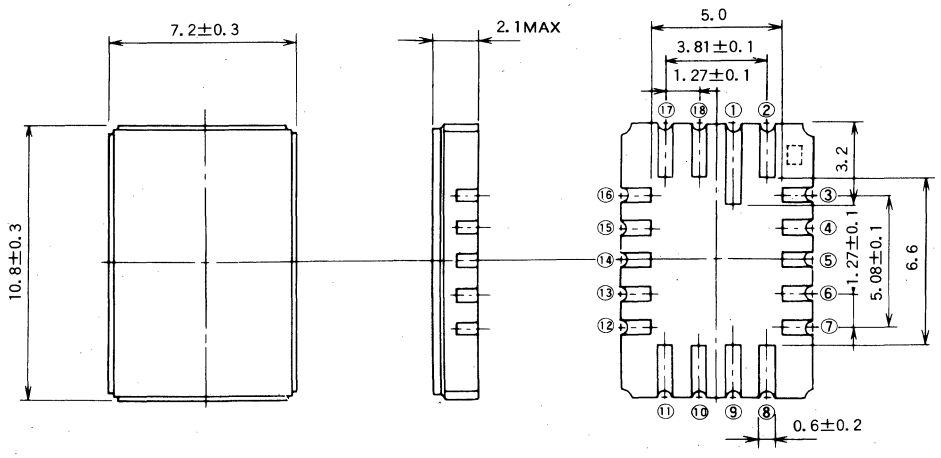
## TYPE 18P4 18-PIN MOLDED PLASTIC DIL

Dimensions in mm




## TYPE 18D0 18-PIN LEADLESS CHIP CARRIER

Dimensions in mm

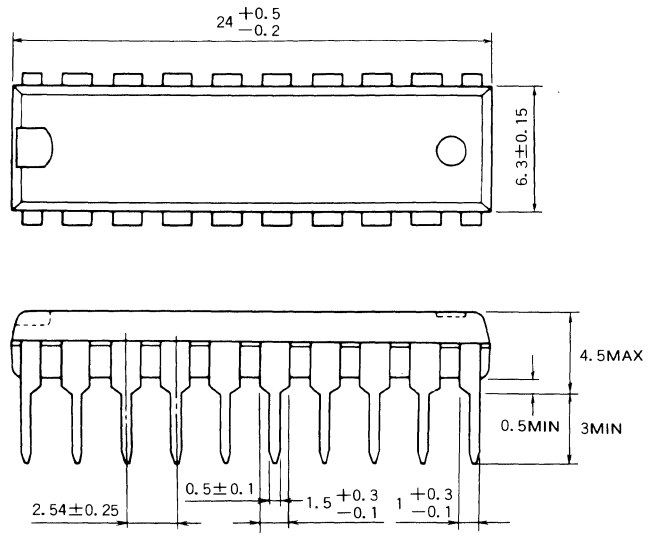





MITSUBISHI ELECTRIC

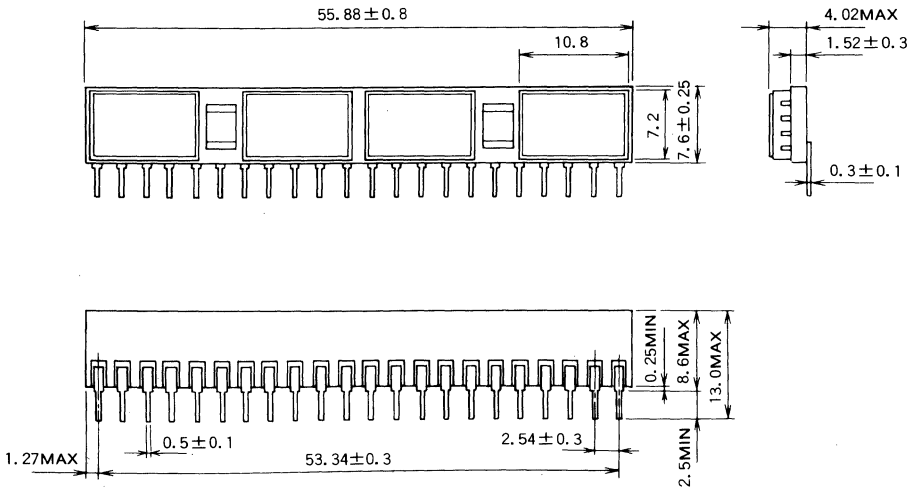
## TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimensions in mm



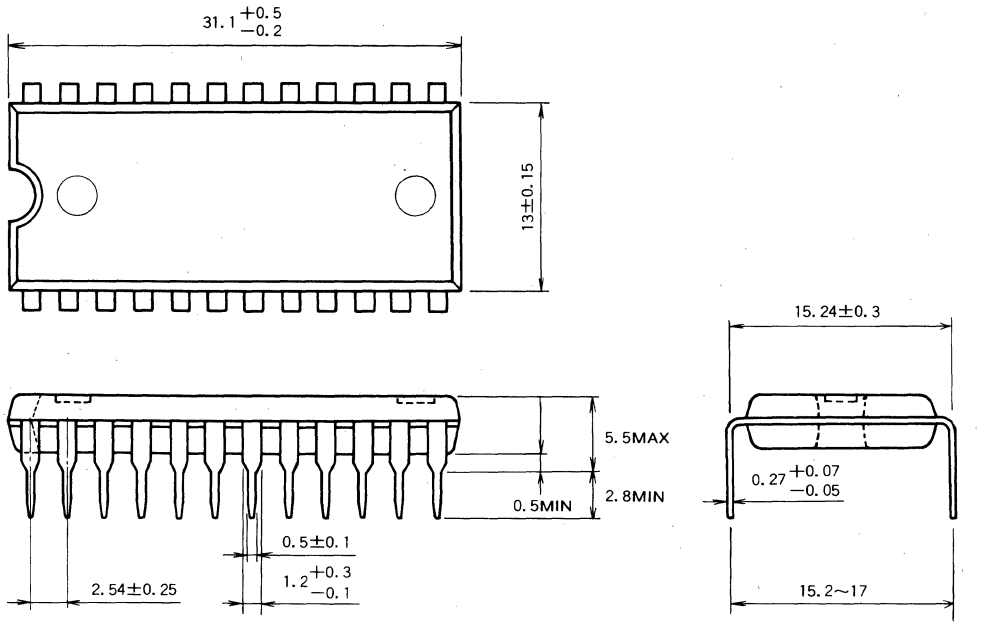

## TYPE 22S5 22-PIN CHIP CARRIER

Dimensions in mm



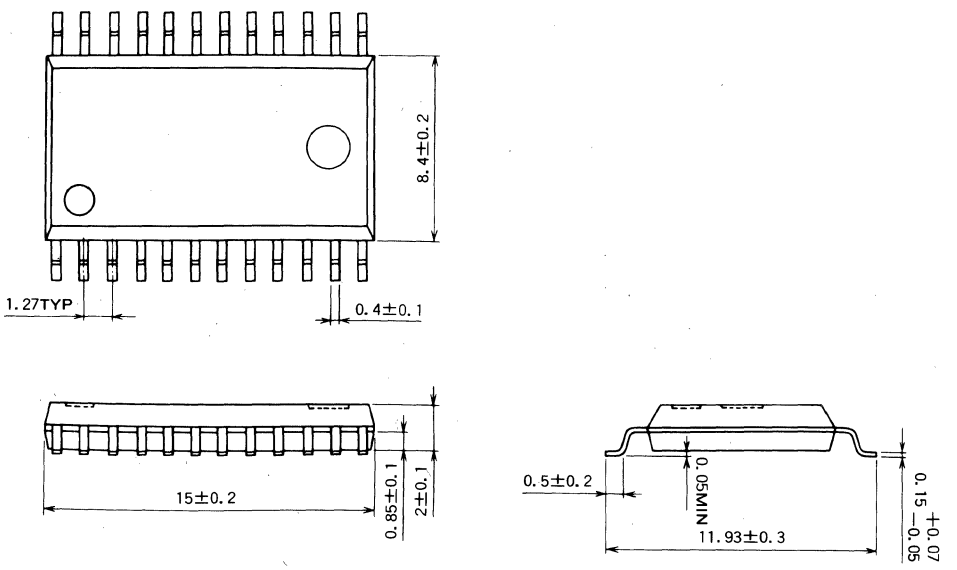
## TYPE 24P4 24-PIN MOLDED PLASTIC DIL

Dimensions in mm




## TYPE 24P2W 24-PIN MOLDED PLASTIC FLAT

Dimensions in mm

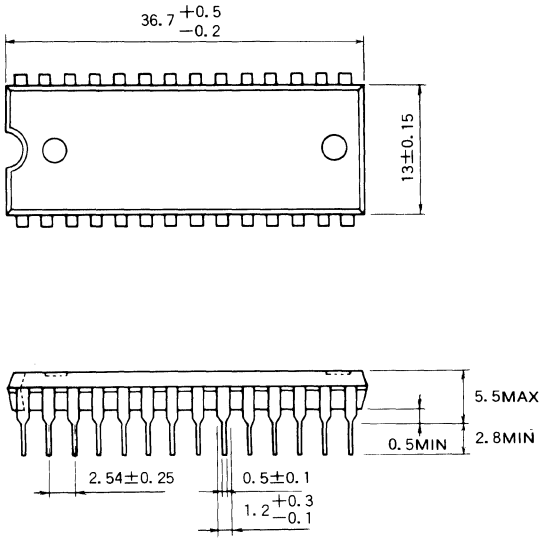





MITSUBISHI ELECTRIC

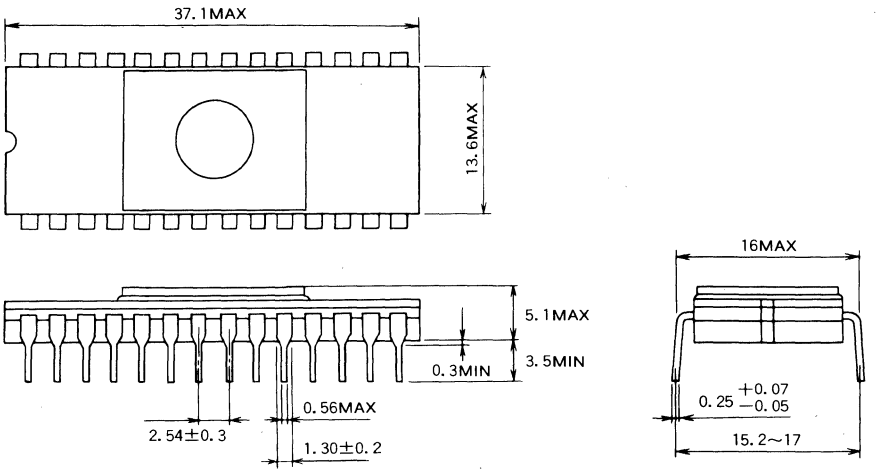
## TYPE 28P4 28-PIN MOLDED PLASTIC DIL

Dimensions in mm



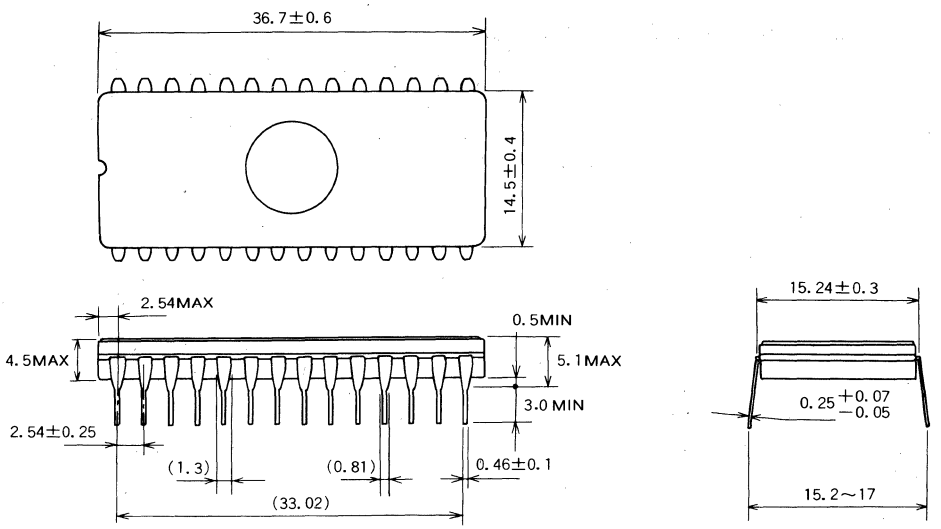

## TYPE 28K1 28-PIN GLASS-SEALED CERAMIC DIL WITH TRANSPARENT LID

Dimensions in mm



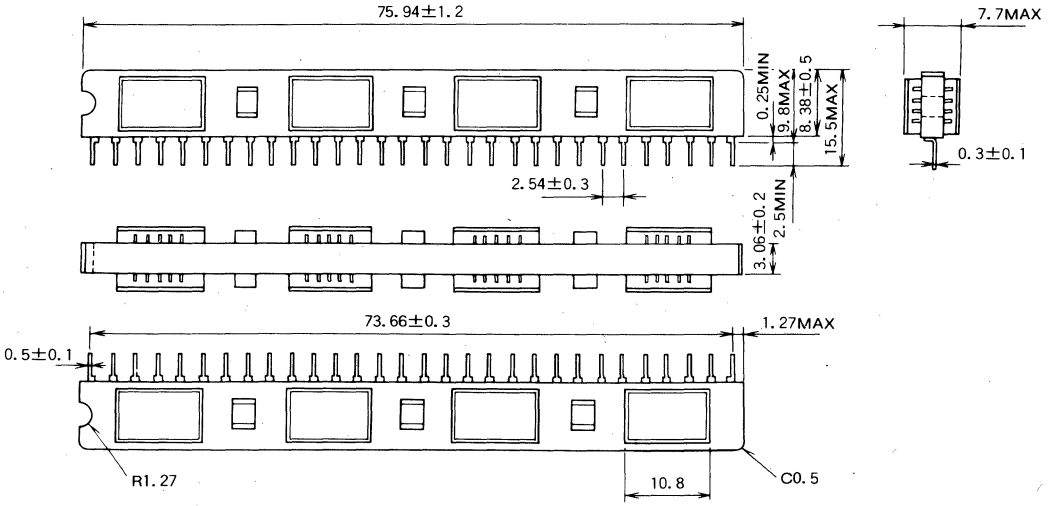
## TYPE 28K4 28-PIN GLASS-SEALED CERAMIC DIL WITH TRANSPARENT LID

Dimensions in mm




## TYPE 30S5 30-PIN CHIP CARRIER

Dimensions in mm



# LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

## 1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

## 2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

### 2.1. General Form

The dynamic parameters are represented by a general symbol of the form:-

$t_{A(BC-DC)F}$ ..... (1)

**where :**

**Subscript A** indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

**Subscript B** indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

**Subscript C** indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

**Subscript D** indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

**Subscript E** indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

**Subscript F** indicates additional information such as mode of operation, test conditions, etc.

Note 1: Subscripts A to F may each consists of one or more letters.
2: Subscripts D and E are not used for transition times.
3: The "–" in the symbol (1) above is used to indicate "to"; hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times. Where no misunderstanding can occur the hyphen may be omitted.

### 2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or $t_{AF}$ – no brackets are used in this case

or $t_{A}$

or $t_{BC-DE}$ – often used for unclassified time intervals

### 2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

## 3. SUBSCRIPT A (For Type of Dynamic Parameter)

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

# LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

b) those that are characteristics of the memory.

The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.

All subscripts A should be in lower-case.

## 3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

| Term | Subscript |
|---|---|
| Cycle time | c |
| Time interval between two signal events | d |
| Fall time | f |
| Hold time | h |
| Precharging time | pc |
| Rise time | r |
| Recovery time | rec |
| Refresh time interval | rf |
| Setup time | su |
| Transition time | t |
| Pulse duration (width) | w |

## 3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

| Characteristic | Subscript |
|---|---|
| Access time | a |
| Disable time | dis |
| Enable time | en |
| Propagation time | p |
| Recovery time | rec |
| Transition time | t |
| Valid time | v |

Note: Recovery time for use as a characteristic is limited to sense recovery time.

## 4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.

All subscripts B and D should be in upper-case.

| Signal or terminal | Subscript |
|---|---|
| Address | A |
| Clock | C |
| Column address | CA |
| Column address strobe | CAS |
| Data input | D |
| Data input/output | DQ |
| Chip enable | E |
| Erasure | ER |
| Output enable | G |
| Program | PR |
| Data output | Q |
| Read | R |
| Row address | RA |
| Row address strobe | RAS |
| Refresh | RF |
| Read/Write | RW |
| Chip select | S |
| Write (write enable) | W |

Note 1: In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used.

2: It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z. (See clause 5)

3: If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter.

## 5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

| Transition of signal | Subscript |
|---|---|
| High logic level | H |
| Low logic level | L |
| Valid steady-state level (either low or high) | V |
| Unknown, changing, or 'don't care' level | X |
| High-impedance state of three-state output | Z |

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.

When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.

All subscripts C and E should be in upper-case.

| Examples | Subscript | |
|---|---|---|
| | Full | Abbreviated |
| Transition from high level to low level | HL | L |
| Transition from low level to high level | LH | H |
| Transition from unknown or changing state to valid state | XV | V |
| Transition from valid state to unknown or changing state | VX | X |
| Transition from high-impedance state to valid state | ZV | V |

Note: Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion.

## 6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

| Modes of operation | Subscript |
|---|---|
| Power-down | PD |
| Page-mode read | PGR |
| Page-mode write | PGW |
| Read | R |
| Refresh | RF |
| Read-modify-write | RMW |
| Read-write | RW |
| Write | W |

## FOR DIGITAL INTEGRATED CIRCUITS

| New symbol | Former symbol | Parameter—definition |
|---|---|---|
| $C_i$ | | Input capacitance |
| $C_o$ | | Output capacitance |
| $C_{i/o}$ | | Input/output terminal capacitance |
| $C_{i(\phi)}$ | | Input capacitance of clock input |
| f | | Frequency |
| $f_{(\phi)}$ | | Clock frequency |
| I | | Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value |
| $I_{BB}$ | | Supply current from $V_{BB}$ |
| $I_{BB(AV)}$ | | Average supply current from $V_{BB}$ |
| $I_{CC}$ | | Supply current from Vcc |
| $I_{CC(AV)}$ | | Avarage supply current from Vcc |
| $I_{CC(PD)}$ | | Power-down supply current from Vcc |
| $I_{DD}$ | | Supply current from $V_{DD}$ |
| $I_{DD(AV)}$ | | Average supply current from $V_{DD}$ |
| $I_{GG}$ | | Supply current from $V_{GG}$ |
| $I_{GG(AV)}$ | | Average supply current from $V_{GG}$ |
| $I_I$ | | Input current |
| $I_{IH}$ | | High-level input current—the value of the input current when $V_{OH}$ is applied to the input considered |
| $I_{IL}$ | | Low-level input current—the value of the input current when $V_{OL}$ is applied to the input considered |
| $I_{OH}$ | | High-level output current—the value of the output current when $V_{OH}$ is applied to the output considered |
| $I_{OL}$ | | Low-level output current—the value of the output current when $V_{OL}$ is applied to the output considered |
| $I_{OZ}$ | | Off-state (high-impedance state) output current—the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output |
| $I_{OZH}$ | | Off-state (high-impedance state) output current, with high-level voltage applied to the output |
| $I_{OZL}$ | | Off-state (high-impedance state) output current, with low-level voltage applied to the output |
| $I_{OS}$ | | Short-circuit output current |
| $I_{SS}$ | | Supply current from $V_{SS}$ |
| Pd | | Power dissipation |
| $N_{EW}$ | | Number of erase/write cycles |
| $N_{RA}$ | | Number of read access unrefreshed |
| $R_i$ | | Input resistance |
| $R_L$ | | External load resistance |
| $R_{OFF}$ | | Off-state output resistance |
| $R_{ON}$ | | On-state output resistance |
| $t_a$ | | Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output |
| $t_{a(A)}$ | $t_{a(AD)}$ | Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output |
| $t_{a(CAS)}$ | | Column address strobe access time |
| $t_{a(E)}$ | $t_{a(CE)}$ | Chip enable access time |
| $t_{a(G)}$ | $t_{a(OE)}$ | Output enable access time |
| $t_{a(PR)}$ | | Data access time after program |
| $t_{a(RAS)}$ | | Row address strobe access time |
| $t_{a(S)}$ | $t_{a(CS)}$ | Chip select access time |
| $t_C$ | | Cycle time |
| $t_{CR}$ | $t_{C(RD)}$ | Read cycle time—the time interval between the start of a read cylce and the start of the next cycle |
| $t_{CRF}$ | $t_{C(REF)}$ | Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level |
| $t_{CPG}$ | $t_{C(PG)}$ | Page-mode cycle time |
| $t_{CRMW}$ | $t_{C(RMR)}$ | Read-modify-write cycle time—the time interval between teh start of a cycle in which the memory is read and new data is entered, and the start of the next cycle |
| $t_{CW}$ | $t_{C(WR)}$ | Write cycle time—the time interval between the start of a write cycle and the start of the next cycle |

| | Former symbol | Parameter—definition |
|---|---|---|
| $t_d$ | | Delay time—the time between the specified reference points on two pulses |
| $t_{d(\phi)}$ | | Delay time between clock pulses—e.g., symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1 |
| $t_{d(CAS\text{-}RAS)}$ | | Delay time, column address strobe to row address strobe |
| $t_{d(CAS\text{-}W)}$ | $t_{d(CAS\text{-}WR)}$ | Delay time, column address strobe to write |
| $t_{d(RAS\text{-}CAS)}$ | | Delay time, row address strobe to column address strobe |
| $t_{d(RAS\text{-}W)}$ | $t_{d(RAS\text{-}WR)}$ | Delay time, row address strobe to write |
| $t_{dis(R\text{-}Q)}$ | $t_{dis(R\text{-}DA)}$ | Output disable time after read |
| $t_{dis(S)}$ | $t_{PXZ(CS)}$ | Output disable time after chip select |
| $t_{dis(W)}$ | $t_{PXZ(WR)}$ | Output disable time after write |
| $t_{DHL}$ | | High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the |
| $t_{DLH}$ | | Low-level to high-level delay time } output is going to the low (high) level and when the device is driven and loaded by specified networks. |
| $t_{en(A\text{-}Q)}$ | $t_{PZV(A\text{-}DQ)}$ | Output enable time after address |
| $t_{en(R\text{-}Q)}$ | $t_{PZV(R\text{-}DQ)}$ | Output enable time after read |
| $t_{en(S\text{-}Q)}$ | $t_{PZX(CS\text{-}DQ)}$ | Output enable time after chip select |
| $t_f$ | | Fall time |
| $t_h$ | | Hold time—the interval time during which a signal at a specified input terminal after an active transition occurs at another specified input terminal |
| $t_{h(A)}$ | $t_{h(AD)}$ | Address hold time |
| $t_{h(A\text{-}E)}$ | $t_{h(AD\text{-}CE)}$ | Chip enable hold time after address |
| $t_{h(A\text{-}PR)}$ | $t_{h(AD\text{-}PRO)}$ | Program hold time after address |
| $t_{h(CAS\text{-}CA)}$ | | Column address hold time after column address strobe |
| $t_{h(CAS\text{-}D)}$ | $t_{h(CAS\text{-}DA)}$ | Data-in hold time after column address strobe |
| $t_{h(CAS\text{-}Q)}$ | $t_{h(CAS\text{-}OUT)}$ | Data-out hold time after column address strobe |
| $t_{h(CAS\text{-}RAS)}$ | | Row address strobe hold time after column address strobe |
| $t_{h(CAS\text{-}W)}$ | $t_{h(CAS\text{-}WR)}$ | Write hold time after column address strobe |
| $t_{h(D)}$ | $t_{h(DA)}$ | Data-in hold time |
| $t_{h(D\text{-}PR)}$ | $t_{h(DA\text{-}PRO)}$ | Program hold time after data-in |
| $t_{h(E)}$ | $t_{h(CE)}$ | Chip enable hold time |
| $t_{h(E\text{-}D)}$ | $t_{h(CE\text{-}DA)}$ | Data-in hold time after chip enable |
| $t_{h(E\text{-}G)}$ | $t_{h(CE\text{-}OE)}$ | Output enable hold time after chip enable |
| $t_{h(R)}$ | $t_{h(RD)}$ | Read hold time |
| $t_{h(RAS\text{-}CA)}$ | | Column address hold time after row address strobe |
| $t_{h(RAS\text{-}CAS)}$ | | Column address strobe hold time after row address strobe |
| $t_{h(RAS\text{-}D)}$ | $t_{h(RAS\text{-}DA)}$ | Data-in hold time after row address strobe |
| $t_{h(RAS\text{-}W)}$ | $t_{h(RAS\text{-}WR)}$ | Write hold time after row address strobe |
| $t_{h(S)}$ | $t_{h(CS)}$ | Chip select hold time |
| $t_{h(W)}$ | $t_{h(WR)}$ | Write hold time |
| $t_{h(W\text{-}CAS)}$ | $t_{h(WR\text{-}CAS)}$ | Column address strobe hold time after write |
| $t_{h(W\text{-}D)}$ | $t_{h(WR\text{-}DA)}$ | Data-in hold time after write |
| $t_{h(W\text{-}RAS)}$ | $t_{h(WR\text{-}RAS)}$ | Row address hold time after write |
| $t_{PHL}$ | | High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type |
| $t_{PLH}$ | | Low-level to high-level propagation time } |
| $t_r$ | | Rise time |
| $t_{rec(W)}$ | $t_{wr}$ | Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle |
| $t_{rec(PD)}$ | $t_{R(PD)}$ | Power-down recovery time |
| $t_{su}$ | | Setup time—the time interval between the application of a signal which is maintained at a speciifed input terminal and a consecutive active tarnsition at another specified input terminal |
| $t_{su(A)}$ | $t_{su(AD)}$ | Address setup time |
| $t_{su(A\text{-}E)}$ | $t_{su(AD\text{-}CE)}$ | Chip enable setup time before address |
| $t_{su(A\text{-}W)}$ | $t_{su(AD\text{-}WR)}$ | Write setup time before address |
| $t_{su(CA\text{-}RAS)}$ | | Row address strobe setup time before column address |

| New symbol | Former symbol | Parameter—definition |
|---|---|---|
| $t_{su(D)}$ | $t_{su(DA)}$ | Data-in setup time |
| $t_{su(D-E)}$ | $t_{su(DA-CE)}$ | Chip enable setup time before data-in |
| $t_{su(D-W)}$ | $t_{su(DA-WR)}$ | Write setup time before data-in |
| $t_{su(E)}$ | $t_{su(CE)}$ | Chip enable setup time |
| $t_{su(E-P)}$ | $t_{su(CE-P)}$ | Precharge setup time before chip enable |
| $t_{su(G-E)}$ | $t_{su(OE-CE)}$ | Chip enable setup time before output enable |
| $t_{su(P-E)}$ | $t_{su(P-CE)}$ | Chip enable setup time before precharge |
| $t_{su(PD)}$ | | Power-down setup time |
| $t_{su(R)}$ | $t_{su(RD)}$ | Read setup time |
| $t_{su(R-CAS)}$ | $t_{su(RA-CAS)}$ | Column address strobe setup time before read |
| $t_{su(RA-CAS)}$ | | Column address strobe setup time before row address |
| $t_{su(S)}$ | $t_{su(CS)}$ | Chip select setup time |
| $t_{su(S-W)}$ | $t_{su(CS-WR)}$ | Write setup time before chip select |
| $t_{su(W)}$ | $t_{su(WR)}$ | Write setup time |
| $t_{THL}$ | | High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network |
| $t_{TLH}$ | | Low-level- to high-level transition time } |
| $t_{v(A)}$ | $t_{dv(AD)}$ | Data valid time after address |
| $t_{v(E)}$ | $t_{dv(CE)}$ | Data valid time after chip enable |
| $t_{v(E)PR}$ | $t_{v(CE)PR}$ | Data valid time after chip enable in program mode |
| $t_{v(G)}$ | $t_{v(OE)}$ | Data valid time after output enable |
| $t_{v(PR)}$ | | Data valid time after program |
| $t_{v(S)}$ | $t_{v(CS)}$ | Data valid time after chip select |
| $t_W$ | | Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms |
| $t_{w(E)}$ | $t_{w(CE)}$ | Chip enable pulse width |
| $t_{w(EH)}$ | $t_{w(CEH)}$ | Chip enable high pulse width |
| $t_{w(EL)}$ | $t_{w(EL)}$ | Chip enable low pulse width |
| $t_{w(PR)}$ | | Program pulse width |
| $t_{w(R)}$ | $t_{w(RD)}$ | Read pulse width |
| $t_{w(S)}$ | $t_{w(CS)}$ | Chip select pulse width |
| $t_{w(W)}$ | $t_{w(WR)}$ | Wrtie pulse width |
| $t_{w(\phi)}$ | | Clock pulse width |
| Ta | | Ambient temperature |
| Topr | | Operating temperature |
| Tstg | | Storage temperature |
| $V_{BB}$ | | $V_{BB}$ supply voltage |
| $V_{CC}$ | | $V_{CC}$ supply voltage |
| $V_{DD}$ | | $V_{DD}$ supply voltage |
| $V_{GG}$ | | $V_{GG}$ supply voltage |
| $V_I$ | | Input voltage |
| $V_{IH}$ | | High-level input voltage—the value of the permitted high-state voltage at the input |
| $V_{IL}$ | | Low-level input voltage—the value of the permitted low-state voltage at the input |
| $V_O$ | | Output voltage |
| $V_{OH}$ | | High-level output voltage—the value of the guaranteed high-state voltage range at the output |
| $V_{OL}$ | | Low-level output voltage—the value of the guaranteed low-state voltage range at the output |
| $V_{SS}$ | | $V_{SS}$ supply voltage |

Note: These abbreviations, with some exceptions, are excerpted from IEC publication 148.

# QUALITY ASSURANCE AND RELIABILITY TESTING

## 1. PLANNING

In recent years, advances in integrated circuits have been rapid, with increasing density and speed accompanied by decreasing cost. Because of these advances, it is now practical and economically justifiable to use these devices in systems of greater complexity and in which they were previously considered too expensive. All of these advances add up to increased demand.

We at Mitsubishi foresaw this increased demand and organized our production facilities to meet it. We also realized that simply increasing production to meet the demand was not enough and that positive steps would have to be taken to assure the reliability of our products.

This realization resulted in development of our Quality Assurance System. The system has resulted in improved products, and Mitsubishi is able to supply its customers' needs with ICs of high reliability and stable quality. This system is the key to future planning for improved design, production and quality assurance.

## 2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System imposes quality controls on Mitsubishi products from the initial conception of a new product to the final delivery of the product to the customer. A diagram of the total system is shown in Fig. 1. For ease of understanding, the system is divided into three stages.

### 2.1 Quality Assurance in the Design Stage

The characteristics of the breadboard devices are carefully checked to assure that all specifications are met. Standard integrated circuits and high-quality discrete components are used. During the design stage, extensive use is made of a sophisticated CAD program, which is updated to always include the latest state-of-the-art techniques.

### 2.2 Quality Assurance in the Limited-Manufacturing Stage

Rigid controls are maintained on the environment, incoming material and manufacturing equipment such as tools and test equipment. The products and materials used are subjected to stringent tests and inspections as they are manufactured. Wafer production is closely monitored.

Finally, a tough quality assurance test and inspection is made before the product is released for delivery to a customer. This final test includes a complete visual inspection and electrical characteristics tests. A sampling technique is used to conduct tests under severe operating conditions to assure that the products meet reliability specifications.

### 2.3 Quality Assurance in the Full Production Stage

Full production of a product is not started until it has been confirmed that it can be manufactured to meet quality and reliability specifications. The controls, tests and inspection procedures developed in §2.2 are continued. The closest monitoring assures that they are complied with.

## 3. RELIABILITY CONTROL

### 3.1 Reliability Tests

The newly established Reliability Center for Electronic Components of Japan has established a qualification system for electronic components. Reliability test methods and procedures are developed to mainly meet MIL-STD-883 and JIS C 7022 specifications. Details of typical tests used on Mitsubishi ICs are shown in Table 1.

**Table 1 Typical reliability test items and conditions**

| Group | Item | Test condition |
|---|---|---|
| 1 | High temperature operating life | Maximum operating ambient temperature 1000h |
| | High temperature storage life | Maximum storage temperature 1000h |
| | Humidity (steady state) life | 85°C 85% RH 500h |
| 2 | Soldering heat | 260°C 10s |
| | Thermal shock | 0 ~ 100°C 15 cycles, 10min/cycle |
| | Temperature cycle | Minimum to maximum storage temperature 10 cycles of 1h/cycle |
| 3 | Soldering | 230°C, 5s, use rosin flux |
| | Lead integrity | Tension: 500g 10s<br>Bending stress: 250g, 90°, 2 tme |
| | Vibration | 20G, X, Y, Z each direction, 4 times<br>100 ~ 2000Hz – 4 min/cycle |
| | Shock | 1500G, 0.5ms in $X_1$. $Y_1$ and $Z_1$ direction, 5 times. |
| | Constant acceleration | 20000G, $Y_1$ direction, 1 min |

### 3.2 Failure Analysis

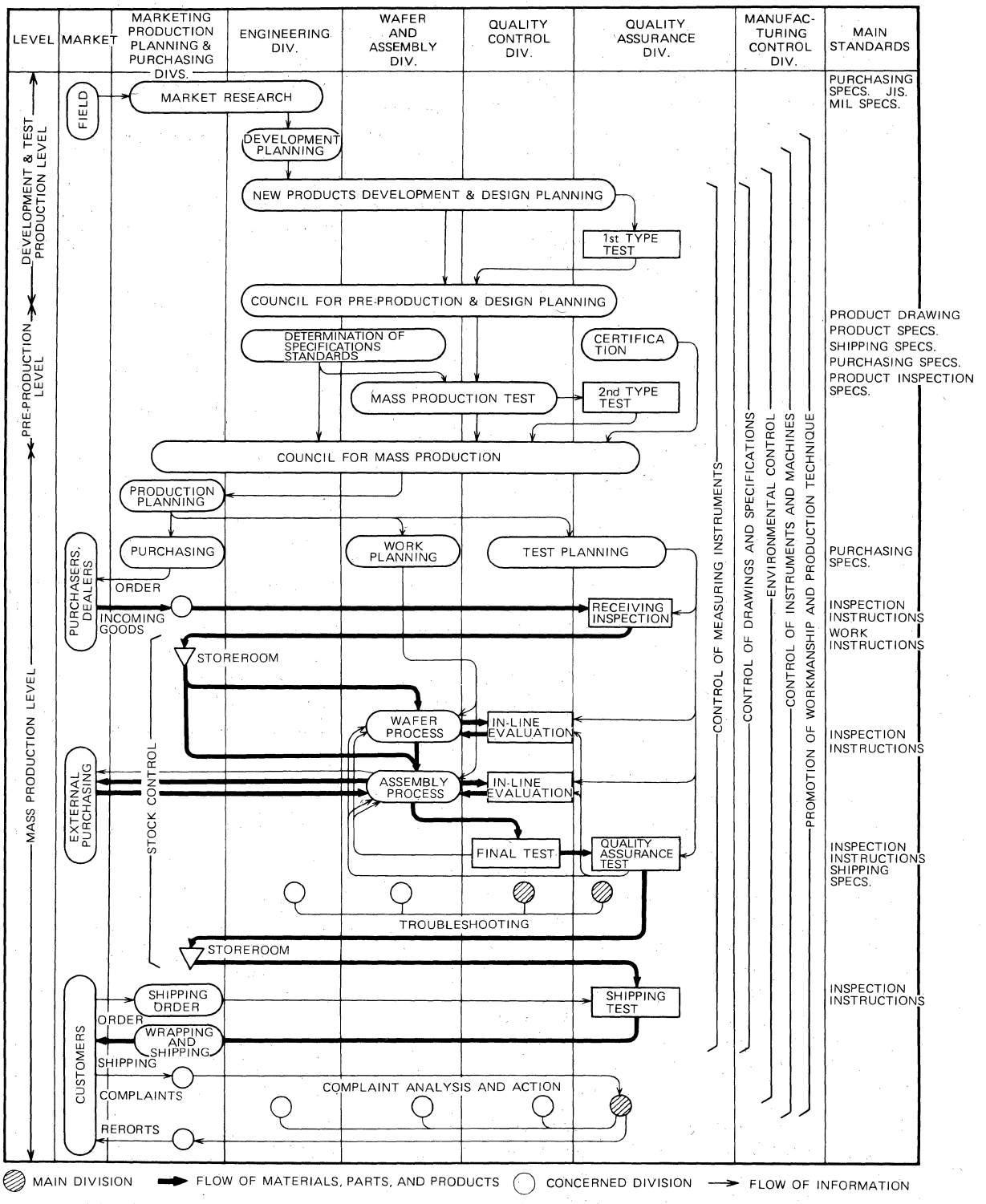
Devices that have failed during reliability or acceleration tests are analyzed to determine the cause of failure. This information is fed back to the process engineering section and manufacturing section so that improvements can be made to increase reliability. A summary of failure analysis procedures is shown in Table 2.

**Table 2 Summary of failure analysis procedures**

| Step | Description |
|---|---|
| 1. External examination | o Inspection of leads, plating, soldering and welding<br>o Inspection of materials, sealing, package and marking<br>o Visual inspection of other items of the specifications<br>o Use of stereo microscopes, metallurgical microscopes, X-ray photographic equipment, fine leakage and gross leakage testers in the examination |
| 2. Electrical tests | o Checking for open circuits, short circuits and parametric degradation by electrical parameter measurement<br>o Observation of characteristics by a synchroscope or a curve tracer and checking of important physical characteristics by electrical characteristics<br>o Stress tests such as environmental or life tests, if required |
| 3. Internal examination | o Removal of the cover of the device, the optical inspection of the internal structure of the device<br>o Checking of the silicon chip surface<br>o Measurement of electrical characteristics by probes, if applicable<br>o Use of SEM, XMA and infrared microscanner if required |
| 4. Chip analysis | o Use of metallurgical analysis techniques to supplement analysis of the internal examination<br>o Slicing for cross sectional inspection<br>o Analysis of oxide film defects<br>o Analysis of diffusion defects |

# QUALITY ASSURANCE AND RELIABILITY TESTING

**Fig.1 Quality assurance system**



## TYPICAL RESULTS OF RELIABILITY TESTS AND FAILURE ANALYSES

### 1. Results of Reliability Test

Formerly, sufficient reliability for memory MOS LSIs was obtained by using metal-sealed ceramic packages, but with the development of high-reliability plastic molding technology, production has been shifted to plastic molded memory MOS LSIs.

The following tests are performed:

(1) Operating life test: Durability is tested at high temperature under operating state conditions by applying clock pulse inputs as shown in Fig. 2.

(2) DC biased test: Durability is tested at high temperature biasing DC voltage, as shown in Fig. 3.

(3) High temperature storage: The durability of devices stored at high temperatures is tested.

Typical results of memory MOS LSI life tests are shown in Table 3. The failure rate computed from this reliability data using an appropriate acceleration factor is 100FIT or less (1FIT = $10^{-9}$/hour)

**Fig. 2 Operating life test procedure for 256K-bit dynamic RAM**

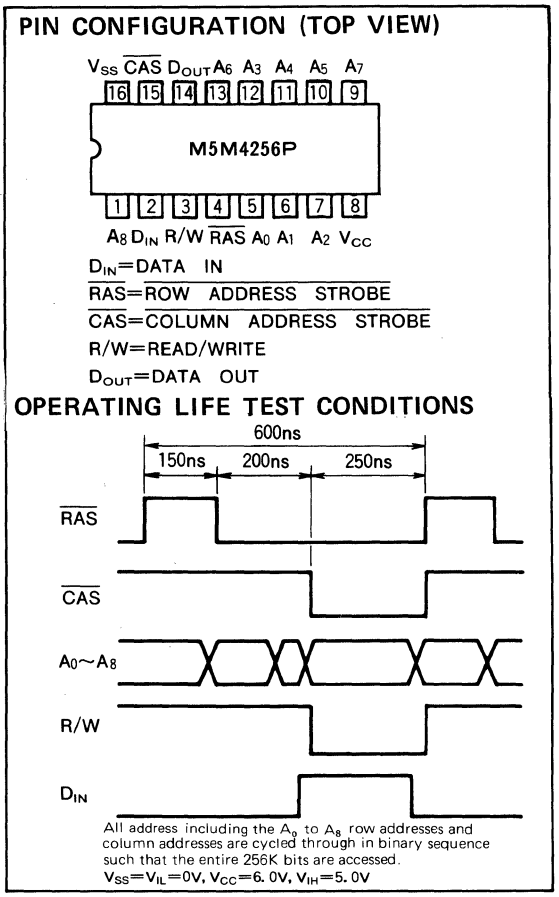



**Fig. 3 DC biased test procedure for 64K-bit static RAM (M5M5165P)**

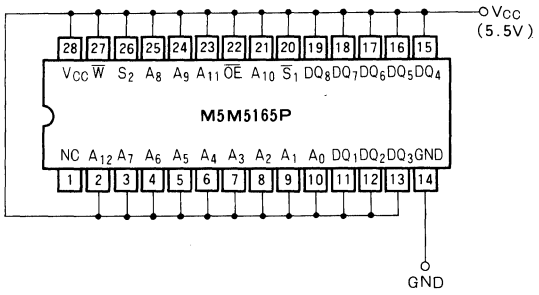



**Table 3 Examples of Endurance Test Results**

| Type | Package | Test category | | Sample size | Component hours | Failures | Remarks |
|---|---|---|---|---|---|---|---|
| M5M4256P<br>M5M4257P | 16 pin plastic-molded DIL | Operating life | 125°C | 200 | 200000 | 0 | |
| | | | | 5000 | 480000 | 2 | Functional failures |
| | | | 150°C | 200 | 200000 | 1 | Functional failure |
| | | High temperature storage | 150°C | 200 | 200000 | 0 | |
| M5M4256S<br>M5M4257S | 16 pin metal-sealed ceramic DIL | Operating life | 125°C | 240 | 240000 | 0 | |
| | | | | 5886 | 235440 | 3 | Functional failures |
| | | High temperature storage | 150°C | 80 | 80000 | 0 | |
| M5K4164AP<br>M5K4164ANP | 16 pin plastic-molded DIL | Operating life | 125°C | 1200 | 1200000 | 1 | Functional failure |
| | | High temperature storage | 150°C | 300 | 300000 | 0 | |
| M5M5165P | 28 pin plastic-molded DIL | Operating life | 125°C | 480 | 480000 | 0 | |
| | | | | 5324 | 212960 | 2 | Functional failures |
| | | High temperature storage | 150°C | 100 | 100000 | 0 | |
| M5M2167P<br>M5M2168P | 20 pin plastic-molded DIL | Operating life | 125°C | 640 | 640000 | 1 | Functional failure |
| | | High temperature storage | 150°C | 320 | 320000 | 0 | |
| M5M5116P<br>M5M5117P<br>M5M5118P | 24 pin plastic-molded DIL | Operating life | 125°C | 172 | 172000 | 0 | |
| | | DC biased | 125°C | 160 | 160000 | 0 | |
| | | High temperature storage | 150°C | 160 | 160000 | 0 | |
| M5L2764K | 28 pin glass-sealed ceramic DIL with glass lid | Operating life | 125°C | 364 | 364000 | 1 | Functional failure |
| | | High temperature storage | 150°C | 144 | 144000 | 0 | |
| M5L27128K | 28 pin glass-sealed ceramic DIL | Operating life | 125°C | 264 | 264000 | 0 | |
| | | High temperature storage | 150°C | 144 | 144000 | 0 | |

**Table 4 Examples of Environmental Test Results**

| Test category | | Test conditions | Type | Sample size | Failures | Remarks |
|---|---|---|---|---|---|---|
| Thermal environment | Soldering heat | 260℃, 10s | M5M4256P<br>M5M4257P<br>M5M4256S<br>M5M4257S | 1,000 | 0 | — |
| | Thermal shock | −55℃～125℃, 10min/cycle, 15 cycles | | | | |
| | Temperature cycling | −65℃～150℃, 1h/cycle, 100 cycles | | | | |
| Mechanical environment | Shock | 1,500G 0.5ms $X_1$, $Y_1$, and $Z_1$ directions, 3 times | M5M4256S<br>M5M4257S | 1,000 | 0 | — |
| | Vibration | 20G, 20～2000Hz X, Y, and Z directions | | | | |
| | Constant acceleration | 30000G, $Y_1$ direction for 1min | | | | |

## CONCLUSION

Mitsubishi Electric's Quality Assurance System is being expanded to provide stronger emphasis on the following points:

1. Establishment of quality and reliability levels that satisfy customers' requirements.
2. Expansion of the reliability tests of wafers and assembly processes for better evaluation, and standardization of circuit and design rules.
3. Establishment of procedures for speeding up the introduction of new technology and improved methods that raise reliability and to improve the accelerated life tests for better failure analysis.
4. Establishment of a system for collecting data on failures in the field, which will then be analyzed to develop improved methods for increasing reliability.

We welcome and appreciate the cooperation of our customers in developing design specifications, establishing quality levels, controlling incoming inspections, developing assembly and adjusting processes and collecting field data. Mitsubishi is anxious to work with its customers to develop ICs of increased reliability that meet their requirements.

# PRECAUTIONS IN HANDLING MOS ICs/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance ($g_m$) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

## 1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

## 2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

## 3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

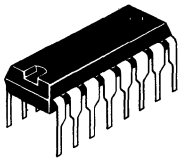
1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1M Ω resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

## 4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

# MOS DYNAMIC RAM

2





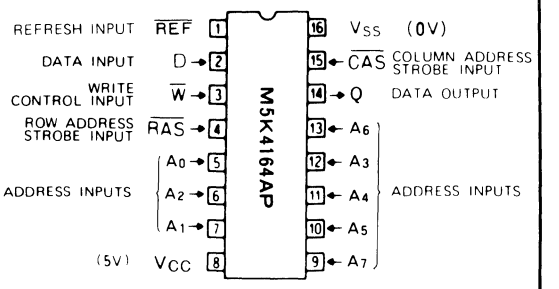
# M5K4164AP-12, -15

## 65 536-BIT (65 536-WORD BY 1-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. The M5K4164AP operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## FEATURES

- High speed

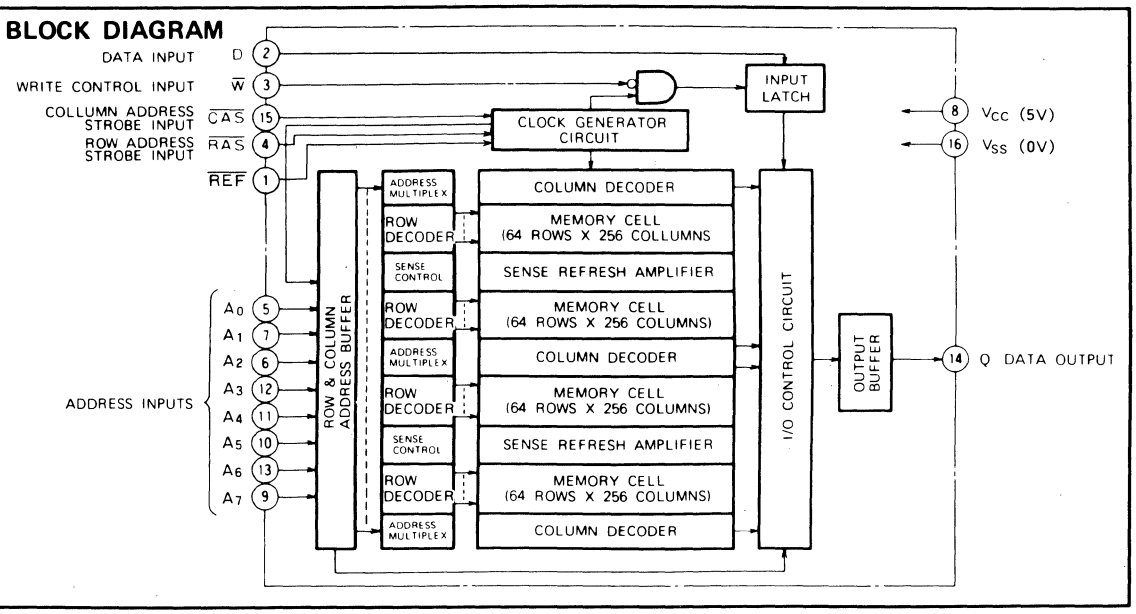
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164AP-12 | 120 | 220 | 175 |
| M5K4164AP-15 | 150 | 260 | 150 |

- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation: 300mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$
- Pin 1 controls automatic- and Self-refresh mode.
- Interchangeable with Fujitsu MB8265A and Motorola's MCM6664 in pin configuration

## APPLICATION

- Main memory unit for computers

## BLOCK DIAGRAM



## FUNCTION

The M5K4164AP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | $\overline{REF}$ | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | NAC | VLD | YES | Page mode identical except refresh is NO. |
| Write | ACT | ACT | ACT | VLD | APD | APD | NAC | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | NAC | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | NAC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | NAC | VLD | YES | |
| Automatic refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Self refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Hidden automatic refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Hidden self refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | NAC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65536 memory cells in the M5K4164AP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5K4164AP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164AP, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164AP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164AP are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Automatic Refresh**

Pin 1 ($\overline{REF}$) has two special functions. The M5K4164AP has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is applied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

**4. Self-Refresh**

The other function of pin 1 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the M5K4164AP will refresh itself. This internal sequence repeats asynchronously every 12 to 16 $\mu$s. After 2 ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 1 ($\overline{REF}$) refresh function gives the user a feature that is free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx 3M\Omega$) on pin 1, so if the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect) without affecting the normal operations.

**5. Hidden Refresh**

A features of the M5K4164AP is that refresh cycle may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164AP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164AP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164AP operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1 ~ 7 | V |
| $V_I$ | Input voltage | | −1 ~ 7 | V |
| $V_O$ | Output voltage | | −1 ~ 7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta = 25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0 ~ 70 | °C |
| Tstg | Storage temperature range | | −65 ~ 150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note. 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V ≦ $V_{OUT}$ ≦ 5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V ≦ $V_{IN}$ ≦ 6.5V, All other pins = 0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164AP-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min output open | | | 50 | mA |
| | | M5K4164AP-15 | | | | 45 | |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS} = V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164AP-12 | $\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(\overline{REF})}$ = min. output open | | | 40 | mA |
| | | M5K4164AP-15 | | | | 35 | |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164AP-12 | $\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$ = min. output open | | | 40 | mA |
| | | M5K4164AP-15 | | | | 35 | |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$, automatic refreshing (Note 3) | M5K4164AP-12 | $\overline{RAS} = V_{IH}$, $\overline{REF}$ cycling $t_{C(REF)}$ = min. output open | | | 40 | mA |
| | | M5K4164AP-15 | | | | 35 | |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, self refreshing | | $\overline{RAS} = V_{IH}$, $\overline{REF} = V_{IL}$ output open | | | 8 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I = V_{SS}$ f = 1MHz $V_I$ = 25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_{I(REF)}$ | Input capacitance, $\overline{REF}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O = V_{SS}$, f = 1MHz, $V_I$ = 25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164AP-12 Limits | | M5K4164AP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | ∞ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 90 | | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | 3 | 35 | ns |

Note 5: An initial pause of 500$\mu$s is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}max$ limit insures that $t_{a(RAS)}max$ can be met. $t_{d(RAS-CAS)}max$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(tTLH)} + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AP-12 Limits | | M5K4164AP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{cR}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 10 | | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$
Note 13: This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}max$. Test conditions; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}max$. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}max$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AP-12 Limits | | M5K4164AP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{cW}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 90 | | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164AP-12 Limits Min | M5K4164AP-12 Limits Max | M5K4164AP-15 Limits Min | M5K4164AP-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 245 | | 295 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 265 | | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 100 | | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 40 | | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 15: $t_{CRW}min$ is defined as $t_{CRW}min = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH}(t_{THL})$

16: $t_{CRMW}$ min is defined as $t_{CRMW}$ min $= t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH}(t_{THL})$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}min$ and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | M5K4164AP-12 Limits Min | M5K4164AP-12 Limits Max | M5K4164AP-15 Limits Min | M5K4164AP-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{c\,PGR}$ | Page-mode read cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{c\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{c\,PGRW}$ | Page-Mode read-write cycle time | — | 150 | | 180 | | ns |
| $t_{c\,PGRMW}$ | Page-Mode read-modify-write cycle time | — | 170 | | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | ns |

## Automatic Refresh Cycle

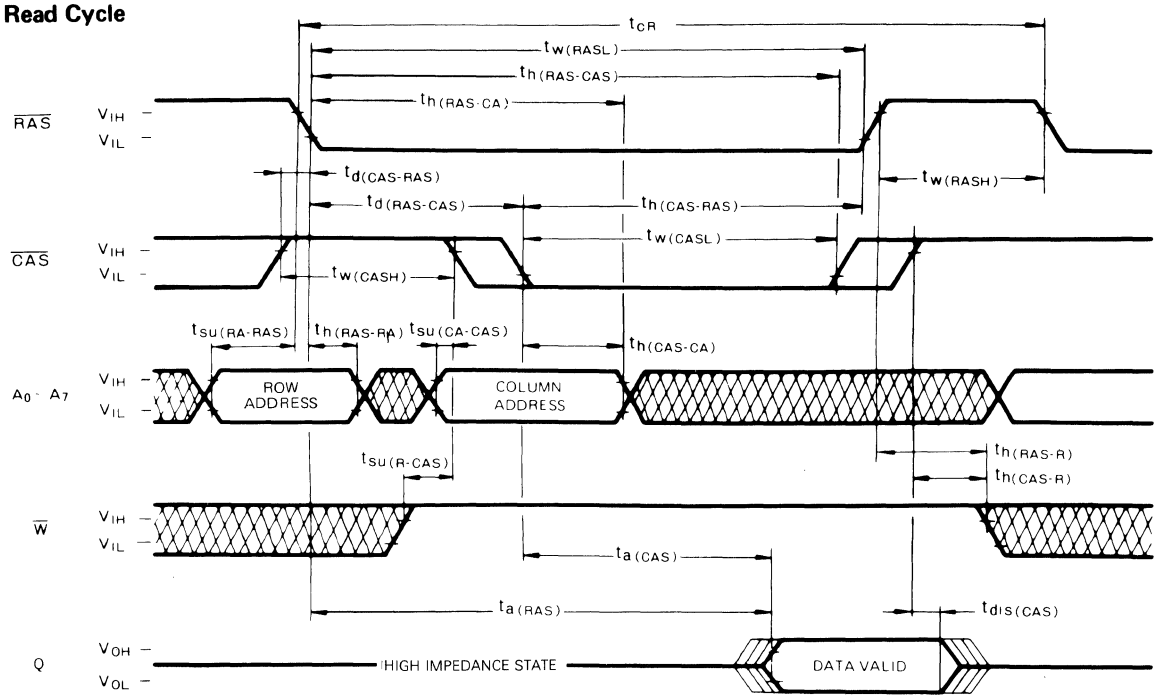
| Symbol | Parameter | Alternative Symbol | M5K4164AP-12 Limits Min | M5K4164AP-12 Limits Max | M5K4164AP-15 Limits Min | M5K4164AP-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{c(REF)}$ | Automatic Refresh cycle time | $t_{FC}$ | 220 | | 260 | | ns |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FP}$ | 60 | 8000 | 60 | 8000 | ns |
| $t_{w(REFH)}$ | $\overline{REF}$ high pulse width | $t_{FI}$ | 30 | | 30 | | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FSR}$ | 30 | | 30 | | ns |
| $t_{su(REF-RAS)}$ | $\overline{REF}$ pulse setup time before $\overline{RAS}$ | $t_{FRD}$ | 250 | | 295 | | ns |

## Self-Refresh Cycle

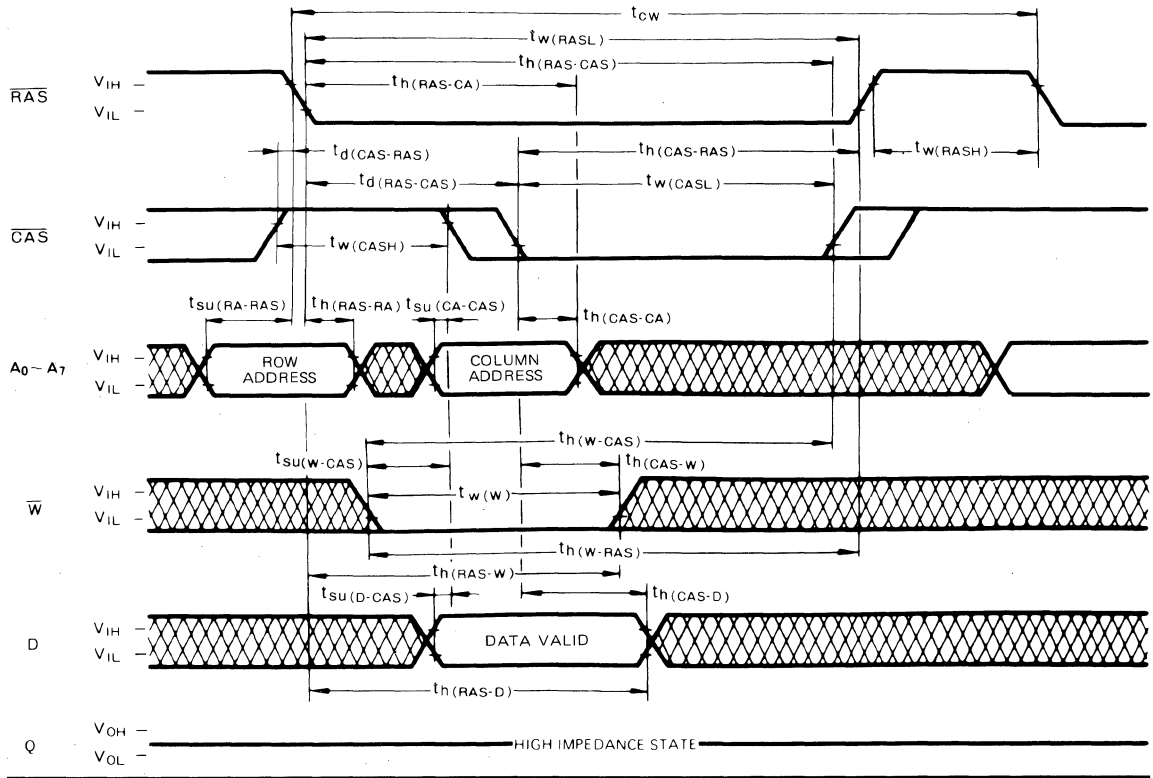
| Symbol | Parameter | Alternative Symbol | M5K4164AP-12 Limits Min | M5K4164AP-12 Limits Max | M5K4164AP-15 Limits Min | M5K4164AP-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FBP}$ | 8000 | ∞ | 8000 | ∞ | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FBR}$ | 310 | | 345 | | ns |

## TIMING DIAGRAMS (Note 18)

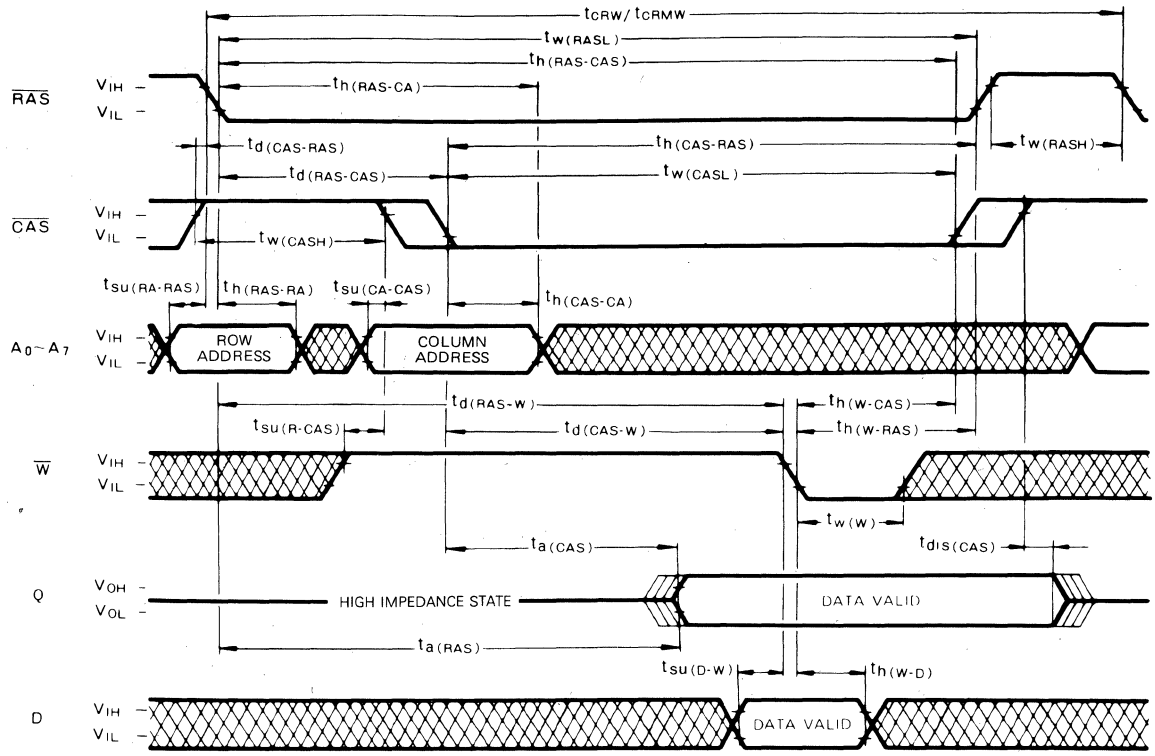
### Read Cycle



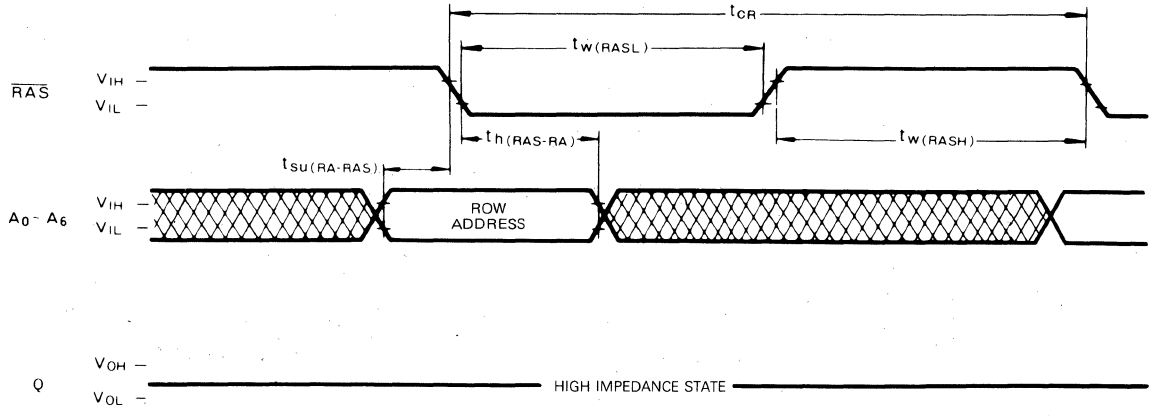

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)



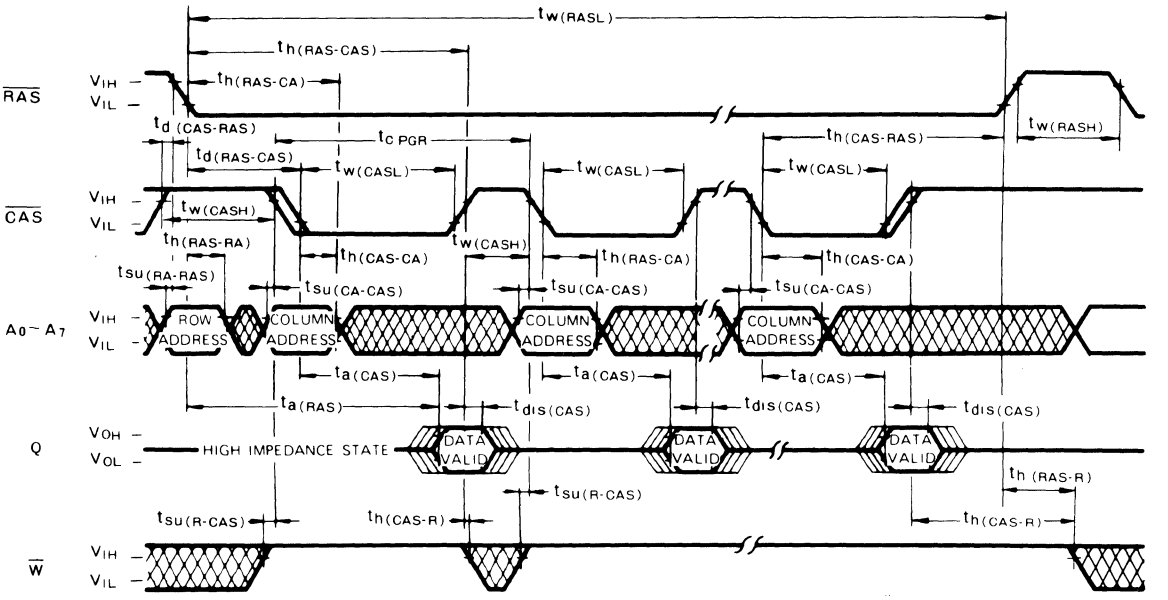

Note 18

Indicates the don't care input

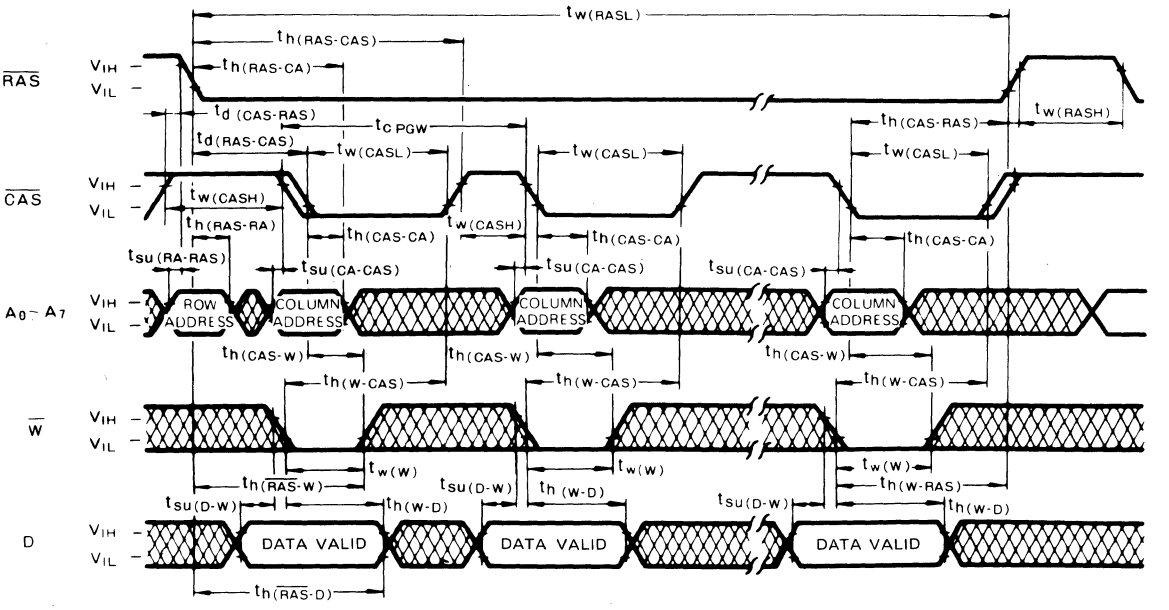
The center-line indicates the high-impedance state

Note 19. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

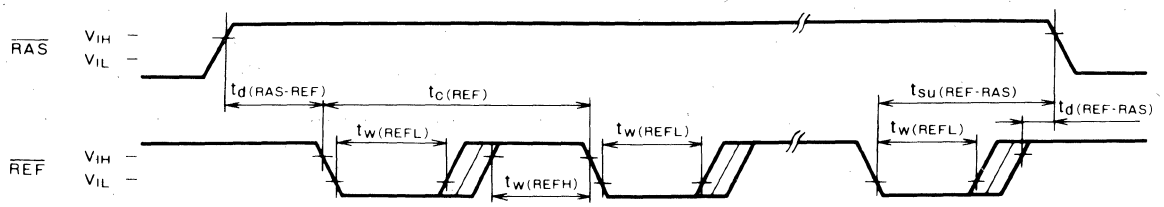
## Page-Mode Read Cycle



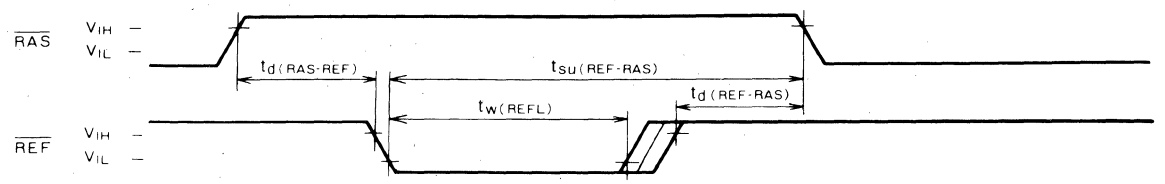

## Page-Mode Write Cycle



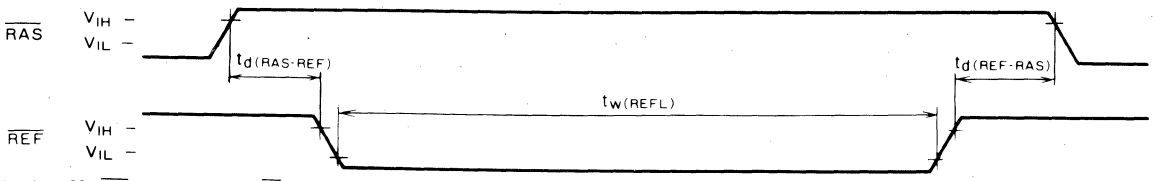
## Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 20)




## Automatic Pulse Refresh Cycle (Single Pulse) (Note 20)

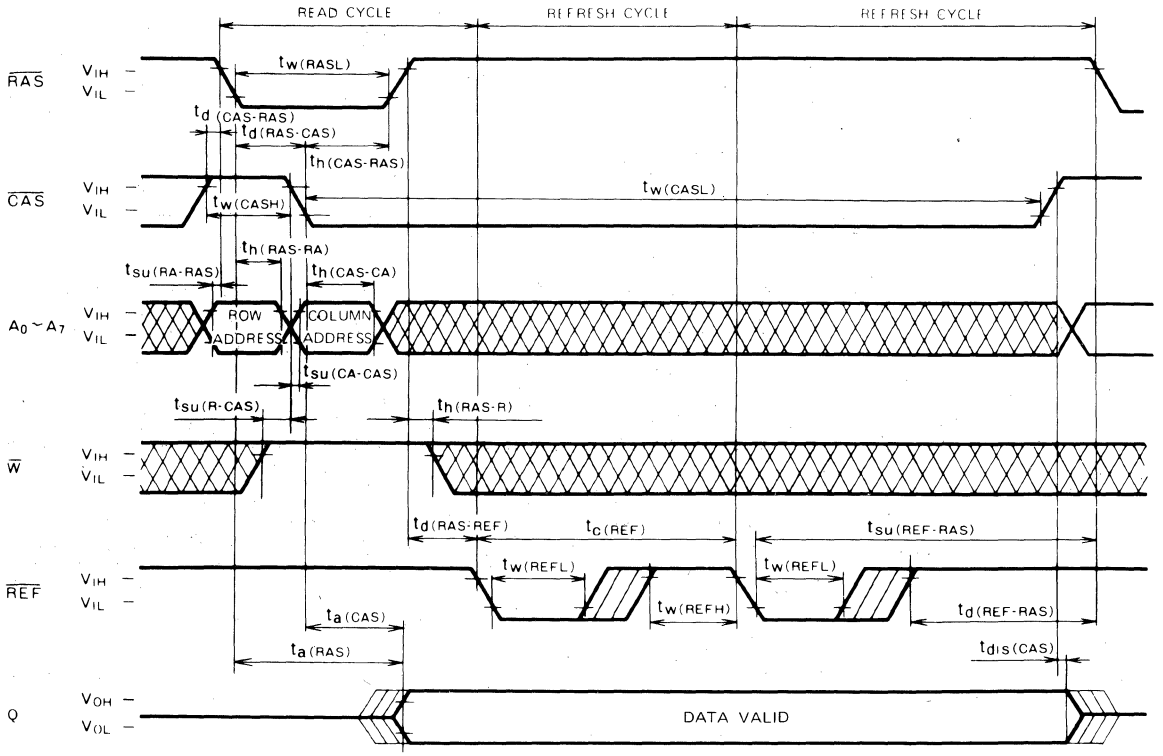



## Self-Refresh Cycle (Note 20)




Note 20: $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

## Hidden Automatic Pulse Refresh Cycle



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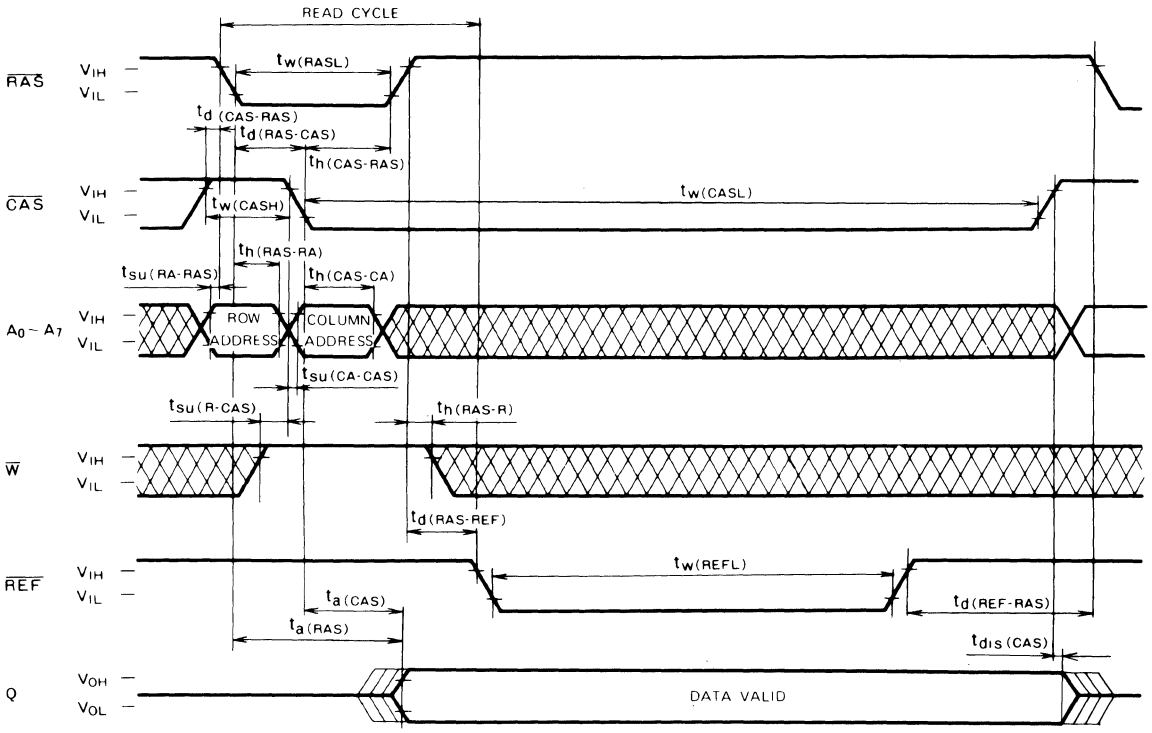
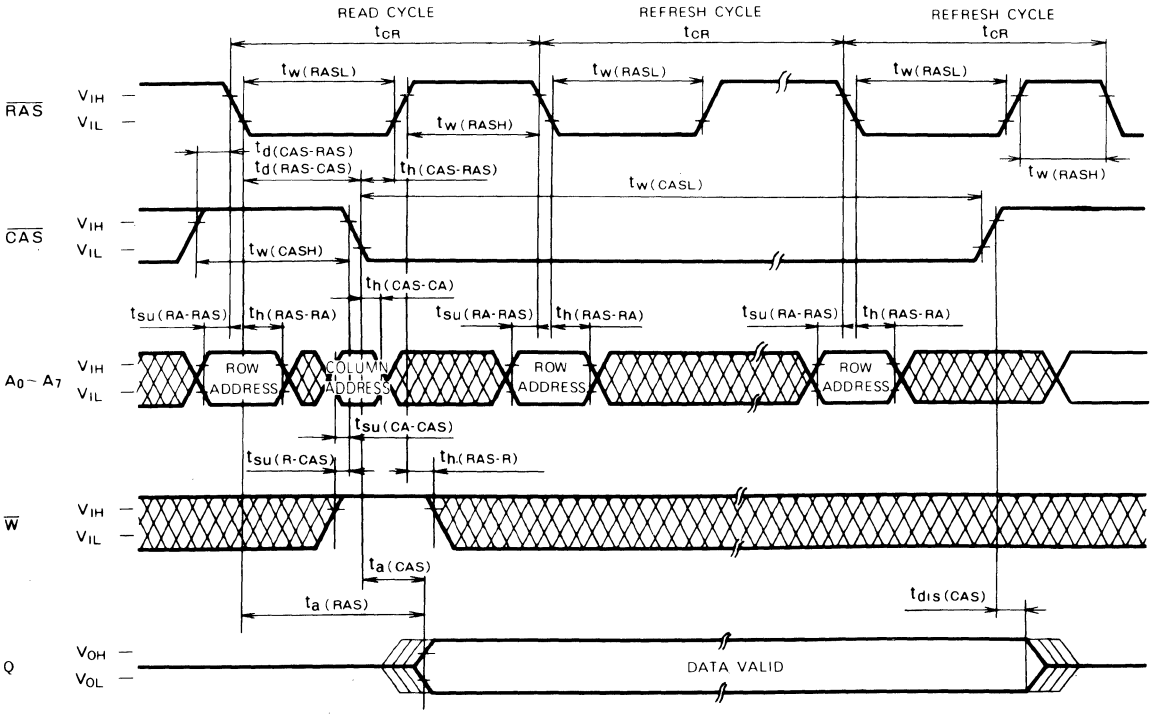
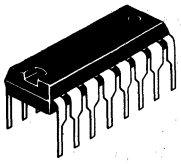
## Hidden Self-Refresh Cycle (Note 21)




Note 21: If the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect).

## Hidden Refresh Cycle (Note 19)





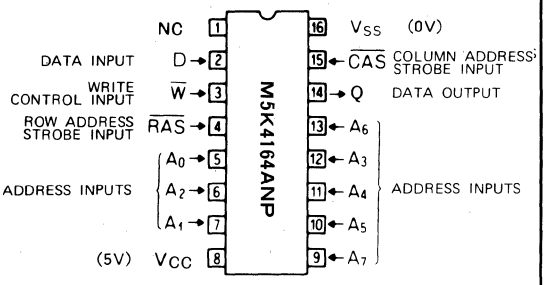
# M5K4164ANP-12, -15

## 65 536-BIT (65 536-WORD BY 1-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. The M5K4164ANP operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P4**

## FEATURES

- High speed

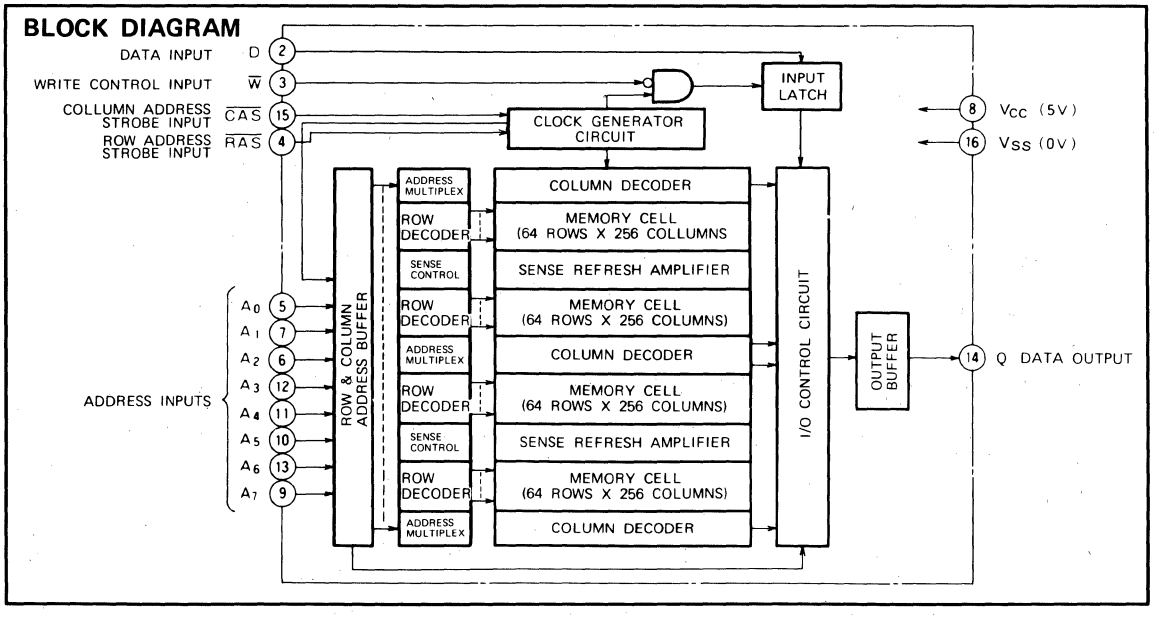
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164ANP-12 | 120 | 220 | 175 |
| M5K4164ANP-15 | 150 | 260 | 150 |

- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation: 300mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$
- Interchangeable with Mostek's MK4564 and Motorola's MCM6665 in pin configuration

## APPLICATION

- Main memory unit for computers

## BLOCK DIAGRAM



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## FUNCTION

The M5K4164ANP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical except refresh is NO. |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| RAS-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65536 memory cells in the M5K4164ANP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5K4164ANP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164ANP, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164ANP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164ANP are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A feature of the M5K4164ANP is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164ANP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164ANP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164ANP operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note. 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note. 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164ANP-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 50 | mA |
| | | M5K4164ANP-15 | $t_{CR}$＝$t_{CW}$＝min output open | | | 45 | |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164ANP-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ | | | 40 | mA |
| | | M5K4164ANP-15 | $t_{C(\overline{REF})}$＝min, output open | | | 35 | |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164ANP-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling | | | 40 | mA |
| | | M5K4164ANP-15 | $t_{CPG}$＝min, output open | | | 35 | |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_I$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_I$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtair ed with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-12 Limits | | M5K4164ANP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | ∞ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 90 | | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | 3 | 35 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$max is specified reference point only;if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-12 Limits | | M5K4164ANP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 10 | | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-12 Limits | | M5K4164ANP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 90 | | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-12 Limits | | M5K4164ANP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 245 | | 295 | | |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 265 | | 310 | | |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 100 | | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 40 | | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | 0 | | |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 100 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RAS\,H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

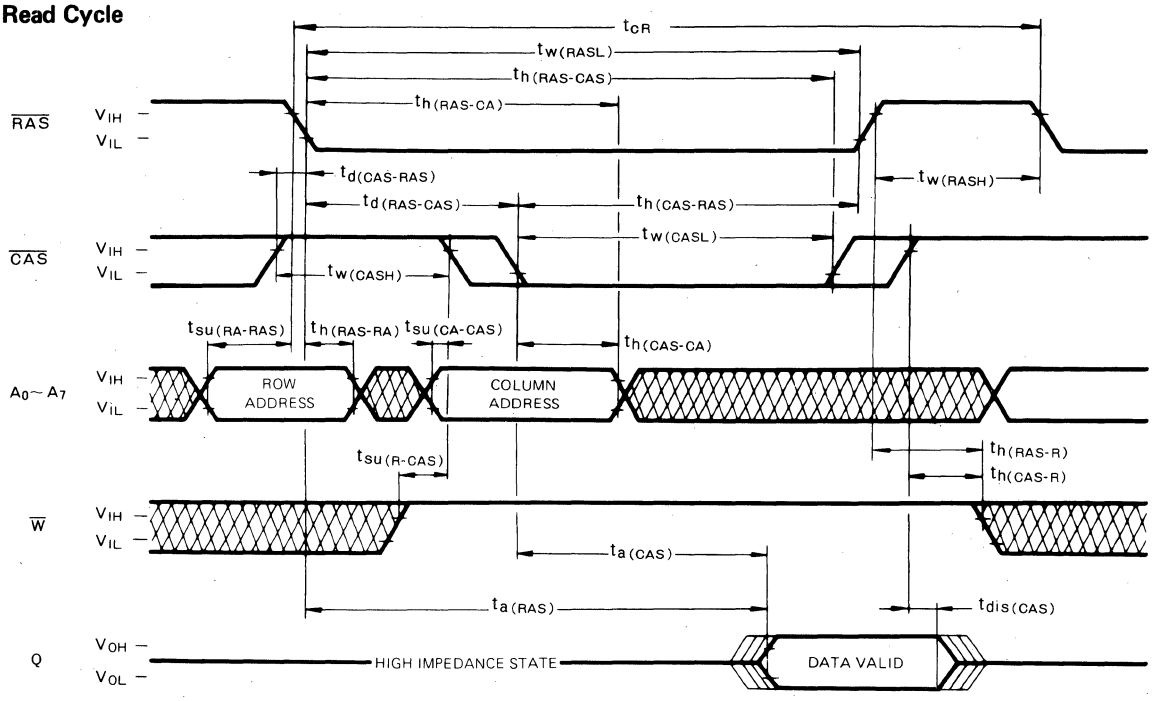
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

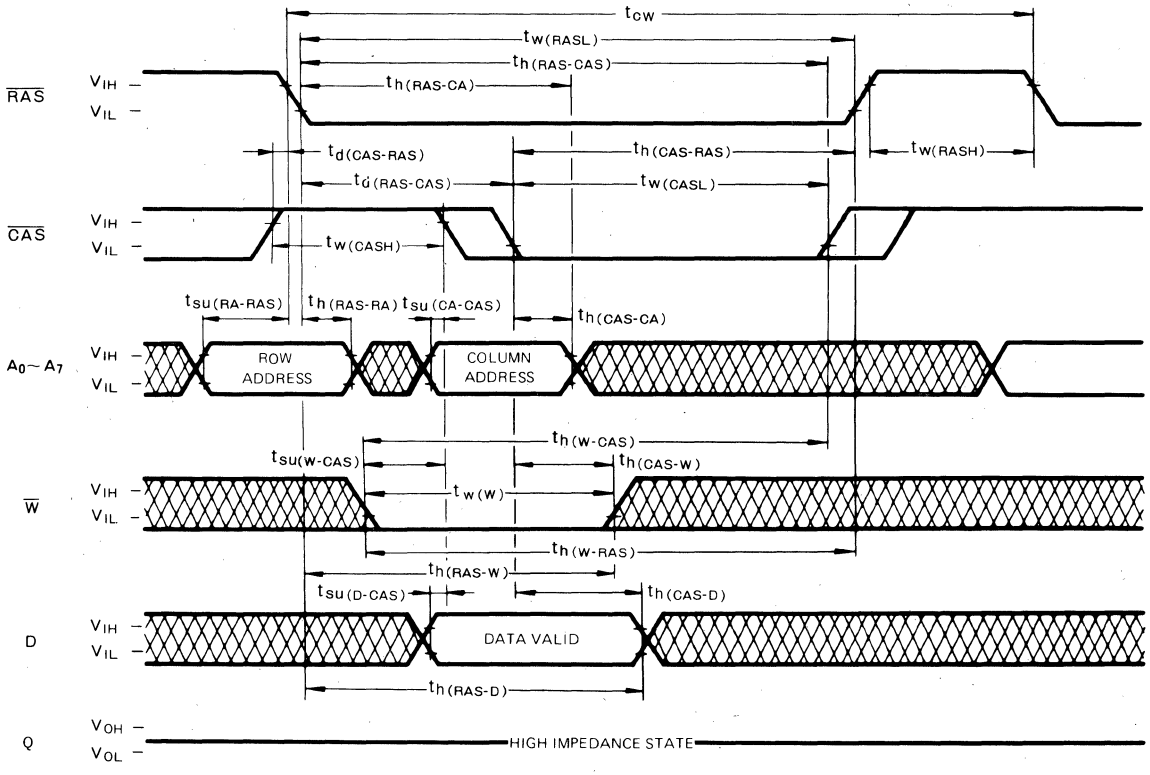
| Symbol | Parameter | Alternative Symbol | M5K4164ANP-12 Limits | | M5K4164ANP-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{c\,PGR}$ | Page-mode read cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{c\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{c\,PGRW}$ | Page-Mode read-write cycle time | — | 150 | | 180 | | ns |
| $t_{c\,PGRMW}$ | Page-Mode read-modify-write cycle time | — | 170 | | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | ns |

## TIMING DIAGRAMS (Note 18)

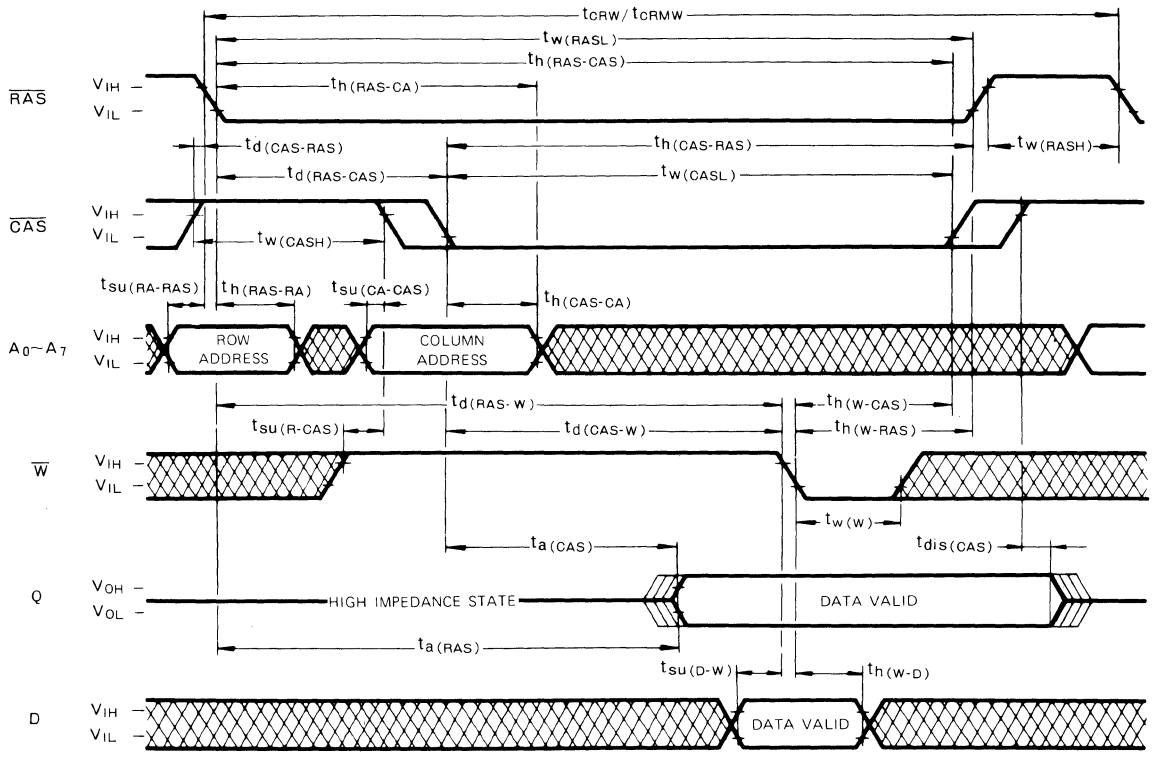
### Read Cycle



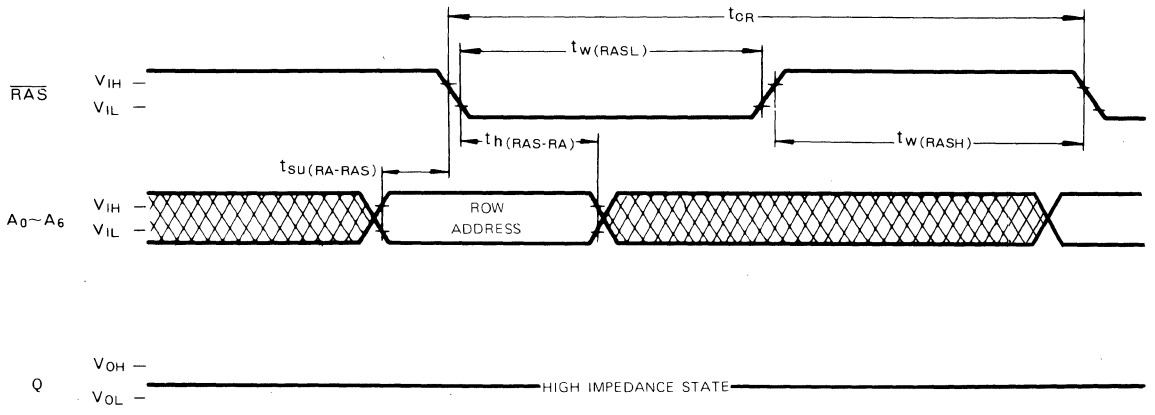

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)



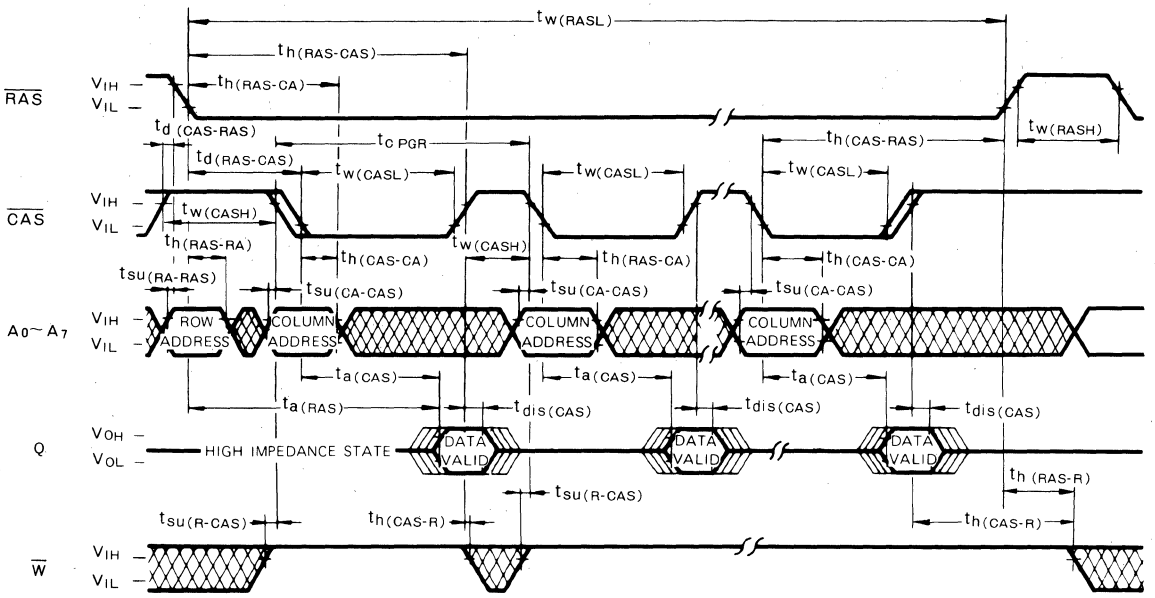

Note 18

Indicates the don't care input

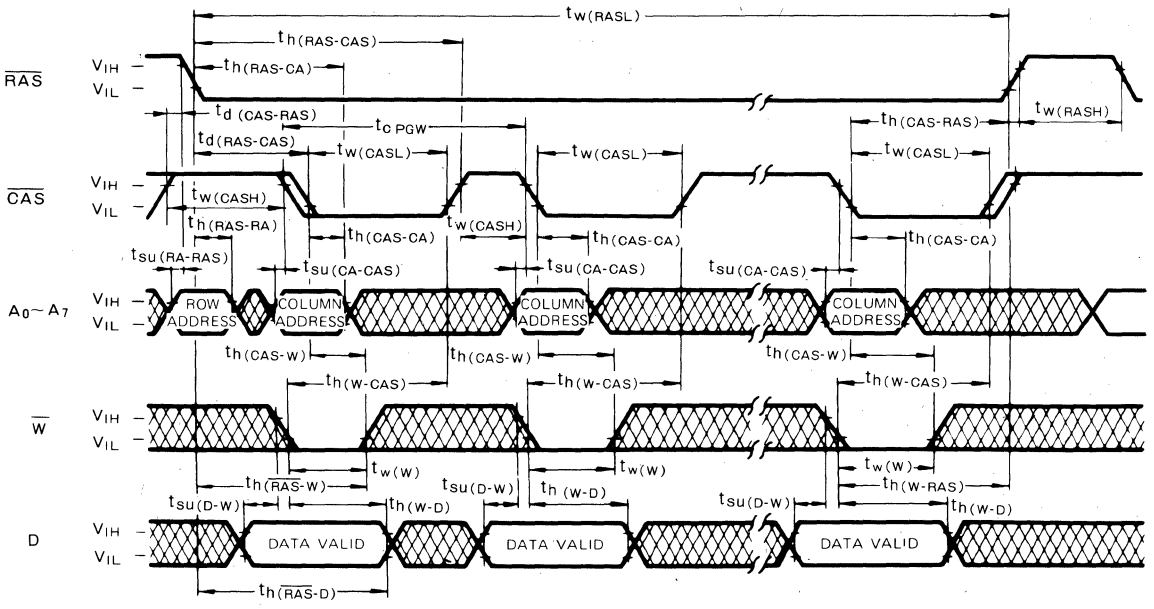
The center-line indicates the high-impedance state

Note 19. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

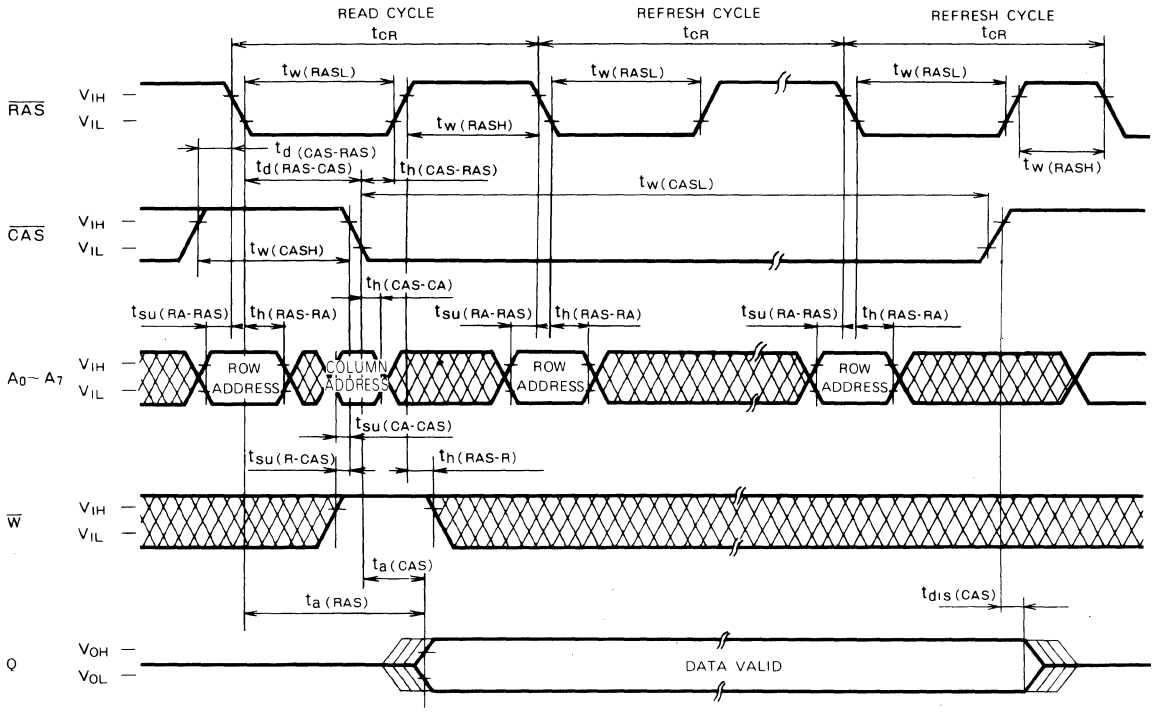
## Page-Mode Read Cycle




## Page-Mode Write Cycle

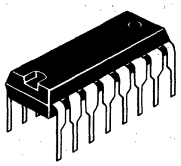


## Hidden Refresh Cycle



# M5K4164ANP-20

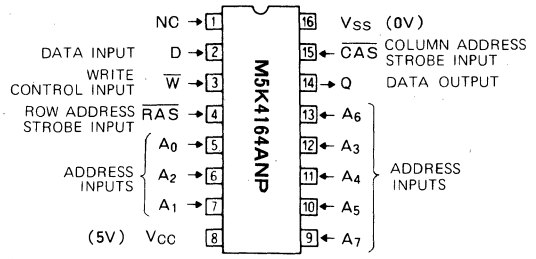
## 65536-BIT (65536-WORD BY 1-BIT) DYNAMIC RAM



## DESCRIPTION

This is a family of 65536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. The M5K4164ANP operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P4**

## FEATURES

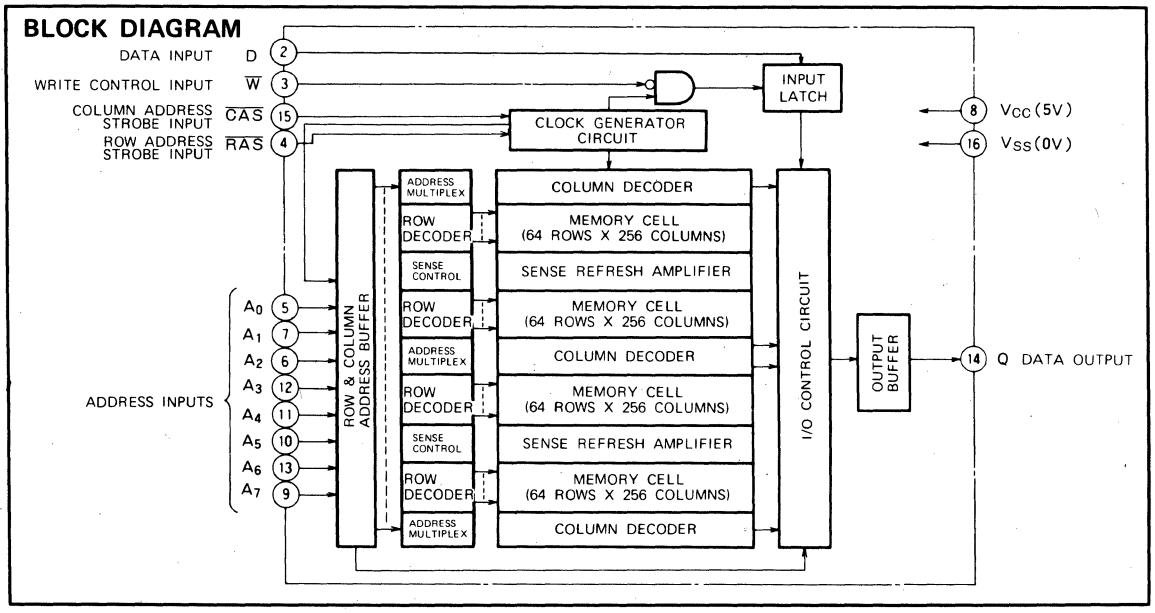
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164ANP-20 | 200 | 330 | 125 |

- Single 5V±20/ supply
- Low standby power dissipation: 22.0 mW (max)
- Low operating power dissipation: 225 mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-stage and directly TTL-compatible
- 128 refresh cycles every 2ms
  (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh.
- Output data can be held infinitely by $\overline{CAS}$.
- Interchangeable with intel's 2164 and Motorola's MCM 6665 in pin configuration.

## APPLICATION

- Main memory unit for computers.

## BLOCK DIAGRAM



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## FUNCTION

The M5K4164ANP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical except refresh is NO. |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65536 memory cells in the M5K4164ANP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of W input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5K4164ANP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164ANP which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2. Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164ANP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164ANP are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A features of the M5K4164ANP is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164ANP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164ANP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164ANP operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | $V_{CC}+1$ | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating $0V \leqq V_{OUT} \leqq 5.5V$ | −10 | | 10 | μA |
| $I_I$ | Input current | | $0V \leqq V_{IN} \leqq 6.5V$, All other pins＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164ANP-20 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}=t_{CW}$＝min output open | | | 40 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}=V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164ANP-20 | $\overline{RAS}$ cycling $\overline{CAS}=V_{IH}$ $t_{C(\overline{REF})}$＝min, output open | | | 30 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164ANP-20 | $\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$＝min, output open | | | 30 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I=V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O=V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-20 Limits Min | M5K4164ANP-20 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 100 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 120 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$)
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$max is specified reference point only;if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(tTLH)} + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-20 Limits Min | M5K4164ANP-20 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-20 Limits Min | M5K4164ANP-20 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 120 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 55 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 120 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164ANP-20 Limits Min | M5K4164ANP-20 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 340 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time. | (Note 16) | $t_{RMWC}$ | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write. | | $t_{RWL}$ | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 150 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 80 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 200 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,\text{min} = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{W(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,\text{min} = t_{a(RAS)}\text{max} + t_{h(W-RAS)} + t_{W(RAS\,H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\text{min}$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\text{min}$ and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\text{min}$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

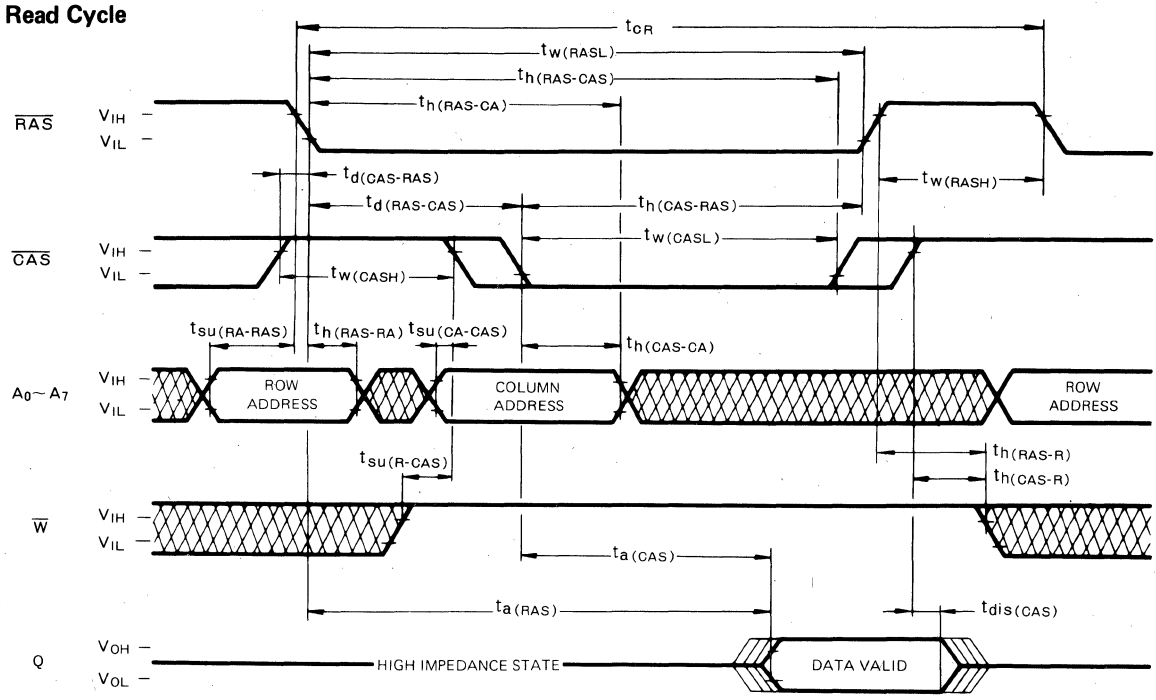
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

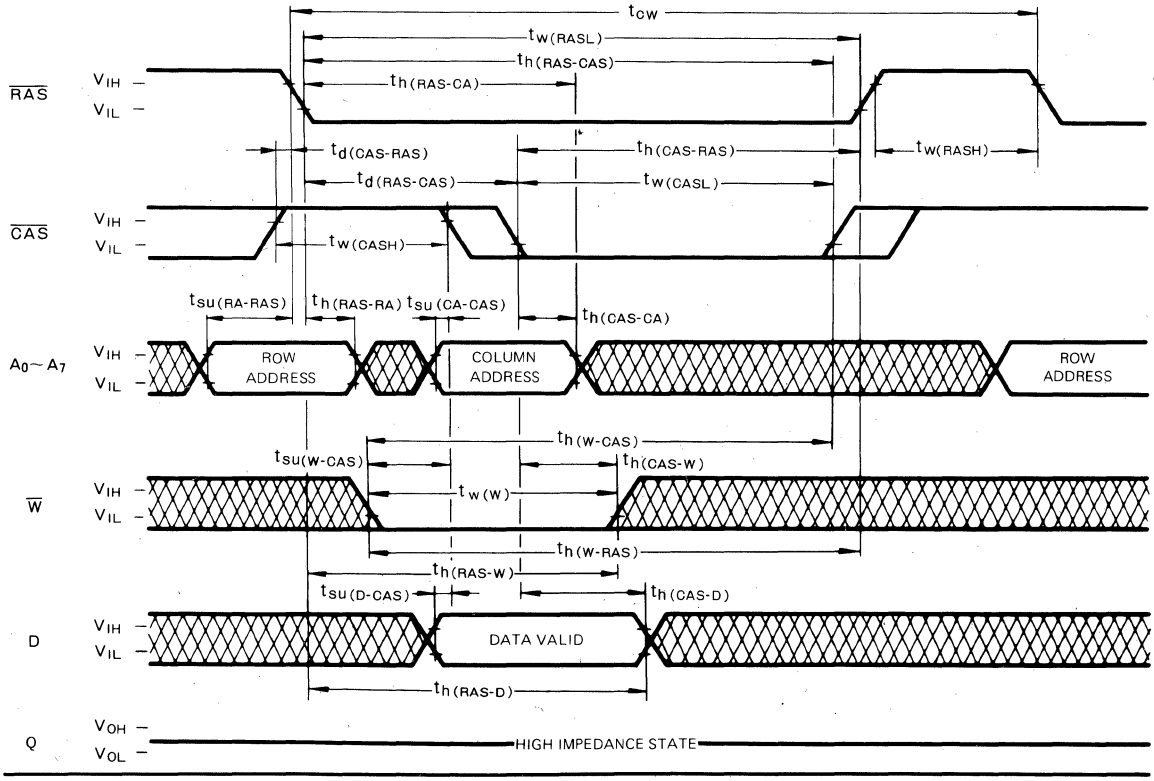
| Symbol | Parameter | Alternative Symbol | M5K4164ANP-20 Limits Min | M5K4164ANP-20 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{C\,PGR}$ | Page-mode read cycle time | $t_{PC}$ | 190 | | ns |
| $t_{C\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 190 | | ns |
| $t_{C\,PGRW}$ | Page-Mode read-write cycle time | — | 230 | | ns |
| $t_{C\,PGRMW}$ | Page-Mode read-modify-write cycle time | — | 245 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 80 | | ns |

## TIMING DIAGRAMS (Note 18)

### Read Cycle




### Write Cycle (Early Write)



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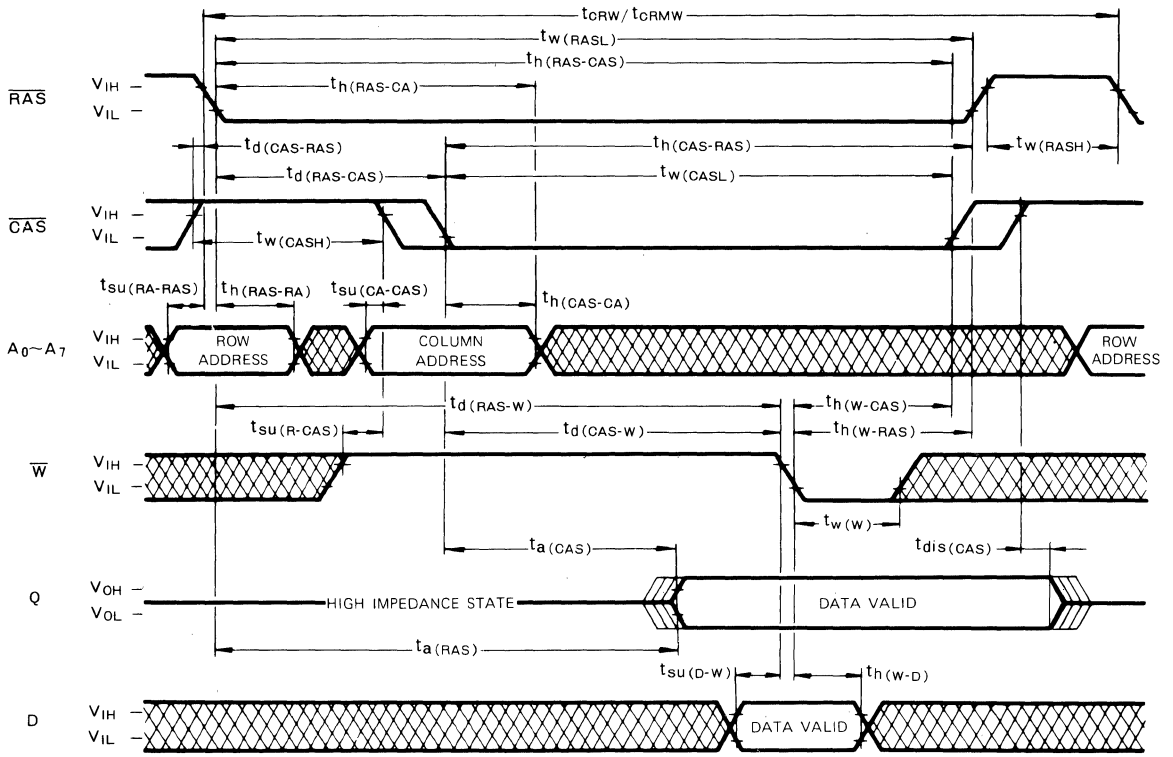
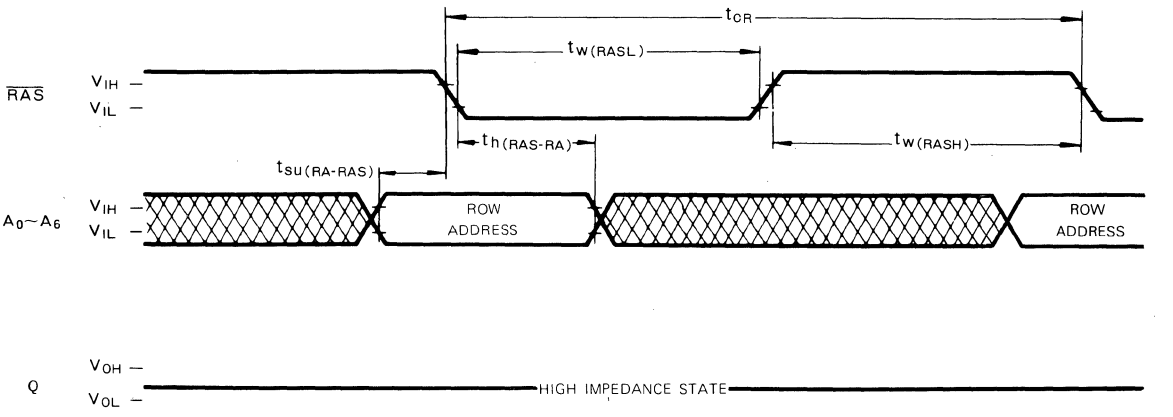
## Read-Write and Read-Modify-Write Cycles

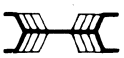



## RAS-Only Refresh Cycle (Note 19)




Note 18

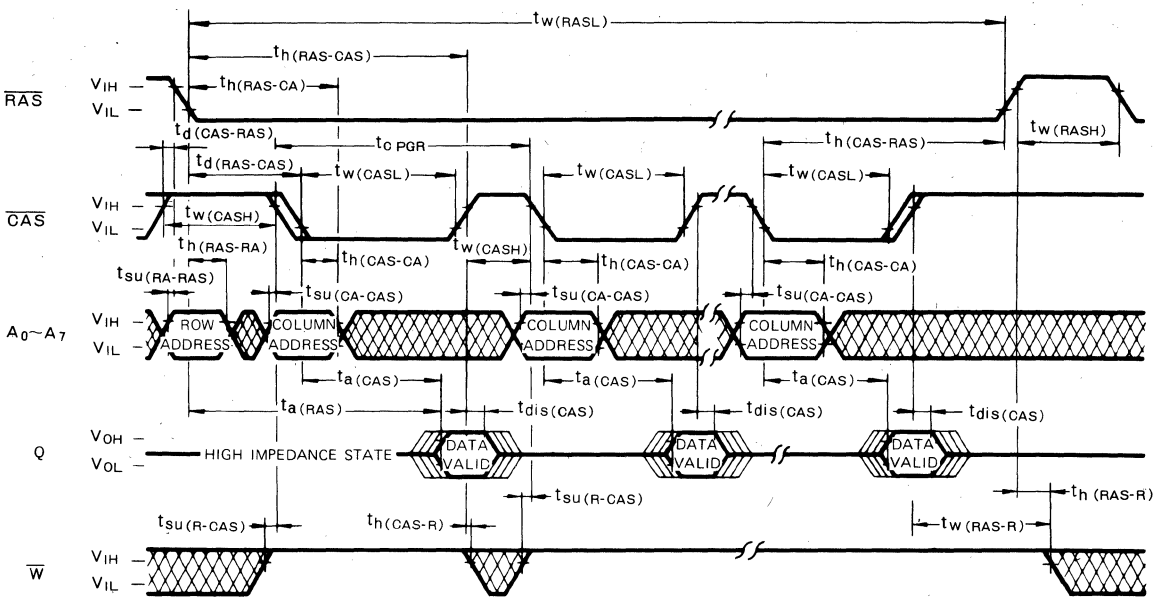
Indicates the don't care input



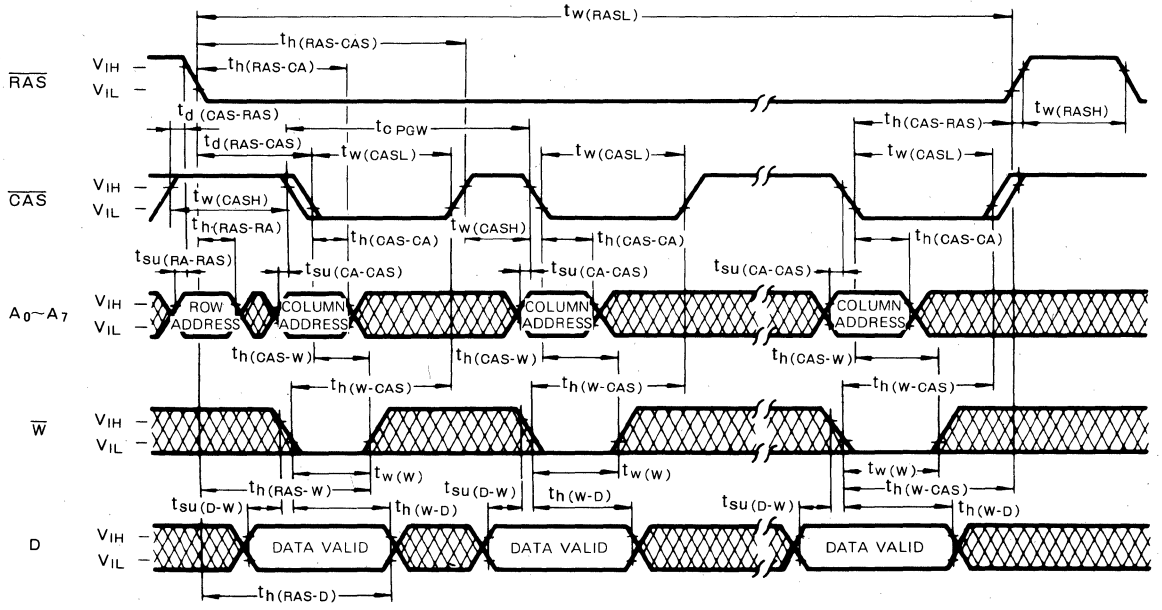
The center-line indicates the high-impedance state

Note 19. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

## Page-Mode Read Cycle




## Page-Mode Write Cycle



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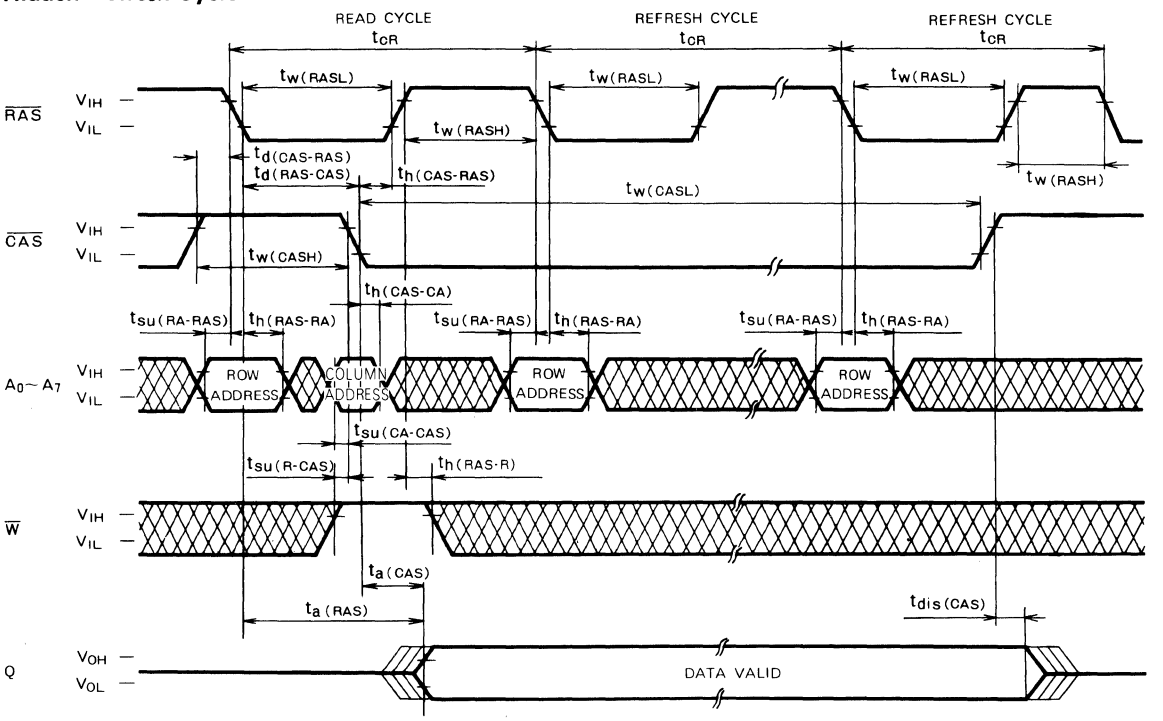
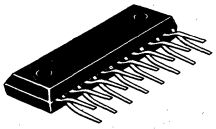
## Hidden Refresh Cycle



# M5K4164AL-12, -15

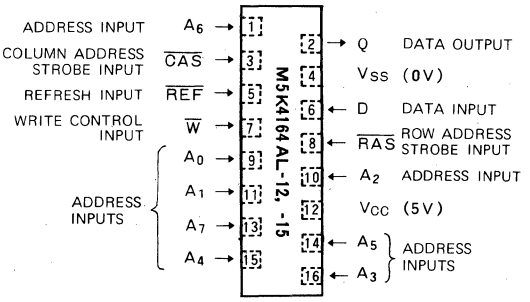
## 65 536-BIT (65 536-WORD BY 1-BIT) DYNAMIC RAM



## DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16-pin zigzag inline package configuration and an increase in system densities. The M5K4164AL operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P5A**

## FEATURES

- High speed

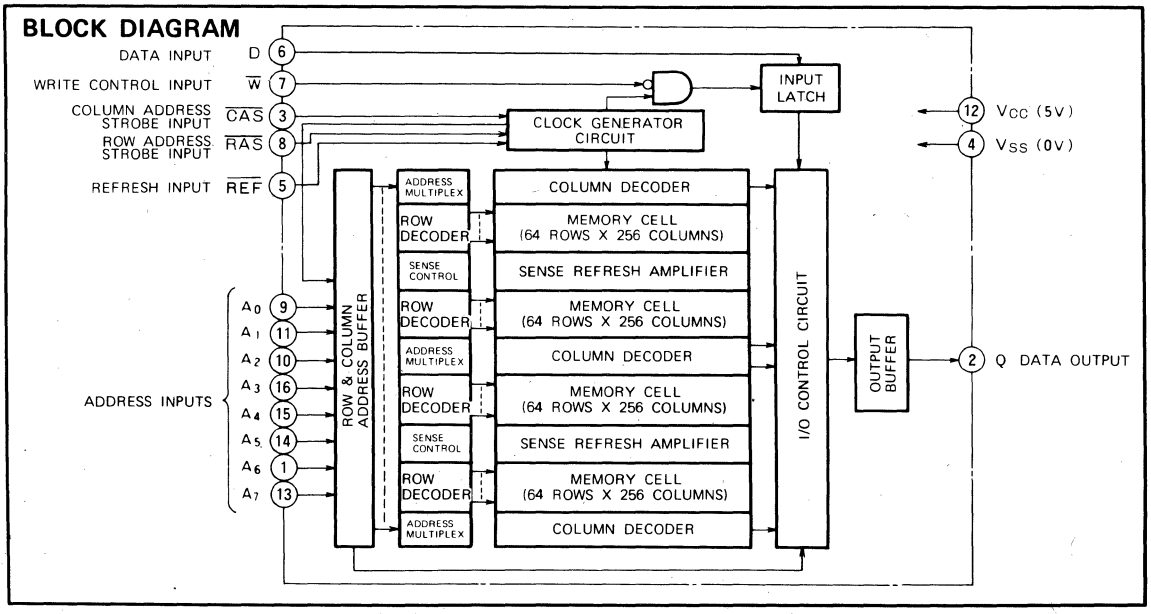
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164AL-12 | 120 | 220 | 175 |
| M5K4164AL-15 | 150 | 260 | 150 |

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  M5K4164AL-12 275mW (max)
  M5K4164AL-15 250mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms
  (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$

## APPLICATION

- Main memory unit for computers
- Refresh memory for CRT

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## FUNCTION

The M5K4164AL provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | $\overline{REF}$ | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | NAC | VLD | YES | Page mode identical. |
| Write (Early write) | ACT | ACT | ACT | VLD | APD | APD | NAC | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | NAC | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | NAC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | NAC | VLD | YES | |
| Automatic refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Self refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Hidden automatic refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Hidden self refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | NAC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65 536 memory cells in the M5K4164AL the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Date to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5K4164AL is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164AL, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2. Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164AL must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164AL are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Automatic Refresh**

Pin 5 ($\overline{REF}$) has two special functions. The M5K416AL has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is applied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

**4. Self-Refresh**

The other function of pin 5 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the M5K4164AL will refresh itself. This internal sequence repeats asynchronously every 12 to 16 $\mu$s. After 2 ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 5 ($\overline{REF}$) refresh function gives the user a feature that is free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx 3M\Omega$) on pin 5, so if the pin 5 ($\overline{REF}$) function is not used, pin 5 may be left open (not connect) without affecting the normal operations.

**5. Hidden Refresh**

A feature of the M5K4164AL is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164AL is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164AL as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164AL operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164AL-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 50 | mA |
| | | M5K4164AL-15 | $t_{CR}$＝$t_{CW}$＝min output open | | | 45 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164AL-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ | | | 40 | mA |
| | | M5K4164AL-15 | $t_{C(REF)}$＝min, output open | | | 35 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164AL-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling | | | 40 | mA |
| | | M5K4164AL-15 | $t_{CPG}$＝min, output open | | | 35 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$, automatic refreshing (Note 3) | M5K4164AL-12 | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$ cycling | | | 40 | mA |
| | | M5K4164AL-15 | $t_{C(REF)}$＝min. output open | | | 35 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, self refreshing | | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$＝$V_{IL}$ output open | | | 8 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_{I(REF)}$ | Input capacitance, $\overline{REF}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164AL-12 Limits Min | M5K4164AL-12 Limits Max | M5K4164AL-15 Limits Min | M5K4164AL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | ∞ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 90 | | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$)
10: Operation within the $t_{d\ (RAS-CAS)}$ max limit insures that $t_{a\ (RAS)}$ max can be met. $t_{d\ (RAS-CAS)}$max is specified reference point only; if $t_{d\ (RAS-CAS)}$ is greater than the specified $t_{d\ (RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d\ (RAS-CAS)min} = t_{h\ (RAS-RA)min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AL-12 Limits Min | M5K4164AL-12 Limits Max | M5K4164AL-15 Limits Min | M5K4164AL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su\ (R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h\ (CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h\ (RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 10 | | 20 | | ns |
| $t_{dis\ (CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a\ (CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a\ (RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 11: Either $t_{h\ (RAS-R)}$ or $t_{h\ (CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis\ (CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13: This is the value when $t_{d\ (RAS-CAS)} \geqq t_{d\ (RAS-CAS)max}$. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d\ (RAS-CAS)} < t_{d\ (RAS-CAS)max}$. When $t_{d\ (RAS-CAS)} \geqq t_{d\ (RAS-CAS)max}$, $t_{a\ (RAS)}$ will increase by the amount that $t_{d\ (RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AL-12 Limits Min | M5K4164AL-12 Limits Max | M5K4164AL-15 Limits Min | M5K4164AL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su\ (W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −5 | | ns |
| $t_{h\ (CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h\ (RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 90 | | 95 | | ns |
| $t_{h\ (W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h\ (W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w\ (W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su\ (D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h\ (CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h\ (RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164AL-12 Limits | | M5K4164AL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 245 | | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 265 | | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 100 | | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 40 | | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RAS\,H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$min, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$min a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | M5K4164AL-12 Limits | | M5K4164AL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C\,PGR}$ | Page-mode read cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{C\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{C\,PGRW}$ | Page-Mode read-write cycle time | — | 150 | | 180 | | ns |
| $t_{C\,PGRMW}$ | Page-Mode read-modify-write cycle time | — | 170 | | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | ns |

## Automatic Refresh Cycle

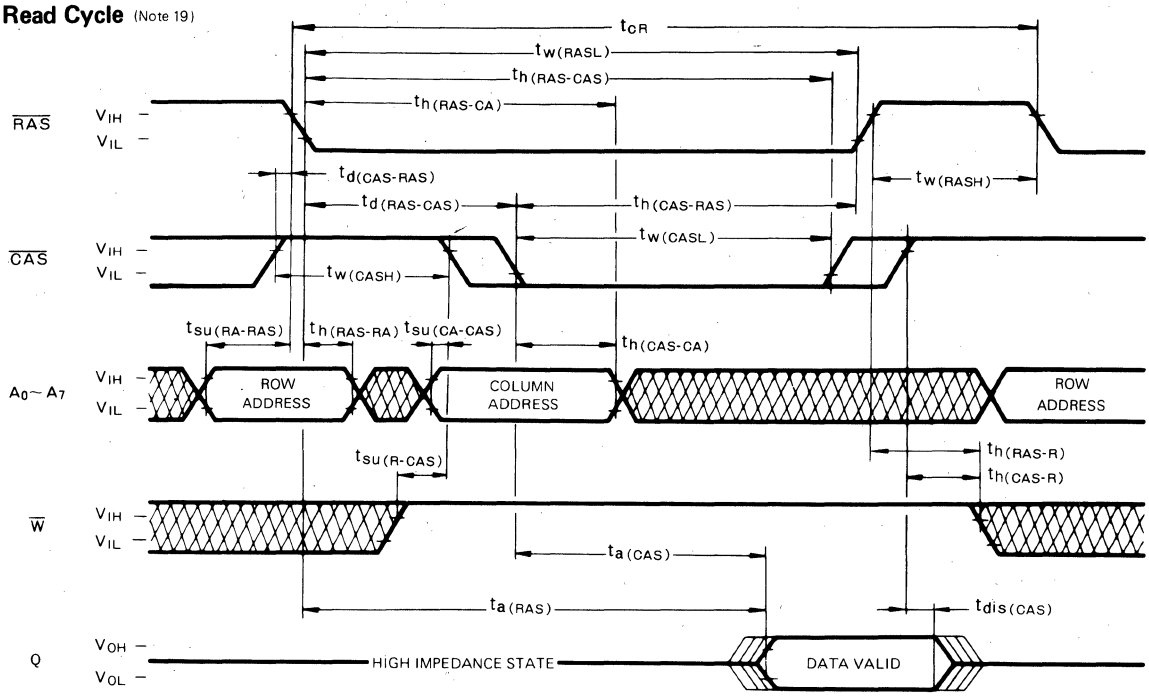
| Symbol | Parameter | Alternative Symbol | M5K4164AL-12 Limits | | M5K4164AL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C(REF)}$ | Automatic Refresh cycle time | $t_{FC}$ | 220 | | 260 | | ns |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FP}$ | 60 | 8000 | 60 | 8000 | ns |
| $t_{w(REFH)}$ | $\overline{REF}$ high pulse width | $t_{FI}$ | 30 | | 30 | | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FSR}$ | 30 | | 30 | | ns |
| $t_{su(REF-RAS)}$ | $\overline{REF}$ pulse setup time before $\overline{RAS}$ | $t_{FRD}$ | 250 | | 295 | | ns |

## Self-Refresh Cycle

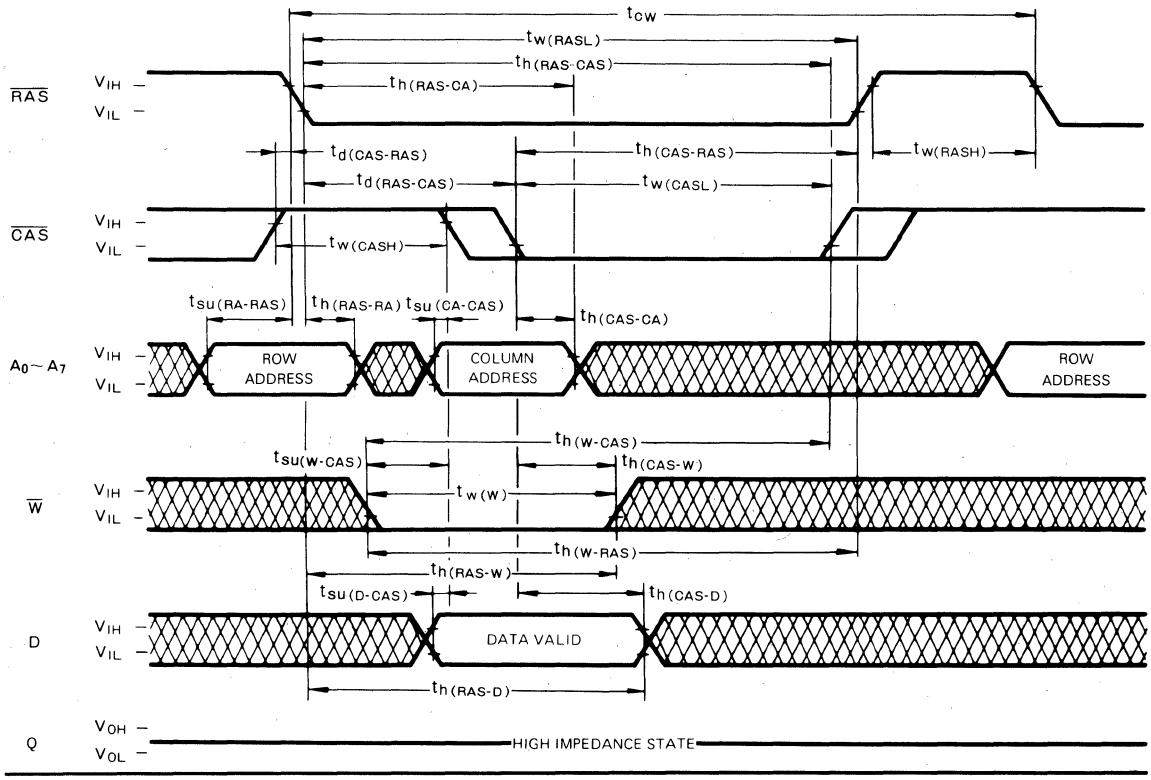
| Symbol | Parameter | Alternative Symbol | M5K4164AL-12 Limits | | M5K4164AL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FBP}$ | 8000 | ∞ | 8000 | ∞ | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FBR}$ | 250 | | 295 | | ns |

## TIMING DIAGRAMS (Note 18)

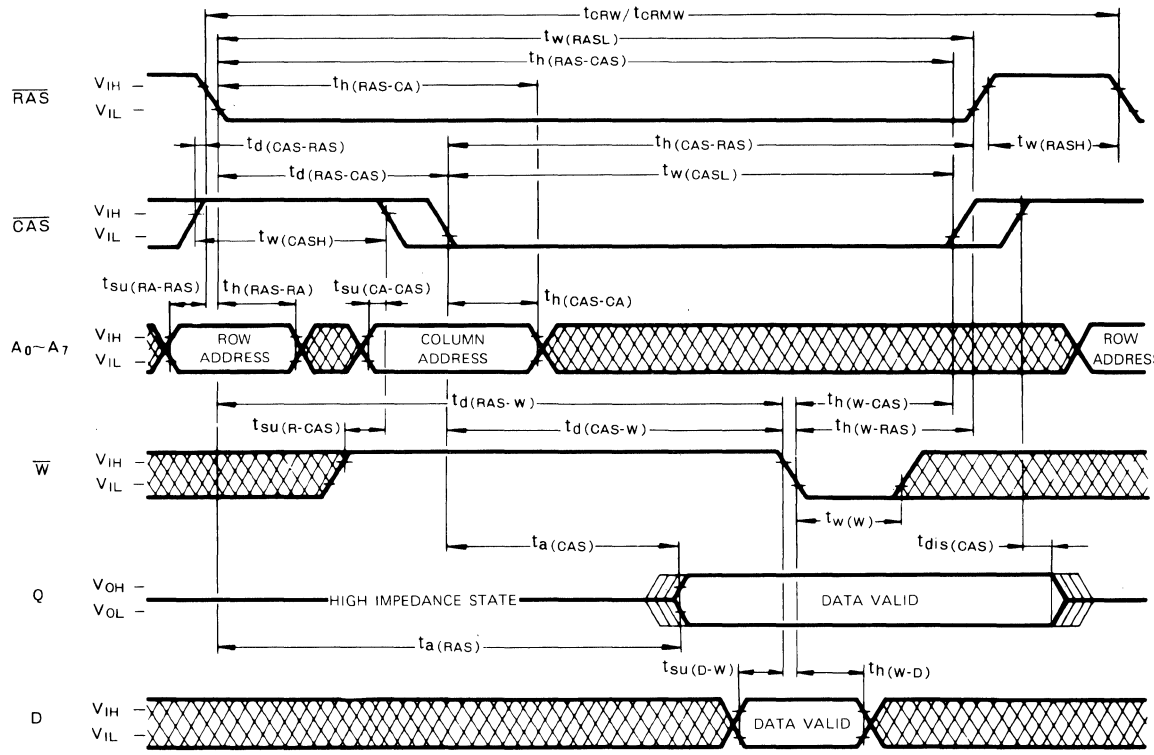
### Read Cycle (Note 19)



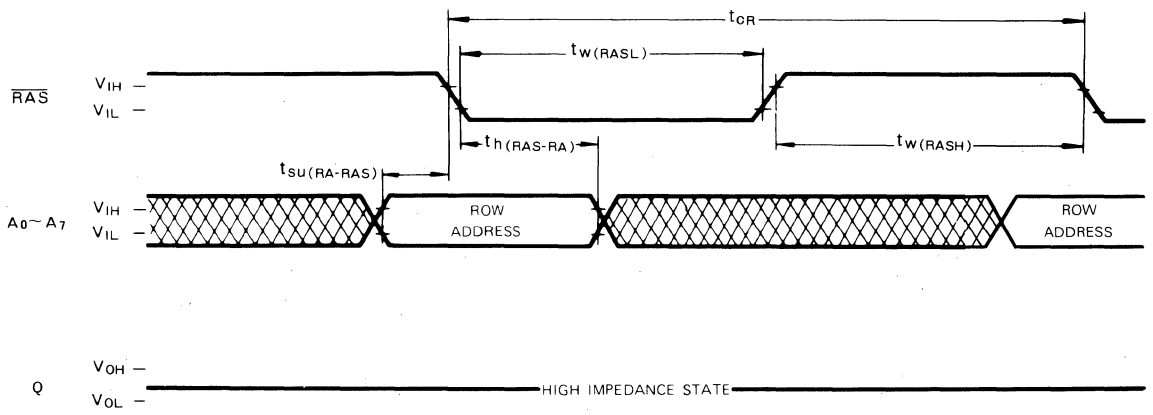

### Write Cycle (Early Write) (Note 19)



## Read-Write and Read-Modify-Write Cycles (Note 19)




## RAS-Only Refresh Cycle (Note 20)



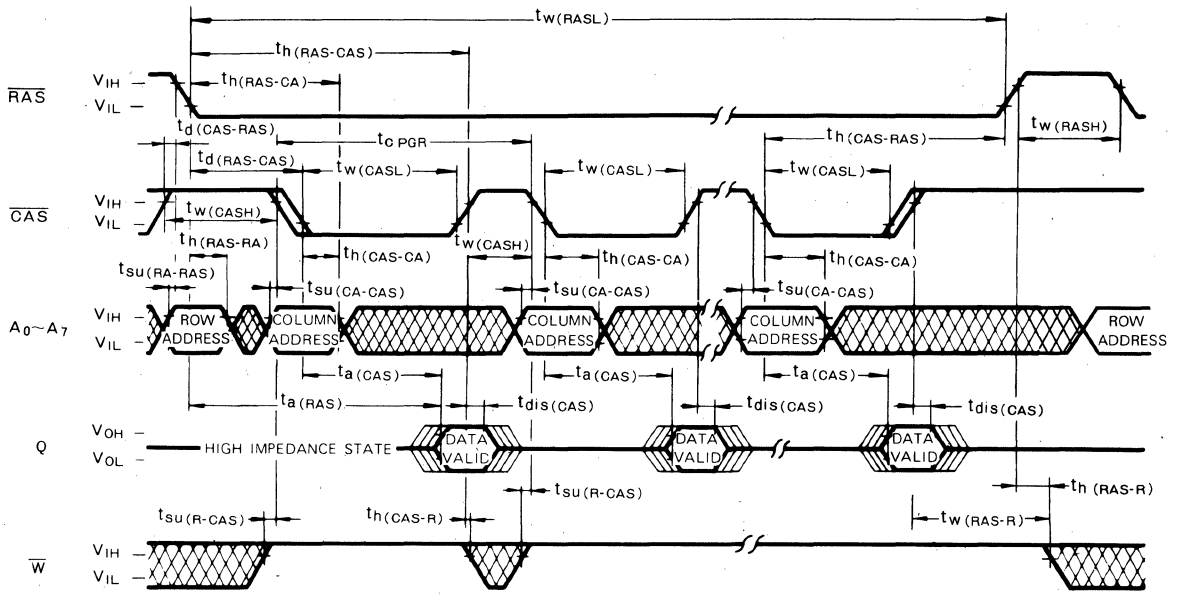

Note 18 Indicates the don't care input

The center-line indicates the high-impedance state

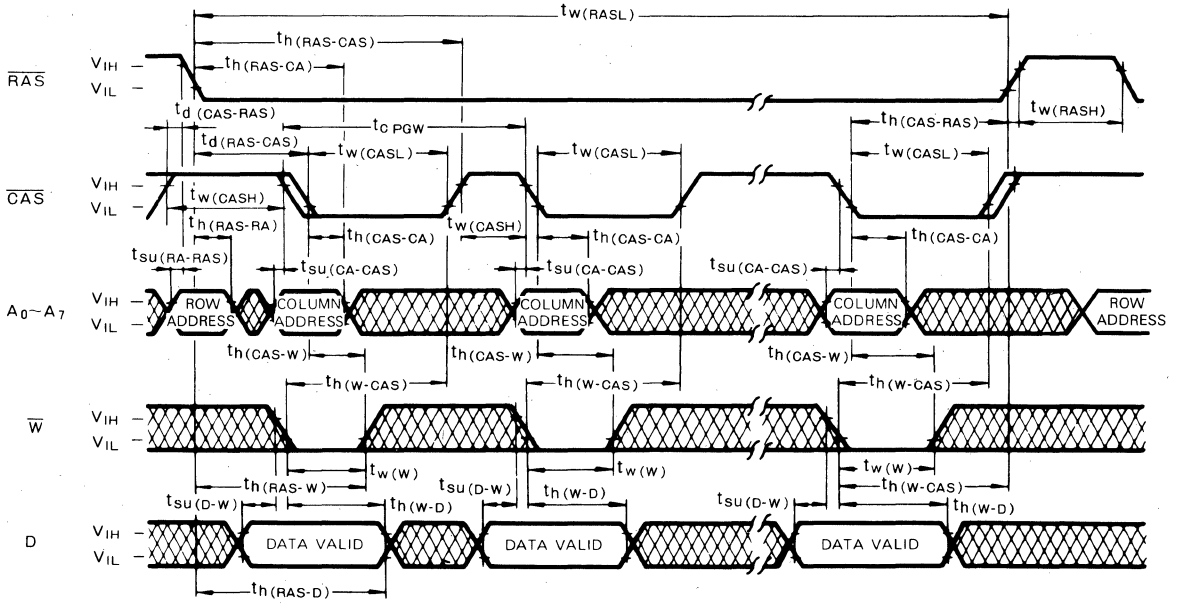
Note 19. $\overline{REF} = V_{IH}$

20. $\overline{CAS} = \overline{REF} = V_{IH}$, $\overline{W}$, D = don't care.
$A_7$ may be $V_{IH}$ or $V_{IL}$.

## Page-Mode Read Cycle (Note 19)



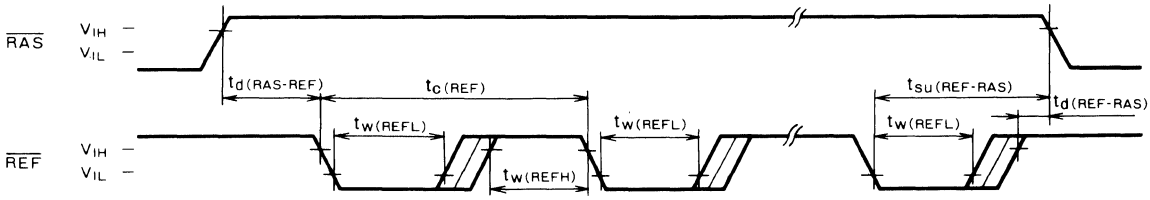

## Page-Mode Write Cycle (Note 19)



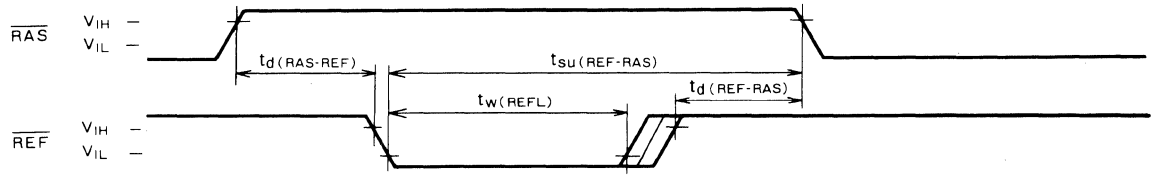


MITSUBISHI ELECTRIC

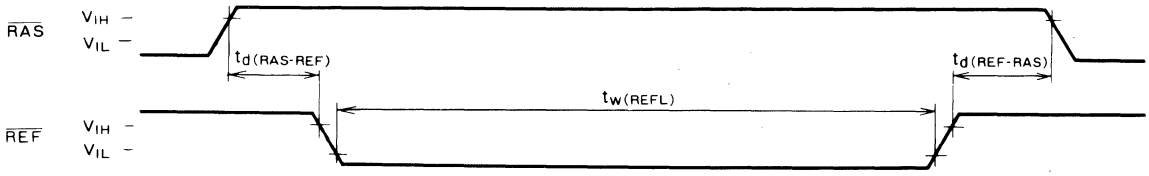
## Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 21)




## Automatic Pulse Refresh Cycle (Single Pulse) (Note 21)

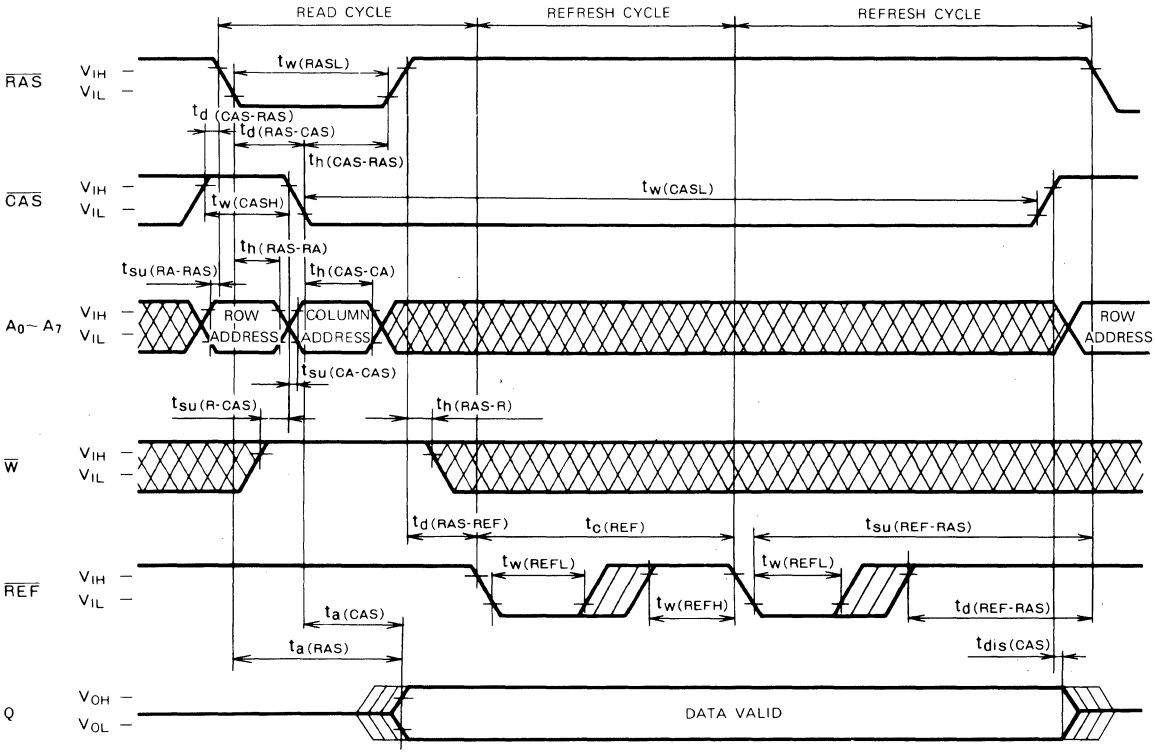



## Self-Refresh Cycle (Note 21)

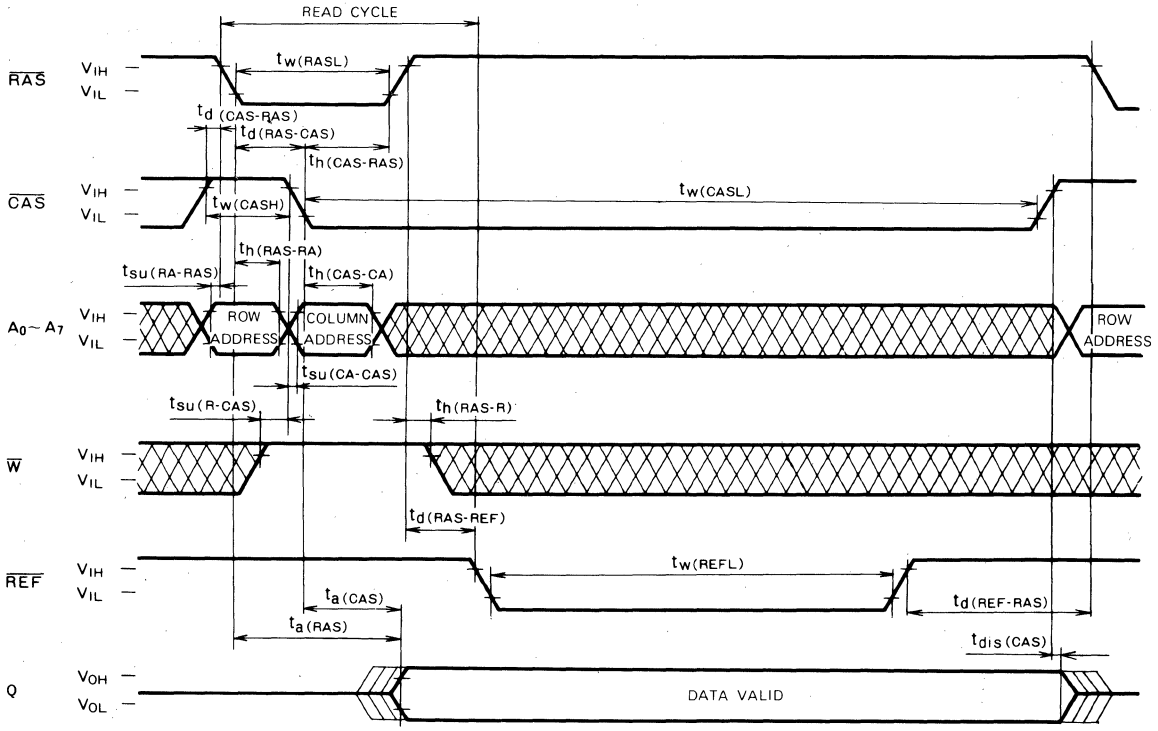



Note 21 $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

## Hidden Automatic Pulse Refresh Cycle

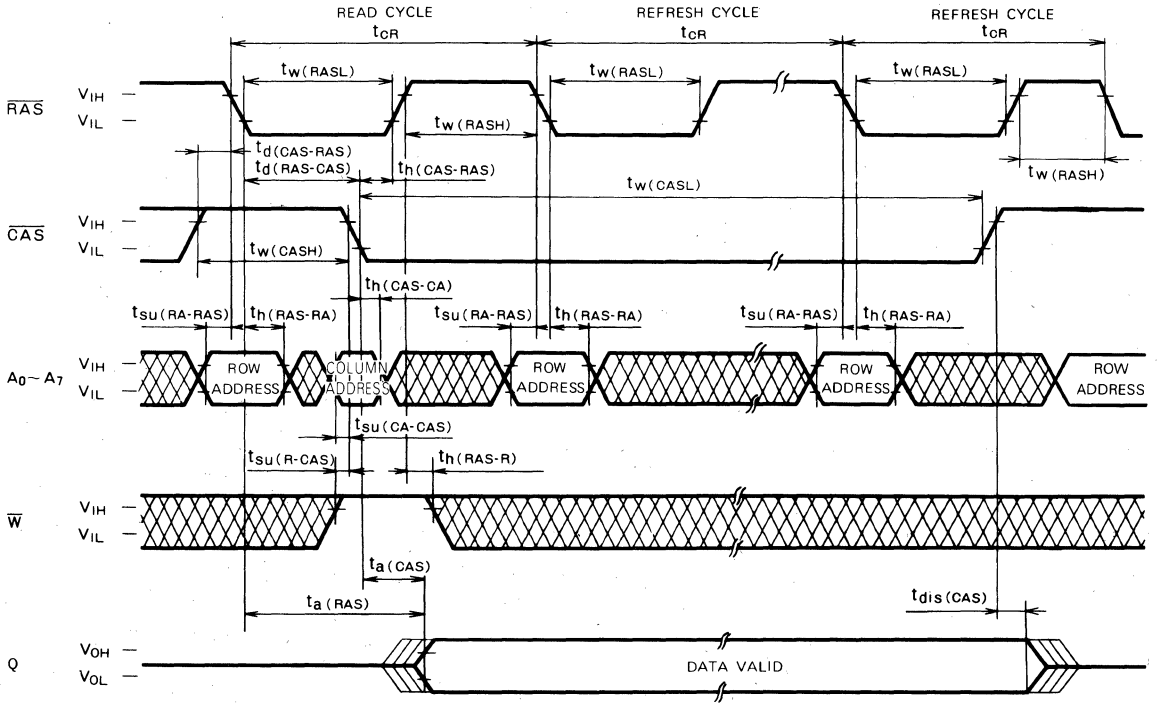


## Hidden Self-Refresh Cycle



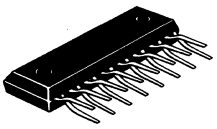

Note 22. If the pin 5 ($\overline{REF}$) function is not used, pin 5 may be left open (not connect).

## Hidden Refresh Cycle (Note 19)



# M5K4164ANL-12, -15

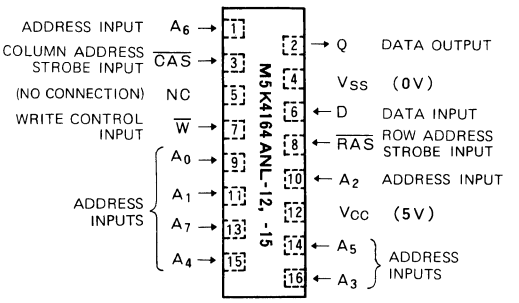
## 65 536-BIT (65 536-WORD BY 1-BIT) DYNAMIC RAM



## DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16-pin zigzag inline package configuration and an increase in system densities. The M5K4164ANL operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P5A**

## FEATURES

- High speed

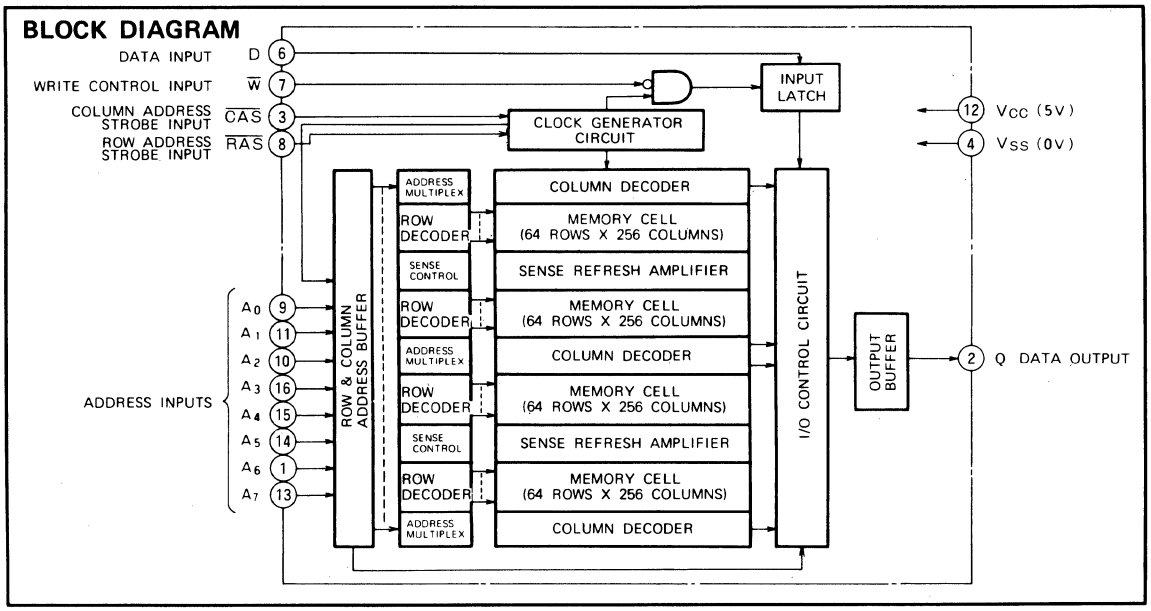
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164ANL-12 | 120 | 220 | 175 |
| M5K4164ANL-15 | 150 | 260 | 150 |

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  M5K4164ANL-12 275mW (max)
  M5K4164ANL-15 250mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms
  (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$

## APPLICATION

- Main memory unit for computers
- Refresh memory for CRT

## BLOCK DIAGRAM



## FUNCTION

The M5K4164ANL provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical. |
| Write (Early write) | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| RAS-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65 536 memory cells in the M5K4164ANL the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\ max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5K4164ANL is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164ANL, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164ANL must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164ANL are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A feature of the M5K4164ANL is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164ANL is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164ANL as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164ANL operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V ± 10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164ANL-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 50 | mA |
| | | M5K4164ANL-15 | $t_{CR}$＝$t_{CW}$＝min output open | | | 45 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164ANL-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ | | | 40 | mA |
| | | M5K4164ANL-15 | $t_{C(\overline{REF})}$＝min, output open | | | 35 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164ANL-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling | | | 40 | mA |
| | | M5K4164ANL-15 | $t_{CPG}$＝min, output open | | | 35 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive; out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164ANL-12 Limits Min | M5K4164ANL-12 Limits Max | M5K4164ANL-15 Limits Min | M5K4164ANL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | ∞ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 90 | | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only, if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL}(t_{TLH}) + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANL-12 Limits Min | M5K4164ANL-12 Limits Max | M5K4164ANL-15 Limits Min | M5K4164ANL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 10 | | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}max$ defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}max$. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}max$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}max$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164ANL-12 Limits Min | M5K4164ANL-12 Limits Max | M5K4164ANL-15 Limits Min | M5K4164ANL-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 90 | | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164ANL-12 Limits | | M5K4164ANL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 245 | | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 265 | | 310 | | ns |
| $th_{(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $th_{(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $tw_{(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $tsu_{(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $td_{(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 100 | | 120 | | ns |
| $td_{(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 40 | | 60 | | ns |
| $tsu_{(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | 0 | | ns |
| $th_{(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | ns |
| $tdis_{(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $ta_{(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $ta_{(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 15: $t_{CRW}min$ is defined as $t_{CRW}min = td_{(RAS-W)} + th_{(W-RAS)} + tw_{(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}$ min $= ta_{(RAS)}max + th_{(W-RAS)} + tw_{(RAS\,H)} + 3t_{TLH(tTHL)}$

17: $tsu_{(W-CAS)}$, $td_{(RAS-W)}$, and $td_{(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $tsu_{(W-CAS)} \geqq tsu_{(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $td_{(RAS-W)} \geqq td_{(RAS-W)}min$, and $td_{(CAS-W)} \geqq tsu_{(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

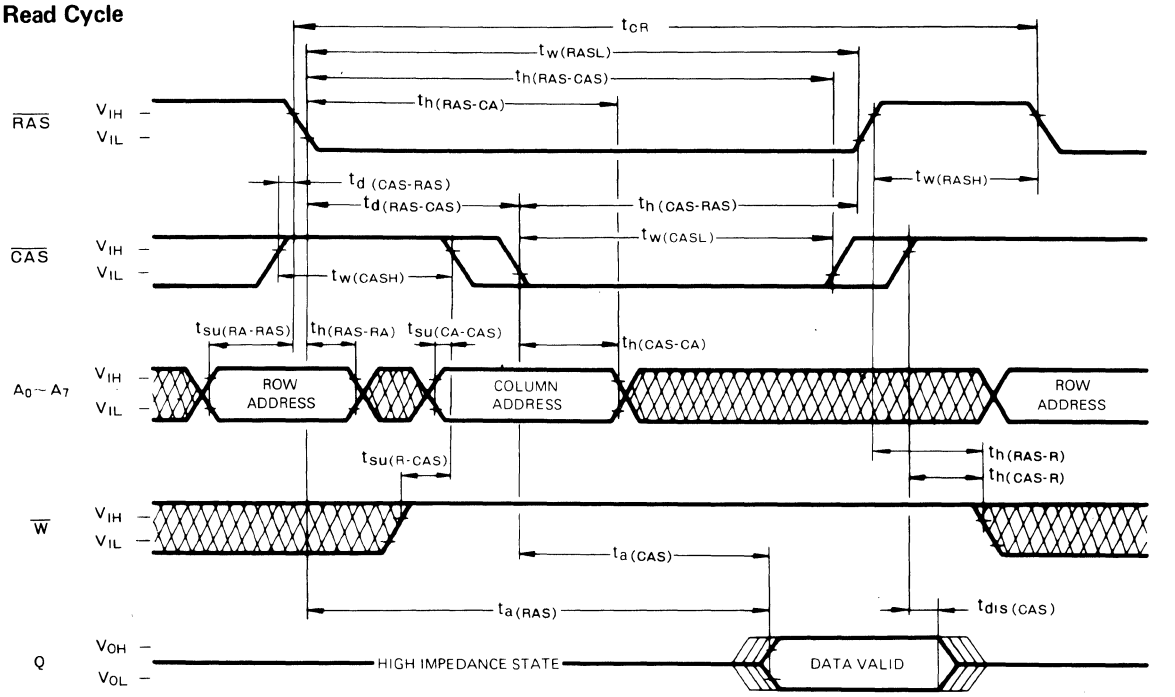
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

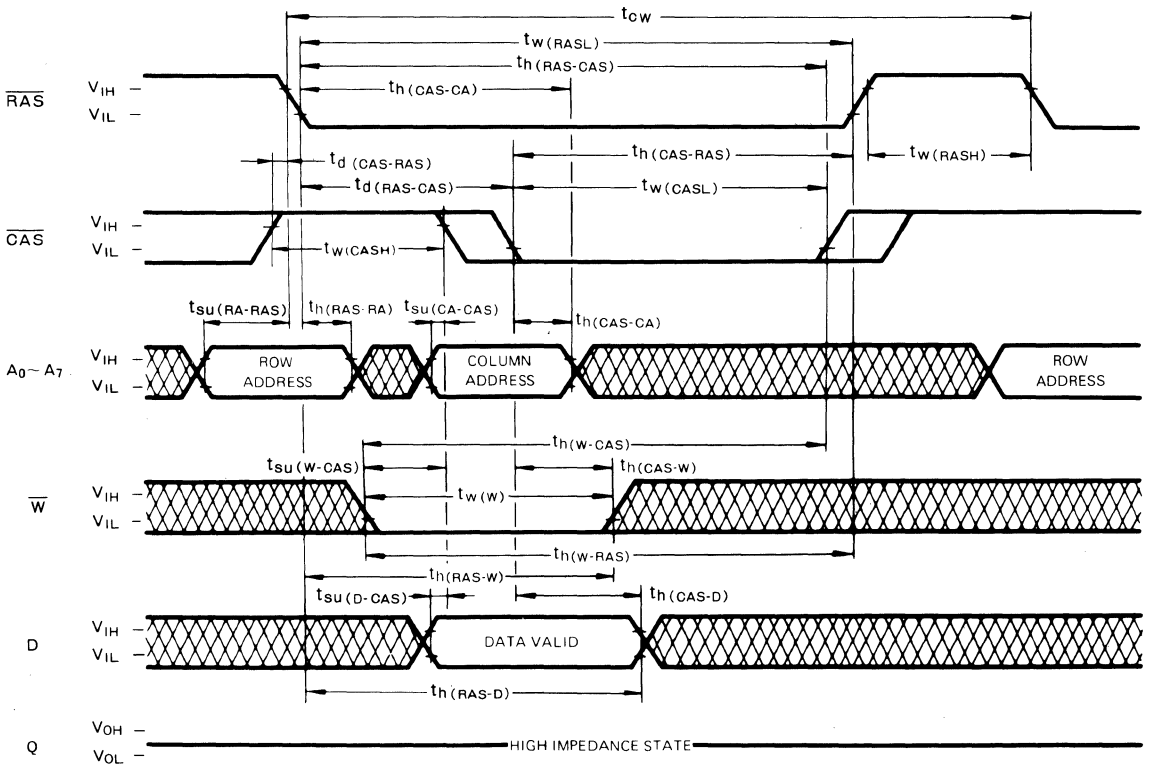
| Symbol | Parameter | Alternative Symbol | M5K4164ANL-12 Limits | | M5K4164ANL-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C\,PGR}$ | Page-mode read cycle time | $t_{PC}$ | 140 | | 140 | | ns |
| $t_{C\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{C\,PGRW}$ | Page-Mode read-write cycle time | — | 150 | | 180 | | ns |
| $t_{CPGRMW}$ | Page-Mode read-modify-write cycle time | — | 170 | | 195 | | ns |
| $tw_{(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | ns |

## TIMING DIAGRAMS (Note 18)

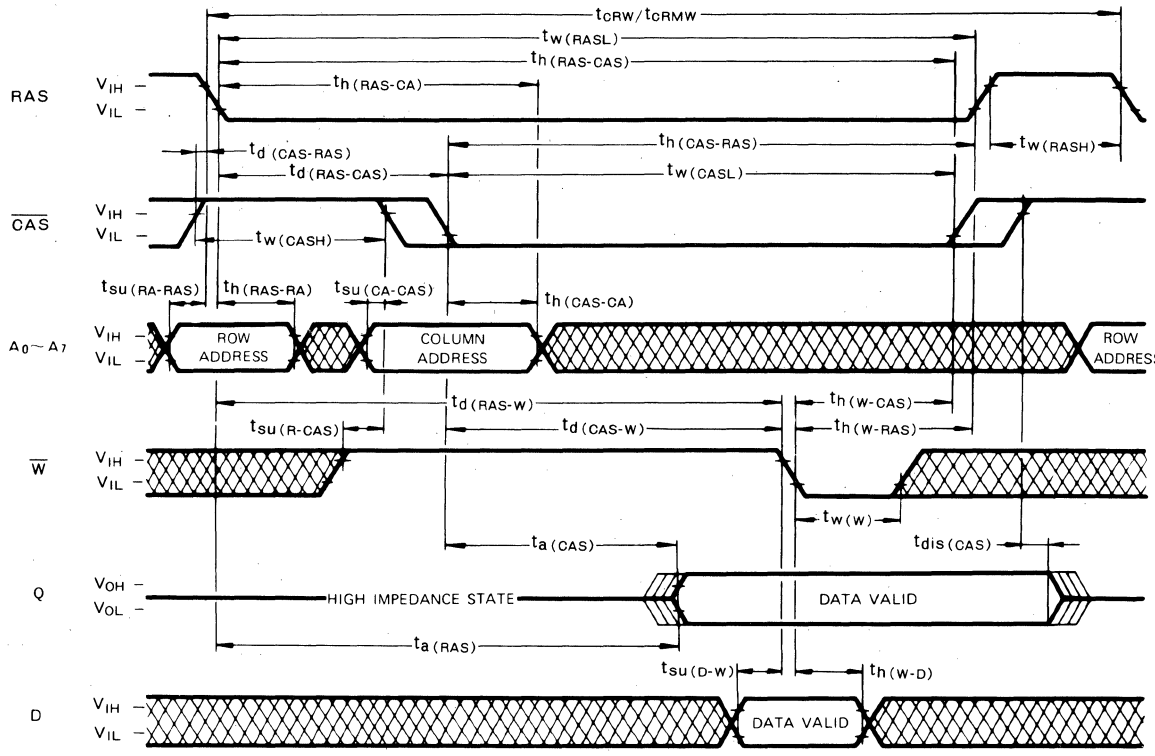
### Read Cycle



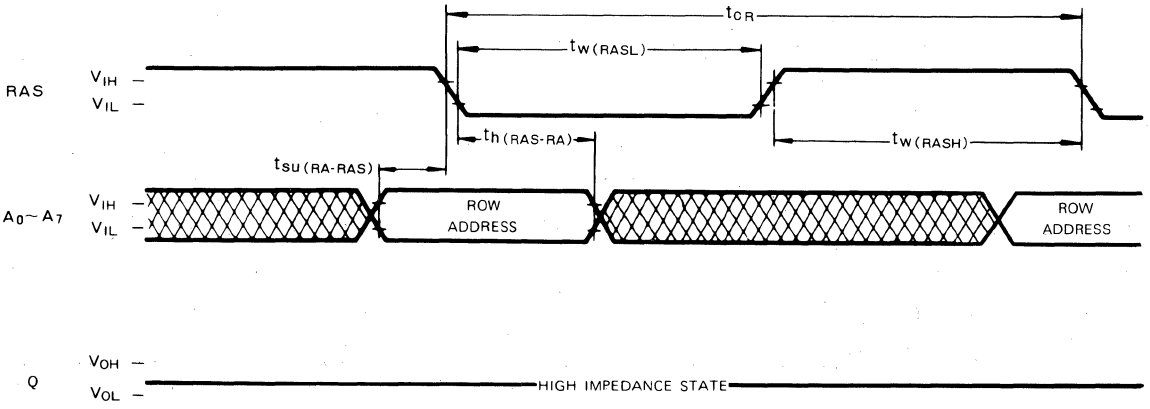

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)




Note 18 Indicates the don't care input

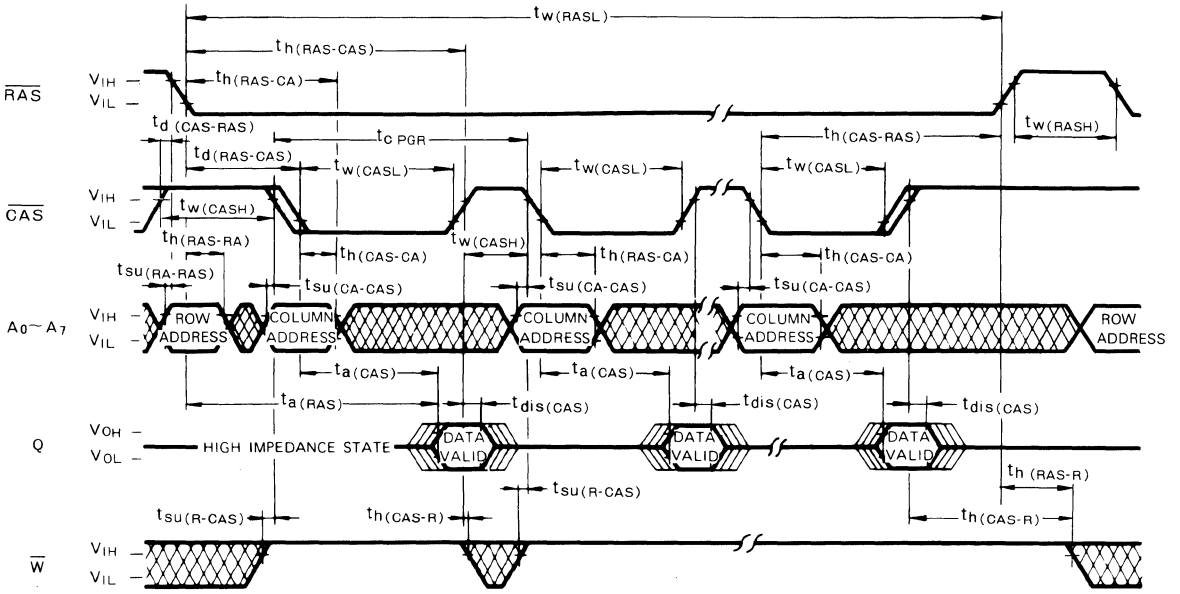
The center-line indicates the high-impedance state

Note 19 $\overline{CAS} = V_{IH}$, $\overline{W}$, D = don't care.
$A_7$ may be $V_{IH}$ or $V_{IL}$.

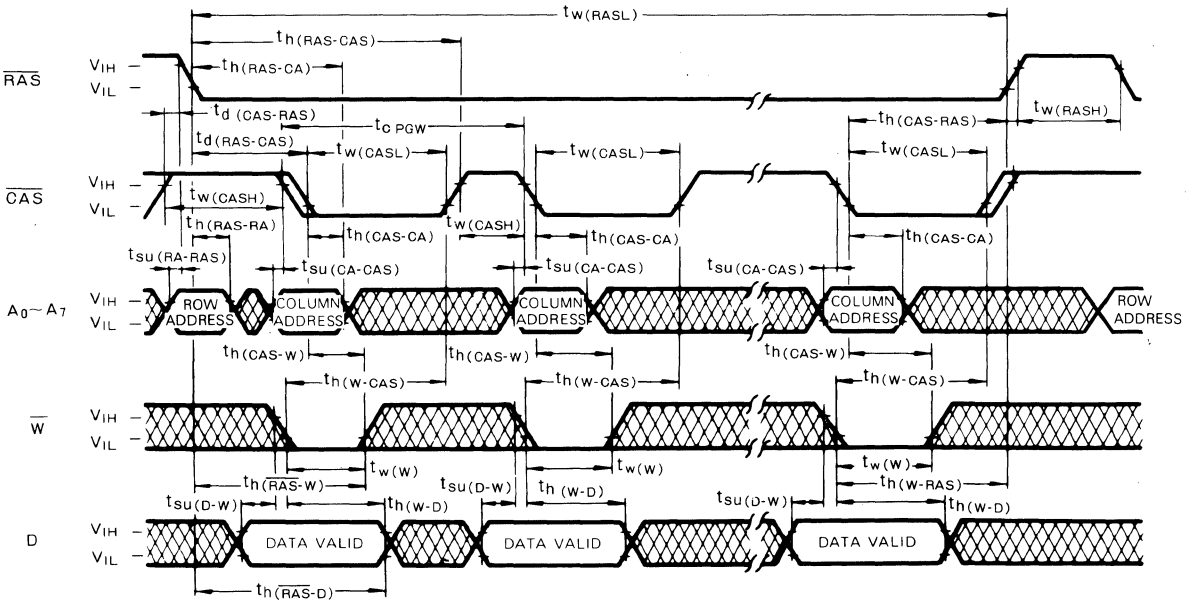


MITSUBISHI ELECTRIC

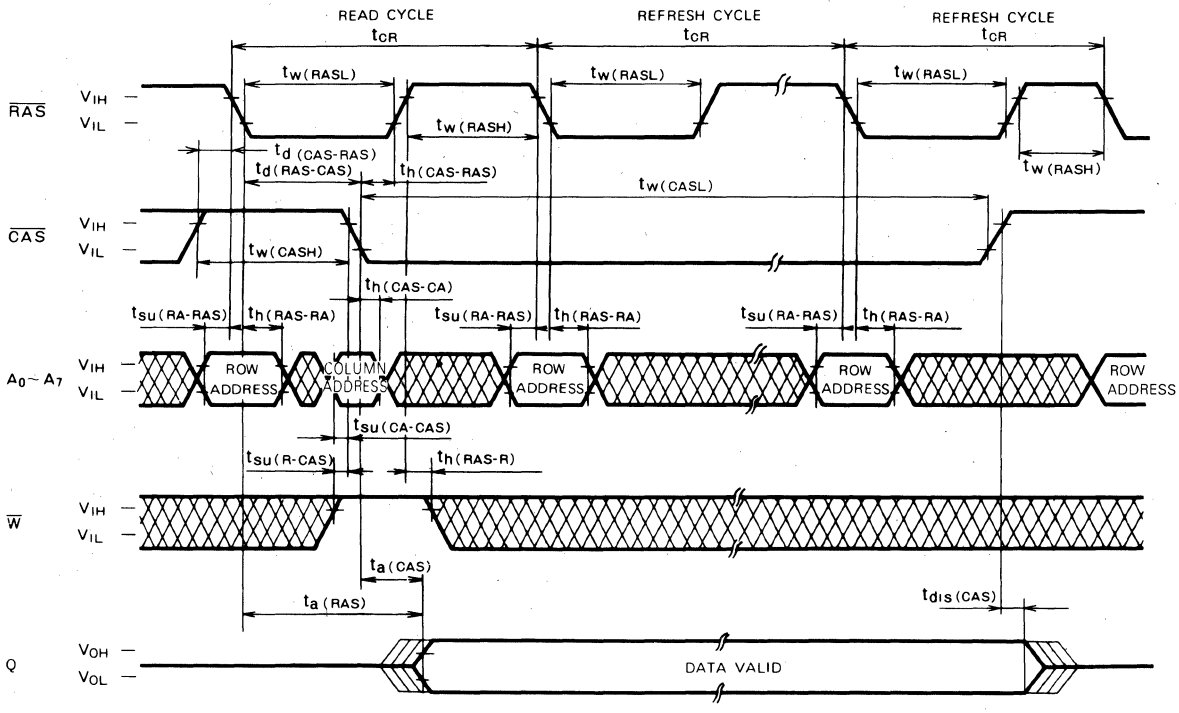
## Page-Mode Read Cycle




## Page-Mode Write Cycle



## Hidden Refresh Cycle



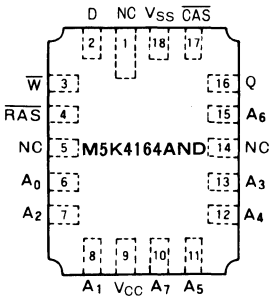
# M5K4164AND-12, -15

## 65 536-BIT (65 536-WORD BY 1-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 18-pin chip carrier package configuration and an increase in system densities. The M5K4164AND operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 18D0**

## FEATURES

- Performance ranges

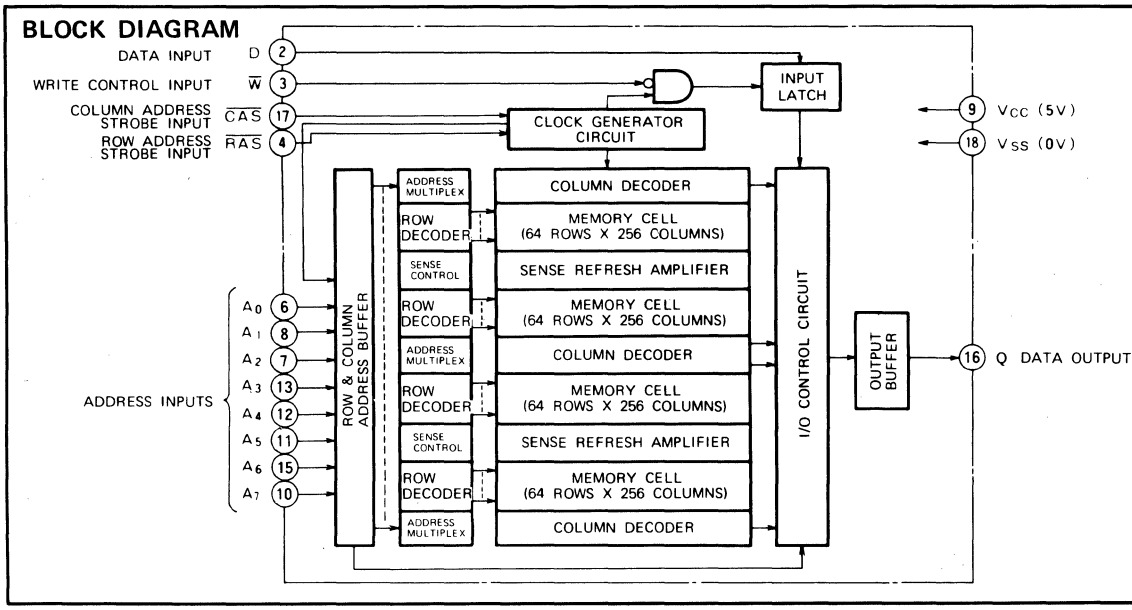
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5K4164AND-12 | 120 | 220 | 175 |
| M5K4164AND-15 | 150 | 260 | 150 |

- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  M5K4164AND-12 275mW (max)
  M5K4164AND-15 250mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms
  (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$

## APPLICATION

- Main memory unit for computers

## BLOCK DIAGRAM



## FUNCTION

The M5K4164AND provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical except refresh is NO. |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| RAS-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 65536 memory cells in the M5K4164AND the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The outut of the M5K4164AND is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K416AND, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K416AND must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164AND are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A features of the M5K4164AND is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5K4164AND is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164AND as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by iindependent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5K4164AND operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5K4164AND-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 50 | mA |
| | | M5K4164AND-15 | $t_{CR}$＝$t_{CW}$＝min output open | | | 45 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5K4164AND-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ | | | 40 | mA |
| | | M5K4164AND-15 | $t_{C(\overline{REF})}$＝min, output open | | | 35 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5K4164AND-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling | | | 40 | mA |
| | | M5K4164AND-15 | $t_{CPG}$＝min, output open | | | 35 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_I$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_I$＝25mVrms | | | 7 | pF |

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | M5K4164AND-12 Limits Min | M5K4164AND-12 Limits Max | M5K4164AND-15 Limits Min | M5K4164AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | ∞ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 90 | | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | 3 | 50 | ns |

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$max is specified reference point only,if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(tTLH)} + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AND-12 Limits Min | M5K4164AND-12 Limits Max | M5K4164AND-15 Limits Min | M5K4164AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 10 | | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12. $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13. This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$max. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | M5K4164AND-12 Limits Min | M5K4164AND-12 Limits Max | M5K4164AND-15 Limits Min | M5K4164AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | 5 | | 5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 90 | | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{W(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5K4164AND-12 Limits | | M5K4164AND-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 245 | | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 265 | | 310 | | ns |
| $th_{(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | ns |
| $th_{(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | ns |
| $tw_{(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $tsu_{(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | ns |
| $td_{(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 100 | | 120 | | ns |
| $td_{(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 40 | | 60 | | ns |
| $tsu_{(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | 0 | | ns |
| $th_{(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | ns |
| $tdis_{(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | ns |
| $ta_{(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | ns |
| $ta_{(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | ns |

Note 15. $t_{CRW}$ min is defined as $t_{CRW}\,min = td_{(RAS-W)} + th_{(W-RAS)} + tw_{(RASH)} + 3t_{TLH}(t_{THL})$

16. $t_{CRMW}$ min is defined as $t_{CRMW}\,min = ta_{(RAS)}max + th_{(W-RAS)} + tw_{(RASH)} + 3t_{TLH}(t_{THL})$

17. $tsu_{(W-CAS)}$, $td_{(RAS-W)}$, and $td_{(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $tsu_{(W-CAS)} \geqq tsu_{(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $td_{(RAS-W)} \geqq td_{(RAS-W)}min$ and $td_{(CAS-W)} \geqq tsu_{(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

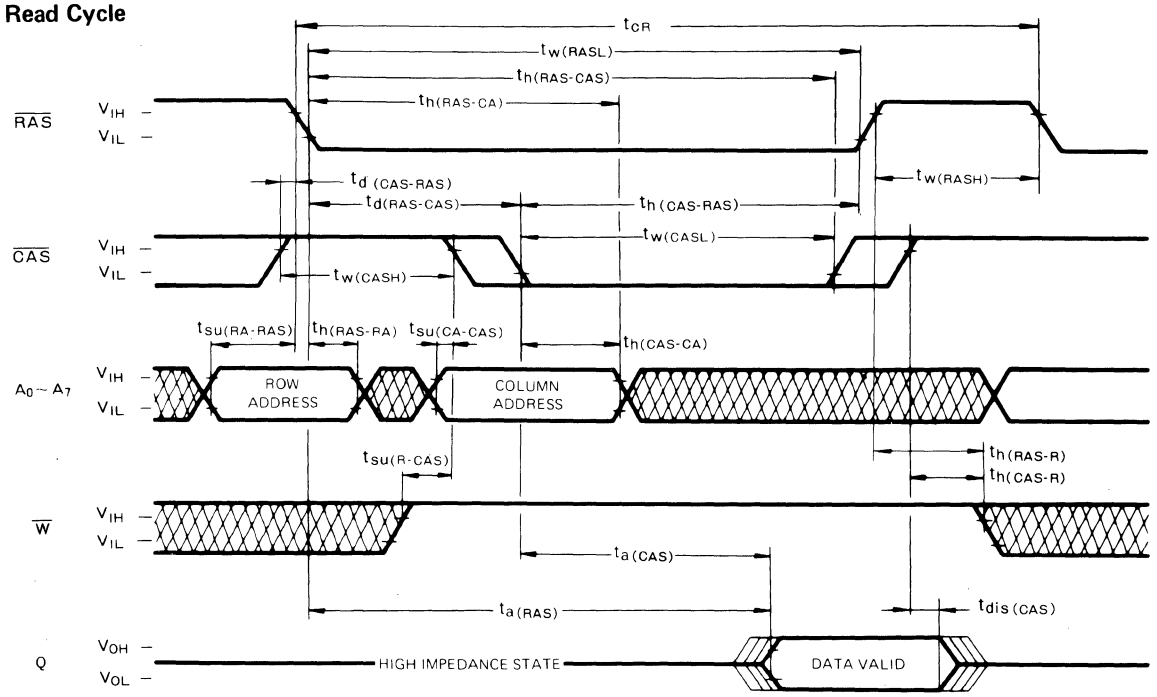
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

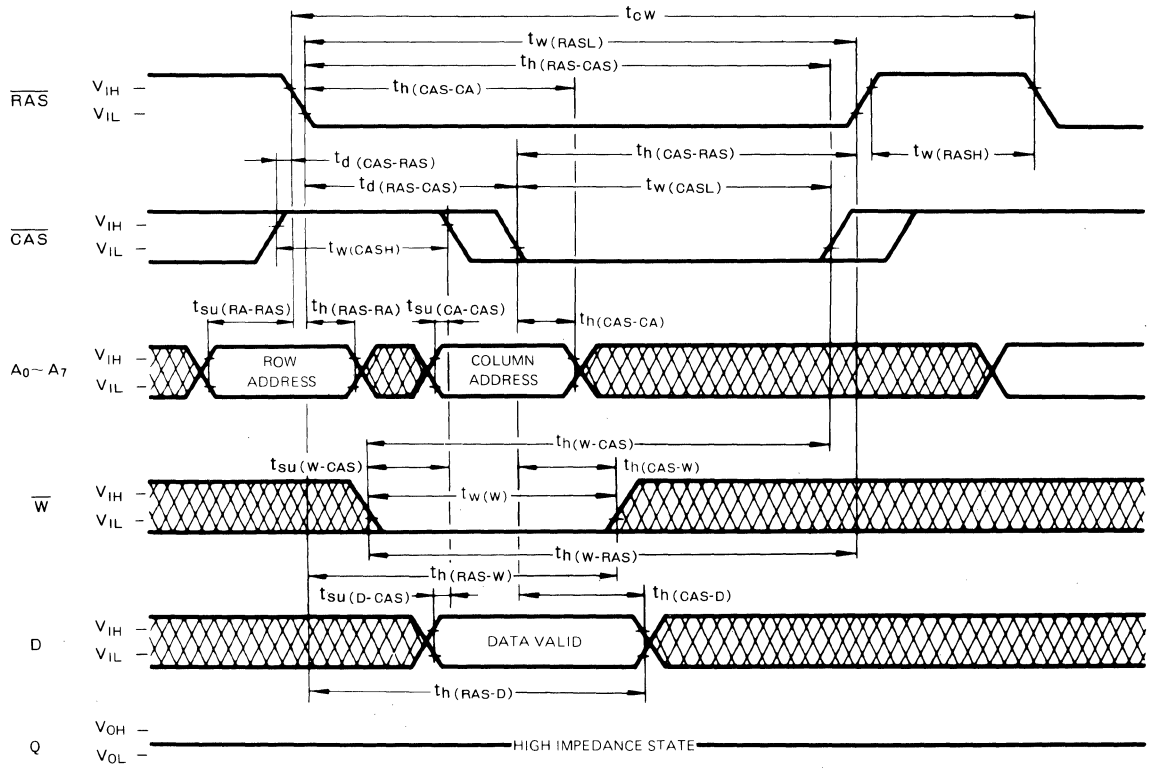
| Symbol | Parameter | Alternative Symbol | M5K4164AND-12 Limits | | M5K4164AND-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C\,PGR}$ | Page-Mode read cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{C\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 140 | | 145 | | ns |
| $t_{C\,PGRW}$ | Page-Mode read-write cycle time | — | 150 | | 180 | | ns |
| $t_{CPGRMW}$ | Page-Mode read-modify-write cycle time | — | 170 | | 195 | | ns |
| $tw_{(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | ns |

## TIMING DIAGRAMS (Note 18)

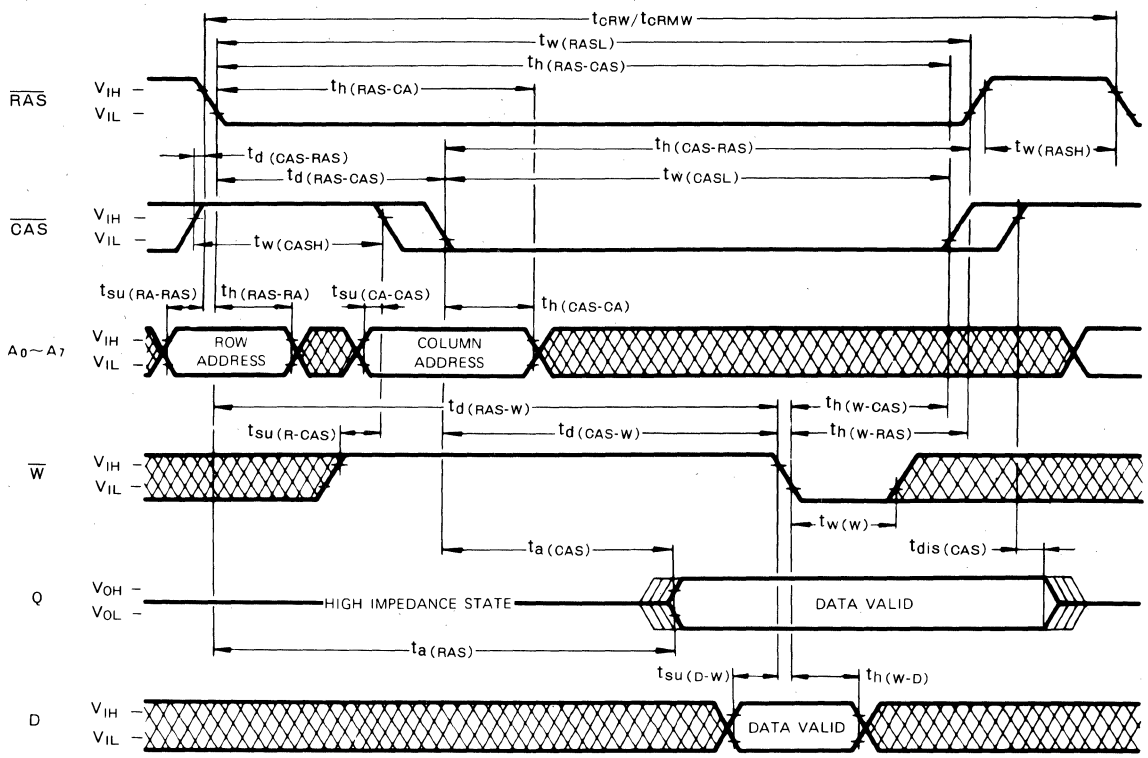
### Read Cycle



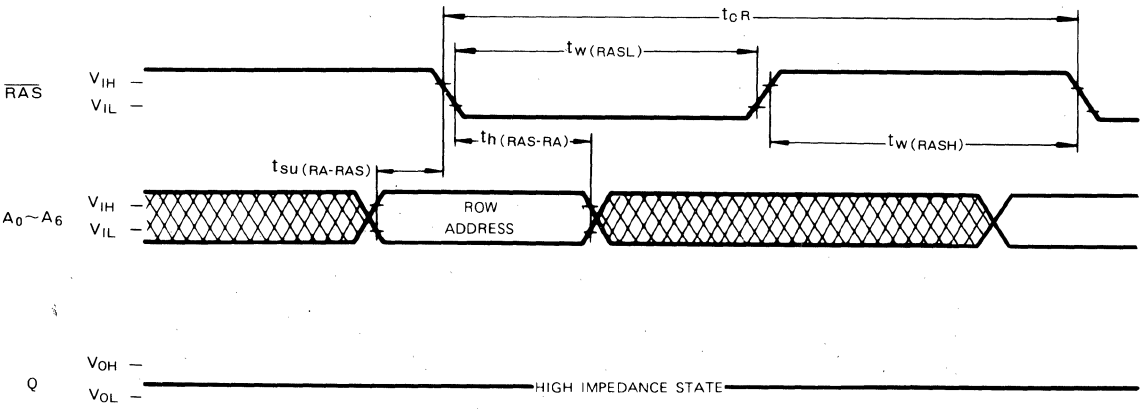

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)

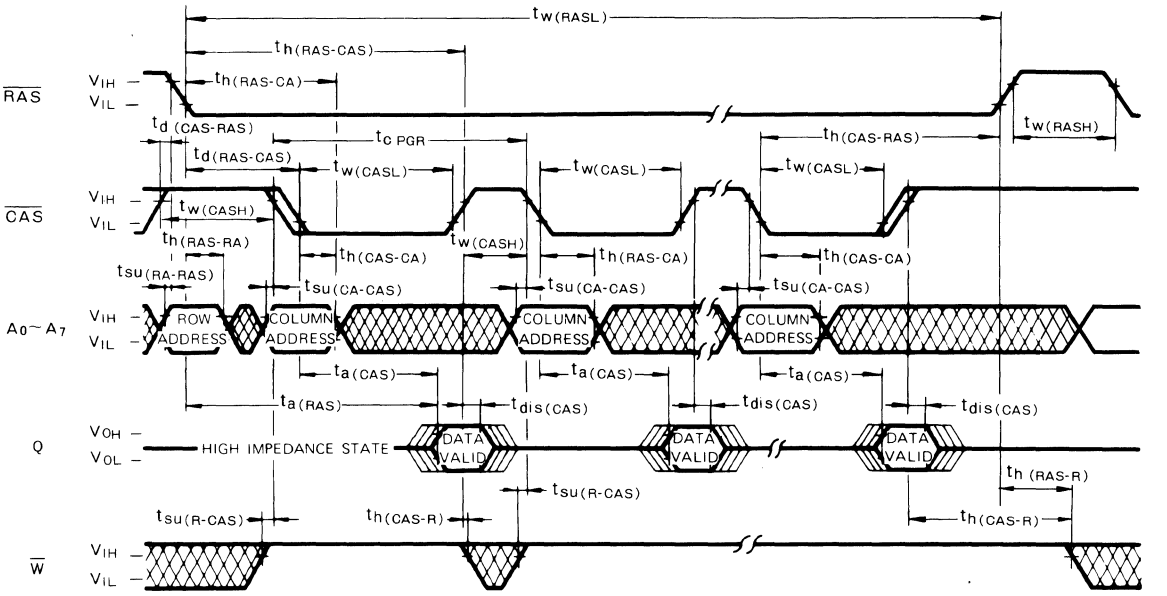



Note 18 Indicates the don't care input

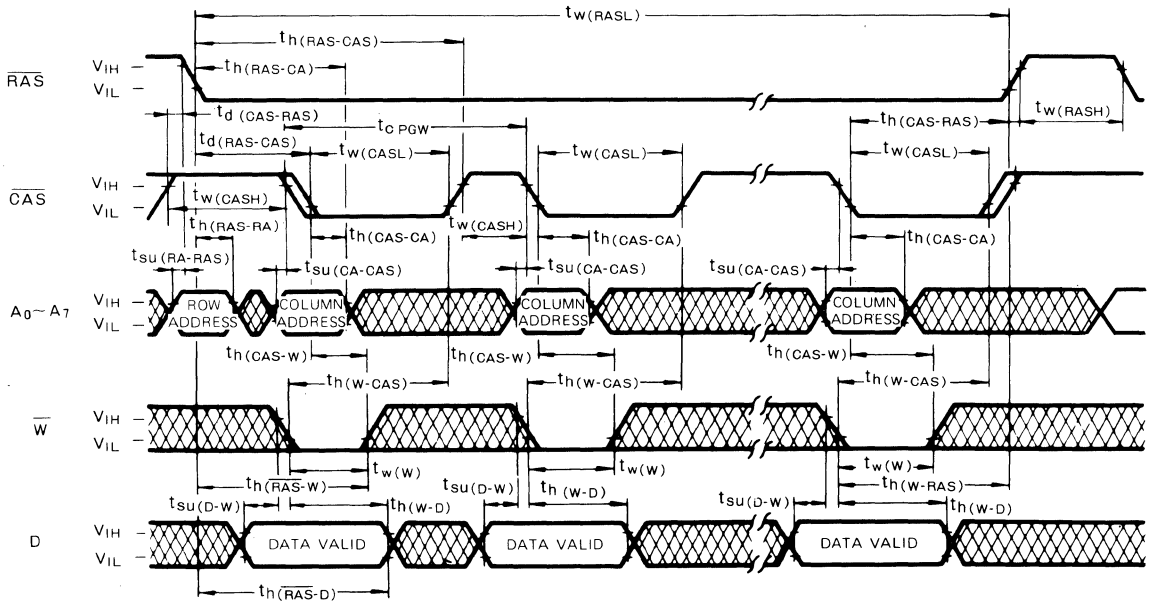
The center-line indicates the high-impedance state

Note 19 $\overline{CAS} = V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

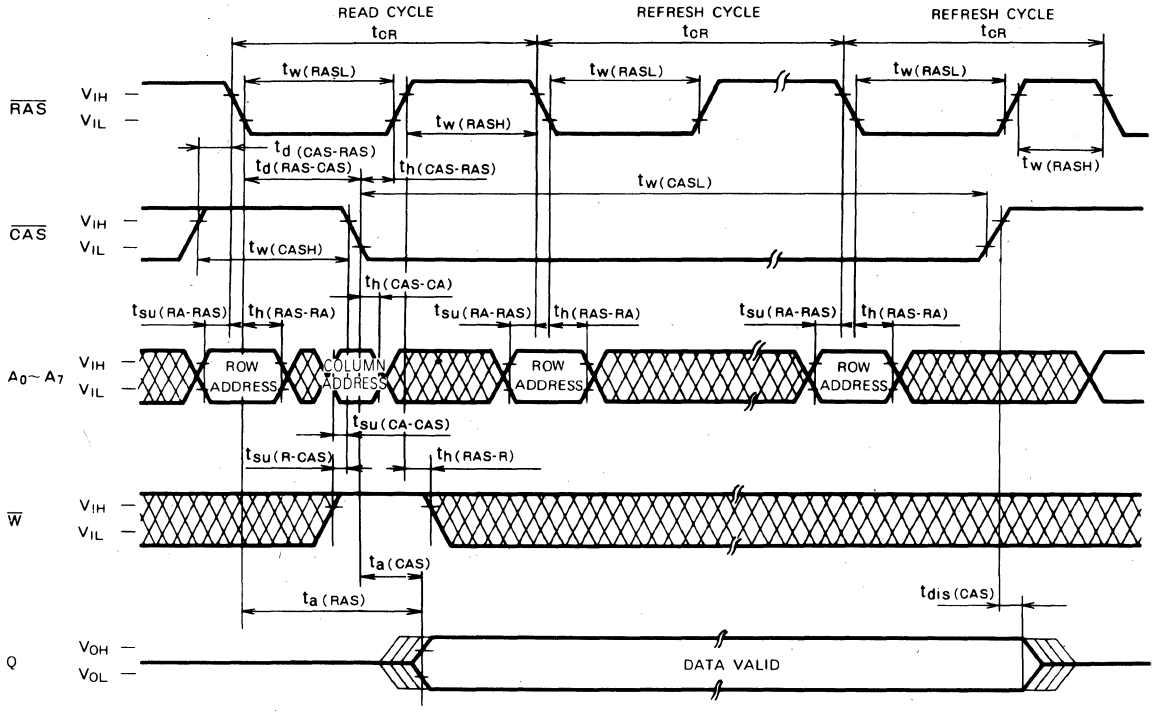
## Page-Mode Read Cycle

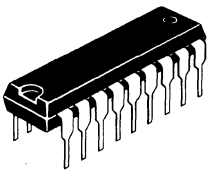



## Page-Mode Write Cycle



## Hidden Refresh Cycle







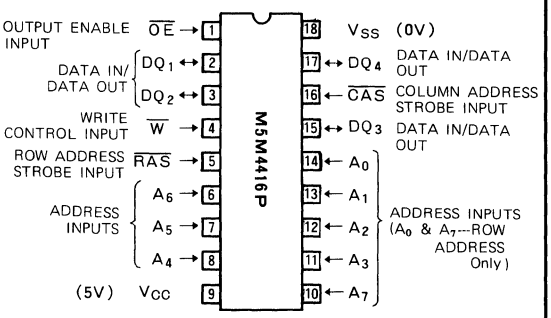
# M5M4416P-12, -15

## 65 536-BIT (16 384-WORD BY 4-BIT) DYNAMIC RAM

## DESCRIPTION

This is family of 16348-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package configuration and an increase in system densities. The M5M4416P operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 18 P4**

## FEATURES

- Performance ranges

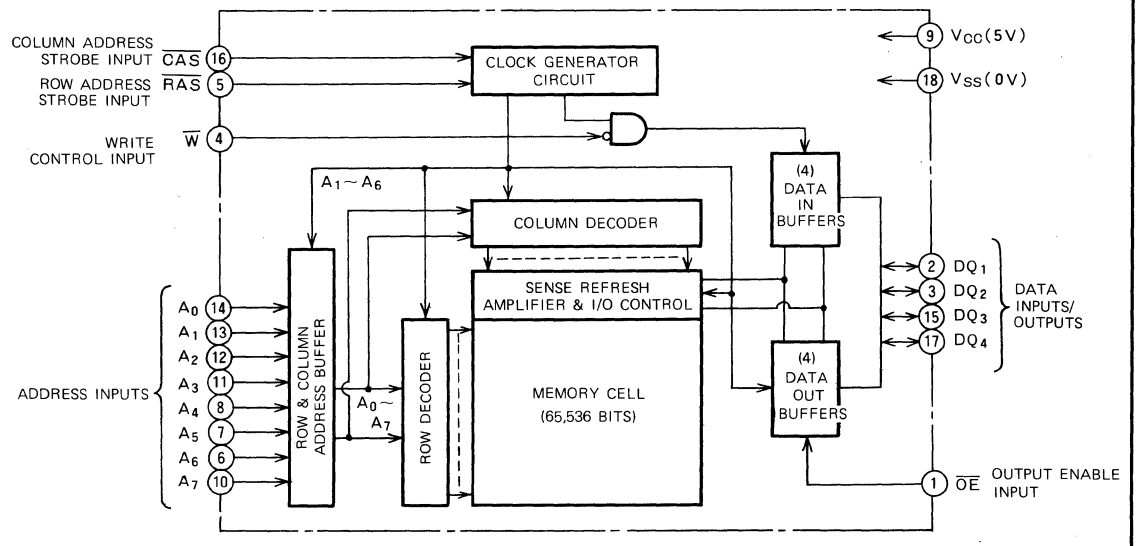
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| **M5M4416P-12** | 120 | 220 | 175 |
| **M5M4416P-15** | 150 | 260 | 150 |

- 16,384 x 4 Organization
- Industry standard 18-pin dual in line package
- Single 5V ±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  M5M4416P-12 275mW (max)
  M5M4416P-15 250mW (max)
- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 128 refresh cycles/2ms. Pin 10 is not needed for refresh
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30$\mu$s max

## APPLICATION

- Refresh memory for CRT

## BLOCK DIAGRAM



## FUNCTION

The M5M4416P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Input/Output | | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | $\overline{OE}$ | Row address | Column adress | Input DQ | Output DQ | | |
| Read | ACT | ACT | NAC | ACT | APD | APD | OPN | VLD | YES | Page mode identical |
| Write (Early Write) | ACT | ACT | ACT | DNC | APD | APD | VLD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | ACT | APD | APD | VLD | VLD | YES | |
| $\overline{RAS}$-only retfesh | ACT | NAC | DNC | DNC | APD | DNC | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | ACT | APD | DNC | OPN | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

## SUMMARY OF OPERATIONS

**address (AO through A7)**

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins AO through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

**write enable ($\overline{W}$)**

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

**data-in (DQ1 through DQ4)**

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

**data-out (DQ1 through DQ4)**

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying $t_{OEHD}$.

**output enable ($\overline{OE}$)**

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

## Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5M4416P must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5M4416P are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A features of the M5M4416P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4416P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4416P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4416P operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | parameter | Condtions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply volrage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta=25°C | 700 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2.0 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta=0～70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−2mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins =0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{cc}$, operating (Note 3,4) | M5M4416P-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 55 | mA |
| | | M5M4416P-15 | tc(rd)=tc(w) = min output open | | | 50 | mA |
| $I_{CC2}$ | Supply current from $V_{cc}$, standby | | $\overline{RAS}$=$V_{IH}$ output open | | | 4.5 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{cc}$, retreshing (Note 3) | M5M4416P-12 | $\overline{RAS}$ cycling $\overline{CAS}$=$V_{IH}$ | | | 45 | mA |
| | | M5M4416P-15 | tc(Prd) = min, output open | | | 40 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{cc}$, page mode (Note 3,4) | M5M4416P-12 | $\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ cycling | | | 45 | mA |
| | | M5M4416P-15 | tc(Prd) = min, output open | | | 40 | mA |

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## CAPACITANCE (Ta=0～70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$=$V_{SS}$ f=1MHz $V_i$=25m$V_{rms}$ | | | 5 | pF |
| $C_{I(OE)}$ | Input capacitance, $\overline{OE}$ input | | | | 7 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | 10 | pF |
| $C_{I/O}$ | Input/Output capacitance, data ports | | | | 10 | pF |

## SWITCHING CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted) (Note 5)

| Symbol | Parameter | | Alternative Symbol | M5M4416P-12 Limits Min | M5M4416P-12 Limits Max | M5M4416P-15 Limits Min | M5M4416P-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{a(C)}$ | Access time from $\overline{CAS}$ | (Note 6,7) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(R)}$ | Access time from $\overline{RAS}$ | (Note 6,8) | $t_{RAC}$ | | 120 | | 150 | ns |
| $t_{a(OE)}$ | Access time from $\overline{OE}$ | (Note 6) | — | | 30 | | 40 | ns |
| $t_{dis(CH)}$ | Output disable time after $\overline{CAS}$ high | (Note 9) | $t_{OFF}$ | 0 | 25 | 0 | 30 | ns |
| $t_{dis(OE)}$ | Output disable time after $\overline{OE}$ high | (Note 9) | — | 0 | 25 | 0 | 30 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If $t_{RLCL}$ is greater than $t_{RLCL}$ max then $t_{a(R)}$ will increase by the amount that $t_{RLCL}$ exceeds $t_{RLCL}$ max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH}$ min or $V_{OL}$ max.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted, See notes 10,11)

| Symbol | Parameter | | Alternative Symbol | M5M4416P-12 Limits Min | M5M4416P-12 Limits Max | M5M4416P-15 Limits Min | M5M4416P-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{C(RF)}$ | Refresh cycle time | | $t_{REF}$ | | 2 | | 2 | ms |
| $t_{W(RH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{RLCL}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low | (Note 12) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{CHRL}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | (Note 13) | $t_{CRP}$ | −20 | | −20 | | ns |
| $t_{su(RA)}$ | Row address setup time before $\overline{RAS}$ low | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA)}$ | Column address setup time before $\overline{CAS}$ low | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RA)}$ | Row address hold time after $\overline{RAS}$ low | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CLCA)}$ | Column address hold time after $\overline{CAS}$ low | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RLCA)}$ | Column address hold time after $\overline{RAS}$ low | | $t_{AR}$ | 80 | | 100 | | ns |
| $t_T$ | Transition time (rise and fall) | (Note 14) | $t_T$ | 3 | 50 | 3 | 50 | ns |

Note 10: The timing requirements are assumed $t_T$=5ns.
11: $V_{IH}$ min and $V_{IL}$ max are reference levels for measuring timing of input signals.
12: $t_{RLCL}$ max is specified as a reference point only; if $t_{RLCL}$ is less than $t_{RLCL}$ max, access time is $t_{a(R)}$, if $t_{RLCL}$ is greater than $t_{RLCL}$ max, access time is $t_{RLCL} + t_{a(C)}$. $t_{RLCL}$ min is specified as $t_{RLCL}$ min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: $t_{CHRL}$ requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: $t_T$ is measured between $V_{IH}$ min and $V_{IL}$ max.

## Read and Refresh Cycles

| Symbol | Parameter | | Alternative Symbol | M5M4416P-12 Limits Min | M5M4416P-12 Limits Max | M5M4416P-15 Limits Min | M5M4416P-15 Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{C(rd)}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 30 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{su(rd)}$ | Read setup time before $\overline{CAS}$ low | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CHrd)}$ | Read hold time after $\overline{CAS}$ high | (Note 15) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RHrd)}$ | Read hold time after $\overline{RAS}$ high | (Note 15) | $t_{RRH}$ | 10 | | 10 | | ns |
| $t_{h(OECH)}$ | $\overline{CAS}$ hold time after $\overline{OE}$ low | | — | 30 | | 40 | | ns |
| $t_{h(OERH)}$ | $\overline{RAS}$ hold time after $\overline{OE}$ low | | — | 30 | | 40 | | ns |
| $t_{h(CLOE)}$ | $\overline{OE}$ hold time after $\overline{CAS}$ low | | — | 60 | | 75 | | ns |
| $t_{h(RLOE)}$ | $\overline{OE}$ hold time after $\overline{RAS}$ low | | — | 120 | | 150 | | ns |
| $t_{DOEL}$ | Delay time, Data to $\overline{OE}$ low | | — | 0 | | 0 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |
| $t_{RHCL}$ | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | | — | 0 | | 0 | | ns |

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

## Write Cycles (Early Write and Delayed Write)

| Symbol | Parameter | | Alternative Symbol | M5M4416P-12 Limits | | M5M4416P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{C(W)}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 30 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{su(WCL)}$ | Write setup time before $\overline{CAS}$ low | (Note 17) | $t_{WCS}$ | −5 | | −5 | | ns |
| $t_{h(CLW)}$ | Write hold time after $\overline{CAS}$ low | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RLW)}$ | Write hold time after $\overline{RAS}$ low | | $t_{WCR}$ | 100 | | 120 | | ns |
| $t_{h(WCH)}$ | $\overline{CAS}$ hold time after Write low | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{h(WRH)}$ | $\overline{RAS}$ hold time after Write low | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{W(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D)}$ | Data setup time | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(WLD)}$ | Data hold time after Write low | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(CLD)}$ | Data hold time after $\overline{CAS}$ low | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(RLD)}$ | Data hold time after $\overline{RAS}$ low | | $t_{DHR}$ | 100 | | 120 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |
| $t_{h(WOE)}$ | $\overline{OE}$ hold time after Write low | | — | 25 | | 30 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5M4416P-12 Limits | | M5M4416P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{C(rdW)}$ | Read write/read modify write cycle time | (Note 16) | $t_{RWC}$ | 295 | | 345 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 195 | 10000 | 255 | 10000 | ns |
| $t_{W(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 135 | | 180 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 195 | | 255 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 135 | | 180 | | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 30 | | ns |
| $t_{su(rd)}$ | Read setup time before $\overline{CAS}$ low | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{CLWL}$ | Delay time, $\overline{CAS}$ low to Write low | (Note 17) | $t_{CWD}$ | 90 | | 110 | | ns |
| $t_{RLWL}$ | Delay time, $\overline{RAS}$ low to Write low | (Note 17) | $t_{RWD}$ | 150 | | 185 | | ns |
| $t_{h(WCH)}$ | $\overline{CAS}$ hold time after Write low | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{h(WRH)}$ | $\overline{RAS}$ hold time after Write low | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{W(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D)}$ | Data setup time | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(WLD)}$ | Data hold time after Write low | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(CLOE)}$ | $\overline{OE}$ hold time after $\overline{CAS}$ low | | — | 60 | | 75 | | ns |
| $t_{h(RLOE)}$ | $\overline{OE}$ hold time after $\overline{RAS}$ low | | — | 120 | | 150 | | ns |
| $t_{DOEL}$ | Delay time, Data to $\overline{OE}$ low | | — | 0 | | 0 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |

Note 16: $t_{C(rdW)}$ is specified as $t_{C(rdW)}$ min = $t_{a(R)}$ max + $t_{OEHD}$ min + $t_{h(WRH)}$ min + $t_{W(RH)}$ min + 4 $t_T$.

17: $t_{su(WCL)}$, $t_{CLWL}$ and $t_{RLWL}$ are specified as reference points only. If $t_{su(WCL)} \geqq t_{su(WCL)}$ min, the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CLWL} \geqq t_{CLWL}$ min and $t_{RLWL} \geqq t_{RLWL}$ min, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to $V_{IH}$) is indeterminate.

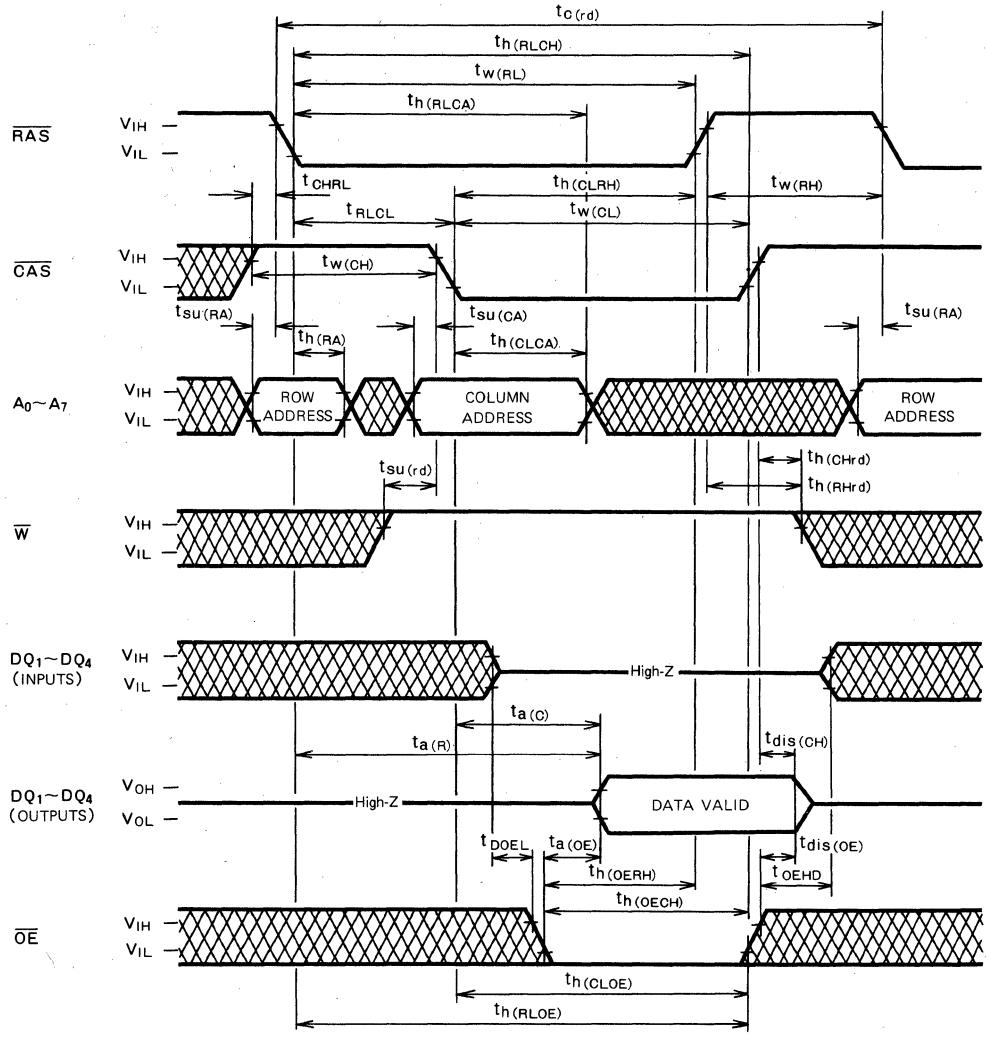
## Page-Mode Cycle (Note 18)

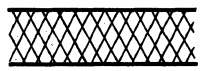
| Symbol | Parameter | Alternative Symbol | M5M4416P-12 Limits | | M5M4416P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C(Prd)}$ | Read cycle time | $t_{PC}$ | 120 | | 145 | | ns |
| $t_{C(PW)}$ | Write cycle time | $t_{PC}$ | 120 | | 145 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width (Note 19) | $t_{RAS}$ | 240 | 30000 | 295 | 30000 | ns |
| $t_{C(PrdW)}$ | Read write/read modify write cycle time | — | 195 | | 250 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width (Note 20) | $t_{RAS}$ | 390 | 30000 | 505 | 30000 | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 50 | | 60 | | ns |

Note 18: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19: Specified for read or write cycle.
20: Specified for read-write or read-modify-write cycle.

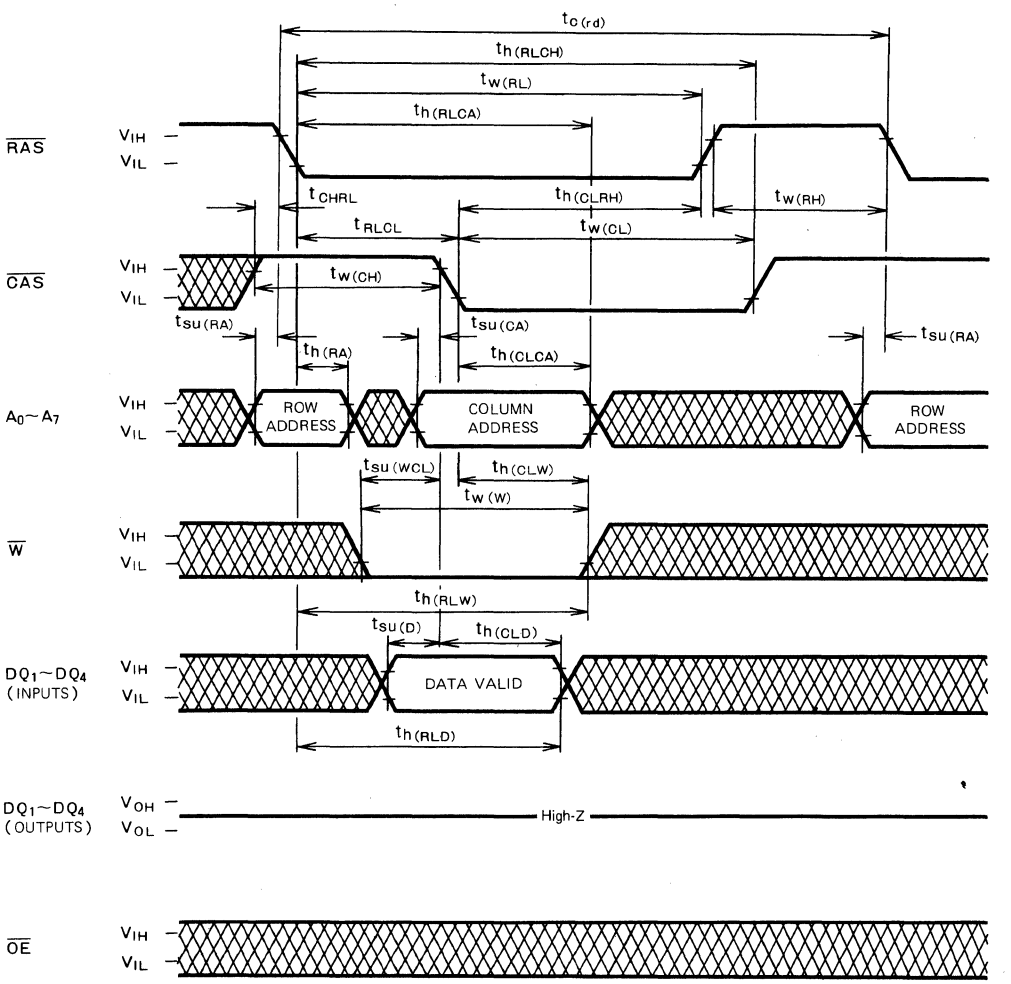
## TIMING DIAGRAMS (Note 21)

### Read Cycle

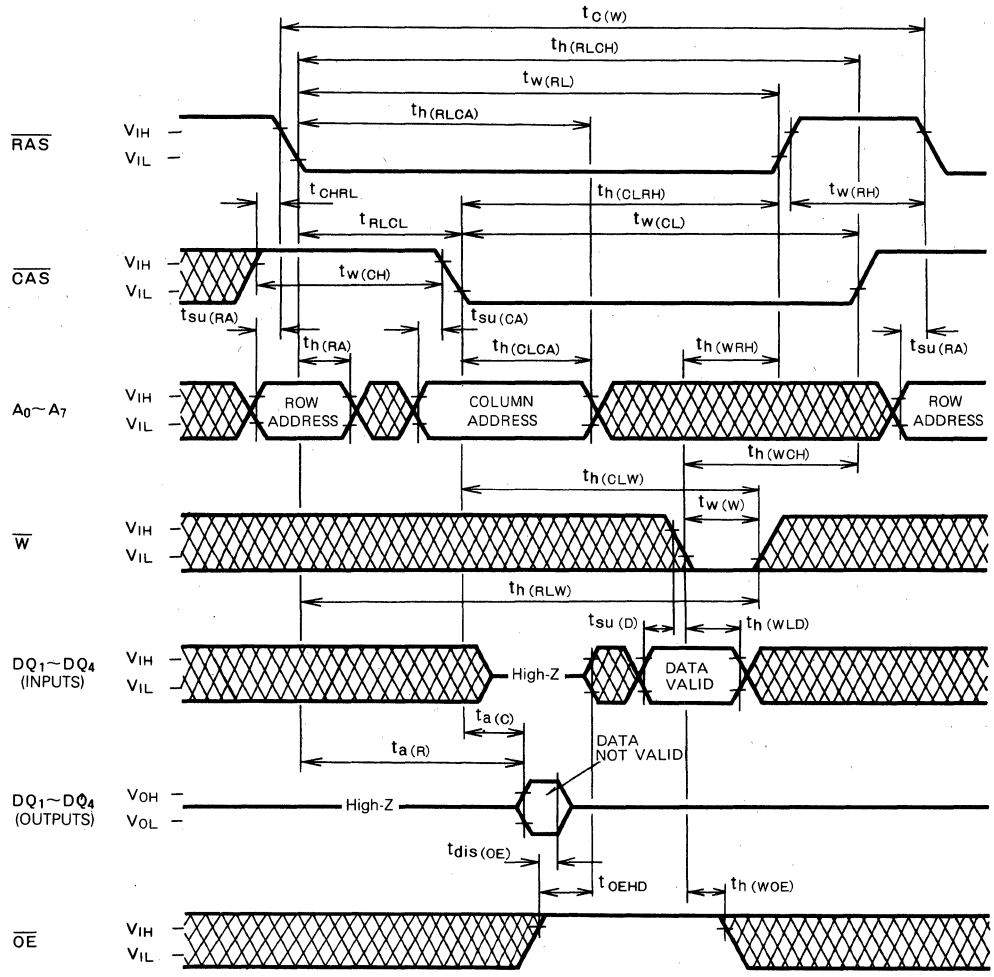



Note 21.  Indicates the don't care input.

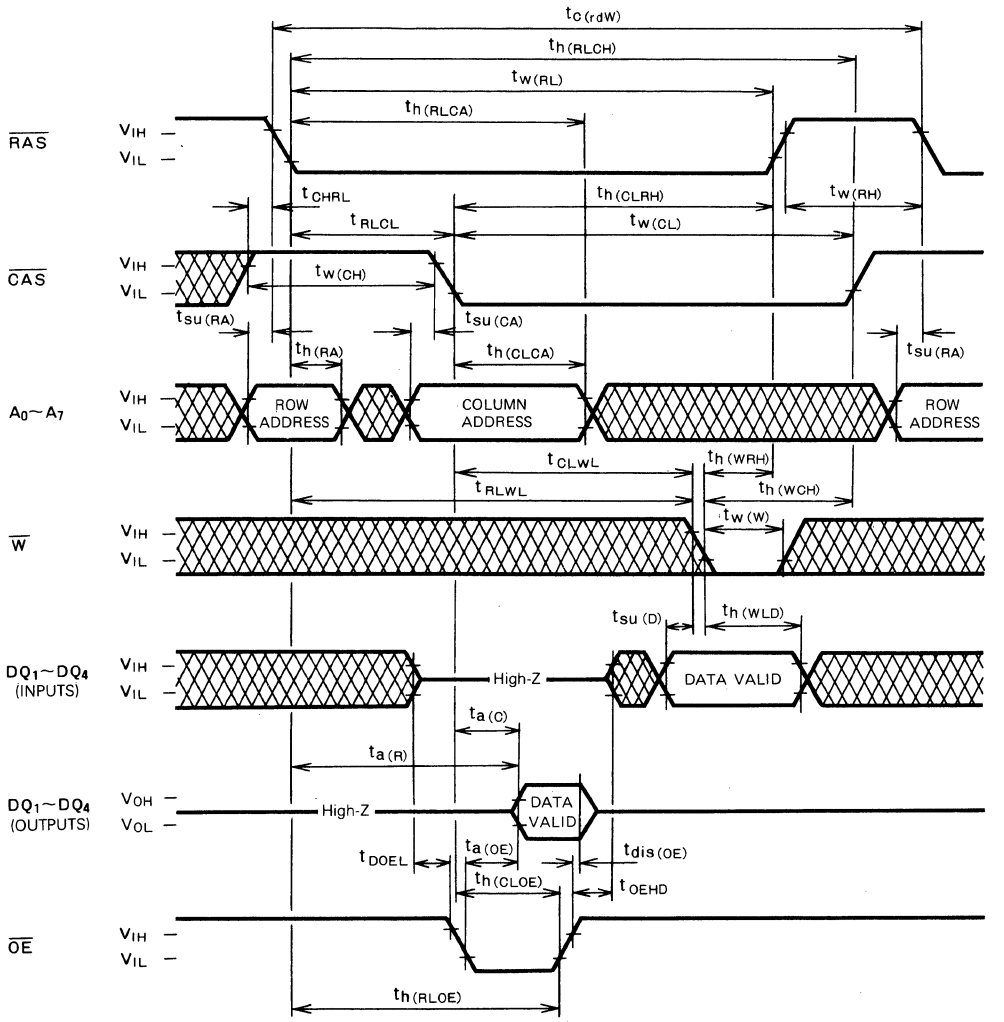
## Write Cycle (Early Write)



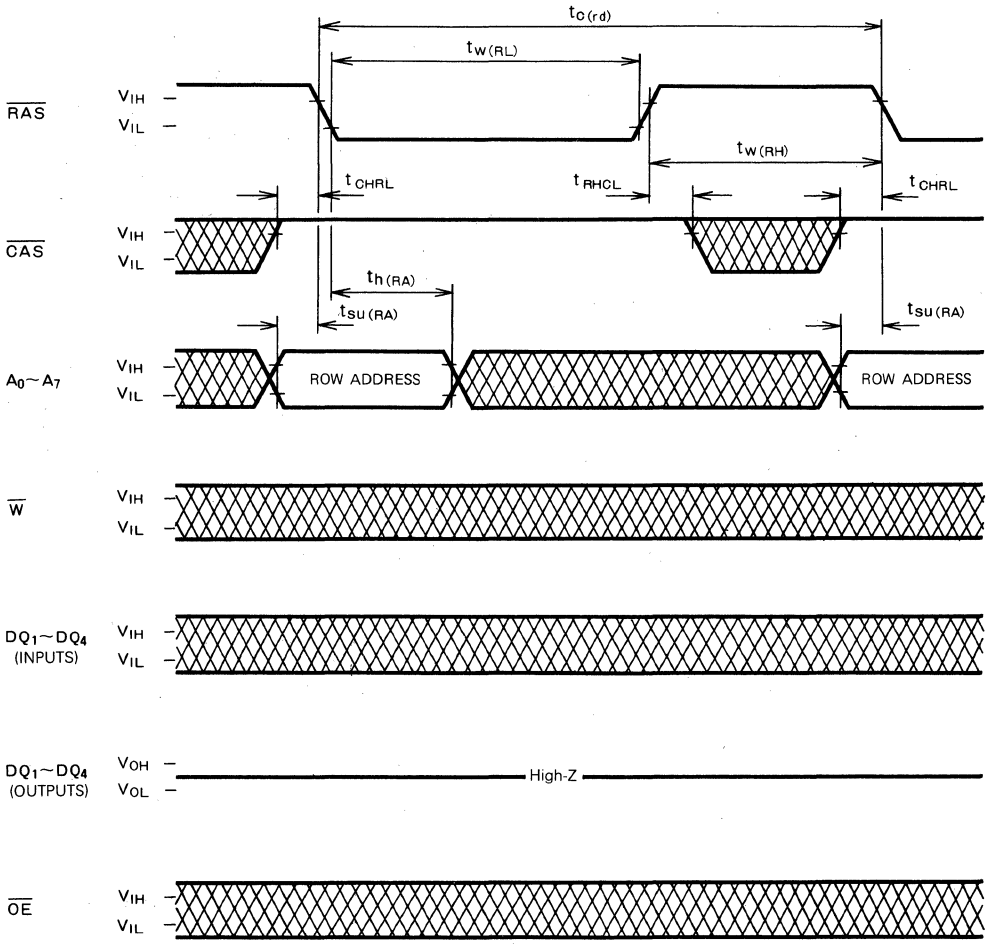
## Write Cycle (Delayed Write)



## Read-Write and Read-Modify-Write Cycles

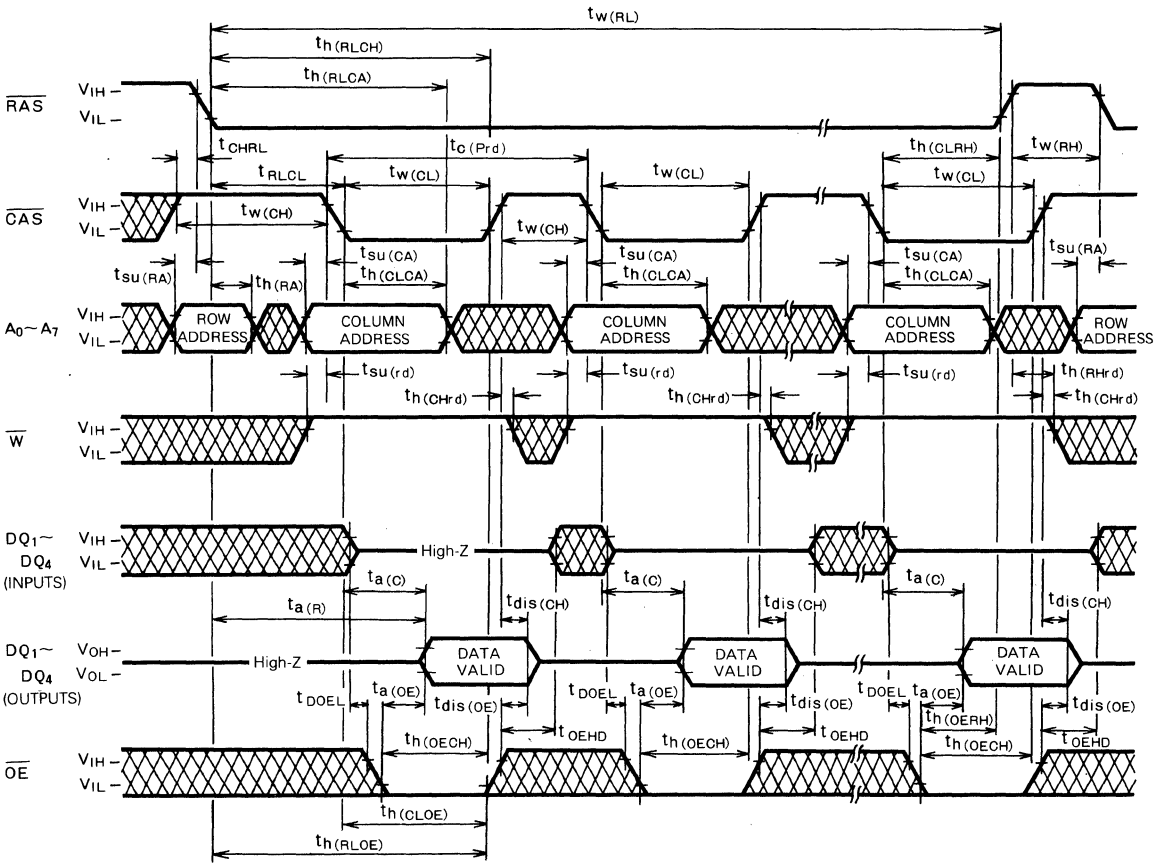


## $\overline{RAS}$-Only Refresh Cycle (Note 22)

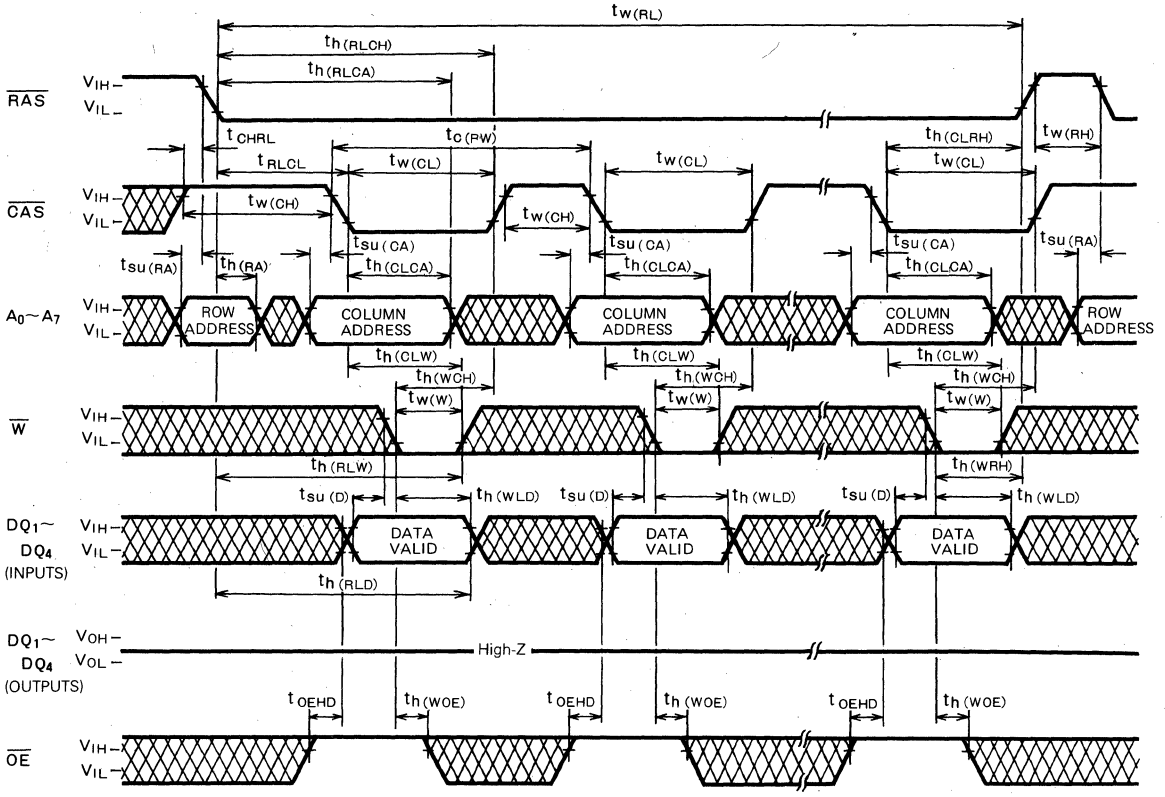



Note 22. $A_7$ may be $V_{IH}$ or $V_{IL}$

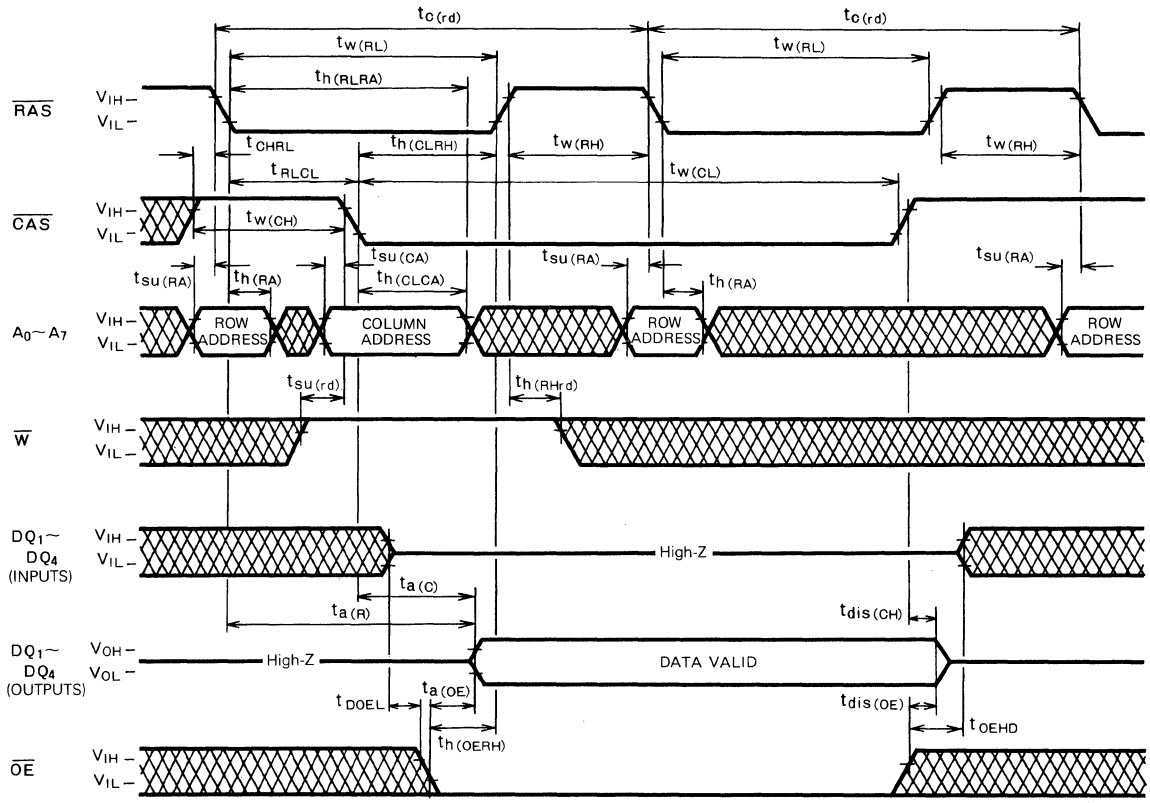
## Page-Mode Read Cycle



## Page-Mode Write Cycle



## Hidden Refresh Cycle



# M5M4256P-12, -15, -20

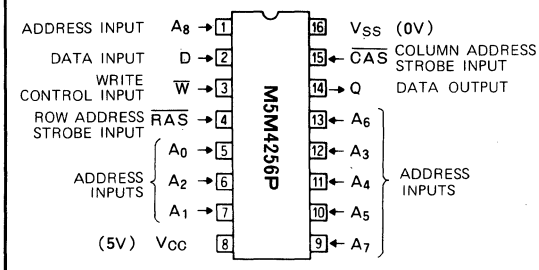
## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM

NEW PRODUCT

## DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P4**

## FEATURES

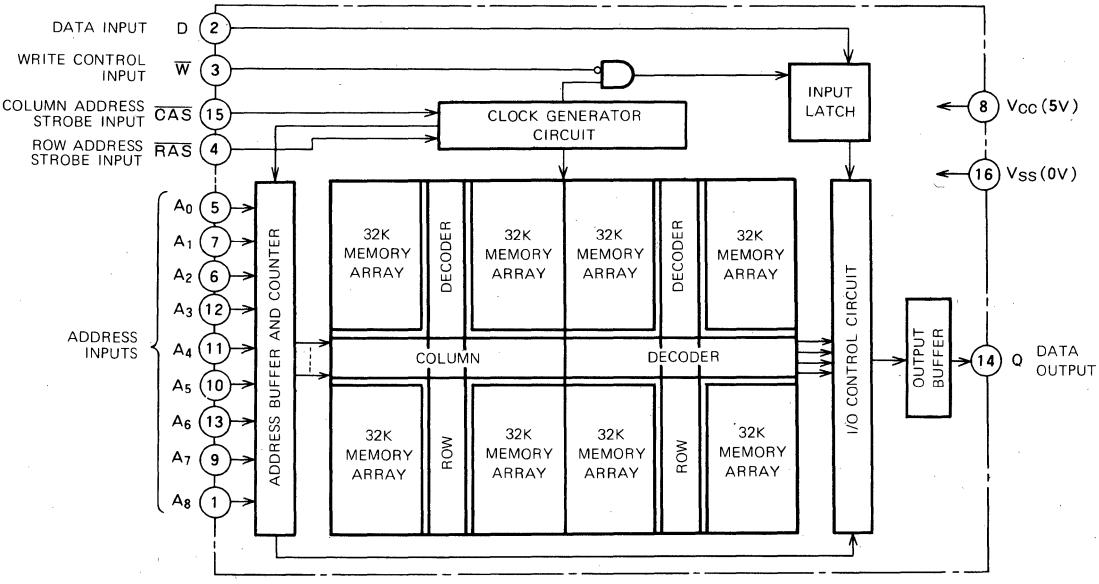
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4256P-12 | 120 | 230 | 260 |
| M5M4256P-15 | 150 | 260 | 230 |
| M5M4256P-20 | 200 | 330 | 190 |

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256P-12 . . . . . 360mW (max)
  - M5M4256P-15 . . . . . 330mW (max)
  - M5M4256P-20 . . . . . 275mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## FUNCTION

The M5M4256P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Page mode identical except refresh is No.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4256P the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4256P is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256P, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256P are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4256P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4256P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4256P operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦$V_{CC}$, Other input pins ＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4256P-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$＝$t_{CW}$＝ min, output open | | | 65 | mA |
| | | M5M4256P-15 | | | | 60 | mA |
| | | M5M4256P-20 | | | | 50 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$\overline{CAS}$＝$V_{IH}$ output open | | | 4.5 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4256P-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ $t_{C(\overline{RAS})}$＝ min, output open | | | 55 | mA |
| | | M5M4256P-15 | | | | 50 | mA |
| | | M5M4256P-20 | | | | 40 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5M4256P-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$＝ min, output open | | | 50 | mA |
| | | M5M4256P-15 | | | | 45 | mA |
| | | M5M4256P-20 | | | | 40 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4256P-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ = min, output open | | | 60 | mA |
| | | M5M4256P-15 | | | | 55 | mA |
| | | M5M4256P-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive; out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 20 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | −5 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)max}$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)max}$ defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions; Load = 2TTL, $C_L$ = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −10 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |

## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15. $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CPG}$ | Page-mode cycle time | $t_{PC}$ | 125 | | 145 | | 190 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | 80 | | ns |
| $t_{CPGRW}$ | Page-mode RW cycle time | $t_{PCRW}$ | 160 | | 180 | | 230 | | ns |
| $t_{CPGRMW}$ | Page-mode RMW cycle time | $t_{PCRMW}$ | 170 | | 195 | | 250 | | ns |

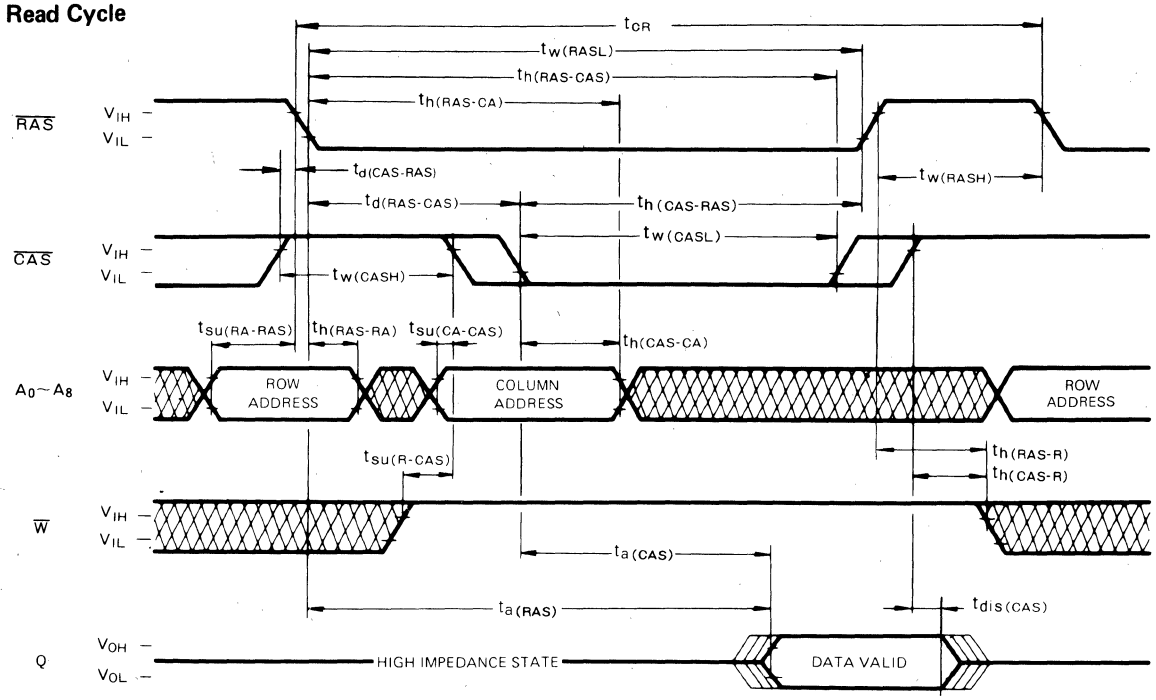
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256P-12 | | M5M4256P-15 | | M5M4256P-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

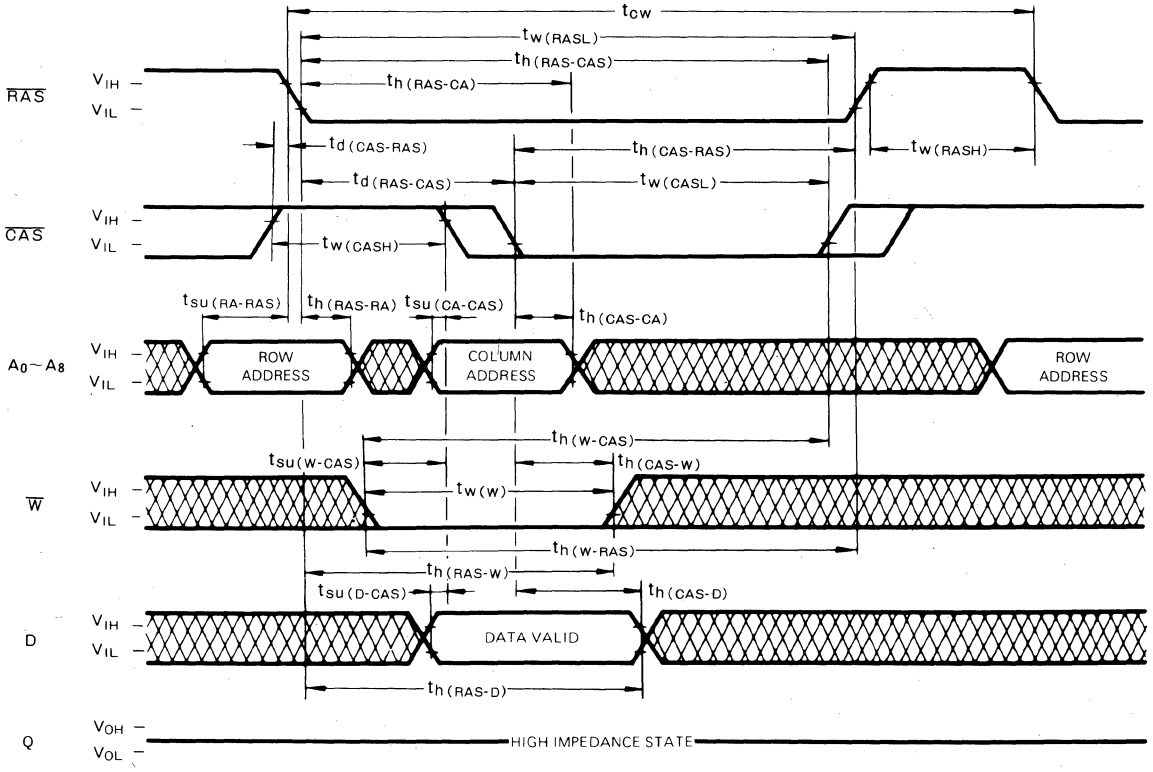
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## TIMING DIAGRAMS (Note 19)

### Read Cycle




### Write Cycle (Early Write) (Note 21)



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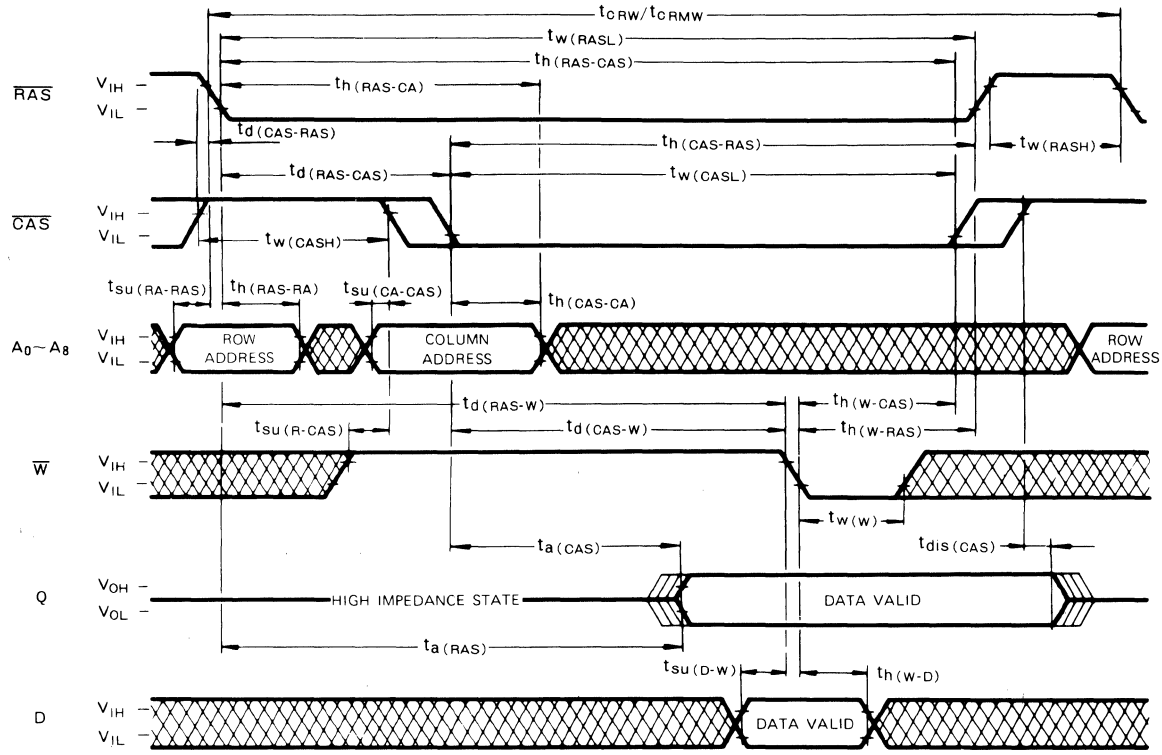
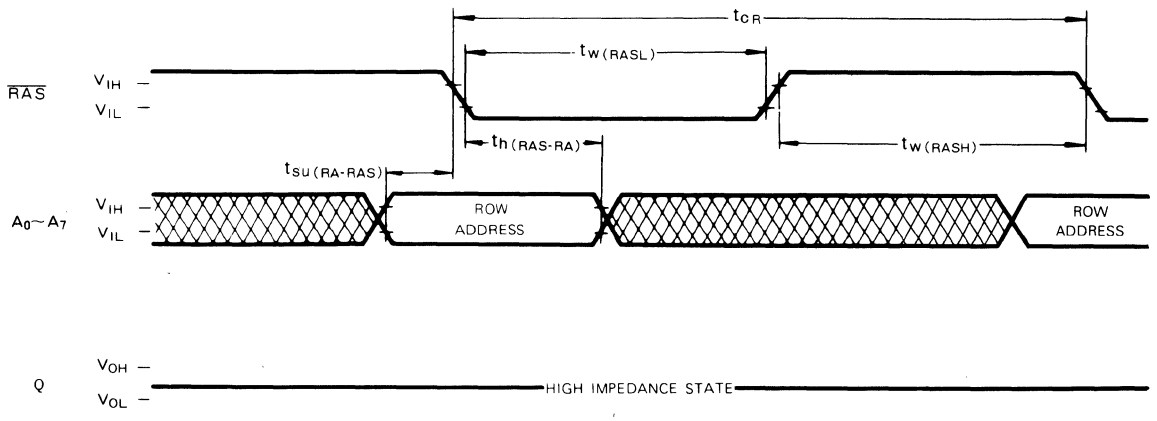
## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 20)

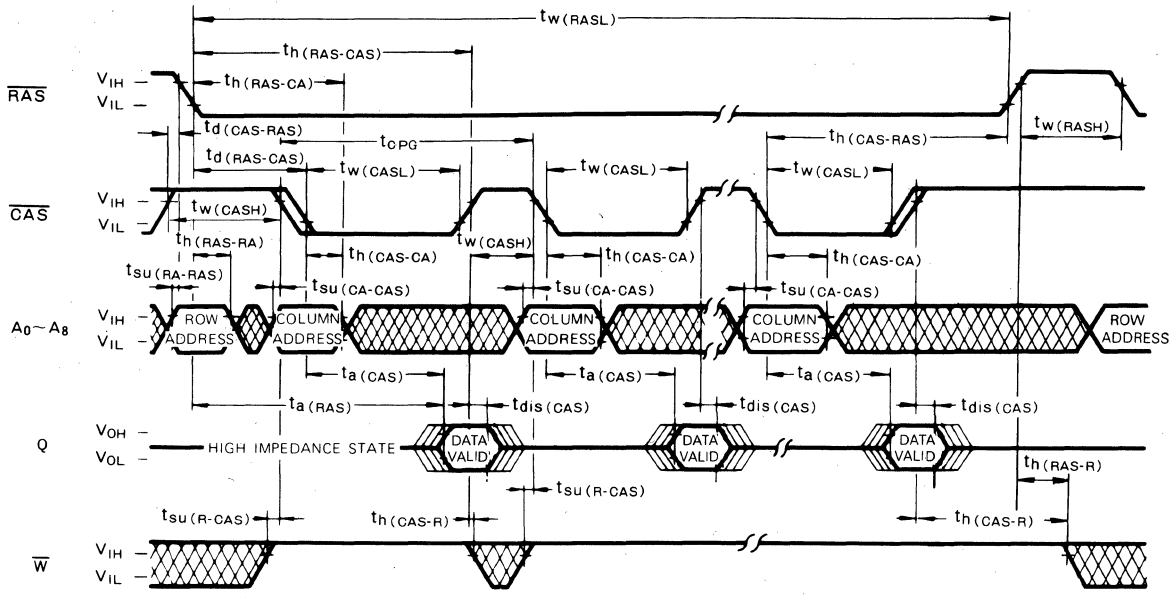



Note 19. Indicates the don't care input

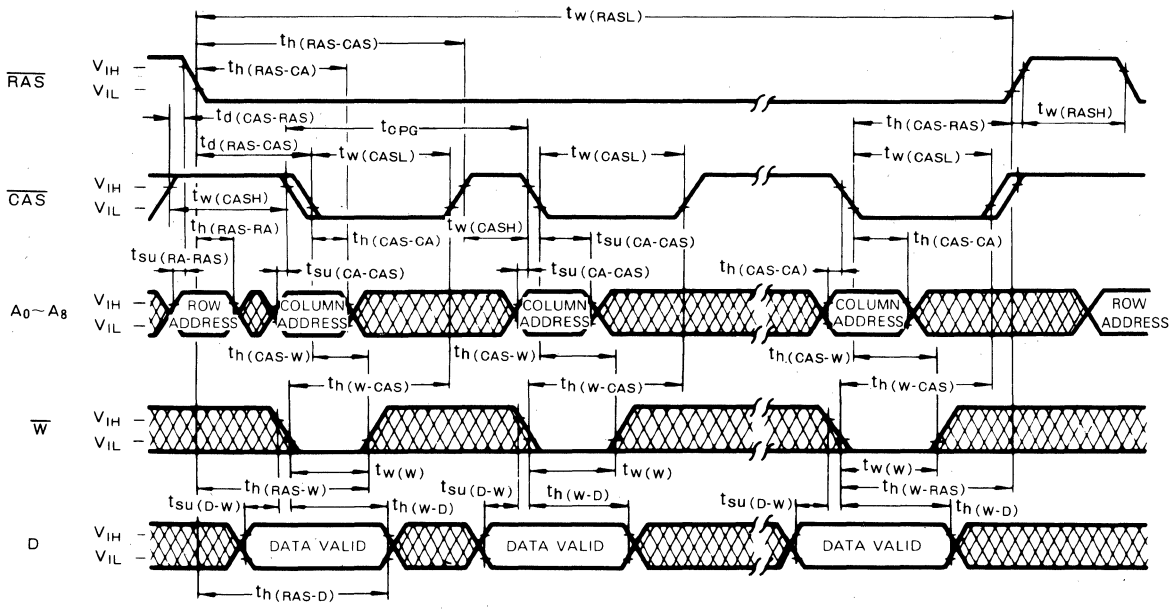
The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
$A_8$ may be $V_{IH}$ or $V_{IL}$.

## Page-Mode Read Cycle




## Page-Mode Write Cycle



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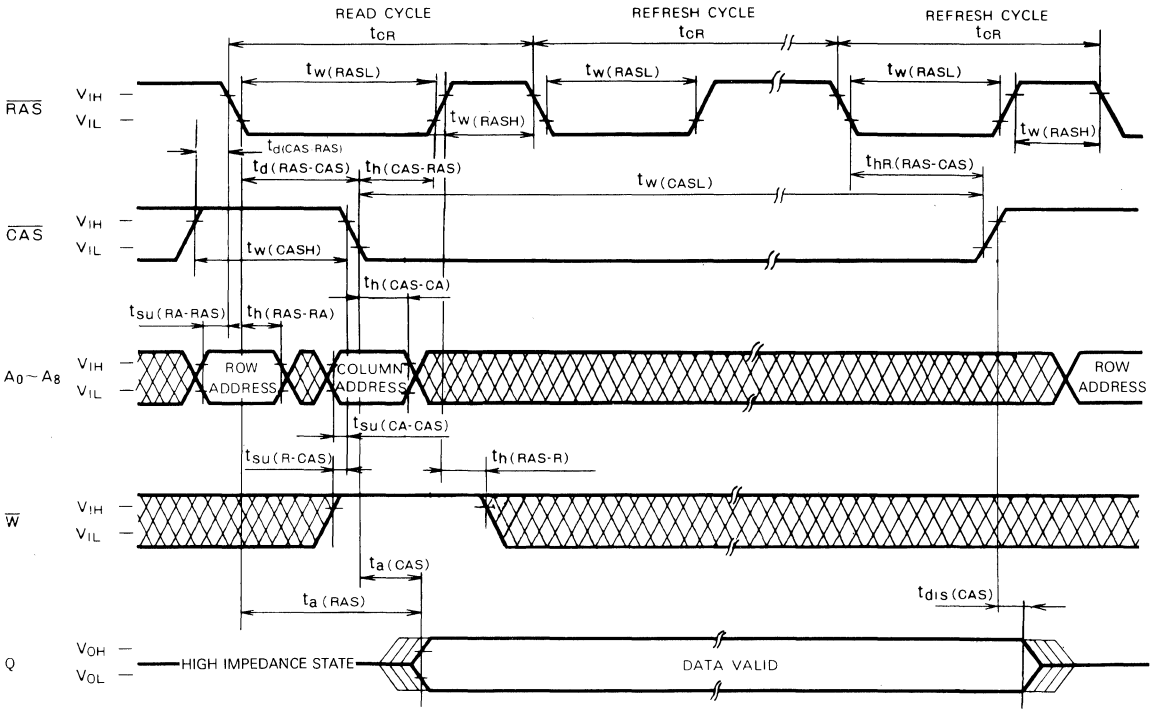
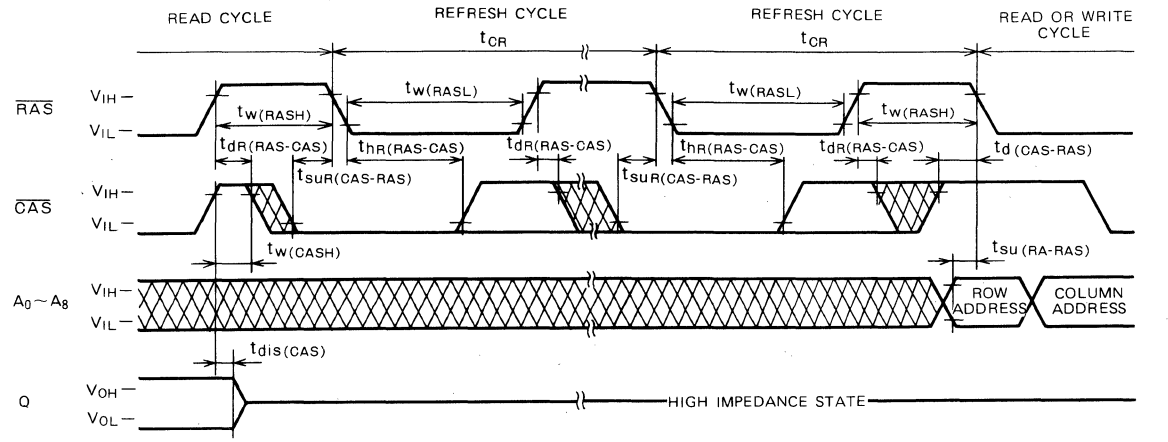
## Hidden Refresh Cycle



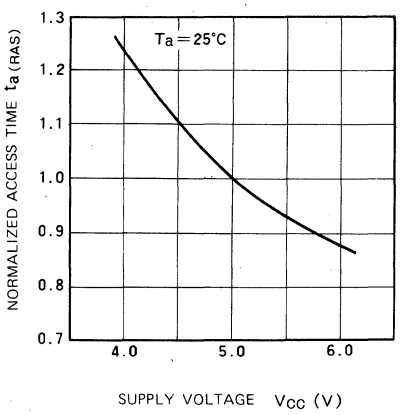

## CAS before RAS Refresh Cycle (Note 21)



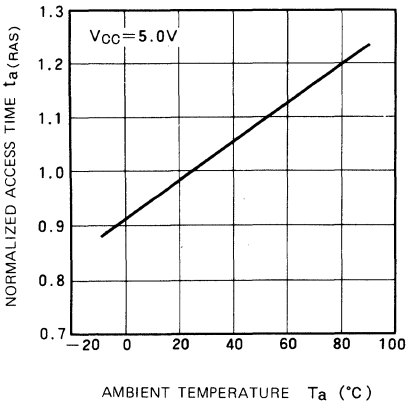

Note 21: W, D = don't care.

## TYPICAL CHARACTERISTICS

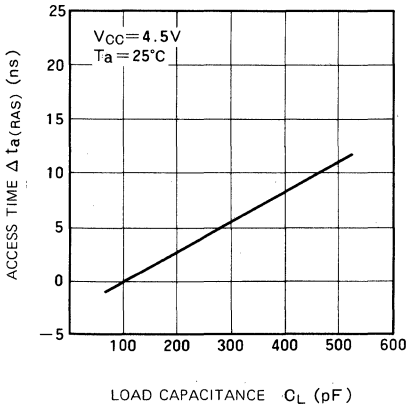
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



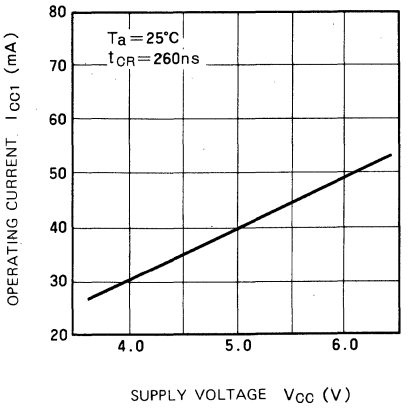

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



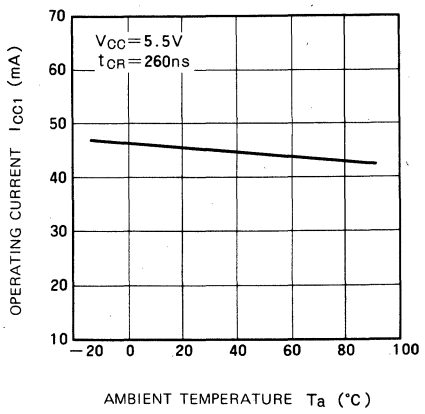

### ACCESS TIME VS. LOAD CAPACITANCE



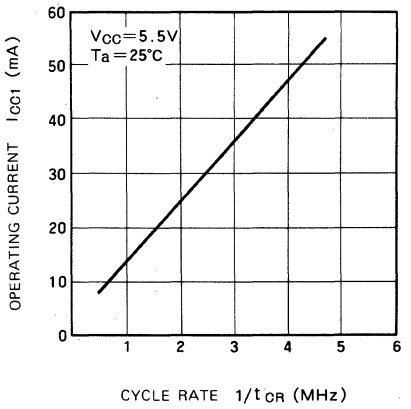

### OPERATING CURRENT VS. SUPPLY VOLTAGE



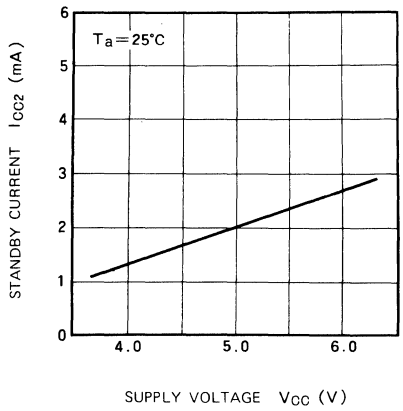

### OPERATING CURRENT VS. AMBIENT TEMPERATURE



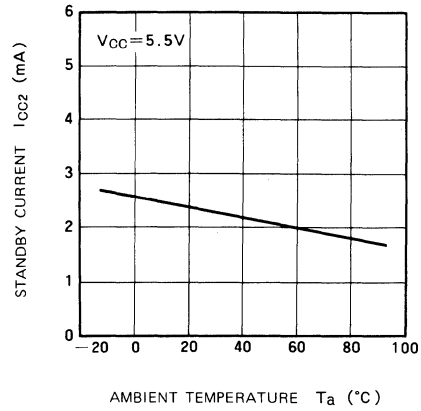

### OPERATING CURRENT VS. CYCLE RATE



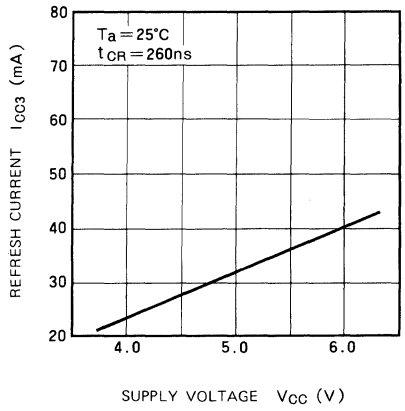
## STANDBY CURRENT VS. SUPPLY VOLTAGE



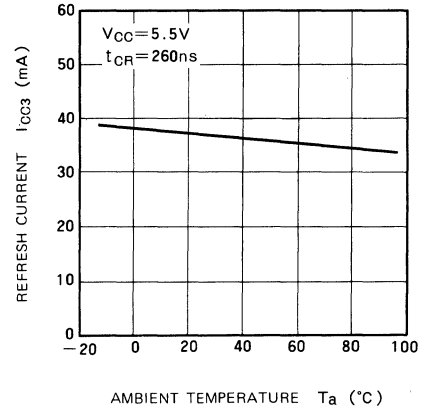

## STANDBY CURRENT VS. AMBIENT TEMPERATURE



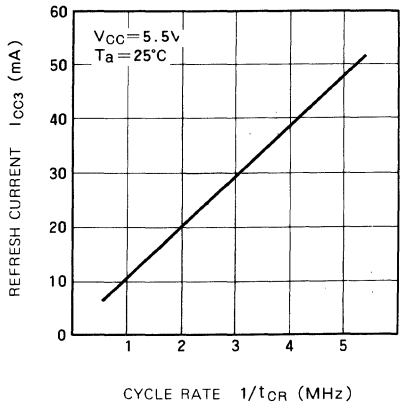

## REFRESH CURRENT VS. SUPPLY VOLTAGE



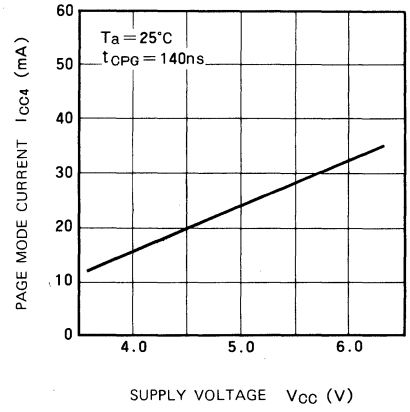

## REFRESH CURRENT VS. AMBIENT TEMPERATURE



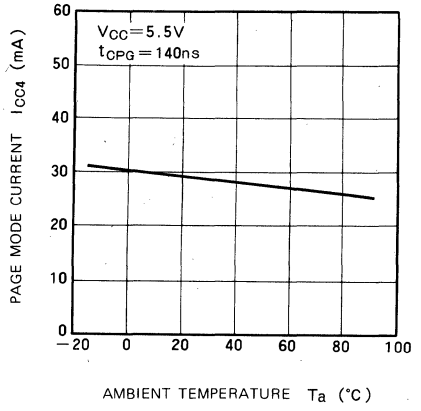

## REFRESH CURRENT VS. CYCLE RATE



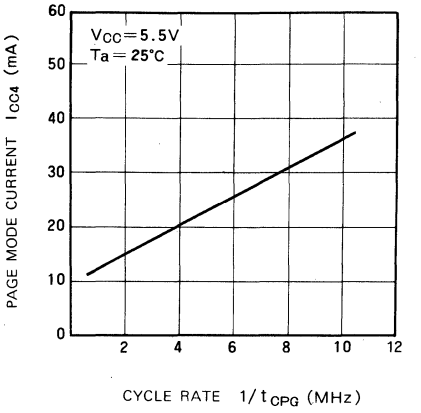

## PAGE MODE CURRENT VS. SUPPLY VOLTAGE



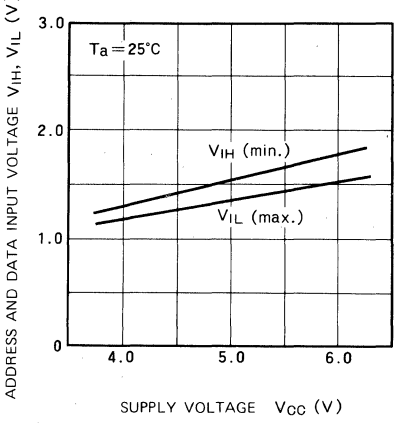
### PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



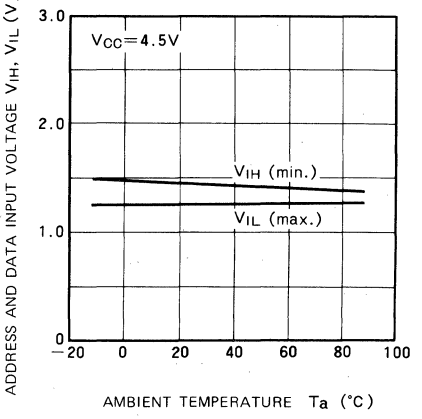

### PAGE MODE CURRENT VS. CYCLE RATE



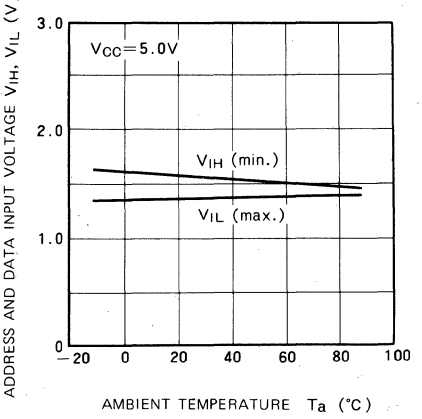

### ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



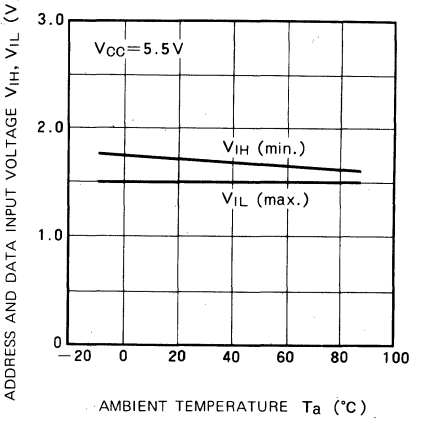

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



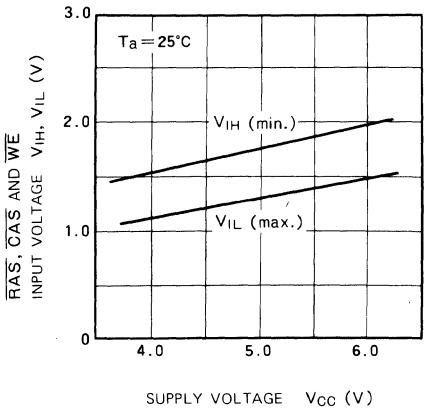

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



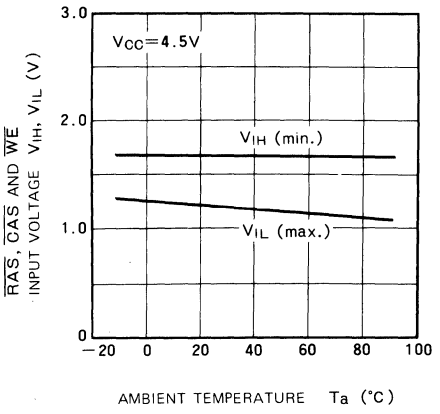

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



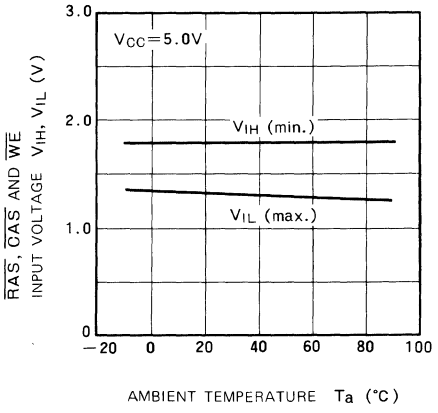
### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



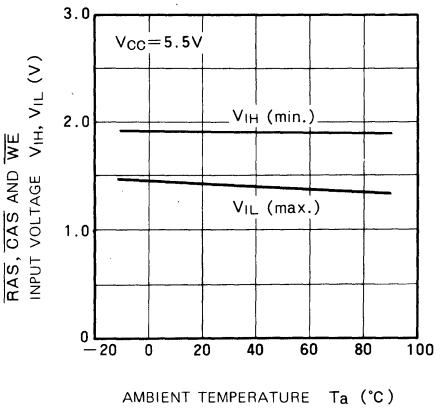

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



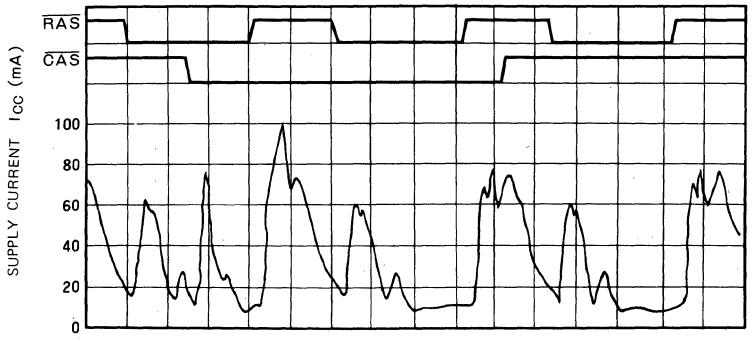

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE




### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

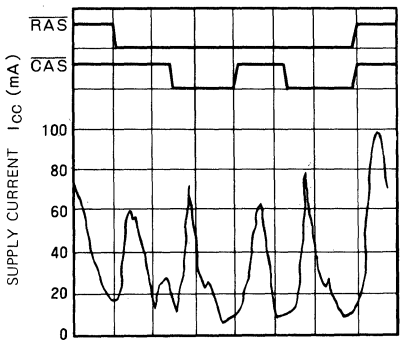


**RAS/CAS CYCLE** **HIDDEN REFRESH CYCLE** **RAS ONLY REFRESH CYCLE**



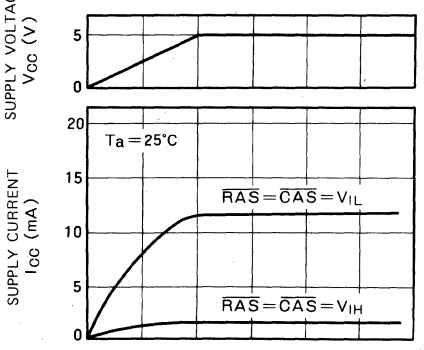

50ns/DIVISION

**PAGE MODE CYCLE**




50ns/DIVISION

**CURRENT WAVEFORM DURING POWER UP**




50μs/DIVISION

# M5M4257P-12, -15, -20

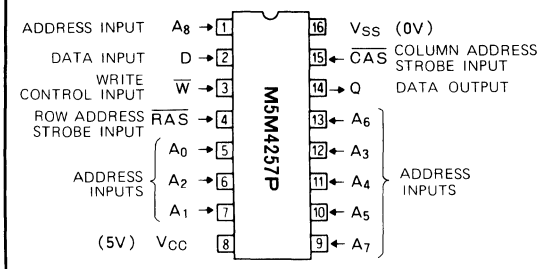
## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM

NEW PRODUCT

## DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P4**

## FEATURES

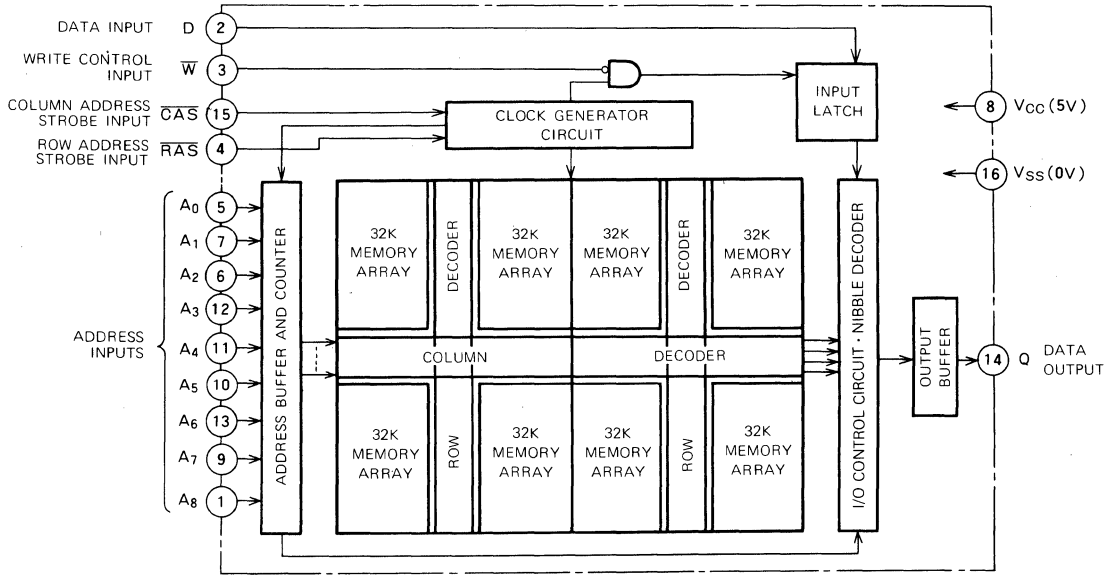
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4257P-12 | 120 | 230 | 260 |
| M5M4257P-15 | 150 | 260 | 230 |
| M5M4257P-20 | 200 | 330 | 190 |

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257P-12 . . . . . 360mW (max)
  - M5M4257P-15 . . . . . 330mW (max)
  - M5M4257P-20 . . . . . 275mW (max)
- Unlatched output enables two-dimensional chip selection
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities. (Pin 1 is used for nibble mode)
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM



## FUNCTION

The M5M4257P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Nibble mode identical except refresh is No. and Nibble mode column address is DNC while toggling $\overline{CAS}$.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4257P the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4257P is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257P, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Nibble-Mode Operation

The M5M4257P is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257P are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{suR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4257P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4257P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4257P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4257P operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta=25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta=0～70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦$V_{CC}$, Other input pins =0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4257P-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}=t_{CW}$= min, output open | | | 65 | mA |
| | | M5M4257P-15 | | | | 60 | mA |
| | | M5M4257P-20 | | | | 50 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}=\overline{CAS}=V_{IH}$ output open | | | 4.5 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4257P-12 | $\overline{RAS}$ cycling $\overline{CAS}=V_{IH}$ $t_{C(\overline{RAS})}$= min, output open | | | 55 | mA |
| | | M5M4257P-15 | | | | 50 | mA |
| | | M5M4257P-20 | | | | 40 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$ nibble mode | M5M4257P-12 | $\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling $t_{CN}$= min, output open | | | 30 | mA |
| | | M5M4257P-15 | | | | 25 | mA |
| | | M5M4257P-20 | | | | 23 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4257P-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ = min, output open | | | 60 | mA |
| | | M5M4257P-15 | | | | 55 | mA |
| | | M5M4257P-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I=V_{SS}$ f=1MHz $V_i$=25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O=V_{SS}$, f=1MHz, $V_i$=25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 20 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | −5 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for nibble-mode.
9: $t_{d(RAS-CAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)max}$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)max}$ defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2TTL, $C_L$ = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −10 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |

## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,min$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,min$ and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Nibble-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CN}$ | Nibble mode cycle time | $t_{NC}$ | 55 | | 70 | | 90 | | ns |
| $t_{aN(CAS)}$ | Nibble mode access time | $t_{NAC}$ | | 30 | | 40 | | 50 | ns |
| $t_{wN(CASL)}$ | Nibble mode $\overline{CAS}$ low pulse width | $t_{NCAS}$ | 30 | | 40 | | 50 | | ns |
| $t_{wN(CASH)}$ | Nibble mode precharge time | $t_{NP}$ | 15 | | 20 | | 30 | | ns |
| $t_{hN(CAS-RAS)}$ | Nibble mode $\overline{RAS}$ hold time | $t_{NRSH}$ | 30 | | 40 | | 50 | | ns |
| $t_{dN(CAS-W)}$ | Nibble mode $\overline{CAS}$ to WRITE delay | $t_{NCWD}$ | 30 | | 40 | | 50 | | ns |
| $t_{wNRMW(CASL)}$ | Nibble mode RMW $\overline{CAS}$ pulse width | $t_{NCRW}$ | 65 | | 85 | | 105 | | ns |
| $t_{hNRMW(W-CAS)}$ | Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time | $t_{NCWL}$ | 30 | | 40 | | 50 | | ns |
| $t_{hNRMW(CAS-RAS)}$ | Nibble mode RMW $\overline{RAS}$ hold time | $t_{NWSH}$ | 65 | | 85 | | 105 | | ns |
| $t_{suN(W-CAS)}$ | Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$ | $t_{NWCS}$ | 0 | | 0 | | 0 | | ns |

## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257P-12 | | M5M4257P-15 | | M5M4257P-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

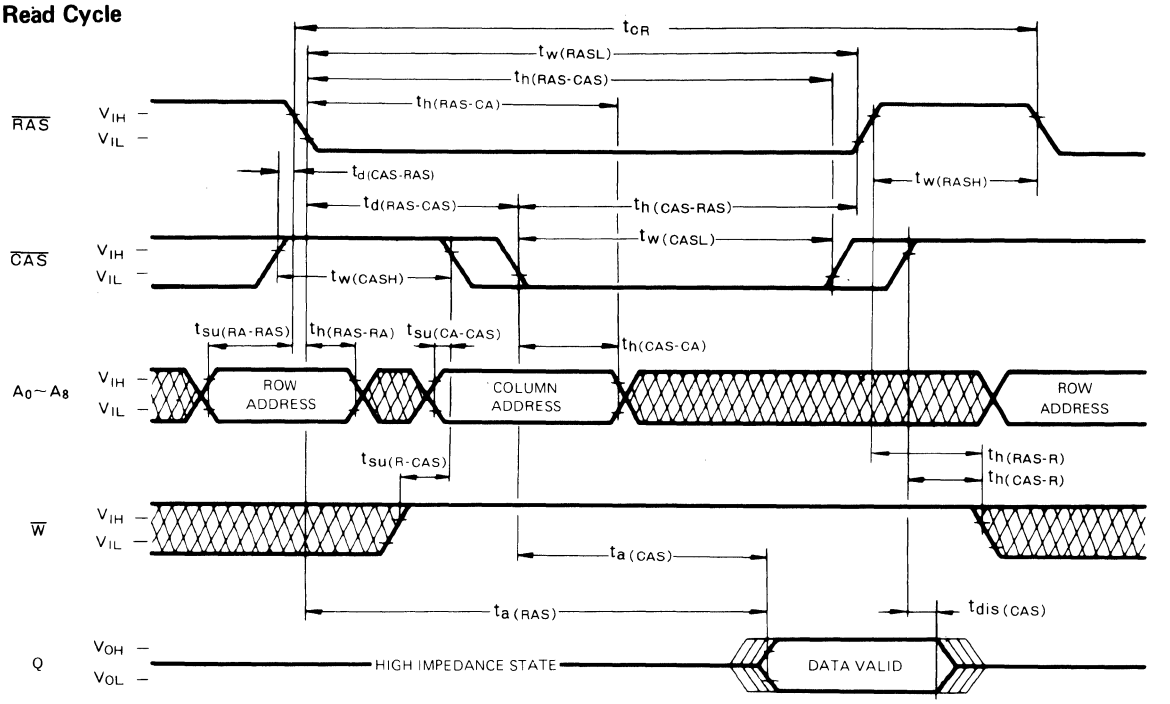
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## Nibble Mode Addressing Sequence Example

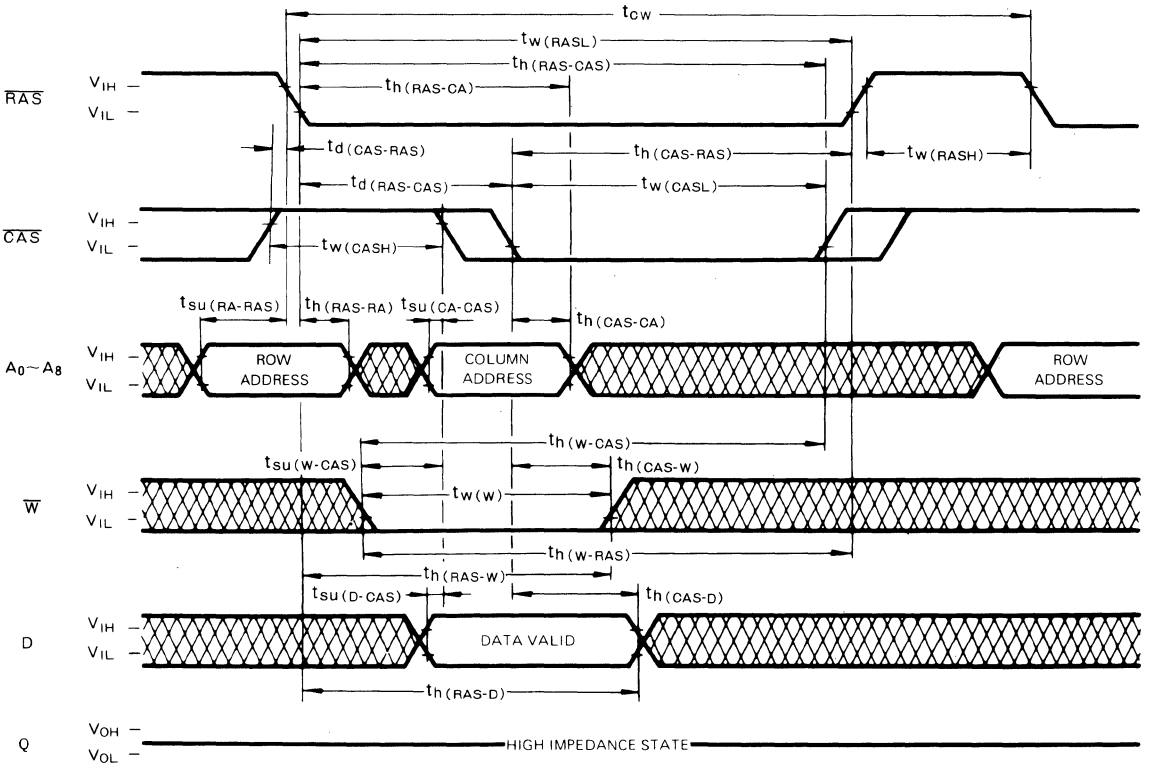
| Sequence | Nibble bit | Column address | | | | | | | | | Row address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | |
| $\overline{RAS}/\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | External address |
| toggle $\overline{CAS}$ | 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Internally generated address |
| toggle $\overline{CAS}$ | 3 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| toggle $\overline{CAS}$ | 4 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | |
| toggle $\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |

## TIMING DIAGRAMS (Note 19)

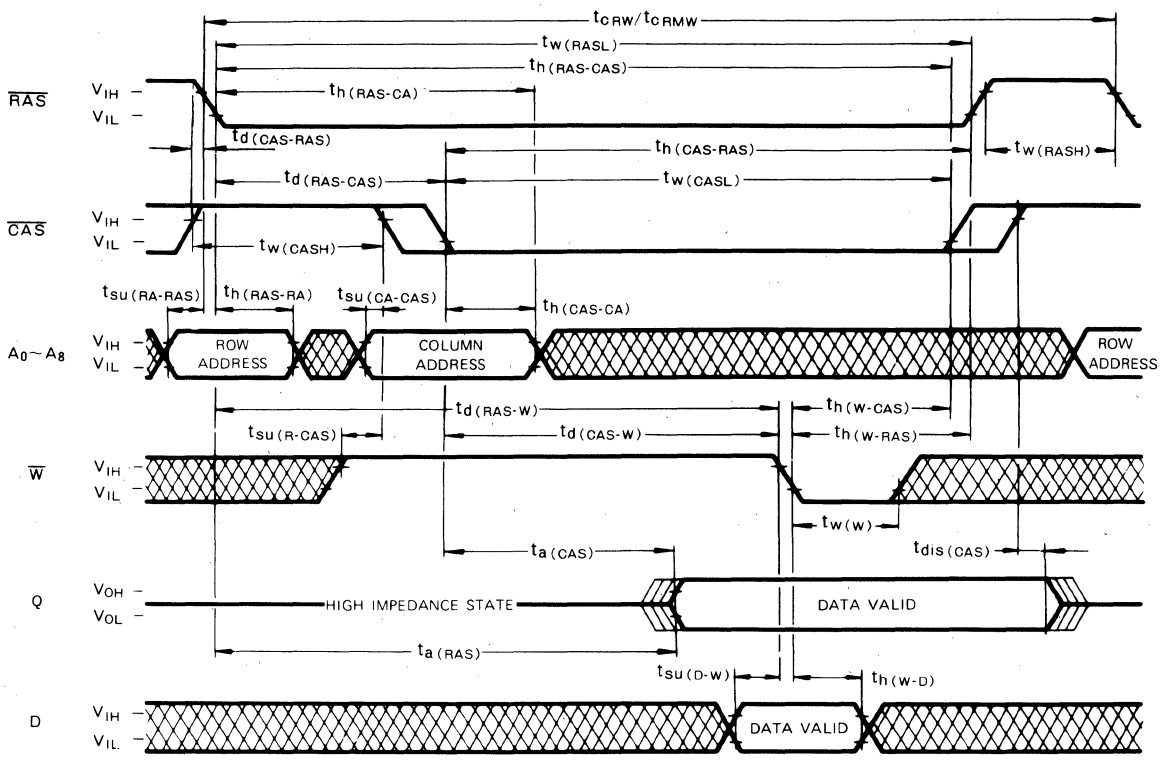
### Read Cycle



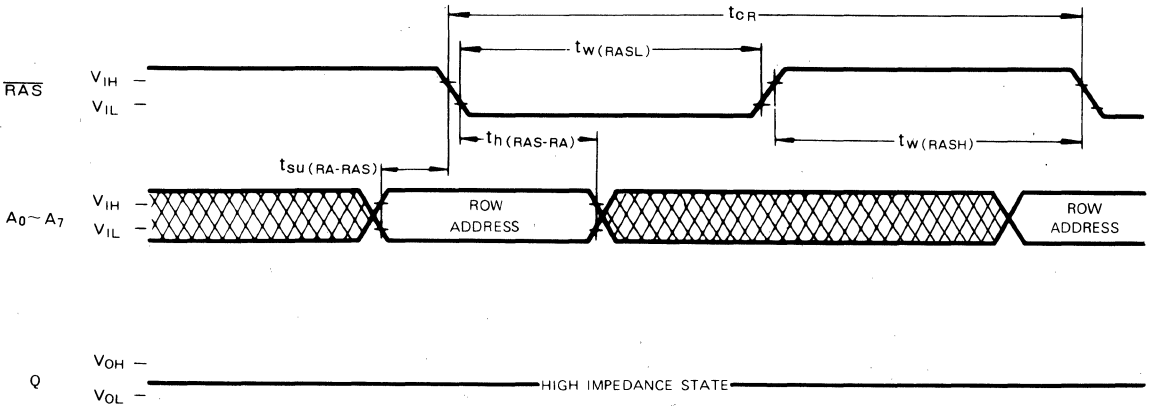

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 20)

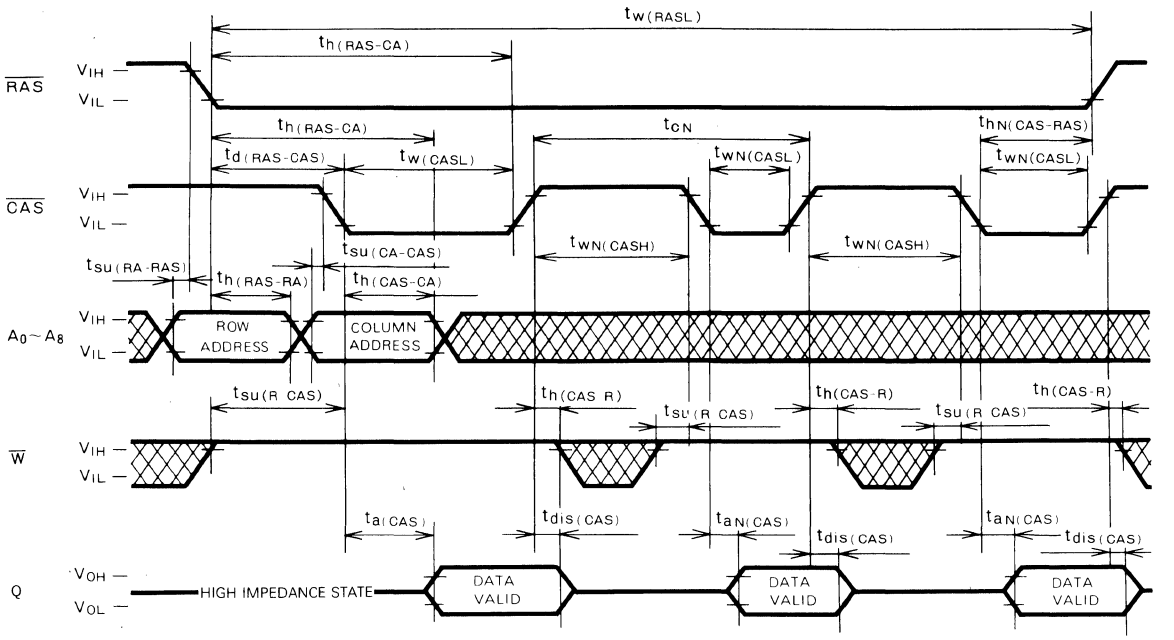



Note 19. Indicates the don't care input

The center-line indicates the high-impedance state

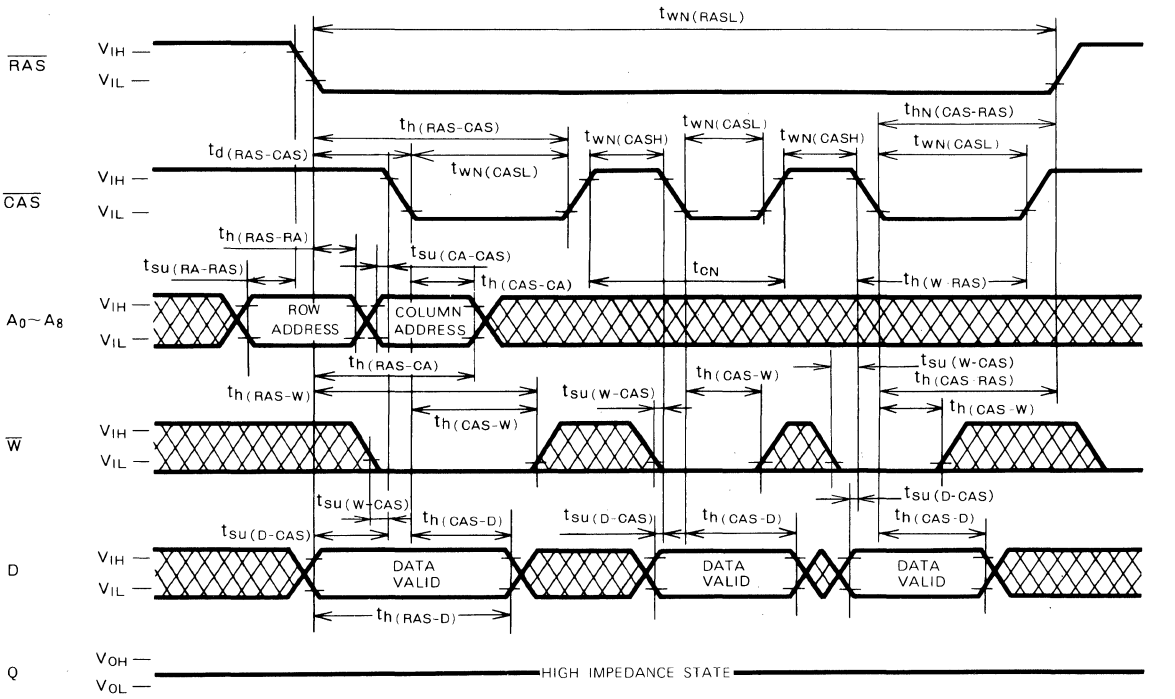
Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
$A_8$ may be $V_{IH}$ or $V_{IL}$.

## Nibble Mode Read Cycle (Note 21)

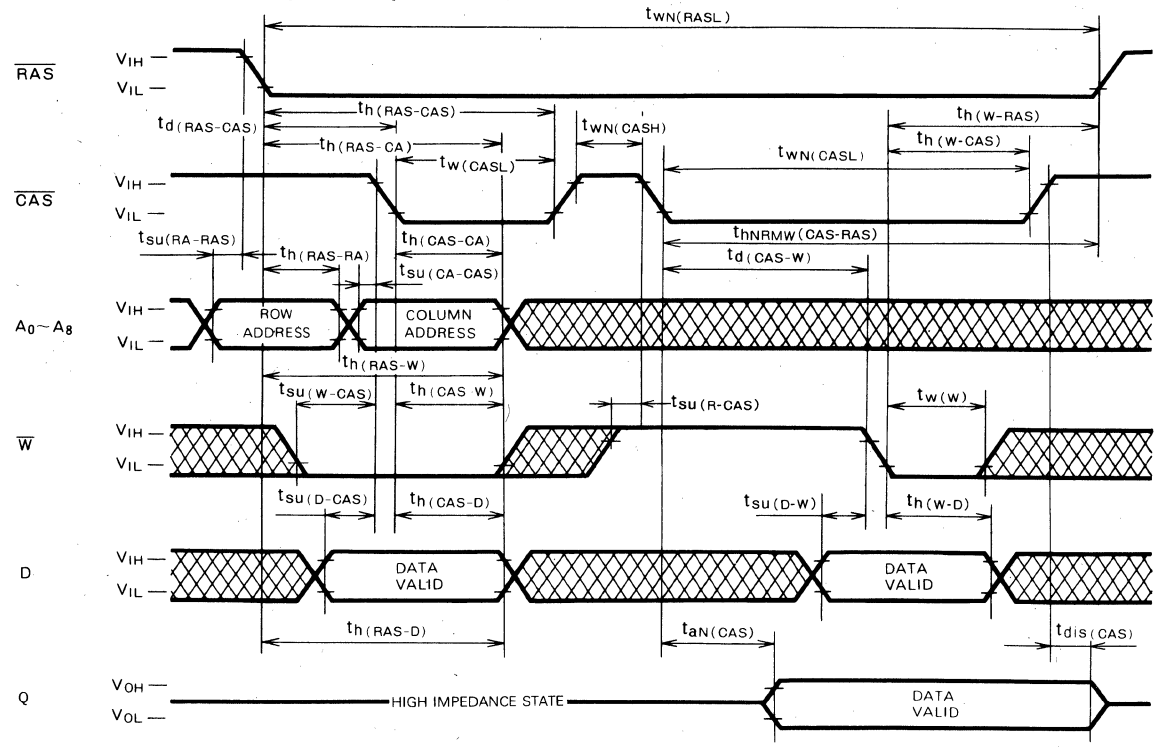



Note 21. Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

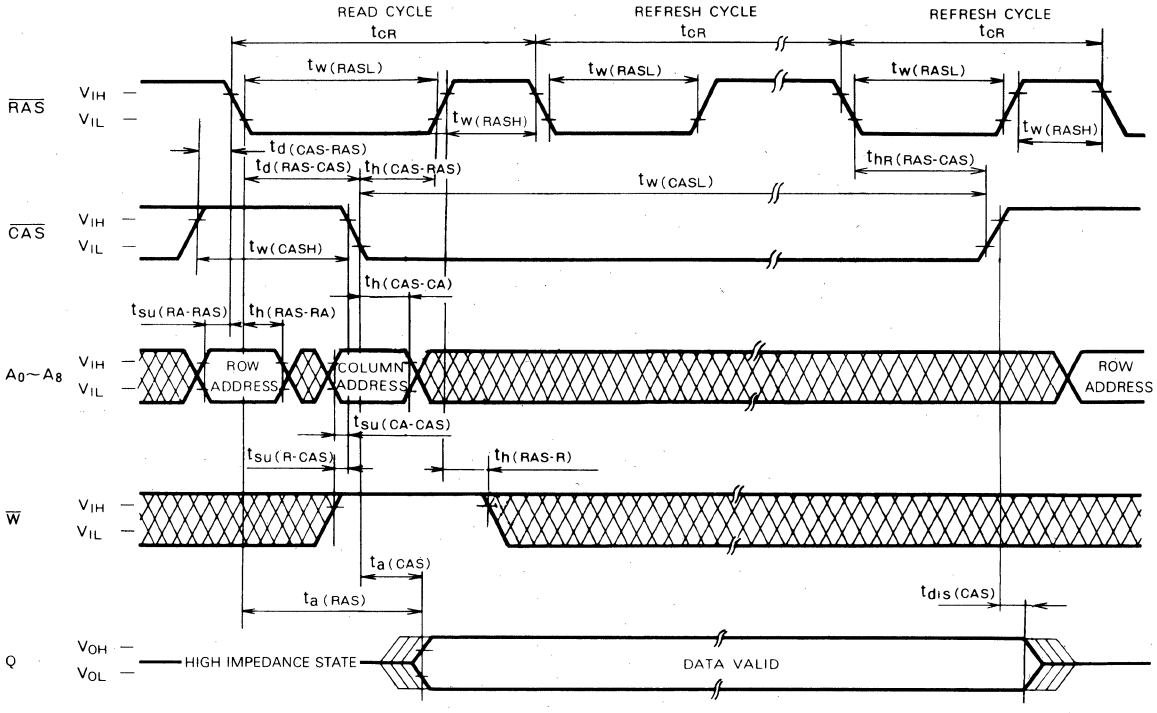
## Nibble Mode Write Cycle (Early Write)



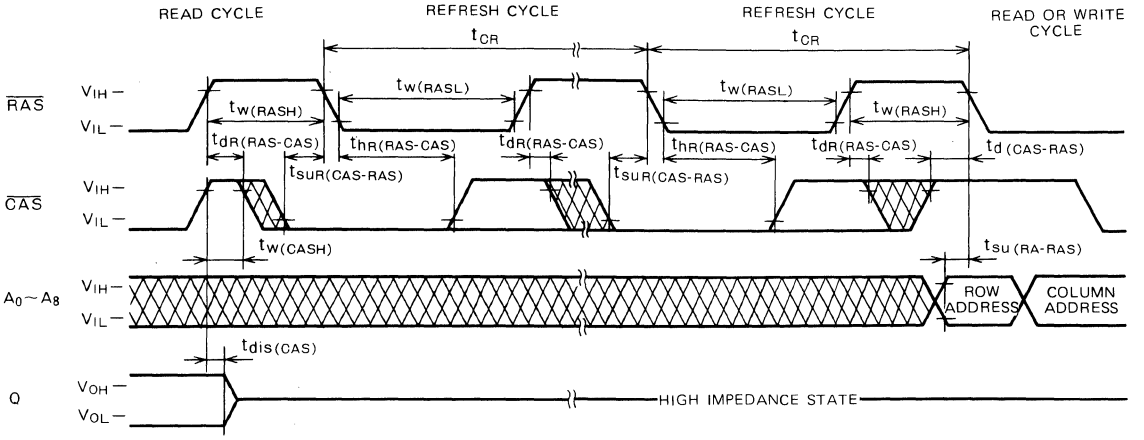
## Nibble Mode Read-Modify-Write Cycle




## Hidden Refresh Cycle



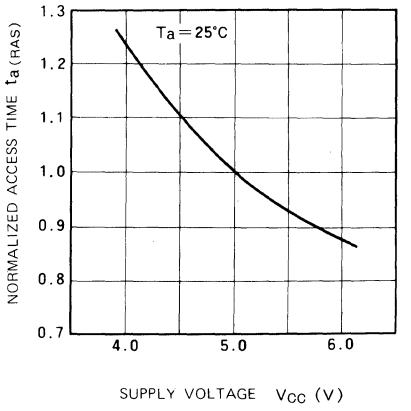
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)



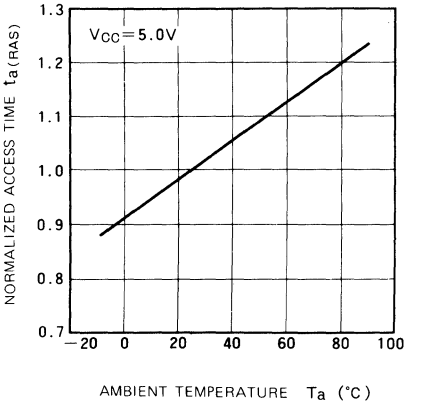

Note 22: $\overline{W}$, D = don't care.

## TYPICAL CHARACTERISTICS

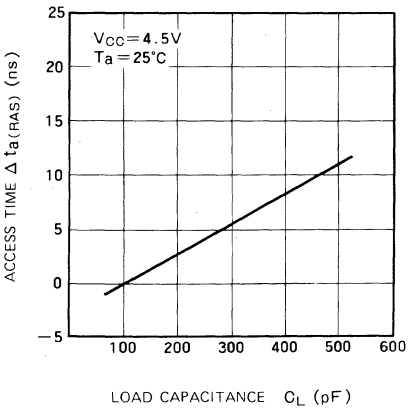
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



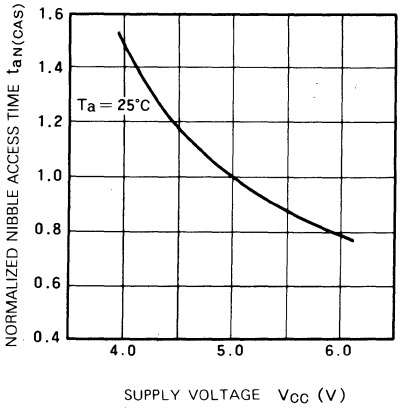

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



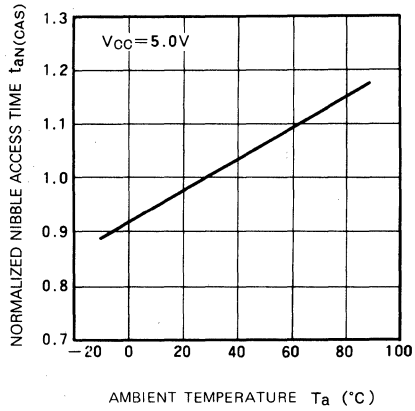

### ACCESS TIME VS. LOAD CAPACITANCE



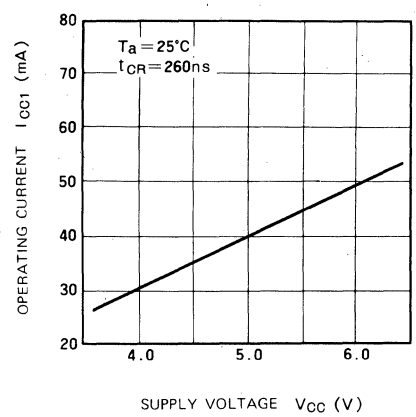

### NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE



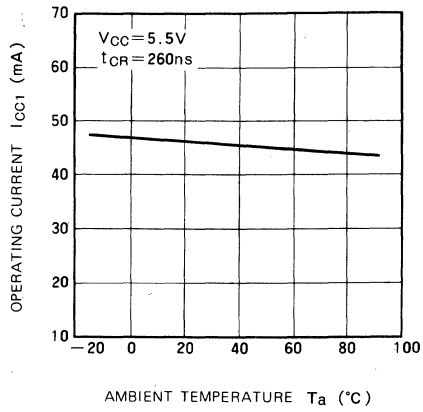
### NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



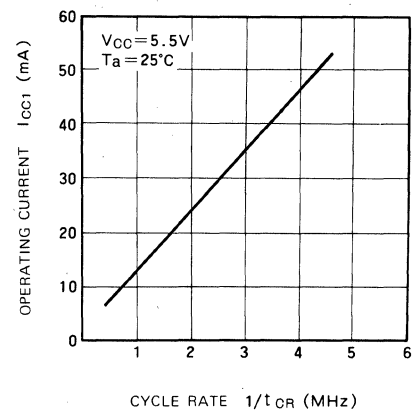

### OPERATING CURRENT VS. SUPPLY VOLTAGE



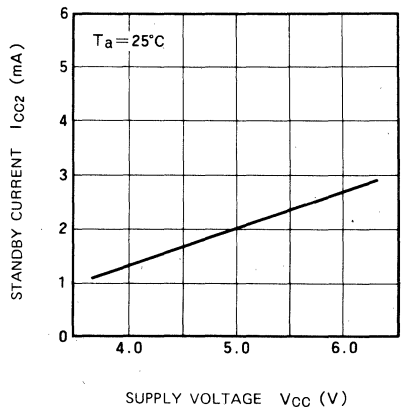

### OPERATING CURRENT VS. AMBIENT TEMPERATURE



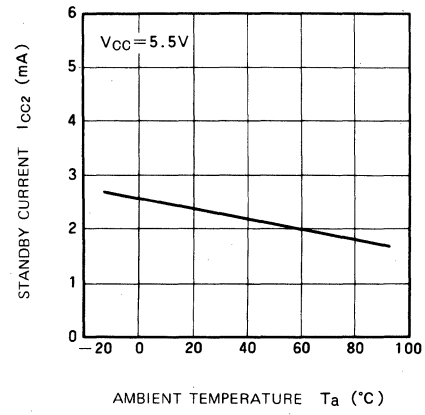

### OPERATING CURRENT VS. CYCLE RATE



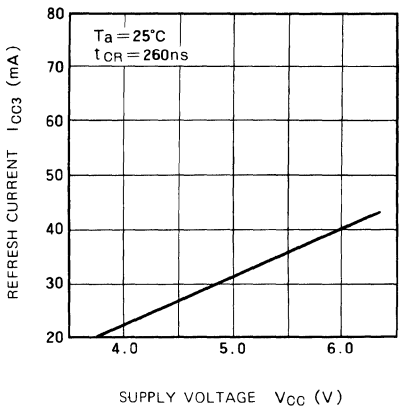

### STANDBY CURRENT VS. SUPPLY VOLTAGE



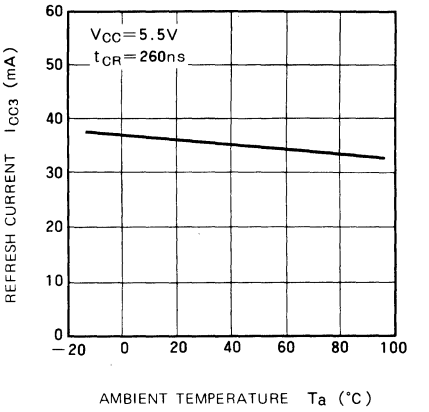

### STANDBY CURRENT VS. AMBIENT TEMPERATURE



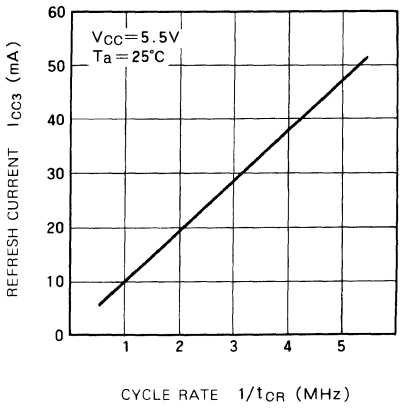
### REFRESH CURRENT VS. SUPPLY VOLTAGE



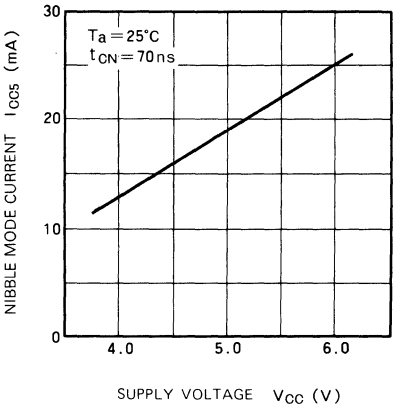

### REFRESH CURRENT VS. AMBIENT TEMPERATURE



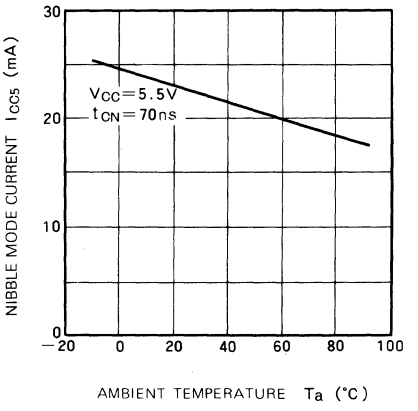

### REFRESH CURRENT VS. CYCLE RATE



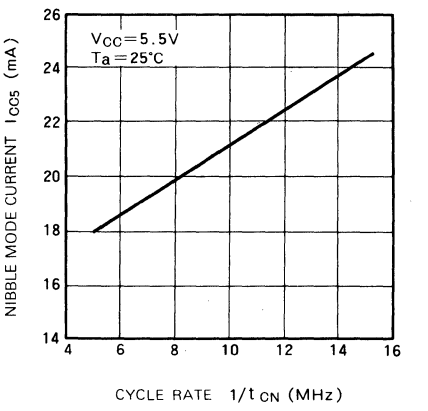

### NIBBLE MODE CURRENT VS. SUPPLY VOLTAGE



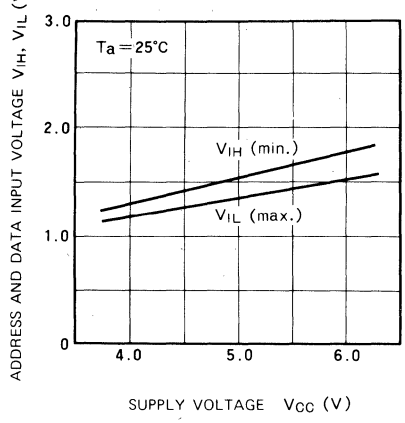

### NIBBLE MODE CURRENT VS. AMBIENT TEMPERATURE



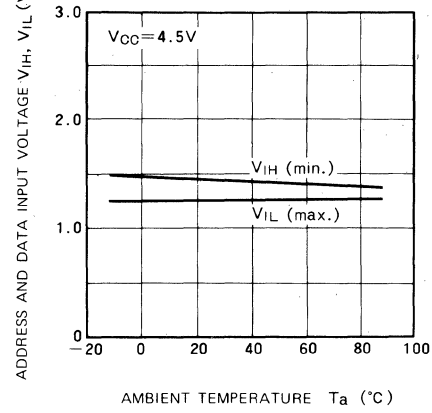

### NIBBLE MODE CURRENT VS. CYCLE RATE



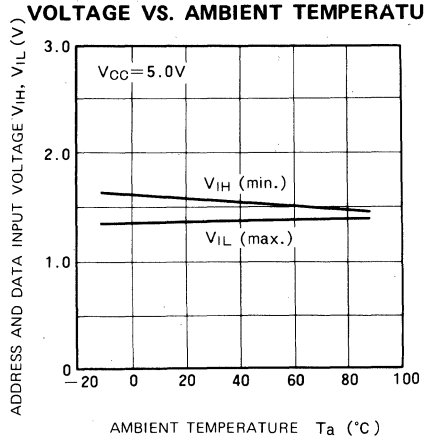
## ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



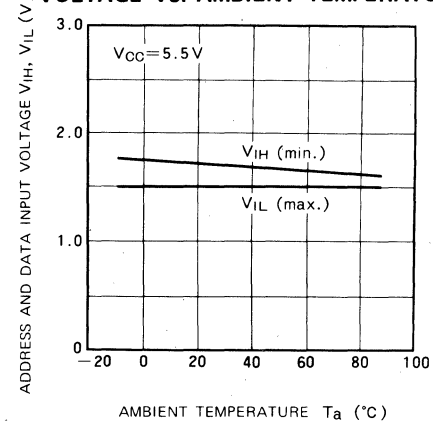

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



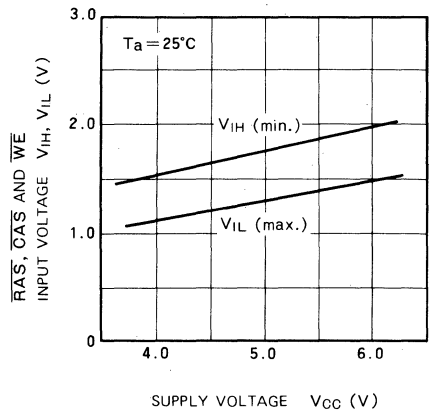

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



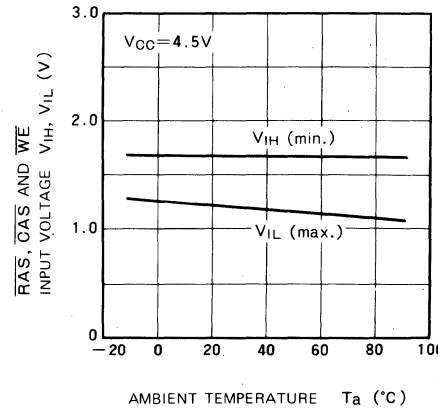

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



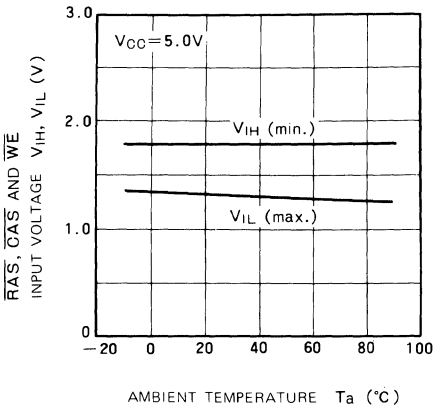

## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



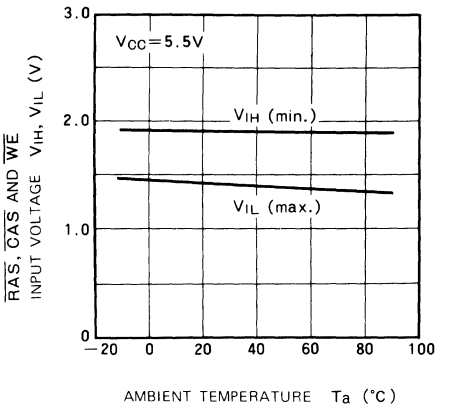

## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



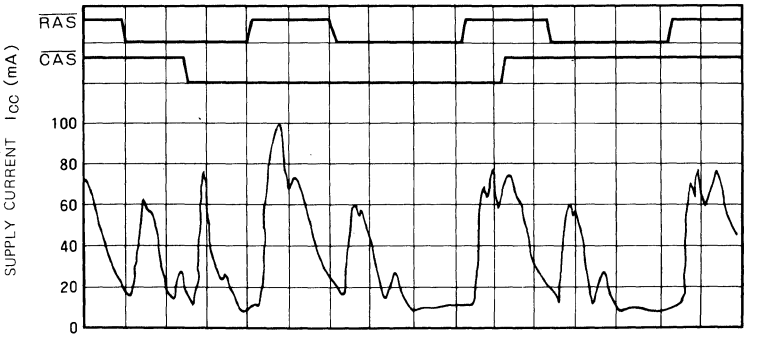
### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE




### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

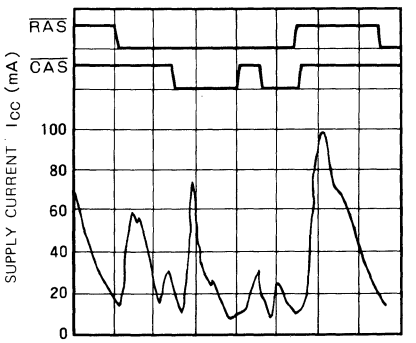



### $\overline{RAS}$/$\overline{CAS}$ CYCLE — HIDDEN REFRESH CYCLE — $\overline{RAS}$ ONLY REFRESH CYCLE



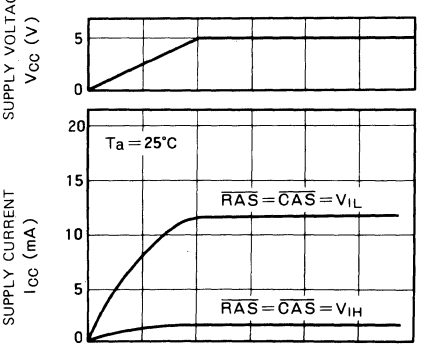

50ns/DIVISION

### NIBBLE MODE CYCLE




50ns/DIVISION

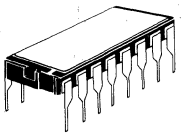
### CURRENT WAVEFORM DURING POWER UP




50μs/DIVISION

# M5M4256S-12, -15, -20

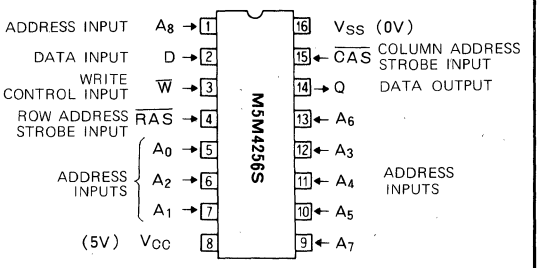
## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM



## DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16S1**

## FEATURES

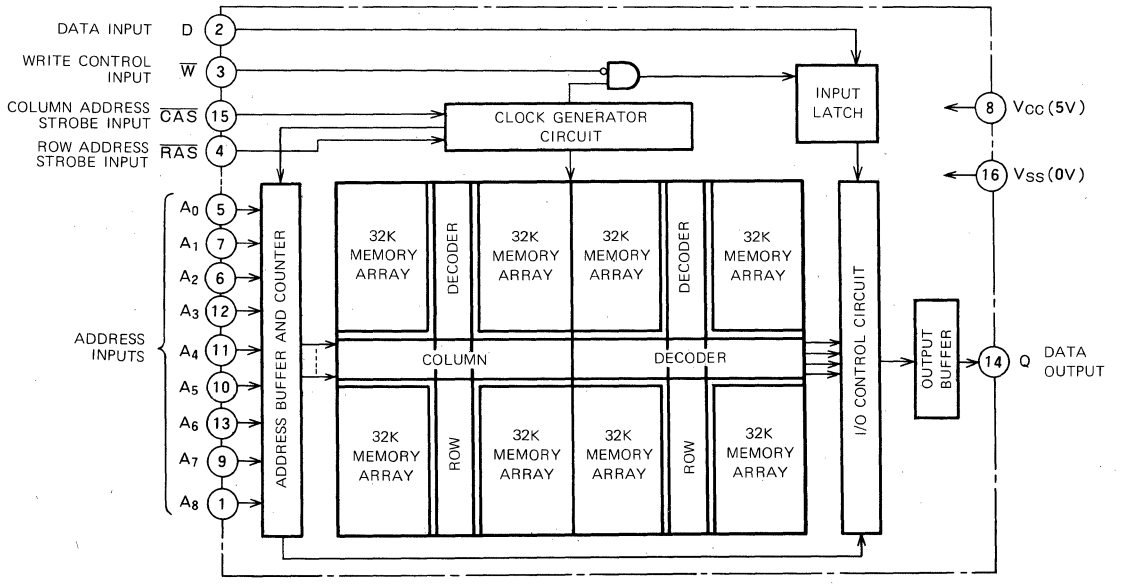
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4256S-12 | 120 | 230 | 260 |
| M5M4256S-15 | 150 | 260 | 230 |
| M5M4256S-20 | 200 | 330 | 190 |

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  - M5M4256S-12 . . . . . 413mW (max)
  - M5M4256S-15 . . . . . 385mW (max)
  - M5M4256S-20 . . . . . 303mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## FUNCTION

The M5M4256S provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Page mode identical except refresh is No.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4256S the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4256S is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256S, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256S must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256S are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4256S is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4256S is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256S as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4256S operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V ± 10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦$V_{CC}$, Other input pins ＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4256S-12 | $\overline{RAS}$, $\overline{CAS}$ cycling<br>$t_{CR}$＝$t_{CW}$＝ min, output open | | | 75 | mA |
| | | M5M4256S-15 | | | | 70 | mA |
| | | M5M4256S-20 | | | | 55 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$\overline{CAS}$＝$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4256S-12 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$<br>$t_{c(\overline{RAS})}$＝ min, output open | | | 60 | mA |
| | | M5M4256S-15 | | | | 55 | mA |
| | | M5M4256S-20 | | | | 45 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5M4256S-12 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling<br>$t_{CPG}$＝ min, output open | | | 55 | mA |
| | | M5M4256S-15 | | | | 50 | mA |
| | | M5M4256S-20 | | | | 45 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4256S-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling<br>$t_{c(\overline{RAS})}$ = min, output open | | | 60 | mA |
| | | M5M4256S-15 | | | | 55 | mA* |
| | | M5M4256S-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$<br>f＝1MHz<br>Vi＝25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{w(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{w(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{w(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$max is specified reference point only;if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\text{min} = t_{h(RAS-RA)}\text{min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)}\text{min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13: This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$max. Test conditions ; Load = 2TTL, $C_L$ = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |

## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RAS\,H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$min, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CPG}$ | Page-mode cycle time | $t_{PC}$ | 125 | | 145 | | 190 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | 80 | | ns |
| $t_{CPGRW}$ | Page-mode RW cycle time | $t_{PCRW}$ | 160 | | 180 | | 230 | | ns |
| $t_{CPGRMW}$ | Page-mode RMW cycle time | $t_{PCRMW}$ | 170 | | 195 | | 250 | | ns |

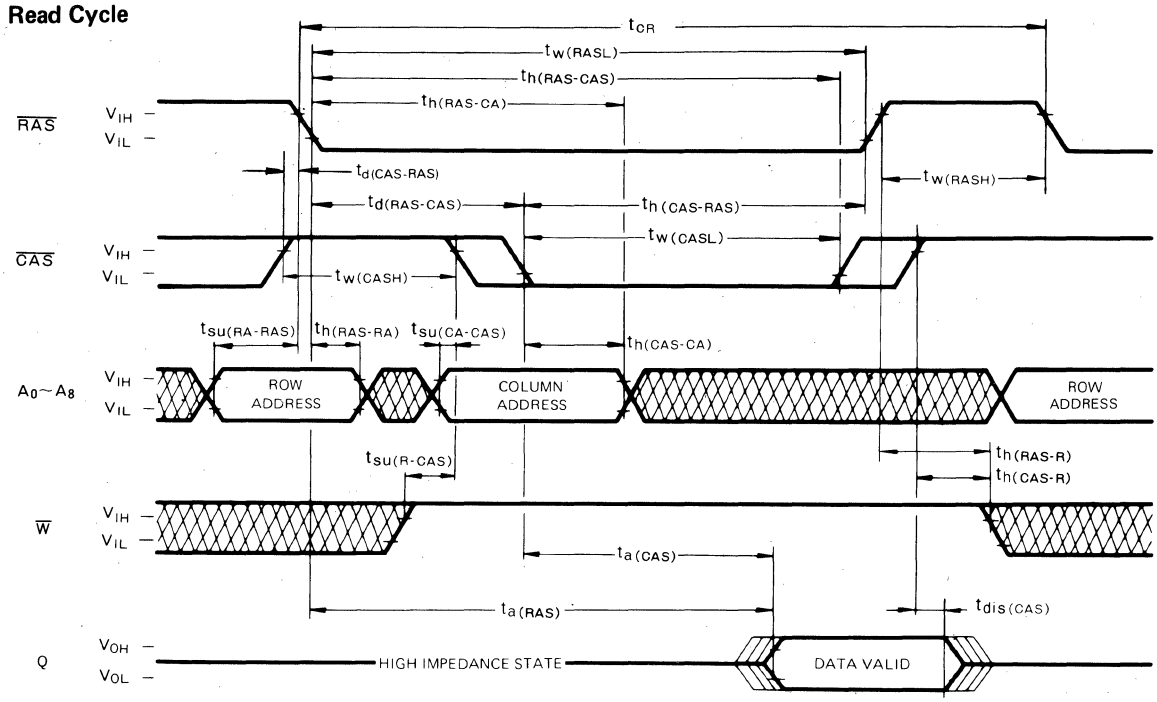
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256S-12 | | M5M4256S-15 | | M5M4256S-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

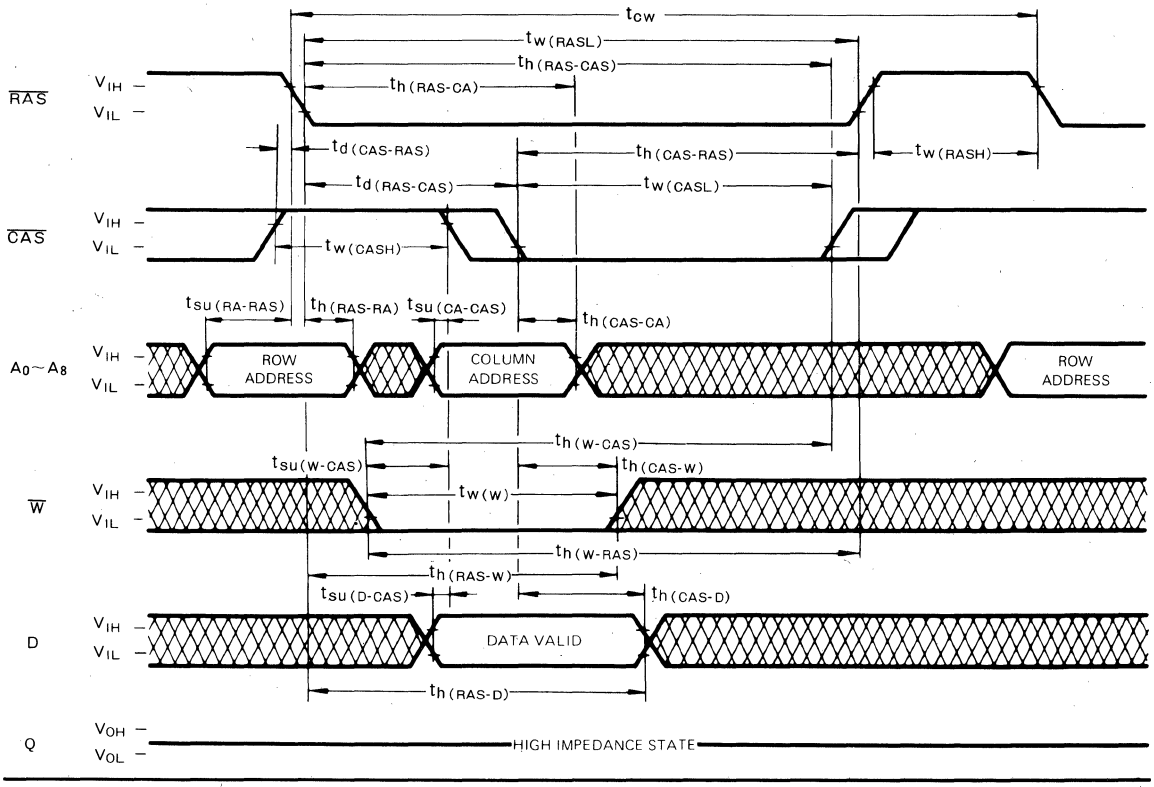
Note 18: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## TIMING DIAGRAMS (Note 19)

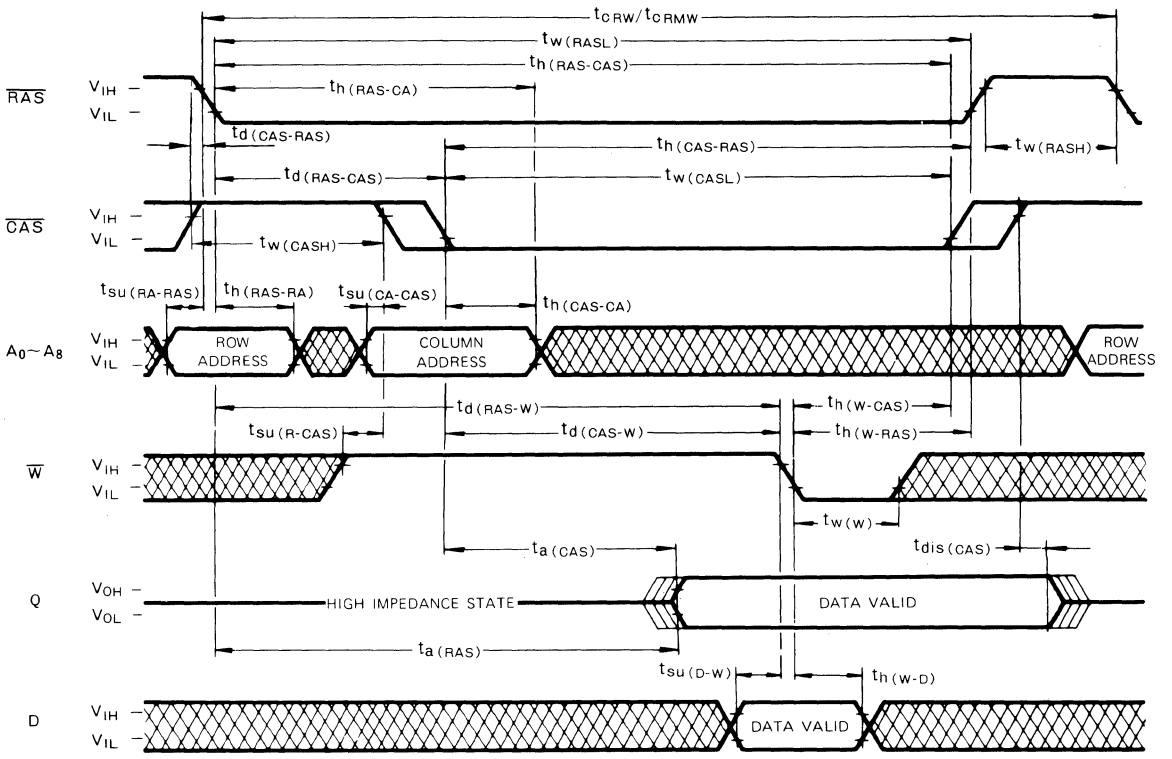
### Read Cycle



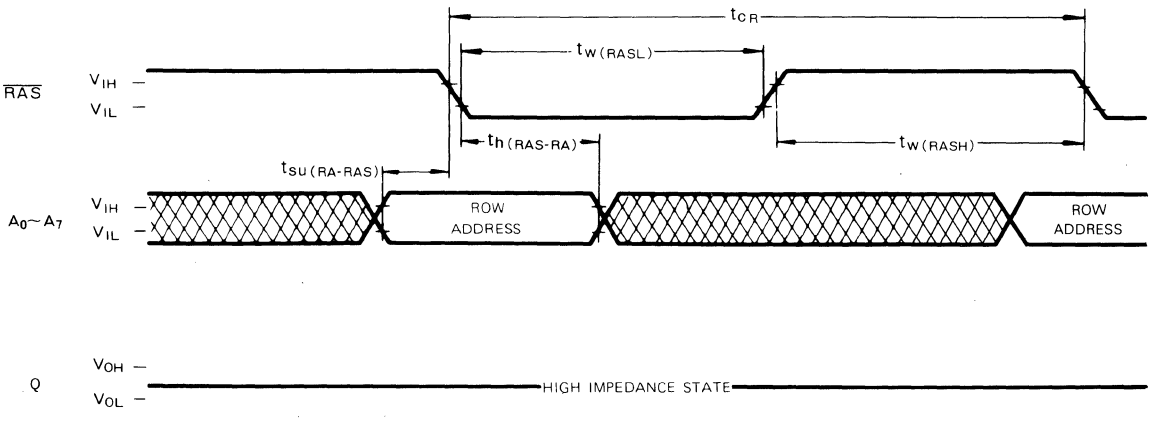

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles

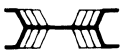



## RAS-Only Refresh Cycle (Note 20)




Note 19.

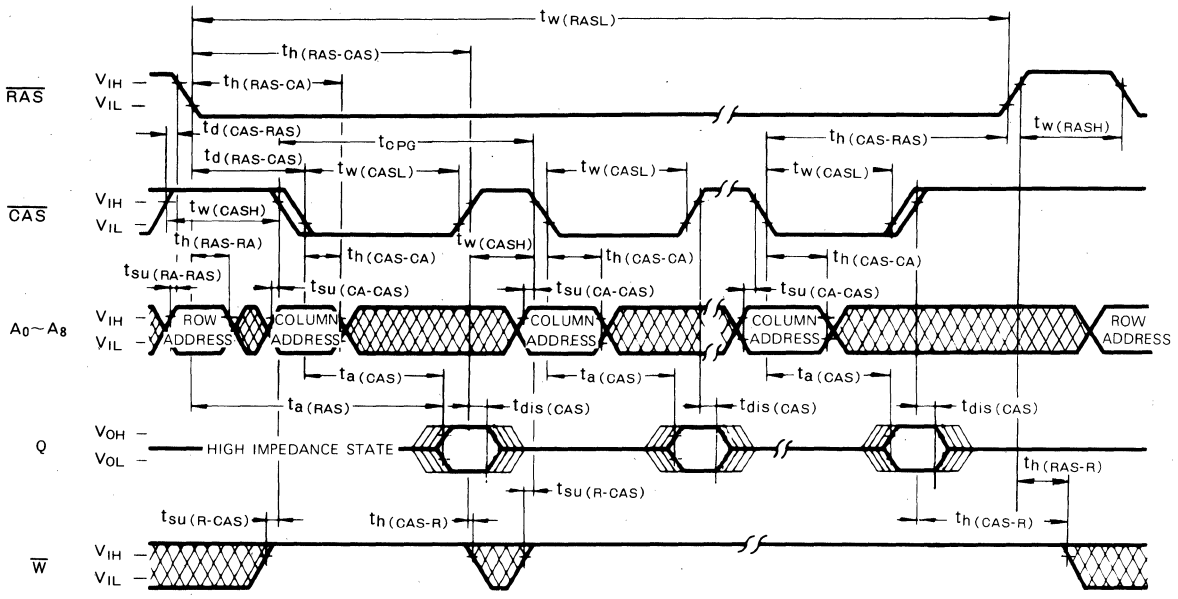
Indicates the don't care input



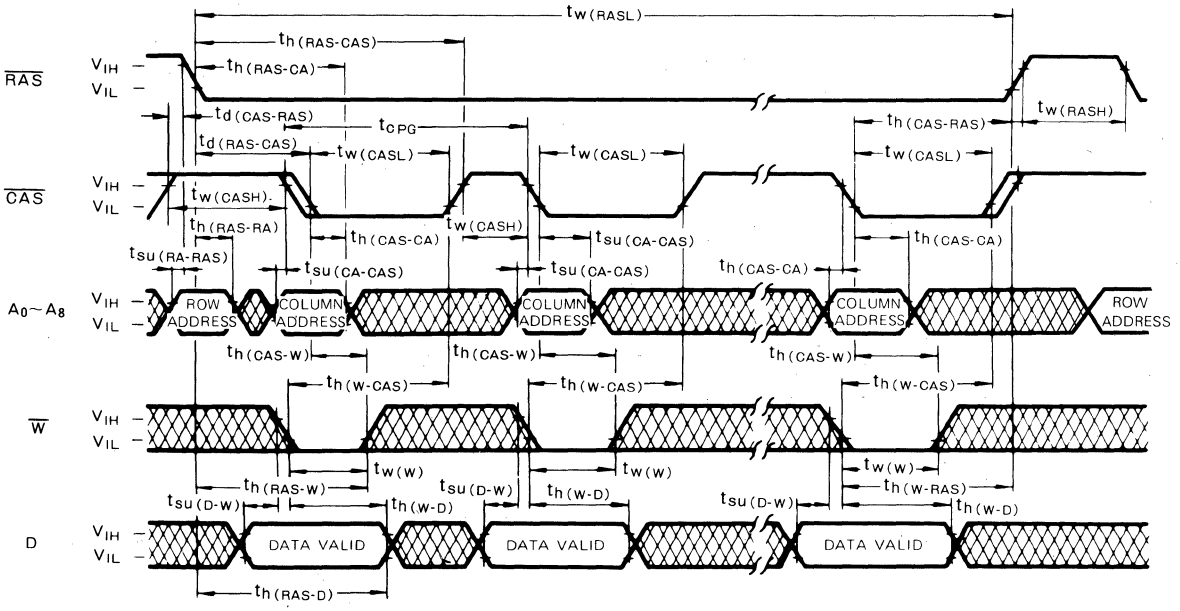
The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
A8 may be $V_{IH}$ or $V_{IL}$.

## Page-Mode Read Cycle




## Page-Mode Write Cycle



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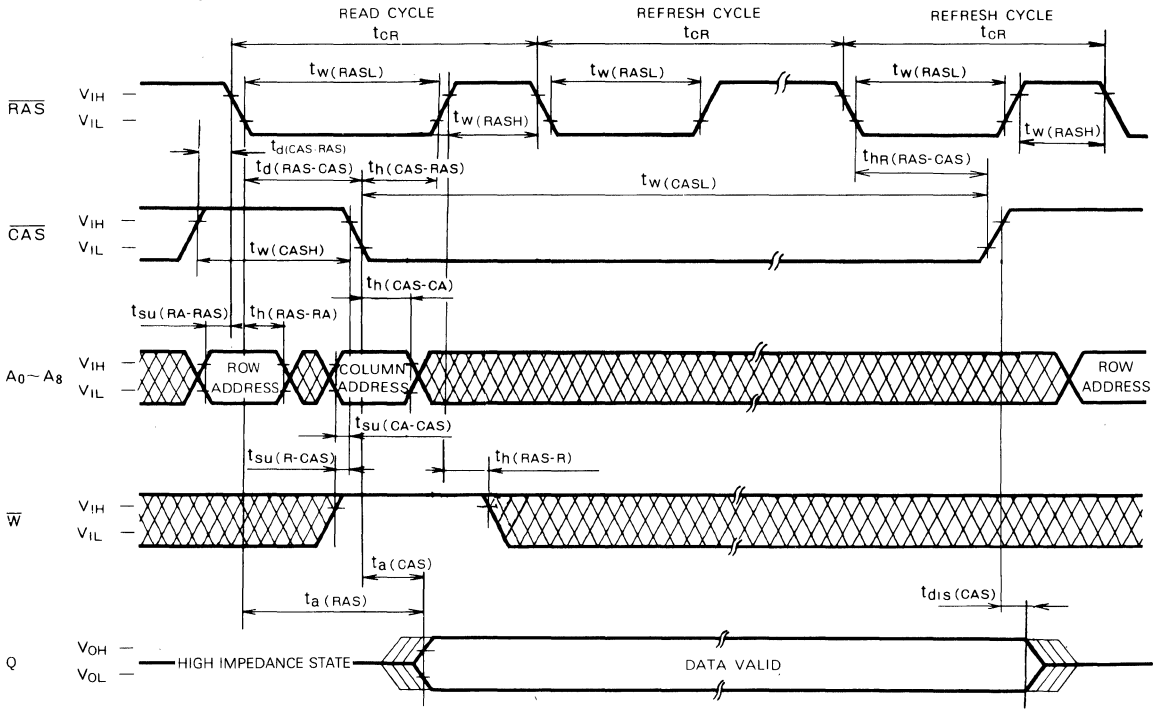
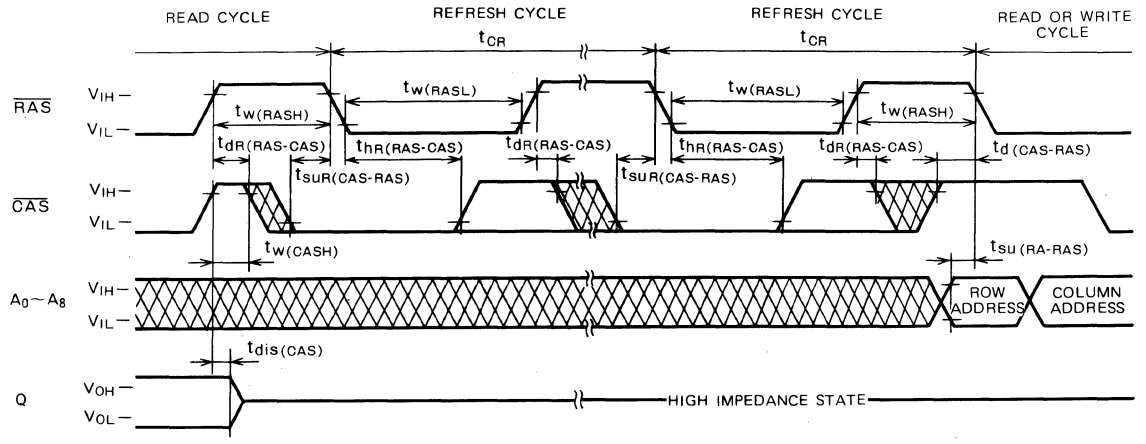
## Hidden Refresh Cycle



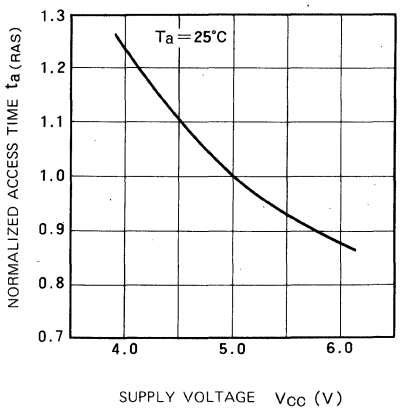

## CAS before RAS Refresh Cycle (Note 21)



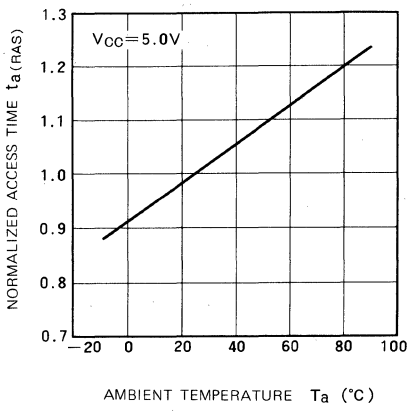

Note 21: $\overline{W}$, D = don't care.

## TYPICAL CHARACTERISTICS

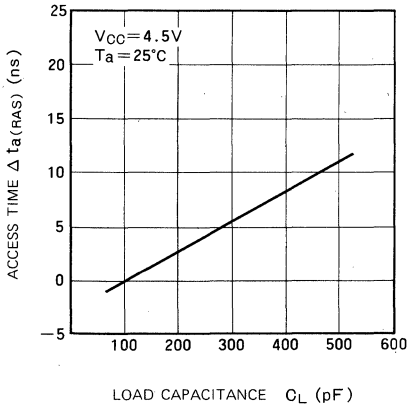
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



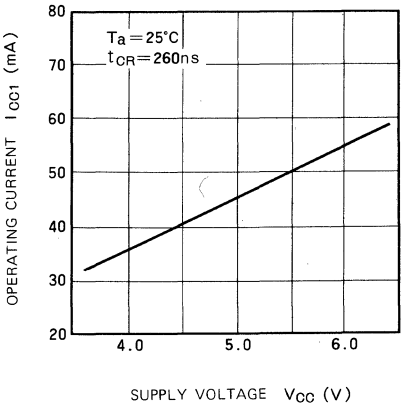

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



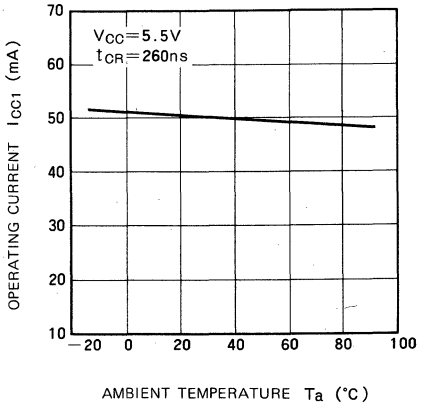

### ACCESS TIME VS. LOAD CAPACITANCE



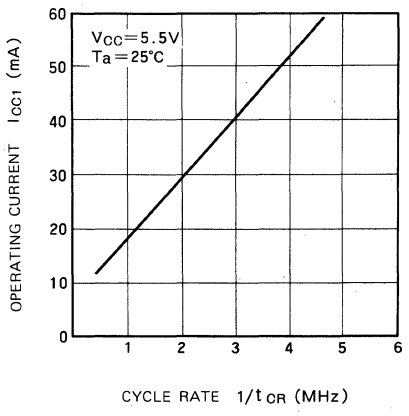

### OPERATING CURRENT VS. SUPPLY VOLTAGE




### OPERATING CURRENT VS. AMBIENT TEMPERATURE




### OPERATING CURRENT VS. CYCLE RATE



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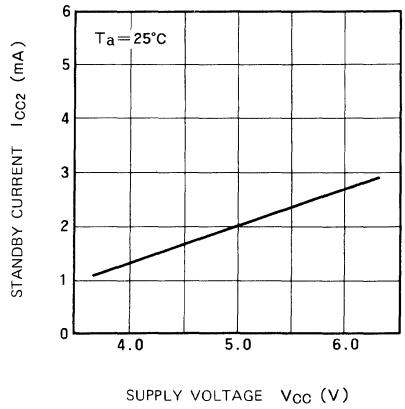
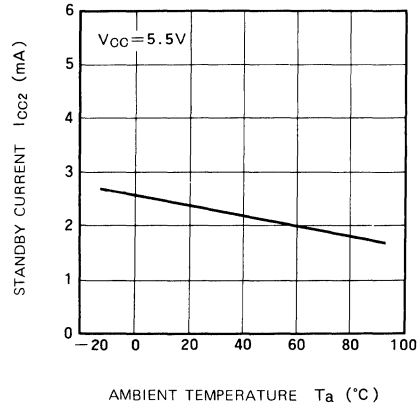
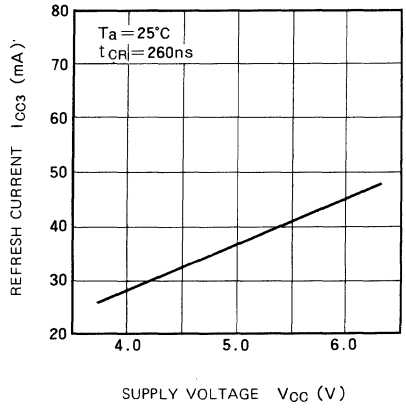
### STANDBY CURRENT VS. SUPPLY VOLTAGE



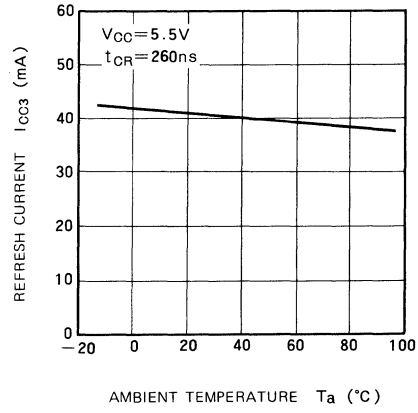

### STANDBY CURRENT VS. AMBIENT TEMPERATURE



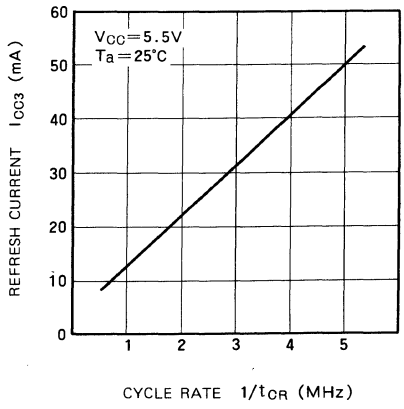

### REFRESH CURRENT VS. SUPPLY VOLTAGE



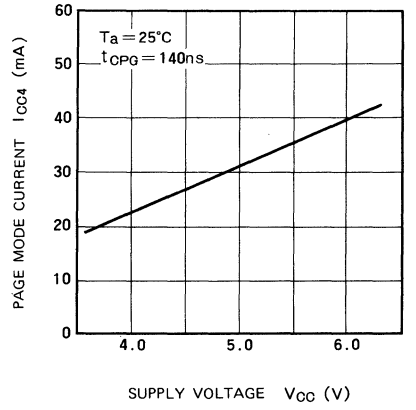

### REFRESH CURRENT VS. AMBIENT TEMPERATURE



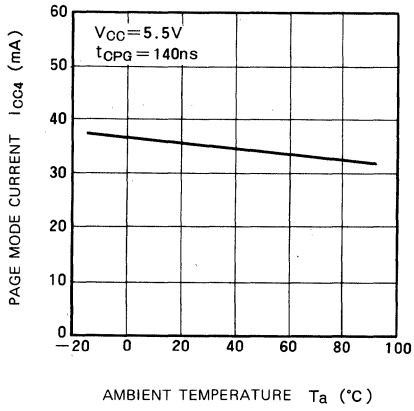

### REFRESH CURRENT VS. CYCLE RATE



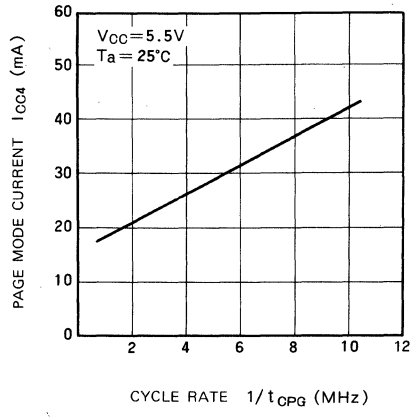

### PAGE MODE CURRENT VS. SUPPLY VOLTAGE



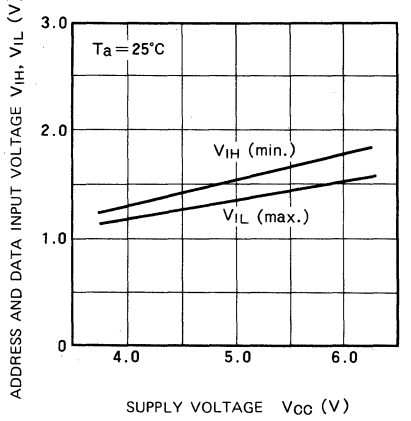
### PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



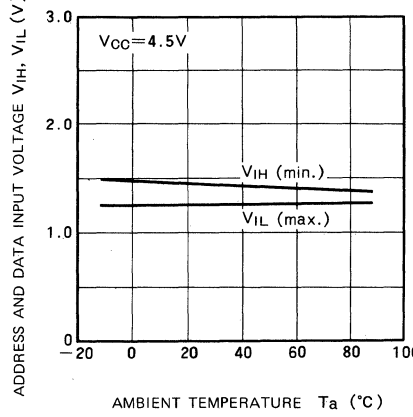

### PAGE MODE CURRENT VS. CYCLE RATE



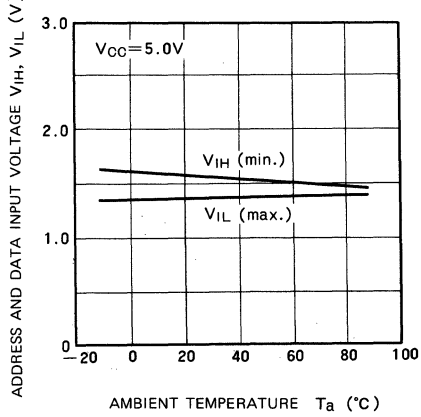

### ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



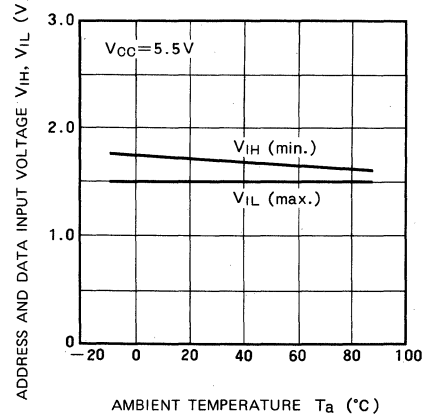

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



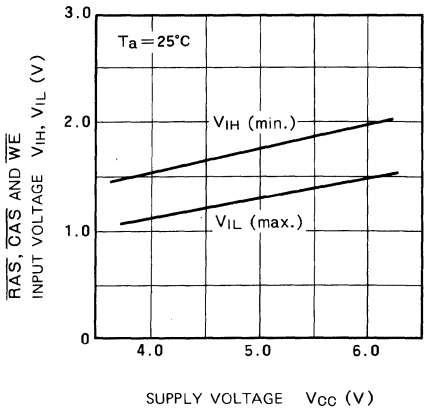

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



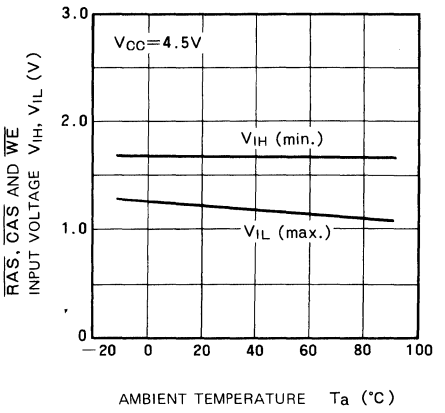

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



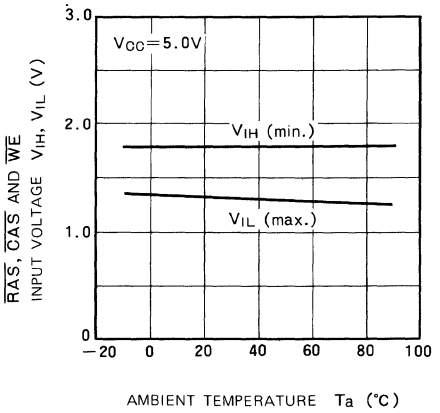
**$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE**



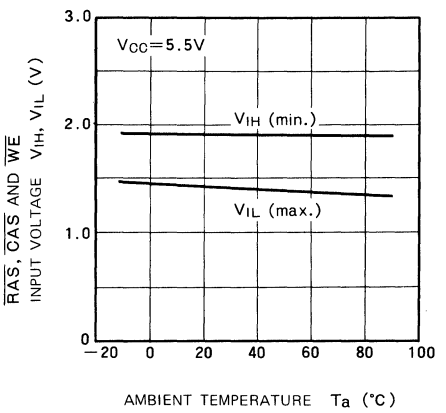

**$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE**



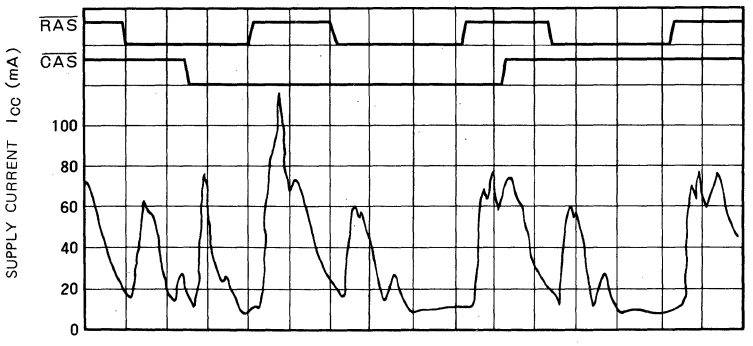

**$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE**




**$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE**

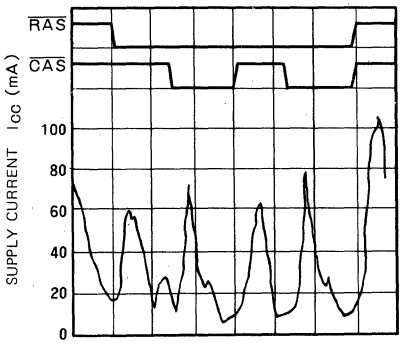


**RAS/CAS CYCLE** **HIDDEN REFRESH CYCLE** **RAS ONLY REFRESH CYCLE**



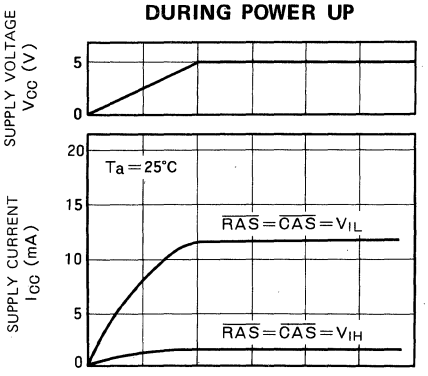

50ns/DIVISION

**PAGE MODE CYCLE**

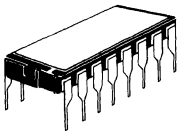



50ns/DIVISION

**CURRENT WAVEFORM DURING POWER UP**




50μs/DIVISION





# M5M4257S-12, -15, -20

## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM

## DESCRIPTION

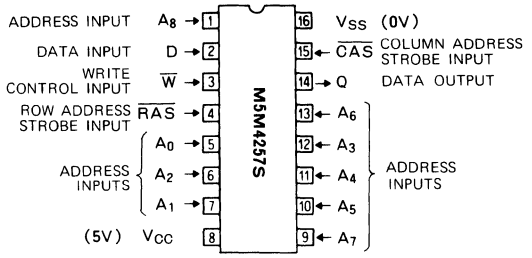
This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## FEATURES

| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4257S-12 | 120 | 230 | 260 |
| M5M4257S-15 | 150 | 260 | 230 |
| M5M4257S-20 | 200 | 330 | 190 |

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  - M5M4257S-12 . . . . . 413mW (max)
  - M5M4257S-15 . . . . . 385mW (max)
  - M5M4257S-20 . . . . . 303mW (max)
- Unlatched output enables two-dimensional chip selection

## PIN CONFIGURATION (TOP VIEW)



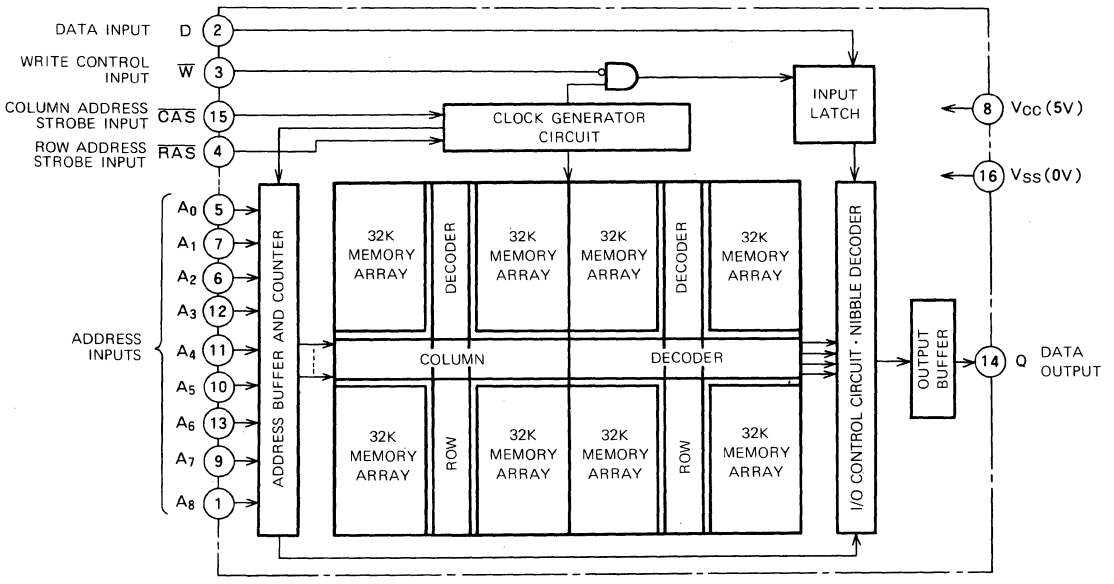

**Outline 16S1**

- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities. (Pin 1 is used for nibble mode)
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM



## FUNCTION

The M5M4257S provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Nibble mode identical except refresh is No, and Nibble mode column address is DNC While toggling $\overline{CAS}$.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4257S the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4257S is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257S, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Nibble-Mode Operation

The M5M4257S is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257S must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257S are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{suR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4257S is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4257S is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4257S as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4257S operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta=25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta=0～70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦$V_{CC}$, Other input pins =0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4257S-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$=$t_{CW}$= min, output open | | | 75 | mA |
| | | M5M4257S-15 | | | | 70 | mA |
| | | M5M4257S-20 | | | | 55 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$=$\overline{CAS}$=$V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4257S-12 | $\overline{RAS}$ cycling $\overline{CAS}$=$V_{IH}$ $t_{C(\overline{RAS})}$= min, output open | | | 60 | mA |
| | | M5M4257S-15 | | | | 55 | mA |
| | | M5M4257S-20 | | | | 45 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$ nibble mode | M5M4257S-12 | $\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ cycling $t_{CN}$= min, output open | | | 35 | mA |
| | | M5M4257S-15 | | | | 30 | mA |
| | | M5M4257S-20 | | | | 28 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4257S-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ = min, output open | | | 60 | mA |
| | | M5M4257S-15 | | | | 55 | mA |
| | | M5M4257S-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$=$V_{SS}$ f=1MHz $V_i$=25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$=$V_{SS}$, f=1MHz, $V_i$=25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for nibble-mode.
9: $t_{d(RAS-CAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)max}$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)max}$ defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2TTL, $C_L$ = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{cw}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |

## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Nibble-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CN}$ | Nibble mode cycle time | $t_{NC}$ | 55 | | 70 | | 90 | | ns |
| $t_{aN(CAS)}$ | Nibble mode access time | $t_{NAC}$ | | 30 | | 40 | | 50 | ns |
| $t_{wN(CASL)}$ | Nibble mode $\overline{CAS}$ low pulse width | $t_{NCAS}$ | 30 | | 40 | | 50 | | ns |
| $t_{wN(CASH)}$ | Nibble mode precharge time | $t_{NP}$ | 15 | | 20 | | 30 | | ns |
| $t_{hN(CAS-RAS)}$ | Nibble mode $\overline{RAS}$ hold time | $t_{NRSH}$ | 30 | | 40 | | 50 | | ns |
| $t_{dN(CAS-W)}$ | Nibble mode $\overline{CAS}$ to WRITE delay | $t_{NCWD}$ | 30 | | 40 | | 50 | | ns |
| $t_{wNRMW(CASL)}$ | Nibble mode RMW $\overline{CAS}$ pulse width | $t_{NCRW}$ | 65 | | 85 | | 105 | | ns |
| $t_{hNRMW(W-CAS)}$ | Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time | $t_{NCWL}$ | 30 | | 40 | | 50 | | ns |
| $t_{hNRMW(CAS-RAS)}$ | Nibble mode RMW $\overline{RAS}$ hold time | $t_{NWSH}$ | 65 | | 85 | | 105 | | ns |
| $t_{suN(W-CAS)}$ | Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$ | $t_{NWCS}$ | 0 | | 0 | | 0 | | ns |

## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257S-12 | | M5M4257S-15 | | M5M4257S-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

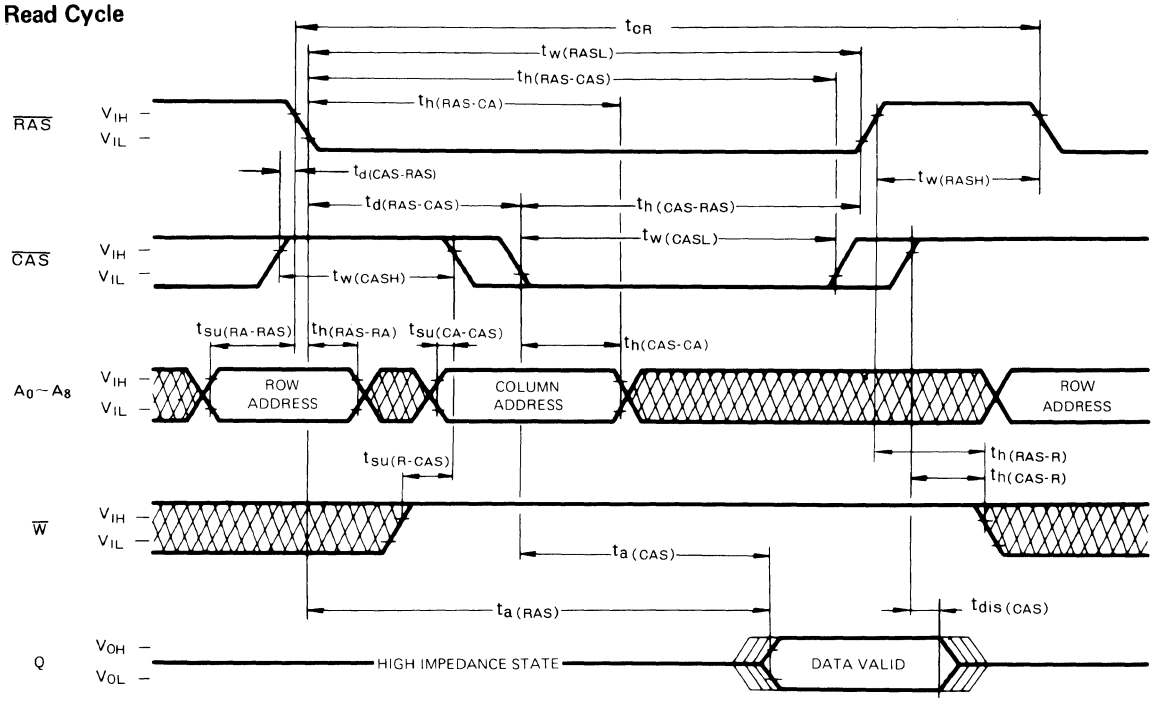
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## Nibble Mode Addressing Sequence Example

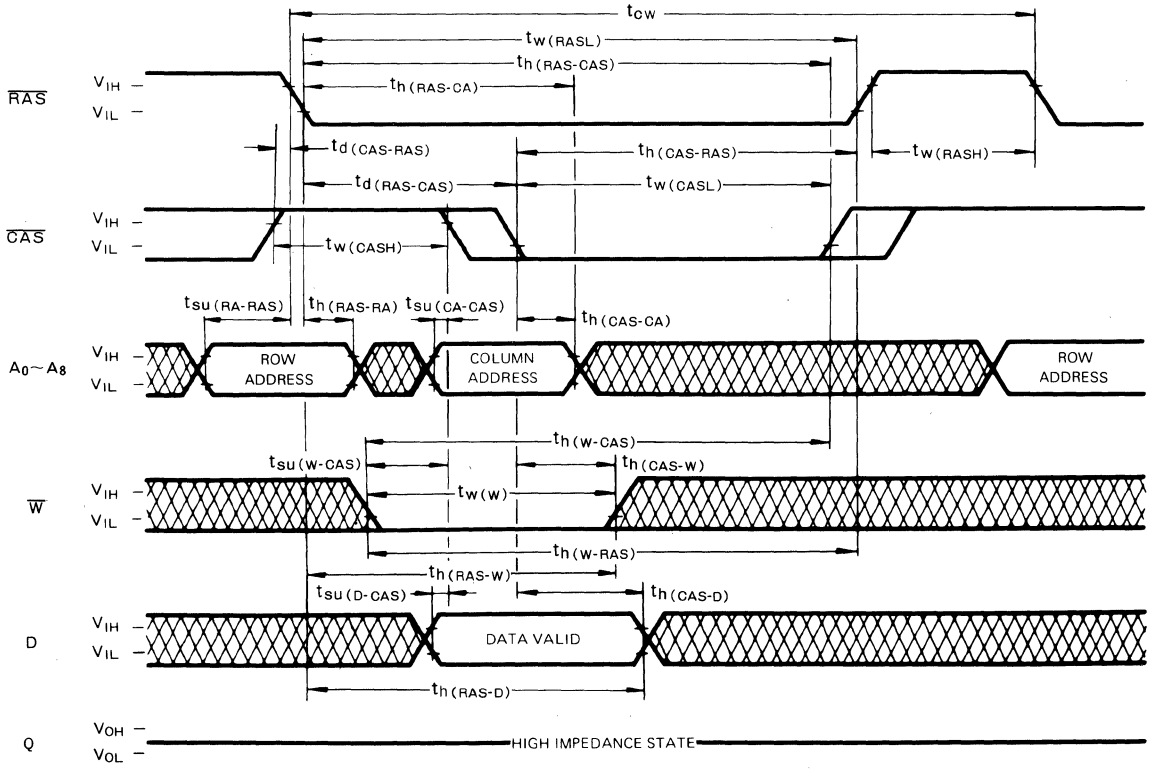
| Sequence | Nibble bit | Column address | | | | | | | | | Row address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | |
| $\overline{RAS}/\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | External address |
| toggle $\overline{CAS}$ | 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Internally generated address |
| toggle $\overline{CAS}$ | 3 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| toggle $\overline{CAS}$ | 4 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | |
| toggle $\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |

## TIMING DIAGRAMS (Note 19)

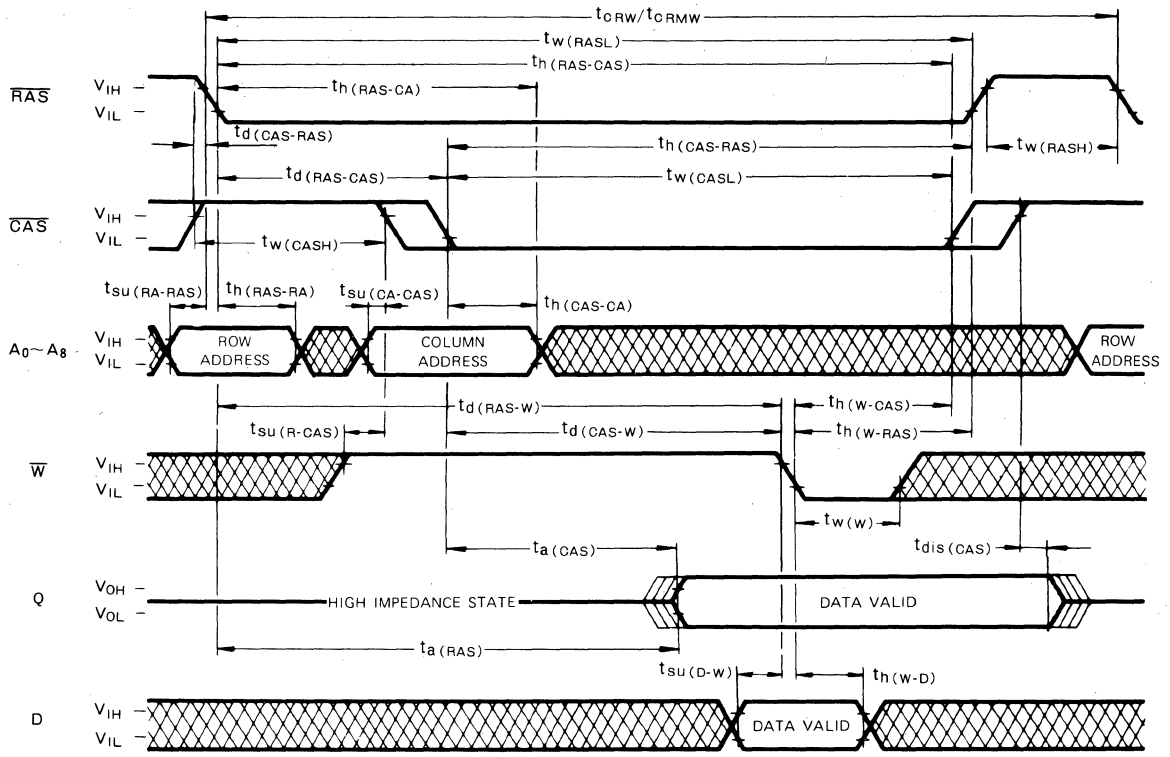
### Read Cycle



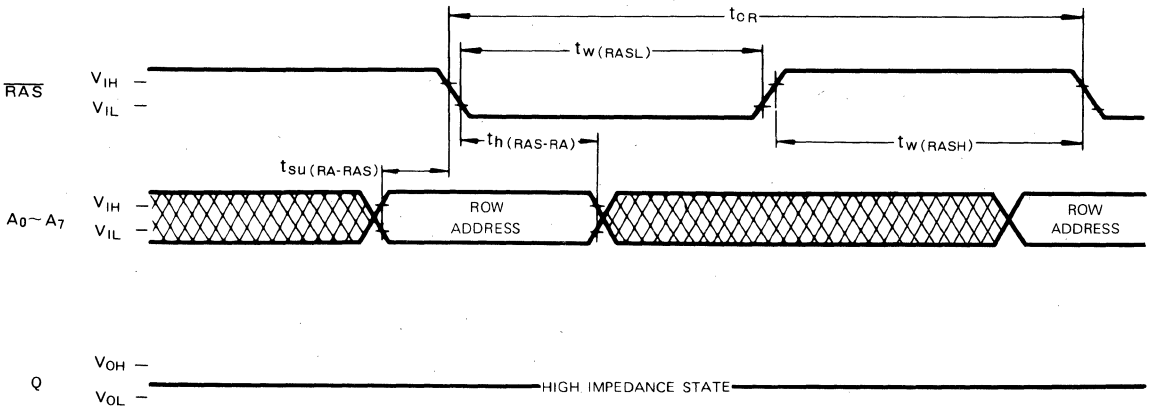

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 20)




Note 19. Indicates the don't care input

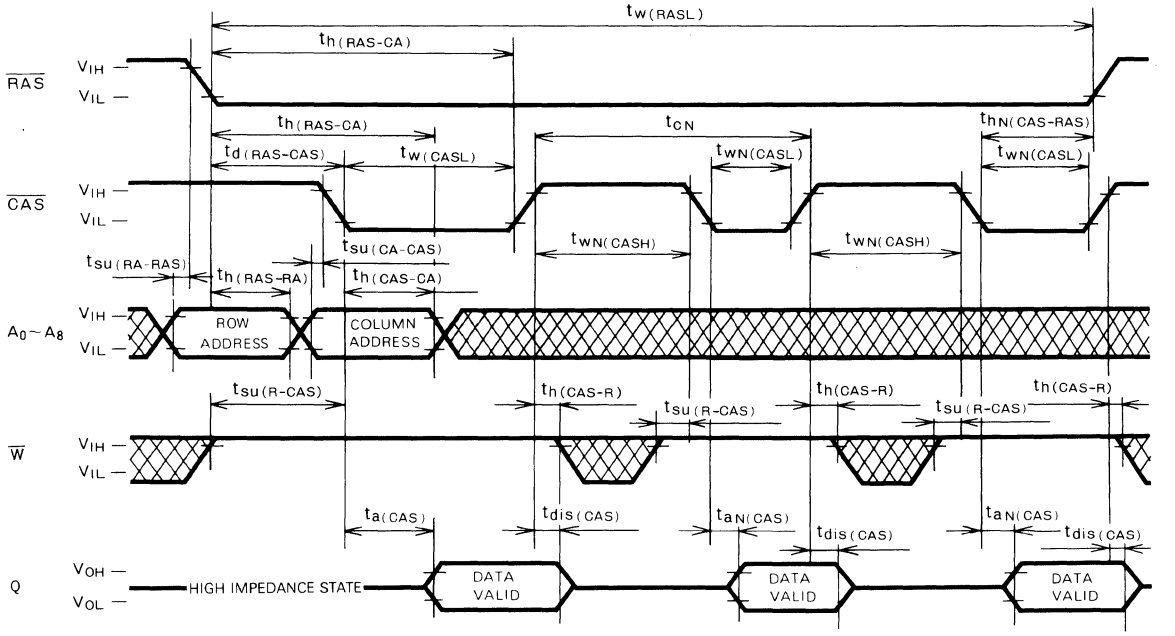
The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
$A_8$ may be $V_{IH}$ or $V_{IL}$.



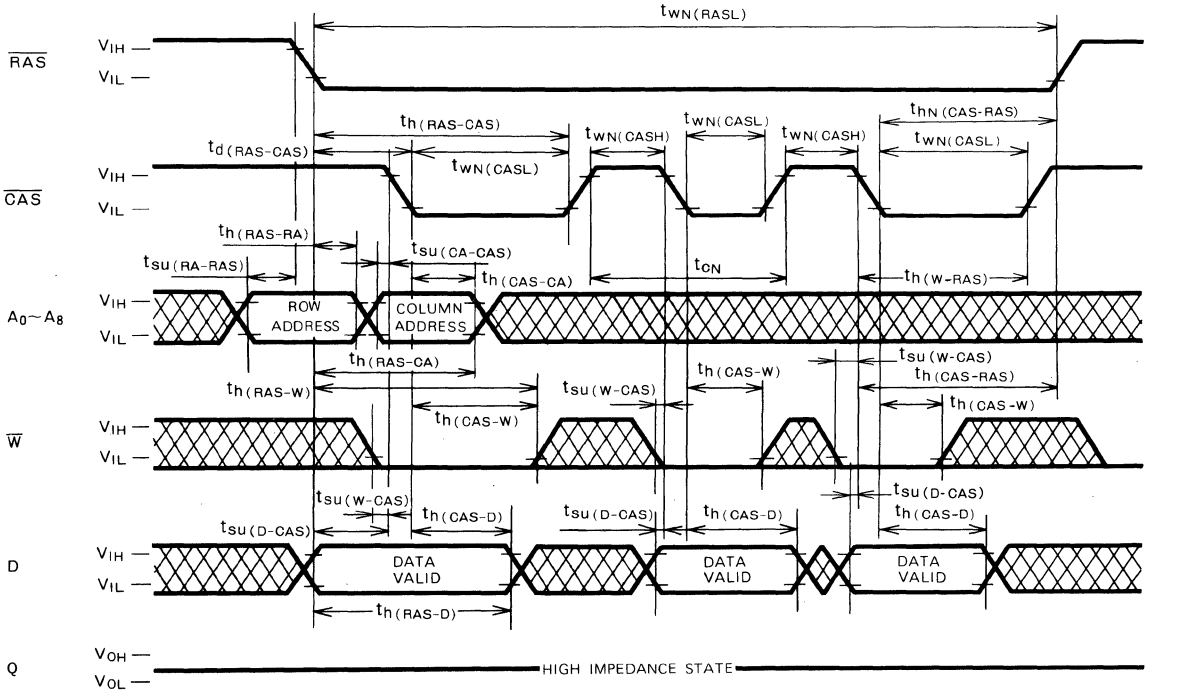
MITSUBISHI ELECTRIC

## Nibble Mode Read Cycle (Note 21)

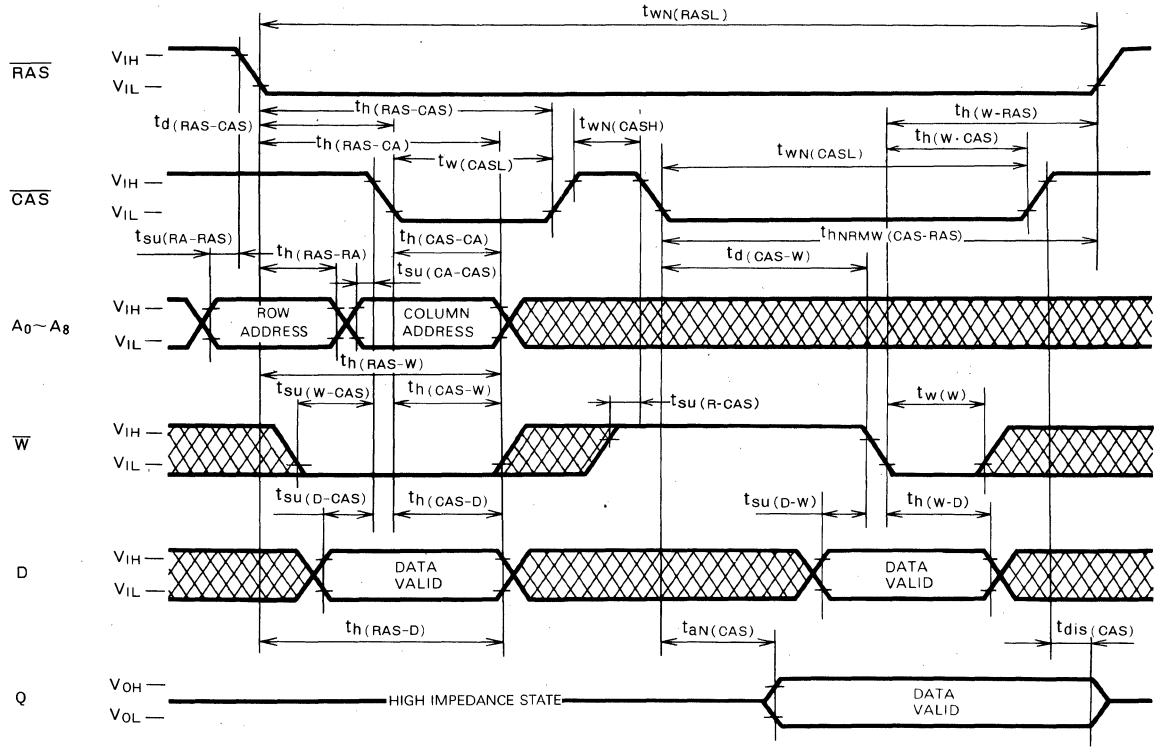



Note 21. Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

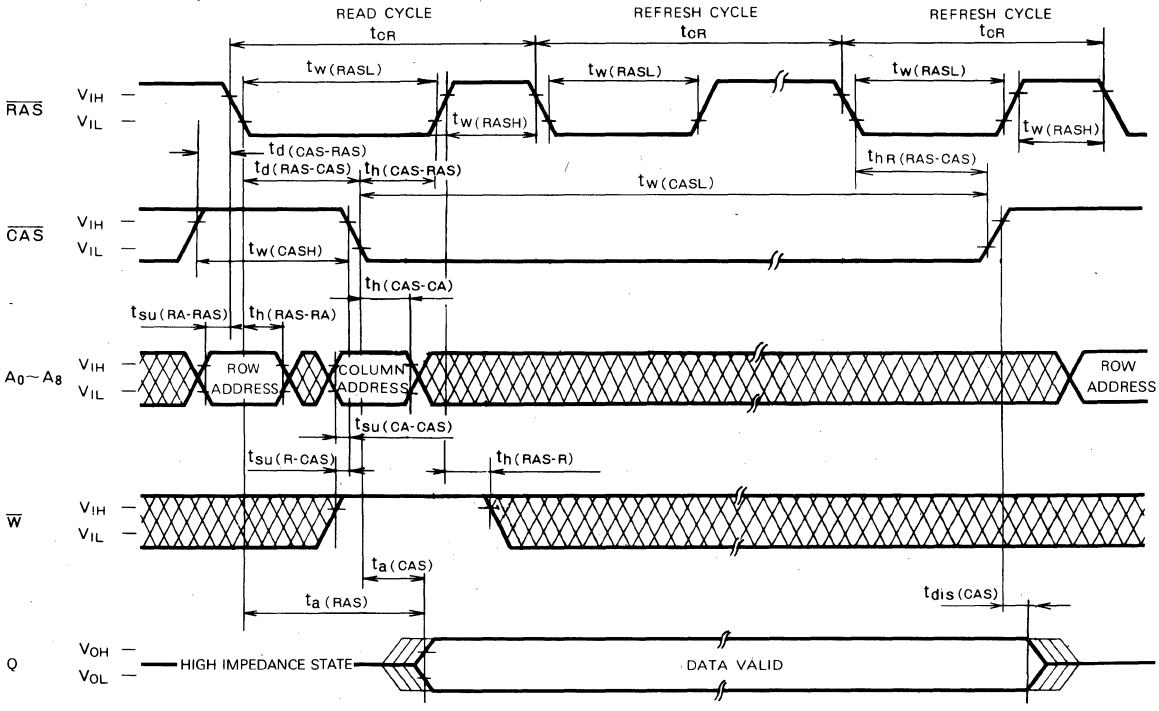
## Nibble Mode Write Cycle (Early Write)



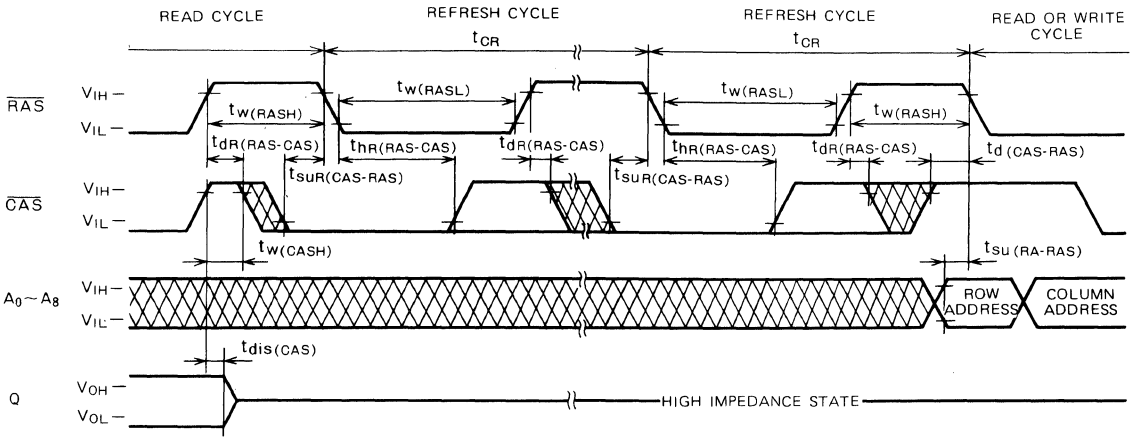
## Nibble Mode Read-Modify-Write




## Hidden Refresh Cycle



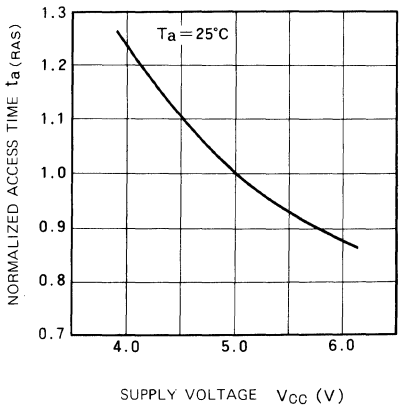
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)



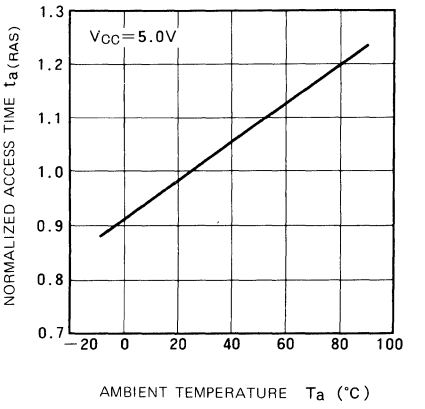

Note 22: $\overline{W}$, D = don't care.

## TYPICAL CHARACTERISTICS

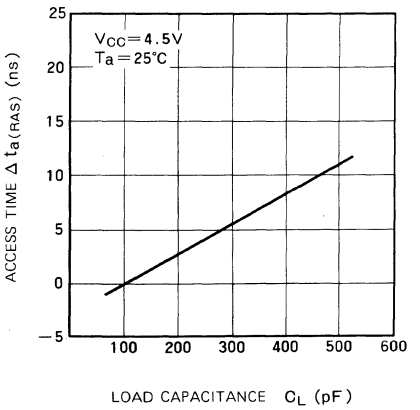
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



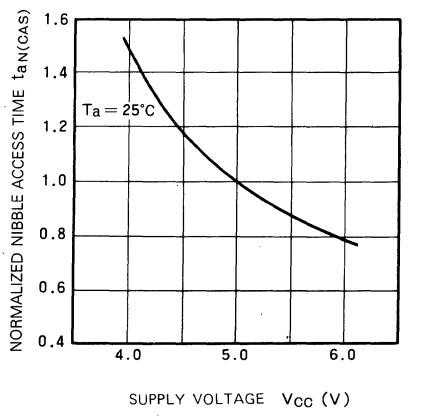

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



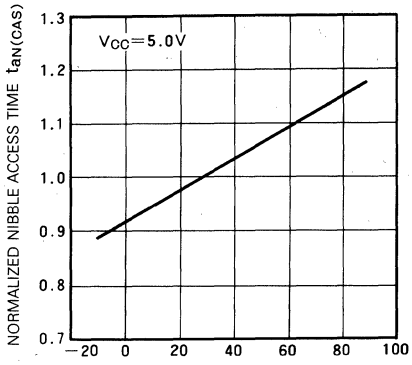

### ACCESS TIME VS. LOAD CAPACITANCE



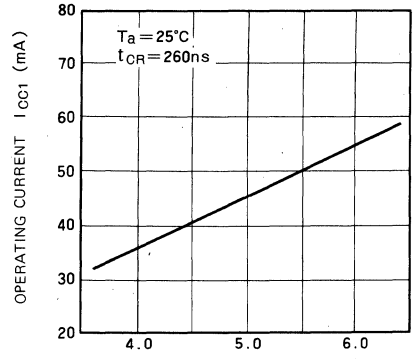

### NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE



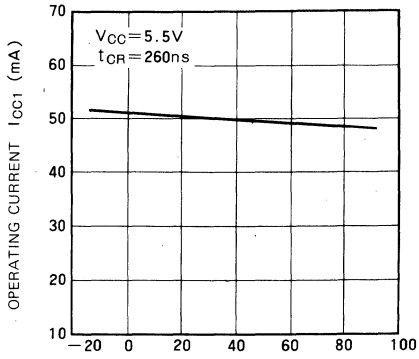
### NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



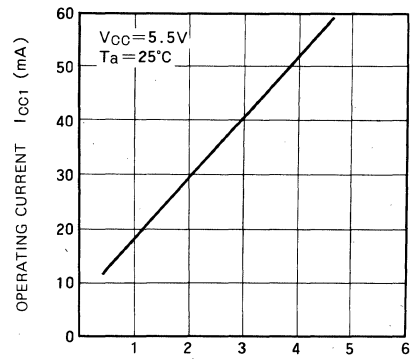

### OPERATING CURRENT VS. SUPPLY VOLTAGE



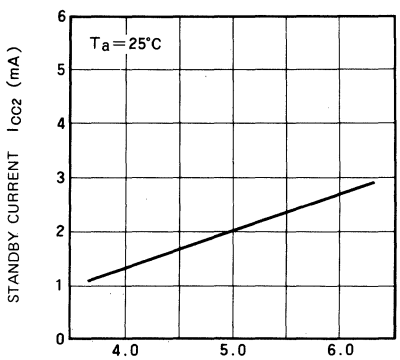

### OPERATING CURRENT VS. AMBIENT TEMPERATURE



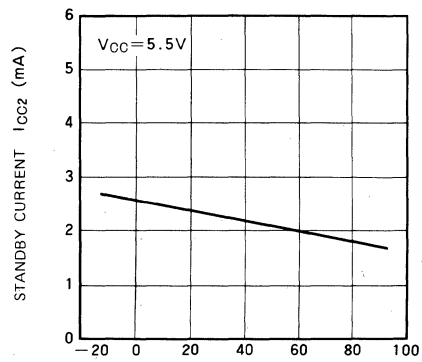

### OPERATING CURRENT VS. CYCLE RATE



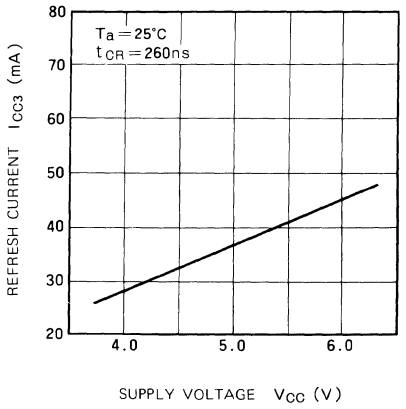

### STANDBY CURRENT VS. SUPPLY VOLTAGE



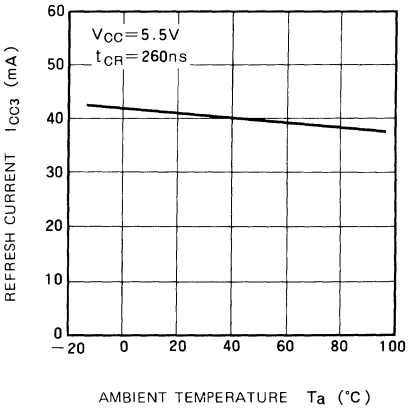

### STANDBY CURRENT VS. AMBIENT TEMPERATURE



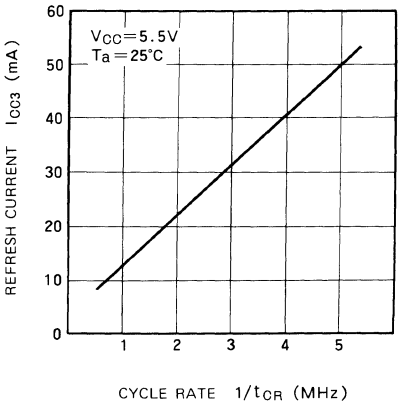
### REFRESH CURRENT VS. SUPPLY VOLTAGE



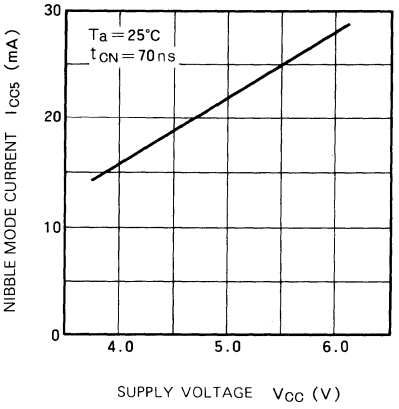

### REFRESH CURRENT VS. AMBIENT TEMPERATURE



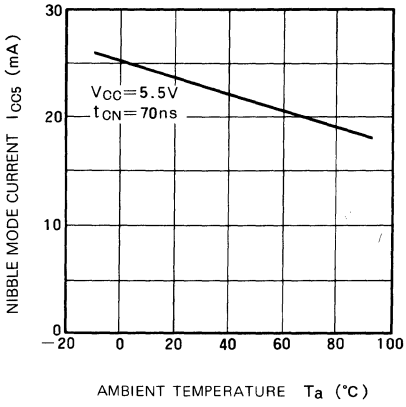

### REFRESH CURRENT VS. CYCLE RATE



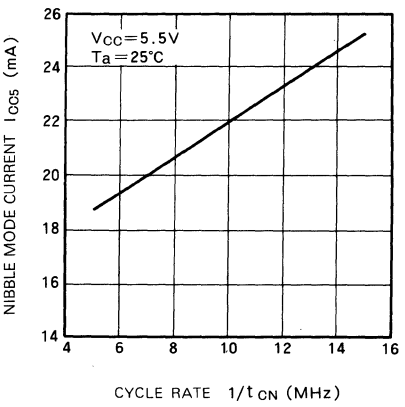

### NIBBLE MODE CURRENT VS. SUPPLY VOLTAGE



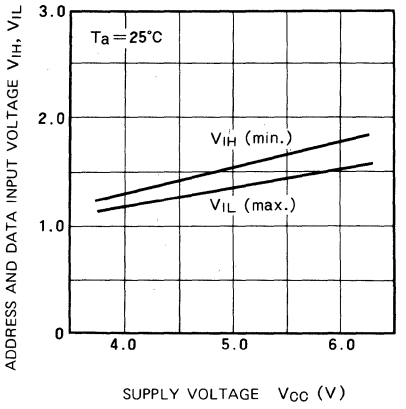

### NIBBLE MODE CURRENT VS. AMBIENT TEMPERATURE



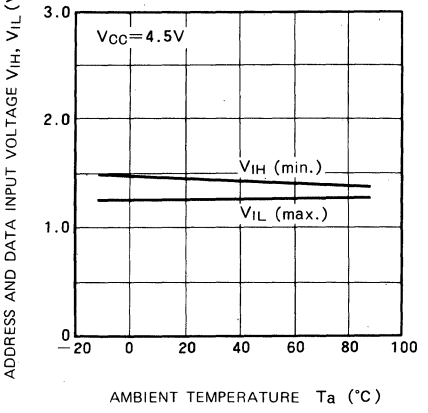

### NIBBLE MODE CURRENT VS. CYCLE RATE



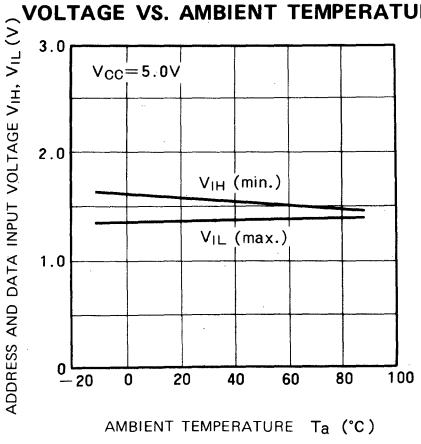
### ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



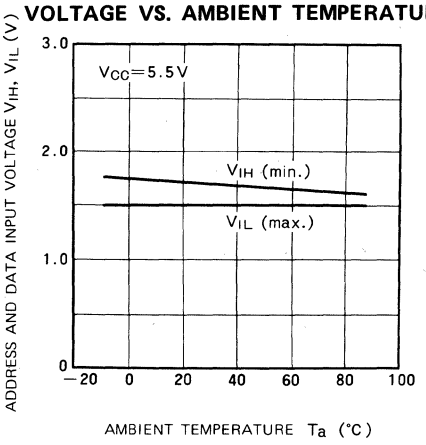

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



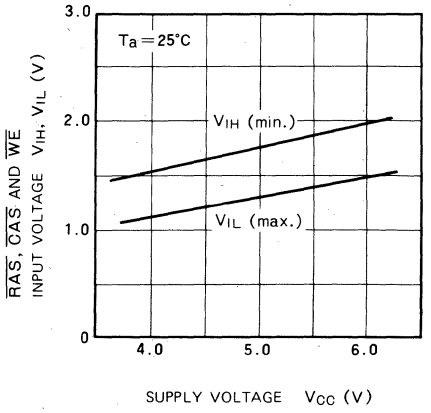

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



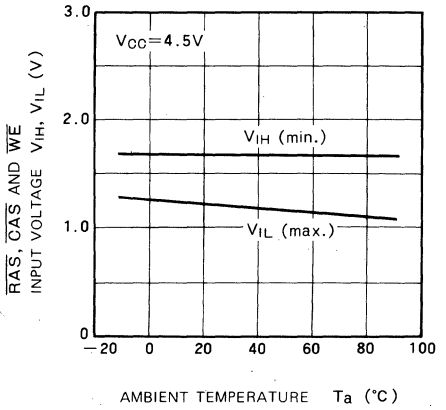

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



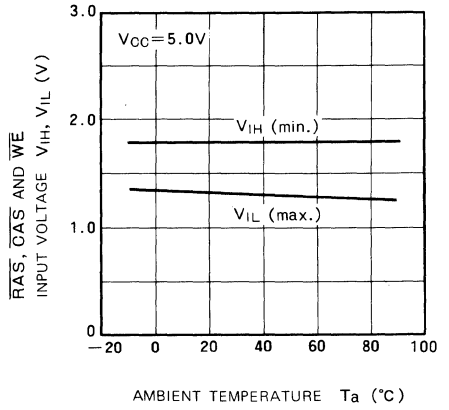

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



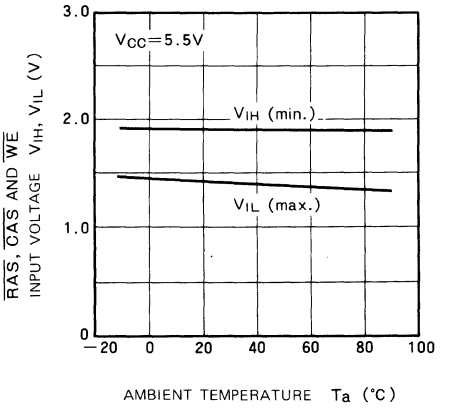

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



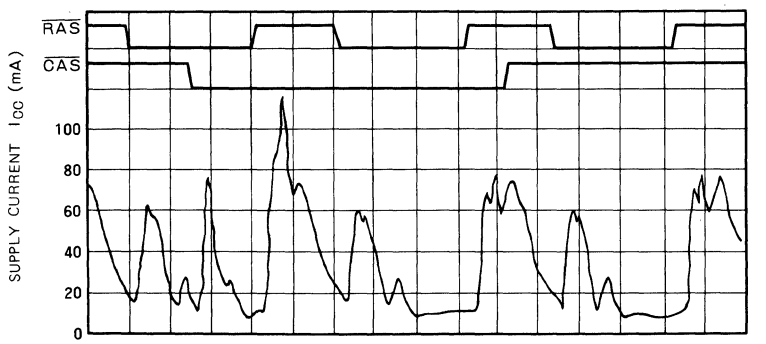
### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE




### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

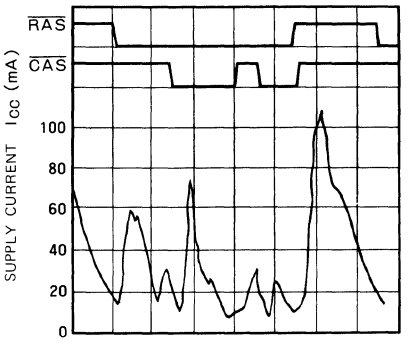



### $\overline{RAS}$/$\overline{CAS}$ CYCLE — HIDDEN REFRESH CYCLE — $\overline{RAS}$ ONLY REFRESH CYCLE



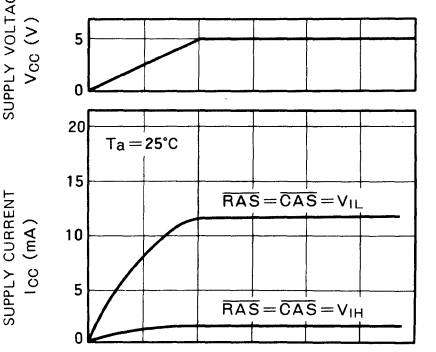

50ns/DIVISION

### NIBBLE MODE CYCLE




50ns/DIVISION

### CURRENT WAVEFORM DURING POWER UP




50μs/DIVISION

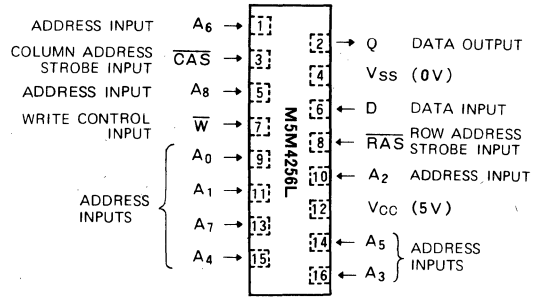
# M5M4256L-12, -15, -20

## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM


## DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16 pin zigzag inline package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## PIN CONFIGURATION (TOP VIEW)




**Outline 16P5A**

## FEATURES

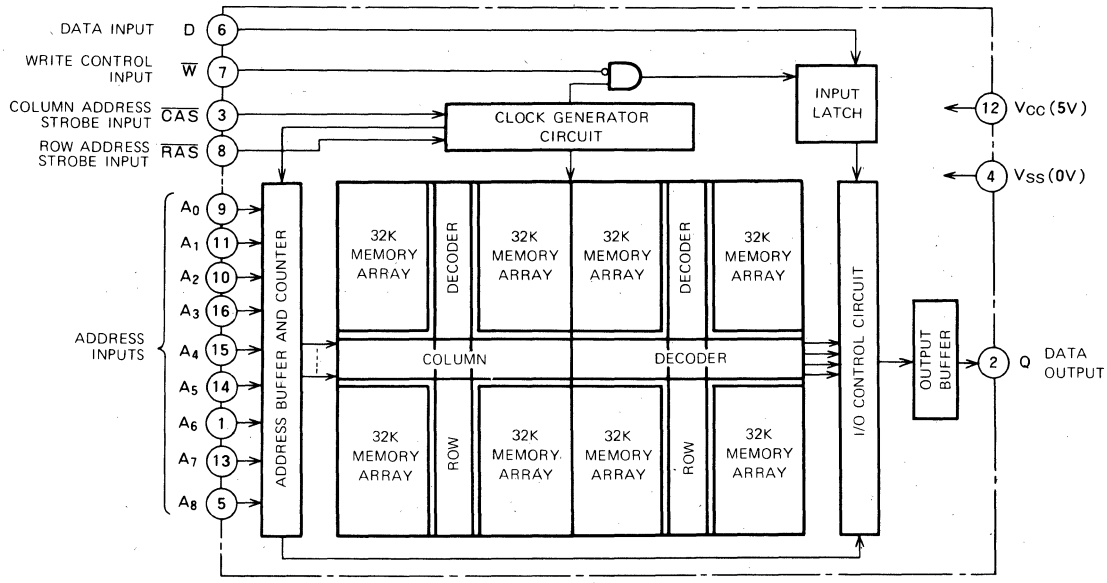
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4256L-12 | 120 | 230 | 260 |
| M5M4256L-15 | 150 | 260 | 230 |
| M5M4256L-20 | 200 | 330 | 190 |

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256L-12 . . . . . 360mW (max)
  - M5M4256L-15 . . . . . 330mW (max)
  - M5M4256L-20 . . . . . 275mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM



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## FUNCTION

The M5M4256L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
*: Page mode identical except refresh is No.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4256L the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4256L is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256L, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256L must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256L are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4256L is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4256L is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256L as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4256L operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1 ~ 7 | V |
| $V_I$ | Input voltage | | −1 ~ 7 | V |
| $V_O$ | Output voltage | | −1 ~ 7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta = 25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0 ~ 70 | °C |
| Tstg | Storage temperature range | | −65 ~ 150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V ≦ $V_{OUT}$ ≦ 5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V ≦ $V_{IN}$ ≦ $V_{CC}$, Other input pins = 0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4256L-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$ = $t_{CW}$ = min, output open | | | 65 | mA |
| | | M5M4256L-15 | | | | 60 | mA |
| | | M5M4256L-20 | | | | 50 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$ output open | | | 4.5 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4256L-12 | $\overline{RAS}$ cycling $\overline{CAS}$ = $V_{IH}$ $t_{C(RAS)}$ = min, output open | | | 55 | mA |
| | | M5M4256L-15 | | | | 50 | mA |
| | | M5M4256L-20 | | | | 40 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | M5M4256L-12 | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$ = min, output open | | | 50 | mA |
| | | M5M4256L-15 | | | | 45 | mA |
| | | M5M4256L-20 | | | | 40 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4256L-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, output open | | | 60 | mA |
| | | M5M4256L-15 | | | | 55 | mA |
| | | M5M4256L-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$ = $V_{SS}$ f = 1MHz Vi = 25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O$ = $V_{SS}$, f = 1MHz, $V_i$ = 25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive; out is negative.

3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2TTL, $C_L$ = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |



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## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15. $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CPG}$ | Page-mode cycle time | $t_{PC}$ | 125 | | 145 | | 190 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 55 | | 60 | | 80 | | ns |
| $t_{CPGRW}$ | Page-mode RMW cycle time | $t_{PCRW}$ | 160 | | 180 | | 230 | | ns |
| $t_{CPGRMW}$ | Page-mode RMW cycle time | $t_{PCRMW}$ | 170 | | 195 | | 250 | | ns |

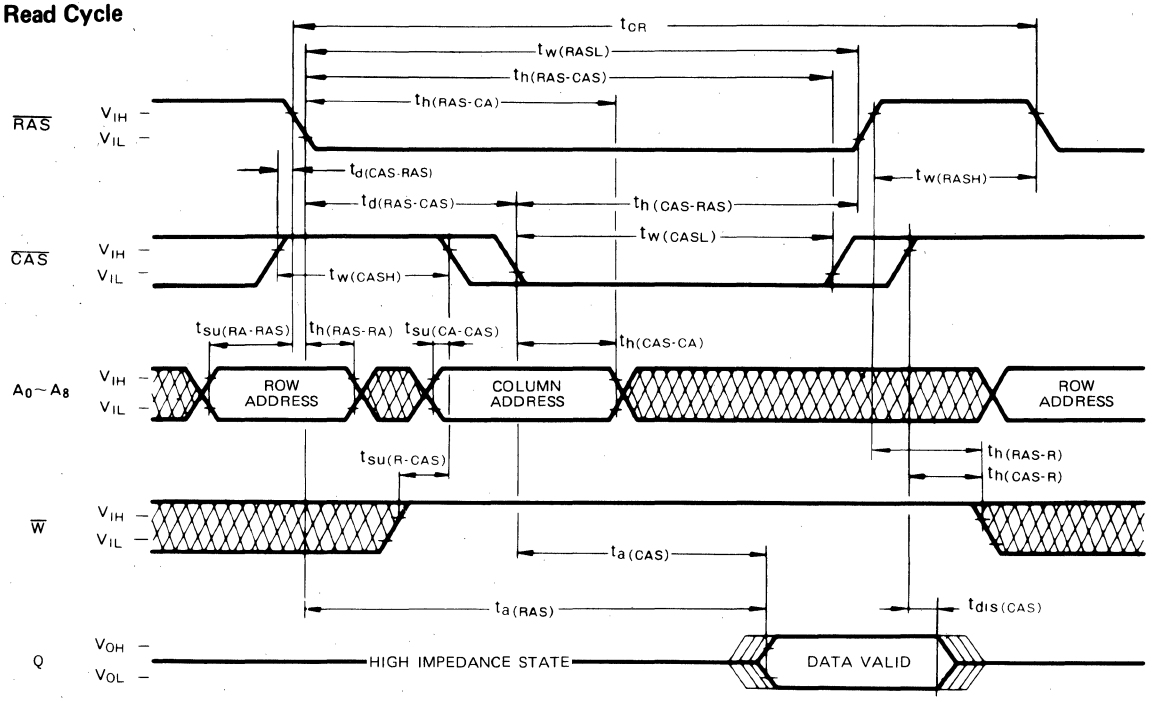
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4256L-12 | | M5M4256L-15 | | M5M4256L-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

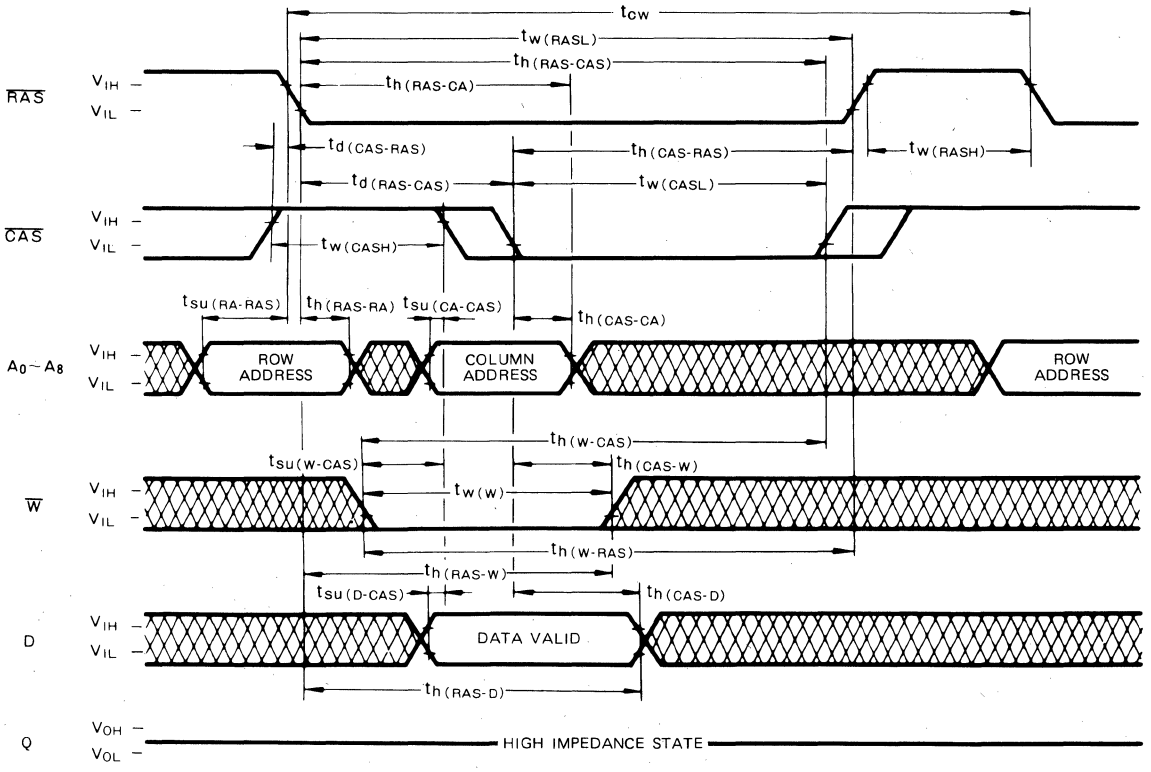
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## TIMING DIAGRAMS (Note 19)

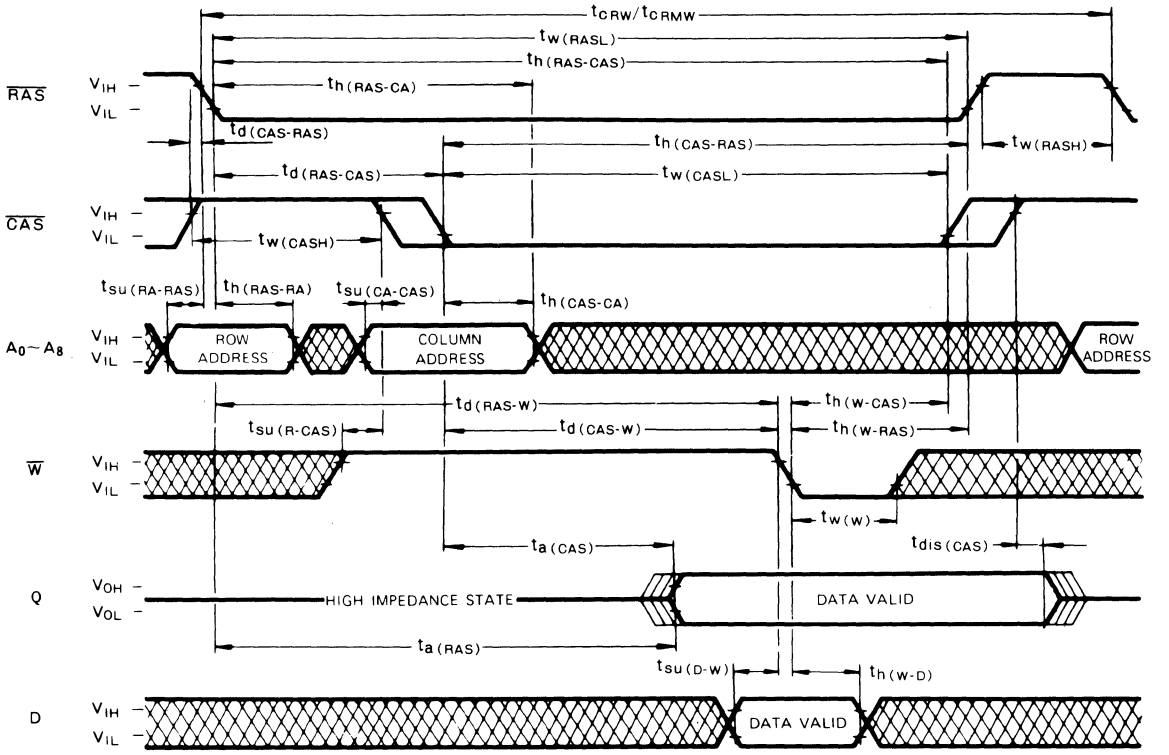
### Read Cycle



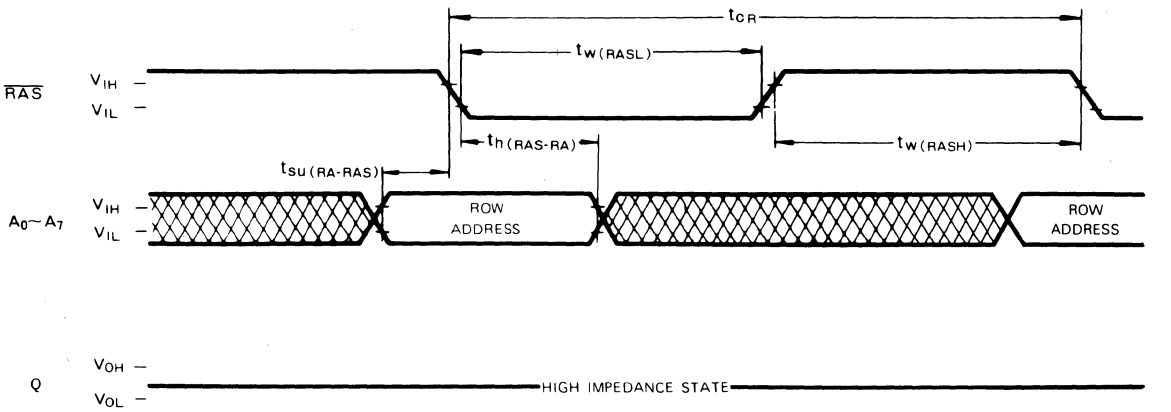

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 20)

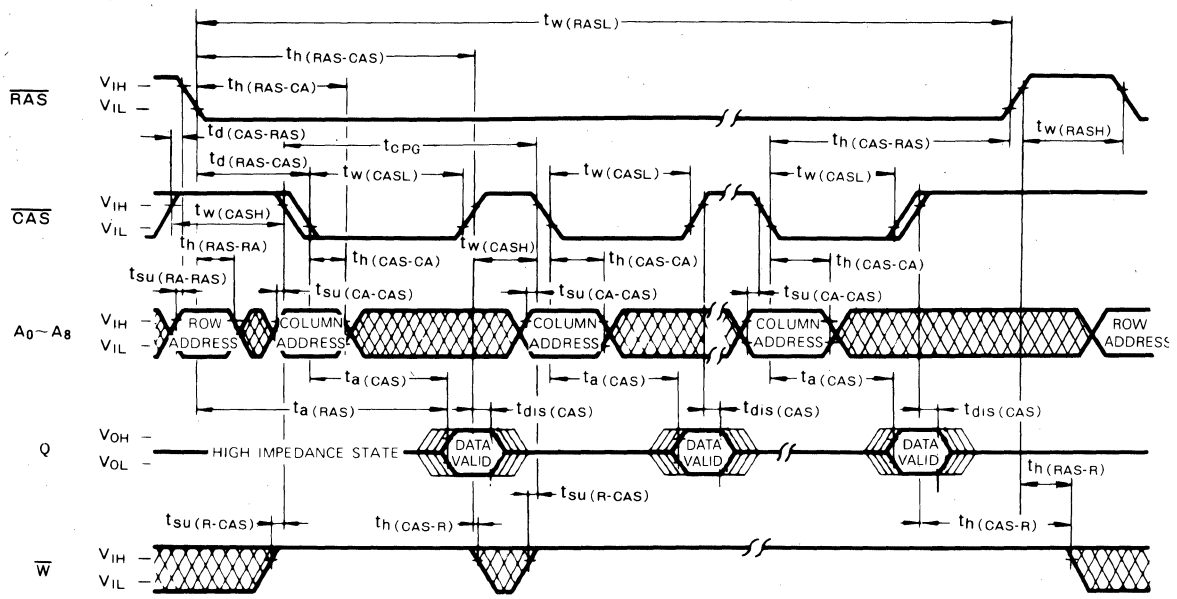



Note 19. Indicates the don't care input

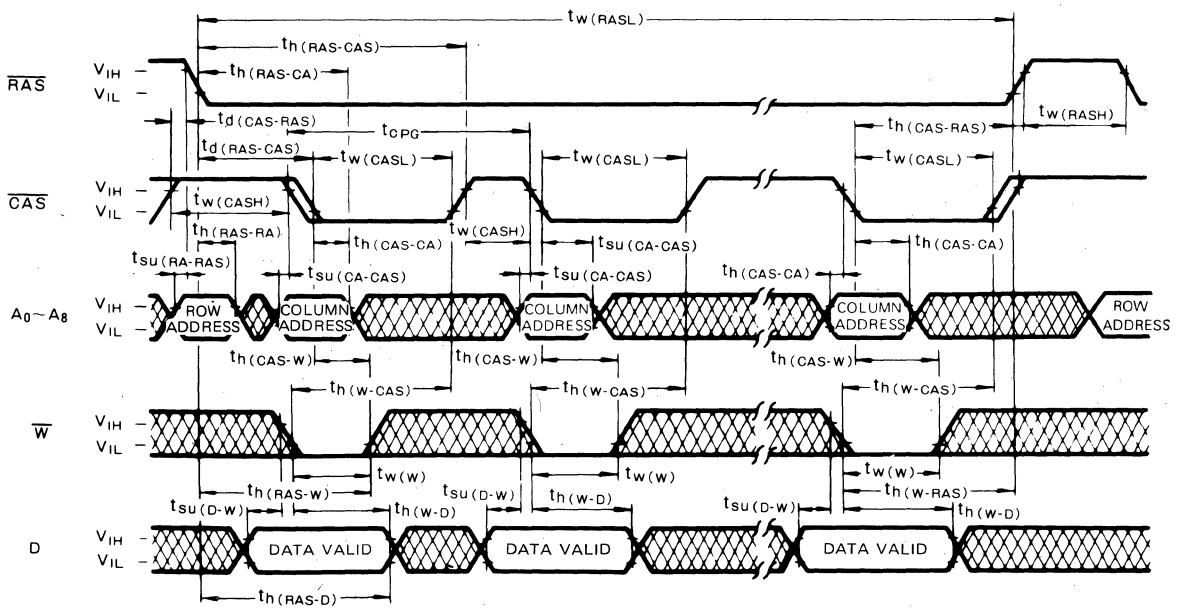
The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
$A_8$ may be $V_{IH}$ or $V_{IL}$.

## Page-Mode Read Cycle



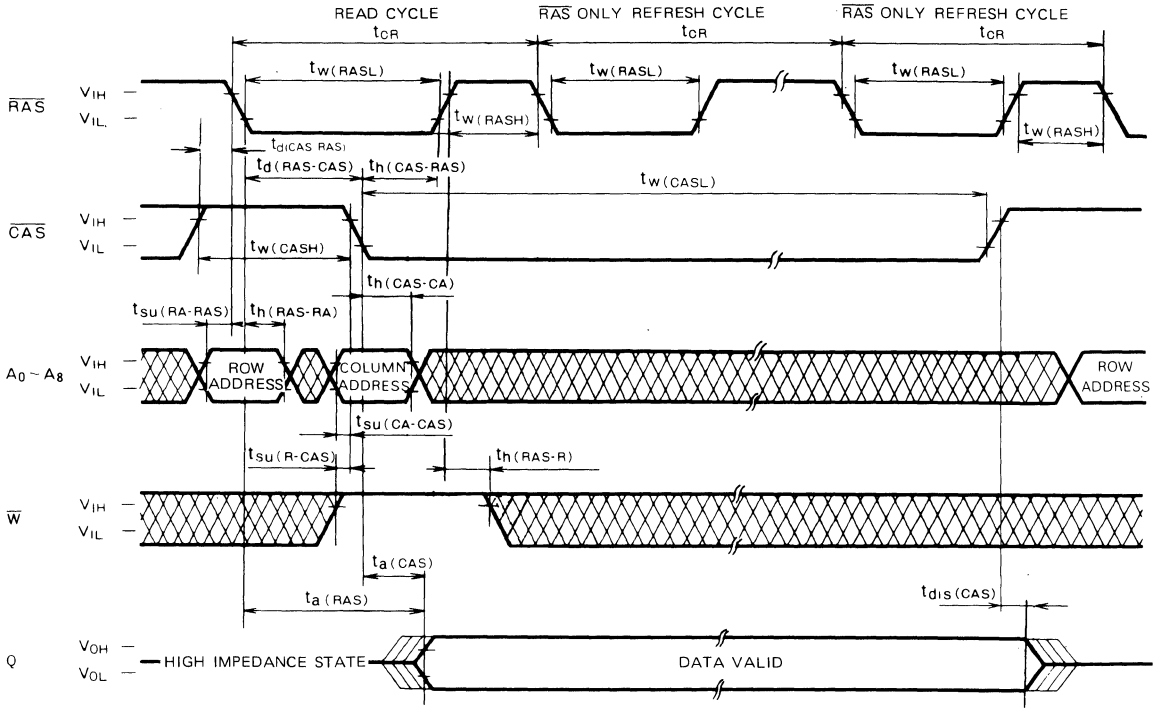

## Page-Mode Write Cycle



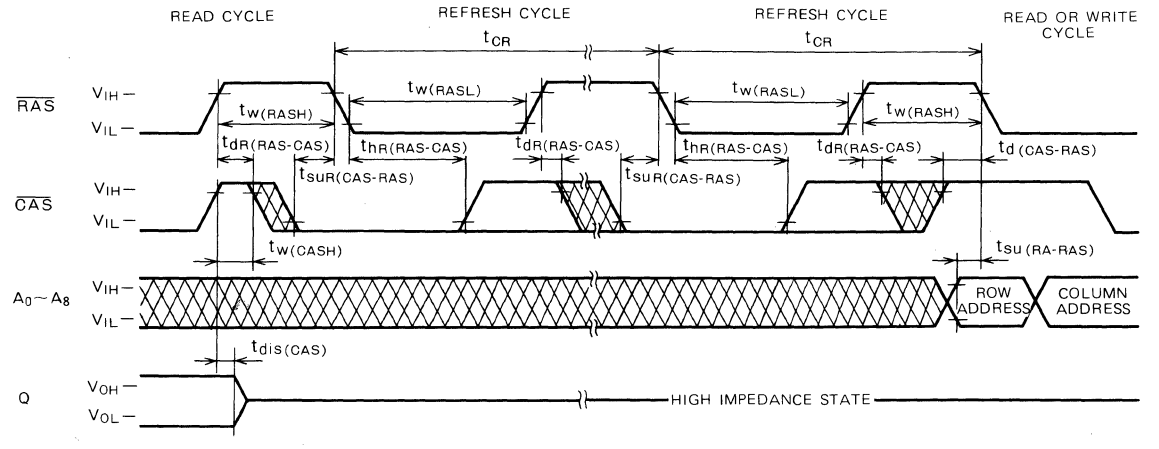



MITSUBISHI ELECTRIC

## Hidden Refresh Cycle



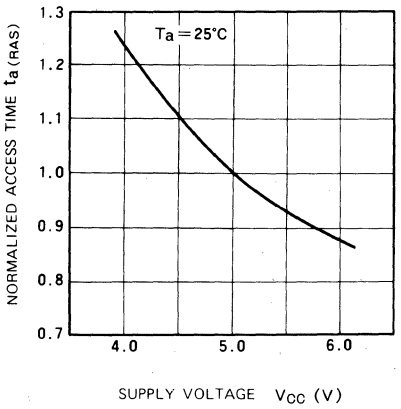

## CAS before RAS Refresh Cycle (Note 21)



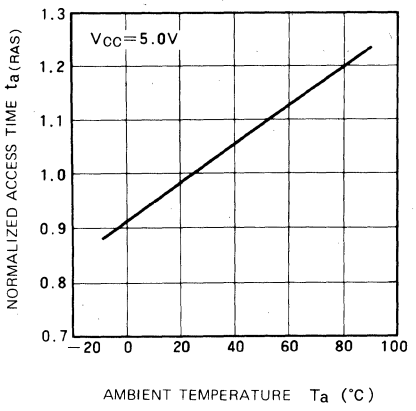

Note 21: W, D = don't care.

## TYPICAL CHARACTERISTICS

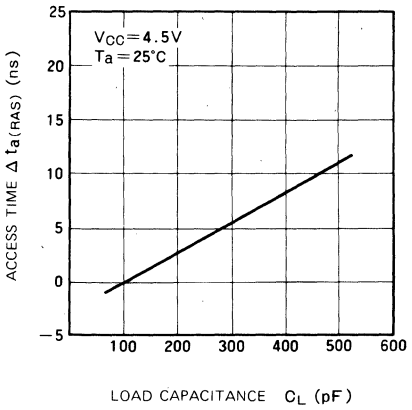
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



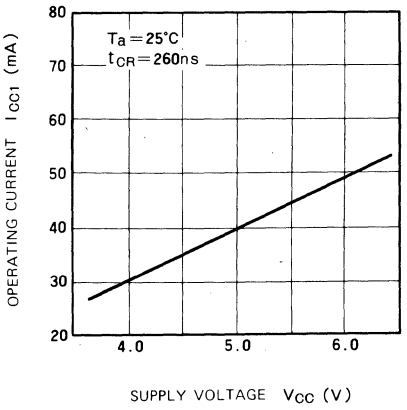

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



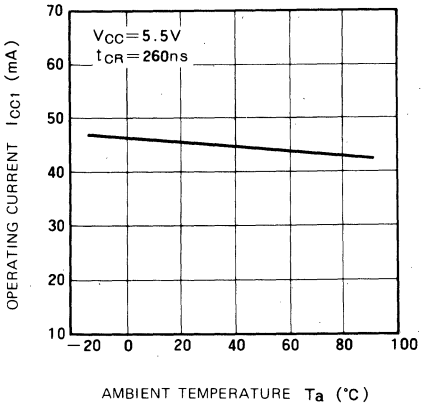

### ACCESS TIME VS. LOAD CAPACITANCE



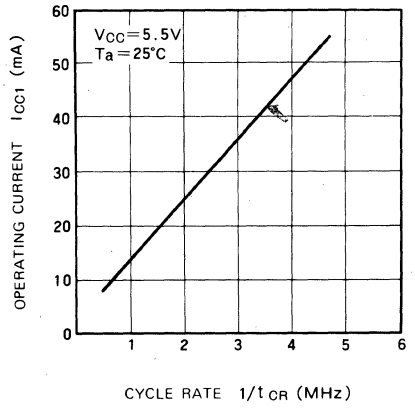

### OPERATING CURRENT VS. SUPPLY VOLTAGE



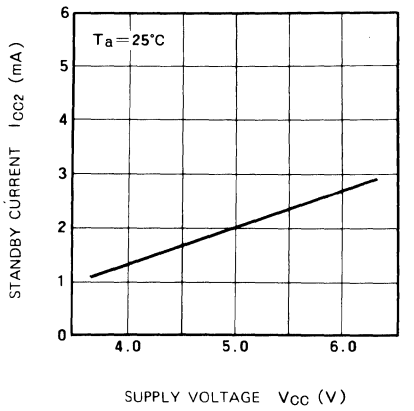

### OPERATING CURRENT VS. AMBIENT TEMPERATURE



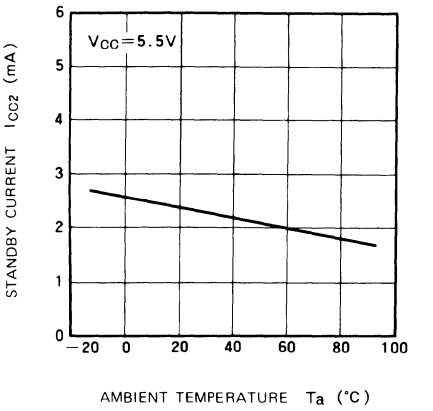

### OPERATING CURRENT VS. CYCLE RATE



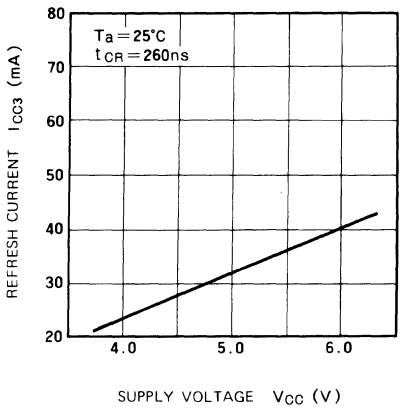
### STANDBY CURRENT VS. SUPPLY VOLTAGE



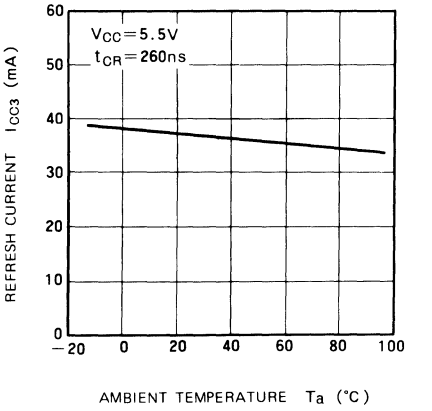

### STANDBY CURRENT VS. AMBIENT TEMPERATURE



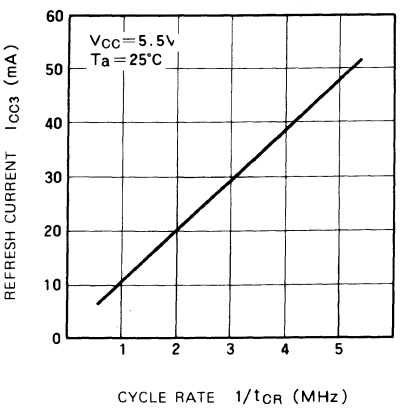

### REFRESH CURRENT VS. SUPPLY VOLTAGE



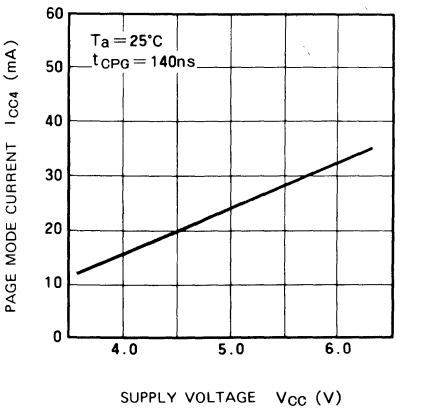

### REFRESH CURRENT VS. AMBIENT TEMPERATURE



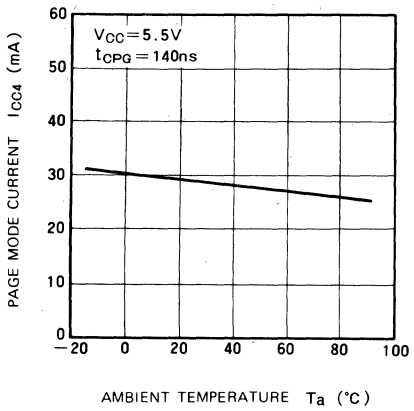

### REFRESH CURRENT VS. CYCLE RATE



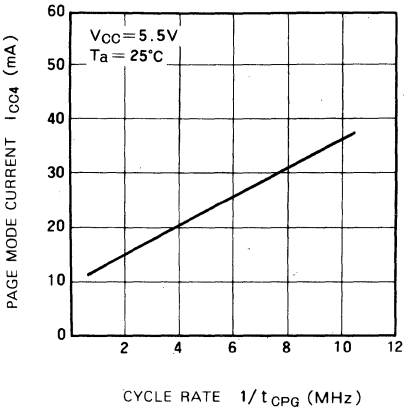

### PAGE MODE CURRENT VS. SUPPLY VOLTAGE



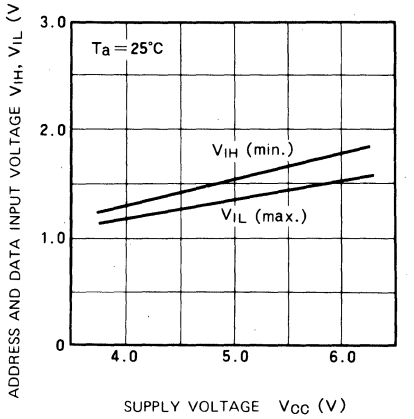
### PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



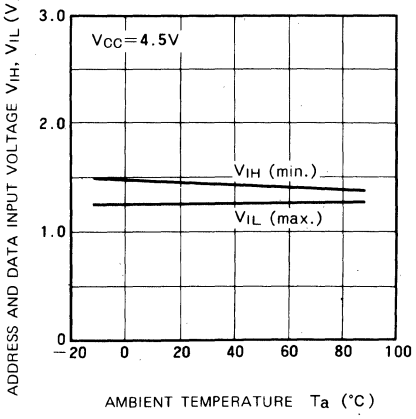

### PAGE MODE CURRENT VS. CYCLE RATE



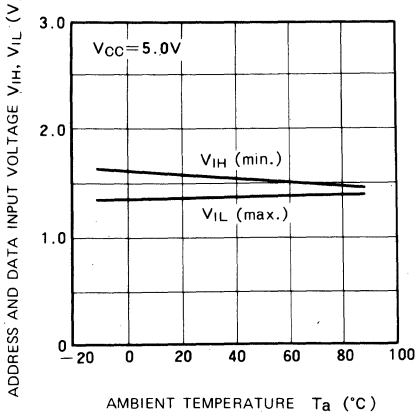

### ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



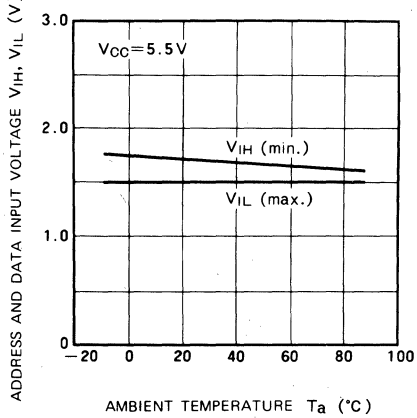

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



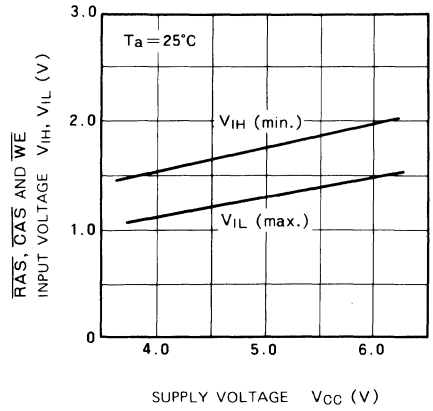

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



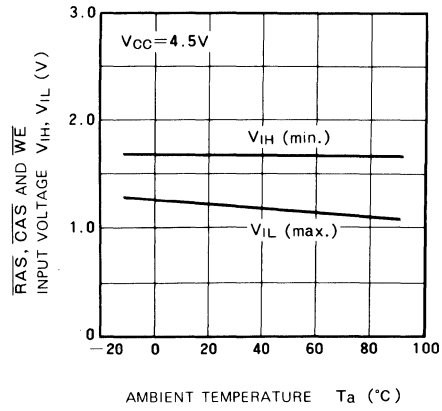

### ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



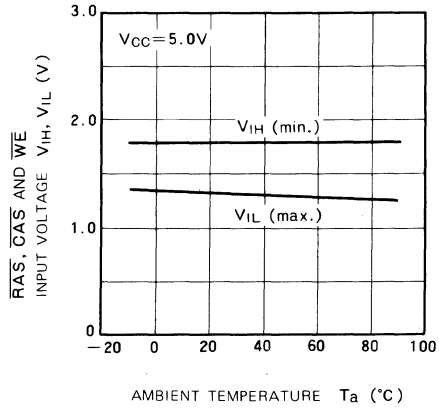
### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



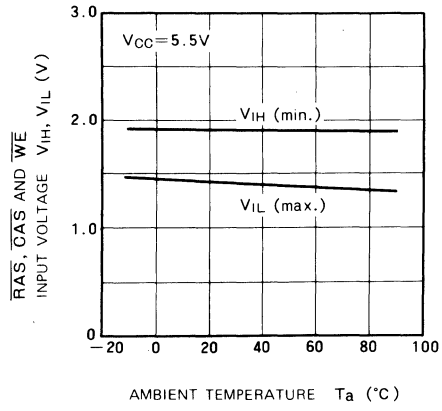

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



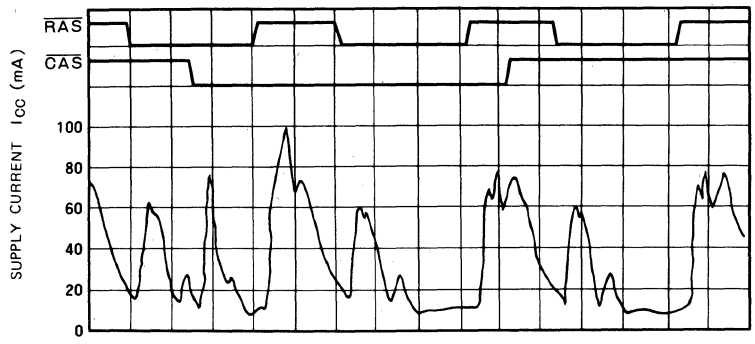

### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE




### $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

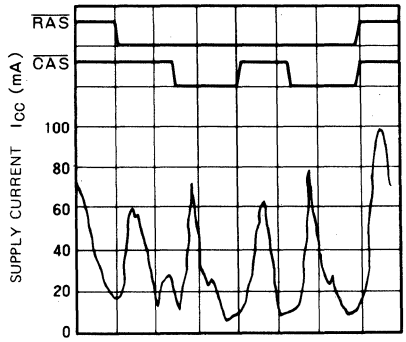


**RAS/CAS CYCLE** **HIDDEN REFRESH CYCLE** **RAS ONLY REFRESH CYCLE**



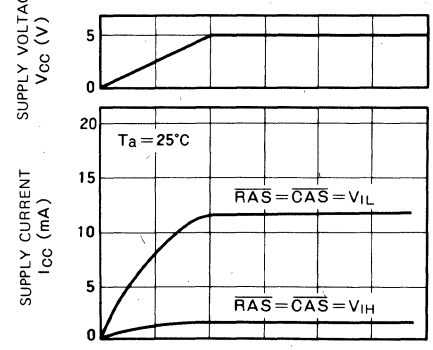

50ns/DIVISION

**PAGE MODE CYCLE**




50ns/DIVISION

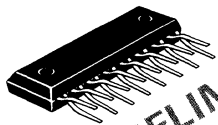
**CURRENT WAVEFORM DURING POWER UP**




50μs/DIVISION

# M5M4257L-12, -15, -20

## 262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM

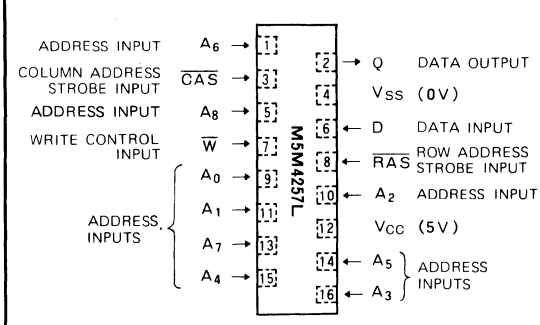


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

## DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16 pin zigzag inline package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

## PIN CONFIGURATION (TOP VIEW)




Outline 16P5A

## FEATURES

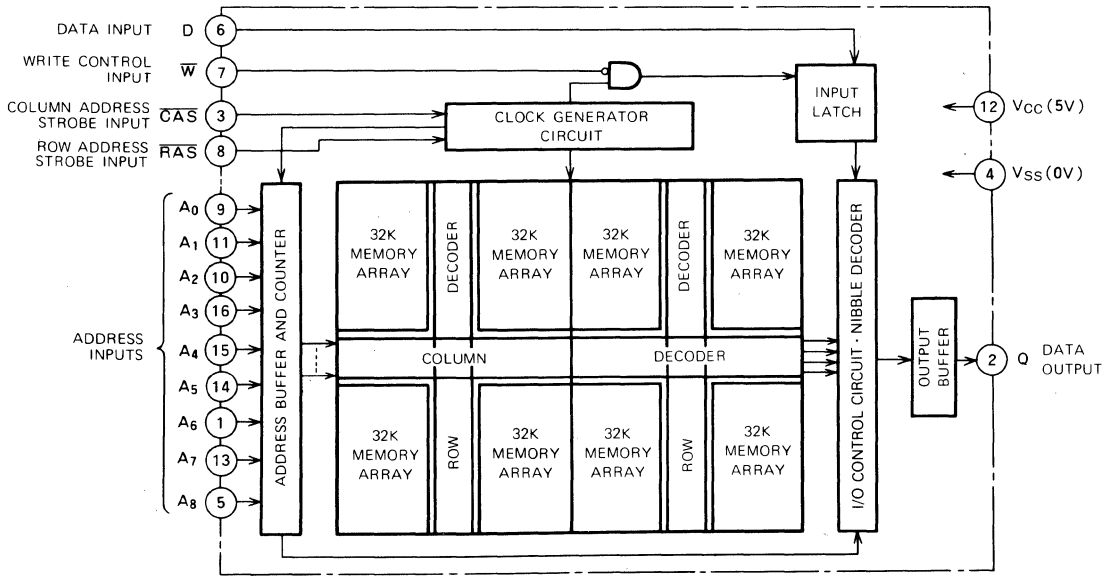
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4257L-12 | 120 | 230 | 260 |
| M5M4257L-15 | 150 | 260 | 230 |
| M5M4257L-20 | 200 | 330 | 190 |

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257L-12 . . . . . 360mW (max)
  - M5M4257L-15 . . . . . 330mW (max)
  - M5M4257L-20 . . . . . 275mW (max)
- Unlatched output enables two-dimensional chip selection
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities. (Pin 1 is used for nibble mode)
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

## APPLICATION

- Main memory unit for computers
- Microcomputer memory

## BLOCK DIAGRAM



## FUNCTION

The M5M4257L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | * |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | DNC | VLD | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
* : Nibble mode identical except refresh is No, and Nibble mode column address is DNC while togging $\overline{CAS}$.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262 144 memory cells in the M5M4257L the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

### Data Output Control

The output of the M5M4257L is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257L, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

**2 Data Output Hold**

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Nibble-Mode Operation

The M5M4257L is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257L must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257L are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{suR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4257L is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4257L is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4257L as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4257L operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1 ~ 7 | V |
| $V_I$ | Input voltage | | −1 ~ 7 | V |
| $V_O$ | Output voltage | | −1 ~ 7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta = 25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0 ~ 70 | °C |
| Tstg | Storage temperature range | | −65 ~ 150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1 All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V ≦ $V_{OUT}$ ≦ 5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V ≦ $V_{IN}$ ≦ $V_{CC}$, Other input pins = 0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | M5M4257L-12 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open | | | 65 | mA |
| | | M5M4257L-15 | | | | 60 | mA |
| | | M5M4257L-20 | | | | 50 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS} = \overline{CAS} = V_{IH}$ output open | | | 4.5 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | M5M4257L-12 | $\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(RAS)}$ = min, output open | | | 55 | mA |
| | | M5M4257L-15 | | | | 50 | mA |
| | | M5M4257L-20 | | | | 40 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$ nibble mode | M5M4257L-12 | $\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling $t_{CN}$ = min, output open | | | 30 | mA |
| | | M5M4257L-15 | | | | 25 | mA |
| | | M5M4257L-20 | | | | 23 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4257L-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, output open | | | 60 | mA |
| | | M5M4257L-15 | | | | 55 | mA |
| | | M5M4257L-20 | | | | 45 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I = V_{SS}$ f = 1MHz $V_i$ = 25mVrms | | | 5 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 5 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 10 | pF |
| $C_O$ | Output capacitance | | $V_O = V_{SS}$, f = 1MHz, $V_i$ = 25mVrms | | | 7 | pF |

Note 2: Current flowing into an IC is positive, out is negative.

3 $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4 $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | | 4 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | 100 | | 120 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | 100 | | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 120 | | 150 | | 200 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 60 | | 75 | | 100 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | 30 | | 30 | | 40 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 25 | 60 | 25 | 75 | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | −5 | | −5 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 15 | | 20 | | 25 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 80 | | 100 | | 135 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 5 An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6 The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7 Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8 Except for nibble-mode.
9 $t_{d(RAS-CAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10 Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only, if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(tTLH)} + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | 20 | | 25 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 11 Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12 $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
13 This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max. Test conditions ; Load = 2TTL, $C_L$ = 100pF
14 This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{cw}$ | Write cycle time | | $t_{RC}$ | 230 | | 260 | | 330 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | −10 | | −10 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 100 | | 120 | | 155 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 30 | | 35 | | 40 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 90 | | 110 | | 140 | | ns |

## Read, Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 260 | | 295 | | 370 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 275 | | 310 | | 390 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 40 | | 45 | | 55 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | 55 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 110 | | 135 | | 180 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 50 | | 60 | | 80 | | ns |
| $t_{su(D-W)}$ | Data-in set-up time before write | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 40 | | 45 | | 55 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 60 | | 75 | | 100 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 120 | | 150 | | 200 | ns |

Note 15 $t_{CRW}$ min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16 $t_{CRMW}$ min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17 $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}min$ and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Nibble-Mode Cycle

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CN}$ | Nibble mode cycle time | $t_{NC}$ | 55 | | 70 | | 90 | | ns |
| $t_{aN(CAS)}$ | Nibble mode access time | $t_{NAC}$ | | 30 | | 40 | | 50 | ns |
| $t_{WN(CASL)}$ | Nibble mode $\overline{CAS}$ low pulse width | $t_{NCAS}$ | 30 | | 40 | | 50 | | ns |
| $t_{WN(CASH)}$ | Nibble mode precharge time | $t_{NP}$ | 15 | | 20 | | 30 | | ns |
| $t_{hN(CAS-RAS)}$ | Nibble mode $\overline{RAS}$ hold time | $t_{NRSH}$ | 30 | | 40 | | 50 | | ns |
| $t_{dN(CAS-W)}$ | Nibble mode $\overline{CAS}$ to WRITE delay | $t_{NCWD}$ | 30 | | 40 | | 50 | | ns |
| $t_{WNRMW(CASL)}$ | Nibble mode RMW $\overline{CAS}$ pulse width | $t_{NCRW}$ | 65 | | 85 | | 105 | | ns |
| $t_{hNRMW(W-CAS)}$ | Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time | $t_{NCWL}$ | 30 | | 40 | | 50 | | ns |
| $t_{suN(W-CAS)}$ | Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$ | $t_{NWCS}$ | 0 | | 0 | | 0 | | ns |

## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M4257L-12 | | M5M4257L-15 | | M5M4257L-20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{suR(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 30 | | 30 | | 40 | | ns |
| $t_{hR(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 50 | | 50 | | 50 | | ns |
| $t_{dR(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns |

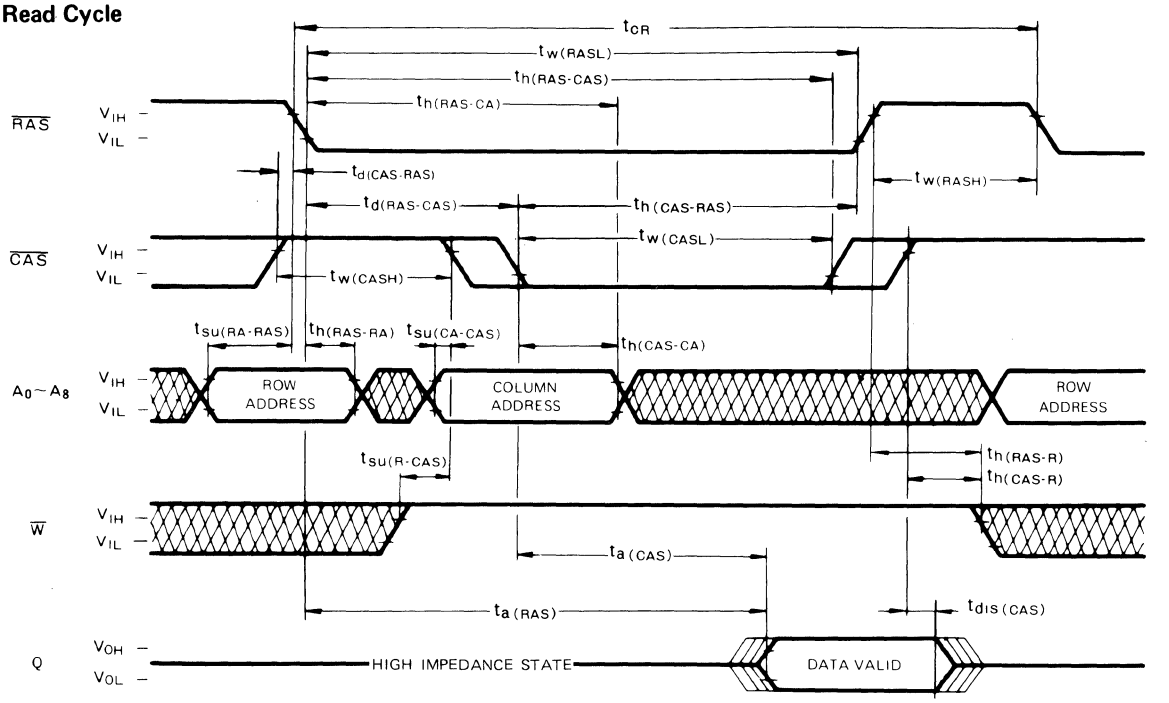
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## Nibble Mode Addressing Sequence Example

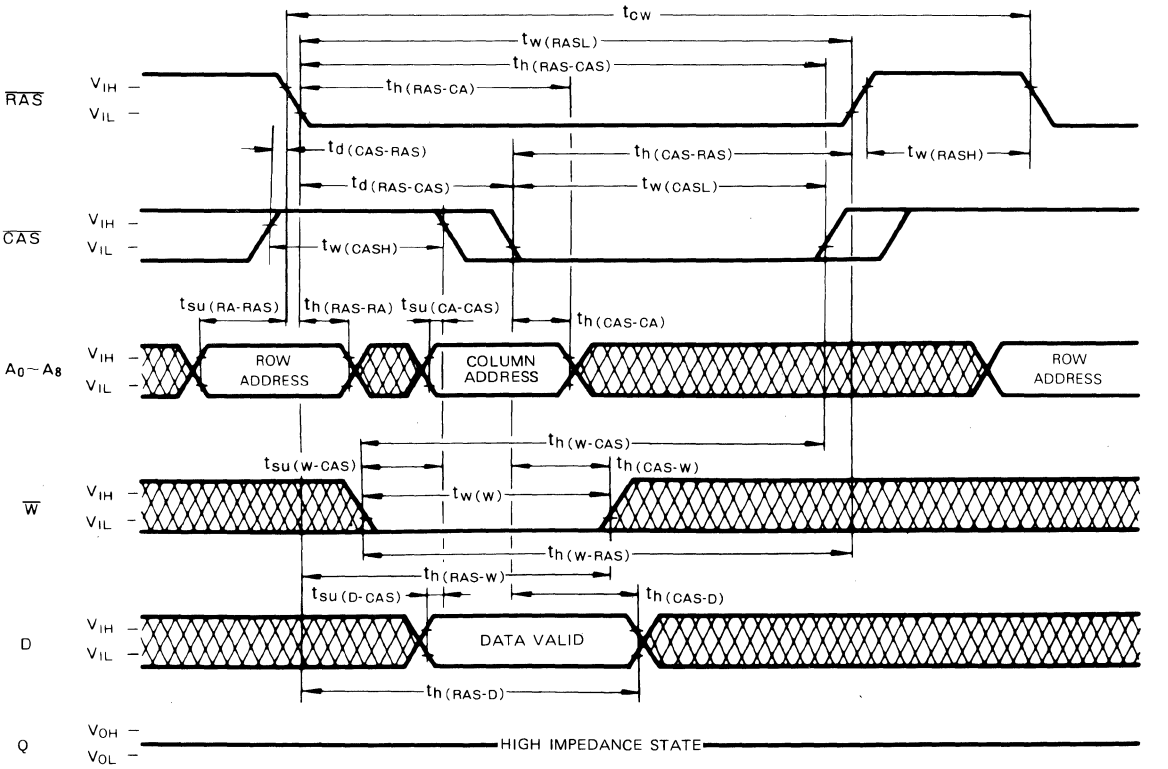
| Sequence | Nibble bit | Column address | | | | | | | | | Row address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | |
| $\overline{RAS}/\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | External address |
| toggle $\overline{CAS}$ | 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Internally generated address |
| toggle $\overline{CAS}$ | 3 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| toggle $\overline{CAS}$ | 4 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | |
| toggle $\overline{CAS}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |

## TIMING DIAGRAMS (Note 19)

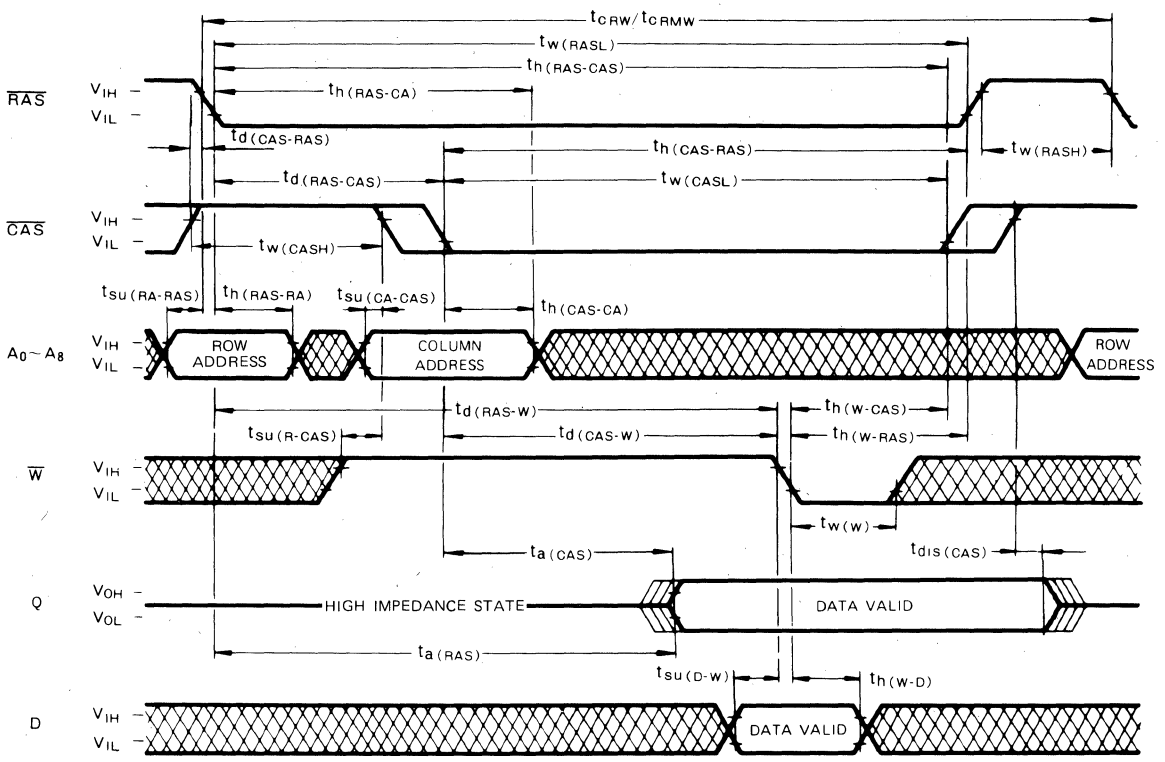
### Read Cycle



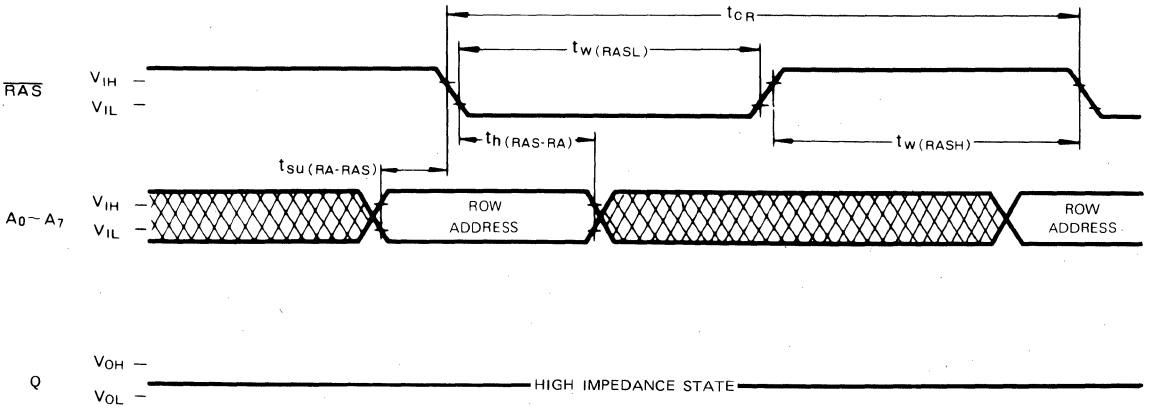

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 20)




Note 19. Indicates the don't care input

The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, D = don't care.
$A_8$ may be $V_{IH}$ or $V_{IL}$.



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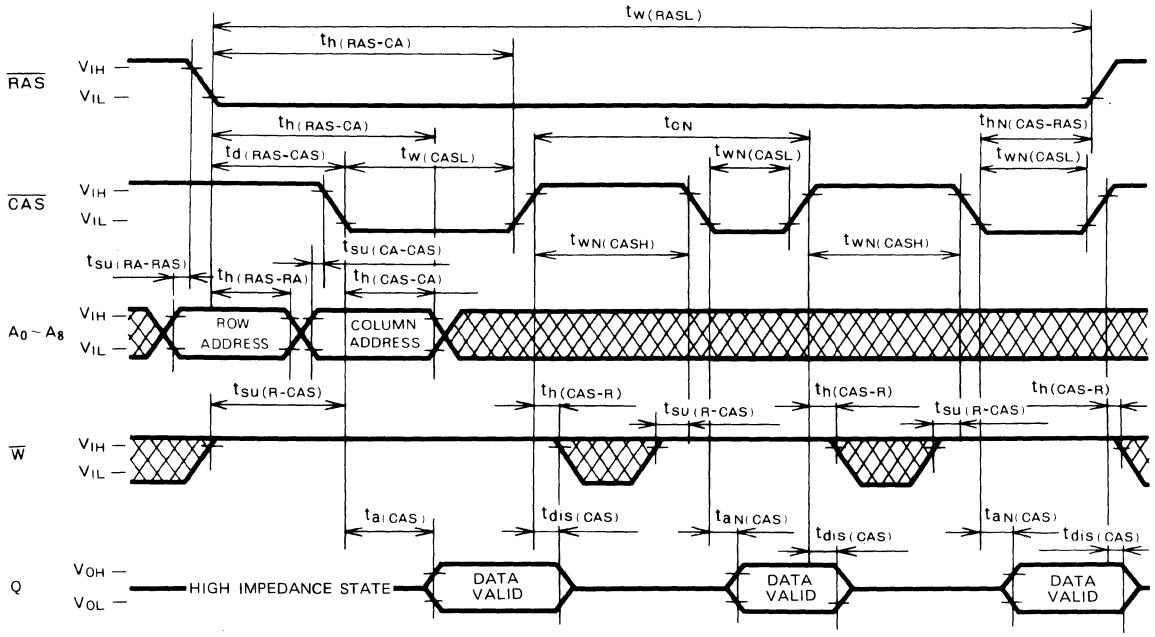
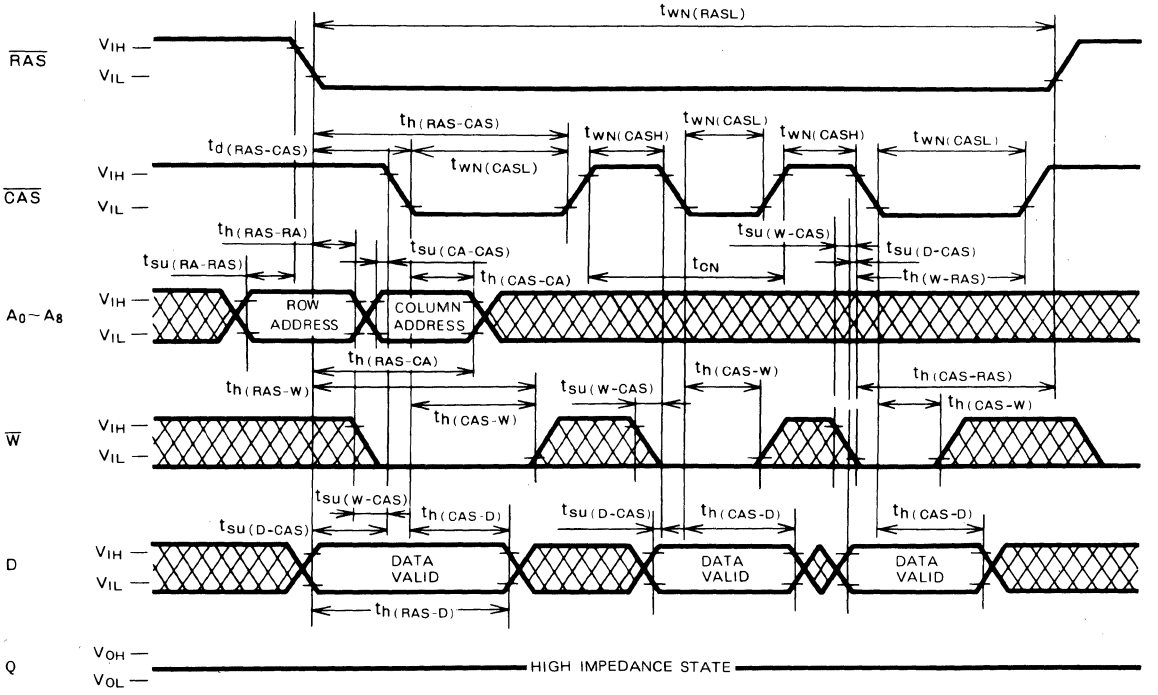
## Nibble Mode Read Cycle (Note 21)

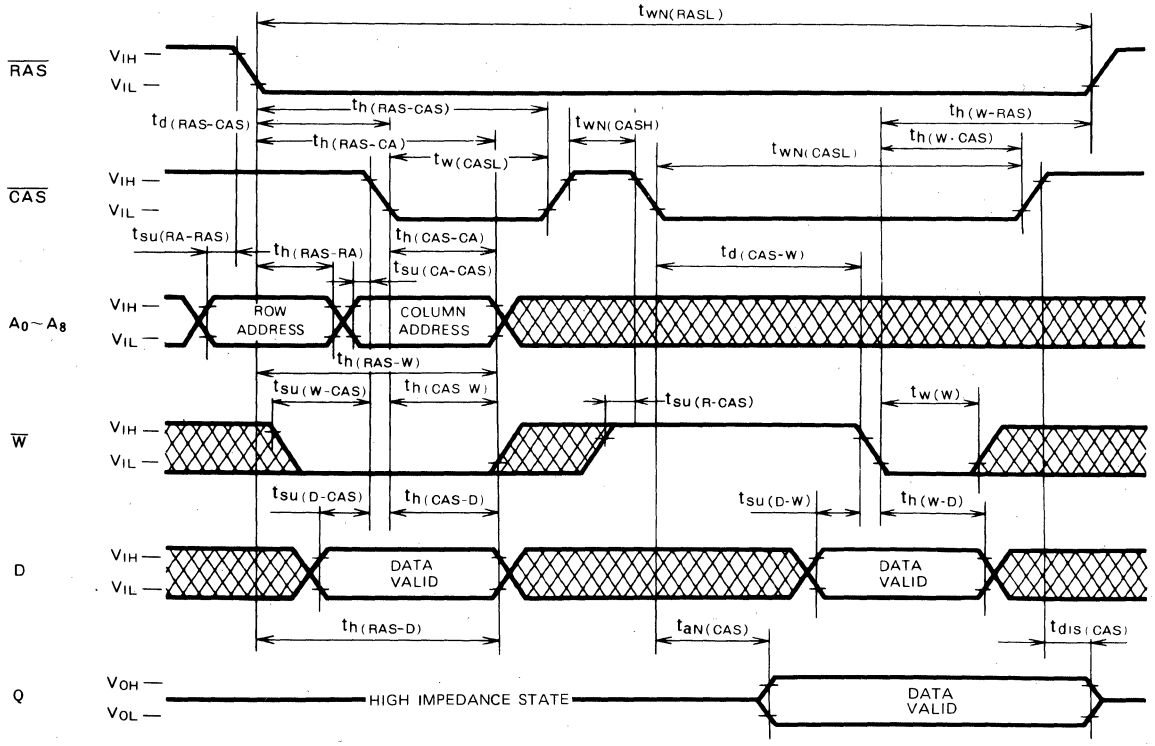



Note 21. Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

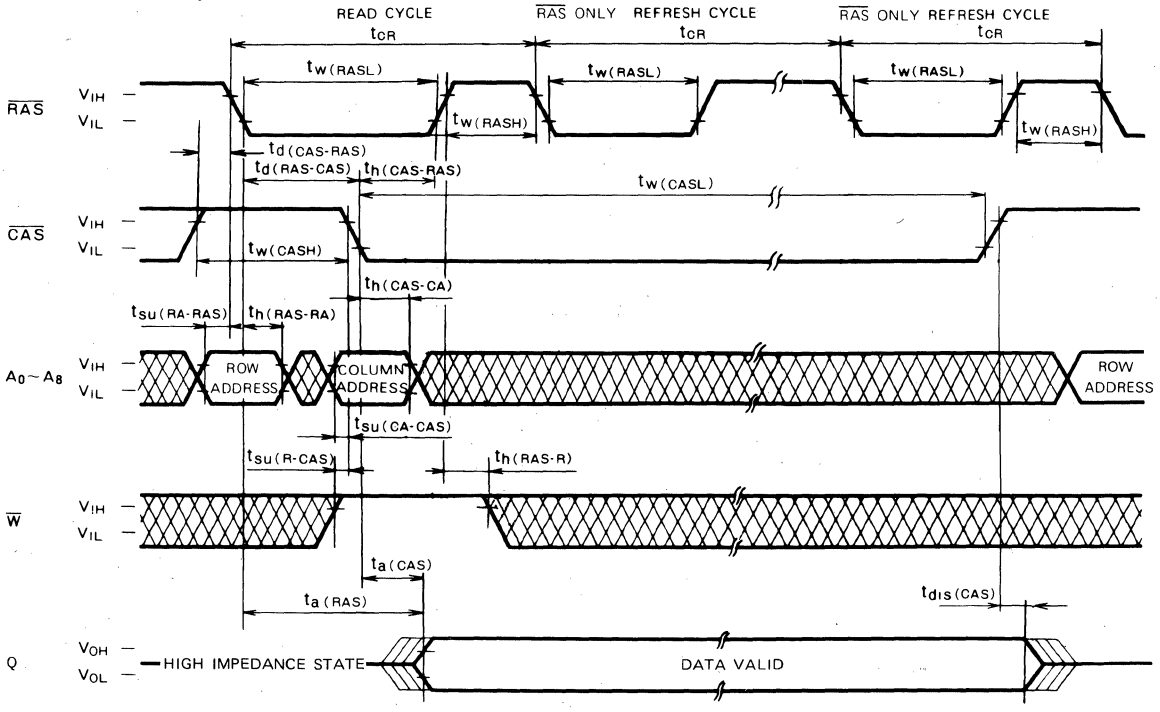
## Nibble Mode Write Cycle (Early Write)



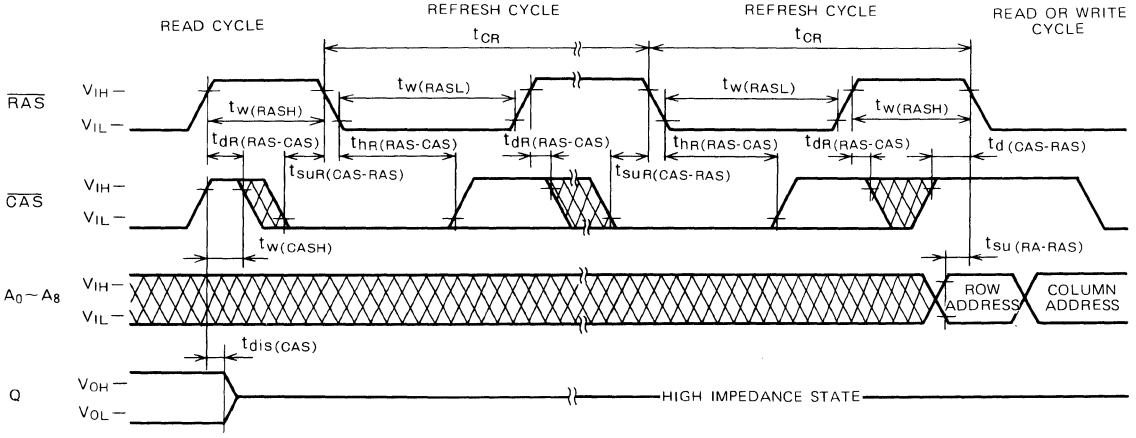
## Nibble Mode Read-Modify-Write Cycle




## Hidden Refresh Cycle



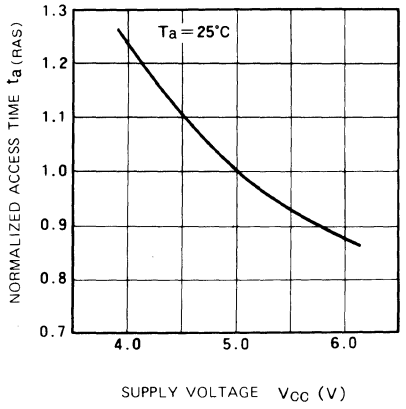
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)



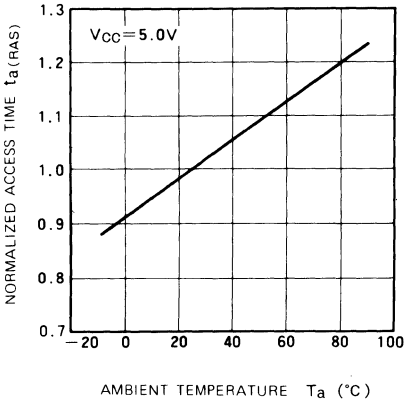

Note 22: $\overline{W}$, D = don't care.

## TYPICAL CHARACTERISTICS

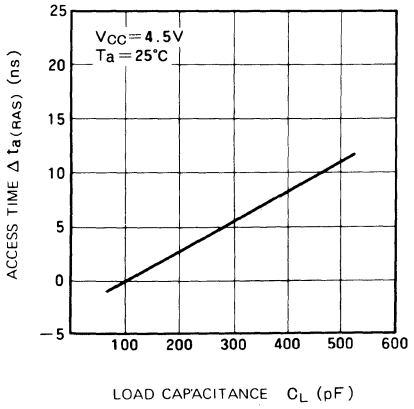
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



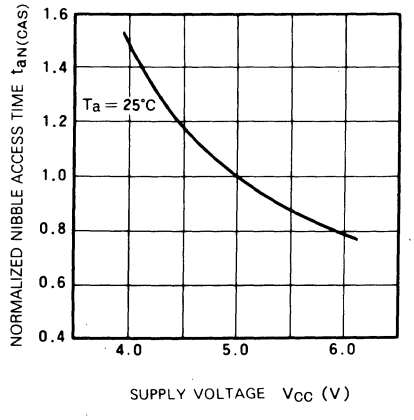

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



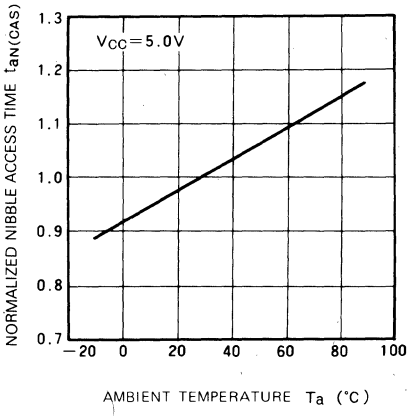

### ACCESS TIME VS. LOAD CAPACITANCE



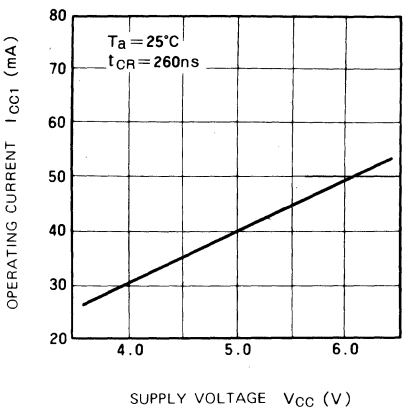

### NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE



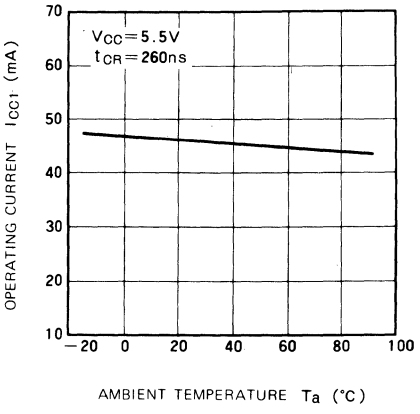
### NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



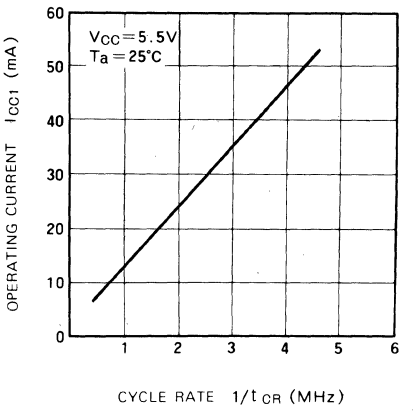

### OPERATING CURRENT VS. SUPPLY VOLTAGE



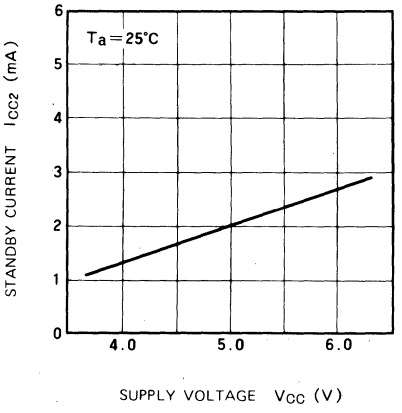

### OPERATING CURRENT VS. AMBIENT TEMPERATURE



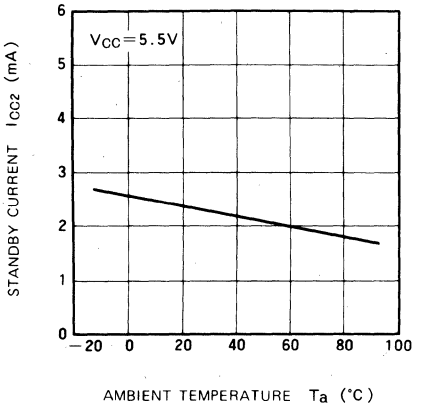

### OPERATING CURRENT VS. CYCLE RATE



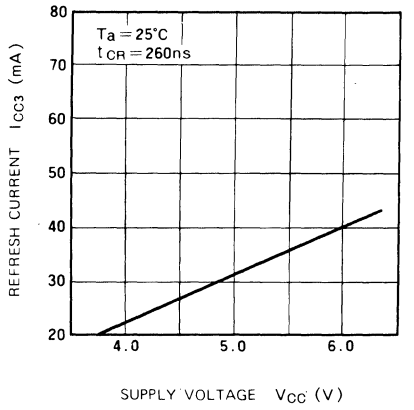

### STANDBY CURRENT VS. SUPPLY VOLTAGE



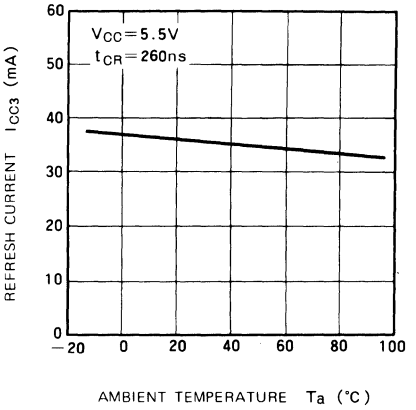

### STANDBY CURRENT VS. AMBIENT TEMPERATURE



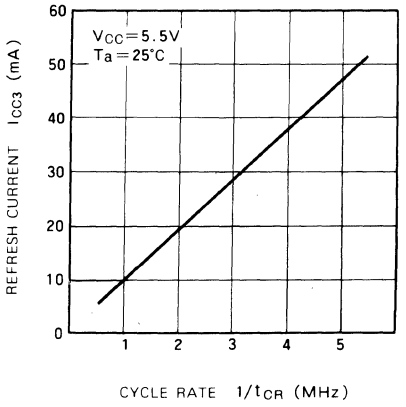
### REFRESH CURRENT VS. SUPPLY VOLTAGE



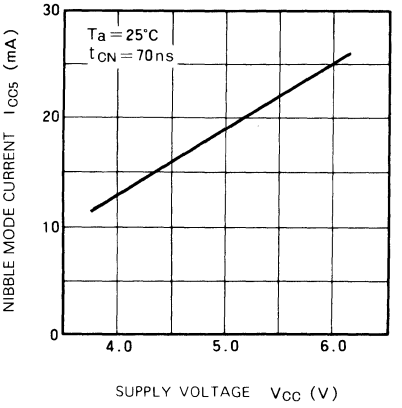

### REFRESH CURRENT VS. AMBIENT TEMPERATURE



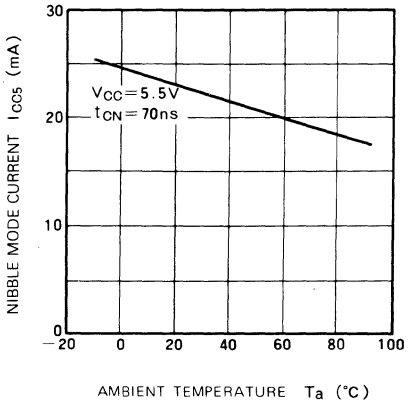

### REFRESH CURRENT VS. CYCLE RATE



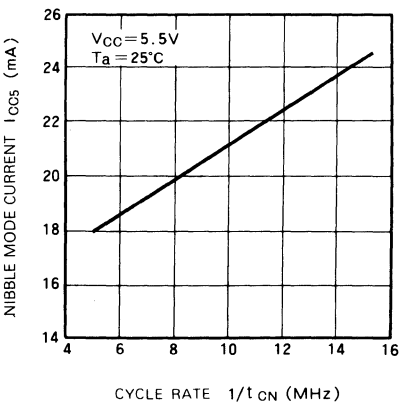

### NIBBLE MODE CURRENT VS. SUPPLY VOLTAGE



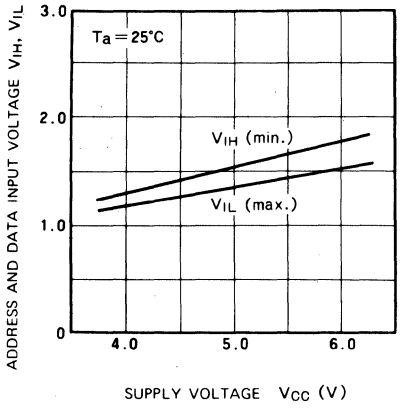

### NIBBLE MODE CURRENT VS. AMBIENT TEMPERATURE



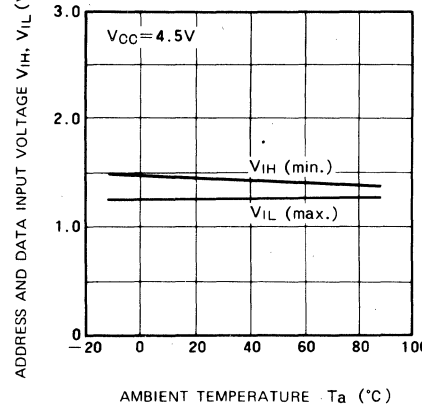

### NIBBLE MODE CURRENT VS. CYCLE RATE



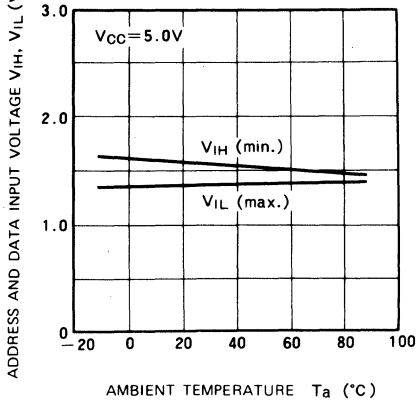
## ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



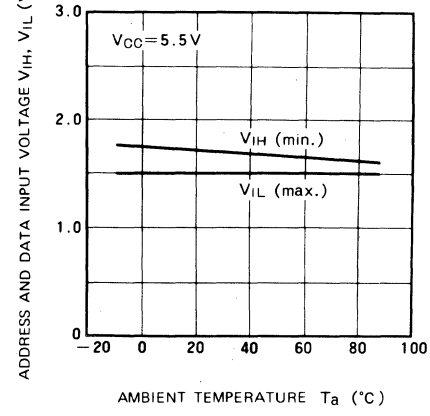

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



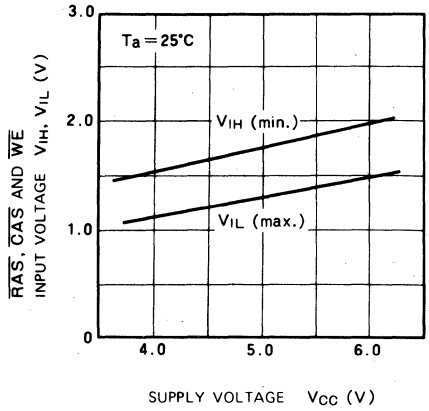

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



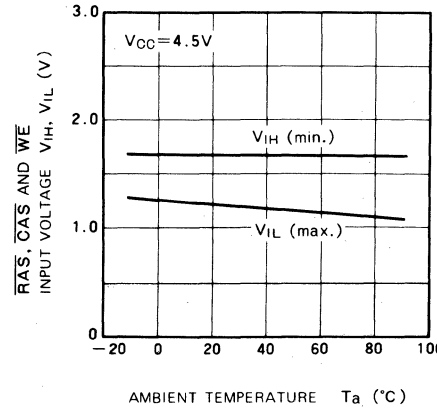

## ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



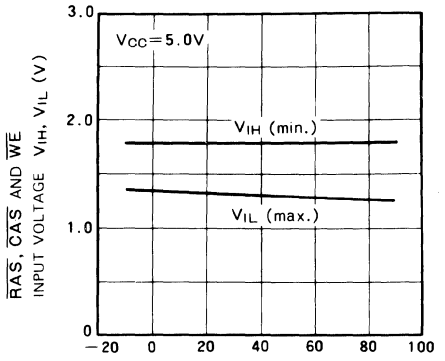

## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



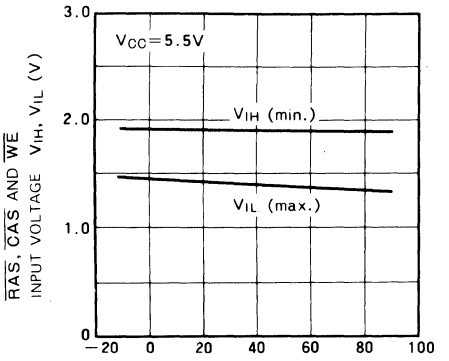

## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



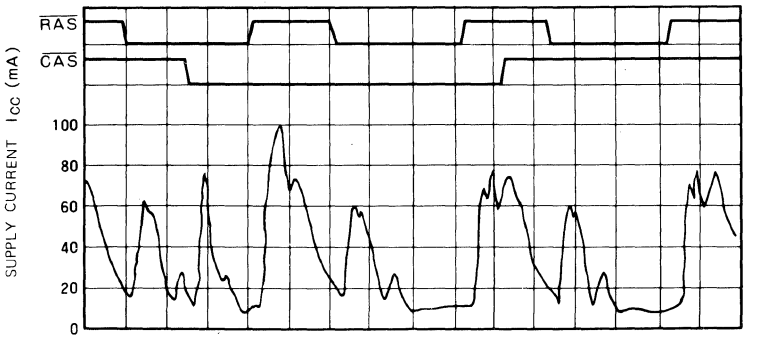
## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



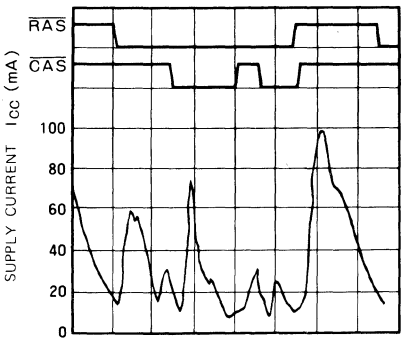

## $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



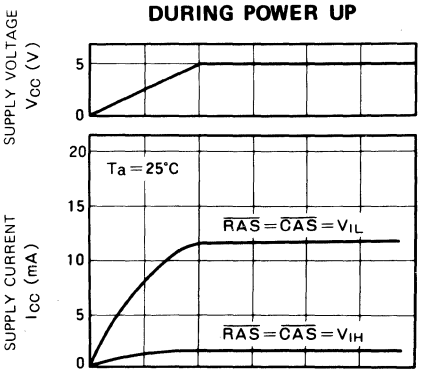

## $\overline{RAS}$/$\overline{CAS}$ CYCLE — HIDDEN REFRESH CYCLE — $\overline{RAS}$ ONLY REFRESH CYCLE




## NIBBLE MODE CYCLE

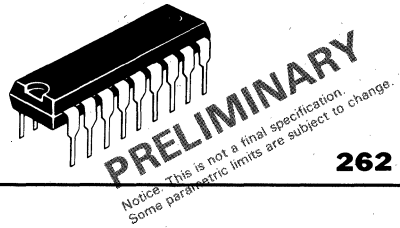



## CURRENT WAVEFORM DURING POWER UP



# M5M4464P-12, -15

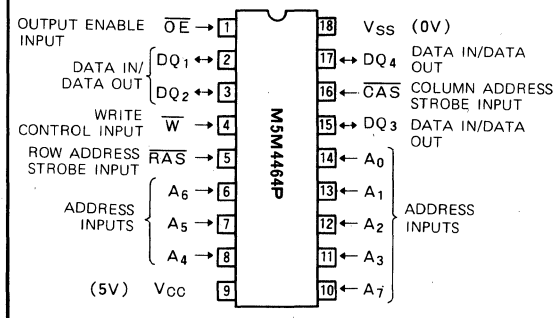
## 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM




## DESCRIPTION

This is family of 65536-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package configuration and an increase in system densities. The M5M4464P operates on a 5V power supply using the on-chip substrate bias generator.

## PIN CONFIGURATION (TOP VIEW)




**Outline 18 P4**

## FEATURES

- Performance ranges

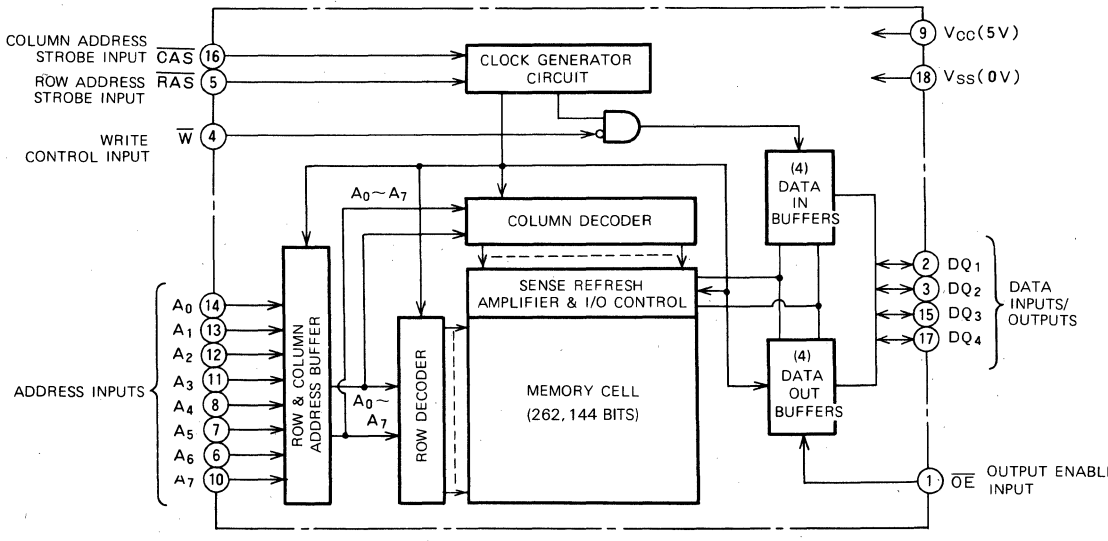
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| M5M4464P-12 | 120 | 220 | 260 |
| M5M4464P-15 | 150 | 260 | 230 |

- 65536 x 4 Organization
- Industry standard 18-pin dual in line package
- Single 5V ±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation:
  M5M4464P-12 360mW (max)
  M5M4464P-15 330mW (max)
- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 256 refresh cycles/4ms
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30$\mu$s max

## APPLICATION

- Refresh memory for CRT
- Micro computer memory

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 262 144-BIT(65 536-WORD BY 4-BIT) DYNAMIC RAM

## FUNCTION

The M5M4464P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Input/Output | | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | $\overline{OE}$ | Row address | Column adress | Input DQ | Output DQ | | |
| Read | ACT | ACT | NAC | ACT | APD | APD | OPN | VLD | YES | Page mode identical |
| Write (Early Write) | ACT | ACT | ACT | DNC | APD | APD | VLD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | ACT | APD | APD | VLD | VLD | YES | |
| $\overline{RAS}$-only retfesh | ACT | NAC | DNC | DNC | APD | DNC | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | ACT | APD | DNC | OPN | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

## SUMMARY OF OPERATIONS

### Addressing

To select one of the 262144 memory cells in the M5M4464P the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to CAS $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

**write enable ($\overline{W}$)**

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

**data-in (DQ1 through DQ4)**

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

**data-out (DQ1 through DQ4)**

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying $t_{OEHD}$

**output enable ($\overline{OE}$)**

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

## Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4464P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4464P are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

In this refresh method, the $\overline{CAS}$ clock should be at a $V_{IH}$ level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

**3. $\overline{CAS}$ before $\overline{RAS}$ Refresh**

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

*If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

**4. Hidden Refresh**

A feature of the M5M4464P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the M5M4464P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4464P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The M5M4464P operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | parameter | Condtions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply volrage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 1000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2.0 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−2mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins ＝0V | −10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{cc}$, operating (Note 3,4) | M5M4464P-12 | $\overline{RAS}$, $\overline{CAS}$ cycling | | | 65 | mA |
| | | M5M4464P-15 | $t_c(rd)=t_c(w)$ = min output open | | | 60 | mA |
| $I_{CC2}$ | Supply current from $V_{cc}$, standby | | $\overline{RAS}=V_{IH}$ output open | | | 4 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{cc}$, retreshing (Note 3) | M5M4464P-12 | $\overline{RAS}$ cycling $\overline{CAS}=V_{IH}$ | | | 55 | mA |
| | | M5M4464P-15 | $t_c(Prd)$ = min, output open | | | 50 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{cc}$, page mode (Note 3,4) | M5M4464P-12 | $\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling | | | 50 | mA |
| | | M5M4464P-15 | $t_c(Prd)$ = min, output open | | | 45 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{cc}$, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M4464P-12 | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling | | | 60 | mA |
| | | M5M4464P-15 | $t_c(RAS)$= min, output open | | | 55 | mA |

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## CAPACITANCE (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$＝$V_{SS}$ f＝1MHz Vi＝25mVrms | | | 5 | pF |
| $C_{I(OE)}$ | Input capacitance, $\overline{OE}$ input | | | | 7 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | 7 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | 10 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | 10 | pF |
| $C_{I/O}$ | Input/Output capacitance, data ports | | | | 10 | pF |

## SWITCHING CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted) (Note 5)

| Symbol | Parameter | | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{a(C)}$ | Access time from $\overline{CAS}$ | (Note 6,7) | $t_{CAC}$ | | 60 | | 75 | ns |
| $t_{a(R)}$ | Access time from $\overline{RAS}$ | (Note 6,8) | $t_{RAC}$ | | 120 | | 150 | ns |
| $t_{a(OE)}$ | Access time from $\overline{OE}$ | (Note 6) | — | | 30 | | 40 | ns |
| $t_{dis(CH)}$ | Output disable time after $\overline{CAS}$ high | (Note 9) | $t_{OFF}$ | 0 | 25 | 0 | 30 | ns |
| $t_{dis(OE)}$ | Output disable time after $\overline{OE}$ high | (Note 9) | — | 0 | 25 | 0 | 30 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If $t_{RLCL}$ is greater than $t_{RLCL}$ max then $t_{a(R)}$ will increase by the amount that $t_{RLCL}$ exceeds $t_{RLCL}$ max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH}$ min or $V_{OL}$ max.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted, See notes 10,11)

| Symbol | Parameter | | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{C(RF)}$ | Refresh cycle time | | $t_{REF}$ | | 4 | | 4 | ms |
| $t_{W(RH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 90 | | 100 | | ns |
| $t_{RLCL}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low | (Note 12) | $t_{RCD}$ | 25 | 60 | 30 | 75 | ns |
| $t_{CHRL}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | (Note 13) | $t_{CRP}$ | 10 | | 10 | | ns |
| $t_{su(RA)}$ | Row address setup time before $\overline{RAS}$ low | | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(CA)}$ | Column address setup time before $\overline{CAS}$ low | | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{h(RA)}$ | Row address hold time after $\overline{RAS}$ low | | $t_{RAH}$ | 15 | | 20 | | ns |
| $t_{h(CLCA)}$ | Column address hold time after $\overline{CAS}$ low | | $t_{CAH}$ | 20 | | 25 | | ns |
| $t_{h(RLCA)}$ | Column address hold time after $\overline{RAS}$ low | | $t_{AR}$ | 80 | | 100 | | ns |
| $t_T$ | Transition time (rise and fall) | (Note 14) | $t_T$ | 3 | 50 | 3 | 50 | ns |

Note 10: The timing requirements are assumed $t_T$=5ns.
11: $V_{IH}$ min and $V_{IL}$ max are reference levels for measuring timing of input signals.
12: $t_{RLCL}$ max is specified as a reference point only; if $t_{RLCL}$ is less than $t_{RLCL}$ max, access time is $t_{a(R)}$, if $t_{RLCL}$ is greater than $t_{RLCL}$ max, access time is $t_{RLCL} + t_{a(C)} \cdot t_{RLCL}$ min is specified as $t_{RLCL}$ min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: $t_{CHRL}$ requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: $t_T$ is measured between $V_{IH}$ min and $V_{IL}$ max.

### Read and Refresh Cycles

| Symbol | Parameter | | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{C(rd)}$ | Read cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{W(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{su(rd)}$ | Read setup time before $\overline{CAS}$ low | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{h(CHrd)}$ | Read hold time after $\overline{CAS}$ high | (Note 15) | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(RHrd)}$ | Read hold time after $\overline{RAS}$ high | (Note 15) | $t_{RRH}$ | 10 | | 10 | | ns |
| $t_{h(OECH)}$ | $\overline{CAS}$ hold time after $\overline{OE}$ low | | — | 30 | | 40 | | ns |
| $t_{h(OERH)}$ | $\overline{RAS}$ hold time after $\overline{OE}$ low | | — | 30 | | 40 | | ns |
| $t_{h(CLOE)}$ | $\overline{OE}$ hold time after $\overline{CAS}$ low | | — | 60 | | 75 | | ns |
| $t_{h(RLOE)}$ | $\overline{OE}$ hold time after $\overline{RAS}$ low | | — | 120 | | 150 | | ns |
| $t_{DOEL}$ | Delay time, Data to $\overline{OE}$ low | | — | 0 | | 0 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |
| $t_{RHCL}$ | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | | — | 0 | | 0 | | ns |

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

## Write Cycles (Early Write and Delayed Write)

| Symbol | Parameter | | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{c(W)}$ | Write cycle time | | $t_{RC}$ | 220 | | 260 | | ns |
| $t_{w(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | ns |
| $t_{w(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 60 | | 75 | | ns |
| $t_{w(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 60 | | 75 | | ns |
| $t_{su(WCL)}$ | Write setup time before $\overline{CAS}$ low | (Note 17) | $t_{WCS}$ | −5 | | −5 | | ns |
| $t_{h(CLW)}$ | Write hold time after $\overline{CAS}$ low | | $t_{WCH}$ | 40 | | 45 | | ns |
| $t_{h(RLW)}$ | Write hold time after $\overline{RAS}$ low | | $t_{WCR}$ | 100 | | 120 | | ns |
| $t_{h(WCH)}$ | $\overline{CAS}$ hold time after Write low | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{h(WRH)}$ | $\overline{RAS}$ hold time after Write low | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D)}$ | Data setup time | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(WLD)}$ | Data hold time after Write low | | $t_{DH}$ | 30 | | 35 | | ns |
| $t_{h(CLD)}$ | Data hold time after $\overline{CAS}$ low | | $t_{DH}$ | 30 | | 35 | | ns |
| $t_{h(RLD)}$ | Data hold time after $\overline{RAS}$ low | | $t_{DHR}$ | 90 | | 110 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |
| $t_{h(WOE)}$ | $\overline{OE}$ hold time after Write low | | — | 25 | | 30 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{c(rdW)}$ | Read write/read modify write cycle time | (Note 16) | $t_{RWC}$ | 295 | | 345 | | ns |
| $t_{w(RL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 195 | 10000 | 255 | 10000 | ns |
| $t_{w(CL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 135 | | 180 | | ns |
| $t_{h(RLCH)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | $t_{CSH}$ | 195 | | 255 | | ns |
| $t_{h(CLRH)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | $t_{RSH}$ | 135 | | 180 | | ns |
| $t_{w(CH)}$ | $\overline{CAS}$ high pulse width | | $t_{CPN}$ | 30 | | 35 | | ns |
| $t_{su(rd)}$ | Read setup time before $\overline{CAS}$ low | | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{CLWL}$ | Delay time, $\overline{CAS}$ low to Write low | (Note 17) | $t_{CWD}$ | 90 | | 110 | | ns |
| $t_{RLWL}$ | Delay time, $\overline{RAS}$ low to Write low | (Note 17) | $t_{RWD}$ | 150 | | 185 | | ns |
| $t_{h(WCH)}$ | $\overline{CAS}$ hold time after Write low | | $t_{CWL}$ | 40 | | 45 | | ns |
| $t_{h(WRH)}$ | $\overline{RAS}$ hold time after Write low | | $t_{RWL}$ | 40 | | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 40 | | 45 | | ns |
| $t_{su(D)}$ | Data setup time | | $t_{DS}$ | 0 | | 0 | | ns |
| $t_{h(WLD)}$ | Data hold time after Write low | | $t_{DH}$ | 40 | | 45 | | ns |
| $t_{h(CLOE)}$ | $\overline{OE}$ hold time after $\overline{CAS}$ low | | — | 60 | | 75 | | ns |
| $t_{h(RLOE)}$ | $\overline{OE}$ hold time after $\overline{RAS}$ low | | — | 120 | | 150 | | ns |
| $t_{DOEL}$ | Delay time, Data to $\overline{OE}$ low | | — | 0 | | 0 | | ns |
| $t_{OEHD}$ | Delay time, $\overline{OE}$ high to Data | | — | 25 | | 30 | | ns |

Note 16: $t_{c(rdW)}$ is specified as $t_{c(rdW)}$ min = $t_{a(R)}$ max + $t_{OEHD}$ min + $t_{h(WRH)}$ min + $t_{w(RH)}$ min + 4 $t_T$.

17: $t_{su(WCL)}$, $t_{CLWL}$ and $t_{RLWL}$ are specified as reference points only. If $t_{su(WCL)} \geqq t_{su(WCL)}$ min, the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CLWL} \geqq t_{CLWL}$ min and $t_{RLWL} \geqq t_{RLWL}$ min, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to $V_{IH}$) is indeterminate.

## Page-Mode Cycle (Note 18)

| Symbol | Parameter | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{C(Prd)}$ | Read cycle time | $t_{PC}$ | 120 | | 145 | | ns |
| $t_{C(PW)}$ | Write cycle time | $t_{PC}$ | 120 | | 145 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width (Note 19) | $t_{RAS}$ | 240 | 30000 | 295 | 30000 | ns |
| $t_{C(PrdW)}$ | Read write/read modify write cycle time | — | 195 | | 250 | | ns |
| $t_{W(RL)}$ | $\overline{RAS}$ low pulse width (Note 20) | $t_{RAS}$ | 390 | 30000 | 505 | 30000 | ns |
| $t_{W(CH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 50 | | 60 | | ns |

Note 18: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19: Specified for read or write cycle.
20: Specified for read-write or read-modify-write cycle.

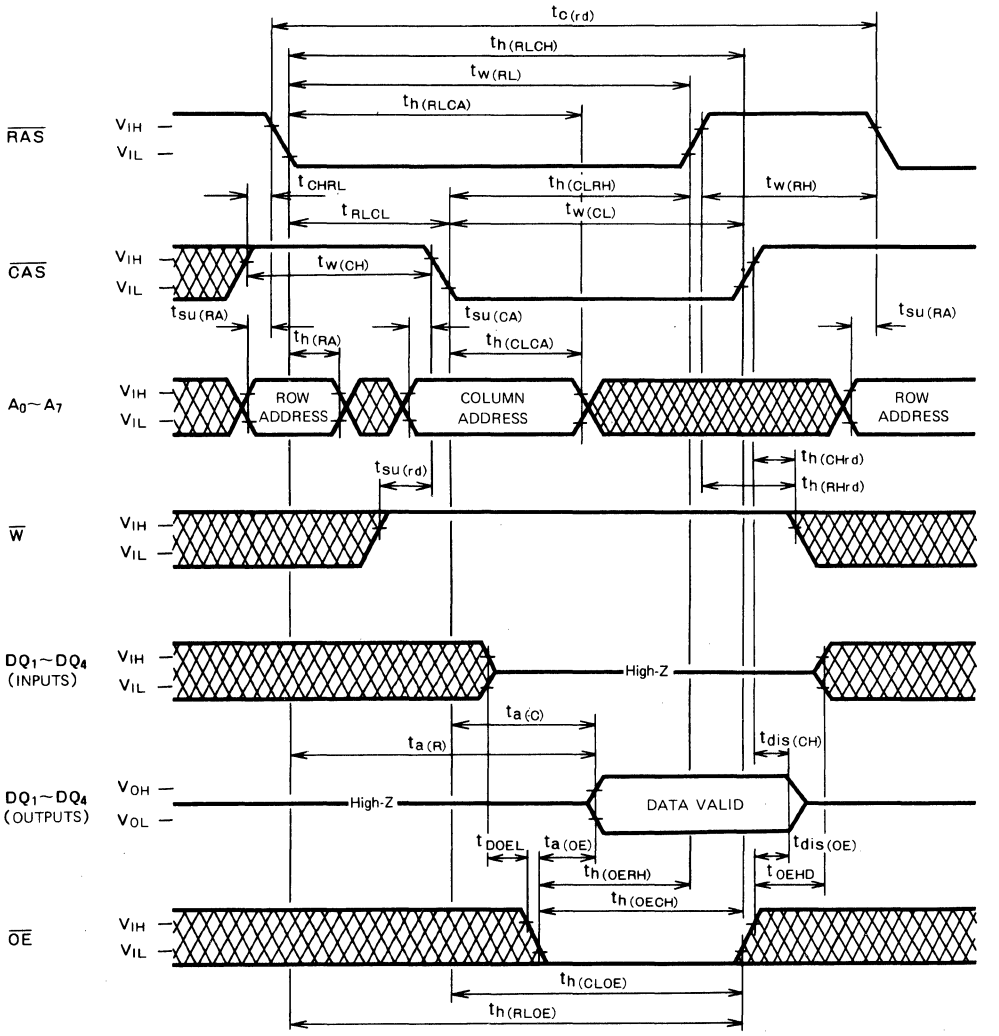
## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

| Symbol | Parameter | Alternative Symbol | M5M4464P-12 Limits | | M5M4464P-15 Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{su\,R(CAS-RAS)}$ | $\overline{CAS}$ setup time for auto refresh | $t_{CSR}$ | 10 | | 10 | | ns |
| $t_{h\,R(RAS-CAS)}$ | $\overline{CAS}$ hold time for auto refresh | $t_{CHR}$ | 25 | | 30 | | ns |
| $t_{d\,R(RAS-CAS)}$ | Precharge to $\overline{CAS}$ active time | $t_{RPC}$ | 0 | | 0 | | ns |

Note 21: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

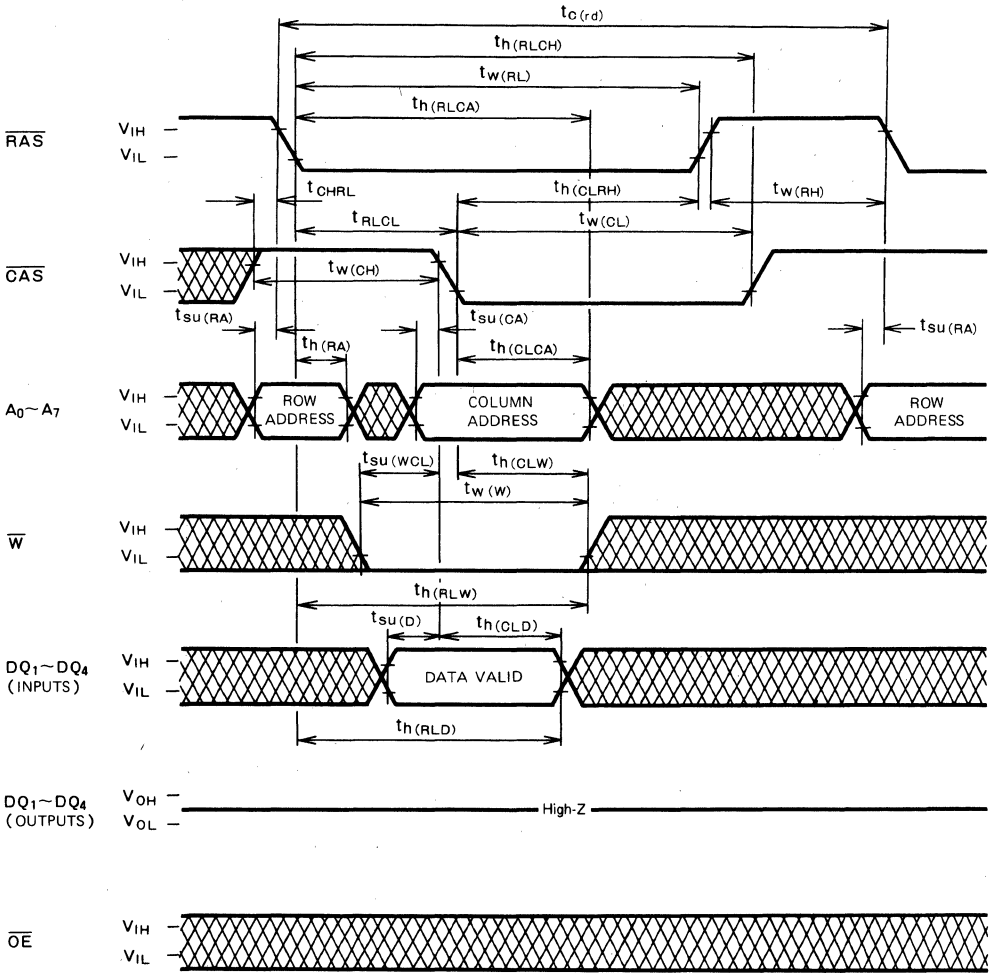
## TIMING DIAGRAMS (Note 22)

### Read Cycle

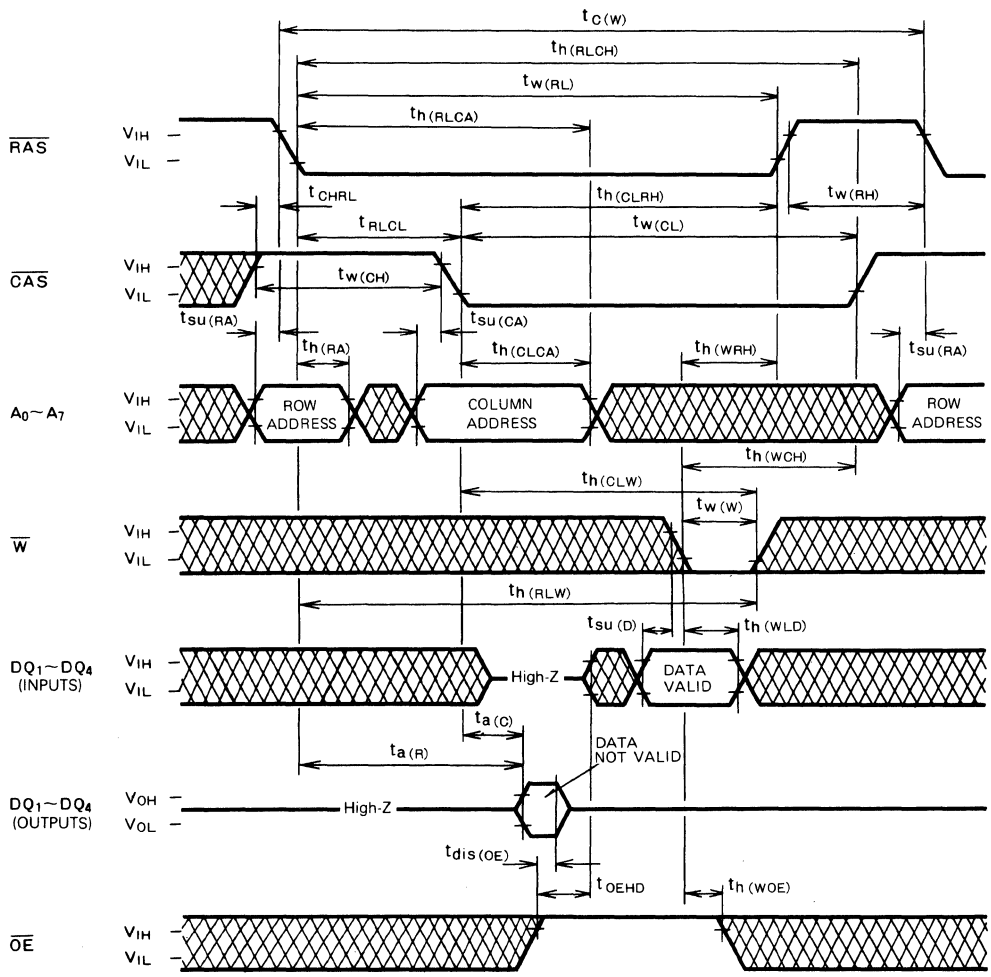



Note 22. Indicates the don't care input.

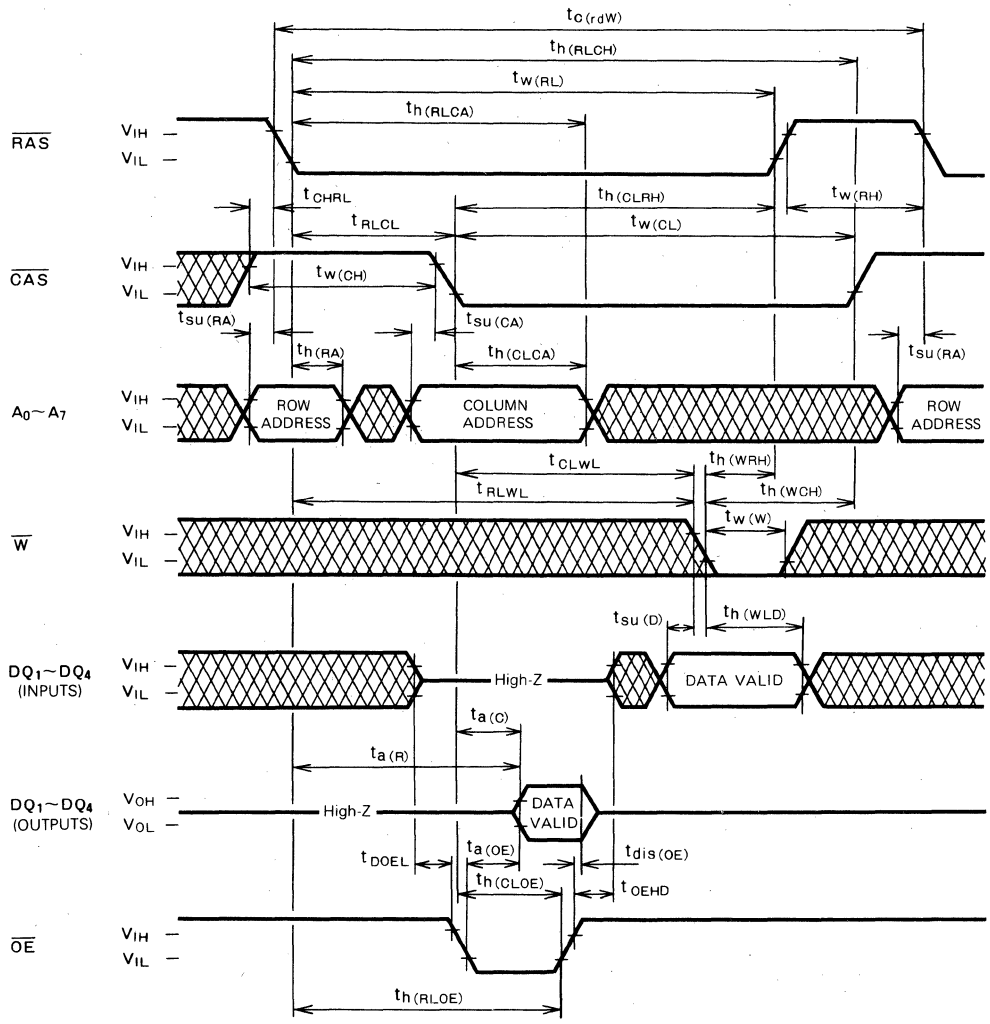
## Write Cycle (Early Write)



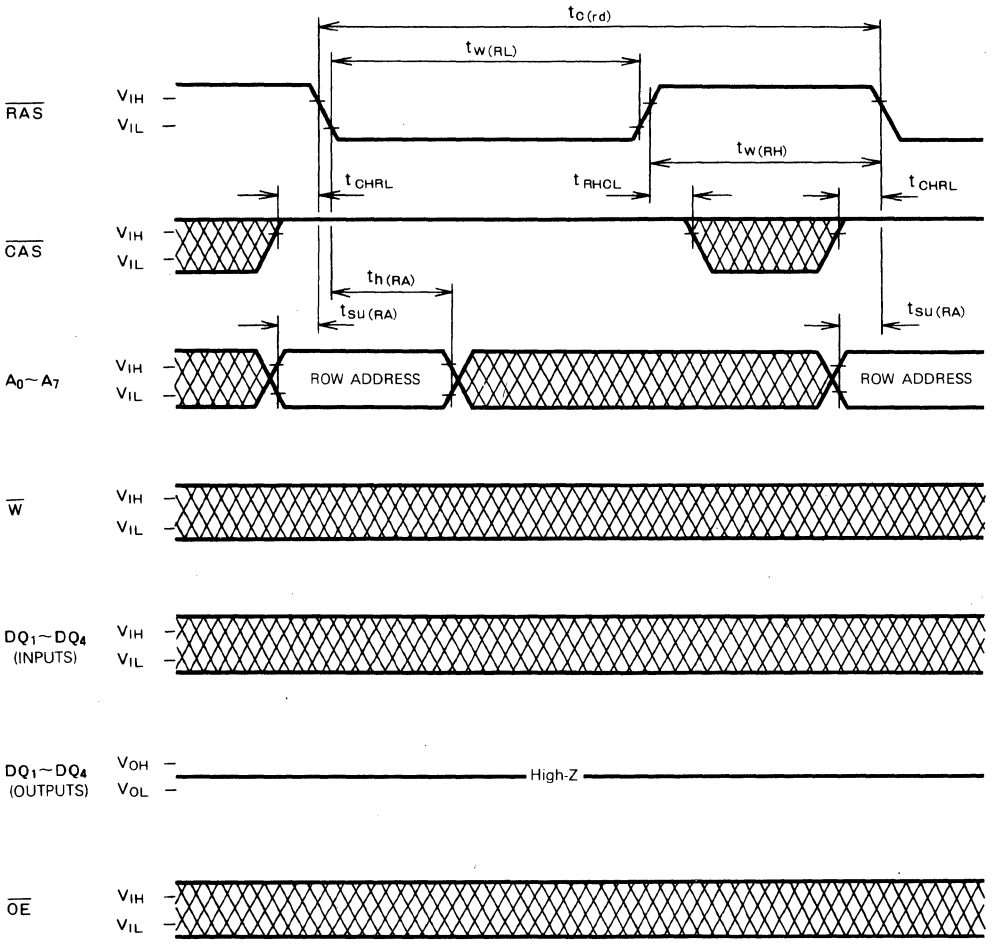
## Write Cycle (Delayed Write)



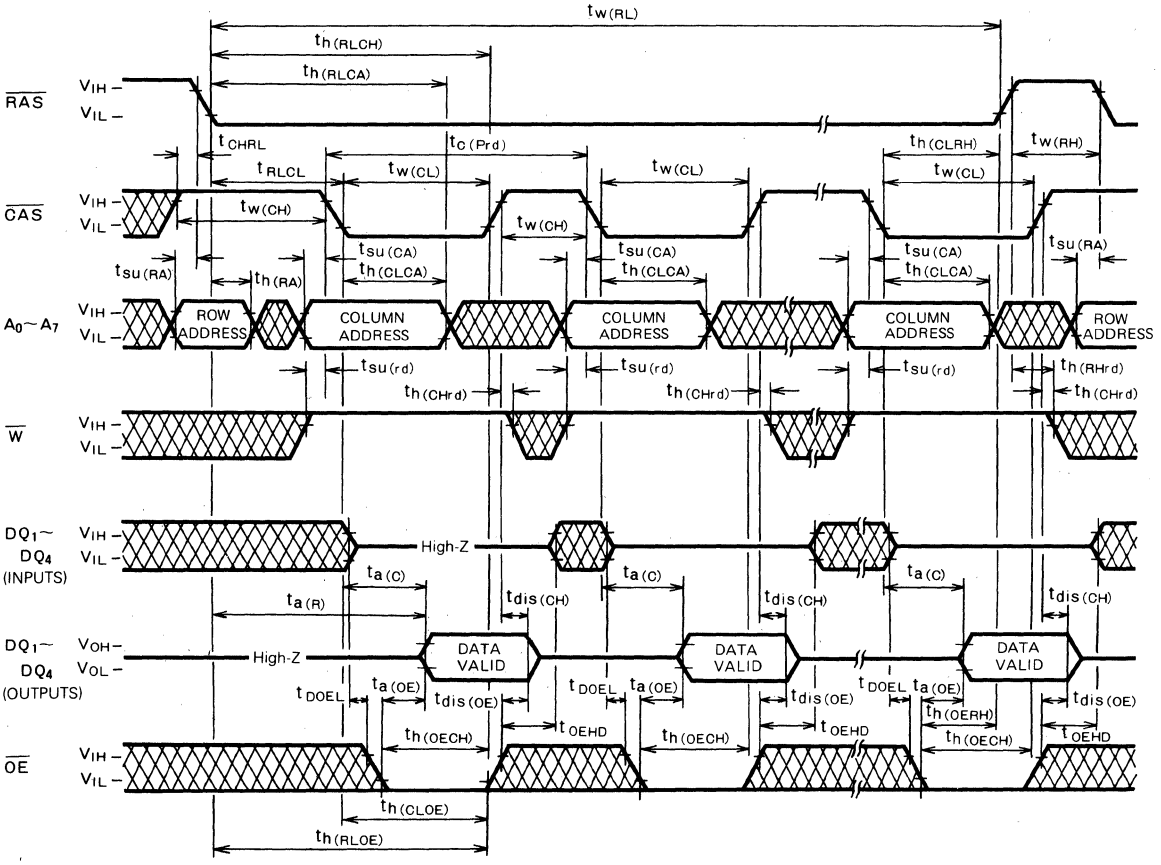
## Read-Write and Read-Modify-Write Cycles



## $\overline{RAS}$-Only Refresh Cycle



## Page-Mode Read Cycle



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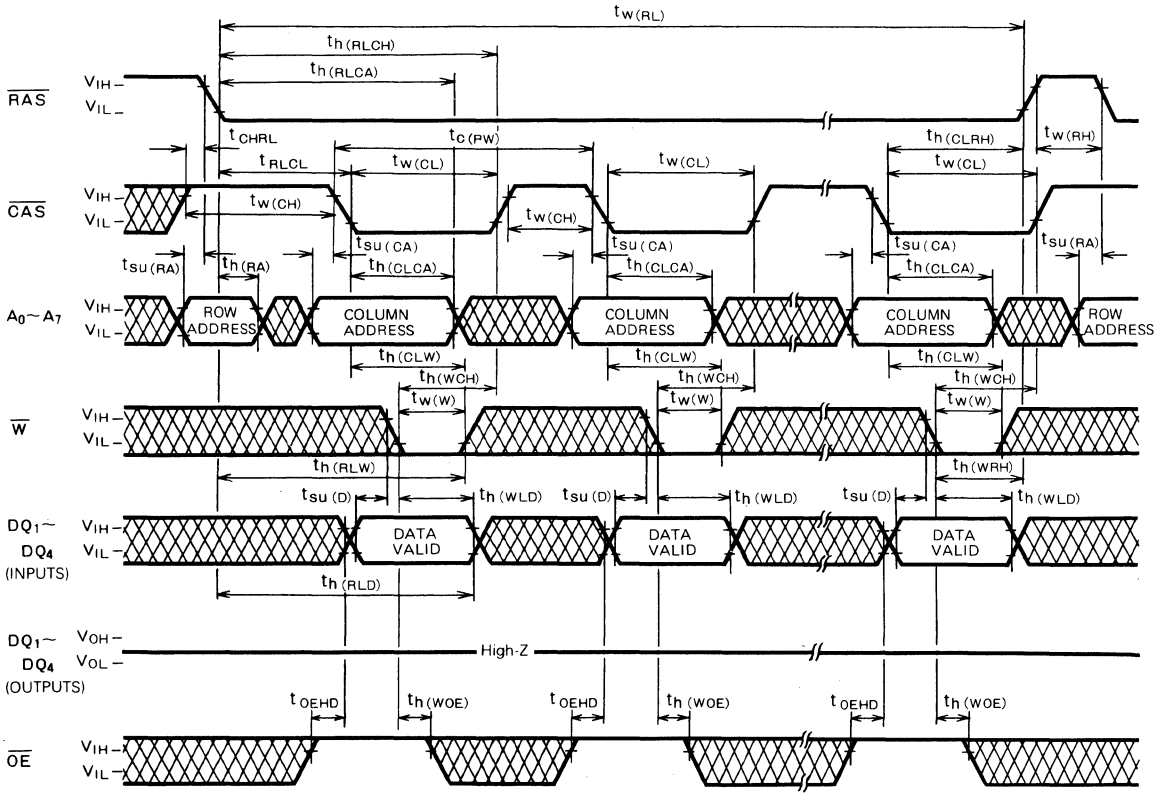
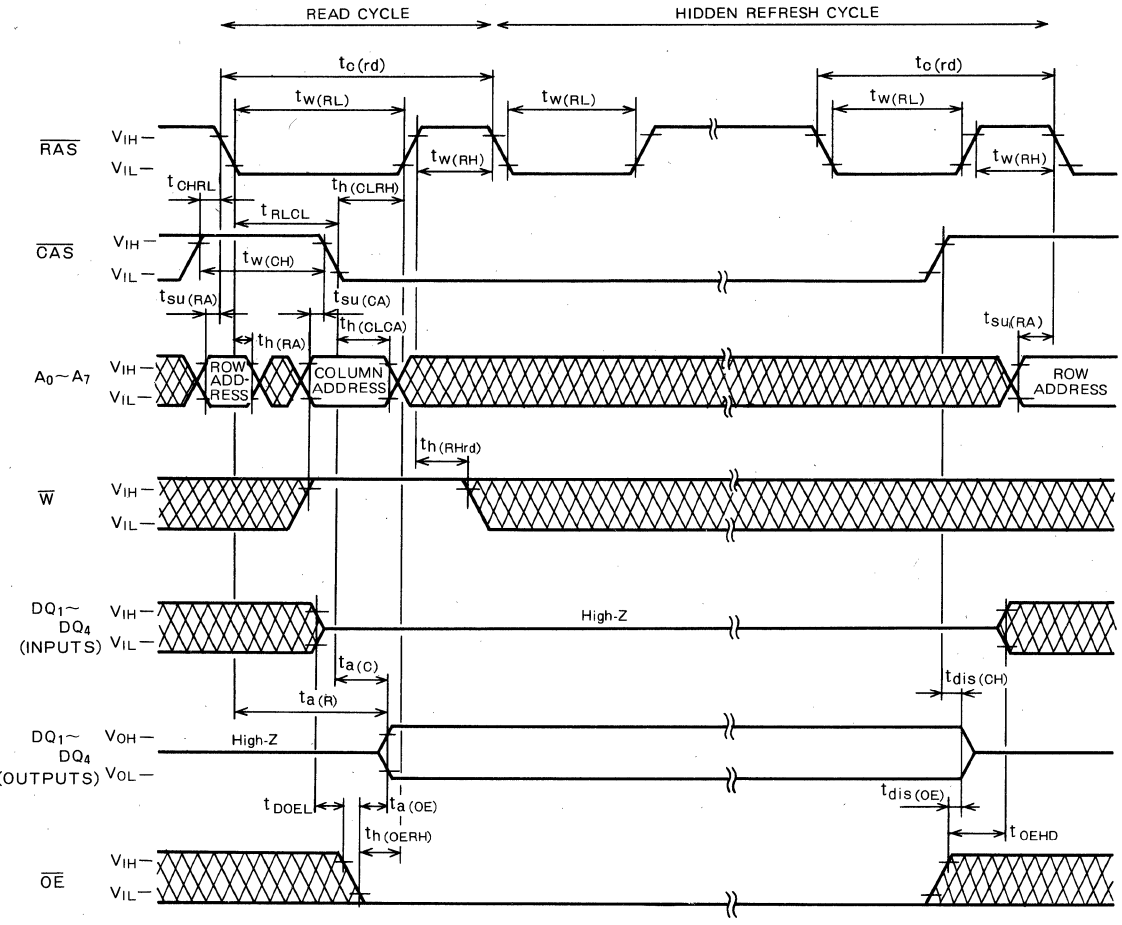
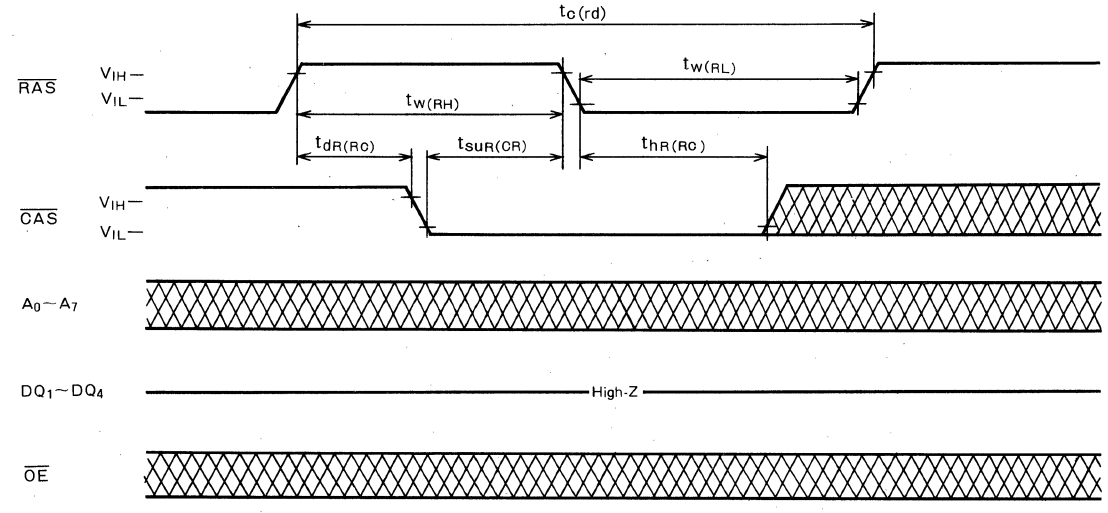
## Page-Mode Write Cycle

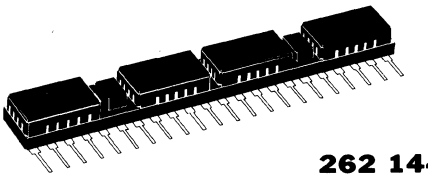


## Hidden Refresh Cycle




## CAS before RAS Refresh Cycle







# MH6404AD1-15

## 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

## DESCRIPTION

The MH6404AD1 is 65 536-word x 4 bit dynamic RAM and consists of four industry standard 64 K x 1 dynamic RAMs in leadless chip carrier.

The mounting of leadless chip carriers on a ceramic single in-line package provides any application where high densities and large quantities of memory are required.

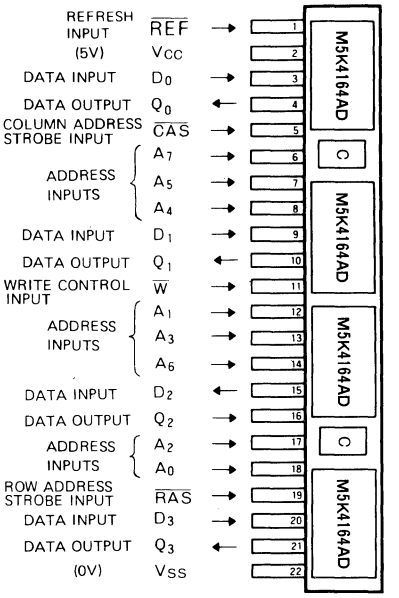
## FEATURES

- High speed

| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| MH6404AD1-15 | 150 | 260 | 600 |

- Utilizes industry standard 64K RAMs in leadless chip carriers
- 22 pin Single In-line Package
- Single +5V (±10%) supply operation
- Low stand by power dissipation ..... 88 mW(max)
- Low operating power dissipation:
  MH6404AD1-15 990mW(max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF x 2) decoupling capacitors
- 128 refresh cycles (every 2ms) $A_7$ Pin is not need for refresh
- Pin 1 controls automatic-and self-refresh mode

## PIN CONFIGURATION (TOP VIEW)

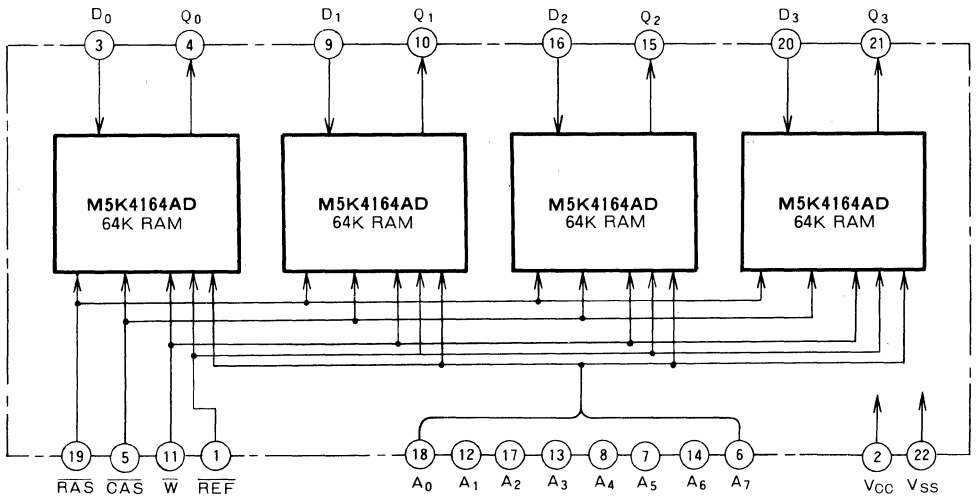



**Outline 22S5**

## APPLICATION

- Main memory unit for computers
- Refresh memory for CRT

## BLOCK DIAGRAM



## FUNCTION

The MH6404AD1 provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | $\overline{REF}$ | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | NAC | VLD | YES | Page mode identical |
| Write | ACT | ACT | ACT | VLD | APD | APD | NAC | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | NAC | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | NAC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | NAC | VLD | YES | |
| Automatic refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Self refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Hidden automatic refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Hidden self refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | NAC | OPN | NO | |

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

## SUMMARY OF OPERATIONS

### Addressing

To select 4 of the 262144 memory cells in the MH6404AD1 the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Date to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is storobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for set-up and hold times.

### Data Output Control

The outputs of the MH6404AD1 are in the high-impedance state when $\overline{CAS}$ is high. When the are memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the outputs entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The outputs will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the MH6404AD1, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, inputs and outputs can be connected directly to give a common I/O data bus.

**2. Data Output Hold**

The data outputs can be held between read cycles, without lenghening the cycle time. This enebles extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the MH6404AD1 must be refreshed every 2 ms to maintain data. The methods of refreshing for the MH6404AD1 are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Automatic Refresh**

Pin1 ($\overline{REF}$) has two special functions. The MH6404AD1 has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is applied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

**4. Self-Refresh**

The other function of pin 1 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the MH6404AD1 will refresh itself. This internal sequence repeats a synchronously every 12 to 16 $\mu$s. After 2 ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 1 (REF) refresh function gives the user a feature that if free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx$800K$\Omega$) on pin 1, so if the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect) without affecting the normal operations.

**5. Hidden Refresh**

A features of the MH6404AD1 is that refresh cycle may be performed while maintaining valid data at the output pins by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the MH6404AD1 is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH6404AD1 as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The MH6404AD1 operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

# 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25℃ | 4000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | ℃ |
| Tstg | Storage temperature range | | −55～150 | ℃ |
| Tsld | Soldering temperature time | | 260・10 | ℃・sec |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −40 | | 40 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note3, 4) | MH6404AD1-15 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$＝$t_{CW}$＝min output open | | | 180 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 16 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | MH6404AD1-15 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ $t_{C(\overline{REF})}$＝min, output open | | | 140 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note3, 4) | MH6404AD1-15 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$＝min, output open | | | 140 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$, automatic refreshing (Note 3) | MH6404AD1-15 | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$ cycling $t_{C(\overline{REF})}$＝min, output open | | | 140 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, self refreshing | | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$＝$V_{IL}$ output open | | | 32 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 35 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 10 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 40 | pF |
| $C_{I(\overline{RAS})}$ | Input capacitance, $\overline{RAS}$ input | | | | | 50 | pF |
| $C_{I(\overline{CAS})}$ | Input capacitance, $\overline{CAS}$ input | | | | | 50 | pF |
| $C_{I(\overline{REF})}$ | Input capacitance, $\overline{REF}$ input | | | | | 50 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 15 | pF |

Note 2: Current flowing into an IC is positive; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted. See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | MH6404AD1-15 Limits Min | MH6404AD1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | ms |
| $t_{w(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | ns |
| $t_{w(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 150 | 10000 | ns |
| $t_{w(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 75 | ∞ | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL}=t_{TLH}=5ns$.
7: Reference levels of input signals are $V_{IH}$min and $V_{IL}$max. Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}$max limit insures that $t_{a(RAS)}$max can be met. $t_{d(RAS-CAS)}$max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)}min$.

## SWITCHING CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | MH6404AD1-15 Limits Min | MH6404AD1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max. Test conditions; Load=2T TL, $C_L$=100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load=2T TL, $C_L$=100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | MH6404AD1-15 Limits Min | MH6404AD1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | MH6404AD1-15 Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,\text{min} = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,\text{min} = t_{a(RAS)}\,\text{max} + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | MH6404AD1-15 Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{CPGR}$ | Page-mode read cycle time | $t_{PC}$ | 145 | | ns |
| $t_{CPGW}$ | Page-Mode write cycle time | $t_{PC}$ | 145 | | ns |
| $t_{CPGRW}$ | Page-Mode read-write cycle time | — | 180 | | ns |
| $t_{CPGRMW}$ | Page-Mode read-modify-write cycle time | — | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 60 | | ns |

## Automatic Refresh Cycle

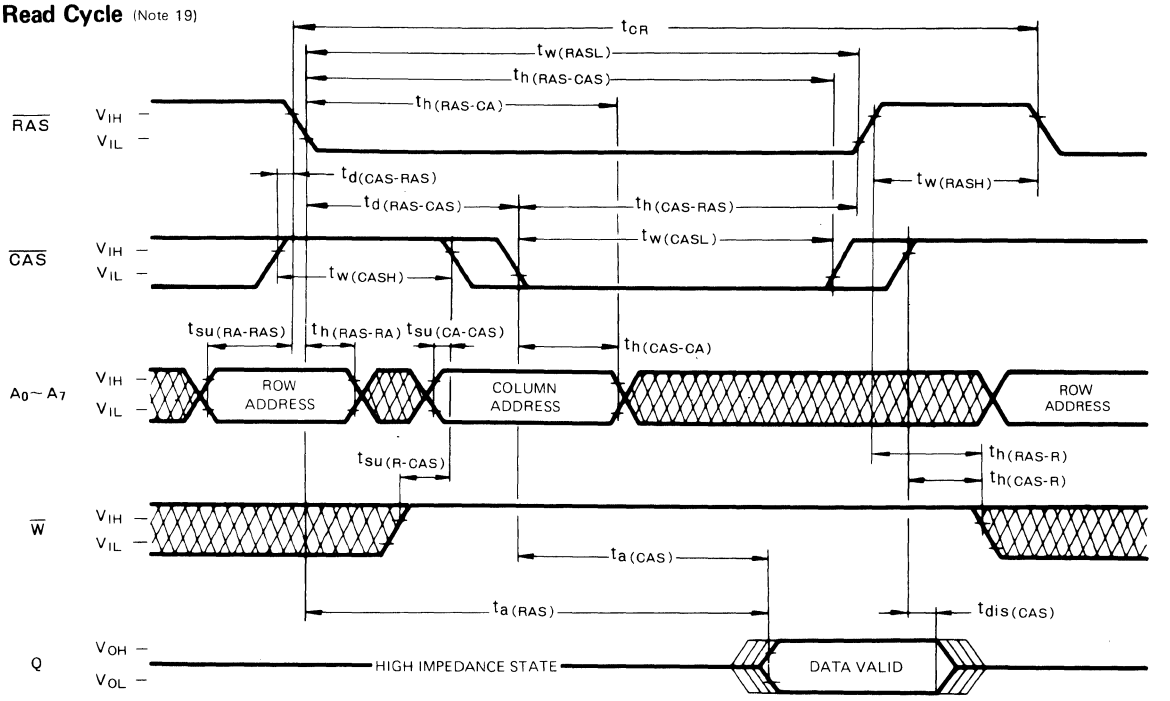
| Symbol | Parameter | Alternative Symbol | MH6404AD1-15 Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{C(REF)}$ | Automatic Refresh cycle time | $t_{FC}$ | 260 | | ns |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FP}$ | 60 | 8000 | ns |
| $t_{w(REFH)}$ | $\overline{REF}$ high pulse width | $t_{FI}$ | 30 | | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FSR}$ | 30 | | ns |
| $t_{su(REF-RAS)}$ | $\overline{REF}$ pulse setup time before $\overline{RAS}$ | $t_{FRD}$ | 295 | | ns |

## Self-Refresh Cycle

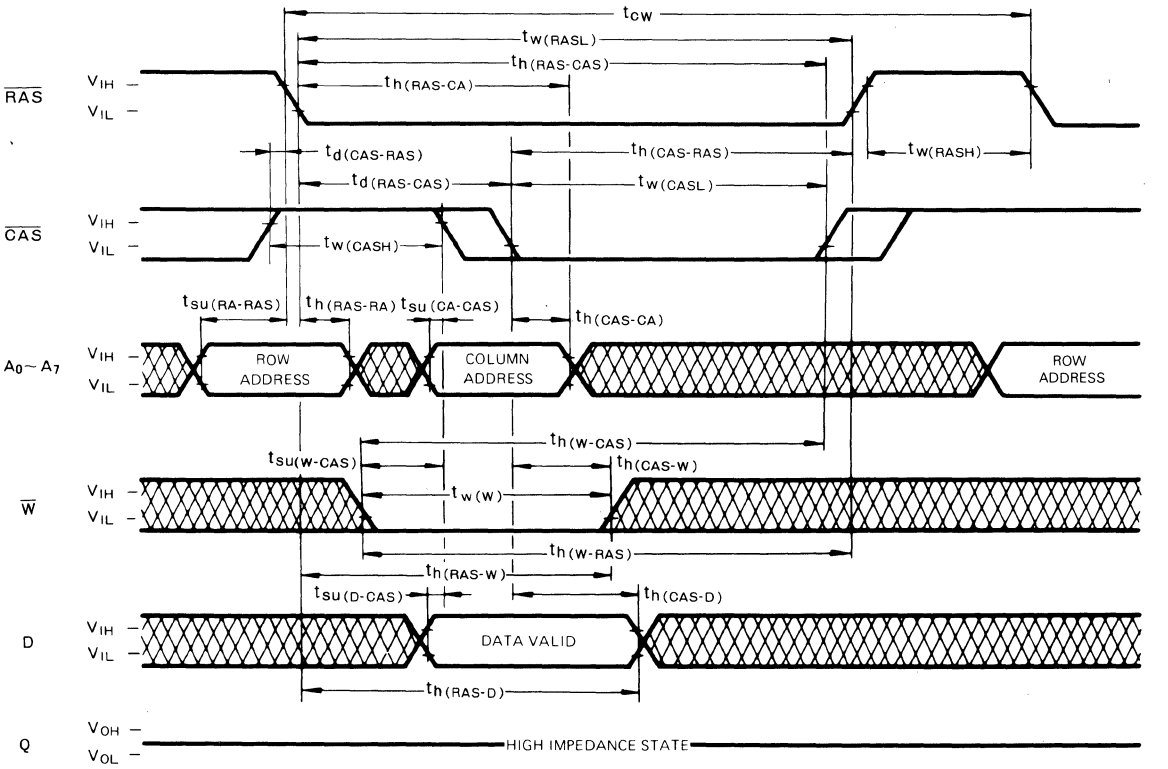
| Symbol | Parameter | Alternative Symbol | MH6404AD1-15 Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FBP}$ | 8000 | ∞ | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FBR}$ | 310 | | ns |

## TIMING DIAGRAMS (Note 18)

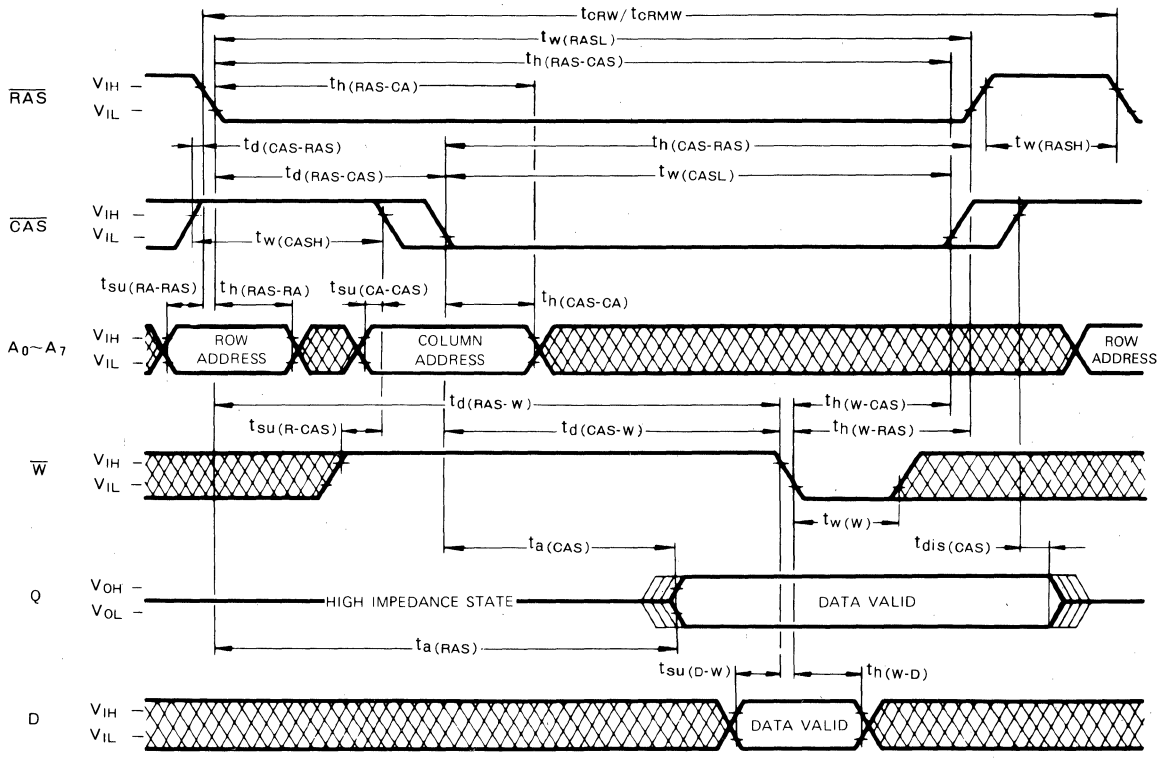
### Read Cycle (Note 19)



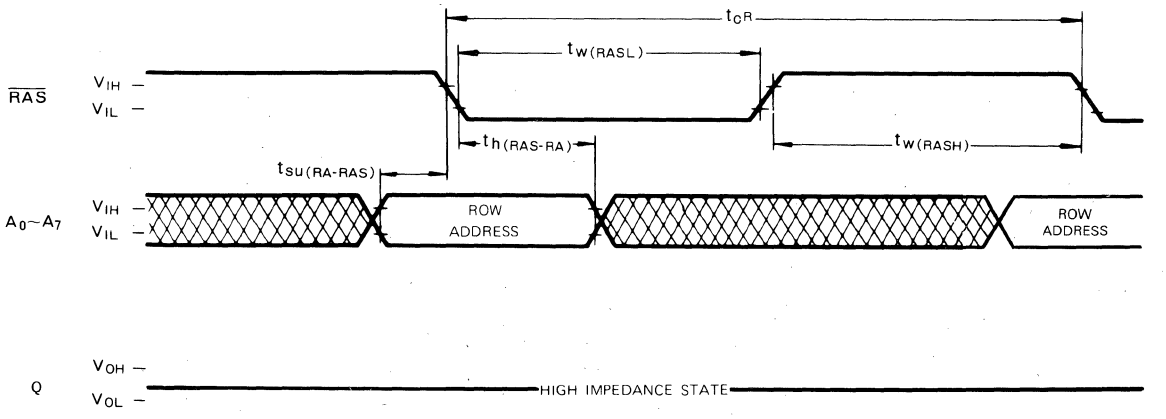

### Write Cycle (Early Write) (Note 19)



## Read-Write and Read-Modify-Write Cycles (Note 19)




## RAS-Only Refresh Cycle (Note 20)



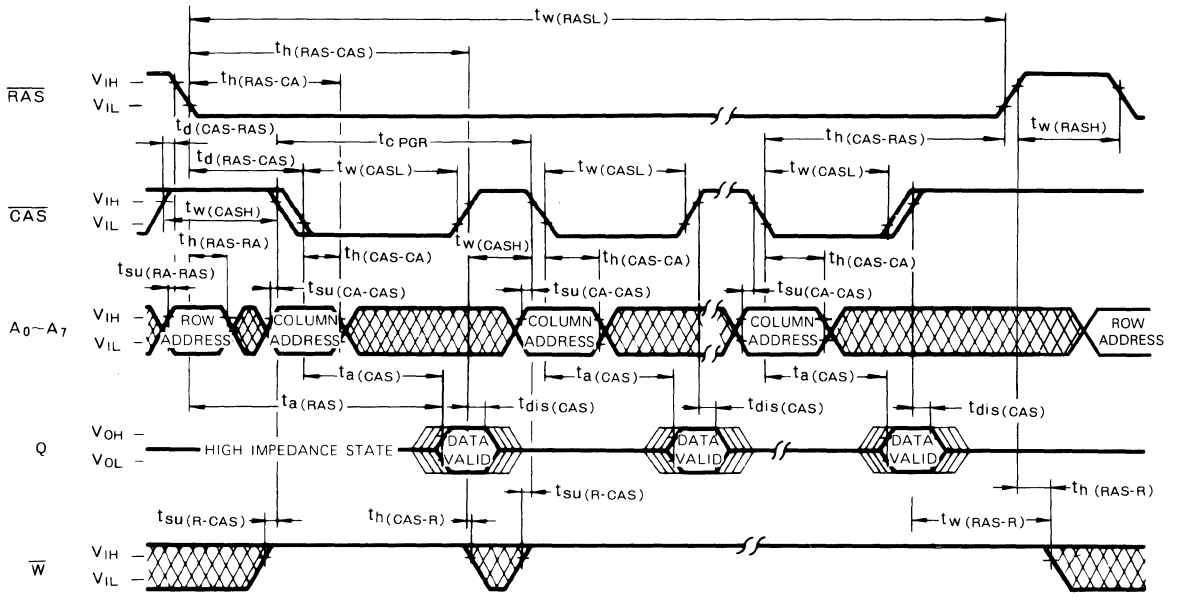

Note 18 — Indicates the don't care input

The center-line indicates the high-impedance state

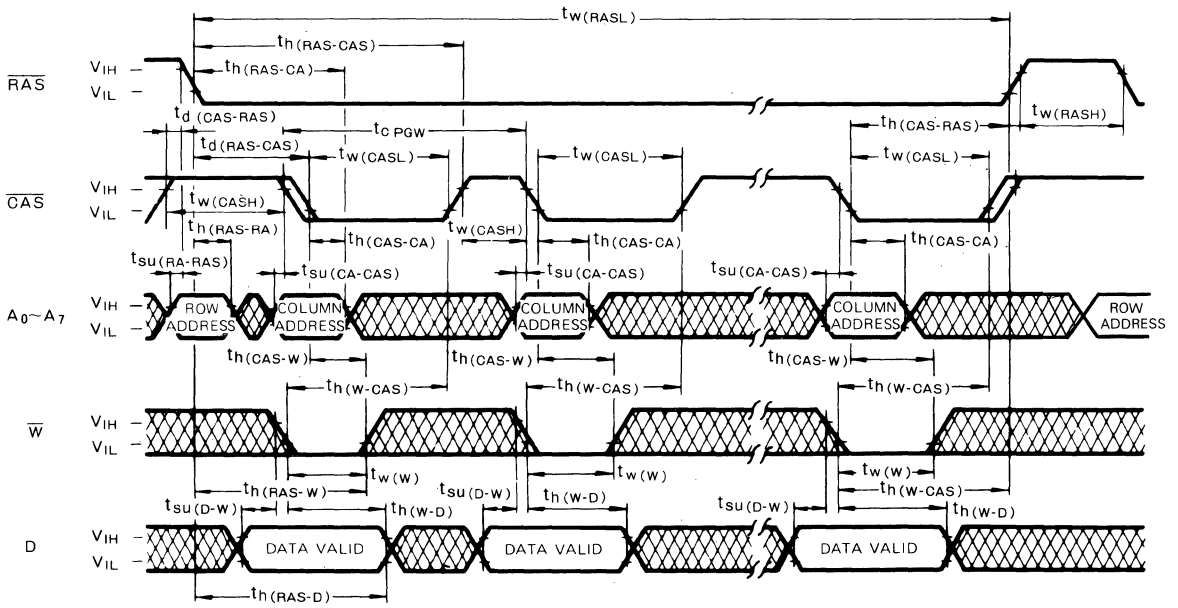
Note 19. $\overline{REF} = V_{IH}$

20. $\overline{CAS} = \overline{REF} = V_{IH}$, $\overline{W}$, D = don't care.
$A_7$ may be $V_{IH}$ or $V_{IL}$.

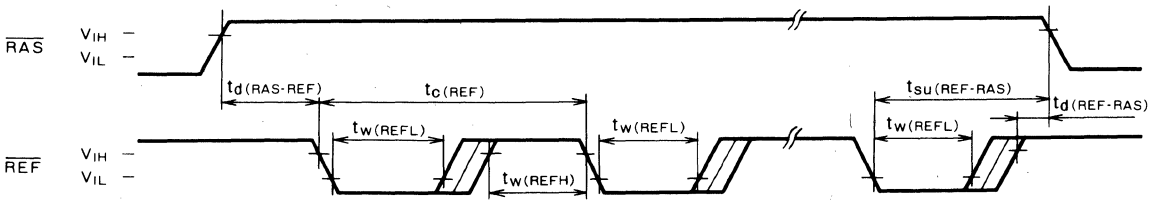
## Page-Mode Read Cycle (Note 19)



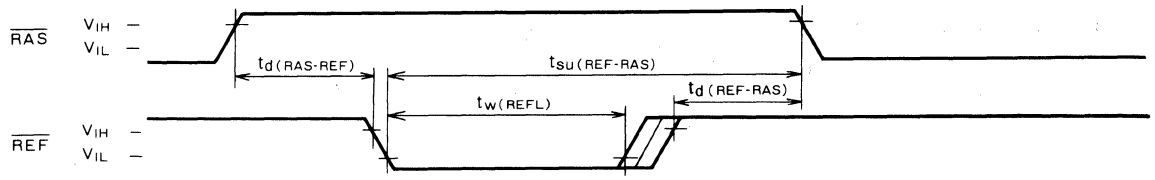

## Page-Mode Write Cycle (Note 19)



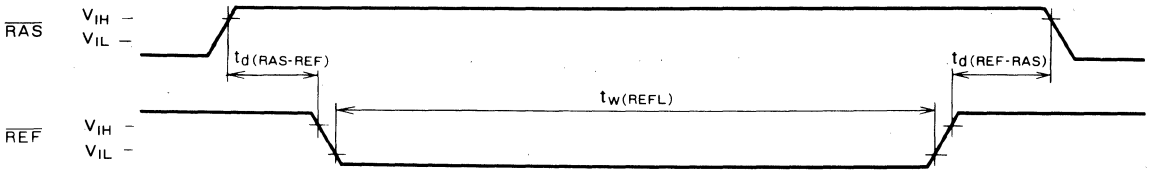
## Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 21)




## Automatic Pulse Refresh Cycle (Single Pulse) (Note 21)

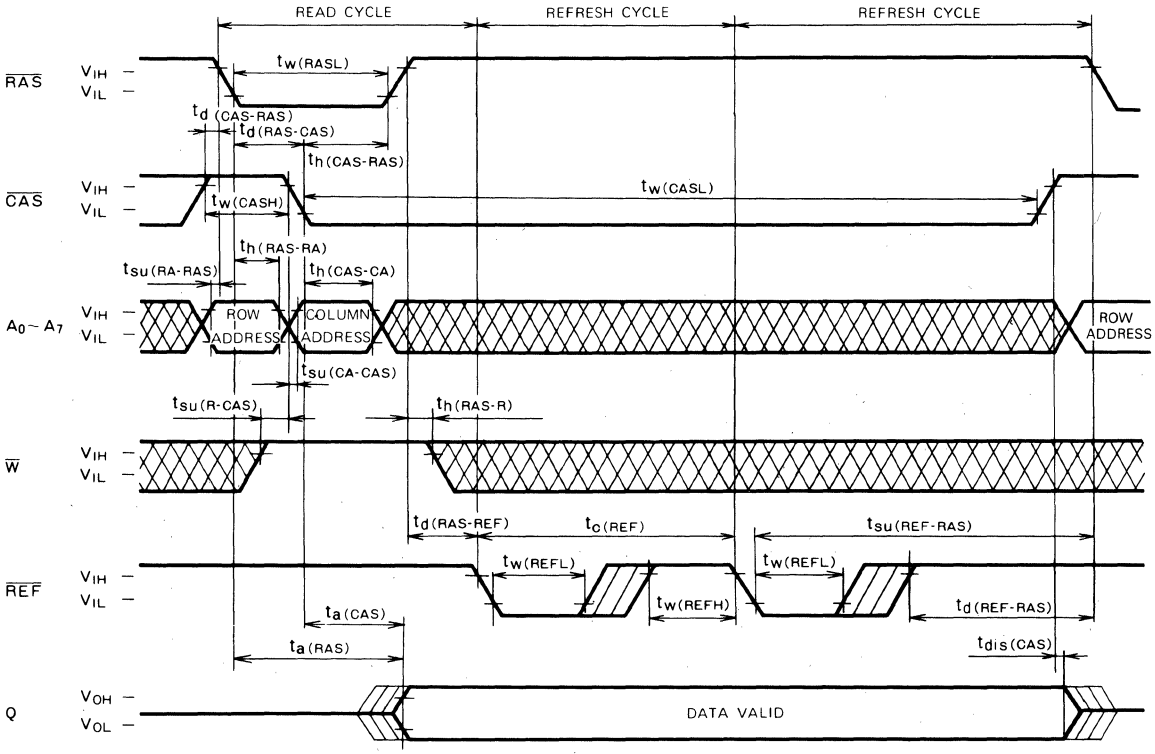



## Self-Refresh Cycle (Note 21)

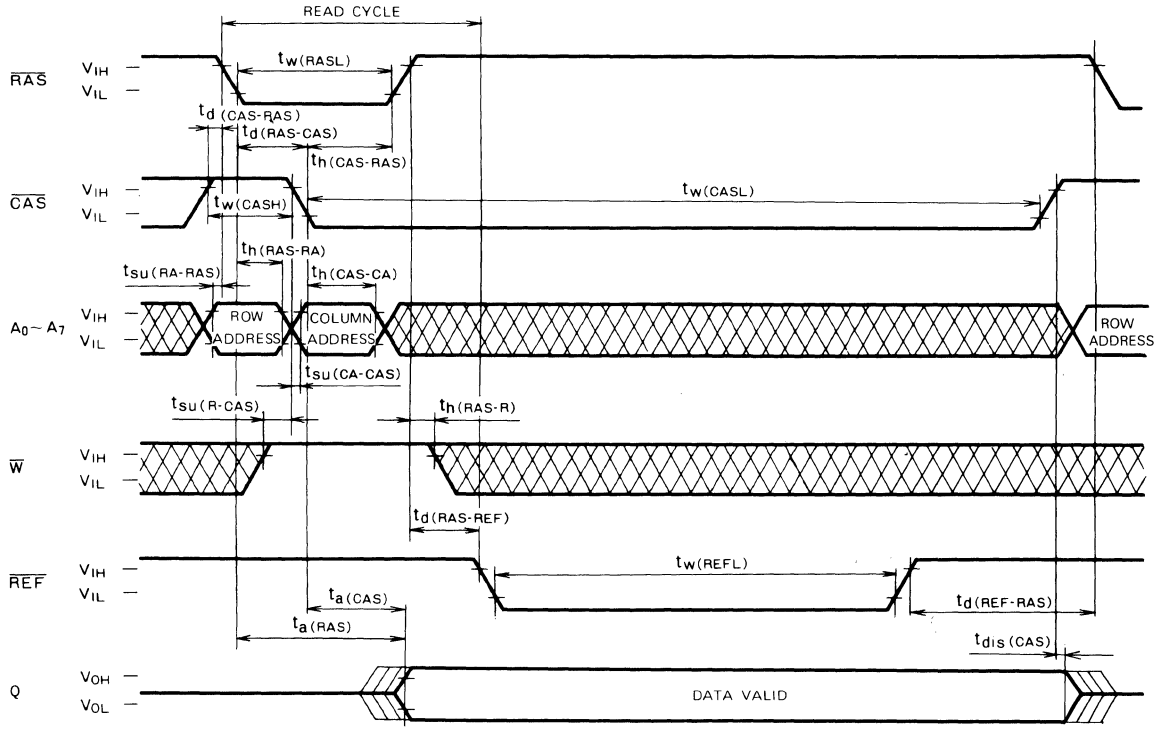



(Note 21) $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

## Hidden Automatic Pulse Refresh Cycle

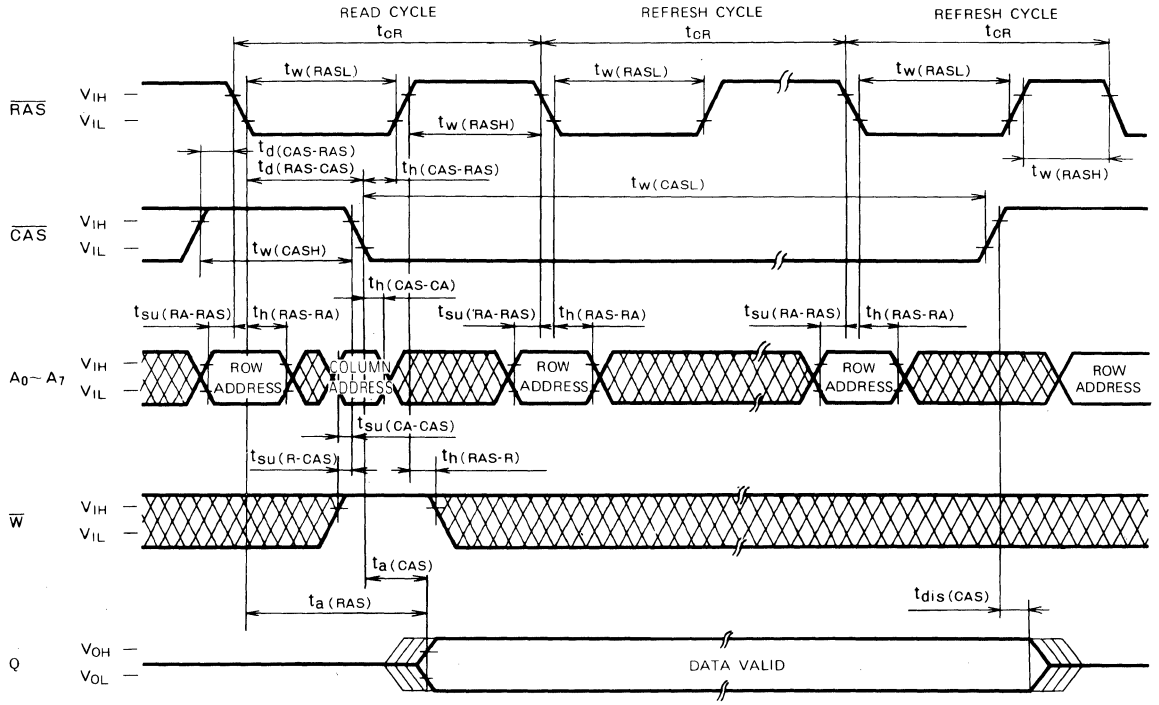


## Hidden Self-Refresh Cycle (Note 22)

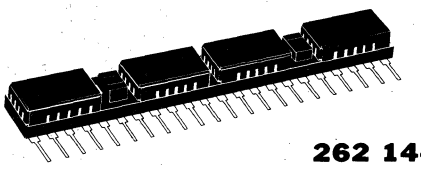



Note 22: If the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect).

## Hidden Refresh Cycle (Note 19)



# MH6404AND1-15



## 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

## DESCRIPTION

The MH6404AND1 is 65 536-word x 4 bit dynamic RAM and consists of four industry standard 64K x 1 dynamic RAMs in leadless chip carrier.
The mounting of leadless chip carriers on a ceramic single in-line package provides any application where high densities and large quantities of memory are required.

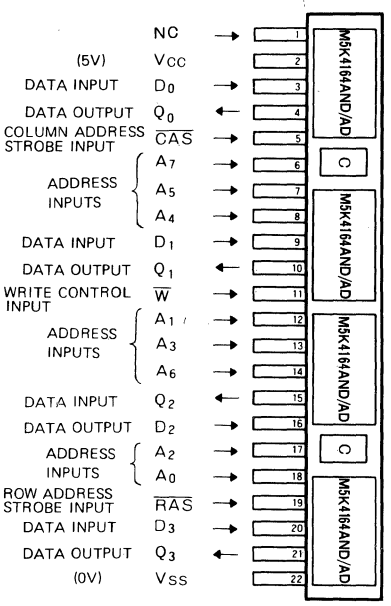
## FEATURES

- High speed

| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| MH6404AND1-15 | 150 | 260 | 600 |

- Utilizes industry standard 64K RAMs in leadless chip carriers
- 22 pin Single In-line Package
- Single +5V (±10%) supply operation
- Low stand by power dissipation . . . . . 88 mW (max)
- Low operating power dissipation:
  MH6404AND1-15 990mW (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22$\mu$F x 2) decoupling capacitors
- 128 refresh cycles (every 2ms) $A_7$ Pin is not need for refresh

## PIN CONFIGURATION (TOP VIEW)

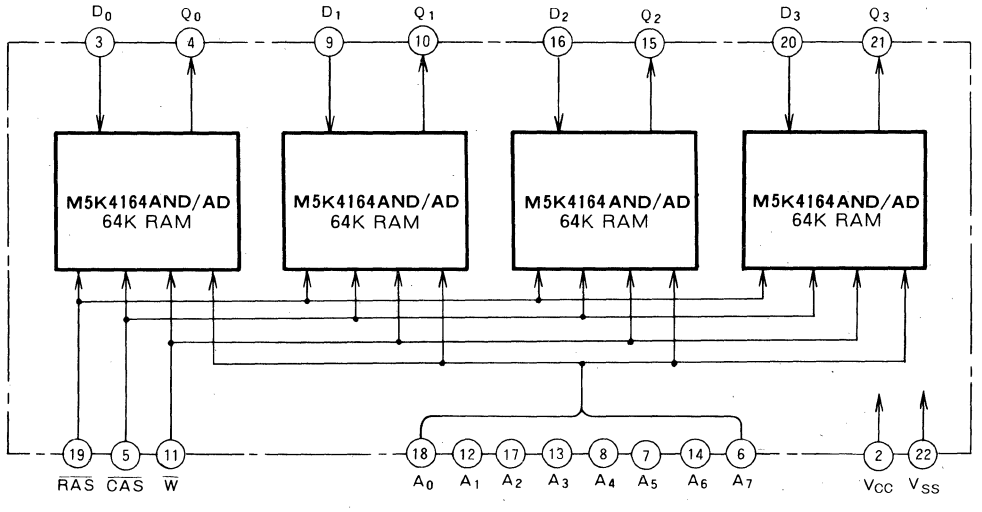



**Outline 22S5**

## APPLICATION

- Main memory unit for computers
- Refresh memory for CRT

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

### FUNCTION

The MH6404AND1 provides, in addition to normal read, write, and read-modify-write operations a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open.

### SUMMARY OR OPERATIONS

#### Addressing

To select 4 of the 262144 memory cells in the MH6404AND1 the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externaly-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

#### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for set-up and hold times.

#### Data Output Control

The outputs of the MH6404AND1 is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the date output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data.. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The outputs will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the MH6404AND1, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, inputs and outputs can be connected directly to give a common I/O data bus.

**2. Data Output Hold**

The data outputs can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0$~$A_6$) of the MH6404AND1 must be refreshed every 2 ms to maintain data. The methods of refreshing for the MH6404AND1 are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A features of the MH6404AND1 is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period. executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In may applications this eliminates the need for off-chiip latches.

## Power Dissipation

Most of the circuitry in the MH6404AND1 is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH6404AND1 as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The MH6404AND1 operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## 262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25℃ | 4000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | ℃ |
| Tstg | Storage temperature range | | −55～150 | ℃ |
| Tsld | Soldering temperature time | | 260・10 | ℃・sec |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Qfloating 0V≦$V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −40 | | 40 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note3, 4) | MH6404AND1-15 | $\overline{RAS}$, $\overline{CAS}$ cycling<br>$t_{CR}$＝$t_{CW}$＝min, output open | | | 180 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 16 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | MH6404AND1-15 | $\overline{RAS}$ cycling, $\overline{CAS}$＝$V_{IH}$<br>$t_{C(\overline{REF})}$＝min, output open | | | 140 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note3, 4) | MH6404AND1-15 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling<br>$t_{CPG}$＝min, output open | | | 140 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$<br>f＝1MHz<br>$V_i$＝25mVrms | | | 35 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 10 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 40 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 50 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 50 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 15 | pF |

Note 2: Current flowing into an IC is positive; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | MH6404AND1-15 Limits Min | MH6404AND1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 150 | 1000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | ns |

Note 5: An initial pause of 500$\mu s$ is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH}$ min and $V_{IL}$ max. Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\text{min} = t_{h(RAS-RA)}\text{min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)}\text{min}$.

## SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | MH6404AND1-15 Limits Min | MH6404AND1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{cR}$ | Read cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2T TL, $C_L$ = 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | MH6404AND1-15 Limits Min | MH6404AND1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{cW}$ | Write cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | − 5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | MH6404AND1-15 Limits Min | MH6404AND1-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 15: $t_{CRW}$ min is defined as $t_{CRW}\,\text{min} = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(t_{THL})}$

16: $t_{CRMW}$ min is defined as $t_{CRMW}\,\text{min} = t_{a(RAS)}\,\text{max} + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(t_{THL})}$

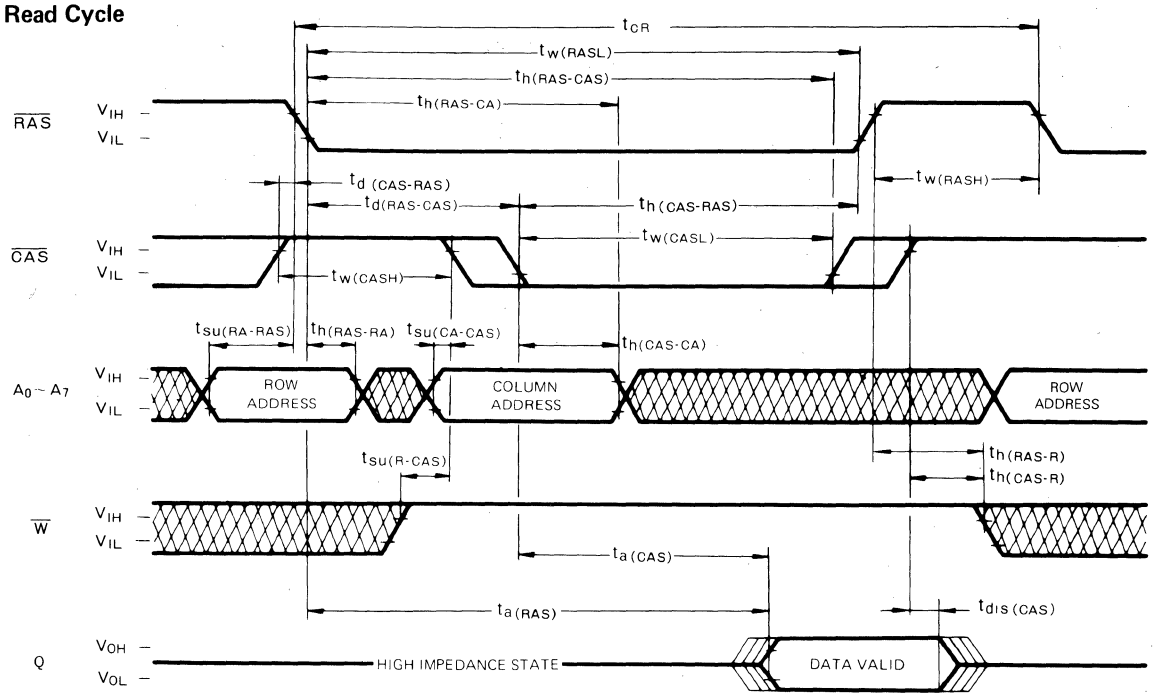
17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,\text{min}$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,\text{min}$ and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,\text{min}$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

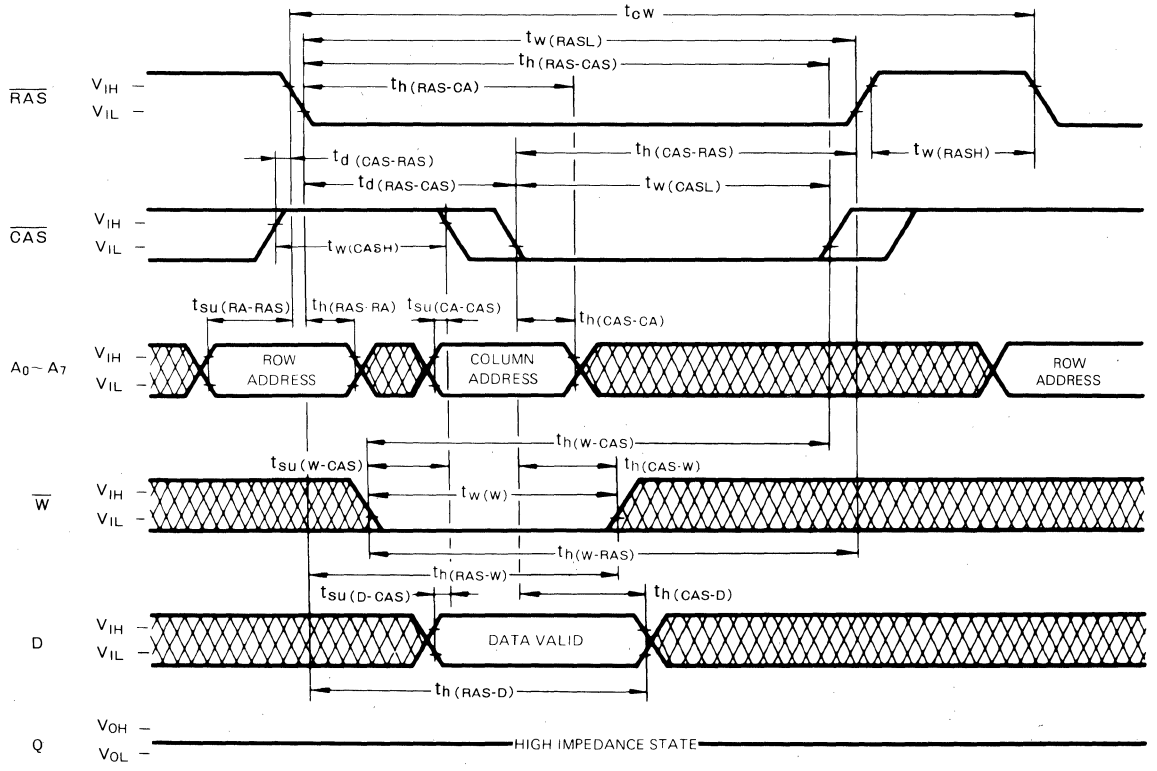
| Symbol | Parameter | Alternative Symbol | MH6404AND1-15 Limits Min | MH6404AND1-15 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{CPGR}$ | Page-mode read cycle time | $t_{PC}$ | 145 | | ns |
| $t_{CPGW}$ | Page-Mode write cycle | $t_{PC}$ | 145 | | ns |
| $t_{CPGRW}$ | Page-Mode read-write cycle time | — | 180 | | ns |
| $t_{CPGRMW}$ | Page-Mode read-modify-write cycle time | — | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 60 | | ns |

## TIMING DIAGRAMS (Note 18)

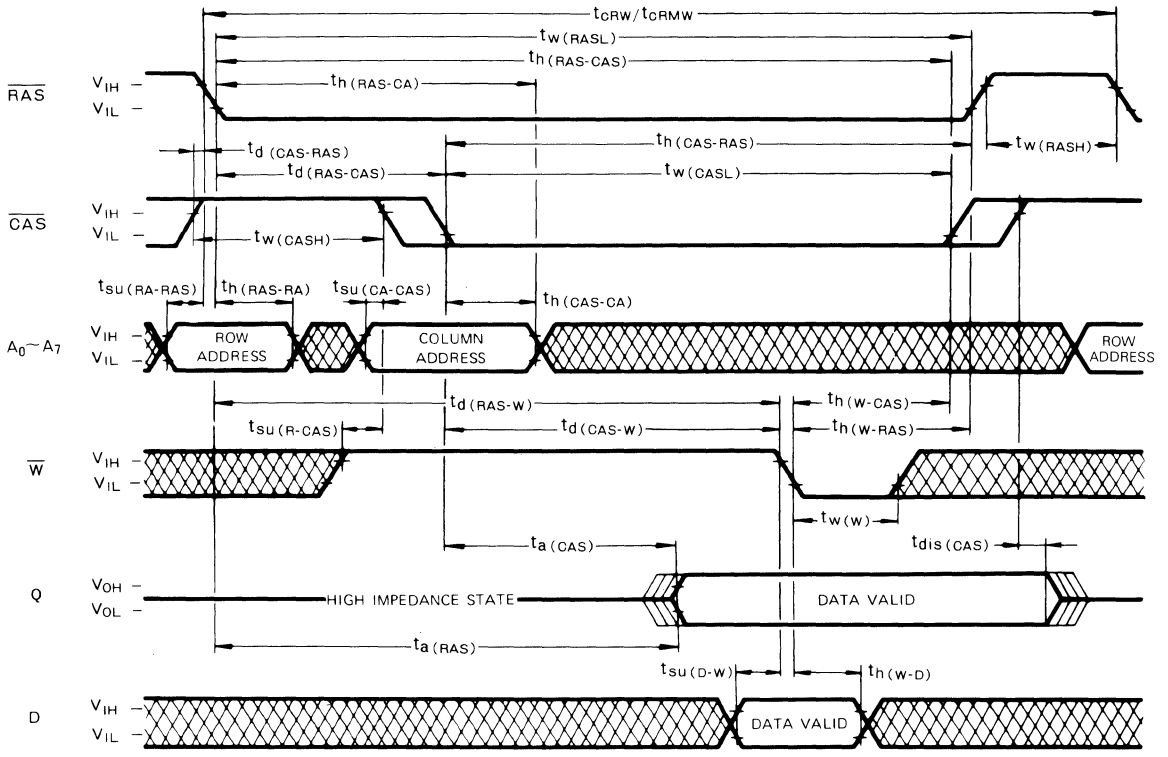
### Read Cycle



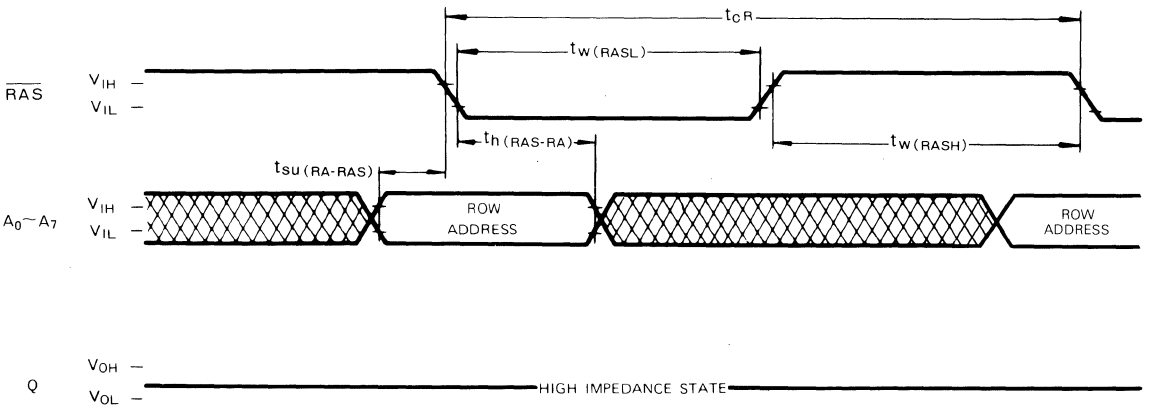

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)

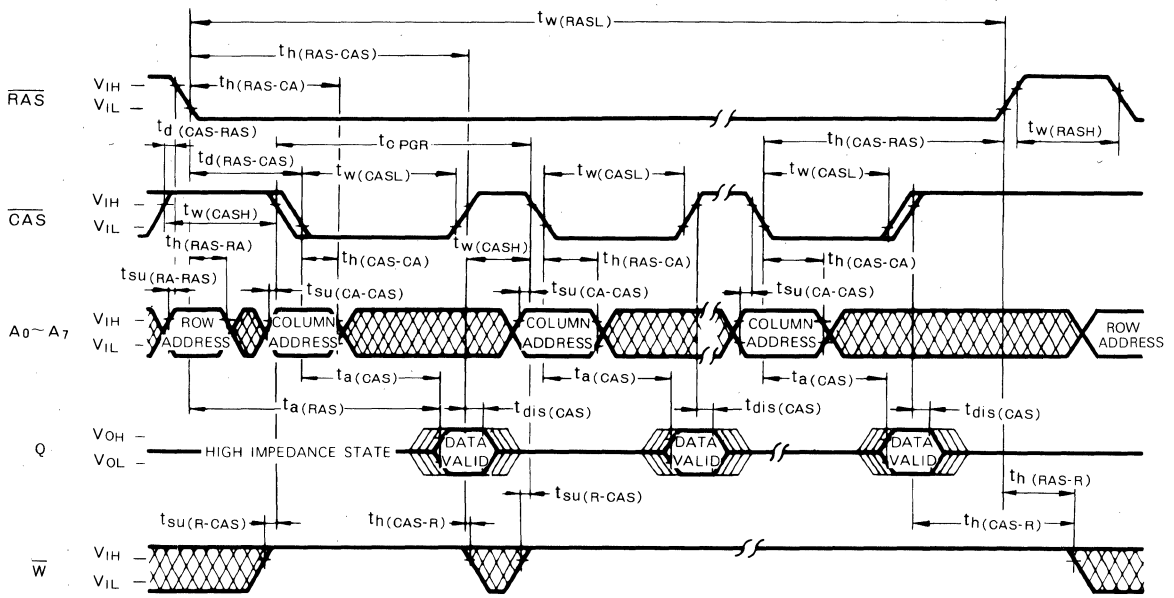



Note 18 Indicates the don't care input

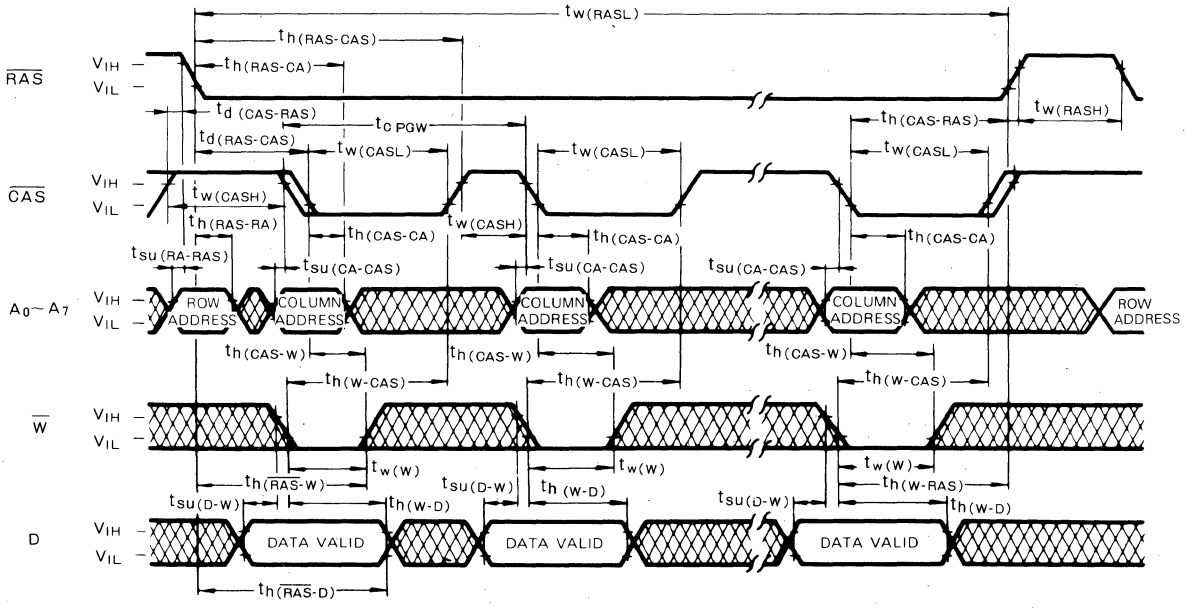
The center-line indicates the high-impedance state

Note 19. $\overline{CAS} = V_{IH}$, $\overline{W}$, D = don't care.
$A_7$ may be $V_{IH}$ or $V_{IL}$.

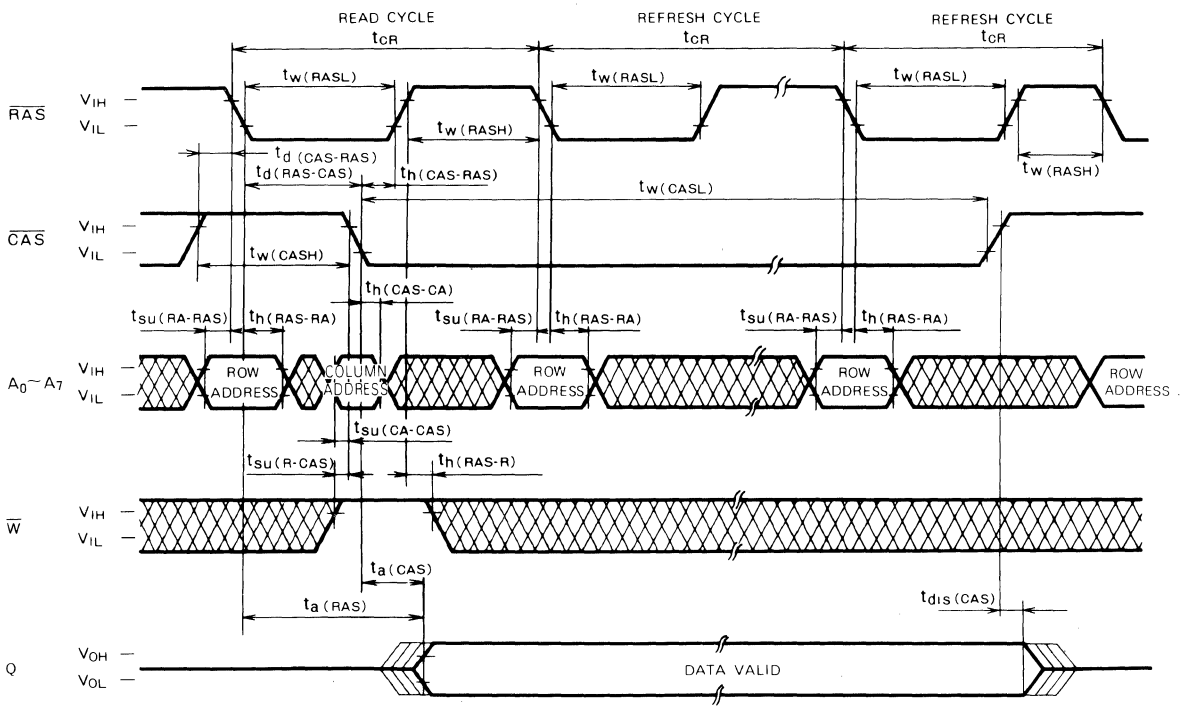
## Page-Mode Read Cycle




## Page-Mode Write Cycle

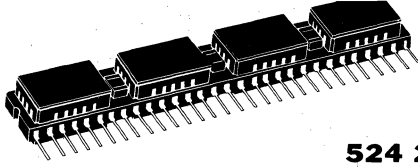


## Hidden Refresh Cycle



# MH6408AD-15

## 524 288-BIT(65 536-WORD BY 8-BIT)DYNAMIC RAM



## DESCRIPTION

The MH6408AD is 65536 word x 8 bit dynamic RAM and consists of eight industry standard 64K x 1 dynamic RAMs in leadless chip carrier.

The mounting of leadless chip carriers on a ceramic single in-line package provides any application where high densities and large quantities of memory are required.

## FEATURES

- Performance ranges

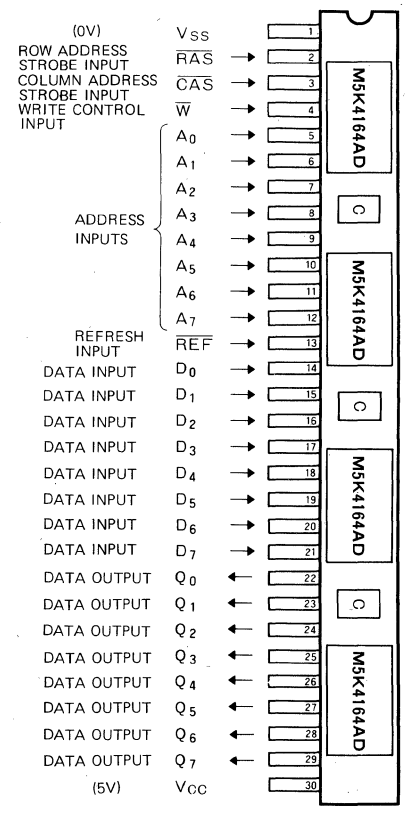
| Part No. | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| MH6408AD-15 | 150 | 260 | 1200 |

- Utilizes industry standard 64K RAMs in leadless chip carriers
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 176mW(max)
- Low operating power dissipation:
  MH6408AD-15 1.9W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22$\mu$F x 6) decoupling capacitors
- 128 refresh cycles (every 2ms) $A_7$ Pin is not need for refresh
- Pin 13 controls automatic - and self-refresh mode.

## APPLICATION

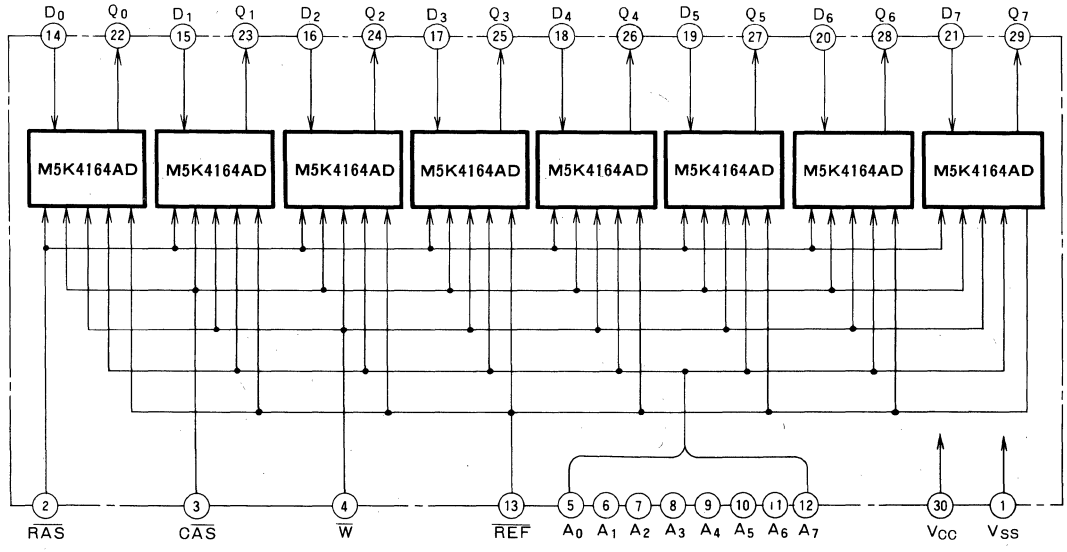
- Main memory unit for computers
- Refresh memory

## PIN DONFIGURATION (TOP VIEW)




**Outline 30S5**

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 524 288-BIT(65 536-WORD BY 8-BIT)DYNAMIC RAM

## FUNCTION

The MH6408AD provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown iin Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | $\overline{REF}$ | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | NAC | VLD | YES | Page mode identical except refresh is NO |
| Write | ACT | ACT | ACT | VLD | APD | APD | NAC | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | NAC | VLD | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | DNC | APD | DNC | NAC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | NAC | VLD | YES | |
| Automatic refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Self refresh | NAC | DNC | DNC | DNC | DNC | DNC | ACT | OPN | YES | |
| Hidden automatic refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Hidden self refresh | NAC | ACT | DNC | DNC | DNC | DNC | ACT | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | NAC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

## SUMMARY OF OPERATIONS

### Addressing

To select 8 of the 524288 memory cells in the MH6408AD the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Date to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the W input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for serup and hold times.

### Data Output Control

The outputs of the MH6408AD are in the high-impedance state when $\overline{CAS}$ is high. When the are memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the outputs entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The outputs will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the MH6408AD, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, inputs and outputs can be connected directly to give a common I/O data bus.

**2. Data Output Hold**

The data outputs can be held between read cycles, without lengthening the cycle time. This enebles extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the MH6408AD must be refreshed every 2 ms to maintain data. The methods of refreshing for the MH6408AD are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Automatic Refresh**

Pin 13 ($\overline{REF}$) has two special functions. The MH6408AD has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is aapplied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

**4. Self-Refresh**

The other function of pin 13 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the MH6408AD will refresh itself. This internal sequence repeats asynchronously every 12 to 16$\mu$s. After 2ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 13 ($\overline{REF}$) refresh function gives the user a feature that if free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx$3M$\Omega$) on pin 13, so if the pin 13($\overline{REF}$) function is not used, pin 1 may be left open (not connect) without affecting the normal operations.

**5. Hidden Refresh**

A features of the MH6408AD is that refresh cycle may be performed while maintaining valid data at the output pins by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuirty in the MH6408AD is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH6408AD as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The MH6408AD operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

## 524 288-BIT(65 536-WORD BY 8-BIT)DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 8000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −55～150 | °C |
| $T_{sid}$ | Soldering temperature･time | | 260・10 | ℃・sec |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V ± 10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝2.1mA | 0 | | 0.45 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −80 | | 80 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −80 | | 80 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | MH6408AD-15 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$＝$t_{CW}$＝min, output open | | | 360 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 32 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | MH6408AD-15 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ $t_{C(REF)}$＝min, output open | | | 280 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | MH6408AD-15 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$＝min, output open | | | 280 | mA |
| $I_{CC5(AV)}$ | Average supply current from $V_{CC}$, automatic refreshing (Note 3) | MH6408AD-15 | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$ cycling $t_{C(REF)}$＝min, output open | | | 280 | mA |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$, self refreshing | | $\overline{RAS}$＝$V_{IH}$, $\overline{REF}$＝$V_{IL}$ output open | | | 64 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_I$＝25mVrms | | | 70 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 30 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 80 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 100 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 100 | pF |
| $C_{I(REF)}$ | Input capacitance, $\overline{REF}$ input | | | | | 100 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_I$＝25mVrms | | | 30 | pF |

Note 2. Current flowing into an IC is positive; out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 30 | 100 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | ns |

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$)
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$
Note 13. This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2T TL, $C_L$ = 100pF
Note 14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{cw}$ | Write cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | 5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{cRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 280 | | ns |
| $t_{cRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 15. $t_{cRW}$ min is defined as $t_{cRW}\,\text{min} = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. $t_{cRMW}$ min is defined as $t_{cRMW}\,\text{min} = t_{a(RAS)}\,\text{max} + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

| Symbol | Parameter | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{cPGR}$ | Page-mode read cycle time | $t_{PC}$ | 145 | | ns |
| $t_{cPGW}$ | Page-Mode write cycle time | $t_{PC}$ | 145 | | ns |
| $t_{cPGRW}$ | Page-Mode read-write cycle time | — | 180 | | ns |
| $t_{cPGRMW}$ | Page-Mode read-modify-write cycle time | — | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 60 | | ns |

## Automatic Refresh Cycle

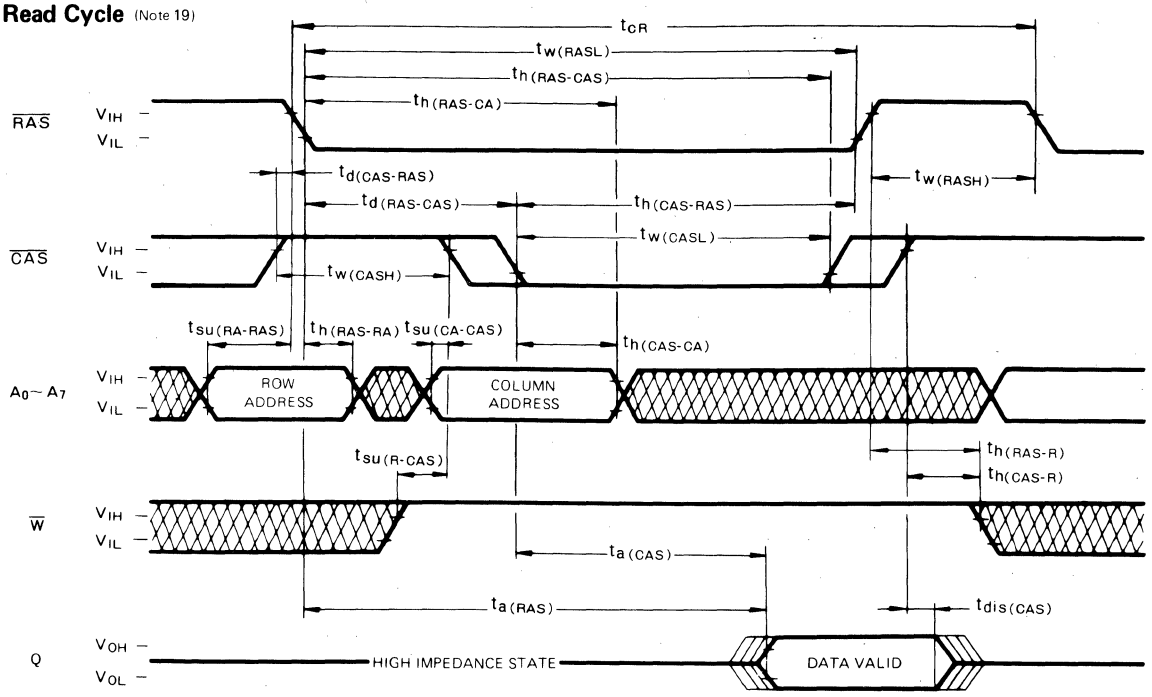
| Symbol | Parameter | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{c(REF)}$ | Automatic Refresh cycle time | $t_{FC}$ | 260 | | ns |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FP}$ | 60 | 8000 | ns |
| $t_{w(REFH)}$ | $\overline{REF}$ high pulse width | $t_{FI}$ | 30 | | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FSR}$ | 30 | | ns |
| $t_{su(REF-RAS)}$ | $\overline{REF}$ pulse setup time before $\overline{RAS}$ | $t_{FRD}$ | 295 | | ns |

## Self-Refresh Cycle

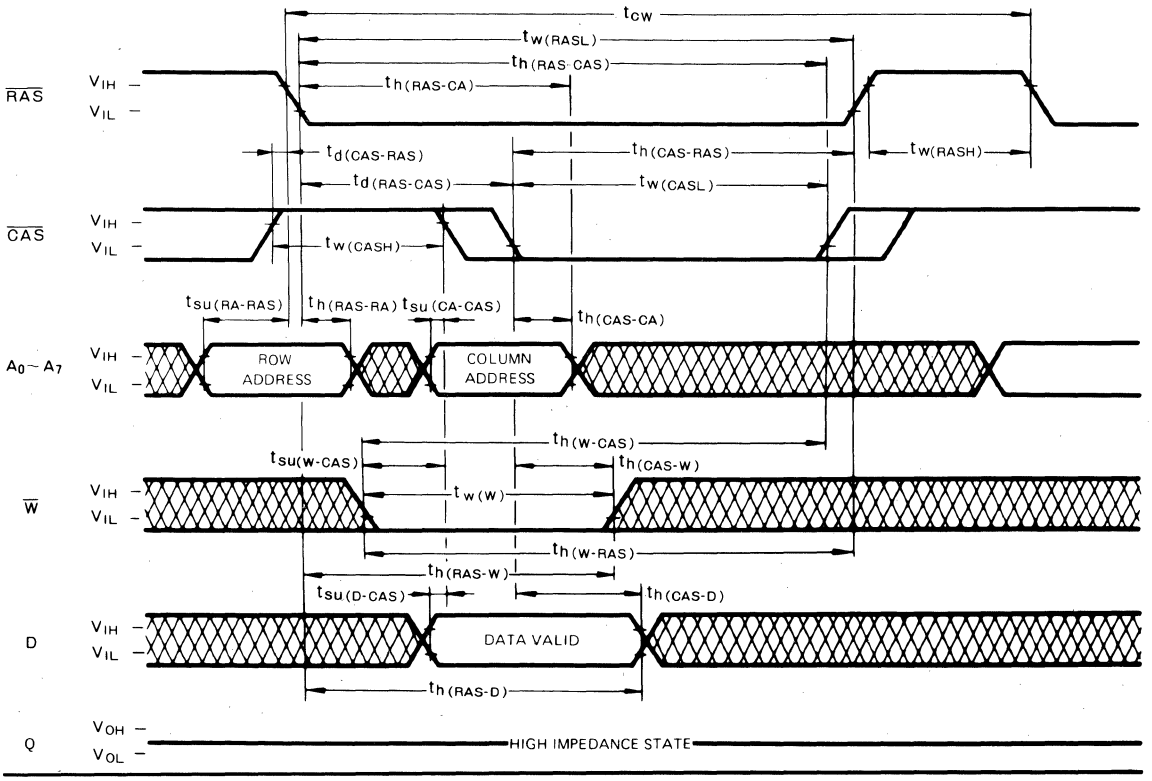
| Symbol | Parameter | Alternative Symbol | MH6408AD-15 Limits Min | MH6408AD-15 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FBP}$ | 8000 | ∞ | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FBR}$ | 295 | | ns |

## TIMING DIAGRAMS (Note 18)

### Read Cycle (Note 19)



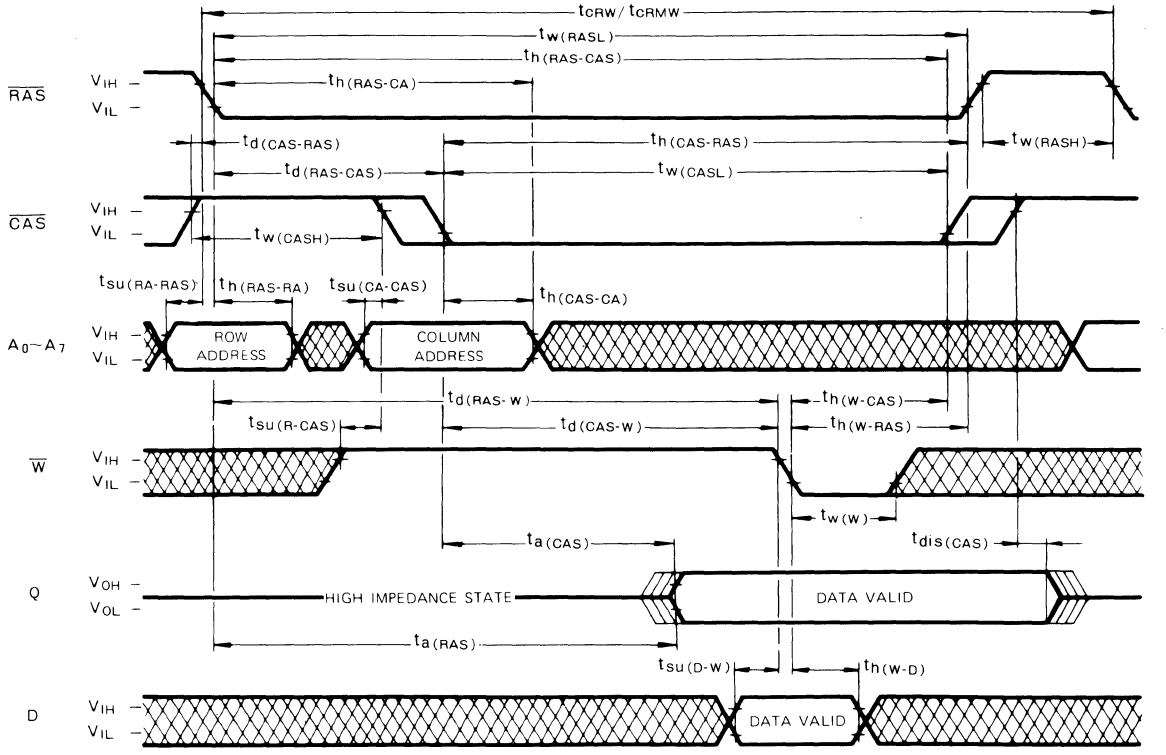

### Write Cycle (Early Write) (Note 19)



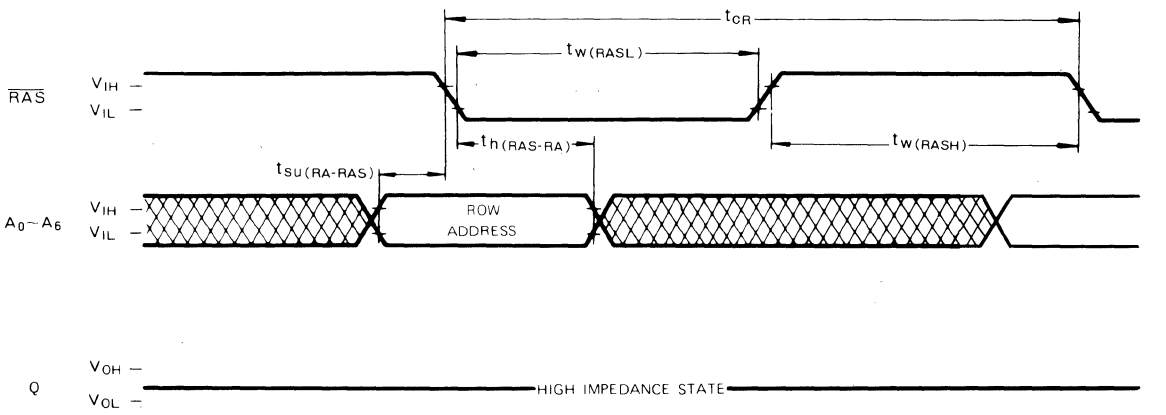



MITSUBISHI ELECTRIC

## Read-Write and Read-Modify-Write Cycles (Note 19)




## RAS-Only Refresh Cycle (Note 20)



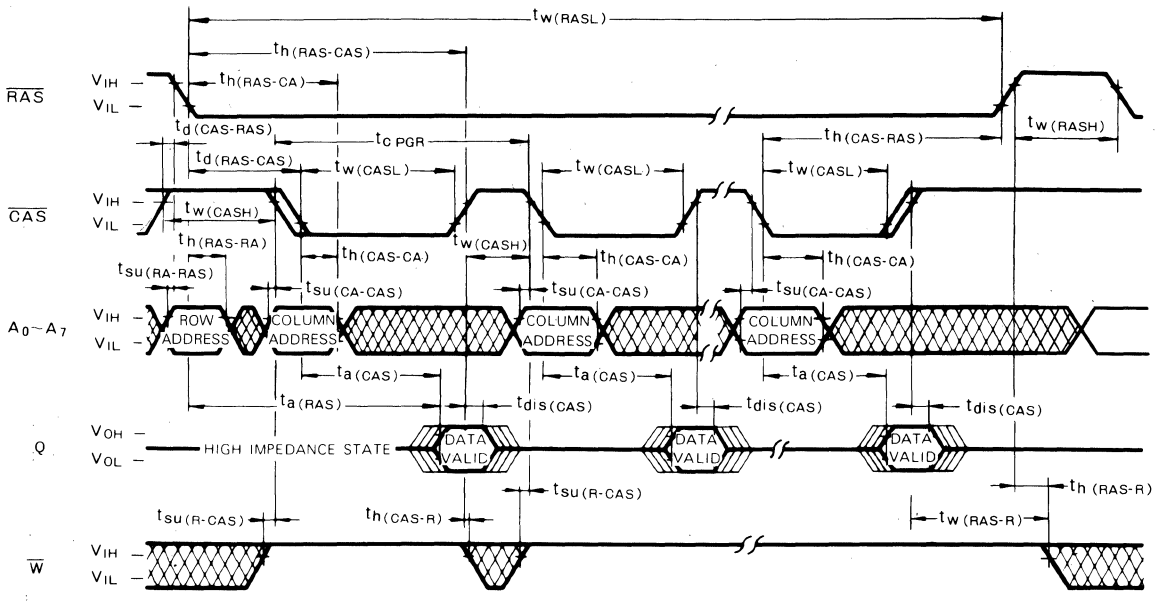

Note 18 Indicates the don't care input

The center-line indicates the high-impedance state

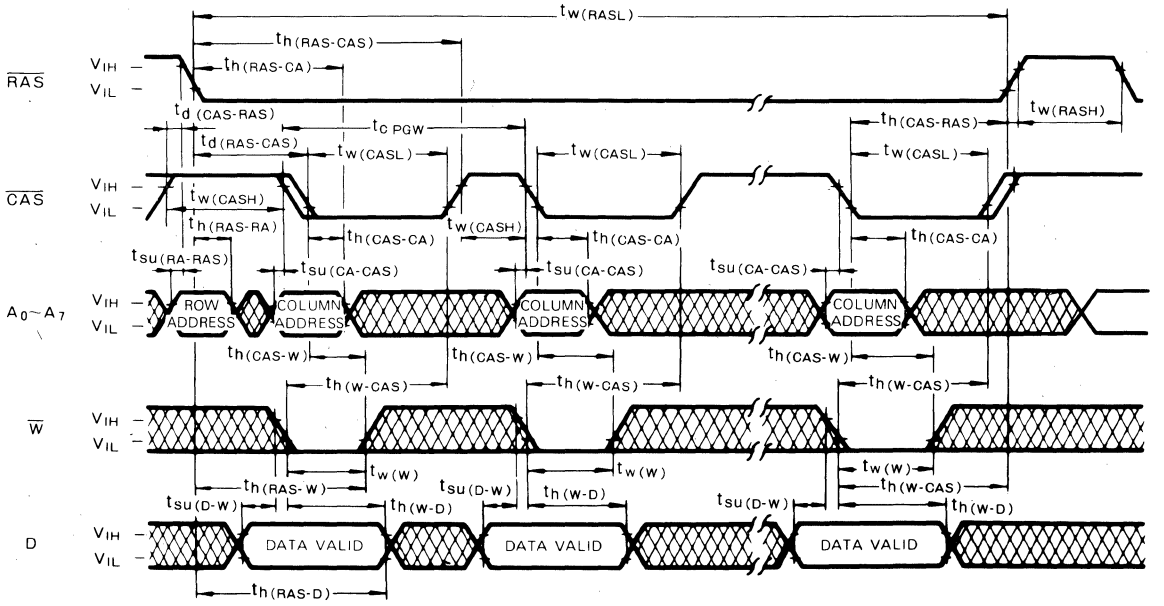
Note 19. $\overline{REF} = V_{IH}$

20. $\overline{CAS} = \overline{REF} = V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

## Page-Mode Read Cycle (Note 19)




## Page-Mode Write Cycle (Note 19)





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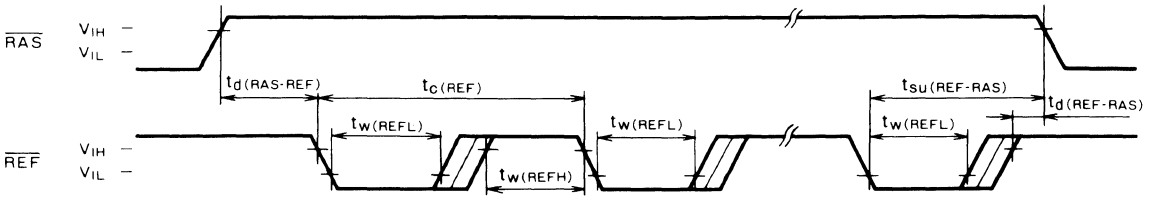
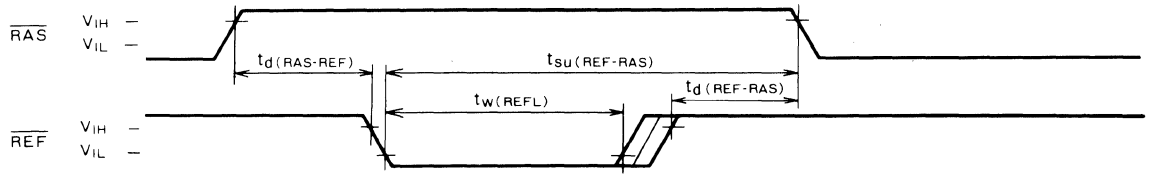
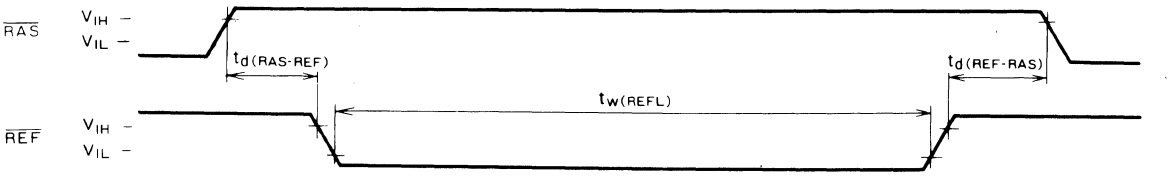
## Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 21)




## Automatic Pulse Refresh Cycle (Single Pulse) (Note 21)

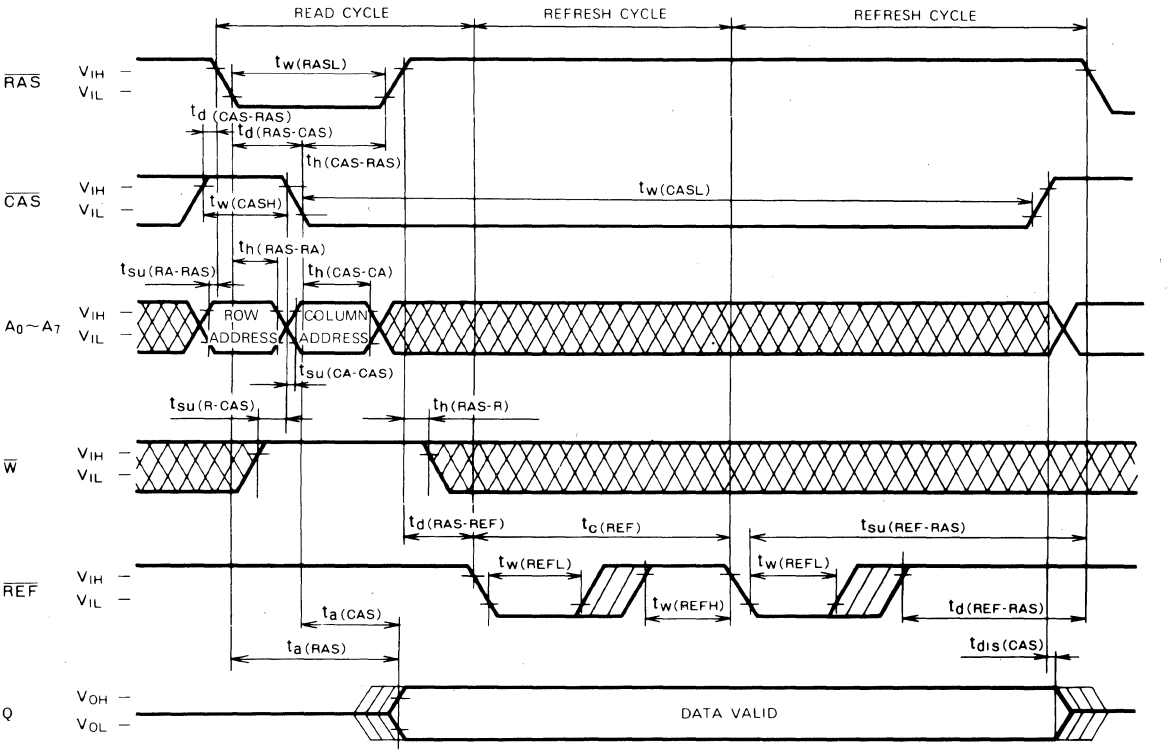



## Self-Refresh Cycle (Note 21)

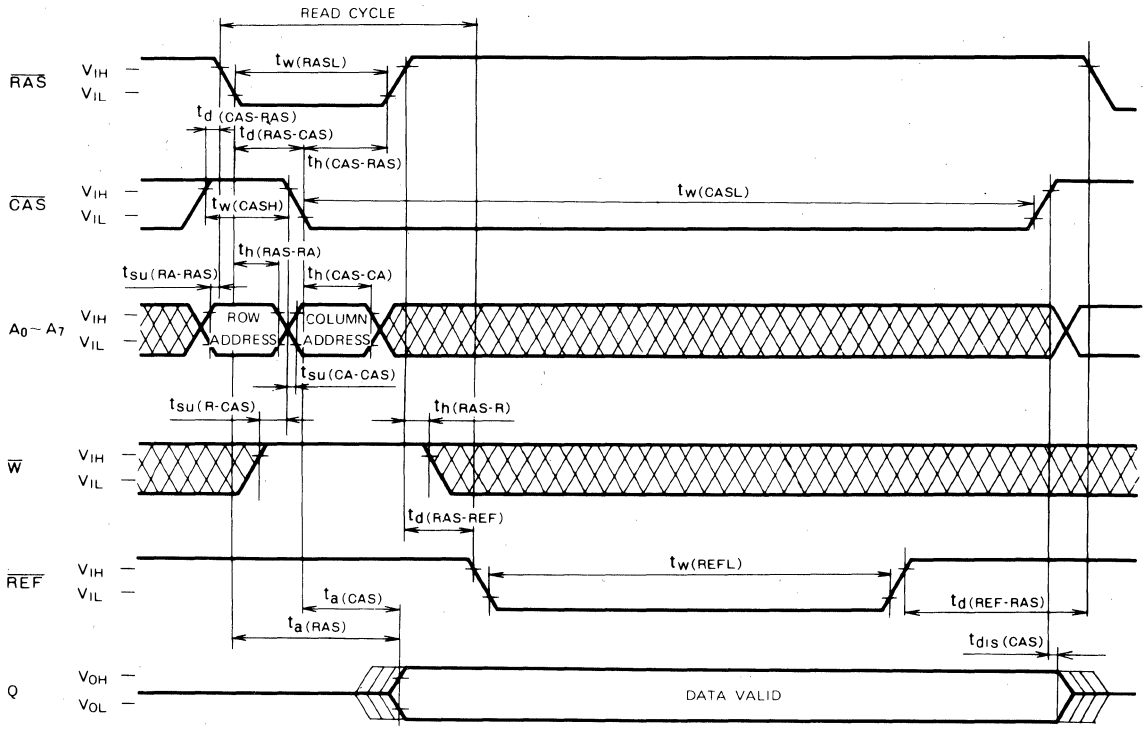



Note 21. $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

## Hidden Automatic Pulse Refresh Cycle

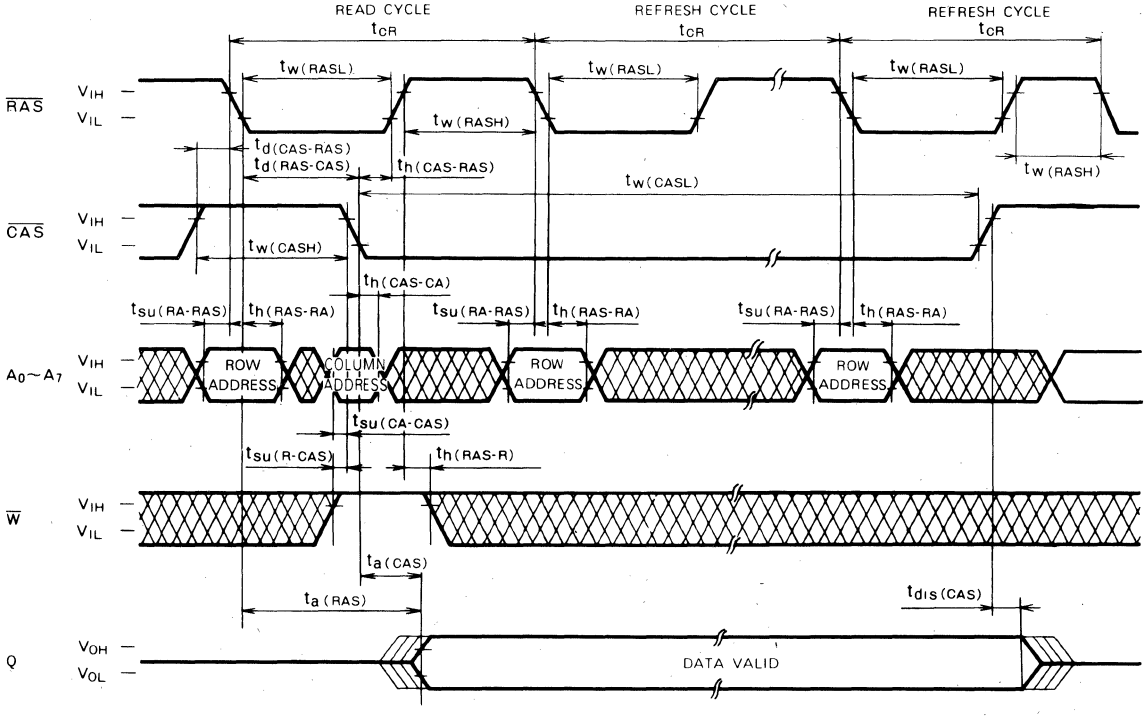


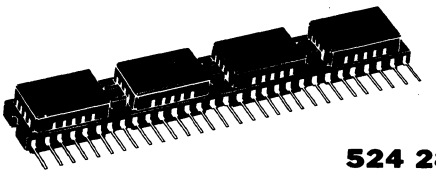
## Hidden Self-Refresh Cycle (Note 22)




Note 22. If the pin 13 ($\overline{REF}$) function is not used, pin 13 may be left open (not connect).

## Hidden Refresh Cycle (Note 19)







# MH6408AND-15

## 524 288-BIT(65 536-WORD BY 8-BIT)DYNAMIC RAM

## DESCRIPTION

The MH6408AND is 65536 word x 8 bit dynamic RAM and consists of eight industry standard 64K x 1 dynamic RAMs in leadless chip carrier.

The mounting of leadless chip carriers on a ceramic single in-line package provides any application where high densities and large quantities of memory are required.

## FEATURES

- Performance ranges

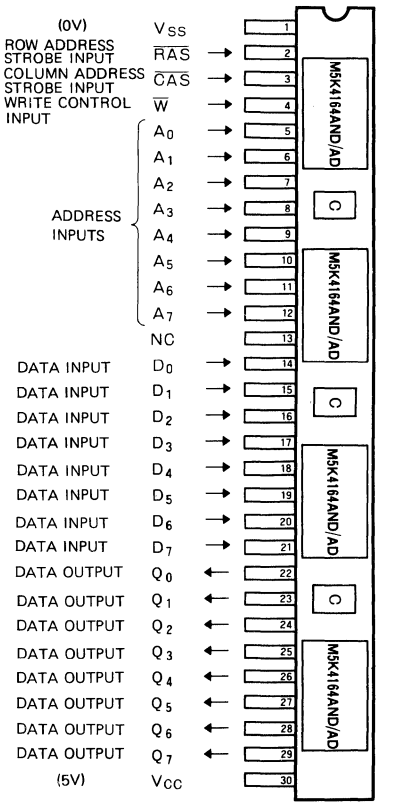
| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| MH6408AND-15 | 150 | 260 | 1200 |

- Utilizes industry standard 64K RAMs in leadless chip carriers
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 176mW(max)
- Low operating power dissipation:
  MH6408AND-15 1.9W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly
- All outputs are three-state and directly TTL compatible
- Includes (0.22$\mu$F x 6) decoupling capacitors
- 128 refresh cycles (every 2ms) $A_7$ Pin is not need for refresh

## APPLICATION

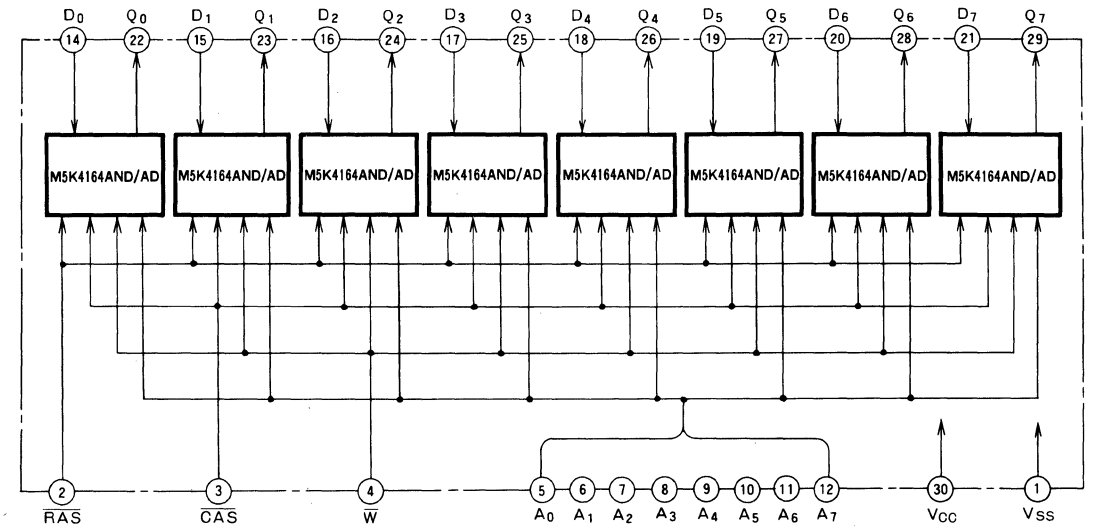
- Main memory unit for computers
- Refresh memory

## PIN CONFIGURATION (TOP VIEW)




**Outline 30S5**

## BLOCK DIAGRAM



## FUNCTION

The MH6408AND provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | | Output | Refresh | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | D | Row address | Column address | Q | | |
| Read | ACT | ACT | NAC | DNC | APD | APD | VLD | YES | Page mode identical except refresh is NO |
| Write | ACT | ACT | ACT | VLD | APD | APD | OPN | YES | |
| Read-modify-write | ACT | ACT | ACT | VLD | APD | APD | VLD | YES | |
| RAS-only refresh | ACT | NAC | DNC | DNC | APD | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | APD | DNC | VLD | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

## SUMMARY OF OPERATIONS

### Addressing

To select 8 of the 524288 memory cells in the MH6408-AND the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods.

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In This case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d\ (RAS\text{-}CAS)\ max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d\ (RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

### Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the W negative transition is set as the reference point for setup and hold times.

### Data Output Control

The outputs of the MH6408AND are in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The outputs will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the MH6408AND, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

**1. Common I/O Operation**

If all write operations are performed in the early-write mode, inputs and outputs can be connected directly to give a common I/O data bus.

**2. Data OUtput Hold**

The data outputs can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

**3. Two Methods of Chip Selection**

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

**4. Extended-Page Boundary**

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

## Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

## Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the MH6408AND must be refreshed every 2 ms to maintain data. The methods of refreshing for the MH6408AND are as follows.

**1. Normal Refresh**

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

**2. $\overline{RAS}$ Only Refresh**

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

**3. Hidden Refresh**

A features of the MH6408AND is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at $V_{IL}$ and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many paalications this eliminates the need for off-chip latches.

## Power Dissipation

Most of the circuitry in the MH6408AND is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH6408AND as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

## Power Supplies

The MH6408AND operates on a single 5V power supply.

A wait of some 500$\mu$s and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Paramater | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 8000 | mW |
| Topr | Operating free-air temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −55～150 | °C |
| $T_{sld}$ | Soldering temperature･time | | 260・10 | ℃・sec |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −2 | | 0.8 | V |

Note 1. All voltage values are with respect to $V_{SS}$

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝2.1mA | 0 | | 0.45 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≦$V_{OUT}$≦5.5V | −80 | | 80 | μA |
| $I_I$ | Input current | | 0V≦$V_{IN}$≦6.5V, All other pins＝0V | −80 | | 80 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3, 4) | MH6408AND-15 | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR}$＝$t_{CW}$＝min, output open | | | 320 | mA |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$V_{IH}$ output open | | | 32 | mA |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3) | MH6408AND-15 | $\overline{RAS}$ cycling $\overline{CAS}$＝$V_{IH}$ $t_{C(\overline{REF})}$＝min, output open | | | 280 | mA |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$, page mode (Note 3, 4) | MH6408AND-15 | $\overline{RAS}$＝$V_{IL}$, $\overline{CAS}$ cycling $t_{CPG}$＝min, output open | | | 280 | mA |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$＝$V_{SS}$ f＝1MHz $V_I$＝25mVrms | | | 70 | pF |
| $C_{I(D)}$ | Input capacitance, data input | | | | | 30 | pF |
| $C_{I(W)}$ | Input capacitance, write control input | | | | | 80 | pF |
| $C_{I(RAS)}$ | Input capacitance, $\overline{RAS}$ input | | | | | 100 | pF |
| $C_{I(CAS)}$ | Input capacitance, $\overline{CAS}$ input | | | | | 100 | pF |
| $C_O$ | Output capacitance | | $V_O$＝$V_{SS}$, f＝1MHz, $V_I$＝25mVrms | | | 30 | pF |

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

( Ta = 0 ~ 70°C , $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V , unless otherwise noted, See notes 5, 6 and 7)

| Symbol | Parameter | | Alternative Symbol | MH6408AND-15 Limits Min | MH6408AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRF}$ | Refresh cycle time | | $t_{REF}$ | | 2 | ms |
| $t_{W(RASH)}$ | $\overline{RAS}$ high pulse width | | $t_{RP}$ | 100 | | ns |
| $t_{W(RASL)}$ | $\overline{RAS}$ low pulse width | | $t_{RAS}$ | 150 | 10000 | ns |
| $t_{W(CASL)}$ | $\overline{CAS}$ low pulse width | | $t_{CAS}$ | 75 | ∞ | ns |
| $t_{W(CASH)}$ | $\overline{CAS}$ high pulse width | (Note 8) | $t_{CPN}$ | 35 | | ns |
| $t_{h(RAS-CAS)}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ | | $t_{CSH}$ | 150 | | ns |
| $t_{h(CAS-RAS)}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ | | $t_{RSH}$ | 75 | | ns |
| $t_{d(CAS-RAS)}$ | Delay time, $\overline{CAS}$ to $\overline{RAS}$ | (Note 9) | $t_{CRP}$ | −20 | | ns |
| $t_{d(RAS-CAS)}$ | Delay time, $\overline{RAS}$ to $\overline{CAS}$ | (Note 10) | $t_{RCD}$ | 30 | 75 | ns |
| $t_{su(RA-RAS)}$ | Row address setup time before $\overline{RAS}$ | | $t_{ASR}$ | 0 | | ns |
| $t_{su(CA-CAS)}$ | Column address setup time before $\overline{CAS}$ | | $t_{ASC}$ | 0 | | ns |
| $t_{h(RAS-RA)}$ | Row address hold time after $\overline{RAS}$ | | $t_{RAH}$ | 20 | | ns |
| $t_{h(CAS-CA)}$ | Column address hold time after $\overline{CAS}$ | | $t_{CAH}$ | 25 | | ns |
| $t_{h(RAS-CA)}$ | Column address hold time after $\overline{RAS}$ | | $t_{AR}$ | 95 | | ns |
| $t_{THL}$ $t_{TLH}$ | Transition time | | $t_T$ | 3 | 35 | ns |

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between $V_{IH}$ and $V_{IL}$.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)min}$.

## SWITCHING CHARACTERISTICS ( Ta = 0 ~ 70°C , $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V , unless otherwise noted)

### Read Cycle

| Symbol | Parameter | | Alternative Symbol | MH6408AND-15 Limits Min | MH6408AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{h(CAS-R)}$ | Read hold time after $\overline{CAS}$ | (Note 11) | $t_{RCH}$ | 0 | | ns |
| $t_{h(RAS-R)}$ | Read hold time after $\overline{RAS}$ | (Note 11) | $t_{RRH}$ | 20 | | ns |
| $t_{dis(CAS)}$ | Output disable time | (Note 12) | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12. $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to $V_{OH}$ or $V_{OL}$.
Note 13. This is the vauel when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2T TL, $C_L$ = 100pF
Note 14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, $C_L$ = 100pF

### Write Cycle

| Symbol | Parameter | | Alternative Symbol | MH6408AND-15 Limits Min | MH6408AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | | $t_{RC}$ | 260 | | ns |
| $t_{su(W-CAS)}$ | Write setup time before $\overline{CAS}$ | (Note 17) | $t_{WCS}$ | −5 | | ns |
| $t_{h(CAS-W)}$ | Write hold time after $\overline{CAS}$ | | $t_{WCH}$ | 45 | | ns |
| $t_{h(RAS-W)}$ | Write hold time after $\overline{RAS}$ | | $t_{WCR}$ | 95 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(D-CAS)}$ | Data-in setup time before $\overline{CAS}$ | | $t_{DS}$ | 0 | | ns |
| $t_{h(CAS-D)}$ | Data-in hold time after $\overline{CAS}$ | | $t_{DH}$ | 45 | | ns |
| $t_{h(RAS-D)}$ | Data-in hold time after $\overline{RAS}$ | | $t_{DHR}$ | 95 | | ns |

## Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Alternative Symbol | MH6408AND-15 Limits Min | MH6408AND-15 Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CRW}$ | Read-write cycle time | (Note 15) | $t_{RWC}$ | 280 | | ns |
| $t_{CRMW}$ | Read-modify-write cycle time | (Note 16) | $t_{RMWC}$ | 310 | | ns |
| $t_{h(W-RAS)}$ | $\overline{RAS}$ hold time after write | | $t_{RWL}$ | 45 | | ns |
| $t_{h(W-CAS)}$ | $\overline{CAS}$ hold time after write | | $t_{CWL}$ | 45 | | ns |
| $t_{w(W)}$ | Write pulse width | | $t_{WP}$ | 45 | | ns |
| $t_{su(R-CAS)}$ | Read setup time before $\overline{CAS}$ | | $t_{RCS}$ | 0 | | ns |
| $t_{d(RAS-W)}$ | Delay time, $\overline{RAS}$ to write | (Note 17) | $t_{RWD}$ | 120 | | ns |
| $t_{d(CAS-W)}$ | Delay time, $\overline{CAS}$ to write | (Note 17) | $t_{CWD}$ | 60 | | ns |
| $t_{su(D-W)}$ | Data-in setup time before write | | $t_{DS}$ | 0 | | ns |
| $t_{h(W-D)}$ | Data-in hold time after write | | $t_{DH}$ | 45 | | ns |
| $t_{dis(CAS)}$ | Output disable time | | $t_{OFF}$ | 0 | 40 | ns |
| $t_{a(CAS)}$ | $\overline{CAS}$ access time | (Note 13) | $t_{CAC}$ | | 75 | ns |
| $t_{a(RAS)}$ | $\overline{RAS}$ access time | (Note 14) | $t_{RAC}$ | | 150 | ns |

Note 15. $t_{CRW}$ min is defined as $t_{CRW}$ min = $t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH}(t_{THL})$

16. $t_{CRMW}$ min is defined as $t_{CRMW}$ min = $t_{a(RAS)}$max + $t_{h(W-RAS)} + t_{w(RAS\,H)} + 3t_{TLH}(t_{THL})$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$min, an early-write cycle is performed, and the data outputs keep the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$min a read-write cycle is performed, and the data of the selected address will be read out on the data outputs.

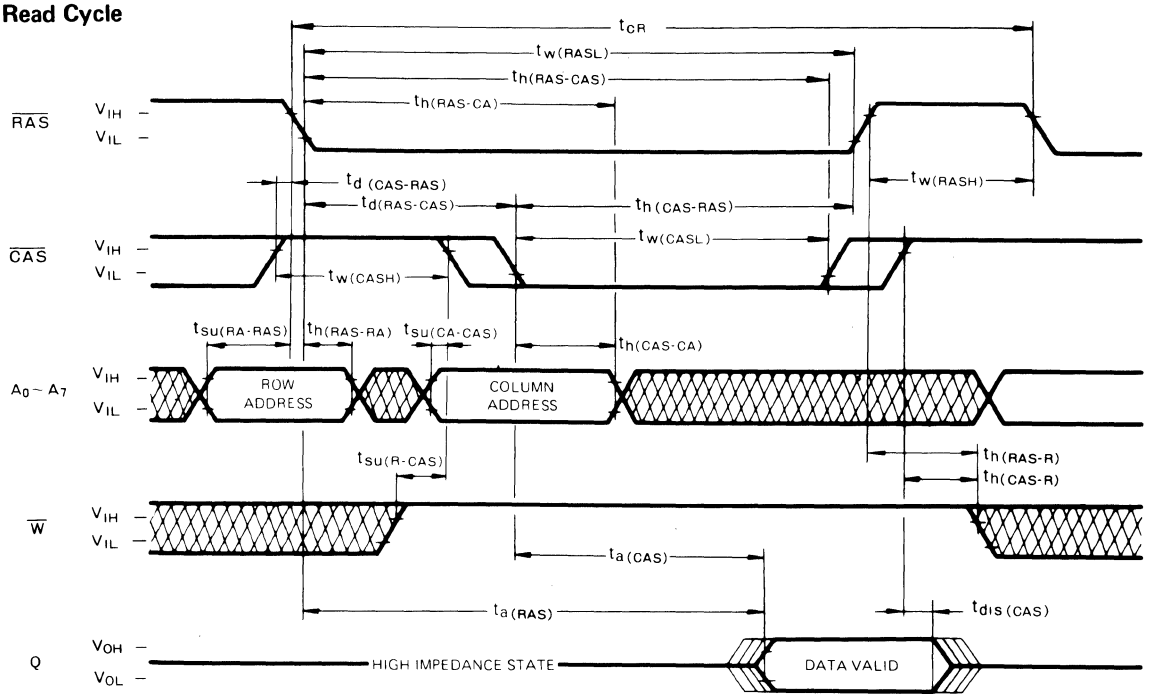
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is not defined.

## Page-Mode Cycle

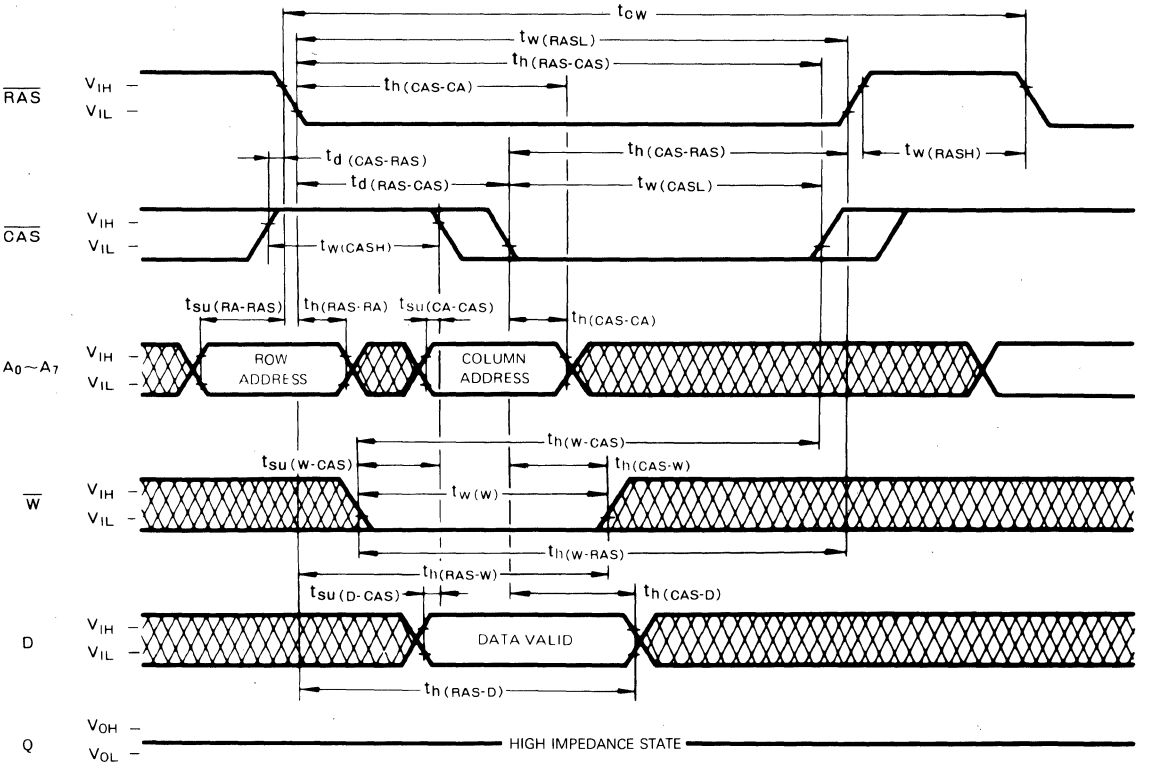
| Symbol | Parameter | Alternative Symbol | MH6408AND-15 Limits Min | MH6408AND-15 Limits Max | Unit |
|---|---|---|---|---|---|
| $t_{c\,PGR}$ | Page-Mode read cycle time | $t_{PC}$ | 145 | | ns |
| $t_{c\,PGW}$ | Page-Mode write cycle time | $t_{PC}$ | 145 | | ns |
| $t_{c\,PGRW}$ | Page-Mode read-write cycle time | — | 180 | | ns |
| $t_{c\,PGRMW}$ | Page-Mode read-modify-write cycle time | — | 195 | | ns |
| $t_{w(CASH)}$ | $\overline{CAS}$ high pulse width | $t_{CP}$ | 60 | | ns |

## TIMING DIAGRAMS (Note 18)

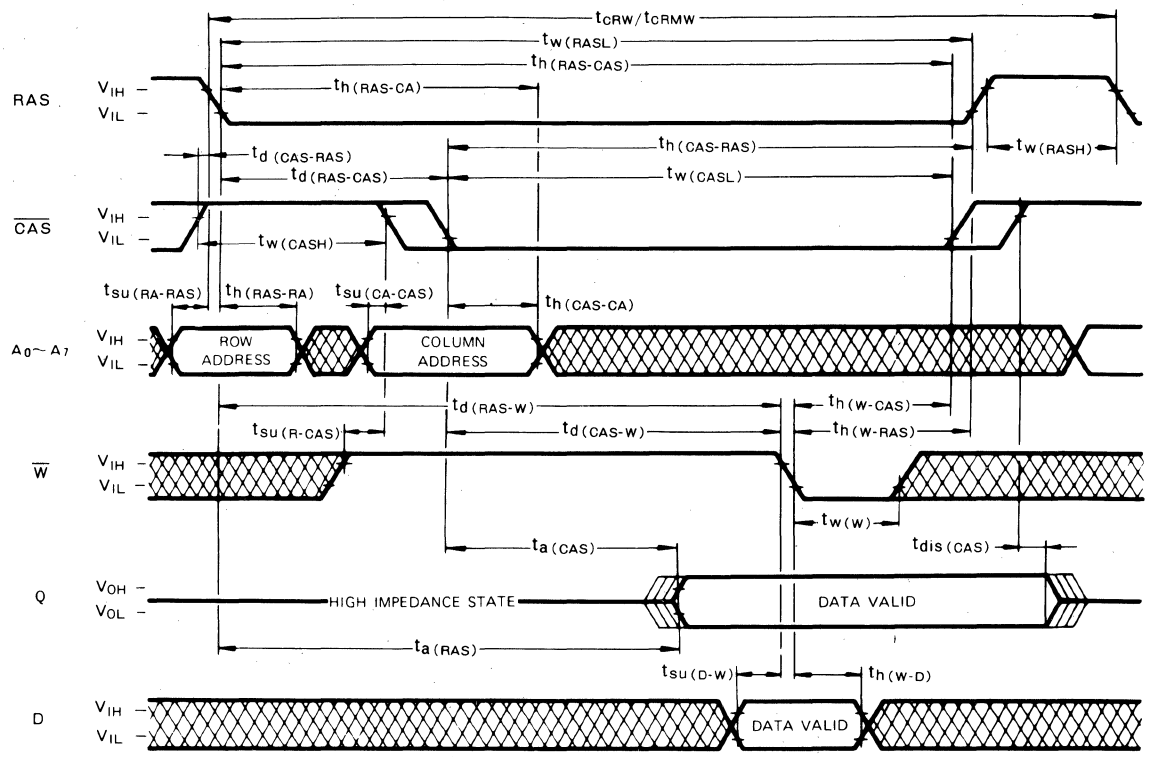
### Read Cycle



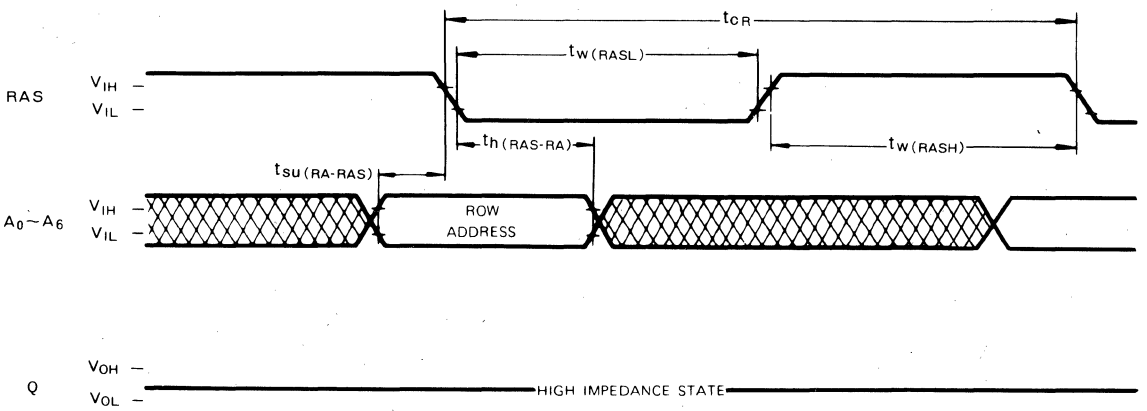

### Write Cycle (Early Write)



## Read-Write and Read-Modify-Write Cycles




## RAS-Only Refresh Cycle (Note 19)




Note 18

Indicates the don't care input

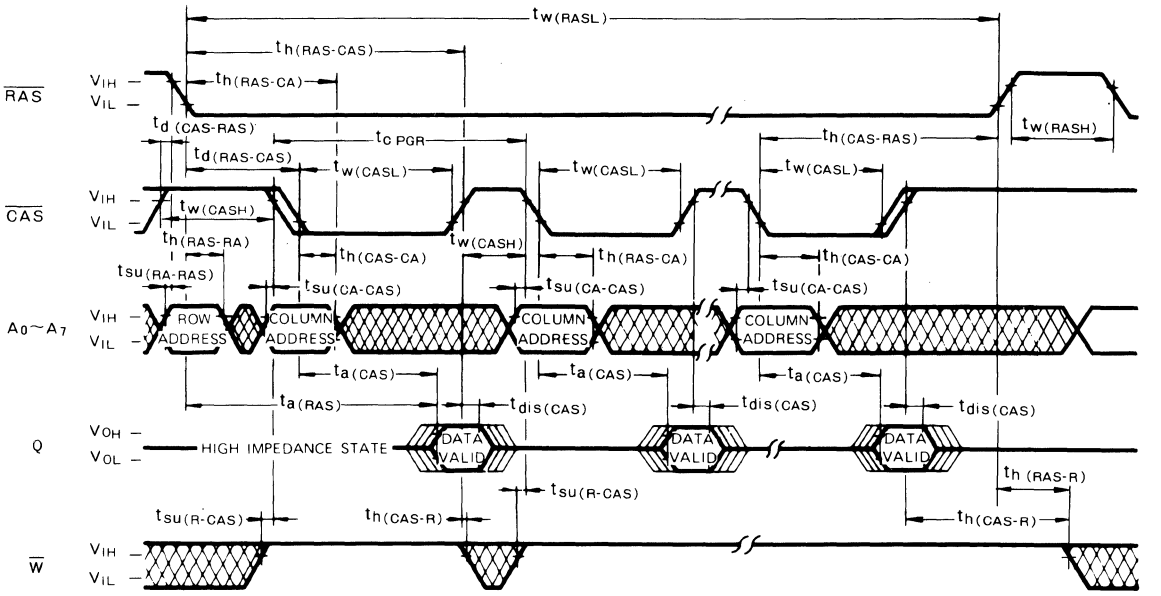
The center-line indicates the high-impedance state

Note 19. $\overline{CAS}$ = $V_{IH}$, $\overline{W}$, $A_7$, D = don't care.

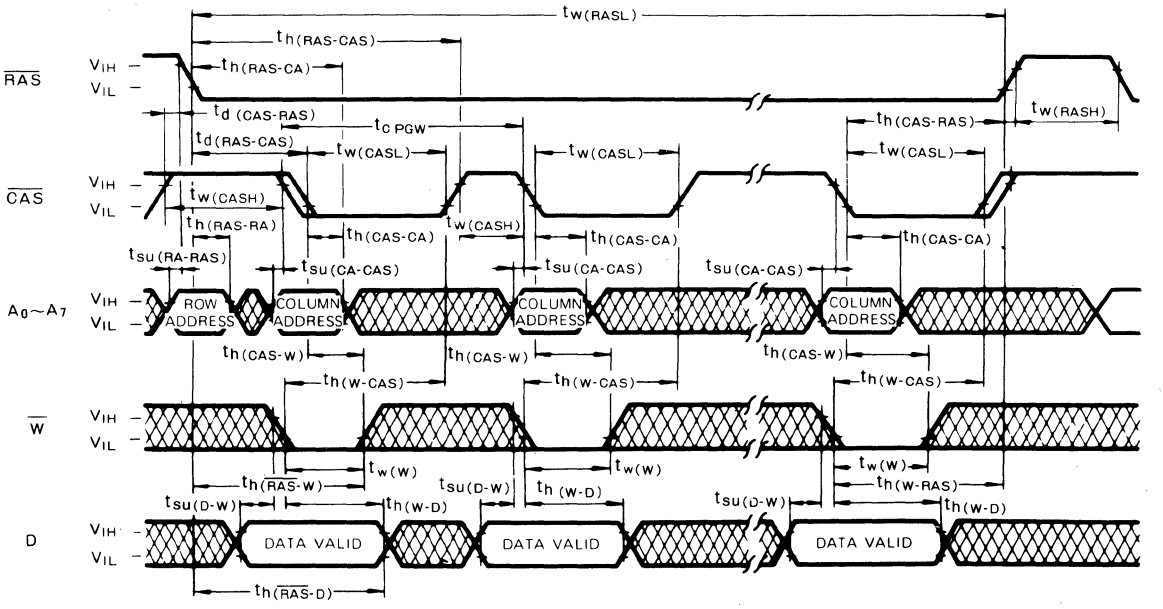


MITSUBISHI ELECTRIC

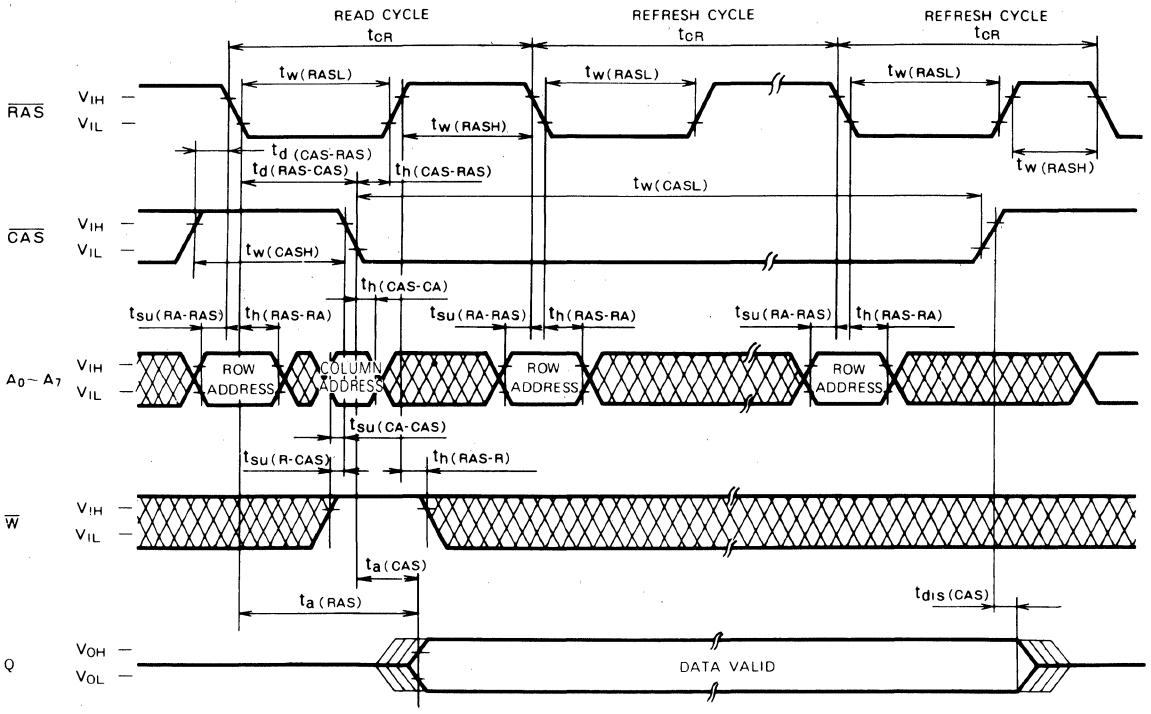
## Page-Mode Read Cycle




## Page-Mode Write Cycle

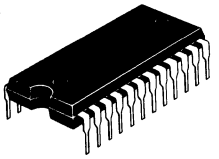


## Hidden Refresh Cycle



# NMOS STATIC RAM

3





# M58725P, -15

## 16 384-BIT (2048-WORD BY 8-BIT) STATIC RAM

## DESCRIPTION

This is a family of 2048-word by 8-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. These devices operate on a single 5V supply, as does TTL, and are directly TTL-compatible.

The input and output terminals are common, and an $\overline{OE}$ terminal is provided. $\overline{S}$ controls the power-down feature.

## FEATURES

- Fast access time:
  - M58725P 200ns (max)
  - M58725 P-15 150ns (max)
- Low power dissipation:
  - Active: 250mW (typ)
  - Stand by: 25mW (typ)
- Power down by $\overline{S}$
- Single 5V supply voltage (±10% tolerance)
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- All outputs are three-state, with OR-tie capability
- Easy memory expansion by chip-select ($\overline{S}$) input
- Common data DQ terminals.
- Same pin configuration as M5L2716K 16 384-bit EPROM

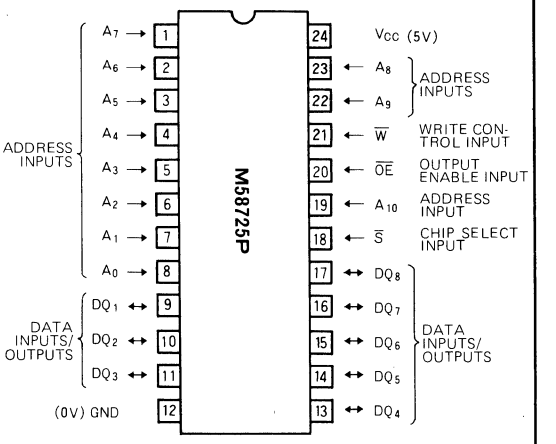
## APPLICATION

- Small-capacity memory units

## FUNCTION

These devices provide common data input and output terminals. During a write cycle, when a location is designated by address signals $A_0 \sim A_{10}$ the $\overline{OE}$ signal is kept high to keep the DQ terminals in the input mode, signal $\overline{W}$ goes low, and the data of the DQ signal at that time is written.

## PIN CONFIGURATION (TOP VIEW)



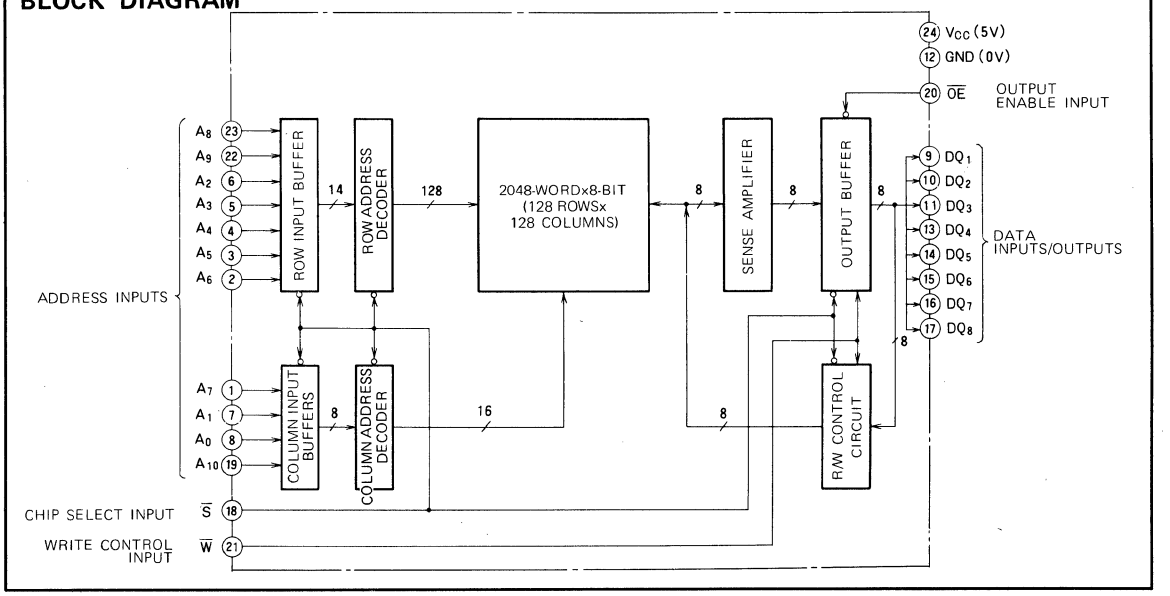

**Outline 24P4**

During a read cycle, when a location is designated by address signals $A_0 \sim A_{10}$ the $\overline{OE}$ signal is kept low to keep the DQ terminals in the output mode, signal $\overline{W}$ goes high, and the data of the designated address is available at the I/O terminals.

When signal $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

Signal $\overline{S}$ controls the power down feature. When $\overline{S}$ goes high power dissipation is reduced to 1/10 of active power. The access time from $\overline{S}$ is equivalent to the address access time.

## BLOCK DIAGRAM



## FUNCTION TABLE

| $\overline{S}$ | $\overline{OE}$ | $\overline{W}$ | $DQ_1 \sim DQ_8$ | Mode |
|---|---|---|---|---|
| H | X | X | Hi-Z | Deselect |
| L | X | L | $D_{IN}$ | Write |
| L | L | H | $D_{OUT}$ | Read |
| L | H | H | Hi-Z | — |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Test conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.5～7 | V |
| $V_I$ | Input voltage | | −0.5～7 | V |
| $V_O$ | Output voltage | | −0.5～7 | V |
| $P_d$ | Maximum power dissipation | Ta＝25°C | 1000 | mW |
| Topr | Operating free-air ambient temperature range | | 0～70 | °C |
| Tstg | Storage temperature range | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C、unless otherwise noted.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | −1 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 6 | V |

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, unless otherwise noted.)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2 | | 6 | V |
| $V_{IL}$ | Low-level input voltage | | | −1 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$＝−1mA, $V_{CC}$＝4.5V | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$＝3.2mA | | | | 0.4 | V |
| $I_I$ | Input current | $V_I$＝0～5.5V | | | | 10 | μA |
| $I_{OZH}$ | Off-state high-level output current | $V_{I(\overline{S})}$＝2V, $V_O$＝2.4V～$V_{CC}$ | | | | 10 | μA |
| $I_{OZL}$ | Off-state low-level output current | $V_{I(\overline{S})}$＝2V, $V_O$＝0.4V | | | | −10 | μA |
| $I_{CC1}$ | Supply current from $V_{CC}$ | $V_I$＝5.5V, $V_{I(\overline{S})}$＝0.8V, outputs open | Ta＝25°C | | 50 | 80 | mA |
| | | | Ta＝0°C | | | 90 | mA |
| $I_{CC2}$ | Stand by current | $V_I$＝5.5V, $V_{I(\overline{S})}$＝2V outputs open | Ta＝25°C | | 5 | 10 | mA |
| | | | Ta＝70°C | | 7 | 15 | mA |
| $C_i$ | Input capacitance, all inputs | $V_I$＝GND, Vi＝25mVrms, f＝1MHz | | | 3 | 5 | pF |
| $C_o$ | Output capacitance | $V_O$＝GND, $V_O$＝25mVrms, f＝1MHz | | | 5 | 8 | pF |

Note 1: Current flowing into an IC is positive, out is negative.

## 16384-BIT (2048-WORD BY 8-BIT) STATIC RAM

### SWITCHING CHARACTERISTICS (For Read Cycle) ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

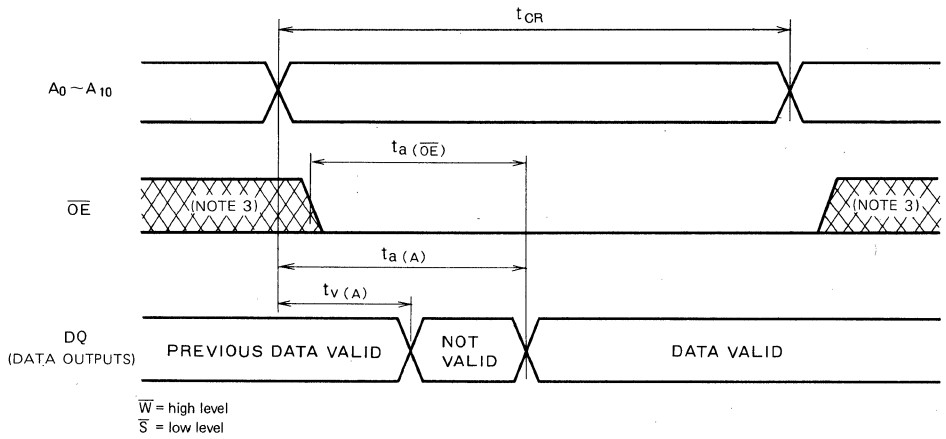
| Symbol | Parameter | M58725P-15 | | | M58725P | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_a$ (A) | Address access time | | | 150 | | | 200 | ns |
| $t_a$ ($\overline{S}$) | Chip select access time | | | 150 | | | 200 | ns |
| $t_a$ ($\overline{OE}$) | Output enable access time | | | 50 | | | 60 | ns |
| $t_v$ (A) | Data valid time after address | 20 | | | 20 | | | ns |
| $t_{PXZ}$ ($\overline{S}$) | Output disable time after chip select | | | 50 | | | 60 | ns |
| $t_{PZX}$ ($\overline{S}$) | Output active time after chip select | 10 | | | 20 | | | ns |
| $t_{PU}$ | Power up time after chip selection | 0 | | | 0 | | | ns |
| $t_{PD}$ | Power down time after chip deselection | | | 60 | | | 80 | ns |

### TIMING REQUIREMENTS (For Write Cycle) ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

| Symbol | Parameter | M58725P-15 | | | M58725P | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 150 | | | 200 | | | ns |
| $t_{su}$ ($\overline{S}$) | Chip select setup time | 100 | | | 120 | | | ns |
| $t_{su}$ (A) | Address setup time | 20 | | | 20 | | | ns |
| $t_w$ ($\overline{W}$) | Write pulse width | 80 | | | 100 | | | ns |
| $t_{wr}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{su}$ ($\overline{OE}$) | Output enable setup time | 40 | | | 40 | | | ns |
| $t_{su}$ (D) | Data setup time | 60 | | | 60 | | | ns |
| $t_h$ (D) | Data hold time | 10 | | | 10 | | | ns |
| $t_{PXZ}$ ($\overline{OE}$) | Output disable time after output enable | | | 40 | | | 40 | ns |
| $t_{PXZ}$ ($\overline{W}$) | Output disable time after write enable | | | 40 | | | 40 | ns |

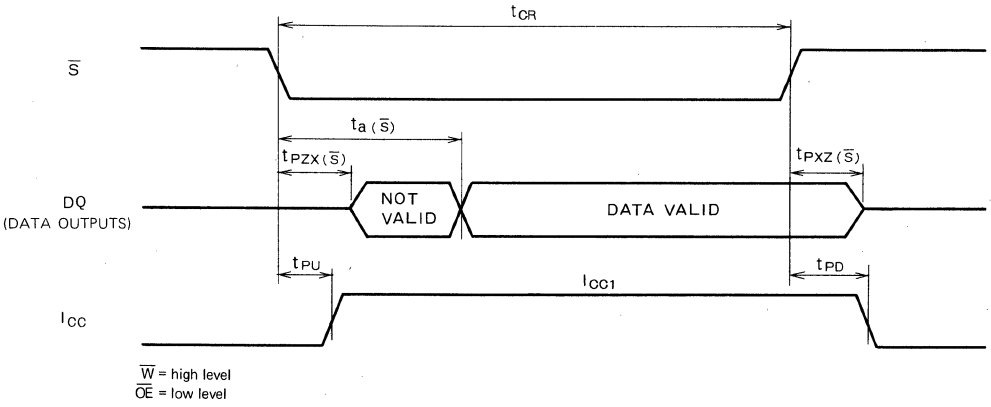
## TIMING DIAGRAMS (Note 2)

### Read Cycle 1




W = high level
S = low level

### Read Cycle 2

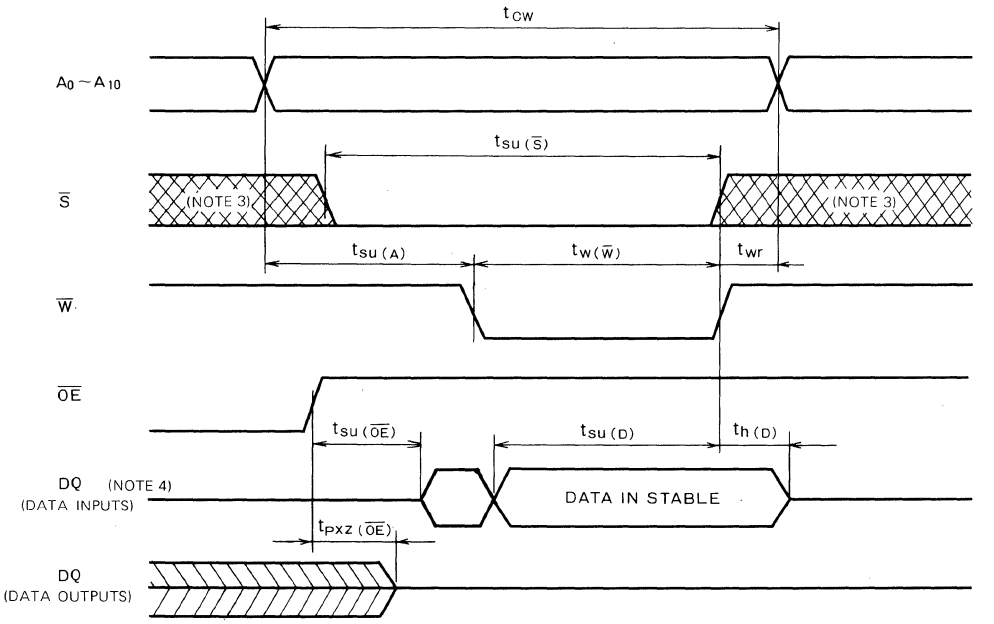



W = high level
OE = low level

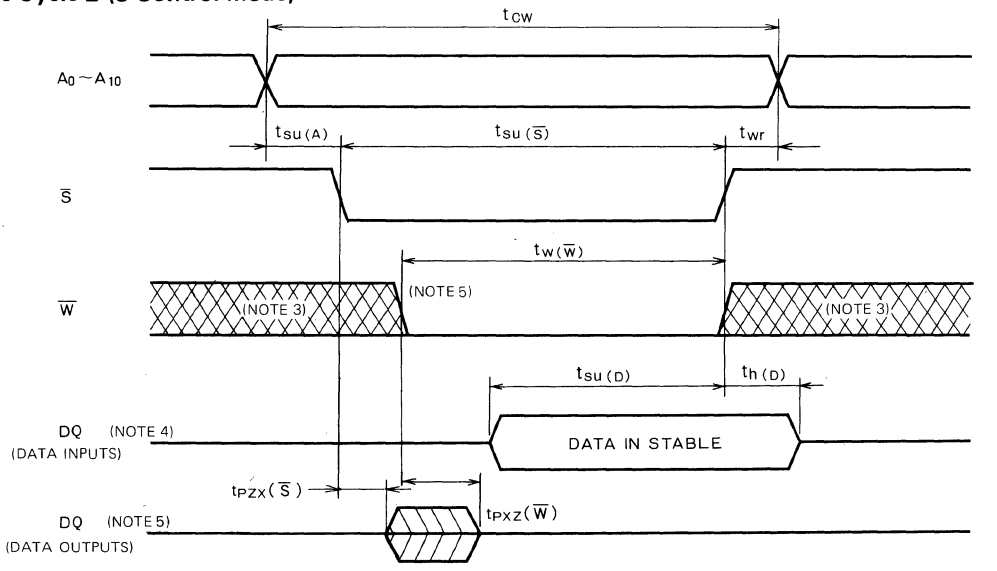


MITSUBISHI ELECTRIC

## Write Cycle 1 ($\overline{W}$ Control Mode)




## Write Cycle 2 ($\overline{S}$ Control Mode)




$\overline{OE}$ = low level

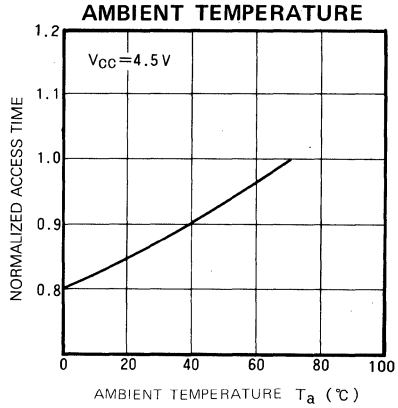
Note 2. Testconditions

| | |
|---|---|
| Input pulse level | 0.4 ~ 2.4V |
| Input pulse rise time | 10ns |
| Input pulse fall time | 10ns |
| Reference level | 1.5 V |
| Load | 1TTL, $C_L$ = 100pF |

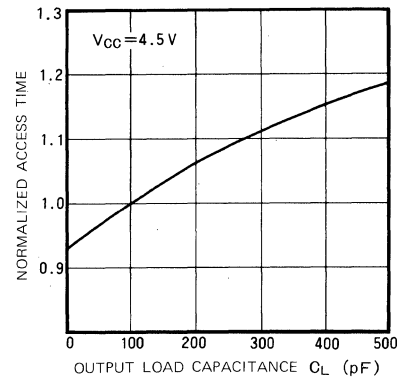
Note 3. Either the high or low state is possible.
4. When the DQ pin is in the output state, a reverse phase signal should not be applied externally.
5. When the falling edge of $\overline{W}$ is simultaneous to or prior to the falling edge of $\overline{S}$, the output is maintained in the high-impedance state.

## TYPICAL CHARACTERISTICS

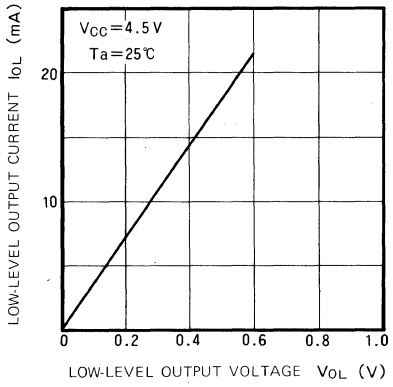
### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



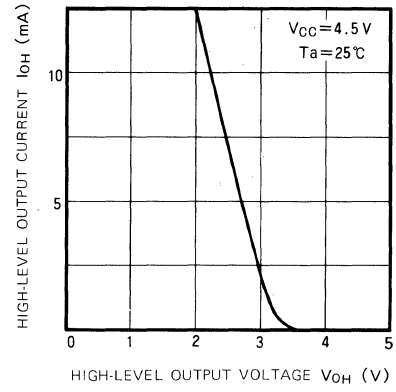

### NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



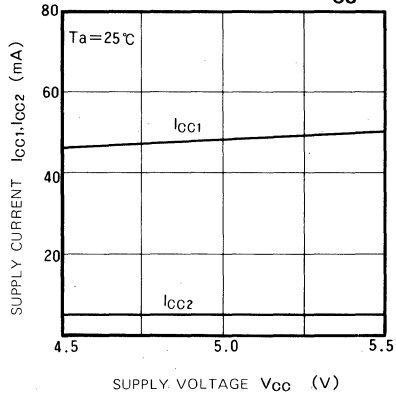

### LOW-LEVEL OUTPUT CURRENT VS. LOW-LEVEL OUTPUT VOLTAGE



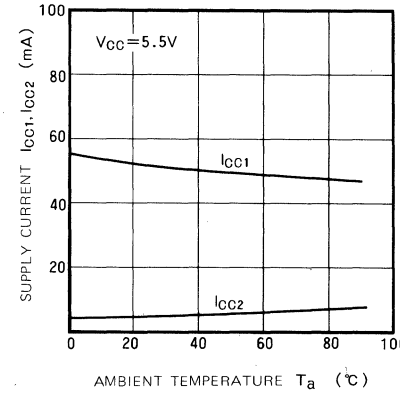

### HIGH-LEVEL OUTPUT CURRENT VS. HIGH-LEVEL OUTPUT VOLTAGE

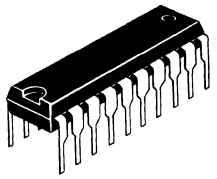



### SUPPLY CURRENT VS. SUPPLY VOLTAGE Vcc




### SUPPLY CURRENT VS. AMBIENT TEMPERATURE







# M5M2167P-55, -70

## 16384-BIT (16384-WORD BY 1-BIT) STATIC RAM

## DESCRIPTION

This is a family of 16384-word by 1-bit static RAMs, fabricated with the high-performance N-channel silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

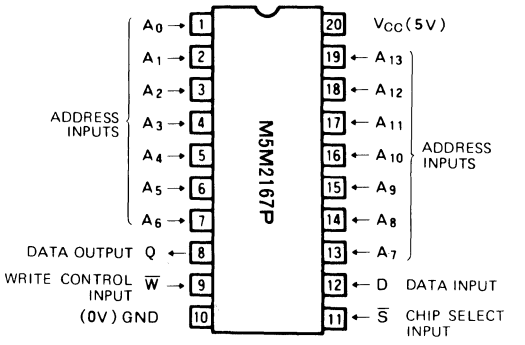
## FEATURES

- Fast access time — M5M2167P-55.....55 ns (max); M5M2167P-70.....70 ns (max)
- Low power dissipation — Active.....400 mW (typ); Standy by.....40 mW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Interchangeable with Intel's 2167

## APPLICATION

- High-speed memory systems

## PIN CONFIGURATION (TOP VIEW)




Outline 20 P4

## FUNCTION

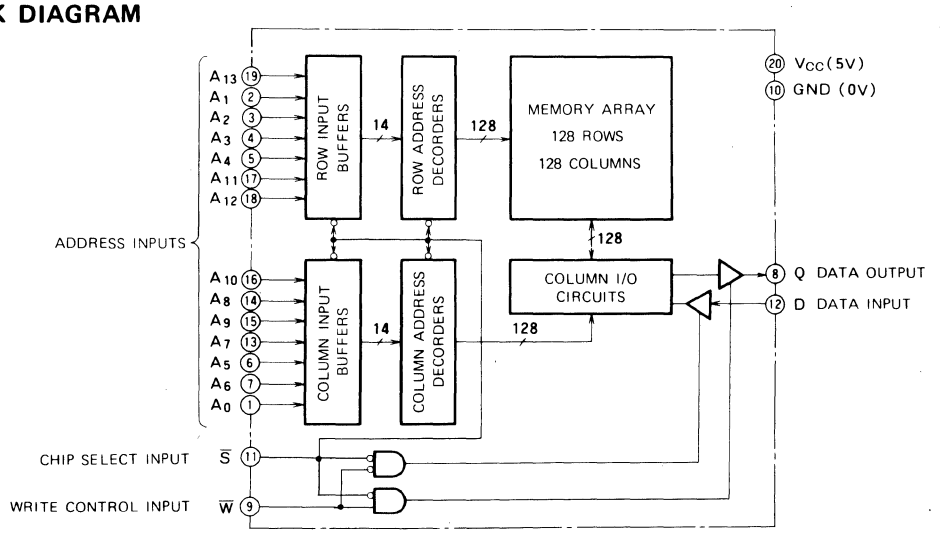
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced to 1/10 of active power. The access time from $\overline{S}$ is equivalent to the address access time.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −3.5 ~ 7 | V |
| $V_I$ | Input voltage | | −3.5 ~ 7 | V |
| $V_O$ | Output voltage | | −3.5 ~ 7 | V |
| Pd | Maximum power dissipation | | 1 | W |
| Topr | Temperature under bias | | −10 ~ 85 | °C |
| Tstg | Storage temperature | | −65 ~ 150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | −3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 6 | V |

Necessary airflow cooling >2m/s

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2 | | 6 | V |
| $V_{IL}$ | Low-level input voltage | | | −3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −4 mA | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA | | | | 0.4 | V |
| $I_I$ | Input current | $V_I$ = 0 ~ 5.5V | | | | 10 | μA |
| $\|I_{OZ}\|$ | Off-state output current | $V_I(\overline{S})$ = 2V, $V_O$ = 0 ~ $V_{CC}$ | | | | 50 | μA |
| $I_{CC1}$ | Supply current from $V_{CC}$ | $V_I(\overline{S})$ = 0.8V, Output open | Ta = 25°C | | 80 | 120 | mA |
| | | | Ta = 0 °C | | | 125 | |
| $I_{CC2}$ | Stand by current | $V_I(\overline{S})$ = 2V output open | | | 8 | 30 | mA |
| $I_{PO}$ | Peak power-on current | $V_{CC}$ = 0 ~ 4.5V, $V_I(\overline{S})$ = Lower of $V_{CC}$ or $V_{IH}$ min | | | | 30 | mA |
| $C_I$ | Input capacitance | $V_I$ = GND, $V_I$ = 25mVrms, f = 1MHz | | | | 5 | pF |
| Co | Output capacitance | $V_O$ = GND, $V_O$ = 25mVrms, f = 1MHz | | | | 6 | pF |

Note 1. Current flow into an IC is positive, out is negative.

## SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | M5M2167P-55 | | | M5M2167P-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{cR}$ | Read cycle time | 55 | | | 70 | | | ns |
| $t_{a(A)}$ | Address access time | | | 55 | | | 70 | ns |
| $t_{a(S)}$ | Chip select access time | | | 55 | | | 70 | ns |
| $t_{v(A)}$ | Data valid time after address | 5 | | | 5 | | | ns |
| $t_{en(S)}$ | Output enable time after chip selection | 10 | | | 10 | | | ns |
| $t_{dis(S)}$ | Output disable time after chip deselection | 0 | | 25 | 0 | | 30 | ns |
| $t_{PU}$ | Power-up time after chip selection | 0 | | | 0 | | | ns |
| $t_{PD}$ | Power down time after chip deselection | | | 30 | | | 40 | ns |

## 16384-BIT (16384-WORD BY 1-BIT) STATIC RAM

## TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | M5M2167P-55 | | | M5M2167P-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{cW}$ | Write cycle time | 55 | | | 70 | | | ns |
| $t_{su(S)}$ | Chip select setup time | 50 | | | 60 | | | ns |
| $t_{su(A)_1}$ | Address setup time 1 ($\overline{W}$ CONTROL) | 5 | | | 5 | | | ns |
| $t_{su(A)_2}$ | Address setup time 2 ($\overline{S}$ CONTROL) | 0 | | | 0 | | | ns |
| $t_{w(W)}$ | Write pulse width | 35 | | | 40 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 5 | | | 5 | | | ns |
| $t_{su(D)}$ | Data setup time | 25 | | | 30 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{dis(W)}$ | Output disable time after $\overline{W}$ low | 0 | | 25 | 0 | | 30 | ns |
| $t_{en(W)}$ | Output enable time after $\overline{W}$ high | 0 | | | 0 | | | ns |
| $t_{su(A-\overline{W}H)}$ | Address to $\overline{W}$ high | 40 | | | 45 | | | ns |

### CONDITIONS

Input pulse levels ..... 0 to 3V
input rise and falltime ..... 5 ns
Input timing reference level ..... 1.5V
Output timing reference level ..... 0.8 ~ 2V
Output load ..... Fig. 1, Fig. 2

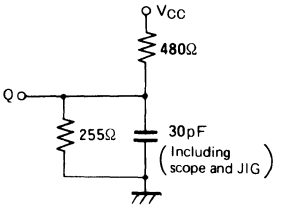



Fig. 1 Output load

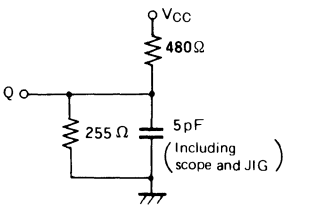
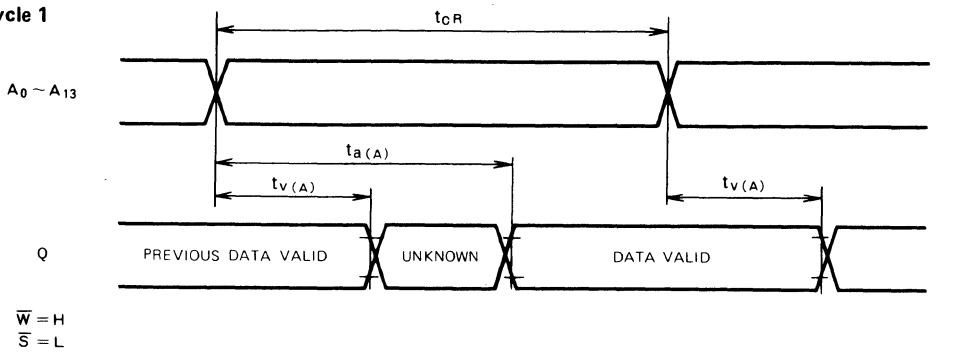


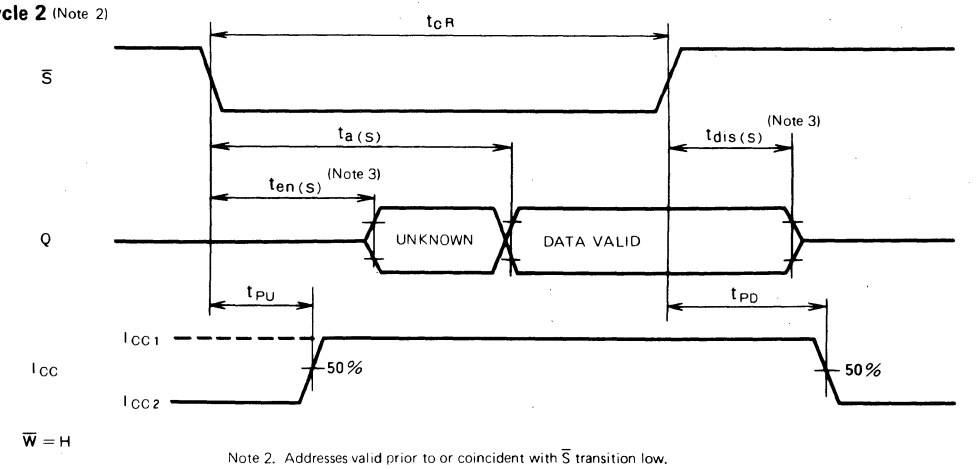

Fig. 2 Output load for ten, tdis

## TIMING DIAGRAMS

**Read cycle 1**



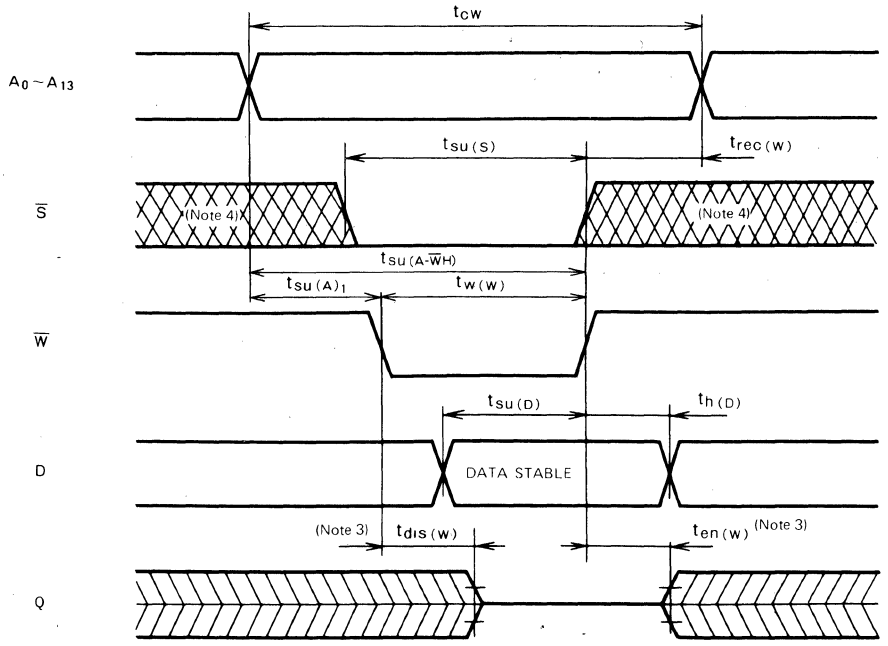

**Read cycle 2** (Note 2)



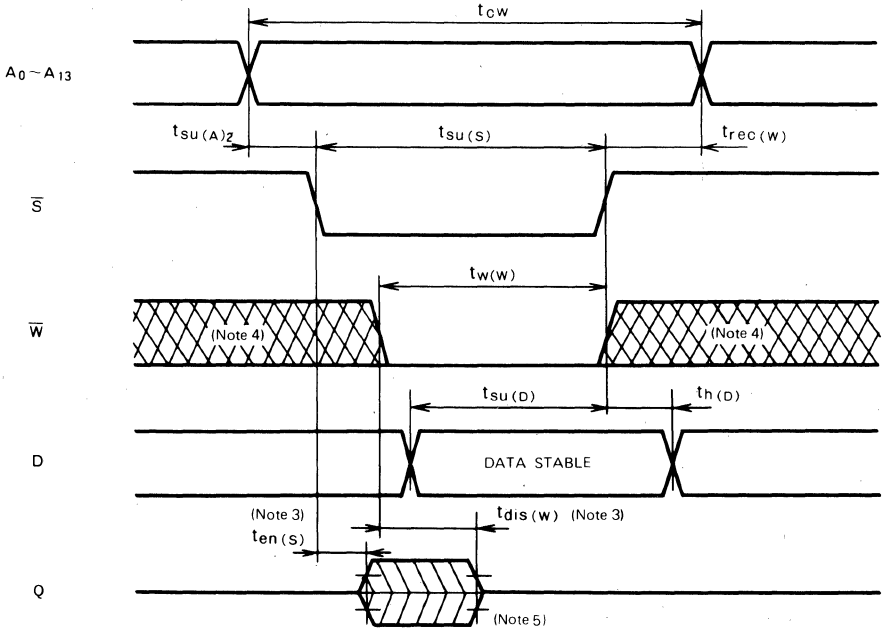

Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

## TIMING DIAGRAMS

**Write cycle 1 ($\overline{W}$ control mode)**

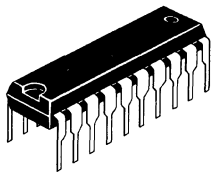



**Write cycle 2 ($\overline{S}$ control mode)**




Note 4. Hatching indicates the state is don't care.

5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.





# M5M2168P-55, -70

## 16384-BIT (4096-WORD BY 4-BIT) STATIC RAM

## DESCRIPTION

This is a family of 4096 word by 4-bit static RAMs, fabricated with the high-performance N-channel silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

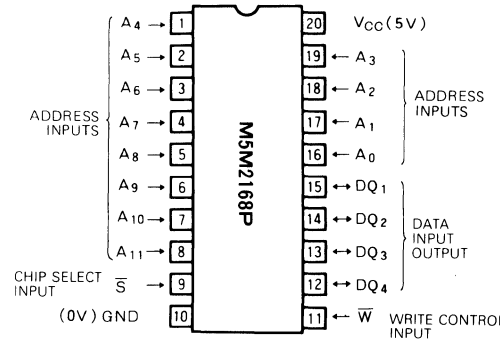
## FEATURES

- Fast access time — M5M2168P-55 ..... 55 ns (max); M5M2168P-70 ..... 70 ns (max)
- Low power dissipation — Active ..... 500 mW (typ); Standy by ..... 40 mW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Interchangeable with Intel's 2168

## APPLICATION

- High-speed memory systems

## PIN CONFIGURATION (TOP VIEW)




**Outline 20 P4**

## FUNCTION

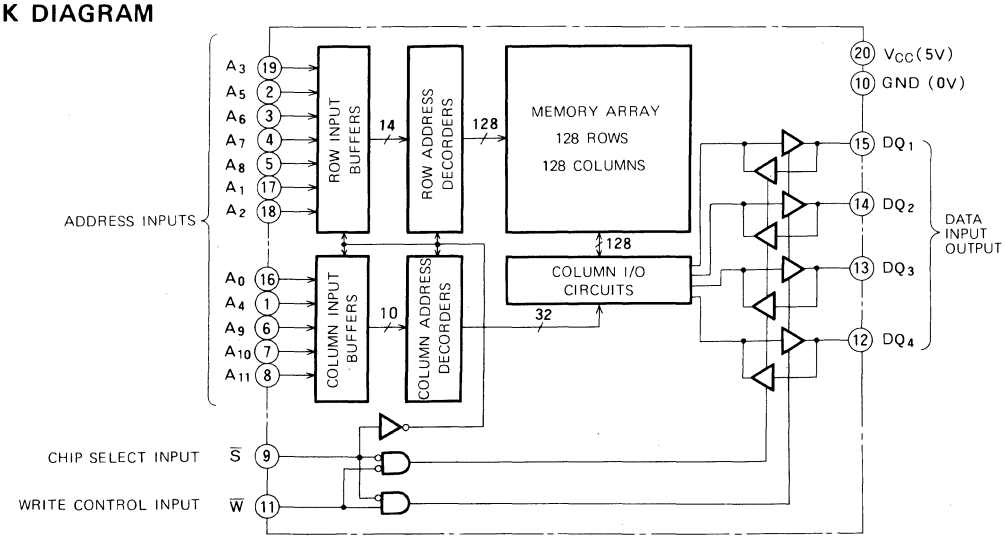
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced to 1/10 of active power. The access time from $\overline{S}$ is equivalent to the address access time.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −3.5～7 | V |
| $V_I$ | Input voltage | | −3.5～7 | V |
| $V_O$ | Output voltage | | −3.5～7 | V |
| Pd | Maximum power dissipation | | 1 | W |
| Topr | Temperature under bias | | −10～85 | °C |
| Tstg | Storage temperature | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_a$ = 0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | −3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 6 | V |

Necessary airflow cooling >2m/s

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0～70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2 | | 6 | V |
| $V_{IL}$ | Low-level input voltage | | | −3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = − 4 mA | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA | | | | 0.4 | V |
| $I_I$ | Input current | $V_I$ = 0～5.5V | | | | 10 | μA |
| $\|I_{OZ}\|$ | Off-state output current | $V_{I(\overline{S})}$ = 2V, $V_O$ = 0～$V_{CC}$ | | | | 50 | μA |
| $I_{CC1}$ | Supply current from $V_{CC}$ | $V_{I(\overline{S})}$ = 0.8V, Output open | Ta = 25°C | | 100 | 150 | mA |
| | | | Ta = 0 °C | | | 155 | |
| $I_{CC2}$ | Stand by current | $V_{I(\overline{S})}$ = 2V output open | | | 8 | 30 | mA |
| $I_{PO}$ | Peak power-on current | $V_{CC}$ = 0～4.5V, $V_{I(\overline{S})}$ = Lower of $V_{CC}$ or $V_{IH}$ min | | | | 30 | mA |
| $C_i$ | Input capacitance | $V_I$ = GND, $V_i$ = 25mVrms, f = 1MHz | | | | 5 | pF |
| Co | Output capacitance | $V_O$ = GND, $V_o$ = 25mVrms, f = 1MHz | | | | 6 | pF |

Note 1. Current flow into an IC is positive, out is negative.

## SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a$ = 0～70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | M5M2168P-55 | | | M5M2168P-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 55 | | | 70 | | | ns |
| $t_{a(A)}$ | Address access time | | | 55 | | | 70 | ns |
| $t_{a(S)}$ | Chip select access time | | | 55 | | | 70 | ns |
| $t_{v(A)}$ | Data valid time after address | 5 | | | 5 | | | ns |
| $t_{en(S)}$ | Output enable time after chip selection | 20 | | | 20 | | | ns |
| $t_{dis(S)}$ | Output disable time after chip deselection | 0 | | 20 | 0 | | 25 | ns |
| $t_{PU}$ | Power-up time after chip selection | 0 | | | 0 | | | ns |
| $t_{PD}$ | Power down time after chip deselection | | | 25 | | | 30 | ns |

## TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | M5M2168P-55 | | | M5M2168P-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{cW}$ | Write cycle time | 50 | | | 60 | | | ns |
| $t_{su(S)}$ | Chip select setup time | 45 | | | 55 | | | ns |
| $t_{su(A)_1}$ | Address setup time 1 ($\overline{W}$ CONTROL) | 0 | | | 0 | | | ns |
| $t_{su(A)_2}$ | Address setup time 2 ($\overline{S}$ CONTROL) | 0 | | | 0 | | | ns |
| $t_{w(W)}$ | Write pulse width | 40 | | | 50 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 0 | | | 0 | | | ns |
| $t_{su(D)}$ | Data setup time | 20 | | | 30 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{dis(W)}$ | Output disable time after $\overline{W}$ low | 0 | | 25 | 0 | | 30 | ns |
| $t_{en(W)}$ | Output enable time after $\overline{W}$ high | 5 | | | 5 | | | ns |
| $t_{su(A-\overline{W}H)}$ | Address to $\overline{W}$ high | 45 | | | 55 | | | ns |

### CONDITIONS

Input pulse levels ..... 0 to 3V
input rise and falltime ..... 5 ns
Input timing reference level ..... 1.5V
Output timing reference level ..... 0.8~2V
Output load ..... Fig. 1, Fig. 2

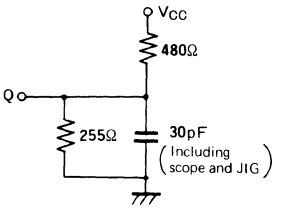



Fig. 1 Output load

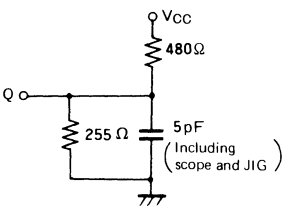
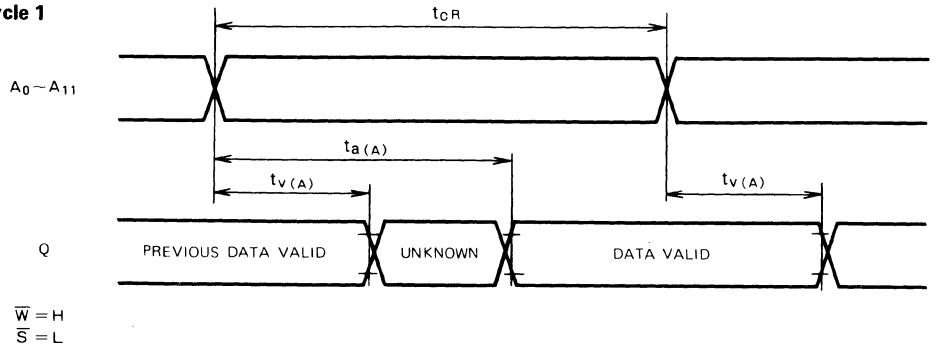


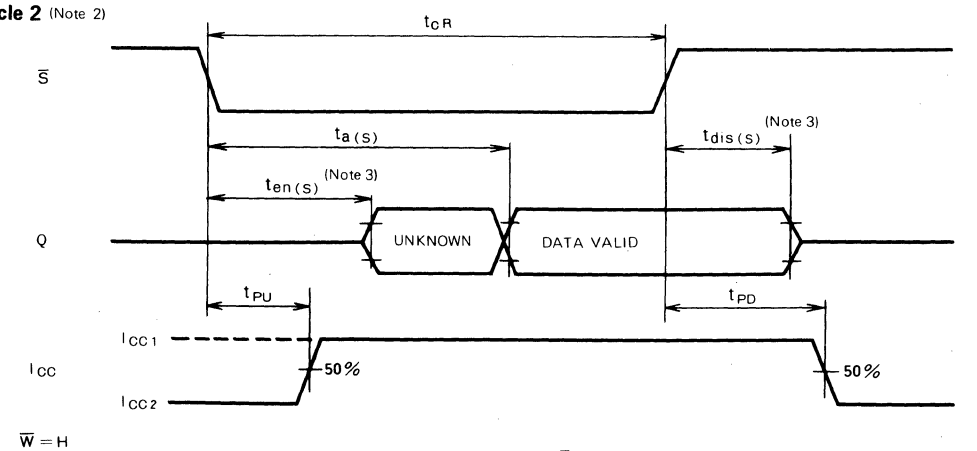

Fig. 2 Output load for ten, tdis

## TIMING DIAGRAMS

**Read cycle 1**



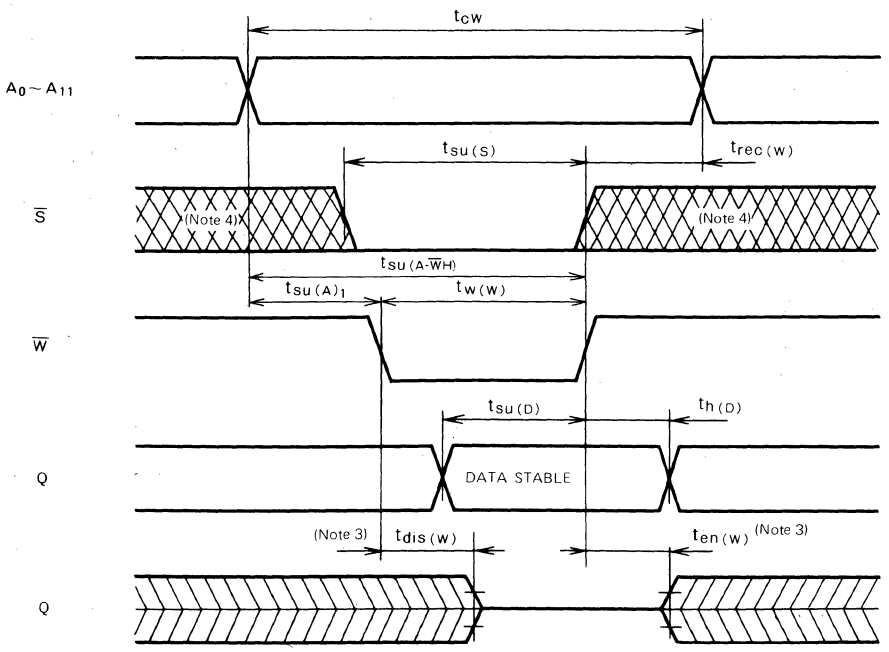

**Read cycle 2** (Note 2)



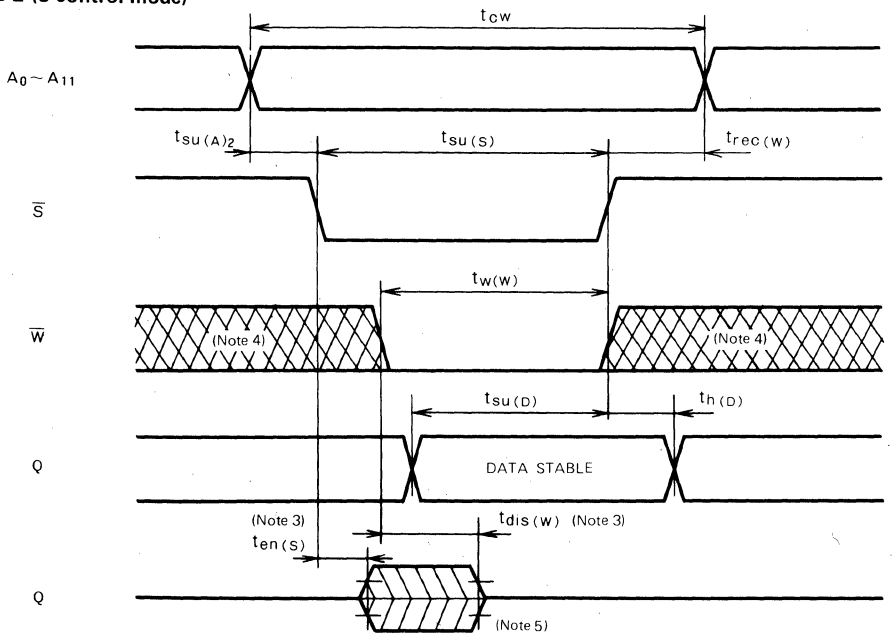

Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

## TIMING DIAGRAMS

**Write cycle 1 ($\overline{W}$ control mode)**




**Write cycle 2 ($\overline{S}$ control mode)**

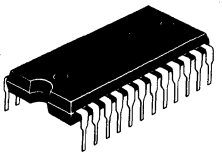



Note 4. Hatching indicates the state is don't care.

5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

# CMOS STATIC RAM

4





# M5M5116P, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5116P series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery backup.

Two chip select inputs are available: $\overline{S_2}$ provides the minimum standby current with battery back-up while $\overline{S_1}$ enables high-speed memory access.

The series is packaged in a standard 24-pin plastic DIL package.

## FEATURES

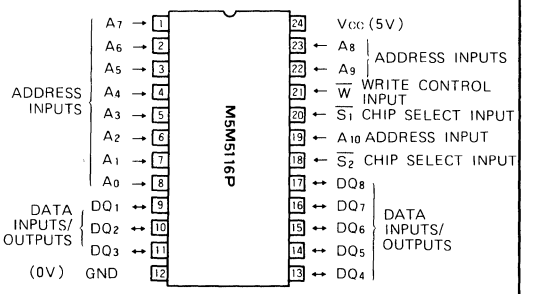
| Type name | Access time (max) | $\overline{S_1}$ access time (max) | Current consumption | |
|---|---|---|---|---|
| | | | Active (max) | Stand-by (max) |
| **M5M5116P-15** | 150ns | 80ns | 50mA | 15$\mu$A |
| **M5M5116P** | 200ns | 100ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins.

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)




**Outline 24P4**

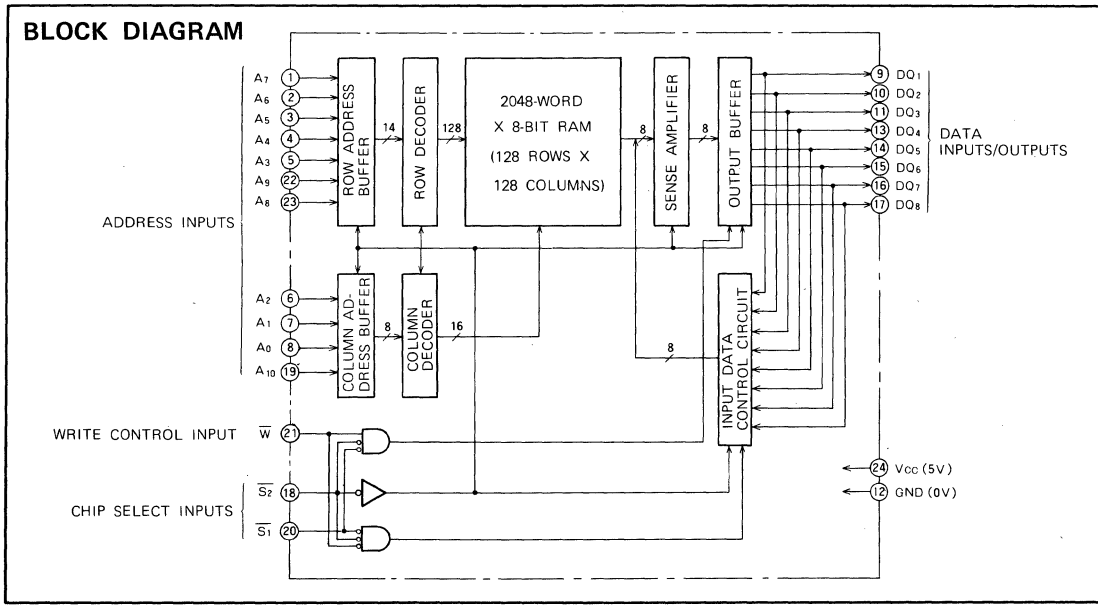
## FUNCTION

The M5M5116P series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use.

The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S_1}$ and $\overline{S_2}$ signals turn low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high,

## BLOCK DIAGRAM



the $\overline{S_1}$ and $\overline{S_2}$ signals are set low, pin DQ is set to the output mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

When signal $\overline{S_1}$ or $\overline{S_2}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins.

The standby mode is established when signal $\overline{S_2}$ is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and the data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

## OPERATION MODES

| $\overline{S_1}$ | $\overline{S_2}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| X | H | X | Non-select | High impedance | Standby |
| H | L | X | Non-select | High impedance | Active |
| L | L | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3~7 | V |
| $V_I$ | Input voltage | | −0.3~$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0~$V_{CC}$ | V |
| Pd | Power dissipation | Ta=25°C | 700 | mW |
| Topr | Operating free-air ambient temperature | | 0~70 | °C |
| Tstg | Storage temperature | | −65~150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

## ELECTRICAL CHARACTERISTICS (Ta=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$=0~$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S_1}$ or $\overline{S_2}$=$V_{IH}$, $V_O$=2.4V~$V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S_1}$ or $\overline{S_2}$=$V_{IH}$, $V_O$=0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5116P-15 | $V_I(\overline{S_1})$=$V_I(\overline{S_2})$=0V Output pin open Other inputs=$V_{CC}$ or 0V | | | 45 | mA |
| | | M5M5116P | | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5116P-15 | $V_I(\overline{S_1})$=$V_I(\overline{S_2})$=$V_{IL}$ Output pin open Other inputs=$V_{IH}$ | | | 50 | mA |
| | | M5M5116P | | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | $\overline{S_2}$=$V_{CC}$−0.2V, Other inputs=0~$V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S_2}$=$V_{IH}$, Other inputs=0~$V_{CC}$ | | | 2 | mA |
| Ci | Input capacitance (Ta=25°C) | | $V_I$=GND, Vi=25mVrms, f=1MHz | | | 6 | pF |
| Co | Output capacitance (Ta=25°C) | | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5116P-15 Limits | | | M5M5116P Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a(S_1)}$ | Chip select 1 access time | | | 80 | | | 100 | ns |
| $t_{a(S_2)}$ | Chip select 2 access time | | | 150 | | | 200 | ns |
| $t_{dis(S_1)}$ | Output disable time from S1 | | | 50 | | | 60 | ns |
| $t_{dis(S_2)}$ | Output disable time from S2 | | | 50 | | | 60 | ns |
| $t_{en(S_1)}$ | Output enable time from S1 | 15 | | | 15 | | | ns |
| $t_{en(S_2)}$ | Output enable time from S2 | 15 | | | 15 | | | ns |
| $t_{v(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5116P-15 Limits | | | M5M5116P Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 150 | | | 200 | | | ns |
| $t_{w(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{dis(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I(S_2)}$ | Chip select input voltage | $2.2V \leqq V_{CC(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC(PD)} \leqq 2.2V$ | | $V_{CC(PD)}$ | | V |
| $I_{CC(PD)}$ | Power-down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 10 | μA |

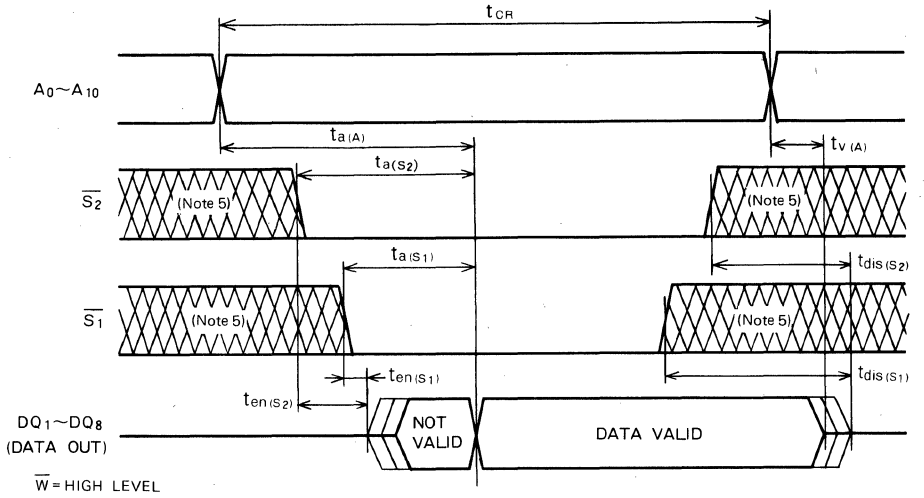
Note 3: When $\overline{S_2}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

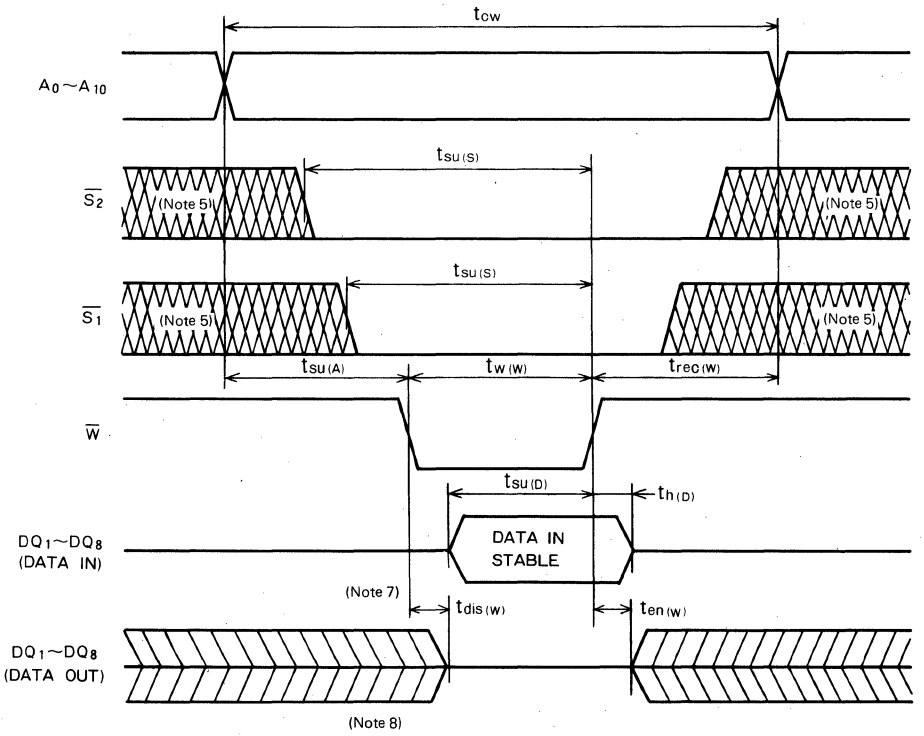
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

## TIMING DIAGRAM

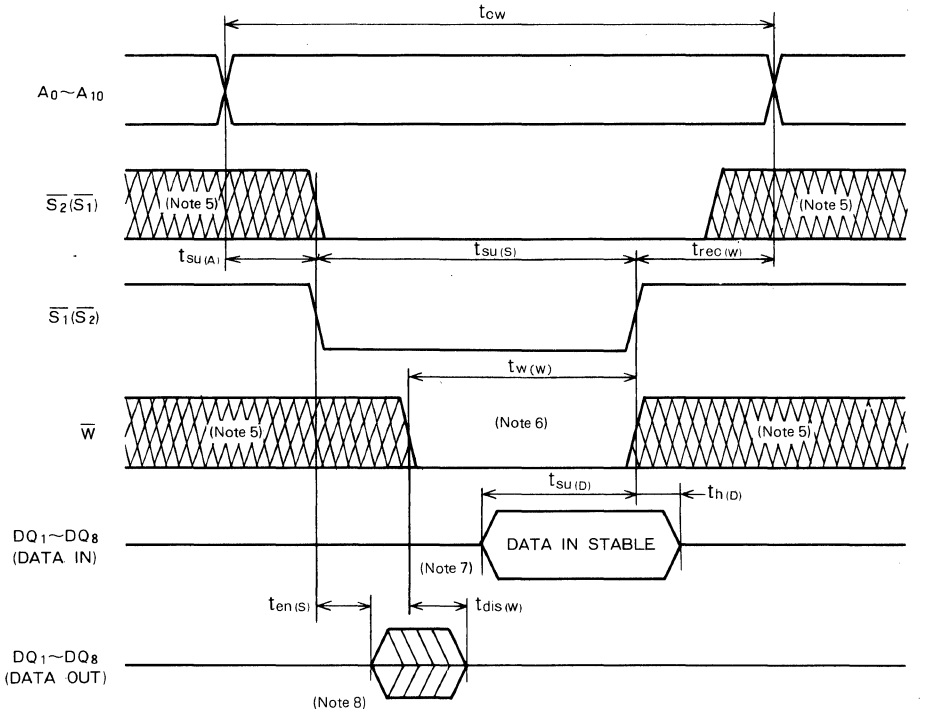
### Read cycle




### Write cycle ($\overline{W}$ control)



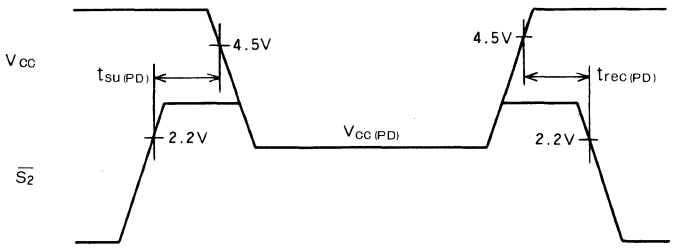
## Write cycle ($\overline{S}$ control)




Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1 TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ falls.
8: A reverse-phase signal should not be supplied when DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS



# M5M5116FP, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5116FP series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery backup.

Two chip select inputs are available: $\overline{S_2}$ provides the minimum standby current with battery back-up while $\overline{S_1}$ enables high-speed memory access.

The series is packaged in a small 24-pin plastic DIL flat package.

## FEATURES

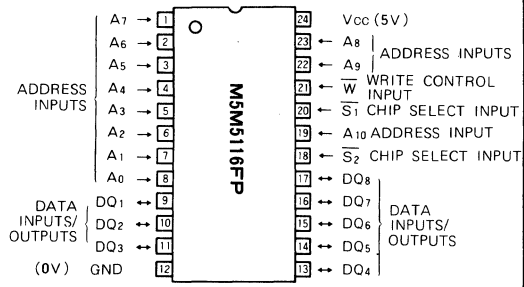
| Type name | Access time (max) | $\overline{S_1}$ access time (max) | Current consumption | |
|---|---|---|---|---|
| | | | Active (max) | Stand-by (max) |
| M5M5116FP-15 | 150ns | 80ns | 50mA | 15μA |
| M5M5116FP | 200ns | 100ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins.

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)




**Outline 24P2W**

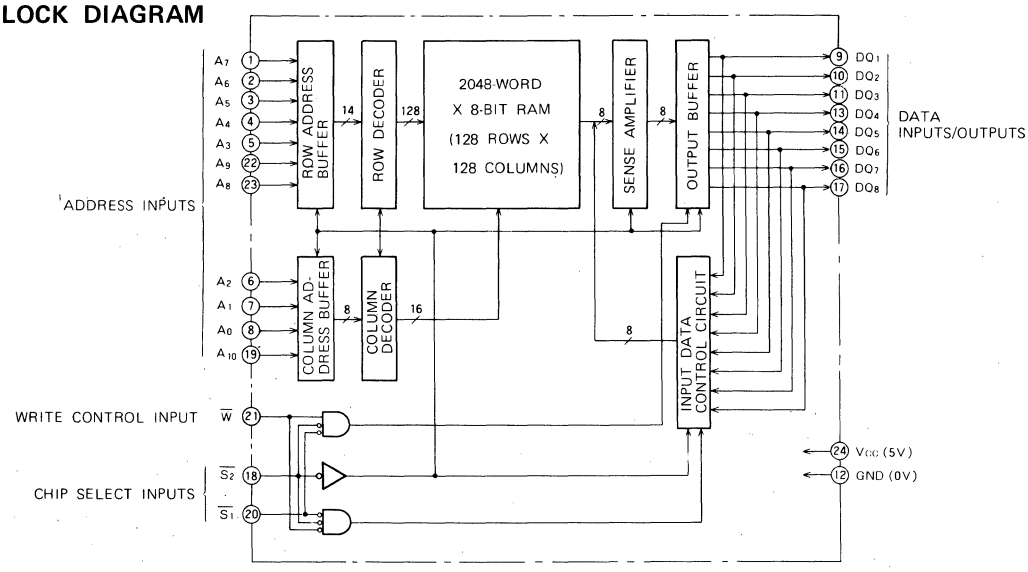
## FUNCTION

The M5M5116FP series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use.

The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S_1}$ and $\overline{S_2}$ signals turn low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high,

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

the $\overline{S_1}$ and $\overline{S_2}$ signals are set low, pin DQ is set to the output mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

When signal $\overline{S_1}$ or $\overline{S_2}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins.

The standby mode is established when signal $\overline{S_2}$ is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and the data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

## OPERATION MODES

| $\overline{S_1}$ | $\overline{S_2}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| X | H | X | Non-select | High impedance | Standby |
| H | L | X | Non-select | High impedance | Active |
| L | L | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3～7 | V |
| $V_I$ | Input voltage | | −0.3～$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0～$V_{CC}$ | V |
| Pd | Power dissipation | Ta＝25°C | 700 | mW |
| Topr | Operating free-air ambient temperature | | 0～70 | °C |
| Tstg | Storage temperature | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$＝0～$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S_1}$ or $\overline{S_2}$＝$V_{IH}$, $V_O$＝2.4V～$V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S_1}$ or $\overline{S_2}$＝$V_{IH}$, $V_O$＝0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5116FP-15 | $V_I(\overline{S_1})$＝$V_I(\overline{S_2})$＝0V Output pin open Other inputs＝$V_{CC}$ or 0V | | | 45 | mA |
| | | M5M5116FP | | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5116FP-15 | $V_I(\overline{S_1})$＝$V_I(\overline{S_2})$＝$V_{IL}$ Output pin open Other inputs＝$V_{IH}$ | | | 50 | mA |
| | | M5M5116FP | | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | $\overline{S_2}$＝$V_{CC}$−0.2V, Other inputs＝0～$V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S_2}$＝$V_{IH}$, Other inputs＝0～$V_{CC}$ | | | 2 | mA |
| Ci | Input capacitance (Ta＝25°C) | | $V_I$＝GND, Vi＝25mVrms, f＝1MHz | | | 6 | pF |
| Co | Output capacitance (Ta＝25°C) | | $V_O$＝GND, $V_O$＝25mVrms, f＝1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5116FP-15 | | | M5M5116FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a(S_1)}$ | Chip select 1 access time | | | 80 | | | 100 | ns |
| $t_{a(S_2)}$ | Chip select 2 access time | | | 150 | | | 200 | ns |
| $t_{dis(S_1)}$ | Output disable time from S1 | | | 50 | | | 60 | ns |
| $t_{dis(S_2)}$ | Output disable time from S2 | | | 50 | | | 60 | ns |
| $t_{en(S_1)}$ | Output enable time from S1 | 15 | | | 15 | | | ns |
| $t_{en(S_2)}$ | Output enable time from S2 | 15 | | | 15 | | | ns |
| $t_{v(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5116FP-15 | | | M5M5116FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{cw}$ | Write cycle time | 150 | | | 200 | | | ns |
| $t_{w(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{dis(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I(\overline{S_2})}$ | Chip select input voltage | $2.2V \leqq V_{CC(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC(PD)} \leqq 2.2V$ | | $V_{CC(PD)}$ | | V |
| $I_{CC(PD)}$ | Power-down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 10 | μA |

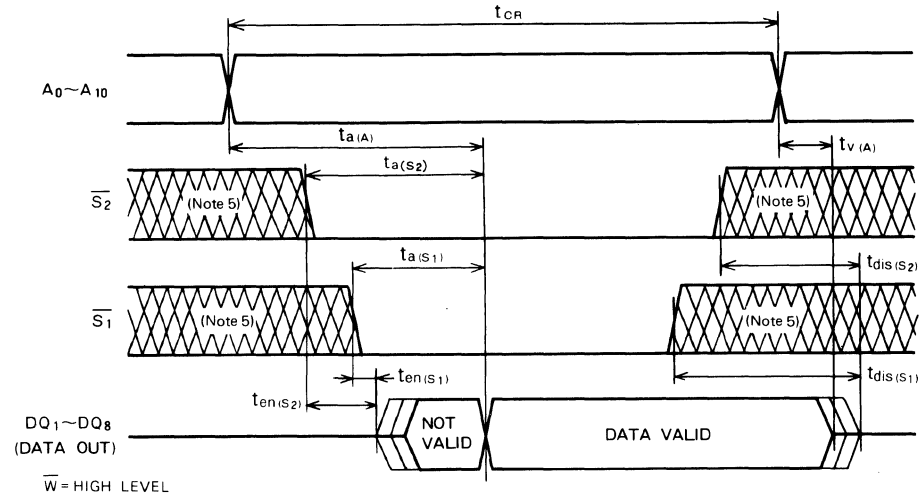
Note 3: When $\overline{S_2}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

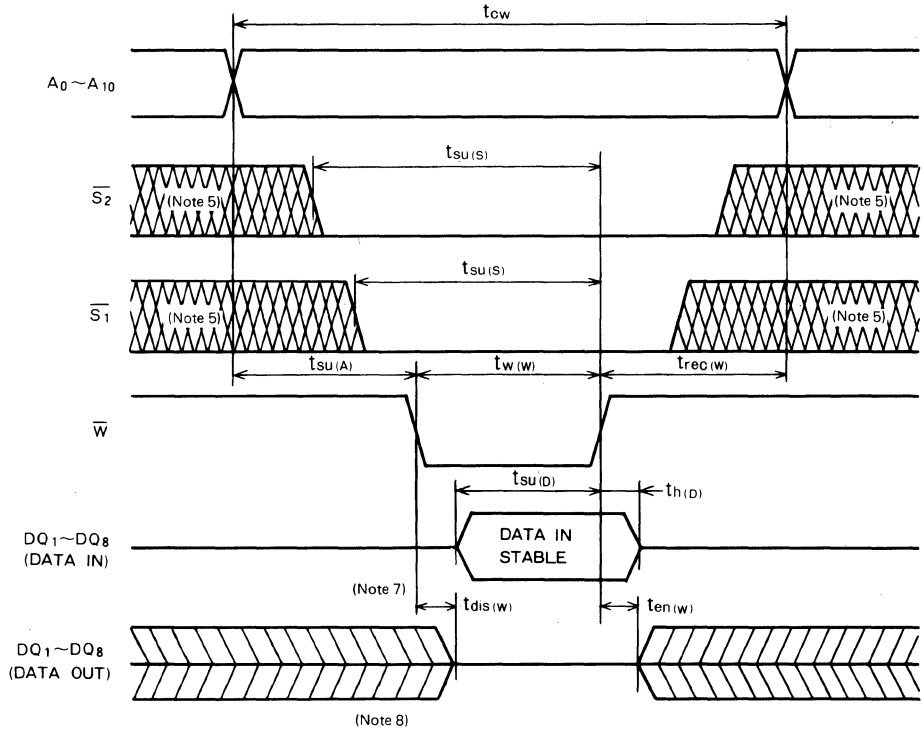
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

## TIMING DIAGRAM

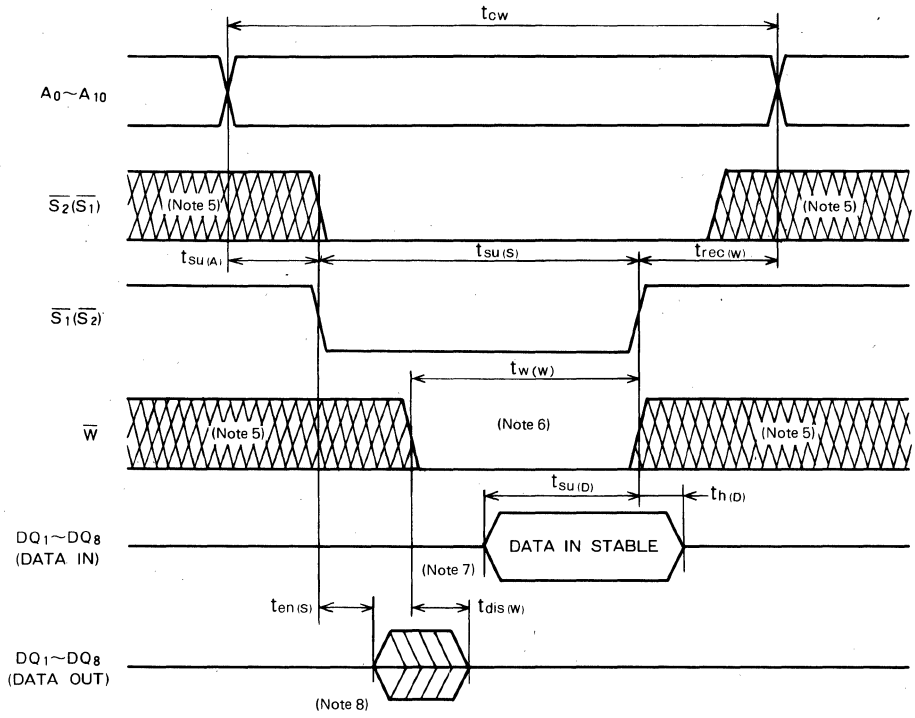
### Read cycle




### Write cycle ($\overline{W}$ control)



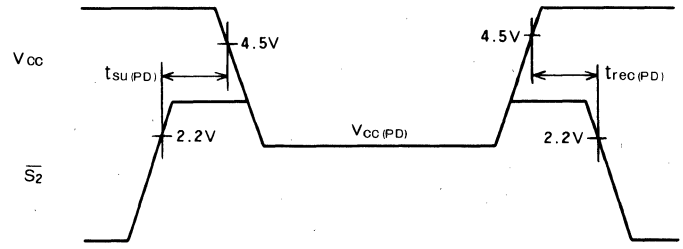
## Write cycle ($\overline{S}$ control)

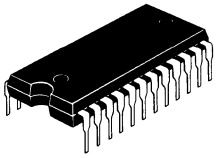



Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1 TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ falls.
8: A reverse-phase signal should not be supplied when DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS







# M5M5117P, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5117P series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery backup.

A chip select input, $\overline{S}$, is available to provide the minimum standby current with battery back-up while an output enable input, $\overline{OE}$, enables high-speed memory access.

The series features pin compatibility with the M5L2716K 16K EPROM and M58725P 16K static RAM, and it is packaged in a standard 24-pin plastic DIL package.

## FEATURES

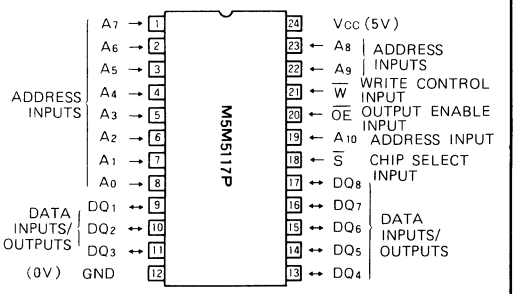
| Type name | Access time (max) | $\overline{OE}$ access time (max) | Current consumption | |
|---|---|---|---|---|
| | | | Active (max) | Stand-by (max) |
| **M5M5117P-15** | 150ns | 80ns | 50mA | 15μA |
| **M5M5117P** | 200ns | 100ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs, and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins.
- Pin compatibility with M5L2716K 16K EPROM and M58725P 16K static RAM.

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)




Outline 24P4

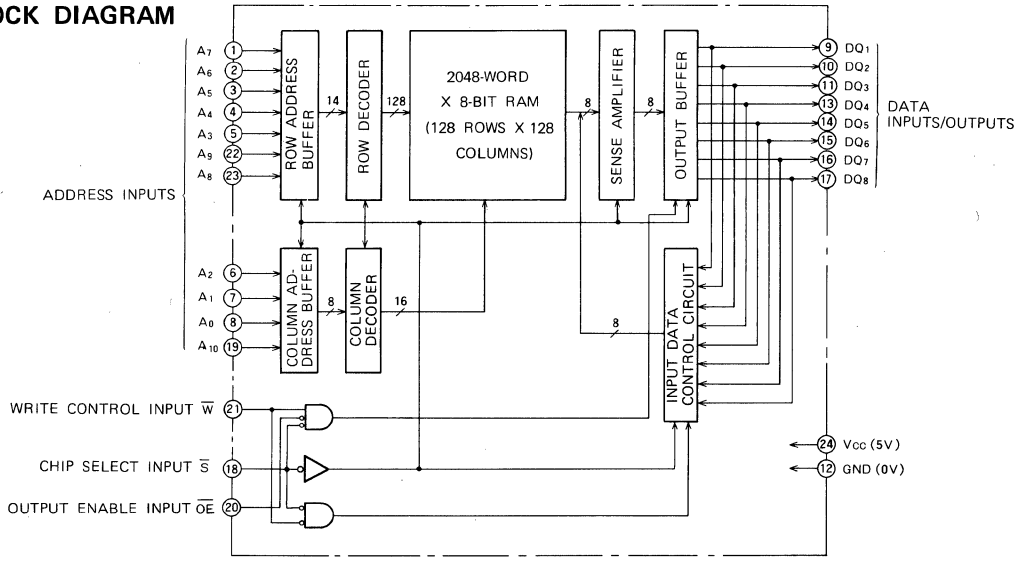
## FUNCTION

The M5M5117P series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use.

The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S}$ signals turns low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high, the $\overline{S}$ and $\overline{OE}$ signals are set low, pin DQ is set to the output mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

## BLOCK DIAGRAM



When signal $\overline{S}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins. When the $\overline{OE}$ signal is set high, the output is put in the floating state. When $\overline{OE}$ is set high during writing for use with an I/O bus system, bus contention between the input and output data can be avoided.

The standby mode is established when signal $\overline{S}$ is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and the data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

## OPERATION MODES

| $\overline{S}$ | $\overline{OE}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| H | X | X | Non-select | High impedance | Standby |
| L | X | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | H | Output disable | High impedance | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3～7 | V |
| $V_I$ | Input voltage | | −0.3～$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0～$V_{CC}$ | V |
| $P_d$ | Power dissipation | $T_a$=25°C | 700 | mW |
| $T_{opr}$ | Operating free-air ambient temperature | | 0～70 | °C |
| $T_{stg}$ | Storage temperature | | −65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_a$=0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

## ELECTRICAL CHARACTERISTICS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$=0～$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S}$ or $\overline{OE}$=$V_{IH}$, $V_O$=2.4V～$V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S}$ or $\overline{OE}$=$V_{IH}$, $V_O$=0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5117P-15 | $V_I(\overline{S})$=0V Output pin open | | | 45 | mA |
| | | M5M5117P | Other inputs=$V_{CC}$ | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5117P-15 | $V_I(\overline{S})$=$V_{IL}$ Output pin open | | | 50 | mA |
| | | M5M5117P | Other inputs=$V_{IH}$ | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | $\overline{S}$=$V_{CC}$−0.2V, Other inputs=0～$V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S}$=$V_{IH}$, Other inputs=0～$V_{CC}$ | | | 2 | mA |
| Ci | Input capacitance ($T_a$=25°C) | | $V_I$=GND, Vi=25mVrms, f=1MHz | | | 6 | pF |
| Co | Output capacitance ($T_a$=25°C) | | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5117P-15 Limits | | | M5M5117P Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a(S)}$ | Chip select access time | | | 150 | | | 200 | ns |
| $t_{a(OE)}$ | Output enable access time | | | 80 | | | 100 | ns |
| $t_{dis(S)}$ | Output disable time from S | | | 50 | | | 60 | ns |
| $t_{dis(OE)}$ | Output disable time from OE | | | 50 | | | 60 | ns |
| $t_{en(S)}$ | Output enable time from S | 15 | | | 15 | | | ns |
| $t_{en(OE)}$ | Output enable time from OE | 15 | | | 15 | | | ns |
| $t_{v(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5117P-15 Limits | | | M5M5117P Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 150 | | | 200 | | | ns |
| $t_{w(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{su(OE)}$ | Output enable set-up time | 40 | | | 40 | | | ns |
| $t_{dis(OE)}$ | Output disable time from OE | | | 50 | | | 60 | ns |
| $t_{dis(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$=0～70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I(S)}$ | Chip select input voltage | 2.2V≦$V_{CC(PD)}$ | 2.2 | | | V |
| | | 2V≦$V_{CC(PD)}$≦2.2V | | $V_{CC(PD)}$ | | V |
| $I_{CC(PD)}$ | Power-down supply current | $V_{CC}$=3V, Other inputs =3V | | | 10 | μA |

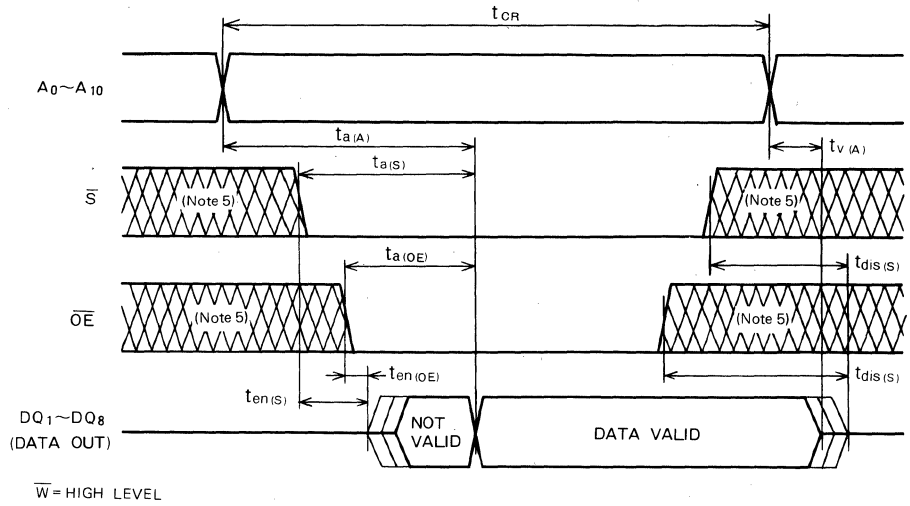
Note 3: When $\overline{S}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$=0～70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{su(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

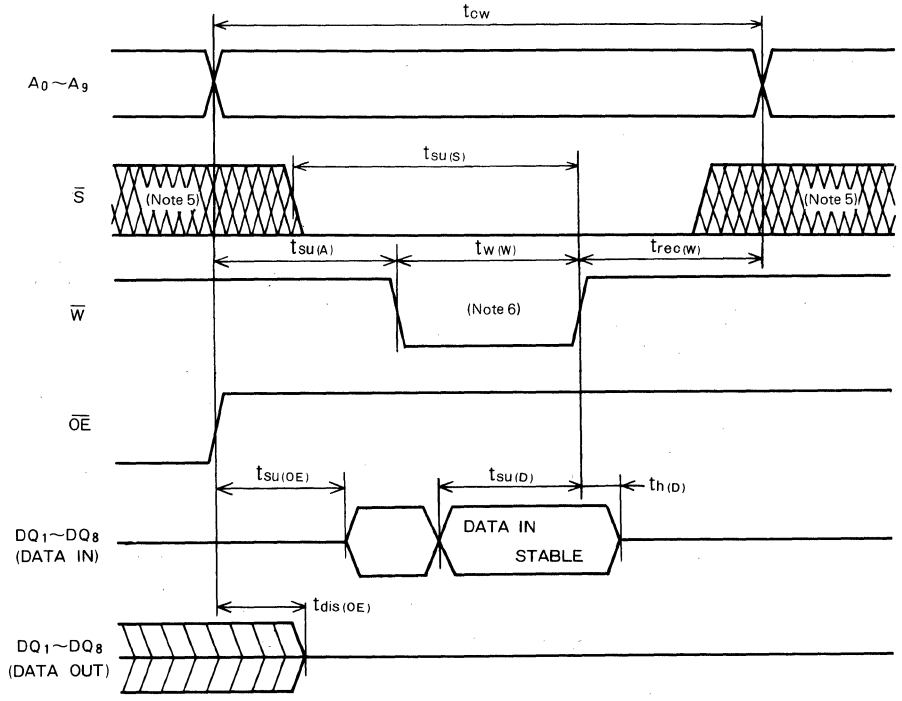
## TIMING DIAGRAM

### Read cycle

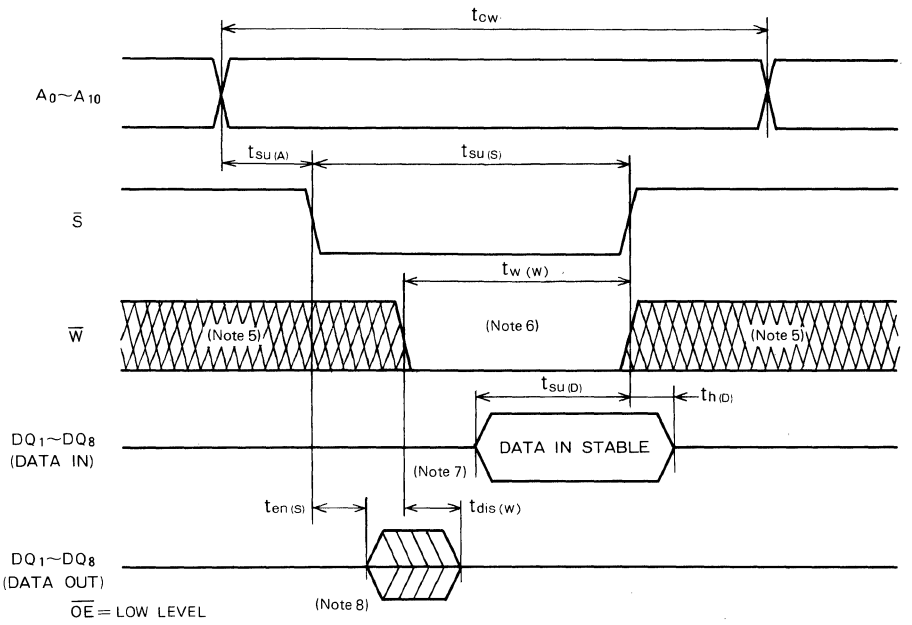



W = HIGH LEVEL

### Write cycle (W control)



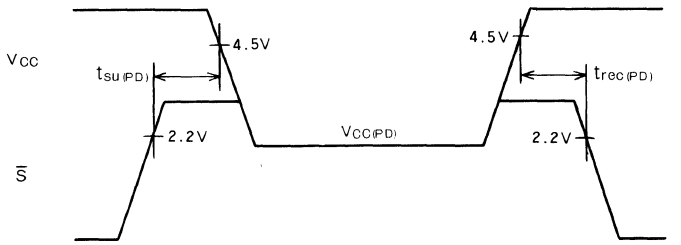
## Write cycle ($\overline{S}$ control)




Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ falls.
8: A reverse phase signal should not be supplied when DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS



# M5M5117FP, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5117FP series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery backup.

A chip select input, $\overline{S}$, is available to provide the minimum standby current with battery back-up while an output enable input, $\overline{OE}$, enables high-speed memory access.

The series features pin compatibility with the M5L2716K 16K EPROM and M58725P 16K static RAM, and it is packaged in a small 24-pin plastic DIL flat package.

## FEATURES

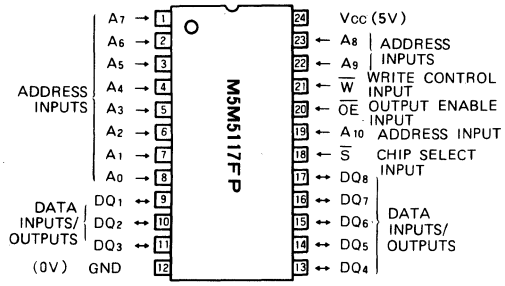
| Type name | Access time (max) | $\overline{OE}$ access time (max) | Current consumption | |
|---|---|---|---|---|
| | | | Active (max) | Stand-by (max) |
| M5M5117FP-15 | 150ns | 80ns | 50mA | 15μA |
| M5M5117FP | 200ns | 100ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs, and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins.
- Pin compatibility with M5L2716K 16K EPROM and M58725P 16K static RAM.

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)




**Outline 24P2W**

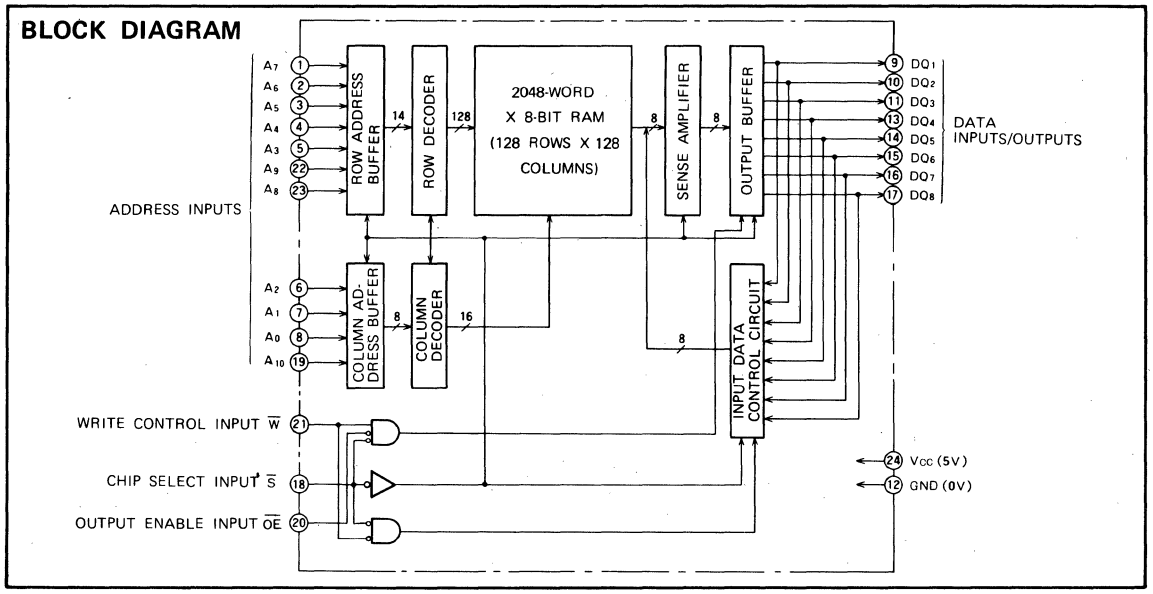
## FUNCTION

The M5M5117FP series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use.

The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S}$ signals turns low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high, the $\overline{S}$ and $\overline{OE}$ signals are set low, pin DQ is set to the output mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

When signal $\overline{S}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins. When the $\overline{OE}$ signal is set high, the output is put in the floating state. When $\overline{OE}$ is set high during writing for use with an I/O bus system, bus contention between the input and output data can be avoided.

The standby mode is established when signal $\overline{S}$ is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and the data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

### OPERATION MODES

| $\overline{S}$ | $\overline{OE}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| H | X | X | Non-select | High impedance | Standby |
| L | X | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | H | Output disable | High impedance | Active |

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3～7 | V |
| $V_I$ | Input voltage | With respect to GND | −0.3～$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | With respect to GND | 0～$V_{CC}$ | V |
| Pd | Power dissipation | Ta=25°C | 700 | mW |
| Topr | Operating free-air ambient temperature | | 0～70 | °C |
| Tstg | Storage temperature | | −65～150 | °C |

### RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

### ELECTRICAL CHARACTERISTICS (Ta=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$=0～$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S}$ or $\overline{OE}$=$V_{IH}$, $V_O$=2.4V～$V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S}$ or $\overline{OE}$=$V_{IH}$, $V_O$=0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5117FP-15 | $V_I(\overline{S})$=0V Output pin open | | | 45 | mA |
| | | M5M5117FP | Other inputs=$V_{CC}$ | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5117FP-15 | $V_I(\overline{S})$=$V_{IL}$ Output pin open | | | 50 | mA |
| | | M5M5117FP | Other inputs=$V_{IH}$ | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | $\overline{S}$=$V_{CC}$−0.2V, Other inputs=0～$V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S}$=$V_{IH}$, Other inputs=0～$V_{CC}$ | | | 2 | mA |
| Ci | Input capacitance (Ta=25°C) | | $V_I$=GND, Vi=25mVrms, f=1MHz | | | 6 | pF |
| Co | Output capacitance (Ta=25°C) | | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5117FP-15 | | | M5M5117FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a\,(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a\,(S)}$ | Chip select access time | | | 150 | | | 200 | ns |
| $t_{a\,(OE)}$ | Output enable access time | | | 80 | | | 100 | ns |
| $t_{dis\,(S)}$ | Output disable time from S | | | 50 | | | 60 | ns |
| $t_{dis\,(OE)}$ | Output disable time from OE | | | 50 | | | 60 | ns |
| $t_{en\,(S)}$ | Output enable time from S | 15 | | | 15 | | | ns |
| $t_{en\,(OE)}$ | Output enable time from OE | 15 | | | 15 | | | ns |
| $t_{v\,(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5117FP-15 | | | M5M5117FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 150 | | | 200 | | | ns |
| $t_{w\,(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su\,(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su\,(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su\,(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h\,(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec\,(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{su\,(OE)}$ | Output enable set-up time | 40 | | | 40 | | | ns |
| $t_{dis\,(OE)}$ | Output disable time from OE | | | 50 | | | 60 | ns |
| $t_{dis\,(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en\,(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC\,(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I\,(S)}$ | Chip select input voltage | $2.2V \leqq V_{CC\,(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC\,(PD)} \leqq 2.2V$ | | $V_{CC\,(PD)}$ | | V |
| $I_{CC\,(PD)}$ | Power-down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 10 | μA |

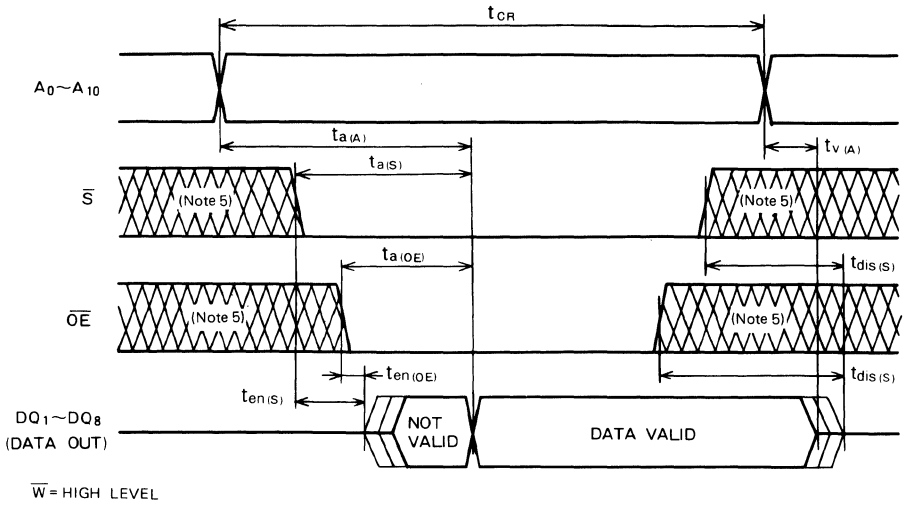
Note 3: When $\overline{S}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC\,(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su\,(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec\,(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

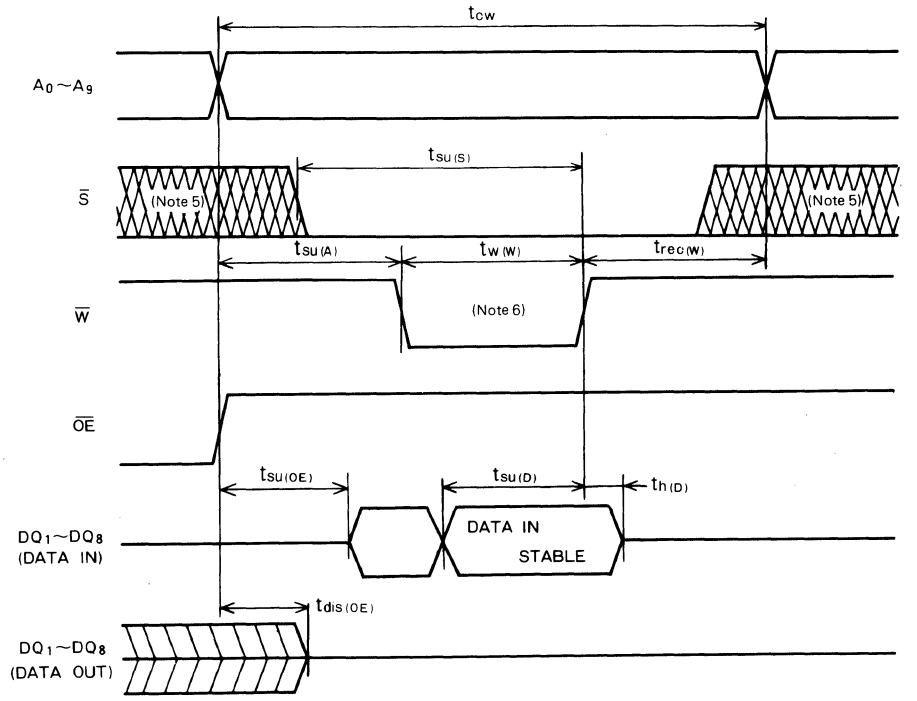
## TIMING DIAGRAM

### Read cycle

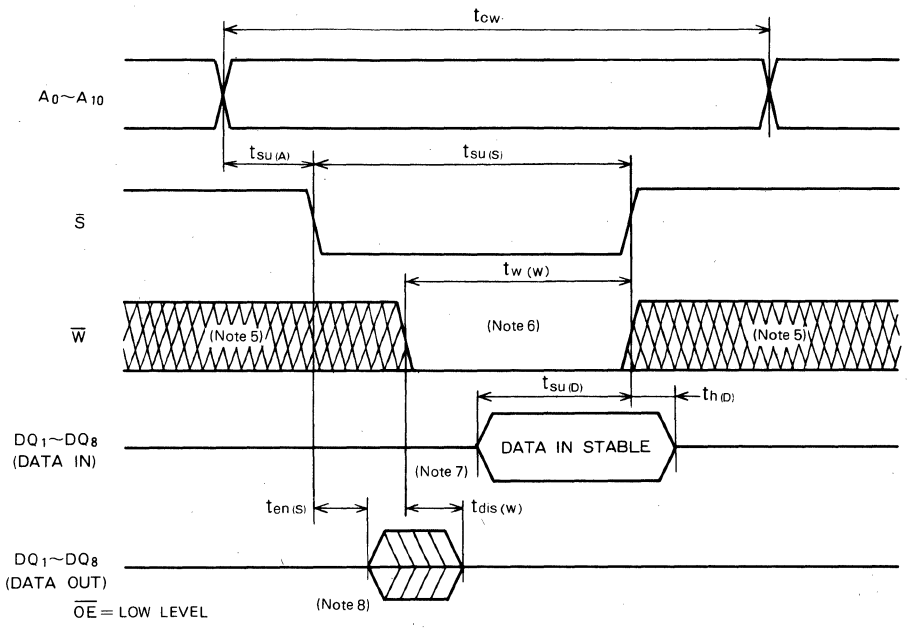



W = HIGH LEVEL

### Write cycle (W control)



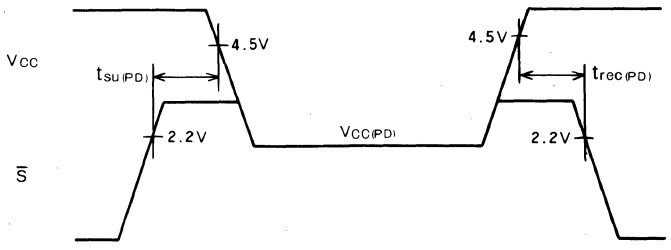
## Write cycle ($\overline{S}$ control)

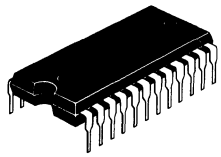



Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ falls.
8: A reverse phase signal should not be supplied when DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS







# M5M5118P, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5118P series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery back-up.

Two chip select inputs, $\overline{S_1}$ and $\overline{S_2}$, are available to provide the minimum standby current with battery back-up. The series is packaged in a standard 24-pin plastic DIL package.

## FEATURES

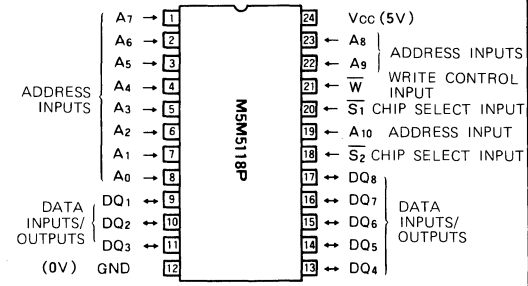
| Type name | Access time (max) | Current consumption | |
|---|---|---|---|
| | | Active (max) | Stand-by (max) |
| M5M5118P-15 | 150ns | 50mA | 15 $\mu$A |
| M5M5118P | 200ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)



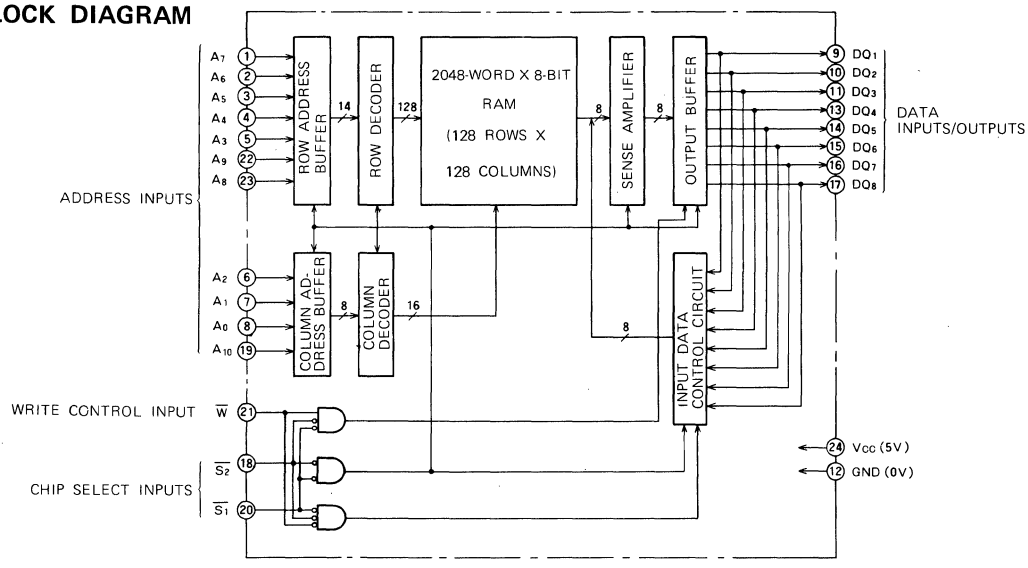

Outline 24 P4

## FUNCTION

The M5M5118P series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use. The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S_1}$ and $\overline{S_2}$ signals turn low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high, the $\overline{S_1}$ and $\overline{S_2}$ signals are set low, pin DQ is set to the output

## BLOCK DIAGRAM



mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

When signal $\overline{S_1}$ or $\overline{S_2}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins.

The standby mode is established when signal $\overline{S_2}$, or signal $\overline{S_1}$ (with signal $\overline{S_2}$ at $V_{CC}$ or GND), is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

## OPERATION MODES

| $\overline{S_1}$ | $\overline{S_2}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| X | H | X | Non-select | High impedance | Standby |
| H | X | X | Non-select | High impedance | Standby |
| L | L | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3～7 | V |
| $V_I$ | Input voltage | | −0.3～$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0～$V_{CC}$ | V |
| Pd | Power dissipation | Ta=25°C | 700 | mW |
| Topr | Operating free-air ambient temperature | | 0～70 | °C |
| Tstg | Storage temperature | | −60～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

## ELECTRICAL CHARACTERISTICS (Ta=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=−1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$=0～$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S_1}$ or $\overline{S_2}$=$V_{IH}$, $V_O$=2.4V～$V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S_1}$ or $\overline{S_2}$=$V_{IH}$, $V_O$=0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5118P-15 | $V_I(\overline{S_1})$=$V_I(\overline{S_2})$=0V Output pin open | | | 45 | mA |
| | | M5M5118P | Other inputs=$V_{CC}$ | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5118P-15 | $V_I(\overline{S_1})$=$V_I(\overline{S_2})$=$V_{IL}$ Output pin open | | | 50 | mA |
| | | M5M5118P | Other inputs=$V_{IH}$ | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | ① $\overline{S_2}$=$V_{CC}$−0.2V, Other inputs=0～$V_{CC}$<br>② $\overline{S_1}$=$V_{CC}$−0.2V, $\overline{S_2}$≦0.2V, Other inputs=0～$V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S_2}$≦0.2V, $\overline{S_1}$=$V_{IH}$, Other inputs=0～$V_{CC}$ | | | 2 | mA |
| $C_i$ | Input capacitance (Ta=25°C) | | $V_I$=GND, Vi=25mVrms, f=1MHz | | | 6 | pF |
| Co | Output capacitance (Ta=25°C) | | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}$ = 5V, $T_a$ = 25°C.



MITSUBISHI ELECTRIC

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5118P-15 | | | M5M5118P | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a(S_1)}$ | Chip select 1 access time | | | 150 | | | 200 | ns |
| $t_{a(S_2)}$ | Chip select 2 access time | | | 150 | | | 200 | ns |
| $t_{dis(S_2)}$ | Output disable time from S1 | | | 50 | | | 60 | ns |
| $t_{dis(S_1)}$ | Output disable time from S2 | | | 50 | | | 60 | ns |
| $t_{en(S_1)}$ | Output enable time from S1 | 15 | | | 15 | | | ns |
| $t_{en(S_2)}$ | Output enable time from S2 | 15 | | | 15 | | | ns |
| $t_{v(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5118P-15 | | | M5M5118P | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{cw}$ | Write cycle time | 150 | | | 200 | | | nn |
| $t_{w(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{dis(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I(S)}$ | Chip select input voltage | $2.2V \leqq V_{CC(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC(PD)} \leqq 2.2V$ | | $V_{CC(PD)}$ | | V |
| $I_{CC(PD)}$ | Power-down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 10 | μA |

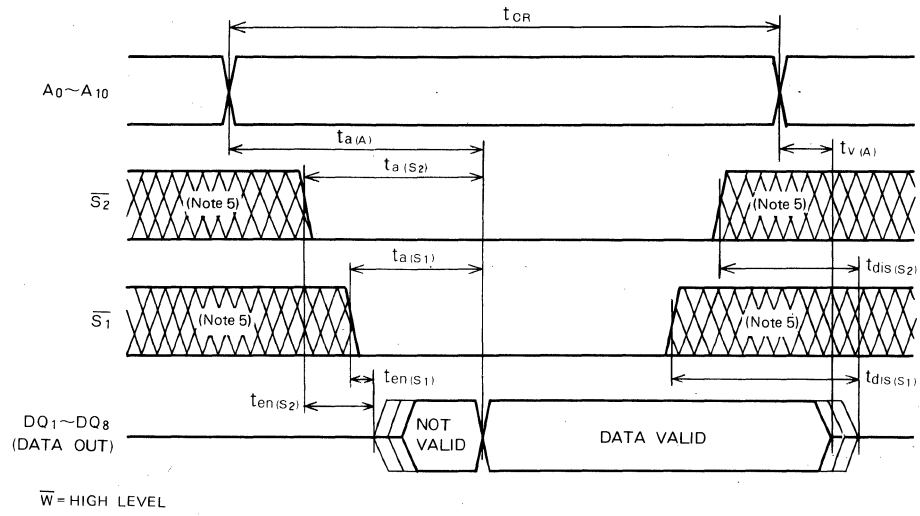
Note 3: When $\overline{S_1}$ or $\overline{S_2}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

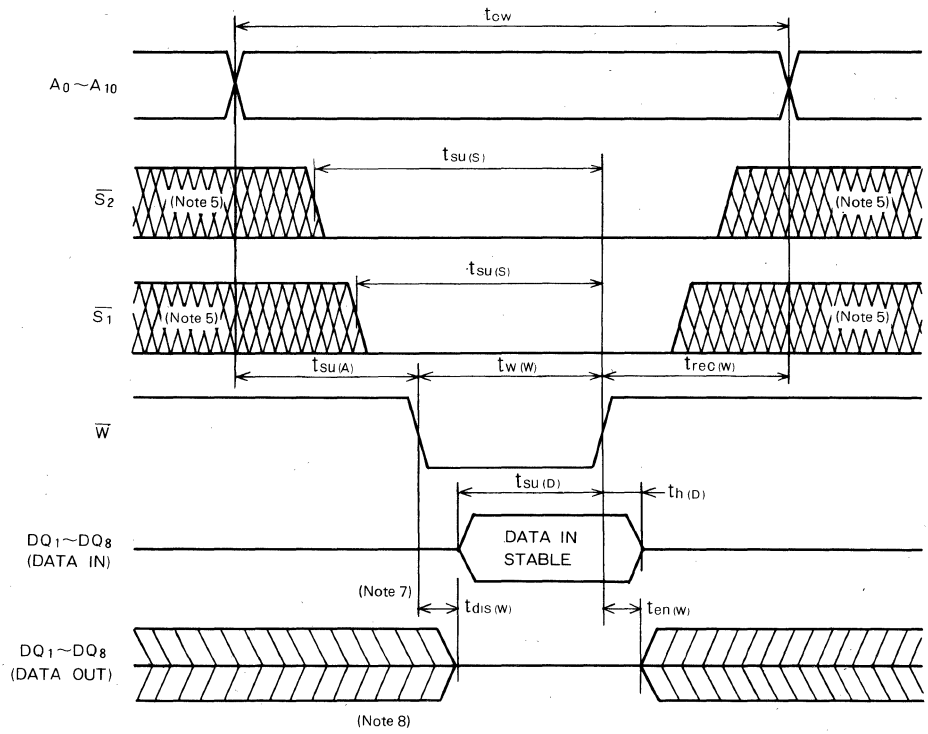
| Symbol | Parameter | Test conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

## TIMING DIAGRAM

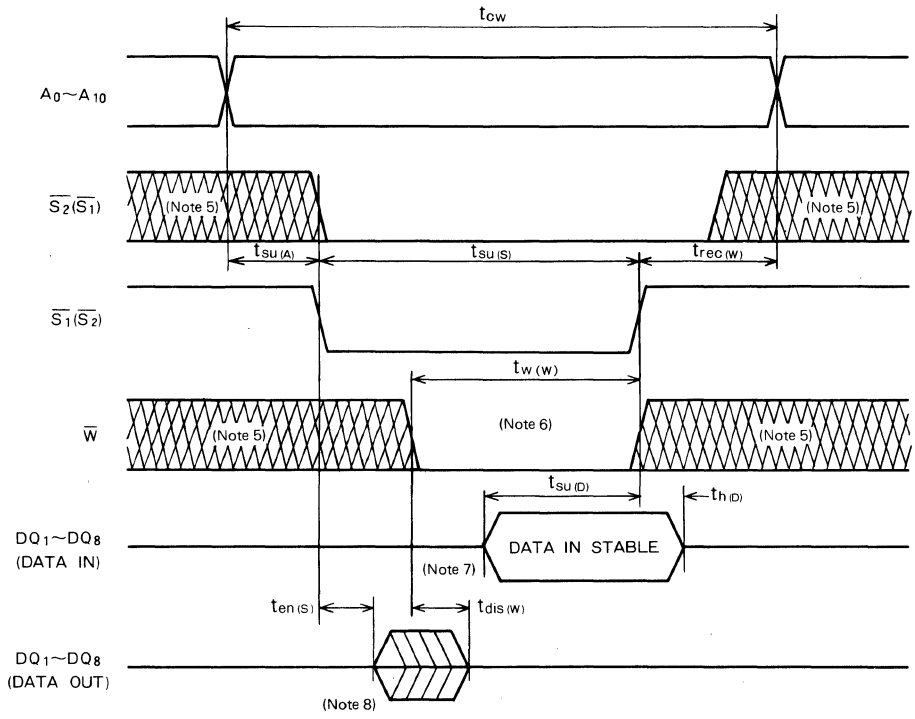
### Read cycle




### Write cycle ($\overline{W}$ control)



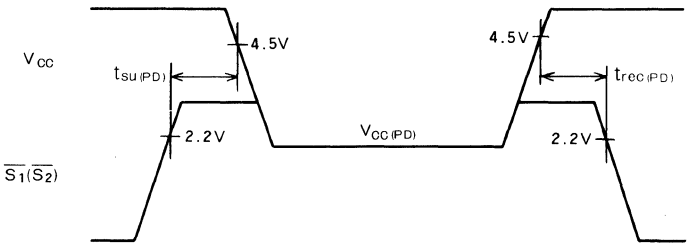
## Write cycle ($\overline{S}$ control)




Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ fall.
8: An reverse-phase signal should not be supplied when pin DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS



# M5M5118FP, -15

## 16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5118FP series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery back-up.

Two chip select inputs, $\overline{S_1}$ and $\overline{S_2}$, are available to provide the minimum standby current with battery back-up.

The series is packaged in a small 24-pin plastic DIL flat package.

## FEATURES

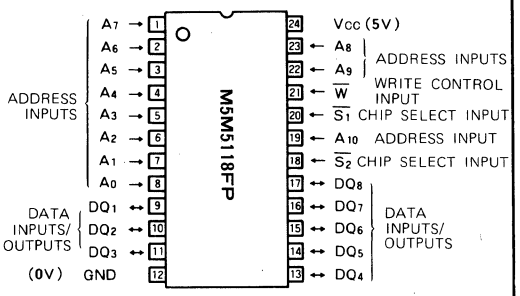
| Type name | Access time (max) | Current consumption | |
|---|---|---|---|
| | | Active (max) | Stand-by (max) |
| M5M5118FP-15 | 150ns | 50mA | 15 $\mu$A |
| M5M5118FP | 200ns | | |

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins

## APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

## PIN CONFIGURATION (TOP VIEW)



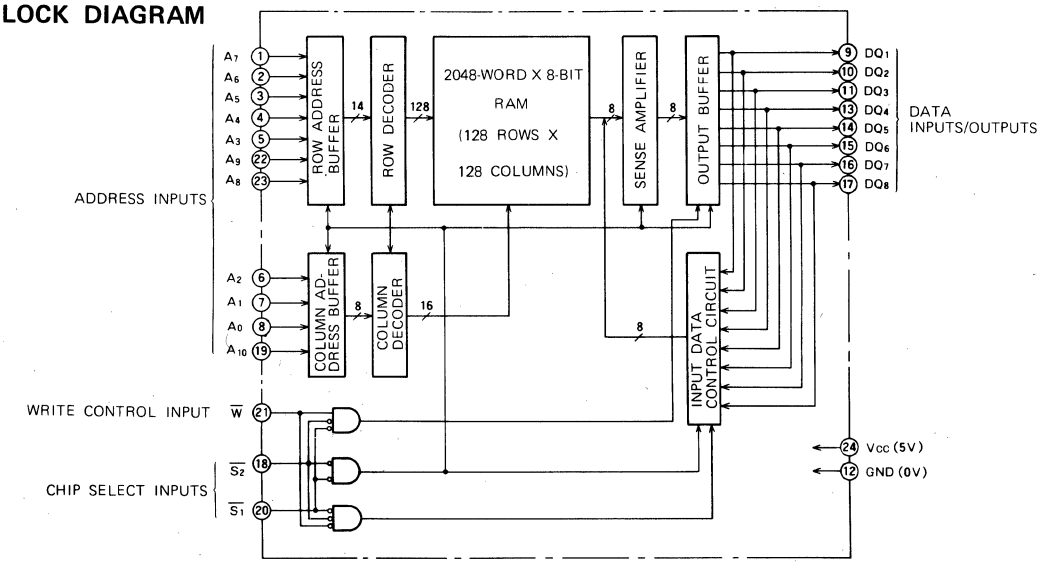

Outline 24P2W

## FUNCTION

The M5M5118FP series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use. The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S_1}$ and $\overline{S_2}$ signals turn low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high, the $\overline{S_1}$ and $\overline{S_2}$ signals are set low, pin DQ is set to the output

## BLOCK DIAGRAM



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mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

When signal $\overline{S_1}$ or $\overline{S_2}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins.

The standby mode is established when signal $\overline{S_2}$, or signal $\overline{S_1}$ (with signal $\overline{S_2}$ at $V_{CC}$ or GND), is set to $V_{CC}$. The supply current is now reduced to the very low level of 15μA (max) and data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

## OPERATION MODES

| $\overline{S_1}$ | $\overline{S_2}$ | $\overline{W}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| X | H | X | Non-select | High impedance | Standby |
| H | X | X | Non-select | High impedance | Standby |
| L | L | L | Write | $D_{IN}$ | Active |
| L | L | H | Read | $D_{OUT}$ | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3 ~ 7 | V |
| $V_I$ | Input voltage | With respect to GND | −0.3 ~ $V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | With respect to GND | 0 ~ $V_{CC}$ | V |
| $P_d$ | Power dissipation | Ta = 25°C | 700 | mW |
| $T_{opr}$ | Operating free-air ambient temperature | | 0 ~ 70 | °C |
| $T_{stg}$ | Storage temperature | | −60 ~ 150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | 2.2 | | $V_{CC}$+0.3 | V |

## ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −1mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 2.1mA | | | 0.4 | V |
| $I_I$ | Input current | | $V_I$ = 0 ~ $V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | Off-state high-level output current | | $\overline{S_1}$ or $\overline{S_2}$ = $V_{IH}$, $V_O$ = 2.4V ~ $V_{CC}$ | | | 1 | μA |
| $I_{OZL}$ | Off-state low-level output current | | $\overline{S_1}$ or $\overline{S_2}$ = $V_{IH}$, $V_O$ = 0V | | | −1 | μA |
| $I_{CC1}$ | Supply current | M5M5118FP-15 | $V_I(\overline{S_1})$ = $V_I(\overline{S_2})$ = 0V Output pin open Other inputs = $V_{CC}$ | | | 45 | mA |
| | | M5M5118FP | | | 30 | 45 | mA |
| $I_{CC2}$ | Supply current | M5M5118FP-15 | $V_I(\overline{S_1})$ = $V_I(\overline{S_2})$ = $V_{IL}$ Output pin open Other inputs = $V_{IH}$ | | | 50 | mA |
| | | M5M5118FP | | | 35 | 50 | mA |
| $I_{CC3}$ | Standby supply current | | ① $\overline{S_2}$ = $V_{CC}$ − 0.2V, Other inputs = 0 ~ $V_{CC}$ ② $\overline{S_1}$ = $V_{CC}$ − 0.2V, $\overline{S_2}$ ≦ 0.2V, Other inputs = 0 ~ $V_{CC}$ | | | 15 | μA |
| $I_{CC4}$ | Standby supply current | | $\overline{S_2}$ ≦ 0.2V, $\overline{S_1}$ = $V_{IH}$, Other inputs = 0 ~ $V_{CC}$ | | | 2 | mA |
| $C_i$ | Input capacitance (Ta = 25°C) | | $V_I$ = GND, Vi = 25mVrms, f = 1MHz | | | 6 | pF |
| $C_o$ | Output capacitance (Ta = 25°C) | | $V_O$ = GND, $V_O$ = 25mVrms, f = 1MHz | | | 8 | pF |

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}$ = 5V, $T_a$ = 25°C.

## SWITCHING CHARACTERISTICS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### READ CYCLE

| Symbol | Parameter | M5M5118FP-15 | | | M5M5118FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 150 | | | 200 | | | ns |
| $t_{a(A)}$ | Address access time | | | 150 | | | 200 | ns |
| $t_{a(S_1)}$ | Chip select 1 access time | | | 150 | | | 200 | ns |
| $t_{a(S_2)}$ | Chip select 2 access time | | | 150 | | | 200 | ns |
| $t_{dis(S_2)}$ | Output disable time from S1 | | | 50 | | | 60 | ns |
| $t_{dis(S_1)}$ | Output disable time from S2 | | | 50 | | | 60 | ns |
| $t_{en(S_1)}$ | Output enable time from S1 | 15 | | | 15 | | | ns |
| $t_{en(S_2)}$ | Output enable time from S2 | 15 | | | 15 | | | ns |
| $t_{v(A)}$ | Data valid time from address | 20 | | | 20 | | | ns |

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### WRITE CYCLE

| Symbol | Parameter | M5M5118FP-15 | | | M5M5118FP | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 150 | | | 200 | | | nn |
| $t_{w(W)}$ | Write pulse width | 90 | | | 120 | | | ns |
| $t_{su(A)}$ | Address set-up time | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set-up time | 90 | | | 120 | | | ns |
| $t_{su(D)}$ | Data set-up time | 40 | | | 60 | | | ns |
| $t_{h(D)}$ | Data hold time | 0 | | | 0 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 10 | | | 10 | | | ns |
| $t_{dis(W)}$ | Output disable time from write | | | 50 | | | 60 | ns |
| $t_{en(W)}$ | Output enable time from write | 15 | | | 15 | | | ns |

## POWER-DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power-down supply voltage | | 2 | | | V |
| $V_{I(S)}$ | Chip select input voltage | $2.2V \leqq V_{CC(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC(PD)} \leqq 2.2V$ | | $V_{CC(PD)}$ | | V |
| $I_{CC(PD)}$ | Power-down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 10 | μA |

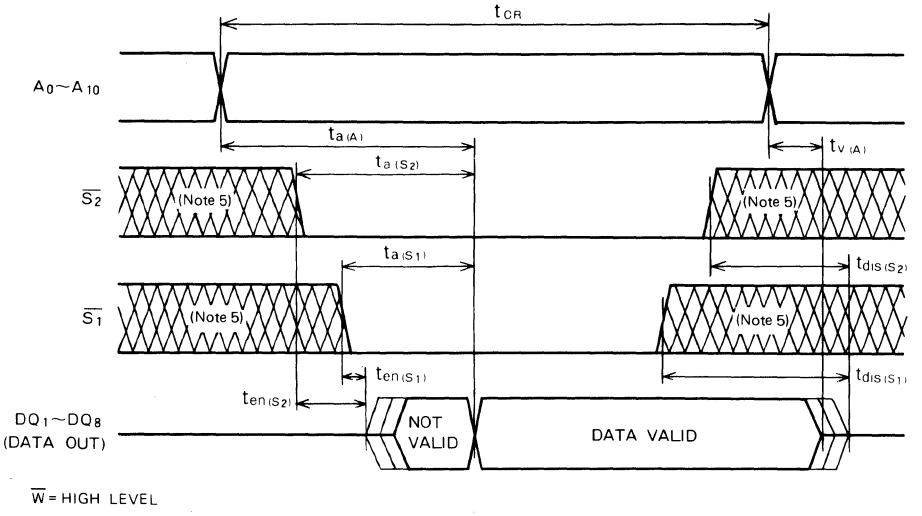
Note 3: When $\overline{S_1}$ or $\overline{S_2}$ is operated at 2.2V ($V_{IH}$ min), the supply current at which $V_{CC(PD)}$ is between 4.5V and 2.4V, is specified by $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

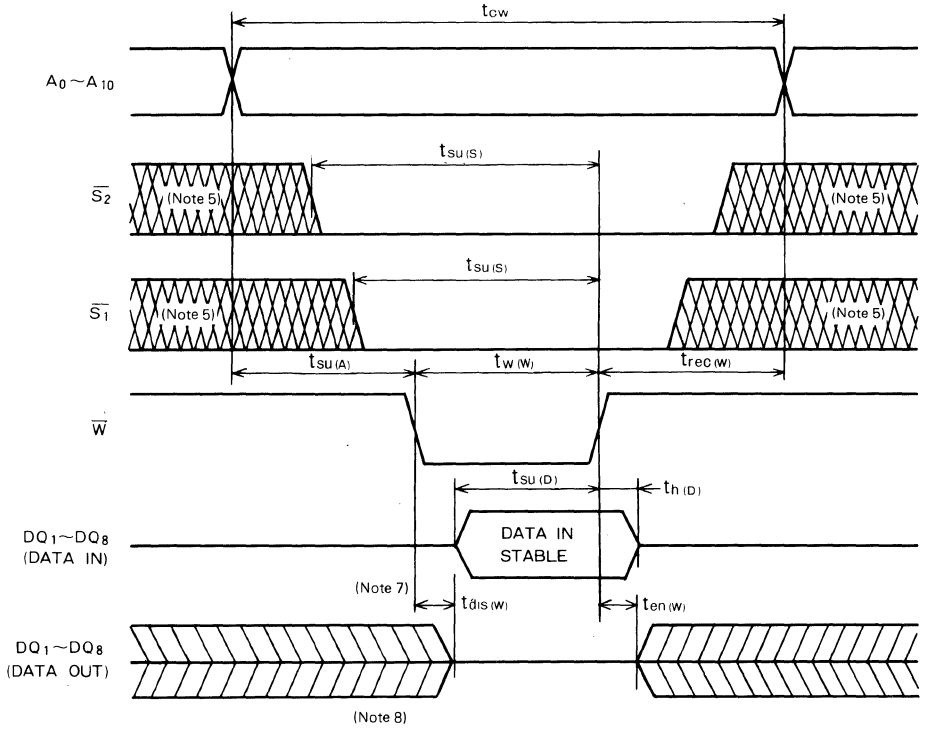
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power-down set-up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power-down recovery time | | $t_{CR}$ | | | ns |

## TIMING DIAGRAM

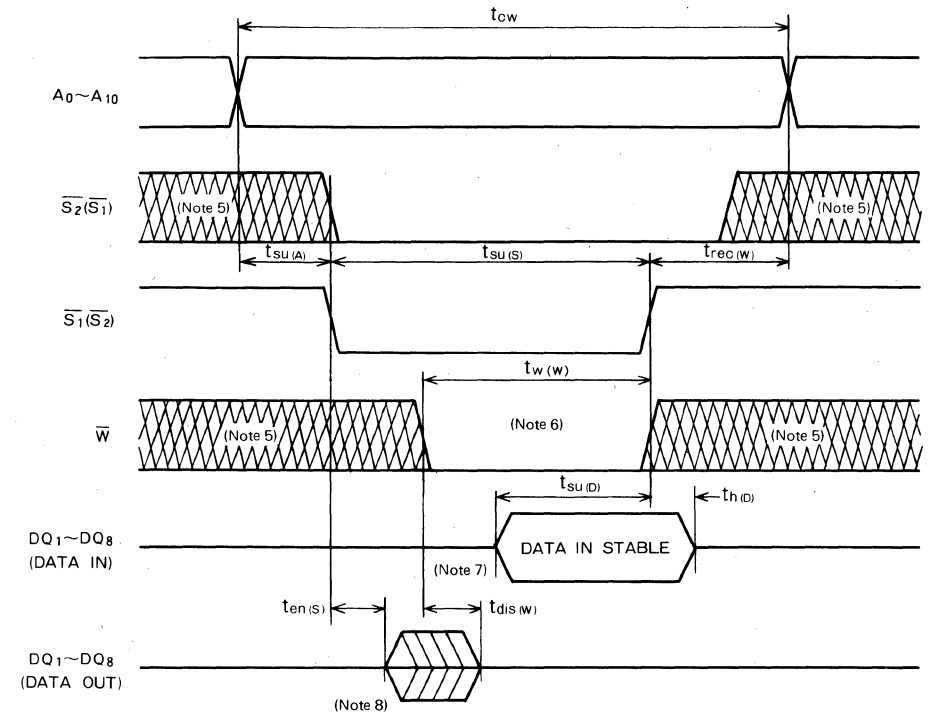
### Read cycle




### Write cycle ($\overline{W}$ control)



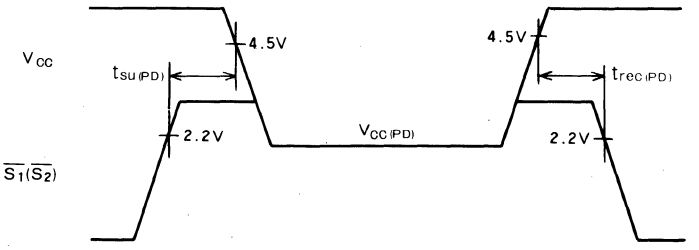
## Write cycle ($\overline{S}$ control)




Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1TTL, $C_L$ = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ fall.
8: An reverse-phase signal should not be supplied when pin DQ is in the output mode.

## POWER-DOWN CHARACTERISTICS





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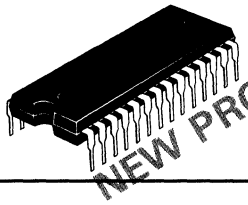



# M5M5165P-70, -10, -12, -15, -70L, -10L, -12L, -15L

## 65536-BIT (8192 WORD BY 8-BIT) CMOS STATIC RAM

Specification of 70, 70L are subject to change.

## DESCRIPTION

The M5M5165P is a 65,536-bit CMOS static RAM organized as 8,192 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 8K x 8-bit pinout.

## FEATURES

| Type | Access time (max) | Power supply current | |
|---|---|---|---|
| | | Active (max) | Stand-by (max) |
| M5M5165P-70 | 70ns | 50 mA | 2mA |
| M5M5165P-10 | 100ns | | |
| M5M5165P-12 | 120ns | | |
| M5M5165P-15 | 150ns | | |
| M5M5165P-70L | 70ns | | 100 $\mu$A |
| M5M5165P-10L | 100ns | | |
| M5M5165P-12L | 120ns | | |
| M5M5165P-15L | 150ns | | |

- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S_1}$, $S_2$
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O
- Pinout Compatible with 64K EPROM M5L2764K

## APPLICATION

Small Capacity Memory Units.

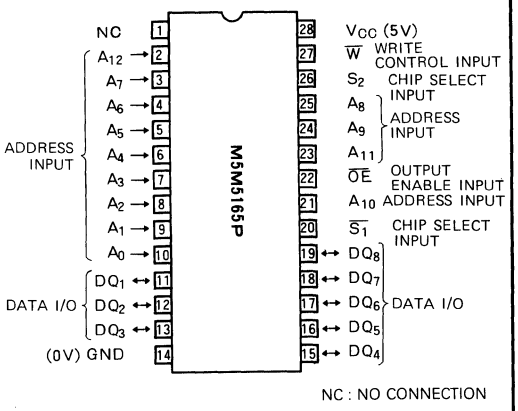
## FUNCTION

The operation mode of the M5M5165P is determined by a combination of the device control inputs $\overline{S_1}$, $S_2$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is excuted whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level $S_2$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or $S_2$, whichever occurs first, requring the set-up and hold time relative to these edge to be maintained. The Output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and $S_2$ are in an active state ($\overline{S_1}$ = L,

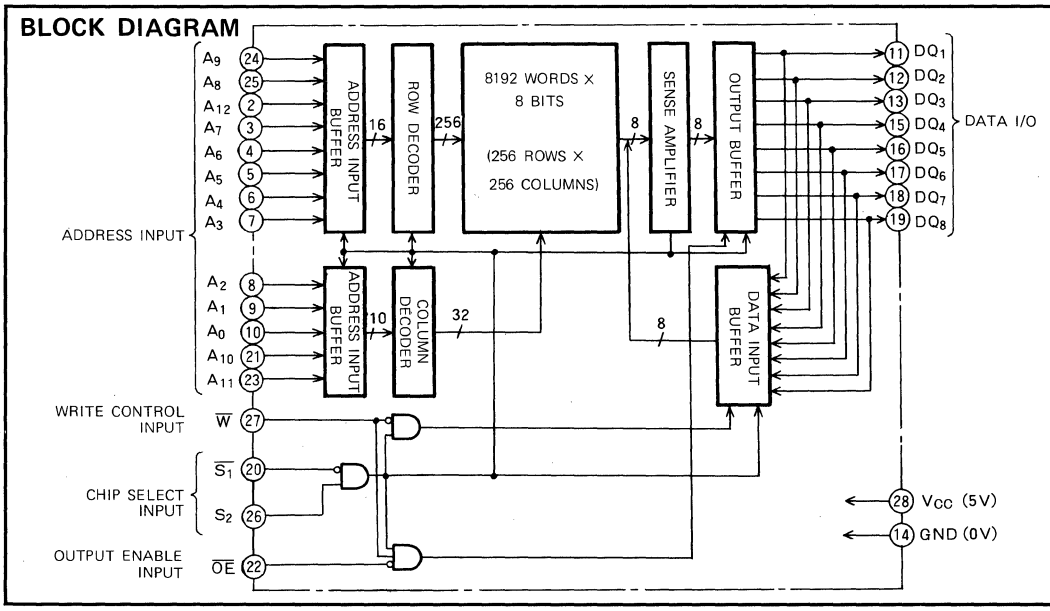
## PIN CONFIGURATION (TOP VIEW)




NC : NO CONNECTION

**Outline 28P4**

## BLOCK DIAGRAM



# M5M5165P-70, -10, -12, -15, -70L, -10L, -12L, -15L

## 65536-BIT (8192 WORD BY 8-BIT) CMOS STATIC RAM

$S_2$=H)

When setting $\overline{S_1}$ at a high level or $S_2$ at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$ and $S_2$. The power supply current is reduced as low as the stand-by current which is specified as $I_{CC3}$ or $I_{CC4}$, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

### FUNCTION TABLE

| $\overline{S_1}$ | $S_2$ | $\overline{W}$ | $\overline{OE}$ | Mode | DQ | $I_{CC}$ |
|---|---|---|---|---|---|---|
| X | L | X | X | Non selection | high-impedance | Standby |
| H | X | X | X | Non selection | high-impedance | Standby |
| L | H | L | X | Write | $D_{IN}$ | Active |
| L | H | H | L | Read | $D_{OUT}$ | Active |
| L | H | H | H | | high-impedance | Active |

### RECOMMENDED OPERATING CONDITIONS ($T_a$=0～70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IL}$ | low input voltage | −0.3 | | 0.8 | V |
| $V_{IH}$ | high input voltage | 2.2 | | $V_{CC}$+0.3 | V |

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3～7 | V |
| $V_I$ | Input voltage | | −0.3～$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0～$V_{CC}$ | V |
| Pd | Power dissipation | $T_a$=25°C | 700 | mW |
| Topr | Operating temperature | | 0～70 | °C |
| Tstg | Storage temperature | | −65～150 | °C |

### ELECTRICAL CHARACTERISTICS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High input voltage | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low input voltage | | −0.3 | | 0.8 | V |
| $V_{OH}$ | High output voltage | $I_{OH}$=−1mA | 2.4 | | | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$=2 mA | | | 0.4 | V |
| $I_I$ | Input current | $V_I$=0～$V_{CC}$ | | | ±1 | μA |
| $I_{OZH}$ | High level output current in off-state | $\overline{S_1}$=$V_{IH}$ or $S_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ | | | 1 | μA |
| $I_{OZL}$ | Low level output current in off-state | $V_{I/O}$=0−$V_{CC}$ | | | −1 | μA |
| $I_{CC1}$ | Active supply current | $\overline{S_1}$≦0.2, $S_2$≧$V_{CC}$−0.2<br>Outout open<br>Other inputs ≦0.2 or ≧$V_{CC}$−0.2 | | 30 | 45 | mA |
| $I_{CC2}$ | Active supply current | $\overline{S_1}$=$V_{IL}$ or $S_2$=$V_{IH}$<br>Output open<br>Other inputs =$V_{IH}$ | | 35 | 50 | mA |
| $I_{CC3}$ | Stand-by supply current | ① $S_2$≦0.2V, Other inputs=0～$V_{CC}$ | | | 2(P) | mA |
| | | ② $\overline{S_1}$≧$V_{CC}$−0.2V, $S_2$≧$V_{CC}$−0.2V, Other inputs =0～$V_{CC}$ | | | 100(P-L) | μA |
| $I_{CC4}$ | Stand-by supply current | $S_2$=$V_{IL}$, $\overline{S_1}$=$V_{IH}$, Other inputs=0～$V_{CC}$ | | | 3 | mA |
| $C_i$ | Output capacitance ($T_a$=25°C) | $V_I$=GND, $V_i$=25mVmrs, f=1MHz | | | 6 | pF |
| $C_o$ | Outout capacitance ($T_a$=25°C) | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is $V_{CC}$=5V, Ta=25°C

## SWITCHING CHARACTERISTICS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

### Read cycle

| Symbol | Parameter | M5M5165P-70 M5M5165P-70L | | | M5M5165P-10 M5M5165P-10L | | | M5M5165P-12 M5M5165P-12L | | | M5M5165P-15 M5M5165P-15L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{CR}$ | Read cycle time | 70 | | | 100 | | | 120 | | | 150 | | | ns |
| $t_{a(A)}$ | Address access time | | | 70 | | | 100 | | | 120 | | | 150 | ns |
| $t_{a(S_1)}$ | Chip select 1 access time | | | 70 | | | 100 | | | 120 | | | 150 | ns |
| $t_{a(S_2)}$ | Chip select 2 access time | | | 70 | | | 100 | | | 120 | | | 150 | ns |
| $t_{a(OE)}$ | Output enable access time | | | 35 | | | 50 | | | 60 | | | 70 | ns |
| $t_{dis(S_1)}$ | Output disable time after $\overline{S_1}$ high | | | 30 | | | 35 | | | 40 | | | 50 | ns |
| $t_{dis(S_2)}$ | Output disable time after $S_2$ low | | | 30 | | | 35 | | | 40 | | | 50 | ns |
| $t_{dis(OE)}$ | Output disable time after $\overline{OE}$ high | | | 30 | | | 35 | | | 40 | | | 50 | ns |
| $t_{en(S_1)}$ | Output enable time after $\overline{S_1}$ low | 5 | | | 10 | | | 10 | | | 10 | | | ns |
| $t_{en(S_2)}$ | Output enable time after $S_2$ high | 5 | | | 10 | | | 10 | | | 10 | | | ns |
| $t_{en(OE)}$ | Output enable time after $\overline{OE}$ low | 5 | | | 10 | | | 10 | | | 10 | | | ns |
| $t_{v(A)}$ | Data valid time after address change | 20 | | | 20 | | | 20 | | | 20 | | | ns |

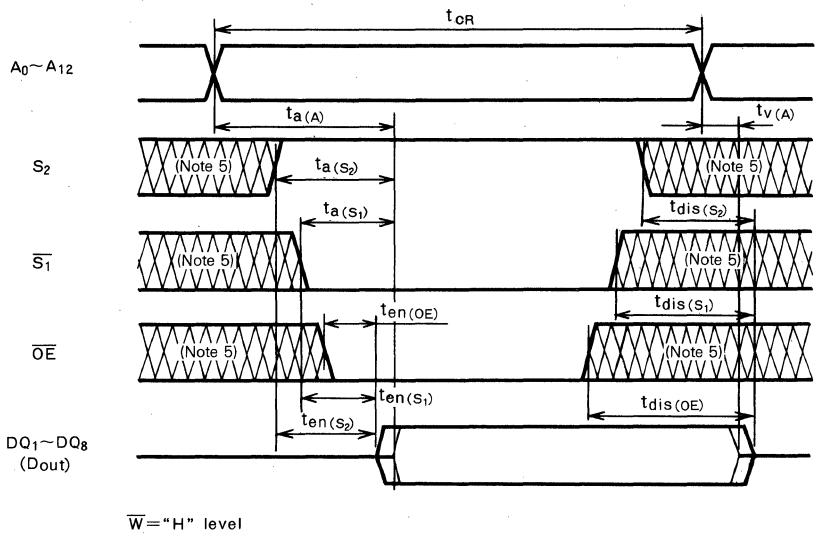
## TIMING REQUIREMENTS ($T_a$=0～70°C, $V_{CC}$=5V±10%, unless otherwise noted)

### Write cycle

| Symbol | Parameter | M5M5165P-70 M5M5165P-70L | | | M5M5165P-10 M5M5165P-10L | | | M5M5165P-12 M5M5165P-12L | | | M5M5165P-15 M5M5165P-15L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Limits | | | Limits | | | Limits | | | Limits | | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{CW}$ | Write cycle time | 70 | | | 100 | | | 120 | | | 150 | | | ns |
| $t_{w(W)}$ | Write pulse width | 40 | | | 60 | | | 70 | | | 90 | | | ns |
| $t_{su(A)}$ | Address set up time | 0 | | | 0 | | | 0 | | | 0 | | | ns |
| $t_{su(S)}$ | Chip select set up time | 65 | | | 80 | | | 85 | | | 100 | | | ns |
| $t_{su(D)}$ | Data set up time | 30 | | | 35 | | | 40 | | | 50 | | | ns |
| $t_{h(D)}$ | Data hold time | 5 | | | 5 | | | 5 | | | 5 | | | ns |
| $t_{rec(W)}$ | Write recovery time | 5 | | | 5 | | | 10 | | | 10 | | | ns |
| $t_{dis(W)}$ | Output disable time after $\overline{W}$ low | 0 | | 30 | | | 35 | | | 40 | | | 50 | ns |
| $t_{dis(OE)}$ | Output disable time after $\overline{OE}$ high | 0 | | 30 | | | 35 | | | 40 | | | 50 | ns |
| $t_{en(W)}$ | Output enable time after $\overline{W}$ high | 5 | | | 10 | | | 10 | | | 10 | | | ns |
| $t_{en(OE)}$ | Output enable time after $\overline{OE}$ low | 5 | | | 10 | | | 10 | | | 10 | | | ns |

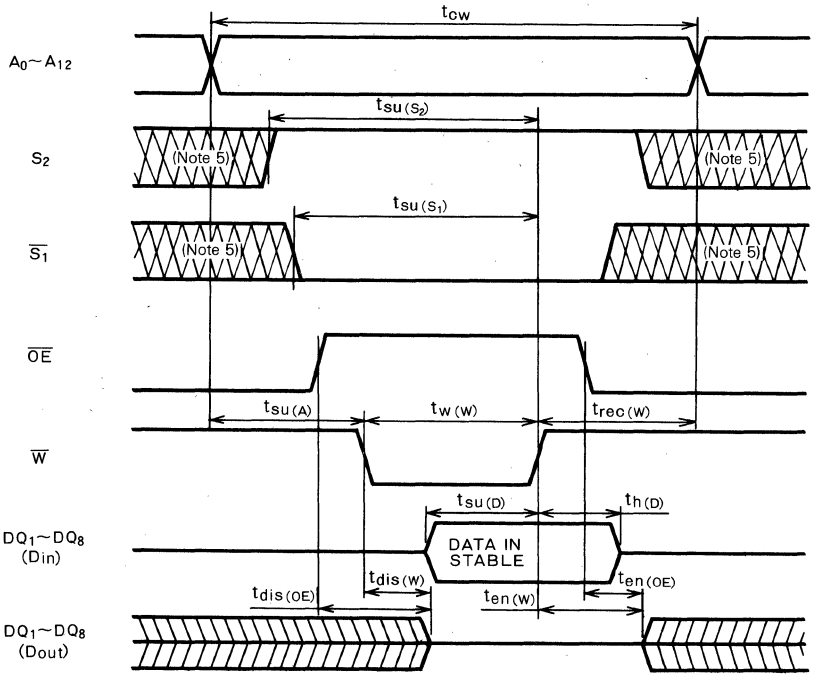
## TIMING DIAGRAM

### Read cycle

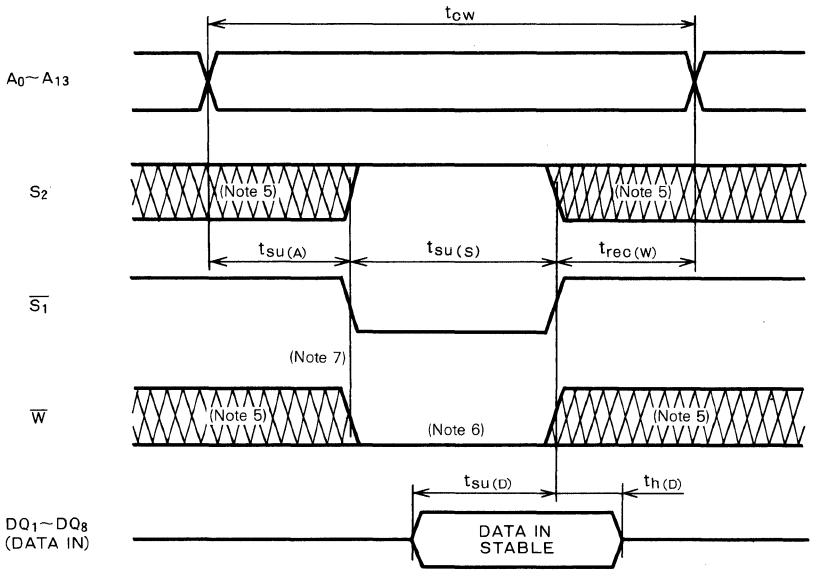



W = "H" level

### Write cycle (WE control)



## Write cycle (S control)




Note 4: Test condition
Input pulse level: 0.6~2.4V
Input pulse rise, fall time: 10ns
Load: 1 TTL, $C_L$ = 100pF (P-15, P-12, P-10, P-15L, P-12L, P-10L)
$C_L$=30pF (P-70, P-70L)
Conditions of assessment: 1.5V
5: Hatching indicates the state is don't care.
6: Writing is executed while $S_2$ high overlaps $\overline{S_1}$ and $\overline{W}$ low.
7: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or $S_2$ high, the output remains in the high-impedance state.
8: Don't apply inverted phase signal externally when DQ pin is in output mode.

## POWER DOWN CHARACTERISTICS

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power down supply voltage | | 2 | | | V |
| $V_{I(\overline{S_1})}$ | Chip select input $\overline{S_1}$ | $2.2V \leqq V_{CC(PD)}$ | 2.2 | | | V |
| | | $2V \leqq V_{CC(PD)} \leqq 2.2V$ | | $V_{CC(PD)}$ | | V |
| $V_{I(S_2)}$ | Chip select input $S_2$ | $4.5V \leqq V_{CC(PD)}$ | | | 0.8 | V |
| | | $V_{CC(PD)} < 4.5V$ | | | 0.2 | V |
| $I_{CC(PD)}$ | Power down supply current | $V_{CC}$ = 3V, Other inputs = 3V | | | 2 (P) | mA |
| | | | | | 50 (P-L) | μA |

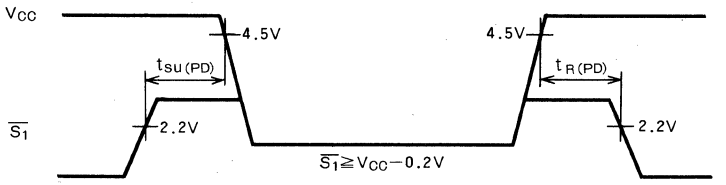
Note 3: When $\overline{S_1}$ is operated at 2.2V ($V_{IH}$ min) and the supply voltage is between 4.5V and 2.4V, supply current is defined as $I_{CC4}$.

## TIMING REQUIREMENTS ($T_a$ = 0 ~ 70°C, unless otherwise noted)

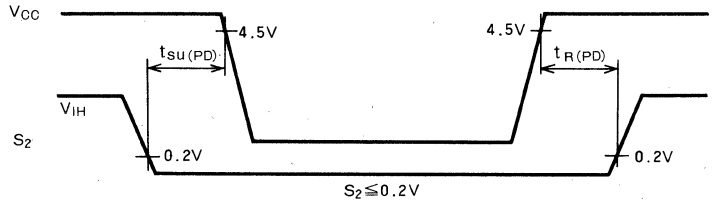
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su\ (PD)}$ | Power down setup time | | 0 | | | ns |
| $t_{rec\ (PD)}$ | Power down recovery time | | $t_{CR}$ | | | ns |

## POWER DOWN CHARACTERISTICS

### $\overline{S_1}$ control

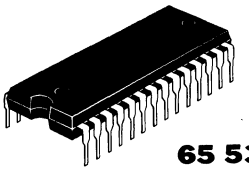



### $S_2$ control



# MOS MASK ROM

5





# M5M2364-XXXP

## 65 536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M2364-XXXP is a 65536-bit mask-programmable high speed read-only memory.

The M5M2364-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIL package. It is interchangeable with the M5L2764K and Intel 2764 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

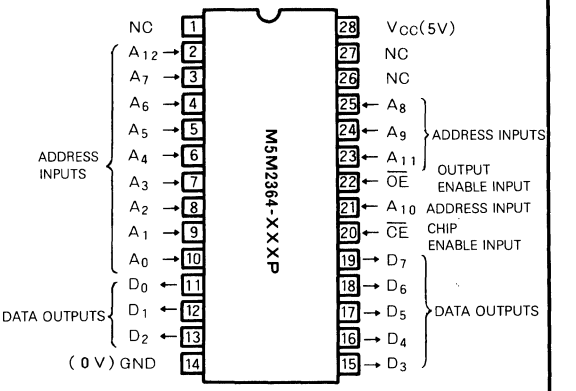
## FEATURES

- 8192 words × 8-bit organization
- Access time ..... 250 ns (MAX)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply
  Current (Icc) active ..... 80 mA (MAX)
  standby ..... 20 mA (MAX)
- Single 5V power supply ($V_{CC}$ = 5V ± 10%)
- 3-State output buffer
- Input and output
- Standard 28-pin DIL package
- Interchangeable with the M5L2764K and Intel 2764

## APPLICATION

- Electronic computers and various software

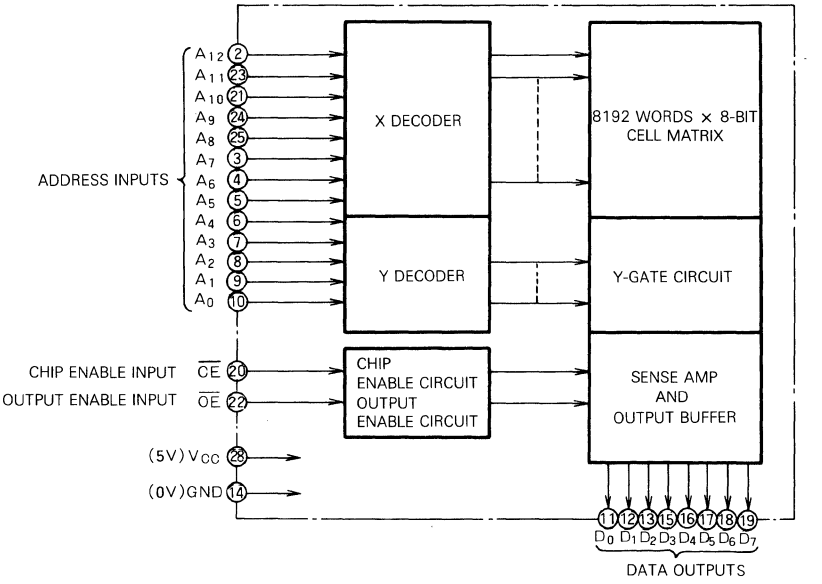
## PIN CONFIGURATION (TOP VIEW)




**Outline** 28P4

NC: NO CONNECTION

## BLOCK DIAGRAM



## 65 536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

### FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level).

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $T_{opr}$ | Operating ambient temperature | | −10~80 | °C |
| $T_{stg}$ | Storage temperature | | −65~150 | °C |
| $V_I$ | Input voltage | With respect to GND | −0.6~7 | V |

### DC ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ | Max | |
| $I_{LI}$ | Input leakage current | $V_{IN}$=5.5V | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=5.5V | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ Supply voltage (Standby) | $\overline{CE}$=$V_{IH}$ | | 10 | 20 | mA |
| $I_{CC2}$ | $V_{CC}$ Supply voltage (Operating) | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | 40 | 80 | mA |
| $V_{IL}$ | Low level input voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | High level input voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$=−400μA | 2.4 | | | V |

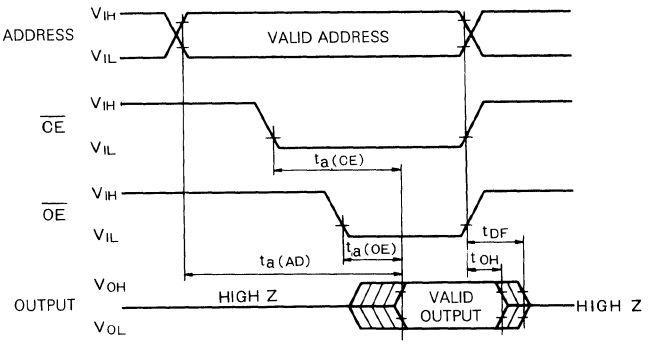
Note 2. Typical value is that with standard supply voltage applied and $T_a$=25°C.

### AC ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address access time | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(CE)}$ | $\overline{CE}$ access time | $\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(OE)}$ | $\overline{OE}$ access time | $\overline{CE}$=$V_{IL}$ | 10 | | 100 | ns |
| $t_{DF}$ | $\overline{OE}$ output floating delay time | $\overline{CE}$=$V_{IL}$ | 0 | | 90 | ns |
| $t_{OH}$ | Data validity period after $\overline{OE}$, $\overline{CE}$ | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | 0 | | | ns |

## 65 536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

### READ-OUT TIMING DIAGRAM




Switching Characteristics Test Conditions

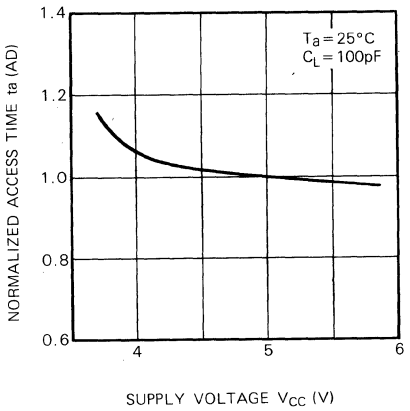
Input voltage: $V_{IL}$ = 0.8V, $V_{IH}$ = 2.2V
Input signal rise-fall time: ≤20ns
Reference voltage for timing measurements: Input 1V, 2V
Output 0.8V, 2V
Loading: 1TTL gate + CL (= 100pF)

### INPUT/OUTPUT CAPACITANCE ($T_a$ = 25°C, f = 1MHz, unless otherwise specified)

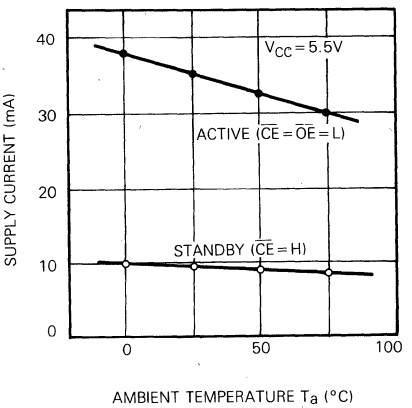
| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | 8 | 12 | pF |

### TYPICAL CHARACTERISTICS

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

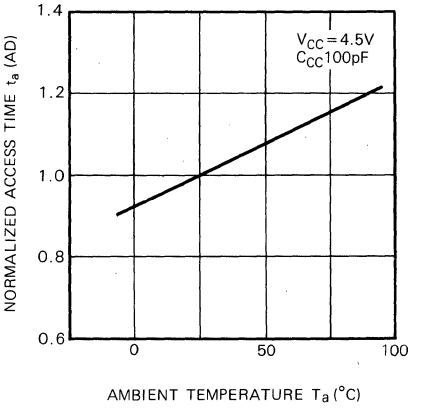



SUPPLY CURRENT VS AMBIENT TEMPERATURE

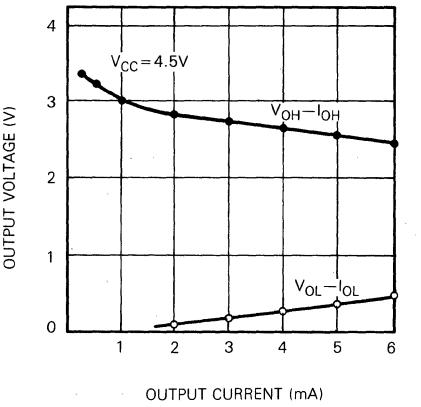


## 65 536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

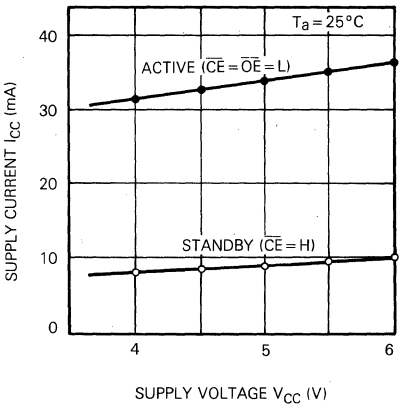
### NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE




### OUTPUT VOLTAGE VS OUTPUT CURRENT

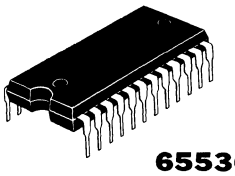



### SUPPLY CURRENT VS SUPPLY VOLTAGE






MITSUBISHI ELECTRIC





# M5M2365-XXXP

## 65536-BIT (8192-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M2365-XXXP is a 65536-bit mask programmable high speed read-only memory.

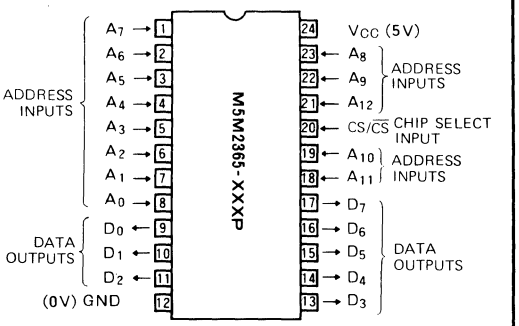
The M5M2365-XXXP is fabricated by N-channel polysilicon gate technology and available in a 24-pin DIL package. It is pin-compatible with the M5L2716K and M5L2732K in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

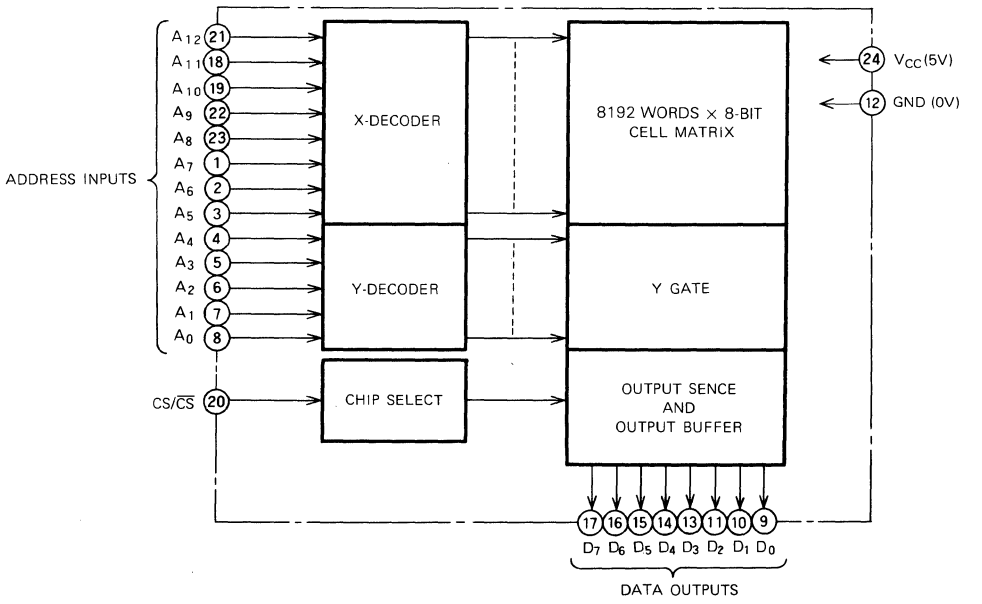
- 8192 word x 8-bit organization
- Access time . . . . . 250ns (max)
- Output control selection (CS/$\overline{CS}$)
- Low power supply current ($I_{CC}$) . . . . . 60mA (max)
- Single 5V power supply
- 3-state outputs for wire-OR expansion
- Input and output TTL-compatible
- Standard 24 pin DIL package
- Pin compatible with 2716, 2732 EPROMs and MK36000 MASK ROM

## PIN CONFIGURATION (TOP VIEW)




**Outline 24P4**

## BLOCK DIAGRAM



## 65536-BIT (8192-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATINGS*

Temperature under bias . . . . . −10°C ~ +80°C
Storage temperature . . . . . −65°C ~ +150°C
All input or output voltage** . . . . . −0.6V ~ +7V

### COMMENT

* Stresses above those listed may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.

** With respect to Ground.

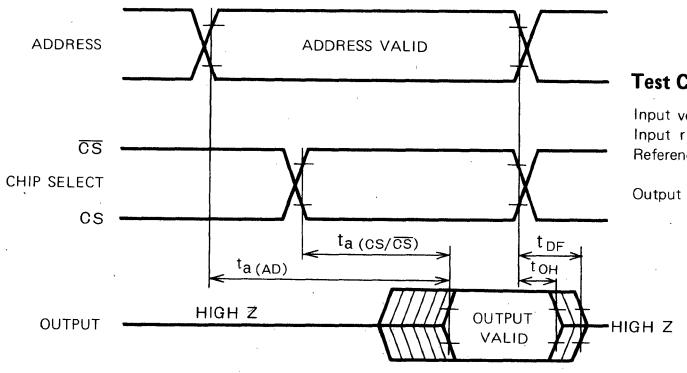
### D.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input leakage current | $V_{IN}$=5.5V | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{out}$=5.5V | −10 | | 10 | μA |
| $I_{CC}$ | $V_{CC}$ current | CS/$\overline{CS}$=H/L | | | 60 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

### A.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address to output delay | CS/$\overline{CS}$=H/L | | | 250 | ns |
| $t_{a(CS/\overline{CS})}$ | Chip select to output delay | | 10 | | 100 | ns |
| $t_{DF}$ | Chip select to output float | | 10 | | 90 | ns |
| $t_{OH}$ | Output hold from chip select | | 10 | | | ns |

### A.C. WAVEFORMS




**Test Conditions for A.C. Characteristics**

Input voltage: $V_{IL}$=0.8V, $V_{IH}$=2.2V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Input 1V and 2V
Outputs 0.8V and 2V
Output road: 1 TTL gate, $C_L$=100pF



MITSUBISHI ELECTRIC

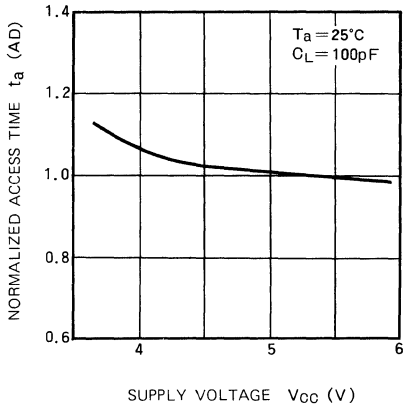
## 65536-BIT (8192-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

### CAPACITANCE ($T_a$=25°C, f=1MHz)

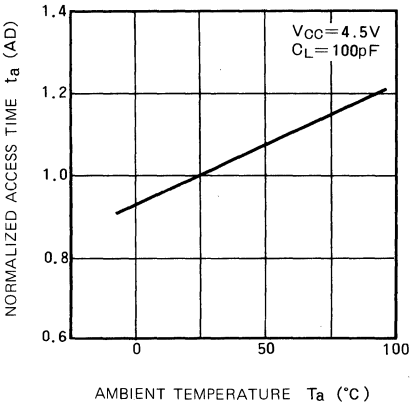
| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | 8 | 12 | pF |

### TYPICAL CHARACTERISTICS

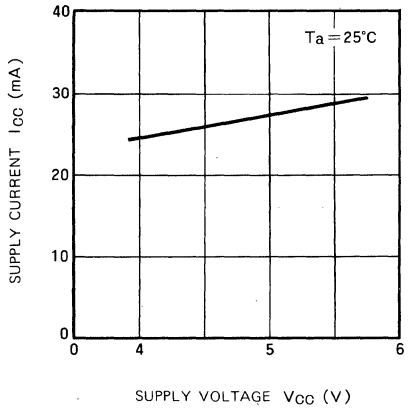
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



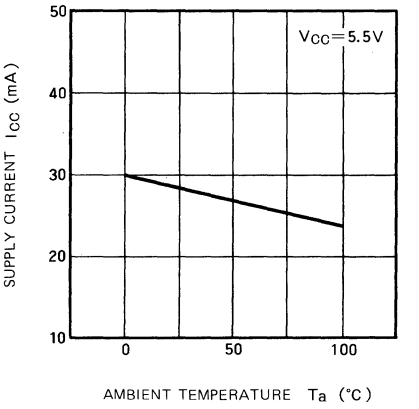

NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



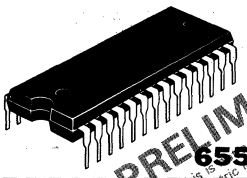

SUPPLY CURRENT VS. SUPPLY VOLTAGE




SUPPLY CURRENT VS. AMBIENT TEMPERATURE



# M5M23C64-XXXP





## 65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M23C64-XXXP is a 65536-bit mask-programmable high speed read-only memory.

The M5M23C64-XXXP is fabricated by Silicon gate CMOS technology and available in a 28-pin DIL package. It is interchangeable with the M5L2764K in read mode.

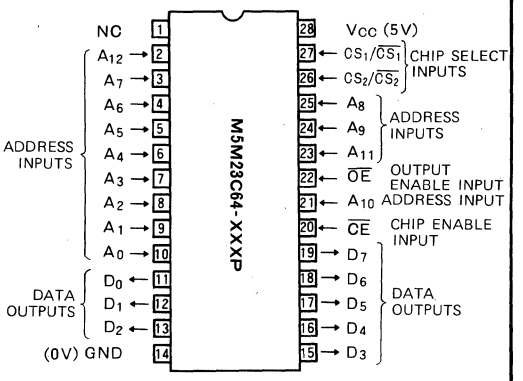
The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

| | |
|---|---|
| $A_0 \sim A_{12}$ | Addresses |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$ | Output enable |
| $D_0 \sim D_7$ | Outputs |
| N.C. | No connection |
| $CS_1/\overline{CS_1}$, $CS_2/\overline{CS_2}$ | Chip select |

- 8192 word x 8-bit organization
- Access time ..... 350 ns (max)
- Low power supply current (Icc)
  - Active ..... 40 mA (max)
  - Standby ..... 10 mA (max) (TTL Compatible)
  - 50 $\mu$A (max) ($\overline{CE}$ = Vcc−0.2V)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIL package
- Interchangeable with The M5L2764K in read mode

## PIN CONFIGURATION (TOP VIEW)




NC; NO CONNECTION

**Outline 28P4**

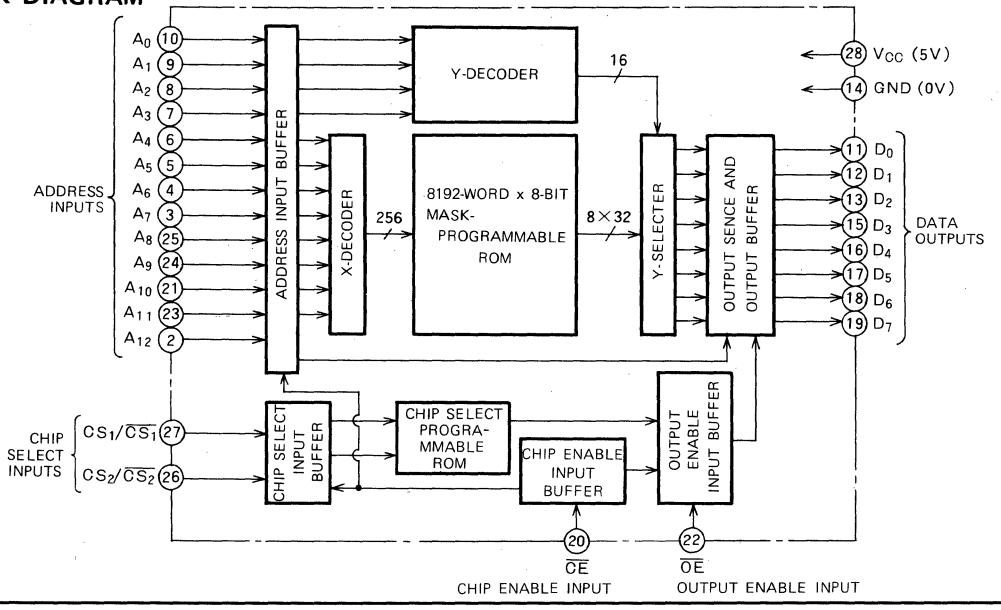
## FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level), and the $CS_1/\overline{CS_1}$ and $CS_2/\overline{CS_2}$ terminals to the read mode (high level/low level).

Low level inputs to $\overline{CE}$ and $\overline{OE}$, high level/low level inputs to $CS_1/\overline{CS_1}$ and $CS_2/\overline{CS_2}$, and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$).

When the $\overline{OE}$ Signal is high, the data input/output are in a floating state.

## BLOCK DIAGRAM



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## 65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

When the $\overline{CE}$ signal is high, the data input/output are in a floating state and the device is in the standby mode or power-down mode.

The active logic level of $CS_1/\overline{CS_1}$ and $CS_2/\overline{CS_2}$ can be programmed at the time of fabricating the ROM mask.

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature under bias ..... −10°C ~ +80°C
Storage temperature ..... −65°C ~ +150°C
All input or output voltage (Note 2) ..... −0.3V ~ +7V

Note 1 Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.
2 With respect to Ground

### RECOMMENDED OPERATING CONDITIONS ($T_a$=0~70°C)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage (Note 1) | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IH}$ | High level input voltage | 2.4 | | $V_{CC}$+0.1 | V |
| $V_{IL}$ | Low level input voltage | −0.1 | | 0.45 | V |

Note1 Need 1μF ceramic capacitor between $V_{CC}$ and GND.

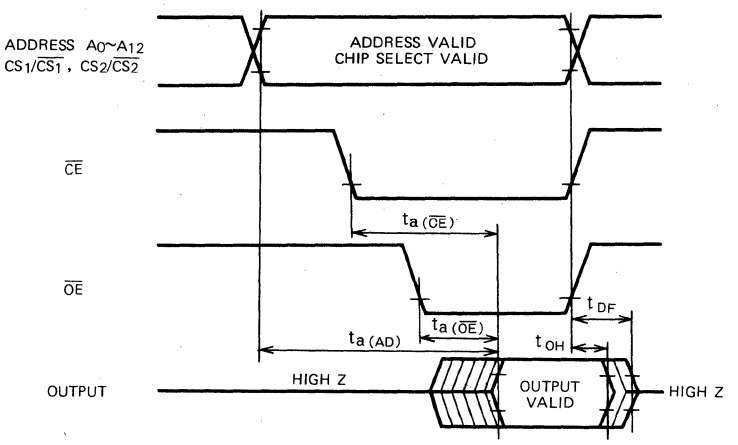
### D.C. CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input load current | | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}=V_{IH}$ | | | 10 | mA |
| | | $\overline{CE}=V_{CC}-0.2V$ | | | 50 | μA |
| $I_{CC2}$ | $V_{CC}$ current active | $\overline{CE}=\overline{OE}=V_{IL}$ Output Open<br>$CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$ | | | 40 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.6 | V |
| $V_{IH}$ | Input high voltage | | 2.2 | | $V_{CC}$+0.1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

### A.C. CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, $V_{IH}$=2.4V, $V_{IL}$=0.45V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}=\overline{OE}=V_{IL}$<br>$CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$ | | | 350 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | $\overline{OE}=V_{IL}$<br>$CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$ | | | 350 | ns |
| $t_{a(\overline{OE})}$ | Output enable to output delay | $\overline{CE}=V_{IL}$<br>$CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$ | | | 200 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}=V_{IL}$<br>$CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$ | 0 | | 200 | ns |
| $t_{OH}$ | Output hold from address | $CS_1/\overline{CS_1}=CS_2/\overline{CS_2}=V_{IH}/V_{IL}$<br>$\overline{CE}=\overline{OE}=V_{IL}$ | 0 | | | ns |

## A.C. WAVEFORMS

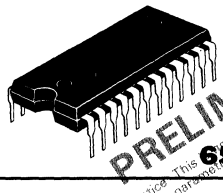



Test Conditions for A.C. Characteristics
Input voltage: $V_{IL}$=0.45V, $V_{IH}$=2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 0.8V and 2V
Output load: 1 TTL gate, $C_L$=100pF Output 0.8V and 2V

## CAPACITANCE ($T_a$=25°C, f=1MHz)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | | 15 | pF |

# M5M23C65-XXXP





## 65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M23C65-XXXP is a 65536-bit mask-programmable high speed read-only memory.

The M5M23C65-XXXP is fabricated by silicon gate CMOS technology and available in a 24-pin DIL package.

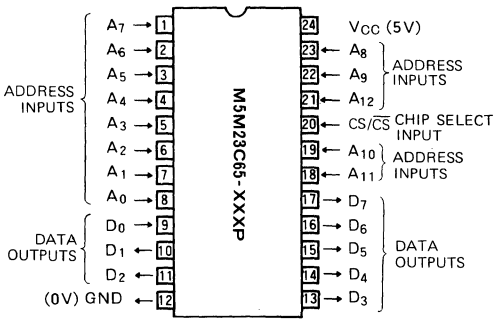
The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

| | |
|---|---|
| $A_0 \sim A_{12}$ | Addresses |
| CS/$\overline{CS}$ | Chip select |
| $D_0 \sim D_7$ | Outputs |

- 8192 word x 8-bit organization
- Access time ..... 350 ns (max)
- Chip select CS/$\overline{CS}$ mask programmable
- Low power supply current (Icc)
  - Active ..... 40 mA (max)
  - Standby ..... 10 mA (max) (TTL-compatible)
  - 50 $\mu$A (max) (CS/$\overline{CS}$ = 0.2V/Vcc–0.2V)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 24-pin DIL package

## PIN CONFIGURATION (TOP VIEW)




**Outline 24P4**

## FUNCTION

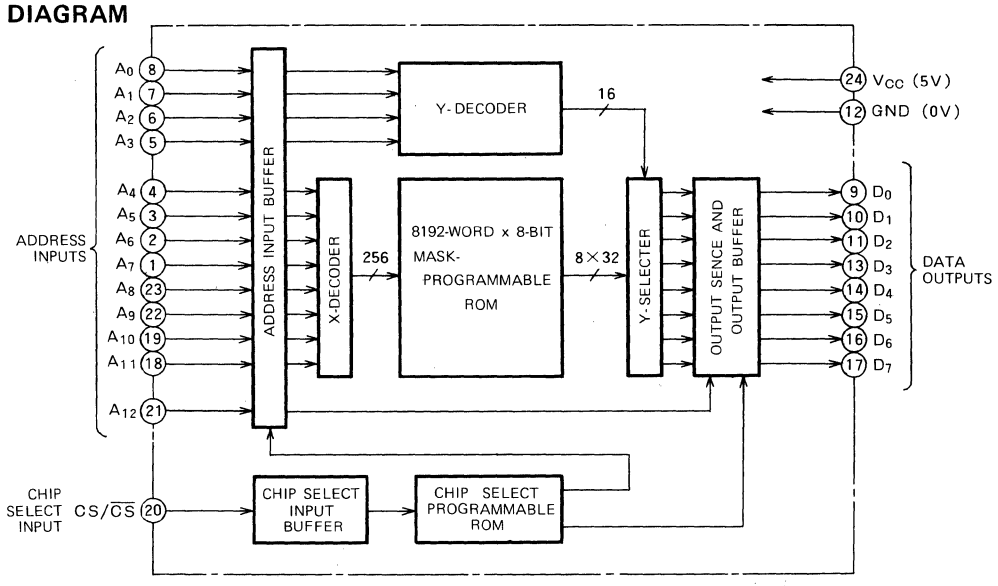
Set the CS/$\overline{CS}$ terminals to the read mode. (high level/low level)

High level/low level inputs to CS/$\overline{CS}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$).

When the CS/$\overline{CS}$ signal is low/high, data input/output are in a floating state, and the device is in the standby mode or power-down mode.

The active logic level of CS/$\overline{CS}$ can be programmed at the time of fabricating the ROM mask.

## BLOCK DIAGRAM



## 65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature under bias ..... −10°C ~ +80°C
Storage temperature ..... −65°C ~ +150°C
All input or output voltage (Note 2) ..... −0.3V ~ +7V

Note 1 Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.
2 With respect to Ground

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage (Note 1) | 4.5 | 5 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| $V_{IH}$ | High level input voltage | 2.4 | | $V_{CC}$+0.1 | V |
| $V_{IL}$ | Low level input voltage | −0.1 | | 0.45 | V |

Note1 Need 1μF ceramic capacitor between $V_{CC}$ and GND.

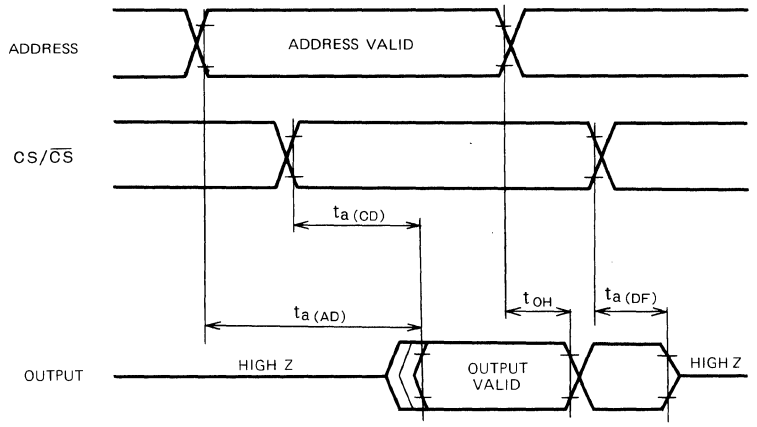
## D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input load current | | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $CS/\overline{CS} = V_{IL}/V_{IH}$ | | | 10 | mA |
| | | $CS/\overline{CS} = 0.2V/V_{CC}-0.2V$ | | | 50 | μA |
| $I_{CC2}$ | $V_{CC}$ current active | $CS/\overline{CS} = V_{IH}/V_{IL}$, Output open | | | 40 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.6 | V |
| $V_{IH}$ | Input high voltage | | 2.2 | | $V_{CC}$+0.1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = −400μA | 2.4 | | | V |

## A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, $V_{IH}$ = 2.4V, $V_{IL}$ = 0.45V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address to output delay | $CS/\overline{CS} = V_{IH}/V_{IL}$ | | | 350 | ns |
| $t_{a(CD)}$ | Chip select to output delay | | | | 350 | ns |
| $t_{a(DF)}$ | Chip select to output float | | | | 200 | ns |
| $t_{OH}$ | Output hold from address | $CS/\overline{CS} = V_{IH}/V_{IL}$ | 0 | | | ns |

## A.C. WAVEFORMS

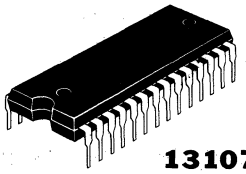



Test Conditions for A.C. Characteristics
Input voltage: $V_{IL}$=0.45V, $V_{IH}$=2.4V
Input rise and fall times : ≦20ns
Reference voltage at timing measurement: Inputs 0.8V and 2V
Output load: 1 TTL gate, $C_L$=100pF Outputs 0.8V and 2V

## CAPACITANCE ($T_a$=25°C, f=1MHz)

| Symbol | Parameter | Text conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$=0V | | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$=0V | | | 15 | pF |

# M5M23128-XXXP



## 131072-BIT(16384-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M23128-XXXP is a 131072-bit mask-programmable high speed read-only memory.

The M5M23128-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIL package. It is interchangeable with the M5L27128K and Intel 27128 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

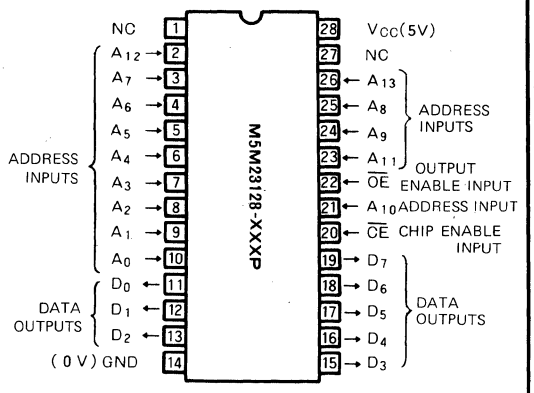
- 16384 word x 8-bit organization
- Access time . . . . . 250ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply current ($I_{CC}$) Active . . 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIL package
- Interchangeable with the M5L27128K and Intel 27128

## FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level.)

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0$~$A_{13}$) make the data contents of the designated address location available at the data output ($D_0$~$D_7$).

## PIN CONFIGURATION (TOP VIEW)



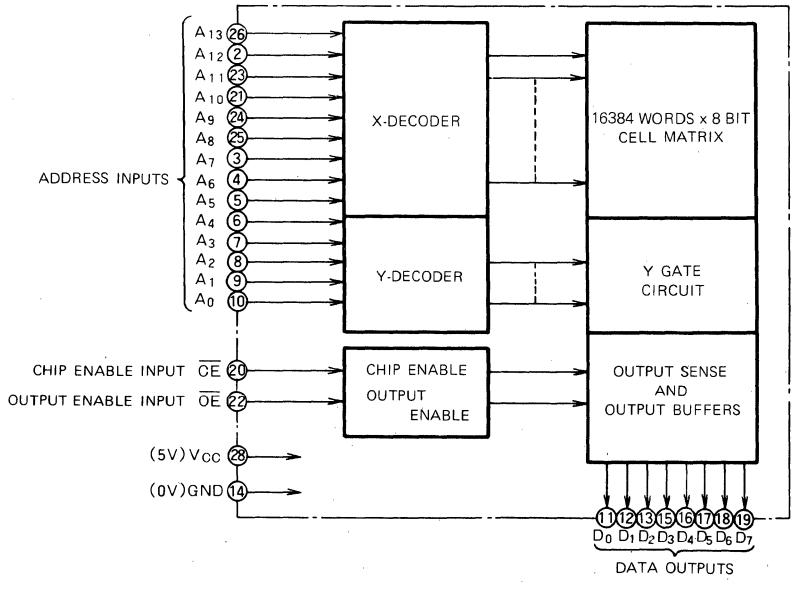

NC; NO CONNECTION

**Outline 28P4**

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 131072-BIT(16384-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATINGS*

Temperature under bias . . . . . −10°C ~ +80°C
Storage temperature . . . . . −65°C ~ +150°C
All input or output voltage** . . . . . −0.6V ~ +7V

### COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.
** With respect to Ground.

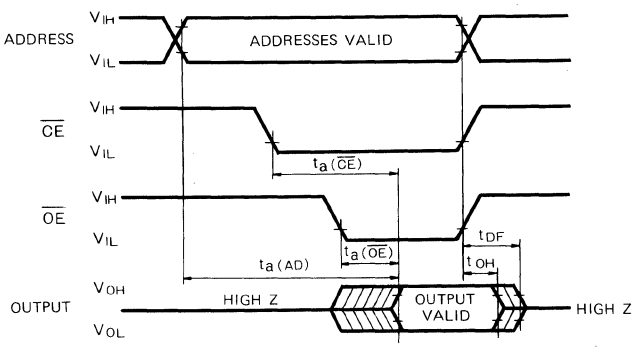
### D.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input leakage current | $V_{IN}$=5.5V | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=5.5V | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}$=$V_{IH}$ | | 15 | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ current active | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | 40 | 80 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

### A.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | $\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(\overline{OE})}$ | Output enable to output delay | $\overline{CE}$=$V_{IL}$ | 10 | | 100 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}$=$V_{IL}$ | 0 | | 90 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ or $\overline{OE}$ | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | 0 | | | ns |

### A.C. WAVEFORMS




**Test Conditions for A.C. Characteristics**

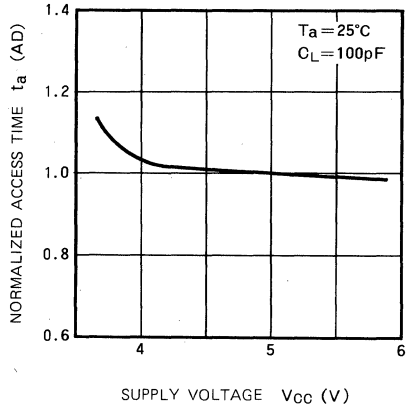
Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, $C_L$ = 100pF

## CAPACITANCE ($T_a$=25°C, f=1MHz)

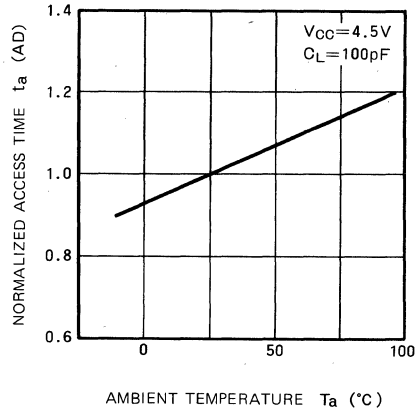
| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | 8 | 12 | pF |

## TYPICAL PERFORMANCE DATA

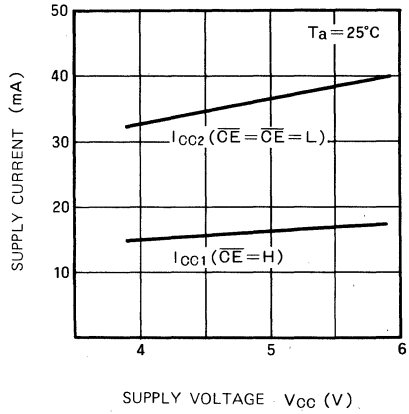
### NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



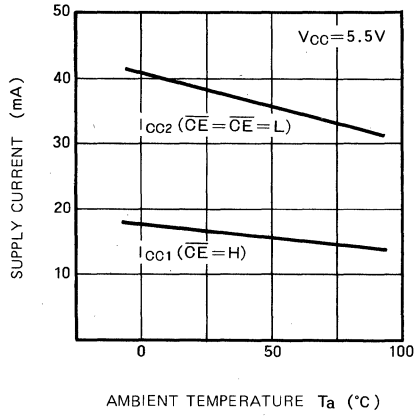

### NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



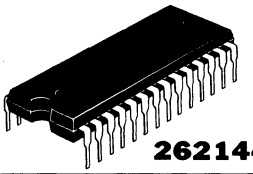

### SUPPLY CURRENT VS. SUPPLY VOLTAGE




### SUPPLY CURRENT VS. AMBIENT TEMPERATURE



# M5M23256-XXXP



## 262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

## DESCRIPTION

The Mitsubishi M5M23256-XXXP is a 262144-bit mask-programmable high speed read-only memory.

The M5M23256-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIL package. It is compatible with the M5L27256K and Intel 27256 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

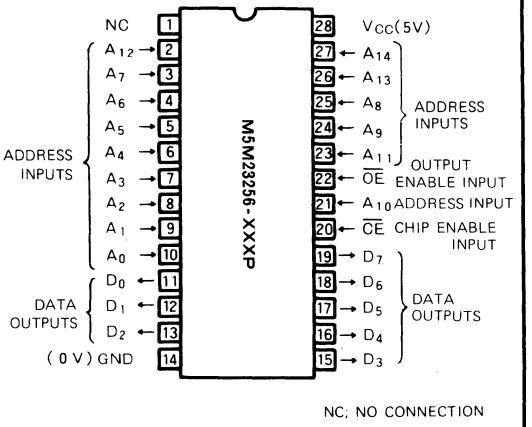
- 32768 word x 8-bit organization
- Access time . . . . . 250ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply current ($I_{CC}$) Active . . 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIL package
- Compatible with Intel 27256

## FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level.)

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

## PIN CONFIGURATION (TOP VIEW)



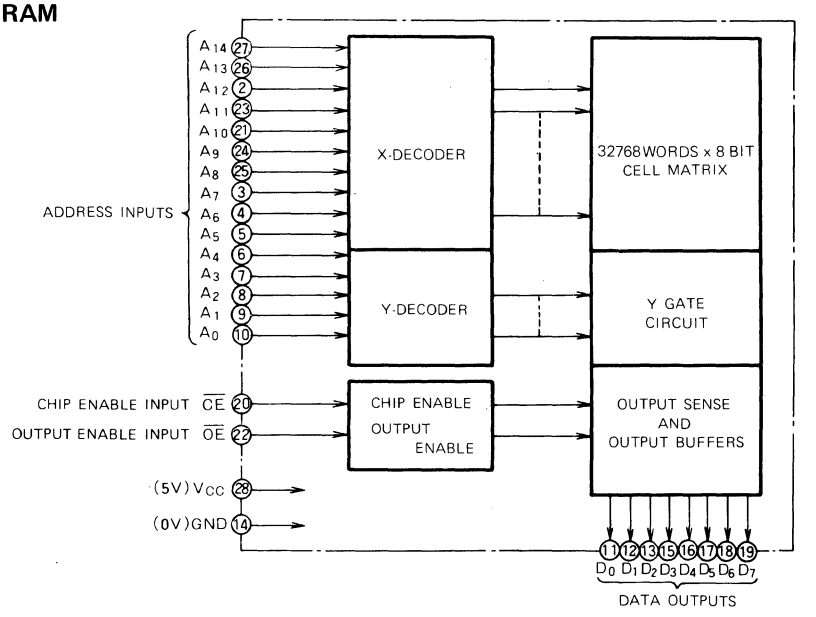

NC; NO CONNECTION

**Outline 28P4**

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

## BLOCK DIAGRAM



## 262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATINGS*

Temperature under bias . . . . . −10°C ~ +80°C
Storage temperature . . . . . −65°C ~ +150°C
All input or output voltage** . . . . . −0.6V ~ +7V

### COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

** With respect to Ground.

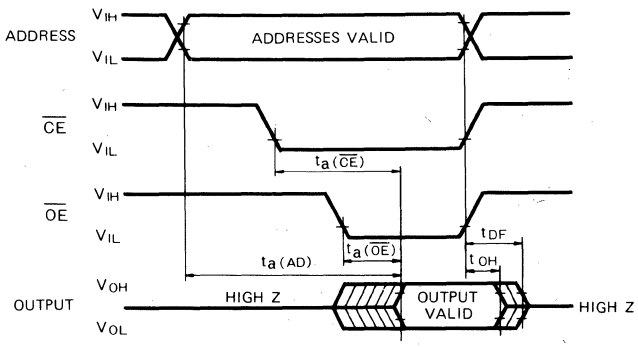
### D.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input leakage current | $V_{IN}$=5.5V | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=5.5V | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}$=$V_{IH}$ | | 15 | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ current active | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | 40 | 80 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

### A.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | $\overline{OE}$=$V_{IL}$ | | | 250 | ns |
| $t_{a(\overline{OE})}$ | Output enable to output delay | $\overline{CE}$=$V_{IL}$ | 10 | | 100 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}$=$V_{IL}$ | 0 | | 90 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ or $\overline{OE}$ | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | 0 | | | ns |

### A.C. WAVEFORMS




**Test Conditions for A.C. Characteristics**

Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, $C_L$ = 100pF



MITSUBISHI ELECTRIC

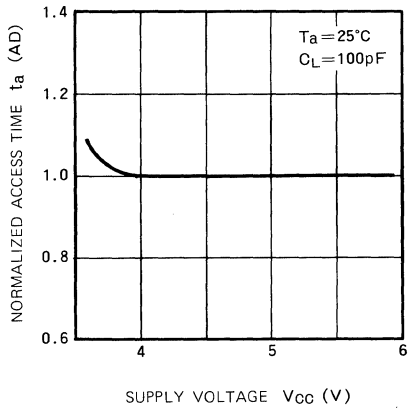
## 262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

### CAPACITANCE ($T_a$=25°C, f=1MHz)

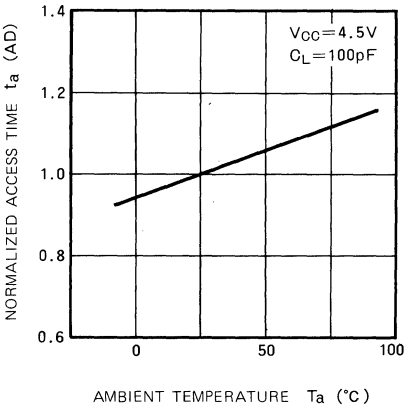
| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | 8 | 12 | pF |

### TYPICAL PERFORMANCE DATA

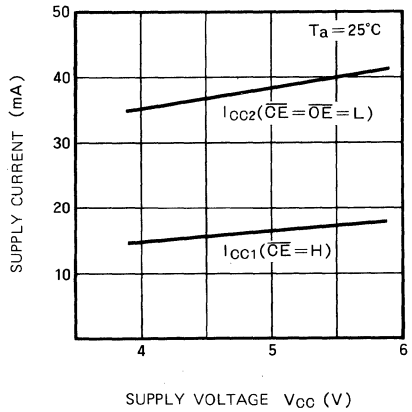
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



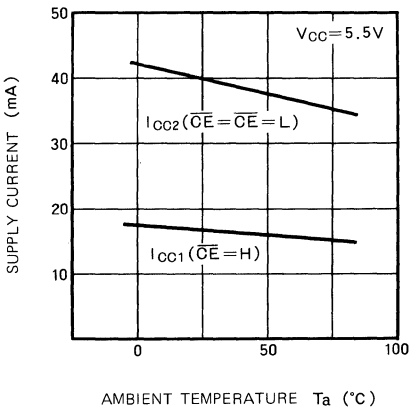

NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE




SUPPLY CURRENT VS. SUPPLY VOLTAGE




SUPPLY CURRENT VS. AMBIENT TEMPERATURE



# M5M231000-XXXP

## 1048576-BIT (131072-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM



## DESCRIPTION

The Mitsubishi M5M231000-XXXP is 1048576-bit mask-programmable high speed read-only memory.

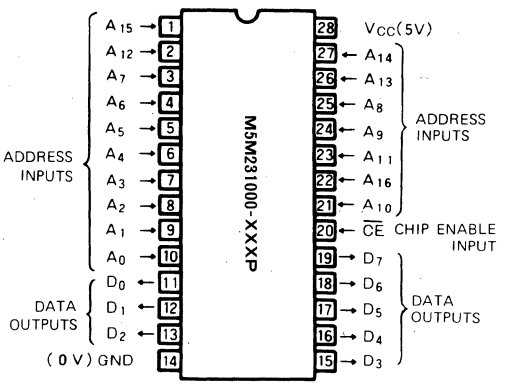
The M5M231000-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIL package.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

## FEATURES

- 131072 word x 8-bit organization
- Access time . . . . . -25 250ns (max)
  . . . . . -30 300ns (max)
- ONE line control $\overline{CE}$
- Low power supply current ($I_{CC}$) Active . . 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIL package

## PIN CONFIGURATION (TOP VIEW)




**Outline 28P4**

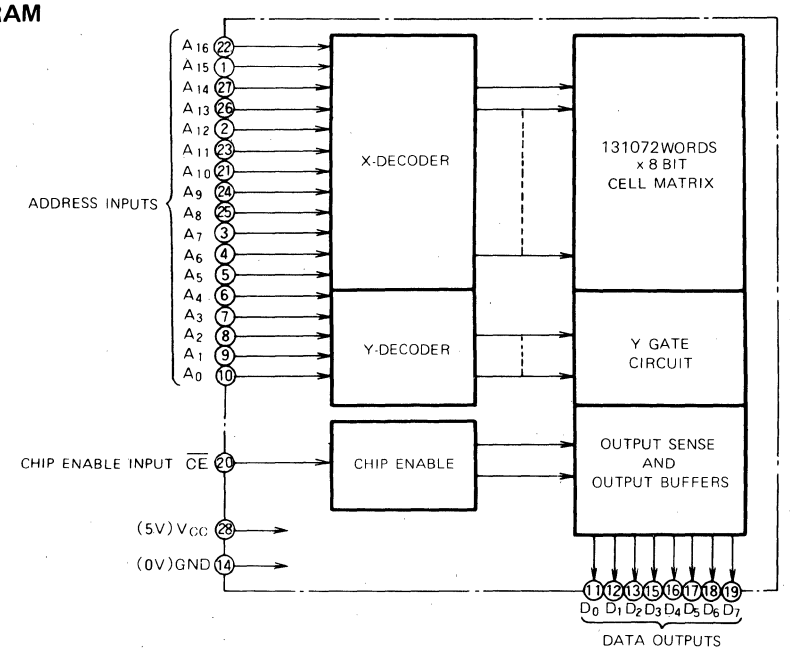
## FUNCTION

Set the CE terminals to the read mode (low level.)

Low level input to $\overline{CE}$ and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{CE}$ signal is high, data output are in a floating state and the device is in the standby mode or power-down mode.

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

## 1048576-BIT (131072-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATINGS*

Temperature under bias . . . . . −10°C ~ +80°C
Storage temperature . . . . . −65°C ~ +150°C
All input or output voltage** . . . . . −0.6V ~ +7V

### COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.
** With respect to Ground.

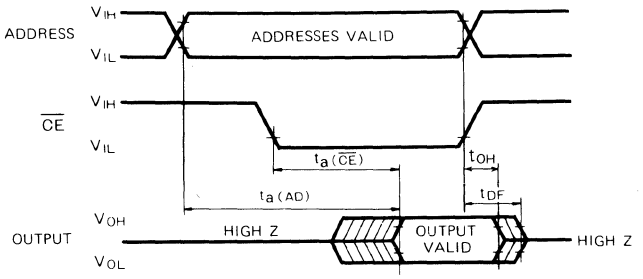
### D.C. ELECTRICAL CHARACTERISTICS ($T_a$=0 ~ 70°C, $V_{CC}$=5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input leakage current | $V_{IN}$=5.5V | −10 | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=5.5V | −10 | | 10 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}$=$V_{IH}$ | | 15 | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ current active | $\overline{CE}$=$V_{IL}$ | | 40 | 80 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

### A.C. ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits−25 | | Limits−30 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}$=$V_{IL}$ | | 250 | | 300 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | | | 250 | | 300 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}$=$V_{IL}$ | 0 | 80 | 0 | 100 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ | $\overline{CE}$=$V_{IL}$ | 0 | | 0 | | ns |

### A.C. WAVEFORMS




**Test Conditions for A.C. Characteristics**

Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, $C_L$ = 100pF

### CAPACITANCE ($T_a$=25°C, f=1MHz)

| Symbol | Parameter | Conditions | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $C_{IN}$ | Input capacitance | $V_{IN}$=0V | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$=0V | | 15 | pF |

# MOS EPROM

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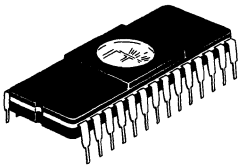




# M5L2764K, -2

## 65536-BIT (8192-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

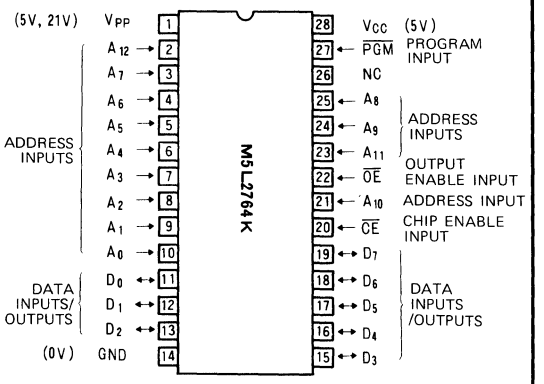
## DESCRIPTION

The Mitsubishi M5L2764K is a high-speed 65536-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L2764K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIL package with a transparent lid.

## FEATURES

- 8192 Word x 8-bit Organization
- Access Time M5L2764K-2 200 ns (Max)
  M5L2764K 250 ns (Max)
- Two Line Control $\overline{OE}$, $\overline{CE}$
- Low Power Current ($I_{CC}$) Active .....150 mA (Max)
  Standby ... 35 mA (Max)
- Single 5V Power Supply
- 3-State Output Buffer
- Input and Output TTL-Compatible in Read and Program Mode
- Standard 28-pin DIL Package
- Single Location Programming with One 50 ms Pulse
- Fast programming algorithm
- Interchangeable with INTEL 2764

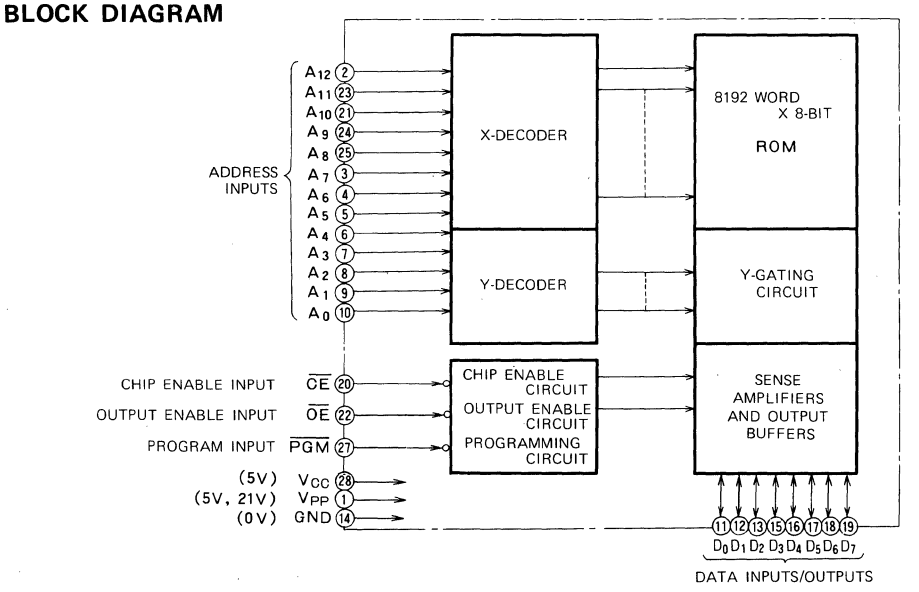
## PIN CONFIGURATION (TOP VIEW)




NC : NO CONNECTION

**Outline 28K1**

## BLOCK DIAGRAM



# 65536-BIT (8192-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## FUNCTION

### Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

In the read mode $V_{PP}$ must be at $V_{CC}$ level.

### Programming

### (Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6-9)

### (Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the $V_{PP}$ power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{12}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leqq t_{PW} \leqq$ 55 ms.

### Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm$^2$. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

## MODE SELECTION

| Mode \ Pins | $\overline{CE}$(20) | $\overline{OE}$(22) | $\overline{PGM}$(27) | $V_{PP}$(1) | $V_{CC}$(28) | Outputs (11~13, 15~19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | Data out |
| Standby | $V_{IH}$ | X* | X* | $V_{CC}$ | $V_{CC}$ | Floating |
| Program | $V_{IL}$ | X* | $V_{IL}$ | $V_{PP}$ | $V_{CC}$ | Data in |
| Program verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PP}$ | $V_{CC}$ | Data out |
| Program inhibit | $V_{IH}$ | X* | X* | $V_{PP}$ | $V_{CC}$ | Floating |

*: X can be either $V_{IL}$ or $V_{IH}$.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $T_{opr}$ | Temperature under bias | −10~80 | °C |
| $T_{stg}$ | Storage temperature | −65~125 | °C |
| $V_{I1}$ | All input or output voltage (Note 2) | −0.6~7 | V |
| $V_{I2}$ | $V_{PP}$ supply voltage during programming (Note 2) | −0.6~26.5 | V |

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.



MITSUBISHI ELECTRIC

# 65536-BIT (8192-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## READ OPERATION

$Ta = 0°$ to 70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$

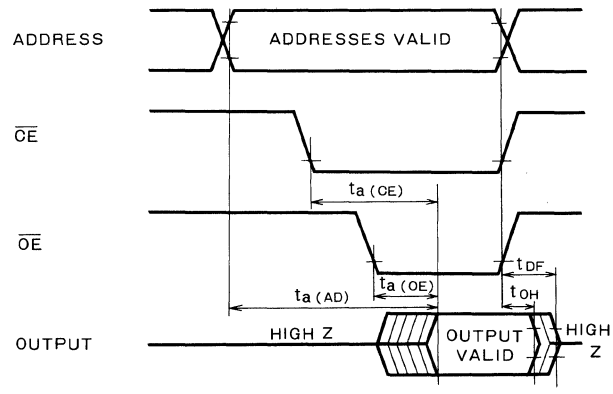
## D.C. CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input load current | $V_{IN} = 5.25V$ | | | 10 | $\mu A$ |
| $I_{LO}$ | Output leakage current | $V_{OUT} = 5.25V$ | | | 10 | $\mu A$ |
| $I_{PP1}$ | $V_{PP}$ current read | $V_{PP} = 5.25V$ | | | 15 | mA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE} = V_{IH}$ | | | 35 | mA |
| $I_{CC2}$ | $V_{CC}$ current active | $\overline{CE} = \overline{OE} = V_{IL}$ | | | 150 | mA |
| $V_{IL}$ | Low-level input voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}+1$ | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -400\mu A$ | 2.4 | | | V |

## A.C. CHARACTERISTICS

| Symbol | Parameter | Test conditions | M5L2764K-2 | | M5L2764K | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 200 | | 250 | ns |
| $t_{a(CE)}$ | $\overline{CE}$ to output delay | $\overline{OE} = V_{IL}$ | | 200 | | 250 | ns |
| $t_{a(OE)}$ | Output enable to output delay | $\overline{CE} = V_{IL}$ | 10 | 70 | 10 | 100 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE} = V_{IL}$ | 0 | 60 | 0 | 90 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ or $\overline{OE}$ | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | 0 | | ns |

## AC WAVEFORMS




Test Conditions for A.C. Characteristics
Input Voltage: $V_{IL}$ = 0.8V, $V_{IH}$ = 2.2V
Input Rise and Fall Times: ≦20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V, Outputs 0.8V and 2V
Output Load: 1 TTL gate, $C_L$ = 100pF

## CAPACITANCE ($T_a$ = 25°C, f = 1 MHz)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN} = 0$ V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT} = 0$ V | | 8 | 12 | pF |

## PROGRAM OPERATION

## CONVENTIONAL PROGRAMMING ALGORITHM ($Ta = 25 \pm 5$ °C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21 \pm 0.5V$ unless otherwise noted)

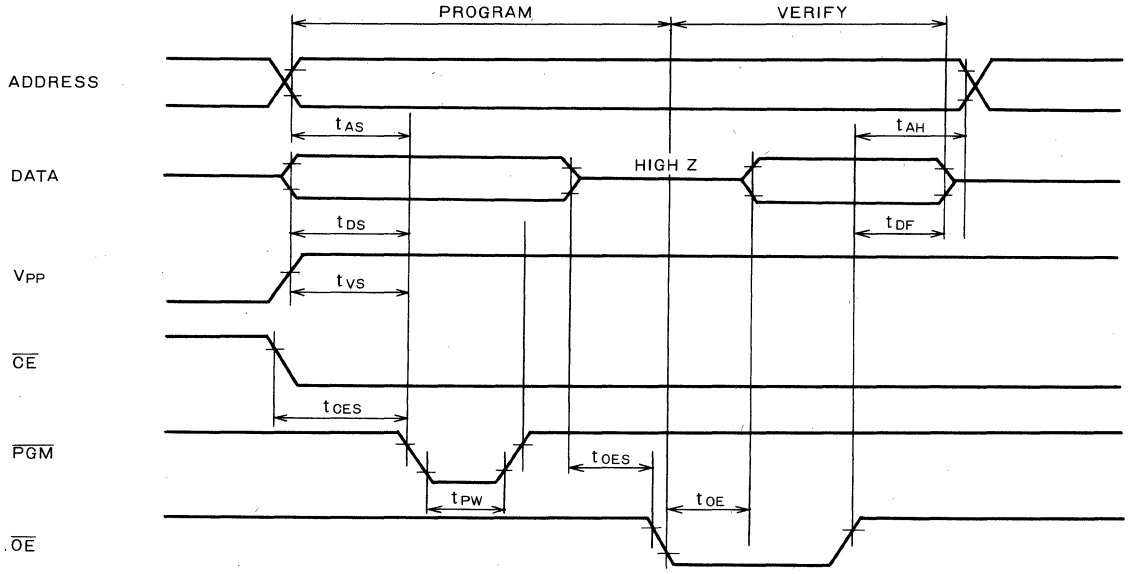
## D. C. CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu$A |
| $V_{OL}$ | Low-level output voltage (verify) | $I_{OL} = 2.1$mA | | | 0.45 | V |
| $V_{OH}$ | High-level output voltage (verify) | $I_{OH} = -400\mu$A | 2.4 | | | V |
| $I_{CC2}$ | $V_{CC}$ supply current (active) | | | | 100 | mA |
| $V_{IL}$ | Low-level input voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}+1$ | V |
| $I_{PP}$ | $V_{PP}$ supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

## A. C. CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address setup time | | 2 | | | $\mu$s |
| $t_{OES}$ | $\overline{OE}$ setup time | | 20 | | | $\mu$s |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu$s |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu$s |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu$s |
| $t_{DF}$ | Chip enable to output delay | | 0 | | 130 | ns |
| $t_{VS}$ | $V_{PP}$ setup time | | 2 | | | $\mu$s |
| $t_{PW}$ | $\overline{PGM}$ pulse width (programming) | | 45 | 50 | 55 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu$s |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

## AC WAVEFORMS




Test Conditions for AC Characteristics
Input Voltage: $V_{IL}$ = 0.8V, $V_{IH}$ = 2.2V
Input Rise and Fall Times: ≦ 20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V
Outputs 0.8V and 2V

## FAST PROGRAMMING ALGORITHM

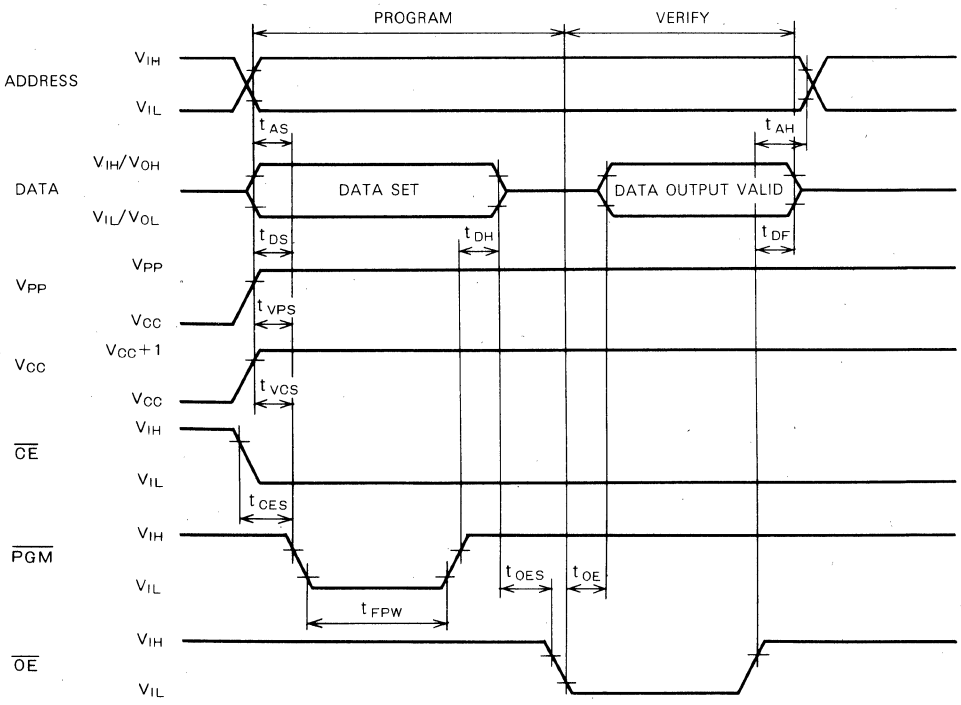
## DC CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu A$ |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH} = -400\mu A$ | 2.4 | | | V |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ | V |
| $I_{CC2}$ | $V_{CC}$ supply current | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

## AC CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

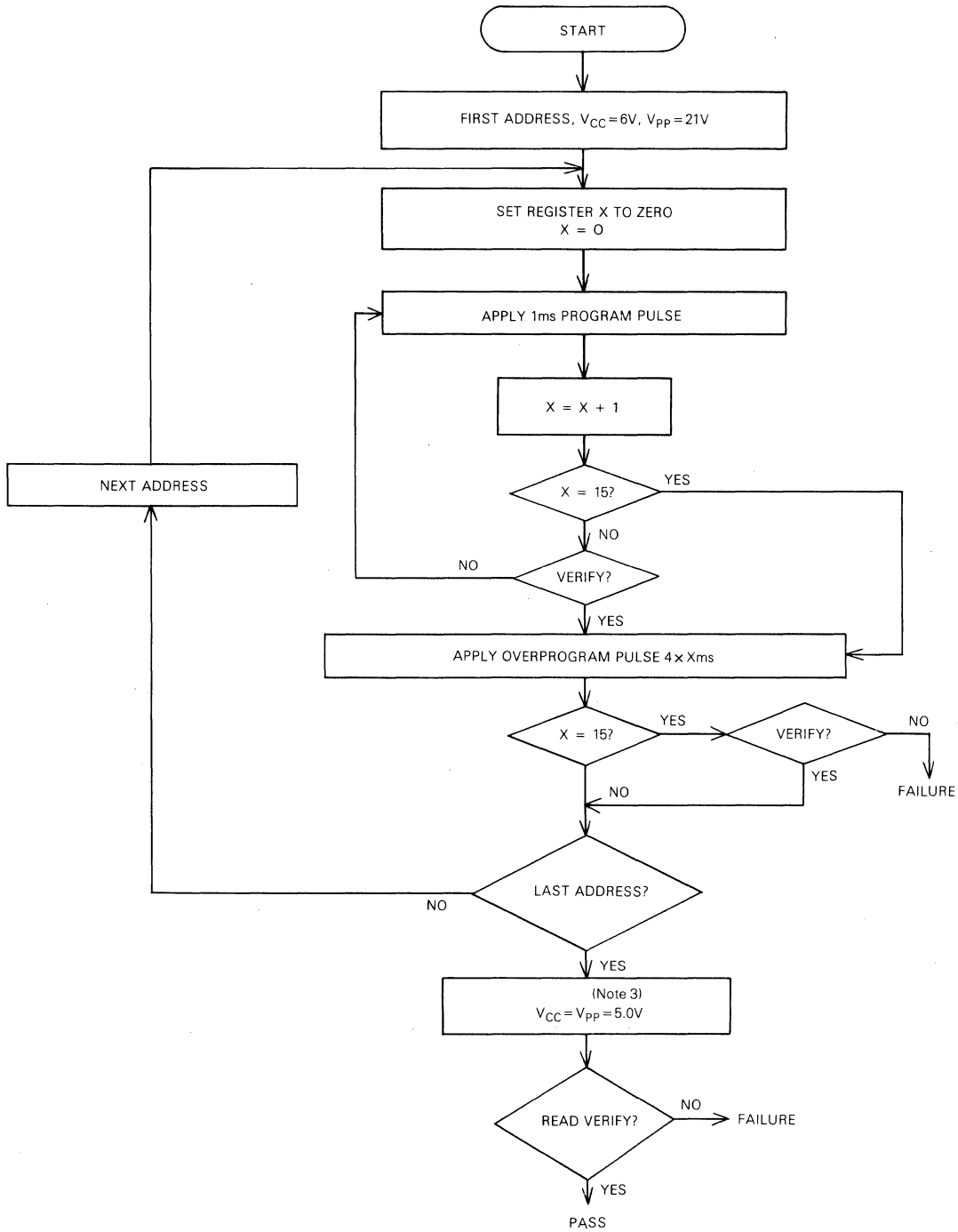
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address setup time | | 2 | | | $\mu s$ |
| $t_{OES}$ | $\overline{OE}$ set up time | | 20 | | | $\mu s$ |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu s$ |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu s$ |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu s$ |
| $t_{DF}$ | Chip enable to output float delay | | 0 | | 130 | ns |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | | $\mu s$ |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | | $\mu s$ |
| $t_{FPW}$ | $\overline{PGM}$ initial program pulse width | | 0.95 | 1 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ over program pulse width | | 3.8 | | 63 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu s$ |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

## AC WAVEFORMS




Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Input rise and fall times: $\leqq 20ns$
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

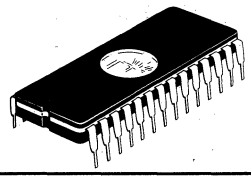
## FAST PROGRAMMING ALGORITHM FLOW CHART




Note 3: $4.75 \leqq V_{CC} = V_{PP} \leqq 5.25V$

# M5L27128K, -2

## 131 072-BIT(16384-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM



## DESCRIPTION

The Mitsubishi M5L27128K is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27128K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIL package with a transparent lid.

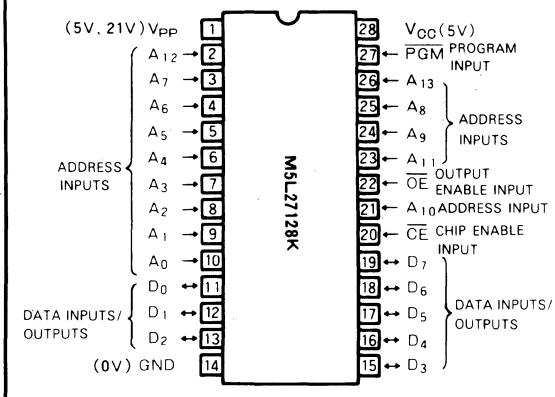
## FEATURES

- 16384 word × 8 bit organization
- Access time M5L27128K-2 .....200ns (max.)
  M5L27128K .....250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current ($I_{CC}$): Active ..... 100mA (max.)
  Standby ..... 45mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIL package
- Fast programming algorithm
- Interchangeable with INTEL 27128

## APPLICATION

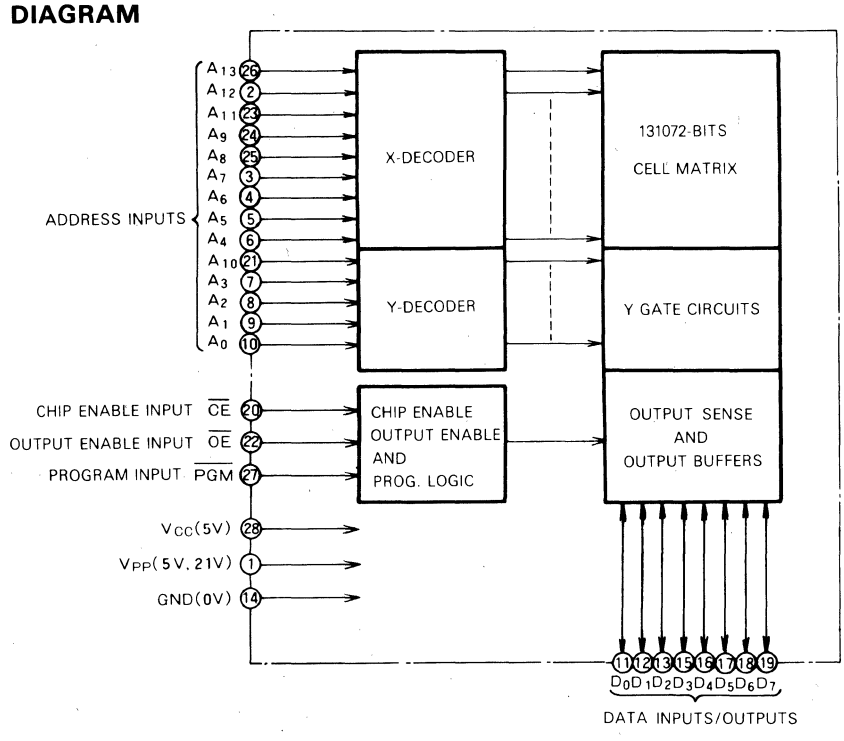
- Microcomputer systems and peripheral equipment

## PIN CONFIGURATION (TOP VIEW)




Outline 28K4

## BLOCK DIAGRAM






MITSUBISHI ELECTRIC

# 131 072-BIT(16384-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## FUNCTION

### Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

### Programming

### (Fast programming algorithm)

First set $V_{CC} = 6V$, $V_{PP} = 21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6-15)

### (Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the $V_{PP}$ power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leqq t_{PW} \leqq$ 55 ms.

### Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm$^2$. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

## MODE SELECTION

| Mode \ Pins | $\overline{CE}$(20) | $\overline{OE}$(22) | $\overline{PGM}$(27) | $V_{PP}$(1) | $V_{CC}$(28) | Outputs (11~13, 15~19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | Data out |
| Standby | $V_{IH}$ | X* | X* | $V_{CC}$ | $V_{CC}$ | Floating |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PP}$ | $V_{CC}$ | Data in |
| Program verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PP}$ | $V_{CC}$ | Data out |
| Program inhibit | $V_{IH}$ | X* | X* | $V_{PP}$ | $V_{CC}$ | Floating |

*: X can be either $V_{IL}$ or $V_{IH}$.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $T_{opr}$ | Temperature under bias | −10~80 | °C |
| $T_{stg}$ | Storage temperature | −65~125 | °C |
| $V_{I1}$ | All input or output voltage (Note 2) | −0.6~7 | V |
| $V_{I2}$ | $V_{PP}$ supply voltage during programming (Note 2) | −0.6~26.5 | V |

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

## READ OPERATION

## DC ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±5%, $V_{PP}$=$V_{CC}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input load current | $V_{IN}$=5.25V | | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=5.25V | | | 10 | μA |
| $I_{PP1}$ | $V_{PP}$ current read | $V_{PP}$=5.25V | | | 5 | mA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}$=$V_{IH}$ | | | 45 | mA |
| $I_{CC2}$ | $V_{CC}$ current Active | $\overline{CE}$=$\overline{OE}$ -$V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input low voltage | | 0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=2.1mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=−400μA | 2.4 | | | V |

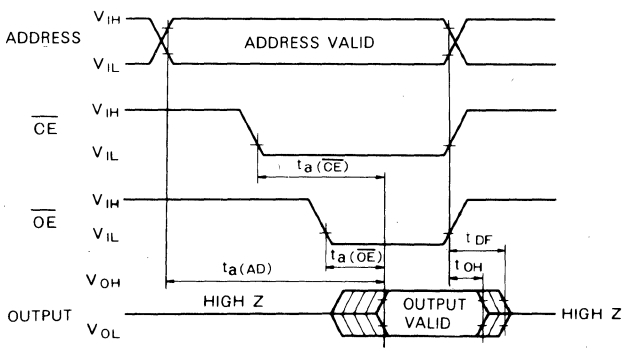
Note 3: Typical values are at Ta=25°C and nominal supply voltages.

## AC ELECTRICAL CHARACTERISTICS ($T_a$=0~70°C, $V_{CC}$=5V±5%, $V_{PP}$=$V_{CC}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | M5L27128K-2 | | M5L27128K | | |
| | | | Min | Max | Min | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | | 200 | | 250 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | $\overline{OE}$=$V_{IL}$ | | 200 | | 250 | ns |
| $t_{a(\overline{OE})}$ | Output enable to output delay | $\overline{CE}$=$V_{IL}$ | | 75 | | 100 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}$=$V_{IL}$ | 0 | 60 | 0 | 85 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ or $\overline{OE}$ | $\overline{CE}$=$\overline{OE}$=$V_{IL}$ | 0 | | 0 | | ns |

Note 4: $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

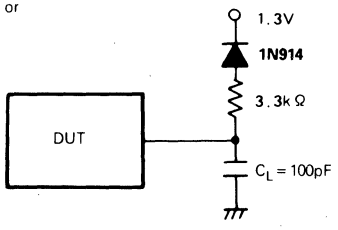
## AC WAVEFORMS




Test conditions for A.C. characteristics
Input voltage: $V_{IL}$=0.45V, $V_{IH}$=2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + $C_L$(100pF)

or




## CAPACITANCE

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $T_a$=25°C, f=1MHz, $V_I$=$V_O$=0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | | | 8 | 12 | pF |



MITSUBISHI ELECTRIC

## PROGRAM OPERATION

### FAST PROGRAMMING ALGORITHM

### DC ELECTRICAL CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu A$ |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH} = -400\mu A$ | 2.4 | | | V |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ | V |
| $I_{CC2}$ | $V_{CC}$ supply current | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

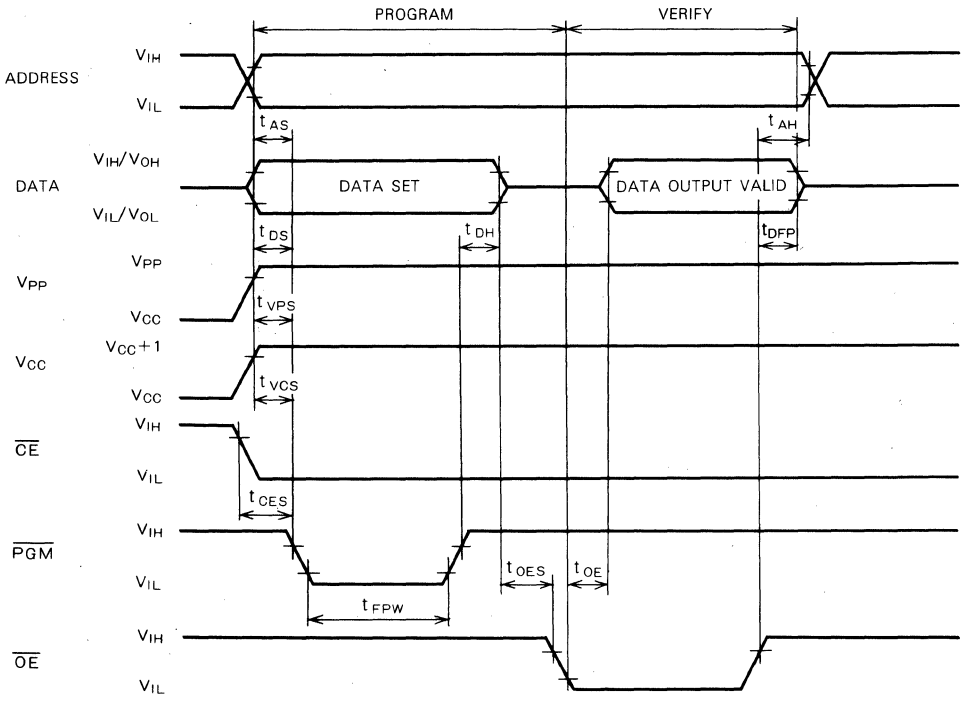
### AC ELECTRICAL CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address setup time | | 2 | | | $\mu s$ |
| $t_{OES}$ | $\overline{OE}$ set up time | | 2 | | | $\mu s$ |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu s$ |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu s$ |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu s$ |
| $t_{DFP}$ | Output enable to output float delay | | 0 | | 130 | ns |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | | $\mu s$ |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | | $\mu s$ |
| $t_{FPW}$ | $\overline{PGM}$ initial program pulse width | | 0.95 | 1 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ over program pulse width | | 3.8 | | 63 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu s$ |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

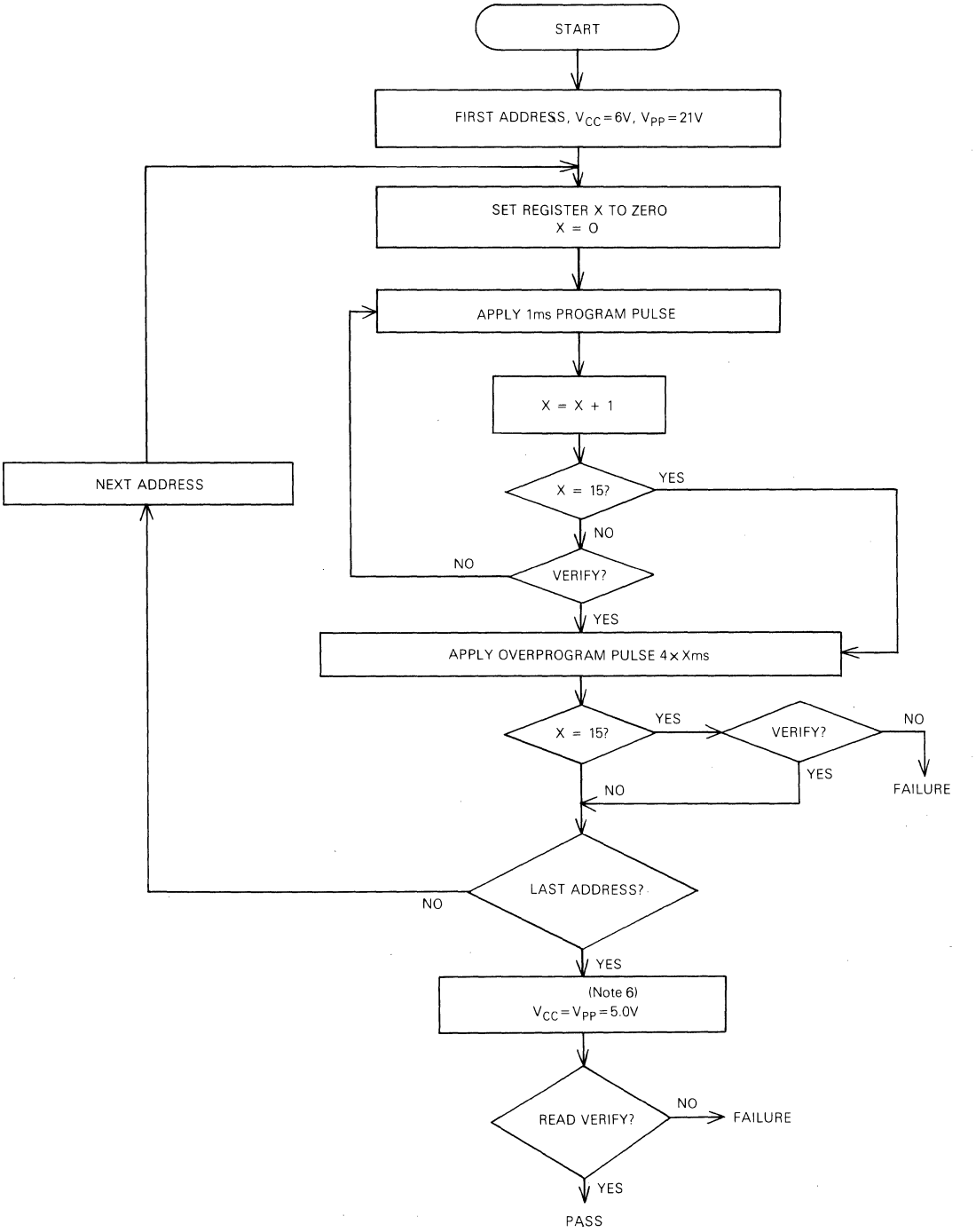
Note 5: $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

## AC WAVEFORMS




Test conditions for A.C. characteristics
Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V

## FAST PROGRAMMING ALGORITHM FLOW CHART




Note 6: $4.75 \leqq V_{CC} = V_{PP} \leqq 5.25V$

## CONVENTIONAL PROGRAMMING ALGORITHM

## DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

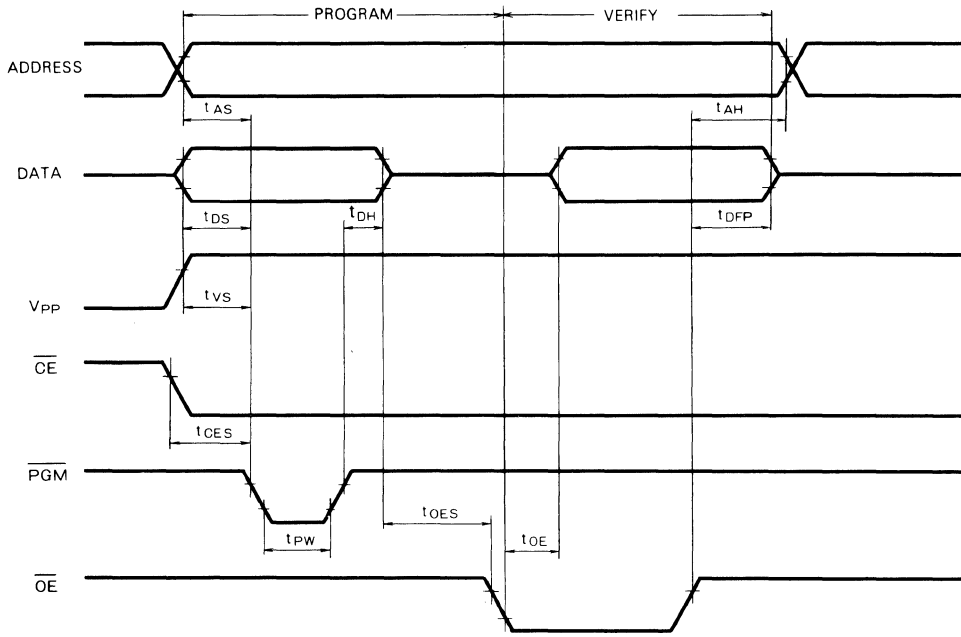
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu$A |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1$mA | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH} = -400\mu$A | 2.4 | | | V |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}+1$ | V |
| $I_{CC2}$ | $V_{CC}$ Supply current | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

## AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address set up time | | 2 | | | $\mu$s |
| $t_{OES}$ | $\overline{OE}$ setup time | | 2 | | | $\mu$s |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu$s |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu$s |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu$s |
| $t_{DFP}$ | Output enable to output delay | | 0 | | 130 | ns |
| $t_{VS}$ | $V_{PP}$ setup time | | 2 | | | $\mu$s |
| $t_{PW}$ | $\overline{PGM}$ Pulse width (during program) | | 45 | 50 | 55 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu$s |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

Note 7: $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

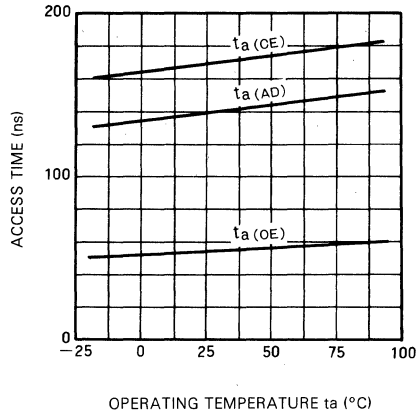
## AC WAVEFORMS



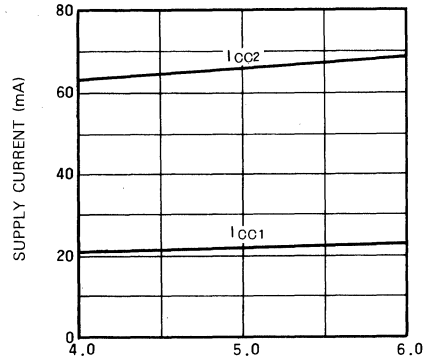

Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Reference voltage at timing measurement: Input 0.8V and 2V
Outputs 0.8V and 2V

## TYPICAL CHARACTERISTICS

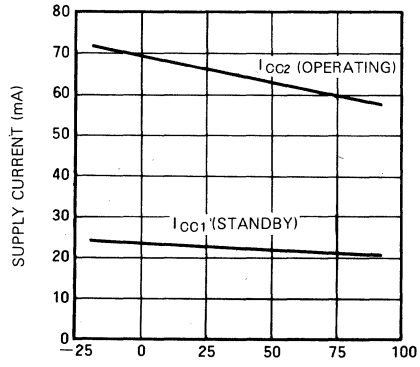
### ACCESS TIME VS OPERATING TEMPERATURE



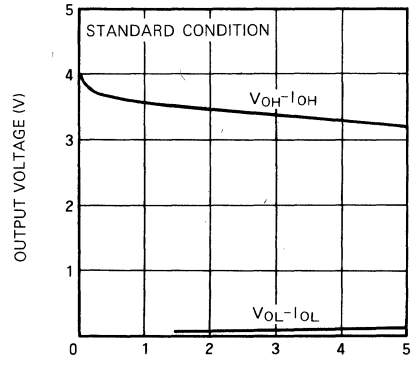

### SUPPLY CURRENT VS SUPPLY VOLTAGE




### SUPPLY CURRENT VS OPERATING TEMPERATURE




### OUTPUT CHARACTERISTICS



# M5M27C128K, -2, -3

## 131 072-BIT(16384-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM



## DESCRIPTION

The Mitsubishi M5M27C128K is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C128K is fabricated by N-channel double polysilicon Memory gate and CMOS technology for peripheral circuits, and available in a 28 pin DIL package with a transparent lid.

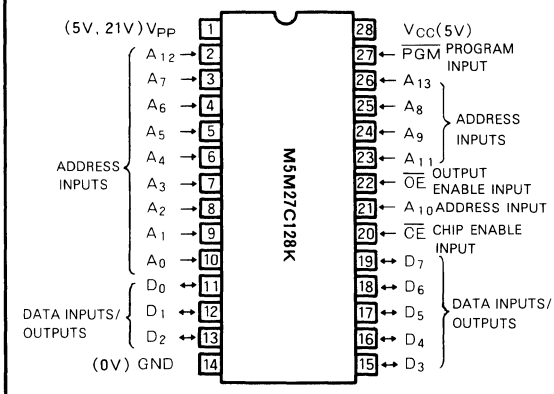
## FEATURES

- 16384 word x 8 bit organization
- Access time M5M27C128K-2 . . . . . 200ns (max.)
  M5M27C128K . . . . . 250ns (max.)
  M5M27C128K-3 . . . . . 300ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current ($I_{CC}$): Active . . . . . 30mA (max.)
  Standby . . . . 1mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIL package
- Fast programming algorithm
- Interchangeable with M5L27128K

## APPLICATION

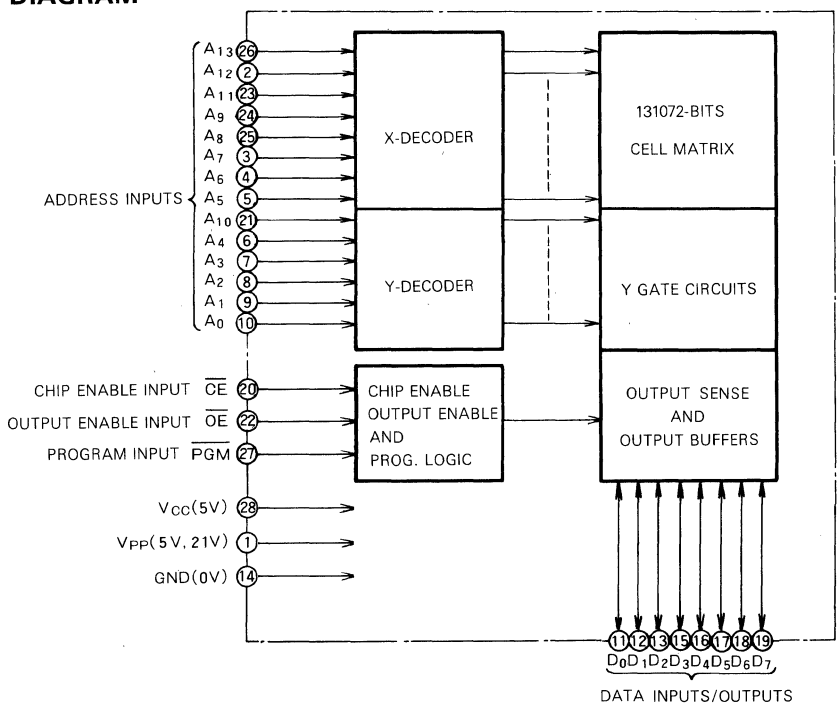
- Microcomputer systems and peripheral equipment

## PIN CONFIGURATION (TOP VIEW)




Outline 28K4

## BLOCK DIAGRAM



## 131 072-BIT(16384-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## FUNCTION

### Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

### Programming

### (Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6-24)

### (Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the $V_{PP}$ power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leqq t_{PW} \leqq$ 55 ms.

### Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm$^2$. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

## MODE SELECTION

| Mode \ Pins | $\overline{CE}$(20) | $\overline{OE}$(22) | $\overline{PGM}$(27) | $V_{PP}$(1) | $V_{CC}$(28) | Outputs (11~13, 15~19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | Data out |
| Standby | $V_{IH}$ | X* | X* | $V_{CC}$ | $V_{CC}$ | Floating |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PP}$ | $V_{CC}$ | Data in |
| Program verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PP}$ | $V_{CC}$ | Data out |
| Program inhibit | $V_{IH}$ | X* | X* | $V_{PP}$ | $V_{CC}$ | Floating |

*: X can be either $V_{IL}$ or $V_{IH}$.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $T_{opr}$ | Temperature under bias | −10~80 | °C |
| $T_{stg}$ | Storage temperature | −65~125 | °C |
| $V_{I1}$ | All input or output voltage (Note 2) | −0.6~7 | V |
| $V_{I2}$ | $V_{PP}$ supply voltage during programming (Note 2) | −0.6~22.0 | V |

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.



MITSUBISHI ELECTRIC

## READ OPERATION

## DC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input load current | $V_{IN}=5.25V$ | | | 10 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}=5.25V$ | | | 10 | μA |
| $I_{PP1}$ | $V_{PP}$ current read | $V_{PP}=5.25V$ | | 1 | 100 | μA |
| $I_{CC1}$ | $V_{CC}$ current standby | $\overline{CE}=V_{IH}$ | | | 1 | mA |
| | | $\overline{CE}=V_{CC}$ | | 1 | 100 | μA |
| $I_{CC2}$ | $V_{CC}$ current Active | $\overline{CE}=\overline{OE}=V_{IL}$ | | | 30 | mA |
| | | f=4MHz | | | 30 | mA |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}+1$ | V |
| $V_{OL}$ | Output low voltage | $I_{OL}=2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}=-400\mu A$ | 2.4 | | | V |

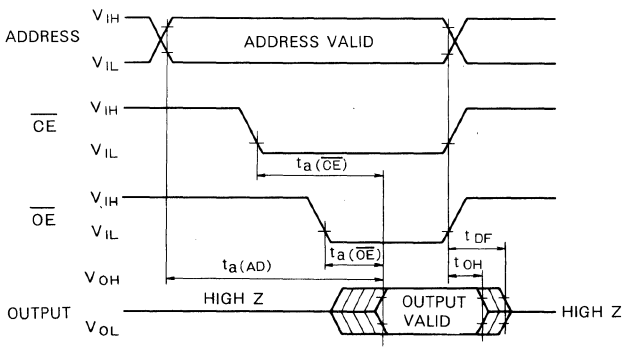
Note 3: Typical values are at Ta=25°C and nominal supply voltages.

## AC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M27C128K-2 | | M5M27C128K | | M5M27C128K-3 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{a(AD)}$ | Address to output delay | $\overline{CE}=\overline{OE}=V_{IL}$ | | 200 | | 250 | | 300 | ns |
| $t_{a(\overline{CE})}$ | $\overline{CE}$ to output delay | $\overline{OE}=V_{IL}$ | | 200 | | 250 | | 300 | ns |
| $t_{a(\overline{OE})}$ | Output enable to output delay | $\overline{CE}=V_{IL}$ | | 75 | | 100 | | 120 | ns |
| $t_{DF}$ | Output enable high to output float | $\overline{CE}=V_{IL}$ | 0 | 60 | 0 | 85 | 0 | 105 | ns |
| $t_{OH}$ | Output hold from $\overline{CE}$ or $\overline{OE}$ | $\overline{CE}=\overline{OE}=V_{IL}$ | 0 | | 0 | | 0 | | ns |

Note 4: $V_{CC}$ must be applied simultaneously $V_{PP}$ and removed simultaneously $V_{PP}$.

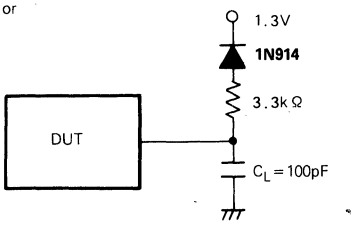
## AC WAVEFORMS




Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + $C_L$(100pF)

or




## CAPACITANCE

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $T_a=25°C$, f=1MHz, $V_I=V_O=0V$ | | 4 | 6 | pF |
| $C_{OUT}$ | Output capacitance | | | 8 | 12 | pF |

## PROGRAM OPERATION

## FAST PROGRAMMING ALGORITHM

## DC ELECTRICAL CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

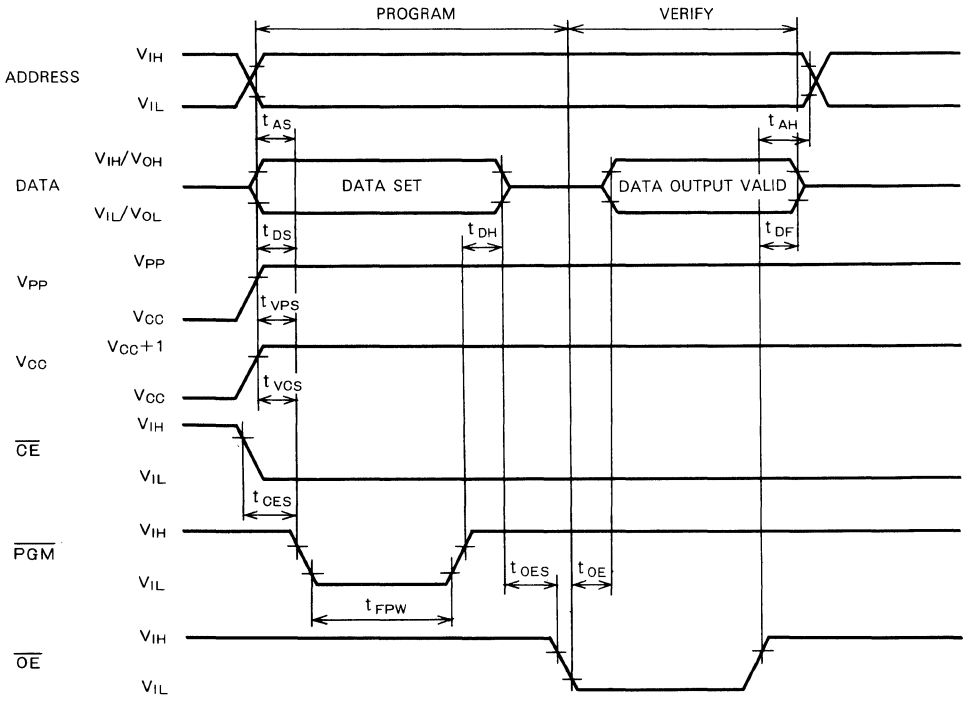
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu A$ |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH} = -400\mu A$ | 2.4 | | | V |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ | V |
| $I_{CC2}$ | $V_{CC}$ supply current | | | | 30 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

## AC ELECTRICAL CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

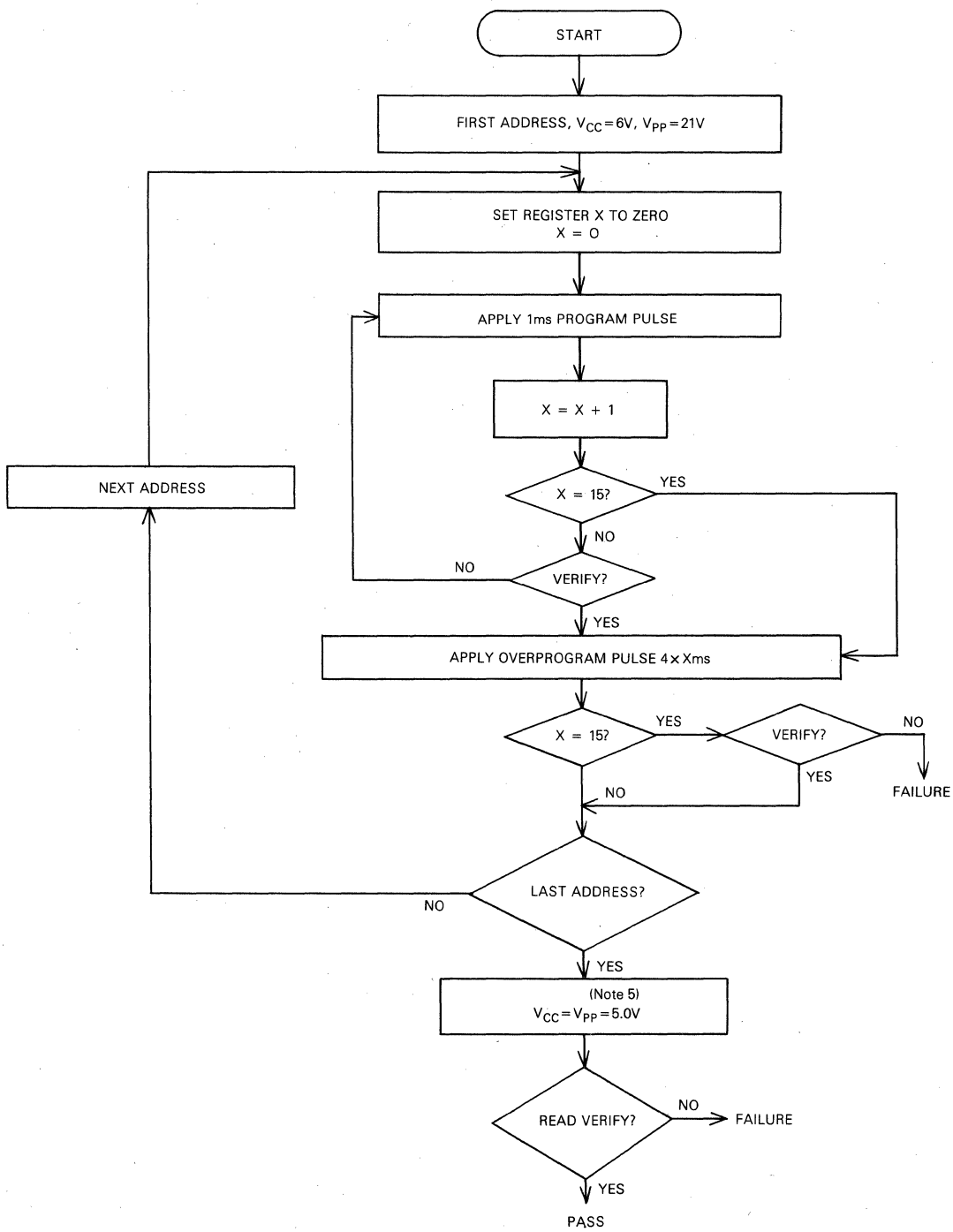
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address setup time | | 2 | | | $\mu s$ |
| $t_{OES}$ | $\overline{OE}$ set up time | | 2 | | | $\mu s$ |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu s$ |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu s$ |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu s$ |
| $t_{DF}$ | Chip enable to output float delay | | 0 | | 130 | ns |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | | $\mu s$ |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | | $\mu s$ |
| $t_{FPW}$ | $\overline{PGM}$ initial program pulse width | | 0.95 | 1 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ over program pulse width | | 3.8 | | 63 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu s$ |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

## AC WAVEFORMS




Test conditions for A.C. characteristics
Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

## FAST PROGRAMMING ALGORITHM FLOW CHART




Note 5: $4.75 \leqq V_{CC} = V_{PP} \leqq 5.25V$

## 131 072-BIT(16384-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## CONVENTIONAL PROGRAMMING ALGORITHM

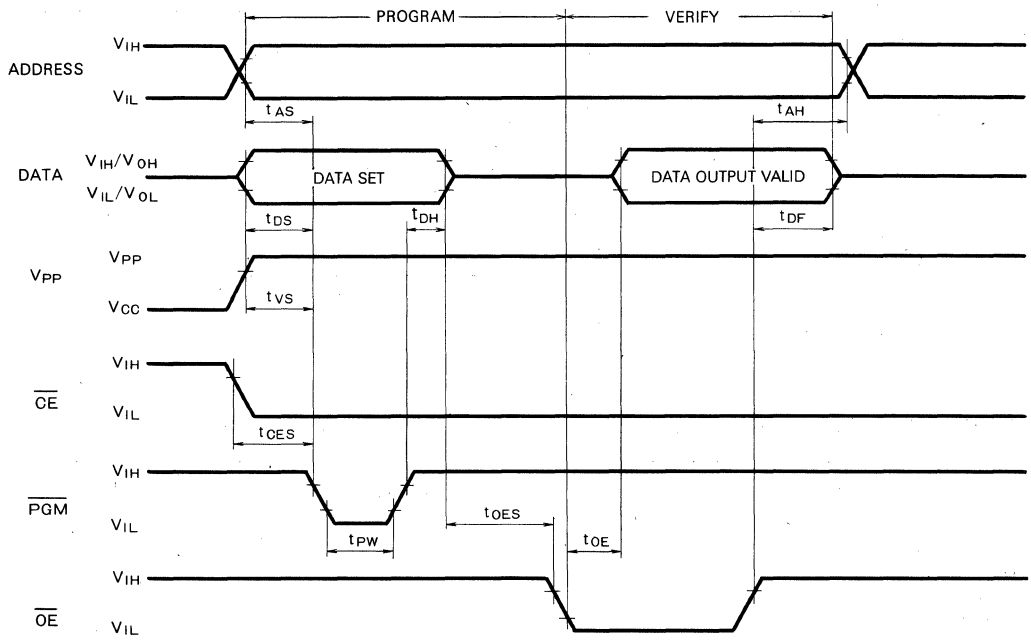
### DC ELECTRICAL CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{LI}$ | Input current | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | $\mu A$ |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1mA$ | | | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH} = -400\mu A$ | 2.4 | | | V |
| $V_{IL}$ | Input low voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}+1$ | V |
| $I_{CC2}$ | $V_{CC}$ Supply current | | | | 30 | mA |
| $I_{PP}$ | $V_{PP}$ Supply current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |

### AC ELECTRICAL CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{AS}$ | Address set up time | | 2 | | | $\mu s$ |
| $t_{OES}$ | $\overline{OE}$ setup time | | 2 | | | $\mu s$ |
| $t_{DS}$ | Data setup time | | 2 | | | $\mu s$ |
| $t_{AH}$ | Address hold time | | 0 | | | $\mu s$ |
| $t_{DH}$ | Data hold time | | 2 | | | $\mu s$ |
| $t_{DF}$ | Chip enable to output delay | | 0 | | 130 | ns |
| $t_{VS}$ | $V_{PP}$ setup time | | 2 | | | $\mu s$ |
| $t_{PW}$ | $\overline{PGM}$ Pulse width (during program) | | 45 | 50 | 55 | ms |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | $\mu s$ |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

## AC WAVEFORMS

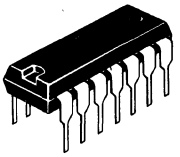



Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: $V_{IL}$ = 0.45V, $V_{IH}$ = 2.4V
Reference voltage at timing measurement: Input 1V and 2V
Outputs 0.8V and 2V

# MOS EAROM

7

# M58653P



## 700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

### DESCRIPTION

The M58653P is a serial input/output 700 bit electrically erasable and reprogrammable ROM organized as 50 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

### FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms/word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . . $10^5$ times (min)
- Number of read access unrefreshed. . . $10^9$ times (min)
- 5V I/O interface

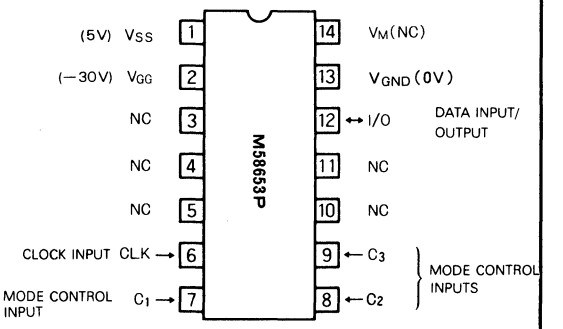
### APPLICATION

- Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

### FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to $C_1$, $C_2$, and $C_3$. Data is stored by internal negative writing pulses that selectively tunnel charges into the $SiO_2$—$Si_3N_4$ interface of the gate insulators of the MNOS memory transistors.

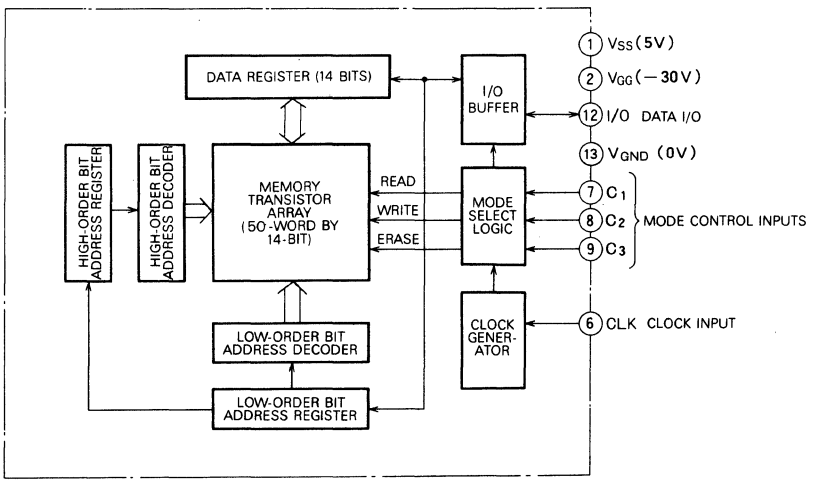
### PIN CONFIGURATION (TOP VIEW)




Outline 14P4

NC: NO CONNECTION

### BLOCK DIAGRAM



# 700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## PIN DESCRIPTION

| Pin | Name | Functions |
|---|---|---|
| I/O | I/O | In the accept address and accept data modes, used for input.<br>In the shift data output mode, used for output.<br>In the standby, read, erase and write modes, this pin is in a floating state. |
| $V_M$ | Test | Used for testing purposes only. It should be left unconnected during normal operation. |
| $V_{SS}$ | Chip substrate voltage | Normally connected to +5V. |
| $V_{GG}$ | Power supply voltage | Normally connected to −30V. |
| CLK | Clock input | 14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode. |
| $C_1 \sim C_3$ | Mode control input | Used to select the operation mode. |
| $V_{GND}$ | Ground voltage | Connected to ground (0V) |

## OPERATION MODES

| $C_1$ | $C_2$ | $C_3$ | Functions |
|---|---|---|---|
| H | H | H | Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state. |
| H | H | L | Not used. |
| H | L | H | Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level. |
| H | L | L | Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits. |
| L | H | H | Read mode: The addressed word is read from the memory into the data register. |
| L | H | L | Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse. |
| L | L | H | Write mode: The data contained in the data register is written into the location designated by the address registers. |
| L | L | L | Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged. |

# 700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{GG}$ | Supply voltage | With respect to $V_{SS}$ | 0.3 ~ −40 | V |
| $V_I$ | Input voltage | | 0.3 ~ −20 | V |
| $V_O$ | Output voltage | | 0.3 ~ −20 | V |
| Tstg | Storage temperature range | | −40 ~ 125 | ℃ |
| Topr | Operating free-air temperature range | | −10 ~ 70 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{GG}$-$V_{SS}$ | Supply voltage | −32.2 | −35 | −37.8 | V |
| $V_{SS}$-$V_{GND}$ | Supply voltage | 4.75 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}$-6.5 | | $V_{SS}$-4.25 | V |

Note 1:
The order of $V_{SS}$ $V_{GG}$ with on or off.
With on, $V_{GG}$ is turned on after $V_{SS}$ is done.
With off, $V_{SS}$ is turned off after $V_{GG}$ is done.

## ELECTRICAL CHARACTERISTICS (Ta = −10 ~ 70℃, $V_{GG}$-$V_{SS}$ = −35V ± 8%, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | $V_{SS}$-6.5 | | $V_{SS}$-4.25 | V |
| $I_{IL}$ | Low-level input current | $V_I$-$V_{SS}$ = −6.5V | | | ±10 | μA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | $V_O$-$V_{SS}$ = −6.5V | | | ±10 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −200μA | $V_{SS}$−1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 10μA | | | $V_{GND}$+0.5 | V |
| $I_{GG}$ | Supply current from $V_{GG}$ | $I_O$ = 0μA | | 5.5 | 8.8 | mA |

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

## TIMING REQUIREMENTS (Ta = −10 ~ 70℃, $V_{GG}$-$V_{SS}$ = −35V ± 8%, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

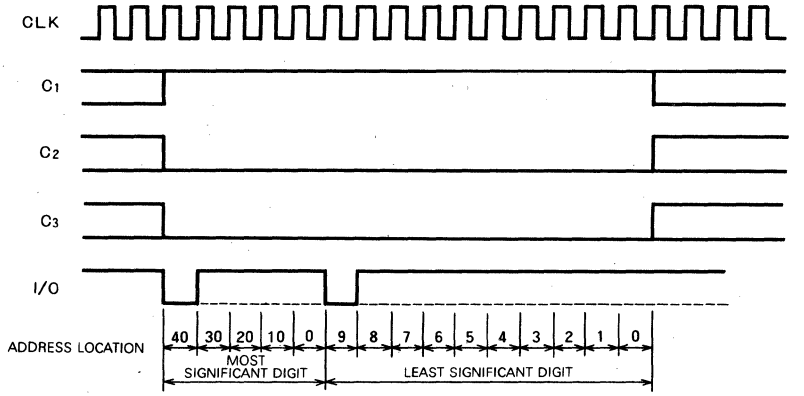
| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| f(φ) | Clock frequency | fφ | | 11.2 | 14 | 16.8 | kHz |
| D(φ) | Clock duty cycle | Dφ | | 30 | 50 | 55 | % |
| tw(w) | Write time | tw | | 16 | 20 | 24 | ms |
| tw(E) | Erase time | te | | 16 | 20 | 24 | ms |
| tr, tf | Risetime, falltime | tr, tf | | | | 1 | μs |
| tsu(c−φ) | Control setup time before the fall of the clock pulse | tCS | | 0 | | | ns |
| th(φ−c) | Control hold time after the rise of the clock pulse | tCH | | 0 | | | ns |

## SWITCHING CHARACTERISTICS (Ta = −10 ~ 70℃, $V_{GG}$ = −35V ± 8%, unless otherwise noted.)

| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| ta(c) | Read access time | tPW | $C_L$ = 100PF, $V_{OH}$ = $V_{SS}$ − 2V, $V_{OL}$ = $V_{GND}$ + 1.5V | | | 20 | μs |
| ts | Unpowered nonvolatile data retention time | Ts | $N_{EW}$ = $10^4$, tw(w) = 20ms, tw(E) = 20ms | 10 | | | Year |
| | | Ts | $N_{EW}$ = $10^5$, tw(w) = 20ms, tw(E) = 20ms | 1 | | | Year |
| $N_{EW}$ | Number of erase/write cycles | Nw | | $10^5$ | | | Times |
| $N_{RA}$ | Number of read access unrefreshed | $N_{RA}$ | | $10^9$ | | | Times |
| tdv | Data valid time | tPW | | | | 20 | μs |

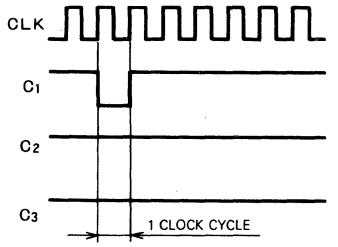
## TIMING DIAGRAM

### Accept Address Mode

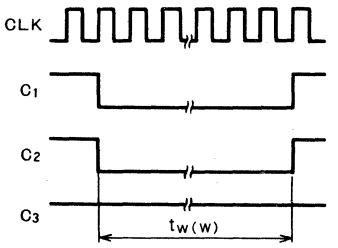



Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 49.

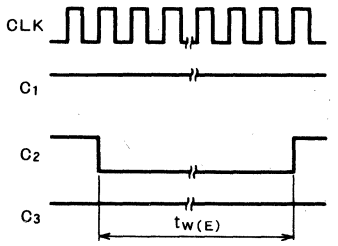
### Read Mode



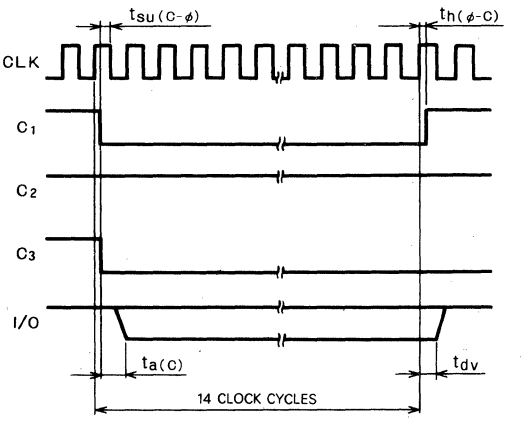

### Write Mode



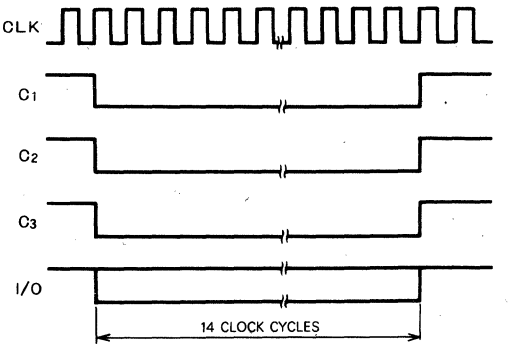

### Erase Mode



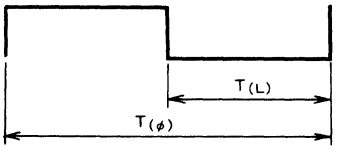

### Shift Data Output Mode




### Accept Data Mode



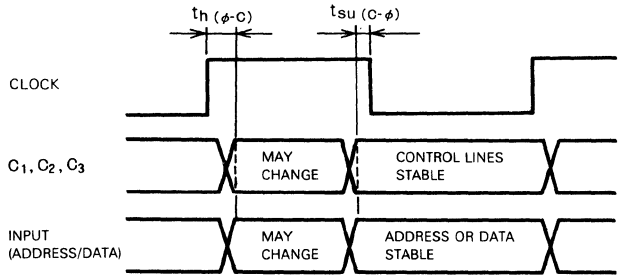
- **The difinition of clock duty cycle, D ($\phi$)**



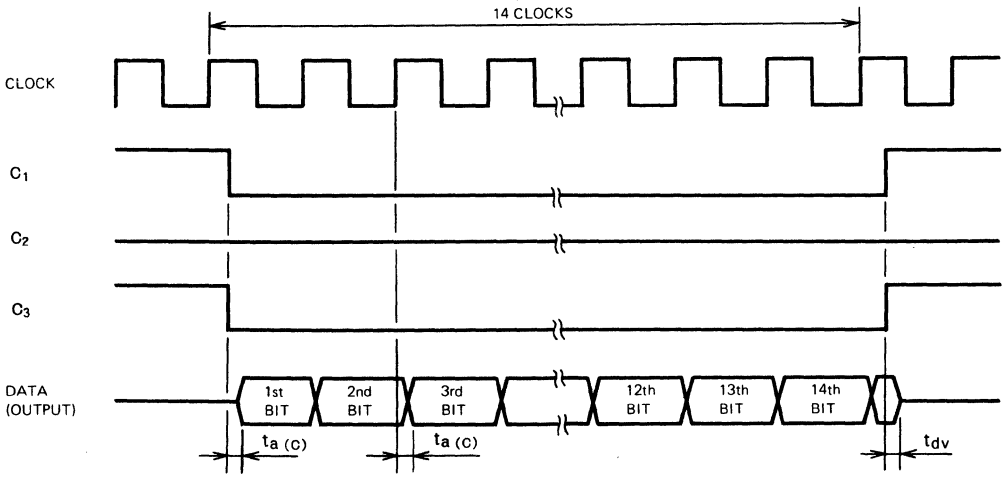

$D(\phi) = T(L)/T(\phi)$

- **Timing of data input and mode control inputs**

Mode control inputs, $C_1$, $C_2$, $C_3$ and input signal my change, when clock is 'H' level.

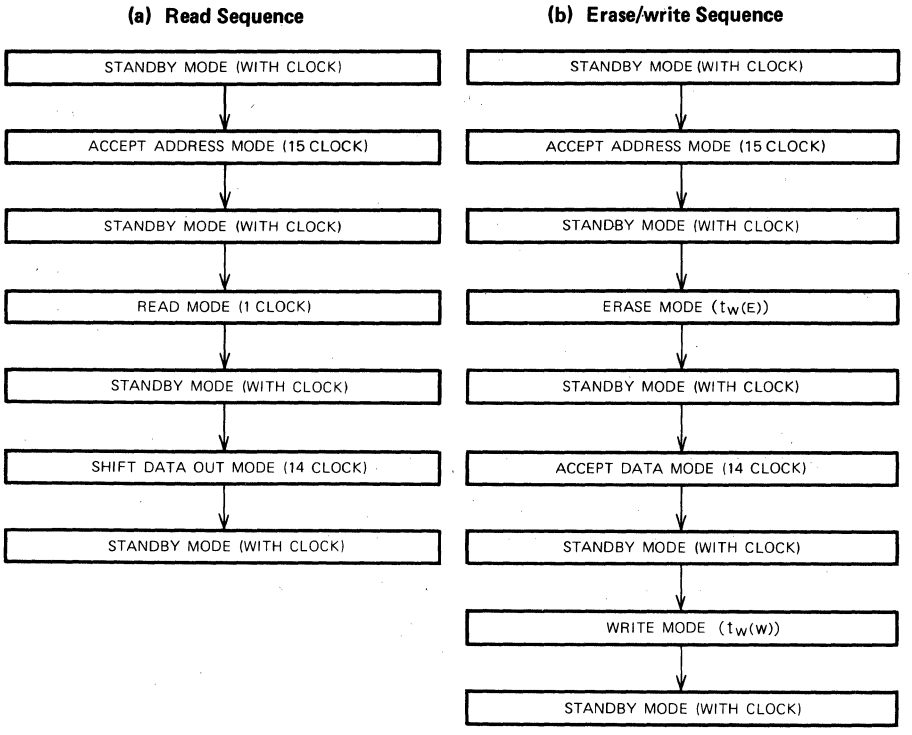


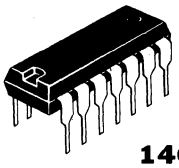

- **Timing of data output**




The 1st bit of output data is output after access time of $t_{a(C)}$ from the mode control transition. And other bits are output after $t_{a(C)}$ from positive edge of clock.

## • Operating sequential flow







# M58657P

## 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

### DESCRIPTION

The M58657P is a serial input/output 1400 bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

### FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . . $10^5$ times (min)
- Number of read access unrefreshed. . . $10^9$ times (min)
- 5V I/O interface

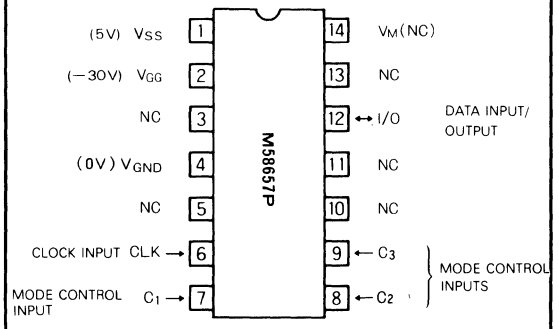
### APPLICATION

- Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

### FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to $C_1$, $C_2$, and $C_3$. Data is stored by internal negative writing pulses that selectively tunnel charges into the $SiO_2$—$Si_3N_4$ interface of the gate insulators of the MNOS memory transistors.

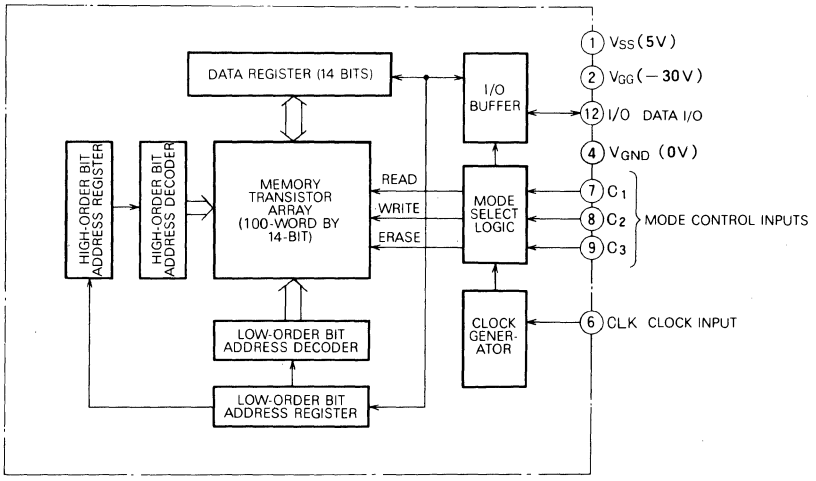
### PIN CONFIGURATION (TOP VIEW)




Outline 14P4

NC NO CONNECTION

### BLOCK DIAGRAM



# 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## PIN DESCRIPTION

| Pin | Name | Functions |
|---|---|---|
| I/O | I/O | In the accept address and accept data modes, used for input.<br>In the shift data output mode, used for output.<br>In the standby, read, erase and write modes, this pin is in a floating state. |
| $V_M$ | Test | Used for testing purposes only. It should be left unconnected during normal operation. |
| $V_{SS}$ | Chip substrate voltage | Normally connected to +5V. |
| $V_{GG}$ | Power supply voltage | Normally connected to −30V. |
| CLK | Clock input | 14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode. |
| $C_1 \sim C_3$ | Mode control input | Used to select the operation mode. |
| $V_{GND}$ | Ground voltage | Connected to ground (0V) |

## OPERATION MODES

| $C_1$ | $C_2$ | $C_3$ | Functions |
|---|---|---|---|
| H | H | H | Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state. |
| H | H | L | Not used. |
| H | L | H | Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level. |
| H | L | L | Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits. |
| L | H | H | Read mode: The addressed word is read from the memory into the data register. |
| L | H | L | Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse. |
| L | L | H | Write mode: The data contained in the data register is written into the location designated by the address registers. |
| L | L | L | Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged. |

# 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{GG}$ | Supply voltage | With respect to $V_{SS}$ | 0.3 ~ −40 | V |
| $V_I$ | Input voltage | | 0.3 ~ −20 | V |
| $V_O$ | Output voltage | | 0.3 ~ −20 | V |
| $T_{stg}$ | Storage temperature range | | −40 ~ 125 | ℃ |
| $T_{opr}$ | Operating free-air temperature range | | −10 ~ 70 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{GG}$-$V_{SS}$ | Supply voltage | −32.2 | −35 | −37.8 | V |
| $V_{SS}$-$V_{GND}$ | Supply voltage | 4.75 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}$-6.5 | | $V_{SS}$-4.25 | V |

Note 1:
The order of $V_{SS}$ $V_{GG}$ with on or off.
With on, $V_{GG}$ is turned on after $V_{SS}$ is done.
With off, $V_{SS}$ is turned off after $V_{GG}$ is done.

## ELECTRICAL CHARACTERISTICS (Ta = −10 ~ 70℃, $V_{GG}$-$V_{SS}$ = −35V ± 8 %, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | $V_{SS}$-6.5 | | $V_{SS}$-4.25 | V |
| $I_{IL}$ | Low-level input current | $V_I$-$V_{SS}$ = −6.5V | | | ± 10 | μA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | $V_O$-$V_{SS}$ = −6.5V | | | ± 10 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −200μA | $V_{SS}$−1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 10μA | | | $V_{GND}$+0.5 | V |
| $I_{GG}$ | Supply current from $V_{GG}$ | $I_O$ = 0μA | | 5.5 | 8.8 | mA |

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

## TIMING REQUIREMENTS (Ta = −10 ~ 70℃, $V_{GG}$-$V_{SS}$ = −35V ± 8 %, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

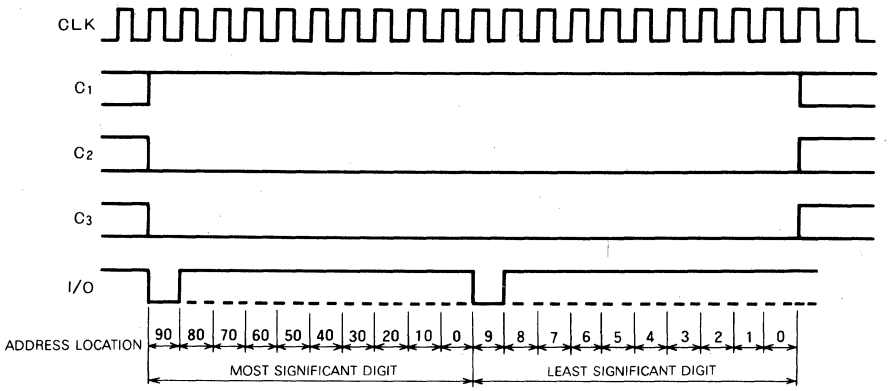
| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| f(φ) | Clock frequency | fφ | | 10 | 14 | 17 | kHz |
| D(φ) | Clock duty cycle | Dφ | | 30 | 50 | 55 | % |
| tw(W) | Write time | tw | | 16 | 20 | 24 | ms |
| tw(E) | Erase time | te | | 16 | 20 | 24 | ms |
| tr tf | Risetime, falltime | tr, tf | | | | 1 | μs |
| tsu(c−φ) | Control setup time before the fall of the clock pulse | tCS | | 0 | | | ns |
| th(φ−c) | Control hold time after the rise of the clock pulse | tCH | | 0 | | | ns |

## SWITCHING CHARACTERISTICS (Ta = −10 ~ 70℃, $V_{GG}$ = −35V ± 8 %, unless otherwise noted.)

| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| ta(c) | Read access time | tPW | $C_L$ = 100pF, $V_{OH}$ = $V_{SS}$ − 2V, $V_{OL}$ = $V_{GND}$ + 1.5V | | | 20 | μs |
| ts | Unpowered nonvolatile data retention time | TS | $N_{EW}$ = $10^4$, tw(W) = 20ms, tw(E) = 20ms | 10 | | | Year |
| | | TS | $N_{EW}$ = $10^5$, tw(W) = 20ms, tw(E) = 20ms | 1 | | | Year |
| $N_{EW}$ | Number of erase/write cycles | NW | | $10^5$ | | | Times |
| $N_{RA}$ | Number of read access unrefreshed | $N_{RA}$ | | $10^9$ | | | Times |
| tdv | Data valid time | tPW | | | | 20 | μs |

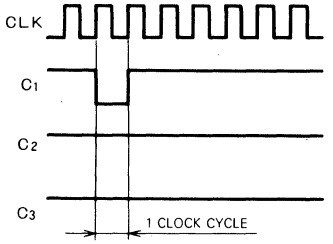
## TIMING DIAGRAM

### Accept Data Mode

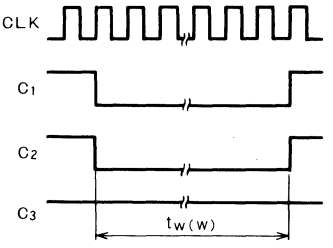



Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 99.

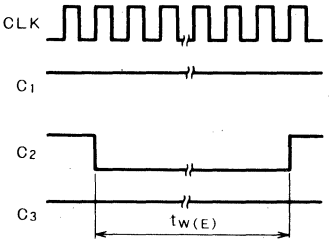
### Read Mode



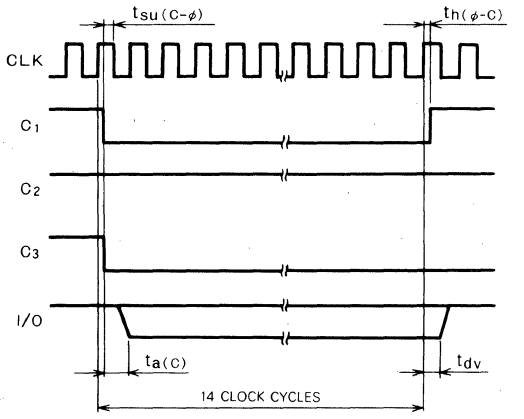

### Write Mode



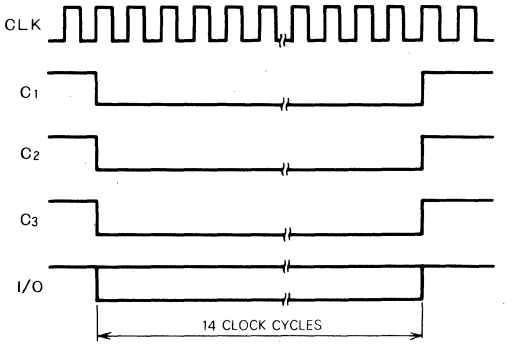

### Erase Mode



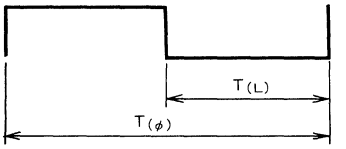

### Shift Data Output Mode




### Accept Data Mode



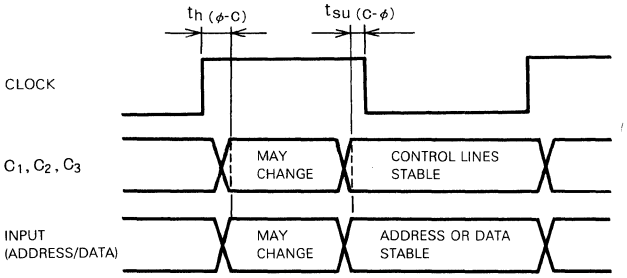
- **The difinition of clock duty cycle, D ($\phi$)**



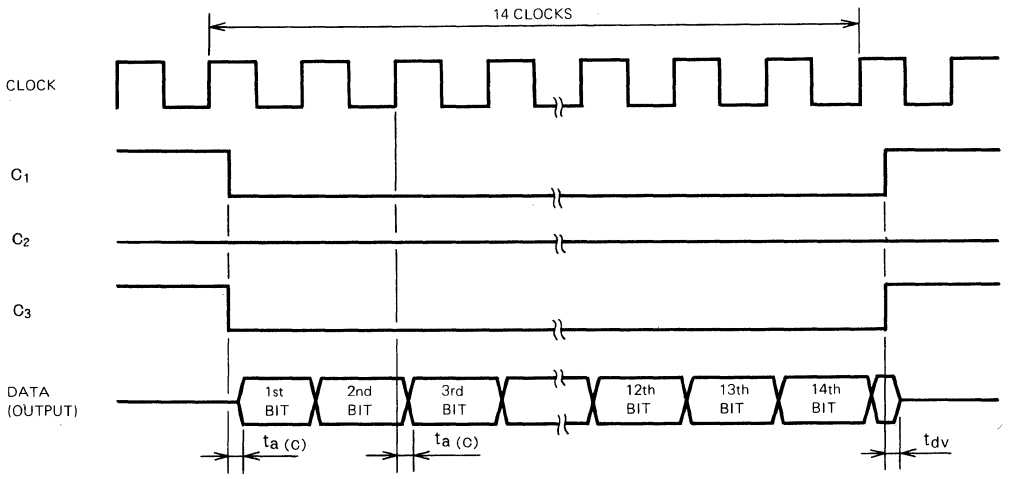

$D_{(\phi)} = T_{(L)} / T_{(\phi)}$

- **Timing of data input and mode control inputs**

Mode control inputs, $C_1$, $C_2$, $C_3$ and input signal my change, when clock is 'H' level.

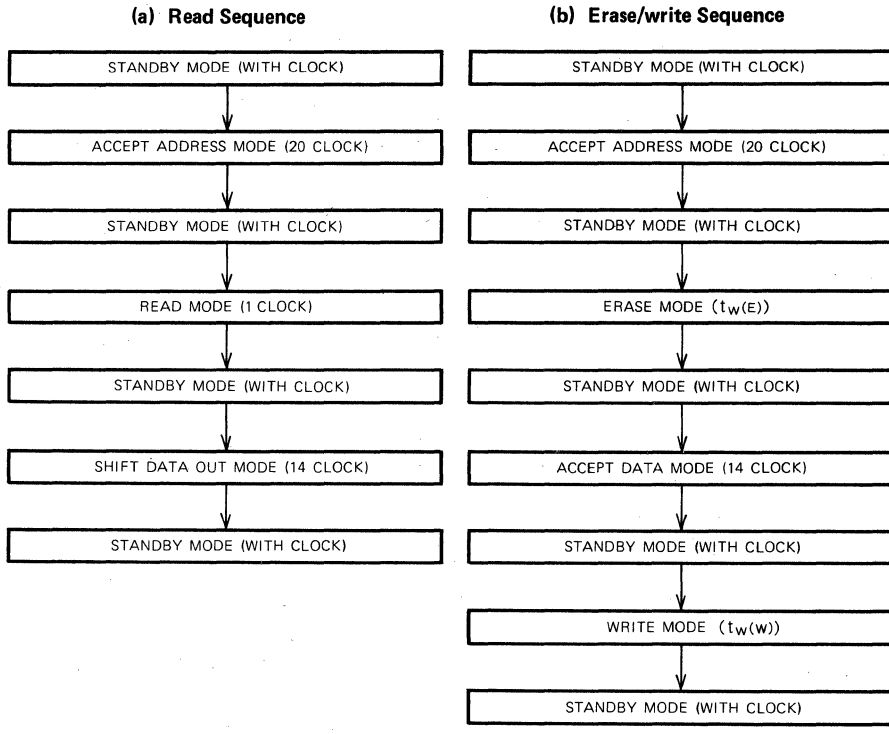


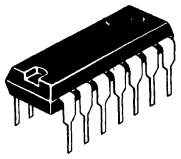

- **Timing of data output**




The 1st bit of output data is output after access time of $t_{a(C)}$ from the mode control transition. And other bits are output after $t_{a(C)}$ from positive edge of clock.

- **Operating sequential flow**







# M58658P

## 320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

### DESCRIPTION

The M58658P is a serial input/output 320 bit electrically erasable and reprogrammable ROM organized as 20 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

### FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . . $10^5$ times (min)
- Number of read access unrefreshed. . . $10^9$ times (min)
- 5V I/O interface

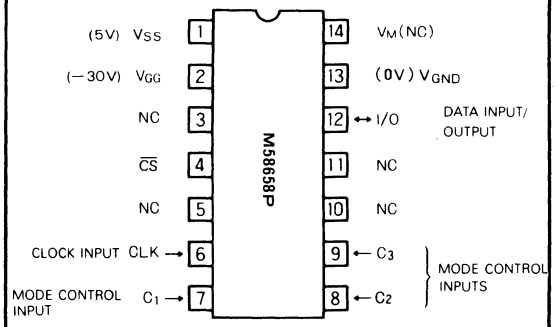
### APPLICATION

- Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

### FUNCTION

The address is designated by two consecutive one-of-four coded digits. Eight modes—accept address, AD accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to $C_1$, $C_2$, and $C_3$. Data is stored by internal negative writing pulses that selectively tunnel charges into the $SiO_2$–$Si_3N_4$ interface of the gate insulators of the MNOS memory transistors.

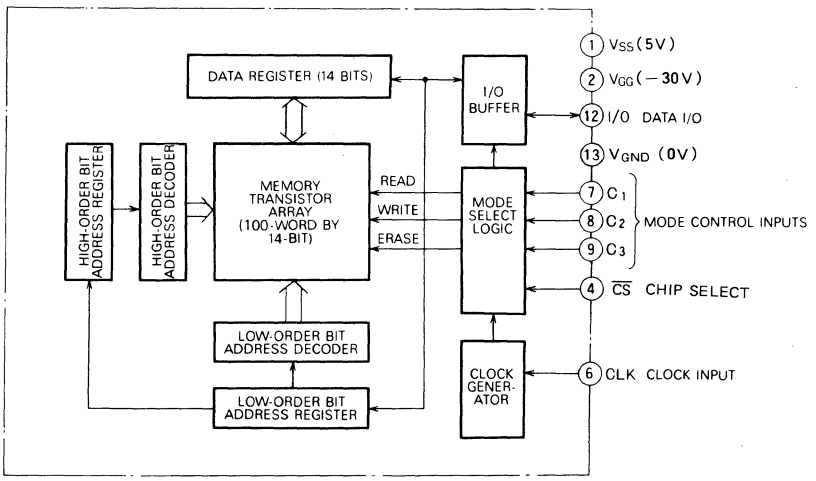
### PIN CONFIGURATION (TOP VIEW)




Outline 14P4

NC: NO CONNECTION

### BLOCK DIAGRAM



## 320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

### PIN DESCRIPTION

| Pin | Name | Functions |
|---|---|---|
| I/O | I/O | In the accept address AD accept address and accept data modes, used for input.<br>In the shift data output mode, used for output.<br>In the standby, read, erase and write modes, this pin is in a floating state. |
| $V_M$ | Test | Used for testing purposes only. It should be left unconnected during normal operation. |
| $V_{SS}$ | Chip substrate voltage | Normally connected to +5V. |
| $V_{GG}$ | Power supply voltage | Normally connected to −30V. |
| CLK | Clock input | Required for all operating modes, when $\overline{CS}$ is low. |
| $C_1 \sim C_3$ | Mode control input | Used to select the operation mode. |
| $V_{GND}$ | Ground voltage | Connected to ground (0V) |
| $\overline{CS}$ | Chip select | Used for chip selection in "L" |

### OPERATION MODES

| $C_1$ | $C_2$ | $C_3$ | Functions |
|---|---|---|---|
| H | H | H | Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state. |
| H | H | L | Additional data (AD) accept address: Data presented at the I/O pin is shifted into the AD address registers one bit with each clock pulse. The address is designated by two one-of-four coded digits. 4-word address is assigned in this mode. |
| H | L | H | Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level. |
| H | L | L | Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-four-coded digits. 16-word address is assigned in this mode. |
| L | H | H | Read mode: The addressed word is read from the memory into the data register. |
| L | H | L | Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse. |
| L | L | H | Write mode: The data contained in the data register is written into the location designated by the address registers. |
| L | L | L | Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged. |

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{GG}$ | Supply voltage | With respect to $V_{SS}$ | 0.3 ~ −40 | V |
| $V_I$ | Input voltage | | 0.3 ~ −20 | V |
| $V_O$ | Output voltage | | 0.3 ~ −20 | V |
| $T_{stg}$ | Storage temperature range | | −40 ~ 125 | ℃ |
| $T_{opr}$ | Operating free-air temperature range | | −10 ~ 70 | ℃ |

### RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{GG}-V_{SS}$ | Supply voltage | −32.2 | −35 | −37.8 | V |
| $V_{SS}-V_{GND}$ | Supply voltage | 4.75 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{SS}-1$ | | $V_{SS}+0.3$ | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}-6.5$ | | $V_{SS}-4.25$ | V |

## 320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

### ELECTRICAL CHARACTERISTICS ($T_a$ = −10 ~ 70°C, $V_{GG}$-$V_{SS}$ = −35V ± 8%, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | $V_{SS}-1$ | | $V_{SS}+0.3$ | V |
| $V_{IL}$ | Low-level input voltage | | $V_{SS}-6.5$ | | $V_{SS}-4.25$ | V |
| $I_{IL}$ | Low-level input current CLK, C1, C2, C3, I/O | $V_I-V_{SS}=-6.5V$ | −10 | | +10 | μA |
| $R_I$ | Input pull-up resistance, $\overline{CS}$ | | | 30 | | kΩ |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | $V_O-V_{SS}=-6.5V$ | −10 | | +10 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}=-200\mu A$ | $V_{SS}-1$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}=10\mu A$ | | | $V_{GND}+0.5$ | V |
| $I_{GG}$ | Supply current from $V_{GG}$ | $I_O=0\mu A$ | | 5.5 | 8.8 | mA |

Note 1: Typical values are at Ta = 25°C and $V_{GG}$-$V_{SS}$ = −35V.

### TIMING REQUIREMENTS ($T_a$ = −10 ~ 70°C, $V_{GG}$-$V_{SS}$ = −35V ± 8%, $V_{SS}$-$V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{L(\phi)}$ | Negative clock pulse width | | 30 | | | μs |
| $T_{H(\phi)}$ | Positive clock pulse width | | 33 | | | μs |
| $T_{(\phi)}$ | Clock period | | | | 300 | μs |
| $t_W$ | Write time | | 16 | 20 | 24 | ms |
| $t_E$ | Erase time | | 16 | 20 | 24 | ms |
| $t_r$, $t_f$ | Risetime, fall time | | | | 1 | μs |
| $t_{su}$ | Control setup time before the fall of the clock pulse | | 1 | | | μs |
| $t_h$ | Control hold time after the rise of the clock pulse | | 0 | | | μs |
| $t_{ss}$ | Clock control setup time before the fall of $\overline{CS}$ | | 1 | | | μs |
| $t_{hs}$ | Clock control hold time after the rise of $\overline{CS}$ | | 1 | | | μs |

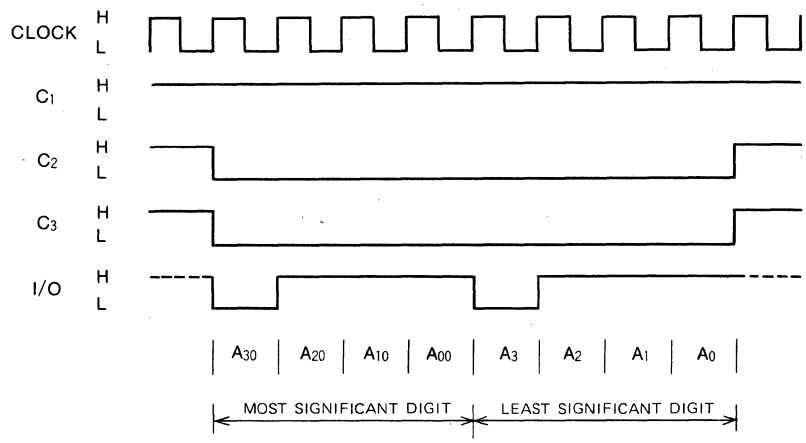
### SWITCHING CHARACTERISTICS ($T_a$ = −10 ~ 70°C, $V_{GG}$ = −35V ± 8%, unless otherwise noted.)

| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| ta(c) | Read access time | $t_{PW}$ | $C_L$ = 100pF, $V_{OH}=V_{SS}-2V$, $V_{OL}=V_{GND}+1.5V$ | | | 20 | μs |
| ts | Unpowered nonvolatile data retention time | $T_S$ | $N_{EW}=10^4$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$ | 10 | | | Year |
| | | $T_S$ | $N_{EW}=10^5$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$ | 1 | | | Year |
| $N_{EW}$ | Number of erase/write cycles | $N_W$ | | $10^5$ | | | Times |
| $N_{RA}$ | Number of read access unrefreshed | $N_{RA}$ | | $10^9$ | | | Times |
| tdv | Data valid time | $t_{PW}$ | | | | 20 | μs |

## TIMING DIAGRAM

### Accept Address Mode (8 clock)

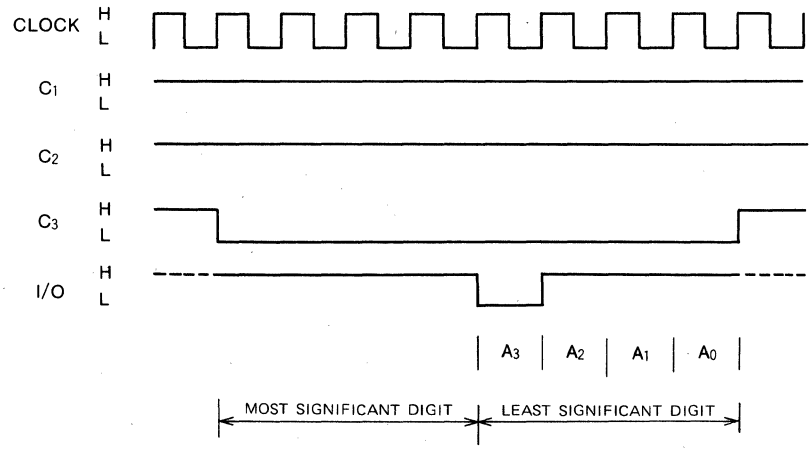
$\overline{CS}$ : L




Note 2: The addresses from $A_{00}$ to $A_{33}$ are designated by two one-of-four coded digits. The above figure shows designation of address $A_{33}$ (decimal address 15).

### AD Accept Address Mode (8 clock)

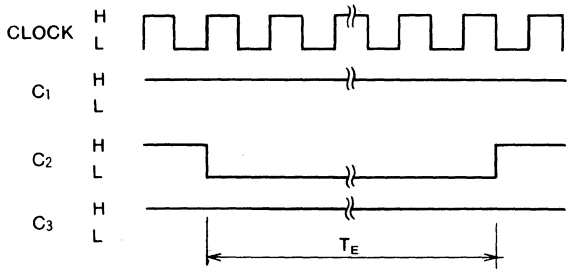
$\overline{CS}$ : L



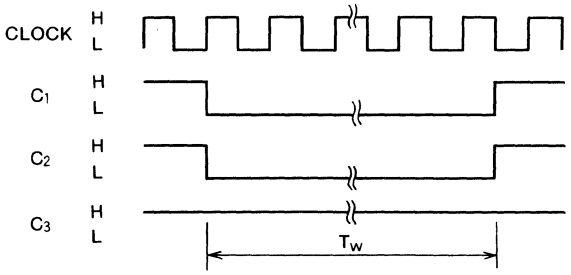

Note 3: In the AD accept address mode, the higher four are set high, and the lower four digits are designated by one of the four coded digits. This address mode allows designation of addresses from $A_0$ to $A_3$. Each address has a 16 bits. The above figure shows designation of address $A_3$.

## 320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

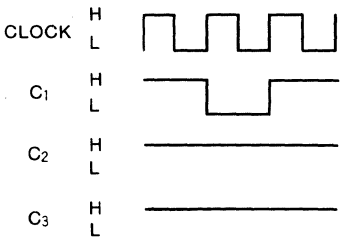
**Erase Mode** $\overline{CS}$ : L



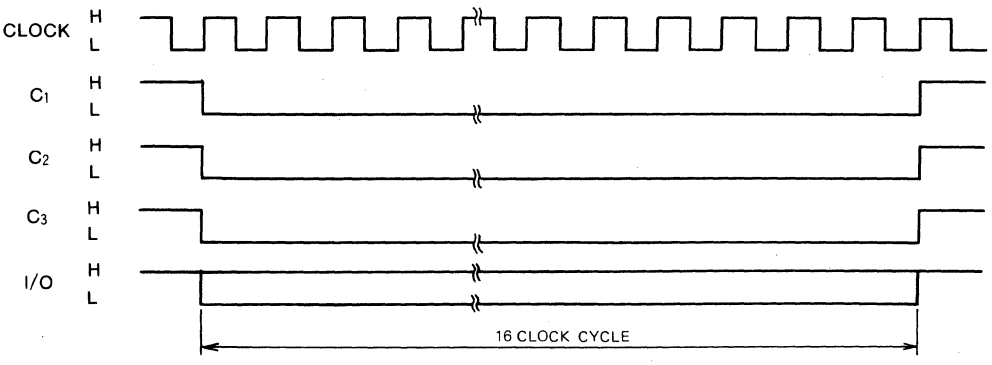

**Write Mode** $\overline{CS}$ : L




**Read Mode (1 clock)** $\overline{CS}$ : L

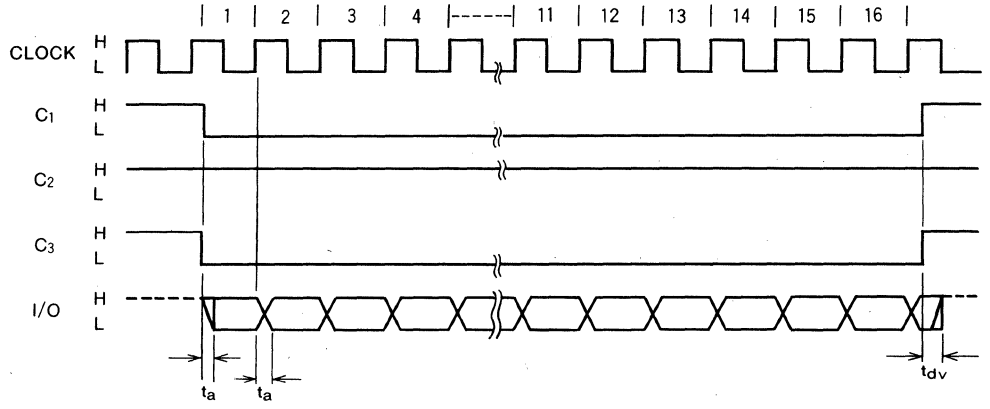



**Accept Data (16 clock)** $\overline{CS}$ : L

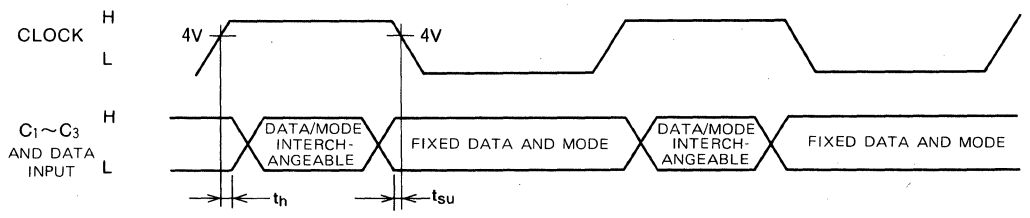


## Shift Data Output Mode (16 clock)

$\overline{CS}$ : L

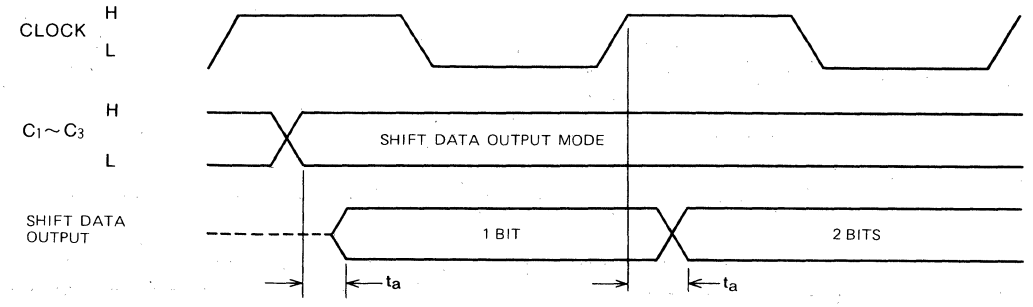



## Timing of clock, $C_1$, $C_2$, $C_3$, and data input



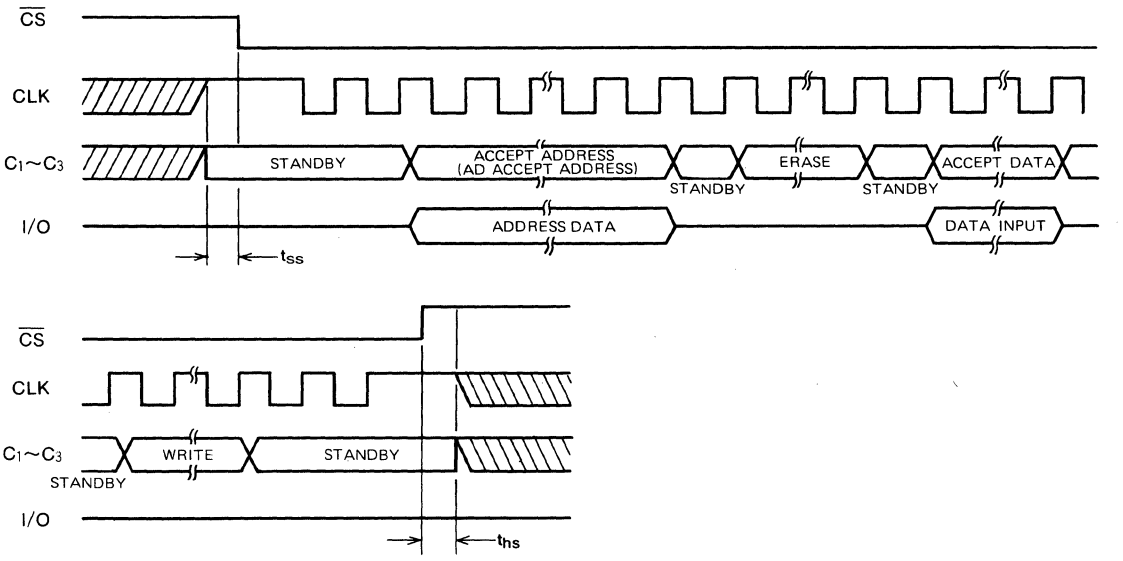

Note 4: $C_1 \sim C_3$ and accept data (AD accept data) are interchnageable while the clock is set high.

## Timing of clock, $C_1$, $C_2$, $C_3$, and data input



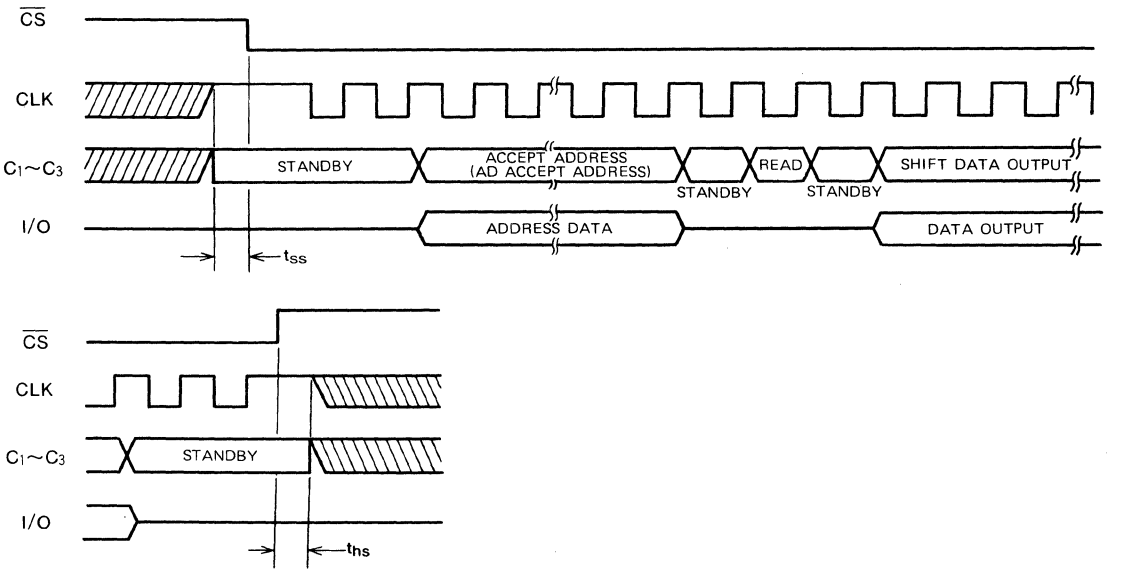
## Operation flowchart

### Rewriting flowchart



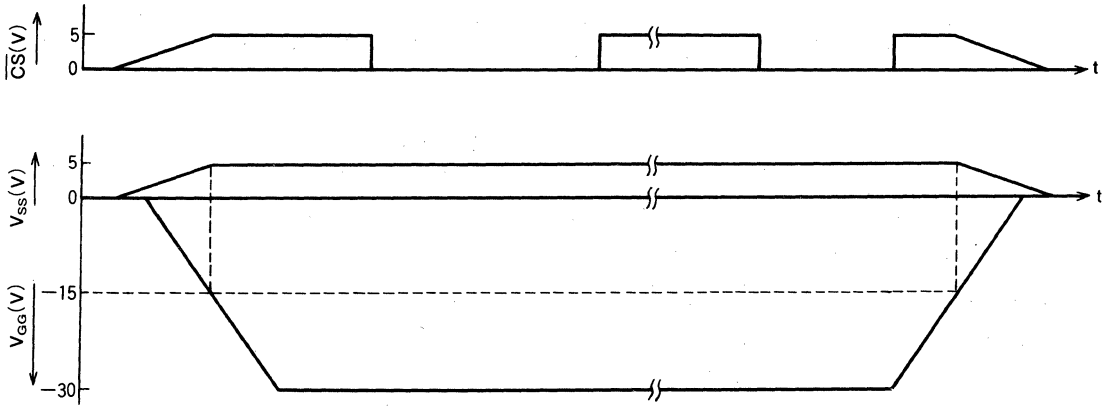

Note 5: One or more clock are required for standby between modes.
6: Set $\overline{CS}$ to the low level after the lapse of $t_{ss}$ and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
7: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of $t_{hs}$.

## Read Flowchart



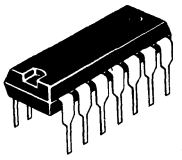
## Power-on/off Conditions

With power-on, $V_{GG}$ is applied after $V_{SS}$ has been applied. With power-off, $V_{SS}$ is cut after $V_{GG}$ has been cut. For power-on and off, hold $\overline{CS}$ in $V_{SS}$ or floating state. The recommended timing chart for power-on and off is as follows.



# M5G1400P

## 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM



### DESCRIPTION

The M5G1400P is a serial input/output 1400-bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

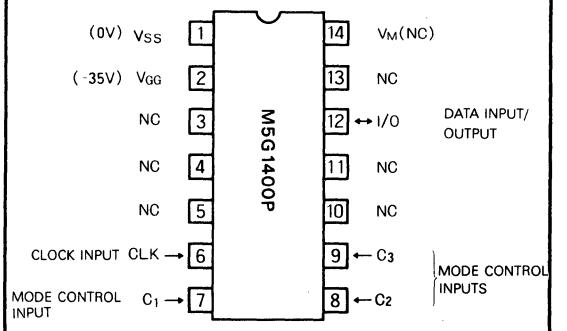
### FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage: ..... 10 years (min)
- Write/erase time: ..... 20ms/word
- Single 35V power supply
- Number of erase-write cycles: ..... $10^5$ times (min)
- Number of read access unrefreshed:.... $10^6$ times (min)
- Interchangeable with GI's ER1400 in pin configuration and electrical characteristics

### APPLICATION

- Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

### PIN CONFIGURATION (TOP VIEW)



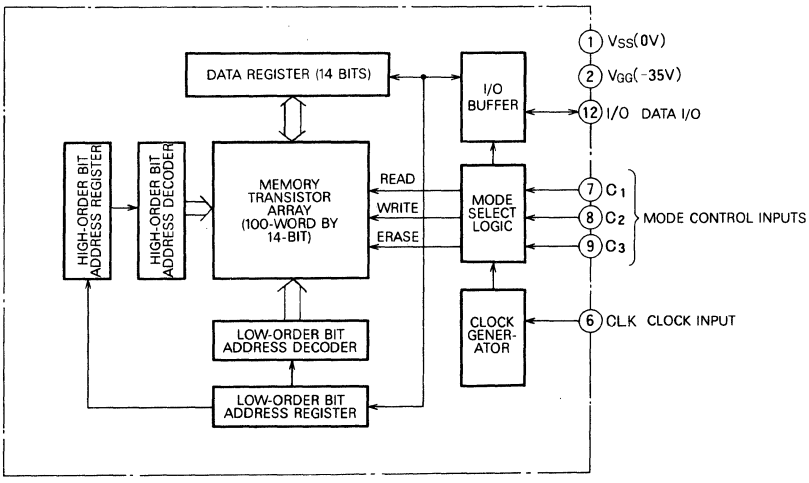

Outline 14P4

NC: NO CONNECTION

### FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to $C_1$, $C_2$, and $C_3$. Data is stored by internal negative writing pulses that selectively tunnel charges into the $SiO_2$—$Si_3N_4$ interface of the gate insulators of the MNOS memory transistors.

### BLOCK DIAGRAM



# 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## PIN DESCRIPTION

| Pin | Name | Functions |
|---|---|---|
| I/O | I/O | In the accept address and accept data modes, used for input.<br>In the shift data output mode, used for output.<br>In the standby, read, erase and write modes, this pin is in a floating state. |
| $V_M$ | Test | Used for testing purposes only. It should be left unconnected during normal operation. |
| $V_{SS}$ | Chip substrate voltage | Normally connected to ground. |
| $V_{GG}$ | Power supply voltage | Normally connected to −35V. |
| CLK | Clock input | 14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode. |
| $C_1 \sim C_3$ | Mode control input | Used to select the operation mode. |

## OPERATION MODES

| $C_1$ | $C_2$ | $C_3$ | Functions |
|---|---|---|---|
| H | H | H | Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state. |
| H | H | L | Not used. |
| H | L | H | Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level. |
| H | L | L | Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits. |
| L | H | H | Read mode: The addressed word is read from the memory into the data register. |
| L | H | L | Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse. |
| L | L | H | Write mode: The data contained in the data register is written into the location designated by the address registers. |
| L | L | L | Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged. |

# 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{GG}$ | Supply voltage | With respect to $V_{SS}$ | 0.3～−40 | V |
| $V_I$ | Input voltage | | 0.3～−20 | V |
| $V_O$ | Output voltage | | 0.3～−20 | V |
| Tstg | Storage temperature range | | −65～150 | ℃ |
| Topr | Operating free-air temperature range | | −10～70 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta=−10～70℃, unless otherwise noted.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{GG}$ | Supply voltage | −32.2 | −35 | −37.8 | V |
| $V_{SS}$ | Supply voltage (GND) | | 0 | | V |
| $V_{IH}$ | High-level input voltage | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}$−15 | | $V_{SS}$−8 | V |

Note 1:
The order of $V_{SS}$ $V_{GG}$ with on or off.
With on, $V_{GG}$ is turned on after $V_{SS}$ is done.
With off, $V_{SS}$ is turned off after $V_{GG}$ is done.

## ELECTRICAL CHARACTERISTICS (Ta=−10～70℃, $V_{GG}$=−35V±8%, unless otherwise noted.)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | | $V_{SS}$−1 | | $V_{SS}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | | $V_{SS}$−15 | | $V_{SS}$−8 | V |
| $I_{IL}$ | Low-level input current | $V_I$=−15V | | | ±10 | μA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | $V_O$=−15V | | | ±10 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$=−200μA | $V_{SS}$−1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$=10μA | | | $V_{SS}$−12 | V |
| $I_{GG}$ | Supply current from $V_{GG}$ | $I_O$=0μA | | 5.5 | 8.8 | mA |

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

## TIMING REQUIREMENTS (Ta=−10～70℃, $V_{GG}$=−35V±8%, unless otherwise noted.)

| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| f(φ) | Clock frequency | fφ | | 11.2 | 14 | 16.8 | kHz |
| D(φ) | Clock duty cycle | Dφ | | 30 | 50 | 55 | % |
| tw(W) | Write time | tw | | 16 | 20 | 24 | ms |
| tw(E) | Erase time | te | | 16 | 20 | 24 | ms |
| tr, tf | Risetime, falltime | tr, tf | | | | 1 | μs |
| tsu(c−φ) | Control setup time before the fall of the clock pulse | tCS | | 0 | | | ns |
| th(φ−c) | Control hold time after the rise of the clock pulse | tCH | | 0 | | | ns |

## SWITCHING CHARACTERISTICS (Ta=−10～70℃, $V_{GG}$=−35V±8%, unless otherwise noted.)

| Symbol | Parameter | Alternative symbols | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| ta(c) | Read access time | tPW | $C_L$= $V_{OH}$=$V_{SS}$−2V, $V_{OL}$=$V_{SS}$−8V | | | 20 | μs |
| ts | Unpowered nonvolatile data retention time | TS | $N_{EW}$=$10^4$, tw(W)=20ms, tw(E)=20ms | 10 | | | Year |
| | | TS | $N_{EW}$=$10^5$, tw(W)=20ms, tw(E)=20ms | 1 | | | Year |
| $N_{EW}$ | Number of erase/write cycles | NW | | $10^5$ | | | Times |
| $N_{RA}$ | Number of read access unrefreshed | $N_{RA}$ | | $10^6$ | $10^9$ | | Times |
| tdv | Data valid time | tPW | | | | 20 | μs |

# APPLICATIONS

8

## APPLICATION OF 64K-BIT DYNAMIC RAM

### Technology

Since the introduction of the 1K RAM in 1970, the development of dynamic RAM devices has progressed at a rate which has seen capacities multiplied by four in approximately two years, the latest stage of development being the 64K RAM.

Today's modern RAM devices take the user into consideration, and 64K dynamic RAMs which operate off a single 5V power supply are common.

We will describe here the new technology which made possible the development of a highly integrated, high-performance 64K RAM which operates from a single 5V supply.

### 1. Cell Structure and Process Technology

The M5K4164AP 64K RAM makes use of the same two-level n-channel polysilicon gate process and one-transistor cell structure used in the triple power supply 16K RAM (M5K4116P/S) which has been used in large quantities.

To achieve a high-density RAM, the masks are manufactured using electron beam technology.

In addition, the geometries on several critical levels of the M5K4164AP are 2.5 ~ 3.0$\mu$m, necessitating the use of positive photo-resist (for resolution and delineation control) as well as dry-plasma processing at these critical levels.

Fig. 1.1 shows the cross-section of the cell structure with Table 1.1 summarizing a comparison of the basic parameters of the device with the 16K RAM.

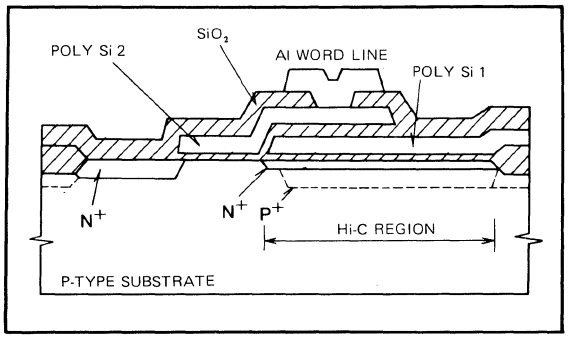



**Fig. 1.1 Hi-C structure memory cell cross-section**

**Table 1.1 Main parameters**

| Parameter | 16K RAM | 64K RAM |
|---|---|---|
| Memory cell area | 350 $\mu m^2$ | 143 $\mu m^2$ |
| Chip area | 16.3mm$^2$ | 23.9 $\mu m^2$ |
| Available channel length | 4 $\mu$m | 2 $\mu$m |
| Gate oxide film | 850 Å | 400 Å |
| Diffusion layer depth | 1.0 $\mu$m | 0.4 $\mu$m |
| Diffusion layer width | 4.0 $\mu$m | 2.5 $\mu$m |
| Aluminum width | 4.0 $\mu$m | 3.0 $\mu$m |

### 2. Substrate Bias Circuit

In order to facilitate the operation from a single 5V supply, the M5K4164AP makes use of an on-chip substrate bias circuit. This bias circuit consists of a ring oscillator, driver circuit, charge pump circuit, and decoupling capacitors. The circuit supplies a bias to the substrate of approximately –3.5V for $V_{CC}$ = 5V (Refer to Fig. 1.2)

The substrate bias circuit has the following functions.

1) It prevents destruction of storage data and disturbance of bipolar transistor operation caused by input undershoot which causes an injection of electrons from the input terminals to the substrate.
2) A reduction in the capacitance of the pn junction formed by the substrate and internal circuit nodes enables an increase in circuit operation speed.
3) The transistor threshold voltage ($V_{TH}$) modulation due to a bias substrate is reduced, resulting in increased circuit operating speed and stability.

As shown in Fig. 1.3, the substrate bias for high values of $V_{CC}$ is lower than for the standby mode due to the effect of increased impact ionization current. Adequate margin, however, is maintained against a value of $V_{IL}$ min of –2V.

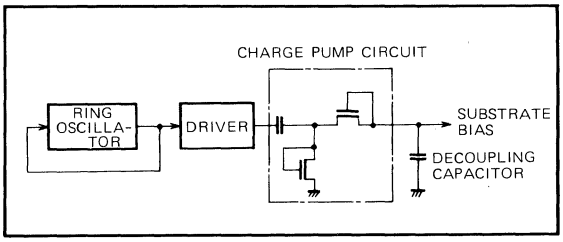



**Fig. 1.2 Substrate bias circuit**

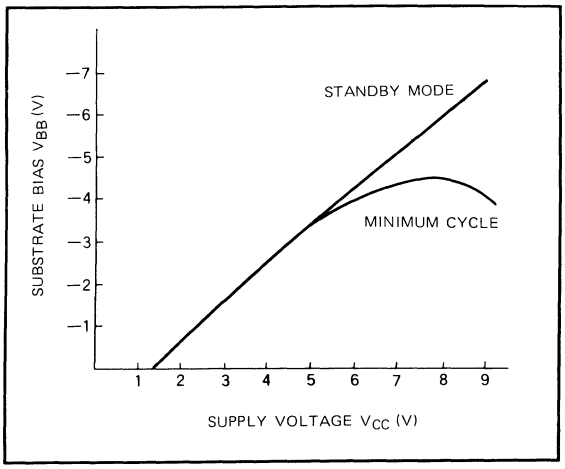



**Fig. 1.3 Substrate bias vs supply voltage**

### 3. Reduced Power Consumption and Noise

For operation from a 5V supply, it is necessary to reduce the transistor threshold voltage, $V_{TH}$. This, however, invites error operation due to noise. For this reason, circuits required to operate from low voltages only make use of transistors with a low $V_{TH}$, while those requiring noise immunity are implemented with transistors having a high value of $V_{TH}$. This scheme insures stable operation.

To lower the peak circuit current, a significant problem in memory system design, and provide for high-speed operation, the ratioless driver circuit shown in Fig. 1.4 was used.

With this circuit, the current flowing in transistors $Q_1$ and $Q_2$ for changes in the output waveform is practically zero. Fig. 1.5 shows the peak current waveforms. The figure shows that the peak currents are kept less than 100mA irrespective of transition on $\overline{RAS}$ and $\overline{CAS}$.

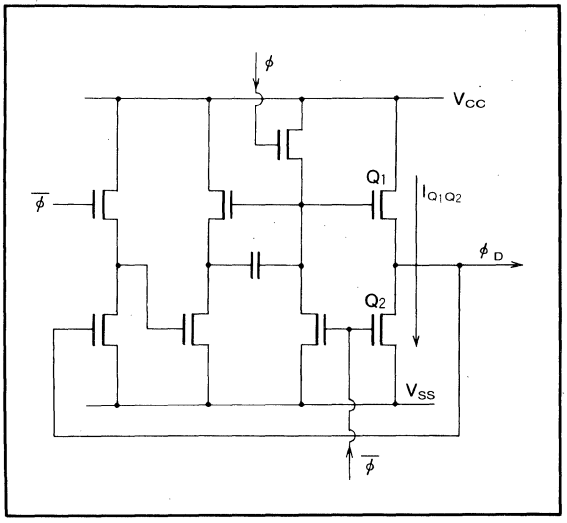



Fig. 1.4 Driver circuit

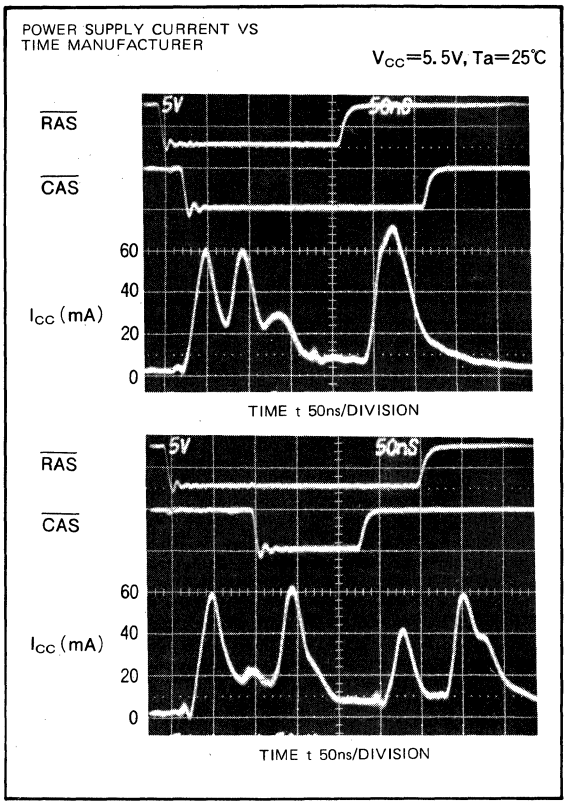



Fig. 1.5 Peak current waveforms

**4. Soft Error Reduction**

Reduction pattern sizes and lower supply voltages for 64K RAM devices which result in smaller storage charges also result in a higher susceptibility to alpha particles causing soft errors.

These soft errors are caused by alpha particles from minute amounts (ppm order) of uranium and thorium which are present in the IC package and decay. These particles cause the formation of electron-hole pairs in the substrate which collect on the surface and can destroy data.

All floating nodes of dynamic circuits are susceptible to such radiation-induced errors and for RAM operation, errors can occur when such phenomena occur in the memory cells and bit lines (including the sense amplifier).

To prevent such soft errors, three approaches are possible.

1) Increase the stored charge in the memory cells.
2) Increase the sense amplifier sensitivity and the bit line signal level.
3) Prevent alpha particles from reaching the chip circuits. As described below, the M5K4164AP makes use of these techniques to reduce the effects of alpha radiation.

**(1) Bootstrapped Word Line Voltage**

Designs of 64K dynamic RAM devices which must operate on 5V supplies must strive to write data into memory with the voltage $V_{CC}$ as well as increase the charge stored in the memory cells in order to reduce the effects of soft errors. This in effect means raising the word line voltage to above the value of $V_{CC} + V_{TH}$ for write and read operations.

Previously, this increase in voltage was accomplished by means of the coupling capacitance between the word line and the delay circuit. However, the increased capacitance resulted in a slow risetime of the word line voltage to $V_{CC}$, as well as increased power consumption. To eliminate these problems a circuit design such as that shown in Fig. 1.6 is used. The transistor $Q_2$ is kept off until the word line voltage reaches $V_{CC}$. This has the word line charge capacity. $C_2$ is then charged by means of transistor $Q_3$ after which $Q_2$ is turned on to connect the word line and $C_2$. The use of this circuit enables increase of the word line voltage without sacrificing operating speed and power consumption, thereby cutting soft error rates by 90%.

**(2) High-Capacity (Hi-C) Memory Cell**

The increase of memory cell stored charge requires an increase in the memory cell capacitance Cs. Limited chip area, however, places restrictions on the size of the memory cell itself. For this reason the Hi-C structure shown in Fig. 1.1 was used. This cell structure makes use of the normal silicon oxide layer and the P+ and n+ junction capacitance. The process for Hi-C memory cell structure requires two additional ion implantation steps and involves the risk of deterioration of the refresh time, an important characteristic of a dynamic RAM device. By selecting the ion implantation level properly, the junction capacitance can be increased without deterioration in the refresh time characteristic. For Hi-C structured cells, a portion of the minority carriers formed in the P+ layer are recombined, resulting in an effective reduction in soft errors. Such ion implantation has achieved a 30% increase in the memory cell capacitance and a reduction in soft error rate to 1/12 of the error rate of a normally structured cell, as shown in Fig. 1.7.

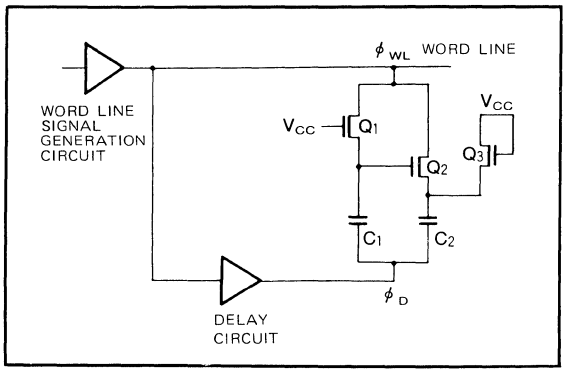



**Fig. 1.6 Bootstrapped word line voltage generation circuit**

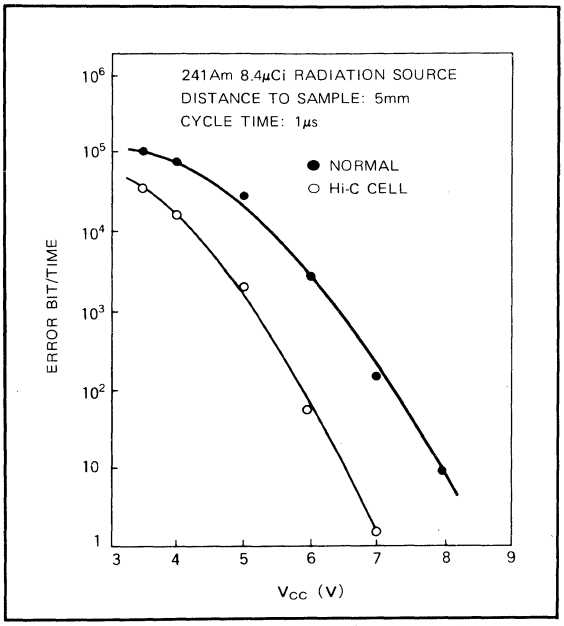



**Fig. 1.7 Soft error rate dependency on supply voltage**

### (3) Sense Amplifier Circuit

Increasing the sensitivity of the sense amplifier circuit is another effective method of reducing soft errors. Fig. 1.8 shows part of the sense amplifier circuit used by Mitsubishi Electric. High sensitivity with respect to the control signals $\phi 1$, $\phi 2$, and $\phi 3$ plays an important role in this amplifier's operation. After the data read from the memory cell is passed to the sense amplifier, the $\phi 3$ signal is controlled to separate the bit line and cut off the noise that is present on the bit line when sensing begins. Smooth sensing begins with the signal $\phi 1$ applied so that the minute potential difference is amplified. Next, $\phi 2$ is applied and amplified at high speed. By careful adjustment of the timing of the three control signals $\phi 1$, $\phi 2$, and $\phi 3$, detection of the potential differences as low as 30mV can be achieved without sacrificing speed in this sense amplifier circuit.

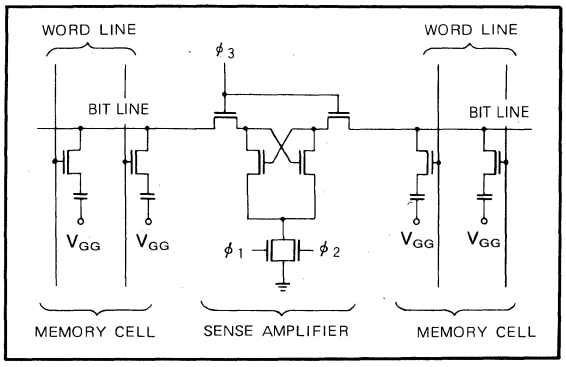



**Fig. 1.8 Sense amplifier circuit**

### (4) 128 Refresh Method

When the sense and amplifier sensitivity (offset) and other factors are considered, it is clear that it is important to maximize the read voltage applied from the memory cell to the bit line. The electrical charge, Q, read from the memory cell determines the voltage change $\Delta V$ by the following relationship

$$\Delta V \approx Q/C_B \text{ (for } C_B \gg Cs)$$

where $C_B$ is the bit line and Cs is the memory cell capacitance.

From this relationship it is seen that to make $\Delta V$ large $C_B$ must be made small. To satisfy this condition the 128 refresh method is used to implement a single bit line with 64 memory cells, a technique which reduces the length of the bit line. Fig. 1.9 shows the chip layout. The memory cells are broken into 64x256 bit units which are narrow, long blocks. The column decoders are located in three blocks totalling 256 decoders at the end of the bit line.

Using this arrangement, the bit line capacitance can be minimized.

### (5) Mold regin

In addition to circuit and device structure improvements aimed at reducing soft errors, the design goal of $10^{-6}$/(device hours) requires further improvements.

When this is done, however, alpha particles emitted from the mold regin material itself cause errors, making material selection critical. The mold resin chosen exhibits an alpha radiation level of $0.05\alpha/cm^2$ (hour), below the measurement sensitivity of an ion chamber. This is low enough that the resulting alpha particle generation level is 1/10 or less that of old material itself.

System evaluations of the M5K4164AP treated in such a manner indicate that the design goal of $10^{-7}$/(device hours) for soft error has been achieved.

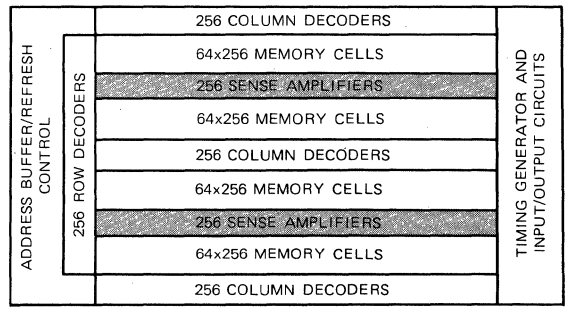



**Fig. 1.9 M5K4164AP Chip arrangement**

## Functional Description

The M5K4164AP is a 64K-bit dynamic RAM which operates off a single 5V supply and has a refresh function built in at pin 1. It can be used in a wide range of applications from large mainframes to microcomputers.

This section presents a functional description of the M5K4164AP and examines how it can be used in design of a memory system.

### 1. Block Diagram

Fig. 1.10 shows the block diagram of the M5K4164AP. To preserve the refresh cycle used for 16k dynamic RAM devices, two 32k blocks (of 128 rows (refresh address) x 256 columns each) were arranged one on top of the other.

In the center of each block is located 256 sense amplifiers making a total of 512 amplifiers in all.

On one end of each of these two array blocks is located one row decoder.

To prevent crosstalk between the column address lines and bit lines, the column decoders are located at the ends of the bit lines opposite to the sense amplifiers. A total of three rows of column decoders are used.

The central column decoder is used commonly by the two blocks.

### 2. Memory Cell

As shown in Fig. 1.11, the memory cell consists of one transistor and one capacitor. Data is stored as a one or zero depending upon the amount of electrical charge stored in the capacitor through the transistor Q.

Because leakage current would result in the stored charge of the cell being reduced with time, the data must be refreshed within 2ms.

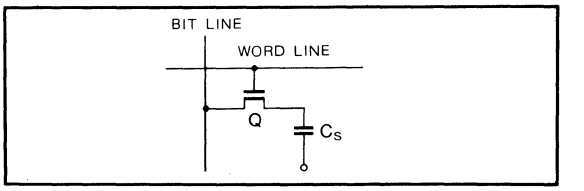



**Fig. 1.11 Memory cell**

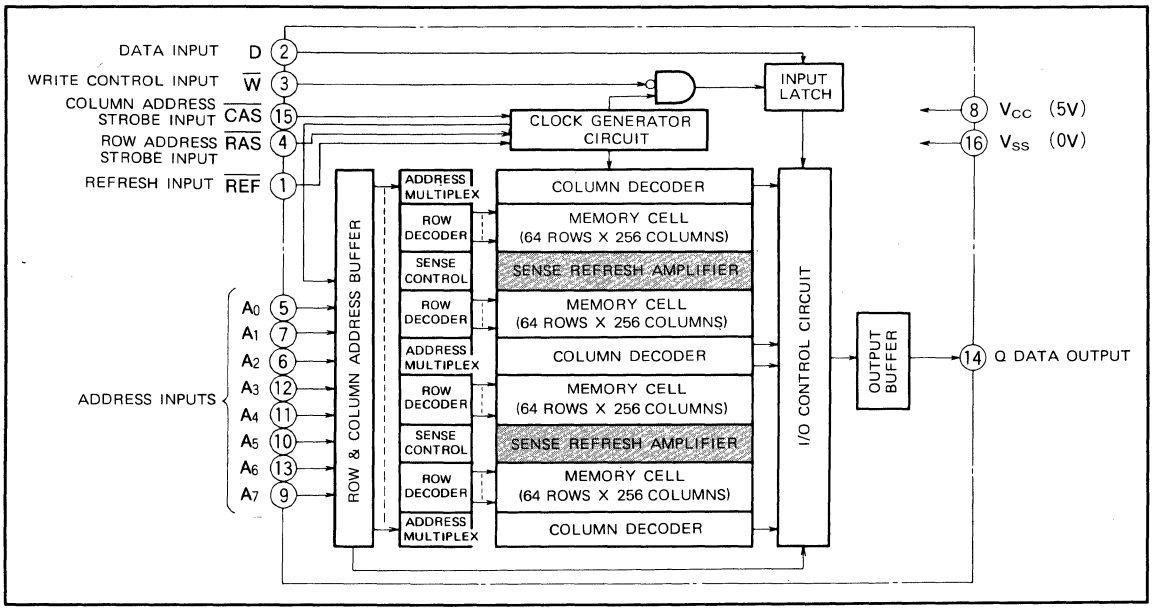



**Fig. 1.10 Block diagram**

### 3. Clock Timing

The M5K4164AP has four clock inputs: $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{REF}$. Among these, $\overline{RAS}$ and $\overline{CAS}$ are the basic clock inputs for the memory operation. The $\overline{RAS}$ input is generally used for memory cell data amplification and refresh operation while the $\overline{CAS}$ is used for data read and write operations only.

To enable the design of a memory system with a large timing margin, it is necessary to know the timing relationships between these two clock inputs and the internal clock signals generated by these clocks.

Fig. 1.13 shows the timing parameters of the $\overline{RAS}$ and $\overline{CAS}$ clocks while Fig. 1.14 and 1.15 show their relationships to the internal clock timing.

For read or write operations, $\overline{RAS}$ goes low after which the falling edge of $\overline{CAS}$ initiates the cycle.

After the read or write is completed, both signals return to a high level and the precharging operation is performed for the next cycle.

For this timing relationship to work, the external $\overline{RAS}$ clock must follow the changes of the internally generated $\overline{RAS}$ clock. To simplify the setting of the timing relationships of the external $\overline{RAS}$ and $\overline{CAS}$ clocks, the internal $\overline{CAS}$ clock $\phi_{CAS}$, $\phi_{\overline{CAS}}$ is controlled by the external $\overline{RAS}$ clock. Fig. 12 shows the internal $\overline{RAS}$ and $\overline{CAS}$ clock generating circuit.

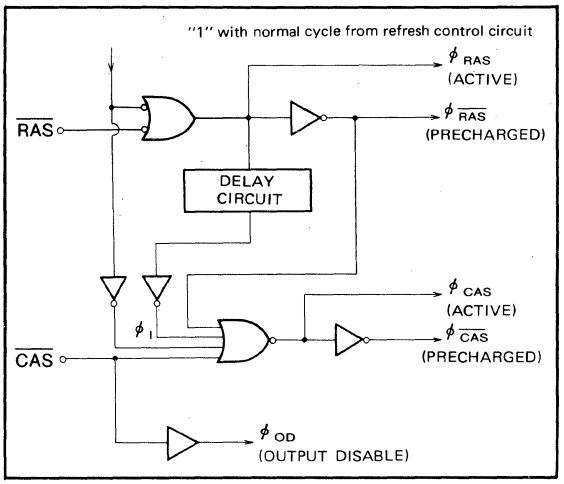



**Fig. 1.12 Internal $\overline{RAS}$ and $\overline{CAS}$ clock generating circuit**

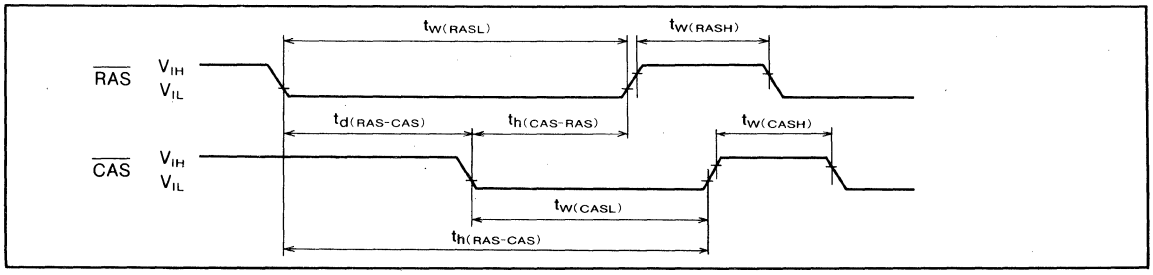



**Fig. 1.13 $\overline{RAS}$, $\overline{CAS}$ timing**

**(1) $\overline{CAS}$ Falling Edge Timing (Fig. 1.14)**

The memory system design must be such that the falling edge timing of $\overline{CAS}$ does not critically affect the access time. In other words as shown by the solid line in Fig. 1.14, the internal $\phi_{CAS}$ phase is prevented by the delay phase $\phi_1$ from approaching $t_{d(RAS-CAS)}$ max. This type of operation is referred to as gated $\overline{CAS}$.

This gated $\overline{CAS}$ feature permits $\overline{CAS}$ to be activated at anytime between the minimum and maximum value of $t_{d(RAS-CAS)}$ without affecting access time.

For gated $\overline{CAS}$ operation, if the generation of internal clock phase $\phi_{CAS}$ is delayed, the effective pulse width of $\phi_{CAS}$ is reduced. For this reason, the rising edge of $\overline{CAS}$ is specified by $t_{h(RAS-CAS)}$ which is reference to $\overline{RAS}$ rather than $t_{w(CASL)}$. This applies to the column address, $\overline{W}$ and D inputs hold time as well.

As shown by the dotted line in Fig. 1.14, if $\overline{CAS}$ falls to a low level after $t_{d(RAS-CAS)}$ max, the $\phi_{CAS}$ phase is generated upon the falling edge of $\overline{CAS}$.

The minimum and maximum values of $t_{d(RAS-CAS)}$, the delay time $\overline{RAS}$ to $\overline{CAS}$, are specified for the M5K4164AP. Operation within the $t_{d(RAS-CAS)}$ max limit ensures that the access time for the device is guaranteed. This value may be exceeded without causing data storage or reading errors but the access time will be increased.

**(2) $\overline{CAS}$ Rising Edge Timing (Fig. 1.15)**

As shown in Fig. 1.15, the internally generated $\overline{CAS}$ circuit precharge signal $\phi_{\overline{CAS}}$ is generated with a timing that is related to the relationship between $\overline{RAS}$ and the $\overline{CAS}$ rising edge.

For a $\overline{CAS}$ rising edge occurring before the $\overline{RAS}$ rising edge, $\phi_{\overline{CAS}}$ is generated with the $\overline{CAS}$ rising edge as a reference point (as shown in Fig. 1.15 as a solid line). If however the $\overline{CAS}$ rising edge occurs after that of $\overline{RAS}$, $\phi_{\overline{CAS}}$ is generated with the $\overline{RAS}$ rising edge as a reference (shown as dotted line in Fig. 1.15).

However, the data in the output buffer is cleared upon the occurrence of the rising edge of $\overline{CAS}$ regardless of the state of $\overline{RAS}$. The required pulse width for clear is $t_{w(CASH)}$.

In this manner, the output data can be maintained for a long period while the internal precharge width is made large.

As described above, if the $\overline{CAS}$ rising edge occurs after that of $\overline{RAS}$, the internal $\overline{CAS}$ pulse width becomes not $t_{w(CASL)}$ but $t_{h(CAS-RAS)}$. Consideration should be given to this point in circuit design.

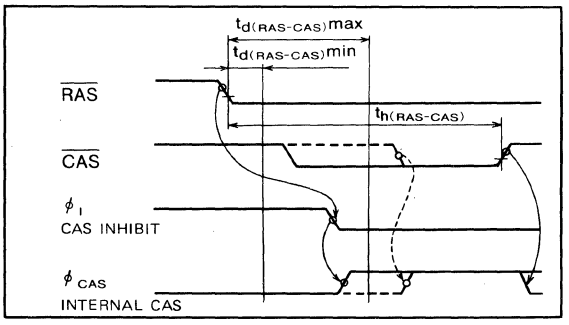



**Fig. 1.14 The timing relationship of $\overline{RAS}$ and $\overline{CAS}$ falling edges to internal clock signals (gated $\overline{CAS}$ operation)**

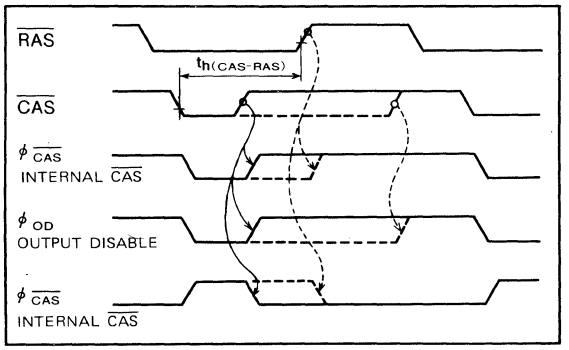



**Fig. 1.15 Relationship of $\overline{RAS}$ and $\overline{CAS}$ rising edges to internal clock timing**

**4. Address Timing**

Addressing of any one of the 65,536 memory cells of the M5K4164AP requires the internal latching of two 8-bit multiplexed address ($A_0$ to $A_7$) by means of clocks $\overline{RAS}$ and $\overline{CAS}$. First, the row address is latched by the falling edge of $\overline{RAS}$. This selects 512 memory cells from the total of 65,536 memory cells. Fig. 1.16 shows the timing relationships for this operation.

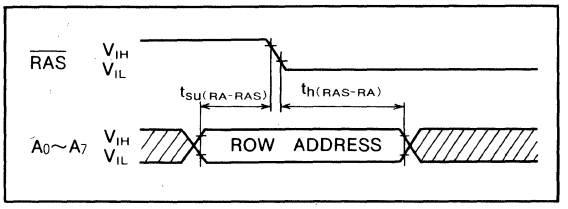



**Fig. 1.16 Row address latching timing relationships**

The setup time $t_{su(RA-RAS)}$ and holdtime $t_{h(RAS-RA)}$ are specified with the $\overline{RAS}$ falling edge as a reference point.

The falling edge of $\overline{CAS}$ latches the column address. This selects one cell from among the 512 cells selected by $\overline{RAS}$. Fig. 1.17 shows the timing relationships for this operation. The setup time $t_{su(CA-CAS)}$ and the hold time $t_{h(CAS-CA)}$ are specified with the falling edge of $\overline{CAS}$ as a reference, while the hold time $t_{h(RAS-CA)}$ is specified with the falling edge of $\overline{RAS}$ as a reference point.

For these operations two timing parameters must be considered. One is the column address setup time $t_{su(CA-CAS)}$ which is specified as minus 5ns, minimum. This means that the column address may be input anytime up to 5ns after the $\overline{CAS}$ falling edge.

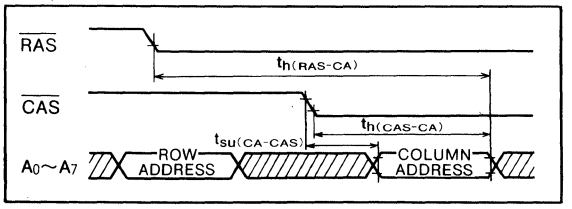



**Fig. 1.17 Column address latch timing**

The other parameter is the column address hold time $t_{h(RAS-CA)}$. For the previously described gated $\overline{CAS}$ operation, if $\overline{RAS}$ to $\overline{CAS}$ delay time $t_{d(RAS-CAS)}$ is set between the specified minimum and maximum values, the time from $\overline{RAS}$, $t_{h(RAS-CA)}$ and time from $\overline{CAS}$, $t_{h(CAS-CA)}$ must both be satisfied as the column address hold time. This applies to both the $\overline{W}$ and D signals to be described later.

The time required to switch from row address to column address is referred to as the multiplex time ($t_{MUX}$). This timing is shown in Fig. 1.18.

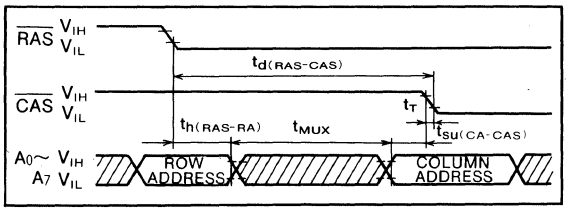



**Fig. 1.18 Address multiplex timing**

The multiplex time $t_{MUX}$ is given by the following expression:

$$t_{MUX} = t_{d(RAS-CAS)} - t_T - t_{h(RAS-RA)} - t_{su(CA-CAS)} \quad \cdots\cdots (1)$$

As long as the access time, $t_{a(RAS)}$ from $\overline{RAS}$ does not exceed the maximum value, the following expression determines the maximum value of $t_{MUX}$ is achieved by the following conditions.

$t_{d(RAS-CAS)}$ = maximum

$t_{a(RAS-RA)}$ = minimum

$t_{su(CA-CAS)}$ = minimum

Table 1.2 shows actual values of $t_{MUX}$ maximum for $t_T$ = 5ns.

**Table 1.2 Maximum multiplex time**

| Device \ Parameter | $t_{MUXmax}$ | $t_{d(RAS-CAS)}$ | $t_{h(RAS-RA)}$ | $t_{su(CA-CAS)}$ |
|---|---|---|---|---|
| M5K4164AP-12 | 40ns | 60ns | 15ns | 0ns |
| M5K4164AP-15 | 50ns | 75ns | 20ns | 0ns |

If the timing is set to satisfy the above described, operation is guaranteed for both read and write functions. To simplify the following description, the timing parameters for address inputs has been eliminated unless absolutely required.

### 5. Read Cycle

Fig. 1.19 shows the timing parameters for the read cycle.

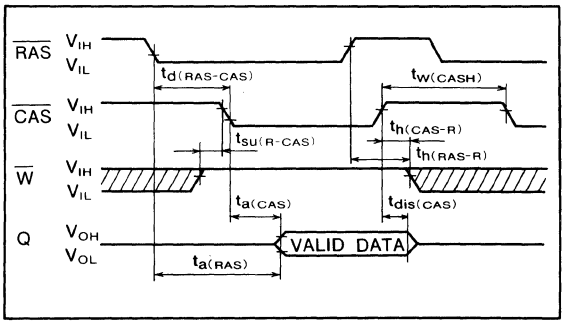



**Fig. 1.19 Read cycle timing**

In this read cycle, $\overline{RAS}$ and $\overline{CAS}$ are made active, and the W input is set to a high level. The setup time, $t_{su(R\text{-}CAS)}$ before $\overline{CAS}$, resulting in output of the data stored in the memory cell at pin Q. The time for the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to the output is defined as the $\overline{RAS}$ access time $t_{a(RAS)}$ and the $\overline{CAS}$ access time $t_{a(CAS)}$ respectively.

The $\overline{RAS}$ access time depends on the $\overline{RAS}$ to $\overline{CAS}$ delay time, $t_{a(RAS)}$ and $t_{d(RAS\text{-}CAS)}$.

As can be seen from this figure, by setting $t_{d(RAS\text{-}CAS)}$ before $t_d$ for gated $\overline{CAS}$ operation, $t_{a(RAS)}$ does not depend on the value of $t_{d(RAS\text{-}CAS)}$ and is constant.

For $t_{d(RAS\text{-}CAS)}$ set after $t_d$, $t_{a(RAS)}$ depends upon the value of $t_{d(RAS\text{-}CAS)}$. For this condition, $t_{a(RAS)}$ is given by the following expression.

$$t_{a(RAS)} = t_{d(RAS\text{-}CAS)} + t_{a(CAS)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

Equation (2) expresses only the electrical characteristics of the RAM device, the guaranteed access time being given by the following expression.

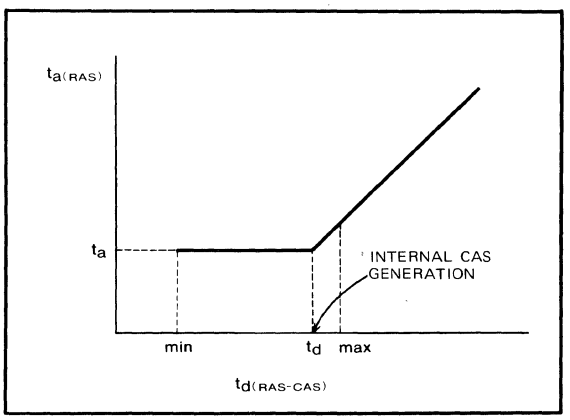



**Fig. 1.20 Dependency of $t_{a(RAS)}$ on $t_{d(RAS\text{-}CAS)}$**

$$t_{a(RAS)} \leqq t_{d(RAS\text{-}CAS)}\ \text{max} + t_{a(CAS)}\ \text{max} \quad \cdots\cdots\cdots \quad (3)$$

In equation (3), for a value of $t_{d(RAS\text{-}CAS)}$ greater than the maximum value ($t_{a(RAS)}$) increases by the increased amount only.

During a read operation when the output is active, inputs $\overline{RAS}$ and $\overline{W}$ have no effect on the output. Only raising $\overline{CAS}$ to a high level will put the output in the high-impedance state.

The time from the rising edge of $\overline{CAS}$ until the output goes into the high-impedance state is defined as the output disable time ($t_{dis(CAS)}$). This time, $t_{dis(CAS)}$ is the period for the RAM output to go to the open state and should be distinguished from that time the output states to go to $V_{OH}$ and $V_{OL}$.

If the pulse width $t_{w(CASH)}$ is satisfied for $\overline{CAS}$, operation is guaranteed for any arbitrary timed rising edge after the next cycle, simplifying the design with respect to $\overline{CAS}$ timing.

The read cycle parameters $t_{h(CAS\text{-}R)}$ and $t_{h(RAS\text{-}R)}$ determine the read cycle ending time. Operation is guaranteed if either of these parameters are satisfied.

### 6. Write Cycle

Three types of write cycles are specified; early write, read write and read modify write.

#### (1) Early Write Cycle

Fig. 1.21 illustrates the timing relationship for this cycle.

This cycle is selected for applications such as I/O common applications in which the output is held at high impedance during the writing of data into the memory cell.

This cycle is executed by causing the $\overline{W}$ input to fall before $\overline{CAS}$.

The $\overline{W}$ and D inputs are latched by $\overline{CAS}$, then the data write is executed, the $\overline{W}$ and D input timing parameters $t_{su(W\text{-}CAS)}$, $t_{su(D\text{-}CAS)}$, $t_{h(CAS\text{-}W)}$, and $t_{h(CAS\text{-}D)}$ are determined by the falling edge of $\overline{CAS}$ as a reference point.

Two points here are worthy of consideration. First is the write pulse setup time $t_{su(W\text{-}CAS)}$. This parameter is specified as minus 10ns, minimum.

The significance of this is that $\overline{W}$ inputs may occur anytime within before 10ns of the falling edge $\overline{CAS}$.

However, should the $\overline{W}$ input falling edge occur after $\overline{CAS}$, the rising edge of $\overline{W}$ is determined not by $t_{h(CAS\text{-}W)}$, but by $t_{w(W)}$.

The other point for consideration is setting $t_{d(RAS\text{-}CAS)}$ between the minimum and maximum values. For this condition, gated $\overline{CAS}$ operation requires that as hold time the time from $\overline{RAS}$ for the $\overline{W}$ and D input, $t_{h(RAS\text{-}W)}$ and $t_{s(RAS\text{-}D)}$ and time from $\overline{CAS}$, $t_{h(CAS\text{-}W)}$ and $t_{h(CAS\text{-}D)}$ both must be satisfied.

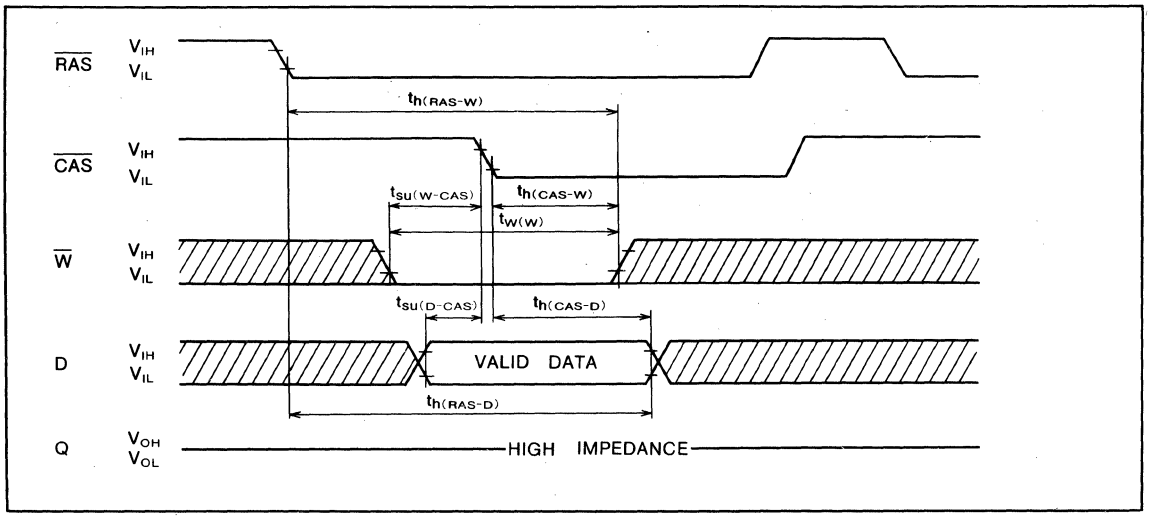



**Fig. 1.21 Early write cycle timing**

**(2) Read Write Cycle Timing**

This cycle is used in applications where data is to be read out of memory while new data is being written into a memory cell.

The timing parameters for this read write cycle are shown in Fig. 1.22.

For this type of cycle, the $\overline{W}$ input signal falls after $t_{d(RAS-W)}$ min and $t_{d(CAS-W)}$ min.

The data read timing is the same as the read cycle. Since the read data is latched into an output buffer, $\overline{W}$ input can be made active without disabling the output.

Since the D input is latched by the falling edge of the $\overline{W}$ input, the $\overline{W}$ input falling edge is determined as a reference point for the D input setup time $t_{su(D-W)}$ and hoid time $t_{h(W-D)}$.

Data is written into the memory cell between the time the $\overline{W}$ input signal falls and $\overline{RAS}$ and $\overline{CAS}$ rise. This time is specified as $t_{h(W-RAS)}$ and $t_{h(W-CAS)}$ and both of these must be satisfied.

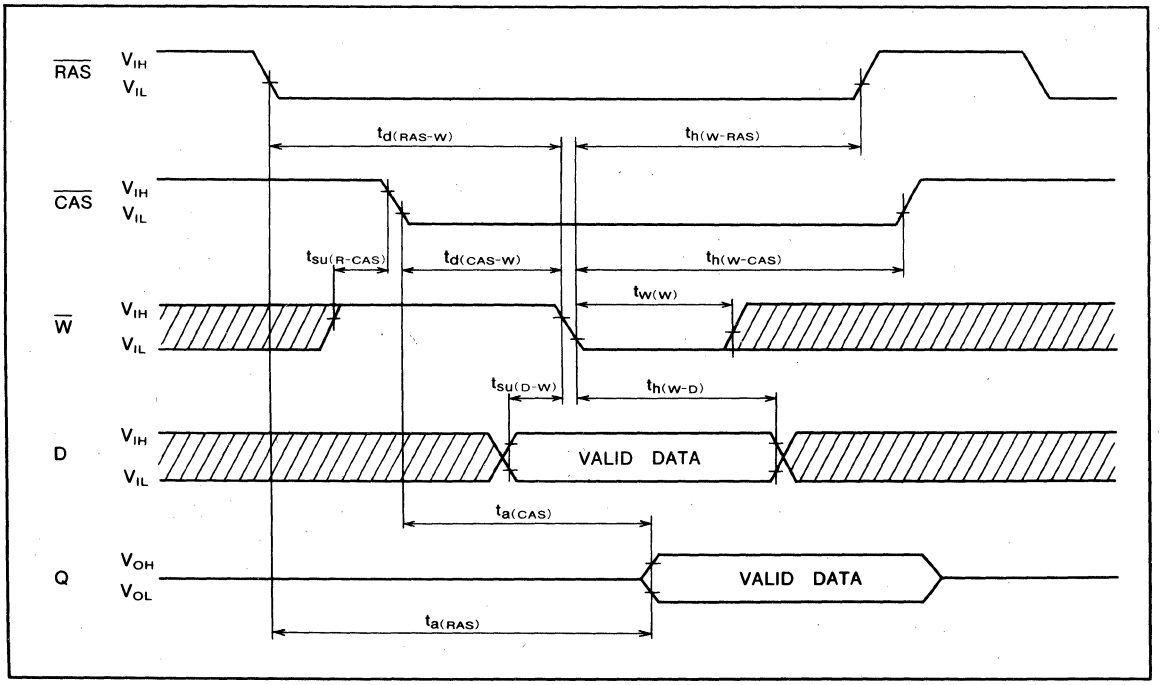



**Fig. 1.22 Read write cycle timing**

**(3) Read Modify Write Cycle**

This cycle is used in applications such as ECC (see section on ECC) on which memory cell data is read and verified for correctness, the correct data being written into the cell if an error is detected. Fig. 1.23 shows the timing parameters of the read modify write cycle.

The RAM operation is the same as the previously described read write cycle except that after the data is read, data is written so the cycle is slightly extended.

The minimum time for the read modify write cycle is given by the following expression.

$$t_{CRMW}\ \text{min} = t_{a(RAS)}\ \text{max} + t_{MOD} + t_{h(W-RAS)}\ \text{min} + t_{w(RASH)}\ \text{min} + 3t_T \quad \cdots\cdots\cdots\cdots (4)$$

In equation (4), $t_{MOD}$ is the time required for incorrect data to be rewritten correctly, and is a function of system design. In the device specifications $t_{CRMW}$ min is specified for $t_{MOD} = 0$.

As previously described, the M5K4164AP write cycle mode is determined by the $\overline{W}$ input falling edge timing. This falling edge timing does not limit the operation of the RAM but merely controls the output state. If the $\overline{W}$ input falling edge does not satisfy the conditions described for the three write modes, data will be writen but the output state will be indeterminate.

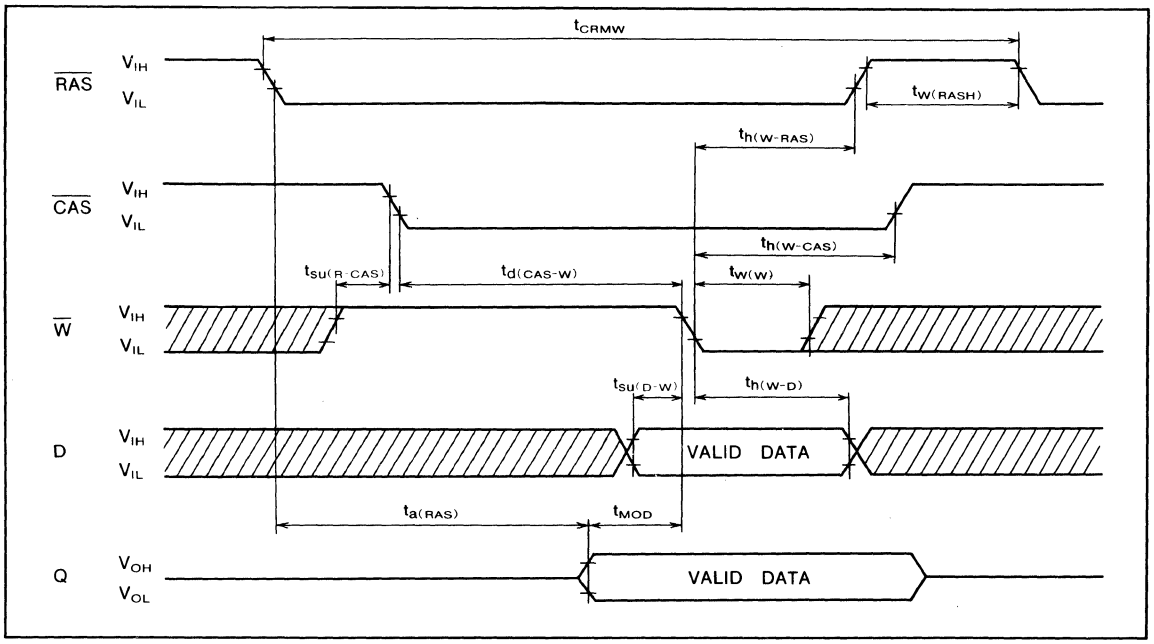



**Fig. 1.23 Read modify write cycle timing**

### 7. Page Mode Timing

Page mode operation is successive memory operations at multiple column locations within the same row address.

As with normal operation, page mode operation can be carried out in the read, early write, read write or read modify write modes. The timing parameters particular to the page mode of operation are shown in Fig. 1.24. The other parameters are the same as for normal cycles.

To perform page mode read and write operations, the $\overline{RAS}$ low-level pulse width, $t_{w(RASL)}$ must be increased, the maximum value being 10$\mu$s. The high-level $\overline{CAS}$ pulse width, $t_{w(CASH)}$ is specified separately for the normal mode cycle and page mode. For the page mode, the pulse width must be increased. For details refer to the specifications.

For page mode operation the hold time $t_{h(CAS-RAS)}$ must be satisfied for even the last cycle, as shown in Fig. 1.24. This applies to $\overline{W}$ as well.

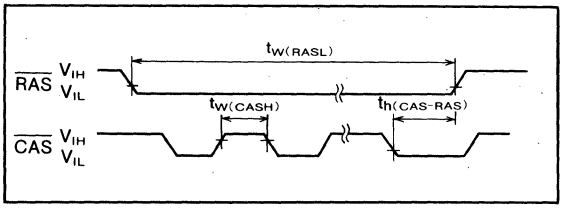



**Fig. 1.24 Page mode cycle timing**

### 8. Refresh

Referring to the block diagram of Fig. 1.10, for each $\overline{RAS}$ cycle, one word line is selected for each of the upper and lower blocks, enabling access to 512 memory cells. Next, the 512 sense amplifiers operate to amplify and refresh the cell data. Address signal $A_7$ (ROW) has no connection with this refresh operation since it is used as a block select address for data read and write operations.

### 9. $\overline{RAS}$ Only Refresh Timing

$\overline{RAS}$ only refresh is performed by setting $\overline{CAS}$ to high which sets the output to high-impedance while refresh is performed.

Both distributed and burst mode refresh can be performed.

Fig. 1.25 shows the timing parameters for $\overline{RAS}$ only refresh operation.

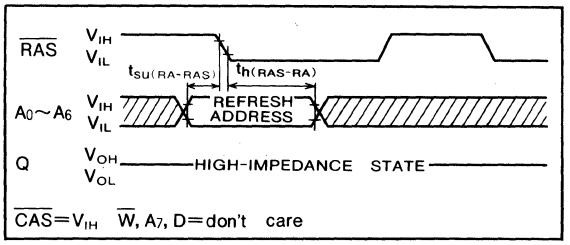



**Fig. 1.25 $\overline{RAS}$-only refresh timing**

### 10. Hidden Refresh Timing

Hidden refresh is accomplished by setting $\overline{CAS}$ to low after a read cycle to hold the data in the valid state while refresh is performed.

Both distributed and burst mode refresh are possible. Fig. 1.26 shows the timing parameters for hidden refresh operations.

Data latched in the output buffer by the read cycle is refreshed during the hidden refresh cycles by $\overline{RAS}$. Therefore output data is held indefinitely as long as hidden refreshing is continued.

Timing design is simplified because the $\overline{W}$ signal may be changed in any state during hidden refreshing.

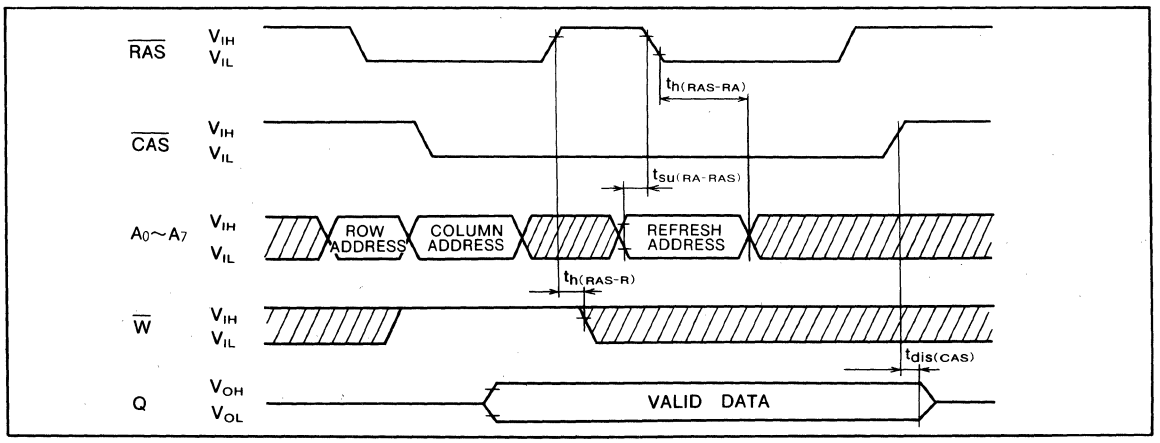



**Fig. 1.26 Hidden refresh timing**

**11. Refresh Operations Using Pin 1**

To simplify the refresh operation, a function absolutely essential to dynamic RAM operation, two special refresh functions easier to use than the conventional $\overline{RAS}$ clock refresh have been provided.

These functions are automatic refresh and self refresh.

These special functions are implemented by an on-chip refresh counter, address multiplexer, and timer, along with the associated control circuity. The following is an operational description of these circuits.

**(1) Refresh Control Circuit**

Fig. 1.27 shows a block diagram of the refresh circuit which makes use of Pin 1. The control circuit controls not only the refresh counter, address multiplexer and timer as shown in Fig. 1.27, but $\overline{RAS}$ and $\overline{CAS}$ circuits as well.

Pin 1 refreshing is controlled externally by the $\overline{REF}$ input and internally by the $\overline{RAS}$ signal which is generated by the refresh control circuit.

During pin 1 refresh operations, the $\overline{CAS}$ circuit with the exclusion of the output buffer is inhibited to prevent data writing and reading.

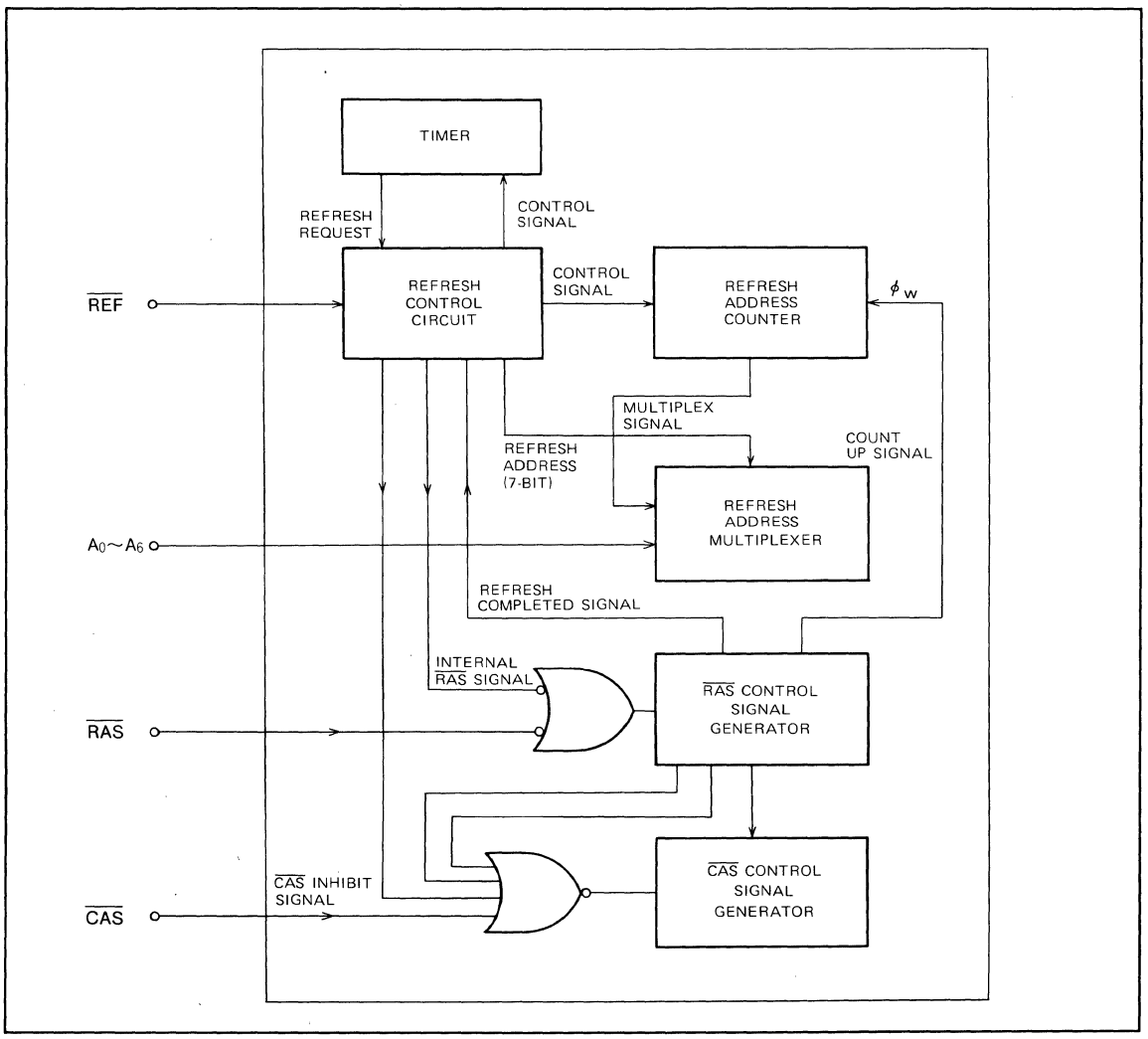



**Fig..1.27 Refresh circuit block diagram**

**(2) Refresh Counter circuit**

The M5K4164AP on-chip refresh counter consists of a 7-bit toggle-type counter, the individual counter output being used as the refresh address bit.

For automatic refresh operations, the refresh counter counts up synchronized to the internal clock signal $\phi_W$ which is synchronized in turn to the $\overline{REF}$ input, 128 $\overline{REF}$ pulses required to cycle to the original state. For self refresh operation, the refresh counter is free-running with a period of from 12 to 16$\mu$s, counting up in synchronous to the refresh request signal REF REQ (described afterwards). A complete cycle and return to the original state requiring that the $\overline{REF}$ input be held low for 16$\mu$s x 128 (approx.) = 2ms.

The above described counting operation is performed approximately in synchronous with the refresh operation completion. The output of the refresh counter, $Q_0$ to $Q_6$ (refresh address) is held until the next refresh cycle, forming the address for the next cycle.

The refresh counter outputs are initialized by approximately 8 dummy cycles of $\overline{RAS}$, $\overline{RAS}/\overline{CAS}$, or $\overline{REF}$. Therefore, no special initialization is required for this refresh counter.

However, the contents of the counter, that is the toggle counter flip-flop states, cannot be reset or preset externally during power up or dummy cycles.

For this reason, using both normal $\overline{RAS}$ and pin 1 refresh will cause the specified refresh time to be exceeded, and therefore should be avoided.

**(3) Address Multiplexer**

Fig. 1.28 shows the M5K4164AP on chip address multiplexer.

The address multiplexer consists of two MOS transistors at the address buffer inputs and the associated control signals (MUX, $\overline{MUX}$).

During a normal cycle, $\overline{MUX}$ is high and MUX is low, so that only the external address $A_0$ to $A_6$ is input.

For pin 1 refresh operations, $\overline{MUX}$ is low and MUX is high so that the refresh counter output signals $Q_0$ to $Q_6$ only are input to the address buffer.

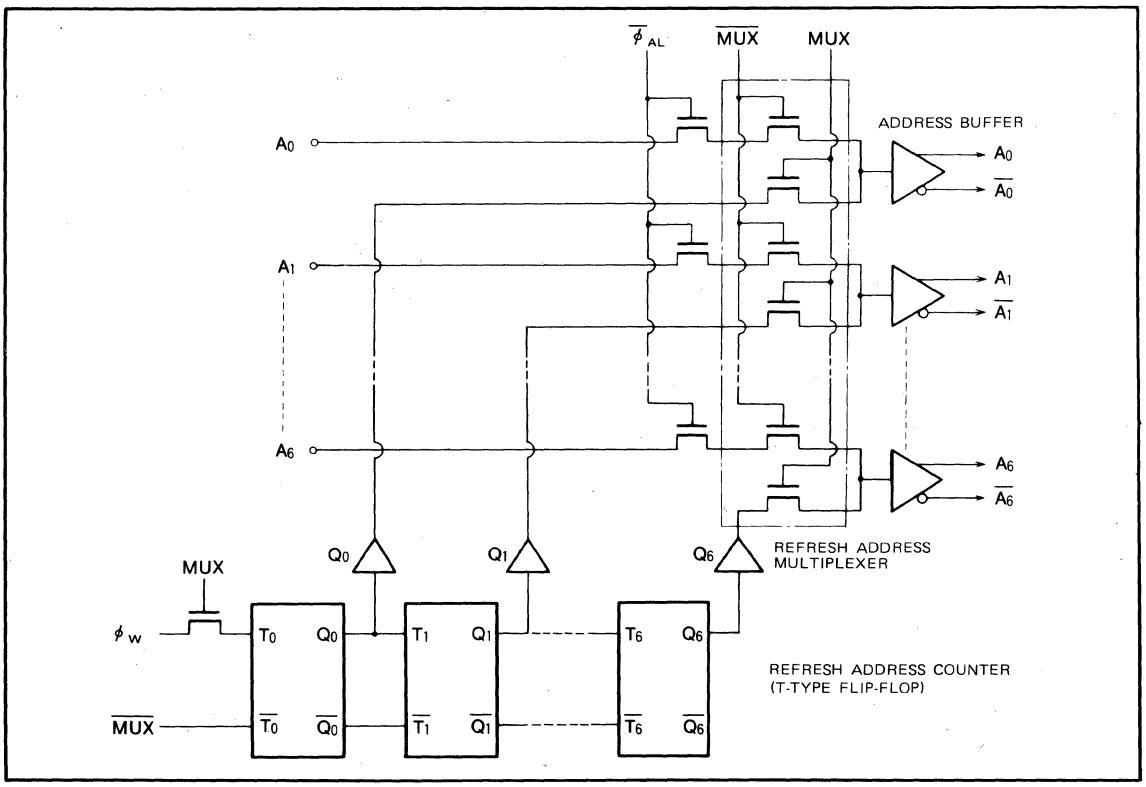



**Fig. 1.28 Refresh address counter and multiplexer circuits**

**(4) Timer Circuit**

Fig. 1.29 shows the timer circuit block diagram while Fig. 1.30 illustrates its timing.

In the circuit of Fig. 1.29, the oscillator provides the substrate bias as well. The other circuits are active when $\overline{REF}$ is low.

When $\overline{REF}$ goes low, transistor $Q_1$ turns on, $Q_2$ turns off and the charge stored in $C_2$ passes through the rectifying circuit $C_1$ and $Q_1$ to discharge upon the falling edge of the oscillator output signal. The charge for one cycle of the oscillator output is proportional to the ratio of the capacitance of $C_1$ and $C_2$.

The ratio of $C_1$ to $C_2$ is chosen such that the voltage across $C_2$ for an oscillator repetition period of 12 to 16$\mu$s is approximately equal to the threshold voltage of the next gate. When the $C_2$ voltage reaches $V_{TH}$, the refresh request signal REFREQ goes active, causing the RAM refresh operation similar to the automatic Refresh external signal $\overline{REF}$. When $C_2$ is charged by REFREQ, REFREQ goes low, causing a repetition of the above described timer operation.

As long as the $\overline{REF}$ signal is kept low, this operation will automatically continue refreshing all memory cells every 2ms.

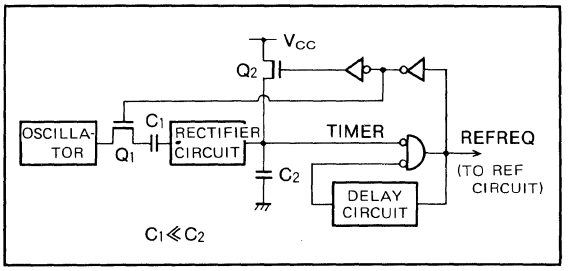



**Fig. 1.29 Timer circuit block diagram**

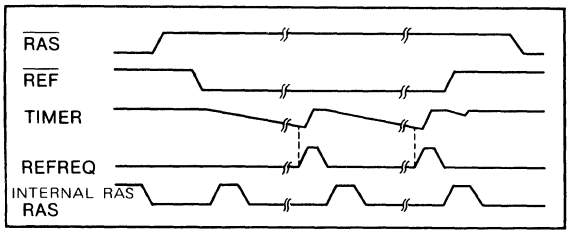



**Fig. 1.30 Timer circuit timing**

**12. Automatic Refresh Timing**

Automatic refresh is accomplished in the same manner as $\overline{RAS}$ only refresh but without providing the refresh address data.

Fig. 1.31 shows the timing of the automatic refresh operation.

Automatic refresh begins when $\overline{REF}$ is set to low $t_{d(RAS-REF)}$ after $\overline{RAS}$ goes high.

Shortly after the refresh cycle begins the internal RAS signal begins to operate to strobe the refresh counter output and perform the refresh.

The $\overline{REF}$ input is internally latched. When the refresh operation is complete an internal refresh complete signal causes the chip to be precharged. Therefore, it is not necessary to use the $\overline{REF}$ input to determine the precharge time greatly simplifying the timing design of $\overline{REF}$.

It is also possible to perform hidden refreshing by holding the $\overline{CAS}$ input low after a read cycle. The timing is very similar to the $\overline{RAS}$ hidden refresh operation timing. For details refer to the specifications.

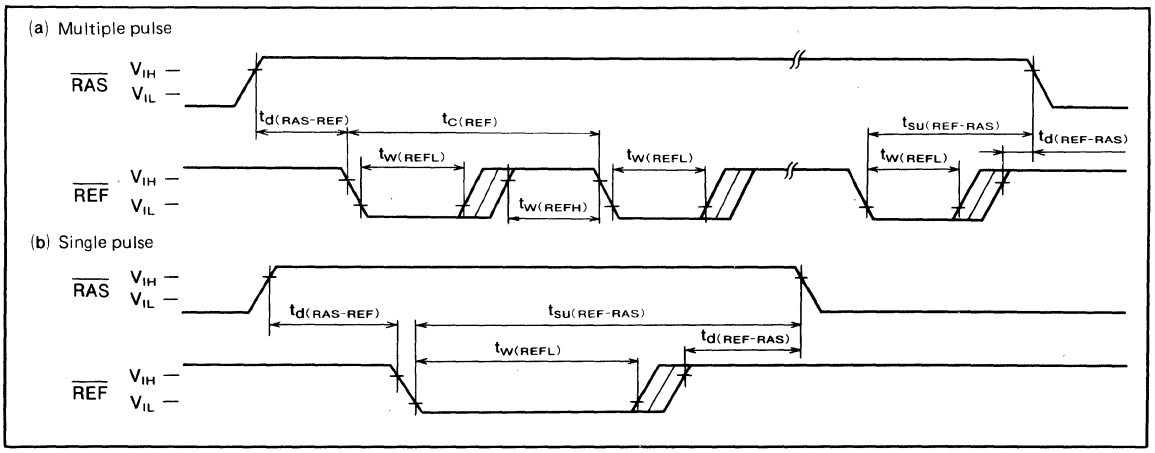



**Fig. 1.31 Automatic refresh timing**

### 13. Self Refresh Timing

Self refresh is generally used for battery backup of memory contents.

Fig. 1.32 shows the self refresh timing relationships from which it can be seen that they are quite similar to those of automatic refresh. Self refresh begins when $\overline{REF}$ is set to low $t_{d(RAS-REF)}$ after $\overline{RAS}$ is set to high.

Shortly after the beginning of the refresh cycle, the internal $\overline{RAS}$ signal begins to operate to strobe the refresh counter and perform the refresh operation.

As long as $\overline{RAS}$ is high and $\overline{REF}$ is low, the RAM will be automatically refreshed. This operation is repeated with a period of from 12 to 16$\mu$s. After 2ms, the refresh counter has gone through all of the row address, refreshing all of the memory cells. Self refresh ends when $\overline{REF}$ is set to high but setting $\overline{REF}$ to high may not terminate the internal operation of the circuit (refer to Fig. 1.30) so that one cycle time of $t_{d(REF-RAS)}$ is required between setting $\overline{REF}$ to high and $\overline{RAS}$ to low.

As with automatic refresh, hidden refreshing is possible. For details refer to the specifications.

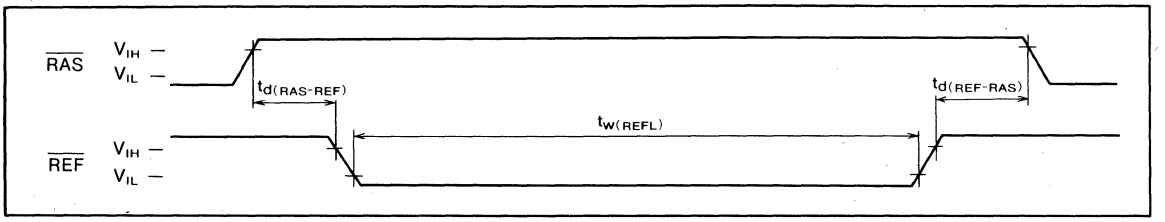



**Fig. 1.32 Self refresh timing**

### 14. Notes on the Use of Pin 1

(1) When pin 1 is not to be used to refresh the chip, it should be handled in the following manner.

Since pin 1 refresh is inhibited by setting the $\overline{REF}$ input to high, the input should be set between $V_{IH}$ min and $V_{IH}$ max. (The pin 1 input leakage current for $V_{IN}$ = 6.5V is guaranteed to be below 10$\mu$A.)

(2) When the above method is not possible, pin 1 should be left open. Since as shown in Fig. 1.33 as MOS transistor is used to connect a pull-up resistor between the input terminals and $V_{CC}$, the terminal will be held to a high level ($V_{CC}$) when left open.

However, when the input is set low in order to perform a refresh operation, a current flows from $V_{CC}$ to the input terminal. This resistance is made a very high value (approximately 3M$\Omega$) in order to guarantee the specified leakage current of 10$\mu$A maximum for $V_{IN}$ = 0V.

This high resistance results in pin 1 being susceptible to the effects of external noise so that if pin 1 is to be left open, such noise should be considered carefully.

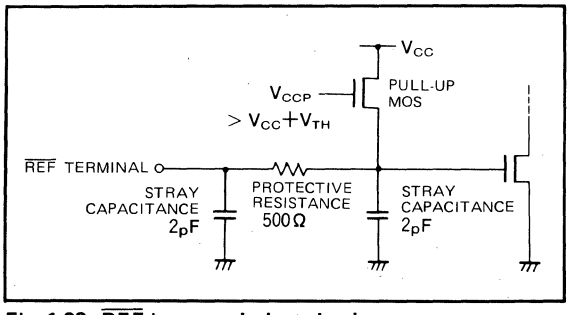



**Fig. 1.33 $\overline{REF}$ input equivalent circuit**

## M5K4164AP Bit Map

To facilitate the generation of worst-case pattern checking and the optimization of test sequences, it is necessary to know the internal topology of a memory device. This section will examine the internal topology of the M5K4164AP.

### 1. Memory Array

Fig. 1.34 shows the dual in-line package as viewed from above with pin 1 to the upper right. It illustrates the memory cell layout.

The row decoder is located to the left of the memory cells while the column decoder is located parallel to the cells.

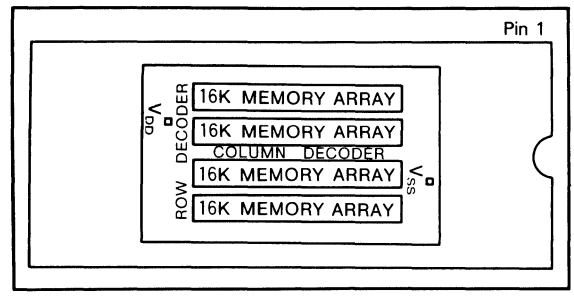



**Fig. 1.34 Memory array location**

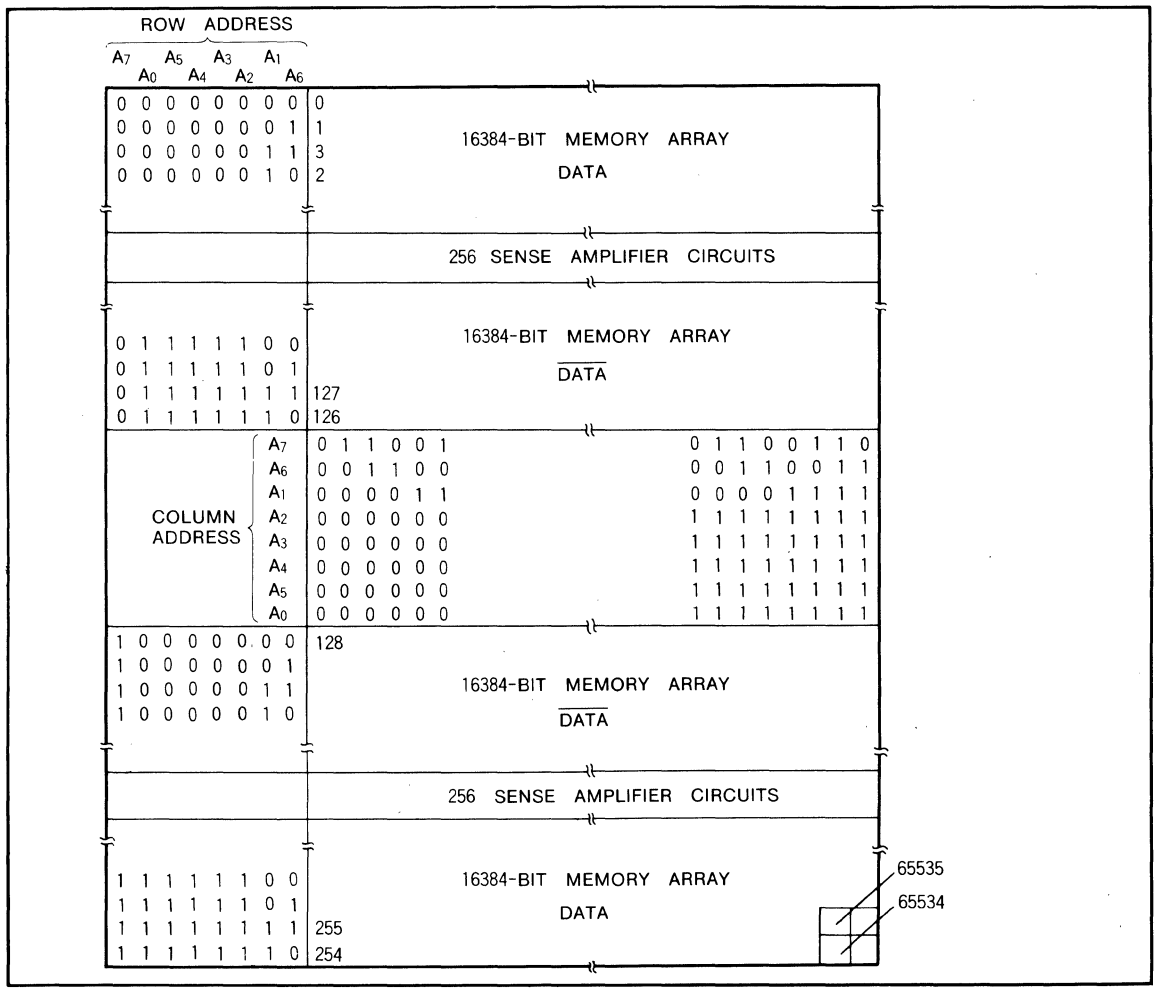



**Fig. 1.35 Address decoder location**

### 2. Address Decoder

Fig. 1.35 shows the address decoder. To optimize pattern layout, the decoder is arranged as shown in Fig. 1.35. For this reason, with $A_0$ (row) as the least significant bit and $A_7$ (column) as the most significant bit, sequential binary addresses will not address adjacent cells in order.

For the arrangement of Fig. 1.35, Table 1.3 shows the addresses that will be accessed for sequentially incremented binary addresses if $A_6$ (row) is the least significant bit and $A_0$ (column) is the most significant bit.

**Table 1.3 Address coding**

| | Column (MSB) | | | | | | | | Row (LSB) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cell No. | $A_0$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_6$ | $A_7$ | $A_7$ | $A_0$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_6$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 32767 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 65535 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 3. Bit Topology

For the purposes of simplified explanation, we have assumed thus far that the memory cells are located in an orderly fashion in a matrix. For actual devices, however, techniques required to increase the density on the chip dictate that an arrangement such as shown in Fig. 1.36 is used.

For this reason, this layout must be considered carefully when designing tests which detect interference between adjacent cells.

### 4. Data Polarity

Because the sense amplifiers are located in the center of the bit lines of the M5K4164AP, half of the data matrix is stored in inverted form. While this has absolutely no effect on actual operation, it must be considered if a test is to be devised which will test all cells in the charged state. This bit inversion pattern is given in Table 1.4.

**Table 1.4 Data polarity arrangement**

| $A_7$ (row) | $A_0$ (row) | Input data | Memory cell data | Output data |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| | | 0 | 0 | 0 |
| | 1 | 1 | 0 | 1 |
| | | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| | | 0 | 1 | 0 |
| | 1 | 1 | 1 | 1 |
| | | 0 | 0 | 0 |

Write operation  Read operation

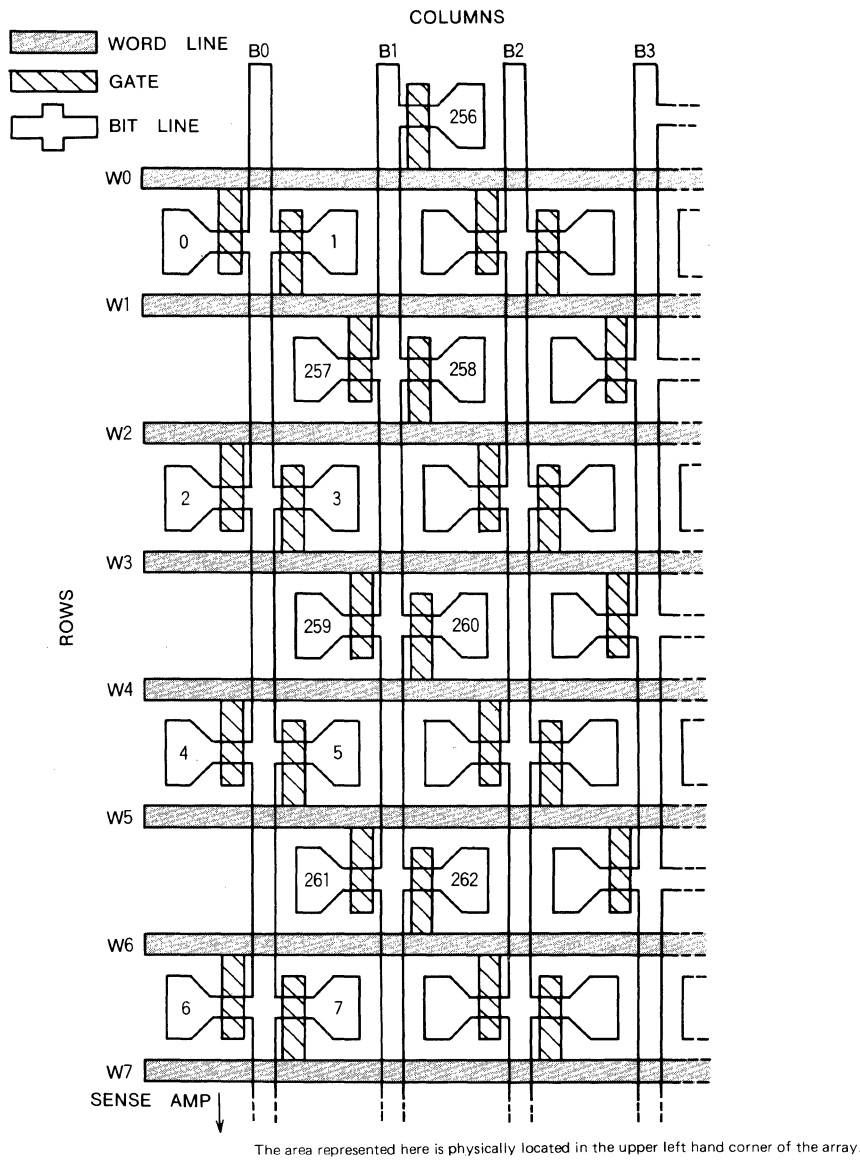



**Fig. 1.36 Simplified internal bit topology**

## Memory System Design Considerations

New memory systems designs are making use of dynamic RAM, static RAM, EPROM and other semiconductor memory devices. All of these devices have some general design considerations in common. This application note will examine some of the delicate timing considerations involved in the design of a dynamic RAM board.

### 1. Power Distribution

Fig. 1.37 shows the current waveform of an M5K4164AP dynamic RAM. Note that when $\overline{RAS}$ and $\overline{CAS}$ go low, the row or column address latch and buffer are charged, and that when $\overline{RAS}$ and $\overline{CAS}$ go high, the row or column address latch and buffer are precharged, resulting in a transient current waveform. The 60 to 80mA current pulse of approximate width 50ns and a risetime of 10 – 20ns represents the risetime which is observed at 50ms per division. With rise and fall times of this magnitude harmonic noise components above 10MHz are generated. It is therefore necessary when designing the board power distribution to suppress such noise and provide the device with a clean supply voltage. Decoupling capacitors should be used which are capable of charging a small loop.

Fig. 1.38 (a) shows the lumped constant equivalent circuit for a PC board. $L_S$ and $R_S$ represent the PC board inductance and resistance respectively. If we let the $L_X$ and $R_S$ of a 10mil wide 2-ounce copper pattern be 10nH/inch and 4mΩ/inch, then the generated spike voltage is given by the following expression.

$$L_S \cdot \frac{di}{dt} = 10nH \times 10 \times \frac{80mA}{10ns} = 800mV$$

$$R_S \cdot i = 4m\Omega \times 10 \times 80mA = 3.2mV$$

Since the effect of the series resistance $R_S$ compared to that of the series inductance is very small, it may be neglected. The series resistance of $L_S$ is frequency dependent, increasing with increasing frequencies.

To reduce the level of the spike voltage, as shown in Fig. 1.38 (b), a decoupling capacitor is used to decrease the series resistance. This is done by shortening the PC board current loop.

For a 0.1μF capacitor value used with a 250ns cycle RAM, the spike voltage is given by the following expression.

$$V = \frac{1}{C}\int i10dt = \frac{80mA}{0.1\mu F} \times 50ns = 40mV$$

This yields an acceptable value of spike voltage.

It is recommended that ceramic capacitors with good high frequency characteristics are used as the decoupling capacitors in memory arrays. The decoupling capacitor is connected between the memory $V_{CC}$ and the ground with as short a lead dressing as possible. In addition, as bulk decoupling a solid tantalum capacitor is required. This type of capacitor has a better transient response than other large value capacitors and can be used with one capacitor per 16-memory devices between $V_{CC}$ and the ground.

The power supply traces for a memory array should be made as wide as possible and it is recommended that they be arranged in a grid. Fig. 1.39 (a) shows an example of such an arrangement.

As another method, the use of multi-layer boards is possible, and is an effective method in simplifying power distribution.

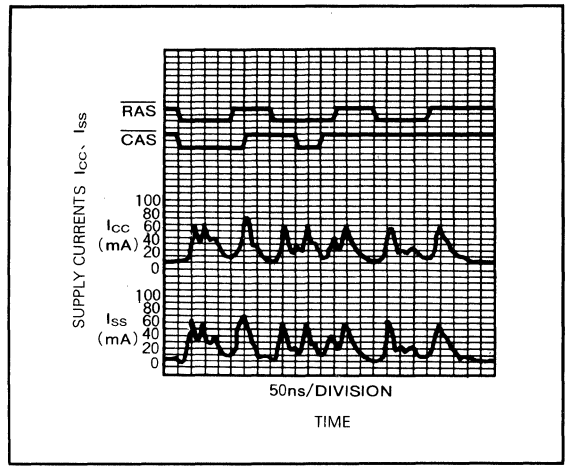



**Fig. 1.37 Supply current vs time $\overline{RAS}/\overline{CAS}$ cycle RAS-only cycle**

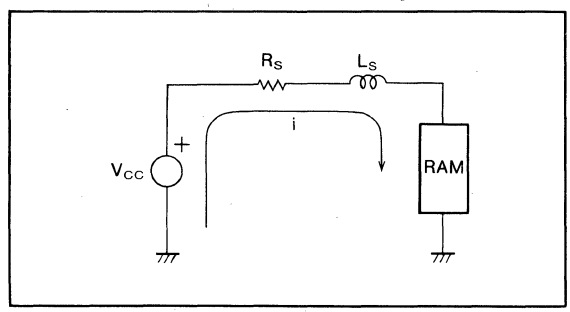



**Fig. 1.38 (a) PC board trace equivalent circuit**

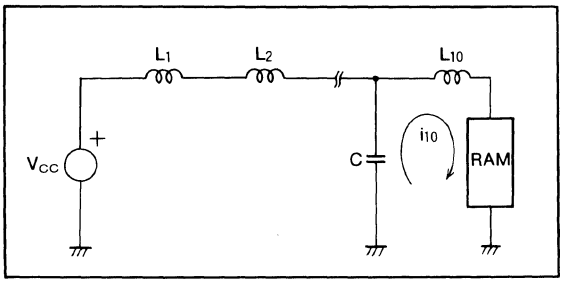



Fig. 1.38 (b) PC board trace equivalent circuit with decoupling capacitors

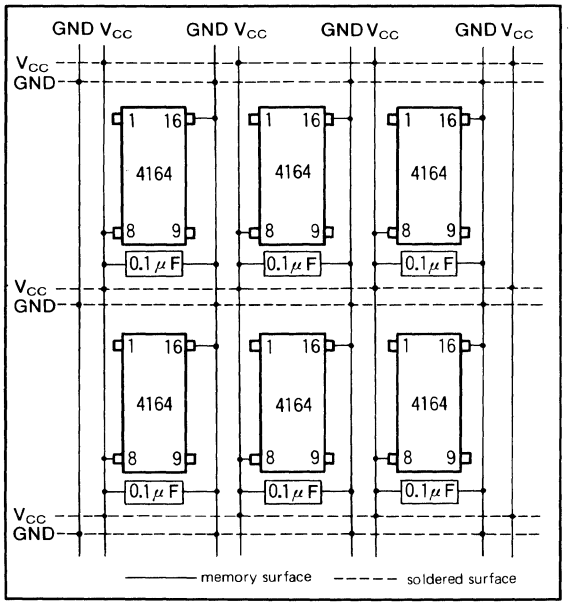



Fig. 1.39 (a) Gridded power distribution and decoupling capacitors

## 2. Signal Distribution

The next most important consideration in the design of a memory system is the design of memory signal (address, data, and control signals) distribution.

For the case of the M5K4164AP dynamic RAM, two types of chip enable signals exist; $\overline{RAS}$ and $\overline{CAS}$. If these are to be driven by TTL circuits, it is very important to keep the driving TTL device as close as possible to the RAM array. This minimizes the transmission line impedance mismatch between the RAM array loaded line and the TTL driver. Another technique is the use of a damping resistor located close to the driver. The value of this resistor is selected to provide a good waveform at the RAM input, the usual values being in the range 10 to 50Ω. This technique brings the output impedance of the driver close to the line impedance which minimizes waveform overshoot and undershoot.

To eliminate crosstalk from $\overline{RAS}$ and $\overline{CAS}$, the $\overline{RAS}$ and $\overline{CAS}$ signal lines should be kept at 90° to the traces for other signals. If this is impossible, they should be kept as far as possible from traces of other signals. In addition the address and data signal traces should be kept as short as possible. Fig. 1.39 (b) shows an example of a printed board pattern for a 128K-bite memory system.

## 3. Logical Considerations

Far memory systems with critical timing, it is necessary to consider the propagation delay to surrounding ICs. To minimize signal delay, gate selection and the use of the same IC package for related signals are effective in reducing the difference in delays between signals. To reduce the capacitive loading on drivers, it is necessary to limit the number of drivers per memory array. For $\overline{RAS}$ and $\overline{CAS}$, 8 memories/driver and for address 16 memories/driver are recommended.

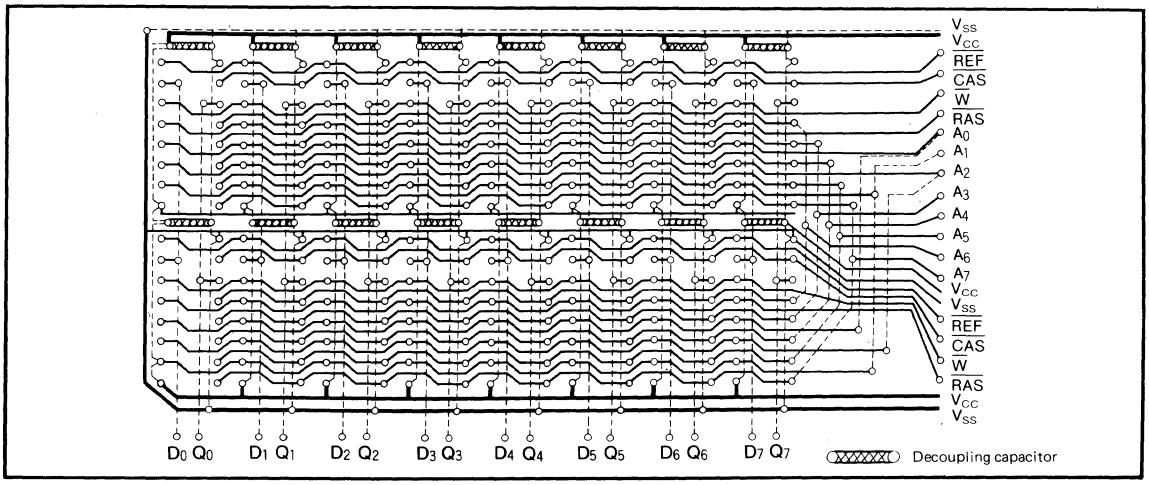


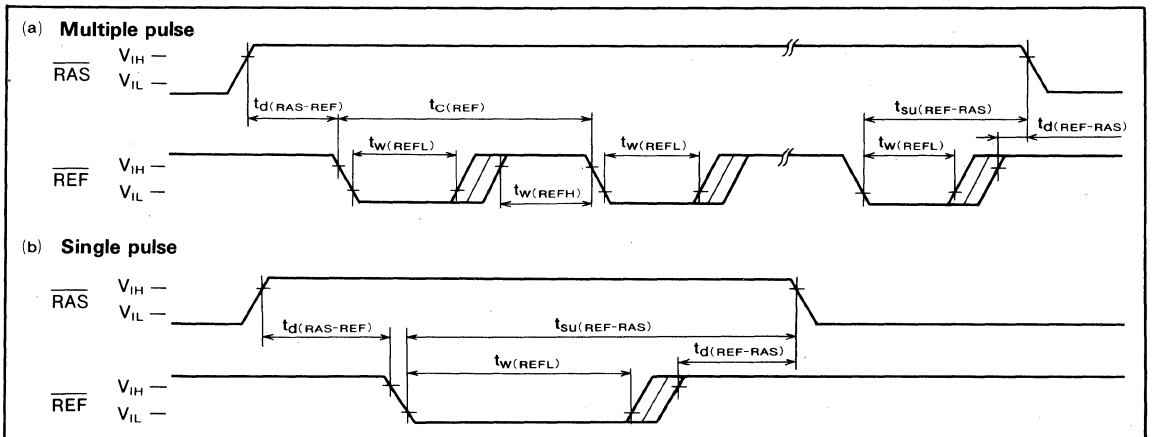

Fig. 1.39 (b) Printed board pattern

## M5K4164AP Refresh Methods

The refreshing of the M5K4164AP cell matrix requires the refreshing of 128 row addresses at least every 2ms. In addition to the previously available $\overline{RAS}$-only refresh method, the M5K4164AP provides $\overline{REF}$ (pin 1) automatic refreshing, and self-refreshing. This section will cover the application of $\overline{REF}$ refresh operations.

### 1. Automatic Refresh

Automatic refresh begins after RAS precharge ($\overline{RAS}$-$V_{IH}$) upon setting $\overline{REF}$ (pin 1) to low. This method is quite similar to the $\overline{RAS}$-only refresh with the refresh address counter output present as a 7-bit word for automatic refreshing the refresh counter being automatically incremented at the end of the refresh cycle. Fig. 1.40 shows the automatic refresh timing.




| Symbol | Parameter | Alternative symbol | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | M5K4164AP-12 | | M5K4164AP-15 | | |
| | | | Min | Max | Min | Max | |
| $t_{C(REF)}$ | Automatic refresh cycle time | $t_{FC}$ | 220 | | 260 | | ns |
| $t_{d(RAS-REF)}$ | Delaytime, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{W(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FP}$ | 60 | 8000 | 60 | 8000 | ns |
| $t_{W(REFH)}$ | $\overline{REF}$ high pulse width | $t_{FI}$ | 30 | | 30 | | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FSR}$ | 30 | | 30 | | ns |
| $t_{su(REF-RAS)}$ | $\overline{REF}$ setup time before $\overline{RAS}$ | $t_{FRD}$ | 250 | | 295 | | ns |

**Fig. 1.40 Automatic refresh timing**

Automatic refresh has many advantages over the $\overline{RAS}$-only refresh method generally used previously. As shown in Fig. 1.41, $\overline{RAS}$-only refresh generally requires logic circuitry. This consists of the row-address, column-address and refresh address multiplexer and refresh address counter. With automatic refresh, the dotted area shown in Fig. 1.41 may be eliminated.

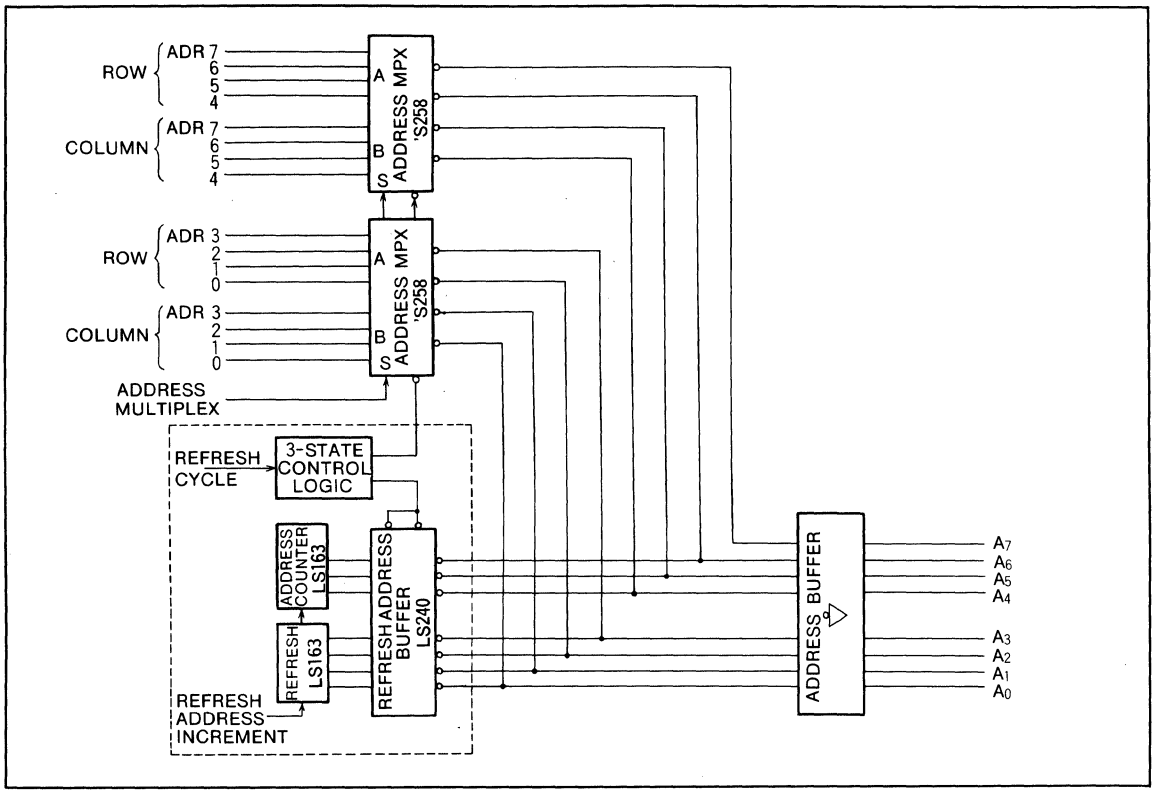



**Fig. 1.41 Address multiplexer and refresh address counter**

By decoding $\overline{RAS}$, one bank of a complex memory system may be selected, while for $\overline{RAS}$-only refresh $\overline{RAS}$ is fed to all portions of the memory requiring the decoder as shown in Fig. 1.42 (a). With automatic refresh, $\overline{RAS}$ is used during the memory cycle and $\overline{REF}$ for the refresh cycle independently so that the gate shown in Fig. 1.42 (b) can be eliminated.

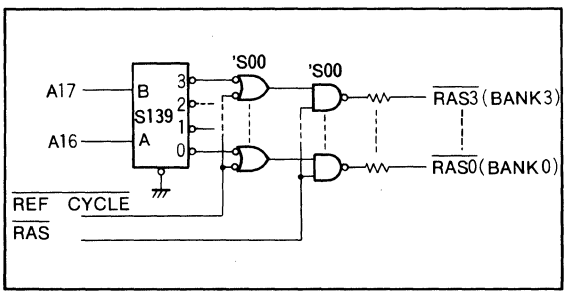



**Fig. 1.42 (a) $\overline{RAS}$ decoder in $\overline{RAS}$-only refresh**

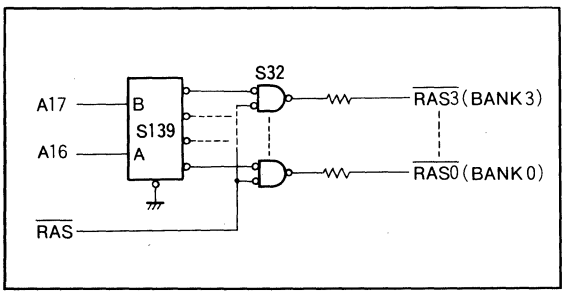



**Fig. 1.42 (b) $\overline{RAS}$ decoder using $\overline{REF}$ pin**

Another feature of automatic refresh is that the timing of the refresh controller is simplified. The timing for $\overline{RAS}$-only refresh and automatic refresh is shown in Fig. 1.43 (a) and Fig. 1.43 (b) respectively.

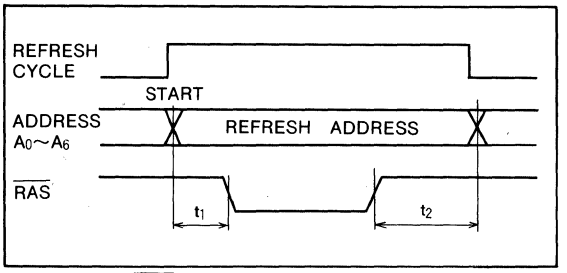



**Fig. 1.43 (a) $\overline{RAS}$-only refresh timing**

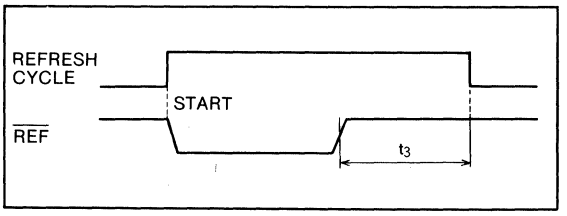


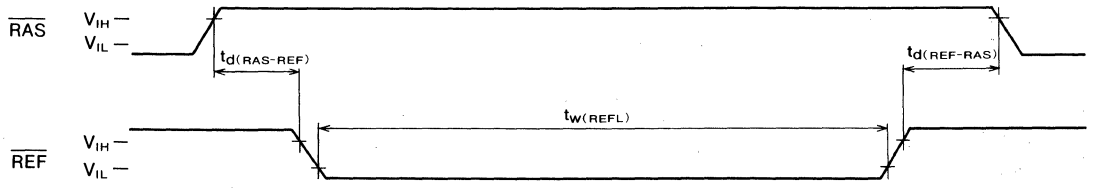

**Fig. 1.43 (b) Automatic refresh timing**

For $\overline{RAS}$-only, the controller disables the address multiplexer upon entering the memory cycle while it enables the refresh counter output. Next, after a delay time of $t_1$ (required because of the address buffer delay time and row address setup time $t_{su(RA-RAS)}$, $\overline{RAS}$ is set to low. The refresh cycle ends at the time $t_2$ that $\overline{RAS}$ is precharging.

In contrast to this, the automatic refresh controller sets $\overline{REF}$ to low simultaneously with the beginning of the refresh cycle, and after the $\overline{RAS}$ precharge time $t_3$, the refresh cycle ends. For this reason, there is no necessity to consider the settling time for address selection.

**2. Self Refresh**

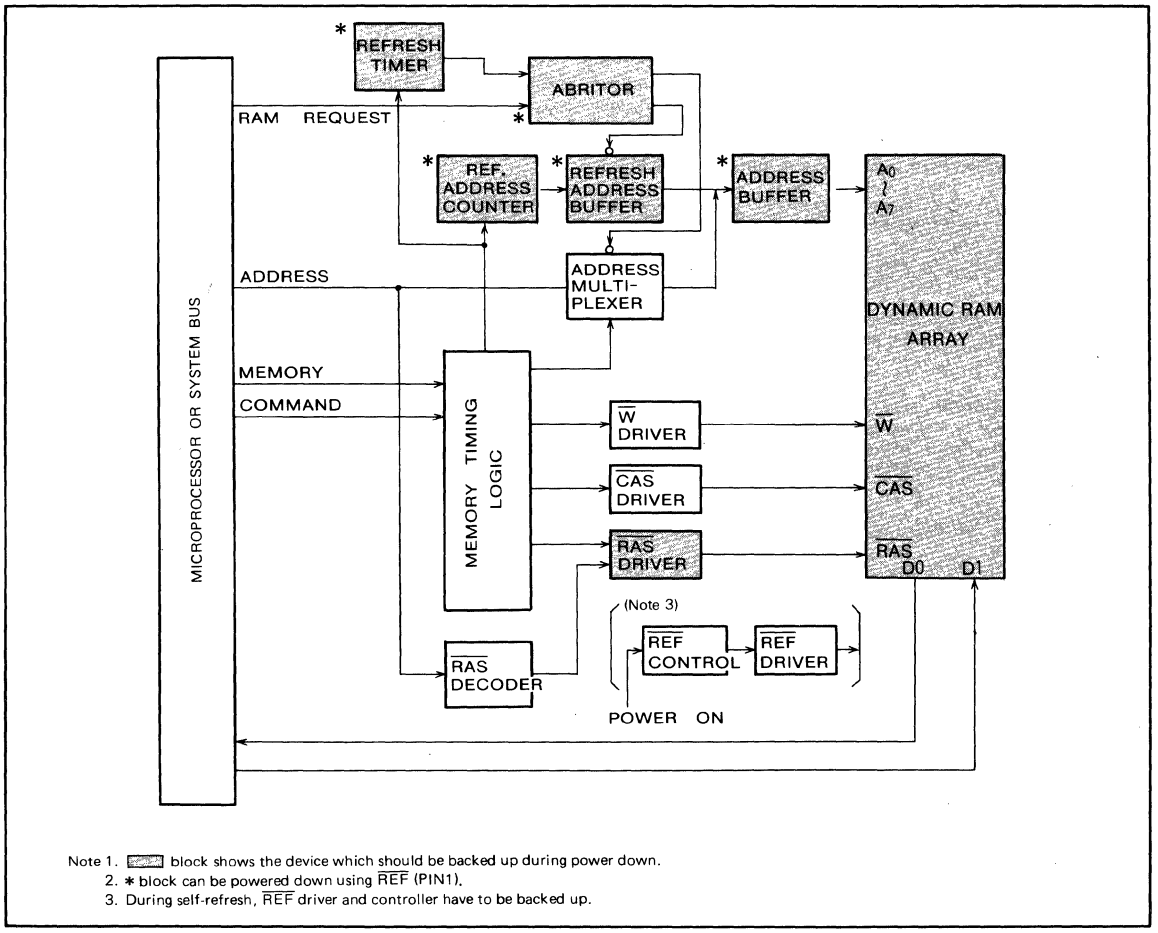
Self refresh, similar to automatic refresh, sets $\overline{REF}$ low after $\overline{RAS}$ precharge occurs, beginning the internal refresh cycle. This method of refresh ignores all other inputs as long as $\overline{RAS}$ is high and $\overline{REF}$ is low, making use of an internal timer to automatically refresh the row addresses every 12 – 16$\mu$s which enables all cells to be refreshed within 2ms. The rising edge of $\overline{REF}$ terminates the refresh operation and after one cycle ($t_{d(REF-RAS)}$)a normal read-write cycle is entered. Fig. 1.44 shows the timing for the self refresh cycle. Self refresh is an extremely effective method of providing memory backup by means of a secondary power supply. As shown in Fig. 1.45, most of the required functions are implemented within the chip for the $\overline{RAS}$-only refresh with a simplified external circuit. This results in low power consumption and a long life for the secondary power supply.




| Symbol | Parameter | Alternative symbol | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | M5K4164AP-15 | | M5K4164AP-20 | | |
| | | | Min | Max | Min | Max | |
| $t_{d(RAS-REF)}$ | Delay time, $\overline{RAS}$ to $\overline{REF}$ | $t_{RFD}$ | 90 | | 100 | | ns |
| $t_{w(REFL)}$ | $\overline{REF}$ low pulse width | $t_{FBP}$ | 8000 | ∞ | 8000 | ∞ | ns |
| $t_{d(REF-RAS)}$ | Delay time, $\overline{REF}$ to $\overline{RAS}$ | $t_{FBR}$ | 310 | | 345 | | ns |

**Fig. 1.44 Self-refresh timing**

As described above, self refresh may not be used in the $\overline{RAS}$-only refresh mode. In designs using two refresh counters (internal and external) which operate independently, guaranteeing the refresh (2ms) time is difficult.




Note 1. ▨ block shows the device which should be backed up during power down.
2. * block can be powered down using $\overline{REF}$ (PIN1).
3. During self-refresh, $\overline{REF}$ driver and controller have to be backed up.

**Fig. 1.45 Typical dynamic RAM system with battery back up**

### 3. Design Example

The design example shows the increased effectiveness of $\overline{REF}$ (pin 1) refresh when the M5K4164AP is used as the memory for a microprocessor. This design example illustrates the interface between the M5K4164AP and the microprocessor.

When using $\overline{REF}$ for the microprocessor memory in interface, two methods are possible. One is asynchronous refresh and the other involves synchronously refreshing the memory. The former technique is not affected by the microprocessor status (i.e., reset, wait state, DMA, and CPU clock). However, control logic is somewhat complex. While the second method makes use of simple control logic, the microprocessor must satisfy the refresh operation timing conditions.

Fig. 1.46 through 1.48 show the block diagram, schematic diagram, and timing deiagram for the asynchronous refresh example. For this example, the refresh cycle counter refresh request ($\overline{REFREQ}$) starts the refresh cycle independently of the microprocessor operation. The arbiter determines whether the microprocessor ($\overline{RAMREQ}$) or refresh cycle counter ($\overline{REFREQ}$) has access to the RAM.

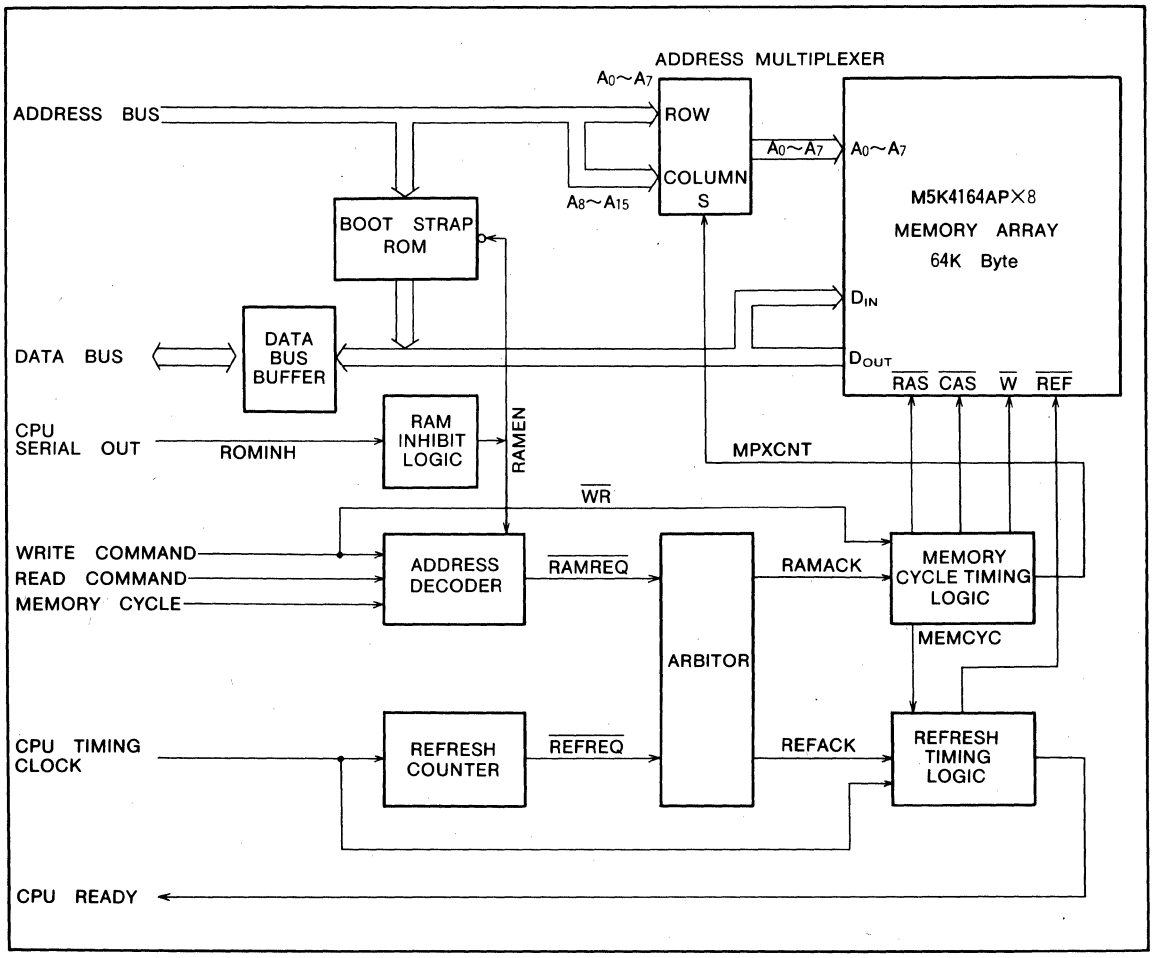
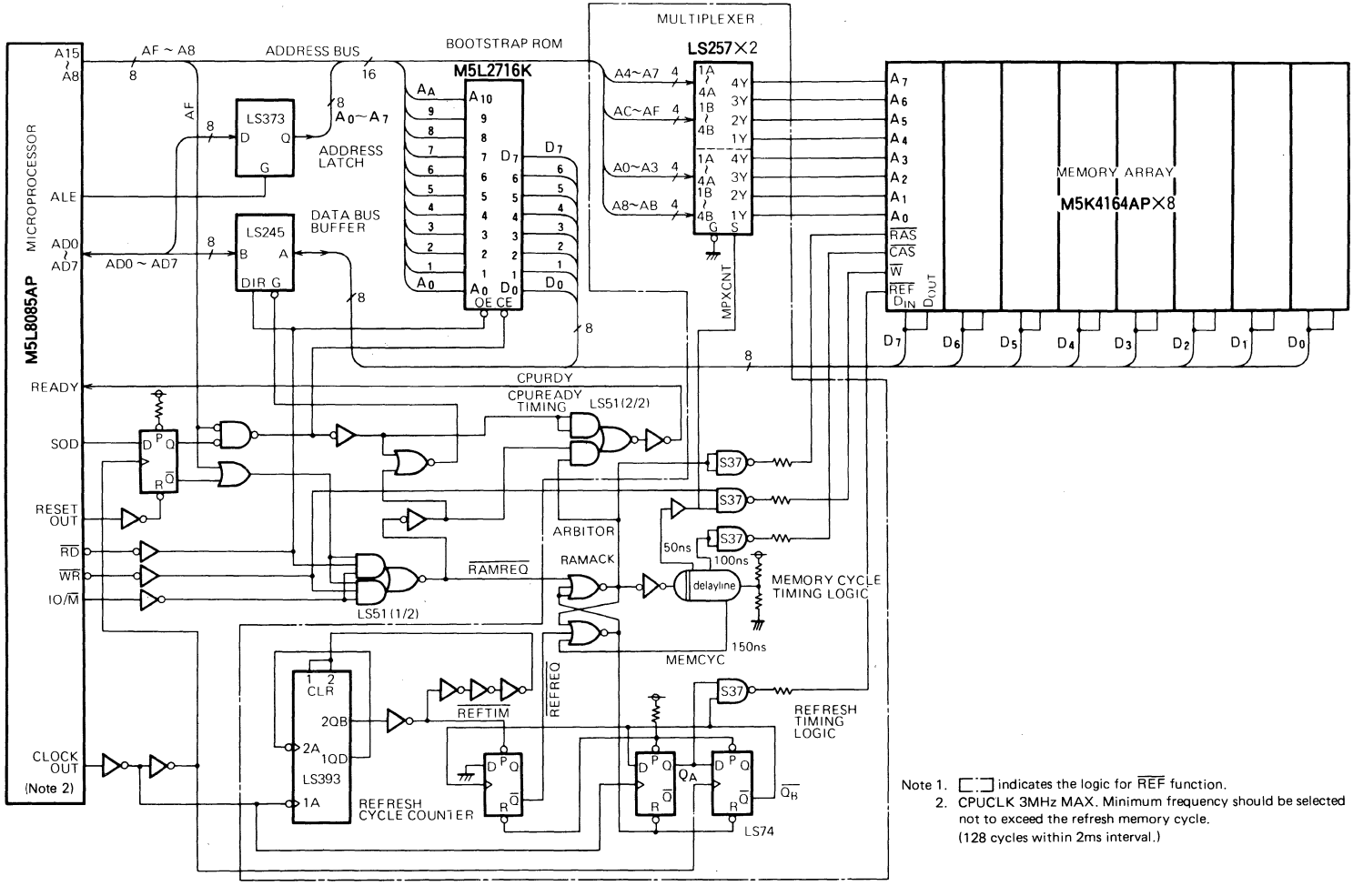
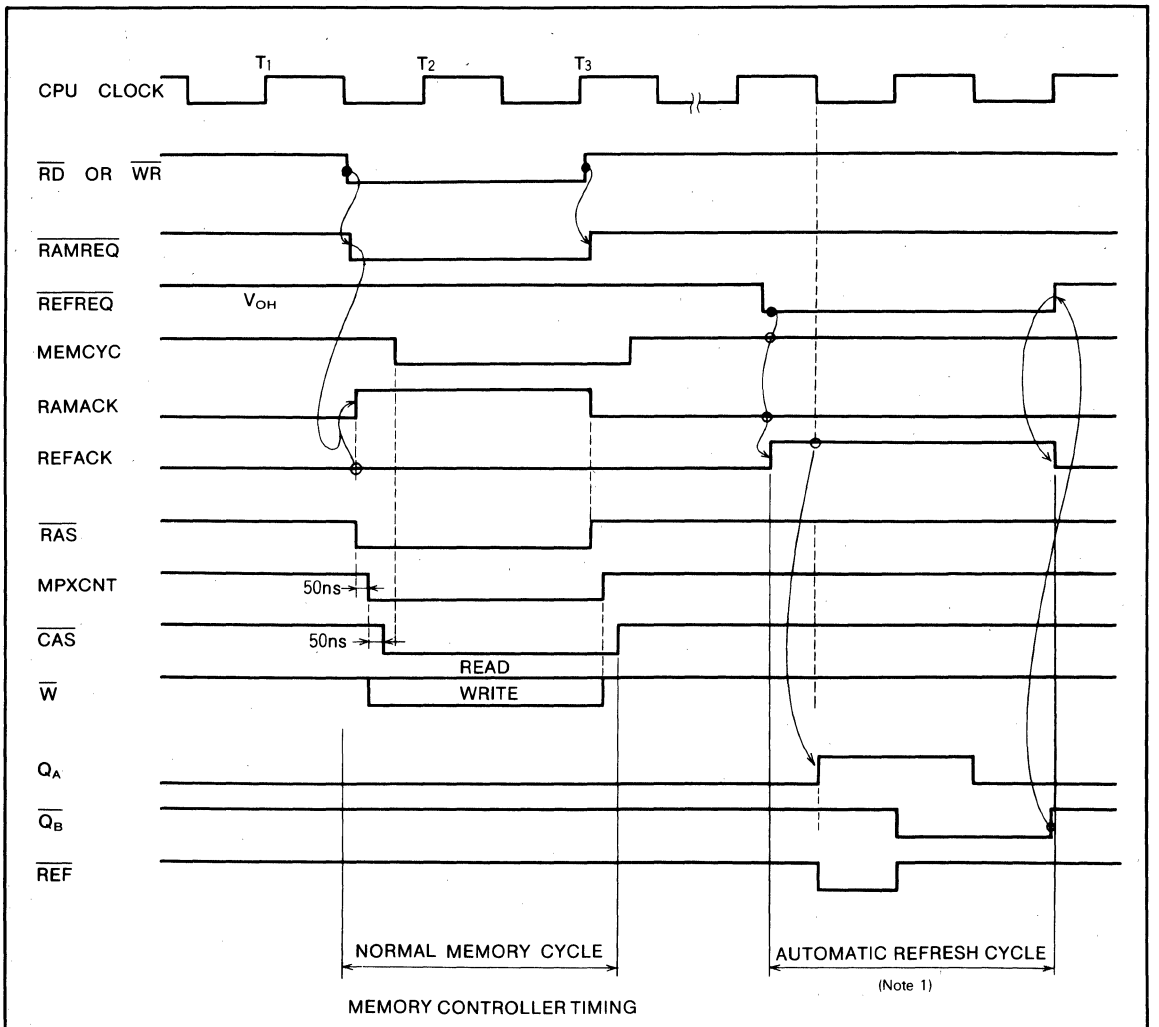



**Fig. 1.46 Block diagram of the design example (Ansynchronous)**




Note 1. ⌐¬ indicates the logic for $\overline{REF}$ function.
2. CPUCLK 3MHz MAX. Minimum frequency should be selected not to exceed the refresh memory cycle.
(128 cycles within 2ms interval.)

**Fig. 1.47 Design example of microprocessor interface (Ansynchronous)**




Note 1. If the microprocessor attempts to access the RAM during this period, it must wait until the refresh is over.

**Fig. 1.48 Memory and refresh timing (Ansynchronous)**

A bootstrap ROM, commonly used in this type of memory system, is shown in the example. This is used to load the initial program of a RAM-based system into RAM from disk, for system initialization. In this example, the SOD (Serial Out Data) of the M5L8085AP is used to select either the bootstrap ROM or RAM as shown in Fig. 1.49.

Fig. 1.50 and 1.51 show the schematic diagram and timing for the synchronous refresh example. In this example a Z80 microprocessor is used with synchronous refresh. As shown in Fig. 1.51, after the Z80 fetch instruction, the refresh operation is performed ($T_3$ and $T_4$ state).

In this manner refresh is performed synchronously with microprocessor operation. As mentioned previously, this type of operation involves a variety of limitations which must be considered carefully when designing such a system. (i.e., wait state, DMA, reset and CPU clock cycle)

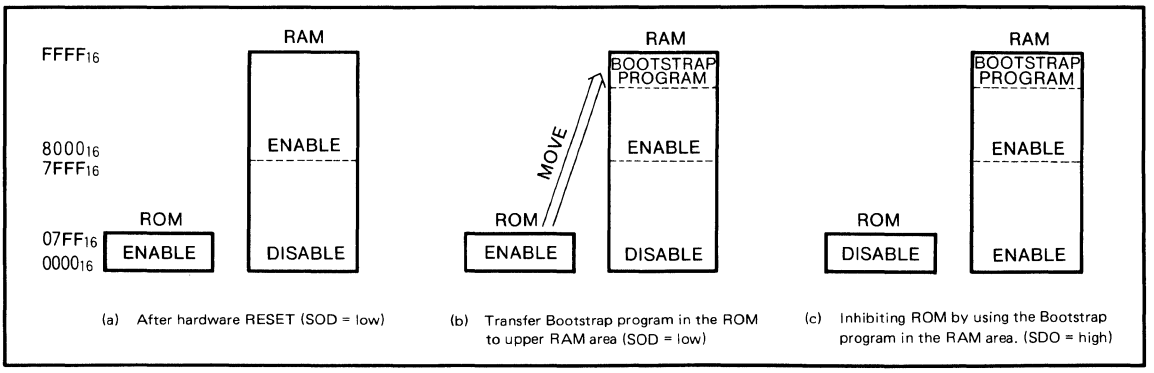



**Fig. 1.49 Start-up procedure of the memory-overlapped system**

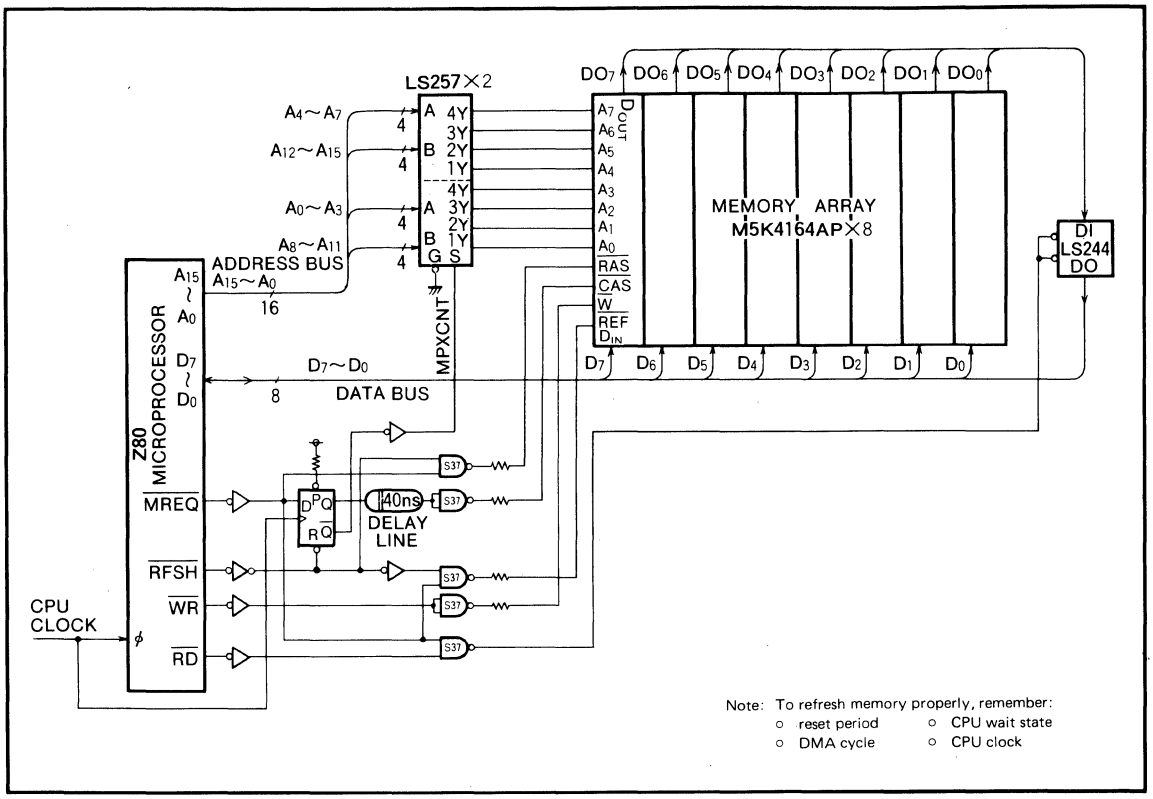



**Fig. 1.50 Design example of microprocessor interface (Synchronous)**

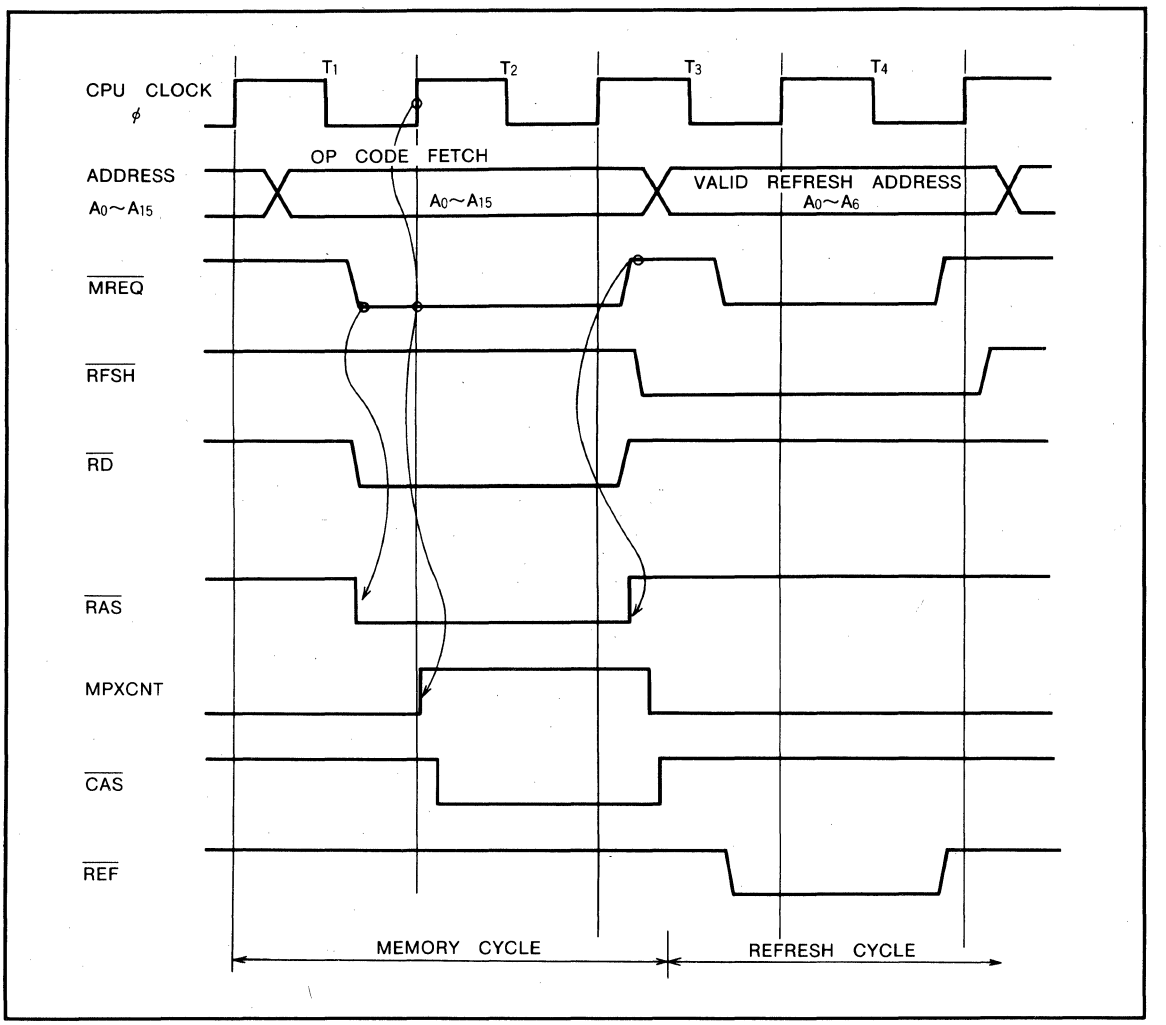



**Fig. 1.51 OP code fetch and refresh timing**

## STATIC RAM TECHNOLOGY

### Introduction

Static RAM, though inferior to dynamic RAM in density of integration, is used for a wide variety of applications. It is easy to use as it does not reguire clocks, refresh operation or related controlling peripheral ICs. In addition, static RAMs are available for equipment requiring high-speed operation or battery backup in case of power failure.

### 1. Classification of Static RAM

Static RAMs are classified into the following:

(1) medium-speed NMOS for easy use and economy
(2) ultra-high speed NMOS for computer application
(3) CMOS for battery backup.

Mitsubishi Electric Corporation provides the following lineup of static RAM.

| | | |
|---|---|---|
| (1) | Medium-speed NMOS | M58725P |
| (2) | Ultra-high-speed NMOS | M5M2167S/P, M5M2168S/P |
| (3) | CMOS | M5M5116P, M5M5117P, M5M5118P, M5M5165P |

### 2. History of Mitsubishi Memory Cells

The history of Mitsubishi memory cells is illustrated in Fig. 2.1. Mitsubishi Electric began producing 256-bit E/E type memory cells and later shifted over to high resistive load types, diminishing cell area and cutting power consumption of memory cells. A high resistive load, which is available up to 100MΩ has reduced the cell current to as low as 10nA/cell. CMOS was started at 1K bits, developed into 4K bits and then to 16K bits. The standby supply current consumed in the cells and in periferal circuits is as low as the leakage current. The specified value is 20μA, but the typical value is less than 1μA, enabling long term battery buckup operation. CMOS, however, has suffered the disadvantage of poor production costs due to its larger cell area. In the past, either economical NMOS or low power CMOS had to be selected to match the application. But, the situation has somewhat changed with the appearance of 64K bit memories, incorporating NMOS and CMOS technology. The mixture of high resistive load NMOS cells and CMOS peripherals, realized the hybrid which has the economy of NMOS and the low power of CMOS. Mitsubishi has provided the M5M5165P fabricated by this technology. The technical factors resulting in the development of this product are as follows: i) limit of large power consumption and ii) technology of fabricating high resistance of several tens of GΩ enabled low standby current which is enough for battery backup applications.

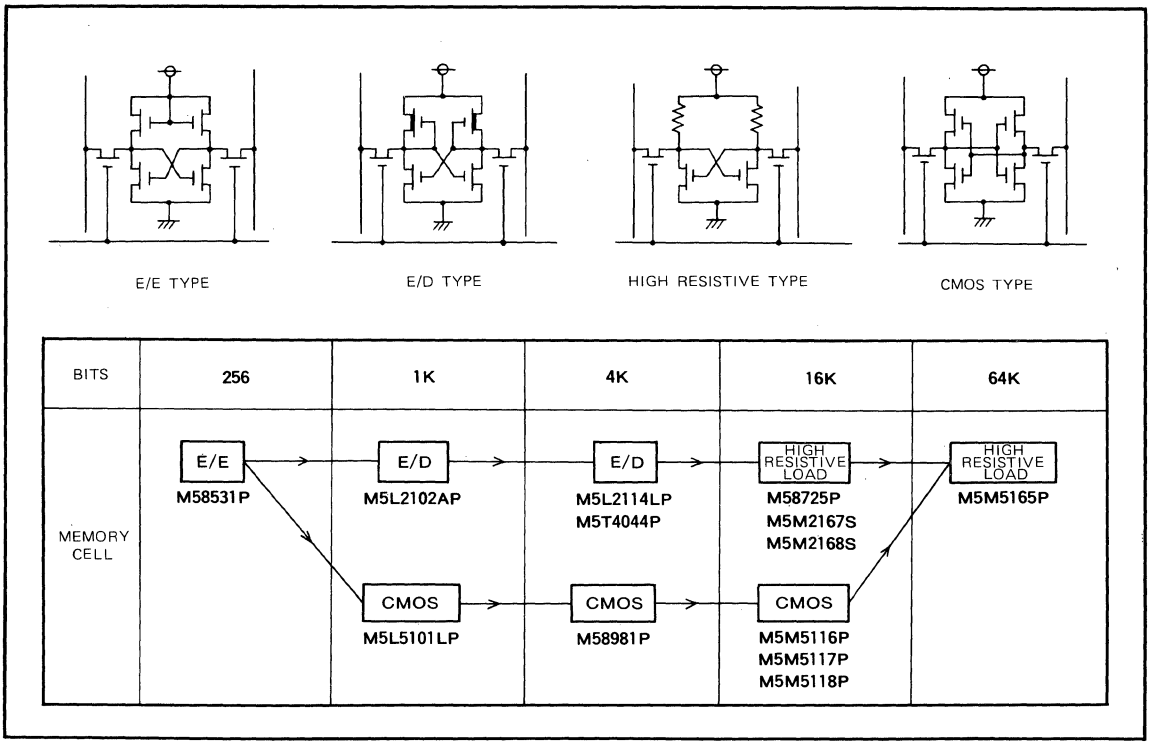



**Fig. 2.1 History of Mitsubishi cells**

## 3. Methods of Power Saving

Power consumption has become a major problem as memory capacity has increased. The solution lies in 1) the use of CMOS for peripheral circuits, 2) the division of cell array and 3) the employment of internal synchronous circuits.

Method (1) has been employed in the 64K CMOS M5M5165P.

Method (2) is aimed at decreasing the number of memory cells selected by the word decoder in order to decrease the current that flows into cells from the bit line. Fig. 2.2 shows examples of dividing the cell array. With 1K and 4K bit RAM, all the bit lines are activated, while 1/2 of the bit lines are activated with 16K and only 1/4 are designed to be activated with 64K. (d) is called the devided word line method (DWL), dividing the memory cell array into arbitrary lines, which is considered to be an important method to deal with RAMs of greater capacity in the future. The internal synchronous circuit (3), designed to cut DC current, lowers the average current greatly by the employment of a dynamic circuit. In previous asynchronouse circuits, DC current was constantly running while chips were in the active state.

A problem with the internal synchronous circuit is providing a standard clock. Unlike dynamic RAM, static RAM is not given an external clock and must generate the clock by itself. As the memory cycle of static RAM starts with an address change, the internal synchronous circuit makes use of changes in the address signal and generates an internal clock. In this circuit, the charging current of internal mode capacitance runs at the peak rate at the beginning of the cycle and no current runs after the access is finished. As the average current can be decreased to 1/10 of the conventional one (at 1 MHz), this device is most suitable for battery-operated equipment such as hand held computers.

## 4. Package

The more the capacity, the more the number of pins. (4K has 18 pins, 16K, 24 pins and 64K, 28 pins). On the other hand, a smaller package is required for the high density mounting. Available packages which meet these requirements are falt package, chip carrier (LCC), ZIL (zigzag in-line), or shrink pack (lead spacing is 2/3 of the normal type).

Mitsubishi provides the 16K CMOS RAM M5M5116FP series using the flat package. Fig. 2.4 shows the outline difference between the DIP and flat package. The flat package is approximately half the size of DIP.

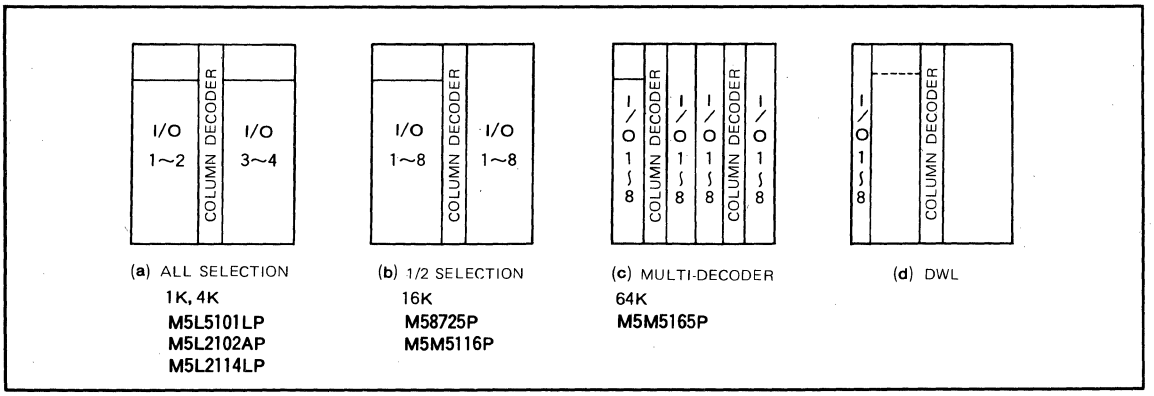



**Fig. 2.2 Examples of memory cell array**

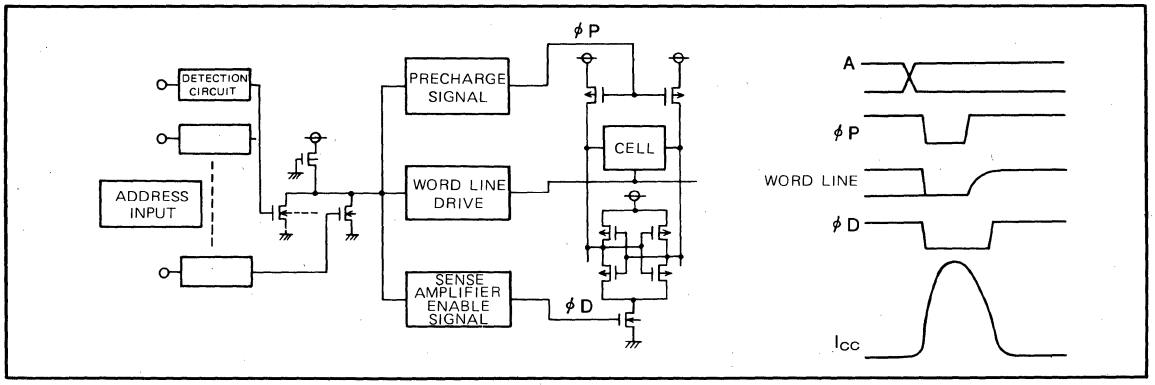



**Fig. 2.3 Circuit diagram of internal synchronous circuit**

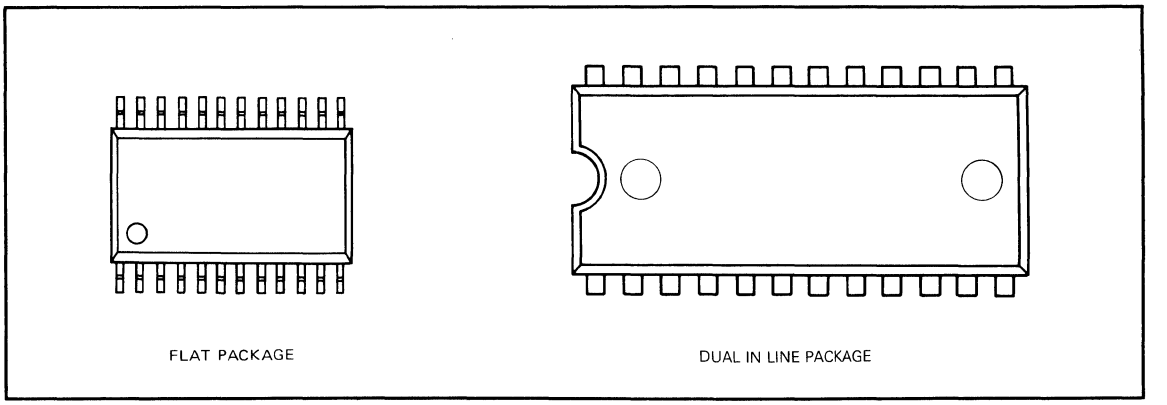



**Fig. 2.4 Comparison of package outlines**

## OPERATION OF STATIC RAM

The timing of static RAM is simple and operation modes are very easily understood because of its asynchronous operation that does not require strobe signals to take in clock signals or external signals.

In this chapter, basic operation of static RAM and functions of various input signals are illustrated using the M58725P 16K static RAM as an example.

Fig. 2.5., 2.6., 2.7. are the block diagram, pin configuration and function table of M58725P.

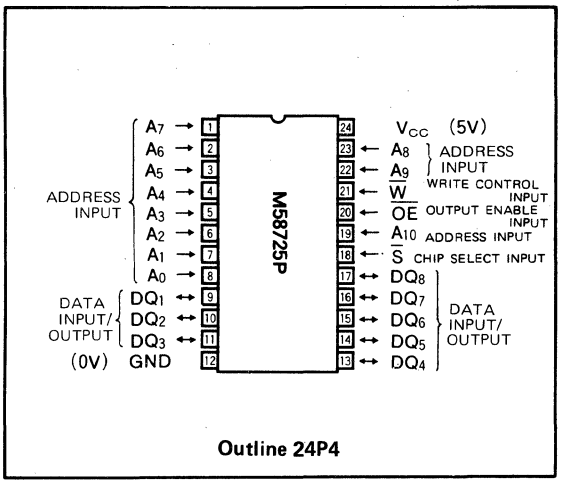



**Fig. 2.6 Pin configuration of M58725P**

| $\overline{S}$ | $\overline{OE}$ | $\overline{W}$ | Modes | $DQ_1 \sim DQ_8$ | $I_{CC}$ |
|---|---|---|---|---|---|
| H | X | X | | High impedance | Standby |
| L | L | H | Read mode | $D_{OUT}$ | Active |
| L | X | L | Write mode | $D_{IN}$ | Active |
| L | H | H | — | High impedance | Active |

**Fig. 2.7 Function table of M58725P**

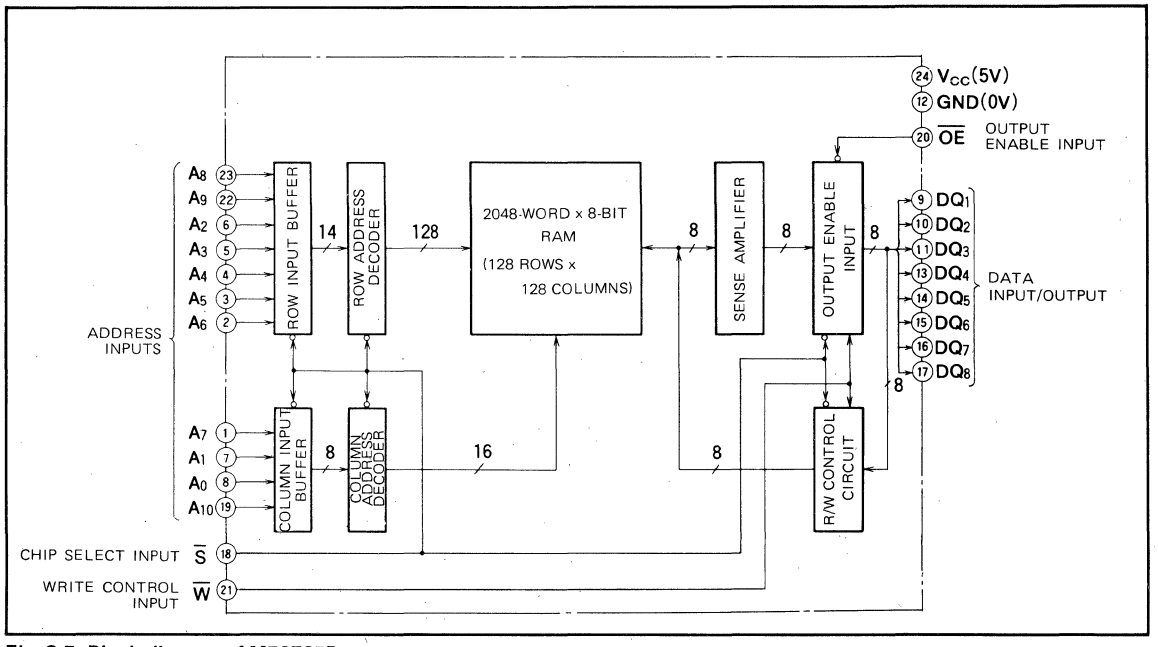



**Fig. 2.5 Block diagram of M58725P**

## 1. Functions of input signals

**(1) Address signals ($A_0$~$A_{10}$)**

Address signals select one random bit out of the memory matrix. Read/write memory operation is made to the cell which selected by address signal.

**(2) Chip select signal ($\overline{S}$)**

When $\overline{S}$ = L, RAM is in the active state, enabling read/write memory operation. When $\overline{S}$ = H, RAM is in the non-selective state, disabling memory operation. In this case, the output is in the high impedance state, easily expanding memory capacity with other memorys by OR connection. In addition the supply current is in standby state and is reduced to one tenth of the normal level which contributes to the power saving of a large memory system. In most cases, like M58725P, the chip select signal is in negative logic (chip is selected when signal is L) but it is noted that S2 of M5M5165P is in positive logic (chip is selected when signal is H).

**(3) Write control signal ($\overline{W}$)**

The $\overline{W}$ signal controls operation modes of read and write. The low level $\overline{W}$ enables the write mode and the high level $\overline{W}$ enables the read mode. When the write mode is enabled the data input/output (DQ) terminal is in high impedance state.

**(4) Output enable signal ($\overline{OE}$)**

The $\overline{OE}$ signal controls the output stage directly at high speed. When $\overline{OE}$ = L, the DQ terminals are in the output mode, and when $\overline{OE}$ = H, they are in the high impedance state. When write operation is enabled and $\overline{OE}$ is set to H, the DQ terminals are in high impedance state and, thus, clash of RAM data output and data input, so called data bus contention, is avoided. When read operation is enabled, $\overline{OE}$ must be L so that DQ terminals may be in the output mode.

## 2. Read operation

Fig. 2.8 shows the timing diagram of the read cycle. When $\overline{S}$ and $\overline{OE}$ and L and $\overline{W}$ is H, the read mode is enabled and the memory cell data selected by the address signal is read at the DQ terminal. There are three kinds of read cycle timing, as showen in Fig. 2.8. They are defined as (a) address access time $t_{a(A)}$, (b) chip select access time $t_{a(S)}$, and (c) $\overline{OE}$ access time $t_{a(OE)}$.

(a) is applied when $\overline{S}$ and $\overline{OE}$ have already been set to L long before the address change. (b) is applied, contrary to (a), when $\overline{S}$ is set to L simultaneously or after the change of the address signal. In this case, $\overline{OE}$ must be L before the address change, as well as in the case of (a).

(c) is applied when the $\overline{OE}$ signal has been set to L well after the change of the address signal or the chip select signal. The $\overline{OE}$ signal controls the output buffer circuit directly at a high speed, so the high speed access time of nealy one-half of that of (a) or (b) is available. When $\overline{OE}$ is set L faster than the timing of $t_{a(A)} - t_{a(OE)}$ or $t_{A(S)} - t_{a(OE)}$, (a) or (b) is applied.

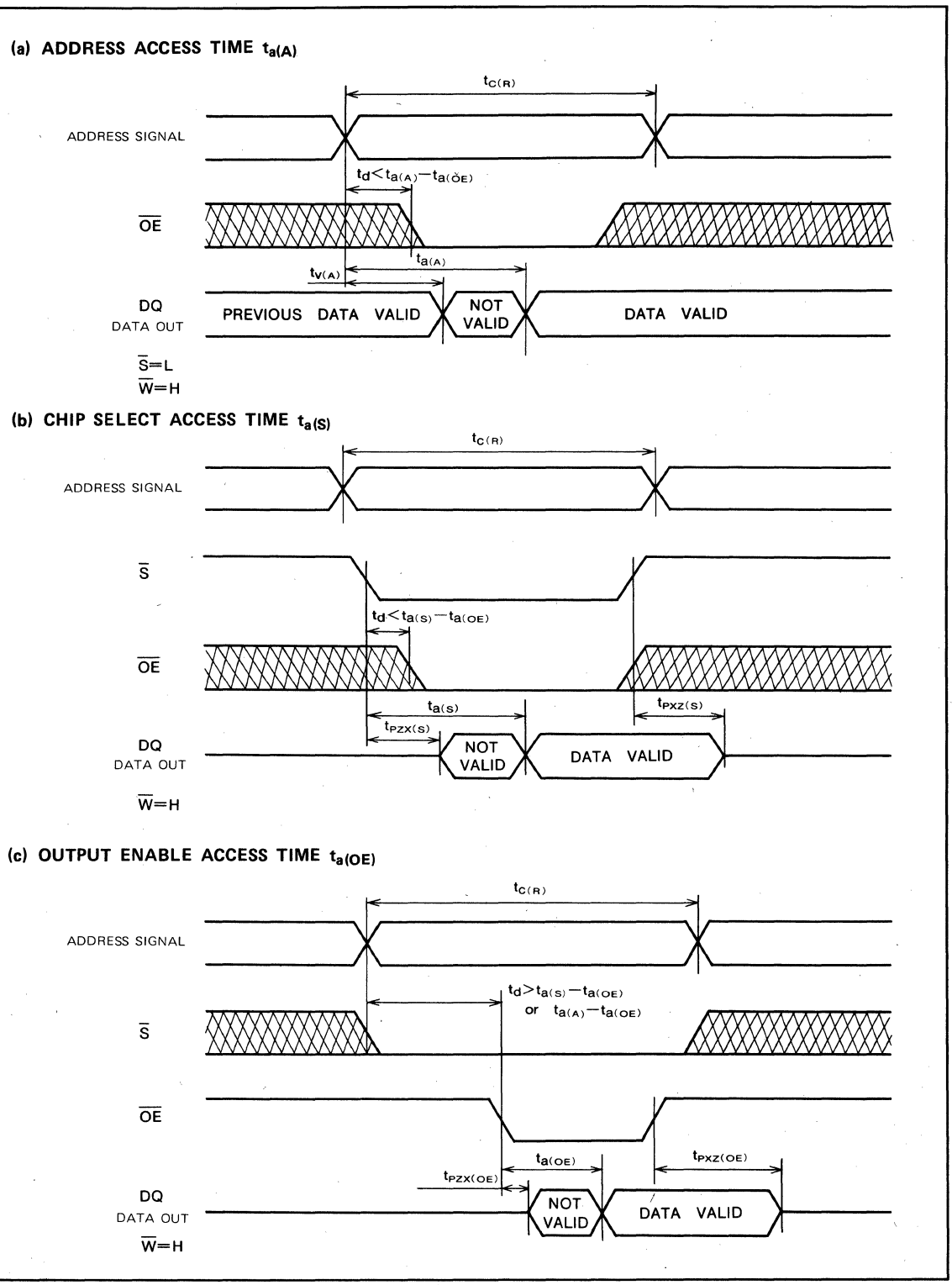



**Fig. 2.8 Read cycle timing**



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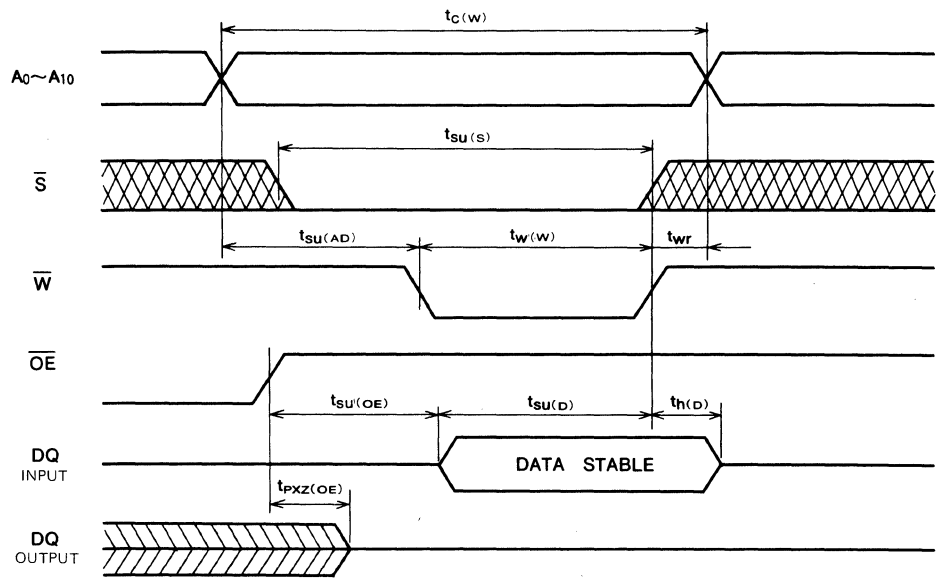
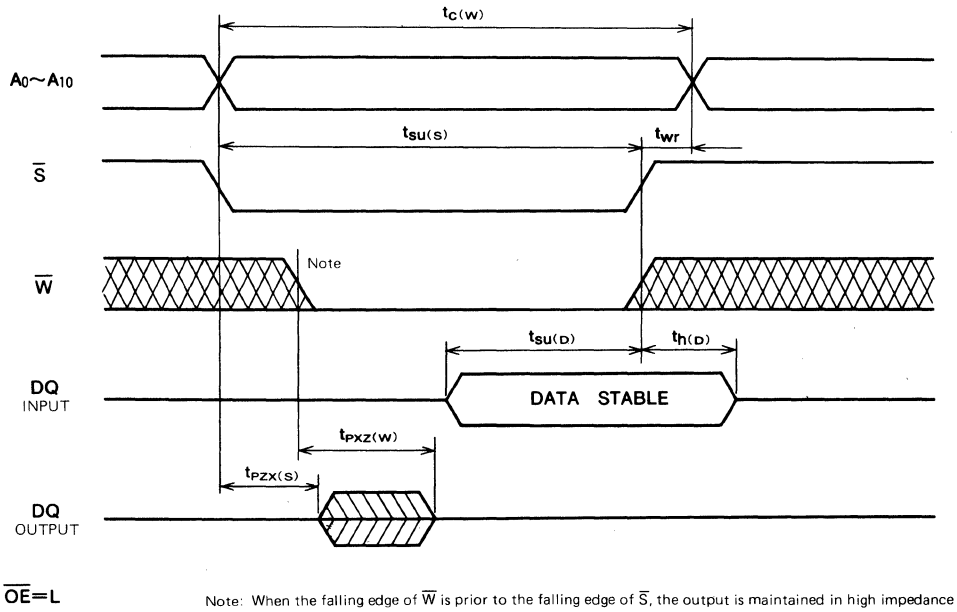
## 3. Write operation

Fig. 2.9 shows the timing diagram of the write cycle. Write operation is excuted when $\overline{S}$ and W are both L. When either $\overline{S}$ or $\overline{W}$ goes to H, the data of the DQ terminal is written into the memory cell. Therefore, for the rise of $\overline{W}$ or $\overline{S}$, data setup time $t_{su(A)}$ and data hold time $t_{h(D)}$ must be maintained. Address setup time $t_{su(A)}$ and write recovery

**(a) WRITE CYCLE 1 ($\overline{W}$ CONTROL MODE)**




**(b) WRITE CYCLE 2 ($\overline{S}$ CONTROL MODE)**




Note: When the falling edge of $\overline{W}$ is prior to the falling edge of $\overline{S}$, the output is maintained in high impedance state.

**Fig. 2.9 Write cycle timing**

time $t_{wr}$ are defined in order to avoid writing into a cell designated by previous or following cycles.

At the write cycle, the data bus contention problem is a matter of concern. The subject is discussed in detail in later chapters.

### 4. Standby Mode

When $\overline{S}$ is H, the chip becomes non-selective mode and the supply current is in the standby mode. The Supply current decreases to one tenth of the normal operation level, which contributes to power saving in systems that use many memory devices. Fig. 2.10 shows the supply current waveform for M58725P.

In the case of CMOS RAM, the stand by current is as low as the leak current and, the memory cell data can be held at a $V_{CC}$ of 2V, enabling battery backup applications.

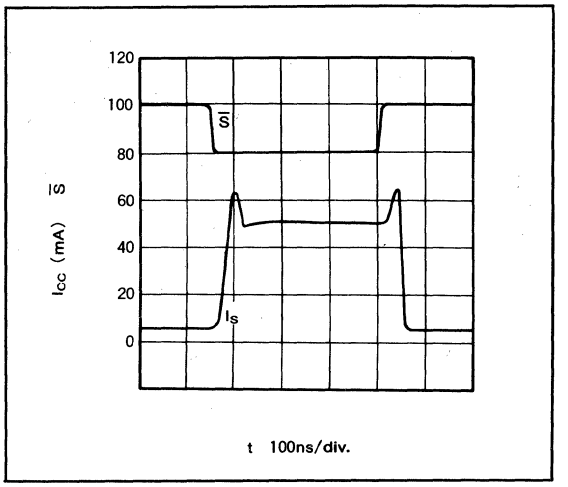


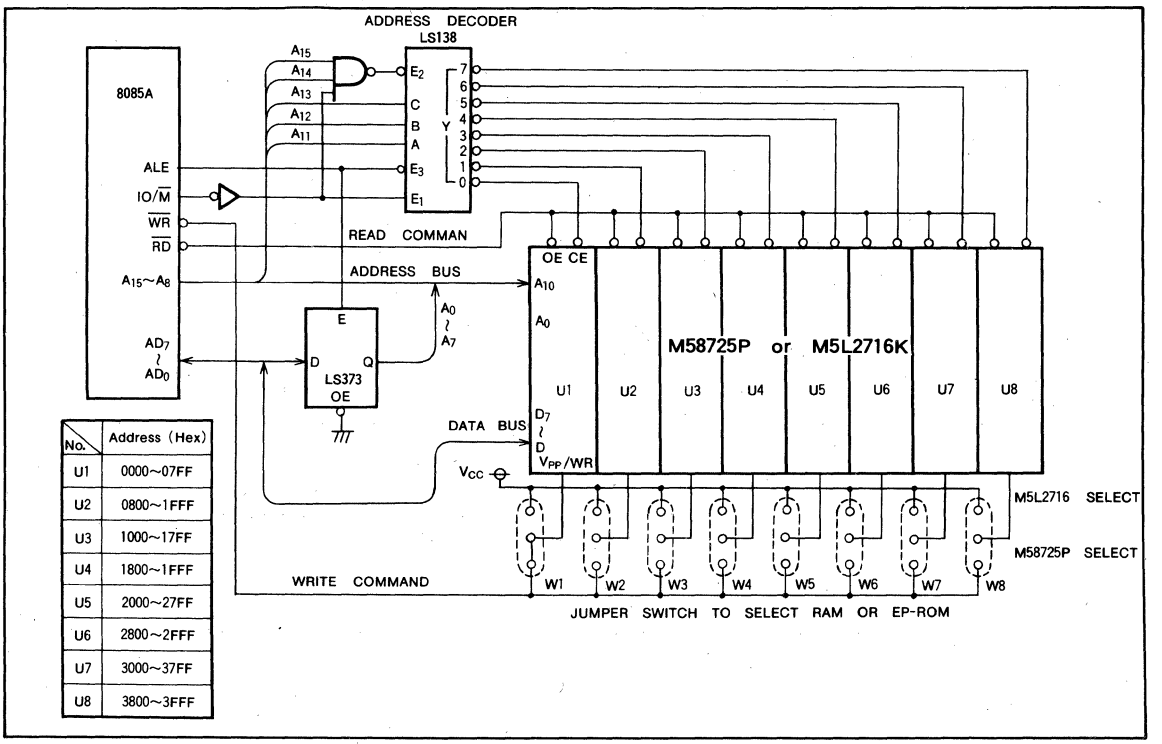

**Fig. 2.10 Power saving by $\overline{S}$**

## APPLICATION OF STATIC RAM

To explain the application of static RAMS, two examples are used; M58725P, which has $\overline{OE}$ input, and M5M5118P, which has no $\overline{OE}$ inputs.

### 1. Application of M58725P

Fig. 2.11 is an example of an M58725P application. The 8085A is used for the CPU. The chip select signal is gated by ALE output of 8085A. Therefore, the chip select signal turns to low, synchronously with the fall of ALE. $\overline{W}$ is connected to $\overline{WR}$ and $\overline{OE}$ is connected to the $\overline{RD}$ output of the CPU. The RAMs which have $\overline{OE}$ input can avoid the data bus contention problem by use of $\overline{RD}$ output as an $\overline{OE}$ signal.




| No. | Address (Hex) |
|---|---|
| U1 | 0000~07FF |
| U2 | 0800~1FFF |
| U3 | 1000~17FF |
| U4 | 1800~1FFF |
| U5 | 2000~27FF |
| U6 | 2800~2FFF |
| U7 | 3000~37FF |
| U8 | 3800~3FFF |

**Fig. 2.11 Application circuit of M58725P**

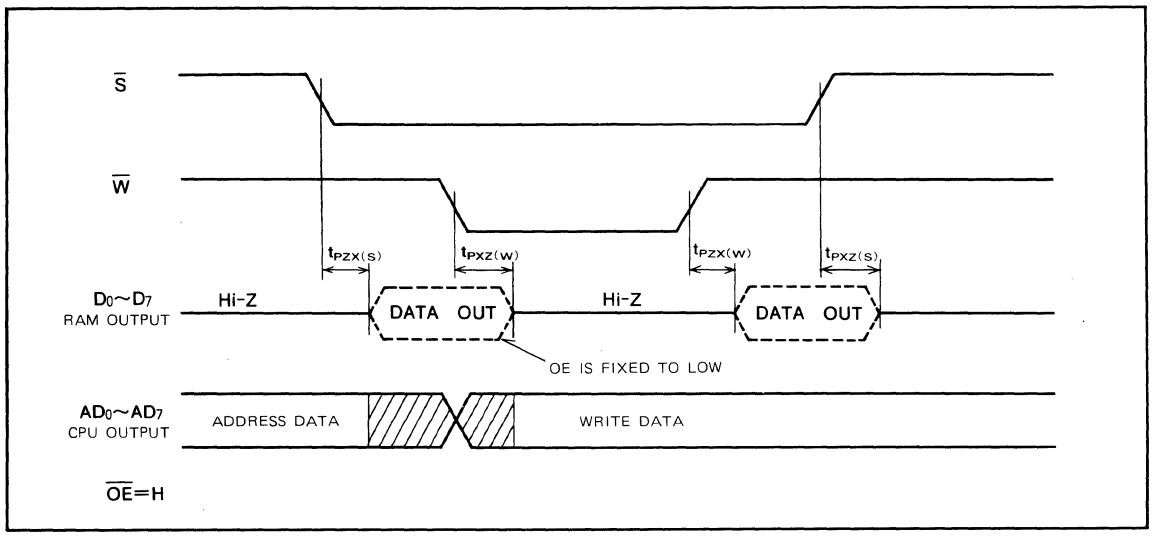



**Fig. 2.12 Write cycle timing**

## 2. Application of M5M5118P

The M5M5118P offers easy memory expansion or battery backup due to its two chip select signals, but because of the lack of $\overline{OE}$ input, the data bus contention problem must be taken into consideration during system design. Fig. 2.12 illustrates the timing diagram of the circuit shown in Fig. 2.11. In this system, $\overline{S}$ is synchronous with ALE and $\overline{S}$ is set to low before setting to $\overline{W}$. Therefore, when a RAM without an $\overline{OE}$ terminal, like M5M5118P, or a RAM whose $\overline{OE}$ terminal is fixed to low is used, data input/output terminals are in the output state during the period shown by broken lines, causing contention of RAM and CPU outputs, making a large current flow through each output transistor. Output bus contention should be considered only at the beginning of the write cycle, the period shown by cross hatching but is no longer a concern once write is completed because both outputs have the same phase. But data bus contention can be avoided when $\overline{S}$ is turned to low simultaneously with $\overline{W}$ or right after $\overline{W}$. This is because, when $\overline{S}$ and $\overline{W}$ are turned to low simultaneously, the output buffer circuit remains in high impedance state. This timing can be obtained by adding $\overline{WR}$ and $\overline{RD}$ as a condition of generating the chip select signal as shown in the application example in Fig. 2.14.

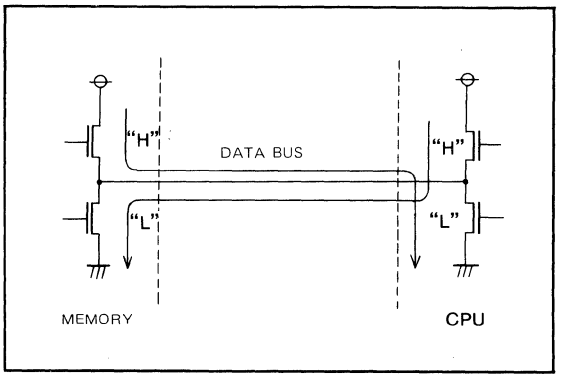



**Fig. 2.13 Data bus contention**

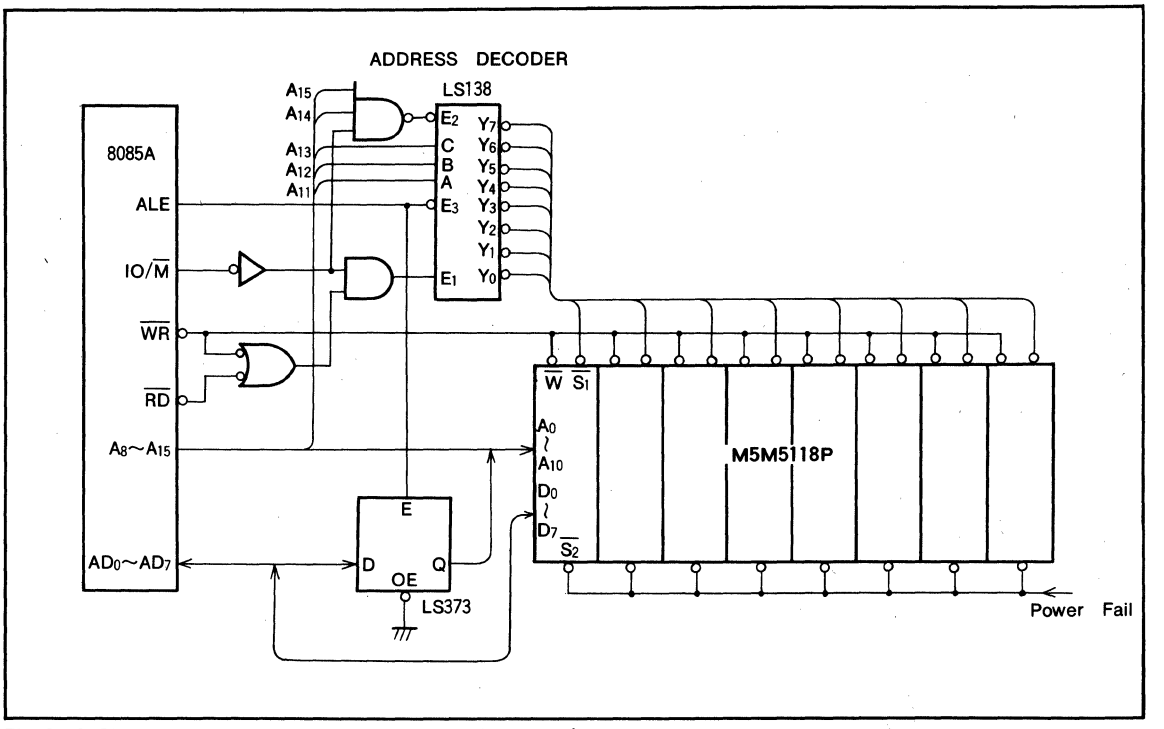



**Fig. 2.14 Circuit diagram for preventing data bus contention (Application circuit of M5M5118P)**

## 3. Precaution against Noise

When memories which have power saving function by chip selection shift from standby mode to operation mode, the supply current shows a change of several 10mA. In the read cycle, the discharging and charging currents for the output load capacitance run as peak currents to $V_{CC}$ and GND. The current increases with the number of output terminals, hence, for a static RAM of x8 structure, the current is considerable. Fig. 2.15 shows the supply current waveform of the M5M5165P. Noises generated by large current changes narrow operating margins or induce faulty operation. Less consideration has been give to SRAM compared to DRAM in the past. Now, due to its considerable improvement on speed, SRAM has become susceptible to noise. Adequate consideration, therefore, must be given to the pattern design of the circuit board. To absorb noise, a 0.1$\mu$F ceramic capacitor is recommended to be placed between each device.

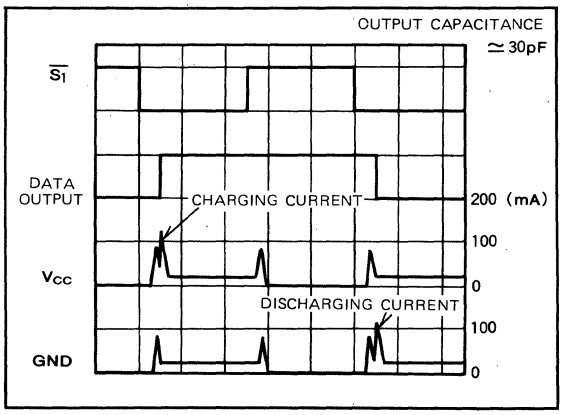



**Fig. 2.15 Waveform of supply current (M5M5165P)**

## APPLICATION OF CMOS RAM

### 1. Power Down Characteristics

The conditions that set supply current in the standby state are different from product to product. Fig. 2.16 shows differences of input circuits. M5M5116P has two chip select inputs with the power saving function which is assigned only to $\overline{S_2}$. When $\overline{S_2}$ is set to $V_{CC}$ level, the minimum standby is obtained. But $\overline{S_2}$ is not set to $V_{CC}$ level penitrate current runs into the first stage inverter of the $\overline{S_2}$ input buffer, as shown in Fig. 2.17. Therefore, in the case of system power failure, $\overline{S_2}$ must quickly be set to the $V_{CC}$ level to prevent the penitrate current and accompanied faulty operation. For the other inputs, there are no limitations on the input level, because all of the other input circuits are controlled by $\overline{S_2}$.

M5M5118P has two chip select inputs, $\overline{S_1}$ and $\overline{S_2}$, and when either of them is set to the $V_{CC}$ level, the device is set in the complete standby state.

The M5M5165P has two chip select inputs, $\overline{S_1}$ and $S_2$, both of which have the power-cut function. As the input circuit of $\overline{S_1}$ is controlled by $S_2$, the circuit is in the complete standby state when $S_2$ = GND. But when $\overline{S_1}$ = $V_{CC}$, $S_2$ must be set to the GND level to accomplish the complete standby state. The distribution of standby current is shown in Fig. 2.18. The standby current of the full CMOS RAM is so small that it enables a very long battery backup operation. (several 100nA) On the other hand, the current of the mixed CMOS RAM (NMOS cell + CMOS periferal) is fairly large (several 10μA). But, it can support battery back operation for the short term. The chois is made according to purpose and application.

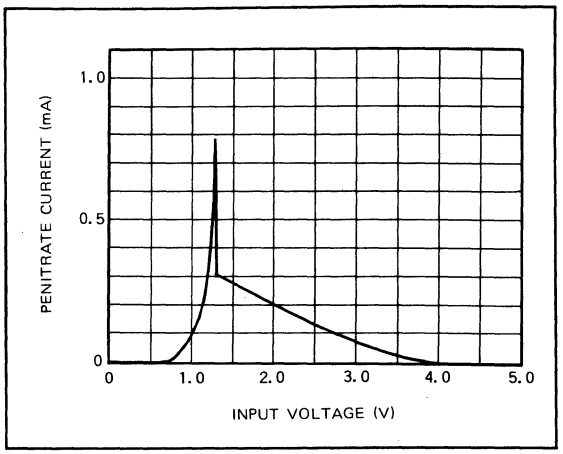



**Fig. 2.17 Penitrate current of CMOS inverter**

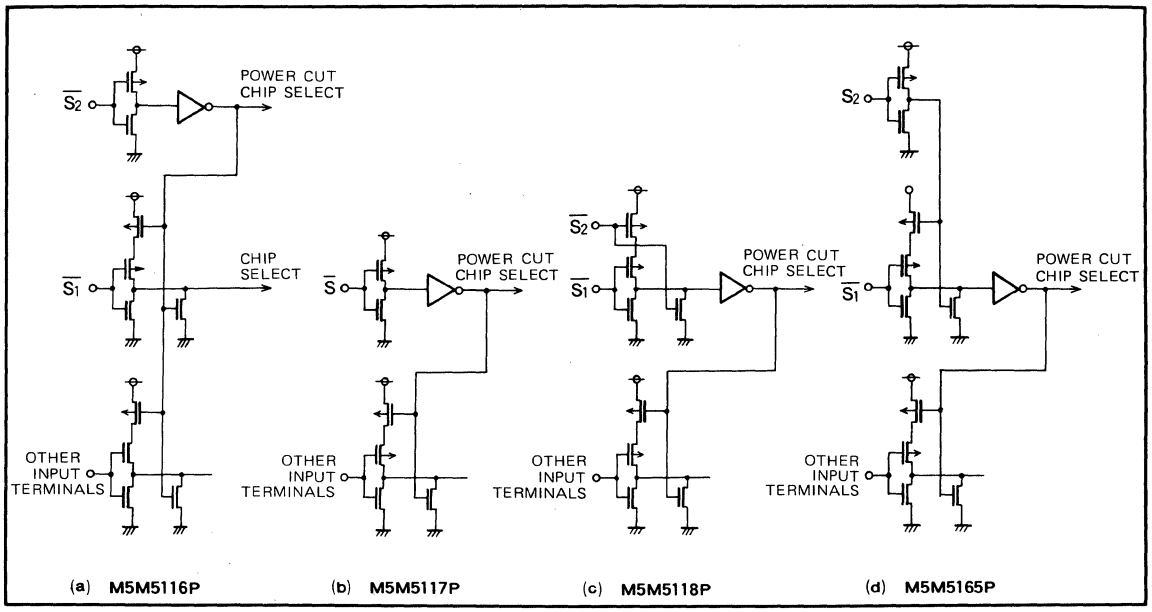



**Fig. 2.16 Difference of input circuits**

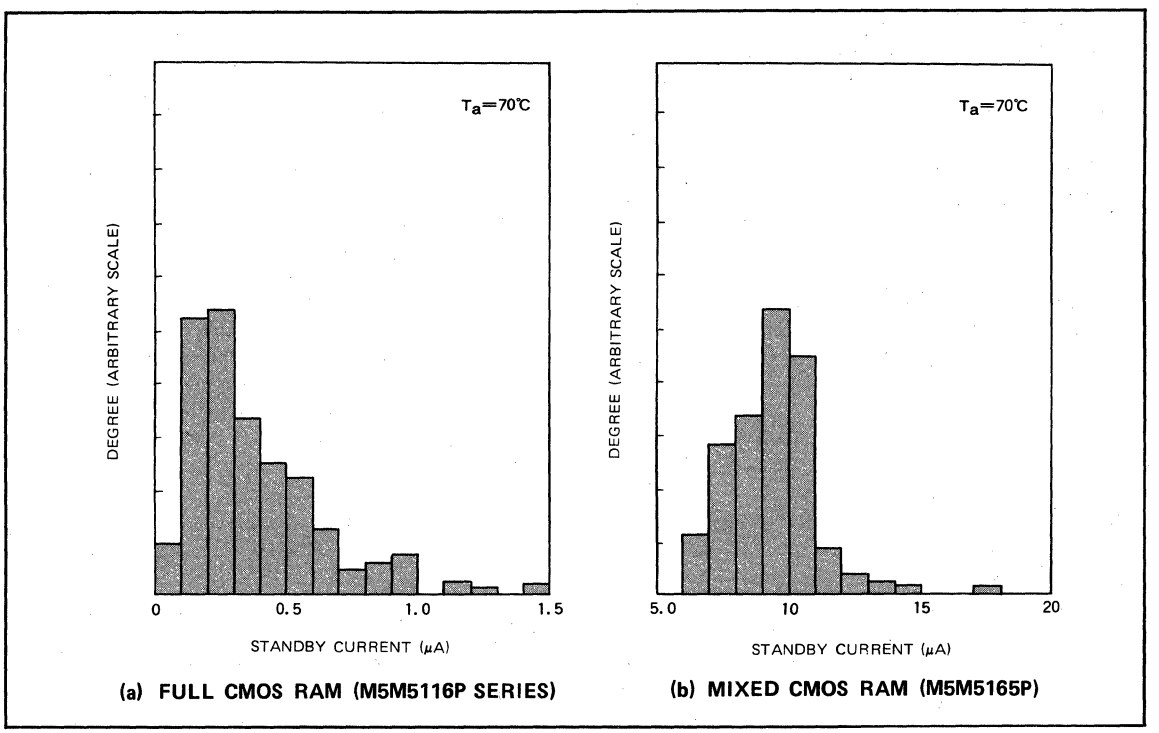



**Fig. 2.18 Distribution of standby current**

## NON-VOLATILE MEMORY SYSTEM

We can relatively easily design a large non-volatile memory system with little additional interface logic by using CMOS RAMs. The block diagram of a basic computer system that uses CMOS RAMs is shown in Fig. 2.19, and the power supply on-off timing of the system are shown in Fig. 2.20. It is usually necessary to have advanced warning that AC power has been lost. This warning signal produced by the power-fail-detect circuit interrupts the processor, which stores the volatile data in the non-volatile area (CMOS RAMs) before the system's DC source drops. And after the RAMs have been protected, their $V_{CC}$ power source is replaced by $V_{BAT}$, as shown in Fig. 2.20.

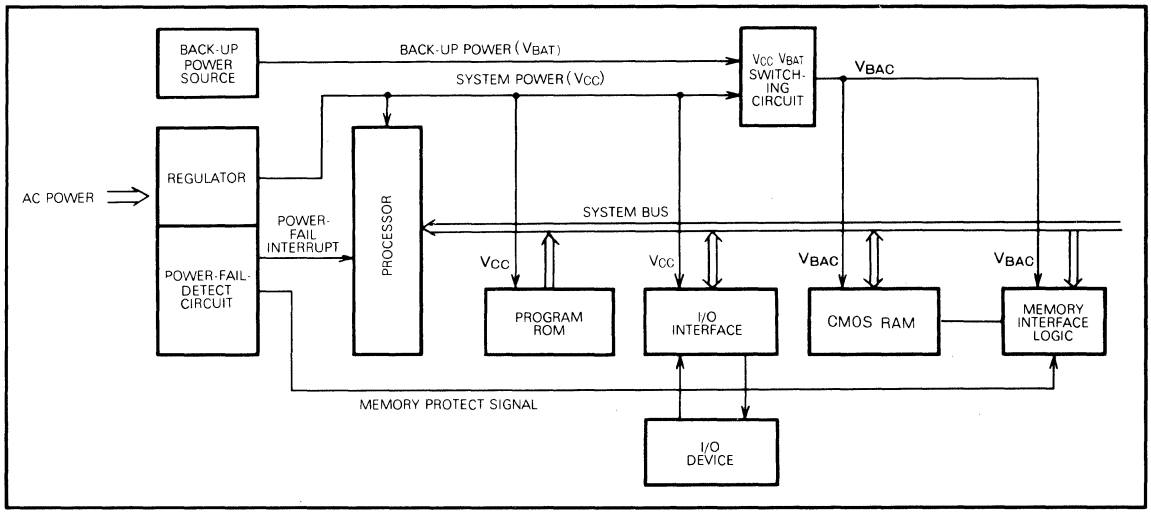



**Fig. 2.19 Non-volatile memory system**

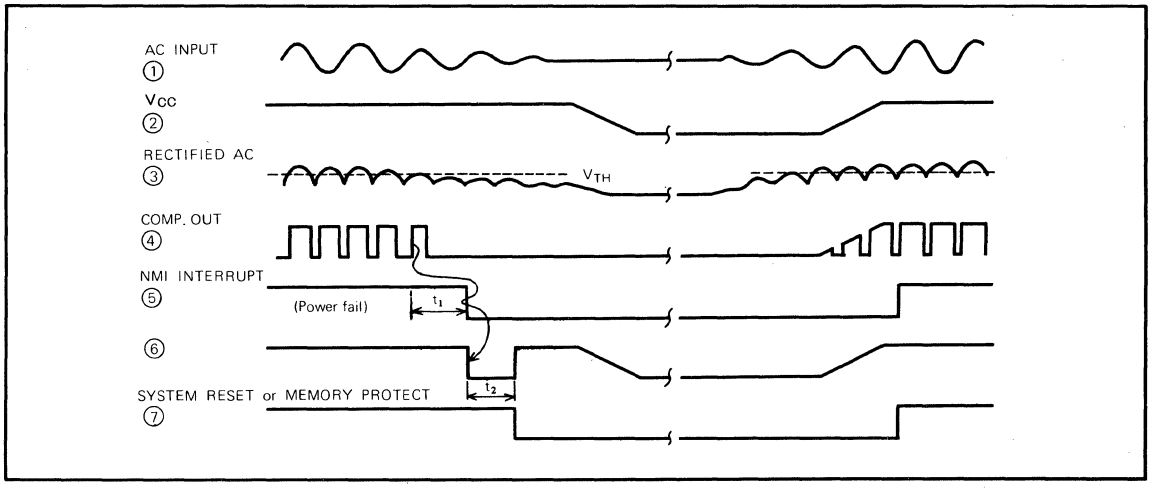



**Fig. 2.20 Power on-off timing**

## EXAMPLE OF CMOS NON-VOLATILE MEMORY SYSTEM

### Power-Failure Detection

The power-fail-detect circuit watches a separate power supply point to provide an advanced warning of power failure. As described before, this warning signal (power fail) can interrup the processor or merely protect the CMOS RAMs.

Fig. 2.23 is a simplified diagram of the power-fail-detect circuit. This shows that the power failure is detected from the secondary transformer output, which is not regulated. The Zener-diode voltage and RC time constant should be well selected to prevent AC power failure from shutting down the memory system.

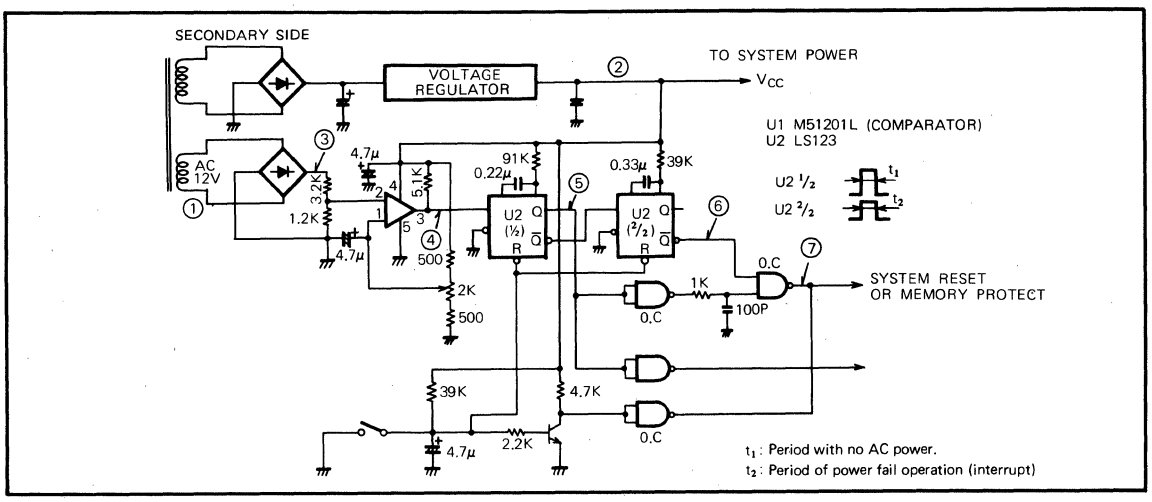



**Fig. 2.21 Power-fail-detect circuit**

### Power-Switching Circuit

The power-switching circuit replaces the main source $V_{CC}$ by the back-up power source $V_{BAT}$ when $V_{CC}$ drops, and replaces the $V_{BAT}$ by the $V_{CC}$ when the $V_{CC}$ voltage rises enough to enable normal operation.

Two types of power-switching circuit are shown in Fig. 2.22 and Fig. 2.23. The diode-coupled circuit in Fig. 2.22 requires the main DC supply $V_{CC}$ to be above the required $V_{BAC}$ voltage by the amount of drop through the diode (about 0.6 ~ 0.7V). Fig. 2.23 shows a transistor-coupled circuit, which has better performance than the circuit in Fig. 4. In this case it is recommended to use a transistor with low collector-base saturation for Q1.

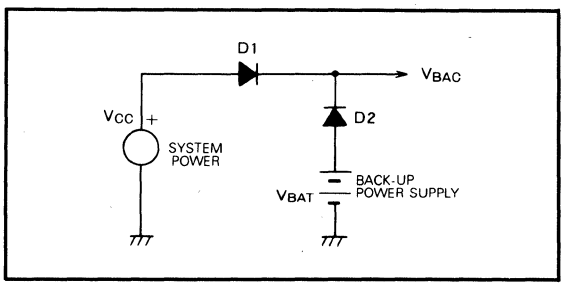



**Fig. 2.22 Diode-coupled switching circuit**

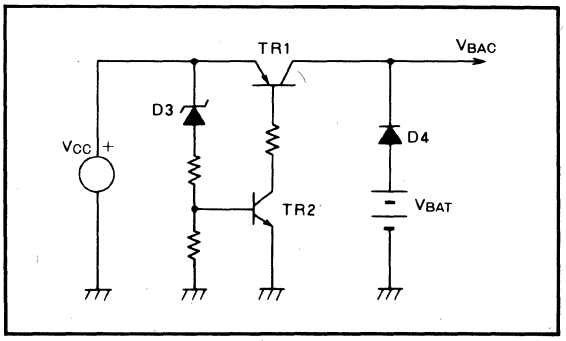



**Fig. 2.23 Transistor-coupled switching circuit**

## 4. Application Circuits

Fig. 2.24 shows an example of a non-volatile memory system using 64K bits CMOS RAM M5M5165P.

In this case, the memory protect signal is detected from the system power supply $V_{CC}$. However it is safer to protect the memory by taking the signal out of the non-regulated power supply, as shown in Fig. 2.21. Because protection is excuted before the fall of $V_{CC}$ and reset after the rise of $V_{CC}$.

### [Bit Map]

To make the best use of a test pattern or to do a failure analysis, it is necessary to know the relationship between external address and the actual cell location inside the chips. In such a case, a bit map is used to know the topology of the memory array. Figs. 2.25 ~ 2.29 show the bit maps of all static RAMS which are in production.

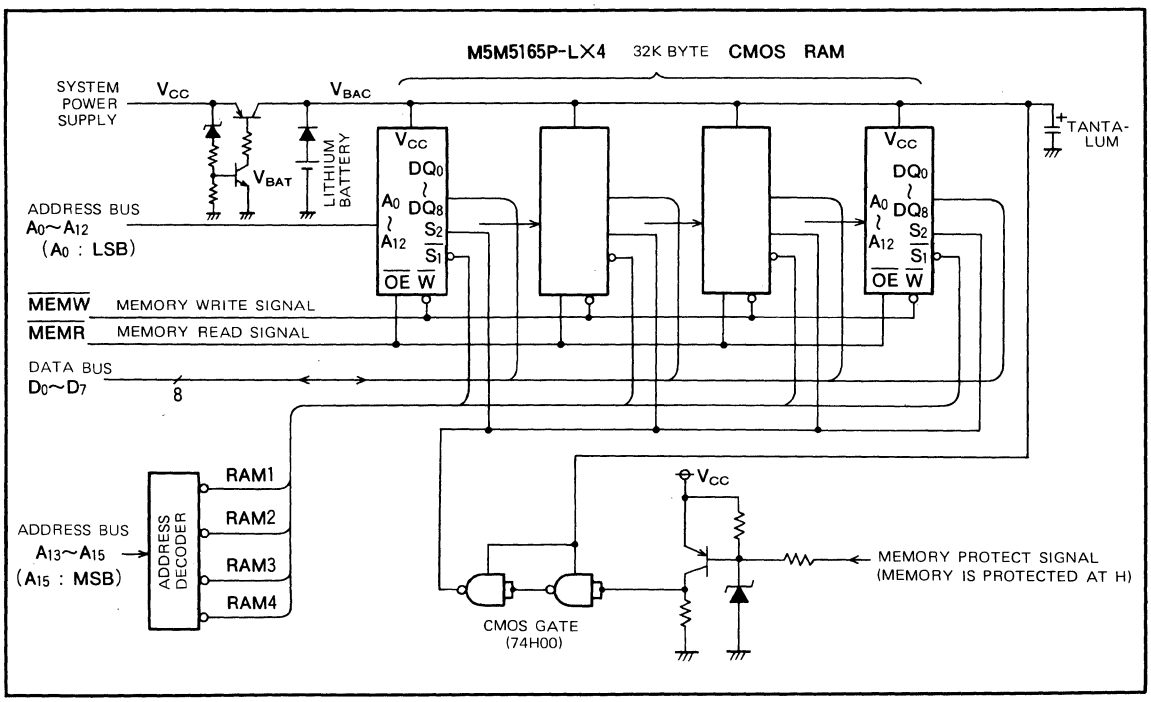



**Fig. 2.24 Application of non-volatile CMOS Memory**

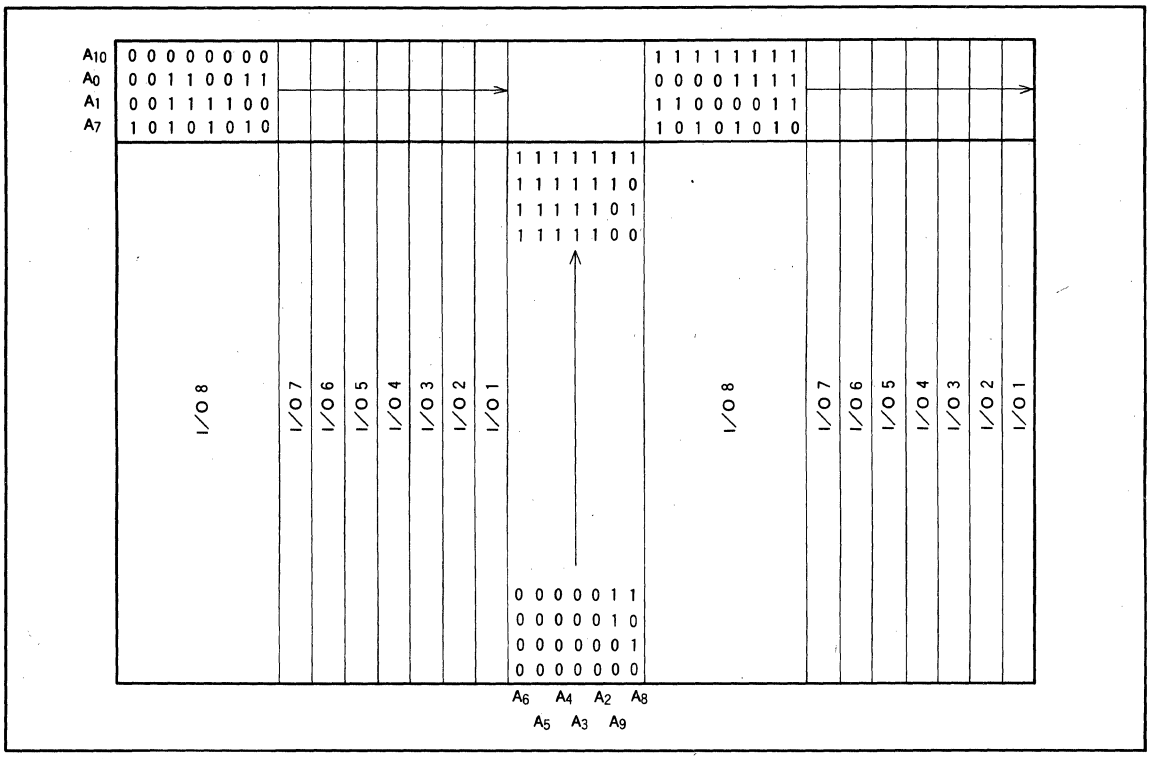



Fig. 2.25 M58725P

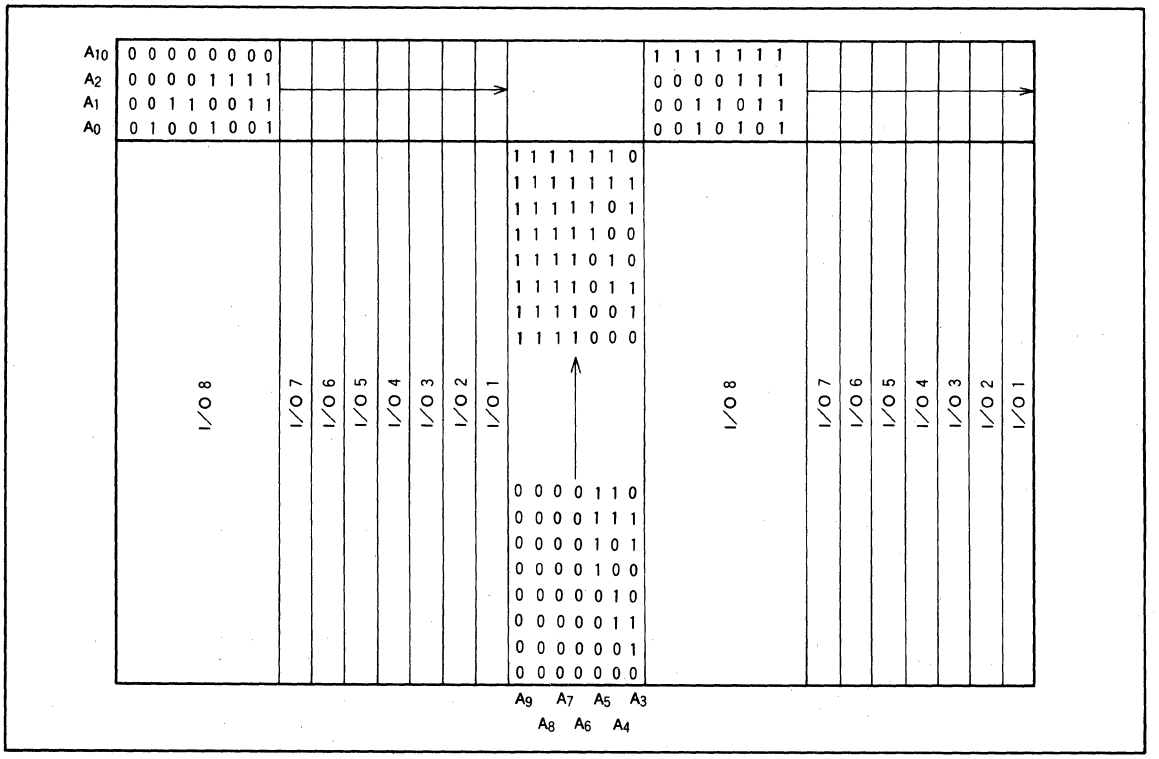



Fig. 2.26 M5M5116P/M5M5117P/M5M5118P



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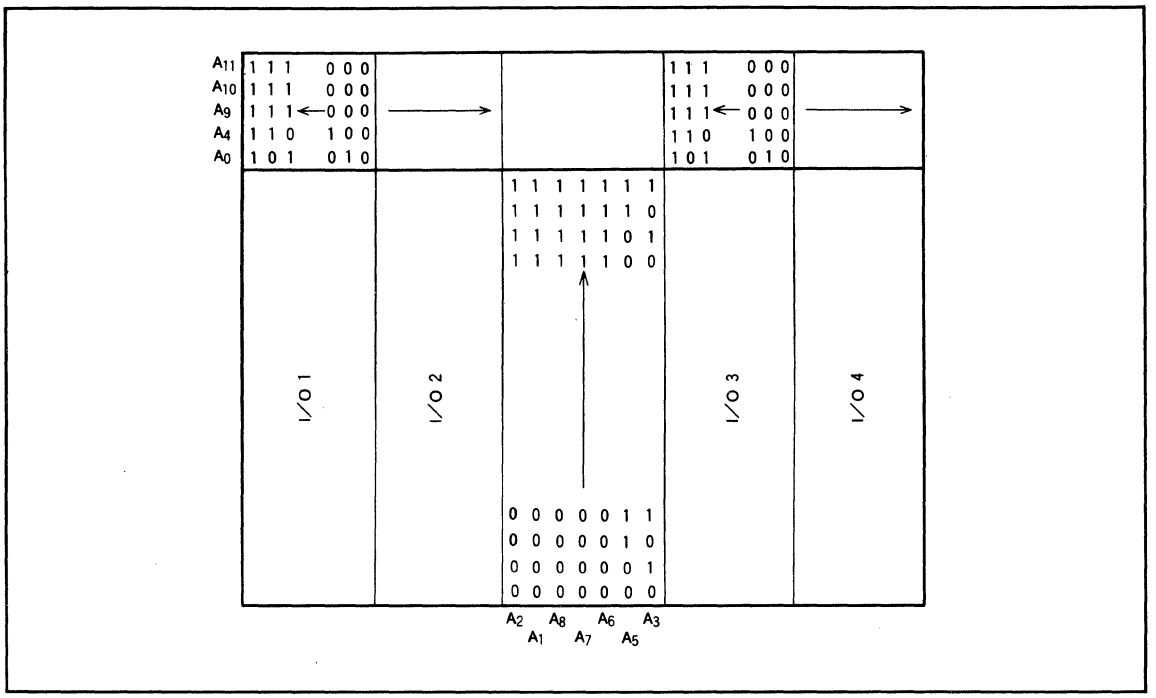



Fig. 2.27 M5M2168S

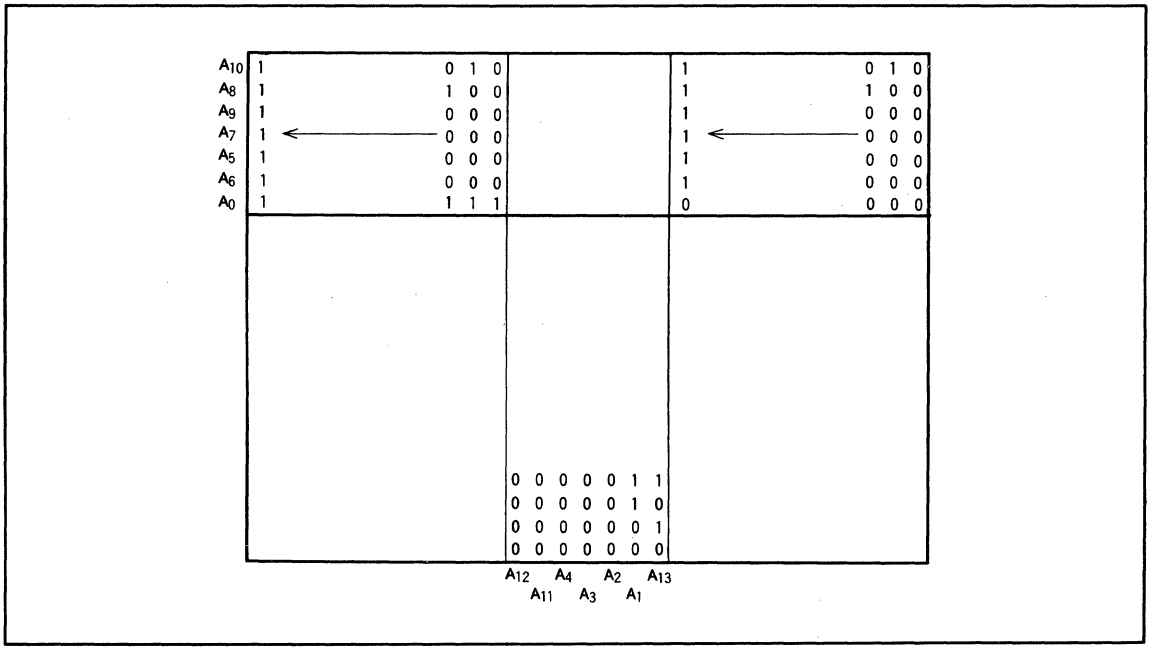



Fig. 2.28 M5M2167S

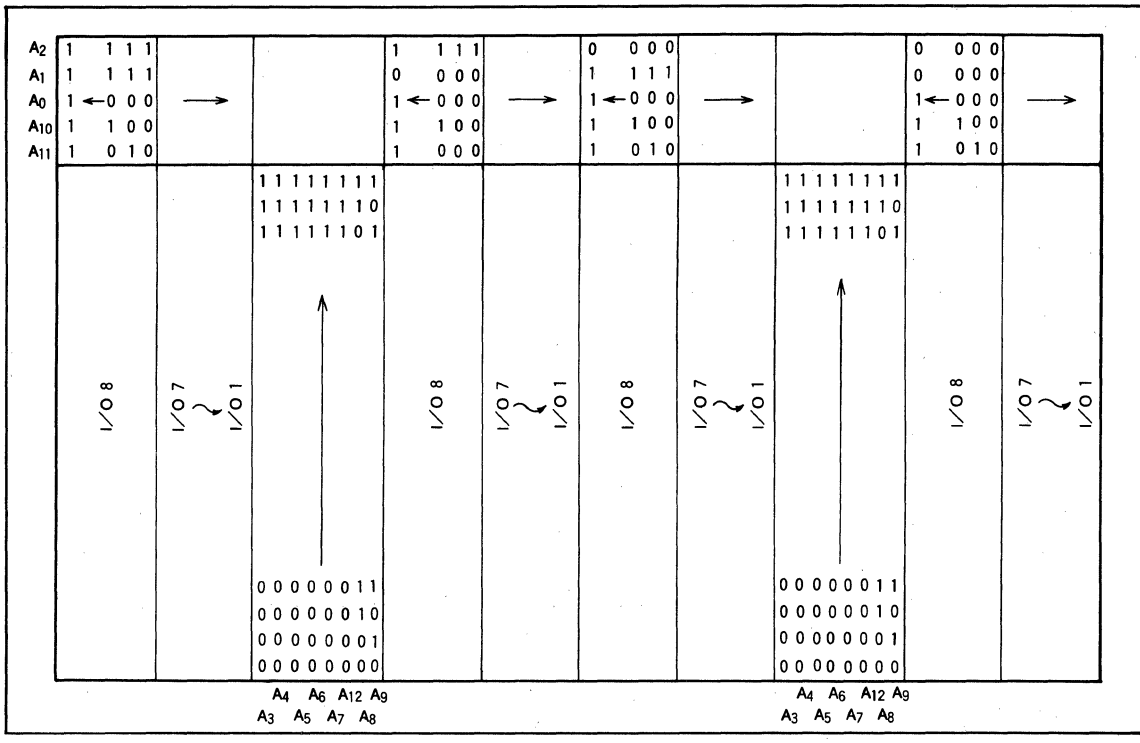



Fig. 2.29 M5M5165P

# 3. EPROM

## 3.1 EPROM Technology

### INTRODUCTION

With their ability to be electrically programmed and erased with ultraviolet light, EPROM (Erasable and Programmable Read Only Memory) devices have achieved high popularity for their ease-of-use and are retaining their position as the target for memory development.

Although the EPROM was originally developed for use as a microprocessor system debugging ROM, the device has undergone significant improvements in density, reliability, and basic process technology as well as cost per bit which have extended its usefulness beyond microprocessors into such equipment as cash registers, point-of-sale equipment, household appliances, entertainment equipment, and a variety of other fields. Since the introduction by Mitsubishi Electric of a p-channel 2K-bit EPROM, the development of n-channel devices has enabled remarkable improvements in access time, and density in the form of an 8K-bit device. The market is now being supplied with easy-to-use, single-power supply 16K/32K bit devices and high-speed, large capacity 64K/128K bit devices. This section will briefly outline the progress made in EPROM technology including a description of circuit configuration and notes on applications.

**The Structure and Basic Operation of a Memory Transistor**

As shown in Fig. 3.1, increasing EPROM capacity has been accompanied by changes in the memory transistor structure. The 2K-bit device made use of a P-channel MOS transistor to form an insulated single-layer polysilicon floating gate. In contrast to this, devices of 8K-bit capacity and greater make use of n-channel transistors and two-layer gate structure with a control gate to which a voltage may be applied placed over the floating gate. A capacitance between the control gate and the floating gate form an acceleration field for electron injection to the floating gate. Programming is performed in the following manner. For programming operations a high voltage is applied to the drain and control gate. By virtue of the control gate, capacitance between control gate and floating gate a channel is formed between the source and drain through which a current flows. As a result, for high drain voltages current induced breakdown occurs. The hot-electrons produced as a result of this breakdown phenomena exceed the high energy barrier and are injected into the floating gate. By imparting a voltage to these injected electrons the control gate can have higher threshold voltage than before injection (refer to Fig. 3.2), and the read voltage may be applied to the control gate while maintaining an open circuit. This ends the write operation. This applies to the memory transistors used in presently available EPROM devices of 8K-bit capacity and over. Fig. 3.3 shows the programming characteristics (dependency of the threshold value on the write pulse width) for 16K- and 32K-bit memory transistors.

The injected charge is located on the floating gate which is surrounded by a 1,000Å thick silicon oxide layer of good insulating characteristics, and is therefore retained for a long period. It is the retention of this charge which holds the written data. A significant feature of two-layer gate structure is the associated increase in density. As shown in Fig. 3.1, whereas in the single-layer gate an additional row selection transistor is required, the two-layer memory transistor eliminates this necessity by having the control gate serve two functions.

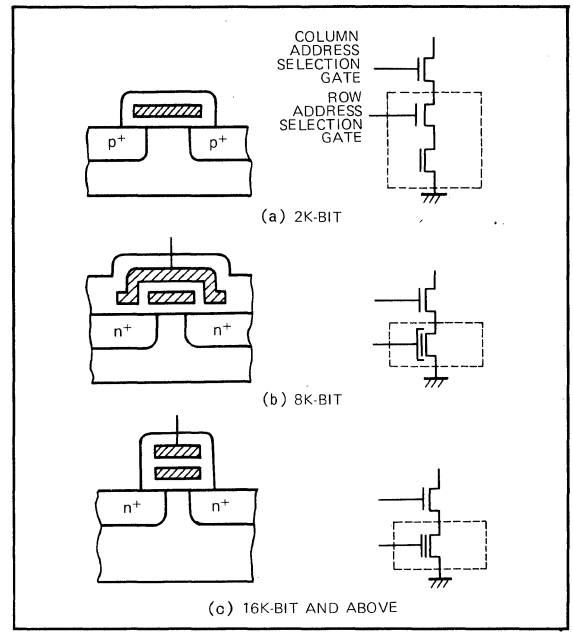



**Fig. 3.1 Memory transistor construction**

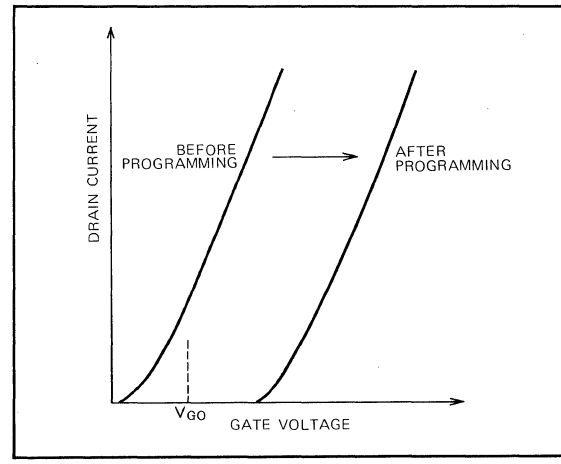



**Fig. 3.2 Variation in memory transistor threshold voltage ($V_{GO}$: Read gate voltage, both vertical and horizontal scales are arbitrary)**

The introduction of 8K- and 16K-bit devices and greater was accompanied by improvements of control gate structure. As shown in Fig. 3.1, whereas for the 8K-bit device the side of the folating gate is completely covered by the control gate, this is not true of devices of 16K-bit capacity and greater. It should be noted that while significant improvements in overall capacity has been made, chip size remains essentially unchanged, the 16K-bit chip size being merely 8.2% greater than that for the 8K-bit device. These devices have been improved to the 64K/128K bit devices by decreasing the chip size vertically and horizontally.

Erasing is done by exposing the device to ultraviolet light. The electrons on the floating gate receive the ultraviolet energy, pass through the oxide layer and escape. The transmittivity of ultraviolet radiation from a low pressure mercury lamp through polysilicon is low compared to silicon oxide. For this reason, the ultraviolet energy reaching the floating gate of 16K-bit and greater memory devices using transistors without polysilicon sides is larger than the 8K-bit structure. This results in shorter erase times for 16K-bit devices and over. Fig. 3.4 illustrates the change in threshold value by exposure of ultraviolet energy.

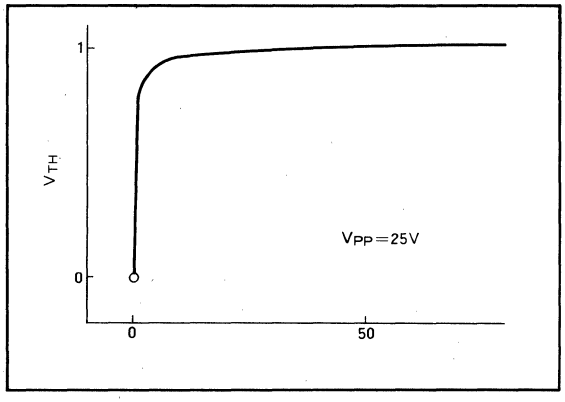



**Fig. 3.3 Dependency of $V_{TH}$ on write pulse width (16K-bit and 32K-bit)**

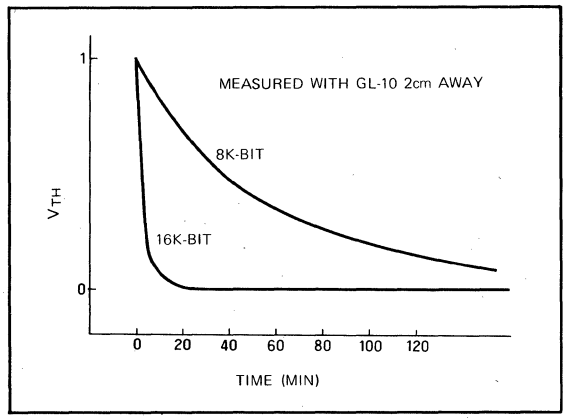



**Fig. 3.4 Variation in $V_{TH}$ with erasure time**

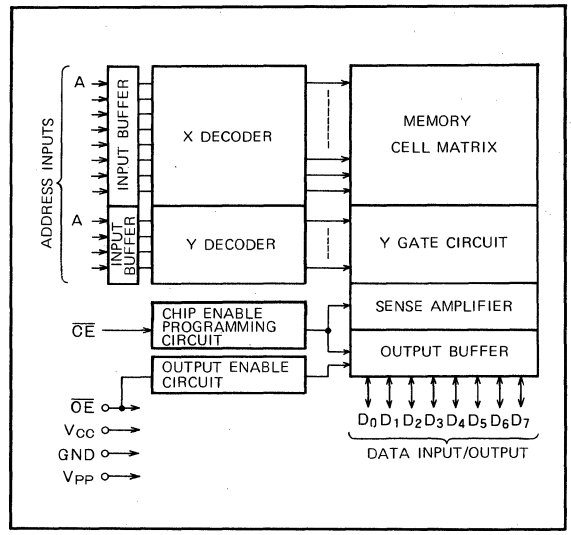



**Fig. 3.5 EPROM Block diagram**

### EPROM Circuit Configuration and Characteristics

#### Circuit Configuration

Fig. 3.5 shows the block diagram of an ultraviolet light erasable EPROM. Currently available devices are configured in 8-bit words with the memory cells arranged in eight blocks. Input and output is performed in parallel by means of the signal lines $D_0 \sim D_7$ connected to these eight blocks. The address signals are divided into column decoder inputs and row decoder inputs. For a 128K-bit EPROM, five address signals are input to the column decoder while nine address signals are input to the row decoder, the memory being arranged as a matrix of $2^5$ (=32) columns by $2^9$ (=512) rows.

After decoding, the column signals are input to the column selection transistor gate which is connected to the memory cell drain. Finally, the decoder row inputs are connected to the memory control gates. Sense amplifiers and data input/output buffers used in read and program operations are connected to the drains (data lines) of the memory cells controlled by the column selector transistors. Almost all of the chip area is taken up by the memory cells, address circuits, decoders, and data circuits, the remaining area being allotted to the important control circuits.

These control circuits consist of the chip enable and output enable circuits. The former controls the power down operation or programming operations. The latter circuit controls the enabling or disabling of the output signal by means of the OEsignal. 16K-bit devices and over are provided with these two select/unselect control circuits. The two line control method is very effective for OR-connecting of multiple devices. If only one signal were allowed to control chip select and unselect, cases could arise where one chip is enabled for output before the previous chip goes into the floating state.

As shown in Fig. 3.6, this results in excessive current flowing and the generation of power supply noise. In addition, data on the bus is unstable before and after address changes. This condition is called "the bus contention problem" and can be eliminated by using the $\overline{CE}$ as the chip enable and $\overline{OE}$ as the output enable signal in a two-line control mode.

**EPROM Operation, Characteristics, and Application Notes.**

The basic operations possible with an EPROM are programming, read, and erase. These operations will be discussed with respect to 16K- and 32K-bit devices along with some precautions for use. Table 1 summarizes a comparison of the characteristics of EPROM devices currently available.

**(1) Programming Operations**

The normal state of all cells for an EPROM device when shipped or after erasure is "1", programming operations change the memory cell contents to 0. Programming operations are performed in groups of 8 bits (one word). After applying the programming voltage to the programming pin and selecting the program mode, the address data is set up. Next, a programming pulse of the required width is input. The active state of this pulse depends on the device (for instance, for 16K-bit devices the pulse is active high while for 32K, 64K and 128K-bit devices it is active low), so that care should be taken when generating this pulse. Although it is often thought that the higher the programming voltage and the wider the programming pulse, the more effective the programming operation will be, the device characteristics dictate that the best programming will be achieved by setting these values to the central specification values. In perticular, the maximum allowable voltage for programming that may be applied to the $V_{pp}$ pin is 26V. Care must be taken that the $V_{pp}$ supply doesn't overshoot the 26-volt maximum specification. Programming for both 16K- and 32K-bit devices can be performed in any arbitrary order, further simplifying the programming operation.

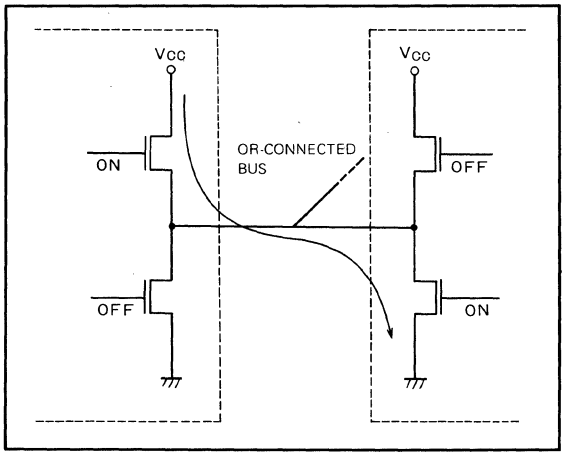



**Fig. 3.6 Fighting for an OR-connected bus**

**Table 3.1 Comparison of Available EPROM Devices**

| MEMORY CAPACITY (BITS) | 2K (256×8) | 3K (1024×8) | 16K (2048×8) | 32K (4096×8) |
|---|---|---|---|---|
| TYPE | M5L1702AS | M5L2708K | M5L2716K | M5L2732K |
| CHANNEL TYPE | p | n | n | n |
| CHIP AREA | 14.2mm² | 17.8mm² | 19.3mm² | 22.5mm² |
| ADDRESS ACCESS TIME (MAX) | 1000ns | 450ns | 450ns | 450ns |
| POWER DISSIPATION (MAX) | 600mW | 800mW | 525mW | 787mW |
| POWER DISSIPATION PER BIT | 0.3mW | 0.1mW | 0.03mW | 0.02mW |
| SUPPLY VOLTAGES | +5, −9V | +5, −5, +12V | +5V | +5V |

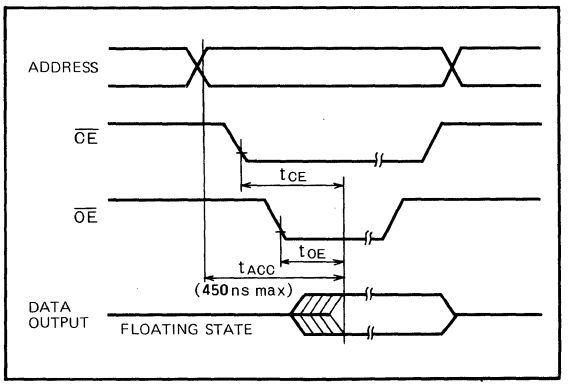



**Fig. 3.7 Read timing diagram**

**(2) Read Operation**

The read mode is enabled by lowering the program voltage and using the chip enable signal to select the chip, and the output control signal to enable the output of the memory contents at the selected address. The chip enable signal serves also as the power down signal, enabling an extreme limitation on power consumption for the non-selected periods. Access time is specified in terms of chip enable, address, and output enable access times, the power down feature making the chip enable access time generally the longest. Operating conditions and output timing should be carefully considered as high temperatures and excessive output loads have an adverse affect on access time. Fig. 3.7 shows the read timing for 16K-bit and 32K-bit devices with Fig. 3.8 and Fig. 3.9 giving the chip enable access time dependency on temperature and load capacitance.

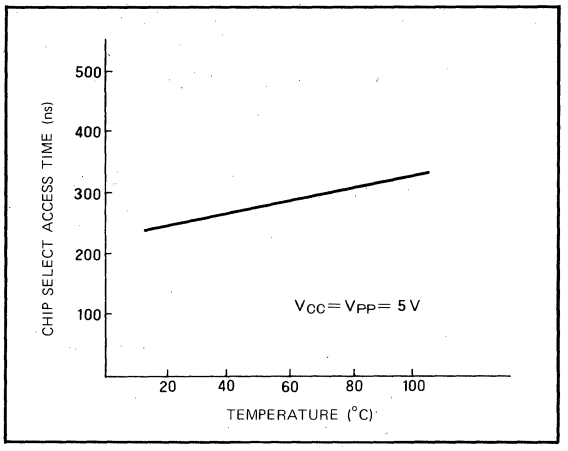



**Fig. 3.8 2716 Chip select access time temperature characteristics example**

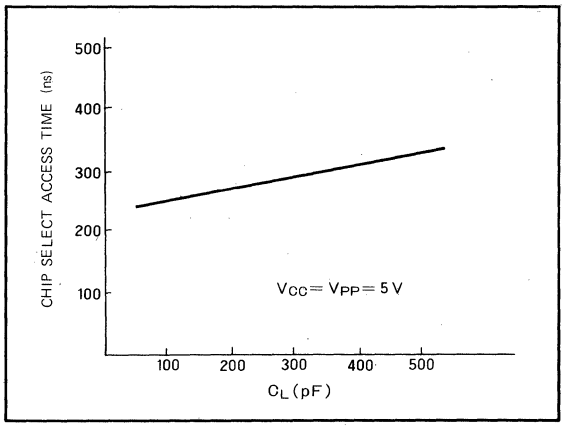



**Fig. 3.9 2716 Chip select access time load capacitance dependency**

**(3) Erasure**

Erasure is performed by exposing the chip to ultraviolet light. Fig. 3.4 shows the change in memory transistor threshold value with relationship to ultraviolet radiation. The erasure time should be selected to allow for variations in the memory transistor characteristics. Fig. 3.10 shows the relationship between the ultraviolet radiation time and the number of bits erased. Verification of erasure by means of a PROM programmer should not be assumed to indicate that the EPROM is sufficiently erased. While the required erasure time depends upon factors such as the type and condition of the lamp used and the distance to the device being erased, the actual erasure procedure should be continued for a period of five times the time required to erase all cells as verified by a PROM programmer. Generally, for 16K- and 32K-bit EPROMs, the erasure time for a GL-10 lamp 2.5cm away from the device is between 15 and 20 minutes.

The erasure characteristics for 8K-bit EPROMs differs from those for 16K-bit and greater capacity for structural reasons, with the differences extending to the degree of influence of sunlight and fluorescent lighting on the inadvertent erasure of data. To prevent such long term ambient radiation from affecting electrical characteristics, the use of a seal to cut out such radiation for normal use is required.

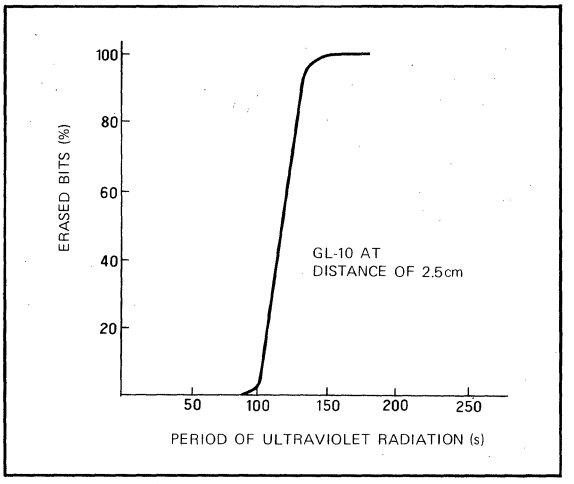



**Fig. 3.10 Erasure characteristics example for 2716 and 2732**

## 3.2 APPLICATION OF EPROMS

**EPROM control functions**

EPROM control functions are provided to simplify interface and allow full utilization of performance. A new generation of dual-control function EPROMs has become popular which has both a chip enable ($\overline{CE}$) and an output enable ($\overline{OE}$) control input.

$\overline{CE}$ (Chip Enable, active low)

The falling edge of $\overline{CE}$ activates the address input buffers and latches the address in preparation for the address decoders and the sense amplifiers to perform their function. This acts also as a power control function, allowing the device to enter a low-power standby mode when the $\overline{CE}$ input is disabled.

$\overline{OE}$ (Output Enable, active low)

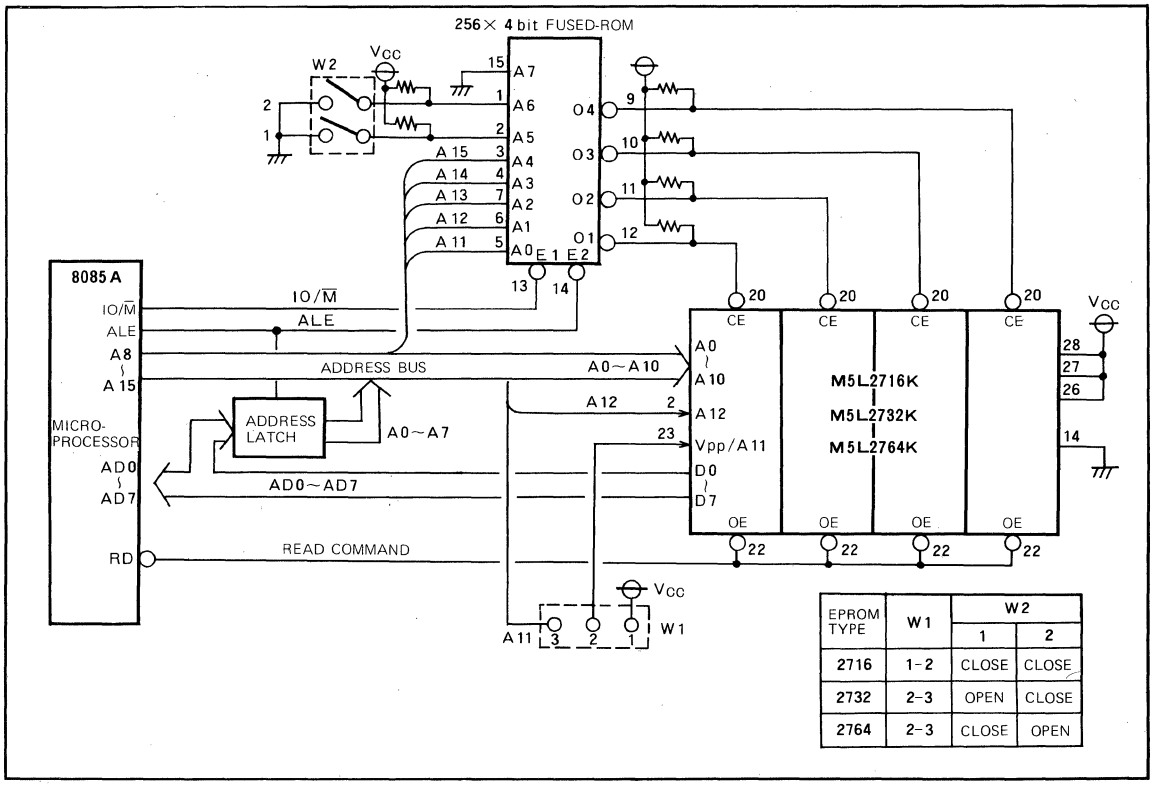
OE controls the device's output buffer, and is used to avoid bus contention since the device's output can be turned on and off directly by the processor. The $\overline{CE}$ and $\overline{OE}$ control functions are ANDed inside the device. This means that only the simultaneous application of $\overline{CE}$ and $\overline{OE}$ will activate the output of the device. (When either of $\overline{CE}$ or $\overline{OE}$ is not active, the output buffer of the device goes into the high-impedence state.)

**Microprocessor interface**

As described above, EPROMs can be interfaced easily to microprocessors using the $\overline{CE}$ and $\overline{OE}$ functions. A typical example is shown in Fig. 3.11. The address from the microprocessor is decoded by the bipolar PROM which generates the primary decoded signal $\overline{CE}$. Next, read memory command from the microprocessor enables $\overline{OE}$. This decoding method makes possible a substantial power saving.

**EPROM package compatibility and design technique**

As the density of EPROMs increase, more address pins will be needed for higher density devices. But the EPROM family has similar pin configurations maintain which keeps the compatibility with each memory size devices. The pinouts of the family are shown in Fig. 3.12 which have different signals at the dotted pinouts only. It may seem as though the 28-pin package is not compatible with the 24-pin devices, but the lower 24 pins are indential to the 24-pin package of 2716 or 2732 as shown in Fig. 3.12.

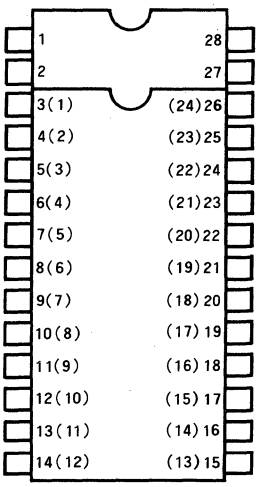



| EPROM TYPE | W1 | W2 | |
|---|---|---|---|
| | | 1 | 2 |
| 2716 | 1-2 | CLOSE | CLOSE |
| 2732 | 2-3 | OPEN | CLOSE |
| 2764 | 2-3 | CLOSE | OPEN |

Fig. 3.11 Microprocessor-EPROM interface example

The pinouts of the EPROM family enable the memory design to support 2K-, 4K-, and 8K-byte EPROMs, which require some techniques of address decoding and print circuit board layout. Fig. 3.11 shows now the EPROM family may be connected to the very popular M5L8085A microprocessor. The high-order microprocessor address bits are fed to a 256x4 bipolar PROM for address spatial decoding. The PROM allows the address space to be re-defined at any time so that various EPROMs can be used. The jumpers W1 and W2 are used to define the type of EPROM according to the table in Fig. 3.11. The address map of the PROM is shown in Table 3.2.

| 2764 | 2732 | 2716 |
|---|---|---|
| $V_{PP}$ | | |
| $A_{12}$ | | |
| $A_7$ | $A_7$ | $A_7$ |
| $A_6$ | $A_6$ | $A_6$ |
| $A_5$ | $A_5$ | $A_5$ |
| $A_4$ | $A_4$ | $A_4$ |
| $A_3$ | $A_3$ | $A_3$ |
| $A_2$ | $A_2$ | $A_2$ |
| $A_1$ | $A_1$ | $A_1$ |
| $A_0$ | $A_0$ | $A_0$ |
| $D_0$ | $D_0$ | $D_0$ |
| $D_1$ | $D_1$ | $D_1$ |
| $D_2$ | $D_2$ | $D_2$ |
| GND | GND | GND |




| 2716 | 2732 | 2764 | |
|---|---|---|---|
| | | $V_{CC}$ | |
| | | $\overline{PGM}$ | |
| $V_{CC}$ | $V_{CC}$ | NC | |
| $A_8$ | $A_8$ | $A_8$ | |
| $A_9$ | $A_9$ | $A_9$ | |
| $V_{PP}$ | $A_{11}$ | $A_{11}$ | * |
| $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $\overline{OE}$ | * |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | |
| $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | |
| $D_7$ | $D_7$ | $D_7$ | |
| $D_6$ | $D_6$ | $D_6$ | |
| $D_5$ | $D_5$ | $D_5$ | |
| $D_4$ | $D_4$ | $D_4$ | |
| $D_3$ | $D_3$ | $D_3$ | |

**Fig. 3.12 EPROM Family pinouts**

**Table 3.2 PROM Address Map**

| Input signal / Decoder address | GND | W2-2 | W2-1 | Microprocessor's address | | | | | Decoder outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | | | | |
| | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $O_1$ | $O_2$ | $O_3$ | $O_4$ |
| 2716 mode | 0 | 0 | 0 | △ | △ | △ | 0 | 0 | 0 | 1 | 1 | 1 |
| | | | | | | | 0 | 1 | 1 | 0 | 1 | 1 |
| | | | | | | | 1 | 0 | 1 | 1 | 0 | 1 |
| | | | | | | | 1 | 1 | 1 | 1 | 1 | 0 |
| 2732 mode | 0 | 0 | 1 | △ | △ | 0 | 0 | * | 0 | 1 | 1 | 1 |
| | | | | | | 0 | 1 | * | 1 | 0 | 1 | 1 |
| | | | | | | 1 | 0 | * | 1 | 1 | 0 | 1 |
| | | | | | | 1 | 1 | * | 1 | 1 | 1 | 0 |
| 2764 mode | 0 | 1 | 0 | △ | 0 | 0 | * | * | 0 | 1 | 1 | 1 |
| | | | | | 0 | 1 | * | * | 1 | 0 | 1 | 1 |
| | | | | | 1 | 0 | * | * | 1 | 1 | 0 | 1 |
| | | | | | 1 | 1 | * | * | 1 | 1 | 1 | 0 |
| Not used | 0 ↓ 1 | 1 ↓ 1 | 1 ↓ 1 | * ↓ 1 | * ↓ 1 | * ↓ 1 | * ↓ 1 | * ↓ 1 | 1 | 1 | 1 | 1 |

Note: * indicates 0 or 1 △ indicates 0 or 1 which defines the EPROM's page address



MITSUBISHI ELECTRIC

## Functional description of M5L8041A-006P

### General

M5L8041A-006P is a slave computer LSI which is designed for EPROM writer control using a mask-programmed M5L8041A-XXXP. The operation mode of the PRPG is defined by the master microprocessor. So it is programmed by the system's software as an I/O peripheral.

Command description

There are 7 commands provided for programming the PRPG. These commands are sent on the data bus with the signal $\overline{CS}$ at low and the signal $A_0$ at high and are stored in the PRPG at the rising edge of the signal $\overline{WR}$.

The summary of PRPG's commands and status is shown in Table 3.3.

### PRPG Timing and interfacing

PRPG's operation timing are triggored by the commands are shown Table 3.3. There are two operation modes, 2716 mode and 2732 mode, whose timing are shown in Fig. 3.13 and Fig. 3.14.

## Application for EPROM writer

### Introduction

M5L8041A-006P is one of the applications for EPROM writer controller which can interface to microprocessors (e.g. 8080A, 8085A, 8086). EPROM writer design is simplified by using M5L8041A-006P.

Features of the M5L8041A-006P;

- EPROM write controll for the 2716 or 2732
- Fully compatible with Mitsubishi microprocessors
- Reduces the master microprocessor's program for EPROM writing.

### PRPG interface and timing

An example of PRPG interfacing is shown in Fig. 3.15. Using the PRPG, the design of the EPROM writer is simplified. M5L8243P is used for the port expander of PRPG.

PRPG's operational timing is managed by the commands shown in Table. 3.3. There are two operation modes (i.e., 2716 and 2732 mode) whose timing is shown in Fig. 3.13 and Fig. 3.14 respectively. If the mode set command is not equal to the hardware switch to select 2716 or 2732 in the Fig. 3.15, the mode will not be set and the FAIL LED will light.

### Design example of EPROM/RAM board

Fig. 3.16 presents the design example of EPROM/RAM board which is fully compatible with the proposed $IE^3$-P796 bus standard. The M5L2716K, M5L2732K or M5L2764K can be used in this board, and also 2Kx8 bit of RAM (M58725 P) can be mixed with M5L2716K.

## Table 3.3 M5L8041A-006P (PRPG) Function Table

| | COMMAND/ STATUS | DESCRIPTION | CODE | LED DISPLAY: PASS | LED DISPLAY: FAIL | NOTES |
|---|---|---|---|---|---|---|
| COMMAND | 1 Mode set | Defines the operation mode of PRPG | MSB M 0 0 0 0 0 $F_1$ $F_0$ LSB $A_0$ 1<br>EPROM Selection: 0 = 2716 Mode, 1 = 2732 Mode<br>Selection of clock input: 0 0 = 3.58 MHz, 0 1 = 4.194303 MHz, 1 0 = 6 MHz | PASS = ON<br>When mode is set correctly. (Mode request LED turns off.) | FAIL = ON<br>When programmed mode is not coincident with hardware switch. | It is necessary to provide mode set command after power on. After mode is set, the operation mode is available until the other mode is set. |
| COMMAND | 2 Address set | Defines the start address (SPA) and the end address (EPA) of programing EPROM | MSB 1 1 1 1 0 0 0 0 LSB $A_0$ 1<br>After providing Address set command, it is necessary to provide following 4 bytes of SPA and EPA continually.<br>1st byte (SPA) HIGHER 0<br>2nd byte (SPA) LOWER 0<br>3rd byte (EPA) HIGHER 0<br>4th byte (EPA) LOWER 0 | | FAIL = ON<br>1 SPA > SPB<br>2 SPA EPA<br>2716 ≧ $800_{16}$ ≧ $800_{16}$<br>2732 ≧ $1000_{16}$ ≧ $1000_{16}$ | A bytes commands after address set command should provide with A0 input low-level. |
| COMMAND | 3 Blank check | Checks the programming EPROM if it is erased. | MSB 1 0 1 1 0 0 0 0 LSB $A_0$ 1 | PASS = ON<br>If EPROM is erased. (i.e. All data are $FF_{16}$) | FAIL = ON<br>If EPROM is not erased. | |
| COMMAND | 4 EPROM write | Writes the data to the EPROM which are sent from master CPU and rerifies the written data if they are correctly programmed. | MSB 1 0 1 0 0 0 0 0 LSB $A_0$ 1<br>After providing this command, PRPG generates EPROM programming timing pulse. | PASS = ON<br>When programming finishes completely. | FAIL = ON<br>If it is not able to write correctly in the EPROM address. (SPA ~ EPA) | |
| COMMAND | 5 Verify | Checks the programmed EPROM if it is written correctly. | MSB 1 1 0 1 0 0 0 0 LSB $A_0$ 1<br>After providing this command, PRPG compares the programed data with the source data of master CPU. | PASS = ON<br>When the programed data are equal to the source data. | FAIL = ON<br>If the programed data are not equal to the source data | |
| COMMAND | 6 Automatic write | Executes the commands 3 , 4 , 5 automatically. | MSB 1 1 0 0 0 0 0 0 LSB $A_0$ 1 | PASS = ON<br>When there is no error in 3 and 5 command. | FAIL = ON<br>When there are any errors in 3 and 5 command. | |
| COMMAND | 7 Copy | Transfers the EPROM's data where are difined SCA and ECA to the master CPU. | MSB 1 1 1 0 0 0 0 0 LSB $A_0$ 1<br>After providing Copy command, it is necessary to provide following 4 bytes of SCA and ECA.<br>1st byte (SCA) HIGHER 0<br>2nd byte (SCA) LOWER 0<br>3rd byte (ECA) HIGHER 0<br>4th byte (ECA) LOWER 0 | PASS = ON<br>When data transfer finishes. | FAIL = ON<br>Same condition as command 2 | SCA = start address of copy data<br>ECA = start address of copy data |
| STATUS | 8 Write data buffer full | Indicates if write data buffer in the PRPG are full or not. | MSB – – – – – – F – LSB $A_0$ 1<br>0 PRPG data buffers: full<br>1 PRPG data buffers: not full | | | The status is used by 4 or 6 command. |

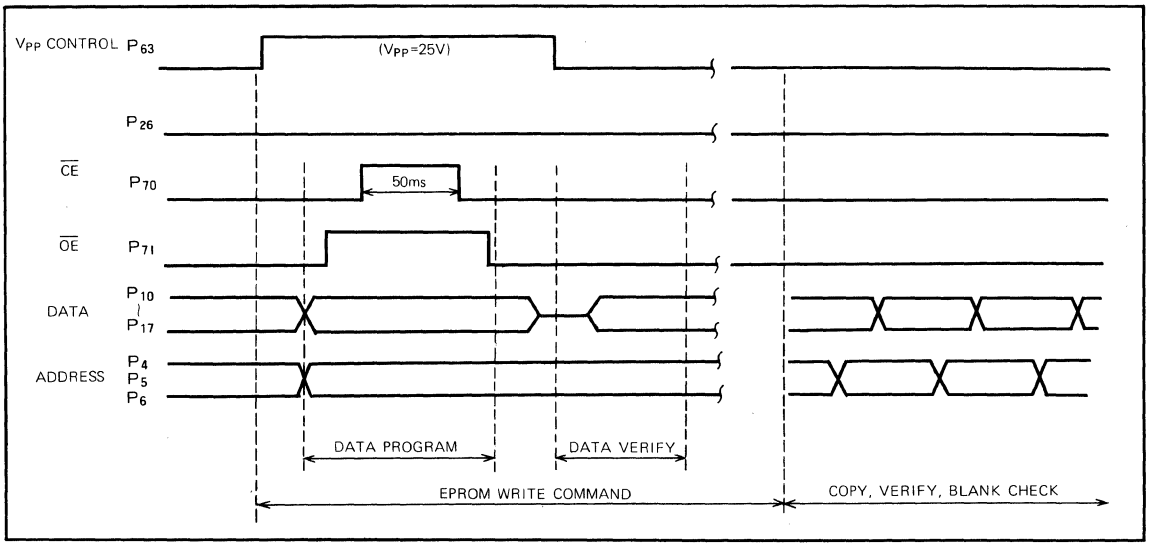



**Fig. 3.13 2716 Programming timing**

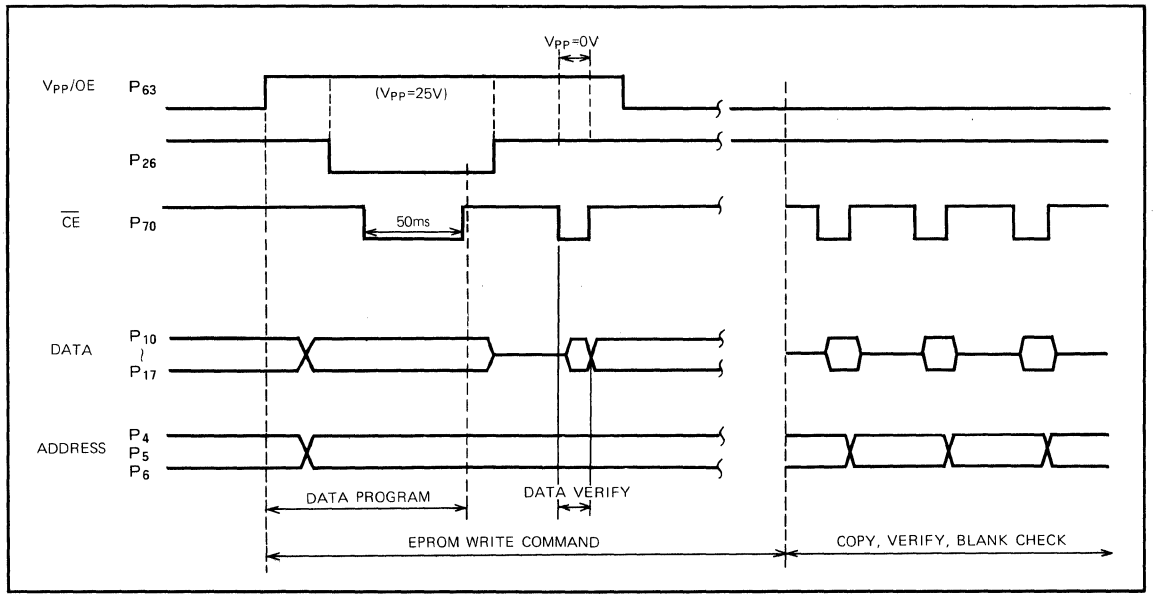



**Fig. 3.14 2732 Programming timing**

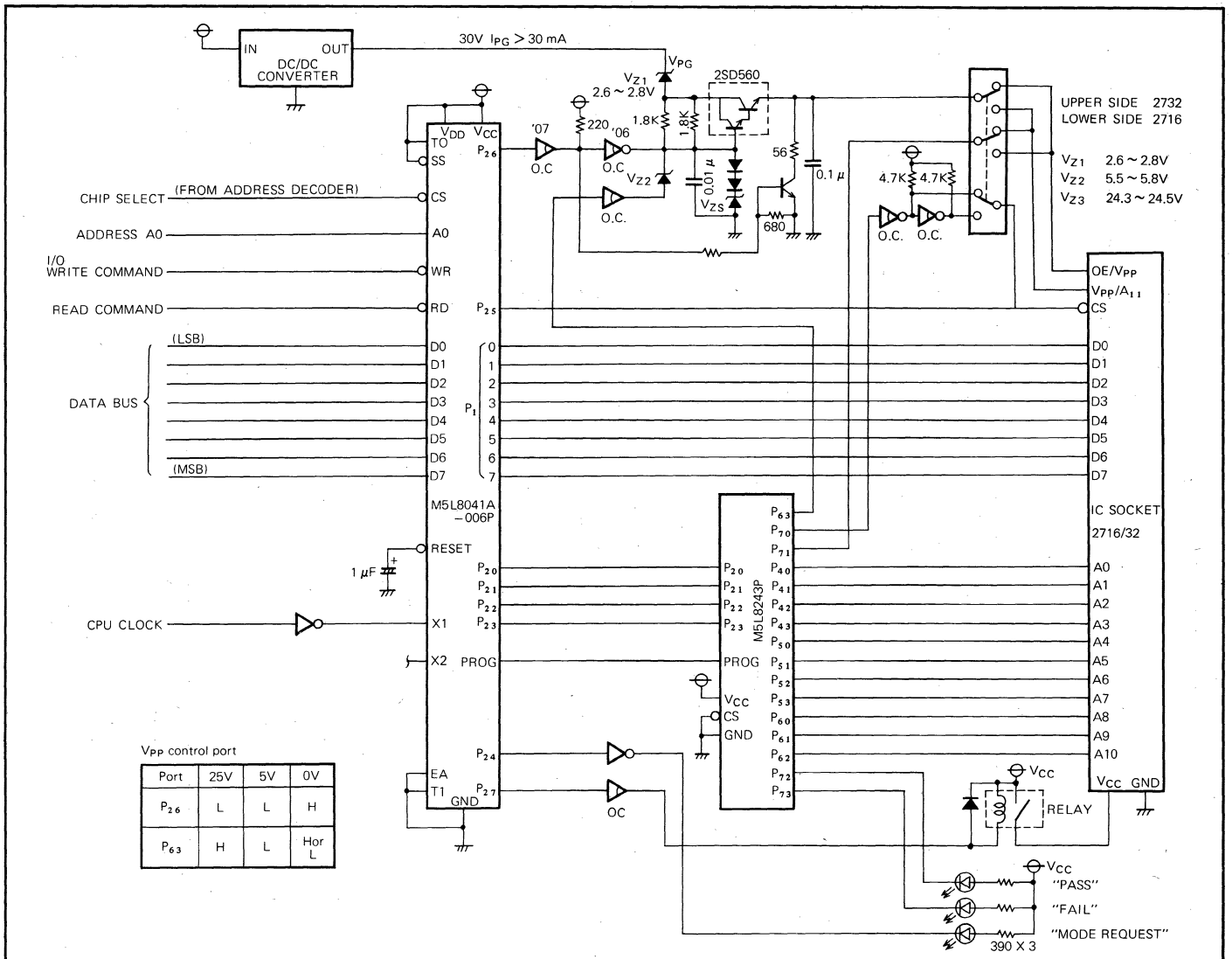



**Fig. 3.15 Design example of PRPG.**

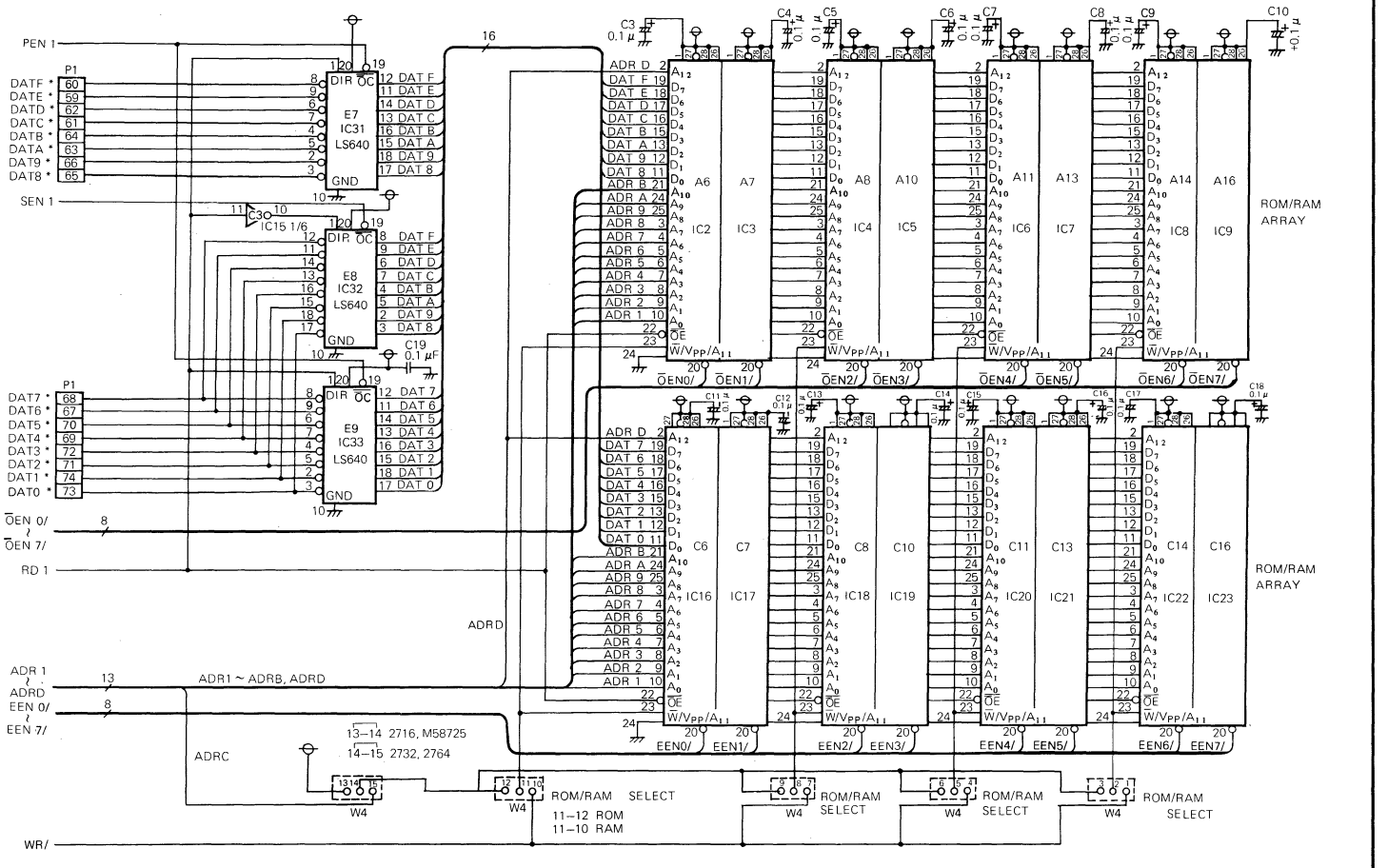
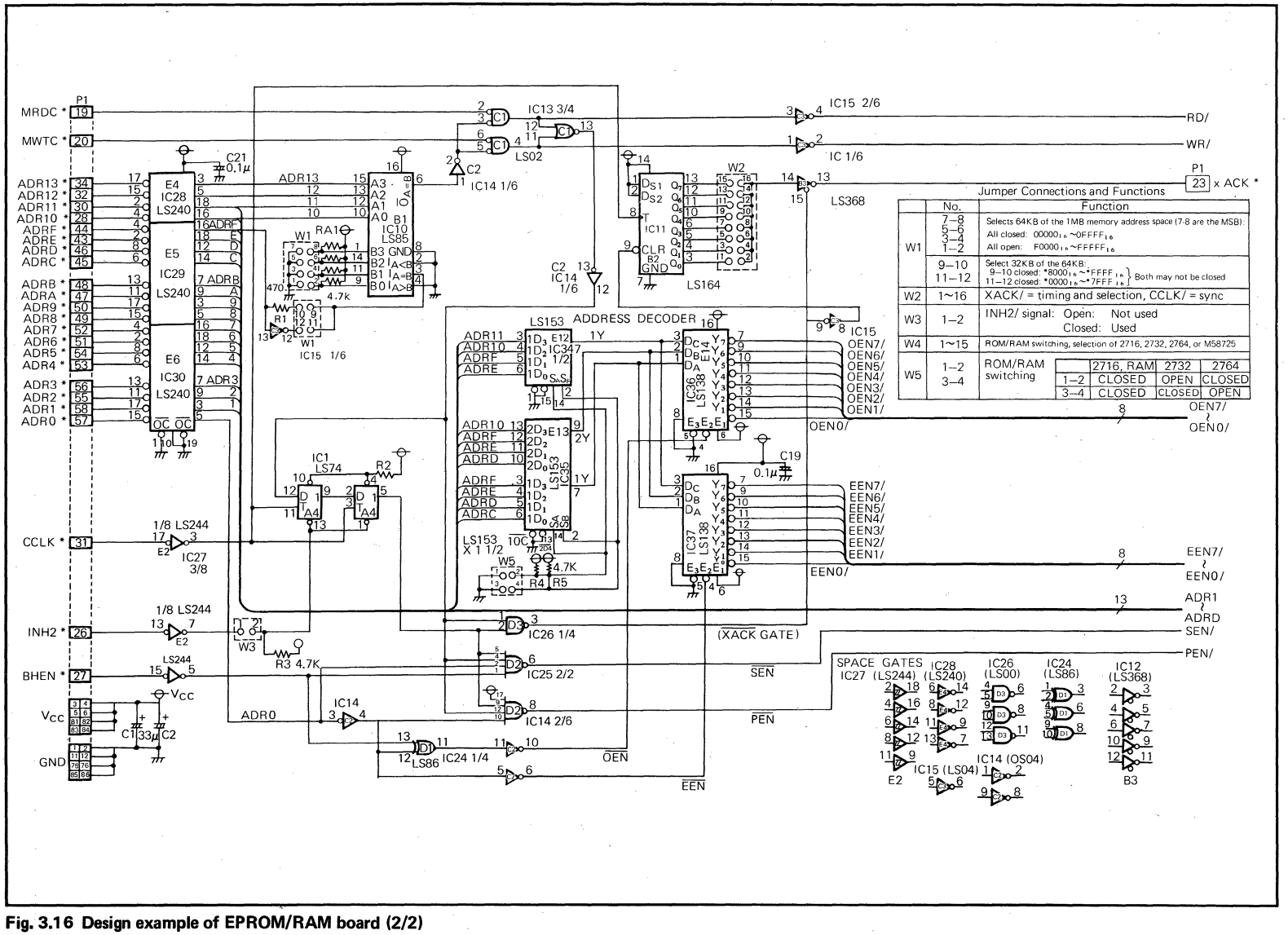



**Fig. 3.16 Design example of EPROM/RAM board (1/2)**




Jumper Connections and Functions

| | No. | Function |
|---|---|---|
| W1 | 7–8<br>5–6<br>3–4<br>1–2 | Selects 64KB of the 1MB memory address space (7-8 are the MSB):<br>All closed: $00000_{16}$ ~ $0FFFF_{16}$<br>All open: $F0000_{16}$ ~ $FFFFF_{16}$ |
| | 9–10<br>11–12 | Select 32KB of the 64KB:<br>9–10 closed: $*8000_{16}$ ~ $*FFFF_{16}$<br>11–12 closed: $*0000_{16}$ ~ $*7FFF_{16}$<br>} Both may not be closed |
| W2 | 1~16 | XACK/ = timing and selection, CCLK/ = sync |
| W3 | 1–2 | INH2/ signal: Open: Not used<br>Closed: Used |
| W4 | 1~15 | ROM/RAM switching, selection of 2716, 2732, 2764, or M58725 |
| W5 | 1–2<br>3–4 | ROM/RAM switching |

| | 2716, RAM | 2732 | 2764 |
|---|---|---|---|
| 1–2 | CLOSED | OPEN | CLOSED |
| 3–4 | CLOSED | CLOSED | OPEN |

**Fig. 3.16 Design example of EPROM/RAM board (2/2)**

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