IC MEMORIES

DATA BOOK

MITSUBISHI
ELECTRIC

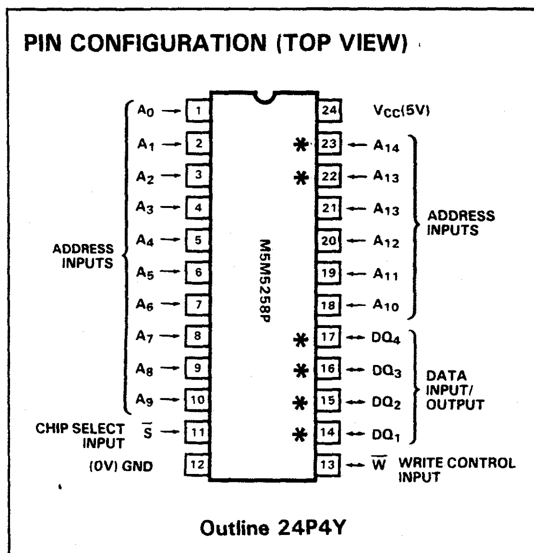
All values shown in this catalogue are subject to change for product improvement.

The information, diagrams and all other data included herein are believed to be correct and reliable. However, no responsibility is assumed by Mitsubishi Electric Corporation for their use, nor for any infringements of patents or other rights belonging to third parties which may result from their use.

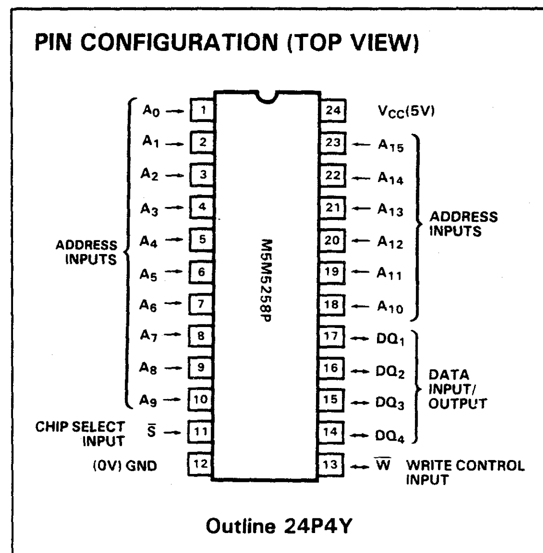
Addendum for M5M5258P (64K × 4) SRAM
in 1987 Memory Data Book

The pin out designation for the M5M5258P has an error for the Data Input/Output pins and for Address pins 14 and 15. The block diagram is also wrong accordingly. The correct designator is shown below.

Incorrect Designation



Correct Designation



GUIDANCE 1

MOS DYNAMIC RAM 2

CMOS STATIC RAM 3

ECL RAM 4

MOS MASK ROM 5

MOS EPROM 6

MOS OTPROM 7

MOS EEPROM 8

MOS EAROM 9

APPLICATIONS 10

CONTENTS

1 GUIDANCE

Page

Guide to Selection of IC Memories ···· 1—2
Index by Function ···· 1—12
Guide to Interchangeability ···· 1—20
Ordering Information ···· 1—32
Package Outlines ···· 1—34
Letter Symbols for The Dynamic Parameters ···· 1—49
Symbology ···· 1—52
Precautions in Handling MOS IC/LSIs ···· 1—55

2 MOS DYNAMIC RAM

M5K4164AP-12, -15 65536-Bit (65536-Word by 1-Bit) Dynamic RAM ···· 2—3
M5K4164ANP-12, -15 65536-Bit (65536-Word by 1-Bit) Dynamic RAM ···· 2—14
M5M4416P-12, -15 65536-Bit (16384-Word by 4-Bit) Dynamic RAM ···· 2—24
M5M4256P-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—39
M5M4257P-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—54
M5M4256L-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—69
M5M4257L-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—84
M5M4256J-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—99
M5M4257J-10, -12, -15 262144-Bit (262144-Word by 1-Bit) Dynamic RAM ···· 2—114
M5M4464P-10, -12, -15 262144-Bit (65536-Word by 4-Bit) Dynamic RAM ···· 2—129
M5M4464L-10, -12, -15 262144-Bit (65536-Word by 4-Bit) Dynamic RAM ···· 2—144
M5M4C264P-10, -12, -15/M5M4C264L-10, -12, -15
262144-Bit Dual-Port Dynamic RAM ···· 2—159
MH25608J-10, -12, -15/MH25608JA-10, -12, -15
2097152-Bit (262144-Word by 8-Bit) Dynamic RAM ···· 2—184
MH25609J-10, -12, -15/MH25609JA-10, -12, -15
2359296-Bit (262144-Word by 9-Bit) Dynamic RAM ···· 2—193
M5M44C256P, J, L-10, -12, -15
Fast Page Mode 1048576-Bit (262144-Word by 4-Bit) Dynamic RAM ···· 2—202
M5M44C258P, J, L-10, -12, -15
Static Cloumn Mode 1048576-Bit (262144-Word by 4-Bit) Dynamic RAM ···· 2—218
M5M4C1000P, J, L-10, -12, -15
Fast Page Mode 1048576-Bit (1048576-Word by 1-Bit) Dynamic RAM ···· 2—234
M5M4C1001P, J, L-10, -12, -15
Nibble Mode 1048576-Bit (1048576-Word by 1-Bit) Dynamic RAM ···· 2—248
M5M4C1002P, J, L-10, -12, -15
Static Cloumn Mode 1048576-Bit (1048576-Word by 1-Bit) Dynamic RAM ···· 2—262

3 CMOS STATIC RAM

M5M21C67P-35, -45, -55 16384-Bit (16384-Word by 1-Bit) CMOS Static RAM ···· 3—3
M5M21C68P-35, -45, -55 16384-Bit (4096-Word by 4-Bit) CMOS Static RAM ···· 3—7
M5M5165P-70, -10, -12, -15, -70L, -10L, -12L, -15L
65536-Bit (8192-Word by 8-Bit) CMOS Static RAM ···· 3—11

		Page
M5M5165FP-70, -10, -12, -15, -70L, -10L, -12L, -15L	65536-Bit (8192-Word by 8-Bit) CMOS Static RAM	3—17
M5M5187P-45, -55	65536-Bit (65536-Word by 1-Bit) CMOS Static RAM	3—23
M5M5187AP-25, -35	65536-Bit (65536-Word by 1-Bit) CMOS Static RAM	3—27
M5M5188P-45, -55	65536-Bit (16384-Word by 4-Bit) CMOS Static RAM	3—31
M5M5188AP-25, -35	65536-Bit (16384-Word by 4-Bit) CMOS Static RAM	3—35
M5M5178P-35, -45, -55	65536-Bit (8192-Word by 8-Bit) CMOS Static RAM	3—39
M5M5179P-35, -45, -55	73728-Bit (8192-Word by 9-Bit) CMOS Static RAM	3—44
M5M5256P-10,-12,-15,-10L,-12L,-15L	262144-Bit(32768-Word by 8-Bit) CMOS Static RAM	3—49
M5M5256FP-10, -12, -15,-10L, -12L, -15L	262144-Bit (32768-Word by 8-Bit) CMOS Static RAM	3—54
M5M5256AP-70, -85, -10, -70L, -85L, -10L	262144-Bit (32768-Word by 8-Bit) CMOS Static RAM	3—59
M5M5257P-35, -45, -55	262144-Bit (262144-Word by 1-Bit) CMOS Static RAM	3—64
M5M5258P-35, -45, -55	262144-Bit (65536-Word by 4-Bit) CMOS Static RAM	3—68

4 ECL RAM

M10422S-5, -7	1024-Bit (256-Word by 4-Bit) Static RAM	4—3
M10474S-10, -15	4096-Bit (1024-Word by 4-Bit) Static RAM	4—7

5 MOS MASK ROM

MASK ROM ORDERING METHOD		5—3
M5M2364-XXXP	65536-Bit (8192-Word by 8-Bit) Mask-Programmable ROM	5—6
M5M23128-XXXP	131072-Bit (16384-Word by 8-Bit) Mask-Programmable ROM	5—10
M5M23256-XXXP	262144-Bit (32768-Word by 8-Bit) Mask-Programmable ROM	5—13
M5M231000-XXXP	1048576-Bit (131072-Word by 8-Bit) Mask-Programmable ROM	5—16
M5M231001-XXXP	1048576-Bit (131072-Word by 8-Bit) Mask-Programmable ROM	5—18
M5M23C100-XXXP	1048576-Bit (131072-Word by 8-Bit) CMOS Mask-Programmable ROM	5—20
M5M23C400-XXXP	4194304-Bit (262144-Word by 16-Bit) CMOS Mask-Programmable ROM/ 4194304-Bit (524288-Word by 8-Bit) CMOS Mask-Programmable ROM	5—22

6 MOS EPROM

M5L2764K, -2	65536-Bit (8192-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM	6—3
M5L27128K, -25, -2, -20	131072-Bit (16384-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM	6—10
M5L27128K-I	131072-Bit (16384-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM	6—18
M5M27C128K, -15, -2	131072-Bit (16384-Word by 8-Bit) CMOS Erasable and Electrically Reprogrammable ROM	6—26
M5L27256K, -15, -2	262144-Bit (32768-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM	6—34
M5L27256K-I	262144-Bit (32768-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM	6—40

Page

M5M27C256K, -12, -15 262144-Bit (32768-Word by 8-Bit) CMOS Erasable and Electrically Reprogrammable ROM ········ 6—46

M5L27512K, -17, -2 524288-Bit (65536-Word by 8-Bit) Erasable and Electrically Reprogrammable ROM ········ 6—52

M5M27C100K, -15, -2 1048576-Bit (131072-Word by 8-Bit) CMOS Erasable and Electrically Reprogrammable ROM ········ 6—58

M5M27C101K, -15, -2 1048576-Bit (131072-Word by 8-Bit) CMOS Erasable and Electrically Reprogrammable ROM ········ 6—59

M5M27C102K, -15, -2 1048576-Bit (65536-Word by 16-Bit) CMOS Erasable and Electrically Reprogrammable ROM ········ 6—60

7 MOS OTPROM

M5M2764P 65536-Bit (8192-Word by 8-Bit) One Time Programmable ROM ········ 7—3

M5M27128P 131072-Bit (16384-Word by 8-Bit) One Time Programmable ROM ········ 7—10

M5M27256P, FP 262144-Bit (32768-Word by 8-Bit) One Time Programmable ROM ········ 7—18

M5M27512P, FP 524288-Bit (65536-Word by 8-Bit) One Time Programmable ROM ········ 7—24

8 MOS EEPROM

M5M28C64P 65536-Bit (8192-Word by 8-Bit) Electrically Erasable and Programmable ROM ········ 8—3

9 MOS EAROM

M58630P 2048-Bit (128-Word by 16-Bit) Electrically Alterable ROM ········ 9—3

M58653P 700-Bit (50-Word by 14-Bit) Electrically Alterable ROM ········ 9—11

M58655P 1024-Bit (64-Word by 16-Bit) Electrically Alterable ROM ········ 9—17

M58657P 1400-Bit (100-Word by 14-Bit) Electrically Alterable ROM ········ 9—25

M58658P 320-Bit (20-Word by 16-Bit) Electrically Alterable ROM ········ 9—31

M58659P 512-Bit (32-Word by 16-Bit) Electrically Alterable ROM ········ 9—39

M5G1400P 1400-Bit (100-Word by 14-Bit) Electrically Alterable ROM ········ 9—47

10 APPLICATIONS

64K, 256K-BIT DYNAMIC RAM ········ 10—3

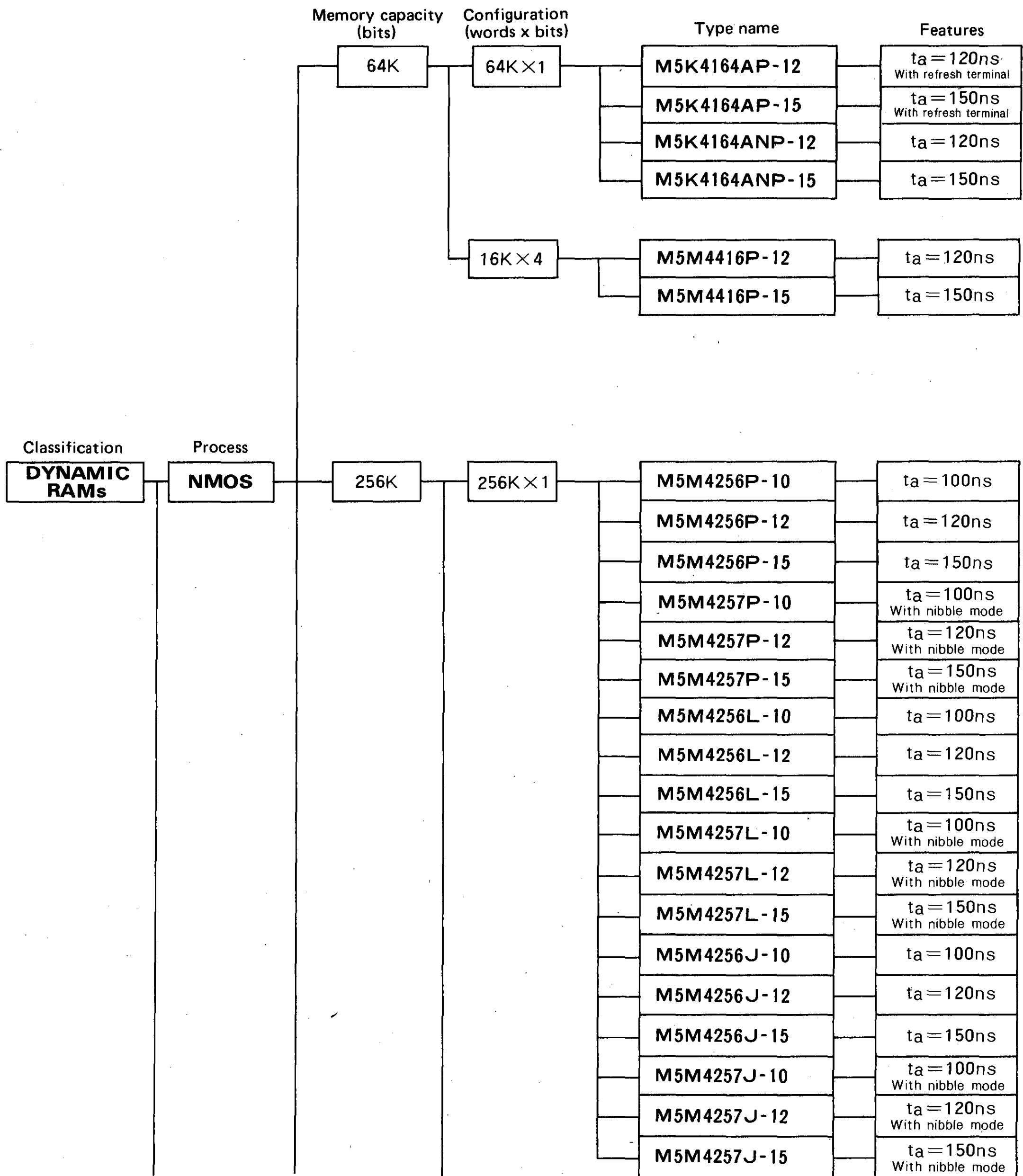
STATIC RAM ········ 10—49

Contact Addresses for Further Information

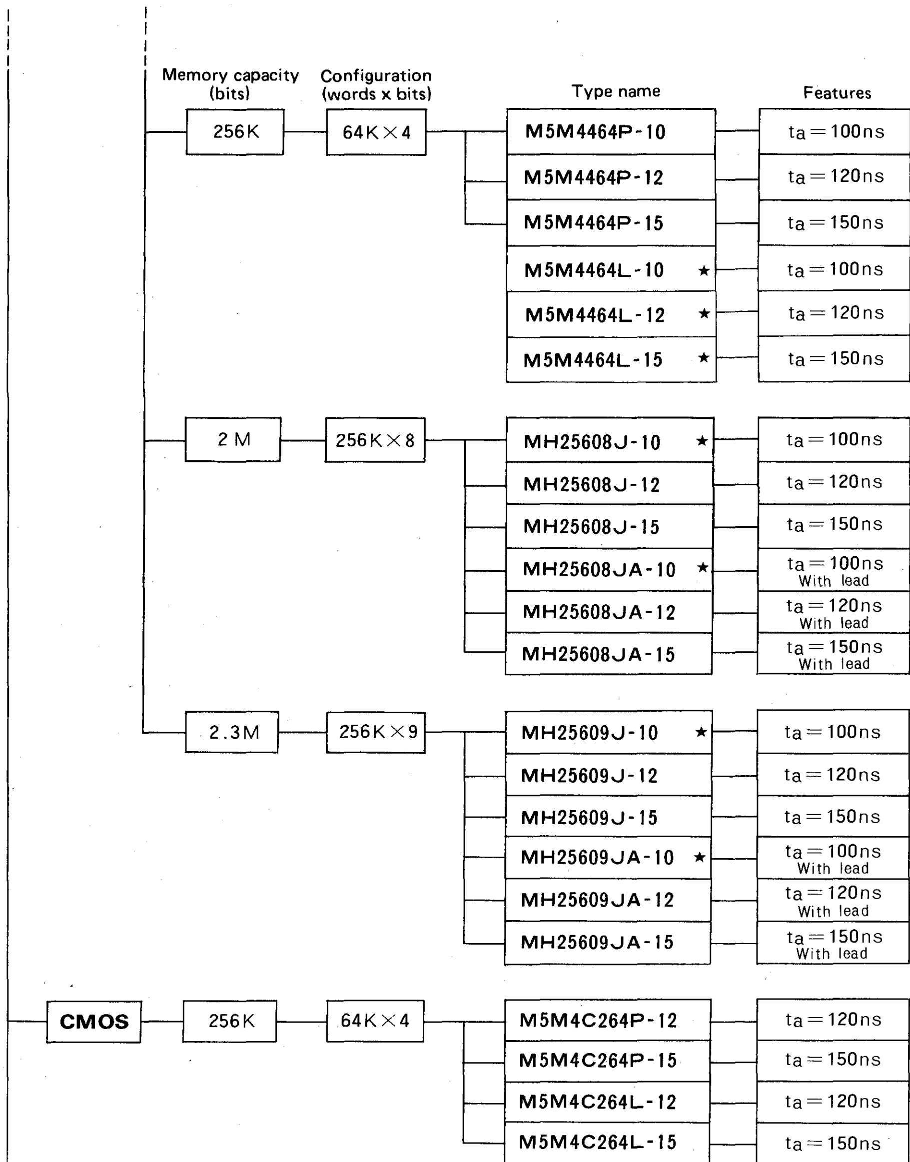
GUIDANCE 1

GUIDE TO SELECTION OF IC MEMORIES

DYNAMIC RAMs



DYNAMIC RAMs



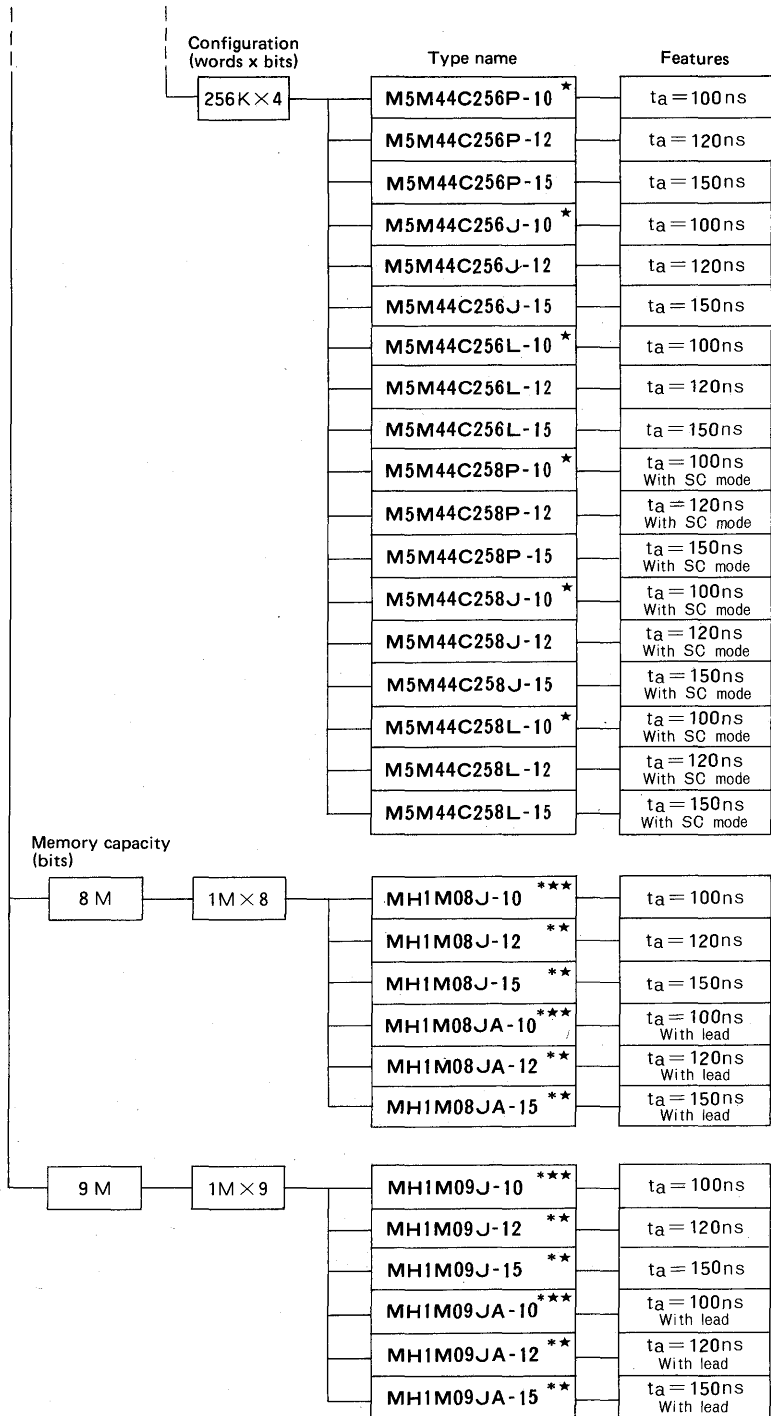
★ : New product

DYNAMIC RAMs

Memory capacity (bits)	Configuration (words x bits)	Type name	Features
1 M	1 M × 1	M5M4C1000P-10 ★	ta = 100ns
		M5M4C1000P-12	ta = 120ns
		M5M4C1000P-15	ta = 150ns
		M5M4C1000J-10 ★	ta = 100ns
		M5M4C1000J-12	ta = 120ns
		M5M4C1000J-15	ta = 150ns
		M5M4C1000L-10 ★	ta = 100ns
		M5M4C1000L-12	ta = 120ns
		M5M4C1000L-15	ta = 150ns
		M5M4C1001P-10 ★	ta = 100ns With nibble mode
		M5M4C1001P-12	ta = 120ns With nibble mods
		M5M4C1001P-15	ta = 150ns With nibble mode
		M5M4C1001J-10 ★	ta = 100ns With nibble mode
		M5M4C1001J-12	ta = 120ns With nibble mode
		M5M4C1001J-15	ta = 150ns With nibble mode
		M5M4C1001L-10 ★	ta = 100ns With nibble mode
		M5M4C1001L-12	ta = 120ns With nibble mode
		M5M4C1001L-15	ta = 150ns With nibble mode
		M5M4C1002P-10 ★	ta = 100ns With SC mode
		M5M4C1002P-12	ta = 120ns With SC mode
		M5M4C1002P-15	ta = 150ns With SC mode
		M5M4C1002J-10 ★	ta = 100ns With SC mode
		M5M4C1002J-12	ta = 120ns With SC mode
		M5M4C1002J-15	ta = 150ns With SC mode
		M5M4C1002L-10 ★	ta = 100ns With SC mode
		M5M4C1002L-12	ta = 120ns With SC mode
		M5M4C1002L-15	ta = 150ns With SC mode

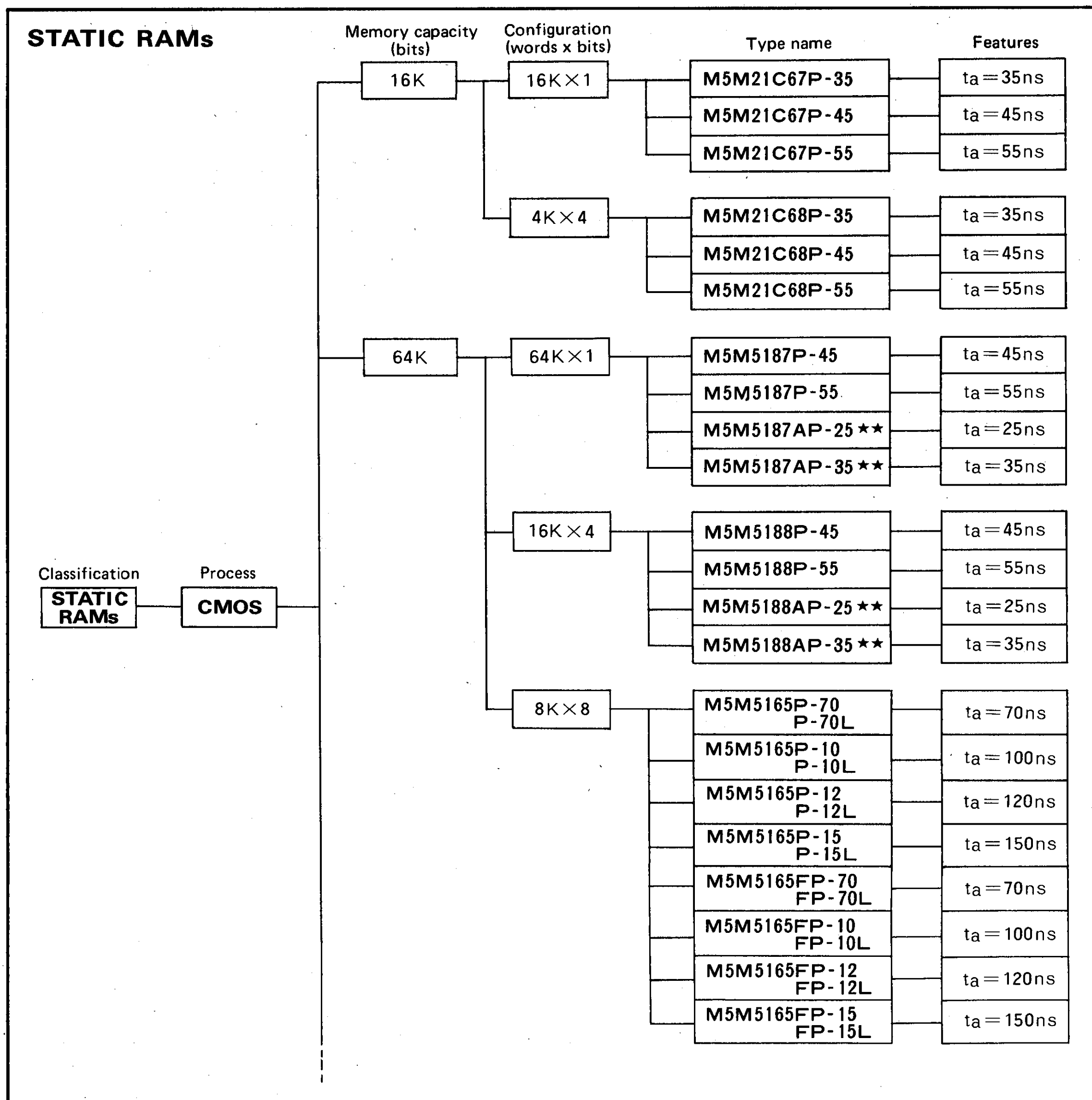
★ : New product.

DYNAMIC RAMs



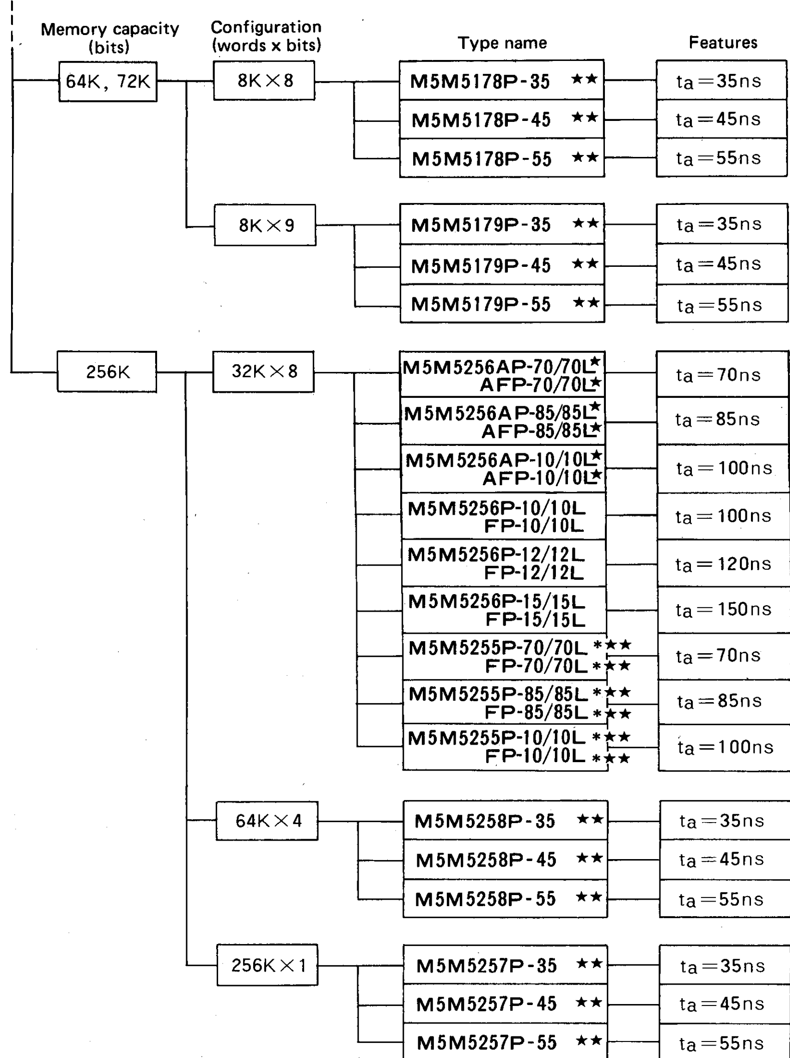
★ : New product ★★ : Under development * : These devices are not published yet.

GUIDE TO SELECTION OF IC MEMORIES



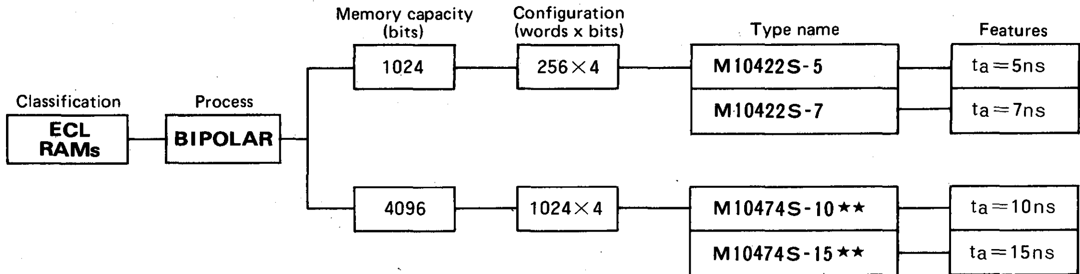
★★ : Under development

STATIC RAMs

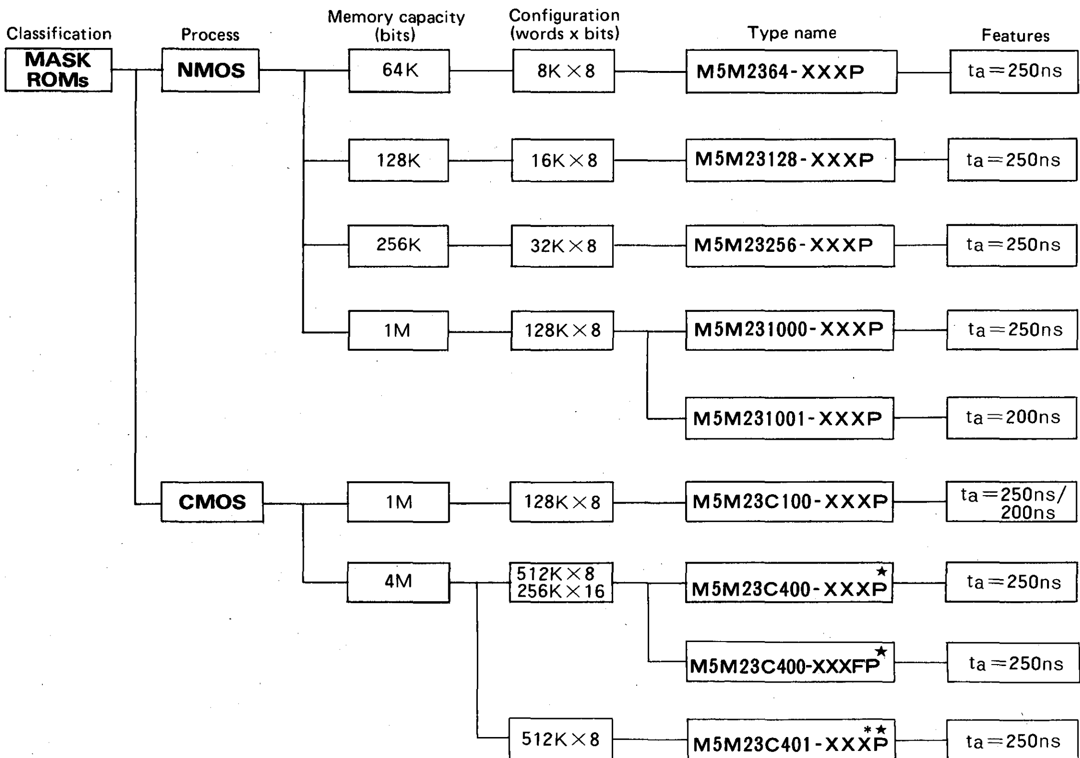


★ : New product ★★ : Under development * : These devices are not published yet.

GUIDE TO SELECTION OF IC MEMORIES



★★ : Under development



★ : New product ✱ : These devices are not published yet.

MITSUBISHI ELECTRIC

GUIDE TO SELECTION OF IC MEMORIES

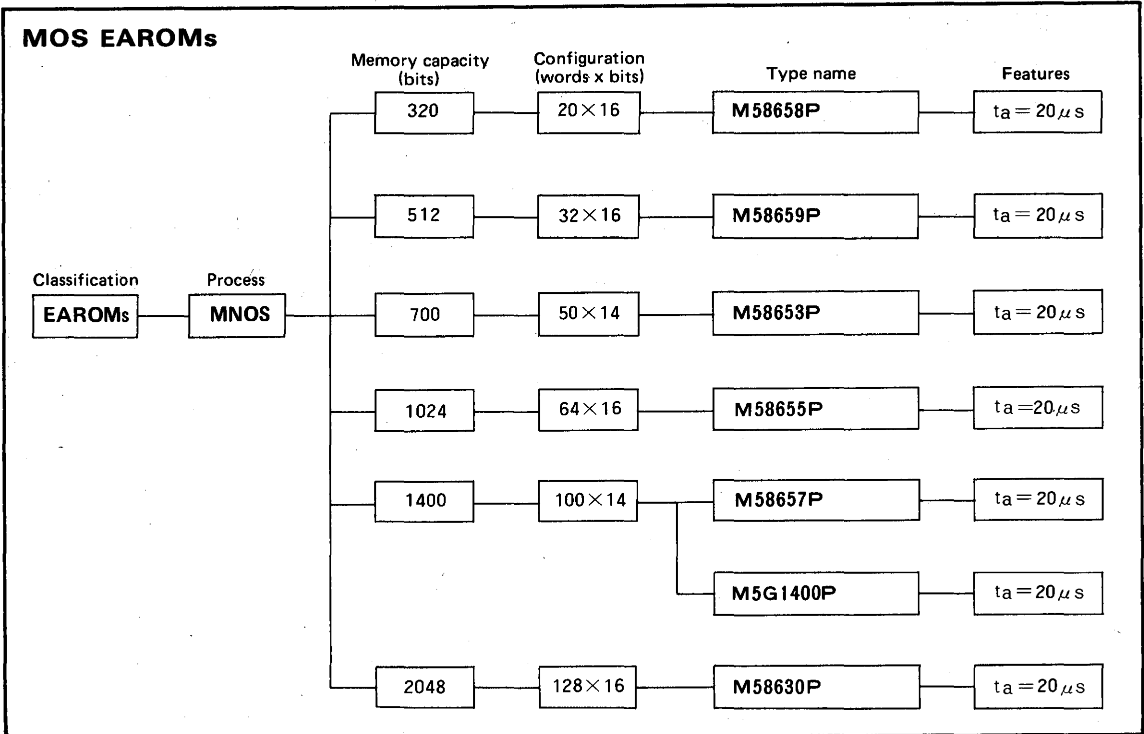
MOS EPROMs

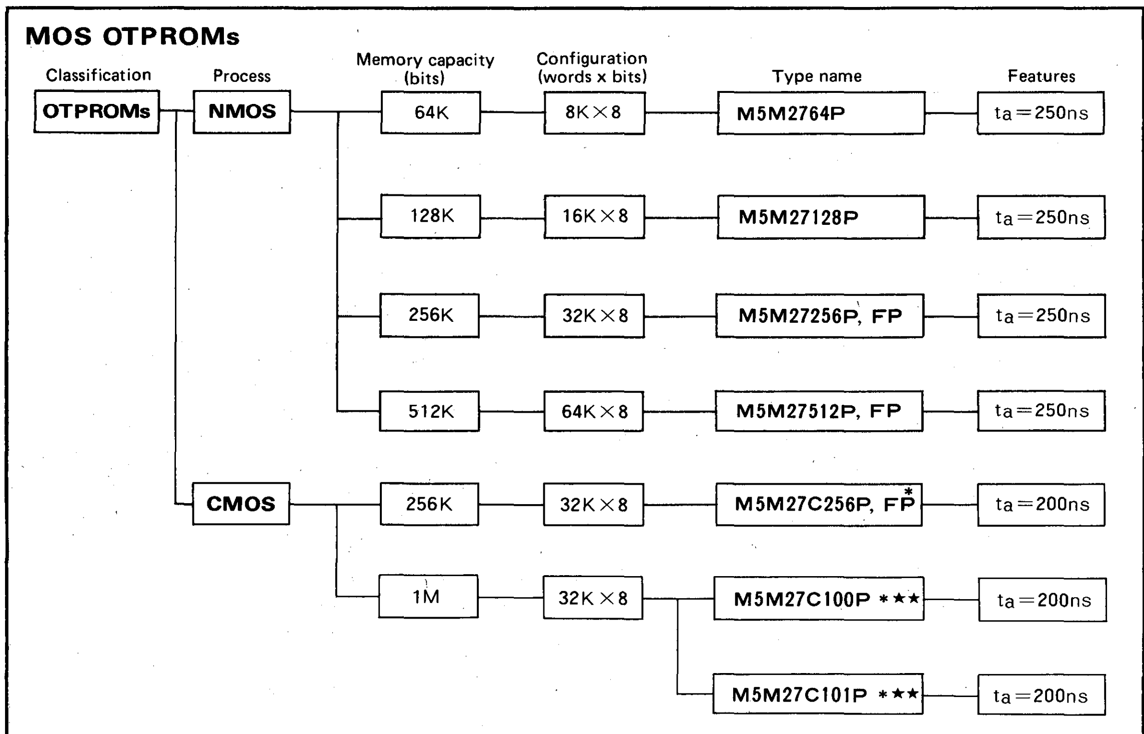
Classification	Process	Memory capacity (bits)	Configuration (words x bits)	Type name	Features
EPROMs	NMOS	64K	8K×8	M5L2764K-2	ta=200ns
				M5L2764K	ta=250ns
		128K	16K×8	M5L27128K-2	ta=200ns
				M5L27128K-20	ta=200ns
				M5L27128K	ta=250ns
				M5L27128K-25	ta=250ns
		256K	32K×8	M5L27256K-15	ta=150ns
				M5L27256K-2	ta=200ns
				M5L27256K	ta=250ns
		512K	64K×8	M5L27512K-17	ta=170ns
				M5L27512K-2	ta=200ns
				M5L27512K	ta=250ns
	CMOS	128K	16K×8	M5M27C128K-15	ta=150ns
				M5M27C128K-2	ta=200ns
				M5M27C128K	ta=250ns
		256K	32K×8	M5M27C256K-12	ta=120ns
				M5M27C256K-15	ta=150ns
				M5M27C256K	ta=250ns
		1M	128K×8	M5M27C100K-15 ★	ta=150ns
				M5M27C100K-2 ★	ta=200ns
				M5M27C100K ★	ta=250ns
			128K×8	M5M27C101K-15 ★	ta=150ns
				M5M27C101K-2 ★	ta=200ns
				M5M27C101K ★	ta=250ns
			64K×16	M5M27C102K-15 ★★	ta=150ns
				M5M27C102K-2 ★★	ta=200ns
				M5M27C102K ★★	ta=250ns

★ : New product ★★ : Under development

MITSUBISHI ELECTRIC

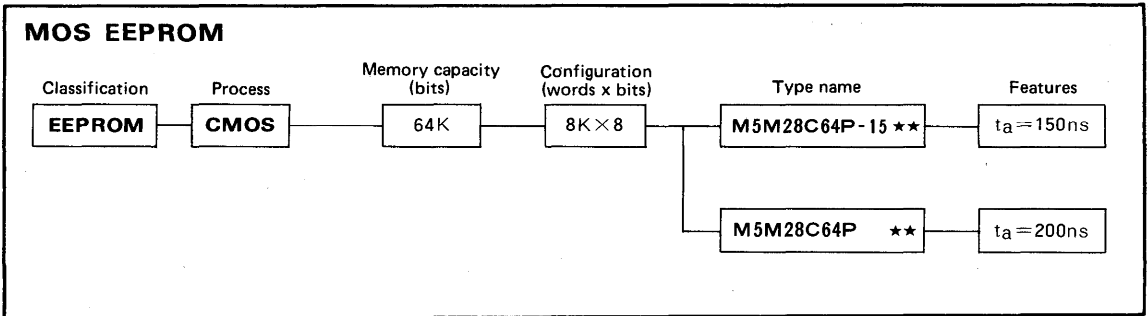
GUIDE TO SELECTION OF IC MEMORIES





**: Under development * : These devices are not published yet.

MITSUBISHI ELECTRIC



★★ : Under development

■64K-Bit DYNAMIC RAM

DIP

Type	Structure	Memory capacity (configuration)	Refresh pin	Access time Max (ns)	Cycle time Min (ns)	Power dissipation Typ (mW)	Low power dissipation Max (mW) Operating time	Specifications	Package outlines	Interchangeable products	Page
M5K4164AP-12	NMOS	64K (64K×1)	Yes	120	220	175	275	● 128 refresh cycles every 2ms ● 1-pin automatic and self-refreshing capability	16P4	See page 1-20	2—3
M5K4164AP-15				150	260	150	250				
M5K4164ANP-12			No	120	220	175	275	● 128 refresh cycles every 2ms ● $\overline{CAS}$ input allows hidden refresh operation			2—14
M5K4164ANP-15				150	260	150	250				
M5M4416P-12		64K (16K×4)		120	220	175	275	● 128 refresh cycles every 2ms ● 4-bit configuration	18P4		2—24
M5M4416P-15				150	260	150	250				

■256K-Bit DYNAMIC RAM

DIP

Type	Structure	Memory capacity (configuration)	Function mode	Access time Max(ns)	Cycle time Min(ns)	Power dissipation Typ(mW)	Low power dissipation Max(mW) Operating time	Specifications	Package outlines	Interchangeable products	Page
M5M4256P-10	NMOS	256K (256K×1)	Page mode	100	200	300	385	● 256 refresh cycles every 4ms ● $\overline{CAS}$ before $\overline{RAS}$ refresh operation capability ● $\overline{CAS}$ input allows hidden refresh operation.	16P4	See page 1-20	2—39
M5M4256P-12				120	230	260	360				
M5M4256P-15				150	260	230	330				
M5M4257P-10			Nibble mode	100	200	300	385				2—54
M5M4257P-12				120	230	260	360				
M5M4257P-15				150	260	230	330				
M5M4464P-10		256K (64K×4)	Page mode	100	200	300	420	● 256 refresh cycles every 4ms. ● $\overline{CAS}$ before $\overline{RAS}$ refresh operation capability. ● $\overline{CAS}$ input allows hidden refresh operation. ● 4-bit configuration	18P4H	See page 1-20	2—129
M5M4464P-12				120	220	260	360				
M5M4464P-15				150	260	230	330				
M5M4C264P-12	CMOS	RAM 256K (64K×4) SAM 1024 (256×4)	Page mode	120	220	300	100	● High speed serial Input/Output ● Dual port RAM ● 256 refresh cycles every 4ms	24P4F		2—159
M5M4C264P-15				150	260	250	80				

PLCC

Type	Structure	Memory capacity (configuration)	Function mode	Access time Max(ns)	Cycle time Min(ns)	Power dissipation Typ(mW)	Low power dissipation Max(mW) Operating time	Specifications	Package outlines	Interchangeable products	Page
M5M4256J-10	NMOS	256K (256K×1)	Page mode	100	200	300	385	● Same electrical characteristics as the M5M4256P and M5M4257P series. ● Package 18-pin chip carrier	18P0A	—	2—99
M5M4256J-12				120	230	260	360			See page 1-20	
M5M4256J-15				150	260	230	330				
M5M4257J-10			Nibble mode	100	200	300	385			—	2—114
M5M4257J-12				120	230	260	360			See page 1-20	
M5M4257J-15				150	260	230	330				

MITSUBISHI ELECTRIC

■256K-Bit DYNAMIC RAM
ZIP

Type	Structure	Memory capacity (configu-ration)	Function mode	Access time Max(ns)	Cycle time Min(ns)	Power dissipation Typ(mW)	Low power dissipation Max(mW) Operating time	Specifications	Package outline	Inter-changeable products	Page
M5M4256L-10	NMOS	256K (256K×1)	Page mode	100	200	300	385	● Same electrical characteristics as the M5M4256P and M5M4257P series. ● Package 16-pin zig-zag in line.	16P5A	—	2—69
M5M4256L-12				120	230	260	360			See page 1-20	
M5M4256L-15				150	260	230	330				
M5M4257L-10			Nibble mode	100	200	300	385			—	2—84
M5M4257L-12				120	230	260	360			See page 1-20	
M5M4257L-15				150	260	230	330				
M5M4464L-10 ★		256K (64K×4	Page mode	100	200	300	420	● Same electrical characteristics as the M5M4464P series	20P5L	—	2—144
M5M4464L-12 ★				120	220	260	360				
M5M4464L-15 ★				150	260	230	330				
M5M4C264L-12	CMOS	RAM 256K (64K×4) SAM 1024 (256×4)		120	220	300	100	● 24-pin Zig-Zag in line	24P5L	—	2—159
M5M4C264L-15				150	260	250	80				

★ : New product

SIP MODULE

Type	Structure	Memory capacity (configu-ration)	Function mode	Access time Max(ns)	Number of chip carrier	Specifications	Package outlines	Inter-changeable products	Page
MH25608J-10 ★	NMOS	2M (256K ×8)	Page mode	100	8	● Package : 30-pin Plug In Type ● External dimensions 17.2×88.9×5.08mm	30N9	—	2—184
MH25608J-12				120				See page 1-20	
MH25608J-15				150					
MH25608JA-10 ★				100		● Package : 30-pin Lead Type ● External dimensions 20.8×78.9×5.08mm	30N5	—	
MH25608JA-12				120				See page 1-20	
MH25608JA-15				150					
MH25609J-10 ★		2.3M (256K ×9)		100	9	● Package : 30-pin Plug In Type ● External dimensions 17.2×88.9×5.08mm	30N9	—	2—193
MH25609J-12				120				See page 1-20	
MH25609J-15				150					
MH25609JA-10 ★				100		● Package : 30-pin Lead Type ● External dimensions 20.8×78.9×5.08mm	30N5	—	
MH25609JA-12				120				See page 1-20	
MH25609JA-15				150					

★ : New product

■1 M-Bit DYNAMIC RAM
DIP

Type	Structure	Memory capacity (configu-ration)	Function mode	Access time Max (ns)	Cycle time Min (ns)	Power dissipation Typ (mW)	Operating dissipation Max (mW)	Specifications	Package outlines	Inter-changeable products	Page
M5M4C1000P-10★	CMOS	1M (1M×1)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh	18P4Y	See page 1-22	2—234
M5M4C1000P-12				120	220	250	358				
M5M4C1000P-15				150	260	200	303				
M5M4C1001P-10★			Nibble mode	100	190	300	413				2—248
M5M4C1001P-12				120	220	250	358				
M5M4C1001P-15				150	260	200	303				
M5M4C1002P-10★			Static Column mode	100	190	300	413				2—262
M5M4C1002P-12				120	220	250	358				
M5M4C1002P-15				150	260	200	303				
M5M44C256P-10★		1M (256K×4)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh ●4-bits configuration	20P4Y		2—202
M5M44C256P-12				120	220	250	358				
M5M44C256P-15				150	260	200	303			—	
M5M44C258P-10★			Static Column mode	100	190	300	413			See page 1-22	2—218
M5M44C258P-12				120	220	250	358				
M5M44C258P-15				150	260	200	303			—	

★ : New product

SOJ

Type	Structure	Memory capacity (configu-ration)	Function mode	Access time Max (ns)	Cycle time Min (ns)	Power dissipation Typ (mW)	Operating power dissipation Max (mW)	Specification	Package outlines	Inter-changeable products	Page
M5M4C1000J-10★	CMOS	1M (1M×1)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh	26P0J	See page 1-22	2—234
M5M4C1000J-12				120	220	250	358				
M5M4C1000J-15				150	260	200	303				
M5M4C1001J-10★			Nibble mode	100	190	300	413				2—248
M5M4C1001J-12				120	220	250	358				
M5M4C1001J-15				150	260	200	303				
M5M4C1002J-10★			Static Column mode	100	190	300	413				2—262
M5M4C1002J-12				120	220	250	358				
M5M4C1002J-15				150	260	200	303			—	
M5M44C256J-10★		1M (256K×4)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh ●4-bits configuration		See page 1-22	2—202
M5M44C256J-12				120	220	250	358				
M5M44C256J-15				150	260	200	303			—	
M5M44C258J-10★			Static Column mode	100	190	300	413			See page 1-22	2—218
M5M44C258J-12				120	220	250	358				
M5M44C258J-15				150	260	200	303			—	

★ : New product

■1M-Bit DYNAMIC RAM

ZIP

Type	Structure	Memory capacity (configu lation)	Function mode	Access time Max (ns)	Cycle time Min (ns)	Power dissipation Typ (mW)	Operating power dissipation Max(mW)	Specifications	Package outlines	Inter-changeable products	Page
M5M4C1000L-10★	CMOS	1M (1M×1)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh	20P5L	See page 1-22	2—234
M5M4C1000L-12				120	220	250	358				
M5M4C1000L-15				150	260	200	303				
M5M4C1001L-10★			Nibble mode	100	190	300	413				2—248
M5M4C1001L-12				120	220	250	358				
M5M4C1001L-15				150	260	200	303				
M5M4C1002L-10★			Static Column mode	100	190	300	413			—	2—262
M5M4C1002L-12				120	220	250	358				
M5M4C1002L-15				150	260	200	303				
M5M44C256L-10★		1M (256K×4)	Fast page mode	100	190	300	413	●512 refresh cycle every 8ms ●CAS before RAS refresh operating capability ●CAS controlled output allows hidden refresh ●4-bits configuration		—	2—202
M5M44C256L-12				120	220	250	358				
M5M44C256L-15				150	260	200	303				
M5M44C258L-10★			Static Column mode	100	190	300	413				2—218
M5M44C258L-12				120	220	250	358				
M5M44C258L-15				150	260	200	303				

★ : New product

SIM/SIP MODULE

Type	Structure	Memory capacity (configu-ration)	Function mode	Access time Max(ns)	Number of chip carrier	Specifications	Package outlines	Inter-changeable products	Page
MH1M08J-10 ***	CMOS	8 M (1M×8)	Fast page mode	100	8	●Package 30-pin plug in type ●External measurements 20.3×88.9×5.08 (Unit mm)	30N9A	—	—
MH1M08J-12 **				120					
MH1M08J-15 **				150					
MH1M08JA-10 ***				100		●Package : 30-pin lead type ●Eyternal measurements 23.6×79.8×5.08 (unit mm)	30N5A		
MH1M08JA-12 **				120					
MH1M08JA-15 **				150					
MH1M09J-10 ***		9 M (1M×9)		100	9	●Package : 30-pin plug in type ●External measurements 20.3×88.9×5.08 (unit mm)	30N9A		
MH1M09J-12 **				120					
MH1M09J-15 **				150					
MH1M09JA-10 ***				100		●Package : 30-pin lead type ●External measurements 23.6×79.8×5.08 (unit mm)	30N5A		
MH1M09JA-12 **				120					
MH1M09JA-15 **				150					

★ : New product ★★ : Under deveropment * : These devices are not published yet.

■16K-Bit STATIC RAM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ (mW)	Access time Max(ns)	Cycle time Min(ns)	Package outlines	Inter-changeable products	Page
M5M21C67P-35	CMOS	16K	16K×1	5±10%	200	35	35	20P4	See page 1-26	3—3
M5M21C67P-45						45	45			
M5M21C67P-55						55	55			
M5M21C68P-35			4K×4			35	35			3—7
M5M21C68P-45						45	45			
M5M21C68P-55						55	55			

■64K-Bit STATIC RAM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Power dissipation Operating Typ(mW)	Power dissipation Standby Max(mW)	Access time Max(ns)	Cycle time Max(ns)	Package outlines	Inter-changeable products	Page
M5M5165P,FP-70	CMOS	64K	8K×8	5±10%	200	11	70	70	28P4 (P) 28P2W (FP)	See page 1-26	3—11 (P) 3—17 (FP)
M5M5165P,FP-10							100	100			
M5M5165P,FP-12							120	120			
M5M5165P,FP-15							150	150			
M5M5165P,FP-70L						0.55	70	70			
M5M5165P,FP-10L							100	100			
M5M5165P,FP-12L							120	120			
M5M5165P,FP-15L							150	150			
M5M5187P-45			64K×1		300	11	45	45	22P4H		3—23
M5M5187P-55							55	55			
M5M5187AP-25 ★★							25	25			3—27
M5M5187AP-35 ★★							35	35		—	
M5M5188P-45			16K×4		300	11	45	45		See page 1-26	3—31
M5M5188P-55							55	55			
M5M5188AP-25 ★★							25	25		—	3—35
M5M5188AP-35 ★★							35	35		See page1-26	
M5M5189AP-25 ★★★					300	11	25	25	24P4Y	—	—
M5M5189AP-35 ★★★							35	35			
M5M5178P-35 ★★			8K×8		300	11	35	35	28P4Y	—	3—39
M5M5178P-45 ★★							45	45		See page 1-26	
M5M5178P-55 ★★							55	55			
M5M5179P-35 ★★		72K	8K×9		300	11	35	35			3—44
M5M5179P-45 ★★							45	45			
M5M5179P-55 ★★							55	55			

★★ : Under development ∗These devices are not published yet, Note : M5M5189AP with $\overline{OE}$

■256K-Bit STATIC RAM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Power dissipation		Access time Max (ns)	Cycle time Max(ns)	Package outlines	Inter-changeable products	Page
					Operating Typ(mW)	Standby Max(mW)					
M5M5256P,FP-10	CMOS	256K	32K×8	5±10%	200	11	100	100	28P4 (P) 28P2W (FP)	See page 1-26	3—49 (P)
M5M5256P,FP-12							120	120			
M5M5256P,FP-15							150	150			
M5M5256P,FP-10L					200	0.55	100	100			3—54 (FP)
M5M5256P,FP-12L							120	120			
M5M5256P,FP-15L							150	150			
M5M5256AP, AFP-70 †★					200	11	70	70		—	3—59
M5M5256AP, AFP-85 †★							85	85		See page 1-26	
M5M5256AP, AFP-10 †★							100	100			
M5M5256AP, AFP-70L †★					200	0.55	70	70		—	
M5M5256AP, AFP-85L †★							85	85		See page 1-26	
M5M5256AP, AFP-10L †★							100	100			
M5M5255P, FP-70 ∗★★					200	11	70	70		—	—
M5M5255P, FP-85 ∗★★							85	80			
M5M5255P, FP-10 ∗★★							100	100		See page1-26	
M5M5255P, FP-70L ∗★★					200	0.55	70	70		—	—
M5M5255P, FP-85L ∗★★							85	85			
M5M5255P, FP-10L ∗★★							100	100		See page1-26	
M5M5257P-35 ★★			256K×1		300	11	35	35	24P4Y	—	3—64
M5M5257P-45 ★★							45	45			
M5M5257P-55 ★★							55	55			
M5M5258P-35 ★★			64K×4		300	11	35	35			3—68
M5M5258P-45 ★★							45	45			
M5M5258P-55 ★★							55	55			

★ : New product ★★ : Under development ∗ : These devices are not published yet. Note : M5M5255P with double CS (without $\overline{OE}$)
† : AFP is not published yet.

■ECL RAM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ(mW)	Access time Max(ns)	Cycle time Min(ns)	Package outline	Inter-changeable products	Page
M10422S-5	Bipolar	1024	256×4	−5.2V ±5%	900	5	—	24S1F	See page 1-28	4—3
M10422S-7		1024	256×4		900	7	—			
M10474S-10 **		4096	1024×4		950	10	—			4—7
M10474S-15 **		4096	1024×4		950	15	—			

** : Under development

■MASK ROM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ (mW)	Access time Max (ns)	Cycle time Min (ns)	Package Outline	Inter-changeable products	Page
M5M2364-XXXP	NMOS			5±10%	200	250	—	28P4	See page 1-28	5—6
M5M23128-XXXP		128K	16K×8		200		—	28P4		5—10
M5M23256-XXXP		256K	32K×8				—			5—13
M5M231000-XXXP		1M	128K×8		150		—			5—16
M5M231001-XXXP		1M	128K×8		150	200	—		—	5—18
M5M23C100-XXXP	CMOS				100	200/250	—		See page 1-28	5—20
M5M23C400-XXXP *		4M	512K×8 256K×16			250	—	40P4		5—22
M5M23C400-XXXFP **							—	64P6W	—	—
M5M23C401-XXXP **			512K×8				—	32P4		

* : New product ** : Under development * : These devices are not published yet.

■EPROM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ (mW)	Access time Max (ns)	Cycle time Min (ns)	Package Outline	Inter-changeable products	Page
M5L2764K-2	NMOS	64K	8K×8	5±5%	300	200	—	28K1	See page 1-28	6—3
M5L2764K						250	—			
M5L27128K-2		128K	16K×8		350	200	—	28K4		6—10
M5L27128K-20 †						200	—			
M5L27128K						250	—			
M5L27128K-25 †						250	—			
M5M27C128K-15	CMOS				160	150	—		—	6—26
M5M27C128K-2						200	—			
M5M27C128K						250	—		See page1-28	
M5L27256K-15	NMOS	256K	32K×8		300	150	—		—	6—34
M5L27256K-2						200	—			
M5L27256K						250	—		See page 1-28	
M5M27C256K-12	CMOS	256K	32K×8		160	120	—			6—46
M5M27C256K-15						150	—			
M5M27C256K						250	—			
M5L27512K-17	NMOS	512K	64K×8		300	170	—		—	6—52
M5L27512K-2						200	—		See page 1-28	
M5L27512K						250	—			
M5M27C100K-15 *	CMOS	1M	128K×8		160	150	—	32K4	—	6—58
M5M27C100K-2 *						200	—		See page 1-28	
M5M27C100K *						250	—			
M5M27C101K-15 *						150	—		—	6—59
M5M27C101K-2 *						200	—		See page 1-28	
M5M27C101K *						250	—			
M5M27C102K-15 **			64K×16			150	—	40K4		6—60
M5M27C102K-2 **						200	—			
M5M27C102K **						250	—			

* : New product ** : Under development † : Supply voltage 5V±10%

■OTPROM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation (mW)	Access time Max (ns)	Cycle time Min (ns)	Package outline	Inter-changeable products	Page
M5M2764P	NMOS	64K	8K×8	5±5%	300	250	—	28P4 (P) 28P2W (FP)	See page 1-30	7—3
M5M27128P		128K	16K×8		350		—			7—10
M5M27256P, FP		256K	32K×8		300		—			7—18
M5M27512P, FP		512K	64K×8		300		—			7—24
M5M27C256P, FP *	CMOS	256K	32K×8		160	200				—
M5M27C100P * **		1M	128K×8			200		32P4	—	—
M5M27C101P * **										—

** : Under development * These devices are not published yet.

■EEPROM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ (mW)	Access time Max (ns)	Cycle time Min (ns)	Package Outline	Inter-changeable products	Page
M5M28C64P-15 **	CMOS	64K	8K×8	5±10%	100	150	—	28P4	—	8—3
M5M28C64P **						200	—			

** : Under development

■EAROM

Type	Structure	Memory capacity	Memory configuration (Word×Bit)	Supply voltage (V)	Typical power dissipation Typ(mW)	Access time Max (ns)	Cycle time Min(ns)	Package outline	Inter-changeable products	Page
M58658P	MNOS	320	20×16	※1	200	20μs	—	14P4	—	9—31
M58659P		512	32×16	※1			—		—	9—39
M58653P		700	50×14	※1			—		—	9—11
M58655P		1024	64×16	※1			—		—	9—17
M58657P		1400	100×14	※1			—		—	9—25
M5G1400P				※2			—		See page 1-30	9—47
M58630P		2048	128×16	※1			—		—	9—3

※1 : $V_{GG}-V_{SS}=-35V\pm8\%$ $V_{SS}-V_{GND}=5V\ ^{+20\%}_{-\ 5\%}$

※2 : $V_{GG}-V_{SS}=-35V\pm8\%$

GUIDE TO INTERCHANGEABILITY

	Mitsubishi Electric	AMD Advanced Micro Devices	GI General Instrument	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
DYNAMIC RAM	**M5K4164AP-12**				MB8265A-12	HM4865AP-12		
	M5K4164AP-15				MB8265A-15	HM4865AP-15		
	M5K4164ANP-12				MB8264A-12	HM4864AP-12		
	M5K4164ANP-15				MB8264A-15	HM4864AP-15		
	M5K4164ANL-12							
	M5K4164ANL-15							
	M5M4416P-12				MB81416-12	HM48416AP-12		
	M5M4416P-15				MB81416-15	HM48416AP-15		
	M5M4256P-10							
	M5M4256P-12				MB81256-12	HM50256P-12		
	M5M4256P-15				MB81256-15	HM50256P-15		
	M5M4257P-10							
	M5M4257P-12				MB81257-12	HM50257P-12		
	M5M4257P-15				MB81257-15	HM50257P-15		
	M5M4256J-10							
	M5M4256J-12				MB81256-12	HM50256CP-12		
	M5M4256J-15				MB81256-15	HM50256CP-15		
	M5M4257J-10							
	M5M4257J-12				MB81257-12	HM50257CP-12		
	M5M4257J-15				MB81257-15	HM50257CP-15		
	M5M4256L-10							
	M5M4256L-12				MB81256-12			
	M5M4256L-15				MB81256-15			
	M5M4257L-10							
	M5M4257L-12				MB81257-12			
	M5M4257L-15				MB81257-15			
	M5M4464P-10				MB81464-10			
	M5M4464P-12				MB81464-12	HM50464P-12		
	M5M4464P-15				MB81464-15	HM50464P-15		
	M5M4464L-10							
	M5M4464L-12							
	M5M4464L-15							
	M5M4C264P-12				MB81461-12	HM53461-12		
	M5M4C264P-15				MB81461-15	HM53461-15		
	M5M4C264L-12							
	M5M4C264L-15							
	MH25608J-10							
	MH25608J-12							
	MH25608J-15							
	MH25608JA-10							
	MH25608JA-12							
	MH25608JA-15							
	MH25609J-10							
	MH25609J-12					HM561003B-12		
	MH25609J-15					HM561003B-15		
	MH25609JA-10							
	MH25609JA-12					HM561003A-12		
	MH25609JA-15					HM561003A-15		

GUIDE TO INTERCHANGEABILITY

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
MK4164N-15							
			µPD4164C-12				
MK4564N-15			µPD4164C-15		TMS4164-15NLJ	TMM4164P-3	
			µPD41416C-12		TMS4416-12NL		
			µPD41416C-15		TMS4416-15NL		
MK4556-12	MCM6256P-12		µPD41256C-12	MSM41256-12RS	TMS4256-12NL	TMM41256P-12	
MK4556-15	MCM6256P-15		µPD41256C-15	MSM41256-15RS	TMS4256-15NL	TMM41256P-15	
	MCM6257P-12			MSM41257-12RS	TMS4257-12NL	TMM41257P-12	
	MCM6257P-15		µPD41257C-15	MSM41257-15RS	TMS4257-15NL	TMM41257P-15	
			µPD41256L-12			TMM41256T-12	
			µPD41256L-15			TMM41256T-15	
			µPD41264C-12			TMM41257T-12	
			µPD41264C-15			TMM41257T-15	
	MCM6644		µPD41464C-12		TMS4464-12NL	TMM41464P-12	
			µPD41464C-15		TMS4464-15NL	TMM41464P-15	
			µPD41264C-12				
			µPD41264C-15				
			MC-41256A8B-12				
			MC-41256A8B-15				
			MC-41256A8A-12				
			MC-41256A8A-15				
			MC-41256A9B-12				
			MC-41256A9B-15				
			MC-41256A9A-12				
			MC-41256A9A-15				

GUIDE TO INTERCHANGEABILITY

	Mitsubishi Electric	AMD Advanced Micro Devices	GI General Instrument	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
DYNAMIC RAM	**M5M4C1000P-10**				MB81C1000-10	HM511000P-10		
	M5M4C1000P-12				MB81C1000-12	HM511000P-12		
	M5M4C1000P-15				MB81C1000-15	HM511000P-15		
	M5M4C1001P-10				MB81C1001-10	HM511001P-10		
	M5M4C1001P-12				MB81C1001-12	HM511001P-12		
	M5M4C1001P-15				MB81C1001-15	HM511001P-15		
	M5M4C1002P-10					HM511002P-10		
	M5M4C1002P-12					HM511002P-12		
	M5M4C1002P-15					HM511002P-15		
	M5M4C1000J-10				MB81C1000-10			
	M5M4C1000J-12				MB81C1000-12			
	M5M4C1000J-15				MB81C1000-15			
	M5M4C1001J-10				MB81C1001-10			
	M5M4C1001J-12				MB81C1001-12			
	M5M4C1001J-15				MB81C1001-15			
	M5M4C1002J-10							
	M5M4C1002J-12							
	M5M4C1002J-15							
	M5M4C1000L-10				MB81C1000-10			
	M5M4C1000L-12				MB81C1000-12			
	M5M4C1000L-15				MB81C1000-15			
	M5M4C1001L-10				MB81C1001-10			
	M5M4C1001L-12				MB81C1001-12			
	M5M4C1001L-15				MB81C1001-15			
	M5M4C1002L-10							
	M5M4C1002L-12							
	M5M4C1002L-15							
	M5M44C256P-10							
	M5M44C256P-12							
	M5M44C256P-15							
	M5M44C258P-10							
	M5M44C258P-12							
	M5M44C258P-15							
	M5M44C256J-10							
	M5M44C256J-12							
	M5M44C256J-15							
	M5M44C258J-10							
	M5M44C258J-12							
	M5M44C258J-15							
	M5M44C256L-10							
	M5M44C256L-12							
	M5M44C256L-15							
	M5M44C258L-10							
	M5M44C258L-12							
	M5M44C258L-15							
	MH1M08J-10							
	MH1M08J-12							
	MH1M08J-15							

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
			μPD421000C-10			TC511000P-10	
			μPD421000C-12			TC511000P-12	
			μPD421001C-10			TC511001P-10	
			μPD421001C-12			TC511001P-12	
			μPD421002C-10			TC511002P-10	
			μPD421002C-12			TC511002P-12	
			μPD421000LA-10			TC511000J-10	
			μPD421000LA-12			TC511000J-12	
			μPD421001LA-10			TC511001J-10	
			μPD421001LA-12			TC511001J-12	
			μPD421002LA-10			TC511002J-10	
			μPD421002LA-12			TC511002J-12	
						TC514256P-10	
						TC514256P-12	
						TC514258P-10	
						TC514258P-12	
						TC514256J-10	
						TC514256J-12	
						TC514258J-10	
						TC514258J-12	

	Mitsubishi Electric	AMD Advanced Micro Devices	GI General Instrument	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
DYNAMIC RAM	MH1M08JA-10							
	MH1M08JA-12							
	MH1M08JA-15							
	MH1M09J-10							
	MH1M09J-12							
	MH1M09J-15							
	MH1M09JA-10							
	MH1M09JA-12							
	MH1M09JA-15							

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks

GUIDE TO INTERCHANGEABILITY

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
STATIC RAM	M5M21C67P-35				MB81C67-35	HM6267-35		
	M5M21C67P-45				MB81C67-45	HM6267-45		
	M5M21C67P-55				MB81C67-55			
	M5M21C68P-35				MB81C68-35	HM6268-35		
	M5M21C68P-45				M B81C68-45	HM6168H-45		
	M5M21C68P-55					HM6168H-55		
	M5M5165P-70, -70L				MB8464A-70			
	M5M5165P-10, -10L				MB8464A-10	HM6264-10		
	M5M5165P-12, -12L				MB8464A-12	HM6264-12		
	M5M5165FP-70, -70L				MB8464A-70			
	M5M5165FP-10, -10L				MB8464A-10	HM6264FP-10		
	M5M5165FP-12, -12L				MB8464A-12	HM6264FP-12		
	M5M5187P-45				MB81C71-45	HM6287-45		
	M5M5187P-55				MB81C71-55	HM6287-55		
	M5M5187AP-25					HM6787-25		
	M5M5187AP-35							
	M5M5188P-45				MB81C74-45	HM6288-45		
	M5M5188P-55				MB81C74-55	HM6288-55		
	M5M5188AP-25							
	M5M5188AP-35					HM6788-30		
	M5M5189AP-25							
	M5M5189AP-35							
	M5M5179P-35							
	M5M5179P-45				MB81C79-45			
	M5M5179P-55				MB81C79-55			
	M5M5178P-35							
	M5M5178P-45				MB81C78-45			
	M5M5178P-55				MB81C78-55			
	M5M5256P-10, -10L				MB84256-10	HM62256-10		
	M5M5256P-12, -12L				MB84256-12	HM62256-12		
	M5M5256P-15, -15L				MB84256-15	HM62256-15		
	M5M5256FP-10, -10L				MB84256-10	HM62256FP-10		
	M5M5256FP-12, -12L				MB84256-12	HM62256FP-12		
	M5M5256FP-15, -15L				MB84256-15	HM62256FP-15		
	M5M5256AP-70, -70L							
	M5M5256AP-85, -85L					HM62256-8		
	M5M5256AP-10, -10L					HM62256-10		
	M5M5255P-70, -70L							
	M5M5255P-85, -85L							
	M5M5255P-10, -10L							
	M5M5257P-35							
	M5M5257P-45							
	M5M5257P-55							
	M5M5258P-35							
	M5M5258P-45							
	M5M5258P-55							

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
			μPD4311C-35				
			μPD4311C-45				
			μPC4311C-55				
			μPD4314C-35				
			μPD4314C-45				
			μPD4314C-55				
			μPD4364C-10				
			μPD4364C-12	MSM5165-12RS		TC5565P-12	
			μPD4364G-10				
			μPD4364G-12			TC5565FP-12	
			μPD4361C-45			TC5562-45	
			μPD4361C-55			TC5562-55	
			μPD4362C-45				
			μPD4362C-55				
						TMM2089-35	
						TMM2089-45	
						TMM2089-55	
			μPD43256C-10	SRM20256-10		TC55257-10	
			μPD43256C-12	SRM20256-12		TC55257-12	
			μPD43256C-15				
				SRM20256LM-10			
				SRM20256LM-12			
			μPD43257C-10				

GUIDE TO INTERCHANGEABILITY

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
ECL RAM	**M10422S-5**				MBM10422A-5			
	M10422S-7				MBM10422A-7	HM10422-7		
	M10474S-10					HM10474-10		
	M10474S-15				MBM10474A-15	HM10474-15		

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
MASK ROM	**M5M2364-XXXP**					HN61364		
	M5M23128-XXXP					HN613128		
	M5M23256-XXXP				MB83256	HN61256		
	M5M231000-XXXP							
	M5M231001-XXXP							
	M5M23C100-XXXP				MB831024	HN62301		
	M5M23C400-XXXP					HN62404		
	M5M23C400-XXXFP							
	M5M23C401-XXXP							

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
EPROM	**M5L2764K-2**				MBM2764-20		D2764-2	
	M5L2764K				MBM2764-25	HN482764G	D2764	
	M5L27128K-2							
	M5L27128K-20				MBM27128-20			
	M5L27128K	Am27128-25				HN4827128-25	D27128	
	M5L27128K-25				MBM27128-25			
	M5M27C128K-2							
	M5M27C128K-15							
	M5M27C128K				MBM27C128-25		D27128	
	M5M27C256K-12							
	M5M27C256K-15							
	M5M27C256K				MBM27C256A-25	HN27C256G-25	D27256	
	M5L27256K-15							
	M5L27256K-2							
	M5L27256K				MBM27256-25	HM27256G-25	D27256	
	M5L27512K-17							
	M5L27512K-2							
	M5L27512K	Am27512				HN27512G-25	D27512	
	M5M27C100K-15							
	M5M27C100K-2				MBM27C1000-20	HN27C301G-20		
	M5M27C100K				MBM27C1000-25	HN27C301G-25		
	M5M27C101K-15							
	M5M27C101K-2				MBM27C1001-20	HN27C101G-20		
	M5M27C101K				MBM27C1001-25	HN27C101G-25		
	M5M27C102K-15					HN27C1024G-15		
	M5M27C102K-2				MBM27C1024-20	HN27C1024G-20		
	M5M27C102K	Am27C1024			MBM27C1024-25			

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
			μPB10422D-7				
			μPB10474D-10				
	MCM10474-15		μPB10474D-15				

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
MK37000			μPD2364	MSM3864	TMS4764	TMM2365P	
			μPD23128	MSM38128A	TMS47128	TMM23128P	
MK38000			μPD23256	MSM38256A		TMM23256P	
			μPD231000				28pin
			μPD23C1000	MSM531000			
							40pin
							64pin
							32pin

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	Remarks
						TMM2764D-2	
MK2764-8			μPD2764D	MSM2764AS		TMM2764D	
			μPD27128D-2			TMM27128D-20	
			μPD27128D			TMM27128D-25	
			μPD27C256AD-12				
			μPD27C256AD-15			TC57256AD-15	
						TMM27512D-20	
						TMM27512D-25	
						TC571001D-20	
						TC571001D-25	
						TC571000D-20	
						TC571000D-25	
		NMC27C1024Q150	μPD27C1024D-15				
		NMC27C1024Q200	μPD27C1024D-20				
			μPD27C1024D-25				

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
OTPPOM	M5M2764P					HN482764P		
	M5M27128P							
	M5M27256P				MBM27256P-25	HN27256P-25	P27256	
	M5M27512P					HN27512P-25	P27512	
	M5M27C256P					HN270256P		
	M5M27C100P							
	M5M27C101P							

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
EEPROM	M5M28C64P							

	Mitsubishi Electric	AMD Advanced Micro Devices	AMI American Microsystems	FSC Fairchild Semiconductor	Fujitsu	Hitachi	INTEL Intel	INTERSIL Intersil
EAROM	M58630P							
	M58653P							
	M58655P							
	M58657P							
	M5G1400P							
	M58658P							
	M58659P							

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	GI General Instrument
			μPD2764C				
			μPD27128C				
						TMM24256AP	
						TMM24512P	
			μPD27C256C			TC54256P	

MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	GI General Instrument

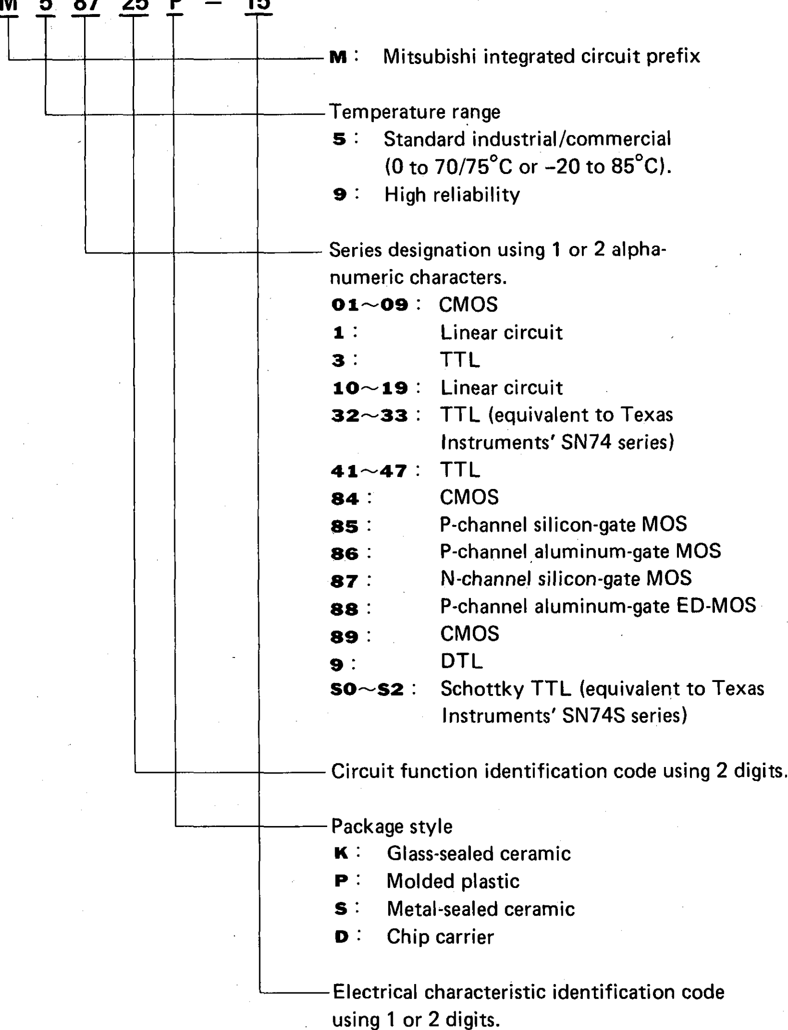
MOSTEK Mostek	MOTOROLA Motorola Semiconductor products	NSC National Semiconductor	Nippon Electric	Oki	TI Texas Instruments	Toshiba	GI General Instrument
							ER1400

ORDERING INFORMATION

FUNCTION CODE

Mitsubishi integrated circuits may be ordered using the following simplified alphanumeric type-codes which define the function of the ICs and the package style.

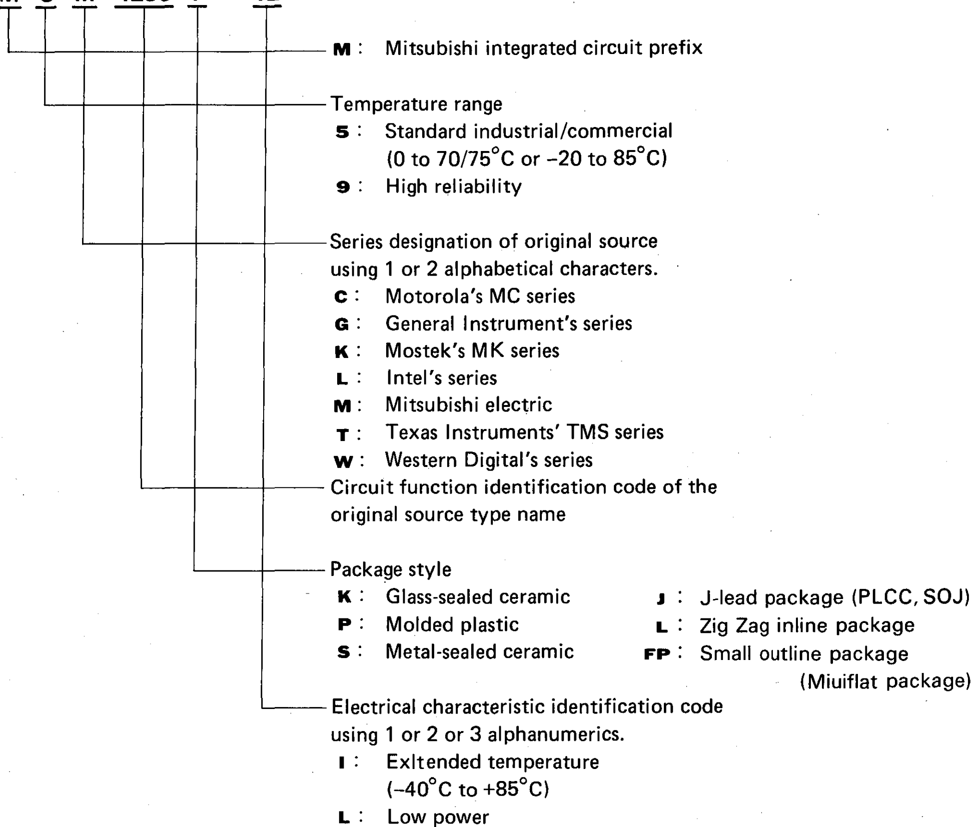
For Mitsubishi Original Products



ORDERING INFORMATION

For Second Source Products

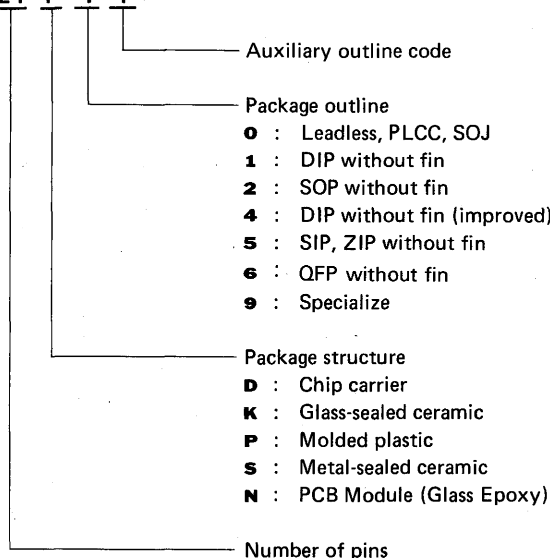
Example:



PACKAGE CODE

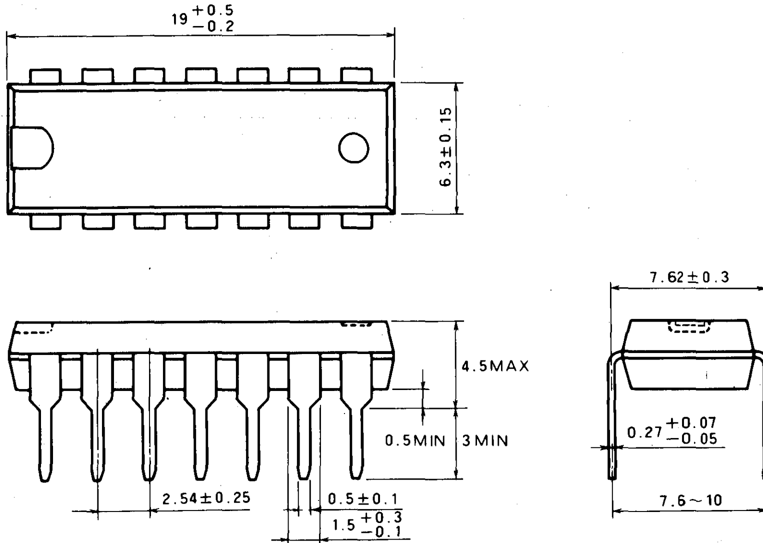
Package style may be specified by using the following simplified alphanumeric code.

Example:



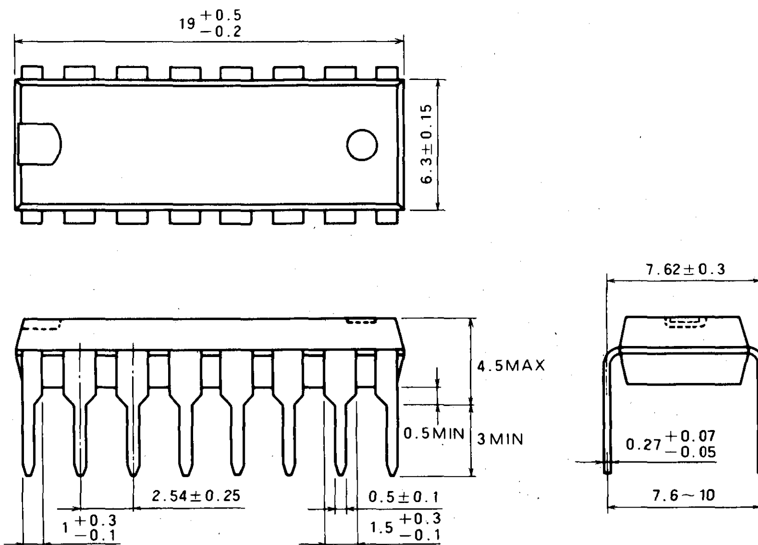
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



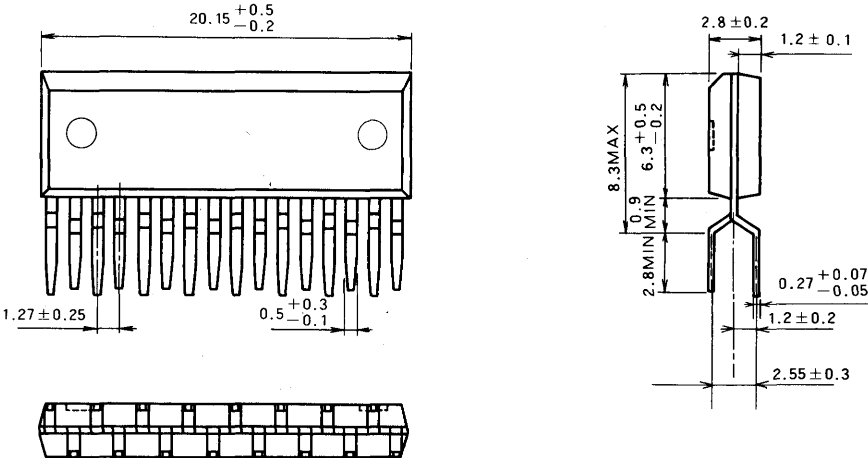
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



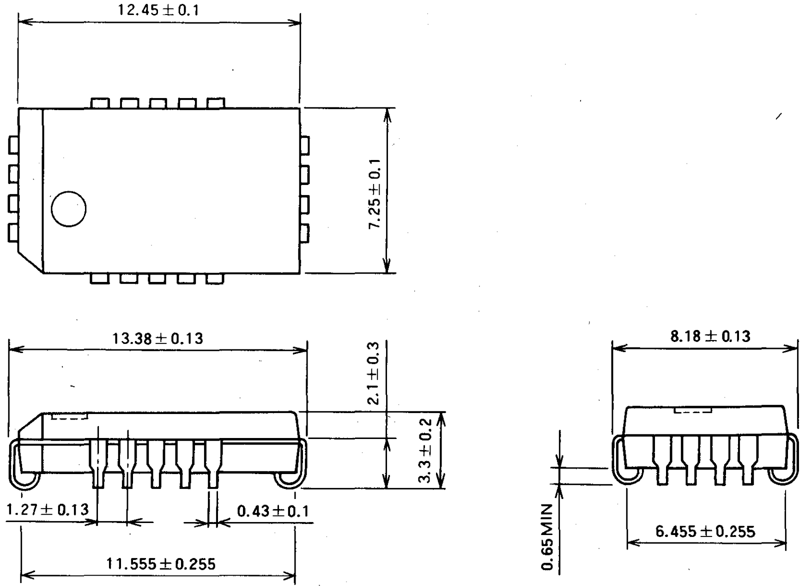
TYPE 16P5A 16-PIN MOLDED PLASTIC ZIP

Dimension in mm



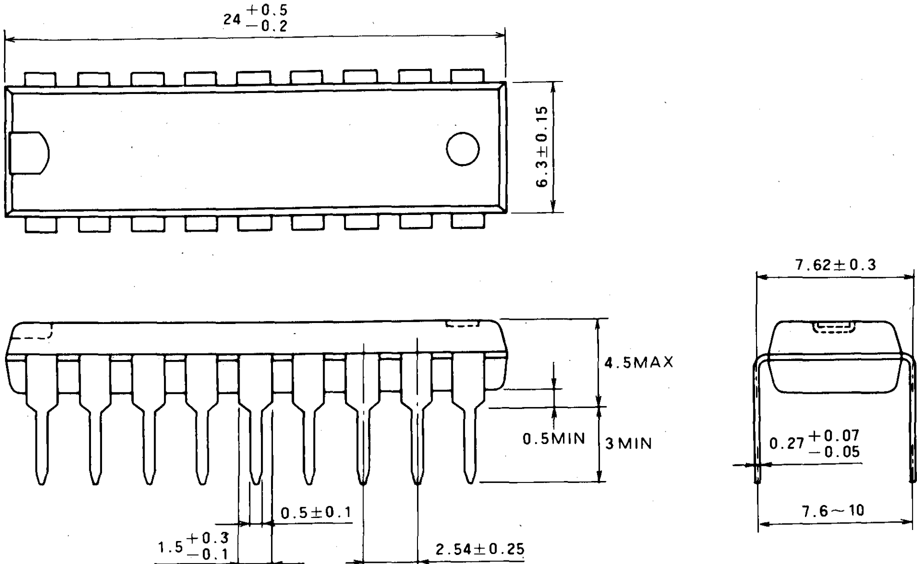
TYPE 18P0A 18-PIN MOLDED PLASTIC LEADLED CHIP CARRIER

Dimension in mm



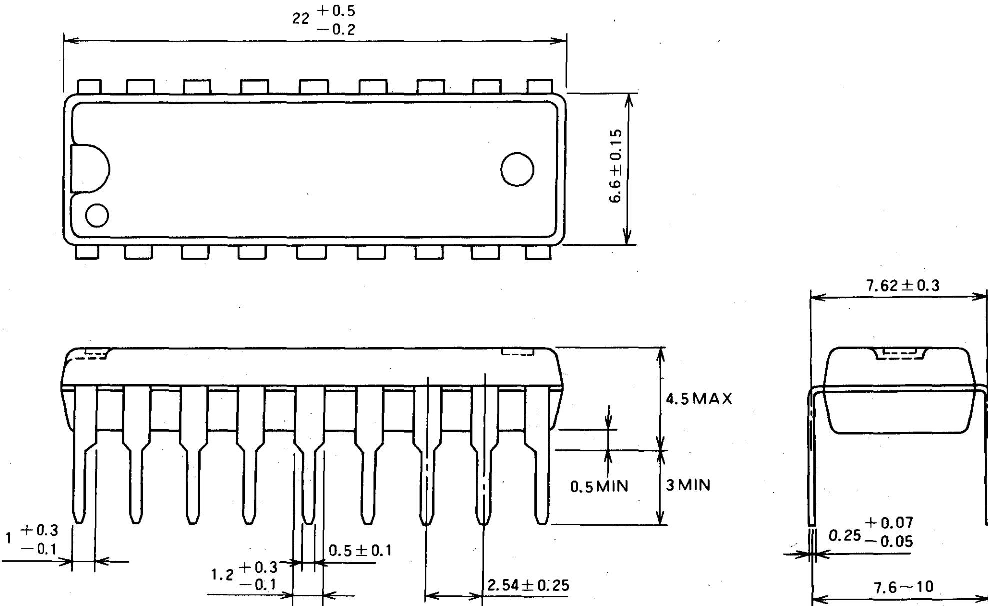
TYPE 18P4 18-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 18P4H 18-PIN MOLDED PLASTIC DIP

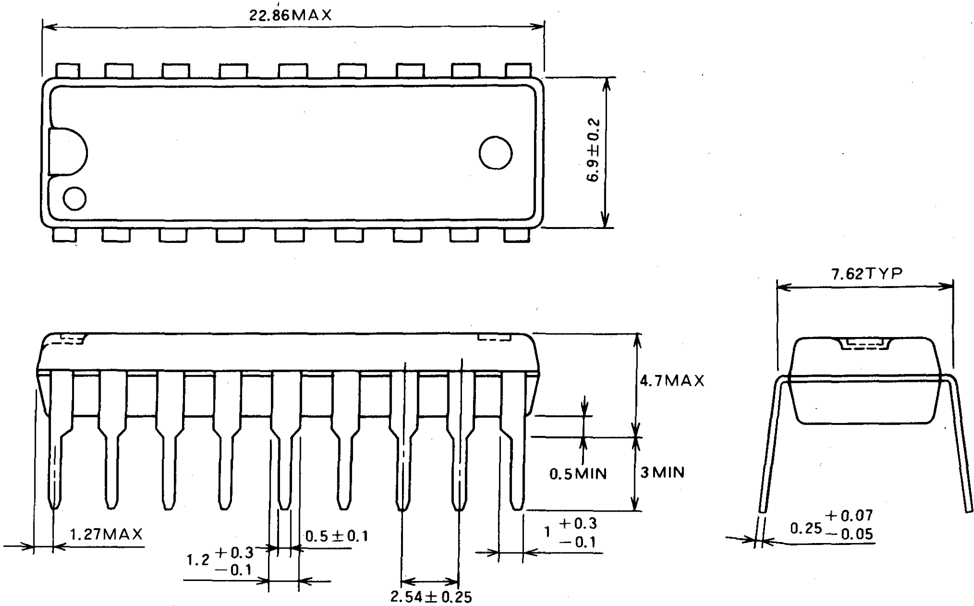
Dimension in mm



MITSUBISHI ELECTRIC

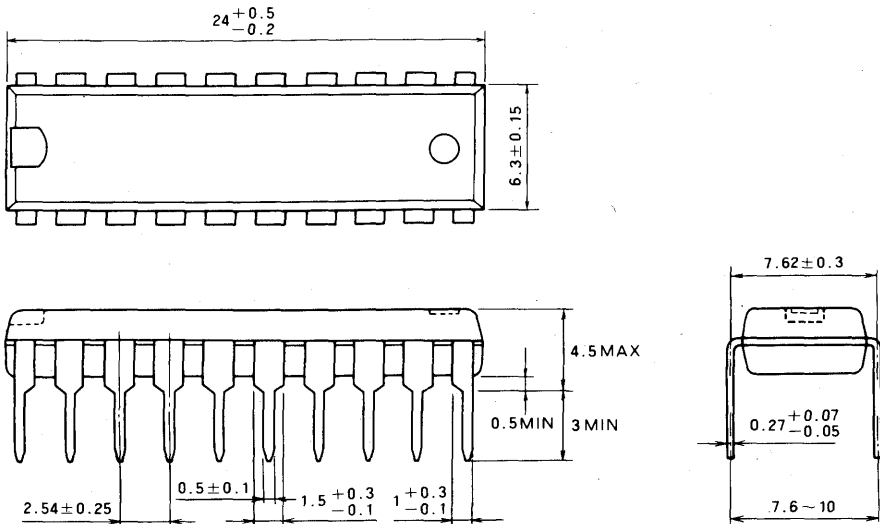
TYPE 18P4Y 18-PIN MOLDED PLASTIC DIP

Dimension in mm



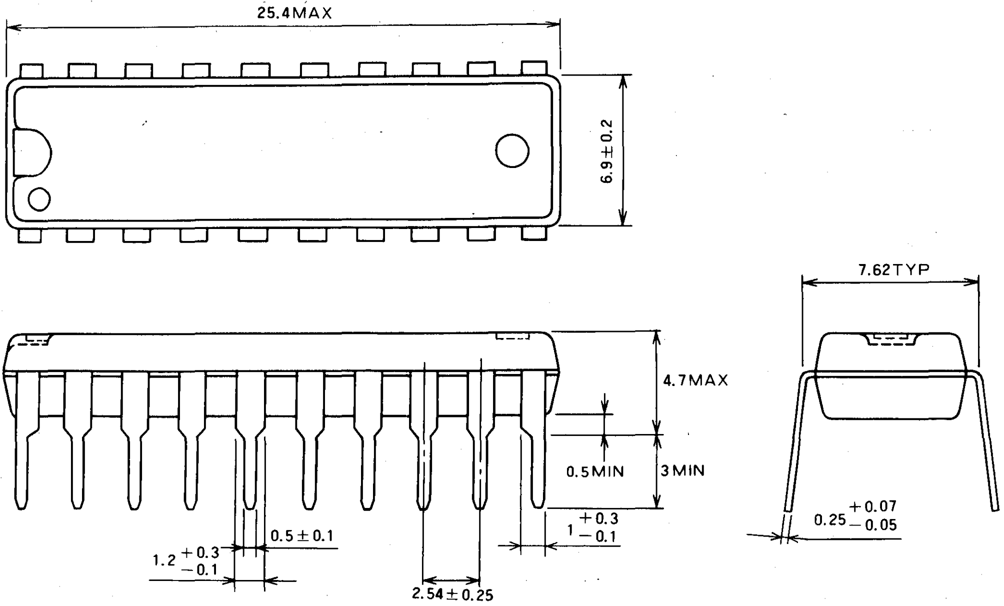
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



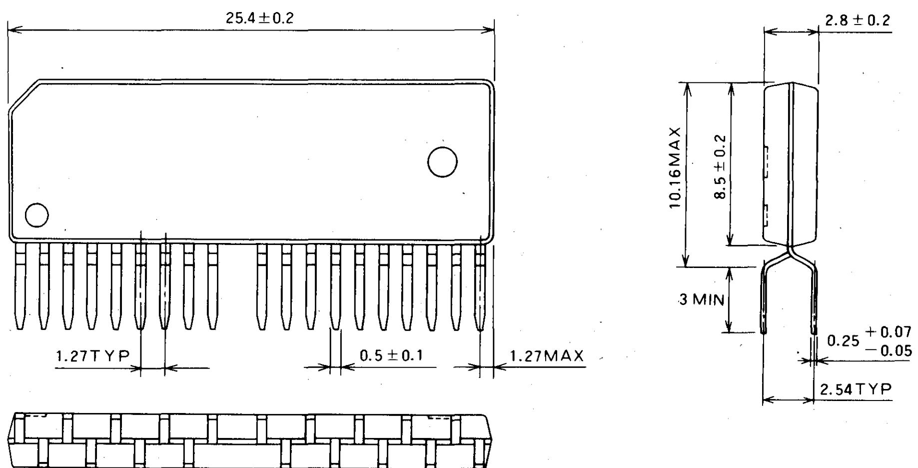
TYPE 20P4Y 20-PIN MOLDED PLASTIC DIP

Dimension in mm



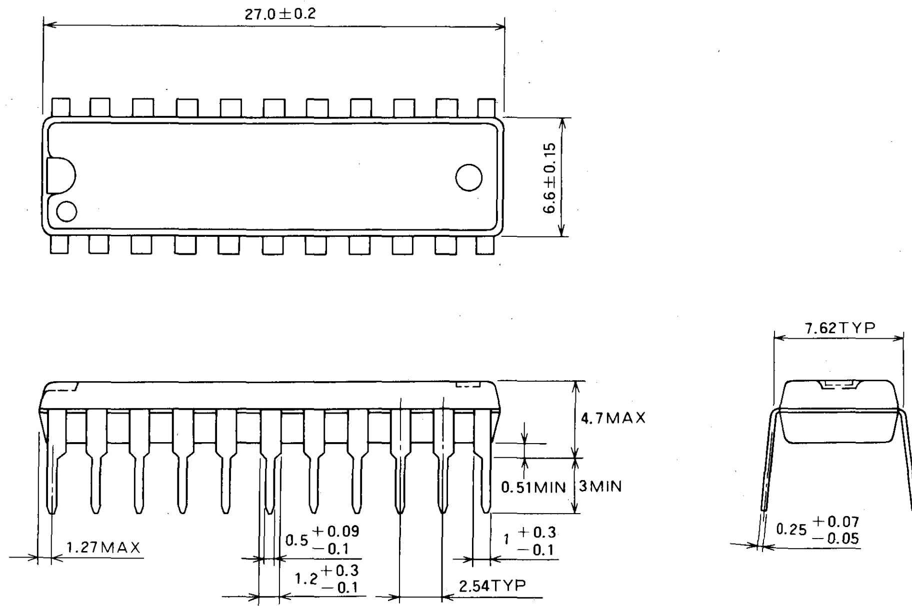
TYPE 20P5L 20-PIN MOLDED PLASTIC ZIP

Dimension in mm



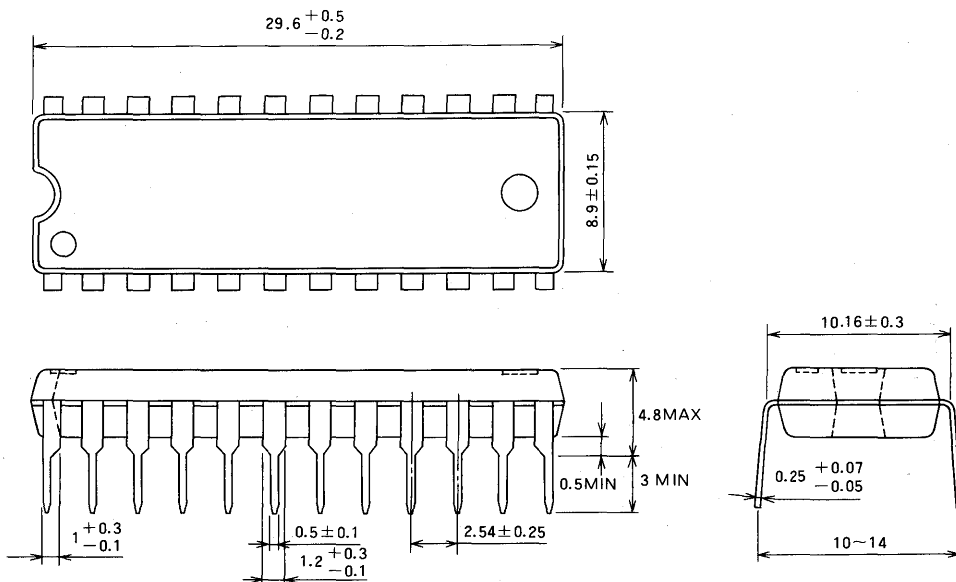
TYPE 22P4H 22-PIN MOLDED PLASTIC DIP

Dimension in mm



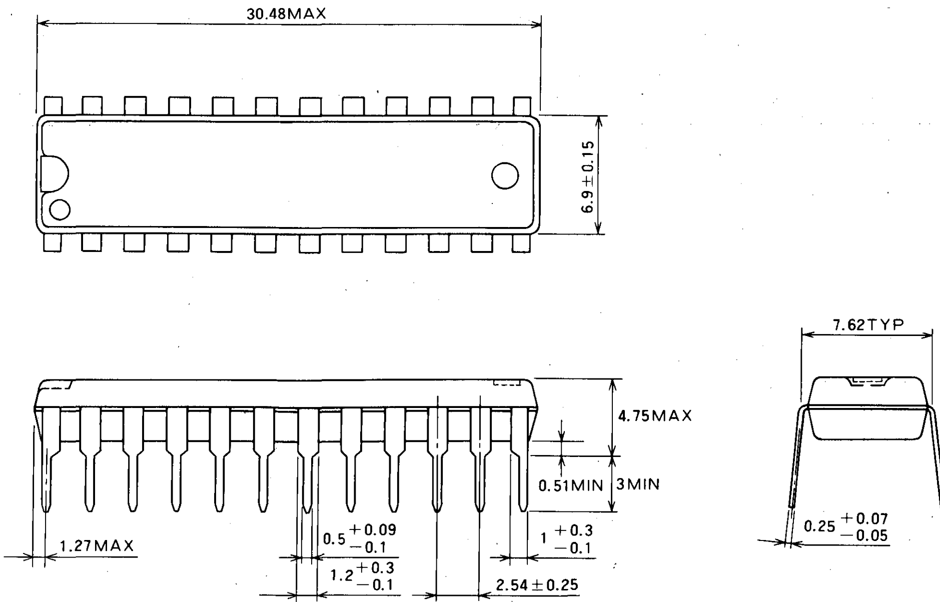
TYPE 24P4F 24-PIN MOLDED PLASTIC DIP

Dimension in mm



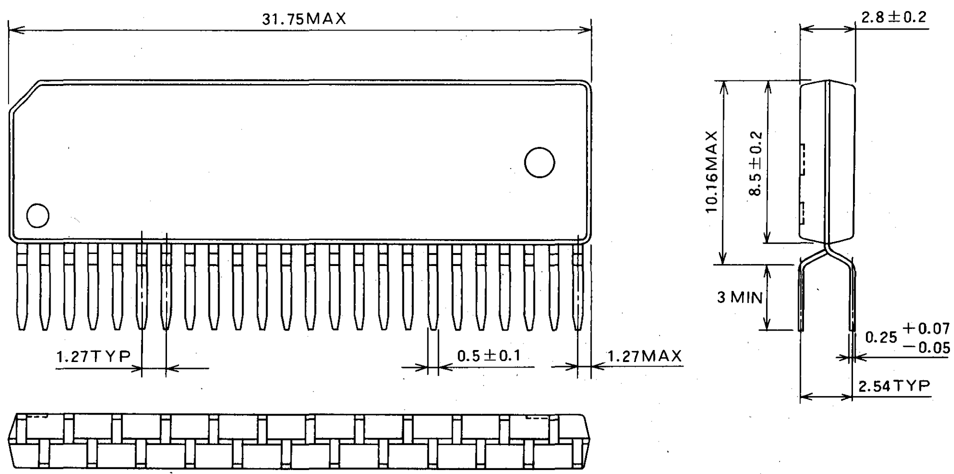
TYPE 24P4Y 24-PIN MOLDED PLASTIC DIP

Dimension in mm



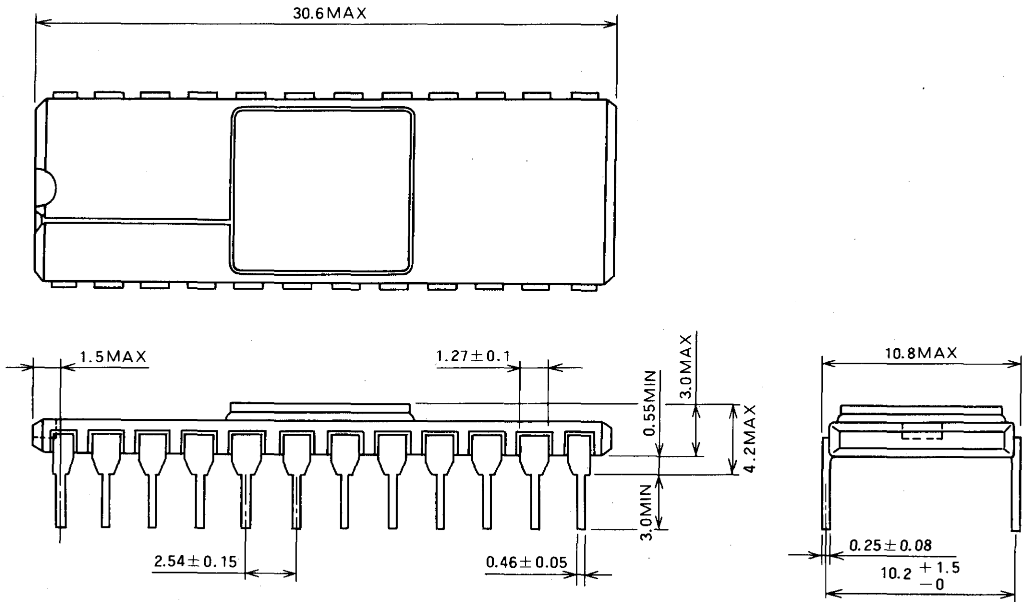
TYPE 24P5L 24-PIN MOLDED PLASTIC ZIP

Dimension in mm



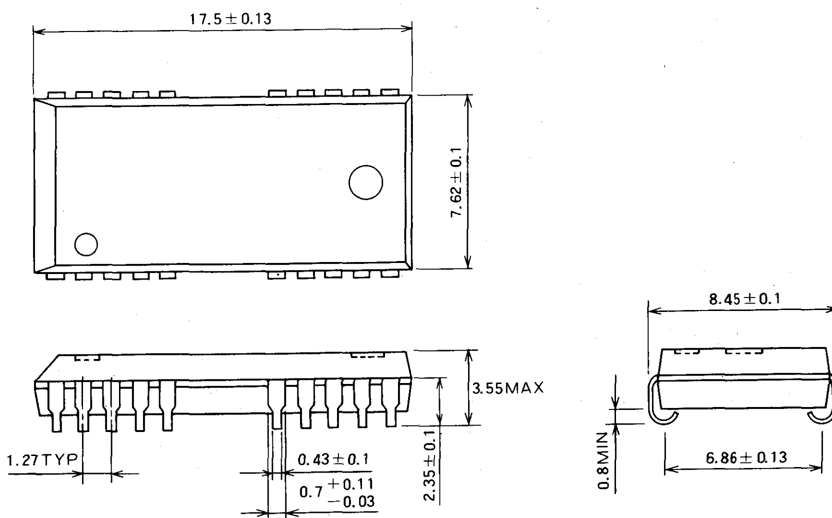
TYPE 24S1F 24-PIN CERAMIC DIP

Dimension in mm



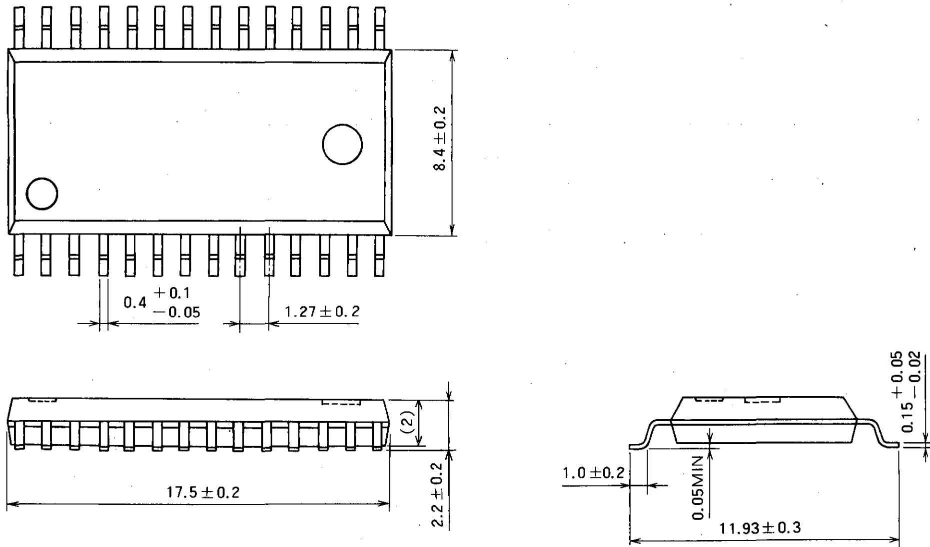
TYPE 26P0J 26-PIN MOLDED PLASTIC SOJ

Dimension in mm



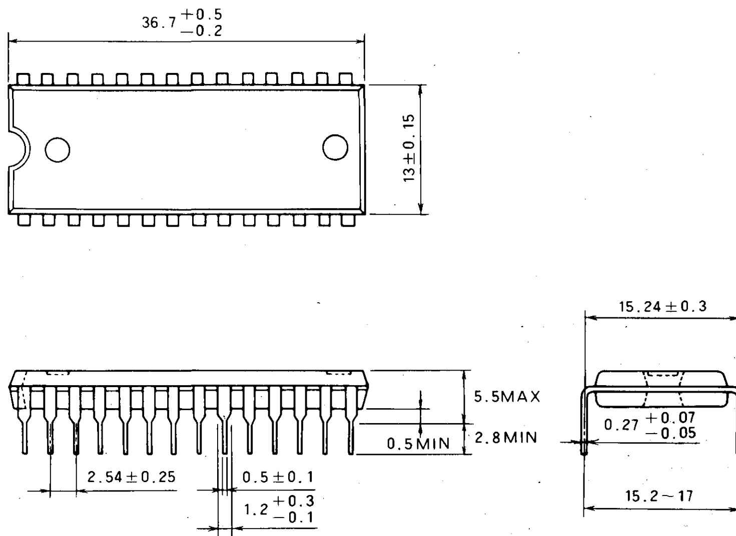
TYPE 28P2W 28-PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 28P4 28-PIN MOLDED PLASTIC DIP

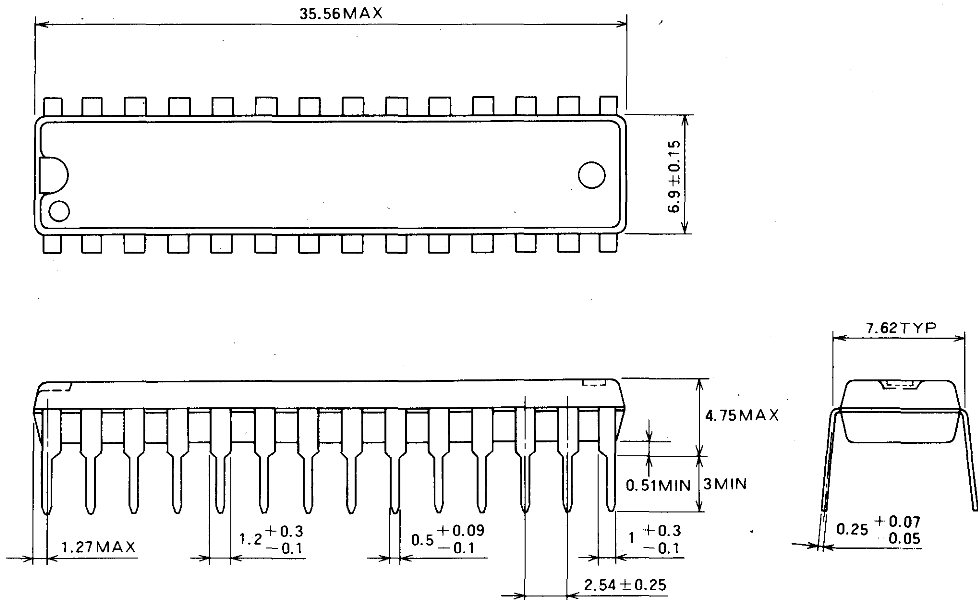
Dimension in mm



MITSUBISHI ELECTRIC

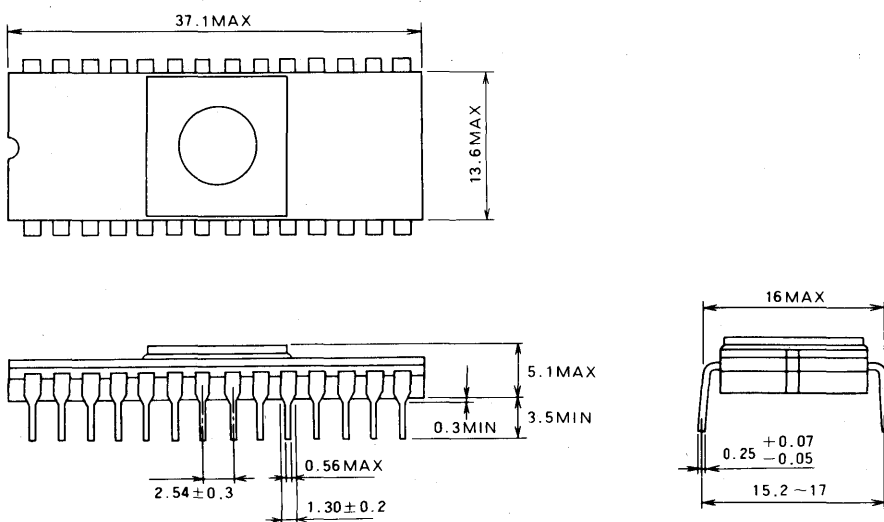
TYPE 28P4Y 28-PIN MOLDED PLASTIC DIP

Dimension in mm

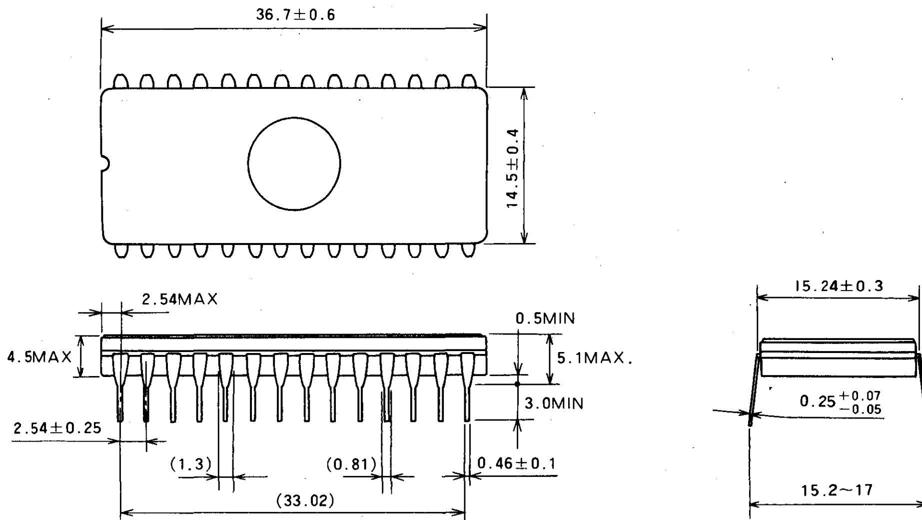


TYPE 28K1 28-PIN GLASS-SEALED CERAMIC DIP WITH TRANSPARENT LID

Dimension in mm

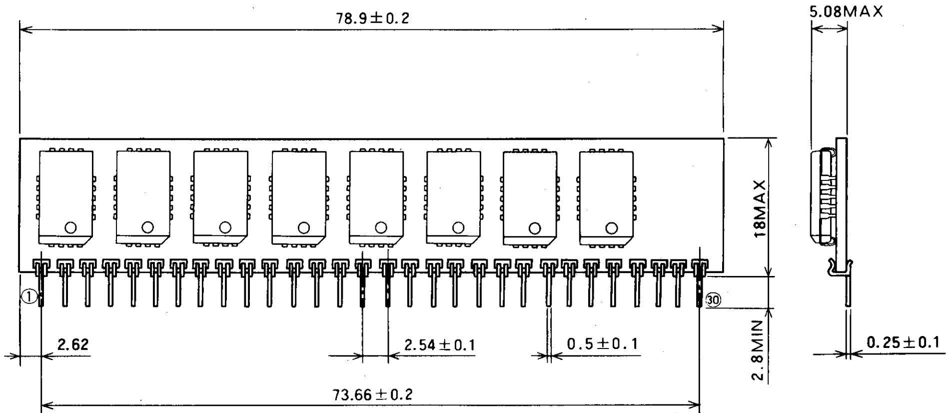


TYPE 28K4 28-PIN GLASS-SEALED CERAMIC DIP WITH TRANSPARENT LID Dimension in mm



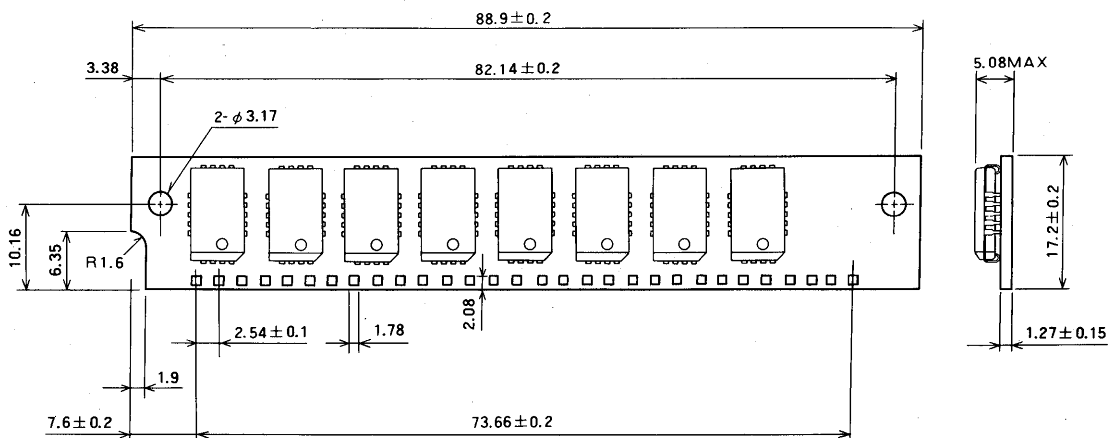
TYPE 30N5 30-PIN MEMORY MODULE (MH25608JA)

Dimension in mm



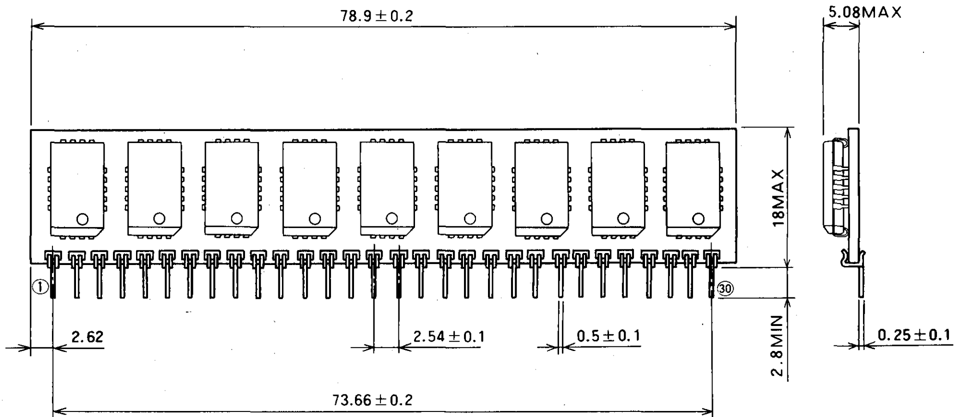
TYPE 30N9 30-PIN MEMORY MODULE (MH25608J)

Dimension in mm



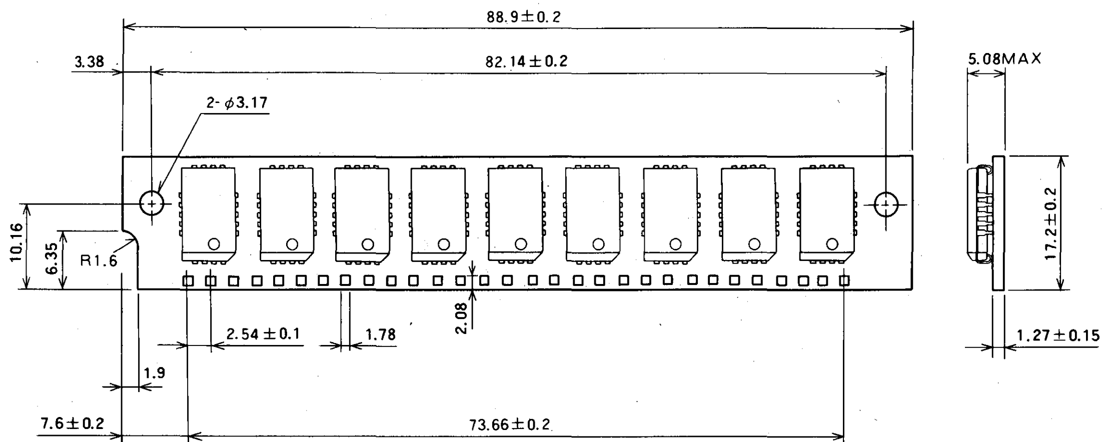
TYPE 30N5 30-PIN MEMORY MODULE (MH25609JA)

Dimension in mm

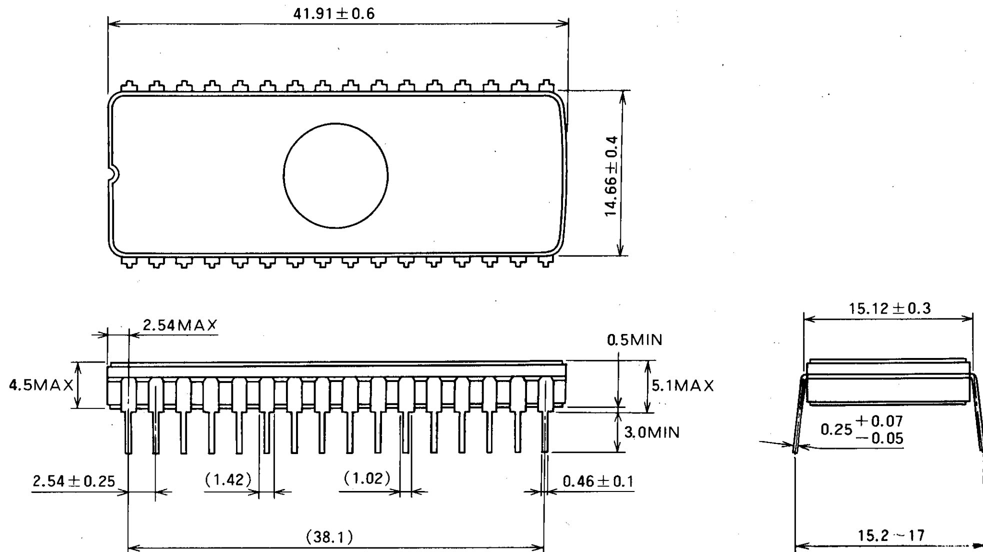


TYPE 30N9 30-PIN MEMORY MODULE (MH25609J)

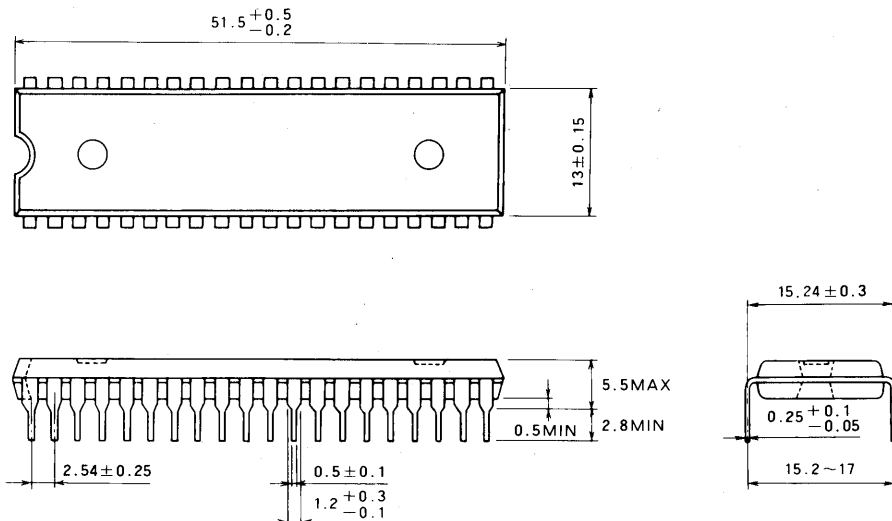
Dimension in mm



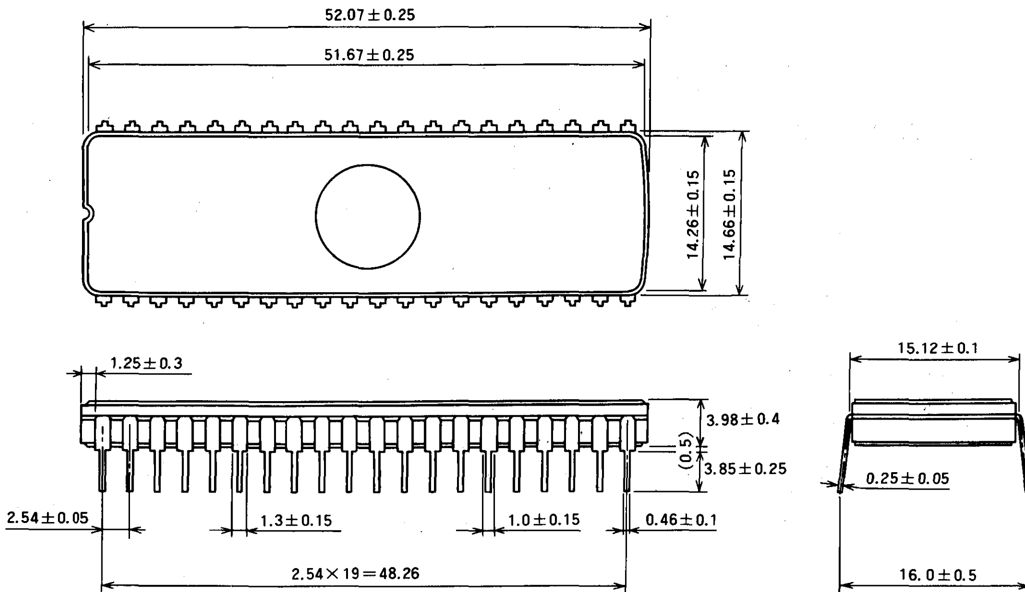
TYPE 32K4A 32-PIN GLASS-SEALED CERAMIC DIP WITH TRANSPARENT LID Dimension in mm



TYPE 40P4 40-PIN MOLDED PLASTIC DIP Dimension in mm



TYPE 40K4A 40-PIN GLASS-SEALED CERAMIC DIP WITH TRANSPARENT LID Dimension in mm



MITSUBISHI ELECTRIC

LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip micro-computers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by a general symbol of the form:-

$t_{A(BC-DC)F}$ .... (1)

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

Note 1: Subscripts A to F may each consists of one or more letters.
2: Subscripts D and E are not used for transition times.
3: The "–" in the symbol (1) above is used to indicate "to"; hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times. Where no misunderstanding can occur the hyphen may be omitted.

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or t_{AF} – no brackets are used in this case

or t_{A}

or t_{BC-DE} – often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter)

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

b) those that are characteristics of the memory. The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.
All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	p
Recovery time	rec
Transition time	t
Valid time	v

Note: Recovery time for use as a characteristic is limited to sense recovery time.

4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.
All subscripts B and D should be in upper-case.

Signal or terminal	*Subscript*
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E
Erasure	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1: In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used.
2: It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z. (See clause 5)
3: If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter.

5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.
When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.
All subscripts C and E should be in upper-case.

Examples	Subscript Full	Subscript Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note: Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion.

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter—definition
C_i		Input capacitance
C_o		Output capacitance
$C_{i/o}$		Input/output terminal capacitance
$C_{i(\phi)}$		Input capacitance of clock input
f		Frequency
$f_{(\phi)}$		Clock frequency
I		Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from Vcc
$I_{CC(AV)}$		Avarage supply current from Vcc
$I_{CC(PD)}$		Power-down supply current from Vcc
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_I		Input current
I_{IH}		High-level input current—the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low-level input current—the value of the input current when V_{OL} is applied to the input considered
I_{OH}		High-level output current—the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current—the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current—the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off-state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low-level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
Pd		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_i		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_{a(A)}$	$t_{a(AD)}$	Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CAS)}$		Column address strobe access time
$t_{a(E)}$	$t_{a(CE)}$	Chip enable access time
$t_{a(G)}$	$t_{a(OE)}$	Output enable access time
$t_{a(PR)}$		Data access time after program
$t_{a(RAS)}$		Row address strobe access time
$t_{a(S)}$	$t_{a(CS)}$	Chip select access time
t_C		Cycle time
t_{CR}	$t_{C(RD)}$	Read cycle time—the time interval between the start of a read cylce and the start of the next cycle
t_{CRF}	$t_{C(REF)}$	Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_{C(PG)}$	Page-mode cycle time
t_{CRMW}	$t_{C(RMR)}$	Read-modify-write cycle time—the time interval between teh start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_{C(WR)}$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle

SYMBOLOGY

New symbol	Former symbol	Parameter—definition
t_{d}		Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$		Delay time between clock pulses—e.g., symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_{d(CAS-RAS)}$		Delay time, column address strobe to row address strobe
$t_{d(CAS-W)}$	$t_{d(CAS-WR)}$	Delay time, column address strobe to write
$t_{d(RAS-CAS)}$		Delay time, row address strobe to column address strobe
$t_{d(RAS-W)}$	$t_{d(RAS-WR)}$	Delay time, row address strobe to write
$t_{dis(R-Q)}$	$t_{dis(R-DA)}$	Output disable time after read
$t_{dis(S)}$	$t_{PXZ(CS)}$	Output disable time after chip select
$t_{dis(W)}$	$t_{PXZ(WR)}$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven and loaded by specified networks.
t_{DLH}		Low-level to high-level delay time
$t_{en(A-Q)}$	$t_{PZV(A-DQ)}$	Output enable time after address
$t_{en(R-Q)}$	$t_{PZV(R-DQ)}$	Output enable time after read
$t_{en(S-Q)}$	$t_{PZX(CS-DQ)}$	Output enable time after chip select
t_{f}		Fall time
t_{h}		Hold time—the interval time during which a signal at a specified input terminal after an active transition occurs at another specified input terminal
$t_{h(A)}$	$t_{h(AD)}$	Address hold time
$t_{h(A-E)}$	$t_{h(AD-CE)}$	Chip enable hold time after address
$t_{h(A-PR)}$	$t_{h(AD-PRO)}$	Program hold time after address
$t_{h(CAS-CA)}$		Column address hold time after column address strobe
$t_{h(CAS-D)}$	$t_{h(CAS-DA)}$	Data-in hold time after column address strobe
$t_{h(CAS-Q)}$	$t_{h(CAS-OUT)}$	Data-out hold time after column address strobe
$t_{h(CAS-RAS)}$		Row address strobe hold time after column address strobe
$t_{h(CAS-W)}$	$t_{h(CAS-WR)}$	Write hold time after column address strobe
$t_{h(D)}$	$t_{h(DA)}$	Data-in hold time
$t_{h(D-PR)}$	$t_{h(DA-PRO)}$	Program hold time after data-in
$t_{h(E)}$	$t_{h(CE)}$	Chip enable hold time
$t_{h(E-D)}$	$t_{h(CE-DA)}$	Data-in hold time after chip enable
$t_{h(E-G)}$	$t_{h(CE-OE)}$	Output enable hold time after chip enable
$t_{h(R)}$	$t_{h(RD)}$	Read hold time
$t_{h(RAS-CA)}$		Column address hold time after row address strobe
$t_{h(RAS-CAS)}$		Column address strobe hold time after row address strobe
$t_{h(RAS-D)}$	$t_{h(RAS-DA)}$	Data-in hold time after row address strobe
$t_{h(RAS-W)}$	$t_{h(RAS-WR)}$	Write hold time after row address strobe
$t_{h(S)}$	$t_{h(CS)}$	Chip select hold time
$t_{h(W)}$	$t_{h(WR)}$	Write hold time
$t_{h(W-CAS)}$	$t_{h(WR-CAS)}$	Column address strobe hold time after write
$t_{h(W-D)}$	$t_{h(WR-DA)}$	Data-in hold time after write
$t_{h(W-RAS)}$	$t_{h(WR-RAS)}$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_{PLH}		Low-level to high-level propagation time
t_{r}		Rise time
$t_{rec(W)}$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec(PD)}$	$t_{R(PD)}$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a speciifed input terminal and a consecutive active tarnsition at another specified input terminal
$t_{su(A)}$	$t_{su(AD)}$	Address setup time
$t_{su(A-E)}$	$t_{su(AD-CE)}$	Chip enable setup time before address
$t_{su(A-W)}$	$t_{su(AD-WR)}$	Write setup time before address
$t_{su(CA-RAS)}$		Row address strobe setup time before column address

New symbol	Former symbol	Parameter—definition
$t_{su(D)}$	$t_{su(DA)}$	Data-in setup time
$t_{su(D-E)}$	$t_{su(DA-CE)}$	Chip enable setup time before data-in
$t_{su(D-W)}$	$t_{su(DA-WR)}$	Write setup time before data-in
$t_{su(E)}$	$t_{su(CE)}$	Chip enable setup time
$t_{su(E-P)}$	$t_{su(CE-P)}$	Precharge setup time before chip enable
$t_{su(G-E)}$	$t_{su(OE-CE)}$	Chip enable setup time before output enable
$t_{su(P-E)}$	$t_{su(P-CE)}$	Chip enable setup time before precharge
$t_{su(PD)}$		Power-down setup time
$t_{su(R)}$	$t_{su(RD)}$	Read setup time
$t_{su(R-CAS)}$	$t_{su(RA-CAS)}$	Column address strobe setup time before read
$t_{su(RA-CAS)}$		Column address strobe setup time before row address
$t_{su(S)}$	$t_{su(CS)}$	Chip select setup time
$t_{su(S-W)}$	$t_{su(CS-WR)}$	Write setup time before chip select
$t_{su(W)}$	$t_{su(WR)}$	Write setup time
t_{THL}		High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_{TLH}		Low-level- to high-level transition time
$t_{v(A)}$	$t_{dv(AD)}$	Data valid time after address
$t_{v(E)}$	$t_{dv(CE)}$	Data valid time after chip enable
$t_{v(E)PR}$	$t_{v(CE)PR}$	Data valid time after chip enable in program mode
$t_{v(G)}$	$t_{v(OE)}$	Data valid time after output enable
$t_{v(PR)}$		Data valid time after program
$t_{v(S)}$	$t_{v(CS)}$	Data valid time after chip select
t_{w}		Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms
$t_{w(E)}$	$t_{w(CE)}$	Chip enable pulse width
$t_{w(EH)}$	$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(EL)}$	$t_{w(EL)}$	Chip enable low pulse width
$t_{w(PR)}$		Program pulse width
$t_{w(R)}$	$t_{w(RD)}$	Read pulse width
$t_{w(S)}$	$t_{w(CS)}$	Chip select pulse width
$t_{w(W)}$	$t_{w(WR)}$	Wrtie pulse width
$t_{w(\phi)}$		Clock pulse width
Ta		Ambient temperature
Topr		Operating temperature
Tstg		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_{I}		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_{O}		Output voltage
V_{OH}		High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low-state voltage range at the output
V_{SS}		V_{SS} supply voltage

Note: These abbreviations, with some exceptions, are excerpted from IEC publication 148.

PRECAUTIONS IN HANDLING MOS ICs/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1M Ω resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

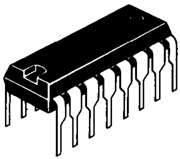
4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

MOS DYNAMIC RAM

2

M5K4164AP-12, -15



65536-BIT (65536-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. The M5K4164AP operates on a 5V power supply using the on-chip substrate bias generator.

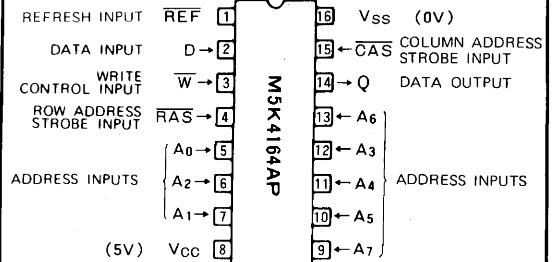
FEATURES

- High speed

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K4164AP-12	120	220	175
M5K4164AP-15	150	260	150

- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation: 300mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, RAS-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible

PIN CONFIGURATION (TOP VIEW)



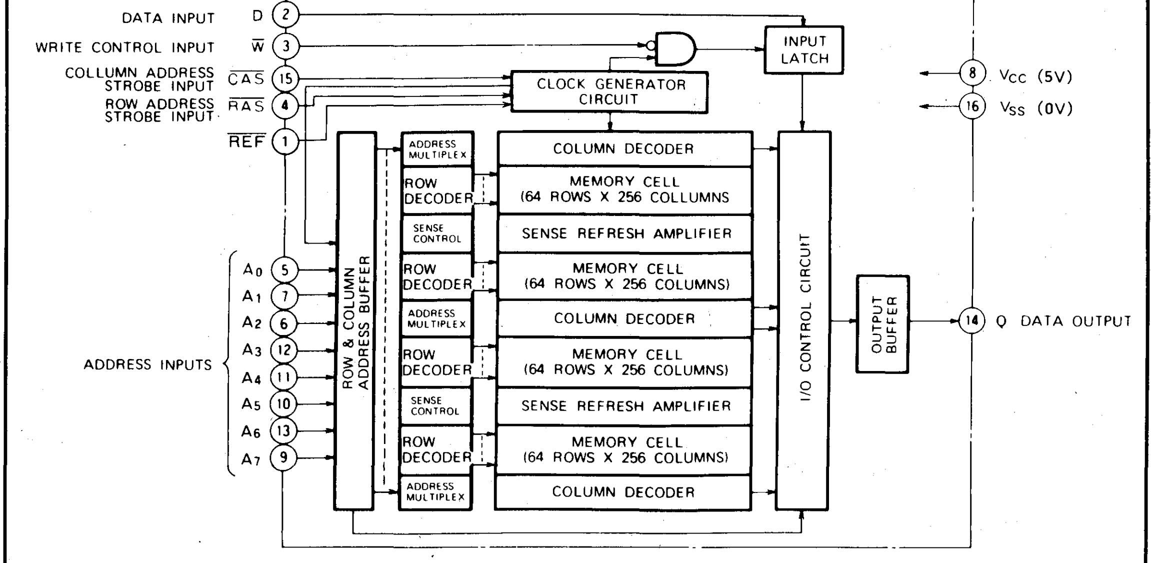
Outline 16P4

- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms (16K dynamic RAMs M5K4116P, S compatible)
- CAS controlled output allows hidden refresh
- Output data can be held infinitely by CAS
- Pin 1 controls automatic- and Self-refresh mode.
- Interchangeable with Fujitsu MB8265A and Motorola's MCM6664 in pin configuration

APPLICATION

Main memory unit for computers

BLOCK DIAGRAM



FUNCTION

The M5K4164AP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs							Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	$\overline{REF}$	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	NAC	VLD	YES	Page mode identical except refresh is NO
Write	ACT	ACT	ACT	VLD	APD	APD	NAC	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	NAC	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	NAC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	APD	DNC	NAC	VLD	YES	
Automatic refresh	NAC	DNC	DNC	DNC	DNC	DNC	ACT	OPN	YES	
Self refresh	NAC	DNC	DNC	DNC	DNC	DNC	ACT	OPN	YES	
Hidden automatic refresh	NAC	ACT	DNC	DNC	DNC	DNC	ACT	VLD	YES	
Hidden self refresh	NAC	ACT	DNC	DNC	DNC	DNC	ACT	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	NAC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 65536 memorv cells in the M5K4164AP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\ max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5K4164AP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164AP, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection
Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary
By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164AP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164AP are as follows.

1. Normal Refresh
Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh
A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Automatic Refresh
Pin 1 ($\overline{REF}$) has two special functions. The M5K4164AP has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is applied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

4. Self-Refresh
The other function of pin 1 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the M5K4164AP will refresh itself. This internal sequence repeats asynchronously every 12 to 16 μs. After 2 ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 1 ($\overline{REF}$) refresh function gives the user a feature that is free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx 3M\Omega$) on pin 1, so if the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect) without affecting the normal operations.

5. Hidden Refresh
A features of the M5K4164AP is that refresh cycle may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5K4164AP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164AP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5K4164AP operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 6.5V, All other pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5K4164AP-12	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min output open			50	mA
		M5K4164AP-15				45	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$ = V_{IH} output open			4	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5K4164AP-12	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} $t_{C(\overline{REF})}$ = min, output open			40	mA
		M5K4164AP-15				35	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5K4164AP-12	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{CPG} = min, output open			40	mA
		M5K4164AP-15				35	
$I_{CC5(AV)}$	Average supply current from V_{CC}, automatic refreshing (Note 3)	M5K4164AP-12	$\overline{RAS}$ = V_{IH}, $\overline{REF}$ cycling $t_{C(REF)}$ = min, output open			40	mA
		M5K4164AP-15				35	
$I_{CC6(AV)}$	Average supply current from V_{CC}, self refreshing		$\overline{RAS}$ = V_{IH}, $\overline{REF}$ = V_{IL} output open			8	mA
$C_{I(A)}$	Input capacitance, address inputs		V_I = V_{SS}, f = 1MHz, V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
$C_{I(REF)}$	Input capacitance, $\overline{REF}$ input					10	pF
C_O	Output capacitance		V_O = V_{SS}, f = 1MHz, V_I = 25mVrms			7	pF

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

65536-BIT (65536-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		2		2	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60	∞	75	∞	ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	−20		−20		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	25	60	30	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	0		0		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	90		95		ns
t_{THL}	Transition time	t_T	3	35	3	35	ns
t_{TLH}			3	35	5	35	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$)
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL}(t_{TLH}) + t_{su(CA-CAS)}min$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	220		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	10		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		120		150	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}
Note 13: This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}max$. Test conditions; Load= T TL, C_L= 100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}max$. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}max$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load=2T TL, C_L= 100pF

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	220		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−5		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	90		95		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	40		45		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	90		95		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	245		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	265		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	100		120		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		120		150	ns

Note 15. t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data outputs keep the high-impedance state.
When $t_{d(RAS-W)} \geq t_{d(RAS-W)}$ min. and $t_{d(CAS-W)} \geq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
$t_{C PGR}$	Page-mode read cycle time	t_{PC}	140		145		ns
$t_{C PGW}$	Page-Mode write cycle time	t_{PC}	140		145		ns
$t_{C PGRW}$	Page-Mode read-write cycle time	—	150		180		ns
$t_{C PGRMW}$	Page-Mode read-modify-write cycle time	—	170		195		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	55		60		ns

Automatic Refresh Cycle

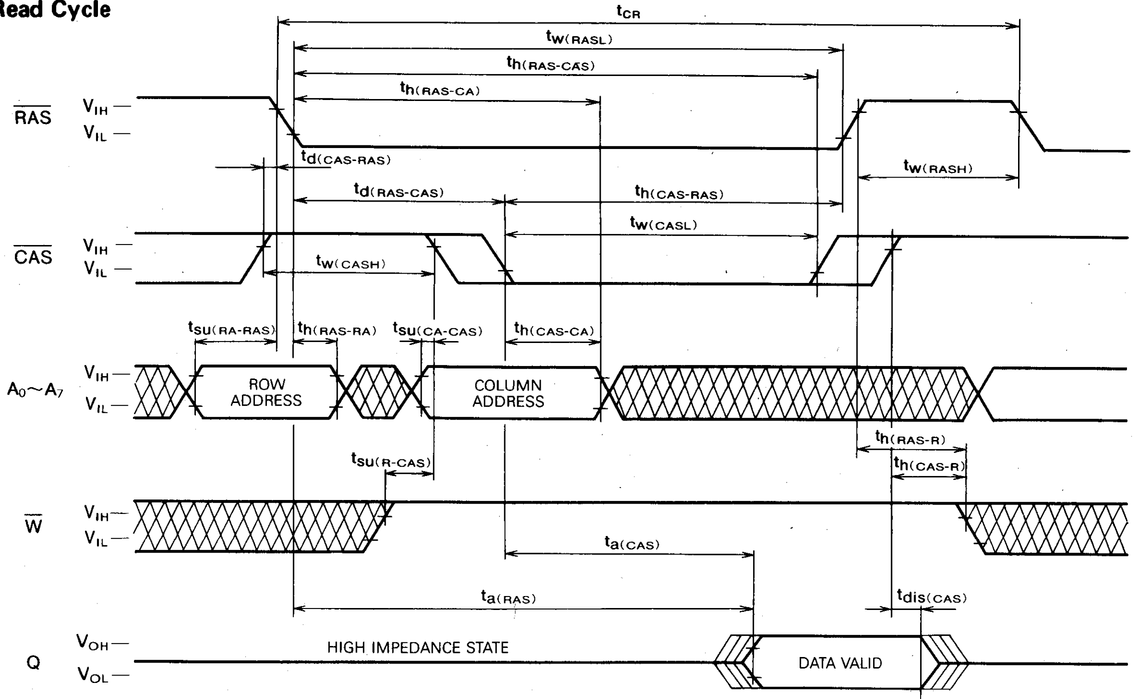
Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
$t_{c(REF)}$	Automatic Refresh cycle time	t_{FC}	220		260		ns
$t_{d(RAS-REF)}$	Delay time, $\overline{RAS}$ to $\overline{REF}$	t_{RFD}	90		100		ns
$t_{w(REFL)}$	$\overline{REF}$ low pulse width	t_{FP}	60	8000	60	8000	ns
$t_{w(REFH)}$	$\overline{REF}$ high pulse width	t_{FI}	30		30		ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FSR}	30		30		ns
$t_{su(REF-RAS)}$	$\overline{REF}$ pulse setup time before $\overline{RAS}$	t_{FRD}	250		295		ns

Self-Refresh Cycle

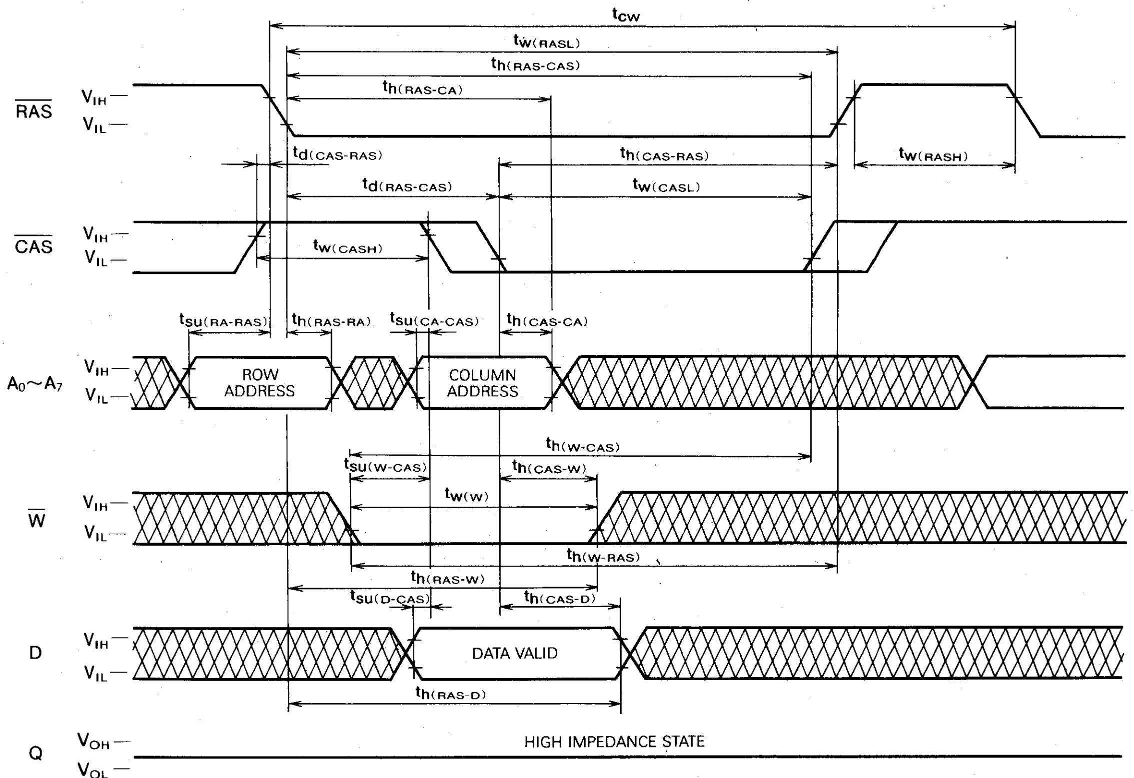
Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
$t_{d(RAS-REF)}$	Delay time, RAS to $\overline{REF}$	t_{RFD}	90		100		ns
$t_{w(REFL)}$	$\overline{REF}$ low pulse width	t_{FBP}	8000	∞	8000	∞	ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FBR}	310		345		ns

TIMING DIAGRAMS (Note 18)

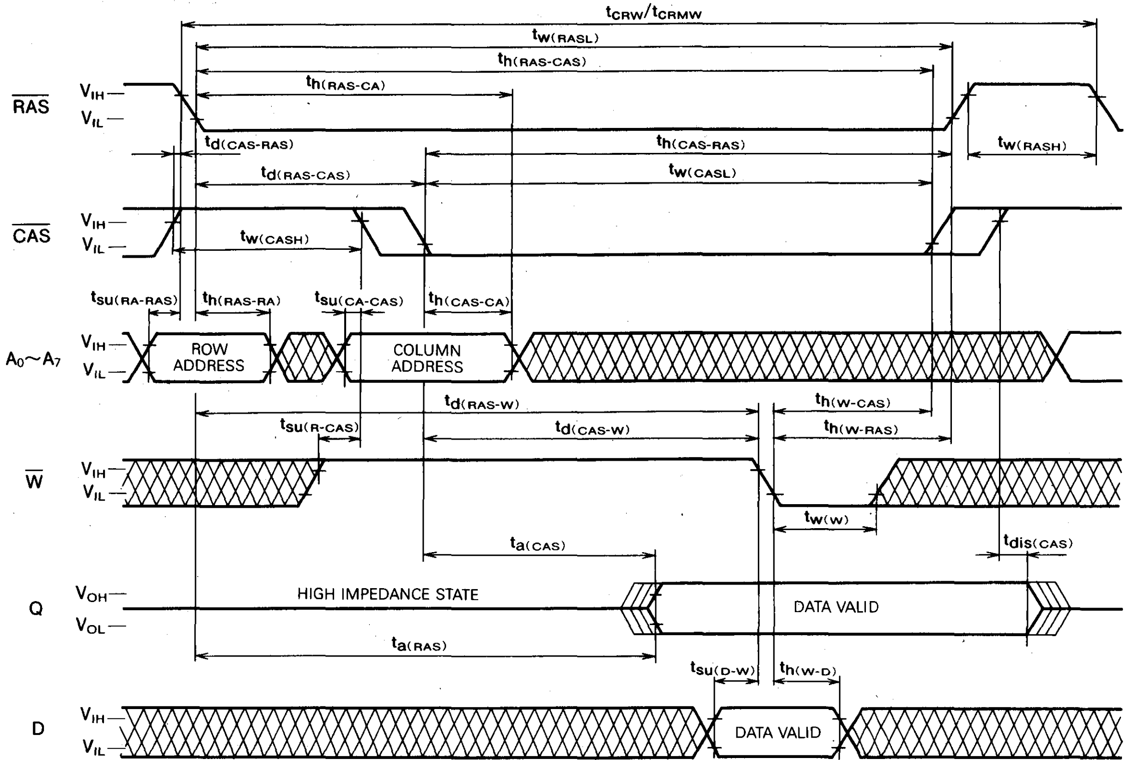
Read Cycle



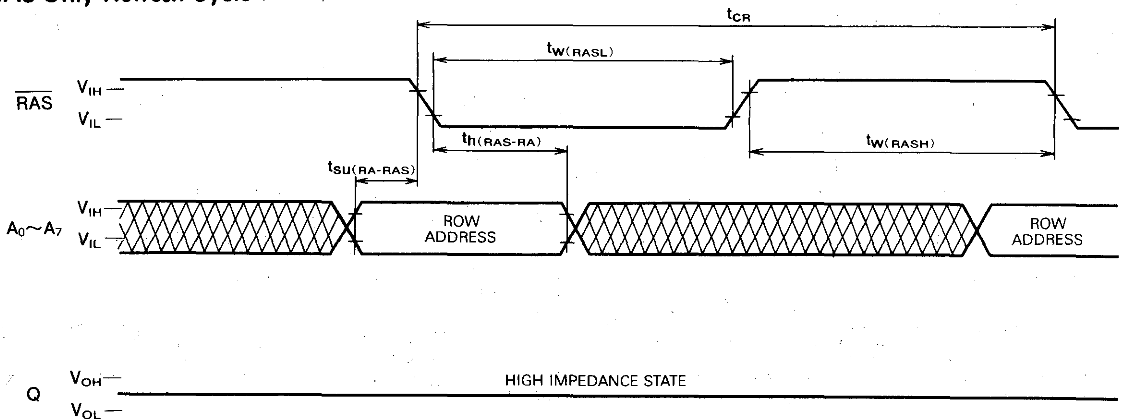
Write Cycle (Early Write)

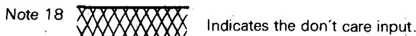


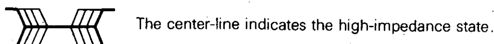
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 19)

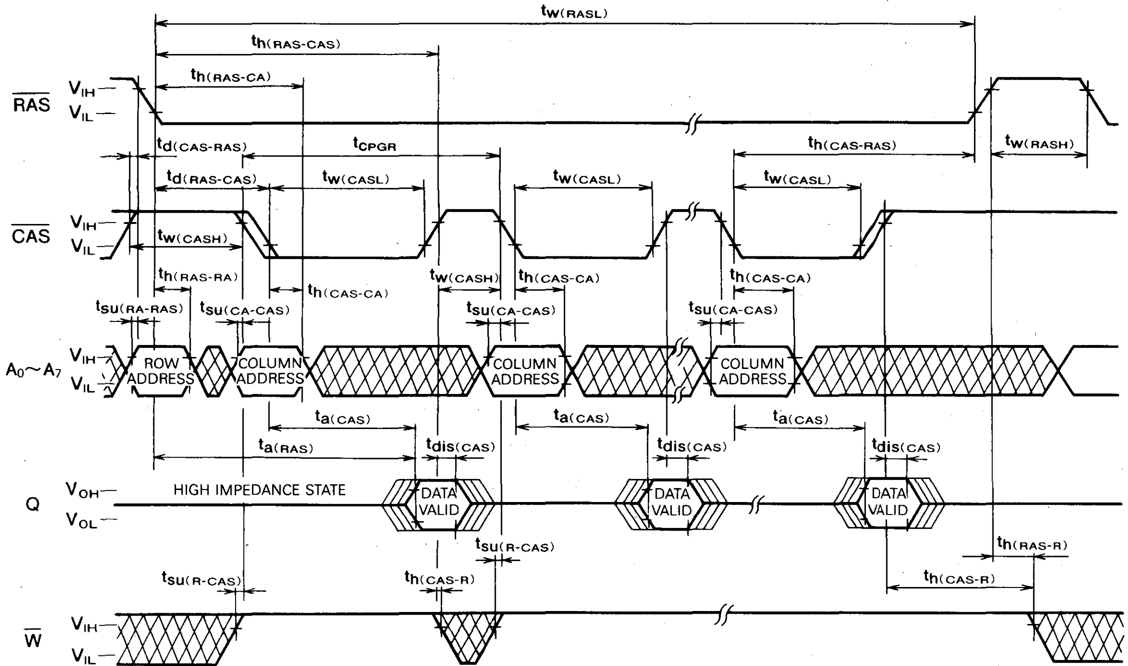


Note 18  Indicates the don't care input.

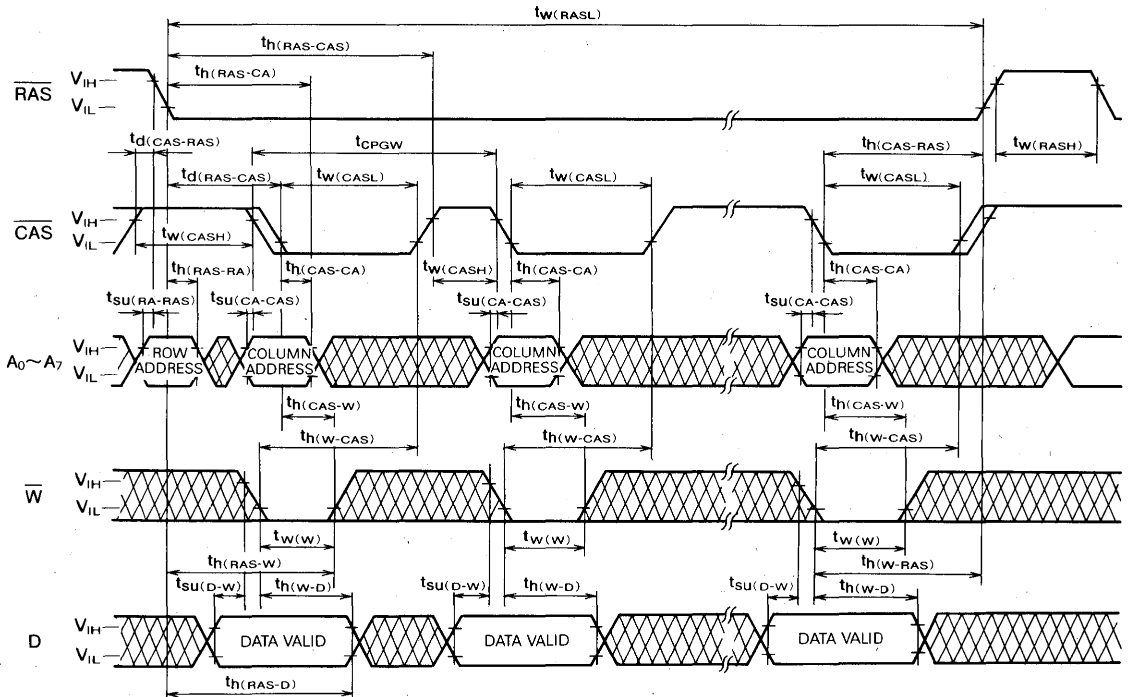
 The center-line indicates the high-impedance state.

Note 19. $\overline{CAS}$ = V_{IH}, $\overline{W}$, A_7, D = don't care.

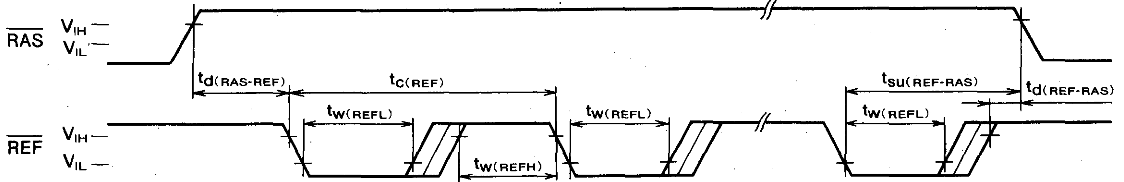
Page-Mode Read Cycle



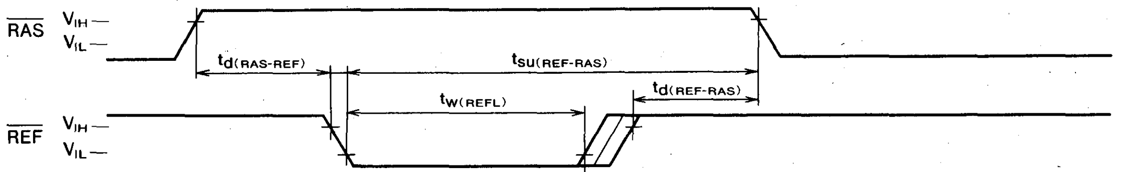
Page-Mode Write Cycle



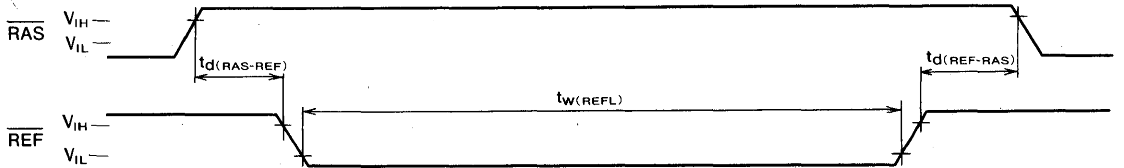
Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 20)



Automatic Pulse Refresh Cycle (Single Pulse) (Note 20)

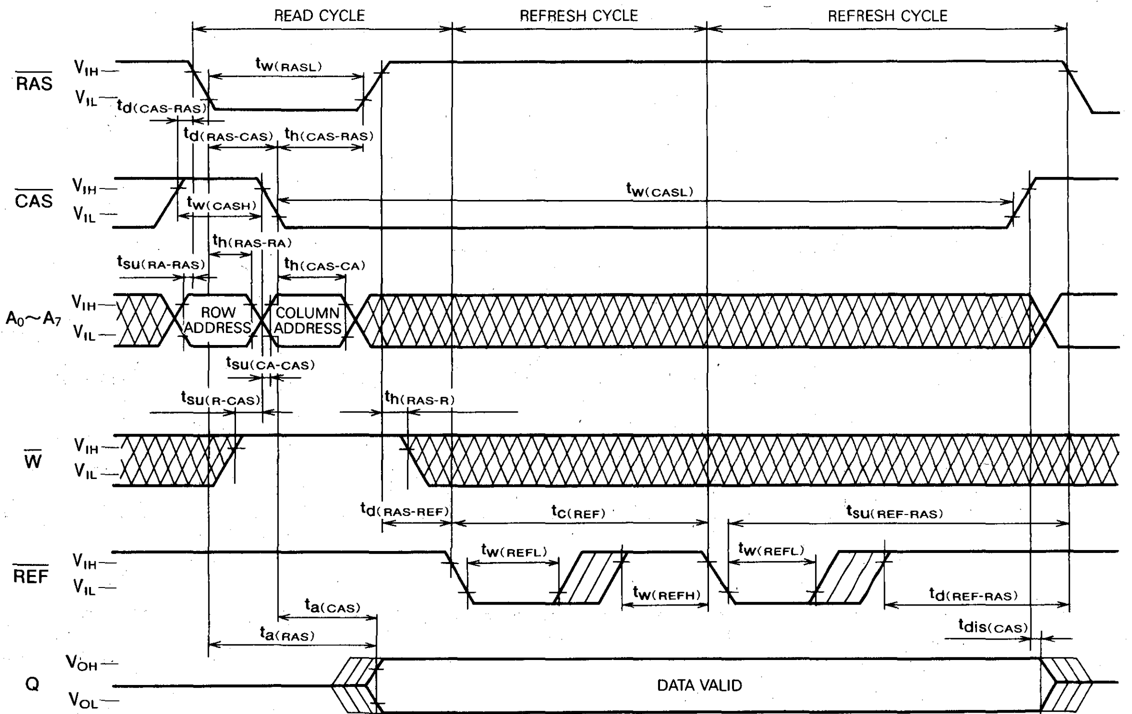


Self-Refresh Cycle (Note 20)

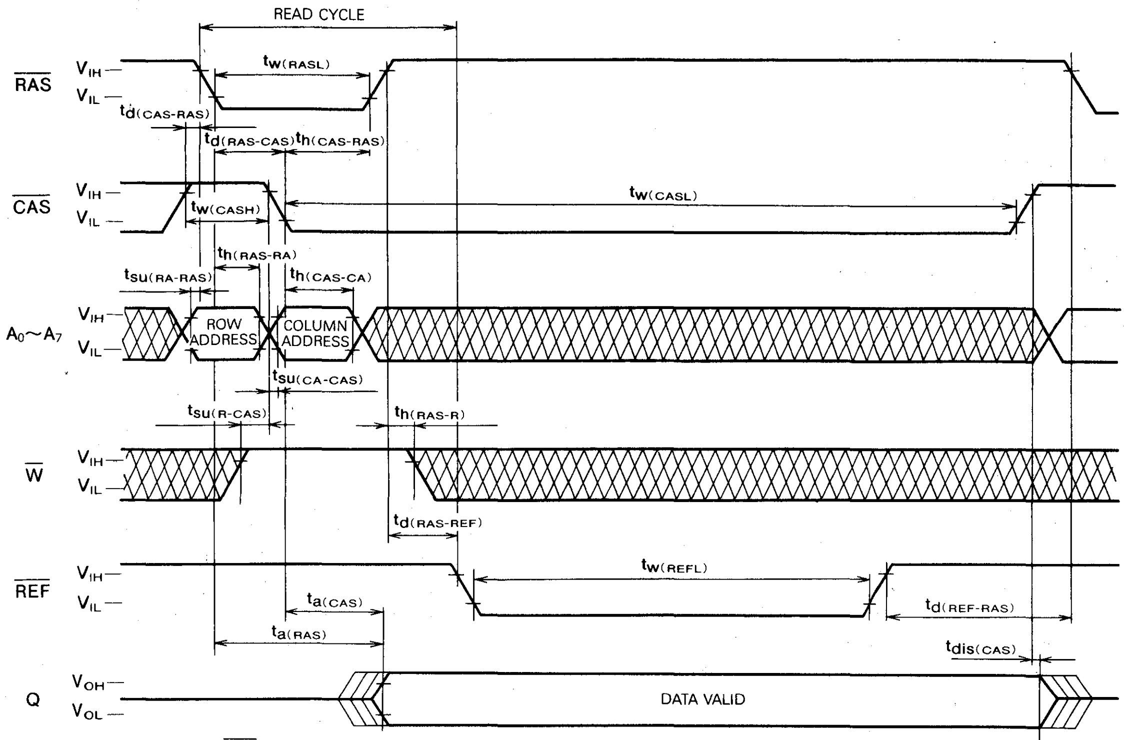


Note 20 : $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

Hidden Automatic Pulse Refresh Cycle

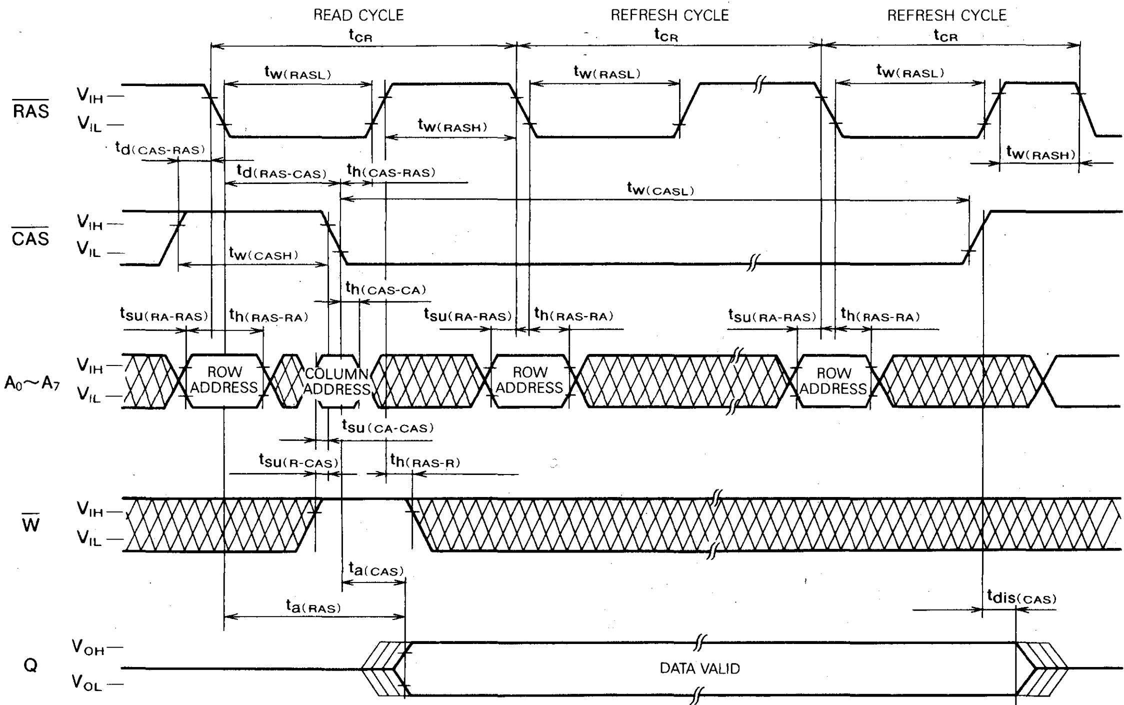


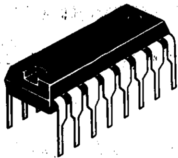
Hidden Self-Refresh Cycle (Note 21)



Note 21 : If the pin 1 (REF) function is not used, pin 1 may be left open (not connect).

Hidden Refresh Cycle (Note 19)





M5K4164ANP-12, -15

65536-BIT (65536-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell privide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. The M5K4164ANP operates on a 5V power supply using the on-chip substrate bias generator.

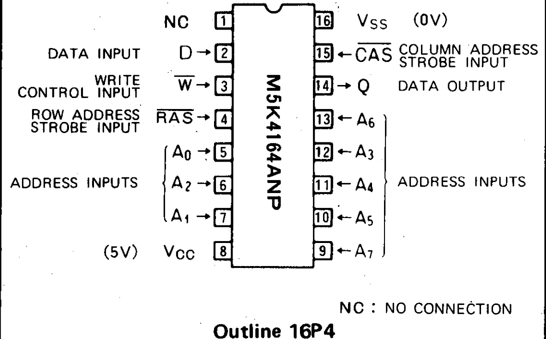
FEATURES

- High speed

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K4164ANP-12	120	220	175
M5K4164ANP-15	150	260	150

- Single 5V±10% supply
- Low standby power dissipation: 22mW (max)
- Low operating power dissipation: 300mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible

PIN CONFIGURATION (TOP VIEW)



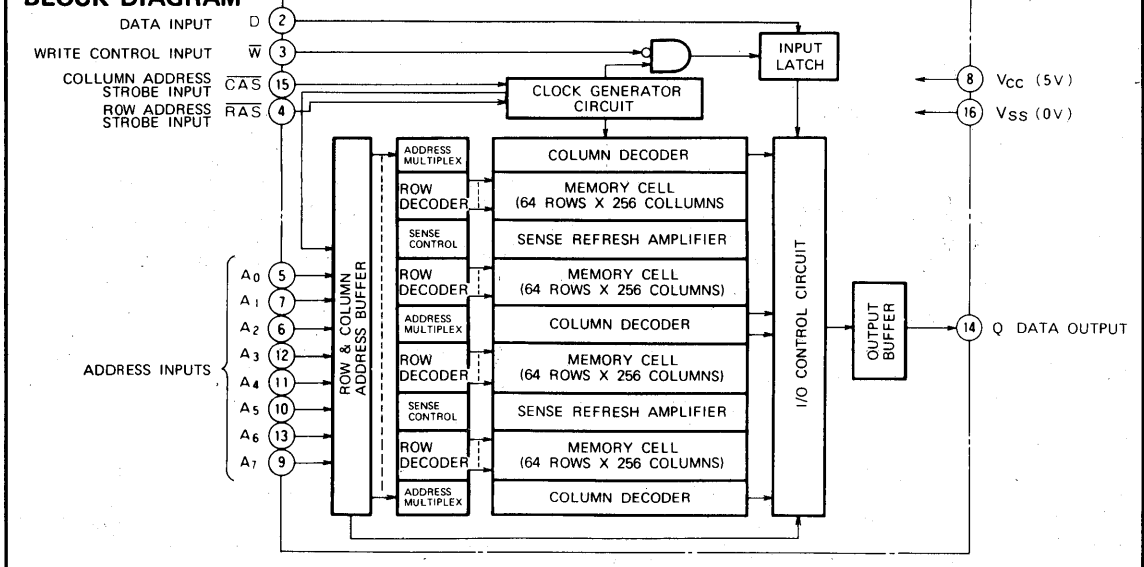
Outline 16P4

- Output is three-state and directly TTL-compatible
- 128 refresh cycles every 2ms (16K dynamic RAMs M5K4116P, S compatible)
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$
- Interchangeable with Mostek's MK4564 and Motorola's MCM6665 in pin configuration

APPLICATION

Main memory unit for computers

BLOCK DIAGRAM



FUNCTION

The M5K4164ANP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Page mode identical except refresh is NO
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	APD	DNC	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 65536 memory cells in the M5K4164ANP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5K4164ANP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164ANP, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164ANP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K4164ANP are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Hidden Refresh

A feature of the M5K4164ANP is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5K4164ANP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164ANP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5K4164ANP operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C, unless otherwise noted) (Note. 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note. 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 6.5V, All other pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5K4164ANP-12	$\overline{RAS}$, $\overline{CAS}$ cycling			50	mA
		M5K4164ANP-15	$t_{CR} = t_{CW}$ = min output open			45	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = V_{IH}$ output open			4	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5K4164ANP-12	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$			40	mA
		M5K4164ANP-15	$t_{C(\overline{REF})}$ = min, output open			35	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5K4164ANP-12	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling			40	mA
		M5K4164ANP-15	t_{CPG} = min, output open			35	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_I = 25mVrms			7	pF

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164ANP-12		M5K4164ANP-15		
			Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		2		2	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60	∞	75	∞	ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	−20		−20		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	25	60	30	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	0		0		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	90		95		ns
t_{THL}	Transition time	t_T	3	35	3	35	ns
t_{TLH}			3	35	3	35	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$)
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\min = t_{h(RAS-RA)}\min + 2t_{THL}(t_{TLH}) + t_{su(CA-CAS)}\min$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164ANP-12		M5K4164ANP-15		
			Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	220		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	10		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the vauel when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164ANP-12		M5K4164ANP-15		
			Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	220		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−5		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	90		95		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	40		45		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	90		95		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164ANP-12		M5K4164ANP-15		
			Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	245		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	265		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	100		120		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		120		100	ns

Note 15. t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

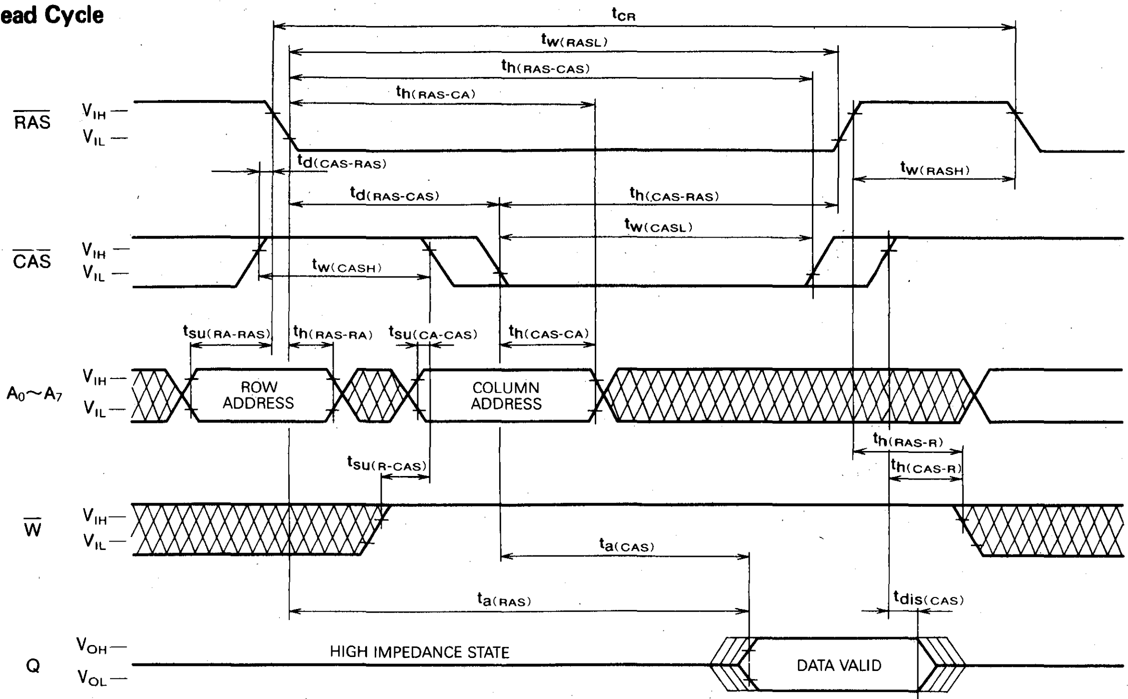
17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data outputs keep the high-impedance state.
When $t_{d(RAS-W)} \geq t_{d(RAS-W)}$ min, and $t_{d(CAS-W)} \geq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

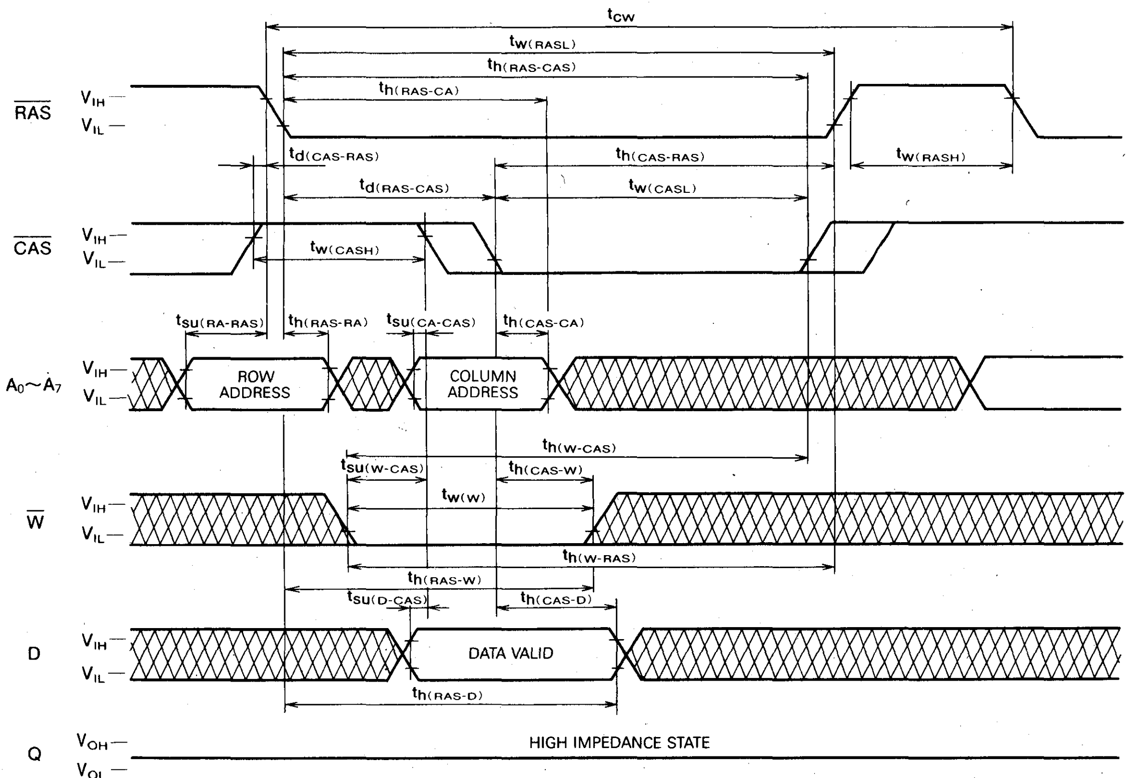
Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5K4164ANP-12		M5K4164ANP-15		
			Min	Max	Min	Max	
$t_{C PGR}$	Page-mode read cycle time	t_{PC}	140		145		ns
$t_{C PGW}$	Page-Mode write cycle time	t_{PC}	140		145		ns
$t_{C PGRW}$	Page-Mode read-write cycle time	—	150		180		ns
$t_{C PGRMW}$	Page-Mode read-modify-write cycle time	—	170		195		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	55		60		ns

TIMING DIAGRAMS (Note 18)

Read Cycle

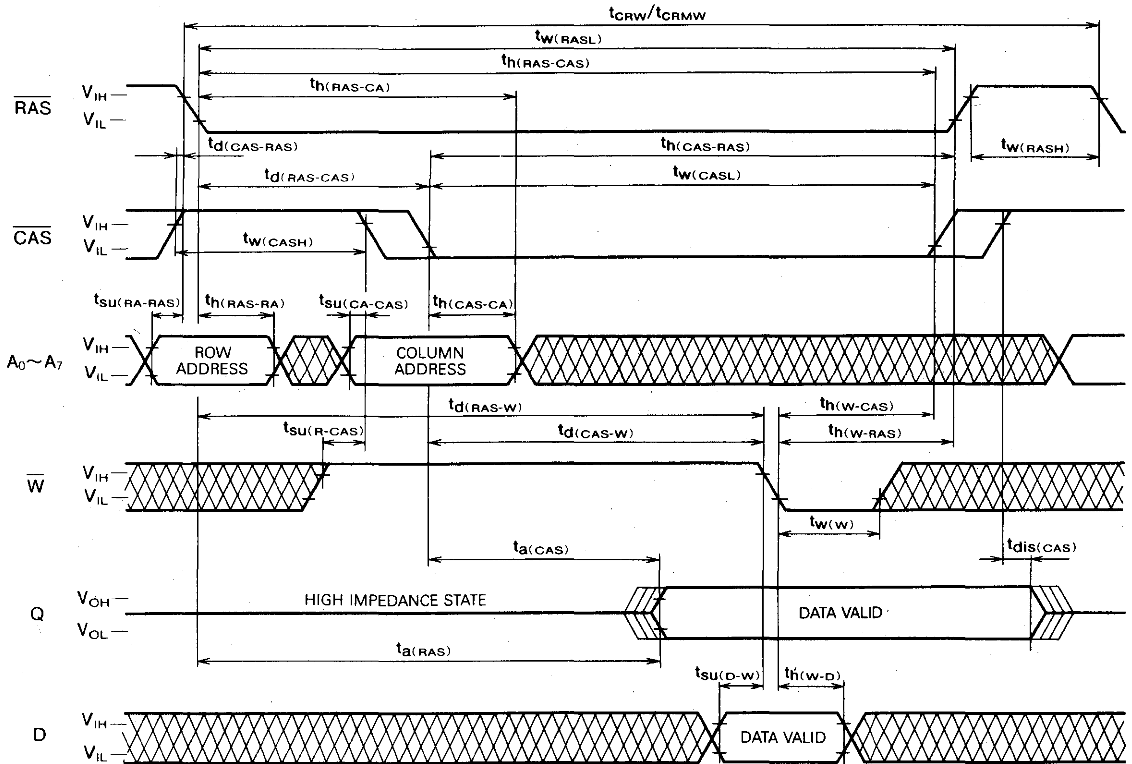


Write Cycle (Early Write)

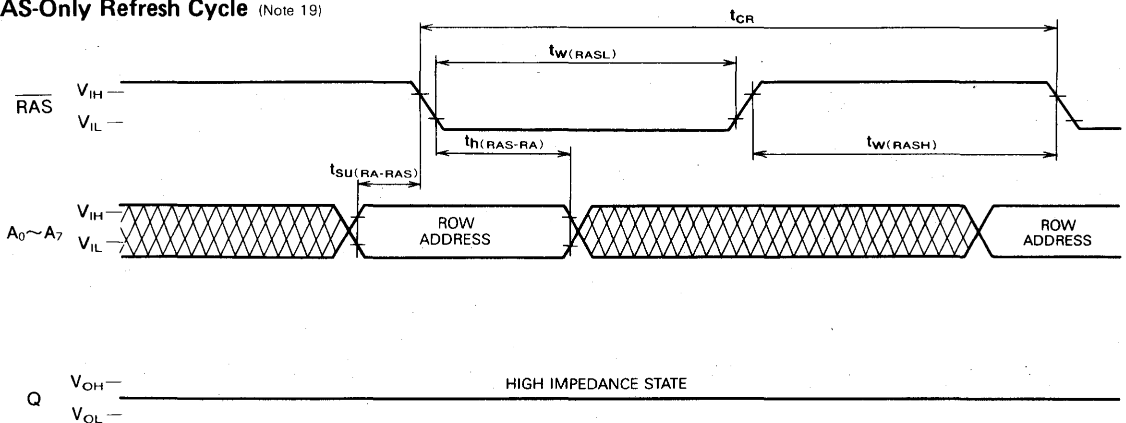


MITSUBISHI ELECTRIC

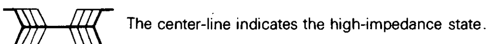
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 19)

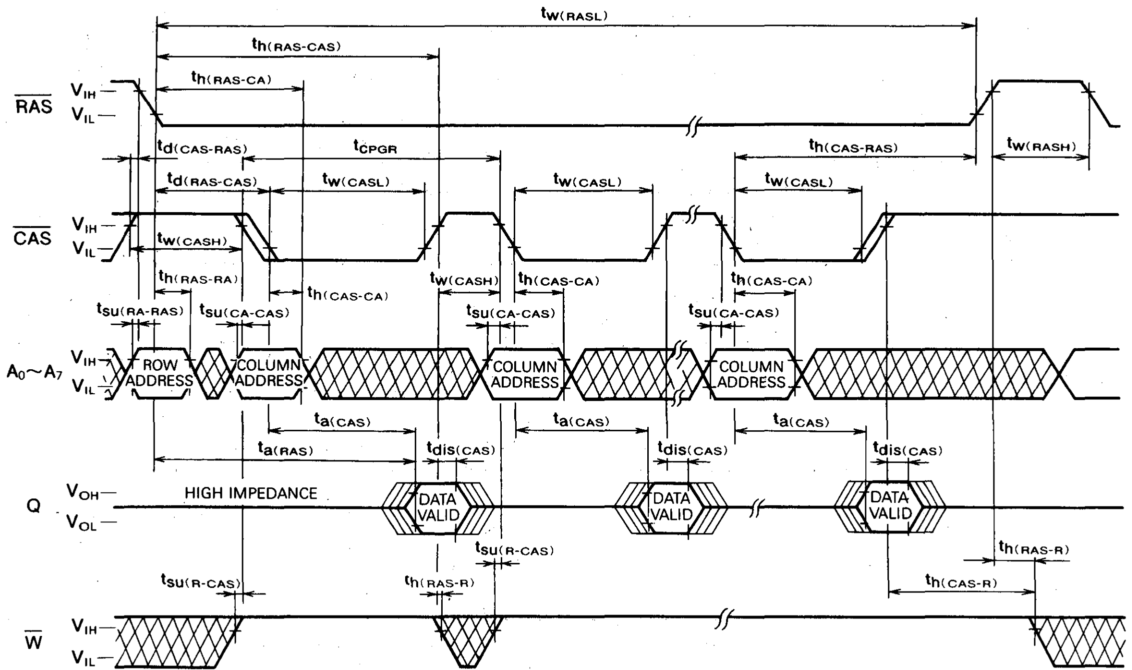


Note 18 Indicates the don't care input.

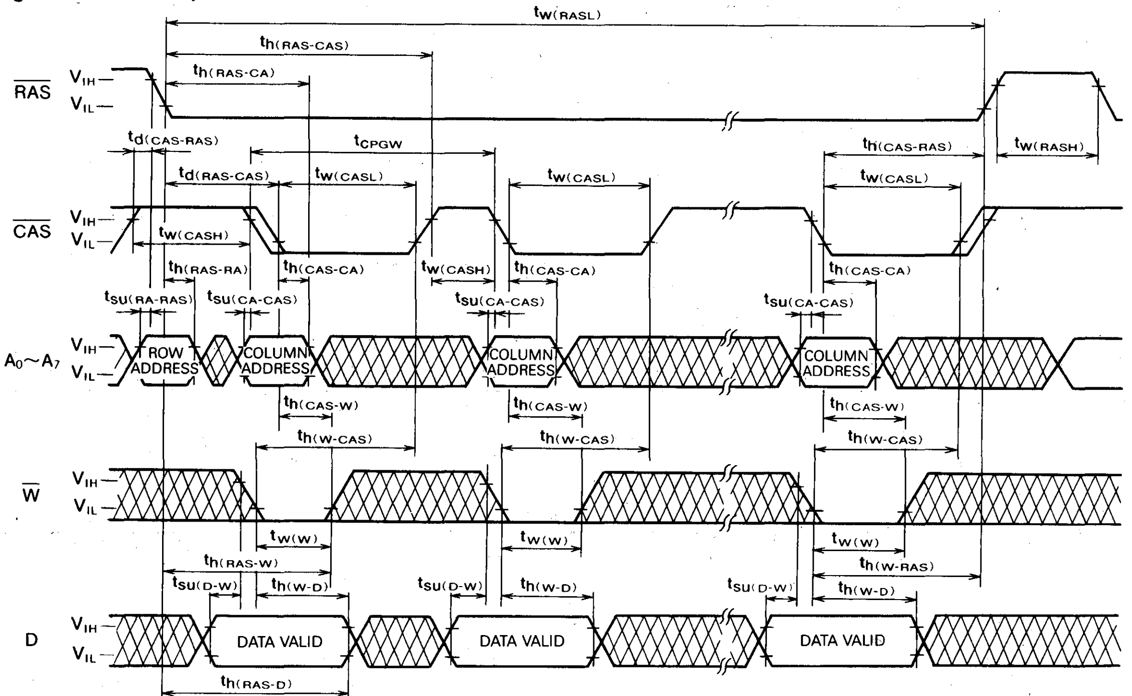
 The center-line indicates the high-impedance state.

Note 19. $\overline{CAS}$ = VIH, $\overline{W}$, A7, D = don't care.

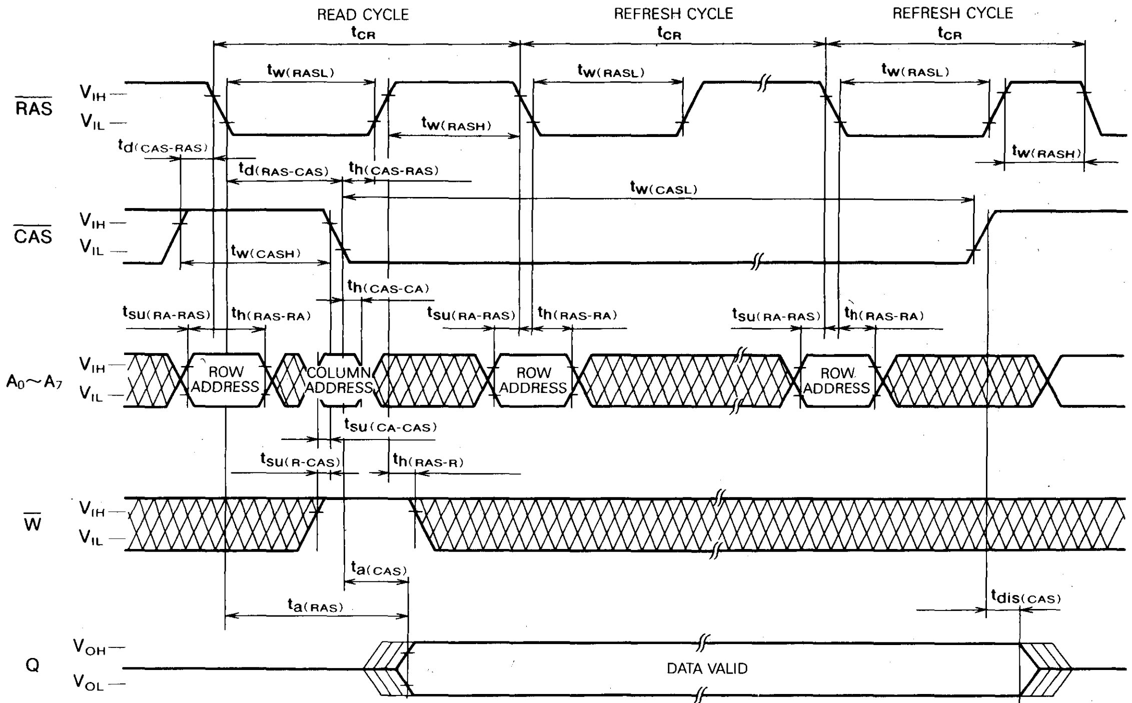
Page-Mode Read Cycle

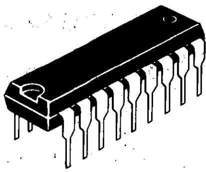


Page-Mode Write Cycle



Hidden Refresh Cycle





MITSUBISHI LSIs

M5M4416P-12, -15

65536-BIT (16384-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is family of 16348-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package configuration and an increase in system densities. The M5M4416P operates on a 5V power supply using the on-chip substrate bias generator.

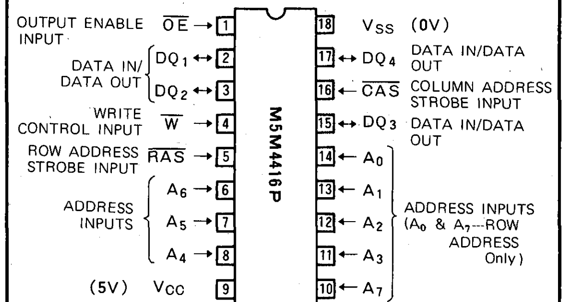
FEATURES

- Performance ranges

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4416P-12	120	220	175
M5M4416P-15	150	260	150

- 16,384 x 4 Organization
- Industry standard 18-pin dual in line package
- Single 5V ±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4416P-12 275mW (max)
  - M5M4416P-15 250mW (max)

PIN CONFIGURATION (TOP VIEW)



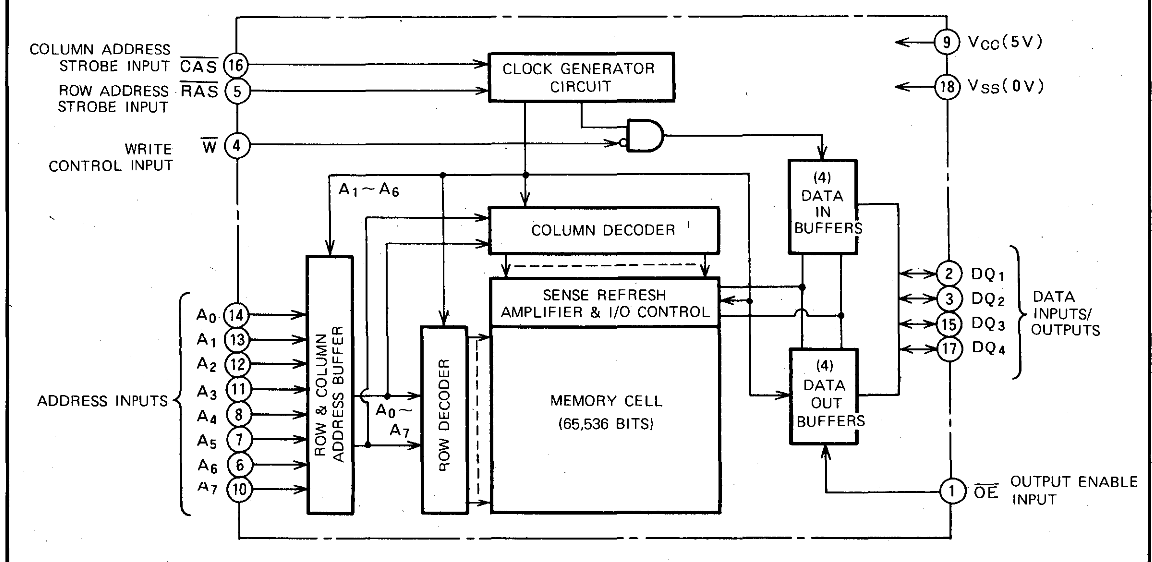
Outline 18 P4

- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 128 refresh cycles/2ms. Pin 10 is not needed for refresh
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30μs max

APPLICATION

Refresh memory for CRT

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION

The M5M4416P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column adress	Input DQ	Output DQ		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Page mode identical
Write (Early Write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only retfesh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

SUMMARY OF OPERATIONS

address (AO through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins AO through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OEHD}.

output enable ($\overline{OE}$)

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5M4416P must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5M4416P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Hidden Refresh

A features of the M5M4416P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4416P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4416P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4416P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	Condtions	Ratings	Unit
V_{CC}	Supply volrage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, All other pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{cc}, operating (Note 3,4)	M5M4416P-12	$\overline{RAS}$, $\overline{CAS}$ cycling			55	mA
		M5M4416P-15	tc(rd)=tc(w) = min output open			50	
I_{CC2}	Supply current from V_{cc}, standby		$\overline{RAS}$=V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{cc}, retreshing (Note 3)	M5M4416P-12	$\overline{RAS}$ cycling $\overline{CAS}$=V_{IH}			45	mA
		M5M4416P-15	tc(Prd) = min, output open			40	
$I_{CC4(AV)}$	Average supply current from V_{cc}, page mode (Note 3,4)	M5M4416P-12	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			45	mA
		M5M4416P-15	tc(Prd) = min, output open			40	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the tastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz Vi=25mVrms			5	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				10	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits				Unit
				M5M4416P-12		M5M4416P-15		
				Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,7)	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,8)	t_{RAC}		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	—		30		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 9)	t_{OFF}	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 9)	—	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If t_{RLCL} is greater than t_{RLCL} max then $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Alternative Symbol	Limits				Unit
				M5M4416P-12		M5M4416P-15		
				Min	Max	Min	Max	
$t_{C(RF)}$	Refresh cycle time		t_{REF}		2		2	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	−20		−20		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	ns

Note 10: The timing requirements are assumed t_T=5ns.
11: V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; if t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. if t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

Read and Refresh Cycles

Symbol	Parameter		Alternative Symbol	Limits				Unit
				M5M4416P-12		M5M4416P-15		
				Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time		t_{RC}	220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	60		75		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	(Note 15)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	(Note 15)	t_{RRH}	10		10		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		—	30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		—	30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		30		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		—	0		0		ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4416P-12		M5M4416P-15		
			Min	Max	Min	Max	
$t_{C(W)}$	Write cycle time	t_{RC}	220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60		75		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low (Note 17)	t_{WCS}	−5		−5		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	100		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	40		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	100		120		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after Write low	—	25		30		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4416P-12		M5M4416P-15		
			Min	Max	Min	Max	
$t_{C(rdW)}$	Read write/read modify write cycle time (Note 16)	t_{RWC}	295		345		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	195	10000	255	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	135		180		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	195		255		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	135		180		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to Write low (Note 17)	t_{CWD}	90		110		ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to Write low (Note 17)	t_{RWD}	150		185		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	40		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	—	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		30		ns

Note 16: $t_{C(rdW)}$ is specified as $t_{C(rdW)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{w(RH)}$ min + 4 t_T.

17: $t_{SU(WCL)}$, t_{CLWL} and t_{RLWL} are specified as reference points only. If $t_{SU(WCL)} \geqq t_{SU(WCL)}$ min, the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CLWL} \geqq t_{CLWL}$ min and $t_{RLWL} \geqq t_{RLWL}$ min, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Page-Mode Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4416P-12		M5M4416P-15		
			Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read write/read modify write cycle time	—	195		250		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 20)	t_{RAS}	390	30000	505	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	50		60		ns

Note 18: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19: Specified for read or write cycle.
20: Specified for read-write or read-modify-write cycle.

TIMING DIAGRAMS (Note 21)

Read Cycle

$t_{C(rd)}$
$t_{h(RLCH)}$
$t_{w(RL)}$
$t_{h(RLCA)}$

RAS
V_{IH} —
V_{IL} —

t_{CHRL}
$t_{h(CLRH)}$
$t_{w(RH)}$
t_{RLCL}
$t_{w(CL)}$

CAS
V_{IH} —
V_{IL} —

$t_{w(CH)}$
$t_{su(RA)}$
$t_{su(CA)}$
$t_{su(RA)}$
$t_{h(RA)}$
$t_{h(CLCA)}$

$A_0 \sim A_7$
V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS

$t_{su(rd)}$
$t_{h(CHrd)}$
$t_{h(RHrd)}$

W
V_{IH} —
V_{IL} —

$DQ_1 \sim DQ_4$ (INPUTS)
V_{IH} —
V_{IL} —
High-Z

$t_{a(C)}$
$t_{a(R)}$
$t_{dis(CH)}$

$DQ_1 \sim DQ_4$ (OUTPUTS)
V_{OH} —
V_{OL} —
High-Z
DATA VALID

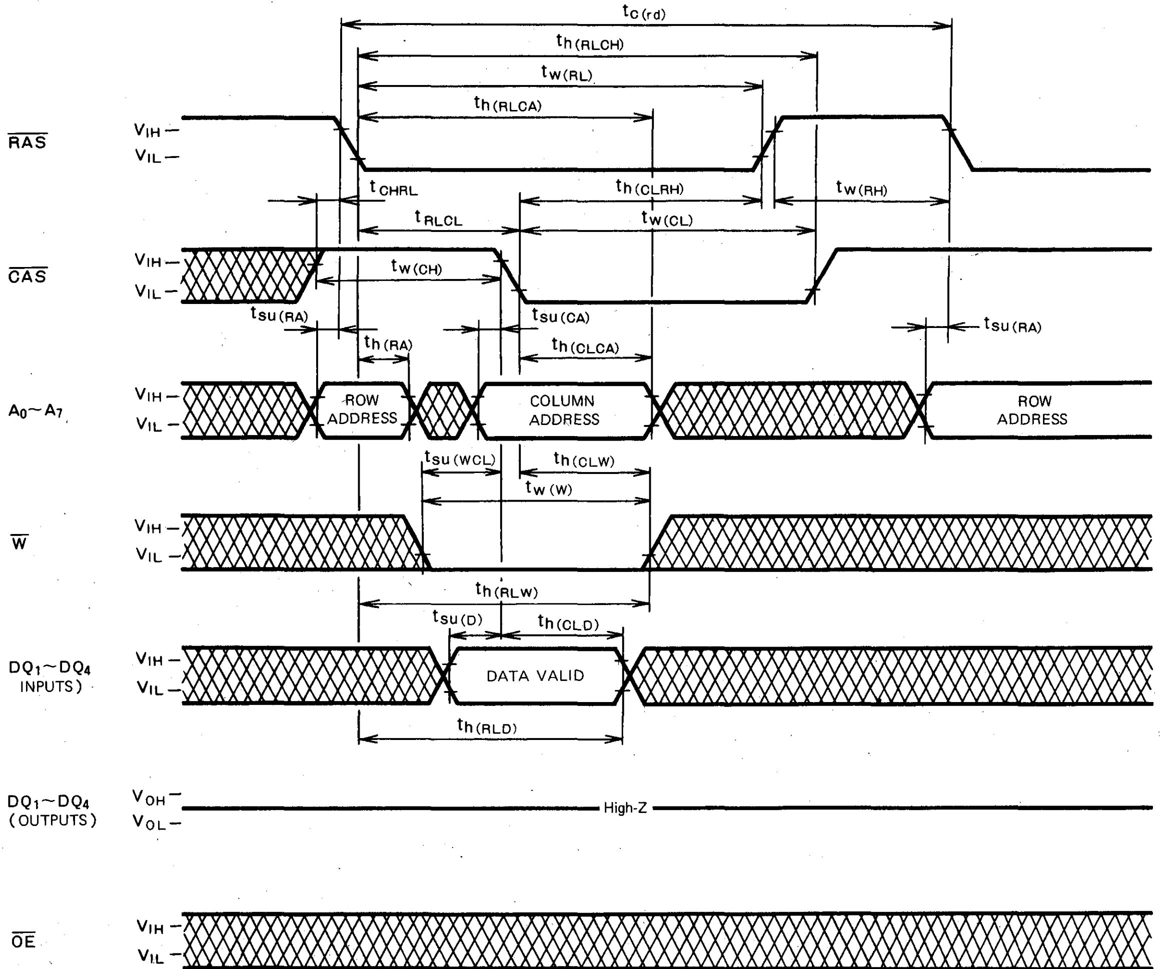
t_{DOEL}
$t_{a(OE)}$
$t_{dis(OE)}$
$t_{h(OERH)}$
t_{OEHD}
$t_{h(OECH)}$

OE
V_{IH} —
V_{IL} —

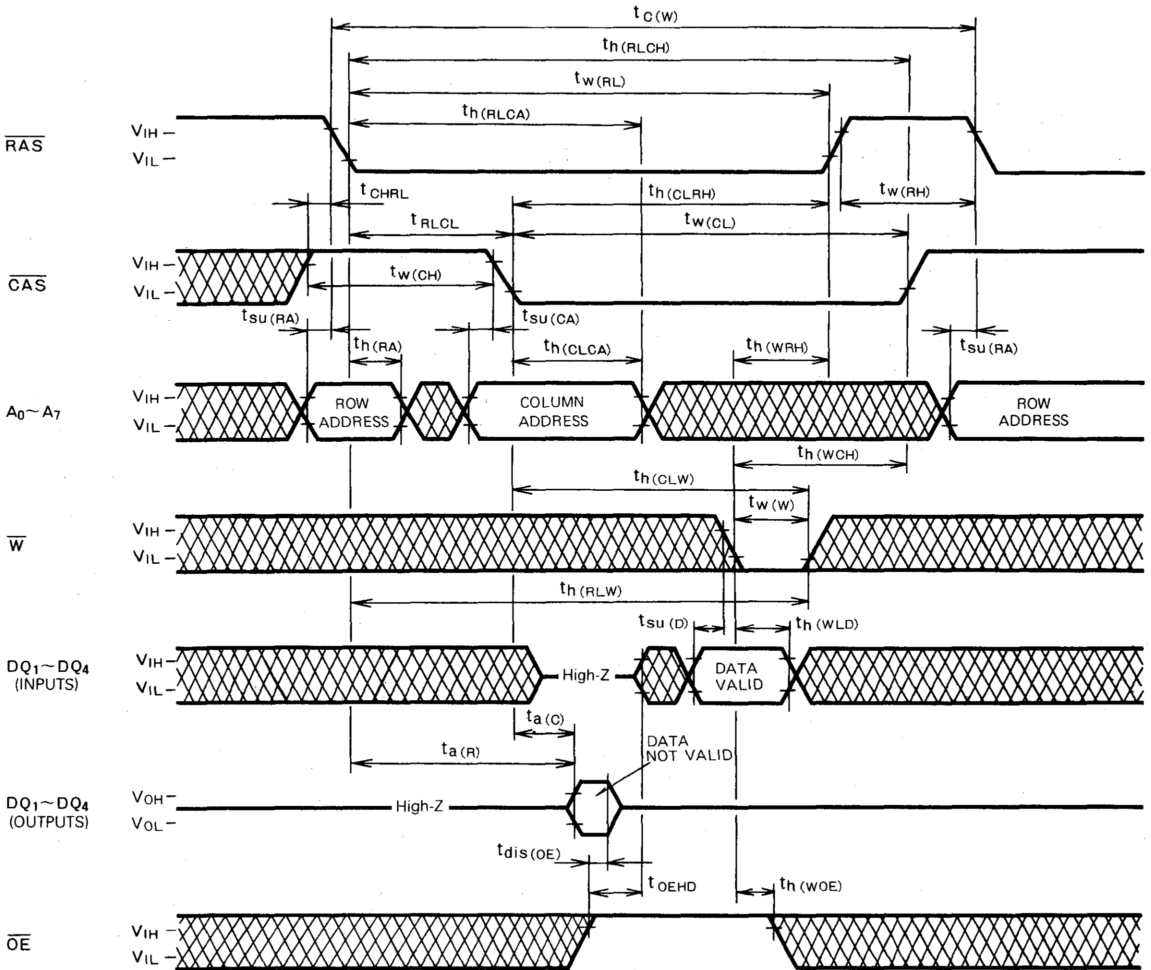
$t_{h(CLOE)}$
$t_{h(RLOE)}$

Note 21. Indicates the don't care input.

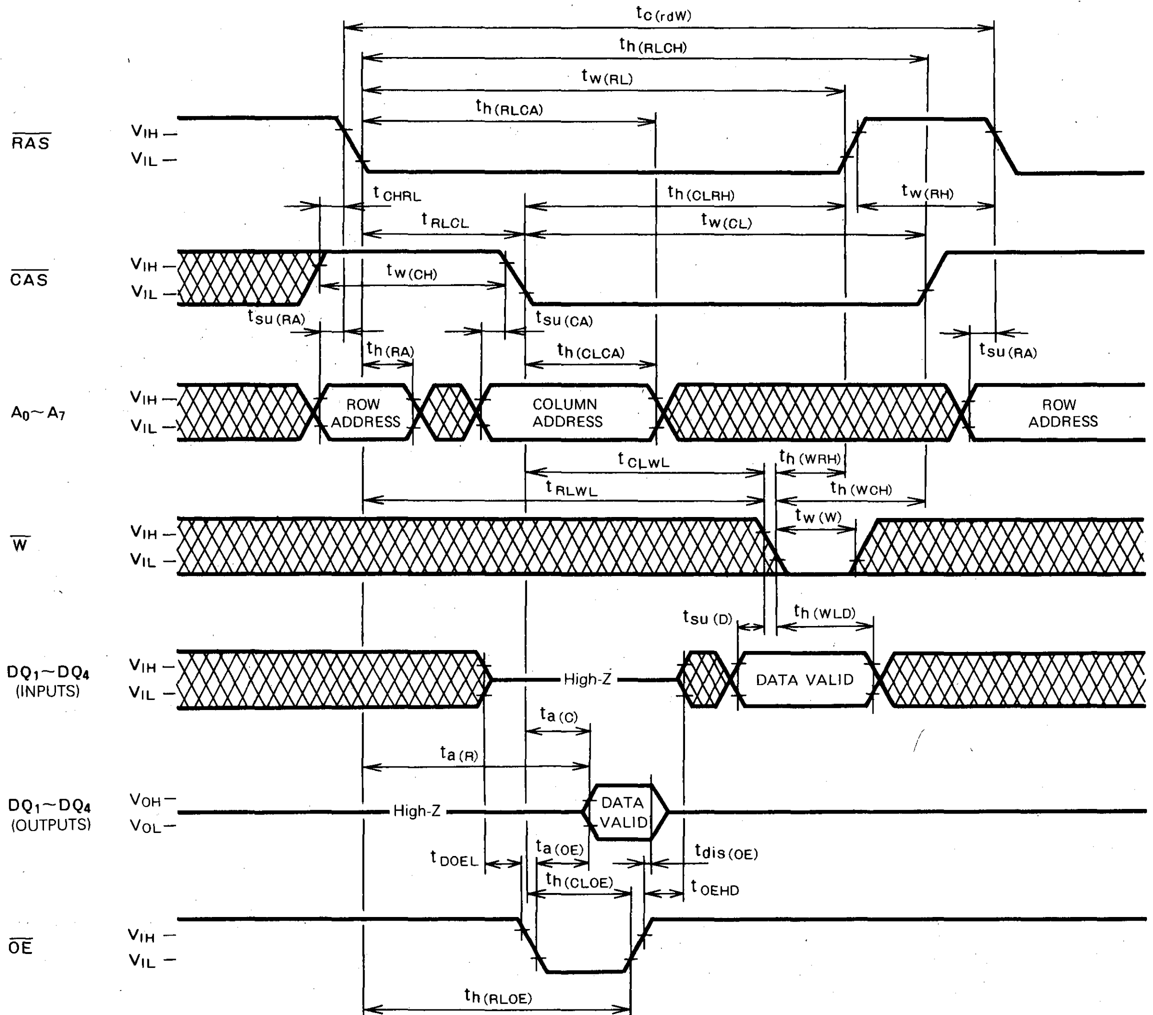
Write Cycle (Early Write)



Write Cycle (Delayed Write)

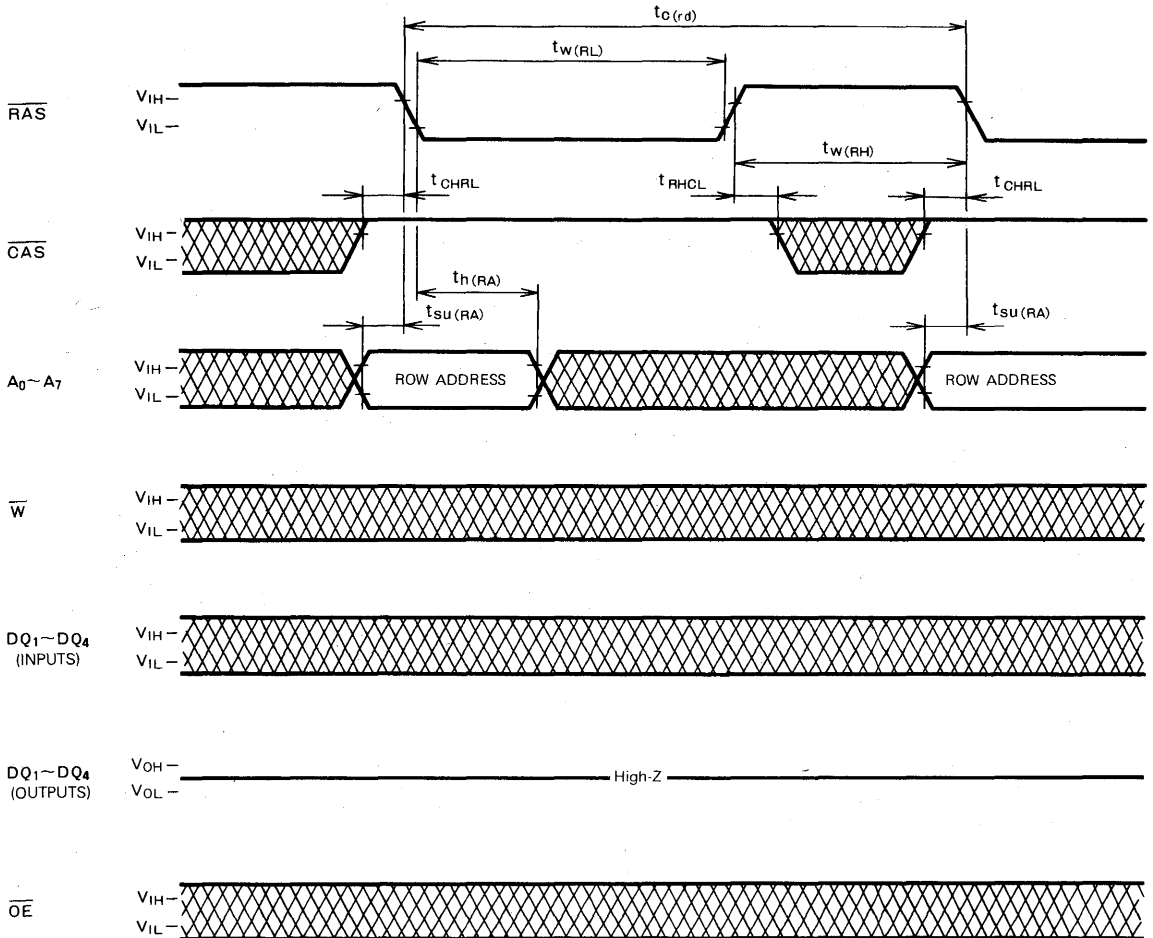


Read-Write and Read-Modify-Write Cycles



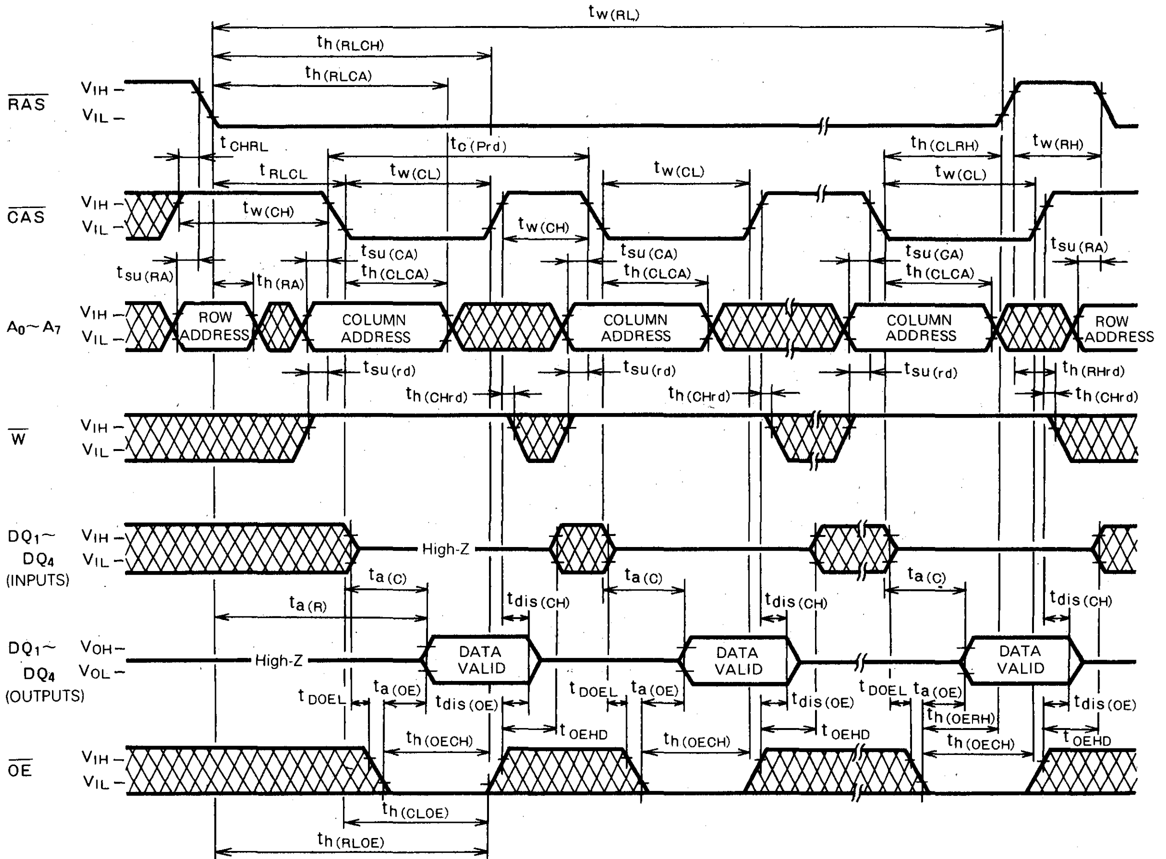
MITSUBISHI ELECTRIC

$\overline{RAS}$-Only Refresh Cycle (Note 22)



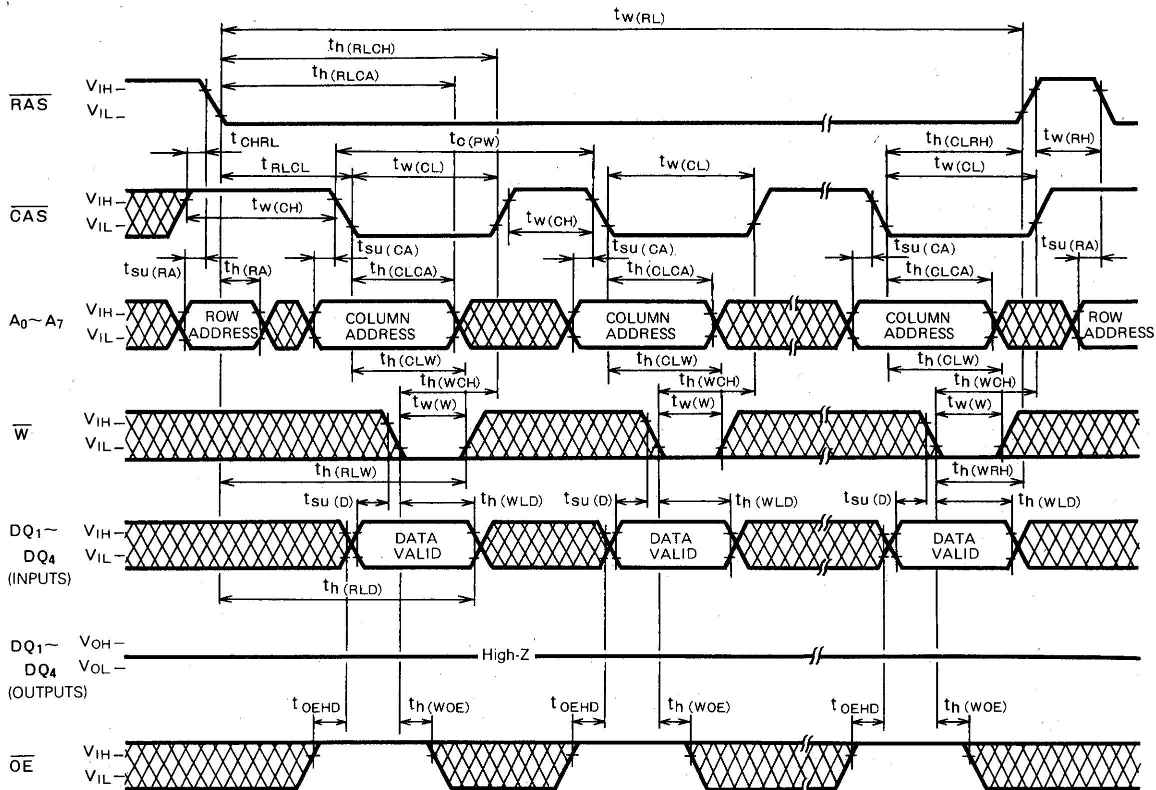
Note 22. A_7 may be V_{IH} or V_{IL}

Page-Mode Read Cycle

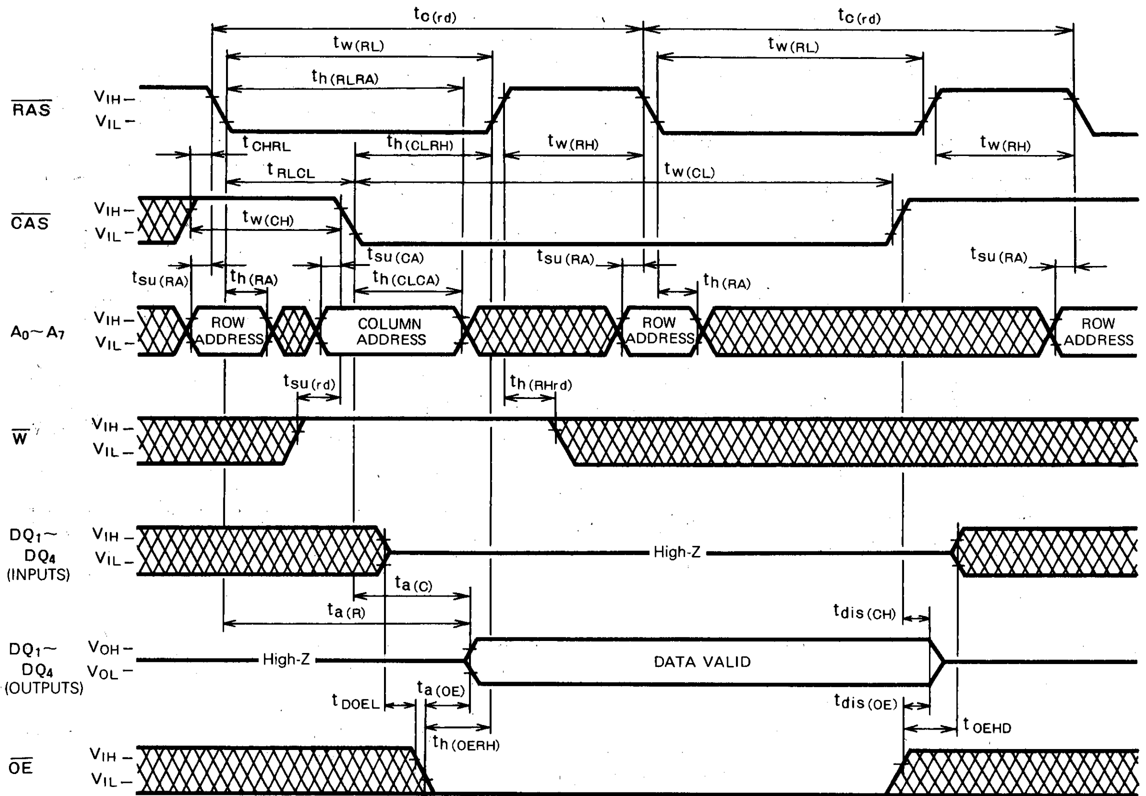


MITSUBISHI ELECTRIC

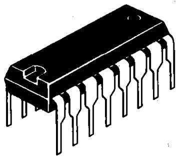
Page-Mode Write Cycle



Hidden Refresh Cycle



MITSUBISHI ELECTRIC



M5M4256P-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

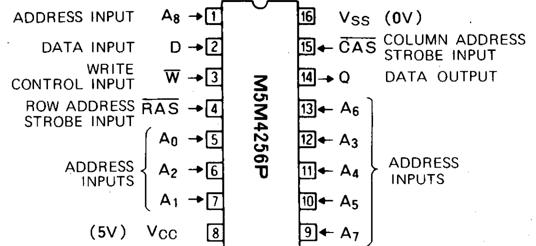
This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4256P-10	100	200	300
M5M4256P-12	120	230	260
M5M4256P-15	150	260	230

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256P-10 .... 385mW (max)
  - M5M4256P-12 .... 360mW (max)
  - M5M4256P-15 .... 330mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

PIN CONFIGURATION (TOP VIEW)

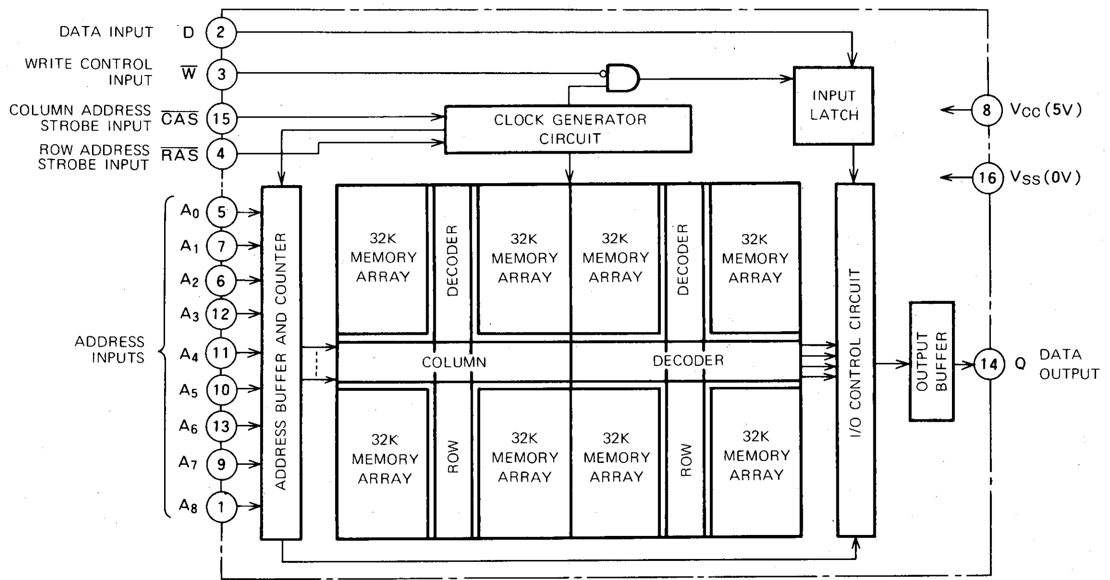


Outline 16P4

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



FUNCTION

The M5M4256P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4256P the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4256P is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256P, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, CAS is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that CAS and/or RAS can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding CAS, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, RAS must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of RAS, because once the row address has been strobed, RAS is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order (RAS) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. RAS Only Refresh

In this refresh method, the CAS clock should be at a V_{IH} level and the system must perform RAS Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the RAS clock and associated internal row locations are refreshed. A RAS Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. CAS before RAS Refresh

If CAS falls $t_{SUR(CAS\text{-}RAS)}$ earlier than RAS and if CAS is kept low by $t_{hR(RAS\text{-}CAS)}$ after RAS falls, CAS before RAS Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If CAS is kept low after the above operation, RAS cycle initiates RAS Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing RAS high and then low while CAS remains high initiates the normal RAS Only Refresh using the external address.

If CAS is kept low after the normal read/write cycle, RAS cycle initiates the RAS Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit CAS is brought high.

4. Hidden Refresh

A feature of the M5M4256P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the CAS active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period, executing a RAS-only cycling, but with CAS held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the CAS asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4256P is dynamic, and most of the power is dissipated when addresses are strobed. Both RAS and CAS are decoded and applied to the M5M4256P as chip-select in the memory system, but if RAS is decoded, all unselected devices go into stand-by independent of the CAS condition, minimizing system power dissipation.

Power Supplies

The M5M4256P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1∼7	V
V_I	Input voltage		−1∼7	V
V_O	Output voltage		−1∼7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	1000	mW
T_{opr}	Operating temperature		0∼70	°C
T_{stg}	Storage temperature		−65∼150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0∼70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0∼70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4256P-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open			70	mA
		M5M4256P-12				65	
		M5M4256P-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = \overline{CAS} = V_{IH}$ output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4256P-10	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(\overline{RAS})}$ = min, output open			60	mA
		M5M4256P-12				55	
		M5M4256P-15				50	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4).	M5M4256P-10	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{CPG} = min, output open			55	mA
		M5M4256P-12				50	
		M5M4256P-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4256P-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ = min, output open			65	mA
		M5M4256P-12				60	
		M5M4256P-15				55	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_i = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_i = 25mVrms			7	pF

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

(Ta = 0 ~ 70°C , V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 5, 6 and 7.)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ns
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined at $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\min = t_{h(RAS-RA)}\min + 2t_{THL(tTLH)} + t_{su(CA-CAS)}\min$.

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M5456P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the vauel when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	225		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{\text{RAS}}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{\text{CAS}}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{\text{CAS}}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{\text{RAS}}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{\text{CAS}}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0		0	35	5	40	ns
$t_{a(CAS)}$	$\overline{\text{CAS}}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{\text{RAS}}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15. t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data outputs keep the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	100		125		145		ns
$t_{w(CASH)}$	$\overline{\text{CAS}}$ high pulse width	t_{CP}	40		55		60		ns
t_{CPGRW}	Page-mode read-write cycle time	t_{PCRW}	130		160		180		ns

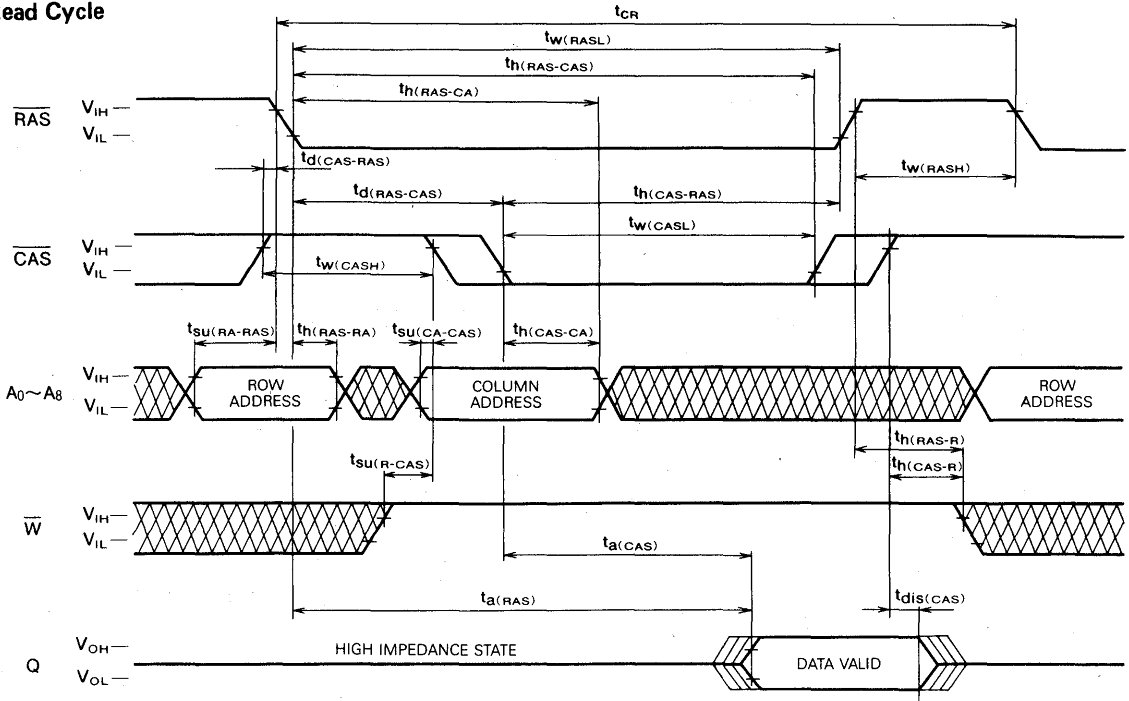
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-10		M5M4256P-12		M5M4256P-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{\text{CAS}}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{\text{CAS}}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{\text{CAS}}$ active time	t_{RPC}	0		0		0		ns

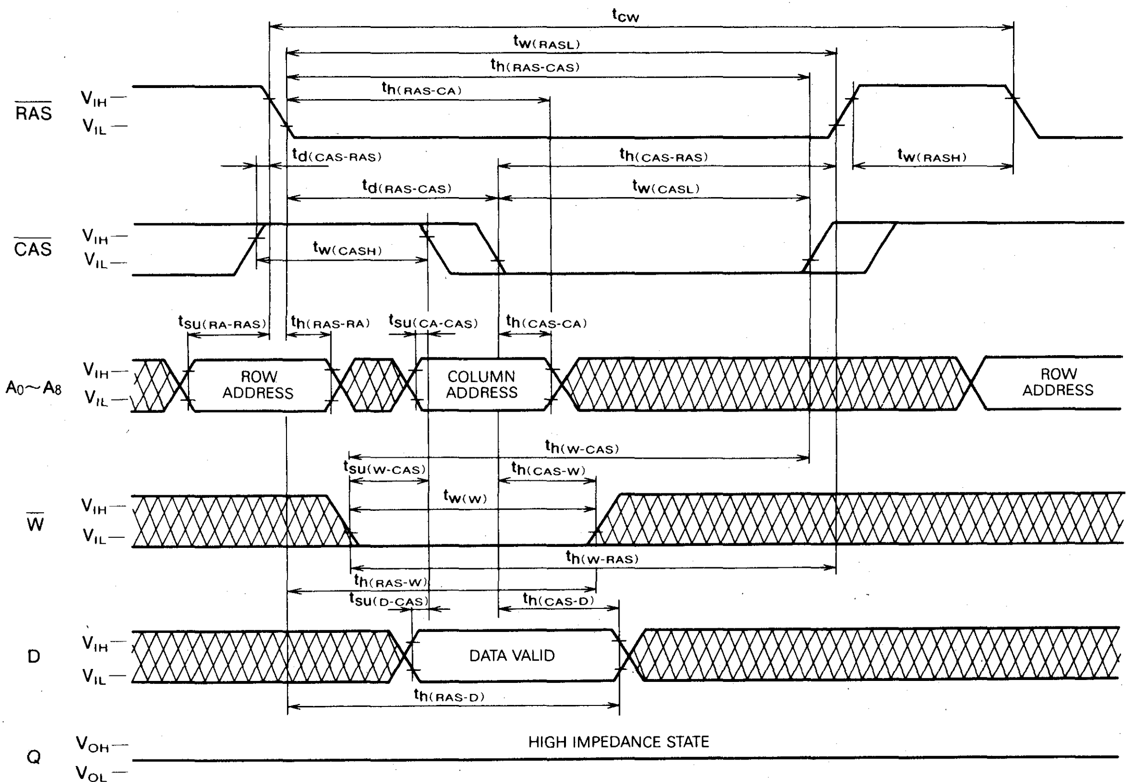
Note 18. Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles is necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

TIMING DIAGRAMS (Note 19)

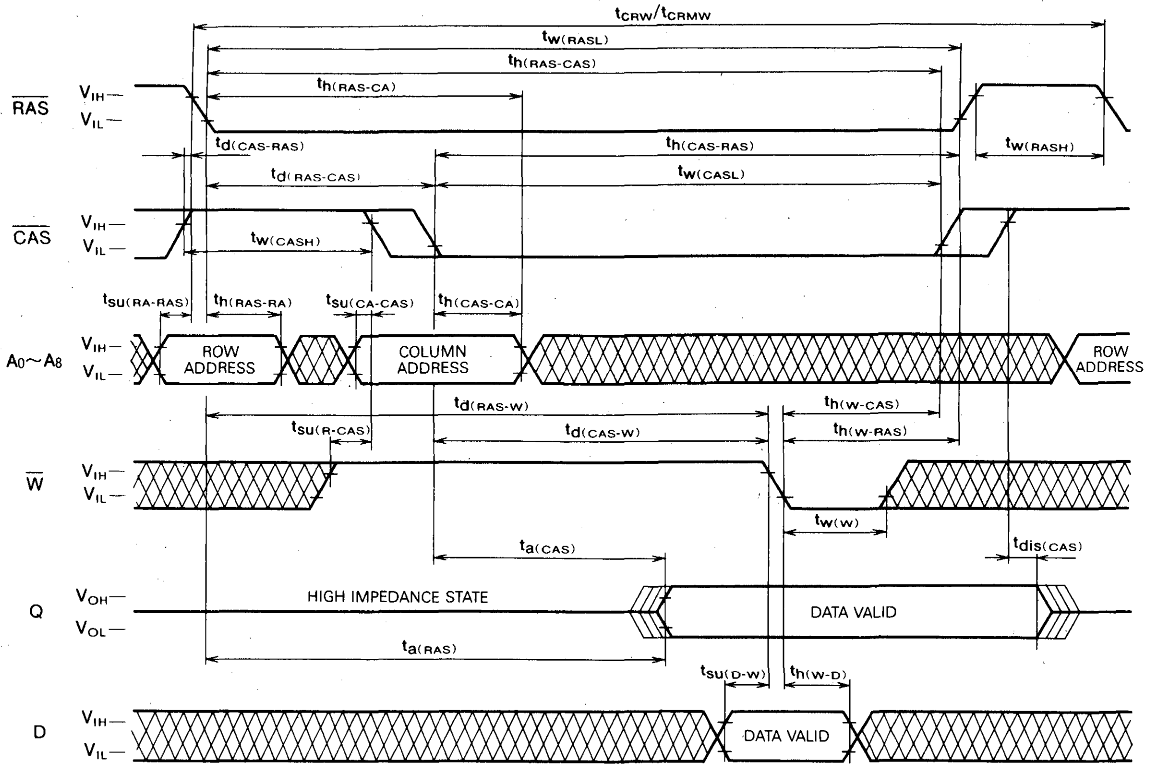
Read Cycle



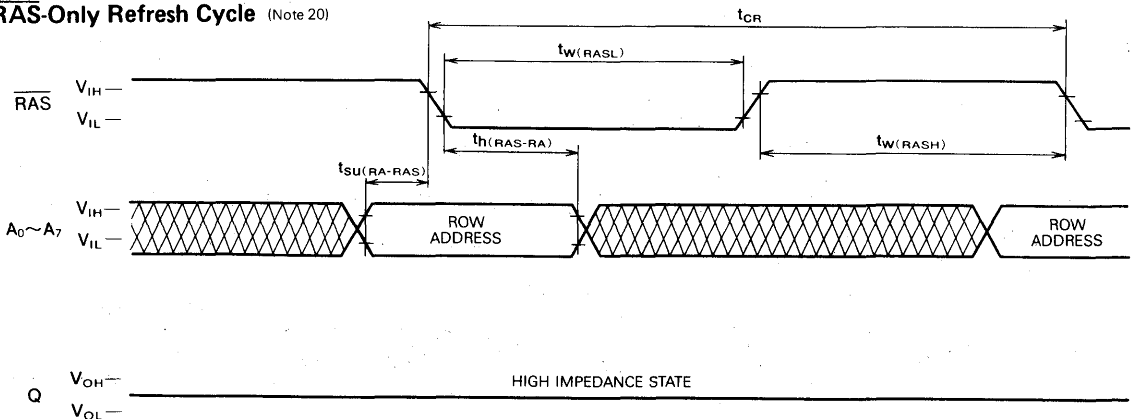
Write Cycle (Early Write)

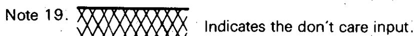


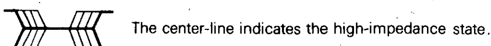
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

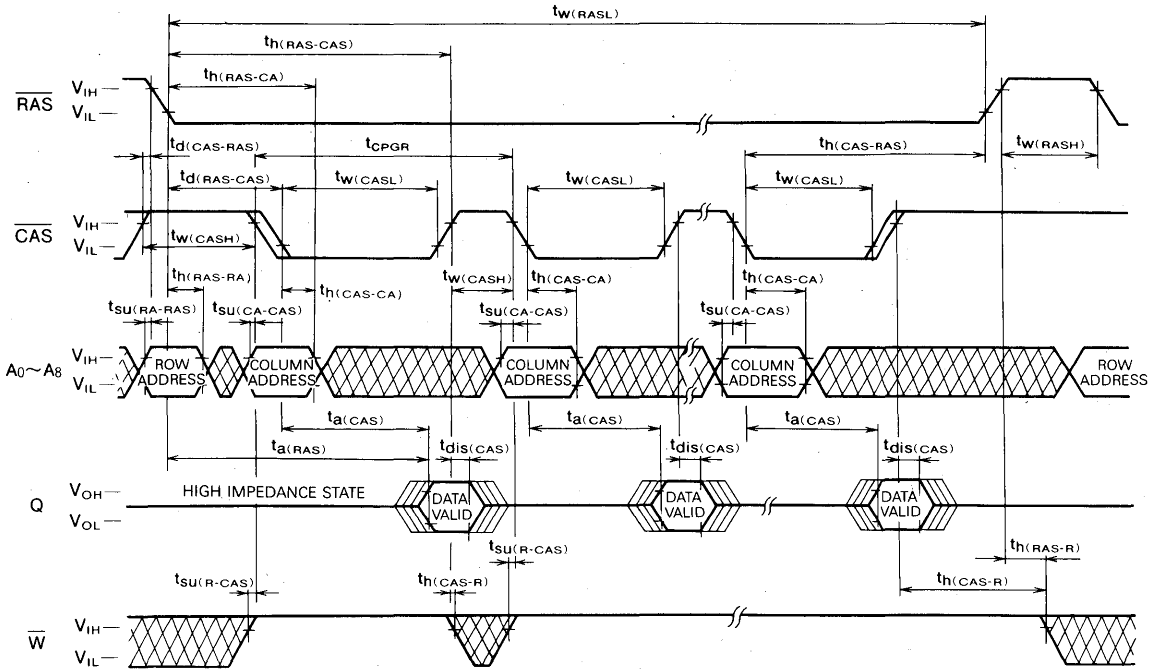


Note 19.  Indicates the don't care input.

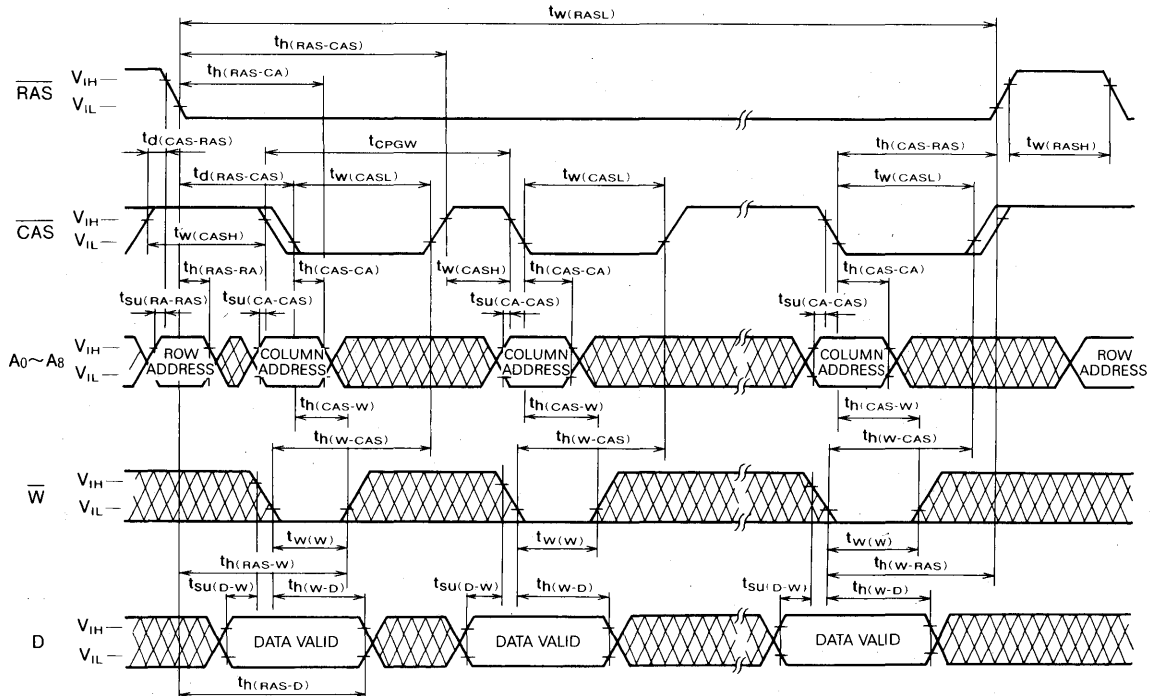
 The center-line indicates the high-impedance state.

Note 20. $\overline{CAS}=V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

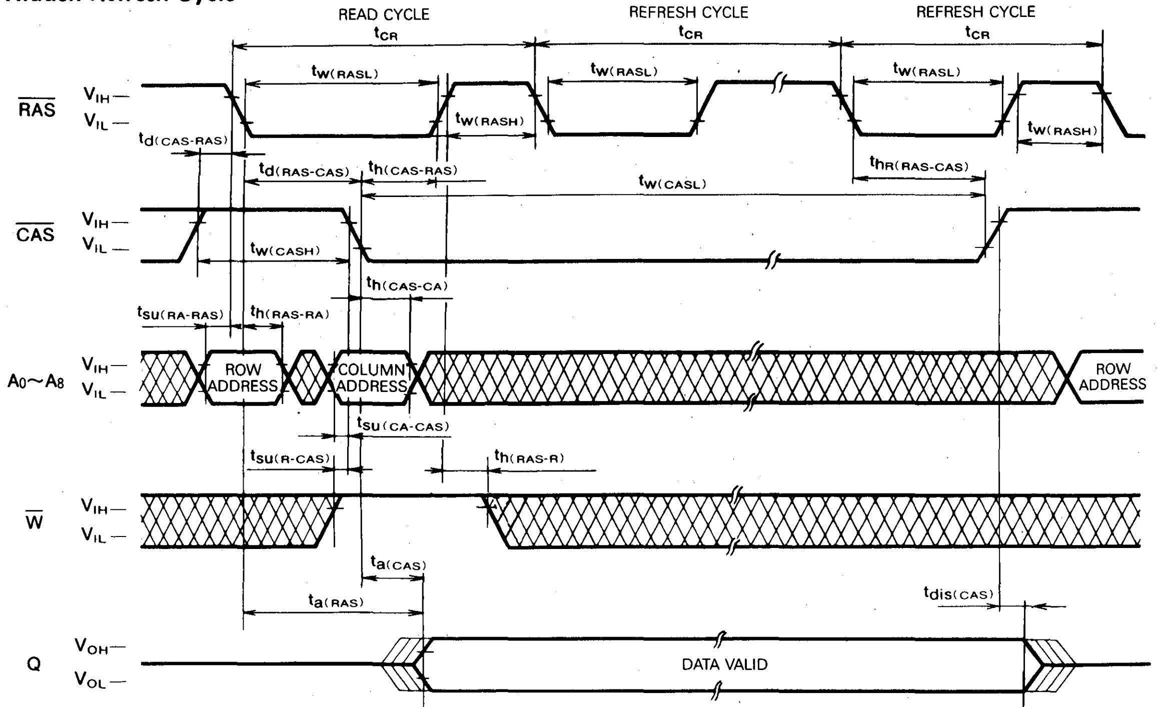
Page-Mode Read Cycle



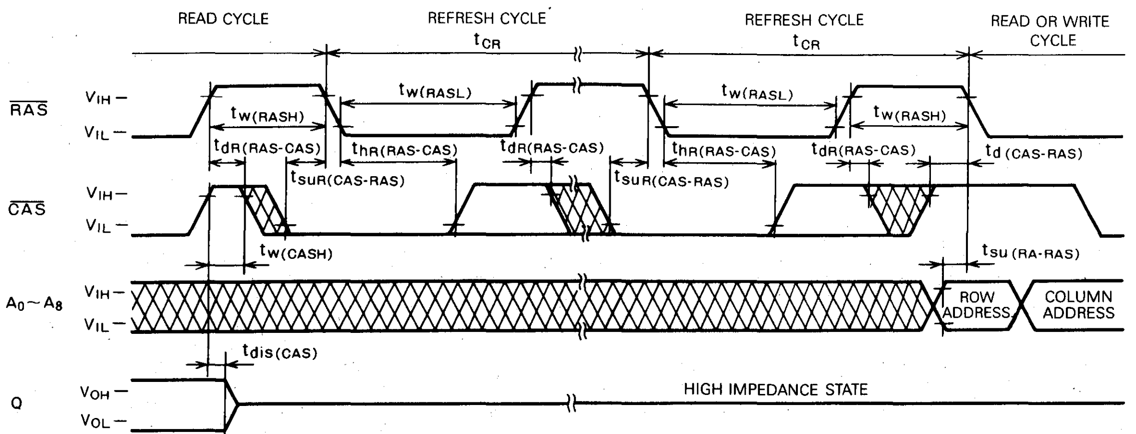
Page-Mode Write Cycle



Hidden Refresh Cycle



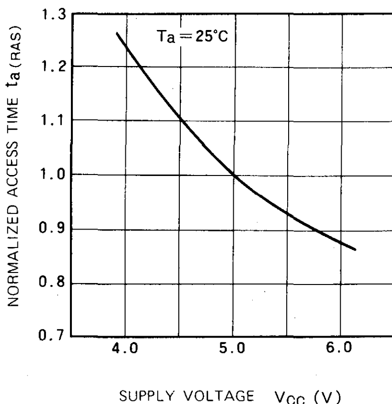
CAS before RAS Refresh Cycle (Note 21)



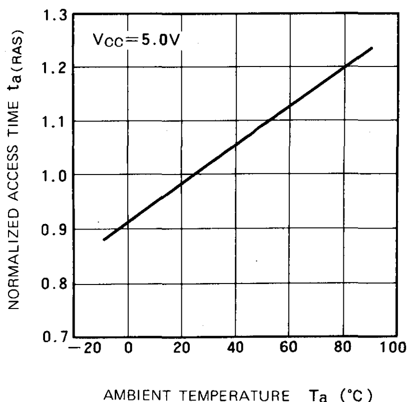
Note 21. W, D = don't care.

TYPICAL CHARACTERISTICS

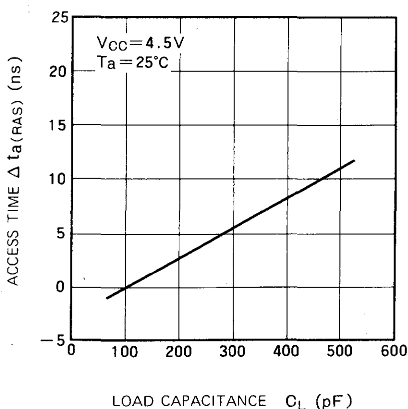
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



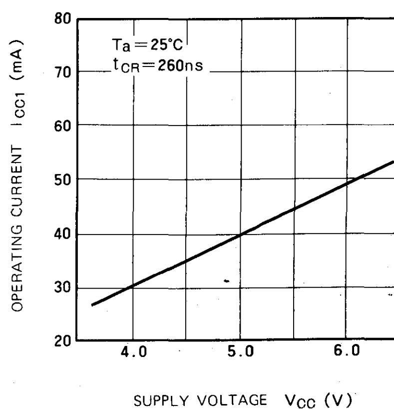
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



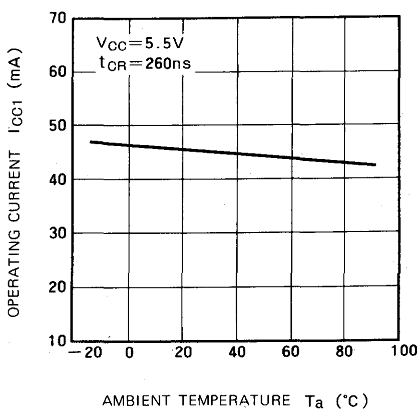
ACCESS TIME VS. LOAD CAPACITANCE



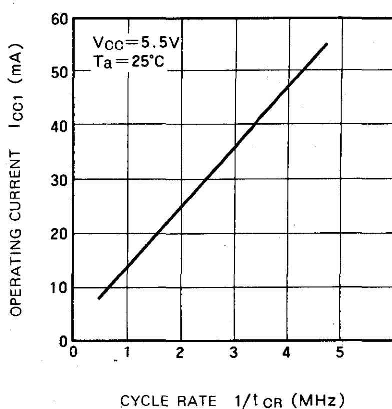
OPERATING CURRENT VS. SUPPLY VOLTAGE



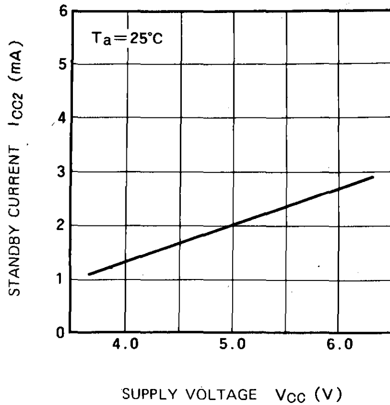
OPERATING CURRENT VS. AMBIENT TEMPERATURE



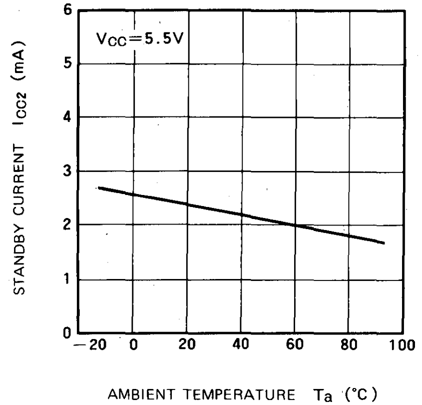
OPERATING CURRENT VS. CYCLE RATE



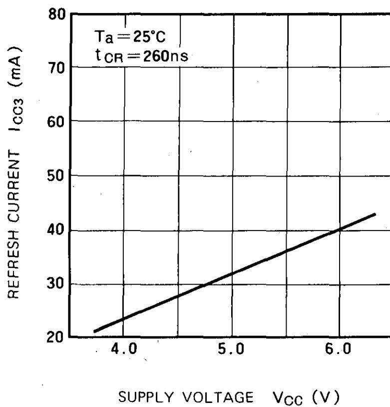
STANDBY CURRENT VS. SUPPLY VOLTAGE



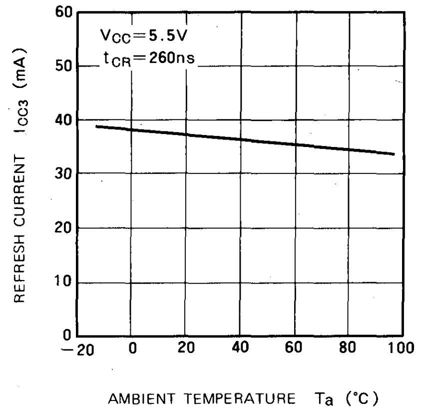
STANDBY CURRENT VS. AMBIENT TEMPERATURE



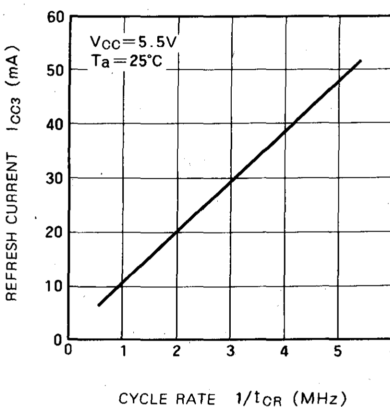
REFRESH CURRENT VS. SUPPLY VOLTAGE



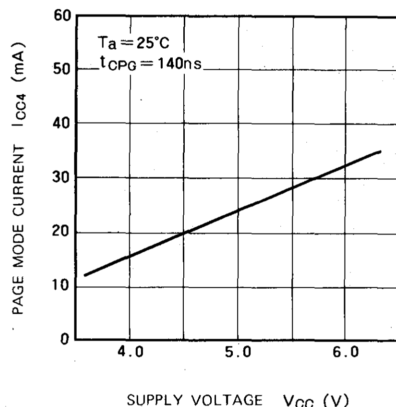
REFRESH CURRENT VS. AMBIENT TEMPERATURE



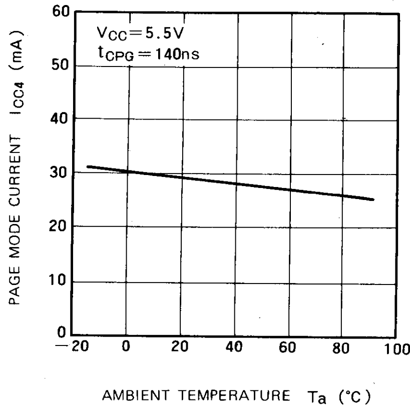
REFRESH CURRENT VS. CYCLE RATE



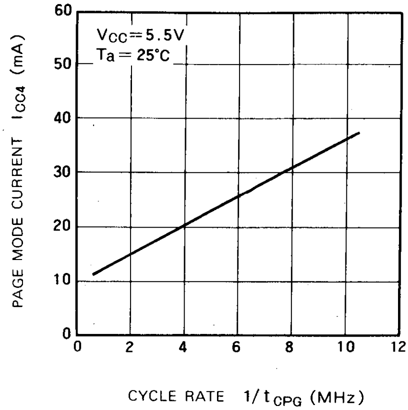
PAGE MODE CURRENT VS. SUPPLY VOLTAGE



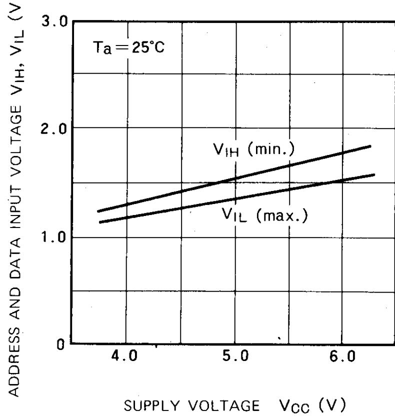
PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



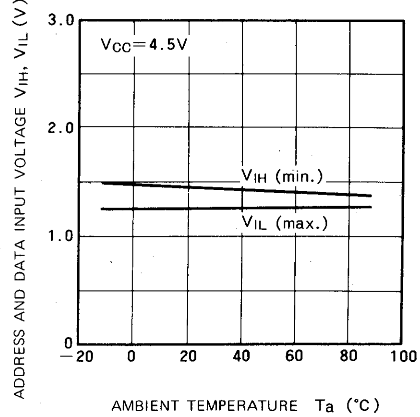
PAGE MODE CURRENT VS. CYCLE RATE



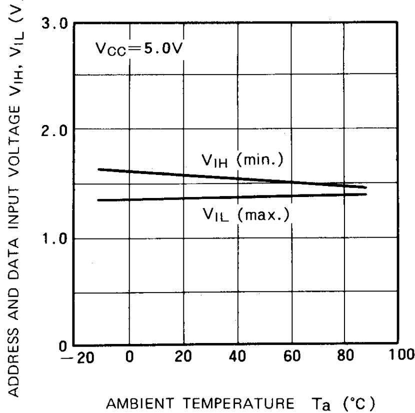
ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



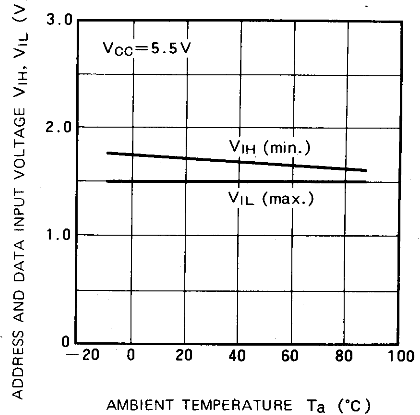
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



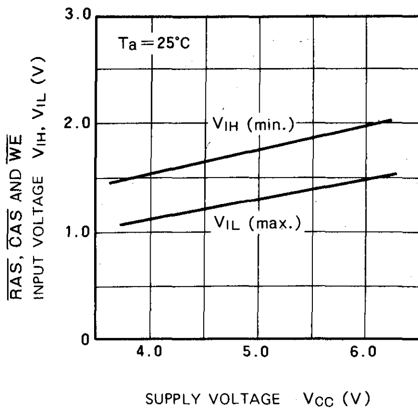
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



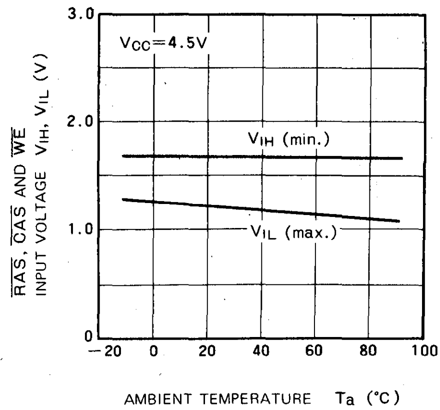
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



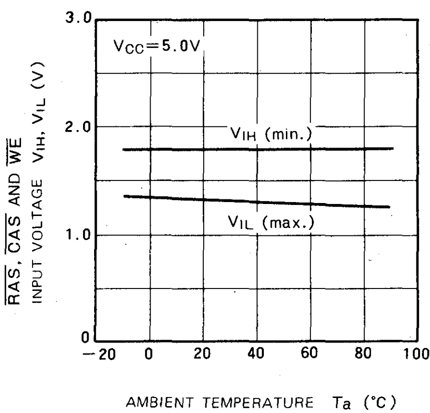
RAS, CAS AND WE INPUT VOLTAGE VS. SUPPLY VOLTAGE



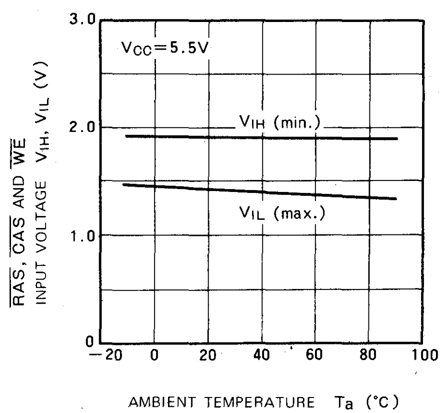
RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE

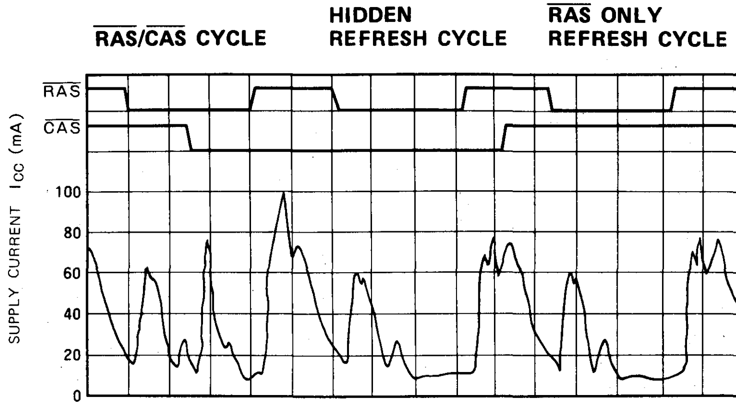


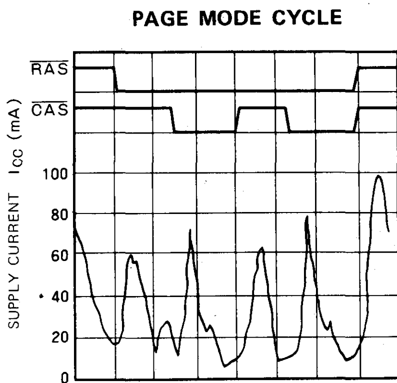
RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE

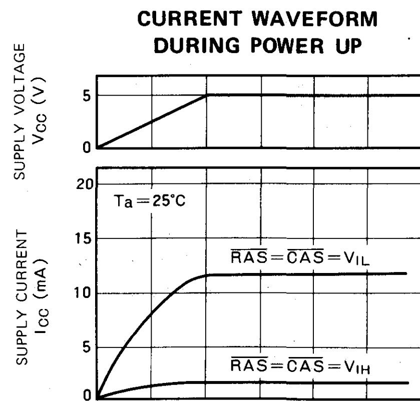


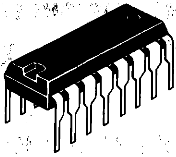
RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE




RAS/CAS CYCLE
HIDDEN REFRESH CYCLE
RAS ONLY REFRESH CYCLE
RAS
CAS
SUPPLY CURRENT Icc (mA)
100
80
60
40
20
0
50ns/DIVISION


PAGE MODE CYCLE
RAS
CAS
SUPPLY CURRENT Icc (mA)
100
80
60
40
20
0
50ns/DIVISION


CURRENT WAVEFORM DURING POWER UP
SUPPLY VOLTAGE Vcc (V)
5
0
SUPPLY CURRENT Icc (mA)
20
15
10
5
0
Ta=25°C
RAS=CAS=VIL
RAS=CAS=VIH
50μs/DIVISION



M5M4257P-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

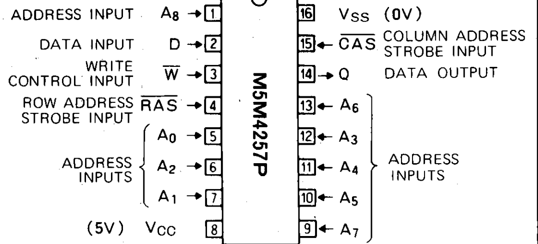
This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4257P-10	100	200	300
M5M4257P-12	120	230	260
M5M4257P-15	150	260	230

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257P-10 .... 385mW (max)
  - M5M4257P-12 .... 360mW (max)
  - M5M4257P-15 .... 330mW (max)
- Unlatched output enables two-dimensional chip selection

PIN CONFIGURATION (TOP VIEW)



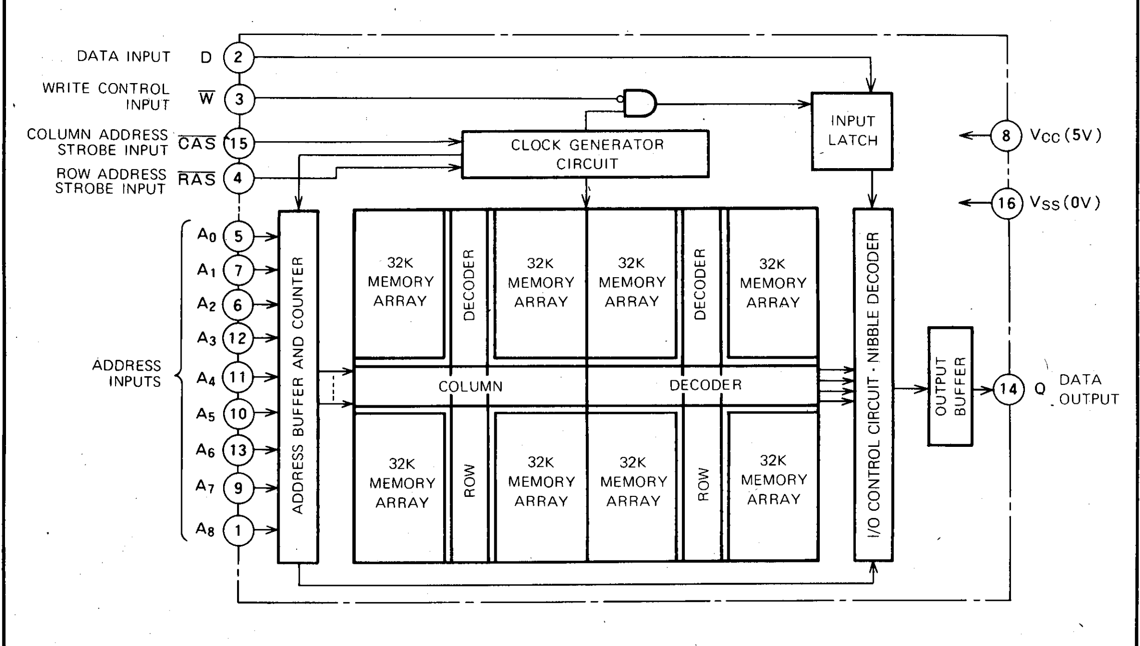
Outline 16P4

- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities. (Pin 1 is used for nibble mode)
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

FUNCTION

The M5M4257P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Nibble mode identical and Nibble mode column address is DNC while toggling $\overline{CAS}$.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4257P the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\ (RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4257P is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257P, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Nibble-Mode Operation

The M5M4257P is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4257P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4257P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4257P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4257P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V ± 10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}, Other input pins ＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4257P-10	$\overline{RAS}$, $\overline{CAS}$ cycling t_{CR}＝t_{CW}＝ min. output open			70	mA
		M5M4257P-12				65	
		M5M4257P-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$＝$\overline{CAS}$＝V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4257P-10	$\overline{RAS}$ cycling $\overline{CAS}$＝V_{IH} $t_{C(\overline{RAS})}$＝ min, output open			60	mA
		M5M4257P-12				55	
		M5M4257P-15				50	
$I_{CC5(AV)}$	Average supply current from V_{CC} nibble mode	M5M4257P-10	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling t_{CN}＝ min, output open			35	mA
		M5M4257P-12				30	
		M5M4257P-15				25	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4257P-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ ＝ min, output open			65	mA
		M5M4257P-12				60	
		M5M4257P-15				55	
$C_{I(A)}$	Input capacitance, address inputs		V_I＝V_{SS} f＝1MHz V_i＝25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		V_O＝V_{SS}, f＝1MHz, V_i＝25mVrms			7	pF

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ns
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	75	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		20		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		25		20		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		100		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for nibble-mode.
9: $t_{d(RAS-CAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}max$ can be met. $t_{d(RAS-CAS)max}$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL}(t_{TLH}) + t_{su(CA-CAS)min}$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)}max$ defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}max$. Test conditions ; Load = 2TTL, C_L = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}max$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}max$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL C_L = 100pF

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	225		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15. t_{CRW}min is defined as $t_{CRW}min = t_{d(RAS-CAS)}max + t_{d(CAS-W)}min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as $t_{CRMW}\ min = t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geq t_{d(RAS-W)}min$, and $t_{d(CAS-W)} \geq t_{su(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Nibble-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
t_{CN}	Nibble mode cycle time	t_{NC}	50		55		70		ns
$t_{aN(CAS)}$	Nibble mode access time	t_{NAC}		25		30		40	ns
$t_{WN(CASL)}$	Nibble mode $\overline{CAS}$ low pulse width	t_{NCAS}	25		30		40		ns
$t_{WN(CASH)}$	Nibble mode precharge time	t_{NP}	15		15		20		ns
$t_{hN(CAS-RAS)}$	Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25		30		40		ns
$t_{dN(CAS-W)}$	Nibble mode $\overline{CAS}$ to WRITE delay	t_{NCWD}	25		30		40		ns
$t_{WNRMW(CASL)}$	Nibble mode RMW $\overline{CAS}$ pulse width	t_{NCRW}	55		65		85		ns
$t_{hNRMW(W-CAS)}$	Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		30		40		ns
$t_{hNRMW(CAS-RAS)}$	Nibble mode RMW $\overline{RAS}$ hold time	t_{NWSH}	55		65		85		ns
$t_{suN(W-CAS)}$	Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$	t_{NWCS}	0		0		0		ns

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257P-10		M5M4257P-12		M5M4257P-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

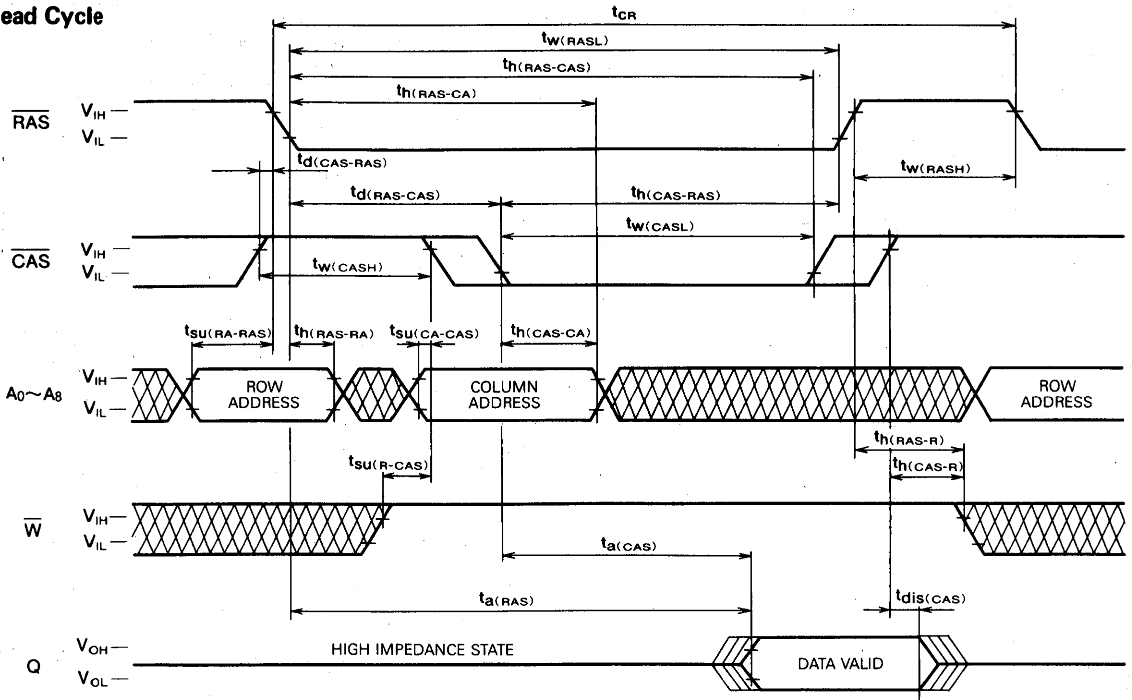
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Nibble Mode Addressing Sequence Example

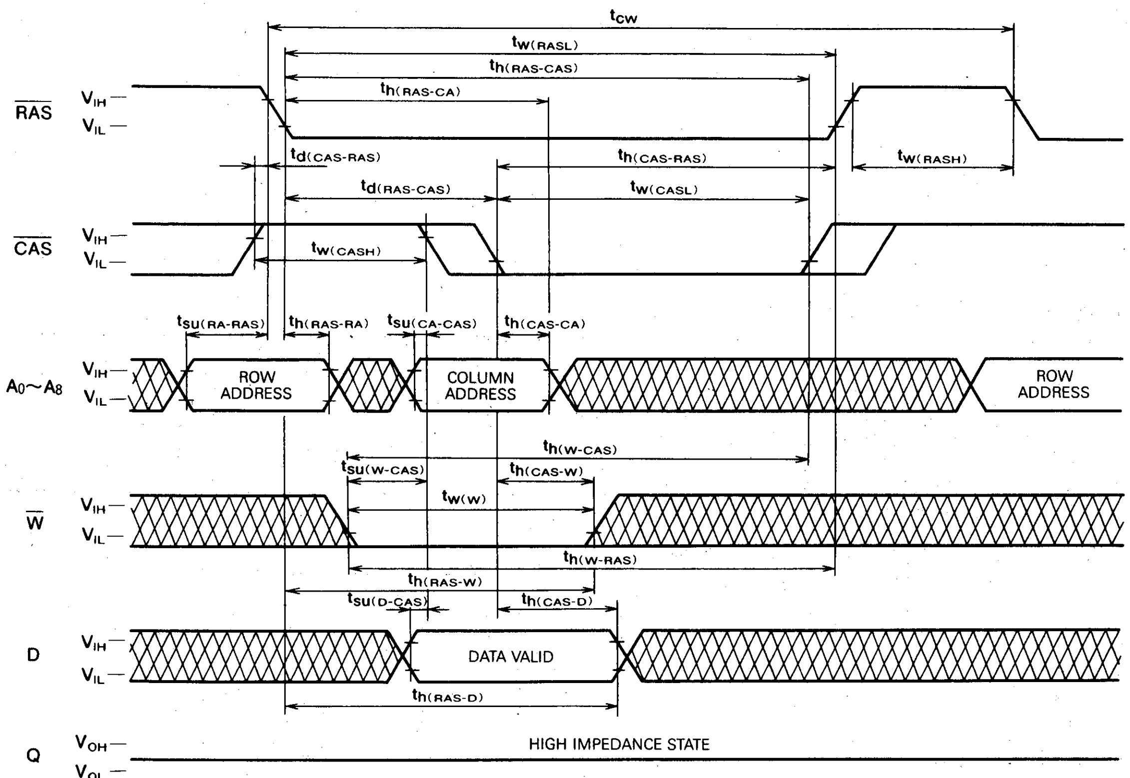
Sequence	Nibble bit	Column address									Row address									
		A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	External address
toggle $\overline{CAS}$	2	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	1	Internally generated address
toggle $\overline{CAS}$	3	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	
toggle $\overline{CAS}$	4	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	1	
toggle $\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	

TIMING DIAGRAMS (Note 19)

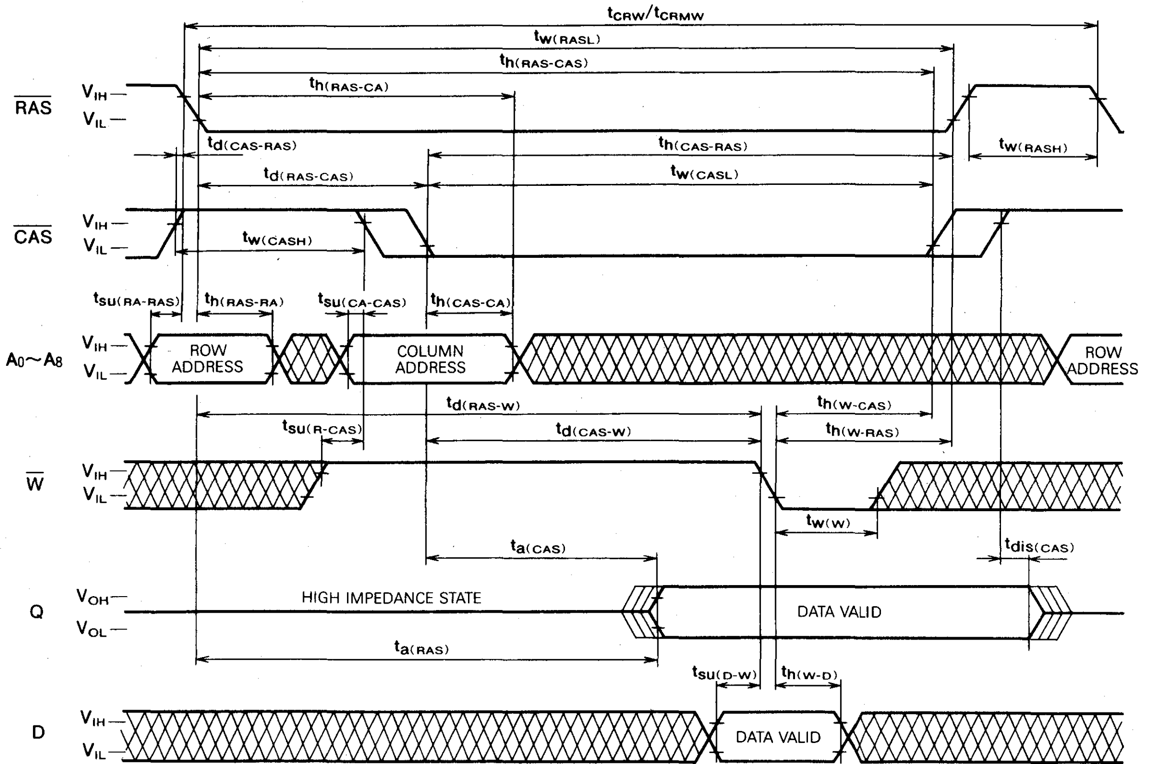
Read Cycle



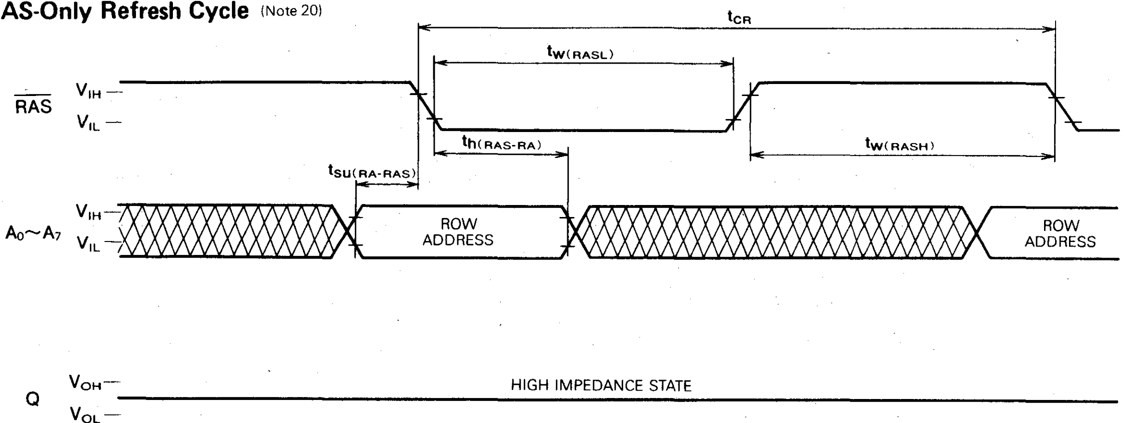
Write Cycle (Early Write)



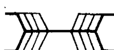
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

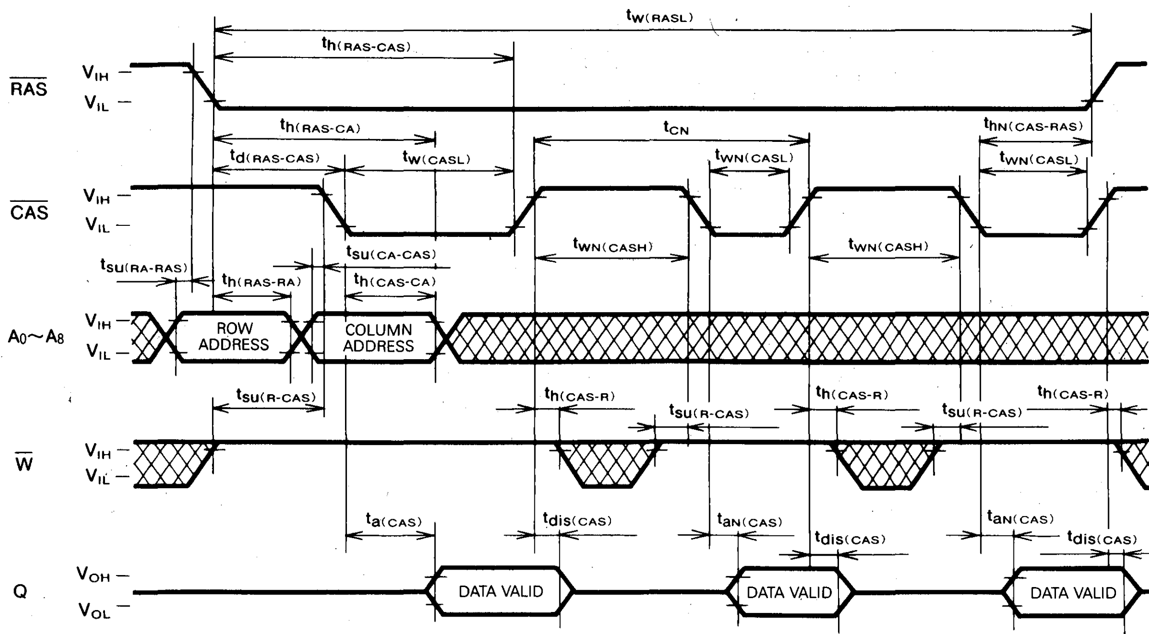


Note 19. Indicates the don't care input.

 The center-line indicates the high-impedance state.

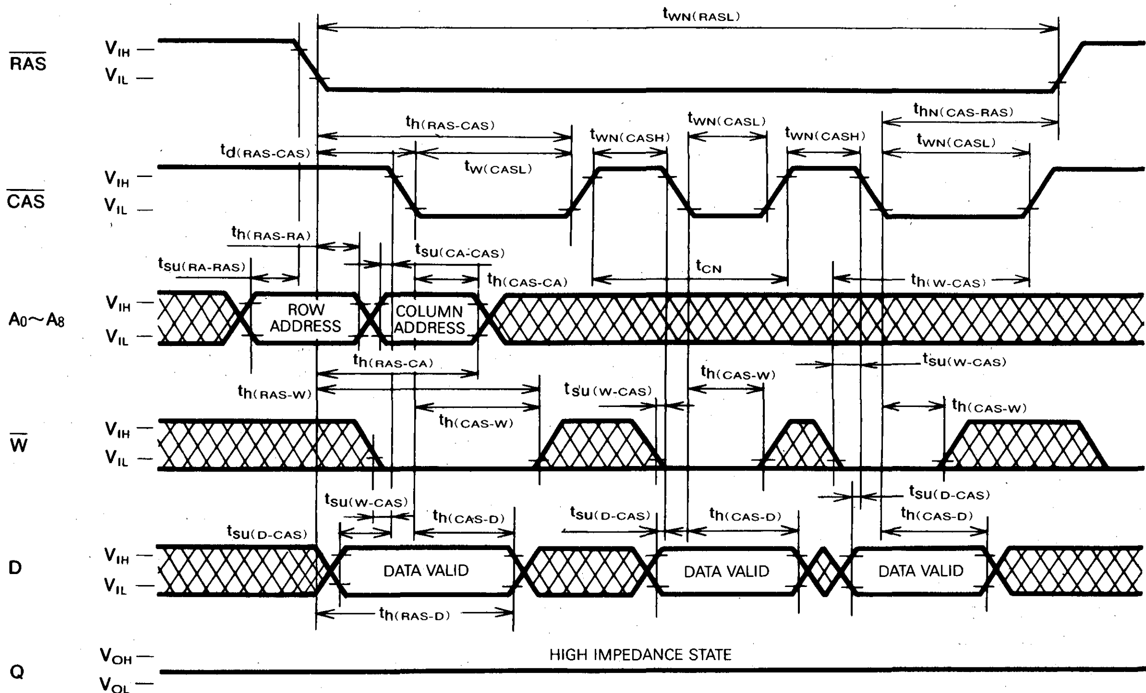
Note 20. $\overline{CAS}$ = VIH, $\overline{W}$, D = don't care.
A8 may be VIH or VIL.

Nibble Mode Read Cycle (Note 21)



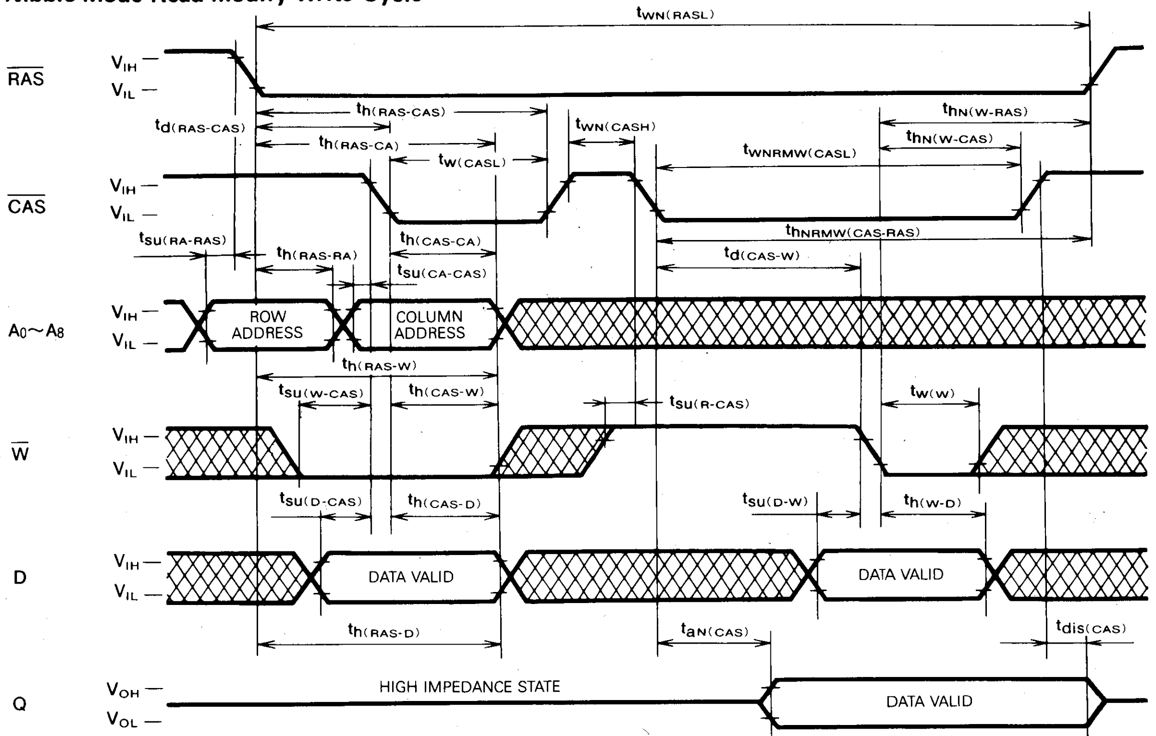
Note 21: Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

Nibble Mode Write Cycle (Early Write)

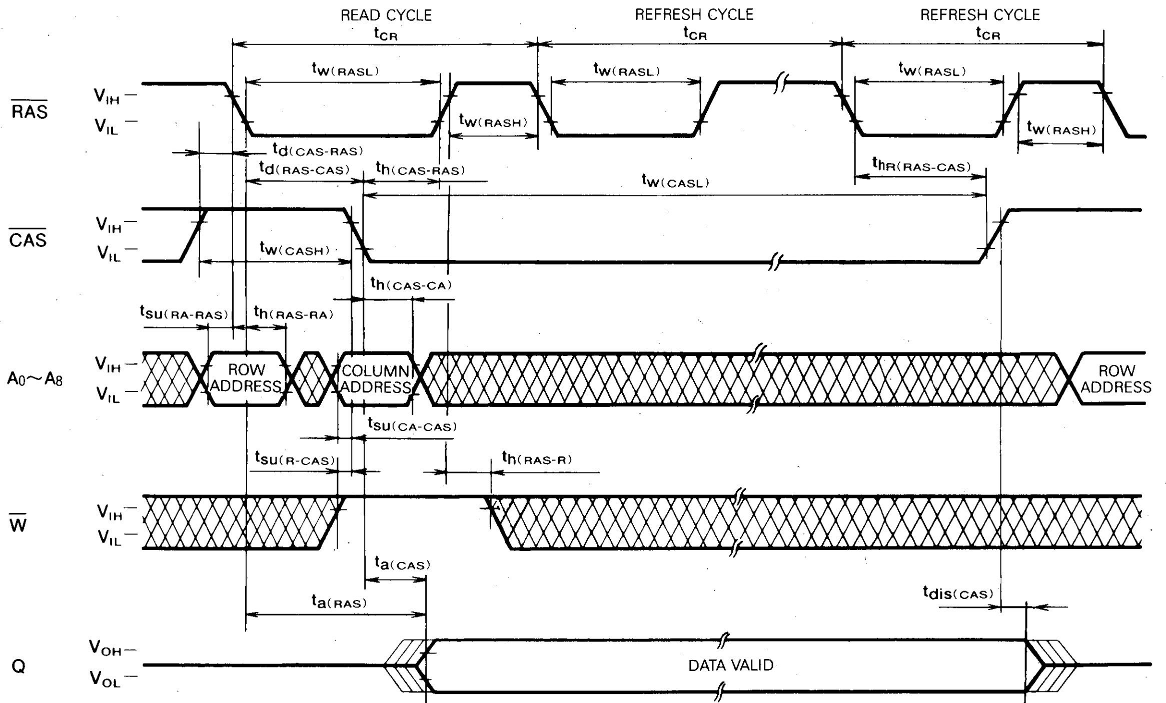


MITSUBISHI ELECTRIC

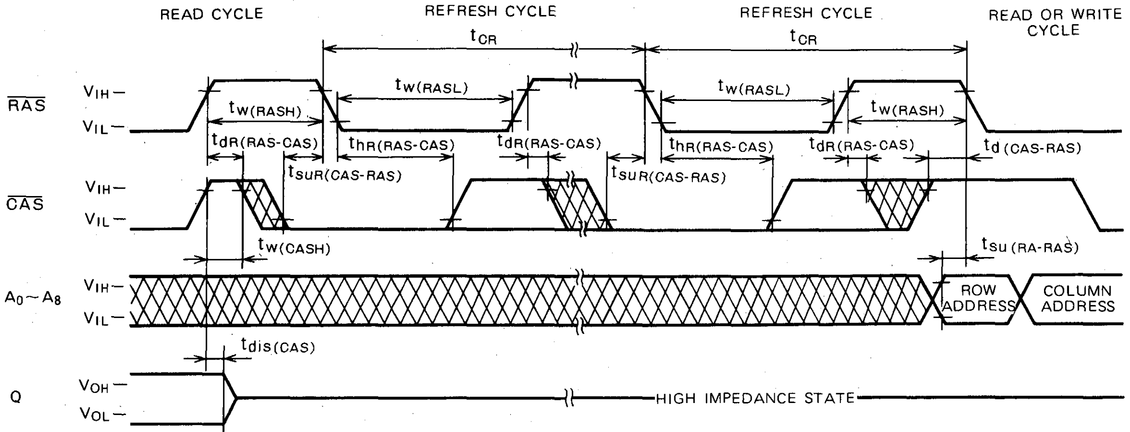
Nibble Mode Read-Modify-Write Cycle



Hidden Refresh Cycle



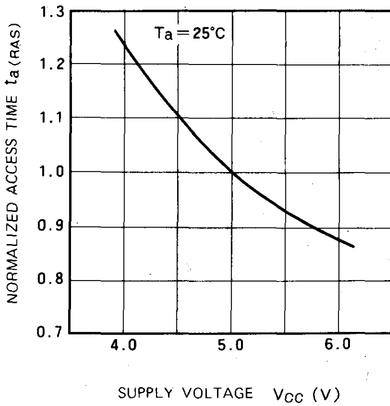
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 22)



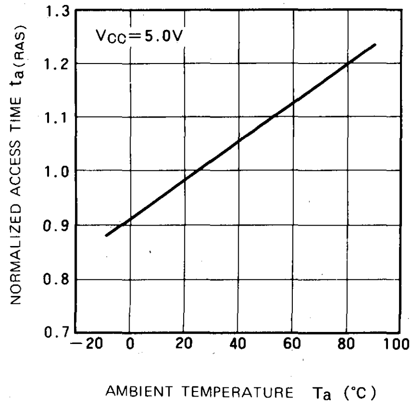
Note 22: $\overline{\text{W}}$, D = don't care.

TYPICAL CHARACTERISTICS

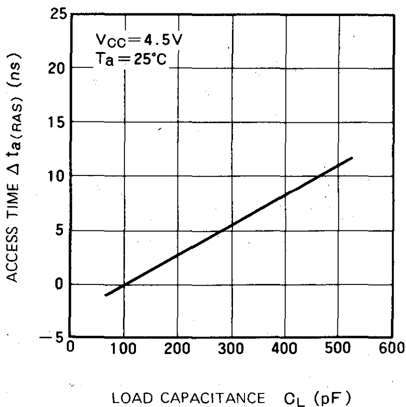
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



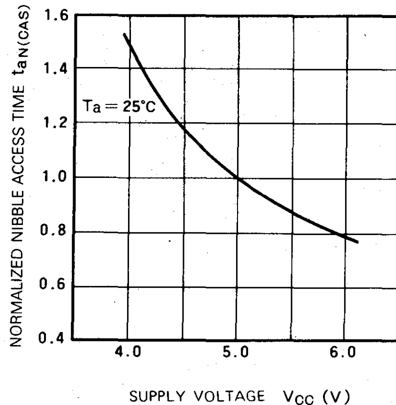
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE

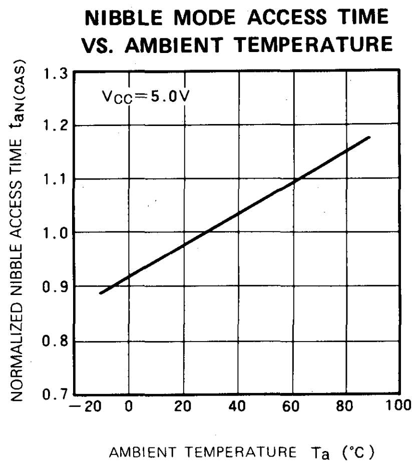


NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE

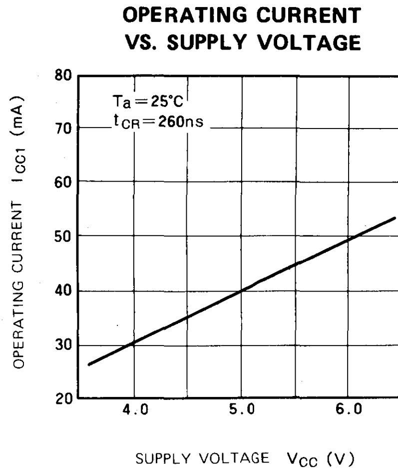


262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

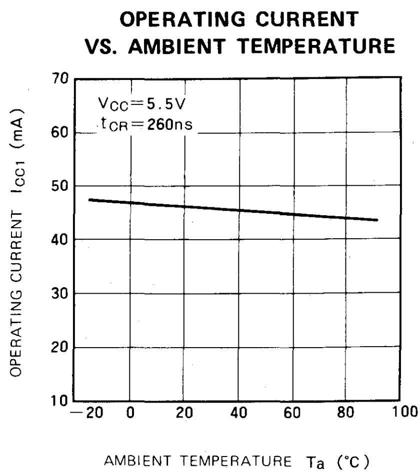
NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



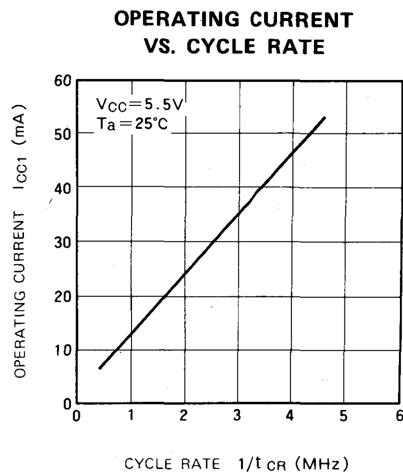
OPERATING CURRENT VS. SUPPLY VOLTAGE



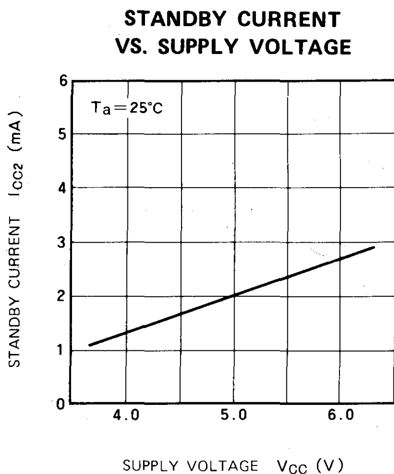
OPERATING CURRENT VS. AMBIENT TEMPERATURE



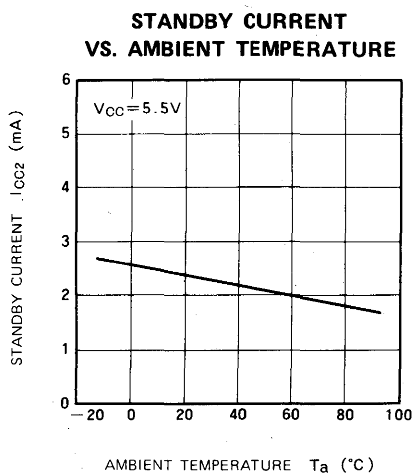
OPERATING CURRENT VS. CYCLE RATE

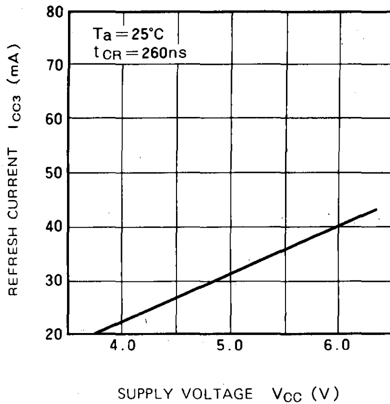


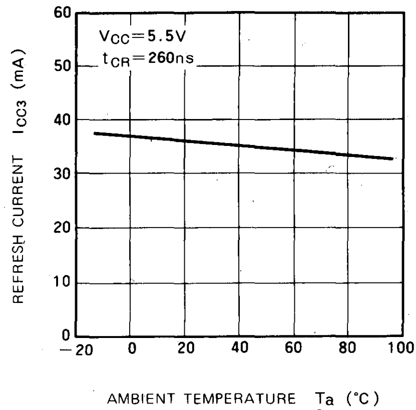
STANDBY CURRENT VS. SUPPLY VOLTAGE

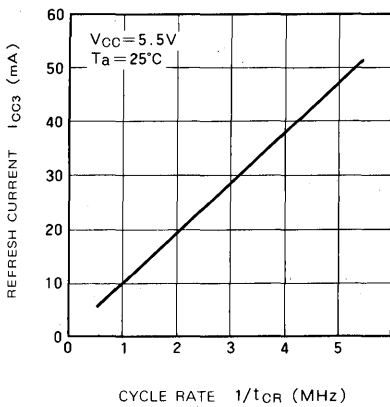


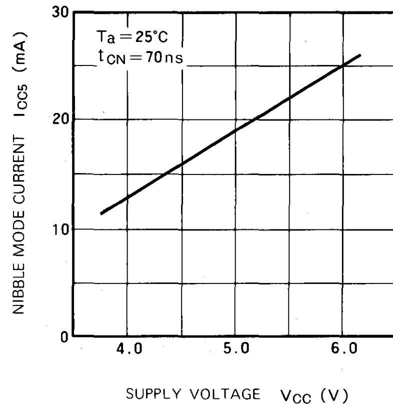
STANDBY CURRENT VS. AMBIENT TEMPERATURE

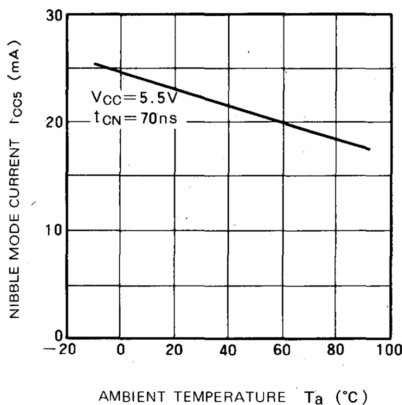


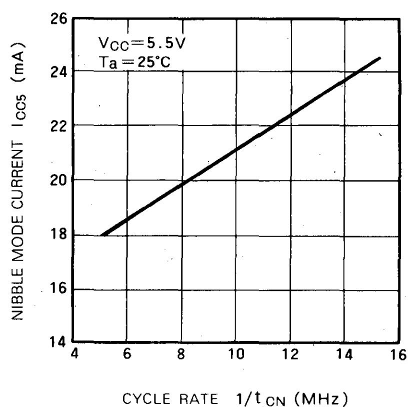

REFRESH CURRENT
VS. SUPPLY VOLTAGE
Ta = 25°C
tCR = 260ns
REFRESH CURRENT ICC3 (mA)
80
70
60
50
40
30
20
4.0
5.0
6.0
SUPPLY VOLTAGE VCC (V)


REFRESH CURRENT
VS. AMBIENT TEMPERATURE
VCC = 5.5V
tCR = 260ns
REFRESH CURRENT ICC3 (mA)
60
50
40
30
20
10
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)

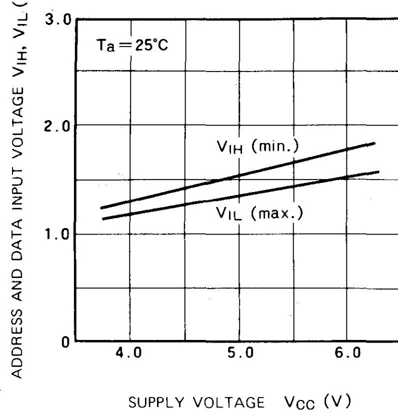

REFRESH CURRENT
VS. CYCLE RATE
VCC = 5.5V
Ta = 25°C
REFRESH CURRENT ICC3 (mA)
60
50
40
30
20
10
0
0
1
2
3
4
5
CYCLE RATE 1/tCR (MHz)


NIBBLE MODE CURRENT
VS. SUPPLY VOLTAGE
Ta = 25°C
tCN = 70ns
NIBBLE MODE CURRENT ICC5 (mA)
30
20
10
0
4.0
5.0
6.0
SUPPLY VOLTAGE VCC (V)

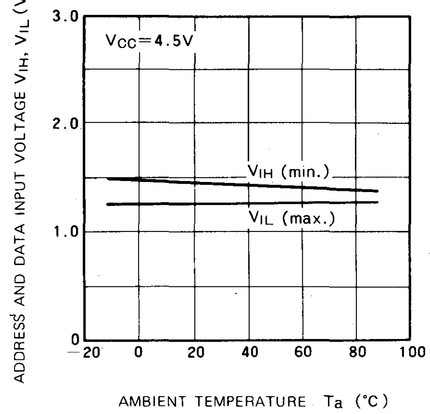

NIBBLE MODE CURRENT
VS. AMBIENT TEMPERATURE
VCC = 5.5V
tCN = 70ns
NIBBLE MODE CURRENT ICC5 (mA)
30
20
10
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)


NIBBLE MODE CURRENT
VS. CYCLE RATE
VCC = 5.5V
Ta = 25°C
NIBBLE MODE CURRENT ICC5 (mA)
26
24
22
20
18
16
14
4
6
8
10
12
14
16
CYCLE RATE 1/tCN (MHz)

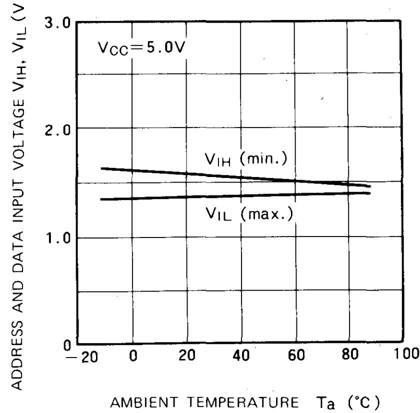
ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



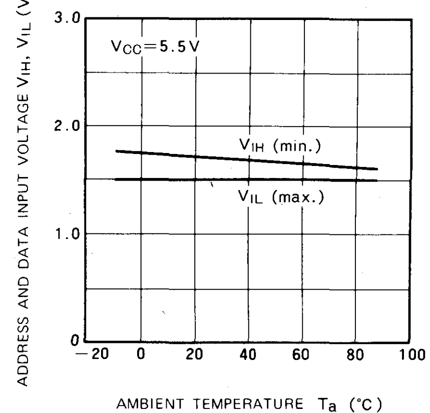
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



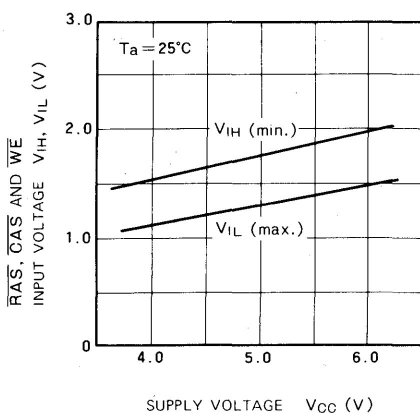
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



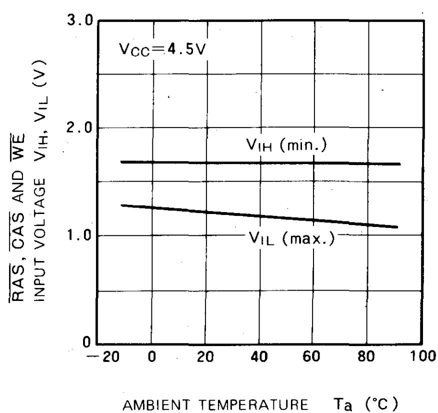
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



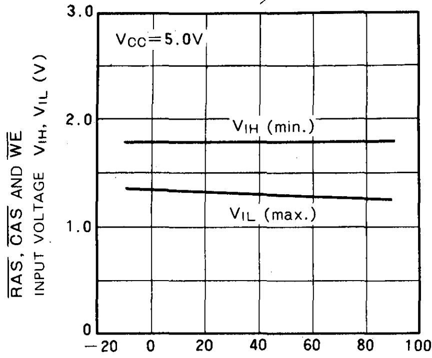
RAS, CAS AND WE INPUT VOLTAGE VS. SUPPLY VOLTAGE



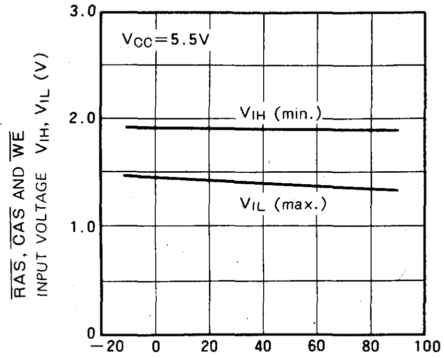
RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE



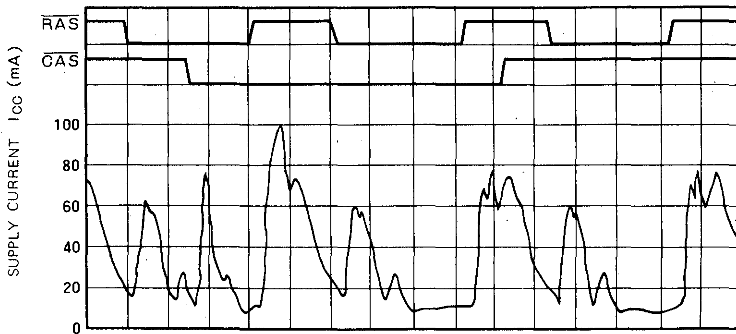
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

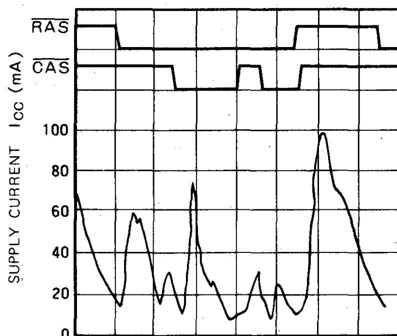


$\overline{RAS}$/$\overline{CAS}$ CYCLE **HIDDEN REFRESH CYCLE** **$\overline{RAS}$ ONLY REFRESH CYCLE**



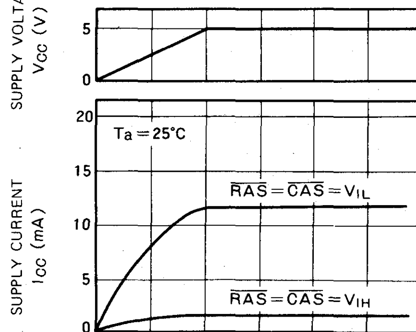
50ns/DIVISION

NIBBLE MODE CYCLE



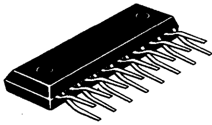
50ns/DIVISION

CURRENT WAVEFORM DURING POWER UP



50μs/DIVISION

MITSUBISHI ELECTRIC



M5M4256L-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

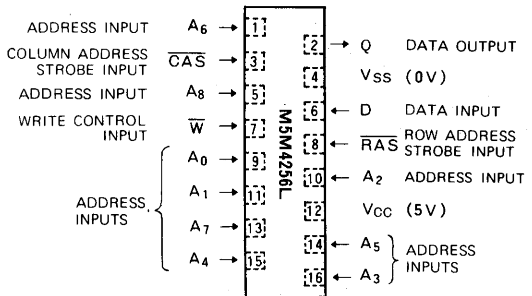
This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16 pin zigzag inline package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4256L-10	100	200	300
M5M4256L-12	120	230	260
M5M4256L-15	150	260	230

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256L-10 . . . . 385mW (max)
  - M5M4256L-12 . . . . 360mW (max)
  - M5M4256L-15 . . . . 330mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.

PIN CONFIGURATION (TOP VIEW)



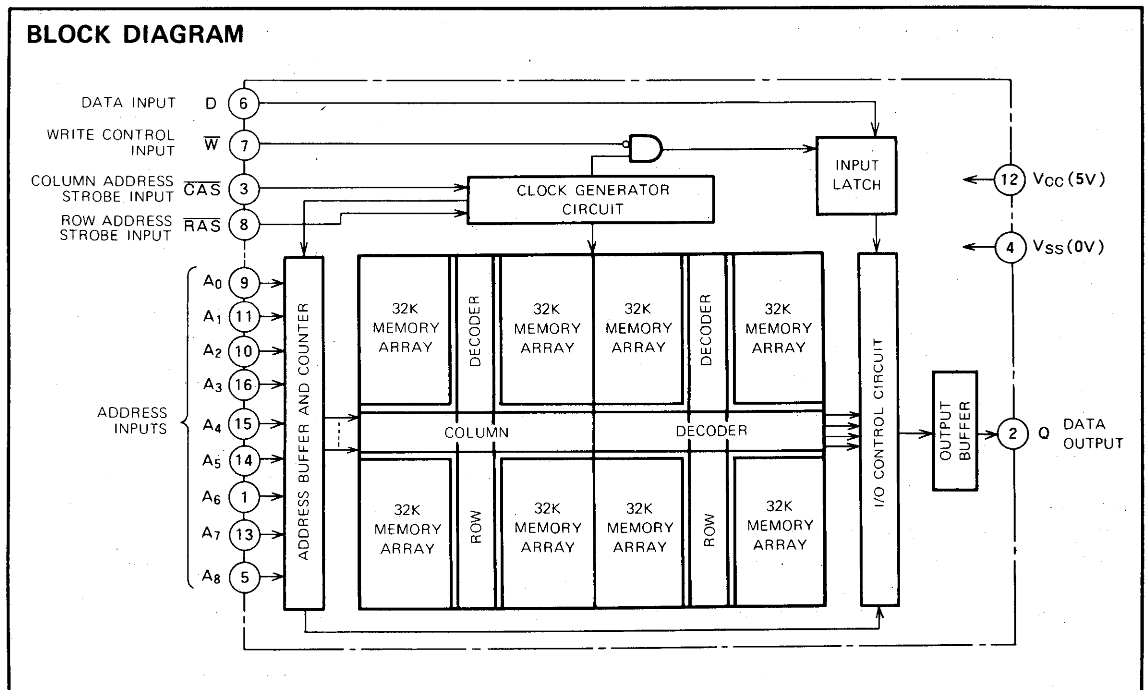
Outline 16P5A

- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 5 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



FUNCTION

The M5M4256L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
*: Page mode identical.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4256L the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4256L is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256L, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection
Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary
By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256L must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256L are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4256L is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4256L is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256L as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4256L operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1 ~ 7	V
V_I	Input voltage		−1 ~ 7	V
V_O	Output voltage		−1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4256L-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open			70	mA
		M5M4256L-12				65	
		M5M4256L-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} output open			4	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4256L-10	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} $t_{C(RAS)}$ = min, output open			60	mA
		M5M4256L-12				55	
		M5M4256L-15				50	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5M4256L-10	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{CPG} = min, output open			55	mA
		M5M4256L-12				50	
		M5M4256L-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4256L-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, output open			65	mA
		M5M4256L-12				60	
		M5M4256L-15				55	
$C_{I(A)}$	Input capacitance, address inputs		V_I = V_{SS} f = 1MHz V_i = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		V_O = V_{SS}, f = 1MHz, V_i = 25mVrms			7	pF

Note 2: Current flowing into an IC is positive ; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ns
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL}(t_{TLH}) + t_{su(CA-CAS)min}$.

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		20		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		0		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25		35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13: This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)max}$. Test conditions ; Load = 2TTL, C_L = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2TTL C_L = 100pF

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	235		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15: t_{CRW} min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}max + t_{d(CAS-W)}min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: t_{CRMW} min is defined as $t_{CRMW}\,min = t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	100		125		145		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		55		60		ns
t_{CPGRW}	Page-Mode read-write cycle time	t_{PCRW}	130		160		180		ns

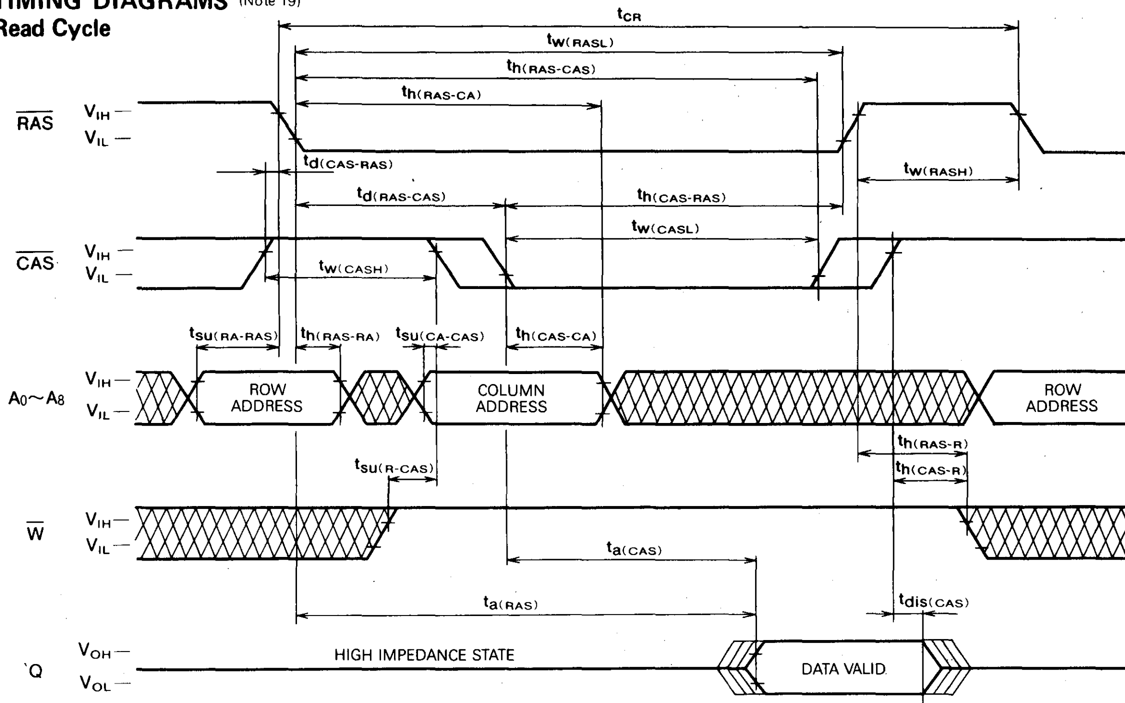
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256L-10		M5M4256L-12		M5M4256L-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

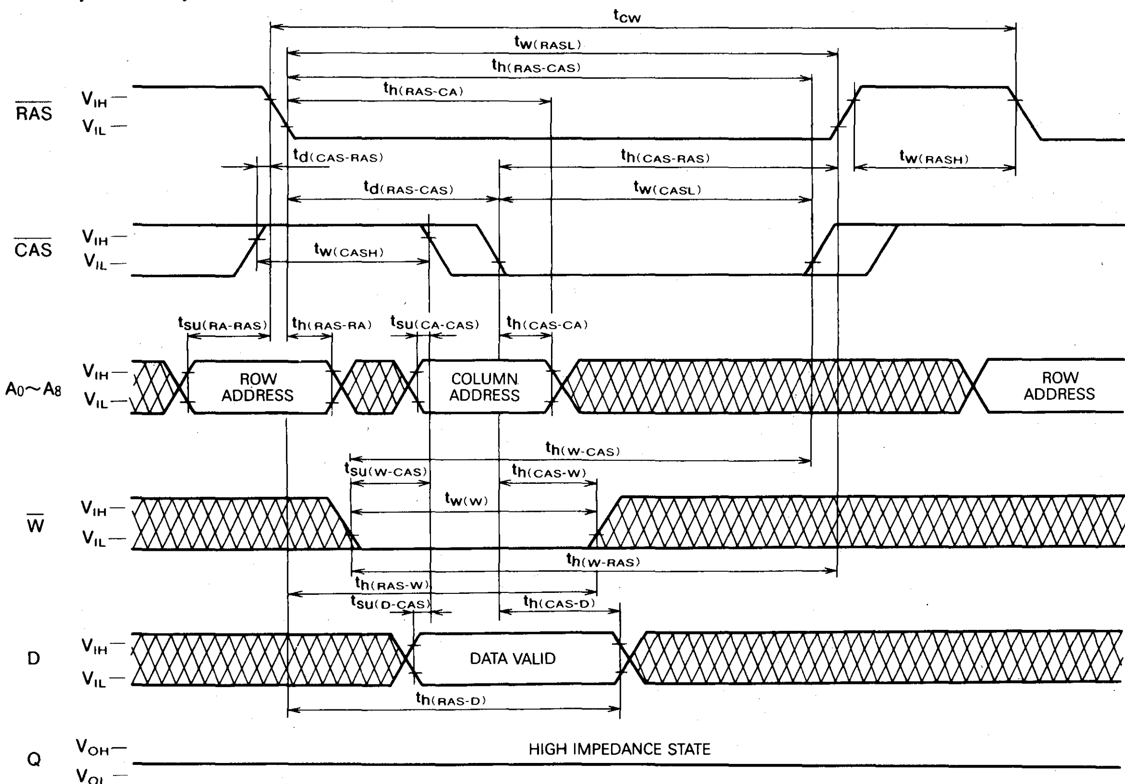
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 19)

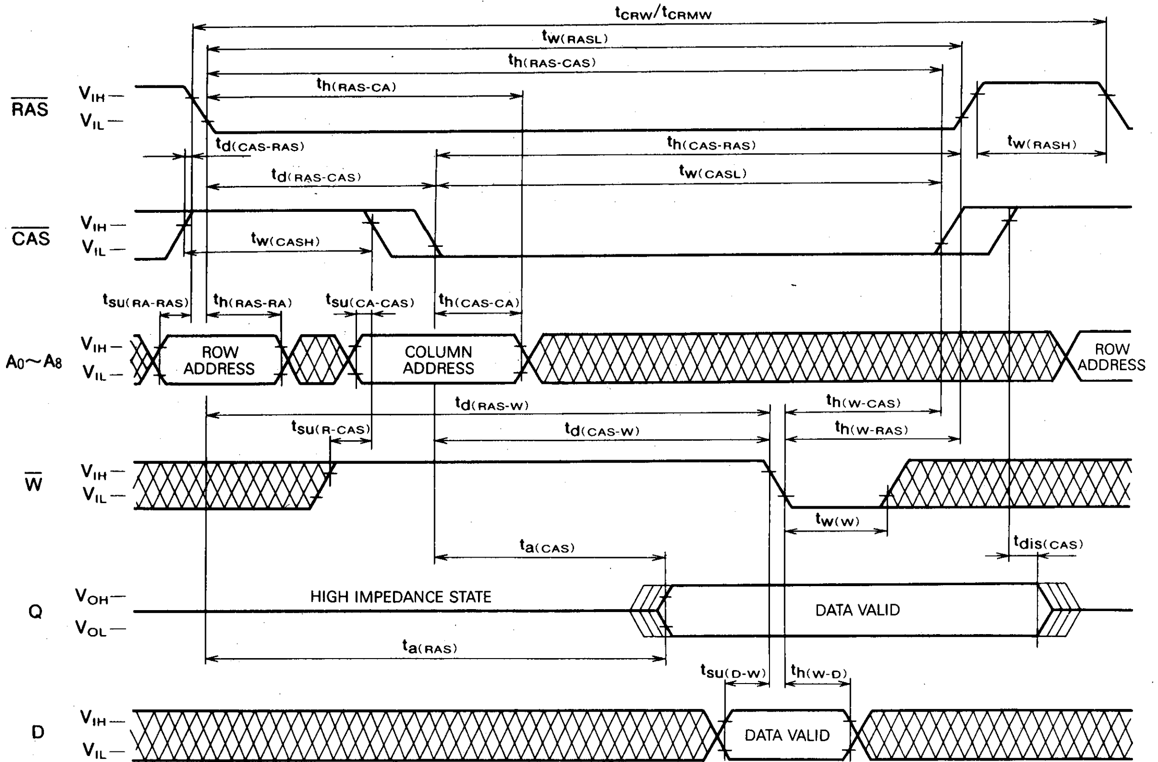
Read Cycle



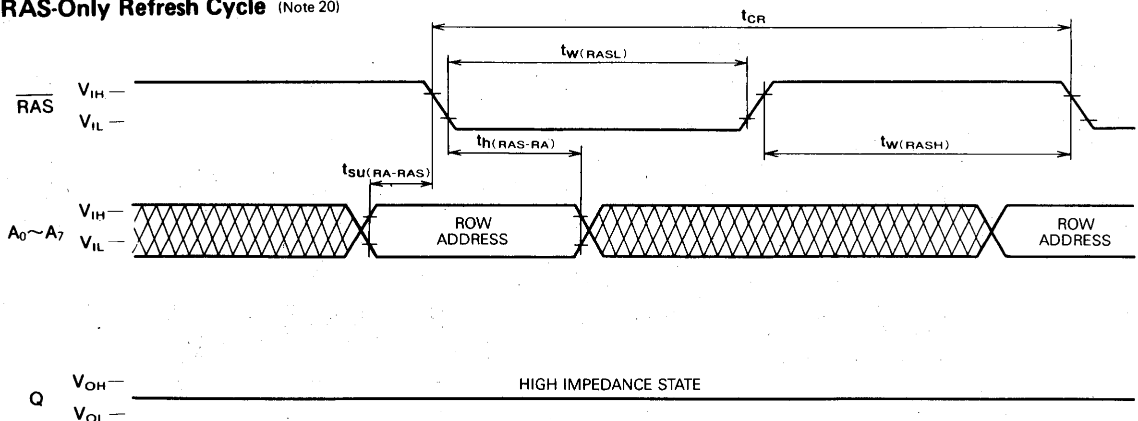
Write Cycle (Early Write)



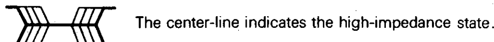
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)



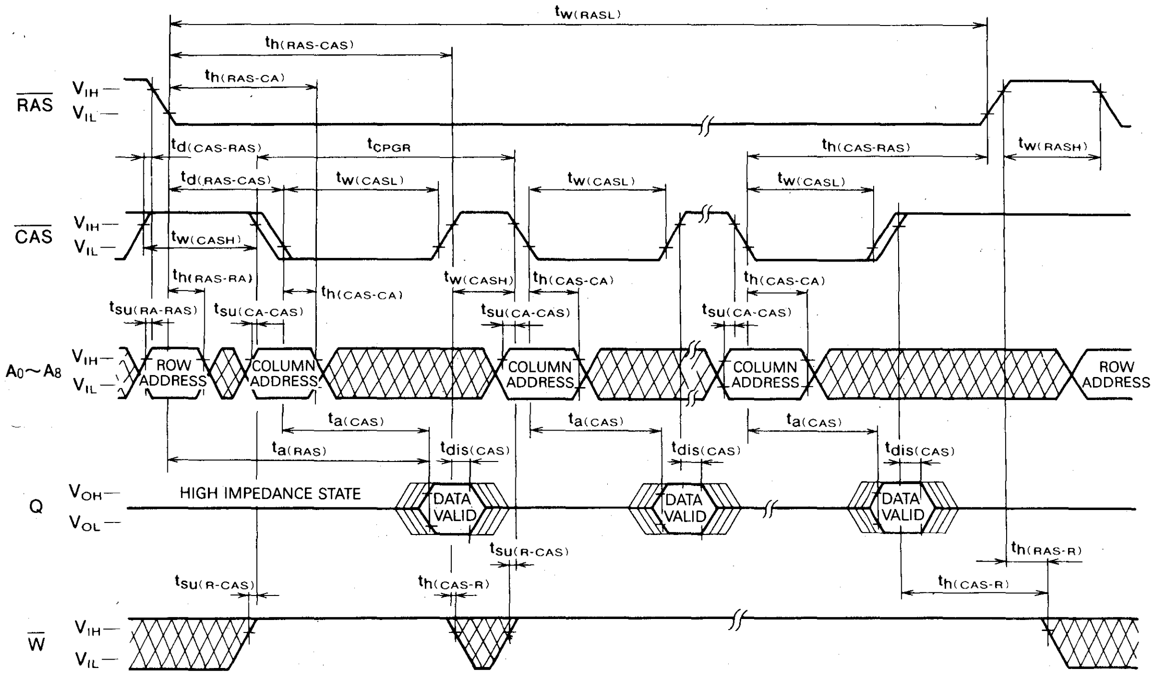
Note 19. Indicates the don't care input.

 The center-line indicates the high-impedance state.

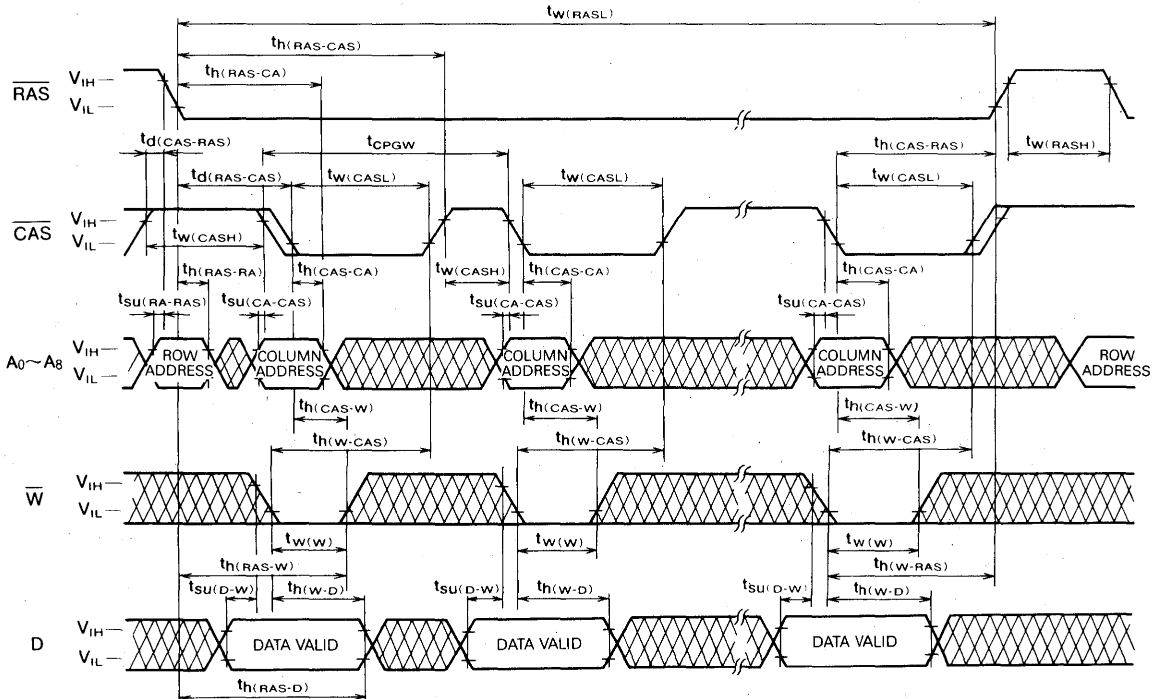
Note 20. $\overline{CAS}=V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

MITSUBISHI ELECTRIC

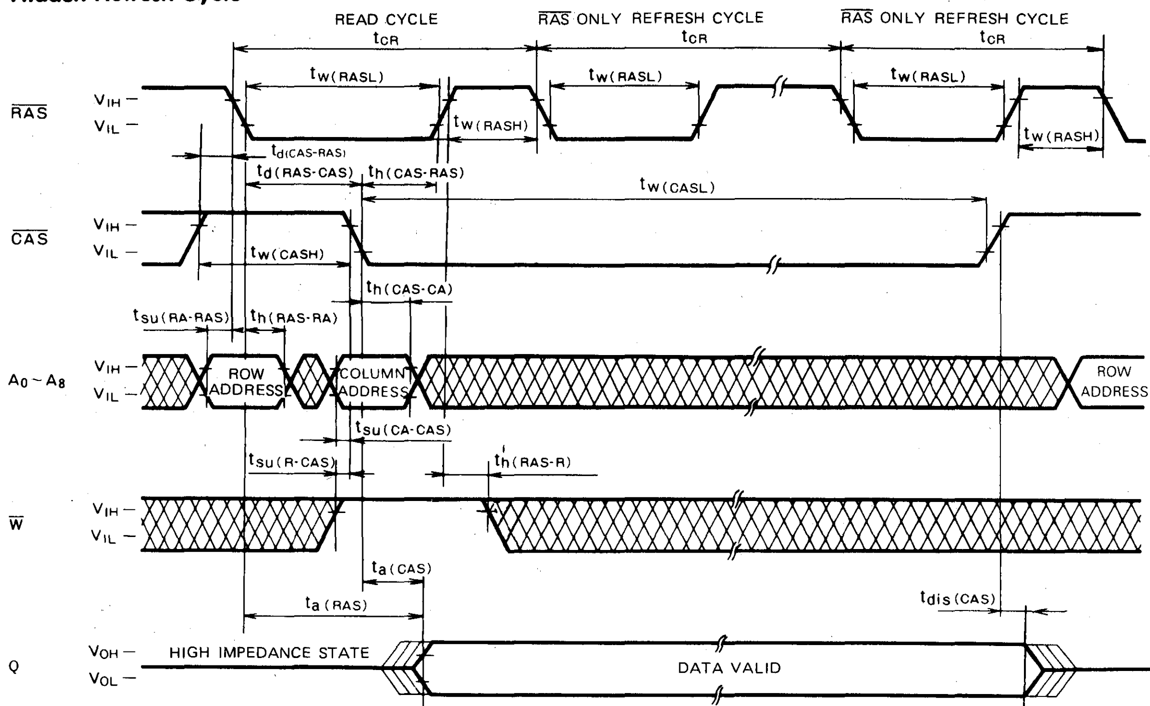
Page-Mode Read Cycle



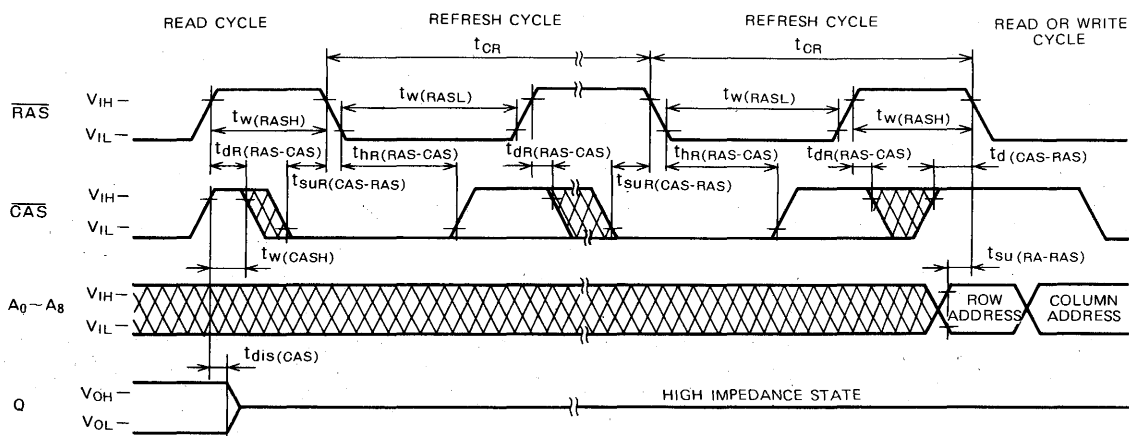
Page-Mode Write Cycle



Hidden Refresh Cycle



CAS before RAS Refresh Cycle (Note 21)

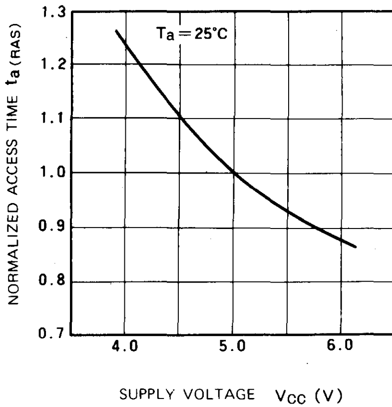


Note 21: W, D = don't care.

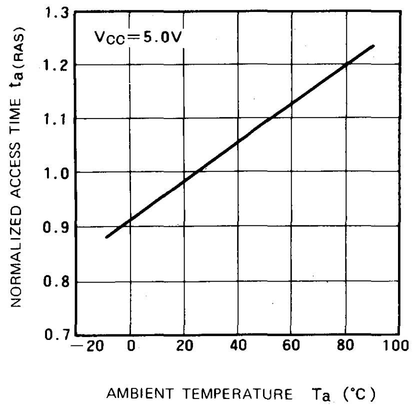
262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TYPICAL CHARACTERISTICS

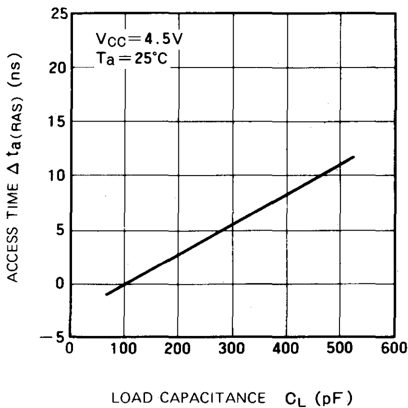
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



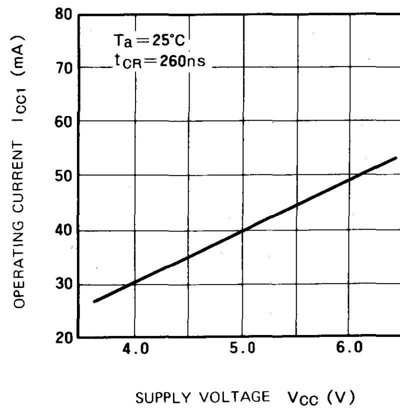
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



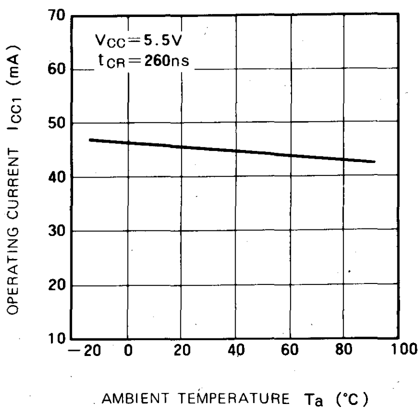
ACCESS TIME VS. LOAD CAPACITANCE



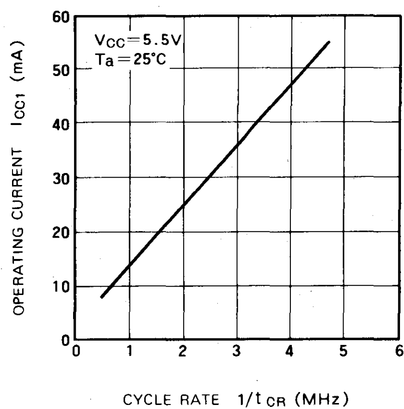
OPERATING CURRENT VS. SUPPLY VOLTAGE



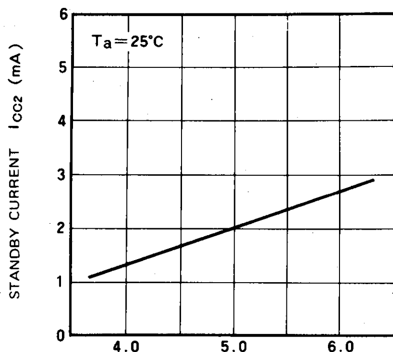
OPERATING CURRENT VS. AMBIENT TEMPERATURE

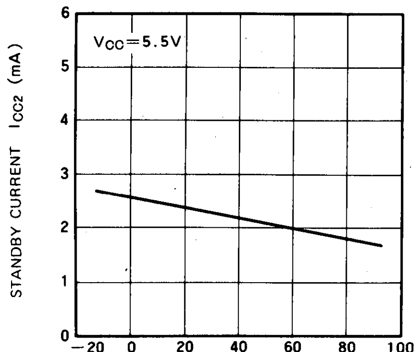


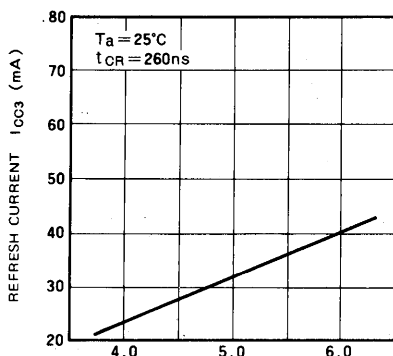
OPERATING CURRENT VS. CYCLE RATE

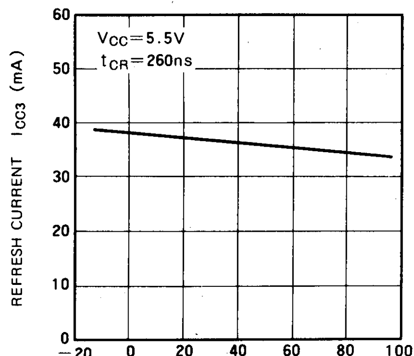


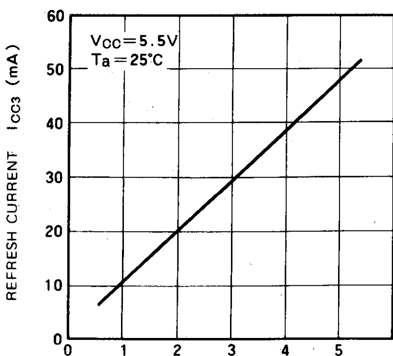
262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

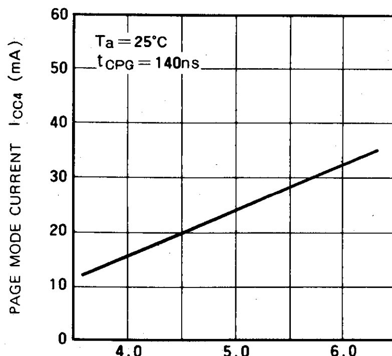




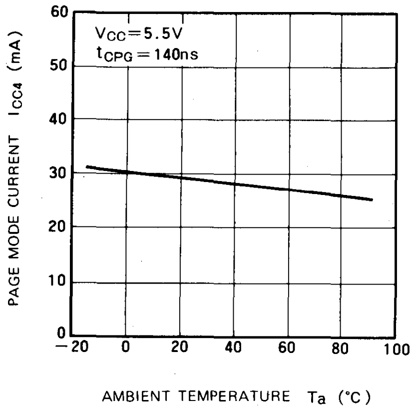


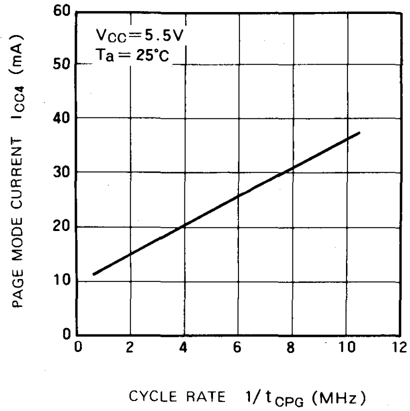


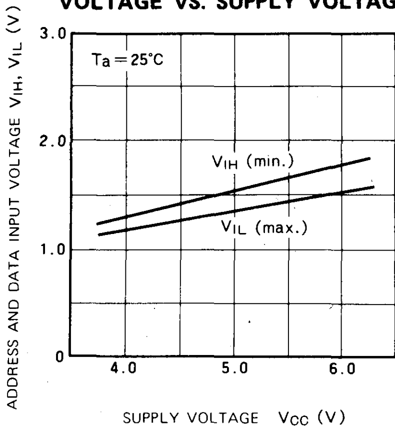


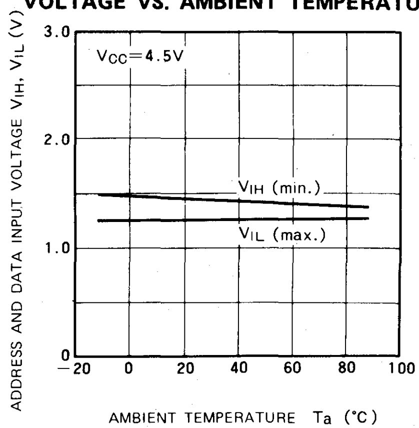


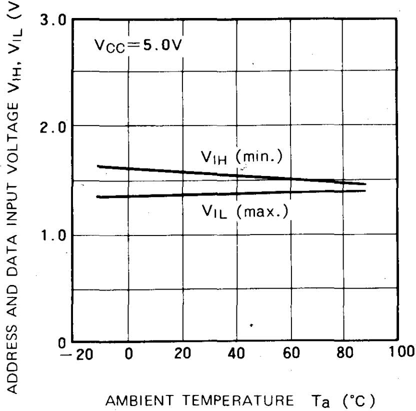
262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

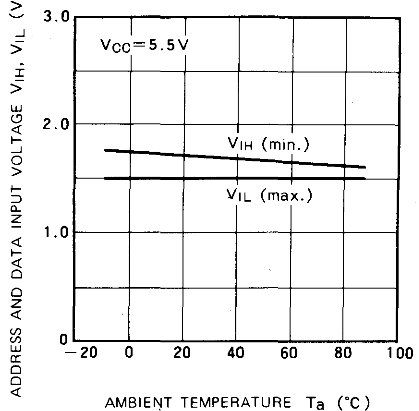


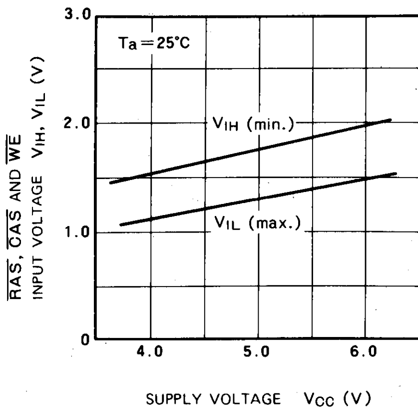


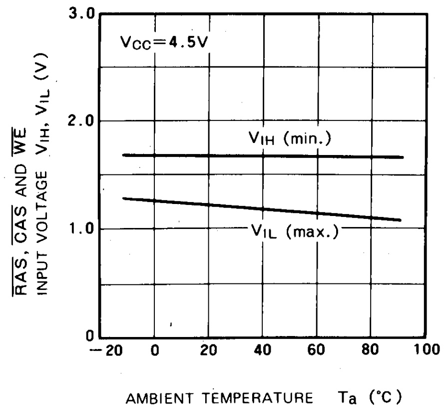


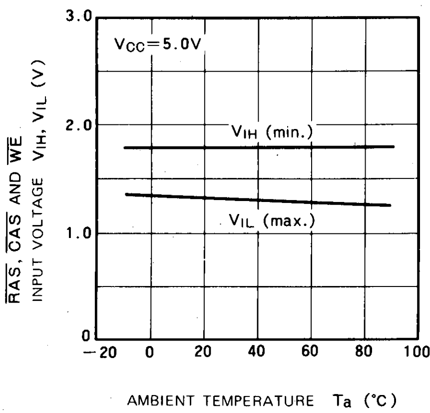


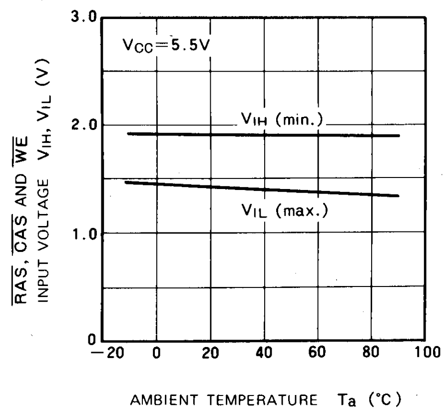




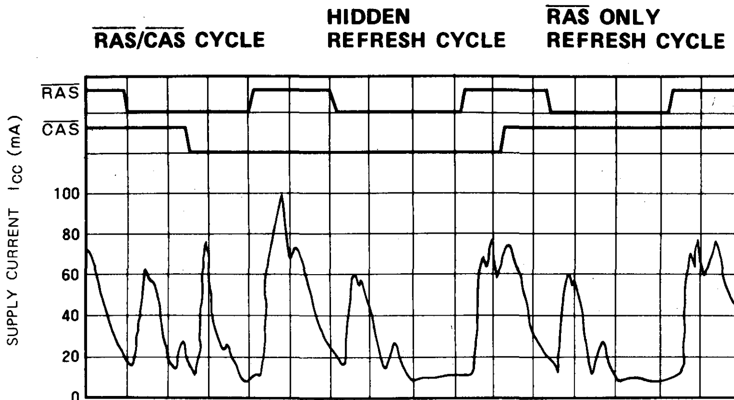

RAS, CAS AND WE INPUT
VOLTAGE VS. SUPPLY VOLTAGE
Ta=25°C
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
4.0
5.0
6.0
SUPPLY VOLTAGE Vcc (V)


RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
Vcc=4.5V
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)


RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
Vcc=5.0V
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)

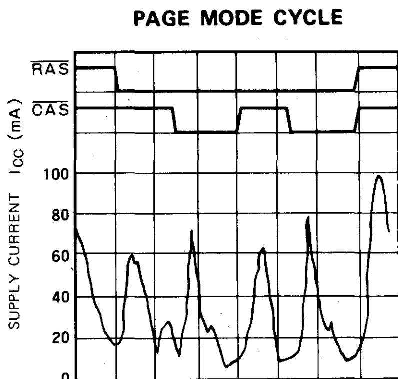

RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
Vcc=5.5V
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM



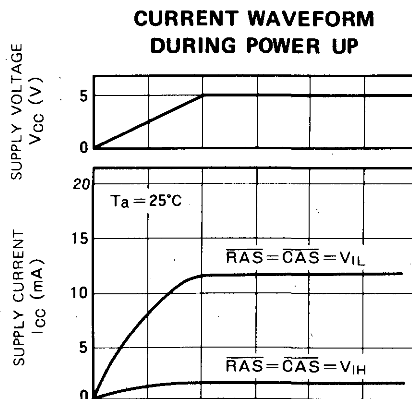
50ns/DIVISION

PAGE MODE CYCLE

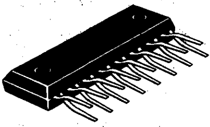


50ns/DIVISION

CURRENT WAVEFORM DURING POWER UP



50μs/DIVISION



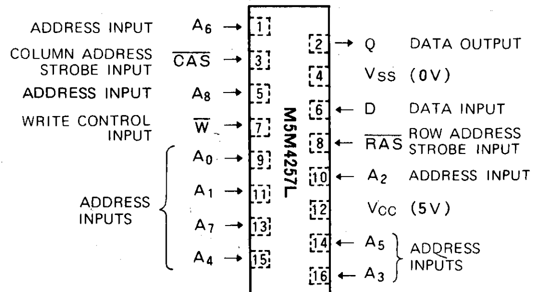
M5M4257L-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 16 pin zigzag inline package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

PIN CONFIGURATION (TOP VIEW)



Outline 16P5A

FEATURES

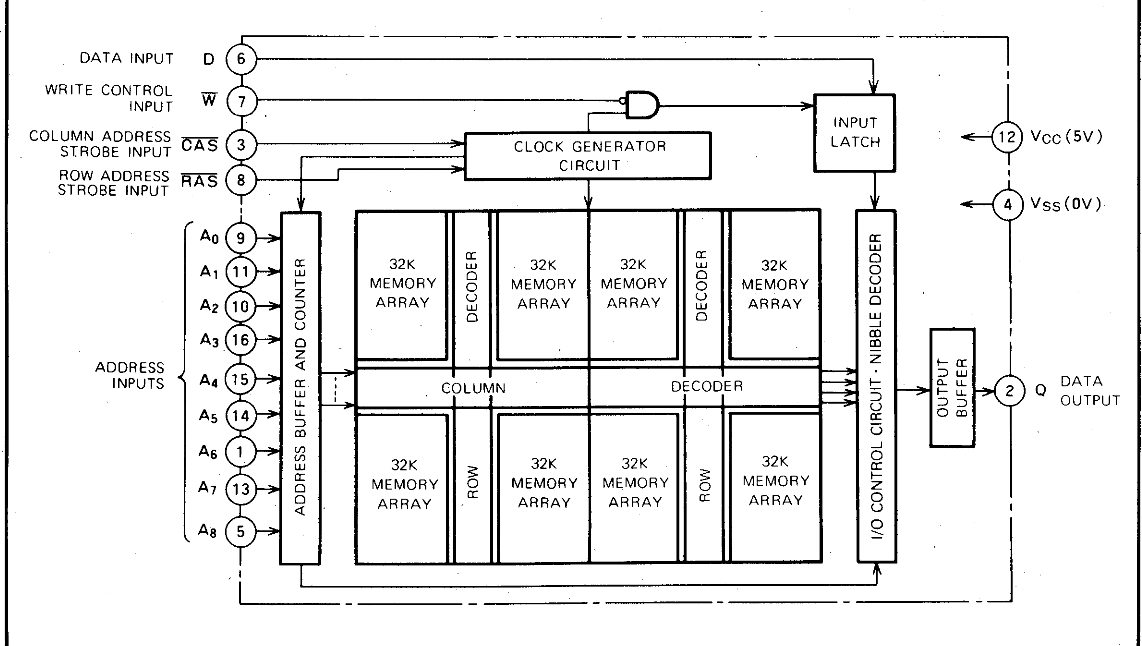
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4257L-10	100	200	200
M5M4257L-12	120	230	260
M5M4257L-15	150	260	230

- 16 pin zigzag inline package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257L-10 . . . . 385mW (max)
  - M5M4257L-12 . . . . 360mW (max)
  - M5M4257L-15 . . . . 330mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities. (Pin 1 is used for nibble mode)
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 5 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



FUNCTION

The M5M4257L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
* : Nibble mode identical and Nibble mode column address is DNC while togging $\overline{CAS}$.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4257L the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4257L is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257L, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, CAS is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that CAS and/or RAS can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding CAS, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, RAS must be applied to all devices.

Nibble-Mode Operation

The M5M4257L is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing CAS high then low (toggle) while RAS remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling CAS causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257L must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257L are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order (RAS) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. RAS Only Refresh

In this refresh method, the CAS clock should be at a V_{IH} level and the system must perform RAS Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the RAS clock and associated internal row locations are refreshed. A RAS Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. CAS before RAS Refresh

If CAS falls $t_{SUR(CAS-RAS)}$ earlier than RAS and if CAS is kept low by $t_{hR(RAS-CAS)}$ after RAS falls, CAS before RAS Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If CAS is kept low after the above operation, RAS cycle initiates RAS Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing RAS high and then low while CAS remains high initiates the normal RAS Only Refresh using the external address.

If CAS is kept low after the normal read/write cycle, RAS cycle initiates the RAS Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit CAS is brought high.

4. Hidden Refresh

A feature of the M5M4257L is that refresh cycles may be performed while maintaining valid data at the output pin by extending the CAS active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period, executing a RAS-only cycling, but with CAS held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the CAS asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4257L is dynamic, and most of the power is dissipated when addresses are strobed. Both RAS and CAS are decoded and applied to the M5M4257L as chip-select in the memory system, but if RAS is decoded, all unselected devices go into stand-by independent of the CAS condition, minimizing system power dissipation.

Power Supplies

The M5M4257L operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1〜7	V
V_I	Input voltage		−1〜7	V
V_O	Output voltage		−1〜7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	1000	mW
T_{opr}	Operating temperature		0〜70	°C
T_{stg}	Storage temperature		−65〜150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0〜70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0〜70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4257L-10	$\overline{RAS}$, $\overline{CAS}$ cycling t_{CR} = t_{CW} = min. output open			70	mA
		M5M4257L-12				65	
		M5M4257L-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4257L-10	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} $t_{C(RAS)}$ = min, output open			60	mA
		M5M4257L-12				55	
		M5M4257L-15				50	
$I_{CC5(AV)}$	Average supply current from V_{CC} nibble mode	M5M4257L-10	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{CN} = min, output open			35	mA
		M5M4257L-12				30	
		M5M4257L-15				25	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4257L-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, output open			65	mA
		M5M4257L-12				60	
		M5M4257L-15				55	
$C_{I(A)}$	Input capacitance, address inputs		V_I = V_{SS} f = 1MHz V_i = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		V_O = V_{SS}, f = 1MHz, V_i = 25mVrms			7	pF

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ns
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.

6. The switching characteristics are defined at $t_{THL} = t_{TLH} = 5ns$.

7. Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.

8. Except for page-mode.

9. $t_{d(CAS-RAS)}$ requirement is only applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\min = t_{h(RAS-RA)}\min + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)}\min$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.

12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.

13. This is the vauel when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.

14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		25		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	225		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15. t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-CAS)} + t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data outputs keep the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min. and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Nibble-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
t_{CN}	Nibble mode cycle time	t_{NC}	50		55		70		ns
$t_{aN(CAS)}$	Nibble mode access time	t_{NAC}		25	3	30		40	ns
$t_{wN(CASL)}$	Nibble mode $\overline{CAS}$ low pulse width	t_{NCAS}	25		30		40		ns
$t_{wN(CASH)}$	Nibble mode precharge time	t_{NP}	15		15		20		ns
$t_{hN(CAS-RAS)}$	Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25		30		40		ns
$t_{dN(CAS-W)}$	Nibble mode $\overline{CAS}$ to WRITE delay	t_{NCWD}	25		30		20		ns
$t_{wNRMW(CASL)}$	Nibble mode RMW $\overline{CAS}$ pulse width	t_{NCRW}	55		65		40		ns
$t_{hNRMW(W-CAS)}$	Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		30		40		ns
$t_{suN(W-CAS)}$	Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$	t_{NWCS}	0		0		80		ns
$t_{hN(CAS-RAS)}$	Nibble mode RMW $\overline{RAS}$ hold time		55						ns

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257L-10		M5M4257L-12		M5M4257L-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

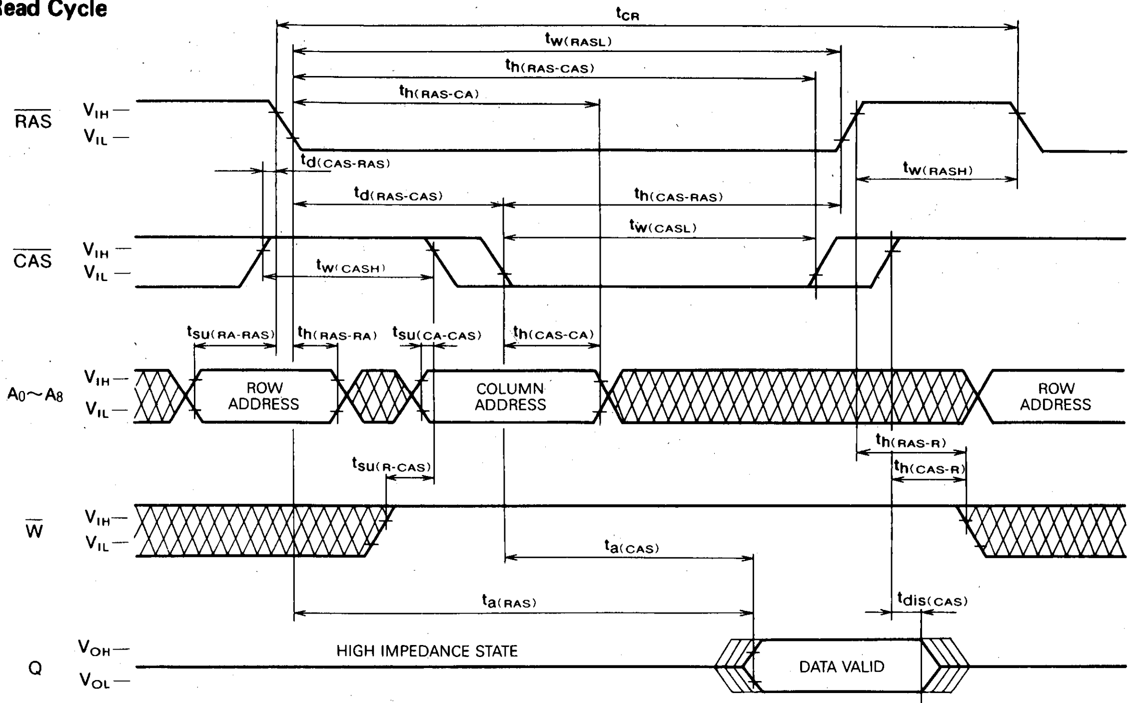
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Nibble Mode Addressing Sequence Example

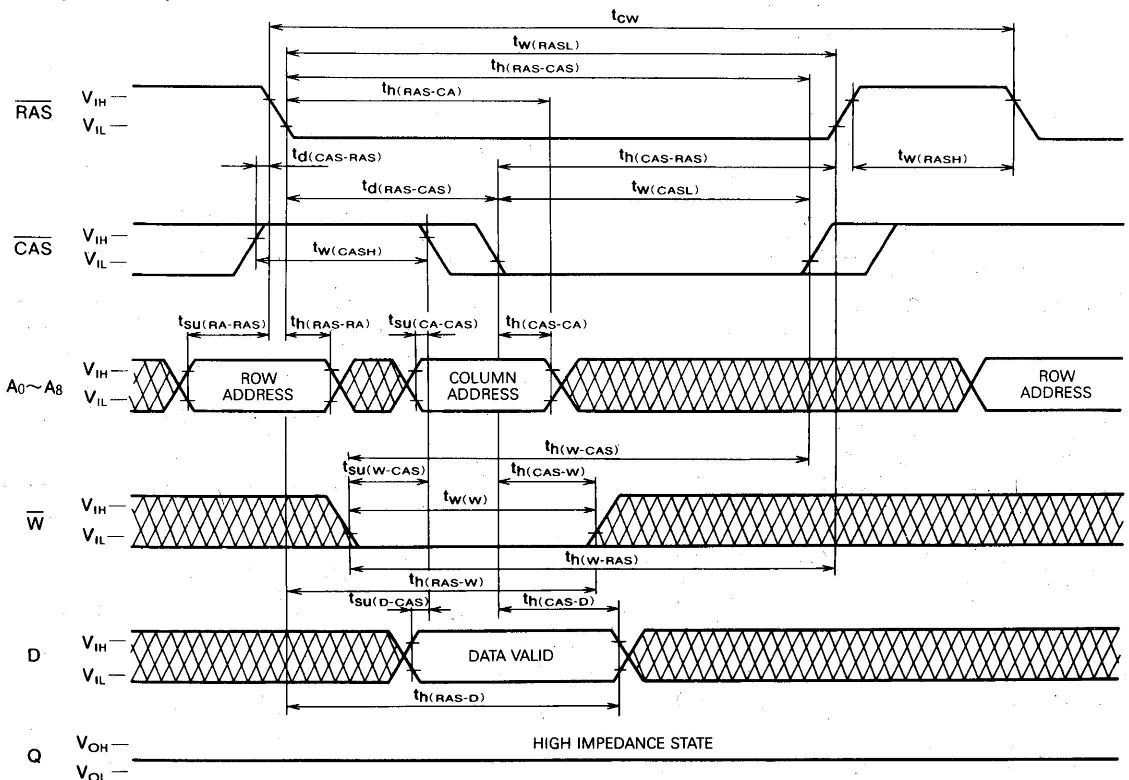
Sequence	Nibble bit	Column address									Row address									
		A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	External address
toggle $\overline{CAS}$	2	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	1	Internally generated address
toggle $\overline{CAS}$	3	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	
toggle $\overline{CAS}$	4	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	1	
toggle $\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	

TIMING DIAGRAMS (Note 19)

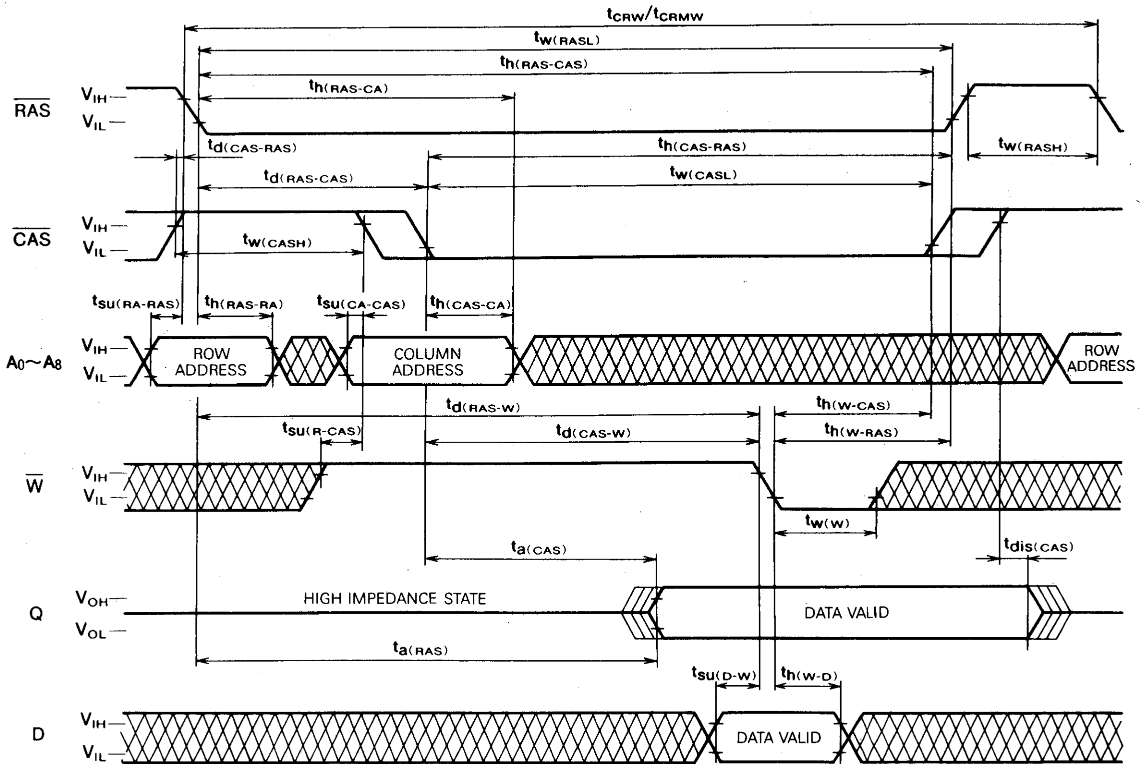
Read Cycle



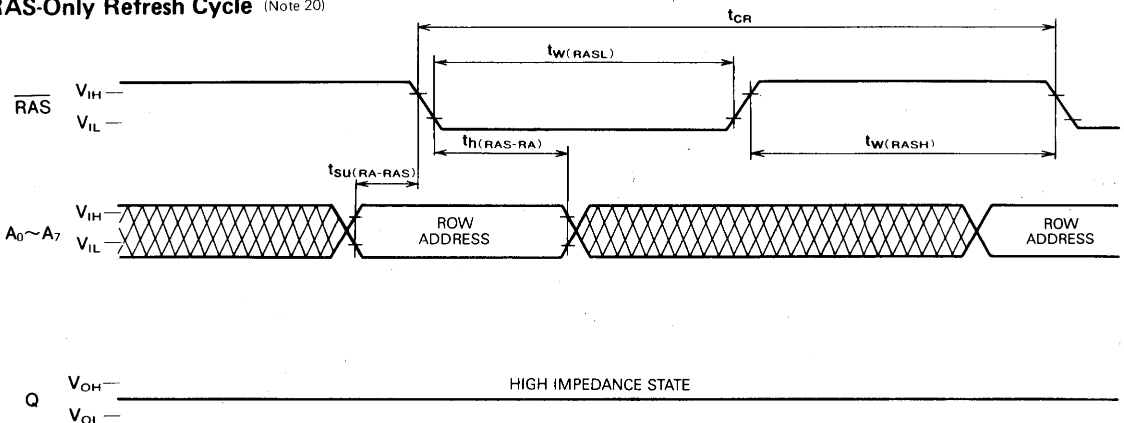
Write Cycle (Early Write)



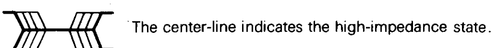
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

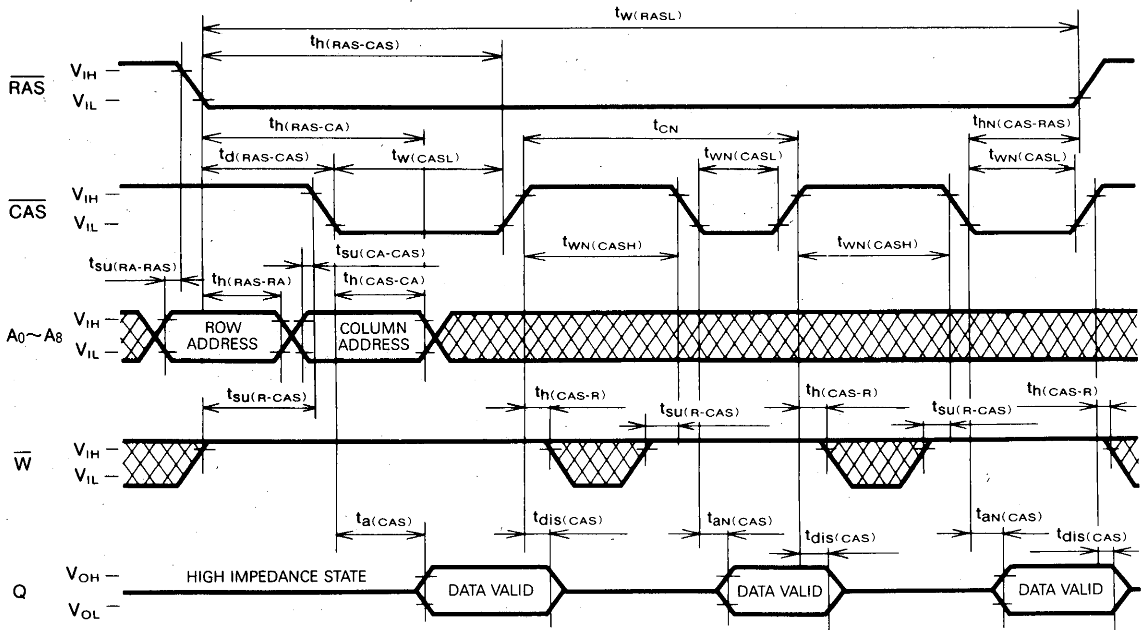


Note 19. Indicates the don't care input.

 The center-line indicates the high-impedance state.

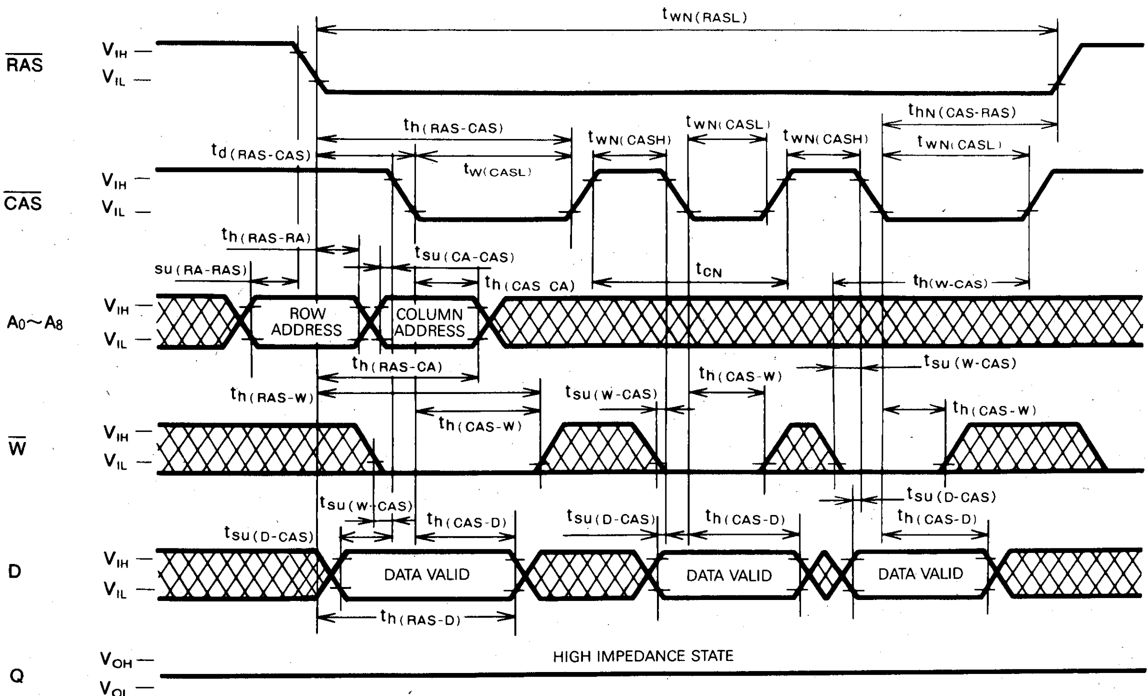
Note 20. $\overline{CAS}=V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

Nibble Mode Read Cycle (Note 21)

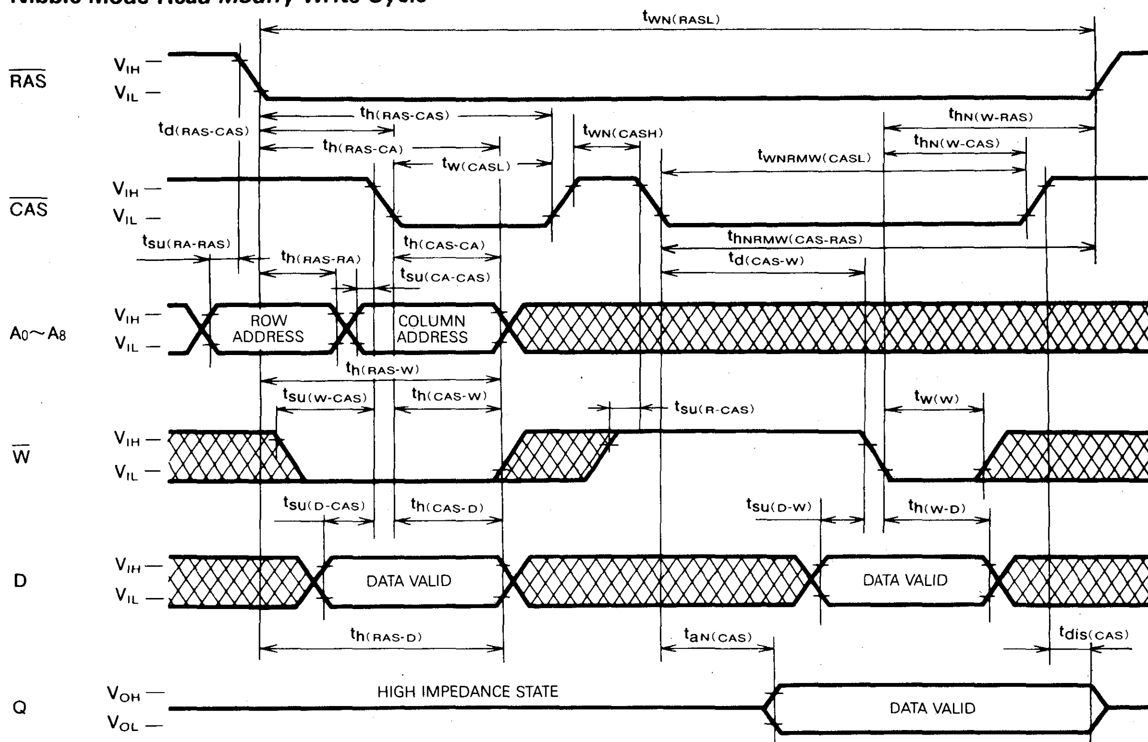


Note 21: Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

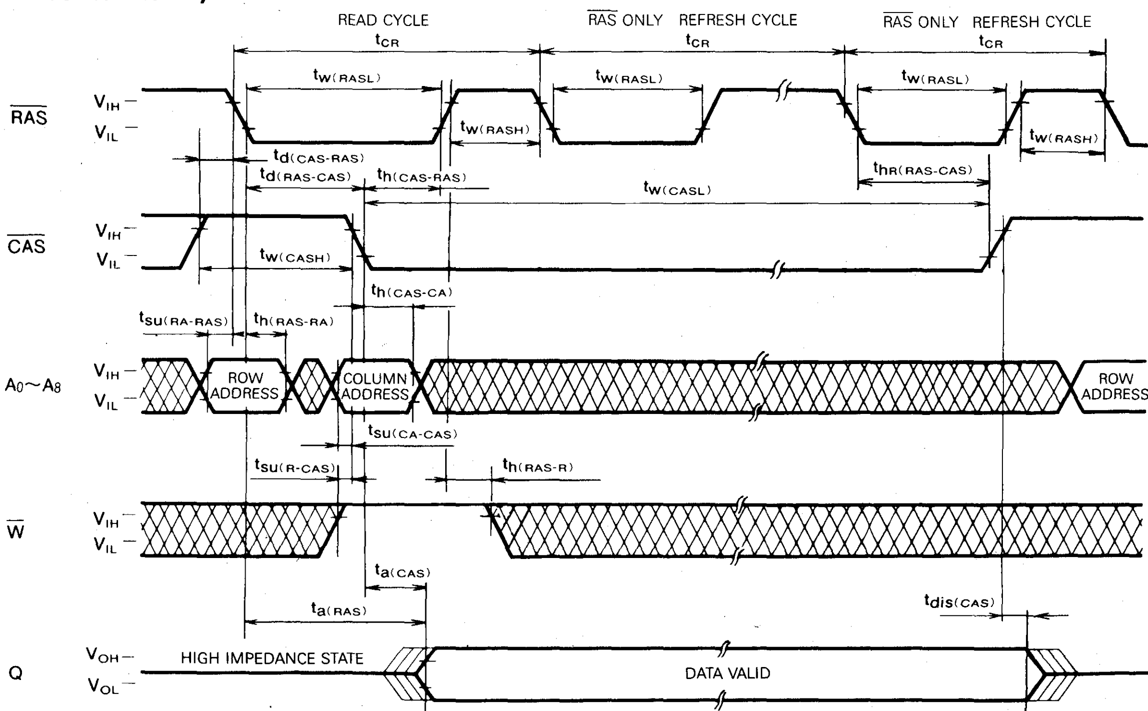
Nibble Mode Write Cycle (Early Write)



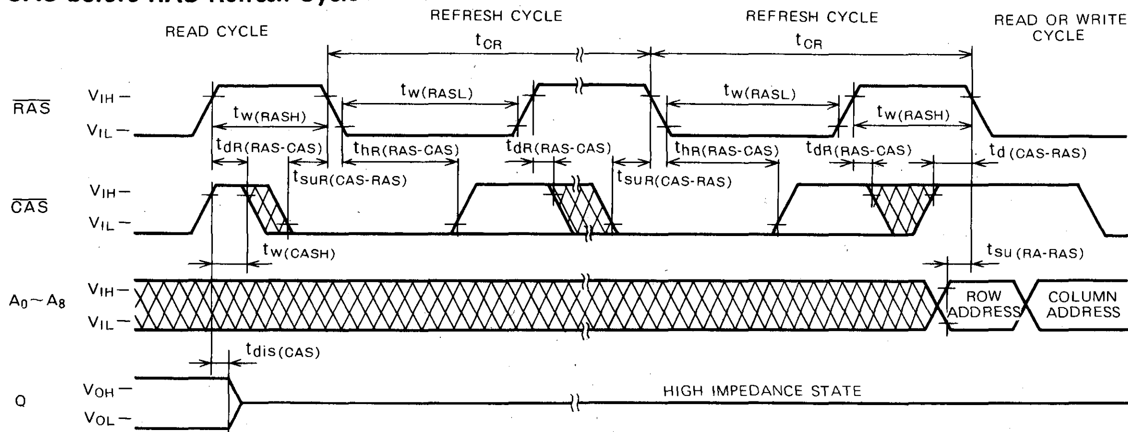
Nibble Mode Read-Modify-Write Cycle



Hidden Refresh Cycle



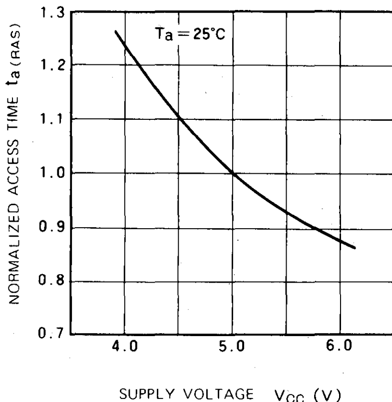
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)



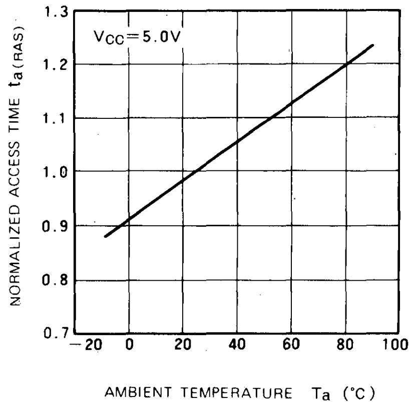
Note 22: $\overline{W}$, D = don't care.

TYPICAL CHARACTERISTICS

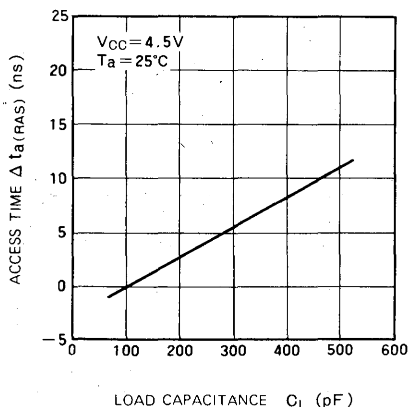
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



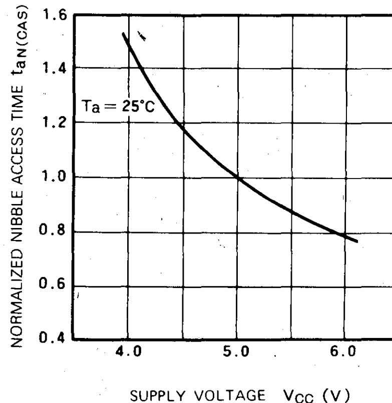
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE

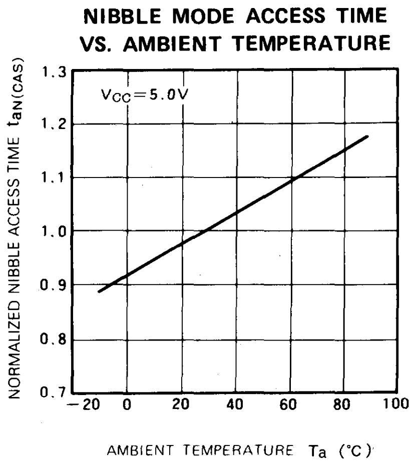


NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE

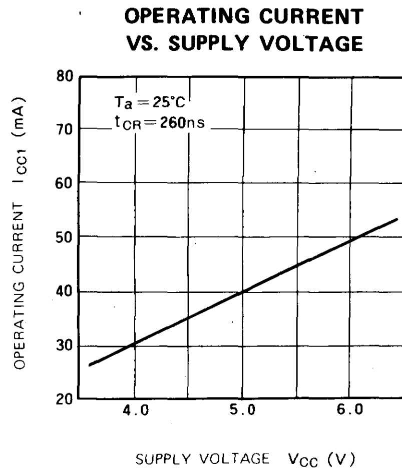


262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

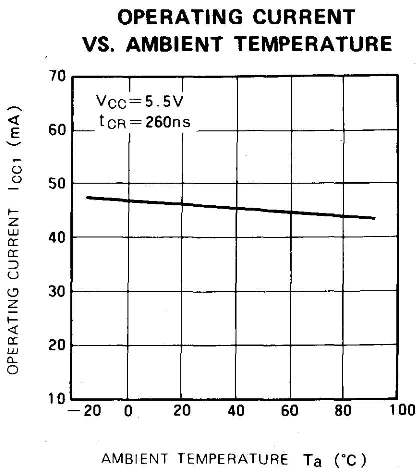
NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



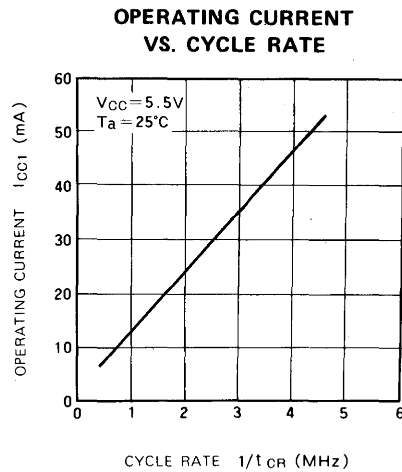
OPERATING CURRENT VS. SUPPLY VOLTAGE



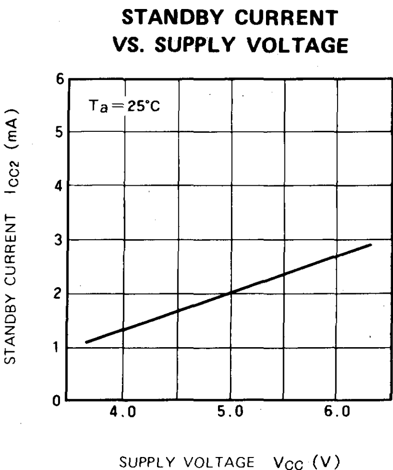
OPERATING CURRENT VS. AMBIENT TEMPERATURE



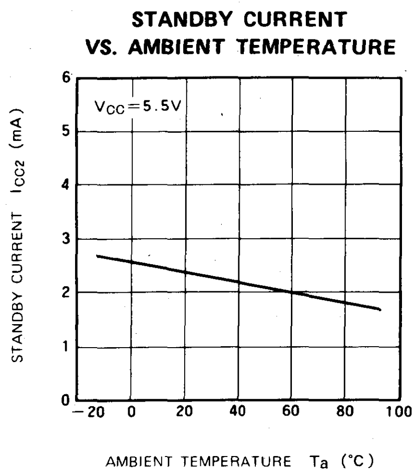
OPERATING CURRENT VS. CYCLE RATE



STANDBY CURRENT VS. SUPPLY VOLTAGE

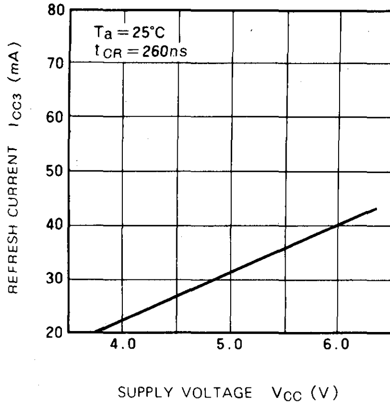


STANDBY CURRENT VS. AMBIENT TEMPERATURE

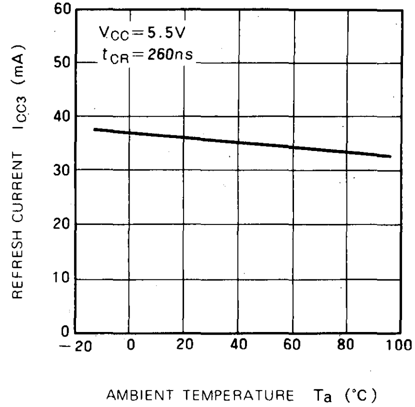


262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

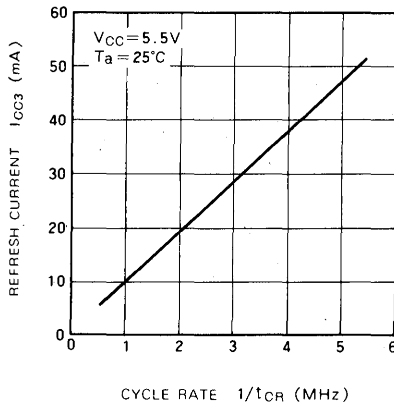
REFRESH CURRENT VS. SUPPLY VOLTAGE



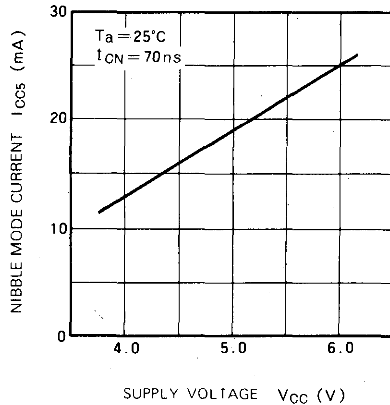
REFRESH CURRENT VS. AMBIENT TEMPERATURE



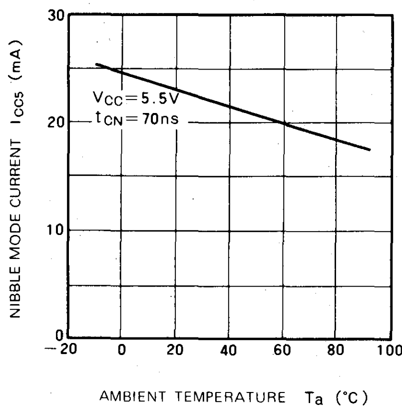
REFRESH CURRENT VS. CYCLE RATE



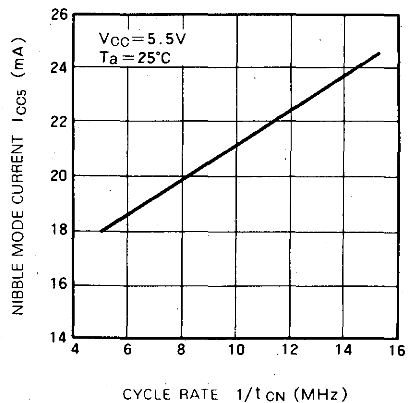
NIBBLE MODE CURRENT VS. SUPPLY VOLTAGE



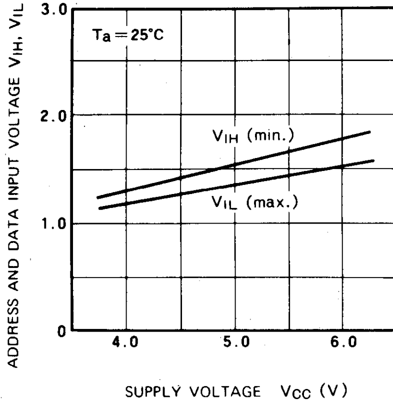
NIBBLE MODE CURRENT VS. AMBIENT TEMPERATURE



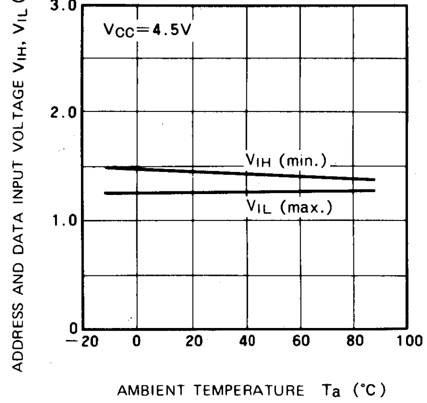
NIBBLE MODE CURRENT VS. CYCLE RATE



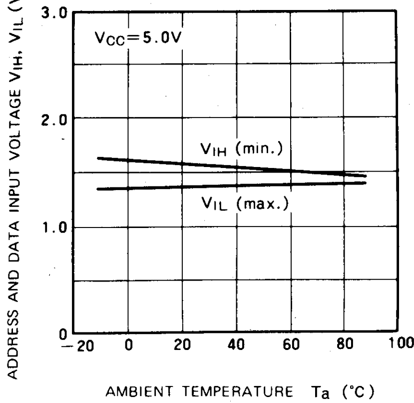
ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



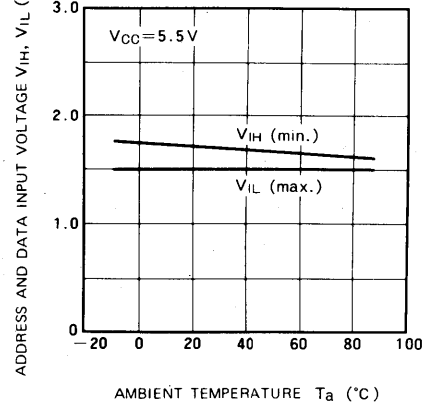
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



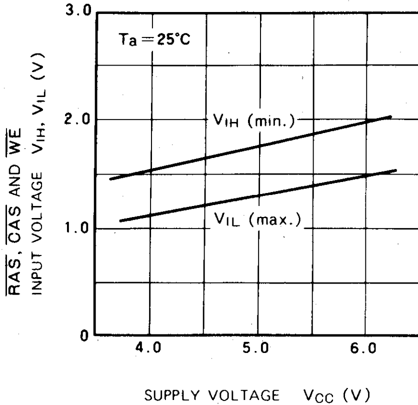
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



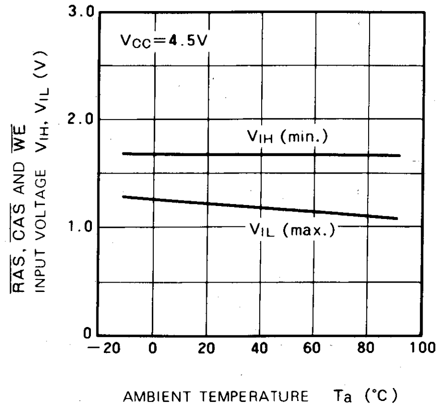
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE

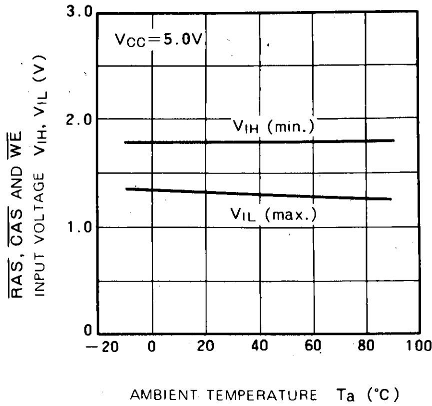


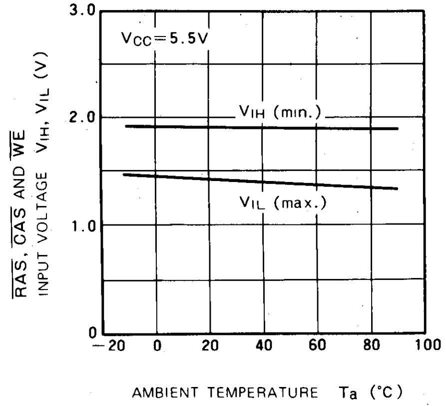
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE

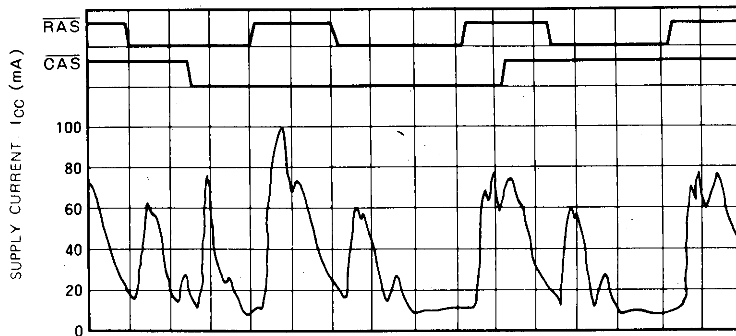


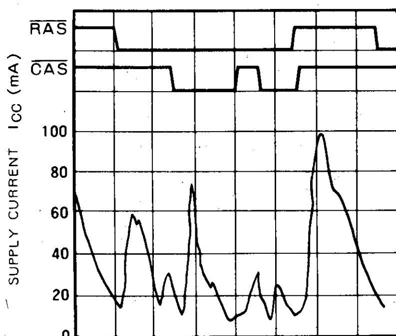
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

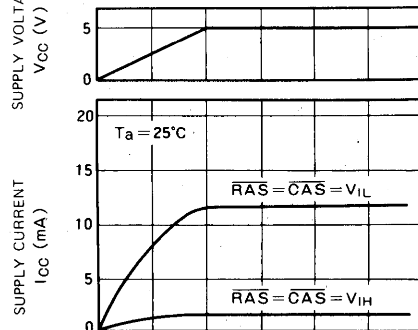


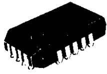

RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC=5.0V
VIH (min.)
VIL (max.)
RAS, CAS AND WE
INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)


RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC=5.5V
VIH (min.)
VIL (max.)
RAS, CAS AND WE
INPUT VOLTAGE VIH, VIL (V)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
AMBIENT TEMPERATURE Ta (°C)


RAS/CAS CYCLE
HIDDEN
REFRESH CYCLE
RAS ONLY
REFRESH CYCLE
RAS
CAS
SUPPLY CURRENT ICC (mA)
100
80
60
40
20
0
50ns/DIVISION


NIBBLE MODE CYCLE
RAS
CAS
SUPPLY CURRENT ICC (mA)
100
80
60
40
20
0
50ns/DIVISION


CURRENT WAVEFORM
DURING POWER UP
SUPPLY VOLTAGE VCC (V)
5
0
20
15
10
5
0
Ta=25°C
RAS=CAS=VIL
RAS=CAS=VIH
SUPPLY CURRENT ICC (mA)
50μs/DIVISION



M5M4256J-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

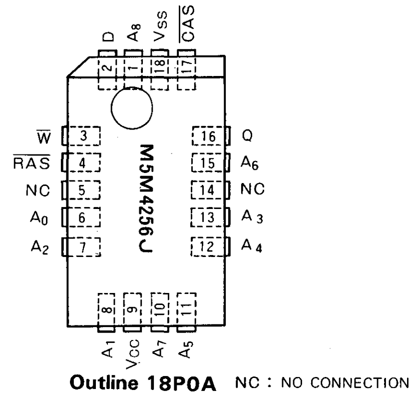
This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 18-pin plastic leaded chip carrier configuration and an increase in system densities. In addition to the RAS only refresh mode, the Hidden refresh mode and CAS before RAS refresh mode are available.

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4256J-10	100	200	300
M5M4256J-12	120	230	260
M5M4256J-15	150	260	230

- 18-pin plastic leaded chip carrier
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256J-10 .... 385mW (max)
  - M5M4256J-12 .... 360mW (max)
  - M5M4256J-15 .... 330mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.

PIN CONFIGURATION (TOP VIEW)



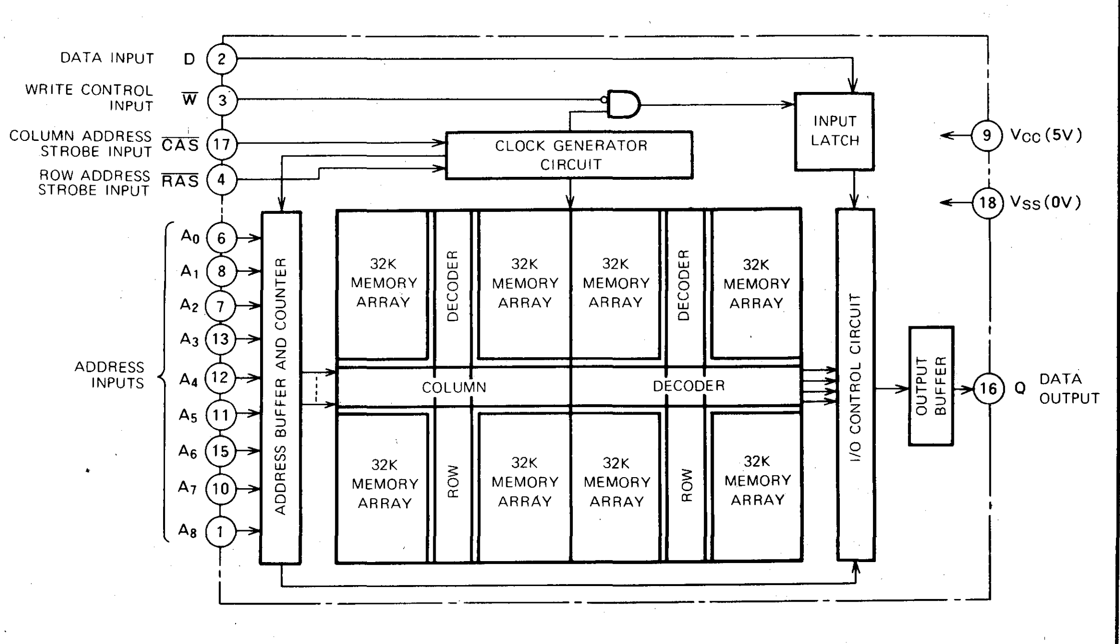
Outline 18P0A NC : NO CONNECTION

- Early-write operation gives common I/O capability
- Read-modify-write, RAS-only-refresh, Page-mode capabilities
- CAS before RAS refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms
- CAS controlled output allows hidden refresh
- Output data can be held infinitely by CAS.

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



FUNCTION

The M5M4256J provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4256J the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4256J is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256J which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256J must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256J are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4256J is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4256J is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256J as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4256J operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1 ~ 7	V
V_I	Input voltage		−1 ~ 7	V
V_O	Output voltage		−1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4256J-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min. output open			70	mA
		M5M4256J-12				65	
		M5M4256J-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = \overline{CAS} = V_{IH}$ output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4256J-10	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(RAS)}$ = min. output open			60	mA
		M5M4256J-12				55	
		M5M4256J-15				50	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5M4256J-10	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{CPG} = min. output open			55	mA
		M5M4256J-12				50	
		M5M4256J-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4256J-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, Output open			65	mA
		M5M4256J-12				60	
		M5M4256J-15				55	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_i = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_i = 25mVrms			7	pF

Note 2. Current flowing into an IC is positive ; out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ns
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined at $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\,min}$ and $V_{IL\,max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\,min = t_{h(RAS-RA)}\,min + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)}\,min$.

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	225		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15. t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-CAS)}$ max $+ t_{d(CAS-W)}$ min $+ t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	100		125		145		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		55		60		ns
t_{CPGRW}	Page-mode read-write cycle time	t_{PCRW}	140		160		180		ns

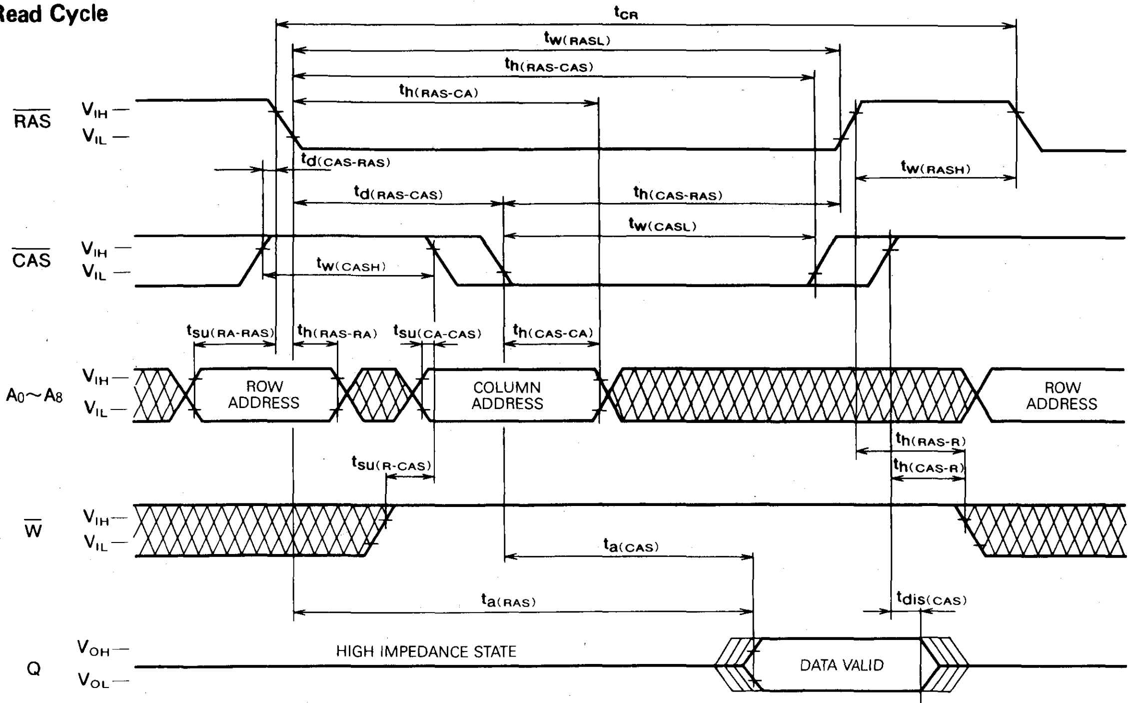
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256J-10		M5M4256J-12		M5M4256J-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

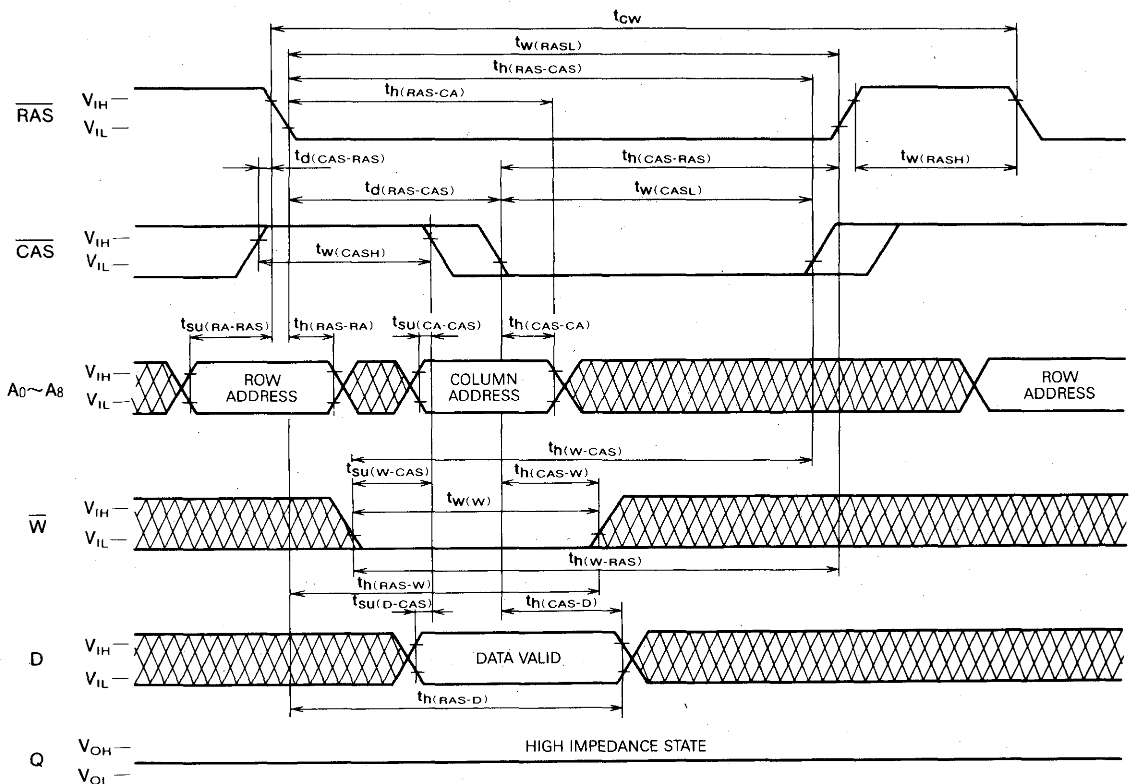
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 19)

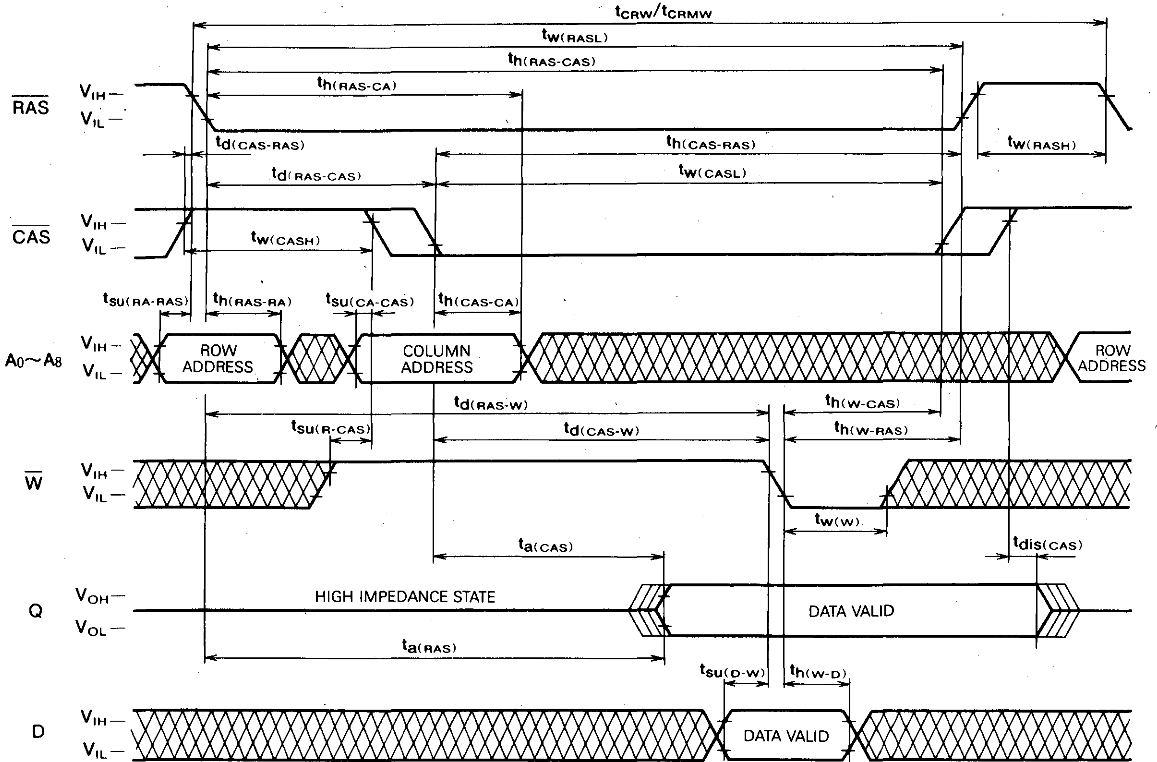
Read Cycle



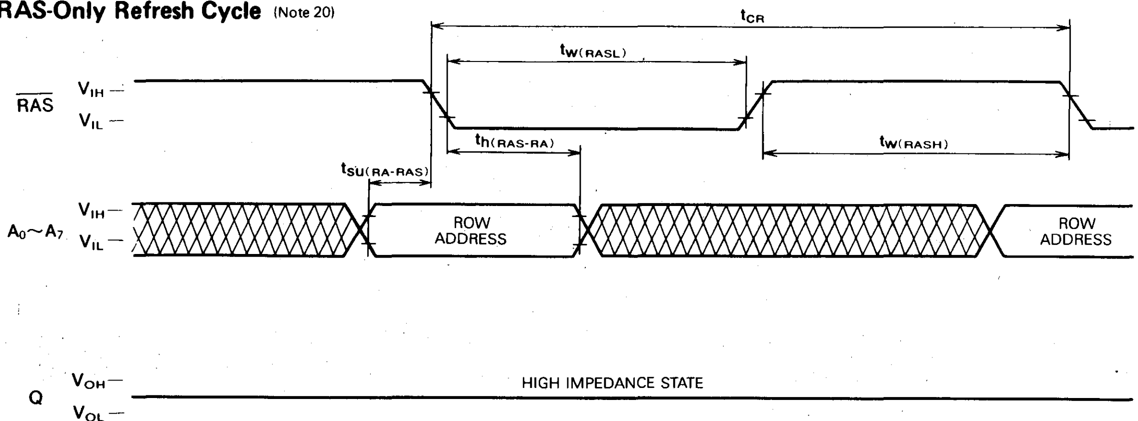
Write Cycle (Early Write)

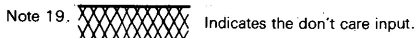


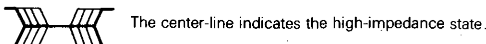
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

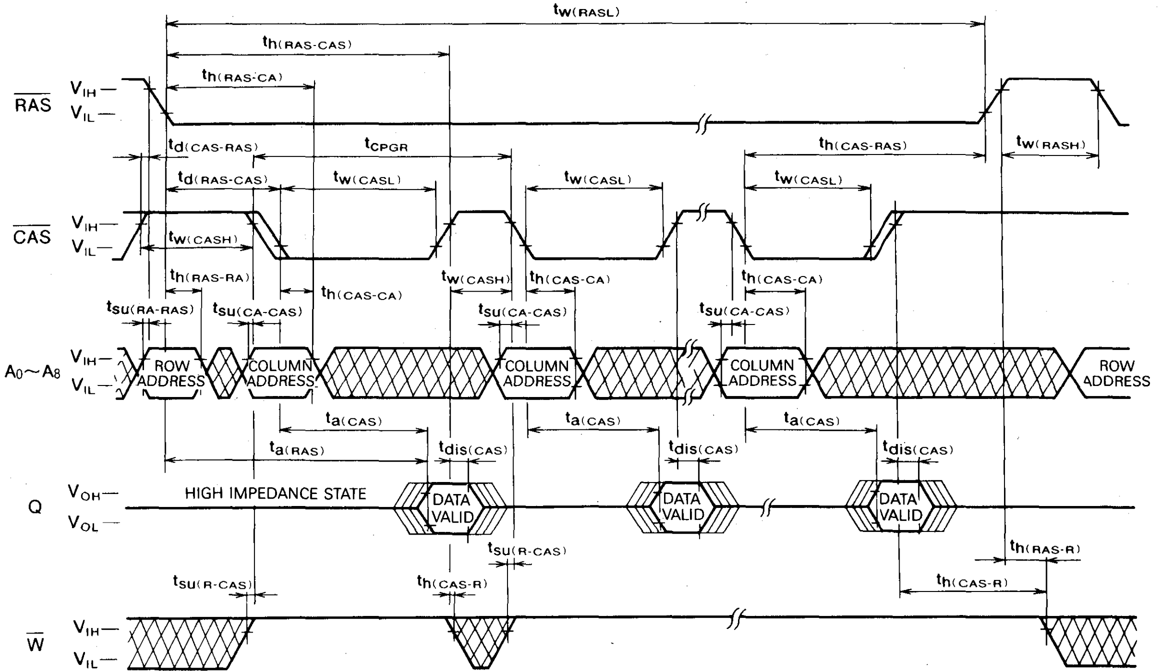


Note 19.  Indicates the don't care input.

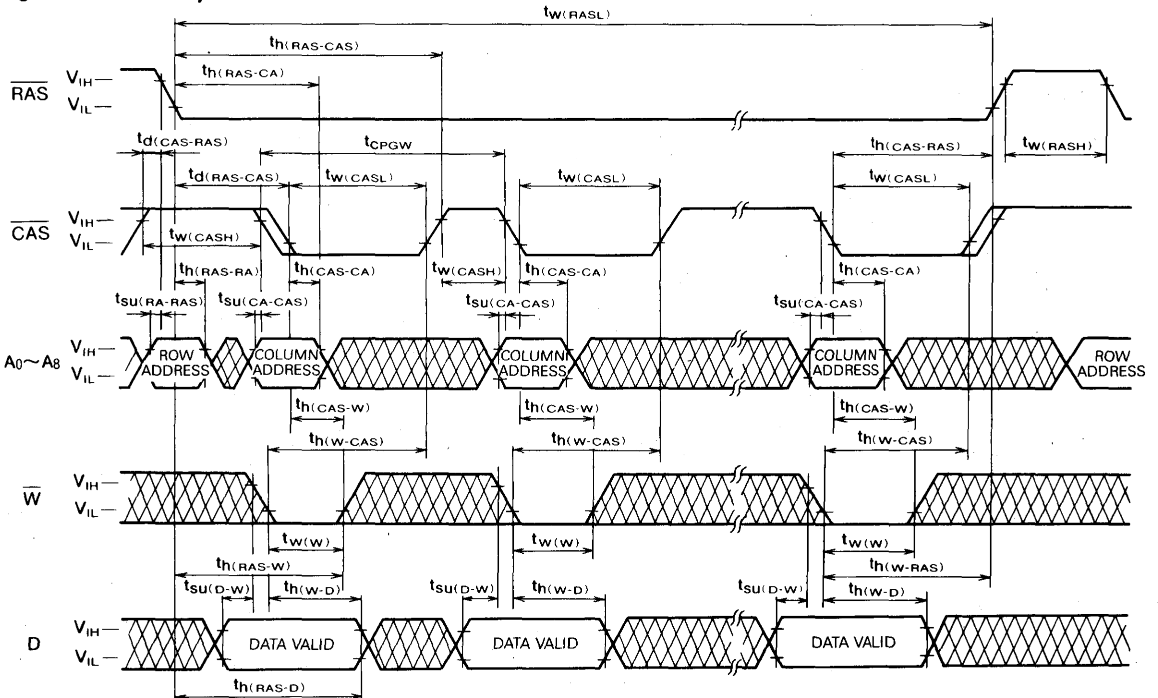
 The center-line indicates the high-impedance state.

Note 20. $\overline{CAS} = V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

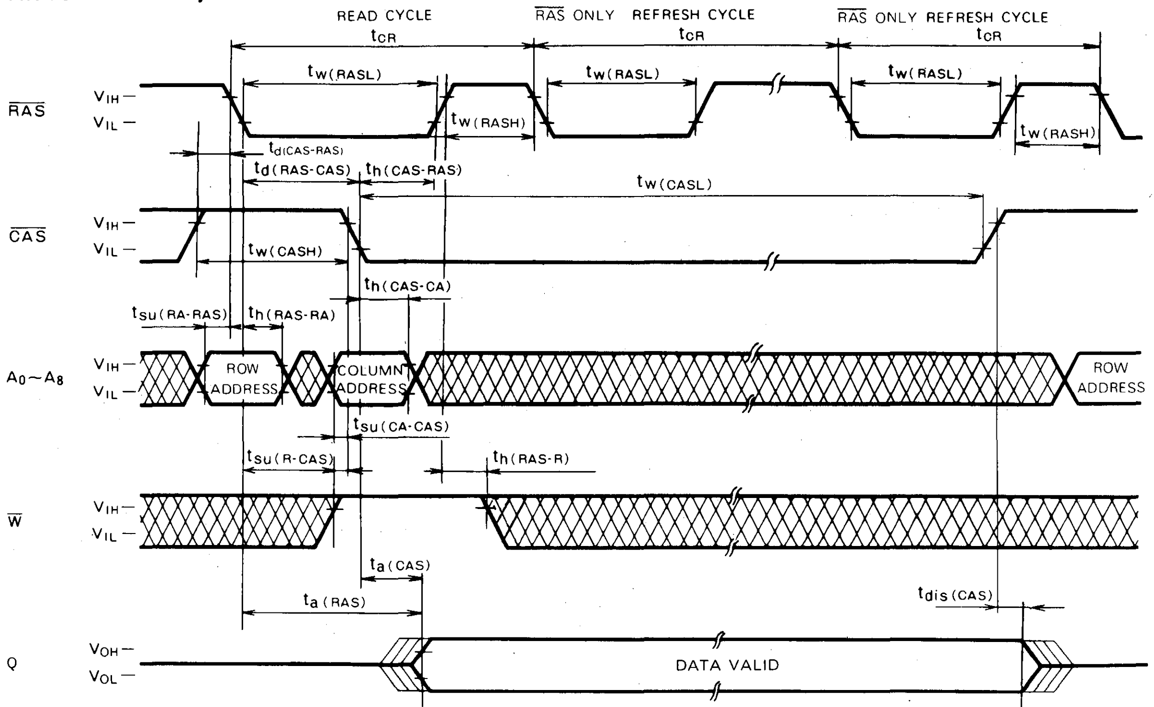
Page-Mode Read Cycle



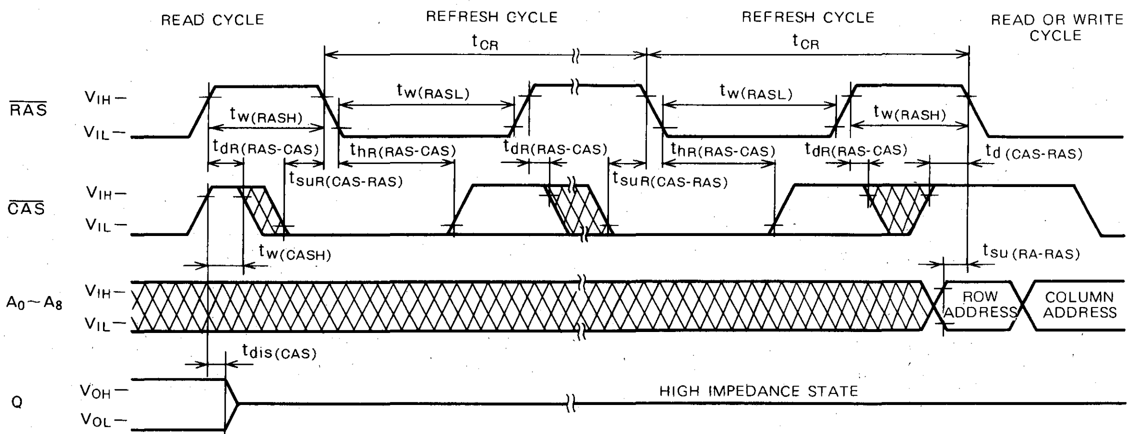
Page-Mode Write Cycle



Hidden Refresh Cycle



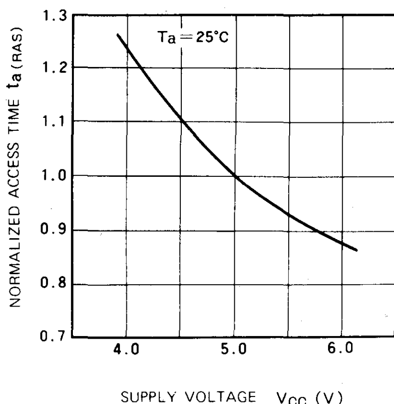
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh (Note 21)



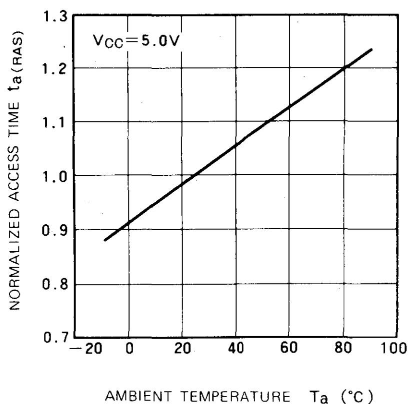
Note 21: $\overline{W}$, D = don't care.

TYPICAL CHARACTERISTICS

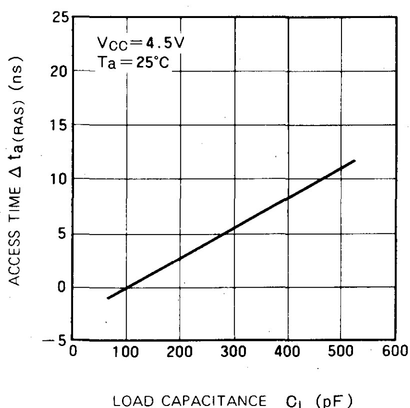
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



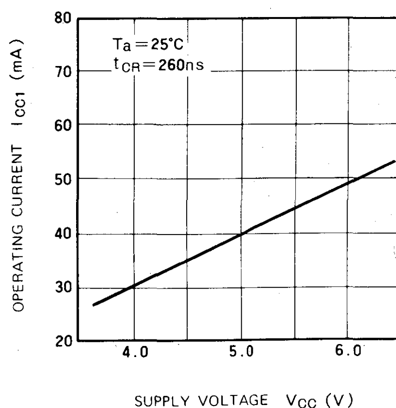
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



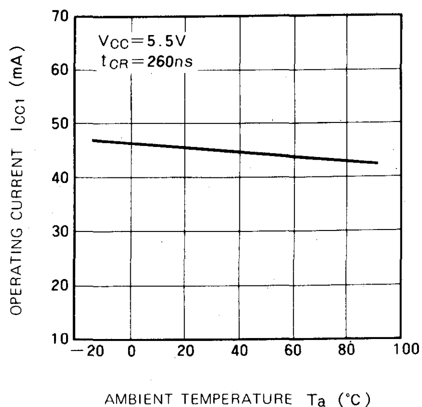
ACCESS TIME VS. LOAD CAPACITANCE



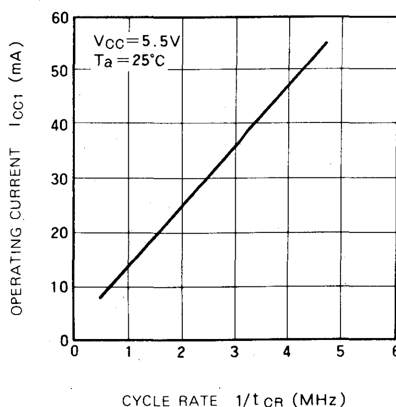
OPERATING CURRENT VS. SUPPLY VOLTAGE



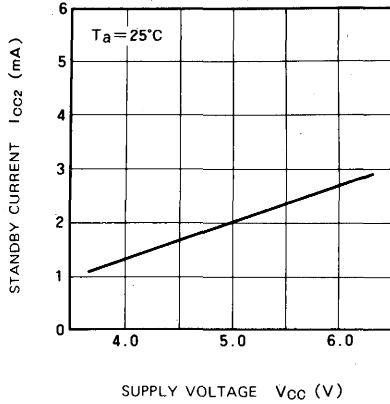
OPERATING CURRENT VS. AMBIENT TEMPERATURE

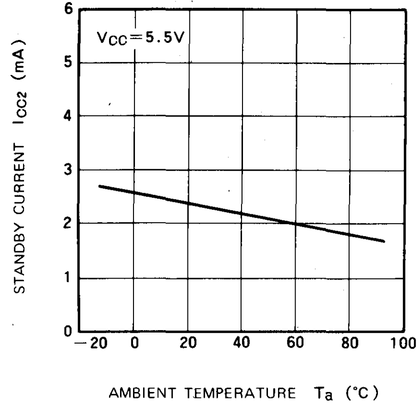


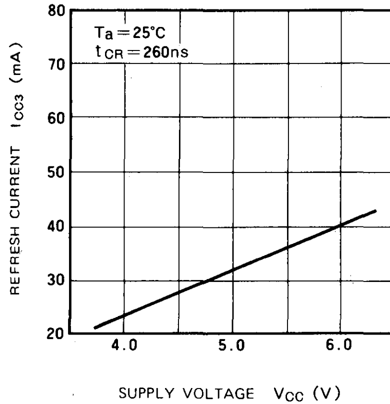
OPERATING CURRENT VS. CYCLE RATE

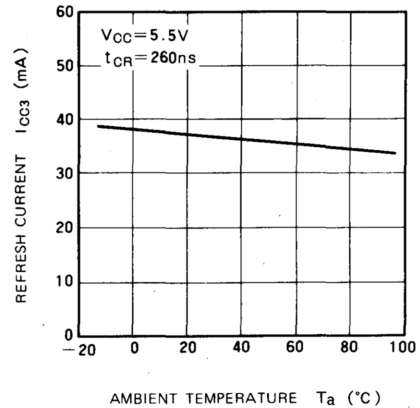


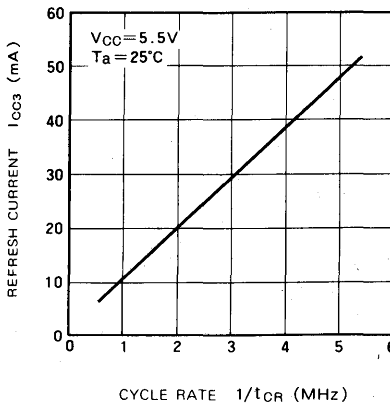
262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

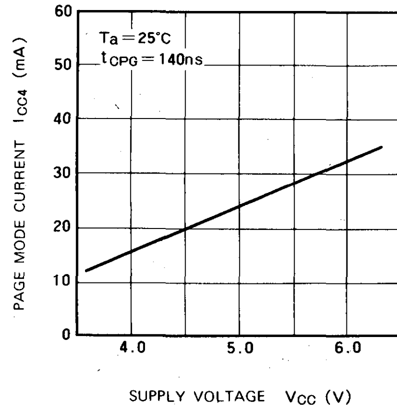




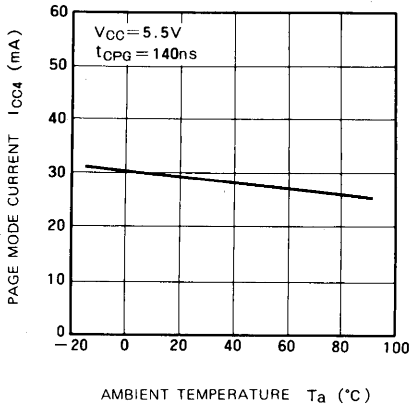




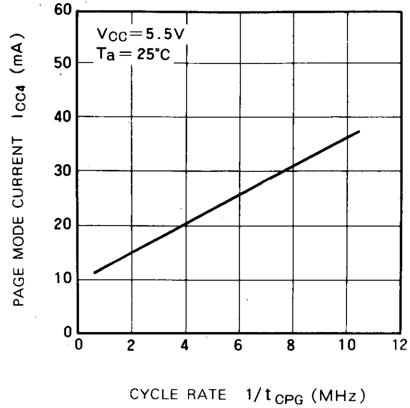




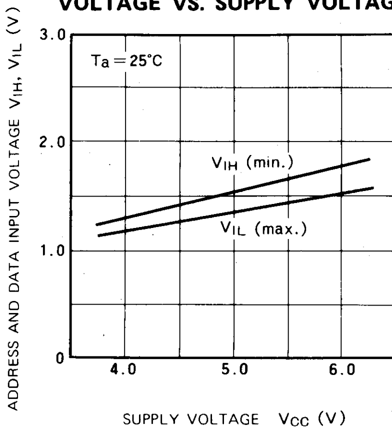
PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



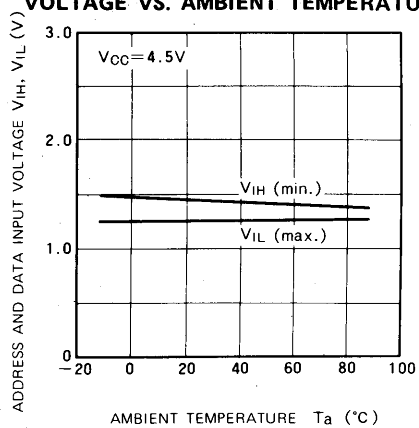
PAGE MODE CURRENT VS. CYCLE RATE



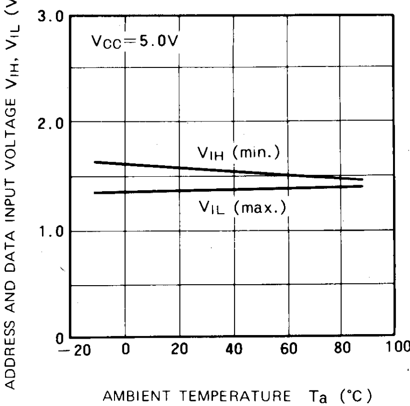
ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



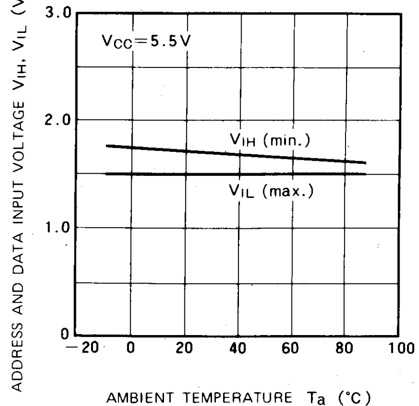
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



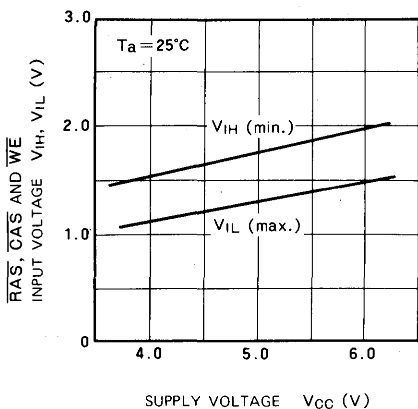
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



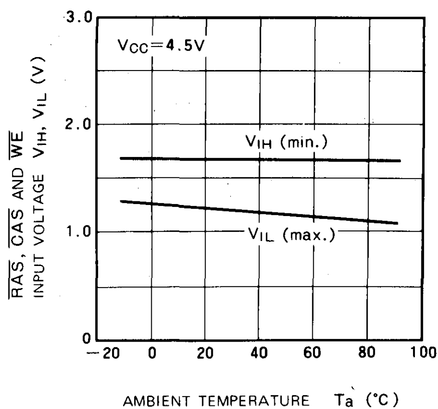
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



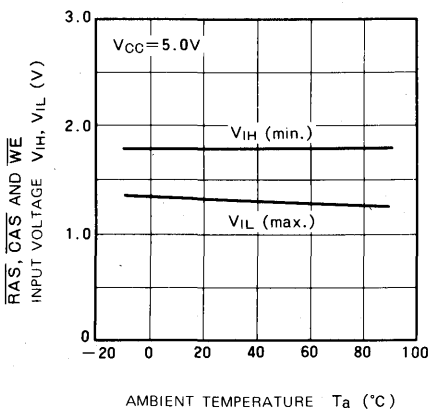
RAS, CAS AND WE INPUT VOLTAGE VS. SUPPLY VOLTAGE



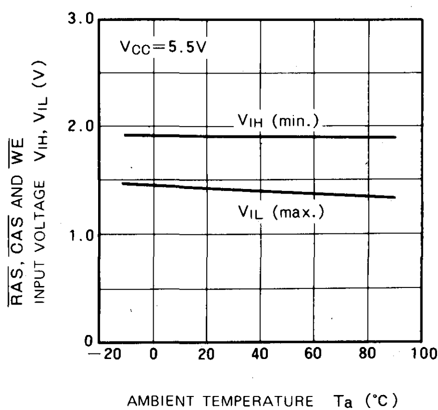
RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE

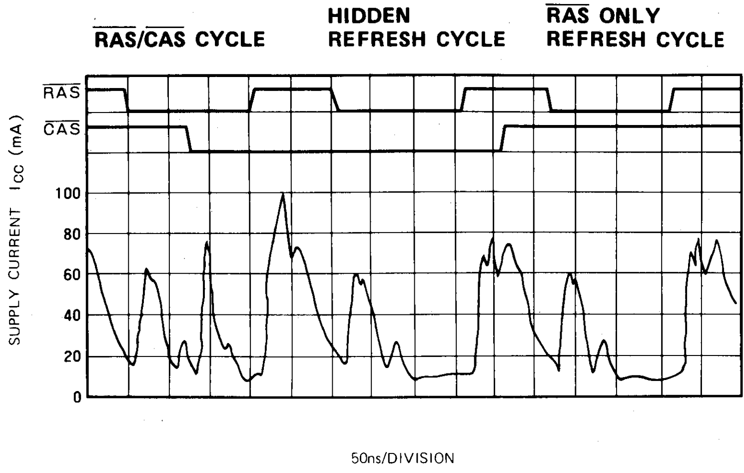


RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE

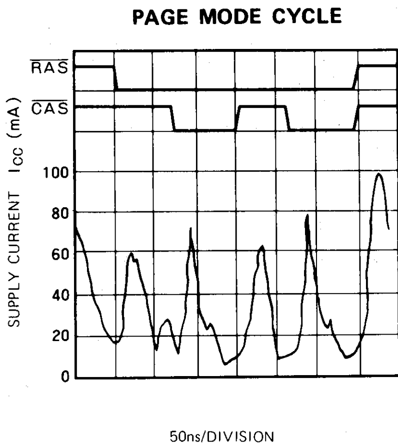


RAS, CAS AND WE INPUT VOLTAGE VS. AMBIENT TEMPERATURE

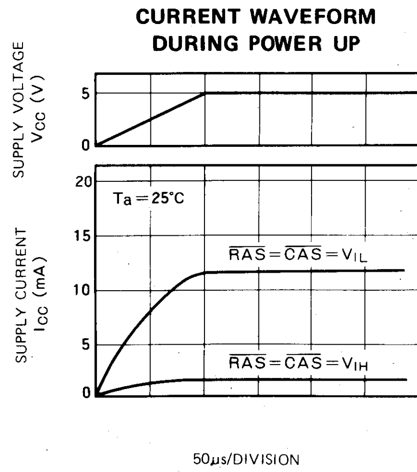




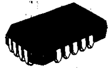
50ns/DIVISION



50ns/DIVISION



50μs/DIVISION



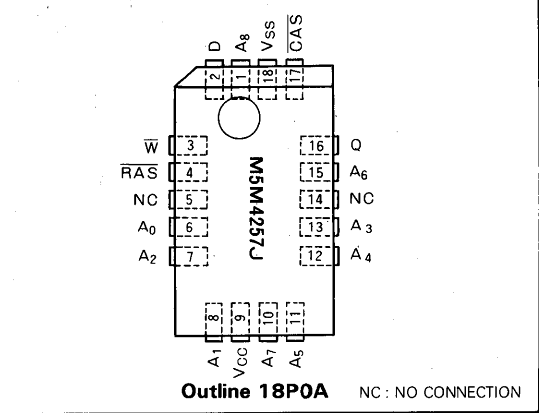
M5M4257J-10, -12, -15

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 18-pin plastic leaded chip carrier configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mo de, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

PIN CONFIGURATION (TOP VIEW)



Outline 18P0A NC : NO CONNECTION

FEATURES

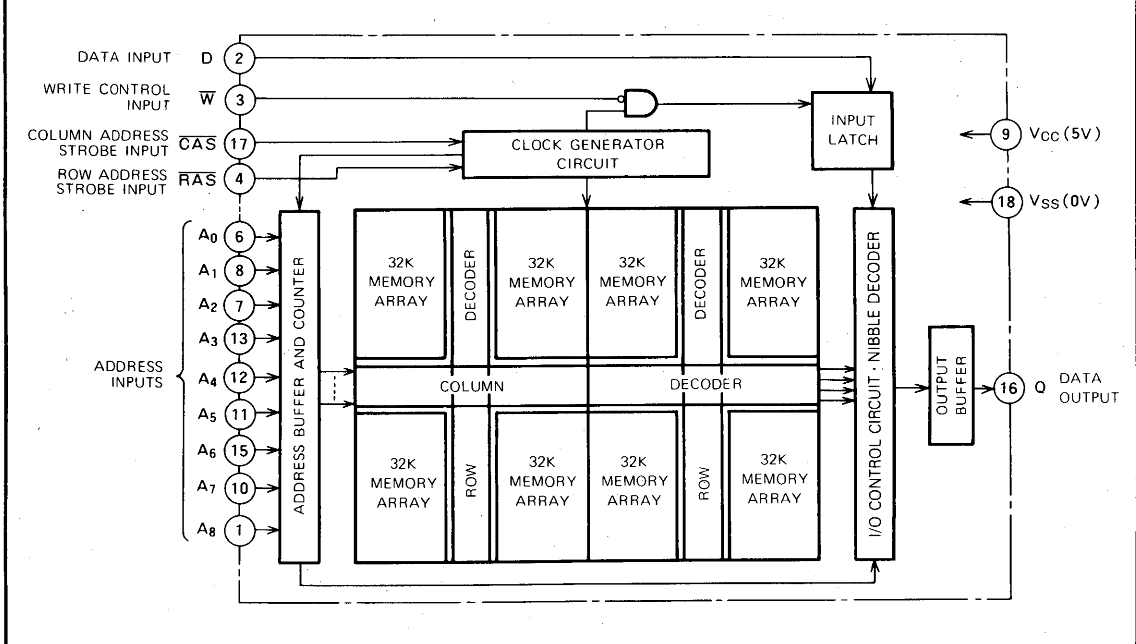
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4257J-10	100	200	300
M5M4257J-12	120	230	260
M5M4257J-15	150	260	230

- 18-pin plastic leaded chip carrier
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257J-10 . . . . 385mW (max)
  - M5M4257J-12 . . . . 360mW (max)
  - M5M4257J-15 . . . . 330mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms, Pin 1 is not needed for refresh
- $\overline{CAS}$ controlled output allows hidden refresh
- Output data can be held infinitely by $\overline{CAS}$.

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

FUNCTION

The M5M4257J provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., nibble mode, RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	RAS	CAS	W	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
CAS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
* : Nibble mode identical except refresh is No, and Nibble mode column address is DNC while togging CAS.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4257J the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse (RAS) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse (CAS) latches the 9 column-address bits. Timing of the RAS and CAS clocks can be selected by either of the following two methods:

1. The delay time from RAS to CAS $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal CAS control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\ max}$ ('gated CAS' operation). The external CAS signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of CAS has already been released, so that the internal CAS control signals are controlled by the externally applied CAS, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of W input and CAS input. Thus when the W input makes its negative transition prior to CAS input (early write), the data input is strobed by CAS, and the negative transition of CAS is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the W input makes its negative transition after CAS, the W negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4257J is in the high-impedance state when CAS is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until CAS goes high, irrespective of the condition of RAS.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4257J, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the CAS pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for RAS and CAS.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Nibble-Mode Operation

The M5M4257J is designed to allow high speed serial read, write or read-modify-write access of 4 bits of data. The first of 4 nibble bits is accessed by the normal mode with read data coming out at $t_{a(CAS)}$ time. Next 2, 3 or 4 nibble bits is read or writen by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Thus the time required to strobe in not only the row address but also the column address is eliminated, thereby faster access and shorter cycle time than that of Page-Mode is achieved.

Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address and allows to access to the next nibble bit. If more than 4 bits are accessed during this mode the same address bit will be accessed cyclically. In Nibble-Mode, any combination of read, write and read-modify-write operation is possible (e.g. first bit read, second bit write, third bit read-modify-write, etc.).

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4257J must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4257J are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4257J is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4257J is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4257J as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4257J operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1 ~ 7	V
V_I	Input voltage		−1 ~ 7	V
V_O	Output voltage		−1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4257J-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open			70	mA
		M5M4257J-12				65	
		M5M4257J-15				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = \overline{CAS} = V_{IH}$ output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4257J-10	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(\overline{RAS})}$ = min, output open			60	mA
		M5M4257J-12				55	
		M5M4257J-15				50	
$I_{CC5(AV)}$	Average supply current from V_{CC}, nibble mode	M5M4257J-10	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{CN} = min, output open			35	mA
		M5M4257J-12				30	
		M5M4257J-15				25	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4257J-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$ = min, Output open			65	mA
		M5M4257J-12				60	
		M5M4257J-15				55	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_i = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_i = 25mVrms			7	pF

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted. See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\ min}$ and $V_{IL\ max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for nibble-mode.
9. $t_{d(RAS-CAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$max can be met. $t_{d(RAS-CAS)}$max is specified reference point only, if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)min}$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max. Test conditions ; Load = 2TTL, C_L = 100pF
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions, Load = 2TTL C_L = 100pF

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time (Note 15)	t_{RWC}	225		260		295		ns
t_{CRMW}	Read-modify-write cycle time (Note 16)	t_{RMWC}	235		275		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write (Note 17)	t_{RWD}	90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write (Note 17)	t_{CWD}	40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write	t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write	t_{DH}	35		40		45		ns
$t_{dis(CAS)}$	Output disable time	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 15: t_{CRW} min is defined as t_{CRW} min $= t_{d(RAS-CAS)}$ max $+ t_{d(CAS-W)}$ min $+ t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: t_{CRMW} min is defined as t_{CRMW} min $= t_{a(RAS)}$ max $+ t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps, the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Nibble-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
t_{CN}	Nibble mode cycle time	t_{NC}	50		55		70		ns
$t_{aN(CAS)}$	Nibble mode access time	t_{NAC}		25		30		40	ns
$t_{wN(CASL)}$	Nibble mode $\overline{CAS}$ low pulse width	t_{NCAS}	25		30		40		ns
$t_{wN(CASH)}$	Nibble mode precharge time	t_{NP}	15		15		20		ns
$t_{hN(CAS-RAS)}$	Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25		30		40		ns
$t_{dN(CAS-W)}$	Nibble mode $\overline{CAS}$ to WRITE delay	t_{NCWD}	25		30		40		ns
$t_{wNRMW(CASL)}$	Nibble mode RMW $\overline{CAS}$ pulse width	t_{NCRW}	55		65		85		ns
$t_{hNRMW(W-CAS)}$	Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		30		40		ns
$t_{hNRMW(CAS-RAS)}$	Nibble mode RMW $\overline{RAS}$ hold time	t_{NWSH}	55		65		85		ns
$t_{suN(W-CAS)}$	Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$	t_{NWCS}	0		0		0		ns

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4257J-10		M5M4257J-12		M5M4257J-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

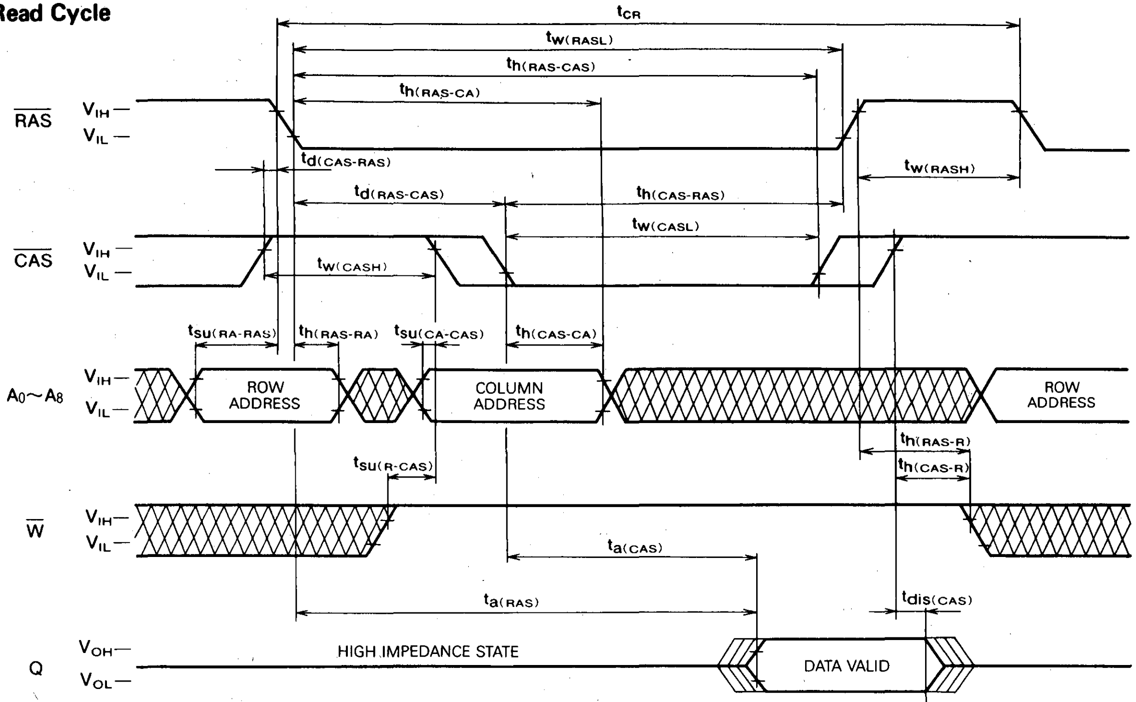
Note 18: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Nibble Mode Addressing Sequence Example

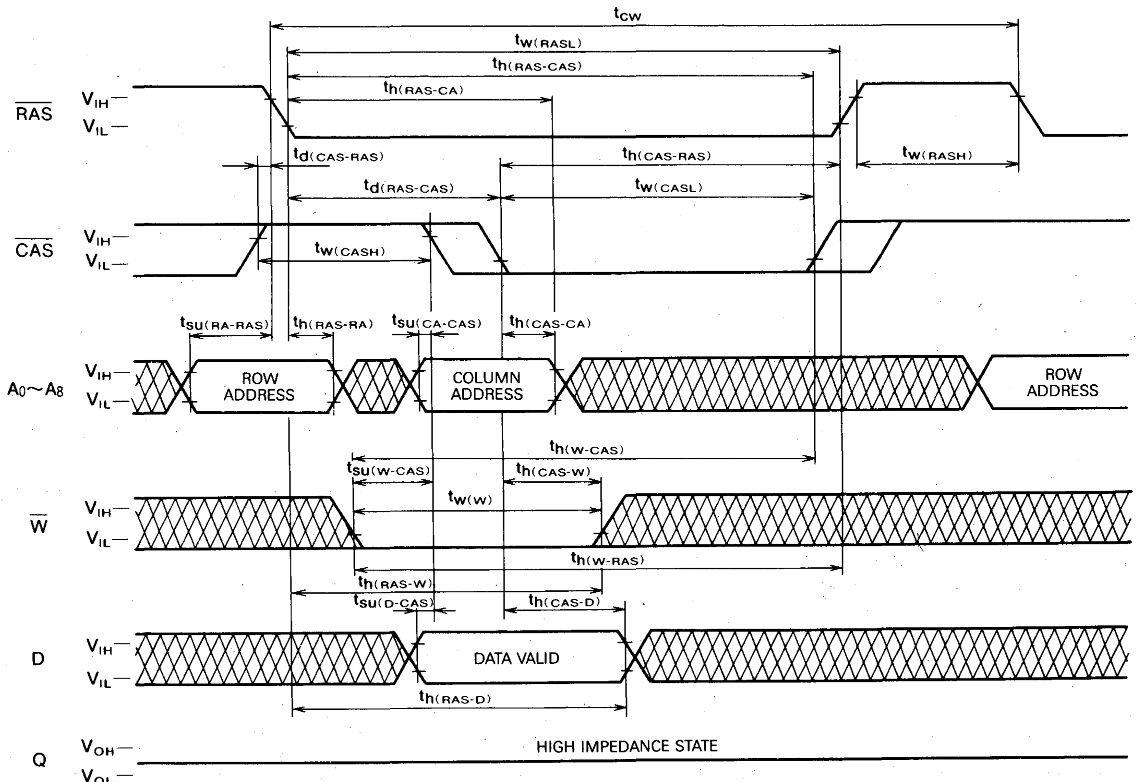
Sequence	Nibble bit	Column address									Row address									
		A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	
$\overline{RAS}$/$\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	External address
toggle $\overline{CAS}$	2	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	1	Internally generated address
toggle $\overline{CAS}$	3	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	
toggle $\overline{CAS}$	4	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	1	
toggle $\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	

TIMING DIAGRAMS (Note 19)

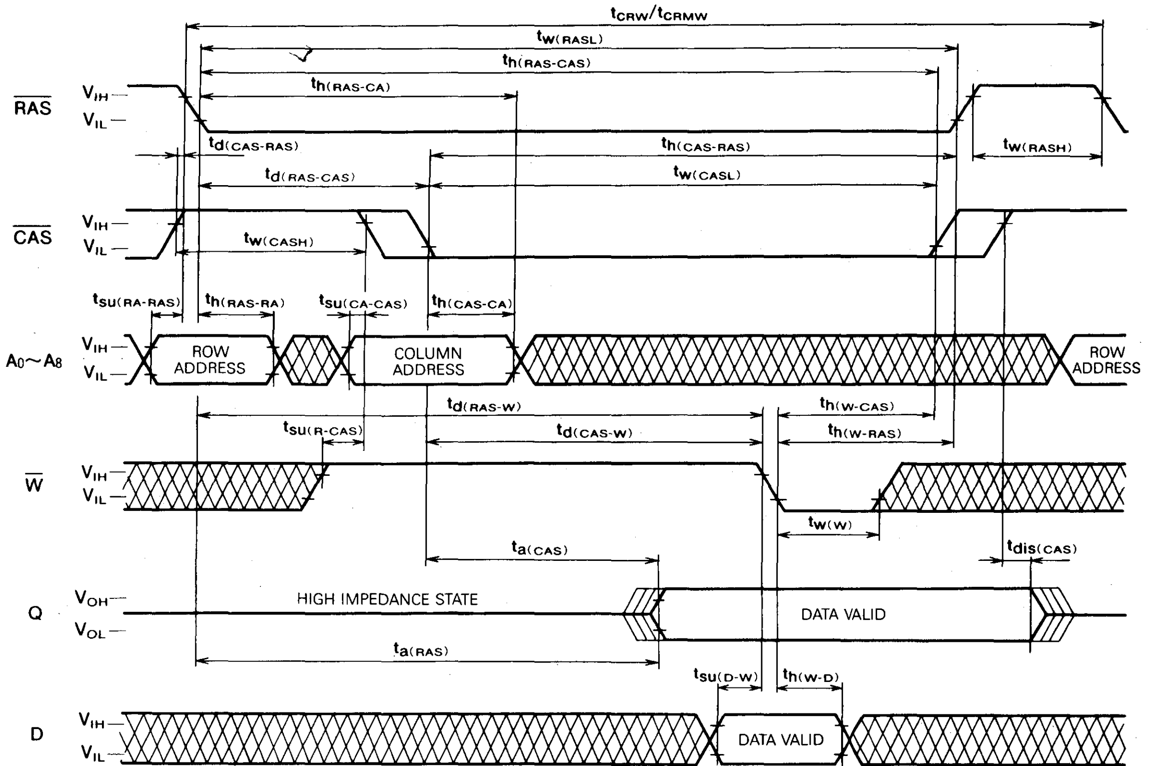
Read Cycle



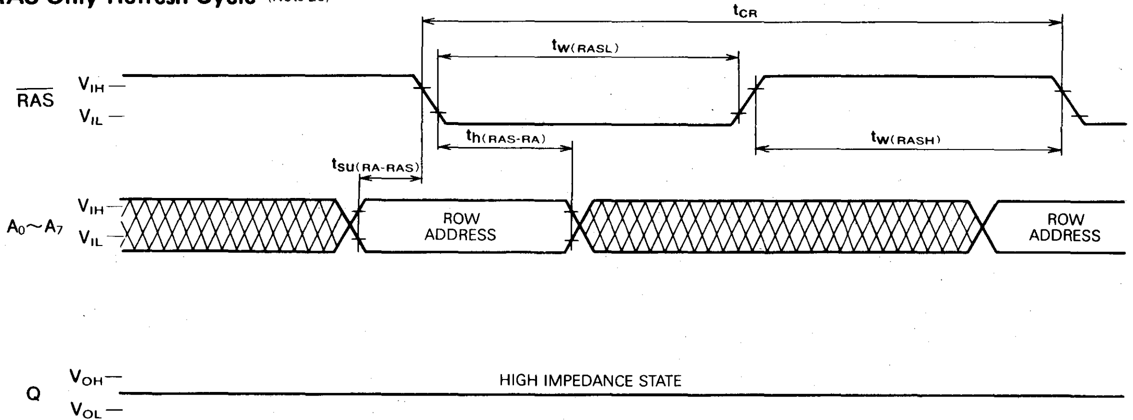
Write Cycle (Early Write)



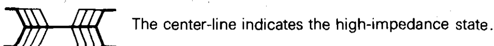
Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

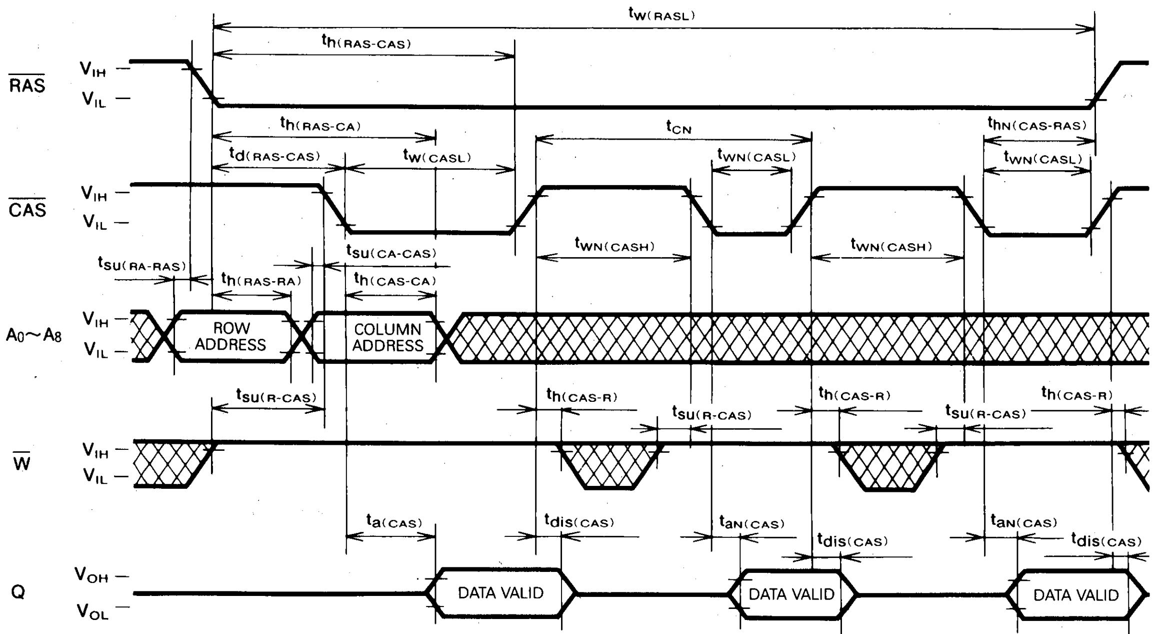


Note 19. Indicates the don't care input.

 The center-line indicates the high-impedance state.

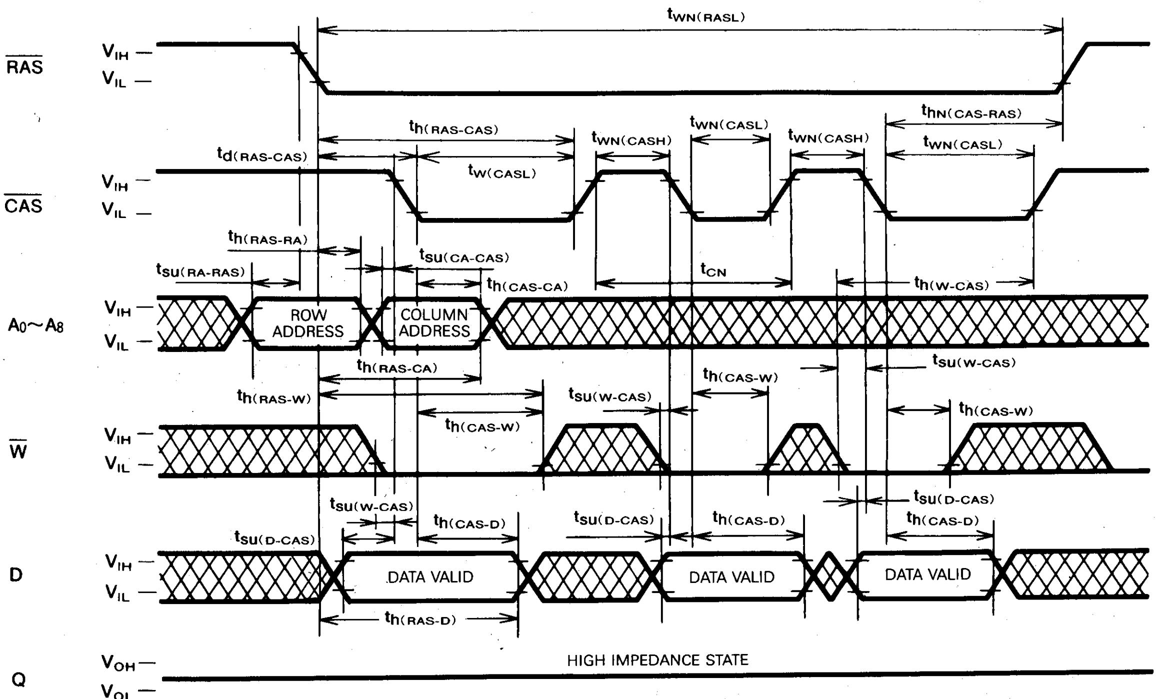
Note 20. $\overline{CAS}=V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

Nibble Mode Read Cycle (Note 21)

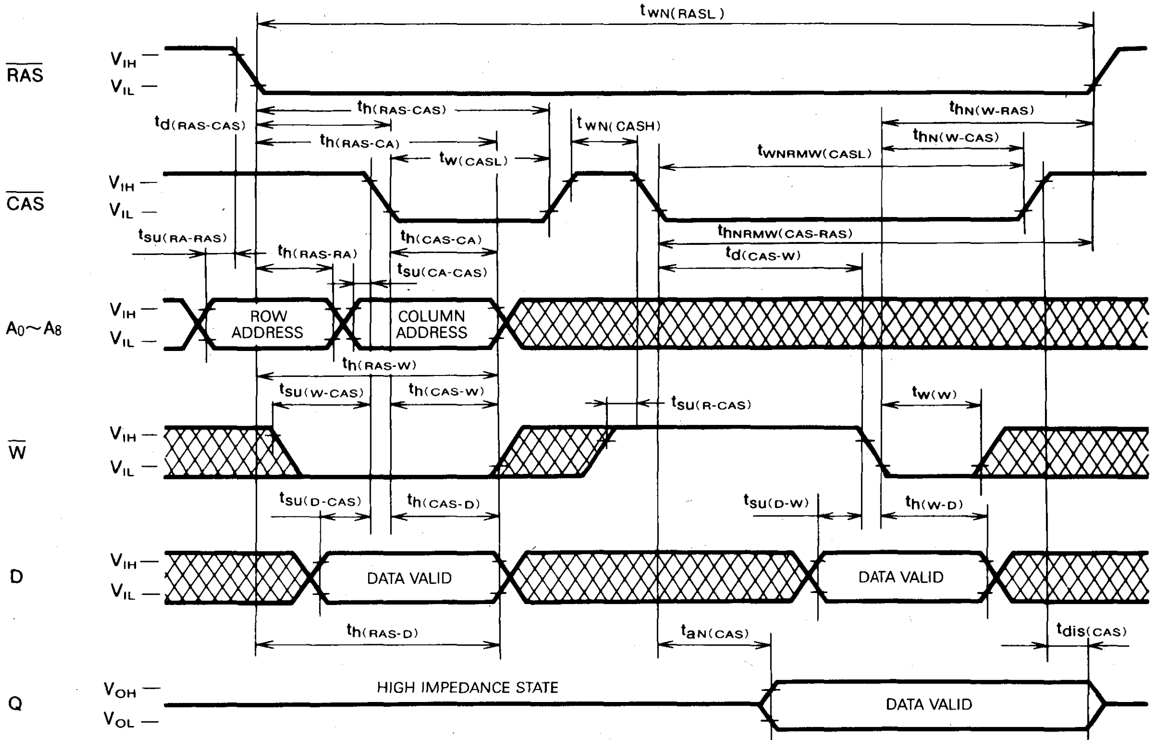


Note 21. Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

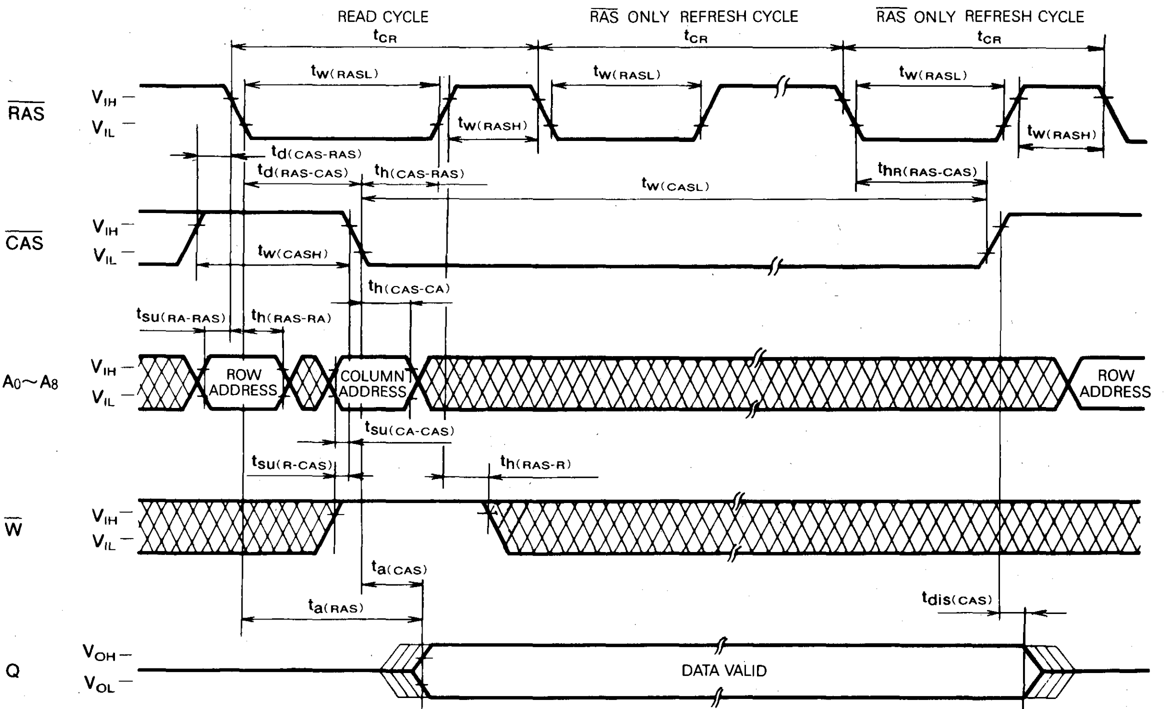
Nibble Mode Write Cycle (Early Write)



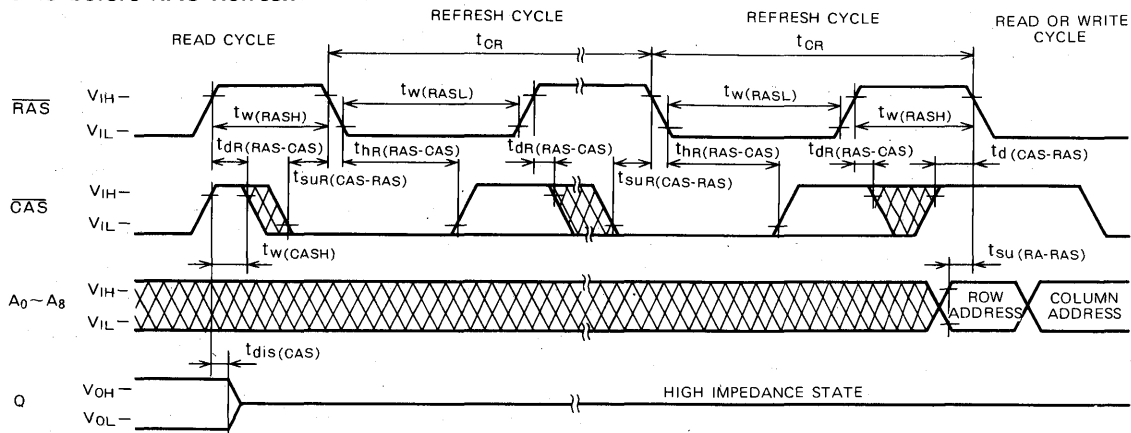
Nibble Mode Read-Modify-Write



Hidden Refresh Cycle



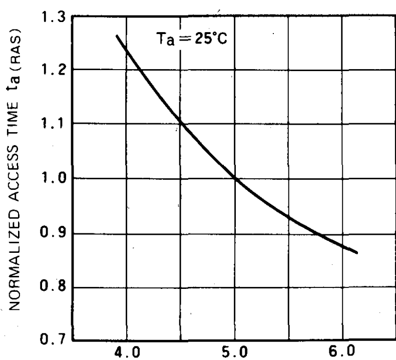
CAS before RAS Refresh (Note 22)



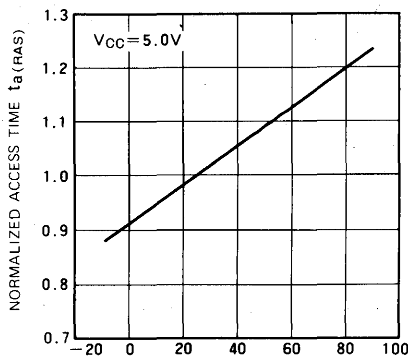
Note 22: $\overline{W}$, D = don't care.

TYPICAL CHARACTERISTICS

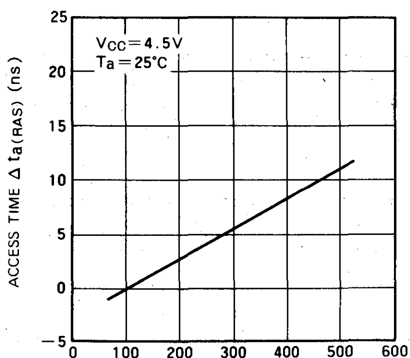
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



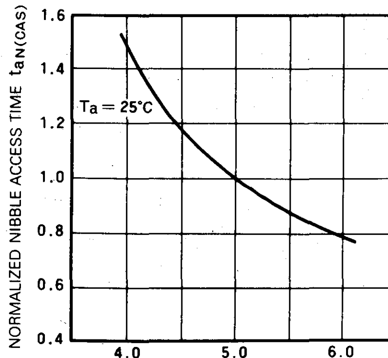
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE

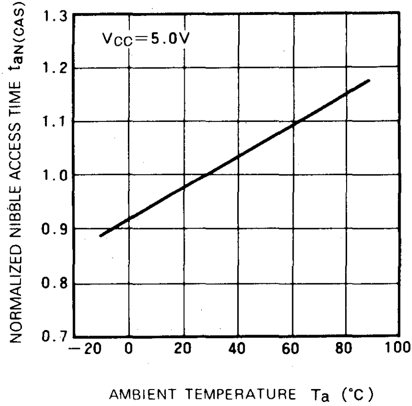


NIBBLE MODE ACCESS TIME VS. SUPPLY VOLTAGE

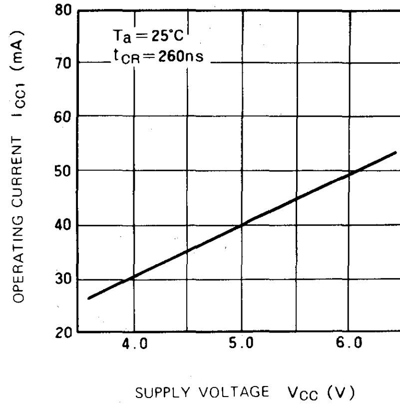


262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

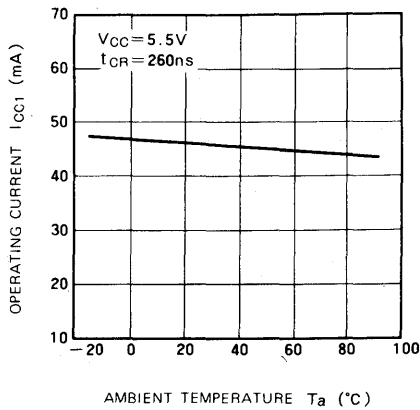
NIBBLE MODE ACCESS TIME VS. AMBIENT TEMPERATURE



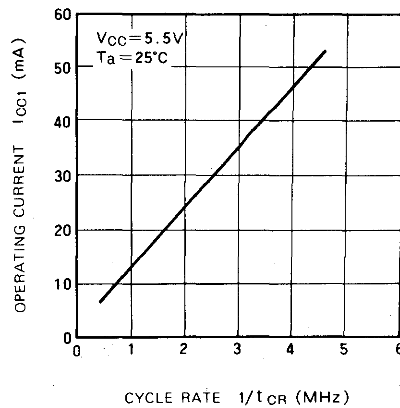
OPERATING CURRENT VS. SUPPLY VOLTAGE



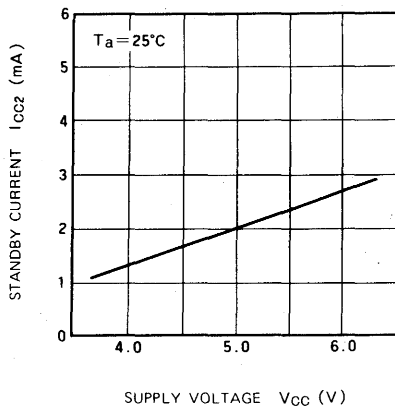
OPERATING CURRENT VS. AMBIENT TEMPERATURE



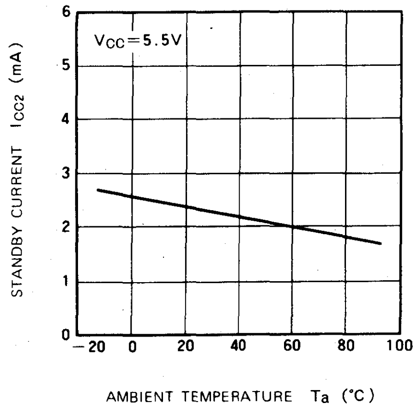
OPERATING CURRENT VS. CYCLE RATE



STANDBY CURRENT VS. SUPPLY VOLTAGE

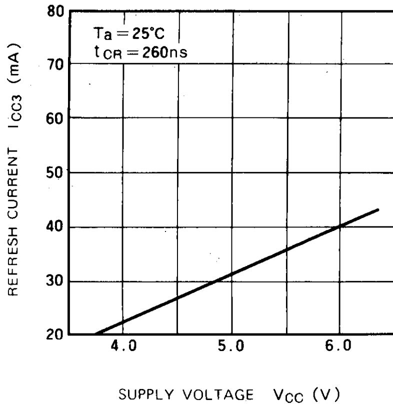


STANDBY CURRENT VS. AMBIENT TEMPERATURE

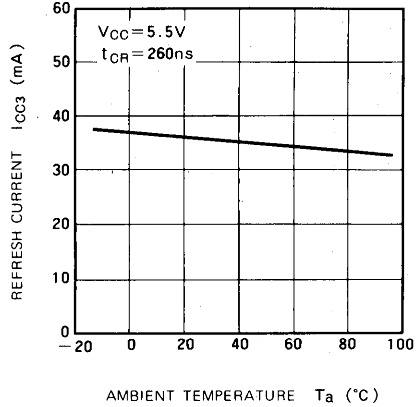


262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

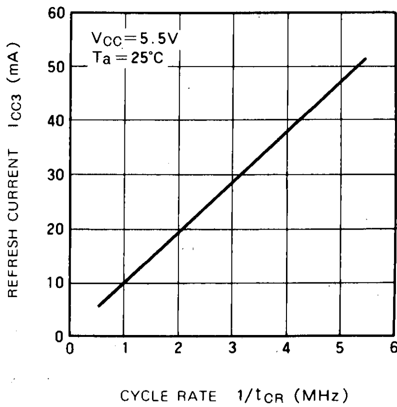
REFRESH CURRENT VS. SUPPLY VOLTAGE



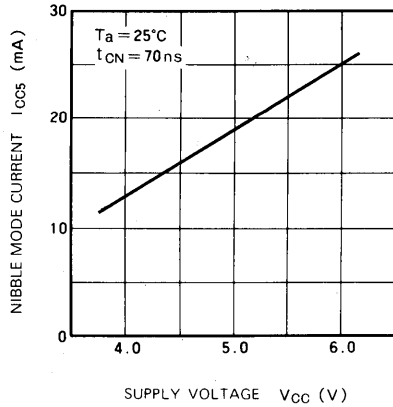
REFRESH CURRENT VS. AMBIENT TEMPERATURE



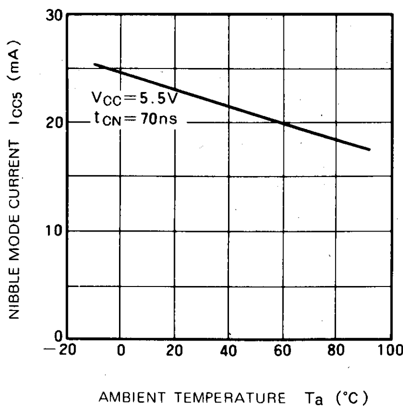
REFRESH CURRENT VS. CYCLE RATE



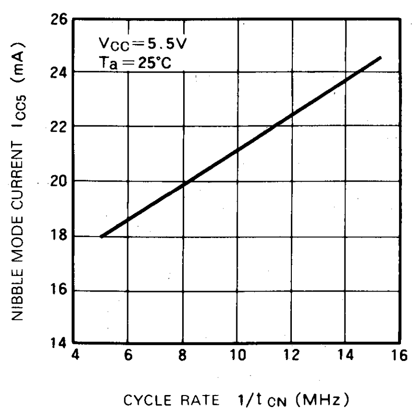
NIBBLE MODE CURRENT VS. SUPPLY VOLTAGE

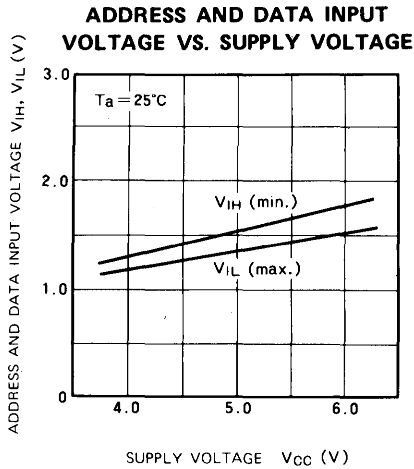


NIBBLE MODE CURRENT VS. AMBIENT TEMPERATURE

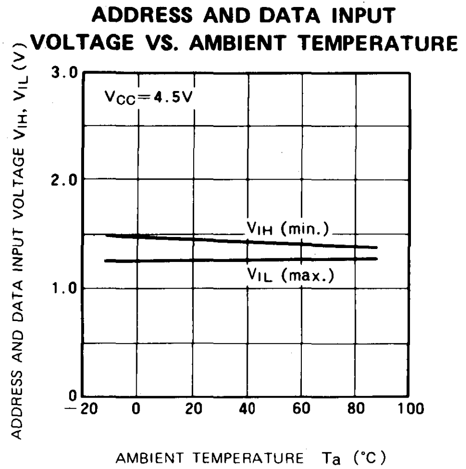


NIBBLE MODE CURRENT VS. CYCLE RATE

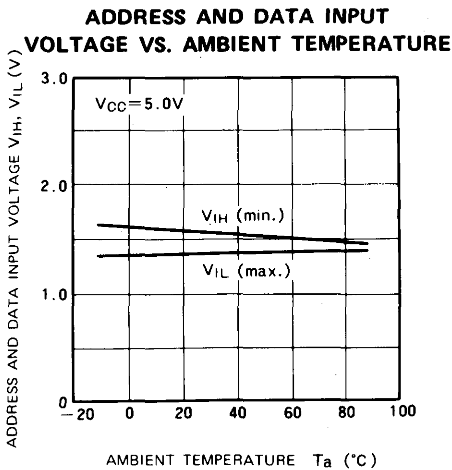




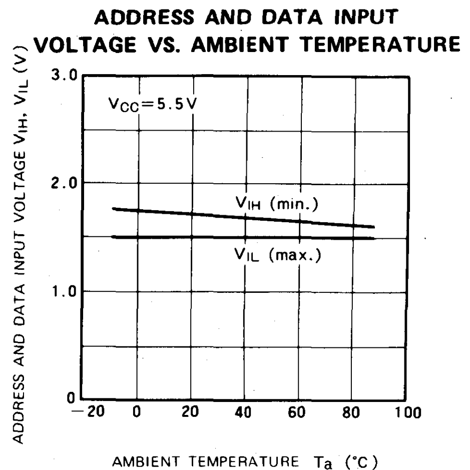
ADDRESS AND DATA INPUT
VOLTAGE VS. SUPPLY VOLTAGE
Ta = 25°C
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
4.0
5.0
6.0
ADDRESS AND DATA INPUT VOLTAGE VIH, VIL (V)
SUPPLY VOLTAGE VCC (V)



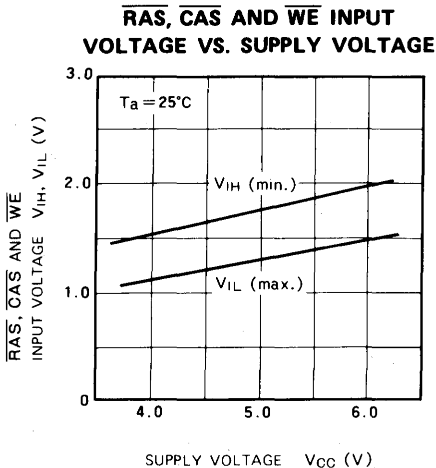
ADDRESS AND DATA INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC = 4.5V
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
ADDRESS AND DATA INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)



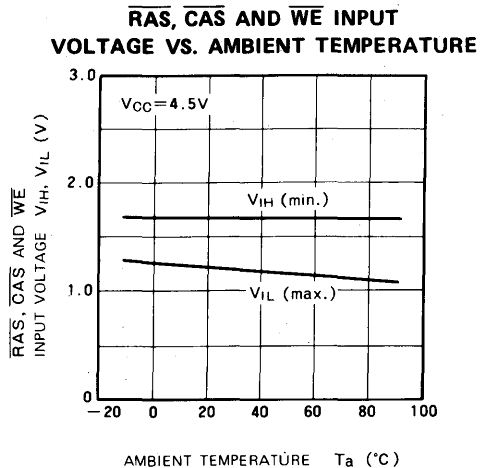
ADDRESS AND DATA INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC = 5.0V
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
ADDRESS AND DATA INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)



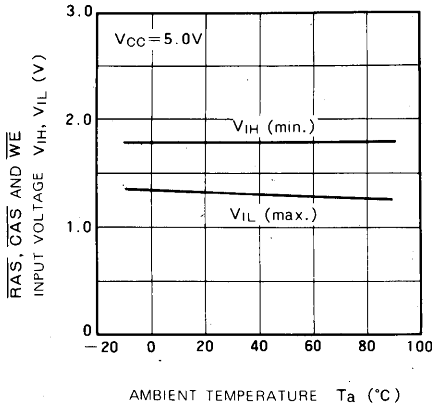
ADDRESS AND DATA INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC = 5.5V
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
ADDRESS AND DATA INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)

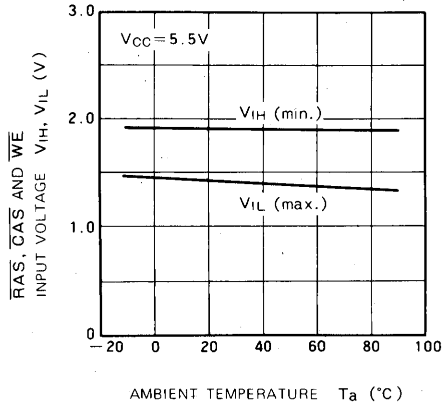


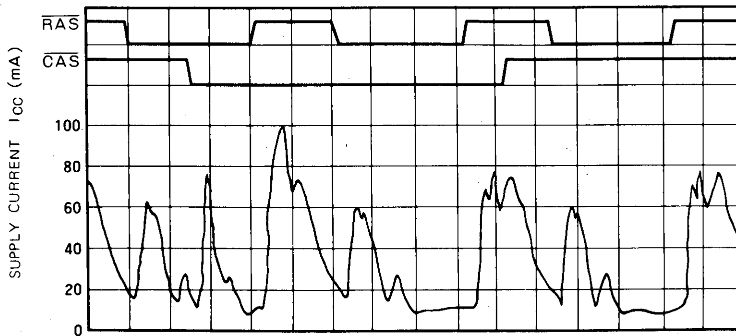
RAS, CAS AND WE INPUT
VOLTAGE VS. SUPPLY VOLTAGE
Ta = 25°C
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
4.0
5.0
6.0
RAS, CAS AND WE
INPUT VOLTAGE VIH, VIL (V)
SUPPLY VOLTAGE VCC (V)

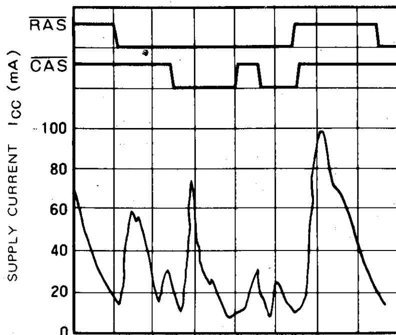


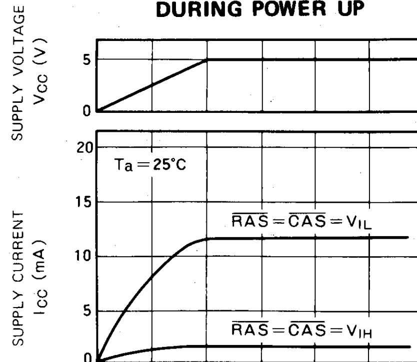
RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC = 4.5V
VIH (min.)
VIL (max.)
3.0
2.0
1.0
0
−20
0
20
40
60
80
100
RAS, CAS AND WE
INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)


RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC=5.0V
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)

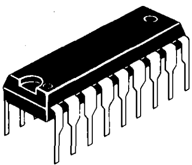

RAS, CAS AND WE INPUT
VOLTAGE VS. AMBIENT TEMPERATURE
VCC=5.5V
VIH (min.)
VIL (max.)
RAS, CAS AND WE INPUT VOLTAGE VIH, VIL (V)
AMBIENT TEMPERATURE Ta (°C)


RAS/CAS CYCLE
HIDDEN REFRESH CYCLE
RAS ONLY REFRESH CYCLE
RAS
CAS
SUPPLY CURRENT ICC (mA)
50ns/DIVISION


NIBBLE MODE CYCLE
RAS
CAS
SUPPLY CURRENT ICC (mA)
50ns/DIVISION


CURRENT WAVEFORM DURING POWER UP
SUPPLY VOLTAGE VCC (V)
Ta=25°C
RAS=CAS=VIL
RAS=CAS=VIH
SUPPLY CURRENT ICC (mA)
50μs/DIVISION

M5M4464P-10, -12, -15



262144-BIT (65536-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65536-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package configuration and an increase in system densities. The M5M4464P operates on a 5V power supply using the on-chip substrate bias generator.

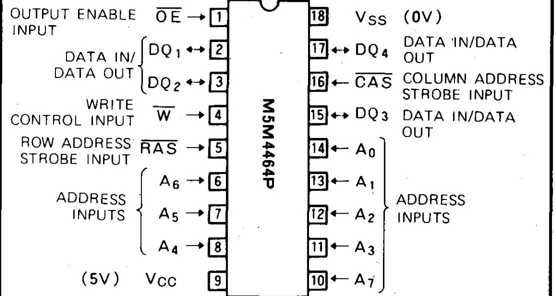
FEATURES

- Performance ranges

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4464P-10	100	200	300
M5M4464P-12	120	220	260
M5M4464P-15	150	260	230

- 65536 x 4 Organization
- Industry standard 18-pin dual in line package
- Single 5V ±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4464P-10 420mW (max)
  - M5M4464P-12 360mW (max)
  - M5M4464P-15 330mW (max)

PIN CONFIGURATION (TOP VIEW)



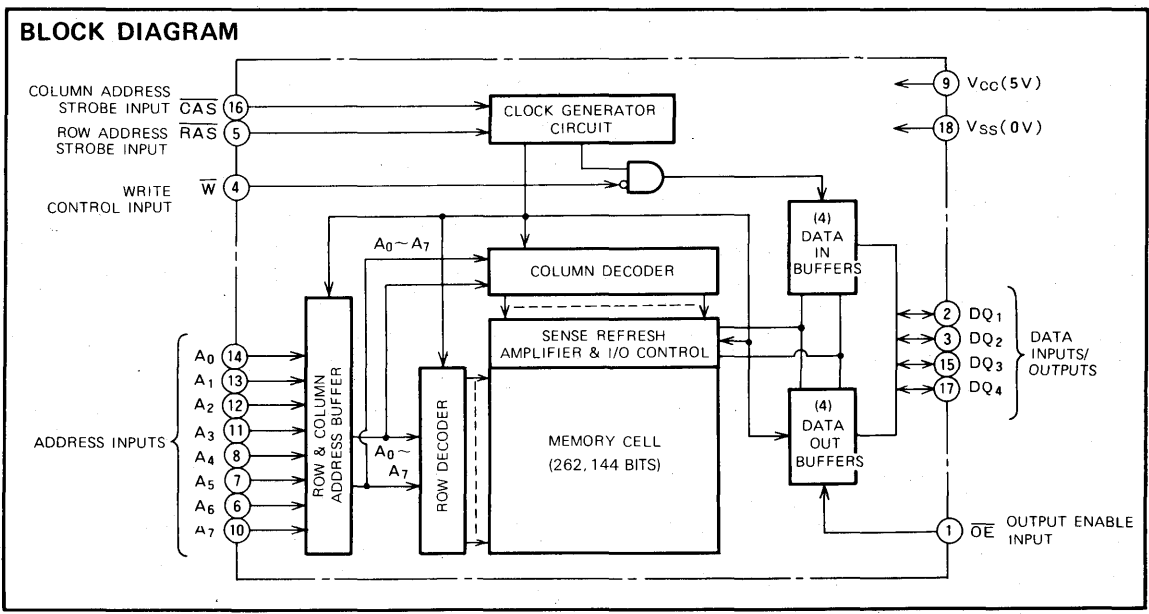
Outline 18 P4H

- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 256 refresh cycles/4ms
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30μs max

APPLICATION

Refresh memory for CRT, Microcomputer memory

BLOCK DIAGRAM



FUNCTION

The M5M4464P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column adress	Input DQ	Output DQ		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	
Write (Early Write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	Page mode identical
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only retfesh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262144 memory cells in the M5M4464P the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to CAS $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OEHD}.

output enable ($\overline{OE}$)

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4464P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4464P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available until $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4464P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4464P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4464P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4464P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

262144-BIT(65536-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	Condtions	Ratings	Unit
V_{CC}	Supply volrage	With respect to V_{SS}	$-1\sim7$	V
V_I	Input voltage		$-1\sim7$	V
V_O	Output voltage		$-1\sim7$	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		$0\sim70$	°C
Tstg	Storage temperature		$-65\sim150$	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		$I_{OH}=-5mA$	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		$I_{OL}=4.2mA$	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V\leqq V_{OUT}\leqq5.5V$	−10		10	μA
I_I	Input current		$0V\leqq V_{IN}\leqq6.5V$, All other pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{cc}, operating (Note 3,4)	M5M4464P-10	$\overline{RAS}$, $\overline{CAS}$ cycling tc(rd)=tc(w) = min output open			75	mA
		M5M4464P-12				65	
		M5M4464P-15				60	
I_{CC2}	Supply current from V_{cc}, standby		$\overline{RAS}=V_{IH}$ output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{cc}, retreshing (Note 3)	M5M4464P-10	$\overline{RAS}$ cycling $\overline{CAS}=V_{IH}$ tc(Prd) = min, output open			60	mA
		M5M4464P-12				55	
		M5M4464P-15				50	
$I_{CC4(AV)}$	Average supply current from V_{cc}, page mode (Note 3,4)	M5M4464P-10	$\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling tc(Prd) = min, output open			55	mA
		M5M4464P-12				50	
		M5M4464P-15				45	
$I_{CC6(AV)}$	Average supply current from V_{cc}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4464P-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tc(RAS)= min, output open			65	mA
		M5M4464P-12				60	
		M5M4464P-15				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the tastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			5	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				10	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464P-10		M5M4464P-12		M5M4464P-15		
				Min	Max	Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,7)	t_{CAC}		50		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,8)	t_{RAC}		100		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	—		25		30		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 9)	t_{OFF}	0	25	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 9)	—	0	25	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RLCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If t_{RLCL} is greater than t_{RLCL} max then $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464P-10		M5M4464P-12		M5M4464P-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(RF)}$	Refresh cycle time		t_{REF}		4		4		4	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	90		90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	50	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	10		10		10		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	70		80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	3	50	ns

Note 10: The timing requirements are assumed t_T=5ns.
11: V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; if t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. if t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

Read and Refresh Cycles

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464P-10		M5M4464P-12		M5M4464P-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time		t_{RC}	200		220		260		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	50	100000	60	100000	75	100000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		35		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	50		60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	(Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	(Note 15)	t_{RRH}	10		10		10		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		—	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		—	25		30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		25		30		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		—	0		0		0		ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464P-10		M5M4464P-12		M5M4464P-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(W)}$	Write cycle time	t_{RC}	200		220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50	100000	60	100000	75	100000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		35		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	50		60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		−5		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	35		40		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	85		100		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	35		40		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		90		110		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after Write low	—	25		25		30		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464P-10		M5M4464P-12		M5M4464P-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(rdW)}$	Read write/read modify write cycle time (Note 16)	t_{RWC}	270		295		345		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	170	10000	195	10000	235	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	120	100000	135	100000	160	100000	ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	170		195		235		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	120		135		160		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		35		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	35		40		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	—	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		25		30		ns

Note 16: $t_{C(rdW)}$ is specified as $t_{C(rdW)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{w(RH)}$ min + 4 t_T.

Page-Mode Cycle (Note 17)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464P-10		M5M4464P-12		M5M4464P-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	100		120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	100		120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 18)	t_{RAS}	200	30000	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read write/read modify write cycle time	—	170		195		230		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	340	30000	390	30000	465	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		50		60		ns

Note 17: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
18: Specified for read or write cycle.
19: Specified for read-write or read-modify-write cycle.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464P-10		M5M4464P-12		M5M4464P-15		
			Min	Max	Min	Max	Min	Max	
$t_{SU\,R(CR)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	10		10		10		ns
$t_{h\,R(RC)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	20		25		30		ns
$t_{d\,R(RC)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

Note 20: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

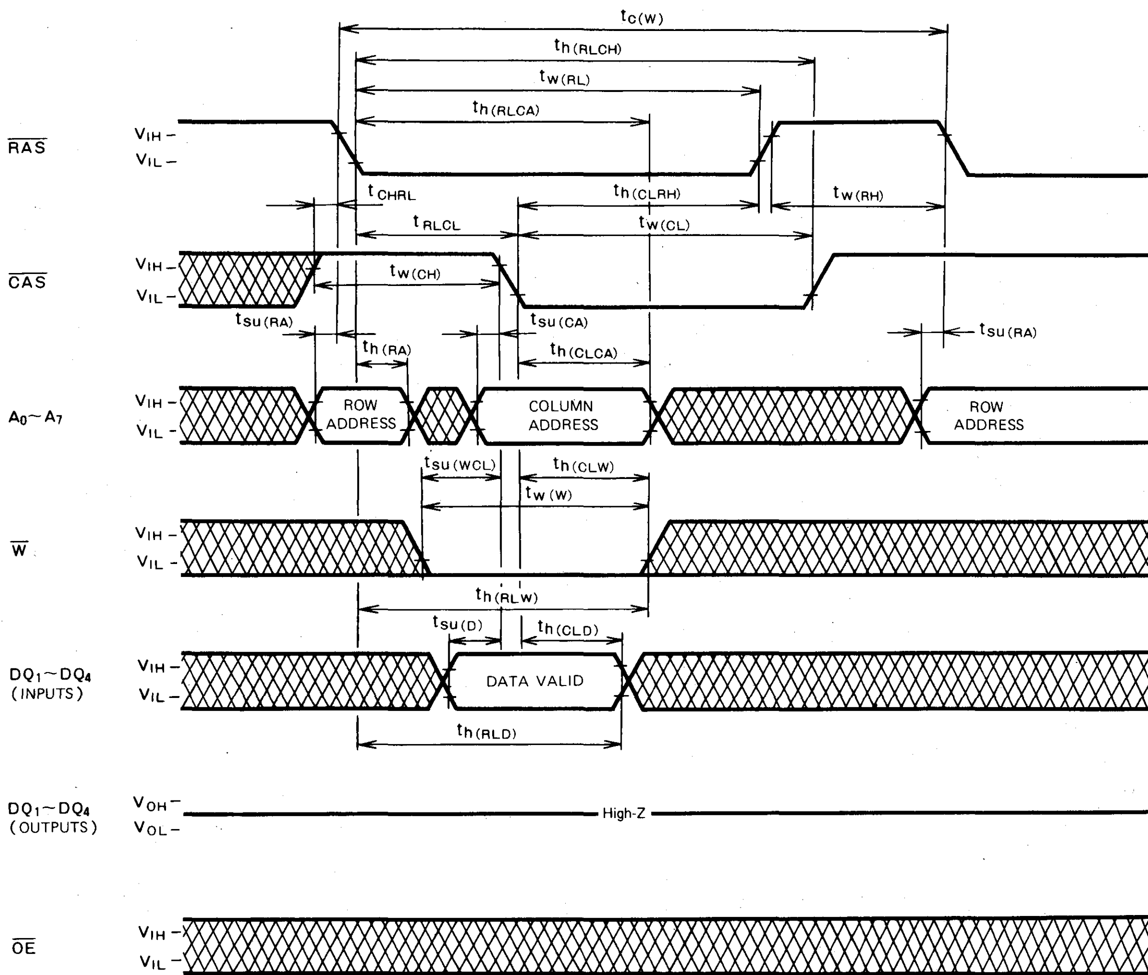
TIMING DIAGRAMS (Note 21)

Read Cycle

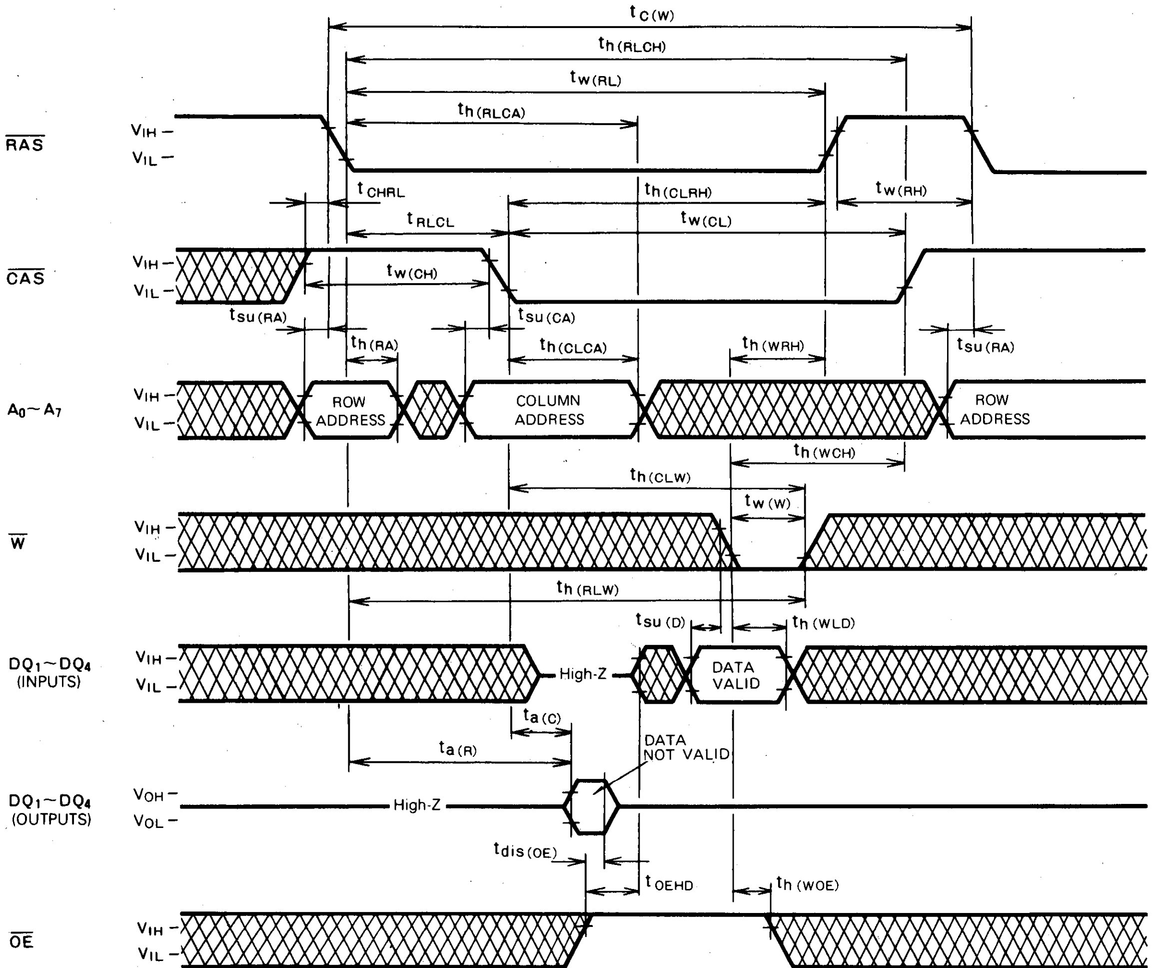
$t_{C(rd)}$
$t_{h(RLCH)}$
$t_{w(RL)}$
$t_{h(RLCA)}$
RAS VIH VIL
t_{CHRL} $t_{h(CLRH)}$ $t_{w(RH)}$
t_{RLCL} $t_{w(CL)}$
CAS VIH VIL
$t_{w(CH)}$
$t_{su(RA)}$ $t_{su(CA)}$ $t_{su(RA)}$
$t_{h(RA)}$ $t_{h(CLCA)}$
$A_0 \sim A_7$ VIH VIL
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
$t_{su(rd)}$ $t_{h(CHrd)}$ $t_{h(RHrd)}$
W VIH VIL
$DQ_1 \sim DQ_4$ (INPUTS) VIH VIL
High-Z
$t_{a(C)}$
$t_{a(R)}$ $t_{dis(CH)}$
$DQ_1 \sim DQ_4$ (OUTPUTS) VOH VOL
High-Z
DATA VALID
t_{DOEL} $t_{a(OE)}$ $t_{dis(OE)}$
$t_{h(OERH)}$ t_{OEHD}
$t_{h(OECH)}$
OE VIH VIL
$t_{h(CLOE)}$
$t_{h(RLOE)}$

Note 21. Indicates the don't care input.

Write Cycle (Early Write)

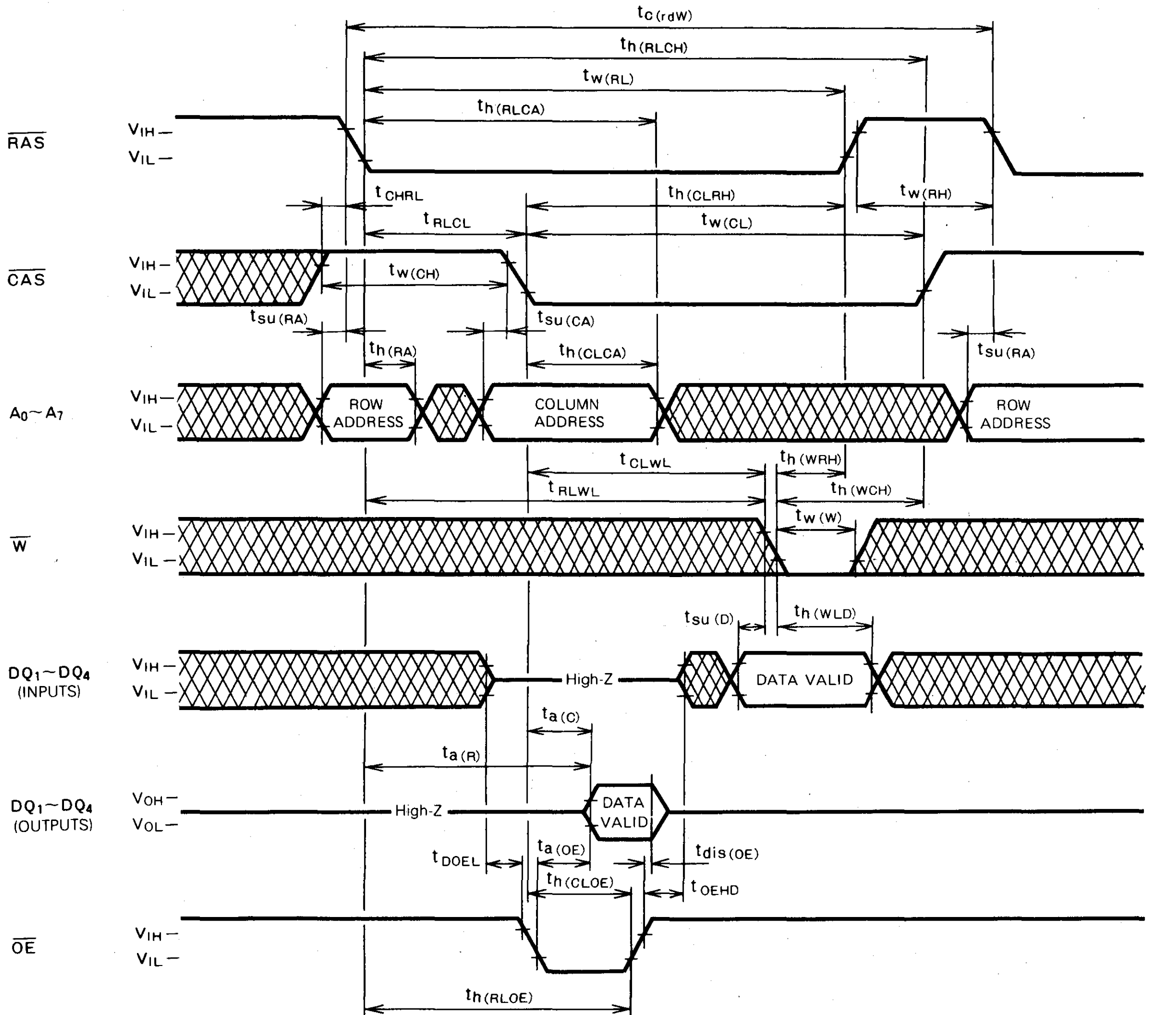


Write Cycle (Delayed Write)

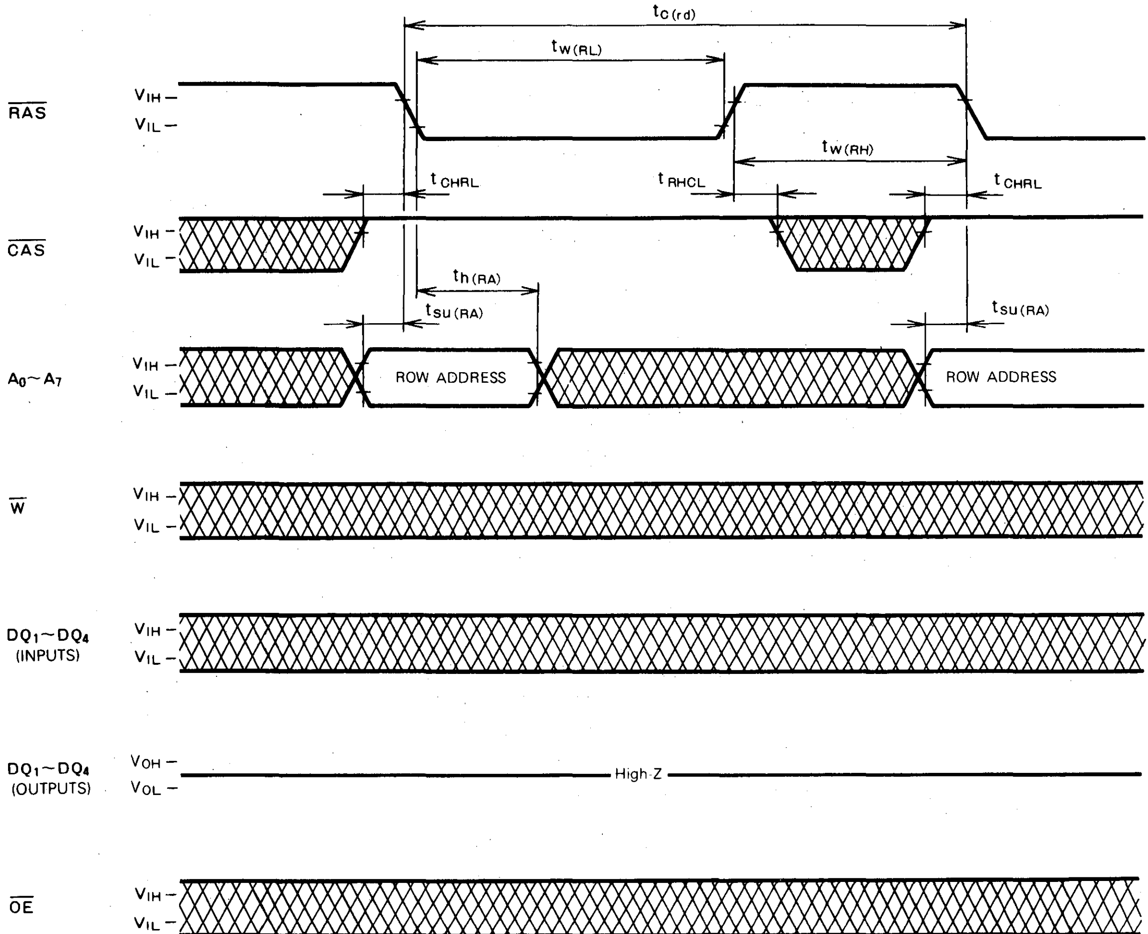


MITSUBISHI ELECTRIC

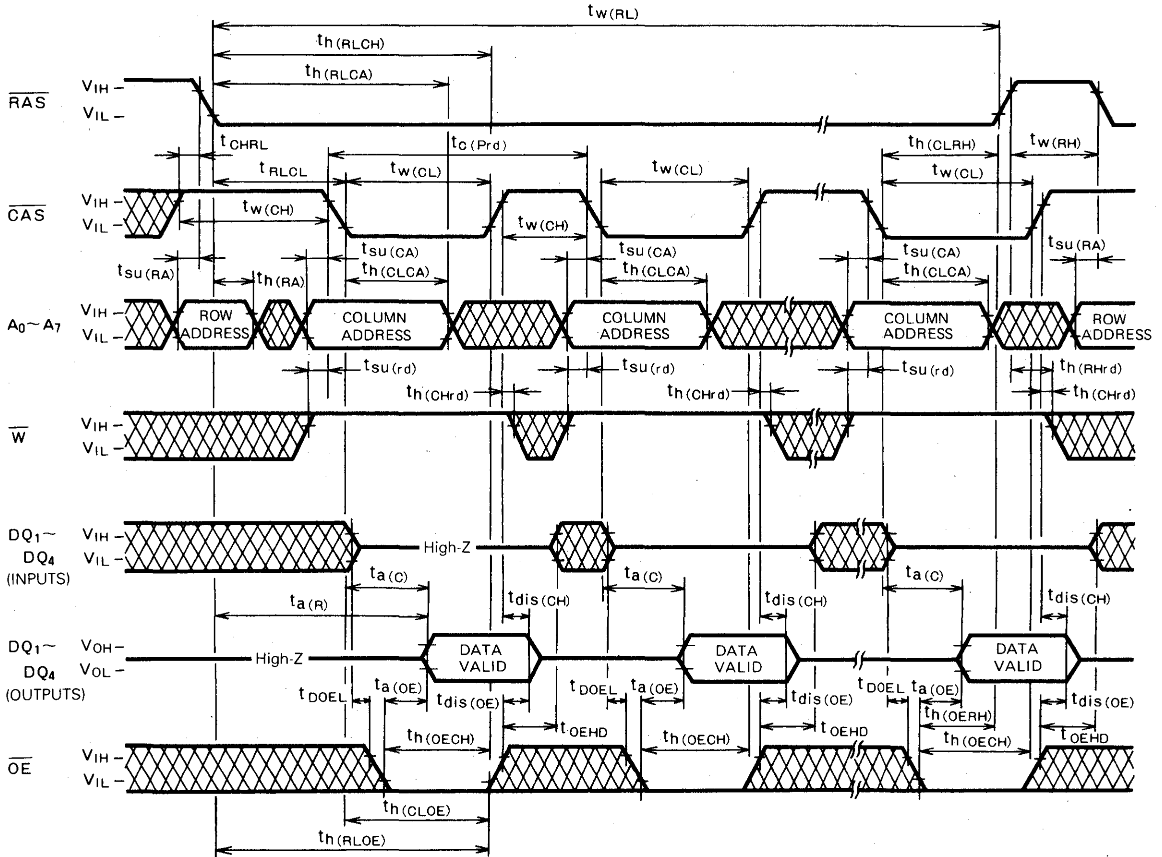
Read-Write and Read-Modify-Write Cycles



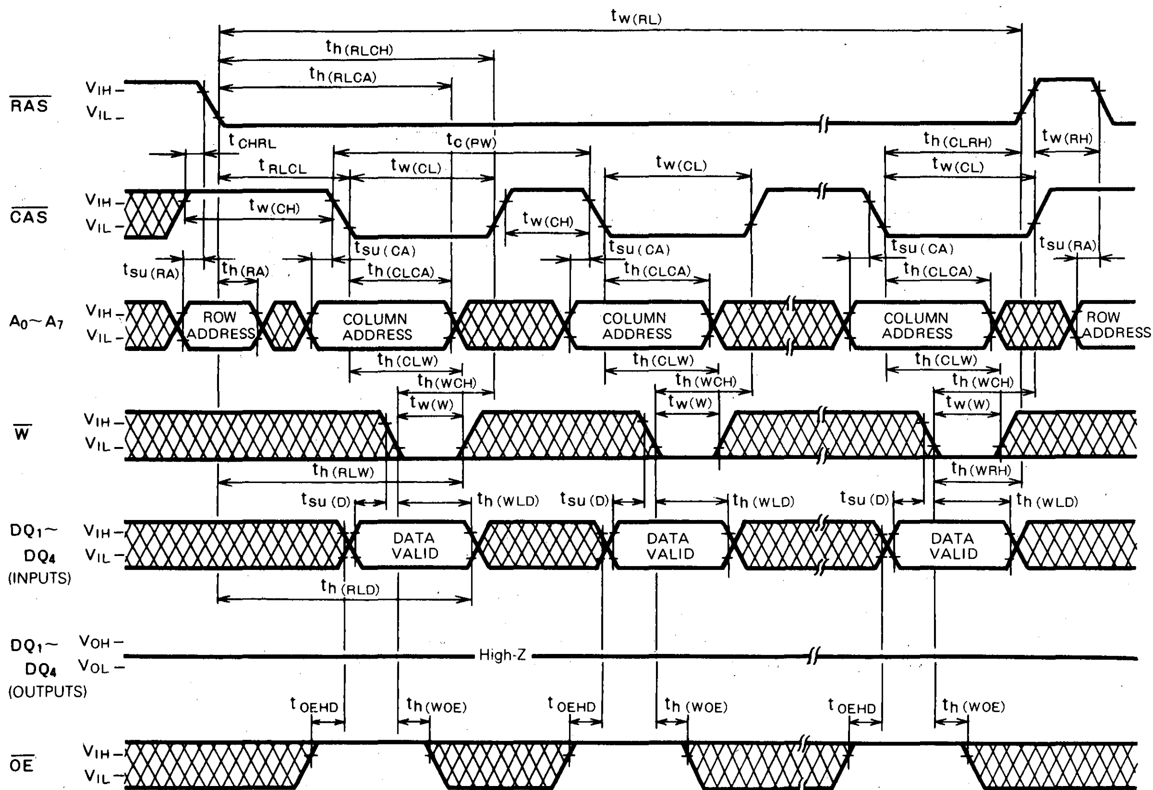
$\overline{RAS}$-Only Refresh Cycle



Page-Mode Read Cycle



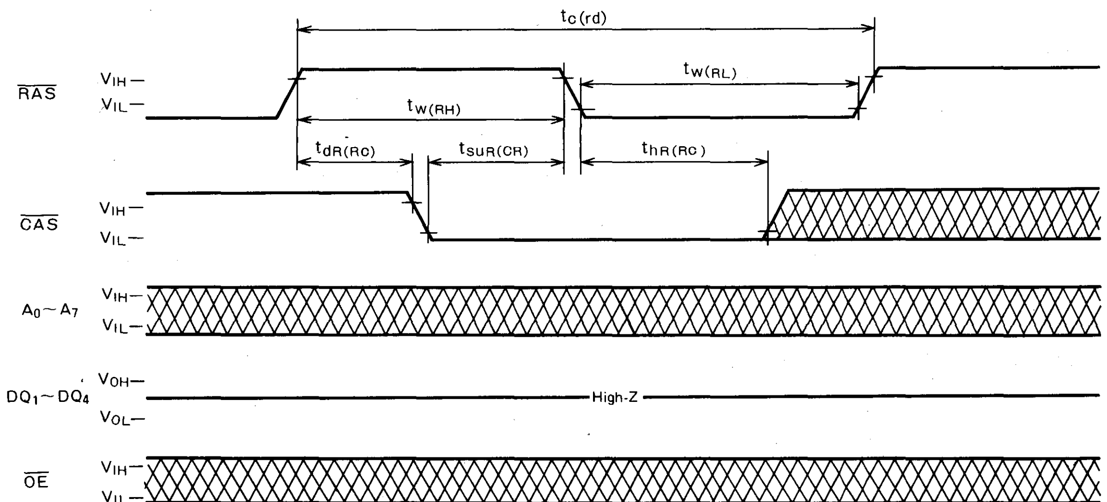
Page-Mode Write Cycle



Hidden Refresh Cycle

READ CYCLE
HIDDEN REFRESH CYCLE
$t_{c(rd)}$
$t_{w(RL)}$
$t_{w(RH)}$
$\overline{RAS}$ V_{IH} – V_{IL} –
t_{CHRL}
$t_{h(CLRH)}$
t_{RLCL}
$\overline{CAS}$ V_{IH} – V_{IL} –
$t_{w(CH)}$
$t_{su(RA)}$
$t_{su(CA)}$
$t_{h(CLCA)}$
$t_{h(RA)}$
$A_0 \sim A_7$ V_{IH} – V_{IL} –
ROW ADD-RESS
COLUMN ADDRESS
ROW ADDRESS
$t_{h(RHrd)}$
$t_{su(rd)}$
$\overline{W}$ V_{IH} – V_{IL} –
$DQ_1 \sim DQ_4$ (INPUTS) V_{IH} – V_{IL} –
High-Z
$t_{a(C)}$
$t_{a(R)}$
$t_{dis(CH)}$
$DQ_1 \sim DQ_4$ (OUTPUTS) V_{OH} – V_{OL} –
High-Z
t_{DOEL}
$t_{a(OE)}$
$t_{dis(OE)}$
$t_{h(OERH)}$
t_{OEHD}
$\overline{OE}$ V_{IH} – V_{IL} –

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



M5M4464L-10, -12, -15

262144-BIT (65536-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65536-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 20 pin Zig-Zag In-Line package configuration and an increase in system densities. The M5M4464L operates on a 5V power supply using the on chip substrate bias generator.

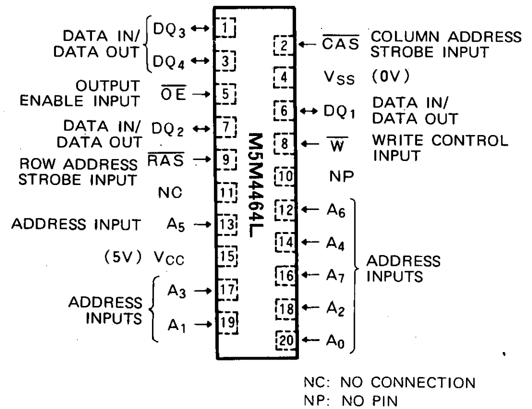
FEATURES

- Performance ranges

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4464L-10	100	200	300
M5M4464L-12	120	220	260
M5M4464L-15	150	260	230

- 65536 x 4 Organization
- Industry standard 20 pin Zig-Zag in line package
- Single 5V ±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4464L-10 420mW (max)
  - M5M4464L-12 360mW (max)
  - M5M4464L-15 330mW (max)

PIN CONFIGURATION (TOP VIEW)



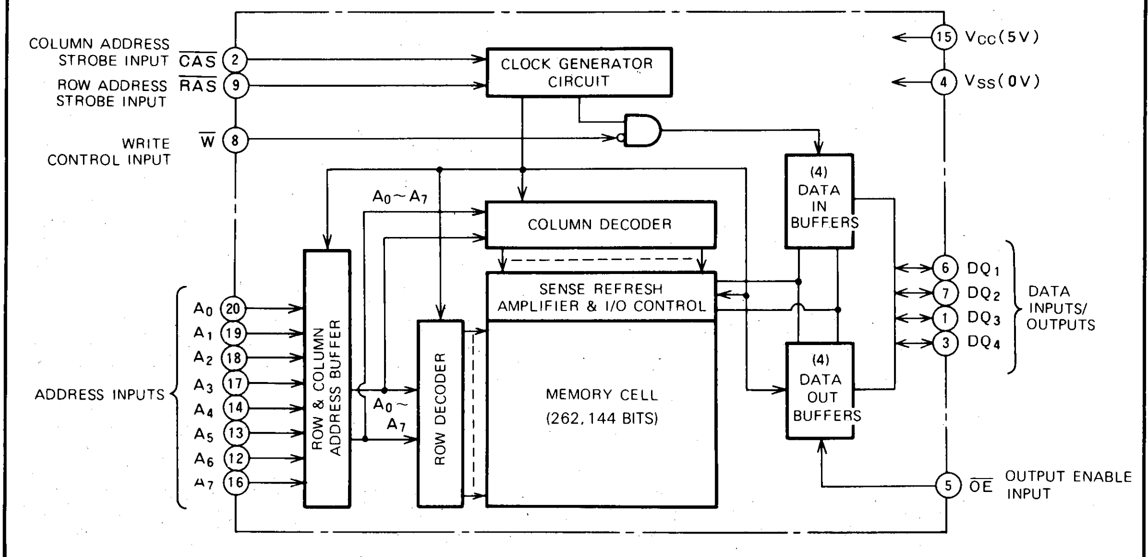
Outline 20P5L

- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 256 refresh cycles/4ms
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30μs max

APPLICATION

Refresh memory for CRT, Micro computer memory

BLOCK DIAGRAM



FUNCTION

The M5M4464L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column adress	Input DQ	Output DQ		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Page mode identical
Write (Early Write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only retfesh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262144 memory cells in the M5M4464L the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to CAS $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OEHD}.

output enable ($\overline{\text{OE}}$)

The $\overline{\text{OE}}$ controls the impedance of the output buffers. When $\overline{\text{OE}}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{\text{OE}}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{\text{OE}}$ or $\overline{\text{CAS}}$ is brought high.

Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{\text{RAS}}$, because once the row address has been strobed, $\overline{\text{RAS}}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4464L must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4464L are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{\text{RAS}}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{\text{RAS}}$ Only Refresh

In this refresh method, the $\overline{\text{CAS}}$ clock should be at a V_{IH} level and the system must perform $\overline{\text{RAS}}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{\text{RAS}}$ clock and associated internal row locations are refreshed. A $\overline{\text{RAS}}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh

If $\overline{\text{CAS}}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{\text{RAS}}$ and if $\overline{\text{CAS}}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{\text{RAS}}$ falls, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{\text{CAS}}$ is kept low after the above operation, $\overline{\text{RAS}}$ cycle initiates $\overline{\text{RAS}}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{\text{RAS}}$ high and then low while $\overline{\text{CAS}}$ remains high initiates the normal $\overline{\text{RAS}}$ Only Refresh using the external address.

If $\overline{\text{CAS}}$ is kept low after the normal read/write cycle, $\overline{\text{RAS}}$ cycle initiates the $\overline{\text{RAS}}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available until $\overline{\text{CAS}}$ is brought high.

4. Hidden Refresh

A feature of the M5M4464L is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{\text{CAS}}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period, executing a $\overline{\text{RAS}}$-only cycling, but with $\overline{\text{CAS}}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{\text{CAS}}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4464L is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are decoded and applied to the M5M4464P as chip-select in the memory system, but if $\overline{\text{RAS}}$ is decoded, all unselected devices go into stand-by independent of the $\overline{\text{CAS}}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4464L operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

262144-BIT(65536-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	Condtions	Ratings	Unit
V_{CC}	Supply volrage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, All other pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{cc}, operating (Note 3,4)	M5M4464L-10	$\overline{RAS}$, $\overline{CAS}$ cycling tc(rd)=tc(w) = min output open			75	mA
		M5M4464L-12				65	
		M5M4464L-15				60	
I_{CC2}	Supply current from V_{cc}, standby		$\overline{RAS}$=V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{cc}, retreshing (Note 3)	M5M4464L-10	$\overline{RAS}$ cycling $\overline{CAS}$=V_{IH} tc(Prd) = min, output open			60	mA
		M5M4464L-12				55	
		M5M4464L-15				50	
$I_{CC4(AV)}$	Average supply current from V_{cc}, page mode (Note 3,4)	M5M4464L-10	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling tc(Prd) = min, output open			55	mA
		M5M4464L-12				50	
		M5M4464L-15				45	
$I_{CC6(AV)}$	Average supply current from V_{cc}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4464L-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tc(RAS)= min, output open			65	mA
		M5M4464L-12				60	
		M5M4464L-15				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_i=25mVrms			5	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				10	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464L-10		M5M4464L-12		M5M4464L-15		
				Min	Max	Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,7)	t_{CAC}		50		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,8)	t_{RAC}		100		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	—		25		30		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 9)	t_{OFF}	0	25	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 9)	—	0	25	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RLCL} \geq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If t_{RLCL} is greater than t_{RLCL} max then $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464L-10		M5M4464L-12		M5M4464L-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(RF)}$	Refresh cycle time		t_{REF}		4		4		4	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	90		90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	50	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	10		10		10		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	70		80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	3	50	ns

Note 10: The timing requirements are assumed t_T=5ns.
11: V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; if t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. if t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

Read and Refresh Cycles

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4464L-10		M5M4464L-12		M5M4464L-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time		t_{RC}	200		220		260		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	50	100000	60	100000	75	100000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		35		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	50		60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	(Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	(Note 15)	t_{RRH}	10		10		10		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		—	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		—	25		30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		25		30		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		—	0		0		0		ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464L-10		M5M4464L-12		M5M4464L-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(W)}$	Write cycle time	t_{RC}	200		220		260		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50	100000	60	100000	75	100000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		35		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	50		60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		−5		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	35		40		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	85		100		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	35		40		45		ns
$t_{W(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	35		40		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		90		110		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after Write low	—	25		25		30		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464L-10		M5M4464L-12		M5M4464L-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(rdW)}$	Read write/read modify write cycle time (Note 16)	t_{RWC}	270		295		345		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	170	10000	195	10000	235	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	120	100000	135	100000	160	100000	ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	170		195		235		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	120		135		160		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	30		30		35		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	35		40		45		ns
$t_{W(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	35		40		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	—	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	25		25		30		ns

Note 16: $t_{C(rdW)}$ is specified as $t_{C(rdW)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{W(RH)}$ min + 4 t_T.

Page-Mode Cycle (Note 17)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464L-10		M5M4464L-12		M5M4464L-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	100		120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	100		120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 18)	t_{RAS}	200	30000	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read write/read modify write cycle time	—	170		195		230		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	340	30000	390	30000	465	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		50		60		ns

Note 17: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
18: Specified for read or write cycle.
19: Specified for read-write or read-modify-write cycle.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4464L-10		M5M4464L-12		M5M4464L-15		
			Min	Max	Min	Max	Min	Max	
$t_{SU\,R(CR)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	10		10		10		ns
$t_{h\,R(RC)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	20		25		30		ns
$t_{d\,R(RC)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

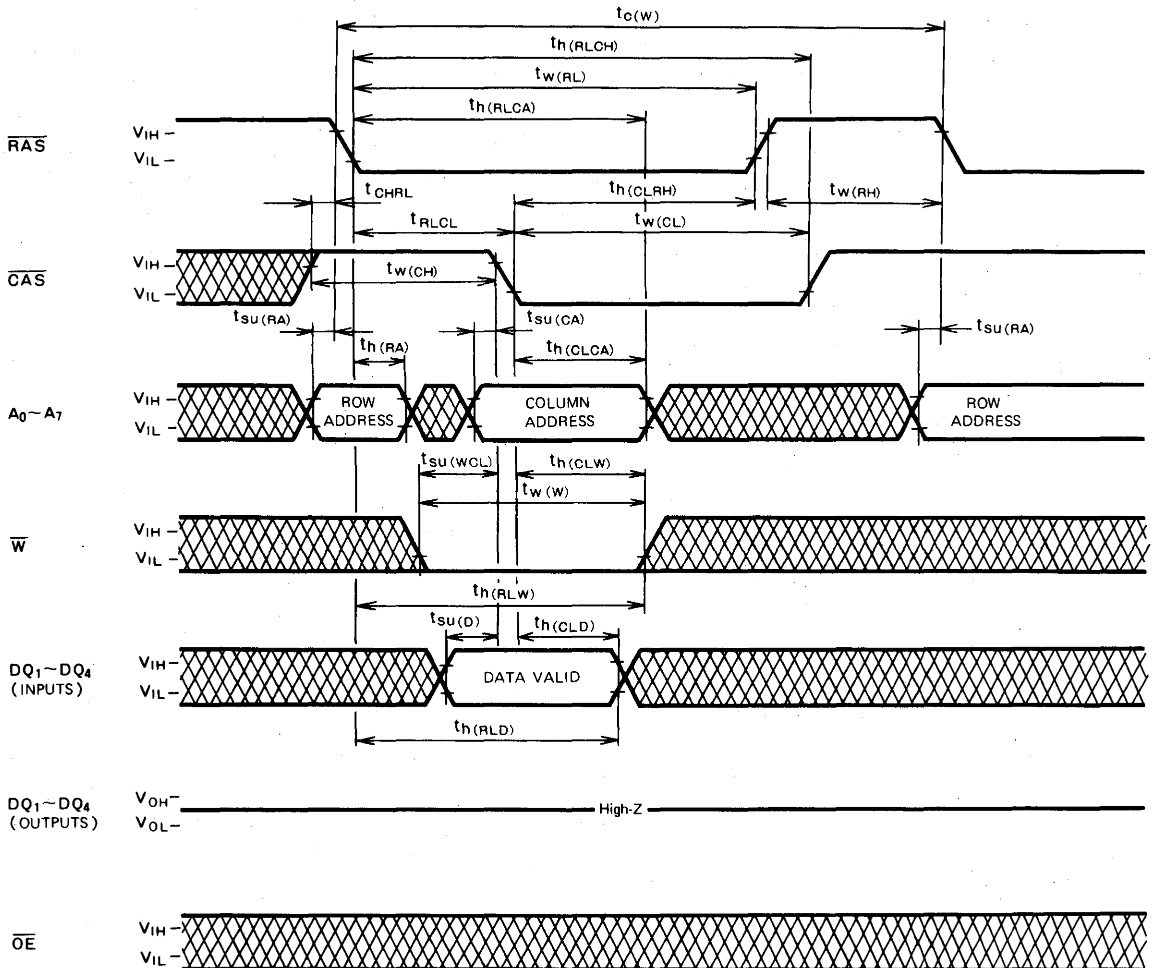
Note 20: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 21)

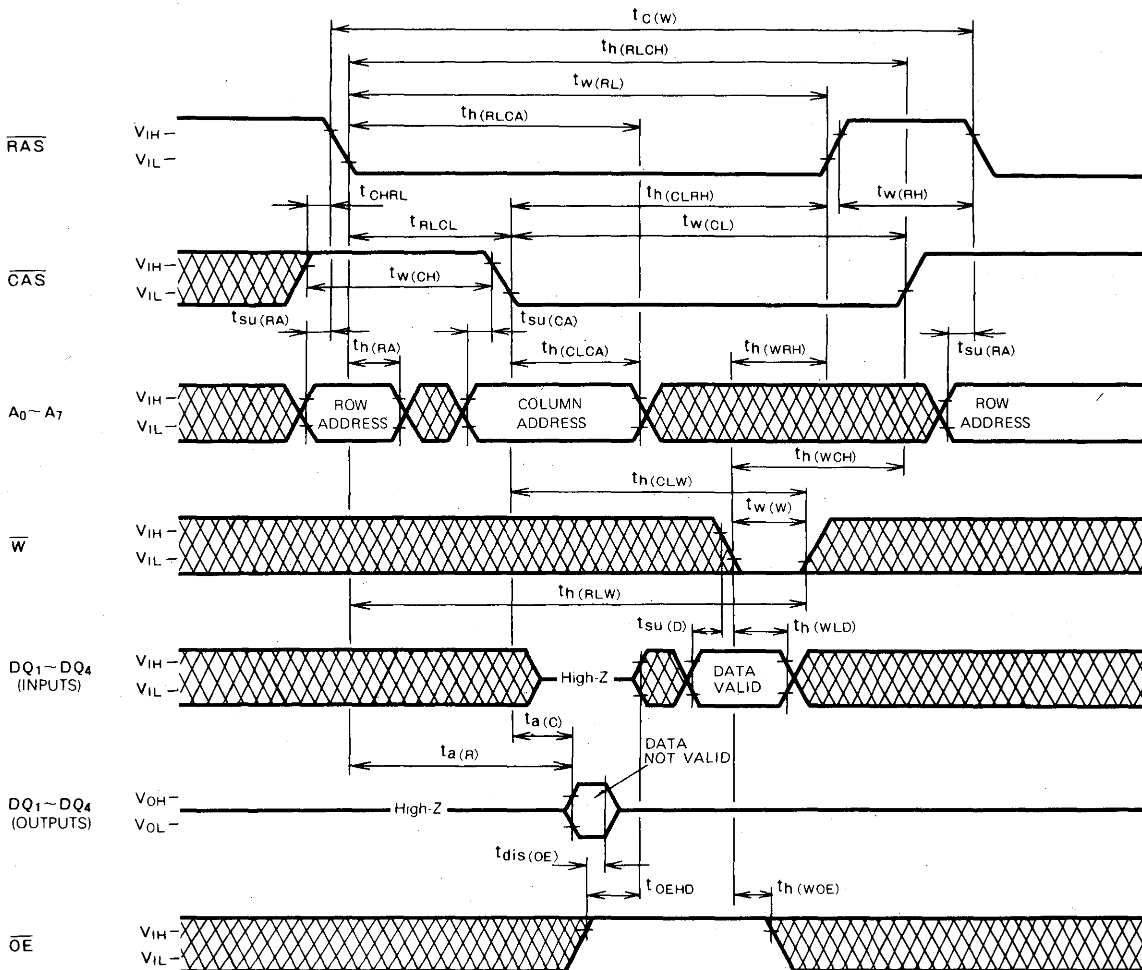
Read Cycle

Note 21. Indicates the don't care input.

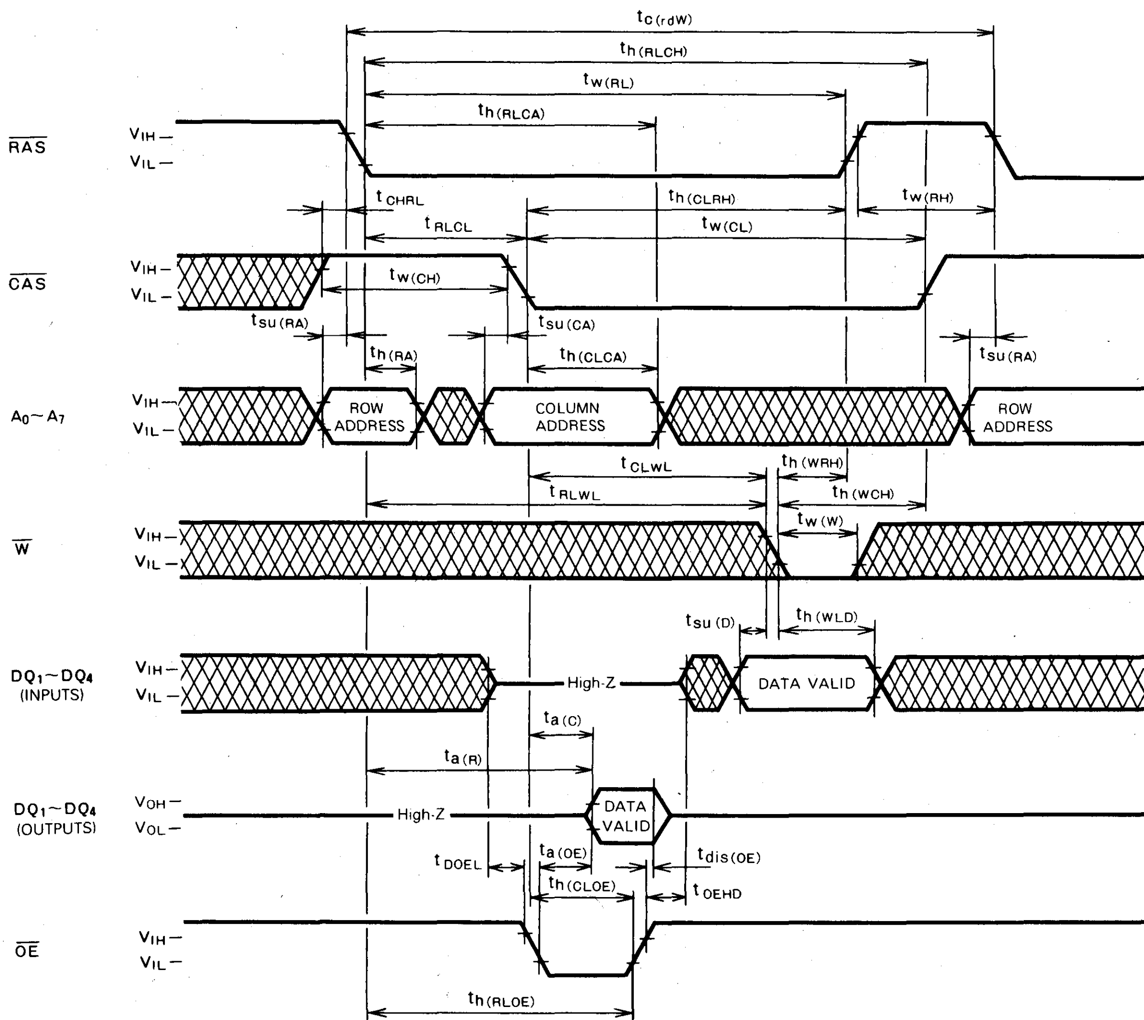
Write Cycle (Early Write)



Write Cycle (Delayed Write)

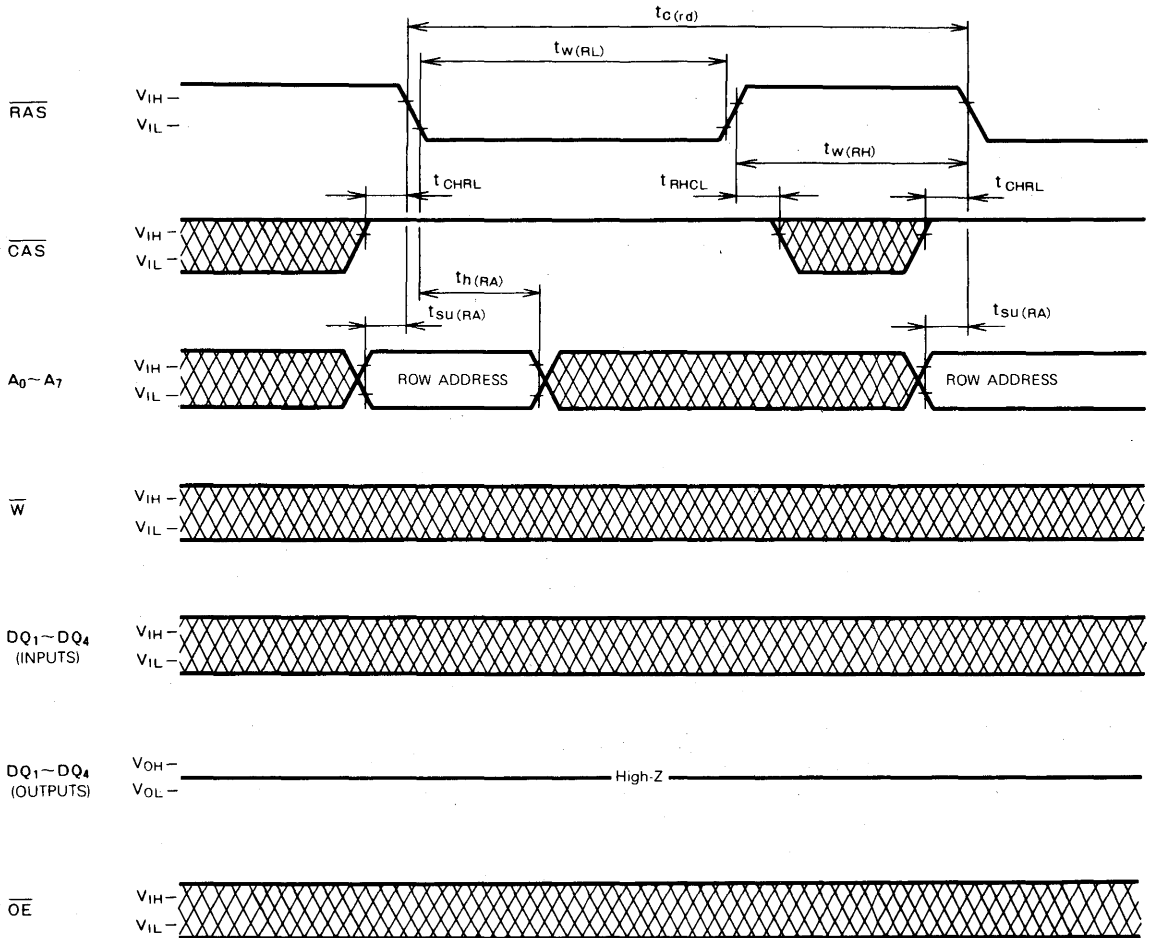


Read-Write and Read-Modify-Write Cycles

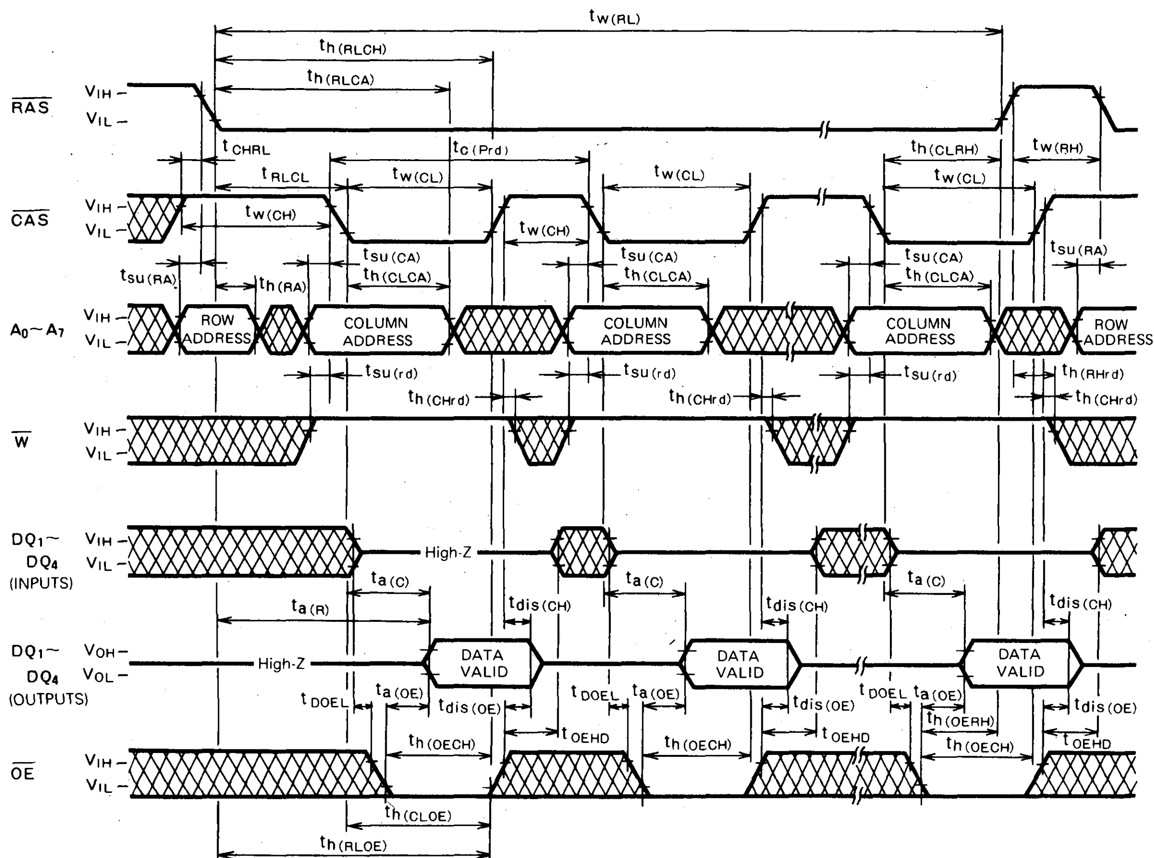


MITSUBISHI ELECTRIC

$\overline{RAS}$-Only Refresh Cycle

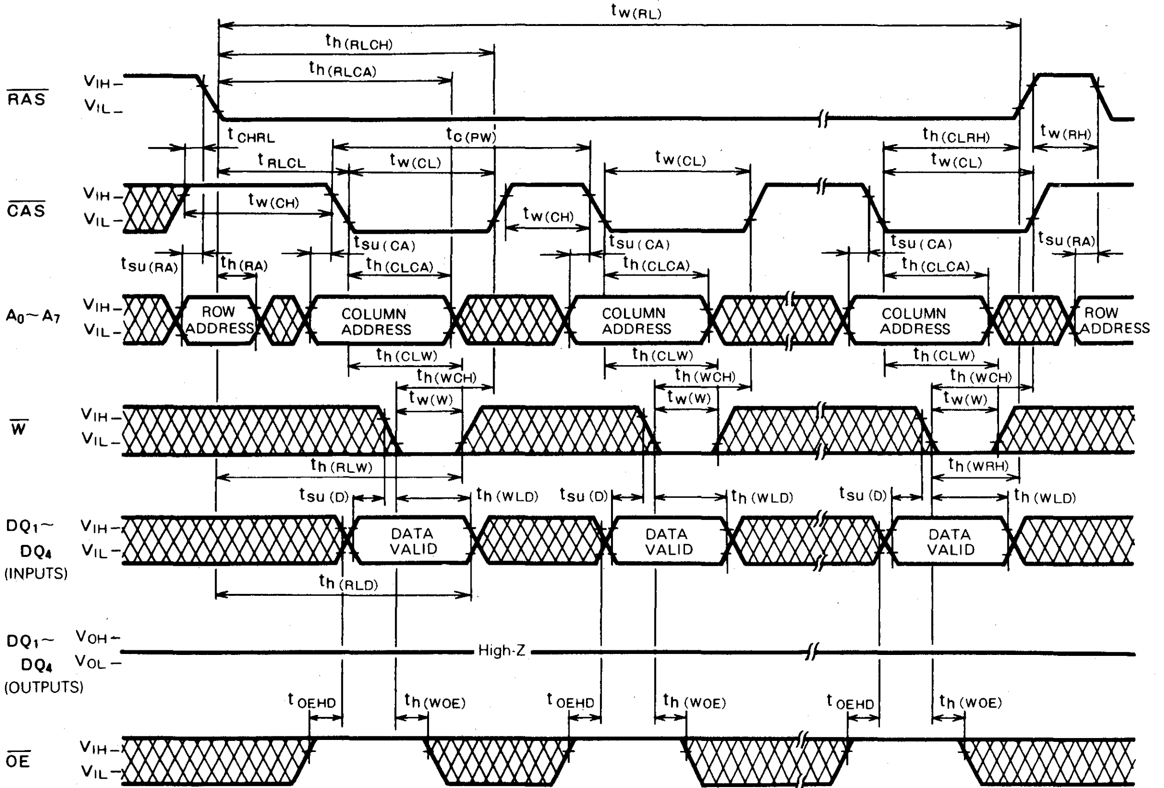


Page-Mode Read Cycle



MITSUBISHI ELECTRIC

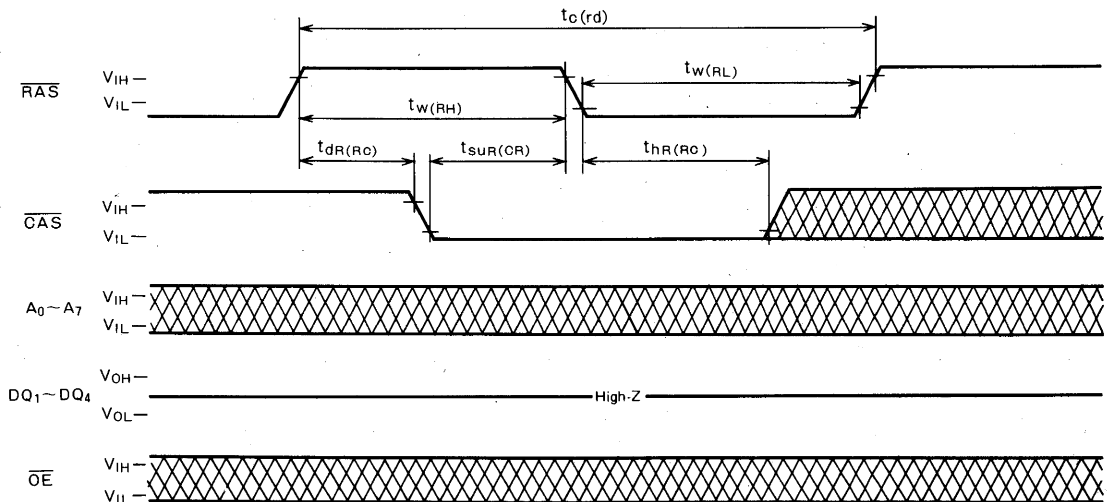
Page-Mode Write Cycle



Hidden Refresh Cycle

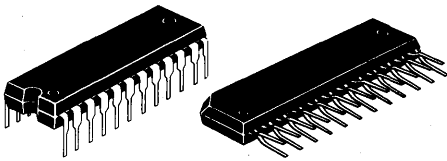
READ CYCLE
HIDDEN REFRESH CYCLE
$t_{c(rd)}$
$t_{w(RL)}$
$t_{w(RH)}$
t_{CHRL}
$t_{h(CLRH)}$
t_{RLCL}
$t_{w(CH)}$
$t_{su(RA)}$
$t_{su(CA)}$
$t_{h(CLCA)}$
$t_{h(RA)}$
$t_{su(rd)}$
$t_{h(RHrd)}$
$t_{a(C)}$
$t_{a(R)}$
$t_{dis(CH)}$
$t_{dis(OE)}$
t_{DOEL}
$t_{a(OE)}$
$t_{h(OERH)}$
t_{OEHD}
RAS
CAS
$A_0 \sim A_7$
ROW ADDRESS
COLUMN ADDRESS
W
$DQ_1 \sim DQ_4$ (INPUTS)
$DQ_1 \sim DQ_4$ (OUTPUTS)
OE
V_{IH}
V_{IL}
V_{OH}
V_{OL}
High-Z

CAS before RAS Refresh Cycle



M5M4C264P-12, -15/ M5M4C264L-12, -15

262144-BIT DUAL-PORT DYNAMIC RAM



DESCRIPTION

The Mitsubishi M5M4C264P,L is a high speed 262,144 bit Dual Port Dynamic Memory equipped with a 64K x 4 Dynamic RAM Port and a 256 x 4 Serial Read/Write Port. The use of N-well CMOS Process combined with silicide technology and a single transistor dynamic storage cell provide high circuit density and low power dissipation.

The Serial Read/Write Port is connected to an internal 1024 bit Data Register through a 256 x 4 Serial Input/Output Control and is serially read out or written in with a clock rate of up to 25MHz.

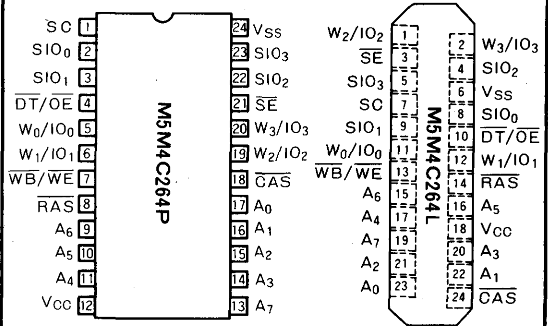
All reads and writes are done relative to the RAM Array, thus Data transfer from the RAM array to the Data Register is referred to as Read Transfer, while Data Transfer from the Data Register to the RAM array is referred to as Write Transfer.

FEATURES

Type name	RAS Access Time	Random Read/Write Cycle Time	Serial Read/Write Cycle Time	Random Read/Write VCC Supply Current	Serial Read/Write VCC Supply Current
M5M4C264P-12 M5M4C264L-12	120ns	220ns	40ns	60mA	40mA
M5M4C264P-15 M5M4C264L-15	150ns	260ns	60ns	50mA	30mA

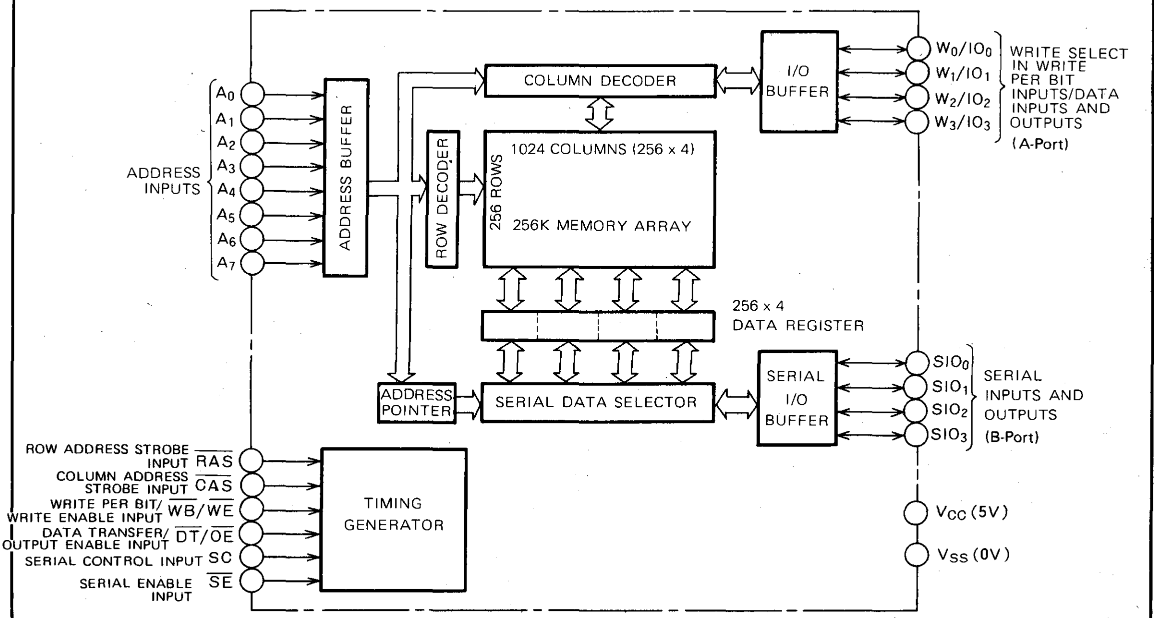
- Dual Port Architecture
  - RAM Port: 64K word x 4 bit
    - Access Time .... 120ns (MAX)
  - Serial Read/Write Port: 256 word x 4 bit
    - Access Time .... 40ns (MAX)
- Bidirectional Data Transfer function between the RAM array and the Data Register.
- Fully Asynchronous Dual Port Accessability (except during the Data Transfer Period.)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function.
- Real Time Data Transfer from the RAM Array to the Data Register.
- Page Mode, Hidden Refresh and CAS before RAS Refresh.
- 256 cycles/4ms Refresh.
- Fully TTL Compatible.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4F (M5M4C264P) Outline 24P5L (M5M4C264L)

BLOCK DIAGRAM



- 24 Pin, 400 mil DIP.
  (M5M4C264P)/24Pin, ZIP(M5M4C264L)
- N-well CMOS Process & Low Power dissipation
  RAM & SAM Active (-12/-15) . . . . . 100/80mA max
  RAM & SAM Standby (-12/-15) . . . . . . 5/5mA max

APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VTR, Videotex, Teletext, Video printer, High Speed data transmission systems.

PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address (A0-A7) and selects the word line. It also selects the write-per-bit, the data transfer and the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address (A8-A15) and reads or writes the selected words. In the data transfer cycle, it becomes the SAM start address.
$A_0 \sim A_7$	ADDRESS INPUT	The M5M4C264P is an address multiplex method for inputting the row addresses and column addresses separately, in order to select one word from the 64K word memory cells. The various addresses are latched by the $\overline{RAS}/\overline{CAS}$ falling edge. In the data transfer cycle, this address input is also combined with the serial access start address.
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT/ WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level in the $\overline{RAS}$ clock falling edge is "L", the write-per-bit or write transfer cycle is selected, and when it is "H", a 4 bit write to the $\overline{RAM}$ or a read transfer cycle from the $\overline{RAM}$ is selected.
$\overline{DT}/\overline{OE}$	DATA TRANSFER OUTPUT ENABLE INPUT	In the RAM read cycle, it makes the data output into enable. Also, when the $\overline{DT}/\overline{OE}$ level in the $\overline{RAS}$ clock falling edge is "L", the data transfer cycle is selected, and when it is "H", the read/write cycle is selected.
$W_0 \sim W_3$/ $IO_0 \sim IO_3$	WRITE-PER-BIT SELECTION INPUT/ DATA INPUT/OUTPUT	These are the data input/output pins to the RAM. During the write-per-bit cycle in the $\overline{RAS}$ clock falling edge, the "H" pin is enable and the selected bit-only-write is performed. Also, in the write cycle, the data in the late falling edge, whether it is $\overline{CAS}$ or $\overline{WE}$, is latched.
SC	SERIAL CONTROL INPUT	The serial access is started from the SC clock rising edge. In the serial read cycle the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
$SIO_0 \sim SIO_3$	SERIAL INPUT/ OUTPUT	256 x 4 word serial data input/output pins.
$\overline{SE}$	SERIAL ENABLE INPUT	This makes serial input/output into enable. In the $\overline{RAS}$ clock falling edge, when $\overline{SE}$ is "H", it is a pseudo transfer, and when it is "L". It is a write transfer.

NB: SAM: Serial Access Memory

FUNCTION

RAM Port Operation

The row/column addresses are specified by the $\overline{RAS}/\overline{CAS}$ clocks.

The RAM read/write cycle is set up by maintaining the $\overline{DT}/\overline{OE}$ at "H" level, while the $\overline{RAS}$ clock is falling. In addition, the column address is specified while the $\overline{RAS}$ clock is held at "L" level and goes into page mode when the $\overline{CAS}$ clock is activated, and then the column datas in one row can be read/written continually.

1. Random Read Cycle

Data is read out when $\overline{DT}/\overline{OE}$ is a "L" level.

2. Random Write Cycle

Data is written in when $\overline{WB}/\overline{WE}$ is a "L" level.

When the $\overline{WE}$ clock is input before the $\overline{CAS}$ clock, it becomes an early write cycle, and the data from the $\overline{CAS}$ clock falling, is written in the RAM.

When the $\overline{WE}$ clock is input after the $\overline{CAS}$ clock, it becomes a late write cycle and the data from the $\overline{WE}$ clock falling is written in the RAM.

The read-modify-write cycle modifies the data which has been read and writes it in again. This time also, the $\overline{OE}$, $\overline{WE}$ clock controls the reading/writing of data.

In this random write cycle, the write-per-bit function (Note 1) is available.

SAM Port Operation

At the falling edge of the RAS clock, the data transfer cycle is set up by maintaining the DT/OE at "L" level. At such a time, the transfer cycle is the read transfer when the WB/WE clock is "H" level, and the write transfer when it is "L" level.

In the transfer cycle, the row address sets up the RAM row and the column address becomes the serial access start address.

- DT/OE signal can be used to select RAM or SAM independent mode (DT = "H") and between RAM and SAM data transfer mode (DT = "L").
- Within one transfer cycle, transfer of data (256 x 4 bits) is possible between any rows in the RAM and SAM.
- WE signal permits the designation of transfer direction. (WE = "H": RAM → SAM (read transfer)/WE = "L": SAM → RAM (write transfer))
- During read transfer, high-speed transfer execution is started at DT/OE leading edge. (Note 2)
- Transfer cycle allows the selection of SAM I/O mode.
- In write transfer mode, SE control allows the transfer execution to be inhibited. (pseudo write transfer) (Note 3)
- ROW address in transfer cycle permits the transfer page of RAM.
- Column address in transfer cycle is specified the read (write) start address of SAM after transfer.

Memory Refresh Operation

The M5M4C264 consists of dynamic RAMs memory cells so a refresh operation is required every 4m seconds.

The refresh operation consists of reading the data from the memory, amplifying it in the sense amp and then rewriting it. With the M5M4C264, all the memory cells are refreshed by performing a refresh operation on all 256 row addresses which are designated by the 8 bits.

1. RAS Only Refresh

When the row address is input while the CAS clock is held at "H" level, and the RAS clock is activated, all the column data in the designated row address are refreshed simultaneously.

2. CAS-Before-RAS Refresh

When the CAS clock is activated before the RAS clock, the designated row address, which is generated by the internal 8 bit refresh counter, is refreshed. The built-in refresh counter is incremented with every refresh cycle. Then all the memory cells are refreshed by repeating the CAS-before-RAS refresh cycle 256 times.

3. Hidden Refresh

The memory cells are refreshed by the 8 bit refresh counter built into the chip, in the same way as the CAS-before-RAS refresh, by activating the RAS clock while the CAS, OE clocks are being held at "L" level after the previous read cycle. At this time, the data which was read into the previous cycle is held in the output.

SAM READ OUT/WRITE IN

In the same way as a shift register, SAM inputs and outputs data simultaneously with the SC clock rise. SE is used to control the data inputs/outputs.

RAM and SAM are connected to each other by 1024 data buses, and the data from RAM can be transferred to SAM and the data from SAM can be transferred to RAM.

1. SERIAL READ TRANSFER CYCLE (RAM→SAM TRANSFER)

When the RAS clock is falling, the serial read transfer mode is selected and at the same time the row address indicates the row for transfer from RAM to SAM and the data are read out. When the column address is input and the DT signal is "H", the one row data read out from RAM is transferred to the data register. At the same time as this, the decoded column address is set to the serial selector and the serial read start address is determined. (pointer control) After this, every time the SC clock goes from "L" to "H", the data is output to the serial port and the selector moves onto the next bit. For the serial selector to be cyclic, when the SC clock is input more than 257 times, the same data from the start address mentioned above is output again. SE clock controls the serial output buffer. When SE is "L", the data register contents are output to the SIO pins and when SE is "H", the SIO pins are at high impedance. The serial selector has no relation with the SE level and shifts one bit every time the SC clock is input. Serial read transfer can be done when SAM is in operation and also, data from different rows can be continuously output. (real time transfer)

A horizontal scroll can easily be realized with the pointer control function which is utilized to indicate the arbitrary address.

The memory can be effectively used with the real time transfer function which is utilized to scan multiple lines horizontally.

2. SERIAL WRITE TRANSFER CYCLE (SAM→ RAM TRANSFER)

When the RAS clock is falling, the serial write transfer mode is selected and at the same time the row transferred from SAM is designated by the row address, in the same way as for the serial read transfer mode. When the column address is input and the DT signal is turned "H", the single row data which are read out from SAM is written into the row selected by RAM. At the same time as this, the decoded row address is set to the serial selector and the next serial write start address is determined. After this, every time the SC clock is input, the data which are input to SIO are written into SAM. SE controls the serial input buffer. It writes into the data register when the level is "L", and when the level is "H", it only shifts the serial selector without writing in the data.

3. PSEUDO WRITE TRANSFER CYCLE

This is the same as the write transfer cycle, except for the fact that data is not transferred from SAM to RAM. (The row address which is input is ignored.)

When the mode changes from serial read to serial write, this cycle is used so that the RAM data is not destroyed, and also for changing the mode of the serial port.

Different to serial read transfer, serial write transfer and pseudo write transfer cycles cannot be done while SAM is operating, and it cannot input data continuously to different rows.

Note 1: Write-Per-Bit Function

During the RAM operation, data is written to the specified terminals of the four I/O common terminals, while being inhibited at the others.

Write-Per-Bit mode is specified by $\overline{WB}$ (="L") at $\overline{RAS}$ falling edge.

Write terminals are specified by W/IO (Write = "H", Write inhibit = "L") at this time. Actual writing is then carried out by $\overline{WE}$ in the same manner as with the conventional DRAM.

Note 2: Real-time Data Transfer

Read transfer (RAM → SAM) is executed with $\overline{DT}$ leading timing in transfer cycle. In the SC clock input before this timing, the SAM contents before transfer are output, while the new SAM contents after read transfer are output in the SC clock input after this timing.

During read transfer, continuous SC clock is also applied, thus making it possible to continuously produce SAM output before read transfer and SAM output after transfer.

Note 3: Pseudo Write Transfer

In order to write data to SAM when it has been in the output mode it is necessary to change the SAM I/O common terminals (SIO) to the input mode using the write transfer mode. If write transfer is not desired, the pseudo write transfer mode should be used.

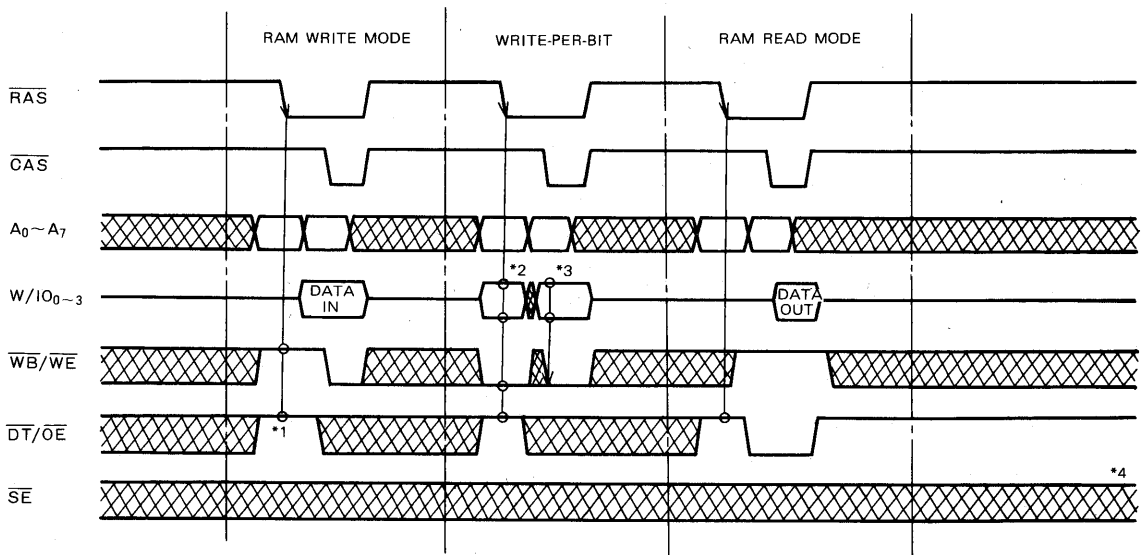
If $\overline{SE}$ is in "H" at $\overline{RAS}$ falling edge of write transfer mode is selected; thus, SAM I/O common terminals are set to the input mode, but SAM to RAM data transfer is not executed.

MODE SELECTION

Input pin state at $\overline{RAS}$ falling				RAM		SAM
$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	W/IO 0~3		Bit Mask	SIO 0~3
H	X	X	X	READ	—	—
H	H	X	X	WRITE	—	—
H	L	X	H	Write-Per-Bit	Non Masked	—
H	L	X	L	Write-Per-Bit	Masked	
L	H	X	X	RAM→SAM (read transfer)	—	Output mode
L	L	L	X	SAM→RAM (write transfer)	—	Input mode
L	L	H	X	Pseudo Write Transfer (No RAM contents will be changed)	—	Input mode

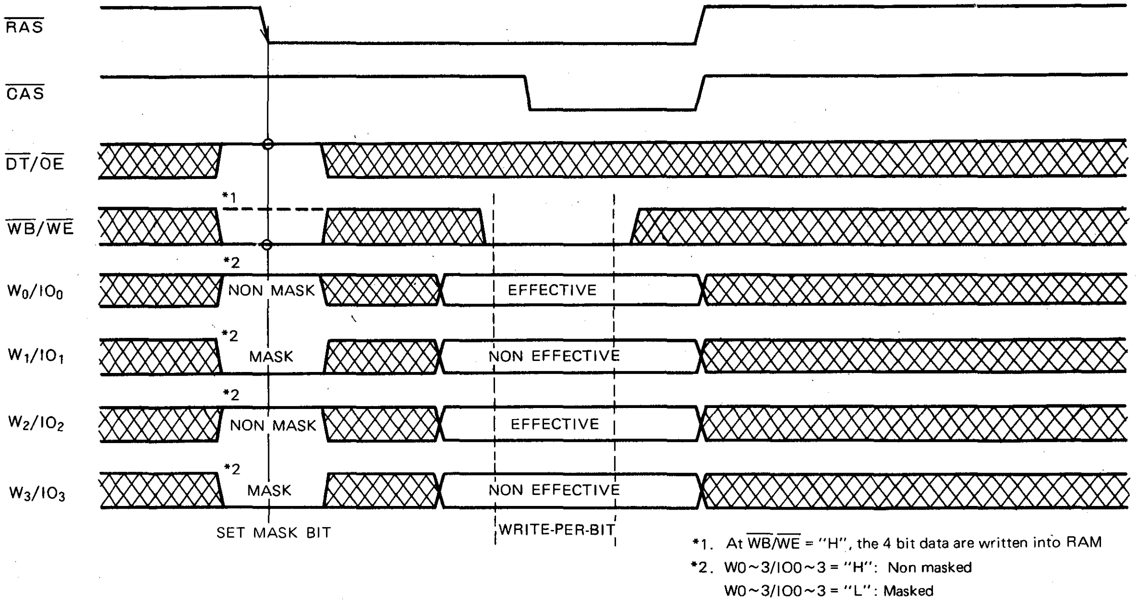
X: Not specified.

RAM Access Mode



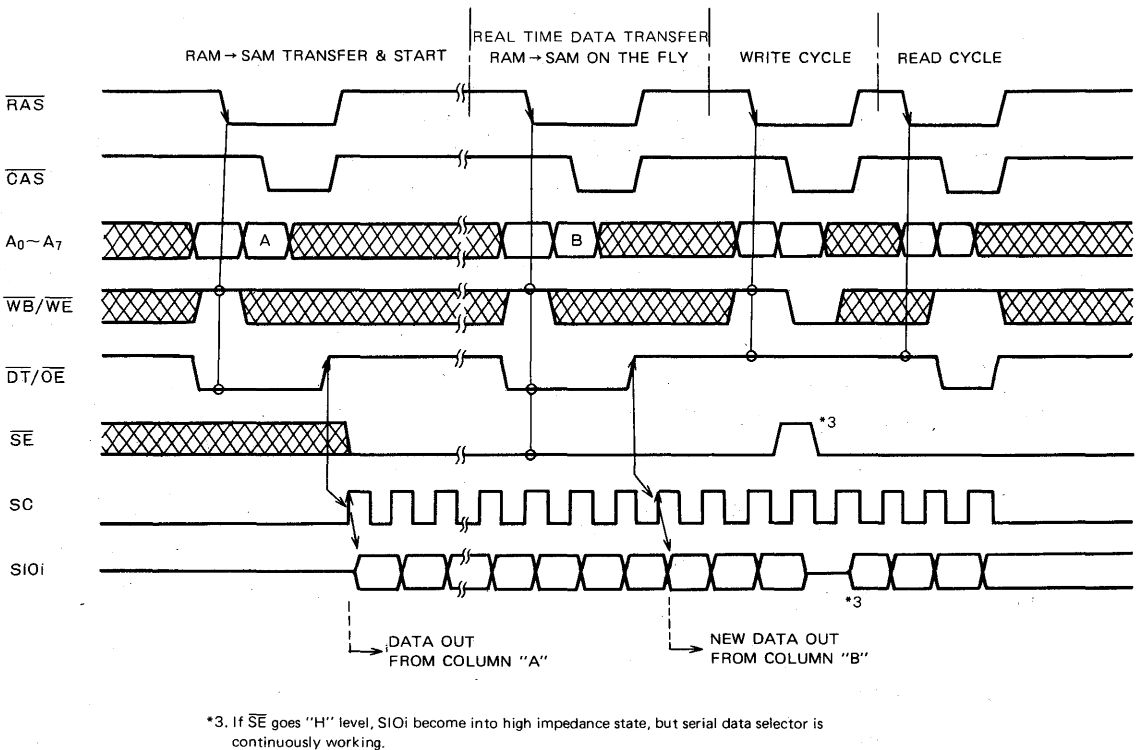
*1: Write 4bit data
*2: Set mask bit
*3: Write selected bit
*4: [hatched] Indicates the don't care input

Write-Per-Bit Operation



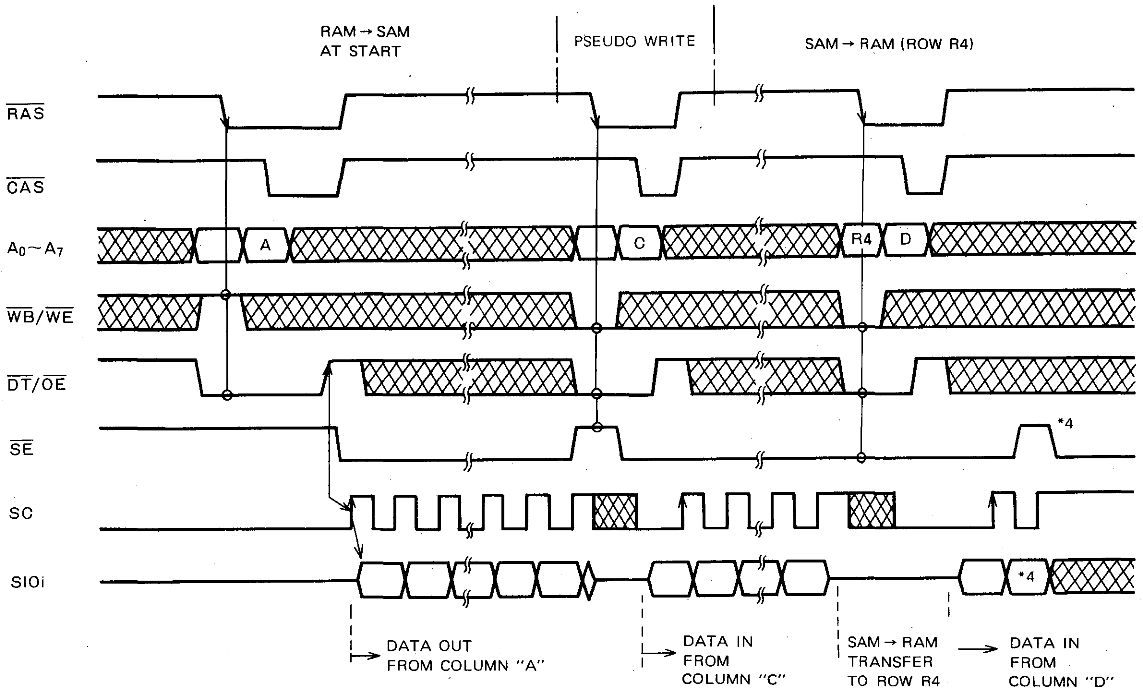
*1. At WB/WE = "H", the 4 bit data are written into RAM
*2. W0~3/IO0~3 = "H": Non masked
W0~3/IO0~3 = "L": Masked

Serial Output Mode



*3. If SE goes "H" level, SIOi become into high impedance state, but serial data selector is continuously working.

Serial Input Mode



*4. If $\overline{SE}$ goes "H" level, SIOi input data is ignored, but serial data selector is continuously working.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta = 25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage all inputs	2.4		$V_{CC}+1$	V
V_{IL}	Low-level input voltage all inputs	−1		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH} (R)	High-level output voltage (RAM Port).	$I_{OH}(R) = -2mA$	2.4		V_{CC}	V
V_{OL} (R)	Low-level output voltage (RAM Port)	$I_{OL}(R) = 4.2mA$	0		0.4	V
V_{OH} (S)	High-level output voltage (Serial I/O Port)	$I_{OH}(S) = -2mA$	2.4		V_{CC}	V
V_{OL} (S)	Low-level output voltage (Serial I/O Port)	$I_{OL}(S) = 4.2mA$	0		0.4	V
I_{OZ}	Off-state output current	Q floating $0V \leqq V_{out} \leqq 5.5V$	−10		10	μA
I_I	Input current	$0V \leqq V_{IN} \leqq V_{CC}$ Other input pins = 0V	−10		10	μA

Note 2: Current flowing into an IC is positive, out is negative

Symbol (Note 3)	Parameter		M5M4C264P, L		Unit
			-12	-15	
	RAM Port	Serial I/O Port	Max	Max	
$I_{CC1(AV)}$	Random R/W cycle ($\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = t_{RC}(min)$)	Standby ($SC = V_{IL}$)	60	50	mA
I_{CC2}	Standby ($\overline{RAS} = V_{IH}$, $Dout = H_{IZ}$) (Note 4)	Standby ($SC = V_{IL}$) (Note 4)	5	5	mA
$I_{CC3(AV)}$	RAS only refresh cycle ($\overline{RAS}$ cycling, $CAS = V_{IH}$, $t_{RC} = t_{RC}(min)$)	Standby ($SC = V_{IL}$)	50	40	mA
$I_{CC4(AV)}$	Page mode cycle ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}(min)$)	Standby ($SC = V_{IL}$)	40	35	mA
$I_{CC5(AV)}$	CAS before RAS refresh ($\overline{CAS}$ low as $\overline{RAS}$ falls, $t_{RC} = t_{RC}(min)$)	Standby ($SC = V_{IL}$)	50	40	mA
$I_{CC6(AV)}$	Data transfer cycle ($\overline{DT}$ low as $\overline{RAS}$ falls, $t_{RC} = t_{RC}(min)$)	Standby ($SC = V_{IL}$)	65	55	mA
$I_{CC7(AV)}$	Random R/W cycle ($\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = t_{RC}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	100	80	mA
$I_{CC8(AV)}$	Standby ($\overline{RAS} = V_{IH}$, $Dout = H_{IZ}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	40	30	mA
$I_{CC9(AV)}$	RAS only refresh cycle ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	90	70	mA
$I_{CC10(AV)}$	Page mode cycle ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	80	65	mA
$I_{CC11(AV)}$	CAS before RAS refresh ($\overline{CAS}$ low as $\overline{RAS}$ falls, $t_{RC} = t_{RC}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	90	70	mA
$I_{CC12(AV)}$	Data transfer cycle ($\overline{DT}$ low as $\overline{RAS}$ falls, $t_{RC} = t_{RC}(min)$)	Active ($t_{SCC} = t_{SCC}(min.)$)	105	85	mA

Note 3: $I_{CC(AV)}$ is obtained with the output open. (AV) specifies average value.
Note 4: If $V_{IH} \geqq V_{CC} \times 0.9$ and $V_{IL} \leqq 0.6V$, then $I_{CC2} \leqq 1.5$ mA. ($\overline{CAS}$, $\overline{SE}$ and $SIO_0 \sim SIO_3$ must be stable in high or low level.)

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$, $V_I = 25mVrms$)

Symbol	Parameter	Min	Max	Unit
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}/\overline{OE}$		8	pF
C_{IN1}	$A_0 \sim A_7$		5	pF
C_{IO0}	$W_0/IO_0 \sim W_3/IO_3$, $SIO_0 \sim SIO_3$		7	pF

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits				Unit
				M5M4C264P-12, L-12		M5M4C264P-15, L-15		
				Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,8)	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,9)	t_{RAC}		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	t_{OEA}		35		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 10)	t_{OFF}	0	30	0	40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 10)	t_{OEZ}	0	30	0	40	ns
$t_{a(SO)}$	Access time from SC high	(Note 7)	t_{SCA}		40		50	ns
$t_{a(SE)}$	Access time from $\overline{SE}$ low	(Note 7)	t_{SOA}		35		50	ns
$t_{dis(SE)}$	Output disable time after $\overline{SE}$ high	(Note 10)	t_{SOZ}	0	30	0	40	ns
$t_{h(SCHD)}$	Serial output hold time after SC high	(Note 7)	t_{SOH}	10		10		ns
t_{SOLD}	Delay time, $\overline{SE}$ low to serial setup	(Note 7)	t_{SOO}	5		5		ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Measured with a load circuit equivalent to 2TTL loads and 50pF.
8: Assume that $t_{RLCL} \geq t_{RLCL}$ max.
9: Assume that $t_{RLCL} < t_{RLCL}$ max. When t_{RLCL} is greater than t_{RLCL} max, $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
10: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 11)

Symbol	Parameter		Alternative Symbol	Limits				Unit
				M5M4C264P-12, L-12		M5M4C264P-15, L-15		
				Min	Max	Min	Max	
$t_{C(RF)}$	Refresh cycle time		t_{REF}		4		4	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	10		10		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	ns
$t_{su(WPB)}$	Write per bit mode setup time before $\overline{RAS}$ low		t_{WBS}	0		0		ns
$t_{h(WPB)}$	Write per bit mode hold time after $\overline{RAS}$ low		t_{WBH}	20		25		ns
$t_{su(W)}$	Write mask setup time before $\overline{RAS}$ low		t_{WS}	0		0		ns
$t_{h(W)}$	Write mask hold time after $\overline{RAS}$ low		t_{WH}	20		25		ns
$t_{su(DTH)}$	$\overline{DT}$ high setup time before $\overline{RAS}$ low		t_{DHS}	0		0		ns
$t_{h(DTH)}$	$\overline{DT}$ high hold time after $\overline{RAS}$ low		t_{DHH}	20		25		ns

Note 11: The timing requirements assume t_T=5ns.
V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; When t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. When t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. $= t_{h(RA)} + 2\,t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

For Read and Refresh Cycles

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4C264P-12, L-12		M5M4C264P-15, L-15		
			Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time	t_{RC}	220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60	10000	75	10000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (Note 15)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (Note 15)	t_{RRH}	20		20		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	—	30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	t_{OES}	30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	t_{COH}	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	t_{OED}	35		40		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		ns
t_{DCL}	Delay time, Data to $\overline{CAS}$ low	t_{DZC}		0		0	ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

For Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4C264P-12, L-12		M5M4C264P-15, L-15		
			Min	Max	Min	Max	
$t_{C(W)}$	Write cycle time	t_{RC}	220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60	10000	75	10000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low (Note 16)	t_{WCS}	0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	35		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	95		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after $\overline{WE}$ low	t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after $\overline{WE}$ low	t_{RWL}	40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low	t_{DH}	35		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	t_{OED}	35		40		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	30		40		ns

Note 16: When $t_{su(WCL)} \geq t_{su(WCL)}$ min, the cycle is an early write cycle and I/O pins will remain high impedance throughout the entire cycle. When $t_{CLWL} = t_{CLWL}$ min, and $t_{RLWL} \geq t_{RLWL}$ min, the cycle is a read-write cycle, and the data of the selected address will be read out on I/O pins. For all conditions other than those described above, the condition of data outputs (at access time and until $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ goes back to V_{IH}) is not defined.

For Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4C264P-12, L-12		M5M4C264P-15, L-15		
			Min	Max	Min	Max	
$t_{C(rdW)}$	Read modify write cycle time (Note 17)	t_{RWC}	295		345		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	195	10000	235	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	135	10000	160	10000	ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	195		235		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	135		160		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{WE}$ low (Note 16)	t_{CWD}	90		110		ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (Note 16)	t_{RWD}	150		185		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after $\overline{WE}$ low	t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after $\overline{WE}$ low	t_{RWL}	40		45		ns
$t_{W(W)}$	Write pulse width	t_{WP}	35		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low	t_{DH}	35		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	t_{COH}	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	t_{OED}	35		40		ns

Note 17: $t_{C(rdW)}$ is specified as $t_{C(rdW)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{W(RH)}$ min + 4 t_T.

For Page-Mode Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits				Unit
			M5M4C264P-12, L-12		M5M4C264P-15, L-15		
			Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read modify write cycle time	t_{RWC}	195		250		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 20)	t_{RAS}	390	30000	505	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	50		60		ns

Note 18: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19: Specified for read or write cycle.
20: Specified for read-modify-write cycle.

For $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Alternative Symbol	M5M4C264P-12, L-12		M5M4C264P-15, L-15		Unit
			Limits		Limits		
			Min	Max	Min	Max	
$t_{suR(CR)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	10		10		ns
$t_{hR(RC)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	25		30		ns
$t_{dR(RC)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		ns

Note 21: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

For Read/Write/Pseudo Write Transfer and Serial Read/Write Cycle

Symbol	Parameter	Alternate Symbol	Limits				Unit
			M5M4C264P-12, L-12		M5M4C264P-15, L-15		
			Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time	t_{RC}	220		260		ns
$t_{C(W)}$	Write cycle time	t_{RC}	220		260		ns
$t_{C(SC)}$	SC clock cycle time	t_{SCC}	40	50000	60	50000	ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	60	10000	75	10000	ns
$t_{W(RH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		ns
$t_{W(SCL)}$	SC low pulse width	t_{SCL}	10		20		ns
$t_{W(SCH)}$	SC high pulse width	t_{SCH}	15		20		ns
$t_{W(SEL)}$	$\overline{SE}$ low pulse width	t_{SOE}	10		20		ns
$t_{W(SEH)}$	$\overline{SE}$ high pulse width	t_{SOP}	10		20		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	60		75		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note 13)	t_{CRP}	10		10		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 12)	t_{RCD}	25	60	30	75	ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		20		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		25		ns
$t_{su(WE)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low	t_{WTS}	0		0		ns
$t_{h(WE)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low	t_{WTH}	20		25		ns
$t_{su(DT)}$	$\overline{DT}$ setup time before $\overline{RAS}$ low	t_{DLS}	0		0		ns
$t_{h(DT)}$	$\overline{DT}$ hold time after $\overline{RAS}$ low	t_{RDH}	90		130		ns
$t_{h(CLDT)}$	$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	40		55		ns
$t_{su(DTRH)}$	$\overline{DT}$ high setup time before $\overline{RAS}$ high	t_{DTR}	10		10		ns
$t_{h(DTRH)}$	$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		25		ns
$t_{su(DTCH)}$	$\overline{DT}$ high setup time before $\overline{CAS}$ high	t_{DTC}	10		10		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ES}	0		0		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low	t_{EH}	15		20		ns
$t_{su(SCDT)}$	SC low set up time before $\overline{DT}$ high	—	10		10		ns
$t_{h(DTSC)}$	SC high hold time after $\overline{DT}$ high	—		90		100	ns
$t_{h(SCDT)}$	SC low hold time after $\overline{DT}$ high	t_{SDH}	10		20		ns
$t_{su(SD)}$	Serial input data setup time before SC high	t_{SIS}	0		0		ns
$t_{h(SD)}$	Serial input data hold time after SC high	t_{SIH}	10		15		ns
t_{SHDH}	Delay time, SC high to $\overline{DT}$ high	t_{SDD}	20		25		ns
$t_{su(SCRL)}$	SC setup time before $\overline{RAS}$ low	t_{SRS}	20		30		ns
$t_{su(SEH)}$	$\overline{SE}$ disable setup time before SC high	t_{SWIS}	10		15		ns
$t_{h(SEH)}$	$\overline{SE}$ disable hold time after SC high	t_{SWIH}	20		30		ns
$t_{su(SEL)}$	$\overline{SE}$ enable setup time before SC high	t_{SWS}	10		15		ns
$t_{h(SEL)}$	$\overline{SE}$ enable hold time after SC high	t_{SWH}	20		30		ns
t_{DDTH}	Delay time, Data to $\overline{DT}$ high	t_{SZS}		0		0	ns
t_{DTHD}	Delay time, $\overline{DT}$ high to Data	—	20		30		ns

TIMING DIAGRAMS (Note 22)

Read Cycle

$t_{C(rd)}$
$t_{h(RLCH)}$
$t_{w(RL)}$
$t_{h(RLCA)}$

RAS (with bar over it): V_{IH}, V_{IL}

t_{CHRL} $t_{h(CLRH)}$ $t_{w(RH)}$
t_{RLCL} $t_{w(CL)}$

CAS (with bar over it): V_{IH}, V_{IL}

$t_{w(CH)}$
$t_{su(RA)}$ $t_{su(CA)}$ $t_{su(RA)}$
$t_{h(RA)}$ $t_{h(CLCA)}$

$A_0 \sim A_7$: V_{IH}, V_{IL} — ROW ADDRESS, COLUMN ADDRESS, ROW ADDRESS

$t_{su(rd)}$ $t_{h(CHrd)}$ $t_{h(RHrd)}$

WB/WE (with bars over them): V_{IH}, V_{IL}

t_{DCL}

Wi/IOi (INPUTS): V_{IH}, V_{IL} — High-Z

$t_{a(C)}$
$t_{a(R)}$ $t_{dis(CH)}$

Wi/IOi (OUTPUTS): V_{OH}, V_{OL} — High-Z, DATA VALID

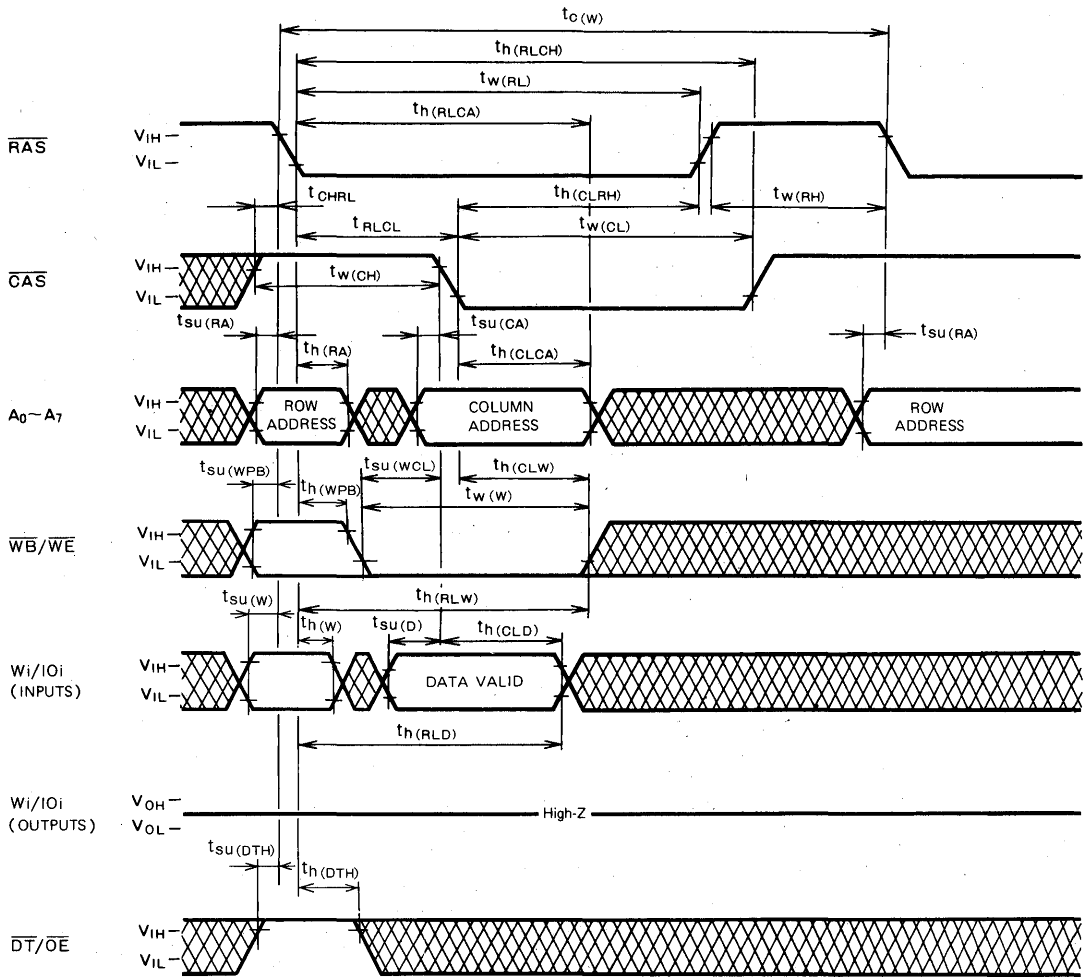
$t_{su(DTH)}$ t_{DOEL} $t_{a(OE)}$ $t_{dis(OE)}$
$t_{h(DTH)}$ $t_{h(OERH)}$ t_{OEHD}
$t_{h(OECH)}$

DT/OE (with bars over them): V_{IH}, V_{IL}

$t_{h(CLOE)}$
$t_{h(RLOE)}$

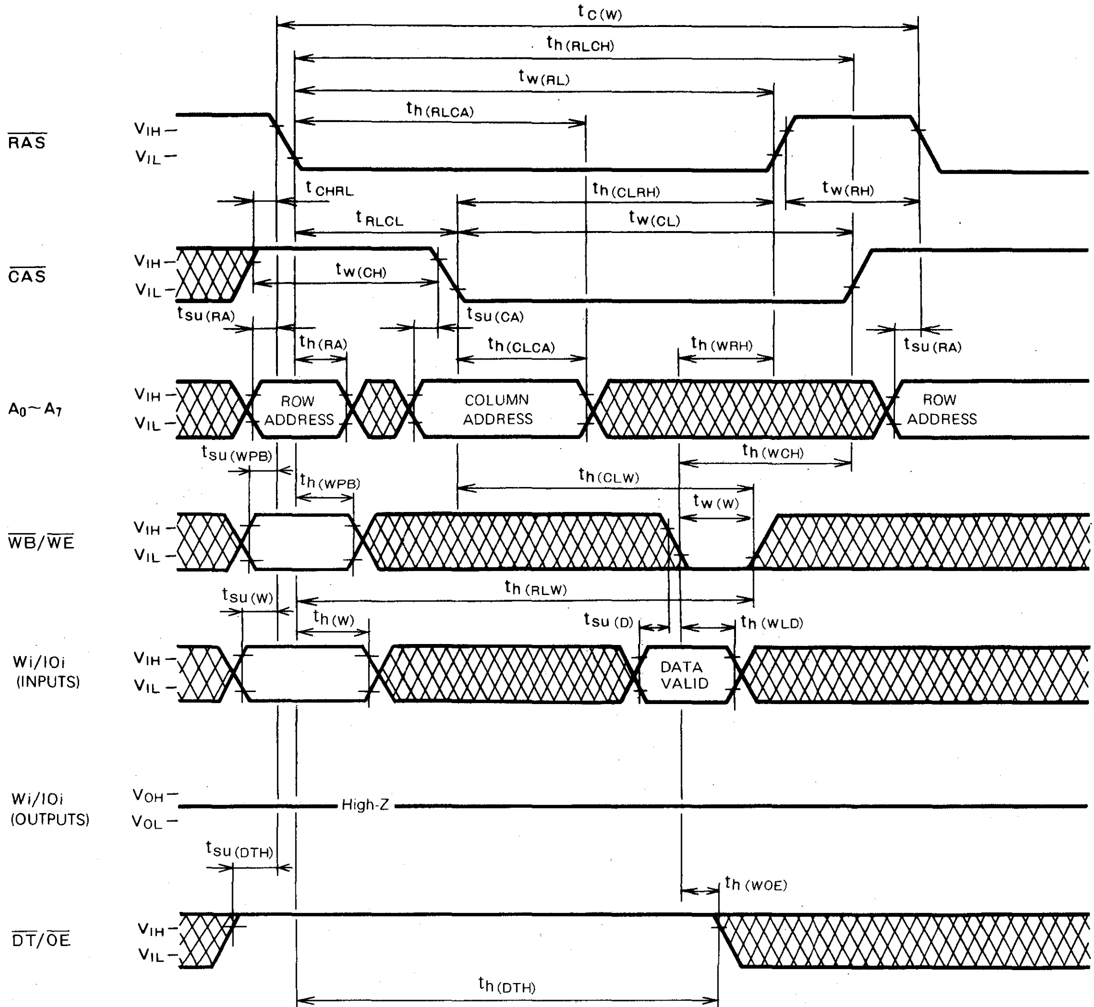
Note 22. Indicates the don't care input.

Write Cycle (Early Write)

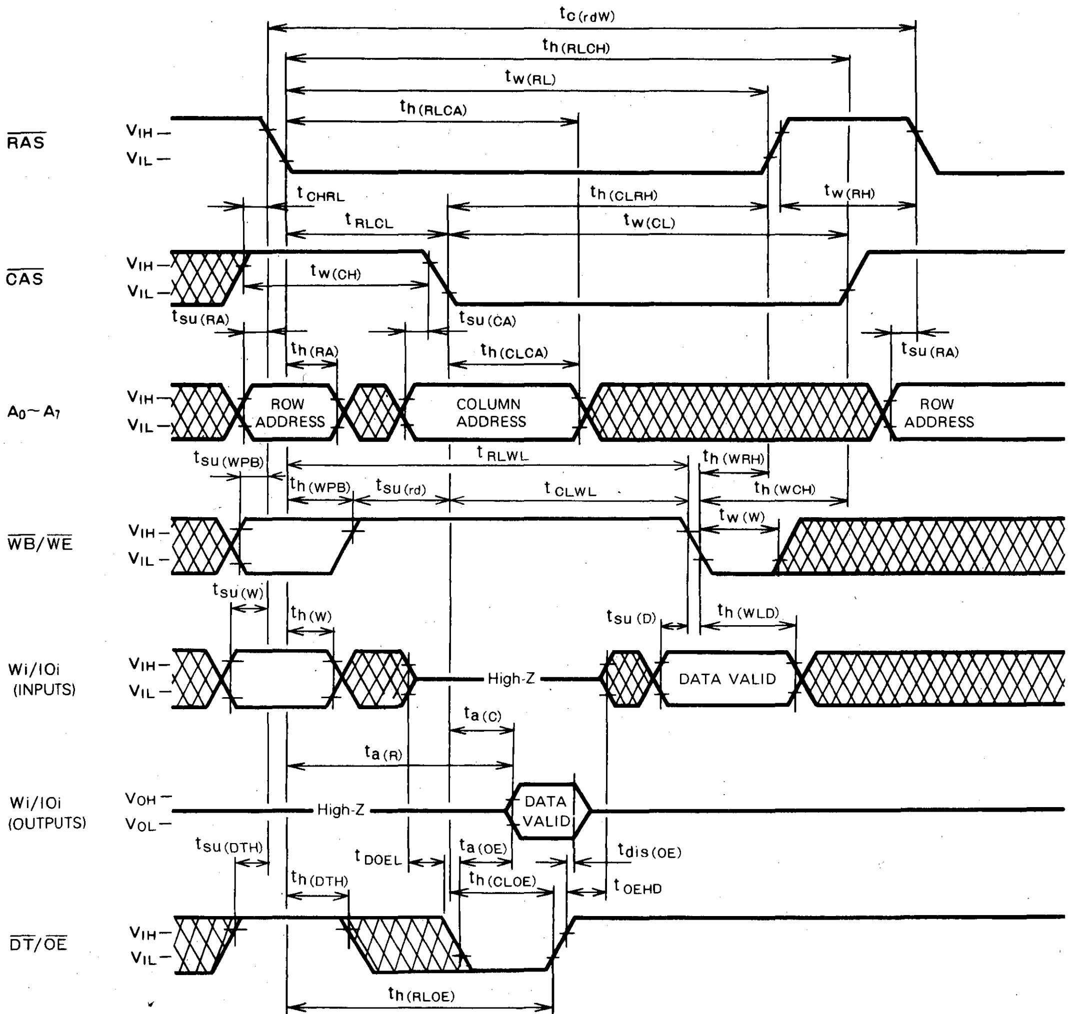


MITSUBISHI ELECTRIC

Write Cycle (Delayed Write)

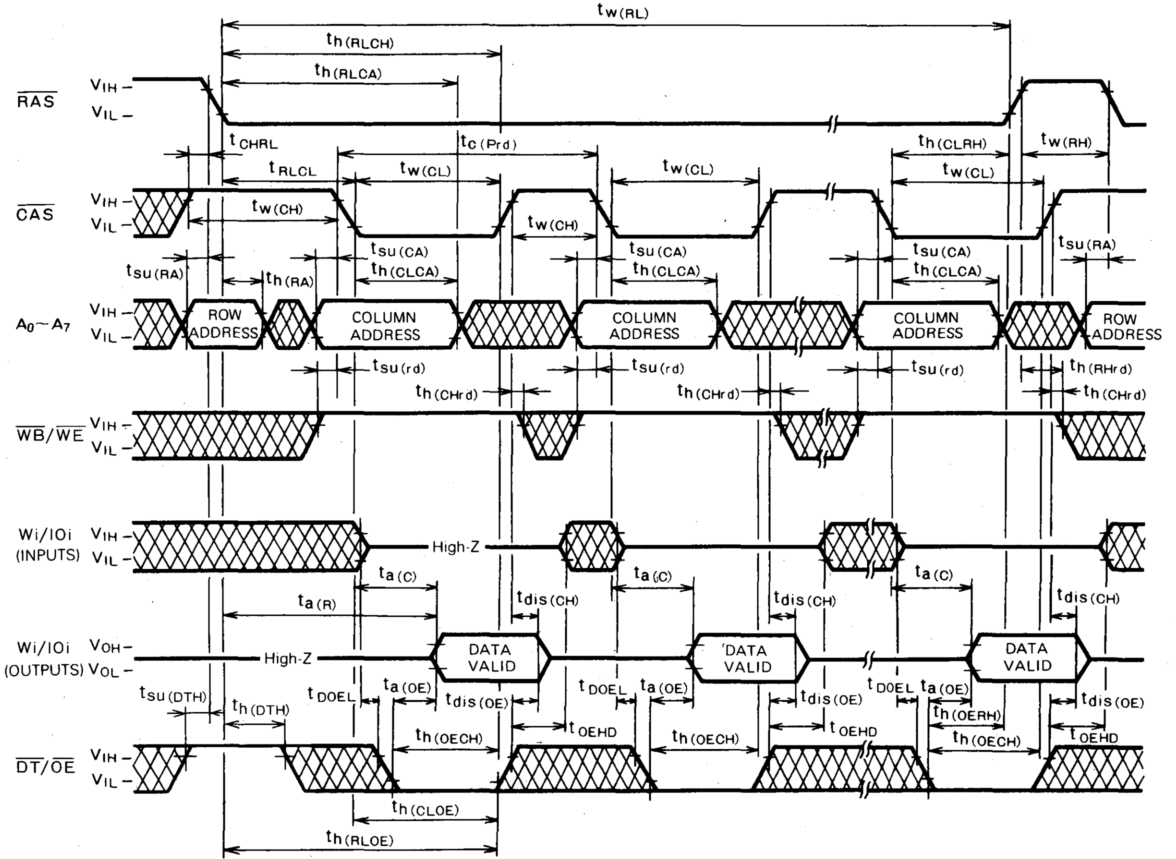


Read-Modify-Write Cycles

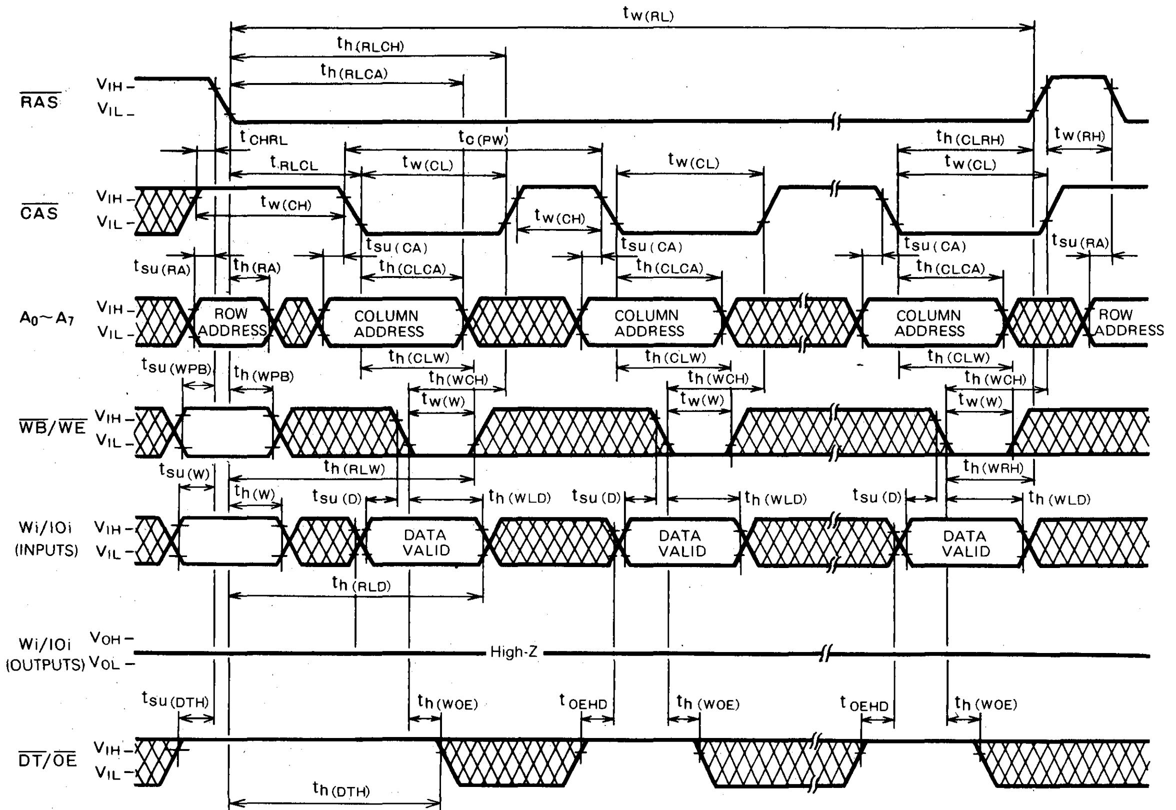


MITSUBISHI ELECTRIC

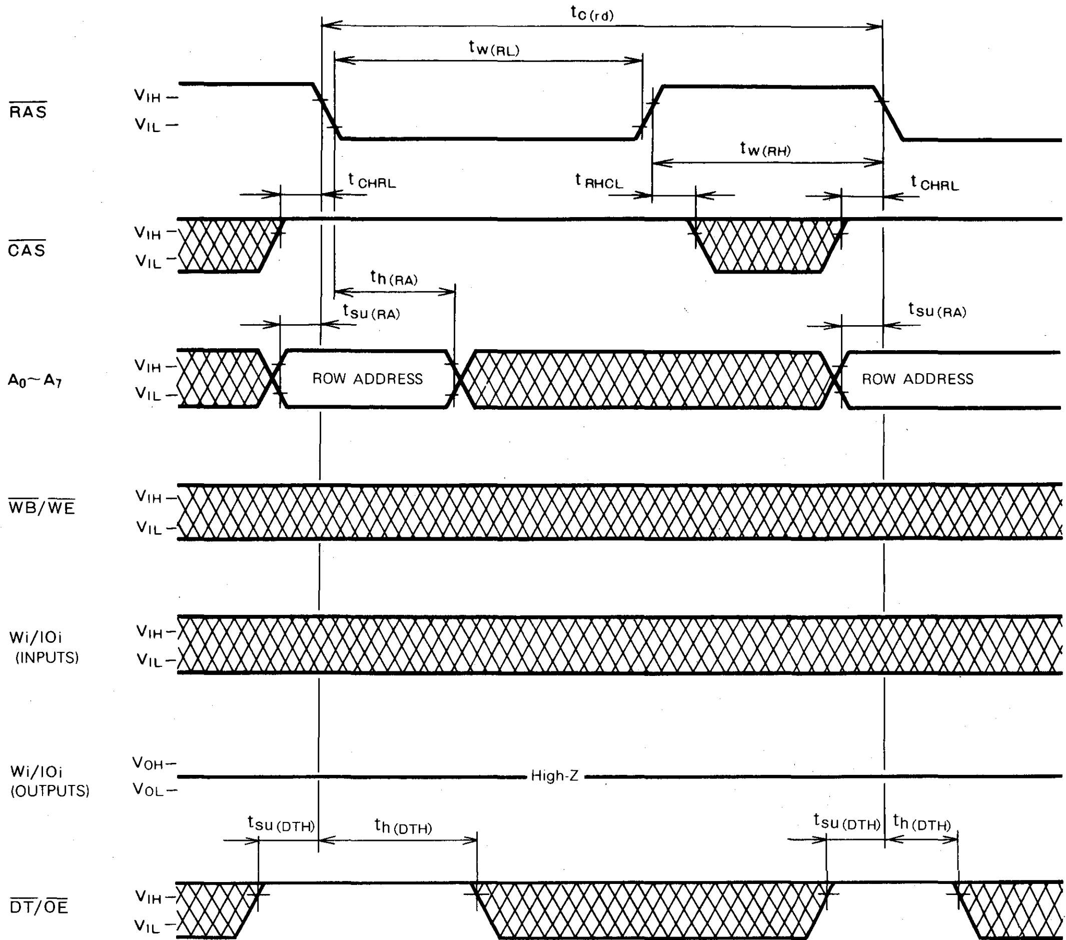
Page-Mode Read Cycle



Page-Mode Write Cycle



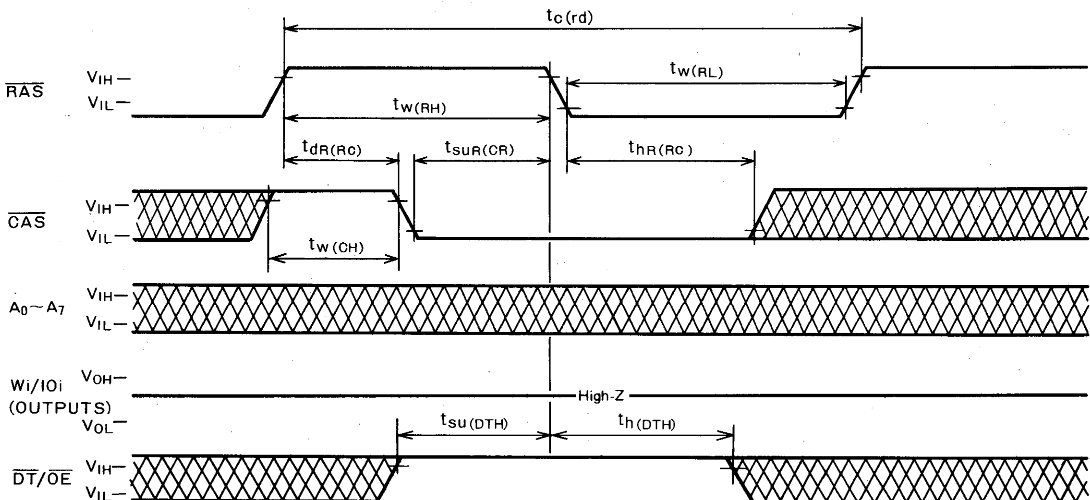
RAS-Only Refresh Cycle



Hidden Refresh Cycle

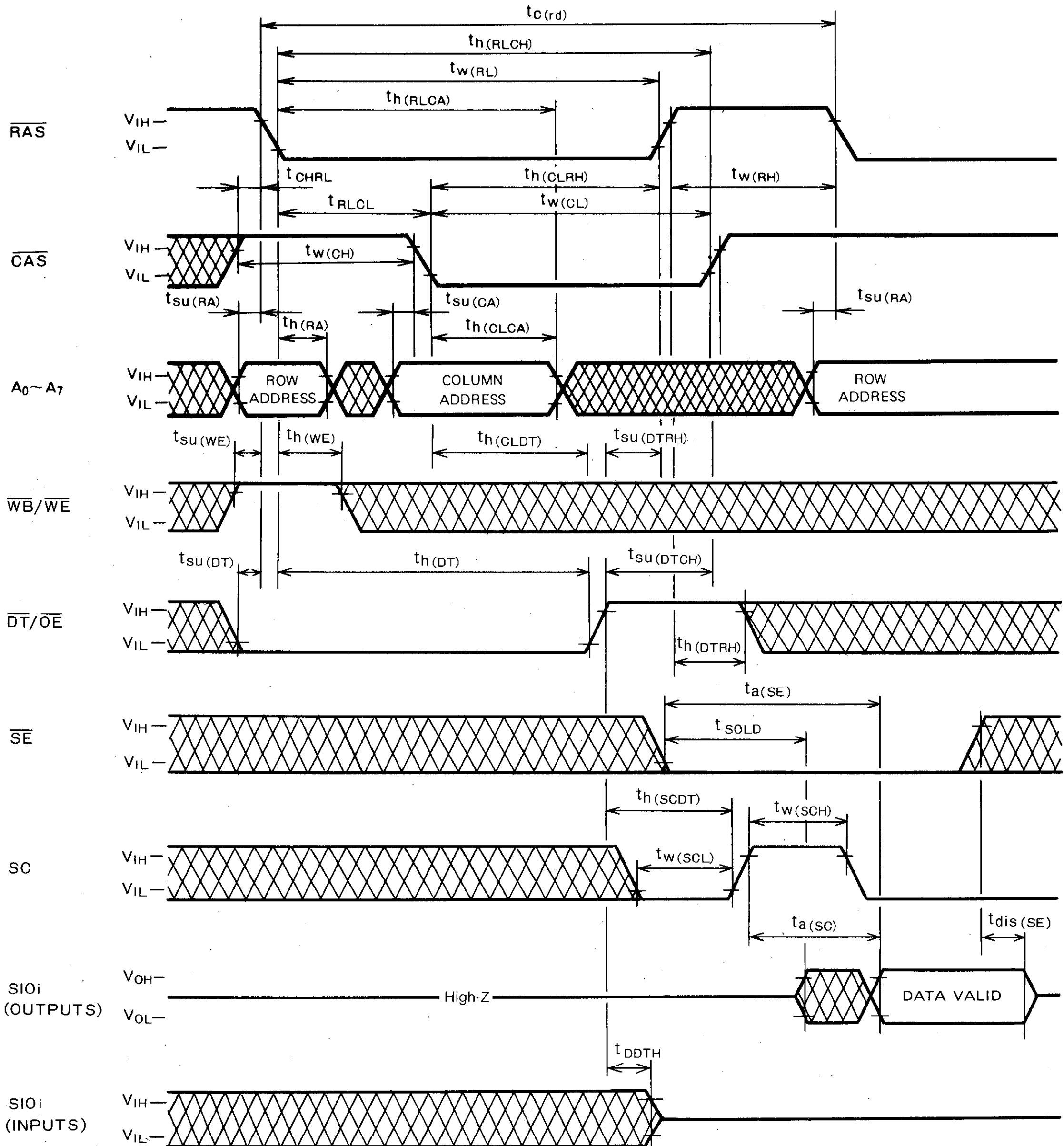
READ CYCLE
HIDDEN REFRESH CYCLE
$t_{c(rd)}$
$t_{w(RL)}$
$t_{w(RH)}$
$\overline{RAS}$ V_{IH} V_{IL}
t_{CHRL}
$t_{h(CLRH)}$
t_{RLCL}
$\overline{CAS}$ V_{IH} V_{IL}
$t_{w(CH)}$
$t_{su(RA)}$
$t_{su(CA)}$
$t_{h(CLCA)}$
$t_{h(RA)}$
$A_0 \sim A_7$ V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
$t_{su(rd)}$
$t_{h(RHrd)}$
$\overline{WB}/\overline{WE}$ V_{IH} V_{IL}
Wi/IOi (INPUTS) V_{IH} V_{IL}
High-Z
$t_{a(C)}$
$t_{a(R)}$
$t_{dis(CH)}$
Wi/IOi (OUTPUTS) V_{OH} V_{OL}
High-Z
DATA VALID
$t_{su(DTH)}$
t_{DOEL}
$t_{a(OE)}$
$t_{dis(OE)}$
$t_{h(DTH)}$
$t_{h(OERH)}$
t_{OEHD}
$\overline{DT}/\overline{OE}$ V_{IH} V_{IL}

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

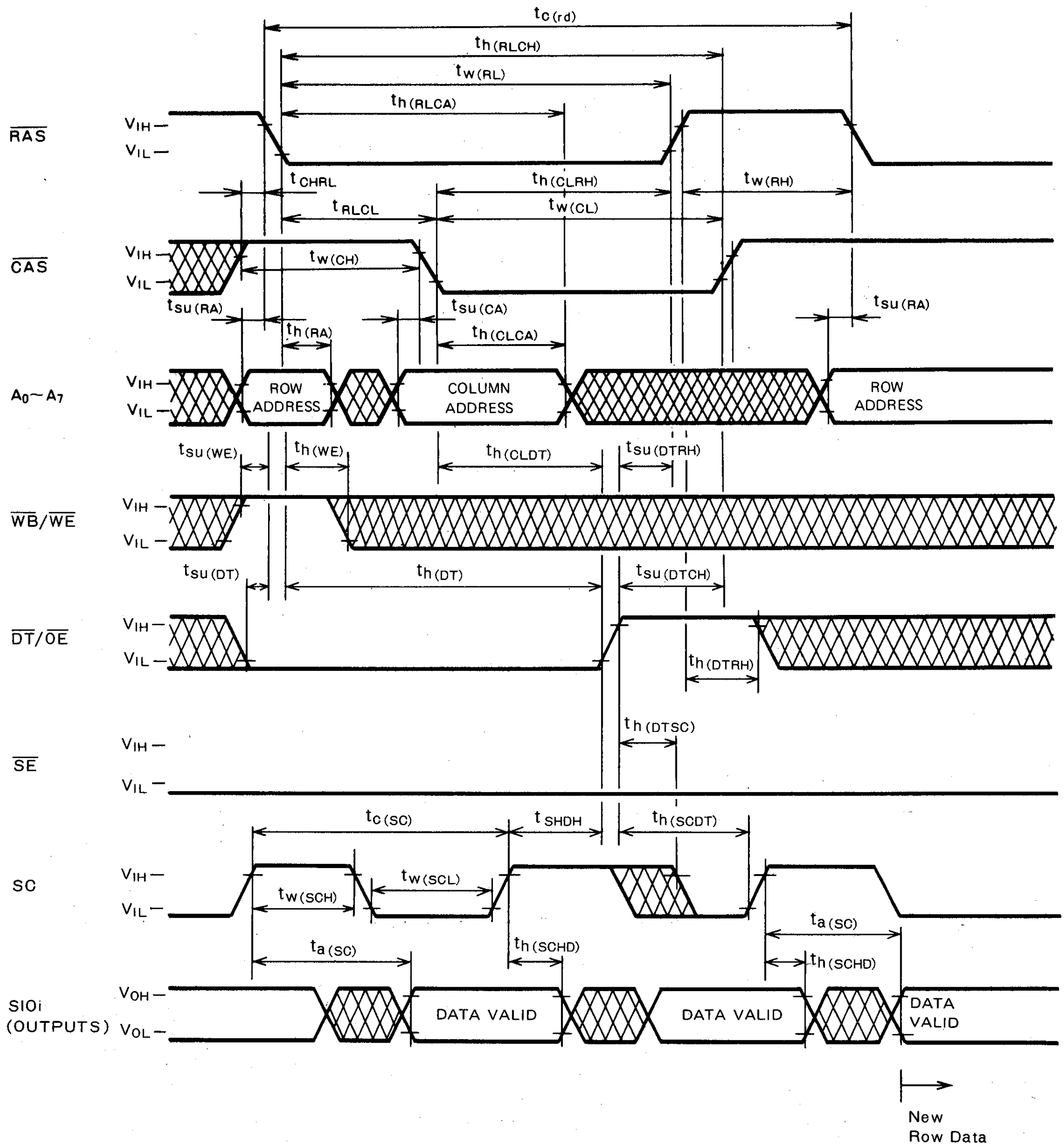


MITSUBISHI ELECTRIC

Read Transfer Cycle (B-port standby) Serial Read Setup (RAM → SAM)

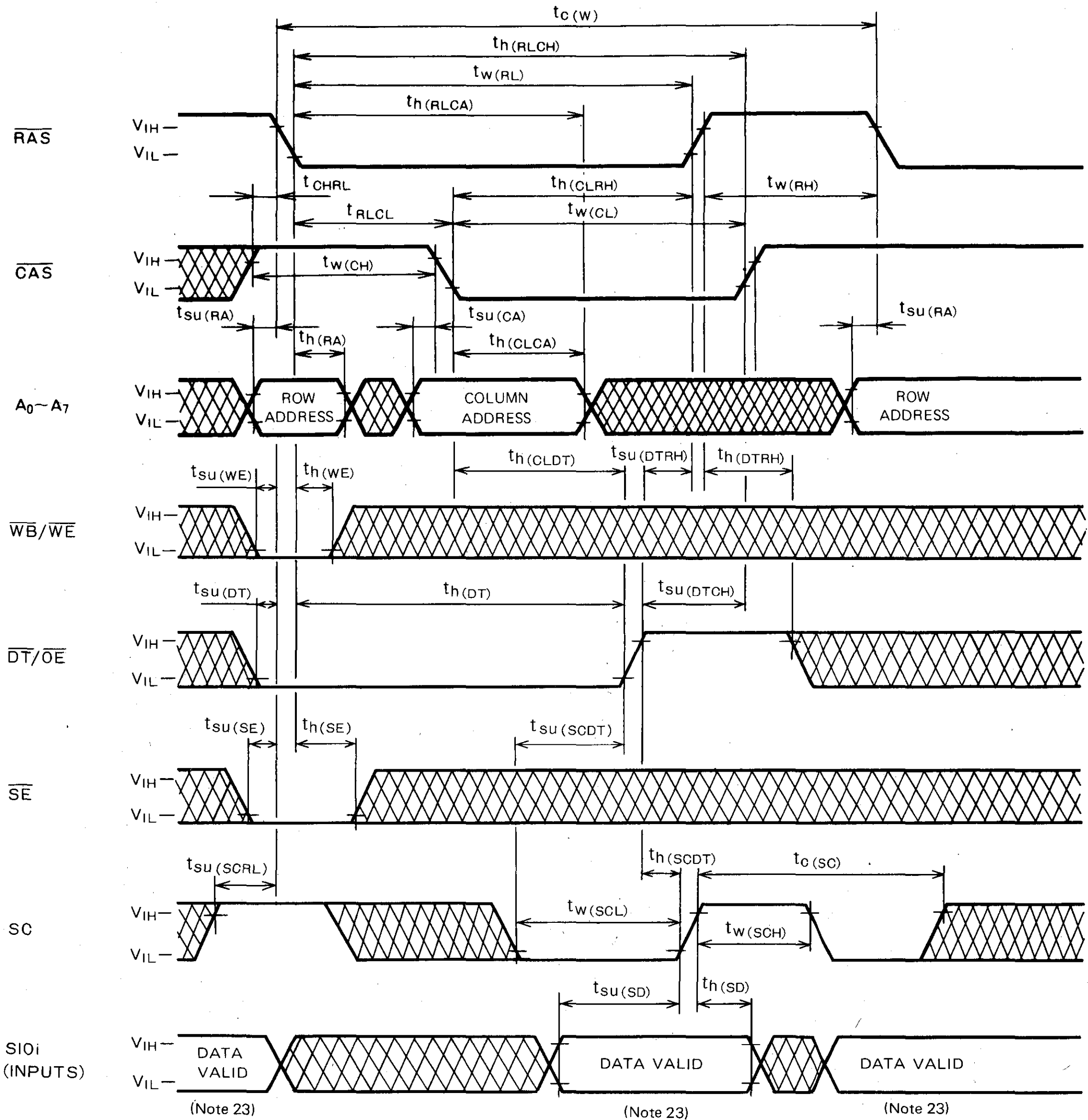


Read Transfer Cycle (B-port Active) Serial Read Setup (RAM → SAM)



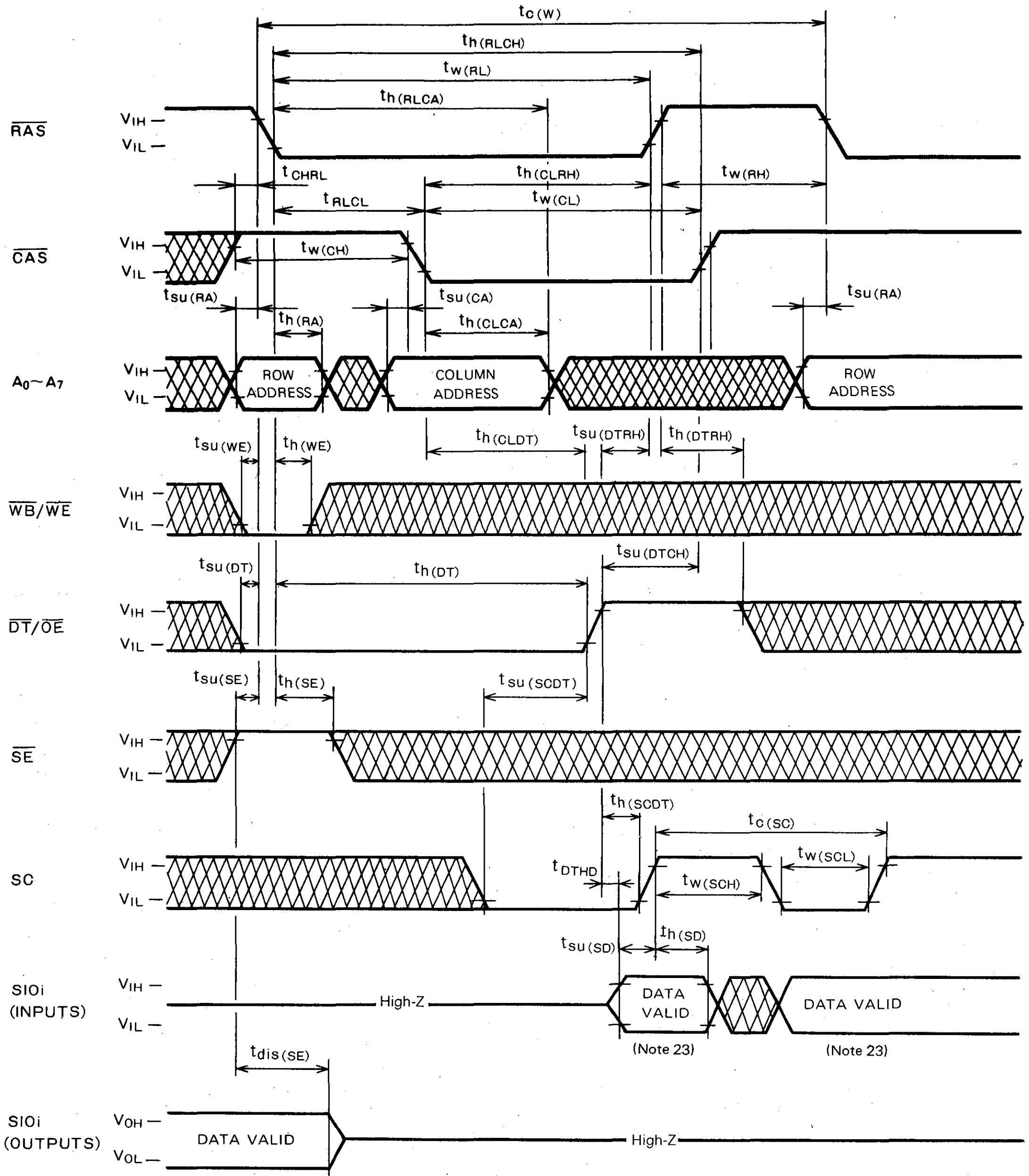
MITSUBISHI
ELECTRIC

Write Transfer Cycle (B-port Active) Serial Write Setup (SAM → RAM)

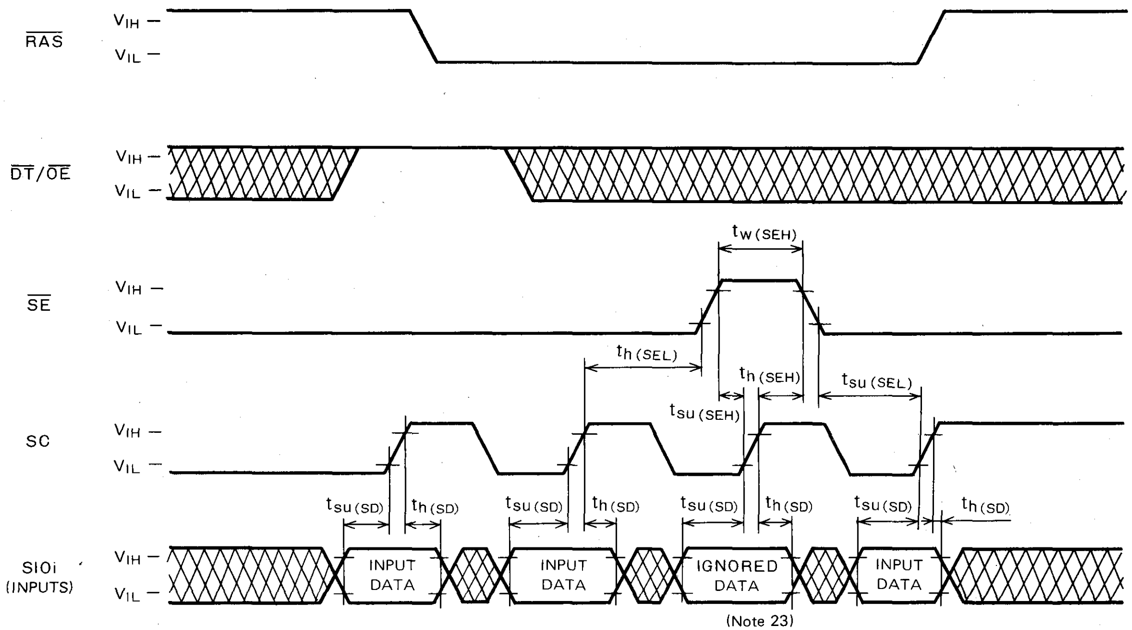


Note 23: When $\overline{SE}$ is "H" level, the serial input data are not written into the Data register, but the serial data selector is worked.

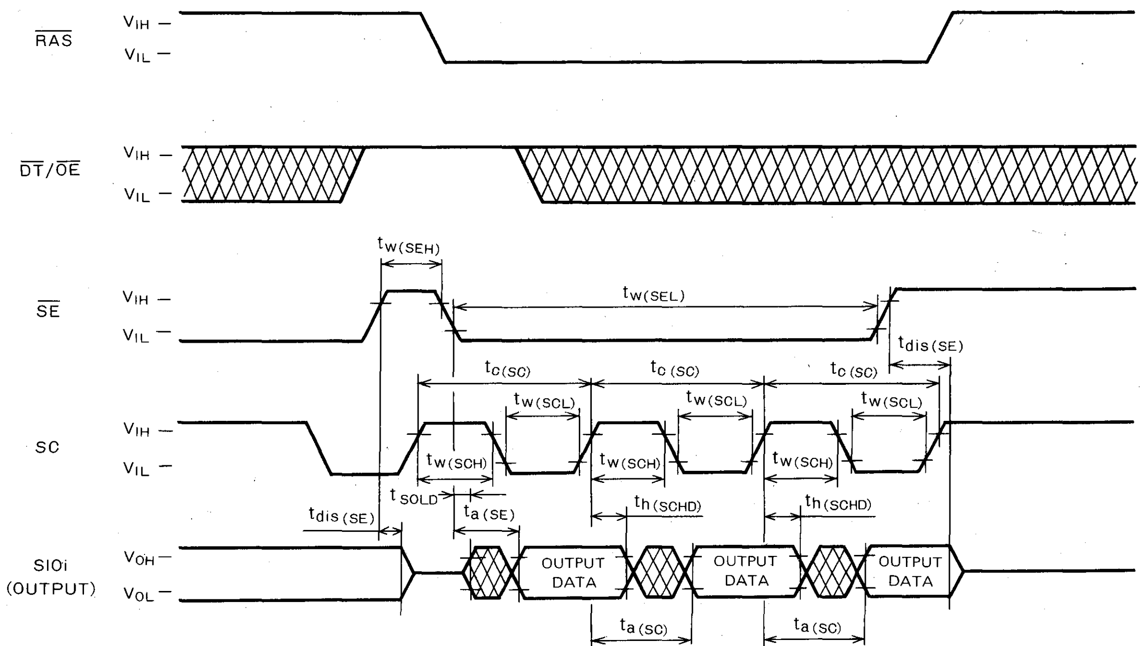
Pseudo Write Transfer Cycle (B-port Active) Serial Write Setup

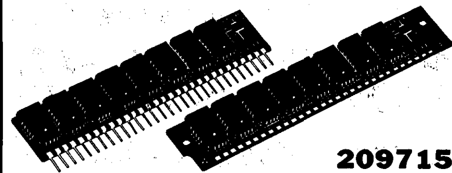


Serial Write Cycle



Serial Read Cycle





MITSUBISHI LSIs

MH25608J-10,-12,-15/ MH25608JA-10,-12,-15

2097152-BIT(262144-WORD BY 8-BIT)DYNAMIC RAM

DESCRIPTION

The MH25608J, JA is 262144 word x 8 bit dynamic RAM and consists of nine industry standard 256K x 1 dynamic RAMs in plastic leaded chip carrier.

The mounting of plastic leaded chip carrier on a single in-line package provides any application where high densities and large quantities of memory are required.

MH25608JA is a leaded type-memory module, allowing direct insertion to normal through-hole-board like DIP devices.

MH25608J is a socket type-memory module, suitable for easy interchanging or addition of modules.

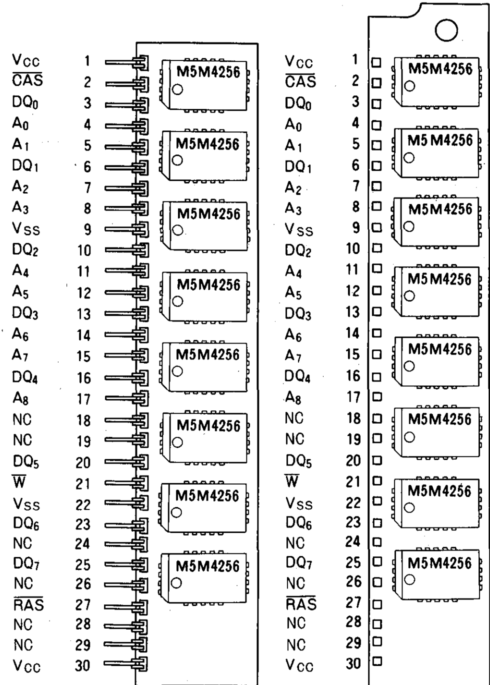
FEATURES

- High-speed

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH25608J-10 MH25608JA-10	100	200	2400
MH25608J-12 MH25608JA-12	120	230	2080
MH25608J-15 MH25608JA-15	150	260	1840

- Utilizes industry standard 256K RAMs in plastic leaded carriers
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 200mW(max)
- Low operation power dissipation:
  - MH25608J-10, MH25608JA-10 3.09W (max)
  - MH25608J-12, MH25608JA-12 2.88W (max)
  - MH25608J-15, MH25608JA-15 2.64W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.15μF x 8) decoupling capacitors
- 256 refresh cycles every 4ms, A_8 Pin is not need for refresh
- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.

PIN CONFIGURATION (TOP VIEW)

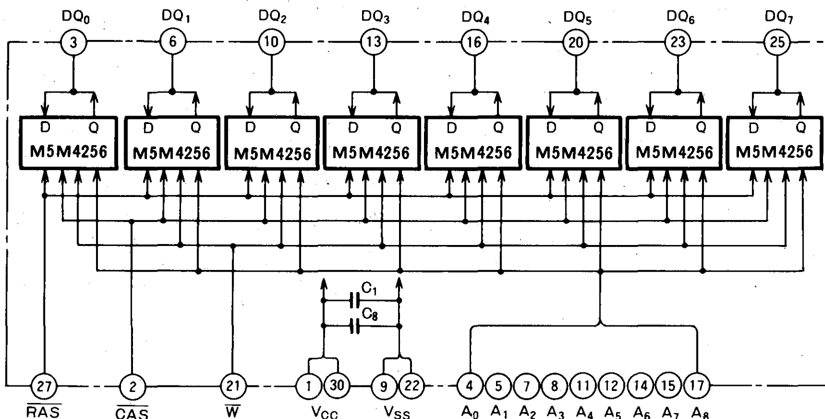


- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION

The MH25608J, JA provides, in addition to normal read and early write operations, a number of other functions, e.g., page mode, $\overline{\text{RAS}}$-only refresh, hidden refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Early write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
$\overline{\text{RAS}}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Page mode identical except refresh is No.

SUMMARY OF OPERATIONS

Addressing

To select 8 of the 2,097,152 memory cells in the MH25608J, JA the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{\text{RAS}}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{\text{CAS}}$) latches the 9 column-address bits. Timing of the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{\text{CAS}}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{\text{CAS}}$' operation). The external $\overline{\text{CAS}}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{\text{CAS}}$ has already been released, so that the internal $\overline{\text{CAS}}$ control signals are controlled by the externally applied $\overline{\text{CAS}}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{\text{W}}$ input and $\overline{\text{CAS}}$ input. Thus when the $\overline{\text{W}}$ input makes its negative transition prior to $\overline{\text{CAS}}$ input (early write), the data input is strobed by $\overline{\text{CAS}}$, and the negative transition of $\overline{\text{CAS}}$ is set as the reference point for set-up and hold times. If the $\overline{\text{W}}$ input makes its negative transition after to $\overline{\text{CAS}}$ input, Data input will contend with the Data output because of the common I/O feature.

Data Output Control

The output of the MH25608J, JA is in the high-impedance state when $\overline{\text{CAS}}$ is high. When the memory cycle in progress is a read, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{\text{CAS}}$ goes high, irrespective of the condition of $\overline{\text{RAS}}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write operation.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{\text{RAS}}$, because once the row address has been strobed, $\overline{\text{RAS}}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the MH25608J, JA must be refresh every 4 ms to maintain data. The methods of refreshing for the MB25608J, JA are as follows.

1. Normal Refresh

Read cycle and Early Write cycle refresh the selected row as defined by the low order ($\overline{\text{RAS}}$) addresses.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the MH25608J, JA is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the MH25608J, JA is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH25608J, JA as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The MH25608J, JA operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

2097152-BIT(262144-WORD BY 8-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage	With respect to V_{SS}	−1~7	V
V_O	Output voltage	With respect to V_{SS}	−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	8	W
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		−55~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−20		20	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−80		80	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	MH25608J-10 MH25608JA-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open			560	mA
		MH25608J-12 MH25608JA-12				520	
		MH25608J-15 MH25608JA-15				480	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = \overline{CAS} = V_{IH}$ output open			36	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	MH25608J-10 MH25608JA-10	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(RAS)}$ = min, output open			480	mA
		MH25608J-12 MH25608JA-12				440	
		MH25608J-15 MH25608JA-15				400	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	MH25608J-10 MH25608JA-10	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{CPG} = min, output open			440	mA
		MH25608J-12 MH25608JA-12				400	
		MH25608J-15 MH25608JA-15				360	
$I_{CC6(AV)}$	Average supply current from V_{CC}, automatic refreshing (Note 3)	MH25608J-10 MH25608JA-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{O(RAS)}$ = min, output open			520	mA
		MH25608J-10 MH25608JA-12				480	
		MH25608J-15 MH25608JA-15				440	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_I = 25mVrms			60	pF
$C_{(DQ)}$	Data input/data output capacitance					20	pF
$C_{I(W)}$	Input capacitance, write control input					80	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					100	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					100	pF

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Early Write, Refresh, and Page-Mode Cycle)

($Ta=0\sim70°C$, $V_{CC}=-5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Limits
			MH25608J-10, JA-10		MH25608J-12, JA-12		MH25608J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ (Note 8)	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500µs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined at $t_{THL}=t_{TLH}=5ns$.
7. Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for all $\overline{RAS}/\overline{CAS}$ cycles
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}\ min = t_{h(RAS-RA)}\ min + 2t_{THL(tTHL)} + t_{su(CA-CAS)}\ min.$

SWITCHING CHARACTERISTIC ($Ta=0\sim70°C$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25608J-10, JA-10		MH25608J-12, JA-12		MH25608J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the vauel when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25608J-10, JA-10		MH25608J-12, JA-12		MH25608J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 15)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Note 15: When $t_{su(W-CAS)} < t_{su(W-CAS)}$ min, Data input will contend with the data output because of the common I/O feature.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25608J-10, JA-10		MH25608J-12, JA-12		MH25608J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	100		125		145		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		55		60		ns

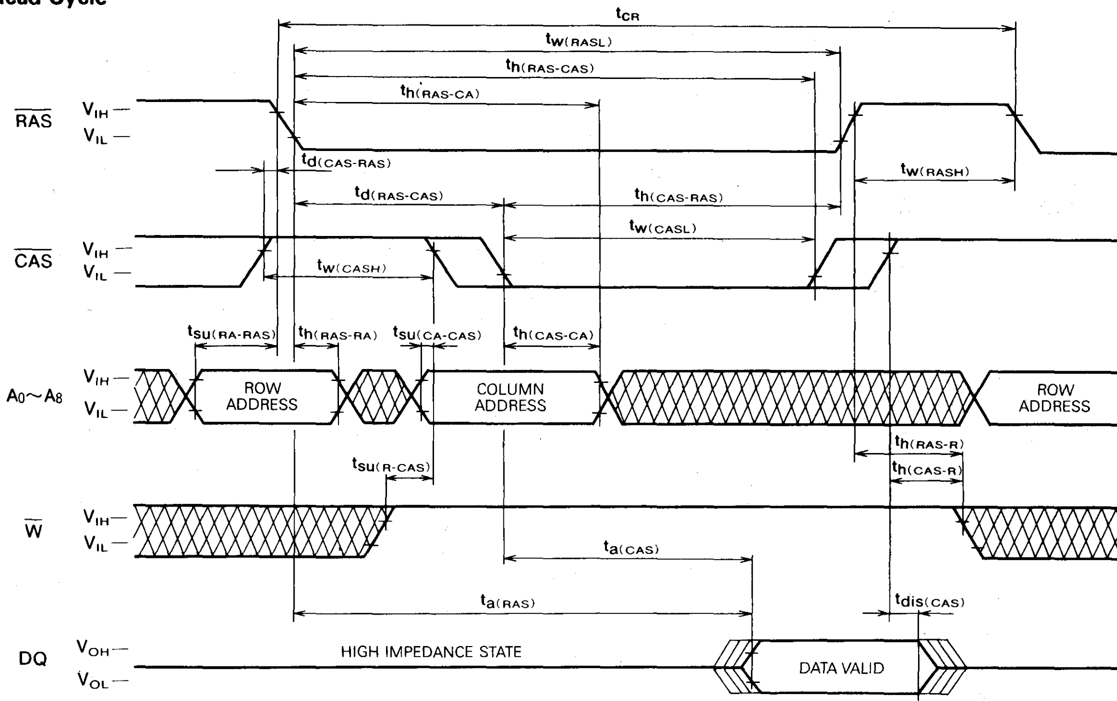
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 16)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25608J-10, JA-10		MH25608J-12, JA-12		MH25608J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
$t_{SUR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

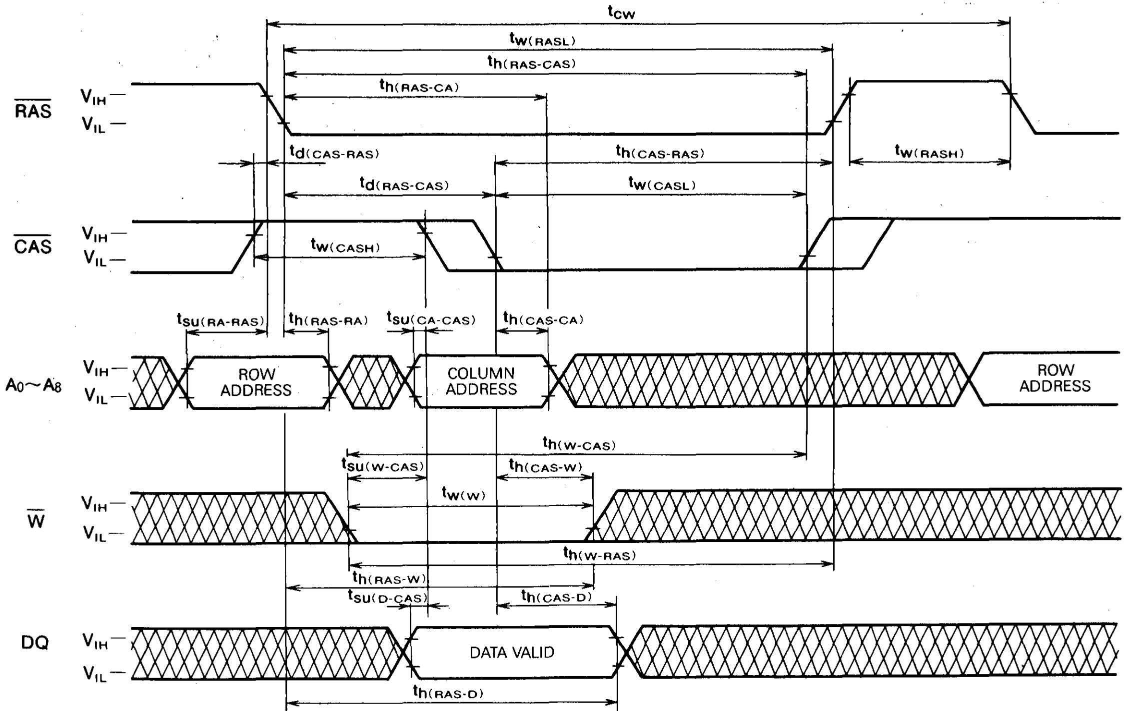
Note 16. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 17)

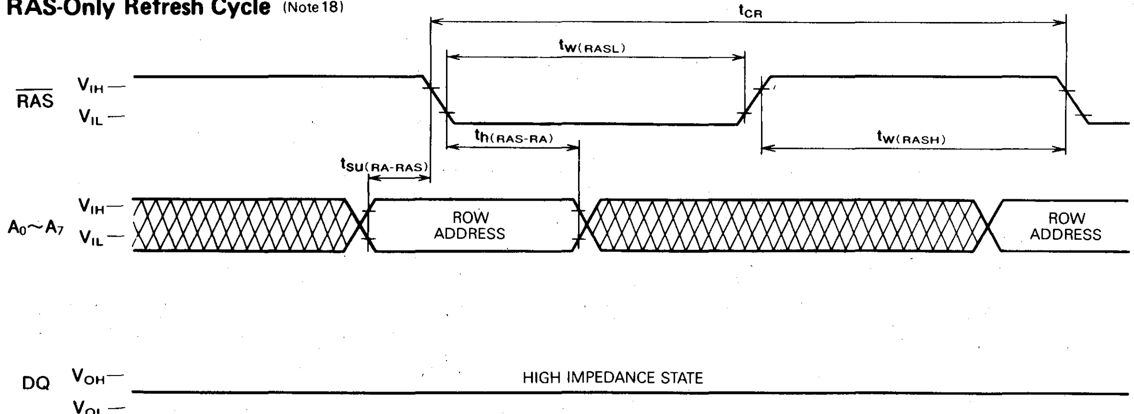
Read Cycle



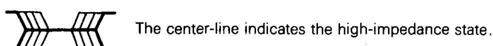
Early Write Cycle



RAS-Only Refresh Cycle (Note 18)

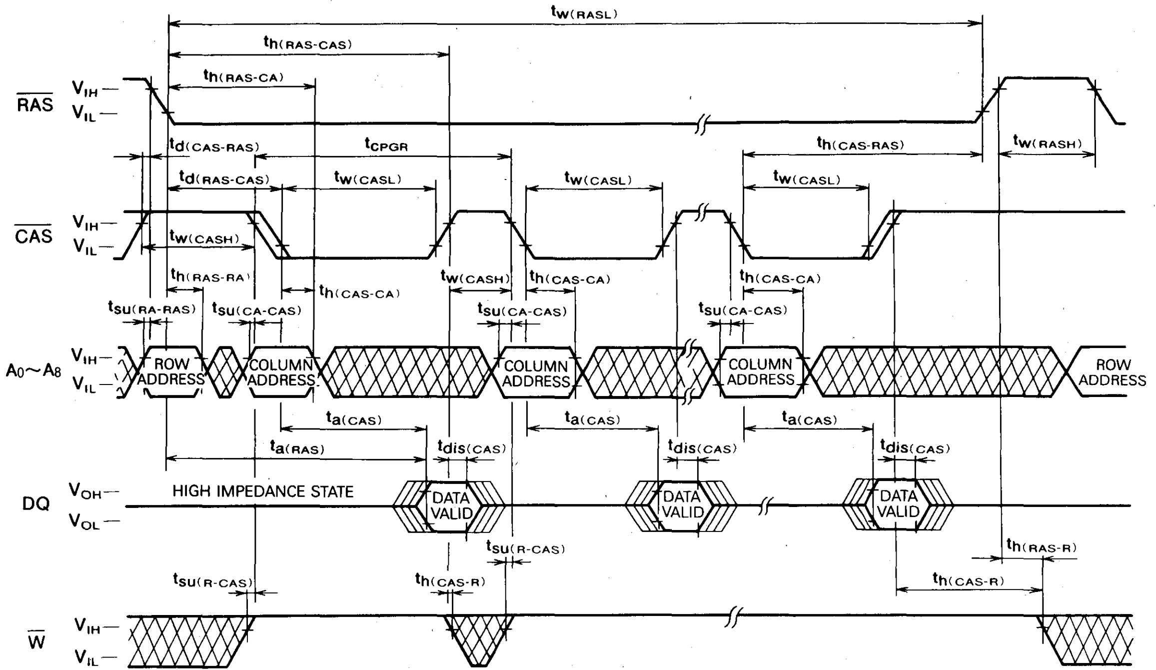


Note 17. Indicates the don't care input.

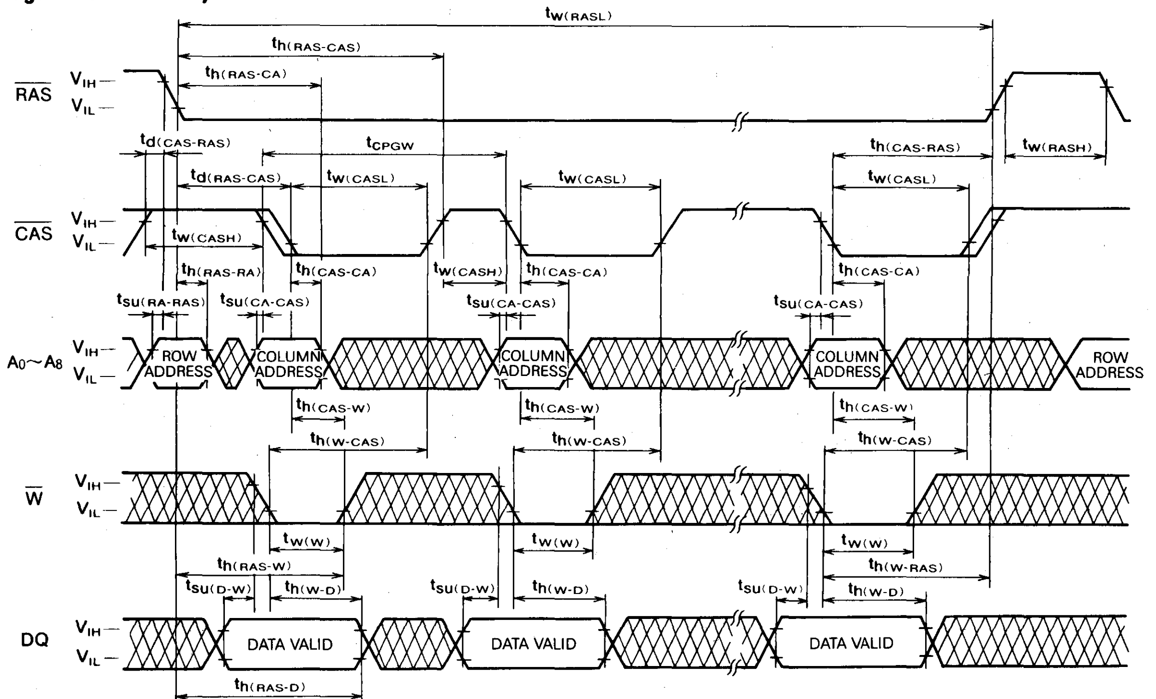
 The center-line indicates the high-impedance state.

Note 18. $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = don't care. A8 may be V_{IH} or V_{IL}.

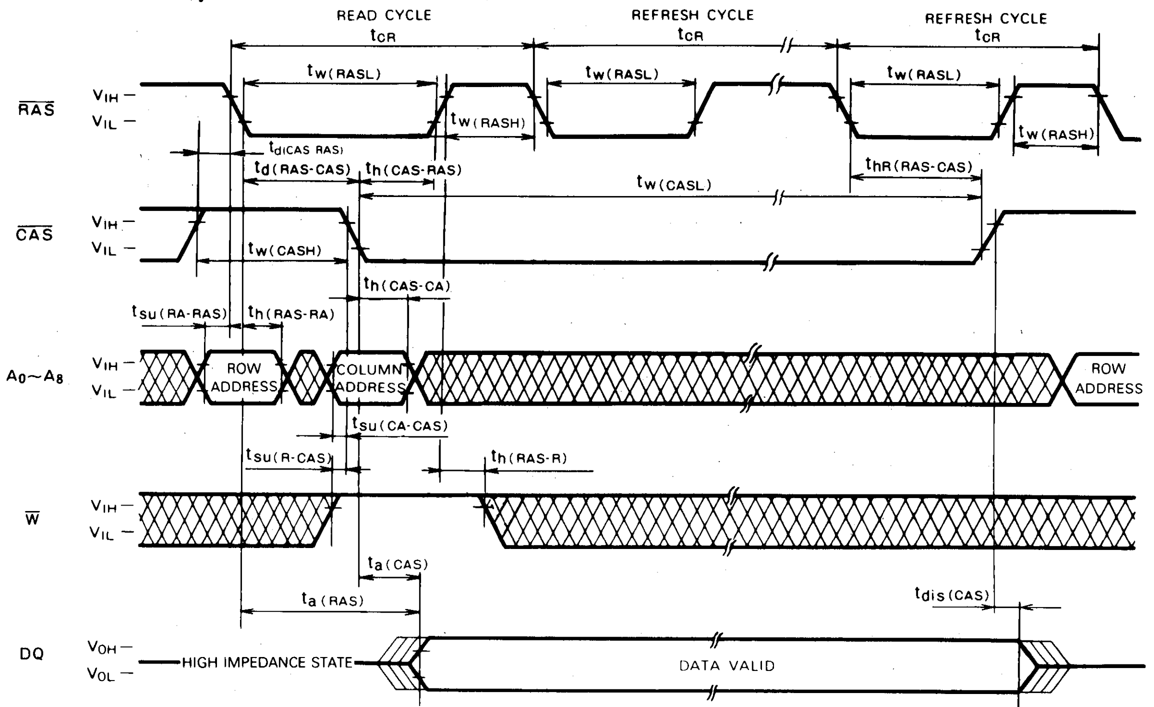
Page-Mode Read Cycle



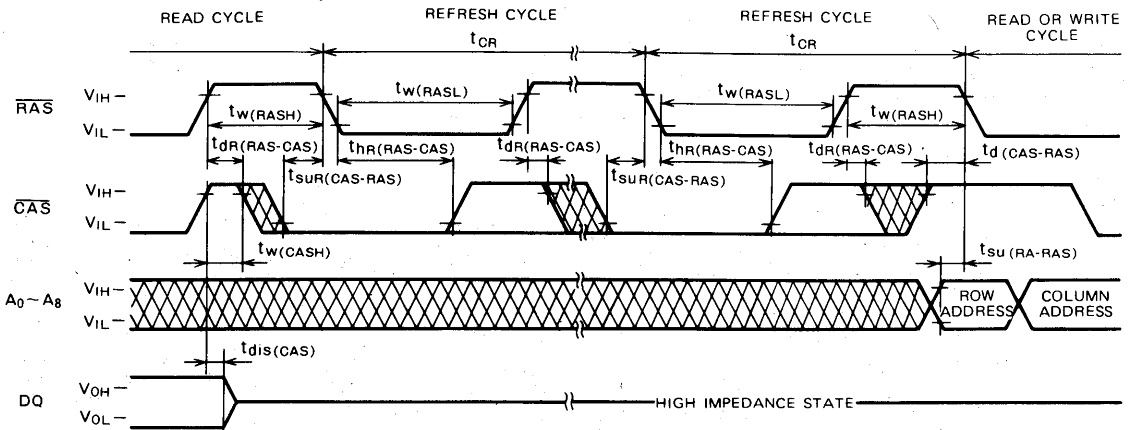
Page-Mode Write Cycle



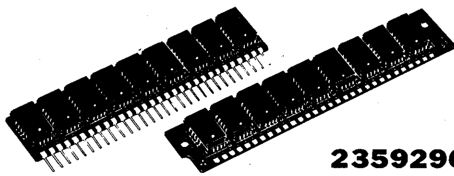
Hidden Refresh Cycle



CAS before RAS Refresh Cycle (Note 19)



Note19 : W, D = don't care.



MH25609J-10,-12, 15/ MH25609JA-10,-12,-15

2359296-BIT(262144-WORD BY 9-BIT)DYNAMIC RAM

DESCRIPTION

The MH25609J, JA is 262144 word x 9 bit dynamic RAM and consists of nine industry standard 256K x 1 dynamic RAMs in plastic leaded chip carrier.

The mounting of plastic leaded chip carrier on a single in-line package provides any application where high densities and large quantities of memory are required.

MH25609JA is a leaded type-memory module, allowing direct insertion to normal through-hole-board like DIP devices.

MH25609J is a socket type-memory module, suitable for easy interchanging or addition of modules.

FEATURES

- High-speed

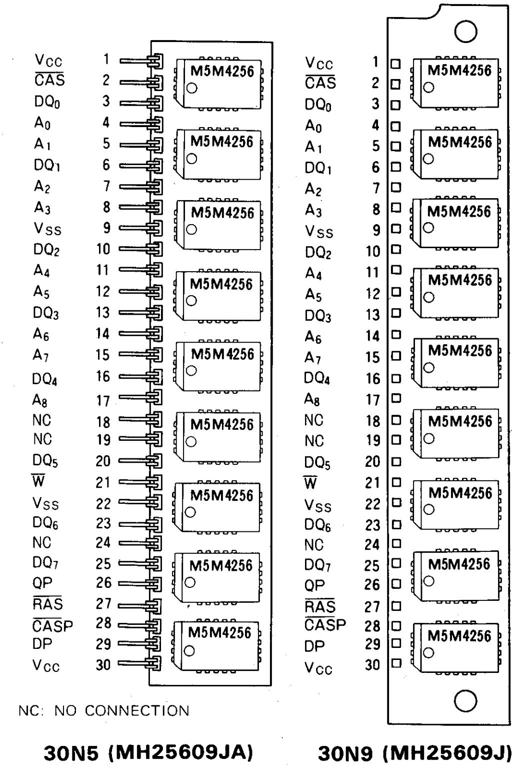
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH25609J-10 MH25609JA-10	100	200	2700
MH25609J-12 MH25609JA-12	120	230	2340
MH25609J-15 MH25609JA-15	150	260	2070

- Utilizes industry standard 256K RAMs in plastic leaded carriers
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 225mW(max)
- Low operation power dissipation:

MH25609J-10, MH25609JA-10	3.47W (max)
MH25609J-12, MH25609JA-12	3.24W (max)
MH25609J-15, MH25609JA-15	2.97W (max)

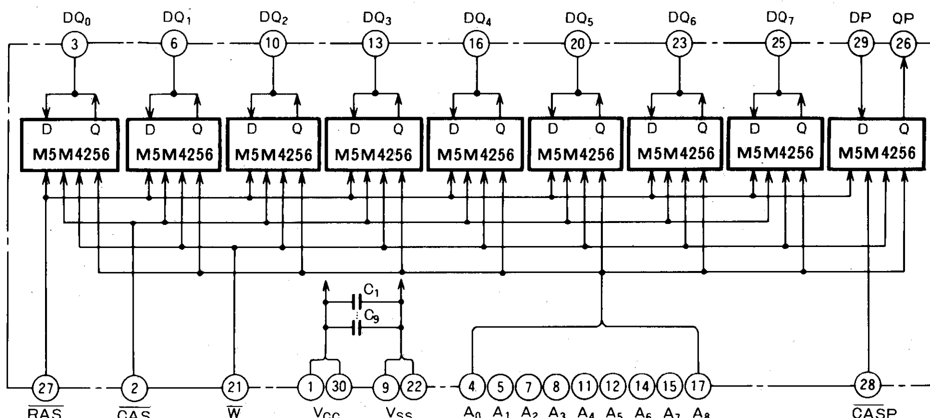
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.15μF x 9) decoupling capacitors
- 256 refresh cycles every 4ms, A_8 Pin is not need for refresh
- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CAS}$ ($\overline{CASP}$) control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.
- Bit nine (DP, QP) controlled by $\overline{CASP}$ is generally used for parity.

PIN CONFIGURATION (TOP VIEW)



30N5 (MH25609JA) 30N9 (MH25609J)

BLOCK DIAGRAM



2359296-BIT(262144-WORD BY 9-BIT)DYNAMIC RAM

APPLICATION
Main memory unit for computers, Microcomputer memory

FUNCTION
The MH25609J, JA provides, in addition to normal read and early write operations, a number of other functions, e.g., page mode, RAS-only refresh, hidden refresh and CAS before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Ope Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Early write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.
* : Page mode identical except refresh is No.

SUMMARY OF OPERATIONS

Addressing
To select 9 of the 2,359,296 memory cells in the MH25609J, JA the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\ (RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input
Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. If the $\overline{W}$ input makes its negative transition after to $\overline{CAS}$ input, Data input will contend with the Data output because of the common I/O feature.

Data Output Control
The output of the MH25609J, JA is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write operation.

Page-Mode Operation
This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh
Each of the 256 rows ($A_0 \sim A_7$) of the MH25609J, JA must be refresh every 4 ms to maintain data. The methods of refreshing for the MH25609J, JA are as follows.

1. Normal Refresh

Read cycle and Early Write cycle refresh the selected row as defined by the low order ($\overline{RAS}$) addresses.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the MH25609J, JA is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the MH25609J, JA is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH25609J, JA as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The MH25609J, JA operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25°C	9	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−55~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−20		20	μA
I_I	Input current		0V ≦ V_{IN} ≦ V_{CC}, Other input pins = 0V	−90		90	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	MH25609J-10 MH25609JA-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{CR} = t_{CW}$ = min, output open			630	mA
		MH25609J-12 MH25609JA-12				585	
		MH25609J-15 MH25609JA-15				540	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = \overline{CAS} = V_{IH}$ output open			40.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	MH25609J-10 MH25609JA-10	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{C(RAS)}$ = min, output open			540	mA
		MH25609J-12 MH25609JA-12				495	
		MH25609J-15 MH25609JA-15				450	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	MH25609J-10 MH25609JA-10	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{CPG} = min, output open			495	mA
		MH25609J-12 MH25609JA-12				450	
		MH25609J-15 MH25609JA-15				405	
$I_{CC6(AV)}$	Average supply current from V_{CC}, automatic refreshing (Note 3)	MH25609J-10 MH25609JA-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{O(RAS)}$ = min, output open			585	mA
		MH25609J-10 MH25609JA-12				540	
		MH25609J-15 MH25609JA-15				495	
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_I = 25mVrms			60	pF
$C_{(DQ)}$	Data input/data output capacitance					20	pF
$C_{I(W)}$	Input capacitance, write control input					80	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					100	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					100	pF
$C_{I(CASP)}$	Input capacitance, $\overline{CAS}$P input					20	pF
$C_{I(DP)}$	Input capacitance					15	pF
$C_{O(QP)}$	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_I = 25mVrms			15	pF

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Early Write, Refresh, and Page-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits						Limits
			MH25609J-10, JA-10		MH25609J-12, JA-12		MH25609J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	90		100		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50		60		75		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		30		35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ (Note 8)	t_{RSH}	50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	20		30		30		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6. The switching characteristics are defined at $t_{THL} = t_{TLH} = 5ns$.
7. Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.
8. Except for page-mode.
9. $t_{d(CAS-RAS)}$ requirement is only applicable for all $\overline{RAS}/\overline{CAS}$ cycles
10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}$ min = $t_{h(RAS-RA)}$ min + $2t_{THL(tTHL)}$ + $t_{su(CA-CAS)}$ min.

SWITCHING CHARACTERISTIC ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25609J-10, JA-10		MH25609J-12, JA-12		MH25609J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	200		230		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	20		20		20		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	25	0	35	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		100		120		150	ns

Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12. $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13. This is the vauel when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25609J-10, JA-10		MH25609J-12, JA-12		MH25609J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	200		230		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 15)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	35		40		45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	85		100		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		40		45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	25		30		35		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	70		90		110		ns

Note 15: When $t_{su(W-CAS)} < t_{su(W-CAS)}$ min, Data input will contend with the data output because of the common I/O feature.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25609J-10, JA-10		MH25609J-12, JA-12		MH25609J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	100		125		145		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	40		55		60		ns

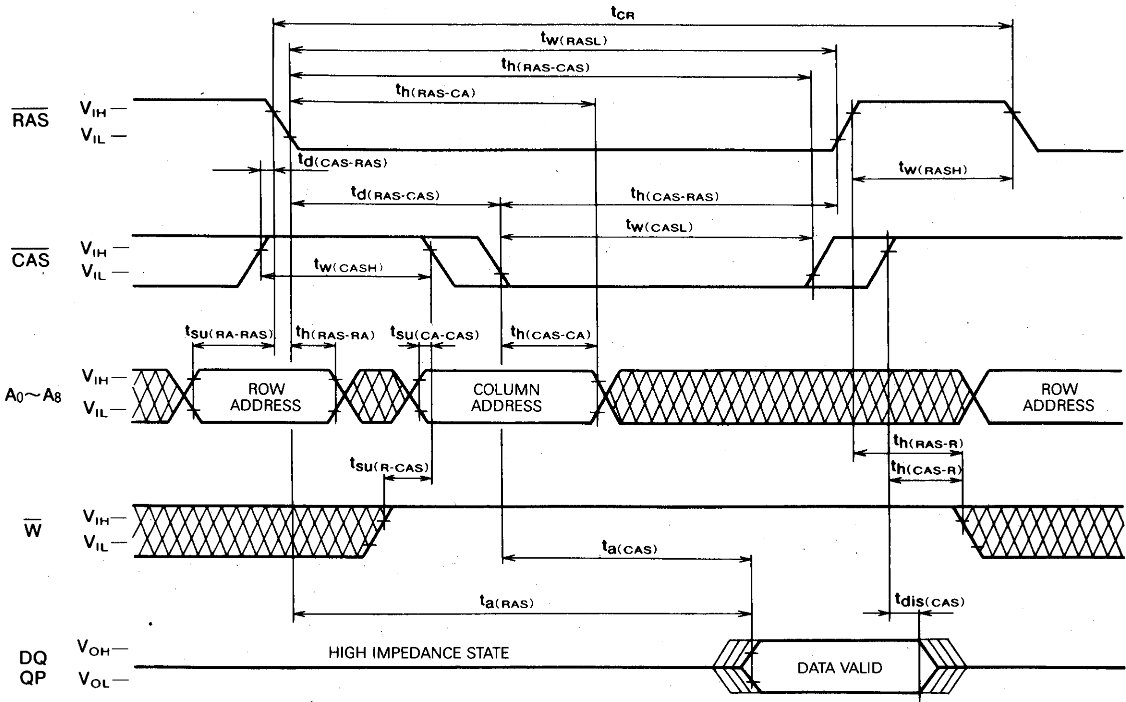
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 16)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			MH25609J-10, JA-10		MH25609J-12, JA-12		MH25609J-15, JA-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

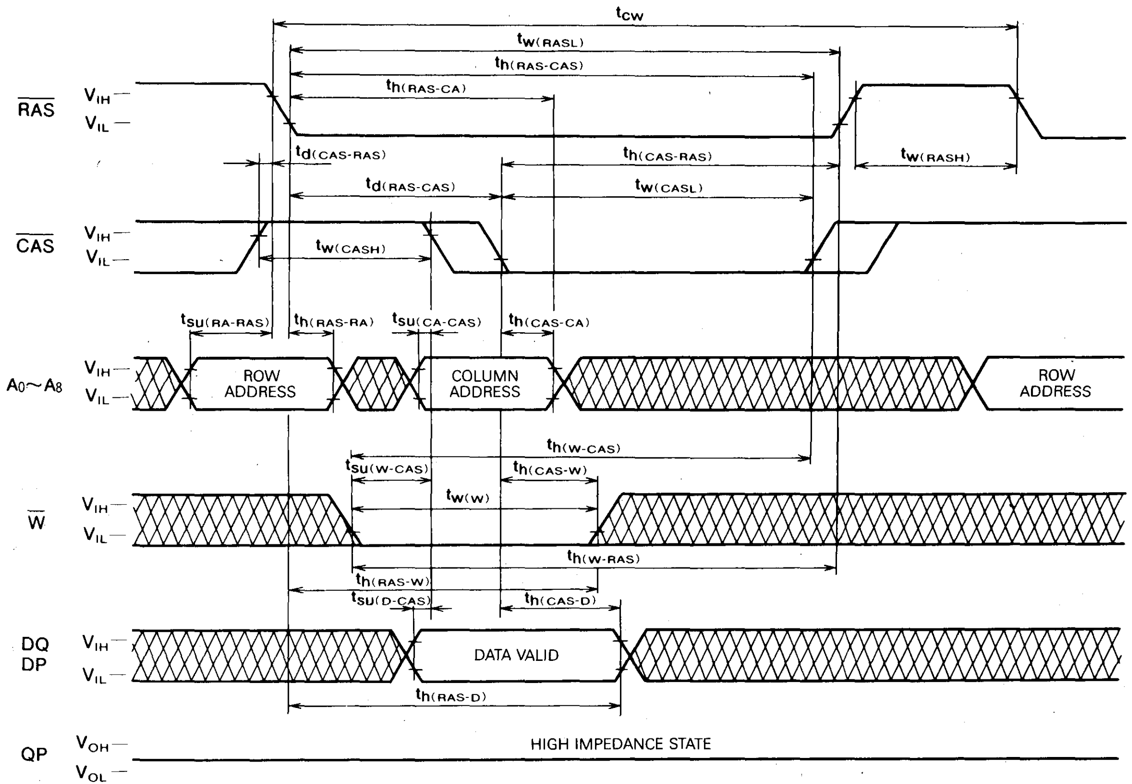
Note 16. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 17)

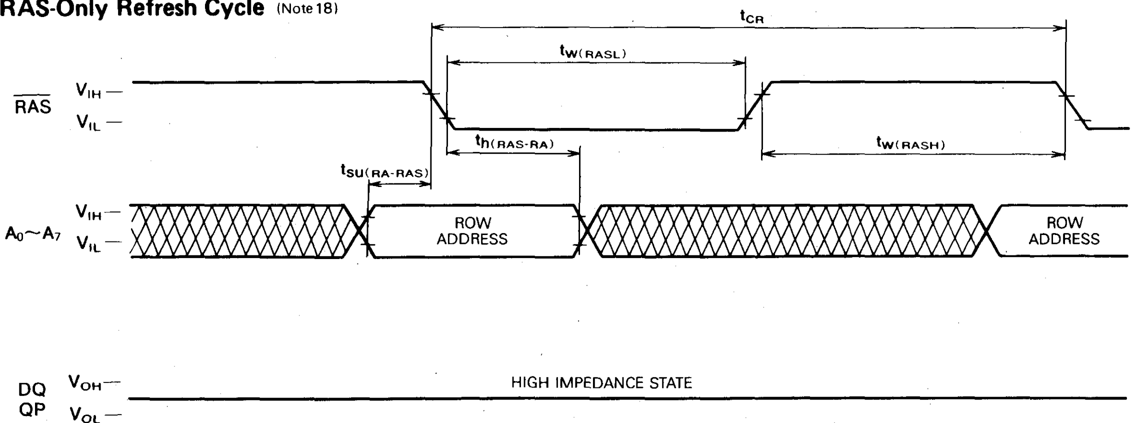
Read Cycle



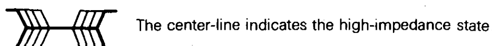
Early Write Cycle



RAS-Only Refresh Cycle (Note 18)

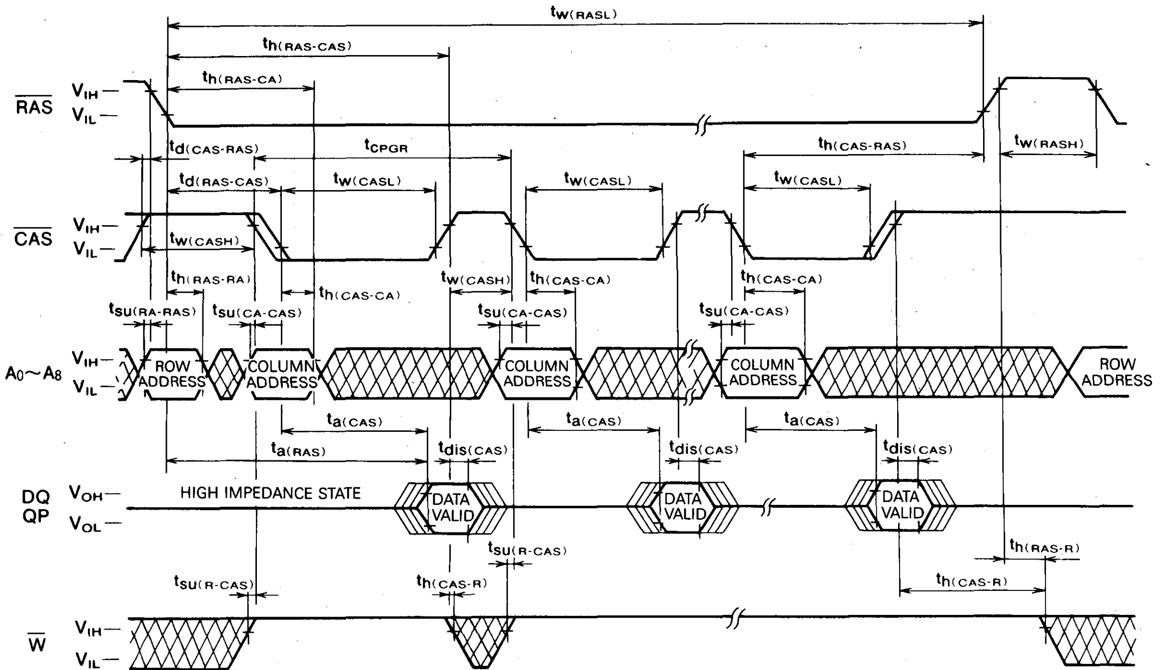


Note 17. Indicates the don't care input.

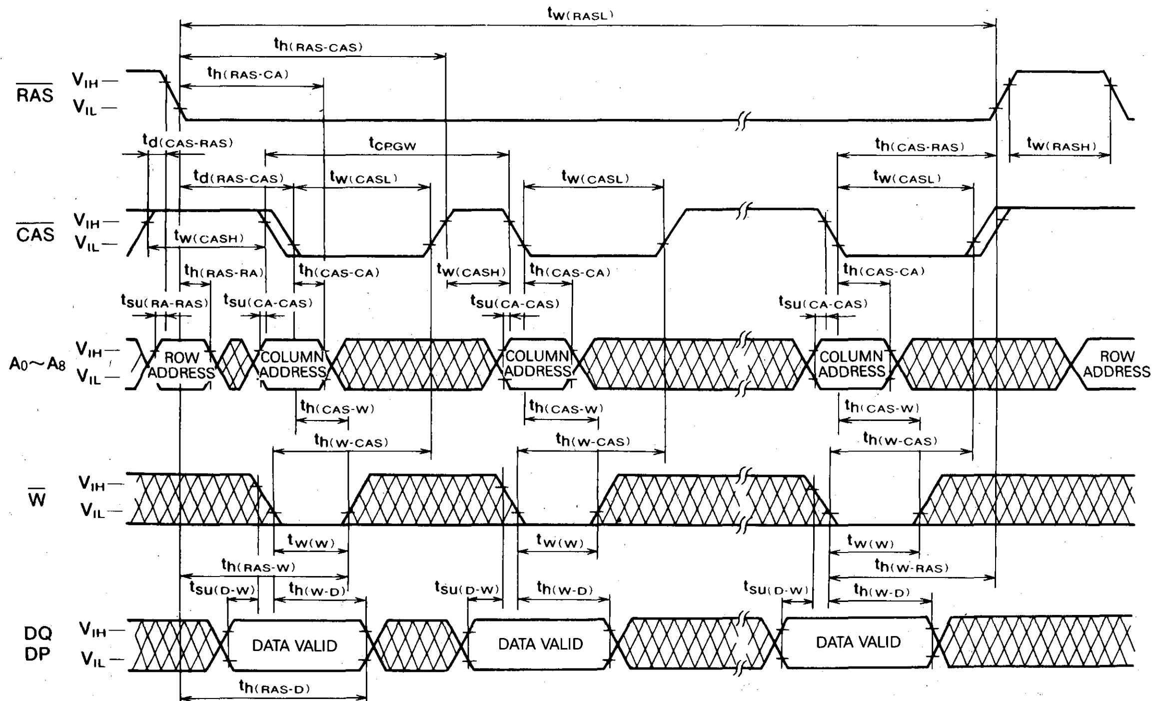
 The center-line indicates the high-impedance state.

Note 18. $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

Page-Mode Read Cycle

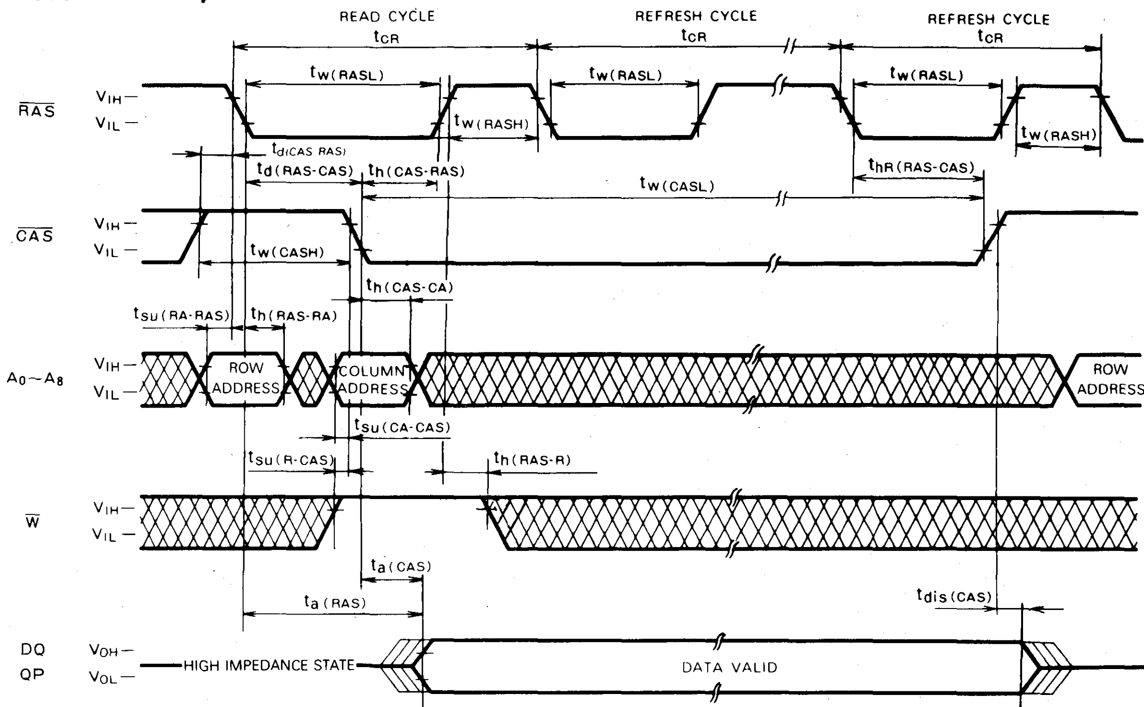


Page-Mode Write Cycle

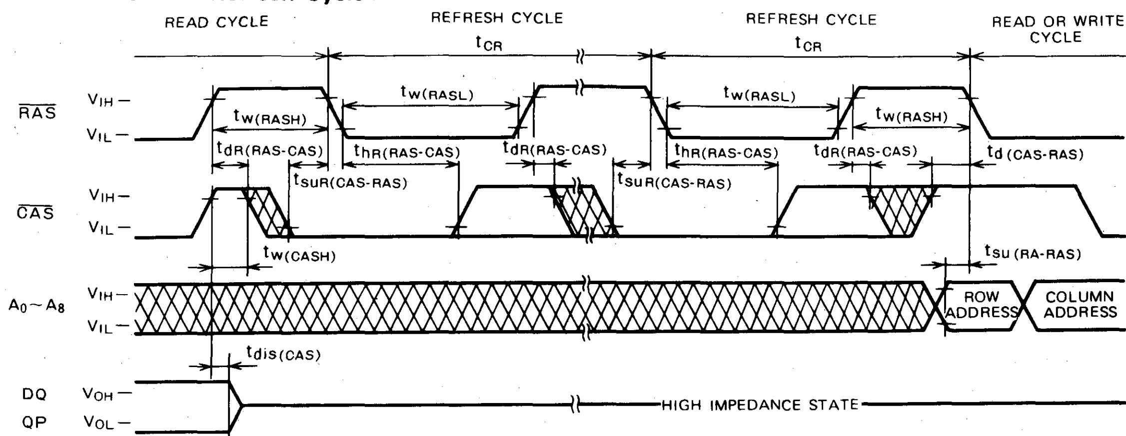


MITSUBISHI ELECTRIC

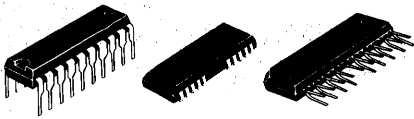
Hidden Refresh Cycle



CAS before RAS Refresh Cycle (Note 19)



Note 19 : $\overline{W}$, D = don't care.



M5M44C256P, J, L-10, -12, -15

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

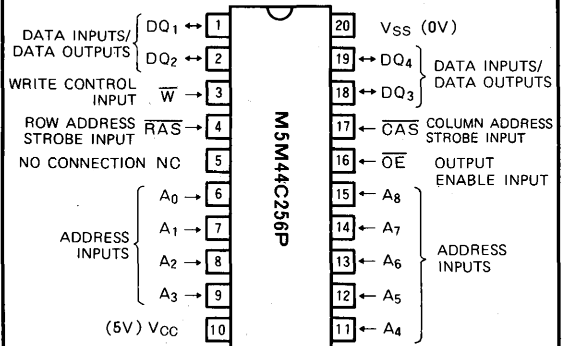
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ.mW)
M5M44C256P/J/L-10	100	25	50	25	190	300
M5M44C256P/J/L-12	120	30	55	30	220	250
M5M44C256P/J/L-15	150	40	70	40	260	200

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) .... CMOS Input level
- Low operating power dissipation
  M5M44C256P, J, L-10 .... 413mW (Max)
  M5M44C256P, J, L-12 .... 358mW (Max)
  M5M44C256P, J, L-15 .... 303mW (Max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{OE}$ control output buffer impedance
- Read-Modify-write, $\overline{RAS}$-only refresh, Fast-page mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- $\overline{CAS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ pulse width for Fast page mode . . 50μs max

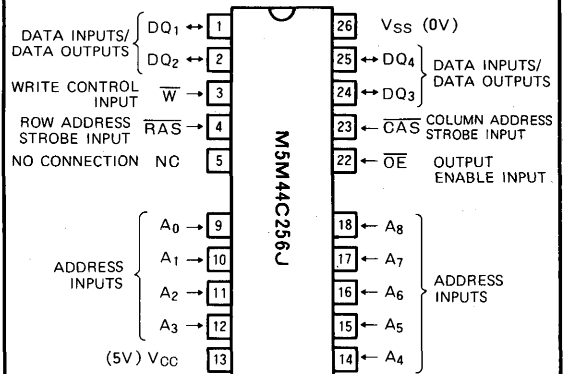
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

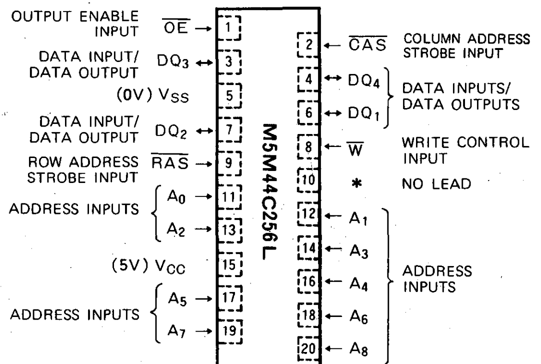
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

FUNCTION

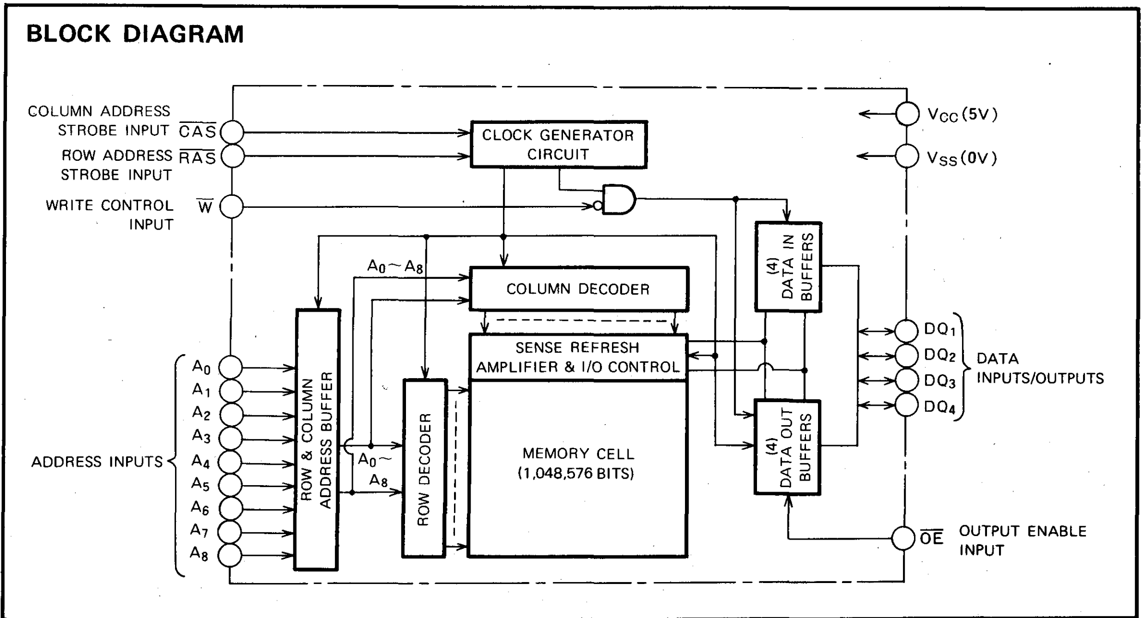
The M5M44C256P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM



FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits Min	Limits Nom	Limits Max	Unit
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{OH}	High-level output voltage		I_{OH}=−2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V. Other inputs pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M44C256-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$= min, output open			75	mA
		M5M44C256-12				65	
		M5M44C256-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CAS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CAS}=\overline{OE}\geqq V_{CC}-0.5$, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M44C256-10	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}= min, output open			75	mA
		M5M44C256-12				65	
		M5M44C256-15				55	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M44C256-10	$\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling t_{PC}= min, output open			65	mA
		M5M44C256-12				55	
		M5M44C256-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44C256-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}= min, output open			75	mA
		M5M44C256-12				65	
		M5M44C256-15				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M44C256-10		M5M44C256-12		M5M44C256-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column Address access time	(Note 6, 9)		50		55		70	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		55		60		75	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		25		30		40	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 11)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after pro-longed periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 12, 13)

Symbol	Parameter		Limits						Unit
			M5M44C256-10		M5M44C256-12		M5M44C256-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	20	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		20		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low		95		110		135		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed t_T = 5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 7, 9.
15: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of fast page mode cycle.
17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
18: $t_{ASC(max)}$ is specified as a reference point only of address access time.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44C256-10		M5M44C256-12		M5M44C256-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	50		55		70		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	25		30		40		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44C256-10		M5M44C256-12		M5M44C256-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	95		115		140		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	20		25		30		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	95		115		140		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to data	20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	20		25		30		ns

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44C256-10		M5M44C256-12		M5M44C256-15		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	245		285		335		ns
t_{RAS}	$\overline{RAS}$ low pulse width	155	10000	185	10000	225	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	80	10000	95	10000	115	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	155		185		225		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	80		95		115		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low (Note 22)	50		60		75		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 22)	125		150		185		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	20		25		30		ns
t_{AWD}	Delay time, address to write low (Note 22)	75		85		105		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	20		25		30		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M44C256-10		M5M44C256-12		M5M44C256-15		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Read, Write cycle time	60		65		80		ns
t_{RWPC}	Read write/read modify write cycle time	110		120		145		ns
t_{RAS}	$\overline{RAS}$ low pulse width for Read, write cycle	155	50000	175	50000	220	50000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle	25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 23)	15	25	15	25	20	30	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns

Note 23: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

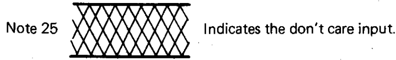
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44C256-10		M5M44C256-12		M5M44C256-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

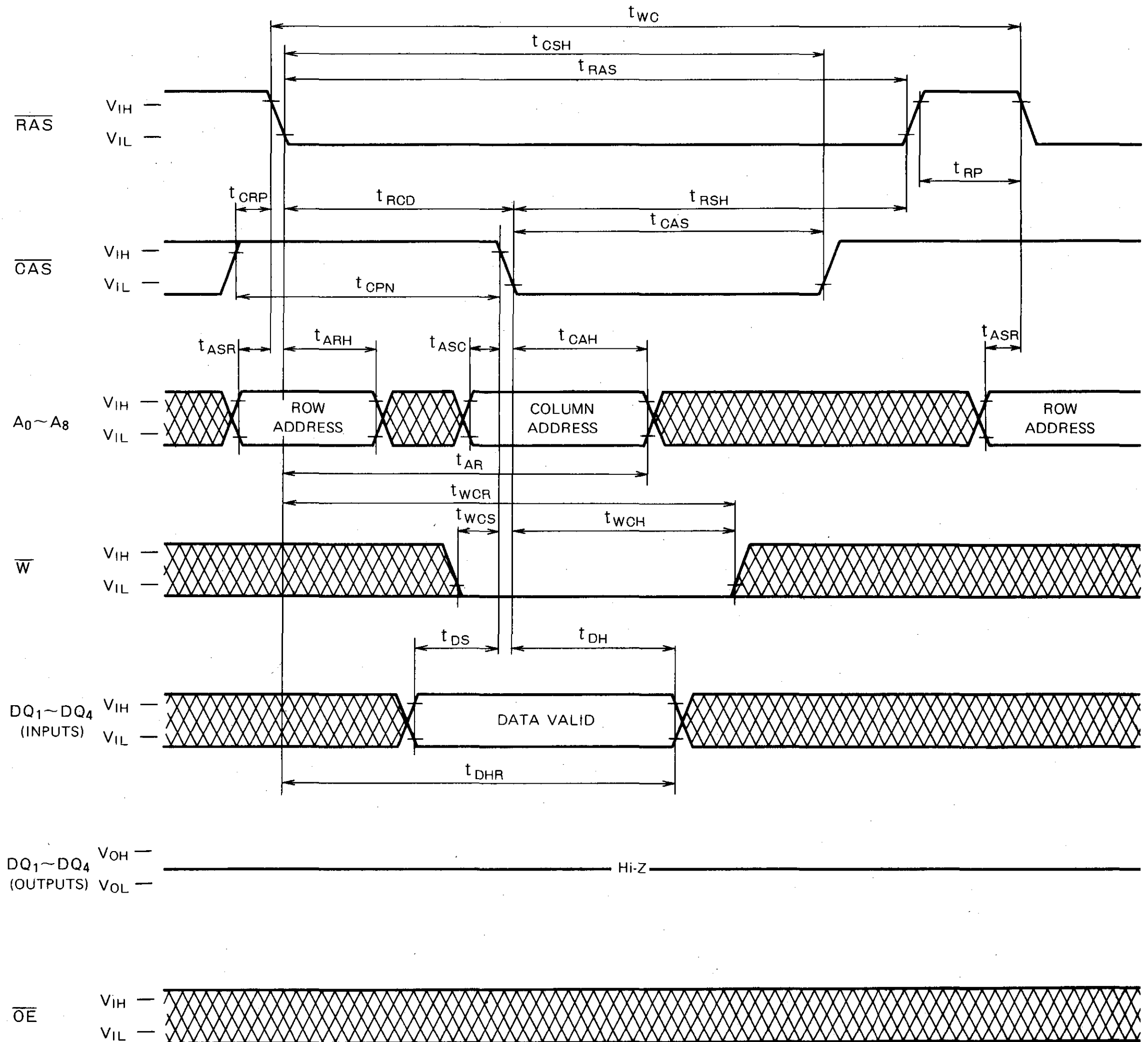
Note 24: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 25)

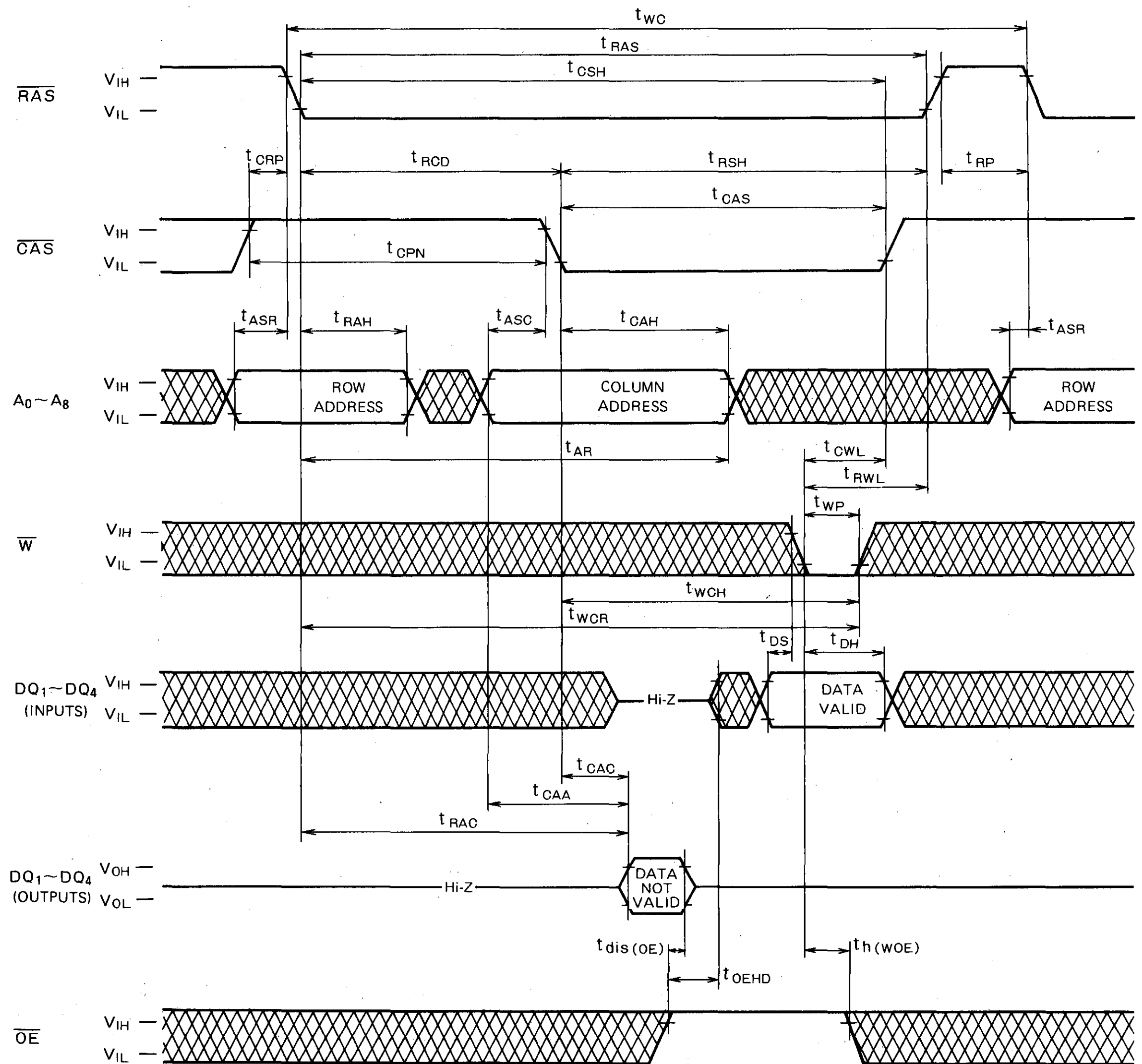
Read Cycle

Note 25  Indicates the don't care input.

Write Cycle (Early write)

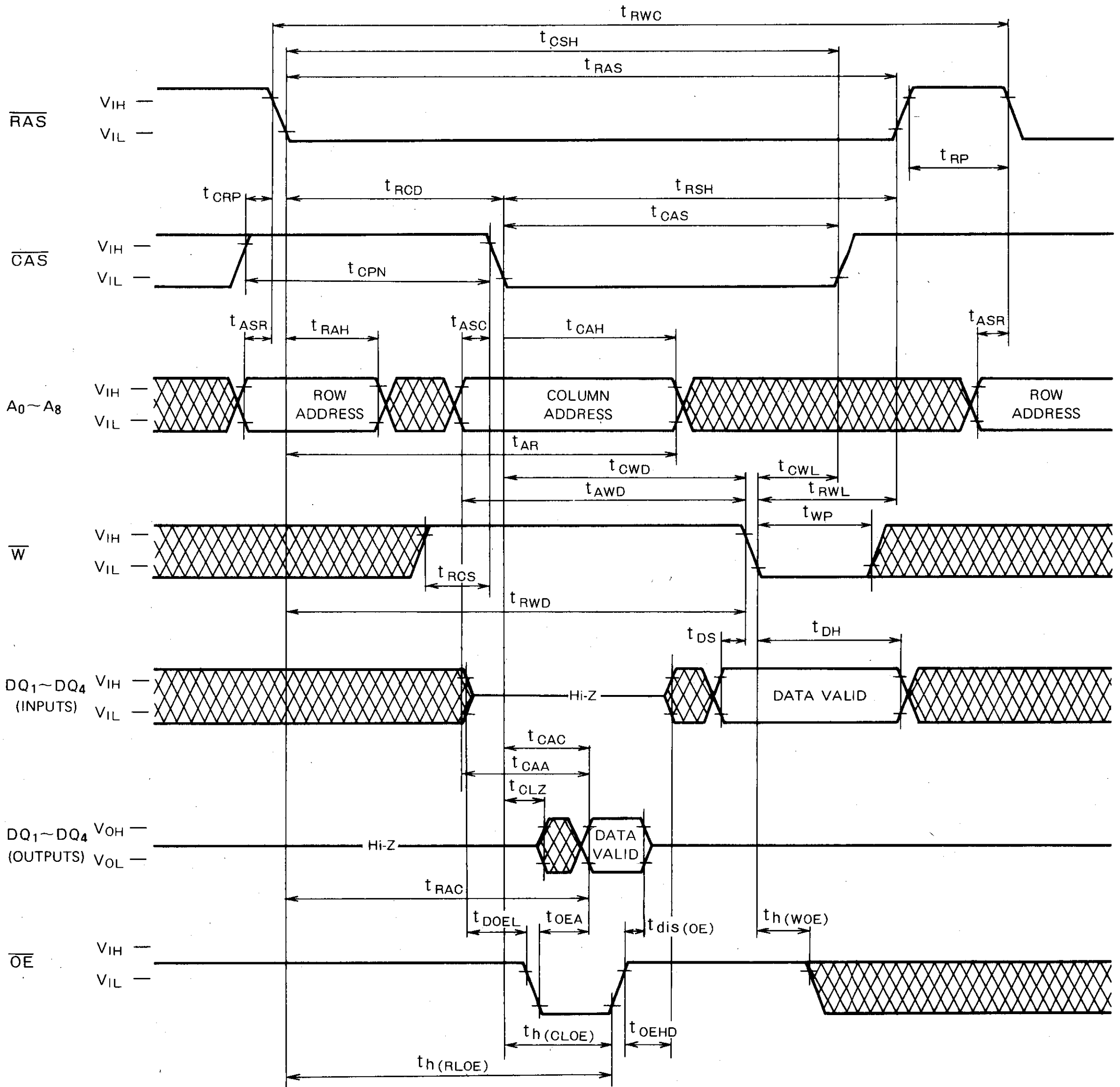


Write Cycle (Delayed Write)

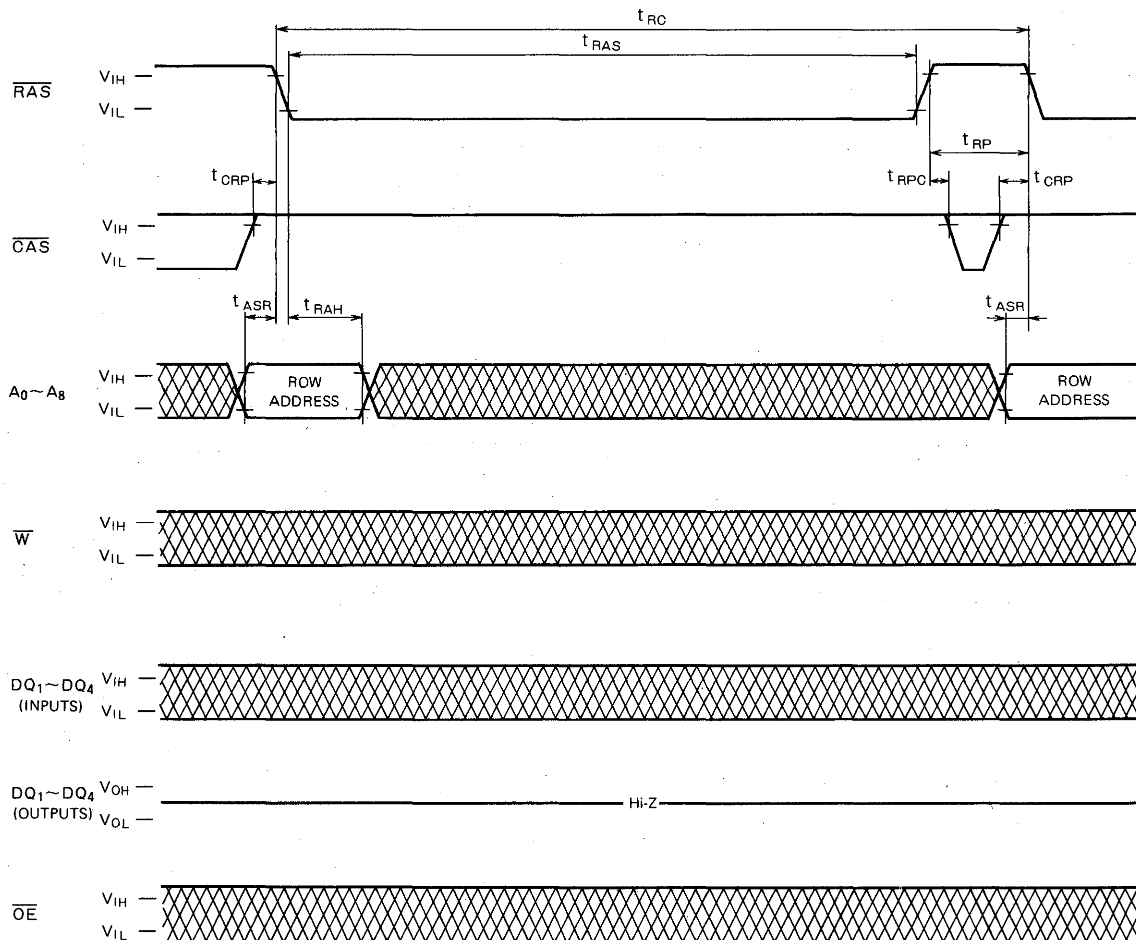


MITSUBISHI ELECTRIC

Read-Write, Read-Modify-Write Cycle

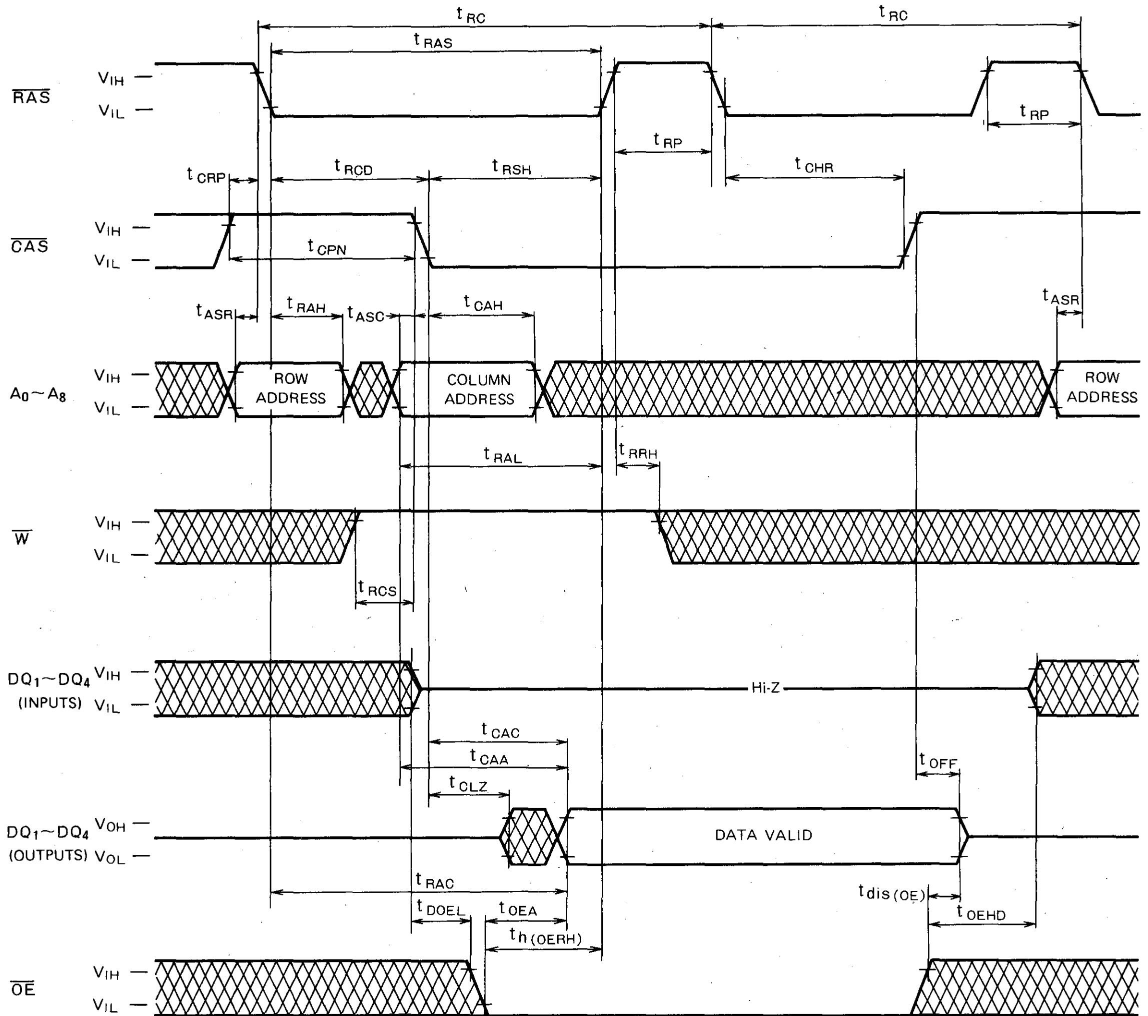


$\overline{RAS}$-only Refresh Cycle

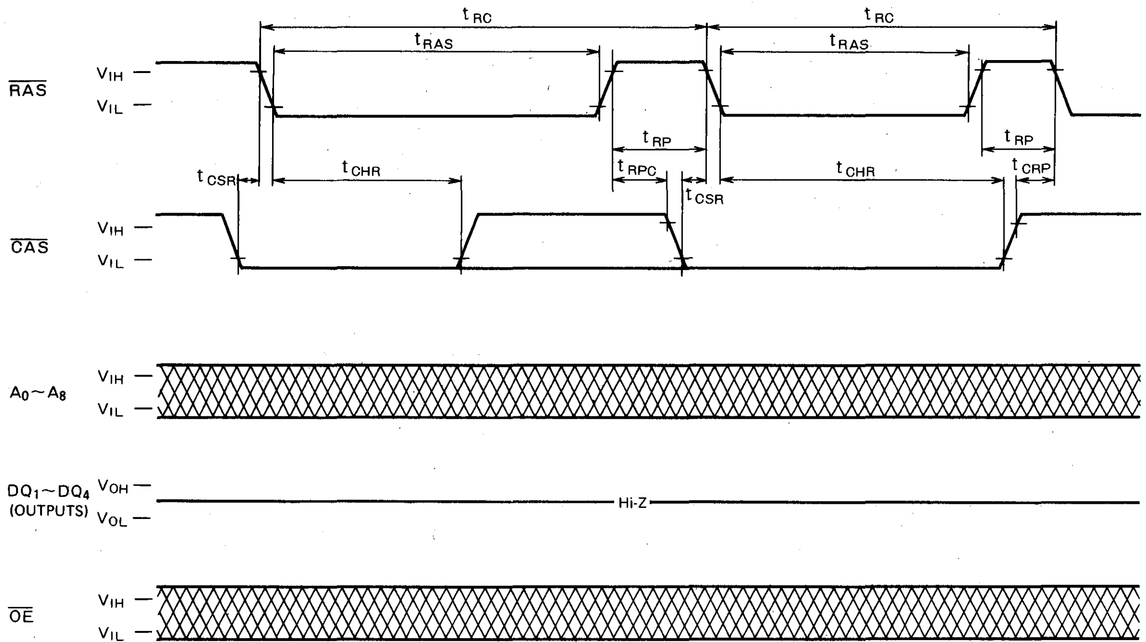


MITSUBISHI ELECTRIC

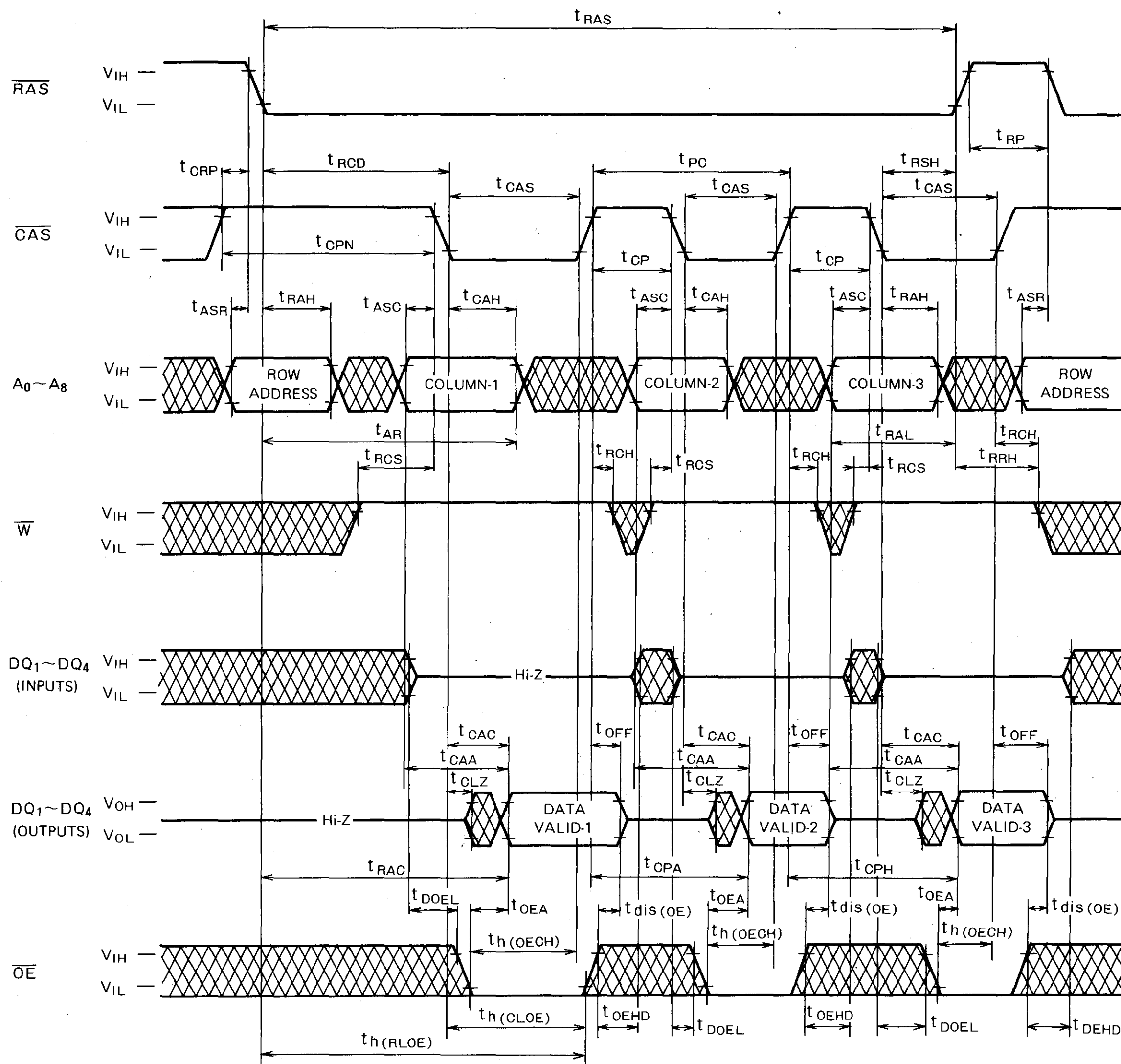
Hidden Refresh Cycle



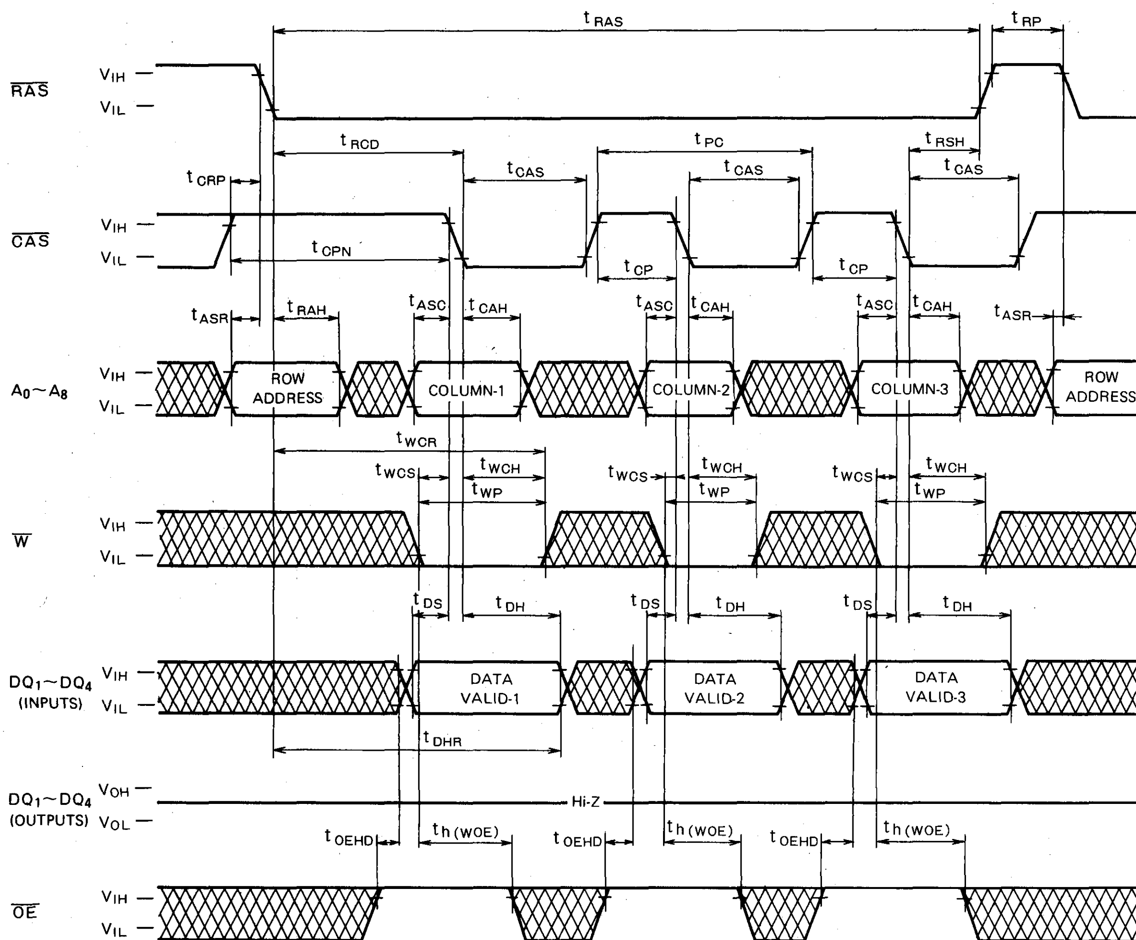
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Fast Page Mode Read Cycle

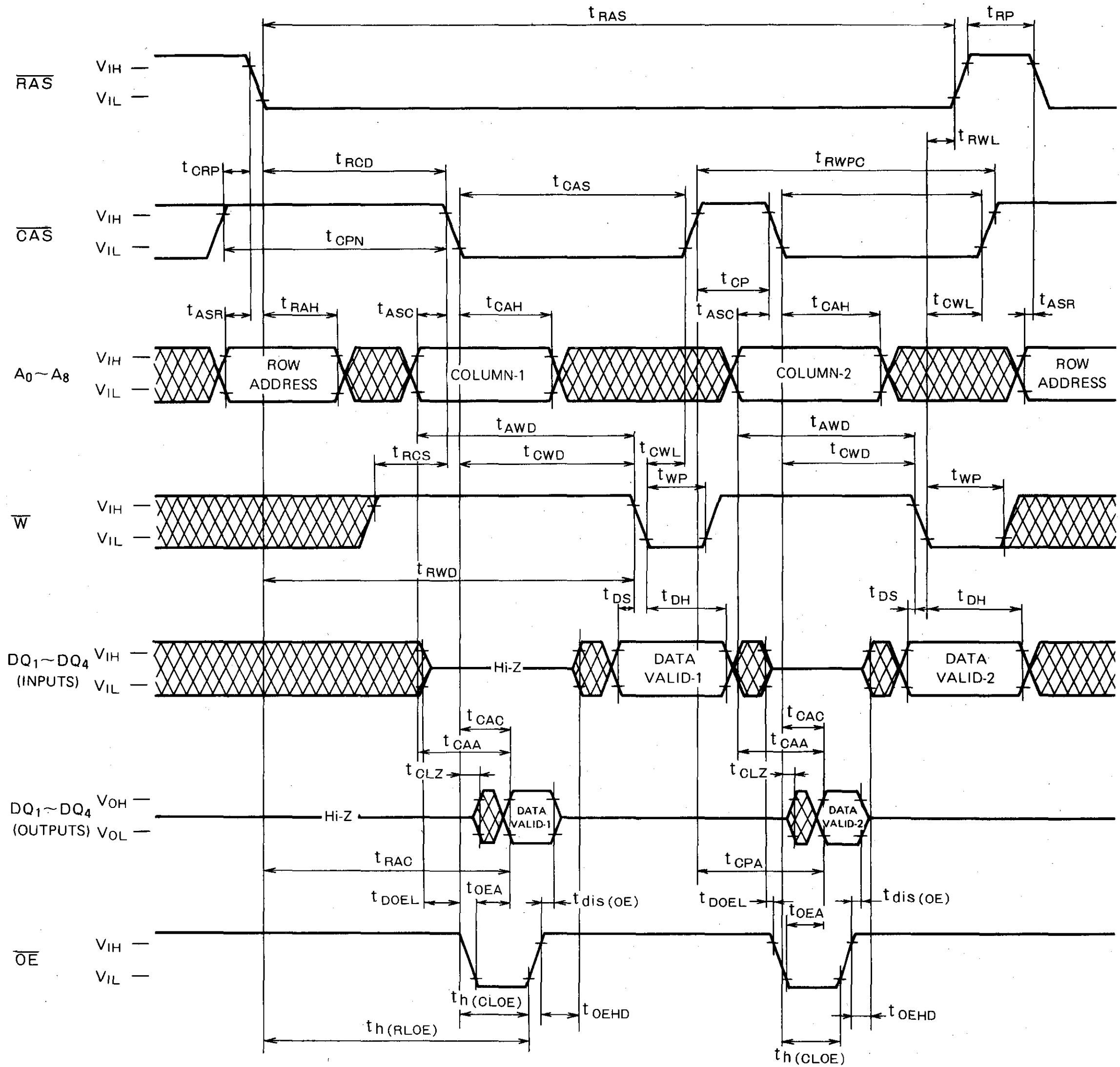


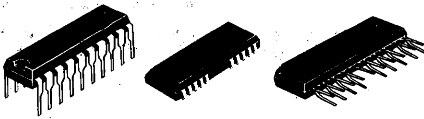
Fast Page Mode Write Cycle



MITSUBISHI ELECTRIC

Fast Page Mode Read-Write, Read-Modify-Write Cycle





M5M44C258P, J, L-10, -12, -15

STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

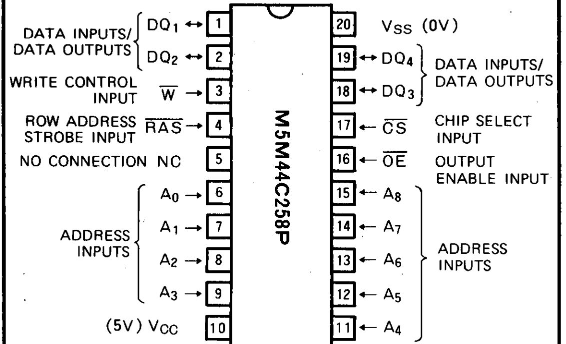
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ.mW)
M5M44C258P/J/L-10	100	25	50	25	190	300
M5M44C258P/J/L-12	120	30	55	30	220	250
M5M44C258P/J/L-15	150	40	70	40	260	200

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . CMOS Input level
- Low operating power dissipation
  M5M44C258P, J, L-10 . . . . 413mW (Max)
  M5M44C258P, J, L-12 . . . . 358mW (Max)
  M5M44C258P, J, L-15 . . . . 303mW (Max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{OE}$ control output buffer impedance
- Read-Modify-write, $\overline{RAS}$-only refresh, Static column mode capabilities
- $\overline{CS}$ before $\overline{RAS}$ refresh mode capability
- $\overline{CS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ pulse width for Static column mode . . . . 50μs max

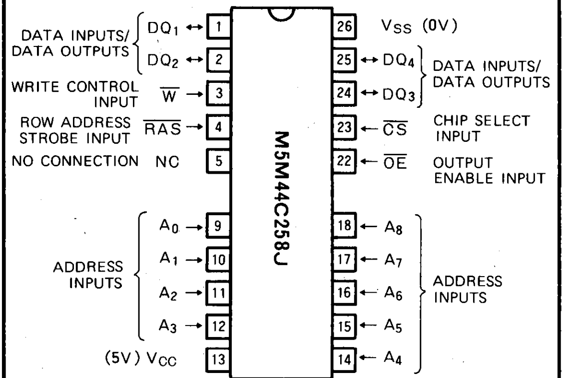
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

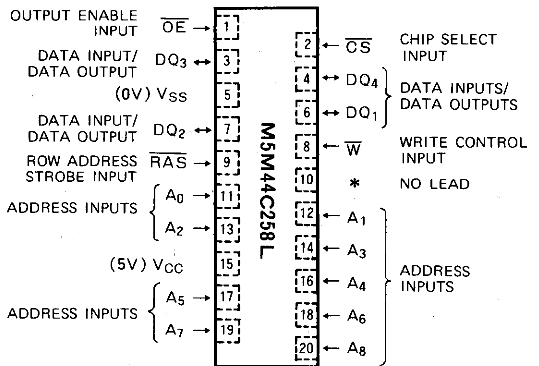
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

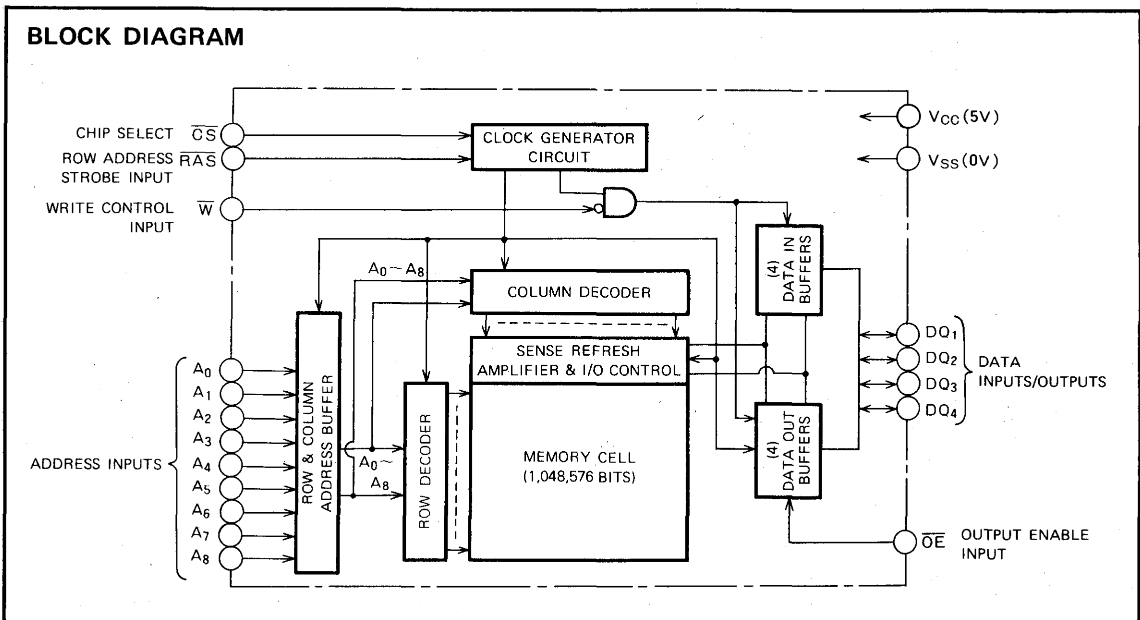
FUNCTION

The M5M44C258P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., static column mode, RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	CS	W	OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Note.
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
CS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open
Static column mode is identical except early write.



STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		$I_{OH}=-2mA$	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		$I_{OL}=4.2mA$	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V \leqq V_{OUT} \leqq 5.5V$	−10		10	μA
I_I	Input current		$0V \leqq V_{IH} \leqq 6.5V$, Other inputs pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M44C258-10	$\overline{RAS}$, $\overline{CS}$ cycling $t_{RC}=t_{WC}=$ min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CS}=\overline{OE} \geqq V_{CC}-0.5$, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M44C258-10	$\overline{RAS}$ cycling, $\overline{CS}=V_{IH}$ $t_{RC}=$ min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44C258-10	$\overline{CS}$ before $\overline{RAS}$ refresh cycling $t_{RC}=$ min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
$I_{CC7(AV)}$	Average supply current from V_{CC}, Static Column mode (Note 3, 4)	M5M44C258-10	$\overline{RAS}=V_{IL}$, Column address cycling $t_{SC}=$ min, output open			65	mA
		M5M44C258-12				55	
		M5M44C258-15				45	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC6(AV)}$ and $I_{CC7(AV)}$ are dependent on cycle rate, maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC7(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CS})}$	Input capacitance, $\overline{CS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance data ports				7	pF

STATIC CLOUMN MODE 1048576 BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column Address access time	(Note 6, 9)		50		55		70	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		25		30		40	ns
t_{WRA}	Access time from $\overline{W}$ high	(Note 6)		60		65		80	ns
t_{OFF}	Output disable time after $\overline{CS}$ high	(Note 10)	0	20	0	25	0	30	ns
t_{CLZ}	Output low impedance time from $\overline{CS}$ low	(Note 6)	5		5		5		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 10)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD} \geqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then t_{RAC} will increase by the amount that t_{RCD} or t_{RAD} exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Static Column Cycles)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 11, 12)

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CS}$ low	(Note 13)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CS}$ high to $\overline{RAS}$ low	(Note 14)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 15)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CS}$ low		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CS}$ low or $\overline{W}$ low		20		20		25		ns
t_T	Transition time	(Note 17)	3	50	3	50	3	50	ns

Note 11: The timing requirements are assumed $t_T = 5ns$.
12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
13: $t_{RCD(max)}$ is specified as a reference point only; If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is $t_{RCD} + t_{CAC}$. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH} + 2t_T + t_{ASC}$.
14: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles.
15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of static column mode cycle.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CS}$ high (Note 18)	10		10		10		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	50		55		70		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	15		15		15		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low	25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(OECH)}$	$\overline{CS}$ hold time after $\overline{OE}$ low	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	25		30		40		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{CWL}	$\overline{CS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{WCS}	Write setup time before $\overline{CS}$ low (Note 20)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CS}$ low	20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	95		115		140		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	15		15		15		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CS}$ low	20		25		30		ns
t_{AWR}	Address hold time after $\overline{RAS}$ low	95		110		135		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	95		115		140		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	20		25		30		ns

STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 19)	245		285		335		ns
t_{RAS}	$\overline{RAS}$ low pulse width	155	10000	185	10000	225	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	80	10000	95	10000	115	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	155		185		225		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	80		95		115		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CS}$ low to write low (Note 20)	50		60		75		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 20)	125		150		185		ns
t_{CWL}	$\overline{CS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	20		25		30		ns
t_{AWD}	Delay time, address to write low (Note 20)	75		85		105		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low	25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	20		25		30		ns

Note 19: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

20: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{CS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Static Column Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{RSC}	SC read cycle time	55		60		75		ns
t_{WSC}	SC write cycle time	55		60		75		ns
t_{RWSC}	SC R/W, R/M/W, cycle time	115		130		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width	155	50000	180	50000	225	50000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CS}$ high pulse width	15		15		20		ns
t_{RSW}	Delay time, $\overline{RAS}$ to 2nd Write low	115		135		165		ns
t_{WI}	Write invalid time	15		15		20		ns
t_{WHRW}	Write high pulse width for R/W, R/M/W, cycle	85		95		115		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{AOH}	Data hold time from address change	10		10		10		ns
t_{WAD}	Delay time write to address change (Note 21)	−10	10	−10	10	−10	10	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
$t_{h(WHOE)}$	$\overline{OE}$ hold time after write high	60		65		80		ns

Note 21: $t_{WAD(max)}$ is specified as a reference point only. If $t_{WAD} \geqq t_{WAD(max)}$, access time is assumed by t_{CAA}.

$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns

Note 22: Eight or more $\overline{CS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CS}$ before $\overline{RAS}$ refresh mode.

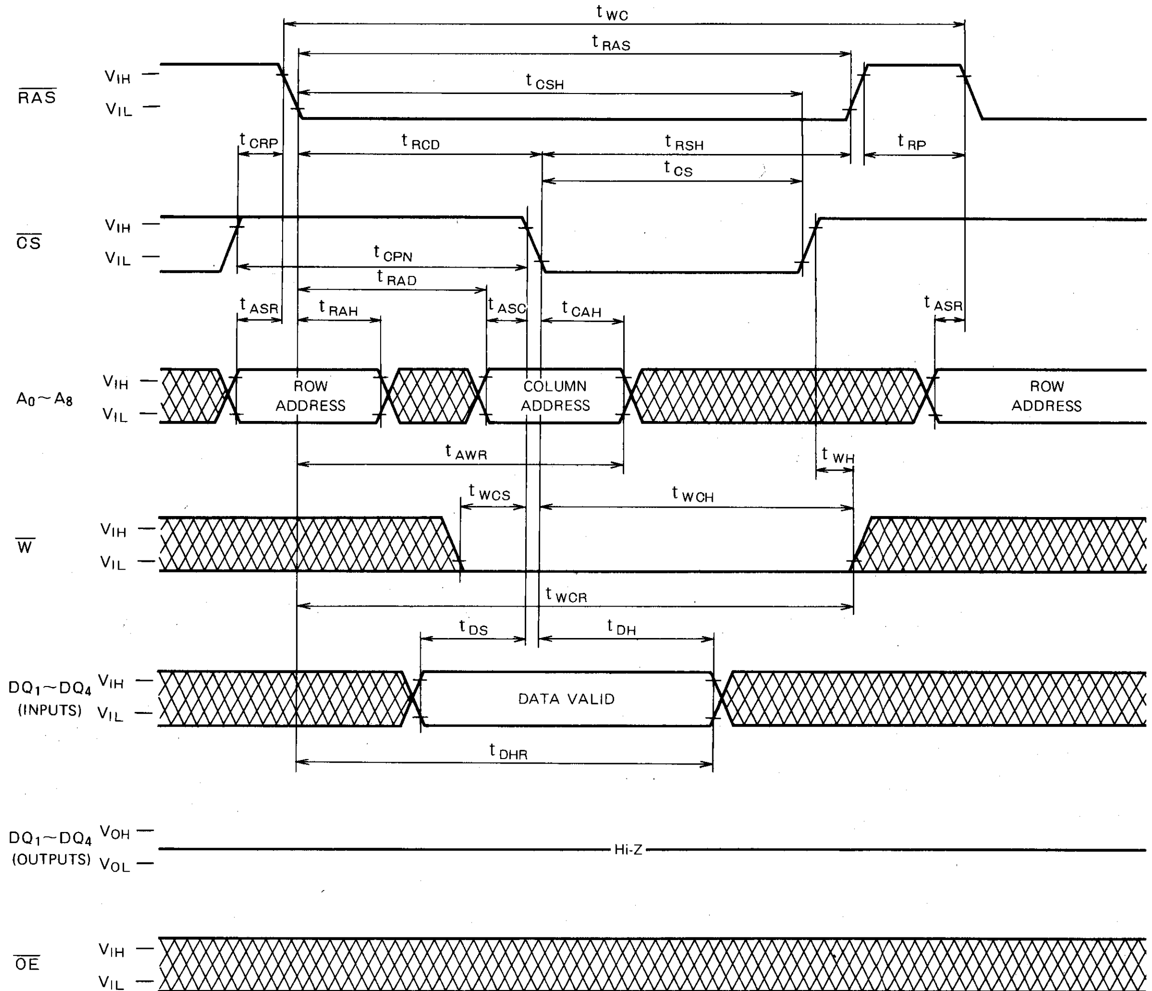
Timing Diagrams (Note 23)

Read Cycle

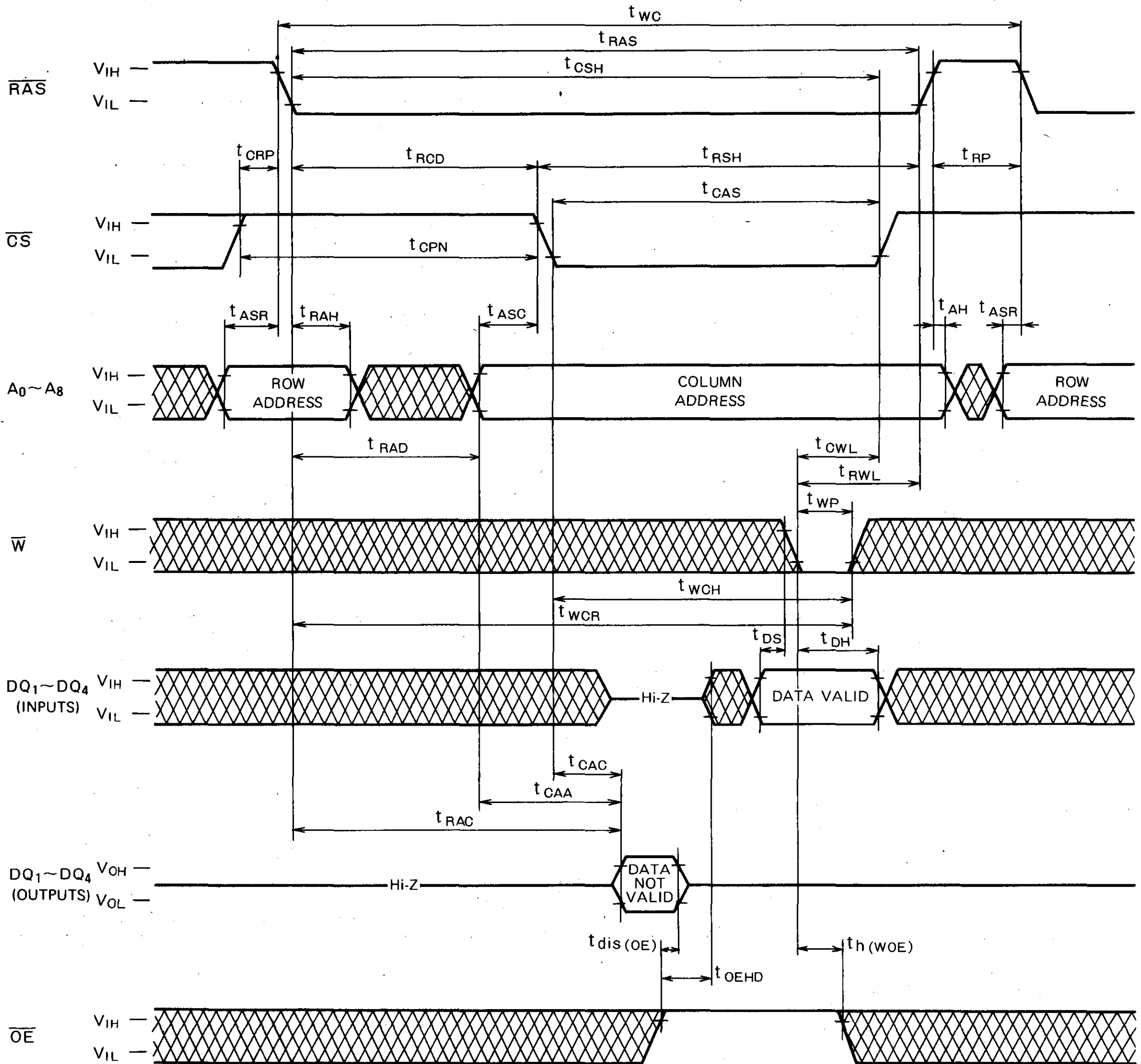
t_{RC}
t_{RCD}
t_{RAS}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{RP}
t_{CRP}
t_{CS}
$\overline{CS}$ V_{IH} — V_{IL} —
t_{CPN}
t_{ASR} t_{RAH}
t_{RAD}
t_{RAL}
t_{AH}
t_{ASR}
$A_0 \sim A_8$ V_{IH} — V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
t_{RRH}
t_{RCS}
t_{RCH}
$\overline{W}$ V_{IH} — V_{IL} —
$DQ_1 \sim DQ_4$ (INPUTS) V_{IH} — V_{IL} —
Hi-Z
t_{CAC}
t_{OFF}
t_{CLZ}
$DQ_1 \sim DQ_4$ (OUTPUTS) V_{OH} — V_{OL} —
DATA VALID
t_{CAA}
t_{RAC}
$t_{dis(OE)}$
t_{DOEL}
t_{OEHD}
t_{OEA}
$t_{h(OECH)}$
$t_{h(OERH)}$
$\overline{OE}$ V_{IH} — V_{IL} —
$t_{h(CLOE)}$
$t_{h(RLOE)}$

Note 23 Indicates the don't care input.

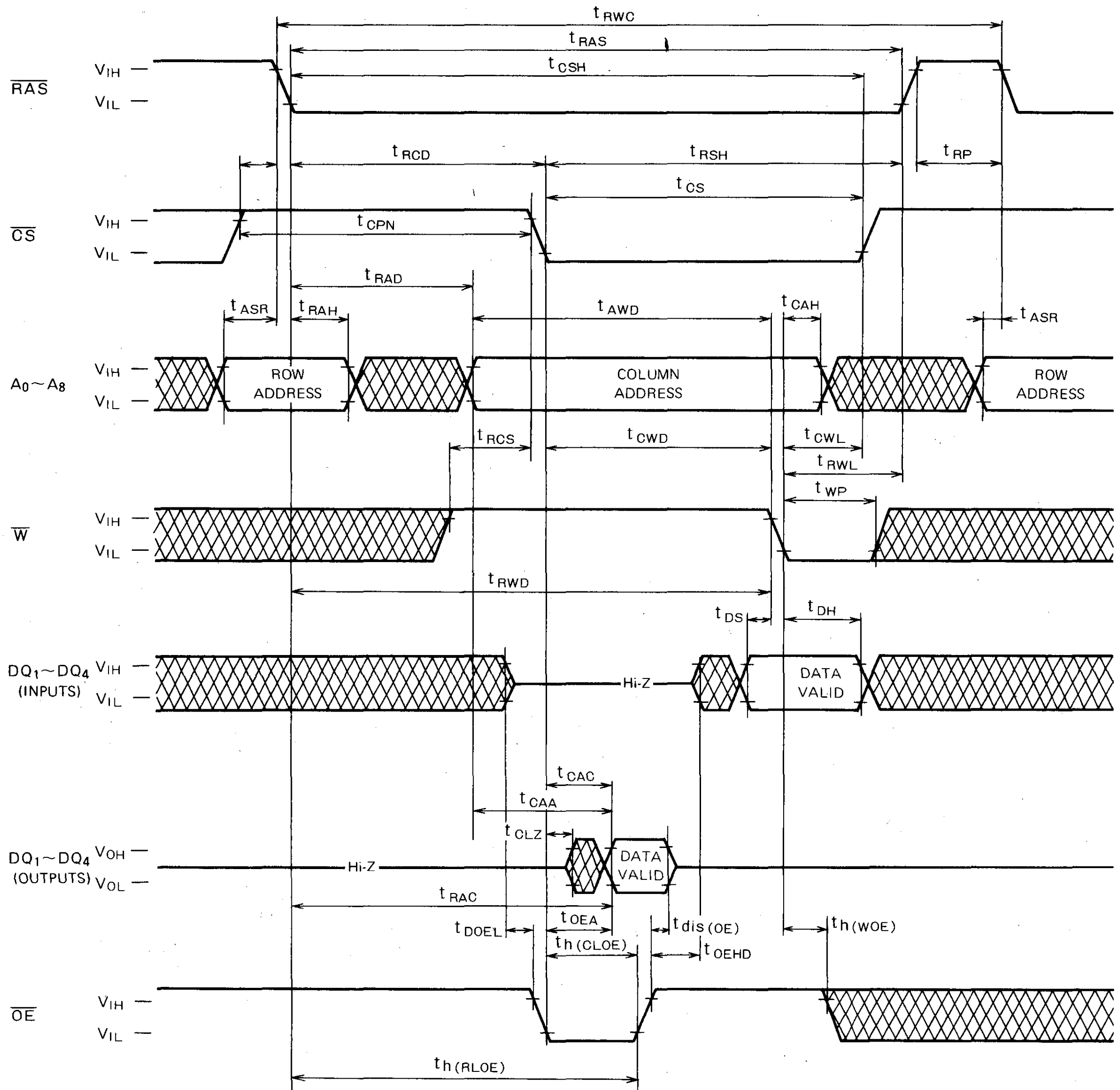
Write Cycle (Early write)



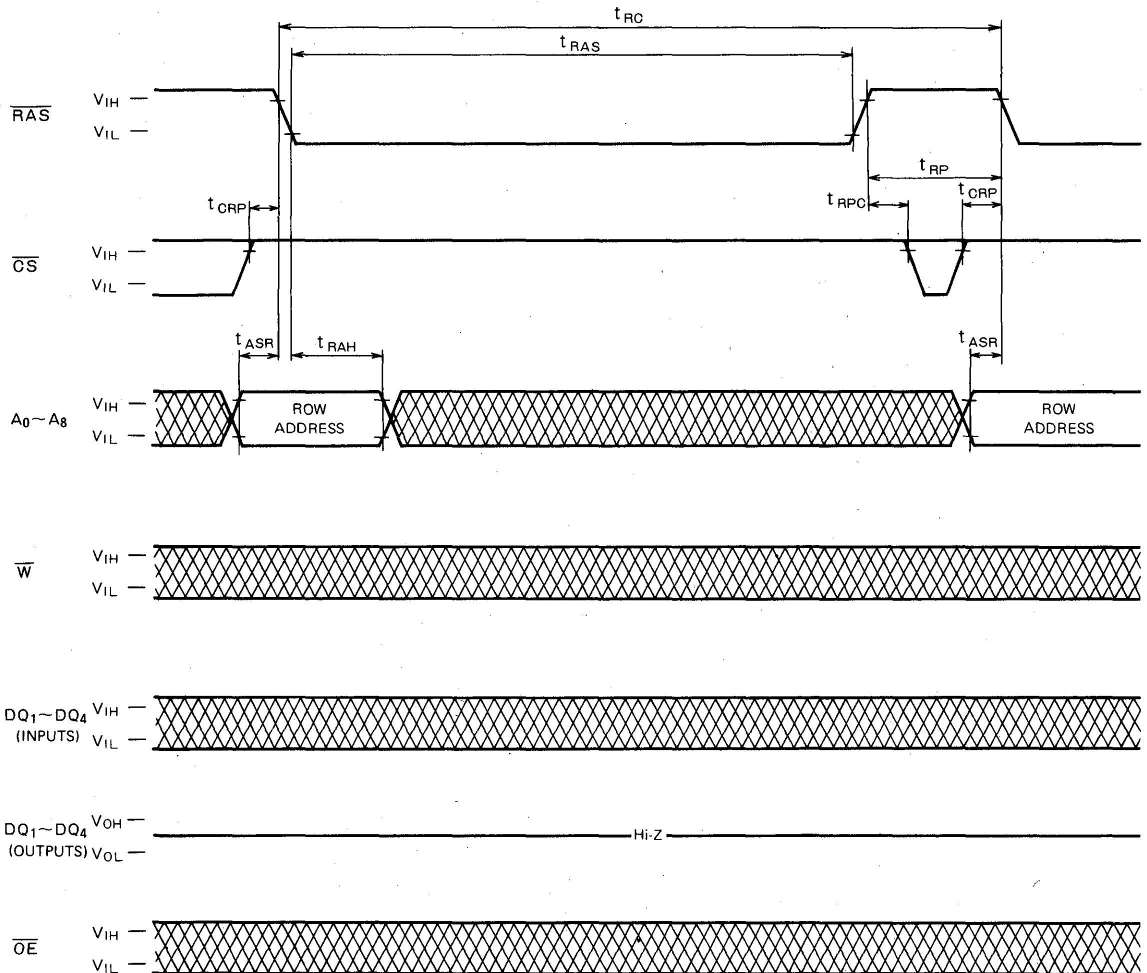
Write Cycle (Delayed Write)



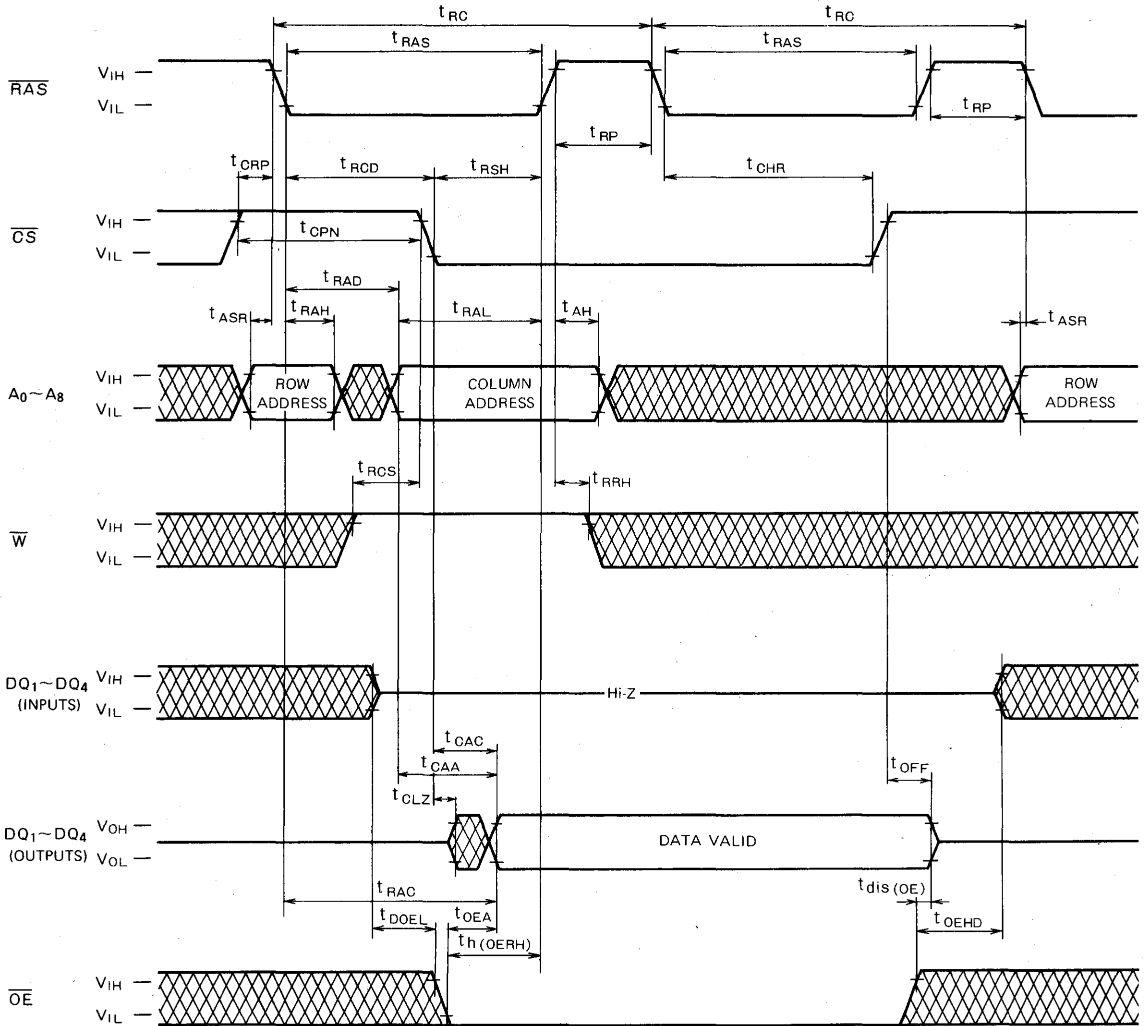
Read-Write, Read-Modify-Write Cycle



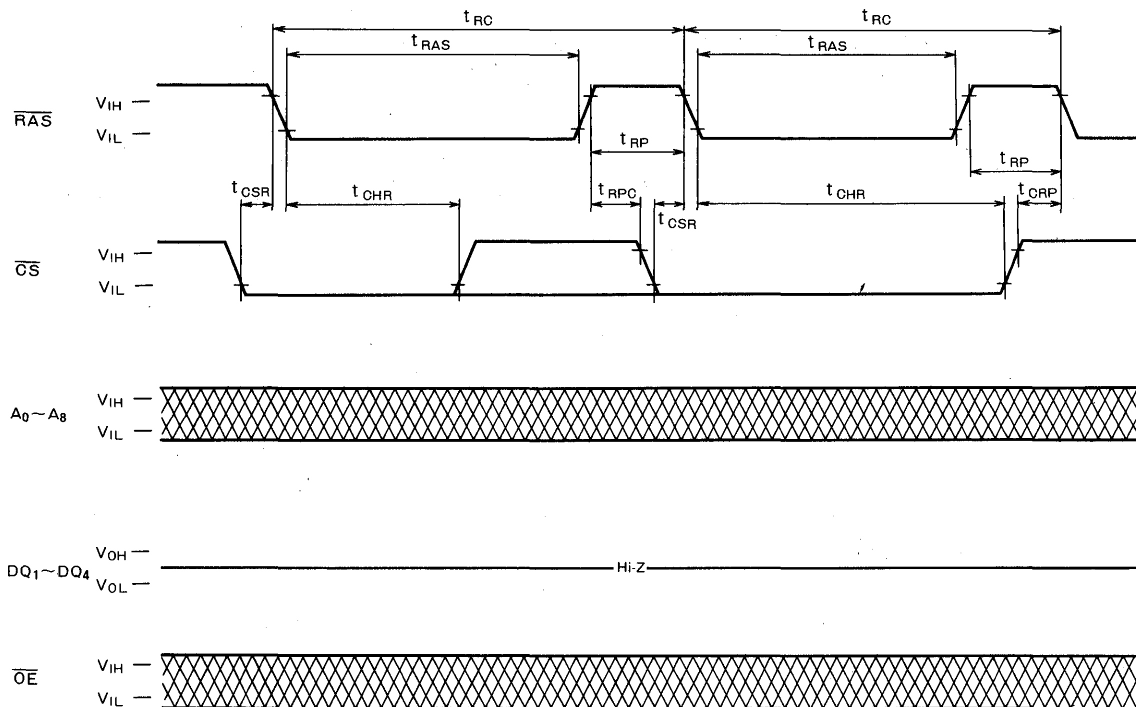
$\overline{RAS}$-only Refresh Cycle



Hidden Refresh Cycle

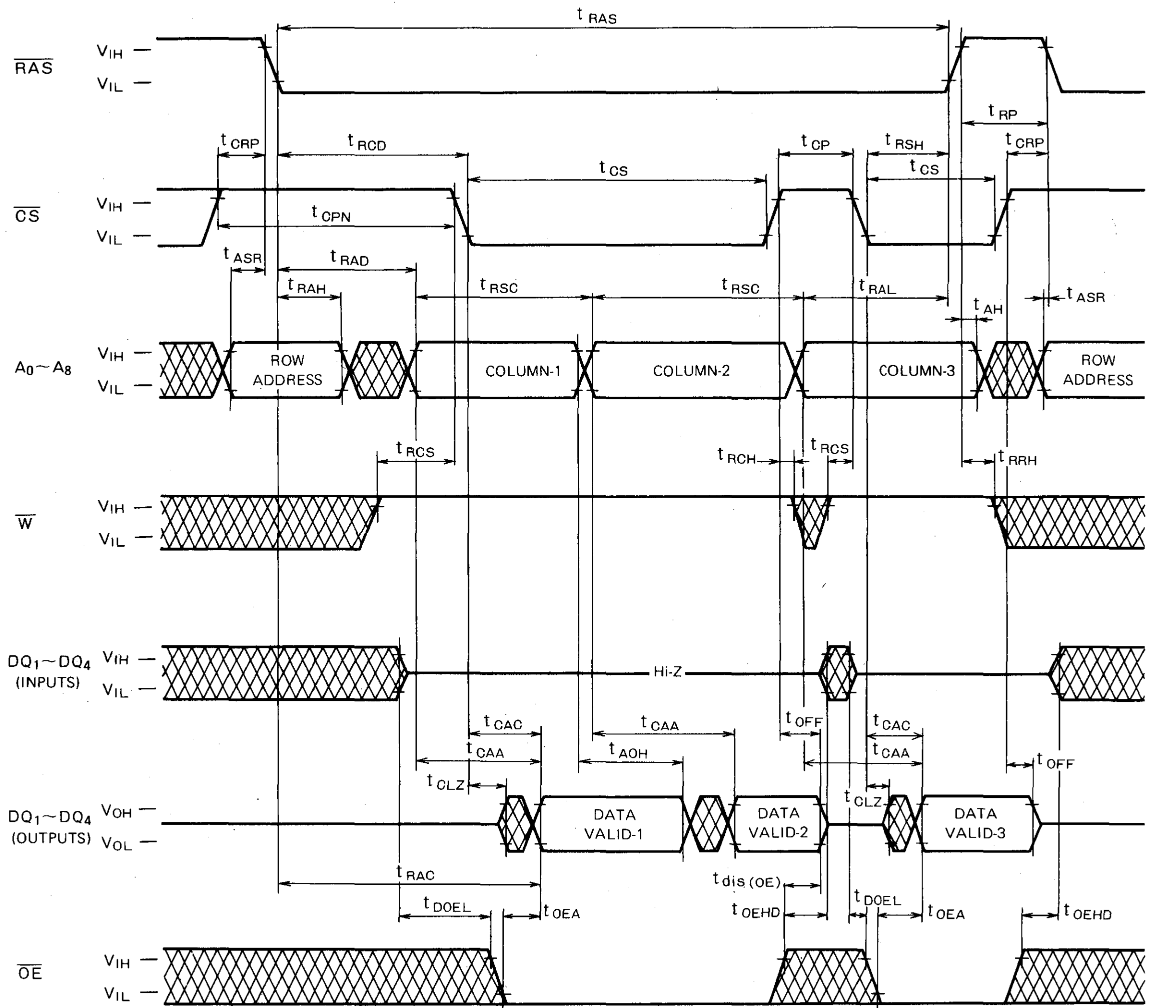


$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

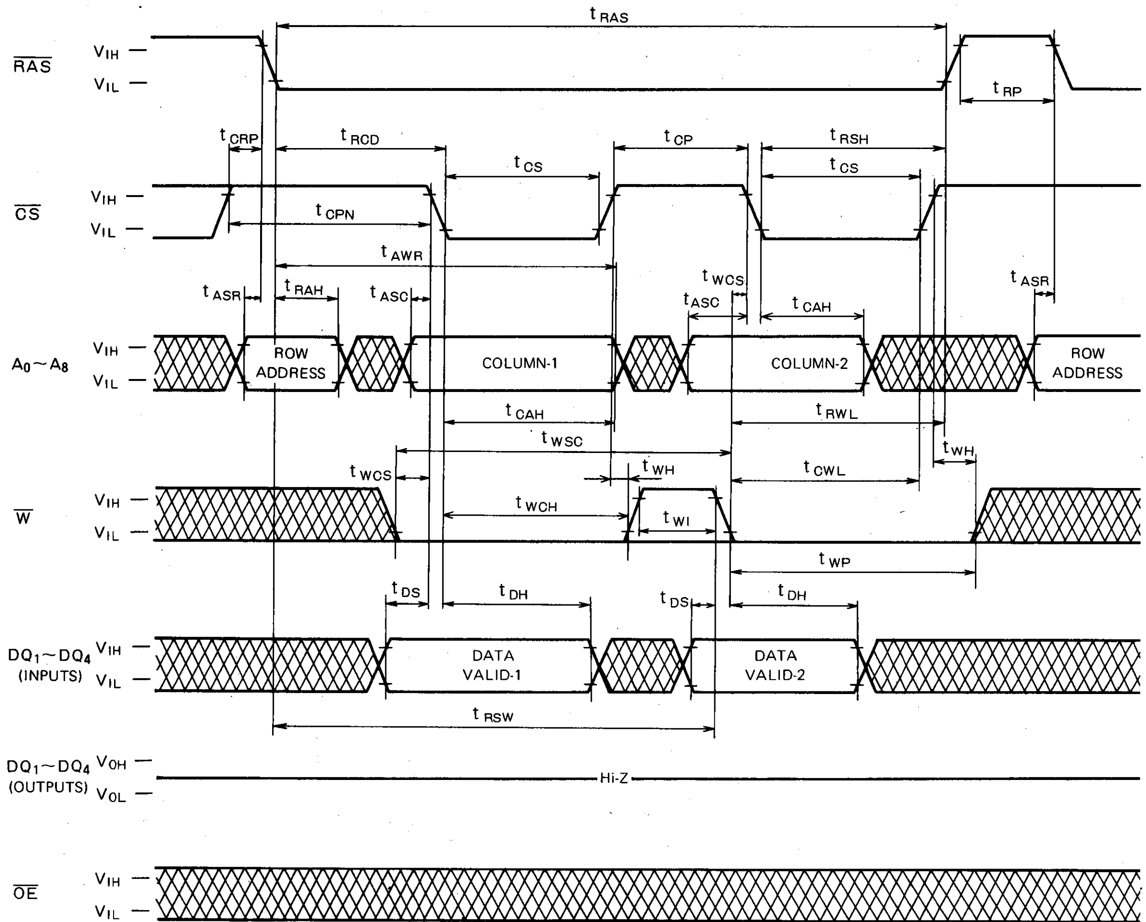


MITSUBISHI ELECTRIC

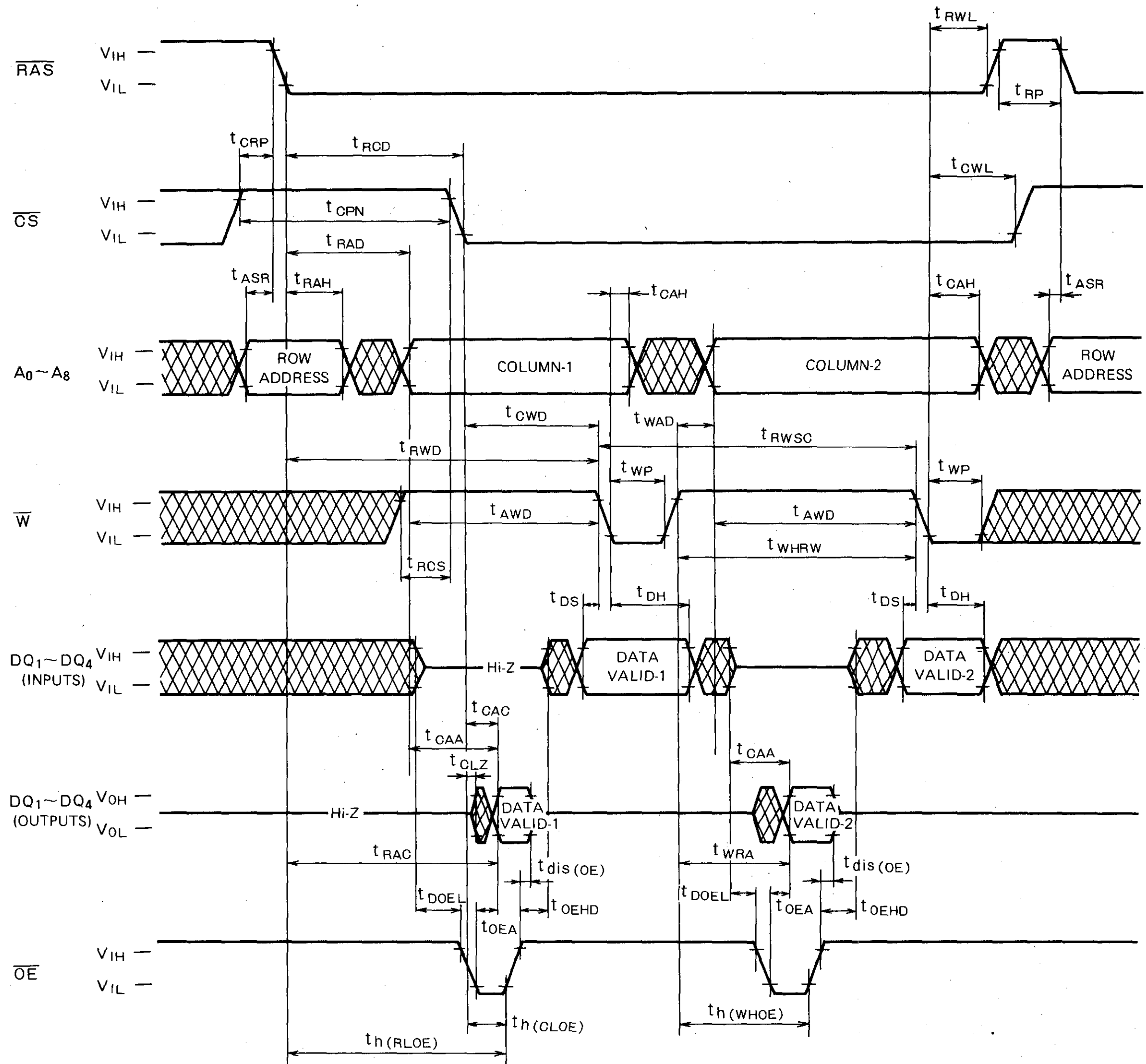
Static Column Mode Read Cycle

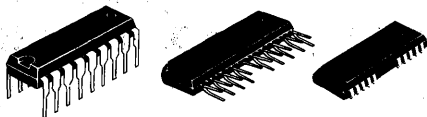


Static Column Mode Early Write Cycle



Static Column Mode Read-Write, Read-Modify-Write Cycle





M5M4C1000P, J, L-10, -12, -15

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

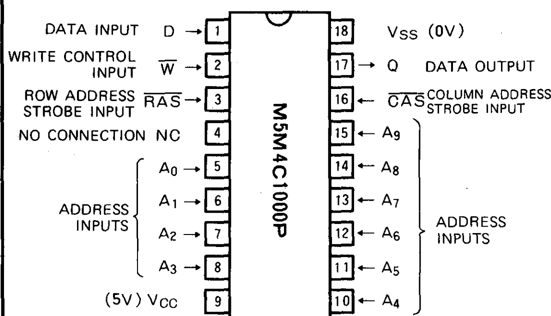
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M4C1000P/J/L-10	100	25	50	190	300
M5M4C1000P/J/L-12	120	30	55	220	250
M5M4C1000P/J/L-15	150	40	70	260	200

- High performance CMOS technology
- Standard 18 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . CMOS Input level
- Low operating power dissipation
  M5M4C1000P, J, L-10 . . . . 413mW (Max)
  M5M4C1000P, J, L-12 . . . . 358mW (Max)
  M5M4C1000P, J, L-15 . . . . 303mW (Max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-Modify-write, $\overline{RAS}$-only-Refresh, Fast-Page-Mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All inputs, output TTL compatible and low capacitance.
- 512 refresh cycles every 8ms
- $\overline{CAS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ low pulse width for
  Fast-Page-Mode . . . . 100μs Max

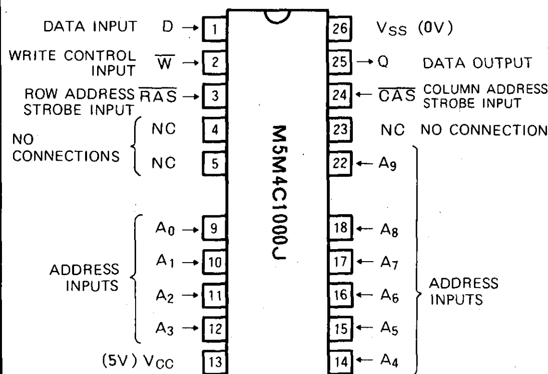
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

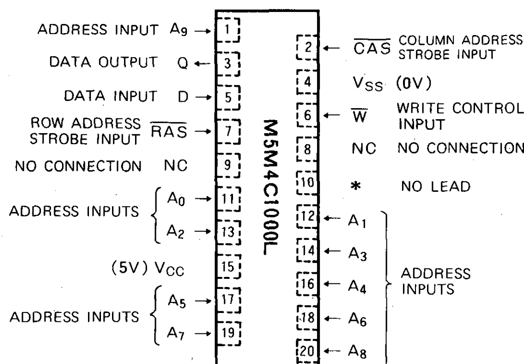
PIN CONFIGURATION (TOP VIEW)



Outline 18P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

FUNCTION

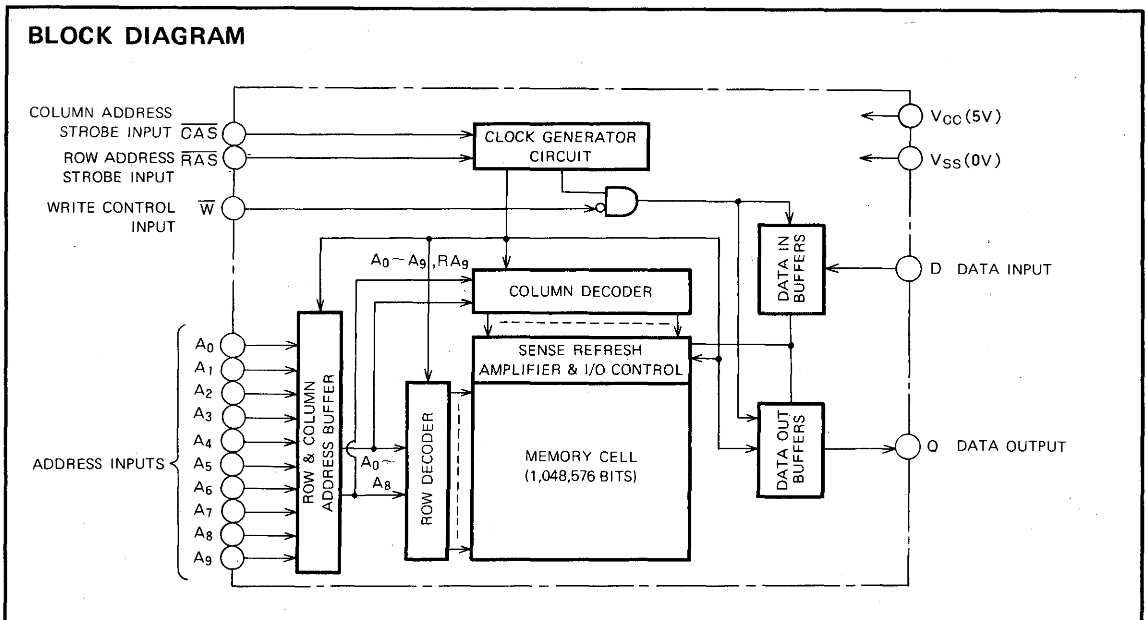
The M5M4C1000P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM



FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M4C1000-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$= min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}−0.5, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M4C1000-10	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}= min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	M5M4C1000-10	$\overline{RAS}$=V_{IL}, $\overline{CAS}$= cycling t_{PC}= min, output open			65	mA
		M5M4C1000-12				55	
		M5M4C1000-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4C1000-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}= min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_i=25mVrms			6	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance	V_O=V_{SS}, f=1MHz, V_i=25mVrms			7	pF

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column address access time	(Note 6, 9)		50		55		70	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		55		60		75	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, see notes 12, 13)

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	20	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		20		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low		95		110		135		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed t_T = 5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in note 7, 9.
15: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of fast page mode cycle.
17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
18: $t_{ASC(max)}$ is specified as a reference point only of address access time.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	50		55		70		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	95		115		140		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	20		25		30		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	95		115		140		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-Write cycle time (Note 21)	200		255		300		ns
t_{RMWC}	Read-Modify-Write cycle time (Note 22)	220		255		300		ns
t_{RAS}	$\overline{RAS}$ low pulse width	130	10000	155	10000	190	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	55	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	130		155		190		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	55		65		80		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low (Note 23)	25		30		40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 23)	100		120		150		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	20		25		30		ns
t_{AWD}	Delay time, address to write low (Note 23)	50		55		70		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.

22: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.

23: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RWD(min)}$, $t_{CWD} \geqq t_{CWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read-Write Read-Modify-Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast Page mode cycle time	60		65		80		ns
t_{RWPC}	Fast Page mode R/W, R/M/W cycle time	90		100		120		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read, write cycle	160	100000	185	100000	230	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle	25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 24)	15	25	15	25	20	30	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	25		30		40		ns

Note 24: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 25: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 26)

Read Cycle

t_{RC} t_{RP} t_{RAS} t_{CSH}

$\overline{RAS}$ V_{IH} V_{IL}

t_{CRP} t_{RCD} t_{RSH} t_{CAS}

$\overline{CAS}$ V_{IH} V_{IL}

t_{CPH} t_{RAD} t_{RAL} t_{ASR} t_{RAH} t_{ASC} t_{CAH} t_{ASR}

$A_0 \sim A_9$ V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS ROW ADDRESS

t_{AR} t_{RCS} t_{RRH}

$\overline{W}$ V_{IH} V_{IL}

D V_{IH} V_{IL}

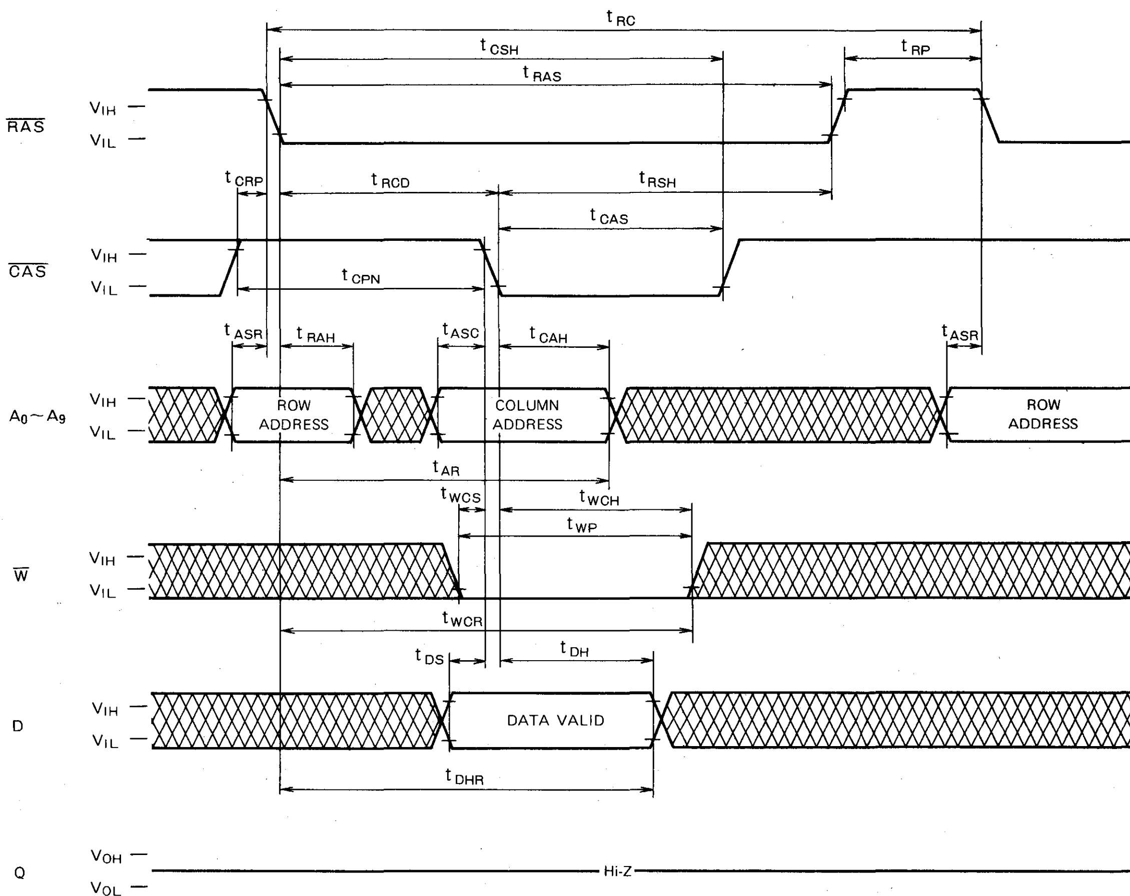
t_{CAC} t_{RCH} t_{CAA} t_{OFF} t_{CLZ}

Q V_{OH} V_{OL} Hi-Z DATA VALID

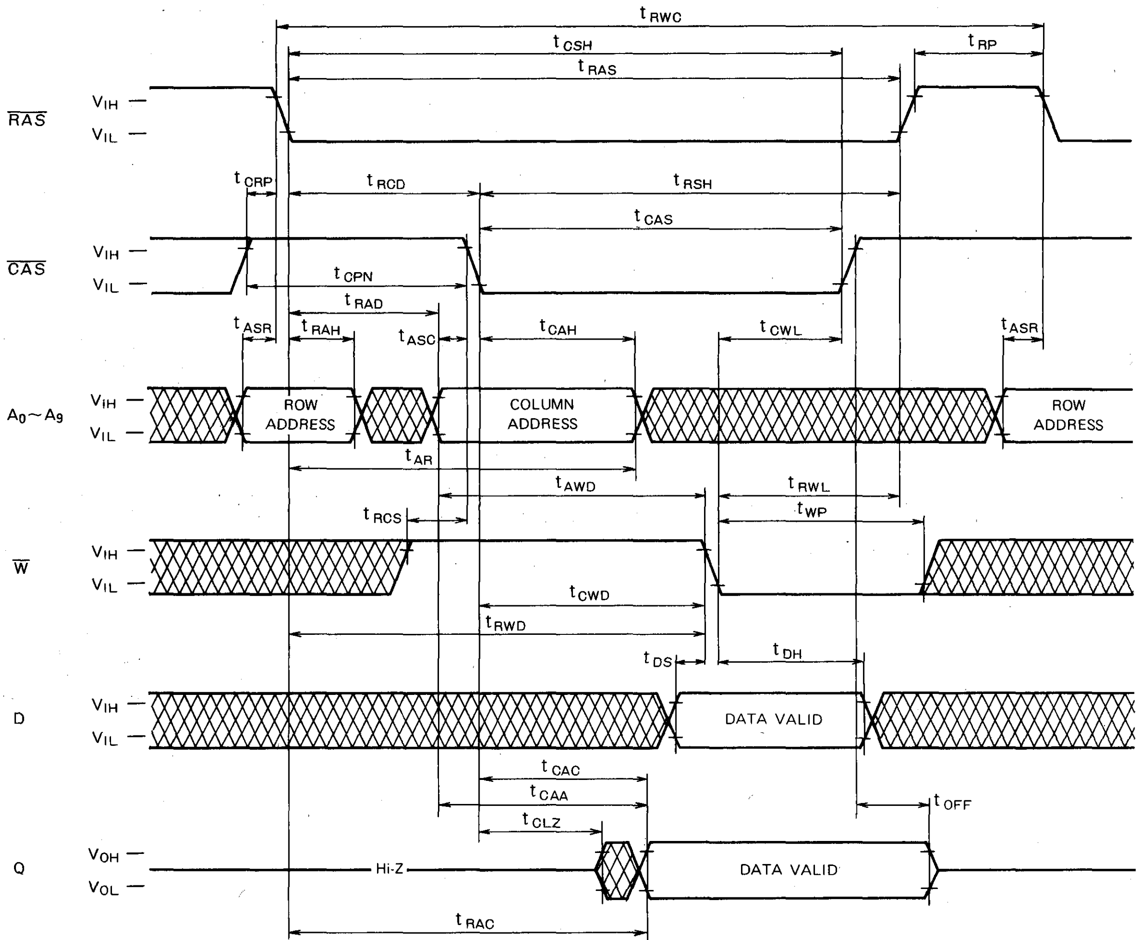
t_{RAC}

Note 26 Indicates the don't care input.

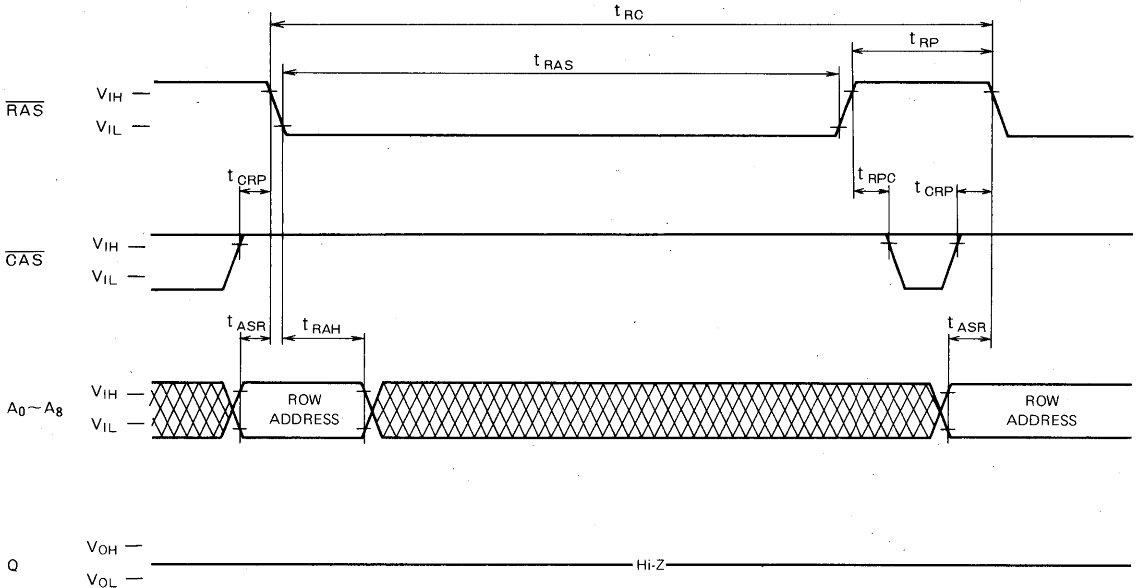
Write Cycle (Early write)



Read-Write, Read-Modify-Write Cycle

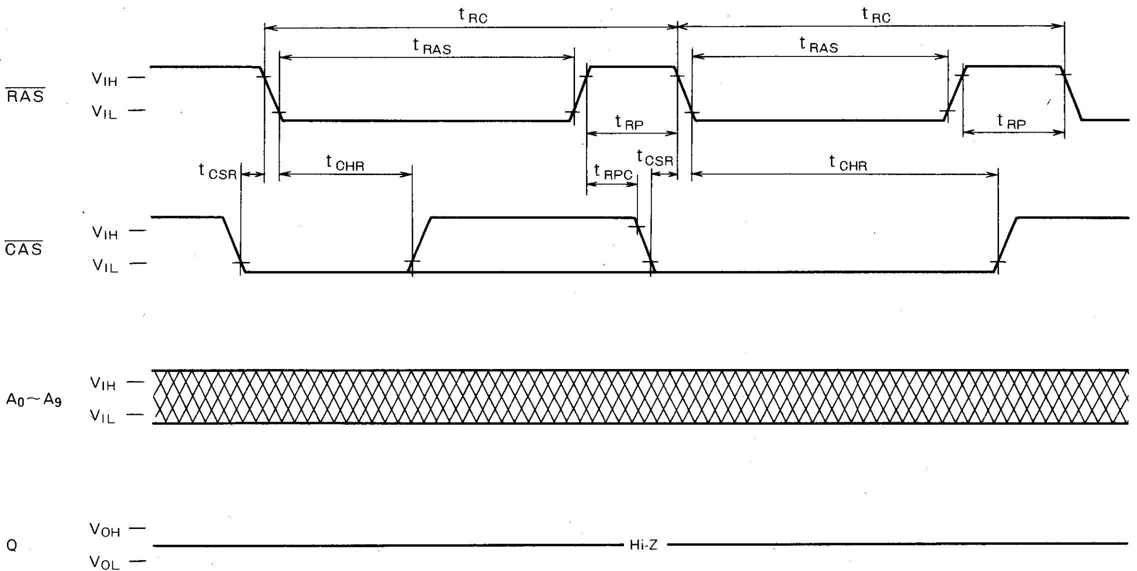


RAS-only Refresh Cycle (Note 27)



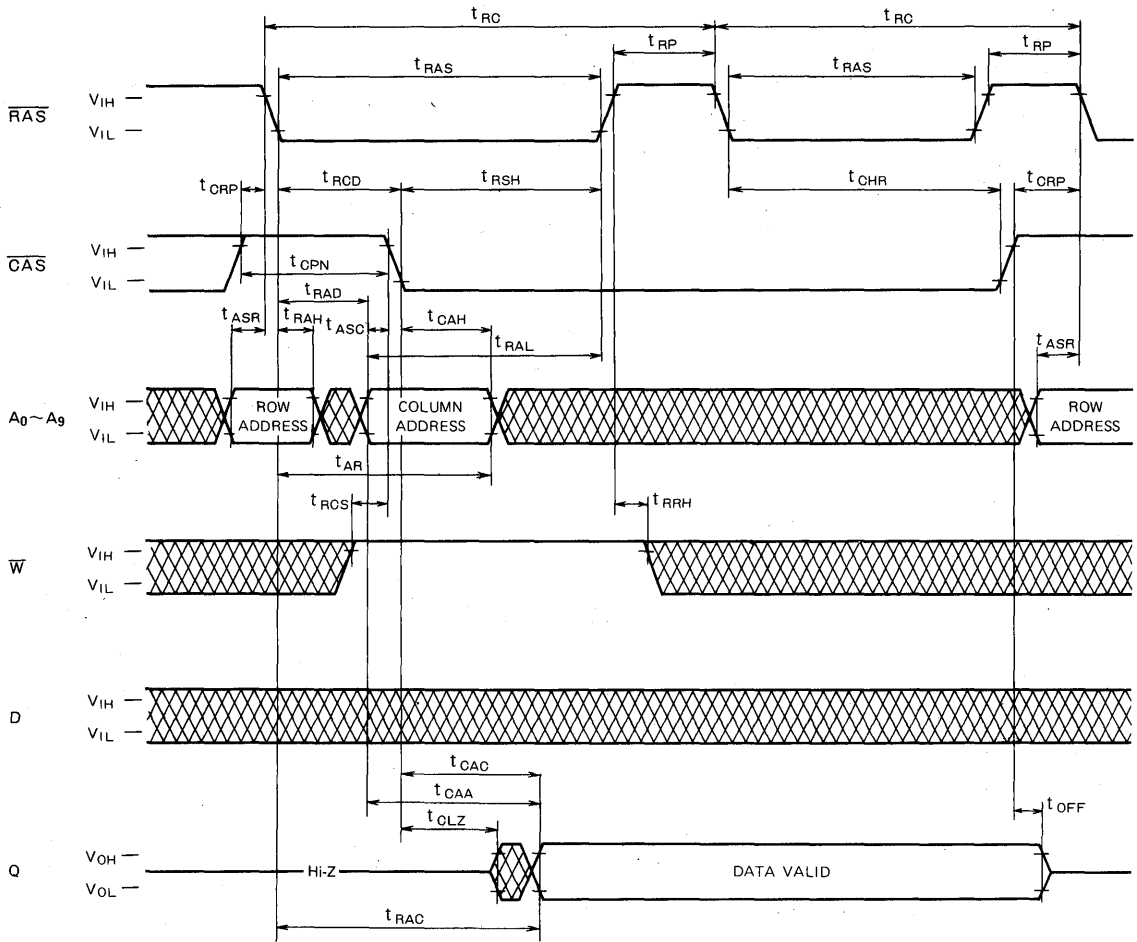
Note 27: $\overline{W}$, D = don't care, A_9 may be V_{IH} or V_{IL}

CAS before RAS Refresh Cycle (Note 28)

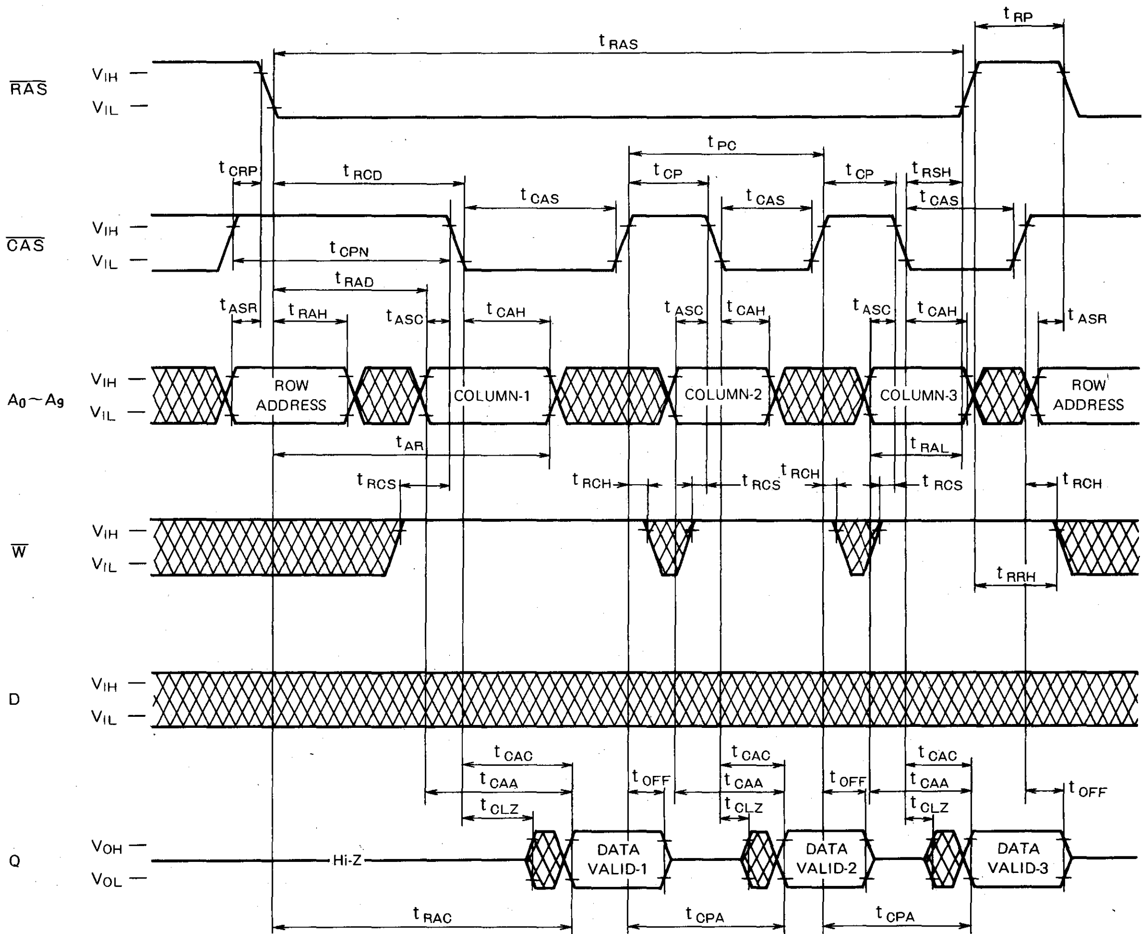


Note 28: $\overline{W}$, D = don't care

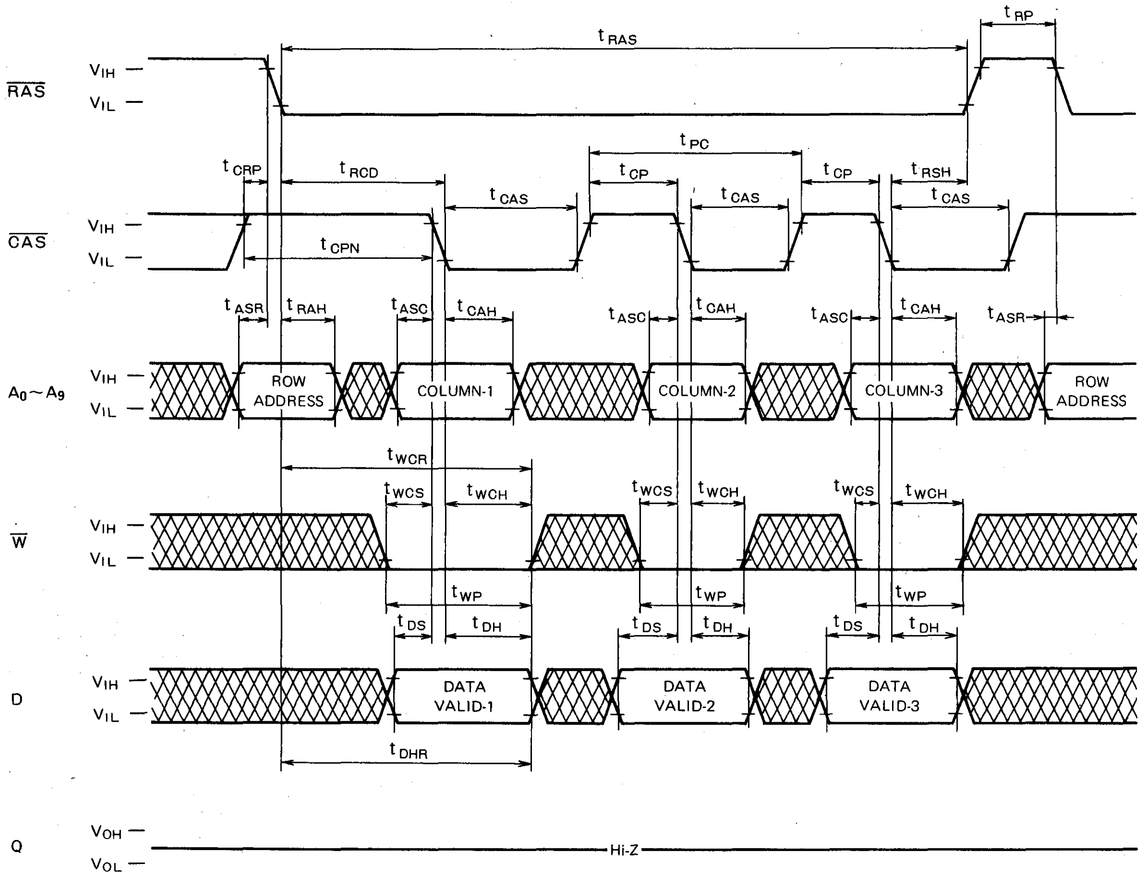
Hidden Refresh Cycle



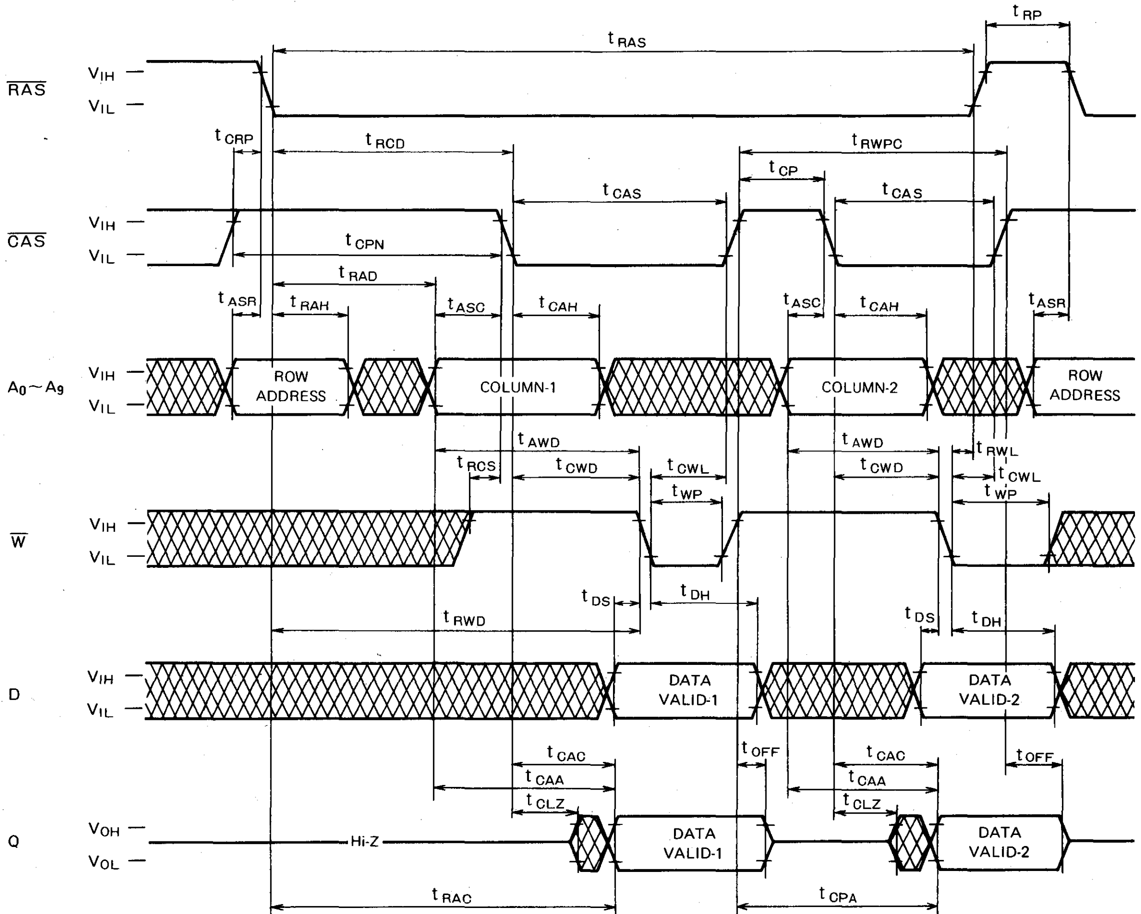
Fast-Page-Mode Read Cycle

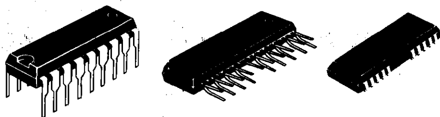


Fast-Page-Mode Early Write Cycle



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle





M5M4C1001P, J, L-10, -12, -15

NIBBLE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

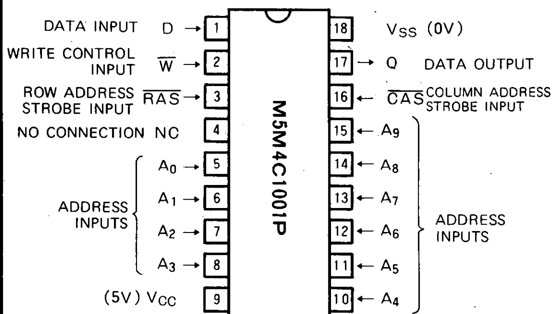
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Nibble access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M4C1001 P, J, L -10	100	50	25	190	300
M5M4C1001 P, J, L -12	120	60	30	220	250
M5M4C1001 P, J, L -15	150	75	40	260	200

- High performance CMOS technology
- Standard 18 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . CMOS Input level
- Low operating power dissipation
  M5M4C1001P, J, L-10 . . . . 413mW (Max)
  M5M4C1001P, J, L-12 . . . . 358mW (Max)
  M5M4C1001P, J, L-15 . . . . 303mW (Max)
- Unlatched output enables two-dimensional chip selection
- Early-write operation gives common I/O capability
- Read-Modify-Write, $\overline{RAS}$-only-Refresh, Nibble Mode capabilities.
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All inputs, output TTL compatible and low capacitance.
- 512 refresh cycles every 8ms
- $\overline{CAS}$ controlled output allows hidden refresh.

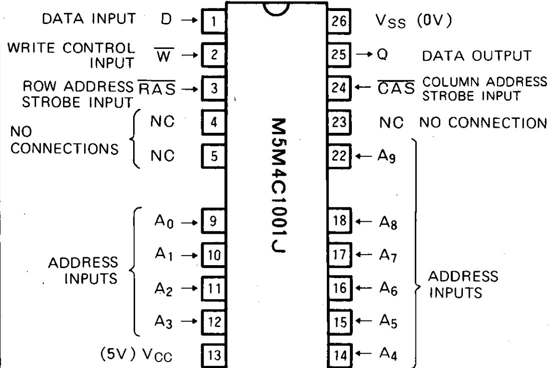
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

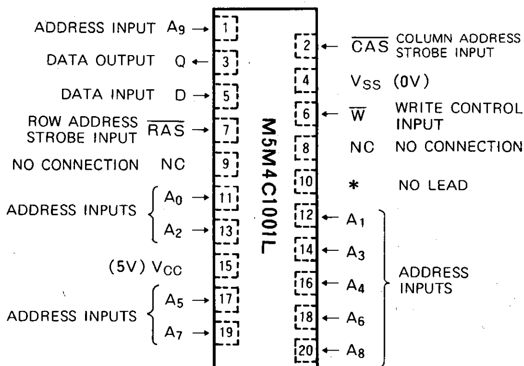
PIN CONFIGURATION (TOP VIEW)



Outline 18P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

NIBBLE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

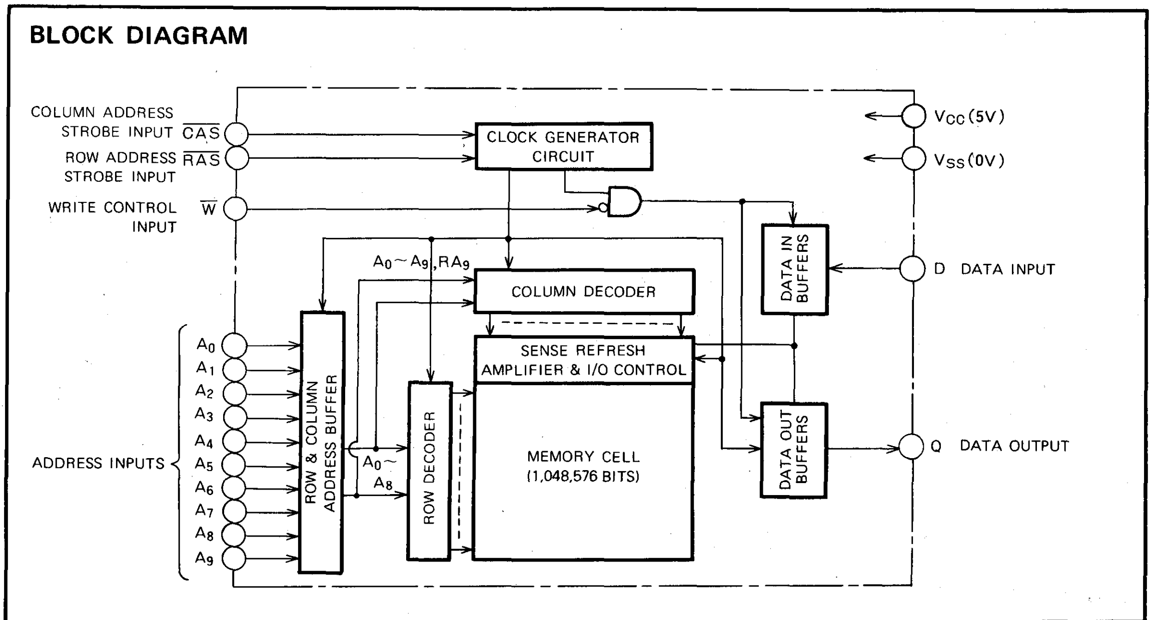
FUNCTION

The M5M4C1001P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Nibble mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Note.
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open
Nibble mode is identical, and nibble mode column address is DNC while toggling $\overline{CAS}$.



NIBBLE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	10000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M4C1001-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$= min, output open			75	mA
		M5M4C1001-12				65	
		M5M4C1001-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CAS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CAS}≧V_{CC}-0.5$, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M4C1001-10	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}= min, output open			75	mA
		M5M4C1001-12				65	
		M5M4C1001-15				55	
$I_{CC5(AV)}$	Average supply current from V_{CC} nibble mode (Note 3, 4)	M5M4C1001-10	$\overline{RAS}=V_{IL}$, $\overline{CAS}$= cycling t_{NC}= min, output open			35	mA
		M5M4C1001-12				30	
		M5M4C1001-15				25	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4C1001-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}= min, output open			75	mA
		M5M4C1001-12				65	
		M5M4C1001-15				55	

Note 2: Current flowing into an IC is positive, out in negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC5(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC5(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance	$V_O=V_{SS}$, f=1MHz, V_i=25mVrms			7	pF

NIBBLE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		50		60		75	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{NAC}	Access time from $\overline{CAS}$ (Nibble mode)	(Note 6, 9)		25		30		40	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 10)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD} \geqq t_{RCD(max)}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$. When $t_{RCD} \geqq t_{RCD(max)}$, t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD(max)}$.
9: Assume that $\overline{CAS}$ access time at the 2nd, 3rd and 4th $\overline{CAS}$ cycles on nibble mode.
10: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Nibble Mode Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, see notes 11, 12)

Symbol	Parameter		Limits						Unit
			M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 13)	20	50	25	60	30	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 14)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 15)	25		30		35		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		20		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low		70		80		100		ns
t_T	Transition time	(Note 16)	3	50	3	50	3	50	ns

Note 11: The timing requirements are assumed t_T = 5 ns.
12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
13: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is $t_{RCD} + t_{CAC}$.
$t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH} + 2t_T + t_{ASC}$.
14: t_{CRP} requirement is applicable for All $\overline{RAS}/\overline{CAS}$ cycles.
15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{NCP} of Nibble mode cycle.
16: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width		100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		50	10000	60	10000	75	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		50		60		75		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 17)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 17)	10		10		10		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 17: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter	Limits						Unit
		M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	50	10000	60	10000	75	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		60		75		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 20)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	70		85		105		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	20		25		30		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	70		85		105		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-Write cycle time (Note 18)	205		235		285		ns
t_{RMWC}	Read-Modify-Write cycle time (Note 19)	220		255		300		ns
t_{RAS}	$\overline{RAS}$ low pulse width	115	10000	135	10000	175	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	65	10000	75	10000	100	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	115		135		175		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	65		75		100		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low (Note 20)	35		40		60		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 20)	85		100		135		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	20		25		30		ns

Note 18: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
19: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
20: t_{WCS}, t_{RWD} and t_{CWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RWD(min)}$, and $t_{CWD} \geqq t_{CWD(min)}$ a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

MITSUBISHI ELECTRIC

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Limits						Unit
		M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 21: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Nibble Mode Cycle (Read, Write, Read-Write Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M4C1001-10		M5M4C1001-12		M5M4C1001-15		
		Min	Max	Min	Max	Min	Max	
t_{NC}	Nibble mode cycle time	50		55		70		ns
t_{NRWC}	Nibble mode Read-Write, Read-Modify-Write cycle time	80		90		110		ns
t_{NCAS}	Nibble mode $\overline{CAS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{NCRW}	Nibble mode $\overline{CAS}$ low pulse width for R-W, R-M-W cycle	55	10000	65	10000	80	10000	ns
t_{NCP}	Nibble mode $\overline{CAS}$ precharge time	15		15		20		ns
t_{NRSH}	Nibble mode $\overline{RAS}$ hold time	25		30		40		ns
t_{NCWD}	Nibble mode $\overline{CAS}$ to write delay	25		30		40		ns
t_{NRWL}	Nibble mode Write to $\overline{RAS}$ lead time	25		30		35		ns
t_{NCWL}	Nibble mode Write to $\overline{CAS}$ lead time	25		30		35		ns
t_{NWCS}	Nibble mode Write setup time before $\overline{CAS}$	0		0		0		ns
t_{NWCH}	Nibble mode Write hold time after $\overline{CAS}$	20		25		30		ns

Nibble-Mode Addressing Sequence Example

Sequence	Nibble bit	Column address										Row address										
		A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	
$\overline{RAS}$/$\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	External address
toggle $\overline{CAS}$	2	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	1	Internaly generated address
toggle $\overline{CAS}$	3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	
toggle $\overline{CAS}$	4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
toggle $\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	

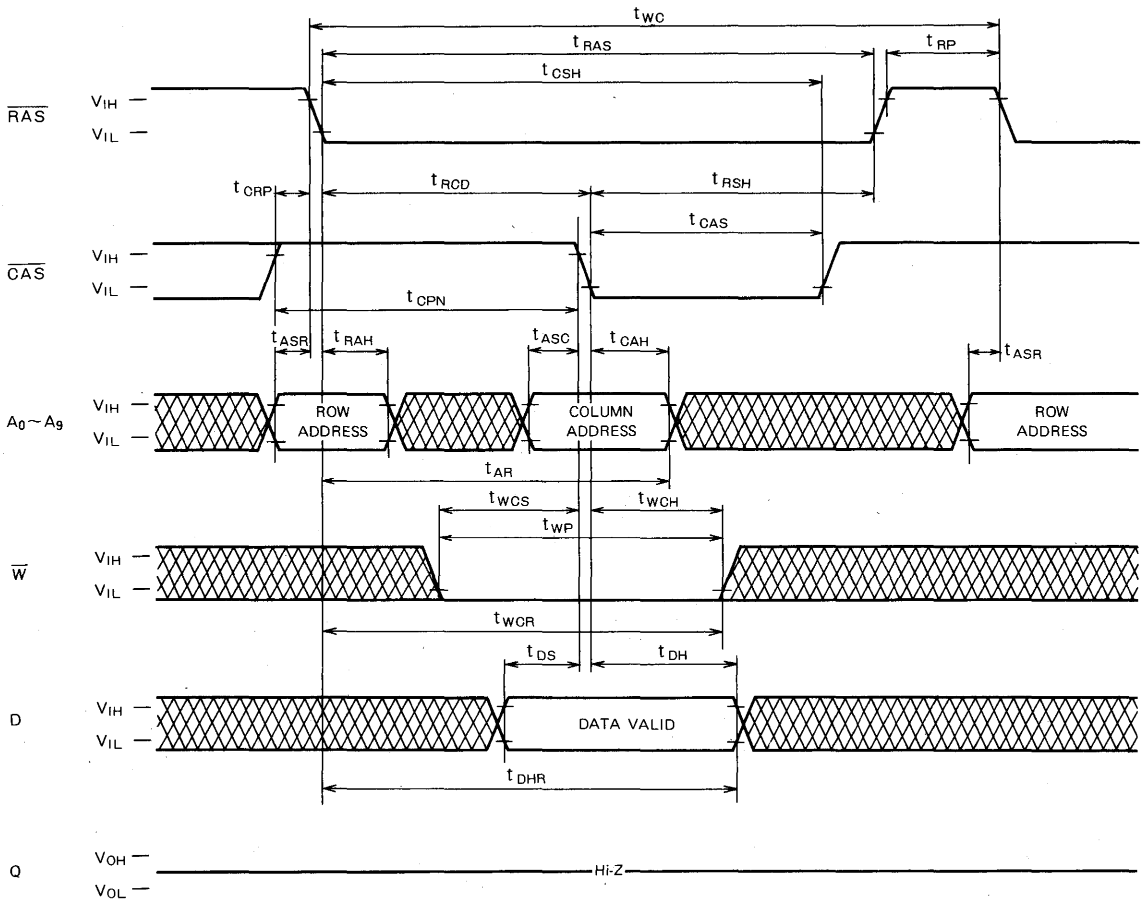
Timing Diagram (Note 22)

Read Cycle

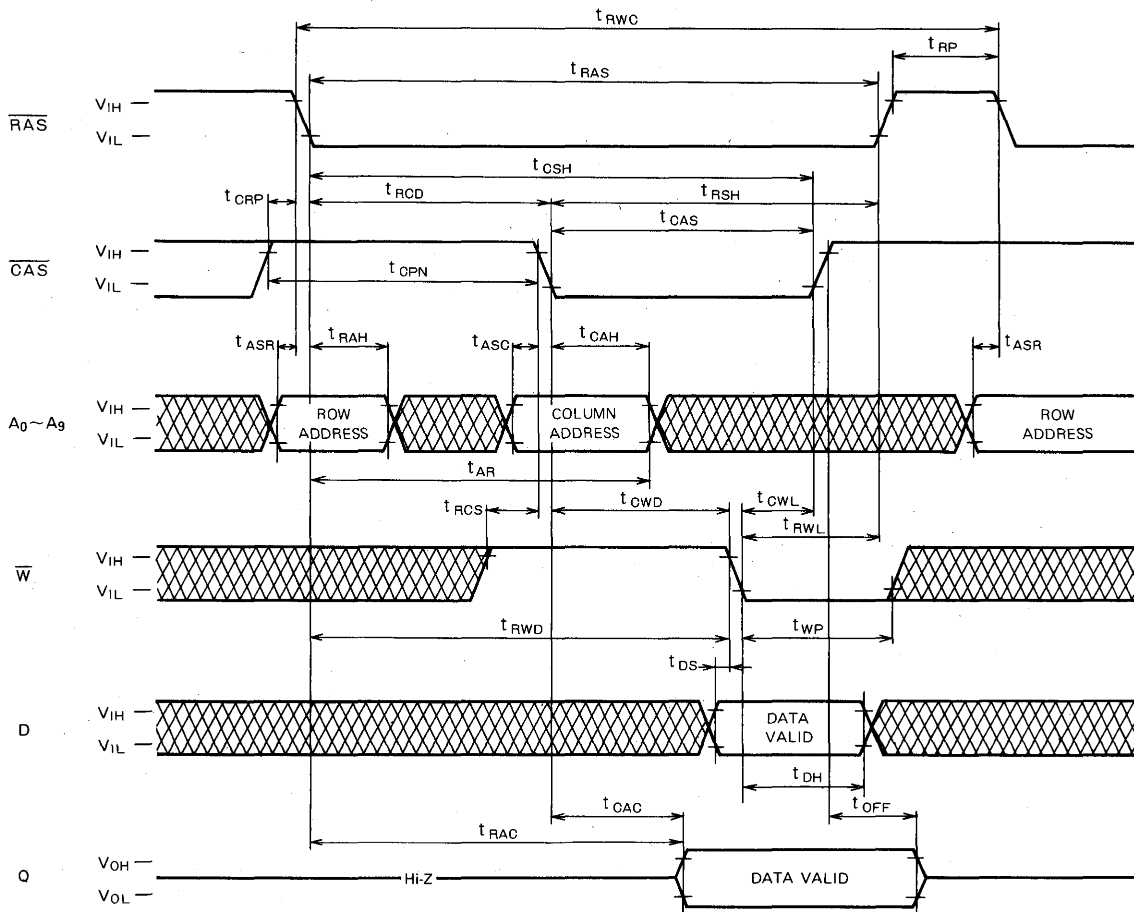
t_{RC}
t_{RAS}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{RP}
t_{CSH}
t_{CRP} t_{RCD} t_{RSH}
t_{CAS}
$\overline{CAS}$ V_{IH} — V_{IL} —
t_{CPN}
t_{ASR} t_{RAH} t_{ASC} t_{CAH} t_{ASR}
$A_0 \sim A_9$ V_{IH} — V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
t_{AR}
t_{RCS} t_{RCH}
$\overline{W}$ V_{IH} — V_{IL} —
t_{RRH}
D V_{IH} — V_{IL} —
t_{CAC} t_{OFF}
t_{RAC}
Q V_{IH} — V_{IL} —
Hi-Z
DATA VALID

Note 22 Indicates the don't care input.

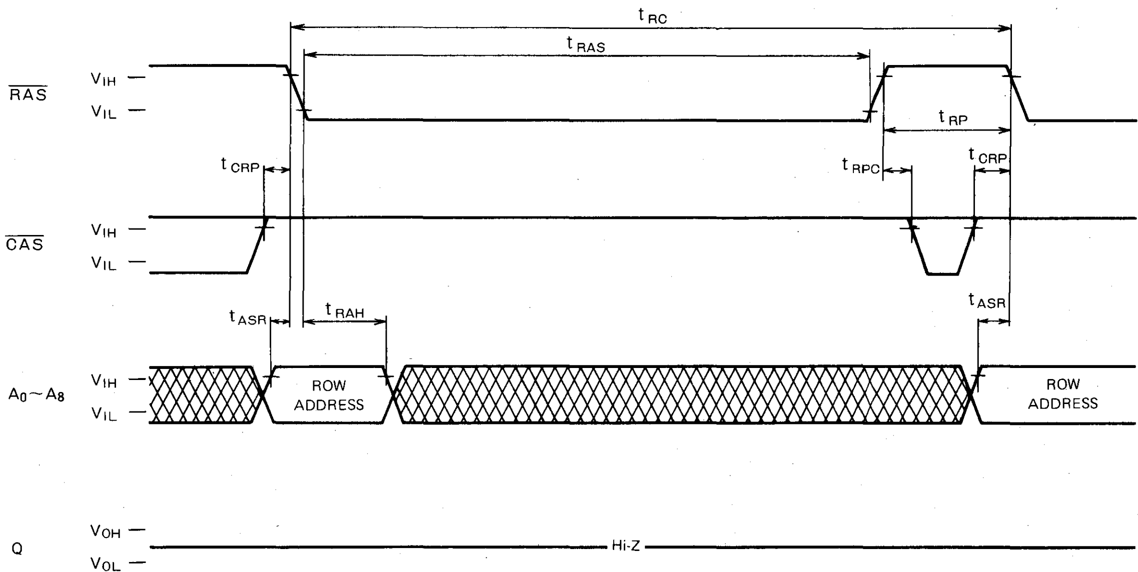
Write Cycle (Early Write)



Read-Write and Read-Modify-Write Cycle

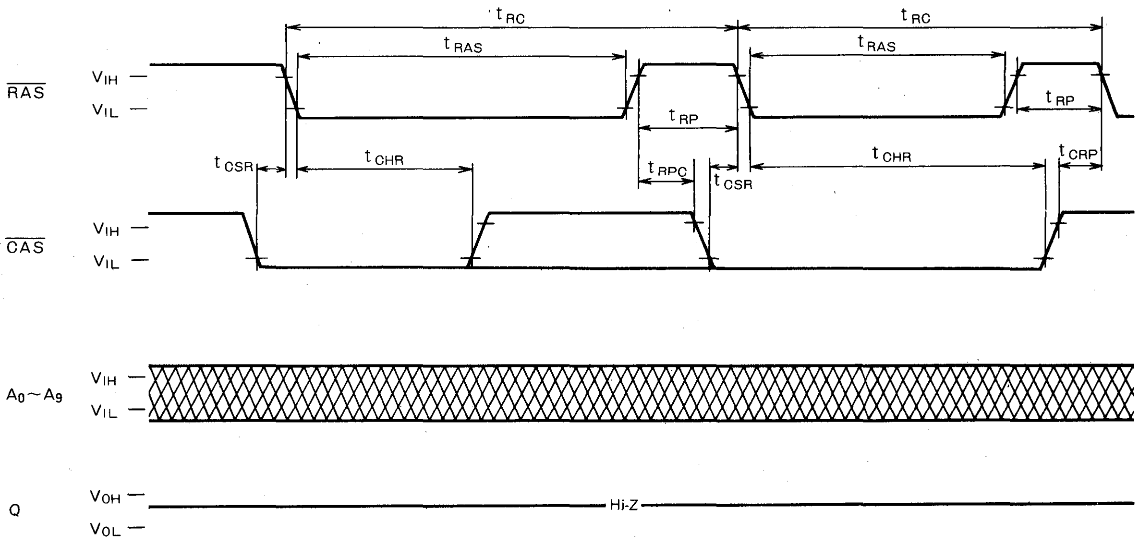


$\overline{RAS}$-only-Refresh Cycle (Note 23)



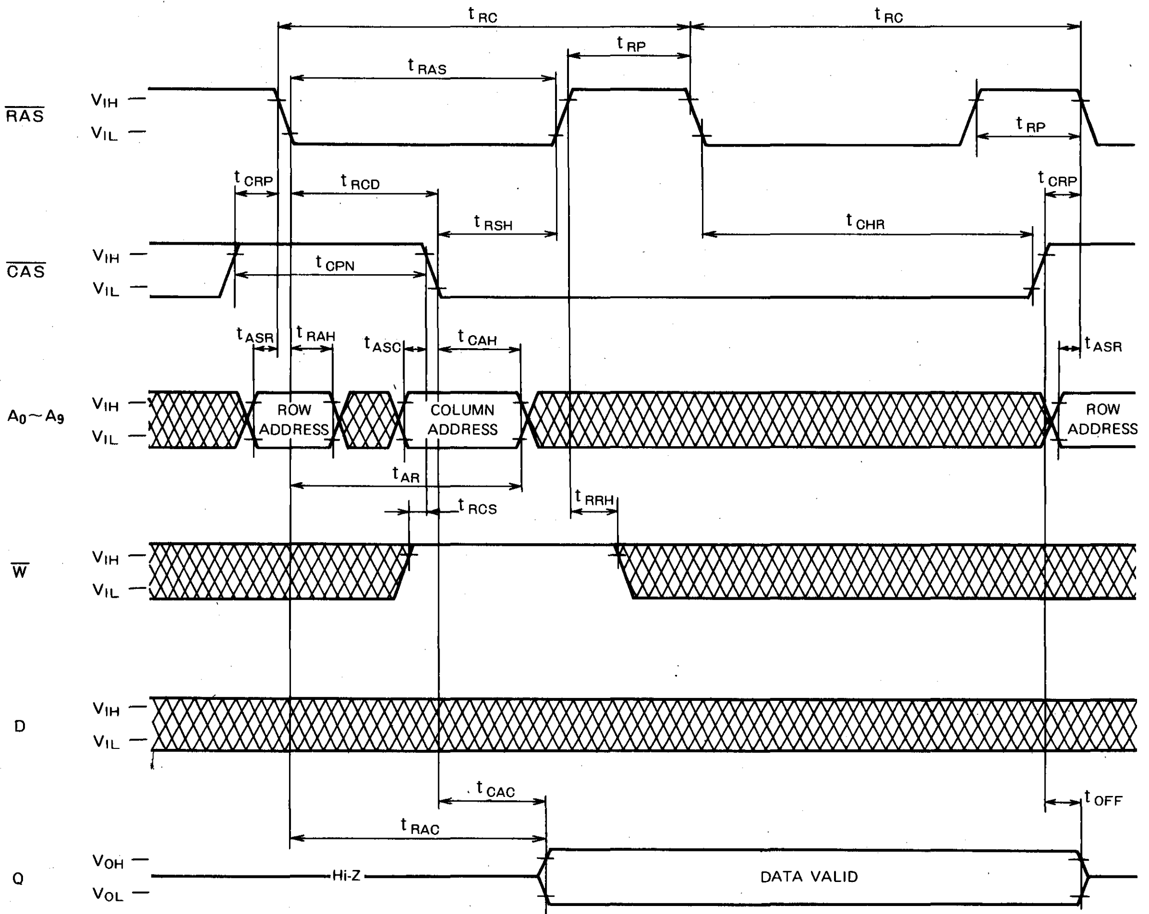
Note 23: $\overline{W}$, D = don't care, A_9 may be V_{IH} or V_{IL}

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)



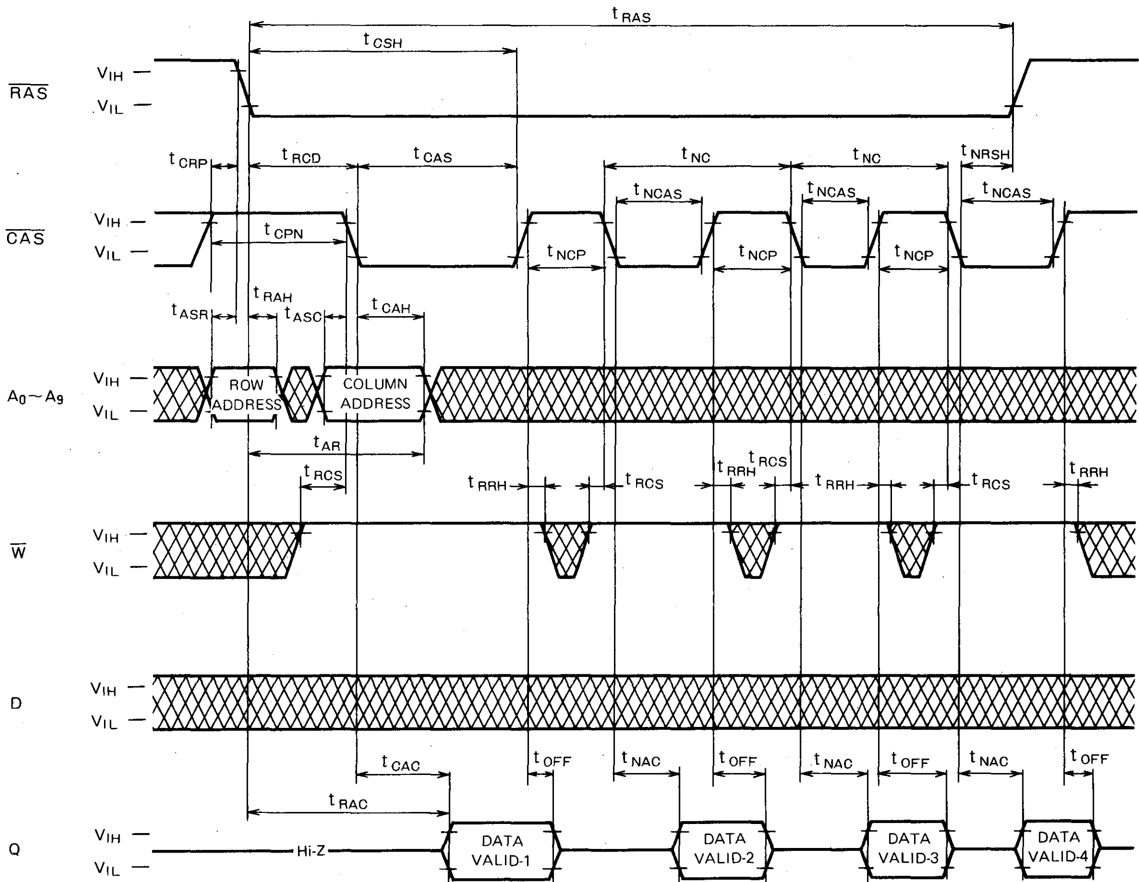
Note 24: $\overline{W}$, D = don't care

Hidden Refresh Cycle

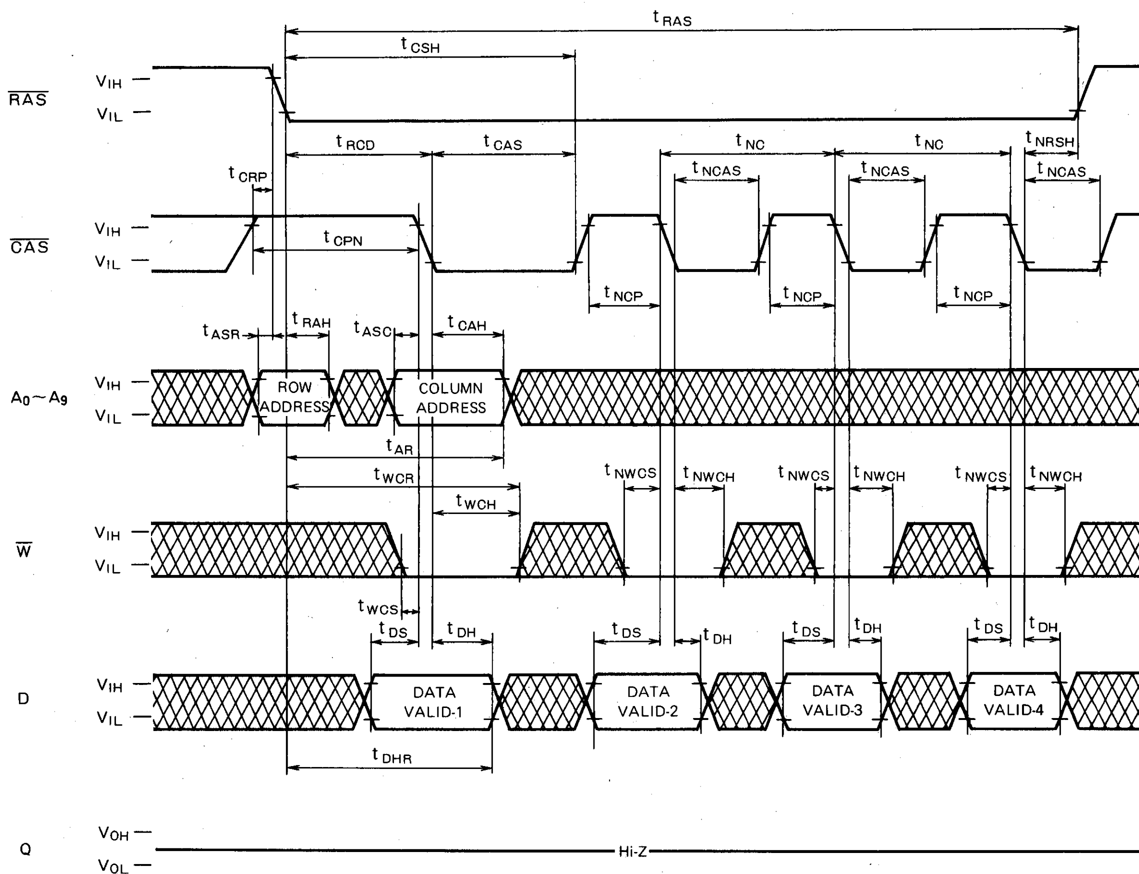


MITSUBISHI ELECTRIC

Nibble Mode Read Cycle



Nibble Mode Write Cycle (Early Write)



Nibble Mode, Read-Write and Read-Modify-Write Cycle

$\overline{RAS}$ V_{IH} V_{IL} t_{RAS} t_{NRWL}

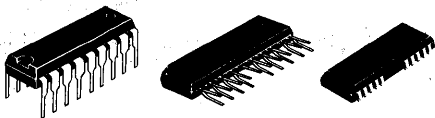
$\overline{CAS}$ V_{IH} V_{IL} t_{CRP} t_{CPN} t_{CAS} t_{NRWC} t_{NCRW} t_{NCP} t_{NCWL}

$A_0 \sim A_9$ V_{IH} V_{IL} t_{ASR} t_{RAH} t_{ASC} t_{CAH} ROW ADDRESS COLUMN ADDRESS t_{AR}

$\overline{W}$ V_{IH} V_{IL} t_{CWD} t_{RCS} t_{NCWD} t_{RWD} t_{WP} t_{WP}

D V_{IH} V_{IL} t_{DS} t_{DH} t_{DS} t_{DH} DATA VALID-1 DATA VALID-2

Q V_{OH} V_{OL} t_{CAC} t_{OFF} t_{OFF} t_{RAC} t_{NAC} Hi-Z DATA VALID-1 DATA VALID-2



M5M4C1002P, J, L-10, -12, -15

STATIC COLUMN MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

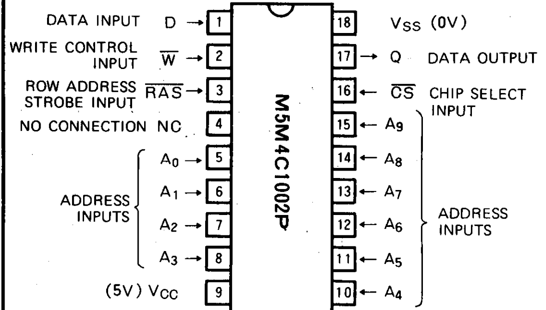
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M4C1002P/J/L-10	100	25	50	190	300
M5M4C1002P/J/L-12	120	30	55	220	250
M5M4C1002P/J/L-15	150	40	70	260	200

- High performance CMOS technology
- Standard 18 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  - 5.5mW (Max) .... CMOS Input level
- Low operating power dissipation
  - M5M4C1002P, J, L-10 .... 413mW (Max)
  - M5M4C1002P, J, L-12 .... 358mW (Max)
  - M5M4C1002P, J, L-15 .... 303mW (Max)
- Unlatched output enables two-dimensional chip selection
- Early-write operation gives common I/O capability
- Read-Modify-Write, $\overline{RAS}$-only-Refresh, Static Column Mode capabilities.
- $\overline{CS}$ before $\overline{RAS}$ refresh mode capability
- All inputs, output TTL compatible and low capacitance.
- 512 refresh cycles every 8ms
- $\overline{CS}$ controlled output allows hidden refresh.
- Wide $\overline{RAS}$ low pulse width for
  - Static Column Mode .... 100μs Max

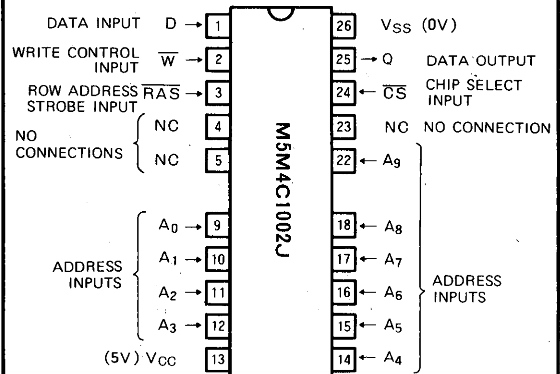
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

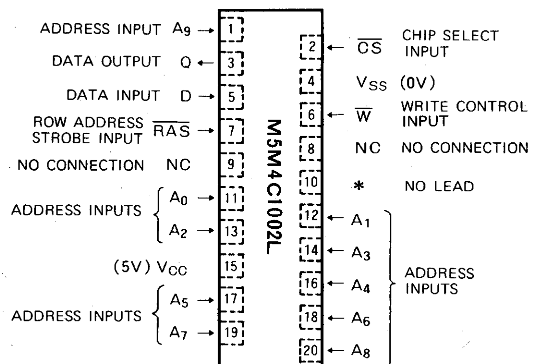
PIN CONFIGURATION (TOP VIEW)



Outline 18P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

STATIC COLUMN MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

FUNCTION

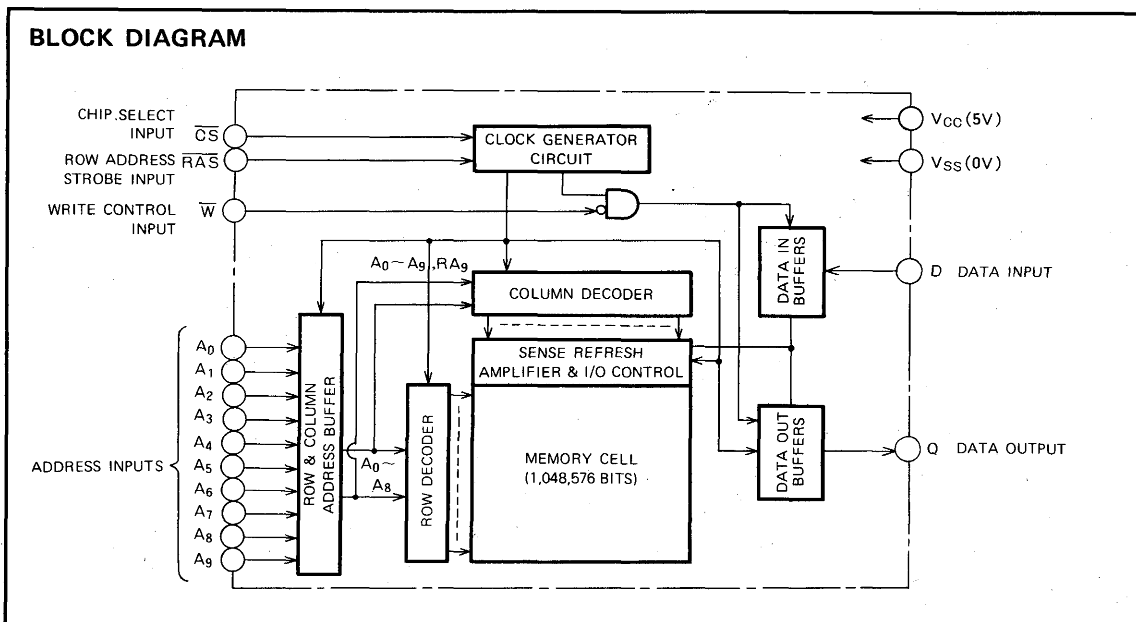
The M5M4C1002P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Static Column mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Note.
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open
Static column mode is identical except early write.

BLOCK DIAGRAM



STATIC COLUMN MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M4C1002-10	$\overline{RAS}$, $\overline{CS}$ cycling $t_{RC}=t_{WC}$= min, output open			75	mA
		M5M4C1002-12				65	
		M5M4C1002-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CS}\geq V_{CC}-0.5$, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M4C1002-10	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}= min, output open			75	mA
		M5M4C1002-12				65	
		M5M4C1002-15				55	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4C1002-10	$\overline{CS}$ before $\overline{RAS}$ refresh cycling t_{RC}= min, output open			75	mA
		M5M4C1002-12				65	
		M5M4C1002-15				55	
$I_{CC7(AV)}$	Average supply current from V_{CC}, Static Column mode (Note 3, 4)	M5M4C1002-10	$\overline{RAS}=V_{IL}$, Column address cycling t_{SC}= min, output open			65	mA
		M5M4C1002-12				55	
		M5M4C1002-15				45	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC6(AV)}$ and $I_{CC7(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC7(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CS})}$	Input capacitance, $\overline{CS}$ input				7	pF
C_O	Output capacitance	$V_O=V_{SS}$, f=1MHz, V_i=25mVrms			7	pF

STATIC COLUMN MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column Address access time	(Note 6, 9)		50		55		70	ns
t_{WRA}	Access time from $\overline{W}$ high	(Note 6)		60		65		80	ns
t_{CLZ}	Output low impedance time from $\overline{CS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CS}$ high	(Note 10)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD} \geqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then t_{RAC} will increase by the amount that t_{RCD} or t_{RAD} exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Static Column Cycles)

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 11, 12)

Symbol	Parameter		Limits						Unit
			M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CS}$ low	(Note 13)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CS}$ high to $\overline{RAS}$ low	(Note 14)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 15)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CS}$ low		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CS}$ low or $\overline{W}$ low		20		20		25		ns
t_T	Transition time	(Note 17)	3	50	3	50	3	50	ns

Note 11: The timing requirements are assumed t_T = 5ns.
12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
13: $t_{RCD(max)}$ is specified as a reference point only; If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is $t_{RCD} + t_{CAC}$. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH} + 2t_T + t_{ASC}$.
14: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles.
15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of static column mode cycle.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CS}$ high (Note 18)	10		10		10		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	50		55		70		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	15		15		15		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter	Limits						Unit
		M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{WCS}	Write setup time before $\overline{CS}$ low (Note 21)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CS}$ low	20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	95		115		140		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CS}$ low	20		25		30		ns
t_{AWR}	Address hold time after $\overline{RAS}$ low	95		110		135		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	95		115		140		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-write cycle time (Note 19)	220		255		300		ns
t_{RMWC}	Read-Modify-Write cycle time (Note 20)	220		255		300		ns
t_{RAS}	$\overline{RAS}$ low pulse width	130	10000	155	10000	190	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	55	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	130		155		190		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	55		65		80		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CS}$ low to write low (Note 21)	25		30		40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 21)	100		120		150		ns
t_{CWL}	$\overline{CS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	20		25		30		ns
t_{AWD}	Delay time, address to write low (Note 21)	50		55		70		ns
t_{WOH}	Output hold time from write high	20		25		30		ns

Note 19: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.

20: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.

21: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only.
When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RWD(min)}$, $t_{CWD} \geqq t_{CWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$ a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition is satisfied, the condition of Q (at access time and until $\overline{CS}$ goes back to V_{IH}) is indeterminate.

Static Column Mode Cycle (Read, Early write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
		Min	Max	Min	Max	Min	Max	
t_{RSC}	SC read cycle time	55		60		75		ns
t_{WSC}	SC write cycle time	55		60		75		ns
t_{RWSC}	SC R/W, R/M/W, cycle time	90		100		120		ns
t_{RAS}	$\overline{RAS}$ low pulse width	155	100000	180	100000	225	100000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CS}$ high pulse width	15		15		20		ns
t_{RSW}	Delay time, $\overline{RAS}$ to 2nd Write low	115		135		165		ns
t_{WI}	Write invalid time	15		15		20		ns
t_{WHRW}	Write high pulse width for R/W, R/M/W, cycle	60		65		80		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{AOH}	Data hold time from address change	10		10		10		ns
t_{WAD}	Delay time write to address change (Note 22)	−10	10	−10	10	−10	10	ns

Note 22: $t_{WAD(max)}$ is specified as a reference point only. If $t_{WAD} \geqq t_{WAD(max)}$, access time is assumed by t_{CAA}.

$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)

Symbol	Parameter	Limits						Unit
		M5M4C1002-10		M5M4C1002-12		M5M4C1002-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns

Note 23: Eight or more $\overline{CS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CS}$ before $\overline{RAS}$ refresh mode.

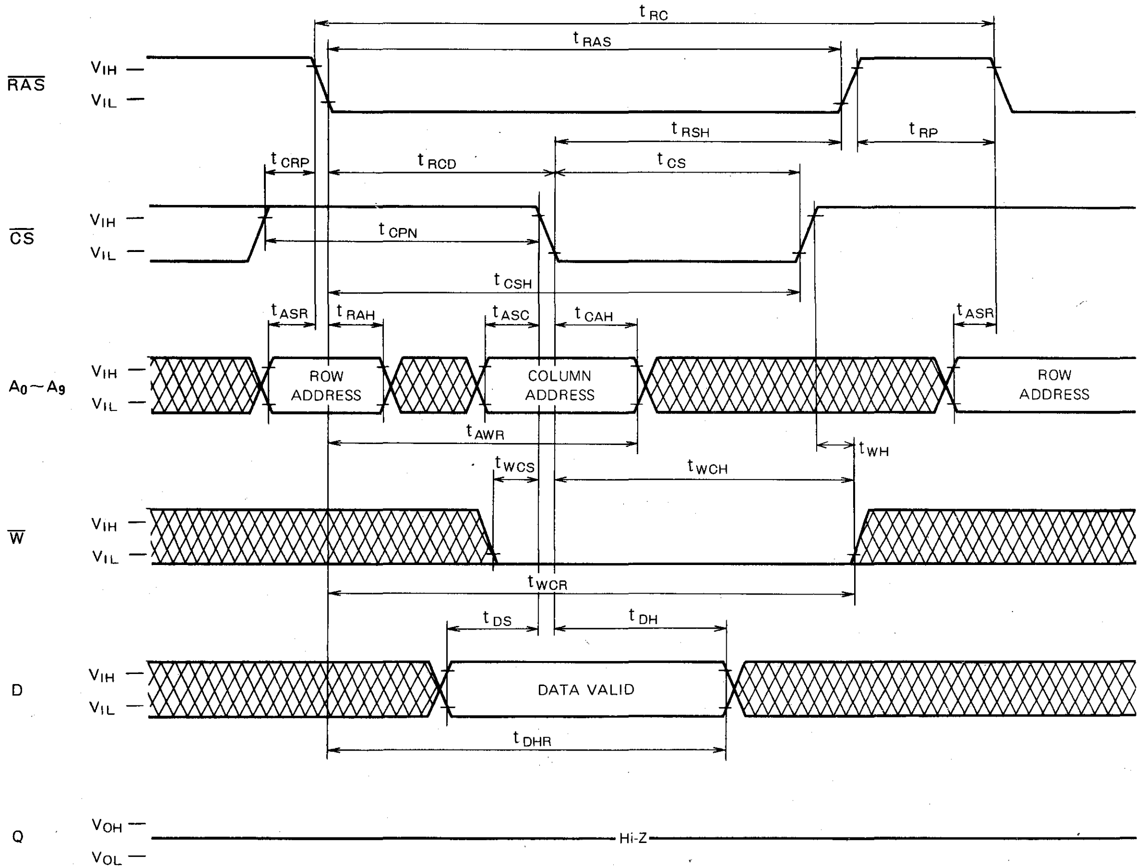
Timing Diagrams (Note 24)

Read Cycle

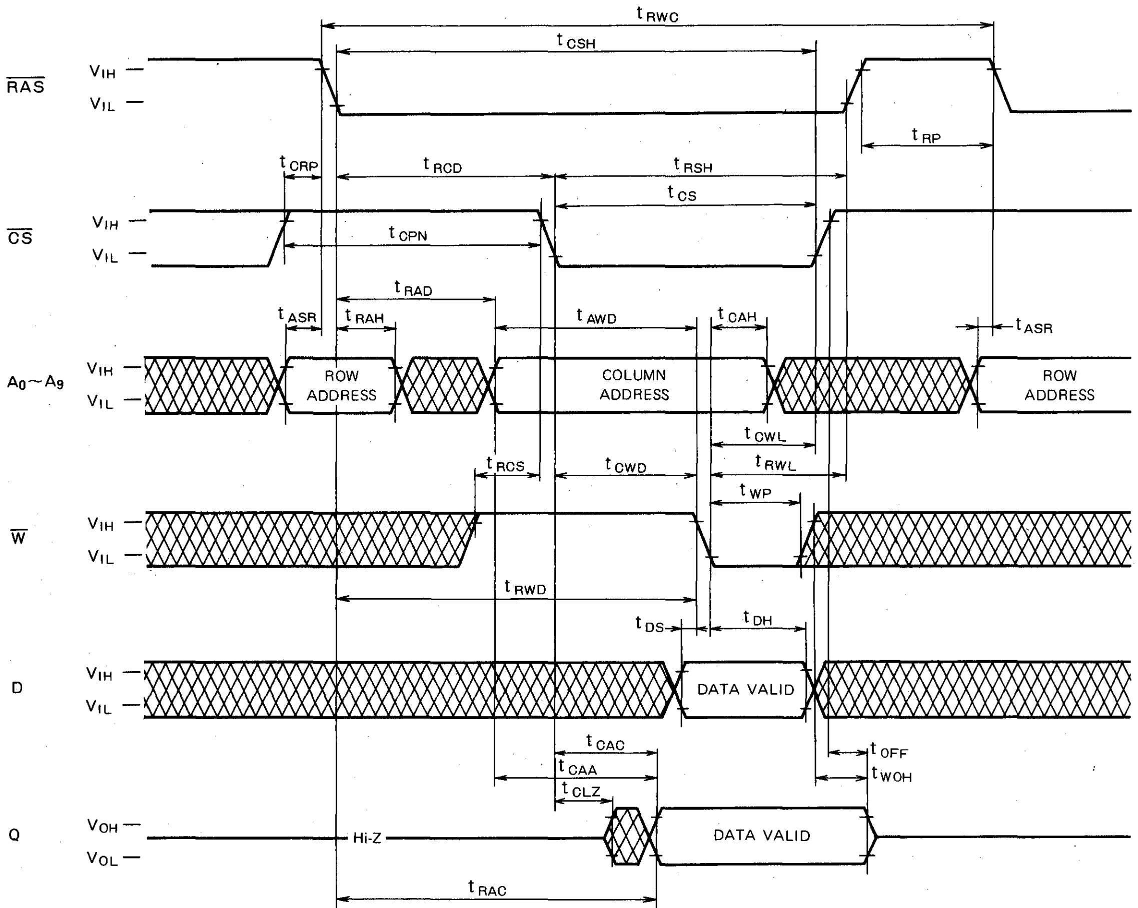
t_{RC}
t_{RAS}
t_{RCD}
$\overline{RAS}$ V_{IH} – V_{IL} –
t_{RSH} t_{RP}
t_{CRP} t_{CSH}
t_{CS}
$\overline{CS}$ V_{IH} – V_{IL} –
t_{CPN}
t_{ASR} t_{RAH} t_{RAL}
t_{RAD} t_{AH} t_{ASR}
$A_0 \sim A_9$ V_{IH} – V_{IL} – ROW ADDRESS COLUMN ADDRESS ROW ADDRESS
t_{RRH}
t_{RCS} t_{RCH}
$\overline{W}$ V_{IH} – V_{IL} –
D V_{IH} – V_{IL} –
t_{CAC} t_{OFF}
t_{CLZ}
Q V_{OH} – V_{OL} – Hi-Z DATA VALID
t_{CAA}
t_{RAC}

Note 24 Indicates the don't care input.

Write Cycle (Early write)

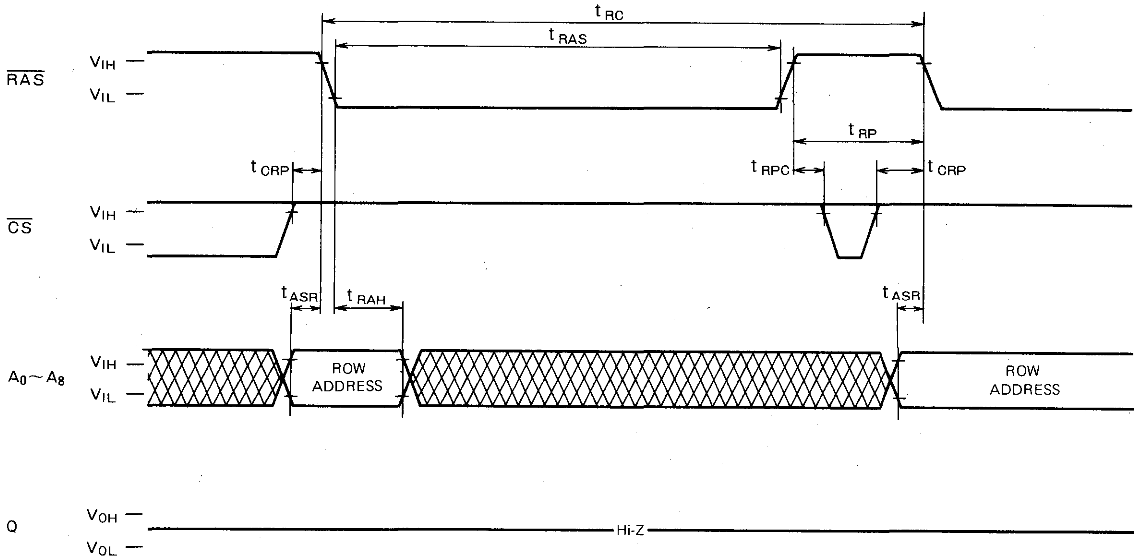


Read-Write, Read-Modify-Write Cycle



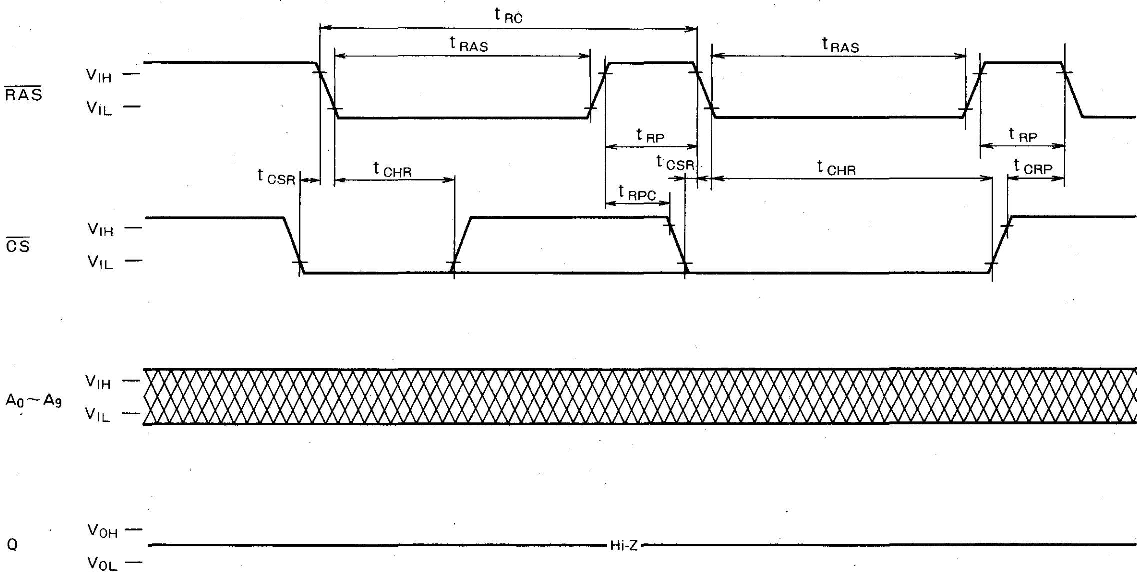
MITSUBISHI ELECTRIC

$\overline{RAS}$ only Refresh Cycle (Note 25)



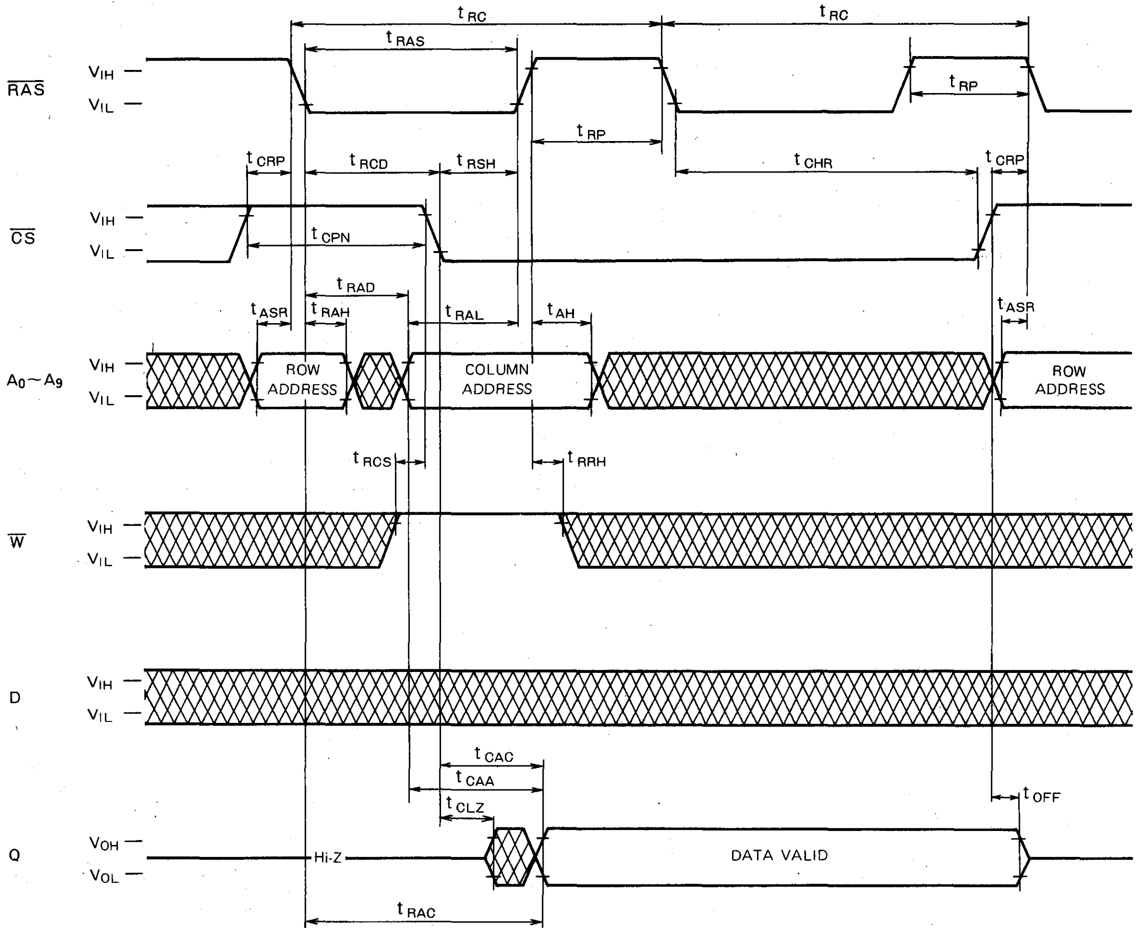
Note 25: $\overline{W}$, D = don't care, A_9 may be V_{IH} or V_{IL}

$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

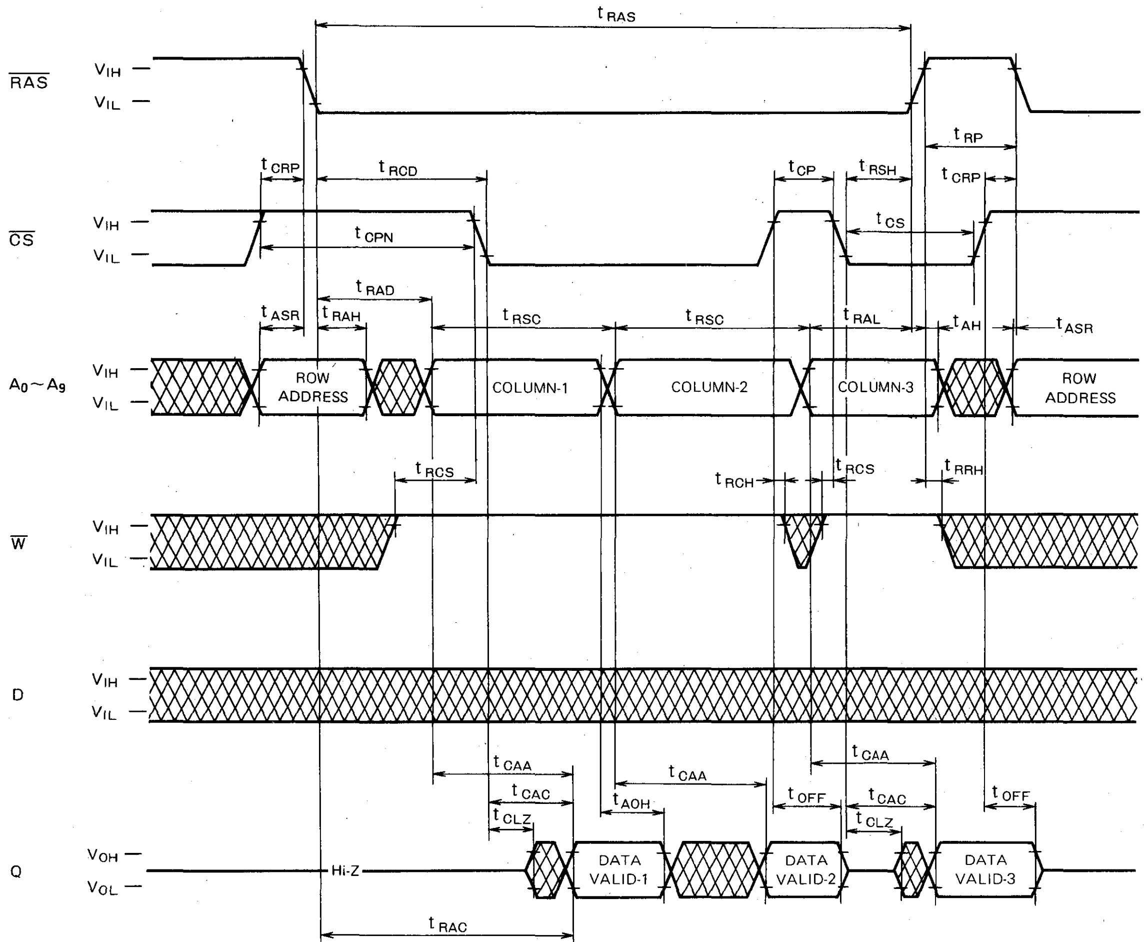


Note 26: $\overline{W}$, D = don't care

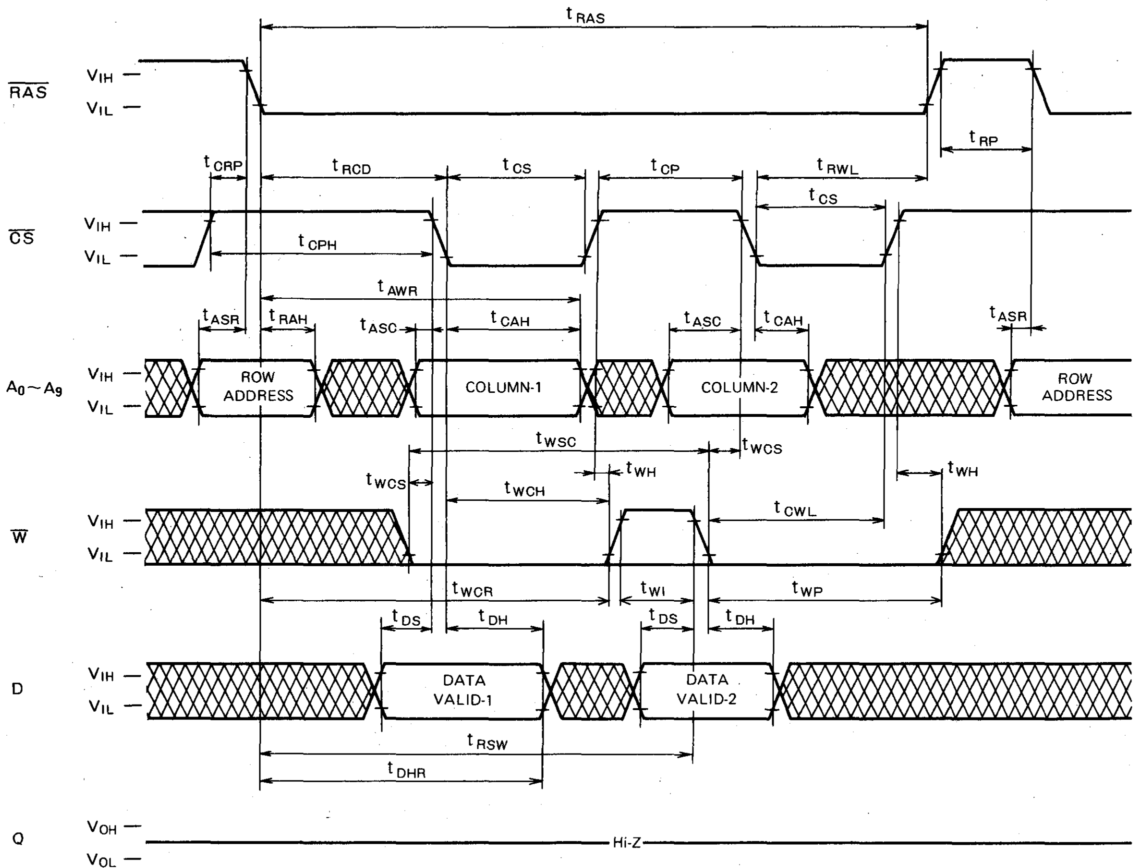
Hidden Refresh Cycle



Static Column Mode Read Cycle

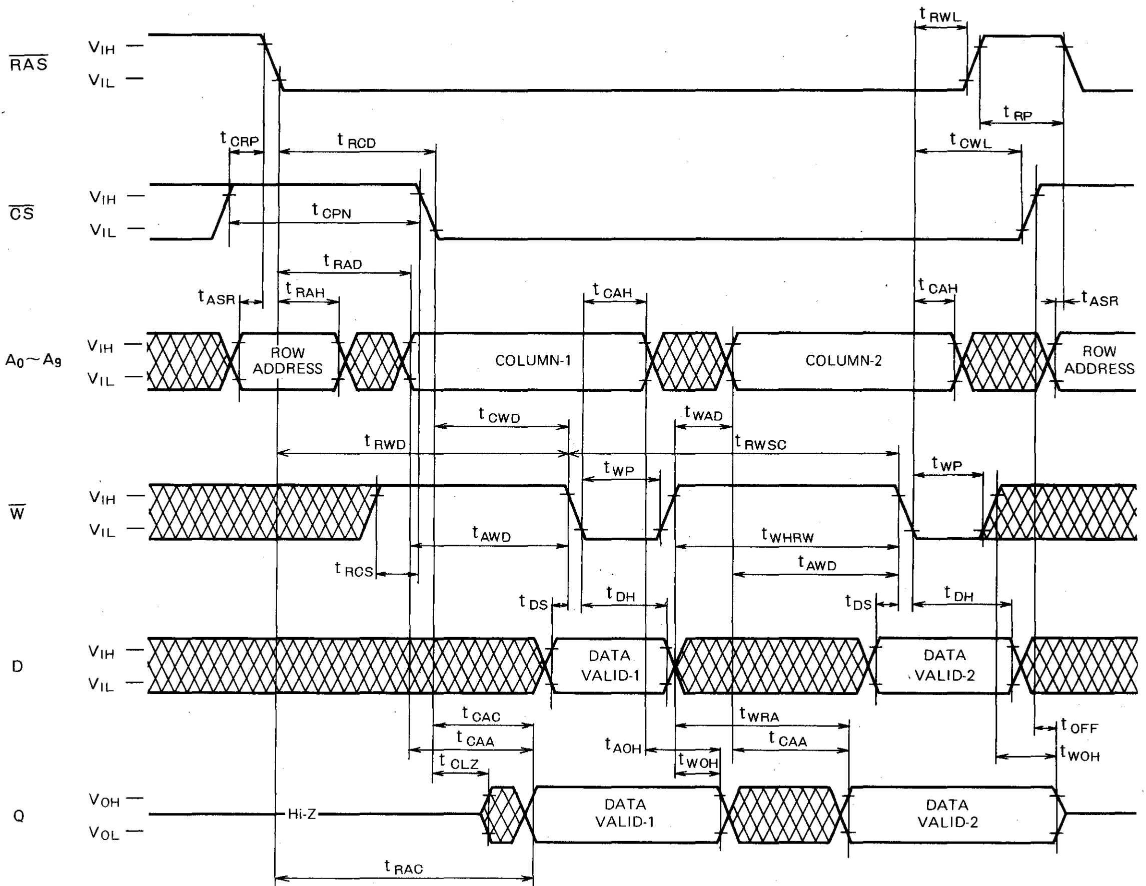


Static Column Mode Early Write Cycle



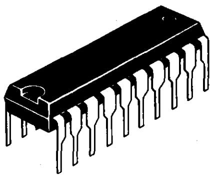
MITSUBISHI ELECTRIC

Static Column Mode Read-Write, Read-Modify-Write Cycle



CMOS STATIC RAM

3



M5M21C67P-35, -45, -55

16384-BIT (16384-WORD BY 1-BIT) CMOS STATIC RAM

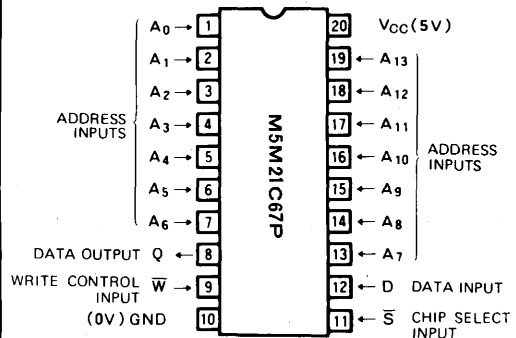
DESCRIPTION

This is a family of 16384-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M21C67P-35 ....35 ns (max)
  M5M21C67P-45 ....45 ns (max)
  M5M21C67P-55 ....55 ns (max)
- Low power dissipation Active .... 200 mW (typ)
  Standy by .... 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Interchangeable with Intel's 2167

PIN CONFIGURATION (TOP VIEW)



Outline 20 P4

APPLICATION

High-speed memory systems

FUNCTION

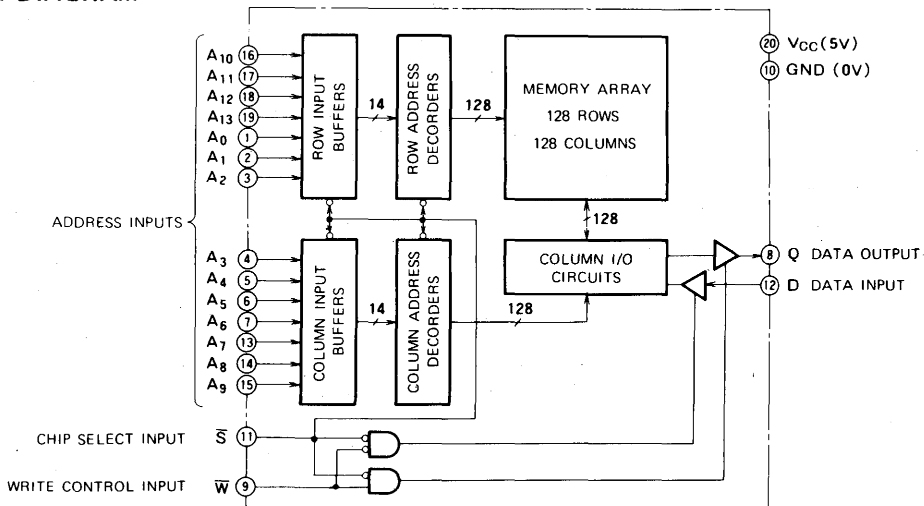
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		−10~85	°C
Tstg	Storage temperature		−65~150	°C

* Pulse width = 20 ns, DC: −0.5V

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−3*		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, DC: −0.5V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		6	V
V_{IL}	Low-level input voltage			−3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA				0.4	V
I_I	Input current	V_I=0 ~ 5.5V				10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}$=2.2V, V_O=0 ~ V_{CC}				50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}$=0.8V Output open	DC		25	50	mA
			AC			80	
I_{CC2}	Stand by current	$V_{I(\bar{S})}$=2.2V Other V_I=2.2V			10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})} \geqq V_{CC}-0.2V$, Other $V_I \leqq 0.2V$ or $V_I \geqq V_{CC}-0.2V$			0.001	2	mA
C_I	Input capacitance	V_I=GND, V_i=25mVrms, f=1MHz				5	pF
Co	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz				6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M21C67P-35			M5M21C67P-45			M5M21C67P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S)}$	Chip select access time			35			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			5			ns
$t_{en(S)}$	Output enable time after chip selection	10			10			10			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		20	0		20	0		25	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power down time after chip deselection			35			45			55	ns

16384-BIT (16384-WORD BY 1-BIT) CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M21C67P-35			M5M21C67P-45			M5M21C67P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	35			45			55			ns
$t_{su(S)}$	Chip select setup time	30			35			40			ns
$t_{su(A)_1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			0			ns
$t_{su(A)_2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			0			ns
$t_{w(W)}$	Write pulse width	20			25			30			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{su(D)}$	Data setup time	20			25			25			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		15	0		20	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	30			35			40			ns

CONDITIONS

Input pulse levels . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . . . 0.8V ~ 2V
Output load . . . . Fig. 1, Fig. 2

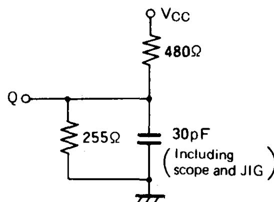


Fig. 1 Output load

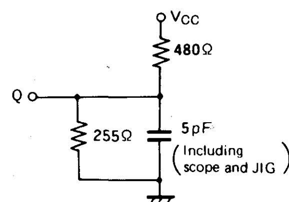
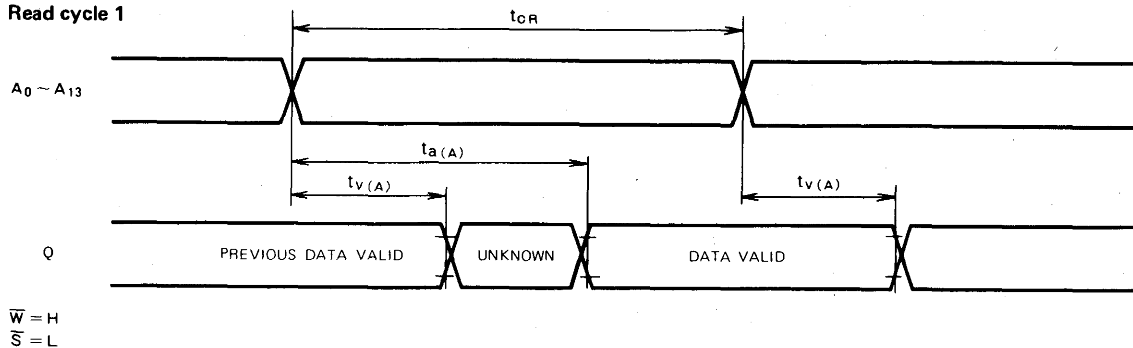


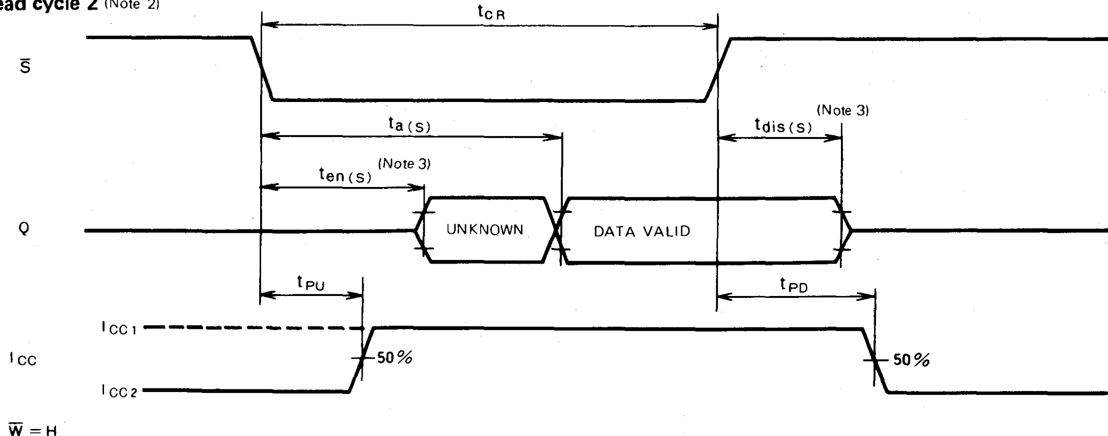
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



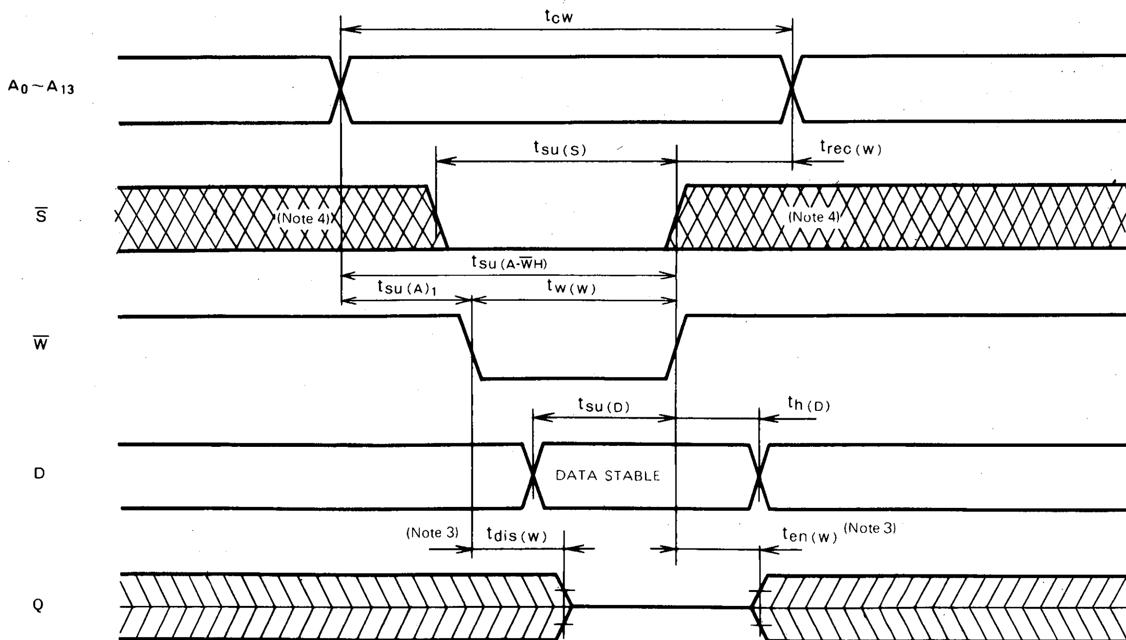
Read cycle 2 (Note 2)



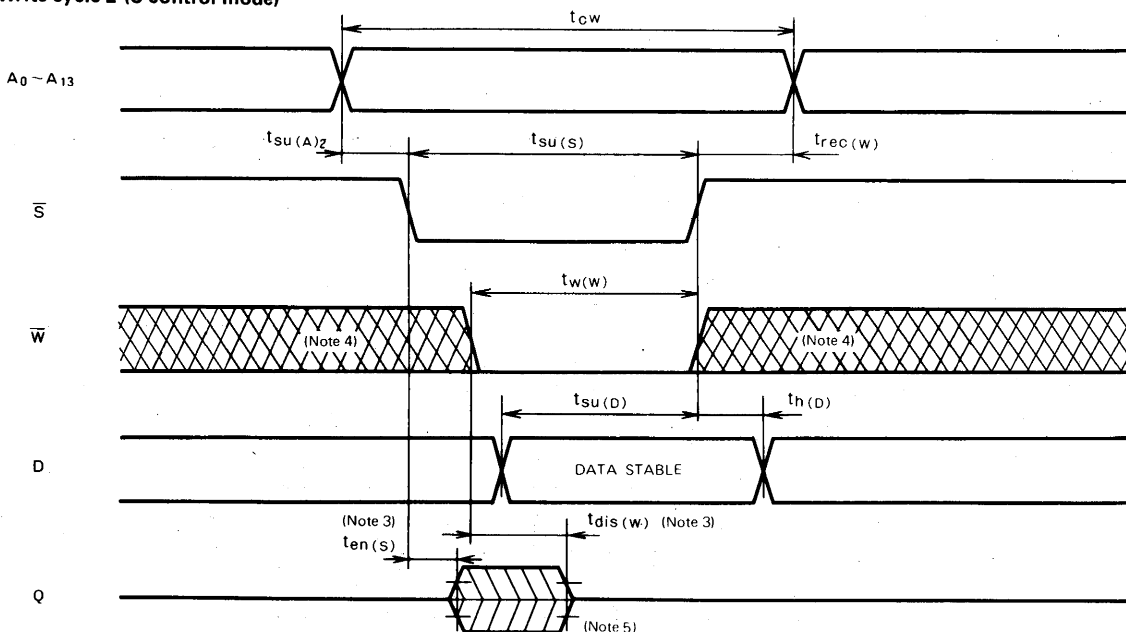
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

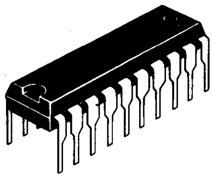
Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.



M5M21C68P-35, -45, -55

16384-BIT (4096-WORD BY 4-BIT) CMOS STATIC RAM

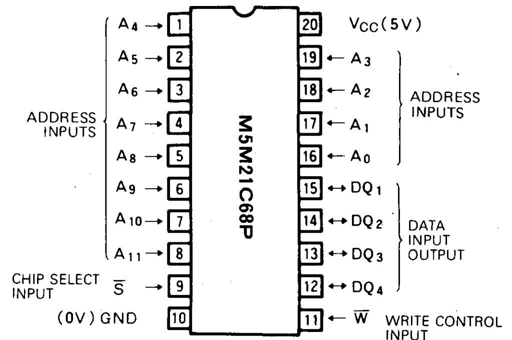
DESCRIPTION

This is a family of 4096 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M21C68P-35 ...... 35 ns (max)
  M5M21C68P-45 ...... 45 ns (max)
  M5M21C68P-55 ...... 55 ns (max)
- Low power dissipation Active .... 200 mW (typ)
  Standy by .... 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Interchangeable with Intel's 2168

PIN CONFIGURATION (TOP VIEW)



Outline 20 P4

APPLICATION

High-speed memory systems

FUNCTION

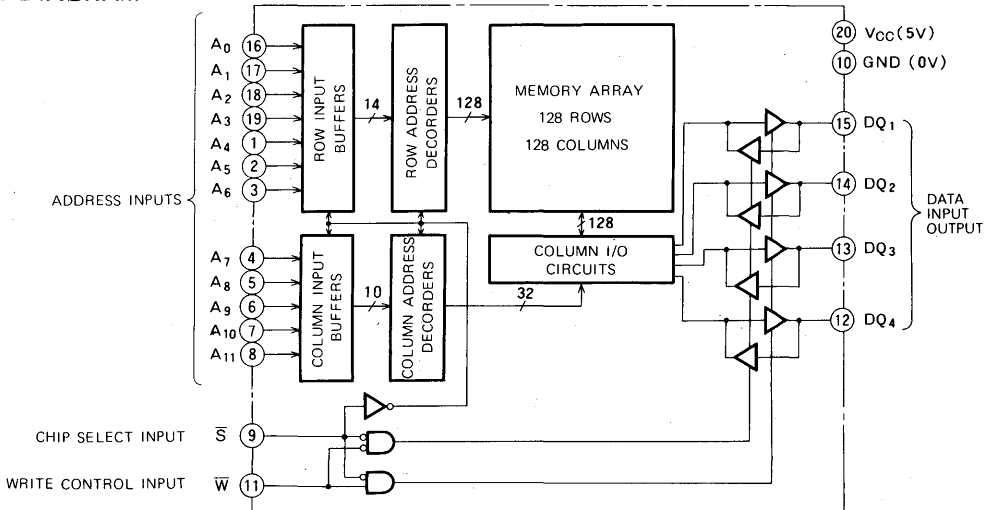
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



16384-BIT (4096-WORD BY 4-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	$-3.5^{*}\sim 7$	V
V_I	Input voltage		$-3.5^{*}\sim 7$	V
V_O	Output voltage		$-3.5^{*}\sim 7$	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		$-10\sim 85$	°C
Tstg	Storage temperature		$-65\sim 150$	°C

* Pulse width = 20 ns, DC: -0.5V

RECOMMENDED OPERATING CONDITIONS ($T_a = 0\sim 70°C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-3^{*}		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, DC: -0.5V

ELECTRICAL CHARACTERISTICS ($T_a = 0\sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		6	V
V_{IL}	Low-level input voltage			-3^{*}		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA		2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA				0.4	V
I_I	Input current	$V_I = 0\sim 5.5V$				10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})} = 2.2V$, $V_O = 0\sim V_{CC}$				50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})} = 0.8V$ Output open	DC		25	50	mA
			AC			80	
I_{CC2}	Stand by current	$V_{I(\bar{S})} = 2.2V$ Other $V_I \leq 0.2V$			10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})} \geq V_{CC} - 0.2V$, Other $V_I \leq 0.2V$ or $V_I \geq V_{CC} - 0.2V$			0.001	2	mA
C_I	Input capacitance	$V_I = GND$, $V_i = 25mVrms$, $f = 1MHz$					pF
Co	Output capacitance	$V_O = GND$, $V_o = 25mVrms$, $f = 1MHz$					pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, DC: -0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a = 0\sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M21C68P-35			M5M21C68P-45			M5M21C68P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S)}$	Chip select access time			35			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			5			ns
$t_{en(S)}$	Output enable time after chip selection	15			20			20			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		20	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power down time after chip deselection			35			45			55	ns

TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M21C68P-35			M5M21C68P-45			M5M21C68P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	35			45			55			ns
$t_{su(S)}$	Chip select setup time	30			35			40			ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			0			ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			0			ns
$t_{w(W)}$	Write pulse width	30			35			40			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{su(D)}$	Data setup time	15			20			20			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		15	0		20	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			5			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	30			35			40			ns

CONDITIONS

Input pulse levels . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . . . 0.8V ~ 2V
Output load . . . . Fig. 1, Fig. 2

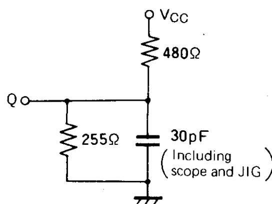


Fig. 1 Output load

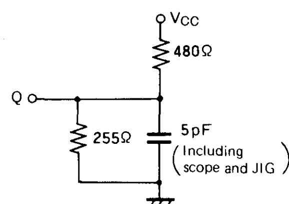
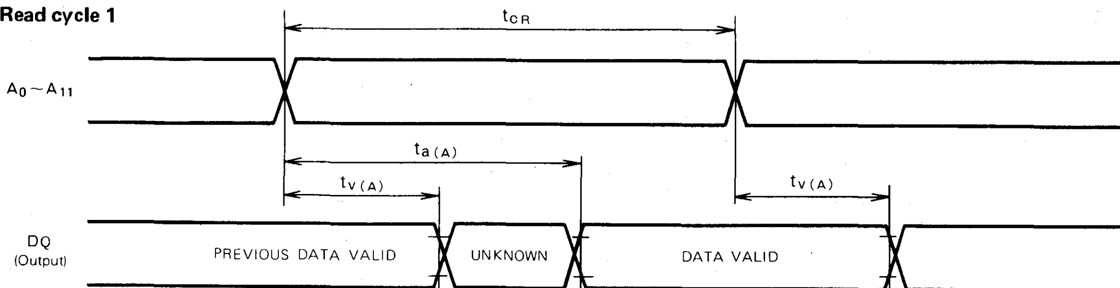


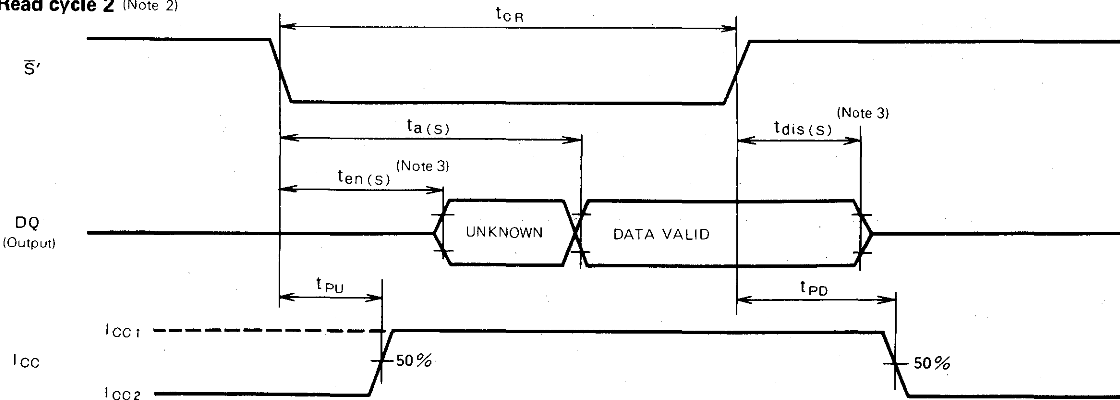
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



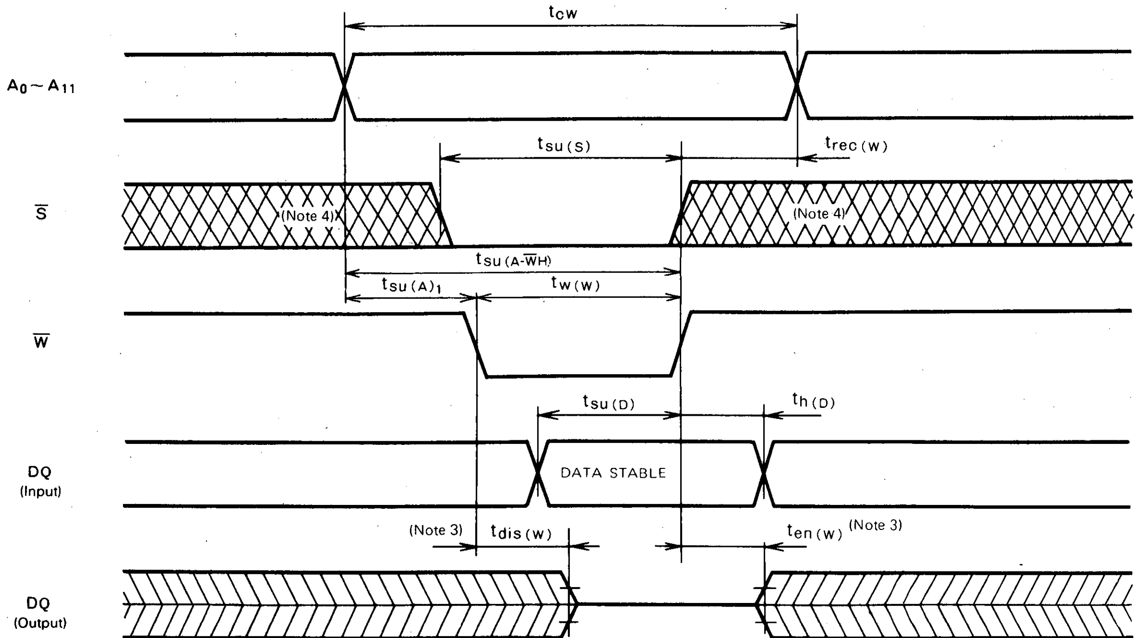
Read cycle 2 (Note 2)



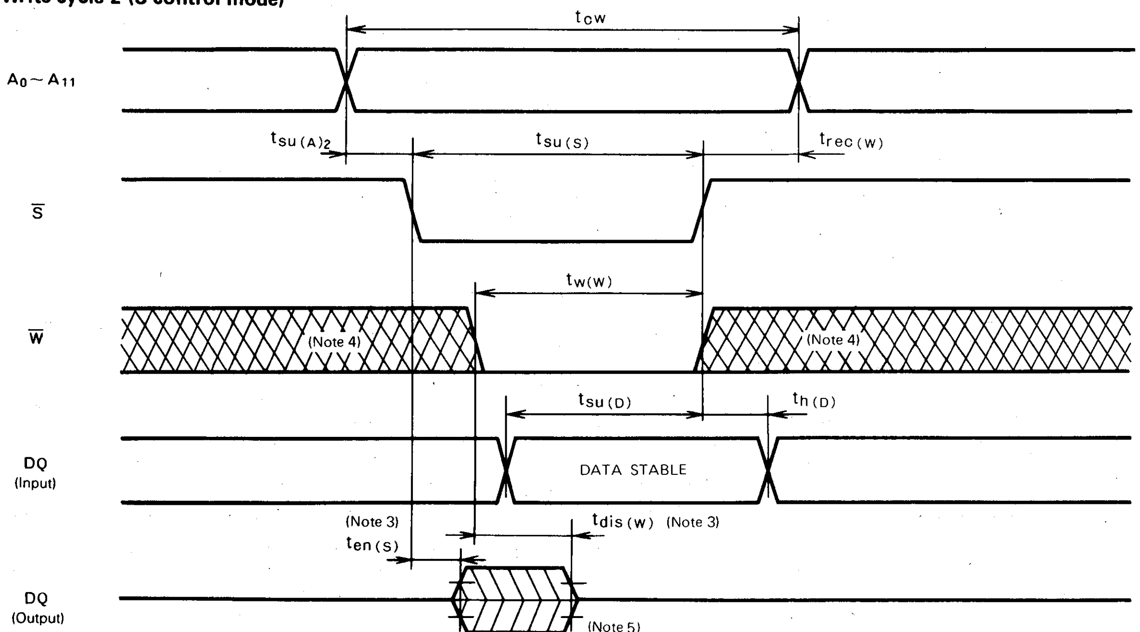
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

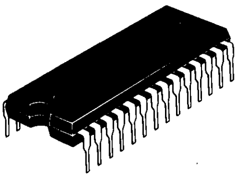
Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.



M5M5165P-70, -10, -12, -15, -70L, -10L, -12L, -15L

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5165P is a 65,536-bit CMOS static RAM organized as 8,192 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 8K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5165P-70	70ns	50mA	2mA
M5M5165P-10	100ns		
M5M5165P-12	120ns		
M5M5165P-15	150ns		
M5M5165P-70L	70ns		100μA
M5M5165P-10L	100ns		
M5M5165P-12L	120ns		
M5M5165P-15L	150ns		

- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S_1}$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O
- Pinout Compatible with 64K EPROM M5L2764K

APPLICATION

Small Capacity Memory Units.

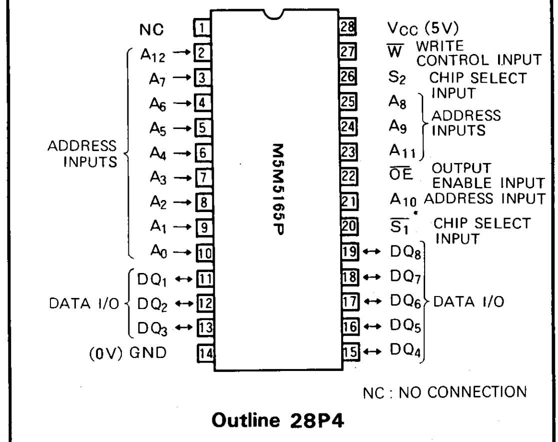
FUNCTION

The operation mode of the M5M5165P is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is excuted whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requring the set-up and hold time relative to these edge to be maintained. The Output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

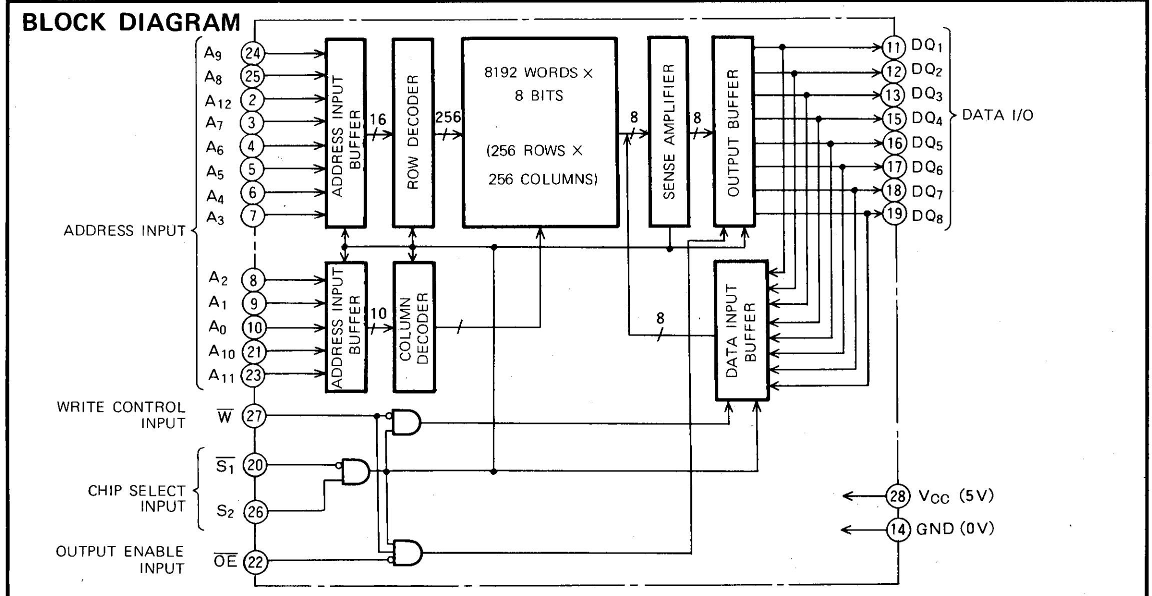
A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L,

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



S_2=H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ *	I_{CC}
X	L	X	X	Non selection	high-impedance	Standby
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA	2.4			V
V_{OL}	Low output voltage	I_{OL}= 2 mA			0.4	V
I_I	Input current	V_I=0～V_{CC}			±1	μA
I_{OZH}	High level output current in off-state	$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0−V_{CC}			1	μA
I_{OZL}	Low level output current in off-state				−1	μA
I_{CC1}	Active supply current	$\overline{S_1}$≦0.2, S_2≧V_{CC}−0.2 Outout open. Other inputs ≦0.2 or ≧V_{CC}−0.2		30	45	mA
I_{CC2}	Active supply current	$\overline{S_1}$=V_{IL} or S_2=V_{IH} Output open Other inputs =V_{IH}		35	50	mA
I_{CC3}	Stand-by supply current	① S_2≦0.2V, Other inputs=0～V_{CC} ② $\overline{S_1}$≧V_{CC}−0.2V, S_2≧V_{CC}−0.2V, Other inputs =0～V_{CC}			2(P)	mA
					100(P-L)	μA
I_{CC4}	Stand-by supply current	S_2=V_{IL}, $\overline{S_1}$=V_{IH}, Other inputs=0～V_{CC}			3	mA
Ci	Output capacitance (Ta=25°C)	V_I=GND, Vi=25mVrms, f=1MHz			6	pF
Co	Outout capacitance (Ta=25°C)	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5165P-70 M5M5165P-70L			M5M5165P-10 M5M5165P-10L			M5M5165P-12 M5M5165P-12L			M5M5165P-15 M5M5165P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			100			120			150			ns
$t_{a(A)}$	Address access time			70			100			120			150	ns
$t_{a(S_1)}$	Chip select 1 access time			70			100			120			150	ns
$t_{a(S_2)}$	Chip select 2 access time			70			100			120			150	ns
$t_{a(OE)}$	Output enable access time			35			50			60			70	ns
$t_{dis(S_1)}$	Output disable time after $\overline{S_1}$ high			30			35			40			50	ns
$t_{dis(S_2)}$	Output disable time after S_2 low			30			35			40			50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35			40			50	ns
$t_{en(S_1)}$	Output enable time after $\overline{S_1}$ low	5			10			10			10			ns
$t_{en(S_2)}$	Output enable time after S_2 high	5			10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

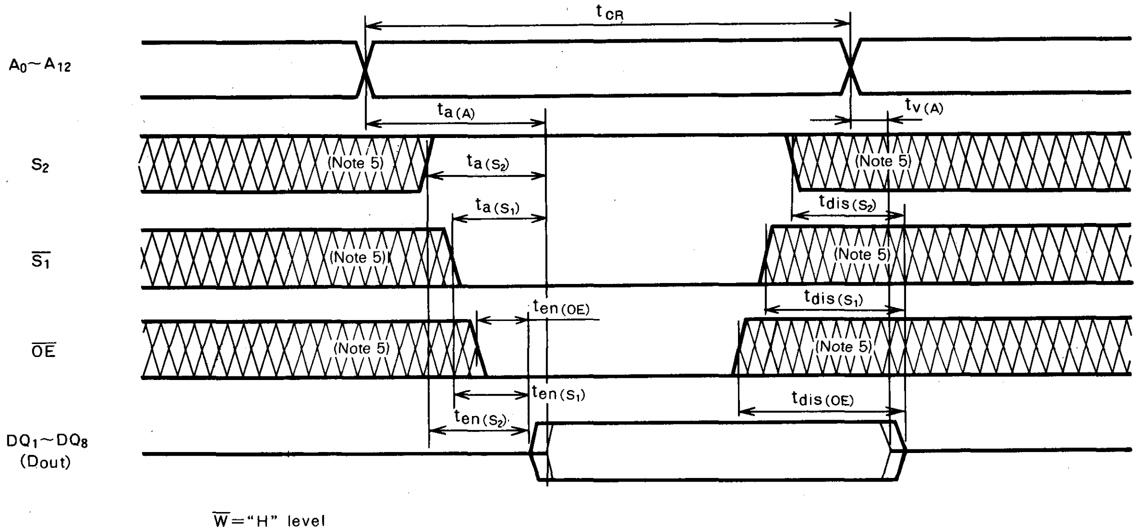
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits												Unit
		M5M5165P-70 M5M5165P-70L			M5M5165P-10 M5M5165P-10L			M5M5165P-12 M5M5165P-12L			M5M5165P-15 M5M5165P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			100			120			150			ns
$t_{w(W)}$	Write pulse width	40			60			70			90			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(S)}$	Chip select set up time	65			80			85			100			ns
$t_{su(D)}$	Data set up time	30			35			40			50			ns
$t_{h(D)}$	Data hold time	5			5			5			5			ns
$t_{rec(W)}$	Write recovery time	5			5			10			10			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		30			35			40			50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		30			35			40			50	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			10			10			10			ns

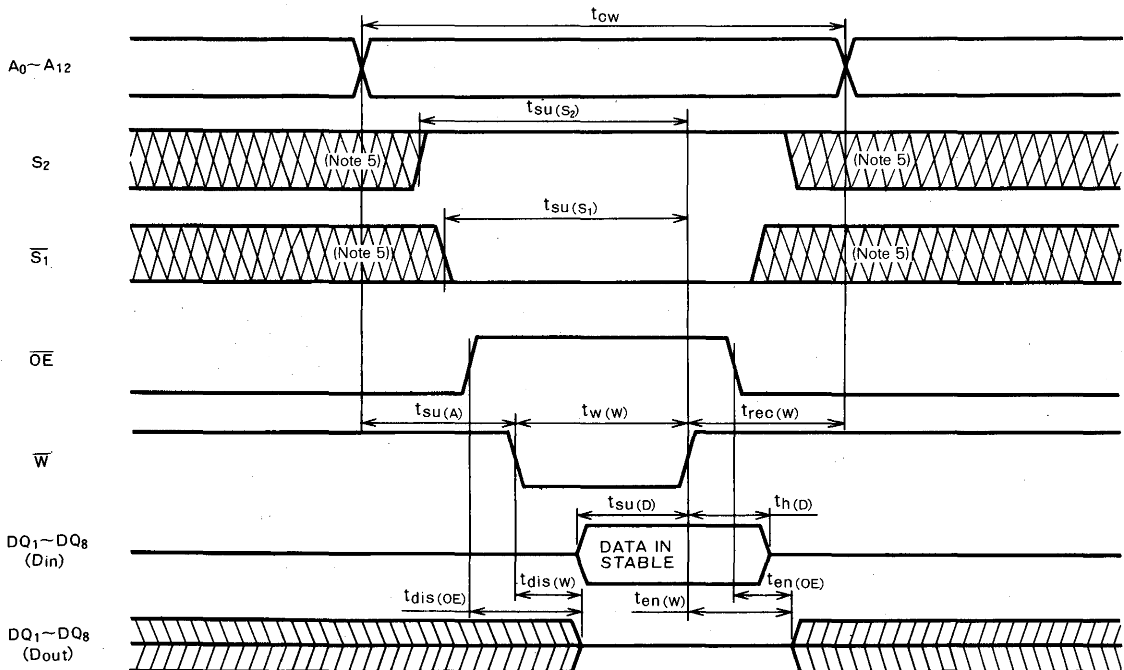
TIMING DIAGRAM

Read cycle

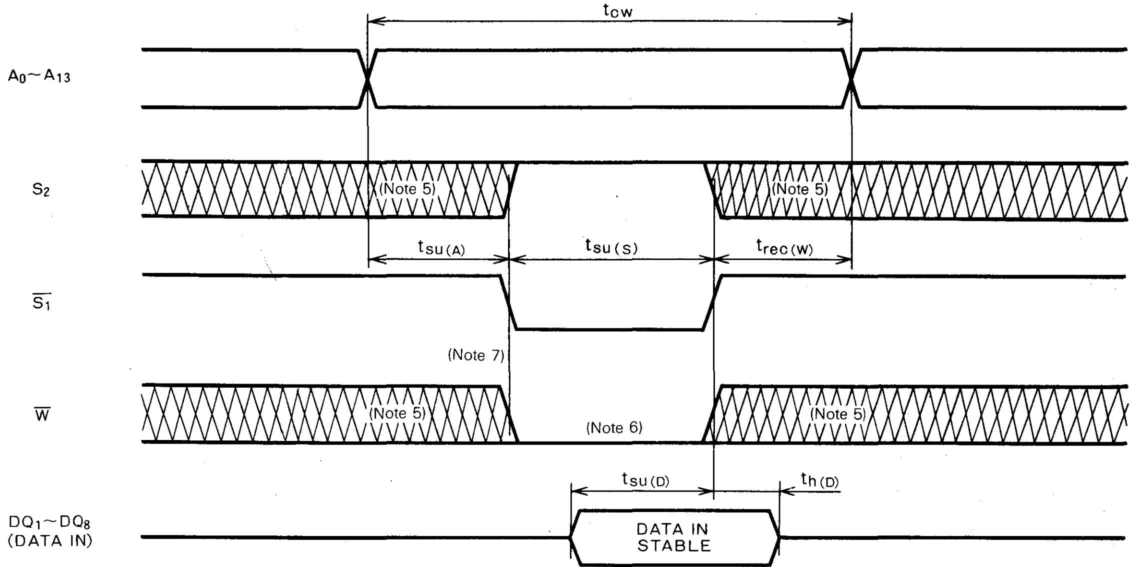


W="H" level

Write cycle (WE control)



Write cycle (S control)



Note 4: Test condition
Input pulse level: 0.6~2.4V
Input pulse rise, fall time: 10ns
Load: 1 TTL, C_L = 100pF (P-15, P-12, P-10, P-15L, P-12L, P-10L)
C_L=30pF (P-70, P-70L)
Conditions of assessment: 1.5V
5: Hatching indicates the state is don't care.
6: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
7: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high-impedance state.
8: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S_1})}$	Chip select input $\overline{S_1}$	$2.2V \leqq V_{CC(PD)}$	2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$		$V_{CC(PD)}$		
$V_{I(S_2)}$	Chip select input S_2	$4.5V \leqq V_{CC(PD)}$			0.8	V
		$V_{CC(PD)} < 4.5V$			0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC}=3V$, Other inputs $=3V$			2(P)	mA
					* 50(P-L)	μA

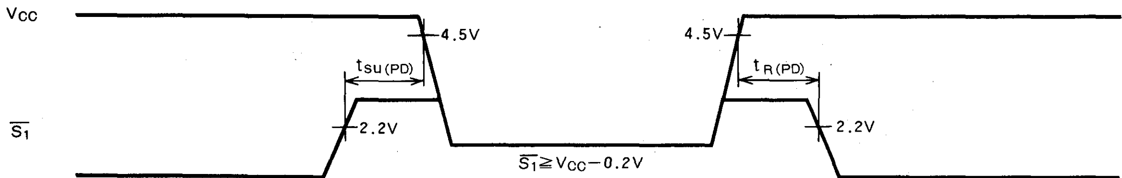
Note 3: When $\overline{S_1}$ is operated at 2.2V (V_{IH} min) and the supply voltage is between 4.5V and 2.4V, supply current is defined as I_{CC4}.
*: $I_{CC}(PD) = 20\mu A$max, Ta = 0 ~ 40°C

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

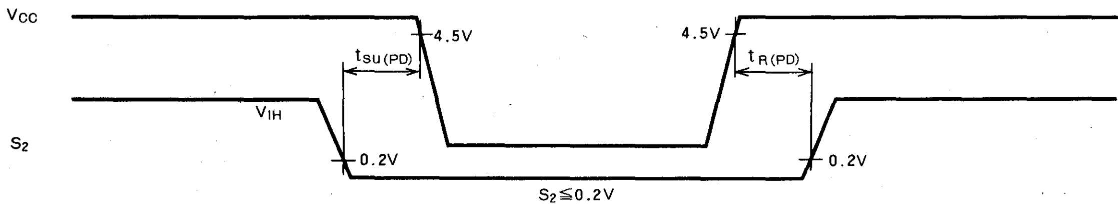
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

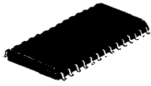
$\overline{S_1}$ control



S_2 control



M5M5165FP-70, -10, -12, -15, -70L, -10L, -12L, -15L



65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5165FP is a 65536-bit CMOS static RAM organized as 8192 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a 28 pin flat package.

FEATURES

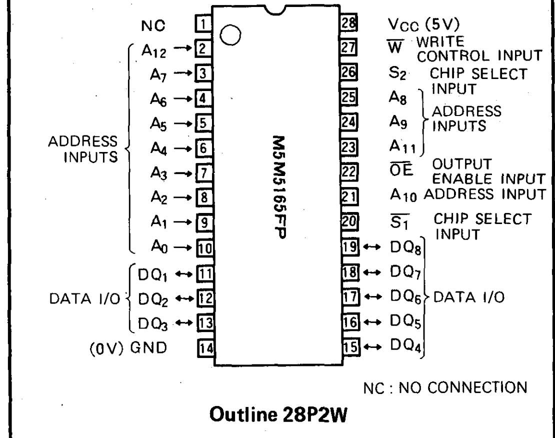
Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5165FP-70	70ns	50mA	2mA
M5M5165FP-10	100ns		
M5M5165FP-12	120ns		
M5M5165FP-15	150ns		
M5M5165FP-70L	70ns		100μA
M5M5165FP-10L	100ns		
M5M5165FP-12L	120ns		
M5M5165FP-15L	150ns		

- Small Outline Package
- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S_1}$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O

APPLICATION

Small Capacity Memory Units.

PIN CONFIGURATION (TOP VIEW)



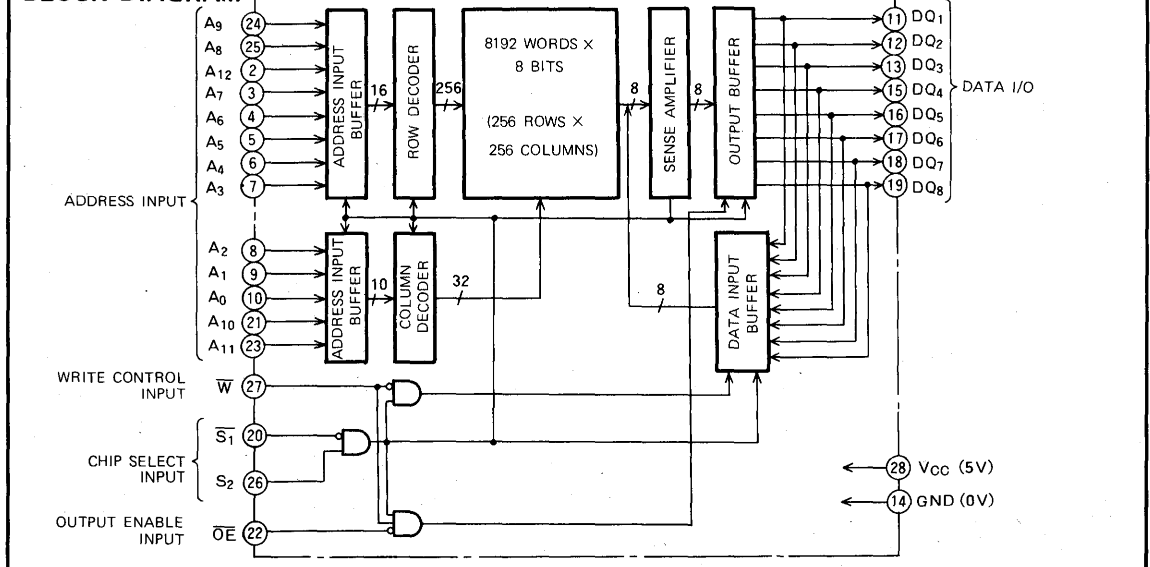
Outline 28P2W

FUNCTION

The operation mode of the M5M5165FP is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is excuted whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The Output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level,

BLOCK DIAGRAM



the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2=H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
X	L	X	X	Non selection	high-impedance	Standby
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA	2.4			V
V_{OL}	Low output voltage	I_{OL}=2 mA			0.4	V
I_I	Input current	V_I=0~V_{CC}			±1	μA
I_{OZH}	High level output current in off-state	$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0−V_{CC}			1	μA
I_{OZL}	Low level output current in off-state				−1	μA
I_{CC1}	Active supply current	$\overline{S_1}$≦0.2, S_2≧V_{CC}−0.2 Outout open Other inputs ≦0.2 or ≧V_{CC}−0.2		30	45	mA
I_{CC2}	Active supply current	$\overline{S_1}$=V_{IL} or S_2=V_{IH} Output open Other inputs =V_{IH}		35	50	mA
I_{CC3}	Stand-by supply current	① S_2≦0.2V, Other inputs=0~V_{CC} ② $\overline{S_1}$≧V_{CC}−0.2V, S_2≧V_{CC}−0.2V, Other inputs =0~V_{CC}			2(P) 100(P−L)	mA μA
I_{CC4}	Stand-by supply current	S_2=V_{IL}, $\overline{S_1}$=V_{IH}, Other inputs=0~V_{CC}			3	mA
Ci	Output capacitance (Ta=25°C)	V_I=GND, V_i=25mVmrs, f=1MHz			6	pF
Co	Outout capacitance (Ta=25°C)	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5 V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5165FP-70 M5M5165FP-70L			M5M5165FP-10 M5M5165FP-10L			M5M5165FP-12 M5M5165FP-12L			M5M5165FP-15 M5M5165FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			100			120			150			ns
$t_{a(A)}$	Address access time			70			100			120			150	ns
$t_{a(S_1)}$	Chip select 1 access time			70			100			120			150	ns
$t_{a(S_2)}$	Chip select 2 access time			70			100			120			150	ns
$t_{a(OE)}$	Output enable access time			35			50			60			70	ns
$t_{dis(S_1)}$	Output disable time after $\overline{S_1}$ high			30			35			40			50	ns
$t_{dis(S_2)}$	Output disable time after S_2 low			30			35			40			50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35			40			50	ns
$t_{en(S_1)}$	Output enable time after $\overline{S_1}$ low	5			10			10			15			ns
$t_{en(S_2)}$	Output enable time after S_2 high	5			10			10			15			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			10			10			15			ns
$t_{V(A)}$	Data valid time after address change	10			10			10			10			ns

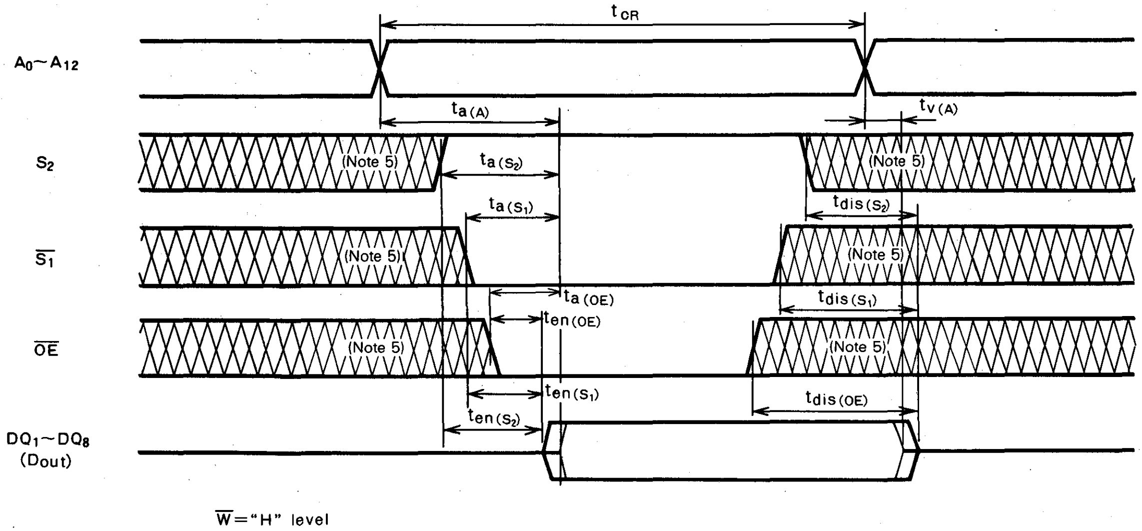
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, V_{CC} = 5 V ± 10%, unless otherwise noted)

Write cycle

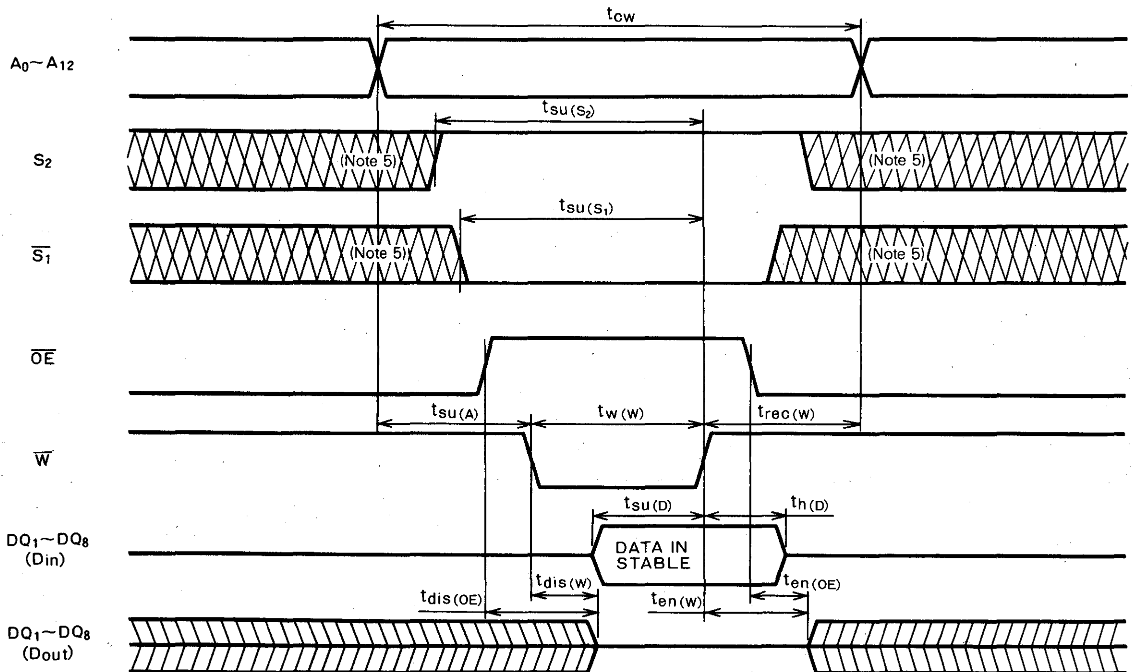
Symbol	Parameter	Limits												Unit
		M5M5165FP-70 M5M5165FP-70L			M5M5165FP-10 M5M5165FP-10L			M5M5165FP-12 M5M5165FP-12L			M5M5165FP-15 M5M5165FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			100			120			150			ns
$t_{W(W)}$	Write pulse width	40			60			70			90			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(S)}$	Chip select set up time	65			80			85			100			ns
$t_{su(D)}$	Data set up time	30			35			40			50			ns
$t_{h(D)}$	Data hold time	5			5			5			5			ns
$t_{rec(W)}$	Write recovery time	5			5			5			5			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		30			35			40			50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		30			35			40			50	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			10			10			15			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			10			10			15			ns

TIMING DIAGRAM

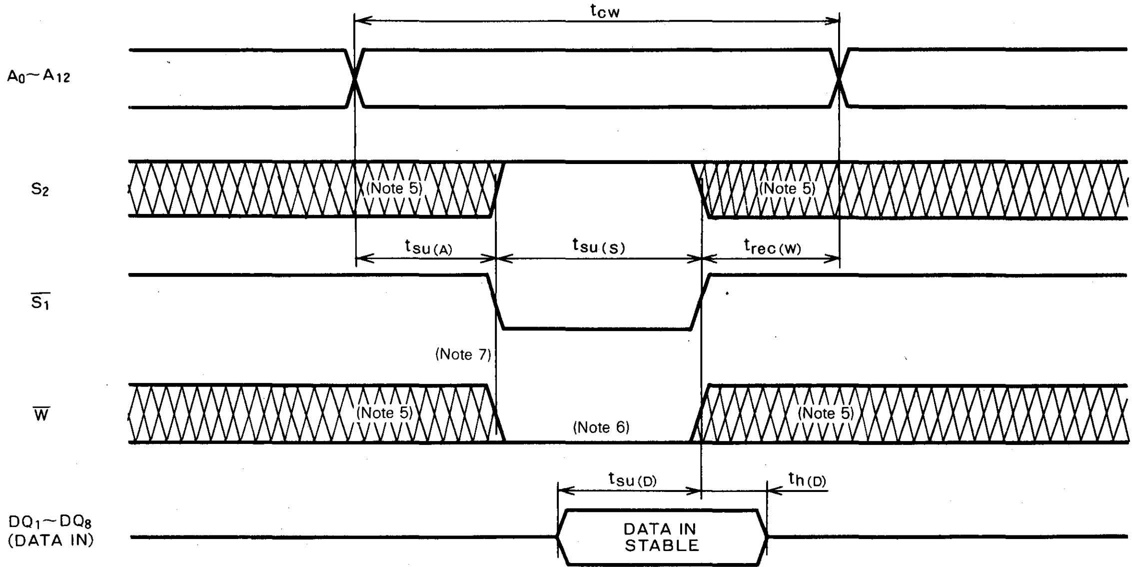
Read cycle



Write cycle (WE control)



Write cycle (S control)



Note 4: Test condition
- Input pulse level: 0.6 ~ 2.4V
- Input pulse rise, fail time: 10ns
- Load: 1 TTL, C_L = 100pF (FP-15, FP-12, FP-10, FP-15L, FP-12L, FP-10L)
  C_L = 30pF (FP-70, FP-70L)
- Reference level: 1.5V

5: Hatching indicates the state is don't care.
6: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
7: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high-impedance state.
8: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S_1})}$	Chip select input $\overline{S_1}$	$2.2V \leqq V_{CC(PD)}$	2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$		$V_{CC(PD)}$		
$V_{I(S_2)}$	Chip select input S_2	$4.5V \leqq V_{CC(PD)}$			0.8	V
		$V_{CC(PD)} < 4.5V$			0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC}=3V$, Other inputs $=3V$			2(P)	mA
				*	50(P-L)	μA

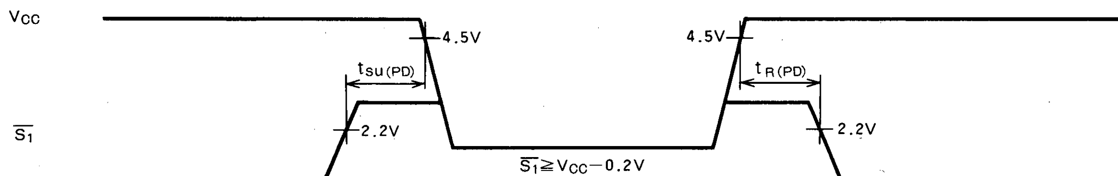
Note 3: When $\overline{S_1}$ is operated at 2.2V (V_{IH} min) and the supply voltage is between 4.5V and 2.4V, supply current is defined as I_{CC4}.
* : I_{cc} (PD) = 20μA max, T_a = 0 ~ 40°C.

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

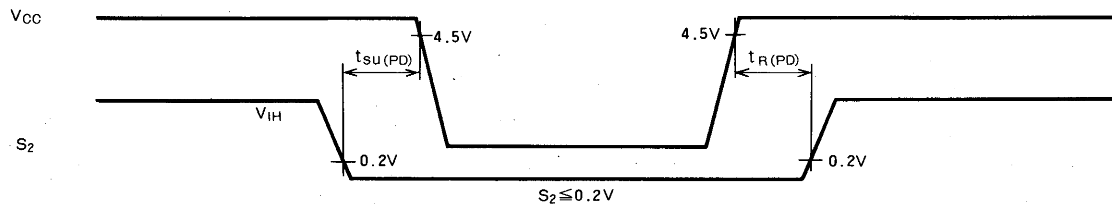
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

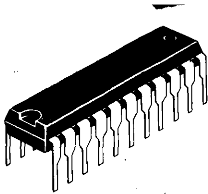
$\overline{S_1}$ control



S_2 control



M5M5187P-45, -55



65536-BIT (65536-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 65536-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

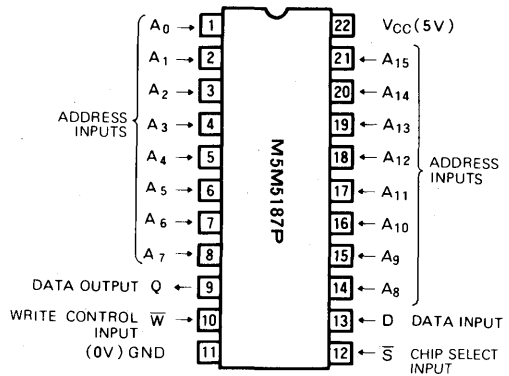
FEATURES

- Fast access time M5M5187P-45 . . . 45 ns (max)
  M5M5187P-55 . . . 55 ns (max)
- Low power dissipation Active .... 300 mW (typ)
  Stand by .... 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 22P4H

FUNCTION

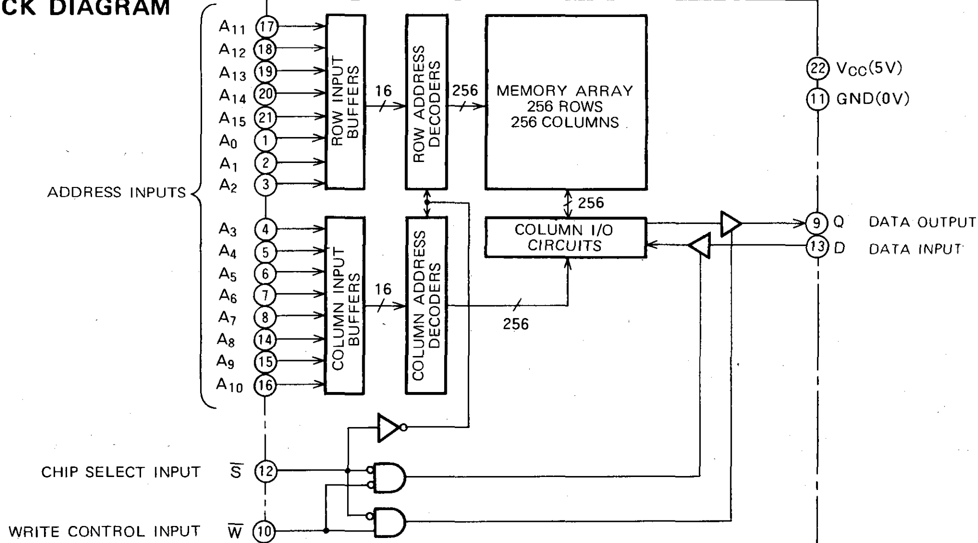
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



65536-BIT (65536-WORD BY 1-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	$-3.5^{*}\sim7$	V
V_I	Input voltage		$-3.5^{*}\sim7$	V
V_O	Output voltage		$-3.5^{*}\sim7$	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		$-10\sim85$	°C
Tstg	Storage temperature		$-65\sim150$	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim70$°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-3^{*}		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		-3^{*}		0.8	V
V_{OH}	High-level output voltage	$I_{OH}=-4$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL}=8$ mA			0.4	V
I_I	Input current	$V_I=0\sim5.5V$			10	μA
$\lvert I_{OZ}\rvert$	Off-state output current	$V_{I(\bar{S})}=2.2V$, $V_O=0\sim V_{CC}$			50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}=0.8V$ Output open			100	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}=2.2V$ Other $V_I\leqq0.2V$		10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})}\geqq V_{CC}-0.2V$, Other $V_I\leqq0.2V$ or $V_I\geqq V_{CC}-0.2V$		0.001	2	mA
C_I	Input capacitance	$V_I=GND$, $V_i=25mVrms$, f=1MHz			5	pF
Co	Output capacitance	$V_O=GND$, $V_o=25mVrms$, f=1MHz			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	M5M5187P-45			M5M5187P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	45			55			ns
$t_{a(A)}$	Address access time			45			55	ns
$t_{a(S)}$	Chip select access time			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Output enable time after chip selection	10			10			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		20	0		25	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			45			55	ns

65536-BIT (65536-WORD BY 1-BIT) CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M5187P-45			M5M5187P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	45			55			ns
$t_{su(S)}$	Chip select setup time	35			40			ns
$t_{su(A)_1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			ns
$t_{su(A)_2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			ns
$t_{w(W)}$	Write pulse width	25			30			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	25			25			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		20	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	35			40			ns

CONDITIONS

Input pulse levels . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . . . 0.8V ~ 2V
Output load . . . . Fig. 1, Fig. 2

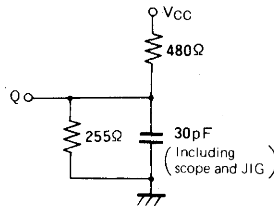


Fig. 1 Output load

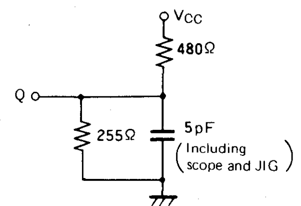
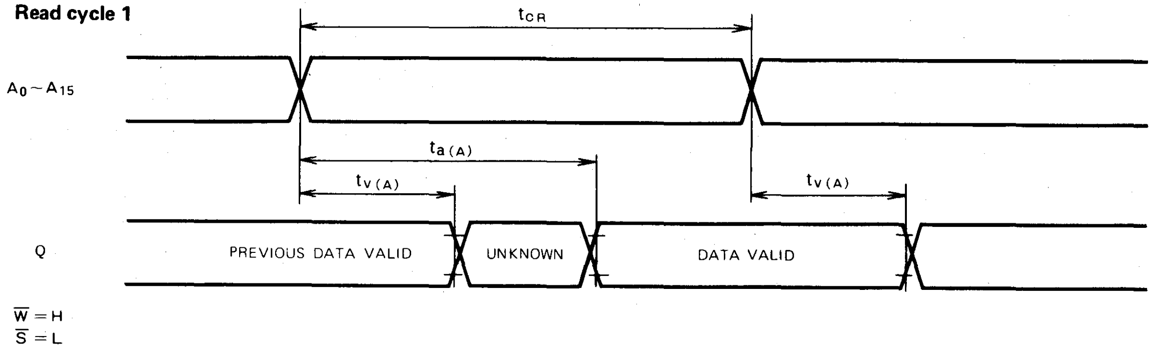


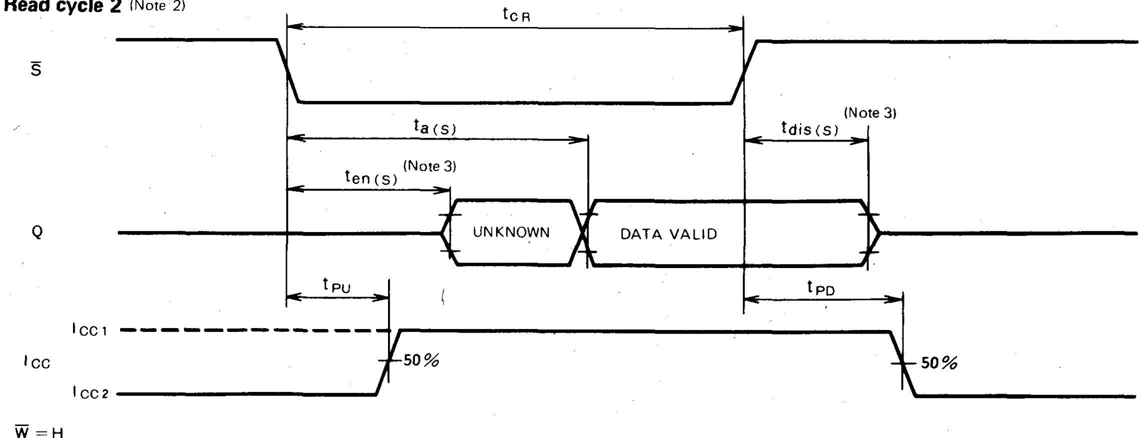
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



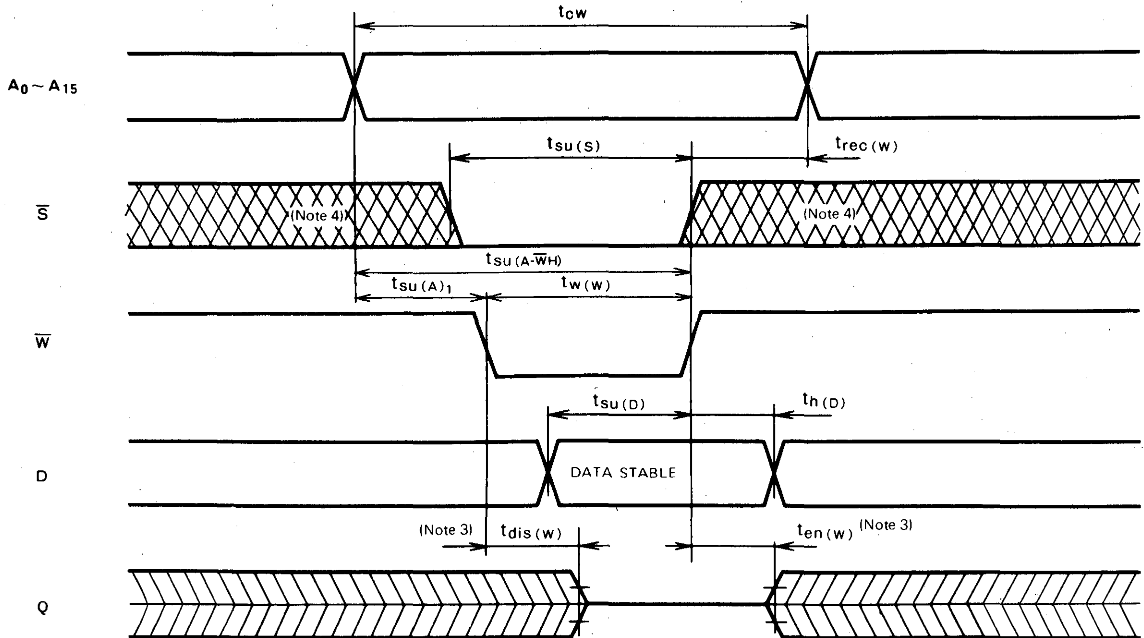
Read cycle 2 (Note 2)



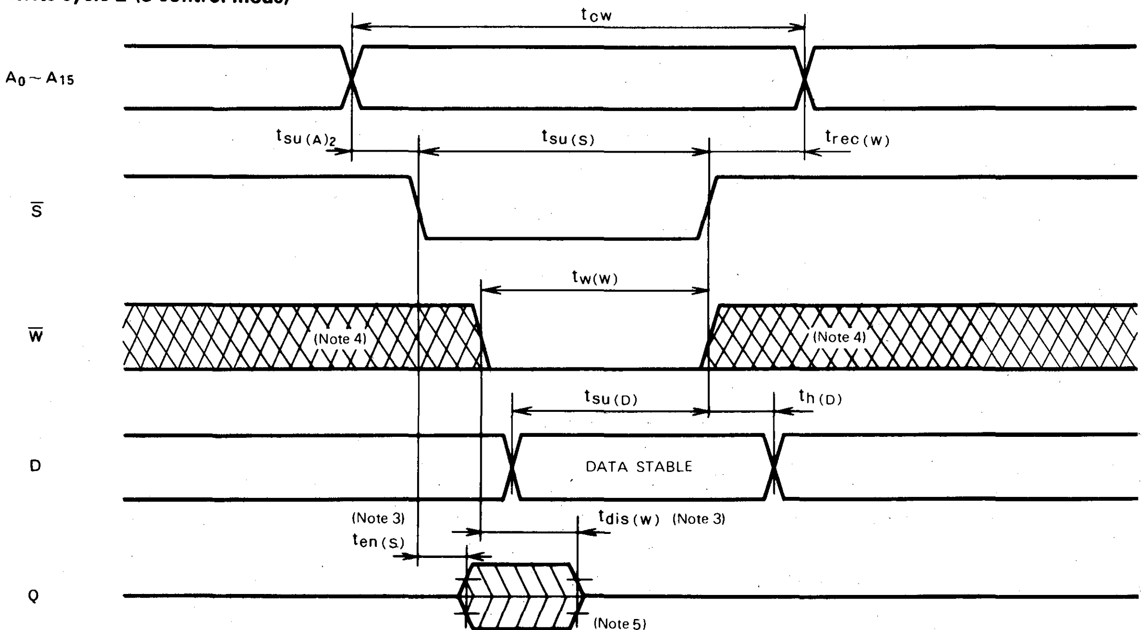
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)



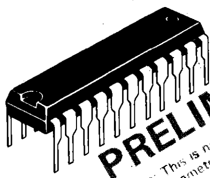
Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

MITSUBISHI ELECTRIC

M5M5187AP-25, -35



65536(65536-WORD BY 1-BIT)CMOS STATIC RAM

DESCRIPTION

This is a family of 65536-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

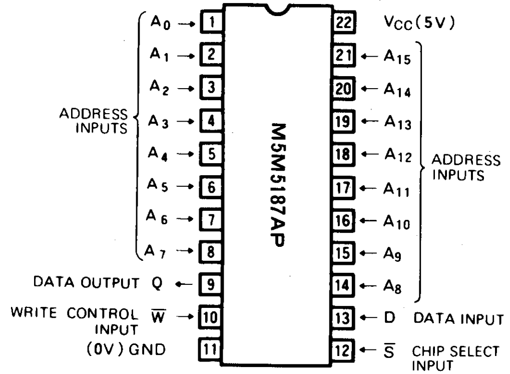
FEATURES

- Fast access time M5M5187AP-25 ... 25 ns (max)
  M5M5187AP-35 ... 35 ns (max)
- Low power dissipation Active .... 300 mW (typ)
  Stand by .... 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 22P4H

FUNCTION

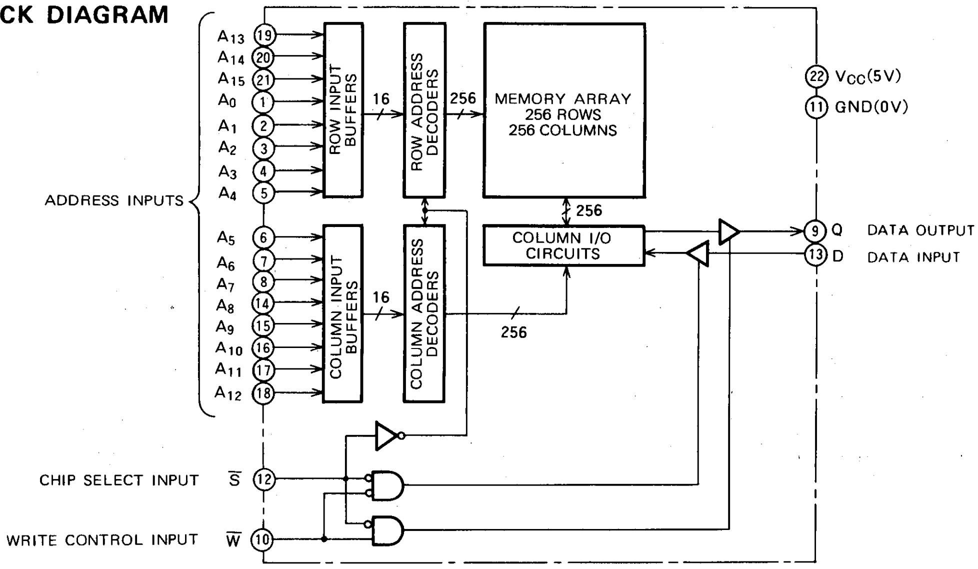
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



65536 (65536-WORD BY 1-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	$-3.5^{*}\sim7$	V
V_I	Input voltage		$-3.5^{*}\sim7$	V
V_O	Output voltage		$-3.5^{*}\sim7$	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		$-10\sim85$	°C
T_{stg}	Storage temperature		$-65\sim150$	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim70$°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-3^{*}		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		-3^{*}		0.8	V
V_{OH}	High-level output voltage	$I_{OH}=-4$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL}=8$ mA			0.4	V
I_I	Input current	$V_I=0\sim V_{CC}$			10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}=2.2V$, $V_O=0\sim V_{CC}$			10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}=0.8V$ Output open			100	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}=2.2V$ Other $V_I\leqq0.2V$		10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})}\geqq V_{CC}-0.2V$, Other $V_I\leqq0.2V$ or $V_I\geqq V_{CC}-0.2V$		0.001	2	mA
C_I	Input capacitance	$V_I=GND$, $V_i=25mVrms$, $f=1MHz$			5	pF
C_O	Output capacitance	$V_O=GND$, $V_o=25mVrms$, $f=1MHz$			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	M5M5187AP-25			M5M5187AP-35			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	25			35			ns
$t_{a(A)}$	Address access time			25			35	ns
$t_{a(S)}$	Chip select access time			25			35	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Output enable time after chip selection	5			5			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		15	0		15	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			25			25	ns

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5187AP-25			M5M5187AP-35			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	25			35			ns
$t_{su(S)}$	Chip select setup time	20			30			ns
$t_{su(A)_1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			ns
$t_{su(A)_2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			ns
$t_{w(W)}$	Write pulse width	20			25			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	20			25			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		10	0		15	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	20			30			ns

CONDITIONS

Input pulse levels . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . . . 0.8V ~ 2V
Output load . . . . Fig. 1, Fig. 2

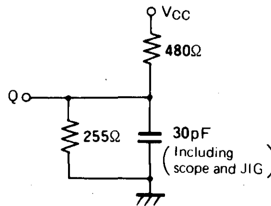


Fig. 1 Output load

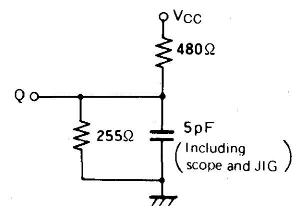
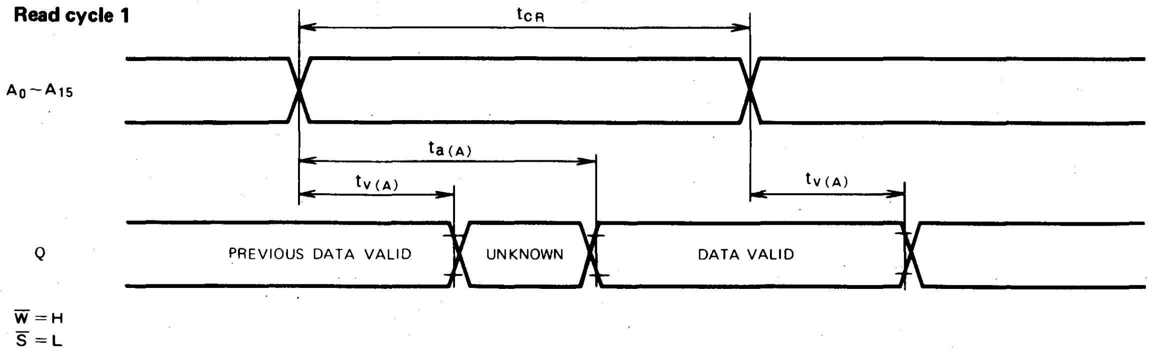


Fig. 2 Output load for ten, tdis

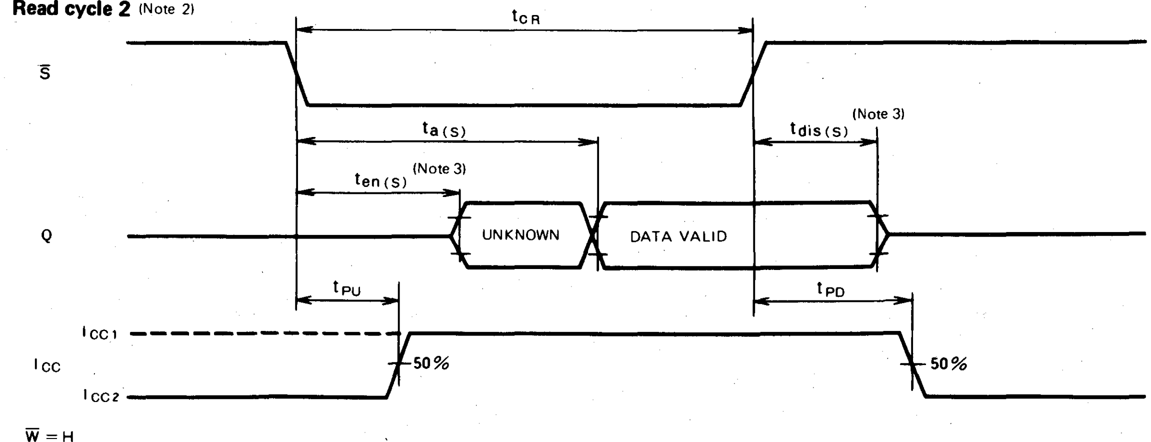
TIMING DIAGRAMS

Read cycle 1



$\overline{W}$ = H
$\overline{S}$ = L

Read cycle 2 (Note 2)

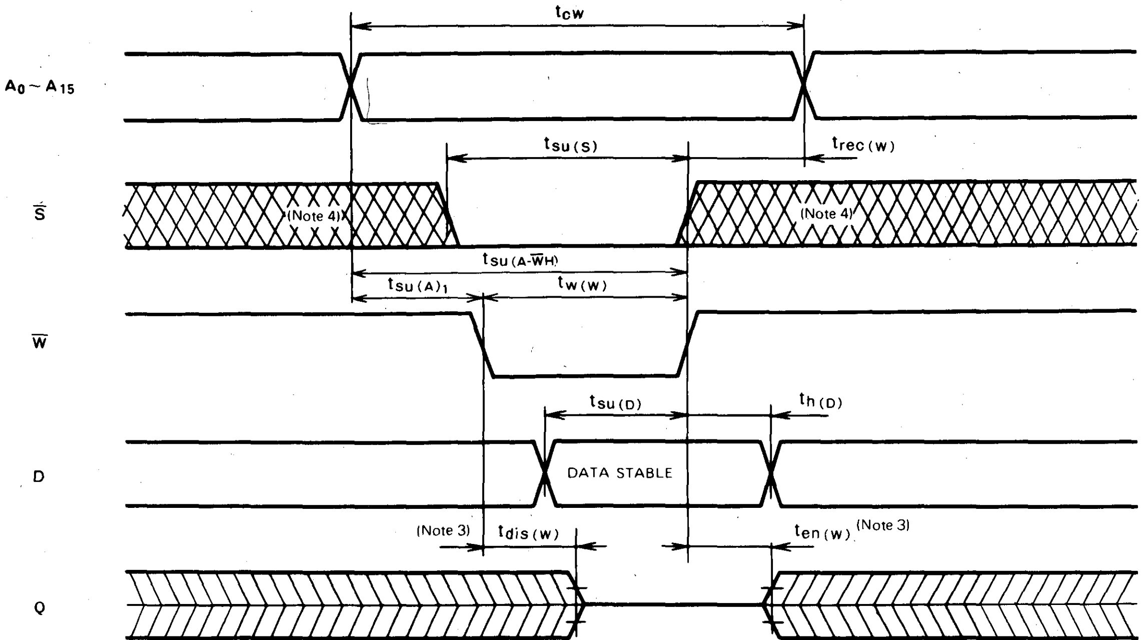


$\overline{W}$ = H

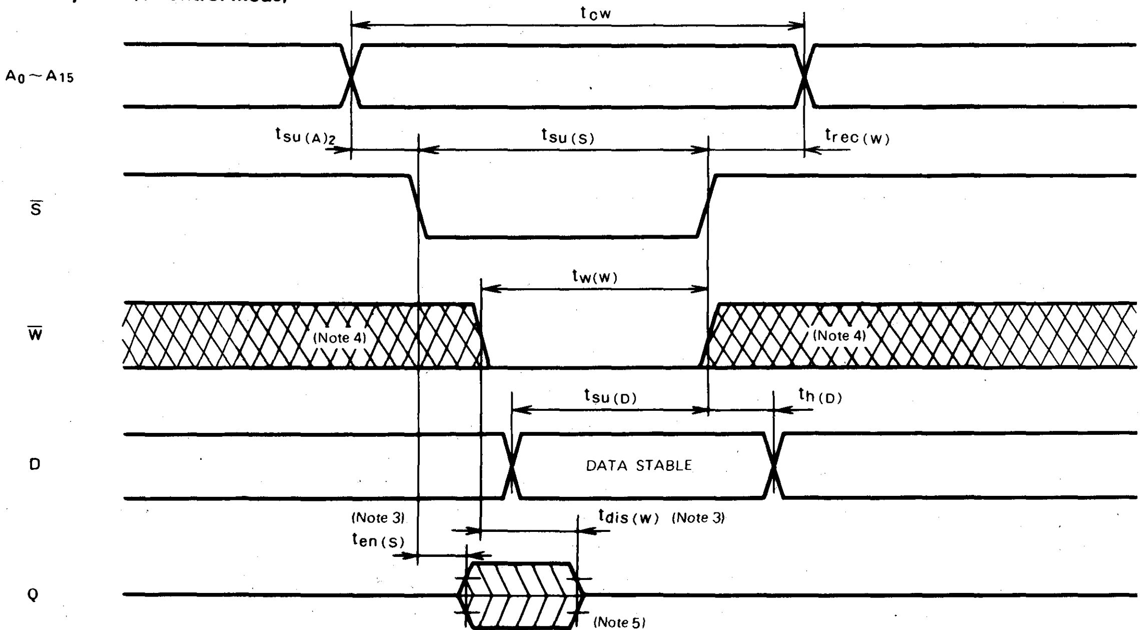
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)

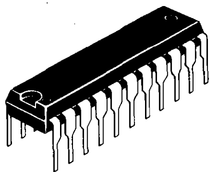


Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

MITSUBISHI ELECTRIC



M5M5188P-45, -55

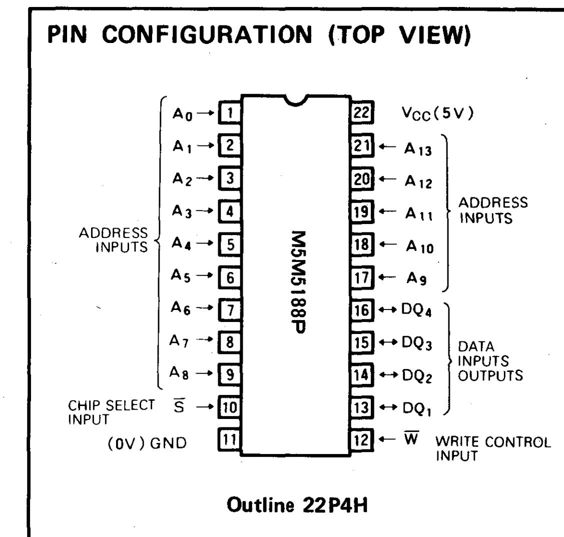
65536-BIT (16384-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION
This is a family of 16384 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES
- Fast access time M5M5188P-45 . . . 45 ns (max)
  M5M5188P-55 . . . 55 ns (max)
- Low power dissipation Active . . . . 300 mW (typ)
  Standby by . . . . . . 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION
High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 22P4H

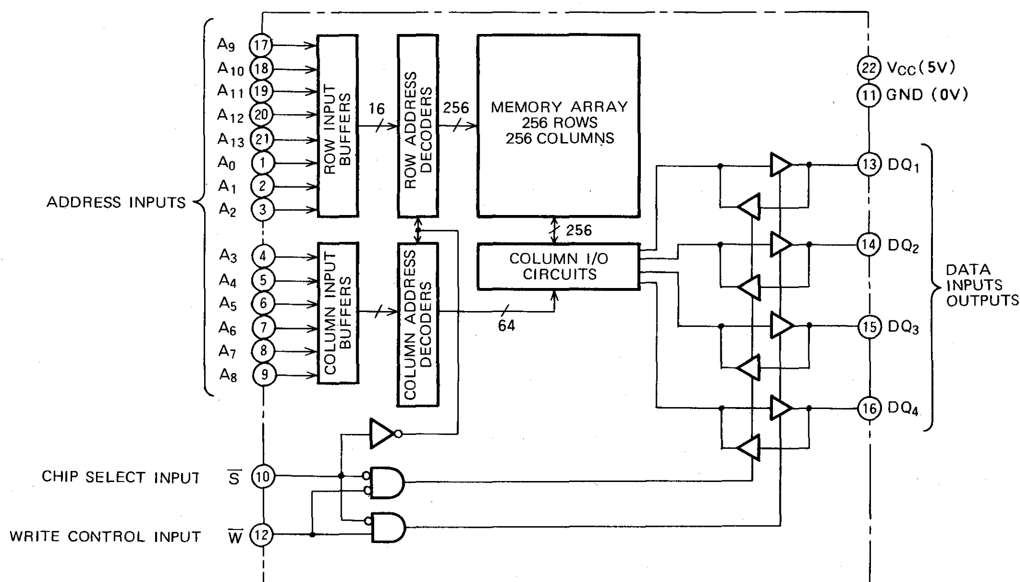
FUNCTION
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	$-3.5^{*}\sim7$	V
V_I	Input voltage	With respect to GND	$-3.5^{*}\sim7$	V
V_O	Output voltage	With respect to GND	$-3.5^{*}\sim7$	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		$-10\sim85$	°C
T_{stg}	Storage temperature		$-65\sim150$	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim70$°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-3^{*}		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		-3^{*}		0.8	V
V_{OH}	High-level output voltage	$I_{OH}=-4$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL}=8$ mA			0.4	V
I_I	Input current	$V_I=0\sim5.5V$			10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}=2.2V$, $V_O=0\sim V_{CC}$			50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}=0.8V$ Output open			100	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}=2.2V$ Other $V_I\leqq0.2V$		10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})}\geqq V_{CC}-0.2V$, Other $V_I\leqq0.2V$ or $V_I\geqq V_{CC}-0.2V$		0.001	2	mA
C_I	Input capacitance	$V_I=GND$, $V_i=25mVrms$, $f=1MHz$			5	pF
C_O	Output capacitance	$V_O=GND$, $V_o=25mVrms$, $f=1MHz$			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a=0\sim70$°C, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	M5M5188P-45			M5M5188P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	45			55			ns
$t_{a(A)}$	Address access time			45			55	ns
$t_{a(S)}$	Chip select access time			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Output enable time after chip selection	20			20			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			45			55	ns

65536-BIT (16384-WORD BY 4-BIT) CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5188P-45			M5M5188P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	45			55			ns
$t_{su(S)}$	Chip select setup time	35			40			ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			ns
$t_{w(W)}$	Write pulse width	35			40			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	20			20			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		20	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	35			40			ns

CONDITIONS

Input pulse levels .... 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level .... 0.8V ~ 2V
Output loads .... Fig. 1, Fig. 2

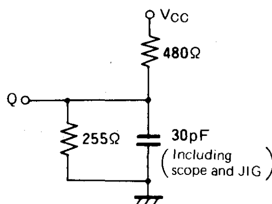


Fig. 1 Output load

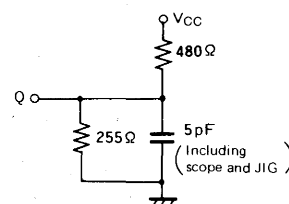
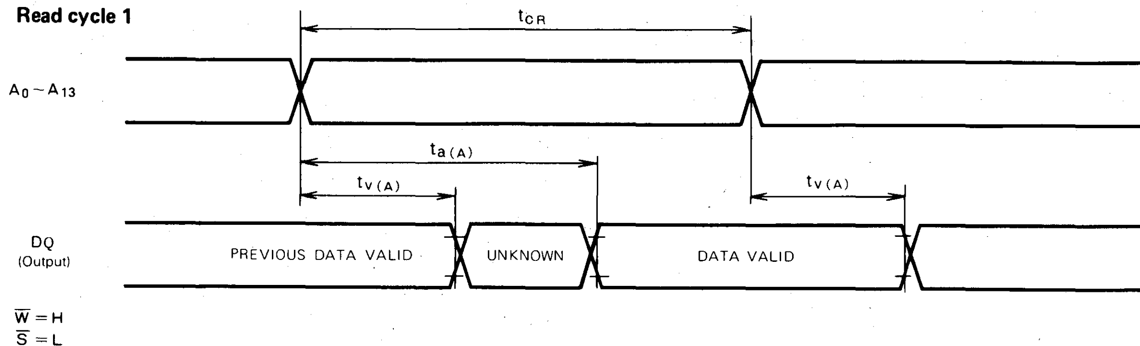


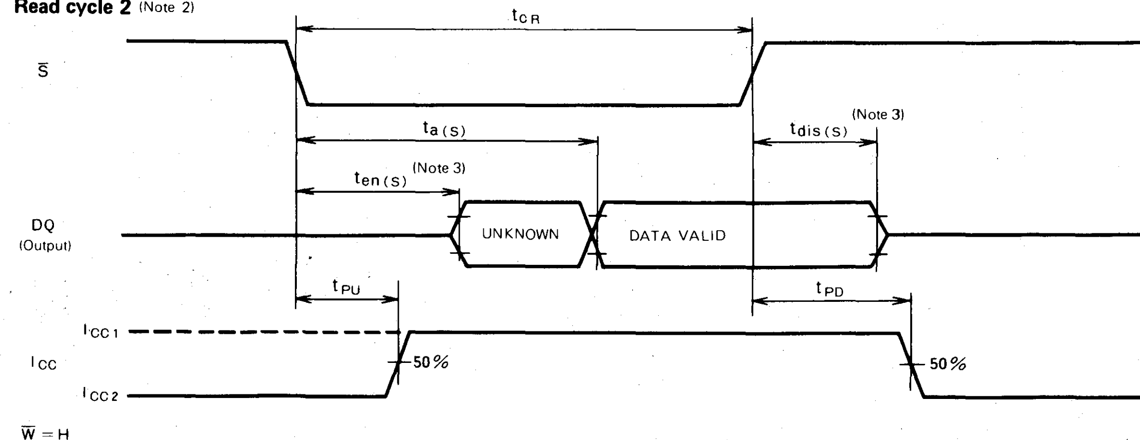
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



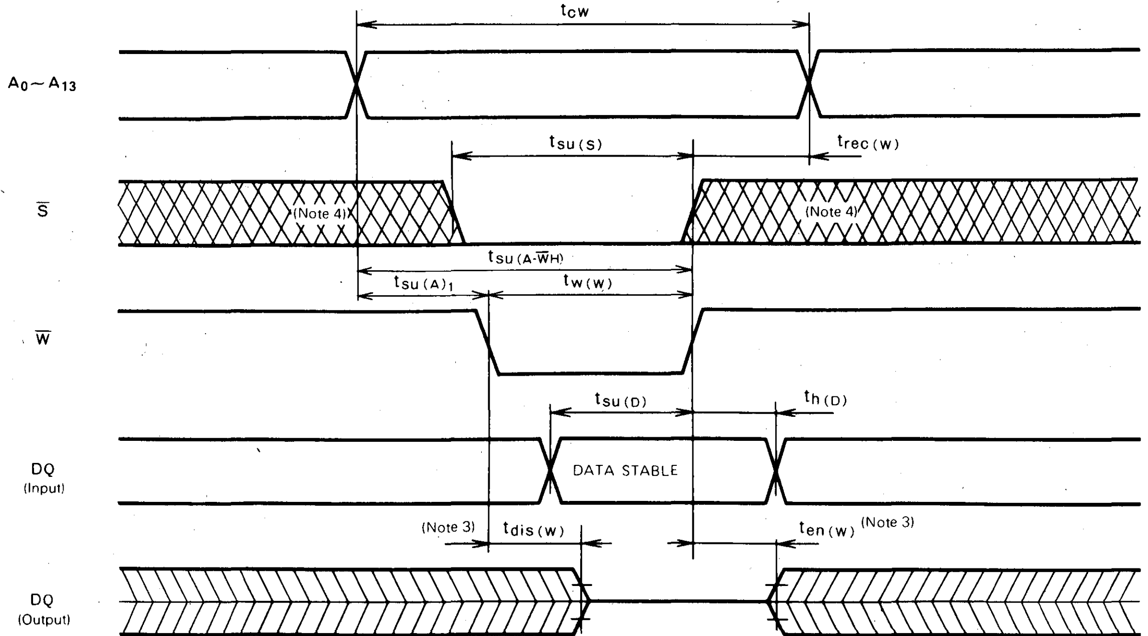
Read cycle 2 (Note 2)



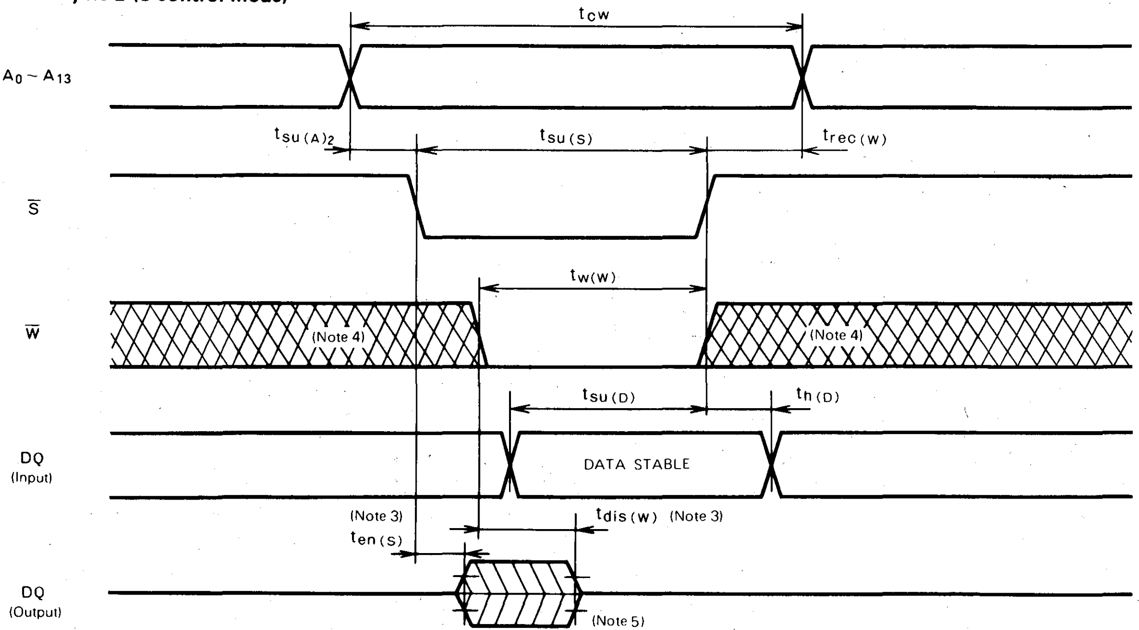
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)



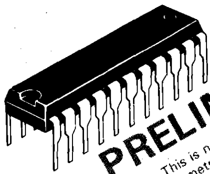
Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

MITSUBISHI ELECTRIC

M5M5188AP-25, -35



65536-BIT (16384-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 16384 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

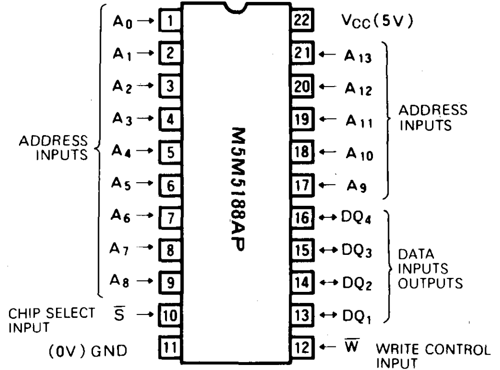
FEATURES

- Fast access time M5M5188AP-25 . . . 25 ns (max)
  M5M5188AP-35 . . . 35 ns (max)
- Low power dissipation Active . . . . 300 mW (typ)
  Standby by . . . . . . 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 22P4H

FUNCTION

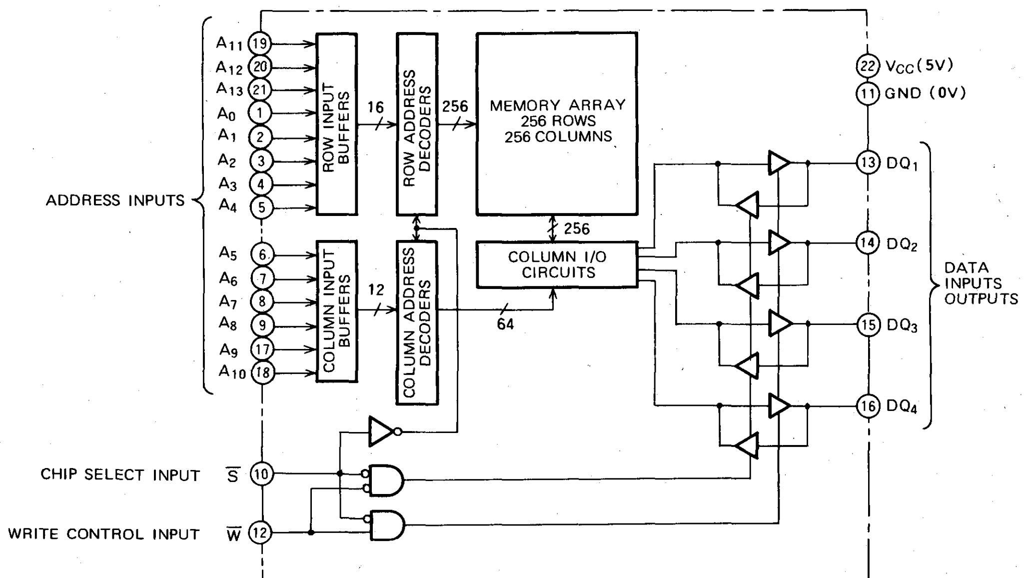
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		−10~85	°C
Tstg	Storage temperature		−65~150	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−3*		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		−3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current	V_I=0 ~ V_{CC}			10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}$=2.2V, V_O=0 ~ V_{CC}			10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}$=0.8V Output open			100	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}$=2.2V Other $V_I \leqq 0.2V$		10	20	mA
I_{CC3}	Standby current	$V_{I(\bar{S})} \geqq V_{CC}-0.2V$, Other $V_I \leqq 0.2V$ or $V_I \geqq V_{CC}-0.2V$		0.001	2	mA
C_I	Input capacitance	V_I=GND, V_i=25mVrms, f=1MHz			5	pF
Co	Output capacitance	V_O=GND, V_o=25mVrms, f=1MHz			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5188AP-25			M5M5188AP-35			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	25			35			ns
$t_{a(A)}$	Address access time			25			35	ns
$t_{a(S)}$	Chip select access time			25			35	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Output enable time after chip selection	5			5			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		15	0		15	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			25			35	ns

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5188AP-25			M5M5188AP-35			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	25			35			ns
$t_{su(S)}$	Chip select setup time	20			30			ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			ns
$t_{w(W)}$	Write pulse width	20			30			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	10			15			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		15	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	20			30			ns

CONDITIONS

Input pulse levels .... 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level .... 0.8V ~ 2V
Output loads .... Fig. 1, Fig. 2

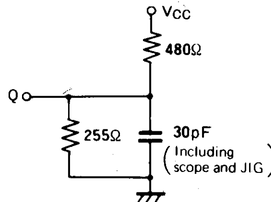


Fig. 1 Output load

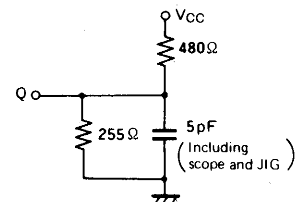
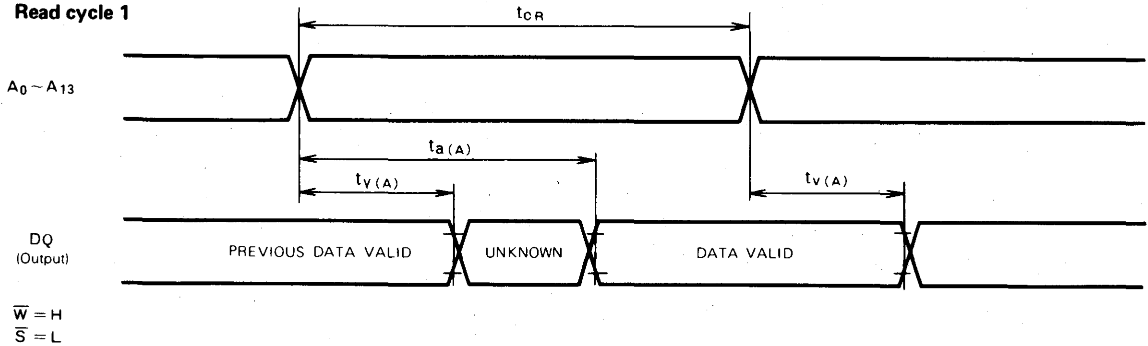


Fig. 2 Output load for ten, tdis

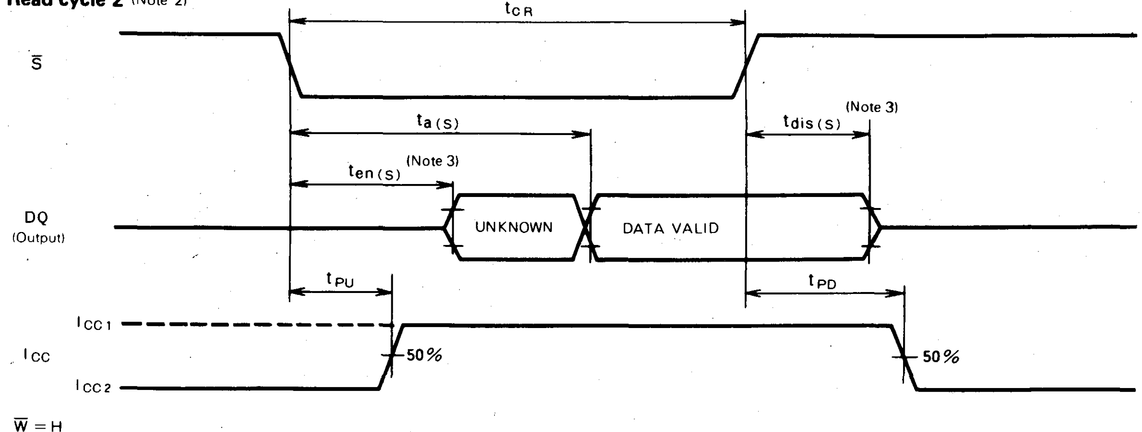
TIMING DIAGRAMS

Read cycle 1



$\overline{W}$ = H
$\overline{S}$ = L

Read cycle 2 (Note 2)

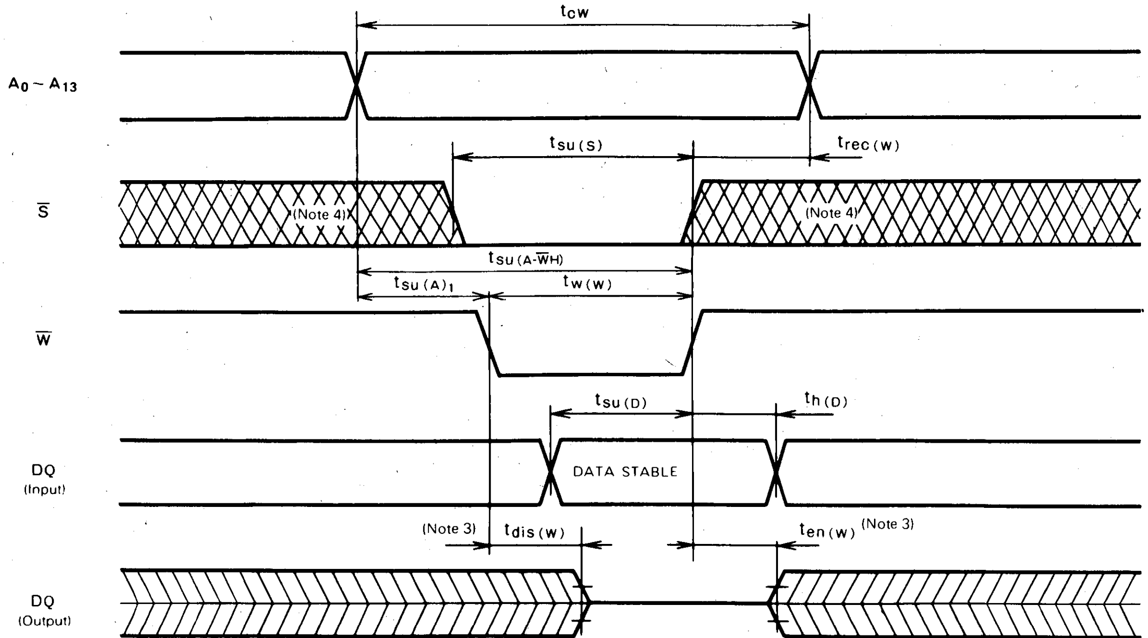


$\overline{W}$ = H

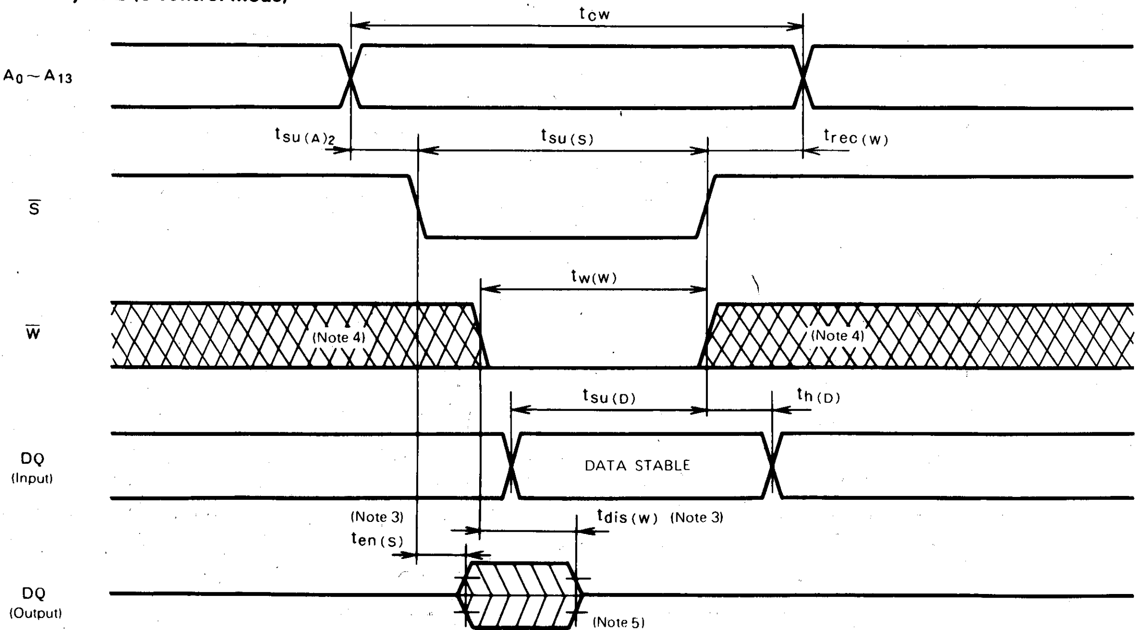
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)



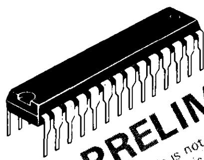
Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.

5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

M5M5178P-35,-45,-55



65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

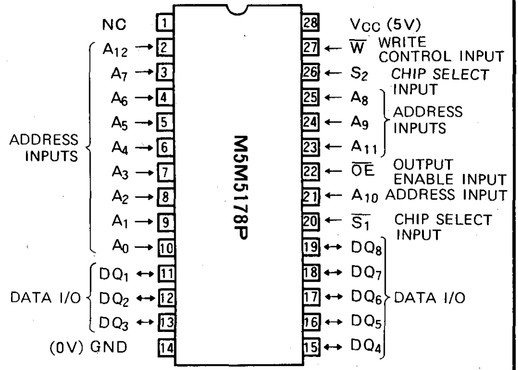
DESCRIPTION

This is a family of 8192 word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time M5M5178P-35 .... 35ns (max.)
  M5M5178P-45 .... 45ns (max.)
  M5M5178P-55 .... 55ns (max.)
- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\overline{S_1}$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O
- 300 mil package

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y

APPLICATION

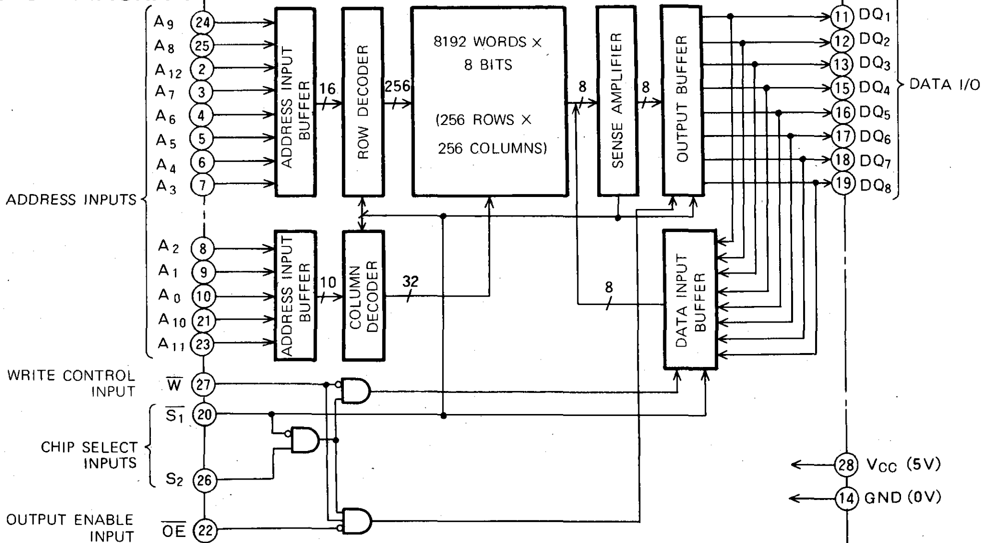
High speed memory system

FUNCTION

The operation mode of the M5M5178P is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3}.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
L	L	X	X	Non selection	high-impedance	Active
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		−10~85	°C
Tstg	Storage temperature		−65~150	°C

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage		I_{OH}=−4mA	2.4			V
V_{OL}	Low output voltage		I_{OL}= 8 mA			0.4	V
I_I	Input current		V_I=0~V_{CC}			±1	μA
I_{OZH}	High level output current in off-state		$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0−V_{CC}			1	μA
I_{OZL}	Low level output current in off-state					−1	μA
I_{CC1}	Active supply current		$\overline{S_1}$=V_{IL} or S_2=V_{IH} Output open Other inputs =V_{IH}			120	mA
I_{CC2}	Stand-by supply current		S_2=V_{IL}, $\overline{S_1}$=V_{IH}, Other inputs=0~V_{CC}			25	mA
I_{CC3}	Stand-by supply current		$\overline{S_1}$≧V_{CC}−0.2V Other inputs ≦0.2V or V_{CC}−0.2V			2	mA
Ci	Output capacitance (Ta=25°C)	$\overline{S_1}$, S_2, $\overline{OE}$, $\overline{W}$	V_I=GND, V_i=25mVrms, f=1MHz			7	pF
		A_0~A_{12}				6	
Co	Outout capacitance (Ta=25°C)		V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5178P-35			M5M5178P-45			M5M5178P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S1)}$	Chip select 1 access time			35			45			55	ns
$t_{a(S2)}$	Chip select 2 access time			15			20			25	ns
$t_{a(OE)}$	Output enable access time			15			20			25	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			20			25			35	ns
$t_{dis(S2)}$	Output disable time after S_2 low			20			25			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			5			5			ns
$t_{en(S2)}$	Output enable time after S_2 high	3			3			3			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns
$t_{v(A)}$	Data valid time after address change	3			3			3			ns

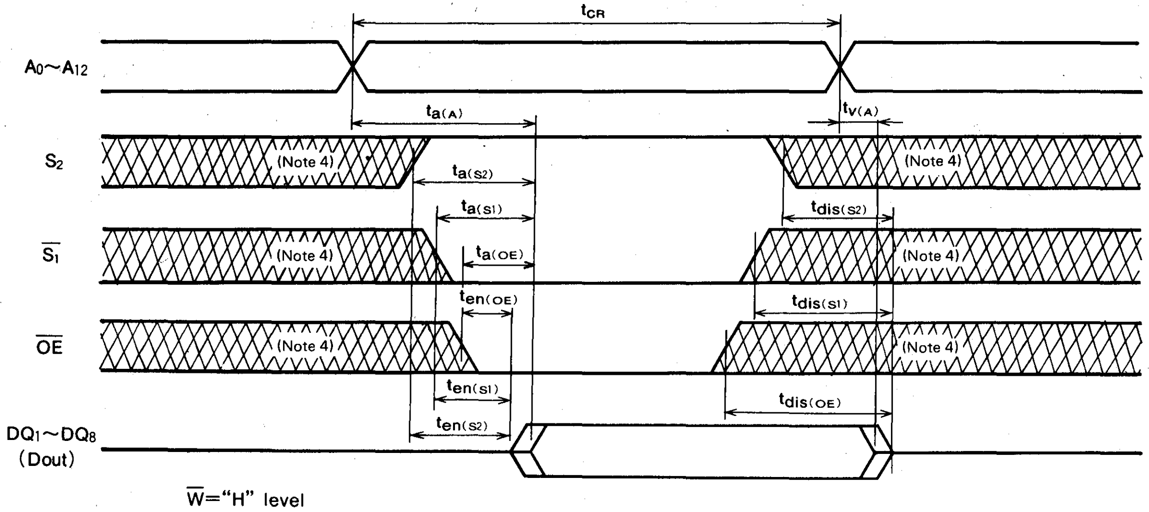
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

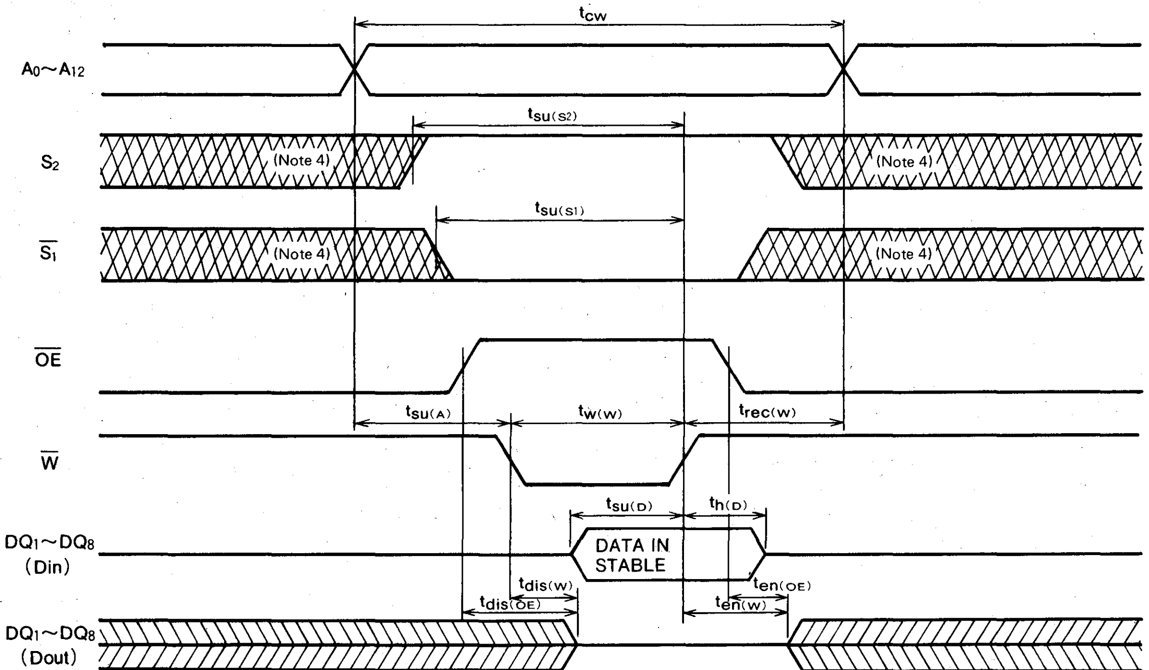
Symbol	Parameter	Limits									Unit
		M5M5178P-35			M5M5178P-45			M5M5178P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	35			45			55			ns
$t_{w(W)}$	Write pulse width	20			25			30			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(S1)}$	Chip select 1 set up time	30			40			45			ns
$t_{su(S2)}$	Chip select 2 set up time	20			25			30			ns
$t_{su(D)}$	Data set up time	17			20			30			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	3			3			3			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			15			20			20	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			0			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns

TIMING DIAGRAM

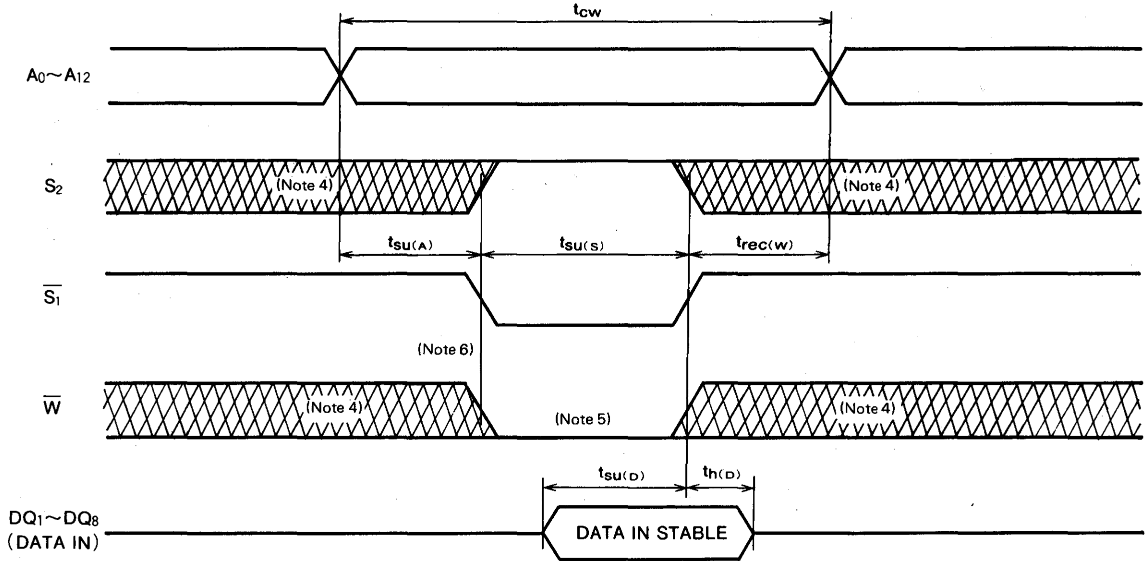
Read cycle



Write cycle (W control)



Write cycle ($\overline{S}$ control)



CONDITIONS

Input pulse levels .... 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level .... 0.8V ~ 2V
Output loads .... Fig. 1, Fig. 2

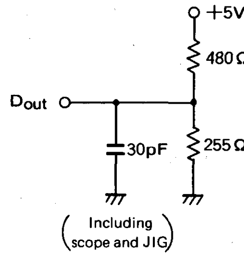


Fig. 1 Output load

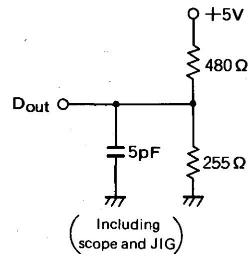
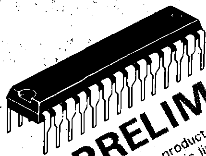


Fig. 2 Output load for t_{en} t_{dis}

Note 4: Hatching indicates the state is don't care.
5: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

M5M5179P-35, -45, -55



73728-BIT (8192-WORD BY 9-BIT) CMOS STATIC RAM

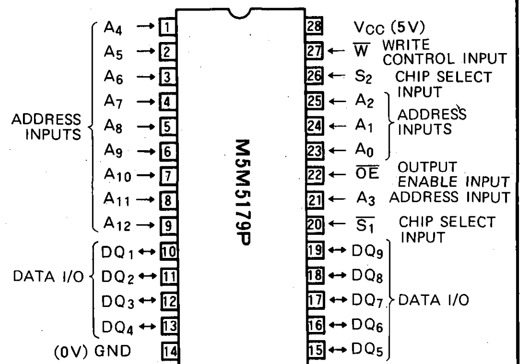
DESCRIPTION

This is a family of 8192 word by 9-bit static RAMs, fabricated with the high performance CMOS silicon gate MOS process and designed for high-speed application. 9 bit organization is useful for parity check system. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time M5M5179P-35 .... 35ns (max.)
  M5M5179P-45 .... 45ns (max.)
  M5M5179P-55 .... 55ns (max.)
- 9 bit organization
- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\overline{S_1}$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O
- 300 mil package

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y

APPLICATION

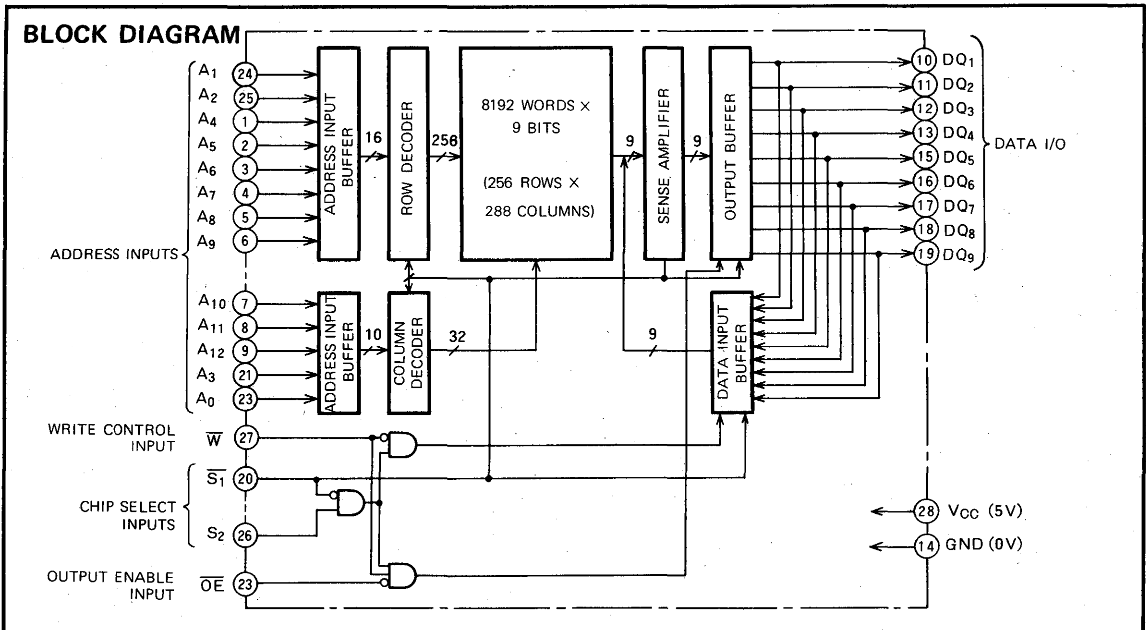
High-Speed memory system

FUNCTION

The operation mode of the M5M5179P is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3}.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
L	L	X	X	Non selection	high-impedance	Active
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	−0.3		0.8	V
V_{IH}	High input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
Pd	Power dissipation	Ta = 25°C	1000	mW
Topr	Operating temperature		−10 ~ 85	°C
Tstg	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage		I_{OH} = −4mA	2.4			V
V_{OL}	Low output voltage		I_{OL} = 8 mA			0.4	V
I_I	Input current		V_I = 0 ~ V_{CC}			±1	μA
I_{OZH}	High level output current in off-state		$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 − V_{CC}			1	μA
I_{OZL}	Low level output current in off-state					−1	μA
I_{CC1}	Active supply current		$\overline{S_1}$ = V_{IL} Output open Other inputs = V_{IH}			120	mA
I_{CC2}	Stand-by supply current		S_2 = V_{IL}, $\overline{S_1}$ = V_{IH}, Other inputs = 0 ~ V_{CC}			25	mA
I_{CC3}	Stand-by supply current		$\overline{S_1}$ ≧ V_{CC} − 0.2V Other inputs ≦ 0.2V or V_{CC} − 0.2V			2	mA
C_i	Output capacitance (Ta=25°C)	$\overline{S_1}$, S_2, $\overline{OE}$, $\overline{W}$	V_I = GND, V_i = 25mVmrs, f = 1MHz			7	pF
		A_0 ~ A_{12}				6	
C_o	Outout capacitance (Ta=25°C)		V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC} = 5V, Ta = 25°C

73728-BIT (8192-WORD BY 9-BIT) CMOS STATIC RAM

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5179P-35			M5M5179P-45			M5M5179P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S1)}$	Chip select 1 access time			35			45			55	ns
$t_{a(S2)}$	Chip select 2 access time			15			20			25	ns
$t_{a(OE)}$	Output enable access time			15			20			25	ns
$t_{dis(S1)}$	Output disable time after $\overline{S}_1$ high			20			25			35	ns
$t_{dis(S2)}$	Output disable time after S_2 low			20			25			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			35	ns
$t_{en(S1)}$	Output enable time after $\overline{S}_1$ low	5			5			5			ns
$t_{en(S2)}$	Output enable time after S_2 high	3			3			3			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns
$t_{v(A)}$	Data valid time after address change	3			3			3			ns

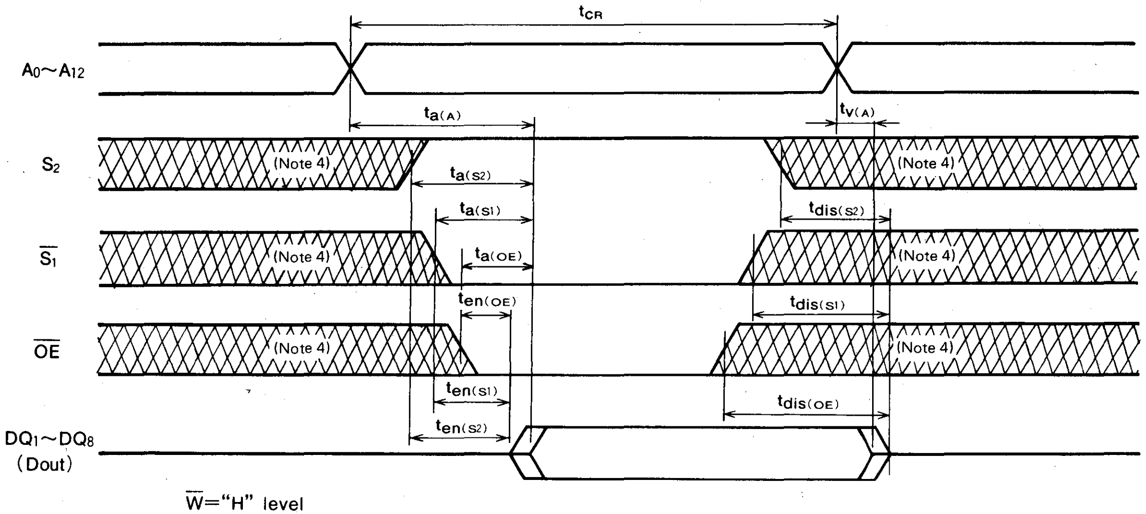
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

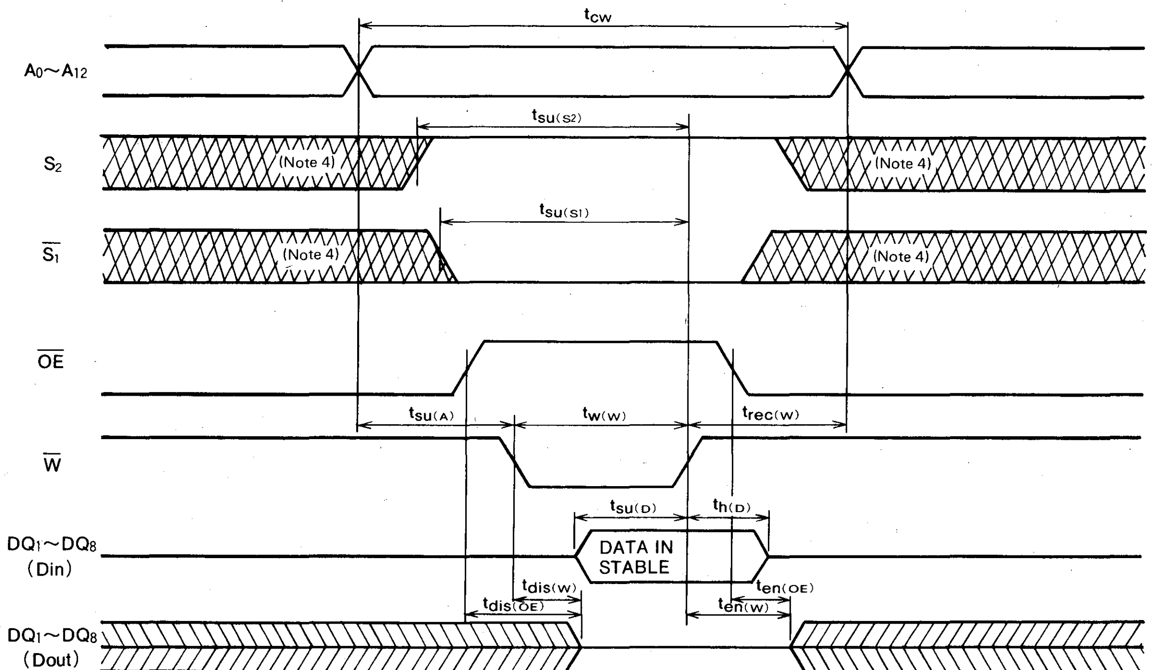
Symbol	Parameter	Limits									Unit
		M5M5179P-35			M5M5179P-45			M5M5179P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	35			45			55			ns
$t_{w(W)}$	Write pulse width	20			25			30			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(S1)}$	Chip select 1 set up time	30			40			45			ns
$t_{su(S2)}$	Chip select 2 set up time	20			25			30			ns
$t_{su(D)}$	Data set up time	17			20			30			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	3			3			3			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			15			20			20	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			0			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns

TIMING DIAGRAM

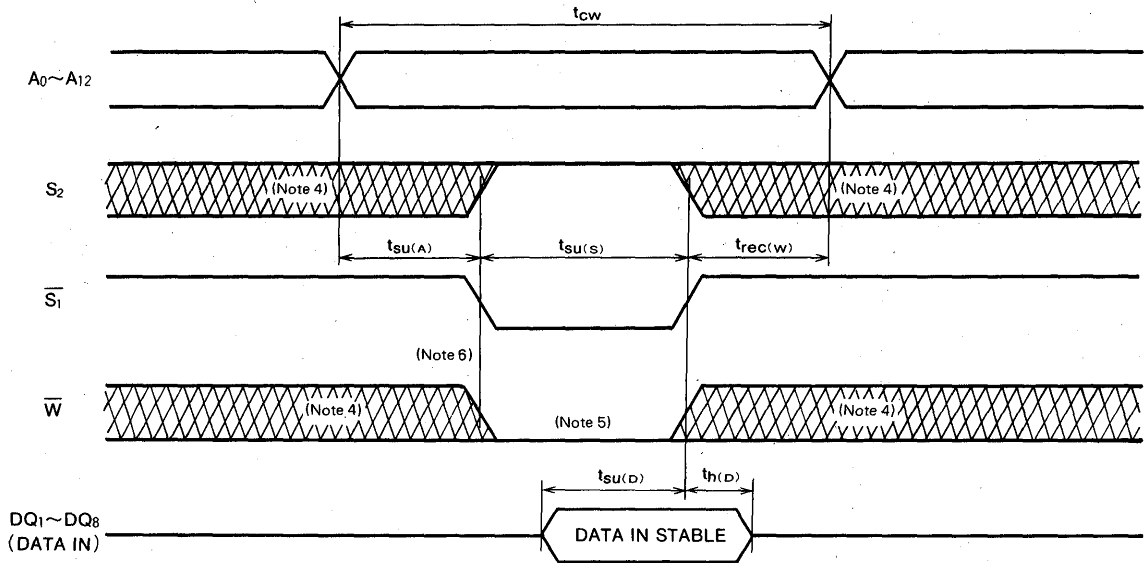
Read cycle



Write cycle (W control)



Write cycle ($\overline{S}$ control)



CONDITIONS

Input pulse levels . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . 0.8V ~ 2V
Output loads . . . . Fig. 1, Fig. 2

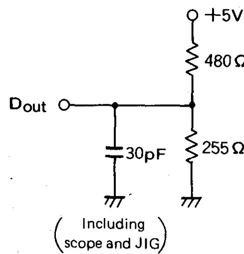


Fig. 1 Output load

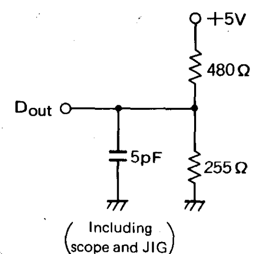
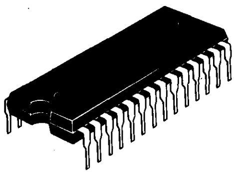


Fig. 2 Output load for t_{en} t_{dis}

Note 4: Hatching indicates the state is don't care.
5: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.



M5M5256P-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256P is a 262,144-bit CMOS static RAM organized as 32,768 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256P-10	100ns	70 mA	2mA
M5M5256P-12	120ns		
M5M5256P-15	150ns		
M5M5256P-10L	100ns		100 μA
M5M5256P-12L	120ns		
M5M5256P-15L	150ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O

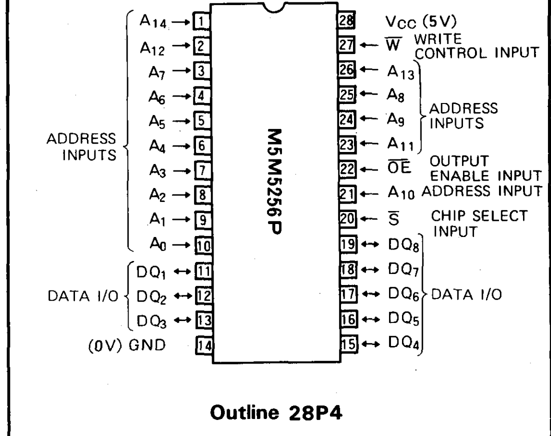
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the M5M5256P is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$.

PIN CONFIGURATION (TOP VIEW)



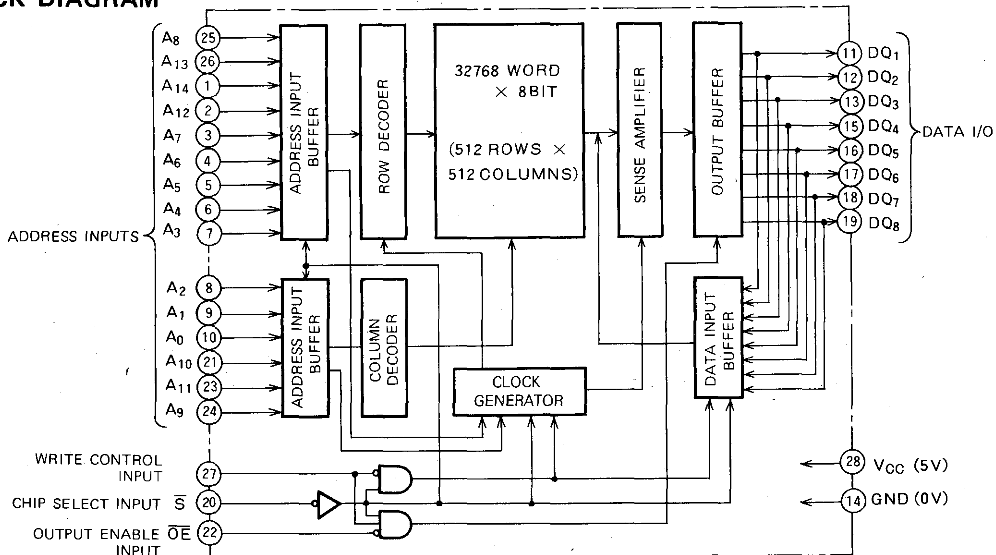
Outline 28P4

Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

BLOCK DIAGRAM



When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC5} or I_{CC6}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
Pd	Power dissipation	Ta = 25°C	700	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = −1mA	2.4			V
V_{OL}	Low output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current	V_I = 0 ~ V_{CC}			±1	μA
I_{OZH}	High level output current in off-state	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 − V_{CC}			1	μA
I_{OZL}	Low level output current in off-state				−1	μA
I_{CC1}	Active supply current (DC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.3 output open other input < 0.2 or > V_{CC} − 0.3 tcycle = 1μs		15	25	mA
I_{CC2}	Active supply current (AC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.3 output open other input < 0.2 or > V_{CC} − 0.3 Min cycle		30	65	mA
I_{CC3}	Active supply current (DC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open other input = V_{IL} or V_{IH} tcycle = 1μs		20	30	mA
I_{CC4}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open other input = V_{IL} or V_{IH} Min cycle		35	70	mA
I_{CC5}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V Other inputs = 0 ~ V_{CC}			2(P)	mA
					100(P-L)	μA
I_{CC6}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0 ~ V_{CC}			3	mA
C_i	Input capacitance (T_a=25°C)	V_I = GND, V_i = 25mVrms, f = 1MHz			6	pF
C_o	Outout capacitance (T_a=25°C)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256P-10 M5M5256P-10L			M5M5256P-12 M5M5256P-12L			M5M5256P-15 M5M5256P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	100			120			150			ns
$t_{a(A)}$	Address access time			100			120			150	ns
$t_{a(S)}$	Chip select access time			100			120			150	ns
$t_{a(OE)}$	Output enable access time			50			60			75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40			45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			ns

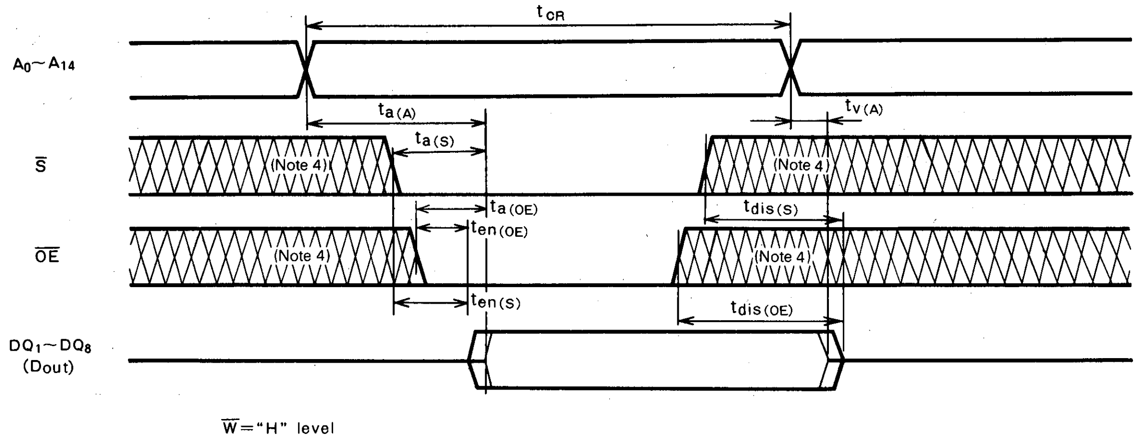
TIMING REQUIREMENTS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Write cycle

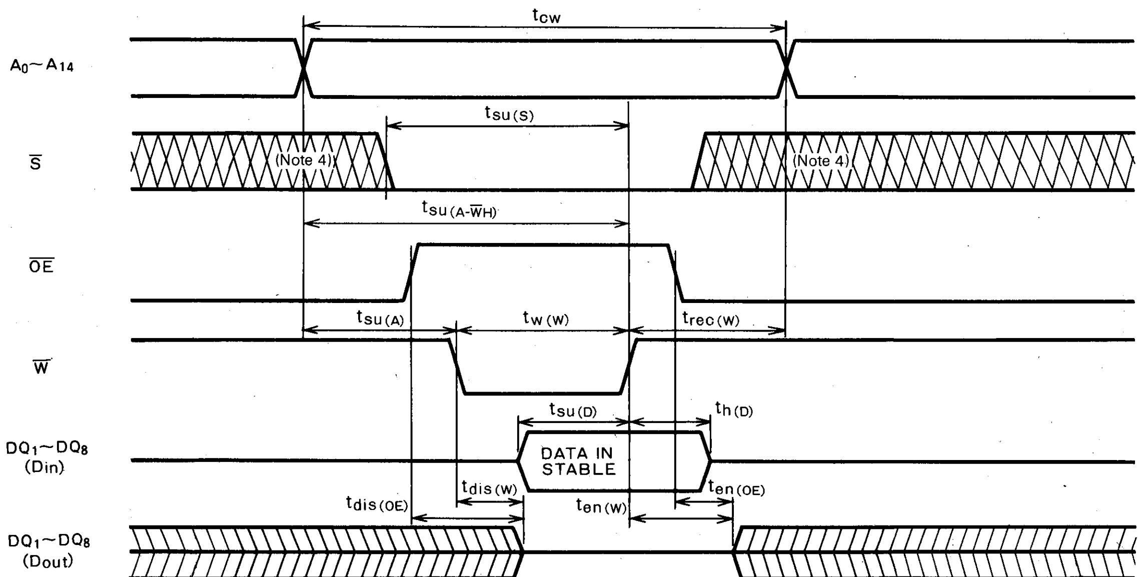
Symbol	Parameter	Limits									Unit
		M5M5256P-10 M5M5256P-10L			M5M5256P-12 M5M5256P-12L			M5M5256P-15 M5M5256P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	100			120			150			ns
$t_{w(W)}$	Write pulse width	60			70			80			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(A\text{-}\overline{W}H)}$	Address set up time with respeet to $\overline{W}$ high	80			85			90			ns
$t_{su(S)}$	Chip select set up time	80			85			90			ns
$t_{su(D)}$	Data set up time	35			40			50			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40			45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			ns

TIMING DIAGRAM

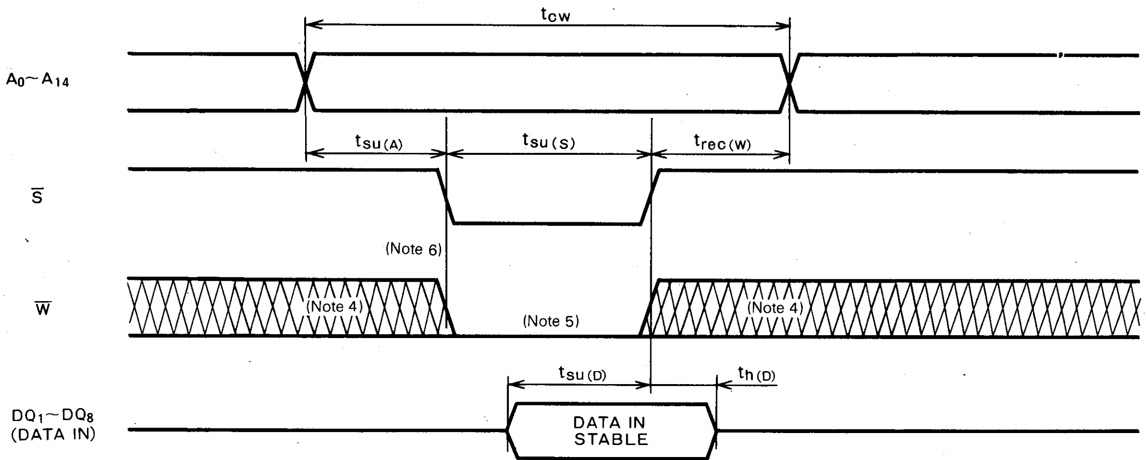
Read cycle



Write cycle (WE control)



Write cycle ($\overline{S}$ control)



Note 3: Test condition
Input pulse level: 0.6~2.4V
Input pulse rise, fall time: 10ns
Load: 1 TTL, C_L = 100pF
Conditions of assessment: 1.5V

4: Hatching indicates the state is don't care.

5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.

6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.

7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

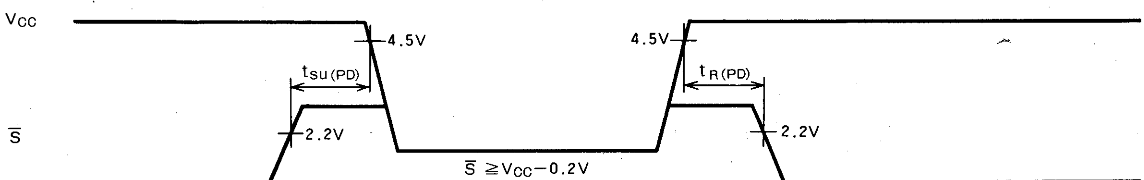
ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

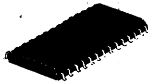
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	$2.2V \leqq V_{CC(PD)}$	2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs =3V			2(P)	mA
					50(P-L)	μA

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS





M5M5256FP-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256FP is a 262,144-bit CMOS static RAM organized as 32,768 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a 28 pin flat package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256FP-10	100ns	70 mA	2mA
M5M5256FP-12	120ns		
M5M5256FP-15	150ns		
M5M5256FP-10L	100ns		100 μA
M5M5256FP-12L	120ns		
M5M5256FP-15L	150ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O

APPLICATION

Small Capacity Memory Units.

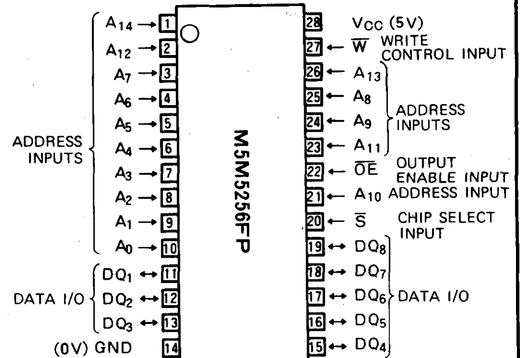
FUNCTION

The operation mode of the M5M5256FP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

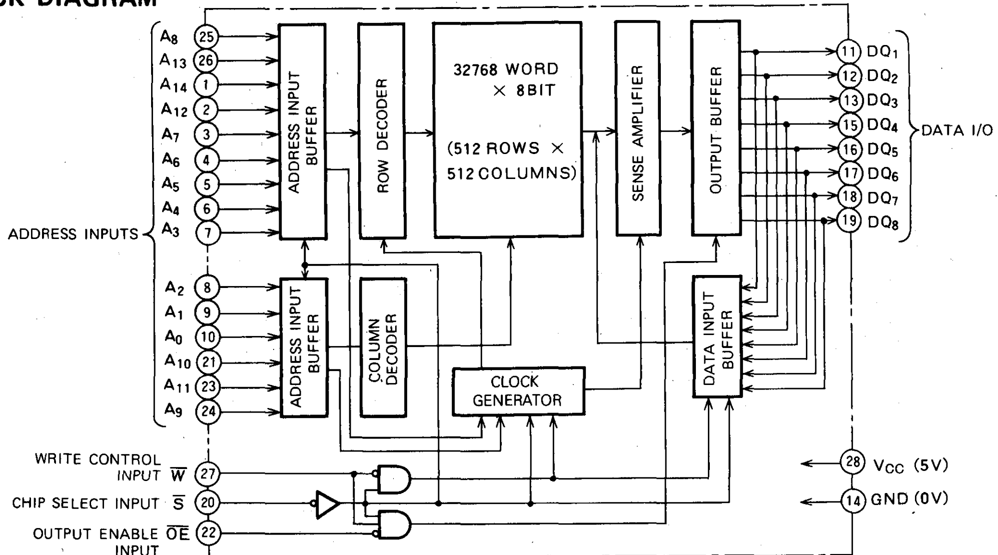
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

PIN CONFIGURATION (TOP VIEW)



Outline 28P2W

BLOCK DIAGRAM



262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC5} or I_{CC6}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA	2.4			V
V_{OL}	Low output voltage	I_{OL}=2 mA			0.4	V
I_I	Input current	V_I=0~V_{CC}			±1	μA
I_{OZH}	High level output current in off-state	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=0−V_{CC}			1	μA
I_{OZL}	Low level output current in off-state				−1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$<0.2, $\overline{W}$>V_{CC}−0.3 output open other input<0.2 or >V_{CC}−0.3 tcycle=1μs		3	10	mA
I_{CC2}	Active supply current (AC, MOS level)	$\overline{S}$<0.2, $\overline{W}$>V_{CC}−0.3 output open other input<0.2 or >V_{CC}−0.3 Min. cycle		30	65	mA
I_{CC3}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} output open other input=V_{IL} or V_{IH} tcycle=1μs		7	15	mA
I_{CC4}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} output open other input=V_{IL} or V_{IH} Min. cycle		35	70	mA
I_{CC5}	Stand-by supply current	$\overline{S}$≧V_{CC}−0.2V Other inputs =0~V_{CC}			2(P)	mA
					100(P−L)	μA
I_{CC6}	Stand-by supply current	$\overline{S}$=V_{IH}, Other inputs=0~V_{CC}			3	mA
C_i	Input capacitance (Ta=25°C)	V_I=GND, V_i=25mVrms, f=1MHz			6	pF
C_o	Outout capacitance (Ta=25°C)	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256FP-10 M5M5256FP-10L			M5M5256FP-12 M5M5256FP-12L			M5M5256FP-15 M5M5256FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	100			120			150			ns
$t_{a(A)}$	Address access time			100			120			150	ns
$t_{a(S)}$	Chip select access time			100			120			150	ns
$t_{a(OE)}$	Output enable access time			50			60			75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40			45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			ns
$t_{V(A)}$	Data valid time after address change	20			20			20			ns

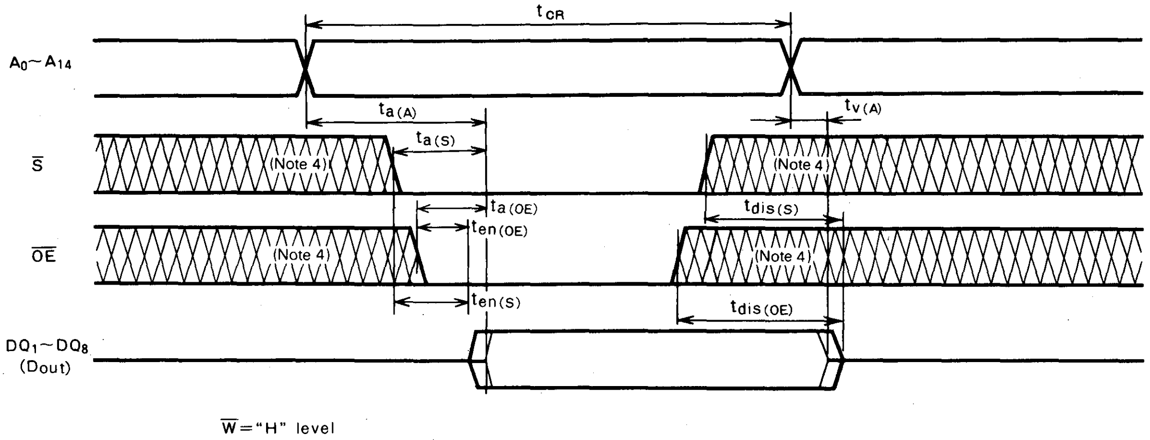
TIMING REQUIREMENTS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Write cycle

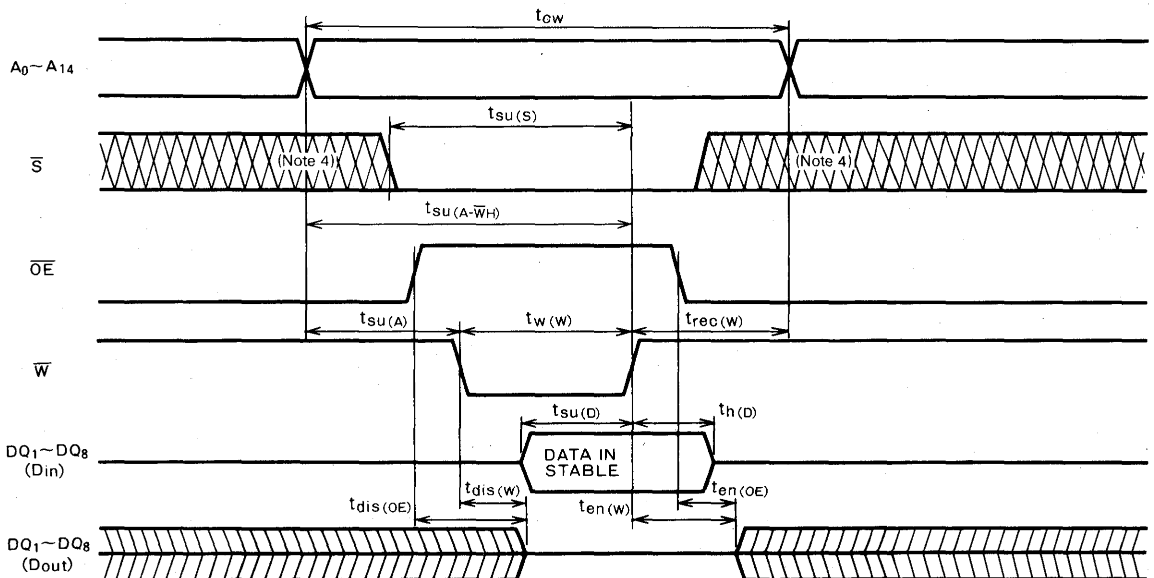
Symbol	Parameter	Limits									Unit
		M5M5256FP-10 M5M5256FP-10L			M5M5256FP-12 M5M5256FP-12L			M5M5256FP-15 M5M5256FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	100			120			150			ns
$t_{W(W)}$	Write pulse width	60			70			80			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address set up time with respeet to $\overline{W}$ high	80			85			90			ns
$t_{su(S)}$	Chip select set up time	80			85			90			ns
$t_{su(D)}$	Data set up time	35			40			50			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40			45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			ns

TIMING DIAGRAM

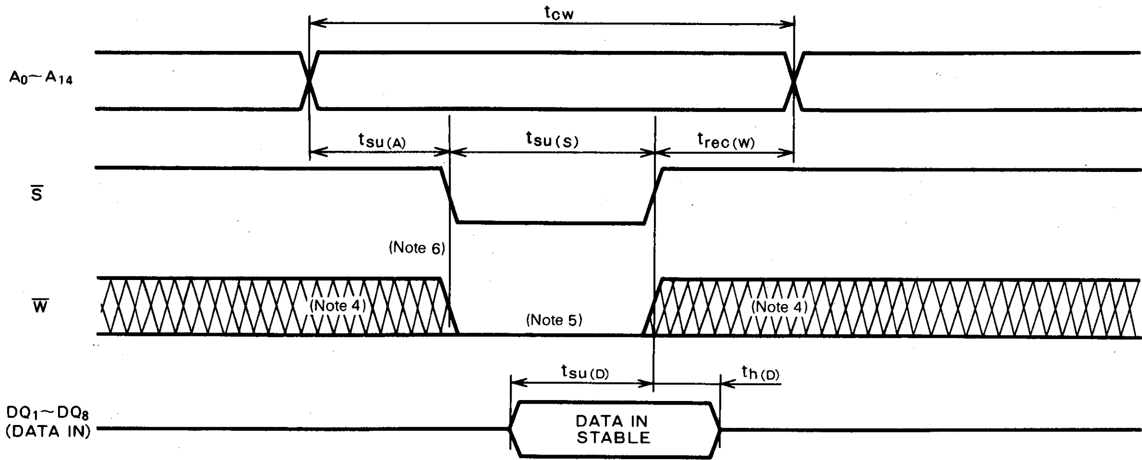
Read cycle



Write cycle (WE control)



Write cycle ($\overline{S}$ control)



Note 3: Test condition
Input pulse level: 0.6~2.4V
Input pulse rise, fall time: 10ns
Load: 1 TTL, C_L = 100pF
Conditions of assessment: 1.5V
4: Hatching indicates the state is don't care.
5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

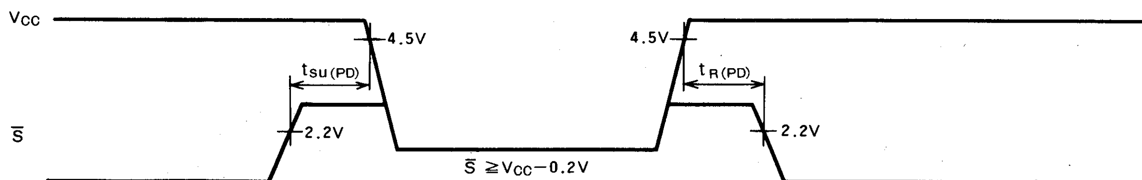
ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

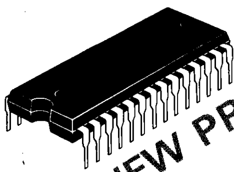
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	$2.2V \leq V_{CC(PD)}$	2.2			V
		$2V \leq V_{CC(PD)} \leq 2.2V$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs =3V			2(P)	mA
					50(P-L)	μA

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS





M5M5256AP-70, -85, -10, -70L, -85L, -10L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256AP is a 262,144-bit CMOS static RAM organized as 32,768 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current: Active (max)	Power supply current: Stand-by (max)
M5M5256AP-70	70ns	70 mA	2mA
M5M5256AP-85	85ns		
M5M5256AP-10	100ns		
M5M5256AP-70L	70ns		100 μA
M5M5256AP-85L	85ns		
M5M5256AP-10L	100ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O

APPLICATION

Small Capacity Memory Units.

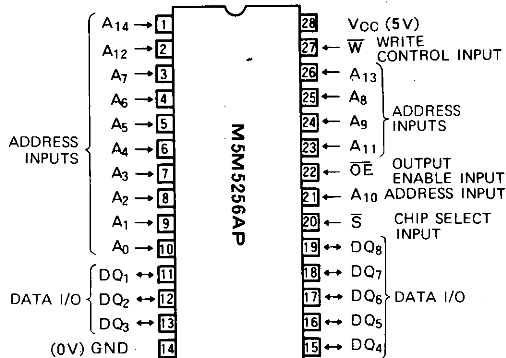
FUNCTION

The operation mode of the M5M5256AP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

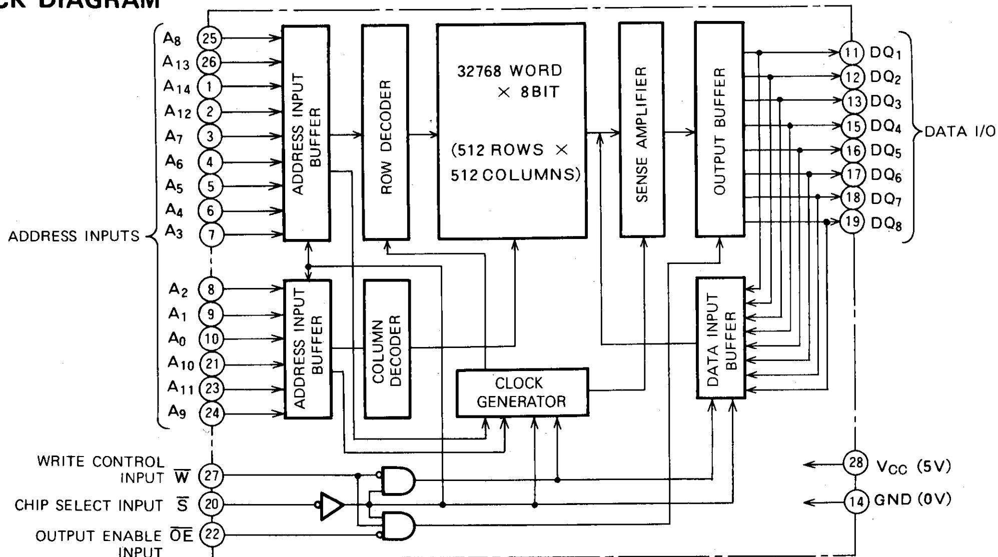
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC5} or I_{CC6}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
Pd	Power dissipation	Ta = 25°C	700	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = −1mA	2.4			V
V_{OL}	Low output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current	V_I = 0 ~ V_{CC}			±1	μA
I_{OZH}	High level output current in off-state	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 − V_{CC}			1	μA
I_{OZL}	Low level output current in off-state				−1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.3, output open other input < 0.2 or > V_{CC} − 0.3 tcycle = 1 μs		3	10	mA
I_{CC2}	Active supply current (AC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.2, output open other input < 0.2 or > V_{CC} − 0.3 Min. cycle		30	65	mA
I_{CC3}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH}, output open other input = V_{IL} or V_{IH} tcycle = 1 μs		7	15	mA
I_{CC4}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open other input = V_{IL} or V_{IH} Min. cycle		35	70	mA
I_{CC5}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V Other inputs = 0 ~ V_{CC}			2(P)	mA
					100(P-L)	μA
I_{CC6}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0 ~ V_{CC}			3	mA
C_i	Input capacitance (Ta=25°C)	V_I = GND, V_i = 25mVrms, f = 1MHz			6	pF
C_o	Outout capacitance (Ta=25°C)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256AP-70 M5M5256AP-70L			M5M5256AP-85 M5M5256AP-85L			M5M5256AP-10 M5M5256AP-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			85			100			ns
$t_{a(A)}$	Address access time			70			85			100	ns
$t_{a(S)}$	Chip select access time			70			86			100	ns
$t_{a(OE)}$	Output enable access time			35			45			50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			30			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			30			35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5			5			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			ns
$t_{V(A)}$	Data valid time after address change	20			20			20			ns

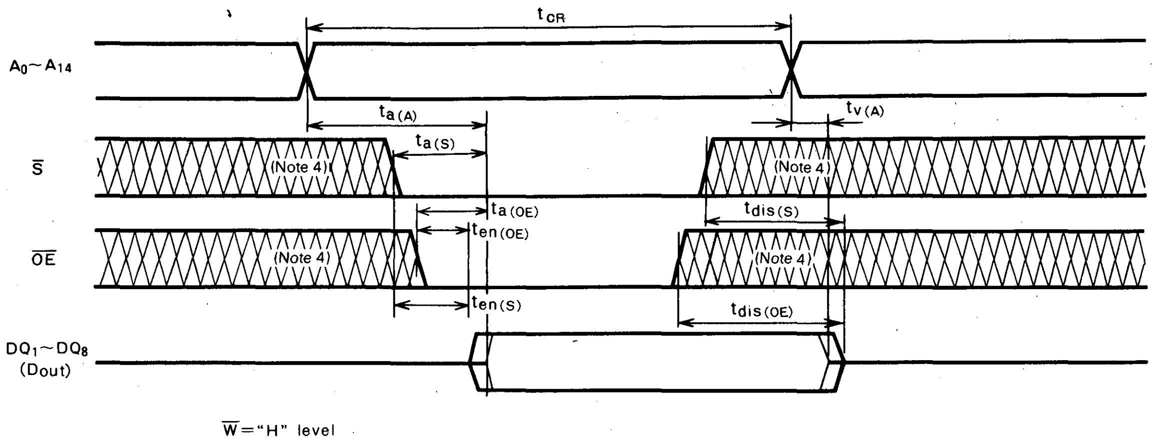
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Write cycle

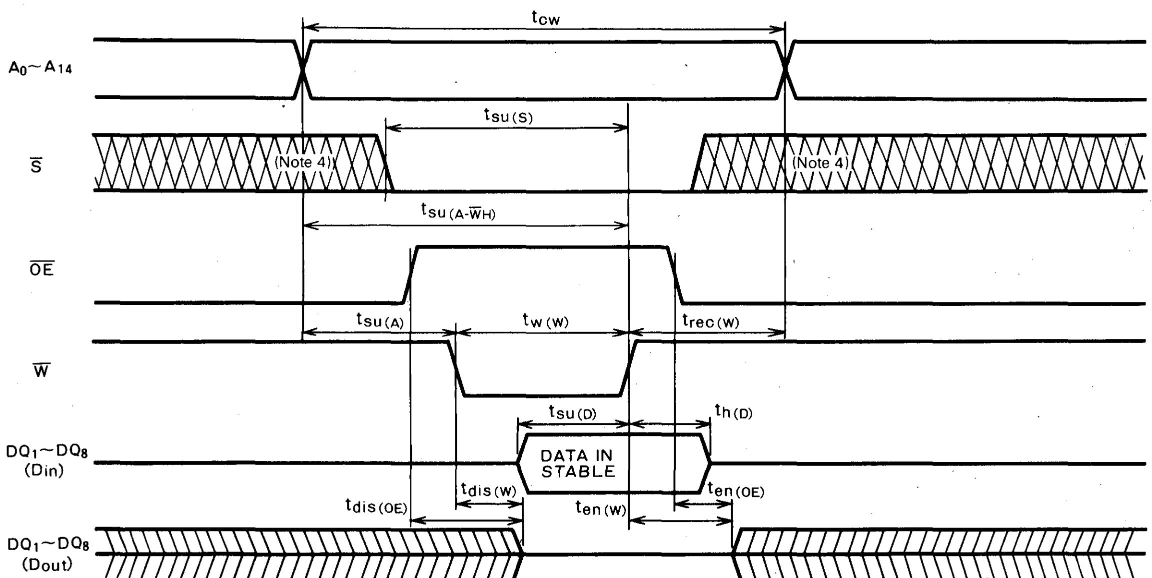
Symbol	Parameter	Limits									Unit
		M5M5256AP-70 M5M5256AP-70L			M5M5256AP-85 M5M5256AP-85L			M5M5256AP-10 M5M5256AP-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			ns
$t_{W(W)}$	Write pulse width	55			60			60			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address set up time with respeet to $\overline{W}$ high	65			75			80			ns
$t_{su(S)}$	Chip select set up time	65			75			80			ns
$t_{su(D)}$	Data set up time	30			35			35			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			ns

TIMING DIAGRAM

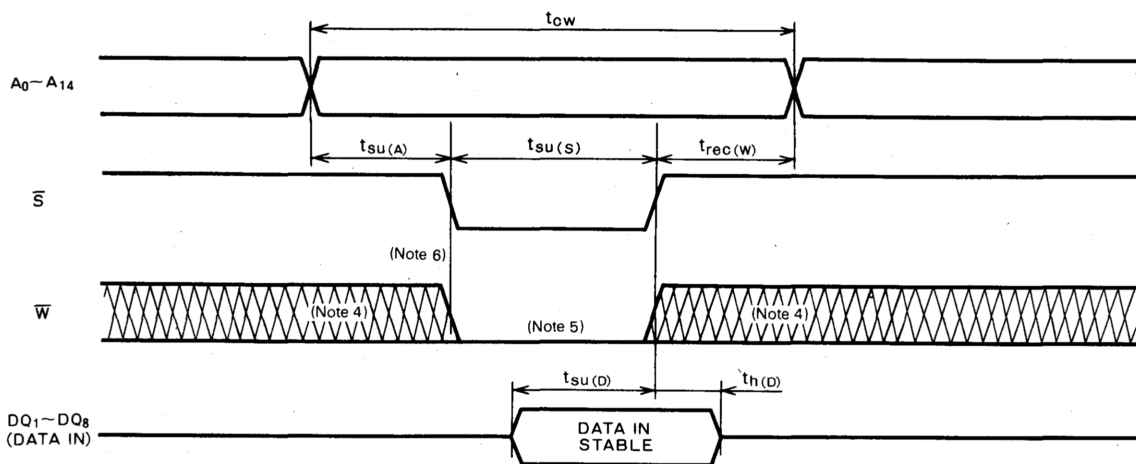
Read cycle



Write cycle (WE control)



Write cycle ($\overline{S}$ control)



Note 3: Test condition
Input pulse level: 0.6~2.4V
Input pulse rise, fall time: 10ns
Load: 1 TTL, C_L =30pF for—70, 100pF for—85, —10
Conditions of assessment: 1.5V
4: Hatching indicates the state is don't care.
5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

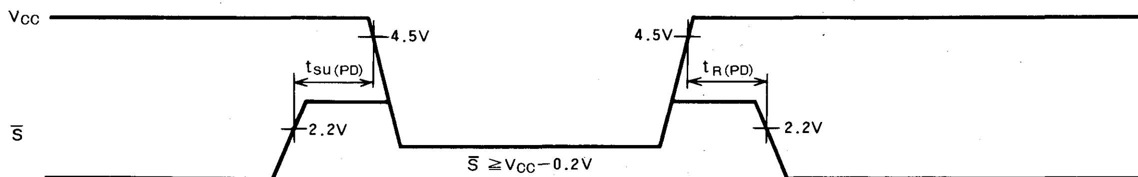
ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	$2.2V \leqq V_{CC(PD)}$	2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs =3V			2(P)	mA
					50(P-L)	μA

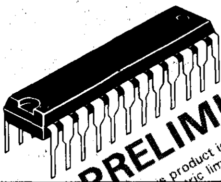
TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su\ (PD)}$	Power down setup time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS



M5M5257P-35, -45, -55



262144-BIT(262144-WORD BY 1-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M5257P is a family of 262144-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5257P-35 . . . 35 ns (max)
  M5M5257P-45 . . . 45 ns (max)
  M5M5257P-55 . . . 55 ns (max)
- Low power dissipation Active . . . . 300 mW (typ)
  Stand by . . . . 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

FUNCTION

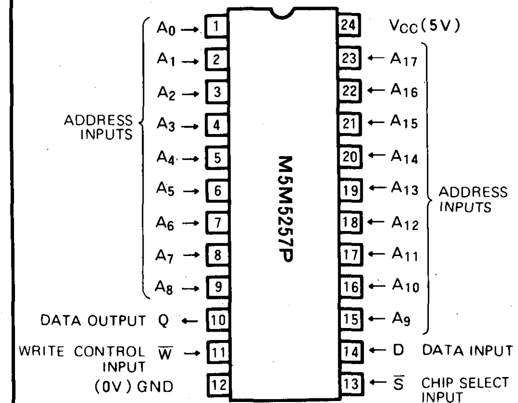
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

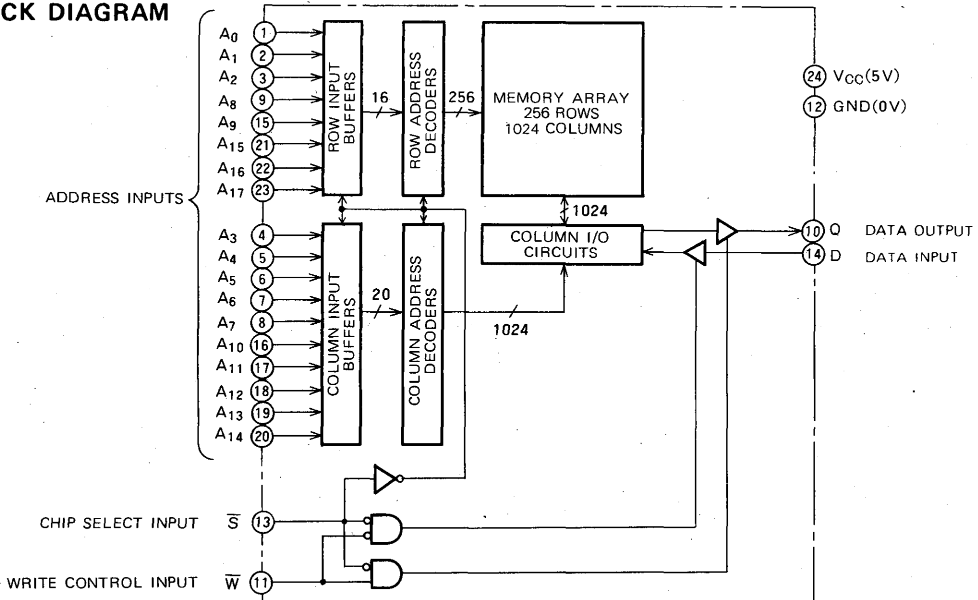
Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y

BLOCK DIAGRAM



262144-BIT(262144-WORD BY 1-BIT)CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		−10~85	°C
T_{stg}	Storage temperature		−65~150	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−3*		0.8	V
V_{IH}	High-level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		−3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current	V_I = 0 ~ 5.5V			10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}$ = 2.2V, V_O = 0 ~ V_{CC}			50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}$ = 0.8V Output open			120	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}$ = 2.2V			3	mA
I_{CC3}	Standby current	$V_{I(\bar{S})} \geqq V_{CC} - 0.2V$		0.1	2	mA
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz			5	pF
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5257P-35			M5M5257P-45			M5M5257P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(R)}$	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S)}$	Chip select access time			35			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			5			ns
$t_{en(S)}$	Chip selection to output active	5			5			5			ns
$t_{dis(S)}$	Output disable time from CS	0		20	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power down time after chip deselection			35			45			55	ns

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5257P-35			M5M5257P-45			M5M5257P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(W)}$	Write cycle time	35			45			55			ns
$t_{su(S)}$	Chip select setup time	30			35			40			ns
$t_{su(A)1}$	Address setup time (W)	0			0			0			ns
$t_{su(A)2}$	Address setup time (S)	0			0			0			ns
$t_{w(W)}$	Write pulse width	25			25			30			ns
$t_{rec(W)}$	Write recovery time	5			5			5			ns
$t_{su(D)}$	Data setup time	20			25			25			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time from W			15			15			20	ns
$t_{en(W)}$	Output enable time from W	0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	30			35			40			ns

CONDITIONS

Input pulse levels .... 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level .... 0.8V ~ 2V
Output loads .... Fig. 1, Fig. 2

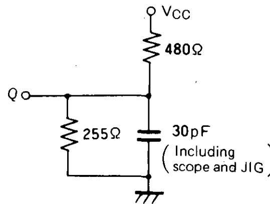


Fig. 1 Output load

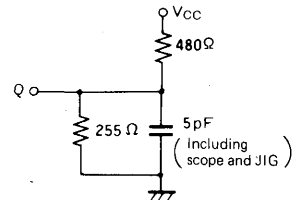
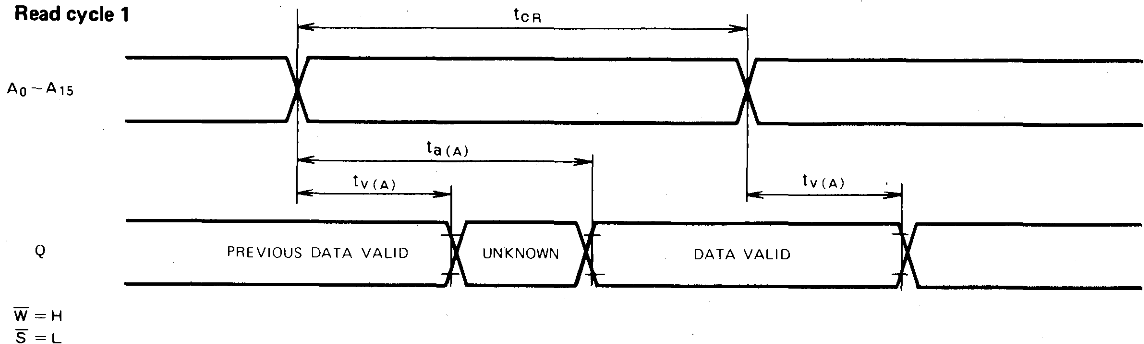


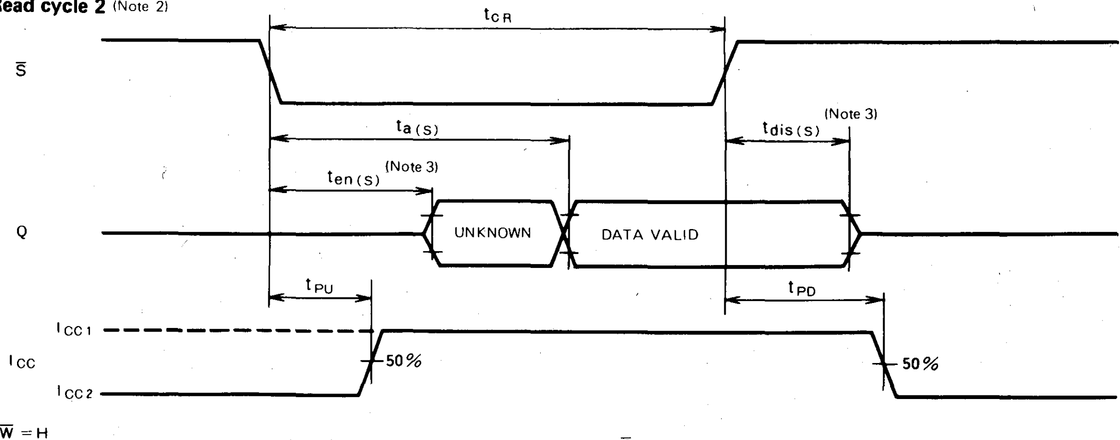
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



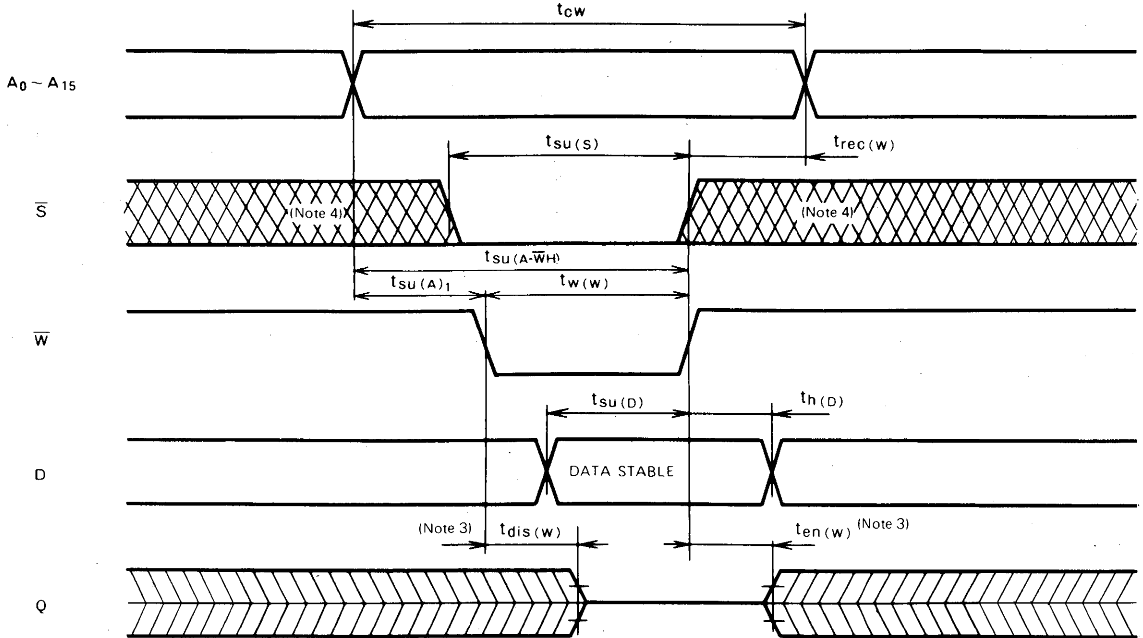
Read cycle 2 (Note 2)



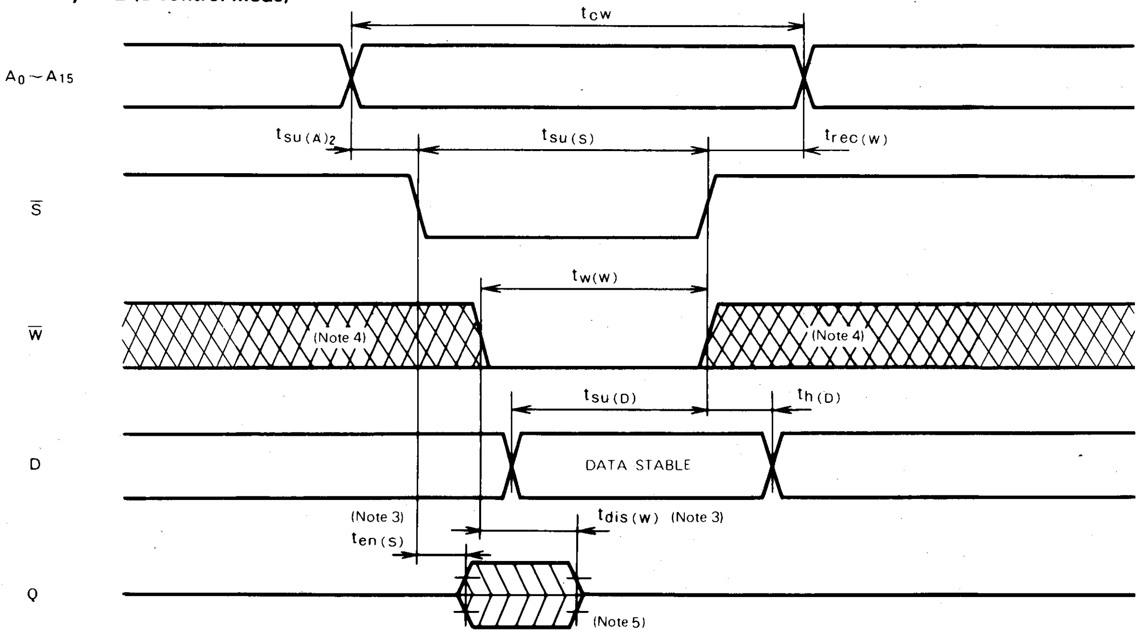
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

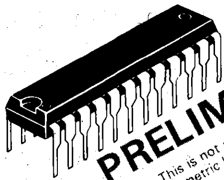
Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.



M5M5258P-35, -45, -55

262144-BIT(65536-WORD BY 4-BIT)CMOS STATIC RAM

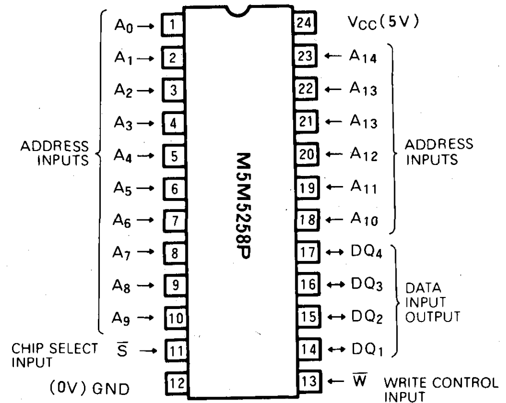
DESCRIPTION

The M5M5258P is a family of 65536 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5258P-35 . . . 35 ns (max)
  M5M5258P-45 . . . 45 ns (max)
  M5M5258P-55 . . . 55 ns (max)
- Low power dissipation Active . . . . 300 mW (typ)
  Standby by . . . . . . 5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y

APPLICATION

High-speed memory systems

FUNCTION

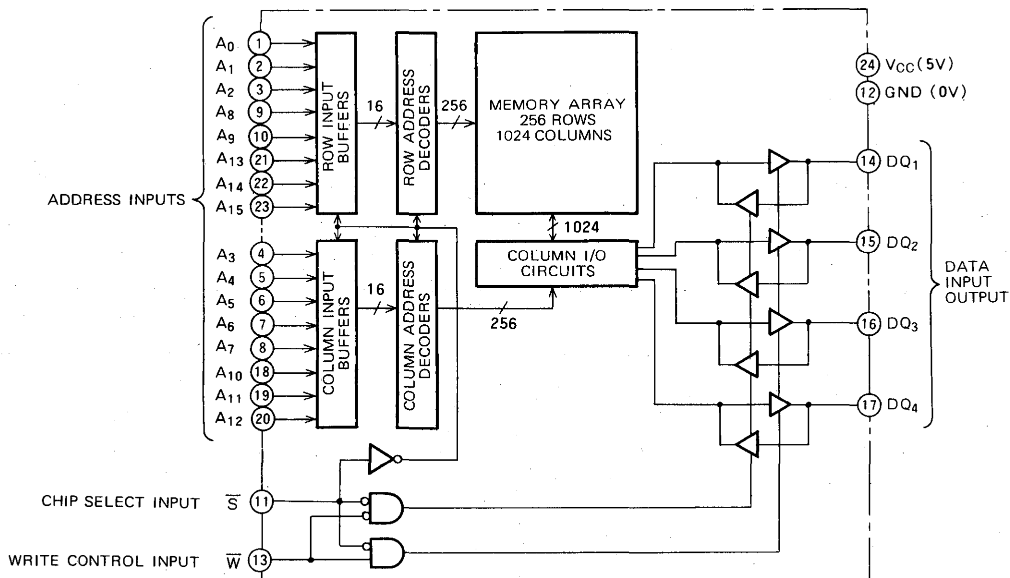
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



262144-BIT(65536-WORD BY 4-BIT)CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		−10~85	°C
Tstg	Storage temperature		−65~150	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−3*		0.8	V
V_{IH}	High level input voltage	2.2		6	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, VCC=5V ±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		6	V
V_{IL}	Low-level input voltage		−3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current	V_I=0 ~ 5.5V			10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\bar{S})}$=2.2V, V_O=0 ~ V_{CC}			50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\bar{S})}$=0.8V Output open			120	mA
I_{CC2}	Stand by current	$V_{I(\bar{S})}$=2.2V			3	mA
I_{CC3}	Stand by current	$V_{I(\bar{S})} \geqq V_{CC}-0.2V$		0.1	2	mA
C_I	Input capacitance	V_I=GND, V_i=25mVrms, f=1MHz			5	pF
Co	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (Ta = 0 ~ 70°C, VCC=5V ±10%, unless otherwise noted)

Symbol	Parameter	M5M5258P-35			M5M5258P-45			M5M5258P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(R)}$	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S)}$	Chip select access time			35			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			5			ns
$t_{en(S)}$	Chip selection to output active	5			5			5			ns
$t_{dis(S)}$	Output disable time from CS	0		20	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power down time after chip deselection			35			45			55	ns

262144-BIT(65536-WORD BY 4-BIT)CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M5258P-35			M5M5258P-45			M5M5258P-55			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(W)}$	Write cycle time	35			45			55			ns
$t_{su(S)}$	Chip select setup time	30			35			40			ns
$t_{su(A)1}$	Address setup time (W)	0			0			0			ns
$t_{su(A)2}$	Address setup time (S)	0			0			0			ns
$t_{w(W)}$	Write pulse width	30			35			40			ns
$t_{rec(W)}$	Write recovery time	5			5			5			ns
$t_{su(D)}$	Data setup time	15			20			20			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time from W			15			15			20	ns
$t_{en(W)}$	Output enable time from W	0			0			0			ns
$t_{su(A-\overline{WH})}$	Address to $\overline{W}$ high	30			35			40			ns

CONDITIONS

Input pulse levels .... 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level .... 0.8V ~ 2V
Output loads .... Fig. 1, Fig. 2

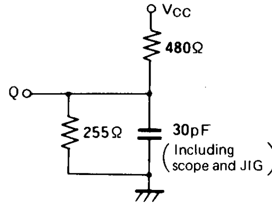


Fig. 1 Output load

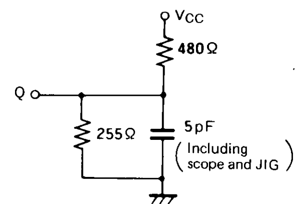
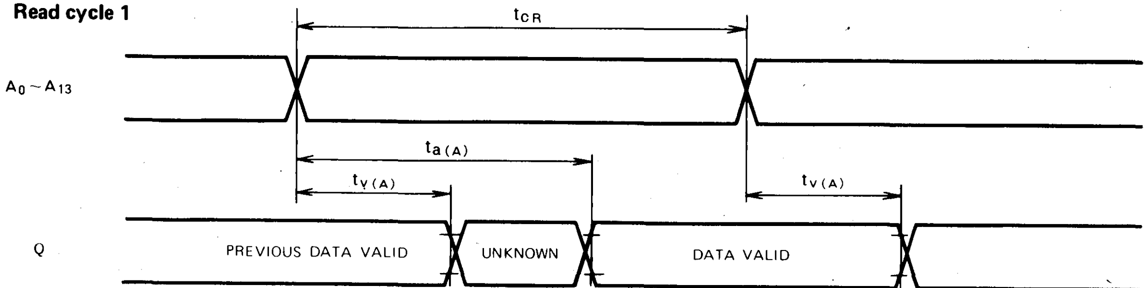


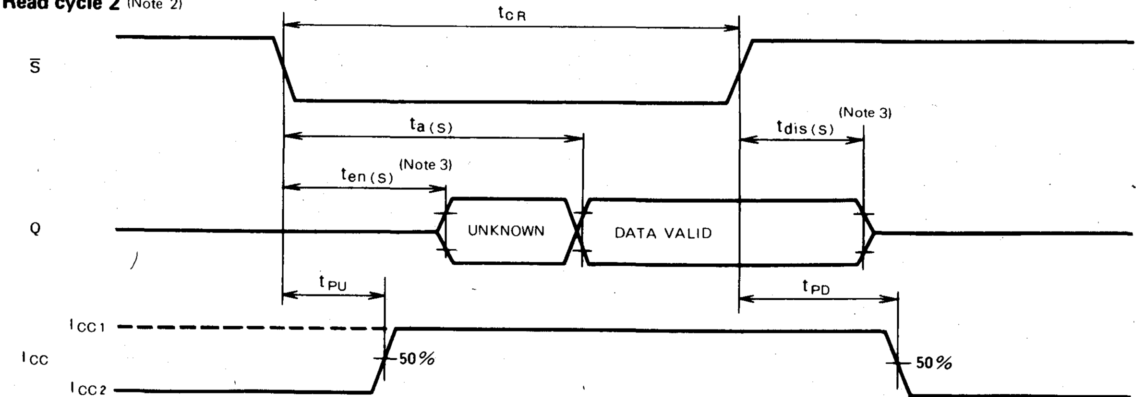
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

Read cycle 1



Read cycle 2 (Note 2)

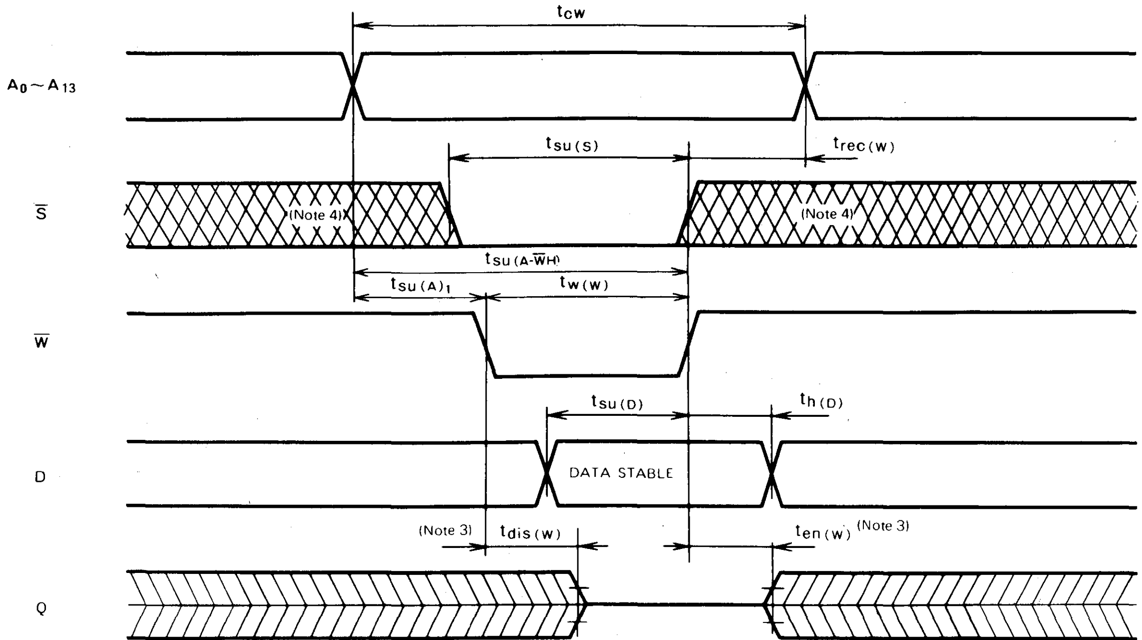


Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

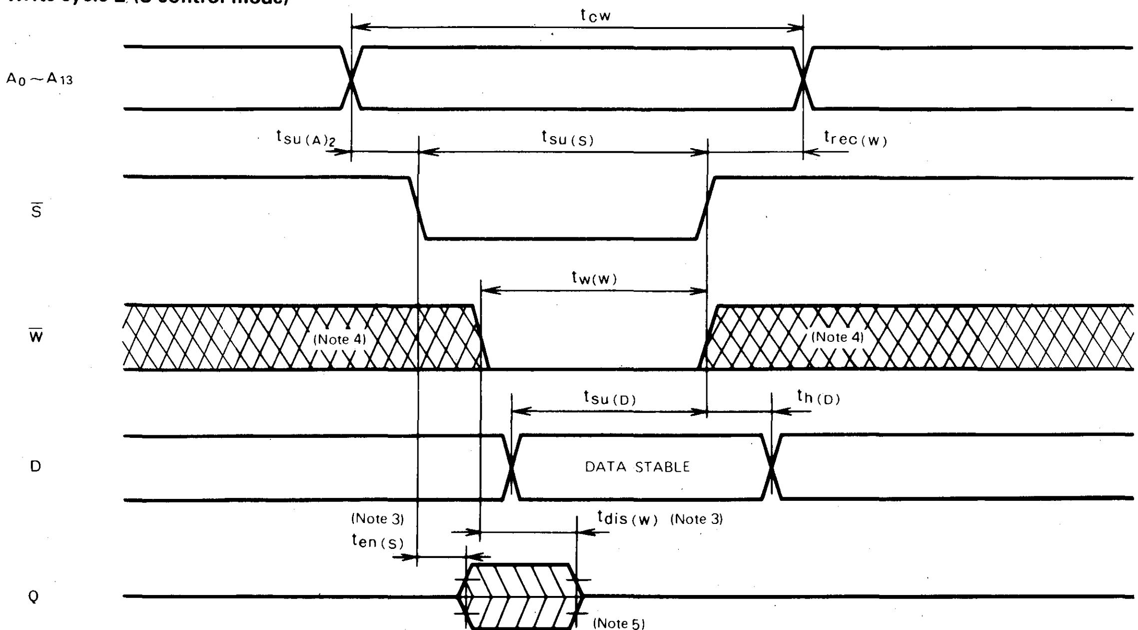
MITSUBISHI ELECTRIC

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



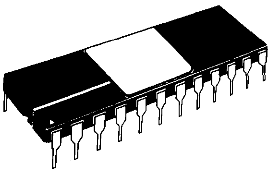
Note 4. Hatching indicates the state is don't care.

5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

ECL RAM

4

M10422S-5, -7



1024-BIT (256-WORD BY 4-BIT) STATIC RAM

DESCRIPTION

The M10422S is a 256 words by 4 bits static RAM, fabricated with the high-performance bipolar process and designed for high-speed application. The M10422S is packaged in a hermetic ceramic 24-pin dual in-line package and is specified for operation over the temperature range 0°C to 75°C.

FEATURES

- Organization .... 256 words x 4 bits
- Fully compatible with 10K series ECL families
- Address access time M10422S-5 .... 5 ns (max)
  M10422S-7 .... 7 ns (max)
- Block select access time .... 4 ns (max)
- Write pulse width M10422S-5 .... 3 ns (min)
  M10422S-7 .... 5 ns (min)
- Open emitter output for ease of memory expantion
- Standard 24 pin dual in-line package
- Interchangeable with Fairchild's F10422

APPLICATION

Scratch pad, control and buffer storage

FUNCTION

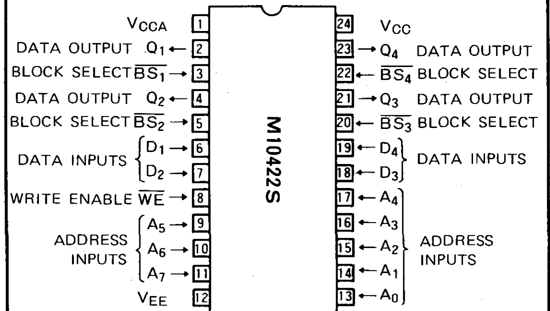
The M10422S is organized 256 words by 4 bits. It is fully compatible with 10K series ECL families.

The write operation is excuted during $\overline{BS_1}$ ~ $\overline{BS_4}$ and $\overline{WE}$ overlap time. In the period, address signals must be stable.

In the read operation, after setting $\overline{WE}$ to high and $\overline{BS_1}$ ~ $\overline{BS_4}$ to low if the address signals are stable, the data are available at the Q_1 ~ Q_4 terminal.

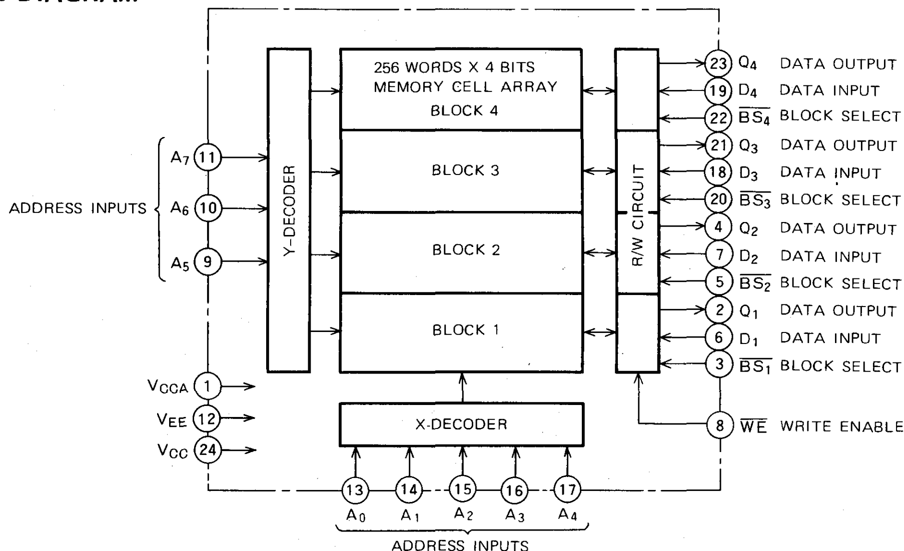
When $\overline{WE}$ is low, or $\overline{BS_1}$ ~ $\overline{BS_4}$ are high, Q_1 ~ Q_4 terminal are fixed to low.

PIN CONFIGURATION (TOP VIEW)



Outline 24S1

BLOCK DIAGRAM



OPERATION MODE

$\overline{BS}$	$\overline{WE}$	D	Mode	Q
H	X	X	Unselect	L
L	H	X	Read	Q
L	L	H	"1" Write	L
L	L	L	"0" Write	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{EE}	Supply voltage	With respect V_{CC}	+0.5~−7.0	V
V_I	Input voltage	With respect V_{CC}	+0.5~V_{EE}	V
I_O	Output current	With respect V_{CC}	−30	mA
Ta	Temperature under bias		−55~+125	°C
Tstg	Storage temperature		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
V_{EE}	Supply voltage	−5.46	−5.2	−4.94	V
Ta	Temperature under bias	0		75	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CCA} = 0V, V_{EE} = -5.2V, Output Load = 50Ω to -2.0V, air cooling > 2 m/s, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	Output voltage	$V_{IN}=V_{IHMAX}$ or V_{ILMIN}	0°C	−1000		−840	mV
			+25°C	−960		−810	
			+75°C	−900		−720	
V_{OL}			0°C	−1870		−1665	mV
			+25°C	−1850		−1650	
			+75°C	−1830		−1625	
V_{OHC}	Output thre hold voltage	$V_{IN}=V_{IHMIN}$ or V_{ILMAX}	0°C	−1020			mV
			+25°C	−980			
			+75°C	−920			
V_{OLC}			0°C			−1645	mV
			+25°C			−1630	
			+75°C			−1605	
V_{IH}	Input voltage	Guaranteed input High Voltage for all inputs	0°C	−1145		−840	mV
			+25°C	−1105		−810	
			+75°C	−1045		−720	
V_{IL}		Guaranteed input Low Voltage for all inputs	0°C	−1870		−1490	mV
			+25°C	−1850		−1475	
			+75°C	−1830		−1450	
I_{IH}	Input current	$V_{IN}=V_{IHMAX}$	0~+75°C			220	μA
I_{IL}		$\overline{BS}$ pin, $V_{IN}=V_{ILMIN}$	0~+75°C	0.5		170	μA
		except $\overline{BS}$ pin, $V_{IN}=V_{ILMIN}$		−50			
I_{EE}	Supply current	All inputs and outputs opened	0~+75°C	−220			mA

SWITCHING CHARACTERISTICS (FOR READ CYCLE)

(V_{CC} = V_{CCA} = 0V, V_{EE} = −5.2V ± 5%, Ta = 0 ~ +75°C, air cooling > 2.5 m/s, Output Load: R_L = 50Ω to −2.0V and C_L = 30pF to GND, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M10422S-5			M10422S-7			
			Min	Typ	Max	Min	Typ	Max	
t_{ABS}	Block select access time	R_L=50 Ω			4			4	ns
t_{RBS}	Block select recovery time	C_L=30pF			4			4	ns
t_{AA}	Address access time	See Figure 1			5			7	ns

SWITCHING CHARACTERISTICS (FOR WRITE CYCLE)

(V_{CC} = V_{CCA} = 0V, V_{EE} = −5.2V ± 5%, Ta = 0 ~ +75°C, air cooling > 2.5 m/s, Output Load: R_L = 50Ω to −2.0V and C_L = 30pF to GND, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M10422S-5			M10422S-7			
			Min	Typ	Max	Min	Typ	Max	
t_W	Write pulse width	t_{WSA}=1ns	3	2		5	2		ns
t_{WSD}	Data setup time		1			1			ns
t_{WHD}	Data hold time		1			1			ns
t_{WSA}	Address setup time	t_W=$t_{W(min)}$	1			1			ns
t_{WHA}	Address hold time		1			1			ns
t_{WSBS}	Block select setup time		1			1			ns
t_{WHBS}	Block select hold time		1			1			ns
t_{WS}	Write disable time			3	5		3	5	ns
t_{WR}	Write recovery time			3	5		3	5	ns

RISE AND FALL TIME

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_r	Output rise time			2		ns
t_f	Output fall time			2		ns

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input pin capacitance			3		pF
C_{out}	Output pin capacitance			5		pF

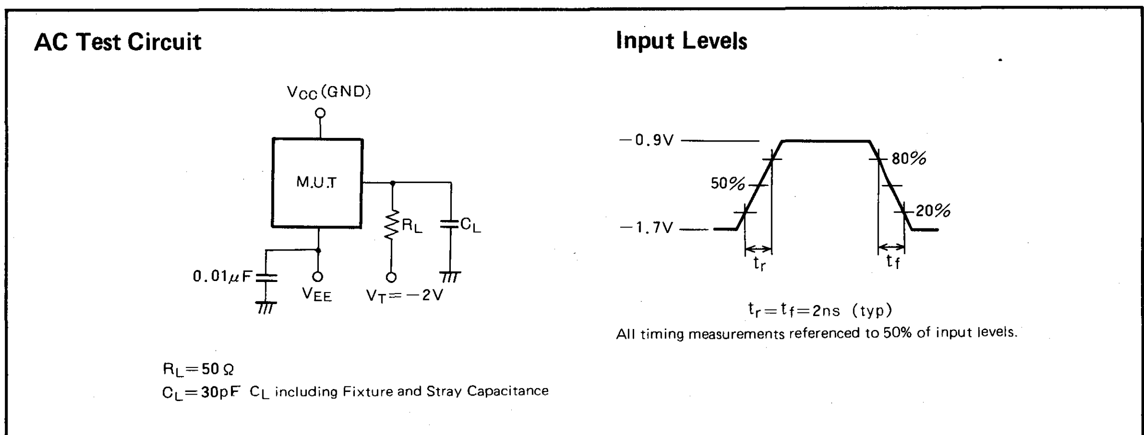
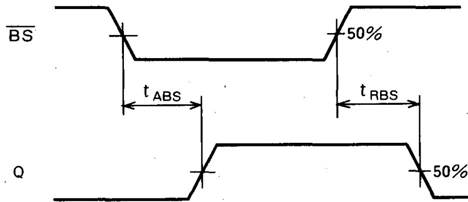


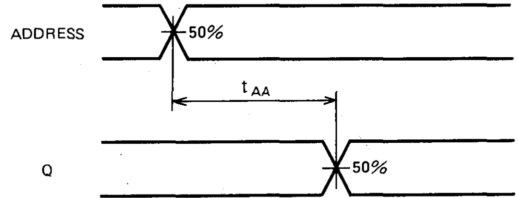
Fig. 1 Switching Test Circuit and Waveforms

Read Mode Timing

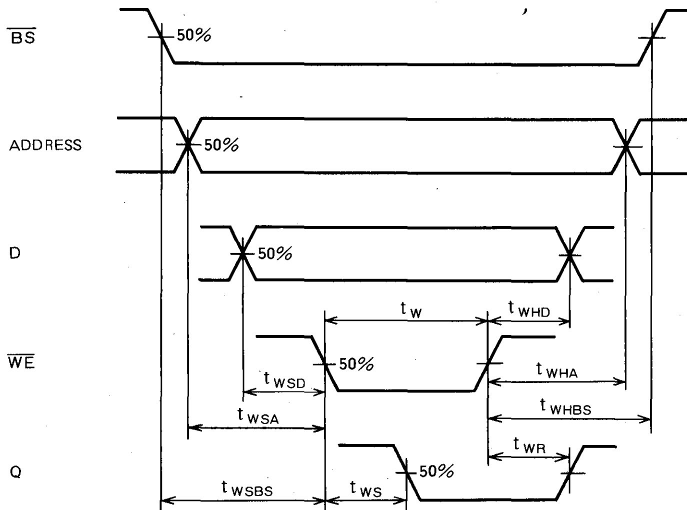
Block Select Access Time



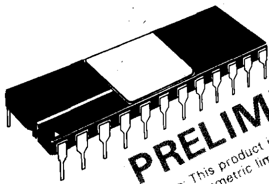
Address Access Time



Write Mode Timing



M10474S-10, -15



4096-BIT(1024-WORD BY 4-BIT)STATIC RAM

DESCRIPTION

The M10474S is a 1024 words by 4 bits static RAM, fabricated with the high-performance bipolar process and designed for high-speed application. The M10474S is packaged in a hermetic ceramic 24-pin dual in-line package and is specified for operation over the temperature range 0℃ to 75℃.

FEATURES

- Organization .... 1024 words × 4 bits
- Fully compatible with 10K series ECL families
- Address access time M10474S-10 .... 10ns (max)
  M10474S-15 .... 15ns (max)
- Write pulse width .... 5ns (min)
- Open emitter output for ease of memory expantion
- Standard 24 pin dual in-line package
- Interchangeable with Fairchild's F10474

APPLICATION

Scratch pad, control and buffer storage

FUNCTION

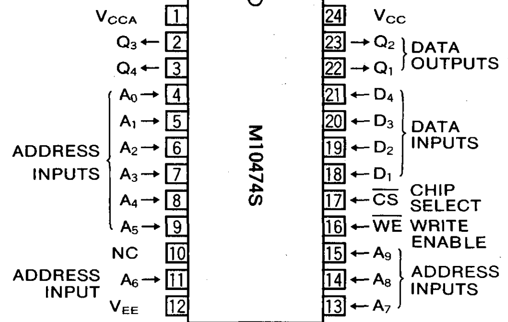
The M10474S is organized 1024 words by 4 bits. It is fully compatible with 10K series ECL families.

The write operation is excuted during $\overline{CS}$ and $\overline{WE}$ overlap time. In the period, address signals must be stable.

In the read operation, after setting $\overline{WE}$ to high and $\overline{CS}$ to low if the address signals are stable, the data are available at the $Q_1 \sim Q_4$ terminals.

When $\overline{WE}$ is low, or $\overline{CS}$ is high, $Q_1 \sim Q_4$ terminals are fixed to low.

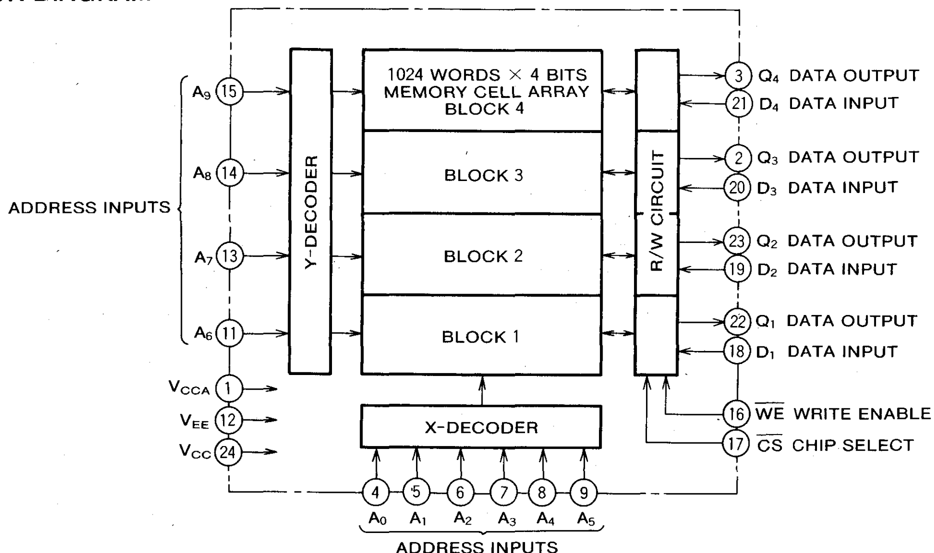
PIN CONFIGURATION (TOP VIEW)



Outline 24S1F

NC:NO CONNECTION

BLOCK DIAGRAM



OPERATION MODE

$\overline{CS}$	$\overline{WE}$	D	Mode	Q
H	X	X	Unselect	L
L	H	X	Read	Q
L	L	H	"1" Write	L
L	L	L	"0" Write	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{EE}	Supply voltage	With respect V_{CC}	+0.5~−7.0	V
V_I	Input voltage		+0.5~V_{EE}	V
I_O	Output current		−30	mA
Ta	Temperature under bias		−55~+125	℃
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	parameter	Limits			Units
		Min	Typ	Max	
V_{EE}	Supply voltage	−5.46	−5.2	−4.94	V
Ta	Temperature under bias	0		75	℃

ELECTRICAL CHARACTERISTICS

($V_{CC}=V_{CCA}=0V$, $V_{EE}=-5.2V$, Output Load=50Ω to −2.0V, air cooling > 2.5m/s, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	Output voltage	$V_{IN}=V_{IHMAX}$ or V_{ILMIN}	0℃	−1000		−840	mV
			+25℃	−960		−810	
			+75℃	−900		−720	
V_{OL}			0℃	−1870		−1665	mV
			+25℃	−1850		−1650	
			+75℃	−1830		−1625	
V_{OHC}	Output threshold voltage	$V_{IN}=V_{IHMIN}$ or V_{ILMAX}	0℃	−1020			mV
			+25℃	−980			
			+75℃	−920			
V_{OLC}			0℃			−1645	mV
			+25℃			−1630	
			+75℃			−1605	
V_{IH}	Input voltage	Guaranteed input High Voltage for all inputs	0℃	−1145		−840	mV
			+25℃	−1105		−810	
			+75℃	−1045		−720	
V_{IL}		Guaranteed input Low Voltage for all inputs	0℃	−1870		−1490	mV
			+25℃	−1850		−1475	
			+75℃	−1830		−1450	
I_{IH}	Input current	$V_{IN}=V_{IHMAX}$	0~+75℃			220	μA
I_{IL}		$\overline{CS}$ pin, $V_{IN}=V_{ILMIN}$	0~+75℃	0.5		170	μA
		Except $\overline{CS}$ pin, $V_{IN}=V_{ILMIN}$		−50			
I_{EE}	Supply current	All inputs and outputs opened	0~+75℃	−220			mA

SWITCHING CHARACTERISTICS (FOR READ CYCLE)

($V_{CC}=V_{CCA}=0V$, $V_{EE}=-5.2V\pm5\%$, $T_a=0\sim+75°C$, air cooling > 2.5m/s, Output Load: $R_L=50\Omega$ to −2.0V and $C_L=30pF$ to GND, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M10474S-10			M10474S-15			
			Min	Typ	Max	Min	Typ	Max	
t_{ACS}	Chip select access time	$R_L=50\Omega$			6			6	ns
t_{RCS}	Chip select recovery time	$C_L=30pF$			6			6	ns
t_{AA}	Address access time	See Figure 1			10			15	ns

SWITCHING CHARACTERISTICS (FOR WRITE CYCLE)

($V_{CC}=V_{CCA}=0V$, $V_{EE}=-5.2V\pm5\%$, $T_a=0\sim+75°C$, air cooling > 2.5m/s, Output Load: $R_L=50\Omega$ to −2.0V and $C_L=30pF$ to GND, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M10474S-10			M10474S-15			
			Min	Typ	Max	Min	Typ	Max	
t_W	Write pulse width	$t_{WSA}=2ns$	5	3		5	3		ns
t_{WSD}	Data setup time		2			2			ns
t_{WHD}	Data hold time		2			2			ns
t_{WSA}	Address setup time	$t_W=5ns$	2			2			ns
t_{WHA}	Address hold time		2			2			ns
t_{WSCS}	Chip select setup time		2			2			ns
t_{WHCS}	Chip select hold time		2			2			ns
t_{WS}	Write disable time				5			5	ns
t_{WR}	Write recovery time				12			12	ns

RISE AND FALL TIME

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_r	Output rise time			2		ns
t_f	Output fall time			2		ns

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input pin capacitance			3		pF
C_{OUT}	Output pin capacitance			5		pF

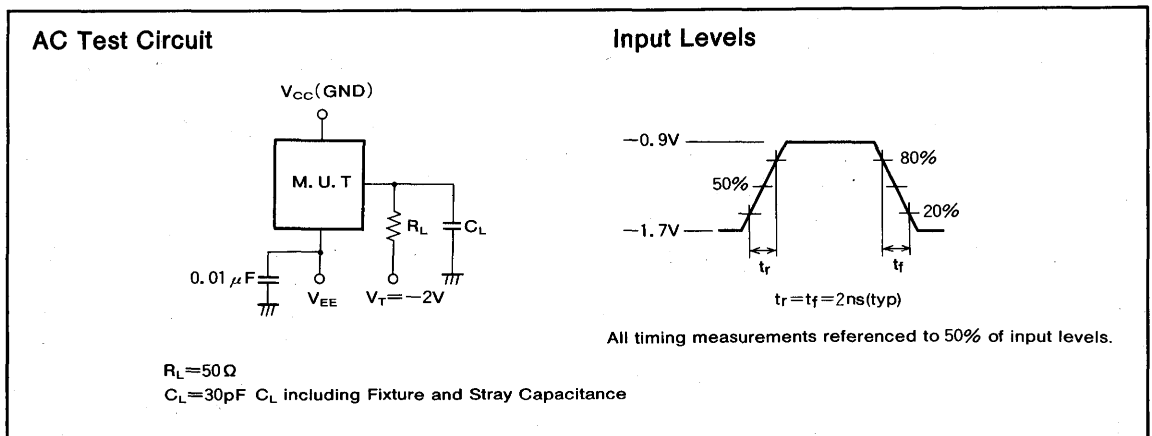
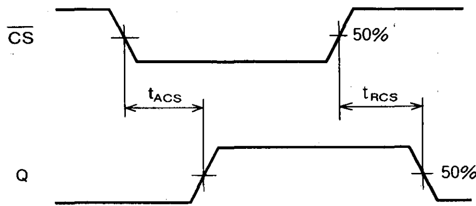


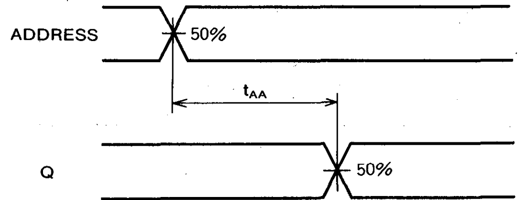
Fig. 1 Switching Test Circuit and Waveforms

Read Mode Timing

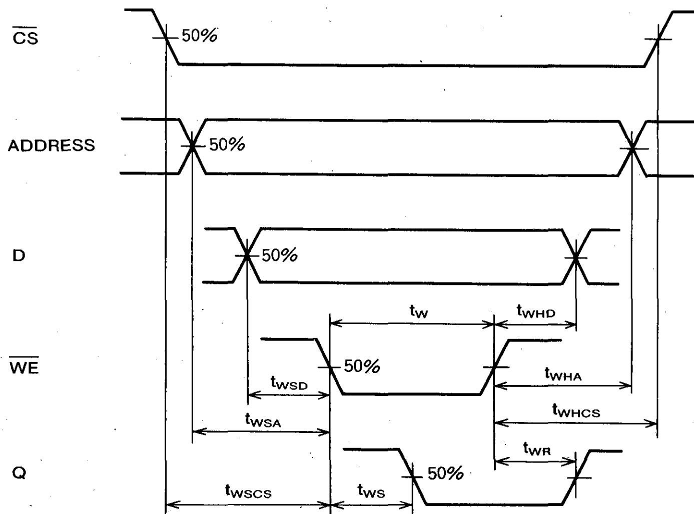
Chip Select Access Time



Address Access Time



Write Mode Timing



MITSUBISHI ELECTRIC

MOS MASK ROM

5

MASK ROM ORDERING METHOD

MASK ROM ORDERING METHOD

Mitsubishi Electric Corp. receives the data for writing programs in the mask ROMs by EPROMs.

When placing an order, submit three sets of the EPROMs in which the data for each pattern are written and the prescribed confirmation statements. If another medium is to be used, consult with Mitsubishi first.

EPROM PRECAUTIONS

1. Mitsubishi's EPROMs are standard, but any EPROMs are available.
2. The EPROM data and address are processed with the contents of "H" taken as "1".
3. Write the products being ordered and the address assignment in the EPROMs. The address to be assigned are written in the confirmation statements.
4. If discrepancies between the EPROMs submitted are found, a notice to that effect will be issued.

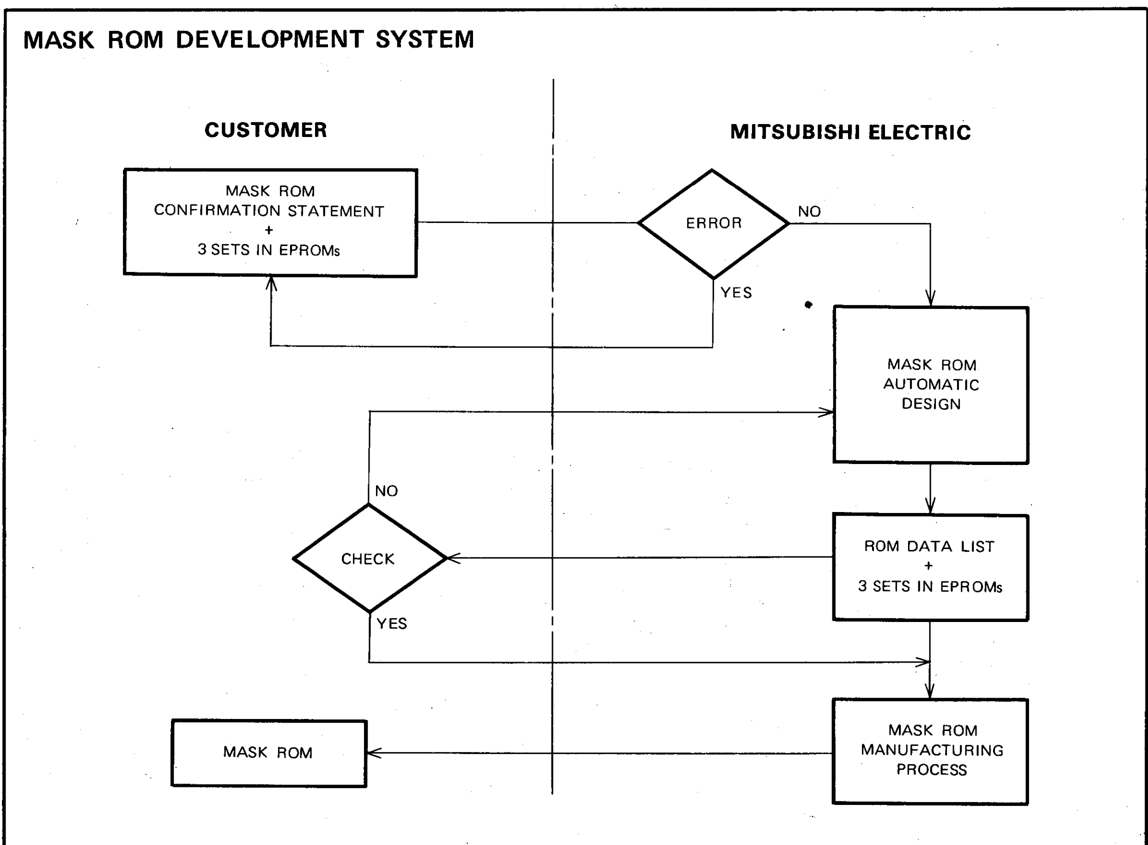
ITEMS TO BE ISSUED WHEN ORDERING

1. Masking confirmation statement . . . . 1 copy
2. Data for ROMs . . . . 3 sets in RPROMs

OPTIONS

Refer to the data book and make the appropriate entries in the confirmation statement.

The ROMs will be prepared in accordance with the data in the EPROMs and the mask confirmation sattelement submitted. The EPROMs and the confirmation statement will not be returned.



Mask ROM number	

Receipt	Date : Year/month/day	
	Section head signature	Supervisor signature

MITSUBISHI MASK ROMs CONFIRMATION STATEMENT

M5M2364-XXXP(28 Pin, 64K Bit)

Note : Please fill in all items marked ※

※ Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
	Date issued	Date : Year/month/day			

1. Confirmation

   Specify the EPROMs submitted.

   3 sets EPROM must be 64K bit (2764), in which the data for each pattern are written.

※ Parts numbers   1. Mask not needed   2. Mark needed

Mitsubishi IC type number -

Note 1 : The mark field should be written to the right.

2 : The identification mark can be up to 12 alphanumeric characters (except J, I and O) and hyphens.

※ Comments

Mask ROM number	

Receipt	Date : Year/month/day	
	Section head signature	Supervisor signature

MITSUBISHI MASK ROMs CONFIRMATION STATEMENT

☐ M5M23128-XXXP(128K Bit)
☐ M5M23256-XXXP(256K Bit)
☐ M5M231000-XXXP(NMOS 1M Bit)
※☐ M5M23C100-XXXP(CMOS 1M Bit)

Note : Please fill in all items marked ※

※ Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
	Date issued	Date : Year/month/day			

※1. Confirmation

Specify the EPROMs submitted.

An EPROM must be submitted for each pattern. (Check @ in the appropriate box.)

MASK ROM \ EPROM	27128	27256
☐M5M23128-XXXP	☐A(0000～3FFF)	☐A(0000～3FFF)

MASK ROM \ EPROM	27128	27256
☐M5M23256-XXXP	☐A(0000～3FFF) ☐B(4000～7FFF)	☐A(0000～7FFF)

MASK ROM \ EPROM	27256	27512
☐M5M231000-XXXP ☐M5M23C100-XXXP	☐A(00000～07FFF) ☐B(08000～0FFFF) ☐C(10000～17FFF) ☐D(18000～1FFFF)	☐A(00000～0FFFF) ☐B(10000～1FFFF)

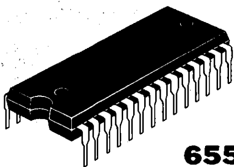
※2. Parts numbers 1. Mark not needed 2. Mark needed

Mitsubishi IC type number

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 12 aiphanumeric characters (except J, I and O) and hyphens.

※3. Comments

M5M2364-XXXP



65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M2364-XXXP is a 65536-bit mask-programmable high speed read-only memory.

The M5M2364-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIP It is interchangeable with the M5L2764K and Intel 2764 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

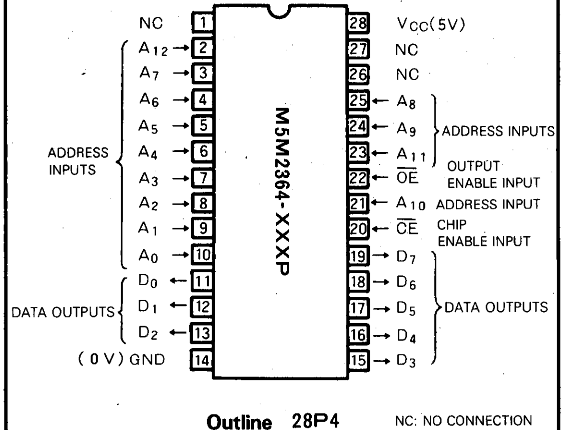
FEATURES

- 8192 words × 8-bit organization
- Access time .... 250 ns (MAX)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply
  Current (Icc) active .... 80 mA (MAX)
  standby .... 20 mA (MAX)
- Single 5V power supply ($V_{CC}=5V\pm10\%$)
- 3-State output buffer
- Input and output
- Standard 28-pin DIP
- Interchangeable with the M5L2764K and Intel 2764

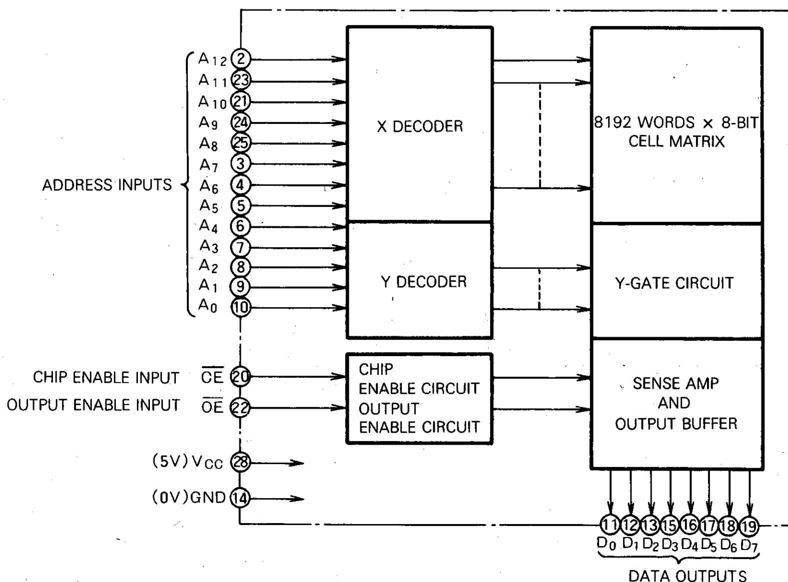
APPLICATION

Electronic computers and various software

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level).

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
T_{opr}	Operating temperature		−10~80	°C
T_{stg}	Storage temperature		−65~150	°C
V_I	Input voltage	With respect to GND	−0.6~7	V

DC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

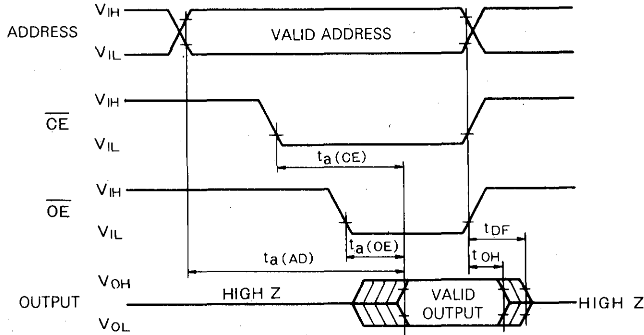
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ	Max	
I_{LI}	Input leakage current	$V_{IN}=5.5V$	−10		10	μA
I_{LO}	Output leakage current	$V_{OUT}=5.5V$	−10		10	μA
I_{CC1}	V_{CC} Supply voltage (Standby)	$\overline{CE}=V_{IH}$		10	20	mA
I_{CC2}	V_{CC} Supply voltage (Operating)	$\overline{CE}=\overline{OE}=V_{IL}$		40	80	mA
V_{IL}	Low level input voltage		−0.1		0.8	V
V_{IH}	High level input voltage		2.0		$V_{CC}+1$	V
V_{OL}	Low level output voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	High level output voltage	$I_{OH}=-400\mu A$	2.4			V

Note 2. Typical value is that with standard supply voltage applied and $T_a = 25°C$.

AC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address access time	$\overline{CE}=\overline{OE}=V_{IL}$			250	ns
$t_{a(CE)}$	$\overline{CE}$ access time	$\overline{OE}=V_{IL}$			250	ns
$t_{a(OE)}$	$\overline{OE}$ access time	$\overline{CE}=V_{IL}$	10		100	ns
t_{DF}	$\overline{OE}$ output floating delay time	$\overline{CE}=V_{IL}$	0		90	ns
t_{OH}	Data validity period after $\overline{OE}$, $\overline{CE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0			ns

READ-OUT TIMING DIAGRAM



Switching Characteristics Test Conditions

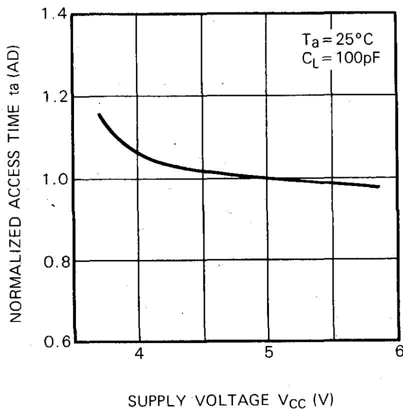
Input voltage: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
Input signal rise-fall time: ≤20ns
Reference voltage for timing measurements: Input 1V, 2V
Output 0.8V, 2V
Loading: 1TTL gate +CL (=100pF)

INPUT/OUTPUT CAPACITANCE ($T_a = 25°C$, f = 1MHz, unless otherwise specified)

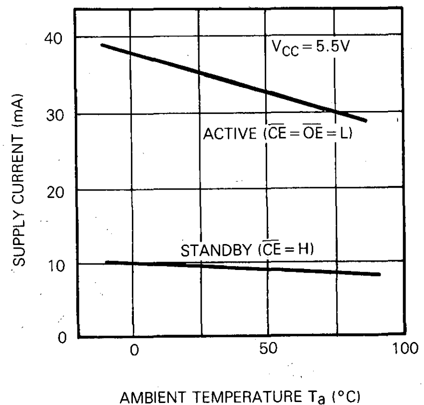
Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		8	12	pF

TYPICAL CHARACTERISTICS

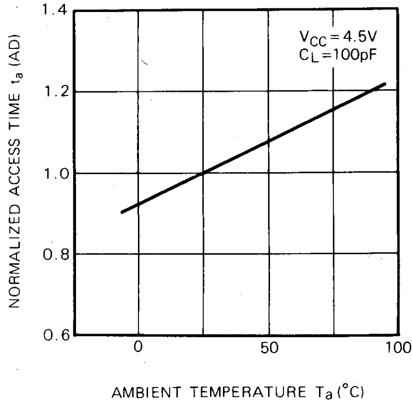
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



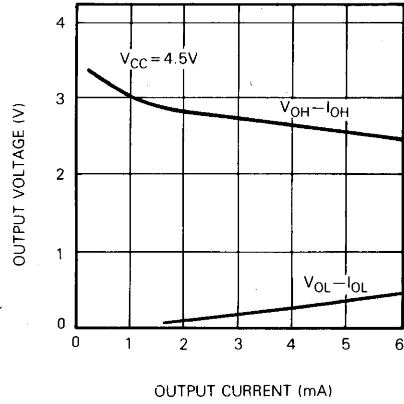
SUPPLY CURRENT VS AMBIENT TEMPERATURE



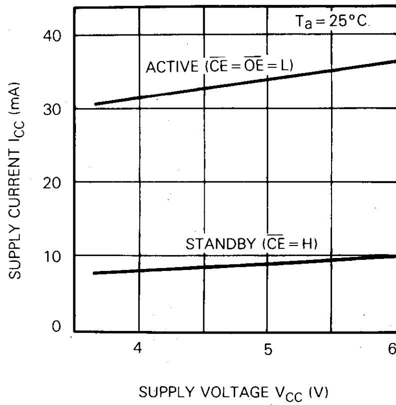
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



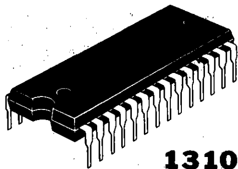
OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS SUPPLY VOLTAGE



M5M23128-XXXP



131072-BIT(16384-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M23128-XXXP is a 131072-bit mask-programmable high speed read-only memory.

The M5M23128-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIP It is interchangeable with the M5L27128K and Intel 27128 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 16384 word x 8-bit organization
- Access time .... 250ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply current (I_{CC}) Active .. 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIP
- Interchangeable with the M5L27128K and Intel 27128

APPLICATION

Electronic computers and various software.

FUNCTION

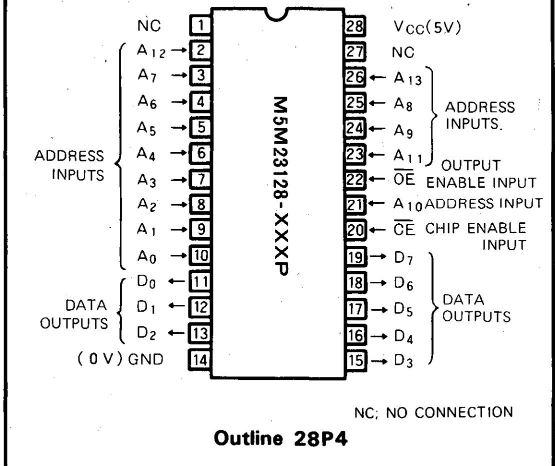
Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level.)

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

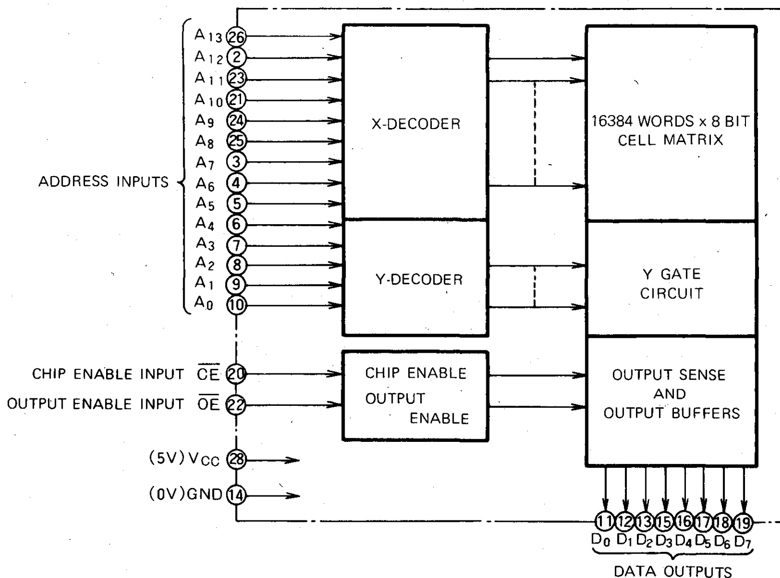
When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating temperature .... $-10°C \sim +80°C$
Storage temperature .... $-65°C \sim +150°C$
All input or output voltage** .... $-0.6V \sim +7V$

COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.
** With respect to Ground.

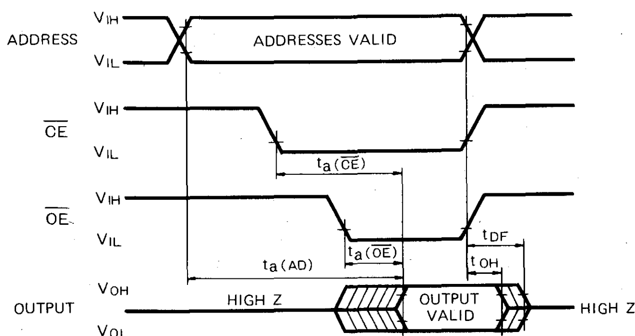
D.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$		15	30	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}=V_{IL}$		40	80	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$			250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$			250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}=V_{IL}$	10		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0		90	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0			ns

A.C. WAVEFORMS



Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

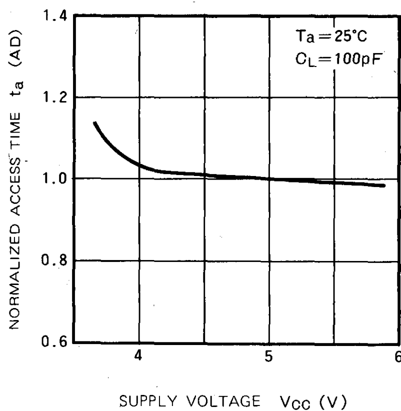
131072-BIT(16384-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

CAPACITANCE (T_a=25°C, f=1MHz)

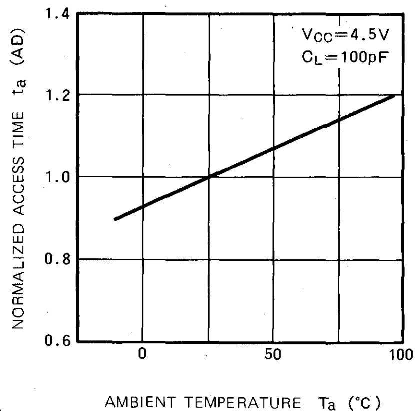
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		8	12	pF

TYPICAL PERFORMANCE DATA

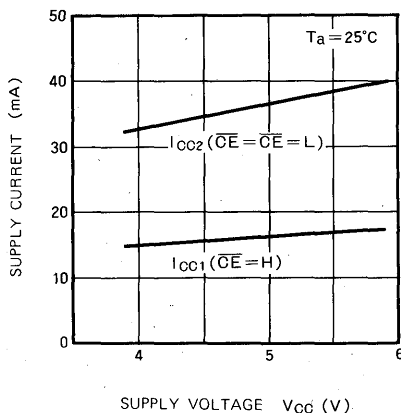
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



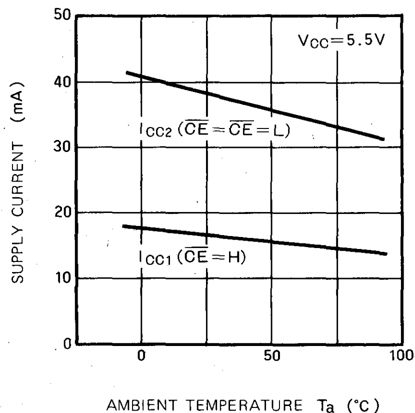
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



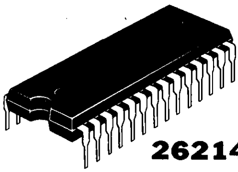
SUPPLY CURRENT VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE



M5M23256-XXXP



262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M23256-XXXP is a 262144-bit mask-programmable high speed read-only memory.

The M5M23256-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIP It is compatible with the M5L27256K and Intel 27256 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 32768 word x 8-bit organization
- Access time . . . . 250ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply current (I_{CC}) Active . . 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIP
- Compatible with Intel 27256

APPLICATION

Electronic computers and various software.

FUNCTION

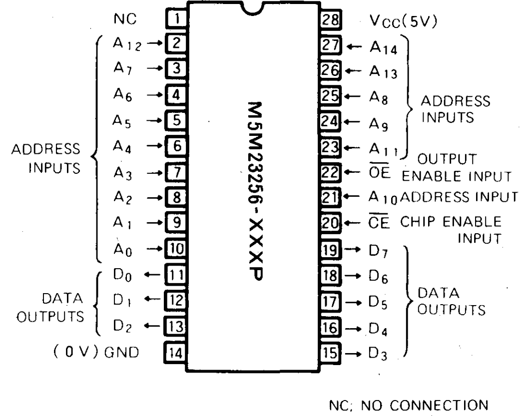
Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level.)

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

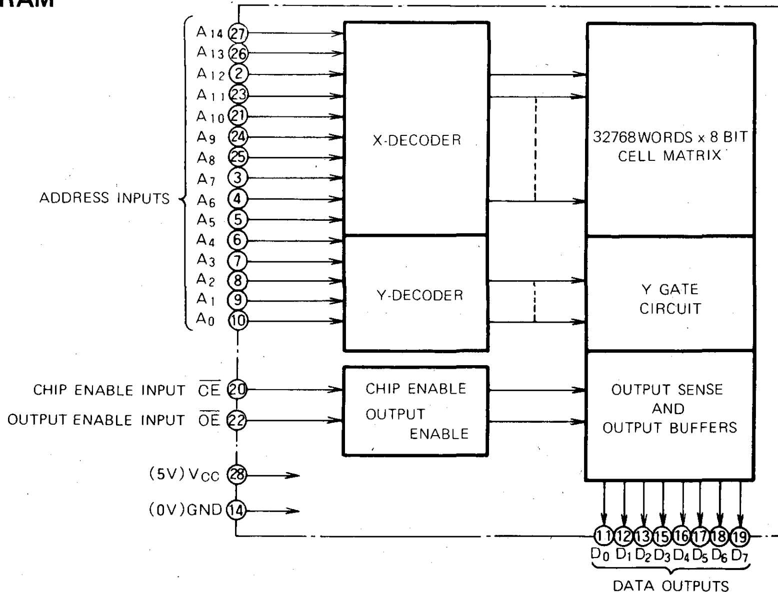
When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS*

Operating temperature . . . . −10°C ~ +80°C
Storage temperature . . . . −65°C ~ +150°C
All input or output voltage** . . . . −0.6V ~ +7V

COMMENT

* Stresses above those listed may cause permanent damage to the device.
  This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
  Exposure to absolute maximum rating conditions for extended periods affects device reliability.

** With respect to Ground.

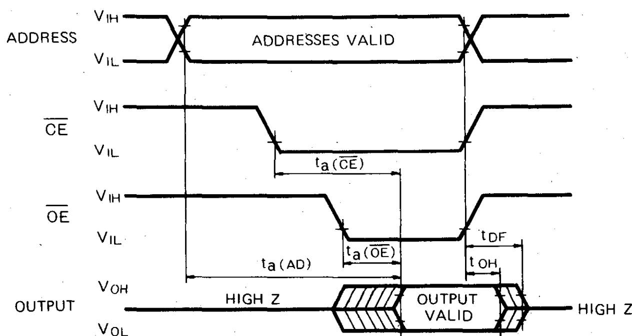
D.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$		15	30	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}=V_{IL}$		40	80	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$			250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$			250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}=V_{IL}$	10		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0		90	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0			ns

A.C. WAVEFORMS



Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

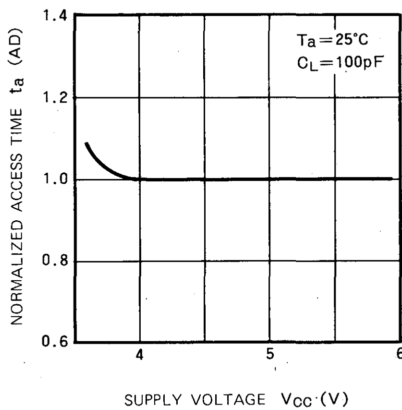
262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

CAPACITANCE (T_a=25°C, f=1MHz)

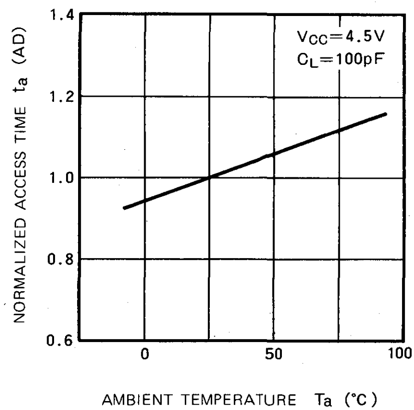
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		8	12	pF

TYPICAL PERFORMANCE DATA

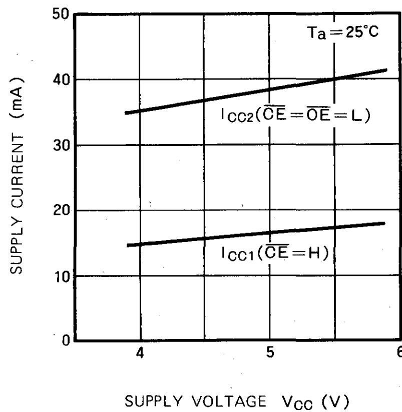
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



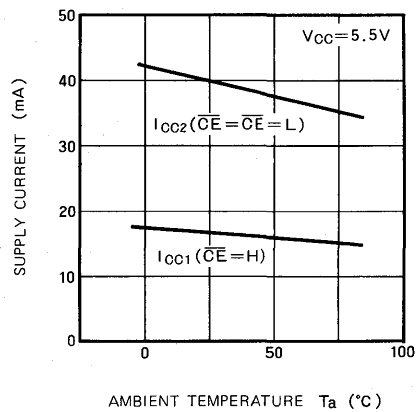
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE

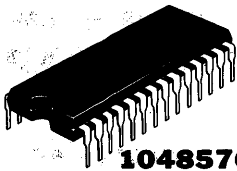


SUPPLY CURRENT VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE





M5M231000-XXXP

1048576-BIT (131072-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M231000-XXXP is 1048576-bit mask-programmable high speed read-only memory.

The M5M231000-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIP

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 131072 word x 8-bit organization
- Access time .... 250ns (max)
- ONE line control $\overline{CE}$
- Low power supply current (I_{CC}) Active .. 60mA (max)
  Standby . 20mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIP

APPLICATION

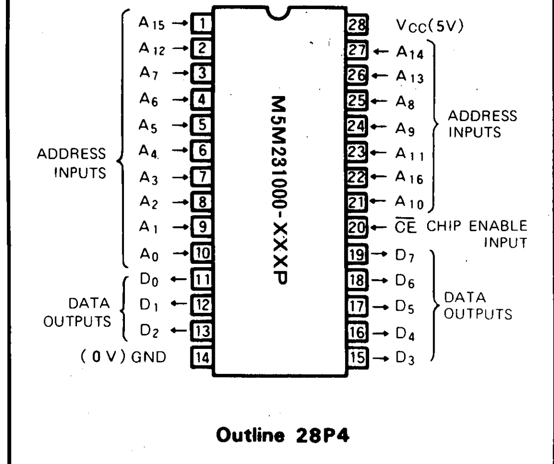
Electronic computers and various software.

FUNCTION

Set the CE terminals to the read mode (low level.)

Low level input to $\overline{CE}$ and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

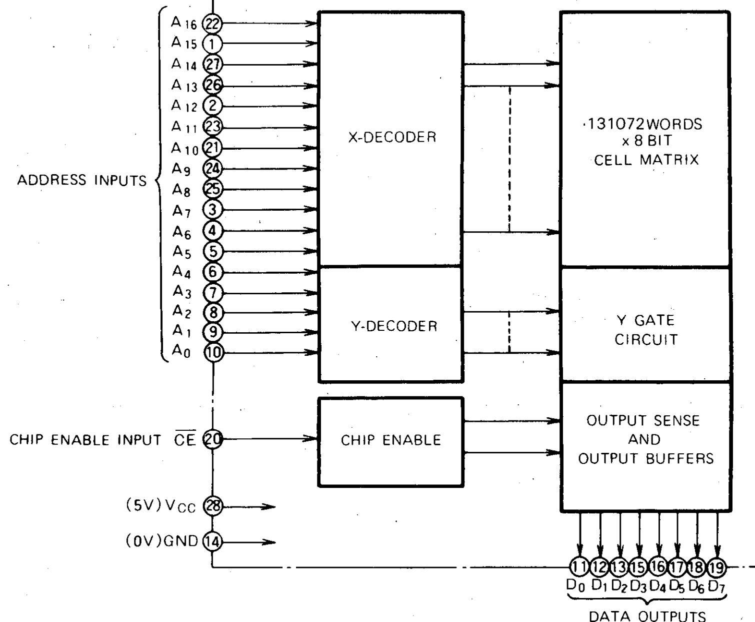
PIN CONFIGURATION (TOP VIEW)



Outline 28P4

When the $\overline{CE}$ signal is high, data output are in a floating state and the device is in the standby mode or power-down mode.

BLOCK DIAGRAM



1048576-BIT (131072-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS*

Operating temperature .... −10°C ~ +80°C
Storage temperature .... −65°C ~ +150°C
All input or output voltage** .... −0.6V ~ +7V

COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.

** With respect to Ground.

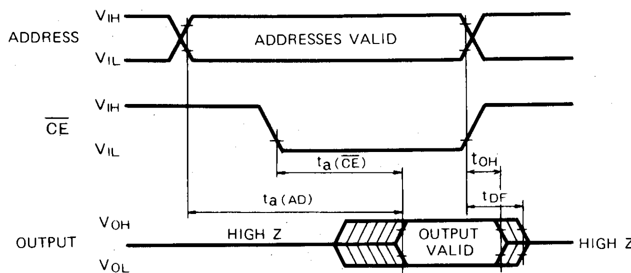
D.C. ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$		10	20	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=V_{IL}$		30	60	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=V_{IL}$		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay			250	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0	80	ns
t_{OH}	Output hold from $\overline{CE}$	$\overline{CE}=V_{IL}$	0		ns

A.C. WAVEFORMS

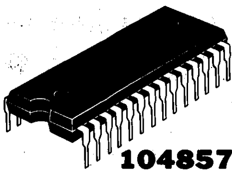


Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

CAPACITANCE (T_a=25°C, f=1MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		6	10	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		6	10	pF



M5M231001-XXXP

1048576-BIT (131072-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M231001-XXXP is 1048576-bit mask-programmable high speed read-only memory.

The M5M231001-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIP.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 131072 word x 8-bit organization
- Access time . . . . 200ns (max)
- One line control $\overline{OE}$
- Low power supply current (I_{CC}) Active . . 60mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIP

APPLICATION

Electronic computers and various software

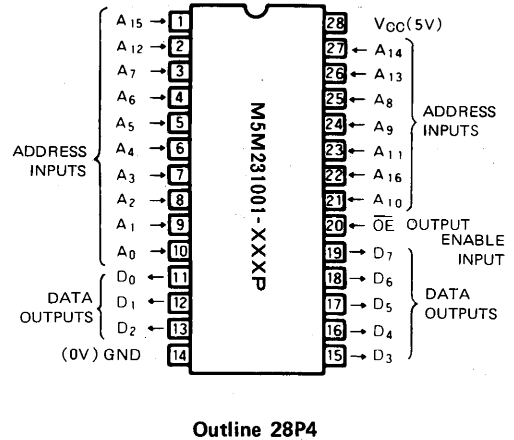
FUNCTION

Set the $\overline{OE}$ terminals to the read mode (low level.)

Low level input to $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

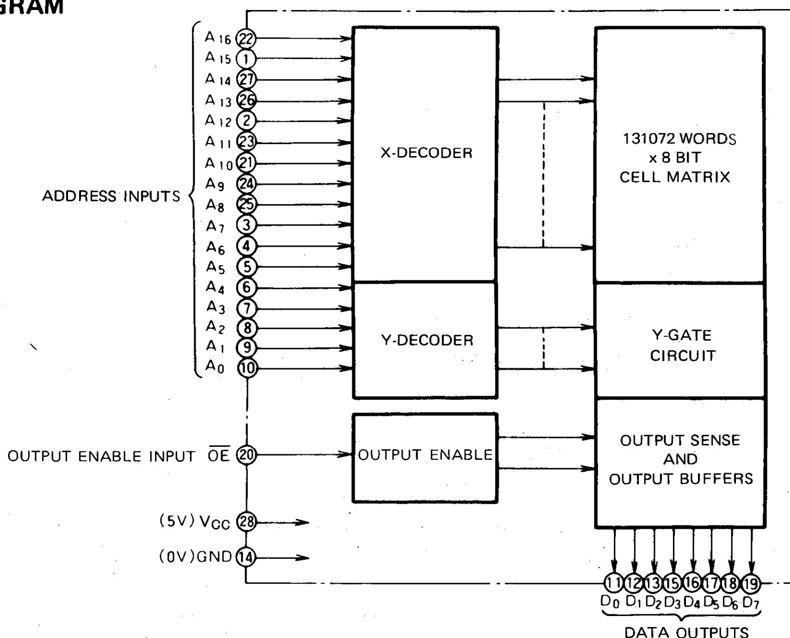
When the $\overline{OE}$ signal is high, data output are in a floating state.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating temperature . . . . −10°C ~ +80°C
Storage temperature . . . . −65°C ~ +150°C
All input or output voltage** . . . . −0.6V ~ +7V

COMMENT

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

** With respect to Ground.

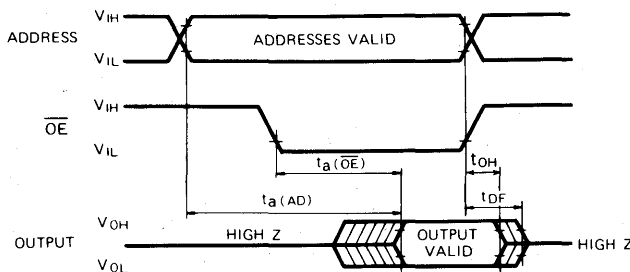
D.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC}	V_{CC} current active			30	60	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$\overline{OE}$=V_{IL}			200	ns
$t_{a(\overline{OE})}$	$\overline{OE}$ to output delay				80	ns
t_{DF}	Output enable high to output float				55	ns
t_{OH}	Output hold from $\overline{OE}$		0			ns

A.C. WAVEFORMS

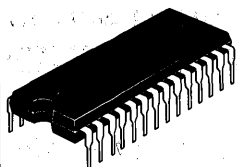


Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≤ 20ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

CAPACITANCE (T_a=25°C, f=1MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		6	10	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		6	10	pF



M5M23C100-XXXP

1048576-BIT (131072-WORD BY 8-BIT) CMOS MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M23C100-XXXP is 1048576-bit mask-programmable high speed read-only memory.

The M5M23C100-XXXP is fabricated by silicon gate CMOS technology and available in a 28-pin DIP.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 131072 words x 8-bit organization
- Access time .... 250 ns (max)
- Low power supply current (I_{CC})
  - Active ...... 30 mA (max)
  - Standby ..... 1 mA (max) (TTL-compatible)
  - 100 μA (max) ($\overline{CE} = V_{CC}$)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIP

APPLICATION

Microcomputer systems and peripheral equipment

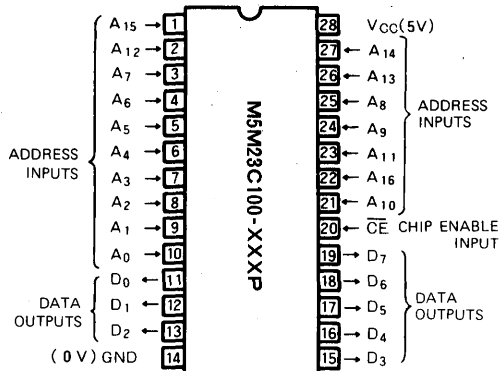
FUNCTION

Set the $\overline{CE}$ terminals to the read mode (low level.)

Low level input to $\overline{CE}$ and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the dat output ($D_0 \sim D_7$).

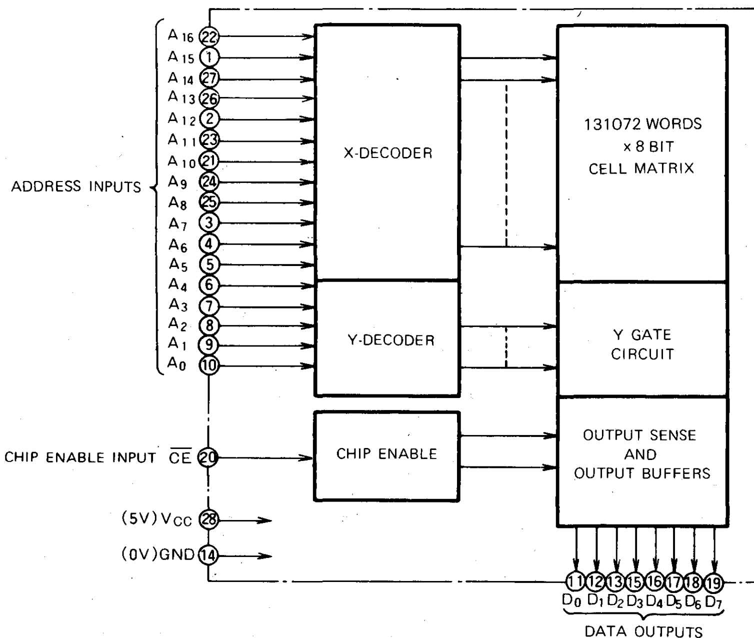
When the $\overline{CE}$ signal is high, data outputs are in a floating state and the device is in the standby mode or power-down mode.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating temperature .... −10°C ~ +80°C
Storage temperature .... −65°C ~ +150°C
All input or output voltage (Note 2) .... −0.6V ~ +7V

Note 1: Stresses above those listed may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.
Note 2: With respect to Ground.

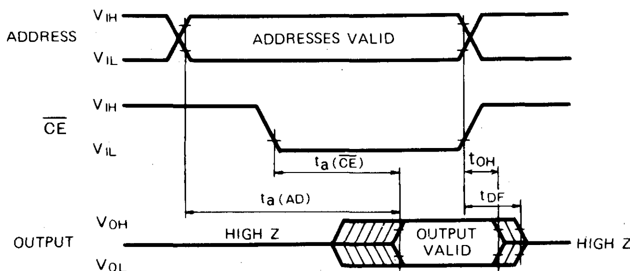
D.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}$=V_{IH}			1	mA
		$\overline{CE}$=V_{CC}		1	100	μA
I_{CC2}	V_{CC} current active	$\overline{CE}$=V_{IL}, 4MHz			30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$=V_{IL}		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay			250	ns
t_{DF}	Output enable high to output float		0	80	ns
t_{OH}	Output hold from $\overline{CE}$		0		ns

A.C. WAVEFORMS

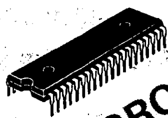


Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20 ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

CAPACITANCE (T_a=25°C, f=1MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		6	10	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		6	10	pF



M5M23C400-XXXP

4194304-BIT(262144-WORD BY 16-BIT)CMOS MASK-PROGRAMMABLE ROM /4194304-BIT(524288-WORD BY 8-BIT)CMOS MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M23C400-xxxP is 4194304-bit mask-programmable high speed read-only memory.

The M5M23C400-xxxP is fabricated by CMOS single gate technology and available in a 40-pin DIP.

The xxx in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

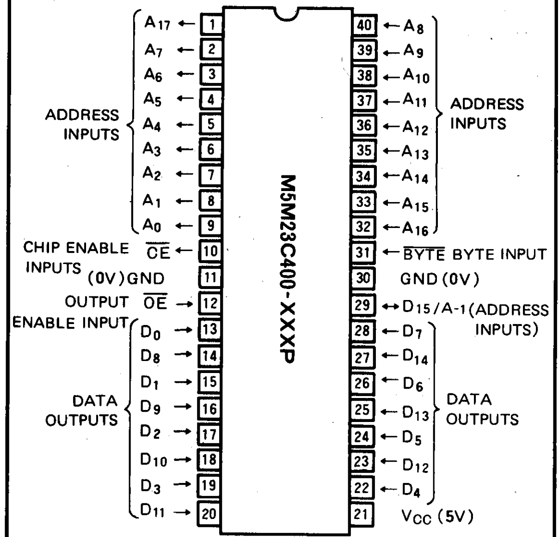
FEATURES

- 262144 words x 16 bit/524288 word x 8 bit organization
- Access time 250ns
- Low power supply current (I_{CC}): Active 30mA
  Standby 100μA
- 2 line control $\overline{OE}$, $\overline{CE}$
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible

APPLICATION

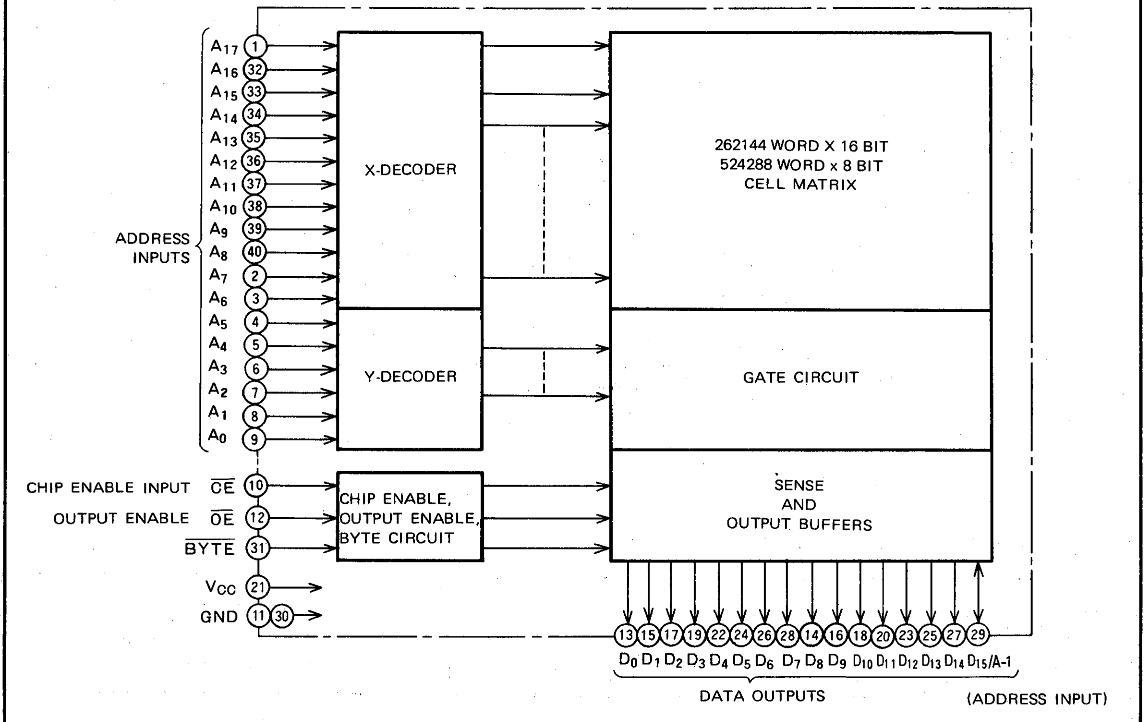
Electronic computers and various software.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



4194304-BIT (262144-WORD BY 16-BIT) CMOS MASK-PROGRAMMABLE ROM /4194304-BIT (524288-WORD BY 8-BIT) CMOS MASK-PROGRAMMABLE ROM

FUNCTION

Low level input to $\overline{CE}$, $\overline{OE}$, $\overline{BYTE}$ and address signal to the address inputs ($A_{-1} \sim A_{17}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).

When the $\overline{BYTE}$ signal is high, and address signals to the address inputs ($A_0 \sim A_{17}$), data outputs are $D_0 \sim D_{15}$.

When the $\overline{CE}$ or $\overline{OE}$ signal is high, data outputs are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (10)	$\overline{OE}$ (12)	$\overline{BYTE}$ (31)	V_{CC} (21)	Outputs $D_0 \sim D_7$ (13, 15, 17, 19, 22, 24, 26, 28)	Outputs $D_8 \sim D_{15}$ (14, 16, 18, 20, 23, 25, 27, 29)
Read	V_{IL}	V_{IL}	V_{IL}	V_{CC}	Data out	Floating
	V_{IL}	V_{IL}	V_{IH}	V_{CC}	Data out	Data out
Standby	V_{IH}	X	X	V_{CC}	Floating	Floating

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating temperature . . . . -10°C ~ +80°C
Storage temperature . . . . -65°C ~ +150°C
All input or output voltage (Note 2) . . . . -0.6V ~ +7V

Note 1: Stresses above those listed may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.
Note 2: With respect to Ground.

D.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

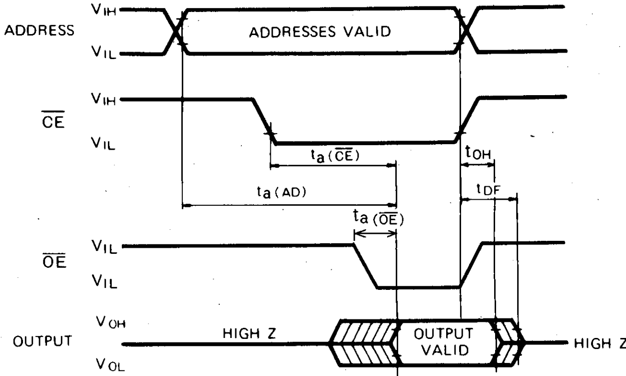
Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{LI}	Input leakage current	V_{IN}=5.5V	−10		10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V	−10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			1	mA
		$\overline{CE}=V_{CC}$		1	100	μA
I_{CC2}	V_{CC} current active	$\overline{CE}=V_{IL}$, 4MHz			30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

A.C. ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V± 10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits Min	Limits Max	Unit
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}$=L		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}$=L		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}$=L		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}$=L	0	80	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$		0		ns

4194304-BIT (262144-WORD BY 16-BIT) CMOS MASK-PROGRAMMABLE ROM /4194304-BIT (524288-WORD BY 8-BIT) CMOS MASK-PROGRAMMABLE ROM

A.C. WAVEFORMS



Test Conditions for A.C. Characteristics

Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20 ns
Reference voltage at timing measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output load: 1 TTL gate, C_L = 100pF

CAPACITANCE (T_a=25°C, f=1MHz)

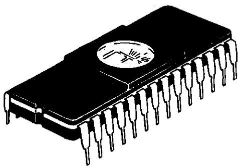
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		6	10	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		6	10	pF

MOS EPROM

6

M5L2764K, -2

65536-BIT (8192-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5L2764K is a high-speed 65536-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L2764K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

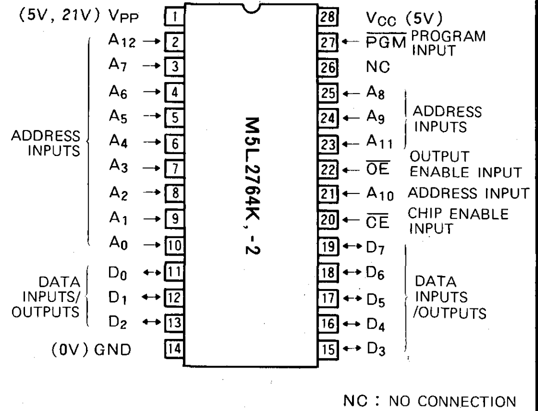
FEATURES

- 8192 Word x 8-bit Organization
- Access Time M5L2764K-2 200 ns (max)
  M5L2764K 250 ns (max)
- Two Line Control $\overline{OE}$, $\overline{CE}$
- Low Power Current (I_{CC}) Active ..... 100 mA (max)
  Standby ... 35 mA (max)
- Single 5V Power Supply
- 3-State Output Buffer
- Input and Output TTL-Compatible in Read and Program Mode
- Standard 28-pin DIP
- Single Location Programming with One 50 ms Pulse
- Fast programming algorithm
- Interchangeable with INTEL 2764

APPLICATION

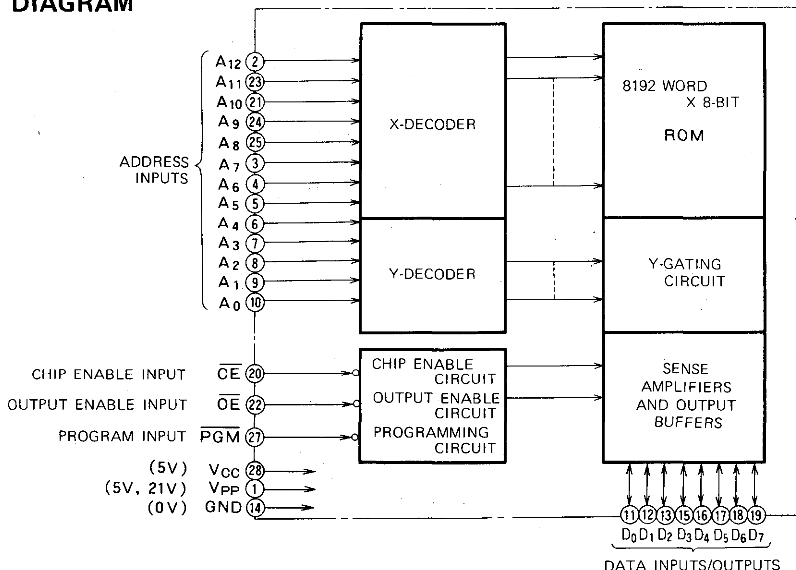
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K1

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level).
Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

In the read mode V_{PP} must be at V_{CC} level.

Programming

(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.7)

(Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the V_{PP} power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{12}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms$\leqq t_{PW} \leqq$55 ms.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	X*	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10~80	°C
T_{stg}	Storage temperature	−65~125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~26.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

65536-BIT (8192-WORD BY 8-BIT)
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

READ OPERATION

$Ta = 0°$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$

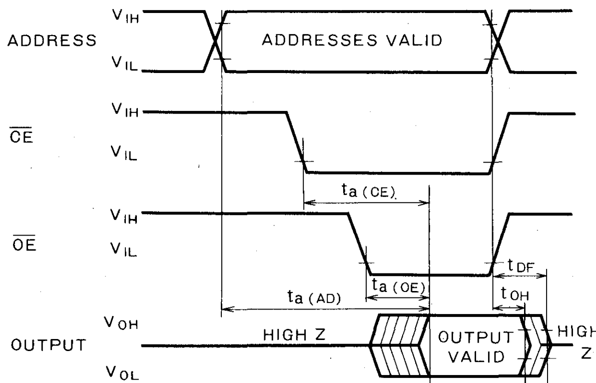
D. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	$V_{IN}=5.25V$			10	μA
I_{LO}	Output leakage current	$V_{OUT}=5.25V$			10	μA
I_{PP1}	V_{PP} current read	$V_{PP}=5.25V$			15	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			35	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}=V_{IL}$			100	mA
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{IH}	High-level input voltage		2.0		$V_{CC}+1$	V
V_{OL}	Low-level output voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	High-level output voltage	$I_{OH}=-400\mu A$	2.4			V

A. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	M5L2764K-2		M5L2764K		Unit
			Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$		200		250	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$		200		250	ns
$t_{a(OE)}$	Output enable to output delay	$\overline{CE}=V_{IL}$	10	70	10	100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0	60	0	90	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0		0		ns

AC WAVEFORMS



Test Conditions for A.C. Characteristics
Input Voltage: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
Input Rise and Fall Times: ≦ 20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output Load: 1 TTL gate, $C_L = 100pF$

CAPACITANCE ($T_a = 25°C$, f = 1 MHz)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN}= 0 V$		4	6	pF
C_{OUT}	Output capacitance	$V_{OUT}= 0 V$		8	12	pF

PROGRAM OPERATION

CONVENTIONAL PROGRAMMING ALGORITHM ($Ta=25\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=21\pm0.5V$ unless otherwise noted)

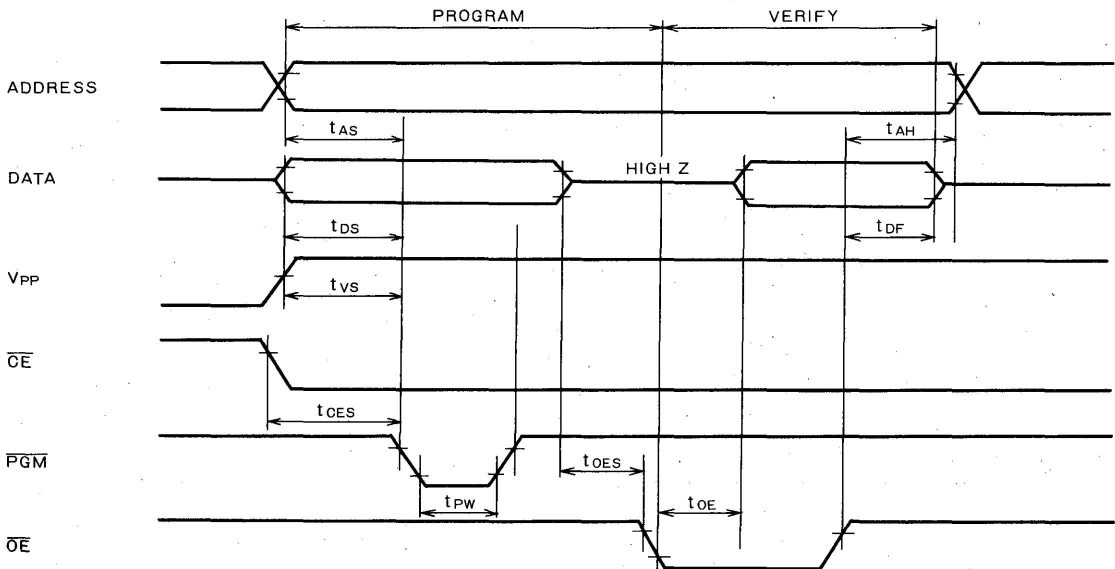
D. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Low-level output voltage (verify)	$I_{OL}=2.1mA$			0.45	V
V_{OH}	High-level output voltage (verify)	$I_{OH}=-400\mu A$	2.4			V
I_{CC2}	V_{CC} supply current (active)				100	mA
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{IH}	High-level input voltage		2.0		$V_{CC}+1$	V
I_{PP}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

A. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		20			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ pulse width (programming)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test Conditions for AC Characteristics
Input Voltage: V_{IL} = 0.8V, V_{IH} = 2.2V
Input Rise and Fall Times: ≦ 20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V
Outputs 0.8V and 2V

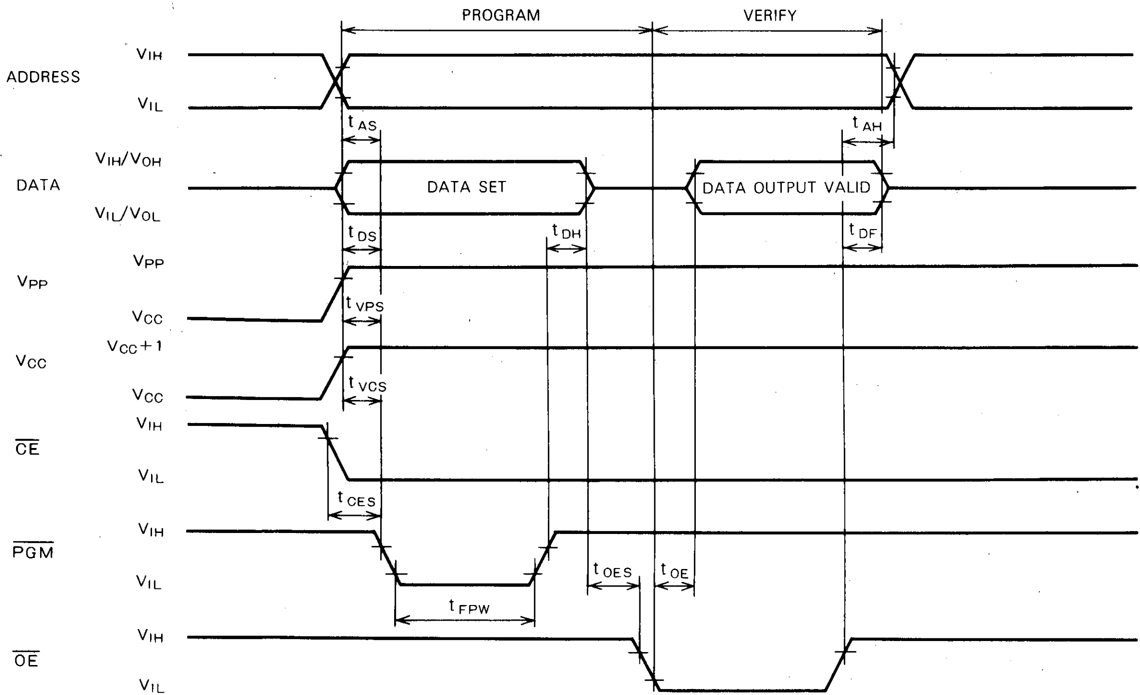
FAST PROGRAMMING ALGORITHM
DC CHARACTERISTICS
($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS
($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

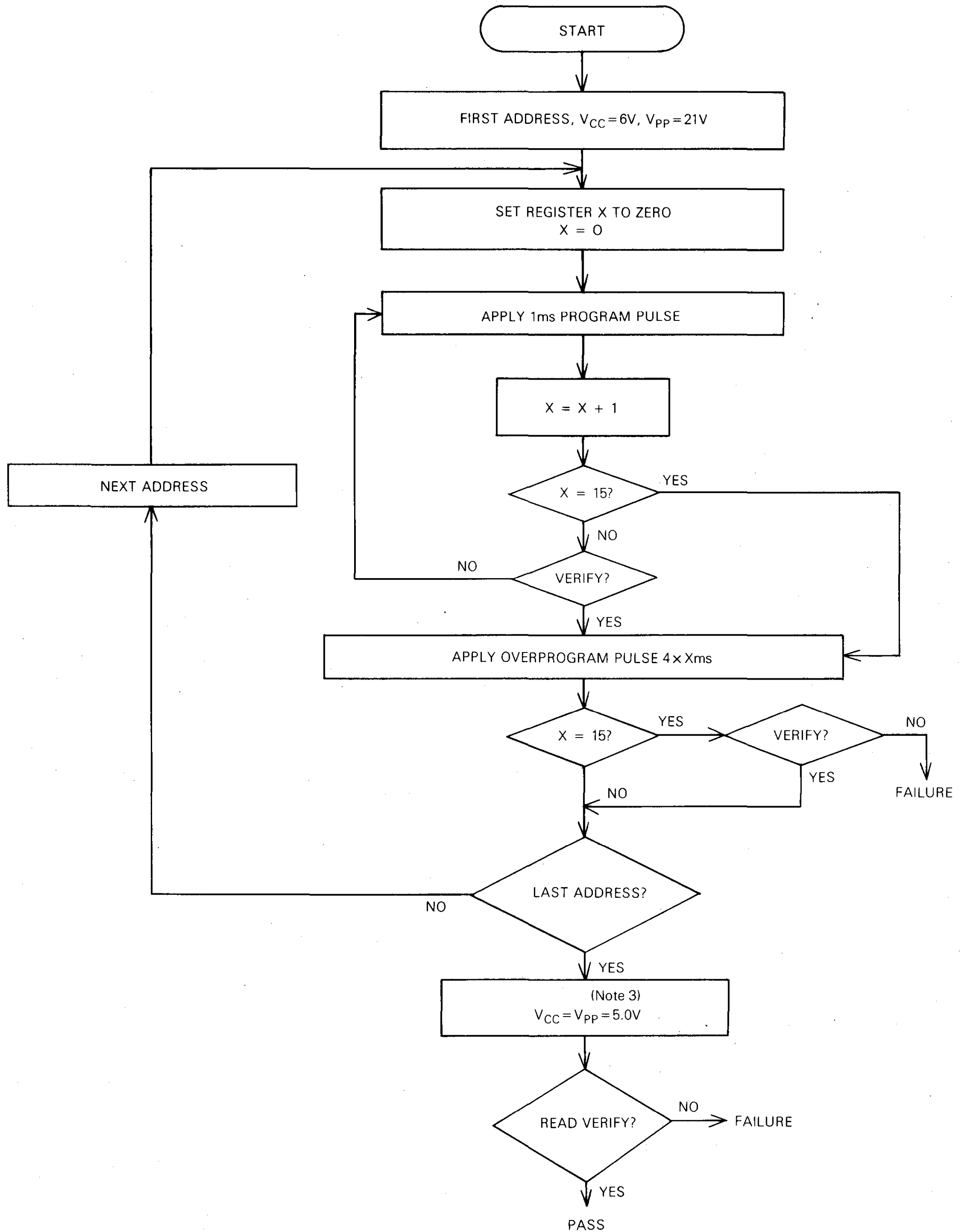
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		20			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



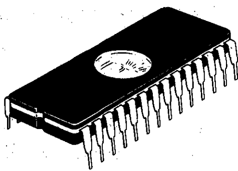
Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Input rise and fall times: $\leqq 20ns$
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

FAST PROGRAMMING ALGORITHM FLOW CHART



Note 3: $4.75 \leq V_{CC} = V_{PP} \leq 5.25V$

M5L27128K, -25, -2, -20



131072-BIT(16384-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5L27128K is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27128K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

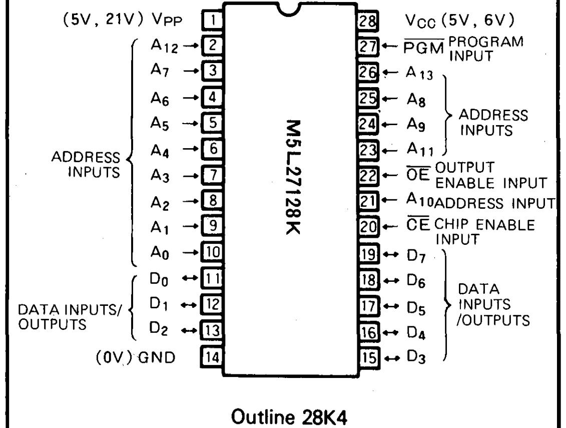
FEATURES

- 16384 words x 8-bit organization
- Access time M5L27128K-2, -20 ...... 200ns (max.)
  M5L27128K, -25 .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active .... 100mA (max.)
  Standby .... 40mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with INTEL 27128
- ±10% V_{CC} Tolerance (Read mode): M5L27128K-25, -20

APPLICATION

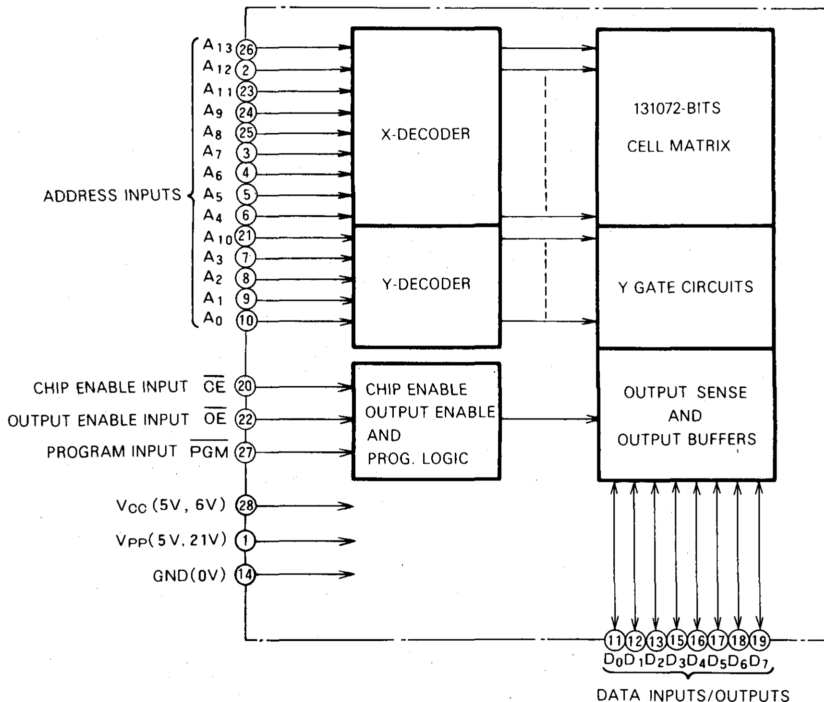
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

131072-BIT(16384-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming

(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6)

(Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the V_{PP} power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leq t_{PW} \leq$ 55 ms.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and flüorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10~80	°C
T_{stg}	Storage temperature	−65~125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~26.5	V
V_{I3}	A9 (Note 2)	−0.6~13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{PP} = V_{CC}, unless otherwise noted)
(V_{CC} = 5V ± 10%: M5L27128K-25, -20, V_{CC} = 5V ± 5%: M5L27128K, -2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			10	μA
I_{PP1}	V_{PP} current read	V_{PP} = 5.5V			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}$ = V_{IH}			40	mA
I_{CC2}	V_{CC} current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			100	mA
V_{IL}	Input low voltage		0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			V

Note 3: Typical values are at T_a = 25°C and nominal supply voltages.

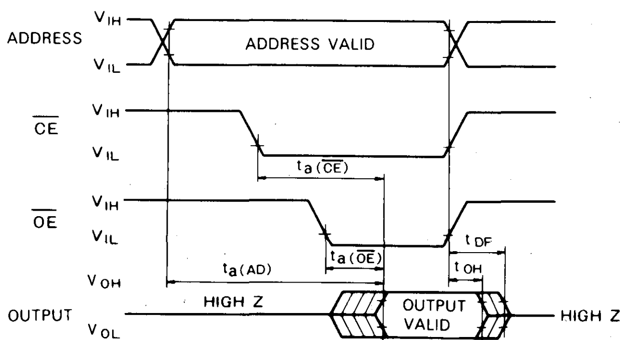
AC ELECTRICAL CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{PP} = V_{CC}, unless otherwise noted)
(V_{CC} = 5V ± 10%: M5L27128K-25, -20, V_{CC} = 5V ± 5%: M5L27128K, -2)

Symbol	Parameter	Test conditions	Limits				Unit
			M5L27128K-2 M5L27128K-20		M5L27128K M5L27128K-25		
			Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250	ns
$t_{a(\overline{CE})}$	Chip enable to output delay	$\overline{OE}$ = V_{IL}		200		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}$ = V_{IL}		75		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}$ = V_{IL}	0	60	0	85	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

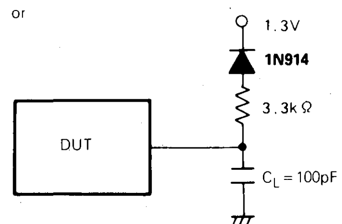
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	T_a = 25°C, f = 1MHz, V_I = V_O = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS

(Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V, unless otherwise noted)

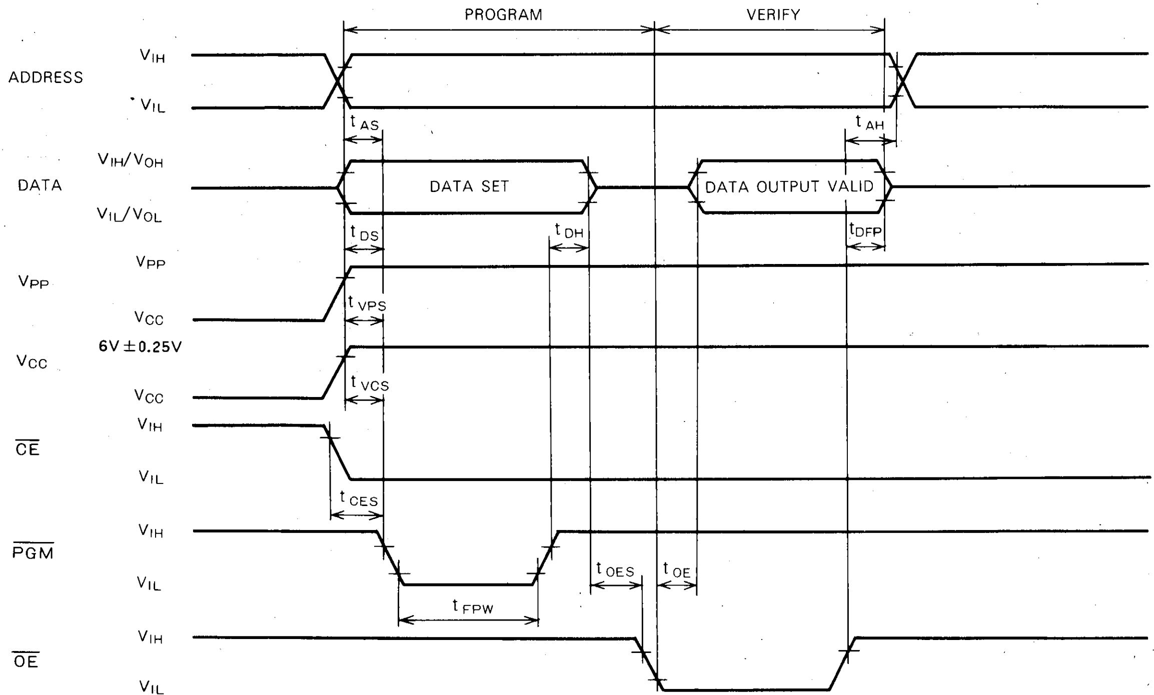
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			35	mA

AC ELECTRICAL CHARACTERISTICS

(Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

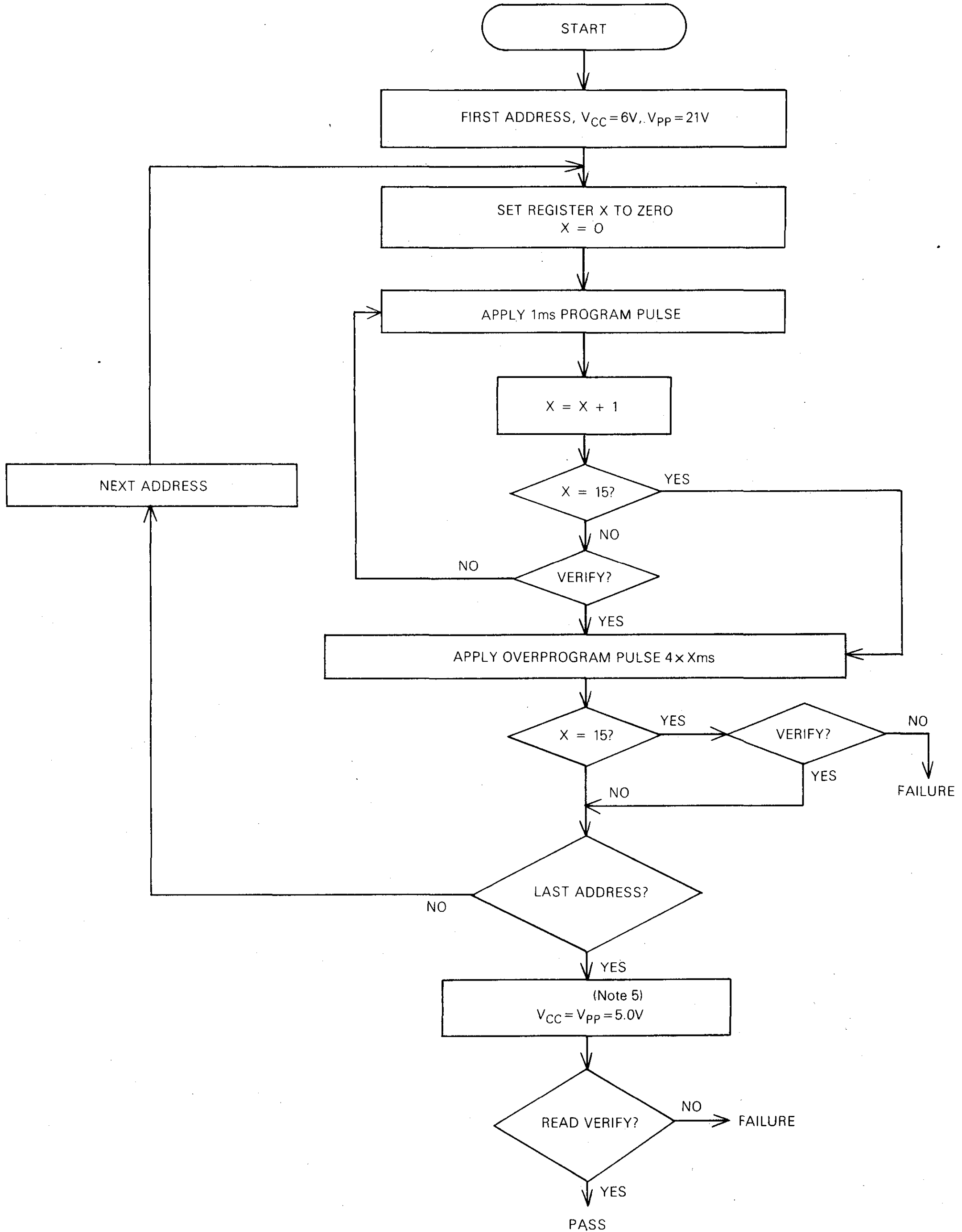
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times: $\leqq 20ns$
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

MITSUBISHI ELECTRIC

FAST PROGRAMMING ALGORITHM FLOW CHART



Note 5: $4.75V \leqq V_{CC} = V_{PP} \leqq 5.25V$: M5L27128K, -2
$4.5V \leqq V_{CC} = V_{PP} \leqq 5.5V$: M5L27128K-25, -20

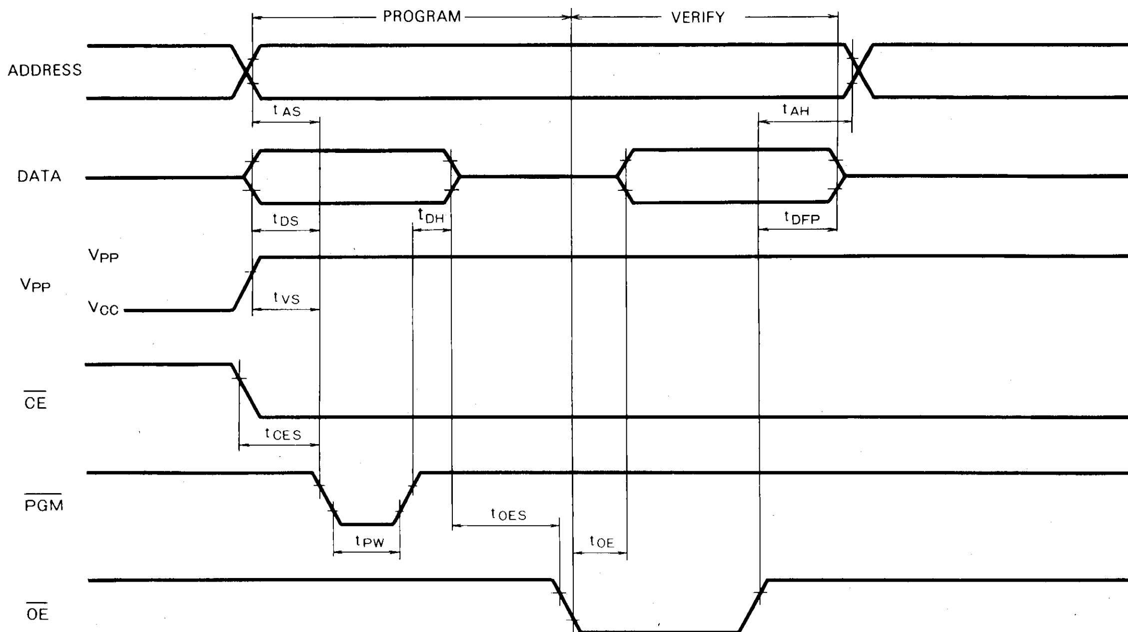
CONVENTIONAL PROGRAMMING ALGORITHM
DC ELECTRICAL CHARACTERISTICS
($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			35	mA

AC ELECTRICAL CHARACTERISTICS
($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ Pulse width (during program)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

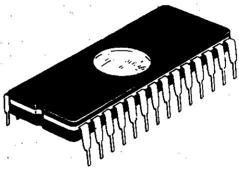
AC WAVEFORMS



Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Reference voltage at timing measurement: Input 1V and 2V
Outputs 0.8V and 2V

M5L27128K-I

131072-BIT(16384-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5L27128K-I is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27128K-I is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

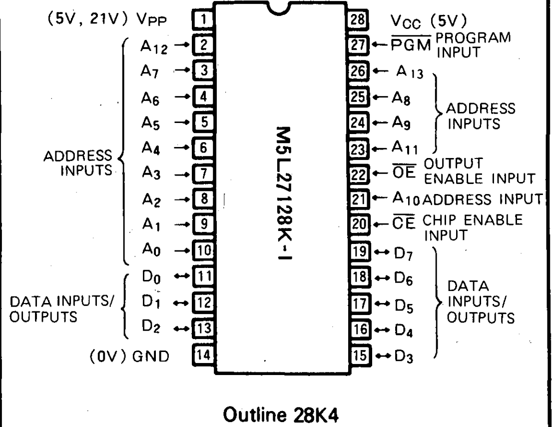
FEATURES

- 16384 word x 8 bit organization
- Access time
  M5L27128K-I .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}):
  Active .... 120mA (max.)
  Standby .... 50mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Wide temperature range: −40°C ~ +85°C

APPLICATION

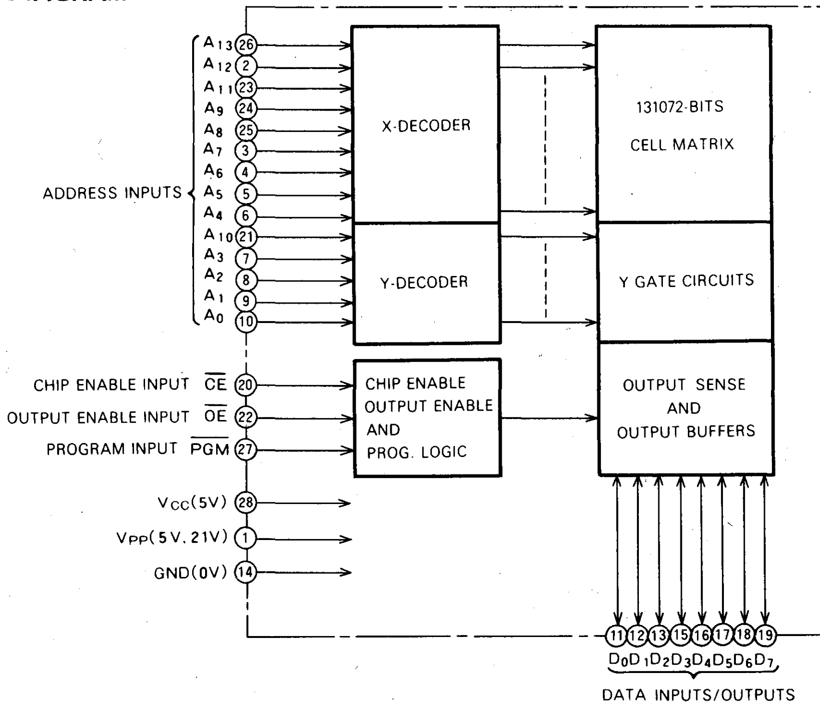
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data content of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming
(Fast programming algorithm)

First set V_{CC} = 6V, V_{PP} = 21V and then set an address to the first address to be programmed. After applying 1ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address are not verified correctly, apply one more 1ms program pulse. The programmer continues 1ms pulse-then-verify routines until the device verifies correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also keeps the total number of 1ms pulses applied to that address in register X. It then applies a program pulse 4 times as long as the value of register X as an overprogram pulse. When the above programming procedure is finished, step to the next address and repeat this procedure till the last address to be programmed.

(Conventional programming algorithm)

The device enters the programming mode when 21V are supplied to the V_{PP} power supply input and $\overline{CE}$ is at a low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition $45ms \leqq t_{PW} \leqq 55ms$.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
Topr	Operating temperature	−50~95	°C
Tstg	Storage temperature	−65~125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~26.5	V
V_{I3}	A_9 (Note 2)	−0.6~13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated is not recommended. Exposure to absolute maximum rating conditions for extended periods affects device reliability.
2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS ($Ta = -40°C \sim +85°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	$V_{IN} = 5.25V$			10	μA
I_{LO}	Output leakage current	$V_{OUT} = 5.25V$			10	μA
I_{PP1}	V_{PP} current read	$V_{PP} = 5.25V$			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE} = V_{IH}$			50	mA
I_{CC2}	V_{CC} current active	$\overline{CE} = \overline{OE} = V_{IL}$			120	mA
V_{IL}	Input low voltage		0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V

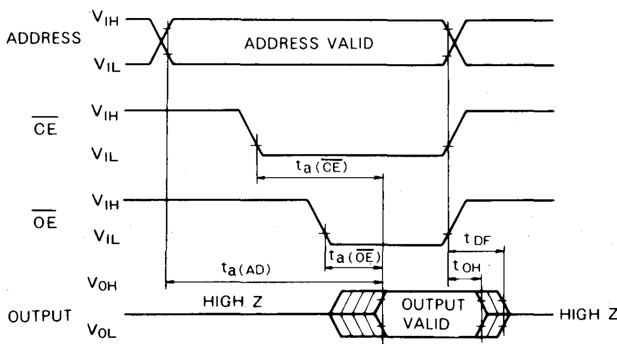
Note 3: Typical values are at $Ta = 25°C$ and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS ($Ta = -40°C \sim +85°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE} = V_{IL}$		100	ns
t_{DF}	Output enable high to output float	$\overline{CE} = V_{IL}$	0	85	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE} = \overline{OE} = V_{IL}$	0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

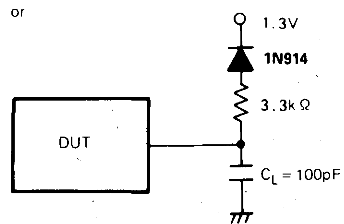
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	$Ta = 25°C$, $f = 1MHz$, $V_I = V_O = 0V$		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

MITSUBISHI ELECTRIC

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 21V ± 0.5V, unless otherwise noted)

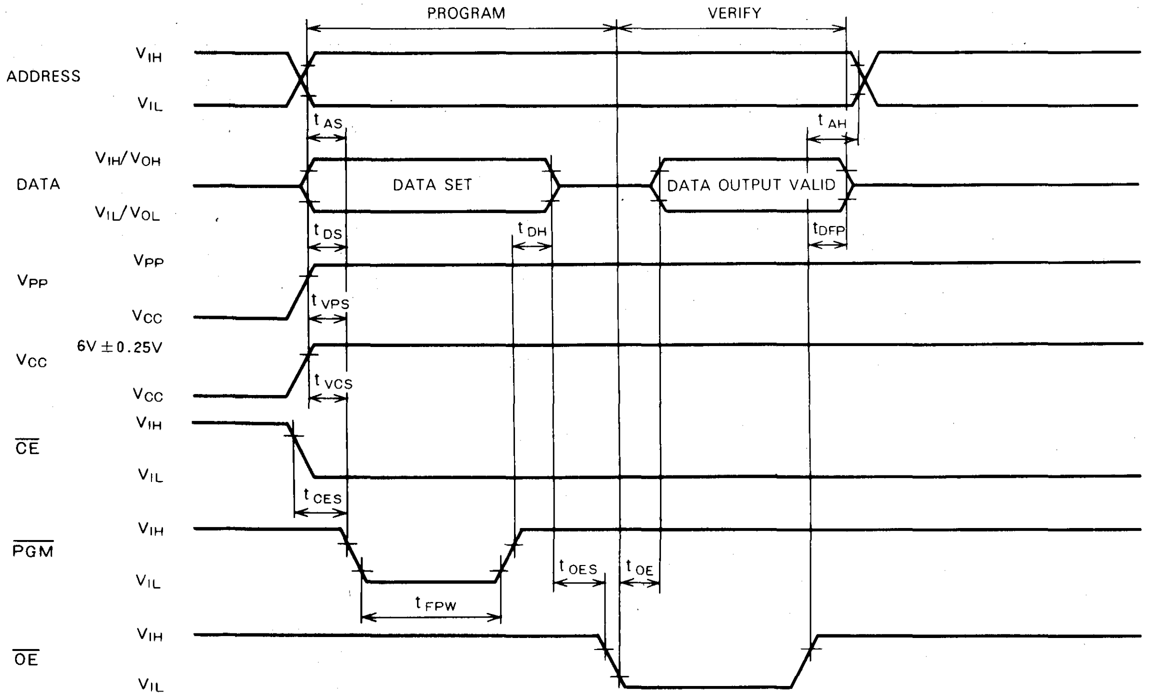
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400μA$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			35	mA

AC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 21V ± 0.5V, unless otherwise noted)

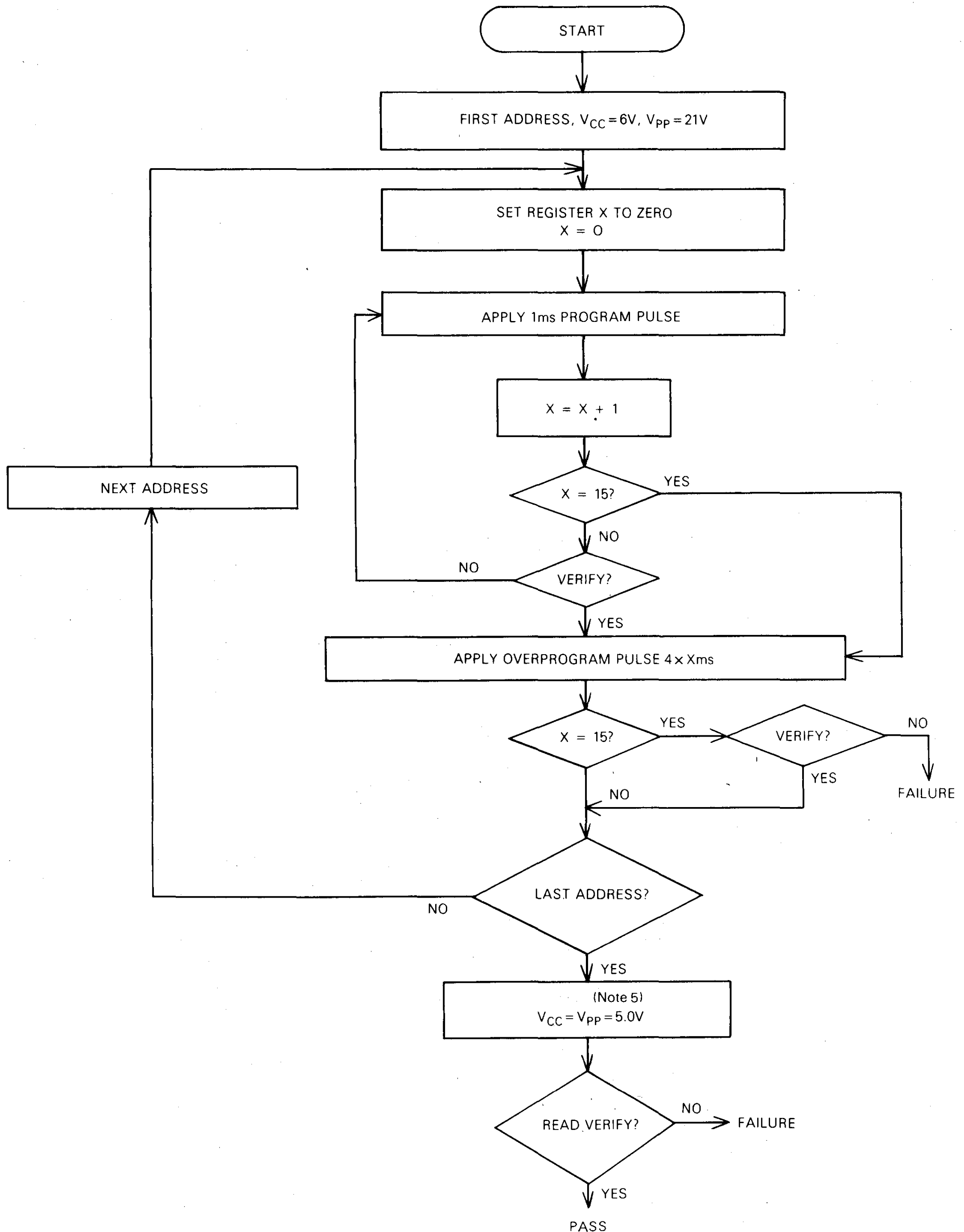
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

FAST PROGRAMMING ALGORITHM FLOW CHART



Note 5: $4.75 \leqq V_{CC} = V_{PP} \leqq 5.25V$

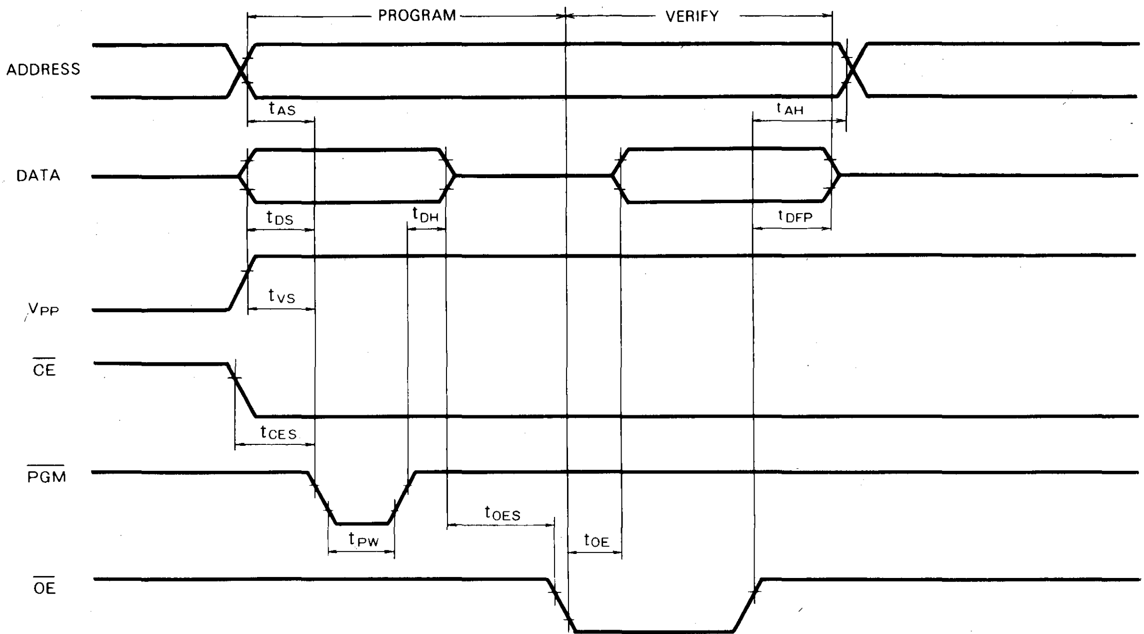
CONVENTIONAL PROGRAMMING ALGORITHM
DC CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			35	mA

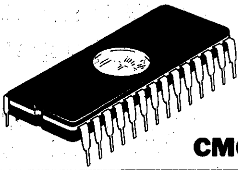
AC CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ Pulse width (during program)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Reference voltage at timing measurement: Input 1V and 2V
Outputs 0.8V and 2V



M5M27C128K, -15, -2

131072-BIT(16384-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

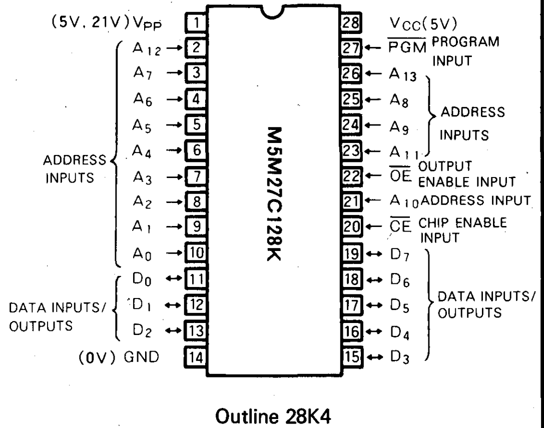
DESCRIPTION

The Mitsubishi M5M27C128K, -15, -2 is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C128K is fabricated by N-channel double polysilicon gate Memory and CMOS technology for peripheral circuits, and available in a 28 pin DIP with a transparent lid.

FEATURES

- 16384 words x 8 bit organization
- Access time M5M27C128K-15 .... 150ns (max.)
  M5M27C128K-2 ....200ns (max.)
  M5M27C128K .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 30mA (max.)
  Standby .... 1mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with M5L27128K

PIN CONFIGURATION (TOP VIEW)

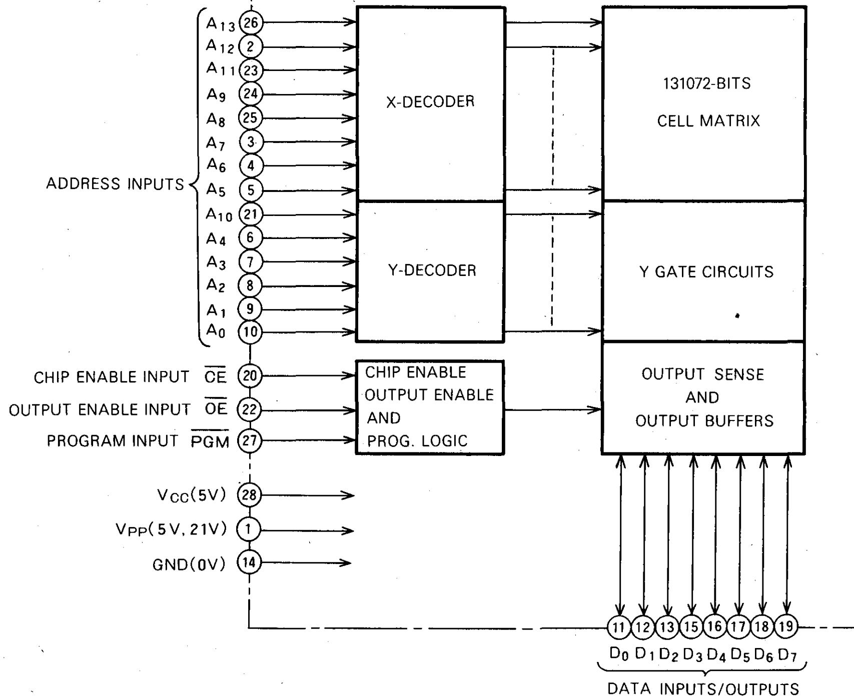


Outline 28K4

APPLICATION

Microcomputer systems and peripheral equipment

BLOCK DIAGRAM



131072-BIT(16384-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level).

Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming

(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6)

(Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the V_{PP} power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms$\leqq t_{PW} \leqq$55 ms.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11~ 13, 15~ 19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~22.0	V
Topr	Operating temperature	−10~80	°C
Tstg	Storage temperature	−65~125	°C

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	($V_{PP}=V_{CC}$)			V
GND	Supply voltage		0		V
V_{IL}	Low-level input voltage	−0.1		0.8	V
V_{IH}	High-level input voltage	2.0		$V_{CC}+1$	V

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, $V_{PP}=V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN}=5.25V			10	μA
I_{LO}	Output leakage current	V_{OUT}=5.25V			10	μA
I_{PP1}	V_{PP} current read or standby	V_{PP}=5.25V		1	100	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			1	mA
		$\overline{CE}=V_{CC}$		1	100	μA
I_{CC2}	V_{CC} current Active	$\overline{CE}=\overline{OE}=V_{IL}$			30	mA
		f=4MHz			30	
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

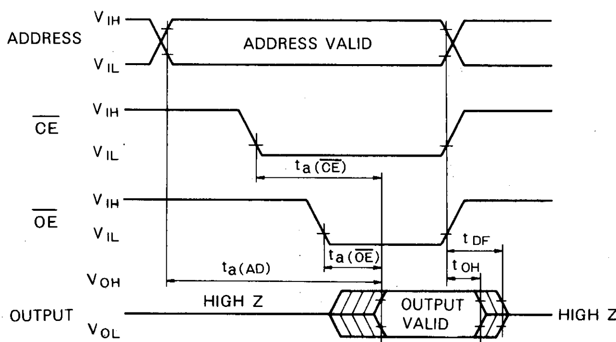
Note 3: Typical values are at Ta=25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, $V_{PP}=V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5M27C128K-15		M5M27C128K-2		M5M27C128K		
			Min	Max	Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$		150		200		250	ns
$t_{a(\overline{CE})}$	CE to output delay	$\overline{OE}=V_{IL}$		150		200		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}=V_{IL}$		75		75		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0	60	0	60	0	85	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0		0		0		ns

Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

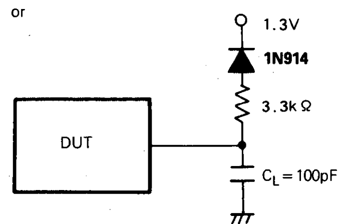
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL}=0.45V, V_{IH}=2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate+C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	T_a=25°C, f=1MHz, $V_I=V_O$=0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V, unless otherwise noted)

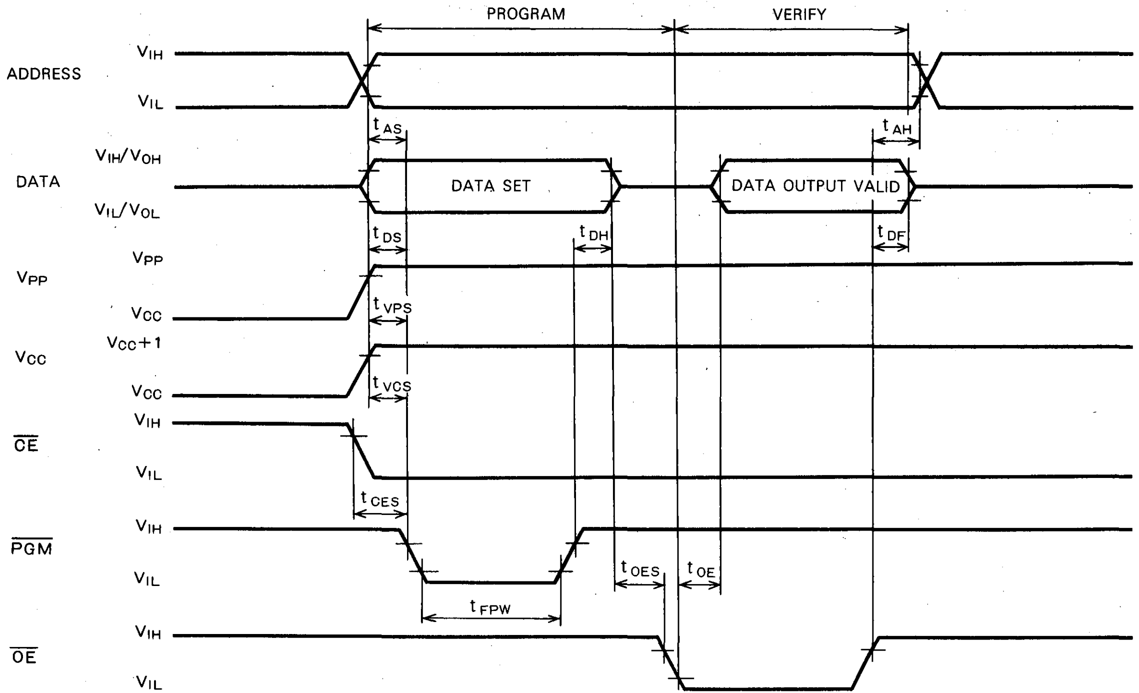
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				30	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

AC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V, unless otherwise noted)

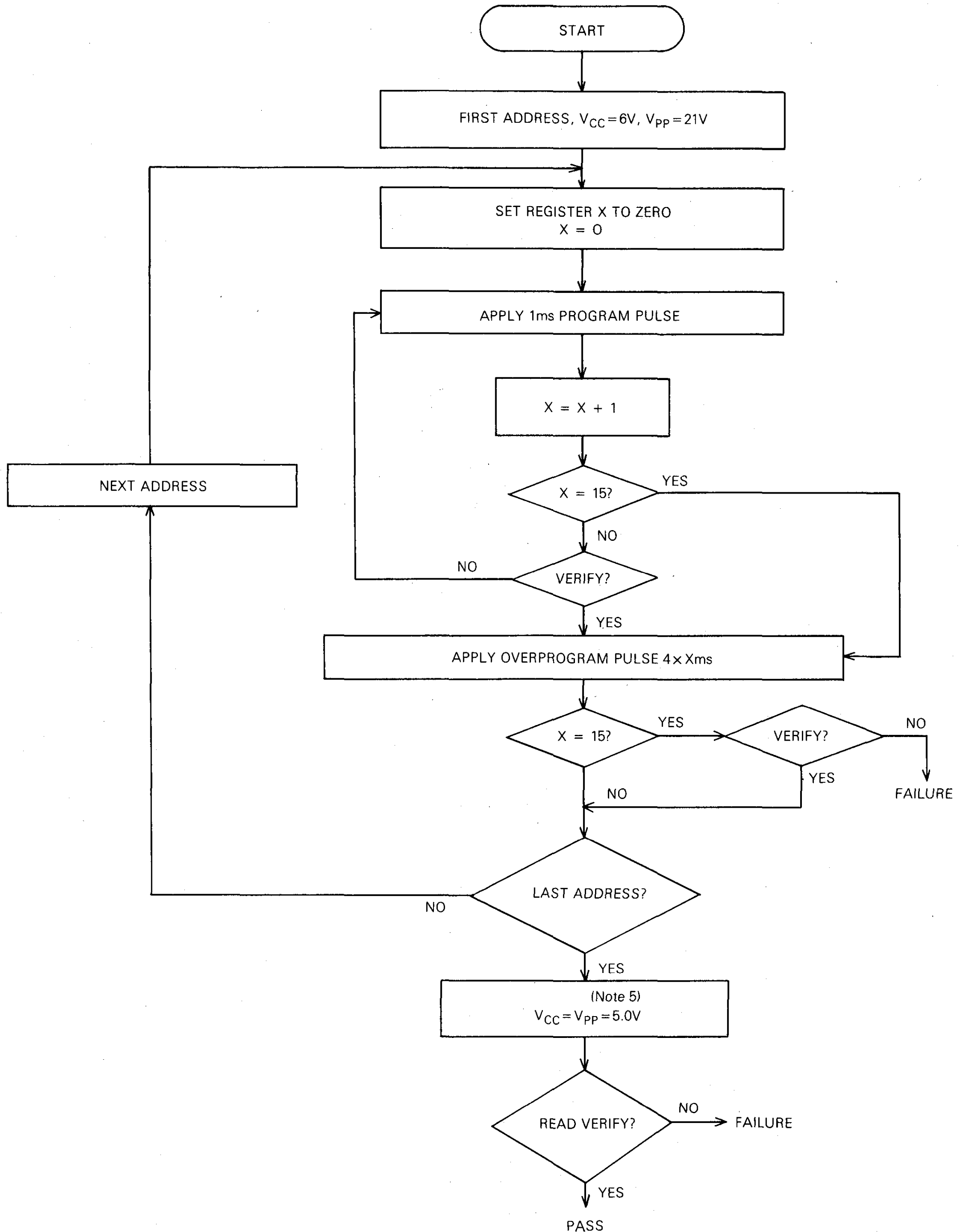
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

FAST PROGRAMMING ALGORITHM FLOW CHART



Note 5: $4.75 \leq V_{CC} = V_{PP} \leq 5.25V$

CONVENTIONAL PROGRAMMING ALGORITHM

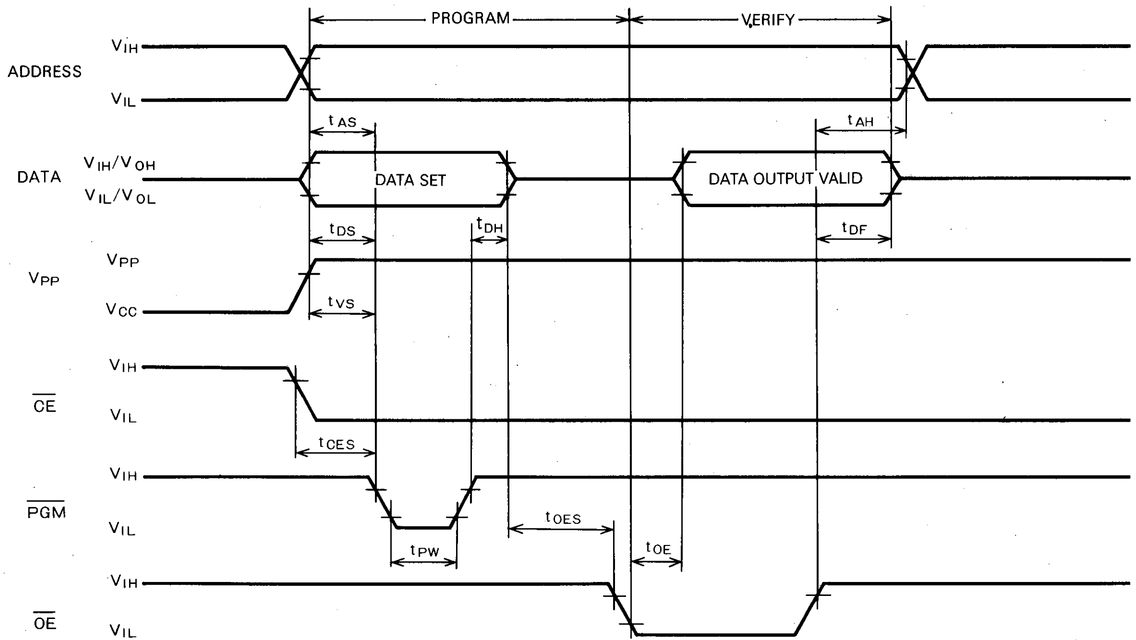
DC ELECTRICAL CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
I_{CC}	V_{CC} Supply current				30	mA
I_{PP2}	V_{PP} Supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

AC ELECTRICAL CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V, unless otherwise noted)

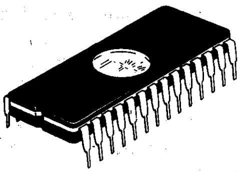
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address set up time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ Pulse width (during program)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Reference voltage at timing measurement: Input 1V and 2V
Outputs 0.8V and 2V

M5L27256K, -15, -2



262144-BIT (32768-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5L27256K is a high-speed 262144-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27256K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

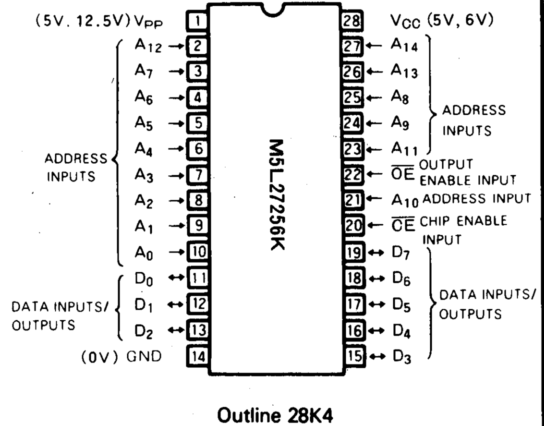
FEATURES

- 32768 Word x 8 bit organization
- Access time M5L27256K-15 .... 150ns (max.)
  M5L27256K-2 .... 200ns (max.)
  M5L27256K .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 80mA (max.)
  Standby .... 25mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with INTEL 27256

APPLICATION

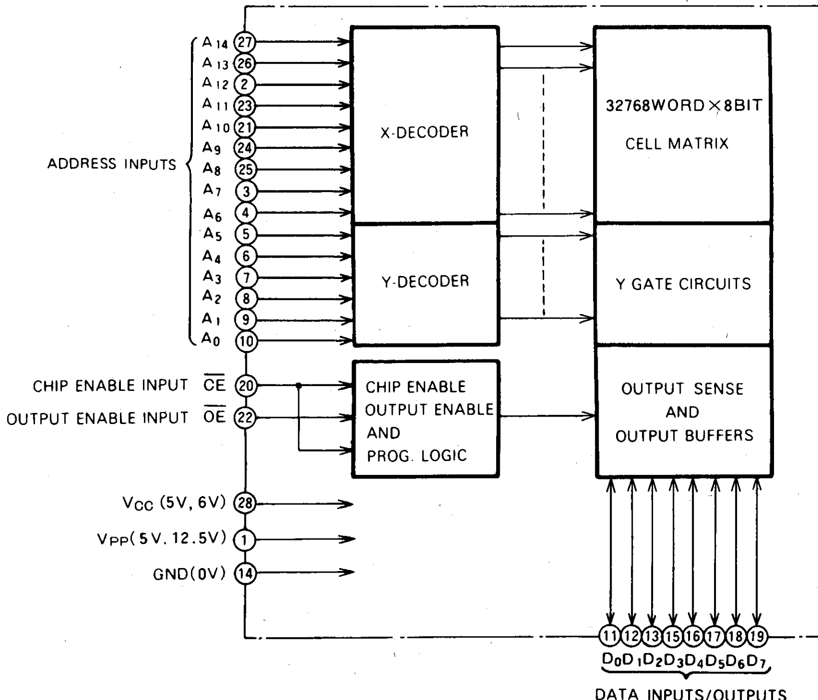
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



262144-BIT (32768-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming
(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=12.5V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	V_{PP}(1)	V_{CC}(28)	Outputs (11～13, 15～19)
Read	V_{IL}	V_{IL}	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Standby	V_{IH}	X*	5V	5V	Floating
Program	V_{IL}	V_{IH}	12.5V	6V	Data in
Program verify	V_{IH}	V_{IL}	12.5V	6V	Data out
Program inhibit	V_{IH}	V_{IH}	12.5V	6V	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10～80	°C
T_{stg}	Storage temperature	−65～125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6～7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6～14.0	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			10	μA
I_{PP1}	V_{PP} current read	V_{PP} = 5.5V			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}$ = V_{IH}			25	mA
I_{CC2}	V_{CC} current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			80	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.4			V

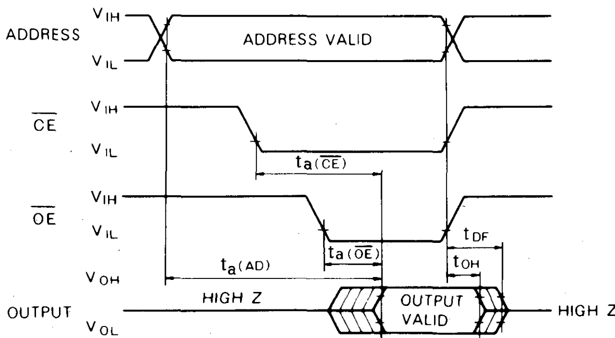
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5L27256K-15		M5L27256K-2		M5L27256K		
			Min	Max	Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		150		200		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}$ = V_{IL}		150		200		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}$ = V_{IL}		60		75		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}$ = V_{IL}	0	50	0	60	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

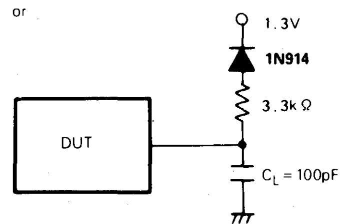
AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≤ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	Ta = 25°C, f = 1MHz, V_I = V_O = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($T_a=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

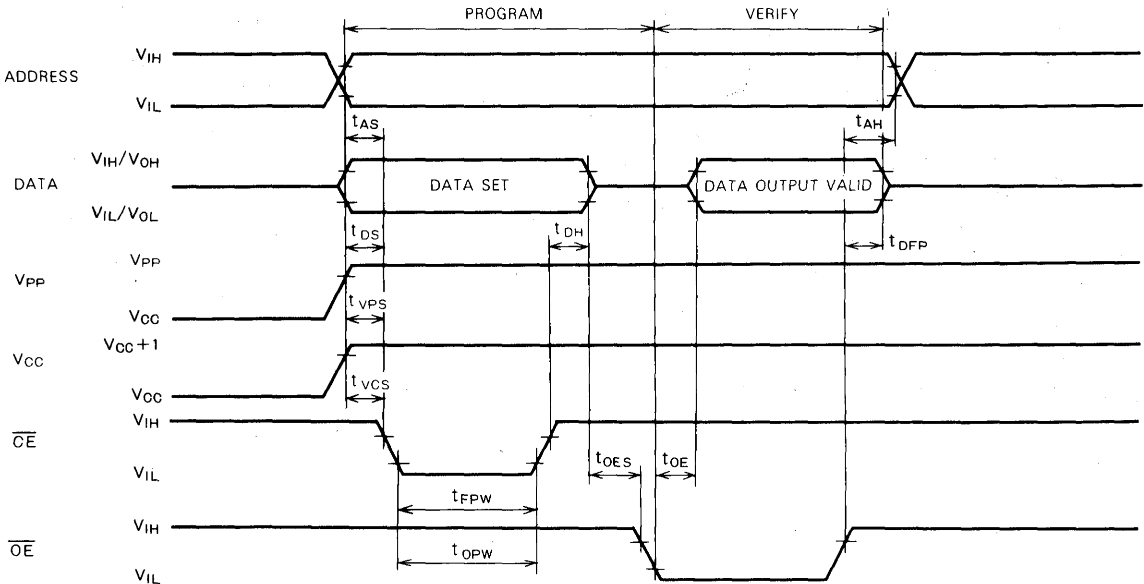
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				80	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}$			50	mA

AC ELECTRICAL CHARACTERISTICS ($T_a=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

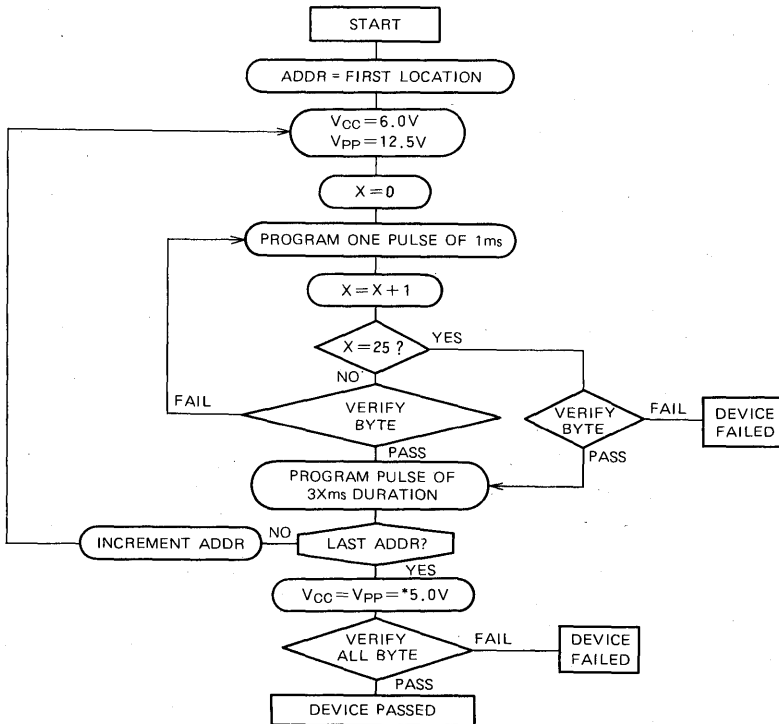
Note 5: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* $4.75V \leqq V_{CC} = V_{PP} \leqq 5.25V$

DEVICE IDENTIFIER MODE

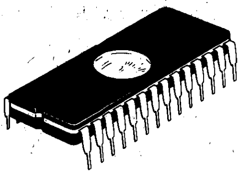
The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5L27256K DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	0	1	0	0	04

Note: $A_9 = 12.0 \pm 0.5V$, $A_1 \sim A_8$, $A_{10} \sim A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$.



M5L27256K-I

262144-BIT (32768-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5L27256K-I is a high-speed 262144-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27256K-I is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

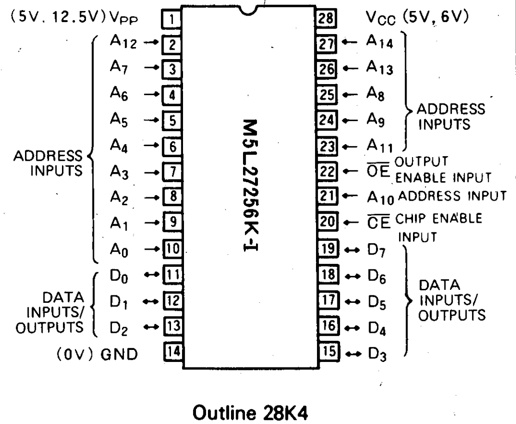
FEATURES

- 32768 word x 8 bit organization
- Access time M5L27256K-I .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}):
  - Active .... 80mA (max.)
  - Standby .... 30mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP package
- Fast programming algorithm
- Wide temperature range: -40°C ~ +85°C

APPLICATION

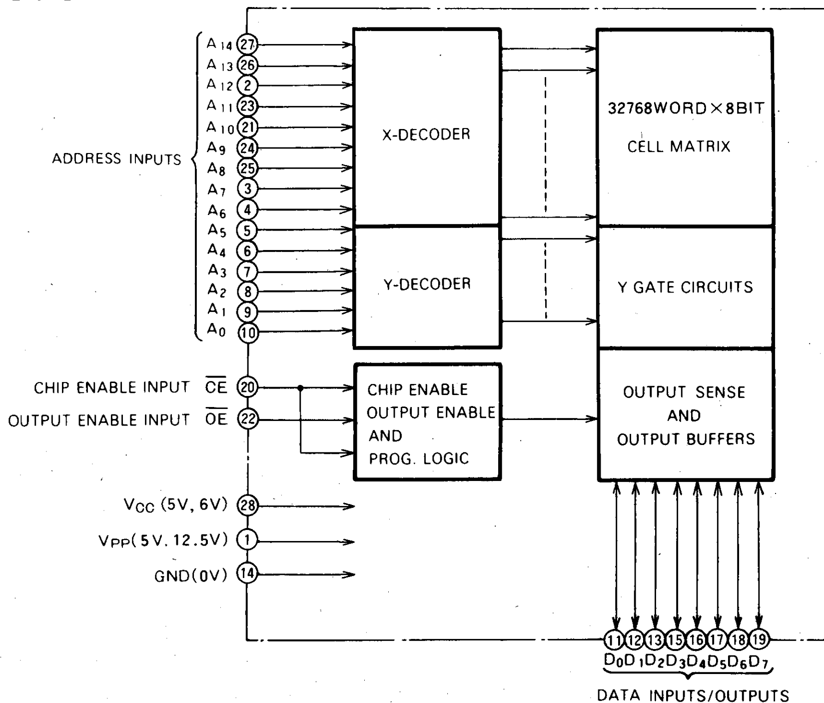
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming
(Fast programming algorithm)

First set $V_{CC} = 6V, V_{PP} = 12.5V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Standby	V_{IH}	X*	5V	5V	Floating
Program	V_{IL}	V_{IH}	12.5V	6V	Data in
Program verify	V_{IH}	V_{IL}	12.5V	6V	Data out
Program inhibit	V_{IH}	V_{IH}	12.5V	6V	Floating

*: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
Topr	Operating temperature	−50~95	°C
Tstg	Storage temperature	−65~125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~14.0	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

262144-BIT (32768-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = −40~85°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unlesee otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{L1}	Input load current	V_{IN} = 5.5V			10	μA
I_{OL}	Output leakage current	V_{OUT} = 5.5V			10	μA
I_{PP1}	V_{PP} current read	V_{PP} = 5.5V			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}$ = V_{IH}			30	mA
I_{CC2}	V_{CC} current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			80	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output low voltage	I_{LO} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.4			V

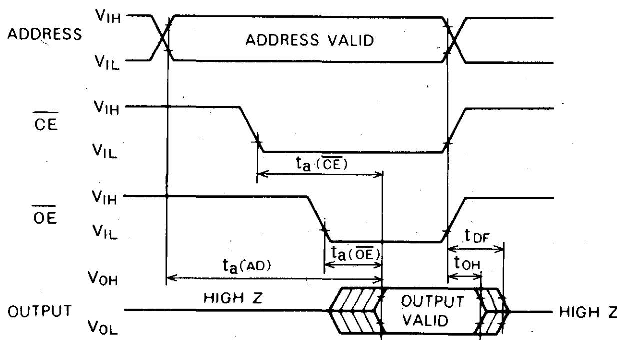
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = −40~85°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}$ = V_{IL}		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}$ = V_{IL}		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}$ = V_{IL}	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

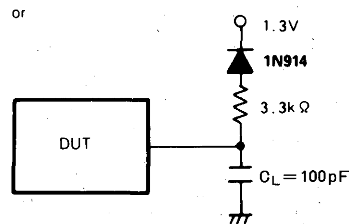
AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	Ta = 25°C, f = 1MHz, V_I = V_O = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

MITSUBISHI ELECTRIC

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

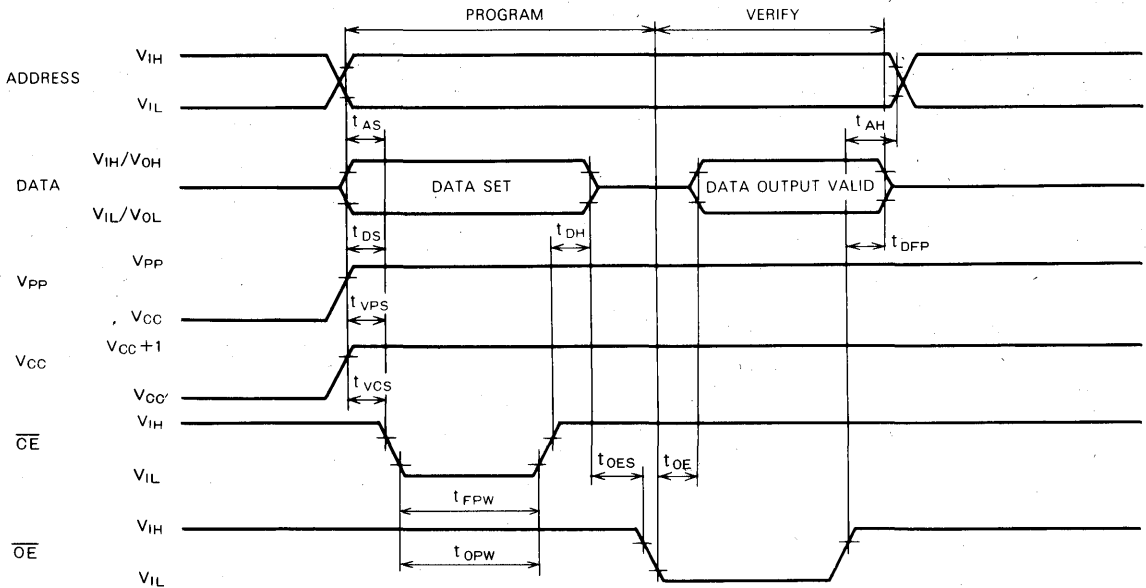
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				80	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}$			50	mA

AC ELECTRICAL CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

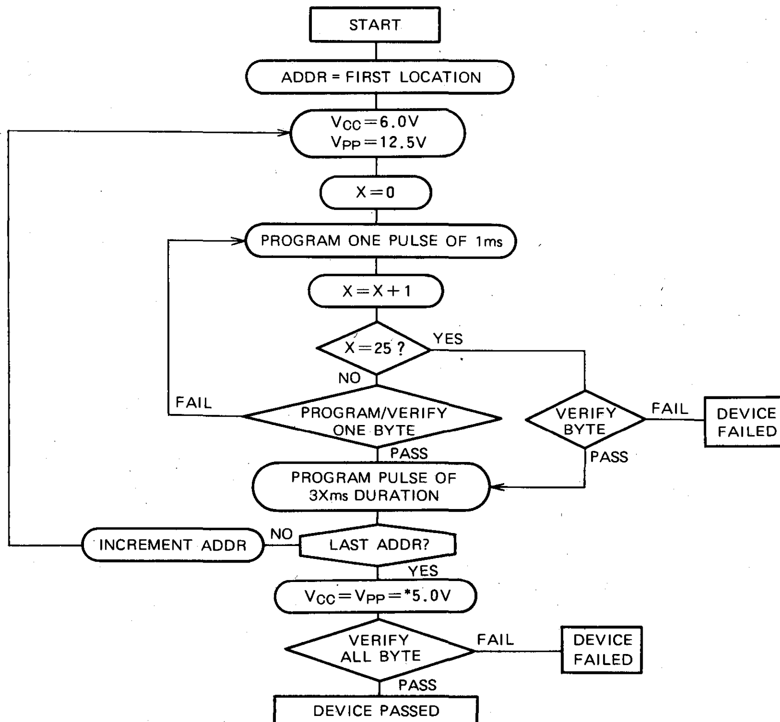
Note 5: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* 4.75V≦V_{CC}=V_{PP}≦5.25V

DEVICE IDENTIFIER MODE

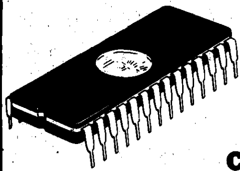
The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5L27256K-I DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	0	1	0	0	04

Note 6: $A_9=12.0\pm0.5V$, $A_1 \sim A_8$, $A_{10} \sim A_{14}$, $\overline{CE}$, $\overline{OE}=V_{IL}$.



M5M27C256K, -12, -15

262144-BIT (32768-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C256K is a high-speed 262144-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C256K is fabricated by N-channel double polisilicon gate memory and CMOS technology for peripheral circuits, and is available in a 28-pin DIP with a transparent lid.

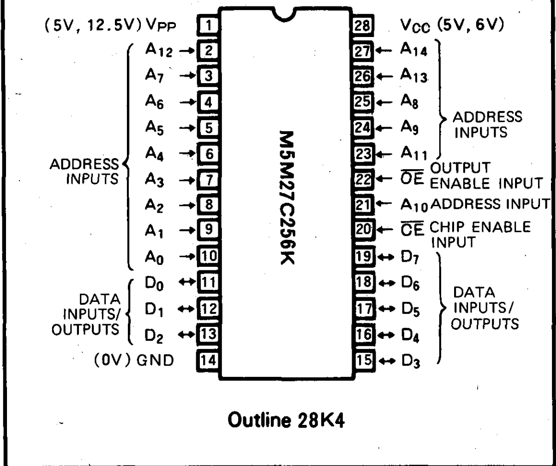
FEATURES

- 32768 word x 8 bit organization
- Access time M5M27C256K-12 .... 120ns (max.)
  M5M27C256K-15 .... 150ns (max.)
  M5M27C256K .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 30mA (max.)
  Standby ..... 1mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with M5L27256K

APPLICATION

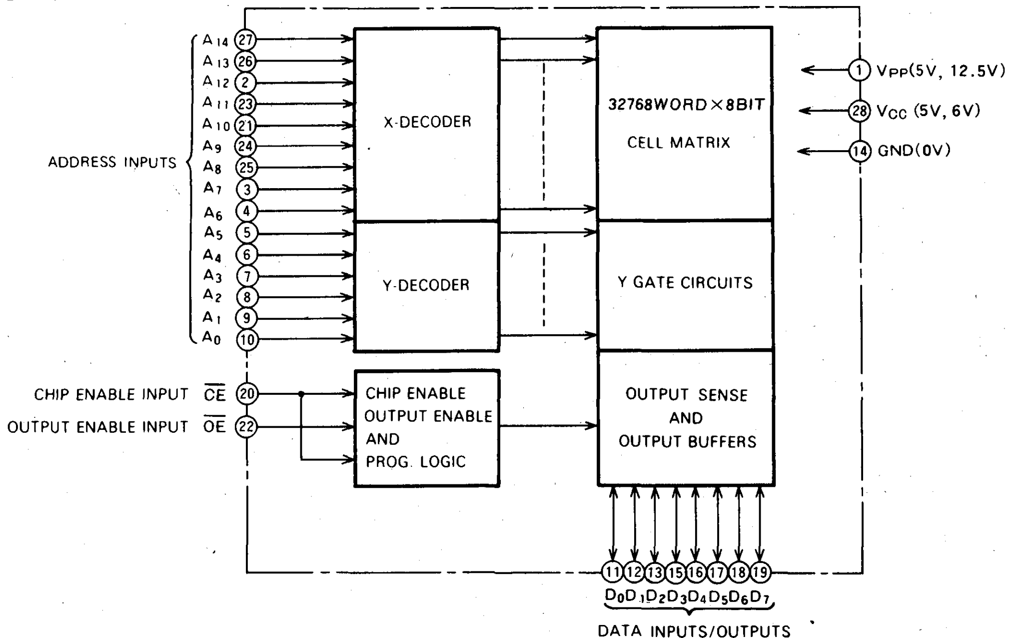
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

262144-BIT (32768-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming
(Fast programming algorithm)

First set V_{CC} = 6V, V_{PP} = 12.5V and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Standby	V_{IH}	X*	5V	5V	Floating
Program	V_{IL}	V_{IH}	12.5V	6V	Data in
Program verify	V_{IH}	V_{IL}	12.5V	6V	Data out
Program inhibit	V_{IH}	V_{IH}	12.5V	6V	Floating

* : X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10~80	°C
T_{stg}	Storage temperature	−65~125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~14.0	V

Note 1: *Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.*

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{L1}	Input load current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			10	μA
I_{PP1}	V_{PP} current read	V_{PP} = 5.5V		1	100	μA
I_{CC1}	V_{CC} current standby	$\overline{CE} = V_{IH}$			1	mA
		$\overline{CE} = V_{CC}$		1	100	μA
I_{CC2}	V_{CC} current active	$\overline{CE} = \overline{OE} = V_{IL}$			30	mA
		f = 4MHz			30	
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			V

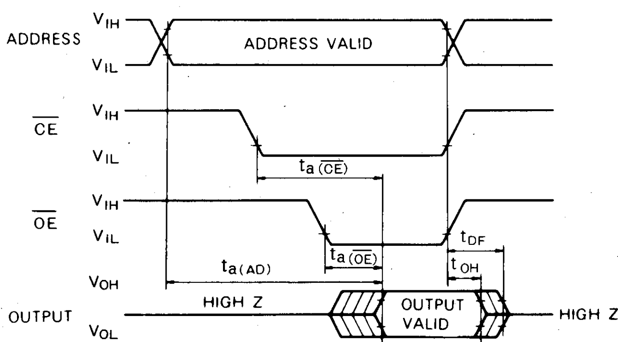
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5M27C256K-12		M5M27C256K-15		M5M27C256K		
			Min	Max	Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		120		150		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE} = V_{IL}$		60		75		100	ns
t_{DF}	Output enable high to output float	$\overline{CE} = V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

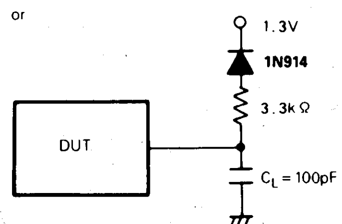
AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	Ta = 25°C, f = 1MHz, $V_I = V_O$ = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

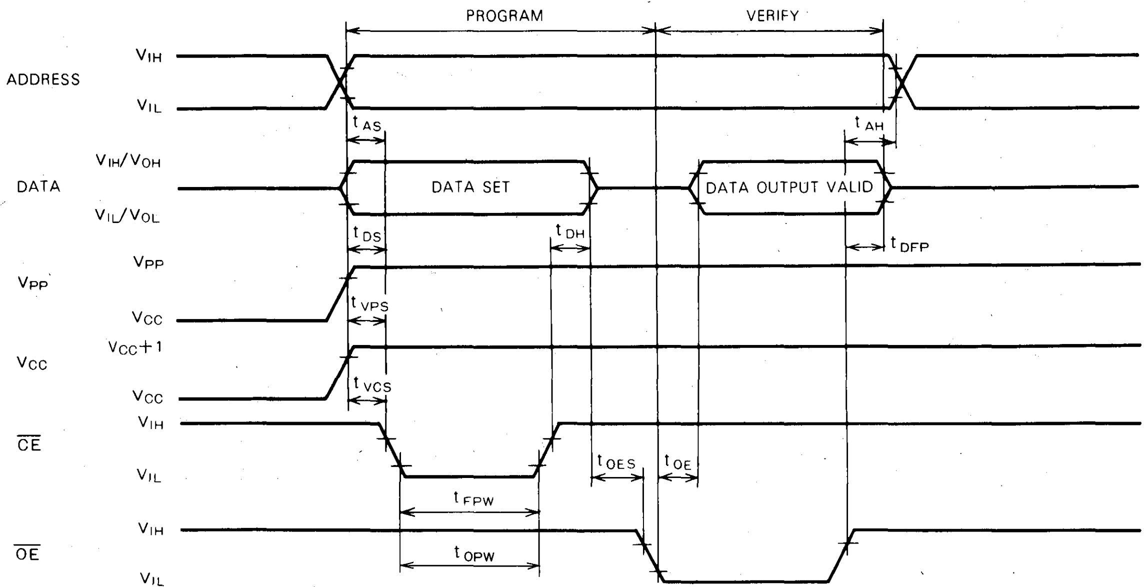
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				30	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}$			30	mA

AC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

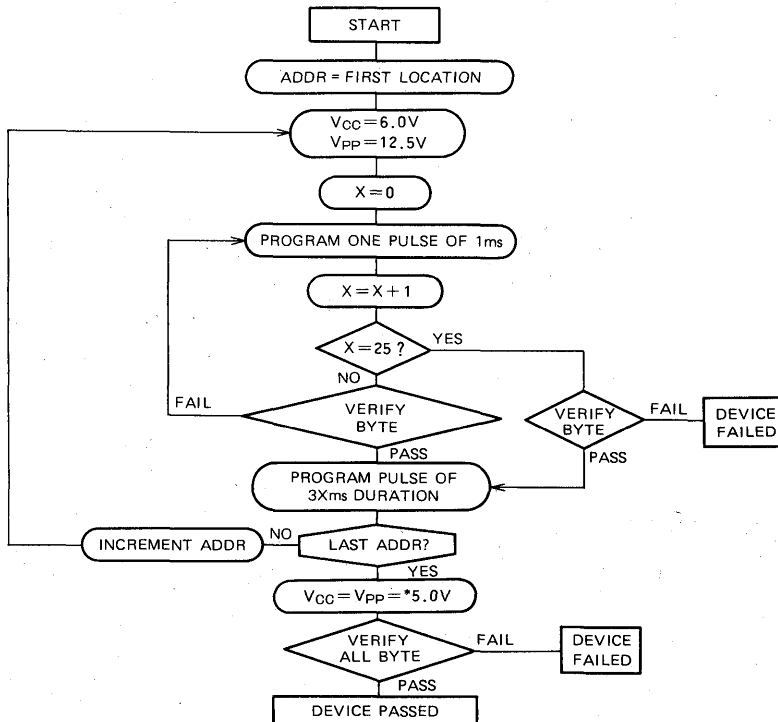
Note 5: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* $4.75V \leqq V_{CC} = V_{PP} \leqq 5.25V$

DEVICE IDENTIFIER MODE

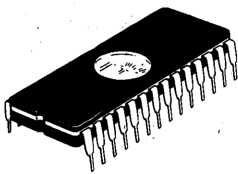
The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C256K DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	0	0	0	1	01

Note: $A_9 = 12.0 \pm 0.5V$, $A_1 \sim A_8$, $A_{10} \sim A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$.



M5L27512K, -17, -2

524288-BIT (65536-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5L27512K is a high-speed 524288 bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27512K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

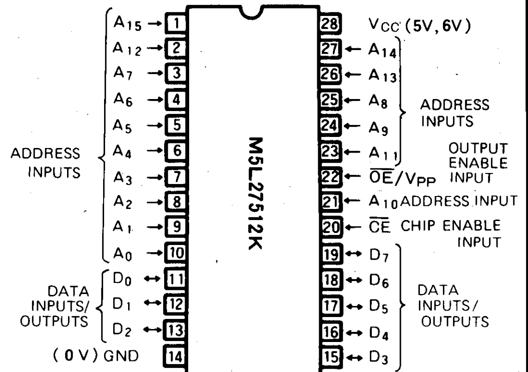
FEATURES

- 65536 Word x 8 bit organization
- Access time M5L27512K-17 .... 170ns (max.)
  M5L27512K-2 .... 200ns (max.)
  M5L27512K .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Lower power current (I_{CC}): Active .. 100mA (max.)
  Standby .. 40mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with INTEL 27512

APPLICATION

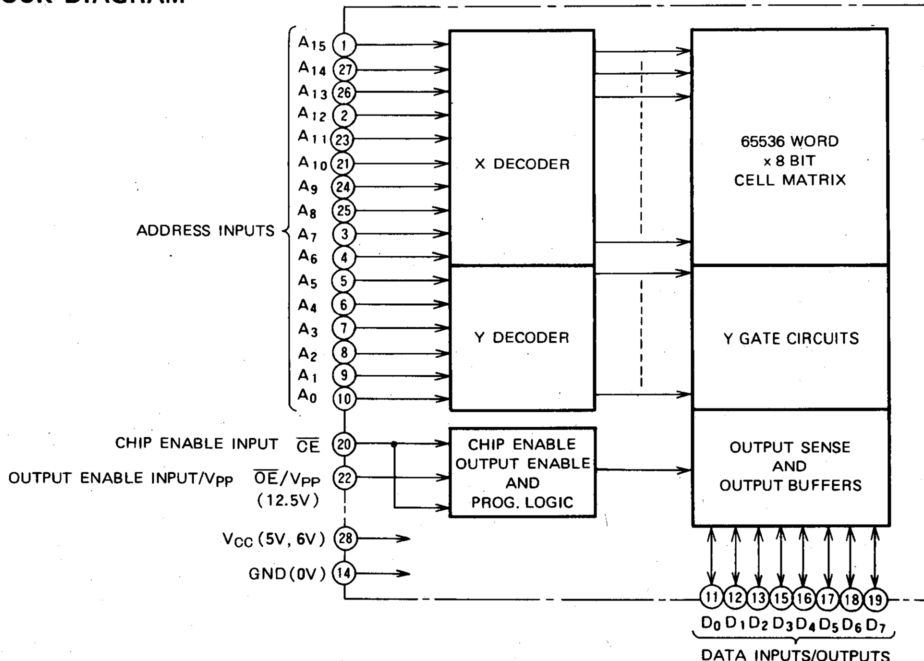
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



**524288-BIT (65536-WORD BY 8-BIT)
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}/V_{PP}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}/V_{PP}$ and address signals to the address inputs ($A_0 \sim A_{15}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}/V_{PP}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signals is high, the device is in the standby mode or power-down mode.

Programming (Fast programming algorithm)

First set V_{CC} = 6V, $\overline{OE}/V_{PP}$ = 12.5V and then set an address to first address to be programmed. After applying 1ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1ms program pulse. The programmer continues 1ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}/V_{PP}$(22)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	5 V	Data out
Output disable	V_{IL}	V_{IH}	5 V	Floating
Standby	V_{IH}	X*	5 V	Floating
Program	V_{IL}	12.5V	6 V	Data in
Program inhibit	V_{IH}	12.5V	6 V	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	− 10 ~ 80	°C
T_{stg}	Storage temperature	− 65 ~ 125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7.0	V
V_{I2}	$\overline{OE}/V_{PP}$ supply voltage (Note 2)	−0.6~14.0	V
V_{I3}	A9 input voltage (Note 2)	−0.6~13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, unless otherwise noted)

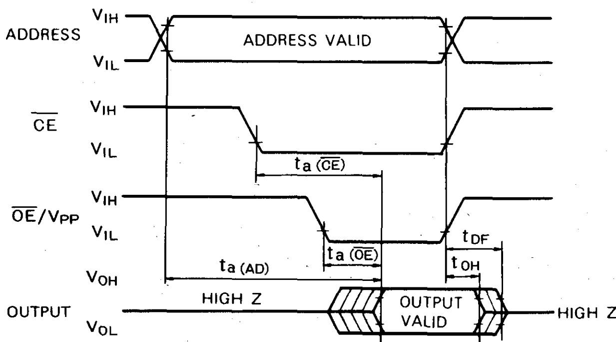
Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{L1}	Input leakage current	V_{IN}=5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V			10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			40	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$			100	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

Note 3: Typical values are at T_a = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	M5L27512K-17 Min	M5L27512K-17 Max	M5L27512K-2 Min	M5L27512K-2 Max	M5L27512K Min	M5L27512K Max	Unit
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$		170		200		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}/V_{PP}=V_{IL}$		170		200		250	ns
$t_{a(\overline{OE})}$	$\overline{OE}$ to output delay	$\overline{CE}=V_{IL}$		60		75		100	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE}=V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$	0		0		0		ns

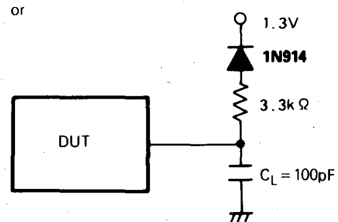
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_{IN}	Input capacitance	T_a=25°C, f= 1MHz, $V_I=V_O$=0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	$\overline{OE}$/Vpp supply current	$\overline{CE}=V_{IL}$			50	mA

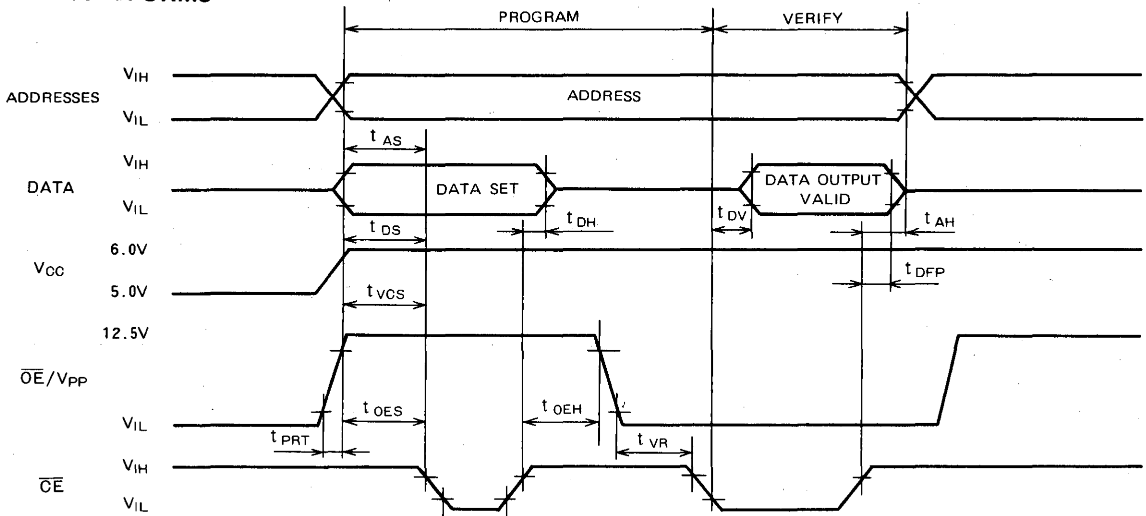
AC ELECTRICAL CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V, unlesee otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$/Vpp setup time		2			μs
t_{OEH}	$\overline{OE}$/Vpp hold time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{CE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{DV}	Data valid from $\overline{CE}$				1	μs
t_{VR}	$\overline{OE}$/Vpp recovery time		2			μs
t_{PRT}	$\overline{OE}$/Vpp pulse rise time during program		50			ns

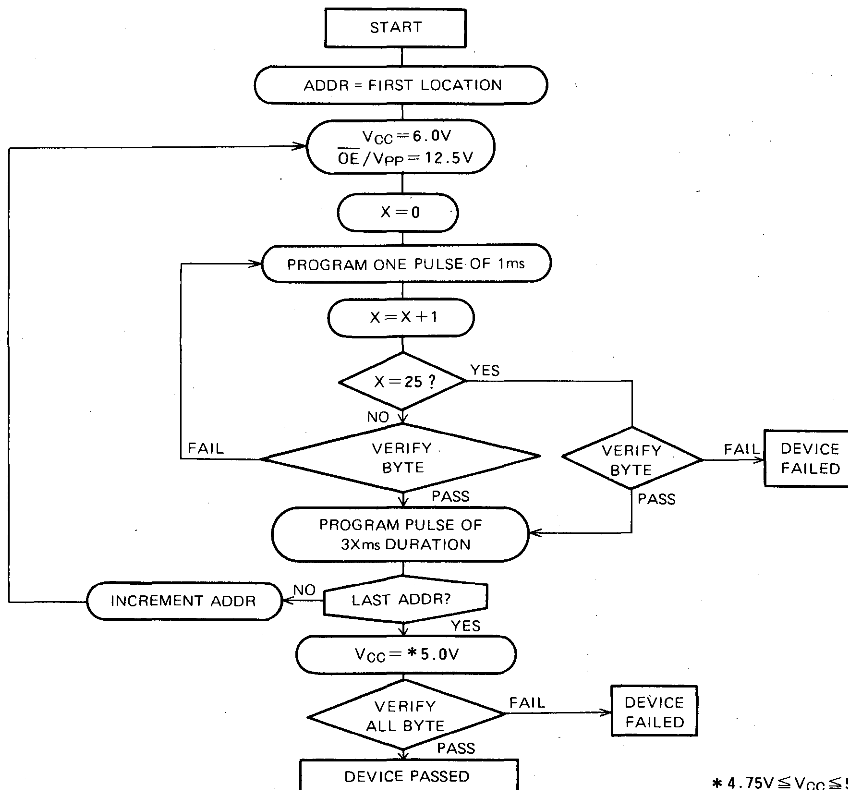
Note 4: V_{CC} must be applied simultaneously or before $\overline{OE}$/Vpp and removed simultaneously or after $\overline{OE}$/Vpp.

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* 4.75V ≦ V_{CC} ≦ 5.25V

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5L27512K DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	1	1	0	1	0D

Note 5: $V_{CC}=5V\pm5\%$, $A_9 = 12.0\pm0.5V$, $A_1 \sim A_8$, $A_{10} \sim A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$

M5M27C100K, -15, -2

1048576-BIT (131072-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

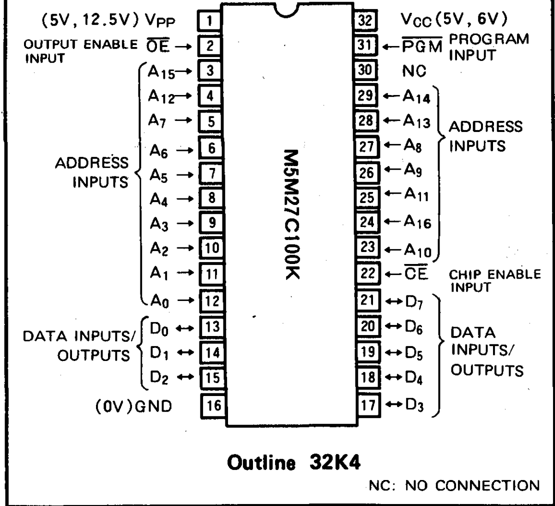
DESCRIPTION

The Mitsubishi M5M27C100K is a high-speed 1048576-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C100K is fabricated by N-channel double polisilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 32 pin DIP with a transparent lid.

FEATURES

- 131072 word x 8 bit organization
- Access time M5M27C100K-15 .... 150ns (max.)
  M5M27C100K-2 .... 200ns (max.)
  M5M27C100K .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 50mA (max.)
  Standby ..... 1mA (max.)
- Single 5V power supply
- Programming voltage 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Pin compatible with 1Mbit MASK ROM
- Fast programming algorithm

PIN CONFIGURATION (TOP VIEW)



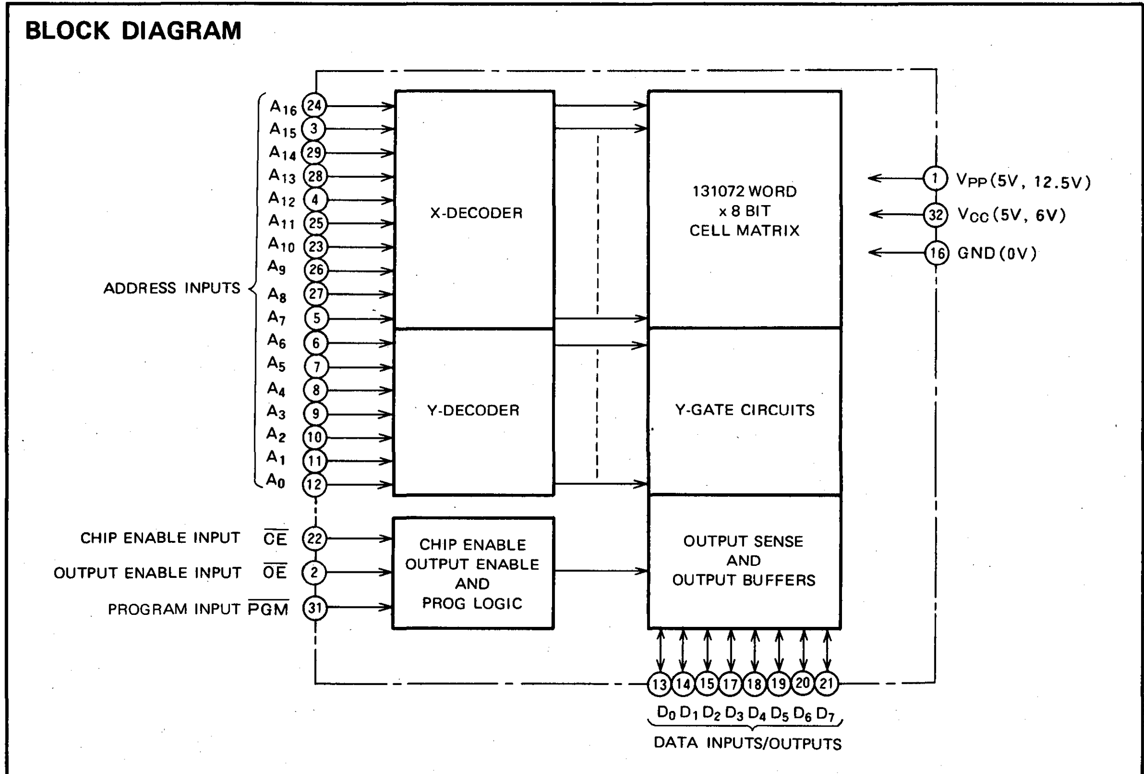
Outline 32K4

NC: NO CONNECTION

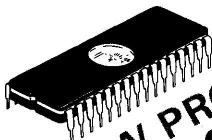
APPLICATION

Microcomputer systems and peripheral equipment

BLOCK DIAGRAM



M5M27C101K, -15, -2



1048576-BIT (131072-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

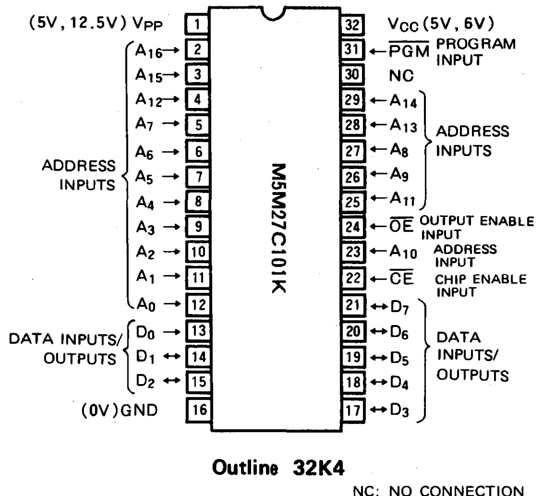
DESCRIPTION

The Mitsubishi M5M27C101K is a high-speed 1048576-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C101K is fabricated by N-channel double polisilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 32 pin DIP with a transparent lid.

FEATURES

- 131072 word x 8 bit organization
- Access time M5M27C101K-15 .... 150ns (max.)
  M5M27C101K-2 .... 200ns (max.)
  M5M27C101K .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 50mA (max.)
  Standby ..... 1mA (max.)
- Single 5V power supply
- Programming voltage 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 32 pin DIP
- Fast programming algorithm

PIN CONFIGURATION (TOP VIEW)



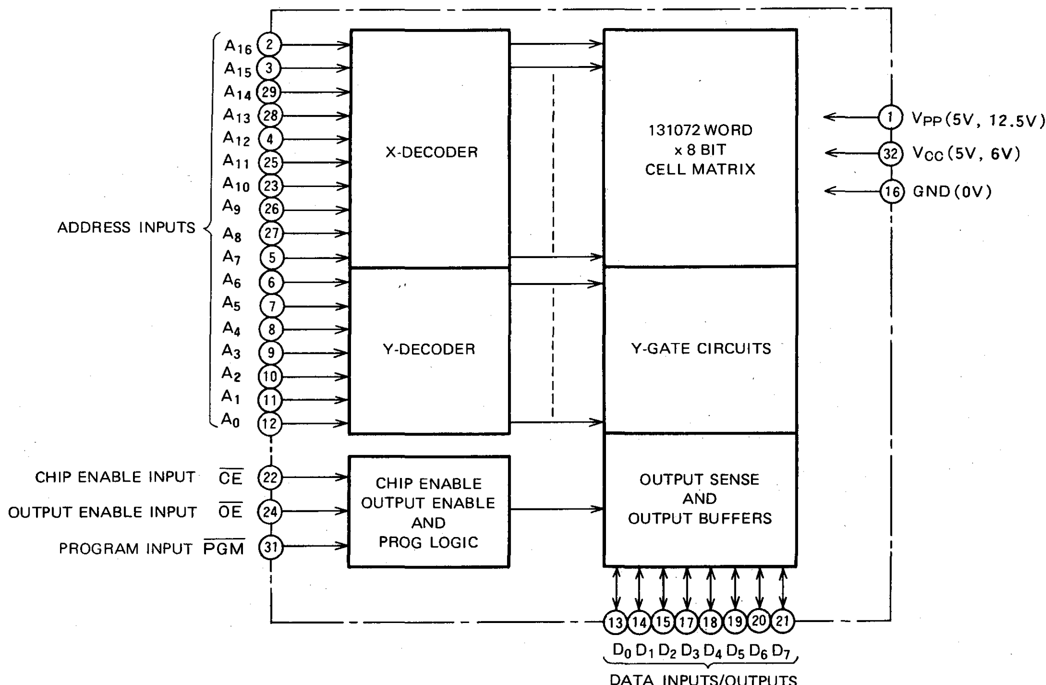
Outline 32K4

NC: NO CONNECTION

APPLICATION

Microcomputer systems and peripheral equipment

BLOCK DIAGRAM



M5M27C102K, -15, -2

1048576-BIT (65536-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C102K is a high-speed 1048576-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C102K is fabricated by N-channel double polisilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 40 pin DIP with a transparent lid.

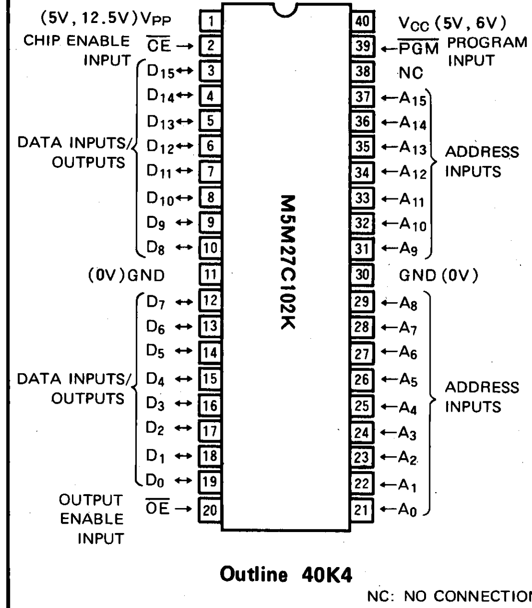
FEATURES

- 65536 word x 16 bit organization
- Access time M5M27C102K-15 .... 150ns (max.)
  M5M27C102K-2 .... 200ns (max.)
  M5M27C102K .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 50mA (max.)
  Standby ..... 1mA (max.)
- Single 5V power supply
- Programming voltage 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 40 pin DIP
- Fast programming algorithm

APPLICATION

Microcomputer systems and peripheral equipment

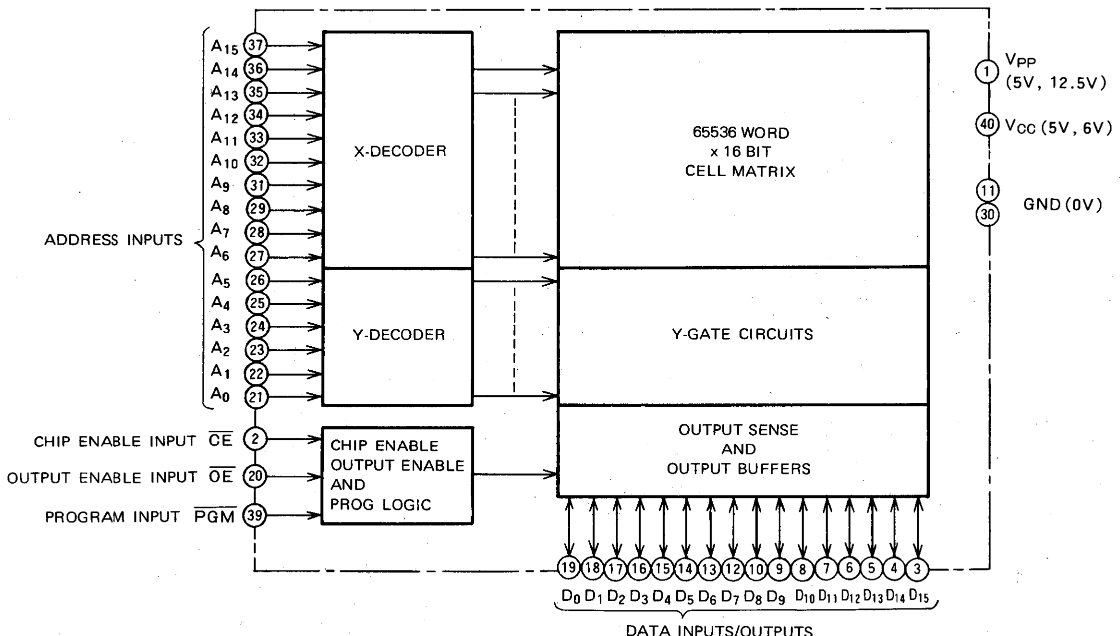
PIN CONFIGURATION (TOP VIEW)



Outline 40K4

NC: NO CONNECTION

BLOCK DIAGRAM

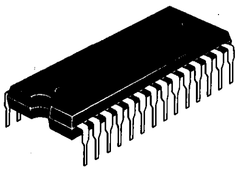


MOS OTPROM

7

M5M2764P

65536-BIT (8192-WORD BY 8-BIT) ONE TIME PROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5M2764P is a high-speed 65536-bit one time programmable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M2764P is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP.

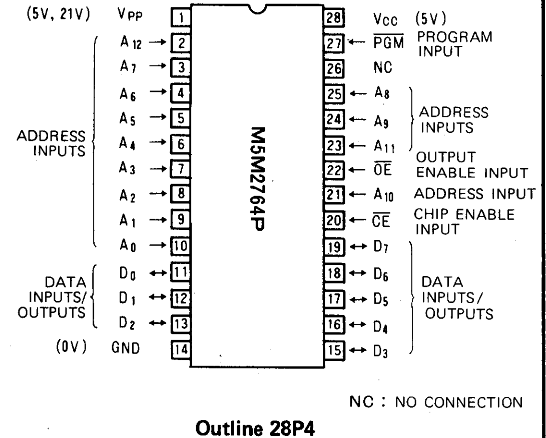
FEATURES

- 8192 word x 8-bit organization
- Access time .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active .... 100mA (max.)
  Standby .... 35mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Single location programming with one 50ms pulse
- Fast programming algorithm
- Interchangeable with Mitsubishi M5L2764K

APPLICATION

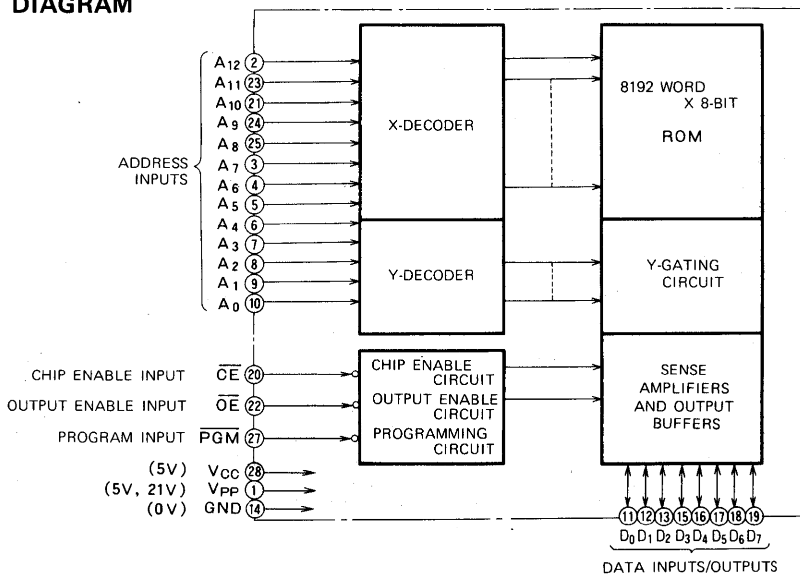
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

In the read mode V_{PP} must be at V_{CC} level.

Programming

(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.7)

(Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the V_{PP} power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{12}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leqq t_{PW} \leqq$ 55 ms.

Erase

The M5M2764P cannot be erased, because it is packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11～13, 15～19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	X*	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10～80	°C
T_{stg}	Storage temperature	−65～150	°C
V_{I1}	All input or output voltage (Note 2)	−0.6～7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6～26.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

$T_a = 0°$ to 70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$

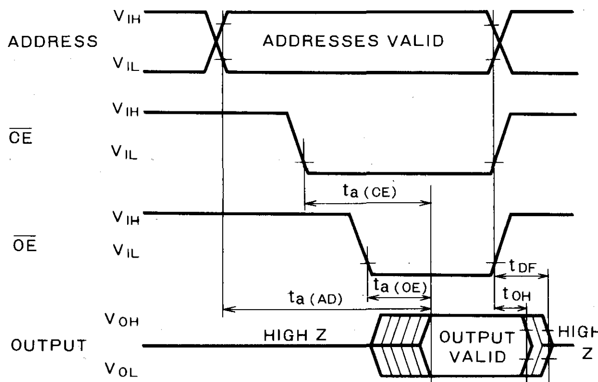
D. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	$V_{IN}=5.25V$			10	μA
I_{LO}	Output leakage current	$V_{OUT}=5.25V$			10	μA
I_{PP1}	V_{PP} current read	$V_{PP}=5.25V$			15	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			35	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}=V_{IL}$			100	mA
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{IH}	High-level input voltage		2.0		$V_{CC}+1$	V
V_{OL}	Low-level output voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	High-level output voltage	$I_{OH}=-400\mu A$	2.4			V

A. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$		250	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$		250	ns
$t_{a(OE)}$	Output enable to output delay	$\overline{CE}=V_{IL}$	10	100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0	90	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0		ns

AC WAVEFORMS



Test Conditions for A.C. Characteristics
Input Voltage: V_{IL} = 0.8V, V_{IH} = 2.2V
Input Rise and Fall Times: ≦ 20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V
Outputs 0.8V and 2V
Output Load: 1 TTL gate, C_L = 100pF

CAPACITANCE (T_a = 25°C, f = 1 MHz)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN}= 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT}= 0 V		8	12	pF

PROGRAM OPERATION

CONVENTIONAL PROGRAMMING ALGORITHM
($Ta=25\pm5$ °C, $V_{CC}=5V\pm5\%$, $V_{PP}=21\pm0.5V$ unless otherwise noted)

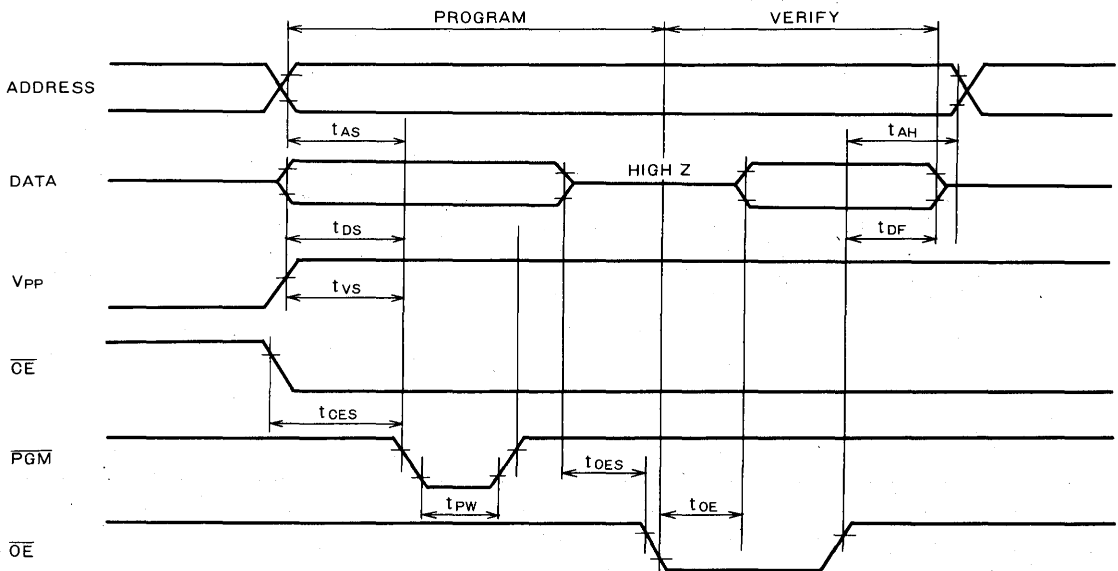
D. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Low-level output voltage (verify)	$I_{OL}=2.1mA$			0.45	V
V_{OH}	High-level output voltage (verify)	$I_{OH}=-400\mu A$	2.4			V
I_{CC2}	V_{CC} supply current (active)				100	mA
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{IH}	High-level input voltage		2.0		$V_{CC}+1$	V
I_{PP}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

A. C. CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		20			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ pulse width (programming)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test Conditions for AC Characteristics
Input Voltage: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Input Rise and Fall Times: ≦ 20ns
Reference Voltage at Timing Measurement: Inputs 1V and 2V
Outputs 0.8V and 2V

FAST PROGRAMMING ALGORITHM

DC CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

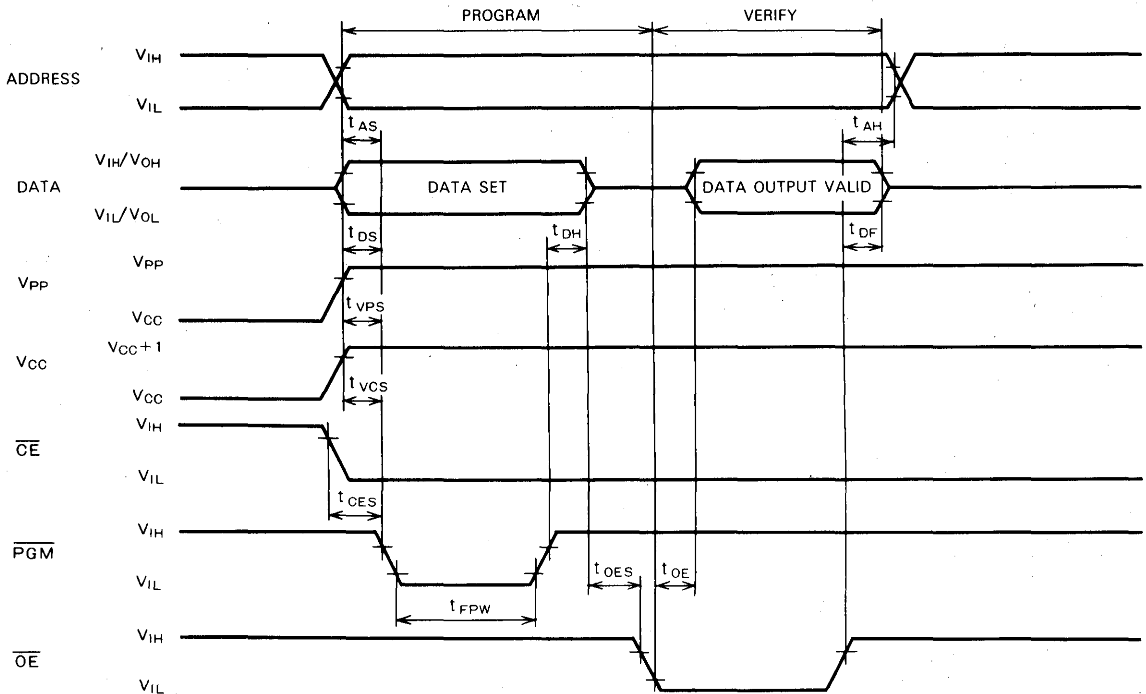
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		20			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DF}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Input rise and fall times: $\leq 20ns$
Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

FAST PROGRAMMING ALGORITHM FLOW CHART

START

FIRST ADDRESS, V_{CC}=6V, V_{PP}=21V

SET REGISTER X TO ZERO
X = 0

APPLY 1ms PROGRAM PULSE

X = X + 1

X = 15? — YES → APPLY OVERPROGRAM PULSE; NO ↓

VERIFY? — NO → APPLY 1ms PROGRAM PULSE; YES ↓

APPLY OVERPROGRAM PULSE 4×Xms

X = 15? — YES → VERIFY? (NO → FAILURE; YES → LAST ADDRESS?); NO ↓

LAST ADDRESS? — NO → NEXT ADDRESS → SET REGISTER X TO ZERO; YES ↓

(Note 3)
$V_{CC}=V_{PP}=5.0V$

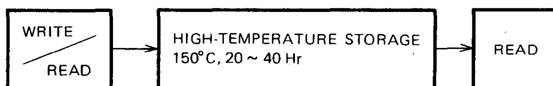
READ VERIFY? — NO → FAILURE; YES ↓

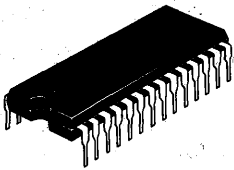
PASS

Note 3: $4.75 \leqq V_{CC}=V_{PP} \leqq 5.25V$

RECOMMENDED SCREENING CONDITION

The following screening test is recommended before using.





M5M27128P

131072-BIT (16384-WORD BY 8-BIT) ONE TIME PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27128P is a high-speed 131072-bit one time programmable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27128P is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP.

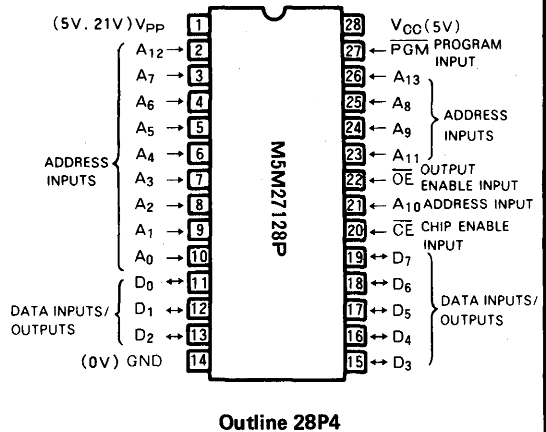
FEATURES

- 16384 word x 8 bit organization
- Access time .... 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active .... 100mA (max.)
  Standby .... 45mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Interchangeable with Mitsubishi M5L27128K

APPLICATION

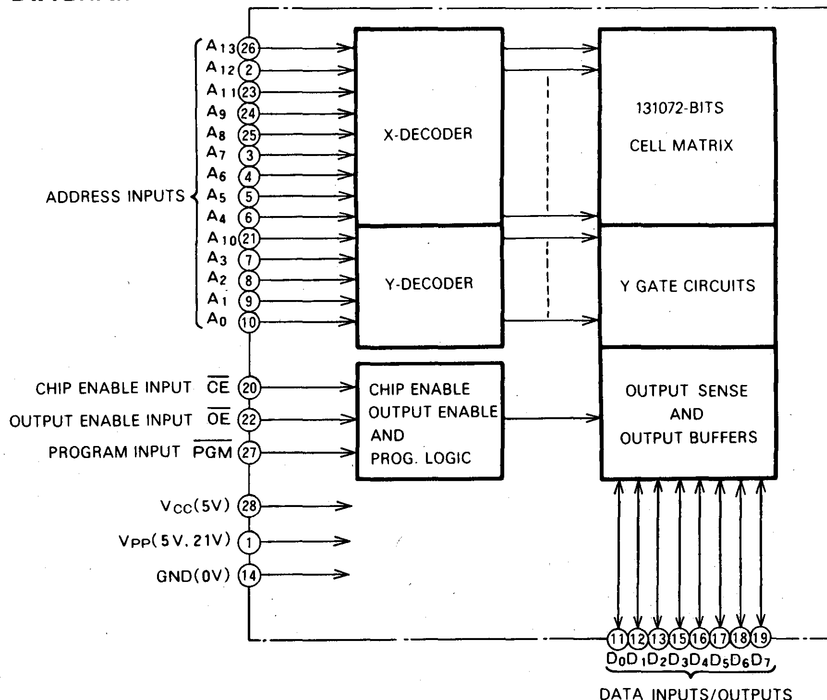
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{13}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming

(Fast programming algorithm)

First set $V_{CC}=6V$, $V_{PP}=21V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6)

(Conventional programming algorithm)

The device enters the programming mode when 21V is supplied to the V_{PP} power supply input and $\overline{CE}$ is at low level. A location is designated by address signals ($A_0 \sim A_{13}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{PGM}$ at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition 45 ms $\leqq t_{PW} \leqq$ 55 ms.

Erase

The M5M27128P cannot be erased, because it is packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	$\overline{PGM}$(27)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Data out
Standby	V_{IH}	X*	X*	V_{CC}	V_{CC}	Floating
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Data out
Program inhibit	V_{IH}	X*	X*	V_{PP}	V_{CC}	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−10~80	°C
T_{stg}	Storage temperature	−65~150	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~26.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V±5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN} = 5.25V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.25V			10	μA
I_{PP1}	V_{PP} current read	V_{PP} = 5.25V			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}$ = V_{IH}			45	mA
I_{CC2}	V_{CC} current Active	$\overline{CE}$ = $\overline{OE}$ −V_{IL}			100	mA
V_{IL}	Input low voltage		0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			V

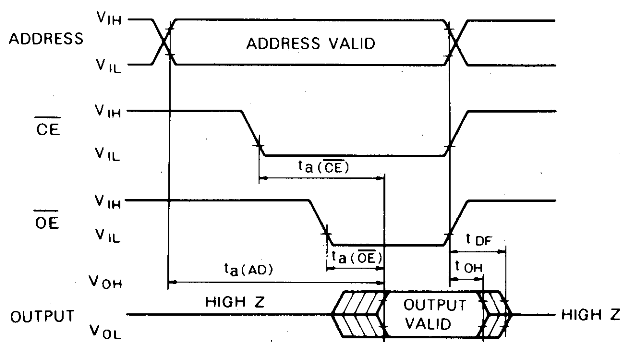
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V±5%, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}$ = V_{IL}		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}$ = V_{IL}		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}$ = V_{IL}	0	85	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

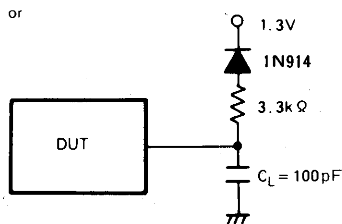
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦20ns
Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	T_a = 25°C, f = 1MHz, V_I = V_O = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS
(Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V, unless otherwise noted)

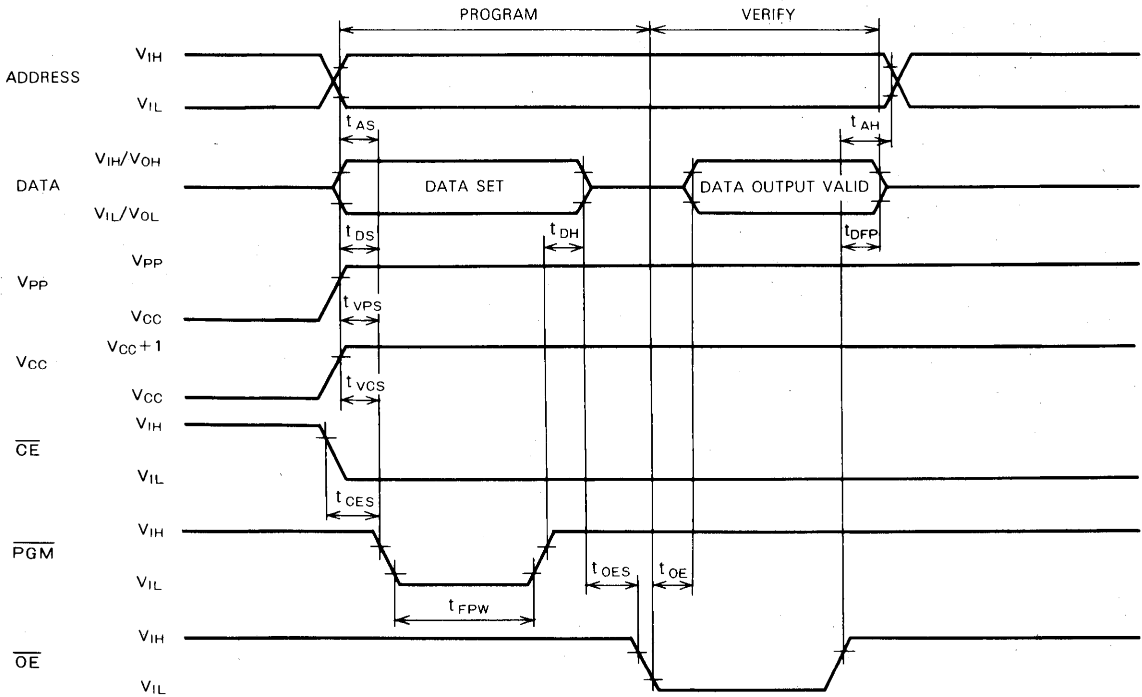
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

AC ELECTRICAL CHARACTERISTICS
(Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		3.8		63	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

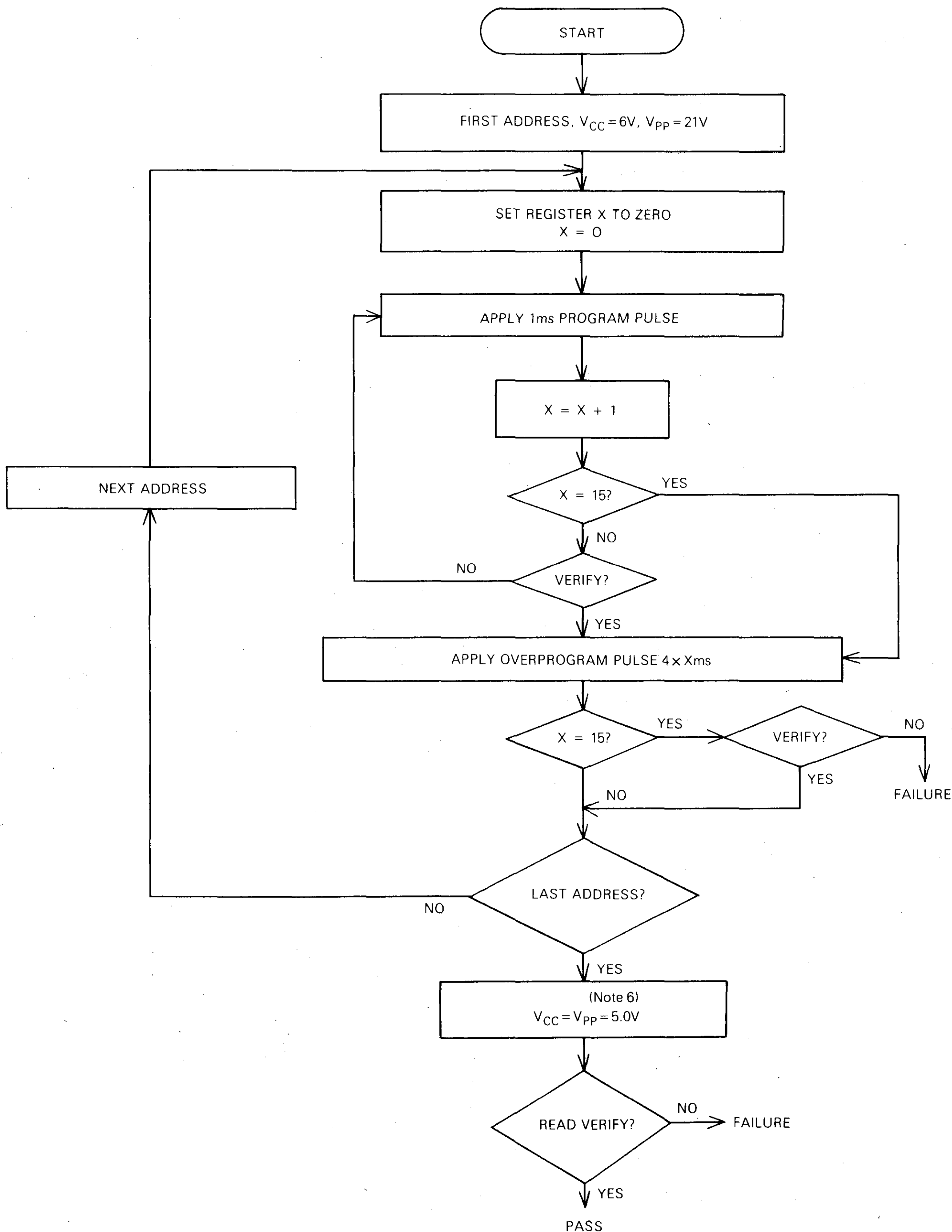
Note 5: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times: $\leq 20ns$
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V

FAST PROGRAMMING ALGORITHM FLOW CHART



Note 6: $4.75 \leqq V_{CC}=V_{PP} \leqq 5.25V$

CONVENTIONAL PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$, unless otherwise noted)

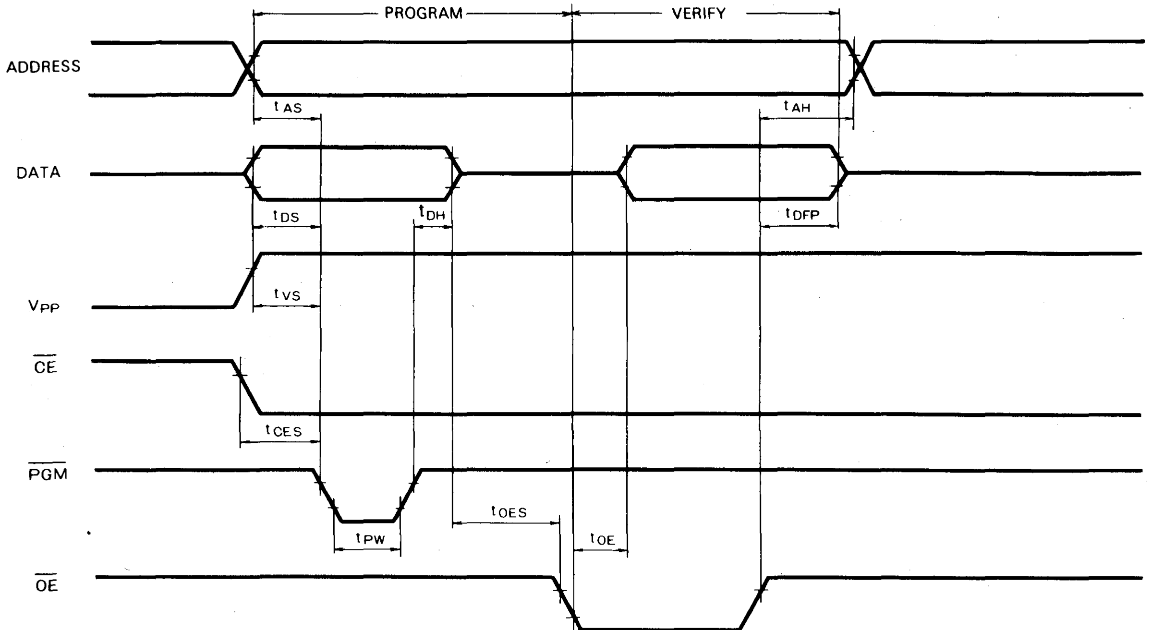
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
I_{CC2}	V_{CC} Supply current				100	mA
I_{PP2}	V_{PP} Supply current	$\overline{CE}=V_{IL}=\overline{PGM}$			30	mA

AC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address set up time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output delay		0		130	ns
t_{VS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ Pulse width (during program)		45	50	55	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Note 7: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

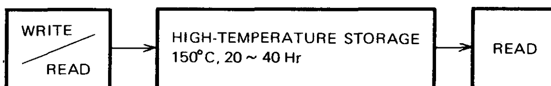
AC WAVEFORMS



Test conditions for A.C. characteristics
Input rise and fall time: ≦20ns
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Reference voltage at timing measurement: Input 0.8V and 2V
Outputs 0.8V and 2V

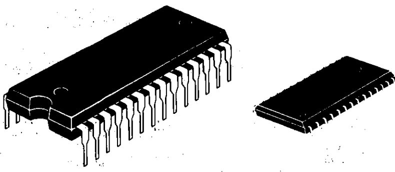
RECOMMENDED SCREENING CONDITION

The following screening test is recommended before using.



M5M27256P, FP

262144-BIT (32768-WORD BY 8-BIT) ONE TIME PROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5M27256P, FP are high-speed 262144-bit one time programmable read only memories. They are suitable for microprocessor programming applications where rapid turn-around is required. The M5M27256P, FP are fabricated by N-channel double polysilicon gate technology and are available in 28-pin plastic packages.

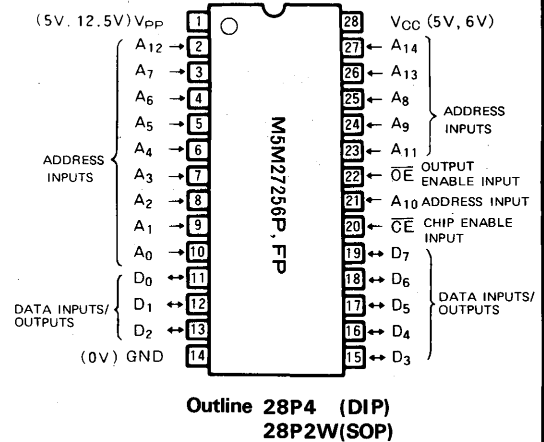
FEATURES

- 32768 Word x 8 bit organization
- Package DIP M5M27256P
  SOP M5M27256FP
- Access time .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active ..... 80mA (max.)
  Standby .... 25mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Fast programming algorithm

APPLICATION

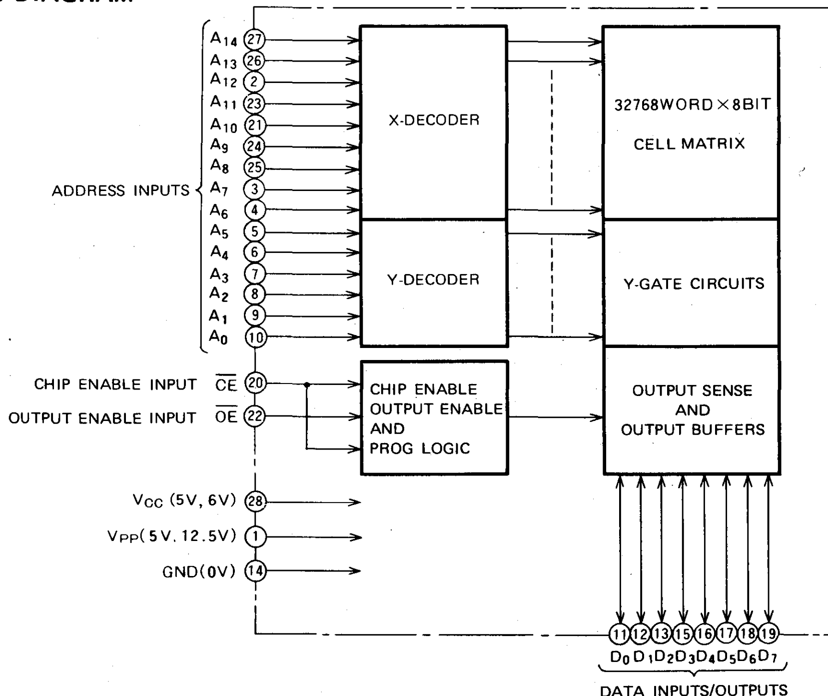
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (DIP)
28P2W(SOP)

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming (Fast programming algorithm)

First set $V_{CC}=6V, V_{PP}=12.5V$ and then set an address to first address to be programmed. After applying 1 ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

The M5M27256P, FP cannot be erased, because it is packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}$(22)	V_{PP}(1)	V_{CC}(28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Standby	V_{IH}	X*	5V	5V	Floating
Program	V_{IL}	V_{IH}	12.5V	6V	Data in
Program verify	V_{IH}	V_{IL}	12.5V	6V	Data out
Program inhibit	V_{IH}	V_{IH}	12.5V	6V	Floating

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
Topr	Operating temperature	−10~80	°C
Tstg	Storage temperature	−65~150	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7	V
V_{I2}	V_{PP} supply voltage during programming (Note 2)	−0.6~14.0	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{LI}	Input load current	$V_{IN}=5.5V$			10	μA
I_{LO}	Output leakage current	$V_{OUT}=5.5V$			10	μA
I_{PP1}	V_{PP} current read	$V_{PP}=5.5V$			5	mA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			25	mA
I_{CC2}	V_{CC} current Active	$\overline{CE}=\overline{OE}=V_{IL}$			80	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V

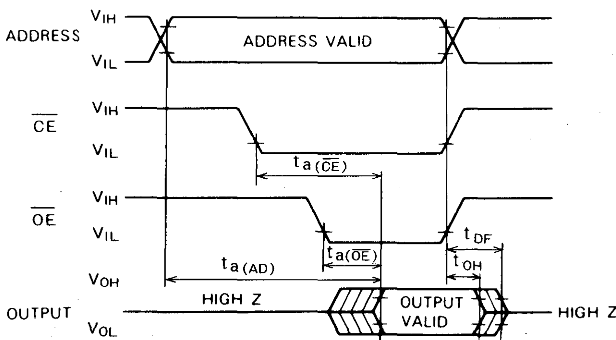
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$		250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE}=V_{IL}$		100	ns
t_{DF}	Output enable high to output float	$\overline{CE}=V_{IL}$	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0		ns

Note 4: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

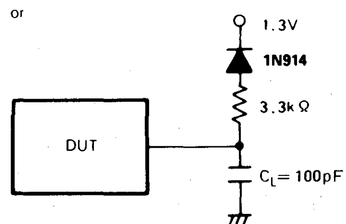
AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L(100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	$Ta=25°C$, $f=1MHz$, $V_I=V_O=0V$		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

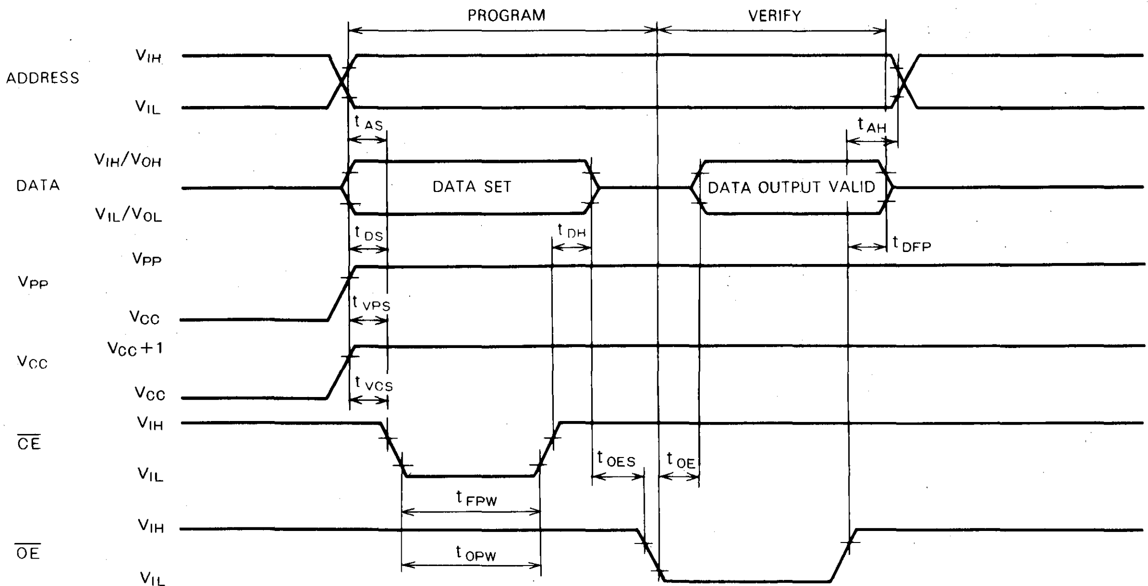
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				80	mA
I_{PP2}	V_{PP} supply current	$\overline{CE}=V_{IL}$			50	mA

AC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

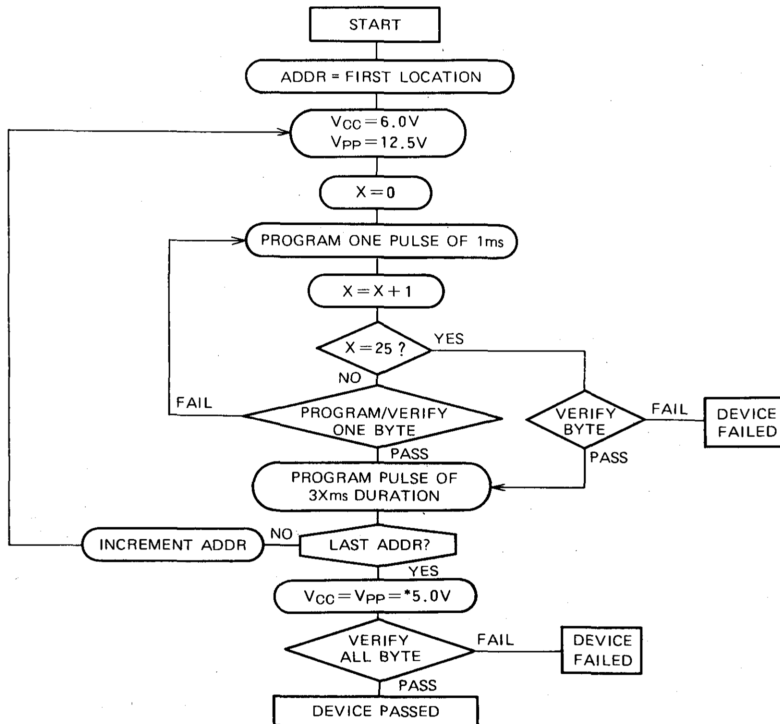
Note 5: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS



Test conditions for A.C. charactristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: $\leq$ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* $4.75V \leqq V_{CC} = V_{PP} \leqq 5.25V$

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the OTP ROM that identifies the manufacturer and device type.

The PROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

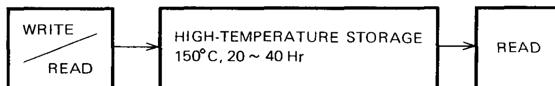
M5M27256P, FP DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	0	1	0	0	04

Note 6: $V_{CC} = 5V \pm 5\%$, $A_9 = 12.0 \pm 0.5V$, $A_1 \sim A_8$, $A_{10} \sim A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$

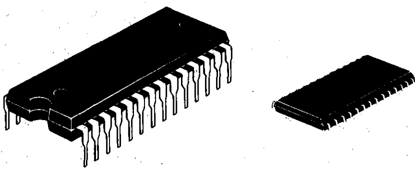
RECOMMENDED SCREENING CONDITION

The following screening test is recommended before using.



M5M27512P, FP

524288-BIT (65536-WORD BY 8-BIT) ONE TIME PROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5M27512P, FP are high-speed 524288-bit one time programmable read only memories. They are suitable for microprocessor programming applications where rapid turn-around is required. The M5M27512P, FP are fabricated by N-channel double polysilicon gate technology and are available in 28-pin plastic packages.

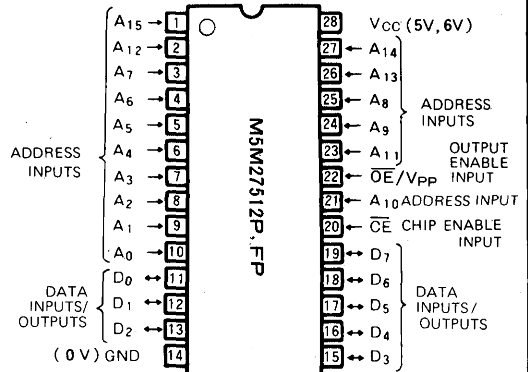
FEATURES

- 65536 Word x 8 bit organization
- Package DIP M5M27512P
  SOP M5M27512FP
- Access time .... 250ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active .... 100mA (max.)
  Standby .... 40mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Fast programming algorithm

APPLICATION

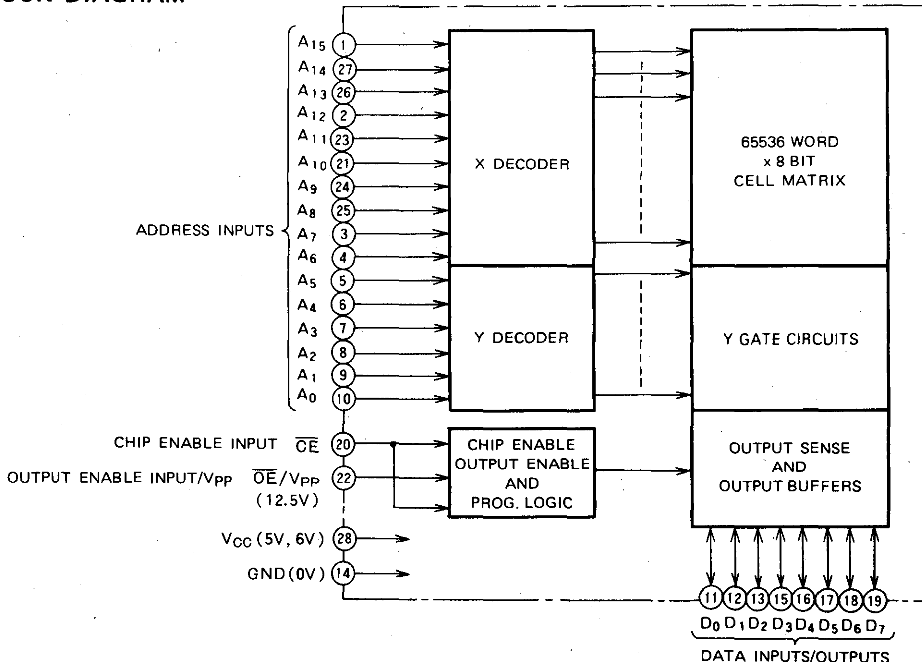
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (DIP)
28P2W(SOP)

BLOCK DIAGRAM



FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}/V_{PP}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}/V_{PP}$ and address signals to the address inputs ($A_0 \sim A_{15}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}/V_{PP}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signals is high, the device is in the standby mode or power-down mode.

Programming (Fast programming algorithm)

First set V_{CC} = 6V, $\overline{OE}/V_{PP}$ = 12.5V and then set an address to first address to be programmed. After applying 1ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1ms program pulse. The programmer continues 1ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

The M5M27512P, FP cannot be erase, because it is packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$(20)	$\overline{OE}/V_{PP}$(22)	V_{CC}(28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	5 V	Data out
Output disable	V_{IL}	V_{IH}	5 V	Floating
Standby	V_{IH}	X*	5 V	Floating
Program	V_{IL}	12.5V	6 V	Data in
Program inhibit	V_{IH}	12.5V	6 V	Floating

*: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	− 10 ~ 80	°C
T_{stg}	Storage temperature	− 65 ~ 150	°C
V_{I1}	All input or output voltage (Note 2)	−0.6~7.0	V
V_{I2}	$\overline{OE}/V_{PP}$ supply voltage (Note 2)	−0.6~14.0	V
V_{I3}	A9 input voltage (Note 2)	−0.6~13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V			10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE}=V_{IH}$			40	mA
I_{CC2}	V_{CC} current active	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$			100	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

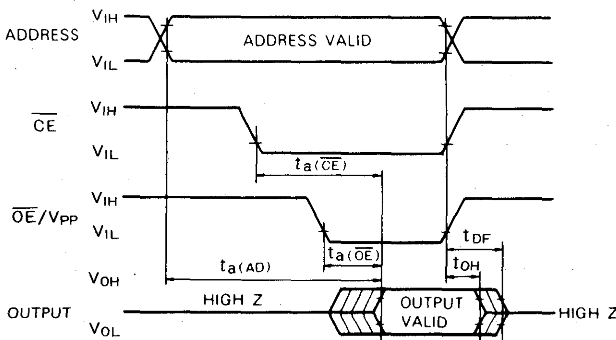
Note 3: Typical values are at T_a = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$		250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}/V_{PP}=V_{IL}$		250	ns
$t_{a(\overline{OE})}$	$\overline{OE}$ to output delay	$\overline{CE}=V_{IL}$		100	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE}=V_{IL}$	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$	0		ns

Note 4: V_{CC} must be applied simultaneously or before $\overline{OE}$/Vpp and removed simultaneously or after $\overline{OE}$/Vpp.

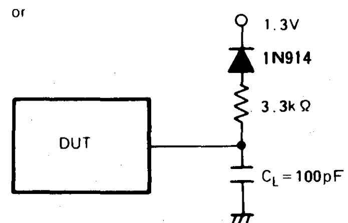
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≤ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C_L (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	Ta = 25°C, f = 1MHz, $V_I = V_O$ = 0V		4	6	pF
C_{OUT}	Output capacitance			8	12	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

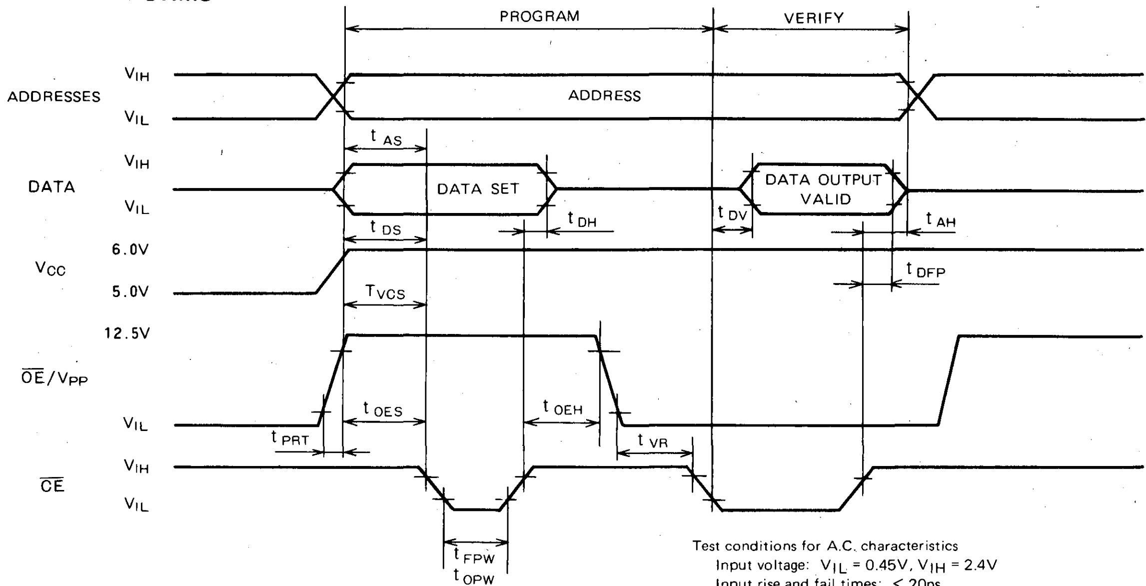
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=V_{IL}$ or V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				100	mA
I_{PP2}	$\overline{OE}$/Vpp supply current	$\overline{CE}=V_{IL}$			50	mA

AC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$/Vpp setup time		2			μs
t_{OEH}	$\overline{OE}$/Vpp hold time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{OE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{DV}	Data valid from $\overline{CE}$				1	μs
t_{VR}	$\overline{OE}$/Vpp recovery time		2			μs
t_{PRT}	$\overline{OE}$/Vpp pulse rise time during program		50			ns

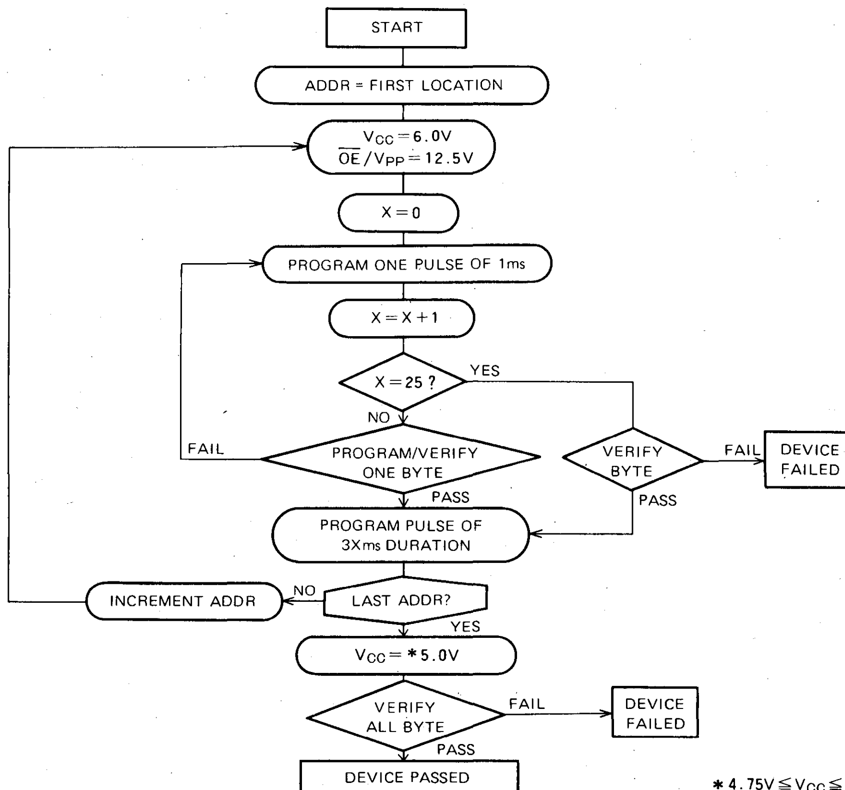
Note 5: V_{CC} must be applied simultaneously or before $\overline{OE}$/Vpp and removed simultaneously or after $\overline{OE}$/Vpp.

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fail times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

FAST PROGRAMMING ALGORITHM FLOW CHART



* 4.75V ≦ V_{CC} ≦ 5.25V

MITSUBISHI ELECTRIC

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the OTP ROM that identifies the manufacturer and device type.

The PROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

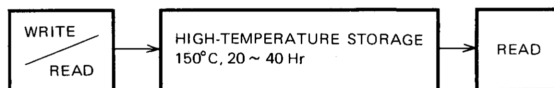
M5M27512P, FP DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	0	0	0	0	1	1	0	1	0D

Note 6: $V_{CC}=5V\pm5\%$, $A_9=12.0\pm0.5V$, $A_1\sim A_8$, $A_{10}\sim A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP}=V_{IL}$

RECOMMENDED SCREENING CONDITION

The following screening test is recommended before using.

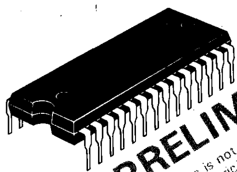


MOS EEPROM

8

M5M28C64P

65536-BIT(8192-WORD BY 8-BIT) ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM



DESCRIPTION

The Mitsubishi M5M28C64P is a 65536 bit electrically erasable and programmable high speed read-only memory.

It is suitable for microprocessor programming applications where on-board programming is required. The M5M28C64P is fabricated by N-channel double polysilicon Memory gate and CMOS technology for peripheral circuits, and available in a 28 pin DIP.

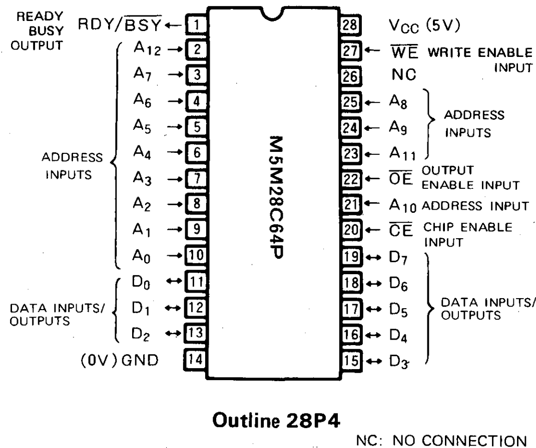
FEATURES

- 5V Only operation
- Page mode write .... 16byte (max.)
- Chip erase time .... 10ms (max.)
- Automatic erase before write
- Fast read access time .... 150ns (max.)
- Low power current (I_{CC}): Active ..... 30mA (max.)
  Standby ..... 1mA (max.)
- JEDEC approved byte-wide pinout
- CMOS double polysilicon gate technology
- 10000 erase/write cycles
- 10 years data retention

APPLICATION

Microcomputer systems and peripheral equipment

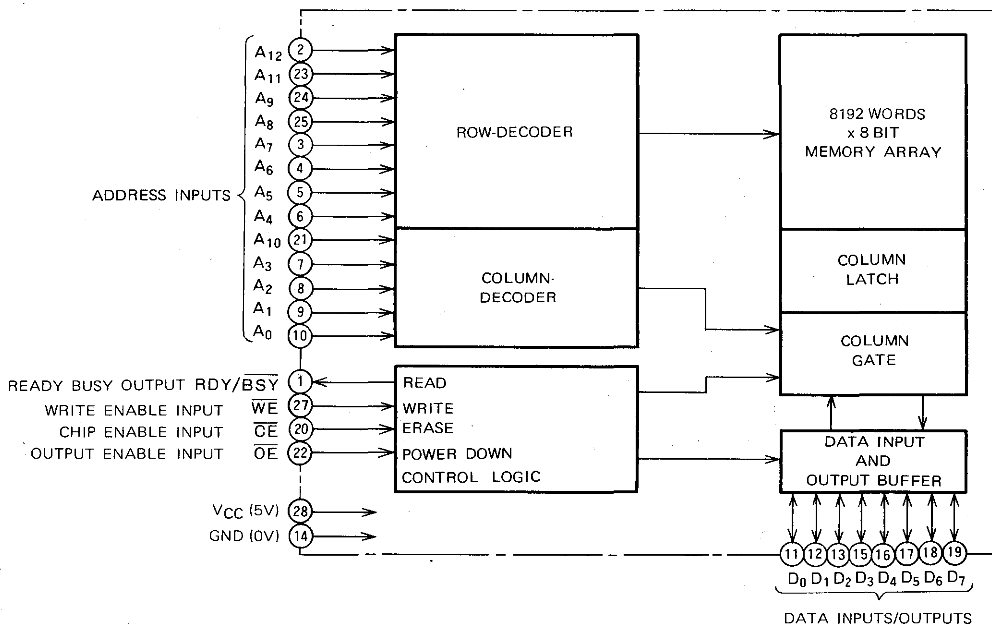
PIN CONFIGURATION (TOP VIEW)



Outline 28P4

NC: NO CONNECTION

BLOCK DIAGRAM



FUNCTION

Read

Low level input to $\overline{CE}$ and $\overline{OE}$, High level input to $\overline{WE}$ and address signals to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power down mode.

Programming

Set the $\overline{CE}$ terminal to the low level and $\overline{OE}$ terminal to the high level. A location is designated by address signals ($A_0 \sim A_{12}$), and the data to be programmed must be applied at 8 bits in parallel to the data inputs ($D_0 \sim D_7$). A program pulse to the $\overline{WE}$ at this state will effect programming.

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{BSY}$ (1)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	Data out
Standby	V_{IH}	X *2	X *2	HIGH-Z	HIGH-Z
Program	V_{IL}	V_{IH}	V_{IL}	HIGH-Z + V_{OL}	Data in
Chip erase	V_{IL}	V_{OE} *1	V_{IL}	HIGH-Z + V_{OL}	Data in = V_{IH}
Program inhibit	X *2	X *2	V_{IH}	HIGH-Z	—— *3
Program inhibit	X *2	V_{IL}	X *2	HIGH-Z	—— *3

*1: V_{OE} 9V to 15V.
*2: X can be either V_{IH} or V_{IL}.
*3: depend on the input condition

ABSOLUTE MAXIMUM RATINGS (Note)

Symbol	Parameter	Condition	Ratings	Unit
V_{I1}	Input voltage (V_{CC}, Data, Address, $\overline{CE}$, $\overline{WE}$)	With respect to GND	−0.6~7	V
V_{I2}	Input voltage ($\overline{OE}$)		−0.6~17	V
Topr	Operating temperature		−10~80	°C
Tstg	Storage temperature		−65~125	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above these indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods affects device reliability.

READ OPERATION

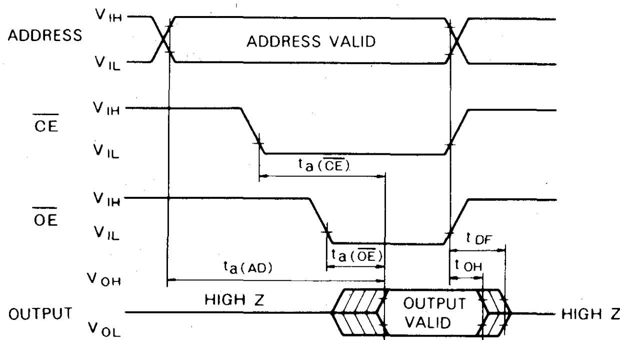
DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	V_{IN}=5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT}=5.5V			10	μA
I_{CC1}	V_{cc} current standby	$\overline{CE}=V_{IH}$			1.0	mA
I_{CC2}	V_{cc} current active	$\overline{CE}=\overline{OE}=V_{IL}$			30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test condition	Limit				Unit
			M5M28C64P-15		M5M28C64P		
			Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}=\overline{OE}=V_{IL}$		150		200	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}=V_{IL}$		150		200	ns
$t_{a(\overline{OE})}$	$\overline{OE}$ to output delay	$\overline{CE}=V_{IL}$		50		75	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE}=V_{IL}$	0	40	0	60	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}=\overline{OE}=V_{IL}$	0		0		ns

AC WAVEFORMS ($\overline{WE}$=H)



Test condition for A.C. characteristics
Input voltage: Vil = 0.45V, Vih = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V, Output 0.8V and 2V
Output load: 1TTL gate + CL (100pF)

CAPACITANCE (Ta=25°C, f=1MHz unless otherwise noted.)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	V_{IN}=0V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT}=0V		8	12	pF

BYTE ERASE, BYTE PROGRAM OPERATION

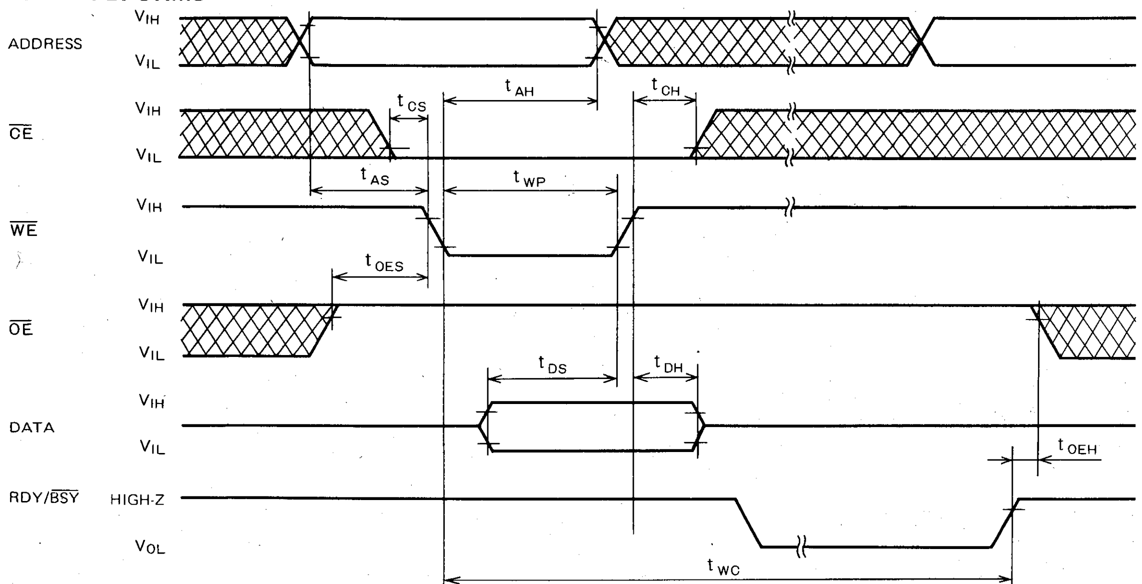
DC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN}=V_{IL}, V_{IH}$			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
I_{CC2}	V_{CC} current active				30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{RB}	Ready/$\overline{Busy}$ output low voltage	$I_{RB}=2.1mA$			0.45	V

AC ELECTRICAL CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		10			ns
t_{AH}	Address hold time		150			ns
t_{CS}	$\overline{CE}$ setup time		0			ns
t_{CH}	$\overline{CE}$ hold time		0			ns
t_{DS}	Data setup time		50			ns
t_{DH}	Data hold time		10			ns
t_{OES}	$\overline{OE}$ setup time		10			ns
t_{OEH}	$\overline{OE}$ hold time		100			μs
t_{WP}	Write pulse width		0.15		200	μs
t_{WC}	Write cycle time		10			ms

AC WAVEFORMS



Test condition for A.C. characteristics
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times: $\leq$ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V, Output 0.8V and 2V

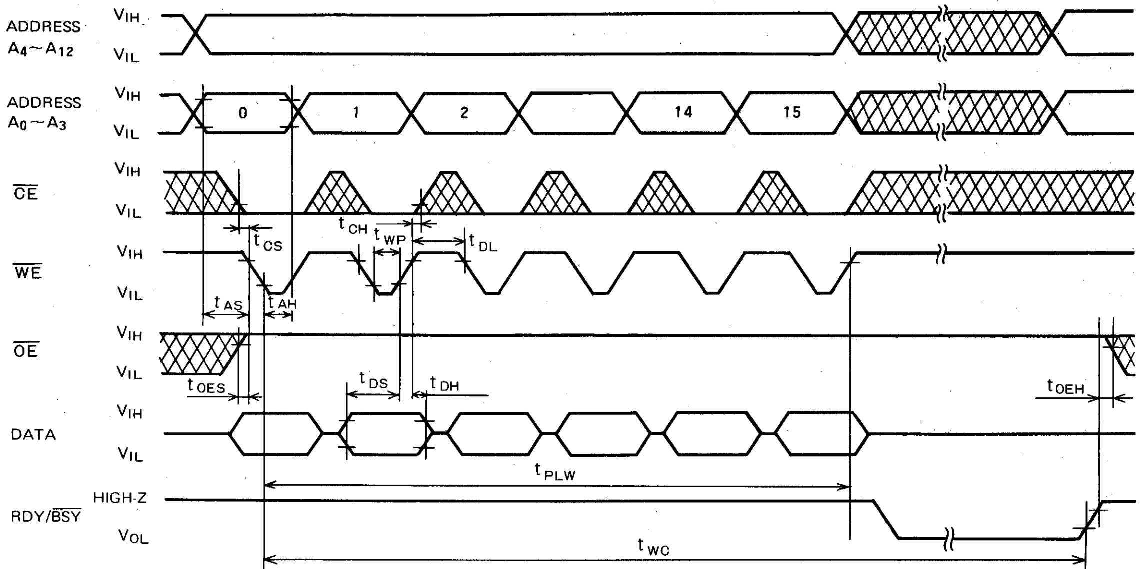
PAGE ERASE, PAGE PROGRAM OPERATION
DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN}=V_{IL}$, V_{IH}			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400μA$	2.4			V
I_{CC2}	V_{CC} current active				30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{RB}	Ready/$\overline{Busy}$ output low voltage	$I_{RB}=2.1mA$			0.45	V

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test condition	Limit			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		10			ns
t_{AH}	Address hold time		150			ns
t_{CS}	$\overline{CE}$ setup time		0			ns
t_{CH}	$\overline{CE}$ hold time		0			ns
t_{DS}	Data setup time		50			ns
t_{DH}	Data hold time		10			ns
t_{OES}	$\overline{OE}$ setup time		10			ns
t_{OEH}	$\overline{OE}$ hold time		100			μs
t_{WP}	Write pulse width		150			ns
t_{DL}	Data latch time		150			ns
t_{PLW}	Page load width				200	μs
t_{WC}	Write cycle time		10			ms

AC WAVEFORMS



Test condition for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input 0.8V and 2V, Output 0.8V and 2V

PAGE MODE WRITE

PAGE MODE WRITE feature allows 1 to 16 bytes of data to be written into a single write cycle.

A page is defined by addresses A_4 through A_{12}. During the page load cycle, these addresses must not be changed.

Following a byte write signal, 1 to 15 additional bytes of data must be loaded into the EEPROM within 200μsec.

READY/BUSY SIGNAL

Ready/Busy signal allows to sign the completion of a byte or page mode write cycle.

During a write cycle, Ready/Busy signal has VOL. After completion of the write cycle, Ready/Busy signal has high impedance.

The Ready/Busy pin is an open-drain output. So the pull-up resistor is required. A typical pullup resistor value for Ready/Busy pin is 3kΩ, assuming total input current of devices connected to Ready/Busy pin is less than 0.5mA.

DATA PROTECTION

(1) Noise Protection
A WE pulse of less than 20ns will not initiate a write cycle.

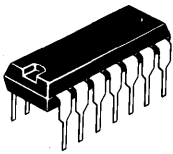
(2) V_{CC} Sense
When the V_{CC} is less than approximately 3.5 volt, write cycle is not initiated

(3) Write Inhibit
Holding OE L, WE H or CE H, inhibits a write cycle during power-on and power-off.

MOS EAROM

9

M58630P



2048-BIT (128-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58630P is a serial input/output 2048 bit electrically erasable and reprogrammable ROM organized as 128 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage .... 10 years (min)
- Write/erase time .... 20ms word
- Typical power supply voltages .... –30V, +5V
- Number of erase-write cycles ...... 10^5 times (min)
- Number of read access unrefreshed .. 10^9 times (min)
- 5V I/O interface

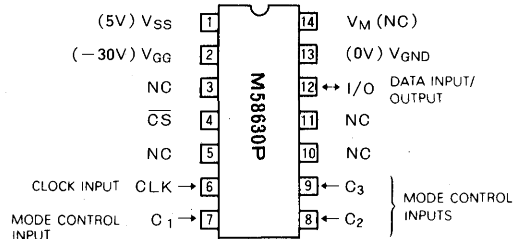
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems.

FUNCTION

The address is designated by one-of-eight and one-of-sixteen coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2–Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

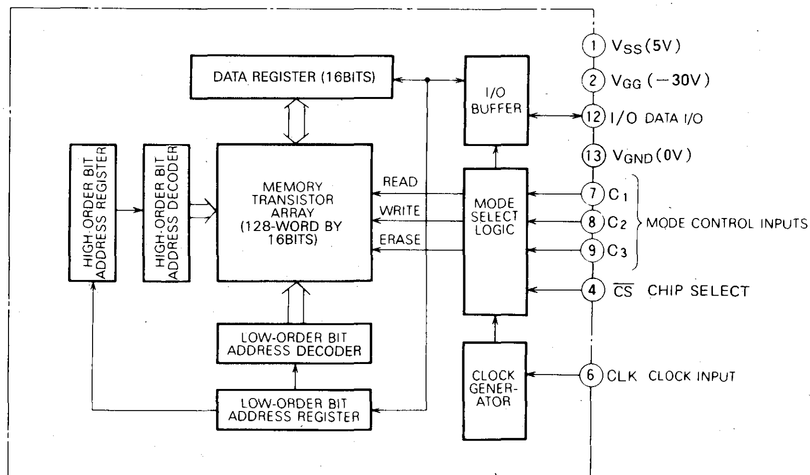
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

BLOCK DIAGRAM



2048-BIT (128-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to –30V.
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.
V_{GND}	Ground voltage	Connected to ground (OV)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode. The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low level.
H	L	L	Accept address mode. Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by one-of-eight and one-of-sixteen-coded digits 128-word address is assigned in this mode.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ –40	V
V_I	Input voltage		0.3 ~ –20	V
V_O	Output voltage		0.3 ~ –20	V
Tstg	Storage temperature		–40 ~ 125	℃
Topr	Operating temperature		–10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = –10 ~ 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{GG}-V_{SS}$	Supply voltage	–32.2	–35	–37.8	V
$V_{SS}-V_{GND}$	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

MITSUBISHI ELECTRIC

2048-BIT (128-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

ELECTRICAL CHARACTERISTICS ($T_a = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		V_{SS}-6.5		V_{SS}-4.25	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	$V_I - V_{SS} = -6.5V$	−10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		kΩ
I_{OZL}	Off-state output current, low-level voltage applied	$V_O - V_{SS} = -6.5V$	−10		+10	μA
V_{OH}	High-level output voltage	$I_{OH} = -200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL} = 80\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O = 0\mu A$		5.5	10	mA

Note 1: Typical values are at Ta = 25°C and $V_{GG}-V_{SS}$ = -35V.

TIMING REQUIREMENTS ($T_a = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted)

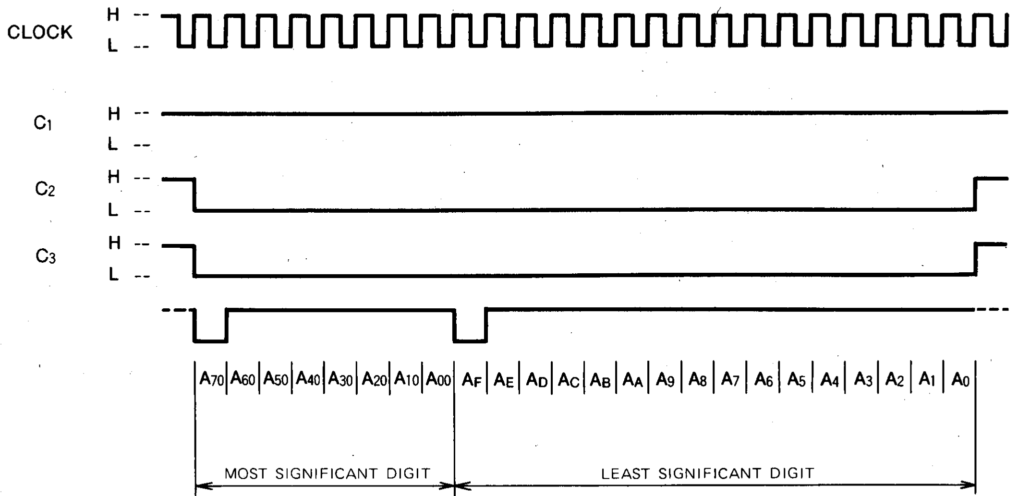
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T_{(\phi)}$	Clock period				1000	μs
t_W	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{SU}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{SS}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS ($T_a = -10 \sim 70°C$, $V_{GG} = -35V \pm 8\%$, unless otherwise noted)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
ta(c)	Read access time	t_{PW}	C_L = 100pF, $V_{OH} = V_{SS} - 2V$, $V_{OL} = V_{GND} + 1.5V$			20	μs
ts	Unpowered nonvolatile data retention time	T_S	$N_{EW} = 10^4$, $t_{W(W)}$ = 20ms, $t_{W(E)}$ = 20 ms	10			Year
		T_S	$N_{EW} = 10^5$, $t_{W(W)}$ = 20ms, $t_{W(E)}$ = 20 ms	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number pF read access unrefreshed	N_{RA}		10^9			Times
tdv	Data valid time	t_{PW}				20	μs

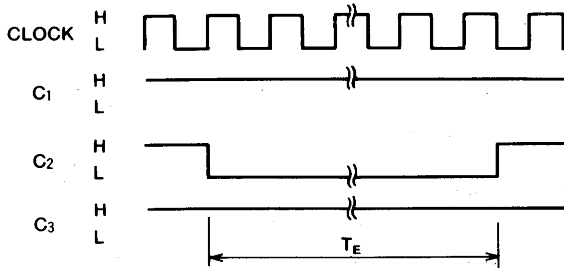
TIMING DIAGRAM

Accept Address Mode (24 clocks) $\overline{CS}$: L

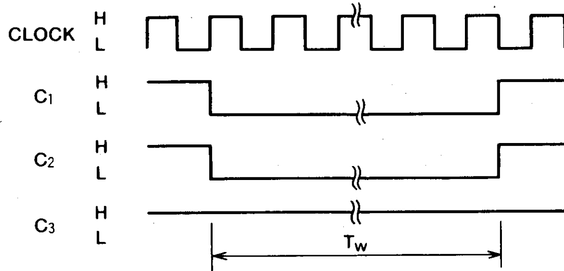


Note 2: The addresses from A_{00} to A_{7F} are designated by one-of-eight and one-of-sixteen coded digits.
The above figure shows designation of address A_{7F}.

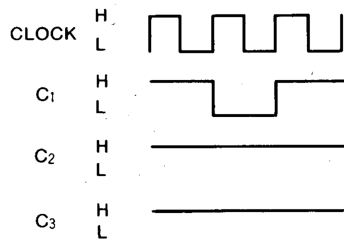
Erase Mode $\overline{CS}$: L



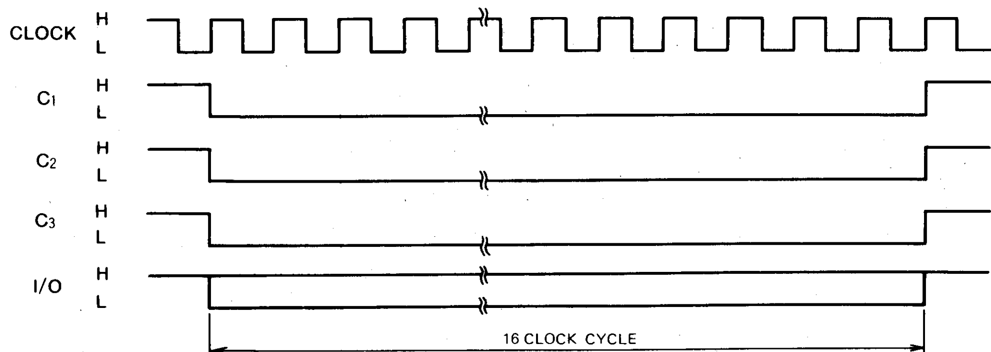
Write Mode $\overline{CS}$: L



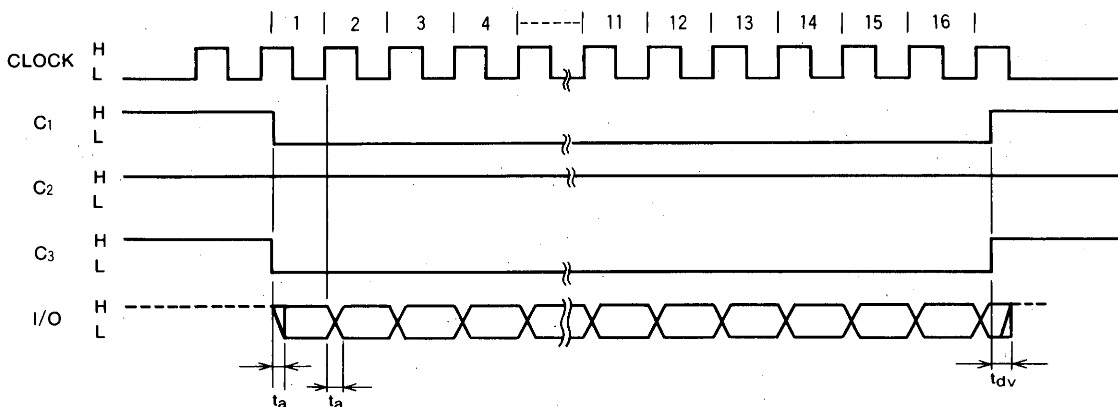
Read Mode (1 clock) $\overline{CS}$: L



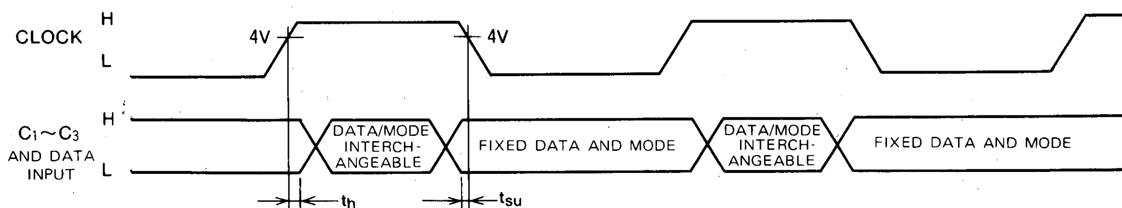
Accept Data (16 clocks) $\overline{CS}$: L



Shift Data Output Mode (16 clocks) $\overline{CS}$: L

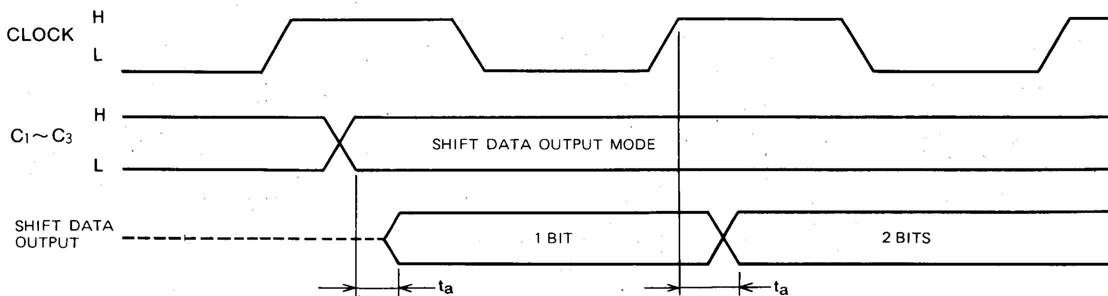


Timing of clock, C_1, C_2, C_3, and data input



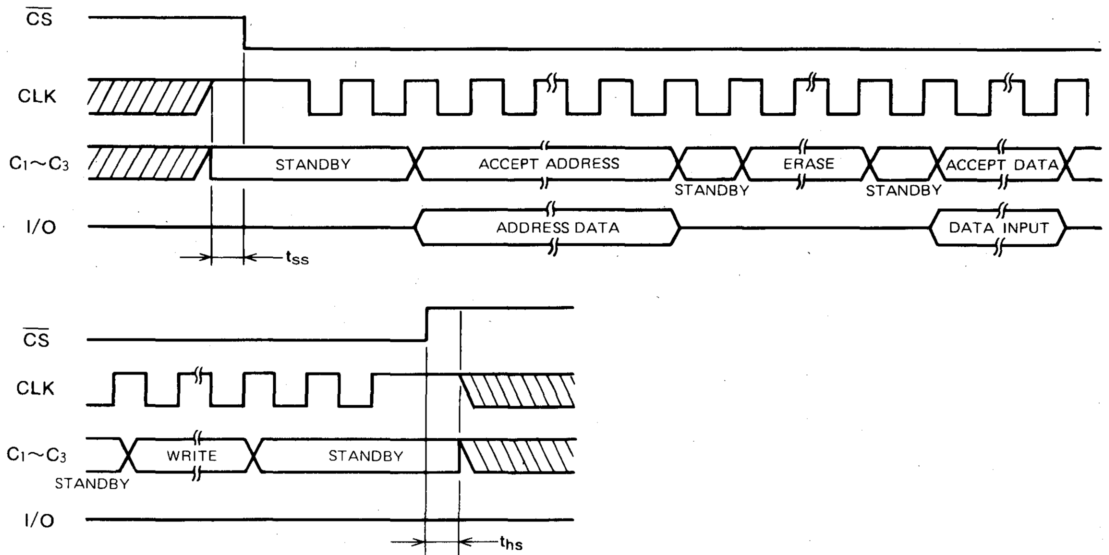
Note 3: $C_1 \sim C_3$ and accept data are interchnageable while the clock is set high.

Timing of clock, C_1, C_2, C_3, and data input



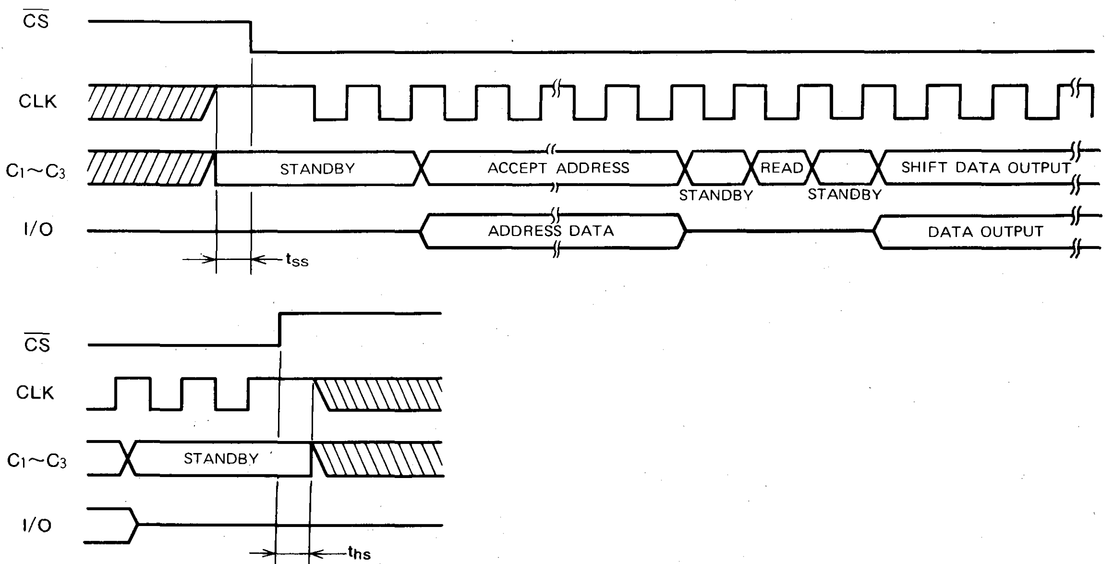
Operation flowchart

Rewriting flowchart



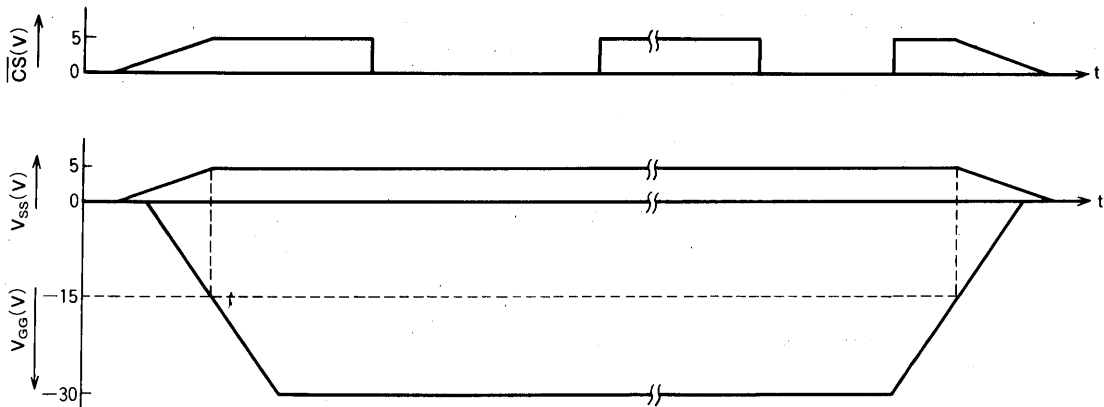
Note 4: One or more clock are required for standby between modes.
5: Set $\overline{CS}$ to the low level after the lapse of t_{ss} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
6: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs}.

Read Flowchart

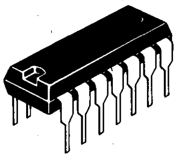


Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied. With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.



M58653P



700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58653P is a serial input/output 700 bit electrically erasable and reprogrammable ROM organized as 50 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time 20ms/word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

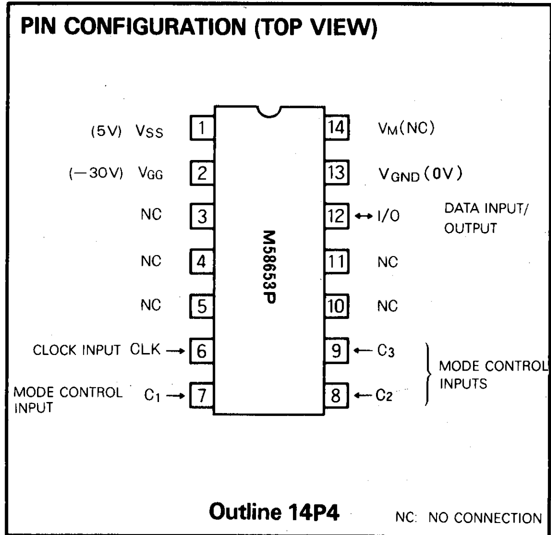
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

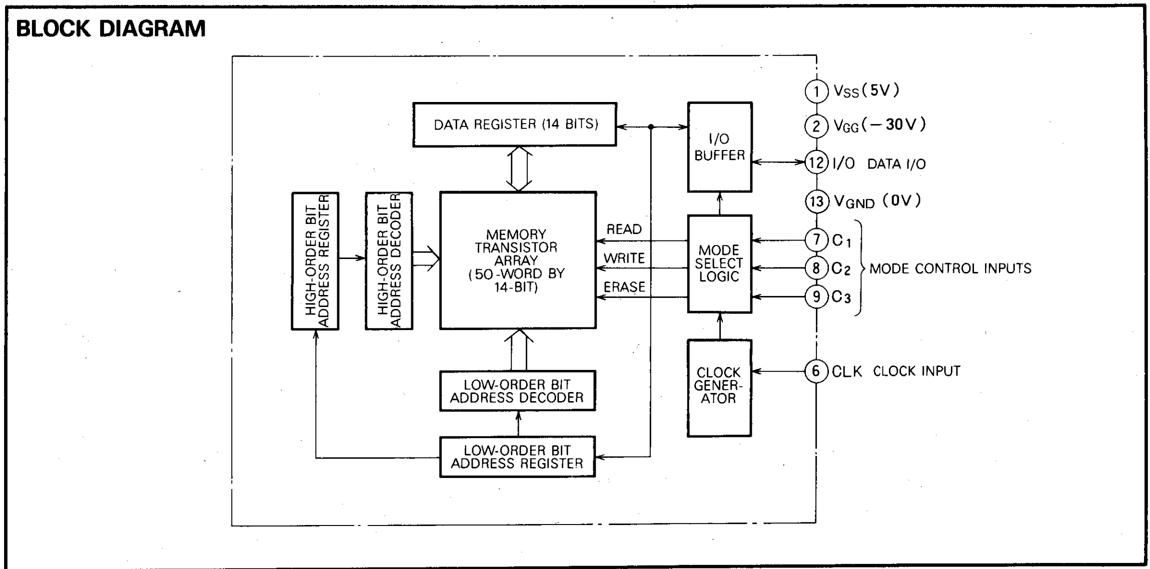
The address is designated by one of five and one of ten coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC: NO CONNECTION

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to −30V.
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.
V_{GND}	Ground voltage	Connected to ground (OV)

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by one of five and one of ten coded digits.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
Tstg	Storage temperature		−40 ~ 125	℃
Topr	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}-V_{SS}	Supply voltage	−32.2	−35	−37.8	V
V_{SS}-V_{GND}	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	V_{SS}-6.5		V_{SS}-4.25	V

Note 1:
The order of V_{SS} V_{GG} with on or off.
With on, V_{GG} is turned on after V_{SS} is done.
With off, V_{SS} is turned off after V_{GG} is done.

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ 70℃, V_{GG}-V_{SS} = −35V ± 8%, V_{SS}-V_{GND} = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		V_{SS}-6.5		V_{SS}-4.25	V
I_{IL}	Low-level input current	V_I-V_{SS} = −6.5V			±10	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_O-V_{SS} = −6.5V			±10	μA
V_{OH}	High-level output voltage	I_{OH} = −200μA	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	I_{OL} = 10μA			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	I_O = 0μA		5.5	8.8	mA

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

TIMING REQUIREMENTS (Ta = −10 ~ 70℃, V_{GG}-V_{SS} = −35V ± 8%, V_{SS}-V_{GND} = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

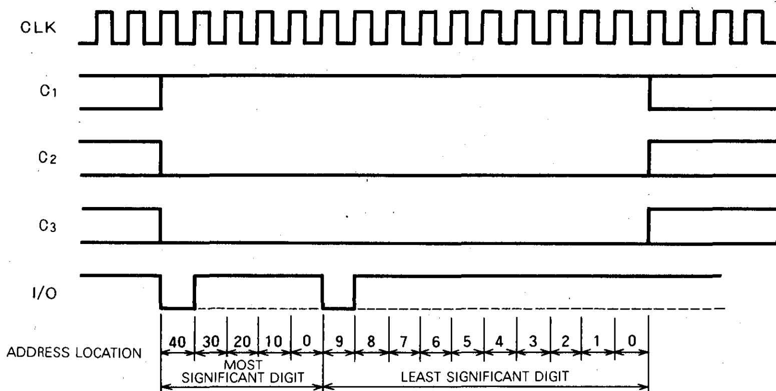
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
f(φ)	Clock frequency	fφ		10	14	17	kHz
D(φ)	Clock duty cycle	Dφ		30	50	55	%
tw(w)	Write time	tw		16	20	24	ms
tw(E)	Erase time	te		16	20	24	ms
tr, tf	Risetime, fall time	tr, tf				1	μs
tsu(c−φ)	Control setup time before the fall of the clock pulse	t_{CS}		0			ns
th(φ−c)	Control hold time after the rise of the clock pulse	t_{CH}		0			ns

SWITCHING CHARACTERISTICS (Ta = −10 ~ 70℃, V_{GG} = −35V ± 8%, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
ta(c)	Read access time	t_{PW}	C_L = 100PF, $V_{OH} = V_{SS} - 2V$, $V_{OL} = V_{GND} + 1.5V$			20	μs
ts	Unpowered nonvolatile data retention time	Ts	$N_{EW} = 10^4$, tw(w) = 20ms, tw(E) = 20ms	10			Year
		Ts	$N_{EW} = 10^5$, tw(w) = 20ms, tw(E) = 20ms	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
tdv	Data valid time	t_{PW}				20	μs

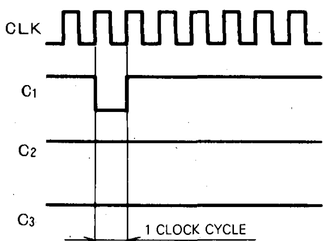
TIMING DIAGRAM

Accept Address Mode

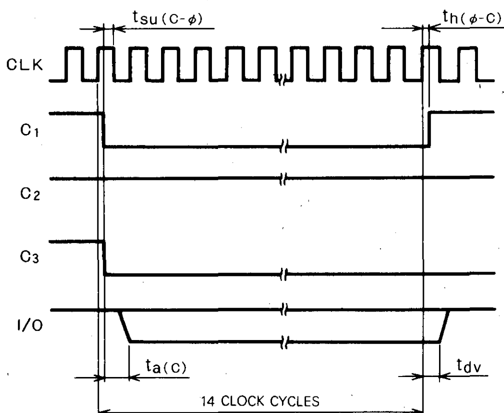


Note 3: The address is designated by one-of-five and one-of-ten coded digits. The figure shows designation of the address 49.

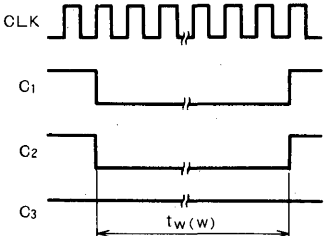
Read Mode



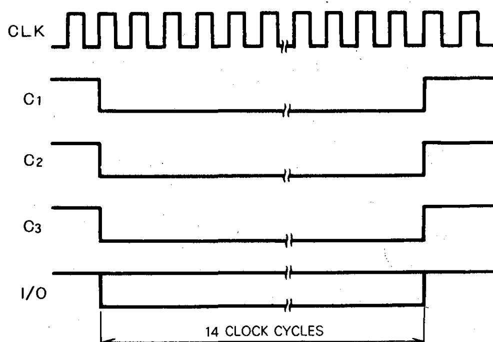
Shift Data Output Mode



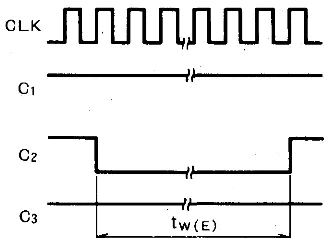
Write Mode



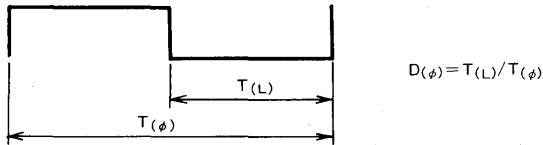
Accept Data Mode



Erase Mode



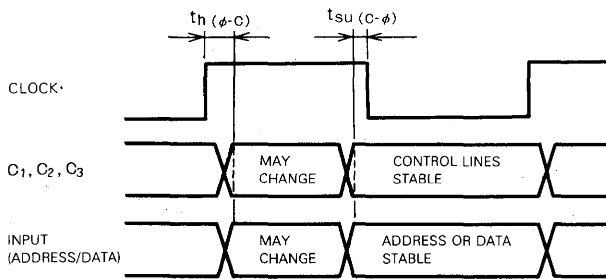
The difinition of clock duty cycle, D (ϕ)



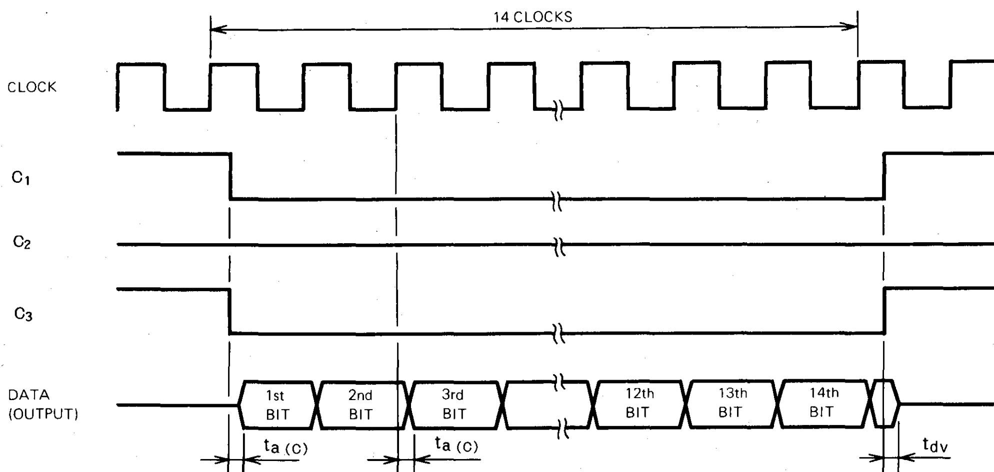
$D_{(\phi)} = T_{(L)}/T_{(\phi)}$

Timing of data input and mode control inputs

Mode control inputs, C_1, C_2, C_3 and input signal my change, when clock is 'H' level.

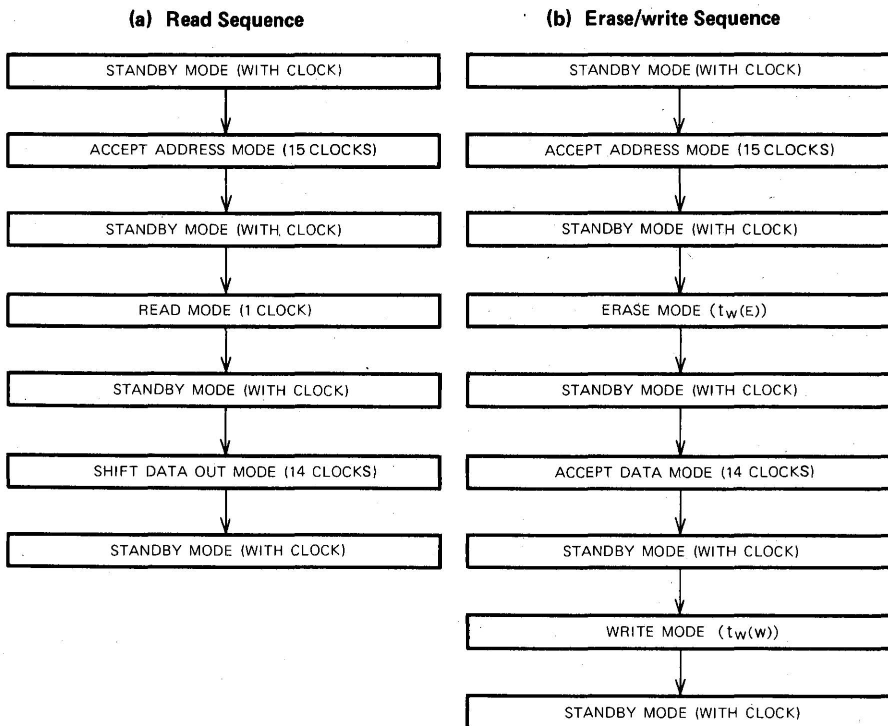


Timing of data output

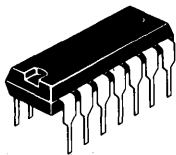


The 1st bit of output data is output after access time of $t_{a(C)}$ from the mode control transition. And other bits are output after $t_{a(C)}$ from positive edge of clock.

Operating sequential flow



M58655P



1024-BIT(64-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58655P is a serial input/output 1024bit electrically erasable and reprogrammable ROM organized as 64 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time . . . . 20ms word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

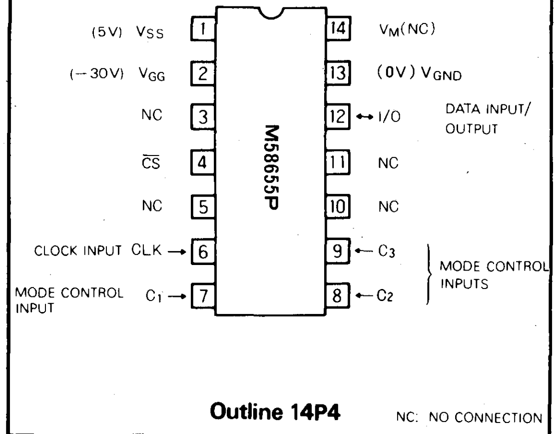
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

The address is designated by two consecutive one-of-eight coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

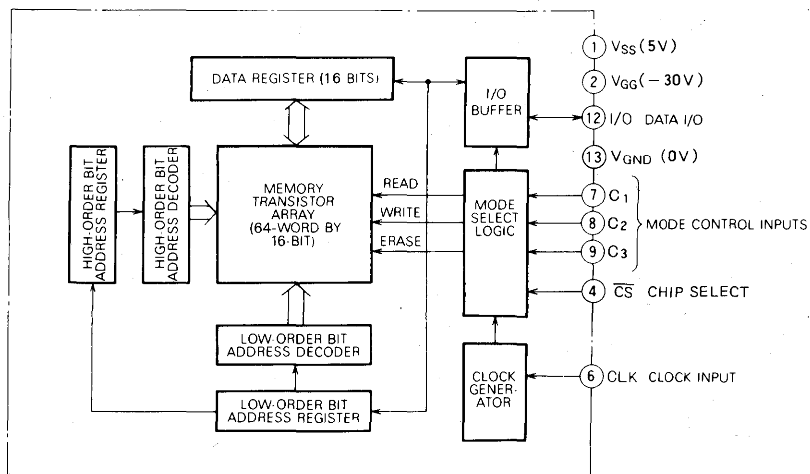
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

BLOCK DIAGRAM



1024-BIT(64-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to −30V.
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode
V_{GND}	Ground voltage	Connected to ground (OV)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged The output buffer is held in the floating state.
H	H	L	Not used
H	L	H	Erase mode: The word stored at the addressed location is erased The data bits after erasing are all low-level
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse The address is designated by two one-of-eight-coded digits. 64-word address is assigned in this mode.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
Tstg	Storage temperature		−40 ~ 125	℃
Topr	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{GG}-V_{SS}$	Supply voltage	−32.2	−35	−37.8	V
$V_{SS}-V_{GND}$	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

ELECTRICAL CHARACTERISTICS (Ta = − 10～70℃, V_{GG}-V_{SS} = −35V ± 8 %, V_{SS}-V_{GND} = 5 V $^{+20\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		V_{SS}-6.5		V_{SS}-4.25	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	V_I-V_{SS} = −6.5V	−10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		kΩ
I_{OZL}	Off-state output current, low-level voltage applied	V_O-V_{SS} = −6.5V	−10		+10	μA
V_{OH}	High-level output voltage	I_{OH} = −200μA	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	I_{OL} = 80μA			V_{GND}+0.5	V
I_{GG}	Supply current from V_{GG}	I_O = 0μA		5.5	8.8	mA

Note 1: Typical values are at Ta = 25°C and V_{GG}-V_{SS} = -35V.

TIMING REQUIREMENTS (Ta = − 10～70℃, V_{GG}-V_{SS} = −35V ± 8 %, V_{SS}-V_{GND} = 5V $^{+20\%}_{-5\%}$, unless otherwise noted)

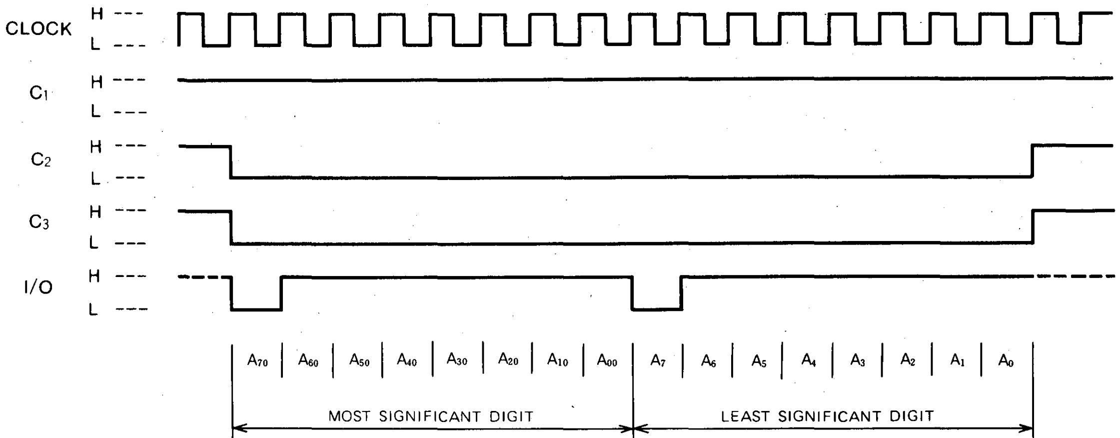
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T_{(\phi)}$	Clock period				300	μs
t_W	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{SU}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{SS}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS (Ta = − 10～70℃, V_{GG} = −35V ± 8 %, unless otherwise noted)

Symbol	Parameter	Alternative symbols	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
ta(c)	Read access time	t_{PW}	C_L = 100pF, $V_{OH} = V_{SS} - 2V$, $V_{OL} = V_{GND} + 1.5V$			20	μs
ts	Unpowered nonvolatile data retention time	T_S	$N_{EW} = 10^4$, $t_{W(W)}$ = 20ms, $t_{W(E)}$ = 20 ms	10			Year
		T_S	$N_{EW} = 10^5$, $t_{W(W)}$ = 20ms, $t_{W(E)}$ = 20 ms	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number pF read access unrefreshed	N_{RA}		10^9			Times
tdv	Data valid time	t_{PW}				20	μs

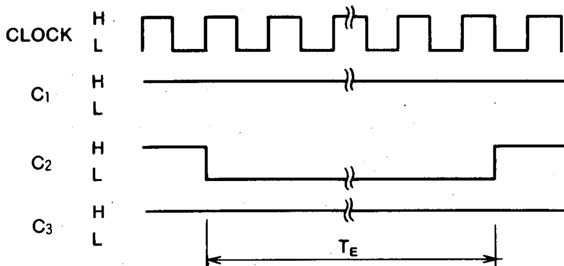
TIMING DIAGRAM

Accept Address Mode (16 clocks) $\overline{CS}$: L

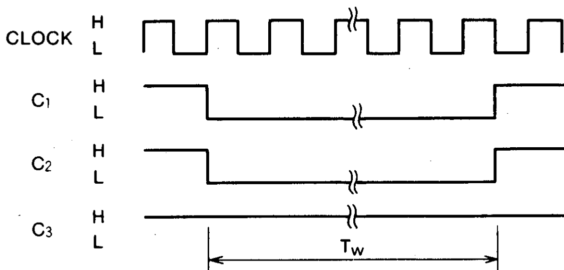


Note 2: The addresses from A_{00} to A_{77} are designated by two one-of-eight coded digits. The above figure shows designation of address A_{77}

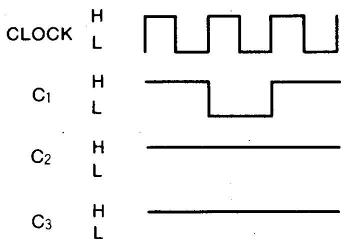
Erase Mode $\overline{CS}$: L



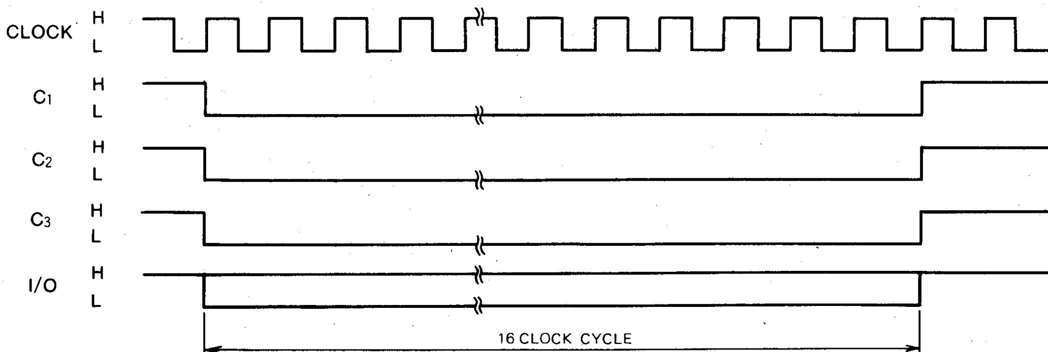
Write Mode $\overline{CS}$: L



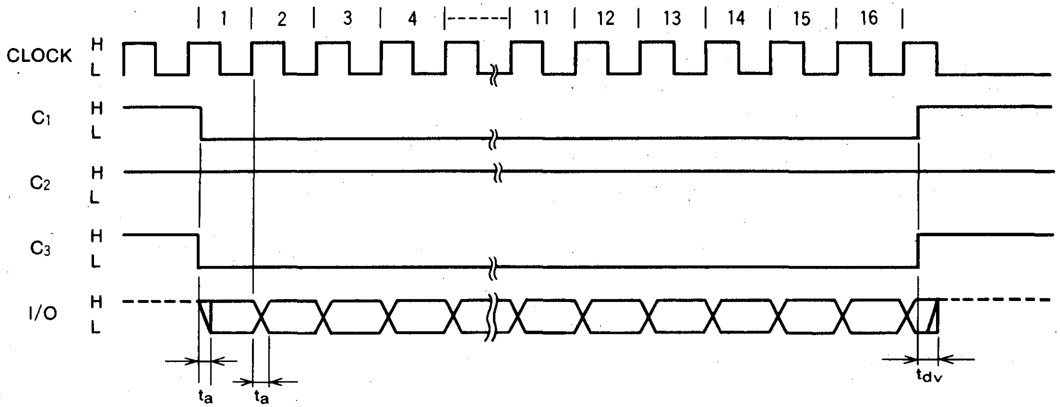
Read Mode (1 clock) $\overline{CS}$: L



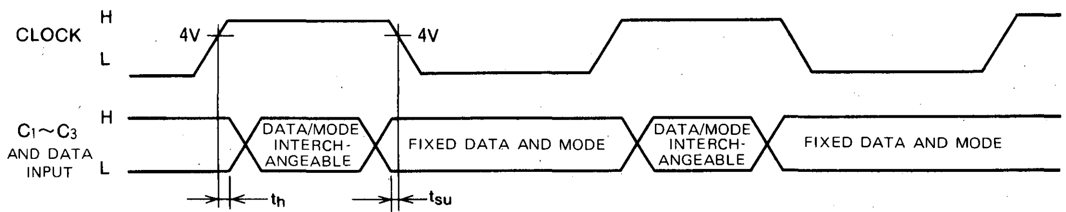
Accept Data (16 clocks) $\overline{CS}$: L



Shift Data Output Mode (16 clocks) $\overline{CS}$: L

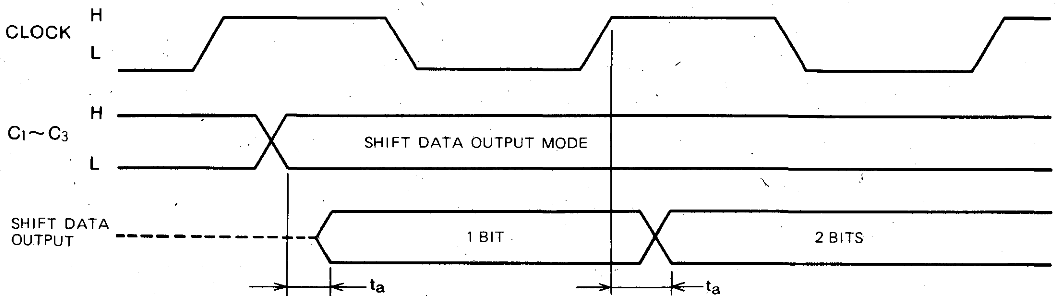


Timing of clock, C_1, C_2, C_3, and data input



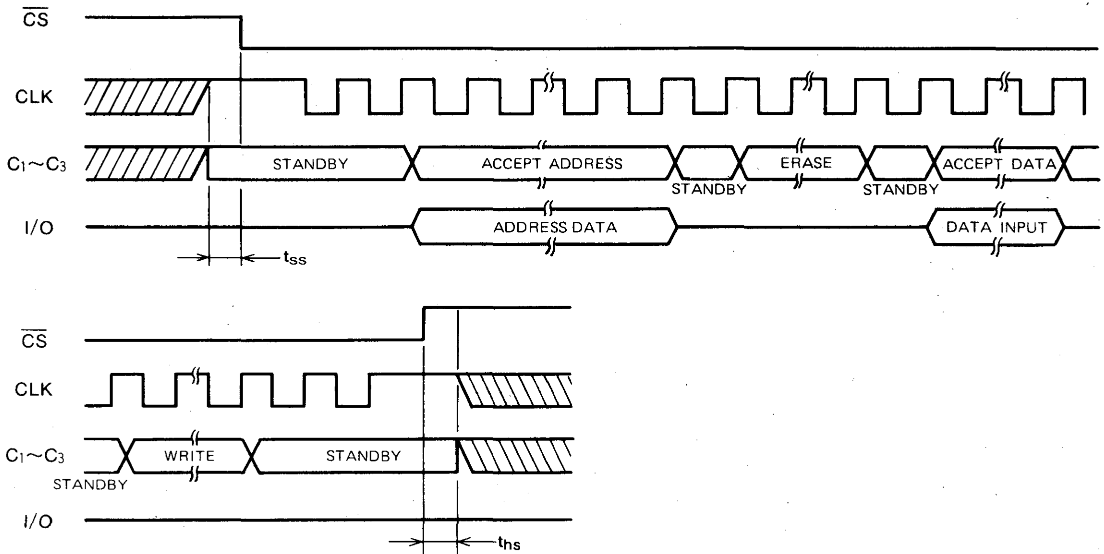
Note 3: C_1 ~ C_3 and accept data are interchnageable while the clock is set high.

Timing of clock, C_1, C_2, C_3, and data input



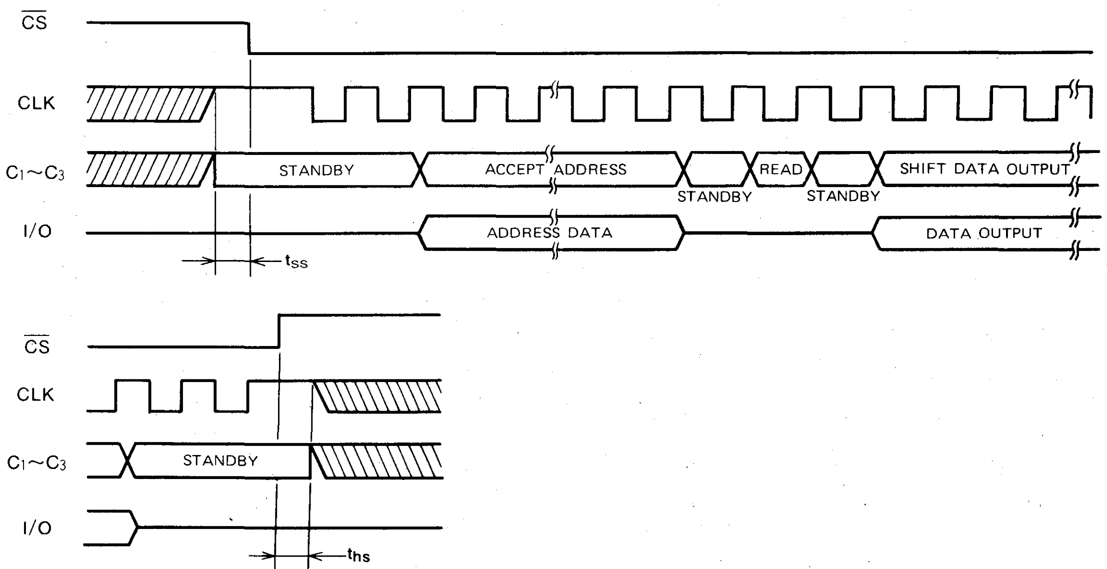
Operation flowchart

Rewriting flowchart



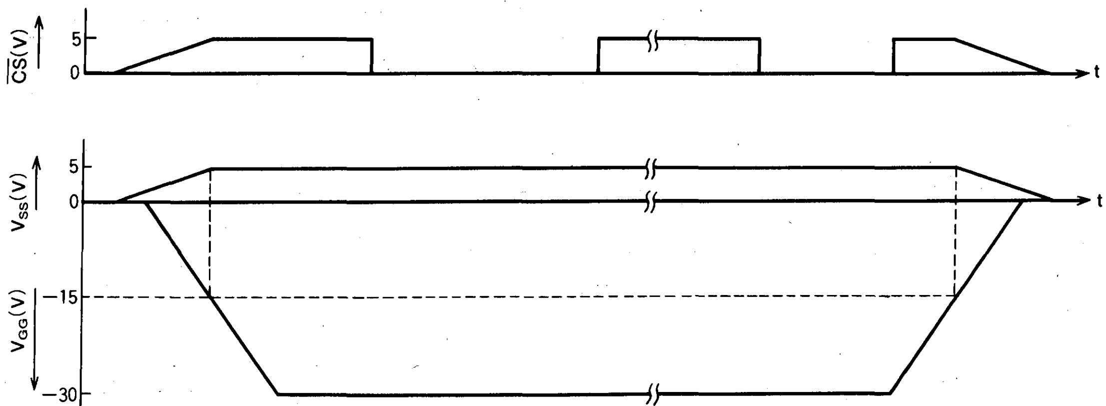
Note 4: One or more clock are required for standby between modes.
5: Set $\overline{CS}$ to the low level after the lapse of t_{SS} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
6: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs}.

Read Flowchart

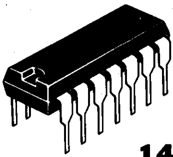


Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied. With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.



M58657P



1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58657P is a serial input/output 1400 bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time . . . . 20ms word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

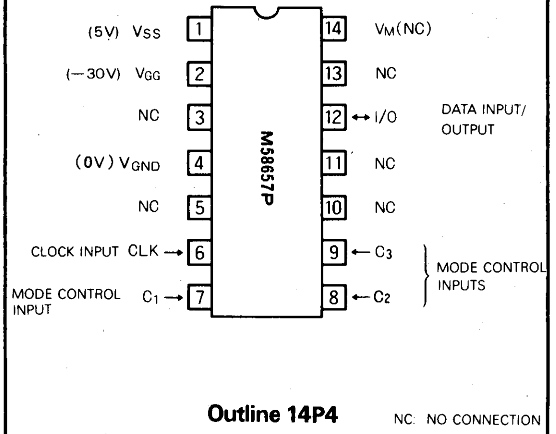
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

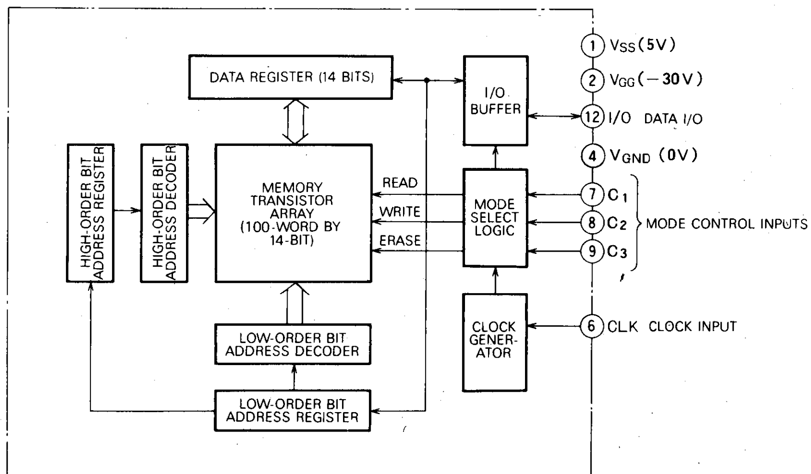
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

BLOCK DIAGRAM



1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to −30V.
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.
V_{GND}	Ground voltage	Connected to ground (OV)

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
T_{stg}	Storage temperature		−40 ~ 125	℃
T_{opr}	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{GG}-V_{SS}$	Supply voltage	−32.2	−35	−37.8	V
$V_{SS}-V_{GND}$	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

Note 1:
The order of V_{SS} V_{GG} with on or off.
With on, V_{GG} is turned on after V_{SS} is done.
With off, V_{SS} is turned off after V_{GG} is done.

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ 70℃, $V_{GG}-V_{SS}$ = −35V ± 8 %, $V_{SS}-V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		$V_{SS}-6.5$		$V_{SS}-4.25$	V
I_{IL}	Low-level input current	$V_I-V_{SS}=-6.5V$			±10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$V_O-V_{SS}=-6.5V$			±10	μA
V_{OH}	High-level output voltage	$I_{OH}=-200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL}=10\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O=0\mu A$		5.5	8.8	mA

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

TIMING REQUIREMENTS (Ta = −10 ~ 70℃, $V_{GG}-V_{SS}$ = −35V ± 8 %, $V_{SS}-V_{GND}$ = 5V $^{+20\%}_{-5\%}$, unless otherwise noted.)

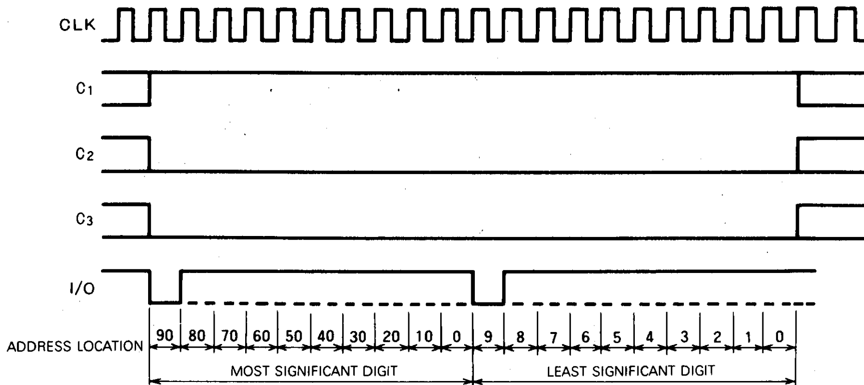
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
f(φ)	Clock frequency	fφ		10	14	17	kHz
D(φ)	Clock duty cycle	Dφ		30	50	55	%
$t_{w(W)}$	Write time	tw		16	20	24	ms
$t_{w(E)}$	Erase time	te		16	20	24	ms
t_r, t_f	Risetime, falltime	tr, tf				1	μs
$t_{su(c-\phi)}$	Control setup time before the fall of the clock pulse	t_{CS}		0			ns
$t_{h(\phi-c)}$	Control hold time after the rise of the clock pulse	t_{CH}		0			ns

SWITCHING CHARACTERISTICS (Ta = −10 ~ 70℃, V_{GG} = −35V ± 8 %, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(c)}$	Read access time	t_{PW}	C_L = 100pF, $V_{OH}=V_{SS}-2V$, $V_{OL}=V_{GND}+1.5V$			20	μs
t_s	Unpowered nonvolatile data retention time	T_S	$N_{EW}=10^4$, $t_{w(W)}$ = 20ms, $t_{w(E)}$ = 20ms	10			Year
		T_S	$N_{EW}=10^5$, $t_{w(W)}$ = 20ms, $t_{w(E)}$ = 20ms	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

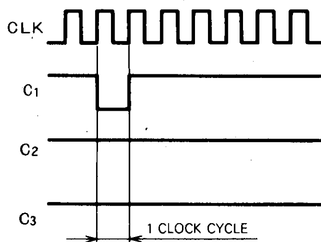
TIMING DIAGRAM

Accept Data Mode

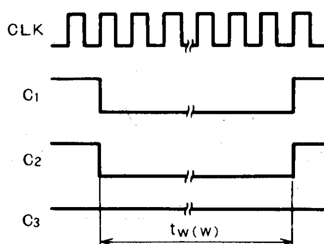


Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 99.

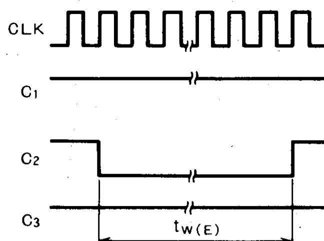
Read Mode



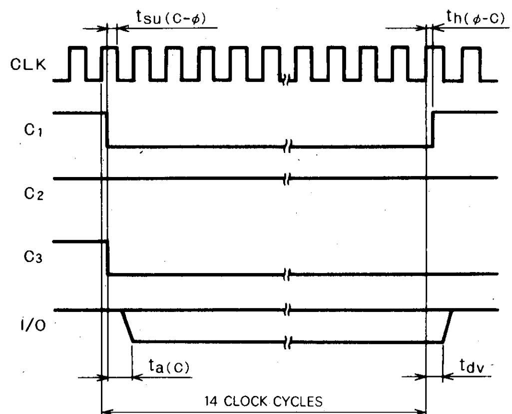
Write Mode



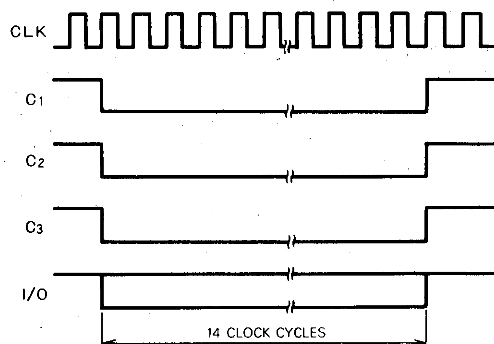
Erase Mode



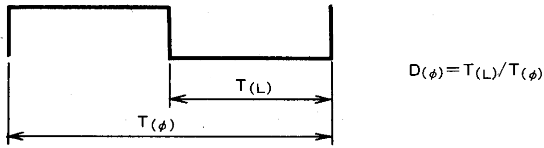
Shift Data Output Mode



Accept Data Mode



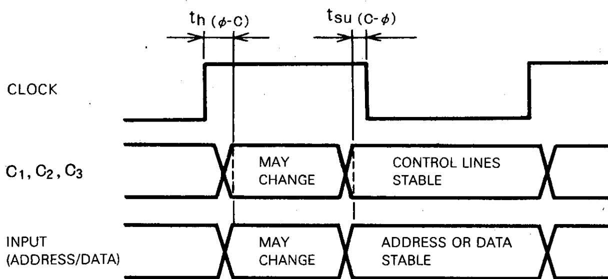
The difinition of clock duty cycle, D (ϕ)



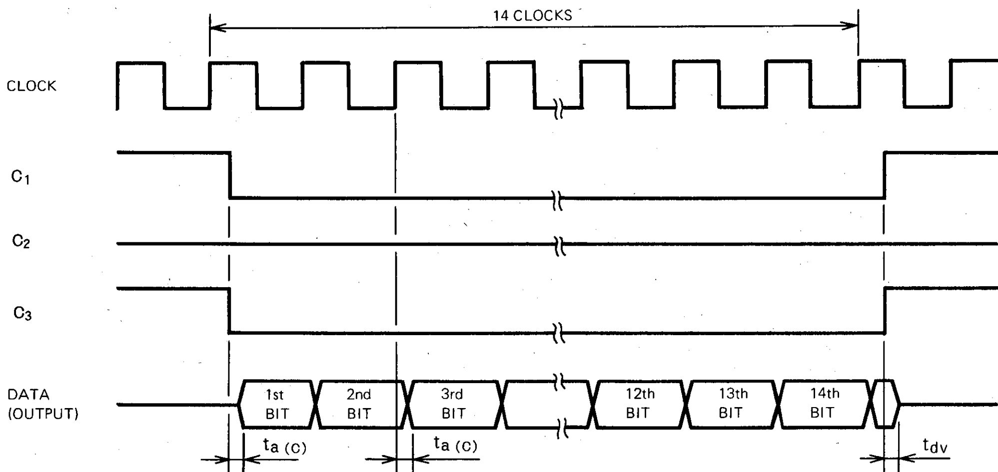
$D(\phi) = T(L)/T(\phi)$

Timing of data input and mode control inputs

Mode control inputs, C_1, C_2, C_3 and input signal my change, when clock is 'H' level.



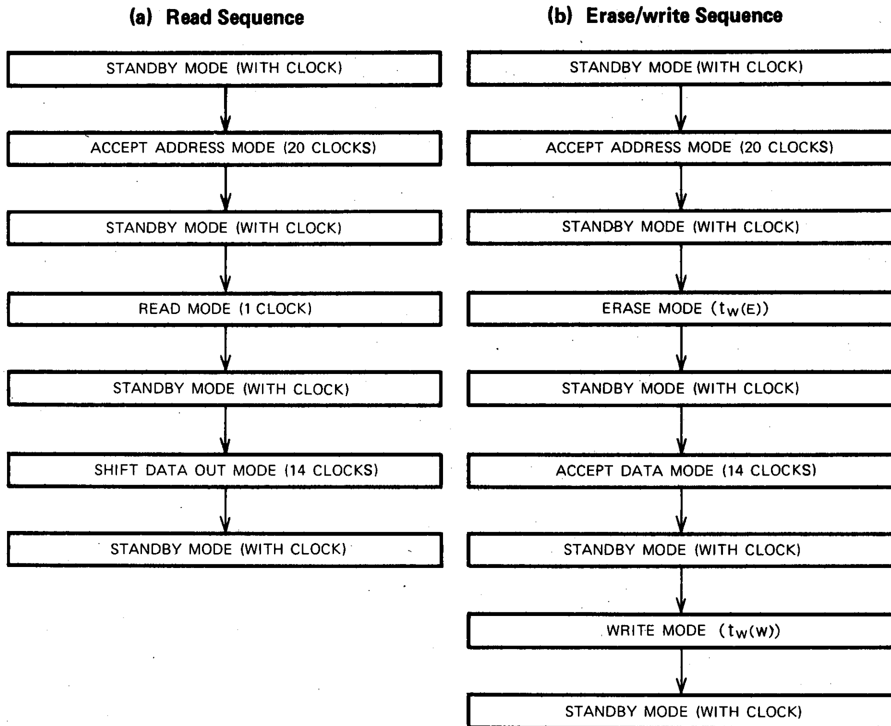
Timing of data output



The 1st bit of output data is output after access time of $t_{a(C)}$ from the mode control transition. And other bits are output after $t_{a(C)}$ from positive edge of clock.

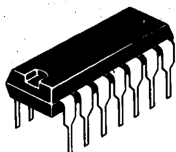
1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

Operating sequential flow



MITSUBISHI ELECTRIC

M58658P



320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58658P is a serial input/output 320 bit electrically erasable and reprogrammable ROM organized as 20 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time . . . . 20ms word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

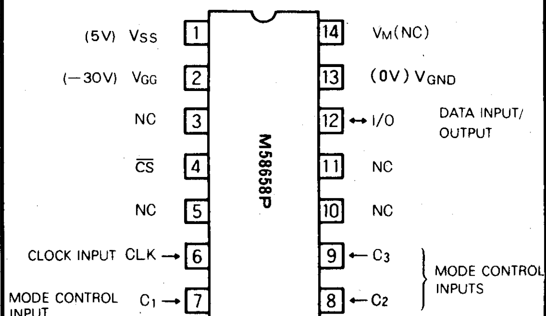
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

The address is designated by two consecutive one-of-four coded digits. Eight modes—accept address, AD accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the $SiO_2-Si_3N_4$ interface of the gate insulators of the MNOS memory transistors.

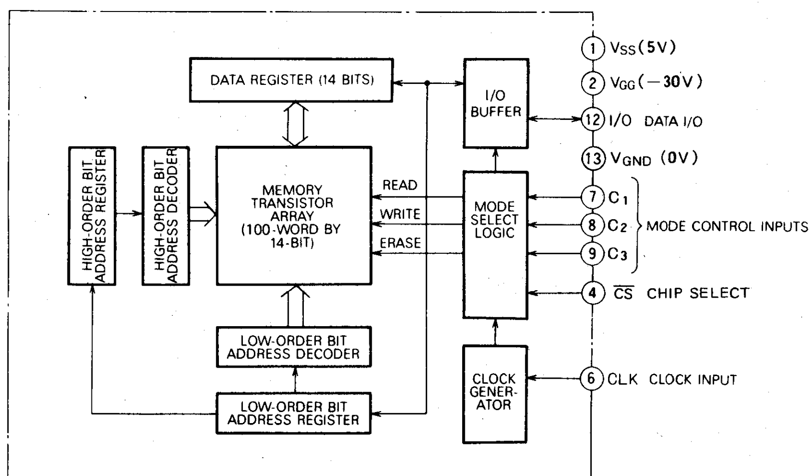
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

BLOCK DIAGRAM



320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address AD accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to −30V.
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.
V_{GND}	Ground voltage	Connected to ground (OV)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C1	C2	C3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged The output buffer is held in the floating state.
H	H	L	Additional data (AD) accept address: Data presented at the I/O pin is shifted into the AD address registers one bit with each clock pulse. The address is designated by two one-of-four coded digits. 4-word address is assigned in this mode.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-four-coded digits. 16-word address is assigned in this mode.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
Tstg	Storage temperature		−40 ~ 125	℃
Topr	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{GG}-V_{SS}$	Supply voltage	−32.2	−35	−37.8	V
$V_{SS}-V_{GND}$	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

ELECTRICAL CHARACTERISTICS ($Ta = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		V_{SS}-6.5		V_{SS}-4.25	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	$V_I-V_{SS}=-6.5V$	−10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		kΩ
I_{OZL}	Off-state output current, low-level voltage applied	$V_O-V_{SS}=-6.5V$	−10		+10	μA
V_{OH}	High-level output voltage	$I_{OH}=-200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL}=10\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O=0\mu A$		5.5	8.8	mA

Note 1: Typical values are at Ta = 25°C and V_{GG}-V_{SS} = -35V.

TIMING REQUIREMENTS ($Ta = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted.)

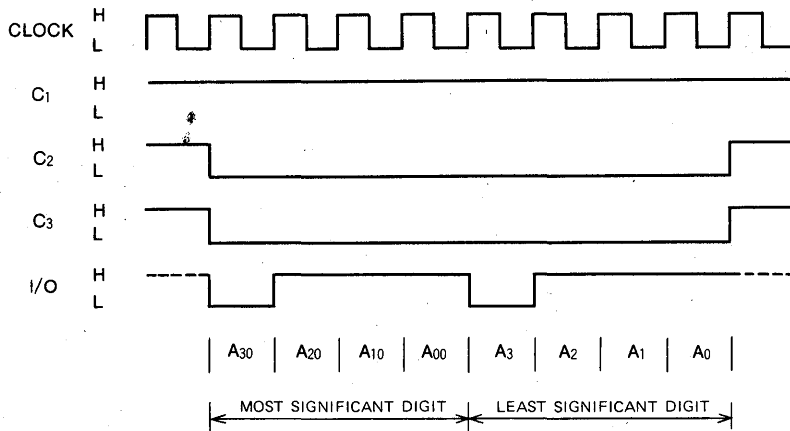
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T_{(\phi)}$	Clock period				300	μs
t_W	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{su}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{ss}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS ($Ta = -10 \sim 70°C$, $V_{GG} = -35V \pm 8\%$, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
ta(c)	Read access time	t_{PW}	$C_L = 100pF$, $V_{OH}=V_{SS}-2V$, $V_{OL}=V_{GND}+1.5V$			20	μs
ts	Unpowered nonvolatile data retention time	T_S	$N_{EW}=10^4$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$	10			Year
		T_S	$N_{EW}=10^5$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

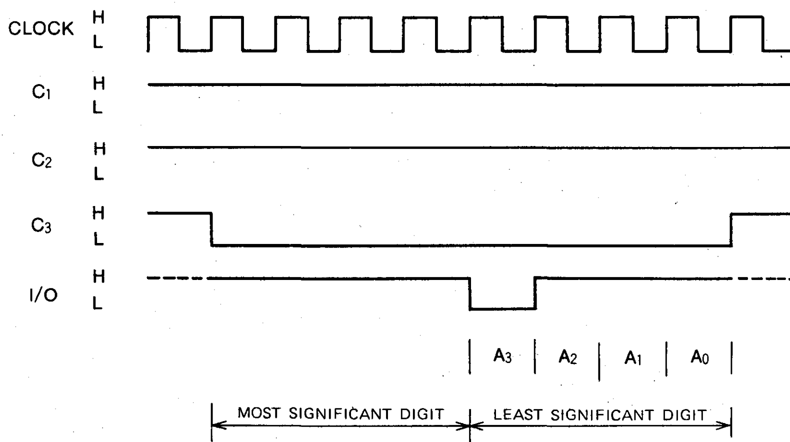
TIMING DIAGRAM

Accept Address Mode (8 clocks) $\overline{CS}$: L



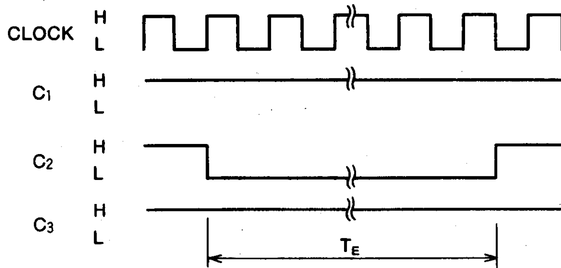
Note 2: The addresses from A_{00} to A_{33} are designated by two one-of-four coded digits. The above figure shows designation of address A_{33} (decimal address 15).

AD Accept Address Mode (8 clocks) $\overline{CS}$: L

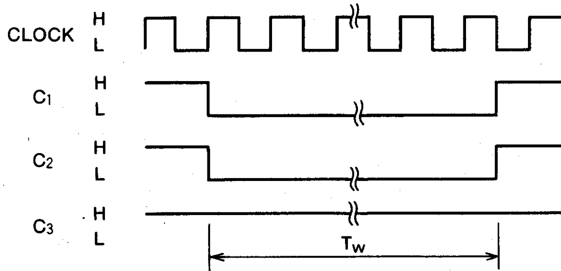


Note 3: In the AD accept address mode, the higher four are set high, and the lower four digits are designated by one of the four coded digits. This address mode allows designation of addresses from A_0 to A_3. Each address has a 16 bits. The above figure shows designation of address A_3.

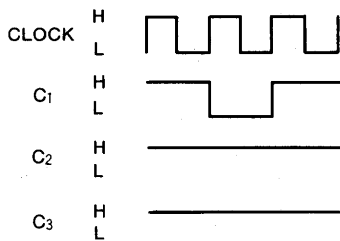
Erase Mode $\overline{CS}$: L



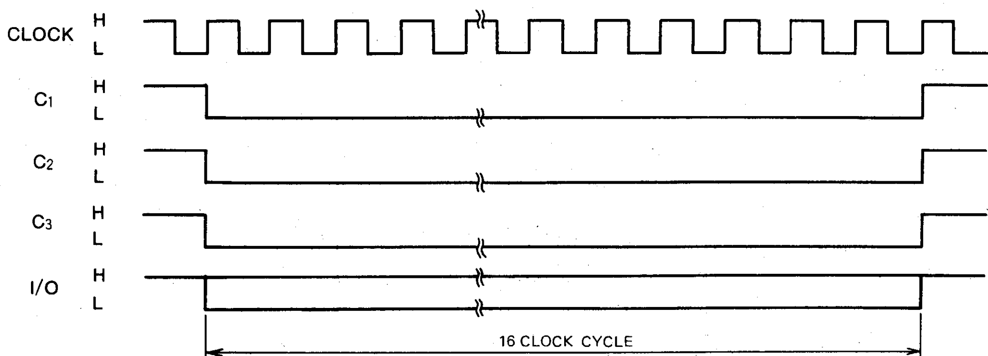
Write Mode $\overline{CS}$: L



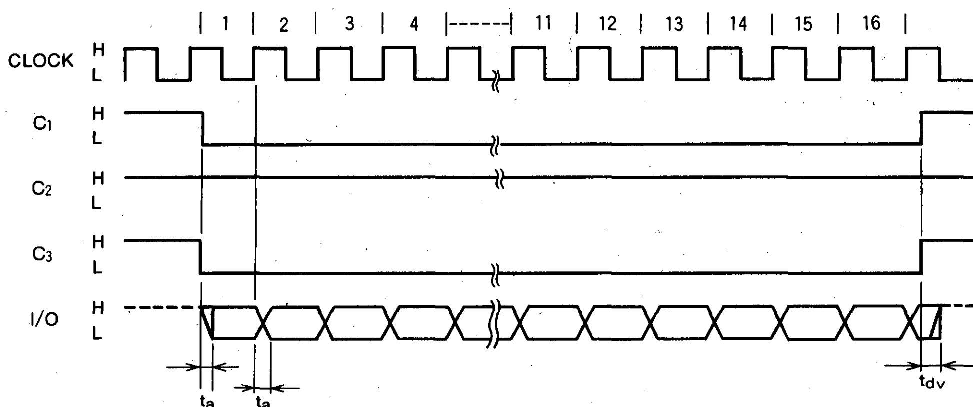
Read Mode (1 clock) $\overline{CS}$: L



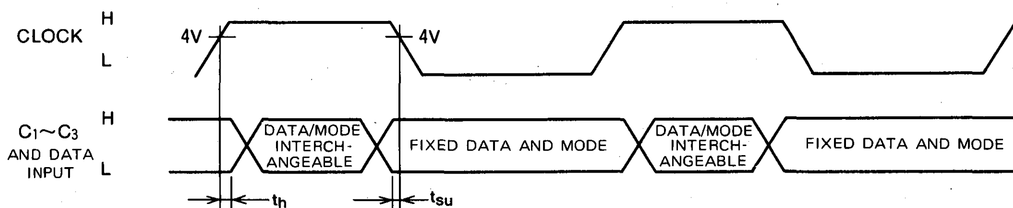
Accept Data (16 clocks) $\overline{CS}$: L



Shift Data Output Mode (16 clocks) $\overline{CS}$: L

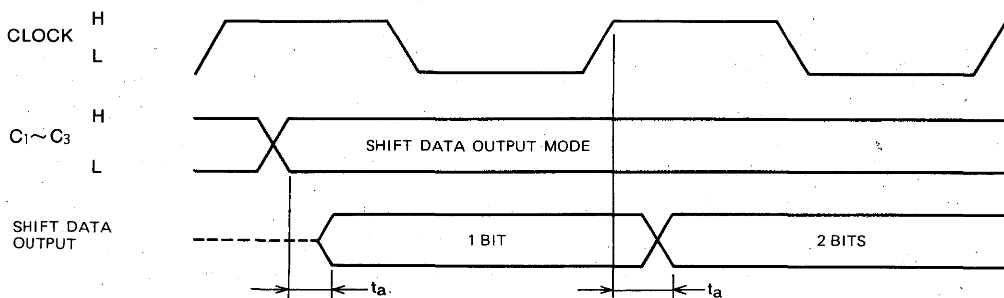


Timing of clock, C_1, C_2, C_3, and data input



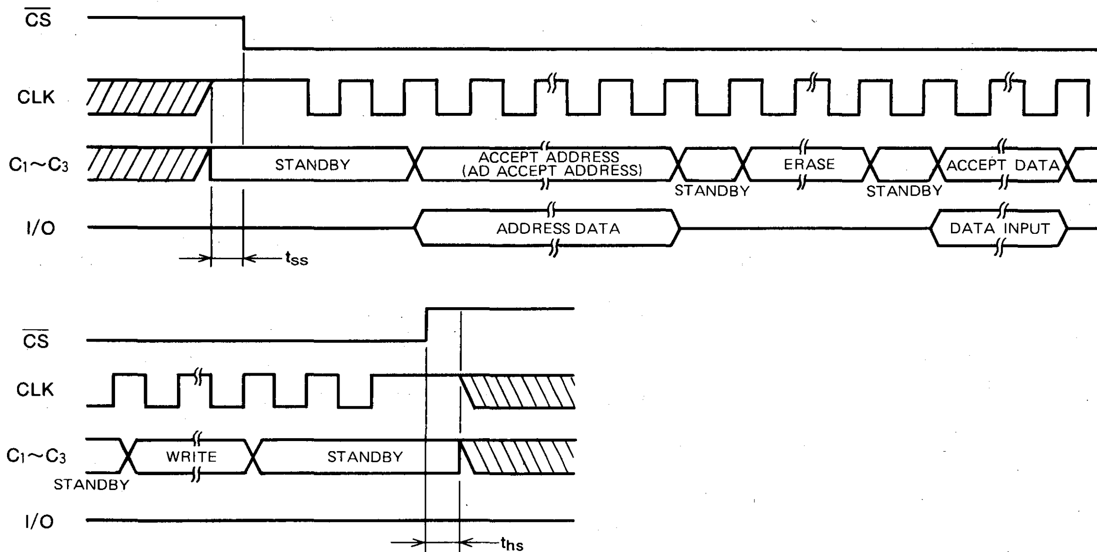
Note 4: $C_1 \sim C_3$ and accept data (AD accept data) are interchnageable while the clock is set high.

Timing of clock, C_1, C_2, C_3, and data input



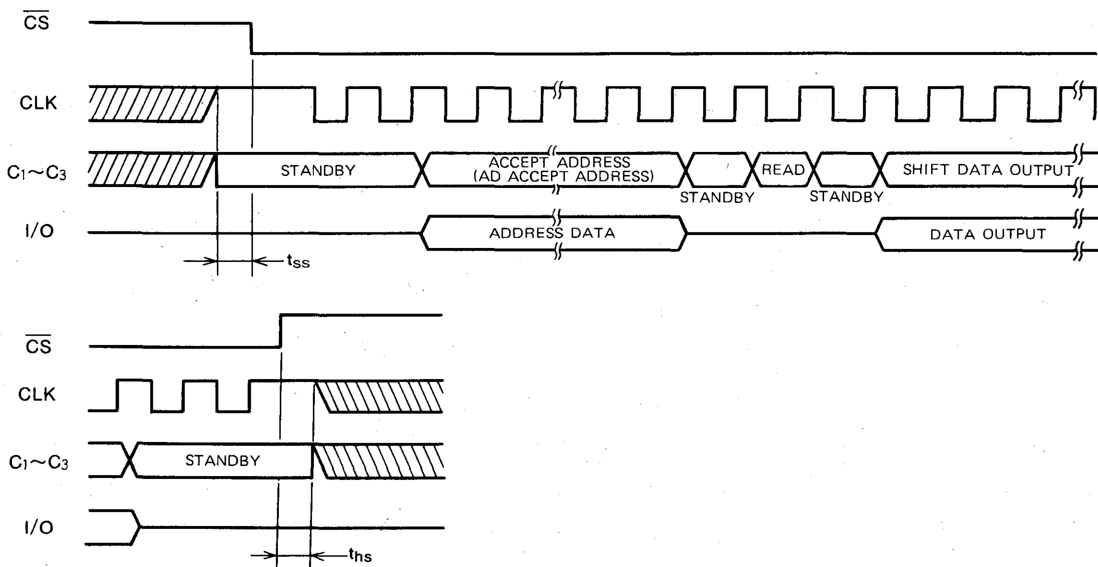
Operation flowchart

Rewriting flowchart



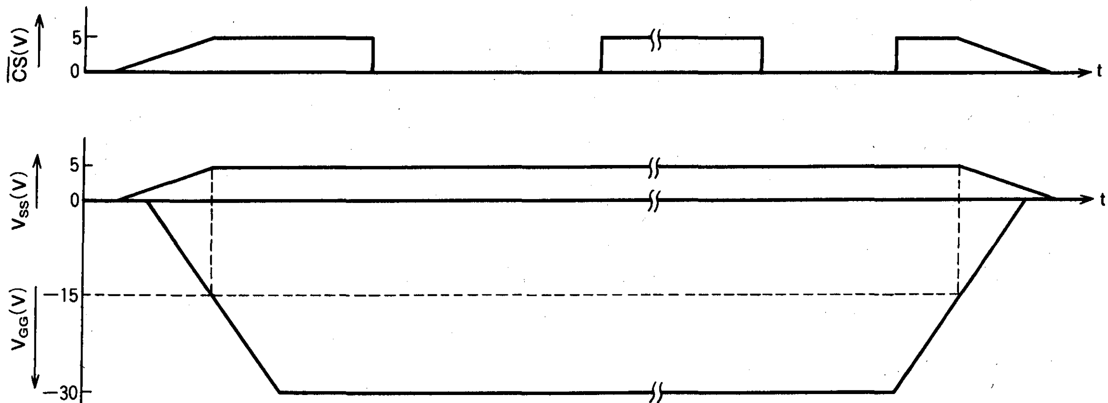
Note 5: One or more clock are required for standby between modes.
6: Set $\overline{CS}$ to the low level after the lapse of t_{SS} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
7: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs}.

Read Flowchart

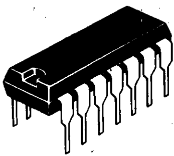


Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied. With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.



MITSUBISHI ELECTRIC



M58659P

512-BIT(32-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58659P is a serial input/output 512 bit electrically erasable and reprogrammable ROM organized as 32 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time . . . . 20ms word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

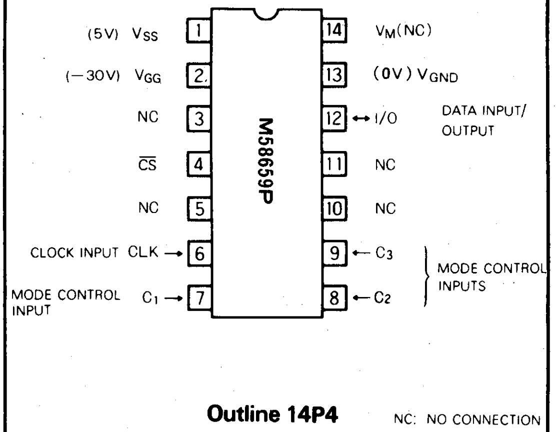
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

The address is designated by one-of-four and one-of-eight coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

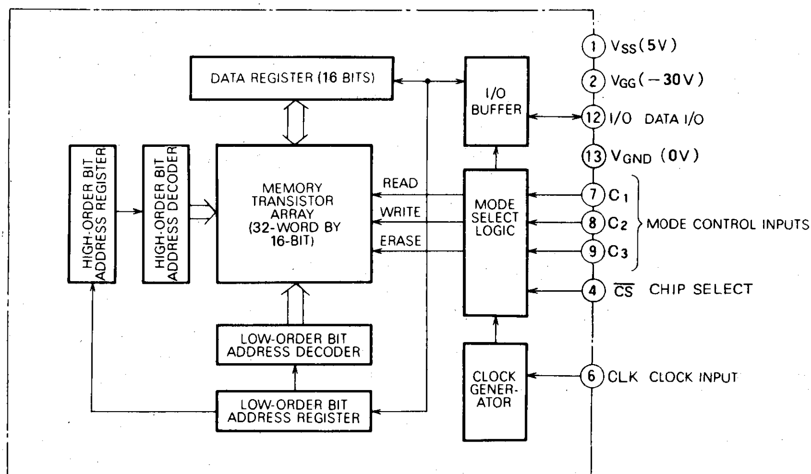
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

BLOCK DIAGRAM



512-BIT(32-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation
V_{SS}	Chip substrate voltage	Normally connected to +5V
V_{GG}	Power supply voltage	Normally connected to −30V
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode
V_{GND}	Ground voltage	Connected to ground (OV)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state
H	H	L	Not used
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by one-of-four and one-of-eight-coded digits. 32-word address is assigned in this mode.
L	H	H	Read mode: The addressed word is read from the memory into the data register
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
Tstg	Storage temperature		−40 ~ 125	℃
Topr	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}-V_{SS}	Supply voltage	−32.2	−35	−37.8	V
V_{SS}-V_{GND}	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

ELECTRICAL CHARACTERISTICS ($Ta = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		V_{SS}-6.5		V_{SS}-4.25	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	$V_I-V_{SS}=-6.5V$.	−10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		kΩ
I_{OZL}	Off-state output current, low-level voltage applied	$V_O-V_{SS}=-6.5V$	−10		+10	μA
V_{OH}	High-level output voltage	$I_{OH}=-200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL}=80\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O=0\mu A$		5.5	8.8	mA

Note 1: Typical values are at Ta = 25°C and $V_{GG}-V_{SS}$ = -35V.

TIMING REQUIREMENTS ($Ta = -10 \sim 70°C$, $V_{GG}-V_{SS} = -35V \pm 8\%$, $V_{SS}-V_{GND} = 5V {}^{+20\%}_{-5\%}$, unless otherwise noted.)

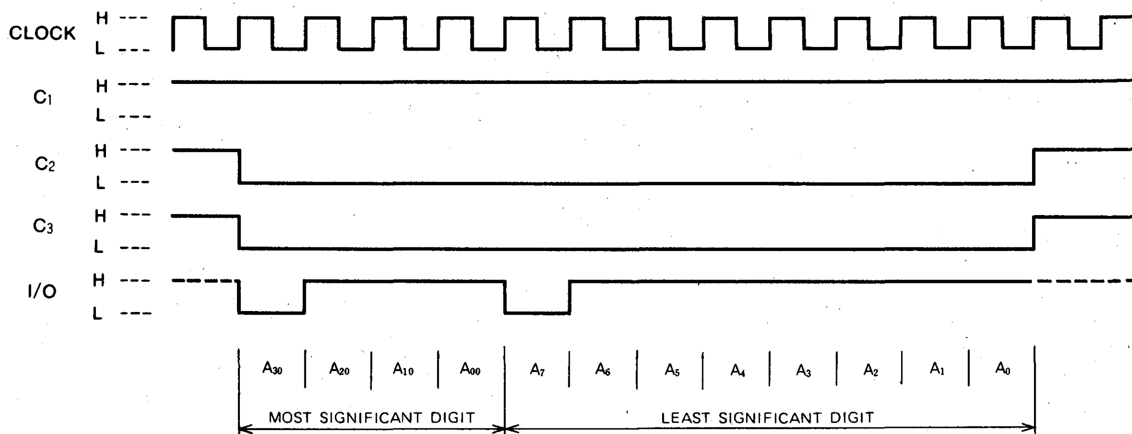
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T_{(\phi)}$	Clock period				300	μs
t_W	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{su}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{ss}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS ($Ta = -10 \sim 70°C$, $V_{GG} = -35V \pm 8\%$, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
ta(c)	Read access time	t_{PW}	$C_L = 100pF$ $V_{OH}=V_{SS}-2V$ $V_{OL}=V_{GND}+1.5V$			20	μs
t_S	Unpowered nonvolatile data retention time	T_S	$N_{EW}=10^4$, $t_{W(W)}=20ms$ $t_{W(E)}=20ms$	10			Year
		T_S	$N_{EW}=10^5$, $t_{W(W)}=20ms$ $t_{W(E)}=20ms$	1			Year
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

TIMING DIAGRAM

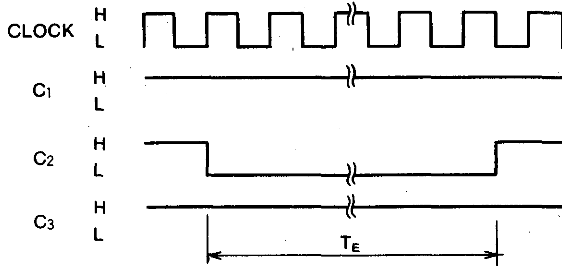
Accept Address Mode (12 clocks) $\overline{CS}$: L



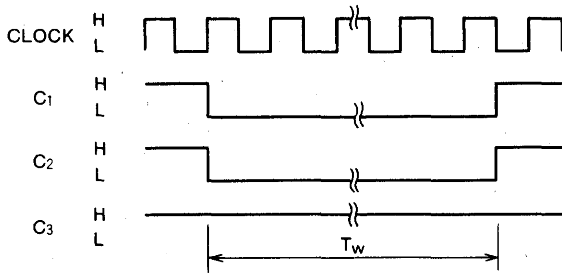
Note 2: The addresses from A_{00} to A_{37} are designated by one-of-four and one-of-eight coded digits. The above figure shows designation of address A_{37}

MITSUBISHI ELECTRIC

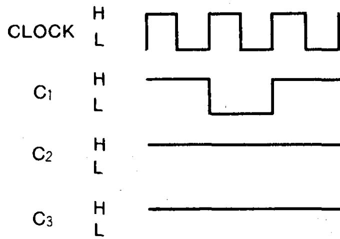
Erase Mode $\overline{CS}$: L



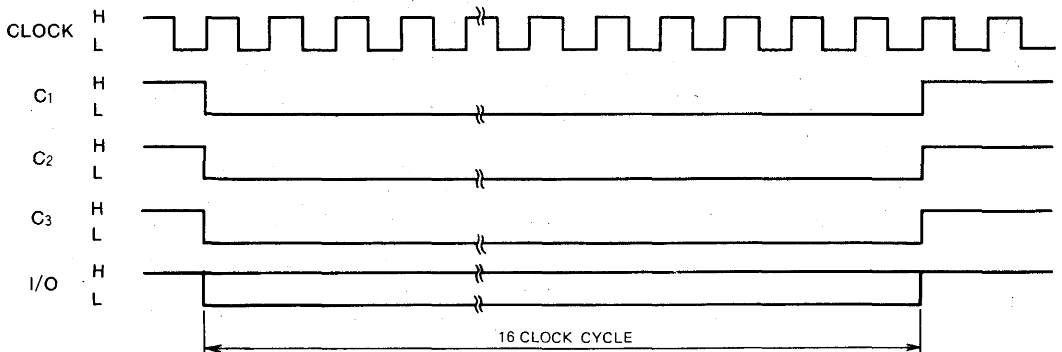
Write Mode $\overline{CS}$: L



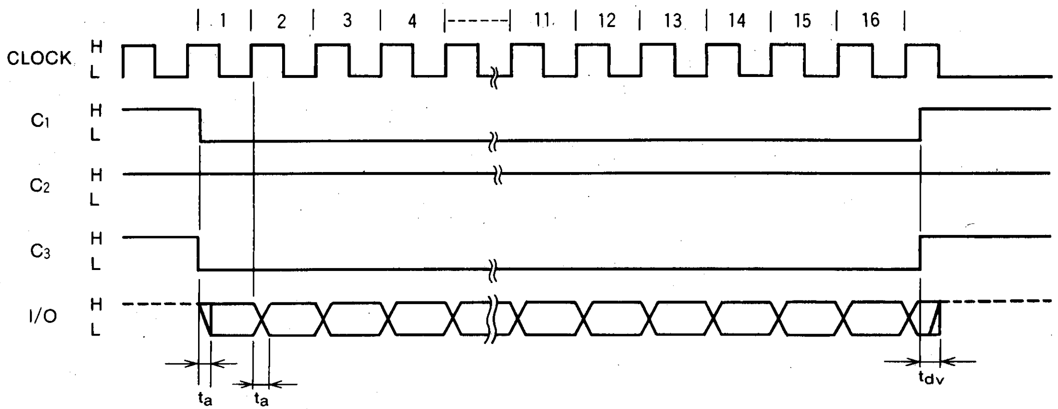
Read Mode (1 clock) $\overline{CS}$: L



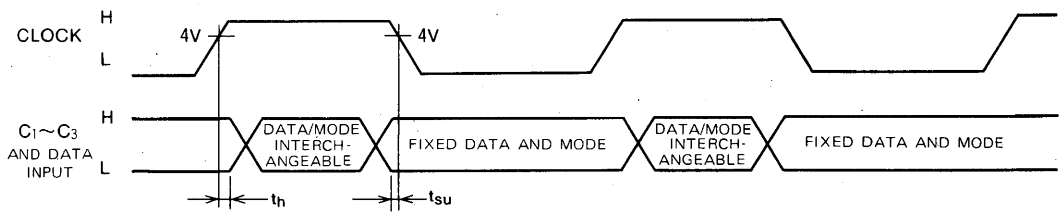
Accept Data (16 clocks) $\overline{CS}$: L



Shift Data Output Mode (16 clocks) $\overline{CS}$: L

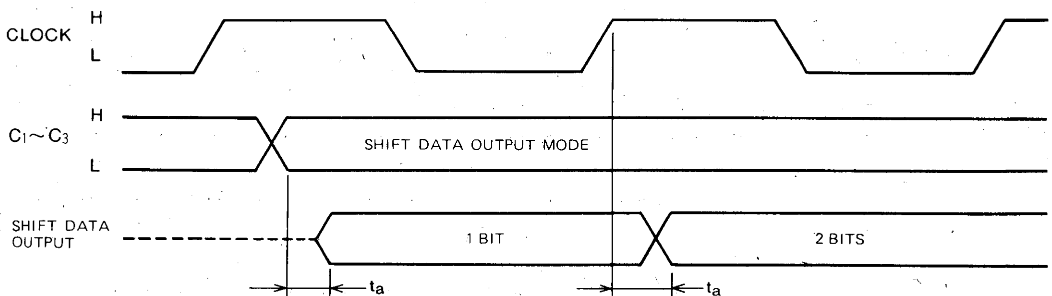


Timing of clock, C_1, C_2, C_3, and data input



Note 3: C_1 ~ C_3 and accept data are interchnageable while the clock is set high.

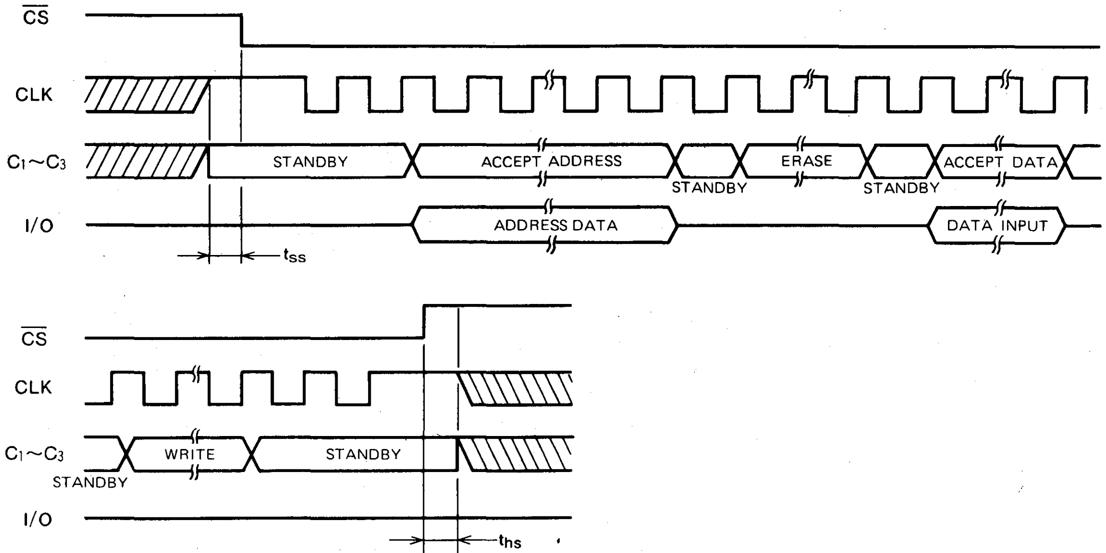
Timing of clock, C_1, C_2, C_3, and data input



MITSUBISHI
ELECTRIC

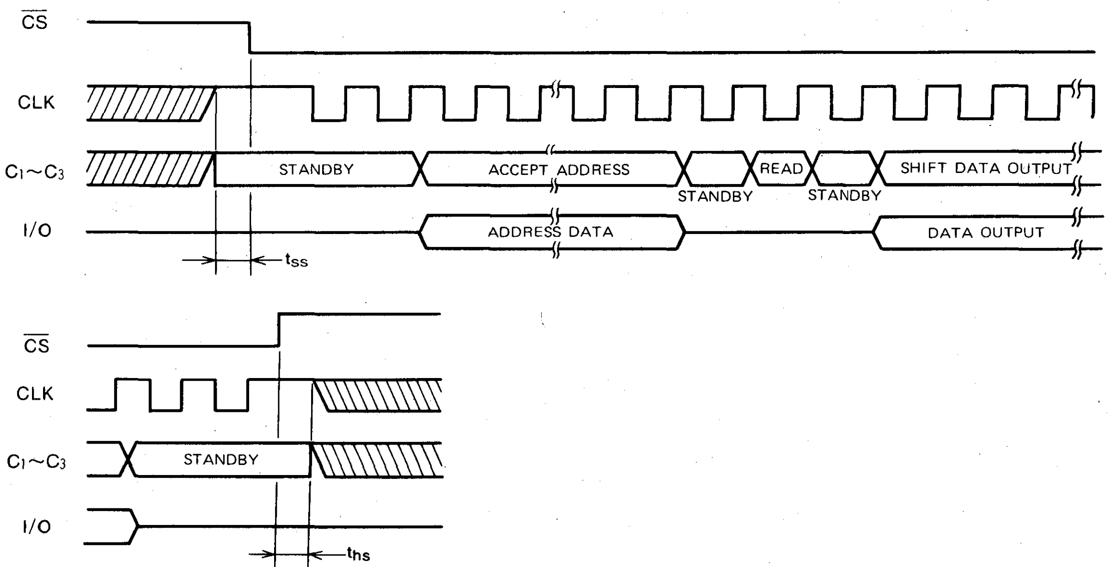
Operation flowchart

Rewriting flowchart



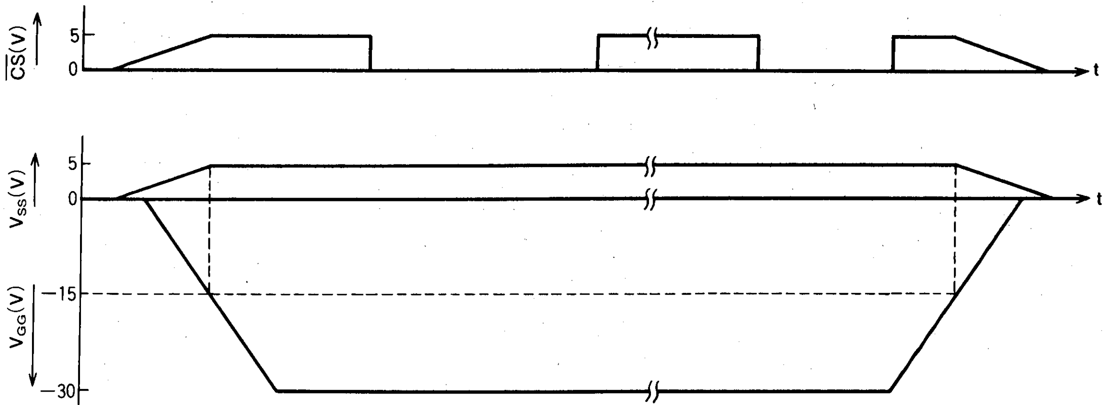
Note 4: One or more clock are required for standby between modes.
5: Set $\overline{CS}$ to the low level after the lapse of t_{SS} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
6: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs}.

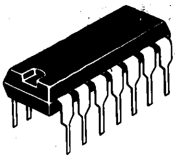
Read Flowchart



Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied. With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.





M5G1400P

1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

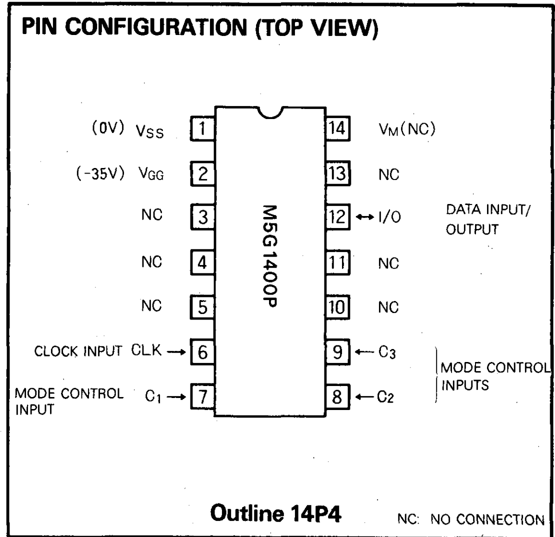
DESCRIPTION
The M5G1400P is a serial input/output 1400-bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES
- Word-by-word electrically alterable
- Non-volatile data storage: .... 10 years (min)
- Write/erase time: 20ms/word
- Single 35V power supply
- Number of erase-write cycles: .... 10^5 times (min)
- Number of read access unrefreshed:···· 10^9 times (min)
- Interchangeable with GI's ER1400 in pin configuration and electrical characteristics

APPLICATION
Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

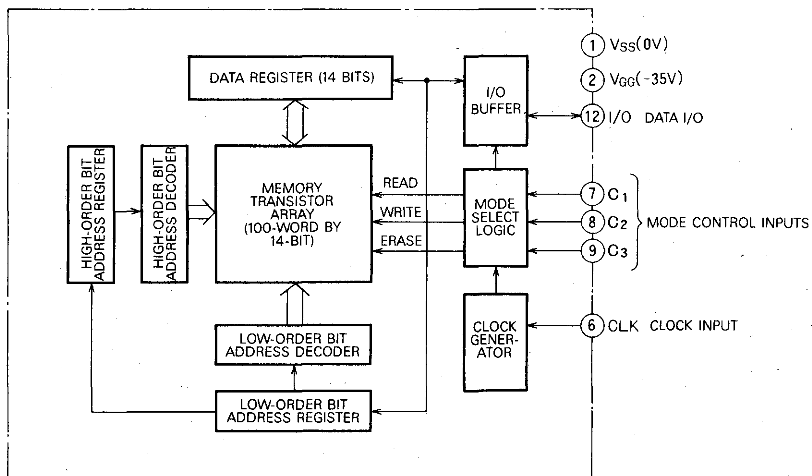
FUNCTION
The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4   NC: NO CONNECTION

BLOCK DIAGRAM



1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to ground.
V_{GG}	Power supply voltage	Normally connected to −35V.
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3～−40	V
V_I	Input voltage		0.3～−20	V
V_O	Output voltage		0.3～−20	V
Tstg	Storage temperature		−65～150	℃
Topr	Operating temperature		−10～70	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−10～70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−32.2	−35	−37.8	V
V_{SS}	Supply voltage (GND)		0		V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-15$		$V_{SS}-8$	V

Note 1:
The order of V_{SS} V_{GG} with on or off.
With on, V_{GG} is turned on after V_{SS} is done.
With off, V_{SS} is turned off after V_{GG} is done.

ELECTRICAL CHARACTERISTICS (Ta=−10～70℃, V_{GG}=−35V± 8%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		$V_{SS}-15$		$V_{SS}-8$	V
I_{IL}	Low-level input current	$V_I=-15V$			±10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$V_O=-15V$			±10	μA
V_{OH}	High-level output voltage	$I_{OH}=-200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL}=10\mu A$			$V_{SS}-12$	V
I_{GG}	Supply current from V_{GG}	$I_O=0\mu A$		5.5	8.8	mA

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

TIMING REQUIREMENTS (Ta=−10～70℃, V_{GG}=−35V± 8%, unless otherwise noted.)

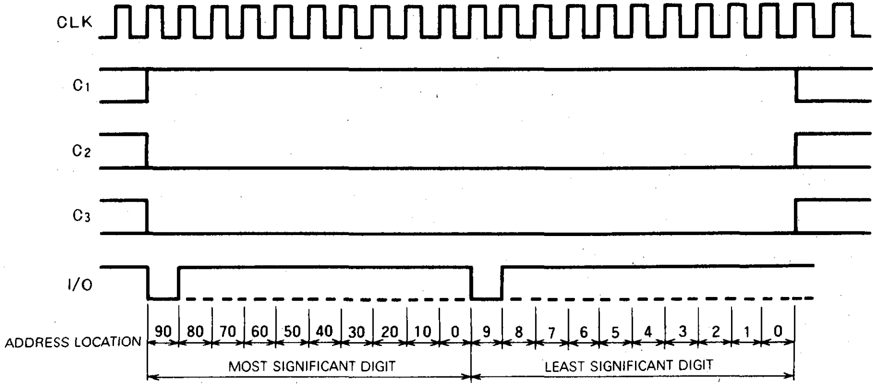
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
f(φ)	Clock frequency	fφ		11.2	14	16.8	kHz
D(φ)	Clock duty cycle	Dφ		30	50	55	%
tw(w)	Write time	tw		16	20	24	ms
tw(E)	Erase time	te		16	20	24	ms
tr, tf	Risetime, falltime	tr, tf				1	μs
tsu(c−φ)	Control setup time before the fall of the clock pulse	t_{CS}		0			ns
th(φ−c)	Control hold time after the rise of the clock pulse	t_{CH}		0			ns

SWITCHING CHARACTERISTICS (Ta=−10～70℃, V_{GG}=−35V± 8%, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
ta(c)	Read access time	t_{PW}	$C_L=100pF$ $V_{OH}=V_{SS}-2V$ $V_{OL}=V_{SS}-8V$			20	μs
ts	Unpowered nonvolatile data retention time	Ts	$N_{EW}=10^4$, tw(w)=20ms tw(E)=20ms	10			Year
		Ts	$N_{EW}=10^5$, tw(w)=20ms tw(E)=20ms	1			
N_{EW}	Number of erase/write cycles	Nw		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
tdv	Data valid time	t_{PW}				20	μs

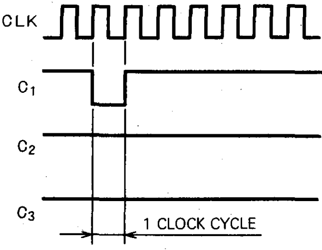
TIMING DIAGRAM

Accept Data Mode

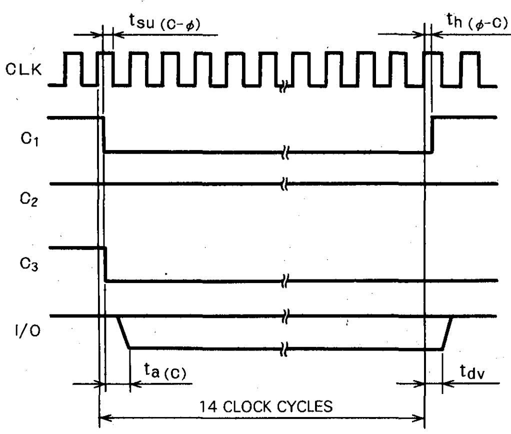


Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 99.

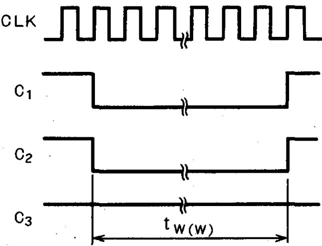
Read Mode



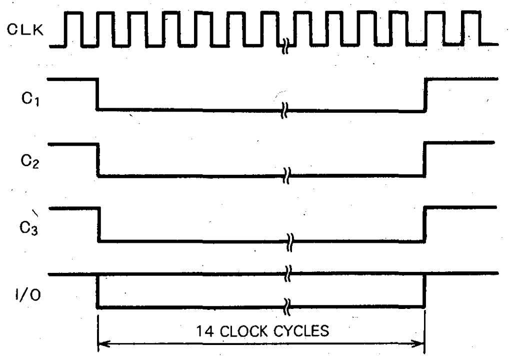
Shift Data Output Mode



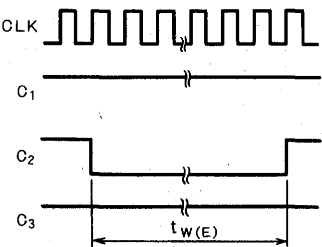
Write Mode



Accept Data Mode



Erase Mode



APPLICATIONS

10

64K, 256K-BIT DYNAMIC RAM

(M5K4164AP/M5K4164ANP)

APPLICATION OF 64K-BIT DYNAMIC RAM

Technology

Since the introduction of the 1K RAM in 1970, the development of dynamic RAM devices has progressed at a rate which has seen capacities multiplied by four in approximately two years, the latest stage of development being the 64K RAM.

Today's modern RAM devices take the user into consideration, and 64K dynamic RAMs which operate off a single 5V power supply are common.

We will describe here the new technology which made possible the development of a highly integrated, high-performance 64K RAM which operates from a single 5V supply.

1. Cell Structure and Process Technology

The M5K4164AP 64K RAM makes use of the same two-level n-channel polysilicon gate process and one-transistor cell structure used in the triple power supply 16K RAM (M5K4116P/S) which has been used in large quantities.

To achieve a high-density RAM, the masks are manufactured using electron beam technology.

In addition, the geometries on several critical levels of the M5K4164AP are 2.5 ~ 3.0μm, necessitating the use of positive photo-resist (for resolution and delineation control) as well as dry-plasma processing at these critical levels.

Fig. 1.1 shows the cross-section of the cell structure with Table 1.1 summarizing a comparison of the basic parameters of the device with the 16K RAM.

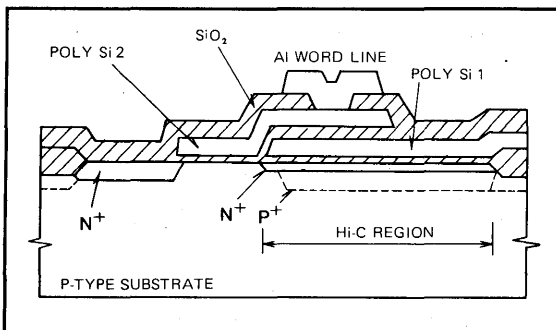


Fig. 1.1 Hi-C structure memory cell cross-section

Table 1.1 Main parameters

Parameter	16K RAM	64K RAM
Memory cell area	350 μm^2	143 μm^2
Chip area	16. 3mm^2	23. 9 μm^2
Available channel length	4 μm	2 μm
Gate oxide film	850 Å	400 Å
Diffusion layer depth	1. 0 μm	0. 4 μm
Diffusion layer width	4. 0 μm	2. 5 μm
Aluminum width	4. 0 μm	3. 0 μm

2. Substrate Bias Circuit

In order to facilitate the operation from a single 5V supply, the M5K4164AP makes use of an on-chip substrate bias circuit. This bias circuit consists of a ring oscillator, driver circuit, charge pump circuit, and decoupling capacitors. The circuit supplies a bias to the substrate of approximately −3.5V for V_{CC} = 5V (Refer to Fig. 1.2)

The substrate bias circuit has the following functions.

1) It prevents destruction of storage data and disturbance of bipolar transistor operation caused by input undershoot which causes an injection of electrons from the input terminals to the substrate.
2) A reduction in the capacitance of the pn junction formed by the substrate and internal circuit nodes enables an increase in circuit operation speed.
3) The transistor threshold voltage (V_{TH}) modulation due to a bias substrate is reduced, resulting in increased circuit operating speed and stability.

As shown in Fig. 1.3, the substrate bias for high values of V_{CC} is lower than for the standby mode due to the effect of increased impact ionization current. Adequate margin, however, is maintained against a value of V_{IL} min of −2V.

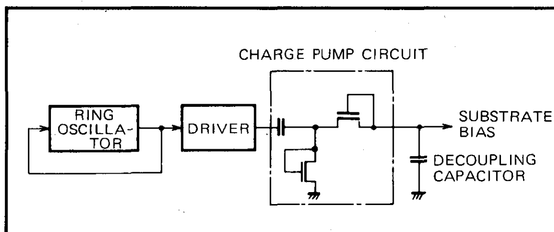


Fig. 1.2 Substrate bias circuit

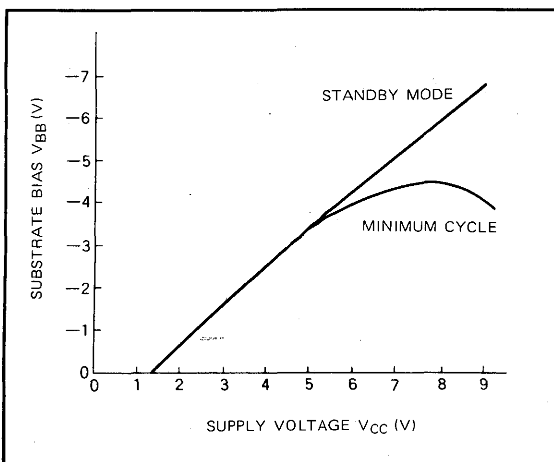


Fig. 1.3 Substrate bias vs supply voltage

3. Reduced Power Consumption and Noise

For operation from a 5V supply, it is necessary to reduce the transistor threshold voltage, V_{TH}. This, however, invites error operation due to noise. For this reason, circuits required to operate from low voltages only make use of transistors with a low V_{TH}, while those requiring noise immunity are implemented with transistors having a high value of V_{TH}. This scheme insures stable operation.

To lower the peak circuit current, a significant problem in memory system design, and provide for high-speed operation, the ratioless driver circuit shown in Fig. 1.4 was used.

With this circuit, the current flowing in transistors Q_1 and Q_2 for changes in the output waveform is practically zero. Fig. 1.5 shows the peak current waveforms. The figure shows that the peak currents are kept less than 100mA irrespective of transition on $\overline{RAS}$ and $\overline{CAS}$.

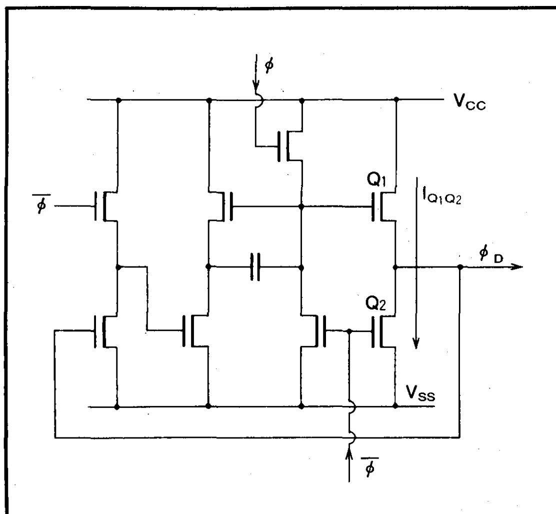


Fig. 1.4 Driver circuit

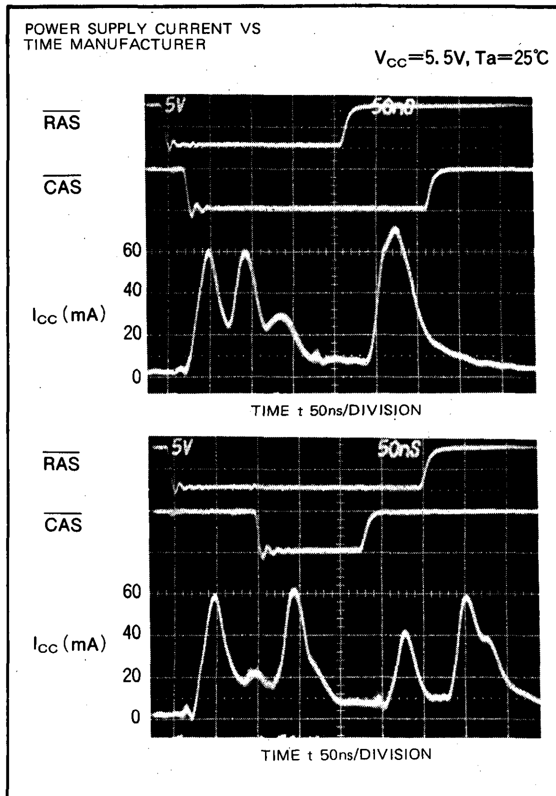


Fig. 1.5 Peak current waveforms

MITSUBISHI ELECTRIC

4. Soft Error Reduction

Reduction pattern sizes and lower supply voltages for 64K RAM devices which result in smaller storage charges also result in a higher susceptibility to alpha particles causing soft errors.

These soft errors are caused by alpha particles from minute amounts (ppm order) of uranium and thorium which are present in the IC package and decay. These particles cause the formation of electron-hole pairs in the substrate which collect on the surface and can destroy data.

All floating nodes of dynamic circuits are susceptible to such radiation-induced errors and for RAM operation, errors can occur when such phenomena occur in the memory cells and bit lines (including the sense amplifier).

To prevent such soft errors, three approaches are possible.

1) Increase the stored charge in the memory cells.
2) Increase the sense amplifier sensitivity and the bit line signal level.
3) Prevent alpha particles from reaching the chip circuits. As described below, the M5K4164AP makes use of these techniques to reduce the effects of alpha radiation.

(1) Bootstrapped Word Line Voltage

Designs of 64K dynamic RAM devices which must operate on 5V supplies must strive to write data into memory with the voltage V_{CC} as well as increase the charge stored in the memory cells in order to reduce the effects of soft errors. This in effect means raising the word line voltage to above the value of $V_{CC} + V_{TH}$ for write and read operations.

Previously, this increase in voltage was accomplished by means of the coupling capacitance between the word line and the delay circuit. However, the increased capacitance resulted in a slow risetime of the word line voltage to V_{CC}, as well as increased power consumption. To eliminate these problems a circuit design such as that shown in Fig. 1.6 is used. The transistor Q_2 is kept off until the word line voltage reaches V_{CC}. This has the word line charge capacity. C_2 is then charged by means of transistor Q_3 after which Q_2 is turned on to connect the word line and C_2. The use of this circuit enables increase of the word line voltage without sacrificing operating speed and power consumption, thereby cutting soft error rates by 90%.

(2) High-Capacity (Hi-C) Memory Cell

The increase of memory cell stored charge requires an increase in the memory cell capacitance Cs. Limited chip area, however, places restrictions on the size of the memory cell itself. For this reason the Hi-C structure shown in Fig. 1.1 was used. This cell structure makes use of the normal silicon oxide layer and the P+ and n+ junction capacitance. The process for Hi-C memory cell structure requires two additional ion implantation steps and involves the risk of deterioration of the refresh time, an important characteristic of a dynamic RAM device. By selecting the ion implantation level properly, the junction capacitance can be increased without deterioration in the refresh time characteristic. For Hi-C structured cells, a portion of the minority carriers formed in the P+ layer are recombined, resulting in an effective reduction in soft errors. Such ion implantation has achieved a 30% increase in the memory cell capacitance and a reduction in soft error rate to 1/12 of the error rate of a normally structured cell, as shown in Fig. 1.7.

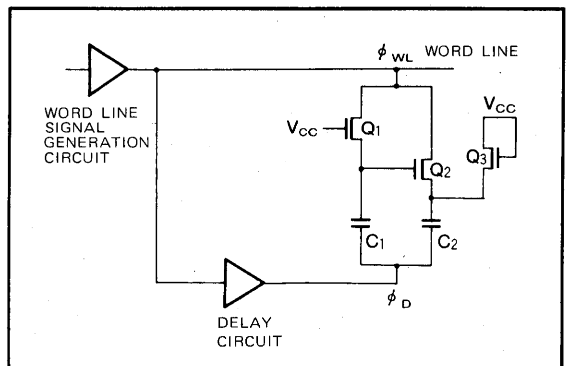


Fig. 1.6 Bootstrapped word line voltage generation circuit

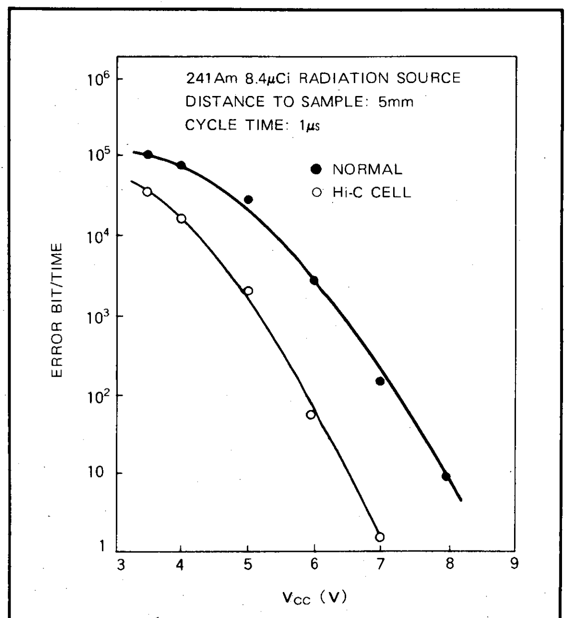


Fig. 1.7 Soft error rate dependency on supply voltage

(3) Sense Amplifier Circuit

Increasing the sensitivity of the sense amplifier circuit is another effective method of reducing soft errors. Fig. 1.8 shows part of the sense amplifier circuit used by Mitsubishi Electric. High sensitivity with respect to the control signals $\phi1$, $\phi2$, and $\phi3$ plays an important role in this amplifier's operation. After the data read from the memory cell is passed to the sense amplifier, the $\phi3$ signal is controlled to separate the bit line and cut off the noise that is present on the bit line when sensing begins. Smooth sensing begins with the signal $\phi1$ applied so that the minute potential difference is amplified. Next, $\phi2$ is applied and amplified at high speed. By careful adjustment of the timing of the three control signals $\phi1$, $\phi2$, and $\phi3$, detection of the potential differences as low as 30mV can be achieved without sacrificing speed in this sense amplifier circuit.

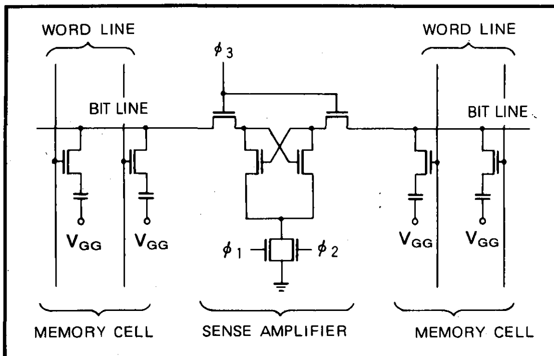


Fig. 1.8 Sense amplifier circuit

(4) 128 Refresh Method

When the sense and amplifier sensitivity (offset) and other factors are considered, it is clear that it is important to maximize the read voltage applied from the memory cell to the bit line. The electrical charge, Q, read from the memory cell determines the voltage change ΔV by the following relationship

$$\Delta V \approx Q/C_B \text{ (for } C_B \gg C_s)$$

where C_B is the bit line and Cs is the memory cell capacitance.

From this relationship it is seen that to make ΔV large C_B must be made small. To satisfy this condition the 128 refresh method is used to implement a single bit line with 64 memory cells, a technique which reduces the length of the bit line. Fig. 1.9 shows the chip layout. The memory cells are broken into 64x256 bit units which are narrow, long blocks. The column decoders are located in three blocks totalling 256 decoders at the end of the bit line.

Using this arrangement, the bit line capacitance can be minimized.

(5) Mold regin

In addition to circuit and device structure improvements aimed at reducing soft errors, the design goal of 10^{-6}/(device hours) requires further improvements.

When this is done, however, alpha particles emitted from the mold regin material itself cause errors, making material selection critical. The mold resin chosen exhibits an alpha radiation level of $0.05\alpha/cm^2$ (hour), below the measurement sensitivity of an ion chamber. This is low enough that the resulting alpha particle generation level is 1/10 or less that of old material itself.

System evaluations of the M5K4164AP treated in such a manner indicate that the design goal of 10^{-7}/(device hours) for soft error has been achieved.

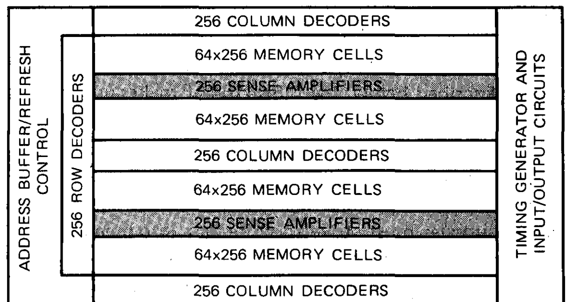


Fig. 1.9 M5K4164AP Chip arrangement

Functional Description

The M5K4164AP is a 64K-bit dynamic RAM which operates off a single 5V supply and has a refresh function built in at pin 1. It can be used in a wide range of applications from large mainframes to microcomputers.

This section presents a functional description of the M5K4164AP and examines how it can be used in design of a memory system.

1. Block Diagram

Fig. 1.10 shows the block diagram of the M5K4164AP. To preserve the refresh cycle used for 16k dynamic RAM devices, two 32k blocks (of 128 rows [refresh address] x 256 columns each) were arranged one on top of the other.

In the center of each block is located 256 sense amplifiers making a total of 512 amplifiers in all.

On one end of each of these two array blocks is located one row decoder.

To prevent crosstalk between the column address lines and bit lines, the column decoders are located at the ends of the bit lines opposite to the sense amplifiers. A total of three rows of column decoders are used.

The central column decoder is used commonly by the two blocks.

2. Memory Cell

As shown in Fig. 1.11, the memory cell consists of one transistor and one capacitor. Data is stored as a one or zero depending upon the amount of electrical charge stored in the capacitor through the transistor Q.

Because leakage current would result in the stored charge of the cell being reduced with time, the data must be refreshed within 2ms.

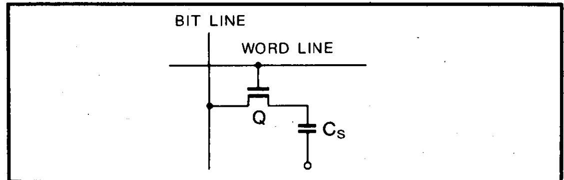


Fig. 1.11 Memory cell

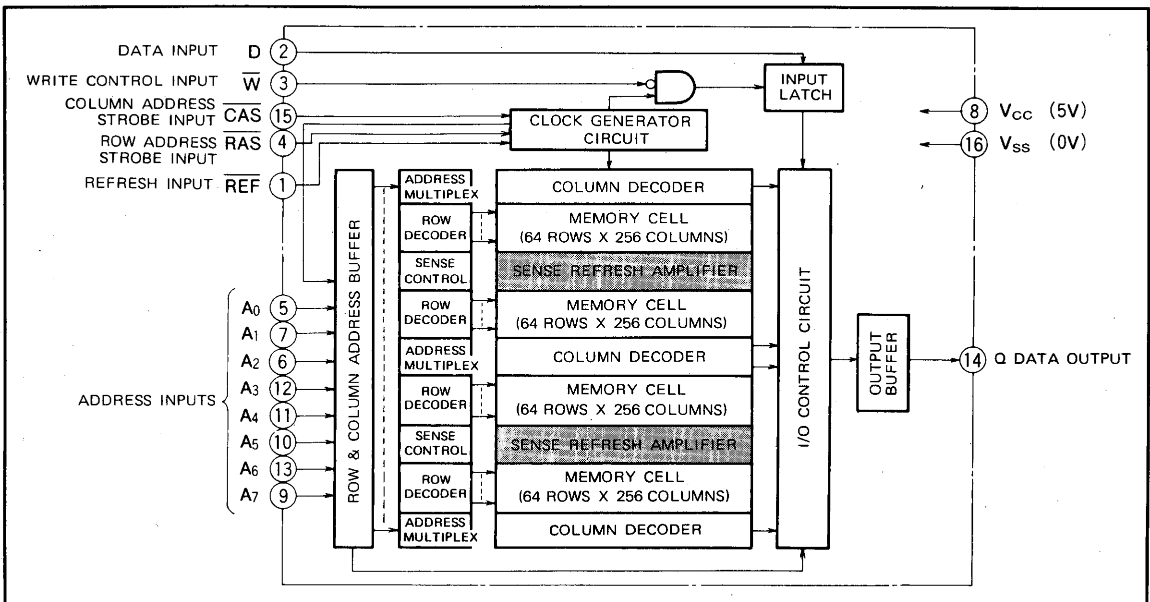


Fig. 1.10 Block diagram

3. Clock Timing

The M5K4164AP has four clock inputs: $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{REF}$. Among these, $\overline{RAS}$ and $\overline{CAS}$ are the basic clock inputs for the memory operation. The $\overline{RAS}$ input is generally used for memory cell data amplification and refresh operation while the $\overline{CAS}$ is used for data read and write operations only.

To enable the design of a memory system with a large timing margin, it is necessary to know the timing relationships between these two clock inputs and the internal clock signals generated by these clocks.

Fig. 1.13 shows the timing parameters of the $\overline{RAS}$ and $\overline{CAS}$ clocks while Fig. 1.14 and 1.15 show their relationships to the internal clock timing.

For read or write operations, $\overline{RAS}$ goes low after which the falling edge of $\overline{CAS}$ initiates the cycle.

After the read or write is completed, both signals return to a high level and the precharging operation is performed for the next cycle.

For this timing relationship to work, the external $\overline{RAS}$ clock must follow the changes of the internally generated $\overline{RAS}$ clock. To simplify the setting of the timing relationships of the external $\overline{RAS}$ and $\overline{CAS}$ clocks, the internal $\overline{CAS}$ clock ϕ_{CAS}, $\phi_{\overline{CAS}}$ is controlled by the external $\overline{RAS}$ clock. Fig. 12 shows the internal $\overline{RAS}$ and $\overline{CAS}$ clock generating circuit.

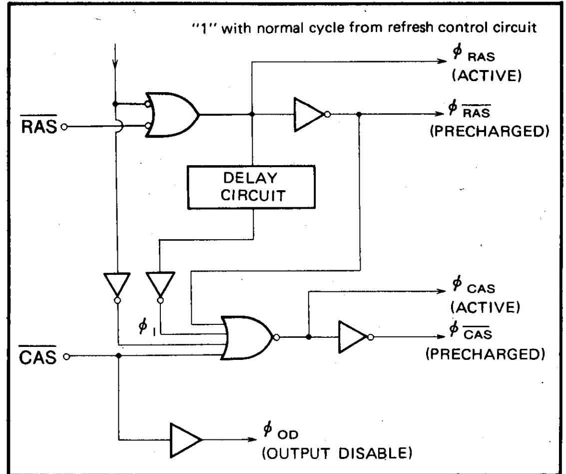


Fig. 1.12 Internal $\overline{RAS}$ and $\overline{CAS}$ clock generating circuit

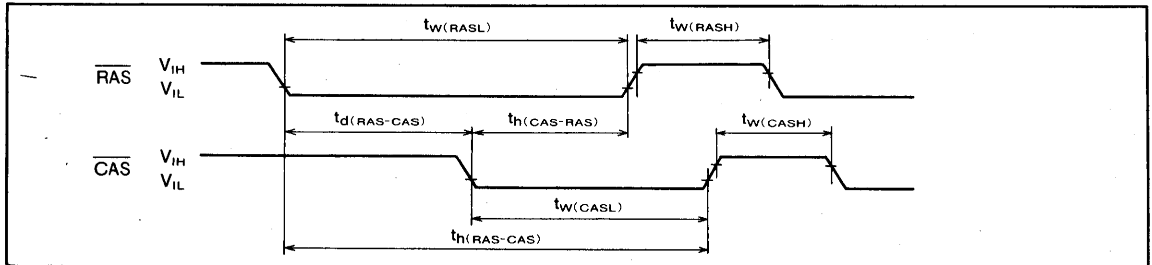


Fig. 1.13 $\overline{RAS}$, $\overline{CAS}$ timing

MITSUBISHI ELECTRIC

(1) $\overline{\text{CAS}}$ Falling Edge Timing (Fig. 1.14)

The memory system design must be such that the falling edge timing of $\overline{\text{CAS}}$ does not critically affect the access time. In other words as shown by the solid line in Fig. 1.14, the internal ϕ_{CAS} phase is prevented by the delay phase ϕ_1 from approaching $t_{d(RAS\text{-}CAS)}$ max. This type of operation is referred to as gated $\overline{\text{CAS}}$.

This gated $\overline{\text{CAS}}$ feature permits $\overline{\text{CAS}}$ to be activated at anytime between the minimum and maximum value of $t_{d(RAS\text{-}CAS)}$ without affecting access time.

For gated $\overline{\text{CAS}}$ operation, if the generation of internal clock phase ϕ_{CAS} is delayed, the effective pulse width of ϕ_{CAS} is reduced. For this reason, the rising edge of $\overline{\text{CAS}}$ is specified by $t_{h(RAS\text{-}CAS)}$ which is reference to $\overline{\text{RAS}}$ rather than $t_{w(CASL)}$. This applies to the column address, $\overline{\text{W}}$ and D inputs hold time as well.

As shown by the dotted line in Fig. 1.14, if $\overline{\text{CAS}}$ falls to a low level after $t_{d(RAS\text{-}CAS)}$ max, the ϕ_{CAS} phase is generated upon the falling edge of $\overline{\text{CAS}}$.

The minimum and maximum values of $t_{d(RAS\text{-}CAS)}$, the delay time $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$, are specified for the M5K4164AP. Operation within the $t_{d(RAS\text{-}CAS)}$ max limit ensures that the access time for the device is guaranteed. This value may be exceeded without causing data storage or reading errors but the access time will be increased.

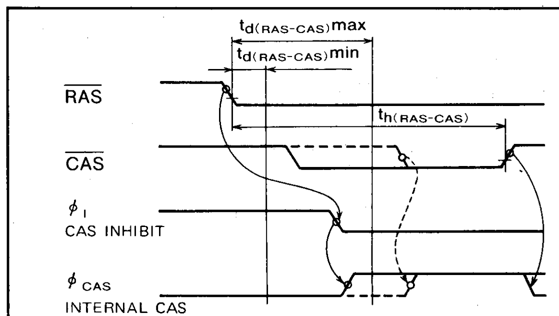


Fig. 1.14 The timing relationship of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ falling edges to internal clock signals (gated $\overline{\text{CAS}}$ operation)

(2) $\overline{\text{CAS}}$ Rising Edge Timing (Fig. 1.15)

As shown in Fig. 1.15, the internally generated $\overline{\text{CAS}}$ circuit precharge signal $\phi_{\overline{CAS}}$ is generated with a timing that is related to the relationship between $\overline{\text{RAS}}$ and the $\overline{\text{CAS}}$ rising edge.

For a $\overline{\text{CAS}}$ rising edge occurring before the $\overline{\text{RAS}}$ rising edge, $\phi_{\overline{CAS}}$ is generated with the $\overline{\text{CAS}}$ rising edge as a reference point (as shown in Fig. 1.15 as a solid line). If however the $\overline{\text{CAS}}$ rising edge occurs after that of $\overline{\text{RAS}}$, $\phi_{\overline{CAS}}$ is generated with the $\overline{\text{RAS}}$ rising edge as a reference (shown as dotted line in Fig. 1.15).

However, the data in the output buffer is cleared upon the occurrence of the rising edge of $\overline{\text{CAS}}$ regardless of the state of $\overline{\text{RAS}}$. The required pulse width for clear is $t_{w(CASH)}$.

In this manner, the output data can be maintained for a long period while the internal precharge width is made large.

As described above, if the $\overline{\text{CAS}}$ rising edge occurs after that of $\overline{\text{RAS}}$, the internal $\overline{\text{CAS}}$ pulse width becomes not $t_{w(CASL)}$ but $t_{h(CAS\text{-}RAS)}$. Consideration should be given to this point in circuit design.

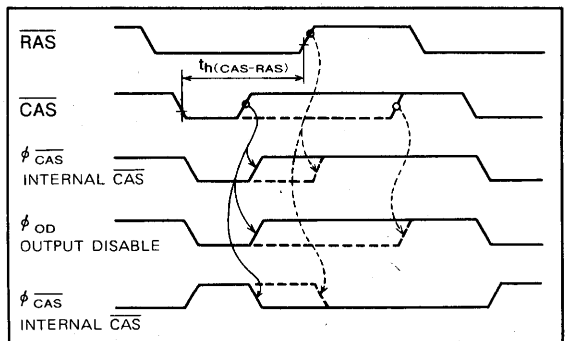


Fig. 1.15 Relationship of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ rising edges to internal clock timing

4. Address Timing

Addressing of any one of the 65,536 memory cells of the M5K4164AP requires the internal latching of two 8-bit multiplexed address (A_0 to A_7) by means of clocks $\overline{RAS}$ and $\overline{CAS}$. First, the row address is latched by the falling edge of $\overline{RAS}$. This selects 512 memory cells from the total of 65,536 memory cells. Fig. 1.16 shows the timing relationships for this operation.

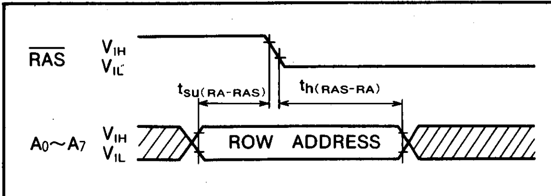


Fig. 1.16 Row address latching timing relationships

The setup time $t_{su(RA-RAS)}$ and holdtime $t_{h(RAS-RA)}$ are specified with the $\overline{RAS}$ falling edge as a reference point.

The falling edge of $\overline{CAS}$ latches the column address. This selects one cell from among the 512 cells selected by $\overline{RAS}$. Fig. 1.17 shows the timing relationships for this operation. The setup time $t_{su(CA-CAS)}$ and the hold time $t_{h(CAS-CA)}$ are specified with the falling edge of $\overline{CAS}$ as a reference, while the hold time $t_{h(RAS-CA)}$ is specified with the falling edge of $\overline{RAS}$ as a reference point.

For these operations two timing parameters must be considered. One is the column address setup time $t_{su(CA-CAS)}$ which is specified as minus 5ns, minimum. This means that the column address may be input anytime up to 5ns after the $\overline{CAS}$ falling edge.

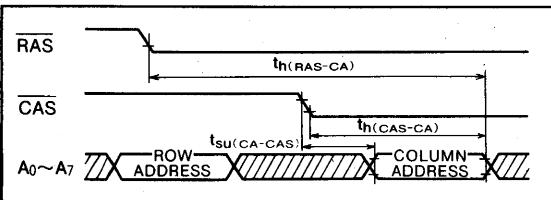


Fig. 1.17 Column address latch timing

The other parameter is the column address hold time $t_{h(RAS-CA)}$. For the previously described gated $\overline{CAS}$ operation, if $\overline{RAS}$ to $\overline{CAS}$ delay time $t_{d(RAS-CAS)}$ is set between the specified minimum and maximum values, the time from $\overline{RAS}$, $t_{h(RAS-CA)}$ and time from $\overline{CAS}$, $t_{h(CAS-CA)}$ must both be satisfied as the column address hold time. This applies to both the $\overline{W}$ and D signals to be described later.

The time required to switch from row address to column address is referred to as the multiplex time (t_{MUX}). This timing is shown in Fig. 1.18.

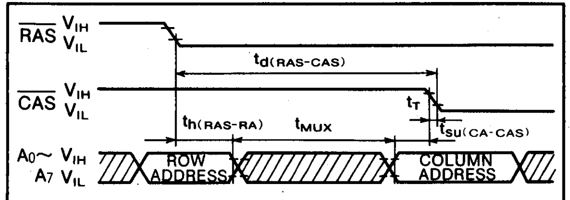


Fig. 1.18 Address multiplex timing

The multiplex time t_{MUX} is given by the following expression:

$$t_{MUX} = t_{d(RAS-CAS)} - t_T - t_{h(RAS-RA)} - t_{su(CA-CAS)} \quad \cdots\cdots (1)$$

As long as the access time, $t_{a(RAS)}$ from $\overline{RAS}$ does not exceed the maximum value, the following expression determines the maximum value of t_{MUX} is achieved by the following conditions.

$t_{d(RAS-CAS)}$ = maximum

$t_{a(RAS-RA)}$ = minimum

$t_{su(CA-CAS)}$ = minimum

Table 1.2 shows actual values of t_{MUX} maximum for t_T = 5ns.

Table 1.2 Maximum multiplex time

Device \ Parameter	t_{MUXmax}	$t_{d(RAS-CAS)}$	$t_{h(RAS-RA)}$	$t_{su(CA-CAS)}$
M5K4164AP-12	40ns	60ns	15ns	0ns
M5K4164AP-15	50ns	75ns	20ns	0ns

If the timing is set to satisfy the above described, operation is guaranteed for both read and write functions. To simplify the following description, the timing parameters for address inputs has been eliminated unless absolutely required.

5. Read Cycle

Fig. 1.19 shows the timing parameters for the read cycle.

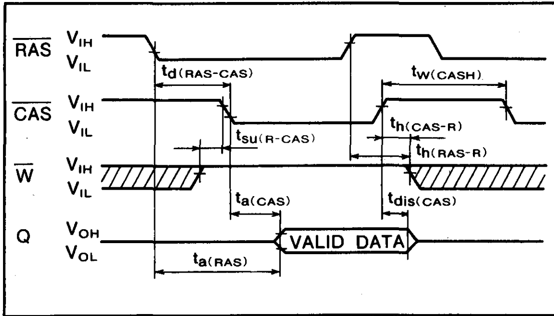


Fig. 1.19 Read cycle timing

In this read cycle, $\overline{RAS}$ and $\overline{CAS}$ are made active, and the W input is set to a high level. The setup time, $t_{su(R\text{-}CAS)}$ before $\overline{CAS}$, resulting in output of the data stored in the memory cell at pin Q. The time for the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to the output is defined as the $\overline{RAS}$ access time $t_{a(RAS)}$ and the $\overline{CAS}$ access time $t_{a(CAS)}$ respectively.

The $\overline{RAS}$ access time depends on the $\overline{RAS}$ to $\overline{CAS}$ delay time, $t_{a(RAS)}$ and $t_{d(RAS\text{-}CAS)}$.

As can be seen from this figure, by setting $t_{d(RAS\text{-}CAS)}$ before t_d for gated $\overline{CAS}$ operation, $t_{a(RAS)}$ does not depend on the value of $t_{d(RAS\text{-}CAS)}$ and is constant.

For $t_{d(RAS\text{-}CAS)}$ set after t_d, $t_{a(RAS)}$ depends upon the value of $t_{d(RAS\text{-}CAS)}$. For this condition, $t_{a(RAS)}$ is given by the following expression.

$$t_{a(RAS)} = t_{d(RAS\text{-}CAS)} + t_{a(CAS)} \quad \cdots\cdots (2)$$

Equation (2) expresses only the electrical characteristics of the RAM device, the guaranteed access time being given by the following expression.

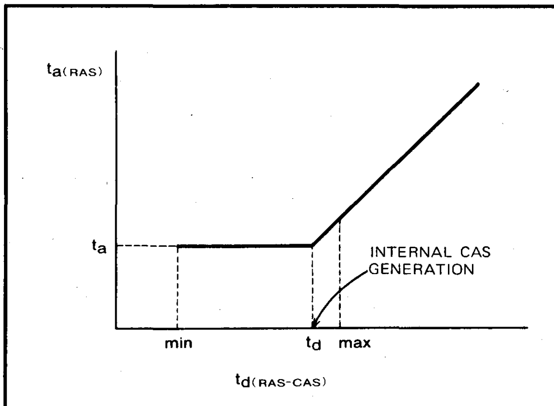


Fig. 1.20 Dependency of $t_{a(RAS)}$ on $t_{d(RAS\text{-}CAS)}$

$$t_{a(RAS)} \leq t_{d(RAS\text{-}CAS)}\ max + t_{a(CAS)}\ max \quad \cdots\cdots (3)$$

In equation (3), for a value of $t_{d(RAS\text{-}CAS)}$ greater than the maximum value ($t_{a(RAS)}$) increases by the increased amount only.

During a read operation when the output is active, inputs $\overline{RAS}$ and $\overline{W}$ have no effect on the output. Only raising $\overline{CAS}$ to a high level will put the output in the high-impedance state.

The time from the rising edge of $\overline{CAS}$ until the output goes into the high-impedance state is defined as the output disable time ($t_{dis(CAS)}$). This time, $t_{dis(CAS)}$ is the period for the RAM output to go to the open state and should be distinguished from that time the output states to go to V_{OH} and V_{OL}.

If the pulse width $t_{w(CASH)}$ is satisfied for $\overline{CAS}$, operation is guaranteed for any arbitrary timed rising edge after the next cycle, simplifying the design with respect to $\overline{CAS}$ timing.

The read cycle parameters $t_{h(CAS\text{-}R)}$ and $t_{h(RAS\text{-}R)}$ determine the read cycle ending time. Operation is guaranteed if either of these parameters are satisfied.

6. Write Cycle

Three types of write cycles are specified; early write, read write and read modify write.

(1) Early Write Cycle

Fig. 1.21 illustrates the timing relationship for this cycle.

This cycle is selected for applications such as I/O common applications in which the output is held at high impedance during the writing of data into the memory cell.

This cycle is executed by causing the $\overline{W}$ input to fall before $\overline{CAS}$.

The $\overline{W}$ and D inputs are latched by $\overline{CAS}$, then the data write is executed, the $\overline{W}$ and D input timing parameters $t_{su(W\text{-}CAS)}$, $t_{su(D\text{-}CAS)}$, $t_{h(CAS\text{-}W)}$, and $t_{h(CAS\text{-}D)}$ are determined by the falling edge of $\overline{CAS}$ as a reference point.

Two points here are worthy of consideration. First is the write pulse setup time $t_{su(W\text{-}CAS)}$. This parameter is specified as minus 10ns, minimum.

The significance of this is that $\overline{W}$ inputs may occur anytime within before 10ns of the falling edge $\overline{CAS}$.

However, should the $\overline{W}$ input falling edge occur after $\overline{CAS}$, the rising edge of $\overline{W}$ is determined not by $t_{h(CAS\text{-}W)}$, but by $t_{w(W)}$.

The other point for consideration is setting $t_{d(RAS\text{-}CAS)}$ between the minimum and maximum values. For this condition, gated $\overline{CAS}$ operation requires that as hold time the time from $\overline{RAS}$ for the $\overline{W}$ and D input, $t_{h(RAS\text{-}W)}$ and $t_{s(RAS\text{-}D)}$ and time from $\overline{CAS}$, $t_{h(CAS\text{-}W)}$ and $t_{h(CAS\text{-}D)}$ both must be satisfied.

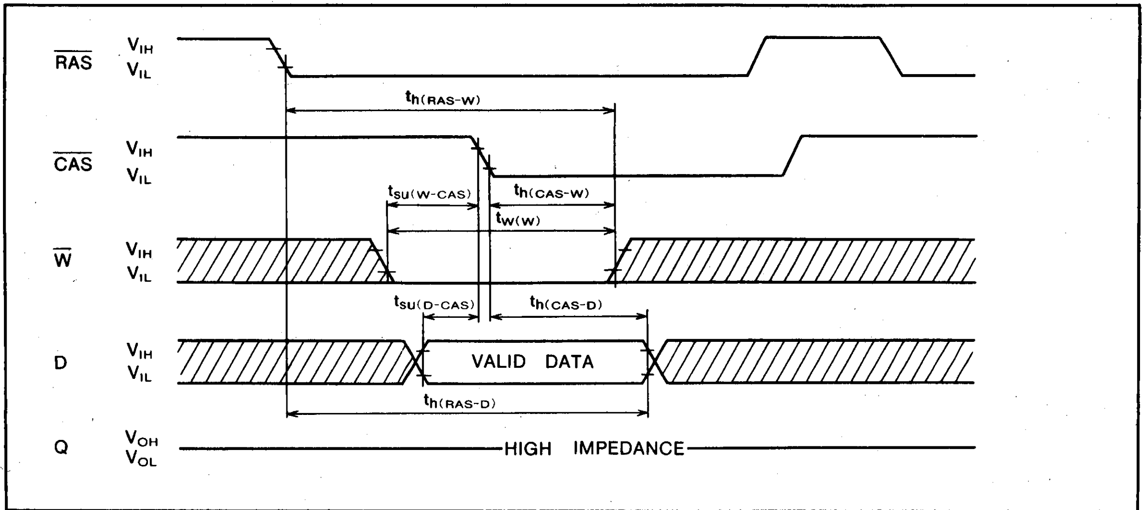


Fig. 1.21 Early write cycle timing

(2) Read Write Cycle Timing

This cycle is used in applications where data is to be read out of memory while new data is being written into a memory cell.

The timing parameters for this read write cycle are shown in Fig. 1.22.

For this type of cycle, the $\overline{W}$ input signal falls after $t_{d(RAS-W)}$ min and $t_{d(CAS-W)}$ min.

The data read timing is the same as the read cycle. Since the read data is latched into an output buffer, $\overline{W}$ input can be made active without disabling the output.

Since the D input is latched by the falling edge of the $\overline{W}$ input, the $\overline{W}$ input falling edge is determined as a reference point for the D input setup time $t_{su(D-W)}$ and hold time $t_{h(W-D)}$.

Data is written into the memory cell between the time the $\overline{W}$ input signal falls and $\overline{RAS}$ and $\overline{CAS}$ rise. This time is specified as $t_{h(W-RAS)}$ and $t_{h(W-CAS)}$ and both of these must be satisfied.

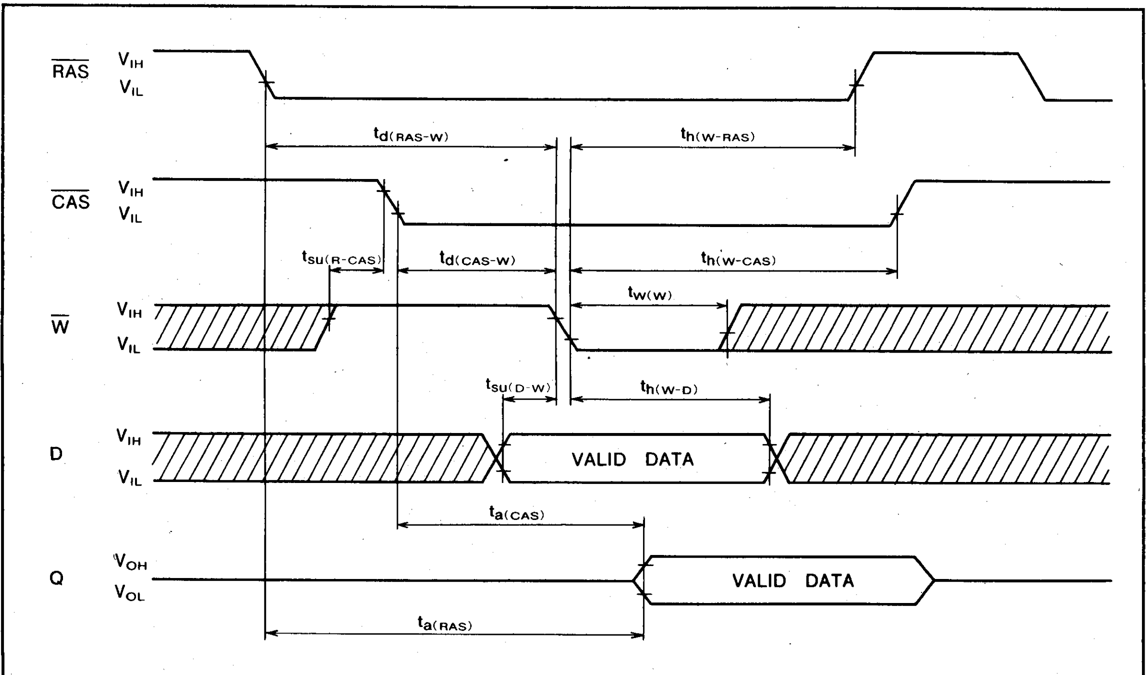


Fig. 1.22 Read write cycle timing

(3) Read Modify Write Cycle

This cycle is used in applications such as ECC (see section on ECC) on which memory cell data is read and verified for correctness, the correct data being written into the cell if an error is detected. Fig. 1.23 shows the timing parameters of the read modify write cycle.

The RAM operation is the same as the previously described read write cycle except that after the data is read, data is written so the cycle is slightly extended.

The minimum time for the read modify write cycle is given by the following expression.

$$t_{CRMW}\ \text{min} = t_{a(RAS)}\ \text{max} + t_{MOD} + t_{h(W-RAS)}\ \text{min} + t_{w(RASH)}\ \text{min} + 3t_T \quad \cdots\cdots\cdots\cdots \quad (4)$$

In equation (4), t_{MOD} is the time required for incorrect data to be rewritten correctly, and is a function of system design. In the device specifications t_{CRMW} min is specified for $t_{MOD} = 0$.

As previously described, the M5K4164AP write cycle mode is determined by the $\overline{W}$ input falling edge timing. This falling edge timing does not limit the operation of the RAM but merely controls the output state. If the $\overline{W}$ input falling edge does not satisfy the conditions described for the three write modes, data will be writen but the output state will be indeterminate.

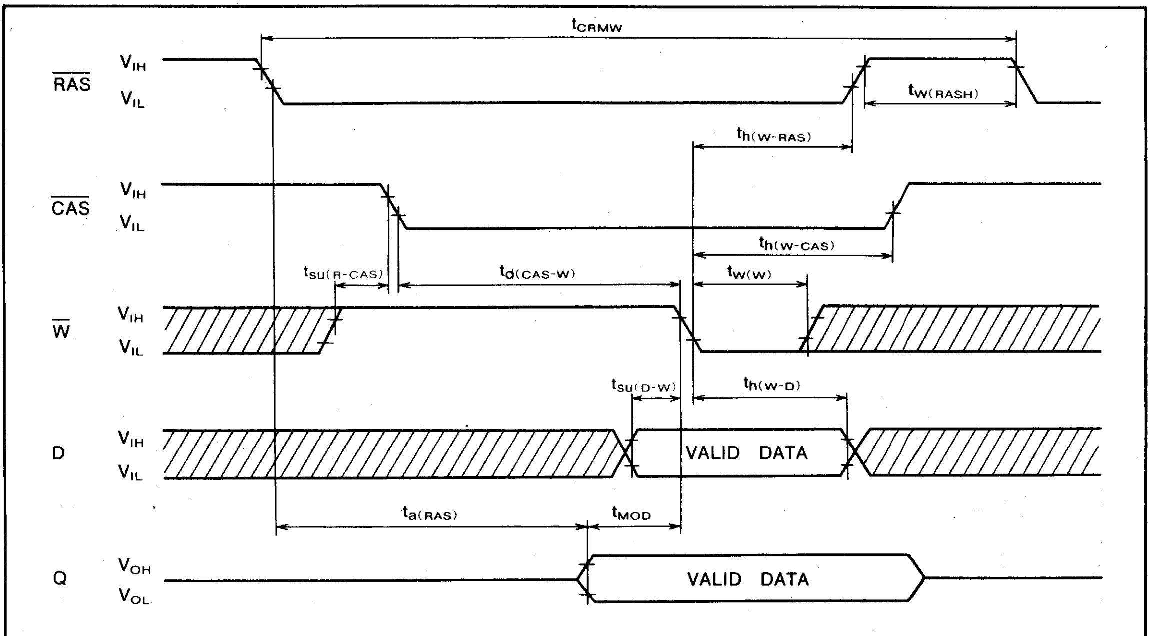


Fig. 1.23 Read modify write cycle timing

7. Page Mode Timing
Page mode operation is successive memory operations at multiple column locations within the same row address.

As with normal operation, page mode operation can be carried out in the read, early write, read write or read modify write modes. The timing parameters particular to the page mode of operation are shown in Fig. 1.24. The other parameters are the same as for normal cycles.

To perform page mode read and write operations, the $\overline{RAS}$ low-level pulse width, $t_{W(RASL)}$ must be increased, the maximum value being 10μs. The high-level $\overline{CAS}$ pulse width, $t_{W(CASH)}$ is specified separately for the normal mode cycle and page mode. For the page mode, the pulse width must be increased. For details refer to the specifications.

For page mode operation the hold time $t_{h(CAS-RAS)}$ must be satisfied for even the last cycle, as shown in Fig. 1.24. This applies to $\overline{W}$ as well.

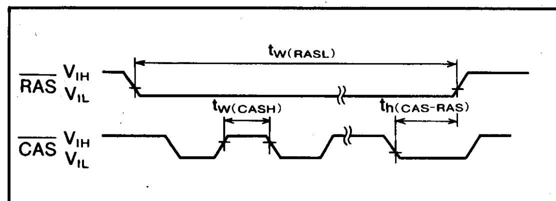


Fig. 1.24 Page mode cycle timing

8. Refresh
Referring to the block diagram of Fig. 1.10, for each $\overline{RAS}$ cycle, one word line is selected for each of the upper and lower blocks, enabling access to 512 memory cells. Next, the 512 sense amplifiers operate to amplify and refresh the cell data. Address signal A_7 (ROW) has no connection with this refresh operation since it is used as a block select address for data read and write operations.

9. $\overline{RAS}$ Only Refresh Timing
$\overline{RAS}$ only refresh is performed by setting $\overline{CAS}$ to high which sets the output to high-impedance while refresh is performed.

Both distributed and burst mode refresh can be performed.

Fig. 1.25 shows the timing parameters for $\overline{RAS}$ only refresh operation.

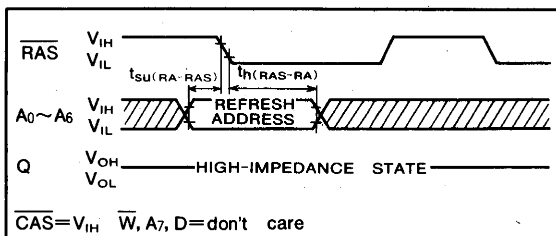


Fig. 1.25 $\overline{RAS}$-only refresh timing

10. Hidden Refresh Timing
Hidden refresh is accomplished by setting $\overline{CAS}$ to low after a read cycle to hold the data in the valid state while refresh is performed.

Both distributed and burst mode refresh are possible. Fig. 1.26 shows the timing parameters for hidden refresh operations.

Data latched in the output buffer by the read cycle is refreshed during the hidden refresh cycles by $\overline{RAS}$. Therefore output data is held indefinitely as long as hidden refreshing is continued.

Timing design is simplified because the $\overline{W}$ signal may be changed in any state during hidden refreshing.

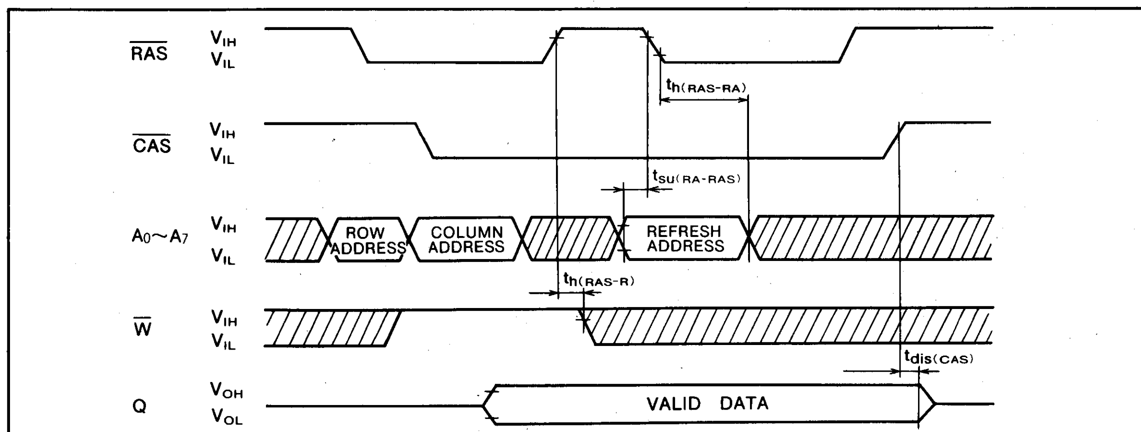


Fig. 1.26 Hidden refresh timing

11. Refresh Operations Using Pin 1

To simplify the refresh operation, a function absolutely essential to dynamic RAM operation, two special refresh functions easier to use than the conventional $\overline{\text{RAS}}$ clock refresh have been provided.

These functions are automatic refresh and self refresh.

These special functions are implemented by an on-chip refresh counter, address multiplexer, and timer, along with the associated control circuity. The following is an operational description of these circuits.

(1) Refresh Control Circuit

Fig. 1.27 shows a block diagram of the refresh circuit which makes use of Pin 1. The control circuit controls not only the refresh counter, address multiplexer and timer as shown in Fig. 1.27, but $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ circuits as well.

Pin 1 refreshing is controlled externally by the $\overline{\text{REF}}$ input and internally by the $\overline{\text{RAS}}$ signal which is generated by the refresh control circuit.

During pin 1 refresh operations, the $\overline{\text{CAS}}$ circuit with the exclusion of the output buffer is inhibited to prevent data writing and reading.

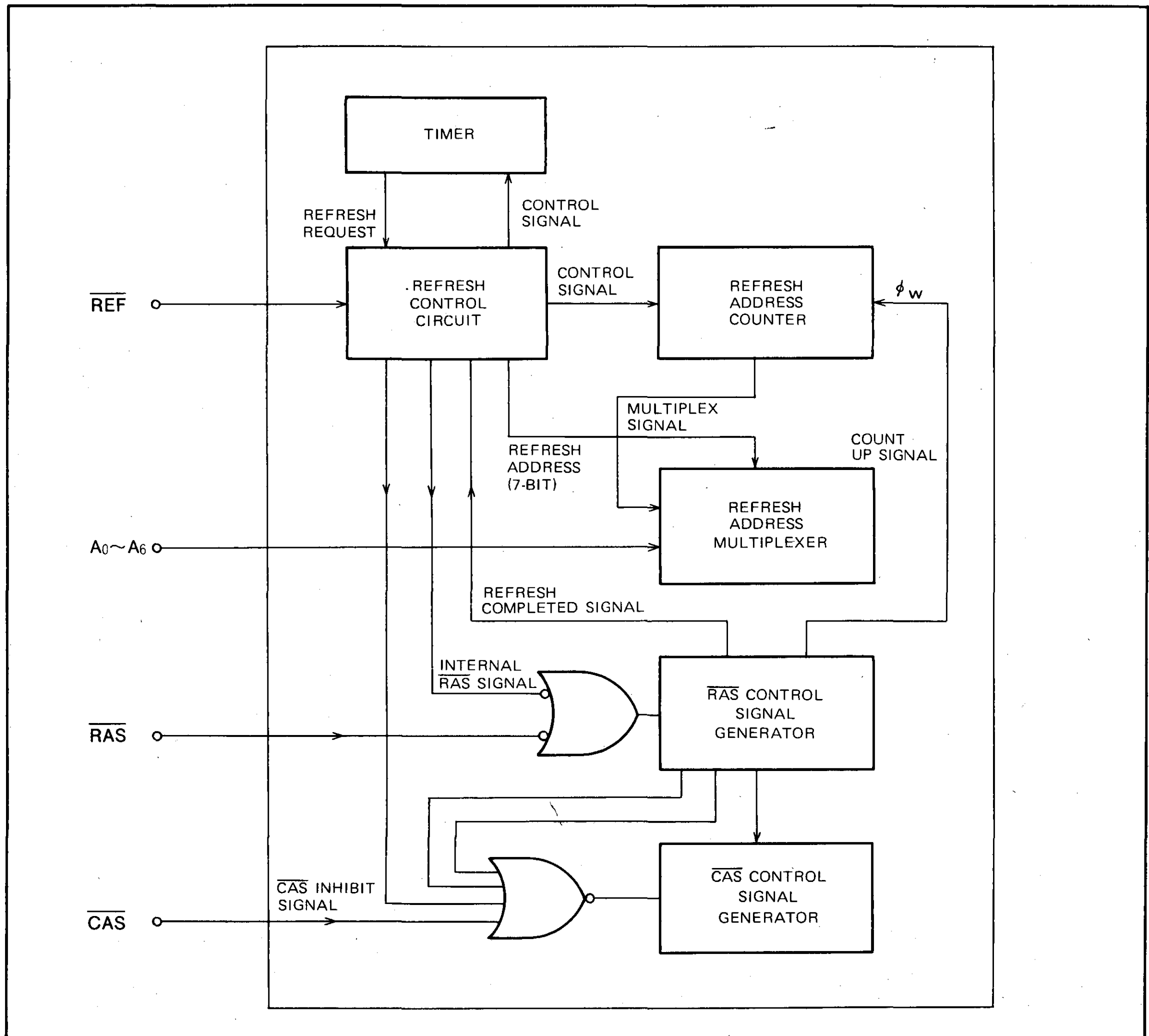


Fig..1.27 Refresh circuit block diagram

(2) Refresh Counter circuit

The M5K4164AP on-chip refresh counter consists of a 7-bit toggle-type counter, the individual counter output being used as the refresh address bit.

For automatic refresh operations, the refresh counter counts up synchronized to the internal clock signal ϕ_W which is synchronized in turn to the $\overline{REF}$ input, 128 $\overline{REF}$ pulses required to cycle to the original state. For self refresh operation, the refresh counter is free-running with a period of from 12 to 16μs, counting up in synchronous to the refresh request signal REF REQ (described afterwards). A complete cycle and return to the original state requiring that the $\overline{REF}$ input be held low for 16μs x 128 (approx.) ≒ 2ms.

The above described counting operation is performed approximately in synchronous with the refresh operation completion. The output of the refresh counter, Q_0 to Q_6 (refresh address) is held until the next refresh cycle, forming the address for the next cycle.

The refresh counter outputs are initialized by approximately 8 dummy cycles of $\overline{RAS}$, $\overline{RAS}/\overline{CAS}$, or $\overline{REF}$. Therefore, no special initialization is required for this refresh counter.

However, the contents of the counter, that is the toggle counter flip-flop states, cannot be reset or preset externally during power up or dummy cycles.

For this reason, using both normal $\overline{RAS}$ and pin 1 refresh will cause the specified refresh time to be exceeded, and therefore should be avoided.

(3) Address Multiplexer

Fig. 1.28 shows the M5K4164AP on chip address multiplexer.

The address multiplexer consists of two MOS transistors at the address buffer inputs and the associated control signals (MUX, $\overline{MUX}$).

During a normal cycle, $\overline{MUX}$ is high and MUX is low, so that only the external address A_0 to A_6 is input.

For pin 1 refresh operations, $\overline{MUX}$ is low and MUX is high so that the refresh counter output signals Q_0 to Q_6 only are input to the address buffer.

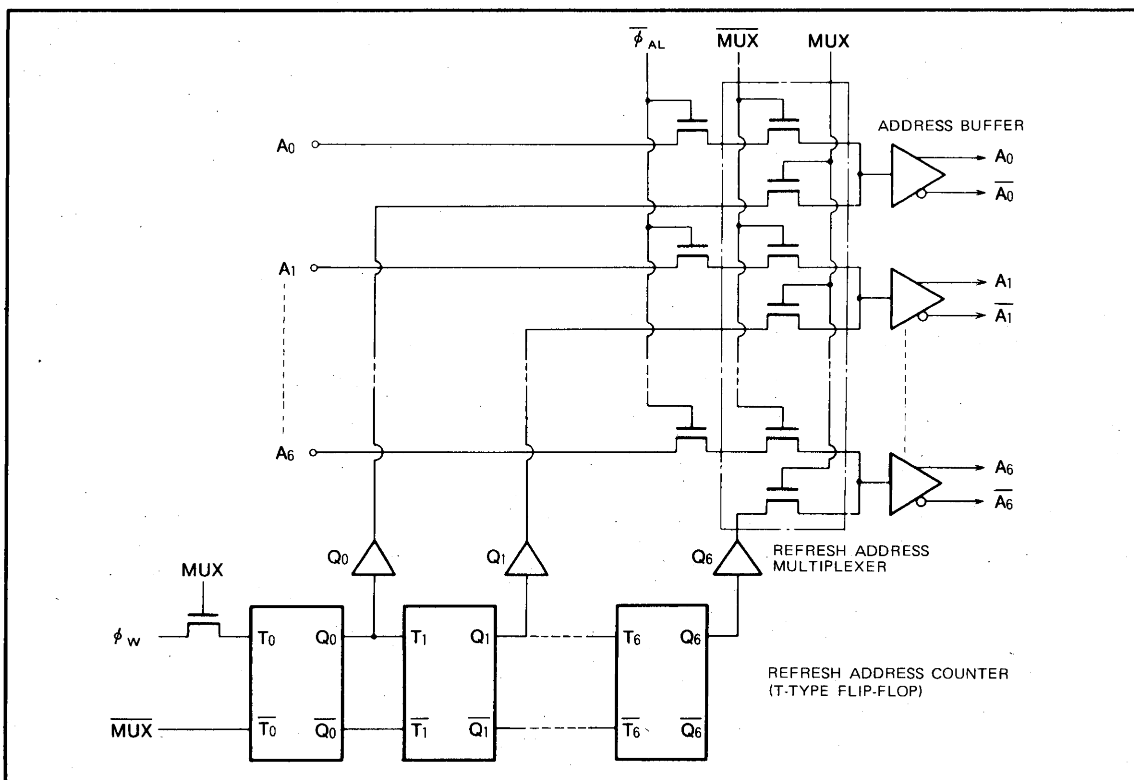


Fig. 1.28 Refresh address counter and multiplexer circuits

MITSUBISHI ELECTRIC

(4) Timer Circuit

Fig. 1.29 shows the timer circuit block diagram while Fig. 1.30 illustrates its timing.

In the circuit of Fig. 1.29, the oscillator provides the substrate bias as well. The other circuits are active when $\overline{\text{REF}}$ is low.

When $\overline{\text{REF}}$ goes low, transistor Q_1 turns on, Q_2 turns off and the charge stored in C_2 passes through the rectifying circuit C_1 and Q_1 to discharge upon the falling edge of the oscillator output signal. The charge for one cycle of the oscillator output is proportional to the ratio of the capacitance of C_1 and C_2.

The ratio of C_1 to C_2 is chosen such that the voltage across C_2 for an oscillator repetition period of 12 to 16μs is approximately equal to the threshold voltage of the next gate. When the C_2 voltage reaches V_{TH}, the refresh request signal REFREQ goes active, causing the RAM refresh operation similar to the automatic Refresh external signal $\overline{\text{REF}}$. When C_2 is charged by REFREQ, REFREQ goes low, causing a repetition of the above described timer operation.

As long as the $\overline{\text{REF}}$ signal is kept low, this operation will automatically continue refreshing all memory cells every 2ms.

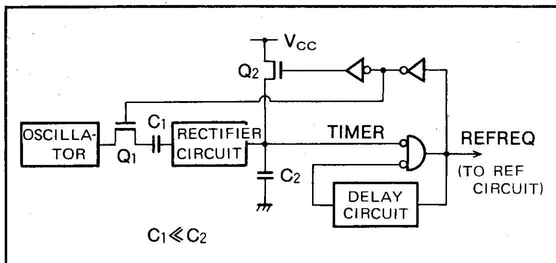


Fig. 1.29 Timer circuit block diagram

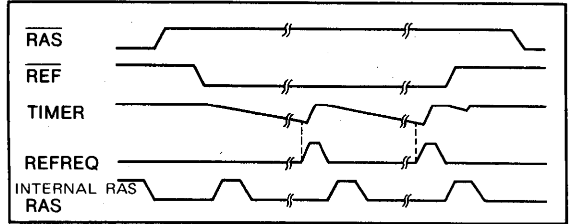


Fig. 1.30 Timer circuit timing

12. Automatic Refresh Timing

Automatic refresh is accomplished in the same manner as $\overline{\text{RAS}}$ only refresh but without providing the refresh address data.

Fig. 1.31 shows the timing of the automatic refresh operation.

Automatic refresh begins when $\overline{\text{REF}}$ is set to low $t_{d(RAS\text{-}REF)}$ after $\overline{\text{RAS}}$ goes high.

Shortly after the refresh cycle begins the internal RAS signal begins to operate to strobe the refresh counter output and perform the refresh.

The $\overline{\text{REF}}$ input is internally latched. When the refresh operation is complete an internal refresh complete signal causes the chip to be precharged. Therefore, it is not necessary to use the $\overline{\text{REF}}$ input to determine the precharge time greatly simplifying the timing design of $\overline{\text{REF}}$.

It is also possible to perform hidden refreshing by holding the $\overline{\text{CAS}}$ input low after a read cycle. The timing is very similar to the $\overline{\text{RAS}}$ hidden refresh operation timing. For details refer to the specifications.

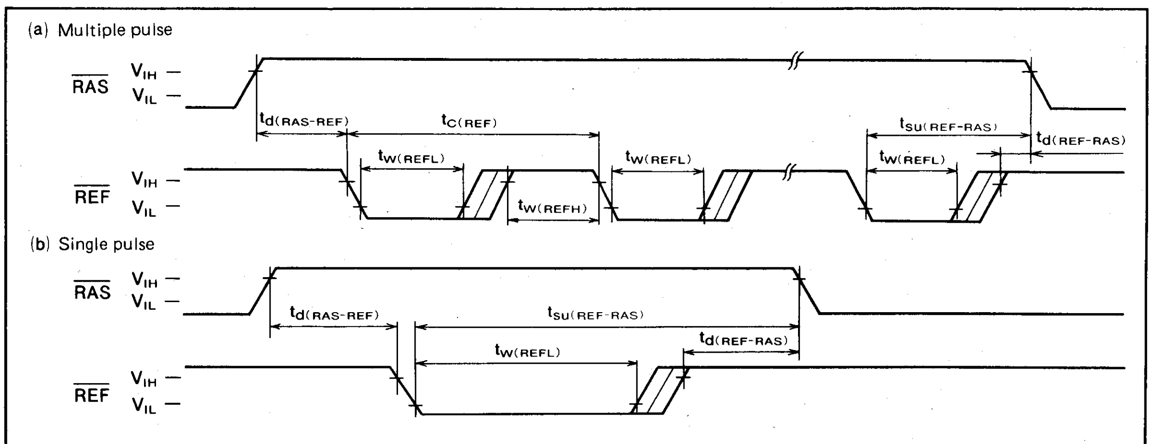


Fig. 1.31 Automatic refresh timing

13. Self Refresh Timing

Self refresh is generally used for battery backup of memory contents.

Fig. 1.32 shows the self refresh timing relationships from which it can be seen that they are quite similar to those of automatic refresh. Self refresh begins when $\overline{REF}$ is set to low $t_{d(RAS-REF)}$ after $\overline{RAS}$ is set to high.

Shortly after the beginning of the refresh cycle, the internal $\overline{RAS}$ signal begins to operate to strobe the refresh counter and perform the refresh operation.

As long as $\overline{RAS}$ is high and $\overline{REF}$ is low, the RAM will be automatically refreshed. This operation is repeated with a period of from 12 to 16μs. After 2ms, the refresh counter has gone through all of the row address, refreshing all of the memory cells. Self refresh ends when $\overline{REF}$ is set to high but setting $\overline{REF}$ to high may not terminate the internal operation of the circuit (refer to Fig. 1.30) so that one cycle time of $t_{d(REF-RAS)}$ is required between setting $\overline{REF}$ to high and $\overline{RAS}$ to low.

As with automatic refresh, hidden refreshing is possible. For details refer to the specifications.

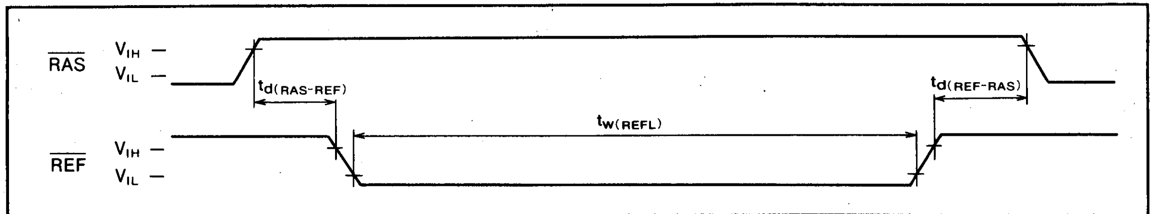


Fig. 1.32 Self refresh timing

14. Notes on the Use of Pin 1

(1) When pin 1 is not to be used to refresh the chip, it should be handled in the following manner.

Since pin 1 refresh is inhibited by setting the $\overline{REF}$ input to high, the input should be set between V_{IH} min and V_{IH} max. (The pin 1 input leakage current for V_{IN} = 6.5V is guaranteed to be below 10μA.)

(2) When the above method is not possible, pin 1 should be left open. Since as shown in Fig. 1.33 as MOS transistor is used to connect a pull-up resistor between the input terminals and V_{CC}, the terminal will be held to a high level (V_{CC}) when left open.

However, when the input is set low in order to perform a refresh operation, a current flows from V_{CC} to the input terminal. This resistance is made a very high value (approximately 3MΩ) in order to guarantee the specified leakage current of 10μA maximum for V_{IN} = 0V.

This high resistance results in pin 1 being susceptible to the effects of external noise so that if pin 1 is to be left open, such noise should be considered carefully.

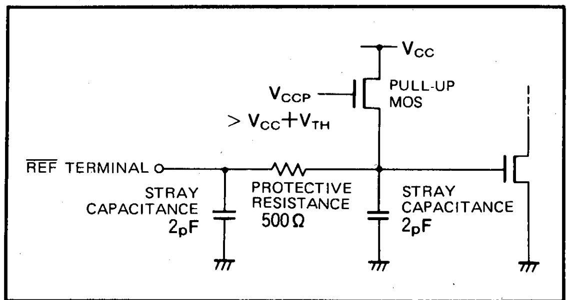


Fig. 1.33 $\overline{REF}$ input equivalent circuit

M5K4164AP Bit Map

To facilitate the generation of worst-case pattern checking and the optimization of test sequences, it is necessary to know the internal topology of a memory device. This section will examine the internal topology of the M5K4164AP.

1. Memory Array

Fig. 1.34 shows the dual in-line package as viewed from above with pin 1 to the upper right. It illustrates the memory cell layout.

The row decoder is located to the left of the memory cells while the column decoder is located parallel to the cells.

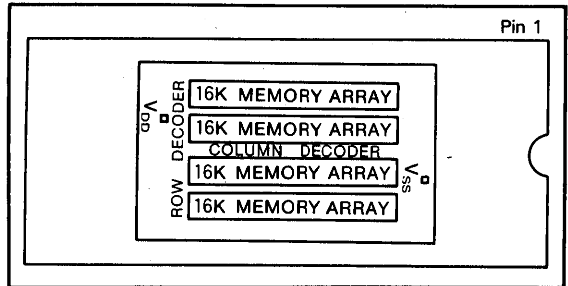


Fig. 1.34 Memory array location

ROW ADDRESS

A7	A0	A5	A4	A3	A2	A1	A6	Row	
0	0	0	0	0	0	0	0	0	16384-BIT MEMORY ARRAY DATA
0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	1	1	3	
0	0	0	0	0	0	1	0	2	
									256 SENSE AMPLIFIER CIRCUITS
0	1	1	1	1	1	0	0		16384-BIT MEMORY ARRAY $\overline{\text{DATA}}$
0	1	1	1	1	1	0	1		
0	1	1	1	1	1	1	1	127	
0	1	1	1	1	1	1	0	126	

COLUMN ADDRESS

A7	0	1	1	0	0	1		0	1	1	0	0	1	1	0
A6	0	0	1	1	0	0		0	0	1	1	0	0	1	1
A1	0	0	0	0	1	1		0	0	0	0	1	1	1	1
A2	0	0	0	0	0	0		1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0		1	1	1	1	1	1	1	1
A4	0	0	0	0	0	0		1	1	1	1	1	1	1	1
A5	0	0	0	0	0	0		1	1	1	1	1	1	1	1
A0	0	0	0	0	0	0		1	1	1	1	1	1	1	1

A7	A0	A5	A4	A3	A2	A1	A6	Row	
1	0	0	0	0	0	0	0	128	16384-BIT MEMORY ARRAY $\overline{\text{DATA}}$
1	0	0	0	0	0	0	1		
1	0	0	0	0	0	1	1		
1	0	0	0	0	0	1	0		
									256 SENSE AMPLIFIER CIRCUITS
1	1	1	1	1	1	0	0		16384-BIT MEMORY ARRAY DATA (65535, 65534)
1	1	1	1	1	1	0	1		
1	1	1	1	1	1	1	1	255	
1	1	1	1	1	1	1	0	254	

Fig. 1.35 Address decoder location

2. Address Decoder

Fig. 1.35 shows the address decoder. To optimize pattern layout, the decoder is arranged as shown in Fig. 1.35. For this reason, with A_0 (row) as the least significant bit and A_7 (column) as the most significant bit, sequential binary addresses will not address adjacent cells in order.

For the arrangement of Fig. 1.35, Table 1.3 shows the addresses that will be accessed for sequentially incremented binary addresses if A_6 (row) is the least significant bit and A_0 (column) is the most significant bit.

Table 1.3 Address coding

	Column								Row							
	(MSB)															(LSB)
Cell No.	A0	A5	A4	A3	A2	A1	A6	A7	A7	A0	A5	A4	A3	A2	A1	A6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
⋮				⋮								⋮				
32767	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
⋮				⋮								⋮				
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3. Bit Topology

For the purposes of simplified explanation, we have assumed thus far that the memory cells are located in an orderly fashion in a matrix. For actual devices, however, techniques required to increase the density on the chip dictate that an arrangement such as shown in Fig. 1.36 is used.

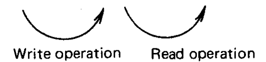
For this reason, this layout must be considered carefully when designing tests which detect interference between adjacent cells.

4. Data Polarity

Because the sense amplifiers are located in the center of the bit lines of the M5K4164AP, half of the data matrix is stored in inverted form. While this has absolutely no effect on actual operation, it must be considered if a test is to be devised which will test all cells in the charged state. This bit inversion pattern is given in Table 1.4.

Table 1.4 Data polarity arrangement

A7 (row)	A0 (row)	Input data	Memory cell data	Output data
0	0	1	1	1
		0	0	0
	1	1	0	1
		0	1	0
1	0	1	0	1
		0	1	0
	1	1	1	1
		0	0	0



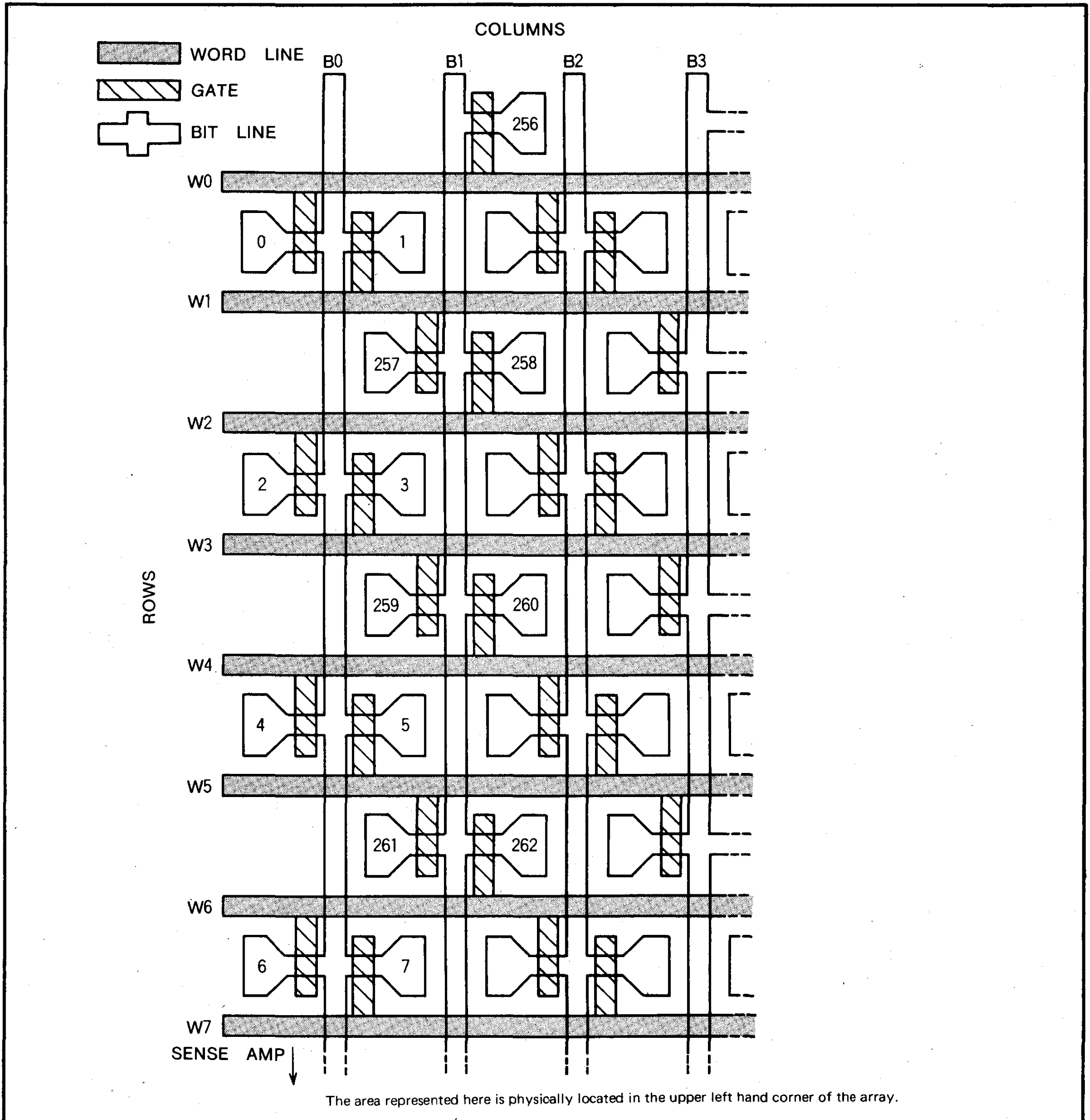


Fig. 1.36 Simplified internal bit topology

Memory System Design Considerations

New memory systems designs are making use of dynamic RAM, static RAM, EPROM and other semiconductor memory devices. All of these devices have some general design considerations in common. This application note will examine some of the delicate timing considerations involved in the design of a dynamic RAM board.

1. Power Distribution

Fig. 1.37 shows the current waveform of an M5K4164AP dynamic RAM. Note that when $\overline{RAS}$ and $\overline{CAS}$ go low, the row or column address latch and buffer are charged, and that when $\overline{RAS}$ and $\overline{CAS}$ go high, the row or column address latch and buffer are precharged, resulting in a transient current waveform. The 60 to 80mA current pulse of approximate width 50ns and a risetime of 10 – 20ns represents the risetime which is observed at 50ms per division. With rise and fall times of this magnitude harmonic noise components above 10MHz are generated. It is therefore necessary when designing the board power distribution to suppress such noise and provide the device with a clean supply voltage. Decoupling capacitors should be used which are capable of charging a small loop.

Fig. 1.38 (a) shows the lumped constant equivalent circuit for a PC board. L_S and R_S represent the PC board inductance and resistance respectively. If we let the L_X and R_S of a 10mil wide 2-ounce copper pattern be 10nH/inch and 4mΩ/inch, then the generated spike voltage is given by the following expression.

$$L_S \cdot \frac{di}{dt} = 10nH \times 10 \times \frac{80mA}{10ns} = 800mV$$

$$R_S \cdot i = 4m\Omega \times 10 \times 80mA = 3.2mV$$

Since the effect of the series resistance R_S compared to that of the series inductance is very small, it may be neglected. The series resistance of L_S is frequency dependent, increasing with increasing frequencies.

To reduce the level of the spike voltage, as shown in Fig. 1.38 (b), a decoupling capacitor is used to decrease the series resistance. This is done by shortening the PC board current loop.

For a 0.1μF capacitor value used with a 250ns cycle RAM, the spike voltage is given by the following expression.

$$V = \frac{1}{C}\int i10dt = \frac{80mA}{0.1\mu F} \times 50ns = 40mV$$

This yields an acceptable value of spike voltage.

It is recommended that ceramic capacitors with good high frequency characteristics are used as the decoupling capacitors in memory arrays. The decoupling capacitor is connected between the memory V_{CC} and the ground with as short a lead dressing as possible. In addition, as bulk decoupling a solid tantalum capacitor is required. This type of capacitor has a better transient response than other large value capacitors and can be used with one capacitor per 16-memory devices between V_{CC} and the ground.

The power supply traces for a memory array should be made as wide as possible and it is recommended that they be arranged in a grid. Fig. 1.39 (a) shows an example of such an arrangement.

As another method, the use of multi-layer boards is possible, and is an effective method in simplifying power distribution.

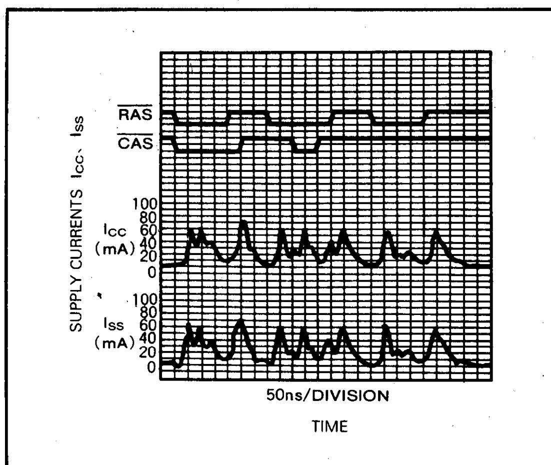


Fig. 1.37 Supply current vs time $\overline{RAS}/\overline{CAS}$ cycle RAS-only cycle

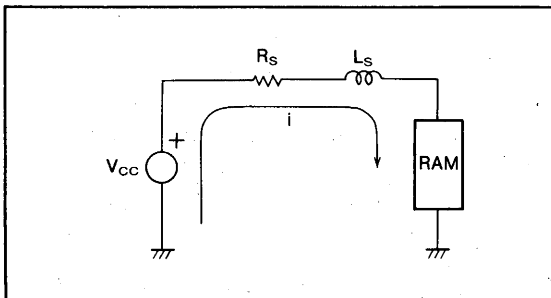


Fig. 1.38 (a) PC board trace equivalent circuit

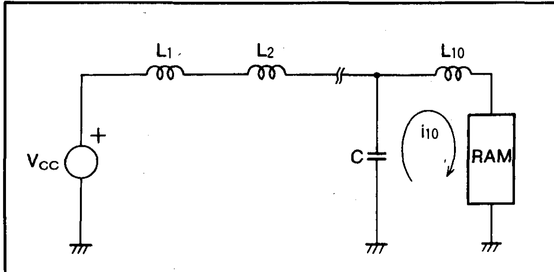


Fig. 1.38 (b) PC board trace equivalent circuit with decoupling capacitors

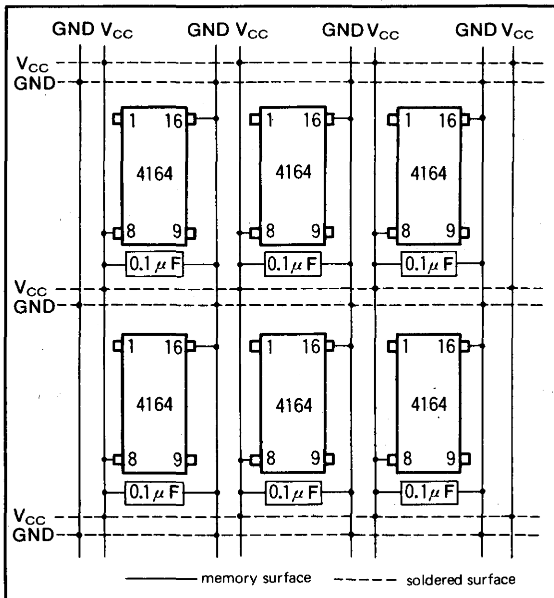


Fig. 1.39 (a) Gridded power distribution and decoupling capacitors

2. Signal Distribution

The next most important consideration in the design of a memory system is the design of memory signal (address, data, and control signals) distribution.

For the case of the M5K4164AP dynamic RAM, two types of chip enable signals exist; $\overline{RAS}$ and $\overline{CAS}$. If these are to be driven by TTL circuits, it is very important to keep the driving TTL device as close as possible to the RAM array. This minimizes the transmission line impedance mismatch between the RAM array loaded line and the TTL driver. Another technique is the use of a damping resistor located close to the driver. The value of this resistor is selected to provide a good waveform at the RAM input, the usual values being in the range 10 to 50Ω. This technique brings the output impedance of the driver close to the line impedance which minimizes waveform overshoot and undershoot.

To eliminate crosstalk from $\overline{RAS}$ and $\overline{CAS}$, the $\overline{RAS}$ and $\overline{CAS}$ signal lines should be kept at 90° to the traces for other signals. If this is impossible, they should be kept as far as possible from traces of other signals. In addition the address and data signal traces should be kept as short as possible. Fig. 1.39 (b) shows an example of a printed board pattern for a 128K-bite memory system.

3. Logical Considerations

Far memory systems with critical timing, it is necessary to consider the propagation delay to surrounding ICs. To minimize signal delay, gate selection and the use of the same IC package for related signals are effective in reducing the difference in delays between signals. To reduce the capacitive loading on drivers, it is necessary to limit the number of drivers per memory array. For $\overline{RAS}$ and $\overline{CAS}$, 8 memories/driver and for address 16 memories/driver are recommended.

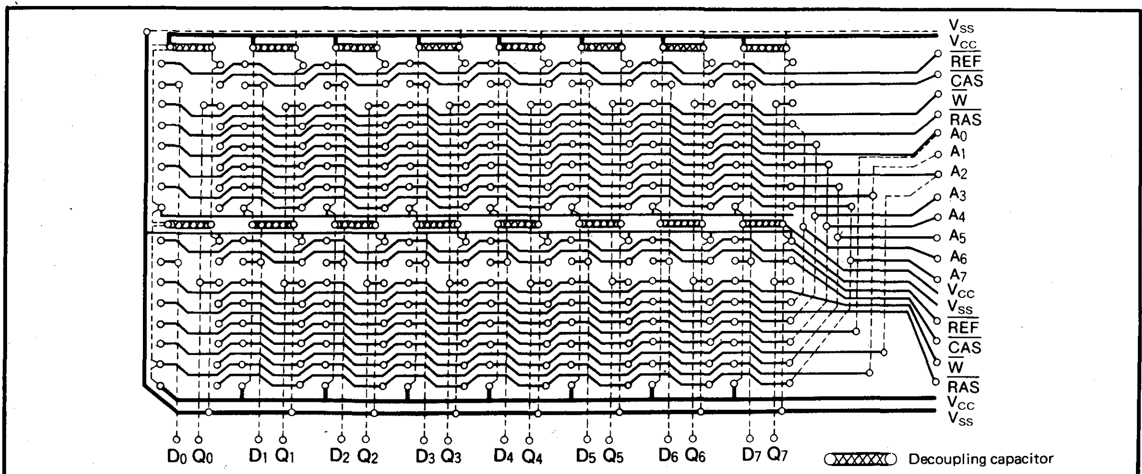


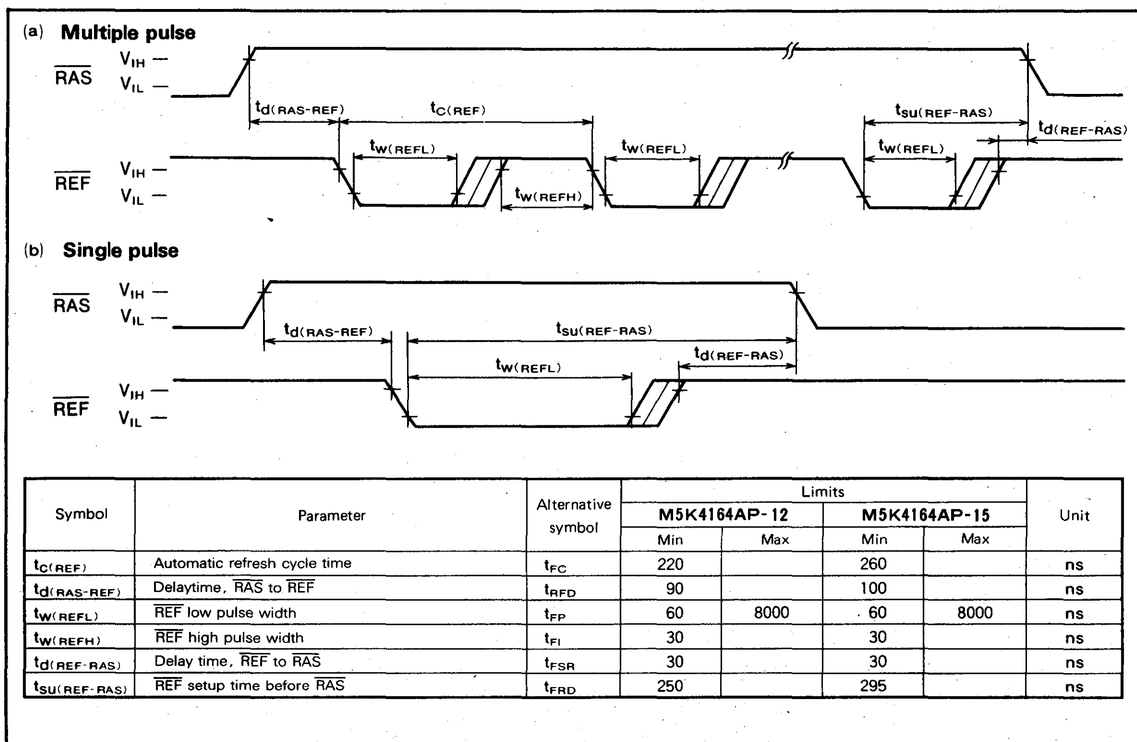
Fig. 1.39 (b) Printed board pattern

M5K4164AP Refresh Methods

The refreshing of the M5K4164AP cell matrix requires the refreshing of 128 row addresses at least every 2ms. In addition to the previously available $\overline{RAS}$-only refresh method, the M5K4164AP provides $\overline{REF}$ (pin 1) automatic refreshing, and self-refreshing. This section will cover the application of $\overline{REF}$ refresh operations.

1. Automatic Refresh

Automatic refresh begins after RAS precharge ($\overline{RAS}$-V_{IH}) upon setting $\overline{REF}$ (pin 1) to low. This method is quite similar to the $\overline{RAS}$-only refresh with the refresh address counter output present as a 7-bit word for automatic refreshing the refresh counter being automatically incremented at the end of the refresh cycle. Fig. 1.40 shows the automatic refresh timing.



Symbol	Parameter	Alternative symbol	Limits				Unit
			M5K4164AP-12		M5K4164AP-15		
			Min	Max	Min	Max	
$t_{C(REF)}$	Automatic refresh cycle time	t_{FC}	220		260		ns
$t_{d(RAS-REF)}$	Delaytime, $\overline{RAS}$ to $\overline{REF}$	t_{RFD}	90		100		ns
$t_{W(REFL)}$	$\overline{REF}$ low pulse width	t_{FP}	60	8000	60	8000	ns
$t_{W(REFH)}$	$\overline{REF}$ high pulse width	t_{FI}	30		30		ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FSR}	30		30		ns
$t_{SU(REF-RAS)}$	$\overline{REF}$ setup time before $\overline{RAS}$	t_{FRD}	250		295		ns

Fig. 1.40 Automatic refresh timing

Automatic refresh has many advantages over the $\overline{RAS}$-only refresh method generally used previously. As shown in Fig. 1.41, $\overline{RAS}$-only refresh generally requires logic circuitry. This consists of the row-address, column-address and refresh address multiplexer and refresh address counter. With automatic refresh, the dotted area shown in Fig. 1.41 may be eliminated.

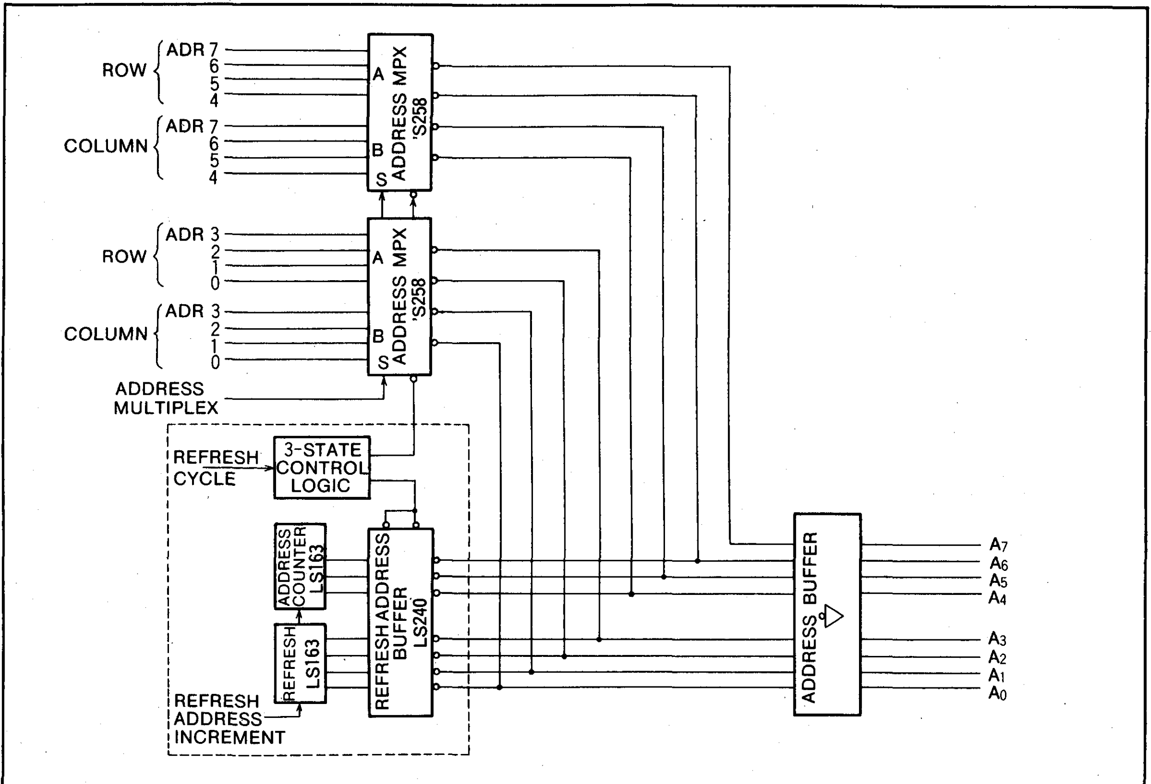


Fig. 1.41 Address multiplexer and refresh address counter

By decoding $\overline{RAS}$, one bank of a complex memory system may be selected, while for $\overline{RAS}$-only refresh $\overline{RAS}$ is fed to all portions of the memory requiring the decoder as shown in Fig. 1.42 (a). With automatic refresh, $\overline{RAS}$ is used during the memory cycle and $\overline{REF}$ for the refresh cycle independently so that the gate shown in Fig. 1.42 (b) can be eliminated.

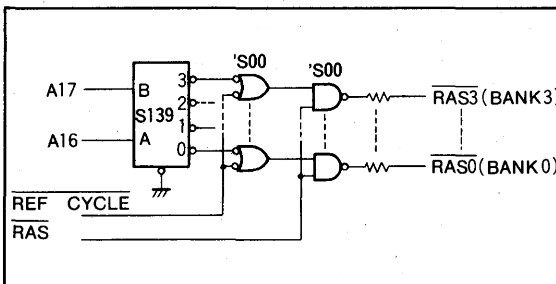


Fig. 1.42 (a) $\overline{RAS}$ decoder in $\overline{RAS}$-only refresh

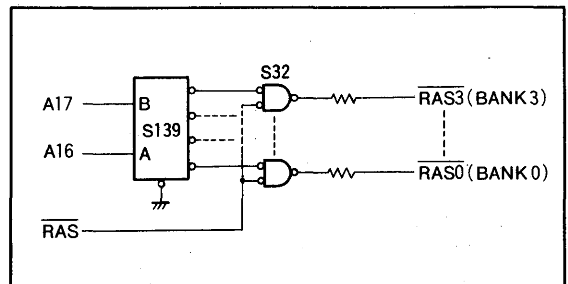


Fig. 1.42 (b) $\overline{RAS}$ decoder using $\overline{REF}$ pin

Another feature of automatic refresh is that the timing of the refresh controller is simplified. The timing for $\overline{RAS}$-only refresh and automatic refresh is shown in Fig. 1.43 (a) and Fig. 1.43 (b) respectively.

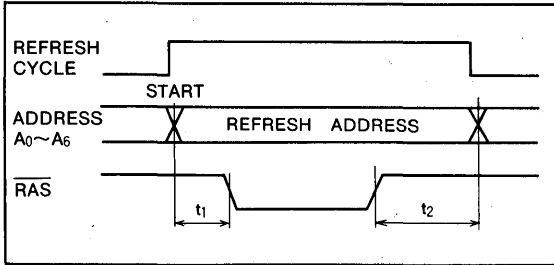


Fig. 1.43 (a) $\overline{RAS}$-only refresh timing

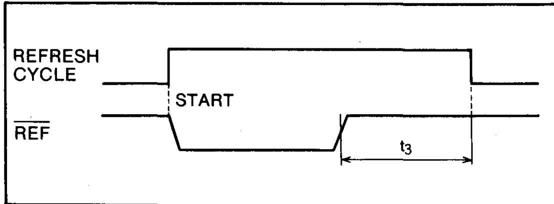


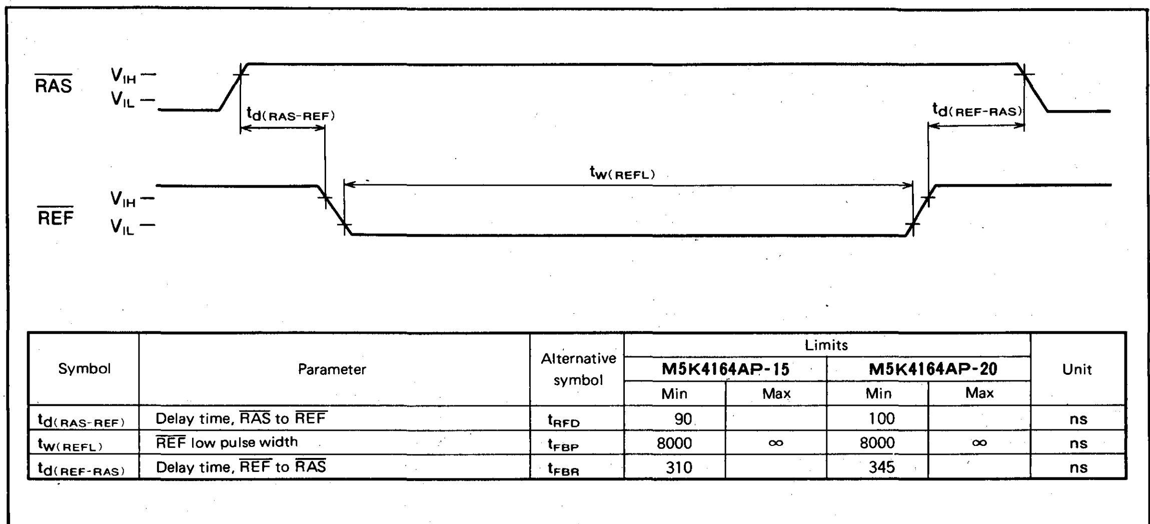
Fig. 1.43 (b) Automatic refresh timing

For $\overline{RAS}$-only, the controller disables the address multiplexer upon entering the memory cycle while it enables the refresh counter output. Next, after a delay time of t_1 (required because of the address buffer delay time and row address setup time $t_{su(RA-RAS)}$, $\overline{RAS}$ is set to low. The refresh cycle ends at the time t_2 that $\overline{RAS}$ is precharging.

In contrast to this, the automatic refresh controller sets $\overline{REF}$ to low simultaneously with the beginning of the refresh cycle, and after the $\overline{RAS}$ precharge time t_3, the refresh cycle ends. For this reason, there is no necessity to consider the settling time for address selection.

2. Self Refresh

Self refresh, similar to automatic refresh, sets $\overline{REF}$ low after $\overline{RAS}$ precharge occurs, beginning the internal refresh cycle. This method of refresh ignores all other inputs as long as $\overline{RAS}$ is high and $\overline{REF}$ is low, making use of an internal timer to automatically refresh the row addresses every 12 – 16μs which enables all cells to be refreshed within 2ms. The rising edge of $\overline{REF}$ terminates the refresh operation and after one cycle ($t_{d(REF-RAS)}$) a normal read-write cycle is entered. Fig. 1.44 shows the timing for the self refresh cycle. Self refresh is an extremely effective method of providing memory backup by means of a secondary power supply. As shown in Fig. 1.45, most of the required functions are implemented within the chip for the $\overline{RAS}$-only refresh with a simplified external circuit. This results in low power consumption and a long life for the secondary power supply.



Symbol	Parameter	Alternative symbol	Limits				Unit
			M5K4164AP-15		M5K4164AP-20		
			Min	Max	Min	Max	
$t_{d(RAS-REF)}$	Delay time, $\overline{RAS}$ to $\overline{REF}$	t_{RFD}	90		100		ns
$t_{w(REFL)}$	$\overline{REF}$ low pulse width	t_{FBP}	8000	∞	8000	∞	ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FBR}	310		345		ns

Fig. 1.44 Self-refresh timing

As described above, self refresh may not be used in the $\overline{RAS}$-only refresh mode. In designs using two refresh counters (internal and external) which operate independently, guaranteeing the refresh (2ms) time is difficult.

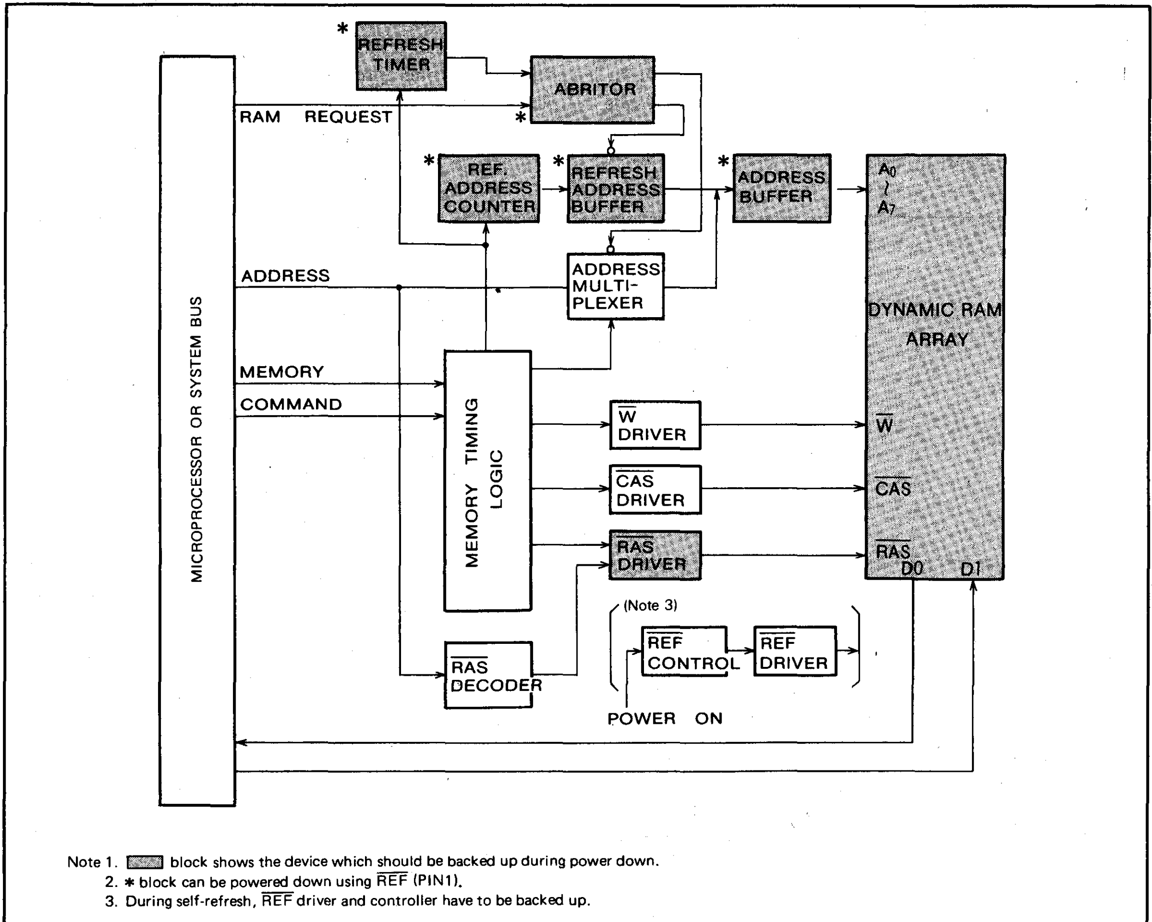


Fig. 1.45 Typical dynamic RAM system with battery back up

3. Design Example

The design example shows the increased effectiveness of $\overline{REF}$ (pin 1) refresh when the M5K4164AP is used as the memory for a microprocessor. This design example illustrates the interface between the M5K4164AP and the microprocessor.

When using $\overline{REF}$ for the microprocessor memory in interface, two methods are possible. One is asynchronous refresh and the other involves synchronously refreshing the memory. The former technique is not affected by the microprocessor status (i.e., reset, wait state, DMA, and CPU clock). However, control logic is somewhat complex. While the second method makes use of simple control logic, the microprocessor must satisfy the refresh operation timing conditions.

Fig. 1.46 through 1.48 show the block diagram, schematic diagram, and timing deiagram for the asynchronous refresh example. For this example, the refresh cycle counter refresh request ($\overline{REFREQ}$) starts the refresh cycle independently of the microprocessor operation. The arbiter determines whether the microprocessor ($\overline{RAMREQ}$) or refresh cycle counter ($\overline{REFREQ}$) has access to the RAM.

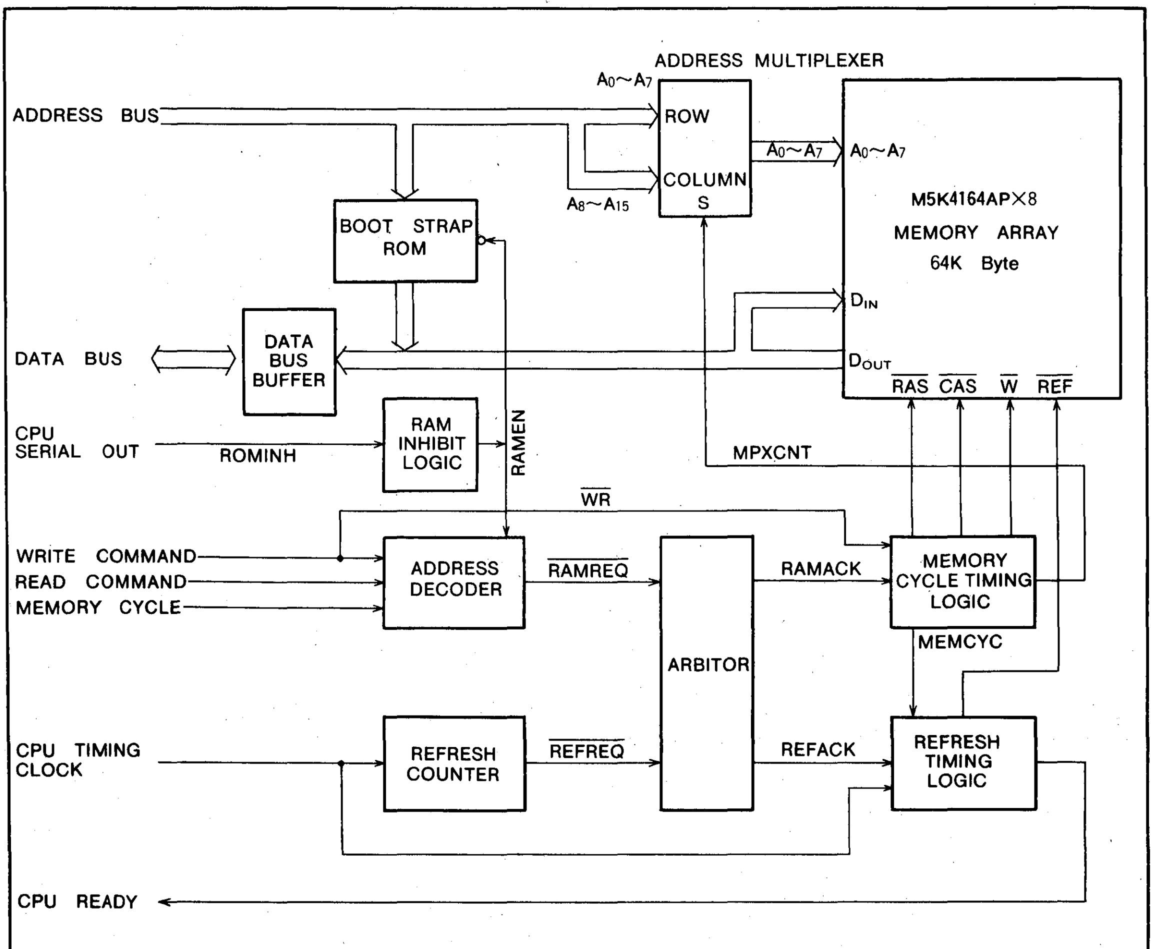


Fig. 1.46 Block diagram of the design example (Ansynchronous)

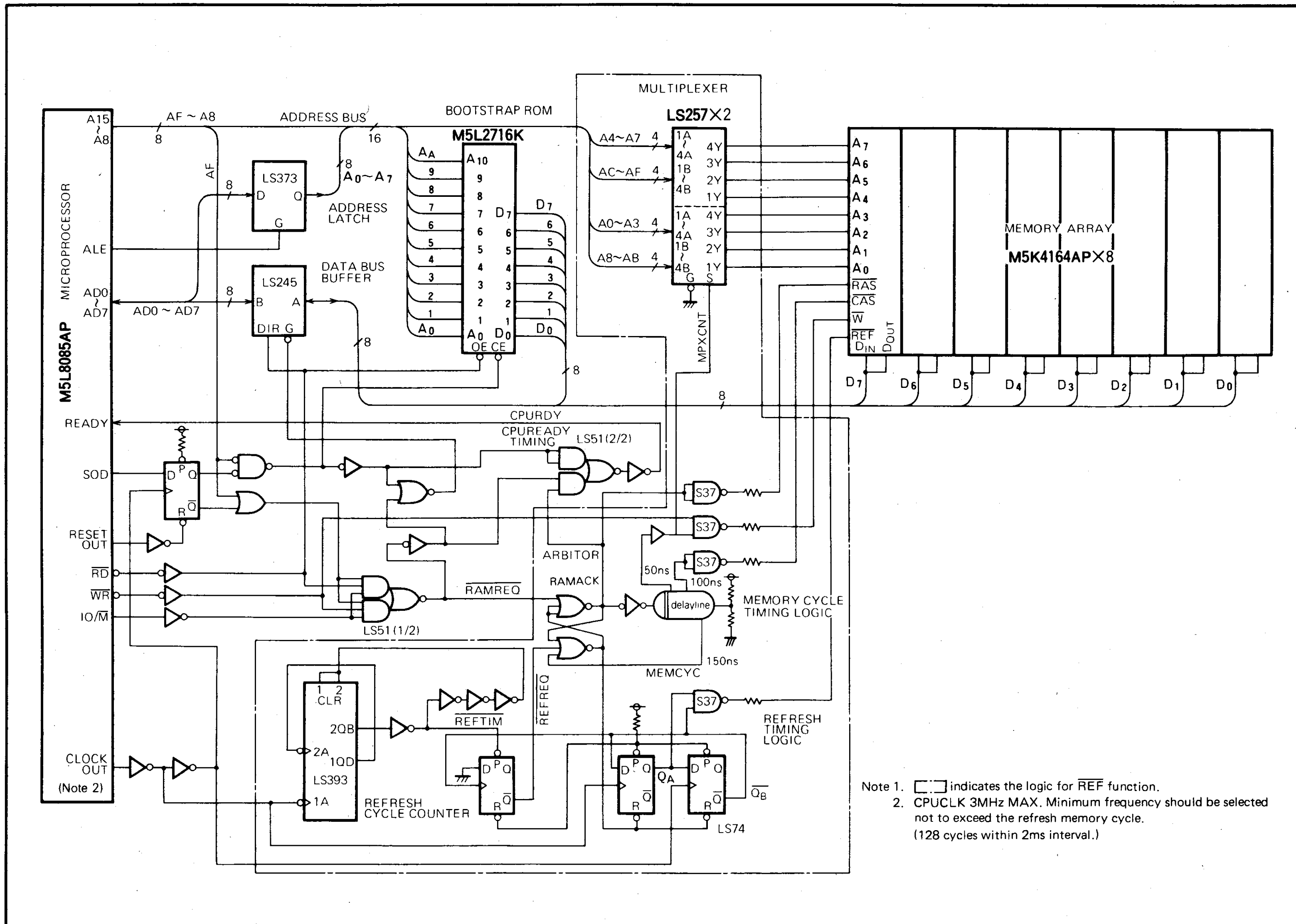
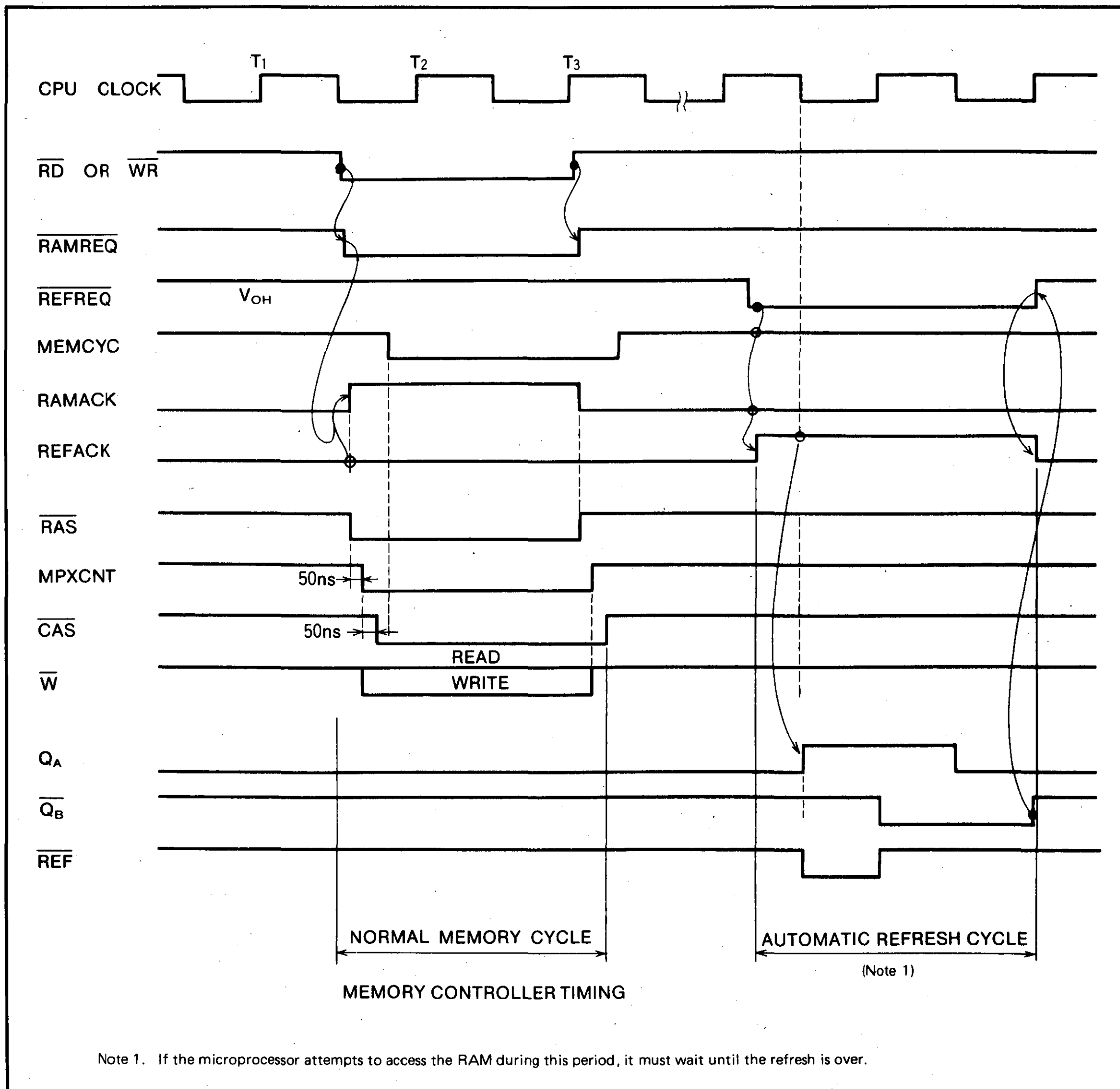


Fig. 1.47 Design example of microprocessor interface (Ansynchronous)



Note 1. If the microprocessor attempts to access the RAM during this period, it must wait until the refresh is over.

Fig. 1.48 Memory and refresh timing (Ansynchronous)

A bootstrap ROM, commonly used in this type of memory system, is shown in the example. This is used to load the initial program of a RAM-based system into RAM from disk, for system initialization. In this example, the SOD (Serial Out Data) of the M5L8085AP is used to select either the bootstrap ROM or RAM as shown in Fig. 1.49.

Fig. 1.50 and 1.51 show the schematic diagram and timing for the synchronous refresh example. In this example a Z80 microprocessor is used with synchronous refresh. As shown in Fig. 1.51, after the Z80 fetch instruction, the refresh operation is performed (T_3 and T_4 state).

In this manner refresh is performed synchronously with microprocessor operation. As mentioned previously, this type of operation involves a variety of limitations which must be considered carefully when designing such a system. (i.e., wait state, DMA, reset and CPU clock cycle)

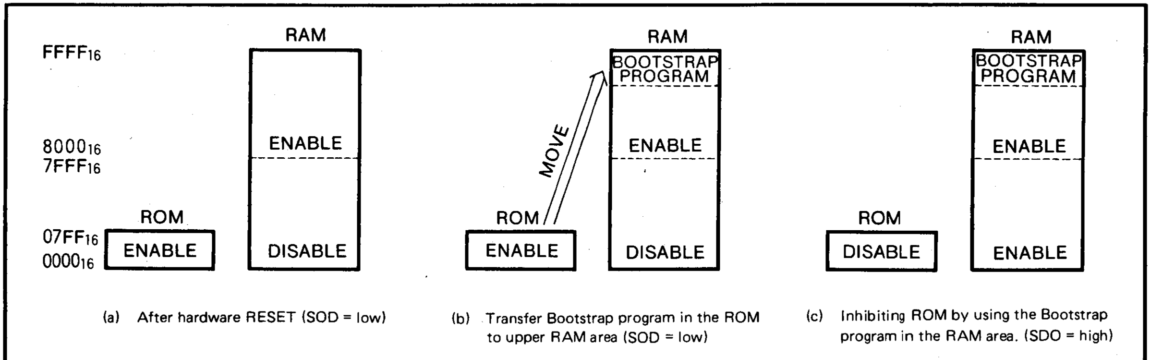


Fig. 1.49 Start-up procedure of the memory-overlapped system

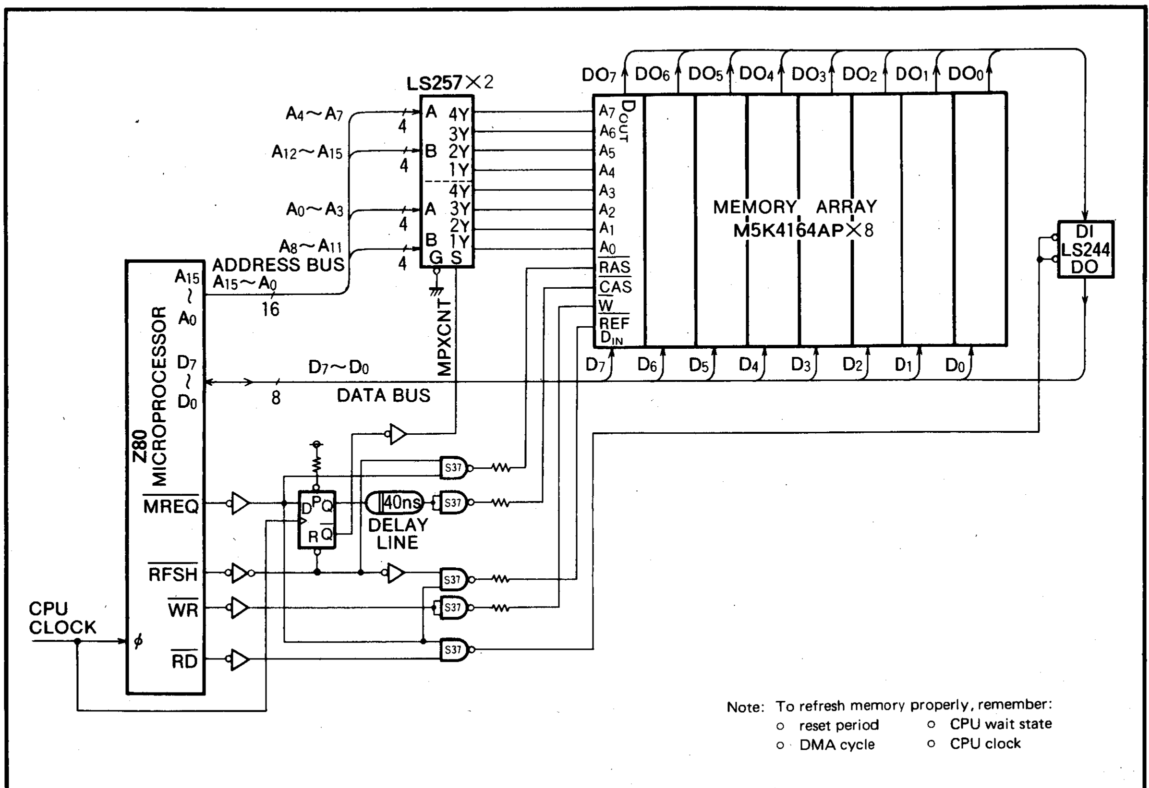


Fig. 1.50 Design example of microprocessor interface (Synchronous)

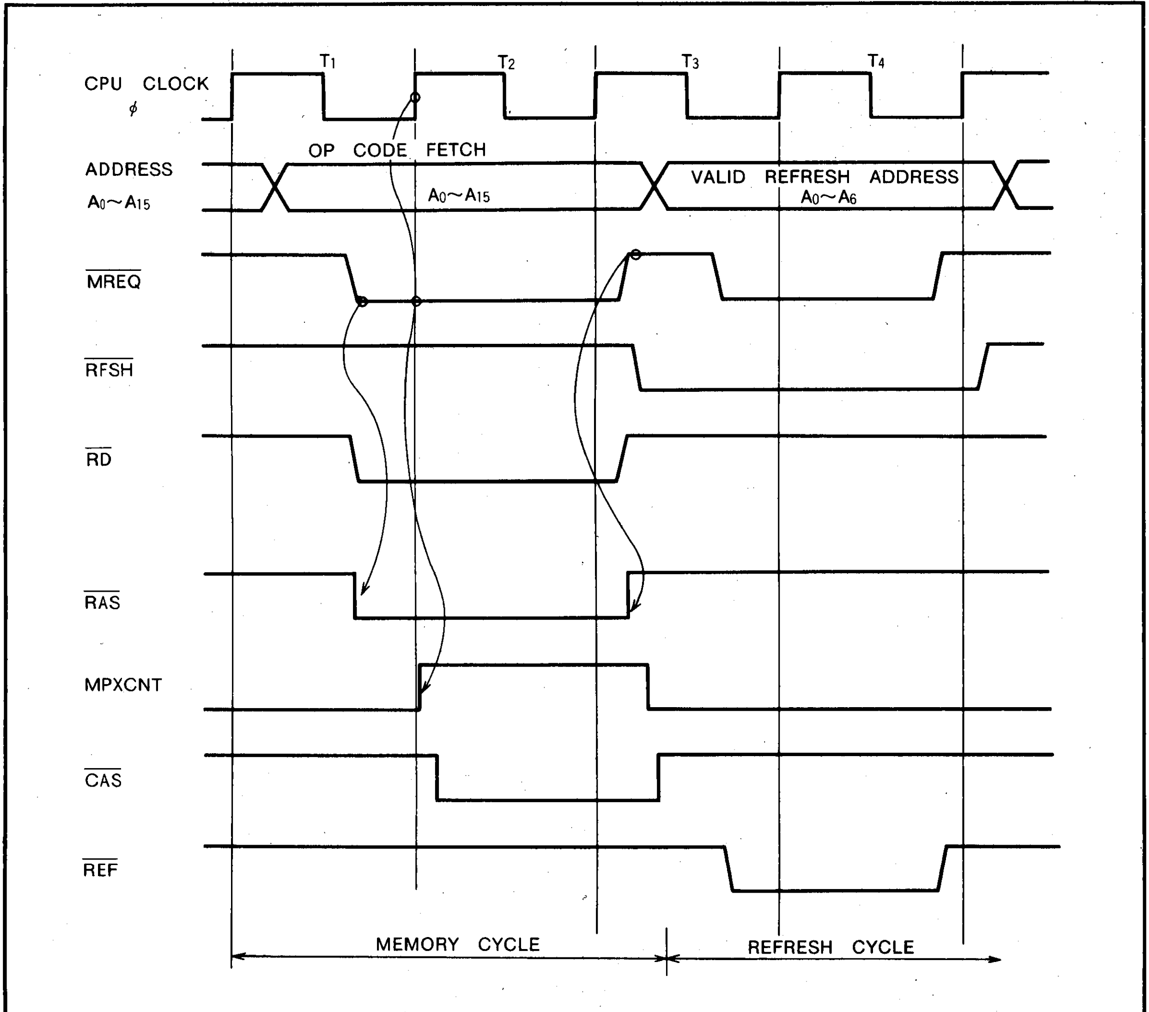


Fig. 1.51 OP code fetch and refresh timing

MITSUBISHI ELECTRIC

APPLICATION OF 256K-BIT DYNAMIC RAM

1. Concepts of the $\overline{CAS}$ before $\overline{RAS}$ refresh function

Several kinds of data refresh method are supported for the dynamic MOS RAM (DRAM). In that, $\overline{RAS}$ only refresh method is the most popular one and all the dynamic MOS RAMs have this function. On the other hand, Mitsubishi 256K bit dynamic MOS RAM families M5M4256/M5M4257, support new data refresh method called $\overline{CAS}$ before $\overline{RAS}$ refresh function.

Figs. 1, 2 show the clock timing of $\overline{RAS}$ only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh, respectively. $\overline{RAS}$ only refresh initiates at the falling edge of $\overline{RAS}$ clock while $\overline{CAS}$ remains at "High" level. In this case, refresh row addresses are applied externally. On the other hand, $\overline{CAS}$ before $\overline{RAS}$ refresh method initiates the data refresh when $\overline{CAS}$ clock falls "low" before the $\overline{RAS}$ clock activation. In this case, refresh row addresses are generated internally. External addresses are ignored. Since $\overline{CAS}$ before $\overline{RAS}$ refresh method does not need specified refresh row address externally that the scheme has an advantage to eliminate some hardware on the memory board.

M5M4256/M5M4257 also offer Hidden refresh function as shown in Fig. 1.54. Hidden refresh (or Hidden $\overline{CAS}$ before $\overline{RAS}$ refresh) is performed while maintaing $\overline{CAS}$ at its "Low" level and executing $\overline{RAS}$ only cycle after the normal read/write cycle. If normal cycle is read cycle, then output data Q is valid until $\overline{CAS}$ goes "High".

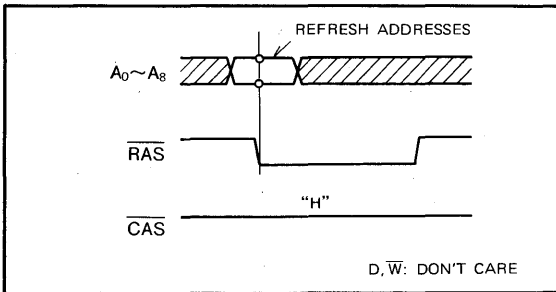


Fig. 1.52 $\overline{RAS}$ only refresh timing

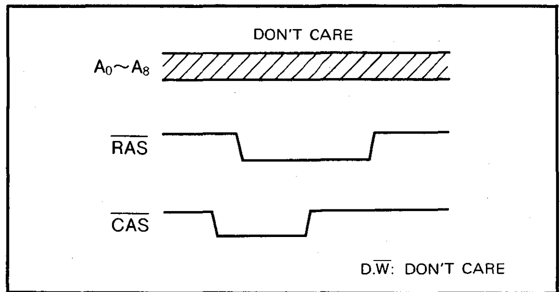


Fig. 1.53 $\overline{CAS}$ before $\overline{RAS}$ refresh timing

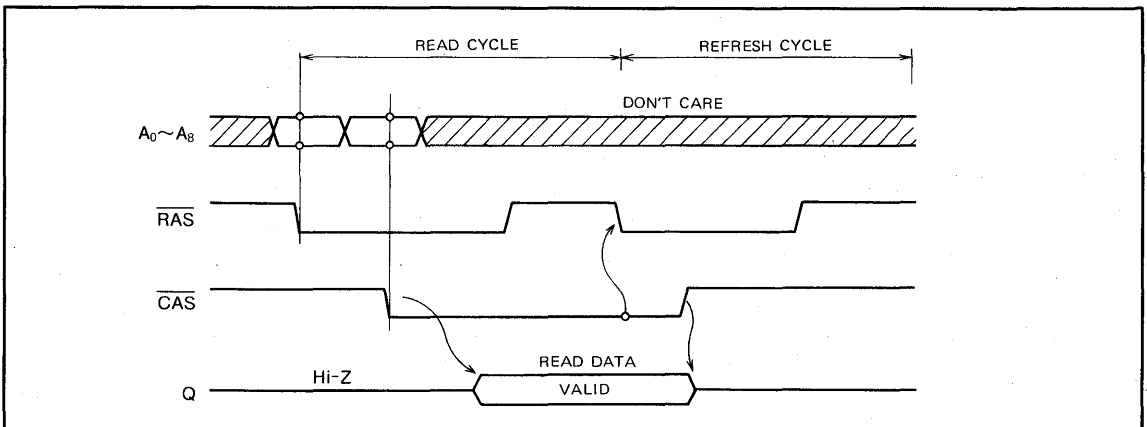


Fig. 1.54 Hidden $\overline{CAS}$ before $\overline{RAS}$ refresh timing

2. DRAM controller using $\overline{CAS}$ before $\overline{RAS}$ refresh

DRAM controller which uses $\overline{CAS}$ before $\overline{RAS}$ refresh is shown in this section. To consider DRAM controller, an object of processer (CPU) shall be specified. Here, following items are assumed (equivalent CPU; 8086, 68000, 32016 etc.)

(1) CPU
- Data bus: 16 bits
- Address space: more than 1M bytes
  (Address are assigned for every bytes. Memory access for each byte is also possible.)

(2) DRAM
- Capacity: 1M bytes (M5M4256/M5M4257 x 32)

(3) Interface signal with CPU (refer Fig. 1.55)
- Data bus: 16
- Address bus: 19 ($A_0 \sim A_{19}$)
  (A_0 is used to specify upper byte or lower byte.)
- High byte enable*: 1
  (Signal which shows that upper byte of memory being accessed. Equivalent to 8086's $\overline{BHE}$ or 68000's $\overline{UDS}$.)
- Low byte enable*: 1
  (Signal which shows that lower byte of memory being accessed. Equivalent to 8086's A_0 or 68000's $\overline{LDS}$.)
- Read command*, Write command*: 1 each
- Ready: 1
- DRAM request: 1
  (Signal from address decoder which shows that DRAM being selected.)

Note 1. * means negative logic.
Note 2. Both High byte enable and Low byte enable become active when data are accessed by 16 bits.

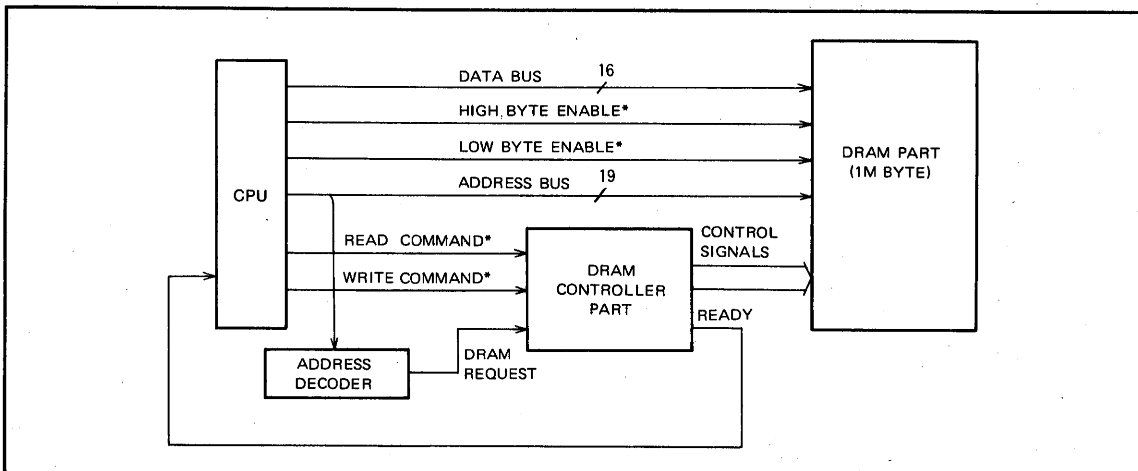


Fig. 1.55 Interface with CPU

(4) Timing requirement

Timing requirement of the signals above are shown in Fig. 1.56 These timing are completely acceptable to 8086, 68000 and 32016.

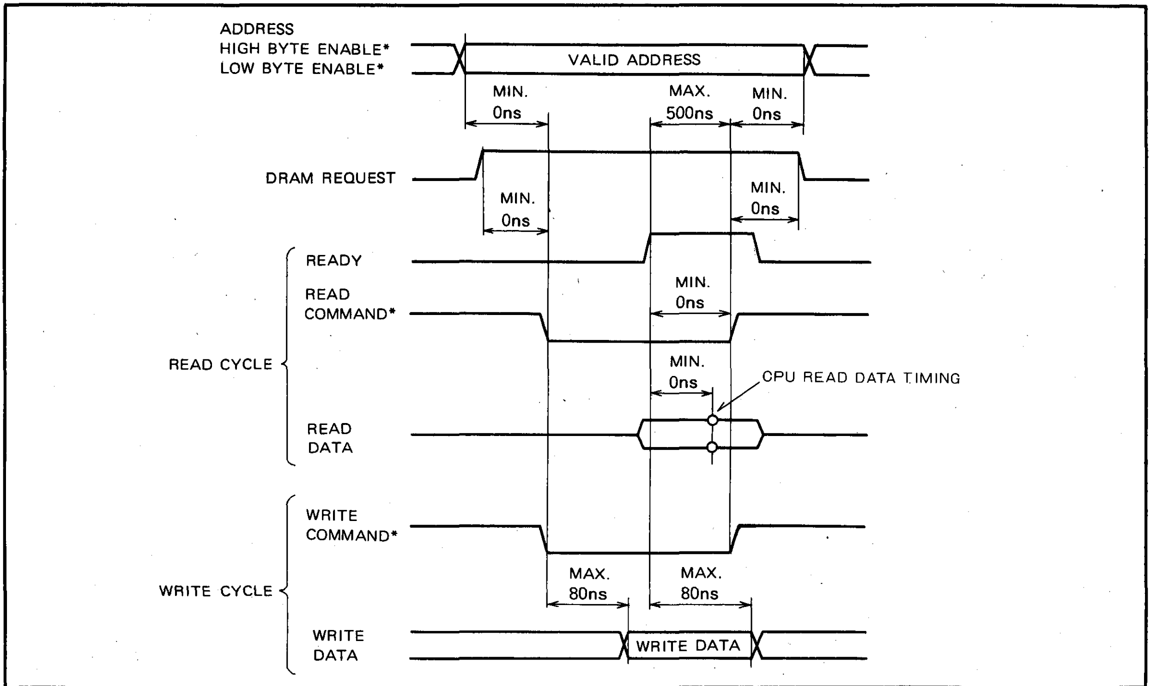


Fig. 1.56 Access timing condition of CPU

2-1 DRAM Controller

Fig. 1.57 shows DRAM controller circuit. In the Figure (also hereafter), signals surrounded by ▭ are interface signal between CPU. Other signals are control signals applied to the memory block. DRAM controller is composed by following 3 main parts.

(1) Refresh timer

This timer generates refresh request signal periodically and composed of LS112, LS393 in the Figure. Here, LS112 works as divided by 3 counter and $2Q_D$ of LS393 becomes to be "High" 128 clocks after the resetting that refresh request signal is generated every 15.3μsec. That is,

$$\frac{1}{25\text{MHz} \times 3 \times 128} = 15.3\mu\text{sec.}$$

(2) Refresh arbiter

This part makes the decision of access requirement from CPU and refresh requirement. The arbiter is composed of the gates F1, F2 and some peripheral gates. Access requirement and refresh requirement are decided by as follows.

(i) F1 = 0, F2 = 0
    Nothing to be done.

(ii) F1 = 1, F2 = 0
    F2 to be 1 is prohibited by G1 and read cycle or write cycle are executed.

(iii) F1 = 0, F2 = 1
    F1 to be 1 is prohibited and refresh cycle is executed.

(iv) F1 = 1, F2 = 1
    F1 is reset and refresh cycle is executed.

Here, F1 and F2 use S112 since high speed operation of gate F1 and F2 are required.

(3) Timing generator

This part generates timing signals needed for DRAM operation and is composed of LS164 and some peripheral gates. LS164's reset condition is absolved by F1 to be 1 or F2 to be 1, and LS164 shifts "High" signal for every one clock from Q_A. Peripheral gates generate the required signals by using these signals (refer Figs. 1.59 and 1.60 for these timing). In the Fig. 1.57, gate G3 has special function at $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. Here $\overline{CAS}$ clock becomes active by G3 when refresh requirement appears. This is compared with $\overline{RAS}$ only refresh method where $\overline{CAS}$ clock is not activated.

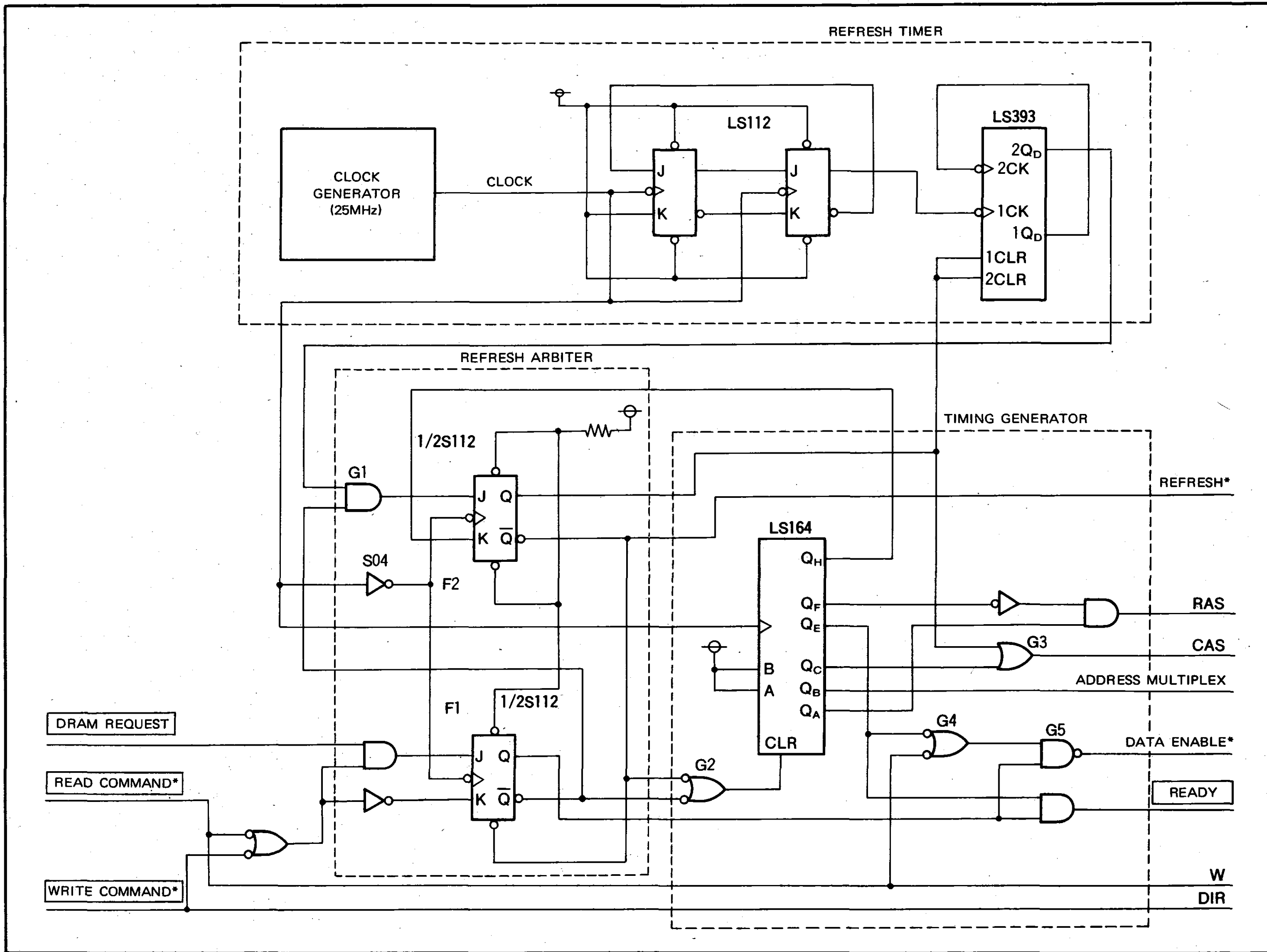


Fig. 1.57 DRAM Controller part

MITSUBISHI ELECTRIC

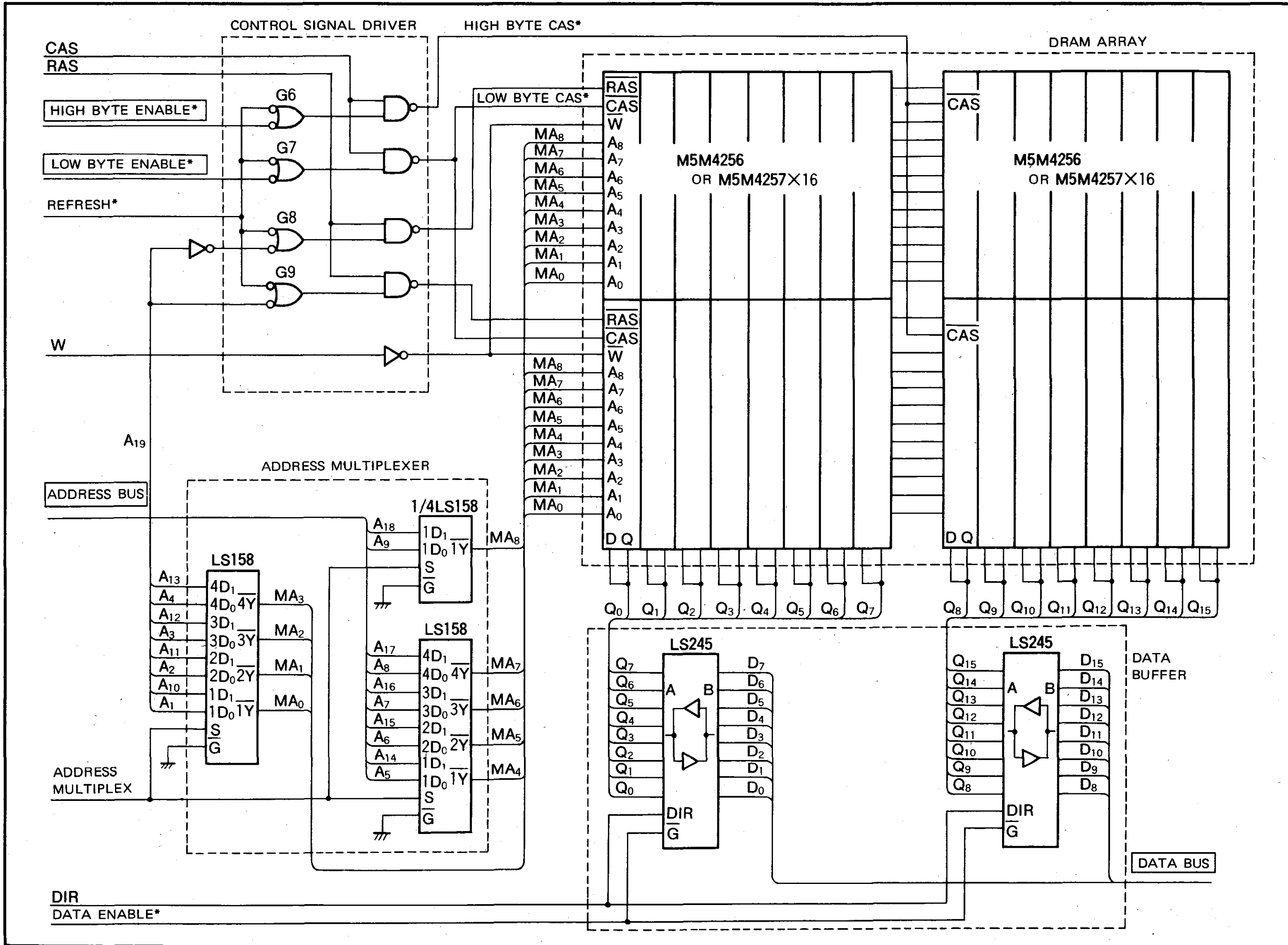


Fig. 1.58 DRAM Part

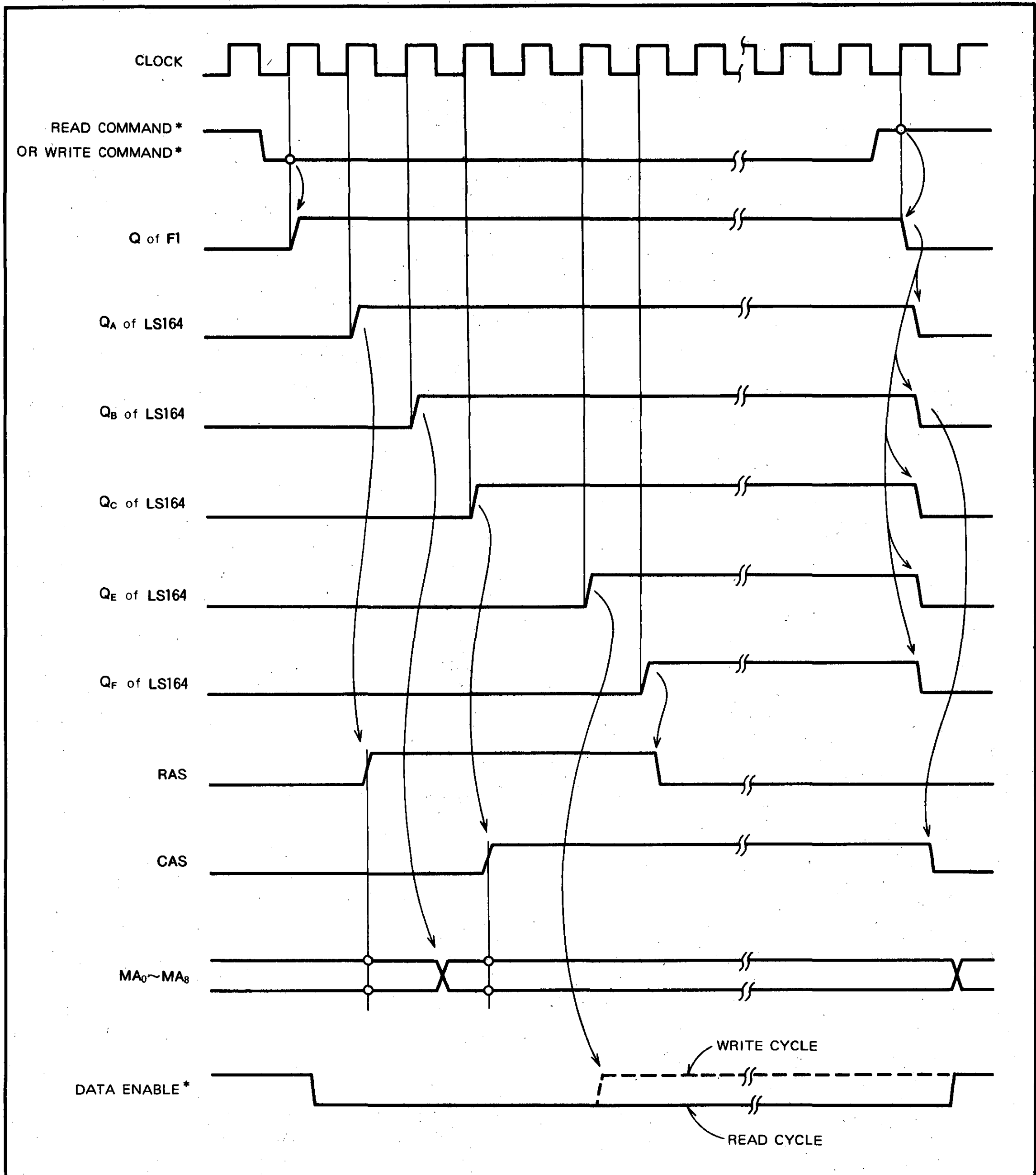


Fig. 1.59 Timing diagram of Read/Write cycle

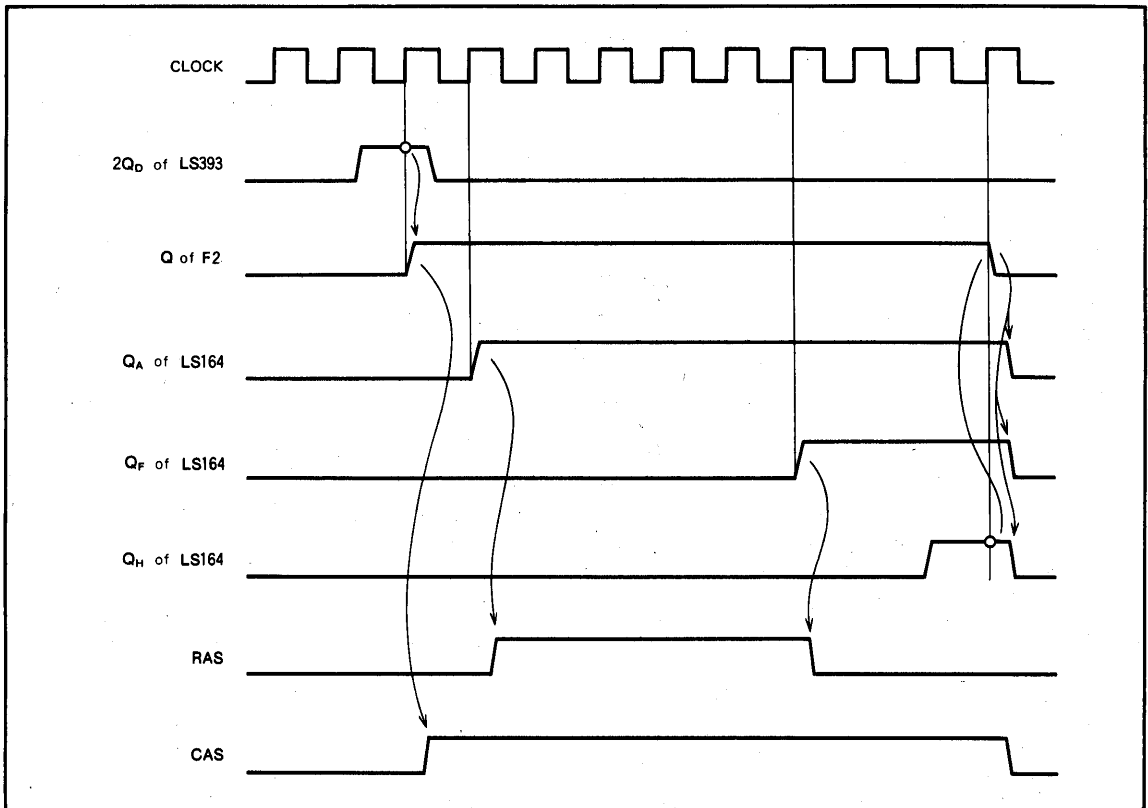


Fig. 1.60 Timing diagram of refresh cycle

2-2 DRAM part

Fig. 1.58 shows DRAM part circuit. The circuit are well known and are composed by following parts.

(1) Address multiplexer

18 address bus are multiplexed by LS158. Address multiplexer becomes very simple like this, since the assignment of refresh address is not required externally. This is an advantage of $\overline{CAS}$ before $\overline{RAS}$ refresh scheme.

For the comparison, additional refresh address counter and $\overline{CAS}$ control circuit changes required in $\overline{RAS}$ only refresh method are shown in Fig. 1.61. In Fig. 1.61, refresh addresses $MA_0 \sim MA_7$ are tied with the output of address multiplexer, $MA_0 \sim MA_7$. The elimination of refresh address counter is an advantage of $\overline{CAS}$ before $\overline{RAS}$ refresh method.

(2) DRAM arrays

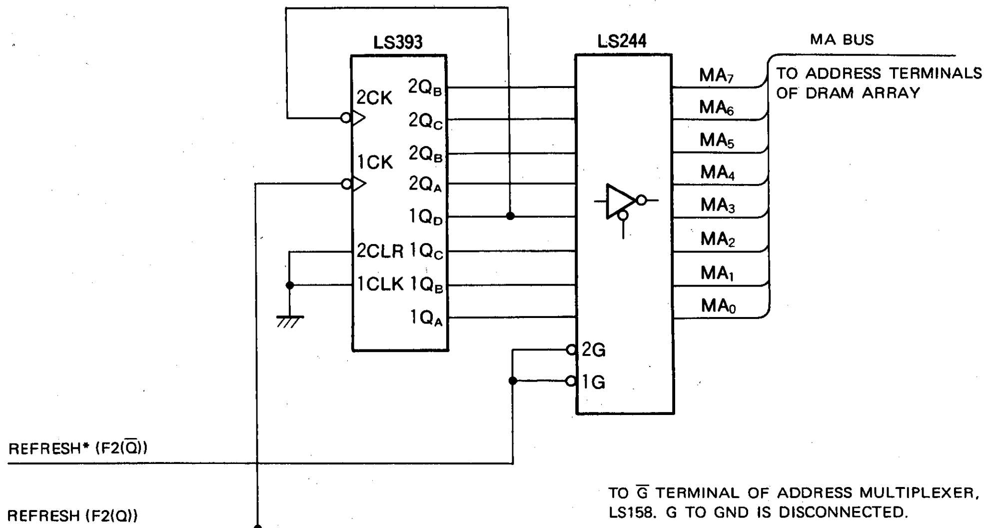
512K words (1M bytes) system are realized by using only 32 pcs of M5M4256/M5M4257. Upper byte or Lower byte of 16 words can be accessed independently by controlling $\overline{CAS}$ clocks individually.

(3) Control signal driver

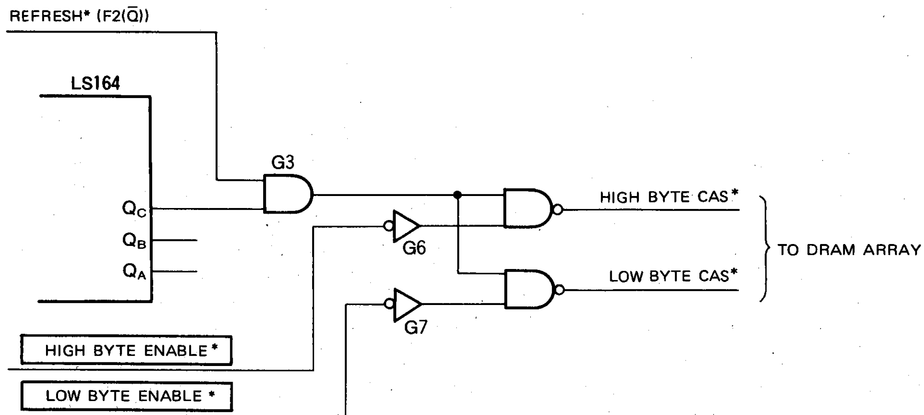
Control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ are driven by control signal driver and applied to DRAM arrays. Address A19 controls upper address and lower address. Also High byte enable, Low byte enable controls Upper byte and Lower byte. When RAMs are refreshed, these signals are absolved by G8 and G9, and all RAMs suffer $\overline{RAS}$ and $\overline{CAS}$ activation. This condition refreshes the RAMs.

(4) Data buffer

Data buffers are composed of 2 pcs. of bi-directional LS245. Control signals DIR and $\overline{G}$ are generated by DRAM controller.



(a) Additional circuits



• G3 IS CHANGED TO AND GATE. REFRESH* IS APPLIED TO THE GATE.
• G6 AND G7 ARE CHANGED TO INVERTER.

(b) Changes of $\overline{CAS}$ control circuit

Fig. 1.61 Additional circuits and changes required in $\overline{RAS}$ only refresh method

3. Interface example with 8086

Interface example explained in Section 2. is applicable for all CPU if interface specification are satisfied. It does not concern the kind of CPU or clock frequency of the CPU. But due to the general purpose of the usage, some faults appear.

(1) Since the clock sequence between CPU and DRAM controller is not synchronized that some period to synchronize both operation are needed. This delays real/ write time.

(2) DRAM controller becomes complicated, somehow.

Here an example of interface circuit using 8086 is shown in which DRAM controller synchronizes with CPU clock sequence.

3-1 CPU part

Fig. 1.62 shows the circuit. 8086 is used with 8MHz frequency. In general, 8086 uses a custom clock generator IC, 8284A, 8284A makes 8MHz clock frequency by dividing 3 from original 24MHz oscillation with crystal, and this 8MHz clock can be applied to 8086. But in case of 8284A, phase difference between original clock and divided clock is too large that as an example here, clocks divided by 3 by S112 from 24MHz original clock are used to 8086's clock. Phase difference in this case becomes less than 5 nsec.

READY and RESET input signals are also applied by synchronizing with clock when used 8284A, originally. But here again, READY signal only is synchronized by S74 (RESET signal is not necessary to be synchronized). Other circuits are well known circuit for 8086, 8288 is used as bus controller. LS373 is used as address latch, also.

3-2 Interface circuit

Fig. 1.63 shows interface circuit and DRAM part. 8086 has an address space of 1M byte that, here as an example, 512K byte RAM is considered by using 16 pcs. of M5M4256 or M5M4257, LS158 are used as address multiplexer.

DRAM controller circuit is essentially same circuit as shown in Fig. 1.57. Here, clock of refresh arbiter S112 is used as clock of 8086 that peripheral timing control becomes simplified. Timing charts are shown in Figs. 1.64 and 1.65. Flip-Flop F1 is used to synchronize the status signals S1* and S2* with clock. In some case of sampling timing of F2, it may happen that status signals S1* and S2* become unstable. The unstable condition is avoided by F1 which synchronizes by using opposite phase of the clock.

LS158 is used as the control signal driver. Control signals are switched between normal access condition and refresh timing. An example cited here has enough margin about access time that LS158 as the control signal drivers is applicable completely. Since DRAM bank is one, switching of $\overline{RAS}$ clock signal by address do not occur.

Also, the circuit cited here is possible to interface with 8086 without wait state except refresh condition.

MITSUBISHI ELECTRIC

Fig. 1.62 CPU Part of 8086

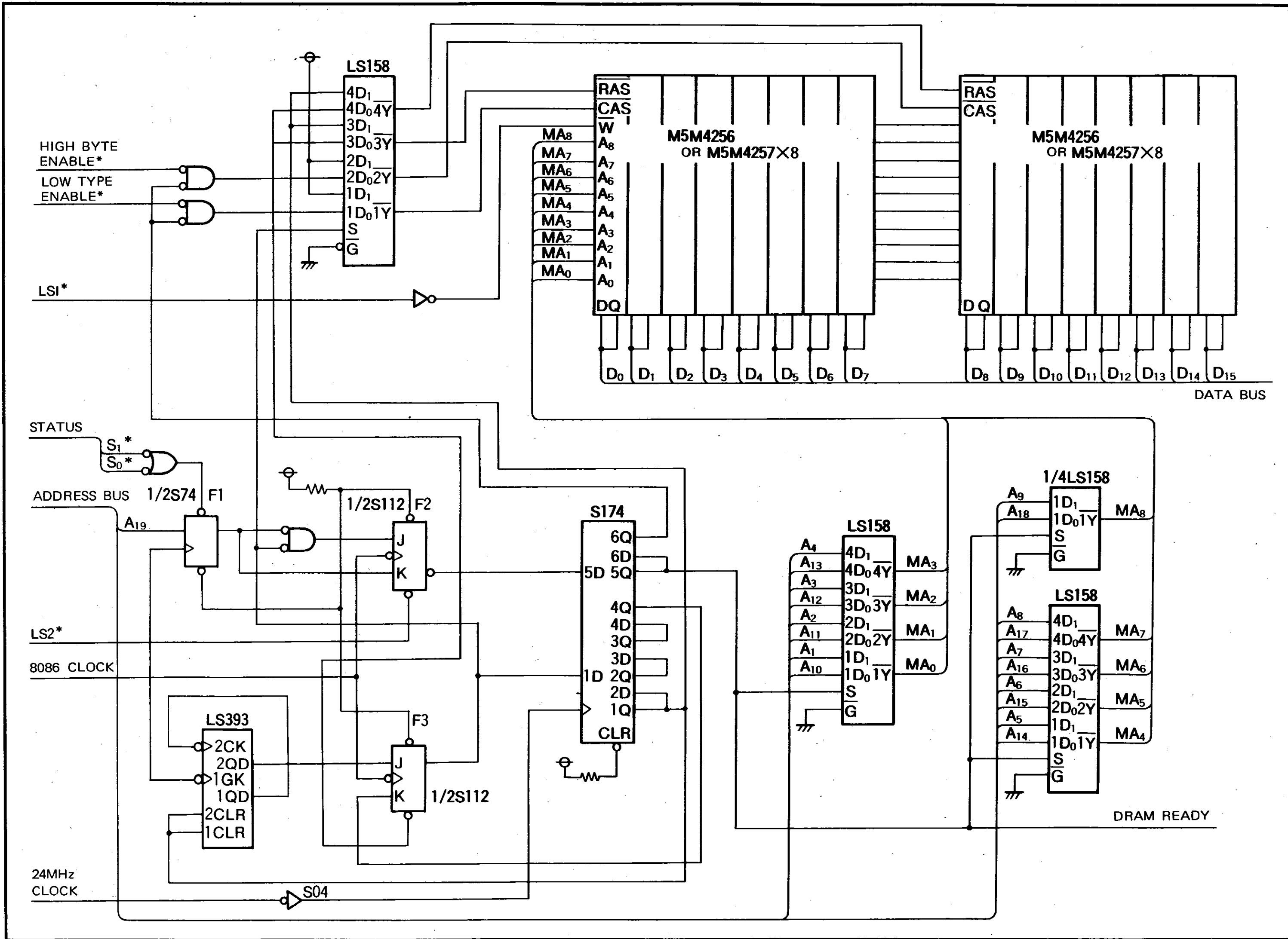


Fig. 1.63 Interface circuit with 8086

MITSUBISHI ELECTRIC

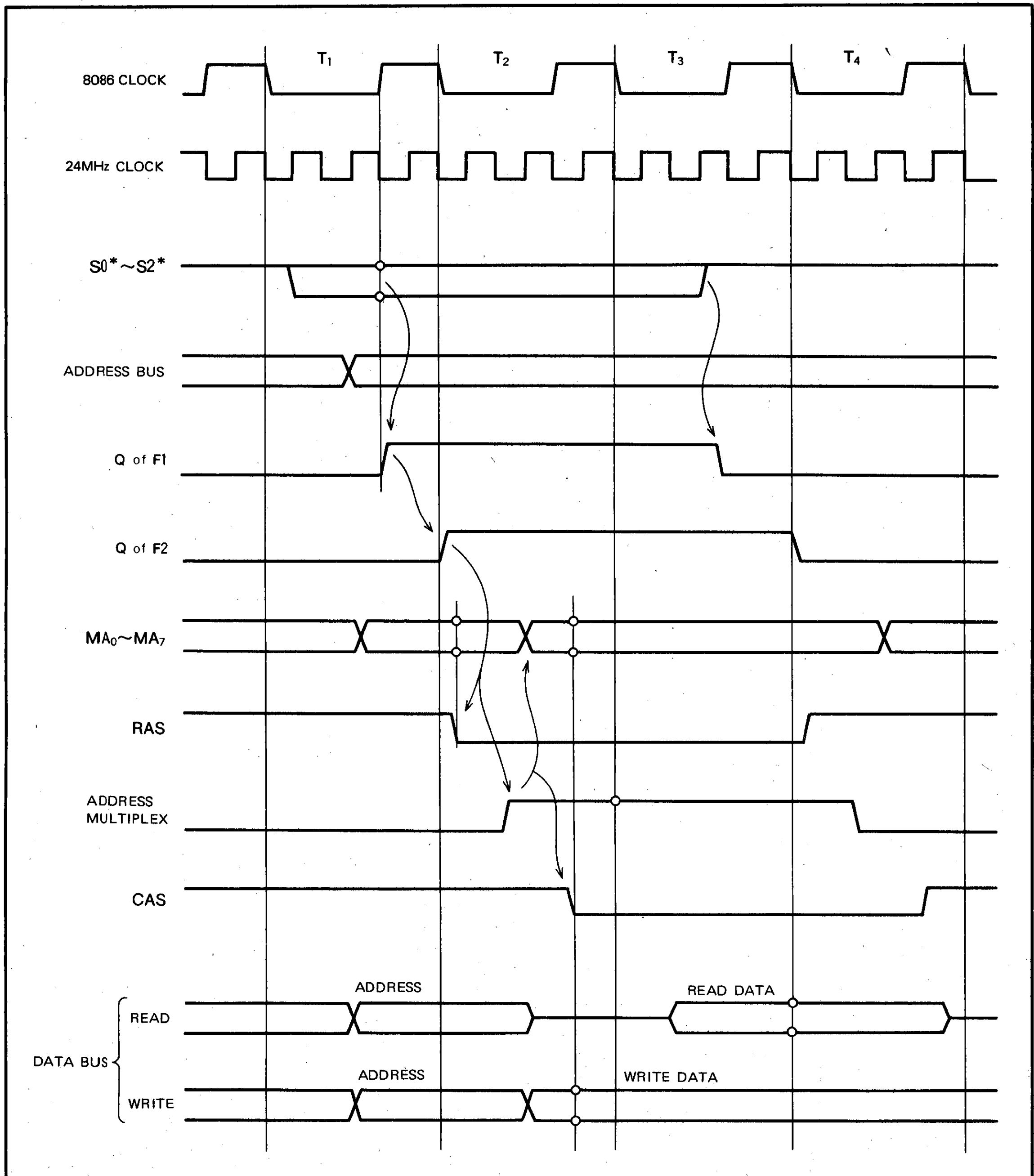


Fig. 1.64 Timing diagram of Read/Write cycle

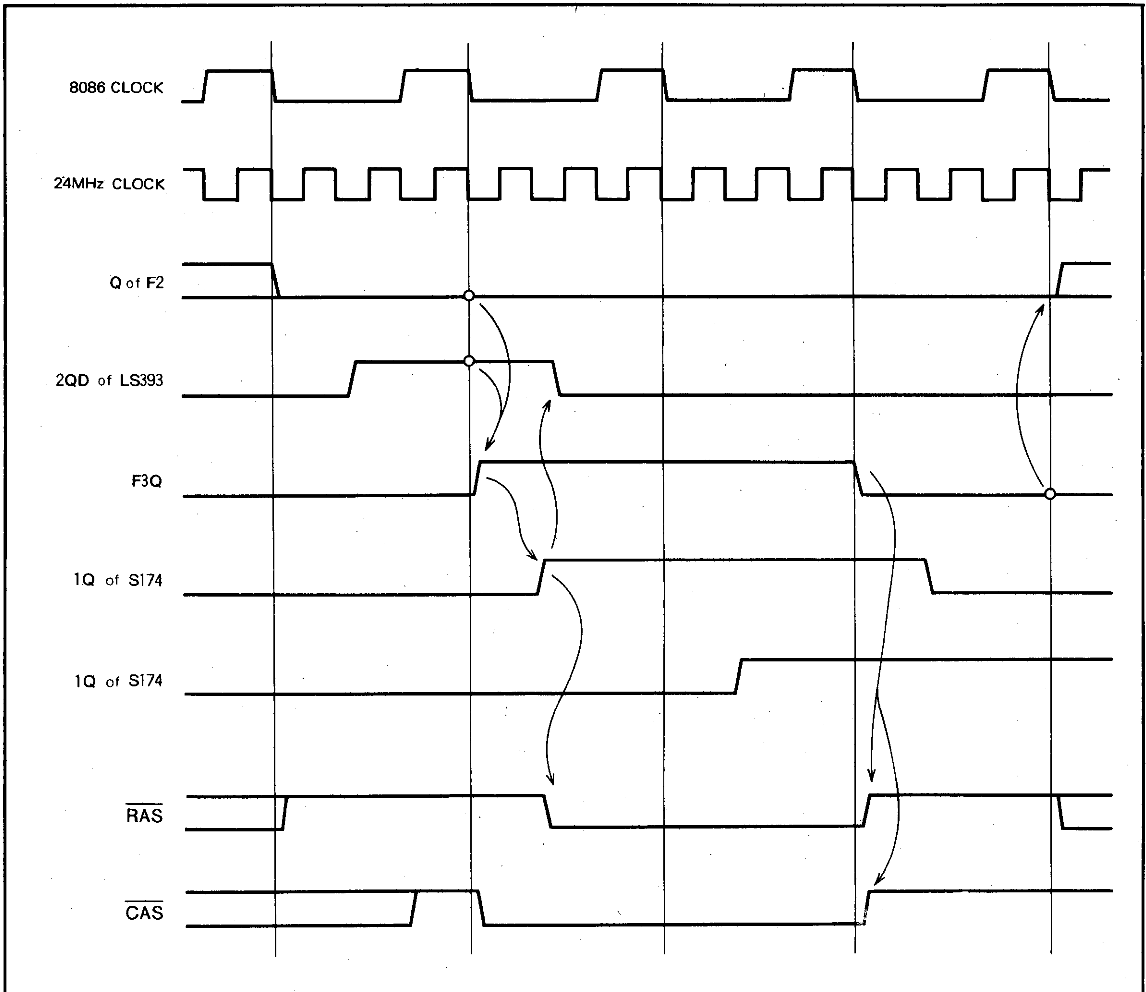


Fig. 1.65 Timing diagram of refresh cycle

Appendix 1. Specification of $\overline{CAS}$ before $\overline{RAS}$ refresh

As discribed in Section 1. if $\overline{CAS}$ falls $t_{SUR(CAR-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state (refer Fig. 1.66).

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available until $\overline{CAS}$ is brought high.

A feature of the M5M4256 is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory ready cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches (refer Fig. 1.67).

Specification of $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is shown in Table 1.

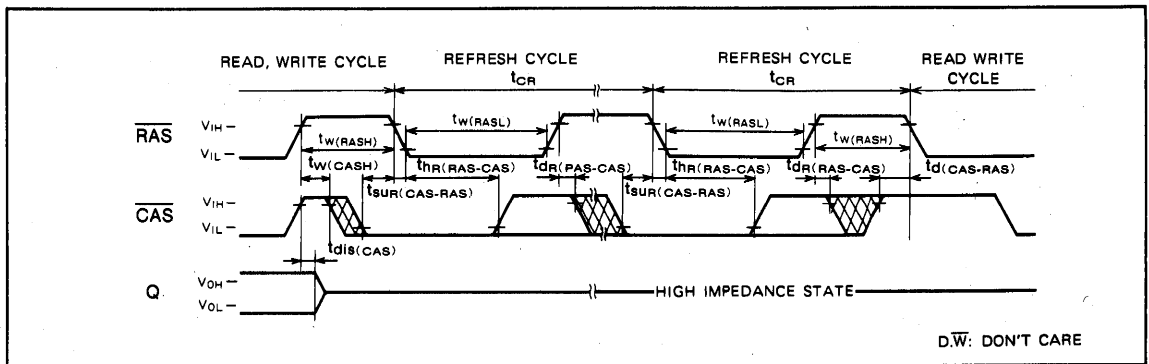


Fig. 1.66 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle

Table 1. Specification of $\overline{CAS}$ before $\overline{RAS}$ refresh cycle

Symbol	Parameter	Alternative symbol	Limits						Unit
			M5M4256-10 M5M4257-10		M5M4256-12 M5M4257-12		M5M4256-15 M5M4257-15		
			Min	Max	Min	Max	Min	Max	
$t_{SUR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	25		30		30		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	40		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

Note: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

MITSUBISHI ELECTRIC

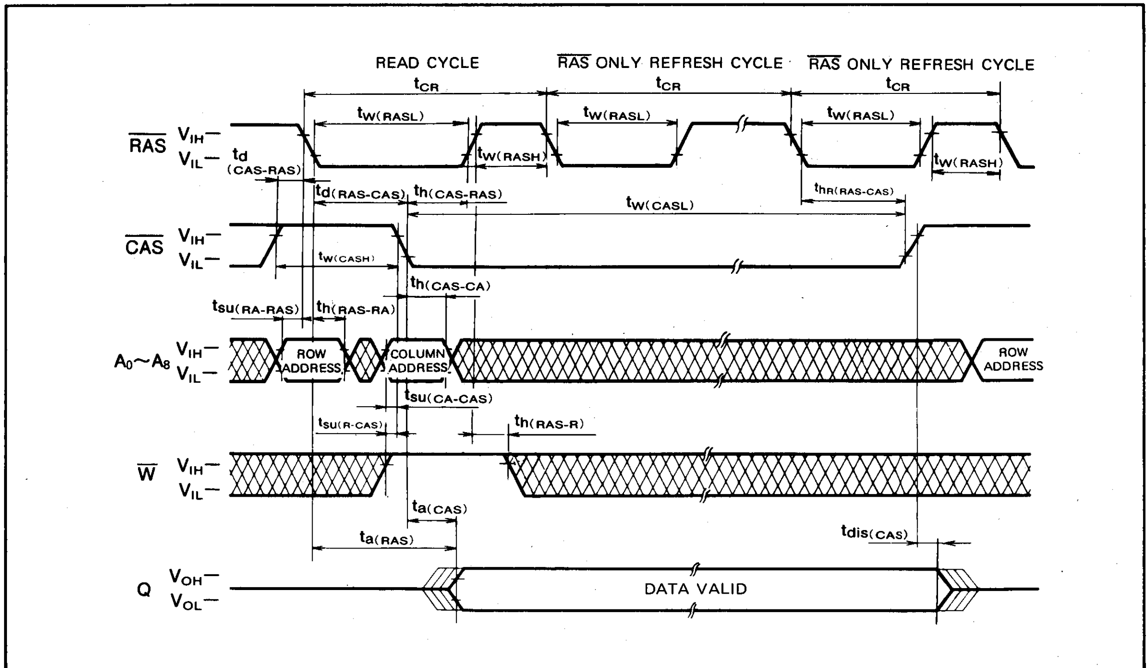


Fig. 1.67 Hidden refresh cycle

Appendix 2. CAS before RAS refresh counter test

The most useful way to test CAS before RAS refresh function is to execute the counter check program. To perform CAS before RAS refresh itself shall be avoided since devices shipped normally have long data hold time.

Counter check sequence is described below. Before the execution of counter test, it is necessary to confirm that the RAM operates properly. Also eight or more CAS before RAS cycles is necessary for proper operation of CAS before RAS refresh mode to initialize the address counter integrated on the chip (in memory system, too).

Counter Check Sequence

The operation of the internal 8-bit counter can be checked by writing in 256 bits using external address, then changing the data for the same 256 bits using internal counter address and finally reading the 256 bits using external address. An example of this checking sequence is as follows.

At the first step, "1" is written in 256 bits with normal write mode using external row address and fixing column address to the arbitrary value. The most significant bit of row address A_8 should be fixed to be "1" or "0".

At the next step, CAS before RAS clocks are applied. In this case, other external $A_0 \sim A_7$ addresses are ignored and $A_0 \sim A_7$ addresses which is generated by the internal counter are led to the address buffer. Then CAS is brought high and then Low while RAS maintains low, external $A_0 \sim A_8$ addresses are latched to be column address. The same column address as the one which is used writing "1" must be prepared and "0" is written in this selected bit. The above described clock should be repeated 256 times until all 256 bits become "0".

At the final step, 256 bits is read checked with normal mode using external address and if all checked data were "0", then this counter is proved having operated correctly. Clock sequence required is shown in Fig. 1.68.

Other varieties of test sequences may be considered.

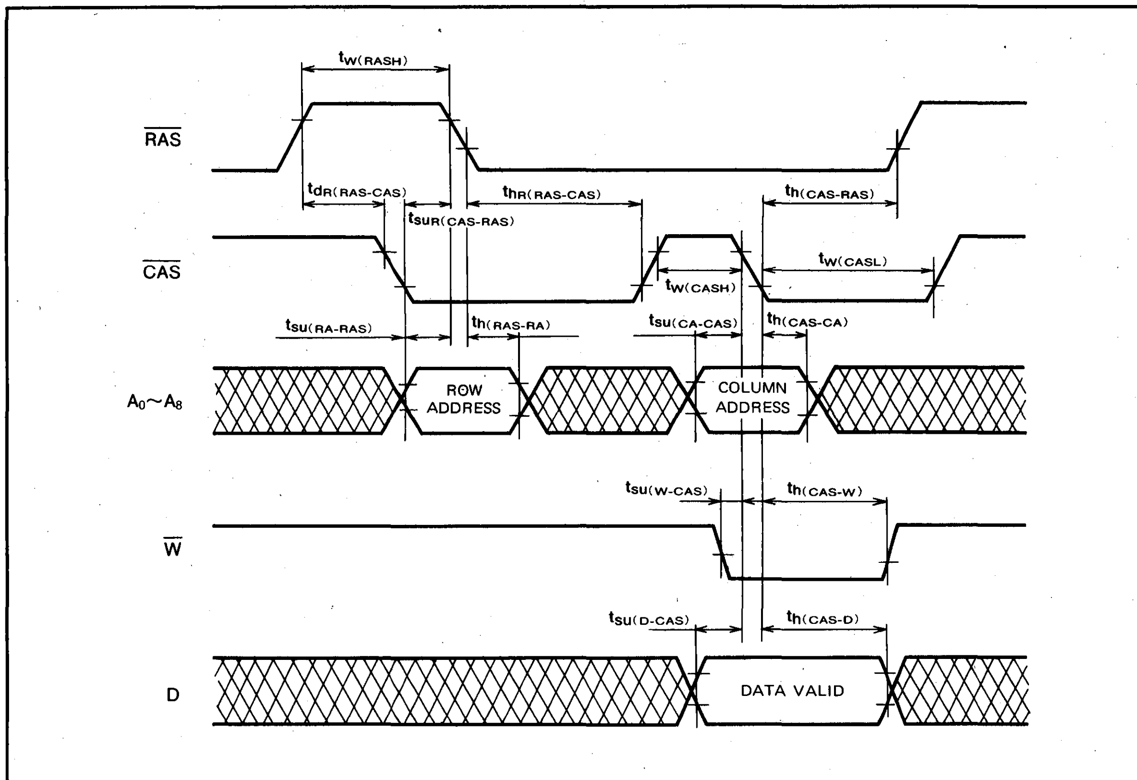


Fig. 1.68 Counter check timing (Early Write)

MITSUBISHI ELECTRIC

STATIC RAM TECHNOLOGY

Introduction

Static RAM, though inferior to dynamic RAM in density of integration, is used for a wide variety of applications. It is easy to use as it does not reguire clocks, refresh operation or related controlling peripheral ICs. In addition, static RAMs are available for equipment requiring high-speed operation or battery backup in case of power failure.

1. Classification of Static RAM

Static RAMs are classified into the following:

(1) medium-speed CMOS for easy use and battery backup
(2) high-speed CMOS for computer application

Mitsubishi Electric Corporation provides the following lineup of static RAM.

(1) medium-speed CMOS M5M5256P, M5M5165P
(2) high-speed CMOS M5M21C67P, M5M21C68P, M5M5187P, M5M5188P

2. History of Mitsubishi Memory Cells

The history of Mitsubishi memory cells is illustrated in Fig. 2.1. Mitsubishi Electric began producing 256-bit E/E type memory cells and later shifted over to high resistive load types, diminishing cell area and cutting power consumption of memory cells. A high resistive load, which is available up to 100MΩ has reduced the cell current to as low as 10nA/cell. CMOS was started at 1K bits, developed into 4K bits and then to 16K bits. The standby supply current consumed in the cells and in periferal circuits is as low as the leakage current. The specified value is 20μA, but the typical value is less than 1μA, enabling long term battery buckup operation. CMOS, however, has suffered the disadvantage of poor production costs due to its larger cell area. In the past, either economical NMOS or low power CMOS had to be selected to match the application. But, the situation has somewhat changed with the appearance of 64K bit memories, incorporating NMOS and CMOS technology. The mixture of high resistive load NMOS cells and CMOS peripherals, realized the hybrid which has the economy of NMOS and the low power of CMOS. Mitsubishi has provided the M5M5165P fabricated by this technology. The technical factors resulting in the development of this product are as follows: i) limit of large power consumption and ii) technology of fabricating high resistance of several tens of GΩ enabled low standby current which is enough for battery backup applications.

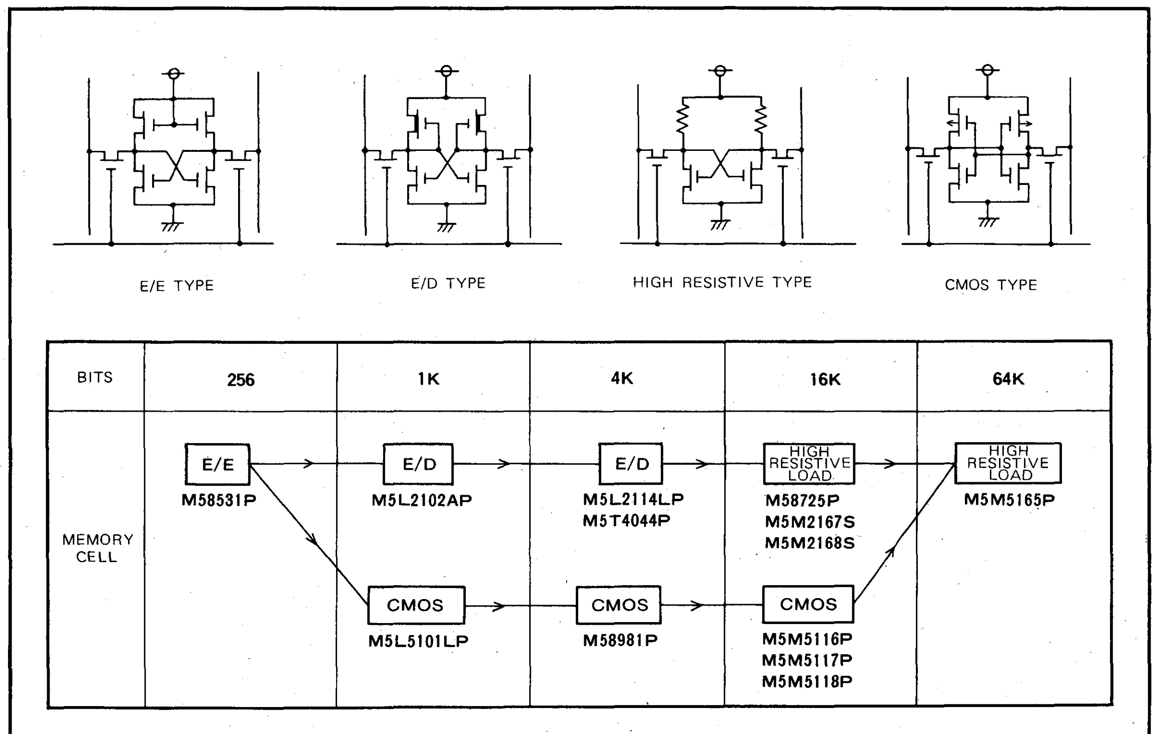


Fig. 2.1 History of Mitsubishi cells

3. Methods of Power Saving

Power consumption has become a major problem as memory capacity has increased. The solution lies in 1) the use of CMOS for peripheral circuits, 2) the division of cell array and 3) the employment of internal synchronous circuits.

Method (1) has been employed in the 64K CMOS M5M5165P.

Method (2) is aimed at decreasing the number of memory cells selected by the word decoder in order to decrease the current that flows into cells from the bit line. Fig. 2.2 shows examples of dividing the cell array. With 1K and 4K bit RAM, all the bit lines are activated, while 1/2 of the bit lines are activated with 16K and only 1/4 are designed to be activated with 64K. (d) is called the devided word line method (DWL), dividing the memory cell array into arbitrary lines, which is considered to be an important method to deal with RAMs of greater capacity in the future. The internal synchronous circuit (3), designed to cut DC current, lowers the average current greatly by the employment of a dynamic circuit. In previous asynchronouse circuits, DC current was constantly running while chips were in the active state.

A problem with the internal synchronous circuit is providing a standard clock. Unlike dynamic RAM, static RAM is not given an external clock and must generate the clock by itself. As the memory cycle of static RAM starts with an address change, the internal synchronous circuit makes use of changes in the address signal and generates an internal clock. In this circuit, the charging current of internal mode capacitance runs at the peak rate at the beginning of the cycle and no current runs after the access is finished. As the average current can be decreased to 1/10 of the conventional one (at 1 MHz), this device is most suitable for battery-operated equipment such as hand held computers.

4. Package

The more the capacity, the more the number of pins. (4K has 18 pins, 16K, 24 pins, 64K and 256K, 28 pins). On the other hand, a smaller package is required for the high density mounting. Available packages which meet these requirements are falt package, chip carrier (LCC), ZIP (zigzag inline), or shrink pack (lead spacing is 2/3 of the normal type).

Mitsubishi provides the 64K CMOS RAM M5M5165FP and 256K CMOS RAM M5M5256FP series using the flat package. Fig. 2.4 shows the outline difference between the DIP and flat package. The flat package is approximately half the size of DIP.

Fig. 2.2 Examples of memory cell array

Fig. 2.3 Circuit diagram of internal synchronous circuit

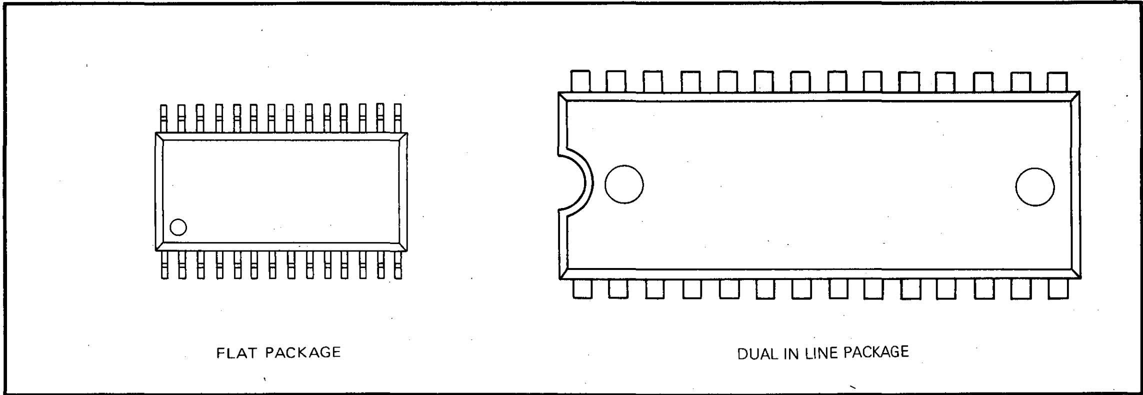


Fig. 2.4 Comparison of package outlines

OPERATION OF STATIC RAM

The timing of static RAM is simple and operation modes are very easily understood because of its asynchronous operation that does not require strobe signals to take in clock signals or external signals.

In this chapter, basic operation of static RAM and functions of various input signals are illustrated using the M5M5256P 256K static RAM as an example.

Fig. 2.5., 2.6., 2.7. are the block diagram, pin configuration and function table of M5M5256P.

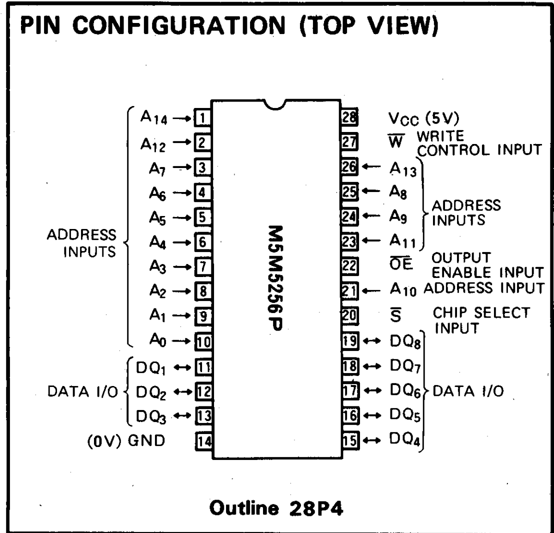


Fig. 2.6 Pin configuration of M5M5256P

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

Fig. 2.7 Function table of M5M5256P

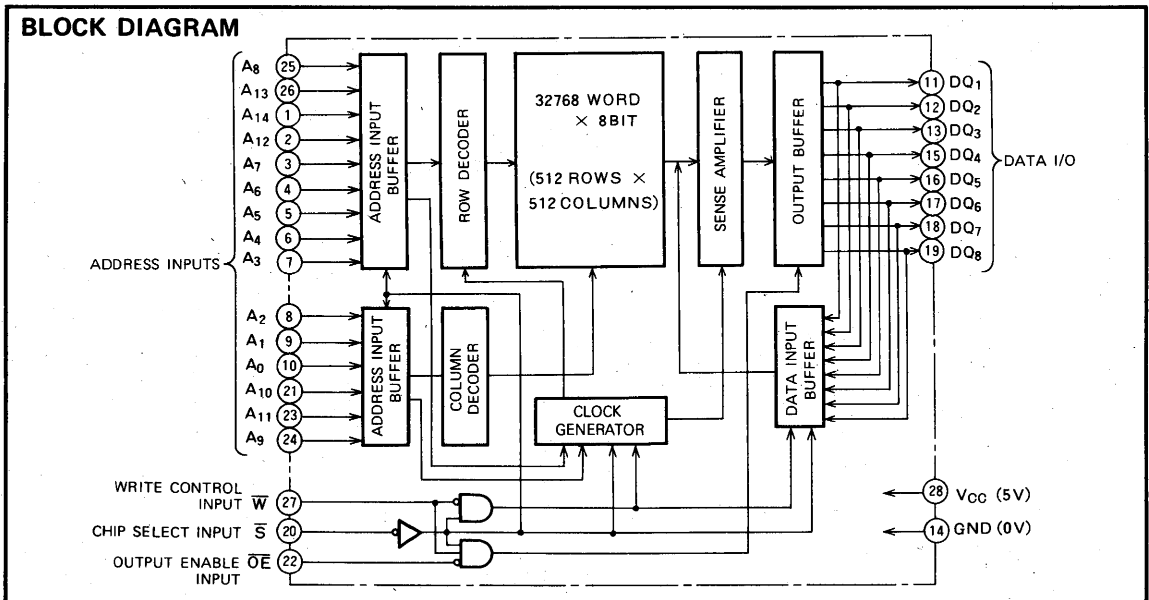


Fig. 2.5 Block diagram of M5M5256P

1. Functions of input signals

(1) Address signals ($A_0 \sim A_{15}$)

Address signals select one random bit out of the memory matrix. Read/write memory operation is made to the cell which selected by address signal.

(2) Chip select signal ($\overline{S}$)

When $\overline{S}$ = L, RAM is in the active state, enabling read/write memory operation. When $\overline{S}$ = H, RAM is in the non-selective state, disabling memory operation. In this case, the output is in the high impedance state, easily expanding memory capacity with other memorys by OR connection. In addition the supply current is in standby state and reduced to smaller than one hundredth of the normal level which contributes to the power saving of a large memory system. In most cases, like M5M5256P, the chip select signal is in negative logic (chip is selected when signal is L) but it is noted that S2 of M5M5165P is in positive logic (chip is selected when signal is H).

(3) Write control signal ($\overline{W}$)

The $\overline{W}$ signal controls operation modes of read and write. The low level $\overline{W}$ enables the write mode and the high level $\overline{W}$ enables the read mode. When the write mode is enabled the data input/output (DQ) terminal is in high impedance state.

(4) Output enable signal ($\overline{OE}$)

The $\overline{OE}$ signal controls the output stage directly at high speed. When $\overline{OE}$ = L, the DQ terminals are in the output mode, and when $\overline{OE}$ = H, they are in the high impedance state. When write operation is enabled and $\overline{OE}$ is set to H, the DQ terminals are in high impedance state and, thus, clash of RAM data output and data input, so called data bus contention, is avoided. When read operation is enabled, $\overline{OE}$ must be L so that DQ terminals may be in the output mode.

2. Read operation

Fig. 2.8 shows the timing diagram of the read cycle. When $\overline{S}$ and $\overline{OE}$ and L and $\overline{W}$ is H, the read mode is enabled and the memory cell data selected by the address signal is read at the DQ terminal. There are three kinds of read cycle timing, as showen in Fig. 2.8. They are defined as (a) address access time $t_{a(A)}$, (b) chip select access time $t_{a(S)}$, and (c) $\overline{OE}$ access time $t_{a(OE)}$.

(a) is applied when $\overline{S}$ and $\overline{OE}$ have already been set to L long before the address change. (b) is applied, contrary to (a), when $\overline{S}$ is set to L simultaneously or after the change of the address signal. In this case, $\overline{OE}$ must be L before the address change, as well as in the case of (a).

(c) is applied when the $\overline{OE}$ signal has been set to L well after the change of the address signal or the chip select signal. The $\overline{OE}$ signal controls the output buffer circuit directly at a high speed, so the high speed access time of nealy one-half of that of (a) or (b) is available. When $\overline{OE}$ is set L faster than the timing of $t_{a(A)} - t_{a(OE)}$ or $t_{A(S)} - t_{a(OE)}$, (a) or (b) is applied.

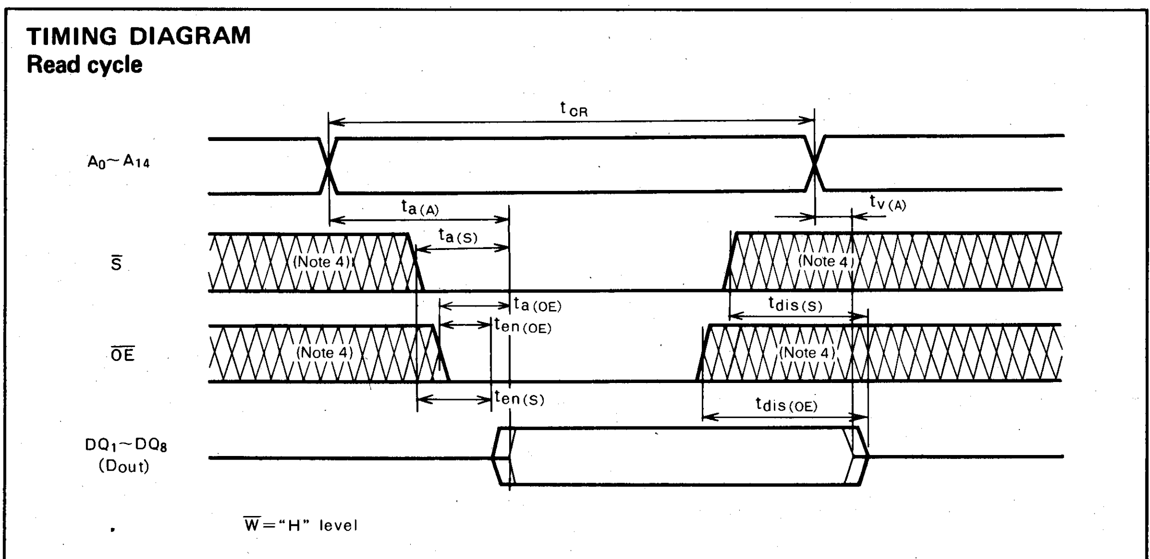


Fig. 2.8 Read cycle timing

3. Write operation

Fig. 2.9 shows the timing diagram of the write cycle. Write operation is excuted when $\overline{S}$ and W are both L. When either $\overline{S}$ or $\overline{W}$ goes to H, the data of the DQ terminal is written into the memory cell. Therefore, for the rise of $\overline{W}$ or $\overline{S}$, data setup time $t_{su(A)}$ and data hold time $t_{h(D)}$ must be maintained. Address setup time $t_{su(A)}$ and write recovery

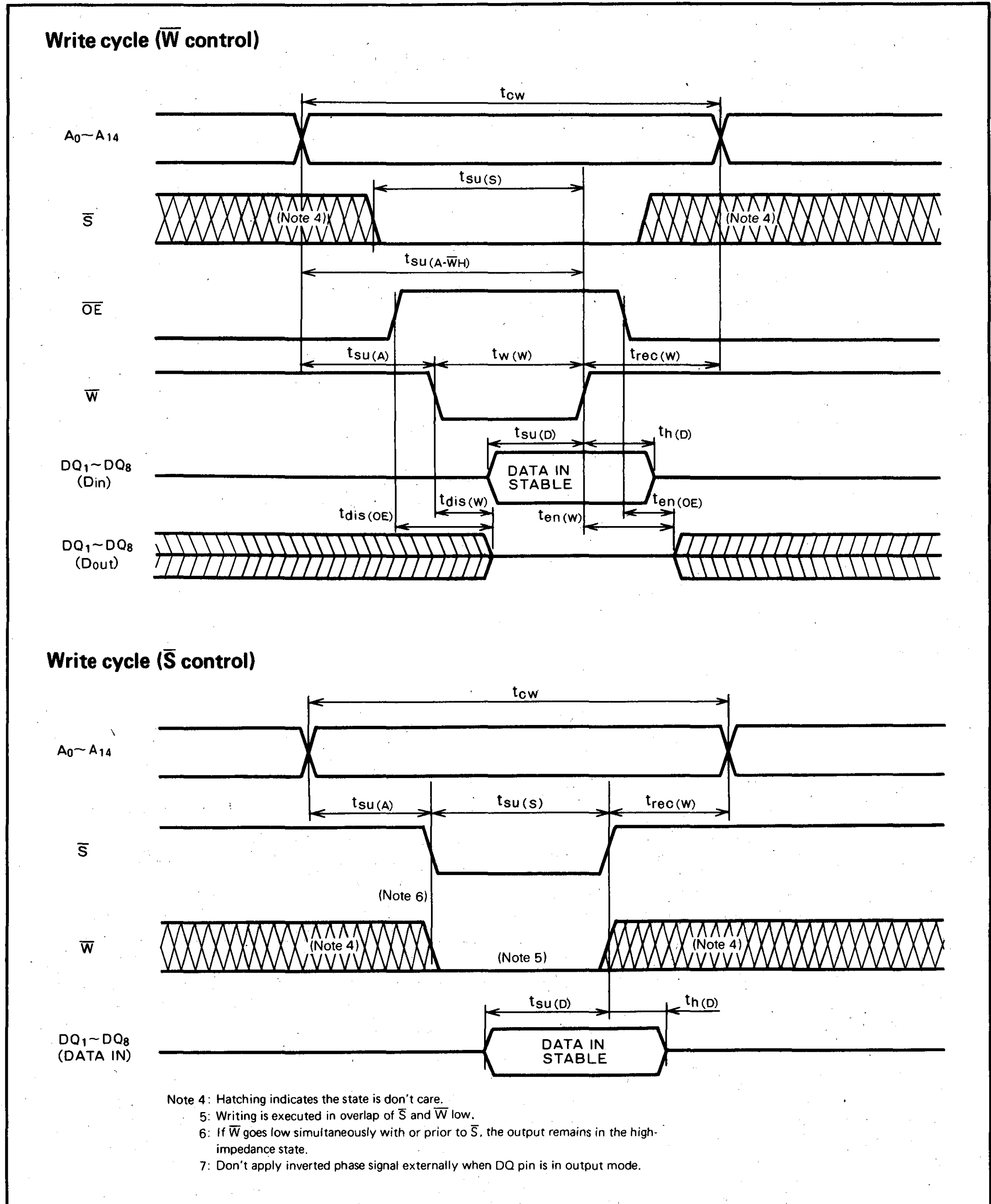


Fig. 2.9 Write cycle timing

MITSUBISHI ELECTRIC

time t_{rec}(W) are defined in order to avoid writing into a cell designated by previous or following cycles.

At the write cycle, the data bus contention problem is a matter of concern. The subject is discussed in detail in later chapters.

4. Standby Mode

When $\overline{S}$ is H, the chip becomes non-selective mode and the supply current is in the standby mode. The Supply current decreases to one tenth of the normal operation level, which contributes to power saving in systems that use many memory devices. Fig. 2.10 shows the supply current waveform for M5M5256P.

In the case of CMOS RAM, the stand by current is as low as the leak current and, the memory cell data can be held at a V_{CC} of 2V, enabling battery backup applications.

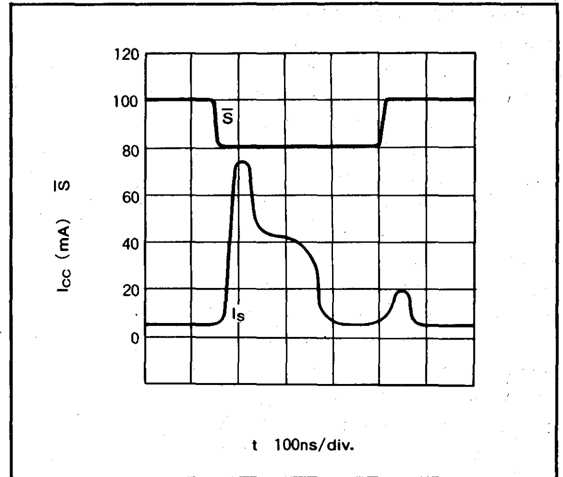


Fig. 2.10 Power saving by $\overline{S}$

APPLICATION OF STATIC RAM

To explain the application of static RAMS, M5M5256P, which has $\overline{OE}$ input.

1. Application of M5M5256P

Fig. 2.11 is an example of an M5M5256P application. The 8085A is used for the CPU. The chip select signal is gated by ALE output of 8085A. Therefore, the chip select signal turns to low, synchronously with the fall of ALE. $\overline{W}$ is connected to $\overline{WR}$ and $\overline{OE}$ is connected to the $\overline{RD}$ output of the CPU. The RAMs which have $\overline{OE}$ input can avoid the data bus contention problem by use of $\overline{RD}$ output as an $\overline{OE}$ signal.

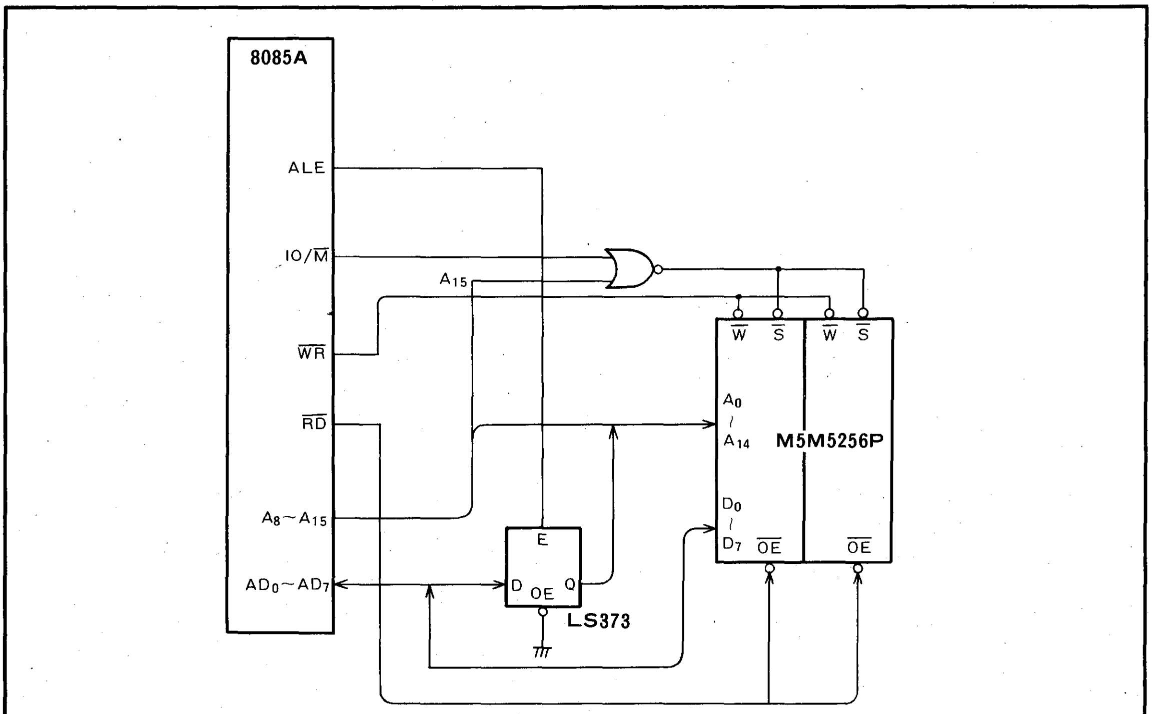


Fig. 2.11 Application circuit of M5M5256P

3. Precaution against Noise

When memories which have power saving function by chip selection shift from standby mode to operation mode, the supply current shows a change of several 10mA. In the read cycle, the discharging and charging currents for the output load capacitance run as peak currents to V_{CC} and GND. The current increases with the number of output terminals, hence, for a static RAM of x8 structure, the current is considerable. Fig. 2.12 shows the supply current waveform of the M5M5165P. Noises generated by large current changes narrow operating margins or induce faulty operation. Less consideration has been give to SRAM compared to DRAM in the past. Now, due to its considerable improvement on speed, SRAM has become susceptible to noise. Adequate consideration, therefore, must be given to the pattern design of the circuit board. To absorb noise, a 0.1μF ceramic capacitor is recommended to be placed between each device.

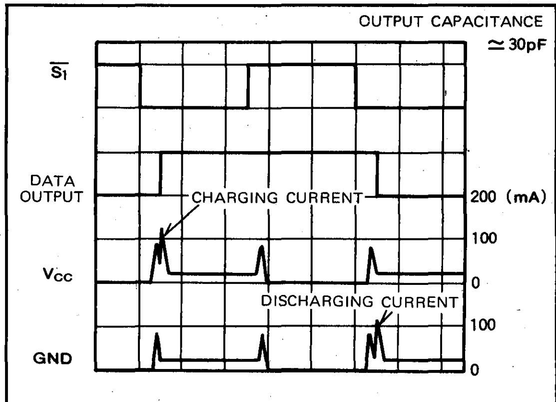


Fig. 2.12 Waveform of supply current (M5M5165P)

NON-VOLATILE MEMORY SYSTEM

We can relatively easily design a large non-volatile memory system with little additional interface logic by using CMOS RAMs. The block diagram of a basic computer system that uses CMOS RAMs is shown in Fig. 2.13, and the power supply on-off timing of the system are shown in Fig. 2.14. It is usually necessary to have advanced warning that AC power has been lost. This warning signal produced by the power-fail-detect circuit interrupts the processor, which stores the volatile data in the non-volatile area (CMOS RAMs) before the system's DC source drops. And after the RAMs have been protected, their V_{CC} power source is replaced by V_{BAT}, as shown in Fig. 2.14.

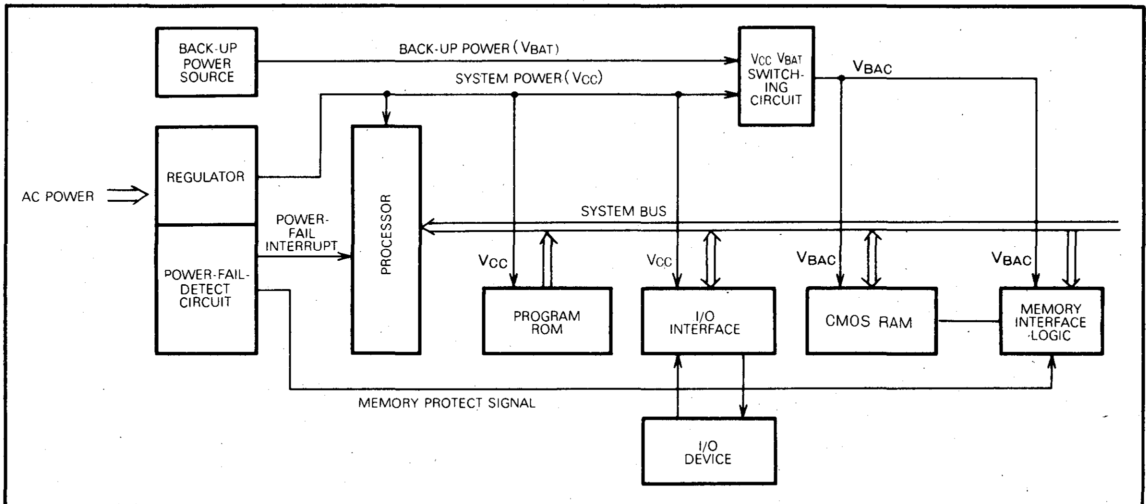


Fig. 2.13 Non-volatile memory system

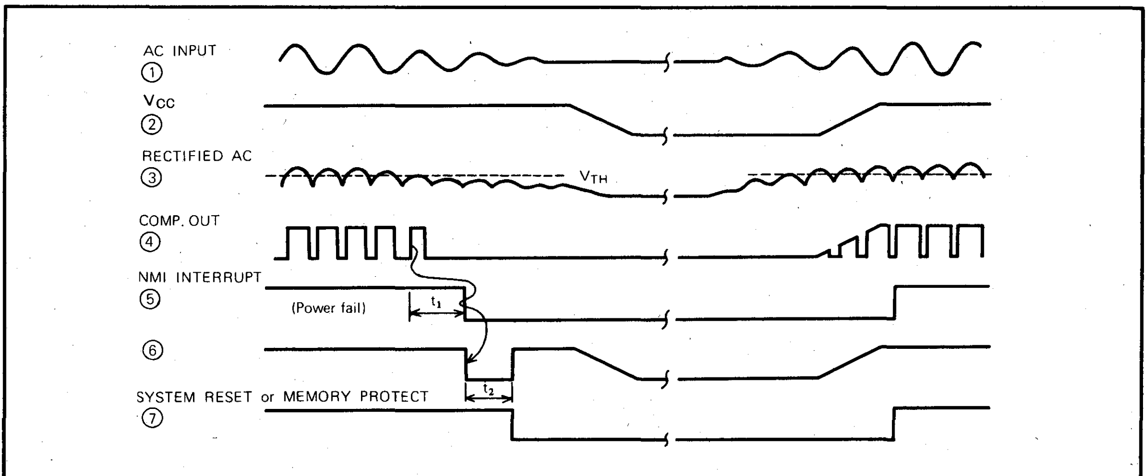


Fig. 2.14 Power on-off timing

EXAMPLE OF CMOS NON-VOLATILE MEMORY SYSTEM

Power-Failure Detection

The power-fail-detect circuit watches a separate power supply point to provide an advanced warning of power failure. As described before, this warning signal (power fail) can interrup the processor or merely protect the CMOS RAMs.

Fig. 2.17 is a simplified diagram of the power-fail-detect circuit. This shows that the power failure is detected from the secondary transformer output, which is not regulated. The Zener-diode voltage and RC time constant should be well selected to prevent AC power failure from shutting down the memory system.

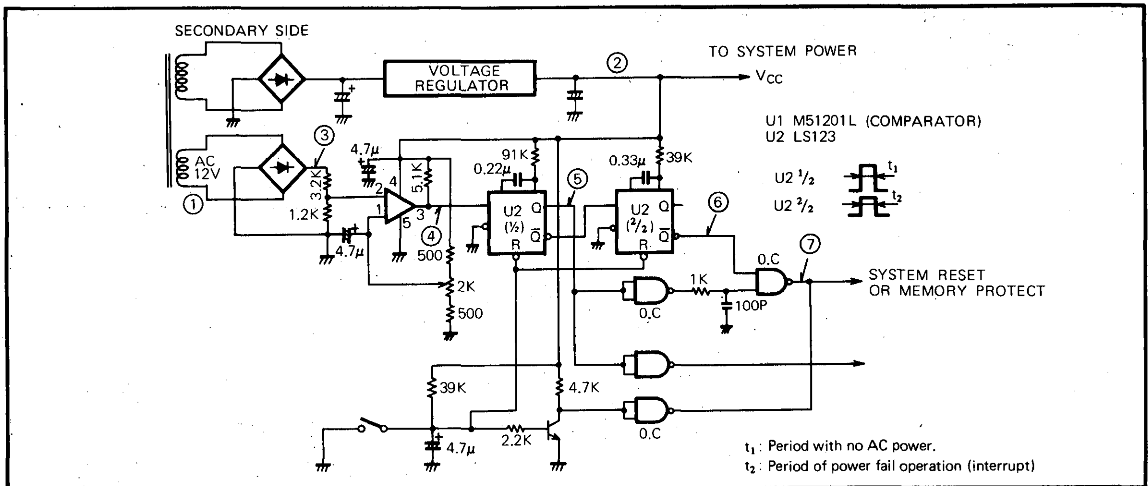


Fig. 2.15 Power-fail-detect circuit

Power-Switching Circuit

The power-switching circuit replaces the main source V_{CC} by the back-up power source V_{BAT} when V_{CC} drops, and replaces the V_{BAT} by the V_{CC} when the V_{CC} voltage rises enough to enable normal operation.

Two types of power-switching circuit are shown in Fig. 2.16 and Fig. 2.17. The diode-coupled circuit in Fig. 2.16 requires the main DC supply V_{CC} to be above the required V_{BAC} voltage by the amount of drop through the diode (about 0.6 ~ 0.7V). Fig. 2.17 shows a transistor-coupled circuit, which has better performance than the circuit in Fig. 4. In this case it is recommended to use a transistor with low collector-base saturation for Q1.

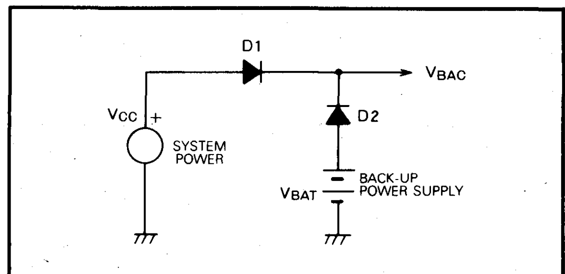


Fig. 2.16 Diode-coupled switching circuit

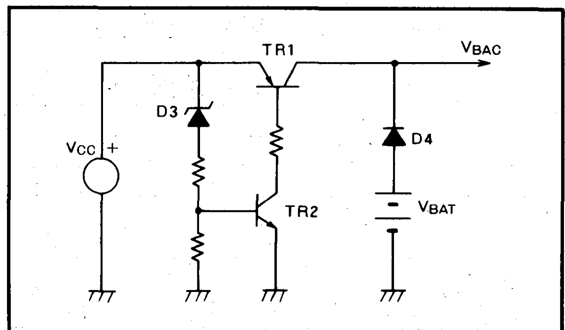


Fig. 2.17 Transistor-coupled switching circuit

4. Application Circuits

Fig. 2.18 shows an example of a non-volatile memory system using 64K bits CMOS RAM M5M5165P.

In this case, the memory protect signal is detected from the system power supply V_{CC}. However it is safer to protect the memory by taking the signal out of the non-regulated power supply, as shown in Fig. 2.15. Because protection is excuted before the fall of V_{CC} and reset after the rise of V_{CC}.

[Bit Map]

To make the best use of a test pattern or to do a failure analysis, it is necessary to know the relationship between external address and the actual cell location inside the chips. In such a case, a bit map is used to know the topology of the memory array. Figs. 2.19, 2.20 show the bit maps of all static RAMS which are in production.

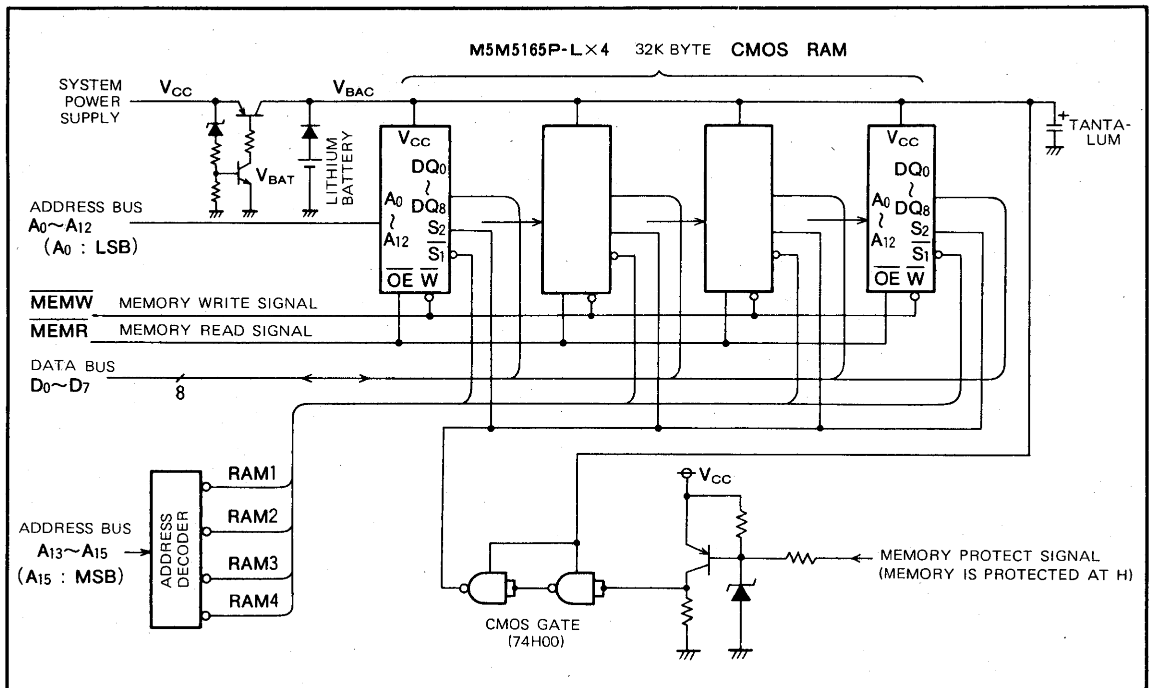


Fig. 2.18 Application of non-volatile CMOS Memory

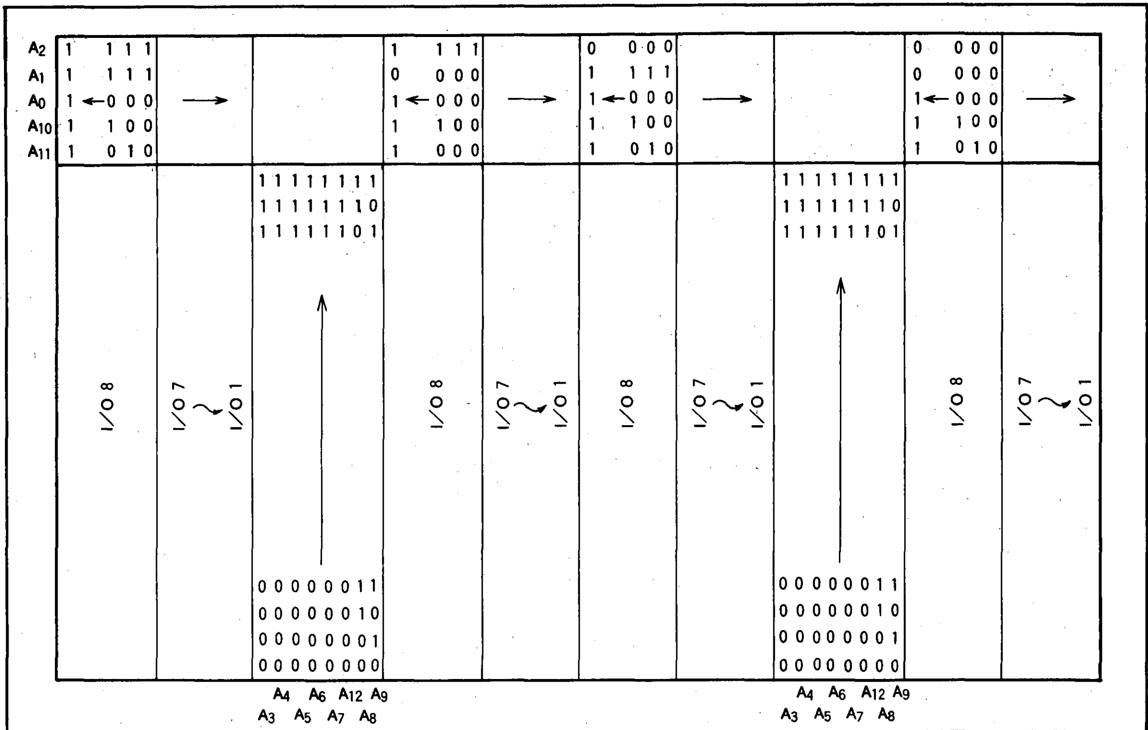


Fig.2.19 M5M5165P

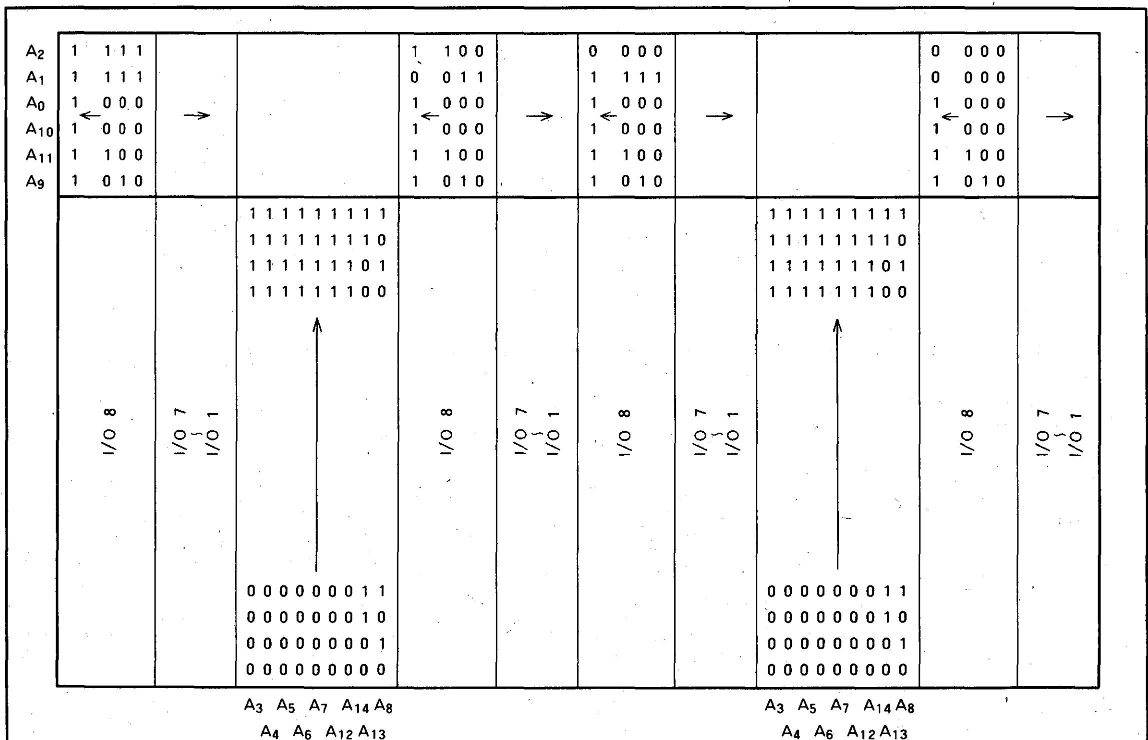


Fig.2.20 M5M5256P

CONTACT ADDRESSES FOR FURTHER INFORMATION

JAPAN

Semiconductor Marketing Division
Mitsubishi Electric Corporation
2-3, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Telex: 24532 MELCO J
Telephone: (03) 218-3473
(03) 218-3499
Facsimile: (03) 214-5570

Overseas Marketing Manager
Kita-Itami Works
4-1, Mizuhara, Itami-shi,
Hyogo-ken 664, Japan
Telex: 526408 KMELCO J
Telephone: (0727) 82-5131
Facsimile: (0727) 72-2329

HONG KONG

Ryoden Electric Engineering Co., Ltd.
22nd fl., Leighton Centre
77, Leighton Road
Causeway Bay, Hong Kong
Telex: 73411 RYODEN HX
Telephone: (5) 7907021
Facsimile: (852) 123-4344

SINGAPORE

MELCO SALES SINGAPORE PTE. LTD.
230 Upper Bukit Timah Road
#03-01/15
Hock Soon Industrial Complex
Singapore 2158
Telex: RS 20845 MELCO
Telephone: 4695255
Facsimile: 4695347

TAIWAN

MELCO-TAIWAN CO., LTD.
1st fl., Chung-Ling Bldg.,
363, Sec. 2, Fu-Hsing S Road,
Taipei, R.O.C.
Telex: 25433 CHURYO
"MELCO-TAIWAN"
Telephone: (02) 735-3030
Facsimile: (02) 735-6771

U.S.A.

NORTHWEST

Mitsubishi Electronics America, Inc.
1050 East Arques Avenue
Sunnyvale, CA 94086, U.S.A.
Telex: 172296 MELA SUVL
Twx: 910-339-9549
Telephone: (408) 730-5900
Facsimile: (408) 730-4972

SOUTHWEST

Mitsubishi Electronics America, Inc.
991 Knox Street
Torrance, CA 90502, U.S.A.
Telex: 664787 MELA TRNC
Telephone: (213) 515-3993
Facsimile: (213) 324-6578

SOUTH CENTRAL

Mitsubishi Electronics America, Inc.
2105 Luna Road, Suite 320
Carrollton, TX 75006, U.S.A.
Telephone: (214) 484-1919
Facsimile: (214) 243-0207

NORTHERN

Mitsubishi Electronics America, Inc.
15612 Highway 7 #243
Minnetonka, MN 55345, U.S.A.
Telex: 291115 MELA MTKA
Telephone: (612) 938-7779
Facsimile: (612) 938-5125

NORTH CENTRAL

Mitsubishi Electronics America, Inc.
800 N. Bierman Circle
Mt. Prospect, IL 60056, U.S.A.
Telex: 270636 MESA CHIMPCT
Telephone: (312) 298-9223
Facsimile: (312) 298-0567

NORTHEAST

Mitsubishi Electronics America, Inc.
200 Unicorn Park Drive
Woburn, MA 01801, U.S.A.
Telex: 951796 MELA WOBN
Twx: 710-348-1229
Telephone: (617) 938-1220
Facsimile: (617) 938-1075

MID ATLANTIC

Mitsubishi Electronics America, Inc.
Two University Plaza
Hackensack, NJ 07601, U.S.A.
Telex: 132205 MELA HAKI
Twx: 710-991-0080
Telephone: (201) 488-1001
Facsimile: (201) 488-0059

SOUTH ATLANTIC

Mitsubishi Electronics America, Inc.
6575 The Corners Parkway
Suite 100
Norcross, GA 30092, U.S.A.
Twx: 910-380-9555
Telephone: (404) 662-0813
Facsimile: (404) 662-5208

SOUTHEAST

Mitsubishi Electronics America, Inc.
Town Executive Center
6100 Glades Road #210
Boca Raton, FL 33433, U.S.A.
Twx: 510-953-7608
Telephone: (305) 487-7747
Facsimile: (305) 487-2046

WEST GERMANY

Mitsubishi Electric Europe GmbH
Headquarters:
Gothear Str. 6
4030 Ratingen 1, West Germany
Telex: 8585070 MED D
Telephone: (02102) 4860
Facsimile: (02102) 486-115

Munich Office:
Arabellastraße 31
8000 München 81, West Germany
Telex: 5214820
Telephone: (089) 919006-09
Facsimile: (089) 9101399

FRANCE

Mitsubishi Electric Europe GmbH
65 Avenue de Colmar Tour Albert 1er
F-92507 Rueil Malmaison Cedex,
France
Telex: 202267 (MELCAM F)
Telephone: (01) 7329234
Facsimile: (01) 7080405

ITALY

Mitsubishi Electric Europe GmbH
Centro Direzionale Colleoni
Palazzo Cassiopea 1
20041 Agrate Brianza I-Milano
Telephone: (039) 636011
Facsimile: (039) 6360120

SWEDEN

Mitsubishi Electric Europe GmbH
Lastbilsvägen 6B
5-19149 Sollentuna, Sweden
Telex: 10877 (meab S)
Telephone: (08) 960468
Facsimile: (08) 966877

U.K.

Mitsubishi Electric (U.K.) Ltd.
Hertford Place, Denham Way,
Maple Cross, Rickmanworth, Herts,
WD3 2BJ, England, U.K.
Telex: 916756 MEUKG
Telephone: (923) 770000
Facsimile: (923) 775282

AUSTRALIA

Mitsubishi Electric Australia Pty. Ltd.
73-75, Epping Road, North Ryde,
P.O. Box 1567, Macquarie Centre,
N.S.W., 2113, Australia
Telex: MESYD AA 26614
Telephone: (02) (888) 5777
Facsimile: (02) (887) 3635

MITSUBISHI SEMICONDUCTORS
IC MEMORIES DATA BOOK

April, First Edition 1987

Editioned by
Committee of editing of Mitsubishi Semiconductor Data Book

Published by
Mitsubishi Electric Corp., Semiconductor Marketing Division

This book, or parts thereof, may not be reproduced in any form without permission of Mitsubishi Electric Corporation.