MITSUBISHI SEMICONDUCTORS 1990

MICROPROCESSORS AND PERIPHERAL CIRCUITS

DATA BOOK

MITSUBISHI ELECTRIC

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8 GMICRO M32 Family PERIPHERAL CIRCUITS

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ pwr dissipation (mW)	Max access time (ns)	Min cycle time (ns)	Max frequency (MHz)	Package	Page

■CMOS PERIPHERAL CIRCUITS

Type	Circuit function and organization	Structure	Supply voltage (V)	Typ pwr dissipation (mW)	Max access time (ns)	Min cycle time (ns)	Max frequency (MHz)	Package	Page
M5M81C55P-2	CMOS 2048-bit Static RAM with I/O Ports and Timer ($\overline{CE}$="L" active)	C,Si	5±10%	35	120	200	5	40P4	4—3
M5M81C55FP-2		C,Si	5±10%	35	120	200	5	40P2R	4—3
M5M81C55J-2		C,Si	5±10%	35	120	200	5	44P0	4—3
M5M81C56P-2	CMOS 2048-bit Static RAM with I/O Ports and Timer (CE="H" active)	C,Si	5±10%	35	120	200	5	40P4	4—13
M5M81C56FP-2		C,Si	5±10%	35	120	200	5	40P2R	4—13
M5M81C56J-2		C,Si	5±10%	35	120	200	5	44P0	4—13
M5M82C37AP-5		C,Si	5±10%	22.5	140	200	5	40P4	4—23
M5M82C37AFP-5 M5M82C37AJ-5	CMOS Programmable DMA Controller	C,Si	5±10%	22.5	140	200	5	40P2R 44P0	4—23
M5M82C51AP		C,Si	5±10%	6	170	320	3	28P4	4—43
M5M82C51AFP	CMOS Programmable Communication Interface	C,Si	5±10%	6	170	320	3	28P2W	4—43
M5M82C51AJ		C,Si	5±10%	6	170	320	3	28P0	
M5M82C54P		C,Si	5±10%	35	120	125	8	24P4	4—61
M5M82C54FP M5M82C54J	CMOS Programmable Interval Timer	C,Si	5±10%	35	120	125	8	24P2W 28P0	4—61
M5M82C55AP-2		C,Si	5±10%	—	120	320	—	40P4	4—72
M5M82C55AFP-2 M5M82C55AJ-2	CMOS Programmable Peripheral Interface	C,Si	5±10%	—	120	320	—	40P2R 44P0	4—72
M5M82C59AP-2		C,Si	5±10%	—	120	310	—	28P4	4—88
M5M82C59AFP-2 M5M82C59AJ-2	CMOS Programmable Interrupt Controller	C,Si	5±10%	—	120	310	—	28P2W 28P0	4—88
M5M82C255ASP	CMOS Programmable Peripheral Interface	C,Si	5±10%	—	120	320	—	64P4B	4—105

■32-BIT MICROPROCESSORS G_{MICRO}™ · M32 FAMILY

Type No	Circuit function	Structure	Supply voltage (V)	Electrical characteristics: Typ. power dissipation (mW)	Max frequency (MHz)	Package	Page
M33210GS/FP-20 ★★	32-Bit Microprocessor(M32/100)	C,Si	5±5%	—	20	135S8/160P6	7—3
M33220GS-20 ★★	32-Bit Microprocessor(M32/200)	C,Si	5±5%	—	20	135S8X-A	7—5
M33230GS-20 ★★	32-Bit Microprocessor(M32/300)	C,Si	5±5%	—	20	179S8X-B	7—7
M33241GS ★★	DMA Controller(M32/DMAC)	C,Si	5±5%	1200	20	179S8X-A	8—3
M33242SP/J ★★	Interrupt Request Controller(M32/IRC)	C,Si	5±5%	200	20	64P4X-A/ 68P0X-A	8—5
M33243GS-25,-30 ★★	TAG Memory(M32/TAGM)	C,Si	5±10%	1250	—	64S8X-A	8—7
M33244T-16,-20 ★★	Clock Pulse Generator for M32/200(CPG/200)	—	5±5%	—	16/20	14T4X-A	8—9
M33245GS ★★	Cache Controller/Memory(M32/CCM)	C,Si	5±5%	—	—	135S8	8—10
M33281GS-20 ★★	Floating Point Processing Unit(M32/FPU)	C,Si	5±5%	—	20	135S8X-A	8—12

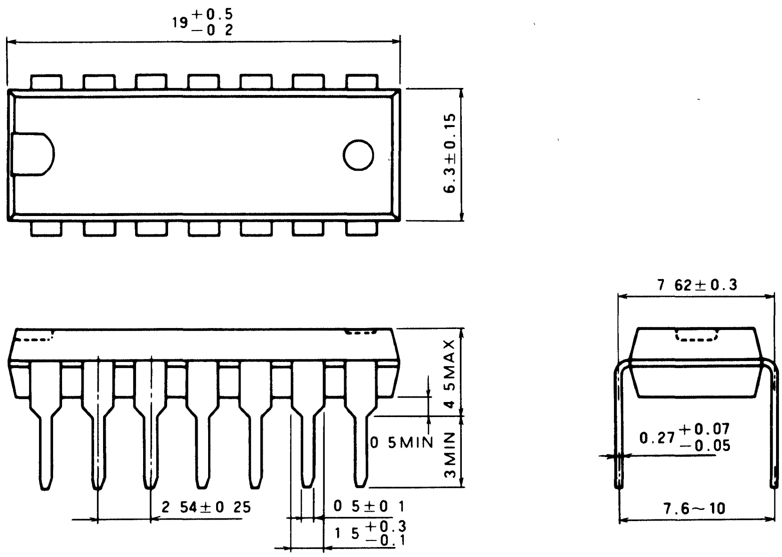
The G$_{MICRO}$™ trade mark indicates a G-MICRO group thoron type micro processor

★★ : Under development
C = CMOS. Si = Silicon gate

PACKAGE OUTLINES

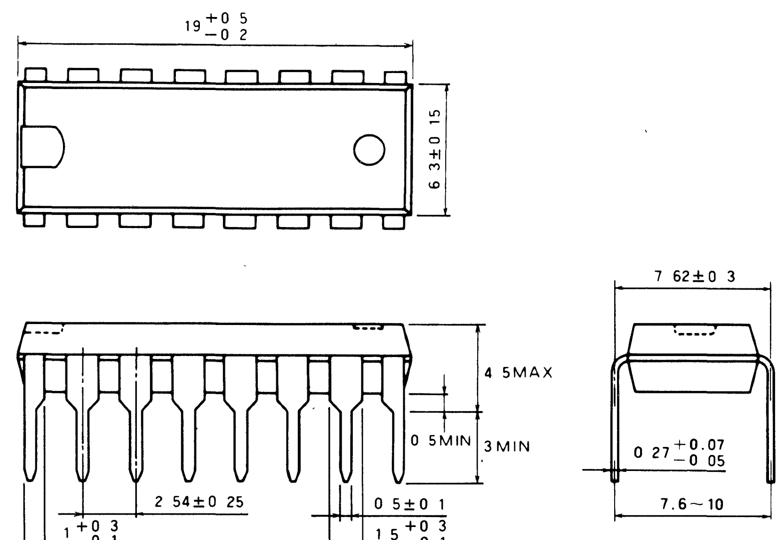
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



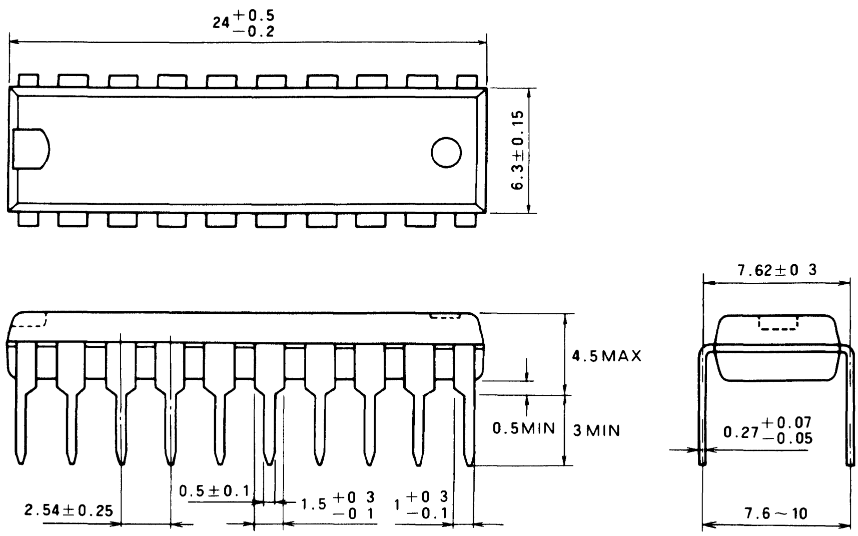
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



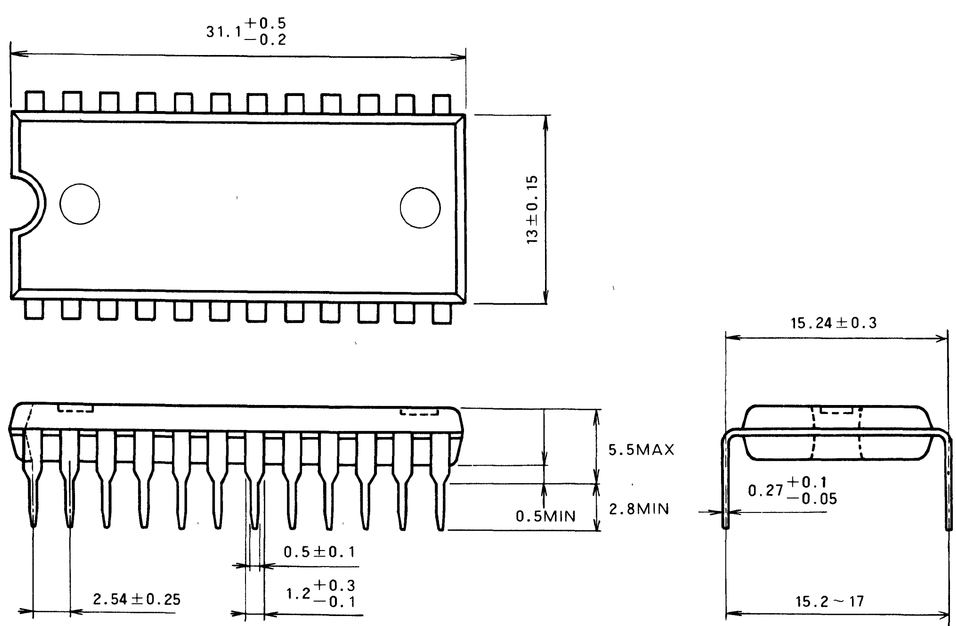
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



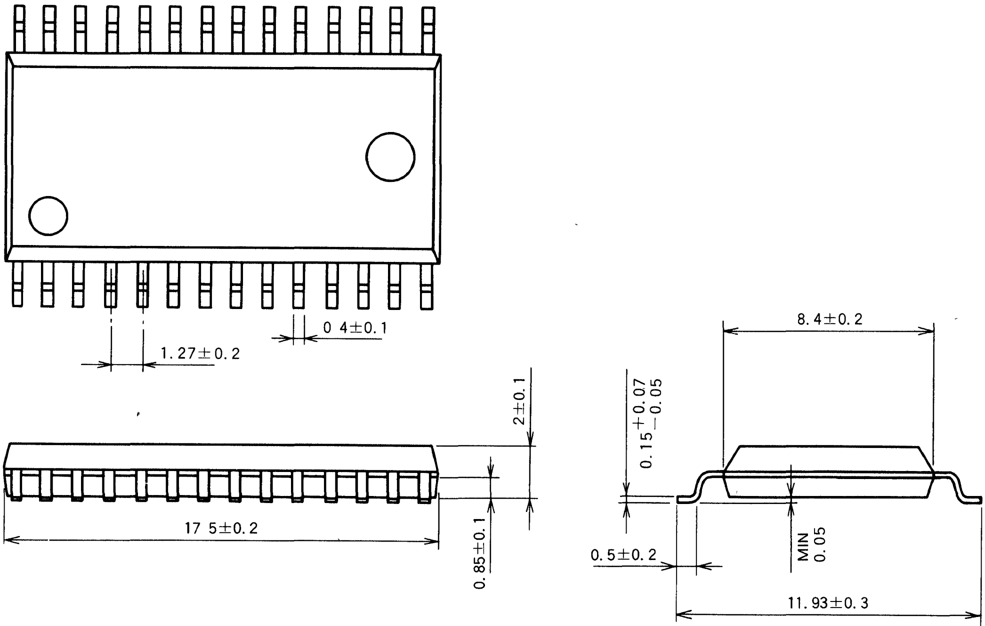
TYPE 24P4 24-PIN MOLDED PLASTIC DIP

Dimension in mm



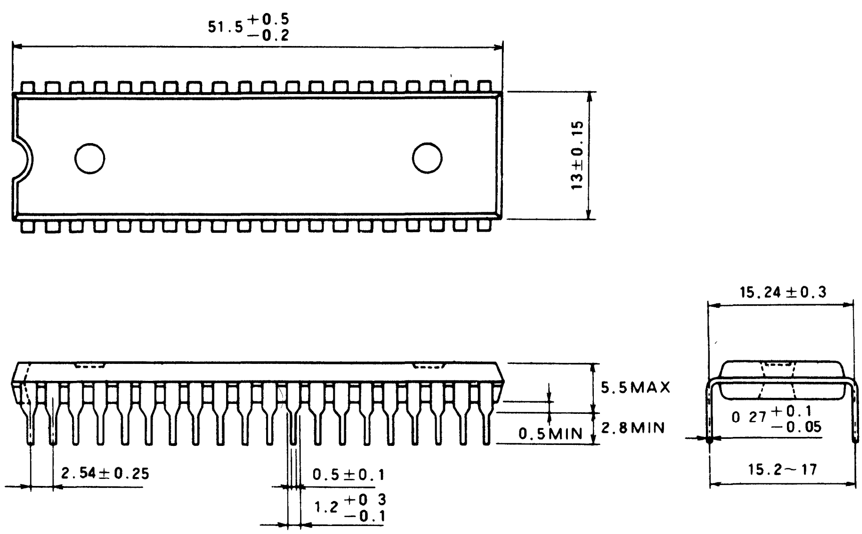
TYPE 28P2W 28-PIN MOLDED PLASTIC FLAT

Dimension in mm



TYPE 40P4 40-PIN MOLDED PLASTIC DIP

Dimension in mm



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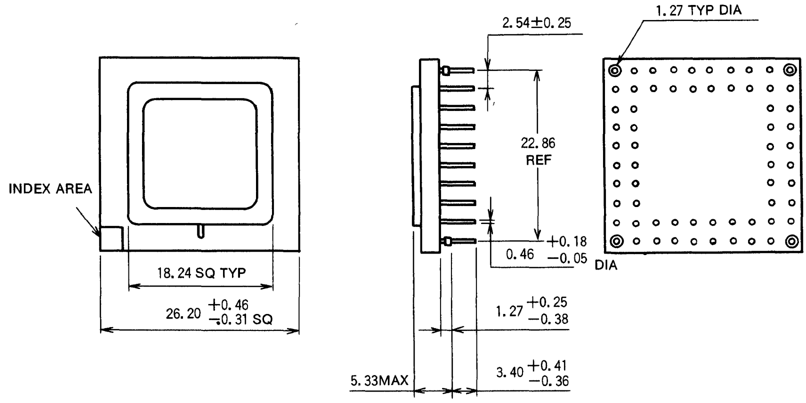
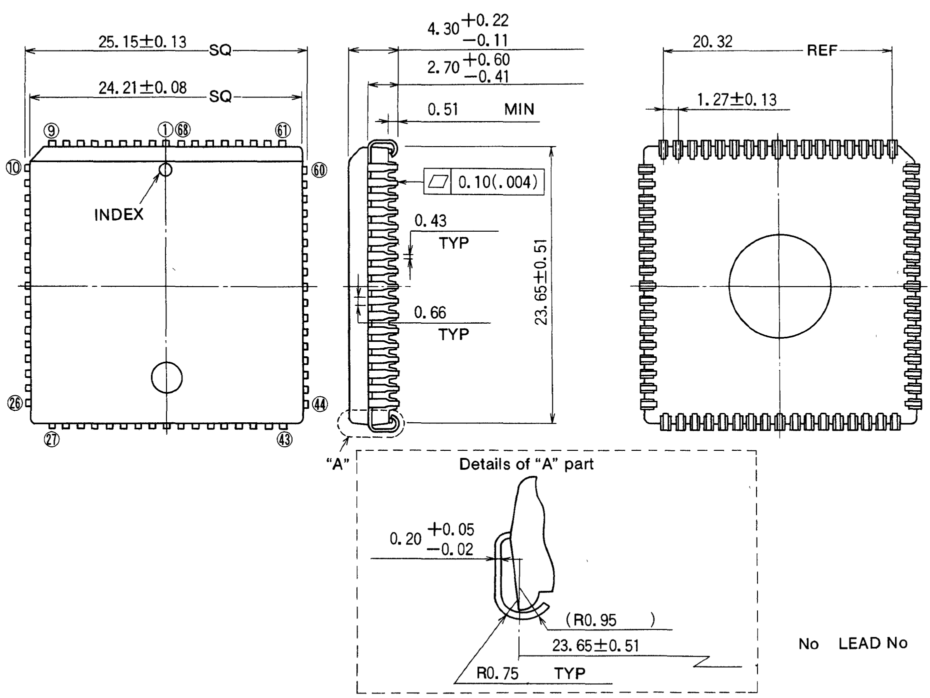
TYPE 64S8X-A 64-PIN METAL-SEALED CERAMIC PGA (GMICRO™)

Dimension in mm



TYPE 68P0X-A 68-PIN MOLDED PLASTIC LEADED CHIP CARRIER (GMICRO™)

Dimension in mm

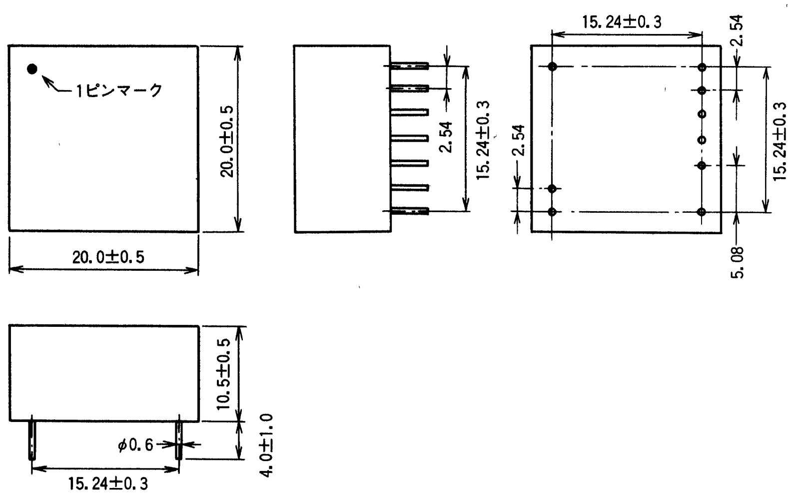


No LEAD No

MITSUBISHI ELECTRIC

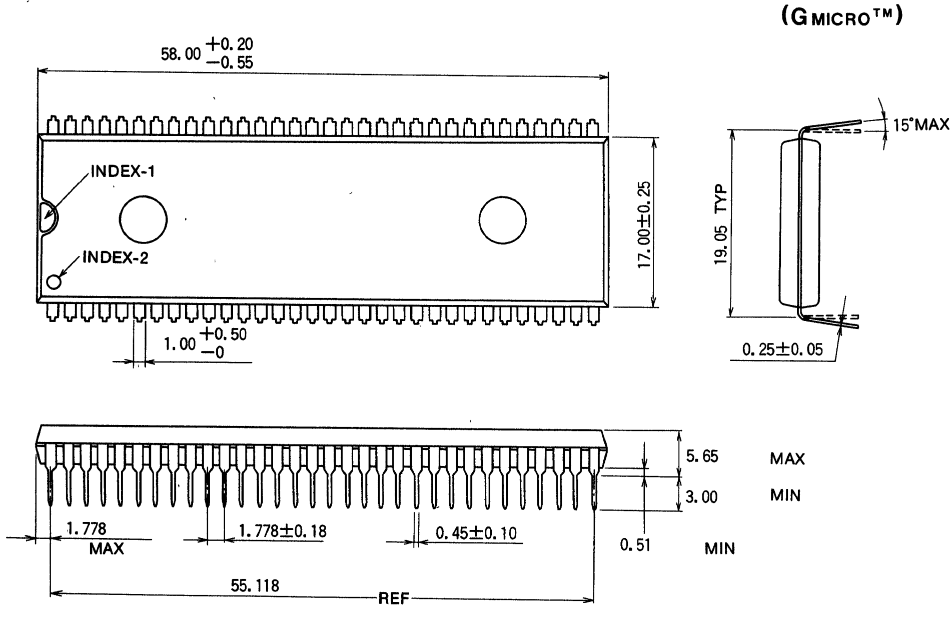
TYPE 14T4X-A 14-PIN HERMETIC-SEALED PACKAGE (GMICRO™)

Dimension in mm



TYPE 64P4X-A 64-PIN MOLDED PLASTIC DIP (LEAD PITCH 1.778mm) (GMICRO™)

Dimension in mm



LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by a general symbol of the form:

$t_{A(BC-DC)F}$ .... (1)

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

Note 1 Subscripts A to F may each consists of one or more letters
2 Subscripts D and E are not used for transition times
3 The "–" in the symbol (1) above is used to indicate "to", hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times Where no misunderstanding can occur the hyphen may be omitted

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or t_{AF} – no brackets are used in this case

or t_{A}

or t_{BC-DE} – often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter)

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

SYMBOLOGY

New symbol	Former symbol	Parameter—definition
t_d		Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$		Delay time between clock pulses—e g , symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_{d(CAS-RAS)}$		Delay time, column address strobe to row address strobe
$t_{d(CAS-W)}$	$t_{d(CAS\ WR)}$	Delay time, column address strobe to write
$t_{d(RAS-CAS)}$		Delay time, row address strobe to column address strobe
$t_{d(RAS-W)}$	$t_{d(RAS-WR)}$	Delay time, row address strobe to write
$t_{dis(R-Q)}$	$t_{dis(R-DA)}$	Output disable time after read
$t_{dis(S)}$	$t_{PXZ(CS)}$	Output disable time after chip select
$t_{dis(W)}$	$t_{PXZ(WR)}$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven and loaded by specified networks
t_{DLH}		Low-level to high-level delay time
$t_{en(A-Q)}$	$t_{PZV(A-DQ)}$	Output enable time after address
$t_{en(R-Q)}$	$t_{PZV(R-DQ)}$	Output enable time after read
$t_{en(S-Q)}$	$t_{PZX(CS-DQ)}$	Output enable time after chip select
t_f		Fall time
t_h		Hold time—the interval time during which a signal at a specified input terminal after an active transition occurs at another specified input terminal
$t_{h(A)}$	$t_{h(AD)}$	Address hold time
$t_{h(A-E)}$	$t_{h(AD-CE)}$	Chip enable hold time after address
$t_{h(A-PR)}$	$t_{h(AD-PRO)}$	Program hold time after address
$t_{h(CAS-CA)}$		Column address hold time after column address strobe
$t_{h(CAS-D)}$	$t_{h(CAS-DA)}$	Data-in hold time after column address strobe
$t_{h(CAS-Q)}$	$t_{h(CAS-OUT)}$	Data-out hold time after column address strobe
$t_{h(CAS-RAS)}$		Row address strobe hold time after column address strobe
$t_{h(CAS-W)}$	$t_{h(CAS-WR)}$	Write hold time after column address strobe
$t_{h(D)}$	$t_{h(DA)}$	Data-in hold time
$t_{h(D-PR)}$	$t_{h(DA-PRO)}$	Program hold time after data-in
$t_{h(E)}$	$t_{h(CE)}$	Chip enable hold time
$t_{h(E-D)}$	$t_{h(CE-DA)}$	Data-in hold time after chip enable
$t_{h(E-G)}$	$t_{h(CE-OE)}$	Output enable hold time after chip enable
$t_{h(R)}$	$t_{h(RD)}$	Read hold time
$t_{h(RAS-CA)}$		Column address hold time after row address strobe
$t_{h(RAS-CAS)}$		Column address strobe hold time after row address strobe
$t_{h(RAS-D)}$	$t_{h(RAS-DA)}$	Data-in hold time after row address strobe
$t_{h(RAS-W)}$	$t_{h(RAS-WR)}$	Write hold time after row address strobe
$t_{h(S)}$	$t_{h(CS)}$	Chip select hold time
$t_{h(W)}$	$t_{h(WR)}$	Write hold time
$t_{h(W-CAS)}$	$t_{h(WR-CAS)}$	Column address strobe hold time after write
$t_{h(W-D)}$	$t_{h(WR-DA)}$	Data-in hold time after write
$t_{h(W-RAS)}$	$t_{h(WR-RAS)}$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_{PLH}		Low-level to high-level propagation time
t_r		Rise time
$t_{rec(W)}$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec(PD)}$	$t_{R(PD)}$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a specifed input terminal and a consecutive active tarnsition at another specified input terminal
$t_{su(A)}$	$t_{su(AD)}$	Address setup time
$t_{su(A-E)}$	$t_{su(AD-CE)}$	Chip enable setup time before address
$t_{su(A-W)}$	$t_{su(AD-WR)}$	Write setup time before address
$t_{su(CA-RAS)}$		Row address strobe setup time before column address

QUALITY ASSURANCE AND RELIABILITY TESTING

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Microprocessor and Peripheral Circuits ICs.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Figure 1.

2.1 Quality Assurance in Designing

The following steps are applied in the designing stage for a new product.

(1). Setting of perfomance, quality and reliability target for new product.
(2) Discussion of performance and quality for circuit design, device structure, process, material and package.
(3) Verification of design by CAD system to meet standardized design rule.
(4) Functional evaluation for bread-board device to confirm electrical performance.
(5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure machanism.
(6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
(7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc.

2.2 Quality Assurance in Manufacturing

Quality assurance in manufacturing is performed as follows

(1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipment, automatic testing equipment, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
(4) In-process inspections in wafer-fabrication, assembly and testing.
(5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
(6) Quality assurance test
-Electrical characteristics and visual inspection, lot by lot sampling
-Environment and endurance test, periodical sampling.
(7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages : new product development, pre-production, and mass-production.

At the development of a new product the reliability test plan is fixed corresponding to the quality and reliability target of each product, respectively. The test plan includes in-house qualification test, and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage, the specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of the mass production product according to the quality assurance test program.

Table 1 TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230℃, 5sec Rosin flux
2	Soldering heat	260℃, 10sec
	Thermal shock	−55℃, 125℃, 15cycles
	Temperature cycling	−65℃, 150℃, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
4	Shock	1500G, 0.5msec
	Vibration	20G, 100~2000Hz X, Y, Z direction 4min /cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min
5	Dynamic operation life	T_a=Toprmax, Vccmax 1000hours
6	High temperature storage life	T_a=150℃, 1000hours
7	High temperature and high humidity	85℃, 85%, 1000hours
	Pressure cooker	121℃, 100%, 100hours

Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipment to analyze the returned product. A failure analysis report is generated to the customer upon completion of the analysis. The failure analysis result enforces taking corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Figure 2 shows the procedure of returned product control from customer.

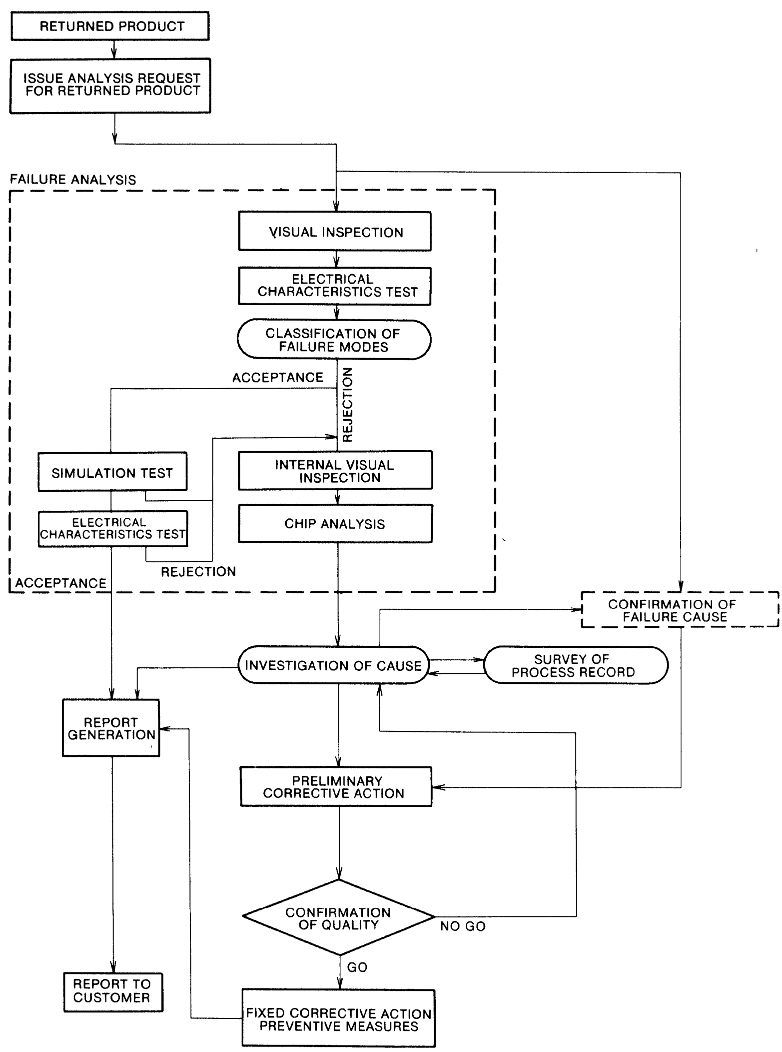


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

Table 4 MECHANICAL TEST RESULTS

Package Pin Count	Test / Test Condition / Type Number	Solderability		Lead Fatigue		Shock Vibration Constant Acceleration	
	Test Condition	See Table 1		See Table 1		See Table 1	
	Type Number	Number of Samples	Number of Failures	Number of Samples	Number of Failures	Number of Samples	Number of Failures
24P4	M5L8253P-5	60	0	30	0	22	0
28P4	M5L8251AP-5	30	0	30	0	22	0
	M5L8259AP	30	0	15	0	22	0
40P4	M5L8085AP	30	0	30	0	22	0
	M5L8255AP-5	30	0	30	0	22	0
28P2W	M5M8259AFP	15	0	15	0	22	0
40P2W	M5M82C55AFP-5	15	0	15	0	22	0

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures casued by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Figure 3, Figure 4 and Figure 5 are examples of a failure which occurs by high temperature storage test of 225℃, 1000hours.

Au-Al intermetallic formation, so-called "Purple plague", by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated at approximately 1.0eV and no failure has been observed so far in practical uses.

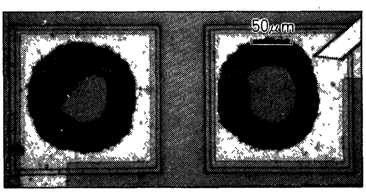


Fig.3
Micrograph of lifted Au ball trace on Al bonding pad

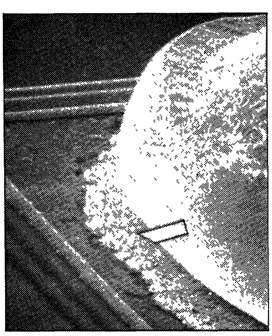


Fig.4
Au-Al plague formation on bonding pad

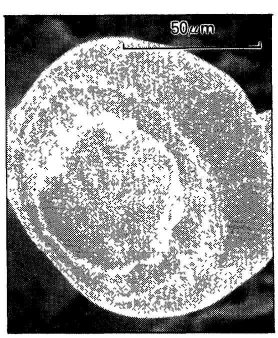


Fig.5
Lifted Au wire ball base

(2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Figure 6, Figure 7 and Figure 8 are examples of corroded failure of aluminum metallization of plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121℃, 100%RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Figure 8.

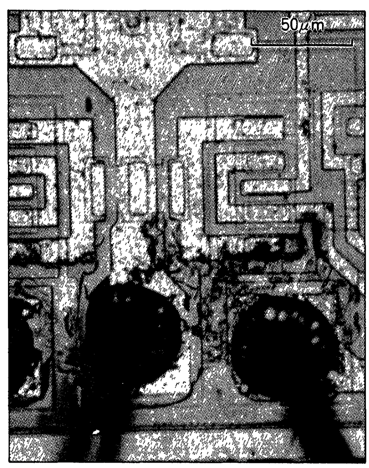


Fig.6
Micrograph of corroded Aluminum metallization

(3) Destructive Failure by Electrical Overstress

Surge voltage marginal tests have been performed to reproduce the electrical overstress failure in field uses. Figure 9 and Figure 10 are examples of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X ray micro analysis.

MITSUBISHI ELECTRIC

PRECAUTIONS IN HANDLING MOS ICs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

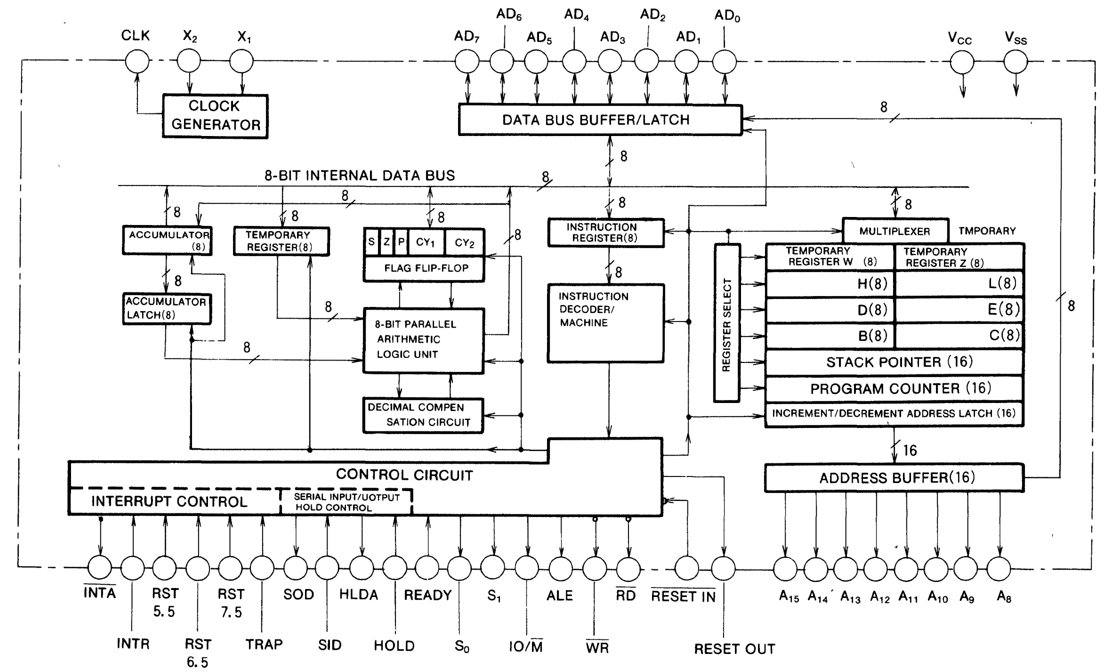
3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1M Ω resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input or output	Functions
X_1, X_2	Clock input	In	These pins are used to connect an external crystal to the internal clock generator An external clock pulse can also be input through X_1
RESET OUT	Reset output	Out	This signal indicates that the CPU is in the reset mode It can be used as a system RESET The signal is synchronised to the processor clock
SOD	Serial output data	Out	This is an output data line for selial data. The output SOD may be set or reset by means of the SIM instruction. It returns to high-level after the RESET.
SID	Serial input data	In	This is an input data line for serial data, and the data on this line is moved to the 7th bit of the accumulator whenever a RIM instruction is executed
TRAP	Trap interrupt	In	A non-maskable restart which is recognized at the same time as an INTR it is not affected by any mask or another interrupt It has the highest interrupt priority
RST5. 5 RST6. 5 RST7. 5	Restart interrupt request	In	Input timing is the same as for INTR for these three signals They all cause an automatic insertion of an internal RESTART RST 7.5 has the highest priority while RST 5.5 has the lowest All three signals have a higher priority than INTR
INTR	Interrupt request signal	In	This signal is for a general purpose interrupt and is sampled only during the last clock cycle of the instruction When an interrupt is acknowledged, the program counter (PC) is held and an $\overline{\text{INTA}}$ signal is generated During this cycle, a RESTART or CALL can be inserted to jump to an interrupt service routine. The interrupt request may be enable and disable by means of software But it is disable by the RESET and immeadiately after an accepted interrupt.
$\overline{\text{INTA}}$	Interrupt acknowledge control signal	Out	This signal is used instead of $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted
$AD_0 \sim AD_7$	Bidirectional address and data bus	In/out	The low-order (I/O address) appears during the first clock cycle During the second and third clock cycles, it becomes the data bus It remains in the bus hold state during the HOLD and HALT modes.
$A_8 \sim A_{15}$	Address bus	Out	Output the high-order 8 bits of the memory address or the 8 bits of the I/O address It remains in the bus hold state during the HOLD and HALT modes.
S_0, S_1	Status	Out	Indicates the status of the bus S_1 S_0 HALT 0 0 WRITE 0 1 READ, DAD 1 0 FETCH 1 1 The S_1 signal can be used as an advanced R/$\overline{\text{W}}$ status
ALE	Address latch enable	Out	This signal is generated during the first clock cycle, to enable the address to be latched into the latches of peripherals The falling edge of ALE is guaranteed to latch the address information The ALE can also be used to strobe the status information, but it is kept in the low-level state during bus idle machine cycles
$\overline{\text{WR}}$	Write control	Out	Indicates that the data on the data bus is to be written into the selected memory at the falling edge of the signal $\overline{\text{WR}}$ It remains the bus hold state during the HOLD and HALT modes
$\overline{\text{RD}}$	Read control	Out	Indicates that the selected memory or I/O address is to be read and that the data bus is active for data transfer It remains in the bus hold state during the HOLD and HALT modes.
IO/$\overline{\text{M}}$	Data transfer control output	Out	This signal indicates whether the read/write is to memory or to I/O_s It remains in the bus hold state during the HOLD and HALT modes
READY	Ready input	In	When it is at high-level during a read or write cycle, the READY indicates that the memory or peripheral is ready to send or receive date. When the signal is at low-level, the CPU will wait for the signal to turn high-level before completing the read or write cycle
$\overline{\text{RESET IN}}$	Reset input	In	This signal (at least three clock cycles are necessary) sets the program counter to zero and resets the interrupt enable and HLDA flip-flops None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset mode as long as the signal is applied
CLK	Clock output	Out	Clock pulses are available from this pin when a crystal is used as an input to the CPU
HLDA	Hold acknowledge signal	Out	By this signal the processor acknowledges the HOLD request signal and indicates that it will relinquish the buses in the next clock cycle The signal is returned to the low-level state after the HOLD request is completed The processor resumes the use of the buses one half clock cycle after the signal HLDA gose low-level
HOLD	Hold request signal	In	When the CPU receives a HOLD request It relinquishes the use of the buses as soon as the current machine cycle is completed The CPU can regain the use of buses only after the HOLD state is removed Upon acknowledging the HOLD signal, the address bus, the data bus, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ lines are put in the bus hold state

Note : HOLD, READY and all interrupt signals are synchronous with clock signal

MACHINE INSTRUCTIONS

Instr class \ Item	Mnemonic	Instruction code D_7D_6	$D_5D_4D_3$	$D_2D_1D_0$	16mal notatn	No of states	No of bytes	No of cycles	Functions	Flags S Z P CY_2 CY_1	Address bus Contents	Mach cycle*	Data bus Contents	I/O	Mach cycle**
Data transfer	MOV r1, r2	0 1	D D D	S S S		4	1	1	$(r_1) \leftarrow (r_2)$	X X X X X					
	MOV M, r	0 1	1 1 0	S S S		7	1	2	$(M) \leftarrow (r)$ Where, $M=(H)(L)$	X X X X X	M	M_4	(r)	O	M_4
	MOV r, M	0 1	D D D	1 1 0		7	1	2	$(r) \leftarrow (M)$ Where, $M=(H)(L)$	X X X X X	M	M_4	(M)	I	M_4
	MVI r, n	0 0	D D D <B2>	1 1 0		7	2	2	$(r) \leftarrow n$	X X X X X			<B2>	I	M_4
	MVI M, n	0 0	1 1 0 <B2>	1 1 0	3 6	10	2	3	$(M) \leftarrow n$ Where, $M=(H)(L)$	X X X X X	M	M_5	<B2>	I	M_5
	LXI B, m	0 0	0 0 0 <B2> <B3>	0 0 1	0 1	10	3	3	$(C) \leftarrow$ <B2> $(B) \leftarrow$ <B3> Where, m = <B3><B2>	X X X X X			<B2> <B3>	I I	M_2 M_3
	LXI D, m	0 0	0 1 0 <B2> <B3>	0 0 1	1 1	10	3	3	$(E) \leftarrow$ <B2> $(D) \leftarrow$ <B3> Where, m = <B3><B2>	X X X X X			<B2> <B3>	I I	M_2 M_3
	LXI H, m	0 0	1 0 0 <B2> <B3>	0 0 1	2 1	10	3	3	$(L) \leftarrow$ <B2> $(H) \leftarrow$ <B3> Where, m = <B3><B2>	X X X X X			<B2> <B3>	I I	M_2 M_3
	LXI SP, m	0 0	1 1 0 <B2> <B3>	0 0 1	3 1	10	3	3	$(SP) \leftarrow m$	X X X X X			<B2> <B3>	I I	M_2 M_3
	SPHL	1 1	1 1 1	0 0 1	F 9	6	1	1	$(SP) \leftarrow (H)(L)$	X X X X X					
	STAX B	0 0	0 0 0	0 1 0	0 2	7	1	2	$((B)(C)) \leftarrow (A)$	X X X X X	(B)(C)	M_4	(A)	O	M_4
	STAX D	0 0	0 1 0	0 1 0	1 2	7	1	2	$((D)(E)) \leftarrow (A)$	X X X X X	(D)(E)	M_4	(A)	O	M_4
	LDAX B	0 0	0 0 1	0 1 0	0 A	7	1	2	$(A) \leftarrow ((B)(C))$	X X X X X	(B)(C)	M_4	((B)(C))	I	M_4
	LDAX D	0 0	0 1 1	0 1 0	1 A	7	1	2	$(A) \leftarrow ((D)(E))$	X X X X X	(D)(E)	M_4	((D)(E))	I	M_4
	STA m	0 0	1 1 0 <B2> <B3>	0 1 0	3 2	13	3	4	$(m) \leftarrow (A)$	X X X X X	m	M_4	(A)	O	M_4
	LDA m	0 0	1 1 1 <B2> <B3>	0 1 0	3 A	13	3	4	$(A) \leftarrow (m)$	X X X X X	m	M_4	(m)	I	M_4
	SHLD m	0 0	1 0 0 <B2> <B3>	0 1 0	2 2	16	3	5	$(m) \leftarrow (L)$ $(m+1) \leftarrow (H)$	X X X X X	m m+1	M_4 M_5	(L) (H)	O O	M_4 M_5
	LHLD m	0 0	1 0 1 <B2> <B3>	0 1 0	2 A	16	3	5	$(L) \leftarrow (m)$ $(H) \leftarrow (m+1)$	X X X X X	m m+1	M_4 M_5	(m) (m+1)	I I	M_4 M_5
	XCHG	1 1	1 0 1	0 1 1	E B	4	1	1	$(H)(L) \leftrightarrow (D)(E)$	X X X X X					
	XTHL	1 1	1 0 0	0 1 1	E 3	16	1	5	$(H)(L) \leftrightarrow ((SP)+1)((SP))$	X X X X X	(SP) (SP)+1	M_2 M_3	((SP)) ((SP)+1)	I I	M_2 M_3
Arithmetic logical compare	ADD r	1 0	0 0 0	S S S		4	1	1	$(A) \leftarrow (A)+(r)$	O O O O O					
	ADD M	1 0	0 0 0	1 1 0	8 6	7	1	2	$(A) \leftarrow (A)+(M)$ Where, $M=(H)(L)$	O O O O O	M	M_4	(M)	I	M_4
	ADI n	1 1	0 0 0 <B2>	1 1 0	C 6	7	2	2	$(A) \leftarrow (A)+n$	O O O O O			<B2>	I	M_4
	ADC r	1 0	0 0 1	S S S		4	1	1	$(A) \leftarrow (A)+(r)+(CY_2)$	O O O O O					
	ADC M	1 0	0 0 1	1 1 0	8 E	7	1	2	$(A) \leftarrow (A)+(M)+(CY_2)$ Where $M=(H)(L)$	O O O O O	M	M_4	(M)	I	M_4
	ACI n	1 1	0 0 1 <B2>	1 1 0	C E	7	2	2	$(A) \leftarrow (A)+n+(CY_2)$	O O O O O			<B2>	I	M_4
	DAD B	0 0	0 0 1	0 0 1	0 9	10	1	3	$(H)(L) \leftarrow (H)(L)+(B)(C)$	X X X O X					
	DAD D	0 0	0 1 1	0 0 1	1 9	10	1	3	$(H)(L) \leftarrow (H)(L)+(D)(E)$	X X X O X					
	DAD H	0 0	1 0 1	0 0 1	2 9	10	1	3	$(H)(L) \leftarrow (H)(L)+(H)(L)$	X X X O X					
	DAD SP	0 0	1 1 1	0 0 1	3 9	10	1	3	$(H)(L) \leftarrow (H)(L)+(SP)$	X X X O X					
	SUB r	1 0	0 1 0	S S S		4	1	1	$(A) \leftarrow (A)-(r)$	O O O O O					
	SUB M	1 0	0 1 0	1 1 0	9 6	7	1	2	$(A) \leftarrow (A)-(M)$ Where, $M=(H)(L)$	O O O O O	M	M_4	(M)	I	M_4
	SUI n	1 1	0 1 0 <B2>	1 1 0	D 6	7	2	2	$(A) \leftarrow (A)-n$	O O O O O			<B2>	I	M_4
	SBB r	1 0	0 1 1	S S S		4	1	1	$(A) \leftarrow (A)-(r)-(CY_2)$	O O O O O					
	SBB M	1 0	0 1 1	1 1 0	9 E	7	1	2	$(A) \leftarrow (A)-(M)-(CY_2)$ Where, $M=(H)(L)$	O O O O O	M	M_4	(M)	I	M_4
	SBI n	1 1	0 1 1 <B2>	1 1 0	D E	7	2	2	$(A) \leftarrow (A)-n-(CY_2)$	O O O O O			<B2>	I	M_4
	ANA r	1 0	1 0 0	S S S		4	1	1	$(A) \leftarrow (A) \wedge (r)$	O O O 0 1					
	ANA M	1 0	1 0 0	1 1 0	A 6	7	1	2	$(A) \leftarrow (A) \wedge (M)$ Where, $M=(H)(L)$	O O O 0 1	M	M_4	(M)	I	M_4
	ANI n	1 1	1 0 0 <B2>	1 1 0	E 6	7	2	2	$(A) \leftarrow (A) \wedge n$	O O O 0 1			<B2>	I	M_4
	XRA r	1 0	1 0 1	S S S		4	1	1	$(A) \leftarrow (A) \forall (r)$	O O O 0 0					
	XRA M	1 0	1 0 1	1 1 0	A E	7	1	2	$(A) \leftarrow (A) \forall (M)$ Where, $M=(H)(L)$	O O O 0 0	M	M_4	(M)	I	M_4
	XRI n	1 1	1 0 1 <B2>	1 1 0	E E	7	2	2	$(A) \leftarrow (A) \forall n$	O O O 0 0			<B2>	I	M_4
	ORA r	1 0	1 1 0	S S S		4	1	1	$(A) \leftarrow (A) \vee (r)$	O O O 0 0					
	ORA M	1 0	1 1 0	1 1 0	B 6	7	1	2	$(A) \leftarrow (A) \vee (M)$ Where, $M=(H)(L)$	O O O 0 0	M	M_4	(M)	I	M_4
	ORI n	1 1	1 1 0 <B2>	1 1 0	F 6	7	2	2	$(A) \leftarrow (A) \vee n$	O O O 0 0			<B2>	I	M_4
	CMP r	1 0	1 1 1	S S S		4	1	1	$(A)-(r)$	O O O O O					
	CMP M	1 0	1 1 1	1 1 0	B E	7	1	2	$(A)-(M)$ Compare, Where, $M=(H)(L)$	O O O O O	M	M_4	(M)	I	M_4
	CPI n	1 1	1 1 1 <B2>	1 1 0	F E	7	2	2	$(A)-n$	O O O O O			<B2>	I	M_4
Register increment/decrement	INR r	0 0	D D D	1 0 0		4	1	1	$(r) \leftarrow (r)+1$	O O O X O					
	INR M	0 0	1 1 0	1 0 0	3 4	10	1	3	$(M) \leftarrow (M)+1$ Where, $M=(H)(L)$	O O O X O	M	M_4	(M)	I	M_4
	DCR r	0 0	D D D	1 0 1		4	1	1	$(r) \leftarrow (r)-1$	O O O X O					
	DCR M	0 0	1 1 0	1 0 1	3 5	10	1	3	$(M) \leftarrow (M)-1$ Where $M=(H)(L)$	O O O X O	M	M_4	(M)	I	M_4
	INX B	0 0	0 0 0	0 1 1	0 3	6	1	1	$(B)(C) \leftarrow (B)(C)+1$	X X X X X					
	INX D	0 0	0 1 0	0 1 1	1 3	6	1	1	$(D)(E) \leftarrow (D)(E)+1$	X X X X X					
	INX H	0 0	1 0 0	0 1 1	2 3	6	1	1	$(H)(L) \leftarrow (H)(L)+1$	X X X X X					
	INX SP	0 0	1 1 0	0 1 1	3 3	6	1	1	$(SP) \leftarrow (SP)+1$	X X X X X					
	DCX B	0 0	0 0 1	0 1 1	0 B	6	1	1	$(B)(C) \leftarrow (B)(C)-1$	X X X X X					
	DCX D	0 0	0 1 1	0 1 1	1 B	6	1	1	$(D)(E) \leftarrow (D)(E)-1$	X X X X X					
	DCX H	0 0	1 0 1	0 1 1	2 B	6	1	1	$(H)(L) \leftarrow (H)(L)-1$	X X X X X					
	DCX SP	0 0	1 1 1	0 1 1	3 B	6	1	1	$(SP) \leftarrow (SP)-1$	X X X X X					
Rotate & shift contents of accumulator	RLC	0 0	0 0 0	1 1 1	0 7	4	1	1	Left shift CY_2 [ ] ← [A_7A_6 … A_1A_0]	X X X O X					
	RRC	0 0	0 0 1	1 1 1	0 F	4	1	1	Right shift CY_2 [ ] ← [A_7A_6 … A_1A_0]	X X X O X					
	RAL	0 0	0 1 0	1 1 1	1 7	4	1	1	Left shift CY_2 [ ] ← [A_7A_6 … A_1A_0]	X X X O X					
	RAR	0 0	0 1 1	1 1 1	1 F	4	1	1	Right shift CY_2 [ ] → [A_7A_6 … A_1A_0]	X X X O X					
Accumu compen	CMA	0 0	1 0 1	1 1 1	2 F	4	1	1	$(A) \leftarrow \overline{(A)}$	X X X X X					
	DAA	0 0	1 0 0	1 1 1	2 7	4	1	1	Results of binary addition are adjusted to BCD	O O O O O					
Carry set	STC	0 0	1 1 0	1 1 1	3 7	4	1	1	$(CY_2) \leftarrow 1$	X X X 1 X					
	CMC	0 0	1 1 1	1 1 1	3 F	4	1	1	$(CY_2) \leftarrow \overline{(CY_2)}$	X X X O X					

* State is T_1 ** State is T_2

MACHINE INSTRUCTIONS SYMBOL MEANING

Symbol	Meaning
r	Register
m	Two-byte data
n	One-byte data
<B2>	Second byte of instruction
<B3>	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, X, CY1, 0, P, X, CY2 (X is indefinite)
PC	Program counter
SP	Stack pointer

Symbol	Meaning
S S S or D D D	Bit pattern designating register or memory. Where M = (H) (L)

Register or memory	S S S or D D D
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memoy location
V	Inclusive OR
⊻	Exclusive OR
Λ	Logical AND
—	1s complement
X	Content of flag is not changed after execution
O	Content offlag is set or reset after execution
I	Input mode
O	Output mode

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	2.5	mA
Topr	Operating free-air temperature range		−20~75	℃
Tstg	Storge temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20~75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{IHX}	X_1, X_2 High-level voltage		4.0		V_{CC}+0.3	V
$V_{IH(\overline{RESIN})}$	High-level reset input voltage		2.4		V_{CC}+0.3	V
$V_{IL(\overline{RESIN})}$	Low-level reset input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_{CC}	Supply current from (Operation)			15	20	mA
	Supply current from V_{CC} (HALT)			7	10	mA
I_{CCS}	Supply current from V_{CC} (Stand by)	(Note 1)		20	30	μA
I_I	Input leak current	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
I_{BHH}	Input current bus hold high	V_I=3.0V (Note 2)	−50		−400	μA
I_{BHL}	Input current bus hold low	V_I=0.8V (Note 3)	50		400	μA
C_i	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			10	pF
C_O	Output terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			15	pF
$C_{I/O}$	Input/Output terminal capacitance	V_{CC}=V_{SS}, f=1MHz 25mVrms, T_a=25℃ (Note 4)			20	pF

Note 1 : I_{CCS} should be measured after execution HALT instruction and then fixing clock on V_{CC} or V_{SS}
V_I=V_{CC} or V_{SS}, V_{CC}=5.5V, outputs unloaded.
Note 2 : I_{BHH} should be measured after rasing V_{IN} in bushold status to V_{CC} and setting it for 3.0V.
Measurable pins ; AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$
Note 3 : I_{BHL} should be measured after lowering V_{IN} in bushold status to V_{SS} and setting it for 0.8V.
Measurable pins ; AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$
Note 4 : Unmeasured pins should be connected to V_{SS}.

Parameters described in the timing requirements and switching characteristics take relevant values in accordance with the relational expression shown in the following tables when the frequency is varied.

Relational expression with the frequency T ($t_{C(CLK)}$) in the M5M80C85AP-2

TIMMING REQUIREMENTS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

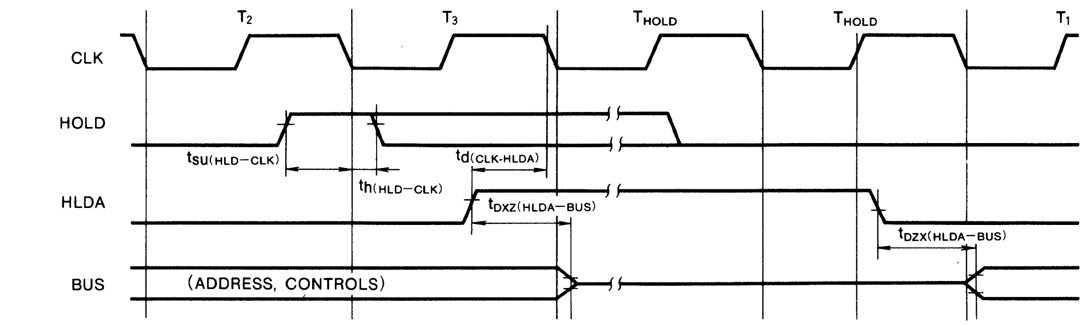
Symbol	Parameter	Test conditions	Relational expression (Note 6)	Limit
$t_{su(DA-AD)}$	DA input setup time	C_L = 150pF	170−(5/2+N)T	Min
$t_{su(DA-\overline{RD})}$	DA input setup time		150−(3/2+N)T	Min
$t_{su(RDY-AD)}$	READY input setup time		200−(3/2)T	Min
$t_{su(DA-ALE)}$	DA input setup time		150−(2+N)T	Min

SWITCHING CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

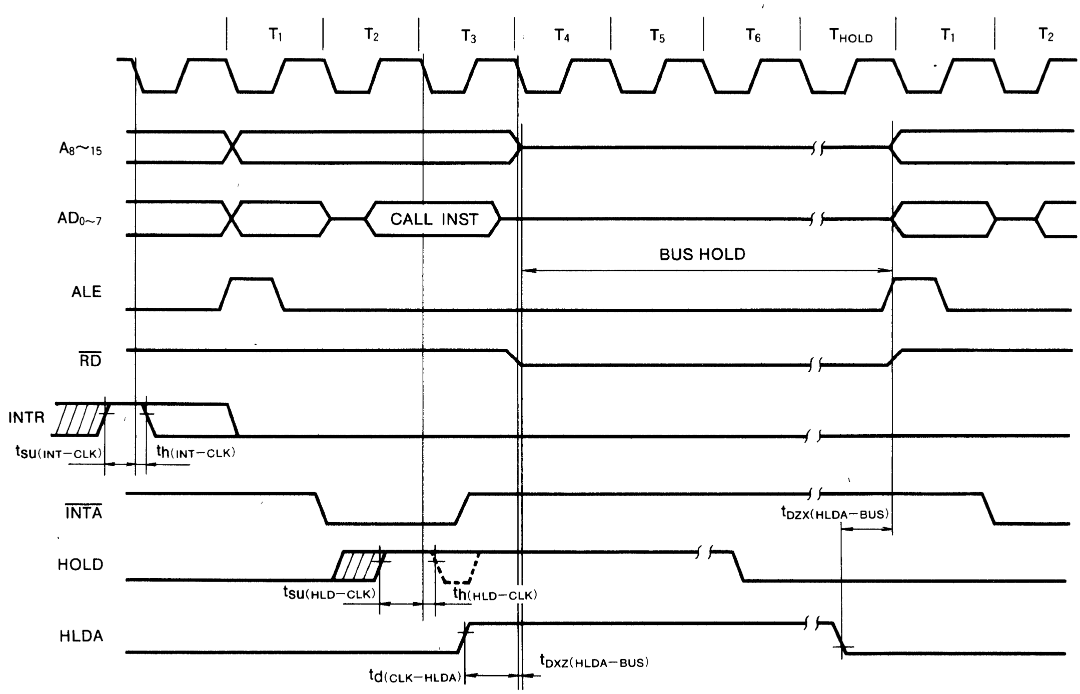
Symbol	Palameter		Test conditions	Relational expression (Note 6)	Limit
$t_{w(\overline{CLK})}$	CLK output low-level pulse width		C_L=150pF	(1/2)T−60	Min
$t_{w(CLK)}$	CLK output high-level pulse width			(1/2)T−30	Min
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		(1/2)T−50	Min
		A_8~A_{15}		(1/2)T−50	
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			(1/2)T−50	Min
$t_{w(ALE)}$	ALE pulse width			(1/2)T−20	Min
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			(1/2)T−50	Min
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			(1/2)T−40	Min
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read			(1/2)T−10	Min
$t_{d(CONT-AD)}$	Address valid time after control signal			(1/2)T−40	Min
$t_{d(DA-\overline{WR})}$	Delay time, data output to $\overline{WR}$ signal			(3/2+N)T−70	Min
$t_{d(\overline{WR}-DA)}$	Delay time $\overline{WR}$ signal to data output			(1/2)T−40	Min
$t_{w(\overline{CONT})}$	Control signal pulse width			(3/2+N)T−70	Min
$t_{d(CONT-ALE)}$	Delay time, CONT to ALE signal			(1/2)T−75	Min
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			(1/2)T−60	Min
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA			(1/2)T+50	Max
$t_{DZX(HLDA-BUS)}$	Bus enable time from HLDA			(1/2)T+50	Max
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			(3/2)T−80	Min
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		T−85	Min
		A_8~A_{15}		T−85	

Note 6 N indicates the total number of wait cycles
$T=t_{C(CLK)}$

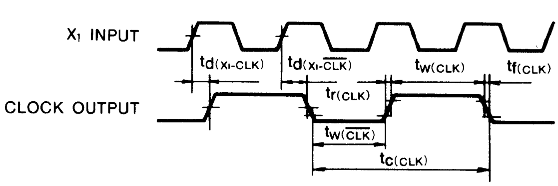
Hold Cycle



Interrupt and Hold Cycle



Clock Output Timing Waveform



DRIVING CIRCUIT OF X_1 AND X_2 INPUTS

Input terminals, X_1 and X_2 of the M5M80C85AP-2 can be driven by either a crystal or external clock. Since the driver clock frequency is divided to 1/2 internally, the input frequency required is twice the actual execution frequency (10MHz for the M5M80C85AP-2 which is operated at 5MHz)

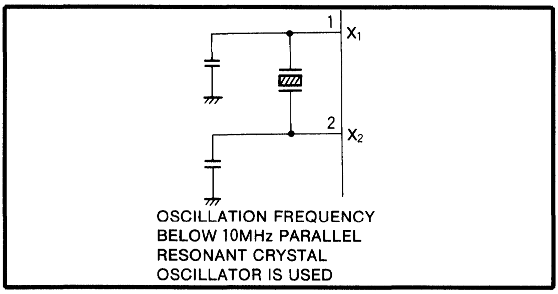
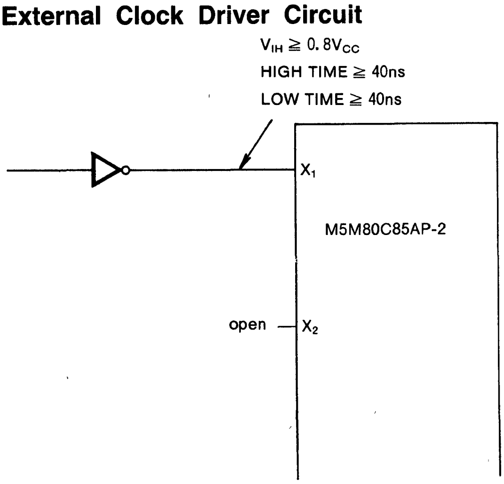


Fig. 5 Connections when crystal is used for X_1 and X_2 inputs

Fig. 5 is a typical connection diagrams for a crystal respectively.

External Clock Driver Circuit



WAIT STATE GENERATOR

Fig. 6 shows a typical 1-wait state generator for low speed RAM and ROM applications.

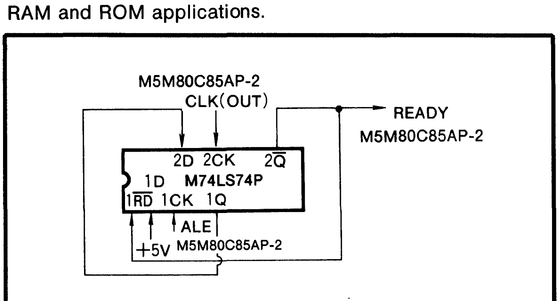


Fig. 6 1-wait state generator

RELATION OF RIM AND SIM INSTRUCTIONS WITH THE ACCUMULATOR (SUPPLEMENTARY DESCRIPTION).

The contents of the accumulator after the execution of a RIM instruction is shown in Fig. 7 .

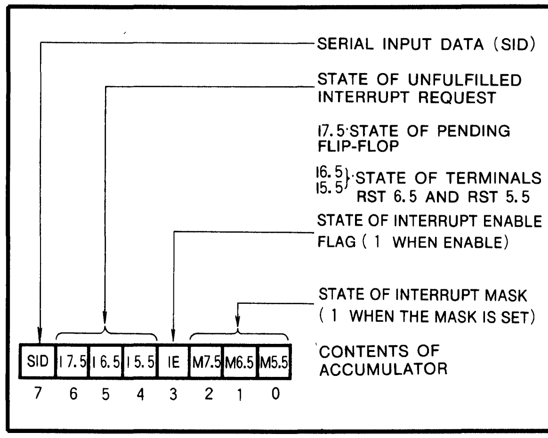


Fig.7 Relation of the SIM instruction RIM with the accumulator

The contents of the accumulator after the execution of a SIM instruction is shown in Fig. 8 .

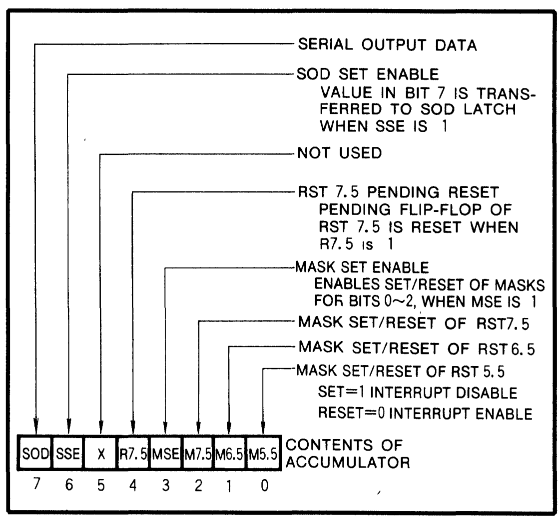


Fig. 8 Relation of the SIM instruction with the accumulator

PIN DESCRIPTIONS

Pin	Name	Input or output	Functions
X_1, X_2	Clock input	In	These pins are used to connect an external crystal or RC circuit to the internal clock generator An external clock pulse can also be input through X_1
RESET OUT	Reset output	Out	This signal indicates that the CPU is in the reset mode It can be used as a system RESET The signal is synchronised to the processor clock
SOD	Serial output data	Out	This is an output data line for serial data The output SOD may be set or reset by means of the SIM instruction It returns to high-level after the RESET
SID	Serial input data	In	This is an input data line for serial data, and the data on this line is moved to the 7th bit of the accumulator whenever a RIM instruction is executed.
TRAP	Trap interrupt	In	A non-maskable restart which is recognized at the same time as an INTR it is not affected by any mask or another interrupt It has the highest interrupt priority
RST5. 5 RST6. 5 RST7. 5	Restart interrupt request	In	Input timing is the same as for INTR for these three signals They all cause an automatic insertion of an internal RESTART RST 7. 5 has the highest priority while RST 5. 5 has the lowest All three signals have a higher priority than INTR
INTR	Interrupt request signal	In	This signal is for a general purpose interrupt and is sampled only during the last clock cycle of the instruction When an interrupt is acknowledged, the program counter (PC) is held and an $\overline{\text{INTA}}$ signal is generated During this cycle, a RESTART or CALL can be inserted to jump to an interrupt service routine The interrupt request may be enable and disable by means of software But it is disable by the RESET and immeadiately after an accepted interrupt
$\overline{\text{INTA}}$	Interrupt acknowledge control signal	Out	This signal is used instead of $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted
$AD_0 \sim AD_7$	Bidirectional address and data bus	In/out	The low-order (I/O address) appears during the first clock cycle During the second and third clock cycles, it becomes the data bus It remains in the high-impedance state during the HOLD and HALT modes
$A_8 \sim A_{15}$	Address bus	Out	Output the high-order 8 bits of the memory address or the 8 bits of the I/O address It remains in the high-impedance state during the HOLD and HALT modes
S_0, S_1	Status	Out	Indicates the status of the bus S_1 S_0 HALT 0 0 WRITE 0 1 READ, DAD 1 0 FETCH 1 1 The S_1 signal can be used as an advanced R/$\overline{\text{W}}$ status
ALE	Address latch enable	Out	This signal is generated during the first clock cycle, to enable the address to be latched into the latches of peripherals The falling edge of ALE is guaranteed to latch the address information The ALE can also be used to strobe the status information, but it is kept in the low-level state during bus idle machine cycles.
$\overline{\text{WR}}$	Write control	Out	Indicates that the data on the data bus is to be written into the selected memory at the falling edge of the signal $\overline{\text{WR}}$ It remains the high-impedance state during the HOLD and HALT modes
$\overline{\text{RD}}$	Read control	Out	Indicates that the selected memory or I/O address is to be read and that the data bus is active for data transfer It remains in the high-impedance state during the HOLD and HALT modes
IO/$\overline{\text{M}}$	Data transfer control output	Out	This signal indicates whether the read/write is to memory or to I/Os It remains in the high-ipedance state during the HOLD and HALT modes
READY	Ready input	In	When it is at high-level during a read or write cycle, the READY indicates that the memory or peripheral is ready to send or receive date When the signal is at low-level, the CPU will wait for the signal to turn high-level before completing the read or write cycle
$\overline{\text{RESET IN}}$	Reset input	In	This signal (at least three clock cycles are necessary) sets the program counter to zero and resets the interrupt enable and HLDA flip-flops None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset mode as long as the signal is applied
CLK	Clock output	Out	Clock pulses are available from this pin when a crystal or RC circuit is used as an input to the CPU
HLDA	Hold acknowledge signal	Out	By this signal the processor acknowledges the HOLD request signal and indicates that it will relinquish the buses in the next clock cycle The signal is returned to the low-level state after the HOLD request is completed The processor resumes the use of the buses one half clock cycle after the signal HLDA gose low-level
HOLD	Hold request signal	In	When the CPU receives a HOLD request It relinquishes the use of the buses as soon as the current machine cycle is completed The CPU can regain the use of buses only after the HOLD state is removed Upon acknowledging the HOLD signal, the address bus, the data bus, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ lines are put in the high-impedance state

Note HOLD, READY and all interrupt signals are synchronous with clock signal

MACHINE INSTRUCTIONS

Instr class	Mnemonic	D_7D_6	$D_5D_4D_3$	$D_2D_1D_0$	16mal notatn	No of states	No of bytes	No of cycles	Functions	Flags S Z P CY_2 CY_1	Address bus Contents	Address bus Mach cycle*	Data bus Contents	Data bus I/O	Data bus Mach cycle**
Data transfer	MOV r1, r2	01	DDD	SSS		4	1	1	$(r_1) \leftarrow (r_2)$	X X X X X					
	MOV M, r	01	110	SSS		7	1	2	(M) ← (r) Where M = (H)(L)	X X X X X	M	M_4	(r)	O	M_4
	MOV r, M	01	DDD	110		7	1	2	(r) ← (M) Where M = (H)(L)	X X X X X	M	M_4	(M)	I	M_4
	MVI r, n	00	DDD $\langle B_2\rangle$	110		7	2	2	(r) ← n	X X X X X			$\langle B_2\rangle$	I	M_4
	MVI M, n	00	110 $\langle B_2\rangle$	110	36	10	2	3	(M) ← n Where M = (H)(L)	X X X X X	M	M_5	$\langle B_2\rangle$	I	M_5
	LXI B, m	00	000 $\langle B_2\rangle$ $\langle B_3\rangle$	001	01	10	3	3	(C) ← $\langle B_2\rangle$ (B) ← $\langle B_3\rangle$ Where, m = $\langle B_3\rangle\langle B_2\rangle$	X X X X X			$\langle B_2\rangle$ $\langle B_3\rangle$	I I	M_2 M_3
	LXI D, m	00	010 $\langle B_2\rangle$ $\langle B_3\rangle$	001	11	10	3	3	(E) ← $\langle B_2\rangle$ (D) ← $\langle B_3\rangle$ Where m = $\langle B_3\rangle\langle B_2\rangle$	X X X X X			$\langle B_2\rangle$ $\langle B_3\rangle$	I I	M_2 M_3
	LXI H, m	00	100 $\langle B_2\rangle$ $\langle B_3\rangle$	001	21	10	3	3	(L) ← $\langle B_2\rangle$ (H) ← $\langle B_3\rangle$ Where m = $\langle B_3\rangle\langle B_2\rangle$	X X X X X			$\langle B_2\rangle$ $\langle B_3\rangle$	I I	M_2 M_3
	LXI SP, m	00	110 $\langle B_2\rangle$ $\langle B_3\rangle$	001	31	10	3	3	(SP) ← m	X X X X X			$\langle B_2\rangle$ $\langle B_3\rangle$	I I	M_2 M_3
	SPHL	11	111	001	F9	6	1	1	(SP) ← (H)(L)	X X X X X					
	STAX B	00	000	010	02	7	1	2	((B)(C)) ← (A)	X X X X X	(B)(C)	M_4	(A)	O	M_4
	STAX D	00	010	010	12	7	1	2	((D)(E)) ← (A)	X X X X X	(D)(E)	M_4	(A)	O	M_4
	LDAX B	00	001	010	0A	7	1	2	(A) ← ((B)(C))	X X X X X	(B)(C)	M_4	((B)(C))	I	M_4
	LDAX D	00	011	010	1A	7	1	2	(A) ← ((D)(E))	X X X X X	(D)(E)	M_4	((D)(E))	I	M_4
	STA m	00	110 $\langle B_2\rangle$ $\langle B_3\rangle$	010	32	13	3	4	(m) ← (A)	X X X X X	m	M_4	(A)	O	M_4
	LDA m	00	111 $\langle B_2\rangle$ $\langle B_3\rangle$	010	3A	13	3	4	(A) ← (m)	X X X X X	m	M_4	(m)	I	M_4
	SHLD m	00	100 $\langle B_2\rangle$ $\langle B_3\rangle$	010	22	16	3	5	(m) ← (L) (m + 1) ← (H)	X X X X X	m m + 1	M_4 M_5	(L) (H)	O O	M_4 M_5
	LHLD m	00	101 $\langle B_2\rangle$ $\langle B_3\rangle$	010	2A	16	3	5	(L) ← (m) (H) ← (m + 1)	X X X X X	m m + 1	M_4 M_5	(m) (m + 1)	I I	M_4 M_5
	XCHG	11	101	011	EB	4	1	1	(H)(L) ↔ (D)(E)	X X X X X					
	XTHL	11	100	011	E3	16	1	5	(H)(L) ↔ ((SP) + 1)((SP))	X X X X X	(SP) (SP) + 1	M_2 M_3	((SP)) ((SP) + 1)	I I	M_2 M_3
Arithmetic logical compare	ADD r	10	000	SSS		4	1	1	(A) ← (A) + (r)	O O O O O					
	ADD M	10	000	110	86	7	1	2	(A) ← (A) + (M) Where M · (H)(L)	O O O O O	M	M_4	(M)	I	M_4
	ADI n	11	000 $\langle B_2\rangle$	110	C6	7	2	2	(A) ← (A) + n	O O O O O			$\langle B_2\rangle$	I	M_4
	ADC r	10	001	SSS		4	1	1	(A) ← (A) + (r) + (CY_2)	O O O O O					
	ADC M	10	001	110	8E	7	1	2	(A) ← (A) + (M) + (CY_2) Where M (H)(L)	O O O O O	M	M_4	(M)	I	M_4
	ACI n	11	001 $\langle B_2\rangle$	110	CE	7	2	2	(A) ← (A) + n + (CY_2)	O O O O O			$\langle B_2\rangle$	I	M_4
	DAD B	00	001	001	09	10	1	3	(H)(L) ← (H)(L) + (B)(C)	X X X O X					
	DAD D	00	011	001	19	10	1	3	(H)(L) ← (H)(L) + (D)(E)	X X X O X					
	DAD H	00	101	001	29	10	1	3	(H)(L) ← (H)(L) + (H)(L)	X X X O X					
	DAD SP	00	111	001	39	10	1	3	(H)(L) ← (H)(L) + (SP)	X X X O X					
	SUB r	10	010	SSS		4	1	1	(A) ← (A) (r)	O O O O O					
	SUB M	10	010	110	96	7	1	2	(A) ← (A) (M) Where, M (H)(L)	O O O O O	M	M_4	(M)	I	M_4
	SUI n	11	010 $\langle B_2\rangle$	110	D6	7	2	2	(A) ← (A) n	O O O O O			$\langle B_2\rangle$	I	M_4
	SBB r	10	011	SSS		4	1	1	(A) ← (A) - (r) — (CY_2)	O O O O O					
	SBB M	10	011	110	9E	7	1	2	(A) ← (A) (M) (CY_2) Where M (H)(L)	O O O O O	M	M_4	(M)	I	M_4
	SBI n	11	011 $\langle B_2\rangle$	110	DE	7	2	2	(A) ← (A) - n (CY_2)	O O O O O			$\langle B_2\rangle$	I	M_4
	ANA r	10	100	SSS		4	1	1	(A) ← (A) ∧ (r)	O O O 0 1					
	ANA M	10	100	110	A6	7	1	2	(A) ← (A) ∧ (M) Where M (H)(L)	O O O 0 1	M	M_4	(M)	I	M_4
	ANI n	11	100 $\langle B_2\rangle$	110	E6	7	2	2	(A) ← (A) ∧ n	O O O 0 1			$\langle B_2\rangle$	I	M_4
	XRA r	10	101	SSS		4	1	1	(A) ← (A) ∀ (r)	O O O 0 0					
	XRA M	10	101	110	AE	7	1	2	(A) ← (A) ∀ (M) Where M (H)(L)	O O O 0 0	M	M_4	(M)	I	M_4
	XRI n	11	101 $\langle B_2\rangle$	110	EE	7	2	2	(A) ← (A) ∀ n	O O O 0 0			$\langle B_2\rangle$	I	M_4
	ORA r	10	110	SSS		4	1	1	(A) ← (A) ∨ (r)	O O O 0 0					
	ORA M	10	110	110	B6	7	1	2	(A) ← (A) ∨ (M) Where, M = (H)(L)	O O O 0 0	M	M_4	(M)	I	M_4
	ORI n	11	110 $\langle B_2\rangle$	110	F6	7	2	2	(A) ← (A) ∨ n	O O O 0 0			$\langle B_2\rangle$	I	M_4
	CMP r	10	111	SSS		4	1	1	(A) − (r)	O O O O O					
	CMP M	10	111	110	BE	7	1	2	(A) − (M) Compare, Where M (H)(L)	O O O O O	M	M_4	(M)	I	M_4
	CPI n	11	111 $\langle B_2\rangle$	110	FE	7	2	2	(A) n	O O O O O			$\langle B_2\rangle$	I	M_4
Register increment/decrement	INR r	00	DDD	100		4	1	1	(r) ← (r) + 1	O O O X O					
	INR M	00	110	100	34	10	1	3	(M) ← (M) + 1 Where M (H)(L)	O O O X O	M	M_4	(M)	I	M_4
	DCR r	00	DDD	101		4	1	1	(r) ← (r) − 1	O O O X O					
	DCR M	00	110	101	35	10	1	3	(M) ← (M) − 1 Where, M (H)(L)	O O O X O	M	M_4	(M)	I	M_4
	INX B	00	000	011	03	6	1	1	(B)(C) ← (B)(C) + 1	X X X X X					
	INX D	00	010	011	13	6	1	1	(D)(E) ← (D)(E) + 1	X X X X X					
	INX H	00	100	011	23	6	1	1	(H)(L) ← (H)(L) + 1	X X X X X					
	INX SP	00	110	011	33	6	1	1	(SP) ← (SP) + 1	X X X X X					
	DCX B	00	001	011	0B	6	1	1	(B)(C) ← (B)(C) 1	X X X X X					
	DCX D	00	011	011	1B	6	1	1	(D)(E) ← (D)(E) 1	X X X X X					
	DCX H	00	101	011	2B	6	1	1	(H)(L) ← (H)(L) 1	X X X X X					
	DCX SP	00	111	011	3B	6	1	1	(SP) ← (SP) 1	X X X X X					
Rotate & shift contents of accumulator	RLC	00	000	111	07	4	1	1	Left shift CY_2 ← A_7A_6 … A_1A_0	X X X O X					
	RRC	00	001	111	0F	4	1	1	Right shift CY_2 ← A_7A_6 … A_1A_0	X X X O X					
	RAL	00	010	111	17	4	1	1	Left shift CY_2 ← A_7A_6 … A_1A_0	X X X O X					
	RAR	00	011	111	1F	4	1	1	Right shift CY_2 → A_7A_6 … A_1A_0	X X X O X					
Accumu compen	CMA	00	101	111	2F	4	1	1	(A) ← $\overline{(A)}$	X X X X X					
	DAA	00	100	111	27	4	1	1	Results of binary addition are adjusted to BCD	O O O O O					
Carry set	STC	00	110	111	37	4	1	1	(CY_2) ← 1	X X X 1 X					
	CMC	00	111	111	3F	4	1	1	(CY_2) ← $\overline{(CY_2)}$	X X X O X					

* State is T_1 ** State is T_2

MACHINE INSTRUCTIONS SYMBOL MEANING

Symbol	Meaning
r	Register
m	Two-byte data
n	One-byte data
⟨B2⟩	Second byte of instruction
⟨B3⟩	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, X, CY1, 0, P, X, CY2 (X is indefinite)
PC	Program counter
SP	Stack pointer

Symbol	Meaning
S S S or D D D	Bit pattern designating register or memory. Where M = (H) (L)

Register or memory	S S S or D D D
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memoy location
V	Inclusive OR
$\forall$	Exclusive OR
Λ	Logical AND
—	1 s complement
X	Content of flag is not changed after execution
O	Content of flag is set or reset after execution
I	Input mode
O	Output mode

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
Pd	Power dissipation	T_a=25℃	1.5	W
Topr	Operating free-air temperature range		−20~75	℃
Tstg	Storge temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage (Except for X_1, X_2)		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.6	V
$V_{IH(\overline{RESIN})}$	High-level reset input voltage		2.4		V_{CC}+0.5	V
$V_{IL(\overline{RESIN})}$	Low-level reset input voltage		−0.5		0.8	V
V_{IHX}	X_1, X_2 High-level voltage		4.0		V_{CC}+0.5	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_{CC}	Supply current from V_{CC}	(Note 2)			200	mA
I_I	Input leak current, except $\overline{\text{RESET IN}}$ (Note 1)	V_I=V_{CC}	−10		10	μA
I_{OZL}	Output floating leak current	V_O=0.45V~V_{CC}	−10		10	μA
V_{IH}−V_{IL}	Hysterisis $\overline{\text{RESET IN}}$ input		0.25			V

Note 1 The input $\overline{\text{RESET IN}}$ is pulled up to V_{CC} with the resistor 3kΩ (typ) when $V_I \geqq V_{IH(\overline{RESIN})}$
2 Maximum I_{CC} is 170mA at T_a = 0~70℃

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Paramater	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(CLK)}$	Clock cycle time	$t_{C(CLK)} \geqq$ 320ns, C_L=150pF	320		2000	ns
$t_{SU(DA-AD)}$	DA input setup time		−575			ns
$t_{SU(DA-\overline{RD})}$	DA input setup time		−300			ns
$t_{h(DA-\overline{RD})}$	DA input hold time		0			ns
$t_{SU(RDY-AD)}$	READY input setup time		−220			ns
$t_{SU(RDY-CLK)}$	READY input setup time				−110	ns
$t_{h(RDY-CLK)}$	READY input hold time		0			ns
$t_{SU(DA-ALE)}$	DA input setup time		−460			ns
$t_{SU(HLD-CLK)}$	HOLD input setup time		170			ns
$t_{h(HLD-CLK)}$	HLD input hold time		0			ns
$t_{SU(INT-CLK)}$	Interrupt setup time		160			ns
$t_{h(INT-CLK)}$	Interrupt hold time		0			ns
$t_{SU(RDY-ALE)}$	READY input setup time		−110			ns

Parameters described in the timing requirements and switching characteristics take relevant values in accordance with the relational expression shown in the following tables when the frequency is varied.

Relational Expression with the frequency T ($t_{C(CLK)}$) in the M5L8085AP

TIMMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

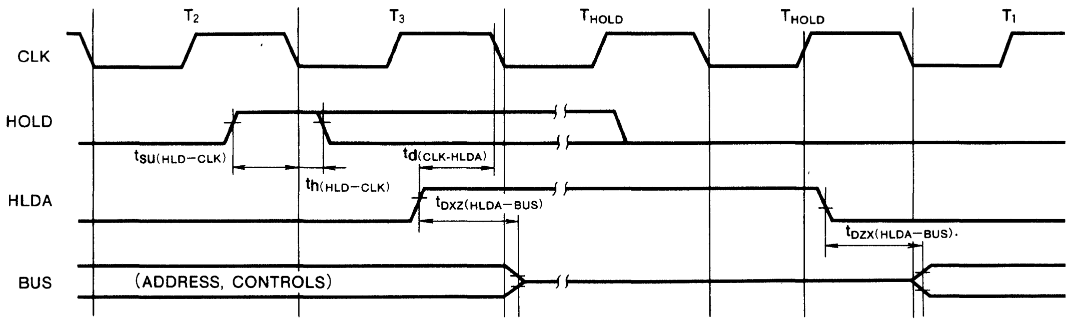
Symbol	Parameter	Test conditions	Relational expression (Note 6)	Limit
$t_{su(DA-AD)}$	DA input setup time	C_L=150pF	225−(5/2+N)T	Min
$t_{su(DA-\overline{RD})}$	DA input setup time		180−(3/2+N)T	Min
$t_{su(RDY-AD)}$	READY input setup time		260−(3/2)T	Min
$t_{su(DA-ALE)}$	DA input setup time		180−2T	Min

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise notes)

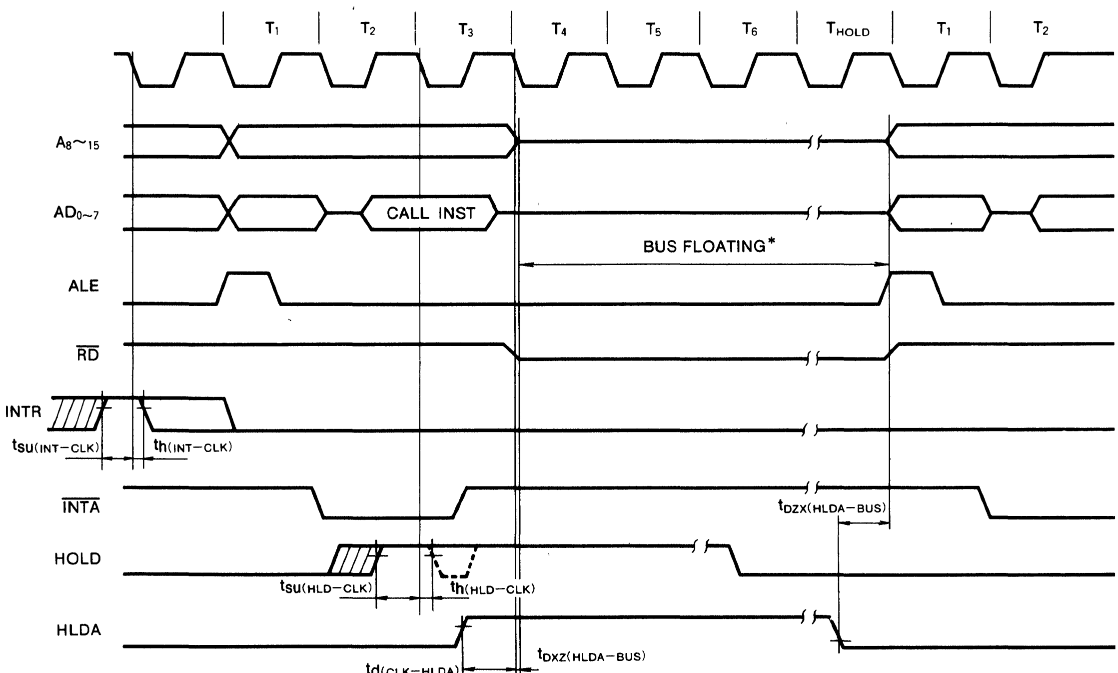
Symbol	Palameter		Test conditions	Relational expression (Note 6)	Limit
$t_{W(\overline{CLK})}$	CLK output low-level pulse width		C_L=150pF	(1/2)T−80	Min
$t_{W(CLK)}$	CLK output high-level pulse width			(1/2)T−40	Min
$t_{d(AD-ALE)}$	Delay time, address output to ALE signal	AD_0~AD_7		(1/2)T−70	Min
		A_8~A_{15}		(1/2)T−45	
$t_{d(ALE-AD)}$	Delay time, ALE signal to address output			(1/2)T−60	Min
$t_{W(ALE)}$	ALE pulse width			(1/2)T−20	Min
$t_{d(ALE-CLK)}$	Delay time, ALE to CLK			(1/2)T−60	Min
$t_{d(ALE-\overline{CONT})}$	Delay time, ALE to control signal			(1/2)T−30	Min
$t_{DZX(\overline{RD}-AD)}$	Address enable time from read			(1/2)T−10	Min
$t_{d(CONT-AD)}$	Address valid time after control signal			(1/2)T−40	Min
$t_{d(DA-\overline{WR})}$	Delay time, data output to $\overline{WR}$ signal			(3/2+N)T−60	Min
$t_{d(\overline{WR}-DA)}$	Delay time $\overline{WR}$ signal to data output			(1/2)T−60	Min
$t_{W(\overline{CONT})}$	Control signal pulse width			(3/2+N)T−80	Min
$t_{d(CONT-ALE)}$	Delay time, CONT to ALE signal			(1/2)T−110	Min
$t_{d(CLK-HLDA)}$	Delay time, CLK to HLDA signal			(1/2)T−50	Min
$t_{DXZ(HLDA-BUS)}$	Bus disable time from HLDA			(1/2)T+50	Max
$t_{DZX(HLDA-BUS)}$	Bus enable time from HLDA			(1/2)T+50	Max
$t_{d(CONT-\overline{CONT})}$	Control signal disable time			(3/2)T−80	Min
$t_{d(AD-\overline{CONT})}$	Delay time, address output to control signal	AD_0~AD_7		T−80	Min
		A_8~A_{15}		T−50	

Note 6 N indicates the total number of wait cycles
T=$t_{C(CLK)}$

Hold Cycle

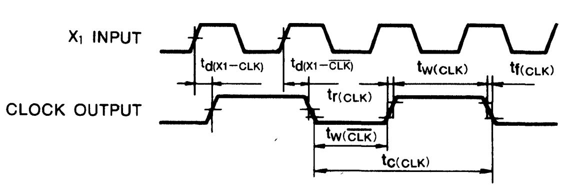


Interrupt and Hold Cycle



*IO/M is floating during this time

Clock Output Timing Waveform



PULL-UP OF THE $\overline{\text{RESET IN}}$ INPUT

In order to increase the noise margin, the $\overline{\text{RESET IN}}$ input terminal is pulled up by about 3kΩ (typ) when the condition $V_I \geqq V_{IH(\overline{RESIN})}$ is satisfied. Fig. 5 is a connection diagram of the $\overline{\text{RESET IN}}$ input, and Fig. 6 shows the relation between input voltage and input current.

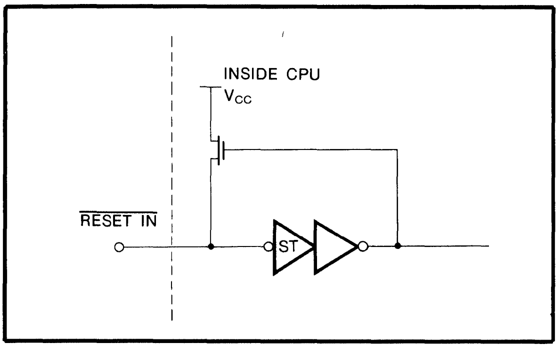


Fig. 5 Connections of $\overline{\text{RESET IN}}$ input

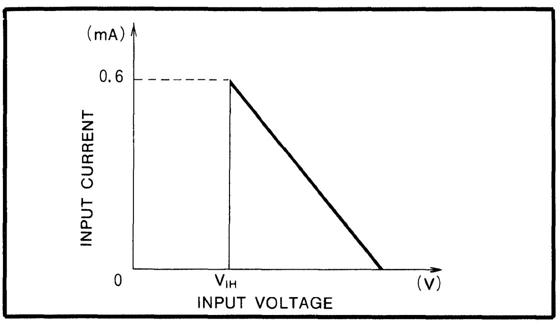
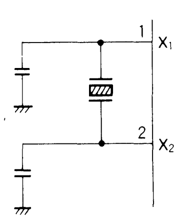


Fig. 6 $\overline{\text{RESET IN}}$ input current vs input voltage

DRIVING CIRCUIT OF X_1 AND X_2 INPUTS

Input terminals, X_1 and X_2 of the M5L8085AP can be driven by either a crystal, RC network, or external clock. Since the driver clock frequency is divided to 1/2 internally, the input frequency required is twice the actual execution frequency (6MHz for the M5L8085AP which is operated at 3MHz). Fig. 7 are typical connection diagram for a crystal circuit respectively.



OSCILLATION FREQUENCY 1~6MHz PARALLEL RESONANT CRYSTAL OSCILLATOR IS USED

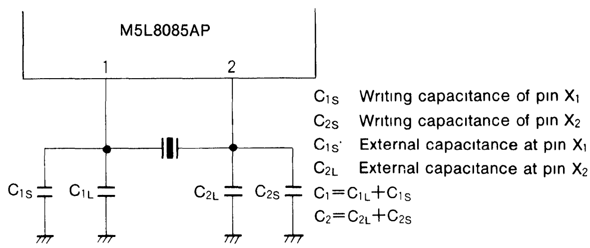
Fig. 7 Connections when crystal is used for X_1 and X_2 inputs

Conditions for Using a Quartz Crystal Element

1. Quartz Crystal Specifications

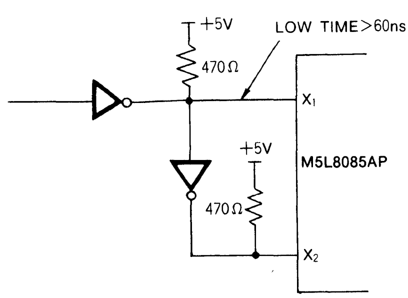
- Parallel resonance
- The frequency is 2 times the operation frequency (2 ~ 6.25MHz)
- Internal load capacitance: Approx. 16pF
- Parallel capacitance: Below 7pF
- Equivalent resistance: Below 75 Ω (for operation above 4MHz)
- For operation in the range 2 ~ 4MHz, the resistance showld be made as small as possible.
- Drive capability: Above 5mW (the power at which the crystal will be destoryed)

2. External Circuitry



- For operation above 4MHz:
  $C_1 = C_2 = 10pF$
- For operation below 4MHz:
  $C_1 = C_2 = 15pF$

External Clock Driver Circuit



Pullup resistors are required to assure that the high level voltage of the input is at least 4V

M5L8212P

8-BIT INPUT/OUTPUT PORT WITH 3-STATE OUTPUT

DESCRIPTION

The M5L8212P is an input/output port consisting of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also a service request flip-flop for the generation and control of interrupts to a microprocessor is included.

FEATURES

- Parallel 8-bit data register and buffer
- Service request flip-flop for interrupt generation
- Three-state outputs
- Low input load current: $I_{IL}=-250\mu A$(max.)
- High output sink current: $I_{OL}=16mA$(max.)
- High-level output voltage for direct interface to a M5L8085AP, CPU: $V_{OH}=3.65V$(min.)

APPLICATION

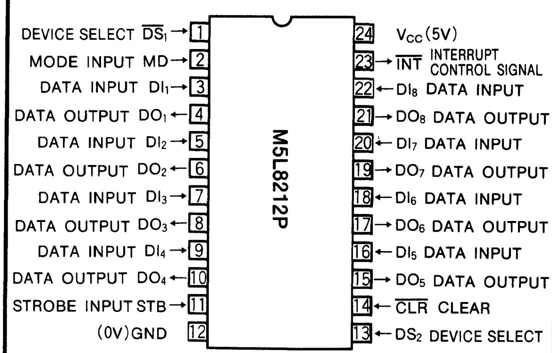
Input/output port for a M5L8085AP
Latches, gate buffers or multiplexers
Peripheral and input/output functions for microcomputer systems

FUNCTION

Device select 1 ($\overline{DS_1}$) and device select 2 (DS_2) are used for chip selection when the mode input MD is low. When $\overline{DS_1}$ is low and DS_2 is high, the data in the latches is transferred to the data outputs $DO_1 \sim DO_8$, and the service request flip-flop SR is set. Also, the strobed input STB is active, the data inputs $DI_1 \sim DI_8$ are latched in the data latches, and the service request flip-flop SR is reset.

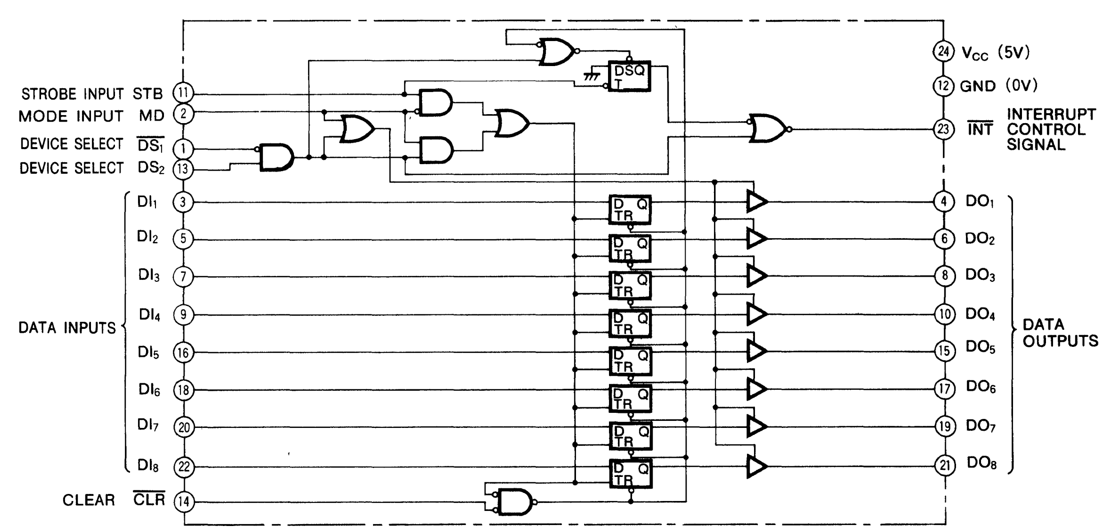
When MD is high, the data in the data latches is transferred to the data outputs. When $\overline{DS_1}$ is low and DS_2 is high, the data inputs are latched in the data latches. The low-level clear input $\overline{CLR}$ resets the data latches and sets the service request flip-flop SR, but the state of the output buffers is not changed.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4

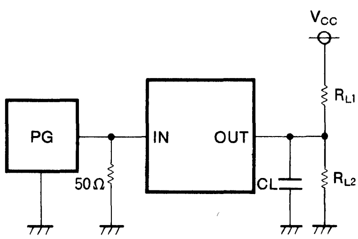
BLOCK DIAGRAM



SWITCHING CHARACTERISTICS (T_a=0~75℃, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{PHL(DI-DO)}$ $t_{PLH(DI-DO)}$	High-to-low-level and low-to-high-level output propagation time, from input DI to output DO	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			30	ns
$t_{PHL(DS2-DO)}$ $t_{PLH(DS2-DO)}$	High-to-low-level and low-to-high-level output propagation time. from input $\overline{DS1}$, DS2 and STB to output DO				40	ns
$t_{PHL(STB-\overline{INT})}$	High-to-low-level output propagation time, from input STB to output $\overline{INT}$				40	ns
$t_{PZL(MD-DO)}$ $t_{PZH(MD-DO)}$	Z-to-low-level and Z-to-high-level output propagation time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω C_L=30pF, R_{L1}=10kΩ, R_{L2}=1kΩ			45	ns
$t_{PHZ(MD-DO)}$ $t_{PLZ(MD-DO)}$	High-to-Z-level and low-to-Z-level output propagation time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ C_L=5pF, R_{L1}=300Ω, R_{L2}=600Ω			45	ns
$t_{PHL(\overline{CLR}-DO)}$	High-to-low-level output propagation time, from input $\overline{CLR}$ to output DO	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			55	ns

Note 4 : Test circuit



M5L8216P / M5L8226P

4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS

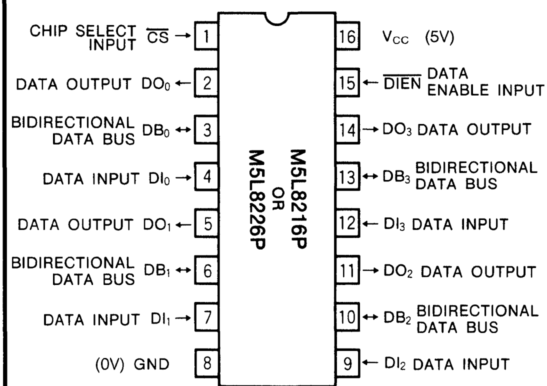
DESCRIPTION

The M5L8216P and M5L8226P are 4-bit bidirectional bus drivers and suitable for the 8-bit parallel CPU M5L8085AP.

FEATURES

- Parallel 8-bit data bus buffer driver
- Low input current $\overline{DIEN}$, $\overline{CS}$: $I_{IL}=-500\mu A$(max.)
  DI, DB: $I_{IL}=-250\mu A$(max.)
- High output current M5L8216P
  DB: $I_{OL}=55mA$(max.)
  $I_{OH}=-10mA$(max.)
  DO: $I_{OH}=-1mA$(max.)
  M5L8226P
  DB: $I_{OL}=50mA$(max.)
  $I_{OH}=-10mA$(max.)
  DO: $I_{OH}=-1mA$(max.)
- Outputs can be connected with the CPU M5L8085AP: $V_{OH}=3.65V$(min.)
- Three-state output

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

APPLICATION

Bidirectional bus driver/receiver for various types of microcomputer systems.

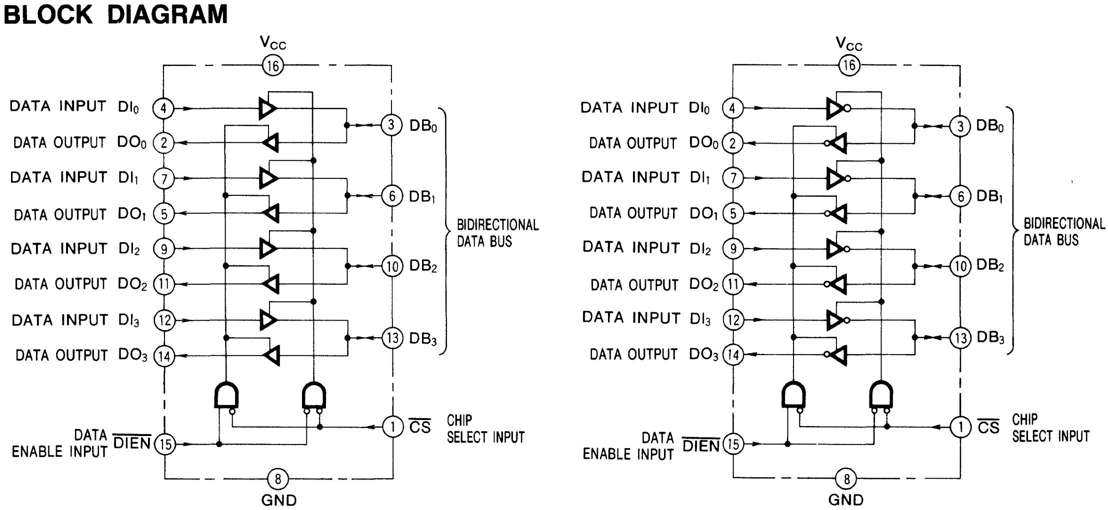
FUNCTION

The M5L8216P is a non-inverting and the M5L8226P is an inverting 4-bit bidirectional bus driver.

When the terminal $\overline{CS}$ is high-level, all outputs are in high-impedance state, and when low-level, the direction of the bidirectional bus can be controlled by the terminal $\overline{DIEN}$.

The terminal $\overline{DIEN}$ controls the data flow. The data flow control is performed by placing one of a pair of buffers in high-impedance state and allowing the other to transfer the data.

BLOCK DIAGRAM

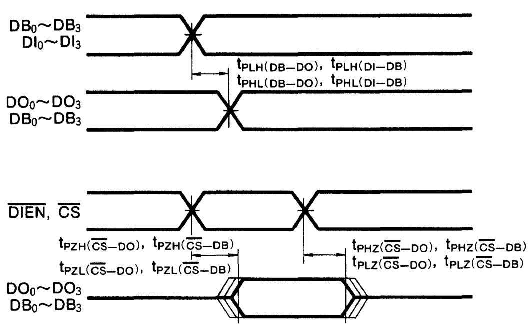


M5L8216P　　M5L8226P

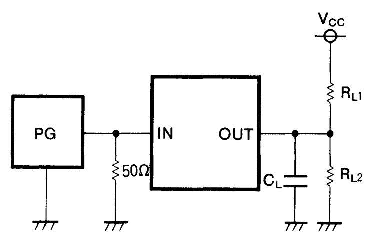
SWITCHING CHARACTERISTICS (V_{CC}=5V±5%, T_a=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions (Note 3)	Limits Min	Limits Typ	Limits Max	Unit
$t_{PHL(DB-DO)}$ $t_{PLH(DB-DO)}$	High-to-low and low-to-high output propagation time. from input DB to output DO		C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			25	ns
$t_{PHL(DI-DB)}$ $t_{PLH(DI-DB)}$	High-to-low and low-to-high output propagation time. from input DI to output DB	M5L8216P	C_L=300pF, R_{L1}=90Ω, R_{L2}=180Ω			30	ns
		M5L8226P				25	
$t_{PHZ(\overline{CS}-DO)}$	High-to-Z and low-to-Z output propagation time. from inputs $\overline{DIEN}$ $\overline{CS}$. to output DO		C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ			35	ns
$t_{PLZ(\overline{CS}-DO)}$			C_L=5pF, R_{L1}=300Ω, R_{L2}=600Ω				
$t_{PZH(\overline{CS}-DO)}$	Output enable time. from inputs $\overline{DIEN}$ $\overline{CS}$ to output DO	M5L8216P	C_L=30pF, R_{L1}=10kΩ, R_{L2}=1kΩ			65	ns
		M5L8226P				54	
$t_{PZL(\overline{CS}-DO)}$		M5L8216P	C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω			65	ns
		M5L8226P				54	
$t_{PHZ(\overline{CS}-DB)}$	Output disable time. from inputs $\overline{DIEN}$. $\overline{CS}$ to output DB		C_L=5pF, R_{L1}=10kΩ, R_{L2}=1kΩ			35	ns
$t_{PLZ(\overline{CS}-DB)}$			C_L=5pF, R_{L1}=90Ω, R_{L2}=180Ω				
$t_{PZH(\overline{CS}-DB)}$	Output enable time from inputs $\overline{DIEN}$. $\overline{CS}$. to output DB	M5L8216P	C_L=300pF, R_{L1}=10kΩ, R_{L2}=1kΩ			65	ns
		M5L8226P				54	
$t_{PZL(\overline{CS}-DB)}$		M5L8216P	C_L=300pF, R_{L1}=90Ω, R_{L2}=180Ω			65	ns
		M5L8226P				54	

TIMING DIAGRAM (Reference level=1.5V)



Note 3 : Test circuit



APPLICATION EXAMPLES

Fig. 1 shows a pair of M5L8216Ps or M5L8226Ps which are directly connected with the 8080A CPU data bus, and their control signal. Fig. 2 shows an example circuit in which the M5L8216P or M5L8226P is used as an interface for memory and I/O to a bidirectional bus.

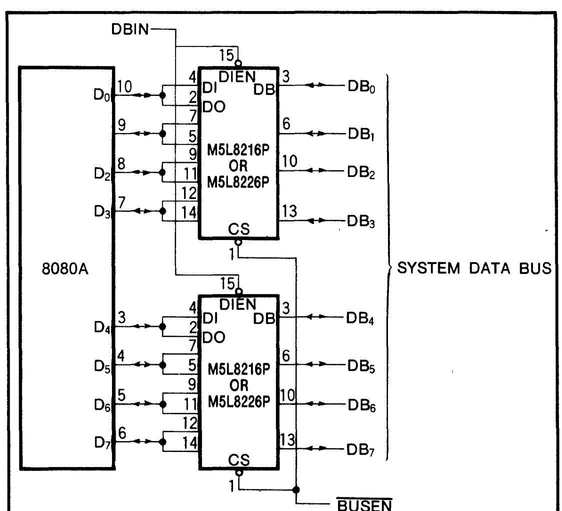


Fig. 1 Data bus buffer

ABSOLUTE MAXIMUM RATINGS (Ta=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	V_{OH}≧2.4V	0		−5	mA
I_{OL}	Low-level output current	V_{OL}≦0.45V	0		32	mA

ELECTRICAL CHARACTERISTICS (Ta=0~75℃, unless otherwise noted)

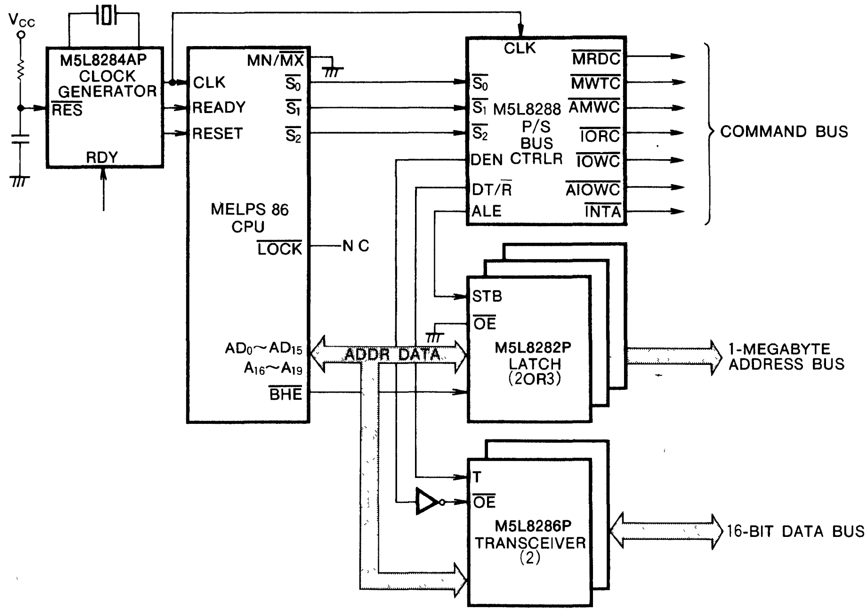
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−5mA			−1	V
V_{OH}	High-level output voltage	V_{CC}=4.5V, I_{OH}=−5mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=32mA			0.45	V
I_{OZH}	Off-state output current, high-level applied to the output	V_{CC}=5.5V, V_I=2V, V_O=5.25V			50	μA
I_{OZL}	Off-state output current, low-level applied to the output	V_{CC}=5.5V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=5.25V			50	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.45V			−0.2	mA
I_{CC}	Supply current	V_{CC}=5.5V			80	mA
C_{IN}	Input capacitance	F=1MHz, V_{BIAS}=2.5V V_{CC}=5V, T_a=25℃			12	pF

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~75℃, unless otherwise noted)

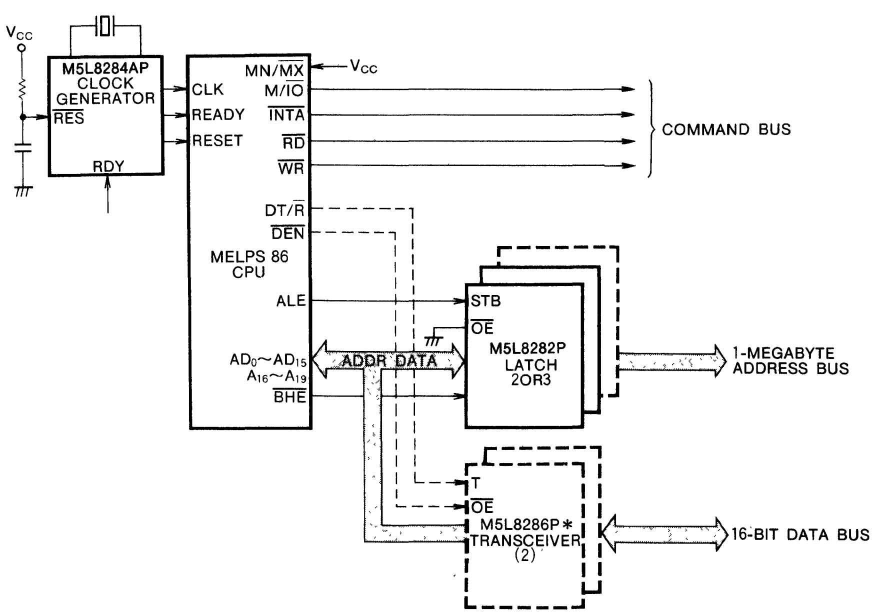
Symbol	Parameter	Alternate symbol	Test conditions	M5L8282P			M5L8283P			Unit
				Limits			Limits			
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation time from DI input to DO or $\overline{DO}$ for low-to-high or high-to-low change	T_{IVOV}	(Note 1)	5		30	5		22	ns
t_{PLH} t_{PHL}	Propagation time from STB input to DO or $\overline{DO}$ for low-to-high and high-to-low change	T_{SHOV}		10		45	10		40	ns
t_{PZH} t_{PZL}	Propagation time from $\overline{OE}$ input to DO or $\overline{DO}$ output when output is enabled	T_{ELOV}		10		30	10		30	ns
t_{PHZ} t_{PLZ}	Propagation time from $\overline{OE}$ input to DO or DO output when the output is disabled	T_{EHOV}		5		18	5		18	ns

APPLICATION EXAMPLES

(1) Use in the maximum mode



(2) Use in the minimum mode



* : Option
Required when the number of devices driving the bus increases

PIN DESCRIPTIONS

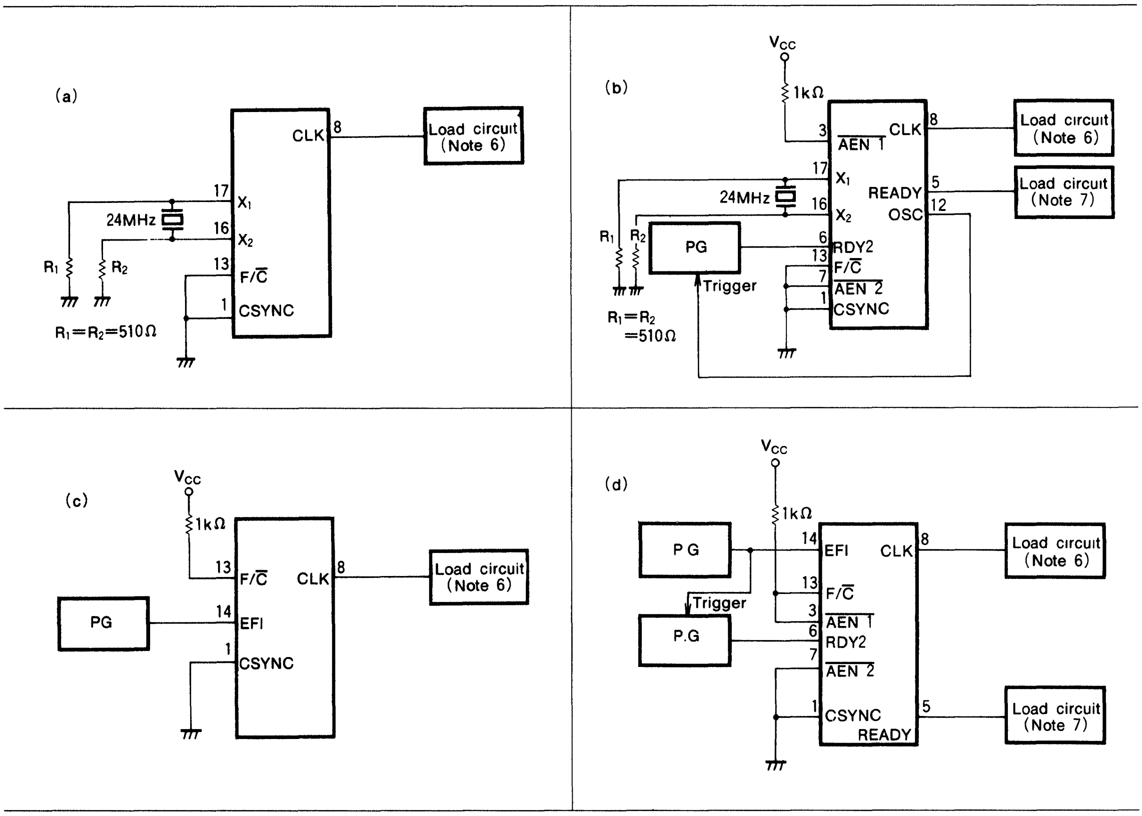
Pin	Name	Input or output	Function
$\overline{AEN1}$, $\overline{AEN2}$	Address enable input	Input	When $\overline{AEN1}$ and $\overline{AEN2}$ are set low, RDY1 and RDY2 are enabled, respectively. By using these two inputs separately, the CPU can be used to access two Multibusses. When not used as a multimaster, $\overline{AEN}$ should be set to low. These inputs are active low.
RDY1, RDY2	Bus ready input	Input	These inputs are connected to the output signal indicating the completion of data reception from a system bus device or, indicating that data is valid RDY1 and RDY2 are.enabled when AEN1 and AEN2 are low, respectively. These inputs are active high.
$\overline{ASYNC}$	Active low input	Input	This signal is used to select the synchronization mode of the READY signal generation circuit. When the $\overline{ASYNC}$ signal is set low, the READY signal is generated in two synchronization steps. When the $\overline{ASYNC}$ signal is set high, the READY signal is generated in one step
READY	Ready output	Output	The state of RDY appears at this output in synchronization with the CLK output This is done to synchronize the READY output to the M5L8284AP internal clock because the RDY input generation is unrelated to the CLK signal. This pin is normally connected to the CPU ready input and cleared after the required hold CPU time has elapsed.
X_1, X_2	Crystal element terminals	Input	These pins are used to connect the crystal. The crystal frequency is 3 times of CPU clock frequency The crystal should be in the 12-25MHz range with the series resistance as possible as small. Care should be taken that these pins are not shorted to ground
F/$\overline{C}$	Clock selection input	Input	When F/$\overline{C}$ is set low, CLK and PCLK outputs are driven from the crystal oscillator circuit When it is set high, they are driven from the EFI input.
EFI	External clock input	Input	When F/$\overline{C}$ is set high, CLK and PCLK output signals are driven from this pin. A TTL level rectangular signal and three times of the CPU frequency should be used.
CLK	Clock output	Output	This output is connected to the clock inputs of the CPU and the peripheral devices on the local bus. The output waveform is 1/3 the frequency of the crystal oscillator connected at X_1 and X_2 or the signal applied to the FEI input, and has a duty cycle of 1/3. Since for V_{CC}=5V, V_{OH}=4.5V, this output can be directly drive the CPU clock input.
PCLK	Peripheral clock output	Output	This output provides a clock signal for use with peripheral devices. The output waveform is 50% duty cycle TTL level rectangular waveform with a frequency 1/2 that of the clock output.
OSC	Oscillator output	Output	This output is a TTL level crystal oscillator output. The frequency is the same as that of the crystal connected at X_1 and X_2, but care should be taken as the frequency will be unstable if these pins are left open.
$\overline{RES}$	Reset input	Input	This active low input is used to generate the reset output signal for the CPU The input is a schmitt trigger input so that by connecting a capacitor and a resistor, the CPU reset signal can be generated at power on.
RESET	Reset output	Output	This pin is connected to the CPU reset input. The signal at this pin is synchronized the $\overline{RES}$ input with the CLK signal. This output is active high.
CSYNC	Clock synchronization input	Input	When using multiple M5L8284AP devices, this input is used as a clock synchronization input When CSYNC is high, the internal counter of the M5L8284AP is reset and when CSYNL is low, it begins operation. CSYNC must be synchronized with EFI. See application notes.

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

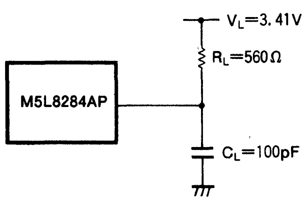
Symbol	Parameter	Alternate symbol	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
T_C	CLK repetition period	t_{CLCL}		100			ns
$T_{W(CLKH)}$	CLK high pulse width	t_{CHCL}	(Note 5 a, b) $CLKF_{req}$≦8MHz	($\frac{1}{3}t_{CLCL}$)+2			ns
			$CLKF_{req}$=10MHz	39			
$T_{W(CLKL)}$	CLK low pulse width	t_{CLCH}	(Note 5 a, b) $CLKF_{req}$≦8MHz	($\frac{2}{3}t_{CLCL}$)−15			ns
			$CLKF_{req}$=10MHz	53			
t_{TLH}	CLK low-high transition time	t_{CH1CH2}	1~3.5V			10	ns
t_{THL}	CLK high-low transition time	t_{CL2CL1}	3.5~1V			10	ns
$T_{W(PCLKH)}$	PCLK high pulse width	t_{PHPL}		t_{CLCL}−20			ns
$T_{W(PCLKL)}$	PCLK low pulse width	t_{PLPH}		t_{CLCL}−20			ns
t_{dIV}	READY inhibit time with respect to CLK (Note 1)	t_{RYLCL}	(Note 5 c, d)	−8			ns
t_{dV}	READY enable time with respect to CLK (Note 2)	t_{RYHCH}	(Note 5 c, d) $CLKF_{req}$≦8MHz	53			ns
			$CLKF_{req}$=10MHz				
$T_{DHL(CLK-RESET)}$	High-low delay time from CLK to RESET	t_{CLIL}				40	ns
$T_{DLH(CLK-PCLK)}$	Low-high delay time from CLK to PCLK	t_{CLPH}				22	ns
$T_{DHL(CLK-PCLK)}$	High-low delay time from CLK to PCLK	t_{CLPL}				22	ns
$T_{DLH(OSC-CLK)}$	Low-high delay time from OSC to CLK	t_{OLCH}		−5		22	ns
$T_{DHL(OSC-CLK)}$	High-low delay time from OSC to CLK	t_{OLCL}		2		35	ns
T_r	Output rise time	t_{OLOH}	0.8~2V (except CLK)			20	ns
t_f	Output fall time	t_{OHOL}	2~0.8V (except CLK)			12	ns

Note 1 : Applies to T2 state time
2 : Applies to T3 and TW state times

Note 5 : Test Circuits

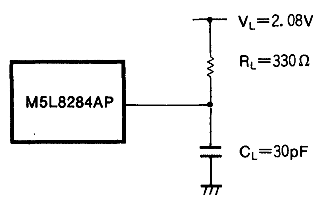


Note 6 : Load Circuit



CLK pins

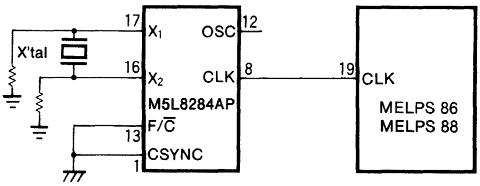
Note 7 : Load circuit



Other pins

APPLICATION NOTES

(1) Connecting the crystal

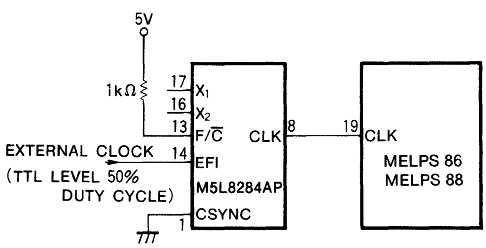


The crystal frequency should be three times the cycle time of the 8086, 8088 or 8089, and the crystal should be located as close to the M5L8284AP as possible.

PRECAUTIONS FOR USE

(1) The oscillator circuit of the M5L8284AP is designed for use with the fundamental mode crystal.
If noise is allowed to enter the XTAL1, XTAL2 or V_{CC} pins, the oscillator frequency will be pulled of the parallel resident frequency and the stray capacitance between XTAL1 and XTAL2 may cause the circuit to go into relaxation oscillation. To prevent this, care should be given to the following points.
(1) The should be one with a small parallel capacitance.
(2) A 0.01 − 0.1μF capacitor should be connected between V_{CC} and ground. This capacitor should be located as close as possible to the IC.

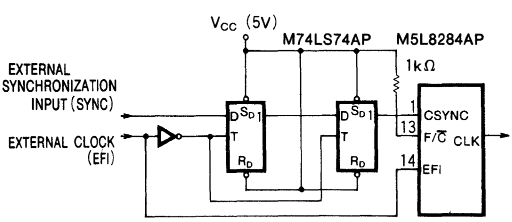
(2) External clock connections



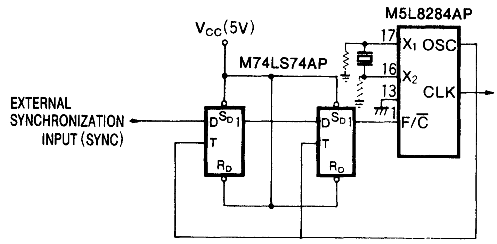
The frequency should be three times the CPU cycle frequency

(3) Synchronizing using the CSYNC input

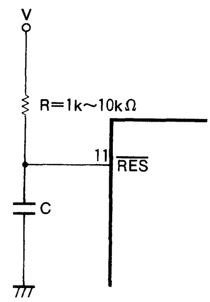
● **When the EFI input is used**



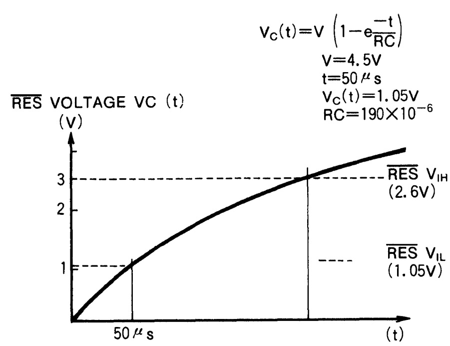
● **When the EFI input is not used**



(4) Power-on reset circuit



Since the MELPS 86, 88 require a reset pulse over 50μs after V_{CC} reaches 4.5V upon power on, the capacitor value should be determined by the graph shown below. Note that the time for V_{CC} to reach 4.5V has not been considered, so that it is necessary to choose the characteristics value of capacitance under consideration of the power supply.



CHANGES IN RES INPUT VOLTAGE

M5L8286P/M5L8287P

OCTAL BUS TRANSCEIVER

DESCRIPTION

The M5L8286P and M5L8287P are semiconductor integrated circuits consisting of a set of eight 3-state output bus transceivers for use with a variety of microprocessor systems.

FEATURES

- 3-state, high-fanout outputs ($I_{OL}=16mA$, $I_{OH}=-1mA$ for the A outputs and $I_{OL}=32mA$, $I_{OH}=-5mA$ for the B outputs)
- Low power dissipation

APPLICATION

Two-way bus transceivers for microcomputer systems

FUNCTION

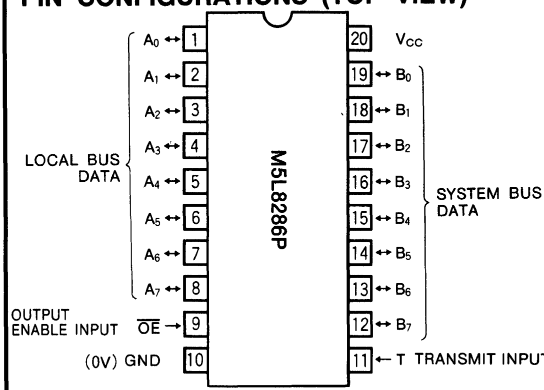
The M5L8286P and M5L8287P are two-way bus transceivers with non-inverted and inverted outputs respectively.

When the output enable input $\overline{OE}$ is high, the local bus data pins $A_0 \sim A_7$ and system data pins $B_0 \sim B_7$ are both placed in the high-impedance state.

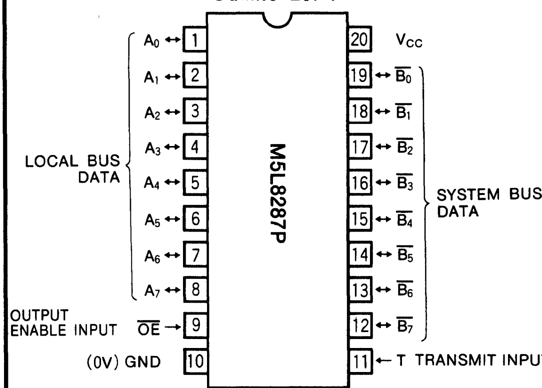
When the output enable input $\overline{OE}$ is low, the input and output states are controlled by the transmit input T.

When T is high, $A_0 \sim A_7$ are input pins and $B_0 \sim B_7$ are output pins. When T is low, $B_0 \sim B_7$ are input pins and $A_0 \sim A_7$ are output pins.

PIN CONFIGURATIONS (TOP VIEW)

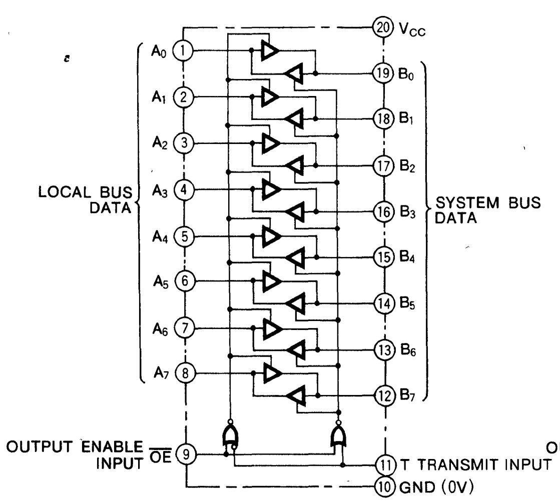


Outline 20P4

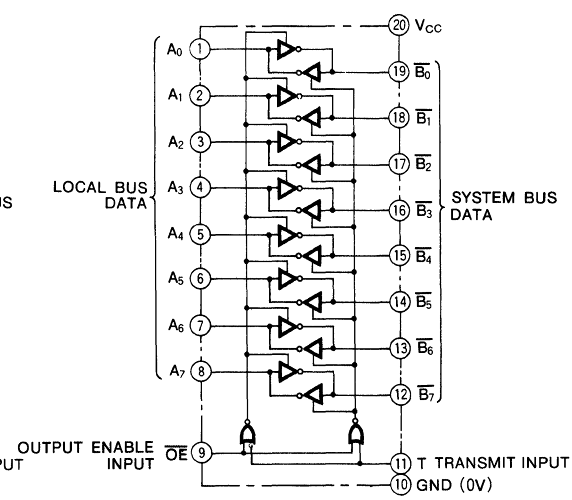


Outline 20P4

BLOCK DIAGRAM



M5L8286P



M5L8287P

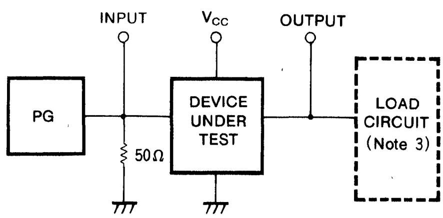
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	M5L8286P			M5L8287P			Unit
				Limits			Limits			
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Low-level to high-level and high-level and low-level transition time from input A B to outputs B, A	TIVOV	(Note 2)	5		30	5		22	ns
t_{PZH} t_{PZL}	Output enable time from $\overline{OE}$ input to A or B output	TELOV		10		30	10		30	ns
t_{PHZ} t_{PLZ}	Output disable time from $\overline{OE}$ input to A or B output	TEHOZ		5		18	5		18	ns

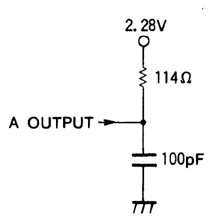
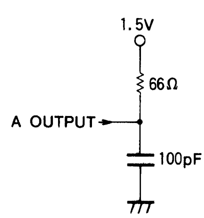
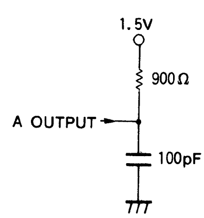
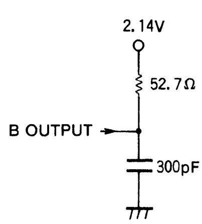
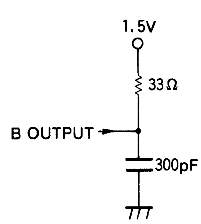
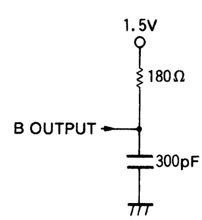
TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate Symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_{SU}	T setup time with respect to $\overline{OE}$	T_{TVFL}		10			ns
t_h	T hold time with respect to $\overline{OE}$	T_{EHTV}		5			ns

Note 2 : Test Circuit



Note 3

Test Item	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
A OUTPUT LOAD CIRCUIT			
B OUTPUT LOAD CIRCUIT			

DESCRIPTION

The M5L8288P is a semiconductor integrated circuit consisting of a bus controller and bus driver for the MELPS 86, 88, 16-bit microprocessors. By using the status signals from the CPU a Multibus (Intel trademark) control signal is generated.

FEATURES

- High-fanout outputs
  Command output $I_{OL}=32mA$, $I_{OH}=-5mA$
  Control output $I_{OL}=16mA$, $I_{OH}=-1mA$
- Advanced command outputs ($\overline{AIOWC}$ and $\overline{AMWC}$ outputs)
- Low power dissipation

APPLICATION

Bus controller and bus driver for maximum mode operation of the MELPS 86, 88

FUNCTION

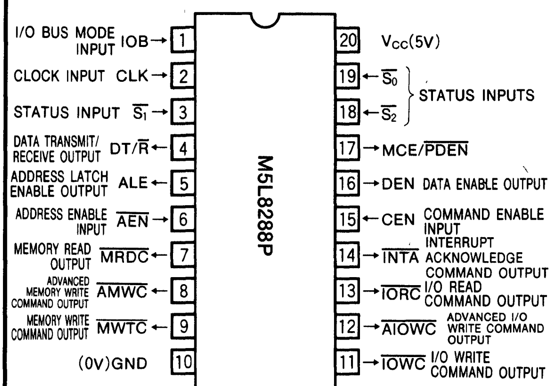
The M5L8288P is a bus controller and driver for maximum mode operation of theMELPS 86, 88 processors.

The command signals and control signals are decoded by means of the $\overline{S_0}\sim\overline{S_2}$ outputs from the CPU and the control signals for I/O devices and memory are output.

The device can be used in the Multimaster mode in which several CPUs acting as masters are connected to one data bus. An input pin for the control signal $\overline{AEN}$ from an 8289 bus arbiter is provided.

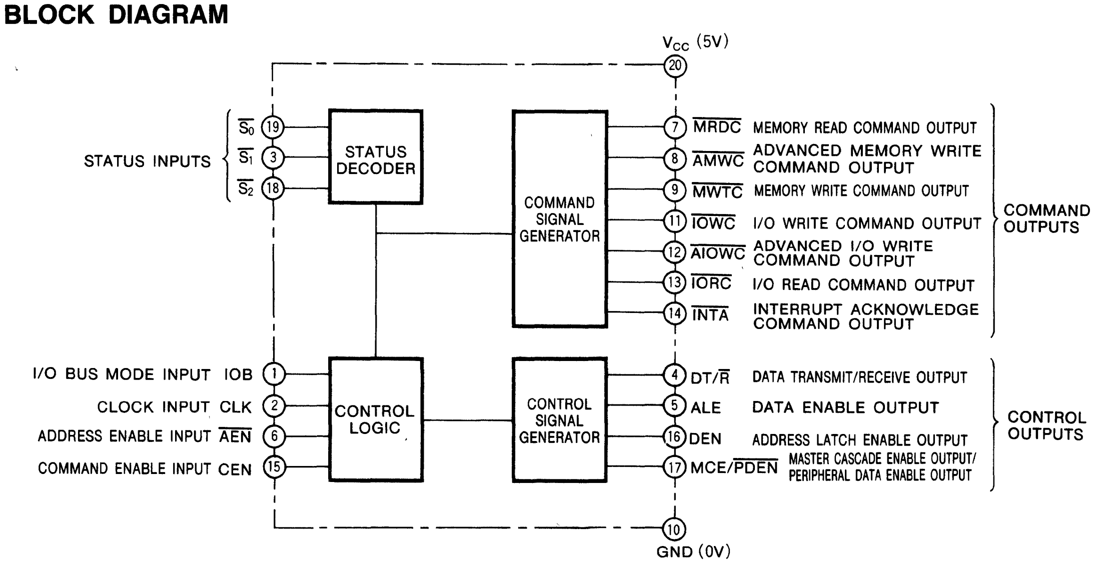
By using the M5L8288P as a bus controller, a highperformance 16-bit microcomputer system can be configured.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The state of the command outputs and control outputs are determined by the CPU status outputs $\overline{S_0} \sim \overline{S_2}$. The table summarizes the states of the outputs $\overline{S_0} \sim \overline{S_2}$ and their corresponding valid command output names.

Depending upon whether the M5L8288S is in the I/O bus mode or system bus mode, the command output sequence will vary.

STATUS INPUTS AND COMMAND OUTPUTS RELATIONSHIPS

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	8086, 8088 status	Valid command output name
L	L	L	Interrupt acknowledge	$\overline{INTA}$
L	L	H	Data read from an I/O port	$\overline{IORC}$
L	H	L	Data write to an I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
L	H	H	Halt	—
H	L	L	Instruction fetch	$\overline{MRDC}$
H	L	H	Read data from memory	$\overline{MRDC}$
H	H	L	Write data to memory	$\overline{MWTC}$, $\overline{AMWC}$
H	H	H	Passive state	—

1. I/O bus mode operation

When IOB is high, the M5L8288S function in the I/O bus mode.

In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

2. System bus mode operation

When IOB is set to low, the M5L8288S enters the system bus mode. In this mode no command is issued until 115 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

3. $\overline{AMWC}$ and $\overline{AIOWC}$ outputs

With respect to the normal write control signals $\overline{MWTC}$ and $\overline{IOWC}$, the advanced-write command signals $\overline{AMWC}$ and $\overline{AIOWC}$ transit low one clock cycle earlier and remain low for two clock cycles.

These signals are used with peripheral devices or static RAM devices which require a long write pulse, so that the CPU does not go into an unnecessarily wait cycle.

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

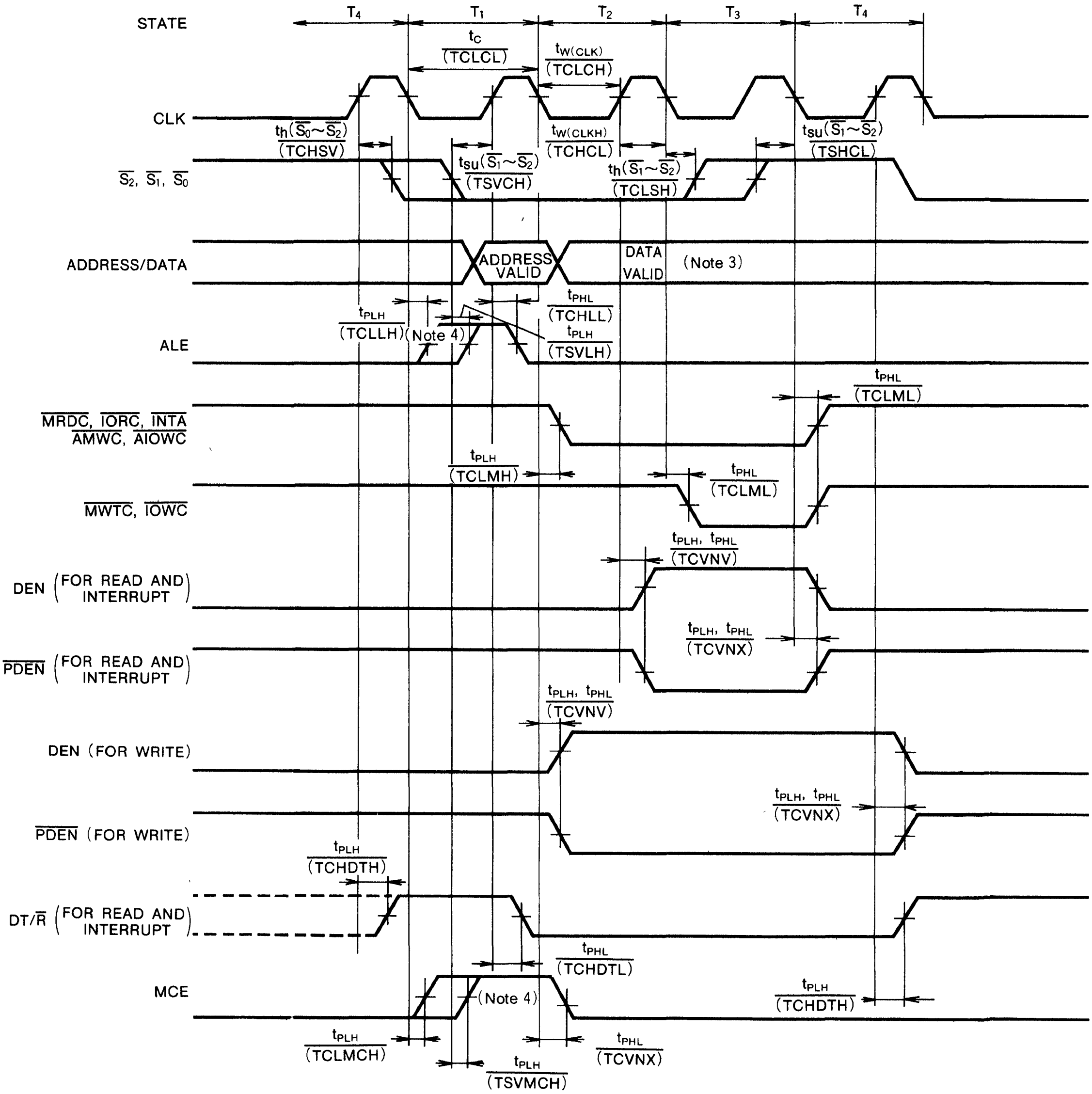
Symbol	Parameter	Alternate symbol	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output	TCVNV		5		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{\text{PDEN}}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output	TCVNX		10		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{\text{PDEN}}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to ALE output	TCLLH				20	ns
t_{PLH}	Output low-level to high-level propagaion time From CLK input to MCE output	TCLMCH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to ALE output	TSVLH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to MCE output	TSVMCH				20	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to ALE output	TCHLL		4		15	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$, and $\overline{\text{IOWC}}$ outputs	TCLML		10		35	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$, and $\overline{\text{IOWC}}$ outputs	TCLMH		10		35	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to DT/$\overline{\text{R}}$ output	TCHDTL	(Note 1)			50	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to DT/$\overline{\text{R}}$ output	TCHDTH				30	ns
t_{PZH}	High-level output enable time From $\overline{\text{AEN}}$ input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$, and $\overline{\text{IOWC}}$ outputs	TAELCH				40	ns
t_{PHZ}	High-level output disable time From $\overline{\text{AEN}}$ input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$, and $\overline{\text{IOWC}}$ outputs	TAEHCZ				40	ns
t_{PHL}	Output high-level to low-level propagation time From $\overline{\text{AEN}}$ input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$, and $\overline{\text{IOWC}}$ outputs	TAELCV		115		200	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From $\overline{\text{AEN}}$ input to DEN output	TAEVNV				20	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From CEN input to $\overline{\text{DEN}}$ and PDEN outputs	TCEVNV				25	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time. From CEN input to $\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, $\overline{\text{INTA}}$, $\overline{\text{AMWC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AIOWC}}$ and $\overline{\text{IOWC}}$ outputs	TCELRH				35	ns

TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_C	Clock CLK cycle time	TCLCL		100			ns
$t_{W(CLKL)}$	Clock CLK low pulse width	TCLCH		50			ns
$t_{W(CLKH)}$	Clock CLK high pulse width	TCHCL		30			ns
$t_{SU(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_1 state	TSVCH		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_4 state	TCHSV		10			ns
$t_{SU(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_3 state	TSHCL		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_3 state	TCLSH		10			ns

TIMING DIAGRAM

1. Command output timing



Note 3 : The address/data bus signals are shown only for reference
4 : The ALE and MCE leading edge occurs in synchronization with the falling edge of CLK or $\overline{S_0}$~$\overline{S_2}$, whichever is later
5 : Unless otherwise noted, the timing of all signals is respect to 1.5V

DESCRIPTION

The M5L8289P is a system bus (®MULTIBUS) arbiter for the MELPS 86, 88 16-bit microprocessors. When a request for access to the system bus is made by any of these microprocessors, the M5L8289P prevents simultaneous access by two or more processors by allowing only the first processor which requests access to access the system, preventing all others from accessing the system bus. It generates the required signals for bus access. (®MULTIBUS is a registered trademark of Intel Corporation.)

FEATURES

- ®MULTIBUS compatible
- Usable in multiprocessing systems using the MELPS 86, 88 microprocessors
- Four modes of request and bus surrender are possible
- Low power dissipation

APPLICATION

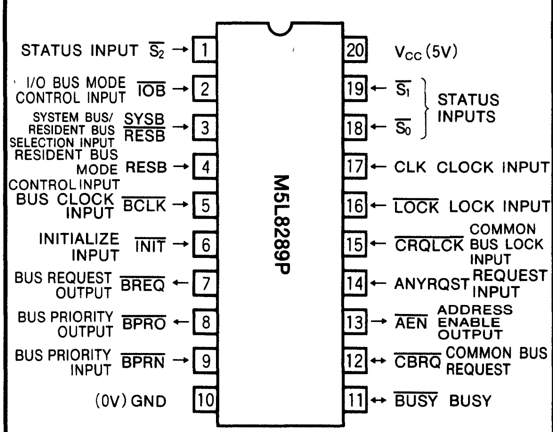
Bus arbitration for MULTIBUS boards using the MELPS 86, 88 or 8089

FUNCTION

The M5L8289P is a bus arbiter for ®MULTIBUS boards using the MELPS 86, 88 microprocessors. When several processors are connected to the system bus (®MULTIBUS), it is necessary to prevent two or more processors from attempting to access the system bus simultaneously.

This function is performed by the M5L8289P, which decodes the processor status, and if access to the system bus is required, prevents other processors from attempting system bus access by generating the required control signals.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM

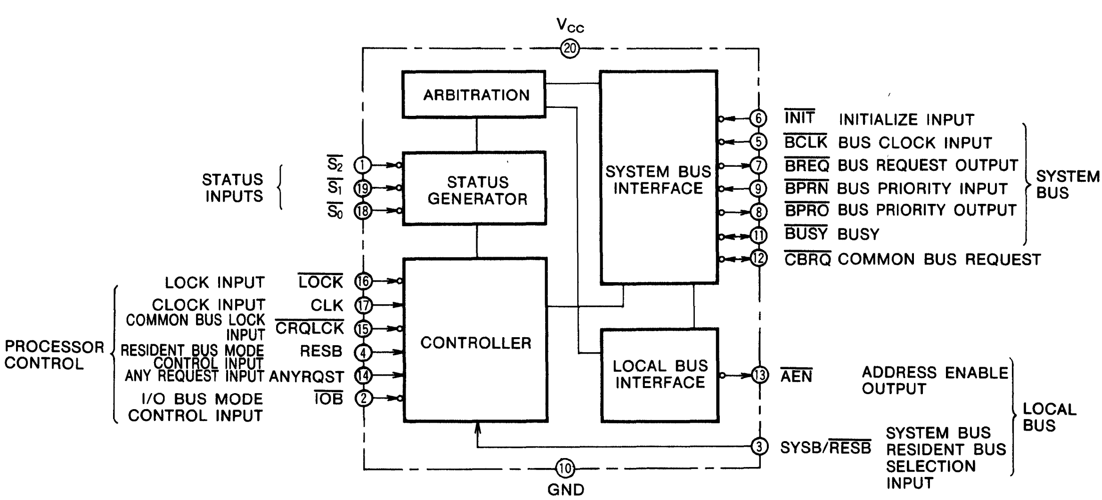


Table 1 M5M8289P Modes and Bus Request and surrender Conditions

Status		I/O Bus mode only	Resident bus mode only		I/O Bus mode resident bus mode		Single bus mode
		$\overline{IOB}$=L RESB=L	$\overline{IOB}$=H RESB=H		$\overline{IOB}$=L RESB=H		$\overline{IOB}$=H RESB=L
Command	$\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$		SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=H	SYSB/$\overline{RESB}$=L	
Interrupt acknowledge	0 0 0	×	○	×	×	×	○
I/O Port read	0 0 1	×	○	×	×	×	○
I/O Write	0 1 0	×	○	×	×	×	○
Halt	0 1 1	×	×	×	×	×	×
Instruction fetch	1 0 0	○	○	×	○	×	○
Memory read	1 0 1	○	○	×	○	×	○
Memory write	1 1 0	○	○	×	○	×	○
Passive cycle	1 1 1	×	×	×	×	×	×

○ …… A request signal is output by the system bus.
× …… The system bus privileges are surrendered

Mode	Input		Bus request condition (excluding halt and passive cycles)	Bus surrender condition (Note 1)
	$\overline{IOB}$	RESB		
Single bus mode	H	L	All bus access states	HLT+(TI-CBRQ)+HPBRQ
Resident bus mode only	H	H	(SYSB/$\overline{RESB}$=high)·(Bus access state)	((SYSB/$\overline{RESB}$=L+T1)·CBRQ) +HLT+HPBRQ
I/O Bus mode only	L	L	All memory access states	(I/O Access state+T1)·CBRQ)+HLT +HPERQ
I/O Bus mode resident bus mode	L	H	(SYSB/$\overline{RESB}$=high)·(Memory access states)	((I/O Access state +(SYSB/$\overline{RESB}$=low))· CBRQ + HPBRQ HLT +HPBRQ

Note 1 : When $\overline{LOCK}$=low, the bus is not released under any circumstances.
When $\overline{CRQLCK}$=low, the bus is not released even when low-priority arbiters request it
2 : HLT············Halt state
TI···············Idle (passive) state
CBRQ·········$\overline{CBRQ}$=low
HPBRQ ······Indicates that a high-priority arbiter is requesting the bus ($\overline{BPRN}$=high)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~7	V
V_I	Input voltage		−1~5.5	V
V_O	Output voltage		−0.5~7	V
T_{opr}	Operating temperature		0~75	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter			Limits Min	Limits Nom	Limits Max	Unit
V_{CC}	Supply voltage			4.5	5	5.5	V
I_{OH}	High-level output current	$\overline{BUSY}$, $\overline{CBRQ}$,	V_{OH}≧2.4V	Open collector			μA
		Other output,	V_{OH}≧2.4V	0		400	
I_{OL}	Low-level output current	$\overline{BUSY}$, $\overline{CBRQ}$,	V_{OL}≦0.45V	0		20	mA
		$\overline{AEN}$	V_{OL}≦0.45V	0		16	
		$\overline{BPRO}$, $\overline{BREQ}$,	V_{OL}≦0.45V	0		10	

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, V_{CC}=5V±10%, unless otherwise noted)

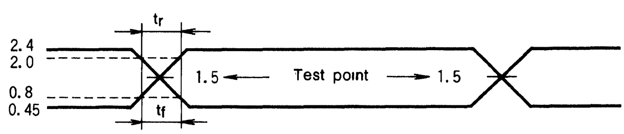
Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{OL}	Low-level output voltage	$\overline{BUSY}$, $\overline{CBRQ}$	I_{OL}=20mA			0.45	V
		$\overline{AEN}$	I_{OL}=16mA			0.45	
		$\overline{BPRO}$, $\overline{BREQ}$	I_{OL}=10mA			0.45	
V_{OH}	High-level output voltage	$\overline{BUSY}$, $\overline{CBRQ}$		Open collector			V
		$\overline{AEN}$, $\overline{BPRO}$, $\overline{BREQ}$	I_{OH}=400μA	2.4			
V_{IC}	Input clamp voltage		V_{CC}=4.50V, I_C=−5mA			−1	V
I_{IL}	Low-level input current		V_{CC}=5.50V, V_F=0.45V			−0.5	mA
I_{IH}	High-level input current		V_{CC}=5.50V, V_R=5.50V			60	μA
I_{CC}	Supply current					120	mA
C_{IN}	Input capcitance	Status	f=1MHz, V_{B2AS}=2.5V			25	pF
		Others				12	

SWITCHING CHARACTERISTICS (T_a=0~75℃, V_{CC}±5V±5%, unless otherwise noted)

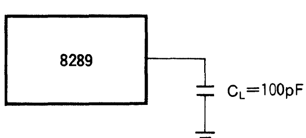
Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PHL(\overline{BREQ})}$	$\overline{\text{BCLK}}$→$\overline{\text{BREQ}}$ ↑, ↓ Delay time	t_{BLBRL}				35	ns
$t_{PLH(\overline{BPRO})}$	$\overline{\text{BCLK}}$→$\overline{\text{BPRO}}$ ↑, ↓ Delay time (See note 2)	t_{BLPOH}				40	ns
$t_{PHL(\overline{BPRO})}$	$\overline{\text{BPRN}}$ ↑, ↓→$\overline{\text{BPRO}}$ ↑ ↓ Delay time (See note 2)	t_{PNPO}				25	ns
$t_{PHL(\overline{BUSY})}$	$\overline{\text{BCLK}}$→$\overline{\text{BUSY}}$ ↓ Delay time	t_{BLBYL}				60	ns
$t_{PLZ(\overline{BUSY})}$	$\overline{\text{BCLK}}$→$\overline{\text{BUSY}}$ Float time (See note 3)	t_{BLBYH}				35	ns
$t_{PLH(\overline{AEN})}$	CLK→$\overline{\text{AEN}}$, ↑ Delay time	t_{CLAEH}				65	ns
$t_{PHL(\overline{AEN})}$	$\overline{\text{BCLK}}$→$\overline{\text{AEN}}$, ↓ Delay time	t_{BLAEL}				40	ns
$t_{PHL(\overline{CBRQ})}$	$\overline{\text{BCLK}}$→$\overline{\text{CBRQ}}$, ↓ Delay time	t_{BLCBL}				60	ns
$t_{PLZ(\overline{CBRQ})}$	$\overline{\text{BCLK}}$→$\overline{\text{CBRQ}}$ Delay time (See note 3)	t_{BLCBH}				35	ns
t_r	Output rise time	t_{OLOH}	0.8V~2.0V			20	ns
t_f	Output fall time (See note 4, 5)	t_{OHOL}	2.0V~0.8V			12	ns

Note 1 : Symbol ↑, ↓ means rise signal and fall signal.
2 : $\overline{\text{BCLK}}$ generate the first $\overline{\text{BPRO}}$ and then BPRO changes lower in the chain are generated through BPRN.
3 : Measured at 0.5V above GND

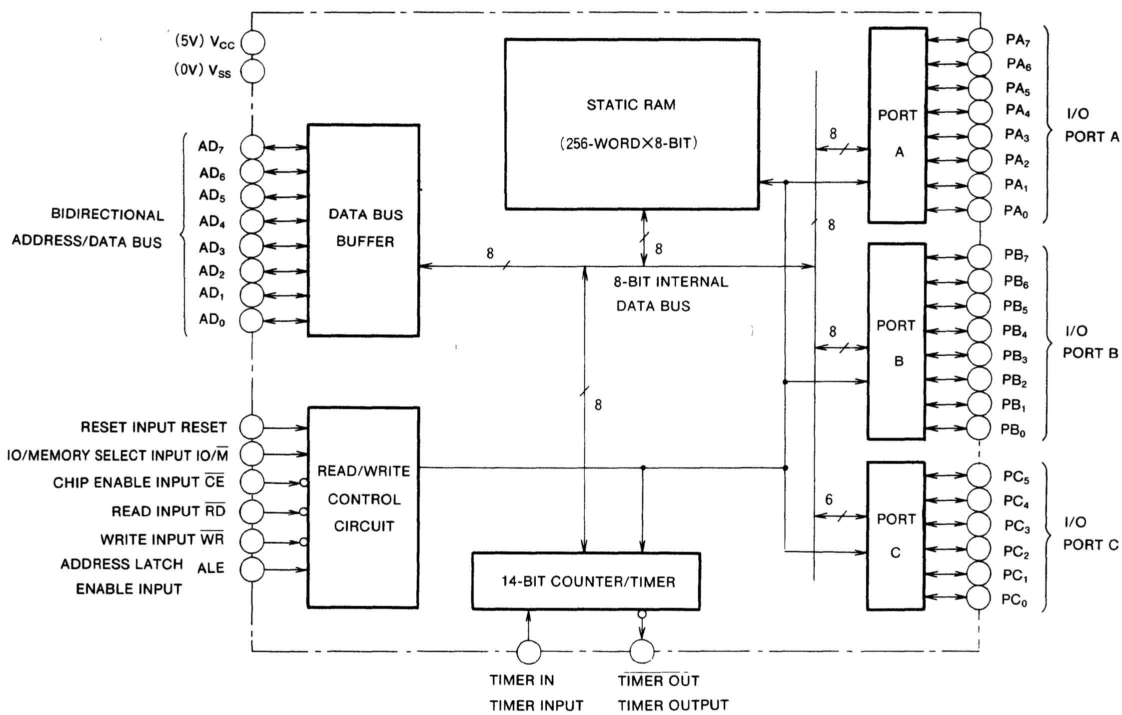
Note 4 A.C. test wave form.



Note 5 · Load circuit



BLOCK DIAGRAM



Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function	
0	INTR A	PORT A INTERRUPT REQUEST	
1	A BF	PORT A BUFFER FULL FLAG	
2	INTE A	PORT A INTERRUPT ENABLE	
3	INTR B	PORT B INTERRUPT REQUEST	
4	B BF	PORT B BUFFER FULL FLAG	
5	INTE B	PORT B INTERRUPT ENABLE	
6	TIMER	COUNTER/TIMER INTERRUPT	(This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used	

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read.

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal $PA_0 \sim PA_7$.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals $PB_0 \sim PB_7$.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals $PC_0 \sim PC_5$. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State / Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{B\ STB}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{A\ STB}$ (port A strobe)	$\overline{A\ STB}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1: Timer mode T_{13}~T_8 The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.
The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in mode 0 and mode 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RAM Hold Mode at Low Voltage (Power Down Mode)

Power down mode starts when the ALE input is fixed at low-level and other inputs at high or low-level after high-level of $\overline{CE}$ input in M5M81C55P-2 is latched by the falling edge of the ALE input.
The contents of RAM are not affected, even if V_{CC} falls into 2 V in power down mode.

RESET

The M5M81C55P-2 is reset by 400ns(min) pulse input on RESET pin.
By reset, all 3 ports are set to input mode. And counter/timer stops but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃ unless otherwise noted)

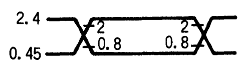
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

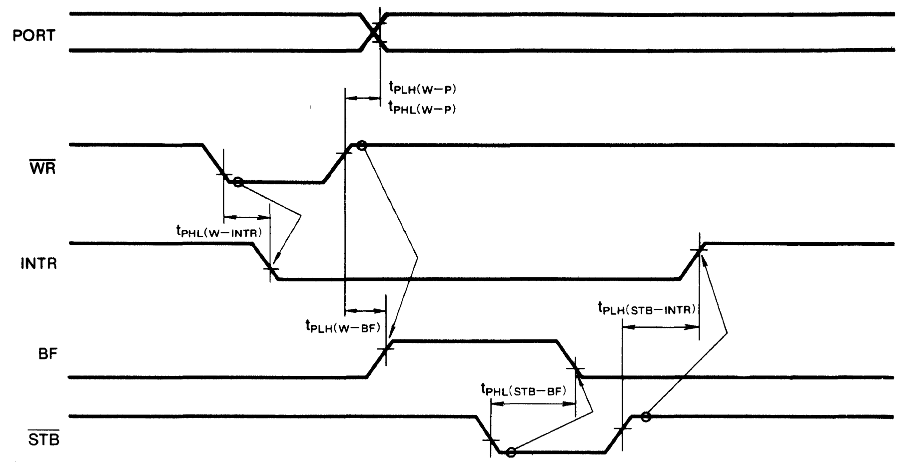
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			120	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				330	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		80	ns
$t_{PHL(W-P)}$ $t_{PLH(W-P)}$	Propagation time from write to data output				300	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				300	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				300	ns
$t_{PHL(\phi-OUT)}$ $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				300	ns

Note 6 : Test conditions are not applied.
7 : A.C Testing waveform

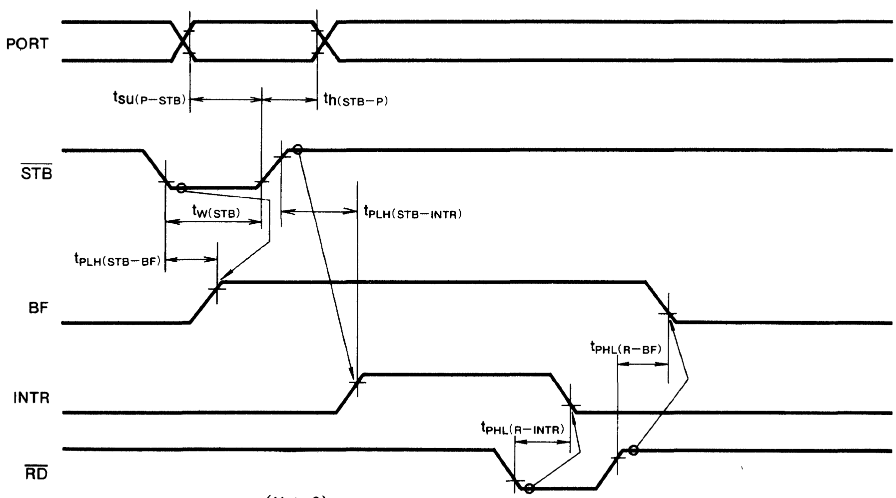
Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



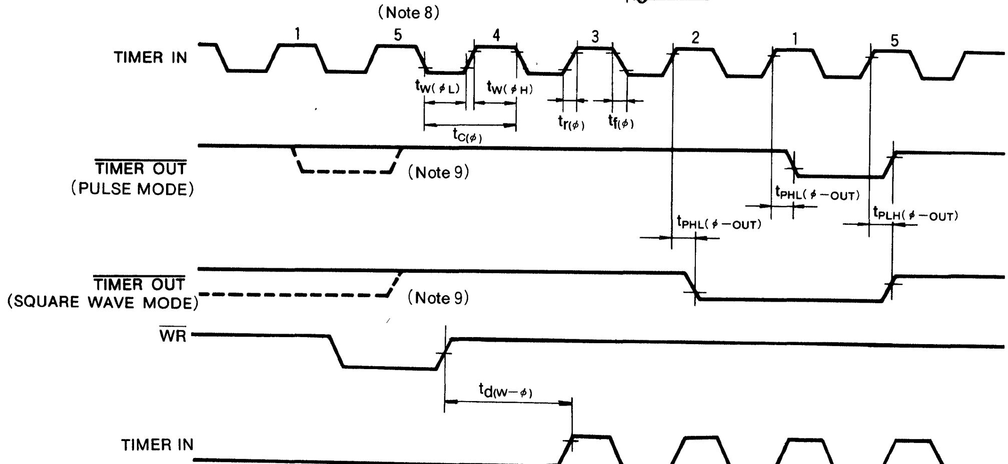
Strobed output



Strobed input

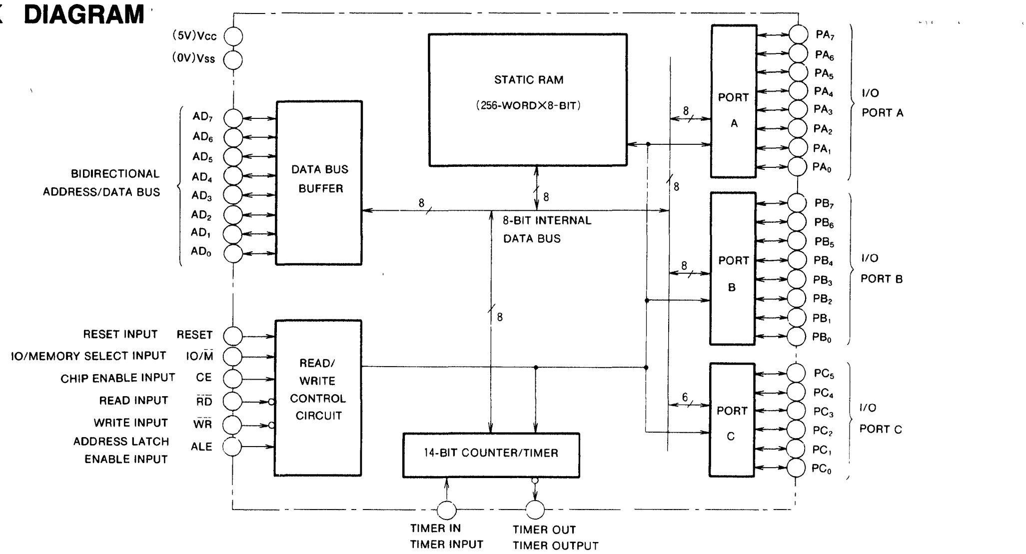


Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1.
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

BLOCK DIAGRAM



Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT (This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read)
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal $PA_0 \sim PA_7$.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals $PB_0 \sim PB_7$.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals $PC_0 \sim PC_5$. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State / Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	$\overline{\text{B STB}}$ (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1: Timer mode $T_{13}\sim T_8$: The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.
The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating 2n+1 count down in mode 0 and mode 1, a high-level signal is output during the former n+1 counting and a low-level signal is output during the later n counting.

RAM Hold Mode at Low Voltage (Power Down Mode)

Power down mode starts when the ALE input is fixed at low-level and other inputs at high or low-level after low-level of CE input in M5M81C56P-2 is latched by the falling edge of the ALE input.
The contents of RAM are not affected, even if V_{CC} falls into 2 V in power down mode.

RESET

The M5M81C56P-2 is reset by 400ns(min) pulse input on RESET pin.
By reset, all 3 ports are set to input mode. And counter/timer stops but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	2.5	mA
T_{opr}	Operating free-air temperature		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

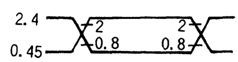
RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

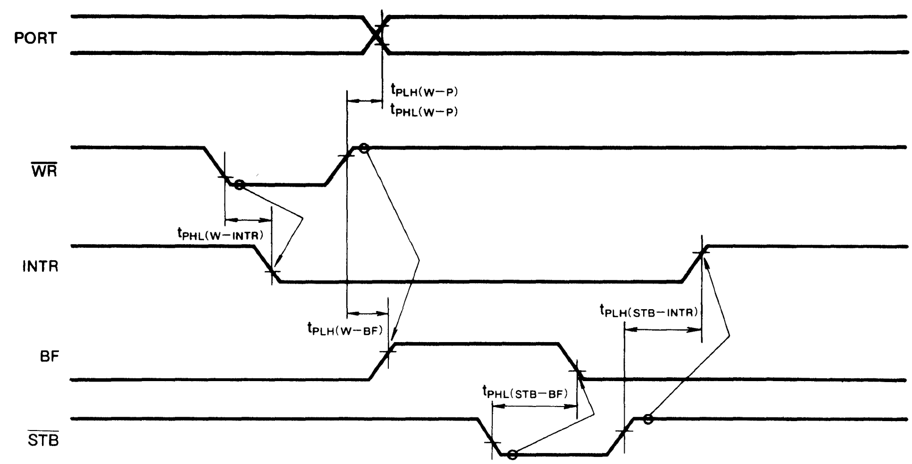
SWITCHING CHARACTERISTICS (Ta=−20~75℃, V_{CC}= 5 V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			120	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				330	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		80	ns
$t_{PHL(W-P)}$ $t_{PLH(W-P)}$	Propagation time from write to data output				300	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				300	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				300	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				300	ns
$t_{PHL(\phi-OUT)}$ $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				300	ns

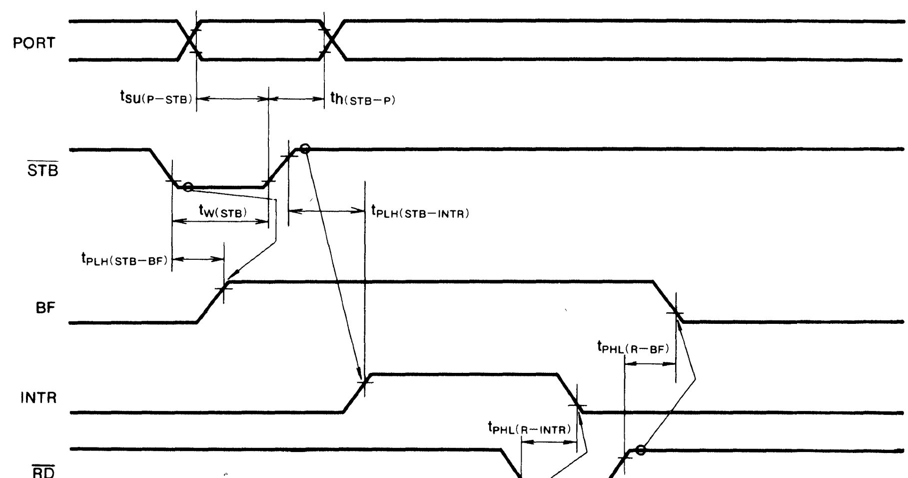
Note 6 : Test conditions are not applied
7 : A C Testing waveform
Input pulse level 0.45~2.4V
Input pulse rise time 10ns
Input pulse fall time 10ns
Reference level input V_{IH}=2V, V_{IL}=0.8V
output V_{OH}=2V, V_{OL}=0.8V



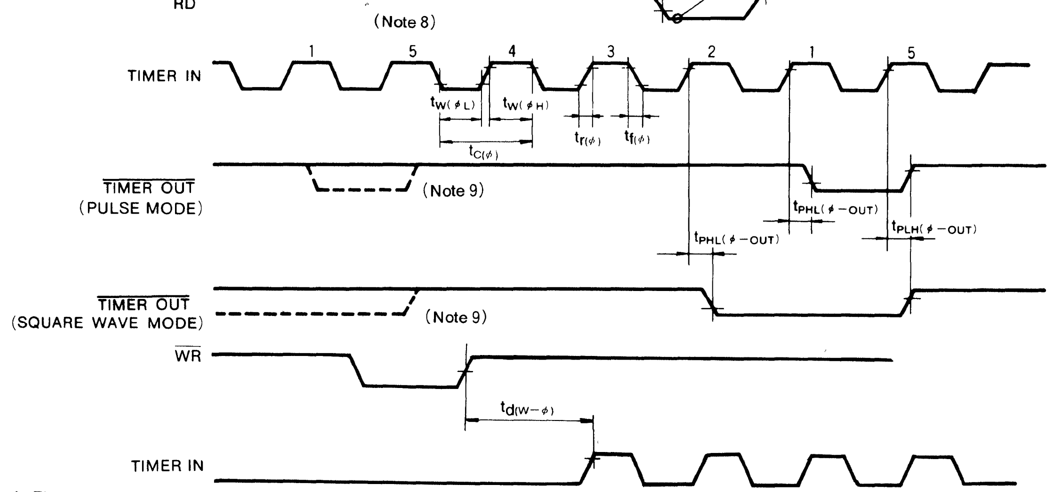
Strobed output



Strobed input

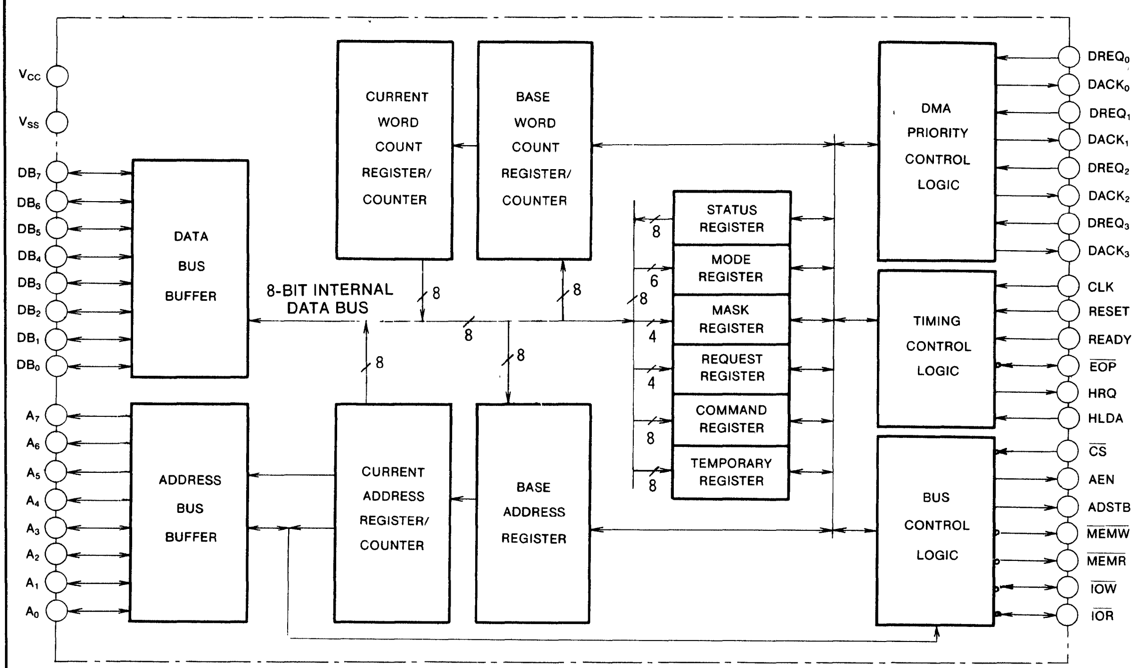


Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

BLOCK DIAGRAM



ADSTB output (address strobe output)

This pin outputs a high-level pulse when the higher 8 bits of the transfer address is output through data bus at the DMA operation. This pulse is used as the strobe pulse for the external address latch circuit.

In non-DMA mode or in cascade mode DMA this output remains low-level.

AEN output (address enable output)

AEN is an output which denotes that the bus control signal address output etc. from the M5M82C37AP-5 are valid. When AEN output is high-level, they are valid output, so AEN is used as a control input for an external three-state bus buffer.

HRQ output (hold request output)

This output denotes that the M5M82C37AP-5 requests the use of the bus to the CPU. The M5M82C37AP-5 sets HRQ high in response to the DMA request.

$\overline{CS}$ input (chip select input)

This input is a chip select signal which is set to low-level when the CPU reads or writes data to the M5M82C37AP-5. When HLDA is high-level, this input is masked and the M5M82C37AP-5 is not selected.

CLK input (clock input)

The master clock for the M5M82C37AP-5 is input.

RESET input (reset input)

When a high-level pulse is input from RESET, the M5M82C37AP-5 is set to the initial state.

DACK0, DACK1, DACK2, DACK3 output (DMA acknowledge output)

DMA acknowledge is the signals which shows a peripheral device whether DMA operaiton for its channel is under execution.

By resetting, they become active low outputs, but they can be mode into active high outputs by altering the contents of the command register.

DREQ0, DREQ1, DREQ2, DREQ3 input (DMA request input)

DREQ is an input which shows that a peripheral device requests DMA service. By resetting, they become active high inputs but they can be made into active low inputs by altering the contents of the command register. DREQ should keep in active until the DACK output returns.

V_{SS}

V_{SS} is connected to system ground.

$DB_7 \sim DB_0$ inputs/outputs (data bus inputs/outputs)

In non-DMA mode, the contents of the registers of the M5M82C37AP-5 are read out or written through $DB_7 \sim DB_0$.

In DMA mode, the higher 8 bits of the transfer address are output through $DB_7 \sim DB_0$ in the S_1 state. In the memory to memory DMA mode, data to be transferred between memories via the temporary register are read and written by the M5M82C37AP-5 through $DB_7 \sim DB_0$.

V_{CC}

The 5V power supply is connected through V_{CC}.

$A_7 \sim A_4$ output, $A_3 \sim A_0$ input/output (address output, address input/output)

In the DMA mode, the lower 8 bits of the transfer address are output through $A_7 \sim A_0$.

In cascade mode DMA, they become high-impedance. In the non-DMA mode, $A_3 \sim A_0$ become register select address inputs, while $A_7 \sim A_4$ become high-impedance.

$\overline{EOP}$ input/output (end of process input/output)

$\overline{EOP}$ is an N-channel open drain input/output. When the word count register reaches count-up, a low-level pulse is output from $\overline{EOP}$. (This is called internal $\overline{EOP}$.) $\overline{EOP}$ may be pulled down to low-level. If $\overline{EOP}$ is pulled down during DMA operation, the DMA operation is forcibly terminated. (This is called external $\overline{EOP}$.)

Note : In cascade mode DMA, the $\overline{EOP}$ pulse is not output, and external $\overline{EOP}$ cannot terminate cascade mode DMA operation

Notes for memory-to-memory transfer

Observe the following points when programming memory-to-memory DMA.

- The contents of the word count register of channel 0 and 1 must be programmed identically.
- The transfer mode of channel 0 and 1 must be set to the block transfer mode.
- All the mask bits must be set to inhibit external DMA request input. (Memory-to-memory DMA is started by software DMA request to channel 0.)
- In memory-to-memory DMA operation, all the DACK outputs are inactive. (but AEN is set during transfer.)

PRIORITY

Two kinds of DMA priority can be programmed for the M5M82C37AP-5. (Command register bit 4) If plural channels request DMA at the same time, DMA is acknowledged for the channel which has the highest priority. (Table 1)

(1) Fixed Priority (bit 4=0)
The DMA channel which has the highest priority is channel 0. Channel 1 has the second, channel 2 has the third and channel 3 has the lowest priority.

(2) Rotating Priority (bit 4=1)
This priority mode is that the channel which has serviced the DMA request, has the lowest priority at the next DMA operation. (Just after reset the lowest priority channel is channel 3)
For example, just after channel 1 DMA is executed, channel 2 has the highest priority, channel 3 has the second highest, channel 0 has the third and channel 1 has the lowest priority.

Table 1 DMA priority for the M5M82C37AP-5

Priority type	DMA channel serviced	DMA priority for next transfer			
		Highest	2nd	3rd	Lowest
Fixed priority	————	ch0	ch1	ch2	ch3
Rotating priority	ch0	ch1	ch2	ch3	ch0
	ch1	ch2	ch3	ch0	ch1
	ch2	ch3	ch0	ch1	ch2
	ch3	ch0	ch1	ch2	ch3

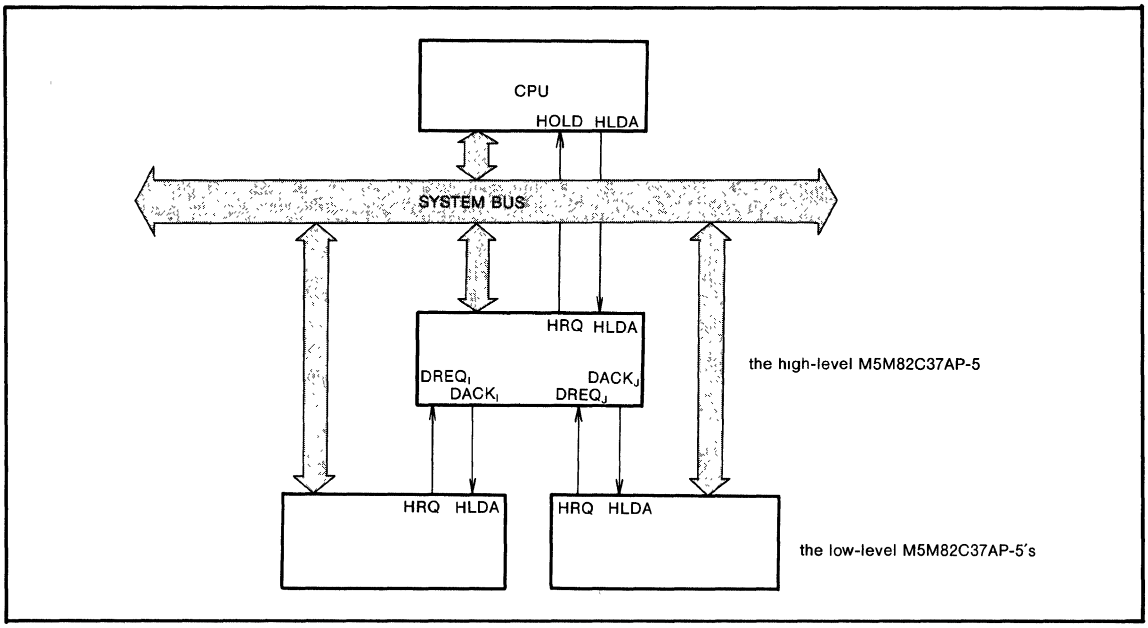


Fig.1 Example of a DMA system using a cascade connection

(5) **Auto initialization feature (mode regsiter bit 4=1)**
When bit 4 of the mode register is set to 1, the programmed channel enters the auto initialization mode. Auto initialization is performed when TC occurs and the contents of the base address/word count registers are loaded in the current address/word count registers. (The contents of the base address/word count registers are programmed to the same value as the current registers, at the same time.)

Note : If a channel is programmed for auto initialization the mask register bit for that channel is not set after TC. If it is not programmed for auto initialization, the mask register bit is set after TC, so the mask register bit must be reset to set this channel to DMA-enable

(6) **Extended write feafure (command register bit 5=1)**
In normal DMA operation, the write pulse $\overline{MEMW}$ (or $\overline{IOW}$) falls down to low-level in the S_3 state. But, if extended write is programmed, the write pulse falls at the S_2 state and the width can be extended for one clock period.

(7) **Compressed timing DMA feafure (command register bit 3=1)**
In normal DMA, the transfer for one word consists of three or four states.
If the compressed timing DMA is programmed, the S_3 state is not executed and the one word transfer consists of two or three states. In this mode, the write output ($\overline{IOW}$, $\overline{MEMW}$) falls to low-level in the S_2 state as well as the read output ($\overline{IOR}$, $\overline{MEMR}$). In memory-to-memory DMA operation, the compressed timing assignment is ignored.

REGISTERS

The following is a description of the registers of M5M82C37AP-5.

(1) **Address registers**
The M5M82C37AP-5 has two 16-bit address registers for each DMA channel.
One is called the current address register. It holds the contents of the memory address at which DMA operation is performed and the contents are incremented (or decremented) at every word transfer. This register is read/write enabled when in the inactive state. The other is the base address register. This register is a write-only register and is written at the same time the current address register is programmed. The contents of the base address register are loaded into the current address register when the channel has reached TC if the channel is programmed in the auto initialize mode.
The registers of the M5M82C37AP-5 are read or written through an 8-bit data bus so the address register must be accessed twice, first the lower 8 bits, second the higher 8 bits. The M5M82C37AP-5 has a first/last flip-flop which is toggled when the 16-bit regsiter is accessed. It selects the lower or higher byte.

(2) **Word count registers**
The M5M82C37AP-5 has two 16-bit word count registers for each DMA channel.
One is called the current word count register. It holds the number of DMA transfer words, and the contents are decremented at the end of every word transfer. TC

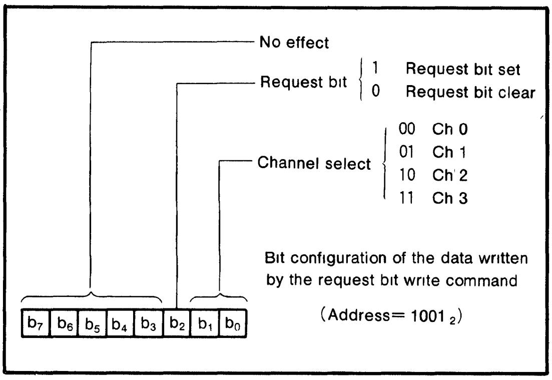


Fig.6 Request register

Note : All the request bits are reset after the DMA operation of one channel So, when the DMA is started by software request, other external DMA requests must be masked by setting all the mask register bits (Software requests are not masked by the mask register) All the request bits are set to 0 after reset.

(7) **Status register**

This register is an 8-bit read only register. The 4 MSBs show the status of the four DREQs. 1 means that the DREQ input is active.

The other 4 bits are the TC bits which are set to 1 when TC occurs. The lower 4 bits are reset after the status registers are read or after reset.

The relation between these bits and the channels is shown in fig. 7.

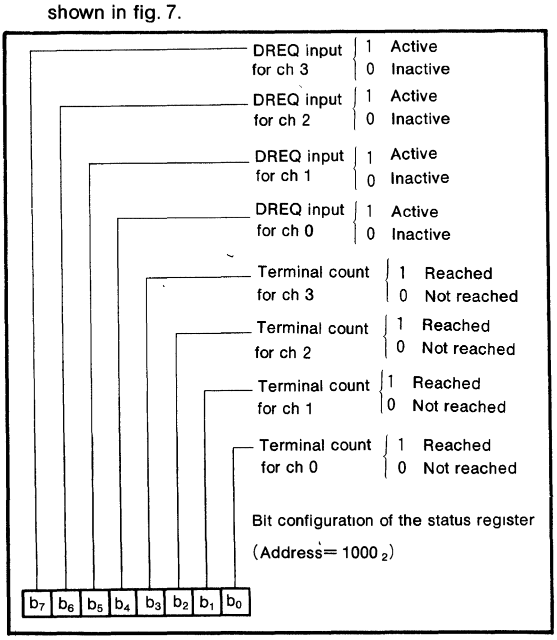


Fig.7 Status register

(8) **Temporary Register**

This register is an 8-bit read only register.

It is used to store temporary data read during the first part of the memory-to-memory DMA operation.

When the CPU reads this register, the register contents are the data which were transfered in memory-to-memory transfer DMA immediately prior to the CPU read.

PROGRAMMING

The registers in the M5M82C37AP-5 can be read or written when $\overline{CS}$ and HLDA inputs are low-level.

The address assignment is shown in Tables 2 and 3 Some of the write operations in these figures do not, in fact, write in any registers. They are called software commands. The following is a description of the software commands.

Clear first/last F/F

In reading or writing a 16-bit register, the higher and lower 8 bits are accessed separately. Selection is done by a first/last flip-flop which toggles when ever one of the 16-bit registers is accessed. This command clears the first/last flip-flop, so after this command is executed, the next access of the 16-bit register is begins at the lower 8 bits.

Master clear

This command executes a software reset.

Note : The following are the effects of the software reset for the M5M82C37AP-5

- Mask bits are set for all the DMA channels
- The command register is cleared to 00_{16} (Note that bit 2 is 0)
- The temporary register is cleared.
- The 4 TC bits of the status register are cleared
- The first/last flip-flop is reset.
- Software DMA request bits are cleared.

(When the hardware reset is performed, together with the above effects, DMA operation is terminated and the M5M82C37AP-5 returns to the S_I state.)

Clear mask register

This command clears all the mask bits and enable DMA for all the channels.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3〜7	V
V_I	Input voltage		−0.3〜V_{CC}+0.3	V
V_O	Output voltage		−0.3〜V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
Topr	Operating free-air temperature range		−20〜75	℃
Tstg	Storage temperature		−65〜150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20〜75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage(GND)		0		V

ELECTRICAL CHARCTERISTICS (T_a=−20〜75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
		I_{OH}=−20μA	4.4			
		I_{OH}=−100μA(HRQ only)	3.3			
V_{OL}	Low-level output voltage	I_{OL}=2.0mA(data bus) I_{OL}=3.2mA(other outputs)			0.45	V
I_I	Input current	V_I=0V, V_{CC}	−10		+10	μA
I_{OZ}	Off-state output current	V_O=0V〜V_{CC}	−10		+10	μA
I_{CC}	Supply current from V_{CC} (operating)	V_I=0V, V_{CC}, f_{CLK}=1/t_C(φ)min.			15	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA
C_i	Input terminal capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{i/o}$	Input/output terminal capacitance	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

SWITCHING CHARACTERISTIC (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

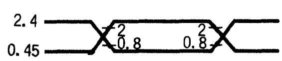
1. SLAVE MODE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Data enable time after read	C_L=150pF			140	ns
$t_{PVZ(R-DQ)}$	Data disable time after read		0		70	ns
$t_{PZV(A-DQ)}$	Address access time				250	ns

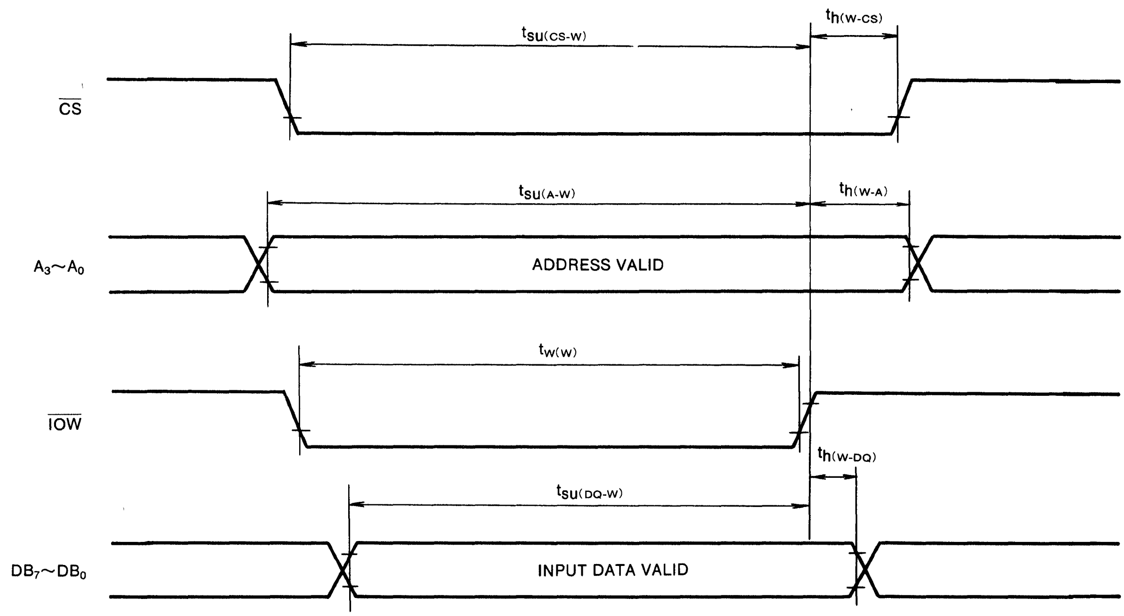
2. DMA MODE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN	C_L=150pF			200	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN				130	ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active				170	ns
$t_{PHL(\phi-A)}$	Propagation time from clock to address stable				170	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating				90	ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data bus				200	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data bus				170	ns
$t_{PLH(\phi-ADSTB)}$	Propagation time from clock to ADSTB				130	ns
$t_{PHL(\phi-ADSTB)}$	Propagation time from clock to ADSTB				90	ns
$t_{SU(DQ-ADSTB)}$	Data output setup time before ADSTB		100			ns
$t_{h(ADSTB-DQ)}$	Data output hold time before ADSTB		30			ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read or write active				150	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$	Propagation time from clock to read or write				190	ns
$t_{PLH(\phi-R)}$	Propagation time from clock to read				190	ns
$t_{PLH(\phi-W)}$	Propagation time from clock to write				130	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read or write floating				120	ns
$t_{h(R-A)}$	Address output hold time after read		$t_{C(\phi)}-100$			ns
$t_{h(W-A)}$	Address output hold time after write		$t_{C(\phi)}-50$			ns
$t_{SU(DQ-MEMW)}$	Data output setup time before $\overline{MEMW}$		125			ns
$t_{h(MEMW-DQ)}$	Data output hold time after $\overline{MEMW}$		10			ns
$t_{PHL(\phi-DACK)}$ $t_{PLH(\phi-DACK)}$	Propagation time from clock to DACK				170	ns
$t_{PHL(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$				170	ns
$t_{PLH(\phi-EOP)}$	Propagation time from clcok to $\overline{EOP}$				170	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ				120	ns

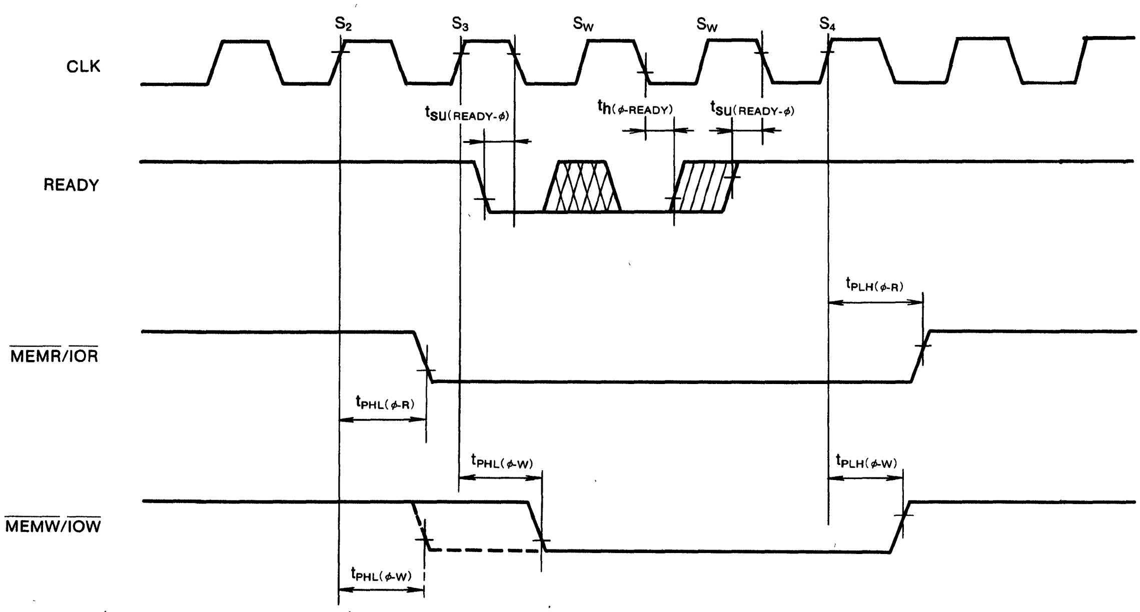
Note : A.C Testing waveform
Input pulse level 0.45~2.4V
Input pulse rise time 10ns
Input pulse fall time 10ns
Reference level input V_{IH}=2V, V_{IL}=0.8V
output V_{OH}=2V, V_{OL}=0.8V



Slave mode timing (WRITE)

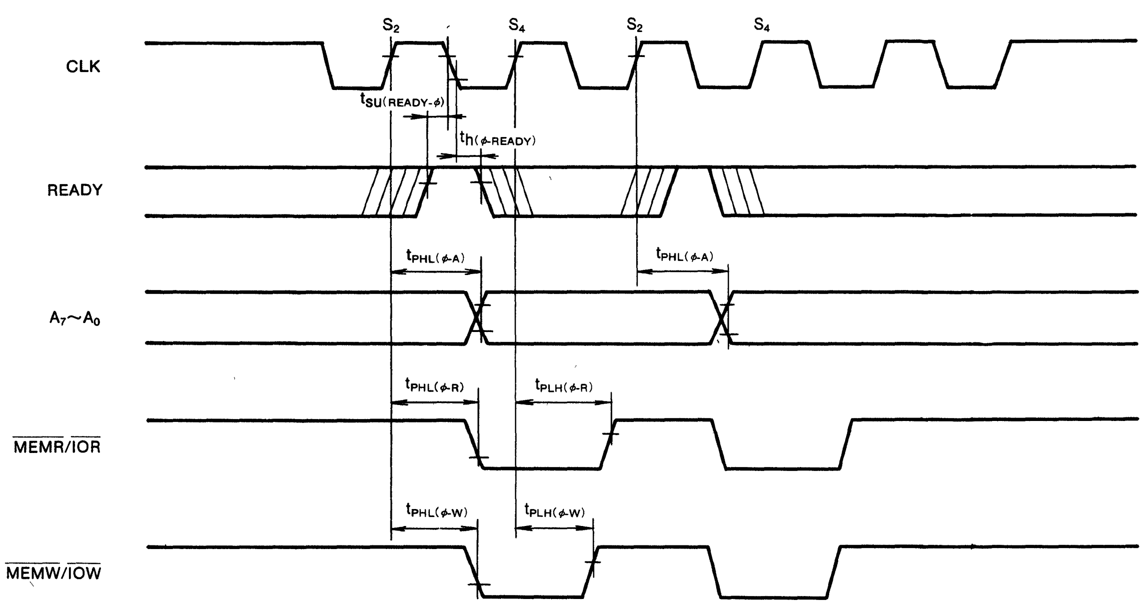


READY input timing



(——— signifies expansion write)

Compressed timing



M5M82C51AP/FP/J

CMOS PROGRAMMABLE COMMUNICATION INTERFACE

DESCRIPTION

The M5M82C51AP is a universal synchronous/asynchronous receiver/transmitter (USART) IC chip designed for data communications use. It is produced using the silicon-gate CMOS process and is mainly used in combination with 8-bit microprocessors. It is housed in a 28-pin plastic molded DIP.

And preparatory for surface equipment M5M82C51AFP (SOP) and M5M82C51AJ(PLCC).

FEATURES

- Single 5V supply voltage
- TTL compatible
- Synchronous and asynchronous operation
  - Synchronous:
    - 5~8-bit characters
    - Internal or external synchronization
    - Automatic SYNC character insertion
  - Asynchronous system:
    - 5~8-bit characters
    - Clock rate— 1 , 16 or 64 times the baud rate
    - 1 , 1½, or 2 stop bits
    - False-start-bit detection
    - Automatic break-state detection
- Baud rate: DC~64K-baud
- Full duplex, double-buffered transmitter/receiver
- Error detection: parity, overrun, and framing

APPLICATION

Modem control of data communications using microcomputers

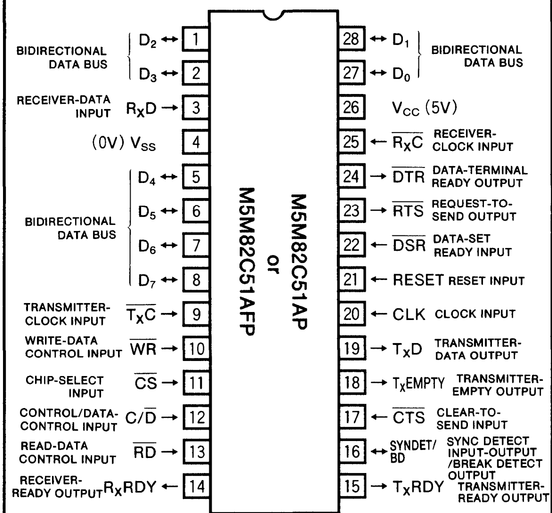
Control of CRT, TTY and other terminal equipment

FUNCTION

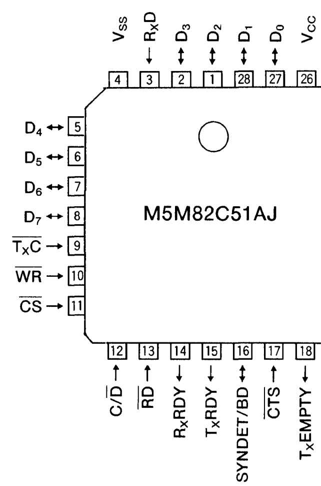
The M5M82C51AP is used in the peripheral circuits of a CPU. It permits assignments, by means of software, of operations in all the currently used serial-data transfer systems.

The M5M82C51AP receives parallel-format data from the CPU, converts it into a serial format, and then transmits via the T_XD pin. It also receives data sent in via the R_XD pin from the external circuit, and converts it into a parallel format for sending to the CPU. On receipt of parallel-format data for transmission from the CPU or serial data for the CPU from external devices, the M5M82C51AP informs the CPU using the T_XRDY or R_XRDY pin. In addition, the CPU can read the M5M82C51AP status at any time. The M5M82C51AP can detect the data received for errors and inform the CPU of the presence of errors as status information. Errors include parity, overrun and frame errors.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (M5M82C51AP)
28P2W (M5M82C51AFP)



Outline 28P0

OPERATION

The M5M82C51AP interfaces with the system bus as shown in Fig.1, positioned between the CPU and the modem or terminal equipment, and offers all the functions required for data communication.

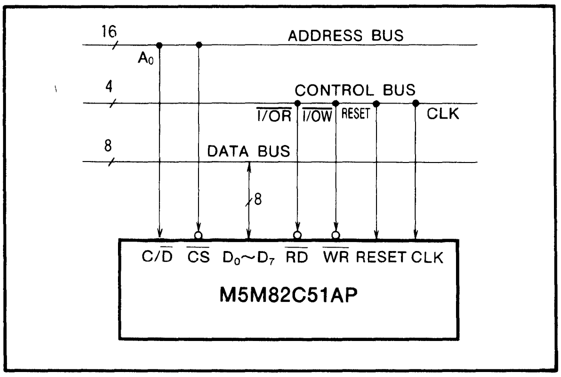


Fig. 1 M5M82C51AP interface to CPU system bus

When using the M5M82C51AP, it is necessary to program, as the initial setting, assignments for synchronous/asynchronous mode selection, baud rate, character length, parity check, and even/odd parity selection in accordance with the communication system used. Once programming is completed, functions appropriate to the communication system can be carried out continuously.

When initial setting of the USART is completed, data communication becomes possible. Though the receiver is always in the enable state, the transmitter is placed in the transmitter-enable state (T_XEN) by a command instruction, and the application of a low-level signal to the $\overline{CTS}$ pin prompts data-transfer start-up. Until this condition is satisfied, transmission is not executed. On receiving data, the receiver informs the CPU that reading for the receiver data in the USART by the CPU has become possible (the R_XRDY terminal has turned to high-level). Since data reception and the entry of the CPU into the data-readable state are output as status information, the CPU can access USART status without accessing the R_XRDY terminal.

During receiving operation, the USART checks errors and gives out status information. There are three types of errors: parity, overrun, and frame. Even though an error occurs, the USART continues its operations, and the error state is retained until error reset (ER) is effected by a command instruction. The M5M82C51AP access methods are listed in Table 1 .

Table 1 M5M82C51AP Access Methods

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
L	L	H	L	Data bus ← Data in USART
L	H	L	L	USART ← Data bus
H	L	H	L	Data bus ← Status
H	H	L	L	Control ← Data bus
X	H	H	L	3-State ← Data bus
X	X	X	H	3-State ← Data bus

Read/Write Control Logic

This logic consists of a control word register and command word register. It receives signals from the CPU control bus and generates internal-control signals for the elements.

Modem Control Circuit

This is a general-purpose control-signal circuit designed to simplify the interface to the modem. Four types of control signal are available: output signals $\overline{DTR}$ and $\overline{RTS}$ are controlled by command instructions, input signal $\overline{DSR}$ is given to the CPU as status information and input signal $\overline{CTS}$ controls direct transmission.

Data-Bus Buffer

This is an 8-bit 3-state bidirectional bus through which control words, command words, status information, and transfer data are transferred. Fig. 2 shows the structure of the data-bus buffer.

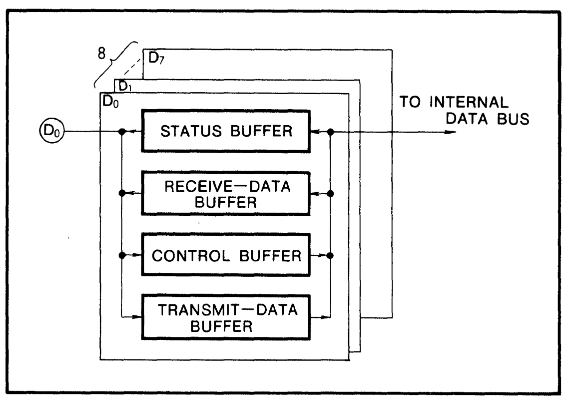


Fig. 2 Data-bus buffer structure

Transmit Buffer

This buffer converts parallel-format data given to the data-bus buffer in to serial data with addition of a start bit, stop bits and a parity bit, and sends out the converted data through the T_XD pin based on the control signal.

Transmit-Control Circuit

This circuit carries out all the controls required for serial data transmission. It controls transmitter data and outputs the signals required by external devices in accordance with the instructions of the read/write control logic.

Clear-To-Send Input ($\overline{CTS}$)
When the T_XEN bit (D_0) of the command instruction has been set to 1 and the $\overline{CTS}$ input is low-level serial data is sent out from the T_XD pin. Usually this is used as a clear-to-send signal for the modem
Note: CTS indicates the modem status as follows:
ON means data transmission is possible;
OFF means data transmission is impossible.

Transmitter-Empty Output (T_XEMPTY)
When no transmisison characters are left in the transmit buffer, this pin enters the high-level state. In the asynchronous mode, the following transmission character is shifted to the transmit buffer when it is loaded from the CPU. Thus, it is automatically reset. In the synchronous mode, a SYNC character is loaded automatically on the transmit buffer when no transfer-data characters are left. In this case, however, the T_XEMPTY does not enter the low-level state when a SYNC character has been sent out, since T_XEMPTY ="H" denotes the state in which there is no transfer character and one or two SYNC characters are being transferred or the state in which a SYNC character is being transferred as a filler. T_XEMPTY is unrelated to the T_XEN bit of the command instruction.

Transmission-Data Output (T_XD)
Parallel-format transmission characters loaded on the M5M82C51AP by the CPU are assembled into the format designated by the mode instruction and sent in serial-data form via the T_XD pin. Data is output, however, only in cases where the D_0 bit (T_XEN) of the command instruction is 1 and the $\overline{CTS}$ terminal is in the low-level state. Once reset, this pin is kept at the mark status (high-level) until the first character is sent.

Clock Input (CLK)
This system-clock input is required for internal-timing generation and is usually connected to the clock-output (CLK) pin of the M5L8085AP. Although there is no direct relation with the data-transfer baud rate, the clock-input (CLK) frequency is more than 30 times the $\overline{T_XC}$ or $\overline{R_XC}$ input frequency in the case of the synchronous system and more than 4. 5 times in the case of the asynchronous system.

Reset Input (RESET)
Once the USART is shifted to the idle mode by a high-level input, this state continues until a new control word is set Since this is a master reset, it is always necessary to load a control word following the reset process. The reset input requires a minimum 6-clock pulse width.

Data-Set Ready Input ($\overline{DSR}$)
This is a general-purpose input signal, but is usually used as a data-set ready signal to test modem status. Its status can be known from the status reading process. The D_7 bit of the status information equals 1 when the $\overline{DSR}$ pin is in the low-level state, and 0 when in the high-level state.
$\overline{DSR}$="L"→D_7 bit of status information=1
$\overline{DSR}$="H"→D_7 bit of status information=0
Note. DSR indicates modem status as follows:
ON means the modem can transmit and receive;
OFF means it cannot.

Request-To-Send Output ($\overline{RTS}$)
This is a general-purpose output signal but is used as a request-to-send signal for the modem. The $\overline{RTS}$ terminal is controlled by the D_5 bit of the command instruction. When D_5 is equal to 1, $\overline{RTS}$="L", and when D_5 is 0, $\overline{RTS}$="H".
Command register D_5=1→$\overline{RTS}$="L"
Command register D_5=0→$\overline{RTS}$="H"
Note: RTS controls the modem transmission carrier as follows:
ON means carrier dispatch;
OFF means carrier stop.

Data-Terminal Ready Output ($\overline{DTR}$)
This is a general-purpose output signal, but is usually used as a data-terminal ready or rate-select signal to the modem. The $\overline{DTR}$ pin is controlled by the D_1 bit of the command instruction; if D_1=1, $\overline{DTR}$="L", and if D_1=0, $\overline{DTR}$= "H".
D_1 of the command register=1→$\overline{DTR}$="L"
D_1 of the command register=0→$\overline{DTR}$="H"

Receiver-Clock Input ($\overline{R_XC}$)
This clock signal controls the baud rate for the sending in of characters via the $\overline{R_XD}$ pin. The data is shifted in by the rising edge of the $\overline{R_XC}$ signal. In the synchronous mode, the $\overline{R_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by mode setting. This relationship is parallel to that of $\overline{T_XC}$, and in usual communication-line systems the transmission and reception baud rates are equal. The $\overline{T_XC}$ and $\overline{R_XC}$ terminals are, therefore, used connected to the same baud-rate generator.

PROGRAMMING

It is necessary for the M5M82C51AP to have the control word loaded by the CPU prior to data transfer. This must always be done following any resetting operation (by external RESET pin or command instruction IR). There are two types of control words: mode instructions specifying general operations required for communications and command instructions to control the M5M82C51AP actual operations.
Following the resetting operation, a mode instruction must be set first. This instruction sets the synchronous or asynchronous system to be used. In the sysnchronous system, a SYNC character is loaded from the CPU. In the case of the bi-sync system, however, a second SYNC character must be loaded in succession.
Loading a command instruction makes data transfer possible. This operation after resetting must be carried out for initializing the M5M82C51AP. The USART command instruction contains an internal-reset IR instruction (D_6bit) that makes it possible to return the M5M82C51AP to its reset state. The initialization flowchart is shown in Fig. 3 and the mode-instruction and command-instruction formats are shown in Figs. 4 and 5.

Asynchronous Transmission Mode
When data characters are loaded on the M5M82C51AP after initial setting, the USART automatically adds a start bit (0), an odd or even parity bit specified by the mode instruction during initialization, and a specified number of stop bits (1). After that, the assembled data characters are transferred as serial data via the T_XD pin, if transfer is enabled ($T_XEN=1 \cdot \overline{CTS}=$"L"). In this case, the transfer data (baud rate) is shifted by the mode instruction at a rate of 1X, 1/16X, or 1/64X the $\overline{T_XC}$ period.
If the data characters are not loaded on the M5M82C51AP, the T_XD pin enters a mark state ("H"). When SBRK is programmed by the command instruction, break characters (0) are output continuously through the T_XD pin

Asynchronous Reception Mode
The R_XD line usually starts operations in a mark state ("H"), triggered by the falling edge of a low-level pulse when it comes to this line. This signal is again strobe at the middle of the bit to confirm that it is a perfect start bit. The detection of a second low-level indicates the validity of the start bit (again strobe is carried out only in the case of 16X and 64X) . After that, the bit counter inside the M5M82C51AP starts operating; each bit of the serial information on the R_XD line is shifted in by the rising edge of $\overline{R_XC}$, and the data bit, parity bit (when necessary), and stop bit are sampled at the middle position.
The occurrence of a parity error causes the setting of a parity-error flag. If the stop bit is 0, a frame error flag is set. Attention should be paid to the fact that the receiver requires only one stop bit even though the program has designated 1.5 or 2 stop bits.
Reception up to the stop bit means reception of a complete character. This character is then transferred to the receiver-data buffer shown in Fig.2, and the R_XRDY becomes active. In cases where this character is not read by the CPU and where the next character is transferred to the receiver-data buffer, the preceding character is destroyed and an overrun-error flag is set.
These error flags can be read as the M5M82C51AP status information. The occurrence of an error does not stop USART operations. The error flags are cleared by the ER (D_4 bit) of the command instruction.
The asynchronous-system transfer formats are shown in Figs. 6 and 7.

Synchronous Transmission Mode
In this mode the T_XD pin remains in the high-level state until initial setting by the CPU is completed. After initialization, the state of $\overline{CTS}=$"L" and $T_XEN=1$ enables serial transmission of characters through the T_XD pin. Then, data characters are sent out and shifted by the falling edge of the $\overline{T_XC}$ signal. The transmission rate equals the $\overline{T_XC}$ rate.
Thus, once data-character transfer starts, it must continue through the T_XD pin at the same rate as that of $\overline{T_XC}$. Unless data characters are provided from the CPU before the transmitter buffer becomes empty, one or two SYNC characters are automatically output from the T_XD pin. In this case, it should be noted that the T_XEMPTY pin enters the high-level state when there are no data characters left in the M5M82C51AP to be transferred, and that the low-level state is not entered until the USART is provided with the next data character from the CPU. Care should also be taken over the fact that merely setting a command instruction does not effect SYNC character insertion, because the SYNC character insertion is enabled after sending out the first data character.
In this mode, too, break characters are sent out in succession from the T_XD pin when SBRK is designated ($D_3=1$) by a command instruction.

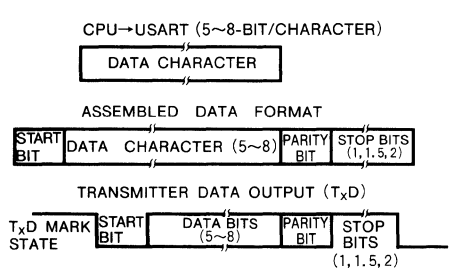
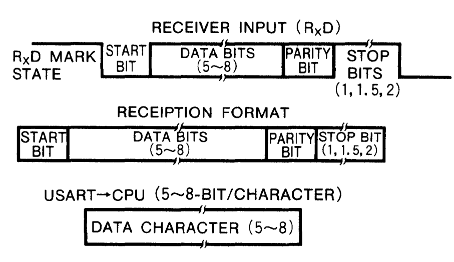


Fig. 6 Asynchronous transmission format I (transmission)



Note When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0

Fig. 7 Asynchronous transmission format II (reception)

Status Information

The CPU can always read USART status by setting the C/$\overline{D}$ to high-level and $\overline{RD}$ to low-level.
The status information format is shown in Fig. 10. In this format R_XRDY, T_XEMPTY and SYNDET have the same definitions as those of the pins. This means that these three pieces of status information become high-level when each pin is 1. The other status information is defined as follows:

DSR: When the $\overline{DSR}$ pin is in the low-level state, status information DSR becomes 1.

FE: The occurrence of a frame error in the receiver section makes the status information FE=1.

OE: The occurrence of an overrun error in the receiver section makes the status information OE=1.

PE: The occurrence of a parity error in the receiver section makes this status information PE=1.

T_XRDY: This information becomes 1 when the transmit data buffer is empty. Be careful because this has a different meaning from the T_XRDY pin that enters the high-level state only when the transmitter buffer is empty, when the $\overline{CTS}$ pin is in the low-level state, and when T_XEN is 1.

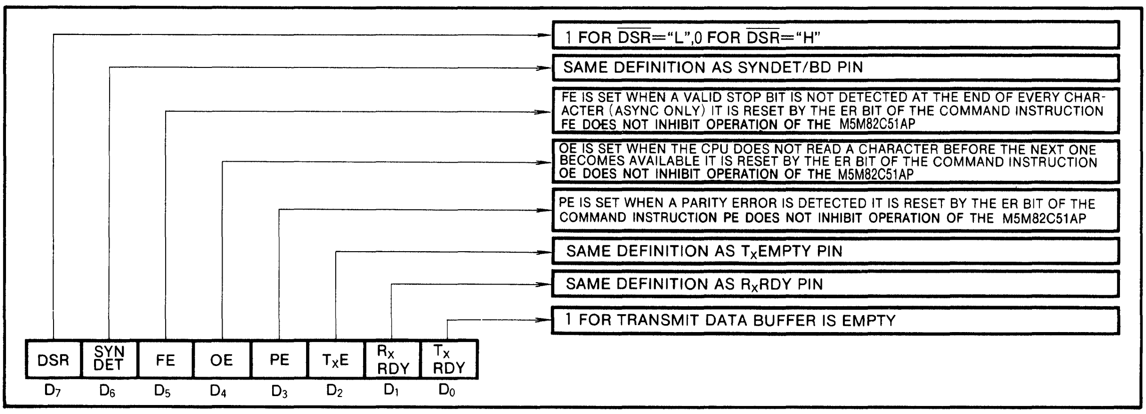


Fig. 10 Status information C/$\overline{D}$="H", $\overline{RD}$="L")

APPLICATION EXAMPLES

Fig. 11 shows an application example for the M5M82C51AP in the asynchronous mode. When the port addresses of the M5M82C51AP are assumed to be 00# and 01# in this figure, initial setting in the asynchronous mode is carried out in the following manner:

MVI	**A, B6#**	Mode setting
OUT	**01#**	
MVI	**A, 27#**	Command instruction
OUT	**01#**	

In this case, the following are set by mode setting:

Asynchronous mode
6-bit/character
Parity enable (even)
1.5 stop bits
Baud rate: 16X

Command instructions set the following

RTS=1→$\overline{RTS}$ pin="L"
R_XE=1
DTR=1→$\overline{DTR}$ pin="L"
T_XEN=1

When the initial setting is complete, transfer operations are allowed. The $\overline{RTS}$ pin is initially set to the low-level by setting RTS to 1, and this serves as a $\overline{CTS}$ input with T_XEN being equal to 1. For this reason the same definition applies to the status and pin of T_XRDY, and 1 is assigned when the transmit-data buffer is empty. Actual transfer of data is carried out in the following way:

IN	**01#**	Status read

The IN instruction prompts the CPU to read the USART's status. The result is; if the T_XRDY equals 1 transmitter data is sent from the CPU and written on the M5M82C51AP. Transmitter data is written in the M5M82C51AP in the following manner:

MVI	**A, 2D#**	$2D_{16}$ is an example of transmitter data.
OUT	**00#**	USART←(A)

Receiver data is read in the following manner:

IN	**00#**	(A)←USART

In the above example, the status information is read and as a result, the transmitter data is written and read. Interruption processing by using the T_XRDY and R_XRDY pins is also possible.
Fig. 12 shows the status of the T_XD pin when data written in the USART is transferred from the CPU. When the data shown in Fig.12 enters the R_XD pin, data sent from the M5M82C51AP to the CPU becomes $2D_{16}$ and bits D_6 and D_7 are treated as 0.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		−0.3～V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Power-supply voltage (GND)		0		V

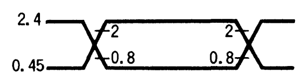
ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}	All outputs are high-level			5	mA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state input current	V_O=0V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			20	pF

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read (Note8)	C_L=150pF			200〔170〕	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		10		100	ns
$t_{PZV(TxC-TxD)}$	T_{XD} enable time after falling edge of $\overline{T_XC}$				1	μs
$t_{PLH(CLB-TxR)}$	Propagation time from center of last bit to T_XRDY (Note9)				8	$t_{C(\phi)}$
$t_{PHL(W-TxR)}$	Propagation time from write data to T_XRDY clear (Note9)				400	ns
$t_{PLH(CLB-RxR)}$	Propagation time from center of last bit to R_XRDY (Note9)				26	$t_{C(\phi)}$
$t_{PHL(R-RxR)}$	Propagation time from read data to R_XRDY clear (Note9)				400	ns
$t_{PLH(RxC-SYD)}$	Propagation time from rising edge of $\overline{R_XC}$ to internal SYNDET (Note9)				26	$t_{C(\phi)}$
$t_{PLH(CLB-TxE)}$	Propagation time from center of last bit to T_XEMPTY (Note9)				20	$t_{C(\phi)}$
$t_{PHL(W-C)}$	Propagation time from rising edge of $\overline{WR}$ to control (Note9)				8	$t_{C(\phi)}$

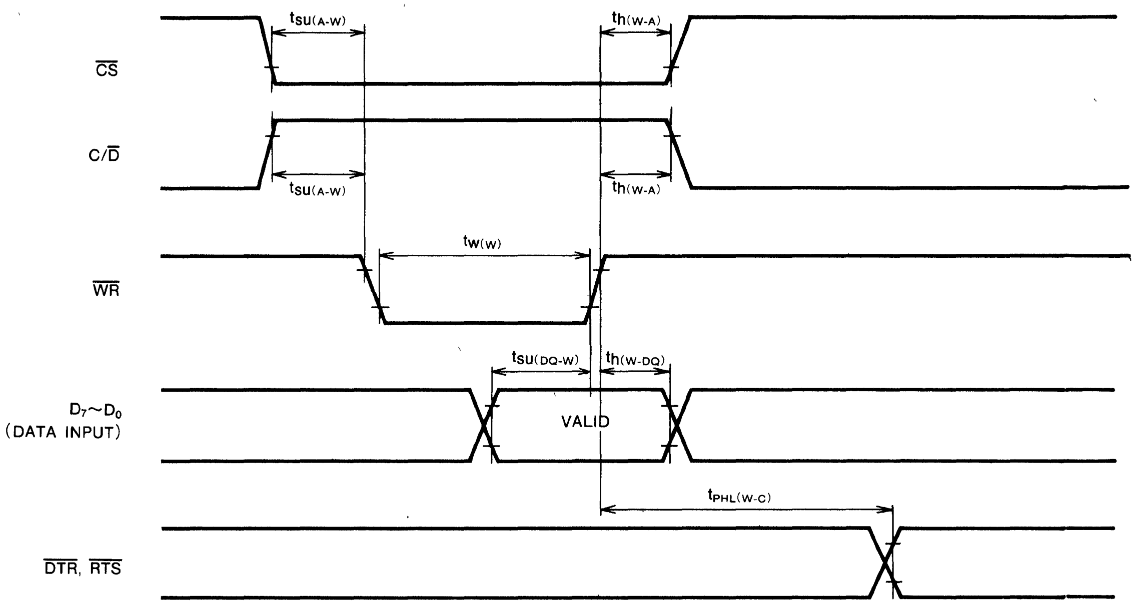
Note 8 : Assumes that address is vaild before falling edge of $\overline{RD}$.
9 : Status-up data can have a maximum delay of 28 clock periods from the event affecting the status.
10 : Input pulse level 0.45~2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 10ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 10ns



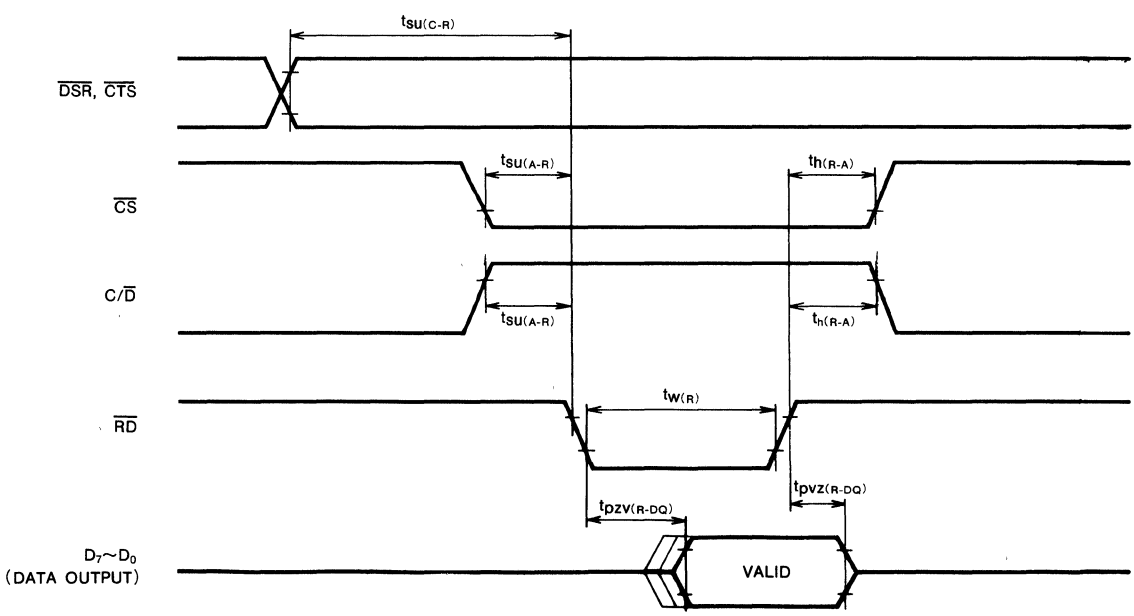
11 : M5M82C51AP is also invested with the extended specification showed in the brackets.

MITSUBISHI ELECTRIC

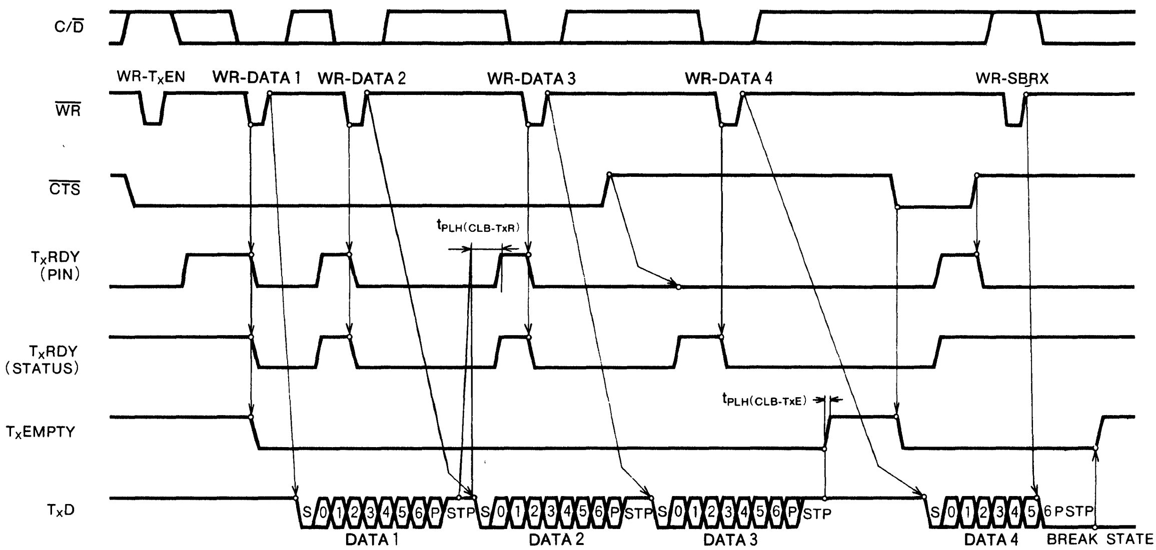
Write Control Cycle (CPU→USART)



Read Control Cycle (USART→CPU)

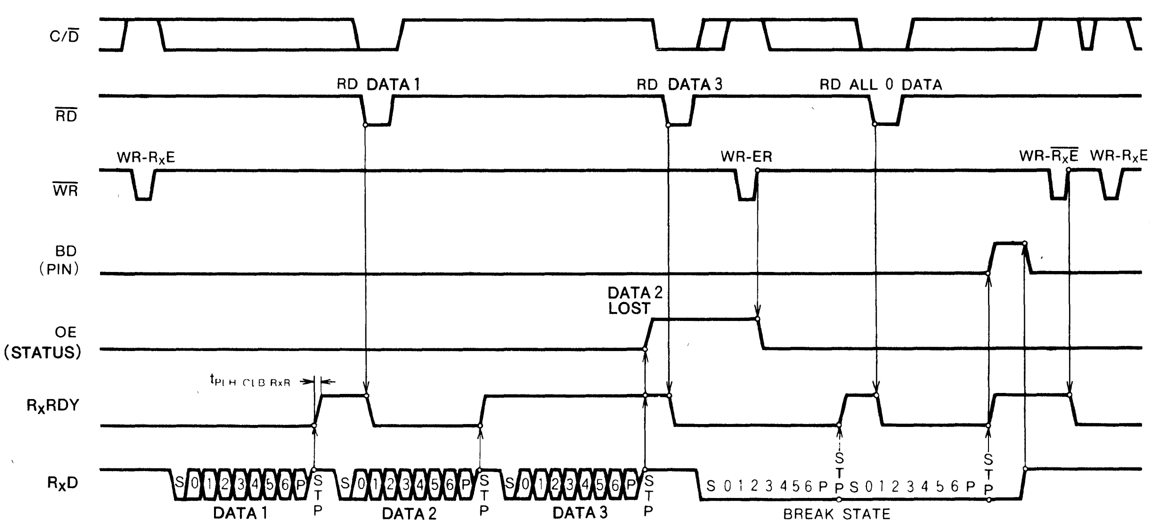


Transmitter Control & Flag Timing (Async Mode)



Note 12 : Example format= 7 bits/character with parity & 2 stop bits
13 : T_XRDY(pin)="H"←(Transmit-data buffer is empty) • (T_XEN= 1) • (CTS="L")
14 : T_XRDY(status)= 1 ←(Transmit-data buffer is empty)

Receiver Control & Flag Timing (Async Mode)



Note 15 : Example format= 7 bits/character with parity & 2 stop bits

MITSUBISHI ELECTRIC

M5M82C54P/FP/J

CMOS PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The M5M82C54P is a programmable general-purpose timer device developed by using the silicon-gate CMOS process. It offers counter and timer functions in systems using an 8-bit parallel-processing CPU. The use of the M5M82C54P frees the CPU from the execution of looped programs, count-operation programs and other simple processing involving many repetitive operations, thus contributing to improved system throughputs. It is housed in a 24-pin plastic molded DIP.

And preparatory for surface equipment M5M82C54FP (SOP) and M5M82C54J(PLCC).

FEATURES

- Single 5V supply voltage
- TTL compatible
- Pin connection compatible with M5L8253P-5 (except M5M82C54J)
- Clock period : DC~8MHz
- 3 independent built-in 16-bit down counters
- 6 counter modes freely assignable for each counter
- Binary or decimal counts
- Read-back command for monitoring the count and status

APPLICATION

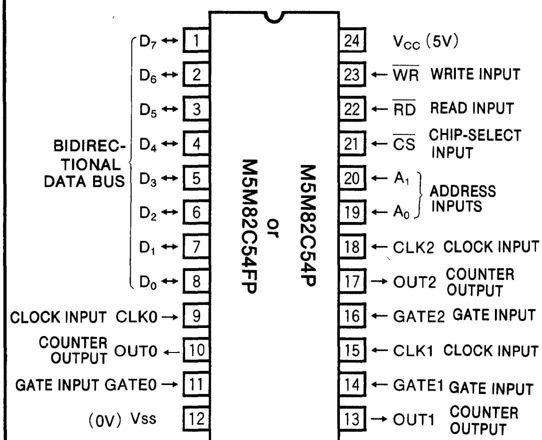
Delayed-time setting, pulse counting and rate generation in microcomputers.

FUNCTION

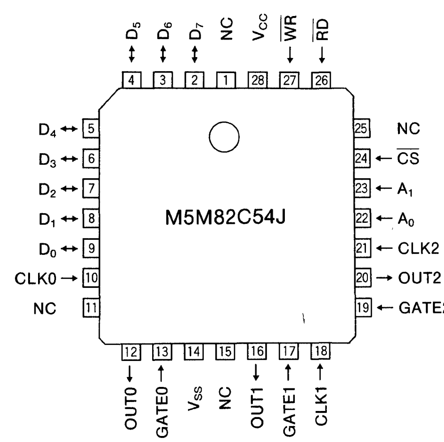
Three independent 16-bit counters allow free programming based on mode-control instructions from the CPU. When roughly classified, there are 6 modes (0 ~ 5). Mode 0 is mainly used as an interruption timer and event counter, mode 1 as a digital one-shot, modes 2 and 3 as a rate generator, mode 4 for a software triggered strobe, and mode 5 for a hardware triggered strobe.

The count can be monitored and set at any time. Besides the count, the status of the counter can be monitored by Read-back command. The counter operates with either the binary or BCD system.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4 (M5M82C54P)
24P2W (M5M82C54FP)



Outline 28P0

NC : NO CONNECTION

DESCRIPTION OF FUNCTIONS

Data-Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the M5M82C54P to the system-side data bus. Transmission and reception of all the data including control words for mode designation and values written in, and read from, the counters are carried out through this buffer.

Read/Write Logic

The read/write logic accepts control signals ($\overline{RD}$, $\overline{WR}$) from the system and generates control signals for each counter. It is enabled or disabled by the chip-select signal ($\overline{CS}$); if $\overline{CS}$ is at the high-level the data-bus buffer enters a floating (high-impedance) state.

Read Input ($\overline{RD}$)

The count of the counter designated by address inputs A_0 and A_1 on the low-level is output to the data bus.

Write Input ($\overline{WR}$)

Data on the data bus is written in the counter or control-word register designated by address inputs A_0 and A_1 on the low-level.

Address Inputs (A_0, A_1)

These are used for selecting one of the 3 internal counters and either of the control-word registers.

Chip-Select Input ($\overline{CS}$)

A low-level on this input enables the M5M82C54P. Changes in the level of the $\overline{CS}$ input have no effect on the operation of the counters.

Control-Word Register

This register stores information required to give instructions about operational modes and to select binary or BCD counting. It allows reading,using Read back command.

Counters 0,1 and 2

These counters are identical in operation and independent of each other. Each is a 16-bit, presettable, down counter, and has clock-input, gate-input and output pins. The counter can operate in either binary or BCD using the falling edge of each clock. The mode of counter operation and the initial value from which to start counting can be designated by software. The count can be read by input instruction at any time, and there is a "read-on-the-fly" function which enables stable reading by latching each instantaneous count to the registers by a special counter-latch instruction.

CONTROL-WORD AND INITIAL-VALUE LOADING

The function of the M5M82C54P depends on the system software. The operational mode of the counters can be specified by writing control words (A_0, A_1 = 1, 1) into the control-word registers.

The programmer must write out to the M5M82C54P the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

Fig. 1 shows control-word format, which consists of 4 fields. Only the counter selected by the D_7 and D_6 bits of the control-word is set for operation. Bits D_5 and D_4 are used for specifying operations to read values in the counter and to initialize. Bits $D_3 \sim D_1$ are used for mode designation, and D_0 for specifying binary or BCD counting. When D_0=0, binary counting is employed, and any number from 0000_{16} to $FFFF_{16}$ can be loaded into the count register. The counter is counted down for each clock. The counting of 0000_{16} causes the transmission of a time-out signal from the count-output pin.

The maximum number of counts is obtained when 0000_{16} is set as the initial value. When D_0 = 1, BCD counting is employed, and any number from 0000_{10} to 9999_{10} can be loaded on the counter.

Neither system resetting nor connecting to the power supply sets the control word to any specific value. Thus to bring the counters into operation, the above-mentioned control words for mode designation must be given to each counter, and then 1~2 byte initial counter values must be set. The following is an example of this programming step.

To designate mode 0 for counter 1 ,with initial value 8254_{16} set by binary count, the following program is used:

MVI	**A, 70_{16}**	Control word 70_{16}
OUT	**n_1**	n_1 is control-word-register address
MVI	**A, 54_{16}**	Low-order 8 bits
OUT	**n_2**	n_2 is counter 1 address
MVI	**A, 82_{16}**	High-order 8 bits
OUT	**n_2**	n_2 is counter 1 address

Thus, the program generally has the following sequence:

(1) Control-word output to counter i (i=0, 1, 2).
(2) Initialization of low-order 8 counter bits
(3) Initialization of high-order 8 counter bits

The three counters can be executed in any sequence. It is possible, for instance, to designate the mode of each counter and then load initial values in a different order. Initialization of the counters designated by RL 1 and RL 0 must be executed in the order of the low-order 8 bits and then the high-order 8 bits for the counter in question.

MODE DEFINITION

Mode 0 (Interrupt on Terminal Count)

Mode set and initialization cause the counter output to go low-level (see Fig. 2). When the counter is loaded with an initial value, it will start counting the clock input. When the terminal count is reached, the output will go high-level and remain high-level until the selected count register is reloaded with the mode. This mode can be used when the CPU is to be interrupted after a certain period or at the time of counting up.

Fig. 2 shows a setting of 4 as the initial value. If gate input goes low-level, counting is inhibited for the duration of the low-level period.

Reloading of the initial value during count operation will stop counting by the loading of the first byte and start the new count by the loading of the second byte.

Mode 1 (Programmable One-Shot)

The gate input functions as a trigger input. A gate-input rising edge causes the generation of low-level one-shot output with a predetermined clock length starting from the next clock. Fig. 3 shows an initial setting of 4. While the counter output is at the low-level (during one-shot), loading of a new value does not change the one-shot pulse width, which has already been output. The current count can be read at any time without affecting the width of the one-shot pulse being output. This mode permits retriggering.

Mode 2 (Rate Generator)

Low-level pulses during one clock operation are generated from the counter output at a rate of one per n clock inputs (where n is the value initially set for the counter). When a new value is loaded during the counter operation, it is reflected on the output after the pulses by the current count have been output. In the example shown in Fig. 4 , n is given as 4 at the outset and is then changed to 3.

In this mode, the gate input provides a reset function. While it is on the low-level, the output is maintained high-level; the counter restarts from the initial value, triggered by a rising gate-input edge. This gate input, therefore, makes possible external synchronization of the counter by hardware.

After the mode is set, the counter does not start counting until the rate n is loaded into the count register, with the counter output remaining at the high-level.

Mode 3 (Square Rate Generator)

This is similar to Mode 2 except that it outputs a square wave with the half count of the set rate. When the set value n is odd, the square-wave output will be high-level for (n+1)/2 clock-input counts and low for (n−1)/2 counts. When a new rate is reloaded into the count register during its operation, it is immediately reflected on the count directly following the output transition (high-to-low or low-to-high) of the current count. Gate-input operations are exactly the same as in Mode 2. Fig. 5 shows an example of Mode 3 operation.

Mode 4 (Software Triggered Strobe)

After the mode is set, the output will be high-level. By loading a number on the counter, however, clock-input counts can be started and on the terminal count, the output will go low-level for one input-clock period and then will go high-level again. Mode 4 differs from Mode 2 in that pulses are not output repeatedly with the same set count. The pulse output is delayed one clock period in Mode 2, as shown in Fig. 6 . When a new value is loaded into the count register during its count operation, it is reflected on the next pulse output without affecting the current count. The count will be inhibited while the gate input is low-level.

Mode 5 (Hardware Triggered Strobe)

This is a variation of Mode 1. The gate input provides a trigger function, and the count is started by its rising edge. On the terminal count, the counter output goes low for on one clock period and then goes high-level. As in Mode 1, retriggering by the gate input is possible. An example of timing in Mode 5 is shown in Fig. 7 .

As mentioned above, the gate input plays different roles according to the mode. The functions are summarized in Table 3.

Table 2 Gate Operations

Gate / Mode	Low-level or going low-level	Rising	High-level
0	Disables counting		Enables counting
1		(1) Initiates counting (2) Resets output after next clock	
2	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output high immediately	(1) Reloads counter (2) Initiates counting	Enables counting
4	Disables counting		Enables counting
5		Initiates counting	

READ BACK COMMAND

M5M82C54P has a function of reading not only the count but also status (Read Back Command). The read back command enables the next four functions.

(1) read the current count "on the fly"

(2) monitor the current state of the OUT pin

(3) monitor the current state of the counter element (whether the count is loaded into the counter element or not)

(4) read the control-word

Read back operation can be specified by writing read back command into the control word registers (A_0, A_1 =1, 1). Fig. 8 shows the format of read back command.

Bits D_7 and D_6 are used for specifying read back command and fixed 1 (D_7 =1, D_6 =1). Respectively bits D_5 ($\overline{\text{count}}$) and D_4 ($\overline{\text{status}}$) are used for reading the count and the status of the counter selected by the $D_3 \sim D_1$ bits. Bit D_0 must be fixed 0.

Only the count can be read "on the fly" by setting D_5 =0 and D_4 =1 as well as counter latch command above mentioned. If $D_3 \sim D_1$ are set 1 all, the counts of three counters are simultaneously latched by one read back command. (By counter-latch command, it must be latched for each counter.) Next, by read operation, the latched count is read out.

Only the status can be latched by setting D_5 =1 and D_4 =0. By read operation, the status shown in Fig. 9 can be read.

Bit D_7 gives the current state of OUT pin. When D_7 =1, OUT = "H", and when D_7 =0, OUT = "L". Bit D_6 indicates the current state of counter element. When D_6 =1, the initial counter value has not been loaded to counter element. This state is following.

(1) The control word is written, but the initial counter value is not loaded

(2) The initial counter value is written to count register, and the CLK inputs are not.

When D_6 = 0, the initial counter value has already been loaded. It is the state when the CLK falls following the rising edge after the initial value is written. Bits $D_5 \sim D_0$ show the current state of the control-word regsiter.

It is possible to read both the count and the status. By setting D_5 =0 and D_4 =0, the status can be read first, and the count next.

The count and/or the status are unlatched when read, so by the next read operation the current counting value can be read. And they are unlatched too when the control-word is set, so the read back command must be set on all such occasions.

If multiple read back commands are written before the read operation, only the first one is valid.

Thus, the read of the status is effective when the state of output and the timing of count reading can be monitored by software.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to V_{SS}	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
T_{opr}	Operating free-air temperature range		−20~75	℃
Tstg	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20~75℃, unless otherwise noted)

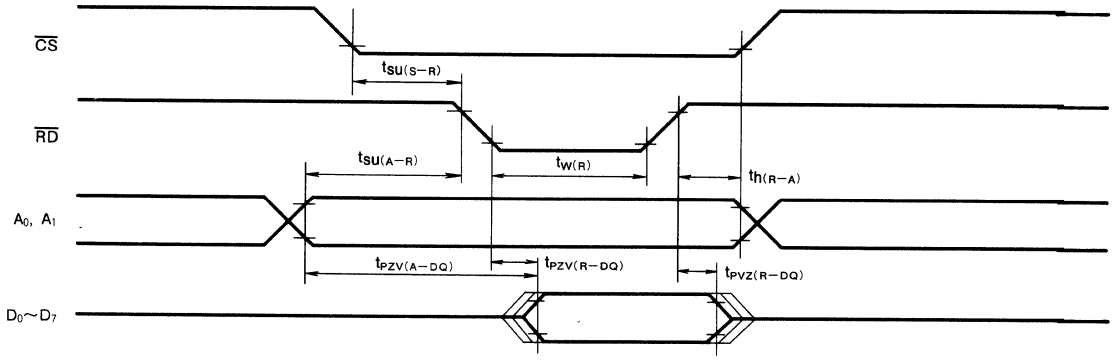
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Power supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

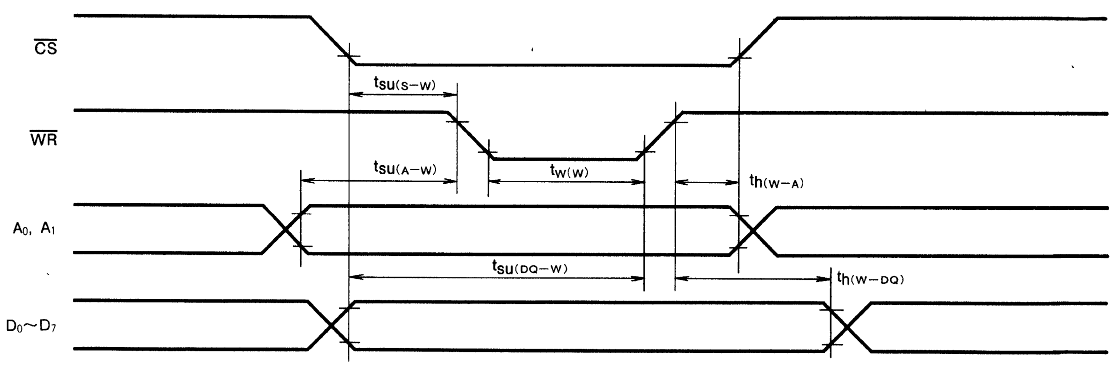
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.0mA			0.45	V
I_{IH}	High-level input current	V_I=V_{CC}			±10	μA
I_{IL}	Low-level input current	V_I=0V			±10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}			±10	μA
I_{CC}	Supply current from V_{CC} (operating)	f=8MHz			10	mA
I_{CCS}	Supply current from V_{CC} (stand by)	V_I=0V, V_{CC}			10	μA
C_i	Input termiral capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{i/o}$	Input/output termiral capacitance	$V_{I/OL}$=V_{SS}, f=1MHz,25mVrms, T_a=25℃			20	pF

TIMING DIAGRAMS

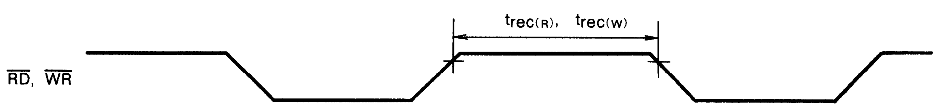
Read Cycle



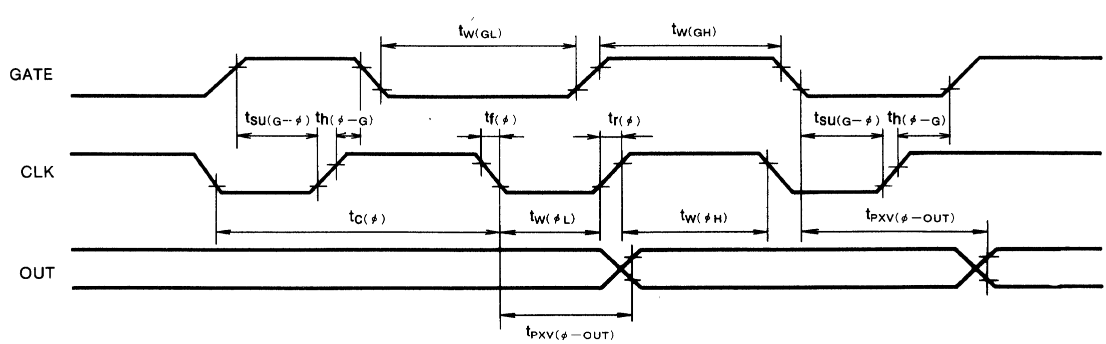
Write Cycle



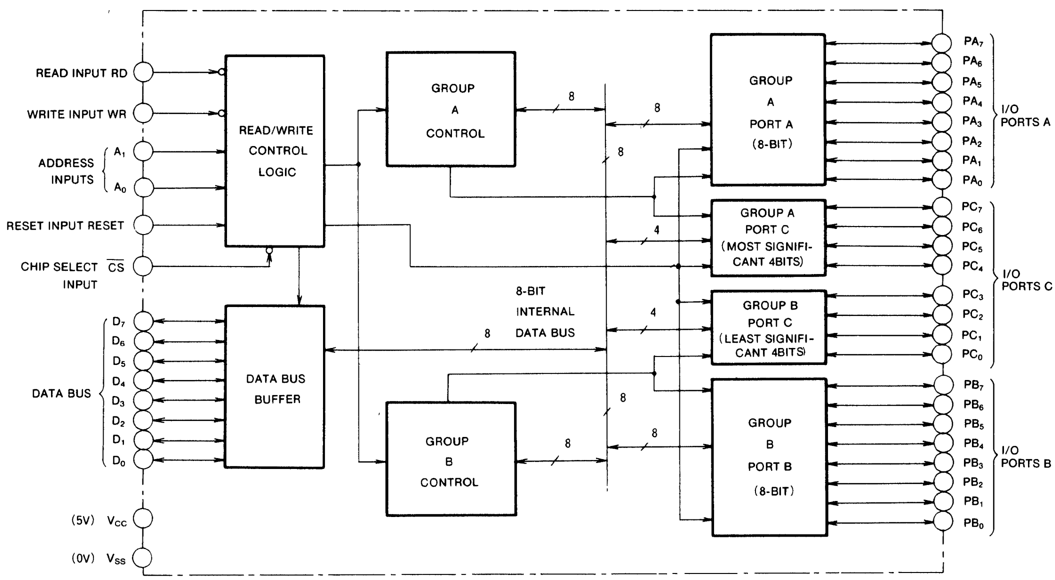
(Recovery Time)



Clock and Gate Cycle



BLOCK DIAGRAM



BASIC OPERATING MODES

The PPI can operate in any one of three selected basic modes.

Mode 0: Basic input/output (group A, group B)
Mode 1: Strobed input/output (group A, group B)
Mode 2: Bidirectional bus (group A only)

The mode of both group A and group B can be selected independently. The control word format for mode set is shown in Fig. 2.

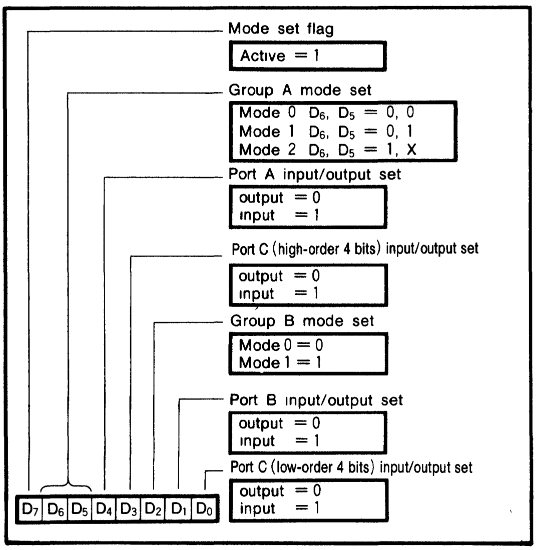
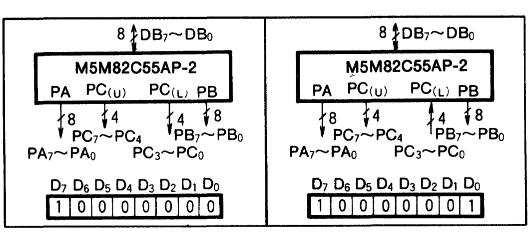
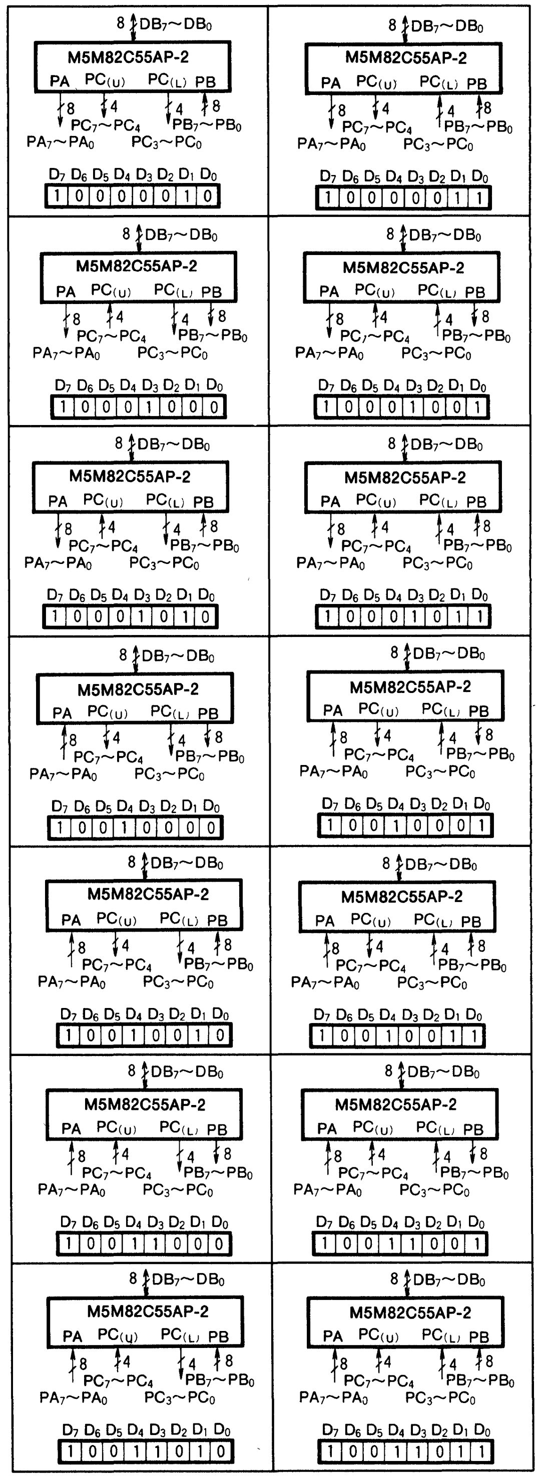


Fig. 2 Control word format for mode set.

1. Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the 3 ports. No "handshaking" is required; data is simply written in, or read from, the specified port. Output data from the CPU to the port can be held, but input data from the port to the CPU cannot be held. Any one of the 8-bit ports and 4-bit ports can be used as an input port or an output port. The diagrams following show the basic input/output operating modes.





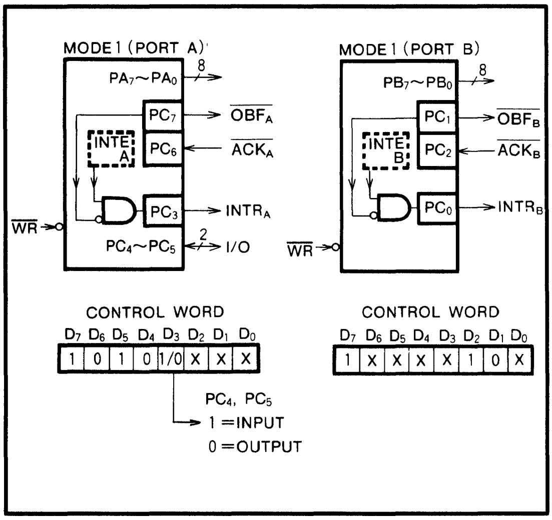


Fig. 5 An example of mode 1 output state

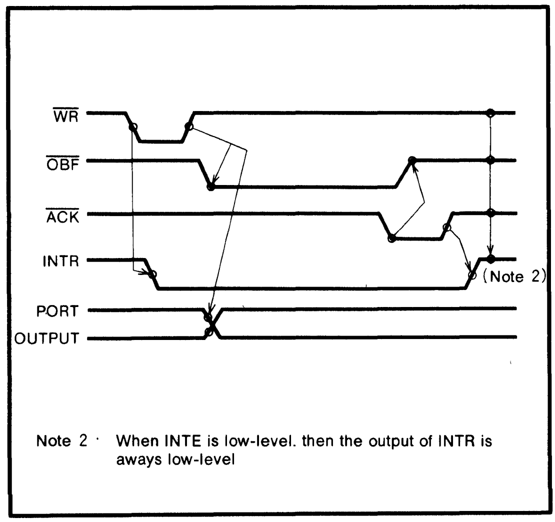


Fig. 6 Timing diagram

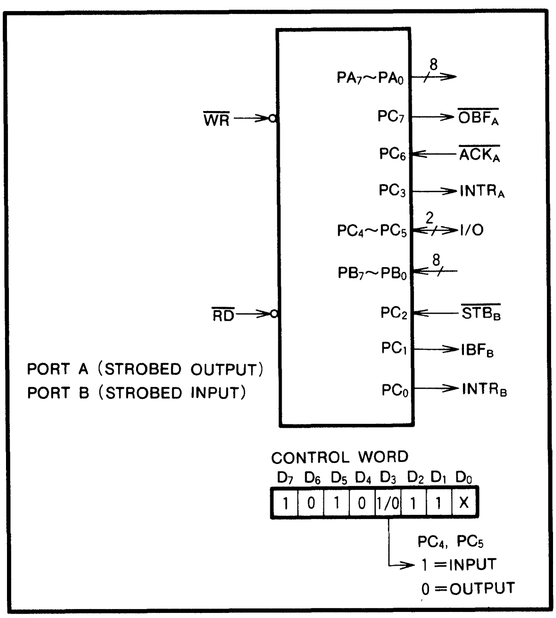


Fig. 7 Mode 1 port A and port B I/O example

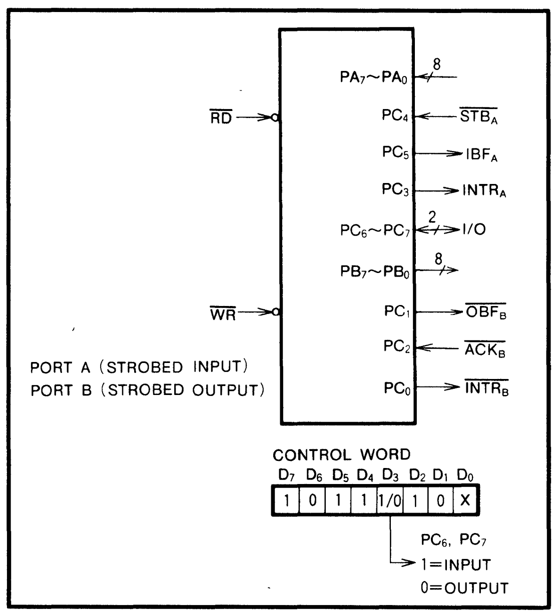


Fig. 8 Mode 1 port A and port B I/O example

4. Control Signal Read

In mode 1 or mode 2 when using port C as a control port, by CPU execution of an IN instruction, each control signal and bus status from port C can be read.

5. Control Word Tables

Control word formats and operation details for mode 0, mode 1, mode 2 and set/reset control of port C are given in Tables 3, 4, 5 and 6, respectively.

Table 2 Read-out control signals

Mode \ Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1, input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
Mode 1, output	$\overline{OBF_A}$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF_B}$	$INTR_B$
Mode 2	$\overline{OBF_A}$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	By group B mode		

Table 3 Mode 0 control words

Control words									Group A		Group B	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal	Port A	Port C (high-order 4 bits)	Port C (low-order 4 bits)	Port B
1	0	0	0	0	0	0	0	80	OUT	OUT	OUT	OUT
1	0	0	0	0	0	0	1	81	OUT	OUT	IN	OUT
1	0	0	0	0	0	1	0	82	OUT	OUT	OUT	IN
1	0	0	0	0	0	1	1	83	OUT	OUT	IN	IN
1	0	0	0	1	0	0	0	88	OUT	IN	OUT	OUT
1	0	0	0	1	0	0	1	89	OUT	IN	IN	OUT
1	0	0	0	1	0	1	0	8A	OUT	IN	OUT	IN
1	0	0	0	1	0	1	1	8B	OUT	IN	IN	IN
1	0	0	1	0	0	0	0	90	IN	OUT	OUT	OUT
1	0	0	1	0	0	0	1	91	IN	OUT	IN	OUT
1	0	0	1	0	0	1	0	92	IN	OUT	OUT	IN
1	0	0	1	0	0	1	1	93	IN	OUT	IN	IN
1	0	0	1	1	0	0	0	98	IN	IN	OUT	OUT
1	0	0	1	1	0	0	1	99	IN	IN	IN	OUT
1	0	0	1	1	0	1	0	9A	IN	IN	OUT	IN
1	0	0	1	1	0	1	1	9B	IN	IN	IN	IN

Note 4 OUT indicates output port, and IN indicates input port

Table 4 Mode 1 control words

Control words									Group A						Group B			
										Port C					Port C			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexa-decimal	Port A	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	Port B
1	0	1	0	0	1	0	X	A4 A5	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	0	1	1	X	A6 A7	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	OUT		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	0	1	1	0	X	AC AD	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	0	1	1	1	X	AE AF	OUT	$\overline{OBF_A}$	$\overline{ACK_A}$	IN		$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	0	1	0	X	B4 B5	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	0	1	1	X	B6 B7	IN	OUT		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN
1	0	1	1	1	1	0	X	BC BD	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{ACK_B}$	$\overline{OBF_B}$	$INTR_B$	OUT
1	0	1	1	1	1	1	X	BE BF	IN	IN		IBF_A	$\overline{STB_A}$	$INTR_A$	$\overline{STB_B}$	IBF_B	$INTR_B$	IN

Note 5 Mode of group A and group B can be programmed independently.
6 It is not necessary for both group A and group B to be in mode 1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3～7		V
V_I	Input voltage		−0.3～V_{CC}+0.3		V
V_O	Output voltage		−0.3～V_{CC}+0.3		V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	Port	−4	mA
			Data bus	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current 2	Port	4	mA
			Data bus	2.5	
T_{opr}	Operating free-air temperature renge		−20～75		℃
Tstg	Storage temperature range		−65～150		℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

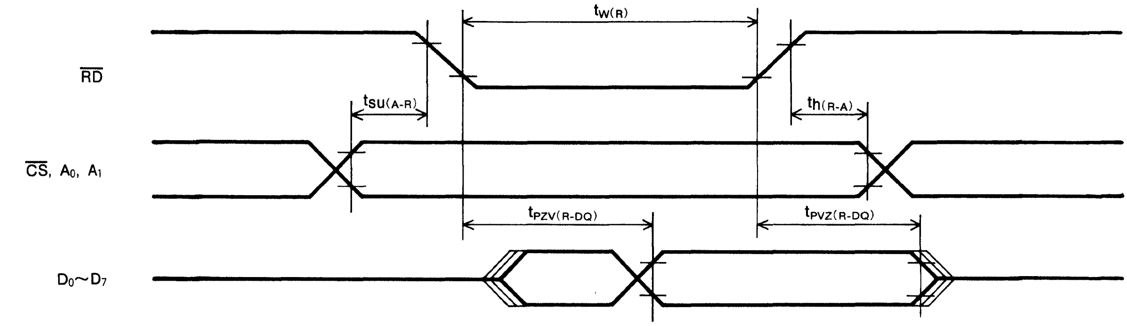
ELECTRICAL CHARACTERISTICS (Ta=−20～75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	Output high voltage (Note10)	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Output low voltage (Note10)	I_{OL}=2.5mA			0.4	V
I_{CC}	Supply current from V_{CC}	All input mode RESET=0V. Other pins=V_{CC}.			10	μA
I_{IL}	Input leak current	V_I=0V, V_{CC}			±10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}			±10	μA
C_i	Input terminal capacitance	f=1MHz			10	pF
$C_{i/o}$	Input/output terminal capacitance	Unmeasured pins=0V			20	pF

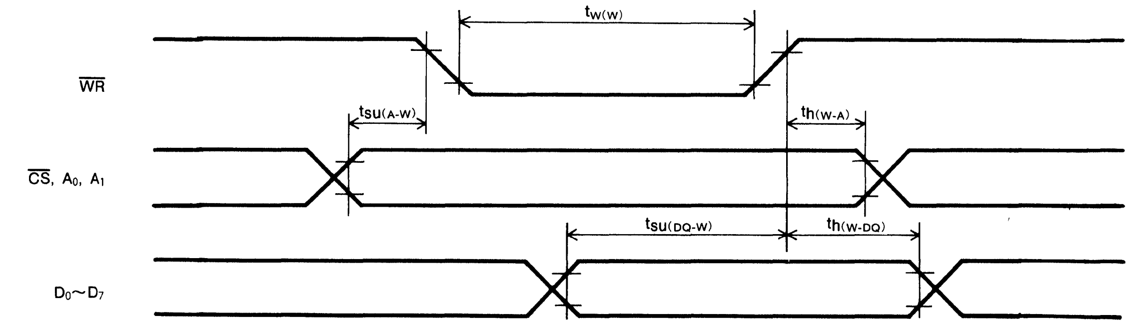
Note 9 : Current flowing into an IC is positive, out is negative.
10 : Output current must be less than ±4mA for each Port pin

TIMING DIAGRAM

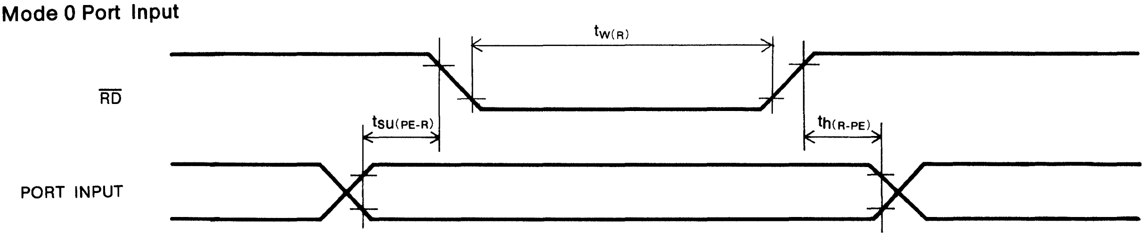
Data Bus Read Operation



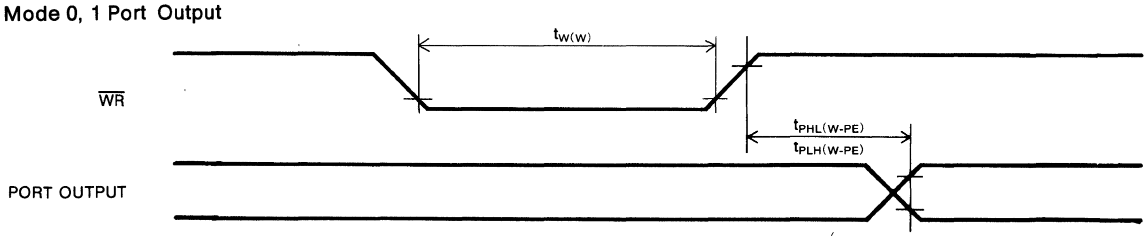
Data Bus Write Operation



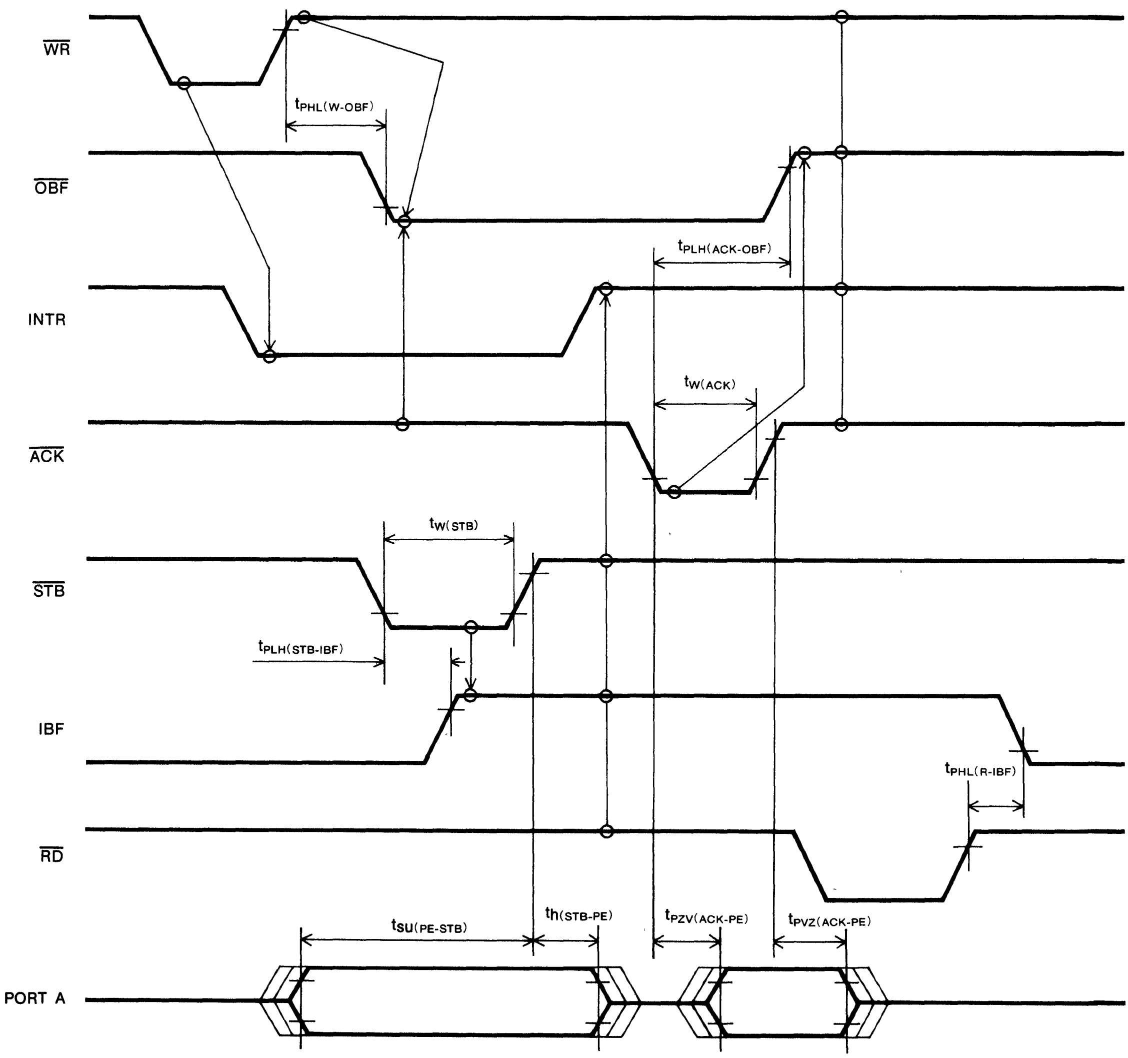
Mode 0 Port Input



Mode 0, 1 Port Output

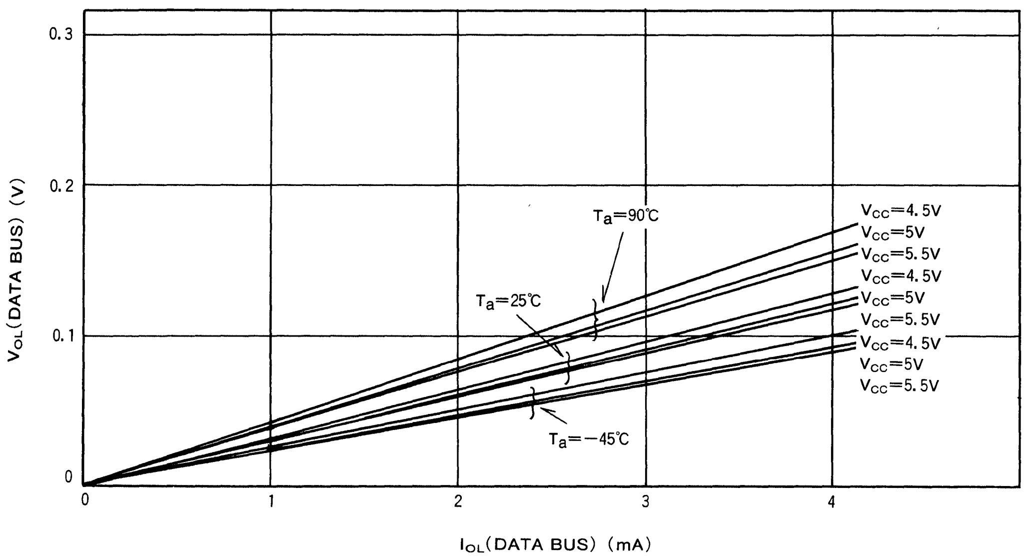


Mode 2 Bidirectional

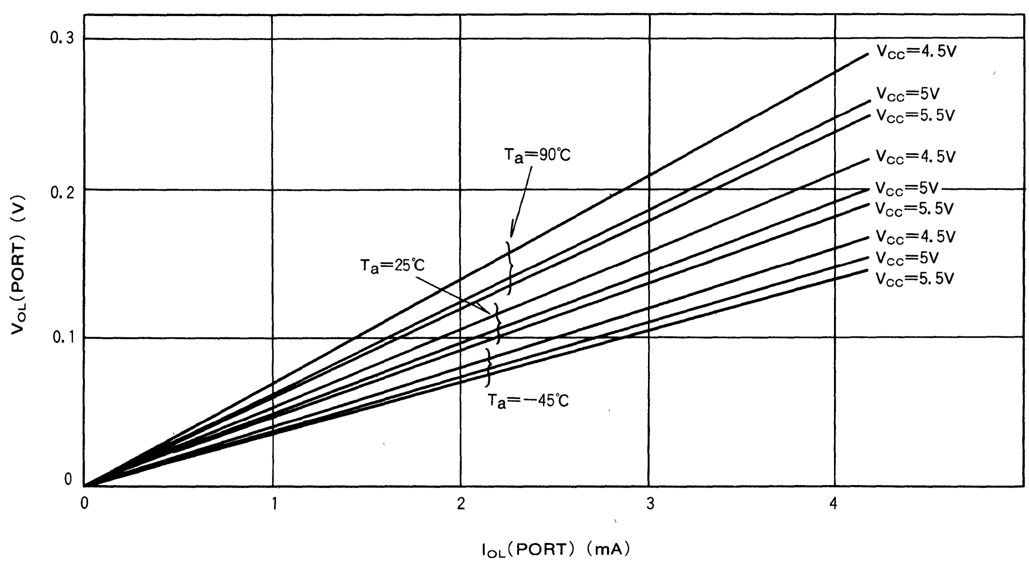


Note 13 : INTR=IBF · $\overline{\text{MASK}}$ · $\overline{\text{STB}}$ · $\overline{\text{RD}}$+$\overline{\text{OBF}}$ · $\overline{\text{MASK}}$ · $\overline{\text{ACK}}$ · $\overline{\text{WR}}$

$V_{OL}-I_{OL}$ CHARACTERISTICS (DATA BUS)

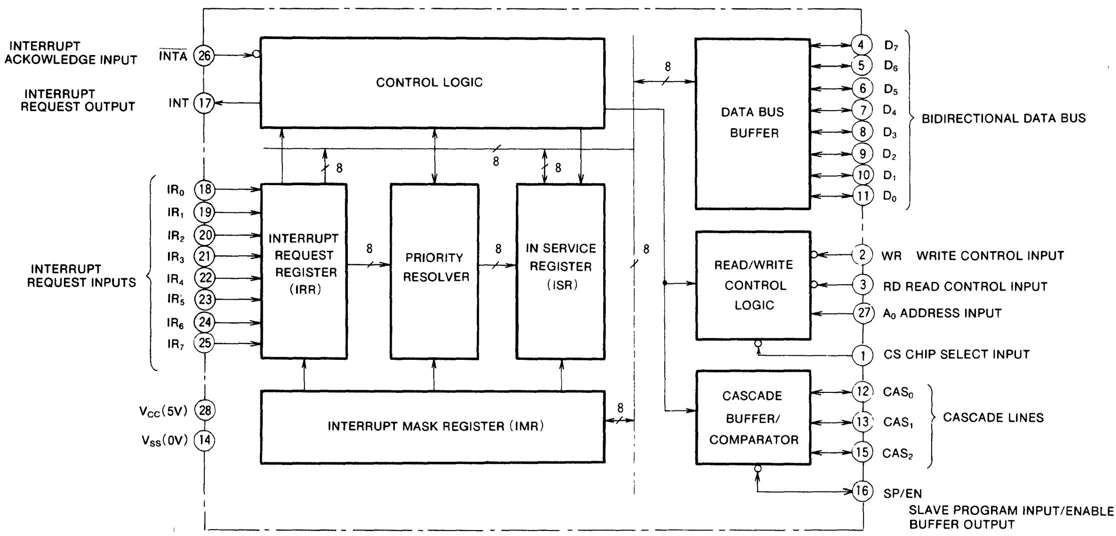


$V_{OL}-I_{OL}$ CHARACTERISTICS (PORT)



CMOS PROGRAMMABLE INTERRUPT CONTROLLER

BLOCK DIAGRAM



Interrupt Sequence

1. When the CPU is a MELPS85

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

(2) Mask state and priority levels are considered and, if appropriate, the M5M82C59AP-2 sends an INT signal to the CPU.

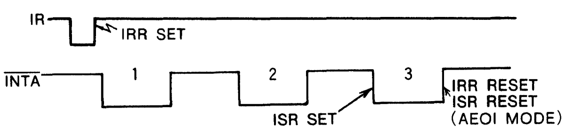
(3) The acknowledgement of the CPU to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, a CALL instruction is released onto the data bus.

(5) A CALL is a 3-byte instruction, so additional two $\overline{INTA}$ pulses are issued to the M5M82C59AP-2 from the CPU.

(6) These two $\overline{INTA}$ pulses allow the M5M82C59AP-2 to release the program address onto the data bus. The low-order 8 bits vectored address is released at the second $\overline{INTA}$ pulse and the high-order 8 bits vectored address is released at the third $\overline{INTA}$ pulse. The ISR bit corresponding to the interrupt request input is set upon receiving the third $\overline{INTA}$ pulse from the CPU, and the corresponding IRR bit is reset.

(7) This completes the 3-byte CALL instruction and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the third $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued.



2. When the CPU is a MELPS86 or MELPS88

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

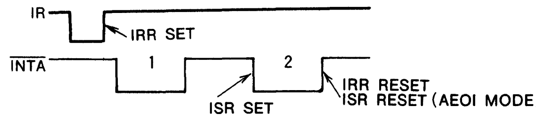
(2) Mask state and priority levels are considered and if appropriated, the M5M82C59AP-2 sends an INT signal to the CPU.

(3) As an acknowledgement to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, the M5M82C59AP-2 does not drive the data bus, and the data bus keeps high-impedance state.

(5) When the second $\overline{INTA}$ pulse is issued from the CPU, an 8-bit pointer is released onto the data bus.

(6) This completes the interrupt cycle and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the second $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued from the CPU.



The interrupt request input must be held at high-level until the first $\overline{INTA}$ pulse is issued. If it is allowed to return to low-level before the first $\overline{INTA}$ pulse is issued, an interrupt request in IR_7 is executed However, in this case the ISR bit is not set.

This is a function for a noise countermeasure of interrupt request inputs. In the interrupt routine of IR_7, if ISR is checked by software either the interrupt by noise or real interrupt can be acknowledged. In the state of edge trigger mode normally the interrupt request inputs hold high-level and its input low-level pulse in the case of interrupt.

Interrupt sequence outputs

1. When the CPU is a MELPS85

A CALL instruction is released onto the data bus when the first $\overline{INTA}$ pulse is issued. The low-order 8 bits of the vectored address are released when the second $\overline{INTA}$ pulse is issued, and the high-order 8 bits are released when the third $\overline{INTA}$ pulse is issued. The format of these three outputs is shown in Table 2.

Table 2 Formats of interrupt CALL instruction and vectored address

First $\overline{INTA}$ pulse (CALL instruction)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

Second $\overline{INTA}$ pulse (low-order 8 bits of vectored address)

IR	Interval= 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	A_5	0	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_7	A_7	A_6	A_5	1	1	1	0	0

Write Control Input ($\overline{WR}$)

When $\overline{WR}$ goes to low-level the M5M82C59AP-2 can be written.

Read Control Input ($\overline{RD}$)

When $\overline{RD}$ goes low-level status information in the internal register of the M5M82C59AP-2 can be read through the data bus.

Address Input (A_0)

The address input is normally connected with one of the address lines and is used along with $\overline{WR}$ and $\overline{RD}$ to control write commands and reading status information.

Cascade Buffer/Comparator

The cascade buffer/comparator stores or compares identification codes. The three cascade lines are output when the M5M82C59AP-2 is a master or input when it is a slave. The identification code on the cascade lines select it as master or slave.

PROGRAMMING THE M5M82C59AP-2

The M5M82C59AP-2 is programmed through the Initialization Command Word (ICW) and the Operation Command Word (OCW). The following explains the functions of these two commands.

Initialization Command Words (ICW_S)

The initialization command word is used for the initial setting of the M5M82C59AP-2. There are four commands in this group and the following explains the details of these four commands. The command flow of ICWs is shown Fig. 2.

ICW1

The meaning of the bits of ICW1 is explained in Fig. 3 along with the functions. ICW1 contains vectored address bits $A_7 \sim A_5$, a flag indicating whether interrupt input is edge triggered or level triggered, CALL address interval, whether a single M5M82C59AP-2 or the cascade mode is used, and whether ICW4 is required or not.

Whenever a command is issued with $A_0 = 0$ and $D_4 = 1$, this is interpreted as ICW1 and the following will automatically occur.

(a) The interrupt mask register (IMR) is cleared.

(b) The interrupt request input IR_7 is assigned the lowest priority.

(c) The special mask mode is cleared and the status read is set to the interrupt request register (IRR).

(d) When IC4=0 all bits in ICW4 are set to 0.

ICW2

ICW2 contains vectored address bits $A_{15} \sim A_8$ or interrupt type $T_7 \sim T_3$, and the format is shown in Fig. 3.

ICW3

When SNGL = 1 it indicates that only a single M5M82C59AP-2 is used in the system, in which case ICW3 is not valid. When SNGL = 0, ICW3 is valid and indicates cascade connections with other M5M82C59AP-2 devices. In the master mode, a 1 is set for each slave.

When the CPU is a MELPS85 the CALL instruction is released from the master at the first $\overline{INTA}$ pulse and the vectored address is released onto the data bus from the slave at the second and third $\overline{INTA}$ pulses.

When the CPU is a MELPS86 the master and slave are in high-impedance at the first $\overline{INTA}$ pulse and the pointer is

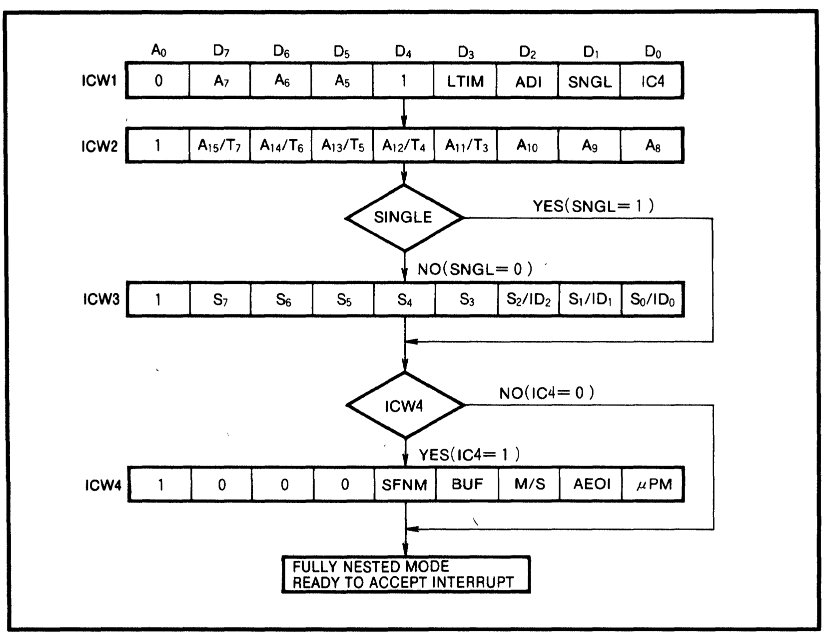


Fig. 2 Initialization sequence

released onto the data bus from the slave at the second $\overline{INTA}$ pulse.
The master mode is specified when $\overline{SP}/\overline{EN}$ pin is high-level or BUF=1 and M/S=1 in ICW4, and slave mode is specified when $\overline{SP}/\overline{EN}$ pin is low-level or BUF=1 and M/S=0 in ICW4. In the slave mode, 3-bit $ID_2 \sim ID_0$ identify the slave. And then when the slave code released on the cascade lines from the master, matches the assigned ID code, the vectored address is released by it onto the data bus at the next $\overline{INTA}$ pulse

ICW4

Only when IC4=1 in ICW1 is ICW4 valid. Otherwise all bits are set to 0. When ICW4 is valid it specifies special fully nested mode, buffer mode master/slave, automatic EOI and microprocessor mode. The format of ICW4 is shown in Fig. 3.

Operation Command Words (OCW_S)

The operation command words are used to change the contents of IMR, the priority of interrupt request inputs and the special mask. After the ICW are programmed into the M5M82C59AP-2, the device is ready to accept interrupt requests. There are three types of OCW_S; explanation of each follows, and the format of OCW_S is shown in Fig 4

OCW1

The meaning of the bits of OCW1 are explained in Fig. 4 along with their functions. Each bit of IMR can be indepen-

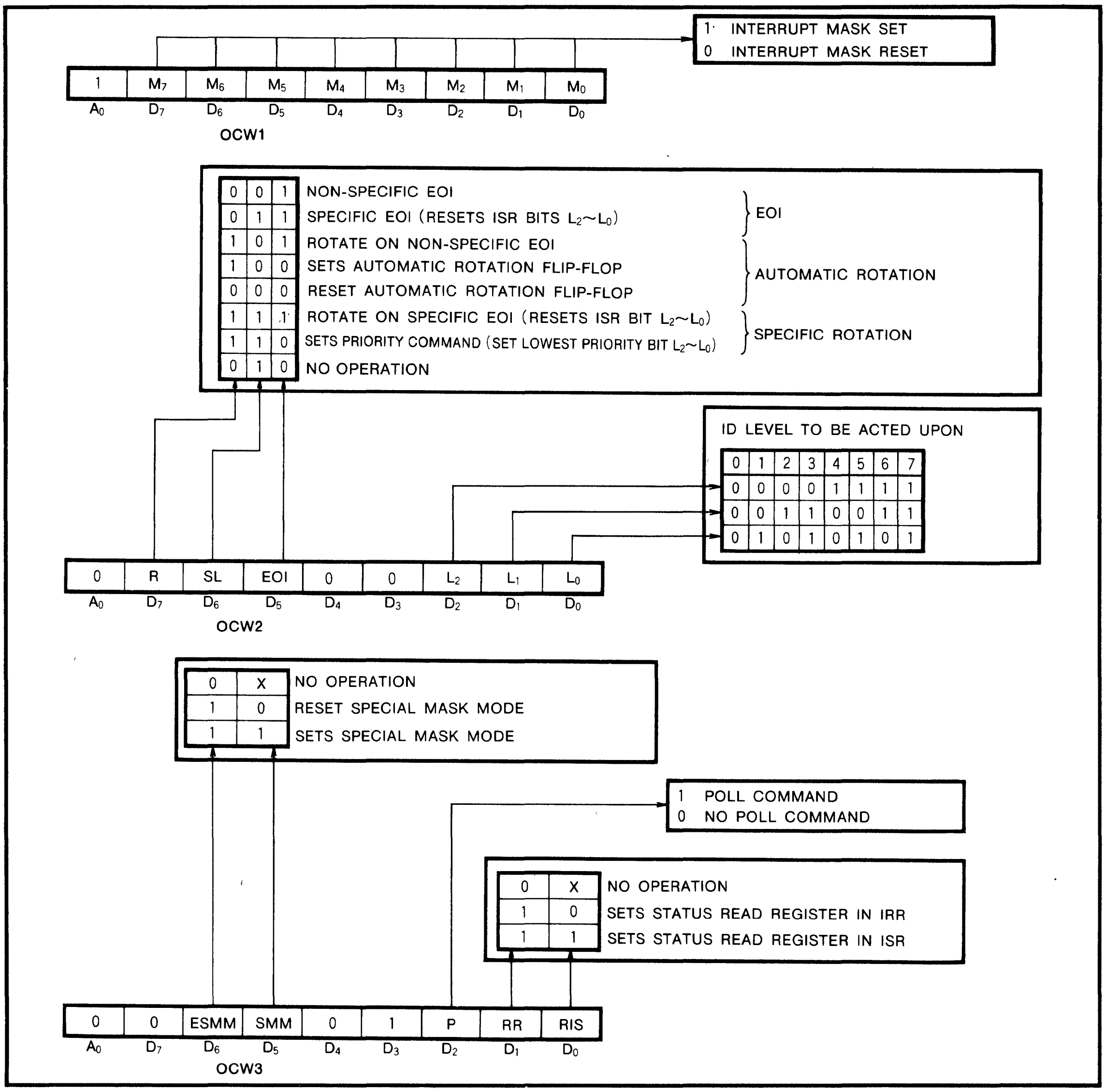


Fig. 4 Operation command word format

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of those that are set. Other ISR bits are reset by a specific EOI and the bit to be reset is specified in the EOI by the program. The SEOI is useful in modes other than fully nested mode. When the M5M82C59AP-2 is in special mask mode ISR bits masked in IMR are not reset by EOI. EOI and SEOI are selected when OCW2 is executed.

Automatic EOI (AEOI)

In the AEOI mode the M5M82C59AP-2 executes non-specific EOI command automatically at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI = 1 in ICW4, the M5M82C59AP-2 is put in AEOI mode continuously until re-programmed in ICW4.

Automatic rotation

The automatic rotation mode is used in applications where many interrupt requests of the same level are expected such as multichannel communication systems In this mode when an interrupt request is serviced, that request is assigned the lowest priority so that if there are other interrupt requests they will have higher priorities. This means that the next request on the interrupt request being serviced must wait until the other interrupt requests are serviced (worst case is waiting for all 7 of the other controllers to be serviced). The priority and serving status are rotated as shown in Fig. 5.

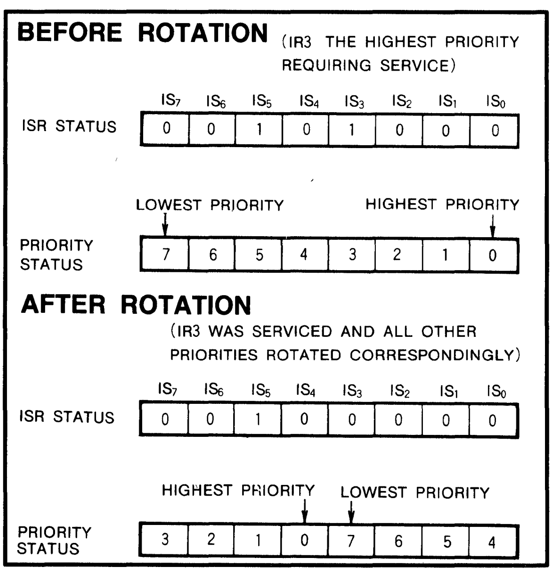


Fig. 5 An example of priority rotation

In the non-specific EOI command automatic rotation mode is selected when R=1, EOI=1, SL=0 in OCW2. The internal priority status is changed by EOI or AEOI commands. The rotation priority A flip-flop is set by R=1, EOI=0 and SL=0 which is useful when the M5M82C59AP-2 is used in the AEOI mode.

Specific rotation

Specific rotation gives the user versatile capabilities in interrupt controlled operations. It serves in those applications in which a specific device's interrupt priority must be altered. As opposed to automatic rotation which automatically sets priorities, specific rotation is completely user controlled. That is, the user selects the interrupt level that is to receive lowest or highest priority. Priority changes can be executed during an EOI command.

Level triggered mode/Edge triggered mode

Selection of level or edge triggered mode of the M5M82C59AP-2 is made by ICW1, When using edge triggered mode not only is a transition from low-level to high-level required, but the high-level must be held until the first $\overline{INTA}$. If the high-level is not held until the first $\overline{INTA}$, the interrupt request will be treated as if it were input on IR_7, except that the ISR bit is not set. When level triggered mode is used the functions are the same as edge triggered mode except that the transition from low-level to high-level is not required to trigger the interrupt request.

In the level triggered mode and using AEOI mode together, if the high-level is held too long the interrupt will occur immediately. To avoid this situation interrupts should be kept disabled until the end of the service routine or until the IR input returns low-level. In the edge triggered mode this type of mistake is not possible because the interrupt request is edge triggered.

Reading the M5M82C59AP-2 internal status

The contents of IRR and ISR can be read by the CPU with status read. When an OCW3 is issued to the M5M82C59AP-2 and an $\overline{RD}$ pulse issued the contents of IRR or ISR can be released onto the data bus. A special command is not required to read the contents of IMR. The contents of IMR can be released onto the data bus by issuing an $\overline{RD}$ pulse when A_0=1. There is no need to issue a read register command every time the IRR or ISR is to be read. Once a read register command is received by the M5M82C59AP-2, it remains valid until it is changed. Remember that the programmer must issue a poll command every time to check whether there is an interrupt request and read the priority level. Polling overrides status read when P=1, RR=1 in OCW3.

CASCADING

The M5M82C59AP-2 can be interconnected in a system of one master with up to 8 slaves to handle up to 64 priority levels. A system of 3 units that can be used with the MELPS85 is shown in Fig. 6.

The master can select a slave by outputting its identification code through the 3 cascade lines. The INT output of each slave is connected to the master interrupt request inputs. When an interrupt request of one of the slaves is to be serviced the master outputs the identification code of the slave through the cascade lines, so the slave will release the vectored address on the next $\overline{INTA}$ pulse.

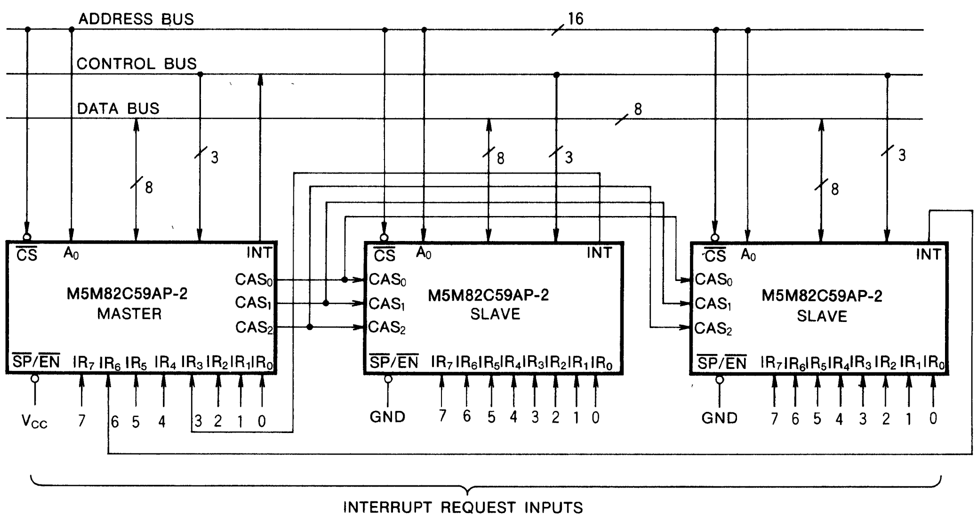
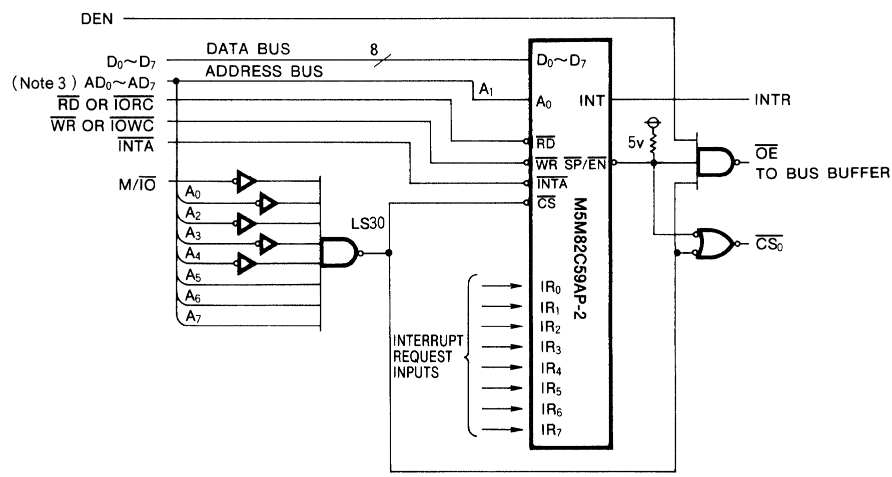


Fig. 6 Cascading the M5M82C59AP-2



Note 3 : $D_0 \sim D_7$ of the M5M82C59AP-2 are direct connected with $AD_0 \sim AD_7$ of the MELPS86

Fig. 7 Example of interface with the MELPS86

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.3∼7	V
V_I	Input voltage		−0.3∼V_{CC}+0.3	V
V_O	Output voltage		−0.3∼V_{CC}+0.3	V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current	2.5	mA
T_{opr}	Operating free-air temperature range		−20∼75	℃
T_{stg}	Storage temperature range		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼75℃, unless otherwise noted)

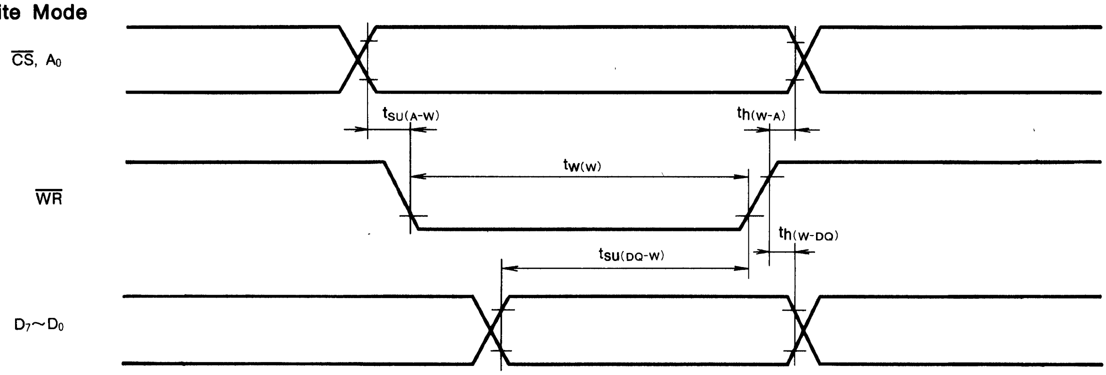
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (Ta=−20∼75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

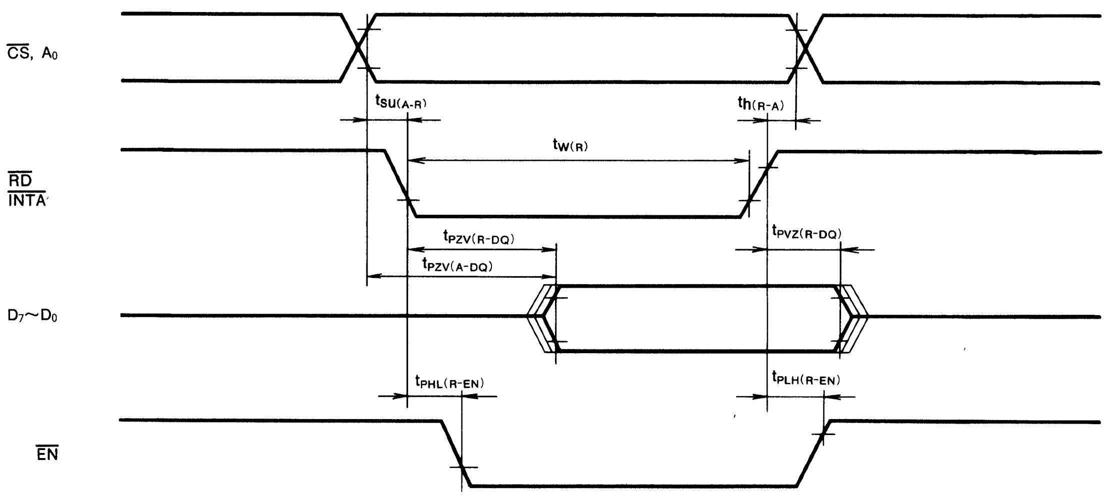
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	2.4			V
		I_{OH}=−100μA	3.5			
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Standby supply current from V_{CC}	V_I=0V, V_{CC} output open			10	μA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V∼V_{CC}	−10		10	μA
I_{LIR1}	IR pin input current	V_I=0V	−300			μA
I_{LIR2}	IR pin input current	V_I=V_{CC}			10	μA
Ci	Input capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$Ci_{/O}$	Input/output capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

TIMING DIAGRAM

Write Mode



Read Mode



CMOS PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5M82C255ASP is a LSI equivalent to two M5M82C55AP-2. It is housed in a single 64-pin shrink DIP. The M5M82C255ASP is fabricated using silicon-gate CMOS technology for a single supply voltage. This LSI is a simple input and output interface for TTL circuits, having 48 input/output pins which correspond to six 8-bit input/output ports.

FEATURES

- Single 5V supply voltage
- Input : TTL compatible (I_{OL}=2.5mA)
  Output : CMOS/TTL compatible
- Each I/O pin has ±4mA driving capability
- Read access time : 120ns
- Timing specification enable easy design of system bus timing
- Noise limiter is built-in to provide high noise margin (RESET, $\overline{ACK}$, $\overline{STB}$)
- 48 programmable I/O pins
- Direct bit set/reset capability
- 64-pin shrink DIL package (lead pitch 0.07 inch) is used for easy mounting

APPLLICATION

Input/output ports for microprocessor

FUNCTION

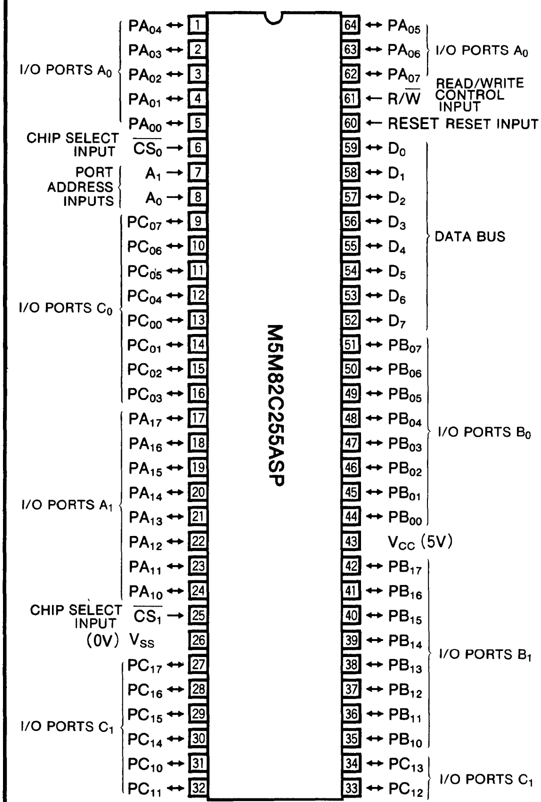
A Block diagram of the M5M82C255ASP is shown in the following page. The M5M82C255ASP consists of block 0 and block 1 each of which is functionally equivalent to the M5M82C55AP-2. Block 0 and block 1 have independent chip select inputs $\overline{CS_0}$ and $\overline{CS_1}$, and independent ports PA_0, PB_0, PC_0, PA_1, PB_1 and PC_1. The 8-bit data bus, address inputs A_0 and A_1, and the RESET input are shared by block 0 and block 1. The CPU's $\overline{RD}$ signal and $\overline{WR}$ signal must be multiplexed to generate the R/$\overline{W}$ signal.

The 48 I/O pins consist of two blocks each with two 12-bit sub blocks A and B. All four blocks can be programmed independently by three mode control commands from the CPU.

In mode 0, four 8-bit I/O ports and four 4-bit I/O ports are available for use as output ports. In mode 1, the 24 I/O pins of each block are divided into groups A and B. In each group, 8 bits are used for input or output data ports. And 4 bits are used for control data ports. In mode 2, 8 bits of group A are used as a bidirectional bus with a 5-bit control signal.

Any of the 8 data bits at port C of each block can set or reset. When reset input (RESET) is high, all ports are set to the input mode (high-impedance state).

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

FUNCTIONAL DESCRIPTION

Block 0 has the same function as block 1. Therefore, block 0 is explained in the following.

R/$\overline{W}$ (Read/Write) Input

Read function operates when the R/$\overline{W}$ is high-level, and data input at the port is transferred to the CPU. Write function operates when the R/$\overline{W}$ is low-level, and data or control from the CPU are written.

A_0, A_1 (Port address) Input

These input signals are used to select one of the three ports: port A, port B, and port C, or the control register. They are normally connected to the least significant two bits of the address bus.

RESET (Reset) Input

At high-level, the control register is cleared. Then all ports are set to the input mode (high-impedance state).

$\overline{CS_0}$, $\overline{CS_1}$ (Chip-Select) Input

At low-level, the communication between M5M82C255ASP and the CPU is enabled. When $\overline{CS_0}$ is low-level block 0 is selected, and when $\overline{CS_1}$ is low-level, block 1 is selected. When $\overline{CS_0}$ and $\overline{CS_1}$ are both high-level, the data bus maintains high impedance state and control from the CPU is ignored. In modes 0 or 1, the previous data is stored.

Read/Write Control Logic

The function of this block is to control transfers of both data and control words. It accepts the address signals (A_0, A_1, $\overline{CS_0}$, $\overline{CS_1}$), I/O control signals (R/$\overline{W}$) and RESET signal, and then issues commands to both of the control groups.

Data Bus Buffer

This three-state, bidirectional, 8-bit buffer is used to transfer the data when an input or output instruction is executed by the CPU. Control words and status information are also transferred through the data bus buffer.

Group A and Group B Control

Accepting commands from the read/write control logic, the control blocks (Group A, Group B) receive 8 bit control words from the internal data bus and issue the proper commands for the associated ports. Control group A is associated with port A and the 4 high-order bits of port C. Control group B is associated with port B and the 4 low-order bits of port C. The control register, which stores control words, can only be written into.

Port A, Port B and Port C

M5M82C255ASP contains six 8-bit ports whose modes and input/output settings are programmed by the system software.

Port A has an output latch/buffer and an input latch/buffer. Port B has an input-output latch/buffer. Port C has an output latch/buffer and an input buffer. Port C can be divided into two 4-bit ports which can be used as ports for control signals for port A and port B.

The basic operations are shown in Table 1.

Table 1 Basic Operations

A_1	A_0	$\overline{CS_0}$	$\overline{CS_1}$	R/$\overline{W}$	Operation
0	0	L	H	H	Data bus ← Port A_0
0	0	H	L	H	Data bus ← Port A_1
0	1	L	H	H	Data bus ← Port B_0
0	1	H	L	H	Data bus ← Port B_1
1	0	L	H	H	Data bus ← Port C_0
1	0	H	L	H	Data bus ← Port C_1
0	0	L	H	L	Port A_0 ← Data bus
0	0	H	L	L	Port A_1 ← Data bus
0	1	L	H	L	Port B_0 ← Data bus
0	1	H	L	L	Port B_1 ← Data bus
1	0	L	H	L	Port C_0 ← Data bus
1	0	H	L	L	Port C_1 ← Data bus
1	1	L	H	L	Control register 0 ← Data bus
1	1	H	L	L	Control register 1 ← Data bus
X	X	H	H	X	Data bus is high-impedance state
1	1	L	H	H	illegal condition
1	1	H	L	H	

CPU INTERFACE

Fig. 1 shows an application with the M5L8085AP as the CPU. In this figure, the M5M82C255ASP is mapped in the I/O space, but it could also be mapped in the memory space. The following description applies to the circuit in the Fig. 1. Characteristics are shown in Figs. 2, 3 and 4.

Chip select signal

The M5M82C255ASP chip select signal ($\overline{CS_0}$, $\overline{CS_1}$) is the logical product of the IO・RD (IO・WR) signal derived from the read (write) signal and IO/$\overline{M}$ signal from the CPU, and the address decoder output generated by decoding the address. Therefore, the timing of chip select signal ($\overline{CS_0}$, $\overline{CS_1}$) is delayed from that of IO・RD (IO・WR) signal. The chip select signals $\overline{CS_0}$ and $\overline{CS_1}$ must not be active simultaneously.

Read operation

The read operation of M5M82C255ASP starts when $\overline{\overline{RD}}$・$\overline{\overline{CS}}$ = 1, just as with the M5M82C55AP-2. When the M5L8085AP CPU enters into I/O read operation, the M5M-82C255ASP R/$\overline{W}$ signal, obtained by inverting the IO・WR signal, is kept at high-level. The actual read operation starts when the chip select signal is activated by the IO・RD signal and address decoder output. The access time of the M5M82C255ASP is specified by the falling edge of the chip select signal, and is defined as $t_{PZV(CS-DQ)}$. Fig. 3 shows the read timing. The delay time (marked by *) extends from the time when the $\overline{RD}$ signal of CPU becomes active until the chip select signal becomes active. It is obtained by adding the delay time of LS02 and LS51 in Fig. 1. Table 2 shows the gate delay time of LS02, LS51, LS04 and LS00 used in the circuit of Fig. 1. The sum of the gate delay times of LS02 and LS51 is 35ns, after which the actual read operation starts. The access time of the M5M82C255ASP is 120ns maximum, so the total access time is 155ns maximum. As the access time of the M5M82C255ASP is specified by the falling edge of the chip select signal, care must be taken when connecting the M5M82C255ASP to a high-speed microprocessor.

The address(Note) setup time and hold time of the M5M82C-55AP-2 read signal are defined as $t_{SU(A-R)}$ and $t_{h(R-A)}$ but, in the M5M82C255ASP, they are defined as $t_{SU(A_i-CS)}$ and $t_{h(CS-A_i)}$ due to above reason, where A_i means address inpus of A_0 or A_1. The time is specified to be 0ns minimum for each.

Note The term "address" used in describing the address setup time and address hold time of M5M82C55AP-2 means the address inputs A_0, A_1 and $\overline{CS}$

Write operation

Fig. 4 shows the write timing. The phase relationship of the R/$\overline{W}$ and chip select signals is marked by an★. For the M5M82C55AP-2, the phase relationship is defined as the address(Note) setup time $t_{SU(A-W)}$ (or t_{AW}) before $\overline{WR}$, and is specified to be 0ns minimum. In the M5M82C255ASP, however, the phase relationship is reversed by the circuit which generates the control signal (See Fig. 1), when the chip select signal becomes active after the R/$\overline{W}$ signal goes low-level. Therefore, we have discarded the previous definition. The phase difference of write signal and chip select signal is defined as $t_{SU(CS-W)}$ and specified as 0ns maximum and −30ns minimum. The phase difference of the write signal and address inputs of A_0 and A_1 is defined as $t_{SU(A_i-W)}$ and the minimum value is −30ns.

This means that the address inputs of A_0 and A_1 and the chip select signal must become stable within 30ns after the R/$\overline{W}$ signal goes low-level. The signals A_0 and A_1 can become stable before R/$\overline{W}$ goes low-level, but the chip select signal must be activated after the R/$\overline{W}$ signal goes low-level. This is required because, if the chip select signal is active before R/$\overline{W}$ signal, the R/$\overline{W}$ signal will be high-level, causing the M5M82C255ASP to enter the read operation. The address inputs of A_0 and A_1 will write properly as long as the minimum value is −30ns.

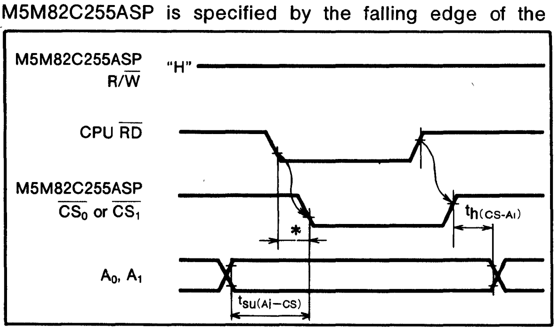


Fig. 3 Read operation of the M5M82C255ASP

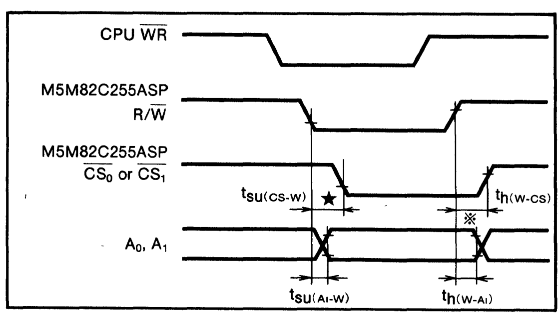


Fig. 4 Write operation of the M5M82C255ASP

Table 2 Gate delay time

Type	LS02		LS51		LS04		LS00		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	6	15	6	20	6	15	6	15	nsec
t_{PHL}	6	15	8	20	6	15	6	15	nsec

(Refer to the Bipolar Digital ICs Section of Mitsubishi Semiconductor Handbook)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3～7		V
V_I	Input voltage		−0.3～V_{CC}+0.3		V
V_O	Output voltage		−0.3～V_{CC}+0.3		V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	Port	−4	mA
			Data bus	−500	μA
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.	Port	4	mA
			Data bus	2.5	mA
Topr	Operating temperature range		−20～75		℃
Tstg	Storage temperature		−65～150		℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

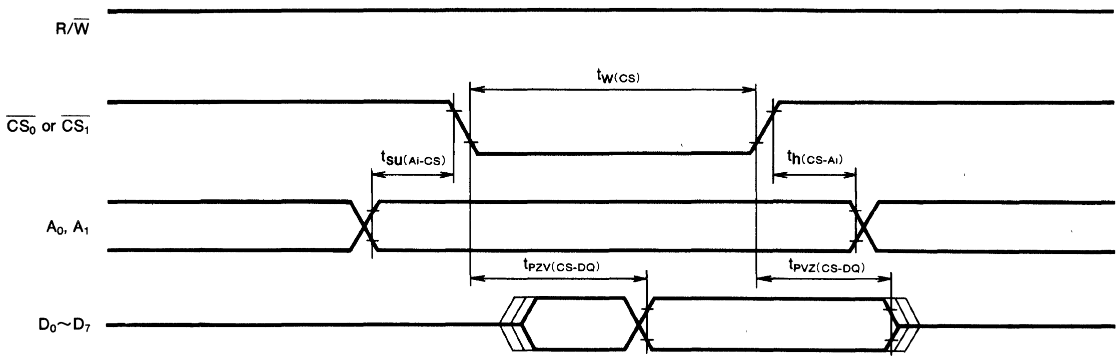
ELECTRICAL CHARACTERISTICS (T_a = −20～75℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage (Note 2)	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage (Note 2)	I_{OL}=2.5mA			0.4	V
I_{CC}	Supply current	All Input Mode RESET=0V, Other Pins=V_{CC}			10	μA
I_{IL}	Input leak current	V_I=0V, V_{CC}			±10	μA
I_{OZ}	Off-state output current	V_O=0V～V_{CC}			±10	μA
C_i	Input capacitance	f=1MHz, 25mVrms, T_a=25℃			10	pF
$C_{I/O}$	I/O capacitance	0V except test pins			30	pF

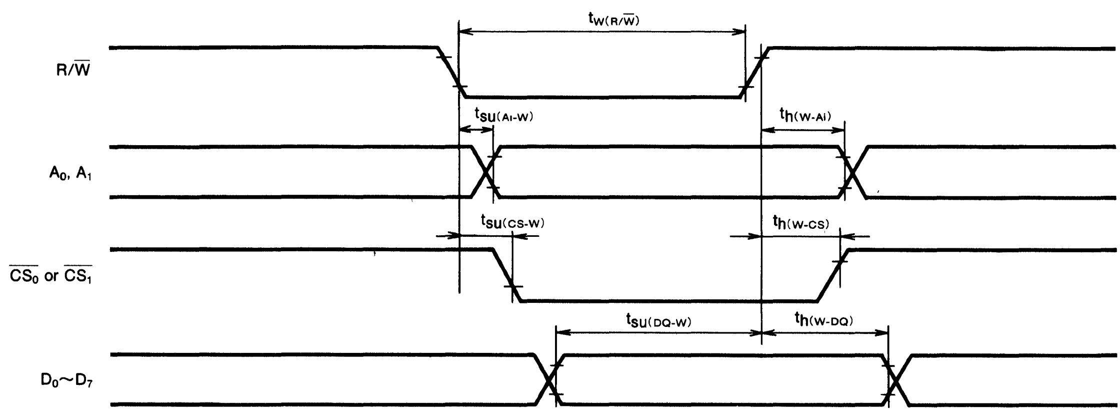
Note 1 : Current flowing into an IC is positive (no sign).
2 : The maximum value of the output current should be held within ±4mA at each port pin.

TIMING DIAGRAM

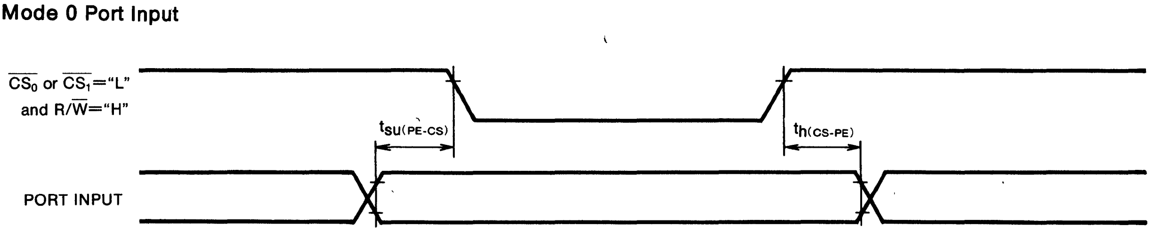
Data Bus Read Timing



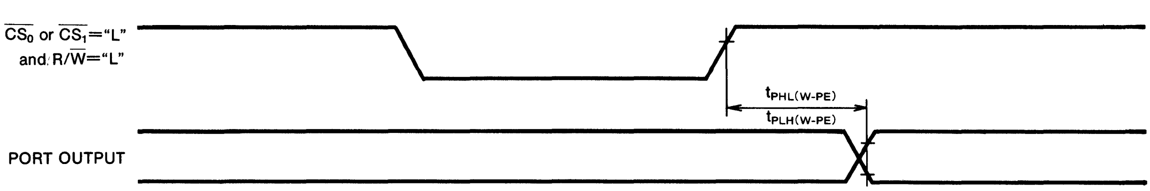
Data Bus Write Timing



Mode 0 Port Input



Mode 0, 1 Port Output



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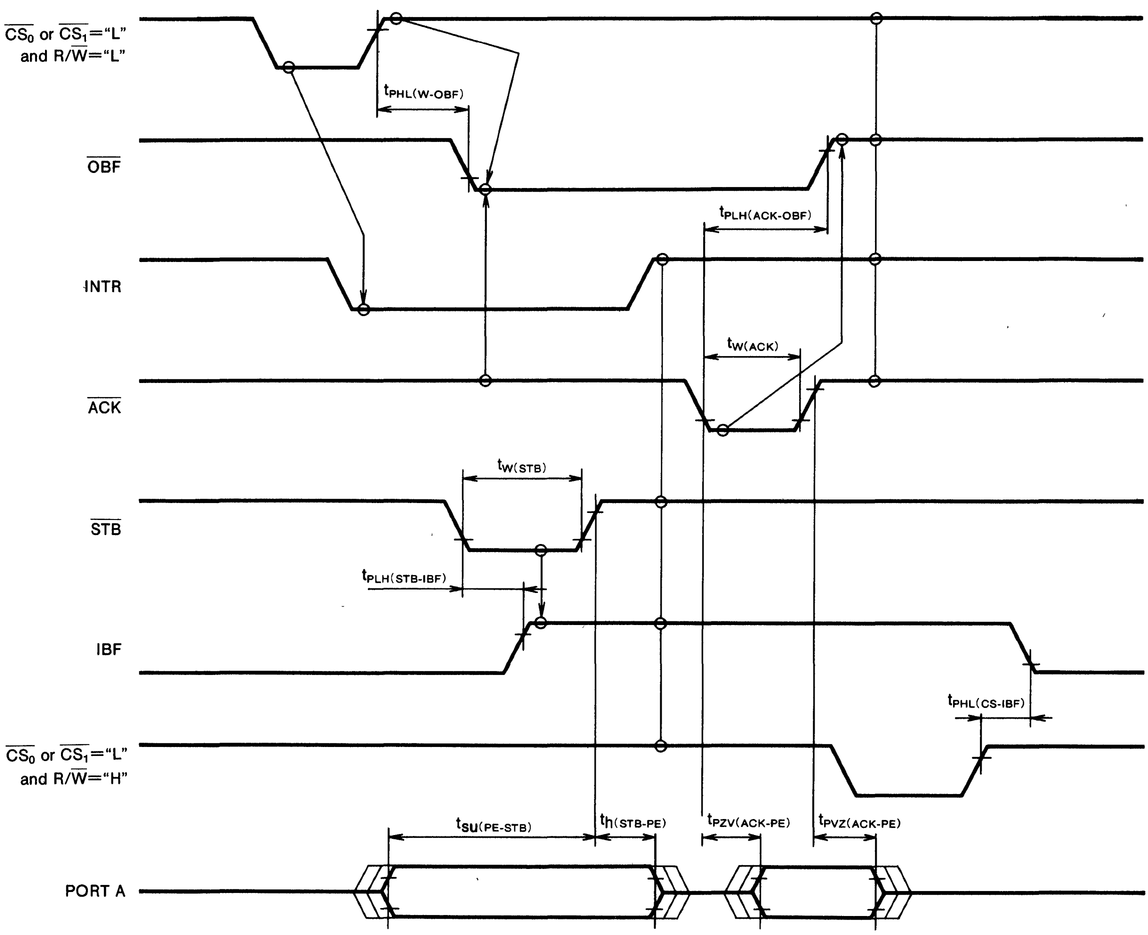
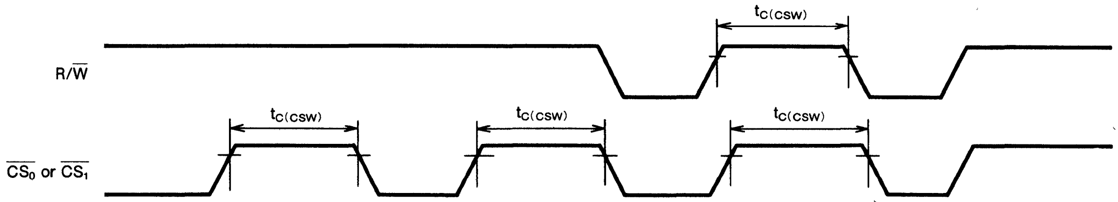
Mode 2 Bidirectional



Note 5 : INTR=IBF·$\overline{MASK}$·$\overline{STB}$·$\overline{CS_0}$ or $\overline{CS_1}$+$\overline{OBF}$·$\overline{MASK}$·$\overline{ACK}$·R/$\overline{W}$



OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals ($\overline{\text{CE}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, IO/$\overline{\text{M}}$, ALE and RESET) from CPU.

Bidirectional Address/Data Bus (AD_0~AD_7)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{\text{M}}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{\text{RD}}$) or write input ($\overline{\text{WR}}$).

Chip Enable Input ($\overline{\text{CE}}$)

When $\overline{\text{CE}}$ is at low-level, the address information on address/data bus is stored in the M5L8155P.

Read Input ($\overline{\text{RD}}$)

When $\overline{\text{RD}}$ is at low-level, the data bus buffer is active. If IO/$\overline{\text{M}}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{\text{M}}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{\text{WR}}$)

When $\overline{\text{WR}}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{\text{M}}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{\text{M}}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5L8155P on the falling edge of ALE along with the levels of $\overline{\text{CE}}$ and IO/$\overline{\text{M}}$.

IO/Memory Input (IO/$\overline{\text{M}}$)

When IO/$\overline{\text{M}}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA_0~PA_7)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB_0~PB_7)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC_0~PC_5)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{\text{B STB}}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{\text{A STB}}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (3MHz max.)

Timer Output ($\overline{\text{TIMER OUT}}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8 bits)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000).

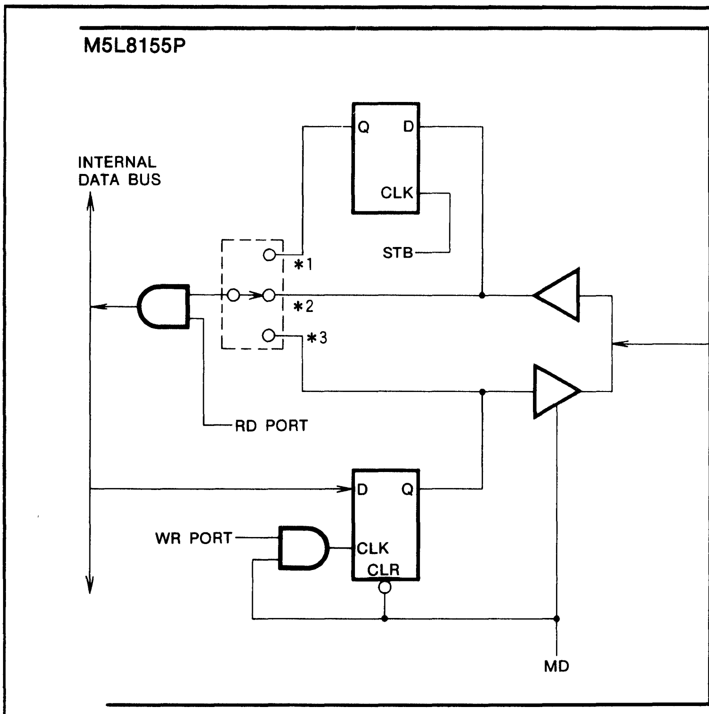
Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1: Output port A 0: Input port A
1	PB	PORT B I/O SET	1: Output port B 0: Input port B
2	PC_1	PORT C SET	00: ALT1 11: ALT2 01: ALT3 10: ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1. Enable interrupt 0. Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1. Enable interrupt 0. Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00: No influence on counter/timer operation 01: Counter/timer operation discontinued (If not already stopped) 10: Counter/timer operation discontinued after the current counter/timer operation is completed 11: Counter/timer operation started	
7	TM2		

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A and B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.



Note 1. WR PORT=IO/$\overline{M}$·WR·CE (PORT ADDRESS SELECTED)
2. RD PORT=IO/$\overline{M}$·RD·CE (PORT ADDRESS SELECTED)
3. MULTIPLEX CONTROL
*1 STROBE INPUT MODE
*2 INPUT MODE
*3 OUTPUT MODE
4. MD= 1 : OUTPUT MODE
0 : INPUT MODE

Fig. 1 Configuration for 1 bit of port A or B

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

Table 5 Basic functions of I/O ports

Address	$\overline{RD}$	$\overline{WR}$	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
$\overline{STB}$	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0~13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FFF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

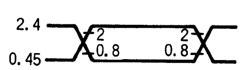
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su(A-L)}$	Address setup time before latch		50			ns
$t_{h(L-A)}$	Address hold time after latch		80			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		100			ns
$t_{w(L)}$	Latch pulse width		100			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		20			ns
$t_{w(RW)}$	Read/write pulse width		250			ns
$t_{su(DQ-W)}$	Data setup time before write		150			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{c(RW)}$	Read/write cycle time		300			ns
$t_{su(P-R)}$	Port setup time before read		70			ns
$t_{h(R-P)}$	Port hold time after read		50			ns
$t_{w(STB)}$	Strobe pulse width		200			ns
$t_{su(P-STB)}$	Port setup time before strobe		50			ns
$t_{h(STB-P)}$	Port hold time after strobe		120			ns
$t_{w(\phi H)}$	Timer input high-level pulse width		120			ns
$t_{w(\phi L)}$	Timer input low-level pulse width		80			ns
$t_{c(\phi)}$	Timer input cycle time		320		DC	ns
$t_{r(\phi)}$	Timer input rise time				30	ns
$t_{f(\phi)}$	Timer input fall time				30	ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted.)

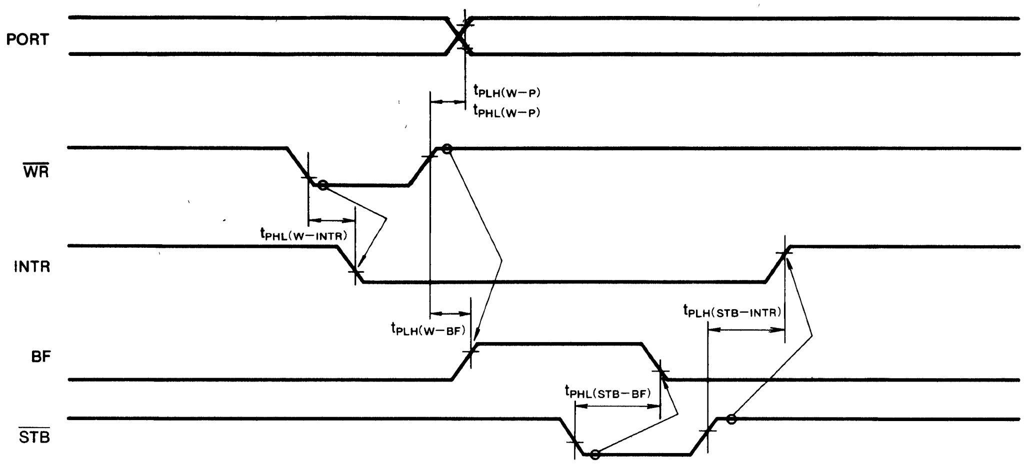
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			170	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				400	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		100	ns
$t_{PHL(W-P)}$ $t_{PLH(W-P)}$	Propagation time from write to data output				400	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				400	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				400	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				400	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				400	ns
$t_{PHL(\phi-OUT)}$ $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				400	ns

Note 6 : Test conditions are not applied.
7 : A.C Testing waveform

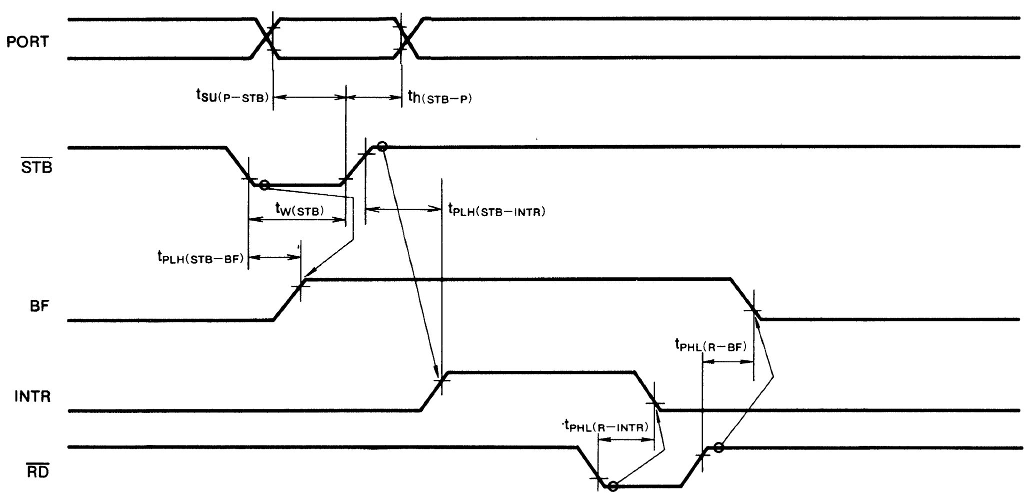
Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



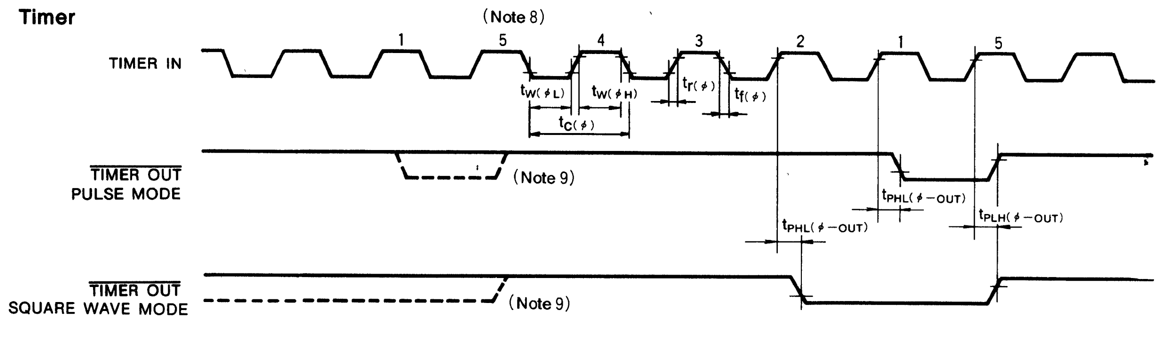
Strobed Output



Strobed Input



Timer



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output.

OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals (CE, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE and RESET) from CPU.

Bidirectional Address/Data Bus ($AD_0 \sim AD_7$)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input (CE)

When CE is at high-level, the address information on address/data bus is stored in the M5L8156P.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5L8156P on the falling edge of ALE along with the levels of CE and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A ($PA_0 \sim PA_7$)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B ($PB_0 \sim PB_7$)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C ($PC_0 \sim PC_5$)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC_5	$\overline{B\ STB}$	(port B strobe)
PC_4	B BF	(port B buffer full)
PC_3	B INTR	(port B interrupt)
PC_2	$\overline{A\ STB}$	(port A strobe)
PC_1	A BF	(port A buffer full)
PC_0	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (3MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8 bits)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of the mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000).
Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1: Output port A 0: Input port A
1	PB	PORT B I/O SET	1. Output port B 0· Input port B
2	PC_1	PORT C SET	00. ALT1 11. ALT2 01. ALT3 10· ALT4
3	PC_2		
4	IEA	PORT A INTERRUPT ENABLE FLAG	1. Enable interrupt 0: Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1· Enable interrupt 0: Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00. No influence on counter/timer operation 01. Counter/timer operation discontinued (If not already stopped) 10: Counter/timer operation discontinued after the current counter/timer operation is completed 11: Counter/timer operation started	
7	TM2		

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A and B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.

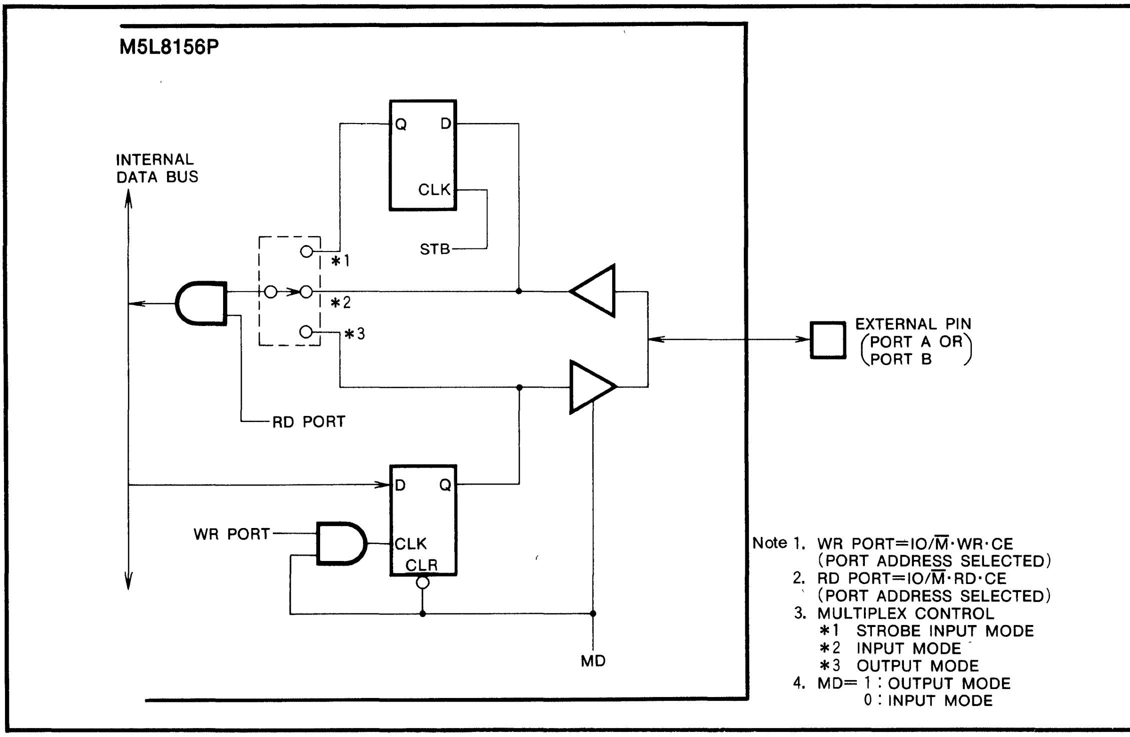


Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	RD	WR	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
STB	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0 ~ 13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5 V ± 5 %, V_{SS} = 0V, unless otherwise noted)

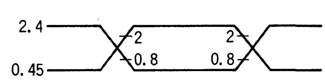
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(A-L)}$	Address setup time before latch		50			ns
$t_{h(L-A)}$	Address hold time after latch		80			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		100			ns
$t_{w(L)}$	Latch pulse width		100			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		20			ns
$t_{w(RW)}$	Read/write pulse width		250			ns
$t_{su(DQ-W)}$	Data setup time before write		150			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{C(RW)}$	Read/write cycle time		300			ns
$t_{su(P-R)}$	Port setup time before read		70			ns
$t_{h(R-P)}$	Port hold time after read		50			ns
$t_{w(STB)}$	Strobe pulse width		200			ns
$t_{su(P-STB)}$	Port setup time before strobe		50			ns
$t_{h(STB-P)}$	Port hold time after strobe		120			ns
$t_{w(\phi H)}$	Timer input high-level pulse width		120			ns
$t_{w(\phi L)}$	Timer input low-level pulse width		80			ns
$t_{C(\phi)}$	Timer input cycle time		320		DC	ns
$t_{r(\phi)}$	Timer input rise time				30	ns
$t_{f(\phi)}$	Timer input fall time				30	ns

SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5 V ± 5 %, V_{SS} = 0V, unless otherwise noted.)

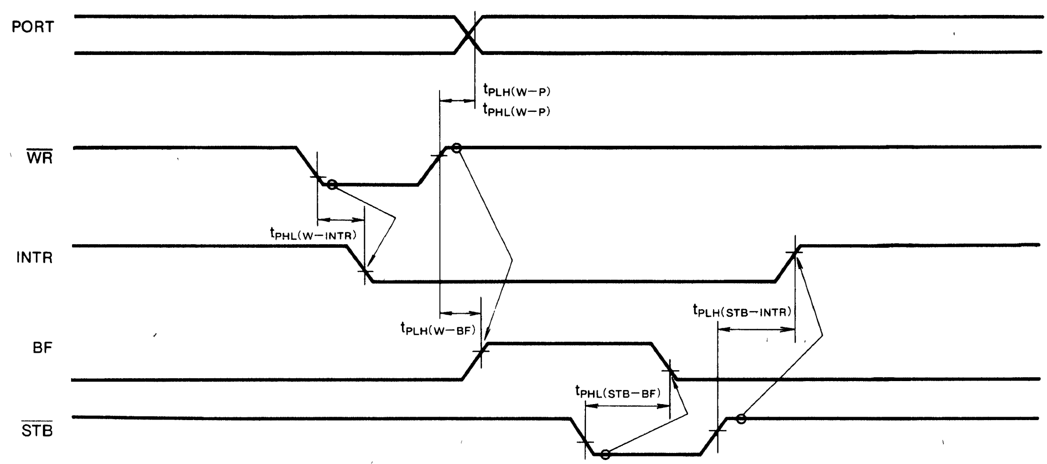
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to data output	C_L = 150pF			170	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				400	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		100	ns
$t_{PHL(W-P)}$ $t_{PLH(W-P)}$	Propagation time from write to data output				400	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag				400	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				400	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				400	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				400	ns
$t_{PHL(\phi-OUT)}$ $t_{PLH(\phi-OUT)}$	Propagation time from timer input to timer output				400	ns

Note 6 : Test conditions are not applied.
7 : A.C Testing waveform

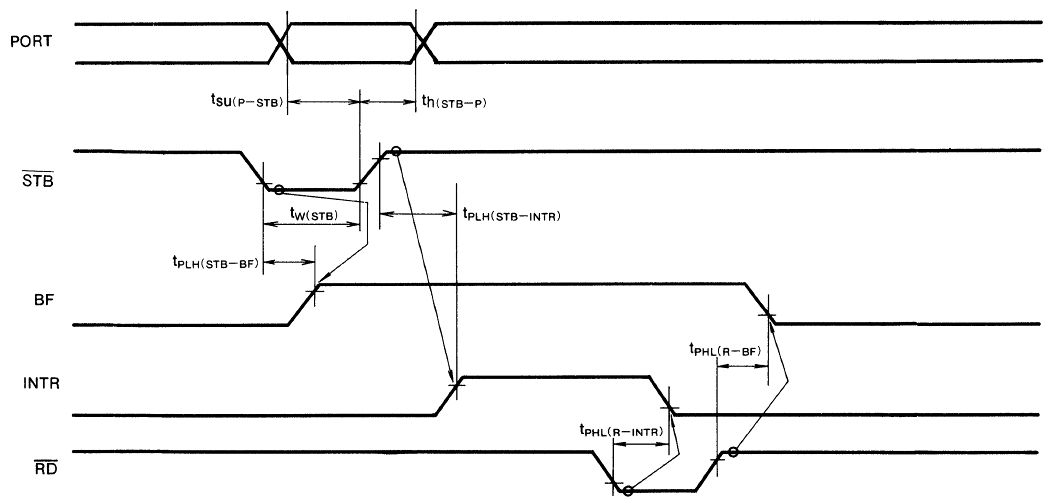
Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



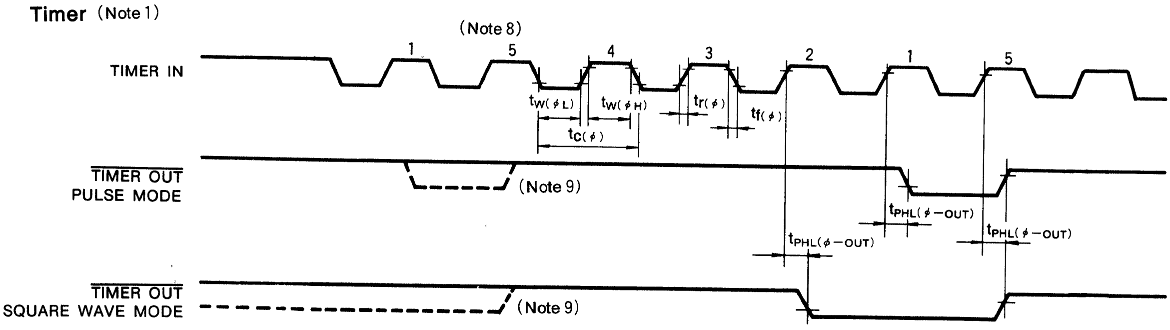
Strobed Output



Basic Input



Timer (Note 1)



Note 8 : The wave form is shown for the case of counting down from 5 to 1
9 : As long as the M1 mode flag of the timer register is at high-level, pulses are continuously output

OPERATION

The M5L8251AP-5 interfaces with the system bus as shown in Fig.1, positioned between the CPU and the modem or terminal equipment, and offers all the functions required for data communication.

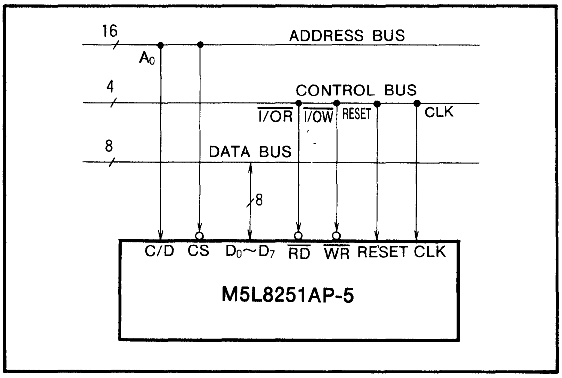


Fig. 1 M5L8251AP-5 interface to CPU system bus

When using the M5L8251AP-5, it is necessary to program, as the initial setting, assignments for synchronous/asynchronous mode selection, baud rate, character length, parity check, and even/odd parity selection in accordance with the communication system used. Once programming is completed, functions appropriate to the communication system can be carried out continuously.

When initial setting of the USART is completed, data communication becomes possible. Though the receiver is always in the enable state, the transmitter is placed in the transmitter-enable state (T_XEN) by a command instruction, and the application of a low-level signal to the $\overline{CTS}$ pin prompts data-transfer start-up. Until this condition is satisfied, transmission is not executed. On receiving data, the receiver informs the CPU that reading for the receiver data in the USART by the CPU has become possible (the R_XRDY terminal has turned to high-level). Since data reception and the entry of the CPU into the data-readable state are output as status information, the CPU can access USART status without accessing the R_XRDY terminal.

During receiving operation, the USART checks errors and gives out status information. There are three types of errors: parity, overrun, and frame. Even though an error occurs, the USART continues its operations, and the error state is retained until error reset (ER) is effected by a command instruction. The M5L8251AP-5 access methods are listed in Table 1.

Table 1 M5L8251AP-5 Access Methods

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
L	L	H	L	Data bus ← Data in USART
L	H	L	L	USART ← Data bus
H	L	H	L	Data bus ← Status
H	H	L	L	Control ← Data bus
X	H	H	L	3-State ← Data bus
X	X	X	H	3-State ← Data bus

Read/Write Control Logic

This logic consists of a control word register and command word register. It receives signals from the CPU control bus and generates internal-control signals for the elements.

Modem Control Circuit

This is a general-purpose control-signal circuit designed to simplify the interface to the modem. Four types of control signal are available: output signals $\overline{DTR}$ and $\overline{RTS}$ are controlled by command instructions, input signal $\overline{DSR}$ is given to the CPU as status information and input signal $\overline{CTS}$ controls direct transmission.

Data-Bus Buffer

This is an 8-bit 3-state bidirectional bus through which control words, command words, status information, and transfer data are transferred. Fig. 2 shows the structure of the data-bus buffer.

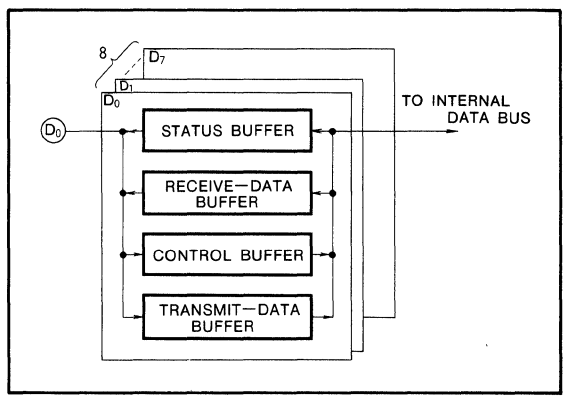


Fig. 2 Data-bus-buffer structure

Transmit Buffer

This buffer converts parallel-format data given to the data-bus buffer in to serial data with addition of a start bit, stop bits and a parity bit, and sends out the converted data through the T_XD pin based on the control signal.

Transmit-Control Circuit

This circuit carries out all the controls required for serial data transmission. It controls transmitter data and outputs the signals required by external devices in accordance with the instructions of the read/write control logic.

Clear-To-Send Input ($\overline{CTS}$)
When the T_XEN bit (D_0) of the command instruction has been set to 1 and the $\overline{CTS}$ input is low-level serial data is sent out from the T_XD pin. Usually this is used as a clear-to-send signal for the modem
Note: CTS indicates the modem status as follows:
ON means data transmission is possible;
OFF means data transmission is impossible.

Transmitter-Empty Output (T_XEMPTY)
When no transmisison characters are left in the transmit buffer, this pin enters the high-level state. In the asynchronous mode, the following transmission character is shifted to the transmit buffer when it is loaded from the CPU. Thus, it is automatically reset. In the synchronous mode, a SYNC character is loaded automatically on the transmit buffer when no transfer-data characters are left. In this case, however, the T_XEMPTY does not enter the low-level state when a SYNC character has been sent out, since T_XEMPTY="H" denotes the state in which there is no transfer character and one or two SYNC characters are being transferred or the state in which a SYNC character is being transferred as a filler. T_XEMPTY is unrelated to the T_XEN bit of the command instruction.

Transmission-Data Output (T_XD)
Parallel-format transmission characters loaded on the M5L8251AP-5 by the CPU are assembled into the format designated by the mode instruction and sent in serial-data form via the T_XD pin. Data is output, however, only in cases where the D_0 bit (T_XEN) of the command instruction is 1 and the $\overline{CTS}$ terminal is in the low-level state. Once reset, this pin is kept at the mark status (high level) until the first character is sent.

Clock Input (CLK)
This system-clock input is required for internal-timing generation and is usually connected to the clock-output (CLK) pin of the M5L8085AP. Although there is no direct relation with the data-transfer baud rate, the clock-input (CLK) frequency is more than 30 times the $\overline{T_XC}$ or $\overline{R_XC}$ input frequency in the case of the synchronous system and more than 4.5 times in the case of the asynchronous system.

Reset Input (RESET)
Once the USART is shifted to the idle mode by a high-level input, this state continues until a new control word is set Since this is a master reset, it is always necessary to load a control word following the reset process. The reset input requires a minimum 6-clock pulse width.

Data-Set Ready Input ($\overline{DSR}$)
This is a general-purpose input signal, but is usually used as a data-set ready signal to test modem status. Its status can be known from the status reading process. The D_7 bit of the status information equals 1 when the $\overline{DSR}$ pin is in the low-level state, and 0 when in the high-level state.
$\overline{DSR}$="L"→D_7 bit of status information=1
$\overline{DSR}$="H"→D_7 bit of status information=0
Note: DSR indicates modem status as follows:
ON means the modem can transmit and receive;
OFF means it cannot.

Request-To-Send Output ($\overline{RTS}$)
This is a general-purpose output signal but is used as a request-to-send signal for the modem. The $\overline{RTS}$ terminal is controlled by the D_5 bit of the command instruction. When D_5 is equal to 1, $\overline{RTS}$="L", and when D_5 is 0, $\overline{RTS}$="H".
Command register D_5=1→$\overline{RTS}$="L"
Command register D_5=0→$\overline{RTS}$="H"
Note: RTS controls the modem transmission carrier as follows:
ON means carrier dispatch;
OFF means carrier stop.

Data-Terminal Ready Output ($\overline{DTR}$)
This is a general-purpose output signal, but is usually used as a data-terminal ready or rate-select signal to the modem. The $\overline{DTR}$ pin is controlled by the D_1 bit of the command instruction; if D_1=1, $\overline{DTR}$="L", and if D_1=0, $\overline{DTR}$="H".
D_1 of the command register=1→$\overline{DTR}$="L"
D_1 of the command register=0→$\overline{DTR}$="H"

Receiver-Clock Input ($\overline{R_XC}$)
This clock signal controls the baud rate for the sending in of characters via the $\overline{R_XD}$ pin. The data is shifted in by the rising edge of the $\overline{R_XC}$ signal. In the synchronous mode, the $\overline{R_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by mode setting. This relationship is parallel to that of $\overline{T_XC}$, and in usual communication-line systems the transmission and reception baud rates are equal. The $\overline{T_XC}$ and $\overline{R_XC}$ terminals are, therefore, used connected to the same baud-rate generator.

PROGRAMMING
It is necessary for the M5L8251AP-5 to have the control word loaded by the CPU prior to data transfer. This must always be done following any resetting operation (by external RESET pin or command instruction IR). There are two types of control words: mode instructions specifying general operations required for communications and command instructions to control the M5L8251AP-5 actual operations.
Following the resetting operation, a mode instruction must be set first. This instruction sets the synchronous or asynchronous system to be used. In the sysnchronous system, a SYNC character is loaded from the CPU. In the case of the bi-sync system, however, a second SYNC character must be loaded in succession.
Loading a command instruction makes data transfer possible. This operation after resetting must be carried out for initializing the M5L8251AP-5. The USART command instruction contains an internal-reset IR instruction (D_6bit) that makes it possible to return the M5L8251AP-5 to its reset state. The initialization flowchart is shown in Fig. 3 and the mode-instruction and command-instruction formats are shown in Figs. 4 and 5.

Asynchronous Transmission Mode

When data characters are loaded on the M5L8251AP-5 after initial setting, the USART automatically adds a start bit (0), an odd or even parity bit specified by the mode instruction during initialization, and a specified number of stop bits (1). After that, the assembled data characters are transferred as serial data via the T_xD pin, if transfer is enabled ($T_xEN = 1 \cdot \overline{CTS} =$ "L"). In this case, the transfer data (baud rate) is shifted by the mode instruction at a rate of 1X, 1/16X, or 1/64X the $\overline{T_xC}$ period.

If the data characters are not loaded on the M5L8251AP-5, the T_xD pin enters a mark state ("H"). When SBRK is programmed by the command instruction, break characters (0) are output continuously through the T_xD pin.

Asynchronous Reception Mode

The R_xD line usually starts operations in a mark state ("H"), triggered by the falling edge of a low-level pulse when it comes to this line. This signal is again strobe at the middle of the bit to confirm that it is a perfect start bit. The detection of a second low-level indicates the validity of the start bit (again strobe is carried out only in the case of 16X and 64X). After that, the bit counter inside the M5L8251AP-5 starts operating; each bit of the serial information on the R_xD line is shifted in by the rising edge of $\overline{R_xC}$, and the data bit, parity bit (when necessary), and stop bit are sampled at the middle position.

The occurrence of a parity error causes the setting of a parity-error flag. If the stop bit is 0, a frame error flag is set. Attention should be paid to the fact that the receiver requires only one stop bit even though the program has designated 1/1.5 or 2 stop bits.

Reception up to the stop bit means reception of a complete character. This character is then transferred to the receiver-data buffer shown in Fig.2, and the R_xRDY becomes active. In cases where this character is not read by the CPU and where the next character is transferred to the receiver-data buffer, the preceding character is destroyed and an overrun-error flag is set.

These error flags can be read as the M5L8251AP-5 status information. The occurrence of an error does not stop USART operations. The error flags are cleared by the ER(D_4 bit) of the command instruction.

The asynchronous-system transfer formats are shown in Figs. 6 and 7.

Synchronous Transmission Mode

In this mode the T_xD pin remains in the high-level state until initial setting by the CPU is completed. After initialization, the state of $\overline{CTS}$="L" and T_xEN =1 enables serial transmission of characters through the T_xD pin. Then, data characters are sent out and shifted by the falling edge of the $\overline{T_xC}$ signal. The transmission rate equals the $\overline{T_xC}$ rate.

Thus, once data-character transfer starts, it must continue through the T_xD pin at the same rate as that of $\overline{T_xC}$. Unless data characters are provided from the CPU before the transmitter buffer becomes empty, one or two SYNC characters are automatically output from the T_xD pin In this case, it should be noted that the T_xEMPTY pin enters the high-level state when there are no data characters left in the M5L8251AP-5 to be transferred, and that the low-level state is not entered until the USART is provided with the next data character from the CPU. Care should also be taken over the fact that merely setting a command instruction does not effect SYNC-character insertion, because the SYNC character insertion is enabled after sending out the first data character.

In this mode, too, break characters are sent out in succession from the T_xD pin when SBRK is designated (D_3=1) by a command instruction.

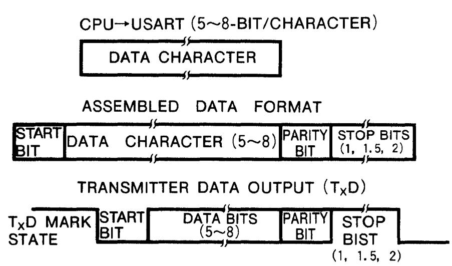
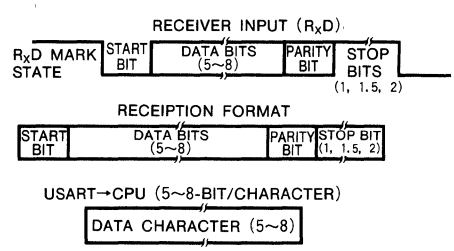


Fig. 6 Asynchronous transmission format I (transmission)



Note : When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0.

Fig. 7 Asynchronous transmission format II (reception)

STATUS INFORMATION

The CPU can always read USART status by setting the C/$\overline{D}$ to high-level and $\overline{RD}$ to low-level.

The status information format is shown in Fig. 10. In this format R_XRDY, T_XEMPTY and SYNDET have the same definitions as those of the pins. This means that these three pieces of status information become high-level when each pin is 1. The other status information is defined as follows:

DSR: When the $\overline{DSR}$ pin is in the low-level state, status information DSR becomes 1.

FE: The occurrence of a frame error in the receiver section makes the status information FE=1.

OE: The occurrence of an overrun error in the receiver section makes the status information OE=1.

PE: The occurrence of a parity error in the receiver section makes this status information PE=1.

T_XRDY: This information becomes 1 when the transmit data buffer is empty. Be careful because this has a different meaning from the T_XRDY pin that enters the high-level state only when the transmitter buffer is empty, when the $\overline{CTS}$ pin is in the low-level state, and when T_XEN is 1.

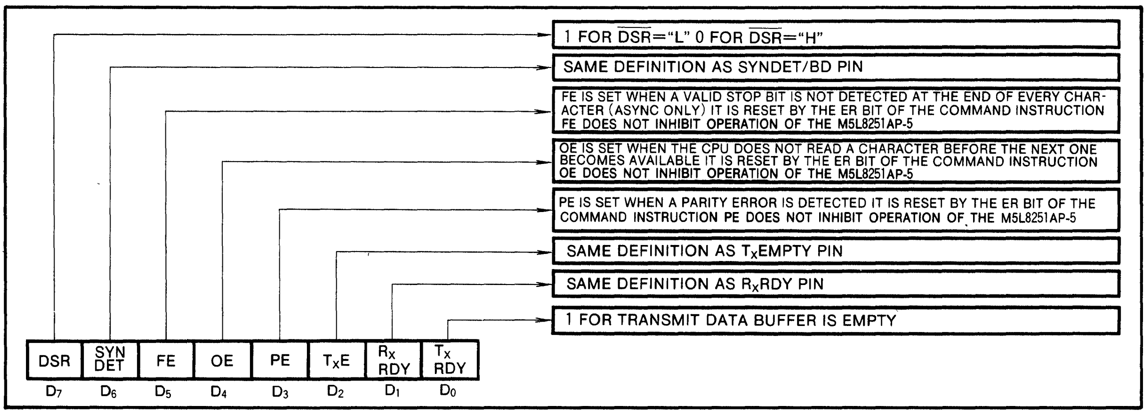


Fig. 10 Status information (C/$\overline{D}$="H", $\overline{WR}$="L")

APPLICATION EXAMPLES

Fig. 11 shows an application example for the M5L8251AP-5 in the asynchronous mode. When the port addresses of the M5L8251AP-5 are assumed to be 00# and 01# in this figure, initial setting in the asynchronous mode is carried out in the following manner:

MVI	**A, B6#**	Mode setting
OUT	**01#**	
MVI	**A, 27#**	Command instruction
OUT	**01#**	

In this case, the following are set by mode setting:

Asynchronous mode
6 bits/character
Parity enable (even)
1.5 stop bits
Baud rate: 16X

Command instructions set the following

RTS=1→$\overline{RTS}$ pin="L"
R_XE=1
DTR=1→$\overline{DTR}$ pin="L"
T_XEN=1

When the initial setting is complete, transfer operations are allowed. The $\overline{RTS}$ pin is initially set to the low-level by setting RTS to 1, and this serves as a $\overline{CTS}$ input with T_XEN being equal to 1. For this reason the same definition applies to the status and pin of T_XRDY, and 1 is assigned when the transmit-data buffer is empty. Actual transfer of data is carried out in the following way:

IN	**01#**	Status read

The IN instruction prompts the CPU to read the USART's status. The result is; if the T_XRDY equals 1 transmitter data is sent from the CPU and written on the M5L8251AP-5. Transmitter data is written in the M5L8251AP-5 in the following manner:

MVI	**A, 2D#**	$2D_{16}$ is an example of transmitter data.
OUT	**00#**	USART←(A)

Receiver data is read in the following manner:

IN	**00#**	(A)←USART

In the above example, the status information is read and as a result, the transmitter data is written and read. Interruption processing by using the T_XRDY and R_XRDY pins is also possible.

Fig. 12 shows the status of the T_XD pin when data written in the USART is transferred from the CPU. When the data shown in Fig.12 enters the R_XD pin, data sent from the M5L8251AP-5 to the CPU becomes $2D_{16}$ and bits D_6 and D_7 are treated as 0.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

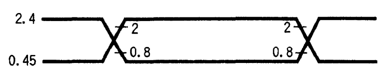
ELECTRICAL CHARACTERISTICS (Ta=−20～75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}	All outputs are high-level			100	mA
I_{IH}	High-level input current	$V_I=V_{CC}$	−10		10	μA
I_{IL}	Low-level input current	V_I=0.45V	−10		10	μA
I_{OZ}	Off-state input current	V_O=0.45V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	$V_{CC}=V_{SS}$, f=1MHz, 25mV_{rms}, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{CC}=V_{SS}$, f=1MHz, 25mV_{rms}, T_a=25℃			20	pF

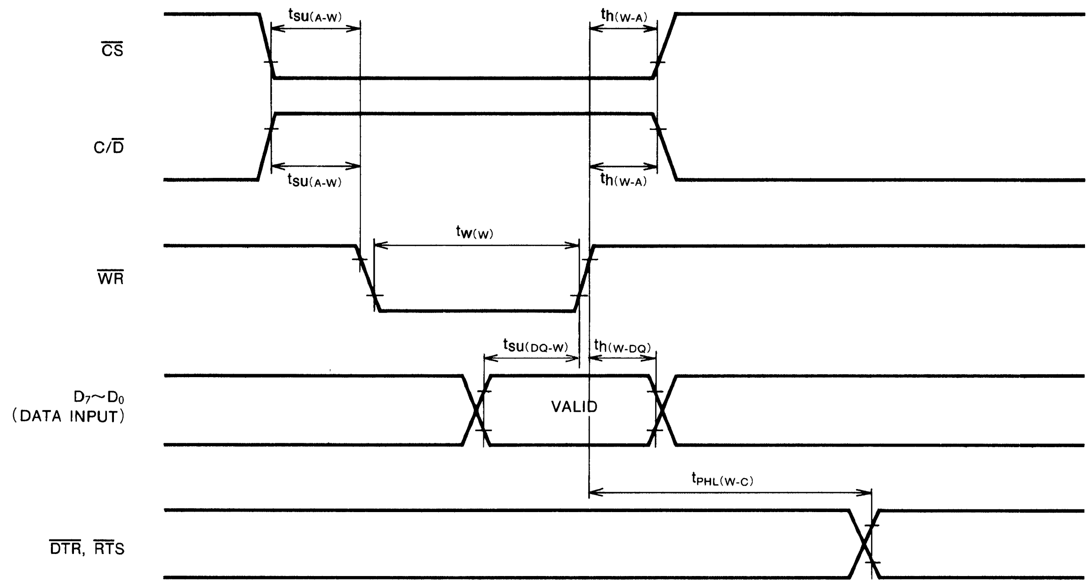
SWITCHING CHARACTERISTICS (T_a=−20∼75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read (Note8)	C_L=150pF			200	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		10		100	ns
$t_{PZV(TxC-TxD)}$	T_XD enable time after falling edge of $\overline{T_XC}$				1	μs
$t_{PLH(CLB-TxR)}$	Propagation time from center of last bit to T_XRDY (Note9)				8	$t_{C(\phi)}$
$t_{PHL(W-TxR)}$	Propagation time from write data to T_XRDY clear (Note9)				400	ns
$t_{PLH(CLB-RxR)}$	Propagation time from center of last bit to R_XRDY (Note9)				26	$t_{C(\phi)}$
$t_{PHL(R-RxR)}$	Propagation time from read data to R_XRDY clear (Note9)				400	ns
$t_{PLH(RxC-SYD)}$	Propagation time from rising edge of $\overline{R_XC}$ to internal SYNDET (Note9)				26	$t_{C(\phi)}$
$t_{PLH(CLB-TxE)}$	Propagation time from center of last bit to T_XEMPTY (Note9)				20	$t_{C(\phi)}$
$t_{PHL(W-C)}$	Propagation time from rising edge of $\overline{WR}$ to control (Note9)				8	$t_{C(\phi)}$

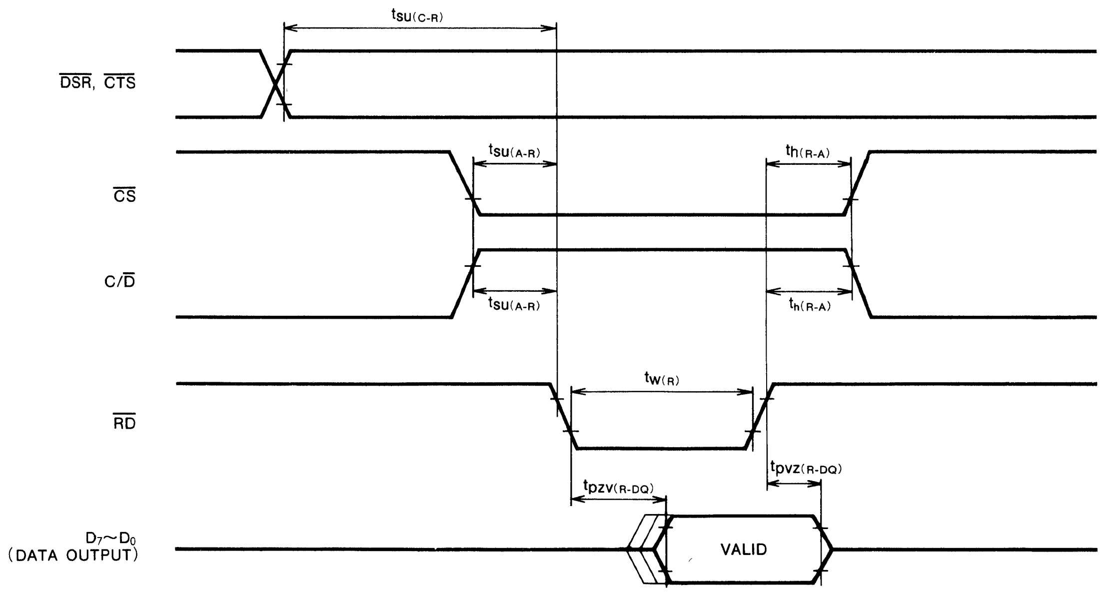
Note 8 : Assumes that address is vaild before falling edge of $\overline{RD}$
9 : Status-up date can have a maximum delay of 28 clock periods from the event affecting the status.
10 : Input pulse level 0.45∼2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 20ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 20ns



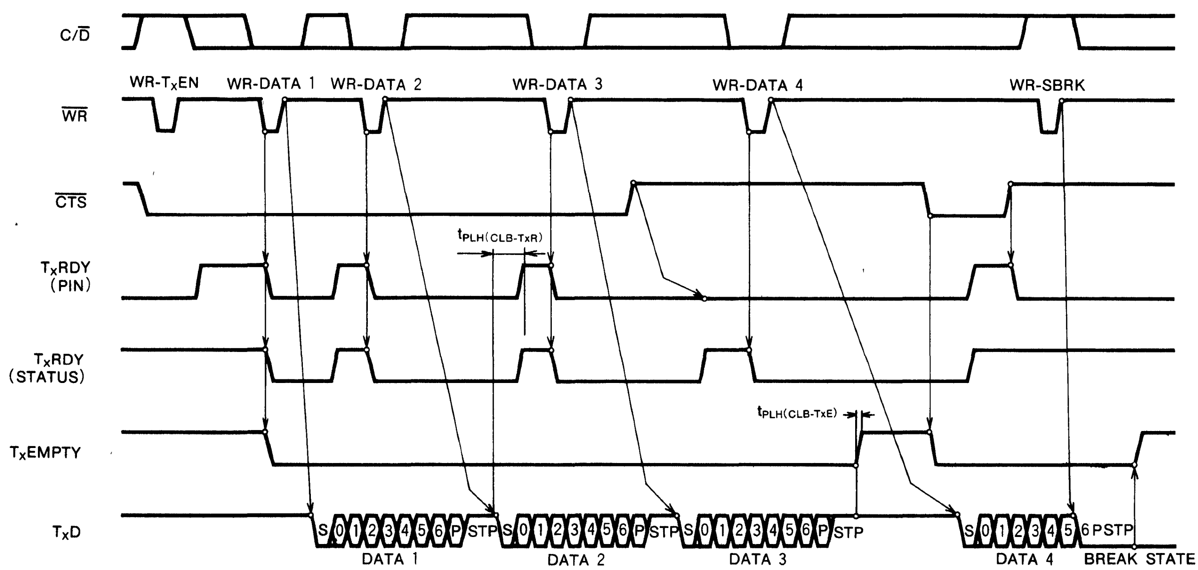
Write Control Cycle (CPU→USART)



Read Control Cycle (USART→CPU)

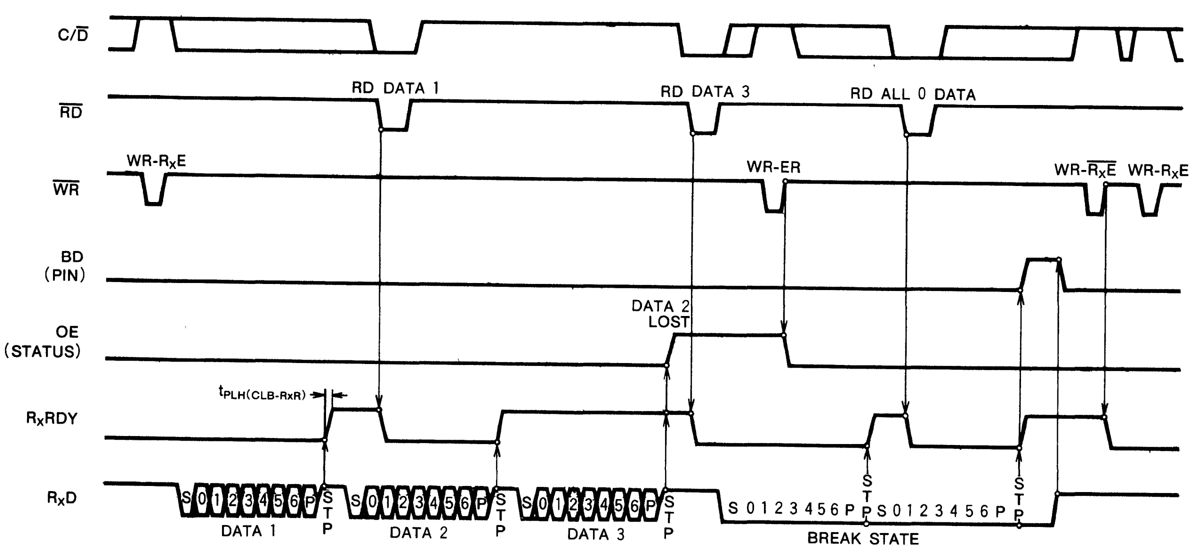


Transmitter Control & Flag Timing (Async Mode)



Note 11 : Example format = 7 bits/character with parity & 2 stop bits
12 : T_XRDY(pin) = "H" ←(Transmit-data buffer is empty) · (T_XEN = 1) · (CTS = "L")
13 : T_XRDY(status) = 1 ←(Transmit-data buffer is empty)

Receiver Control & Flag Timing (Async Mode)



Note 14 : Example format = 7 bits/character with parity & 2 stop bits

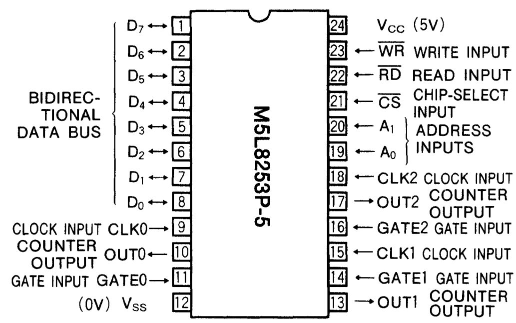
DESCRIPTION

The M5L8253P-5 is a programmable general-purpose timer device developed by using the N-channel silicon-gate ED-MOS process. It offers counter and timer functions in systems using an 8-bit parallel-processing CPU.

The use of the M5L8253P-5 frees the CPU from the execution of looped programs, count-operation programs and other simple processing involving many repetitive operations, thus contributing to improved system throughputs.

The M5L8253P-5 works on a single power supply, and both its input and output can be connected to a TTL circuit.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4

FEATURES

- Single 5V supply voltage
- TTL compatible
- Clock period: DC~2. 6MHz
- 3 independent built-in 16-bit down counters
- 6 counter modes freely assignable for each counter
- Binary or decimal counts

APPLICATION

Delayed-time setting, pulse counting and rate generation in microcomputers.

FUNCTION

Three independent 16-bit counters allow free programming based on mode-control instructions from the CPU. When roughly classified, there are 6 modes (0~5). Mode 0 is mainly used as an interruption timer and event counter, mode 1 as a digital one-shot, modes 2 and 3 as a rate generator, mode 4 for a software triggered strobe, and mode 5 for a hardware triggered strobe. The count can be monitored and set at any time. The counter operates with either the binary or BCD system.

BLOCK DIAGRAM

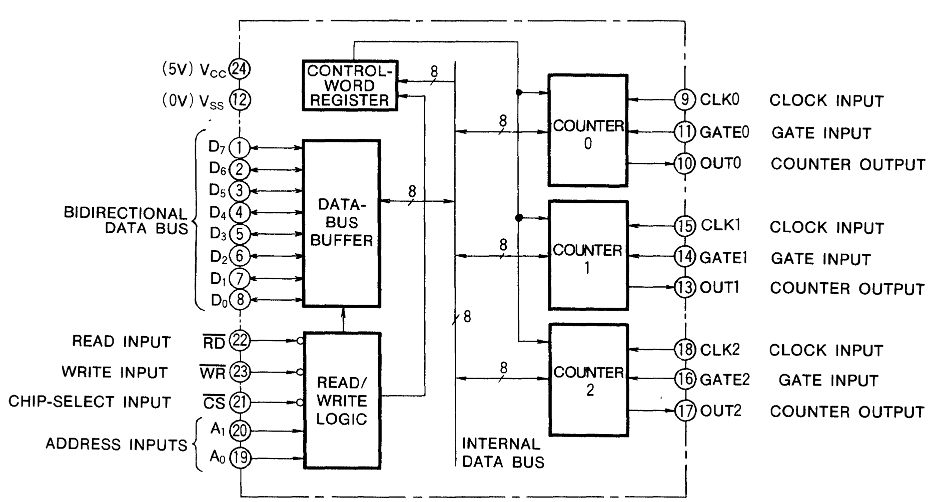


Table 1 Basic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Function
L	H	L	0	0	Data bus→Counter 0
L	H	L	0	1	Data bus→Counter 1
L	H	L	1	0	Data bus→Counter 2
L	H	L	1	1	Data bus→Control-word register
L	L	H	0	0	Data bus←Counter 0
L	L	H	0	1	Data bus←Counter 1
L	L	H	1	0	Data bus←Counter 2
L	L	H	1	1	3-state
H	×	×	×	×	3-state
L	H	H	×	×	3-state

● SC (Select Counter)

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Prohibited combination

● RL (Read/Load)

RL1	RL0	
0	0	Counter Latch Command
0	1	Read/load low-order 8 bits only
1	0	Read/load high-order 8 bits only
1	1	Read/load low-order 8 bits and then high-order 8 bits

● M (Mode)

M2	M1	M0	
0	0	0	Mode0
0	0	1	Mode1
×	1	0	Mode2
×	1	1	Mode3
1	0	0	Mode4
1	0	1	Mode5

● BCD

0	Binary counter (16-bit)
1	Binary-coded decimal counter (4 decades)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
SC		RL		M			BCD

Fig. 1 Control-Word Format

MITSUBISHI ELECTRIC

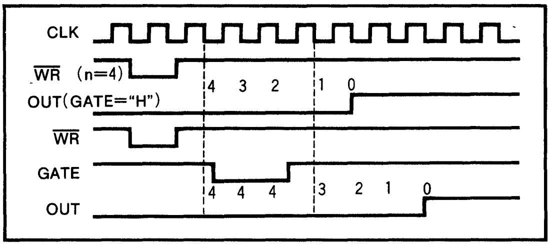


Fig. 2 Mode 0

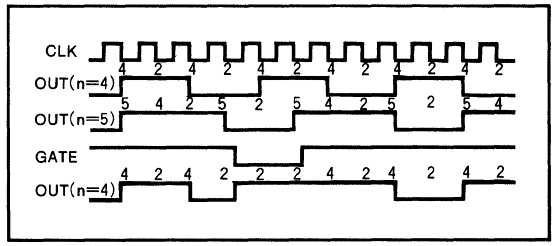


Fig. 5 Mode 3

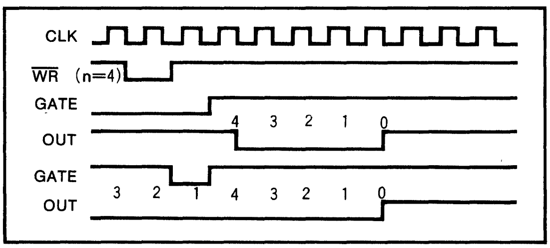


Fig. 3 Mode 1

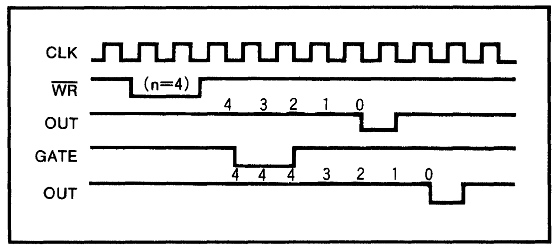


Fig. 6 Mode 4

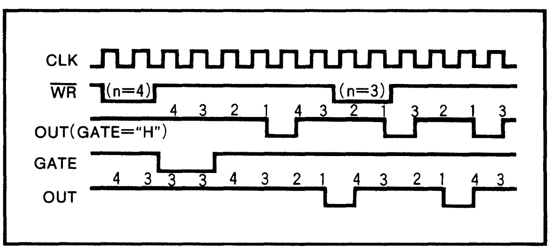


Fig. 4 Mode 2

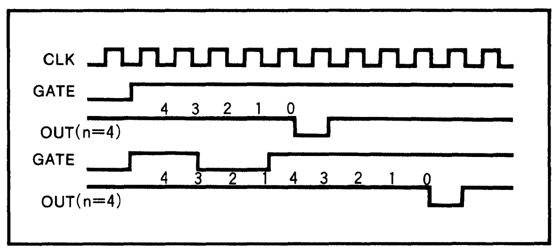


Fig. 7 Mode 5

COUNTER MONITORING

Sometimes the counter must be monitored by reading its count or using it as an event counter. The M5L8253P-5 offers the following two methods for count reading:

Read Operation

The count can be read by designating the address of the counter to be monitored and executing a simple I/O read operation. In order to ensure correct reading of the count, it is necessary to cause the clock input to pause by external logic or prevent a change in the count by gate input. An example of a program to read the counter 1 count is shown below. If RL1, RL0=1, 1 has been specified in the control word, the first IN instruction enables the low-order 8 bits to be read and the second IN instruction enables the high-order 8 bits.

IN	**n_2**	···· n_2 is the counter 1 address
MOV	**D, A**	
IN	**n_2**	
MOV	**E, A**	

The IN instruction should be executed once or twice by the RL1 and RL0 designations in the control-word register.

Read-on-the-Fly Operation

This method makes it possible to read the current count without affecting the count operation at all. A special counter-latch command is first written in the control-word register. This causes latching of all the instantaneous counts to the register, allowing retention of stable counts. An example of a program to execute this operation for counter 2 is given below.

MVI	**A, 1000XXXX**	···· $D_5 = D_4 = 0$ designates counter latching
OUT	**n_1**	···· n_1 is the control-word-register address
IN	**n_3**	···· n_3 is the counter 2 address
MOV	**D, A**	
IN	**n_3**	
MOV	**E, A**	

In this example, the IN instruction is executed twice. Due to the internal logic of the M5L8253P-5 it is absolutely essential to complete the entire reading procedure. If 2 bytes are programmed to be read, then two bytes must be read before any OUT instruction can be executed to the same counter.

TIMING REQUIREMENTS ($T_a = -20 \sim 75°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(R)}$	Read pulse width		300			ns
$t_{SU(A-R)}$	Address setup time before read		30			ns
$t_{h(R-A)}$	Address hold time after read		5			ns
$t_{rec(R)}$	Read recovery time		1000			ns

Write cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(W)}$	Write pulse width		300			ns
$t_{su(A-W)}$	Address setup time before write		30			ns
$t_{h(W-A)}$	Address hold time after write		30			ns
$t_{su(DQ-W)}$	Data setup time before write		250			ns
$t_{h(W-DQ)}$	Data hold time after write		30			ns
$t_{rec(W)}$	Write recovery time		1000			ns

Clock and gate timing

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi H)}$	Clock high pulse width		230			ns
$t_{w(\phi L)}$	Clock low pulse width		150			ns
$t_{c(\phi)}$	Clock cycle time		380		DC	ns
$t_{w(GH)}$	Gate high pulse width		150			sn
$t_{w(GL)}$	Gate low pulse width		100			ns
$t_{su(G-\phi)}$	Gate setup time before clock		100			ns
$t_{h(\phi-G)}$	Gate hold time after clock		50			ns

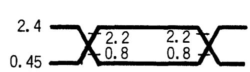
SWITCHING CHARACTERISTICS ($T_a = -20 \sim 75°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Propagation time from read to output	$C_L = 150pF$			200	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to output floating (Note 2)		25		100	ns
$t_{PXV(G-OUT)}$	Propagation time from gate to output				300	ns
$t_{PXV(\phi-OUT)}$	Propagation time from clock to output				400	ns

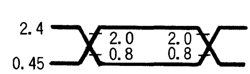
Note 1 : A C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	$V_{IH} = 2.2V$, $V_{IL} = 0.8V$
output	$V_{OH} = 2.0V$, $V_{OL} = 0.8V$

2 : Test condition is not applied



Input



Output

PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5L8255AP-5 is a family of general-purpose programmable input/ output devices designed for use with an 8-bit/16-bit parallel CPU as input/output ports. Device is fabricated using N-channel silicon-gate ED-MOS technology for a single supply voltage. They are simple input and output interfaces for TTL circuits, having 24 input/output pins which correspond to three 8-bit input/output ports.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Darlington drive capability
- 24 programmable I/O pins
- Direct bit set/reset capability

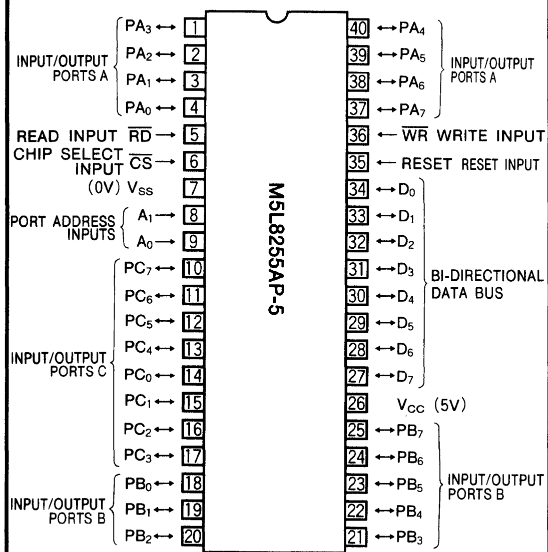
APPLICATION

Input/output ports for microprocessor

FUNCTION

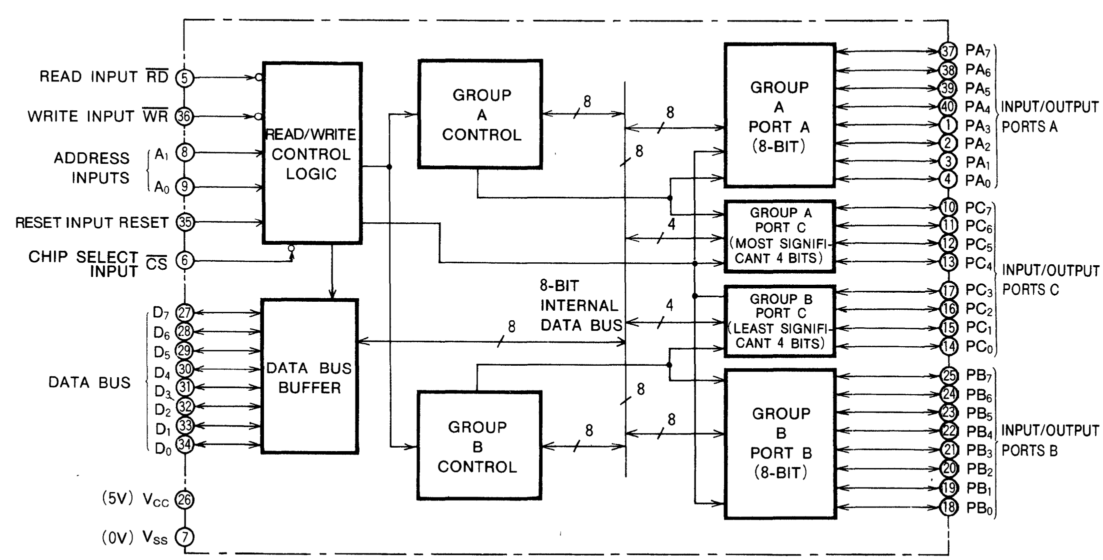
These PPIs have 24 input/output pins which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. They are used in three major modes of operation, mode 0, mode 1 and mode 2. Operating in mode 0 , each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1, the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to serve as input or output, and one 4-bit control port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port. Bit set/reset is controlled by CPU. A high-level reset input (RESET) clears the control register, and all ports are set to the input mode (high-impedance state).

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

BASIC OPERATING MODES

The PPI can operate in any one of three selected basic modes.

Mode 0: Basic input/output (group A, group B)
Mode 1: Strobed input/output (group A, group B)
Mode 2: Bidirectional bus (group A only)

The mode of both group A and group B can be selected independently. The control word format for mode set is shown in Fig. 2.

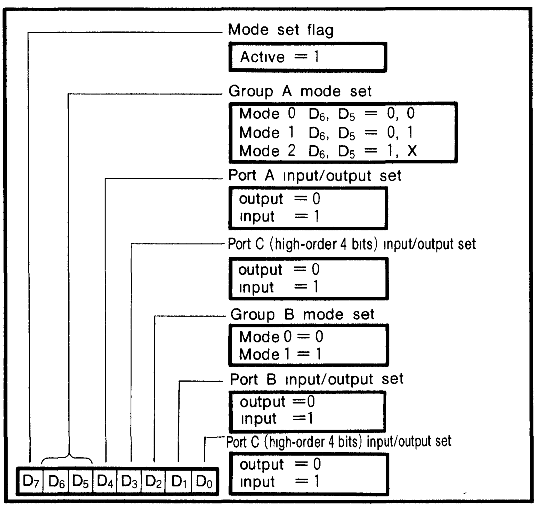
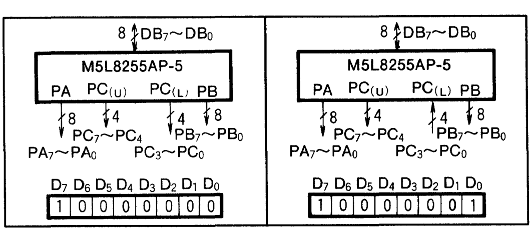
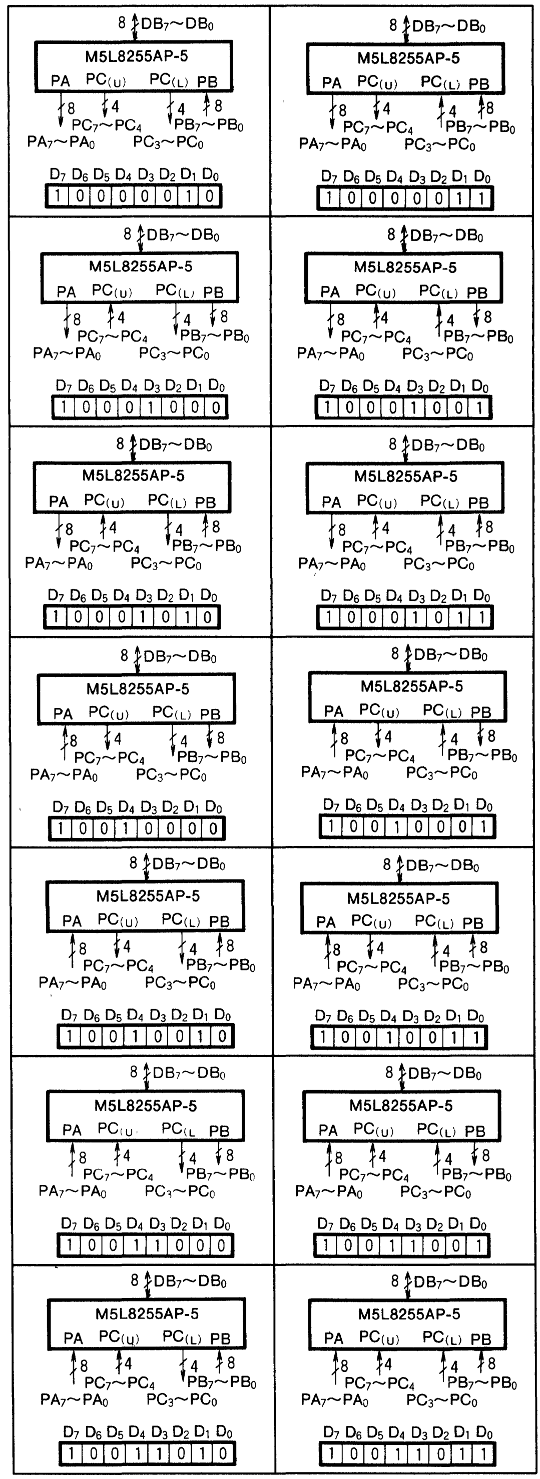


Fig. 2 Control word format for mode set.

1. Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the 3 ports. No "handshaking" is required; data is simply written in, or read from, the specified port. Output data from the CPU to the port can be held, but input data from the port to the CPU cannot be held. Any one of the 8-bit ports and 4-bit ports can be used as an input port or an output port. The diagrams following show the basic input/output operating modes.





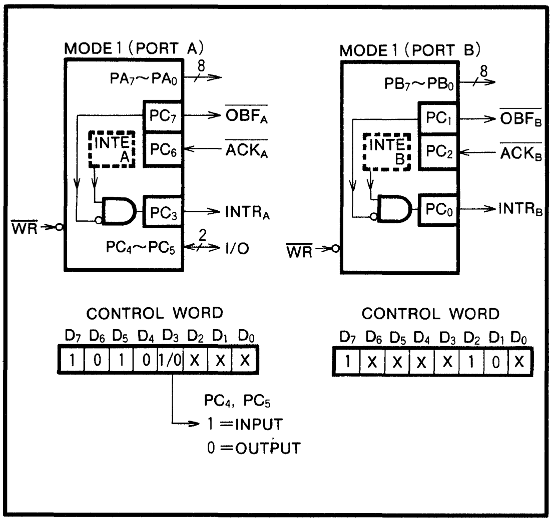


Fig. 5 An example of mode 1 output state

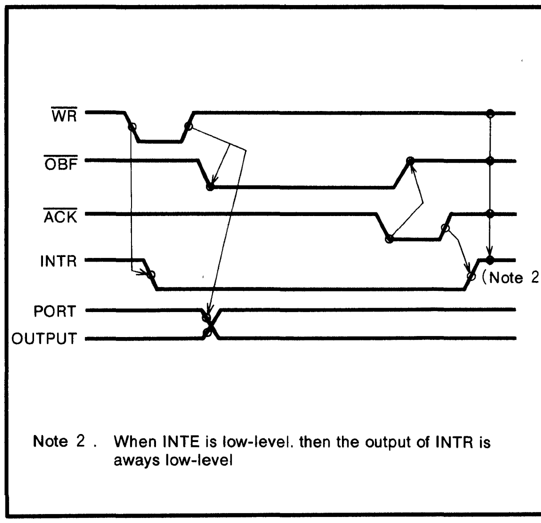


Fig. 6 Timing diagram

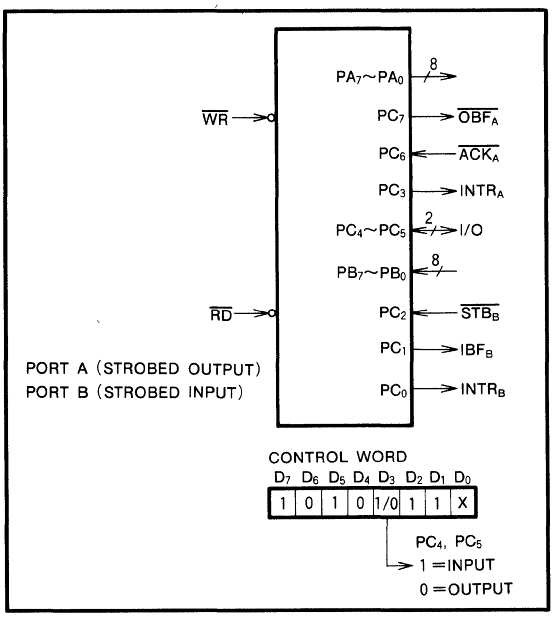


Fig. 7 Mode 1 port A and port B I/O example

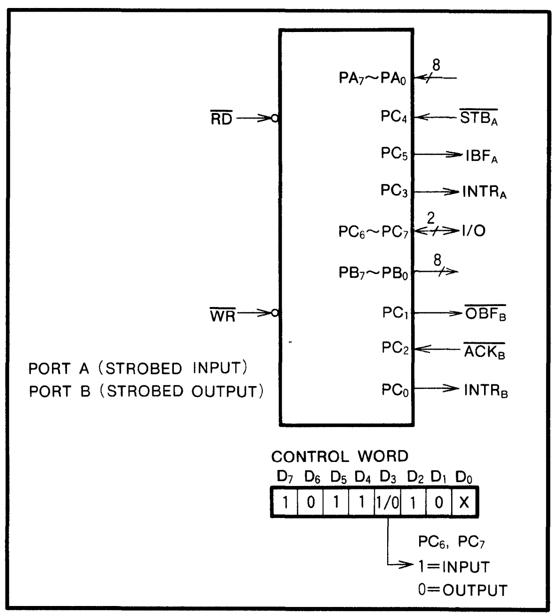


Fig. 8 Mode 1 port A and port B I/O example

4. Control Signal Read

In mode 1 or mode 2 when using port C as a control port, by CPU execution of an IN instruction, each control signal and bus status from port C can be read.

5. Control Word Tables

Control word formats and operation details for mode 0, mode 1, mode 2 and set/reset control of port C are given in Tables 3, 4, 5 and 6, respectively.

Table 2 Read-out control signals

Mode \ Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1, input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
Mode 1, output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
Mode 2	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	By group B mode		

Table 3 Mode 0 control words

Control words									Group A		Group B	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal	Port A	Port C (high-order 4 bits)	Port C (low-order 4 bits)	Port B
1	0	0	0	0	0	0	0	80	OUT	OUT	OUT	OUT
1	0	0	0	0	0	0	1	81	OUT	OUT	IN	OUT
1	0	0	0	0	0	1	0	82	OUT	OUT	OUT	IN
1	0	0	0	0	0	1	1	83	OUT	OUT	IN	IN
1	0	0	0	1	0	0	0	88	OUT	IN	OUT	OUT
1	0	0	0	1	0	0	1	89	OUT	IN	IN	OUT
1	0	0	0	1	0	1	0	8A	OUT	IN	OUT	IN
1	0	0	0	1	0	1	1	8B	OUT	IN	IN	IN
1	0	0	1	0	0	0	0	90	IN	OUT	OUT	OUT
1	0	0	1	0	0	0	1	91	IN	OUT	IN	OUT
1	0	0	1	0	0	1	0	92	IN	OUT	OUT	IN
1	0	0	1	0	0	1	1	93	IN	OUT	IN	IN
1	0	0	1	1	0	0	0	98	IN	IN	OUT	OUT
1	0	0	1	1	0	0	1	99	IN	IN	IN	OUT
1	0	0	1	1	0	1	0	9A	IN	IN	OUT	IN
1	0	0	1	1	0	1	1	9B	IN	IN	IN	IN

Note 4 · OUT indicates output port, and IN indicates input port

Table 4 Mode 1 control words

Control words									Group A						Group B			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexa-decimal	Port A	Port C PC_7	PC_6	PC_5	PC_4	PC_3	Port C PC_2	PC_1	PC_0	Port B
1	0	1	0	0	1	0	X	A4 A5	OUT	$\overline{OBF}_A$	$\overline{ACK}_A$	OUT		$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$	OUT
1	0	1	0	0	1	1	X	A6 A7	OUT	$\overline{OBF}_A$	$\overline{ACK}_A$	OUT		$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$	IN
1	0	1	0	1	1	0	X	AC AD	OUT	$\overline{OBF}_A$	$\overline{ACK}_A$	IN		$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$	OUT
1	0	1	0	1	1	1	X	AE AF	OUT	$\overline{OBF}_A$	$\overline{ACK}_A$	IN		$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$	IN
1	0	1	1	0	1	0	X	B4 B5	IN	OUT		IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$	OUT
1	0	1	1	0	1	1	X	B6 B7	IN	OUT		IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$	IN
1	0	1	1	1	1	0	X	BC BD	IN	IN		IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$	OUT
1	0	1	1	1	1	1	X	BE BF	IN	IN		IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$	IN

Note 5 : Mode of group A and group B can be programmed independently
6 : It is not necessary for both group A and group B to be in mode 1.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5 V±5%, V_{SS}=0 V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			−0.5		0.8	V
V_{OH}	High-level output voltage	Data bus	I_{OH}=−400μA	2.4			V
		Port	I_{OH}=−200μA				
V_{OL}	Low-level output voltage	Data bus	I_{OL}=2.5mA			0.45	V
		Port	I_{OL}=1.7mA				
I_{OH}	High-level output current (Note10)		V_{OH}=1.5V, R_{EXT}=750Ω	−1		−4	mA
I_{CC}	Supply current from V_{CC}					120	mA
I_{IH}	High-level input current		V_I=V_{CC}			±10	μA
I_{IL}	Low-level input current		V_I=0V			±10	μA
I_{OZ}	Off-state output current		V_O=0V~V_{CC}			±10	μA
C_i	Input terminal capacitance		V_{IL}=V_{SS}, f=1MHz, 25mVrms T_a=25℃			10	pF
$C_{i/o}$	Input/output terminal capacitance		$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms T_a=25℃			20	pF

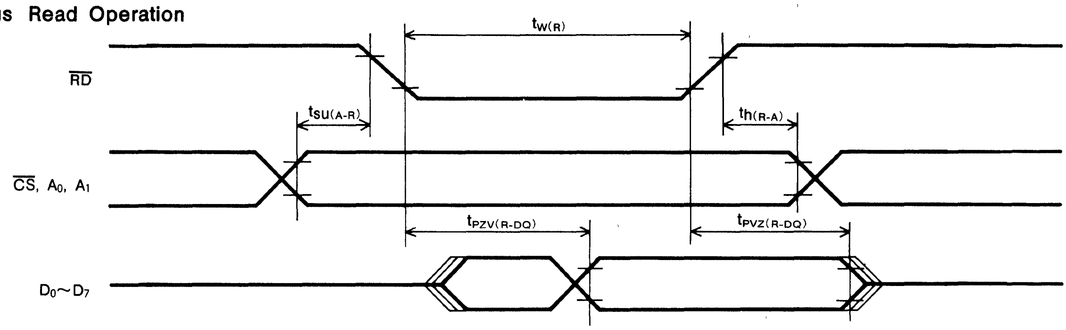
Note 9 : Current flowing into an IC is positive. out is negative
10 It is valid only for any 8 input/output pins of PB and PC.

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5 V±5%, V_{SS}=0 V, unless otherwise noted)

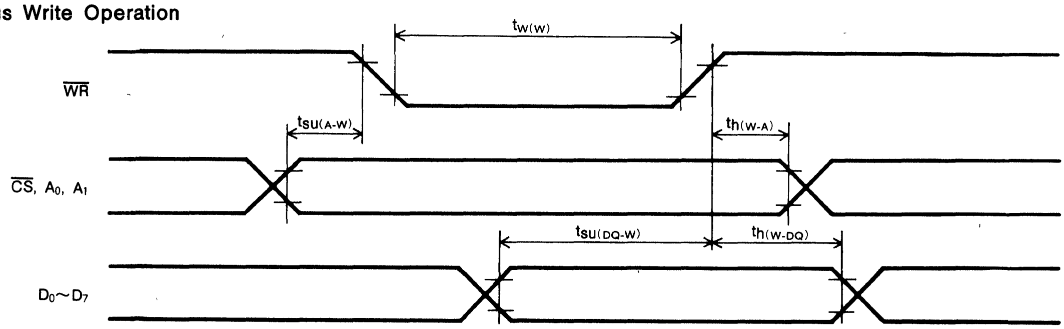
Symbol	Prameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(R)}$	Read pulse width		300			ns
$t_{su(PE-R)}$	Peripheral setup time before read		0			ns
$t_{h(R-PE)}$	Peripheral hold time after read		0			ns
$t_{su(A-R)}$	Address setup time before read		0			ns
$t_{h(R-A)}$	Address hold time after read		0			ns
$t_{w(W)}$	Write pulse width		300			ns
$t_{su(DQ-W)}$	Data setup time before write		100			ns
$t_{h(W-DQ)}$	Data hold time after write		30			ns
$t_{su(A-W)}$	Address setup time before write		0			ns
$t_{h(W-A)}$	Address hold time after write		20			ns
$t_{w(ACK)}$	Acknowledge pulse width		300			ns
$t_{w(STB)}$	Strobe pulse width		500			ns
$t_{su(PE-STB)}$	Peripheral setup time before strobe		0			ns
$t_{h(STB-PE)}$	Peripheral hold time after strobe		180			ns
$t_{c(RW)}$	Read/write cycle time		850			ns

TIMING DIAGRAM

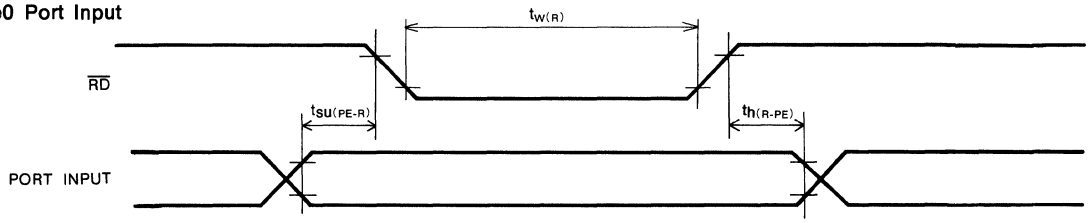
Data Bus Read Operation



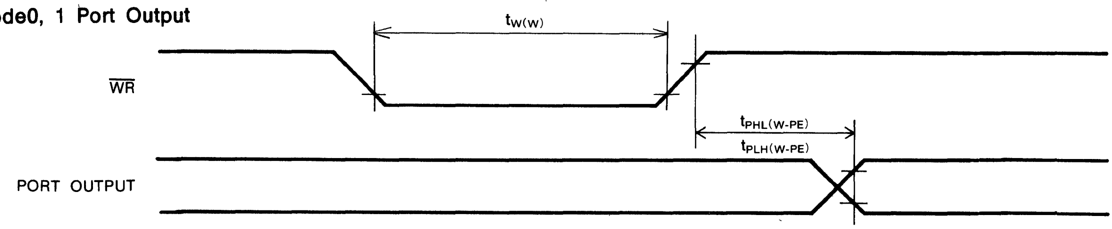
Data Bus Write Operation



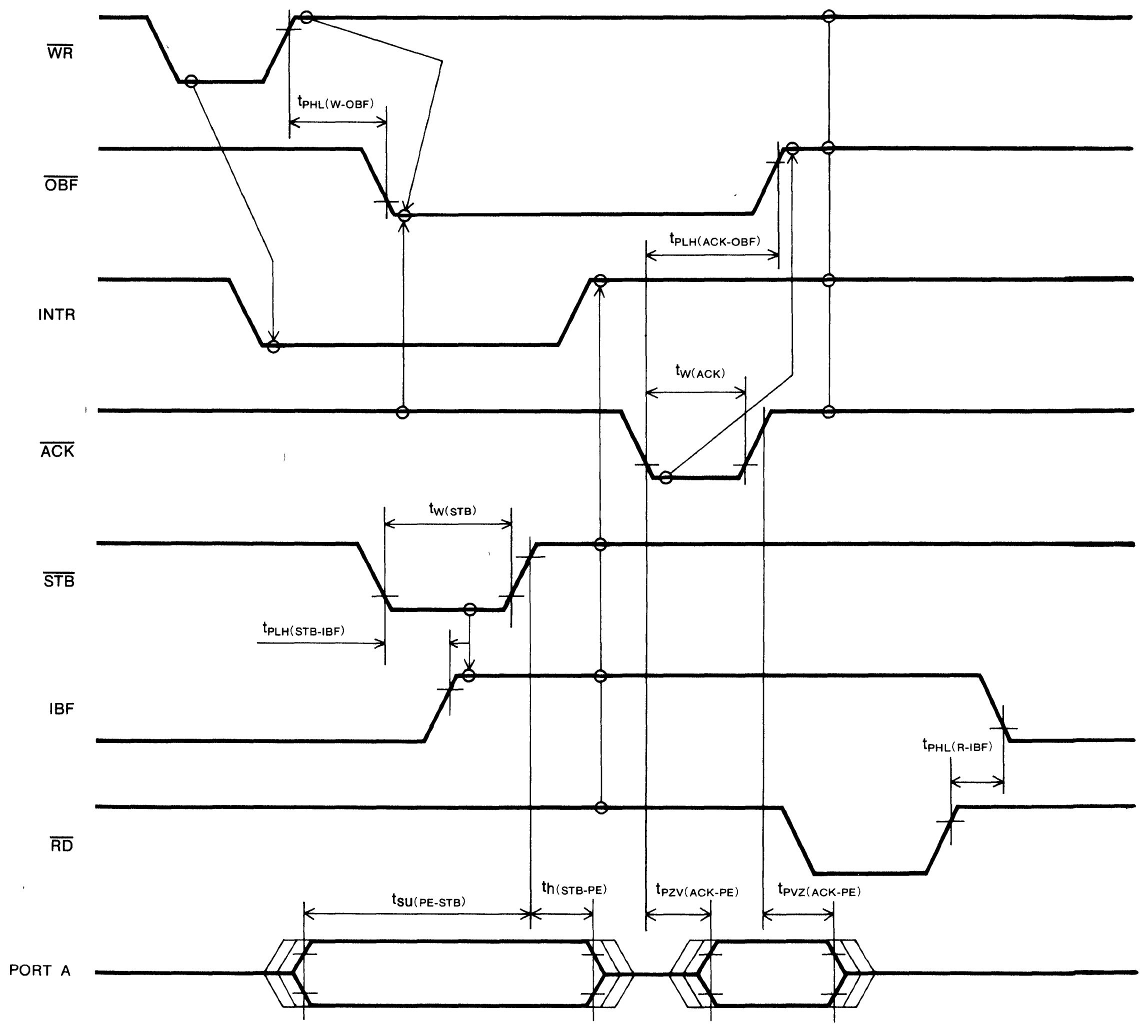
Mode0 Port Input



Mode0, 1 Port Output



Mode2 Bidirectional



Note 13 INTR=IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$

2. Mode 1

An example of a circuit for an application using mode 1 is shown in Fig. 12.

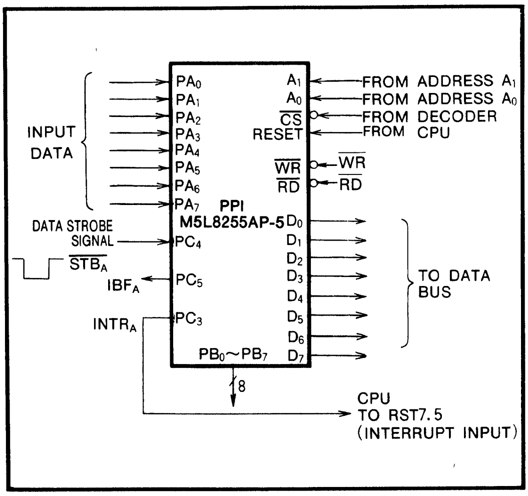


Fig. 12 A circuit for an application using mode 1

Transferring data from a terminal unit to port A and sending a strobe signal to PC_4 will hold the data in the internal latch of the PPI, and PC_5 (IBF input buffer full flag) is set to high-level. If a bit-set of PC_4 has been executed in advance, the CPU can be interrupted by the INTR signal of PC_3 when the input data is latched in the PPI. In this way, port A becomes an interrupting port; and at the same time, port B can select its mode independently.

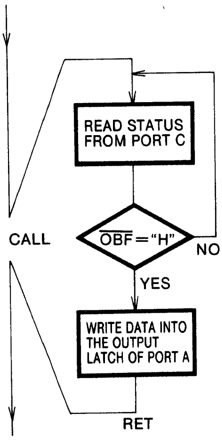
The actual program for the circuit of Fig. 12 is as follows:

MVI	**A, B0#**	Control word is 10110000, port A is the mode 1 input and the others are output
OUT	**03#**	Outputting to the control address
MVI	**A, 09#**	PC_4bit-set 00001001
OUT	**03#**	Outputting to the control address
EI		Interrupt enable
HLT		Halt

If the data has been set in a terminal unit, and the strobe signal has been input, then the data will be latched in port A and the CPU RST7.5 goes high-level. In the case of Fig. 11, a jump to $003C_{16}$ is executed to continue the program as follows:

$003C_{16}$	**IN**	**00#**	CPU register A ← Port A PC_3 interrupt signal becomes low-level
	EI		
	RET		

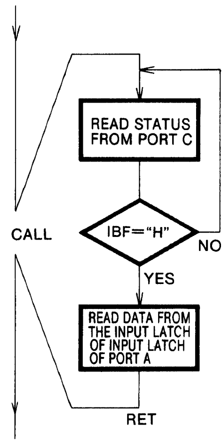
1. Master CPU subroutine for transmitting data to the slave CPU.



Program example

```
MOUT  PUSH  PSW
OBF   IN    02#
      ANI   80#
      JZ    OBF
      POP   PSW
      OUT   00#
      RET
```

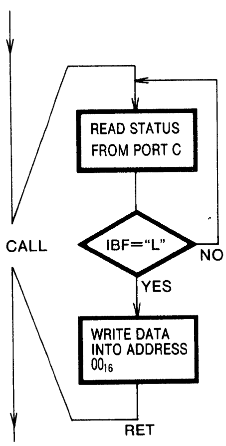
2. Subroutine for receiving data from the slave CPU.



Program example

```
MIN   IN    02#
      ANI   20#
      JZ    MIN
      IN    00#
      RET
```

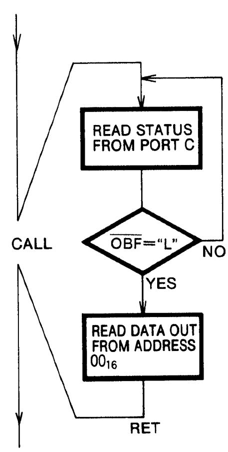
3. Slave CPU subroutine for transmitting data to the master CPU.



Program example

```
SOUT  PUSH  PSW
IBF   IN    01#
      ANI   02#
      JNZ   IBF
      POP   PSW
      OUT   00#
      RET
```

4. Subroutine for receiving data from the master CPU.



Program example

```
SIN   IN    01#
      ANI   01#
      JNZ   SIN
      IN    00#
      RET
```

M5L8257P-5

PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5L8257P-5 is a programmable 4-channel direct memory access (DMA) controller. It is produced using the N-channel silicon-gate ED-MOS process and is specifically designed to simplify data transfer at high speeds for microcomputer systems

The LSI operates on a single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible interface
- Priority DMA request logic
- Channel-masking function
- Terminal count and Modulo 128 outputs
- 4-channel DMA controller
- Compatible with MELPS85 devices

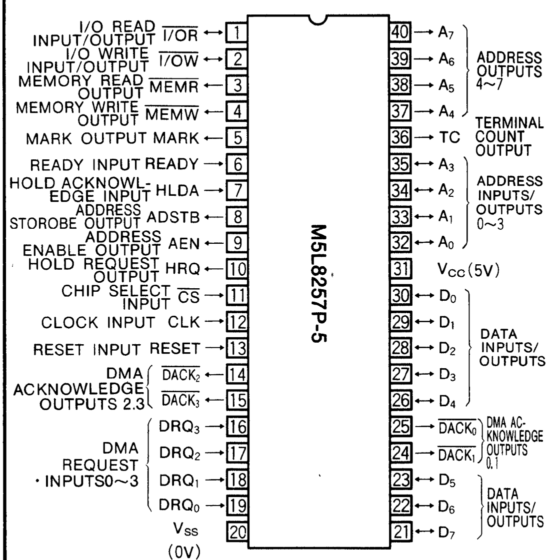
APPLICATION

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

FUNCTION

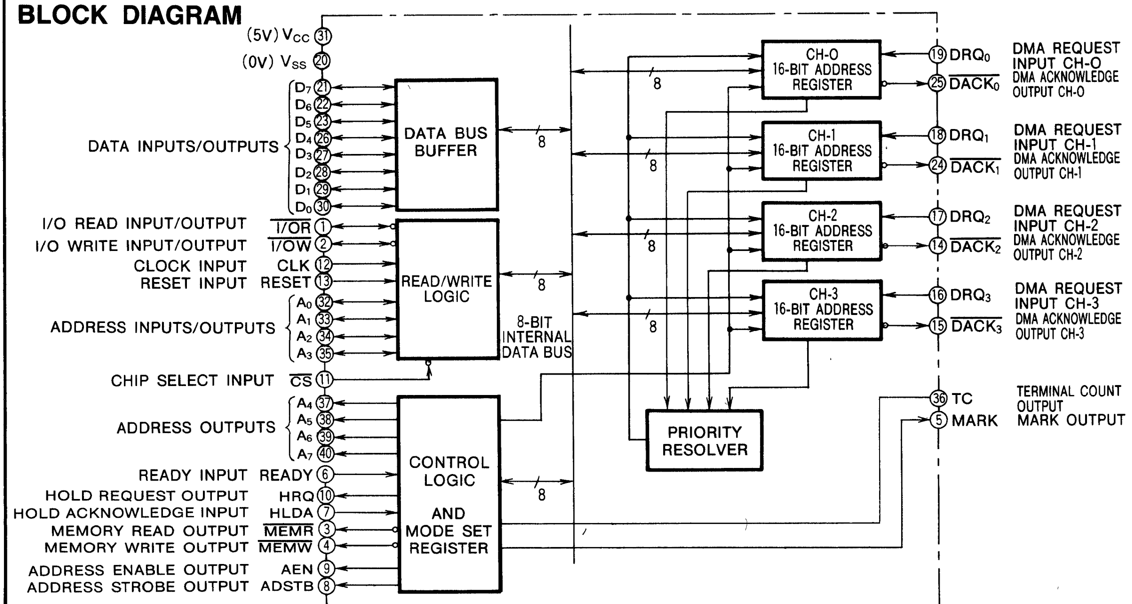
The M5L8257P-5 controller is used in combination with the M5L8212P 8-bit input/output port in 8-bit microcomputer systems. It consists of a channel section to acknowledge DMA requests, control logic to exchange commands and data with the CPU, read/write logic, and registers to hold transfer addresses and count the number of bytes to be transferred. When a DMA request is made to an unmasked channel from the peripherals after setting of the transfer mode, transfer-start address and the number of transferred bytes for the registers, the M5L8257P-5 issues a priority request for the use of the bus to the CPU. On receiving an HLDA signal from the CPU, it sends a DMA acknowledge signal to the channel with the highest priority, starting DMA operation. During DMA operation, the contents of the high-order 8 bits of the transfer memory address are transmitted to the M5L8212P address-latch device through pins $D_0 \sim D_7$. The contents of the low-order 8 bits are transmitted through pins $A_0 \sim A_7$. After address transmission, DMA transfer can be started by dispatching read and write signals to the memories and peripherals.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



Register Initialization

Two 16-bit registers are provided for each of the 4 channels.

DMA Address register

15															0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

DMA TRANSFER STARTING ADDRESS

Terminal count register

15	14	13													0
Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

DMA MODE　NUMBER OF TRANSFERRED BYTES—1

The DMA transfer starting address, number of transferred bytes, and DMA mode are written for each channel in 2 steps using the 8-bit data bus. The lower-order and upper-order bytes are automatically indicated by the first-last flip-flop for the writing and reading in 2 continuous steps.

The DMA mode (read, write, or verify) is indicated by the upper 2 bits of the terminal count register. The read mode refers to the operation of peripheral devices reading data out of memory. The write mode refers to data from peripheral devices being written into memory. The verify mode sends neither the read nor the write signals and performs a date check at the peripheral device.

In addition to the above-mentioned registers, there is a mode set register and a status register.

Mode set register (write only)

7							0
AL	TCS	EW	RP	EN3	EN2	EN1	EN0

ADDED FUNCTION SETTING BITS　CHANNEL ENABLE BITS

Status Register (read only)

7							0
0	0	0	UP	TC3	TC2	TC1	TC0

The upper-order 4 bits of the mode set register are used to select the added function, as described in 5-66. The lower-order 4 bits are mask bits for each channel. When set to 1, DMA requests are allowed. When the reset signal is input, all bits of the mode set and status registers are reset and DMA is inhibited for all channels. Therefore, to execute DMA operations, registers must first be initialized. An example of such an initialization is shown below.

```
MODESET:
    MVI  A, ADDL
    OUT  00#:  Channel 0 lower-order address
    MVI  A, ADDH
    OUT  00#:  Channel 0 upper-order address
    MVI  A, TCL
    OUT  01#:  Channel 0 terminal count lower-order
    MVI  A, TCH
    OUT  01#:  Channel 0 terminal count upper-order
    MVI  A, XX
    OUT  08#:  Mode set resister
```

As can be seen from the above example, until the contents of the address register and terminal count register become valid, the enable bit of the mode set register must not be set. This prevents memory contents from being destroyed by improper DRQ signals from peripheral devices.

DMA OPERATION DESCRIPTION

When a DMA request signal is received at the DRQ pin from a peripheral device after register initialization for a channel that is not masked, the M5L8257P-5 outputs a hold request signal to the CPU to begin DMA operation (S_1).

The CPU, upon receipt of the HRQ signal, outputs the HLDA signal which reserves capture of the bus after it has executed the present instruction to place this system in the hold state.

When the M5L8257P-5 receives the HLDA signal, an internal priority determining circuit selects the channel with the highest priority for the beginning of data transfer (S_0).

Upon the next S_1 state, the address signal is sent. The lower-order 8 bits and upper-order 8 bits are sent by means of the $A_0 \sim A_7$ and $D_0 \sim D_7$ pins respectively, latched into the M5L8212P and output at pins $A_8 \sim A_{15}$. Simultaneous with this, the AEN signal is output to prohibit the selection of a device not capable of DMA.

In the S_2 state, the read, extended write, and DACK signals are output and data transferred from memory or a peripheral device appears on the data bus.

In the S_3 state, the write signal required to write data from the bus is output. At this time if the remaining number of bytes to be transferred from the presently selected channel has reached 0, the terminal count (TC) signal is output. Simultaneously with this, after each 128-byte data transfer a mark signal is output as required. In addition, in this state the READY pin is sampled and, if low-level, the wait state (S_W) is entered. This is used to perform DMA with slow access memory devices. In the verify mode, READY input is ignored.

INTERNAL REGISTERS OF THE M5L8257P-5

Channel	Upper D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Lower D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Register
channel-0	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DMA address
	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	terminal count
channel-1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DMA address
	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	terminal count
channel-2	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DMA address
	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	terminal count
channel-3	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DMA address
	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	terminal count
									AL	TCS	EW	RP	EN3	EN2	EN1	EN0	Mode setting (for write only)
									0	0	0	UP	TC3	TC2	TC1	TC0	Status (for read only)

$A_0 \sim A_{15}$: Address of the memories for which DMA will be carried out from now on In initialization, DMA start addresses must be written

$C_0 \sim C_{13}$: Terminal counts-in this IC (the number of remaining transfer bytes minus 1) The address is decremented for each DMA transfer of one byte, and when the transfer is finished, becomes $(3FFF)_H$ If additional DRQ signals are input, the address continues to be decremented.

Rd. Wr : Used for DMA-mode setting by the following convention·

Rd	Wr	Mode to be set
0	0	DMA verify
0	1	DMA write
1	0	DMA read
1	1	Prohibition

AL : Automatic load mode. When this bit has been set, contents of the channel 3 register are written, as are on the channel 2 register when channel 2 DMA transfer comes to an end This mode allows quick, automatic chaining operations without intervention of the software

EW : Extended write signal mode When this bit has been set, write signals can be transmitted in advance to memories and peripheral equipment requiring long access time

TCS : Terminal count stop When a DMA transfer process is complete, with terminal-count output, the channel-enable mask of that channel is reset, prohibiting subsequent DMA cycles.

RP : Rotating priority mode The setting of this mode allows the priority order to be rotated by each byte transfer.
The setting priority is fixed with the channel 0 as highest, followed by channel 1 , 2 and 3 in descending order

Channel used for the present data transfer		CH-0	CH-1	CH-2	CH-3
Priority list for the next cycle	1	CH-1	CH-2	CH-3	CH-0
	2	CH-2	CH-3	CH-0	CH-1
	3	CH-3	CH-0	CH-1	CH-2
	4	CH-0	CH-1	CH-2	CH-3

EN0~EN3 : Channel-enable bit. This mask prohibits or allows the DMA request When the reset signal is applied, all channels are disabled.

UP : Update flag. This is set when register contents are transferred in an automatic load mode from channel 3 to channel 2.

TC0~TC3 : Terminal-count status flags. At the time of terminal-count output, the flag corresponding to the channel is set
The flag is, set by reading the status register, annd is unaffected by the TCS bits

ELECTRICAL CHARACTERISTICS ($T_a=-20\sim75°C$, $V_{CC}=5V\pm5\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OL}	Low-level output voltage	$I_{OL}=1.6mA$			0.45	V
V_{OH1}	High-level output voltage for AB, DB and AEN	$I_{OH}=-150\mu A$	2.4			V
V_{OH2}	High-level output voltage for HRQ	$I_{OH}=-80\mu A$	3.3			V
V_{OH3}	High-level output voltage for others		2.4			V
I_{CC}	Supply current from V_{CC}				120	mA
I_I	Input current	$V_I=0V, V_{CC}$	−10		10	μA
I_{OZ}	Off-state output current	$V_O=0V\sim V_{CC}$	−10		10	μA
C_I	Input terminal capacitance	$T_a=25°C$, $V_{CC}=V_{SS}$ Pins other than that under measurement are set to 0V, $f_C=1MHz$			10	pF
$C_{I/O}$	Input/output terminal capacitance				20	pF

TIMING REQUIREMENTS ($T_a=-20\sim75°C$, $V_{CC}=5V\pm5\%$, $V_{SS}=0V$, unless otherwise noted)

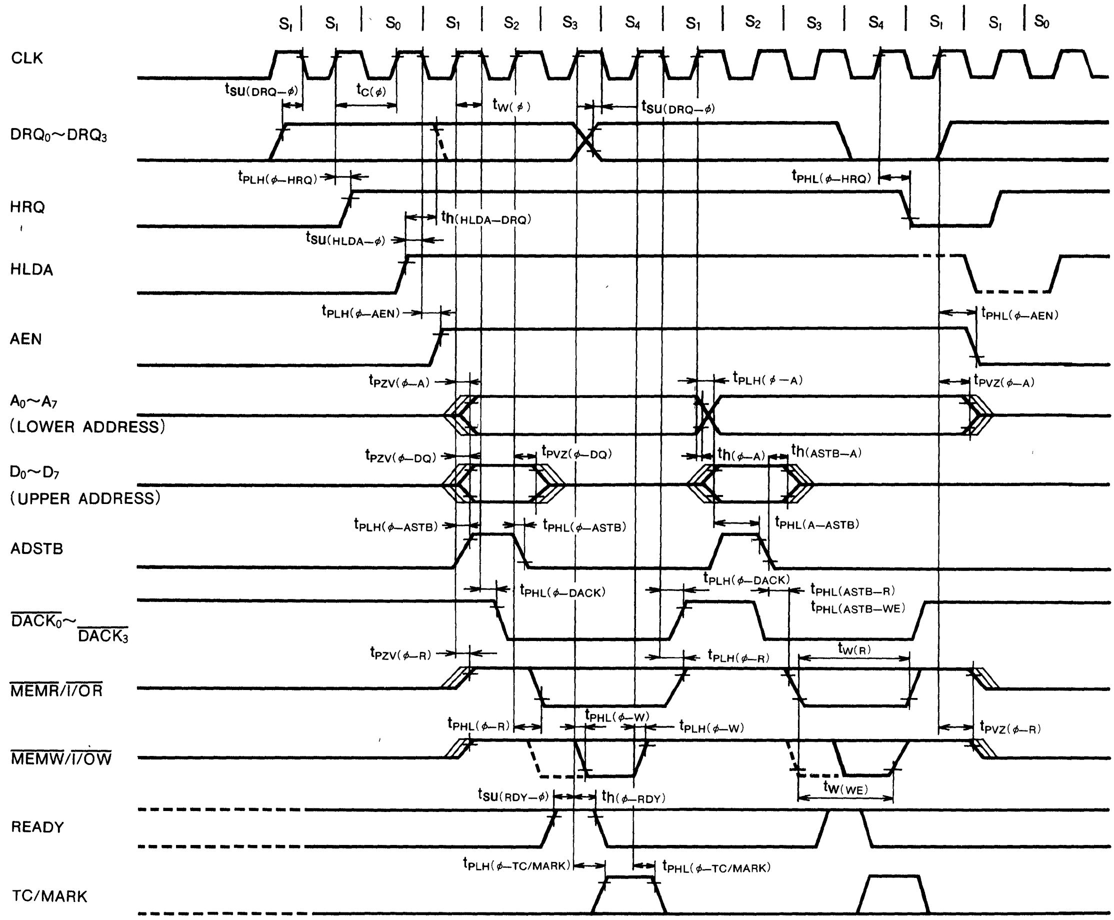
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(R)}$	Read pulse width		250			ns
$t_{su(A-R)}$ $t_{su(CS-R)}$	Address or $\overline{CS}$ setup time before read		0			ns
$t_{h(R-A)}$ $t_{h(R-CS)}$	Address or $\overline{CS}$ hold time after read		0			ns
$t_{w(W)}$	White pulse width		200			ns
$t_{su(A-W)}$	Address setup time before write		20			ns
$t_{h(W-A)}$	Address hold time after write		0			ns
$t_{su(DQ-W)}$	Data setup time before write		200			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{w(RST)}$	Reset pulse width		300			ns
$t_{su(Vcc-RST)}$	Supply voltage setup time before reset		500			ns
t_r	Input signal rise time				20	ns
t_f	Input signal fall time				20	ns
$t_{su(RST-W)}$	Reset setup time before write		2			$t_{C(\phi)}$
$t_{C(\phi)}$	Clock cycle time		0.32		4	μs
$t_{W(\phi)}$	Clock pulse width high-level		80		$0.8t_{C(\phi)}$	ns
$t_{su(DRQ-\phi)}$	DRQ setup time before clock		70			ns
$t_{h(HLDA-DRQ)}$	DRQ hold time after HLDA		0			ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock		100			ns
$t_{su(RDY-\phi)}$	Ready setup time before clock		30			ns
$t_{h(\phi-RDY)}$	Ready hold time after clock		20			ns

SLAVE MODE SWITCHING CHARACTERISTICS ($T_a=-20\sim75°C$, $V_{CC}=5V\pm5\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{PZV(R-DQ)}$	Output data enable time after read	$C_L=150pF$	0		200	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		20		100	ns

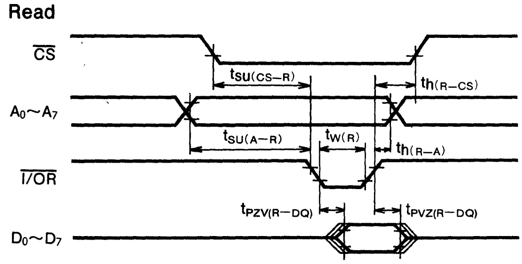
TIMING DIAGRAMS

DMA Mode

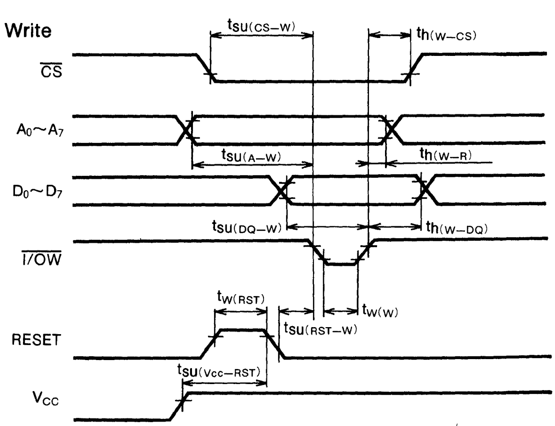


Slave Mode

Read



Write



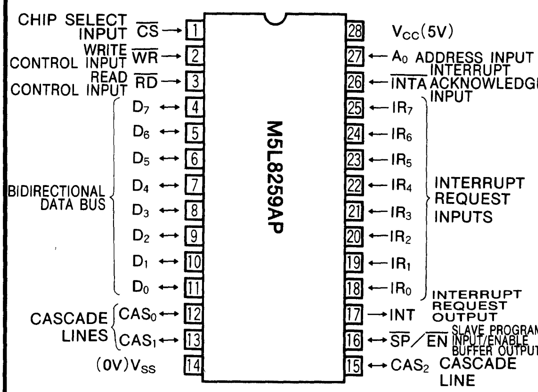
MITSUBISHI
ELECTRIC

DESCRIPTION
The M5L8259AP is a programmable LSI for interrupt control. It is fabricated using N-channel silicon-gate ED-MOS technology and is designed to be used easily in connection with an MELPS85, MELPS86 or MELPS88.

FEATURES
- Single 5V supply voltage
- TTL compatible
- CALL instruction to the CPU is generated automatically
- Priority, interrupt mask and vectored address for each interrupt request input are programmable
- Up to 64 levels of interrupt requests can be controlled by cascading with M5L8259AP
- Polling functions

APPLICATION
The M5L8259AP can be used as an interrupt controller for MELPS85, MELPS86 and MELPS88.

PIN CONFIGURATION (TOP VIEW)

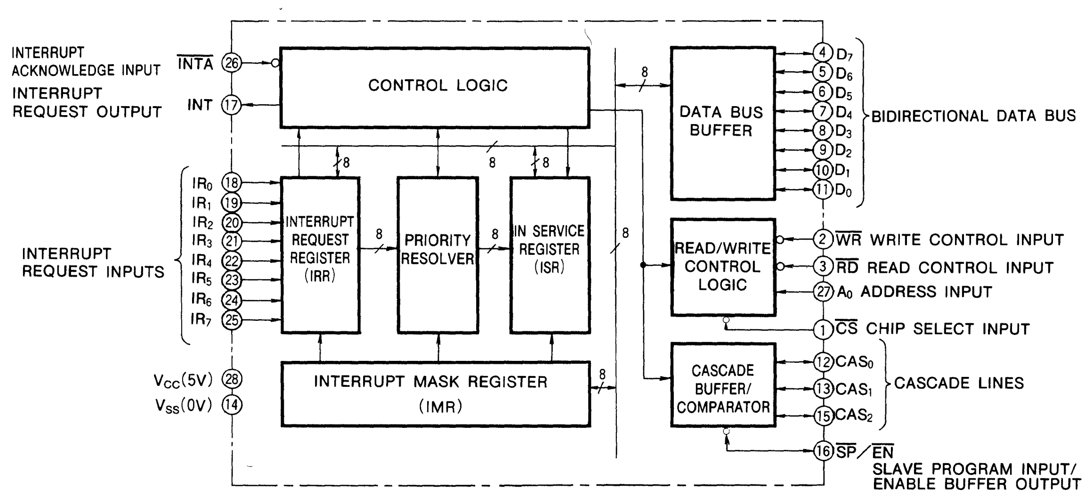


Outline 28P4

FUNCTION
The M5L8259AP is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight level requests and has built-in features for expandability to other M5L8259APs. The priority and interrupt mask can be changed or reconfigured at any time by the main program

When an interrupt is generated because of an interrupt request at 1 of the pins, the M5L8259AP based on the mask and priority will output an INT to the CPU. After that, when an $\overline{INTA}$ signal is received from the CPU or the system controller, a CALL instruction and a programmed vector address is released onto the data bus.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

Interrupt Sequence

1. When the CPU is a MELPS85

(1) When one or more of the interrupt request inputs are raised high-level, the corresponding IRR bit(s) for the high-level inputs will be set

(2) Mask state and priority levels are considered and, if appropriate, the M5L8259AP sends an INT signal to the CPU.

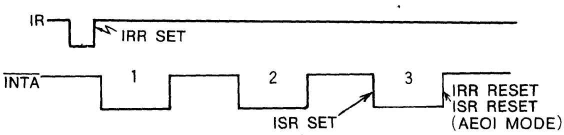
(3) The acknowledgement of the CPU to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5L8259AP.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, a CALL instruction is released onto the data bus.

(5) A CALL is a 3-byte instruction, so additional two $\overline{INTA}$ pulses are issued to the M5L8259AP from the CPU.

(6) These two $\overline{INTA}$ pulses allow the M5L8259AP to release the program address onto the data bus. The low-order 8 bits vectored address is released at the second $\overline{INTA}$ pulse and the high-order 8 bits vectored address is released at the third $\overline{INTA}$ pulse. The ISR bit corresponding to the interrupt request input is set upon receiving the third $\overline{INTA}$ pulse from the CPU, and the corresponding IRR bit is reset.

(7) This completes the 3-byte CALL instruction and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the third $\overline{INTA}$ pulse in the AEOI mode In the other modes the ISR bit is not reset until an EOI command is issued.



2. When the CPU is a MELPS86 or MELPS88

(1) When one or more of the interrupt request inputs are raised high-level, the corresponding IRR bit(s) for the high-level inputs will be set.

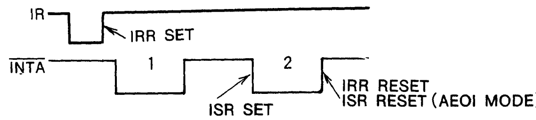
(2) Mask state and priority levels are considered and if appropriated, the M5L8259AP sends an INT signal to the CPU.

(3) As an acknowledgement to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5L8259AP.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, the M5L8259AP does not drive the data bus, and the data bus keeps high-impedance state.

(5) When the second $\overline{INTA}$ pulse is issued from the CPU, an 8-bit pointer is released onto the data bus.

(6) This completes the interrupt cycle and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the second $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued from the CPU.



The interrupt request input must be held at high-level until the first $\overline{INTA}$ pulse is issued. If it is allowed to return to low-level before the first $\overline{INTA}$ pulse is issued, an interrupt request in IR_7 is executed. However, in this case the ISR bit is not set.
This is a function for a noise countermeasure of interrupt request inputs. In the interrupt routine of IR_7, if ISR is checked by software either the interrupt by noise or real interrupt can be acknowledged. In the state of edge trigger mode normally the interrupt request inputs hold high-level and its input low-level pulse in the case of interrupt

Interrupt sequence outputs

1. When the CPU is a MELPS85

A CALL instruction is released onto the data bus when the first $\overline{INTA}$ pulse is issued. The low-order 8 bits of the vectored address are released when the second $\overline{INTA}$ pulse is issued, and the high-order 8 bits are released when the third $\overline{INTA}$ pulse is issued. The format of these three outputs is shown in Table 2.

Table 2 Formats of interrupt CALL instruction and vectored address

First $\overline{INTA}$ pulse (CALL instruction)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

Second $\overline{INTA}$ pulse (low-order 8 bits of vectored address)

IR	Interval= 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	A_5	0	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_7	A_7	A_6	A_5	1	1	1	0	0

Read Control Input ($\overline{RD}$)
When $\overline{RD}$ goes low-level status information in the internal register of the M5L8259AP can be read through the data bus.

Address Input (A_0)
The address input is normally connected with one of the address lines and is used along with $\overline{WR}$ and $\overline{RD}$ to control write commands and reading status information.

Cascade Buffer/Comparator
The cascade buffer/comparator stores or compares identification codes. The three cascade lines are output when the M5L8259AP is a master or input when it is a slave. The identification code on the cascade lines select it as master or slave.

PROGRAMMING THE M5L8259AP

The M5L8259AP is programmed through the Initialization Command Word (ICW) and the operation command word (OCW). The following explains the functions of these two commands.

Initialization Command Words (ICW_S)
The initialization command word is used for the initial setting of the M5L8259AP. There are four commands in this group and the following explains the details of these four commands. The command flow of ICWs is shown Fig. 2.

ICW1
The meaning of the bits of ICW1 is explained in Fig. 3 along with the functions. ICW1 contains vectored address bits $A_7 \sim A_5$, a flag indicating whether interrupt input is edge triggered or level triggered, CALL address interval, whether a single M5L8259AP or the cascade mode is used, and whether ICW4 is required or not.
Whenever a command is issued with $A_0=0$ and $D_4=1$, this is interpreted as ICW1 and the following will automatically occur.

(a) The interrupt mask register (IMR) is cleared.
(b) The interrupt request input IR_7 is assigned the lowest priority.
(c) The special mask mode is cleared and the status read is set to the interrupt request register (IRR).
(d) When IC4=0 all bits in ICW4 are set to 0.

ICW2
ICW2 contains vectored address bits $A_{15} \sim A_8$ or interrupt type $T_7 \sim T_3$, and the format is shown in Fig. 3.

ICW3
When SNGL=1 it indicates that only a single M5L8259AP is used in the system, in which case ICW3 is not valid. When SNGL=0, ICW3 is valid and indicates cascade connections with other M5L8259AP devices. In the master mode, a 1 is set for each slave.
When the CPU is a MELPS85 the CALL instruction is released from the master at the first $\overline{INTA}$ pulse and the vectored address is released onto the data bus from the slave at the second and third $\overline{INTA}$ pulses.
When the CPU is a MELPS86 the master and slave are in high-impedance at the first $\overline{INTA}$ pulse and the pointer is released onto the data bus from the slave at the second $\overline{INTA}$ pulse.

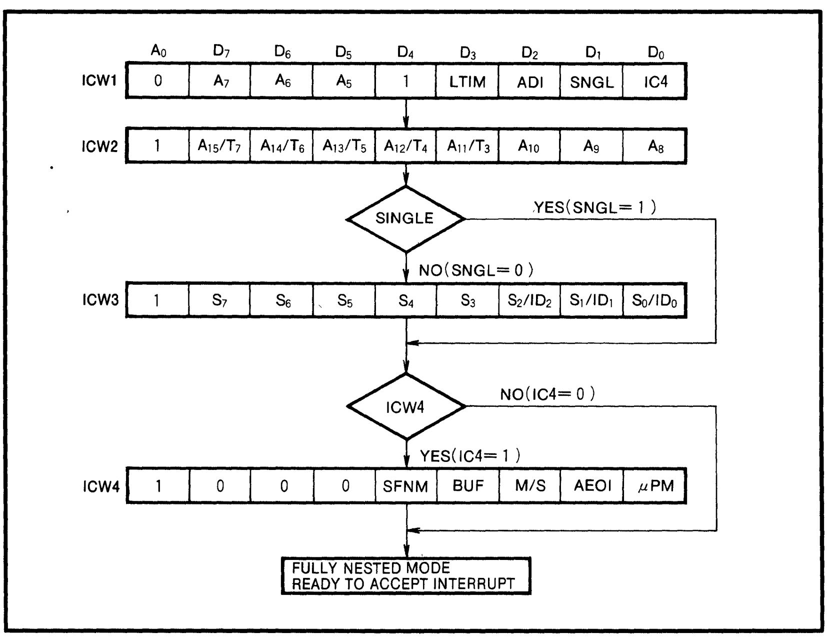


Fig. 2 Initialization sequence

The master mode is specified when $\overline{SP}/\overline{EN}$ pin is high-level or BUF=1 and M/S=1 in ICW4, and slave mode is specified when $\overline{SP}/\overline{EN}$ pin is low-level or BUF = 1 and M/S = 0 in ICW4. In the slave mode, three bits $ID_2 \sim ID_0$ identify the slave. And then when the slave code released on the cascade lines from the master, matches the assigned ID code, the vectored address is released by it onto the data bus at the next $\overline{INTA}$ pulse.

ICW4

Only when IC4=1 in ICW1 is ICW4 valid. Otherwise all bits are set to 0. When ICW4 is valid it specifies special fully nested mode, buffer mode, master/slave, automatic EOI and microprocessor mode The format of ICW4 is shown in Fig. 3.

Operation Command Words (OCW_S)

The operation command words are used to change the contents of IMR, the priority of interrupt request inputs and the special mask. After the ICW are programmed into the M5L8259AP, the device is ready to accept interrupt requests. There are three types of OCW_S; explanation of each follows, and the format of OCW_S is shown in Fig. 4.

OCW1

The meaning of the bits of OCW1 are explained in Fig. 4 along with their functions. Each bit of IMR can be independently changed (set or reset) by OCW1.

OCW2

The OCW2 is used for issuing EOI commands to the M5L8259AP and for changing the priority of the interrupt re-

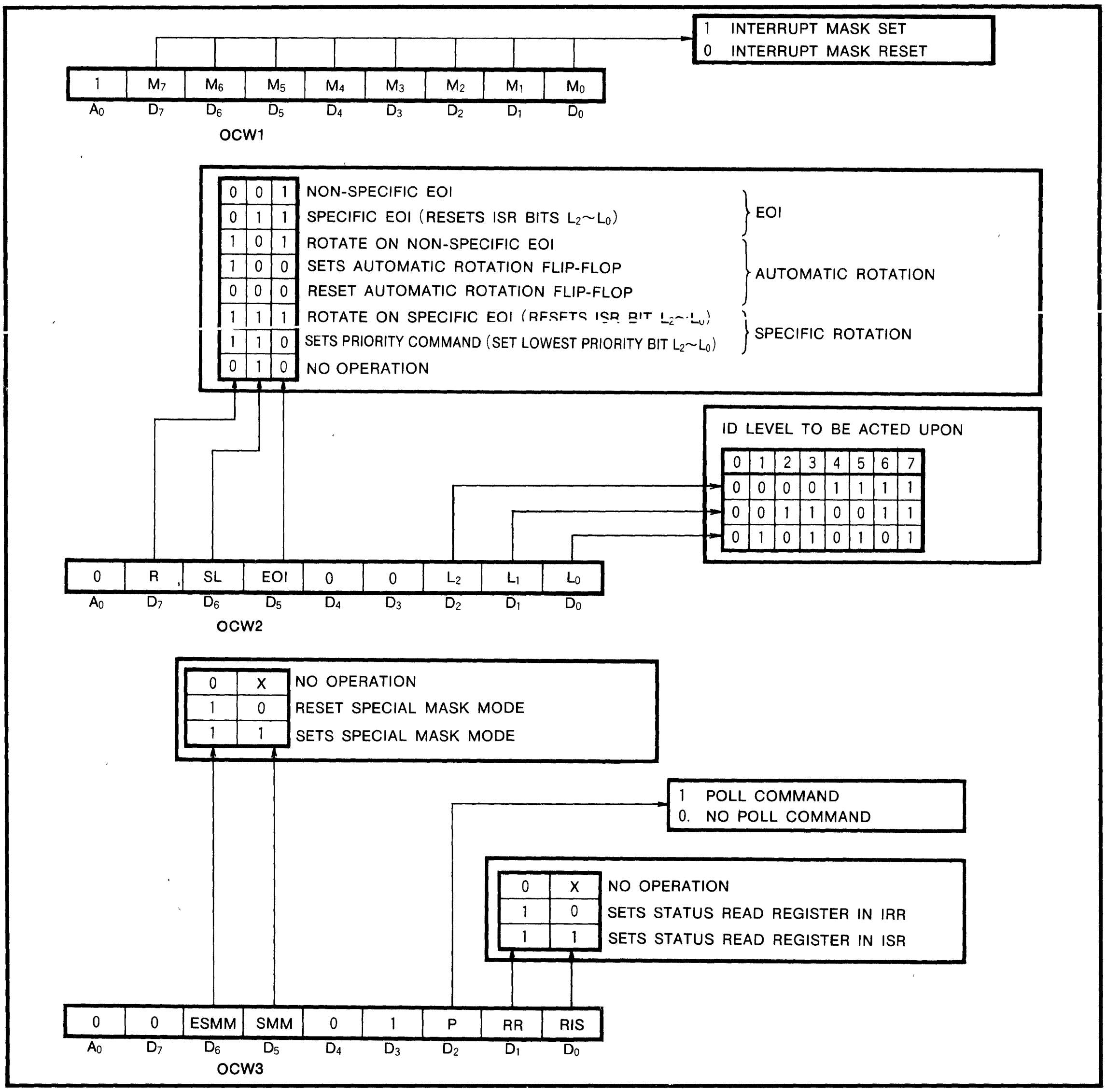


Fig. 4 Operation command word format

mode. When the M5L8259AP is in special mask mode ISR bits masked in IMR are not reset by EOI. EOI and SEOI are selected when OCW2 is executed.

Automatic EOI (AEOI)

In the AEOI mode the M5L8259AP executes non-specific EOI command automatically at the trailing edge of the last $\overline{\text{INTA}}$ pulse. When AEOI=1 in ICW4, the M5L8259AP is put in AEOI mode continuously until reprogrammed in ICW4.
The AEOI mode can only be used in a master M5L8259AP and not a slave.

Automatic rotation

The automatic rotation mode is used in applications where many interrupt requests of the same level are expected such as multichannel communication systems. In this mode when an interrupt request is serviced, that request is assigned the lowest priority so that if there are other interrupt requests they will have higher priorities. This means that the next request on the interrupt request being serviced must wait until the other interrupt requests are serviced (worst case is waiting for all 7 of the other controllers to be serviced). The priority and serving status are rotated as shown in Fig. 5.

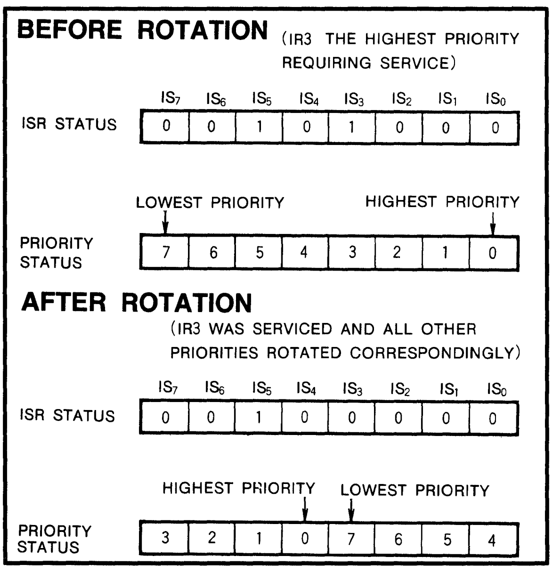


Fig. 5 An example of priority rotation

In the non-specific EOI command automatic rotation mode is selected when R=1, EOI=1, SL=0 in OCW2. The internal priority status is changed by EOI or AEOI commands. The rotation priority A flip-flop is set by R=1, EOI=0 and SL=0 which is useful when the M5L8259AP is used in the AEOI mode.

Specific rotation

Specific rotation gives the user versatile capabilities in interrupt controlled operations. It serves in those applications in which a specific device's interrupt priority must be altered. As opposed to automatic rotation which automatically sets priorities, specific rotation is completely user controlled. That is, the user selects the interrupt level that is to receive lowest or highest priority. Priority changes can be executed during an EOI command.

Level triggered mode/Edge triggered mode

Selection of level or edge triggered mode of the M5L8259AP is made by ICW1, When using edge triggered mode not only is a transition from low-level to high-level required, but the high-level must be held until the first $\overline{\text{INTA}}$. If the high-level is not held until the first $\overline{\text{INTA}}$, the interrupt request will be treated as if it were input on IR_7, except that the ISR bit is not set. When level triggered mode is used the functions are the same as edge triggered mode except that the transition from low-level to high-level is not required to trigger the interrrupt request.
In the level triggered mode and using AEOI mode together, if the high-level is held too long the interrupt will occur immediately. To avoid this situation interrupts should be kept disabled until the end of the service routine or until the IR input returns low-level. In the edge triggered mode this type of mistake is not possible because the interrupt request is edge triggered.

Reading the M5L8259AP internal status

The contents of IRR and ISR can be read by the CPU with status read. When an OCW3 is issued to the M5L8259AP and an $\overline{\text{RD}}$ pulse issued the contents of IRR or ISR can be released onto the data bus. A special command is not required to read the contents of IMR. The contents of IMR can be released onto the data bus by issuing an $\overline{\text{RD}}$ pulse when A_0=1. There is no need to issue a read register command every time the IRR or ISR is to be read. Once a read register command is received by the M5L8259AP, it remains valid until it is changed. Remember that the programmer must issue a poll command every time to check whether there is an interrupt request and read the priority level. Polling overrides status read when P=1, RR=1 in OCW3.

CASCADING

The M5L8259AP can be interconnected in a system of one master with up to 8 slaves to handle up to 64 priority levels. A system of 3 units that can be used with the MELPS85 is shown in Fig. 6.
The master can select a slave by outputting its identification code through the 3 cascade lines. The INT output of each slave is connected to the master interrupt request inputs. When an interrupt request of one of the slaves is to be serviced the master outputs the identification code of the slave through the cascade lines, so the slave will release the vectored address on the next $\overline{\text{INTA}}$ pulse.
The cascade lines of the master are nomally low-level, and will contain the slave identification code from the leading edge of the first $\overline{\text{INTA}}$ pulse to the trailing edge of the last

INSTRUCTION SET

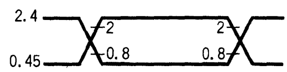
Item / Number	Mnemonic	Instruction code									Function			
		A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	ICW4 required?	Intervel	Single	Trigger
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	N	4	Y	E
2	ICW1 B	0	A_7	A_6	A_5	1	1	1	1	0	N	4	Y	L
3	ICW1 C	0	A_7	A_6	A_5	1	0	1	0	0	N	4	N	E
4	ICW1 D	0	A_7	A_6	A_5	1	1	1	0	0	N	4	N	L
5	ICW1 E	0	A_7	A_6	0	1	0	0	1	0	N	8	Y	E
6	ICW1 F	0	A_7	A_6	0	1	1	0	1	0	N	8	Y	L
7	ICW1 G	0	A_7	A_6	0	1	0	0	0	0	N	8	N	E
8	ICW1 H	0	A_7	A_6	0	1	1	0	0	0	N	8	N	L
9	ICW1 I	0	A_7	A_6	A_5	1	0	1	1	1	Y	4	Y	E
10	ICW1 J	0	A_7	A_6	A_5	1	1	1	1	1	Y	4	Y	L
11	ICW1 K	0	A_7	A_6	A_5	1	0	1	0	1	Y	4	N	E
12	ICW1 L	0	A_7	A_6	A_5	1	1	1	0	1	Y	4	N	L
13	ICW1 M	0	A_7	A_6	0	1	0	0	1	1	Y	8	Y	E
14	ICW1 N	0	A_7	A_6	0	1	1	0	1	1	Y	8	Y	L
15	ICW1 O	0	A_7	A_6	0	1	0	0	0	1	Y	8	N	E
16	ICW1 P	0	A_7	A_6	0	1	1	0	0	1	Y	8	N	L
17	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	8-bit vectored address			
18	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Slave connections (master mode)			
19	ICW3 S	1	0	0	0	0	0	ID_2	ID_1	ID_0	Slave identification code (slave mode)			
											SFNM	BUF	AEOI	MELPS86
20	ICW4 A	1	0	0	0	0	0	0	0	0	N	N	N	N
21	ICW4 B	1	0	0	0	0	0	0	0	1	N	N	N	Y
22	ICW4 C	1	0	0	0	0	0	0	1	0	N	N	Y	N
23	ICW4 D	1	0	0	0	0	0	0	1	1	N	N	Y	Y
24	ICW4 E	1	0	0	0	0	0	1	0	0	N	N	N	N
25	ICW4 F	1	0	0	0	0	0	1	0	1	N	N	N	Y
26	ICW4 G	1	0	0	0	0	0	1	1	0	N	N	Y	N
27	ICW4 H	1	0	0	0	0	0	1	1	1	N	N	Y	Y
28	ICW4 I	1	0	0	0	0	1	0	0	0	N	Y S	N	N
29	ICW4 J	1	0	0	0	0	1	0	0	1	N	Y S	N	Y
30	ICW4 K	1	0	0	0	0	1	0	1	0	N	Y S	Y	N
31	ICW4 L	1	0	0	0	0	1	0	1	1	N	Y S	Y	Y
32	ICW4 M	1	0	0	0	0	1	1	0	0	N	Y M	N	N
33	ICW4 N	1	0	0	0	0	1	1	0	1	N	Y M	N	Y
34	ICW4 O	1	0	0	0	0	1	1	1	0	N	Y M	Y	N
35	ICW4 P	1	0	0	0	0	1	1	1	1	N	Y M	Y	Y
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Y	N	N	N
37	ICW4 NB	1	0	0	0	1	0	0	0	1	Y	N	N	Y
38	ICW4 NC	1	0	0	0	1	0	0	1	0	Y	N	Y	N
39	ICW4 ND	1	0	0	0	1	0	0	1	1	Y	N	Y	Y
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Y	N	N	N
41	ICW4 NF	1	0	0	0	1	0	1	0	1	Y	N	N	Y
42	ICW4 NG	1	0	0	0	1	0	1	1	0	Y	N	Y	N
43	ICW4 NH	1	0	0	0	1	0	1	1	1	Y	N	Y	Y
44	ICW4 NI	1	0	0	0	1	1	0	0	0	Y	Y S	N	N
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	Y	Y S	N	Y
46	ICW4 NK	1	0	0	0	1	1	0	1	0	Y	Y S	Y	N
47	ICW4 NL	1	0	0	0	1	1	0	1	1	Y	Y S	Y	Y
48	ICW4 NM	1	0	0	0	1	1	1	0	0	Y	Y M	N	N
49	ICW4 NN	1	0	0	0	1	1	1	0	1	Y	Y M	N	Y
50	ICW4 NO	1	0	0	0	1	1	1	1	0	Y	Y M	Y	N
51	ICW4 NP	1	0	0	0	1	1	1	1	1	Y	Y M	Y	Y
52	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Interrupt mask			
53	OCW2 E	0	0	0	1	0	0	0	0	0	EOI			
54	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	SEOI			
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI command (Automatic rotation)			
56	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate on Specific EOI command (Specific rotation)			
57	OCW2 R	0	1	0	0	0	0	0	0	0	Rotate in AEOI Mode (SET)			
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Rotate in AEOI Mode (CLEAR)			
59	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	Set priority without EOI			
60	OCW3 P	0	0	0	0	0	1	1	0	0	Poll mode			
61	OCW3 RIS	0	0	0	0	0	1	0	1	1	Sets Status Read Resister in ISR			
62	OCW3 RR	0	0	0	0	0	1	0	1	0	Sets Status Read Resister in IRR			
63	OCW3 SM	0	0	1	1	0	1	0	0	0	Sets Special Mask mode			
64	OCW3 RSM	0	0	1	0	0	1	0	0	0	Reset Special Mask mode			

Note 4 · Y. yes, N no, E edge, L. level, M: master, S· slave

SWITCHING CHARACTERISTICS ($T_a=-20\sim75℃$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

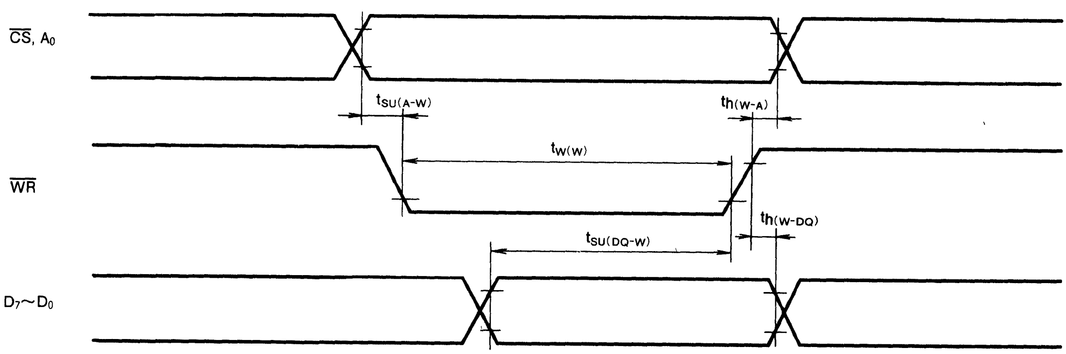
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{PZV(R-DQ)}$	Data output enable time after read	$C_L=100pF$ Where $\overline{SP}/\overline{EN}$ pin is 15pF			200	ns
$t_{PVZ(R-DQ)}$	Data output disable time after read		10		100	ns
$t_{PZV(A-DQ)}$	Data output enable time after address				200	ns
$t_{PHL(R-EN)}$	Propagation time from read to enable signal output				125	ns
$t_{PLH(R-EN)}$	Propagation time from read to disable signal output				150	ns
$t_{PLH(IR-INT)}$	Propagation time from interrupt request input to interrupt request output				350	ns
$t_{PLV(INTA-CAS)}$	Propagation time from $\overline{INTA}$ to cascade output (master)				565	ns
$t_{PZV(CAS-DQ)}$	Data output enable time after cascade output (slave)				300	ns

Note 5 : $\overline{INTA}$ signal is considered read signal
$\overline{CS}$ signal is considered address signal
Input pulse level 0.45~2.4V
Input pulse rise time 20ns
Input pulse fall time 20ns
Reference level input $V_{IH}=2V$, $V_{IL}=0.8V$
output $V_{OH}=2V$, $V_{OL}=0.8V$

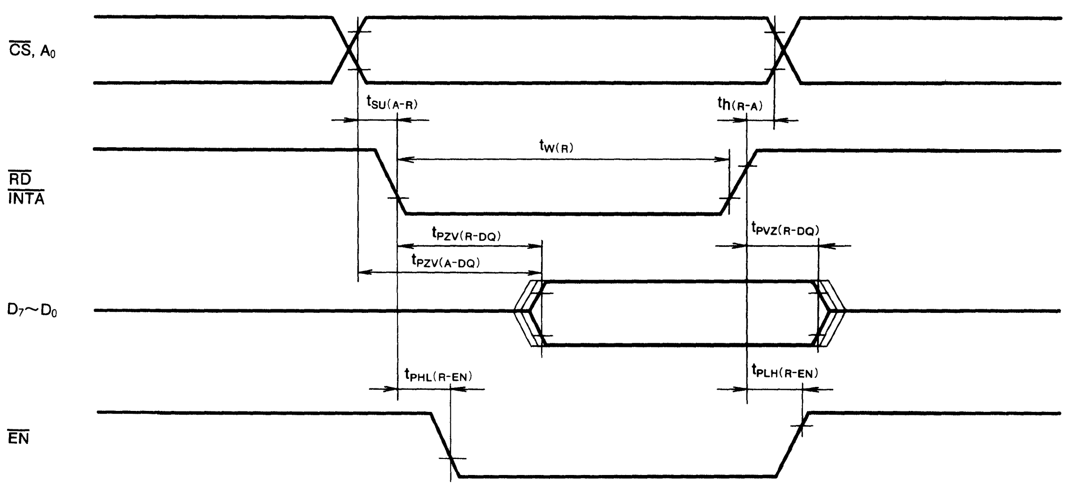


TIMING DIAGRAM

Write Mode



Read Mode



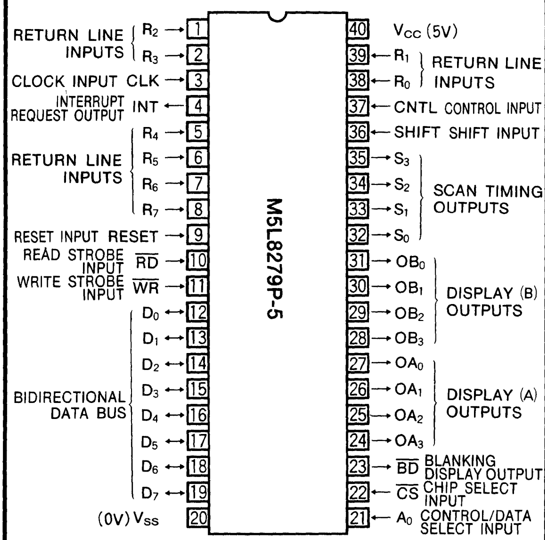
DESCRIPTION

The M5L8279P-5 is a programmable keyboard and display interface device that is designed to be used in combination with an 8-bit/16-bit microprocessor. This device is fabricated with N-channel silicon-gate ED-MOS process technology and is packed in a 40-pin DIL package. It needs only single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Keyboard mode
- Sensor matrix mode
- Strobed mode
- Internally provided key bounce protection circuit
- Programmable debounce time
- 2-key lockout/N-key rollover
- 8-character keyboard FIFO
- Internally contained 16 × 8-bit display RAM
- Programmable right and left entry

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

APPLICATION

Microcomputer I/O device

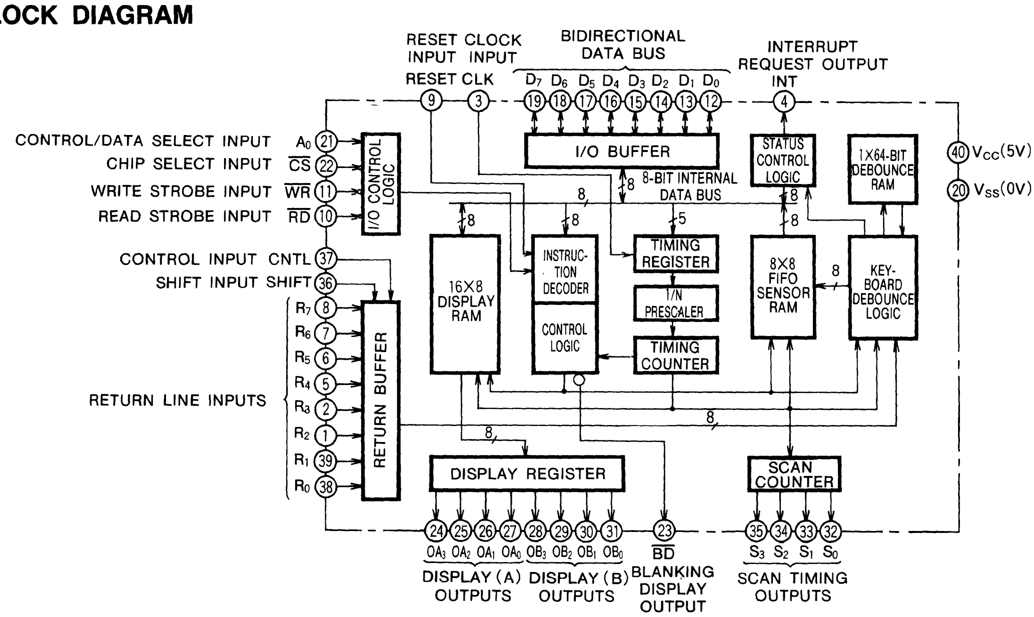
64 contact key input device for such items as electronic cash registers

Dual 8- or single 16-alphanumeric display

FUNCTION

The total chip, consisting of a keyboard interface and a display interface, can be programmed by eight 8-bit commands. The keyboard portion is provided with a 64-bit key debounce buffer and an 8 × 8-bit FIFO/SENSOR RAM. It operates in any one of the scanned keyboard mode, scanned sensor matrix mode or strobed entry mode. The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16× 4 configuration. Also, an 8-digit display configuration is possible by means of programming.

BLOCK DIAGRAM



COMMAND DESCRIPTION

There are eight commands provided for programming the operating modes of the M5L8279P-5. These commands are sent on the data bus with the signal $\overline{CS}$ in low-level and the signal A_0 in 1 and are stored in the M5L8279P-5 at the rising edge of the signal $\overline{WR}$. The order of the command execution is arbitrary.

1. Mode Set Command

	MSB							LSB
Code :	0	0	0	D	D	K	K	K

DD (Display mode set command)

DD	
0 0	8—8-bit character display—left entry
0 1	16—8-bit character display—left entry (Note1)
1 0	8—8-bit character display—right entry
1 1	16—8-bit character display—right entry

KKK (Keyboard mode set command)

KKK	
0 0 0	Encoded display keyboard mode — 2-key lockout (Note1)
0 0 1	Decoded display keyboard mode — 2-key lockout
0 1 0	Encoded display keyboard mode — N-key rollover
0 1 1	Decoded display keyboard mode — N-key rollover
1 0 0	Encoded display, sensor mode
1 0 1	Decoded display, sensor mode
1 1 0	Encoded display, strobed entry mode
1 1 1	Decoded display, strobed entry mode

Note 1 : Default after reset.

2. Program Clock Command

	MSB							LSB
Code :	0	0	1	P	P	P	P	P

The external clock is divided by the prescaler value PPPPP designated by this command to obtain the basic internal frequency.

When the internal clock is set to 100kHz, it will give a 5.1ms keyboard scan time and a 10.3ms debounce time. The prescale value that can be specified by PPPPP is from 2 to 31. In case PPPPP is 00000 or 00001, the prescale is set to 2. Default after a reset pulse is 31, but the prescale value is not cleared by the clear command.

3. Read FIFO Command

	MSB							LSB	
Code :	0	1	0	AI	X	A	A	A	X = Don't care

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the FIFO. As long as data is to be read from the FIFO, no additional commands are necessary.

AI and AAA are used only in the sensor mode. AAA designates the address of the FIFO to be read, and AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read operation. This auto-increment bit does not affect the auto-increment of the display RAM.

4. Read Display RAM Command

	MSB							LSB
Code :	0	1	1	AI	A	A	A	A

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the display RAM. As long as data is to be read from the display RAM, no additional commands are necessary.

The data AAAA is the value with which the display RAM read/write counter is set, and it specifies the address of the display RAM to be read or written next.

AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read/write operation. This auto-increment bit does not affect the auto-increment of FIFO readout in the sensor mode.

5. Write Display RAM Command

	MSB							LSB
Code :	1	0	0	AI	A	A	A	A

With this command, following display RAM read/write addressing is achieved without changing the data readout source (FIFO or display RAM). Meaning of AI and AAAA are identical with read display RAM command.

6. Display Write inhibit/Blanking Command

	MSB							LSB	
Code :	1	0	1	X	IW	IW	BL	BL	X = Don't care
					A	B	A	B	

The IW is a write inhibit bit to the display RAM that corresponds with the output A or B. Inhibit is activated by turning the IW 1.

The BL is used in blanking the out A or B. Blanking is activated by turning the BL 1. Setting both BL flags makes the signal $\overline{BD}$ low-level so that it can be used in 8-bit display mode.

Resetting the flags makes all IW and BL turn 0.

7. Clear Command

	MBS							LSB
Code :	1	1	0	C_D	C_D	C_D	C_F	C_A

C_D: Clears the display RAM.

C_D	C_D	C_D	
0	X	X	No specific performance
1	0	X	Entire contents of the display RAM are turned 0.
1	1	0	The contents of the display RAM are turned 20H (00100000 = $0A_30A_20A_10A_0$ $0B_30B_20B_10B_0$).
1	1	1	Entire contents of the display RAM are turned 1.

CPU INTERFACE

1. Command Write

A command is written on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 1.

2. Data Write

Data is written to the display RAM on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 0.

The address of the display RAM is also incremented on the rising edge of the signal $\overline{WR}$ if AI is set for the display RAM.

3. Status Read

The status word is read when $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 1. The status word appears on the data bus as long as the signal $\overline{RD}$ is low-level.

4. Data Read

Data is read from either the FIFO or the display RAM with $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 0. The source of the data (FIFO or display RAM) is decided by the latest command (read display or read FIFO). The data read appears on the data bus as long as the signal $\overline{RD}$ is low-level.

The trailing edge of the signal $\overline{RD}$ increments the address of the FIFO or the display RAM when AI is set. After the reset, data will be read from the FIFO, however.

A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Operation
1	L	H	L	Command write
0	L	H	L	Data write
1	L	L	H	Status read
0	L	L	H	Data read
X	H	X	X	No operation

KEYBOARD INTERFACE

Keyboard interface is done by the scan timing signals ($S_0 \sim S_3$), the return line inputs ($R_0 \sim R_7$), the SHIFT and the CNTRL inputs.

In the decoded mode, the low-order of 2 bits of the internal scan counter are decoded and come out on the timing pins ($S_0 \sim S_3$). In the encoded mode, the four binary bits of the scan counter are directly output on the timing pins, thus a 3-to-8 decoder must be employed to generate keyboard scan timing.

The return line inputs ($R_0 \sim R_7$), the SHIFT and the CNTL inputs are pulled up high-level by internal pullup transistors until a switch closure pulls one low.

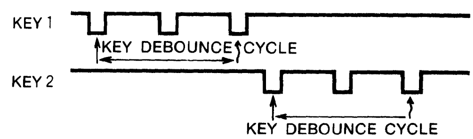
The internal key debounce logic works for a 64-key matrix that is obtained by combining the return line inputs with the scan timing.

For the keyboard interface, M5L8279P-5 has four distinctive modes that allow various kinds of applications. In the following explanation, a "key scan cycle" is the time needed to scan a 64-key matrix, and a "key debounce cycle" needs a duration of two "key scan" cycles. (In the decoded mode 32 keys, unlike 64 keys in the encoded mode, can be employed for a maximum key matrix due to the limit of timing signals However, both the key scan cycle and the key debounce cycle are the same as in the encoded mode.)

1. 2-Key Lockout (Scanned Keyboard Mode)

The detection of a new key closure resets the internal debounce counter and starts counting. At the end of a key debounce cycle, the key is checked and entered into the FIFO if it is still down. An entry in the FIFO sets the INT output high. If any other keys are depressed in a key debounce cycle, the internal key debounce counter is reset each time it encounters a new key. Thus only a single-key depression within a key debounce duration is accepted, but all keys are ignored when more than two keys are depressed at the same time.

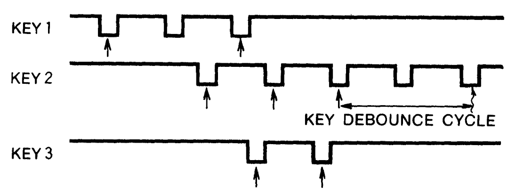
Example 1 : Accepting two successive key depressions



Note 2 : ↑ : Debounce counter reset

↑ : Key input

Example 2 : Overlapped depression of three keys



Note 3 : Only key 2 is acceptable

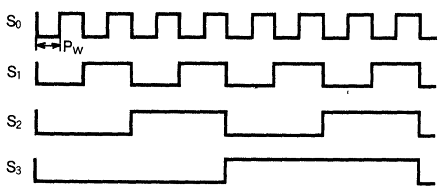
DISPLAY INTERFACE

The display interface is done by 8 display outputs ($OA_0 \sim OA_3$, $OB_0 \sim OB_3$), a blanking signal ($\overline{BD}$), and scan timing outputs ($S_0 \sim S_3$).
The relation between the data bus and the display outputs is as shown below:

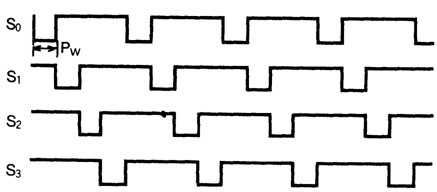
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
↓	↓	↓	↓	↓	↓	↓	↓
OA_3	OA_2	OA_1	OA_0	OB_3	OB_2	OB_1	OB_0

Clearing the display RAM is not achieved by the reset signal (9-pin) but requires the execution of the clear command.
The timing diagrams for both the encoded and decoded modes are shown below.
For the encoded mode, a 3-to-8 or 4-to-16 decoder is required, according to whether eight or sixteen digit display used.

(1) Encoded mode

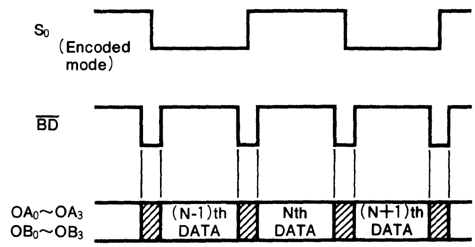


(2) Decoded mode



Note 4 : Here P_W is 640μs if the internal clock frequency is set to 100kHz.

Timing relations of S_0, $\overline{BD}$, and display outputs ($OA_0 \sim OA_3$, $OB_0 \sim OB_3$) are shown below.



Note 5 : Values of the output data shown in the slanted line areas are decided upon the clear command executed last to become the value of the display RAM after the reset. The values in the slanted areas after reset will go low-level. In the same manner, the values $OA_0 \sim OA_3$, $OB_0 \sim OB_3$ are dependent on the clear command executed last. When the both A and B are blanked, the signal $\overline{BD}$ will be in low-level.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Maximum power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−60~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted.)

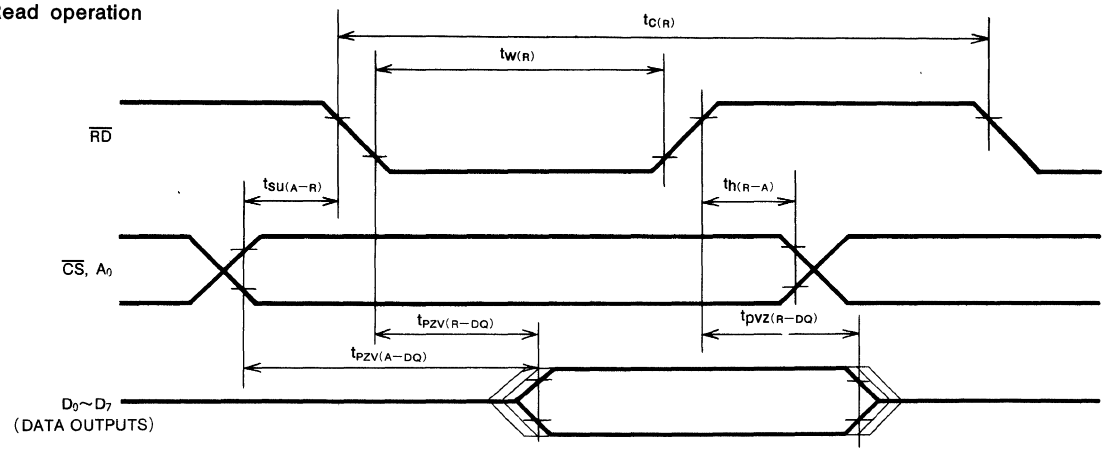
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

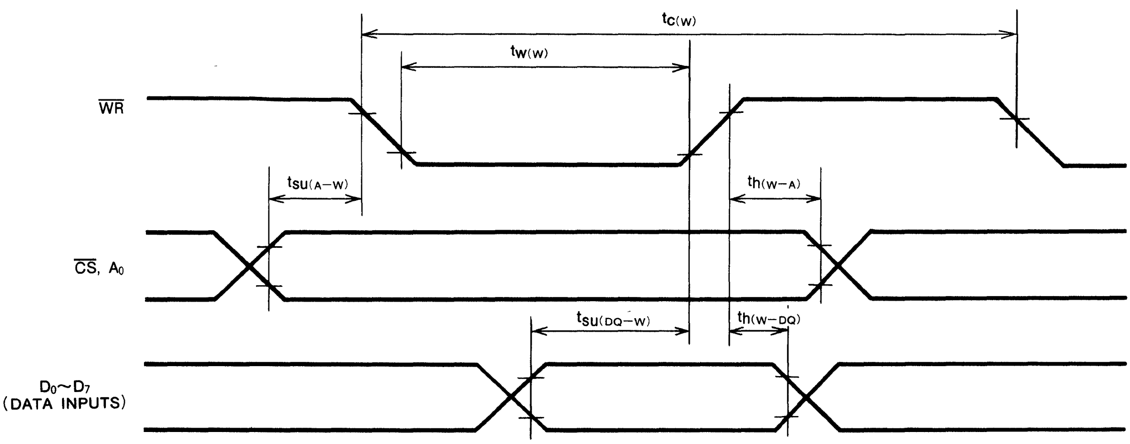
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH(RL)}$	High-level input voltage, for return line inputs		2.2			V
V_{IH}	High-level input voltage, all others		2.0			V
$V_{IL(RL)}$	Low-level input voltage, for return line inputs		V_{SS}-0.5		1.4	V
V_{IL}	Low-level input voltage, all others		V_{SS}-0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	3.5			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}				120	mA
$I_{I(RL)}$	Input current, return line inputs, shift input and control input	V_I=V_{CC}			10	μA
		V_I=0V	−100			
I_I	Input current, all others	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_I=V_{CC}	5		10	pF
C_O	Output terminal capacitance	V_O=V_{CC}	10		20	pF

TIMING DIAGRAM

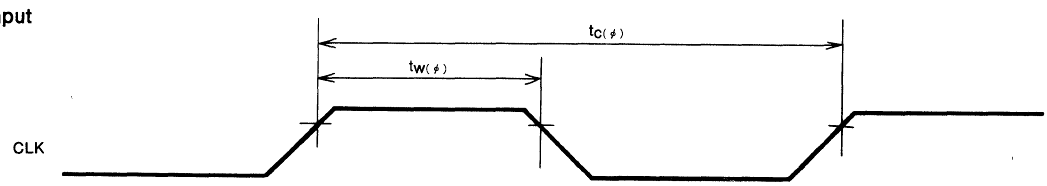
Read operation



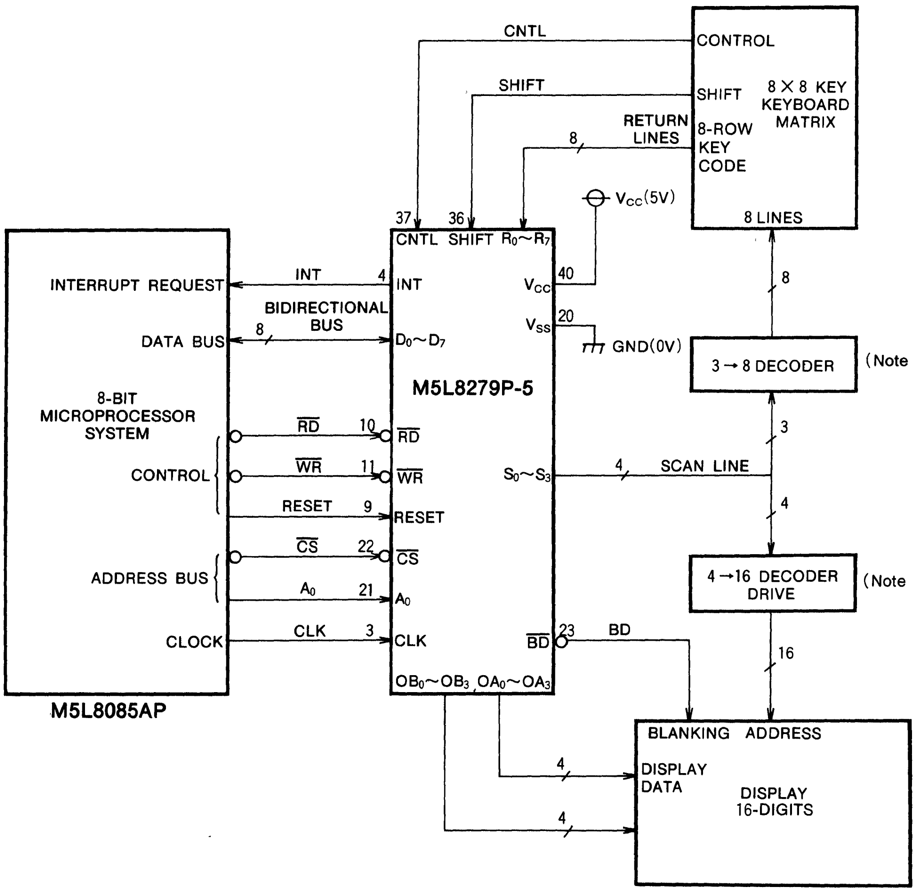
Write operation



Clock input



APPLICATION EXAMPLE



Note 8 : When using an 8-bit character display of more than 9 digits for the decoder display, it is necessary to provide two decoders for example 4 →10 decoder, 4 →16 decoder and key scan 3 → 8 decoder.
Only S_0, S_1 and S_2 may be used as inputs to the key scan 3 → 8 decoder.
(Don't drive the keyboard decoder with the MSB of the scan line)

4. TRANSFER CHARACTERISTICS AND POWER DISSIPATION

For COMS devices, the circuit threshold voltage is approximately one-half of V_{CC}. Contrasted with NMOS logic, where threshold voltage is a fixed level not related to supply voltage, ideal transfer characteristics can be achieved.
In order to maintain compatibility with the conventional NMOS devices, transfer characteristics of CMOS peripherals I/O circuits have been established at TTL level.
Fig. 4 illustrates input voltage V_{IN} versus supply current I_{CC} for M5M82C55AP-2. Here, when V_{IN} reaches 1.3 to 1.5V, the resulting switch in internal circuits causes a sharp increase in I_{CC} flow.

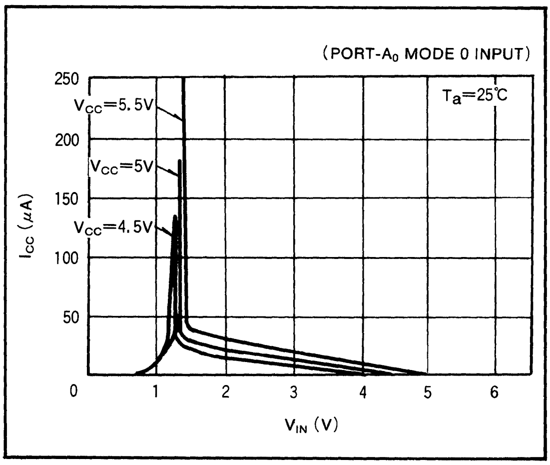


Fig. 4 Input voltage vs. dissipation current
M5M82C55AP-2

In a CMOS curcuit, since p-channel and n-channel transistors are connected in series between the V_{CC} and V_{SS}, as long as gate voltage is at the V_{CC} or V_{SS} level, one of the two transistors will be in an off state. Consequently, fixing the input pin at the V_{CC} or V_{SS} level causes the static dissipation current (I_{CC}) flow from the V_{CC} to V_{SS} pin to consist only of p-n junction leakage current. As a consequence, the per-gate static dissipation current remains at about 50pA at T_a = 25℃, and will not go over more than a few nanoamperes even at T_a=85℃. This is the primary reason behind CMOS devices low power dissipation.
Note however that power dissipation does increase when CMOS circuits are used in the switching mode. As was mentioned in the transfer characteristic description, transients in the input voltage cause current to flow from the V_{CC} to V_{SS}. The amount of current flow increases relative to higher V_{CC} values and operating frequency. Additionally, when capacitive loads (load capacitance also varies depending on the number of fanouts) are connected to the device, charging currents will be requied, which also increases power dissipation.
The M5M82C55AP-2 illustrated in Fig. 4 has parallel-connected I/O ports, and is relatively limited in switching operations. However, devices such as the programmable timer M5M82C54P are subjected to constant clock operations, and the current flow for each CMOS circuit must be added to get the total for the device. As shown in Fing. 5, currnet dissipation increases along with increases in operating frequency.

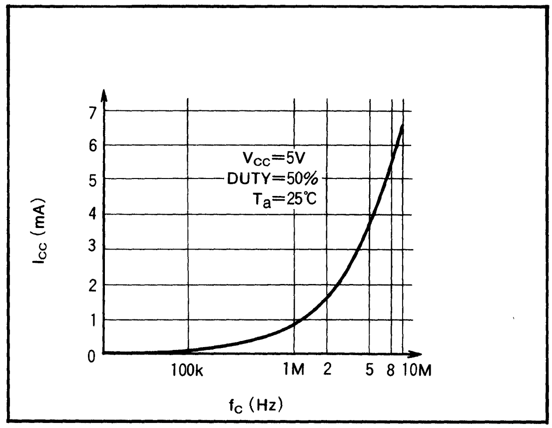


Fig. 5 Operating frequency vs. power dissipation
M5M82C54P

The power dissipation characteristics of DMA controller M5M82C37AP-5 are illustrated in Fig.6.

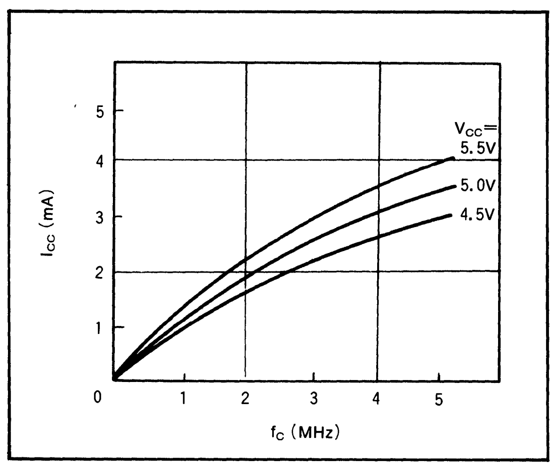


Fig. 6 Operating frequency vs. power dissipation
M5M82C37AP-5

be driven, so signal switching response is slower. In this case, the load (s) to be driven must be divided (or allocated to several devices) as with previous devices.

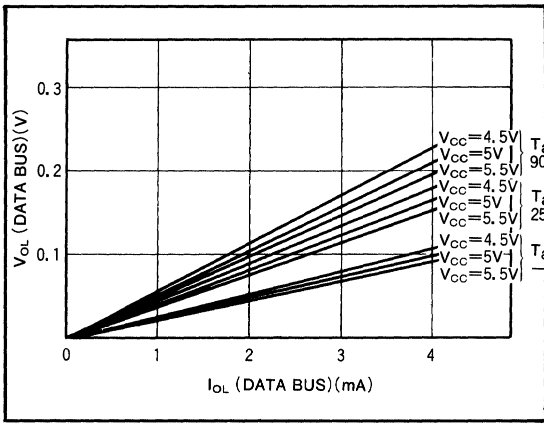


Fig. 9 I_{OL}-V_{OL} characteristics M5M82C55AP-2

7. INPUT CIRCUIT

Fig. 10 shows an equivalent circuit diagram of the input circuit for CMOS peripheral devices. The gate oxide layer of the transistors is extremely thin, and high voltages applied directly to the gates are likely to rupture their insulation, causing permanent demage to the device. To prevent gate damage, the diodes and input resistor shown in the diagram form a protection circuit.

Since threshold voltage for the input transistor is set at approximately 1.5V, as noted in section 4, if the input voltage is held at this level, a through current starts to flow from V_{CC} to V_{SS}. In systems where low dissipation current is required, this characteristic can cause problems in the design of the power supply.

Where a data bus is left floating, through current is likely to become a particular problem, so bus lines should be fixed at a certain level with a pull-up (or pull-down) circuit having high resistance values.

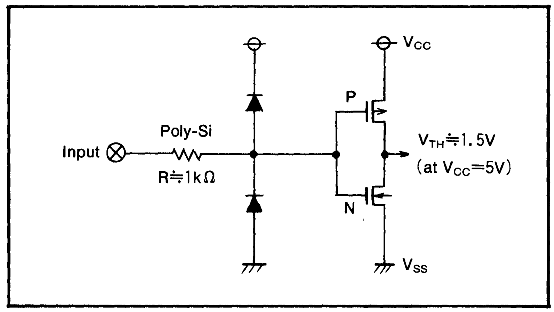


Fig. 10 CMOS peripheral device input circuit (equivalent diagram)

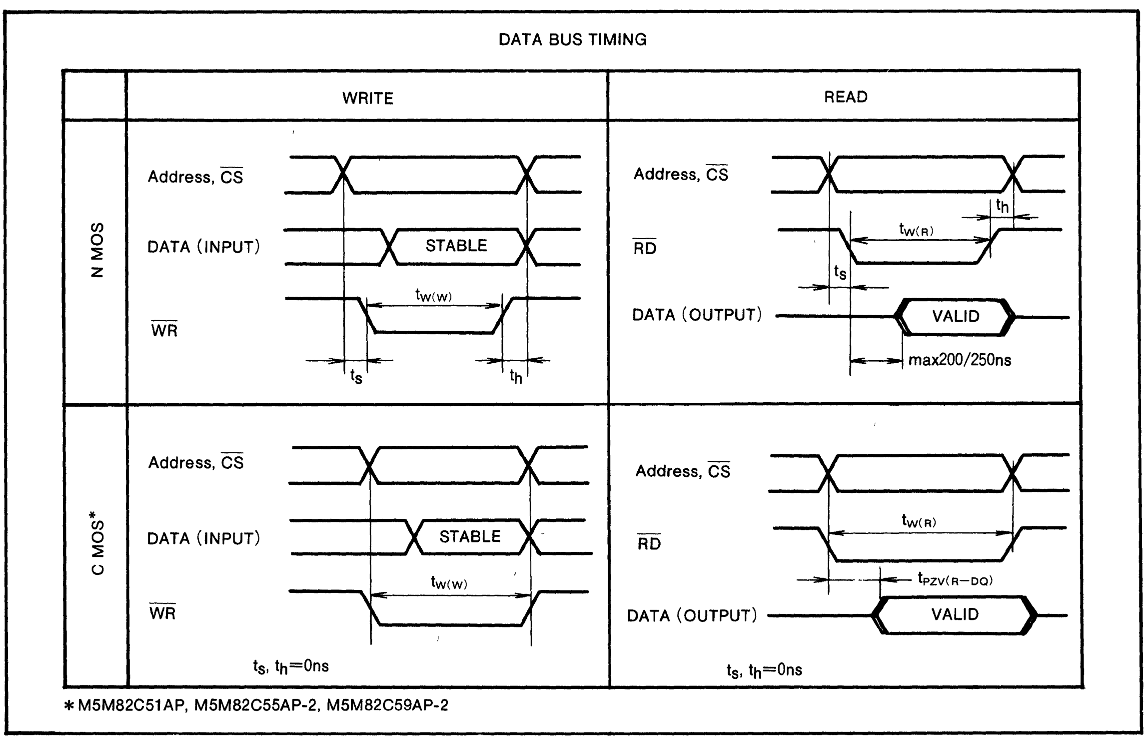


Fig. 11 Bus timing characteristics

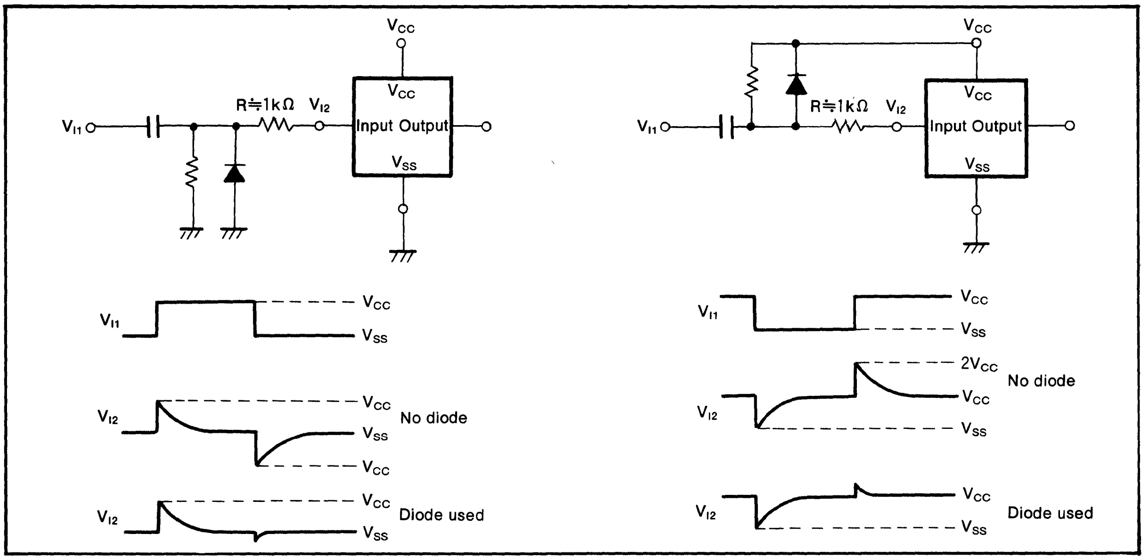


Fig. 13 Preventing latchup when using differential circuits

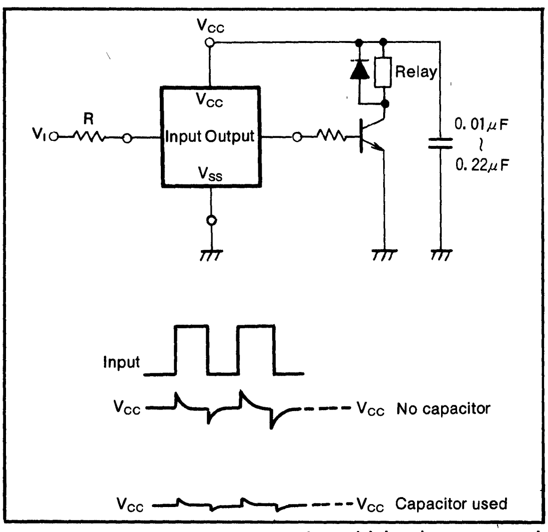


Fig. 14 Preventing latchup when driving large current circuits

Conditions (b) or (d)

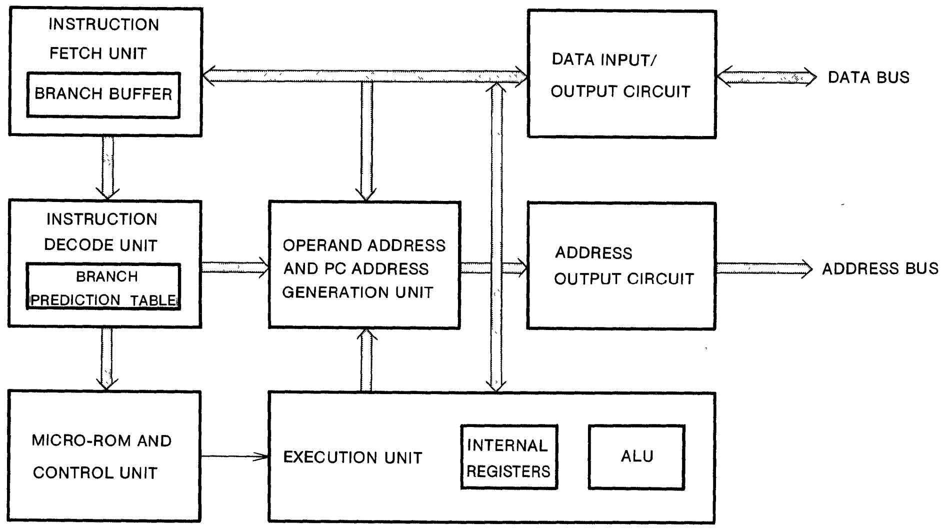
Applying a constant voltage to an output pin is not one of the normal usage configurations of a CMOS device, but a capacitor connected between output and V_{CC} (or V_{SS}) would be a cause for latchup. This is due to the high impedance created in the power supply line, combined with the fact that switching the power supply on and off produces fluctuations in the power supply line which causes the capacitor to discharge a trigger current.

Condition (e)

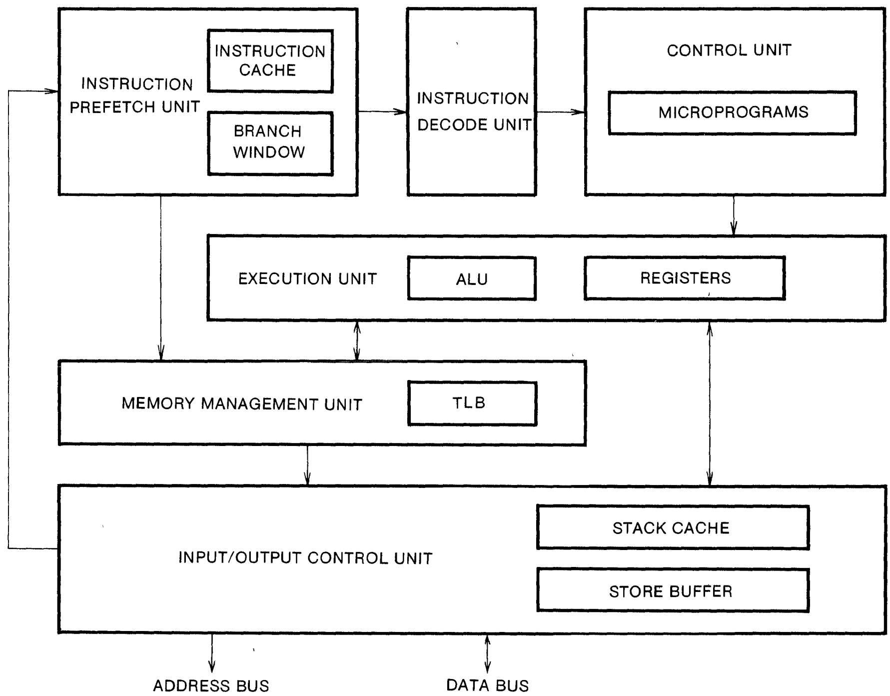
Condition (e) can be created by exceeding the absolute maximum voltage ratings at the V_{CC} pin. Also, even though V_{CC} is within the recommended operating conditions, device latchup can be caused by the surge voltage superimposing at power ON, or crosstalk between lines. The voltage at V_{CC} should never exceed absolute maximum rating values under any circumstances.

Provisions should be made to reduce power ON surge voltage to a minimum, and as described in section 6, a capacitor should be connected beteen V_{CC} and V_{SS} to reduce impedance in the power line.

BLOCK DIAGRAM



BLOCK DIAGRAM

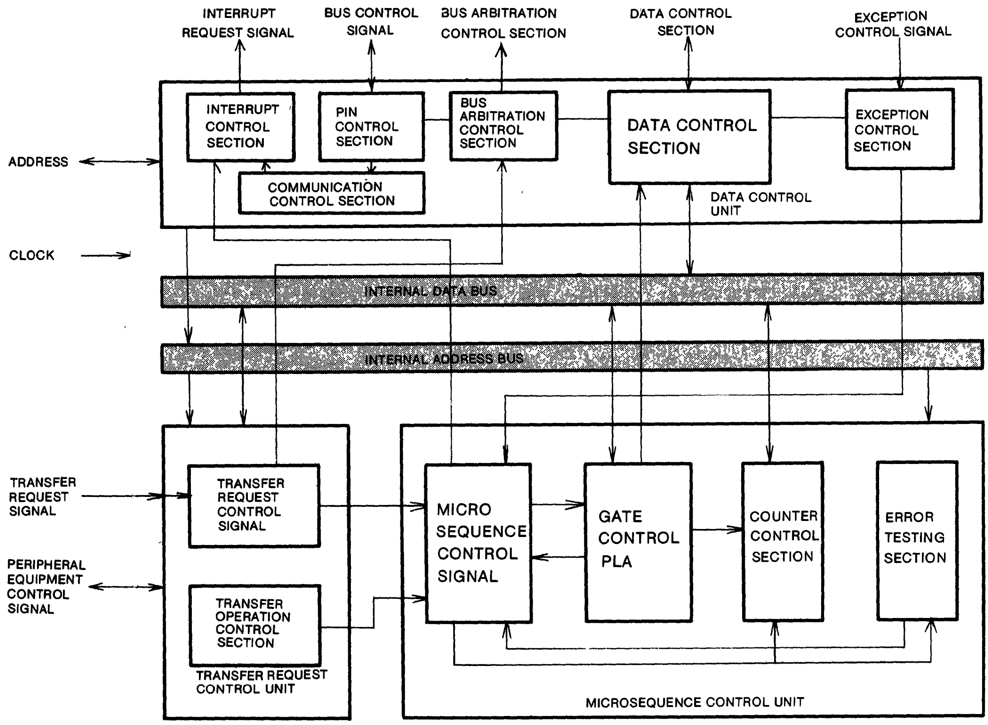


PIN ASSIGNMENT

PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME	PIN CODE	NAME
A2	*2	C3	V_{SS}	G2	$\overline{FLOAT}$	N2	A_{13}	T18	V_{CC}
A3	$\overline{OCCPRG}$	C4	$\overline{GBR}$	G3	*2	N3	A_{15}	U1	A_{22}
A4	*1	C5	WAY	G16	V_{CC}	N16	V_{SS}	U2	V_{SS}
A5	V_{SS}	C6	V_{CC}	G17	$CPST_0$	N17	A_{29}	U3	V_{CC}
A6	*2	C7	*2	G18	$CPST_1$	N18	A_{30}	U4	D_{30}
A7	$\overline{HACK}$	C8	RNG_1	H1	A_1	P1	A_{14}	U5	D_{28}
A8	V_{SS}	C9	BAT_2	H2	A_0	P2	A_{16}	U6	V_{SS}
A9	BAT_0	C10	V_{SS}	H3	V_{CC}	P3	A_{18}	U7	D_{23}
A10	$\overline{HALT}$	C11	CLKf	H16	$CPST_2$	P16	A_{24}	U8	D_{20}
A11	$\overline{HREQ}$	C12	$\overline{CLKf}$	H17	$\overline{NCA}$	P17	A_{27}	U9	V_{CC}
A12	$\overline{RESET}$	C13	V_{SS}	H18	$\overline{BLACKF}$	P18	A_{28}	U10	V_{CC}
A13	V_{CC}	C14	V_{CC}	J1	A_4	R1	A_{17}	U11	D_{18}
A14	$BCLK_1$	C15	V_{SS}	J2	A_3	R2	V_{SS}	U12	D_{15}
A15	$BCLK_2$	C16	$L/\overline{C}$	J3	A_2	R3	A_{21}	U13	D_{13}
A16	A_{19} V_{SS}	C17	$\overline{BLOCK}$	J16	$\overline{BLACKS}$	R4	V_{CC}	U14	D_{10}
A17	A_{22} $\overline{AS}$	C18	V_{SS}	J17	V_{SS}	R15	V_{SS}	U15	D_8
B1	*2	D1	IRL_0	J18	V_{CC}	R16	D_1	U16	D_7
B2	*2	D2	IRL_1	K1	A_5	R17	A_{25}	U17	D_3
B3	$\overline{ICCPRG}$	D3	*2	K2	V_{SS}	R18	A_{26}	U18	D_2
B4	$\overline{TCS}$	D15	V_{SS}	K3	A_6	T1	A_{19}	V2	V_{CC}
B5	*1	D16	$\overline{DS}$	K16	$\overline{BC_1}$	T2	A_{20}	V3	V_{SS}
B6	V_{CC}	D17	$\overline{RETRY}$	K17	$\overline{BC_2}$	T3	A_{23}	V4	D_{29}
B7	$\overline{DAT}$	D18	$\overline{BERR}$	K18	$\overline{BC_3}$	T4	V_{SS}	V5	D_{26}
B8	RNG_0	E1	*1	L1	A_7	T5	D_{31}	V6	D_{25}
B9	BAT_1	E2	*1	L2	A_8	T6	D_{27}	V7	D_{22}
B10	V_{CC}	E3	IRL_2	L3	A_9	T7	D_{24}	V8	V_{CC}
B11	V_{CC}	E16	V_{CC}	L16	$\overline{NCAO}$	T8	$CPST_2$ D_{21}	V9	V_{SS}
B12	V_{SS}	E17	$\overline{ASDC}$	L17	V_{SS}	T9	V_{SS}	V10	V_{SS}
B13	V_{SS}	E18	$\overline{SDC}$	L18	$\overline{BC_0}$	T10	V_{CC}	V11	D_{19}
B14	*2	F1	*1	M1	A_{10}	T11	D_{17}	V12	D_{16}
B15	V_{CC}	F2	*1	M2	A_{11}	T12	D_{14}	V13	V_{SS}
B16	V_{CC}	F3	*1	M3	V_{CC}	T13	D_{11}	V14	D_{12}
B17	V_{SS} $\overline{BS}$	F16	$\overline{CPDC}$	M16	A_{31}	T14	V_{SS}	V15	D_9
B18	V_{CC} $R/\overline{W}$	F17	V_{CC}	M17	$\overline{MVIN}$	T15	D_6	V16	V_{CC}
C1	V_{CC}	F18	V_{SS}	M18	$\overline{LOC}$	T16	D_4	V17	D_5
C2	V_{SS}	G1	V_{SS}	N1	A_{12}	T17	D_0		

* 1 : Connect to V_{CC}.
* 2 : No connect

BLOCK DIAGRAM



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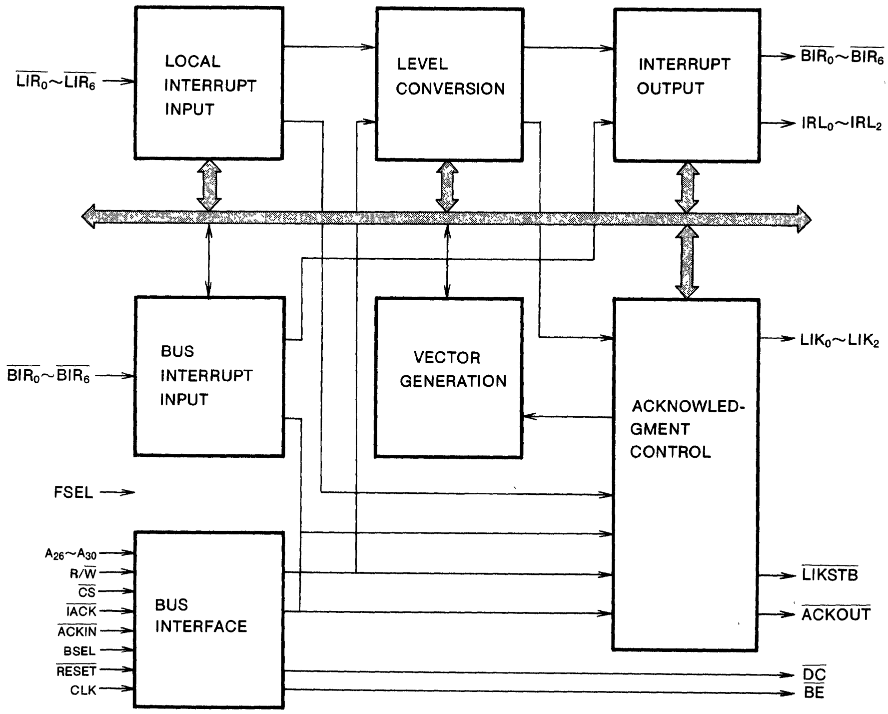
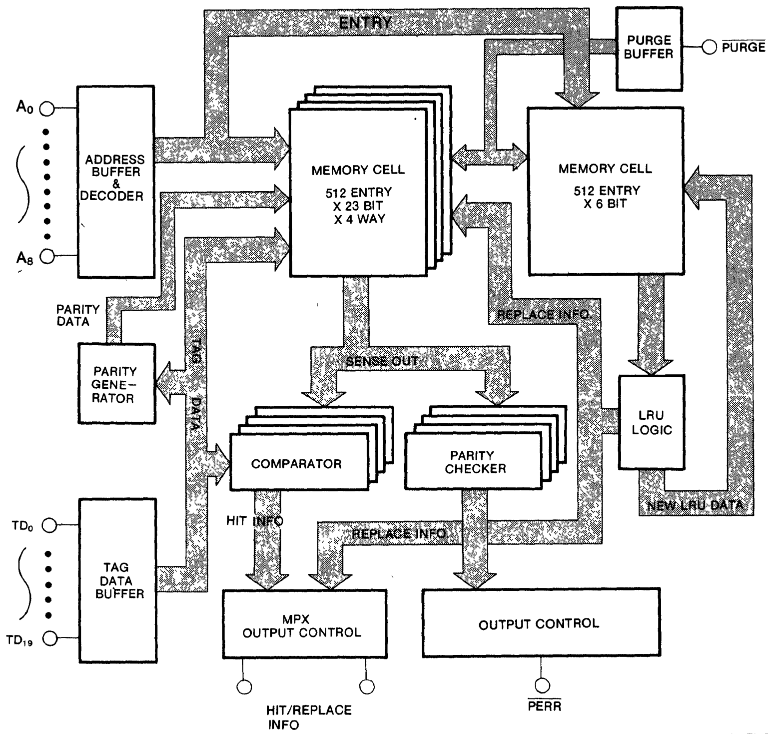
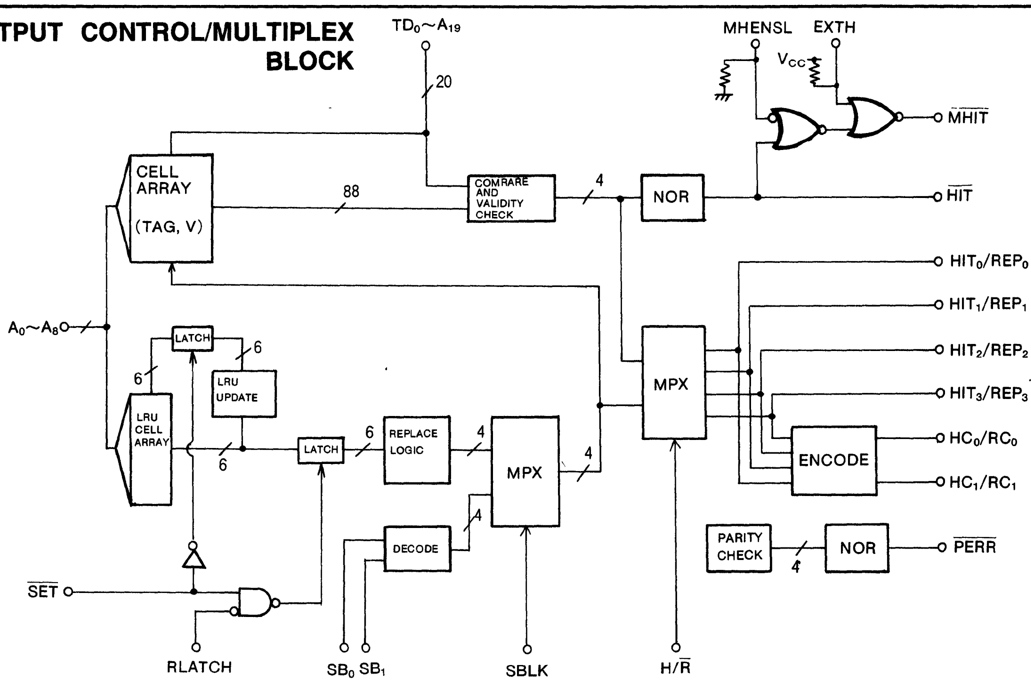


MITSUBISHI ELECTRIC

BLOCK DIAGRAM



OUTPUT CONTROL/MULTIPLEX BLOCK



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M33245GS

CMOS CACHE CONTROLLER/MEMORY (M32/CCM)

DESCRIPTION

M33245GS (M32/CCM) is a cache controller/memory for M32 family microprocessors (M33210GS-20, M33220GS-20, M33230GS-20).

It improves the MPU's average memory access time.

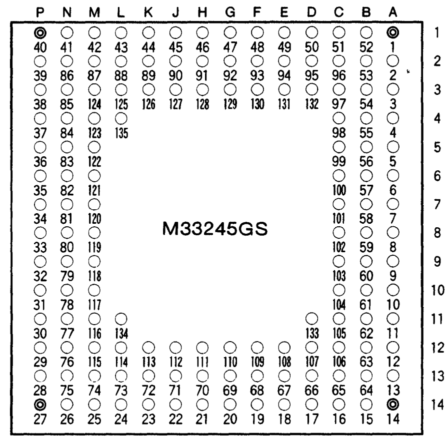
FEATURES

- 16kB real address external cache
- No wait reads possible when the cache is hit
- Fast 4 words burst read when the cache is missed
- Fully synchronous operation with M32 family processors
- Internal address comparator allows multiple usage
- Division into data cache and instruction cache
- Coherency maintained by address monitor
- Purge and freeze functions in way units
- Write-through main memory replace
- 4-way set associative cache
- LRU (Least Recently Used) replace control
- Each line consists of 4 words (16 bytes) and a validity bit
- Package : 135 pin PGA

APPLICATION

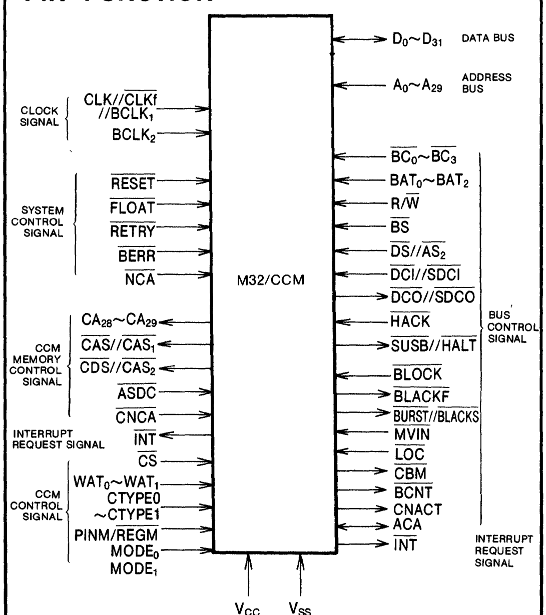
High performance cache memory system

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8

PIN FUNCTION



// : Multi function
Change by mode (MODE₀~MODE₁)

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M33281GS-20

CMOS FLOATING-POINT PROCESSING UNIT (M32/FPU)

DESCRIPTION

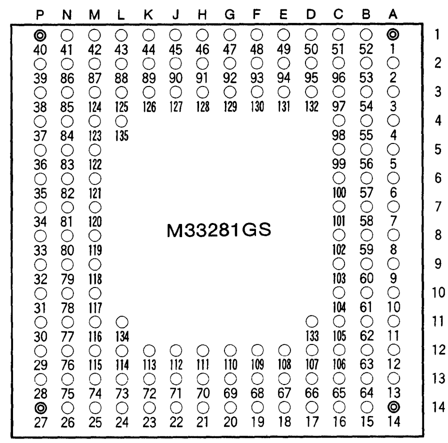
M33281GS-20 is a high-speed floating-point arithmetic LSI unit, and support the extended precision data format of IEEE standard.

The M33281GS-20 is designed to give maximum performance as a coprocessor for M32 family microprocessors (M33220GS-20, M33230GS-20). In addition to arithmetic operations and square roots, it has elementary function instructions, inner product instructions for fast matrix and vector calculations, area discrimination instructions for clipping discrimination, graphics oriented instructions and many more.

FEATURES

- Performance (20MHz operation with M33220GS-20)
  - Addition or subtraction 0.5μs
  - Multipulication 0.45μs
  - Division 1.5μs
- Elementary function calculation
- Graphics support
- Conforms to IEEE754
- Fast coprocessor interface
- Comprehensive system functions
- Softwave and system support
- Variety of instruction types
  - 31 arithmetic related
  - 21 control related
- 16 floating point operation registers (80-bit)

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8X-A

- Peripheral device mode specifiable (for use when MPU lacks coprocessor interface)
- Package 135 pin PGA

APPLICATION

Scientific and technical calculations, engineering diagram processing

PIN ASSIGN

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	V_{SS}	B10	61	$\overline{CPDC}$	D12	107	D_{16}	H3	128	D_{10}	L14	24	V_{CC}	N9	79	V_{SS}
A2	2	A_{29}	B11	62	$\overline{BERR}$	D13	66	D_{19}	H12	111	V_{CC}	M1	42	V_{SS}	N10	78	V_{CC}
A3	3	$\overline{HACK}$	B12	63	$CPST_2$	D14	17	V_{CC}	H13	70	V_{SS}	M2	87	$FCPST_1$	N11	77	V_{CC}
A4	4	$\overline{BC_2}$	B13	64	V_{SS}	E1	49	V_{CC}	H14	21	V_{CC}	M3	124	LD	N12	76	V_{CC}
A5	5	$R/\overline{W}$	B14	15	V_{CC}	E2	94	D_3	J1	45	D_9	M4	123	$CPID_1$	N13	75	V_{SS}
A6	6	BAT_0	C1	51	V_{CC}	E3	131	D_0	J2	90	D_{11}	M5	122	$\overline{IRL}$	N14	26	V_{SS}
A7	7	V_{SS}	C2	96	V_{CC}	E12	108	D_{18}	J3	127	D_{13}	M6	121	V_{SS}	P1	40	V_{CC}
A8	8	NC	C3	97	A_{28}	E13	67	D_{21}	J12	112	D_{29}	M7	120	V_{SS}	P2	39	$\overline{RESET}$
A9	9	V_{SS}	C4	98	$\overline{BC_0}$	E14	18	D_{23}	J13	71	D_{27}	M8	119	V_{CC}	P3	38	$CPID_0$
A10	10	V_{SS}	C5	99	$\overline{BC_3}$	F1	48	D_6	J14	22	D_{26}	M9	118	V_{CC}	P4	37	V_{SS}
A11	11	V_{CC}	C6	100	V_{SS}	F2	93	D_4	K1	44	V_{SS}	M10	117	V_{CC}	P5	36	SIZ16
A12	12	V_{SS}	C7	101	BAT_2	F3	130	D_2	K2	89	D_{12}	M11	116	V_{CC}	P6	35	NC
A13	13	$CPST_0$	C8	102	V_{CC}	F12	109	D_{20}	K3	126	D_{15}	M12	115	V_{CC}	P7	34	V_{CC}
A14	14	V_{CC}	C9	103	V_{CC}	F13	68	V_{CC}	K12	113	D_{30}	M13	74	V_{CC}	P8	33	CLKf
B1	52	V_{SS}	C10	104	$\overline{RETRY}$	F14	19	V_{SS}	K13	72	D_{28}	M14	25	D_{31}	P9	32	V_{SS}
B2	53	V_{CC}	C11	105	$\overline{DC}$	G1	47	V_{SS}	K14	23	V_{SS}	N1	41	$FCPST_2$	P10	31	$\overline{FCPDC}$
B3	54	A_{27}	C12	106	$CPST_1$	G2	92	D_7	L1	43	V_{CC}	N2	86	V_{SS}	P11	30	V_{CC}
B4	55	$\overline{BC_1}$	C13	65	D_{17}	G3	129	D_5	L2	88	D_{14}	N3	85	UD	P12	29	V_{CC}
B5	56	$\overline{BS}$	C14	16	V_{SS}	G12	110	D_{22}	L3	125	V_{SS}	N4	84	$CPID_2$	P13	28	NC
B6	57	V_{CC}	D1	50	V_{SS}	G13	69	D_{24}	L4	135	V_{CC}	N5	83	V_{CC}	P14	27	V_{CC}
B7	58	BAT_1	D2	95	D_1	G14	20	D_{25}	L11	134	$FCPST_0$	N6	82	V_{CC}			
B8	59	V_{SS}	D3	132	V_{SS}	H1	46	D_8	L12	114	V_{SS}	N7	81	V_{SS}			
B9	60	$\overline{CDE}$	D11	133	V_{SS}	H2	91	D_{10}	L13	73	V_{SS}	N8	80	$\overline{CLKf}$			

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