MITSUBISHI SEMICONDUCTORS 1996

MEMORIES
DRAM

DATA BOOK

MITSUBISHI ELECTRIC

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GUIDANCE 1

INDEX BY FUNCTION

■ 4M-Bit DRAM (5V Version)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
4M	4M × 1	Fast Page	60	400	M5M44100BJ-6	26P0J	2-3
					M5M44100BTP-6	26P3Z-E	
			70	350	M5M44100BJ-7	26P0J	
					M5M44100BTP-7	26P3Z-E	
		Fast Page Self-Refresh mode Low Power	60	400	M5M44100BJ-6S	26P0J	
					M5M44100BTP-6S	26P3Z-E	
			70	350	M5M44100BJ-7S	26P0J	
					M5M44100BTP-7S	26P3Z-E	
		Fast Page	50	500	M5M44100CJ-5 ★★	26P0J	2-27
					M5M44100CTP-5 ★★	26P3Z-E	
			60	400	M5M44100CJ-6 ★	26P0J	
					M5M44100CTP-6 ★	26P3Z-E	
			70	350	M5M44100CJ-7 ★	26P0J	
					M5M44100CTP-7 ★	26P3Z-E	
		Fast Page Self-Refresh mode Low Power	50	500	M5M44100CJ-5S ★★	26P0J	
					M5M44100CTP-5S ★★	26P3Z-E	
			60	400	M5M44100CJ-6S ★	26P0J	
					M5M44100CTP-6S ★	26P3Z-E	
			70	350	M5M44100CJ-7S ★	26P0J	
					M5M44100CTP-7S ★	26P3Z-E	
	1M × 4	Fast Page	60	400	M5M44400BJ-6	26P0J	2-49
					M5M44400BTP-6	26P3Z-E	
			70	350	M5M44400BJ-7	26P0J	
					M5M44400BTP-7	26P3Z-E	
		Fast Page Self-Refresh mode Low Power	60	400	M5M44400BJ-6S	26P0J	
					M5M44400BTP-6S	26P3Z-E	
			70	350	M5M44400BJ-7S	26P0J	
					M5M44400BTP-7S	26P3Z-E	
		Fast Page	50	500	M5M44400CJ-5 ★★	26P0J	2-73
					M5M44400CTP-5 ★★	26P3Z-E	
			60	400	M5M44400CJ-6 ★	26P0J	
					M5M44400CTP-6 ★	26P3Z-E	
			70	350	M5M44400CJ-7 ★	26P0J	
					M5M44400CTP-7 ★	26P3Z-E	
		Fast Page Self-Refresh mode Low Power	50	500	M5M44400CJ-5S ★★	26P0J	
					M5M44400CTP-5S ★★	26P3Z-E	
			60	400	M5M44400CJ-6S ★	26P0J	
					M5M44400CTP-6S ★	26P3Z-E	
			70	350	M5M44400CJ-7S ★	26P0J	
					M5M44400CTP-7S ★	26P3Z-E	

★ : New product ★★ : Under development

■ 4M-Bit DRAM (5V Version) (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name		Package outline	Page
4M	512K × 8	Fast Page	50	450	M5M44800CJ-5	★★	28P0K	2-96
					M5M44800CTP-5	★★	28P3Y-H	
			60	375	M5M44800CJ-6		28P0K	
					M5M44800CTP-6		28P3Y-H	
			70	325	M5M44800CJ-7		28P0K	
					M5M44800CTP-7		28P3Y-H	
		Fast Page Self-Refresh mode Low Power	50	450	M5M44800CJ-5S	★★	28P0K	
					M5M44800CTP-5S	★★	28P3Y-H	
			60	375	M5M44800CJ-6S		28P0K	
					M5M44800CTP-6S		28P3Y-H	
			70	325	M5M44800CJ-7S		28P0K	
					M5M44800CTP-7S		28P3Y-H	
	256K × 16	Fast Page	50	625	M5M44260CJ-5	★★	40P0K	2-117
					M5M44260CTP-5	★★	44P3W-L	
			60	550	M5M44260CJ-6		40P0K	
					M5M44260CTP-6		44P3W-L	
			70	475	M5M44260CJ-7		40P0K	
					M5M44260CTP-7		44P3W-L	
		Fast Page Self-Refresh mode Low Power	50	625	M5M44260CJ-5S	★★	40P0K	
					M5M44260CTP-5S	★★	44P3W-L	
			60	550	M5M44260CJ-6S		40P0K	
					M5M44260CTP-6S		44P3W-L	
			70	475	M5M44260CJ-7S		40P0K	
					M5M44260CTP-7S		44P3W-L	
		EDO (Hyper Page)	50	625	M5M44265CJ-5	★★	40P0K	2-146
					M5M44265CTP-5	★★	44P3W-L	
			60	550	M5M44265CJ-6		40P0K	
					M5M44265CTP-6		44P3W-L	
			70	475	M5M44265CJ-7		40P0K	
					M5M44265CTP-7		44P3W-L	
		EDO (Hyper Page) Self-Refresh mode Low Power	50	625	M5M44265CJ-5S	★★	40P0K	
					M5M44265CTP-5S	★★	44P3W-L	
			60	550	M5M44265CJ-6S		40P0K	
					M5M44265CTP-6S		44P3W-L	
			70	475	M5M44265CJ-7S		40P0K	
					M5M44265CTP-7S		44P3W-L	

★★ : Under development

■ 4M-Bit DRAM (3.3V Version)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
4M	1M × 4	Fast Page Low Voltage (Vcc = 3.3 ± 0.3V)	60	180	M5M4V4400TP-6	26P3Z-E	3-3
			70	160	M5M4V4400TP-7	26P3Z-E	
			80	130	M5M4V4400TP-8	26P3Z-E	
		Fast Page Self-Refresh mode Low Power Low Voltage (Vcc = 3.3 ± 0.3V)	60	180	M5M4V4400TP-6S	26P3Z-E	
			70	160	M5M4V4400TP-7S	26P3Z-E	
			80	130	M5M4V4400TP-8S	26P3Z-E	
	512K × 8	Fast Page Low Voltage (Vcc = 3.3 ± 0.3V)	70	190	M5M4V4800TP-7	28P3Y-H	3-25
			80	160	M5M4V4800TP-8	28P3Y-H	
		Fast Page Self-Refresh mode Low Power Low Voltage (Vcc = 3.3 ± 0.3V)	70	190	M5M4V4800TP-7S	28P3Y-H	
			80	160	M5M4V4800TP-8S	28P3Y-H	
		Fast Page Low Voltage (Vcc = 3.3 ± 0.3V)	60	230	M5M4V4800CTP-6 ★★	28P3Y-H	3-47
			70	200	M5M4V4800CTP-7 ★★	28P3Y-H	
		Fast Page Self-Refresh mode Low Power Low Voltage (Vcc = 3.3 ± 0.3V)	60	230	M5M4V4800CTP-6S ★★	28P3Y-H	
			70	200	M5M4V4800CTP-7S ★★	28P3Y-H	
	256K × 16	Fast Page 2CAS,1W 512 Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	70	300	M5M4V4260TP-7	44P3W-L	3-68
			80	260	M5M4V4260TP-8	44P3W-L	
		Fast Page 2CAS,1W Self-Refresh mode Low Power 512 Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	70	300	M5M4V4260TP-7S	44P3W-L	
			80	260	M5M4V4260TP-8S	44P3W-L	
		Fast Page Low Voltage (Vcc = 3.3 ± 0.3V)	60	333	M5M4V4260CTP-6 ★★	44P3W-L	3-98
			70	290	M5M4V4260CTP-7 ★★	44P3W-L	
		Fast Page Self-Refresh mode Low Power Low Voltage (Vcc = 3.3 ± 0.3V)	60	333	M5M4V4260CTP-6S ★★	44P3W-L	
			70	290	M5M4V4260CTP-7S ★★	44P3W-L	
		EDO (Hyper Page) Low Voltage (Vcc = 3.3 ± 0.3V)	60	333	M5M4V4265CTP-6 ★★	44P3W-L	3-127
			70	290	M5M4V4265CTP-7 ★★	44P3W-L	
		EDO (Hyper Page) Self-Refresh mode Low Power Low Voltage (Vcc = 3.3 ± 0.3V)	60	333	M5M4V4265CTP-6S ★★	44P3W-L	
			70	290	M5M4V4265CTP-7S ★★	44P3W-L	

★★ : Under development

■ 16M-Bit DRAM (5V Version)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
16M	16M × 1	Fast Page 4K Refresh Cycle	50	495	M5M416100BJ-5 ★★	26P0D-B	4-3
					M5M416100BTP-5 ★★	26P3D-E	
			60	405	M5M416100BJ-6	26P0D-B	
					M5M416100BTP-6	26P3D-E	
			70	340	M5M416100BJ-7	26P0D-B	
					M5M416100BTP-7	26P3D-E	
	4M × 4	Fast Page 4K Refresh Cycle	50	495	M5M416400BJ-5 ★★	26P0D-B	4-22
					M5M416400BTP-5 ★★	26P3D-E	
			60	405	M5M416400BJ-6	26P0D-B	
					M5M416400BTP-6	26P3D-E	
			70	340	M5M416400BJ-7	26P0D-B	
					M5M416400BTP-7	26P3D-E	
		Fast Page 4K Refresh Cycle Self-Refresh mode	50	495	M5M416400BJ-5S ★★	26P0D-B	
					M5M416400BTP-5S ★★	26P3D-E	
			60	405	M5M416400BJ-6S	26P0D-B	
					M5M416400BTP-6S	26P3D-E	
			70	340	M5M416400BJ-7S	26P0D-B	
					M5M416400BTP-7S	26P3D-E	
		Fast Page 4K Refresh Cycle	50	495	M5M416400CJ-5 ★★	26P0D-B	4-42
					M5M416400CTP-5 ★★	26P3D-E	
			60	405	M5M416400CJ-6 ★★	26P0D-B	
					M5M416400CTP-6 ★★	26P3D-E	
			70	340	M5M416400CJ-7 ★★	26P0D-B	
					M5M416400CTP-7 ★★	26P3D-E	
		Fast Page 4K Refresh Cycle Self-Refresh mode	50	495	M5M416400CJ-5S ★★	26P0D-B	
					M5M416400CTP-5S ★★	26P3D-E	
			60	405	M5M416400CJ-6S ★★	26P0D-B	
					M5M416400CTP-6S ★★	26P3D-E	
			70	340	M5M416400CJ-7S ★★	26P0D-B	
					M5M416400CTP-7S ★★	26P3D-E	
		Hyper Page 4K Refresh Cycle	50	495	M5M416405CJ-5 ★★	26P0D-B	4-63
					M5M416405CTP-5 ★★	26P3D-E	
			60	405	M5M416405CJ-6 ★★	26P0D-B	
					M5M416405CTP-6 ★★	26P3D-E	
			70	340	M5M416405CJ-7 ★★	26P0D-B	
					M5M416405CTP-7 ★★	26P3D-E	
		Hyper Page 4K Refresh Cycle Self-Refresh mode	50	495	M5M416405CJ-5S ★★	26P0D-B	
					M5M416405CTP-5S ★★	26P3D-E	
			60	405	M5M416405CJ-6S ★★	26P0D-B	
					M5M416405CTP-6S ★★	26P3D-E	
			70	340	M5M416405CJ-7S ★★	26P0D-B	
					M5M416405CTP-7S ★★	26P3D-E	

★★ : Under development

■ 16M-Bit DRAM (5V Version) (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
16M	4M × 4	Fast Page 2K Refresh Cycle	50	655	M5M417400BJ-5 ★	26P0D-B	4-87
					M5M417400BTP-5 ★	26P3D-E	
			60	540	M5M417400BJ-6	26P0D-B	
					M5M417400BTP-6	26P3D-E	
			70	475	M5M417400BJ-7	26P0D-B	
					M5M417400BTP-7	26P3D-E	
		Fast Page 2K Refresh Cycle Self-Refresh mode	50	655	M5M417400BJ-5S ★	26P0D-B	
					M5M417400BTP-5S ★	26P3D-E	
			60	540	M5M417400BJ-6S	26P0D-B	
					M5M417400BTP-6S	26P3D-E	
			70	475	M5M417400BJ-7S	26P0D-B	
					M5M417400BTP-7S	26P3D-E	
		Fast Page 2K Refresh Cycle	50	655	M5M417400CJ-5 ★★	26P0D-B	4-107
					M5M417400CTP-5 ★★	26P3D-E	
			60	540	M5M417400CJ-6	26P0D-B	
					M5M417400CTP-6	26P3D-E	
			70	475	M5M417400CJ-7	26P0D-B	
					M5M417400CTP-7	26P3D-E	
		Fast Page 2K Refresh Cycle Self-Refresh mode	50	655	M5M417400CJ-5S ★★	26P0D-B	
					M5M417400CTP-5S ★★	26P3D-E	
			60	540	M5M417400CJ-6S	26P0D-B	
					M5M417400CTP-6S	26P3D-E	
			70	475	M5M417400CJ-7S	26P0D-B	
					M5M417400CTP-7S	26P3D-E	
		Hyper Page 2K Refresh Cycle	50	655	M5M417405CJ-5 ★★	26P0D-B	4-128
					M5M417405CTP-5 ★★	26P3D-E	
			60	540	M5M417405CJ-6 ★★	26P0D-B	
					M5M417405CTP-6 ★★	26P3D-E	
			70	475	M5M417405CJ-7 ★★	26P0D-B	
					M5M417405CTP-7 ★★	26P3D-E	
		Hyper Page 2K Refresh Cycle Self-Refresh mode	50	655	M5M417405CJ-5S ★★	26P0D-B	
					M5M417405CTP-5S ★★	26P3D-E	
			60	540	M5M417405CJ-6S ★★	26P0D-B	
					M5M417405CTP-6S ★★	26P3D-E	
			70	475	M5M417405CJ-7S ★★	26P0D-B	
					M5M417405CTP-7S ★★	26P3D-E	
	2M × 8	Fast Page 2K Refresh Cycle	60	540	M5M417800AJ-6	28P0K	4-152
					M5M417800ATP-6	28P3Y-H	
			70	475	M5M417800AJ-7	28P0K	
					M5M417800ATP-7	28P3Y-H	
		Fast Page 2K Refresh Cycle Self-Refresh mode	60	540	M5M417800AJ-6S	28P0K	
					M5M417800ATP-6S	28P3Y-H	
			70	475	M5M417800AJ-7S	28P0K	
					M5M417800ATP-7S	28P3Y-H	

★ : New product ★★ : Under development

■ 16M-Bit DRAM (5V Version) (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name		Package outline	Page
16M	2M × 8	Fast Page 2K Refresh Cycle	50	655	M5M417800CJ-5	★★	28P0N-A	4-173
					M5M417800CTP-5	★★	28P3N-C	
			60	540	M5M417800CJ-6	★★	28P0N-A	
					M5M417800CTP-6	★★	28P3N-C	
			70	475	M5M417800CJ-7	★★	28P0N-A	
					M5M417800CTP-7	★★	28P3N-C	
		Fast Page 2K Refresh Cycle Self-Refresh mode	50	655	M5M417800CJ-5S	★★	28P0N-A	
					M5M417800CTP-5S	★★	28P3N-C	
			60	540	M5M417800CJ-6S	★★	28P0N-A	
					M5M417800CTP-6S	★★	28P3N-C	
			70	475	M5M417800CJ-7S	★★	28P0N-A	
					M5M417800CTP-7S	★★	28P3N-C	
		Hyper Page 2K Refresh Cycle	50	655	M5M417805CJ-5	★★	28P0N-A	4-194
					M5M417805CTP-5	★★	28P3N-C	
			60	540	M5M417805CJ-6	★★	28P0N-A	
					M5M417805CTP-6	★★	28P3N-C	
			70	475	M5M417805CJ-7	★★	28P0N-A	
					M5M417805CTP-7	★★	28P3N-C	
		Hyper Page 2K Refresh Cycle Self-Refresh mode	50	655	M5M417805CJ-5S	★★	28P0N-A	
					M5M417805CTP-5S	★★	28P3N-C	
			60	540	M5M417805CJ-6S	★★	28P0N-A	
					M5M417805CTP-6S	★★	28P3N-C	
			70	475	M5M417805CJ-7S	★★	28P0N-A	
					M5M417805CTP-7S	★★	28P3N-C	
	1M × 16	Fast Page 4K Refresh Cycle	60	430	M5M416160BJ-6		42P0K	4-218
					M5M416160BTP-6		50P3W-L	
			70	385	M5M416160BJ-7		42P0K	
					M5M416160BTP-7		50P3W-L	
		Fast Page 4K Refresh Cycle Self-Refresh mode	60	430	M5M416160BJ-6S		42P0K	
					M5M416160BTP-6S		50P3W-L	
			70	385	M5M416160BJ-7S		42P0K	
					M5M416160BTP-7S		50P3W-L	
		Fast Page 1K Refresh Cycle	60	680	M5M418160BJ-6		42P0K	4-248
					M5M418160BTP-6		50P3W-L	
			70	590	M5M418160BJ-7		42P0K	
					M5M418160BTP-7		50P3W-L	
		Fast Page 1K Refresh Cycle Self-Refresh mode	60	680	M5M418160BJ-6S		42P0K	
					M5M418160BTP-6S		50P3W-L	
			70	590	M5M418160BJ-7S		42P0K	
					M5M418160BTP-7S		50P3W-L	
		Hyper Page 1K Refresh Cycle	60	680	M5M418165BJ-6		42P0K	4-278
					M5M418165BTP-6		50P3W-L	
			70	590	M5M418165BJ-7		42P0K	
					M5M418165BTP-7		50P3W-L	
		Hyper Page 1K Refresh Cycle Self-Refresh mode	60	680	M5M418165BJ-6S		42P0K	
					M5M418165BTP-6S		50P3W-L	
			70	590	M5M418165BJ-7S		42P0K	
					M5M418165BTP-7S		50P3W-L	

★★ : Under development

■ 16M-Bit DRAM 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name		Package outline	Page
16M	1M × 16	Fast Page 4K Refresh Cycle	50	540	M5M416160CJ-5	★★	42P0N-A	4-308
					M5M416160CTP-5	★★	50P3G-F	
			60	430	M5M416160CJ-6	★★	42P0N-A	
					M5M416160CTP-6	★★	50P3G-F	
			70	385	M5M416160CJ-7	★★	42P0N-A	
					M5M416160CTP-7	★★	50P3G-F	
		Fast Page 4K Refresh Cycle Self-Refresh mode	50	540	M5M416160CJ-5S	★★	42P0N-A	
					M5M416160CTP-5S	★★	50P3G-F	
			60	430	M5M416160CJ-6S	★★	42P0N-A	
					M5M416160CTP-6S	★★	50P3G-F	
			70	385	M5M416160CJ-7S	★★	42P0N-A	
					M5M416160CTP-7S	★★	50P3G-F	
		Fast Page 1K Refresh Cycle	50	810	M5M418160CJ-5	★★	42P0N-A	4-338
					M5M418160CTP-5	★★	50P3G-F	
			60	675	M5M418160CJ-6	★★	42P0N-A	
					M5M418160CTP-6	★★	50P3G-F	
			70	585	M5M418160CJ-7	★★	42P0N-A	
					M5M418160CTP-7	★★	50P3G-F	
		Fast Page 1K Refresh Cycle Self-Refresh mode	50	810	M5M418160CJ-5S	★★	42P0N-A	
					M5M418160CTP-5S	★★	50P3G-F	
			60	675	M5M418160CJ-6S	★★	42P0N-A	
					M5M418160CTP-6S	★★	50P3G-F	
			70	585	M5M418160CJ-7S	★★	42P0N-A	
					M5M418160CTP-7S	★★	50P3G-F	
		Hyper Page 4K Refresh Cycle	50	540	M5M416165CJ-5	★★	42P0N-A	4-368
					M5M416165CTP-5	★★	50P3G-F	
			60	430	M5M416165CJ-6	★★	42P0N-A	
					M5M416165CTP-6	★★	50P3G-F	
			70	385	M5M416165CJ-7	★★	42P0N-A	
					M5M416165CTP-7	★★	50P3G-F	
		Hyper Page 4K Refresh Cycle Self-Refresh mode	50	540	M5M416165CJ-5S	★★	42P0N-A	
					M5M416165CTP-5S	★★	50P3G-F	
			60	430	M5M416165CJ-6S	★★	42P0N-A	
					M5M416165CTP-6S	★★	50P3G-F	
			70	385	M5M416165CJ-7S	★★	42P0N-A	
					M5M416165CTP-7S	★★	50P3G-F	
		Hyper Page 1K Refresh Cycle	50	810	M5M418165CJ-5	★★	42P0N-A	4-399
					M5M418165CTP-5	★★	50P3G-F	
			60	675	M5M418165CJ-6	★★	42P0N-A	
					M5M418165CTP-6	★★	50P3G-F	
			70	585	M5M418165CJ-7	★★	42P0N-A	
					M5M418165CTP-7	★★	50P3G-F	
		Hyper Page 1K Refresh Cycle Self-Refresh mode	50	810	M5M418165CJ-5S	★★	42P0N-A	
					M5M418165CTP-5S	★★	50P3G-F	
			60	675	M5M418165CJ-6S	★★	42P0N-A	
					M5M418165CTP-6S	★★	50P3G-F	
			70	585	M5M418165CJ-7S	★★	42P0N-A	
					M5M418165CTP-7S	★★	50P3G-F	

★★ : Under development

■ 16M-Bit DRAM (3.3V Version)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
16M	4M × 4	Fast Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	60	270	M5M4V16400BJ-6	26P0D-B	5-3
					M5M4V16400BTP-6	26P3D-E	
			70	225	M5M4V16400BJ-7	26P0D-B	
					M5M4V16400BTP-7	26P3D-E	
		Fast Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	60	270	M5M4V16400BJ-6S	26P0D-B	
					M5M4V16400BTP-6S	26P3D-E	
			70	225	M5M4V16400BJ-7S	26P0D-B	
					M5M4V16400BTP-7S	26P3D-E	
		Fast Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	330	M5M4V16400CJ-5 ★★	26P0D-B	5-23
					M5M4V16400CTP-5 ★★	26P3D-E	
			60	270	M5M4V16400CJ-6 ★★	26P0D-B	
					M5M4V16400CTP-6 ★★	26P3D-E	
			70	225	M5M4V16400CJ-7 ★★	26P0D-B	
					M5M4V16400CTP-7 ★★	26P3D-E	
		Fast Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	330	M5M4V16400CJ-5S ★★	26P0D-B	
					M5M4V16400CTP-5S ★★	26P3D-E	
			60	270	M5M4V16400CJ-6S ★★	26P0D-B	
					M5M4V16400CTP-6S ★★	26P3D-E	
			70	225	M5M4V16400CJ-7S ★★	26P0D-B	
					M5M4V16400CTP-7S ★★	26P3D-E	
		Hyper Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	330	M5M4V16405CJ-5 ★★	26P0D-B	5-44
					M5M4V16405CTP-5 ★★	26P3D-E	
			60	270	M5M4V16405CJ-6 ★★	26P0D-B	
					M5M4V16405CTP-6 ★★	26P3D-E	
			70	225	M5M4V16405CJ-7 ★★	26P0D-B	
					M5M4V16405CTP-7 ★★	26P3D-E	
		Hyper Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	330	M5M4V16405CJ-5S ★★	26P0D-B	
					M5M4V16405CTP-5S ★★	26P3D-E	
			60	270	M5M4V16405CJ-6S ★★	26P0D-B	
					M5M4V16405CTP-6S ★★	26P3D-E	
			70	225	M5M4V16405CJ-7S ★★	26P0D-B	
					M5M4V16405CTP-7S ★★	26P3D-E	
		Fast Page 2K Refresh Cycle (Vcc = 3.3 ± 0.3V)	60	360	M5M4V17400BJ-6	26P0D-B	5-68
					M5M4V17400BTP-6	26P3D-E	
			70	315	M5M4V17400BJ-7	26P0D-B	
					M5M4V17400BTP-7	26P3D-E	
		Fast Page 2K Refresh Cycle Self-Refresh mode (Vcc = 3.3 ± 0.3V)	60	360	M5M4V17400BJ-6S	26P0D-B	
					M5M4V17400BTP-6S	26P3D-E	
			70	315	M5M4V17400BJ-7S	26P0D-B	
					M5M4V17400BTP-7S	26P3D-E	
		Fast Page 2K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17400CJ-5 ★★	26P0D-B	5-88
					M5M4V17400CTP-5 ★★	26P3D-E	
			60	360	M5M4V17400CJ-6 ★★	26P0D-B	
					M5M4V17400CTP-6 ★★	26P3D-E	
			70	315	M5M4V17400CJ-7 ★★	26P0D-B	
					M5M4V17400CTP-7 ★★	26P3D-E	
		Fast Page 2K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17400CJ-5S ★★	26P0D-B	
					M5M4V17400CTP-5S ★★	26P3D-E	
			60	360	M5M4V17400CJ-6S ★★	26P0D-B	
					M5M4V17400CTP-6S ★★	26P3D-E	
			70	315	M5M4V17400CJ-7S ★★	26P0D-B	
					M5M4V17400CTP-7S ★★	26P3D-E	

★★ : Under development

■ 16M-Bit DRAM 〔3.3V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
16M	4M × 4	Hyper Page 2K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17405CJ-5 ★★	26P0D-B	5-109
					M5M4V17405CTP-5 ★★	26P3D-E	
			60	360	M5M4V17405CJ-6 ★★	26P0D-B	
					M5M4V17405CTP-6 ★★	26P3D-E	
			70	315	M5M4V17405CJ-7 ★★	26P0D-B	
					M5M4V17405CTP-7 ★★	26P3D-E	
		Hyper Page 2K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17405CJ-5S ★★	26P0D-B	
					M5M4V17405CTP-5S ★★	26P3D-E	
			60	360	M5M4V17405CJ-6S ★★	26P0D-B	
					M5M4V17405CTP-6S ★★	26P3D-E	
			70	315	M5M4V17405CJ-7S ★★	26P0D-B	
					M5M4V17405CTP-7S ★★	26P3D-E	
	2M × 8	Fast Page 2K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	60	360	M5M4V17800AJ-6	28P0K	5-133
					M5M4V17800ATP-6	28P3Y-H	
			70	315	M5M4V17800AJ-7	28P0K	
					M5M4V17800ATP-7	28P3Y-H	
		Fast Page 2K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	60	360	M5M4V17800AJ-6S	28P0K	
					M5M4V17800ATP-6S	28P3Y-H	
			70	315	M5M4V17800AJ-7S	28P0K	
					M5M4V17800ATP-7S	28P3Y-H	
		Fast Page 2K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17800CJ-5 ★★	28P0N-A	5-154
					M5M4V17800CTP-5 ★★	28P3N-C	
			60	360	M5M4V17800CJ-6 ★★	28P0N-A	
					M5M4V17800CTP-6 ★★	28P3N-C	
			70	315	M5M4V17800CJ-7 ★★	28P0N-A	
					M5M4V17800CTP-7 ★★	28P3N-C	
		Fast Page 2K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17800CJ-5S ★★	28P0N-A	
					M5M4V17800CTP-5S ★★	28P3N-C	
			60	360	M5M4V17800CJ-6S ★★	28P0N-A	
					M5M4V17800CTP-6S ★★	28P3N-C	
			70	315	M5M4V17800CJ-7S ★★	28P0N-A	
					M5M4V17800CTP-7S ★★	28P3N-C	
		Hyper Page 2K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17805CJ-5 ★★	28P0N-A	5-175
					M5M4V17805CTP-5 ★★	28P3N-C	
			60	360	M5M4V17805CJ-6 ★★	28P0N-A	
					M5M4V17805CTP-6 ★★	28P3N-C	
			70	315	M5M4V17805CJ-7 ★★	28P0N-A	
					M5M4V17805CTP-7 ★★	28P3N-C	
		Hyper Page 2K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	435	M5M4V17805CJ-5S ★★	28P0N-A	
					M5M4V17805CTP-5S ★★	28P3N-C	
			60	360	M5M4V17805CJ-6S ★★	28P0N-A	
					M5M4V17805CTP-6S ★★	28P3N-C	
			70	315	M5M4V17805CJ-7S ★★	28P0N-A	
					M5M4V17805CTP-7S ★★	28P3N-C	
	1M × 16	Fast Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	60	285	M5M4V16160BTP-6	50P3W-L	5-199
			70	255	M5M4V16160BTP-7	50P3W-L	
		Fast Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	60	285	M5M4V16160BTP-6S	50P3W-L	
			70	255	M5M4V16160BTP-7S	50P3W-L	

★★ : Under development

■ 16M-Bit DRAM (3.3V Version) (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name	Package outline	Page
16M	1M × 16	Fast Page 1K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	60	450	M5M4V18160BTP-6	50P3W-L	5-229
			70	390	M5M4V18160BTP-7	50P3W-L	
		Fast Page 1K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	60	450	M5M4V18160BTP-6S	50P3W-L	
			70	390	M5M4V18160BTP-7S	50P3W-L	
		Hyper Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	60	285	M5M4V16165BTP-6	50P3W-L	5-259
			70	255	M5M4V16165BTP-7	50P3W-L	
		Hyper Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	60	285	M5M4V16165BTP-6S	50P3W-L	
			70	255	M5M4V16165BTP-7S	50P3W-L	
		Hyper Page 1K Refresh Cycle (Vcc = 3.3 ± 0.3V)	60	450	M5M4V18165BTP-6	50P3W-L	5-289
			70	390	M5M4V18165BTP-7	50P3W-L	
		Hyper Page 1K Refresh Cycle Self-Refresh mode (Vcc = 3.3 ± 0.3V)	60	450	M5M4V18165BTP-6S	50P3W-L	
			70	390	M5M4V18165BTP-7S	50P3W-L	
		Fast Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	360	M5M4V16160CTP-5 ★★	50P3G-F	5-319
			60	285	M5M4V16160CTP-6 ★★	50P3G-F	
			70	255	M5M4V16160CTP-7 ★★	50P3G-F	
		Fast Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	360	M5M4V16160CTP-5S ★★	50P3G-F	
			60	285	M5M4V16160CTP-6S ★★	50P3G-F	
			70	255	M5M4V16160CTP-7S ★★	50P3G-F	
		Fast Page 1K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	540	M5M4V18160CTP-5 ★★	50P3G-F	5-349
			60	450	M5M4V18160CTP-6 ★★	50P3G-F	
			70	390	M5M4V18160CTP-7 ★★	50P3G-F	
		Fast Page 1K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	540	M5M4V18160CTP-5S ★★	50P3G-F	
			60	450	M5M4V18160CTP-6S ★★	50P3G-F	
			70	390	M5M4V18160CTP-7S ★★	50P3G-F	
		Hyper Page 4K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	360	M5M4V16165CTP-5 ★★	50P3G-F	5-379
			60	285	M5M4V16165CTP-6 ★★	50P3G-F	
			70	255	M5M4V16165CTP-7 ★★	50P3G-F	
		Hyper Page 4K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	360	M5M4V16165CTP-5S ★★	50P3G-F	
			60	285	M5M4V16165CTP-6S ★★	50P3G-F	
			70	255	M5M4V16165CTP-7S ★★	50P3G-F	

★★ : Under development

■ 16M-Bit DRAM (3.3V Version) (Cont.)

Memory capacity	Configuration (Word × Bit)	Function mode	Access time Max (ns)	Power dissipation Typ (mW)	Type name		Package outline	Page
16M	1M × 16	Hyper Page 1K Refresh Cycle Low Voltage (Vcc = 3.3 ± 0.3V)	50	540	M5M4V18165CTP-5	★★	50P3G-F	5-410
			60	450	M5M4V18165CTP-6	★★	50P3G-F	
			70	390	M5M4V18165CTP-7	★★	50P3G-F	
		Hyper Page 1K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.3 ± 0.3V)	50	540	M5M4V18165CTP-5S	★★	50P3G-F	
			60	450	M5M4V18165CTP-6S	★★	50P3G-F	
			70	390	M5M4V18165CTP-7S	★★	50P3G-F	
		Pipeline Burst 1K Refresh Cycle Low Voltage (Vcc = 3.15~3.6V)	50	540	M5M4V18167CTP-5	★★	50P3G-F	5-441
			60	450	M5M4V18167CTP-6	★★	50P3G-F	
			70	390	M5M4V18167CTP-7	★★	50P3G-F	
		Pipeline Burst 1K Refresh Cycle Self-Refresh mode Low Voltage (Vcc = 3.15~3.6V)	50	540	M5M4V18167CTP-5S	★★	50P3G-F	
			60	450	M5M4V18167CTP-6S	★★	50P3G-F	
			70	390	M5M4V18167CTP-7S	★★	50P3G-F	

★★ : Under development

■ 16M-Bit SYNCHRONOUS DRAM (3.3V Version)

Memory capacity	Configuration (Word × Bit)	Access time Max (ns)	Power dissipation Typ (mW)	Type name		Package outline	Page
16M	2M × 8	5	515	M5M4S16S31CTP-7	★★	44P3L-B	6-3
		6	455	M5M4S16S31CTP-8	★★		
		8	380	M5M4S16S31CTP-10	★★		
	4M × 4	5	515	M5M4S16S21CTP-7	★★	44P3L-B	6-44
		6	455	M5M4S16S21CTP-8	★★		
		8	380	M5M4S16S21CTP-10	★★		

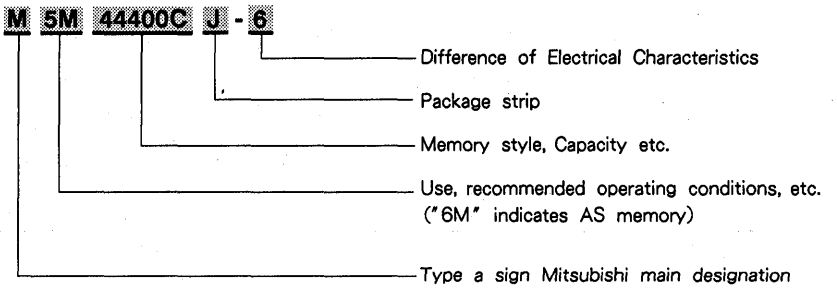
★★ : Under development

ORDERING INFORMATION

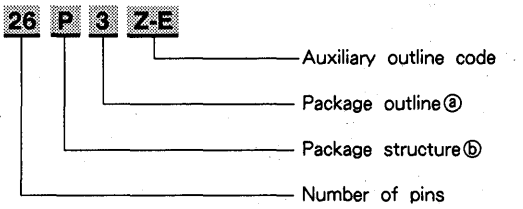
Understanding the Type-Designation Code

Type-designation examples are provided below to provide information about the products and their packages. These type designations are comprised of code elements. The blanks in some of the examples indicate that a code element is not necessary. When writing the type designation, the blank spaces are closed.

Example 1.



Example 2.(Package)

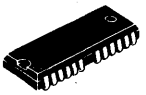


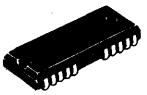
ⓐ **1** : DIP (Except for Plastic)
2 : SOP
3 : TSOP
4 : DIP (Plastic)
5 : SIP, ZIP
6 : QFP
8 : PGA
9 : Specialize, SIP
0 : Leadless, PLCC, SOJ

ⓑ **K** : Glass-sealed ceramic
N : PCB Module (Glass epoxy)
P : Molded plastic

PACKAGE OUTWARD

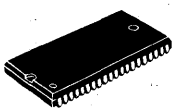
SOJ

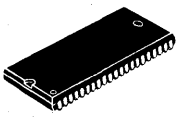

26P0D-B

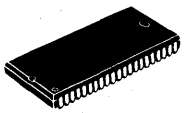

26P0J


28P0K

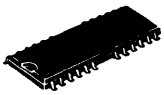

28P0N-A

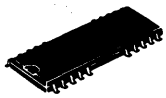

40P0K

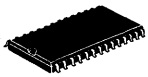

42P0K

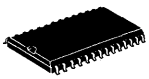

42P0N-A

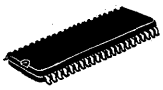
TSOP

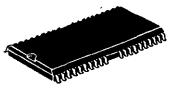

26P3D-E

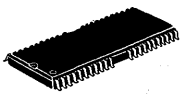

26P3Z-E

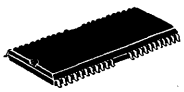

28P3N-C


28P3Y-H


44P3L-B


44P3W-L


50P3G-F


50P3W-L

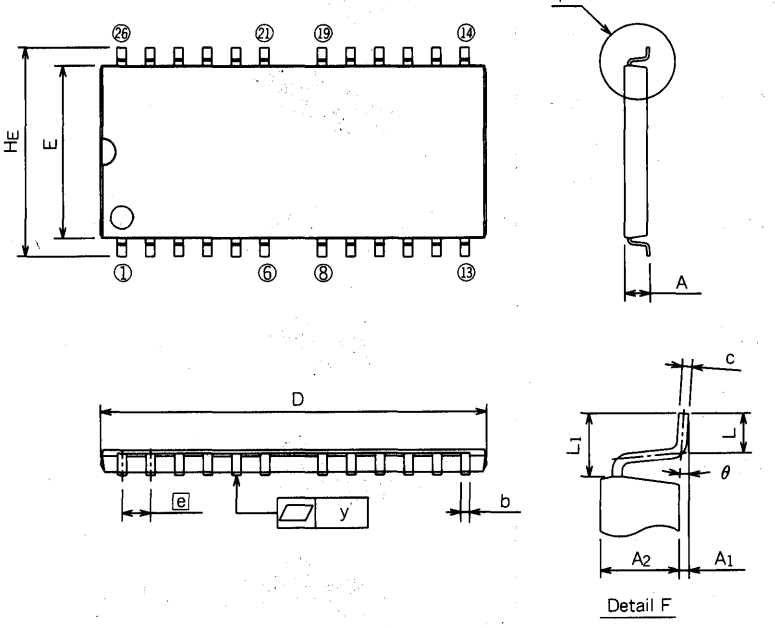
PACKAGE OUTLINES

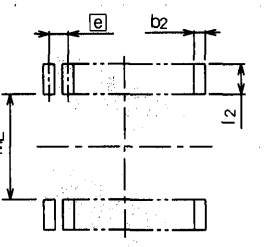
26P3D-E

Plastic 26pin 300mil TSOP(II)(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 26/24-P-300-1.27	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

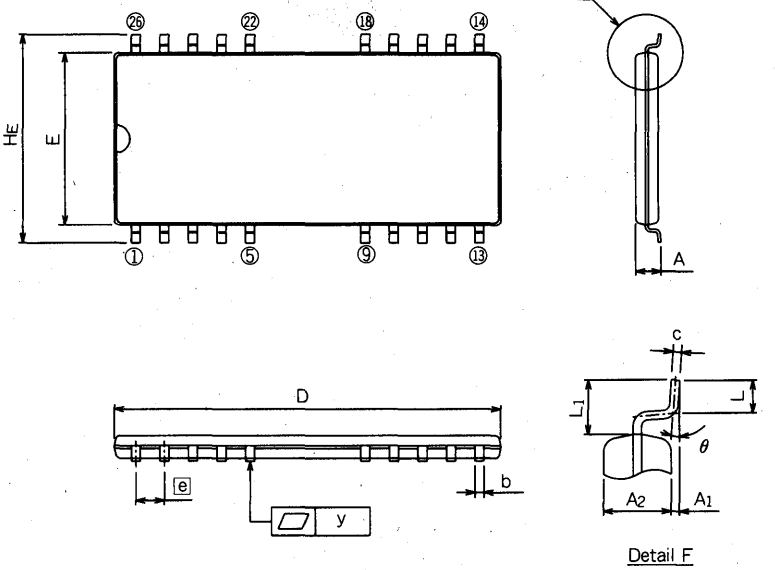
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	17.04	17.14	17.24
E	7.52	7.62	7.72
e	—	1.27	—
H_E	9.02	9.22	9.42
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	7.82	—
l_2	0.9	—	—
b_2	—	0.76	—

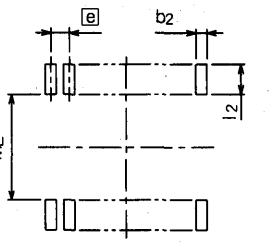
26P3Z-E

Plastic 26pin 300mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 26/20-P-300-1.27	—	0.32	Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	17.04	17.14	17.24
E	7.52	7.62	7.72
e	—	1.27	—
H_E	9.02	9.22	9.42
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	7.82	—
l_2	0.9	—	—
b_2	—	0.76	—

MITSUBISHI ELECTRIC

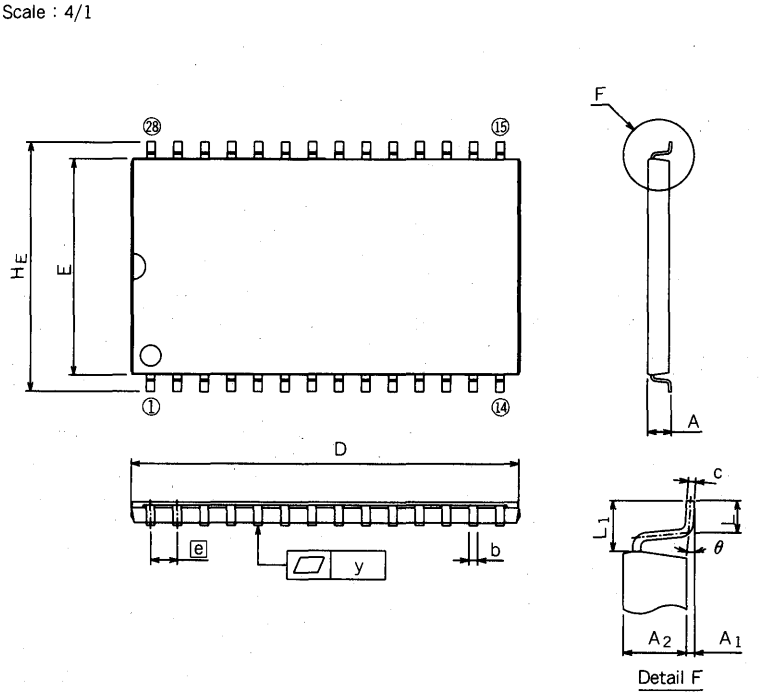
PACKAGE OUTLINES

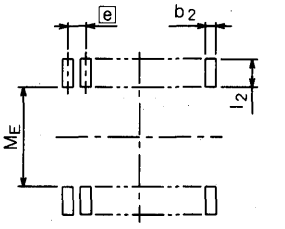
28P3N-C

Plastic 28pin 400mil TSOP(II)(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 28-P-400-1.27	—		Alloy 42

Scale : 4/1





Recommended Mount Pad

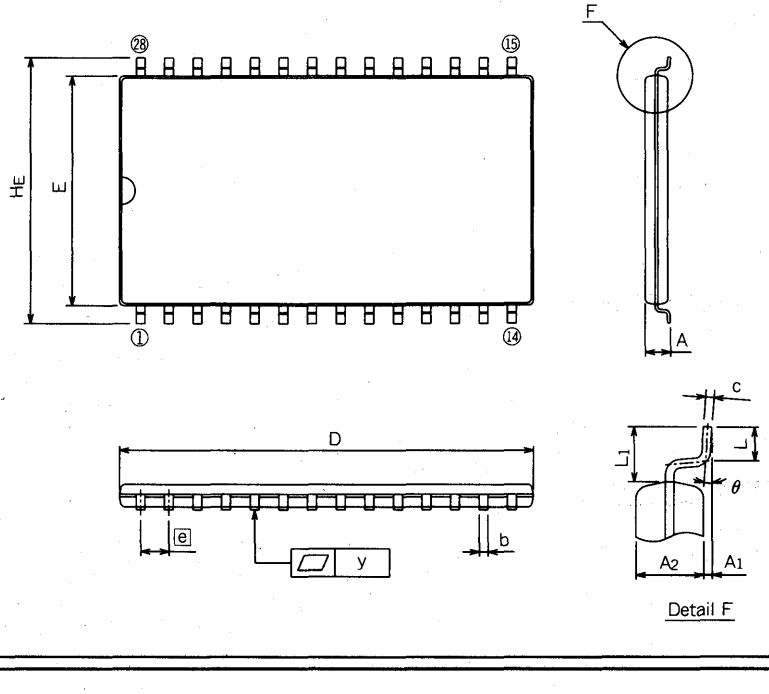
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	1.27	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.76	—

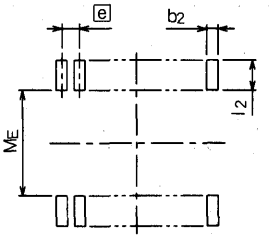
28P3Y-H

Plastic 28pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 28-P-400-1.27	—	0.45	Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	1.27	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.76	—

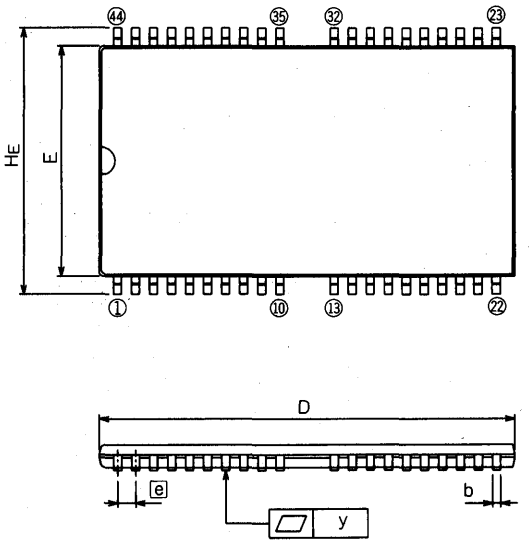
PACKAGE OUTLINES

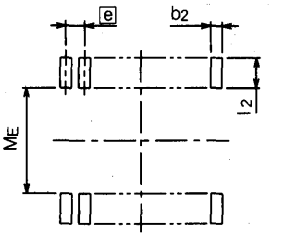
44P3W-L

Plastic 44pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 44/40-P-400-0.80	—	0.47	Alloy 42

Scale : 3/1





Recommended Mount Pad

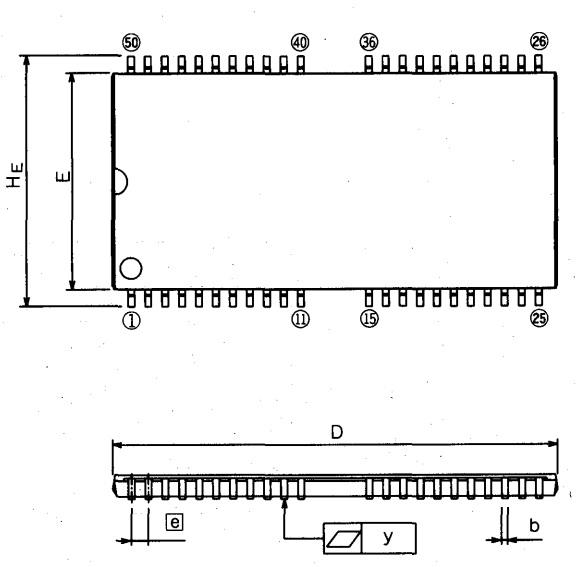
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	0.8	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.5	—

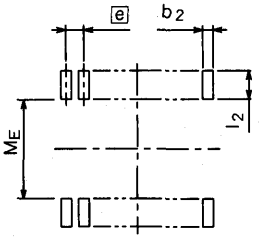
50P3G-F

Plastic 50pin 400mil TSOP(II)(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 50/44-P-400-0.80	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	—	0.8	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.5	—

MITSUBISHI ELECTRIC

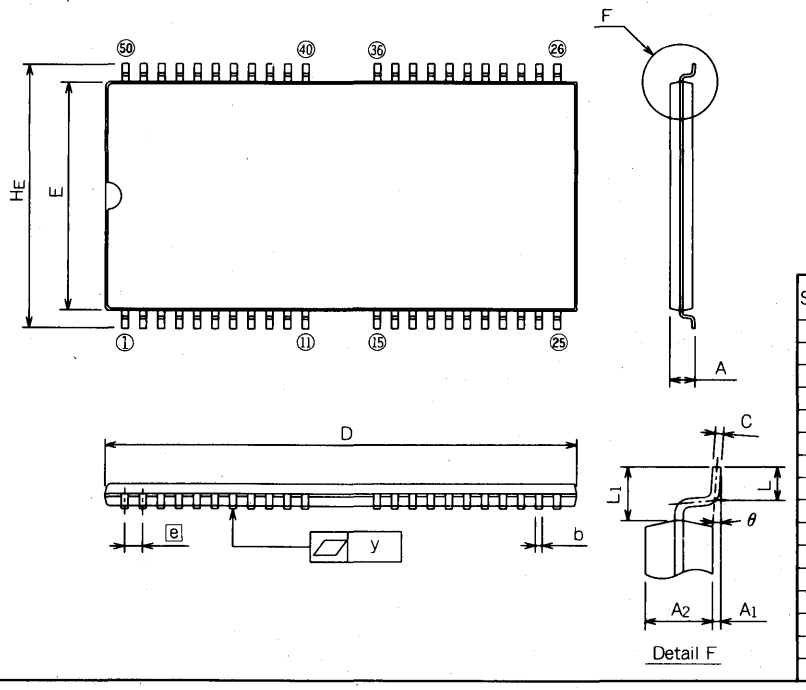
PACKAGE OUTLINES

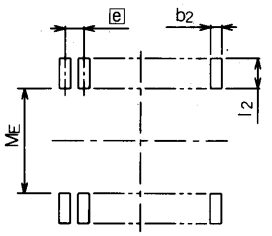
50P3W-L

Plastic 50pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)
*TSOP050-P-0400	–	

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.2
A_2	–	1.0	–
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	–	0.8	–
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	10.36	–
l_2	0.9	–	–
b_2	–	0.5	–

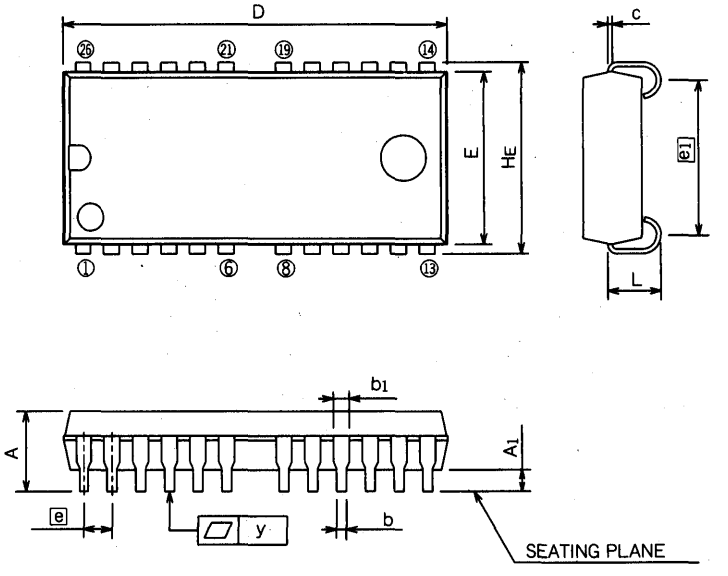
PACKAGE OUTLINES

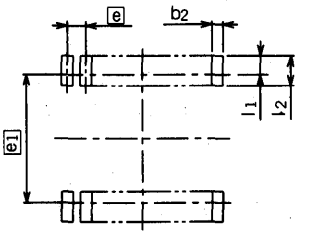
26P0D-B

Plastic 26pin 300mil SOJ(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ26/24-P-300-1.27	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

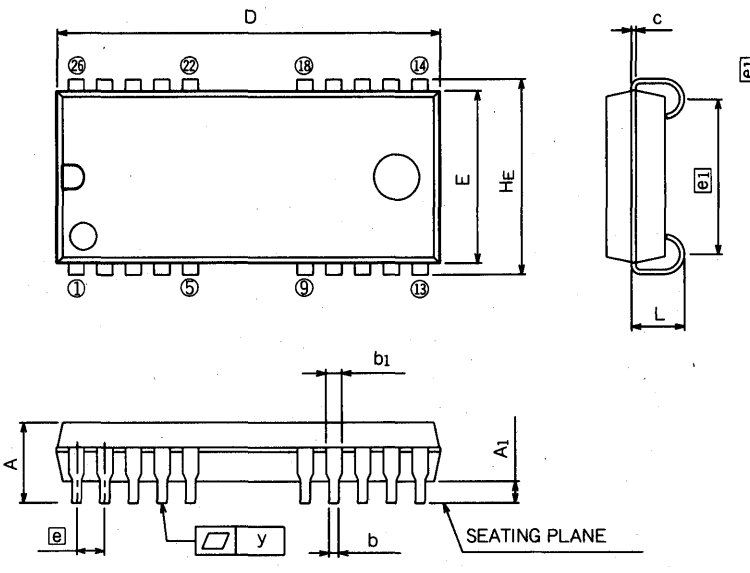
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	17.01	17.14	17.27
E	7.52	7.62	7.72
e	—	1.27	—
e_1	6.73	6.86	6.99
H_E	8.35	8.45	8.55
L	2.75	2.85	2.95
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

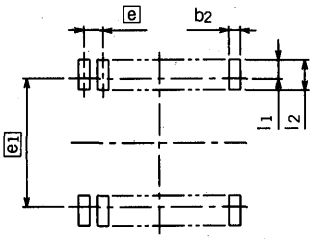
26P0J

Plastic 26pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ26/20-P-300-1.27	—	0.75	Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	17.02	17.15	17.28
E	7.52	7.62	7.72
e	—	1.27	—
e_1	6.73	6.86	6.99
H_E	8.35	8.45	8.55
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

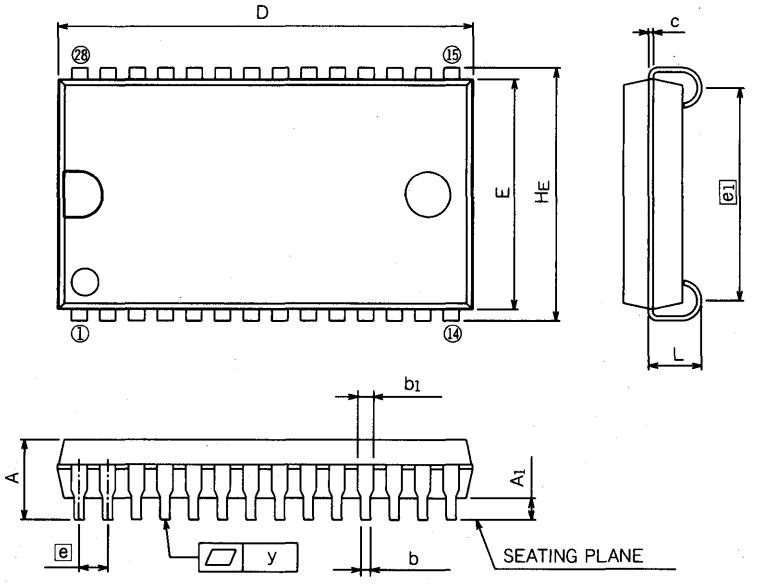
PACKAGE OUTLINES

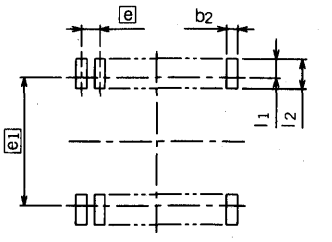
28P0K

Plastic 28pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ28-P-400-1.27	MO-061AA	1.08	Alloy 42

Scale : 3/1





Recommended Mount Pad

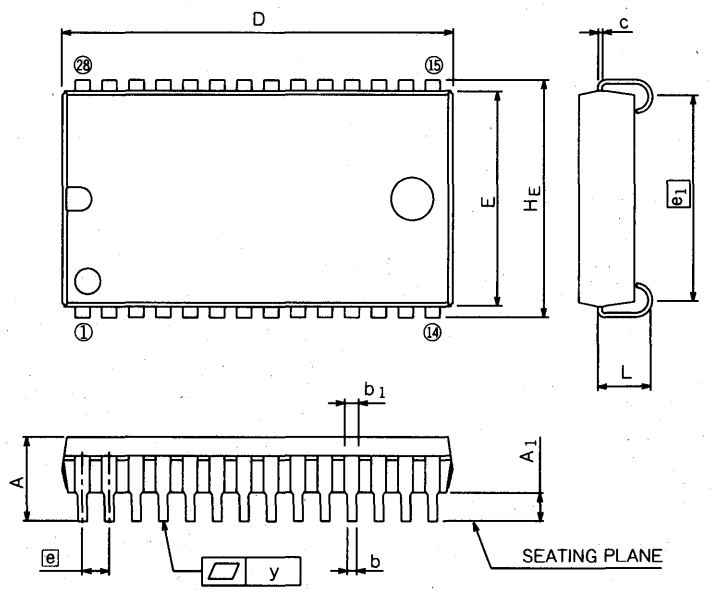
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	18.28	18.41	18.54
E	10.03	10.16	10.29
e	—	1.27	—
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

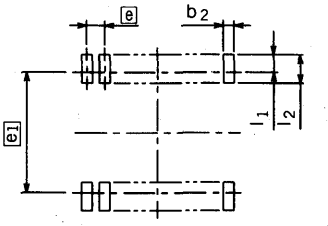
28P0N-A

Plastic 28pin 400mil SOJ(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ28-P-400-1.27	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	18.28	18.41	18.54
E	10.03	10.16	10.29
e	—	1.27	—
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.75	2.85	2.95
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

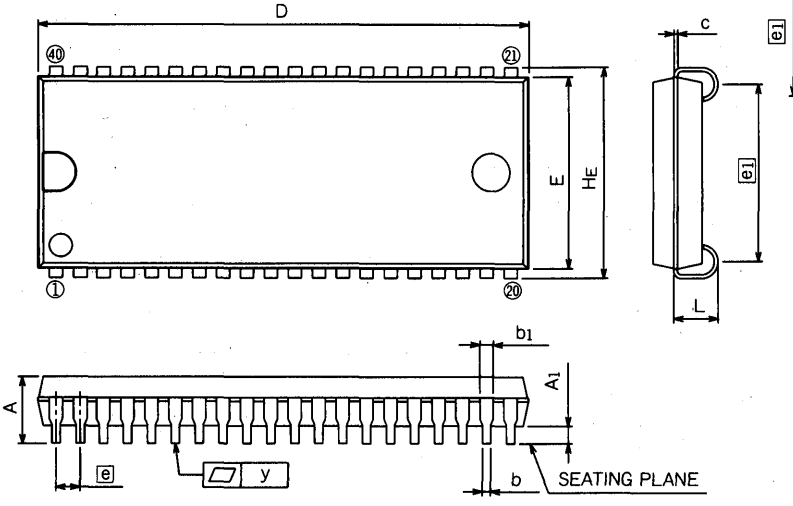
PACKAGE OUTLINES

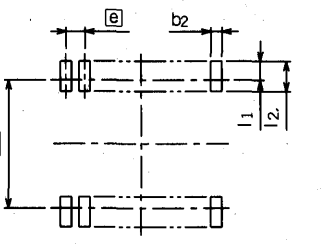
40P0K

Plastic 40pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ40-P-400-1.27	–	1.53	Alloy 42

Scale : 2.5/1





Recommended Mount Pad

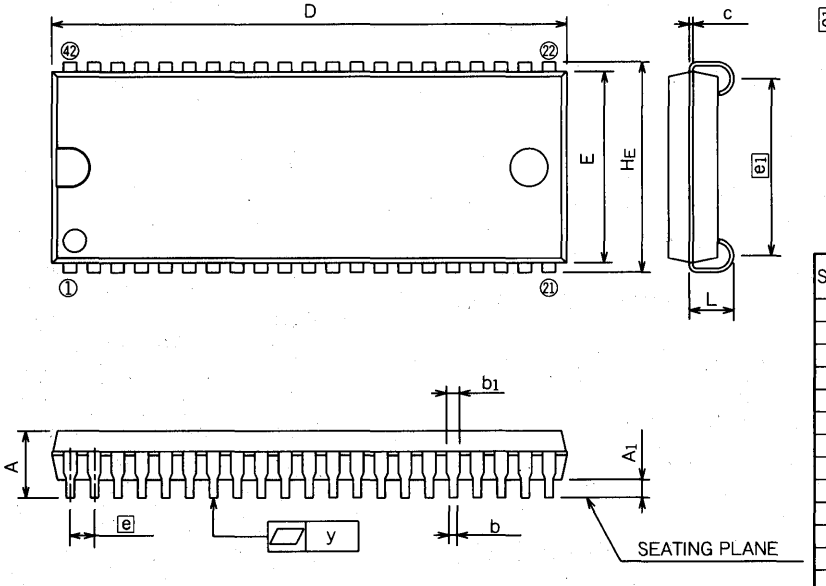
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	25.91	26.04	26.17
E	10.03	10.16	10.29
e	–	1.27	–
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–

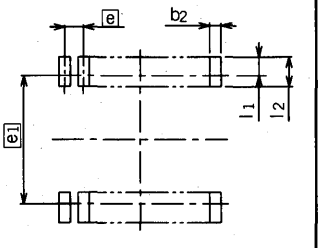
42P0K

Plastic 42pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ42-P-400-1.27	–		Alloy 42

Scale : 2.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	27.17	27.3	27.43
E	10.03	10.16	10.29
e	–	1.27	–
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–

MITSUBISHI ELECTRIC

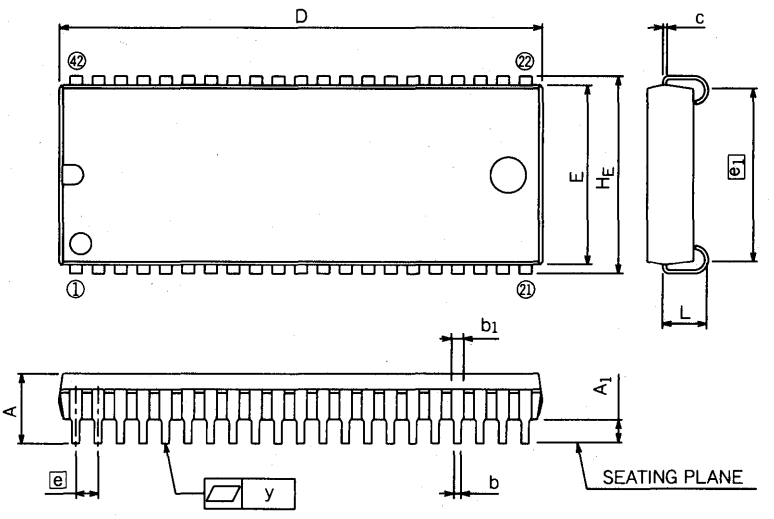
PACKAGE OUTLINES

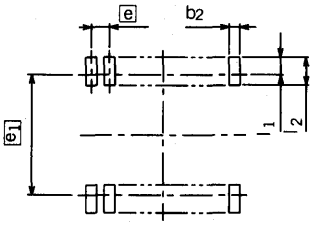
42P0N-A

Plastic 42pin 400mil SOJ(LOC)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ42-P-400-1.27	—		Alloy 42

Scale : 2.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	27.17	27.3	27.43
E	10.03	10.16	10.29
e	—	1.27	—
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.75	2.85	2.95
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

PRECAUTIONS IN HANDLING MOS ICs/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1MΩ resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchro-scopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to § 2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

4M DRAM(5V Version)

2

M5M44100BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 1-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)
M5M44100BXX-6,-6S	60	15	30
M5M44100BXX-7,-7S	70	20	35

Type name	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44100BXX-6,-6S	110	400
M5M44100BXX-7,-7S	130	350

XX = J, TP

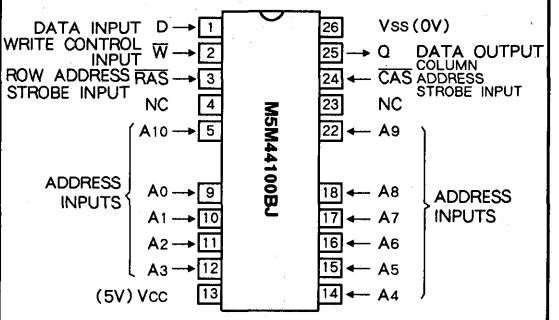
- Standard 26pin SOJ, 26pin TSOP (II)
- Single 5V ± 10% supply
- Low stand-by power dissipation
  - CMOS Input level ..... 5.5mW (max)
  - CMOS Input levle ..... 0.55mW (max)*
- Low operating power dissipation
  - M5M44100BXX-6,-6S ..... 550.0mW (max)
  - M5M44100BXX-7,-7S ..... 467.5mW (max)
- Extended refresh capability
  - Extended refresh current ..... 150 µA (max)
- Self refresh capability
  - Self refresh current ..... 150 µA (max)*
- Fast-page mode (2048-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, CBR Self Refresh (-6S, -7S) capabilities.
- Early write operation gives common I/O capability.
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9)*
- 16-bit parallel test mode capability

* : Applicable to self refresh version (M5M44100BJ, TP -6S, -7S : option) only.

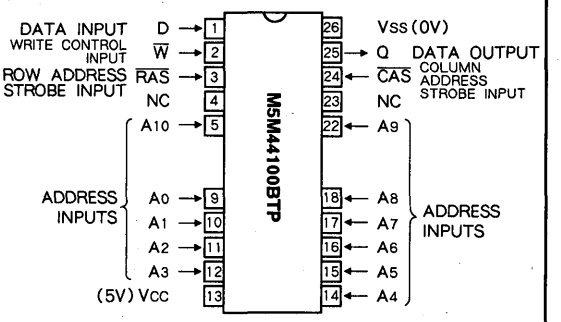
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J (300mil SOJ)



Outline 26P3Z-E (300mil TSOP)

NC : NO CONNECTION

FUNCTION

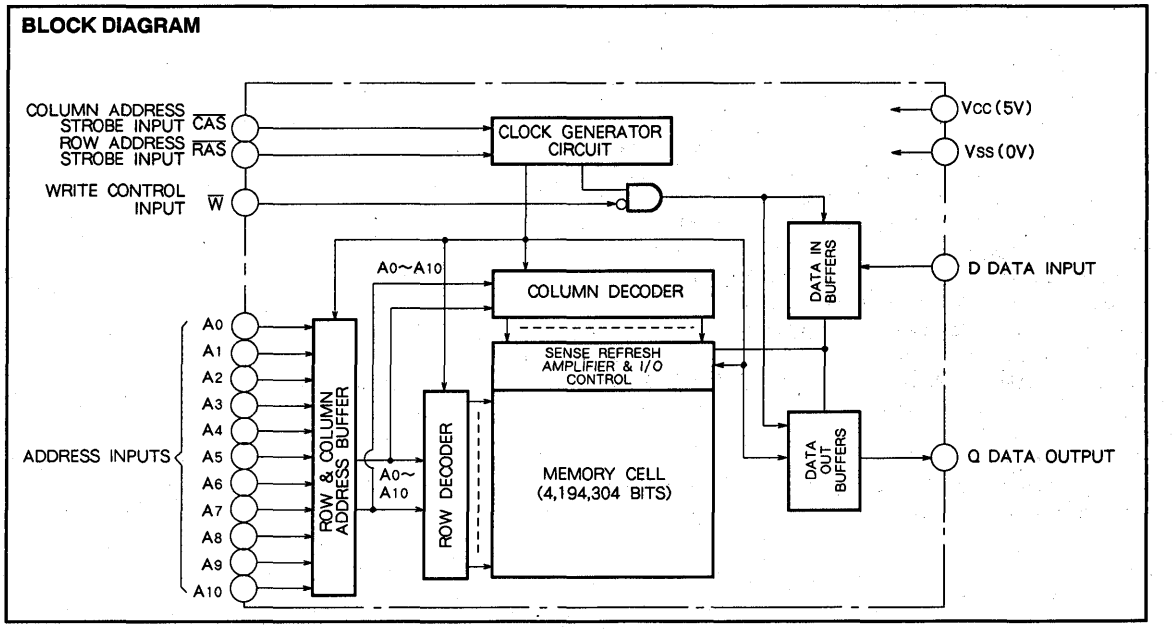
The M5M44100BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1. Input condition for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	VLD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh (Extended*)	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self Refresh*	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	− 1~7	V
V_I	Input voltage		− 1~7	V
V_O	Output voltage		− 1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage	− 2.0		0.8	V

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = − 5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V ≦ V_{OUT} ≦ 5.5V	− 10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 6.5V, 0ther inputs pins=0V	− 10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4, 5)	M5M44100B-6, -6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			100	mA
		M5M44100B-7, -7S				85	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
		M5M44100B	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5, output open			1	
		M5M44100B(S)				0.1*	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3, 5)	M5M44100B-6, -6S	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}, t_{RC} = min. output open			100	mA
		M5M44100B-7, -7S				85	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Page-Mode (Note 3, 4, 5)	M5M44100B-6, -6S	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min., output open			100	mA
		M5M44100B-7, -7S				85	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M44100B-6, -6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC} = min. output open			85	mA
		M5M44100B-7, -7S				75	
$I_{CC8(AV)}$*	Average supply current from V_{CC} Extended-refresh cycle (Note 6)		Stand-by: $\overline{RAS}$ ≧ V_{CC} − 0.2V, $\overline{CAS}$ ≧ V_{CC} − 0.2V or $\overline{CAS}$ ≦ 0.2V; $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling, $\overline{W}$ ≦ 0.2V or ≧ V_{CC} − 0.2V, $\overline{OE}$ ≦ 0.2V or ≧ V_{CC} − 0.2V, A_0~A_9 ≦ 0.2V or ≧ V_{CC} − 0.2V, DQ = open, t_{RC} = 125 μs, t_{RAS} = t_{RAS} min~1 μs			150	μA
$I_{CC9(AV)}$*	Average supply current from V_{CC}, Self-refresh cycle (Note 6)	M5M44100B(S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			150	μA

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44100BJ,TP	V_I = Vss f = 1MHz V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
C_O	Output capacitance		V_O = Vss, f = 1MHz, V_I = 25mVrms			7	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44100B-6, -6S		M5M44100B-7, -7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		60		70	ns
t_{AA}	Column Address access time	(Note 7, 10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40	ns
t_{CLZ}	Output low impedance from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	20	ns

Note 6. An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms/128ms*) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{ASC} \geq t_{ASC}(max)$.
9. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
10. Assumes that $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \leq t_{ASC}(max)$.
11. Assumes that $t_{CP} \leq t_{CP}(max)$ and $t_{ASC} \geq t_{ASC}(max)$.
12. $t_{OFF}(max)$ and $t_{OEZ}(max)$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\,\mu A|$) and is not reference to $V_{OH}(min)$ or $V_{OL}(max)$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)
(T_a = 0~70℃, V_{CC}=5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44100B-6, -6S		M5M44100B-7, -7S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time	M5M44100B		16.4		16.4	ms
		M5M44100B(S)		128		128	
t_{RP}	$\overline{RAS}$ high pulse width		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_T	Transition time	(Note 18)	1	50	1	50	ns

Note 13. The timing requirements are assumed t_T = 5ns.
14. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.
15. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$, access time is t_{RAC}.
If t_{RCD} is greater than $t_{RCD}(max)$, access time is controlled exclusively by t_{CAC} or t_{AA}.
$t_{RCD}(min)$ is specified as $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
16. $t_{RAD}(max)$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \leq t_{ASC}(max)$, access time is controlled exclusively by t_{AA}.
17. $t_{ASC}(max)$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD}(max)$ and $t_{ASC} \geq t_{ASC}(max)$, access time is controlled exclusively by t_{CAC}.
18. t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 19)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 19)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns

Note 19. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{RWC}	Read Write cycle time (Note 20)	130		155		ns
t_{RMWC}	Read modify write cycle time (Note 21)	130		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width	85	10000	95	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	40	10000	45	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	85		95		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	40		45		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	15		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	60		70		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	30		35		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		15		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		15		ns

Note 20. t_{RWC} is specified as $t_{RWC}(min) = t_{RCD}(max) + t_{CWD}(min) + t_{RWL}(min) + t_{RP}(min) + 3t_T$.

21. t_{RMWC} is specified as $t_{RMWC}(min) = t_{RAC}(max) + t_{RWL}(min) + t_{RP}(min) + 3t_T$.

22. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{WCS} \geqq t_{WCS}(min)$, an early write cycle is performed, and the data output keeps the high impedance state. When $t_{RWD} \geqq t_{RWD}(min)$, $t_{CWD} \geqq t_{CWD}(min)$, $t_{AWD} \geqq t_{AWD}(min)$, and $t_{CPWD} \geqq t_{CPWD}(min)$ (for fast page mode cycle only), a read write cycle is performed, and the data of the selected address will be read out on the data output.
If neither of the above condition (delayed write) is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 23)

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	60		70		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	105	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$low (Note 22)	35		40		ns

Note 23. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24. t_{RAS}(min) is specified as two cycles of $\overline{CAS}$ input are performed.
25. t_{CP}(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh Cycle* (Note 26)

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		ns

Note 26. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits				Unit
		M5M44100B-6S		M5M44100B-7S		
		Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Test Mode Specifications (Note 27)

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4, 5)	M5M44100B-6, -6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			115	mA
		M5M44100B-7, -7S				100	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3, 5)	M5M44100B-6, -6S	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}, t_{RC} = min. output open			115	mA
		M5M44100B-7, -7S				100	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4, 5)	M5M44100B-6, -6S	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min., output open			115	mA
		M5M44100B-7, -7S				100	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M44100B-6, -6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC} = min. output open			100	mA
		M5M44100B-7, -7S				85	

Note 27. All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	ParameterLimits		Limits				Unit
			M5M44100B-6, -6S		M5M44100B-7, -7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		65		75	ns
t_{AA}	Column address access time	(Note 7, 10)		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45	ns

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	115		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width	65	10000	75	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	65		75		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	35		40		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M44100B-6, -6S		M5M44100B-7, -7S		
			Min	Max	Min	Max	
t_{RWC}	Read write cycle time	(Note 20)	135		160		ns
t_{RMWC}	Read modify write cycle time	(Note 21)	135		160		ns
t_{RAS}	$\overline{RAS}$ low pulse width		90	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		45	10000	50	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		90		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		45		50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	65		75		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 22)	35		40		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M44100B-6, -6S		M5M44100B-7, -7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		65		75		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 25)	115	200000	125	200000	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	40		45		ns

Test Mode Set Cycle

Symbol	Parameter	Limits				Unit
		M5M44100B-6, -6S		M5M44100B-7, -7S		
		Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	10		15		ns

Note 28. Self refresh sequence

Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distriduted refresh during Read/Write operation

(A) Timing Diagrams

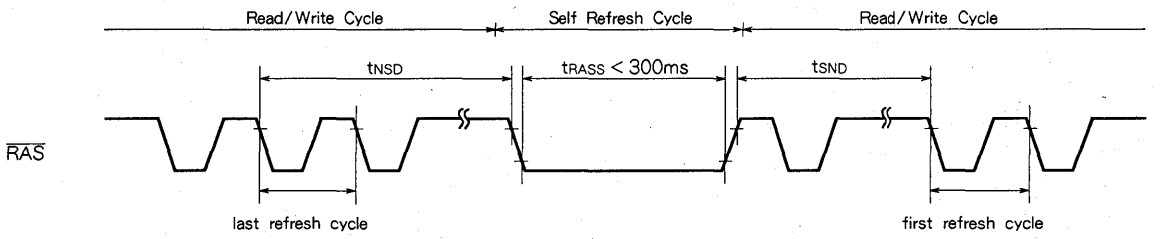


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

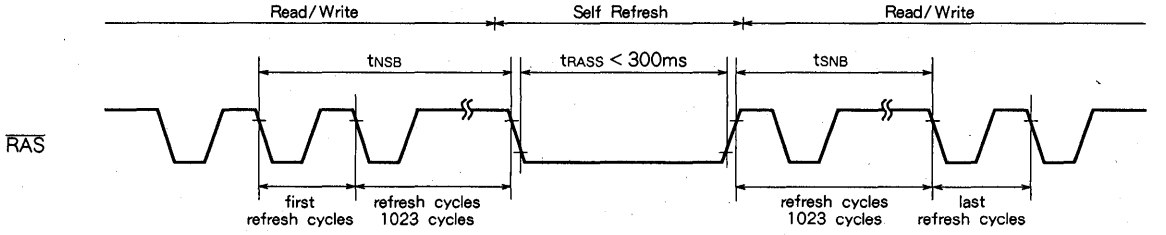


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

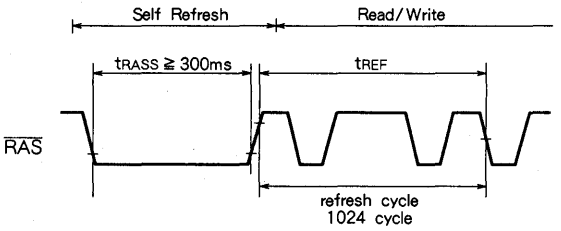


Table 4

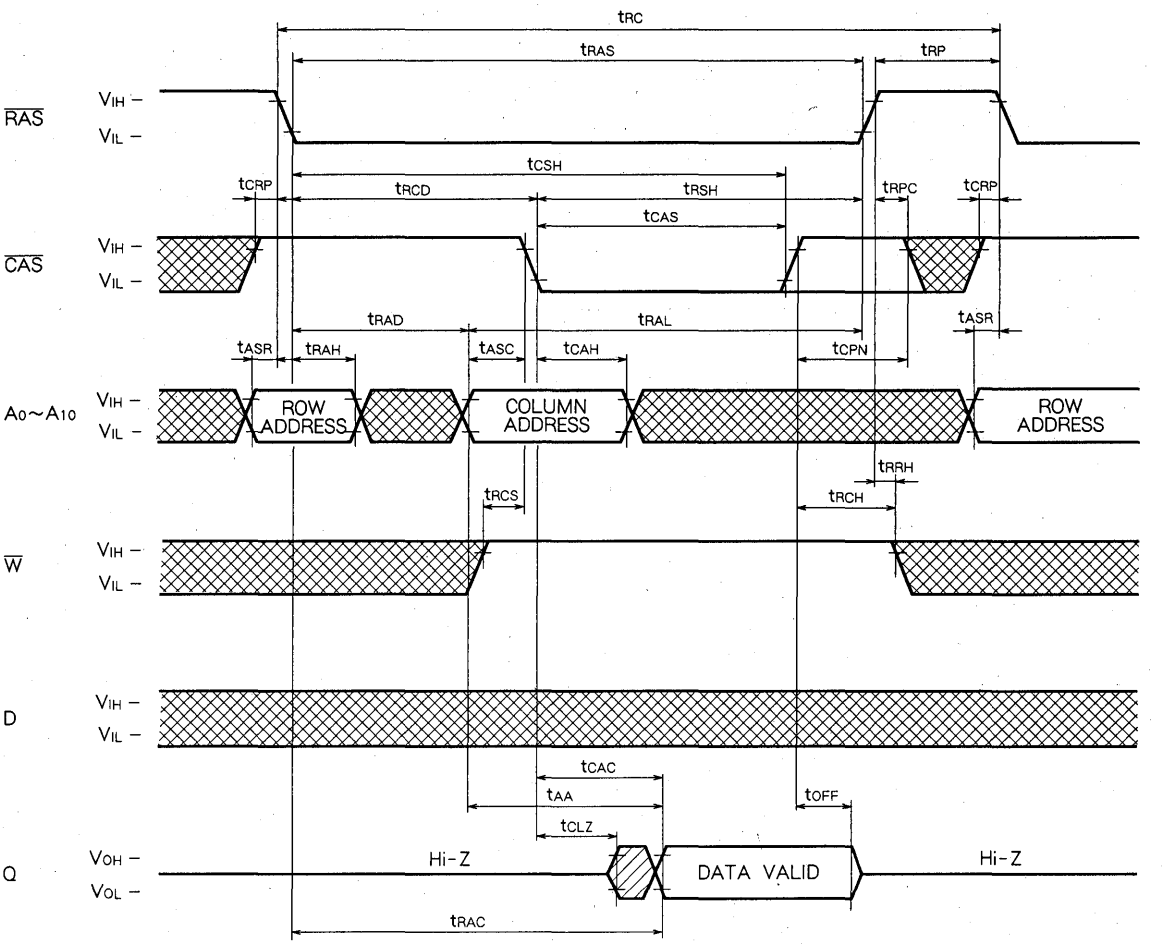
Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh RAS only distributed refresh CBR burst refresh RAS only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, RAS only distributed refresh, CBR burst refresh, RAS only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of RAS signal at the end of self refresh operation.

Timing Diagrams (Note 29)

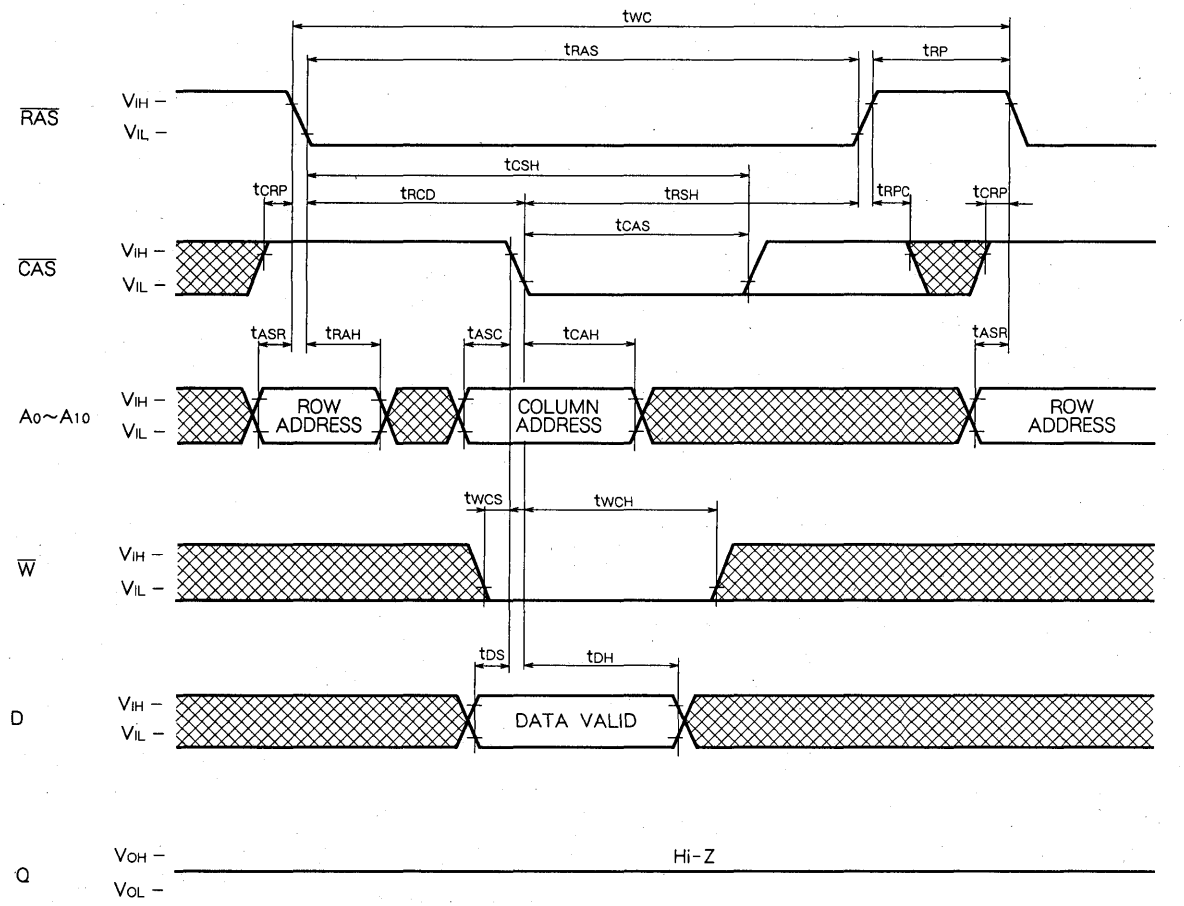
Read Cycle



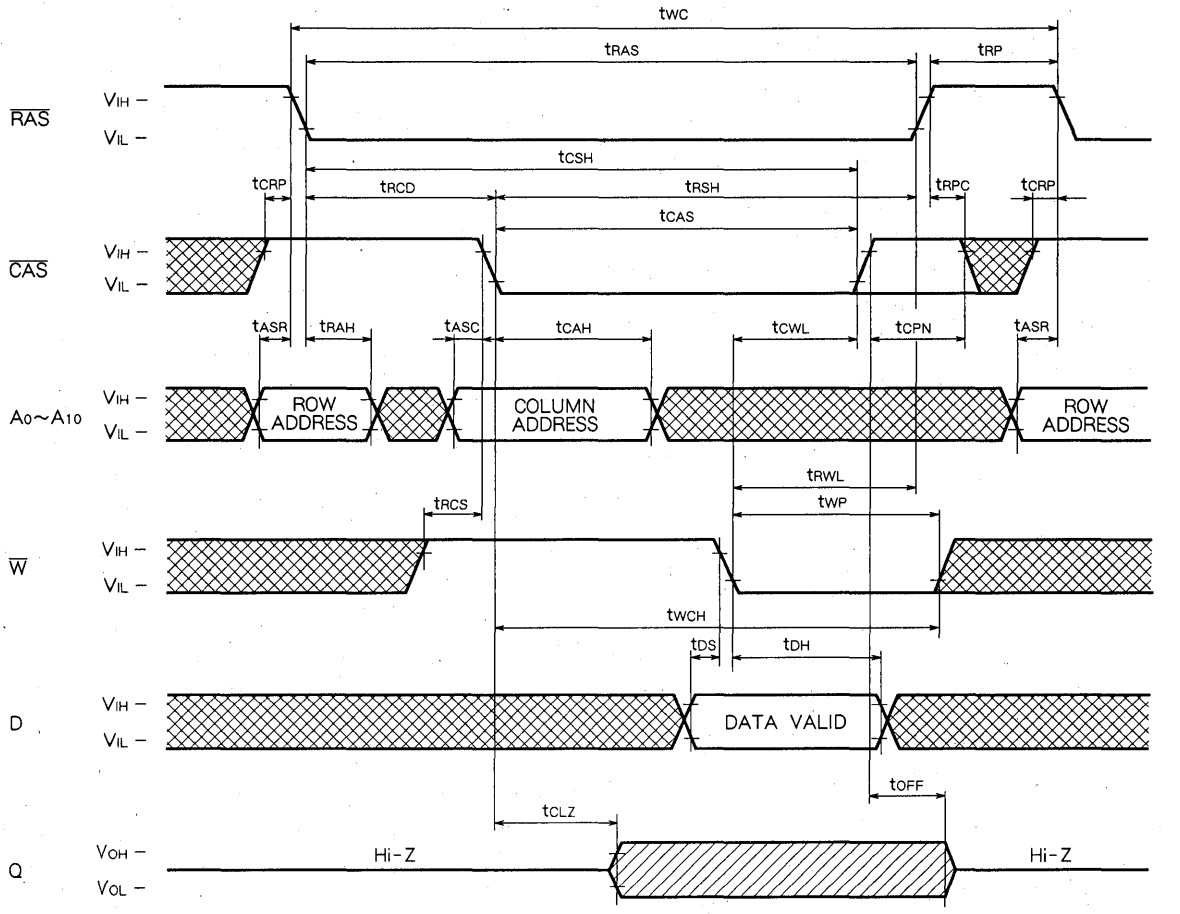
Note 29. Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$.

Indicates the invalid output.

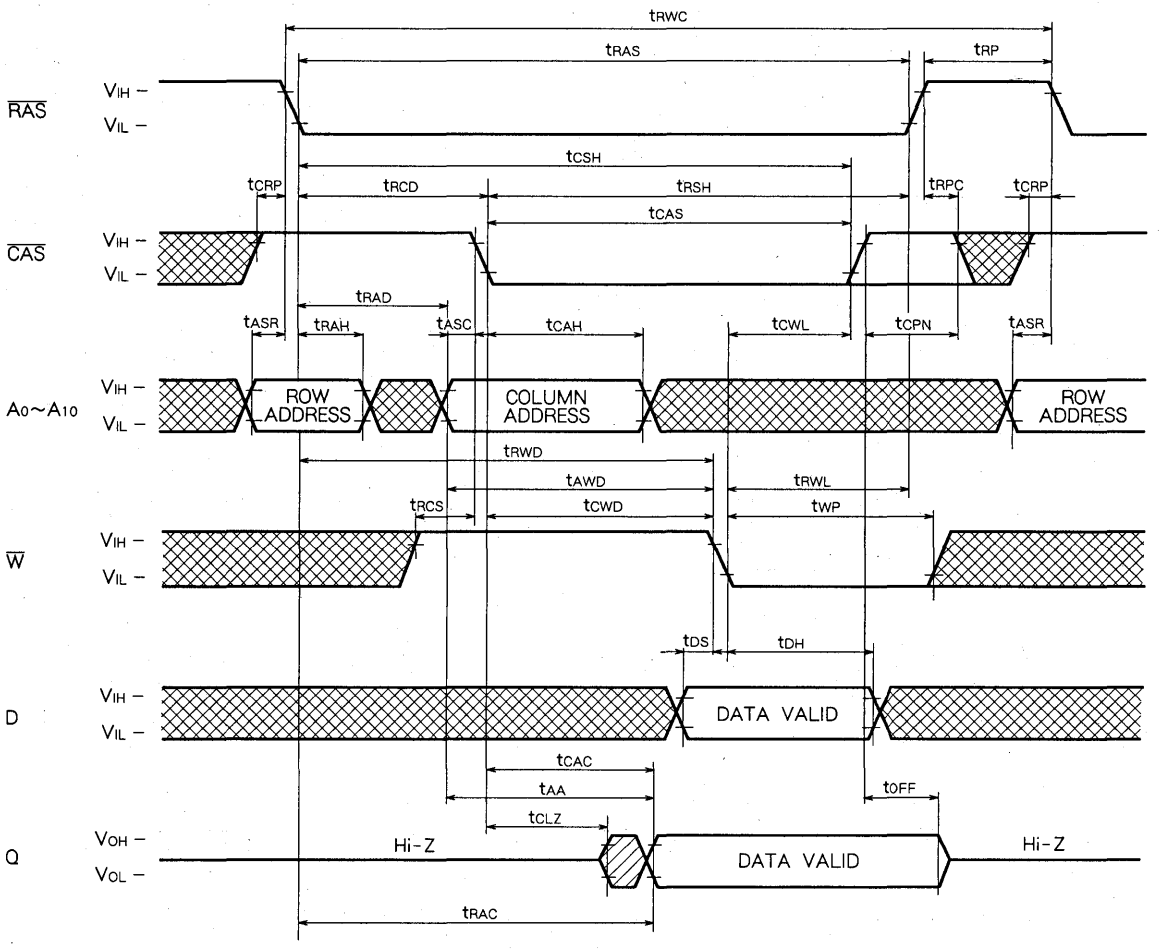
Write Cycle (Early write)



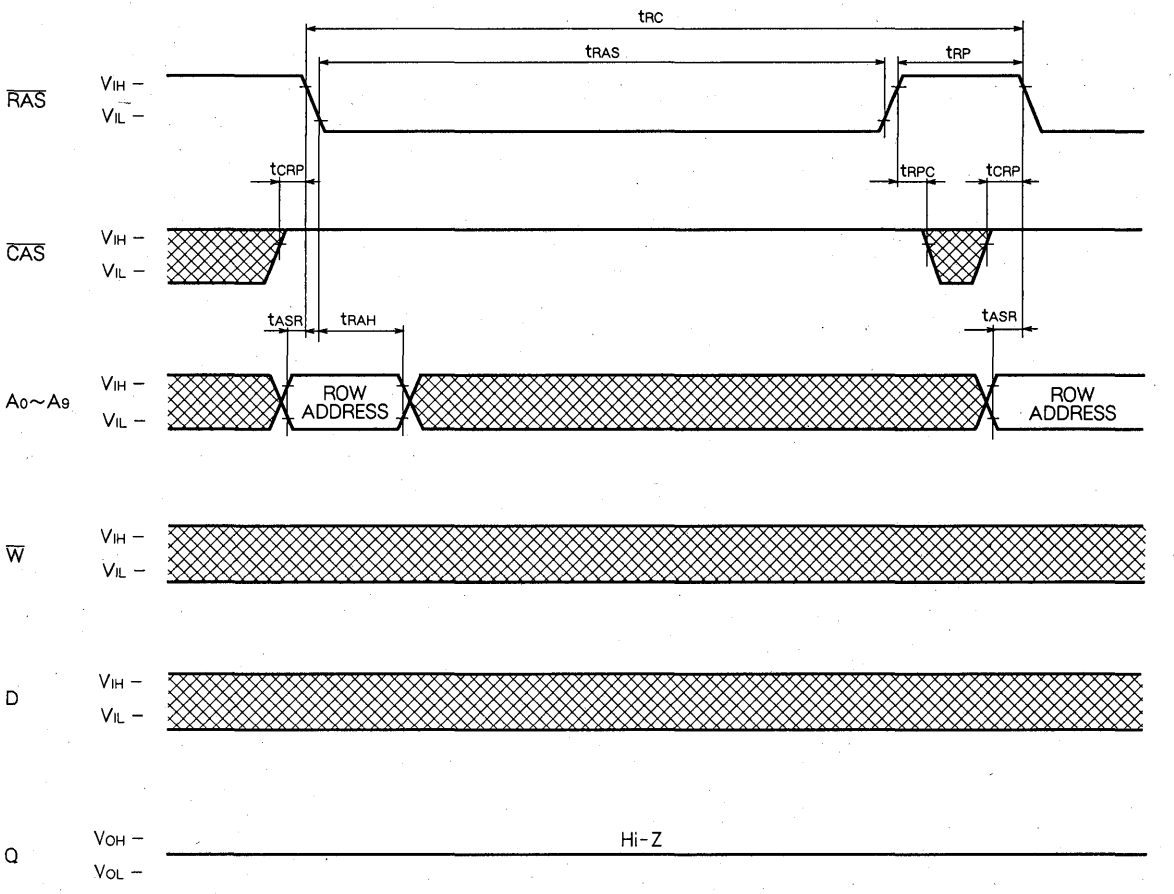
Write Cycle (Delayed Write)



Read-Write, Read-Modify-Write Cycle

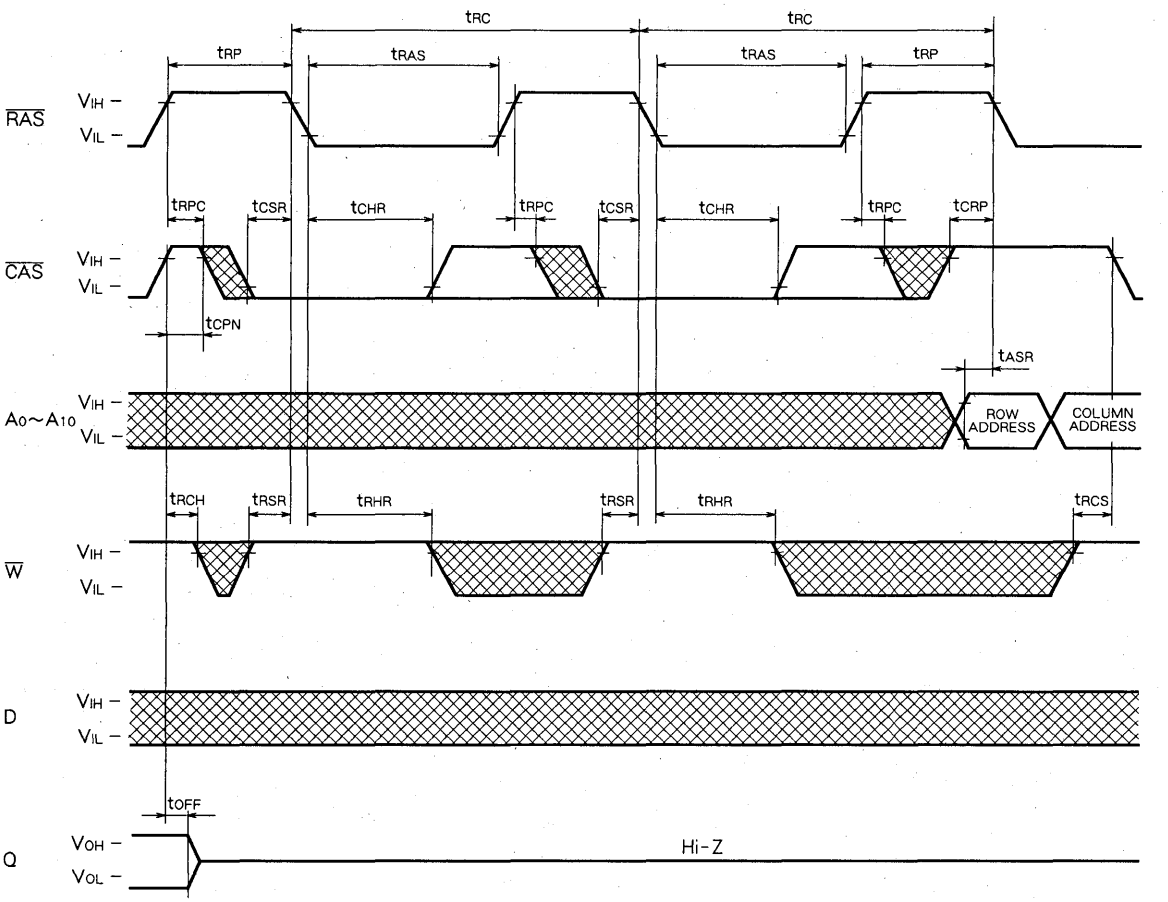


$\overline{RAS}$-only Refresh Cycle (Note 30)

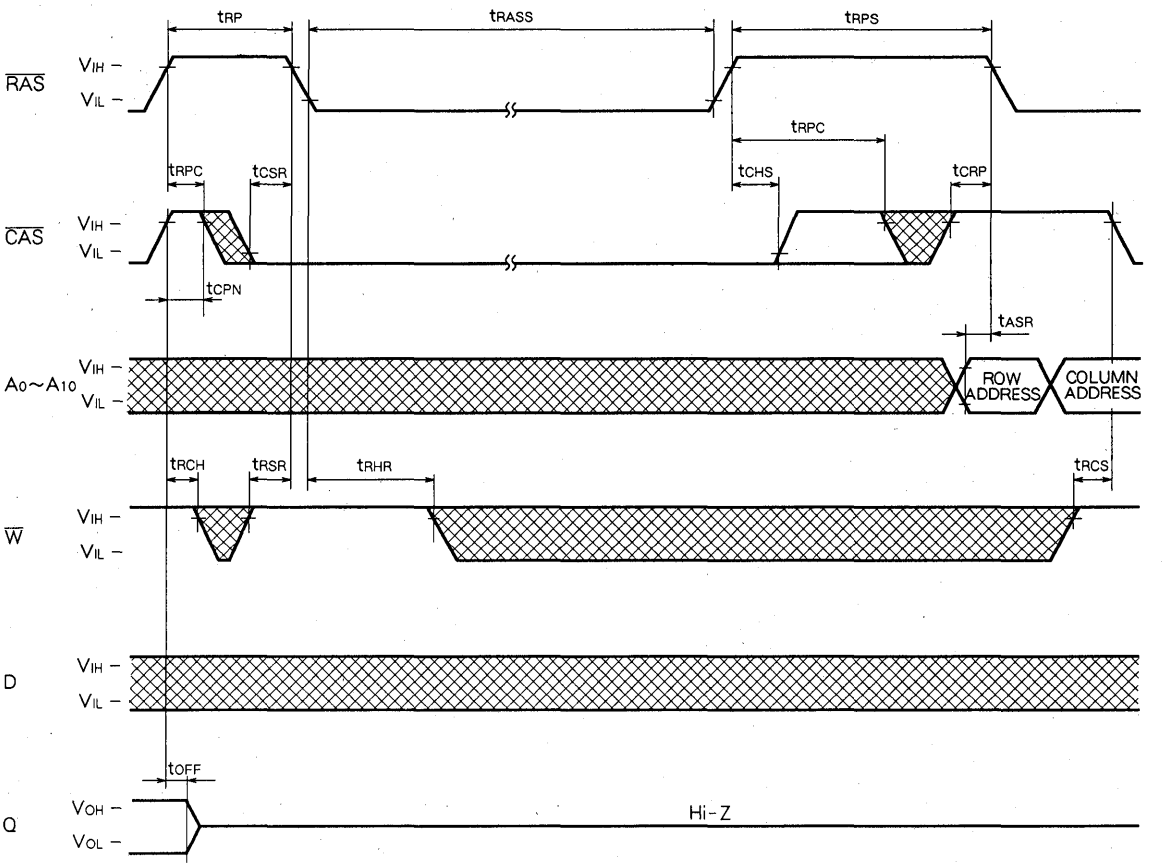


Note 30. A10 may be VIH or VIL. Refresh address : A0 (ROW)~A9 (ROW)

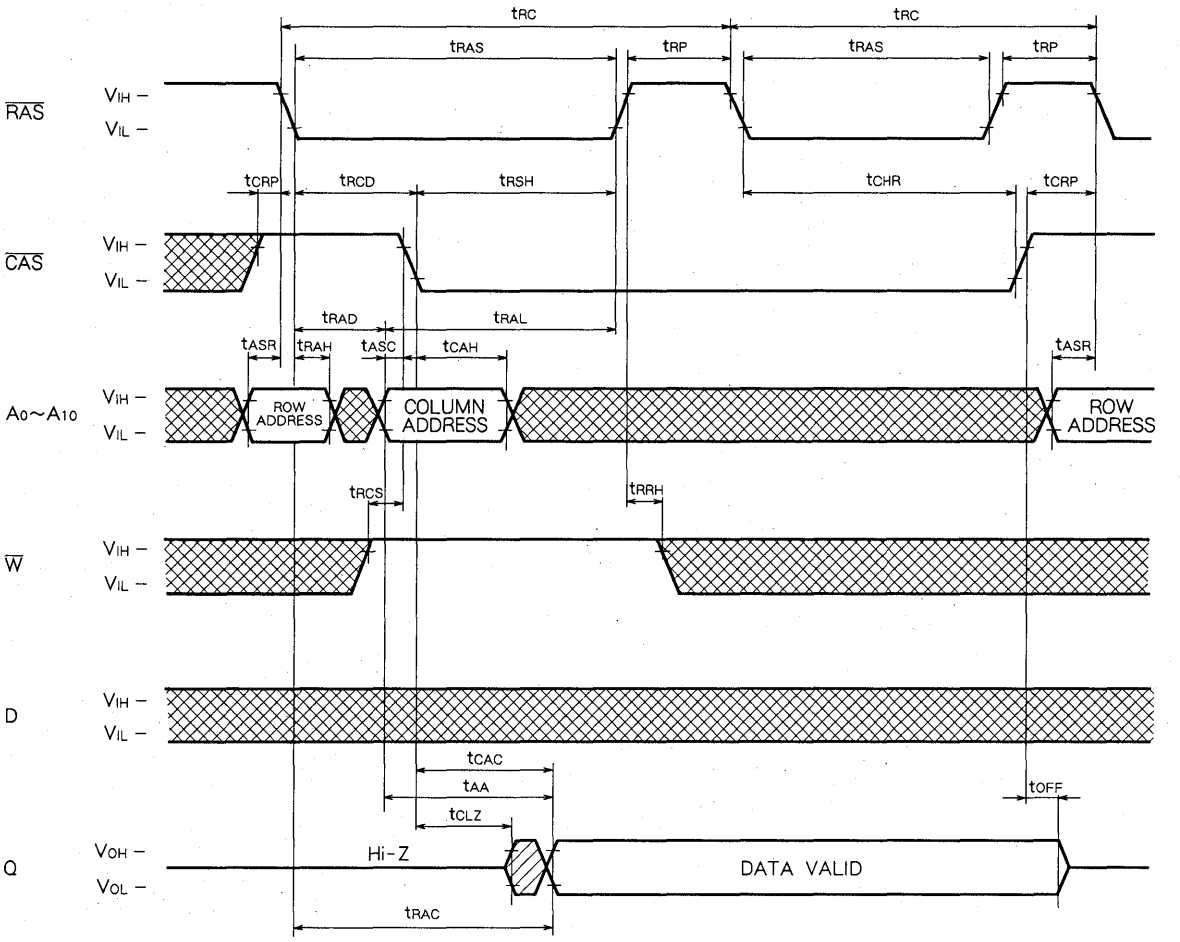
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



Self Refresh Cycle* (Note 28)

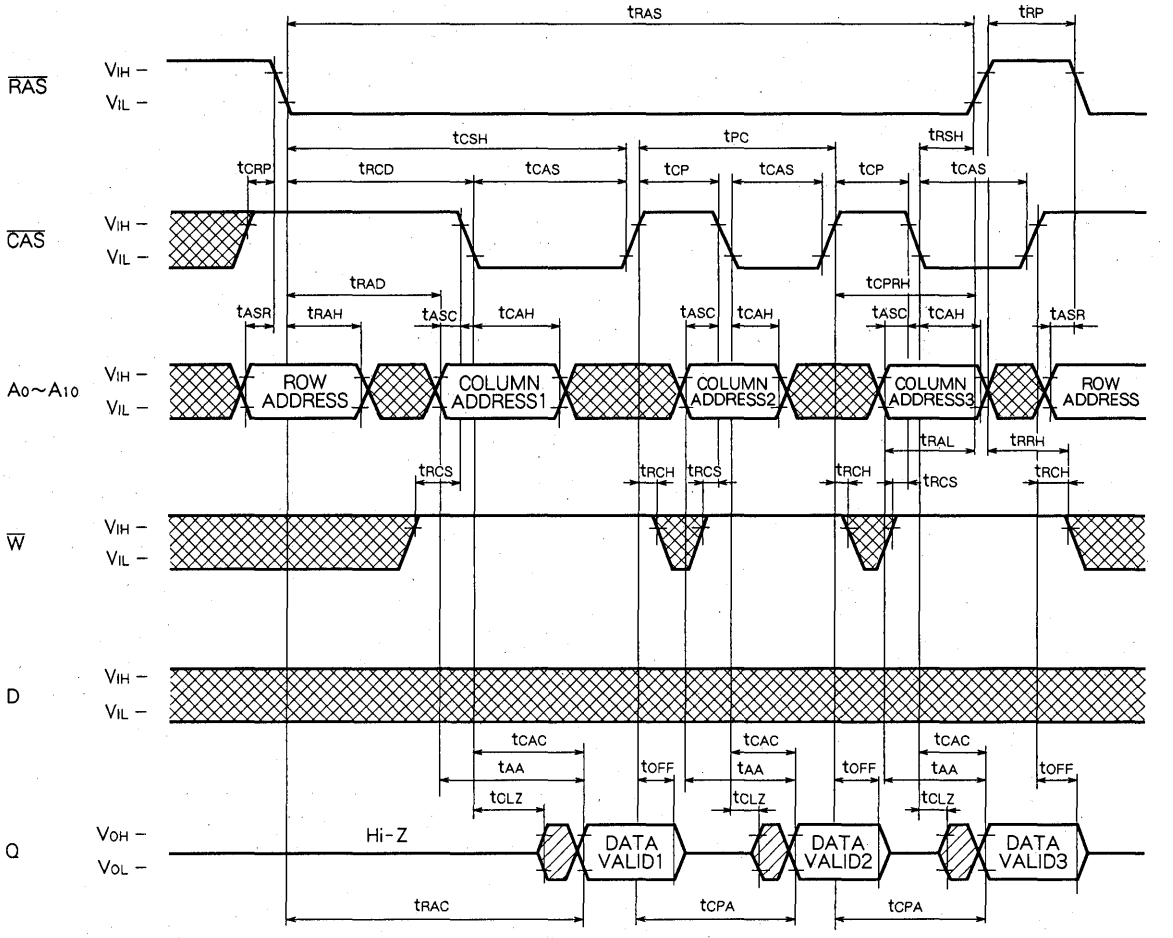


Hidden Refresh Cycle (Read) (Note 31)

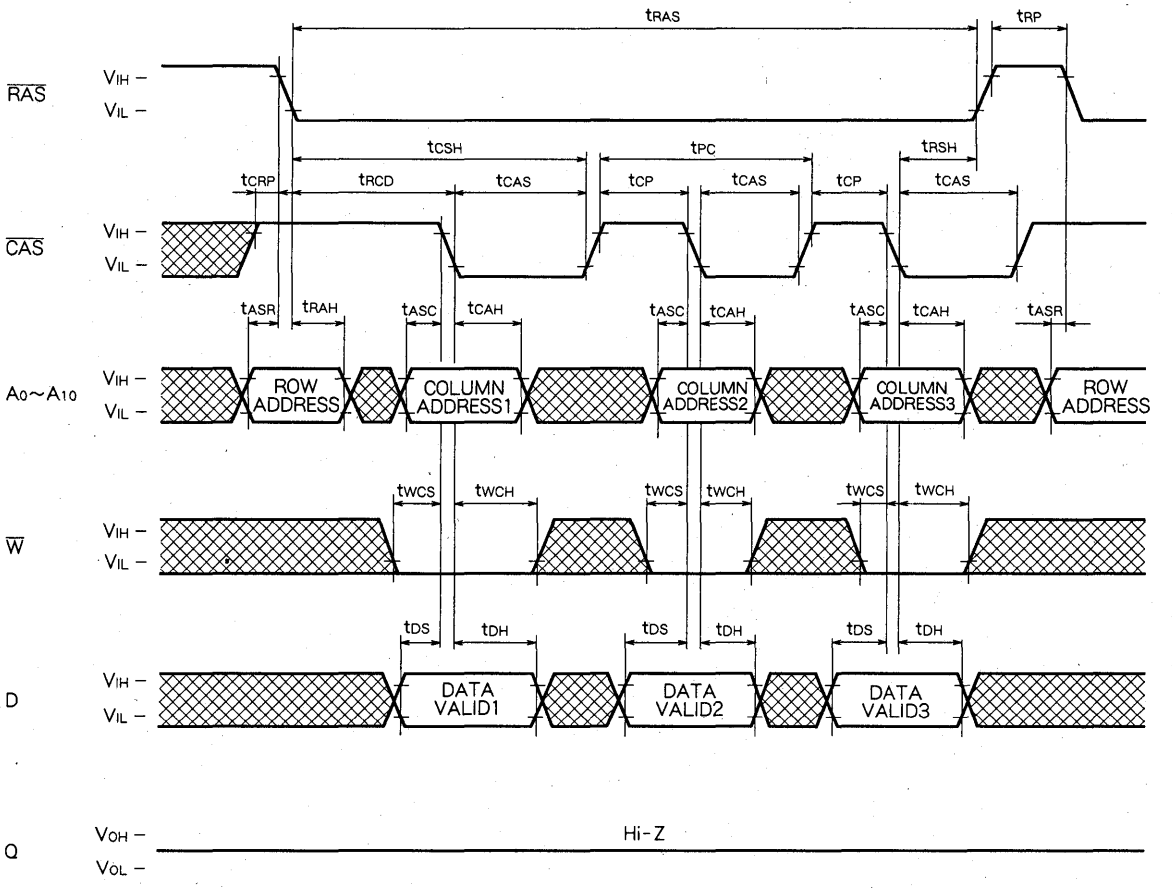


Note 31. Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

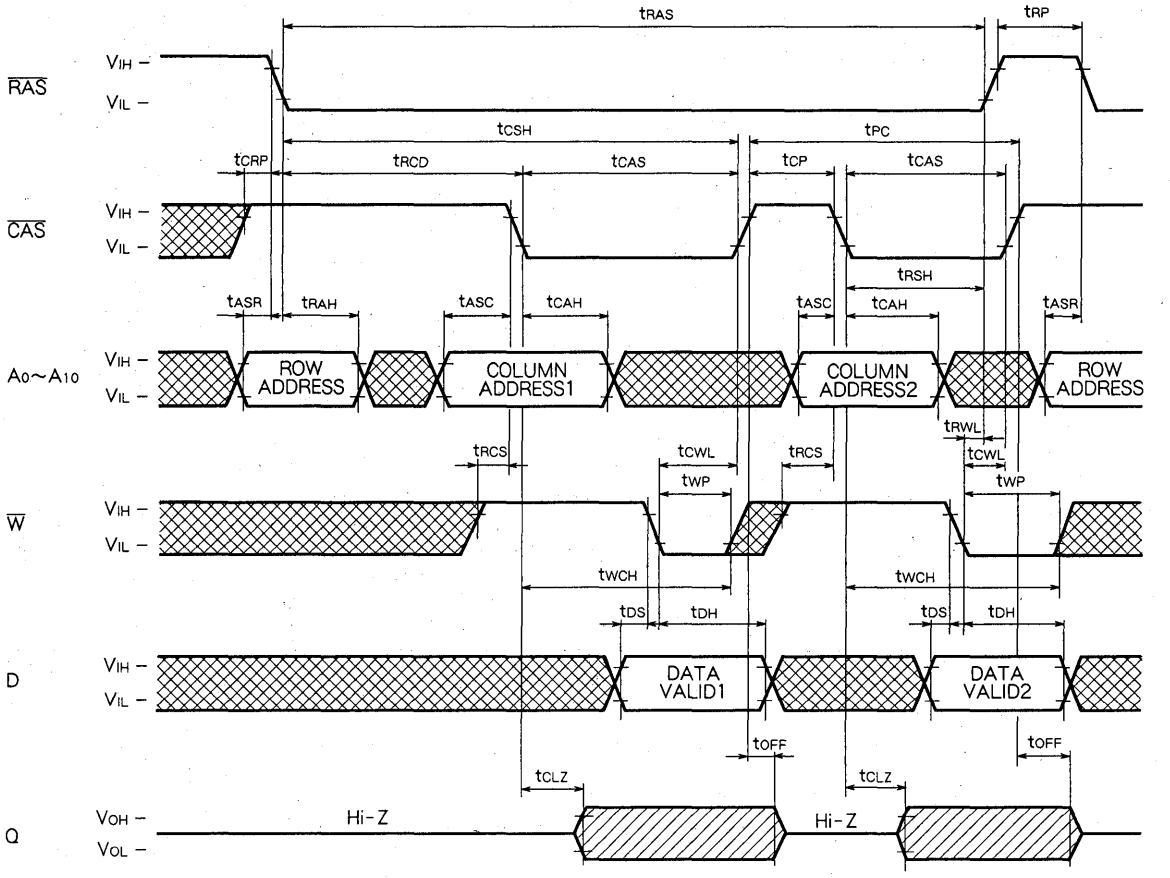
Fast Page Mode Read Cycle



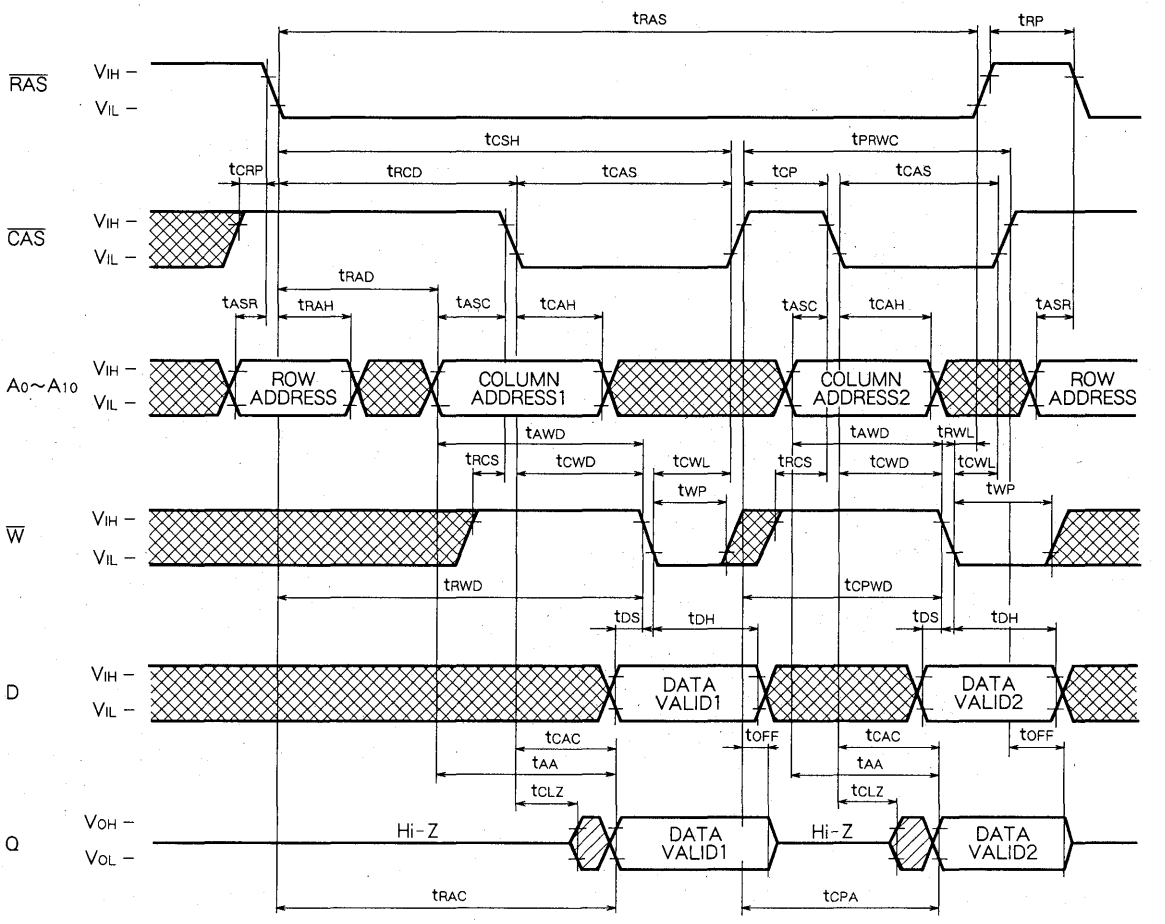
Fast Page Mode Write Cycle (Early Write)



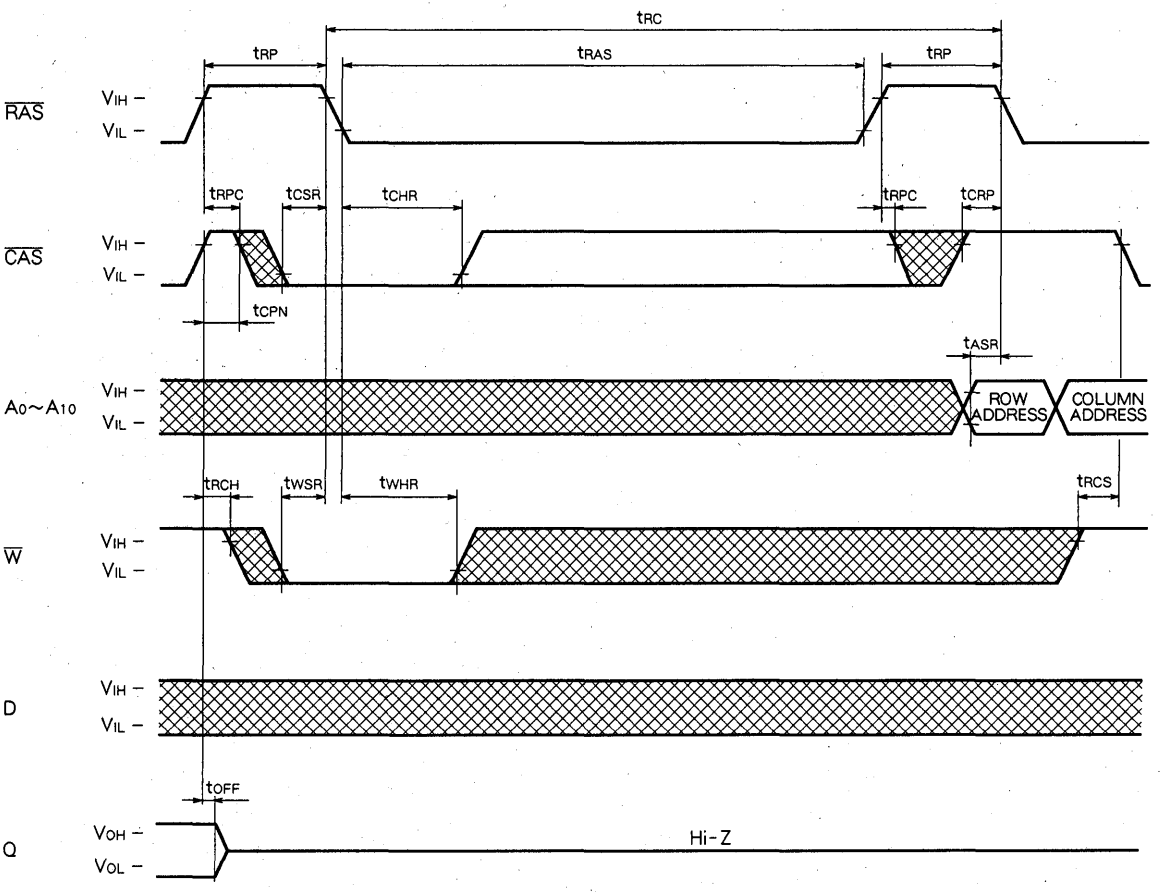
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Test Mode Set Cycle (Note 32)



Note 32. This cycle is also available for the initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the devics is intemally organized as 16-bits wide (256 kilobytes deep).
No addressind of A_{10} (both row and column) and A_0, A_1 (column only) is required.
During a write cycle, data on the input pin is written in parallel into all 16-bits.
During a read cycle, the each output pin indicates a HIGH state if all 16-bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

M5M44100CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (4194304-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

FEATURES

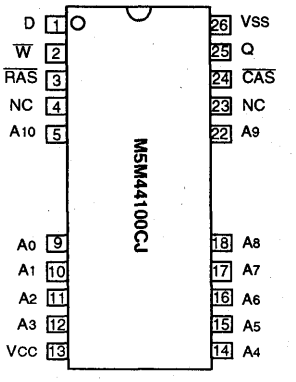
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44100CXX-5,-5S	50	13	25	90	500
M5M44100CXX-6,-6S	60	15	30	110	400
M5M44100CXX-7,-7S	70	20	35	130	350

XX=J,TP

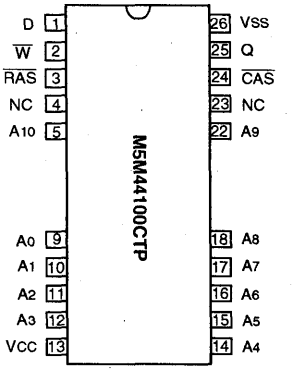
- Standard 26pin SOJ, 26pin TSOP (II)
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max) *
- Operating power dissipation
  - M5M44100Cxx-5,-5S ---------- 687.5mW (Max)
  - M5M44100Cxx-6,-6S ---------- 550.0mW (Max)
  - M5M44100Cxx-7,-7S ---------- 467.5mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 120 μA(Max)
- Extended refresh capability
  - Extended refresh current ---------- 120 μA(Max)
- Fast page mode(2048-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write operation gives common I/O capability.
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)
- 1024 refresh cycles every 128ms (A_0 ~ A_9) *
- 16-bit parallel test mode capability

* :Applicable to self refresh version (M5M44100CJ,TP-5S,-6S,-7S :option) only

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J(300mil SOJ)



Outline 26P3Z-E(300mil TSOP)

NC:NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
D	Data input
Q	Data output
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
Vcc	Power supply (+5V)
Vss	Ground (0V)

M5M44100CJ,TP-5,-5S:Under development

FUNCTION

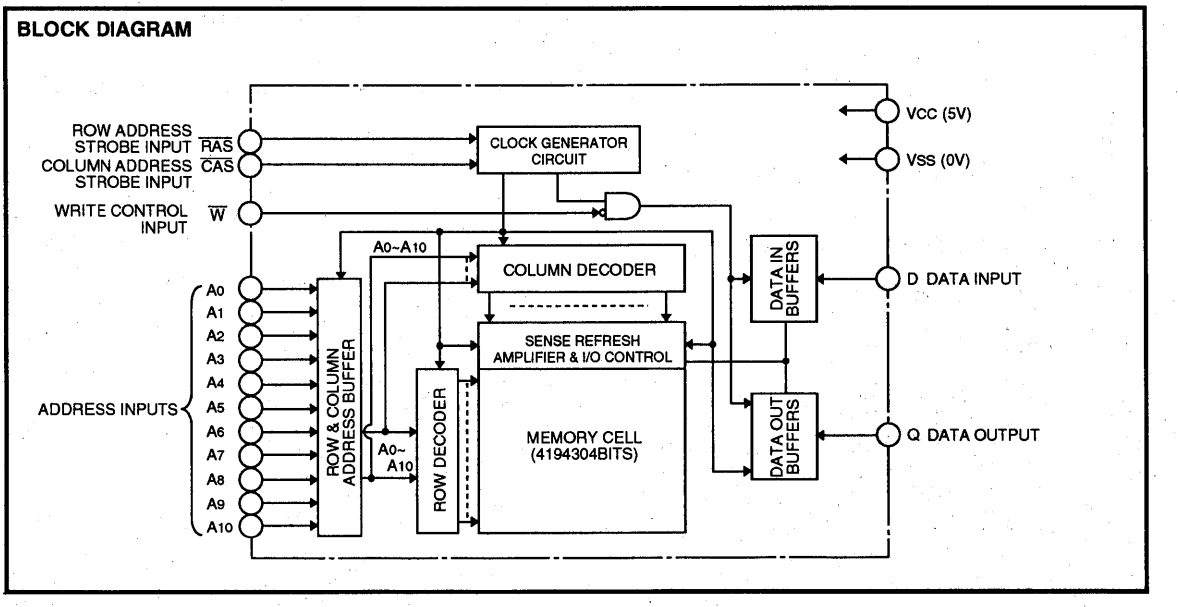
In addition to normal read, write, and read-modify-write operations the M5M44100CJ,TP provide a number of other functions, e. g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	VLD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	-2.0		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44100C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			125	mA
		M5M44100C-6,-6S				100	
		M5M44100C-7,-7S				85	
I_{CC2} (AV)	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.5V output open			1.0	
						0.1*	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44100C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			125	mA
		M5M44100C-6,-6S				100	
		M5M44100C-7,-7S				85	
I_{CC4}(AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44100C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			105	mA
		M5M44100C-6,-6S				85	
		M5M44100C-7,-7S				75	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44100C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			105	mA
		M5M44100C-6,-6S				85	
		M5M44100C-7,-7S				75	
I_{CC8}(AV)*	Average supply current from Vcc, Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V(Except for $\overline{RAS}$ falling edge) or ≧Vcc-0.2V A_0~A_{10}≦0.2V or ≧Vcc-0.2V, Q=open t_{RC}=125 μs, t_{RAS}=t_{RAS}min~1 μs			120	μA
I_{CC9}(AV)*	Average supply current from Vcc, Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			120	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I(D)}$	Input capacitance, data input	V_I=25mVrms			7	pF
C_O	Output capacitance	V_O=Vss, f=1MHz, V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns

Note 6:An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$- only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than $t_{REF(max)}$) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7:Measured with a load circuit equivalent to 2TTL loads and 100pF.
8:Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9:Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
10:Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11:Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12:$t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4	ms
t_{REF}	Refresh cycle time*			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	7	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_T	Transition time	(Note 18)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T=5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 19)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 19)	0		0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		35		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 21)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		8		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{WP}	Write pulse width		8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 20)	108		130		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width		68	10000	80	10000	95	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		31	10000	35	10000	45	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		68		80		95		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		31		35		45		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 21)	13		15		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 21)	50		60		70		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 21)	25		30		35		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{WP}	Write pulse width		8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns

Note 20: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{RWL(min)}+t_{RP(min)}+3t_T$.

21: t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the data output keeps the high impedance state. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the data will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the condition of the Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 22)

Symbol	Parameter	Limits						Unit
		M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	53		60		70		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 23)	85	100000	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 24)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 21)	30		35		40		ns

Note 22: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
23: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
24: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 25)

Symbol	Parameter	Limits						Unit
		M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		20		25		ns

Note 25: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 26)

Symbol	Parameter	Limits						Unit
		M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Test Mode Specification (Note 27)

ELECTRICAL CHARACTERISTICS (T_a=0～70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1} (AV)	Average supply current from V_{CC}, operating (Note 3,4,5)	M5M44100C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			145	mA
		M5M44100C-6,-6S	t_{RC}=t_{WC}=min.			115	
		M5M44100C-7,-7S	output open			100	
I_{CC3} (AV)	Average supply current from V_{CC}, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44100C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}			145	mA
		M5M44100C-6,-6S	t_{RC}=min.			115	
		M5M44100C-7,-7S	output open			100	
I_{CC4} (AV)	Average supply current from V_{CC}, Fast Page mode (Note 3,4,5)	M5M44100C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			120	mA
		M5M44100C-6,-6S	t_{PC}=min.			100	
		M5M44100C-7,-7S	output open			85	
I_{CC6} (AV)	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44100C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			120	mA
		M5M44100C-6,-6S	t_{RC}=min.			100	
		M5M44100C-7,-7S	output open			85	

Note 27:All previously specified electrical characteristics, switching characteristics, and timing requirements are applicable to that of rest mode.

SWITCHING CHARATERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6, 13, 14)

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7, 8)		18		20		25	ns
tRAC	Access time from $\overline{RAS}$	(Note 7, 9)		55		65		75	ns
tAA	Column address access time	(Note 7, 10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40		45	ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 13, 14)

Read and Refresh Cycle

Symbol	Parameter	Limits						Unit
		M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	95		115		135		ns
tRAS	$\overline{RAS}$ low pulse width	55	10000	65	10000	75	10000	ns
tCAS	$\overline{CAS}$ low pulse width	18	10000	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	55		65		75		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	18		20		25		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		ns

Read-Write and Read-Modify-Write Cycle

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 20)	113		135		160		ns
tRAS	$\overline{RAS}$ low pulse width		73	10000	85	10000	100	10000	ns
tCAS	$\overline{CAS}$ low pulse width		36	10000	40	10000	50	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		73		85		100		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		36		40		50		ns
tCWD	Delay time, $\overline{CAS}$ low $\overline{W}$ low	(Note 21)	18		20		25		ns
tRWD	Delay time, $\overline{RAS}$ low $\overline{W}$ low	(Note 21)	55		65		75		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 21)	30		35		40		ns

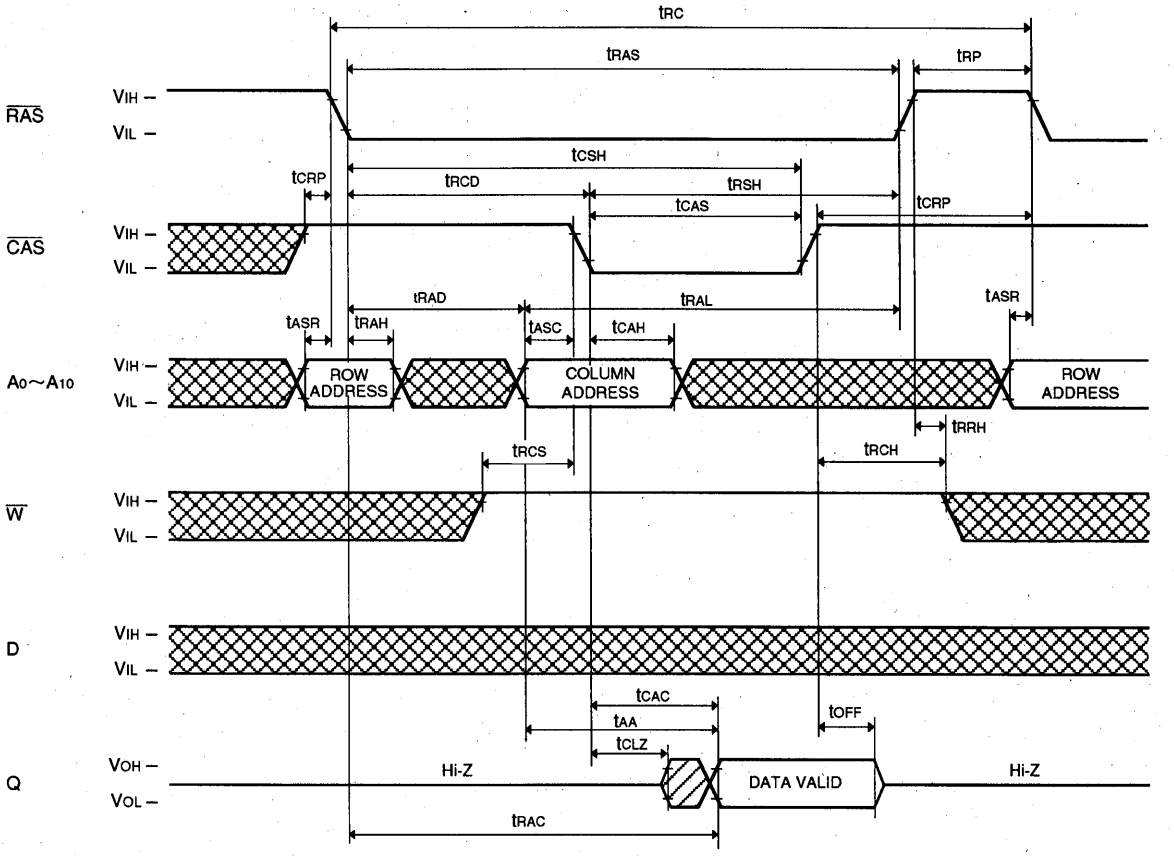
Fast page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter		Limits						Unit
			M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		40		45		50		ns
tPRWC	Fast page mode read write/read modify write cycle time		58		65		75		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle	(Note 23)	95	200000	110	200000	125	200000	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		45		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 21)	35		40		45		ns

Test Mode Set Cycle

Symbol	Parameter	Limits						Unit
		M5M44100C-5,-5S		M5M44100C-6,-6S		M5M44100C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	Write setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	Write hold time after $\overline{RAS}$ low	10		10		15		ns

Timing Diagrams (Note 28)
Read Cycle

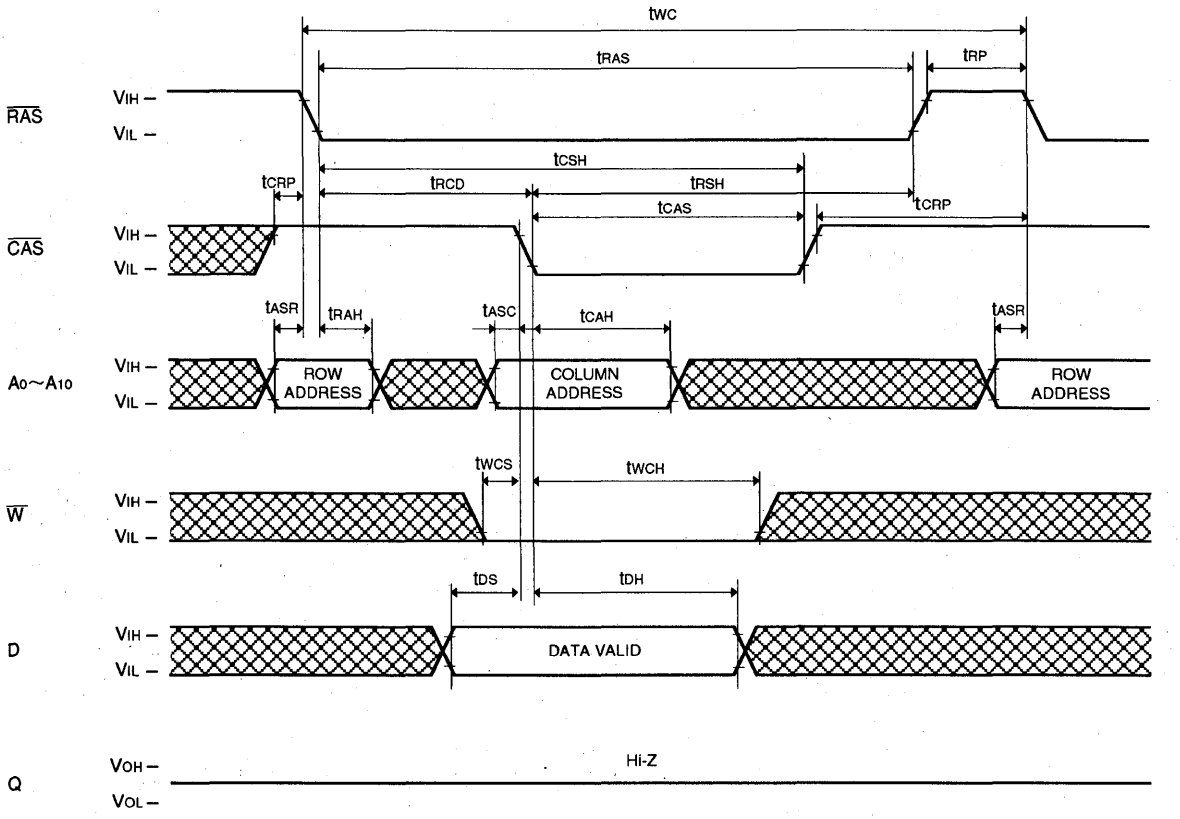


Note 28

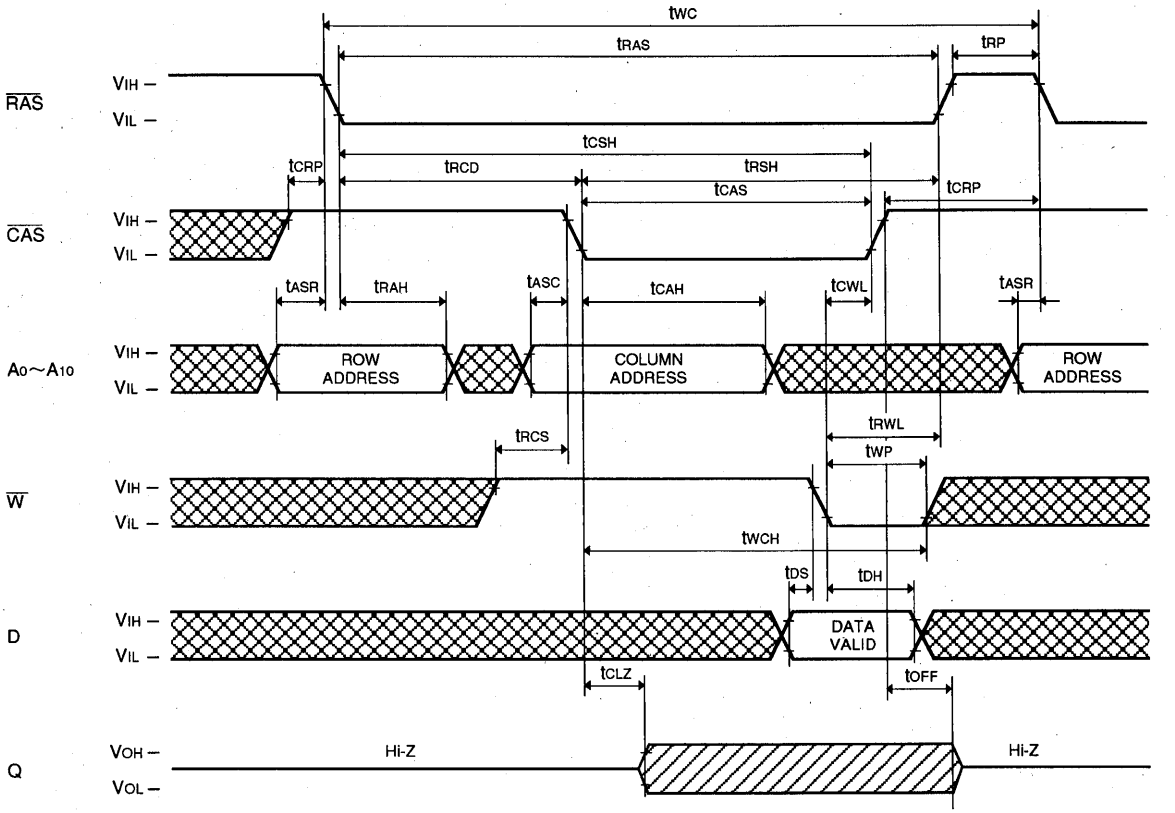
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

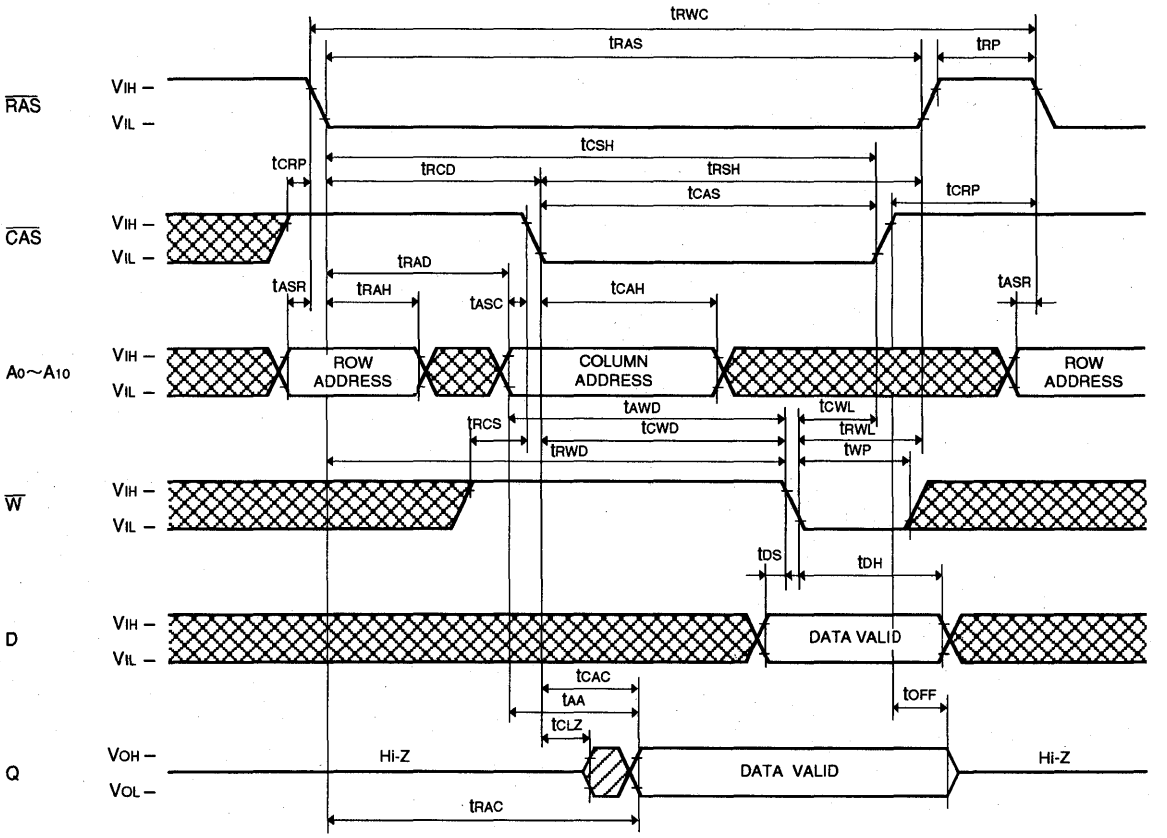
Write Cycle (Early write)



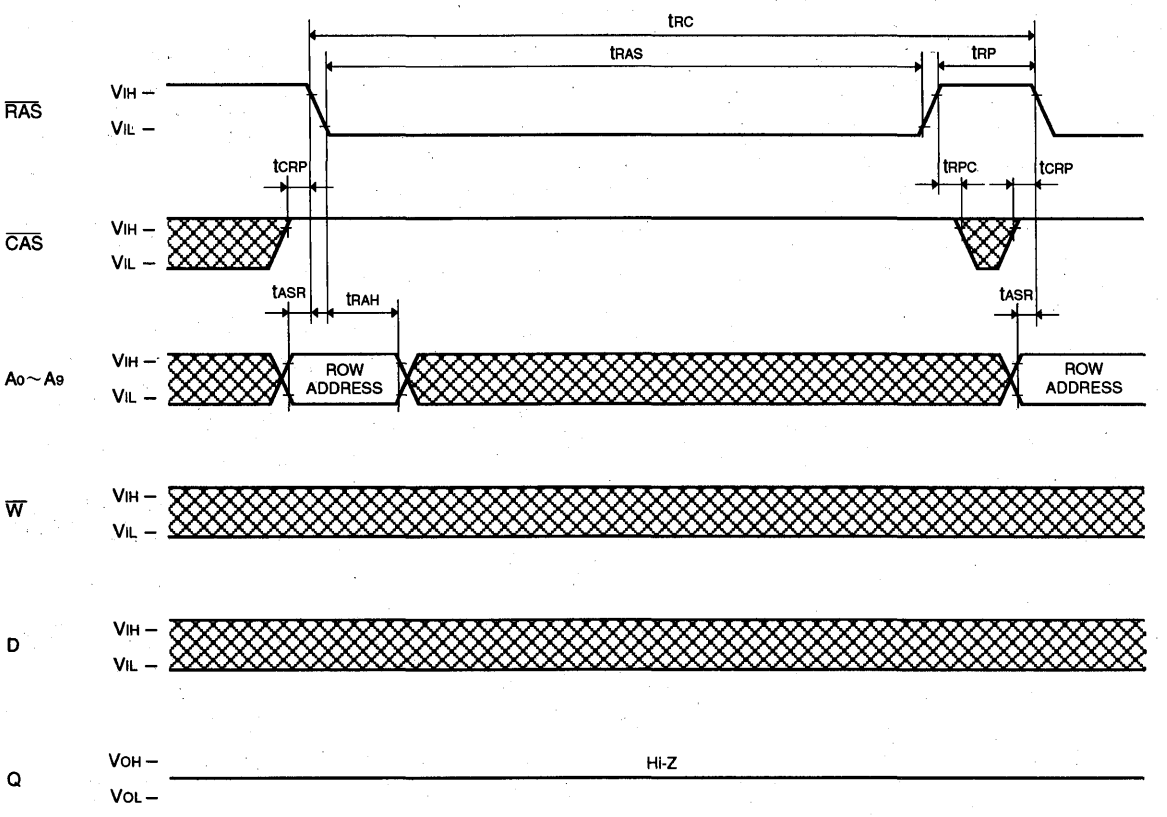
Write Cycle (Delayed write)



Read-Write, Read-Modify-Write Cycle

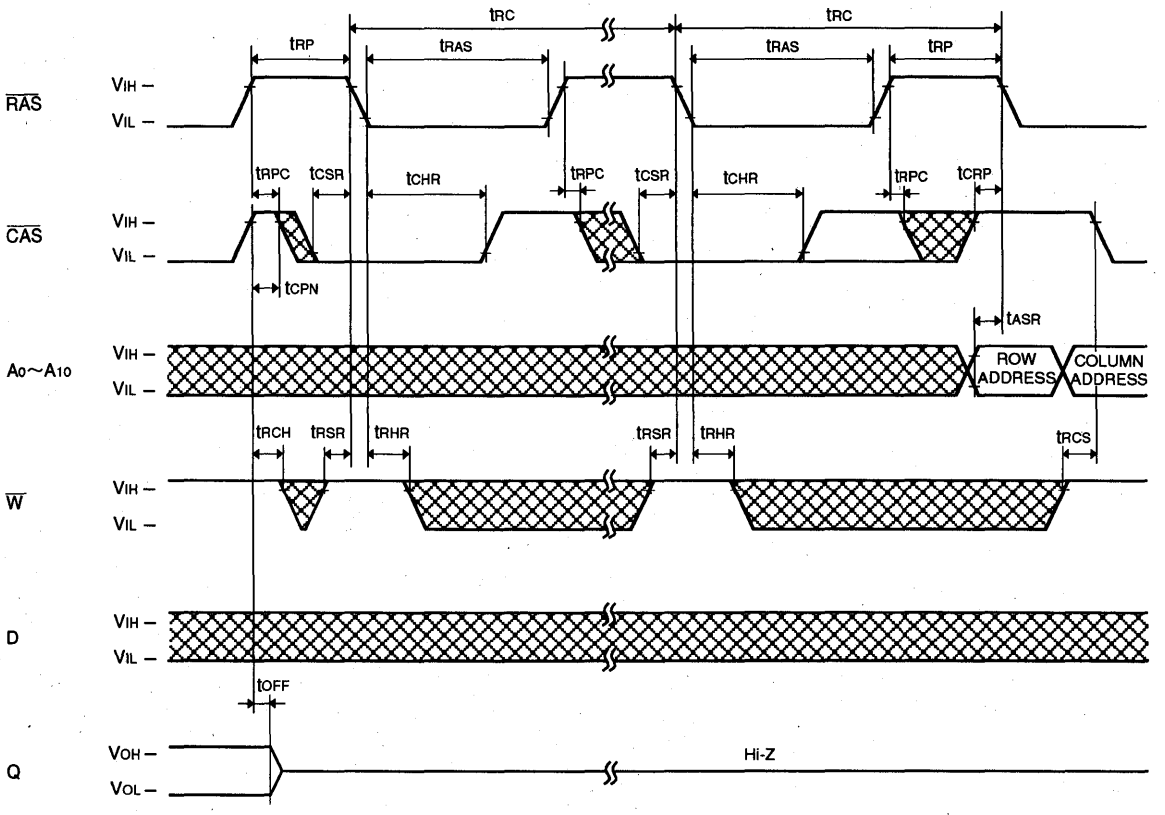


$\overline{RAS}$-only Refresh Cycle (Note 29)

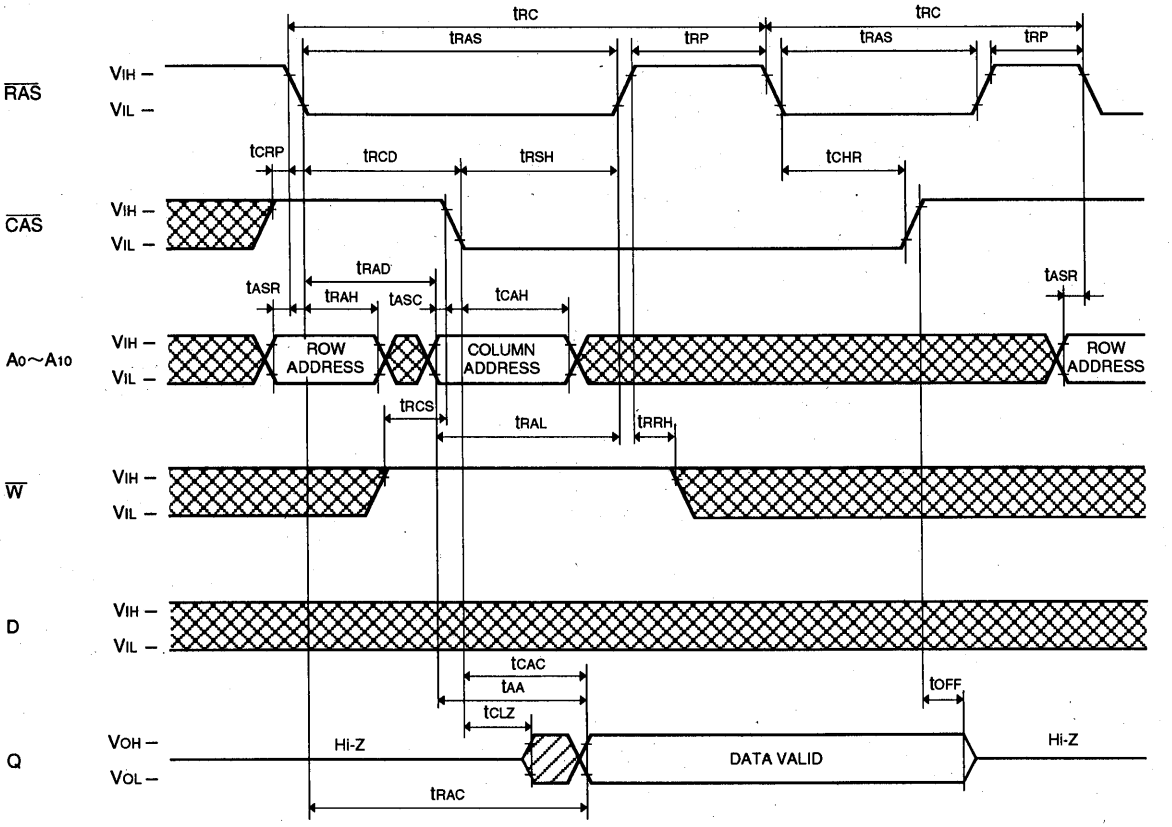


Note 29 : A10 may be VIH or VIL. Refresh address : A0(ROW)~A9(ROW)

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

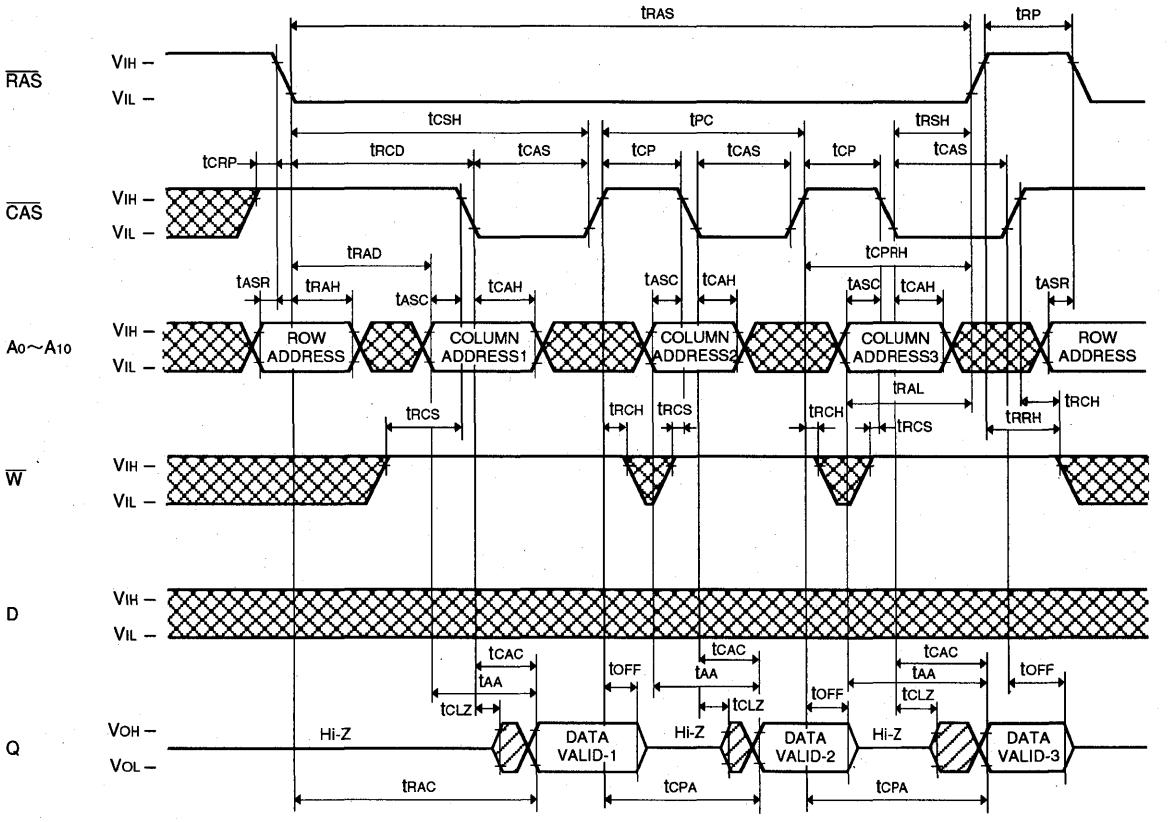


Hidden Refresh Cycle (Read) (Note 30)

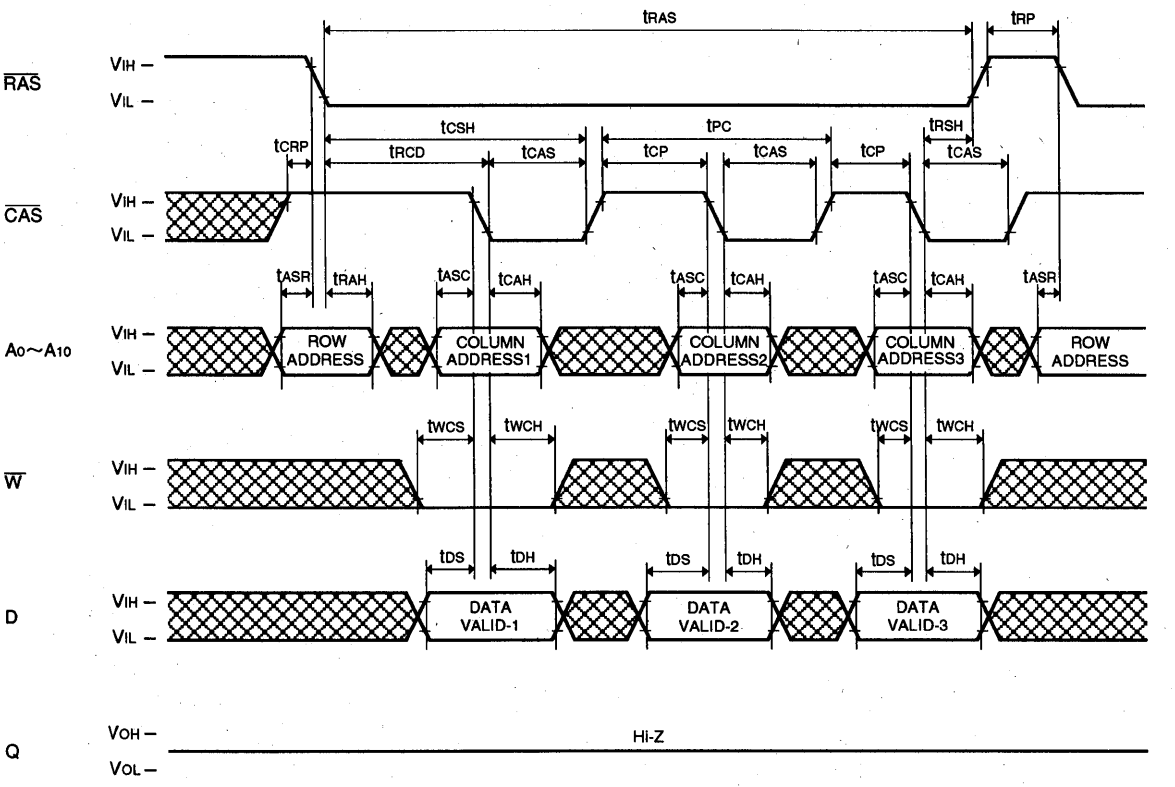


Note 30 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

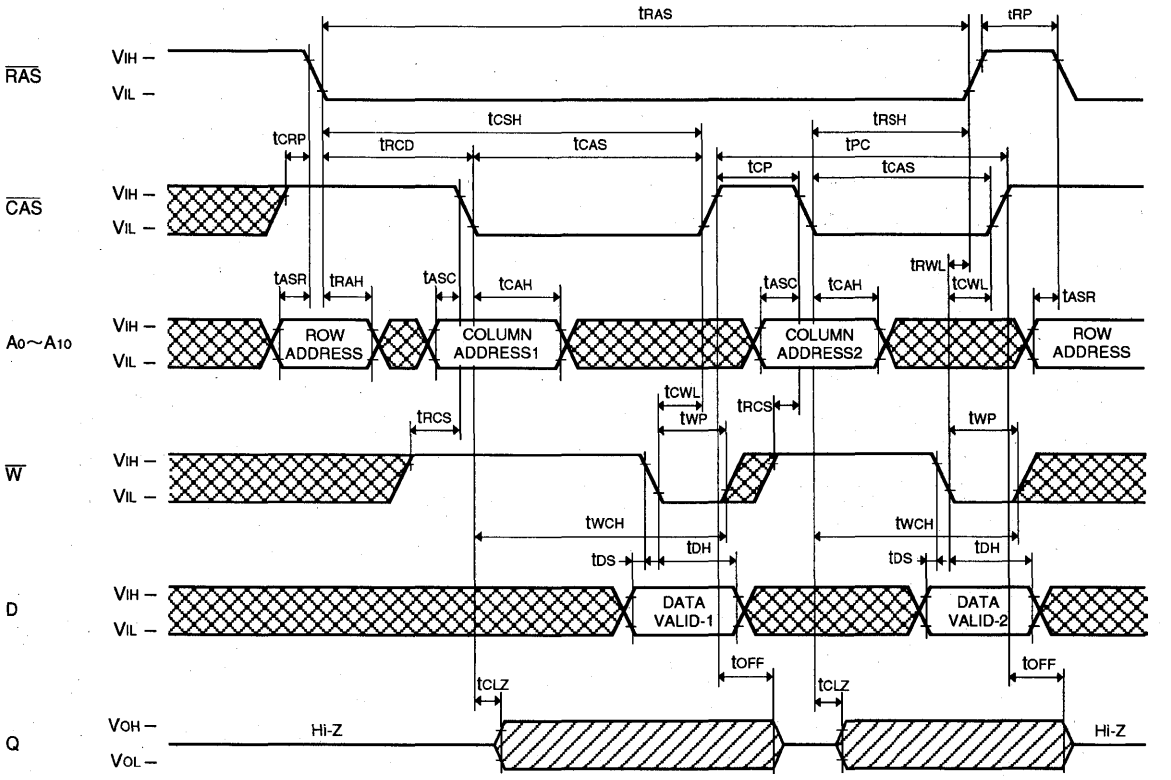
Fast Page Mode Read Cycle



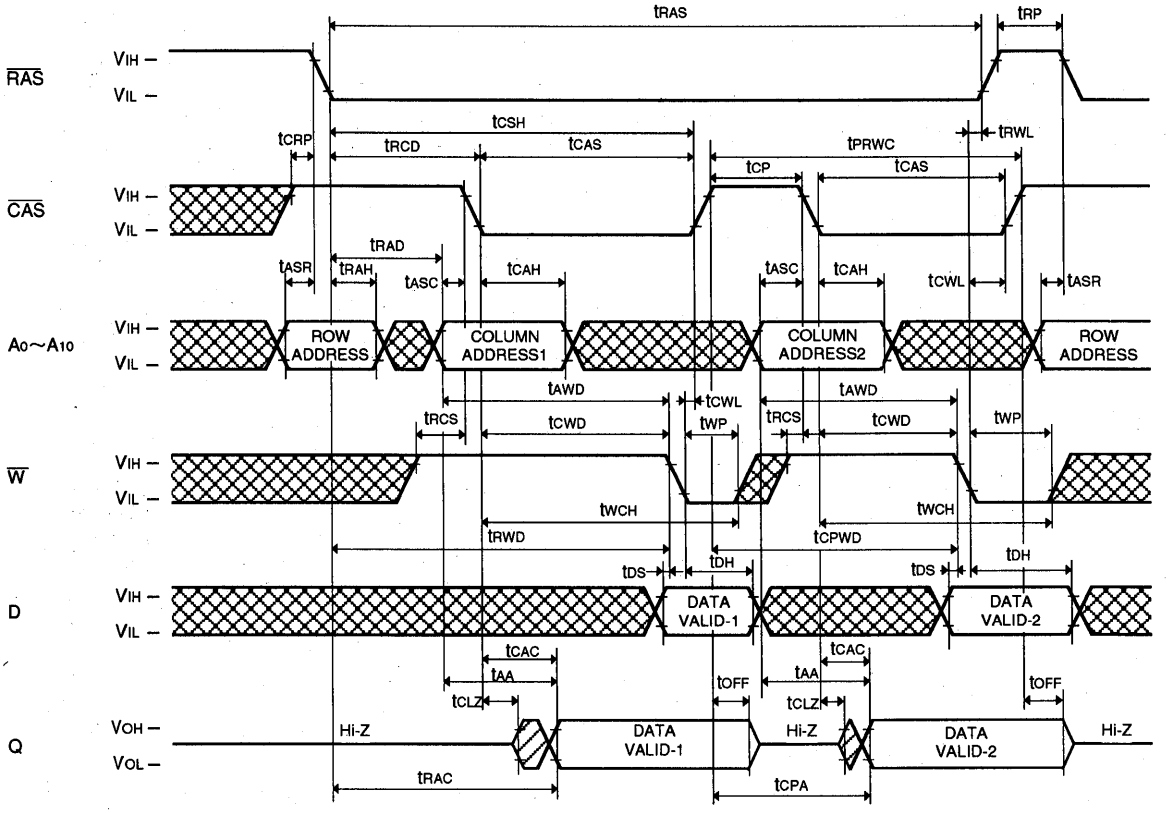
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



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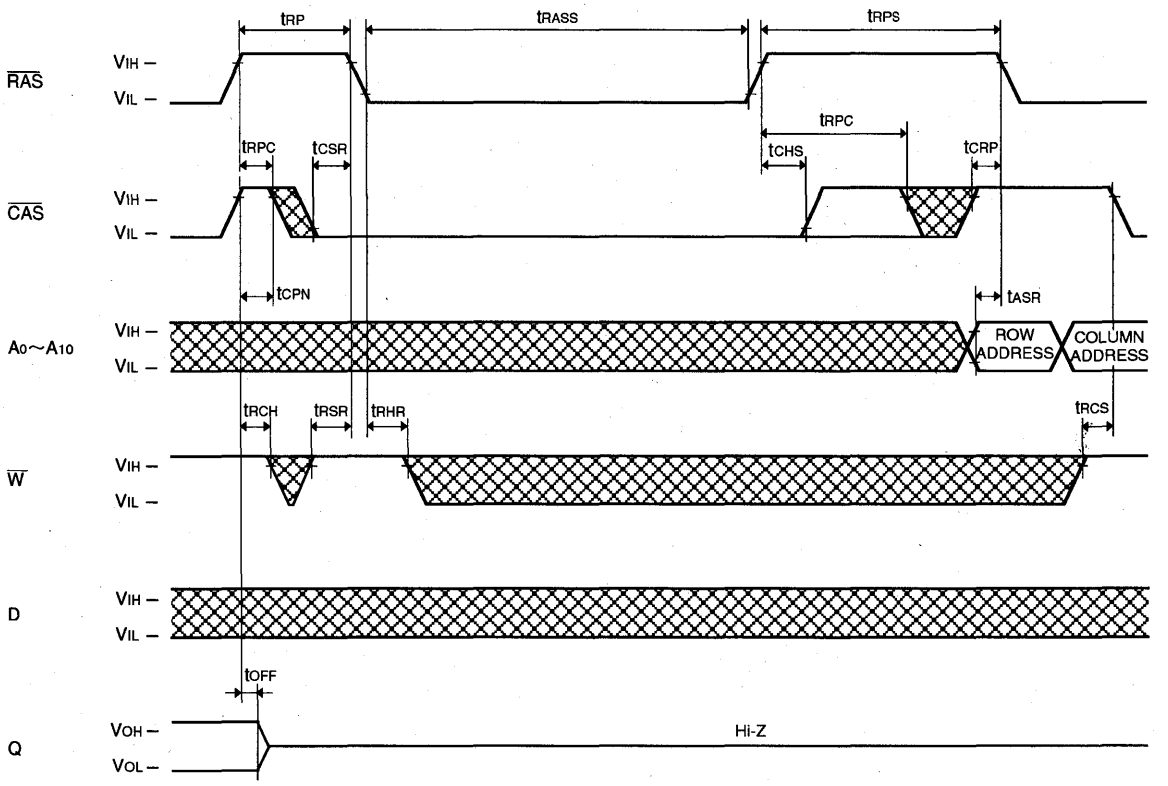
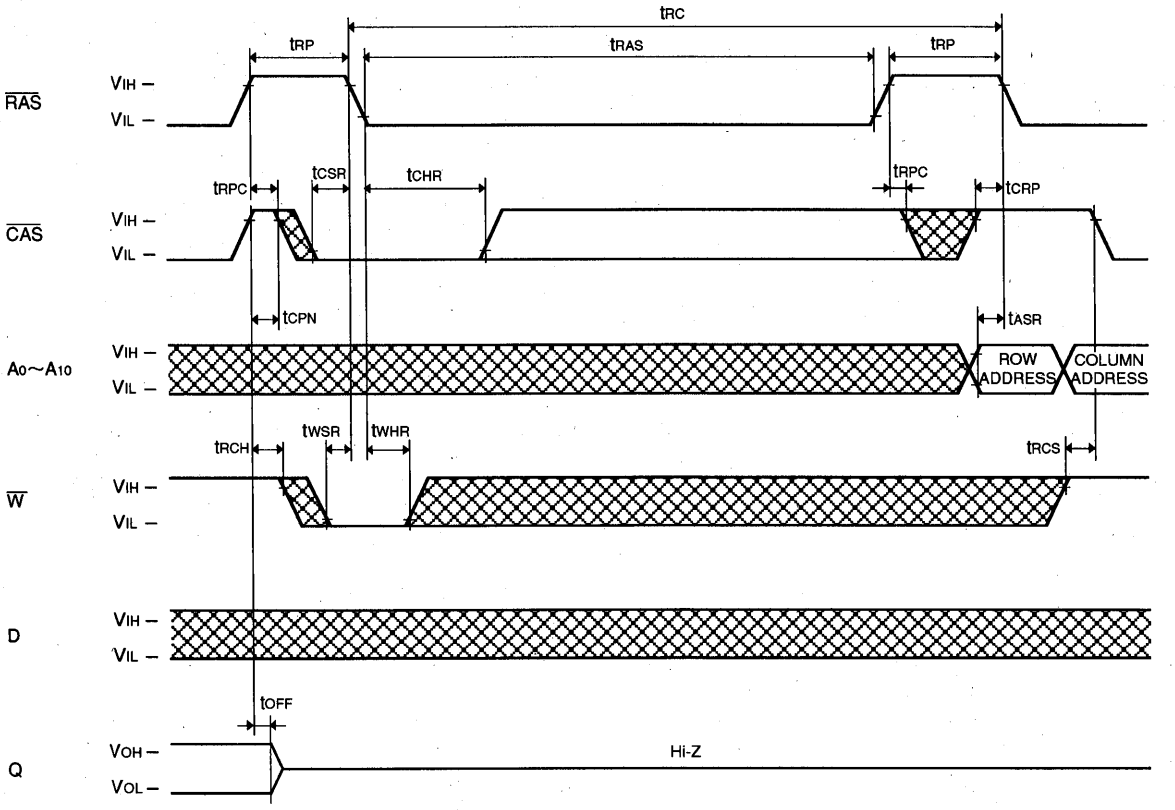
Self Refresh Cycle* (Note 26)



Test Mode Set Cycle (Note 31)



Note 31: The cycle is also available for the initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$(CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (256k-bytes deep) for each DQ (input/output) port.
No addressing of A10 (both row and column) and A0, A1 (column only) is required.
During a write cycle, data on the input pin is written in parallel into all 16-bits.
During a read cycle, the each output pin indicates a HIGH state if all 16-bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

Note 26:Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing diagram

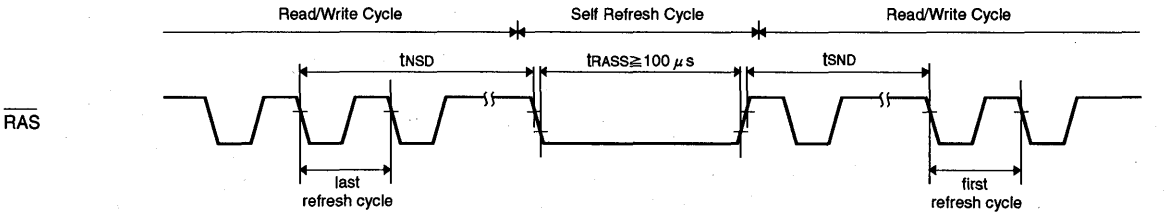
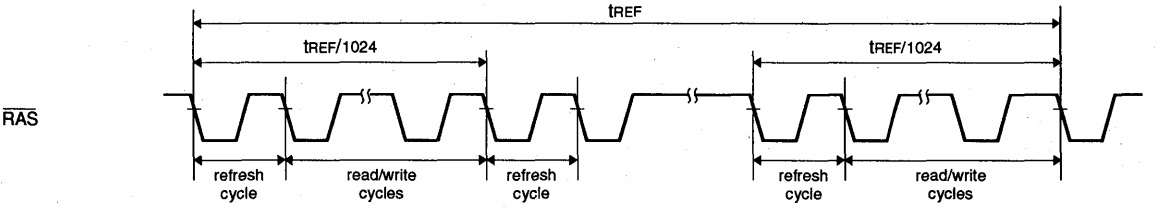


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} \leqq 125\ \mu s$	$t_{SND} \leqq 125\ \mu s$
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max.) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of row address signals ($A_0 \sim A_9$) are selected during 1024 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation

(A) Timing diagram

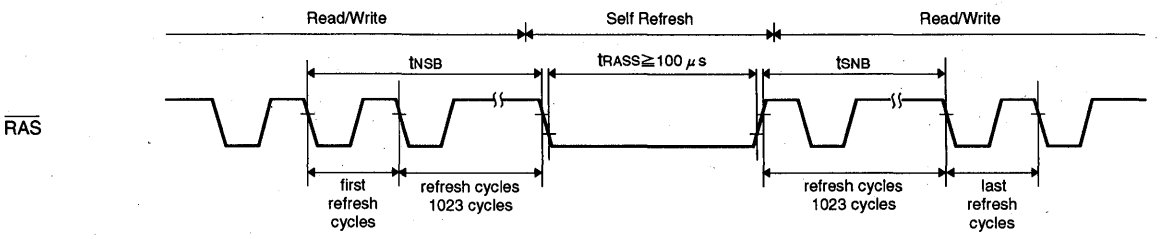
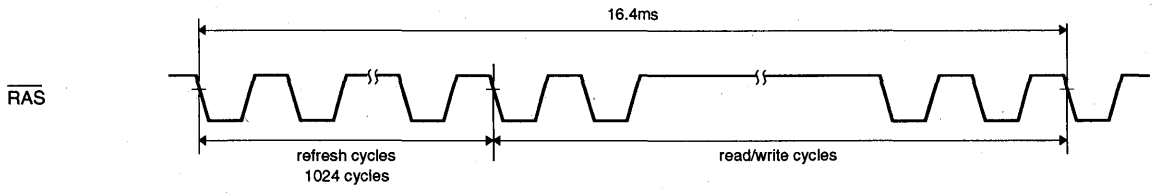


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	tNSB≦16.4ms	tSNB≦16.4ms
RAS only burst refresh	tNSB+tSNB≦16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of RAS only burst refresh

All combination of row address signals (A_0~A_9) are selected during 1024 continuous RAS only refresh cycles within 16.4ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation.
  The time interval tNSB from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation.
  The time interval tSNB from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 RAS only burst refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read / write operation.
  The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

M5M44400BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access (max. ns)
M5M44400BXX-6,-6S	60	15	30
M5M44400BXX-7,-7S	70	20	35

Type name	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44400BXX-6,-6S	15	110	400
M5M44400BXX-7,-7S	20	130	350

XX = J, TP

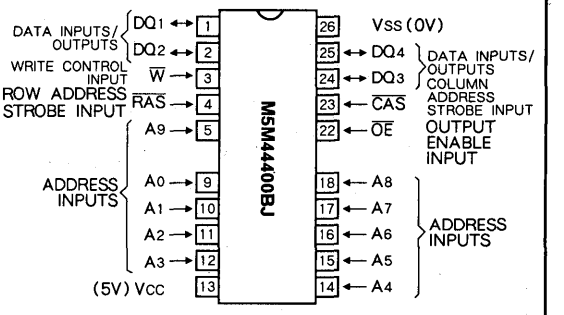
- Standard 26pin SOJ, 26pin TSOP (II)
- Single 5V ± 10% supply
- Low stand-by power dissipation
  - CMOS Input level ..... 5.5mW (max)
  - CMOS Input level ..... 0.55mW (max) *
- Low operating power dissipation
  - M5M44400BXX-6,-6S ..... 550.0mW (max)
  - M5M44400BXX-7,-7S ..... 467.5mW (max)
- Self refresh capability *
  - Self refresh current ..... 150 μA (max)
- Extended refresh capability
  - Extended refresh current ..... 150 μA (max)
- Fast-page mode (1024-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, CBR Self Refresh (-6S, -7S) capabilities.
- Early write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9) *
- 4-bit parallel test mode capability

* : Applicable to self refresh version (M5M44400BJ, TP -6S, -7S : option) only.

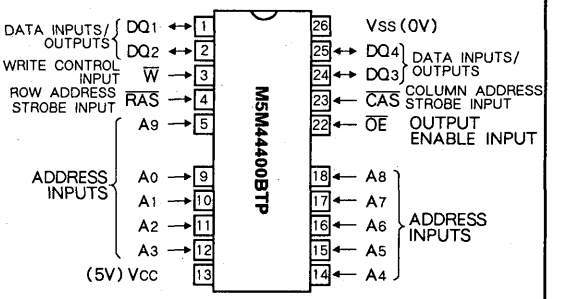
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TIO WIVEW)



Outline 26P0J (300mil SOJ)



Outline 26P3Z-E (TSOP)

FUNCTION

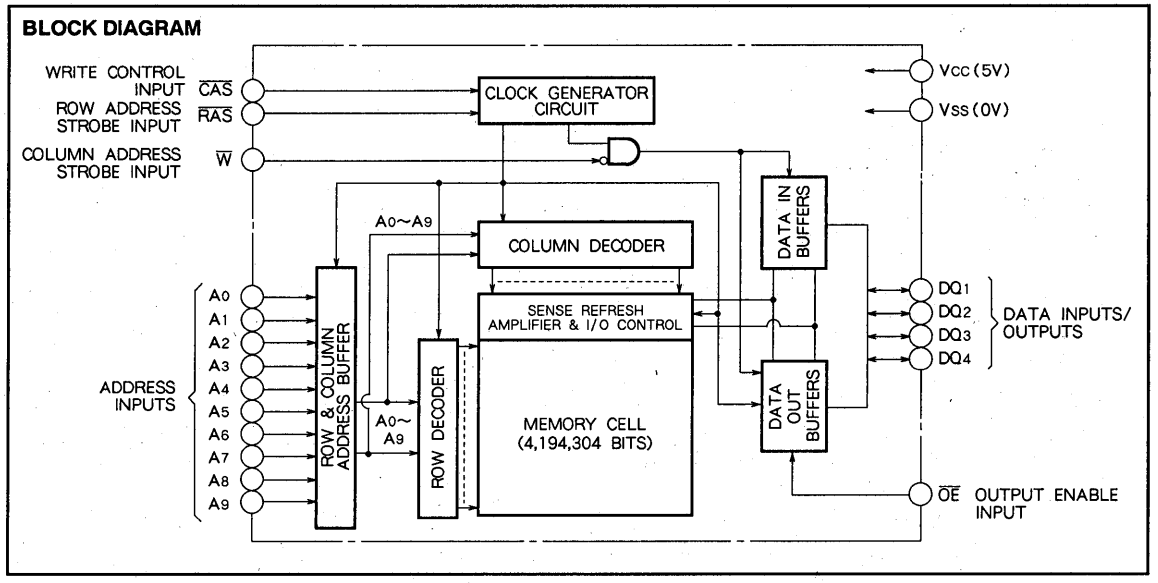
The M5M44400BJ,TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input condition for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input D	Output Q		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	
Write(Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	Fast page mode identical
Write(Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh(Extended*)	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self Refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low-level input voltage	DQ_1~DQ_4	−1.0		0.8	V
		Others	−2.0		0.8	

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, Other inputs pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4, 5)	M5M44400B-6, -6S	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{WC} = min., output open			100	mA
		M5M44400B-7, -7S				85	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 6)	M5M44400B	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
		M5M44400B(S)	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5, output open			1	
						0.1	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3, 5)	M5M44400B-6, -6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min., output open			100	mA
		M5M44400B-7, -7S				85	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Page-Mode (Note 3, 4, 5)	M5M44400B-6, -6S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{RC} = min, output open			100	mA
		M5M44400B-7, -7S				85	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400B-6, -6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{PC} = min., output open			85	mA
		M5M44400B-7, -7S				75	
$I_{CC8(AV)}$	Average supply current from V_{CC} Extended-Refresh cycle (Note 6)		Stand-by: $\overline{RAS}$ ≧ V_{CC} − 0.2V, $\overline{CAS}$ ≧ V_{CC} − 0.2V or $\overline{CAS}$ ≦ 0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$ ≦ 0.2V or ≧ V_{CC} − 0.2V $\overline{OE}$ ≦ 0.2V or ≧ V_{CC} − 0.2V A_0~A_9 ≦ 0.2V or ≧ V_{CC} − 0.2V DQ = open, t_{RC} = 125 μs t_{RAS} = t_{RAS} min~1 μs			150	μA
$I_{CC9(AV)}$	Average supply current from V_{CC} Self-Refresh cycle (Note 6)	M5M44400B(S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			150	μA

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44400BJ,TP	V_I = Vss f = 1MHz V_I = 25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	M5M44400BJ,TP				7	pF
$C_{I/O}$	Input/Output capacitance, data ports	M5M44400BJ,TP				7	pF

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44400B-6, -6S		M5M44400B-7, -7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7, 8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7, 9)		60		70	ns
tAA	Column Address access time	(Note 7, 10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tCLZ	Output low impedance from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	20	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	ns

Note 6. An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max).
9. Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD or tRAD exceeds the value shown.
10. Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).
11. Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).
12. tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT ≦ | ± 10 μA |) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44400B-6, -6S		M5M44400B-7, -7S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time	M5M44400B		16.4		16.4	ms
		M5M44400B(S)		128		128	
t_{RP}	$\overline{RAS}$ high pulse width		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 19)	15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 19)	15		20		ns
t_T	Transition time	(Note 20)	1	50	1	50	ns

Note 13. The timing requirements are assumed t_T = 5ns.
14. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
15. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is less than t_{RCD}(max), access time is t_{RAC}.
If t_{RCD} is greater than t_{RCD}(max), access time is controlled exclusively by t_{CAC} or t_{AA}.
t_{RCD}(min) is specified as $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
16. t_{RAD}(max) is specified as a reference point only. If $t_{RAD} \geqq t_{RAD}$(max) and $t_{ASC} \leqq t_{ASC}$(max), access time is controlled exclusively by t_{AA}.
17. t_{ASC}(max) is specified as a reference point only. If $t_{RCD} \geqq t_{RCD}$(max) and $t_{ASC} \geqq t_{ASC}$(max), access time is controlled exclusively by t_{CAC}.
18. Either t_{DZC} or t_{DZO} must be satisfied.
19. Either t_{CDD} or t_{ODD} must be satisfied.
20. t_T is measured between V_{IH}(min) and V_{IL}(max).

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7-7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 21. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7,-7S		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
tWP	Write pulse width	10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
tRWC	Read Write/read modify write cycle time (Note 22)	150		175		ns
tRAS	$\overline{RAS}$ low pulse width	95	10000	115	10000	ns
tCAS	$\overline{CAS}$ low pulse width	50	10000	65	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		115		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		65		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	35		40		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	80		90		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	50		55		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
tWP	Write pulse width	10		15		ns
tDS	Data setup time before $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		ns

Note 22. t_{RWC} is specified as $t_{RWC}(min) = t_{RAC}(max) + t_{ODD}(min) + t_{RWL}(min) + t_{RP}(min) + 4t_T$.
23. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$, and $t_{CPWD} \geq t_{CPWD}(min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		ns
tPRWC	Fast Page mode read write/read modify write cycle time	75		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	100	100000	115	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	35		40		ns

Note 24. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25. $t_{RAS}(min)$ is specified as two cycles of $\overline{CAS}$ input are performed.
26. $t_{CP}(max)$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh*Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		ns

Note 27. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits				Unit
		M5M44400B-6S		M5M44400B-7S		
		Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Test Mode Specification (Note 28)
ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4, 5)	M5M44400B-6, -6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			115	mA
		M5M44400B-7, -7S				100	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3, 5)	M5M44400B-6, -6S	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}, t_{RC} = min. output open			115	mA
		M5M44400B-7, -7S				100	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4, 5)	M5M44400B-6, -6S	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min., output open			115	mA
		M5M44400B-7, -7S				100	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400B-6, -6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC} = min. output open			100	mA
		M5M44400B-7, -7S				85	

Note 28. All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44400B-6, -6S		M5M44400B-7, -7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7, 8)		20		25	ns
tRAC	Access time from $\overline{RAS}$	(Note 7, 9)		65		75	ns
tAA	Column Address access time	(Note 7, 10)		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		20		25	ns

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 13, 14)

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
tRC	Read cycle time	115		135		ns
tRAS	$\overline{RAS}$ low pulse width	65	10000	75	10000	ns
tCAS	$\overline{CAS}$ low pulse width	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	65		75		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		ns
tRAL	Column address to $\overline{RAS}$ hold time	35		40		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		25		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M44400B-6, -6S		M5M44400B-7, -7S		
			Min	Max	Min	Max	
tRWC	Read Write/read modify write cycle time	(Note 22)	155		180		ns
tRAS	$\overline{RAS}$ low pulse width		100	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		55	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		ns
tRSH	$\overline{RAS}$ hold time $\overline{CAS}$ low		55		70		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	55		60		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	45		50		ns
tPRWC	Fast page mode read write/read modify write cycle time	80		100		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	110	100000	125	100000	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	40		45		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	40		45		ns

Test Mode Set Cycle

Symbol	Parameter	Limits				Unit
		M5M44400B-6, -6S		M5M44400B-7, -7S		
		Min	Max	Min	Max	
tWSR	Write setup time before $\overline{RAS}$ low	10		10		ns
tWHR	Write hold time after $\overline{RAS}$ low	10		15		ns

Note 29. Self refresh sequence

Two refreshing ways shoud be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distriduted refresh during Read/Write operation

(A) Timing Diagrams

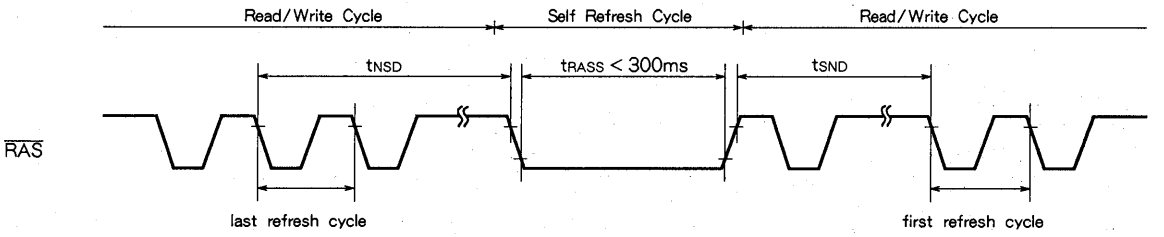


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of nine row address signals (A_0~A_8) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

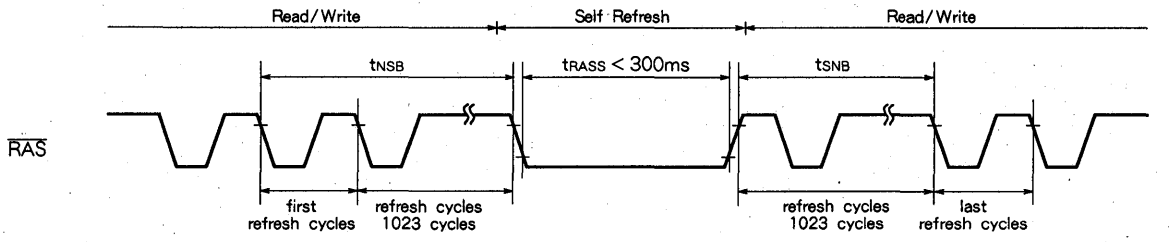


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

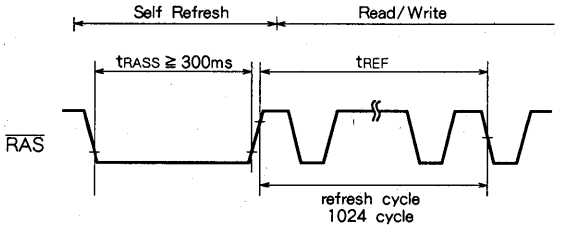


Table 4

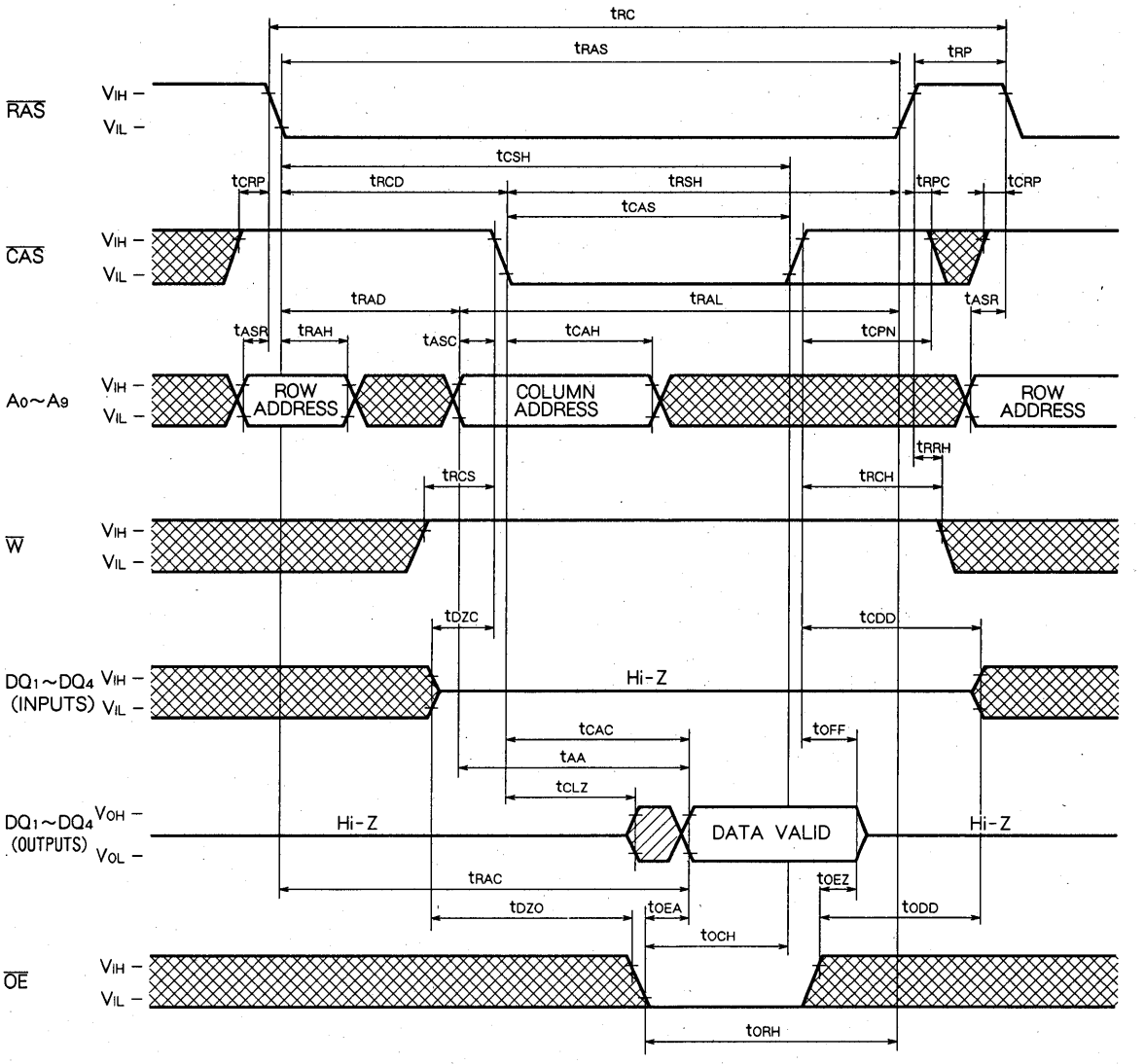
Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.

Timing Diagrams (Note 30)

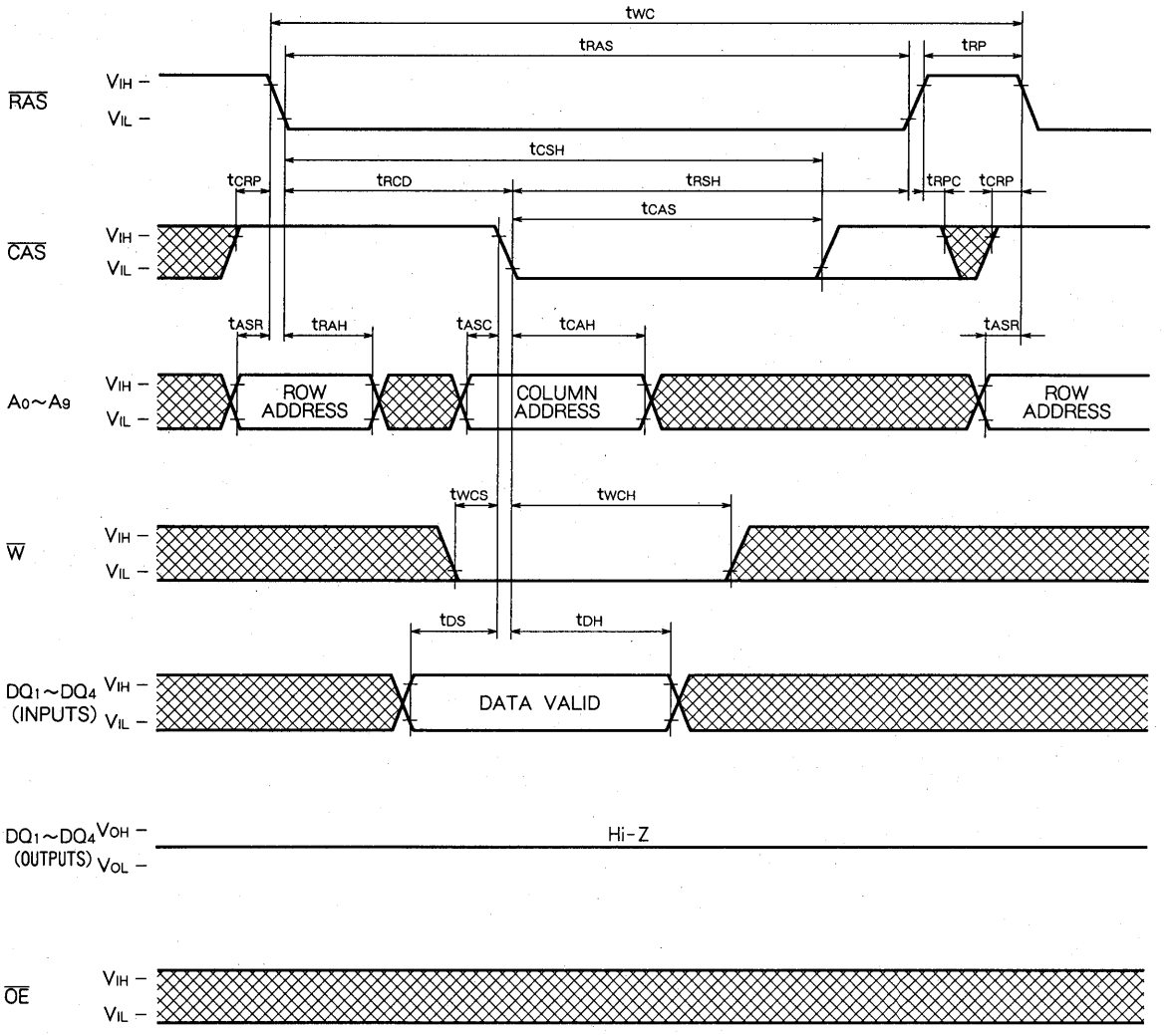
Read Cycle



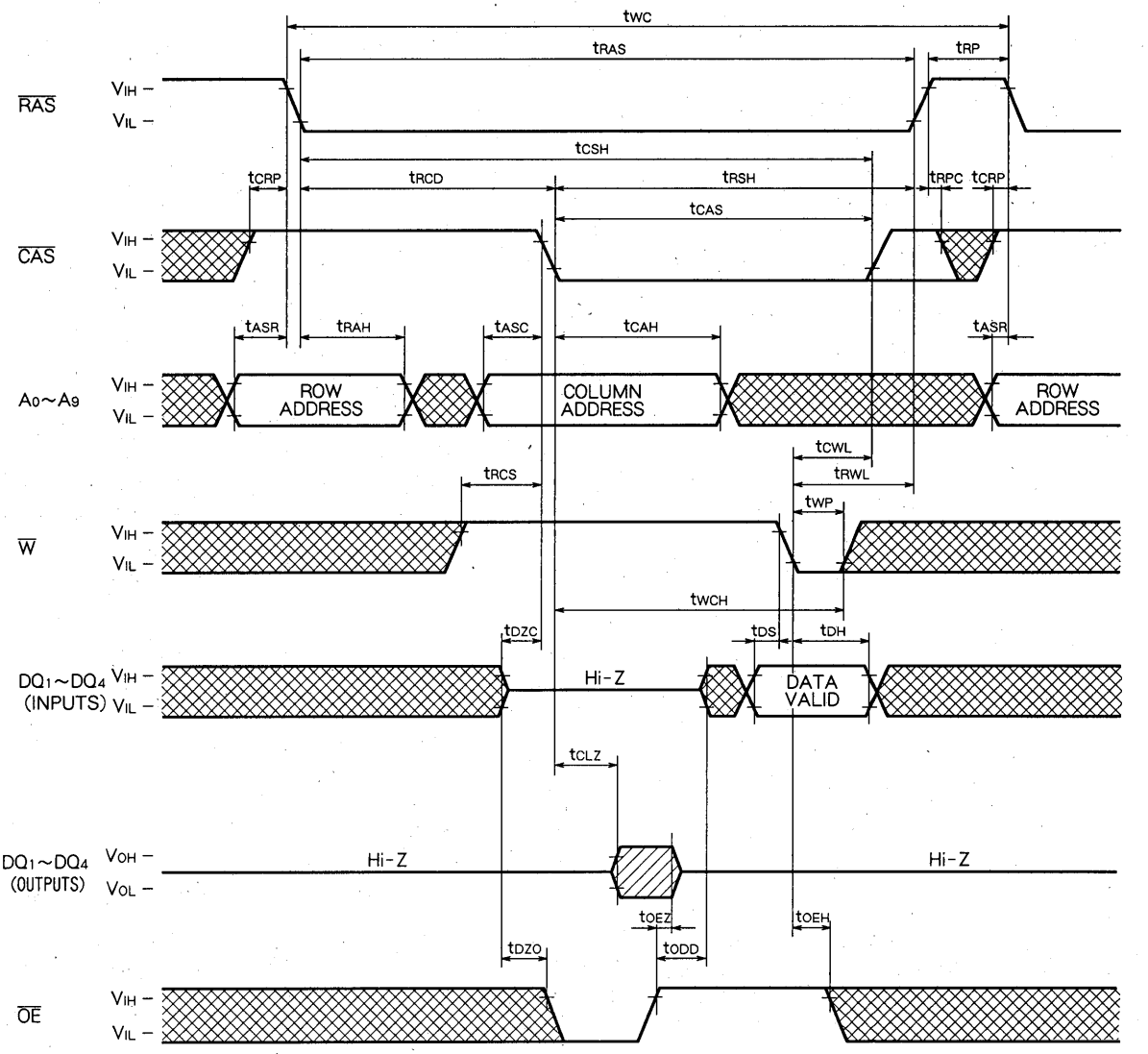
Note 30. Indicates the don't care input.
VIH (min) ≦ VIN ≦ VIH (max) or VIL (min) ≦ VIN ≦ VIL (max)

Indicates the invalid output.

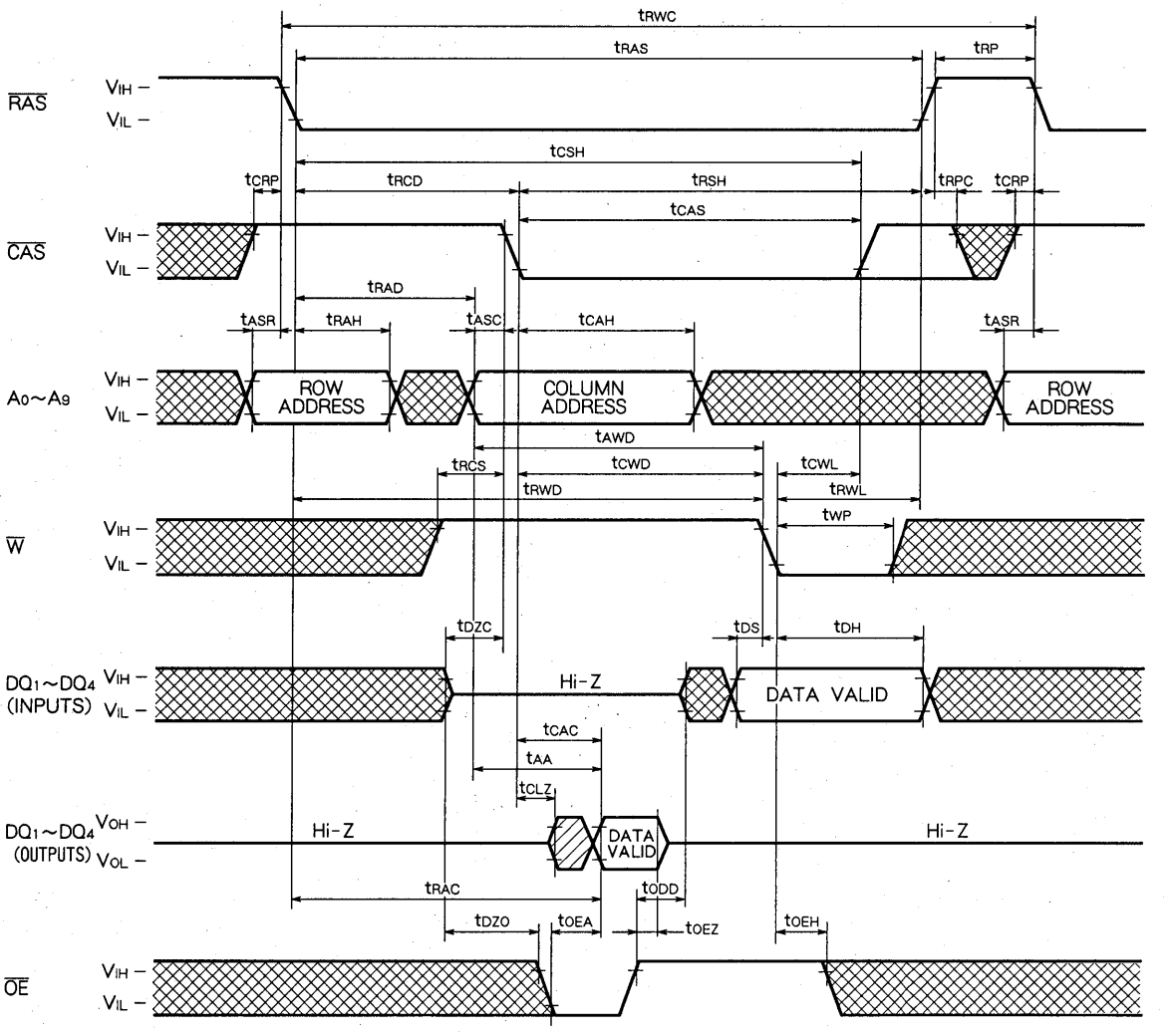
Write Cycle (Early write)



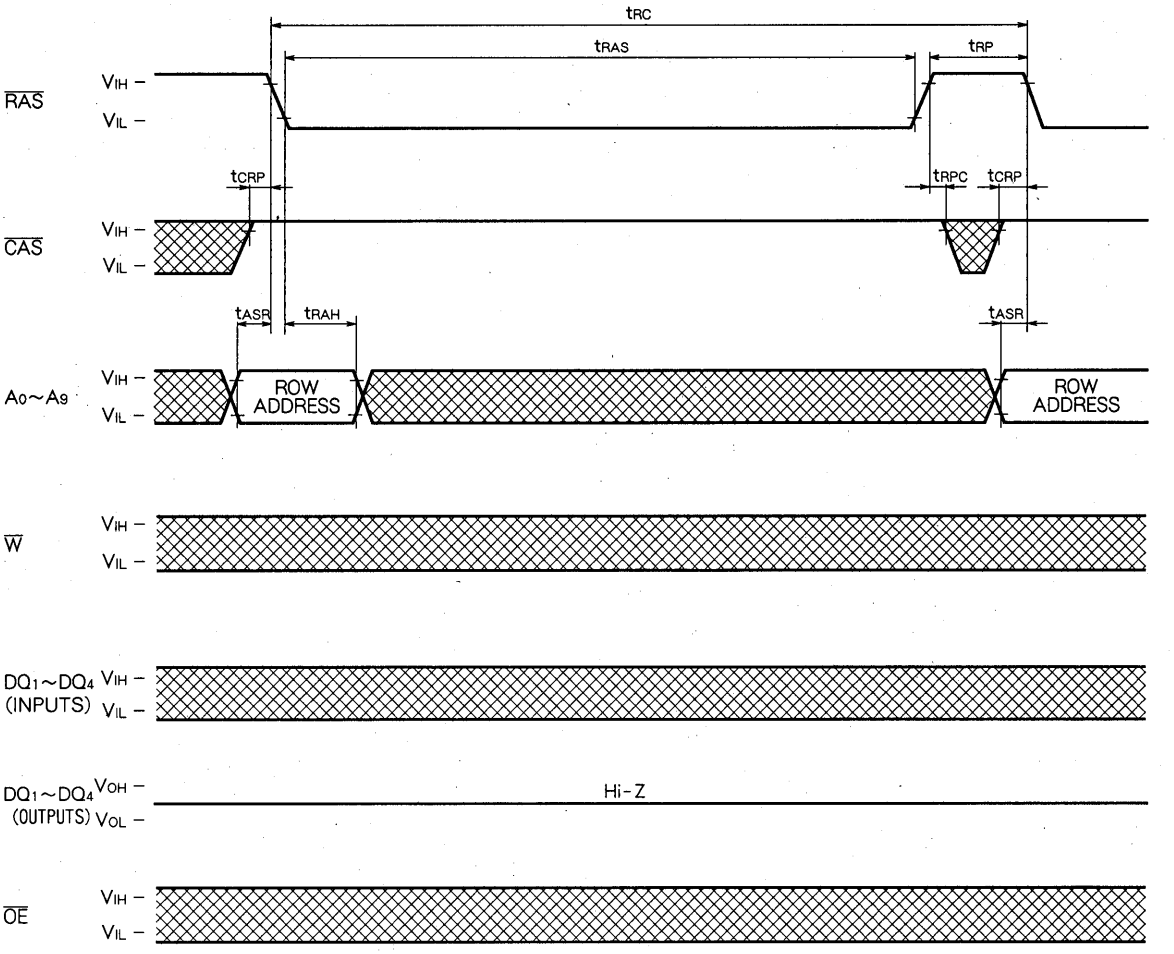
Write Cycle (Delayed Write)



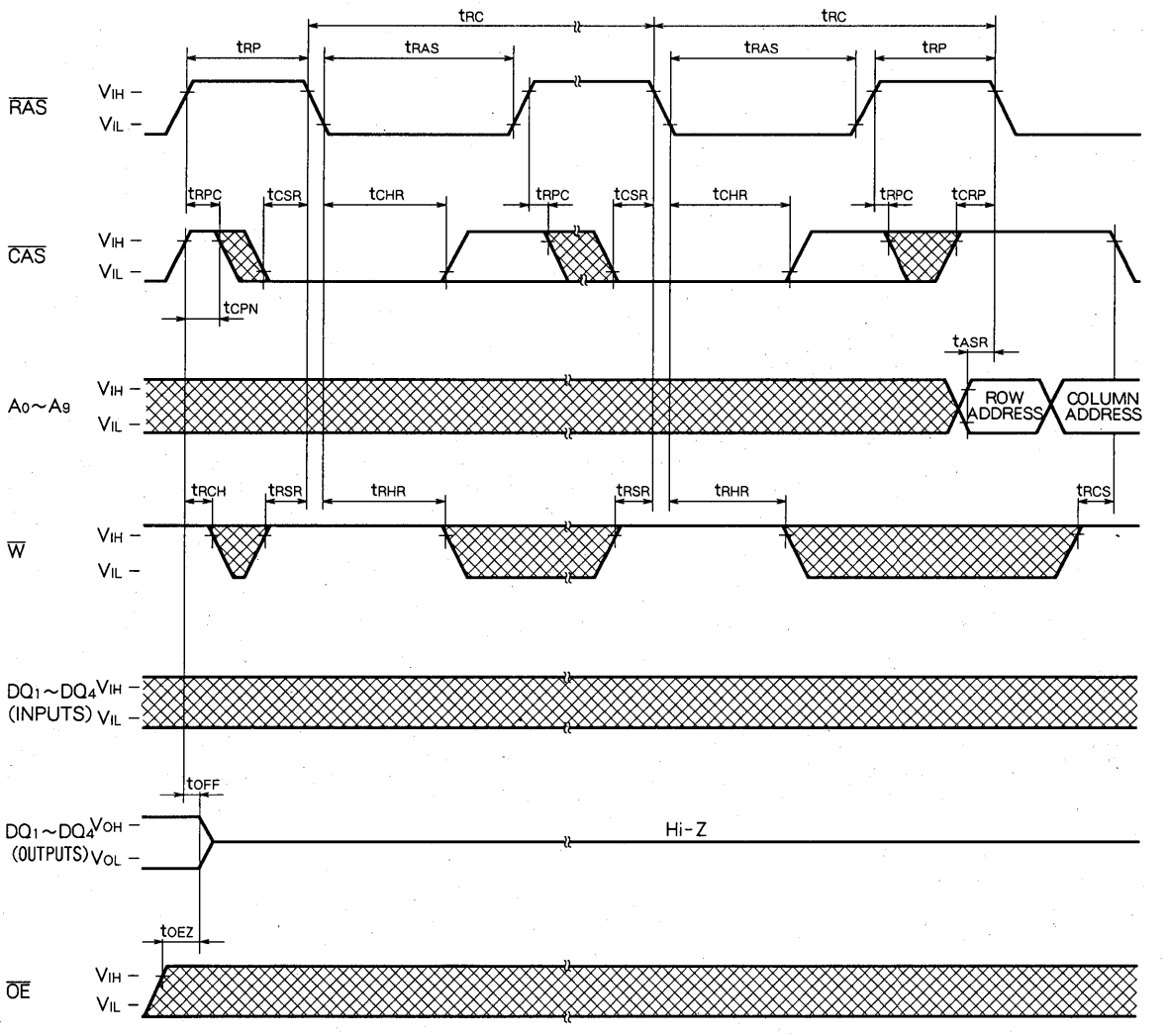
Read-Write, Read-Modify-Write Cycle



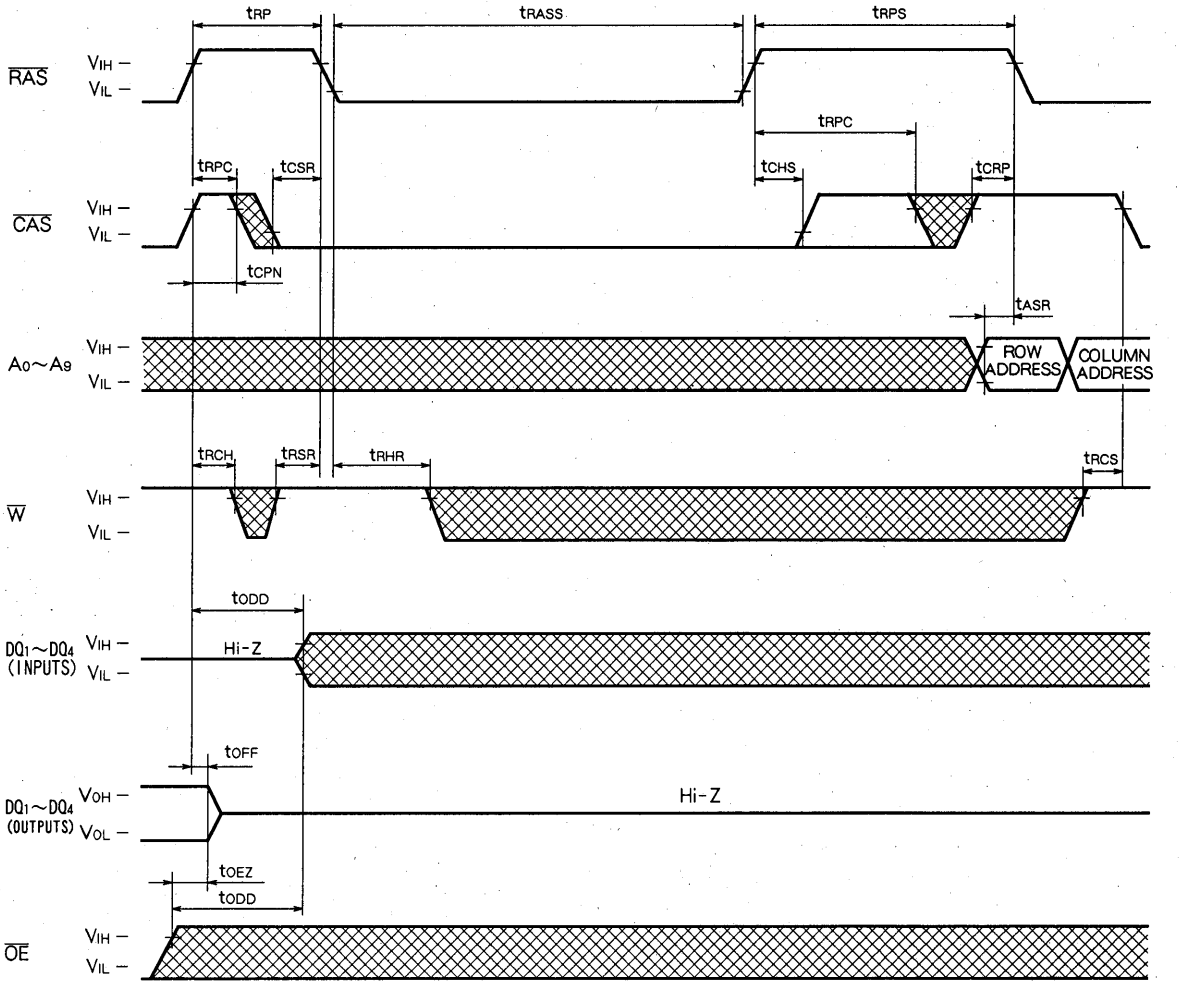
$\overline{RAS}$-only Refresh Cycle



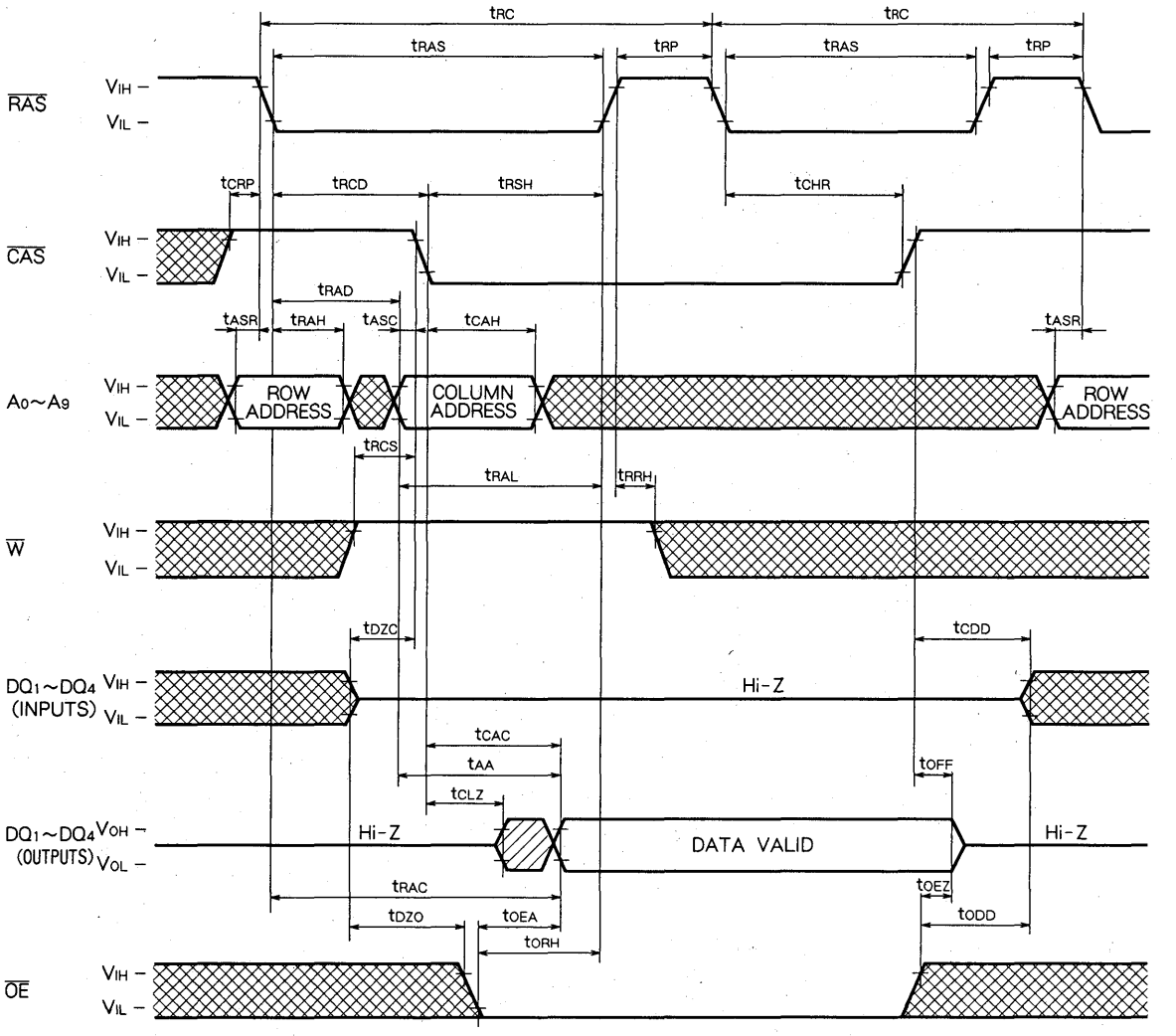
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



Self Refresh Cycle* (Note 29)

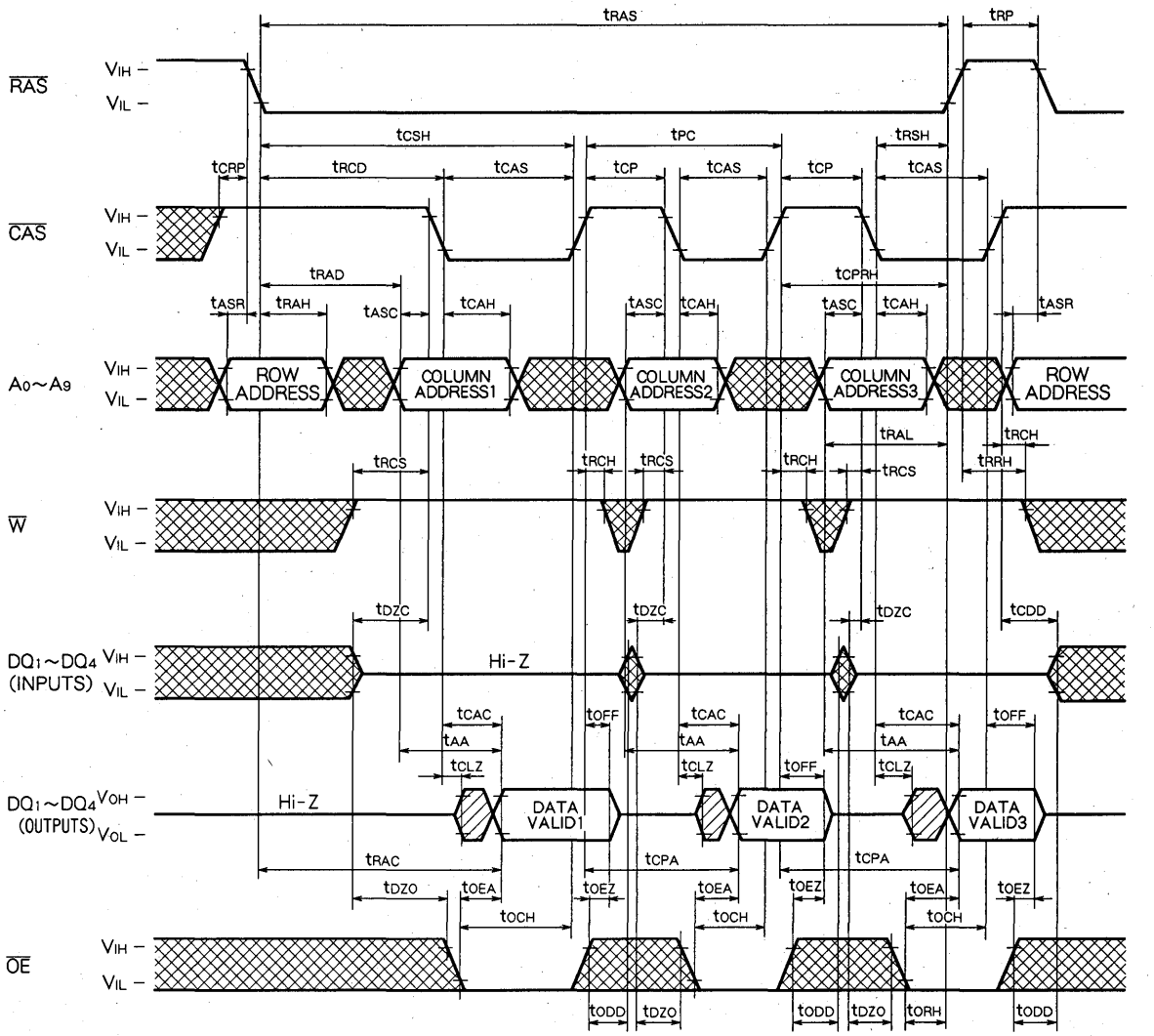


Hidden Refresh Cycle (Read) (Note 31)



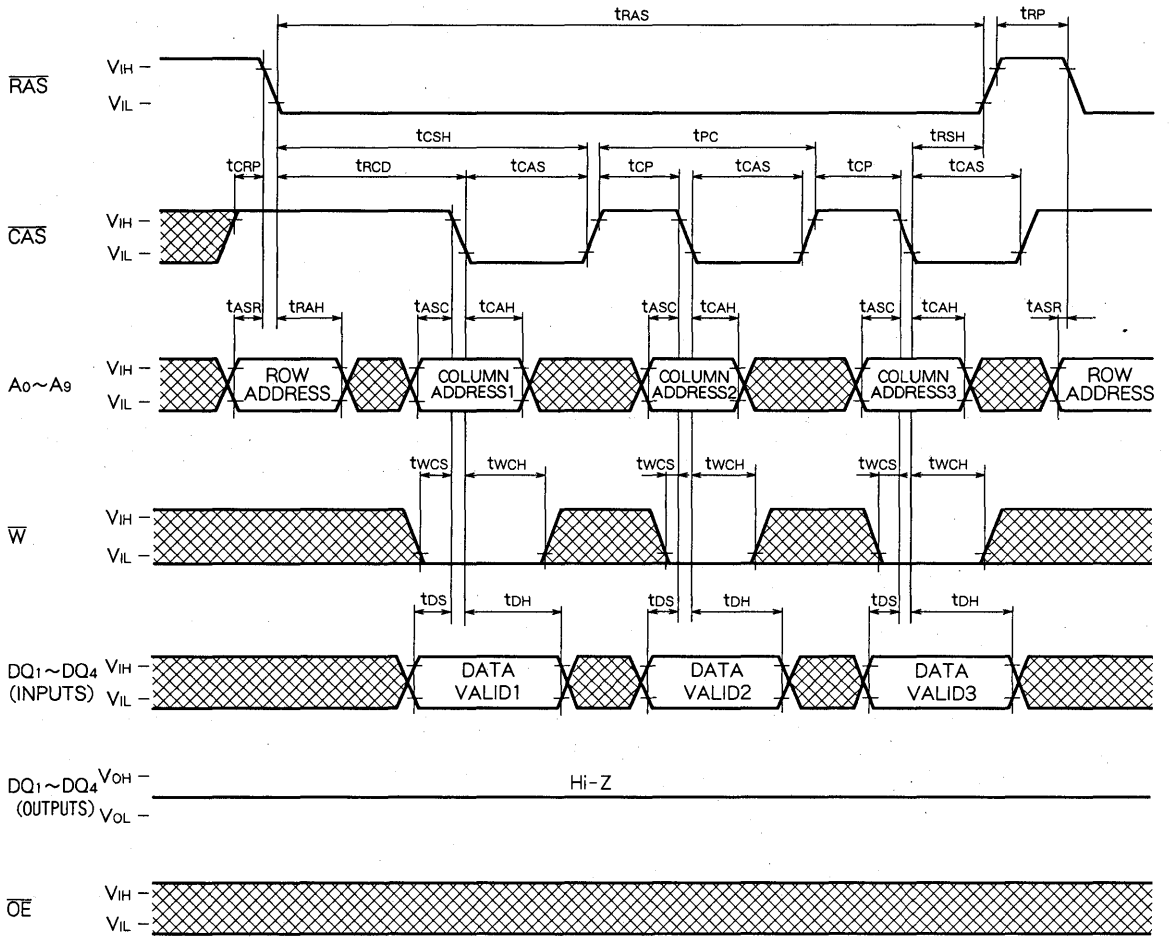
Note 31. Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle

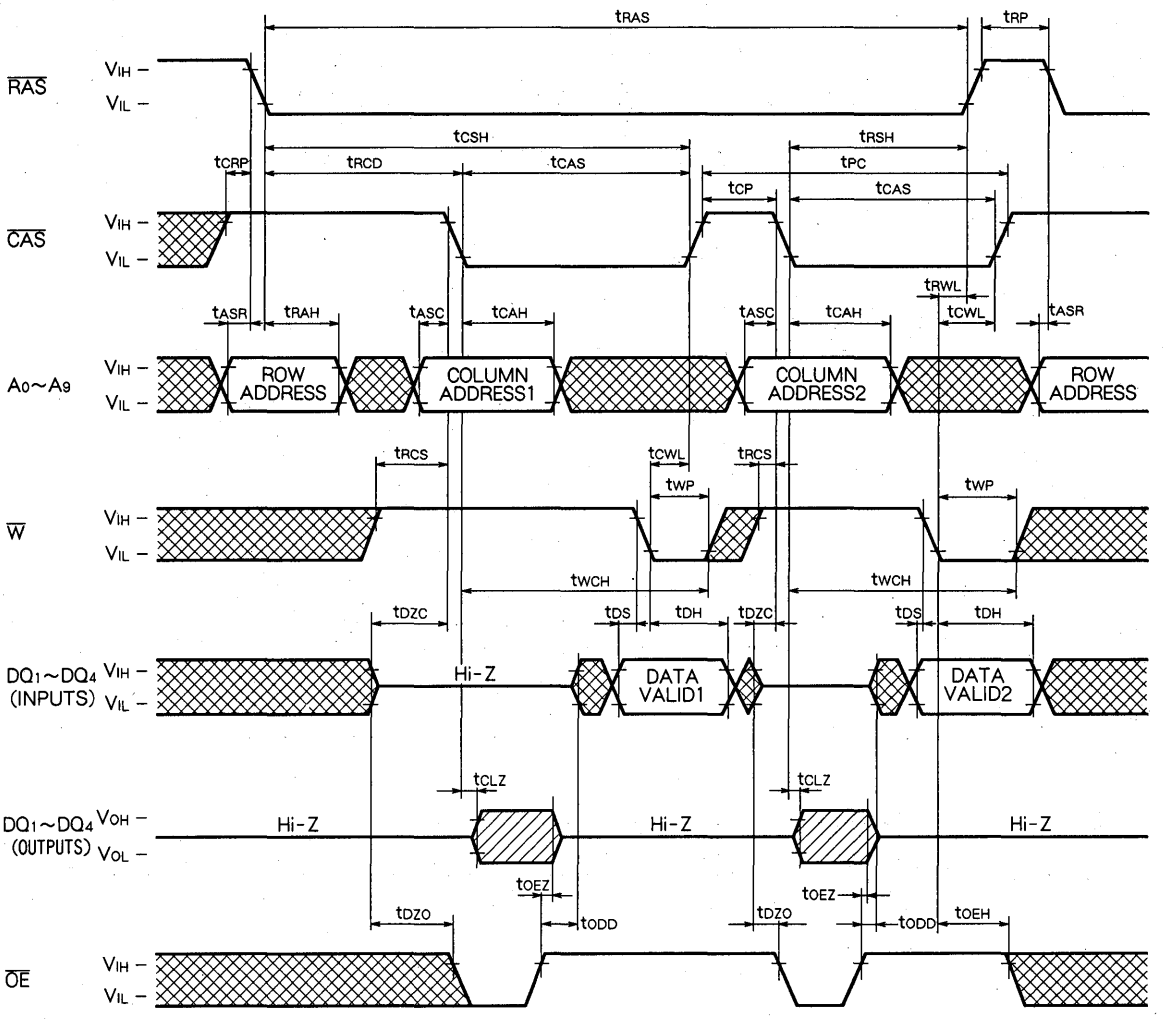


MITSUBISHI ELECTRIC

Fast Page Mode Write Cycle (Early Write)

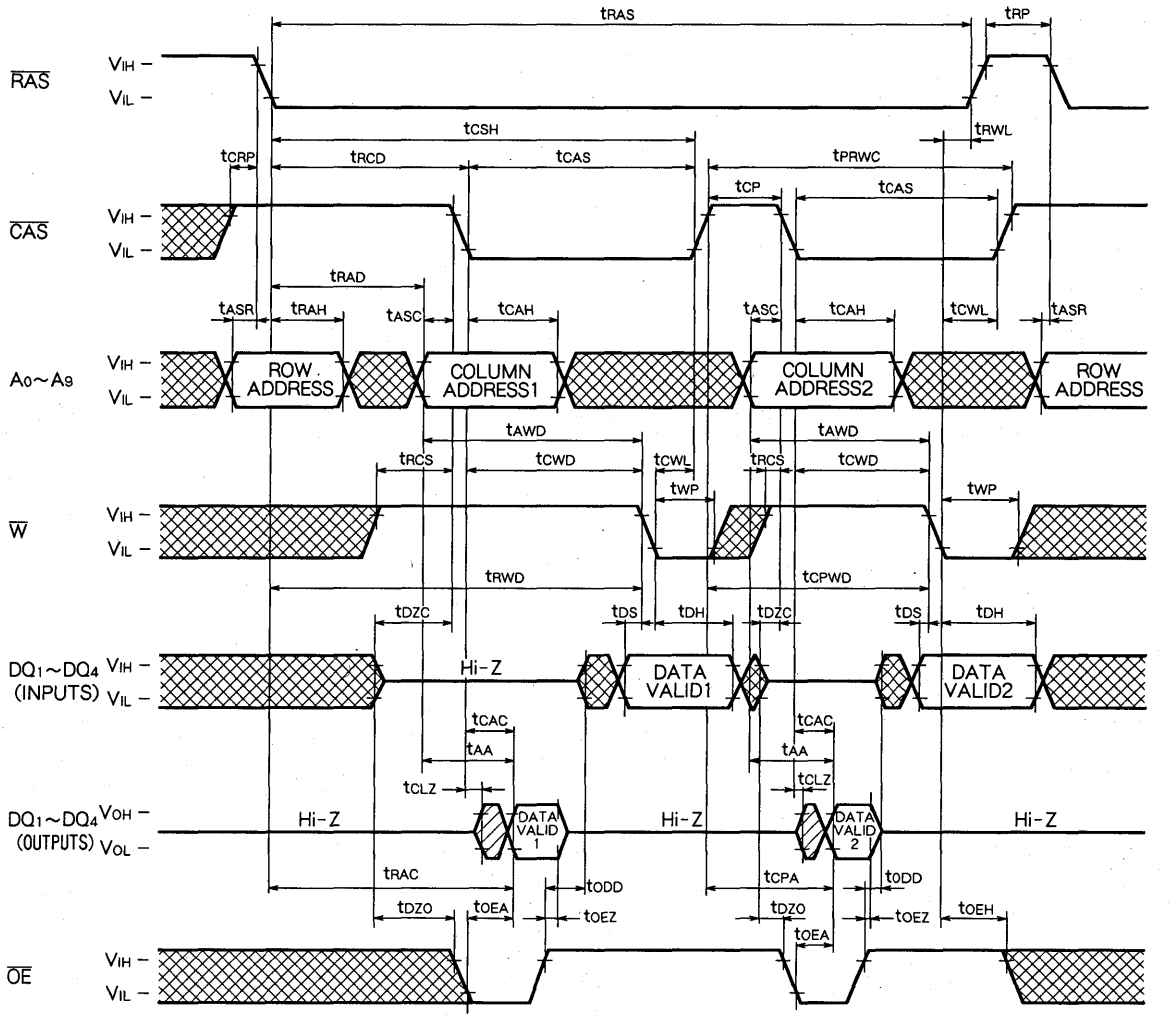


Fast Page Mode Write Cycle (Delayed Write)

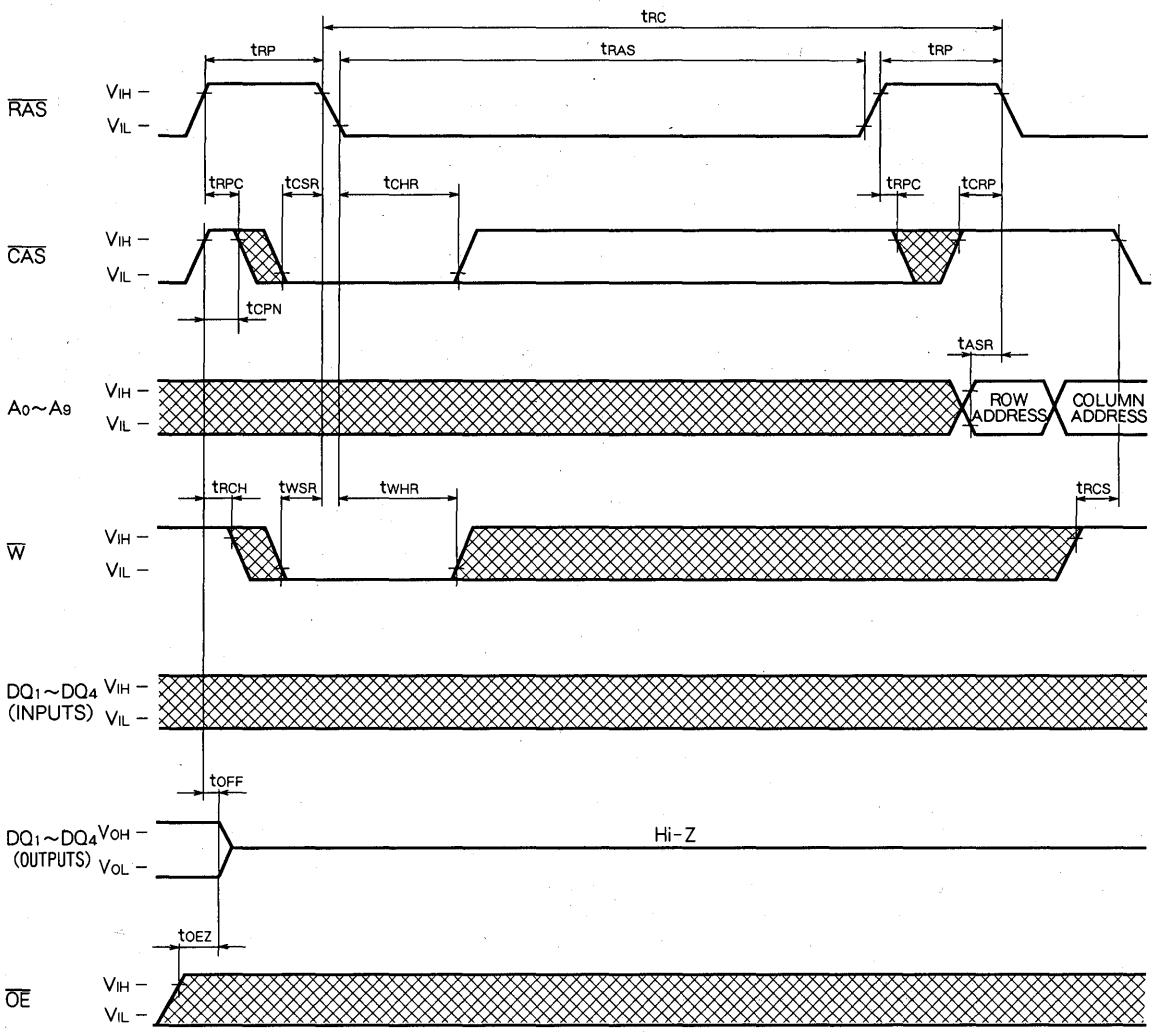


MITSUBISHI ELECTRIC

Fast Page Mode Read-Write, Read-Modify-Write Cycle



Test Mode Set Cycle (Note 32)



Note 32. The cycle is also available for the initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 4 bits wide (256 kilobytes deep) for each DQ (input/output) port.
No addressing of A0, A1 (column only) is required.
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4 bits for each DQ port and can be written independently for each DQ port.
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4 bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

M5M44400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

FEATURES

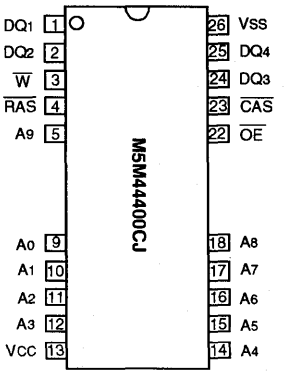
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44400CXX-5,-5S	50	13	25	13	90	500
M5M44400CXX-6,-6S	60	15	30	15	110	400
M5M44400CXX-7,-7S	70	20	35	20	130	350

XX=J,TP

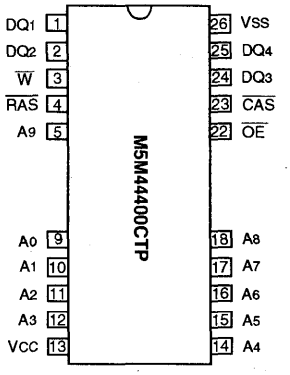
- Standard 26pin SOJ, 26pin TSOP (Ⅱ)
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max) *
- Operating power dissipation
  - M5M44400Cxx-5,-5S ---------- 687.5mW (Max)
  - M5M44400Cxx-6,-6S ---------- 550.0mW (Max)
  - M5M44400Cxx-7,-7S ---------- 467.5mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 120 μA(Max)
- Extended refresh capability
  - Extended refresh current ---------- 120 μA(Max)
- Fast-page mode(1024-column random access),Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{CAS}$ and $\overline{OE}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)
- 1024 refresh cycles every 128ms (A_0 ~ A_9) *
- 4-bit parallel test mode capability

  *:Applicable to self refresh version (M5M44400CJ,TP-5S,-6S,-7S :option) only

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J(300mil SOJ)



Outline 26P3Z-E(300mil TSOP)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

M5M44400CJ,TP-5,-5S:Under development

FUNCTION

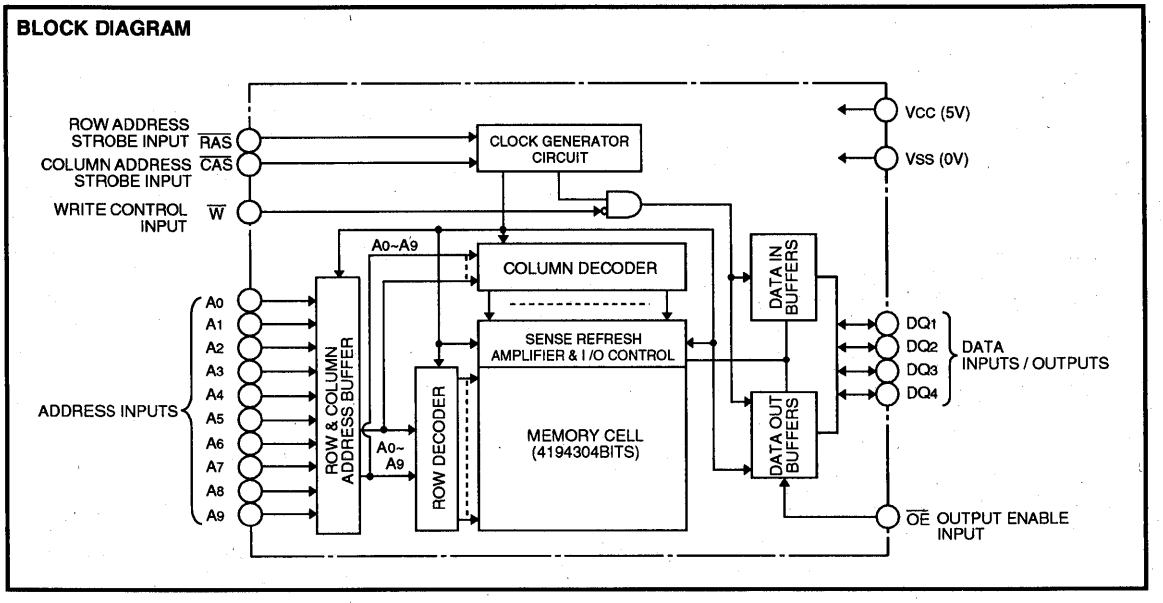
In addition to normal read, write, and read-modify-write operations the M5M44400CJ, TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	NAC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low-level input voltage	DQ_1~DQ_4	-1.0		0.8	V
		Others	-2.0		0.8	

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			125	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	
I_{CC2} (AV)	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.5V output open			1.0	
						0.1*	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			125	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	
I_{CC4}(AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			105	mA
		M5M44400C-6,-6S				85	
		M5M44400C-7,-7S				75	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			105	mA
		M5M44400C-6,-6S				85	
		M5M44400C-7,-7S				75	
I_{CC8}(AV)*	Average supply current from Vcc, Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V(Except for $\overline{RAS}$ falling edge) or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_9≦0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=125μs, t_{RAS}=t_{RASmin}~1μs			120	μA
I_{CC9}(AV)*	Average supply current from Vcc, Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			120	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns

Note 6:An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$- only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than $t_{REF(max)}$) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7:Measured with a load circuit equivalent to 2TTL loads and 100pF.
8:Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9:Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RCD} exceeds the value shown.
10:Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11:Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12:$t_{OFF(max)}$, $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(T_a=0 ~70°C, V_{CC} = 5V±10%, V_{SS}=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4	ms
t_{REF}	Refresh cycle time*			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	7	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		20		ns
t_T	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T=5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	0		0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		8		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{WP}	Write pulse width		8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 22)	126		150		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		86	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		49	10000	55	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		86		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		49		55		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	31		35		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	68		80		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 23)	43		50		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{WP}	Write pulse width		8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	71		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 25)	85	100000	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	48		55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		20		25		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RSR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Test Mode Specification (Note 29)

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			145	mA
		M5M44400C-6,-6S	t_{RC}=t_{WC}=min.			115	
		M5M44400C-7,-7S	output open			100	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}			145	mA
		M5M44400C-6,-6S	t_{RC}=min.			115	
		M5M44400C-7,-7S	output open			100	
I_{CC4} (AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			120	mA
		M5M44400C-6,-6S	t_{PC}=min.			100	
		M5M44400C-7,-7S	output open			85	
I_{CC6} (AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			120	mA
		M5M44400C-6,-6S	t_{RC}=min.			100	
		M5M44400C-7,-7S	output open			85	

Note 29:All previously specified electrical characteristics, switching characteristics, and timing requirements are applicable to that of test mode.

SWITCHING CHARATERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6, 13, 14)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7, 8)		18		20		25	ns
tRAC	Access time from $\overline{RAS}$	(Note 7, 9)		55		65		75	ns
tAA	Column address access time	(Note 7, 10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		18		20		25	ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 13, 14)

Read and Refresh Cfycle

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	95		115		135		ns
tRAS	$\overline{RAS}$ low pulse width	55	10000	65	10000	75	10000	ns
tCAS	$\overline{CAS}$ low pulse width	18	10000	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	55		65		75		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	18		20		25		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	18		20		25		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	18		20		25		ns

Read Write and Read-Modify-Write Cfycle

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	131		155		185		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	125	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	75	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		125		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		75		ns
tCWD	Delay time, $\overline{CAS}$ low $\overline{W}$ low	(Note 23)	36		40		50		ns
tRWD	Delay time, $\overline{RAS}$ low $\overline{W}$ low	(Note 23)	73		85		100		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	48		55		65		ns

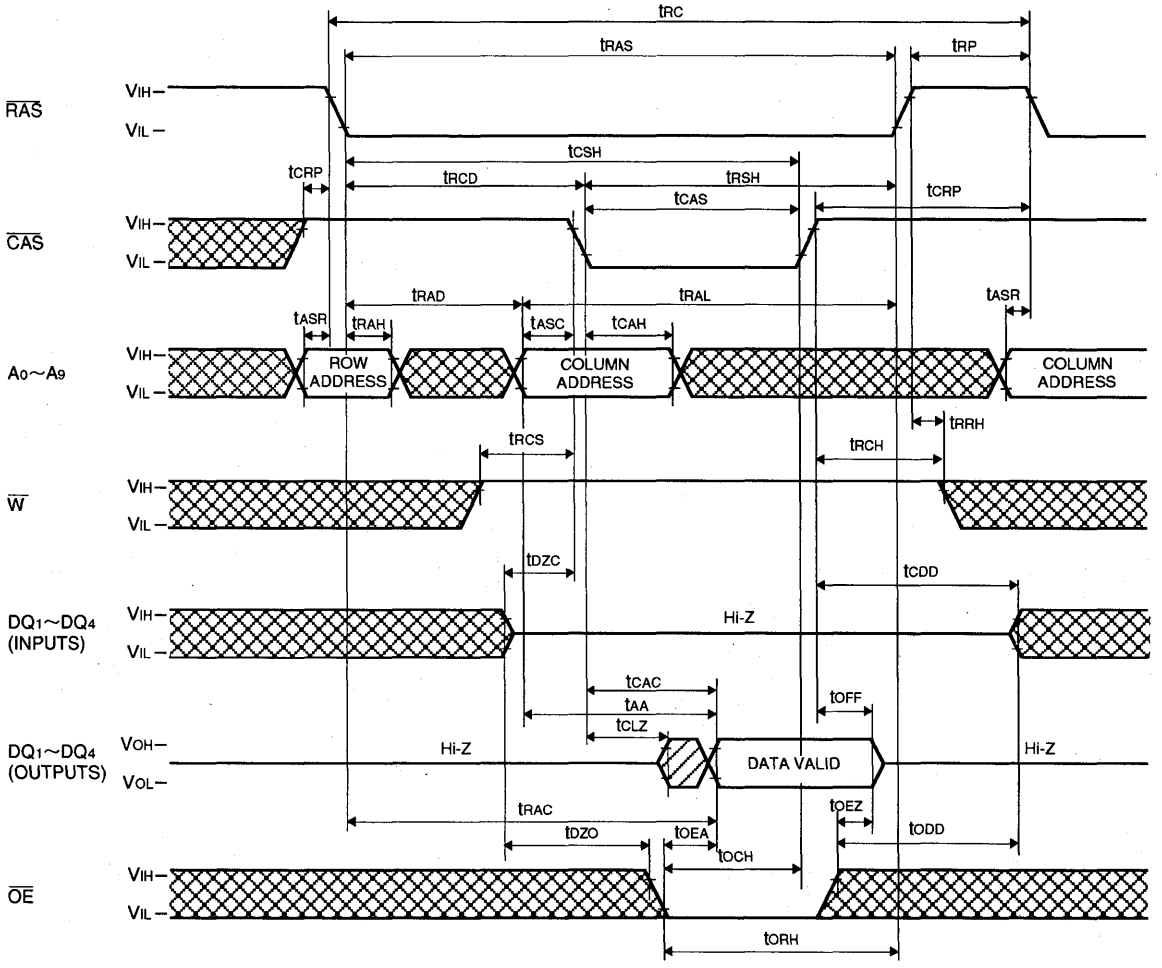
Fast page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		40		45		50		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		100		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle	(Note 25)	95	100000	110	100000	125	100000	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		45		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	53		60		70		ns

Test Mode Set Cycle

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	Write setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	Write hold time after $\overline{RAS}$ low	10		10		15		ns

Timing Diagrams (Note 30)
Read Cycle

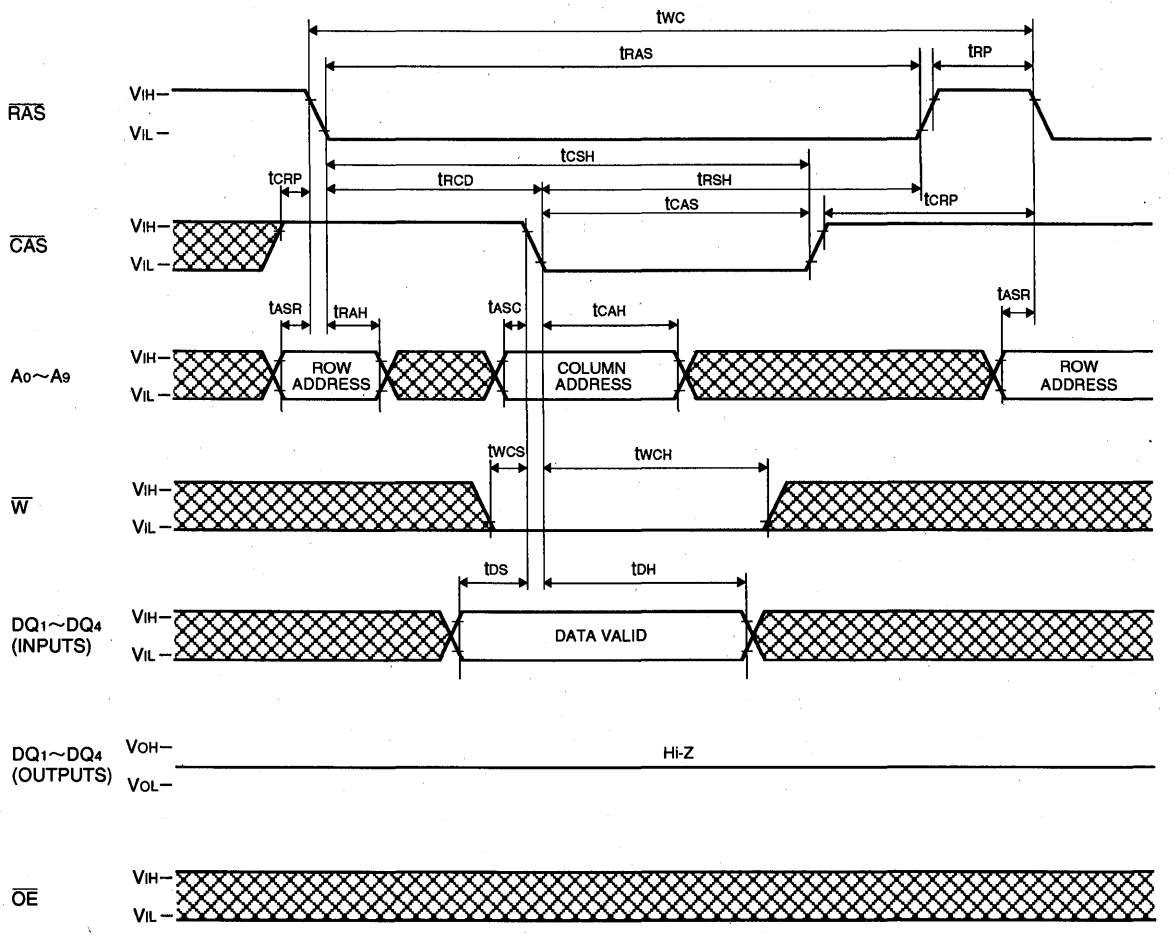


Note 30

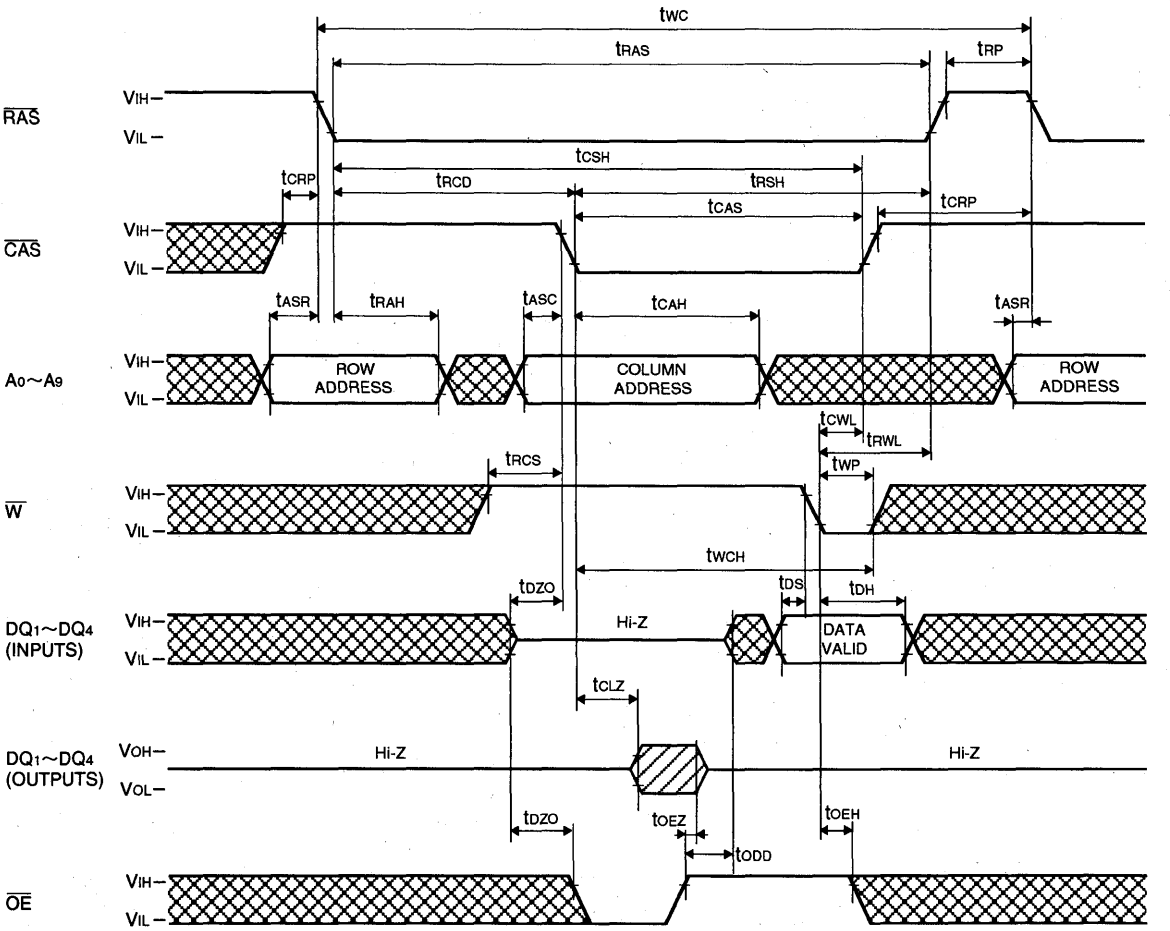
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

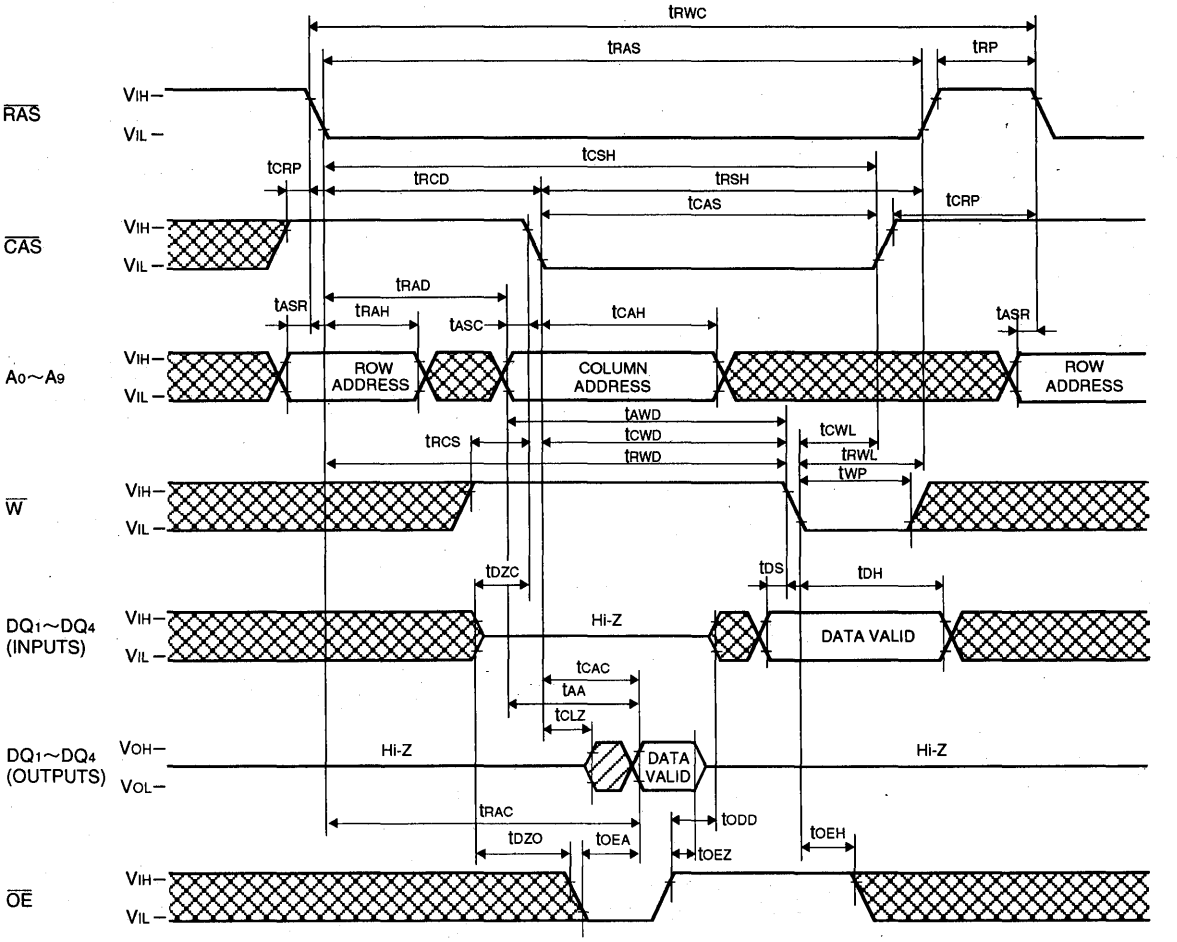
Write Cycle (Early write)



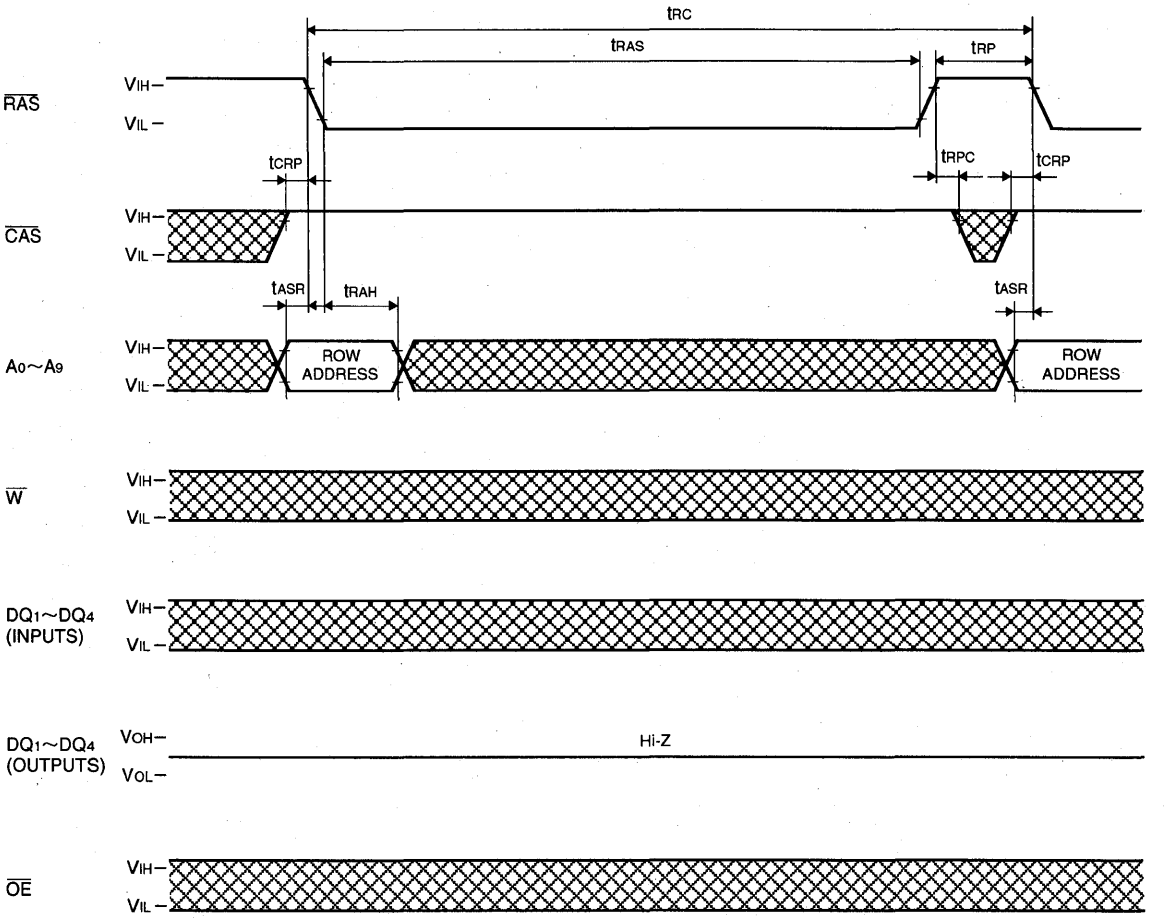
Write Cycle (Delayed write)



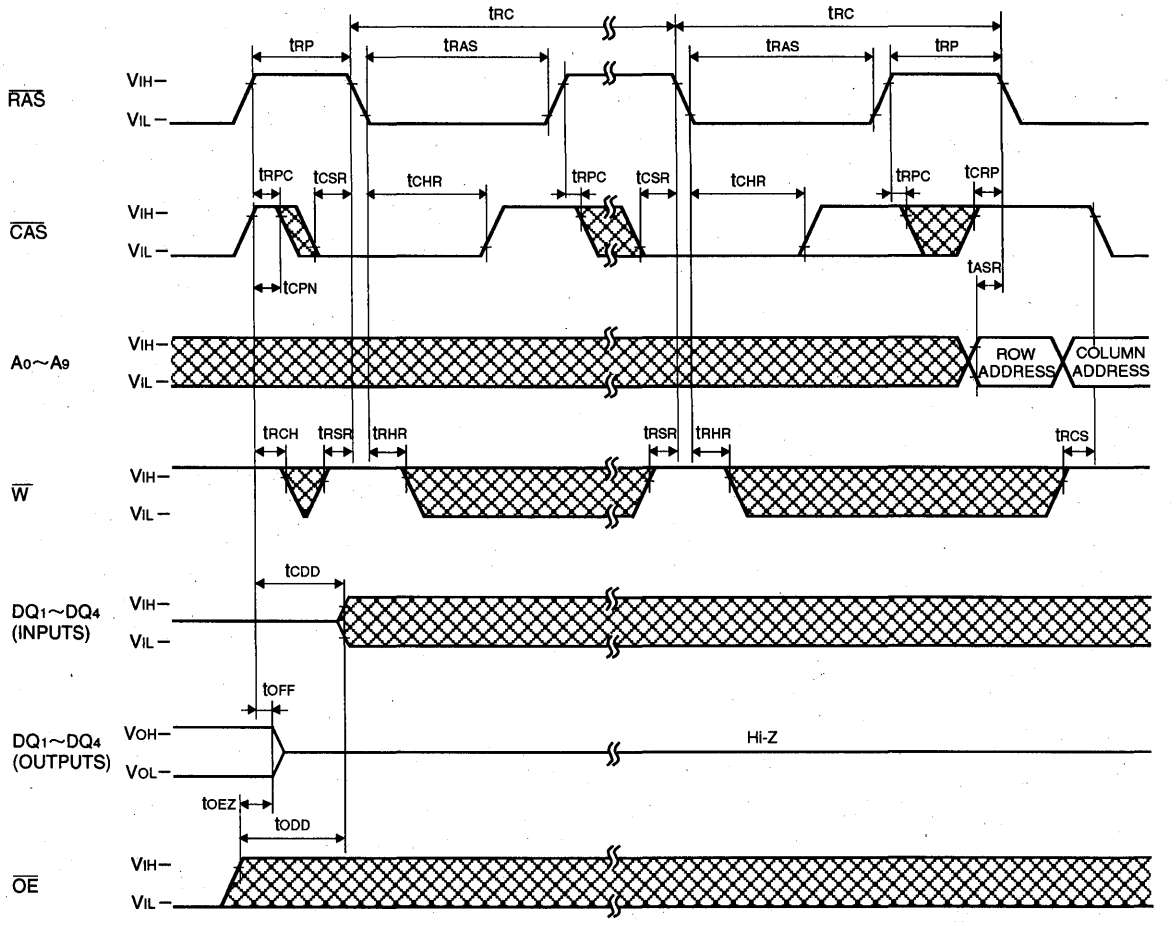
Read-Write, Read-Modify-Write Cycle



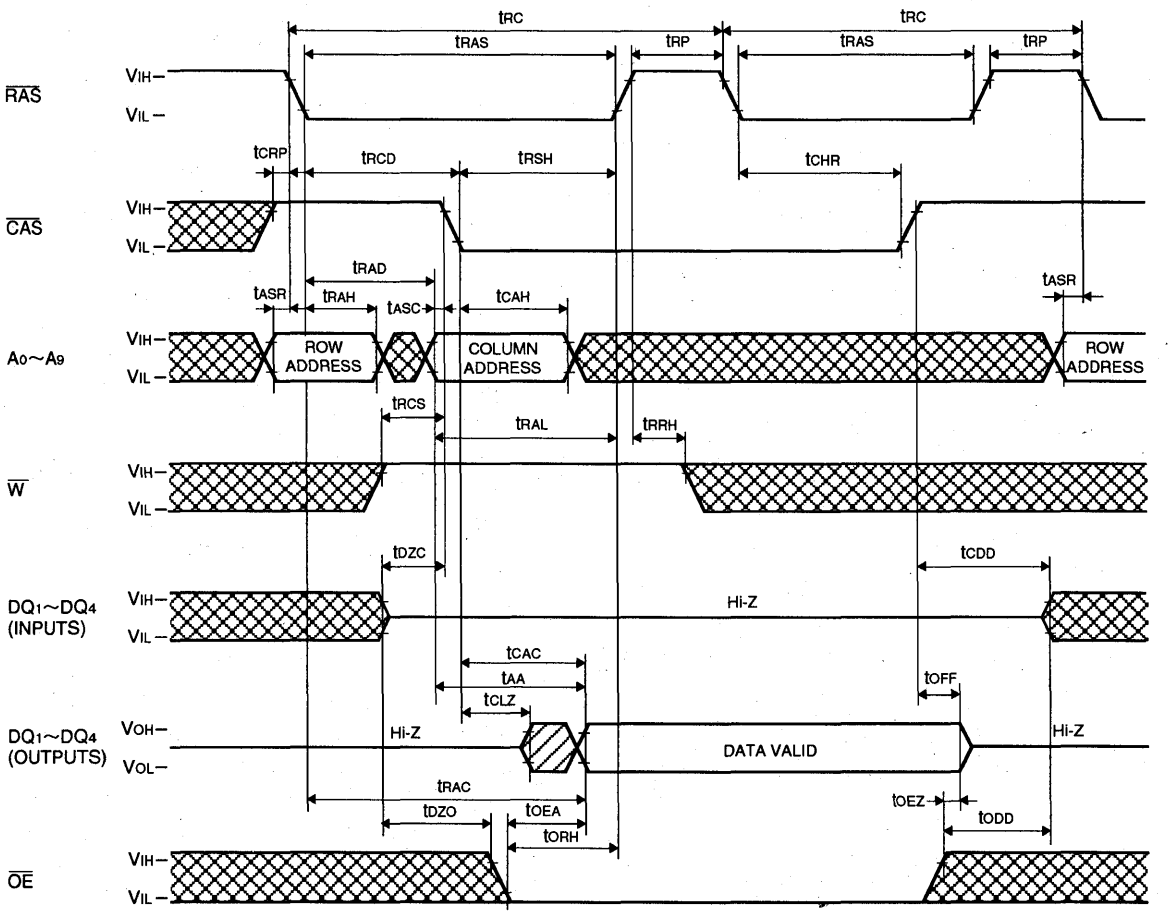
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

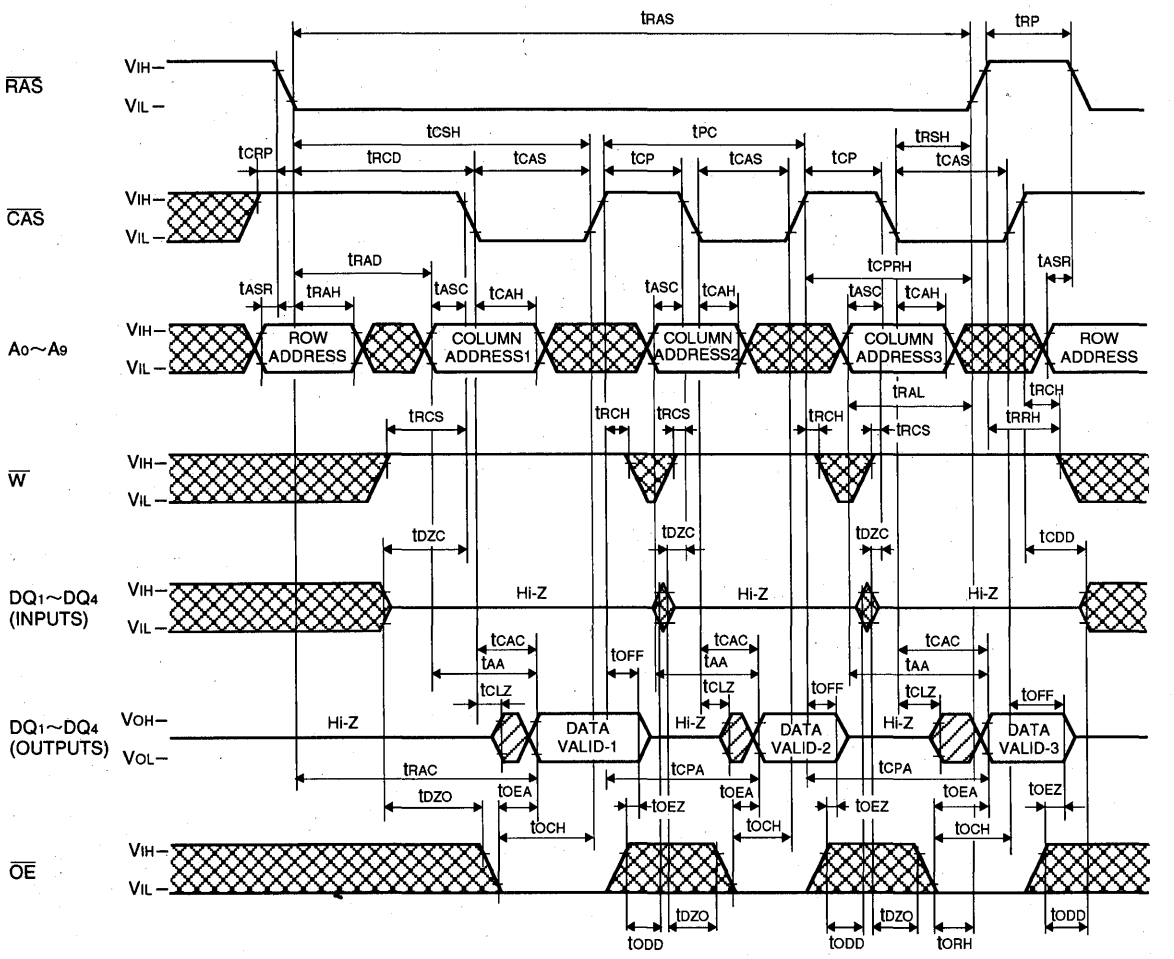


Hidden Refresh Cycle (Read) (Note 31)



Note 31: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

Fast Page Mode Read Cycle



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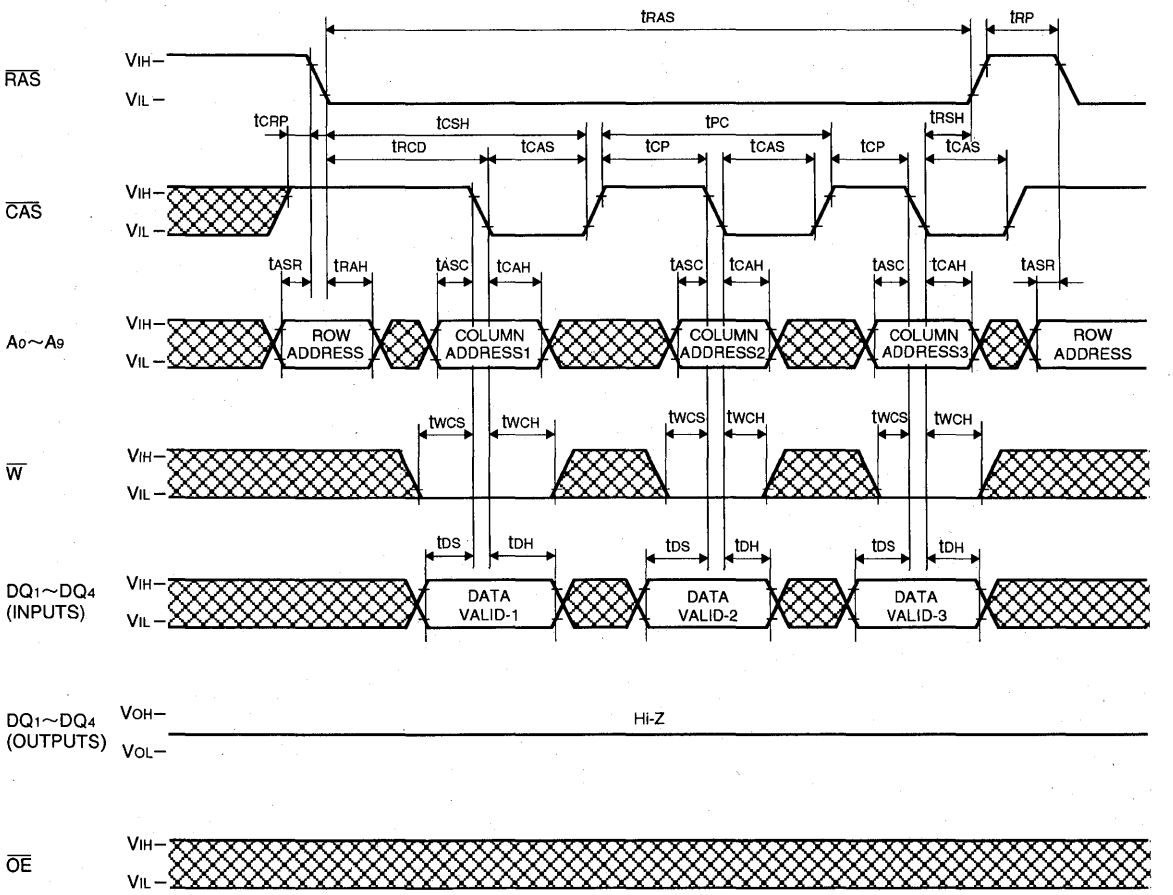
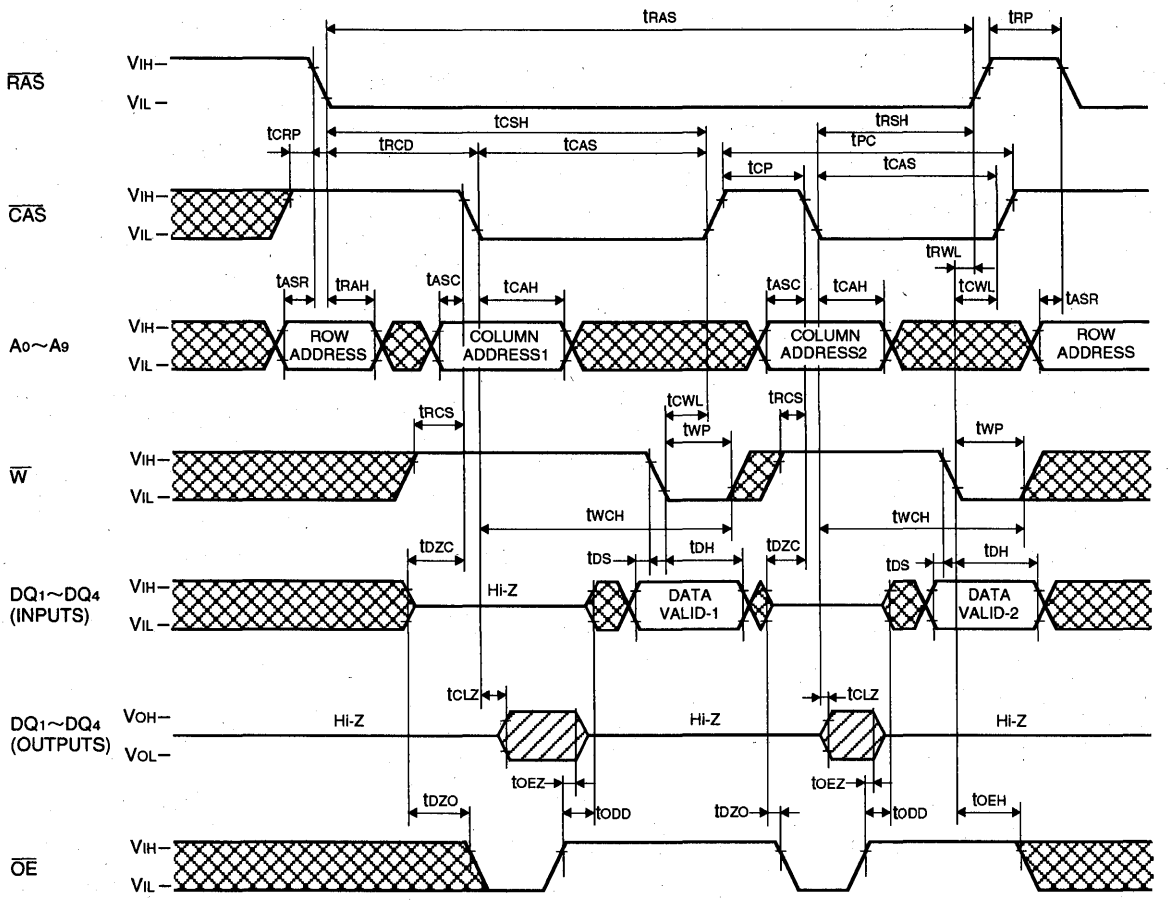
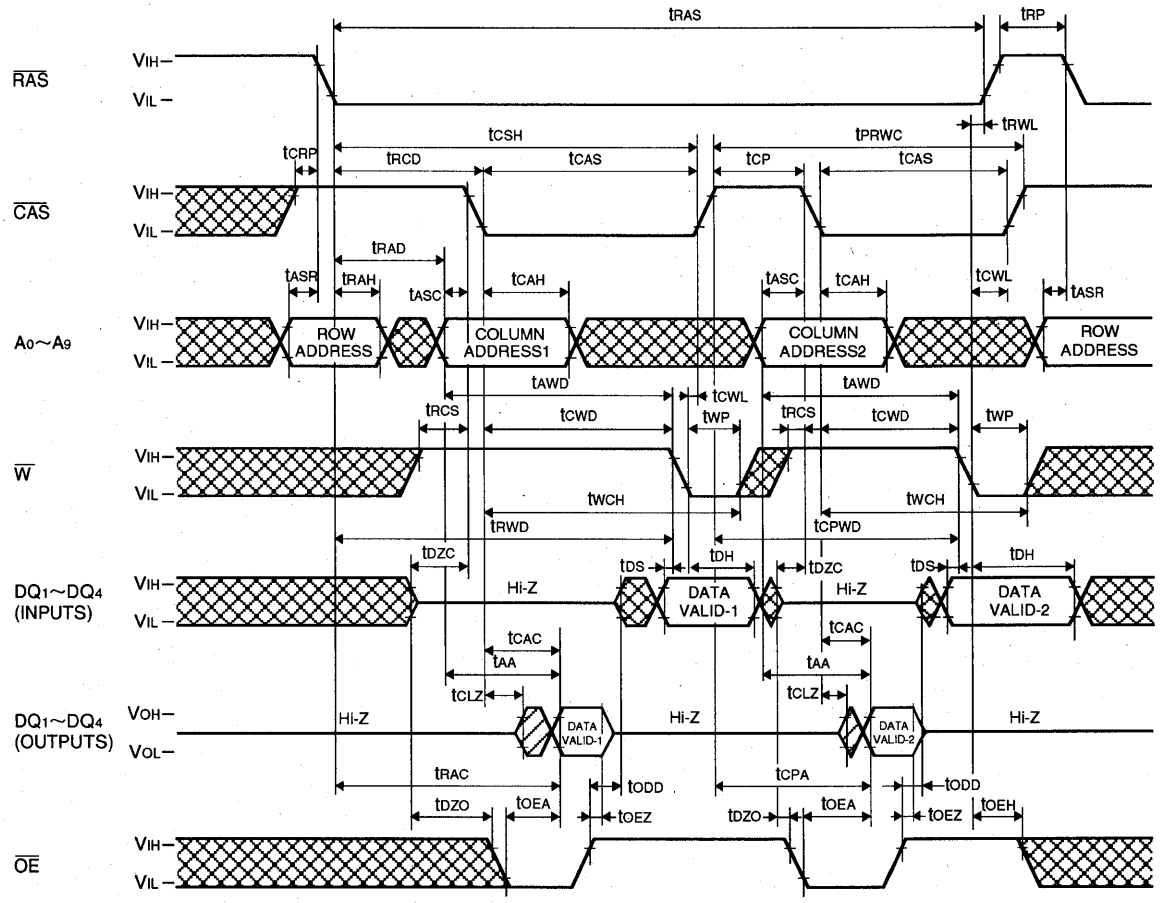
Fast Page Mode Write Cycle (Early Write)



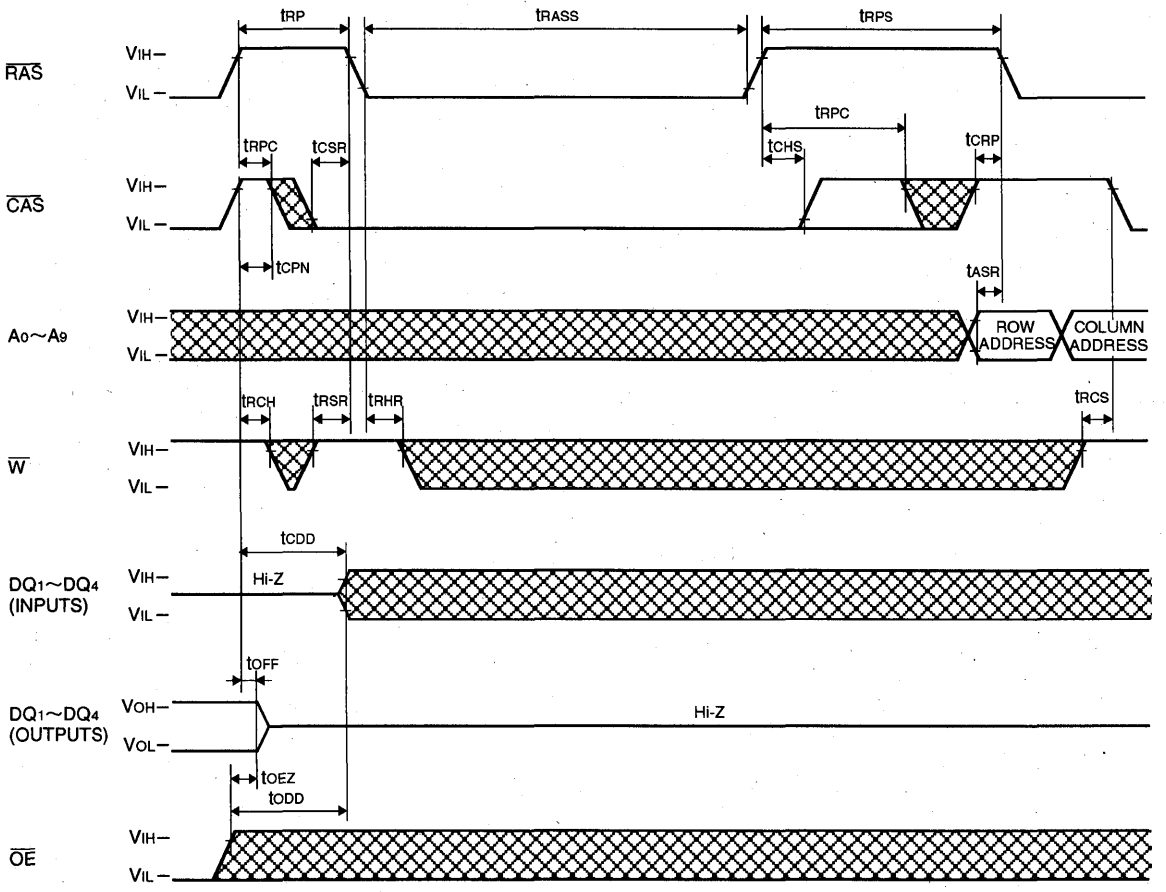
Fast-Page Mode Write Cycle (Delayed Write)



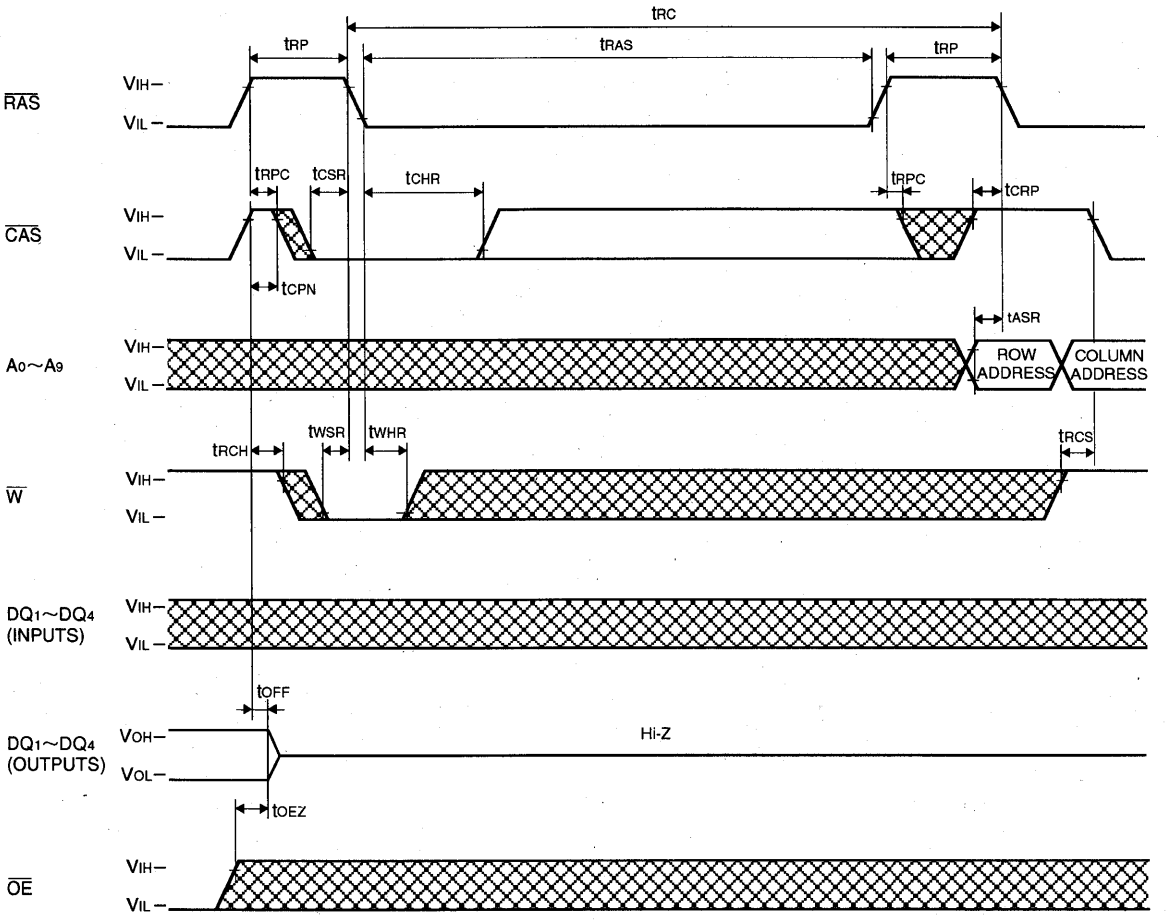
Fast Page Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 28)



Test Mode Set Cycle (Note 32)



Note : 32 The cycle is also availlable for initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle(WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$(CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 4-bits wide (256k-bytes deep) for each DQ (input/output) port.
No addressing of A0,A1(column only) is required.
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4-bits for each DQ port and can be written independently for each DQ port.
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4-bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

Note 28:Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing diagram

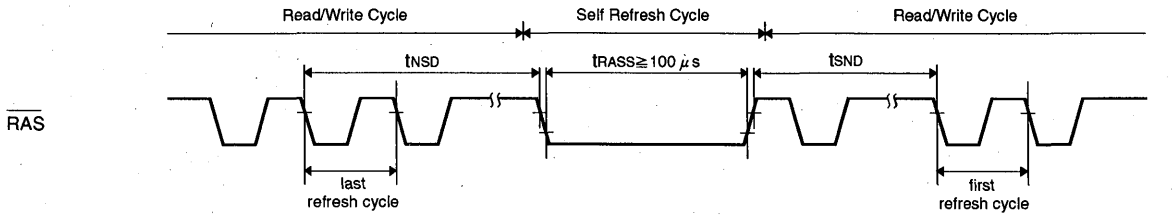
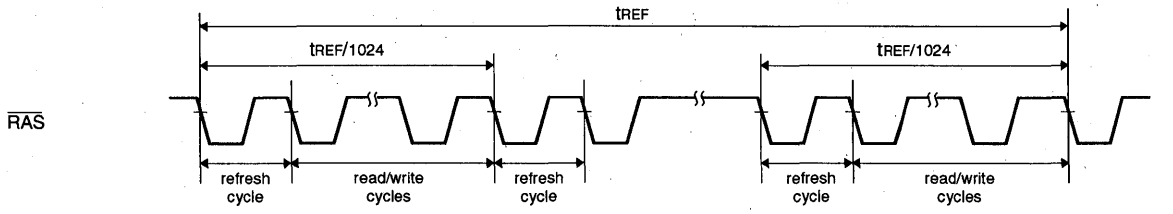


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	t_{NSD}≧125 μs	t_{SND}≧125 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≧16 μs	t_{SND}≧16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max.) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of row address signals (A_0~A_9) are selected during 1024 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation

(A) Timing diagram

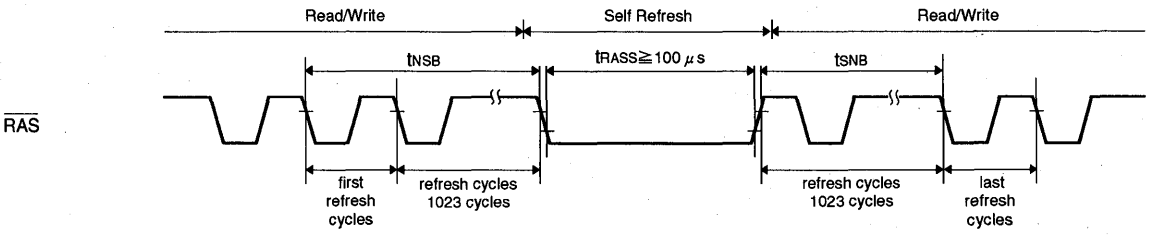
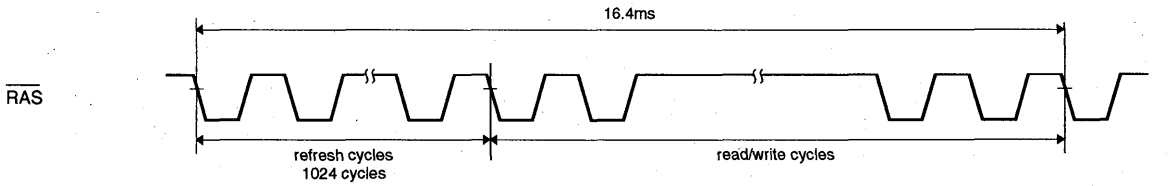


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	tNSB≦16.4ms	tSNB≦16.4ms
$\overline{RAS}$ only burst refresh	tNSB+tSNB≦16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read / write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

M5M44800CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (524288-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 524288-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44800CXX-5,-5S	50	13	25	13	90	450
M5M44800CXX-6,-6S	60	15	30	15	110	375
M5M44800CXX-7,-7S	70	20	35	20	130	325

XX=J,TP

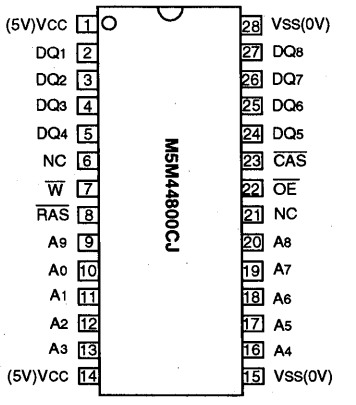
- Standard 28pin SOJ, 28pin TSOP (Ⅱ)
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max) *
- Operating power dissipation
  - M5M44800Cxx-5,-5S ---------- 495mW (Max)
  - M5M44800Cxx-6,-6S ---------- 413mW (Max)
  - M5M44800Cxx-7,-7S ---------- 358mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 150 μA(Max)
- Extended refresh capability
  - Extended refresh current ---------- 150 μA(Max)
- Fast page mode(1024-column random access),Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{CAS}$ and $\overline{OE}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)
- 1024 refresh cycles every 128ms (A_0 ~ A_9) *

* :Applicable to self refresh version (M5M44800CJ,TP-5S,-6S,-7S :option) only

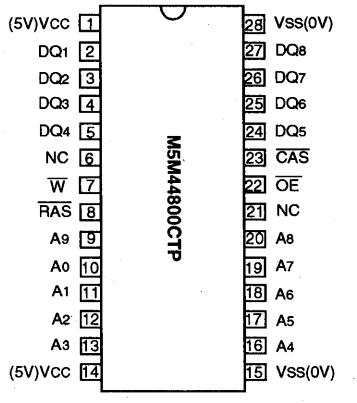
APPLICATION

Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K(400mil SOJ)



Outline 28P3Y-H(400mil TSOP Normal Bend)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_8	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

M5M44800CJ,TP-5,-5S:Under development

MITSUBISHI ELECTRIC

FAST PAGE MODE 4194304-BIT (524288-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

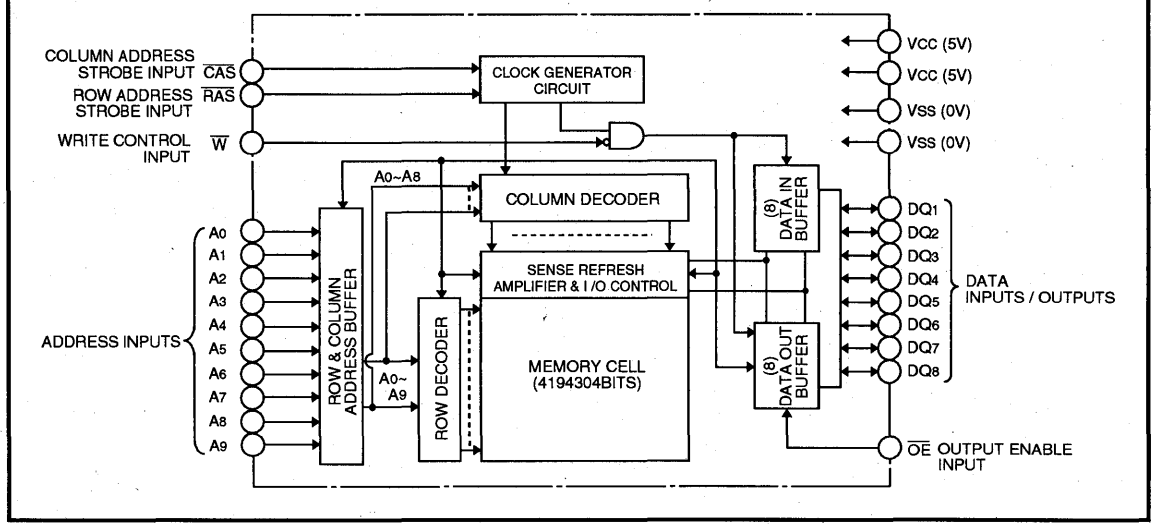
In addition to normal read, write, and read-modify-write operations the M5M44800CJ, TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-0.5**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : $V_{IL(min)}$ is -2.0V when pulse width is less than 25ns. (Pulse width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.0V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44800C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			90	mA
		M5M44800C-6,-6S	t_{RC}=t_{WC}=min.			75	
		M5M44800C-7,-7S	output open			65	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.5V output open			1.0	
						0.1*	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44800C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH}			90	mA
		M5M44800C-6,-6S	t_{RC}=min.			75	
		M5M44800C-7,-7S	output open			65	
I_{CC4}(AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44800C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			90	mA
		M5M44800C-6,-6S	t_{PC}=min.			75	
		M5M44800C-7,-7S	output open			65	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44800C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			80	mA
		M5M44800C-6,-6S	t_{RC}=min.			65	
		M5M44800C-7,-7S	output open			55	
I_{CC8}(AV)*	Average supply current from Vcc, Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_9≦0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=125μs, t_{RAS}=t_{RAS}min~1μs			150	μA
I_{CC9}(AV)*	Average supply current from Vcc, Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			150	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns

Note 6:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$- only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7:Measured with a load circuit equivalent to 2TTL loads and 100pF.

8:Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9:Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10:Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11:Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12:$t_{OFF(max)}$, $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(T_a=0 ~70°C, V_{CC} = 5V±10%, V_{SS}=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4	ms
t_{REF}	Refresh cycle time*			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	7	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		20		ns
t_T	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T=5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	0		0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	126		150		180		ns
tRAS	$\overline{RAS}$ low pulse width		86	10000	100	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		49	10000	55	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		86		100		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		49		55		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	31		35		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	68		80		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	43		50		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	71		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 25)	85	100000	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	48		55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

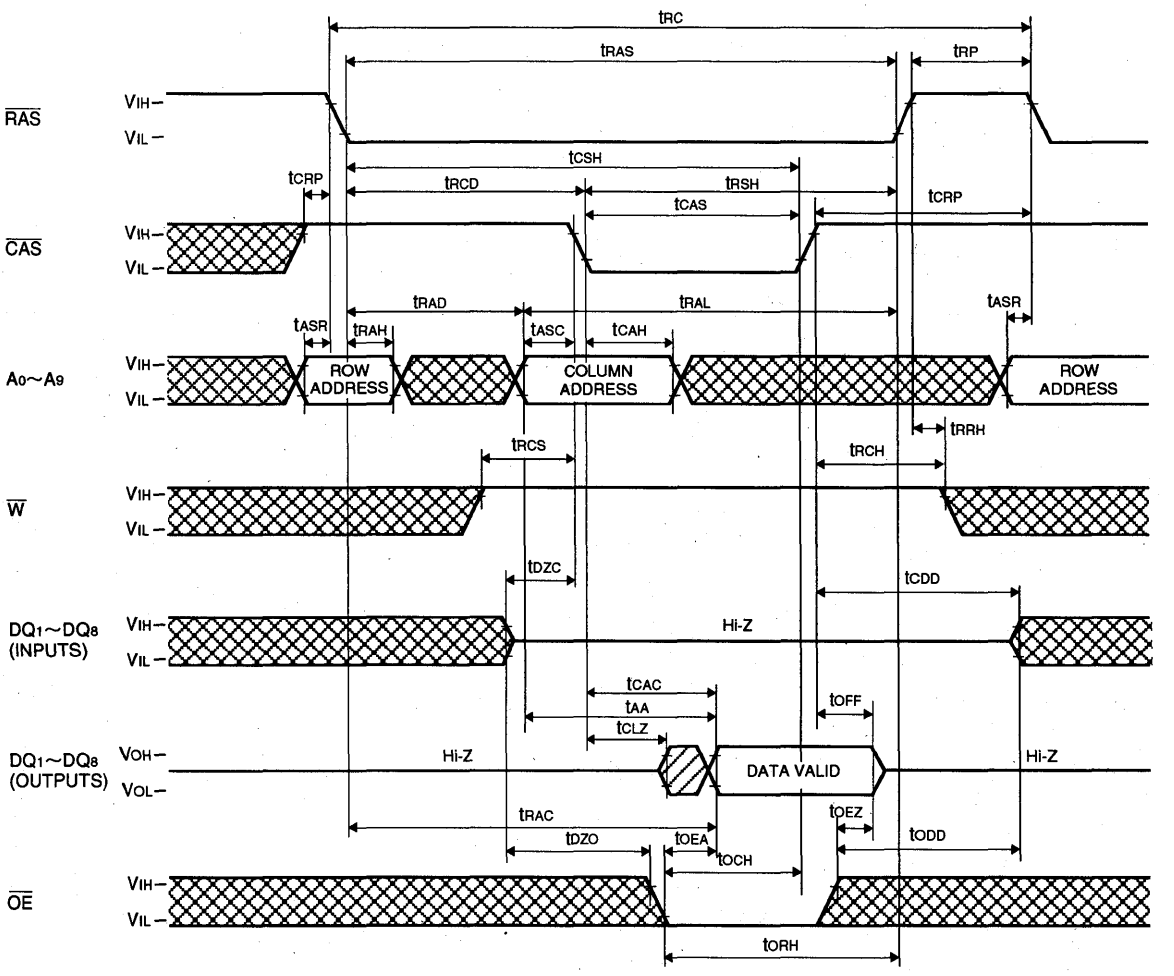
Symbol	Parameter	Limits						Unit
		M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		20		25		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits						Unit
		M5M44800C-5,-5S		M5M44800C-6,-6S		M5M44800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns

Timing Diagrams (Note 29)
Read Cycle

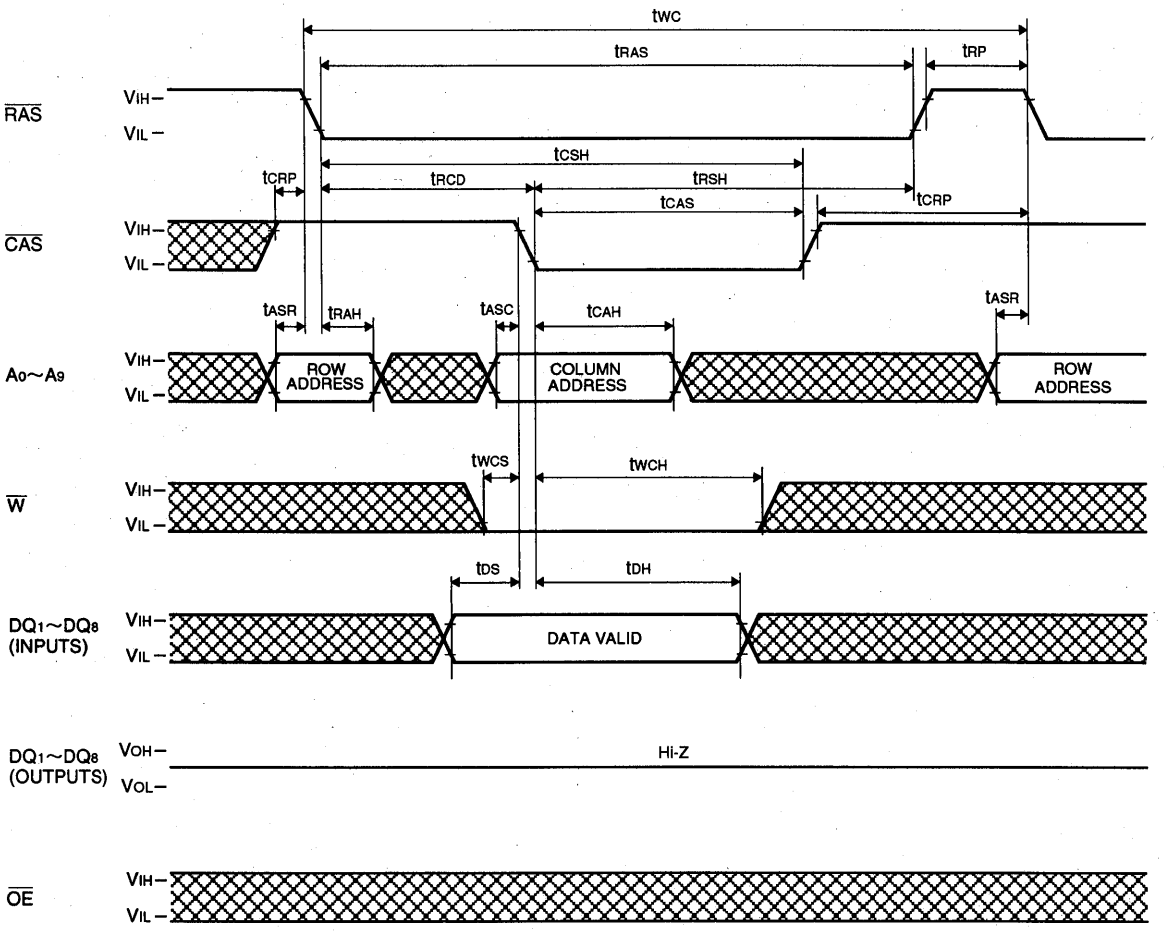


Note 29

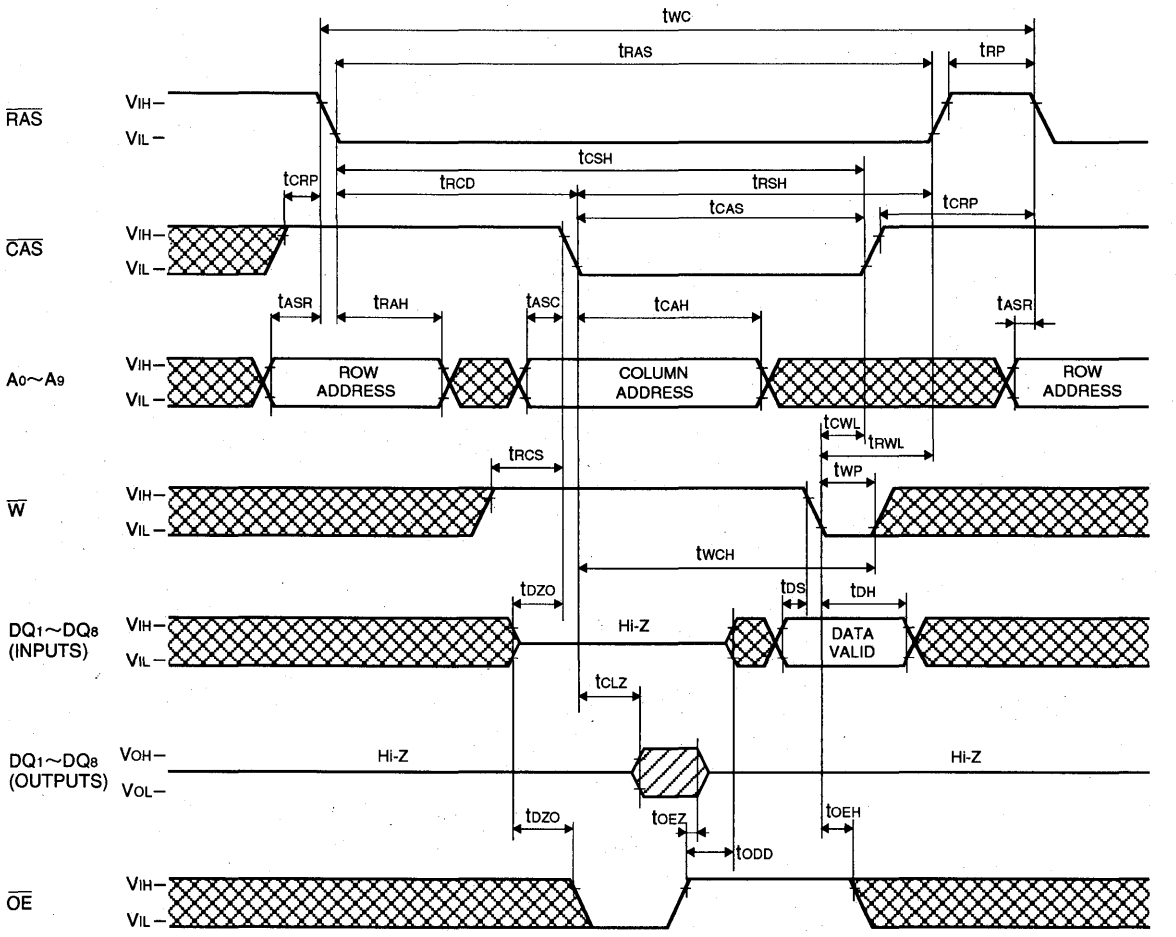
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

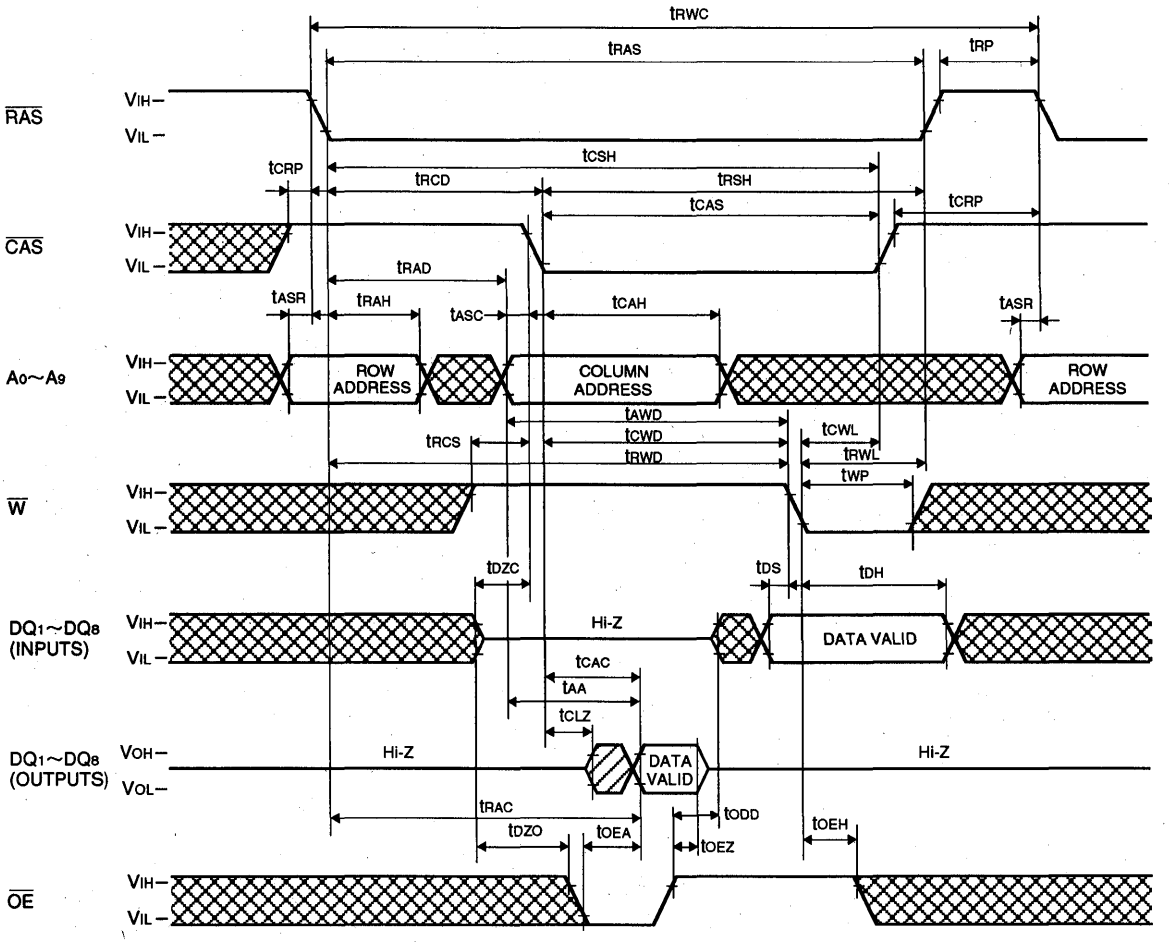
Write Cycle (Early write)



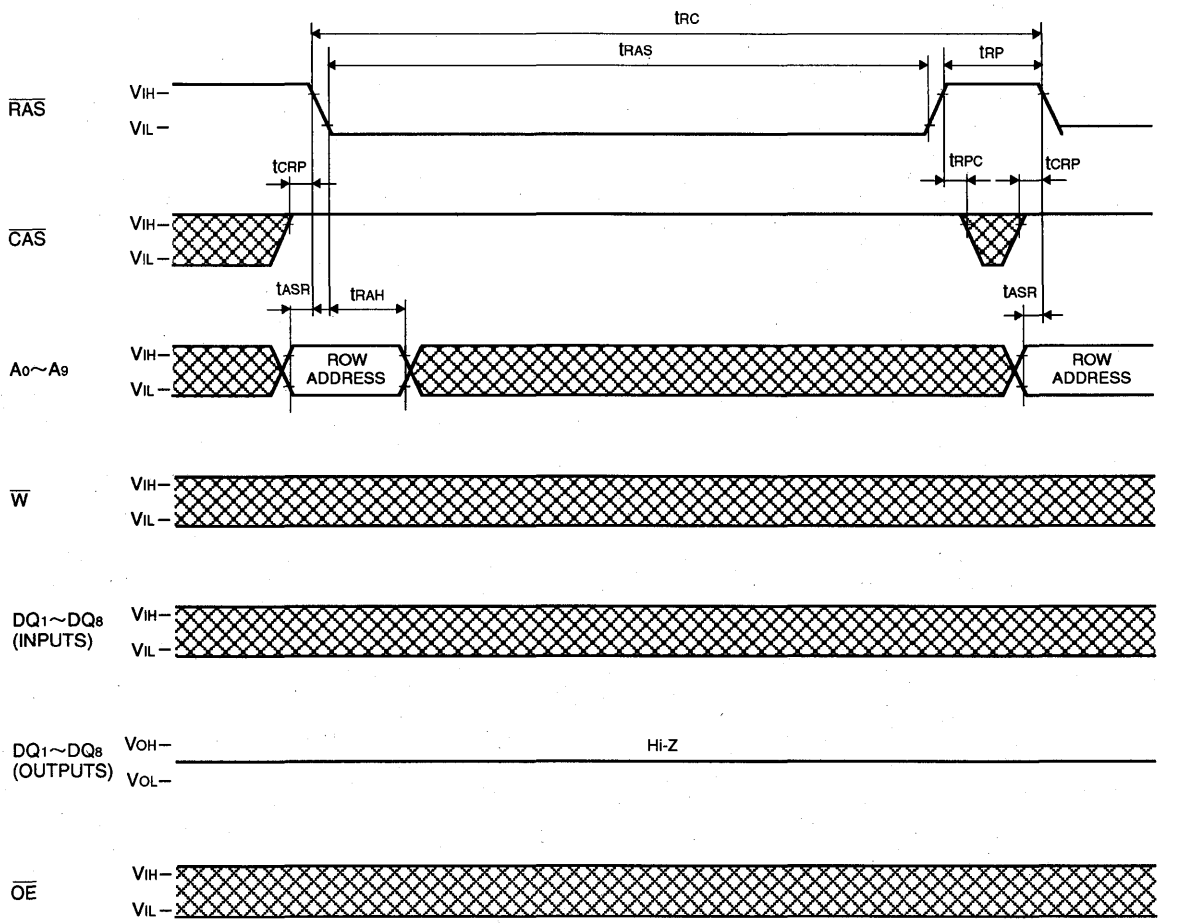
Write Cycle (Delayed write)



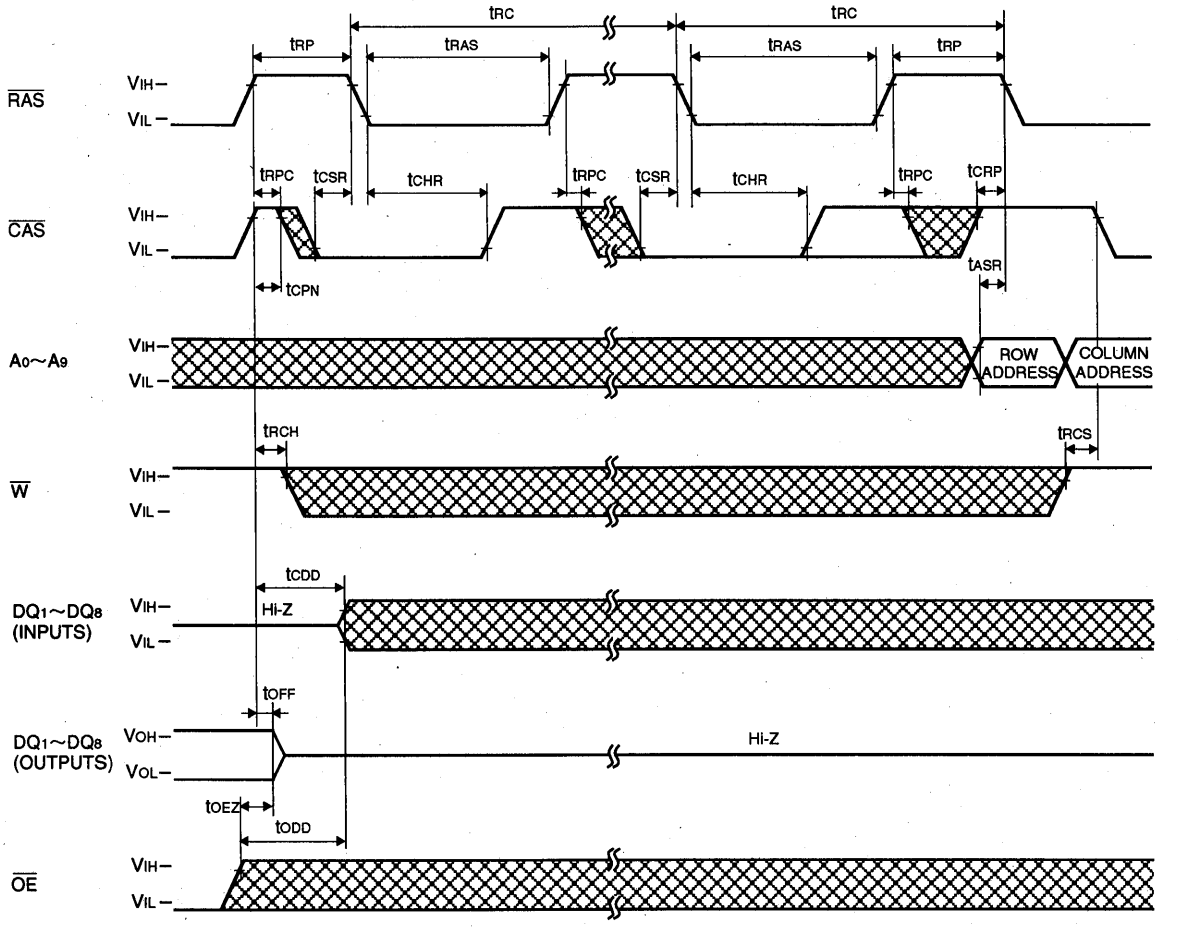
Read-Write, Read-Modify-Write Cycle



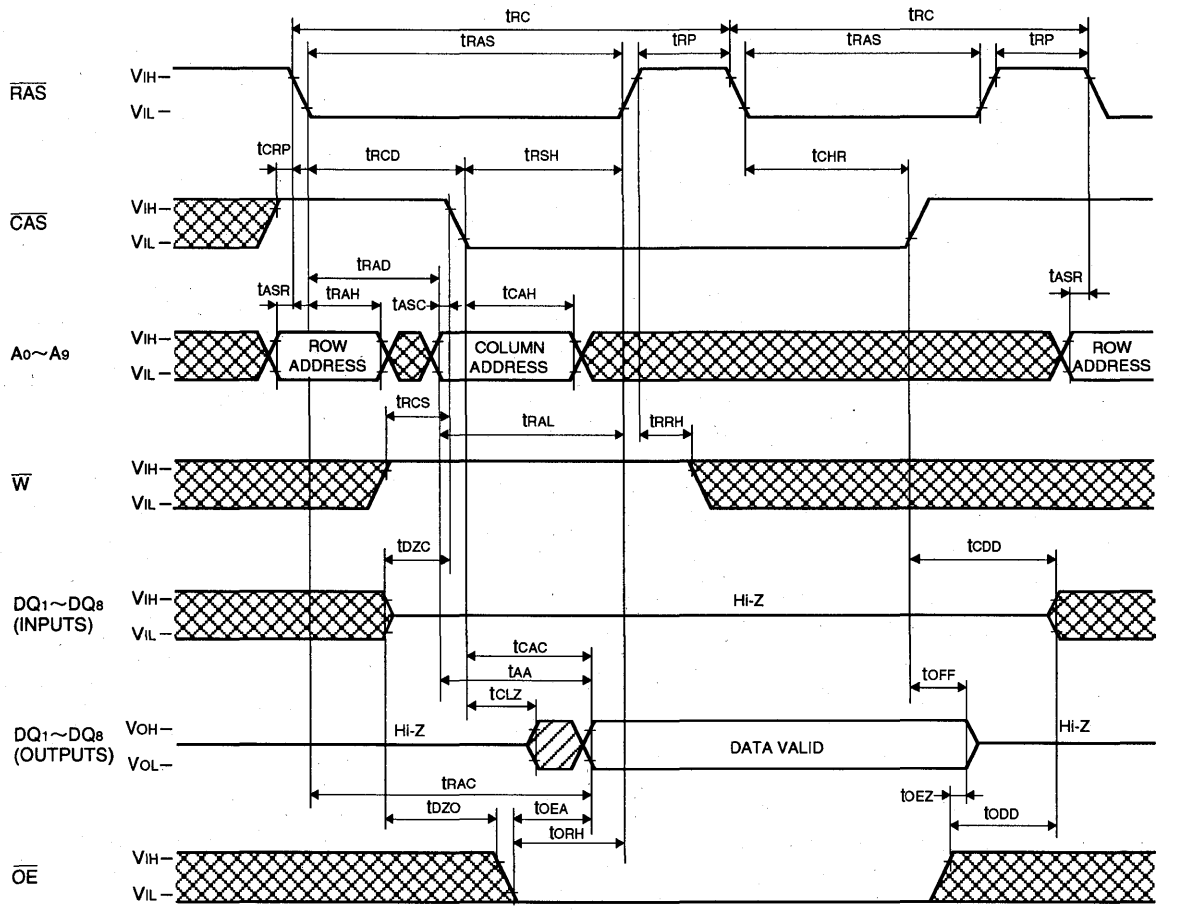
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

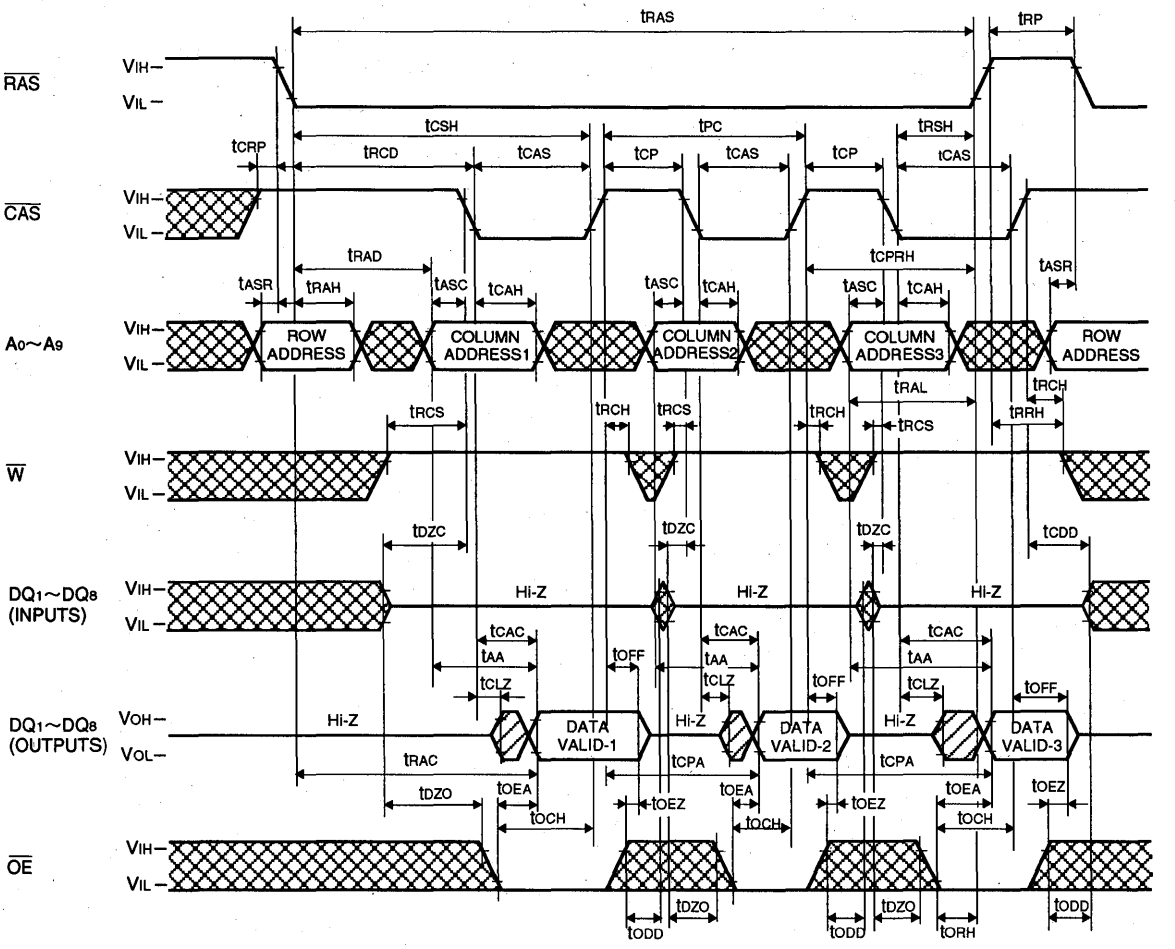


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

Fast Page Mode Read Cycle



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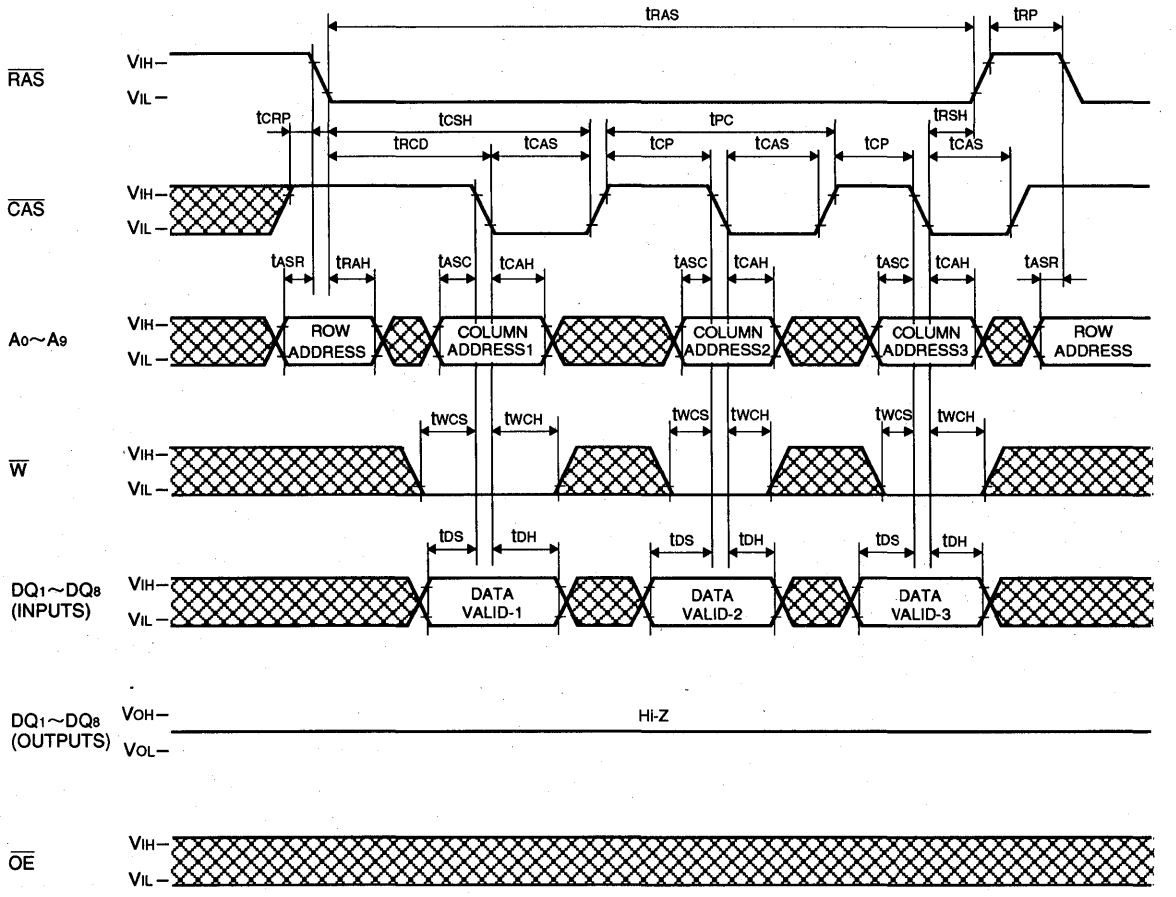
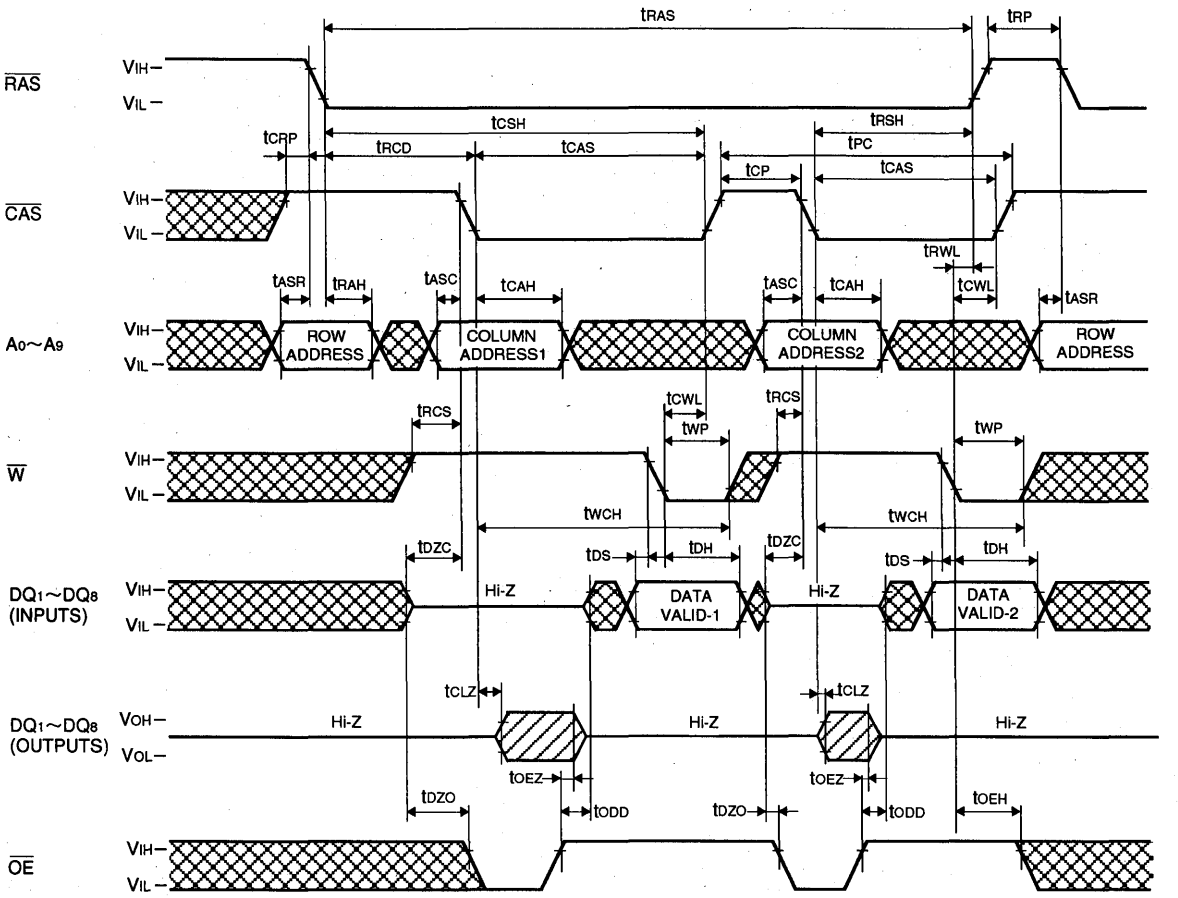
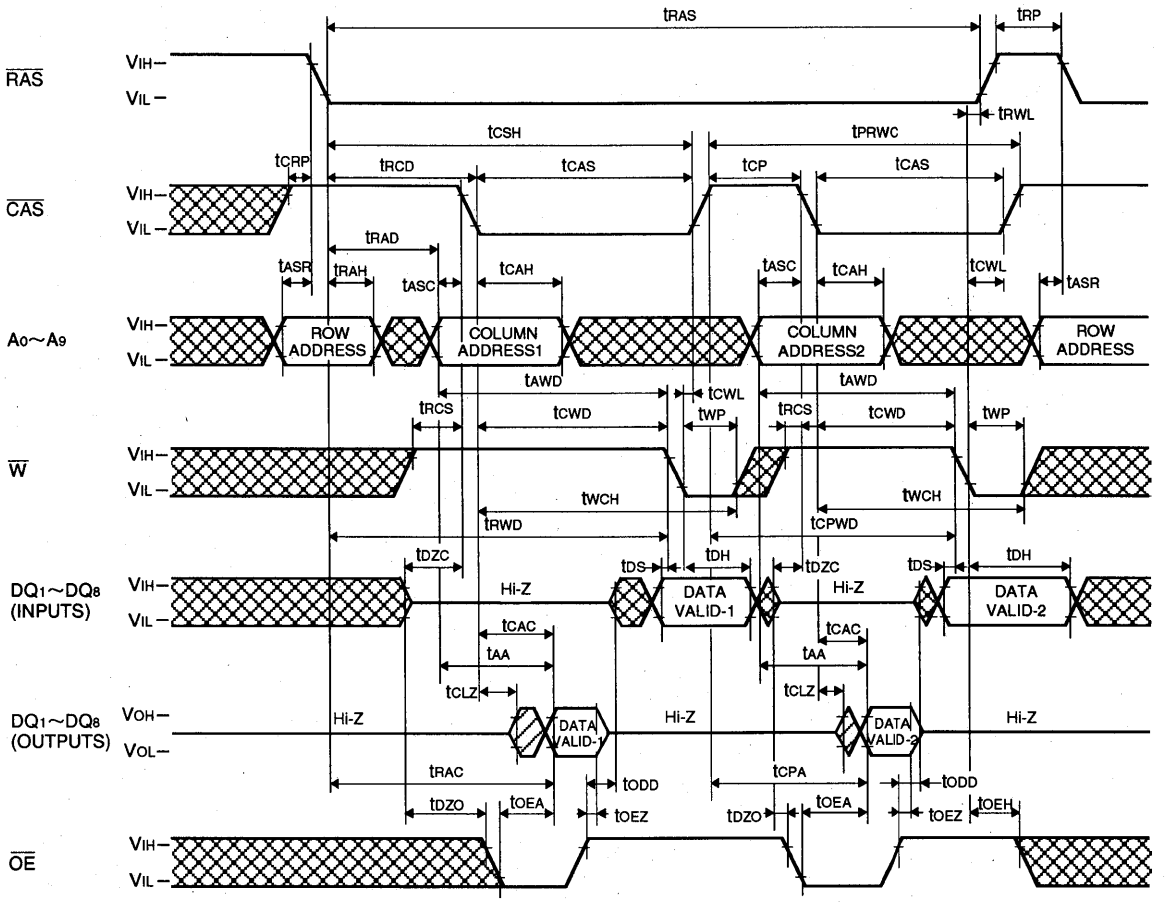
Fast Page Mode Write Cycle (Early Write)



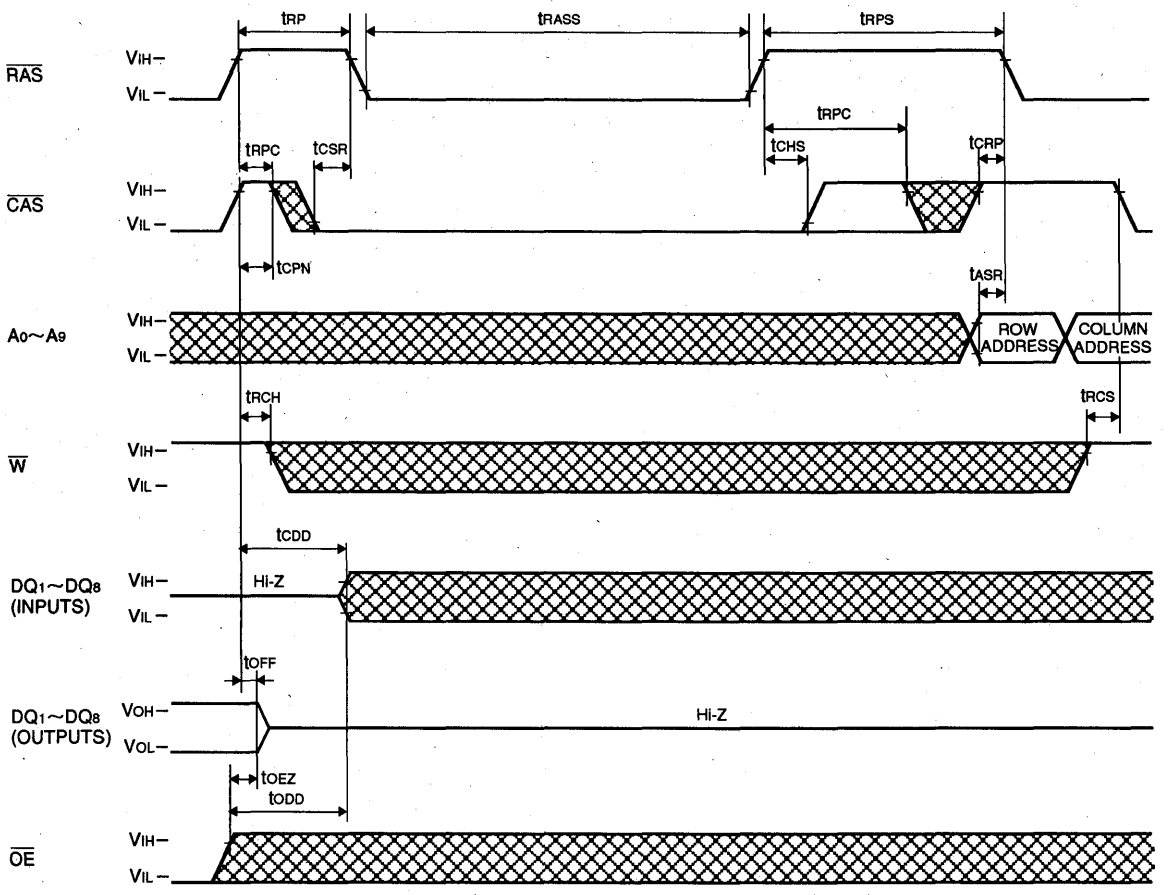
Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 28)



Note 28:Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing diagram

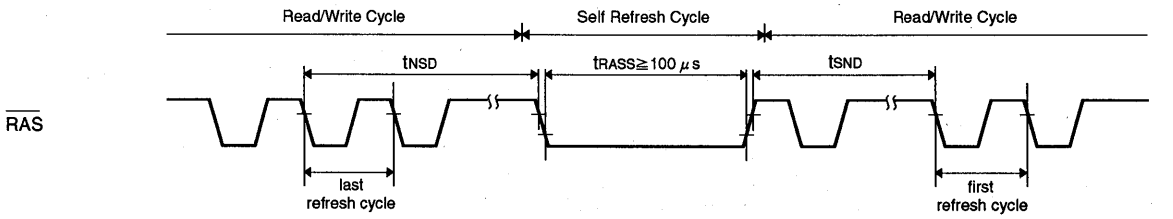
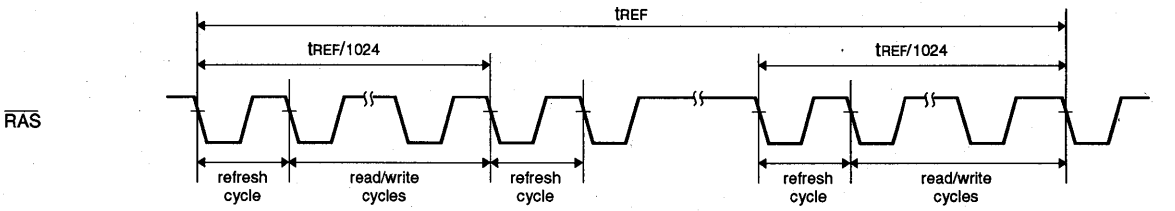


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	t_{NSD}≦125 μs	t_{SND}≦125 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≦16 μs	t_{SND}≦16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max.) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 1024 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation

(A) Timing diagram

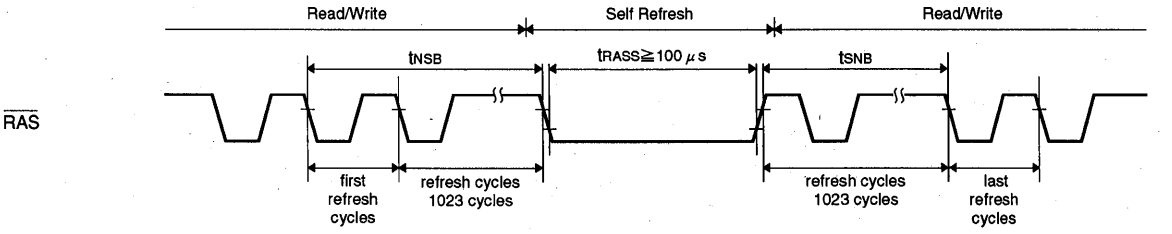
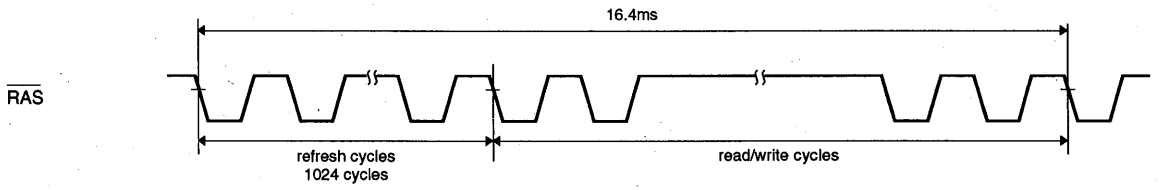


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB}+t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of nine row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read / write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

M5M44260CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is small enough for battery back-up application.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44260CXX-5,-5S	50	13	25	13	90	625
M5M44260CXX-6,-6S	60	15	30	15	110	550
M5M44260CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 40pin SOJ, 44 pin TSOP (II)
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max)*
- Operating power dissipation
  - M5M44260Cxx-5,-5S ---------- 688mW (Max)
  - M5M44260Cxx-6,-6S ---------- 605mW (Max)
  - M5M44260Cxx-7,-7S ---------- 523mW (Max)
- Self refresh capability*
  - Self refresh current ---------- 150 μA (Max)
- Extended refresh capability
  - Extended refresh current ---------- 150 μA (Max)
- Fast-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{LCAS}$ / $\overline{UCAS}$ and $\overline{OE}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 128ms (A_0~A_8)*
- Byte or word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

*: Applicable to self refresh version (M5M44260CJ,TP-5S,-6S,-7S : option) only

APPLICATION

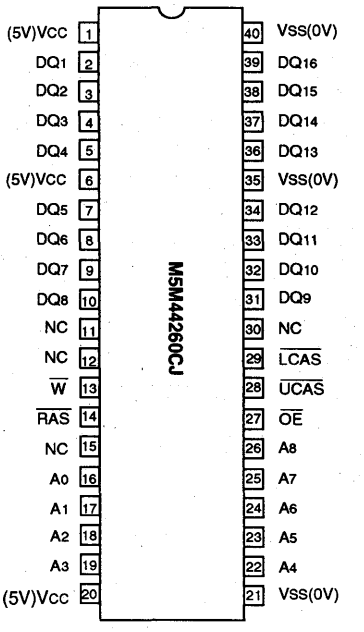
Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

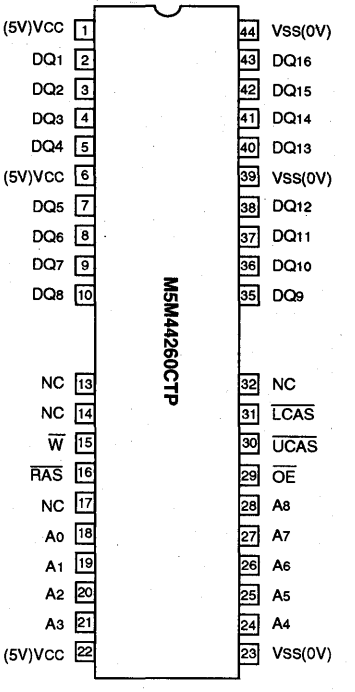
Pin name	Function
A_0~A_8	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

M5M44260CJ,TP-5,-5S : under development

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400mil SOJ)



Outline 44P3W-L (400mil TSOP Nomal Bend)

NC: NO CONNECTION

FUNCTION

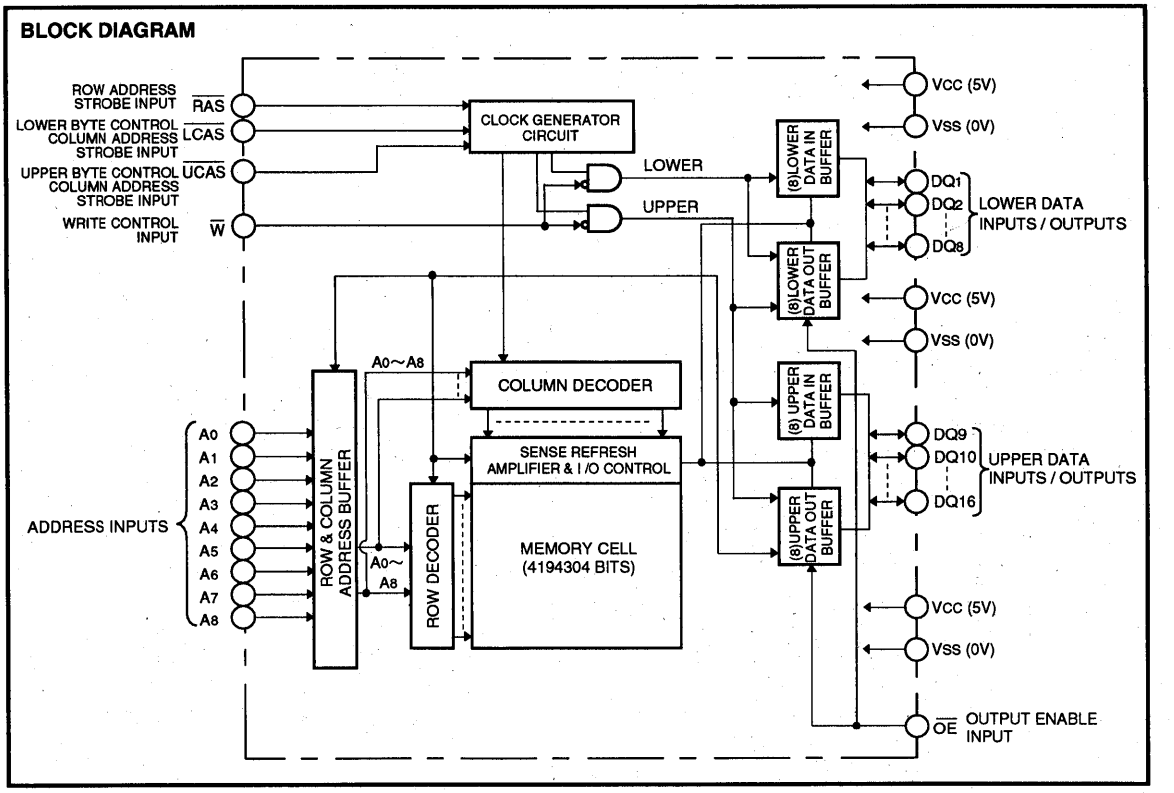
In addition to normal read,write and read-modify-write operations the M5M44260CJ, TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs							Input/Output		Refresh	Remark.
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	DQ1~DQ8	DQ9~DQ16		
Lower byte read	ACT	ACT	NAC	NAC	ACT	APD	APD	DOUT	OPN	YES	Fast page mode identical
Upper byte read	ACT	NAC	ACT	NAC	ACT	APD	APD	OPN	DOUT	YES	
Word read	ACT	ACT	ACT	NAC	ACT	APD	APD	DOUT	DOUT	YES	
Lower byte write	ACT	ACT	NAC	ACT	NAC	APD	APD	DIN	DNC	YES	
Upper byte write	ACT	NAC	ACT	ACT	NAC	APD	APD	DNC	DIN	YES	
Word write	ACT	ACT	ACT	ACT	NAC	APD	APD	DIN	DIN	YES	
$\overline{RAS}$ only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	DNC	ACT	DNC	DNC	DOUT	DOUT	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended *) refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Self refresh *	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	No	

Note : ACT : active, NAC : nonactive, DNC : don' t care, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
V_O	Output voltage		-1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-0.5**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : VIL(min) is -2.0V when pulse width is less than 25ns. (Pulse width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.0V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M44260C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			125	mA
		M5M44260C-6,-6S				110	
		M5M44260C-7,-7S				95	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc -0.5V output open			1.0	
						0.1*	
$I_{CC3(AV)}$	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44260C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			125	mA
		M5M44260C-6,-6S				110	
		M5M44260C-7,-7S				95	
$I_{CC4(AV)}$	Average supply current from Vcc Fast page mode (Note 3,4,5)	M5M44260C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			125	mA
		M5M44260C-6,-6S				110	
		M5M44260C-7,-7S				95	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44260C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			115	mA
		M5M44260C-6,-6S				100	
		M5M44260C-7,-7S				85	
$I_{CC8(AV)}$*	Average supply current from Vcc Extended-refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0～A_8 ≦ 0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=250 μs, t_{RAS}=$t_{RAS\ min}$～1 μs			150	μA
$I_{CC9(AV)}$*	Average supply current from Vcc Self-refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			150	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0～70℃ , Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0～70 ℃, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			8.2		8.2		8.2	ms
tREF	Refresh cycle time *			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	7	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		20		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 22)	126		150		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	86	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	49	10000	55	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	86		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	49		55		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	31		35		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	68		80		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 23)	43		50		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V IH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	71		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 25)	85	100000	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	48		55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

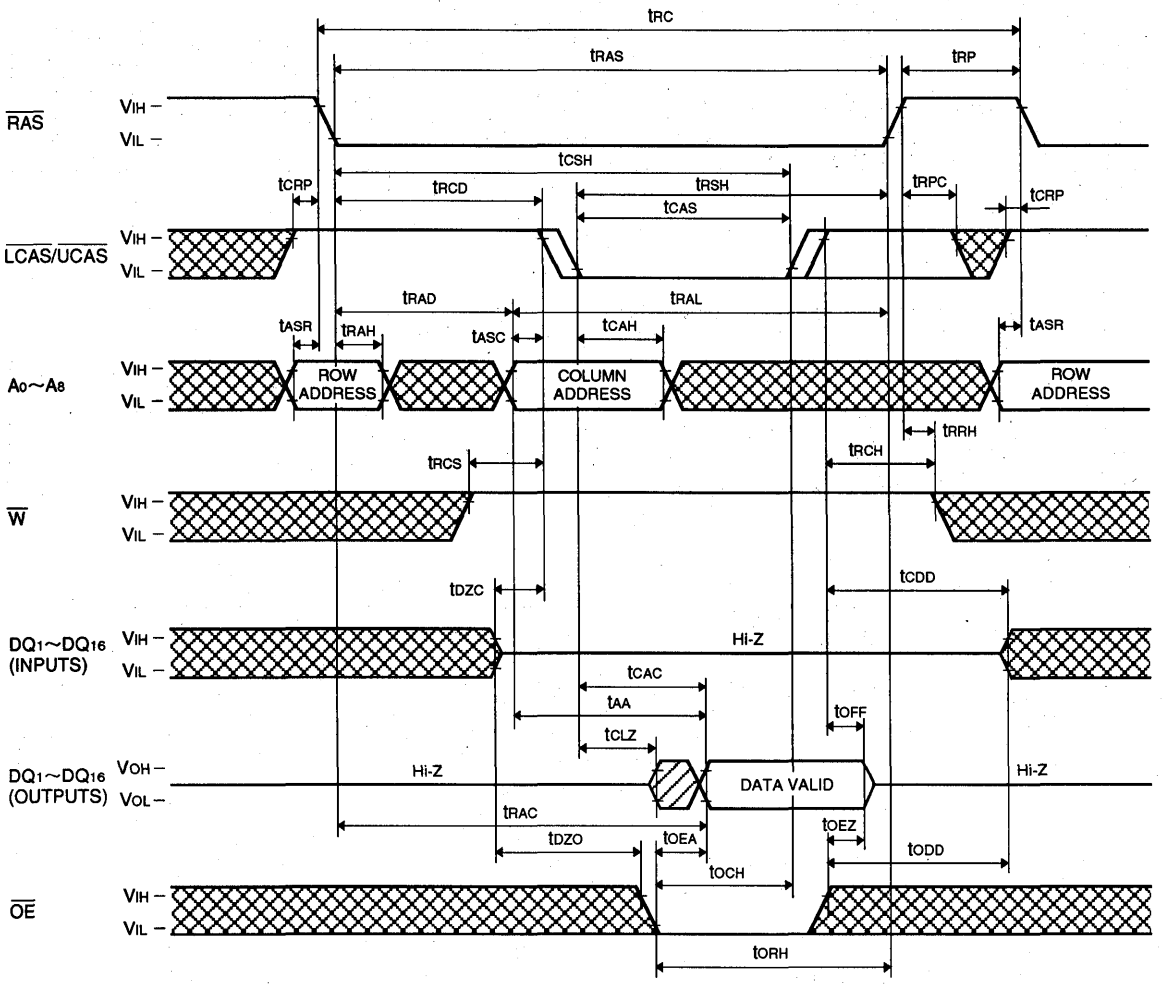
Symbol	Parameter	Limits						Unit
		M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		20		25		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle * (Note 28)

Symbol	Parameter	Limits						Unit
		M5M44260C-5,-5S		M5M44260C-6,-6S		M5M44260C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns

Timing Diagrams (Note 29)
Read Cycle

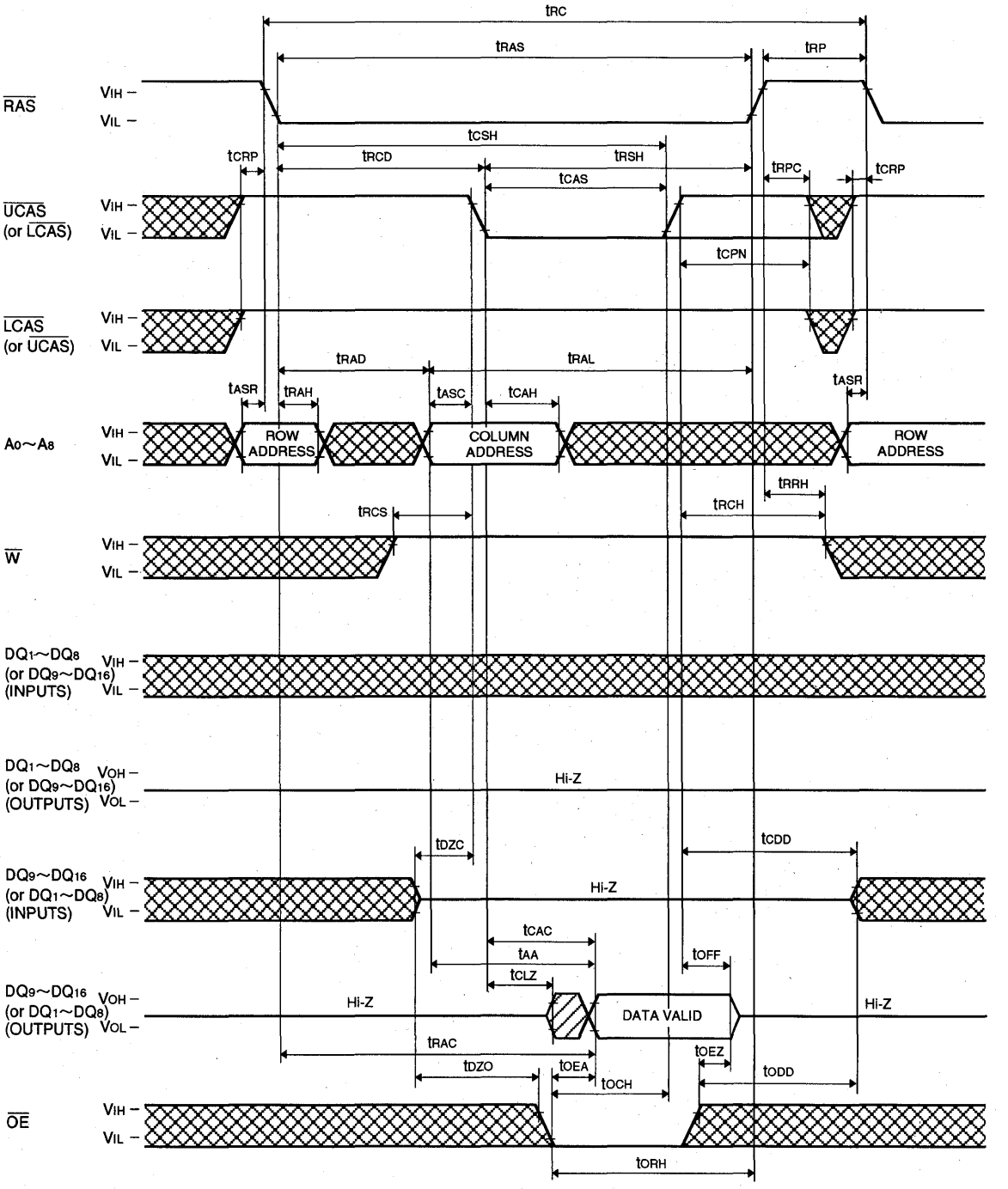


Note 29

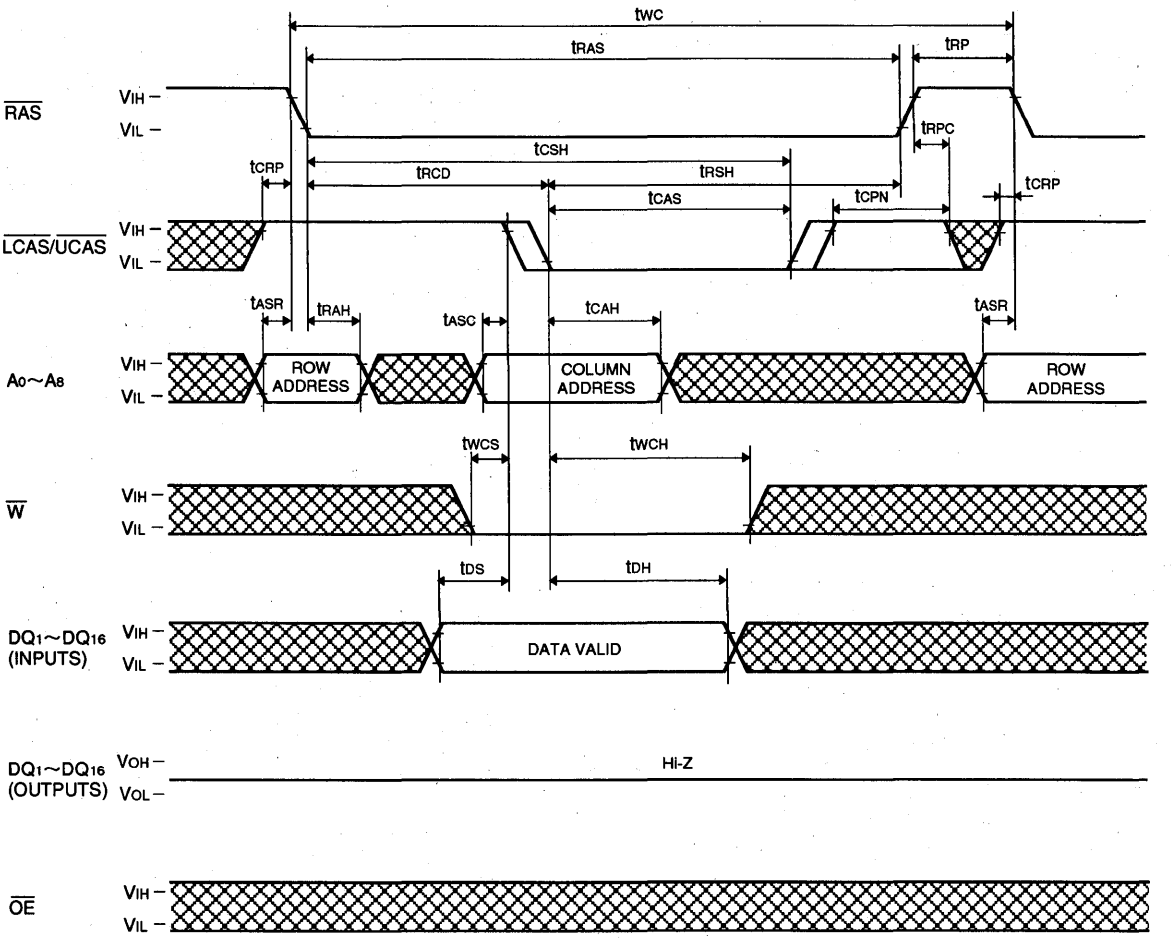
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

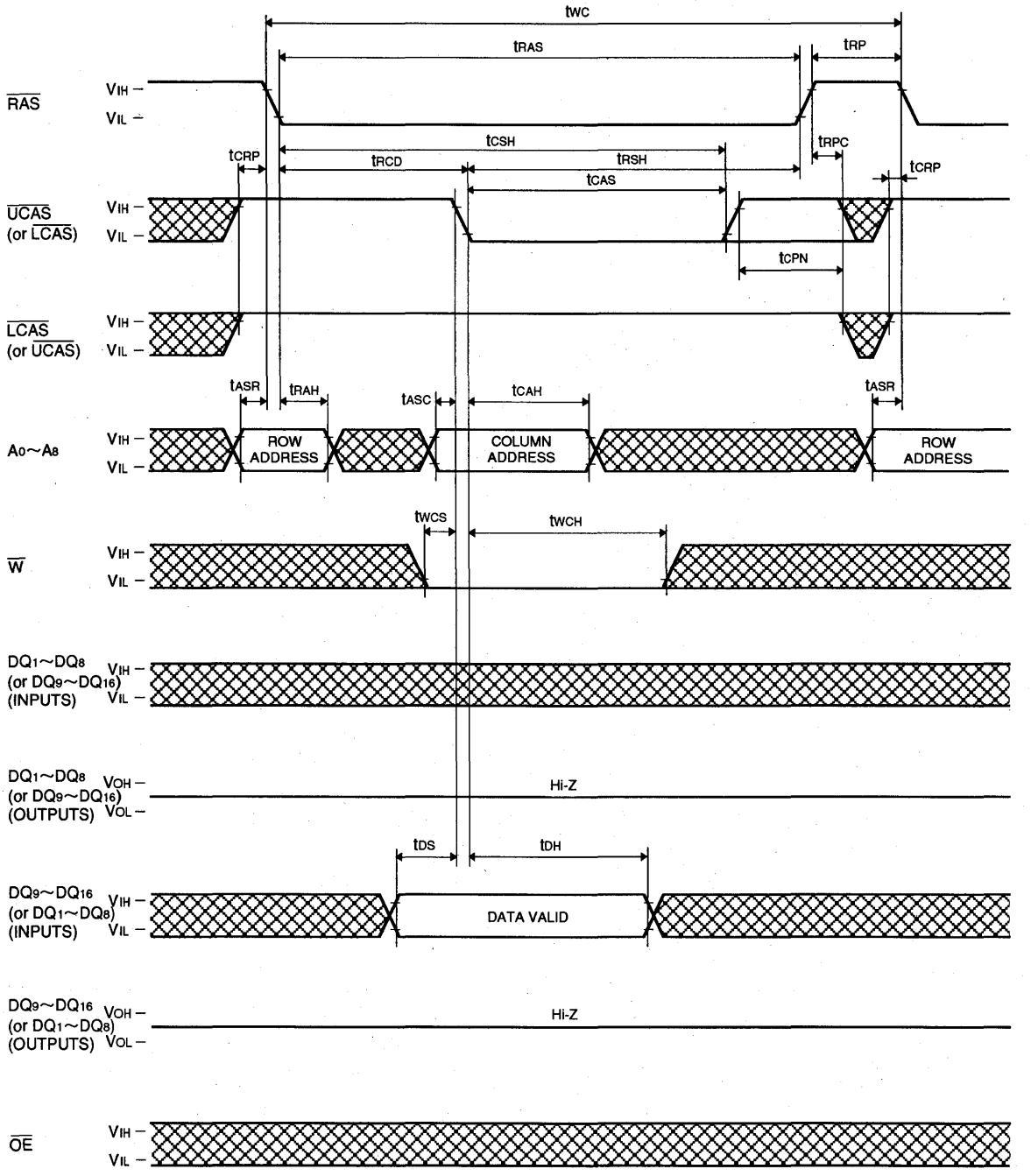
Byte Read Cycle



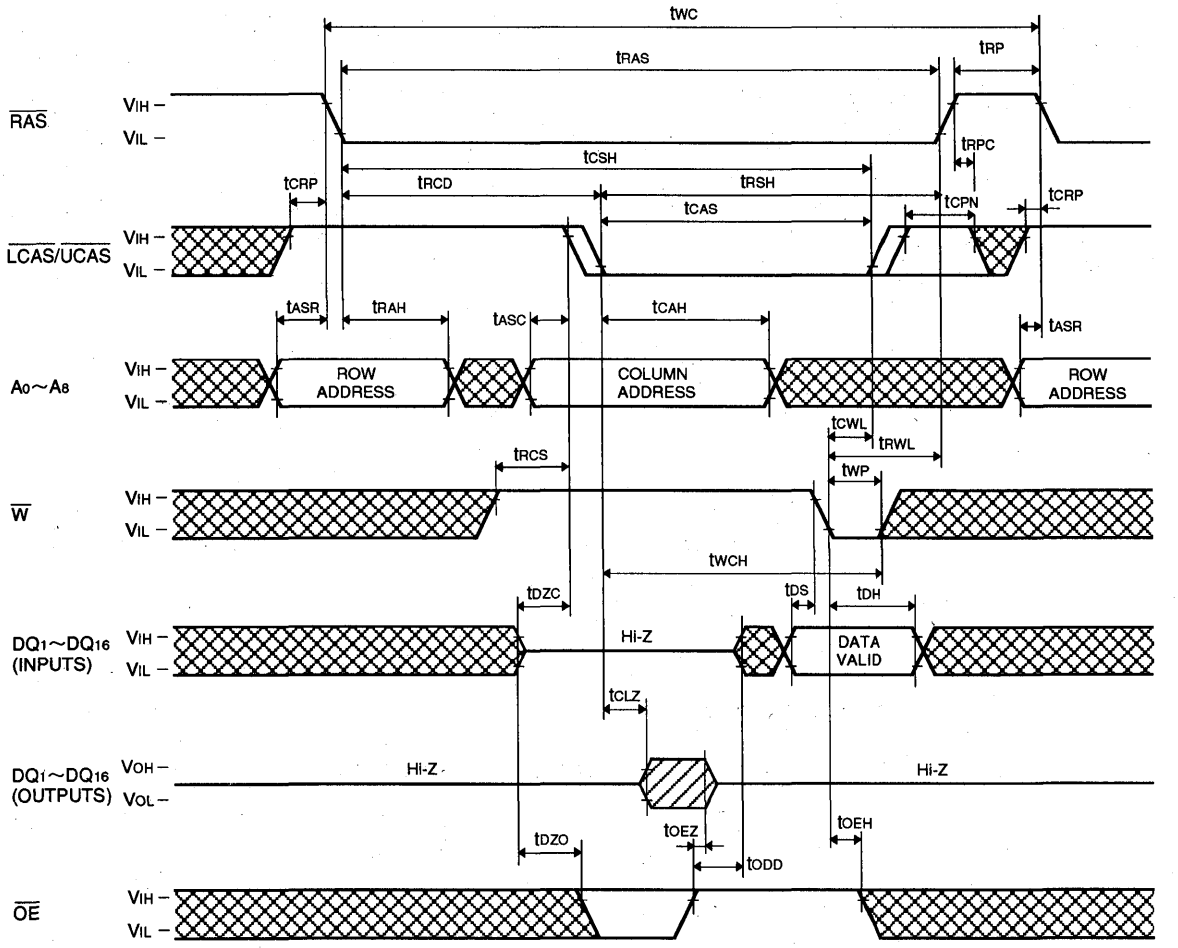
Write Cycle (Early write)



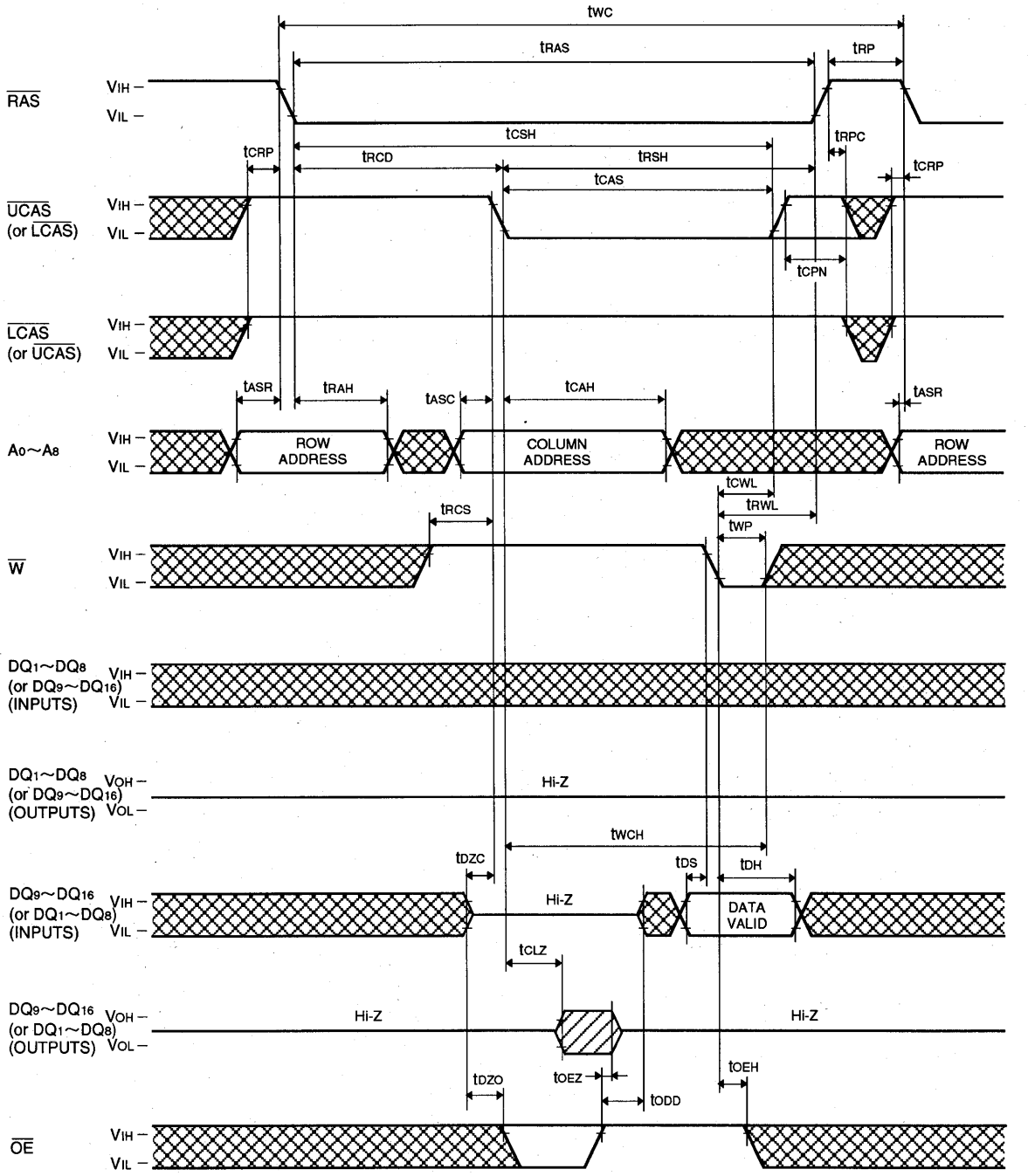
Byte Write Cycle (Early write)



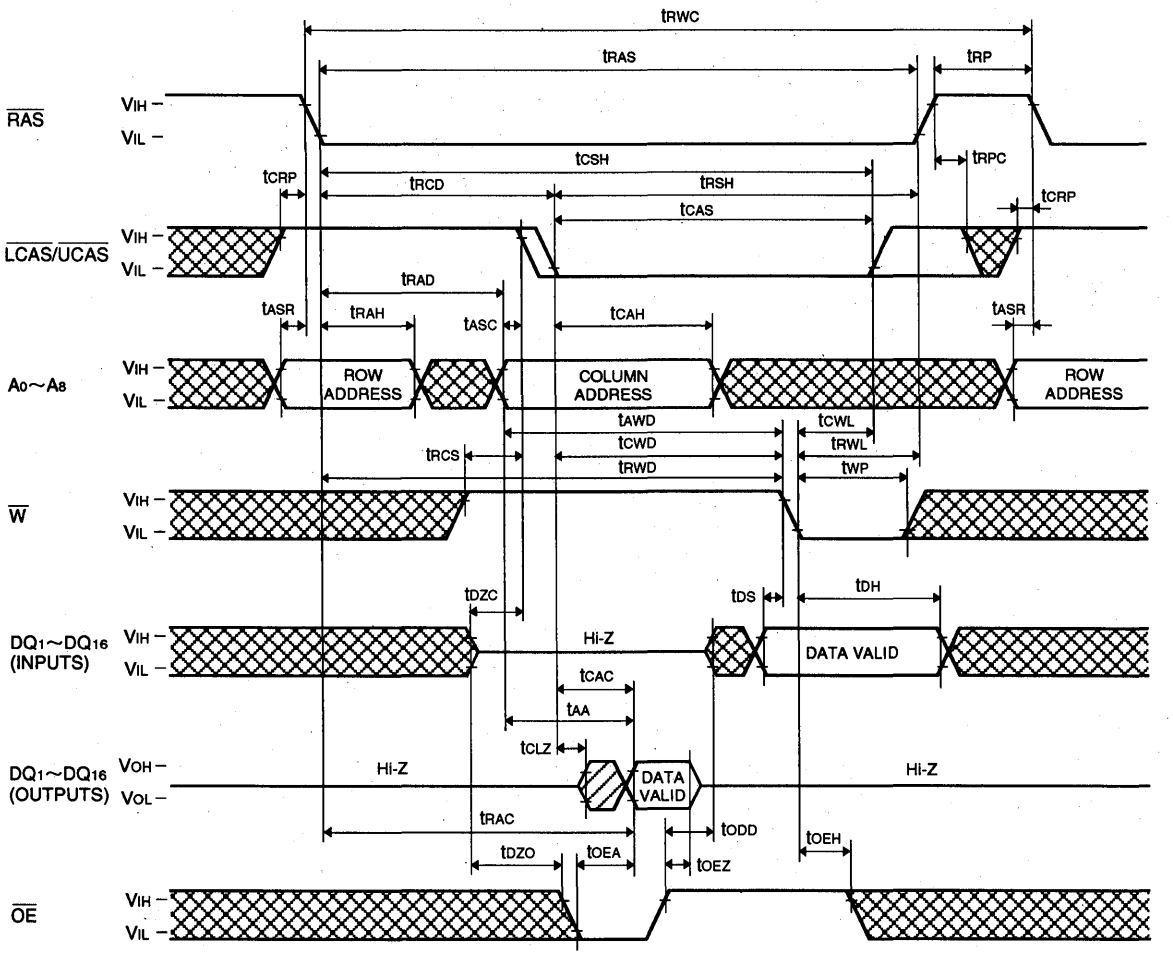
Write Cycle (Delayed write)



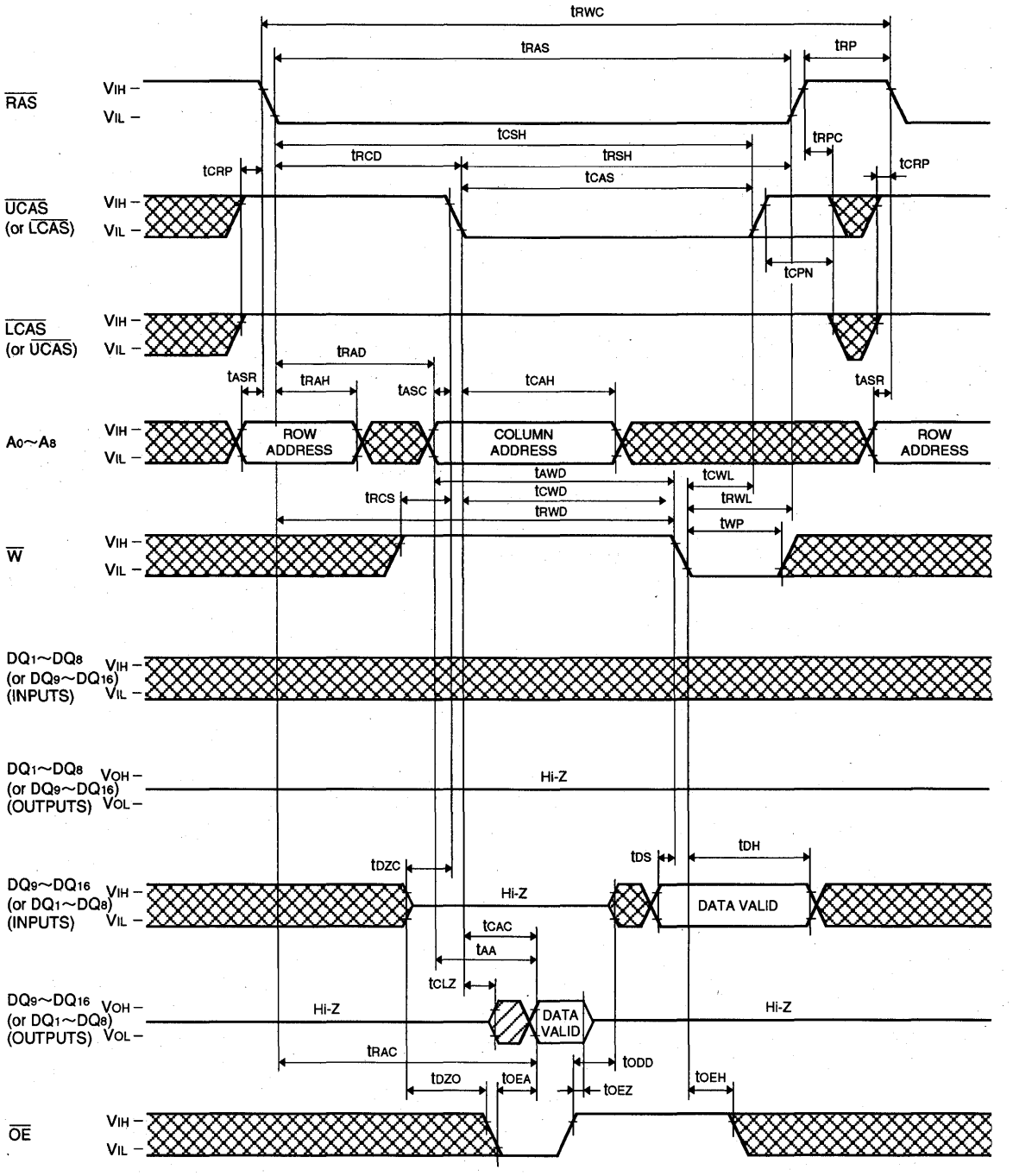
Byte Write Cycle (Delayed write)



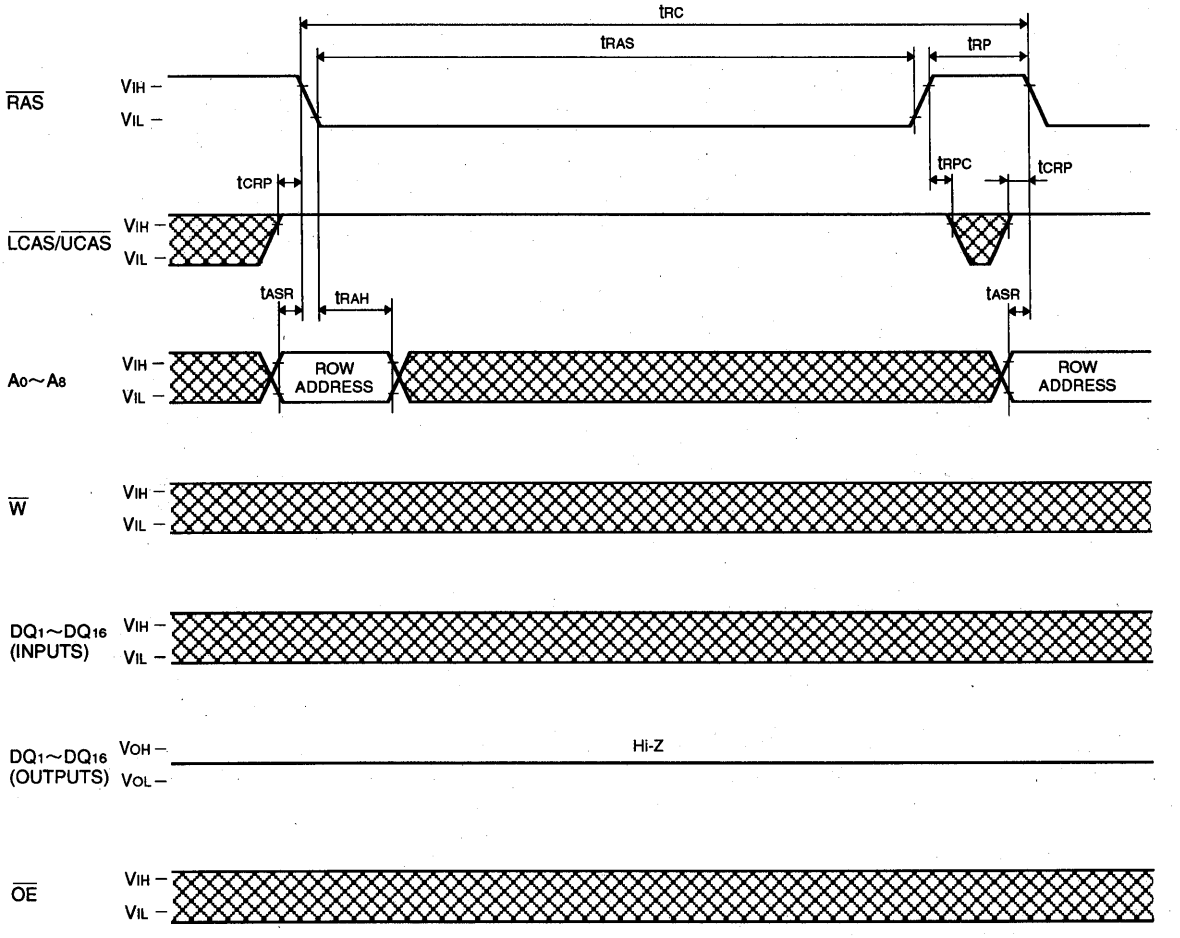
Read-Write, Read-Modify-Write Cycle



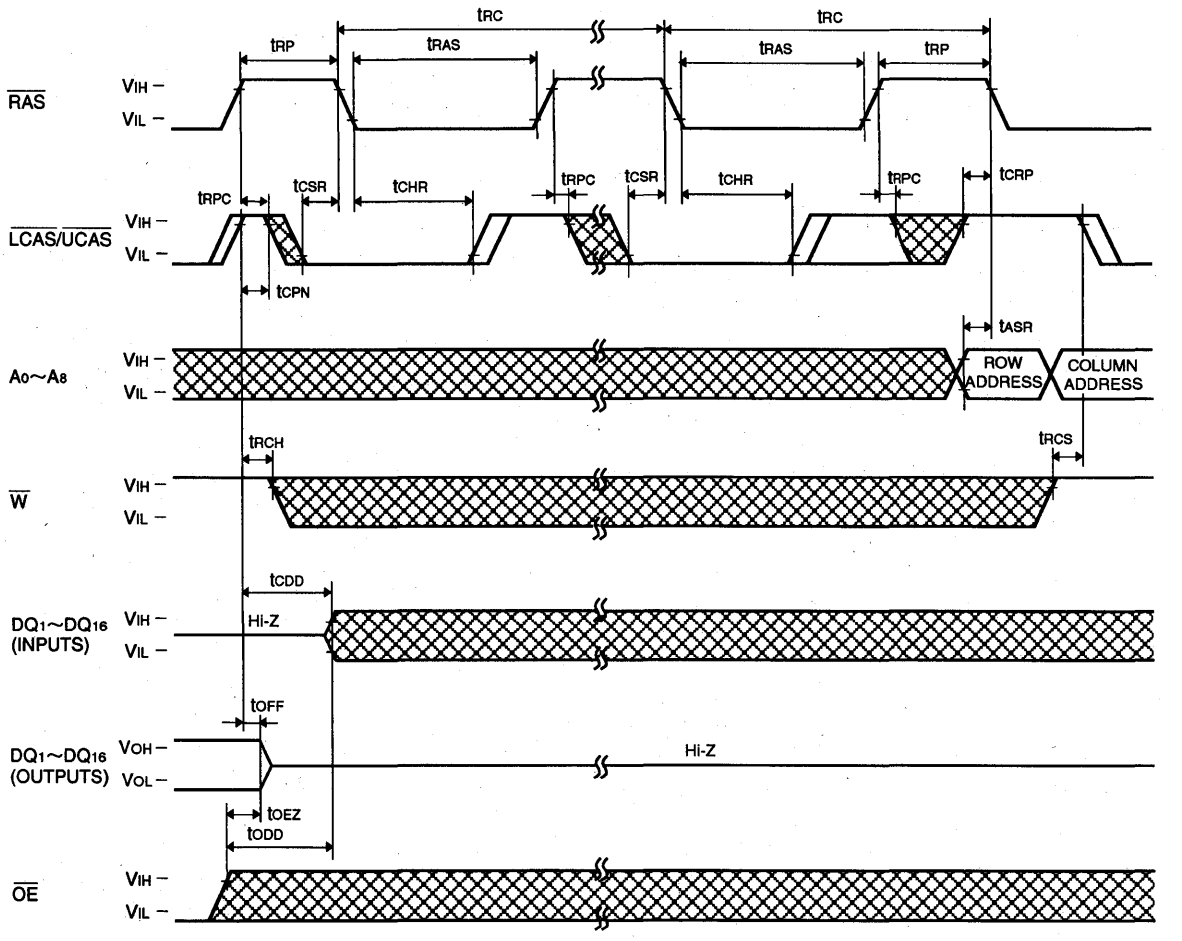
Byte Read-Write, Read-Modify-Write Cycle



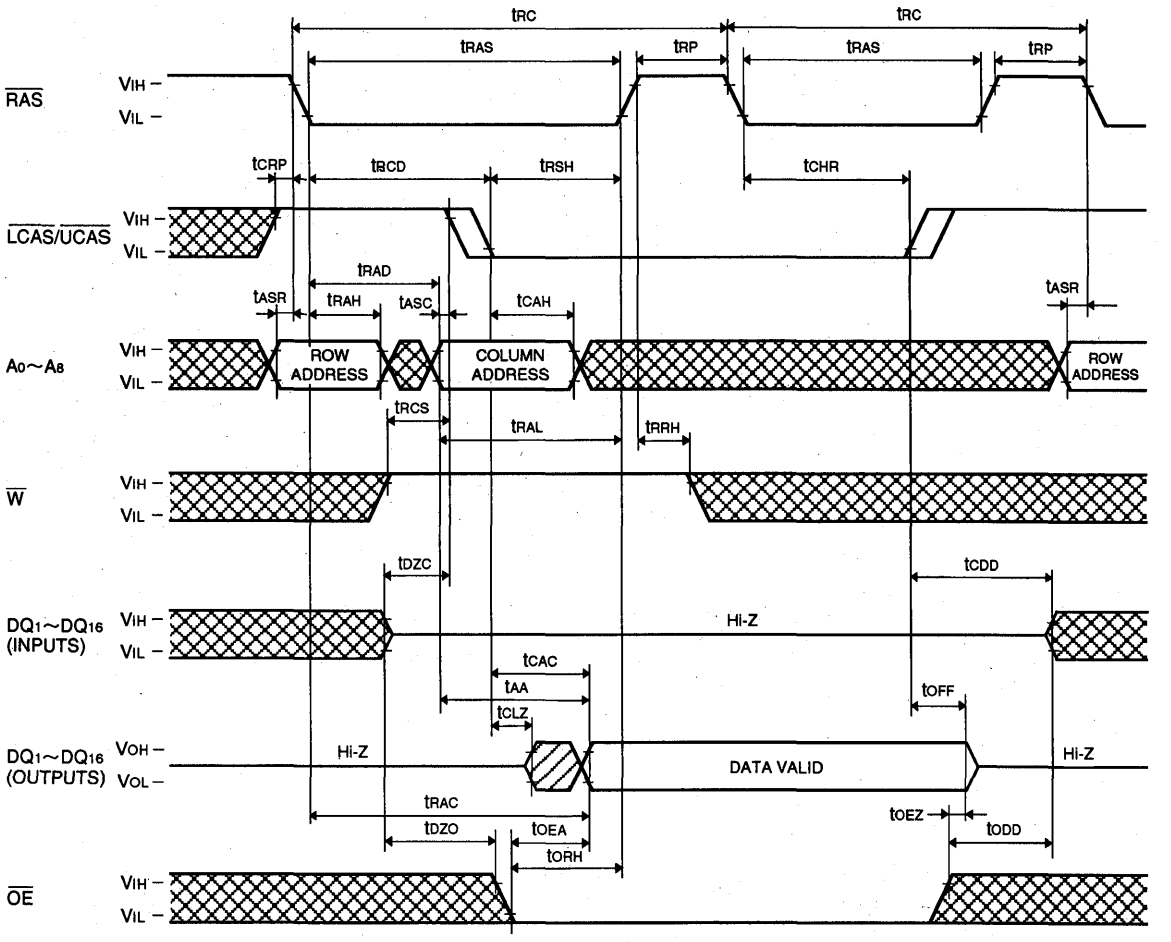
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

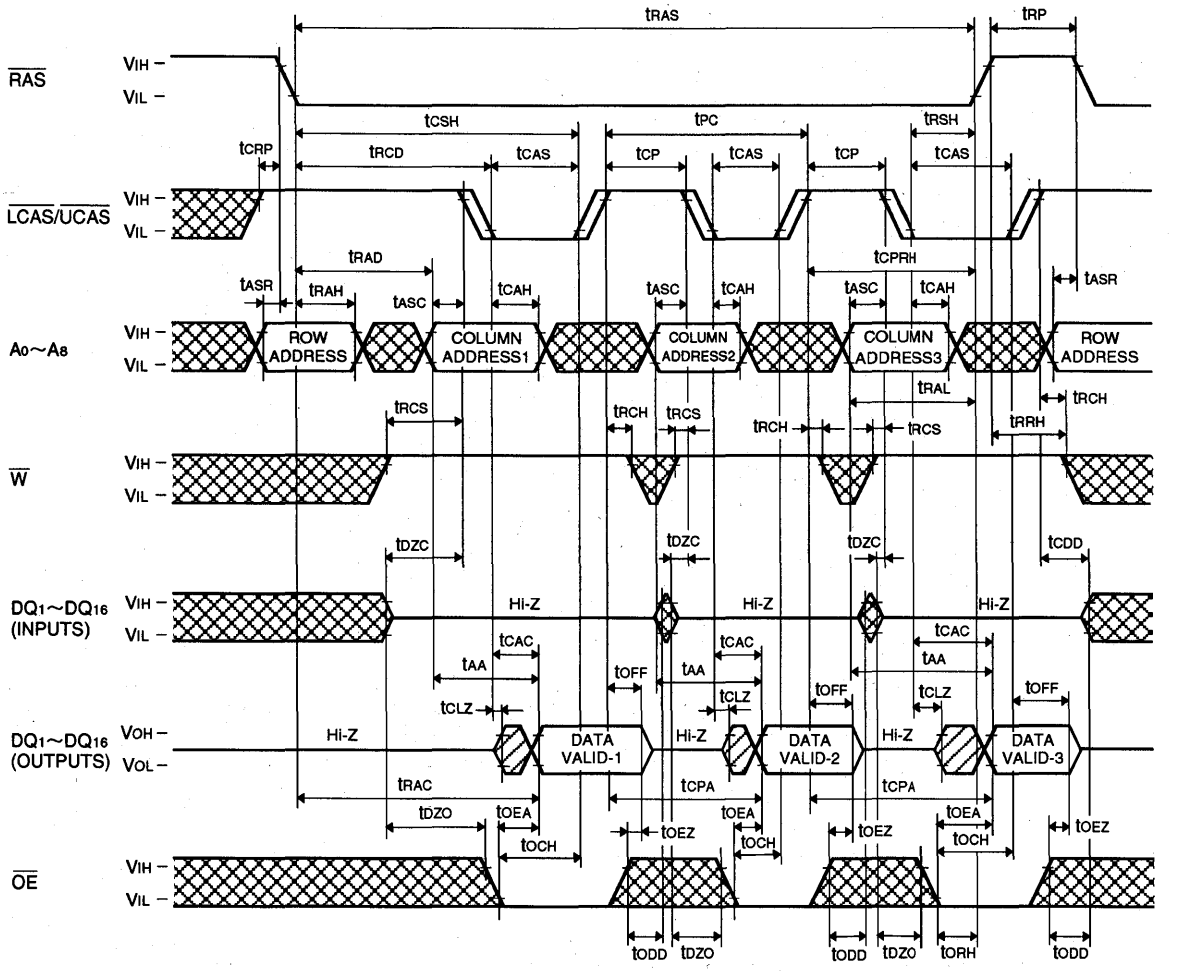


Hidden Refresh Cycle (Read) (Note 30)

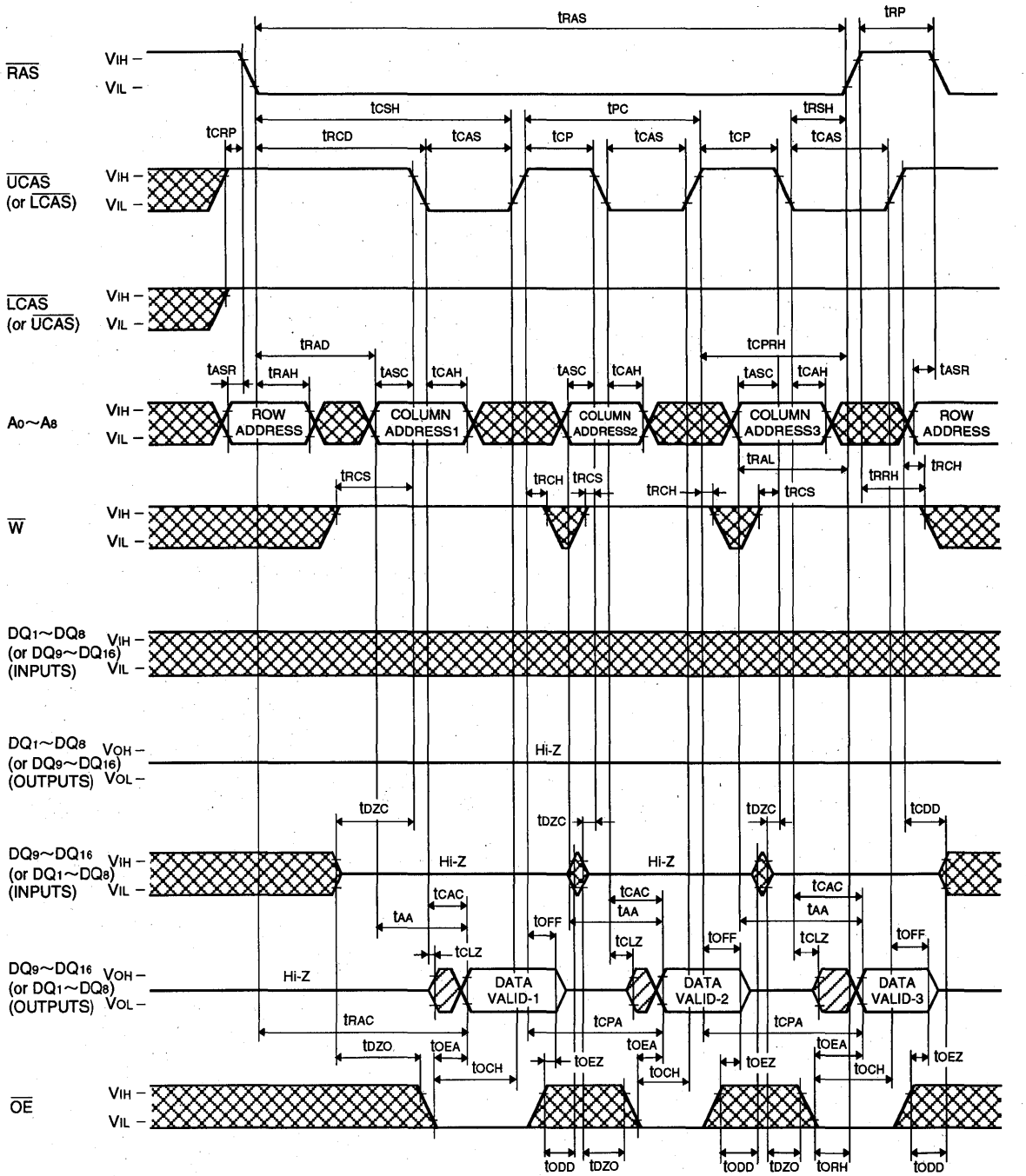


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

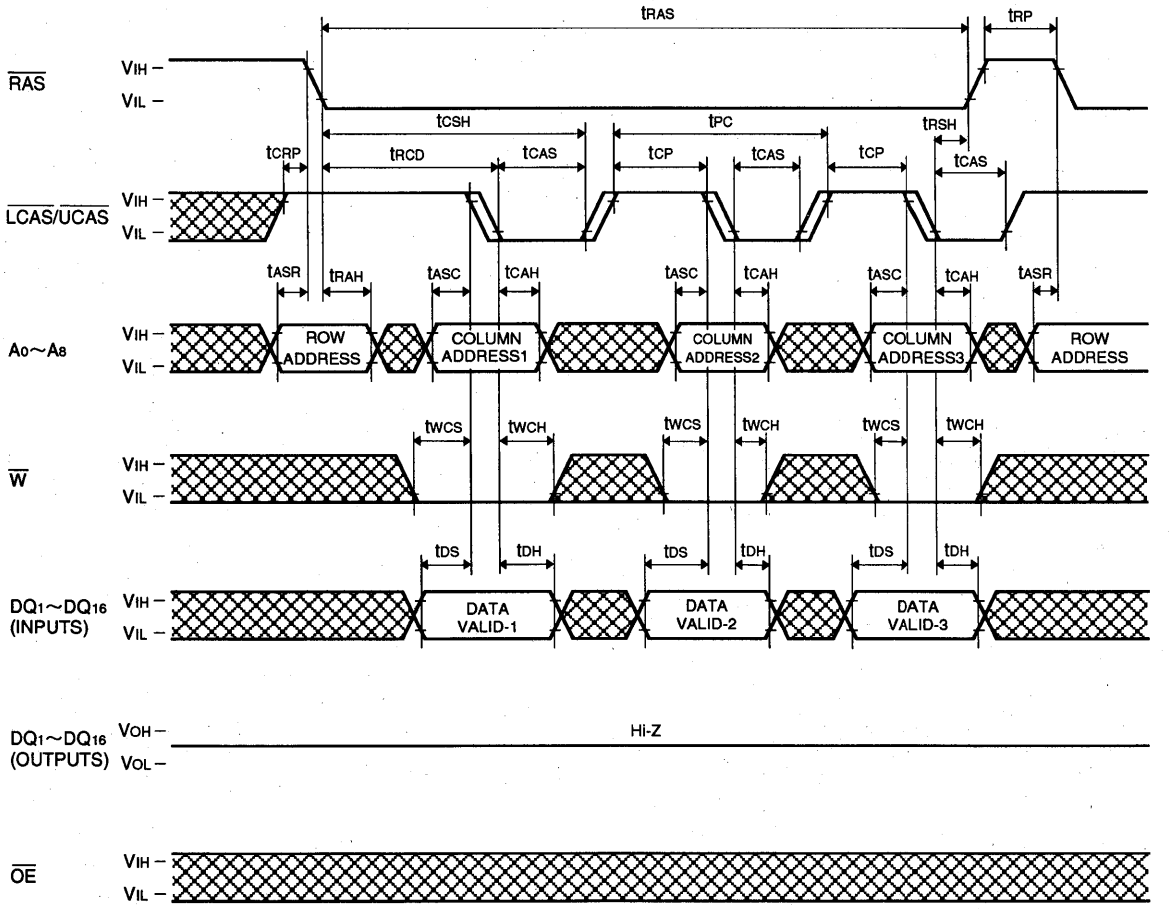
Fast Page Mode Read Cycle



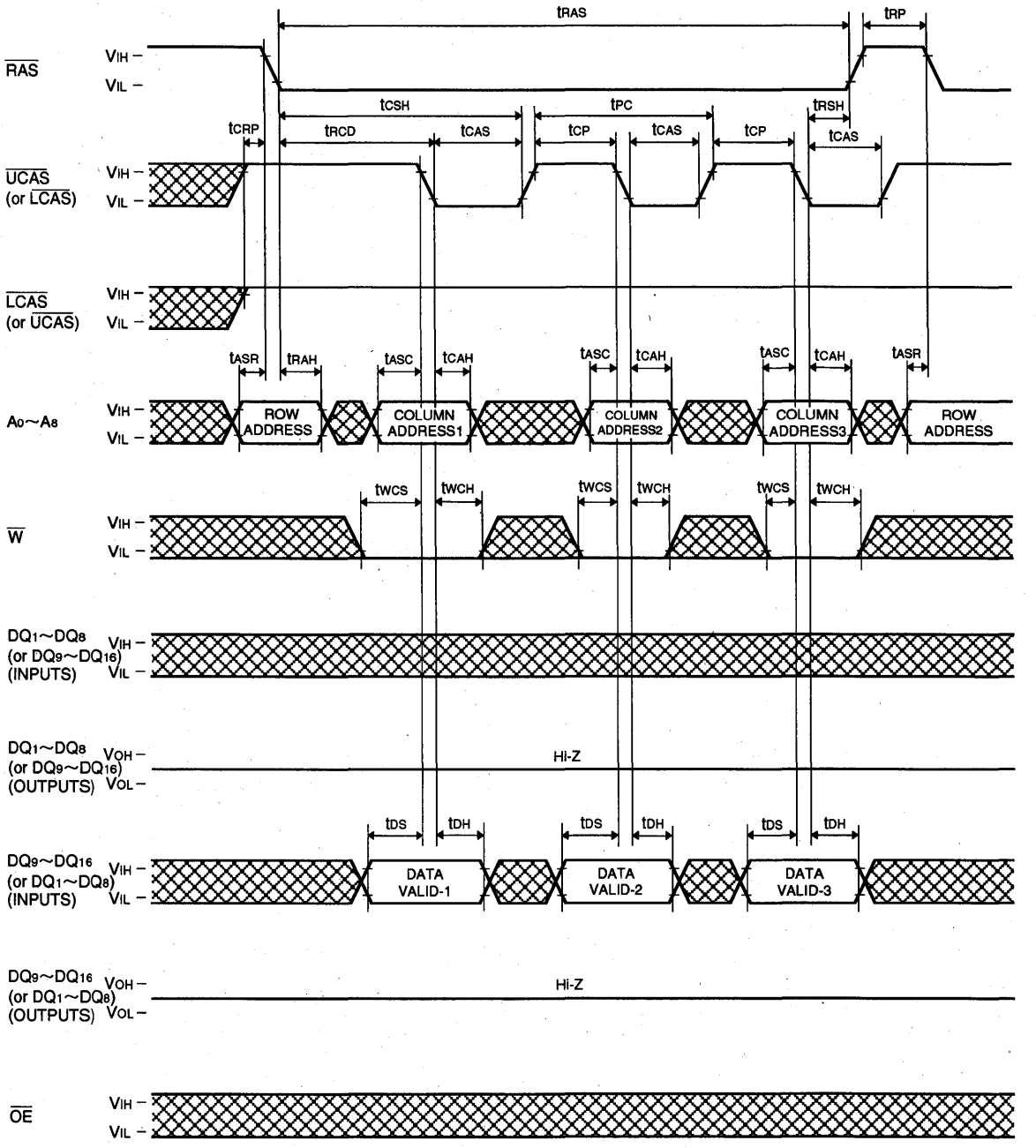
Fast Page Mode Byte Read Cycle



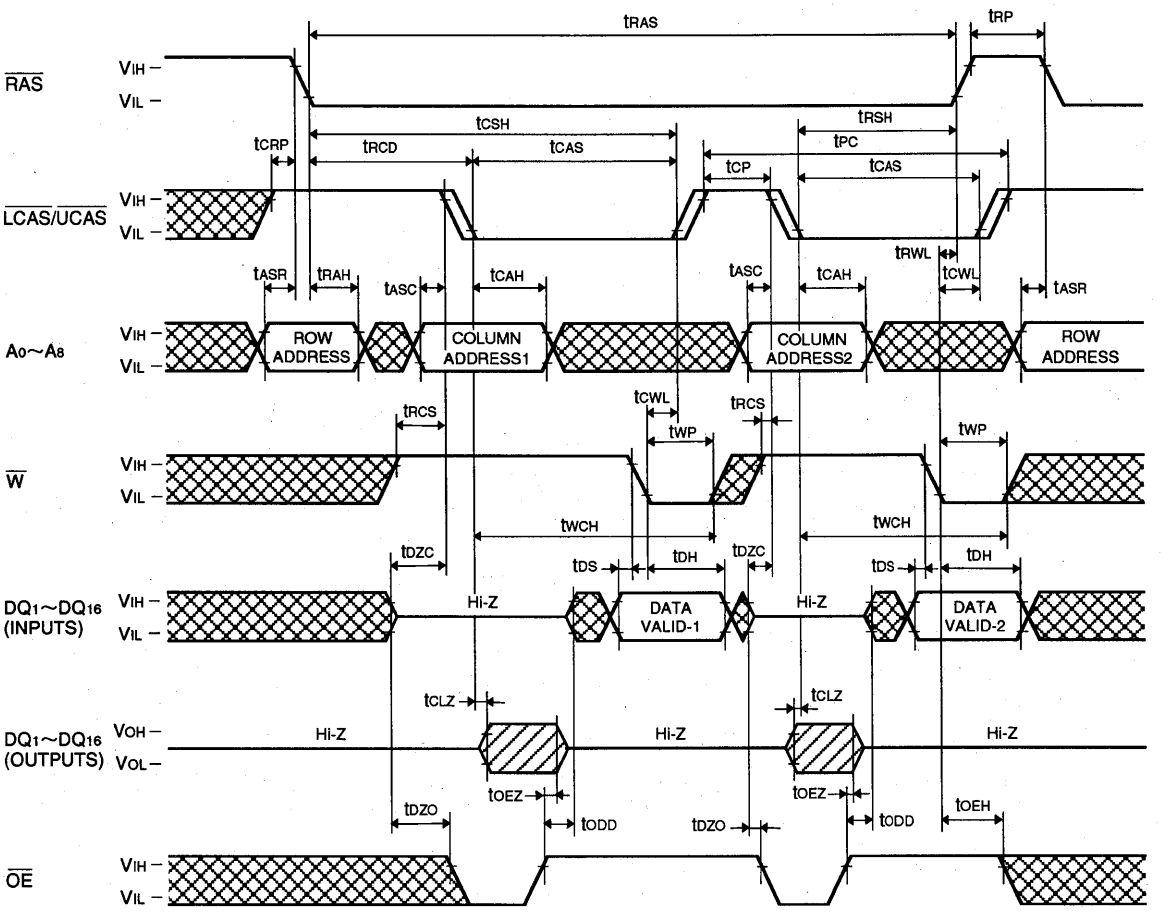
Fast Page Mode Write Cycle (Early Write)



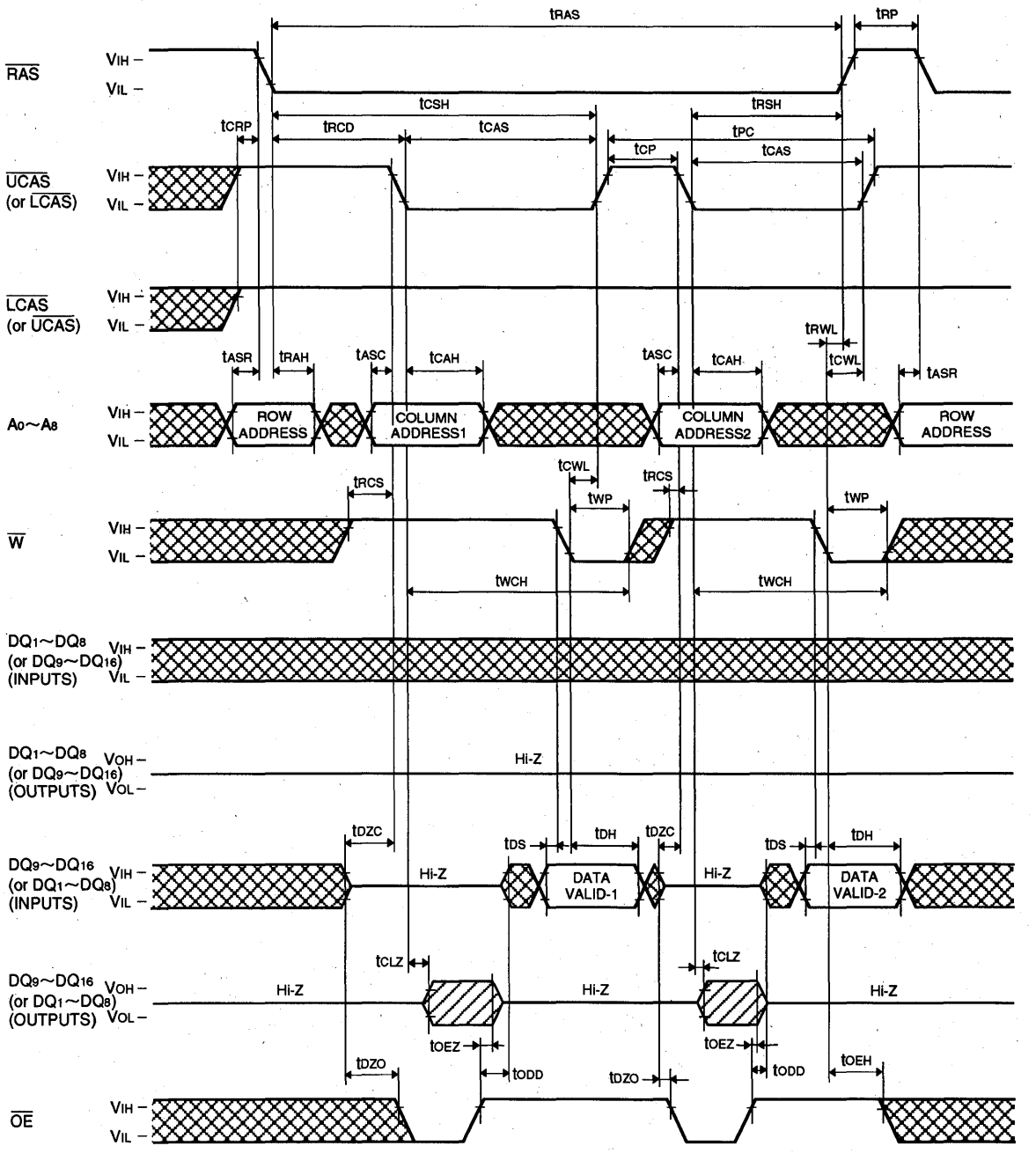
Fast Page Mode Byte Write Cycle (Early Write)



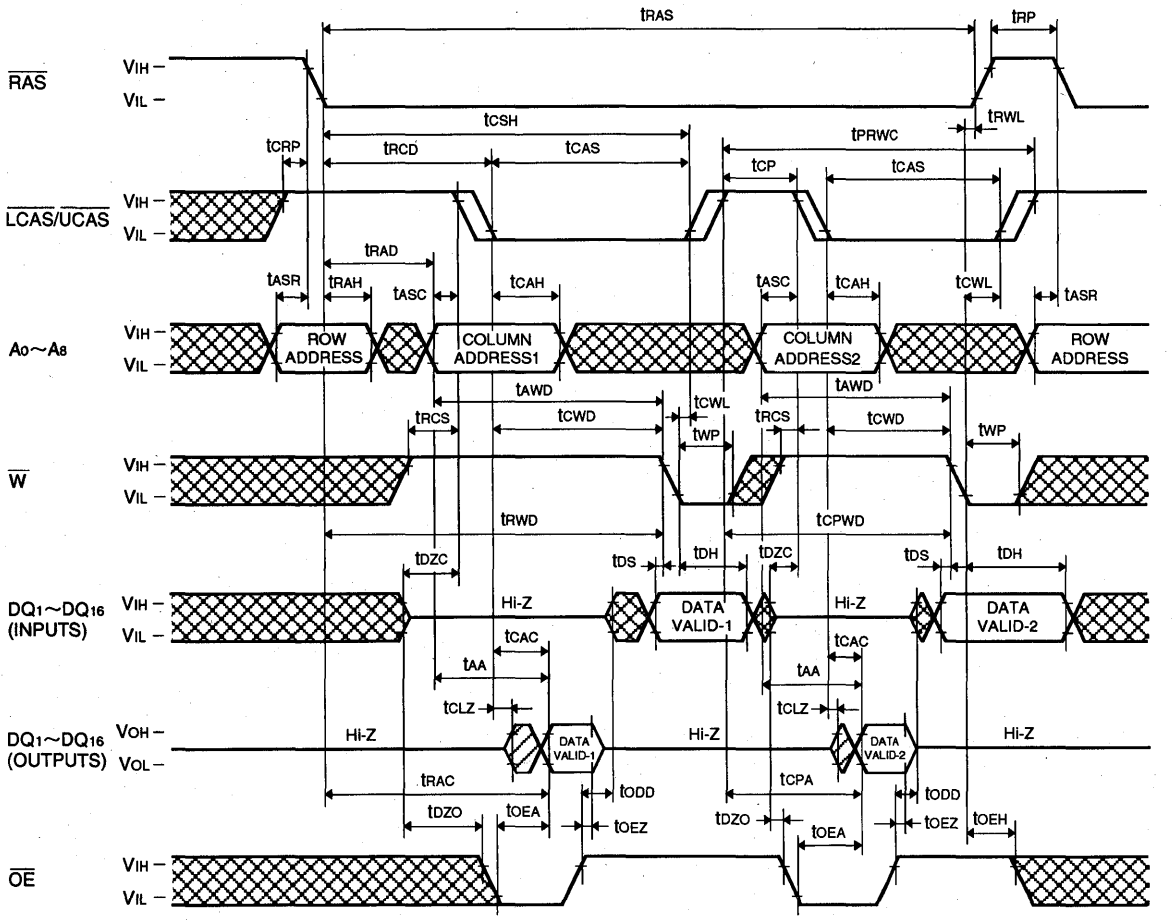
Fast-Page Mode Write Cycle (Delayed Write)



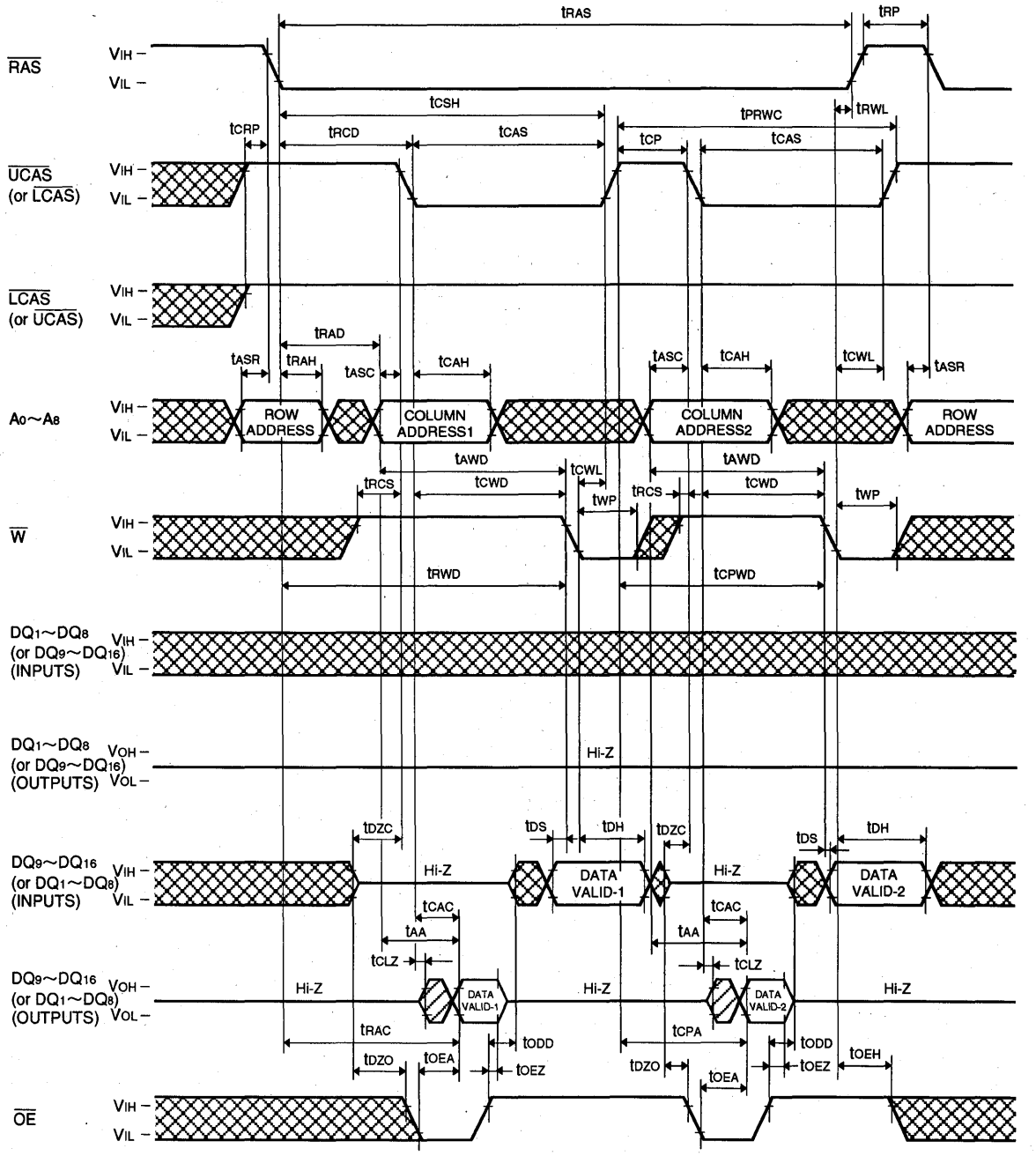
Fast-Page Mode Byte Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Byte Read-Write, Read-Modify-Write Cycle



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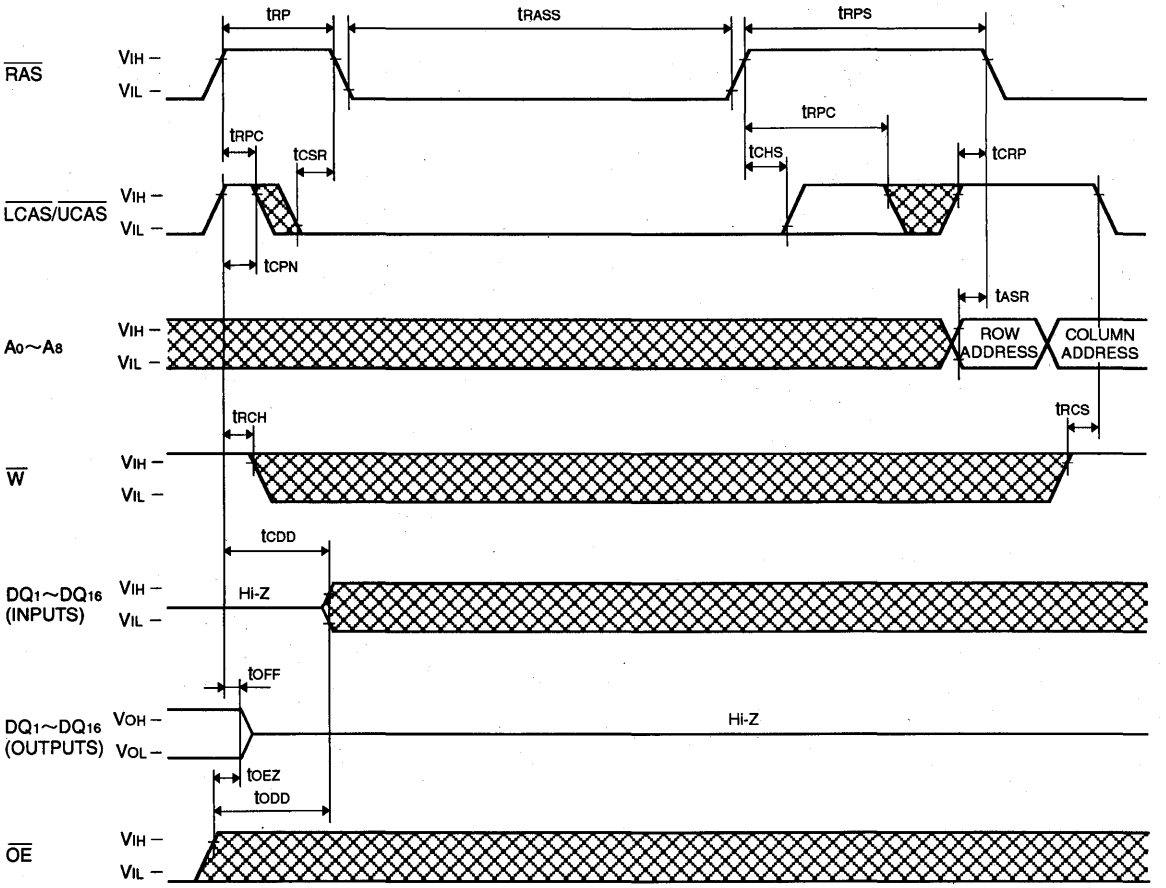
Self Refresh Cycle * (Note28)



Note 28 : Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing Diagram

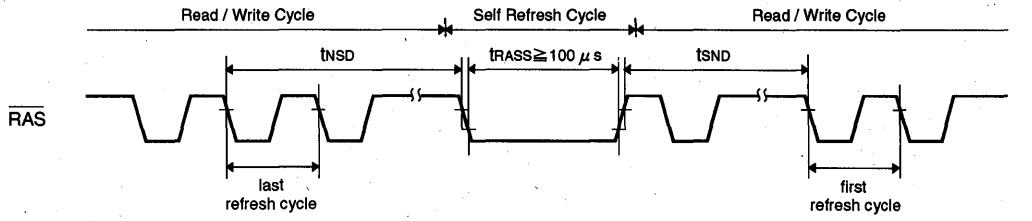
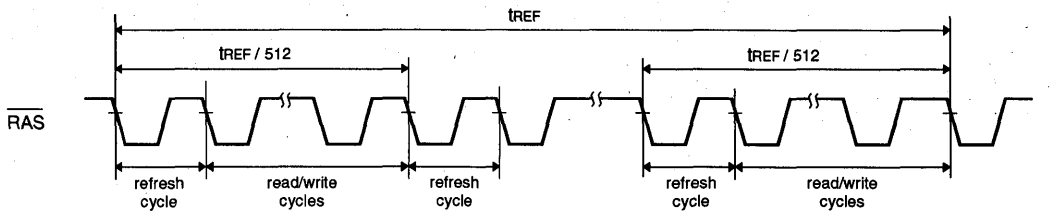


Table 2

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR distributed refresh	$t_{NSD} \leqq 250\ \mu s$	$t_{SND} \leqq 250\ \mu s$
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250 μs max.) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 8.2 ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation
(A) Timing diagram

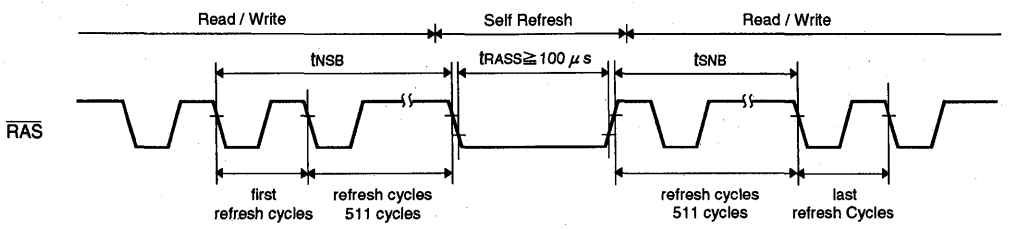
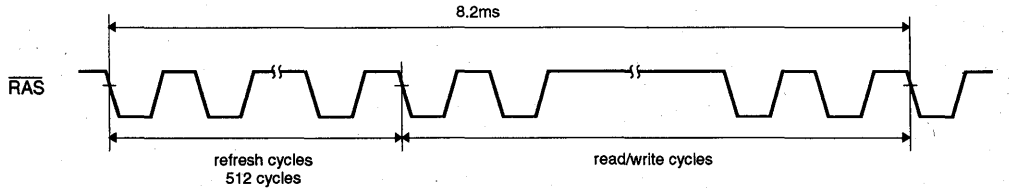


Table 3

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR burst refresh	tNSB≦8.2ms	tSNB≦8.2ms
RAS only burst refresh	tNSB+tSNB≦8.2ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of RAS only burst refresh

All combination of nine row address signals (A_0~A_8) are selected during 512 continuous RAS only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 RAS only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

M5M44265CJ,TP-5,-6,-7, -5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for the buffer memory systems of personal computer graphics and HDD where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44265CXX-5,-5S	50	13	25	13	90	625
M5M44265CXX-6,-6S	60	15	30	15	110	550
M5M44265CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 40pin SOJ, 44 pin TSOP (II)
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max)*
- Operating power dissipation
  - M5M44265Cxx-5,-5S ---------- 688mW (Max)
  - M5M44265Cxx-6,-6S ---------- 605mW (Max)
  - M5M44265Cxx-7,-7S ---------- 523mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 150 μA (Max)
- Extended refresh capability
  - Extended refresh current ---------- 150 μA (Max)
- Hyper-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 128ms (A_0~A_8)*
- Byte or word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

*: Applicable to self refresh version (M5M44265CJ,TP-5S,-6S,-7S : option) only

APPLICATION

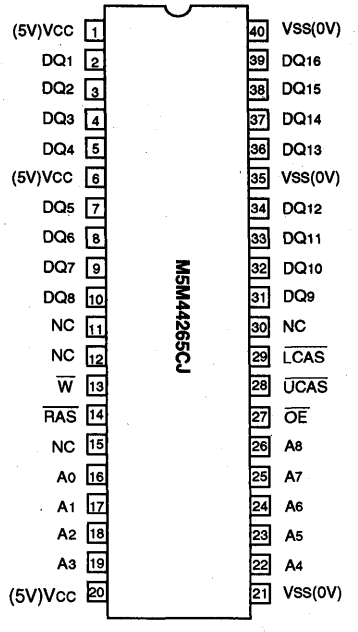
Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT

PIN DESCRIPTION

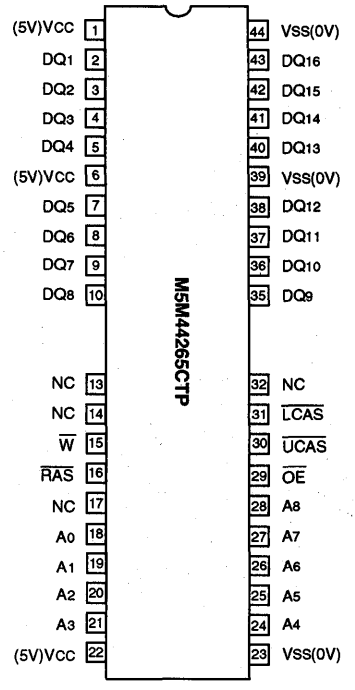
Pin name	Function
A_0~A_8	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+5V)
V_{SS}	Ground (0V)

M5M44265CJ,TP-5,-5S : under development

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400mil SOJ)



Outline 44P3W-L (400mil TSOP Nomal Bend)

NC: NO CONNECTION

MITSUBISHI ELECTRIC

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

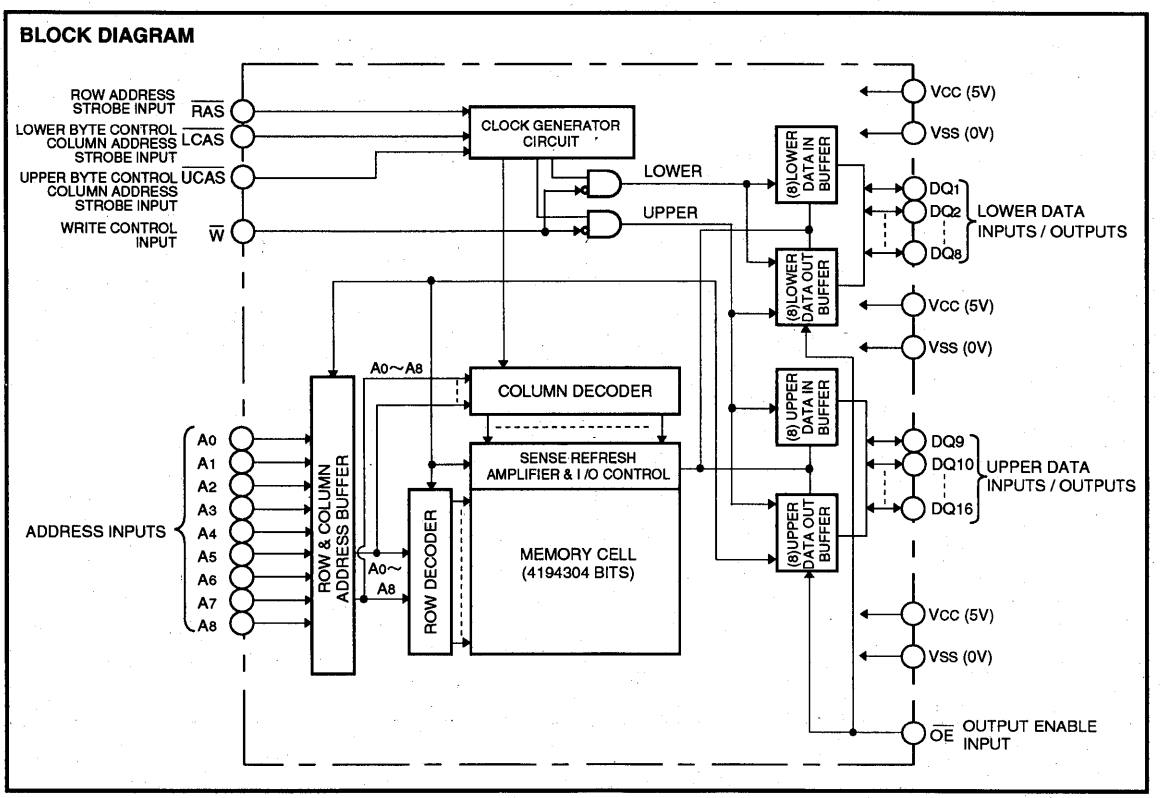
In addition to Hyper page mode, normal read, write and read-modify-write operations the M5M44265CJ, TP provides a number of other functions, e.g., $\overline{RAS}$-only refresh and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_1 \sim DQ_8$	$DQ_9 \sim DQ_{16}$
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$ only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ (Extended *) refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Self refresh *	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, OPN : open

BLOCK DIAGRAM



EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
V_O	Output voltage		-1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-0.5**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min) is -2.0V when pulse width is less than 25ns. (Pulse width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.0V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M44265C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			125	mA
		M5M44265C-6,-6S				110	
		M5M44265C-7,-7S				95	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.5V output open			1.0	
						0.1*	
$I_{CC3(AV)}$	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44265C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			125	mA
		M5M44265C-6,-6S				110	
		M5M44265C-7,-7S				95	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper page mode (Note 3,4,5)	M5M44265C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			125	mA
		M5M44265C-6,-6S				110	
		M5M44265C-7,-7S				95	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44265C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			115	mA
		M5M44265C-6,-6S				100	
		M5M44265C-7,-7S				85	
$I_{CC8(AV)}$*	Average supply current from Vcc Extended-refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0～A_8 ≦ 0.2V or ≧Vcc-0.2V DQ=open t_{RC}=250 μs, t_{RAS}=$t_{RAS\ min}$～1 μs			150	μA
$I_{CC9(AV)}$*	Average supply current from Vcc Self-refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			150	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0~70℃ , Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70 ℃, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		28		33		38	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$	(Note 13)	5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1TTL and 50pF.
The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			8.2		8.2		8.2	ms
tREF	Refresh cycle time *			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		8		10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
t_{WP}	Write pulse width		8		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for Hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Hyper Page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper page mode read write / read modify write cycle time	57		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ pulse width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ pulse width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper page mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

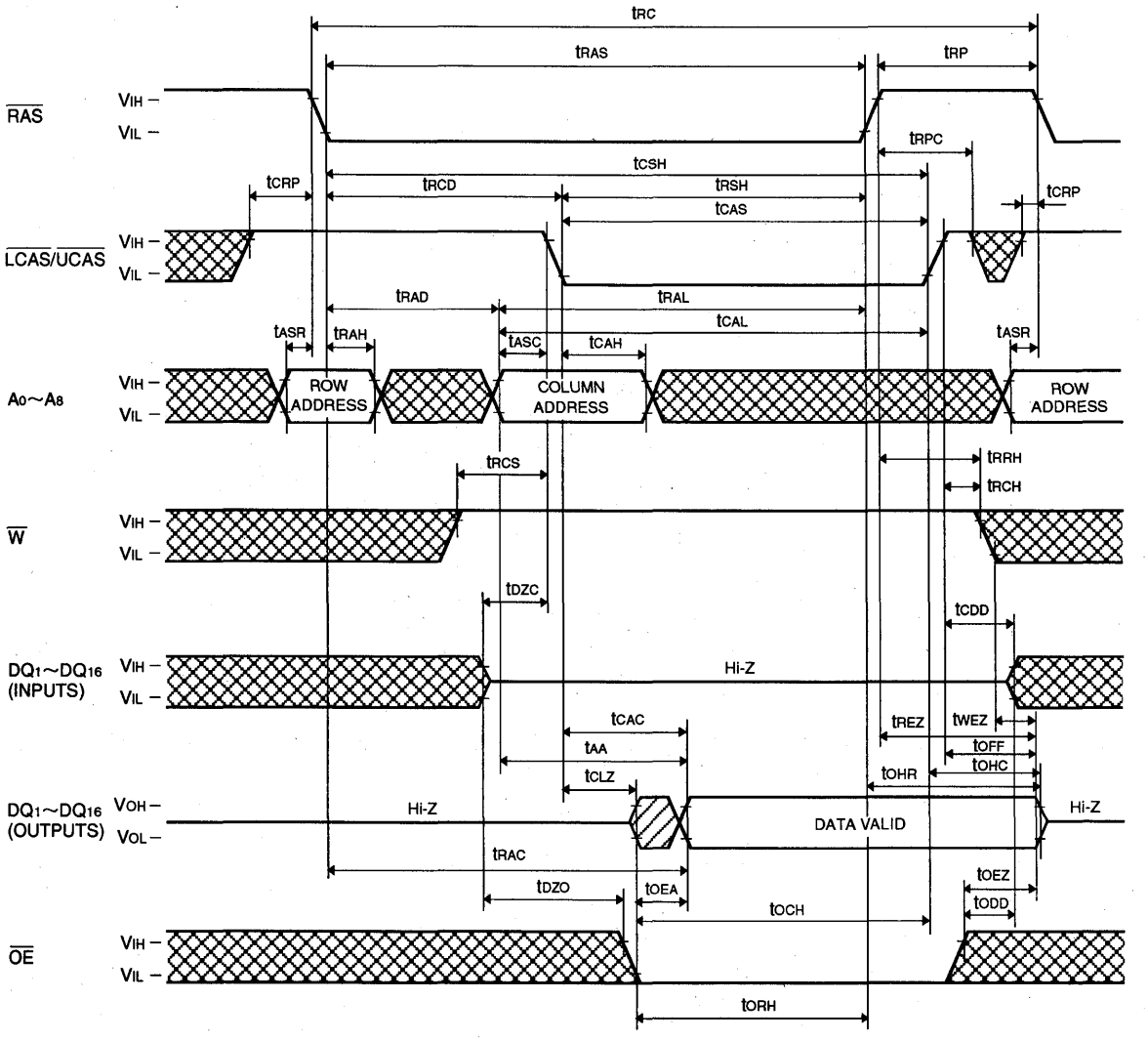
Symbol	Parameter	Limits						Unit
		M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle * (Note 30)

Symbol	Parameter	Limits						Unit
		M5M44265C-5,-5S		M5M44265C-6,-6S		M5M44265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns

Timing Diagrams (Note 31)
Read Cycle

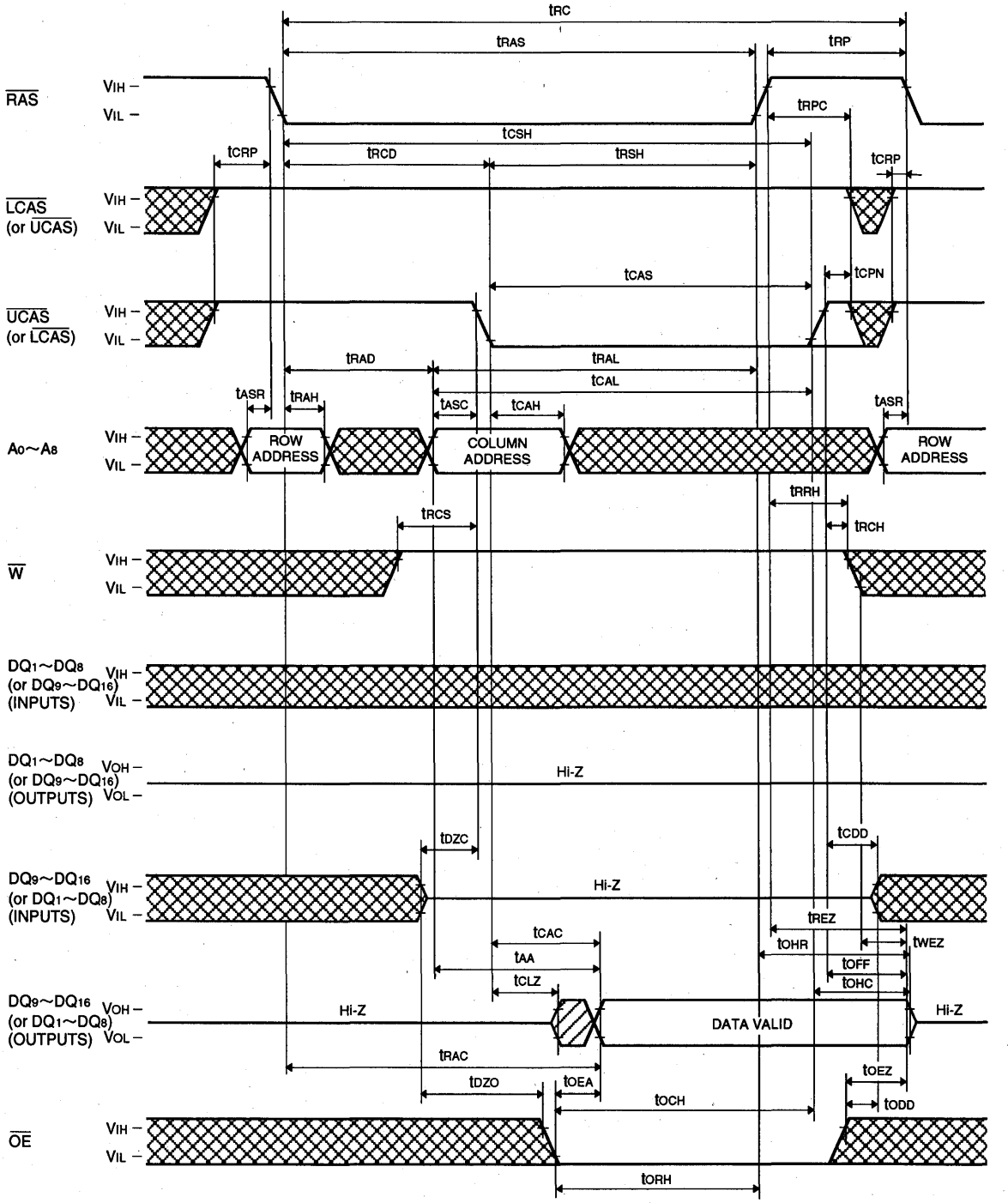


Note 31

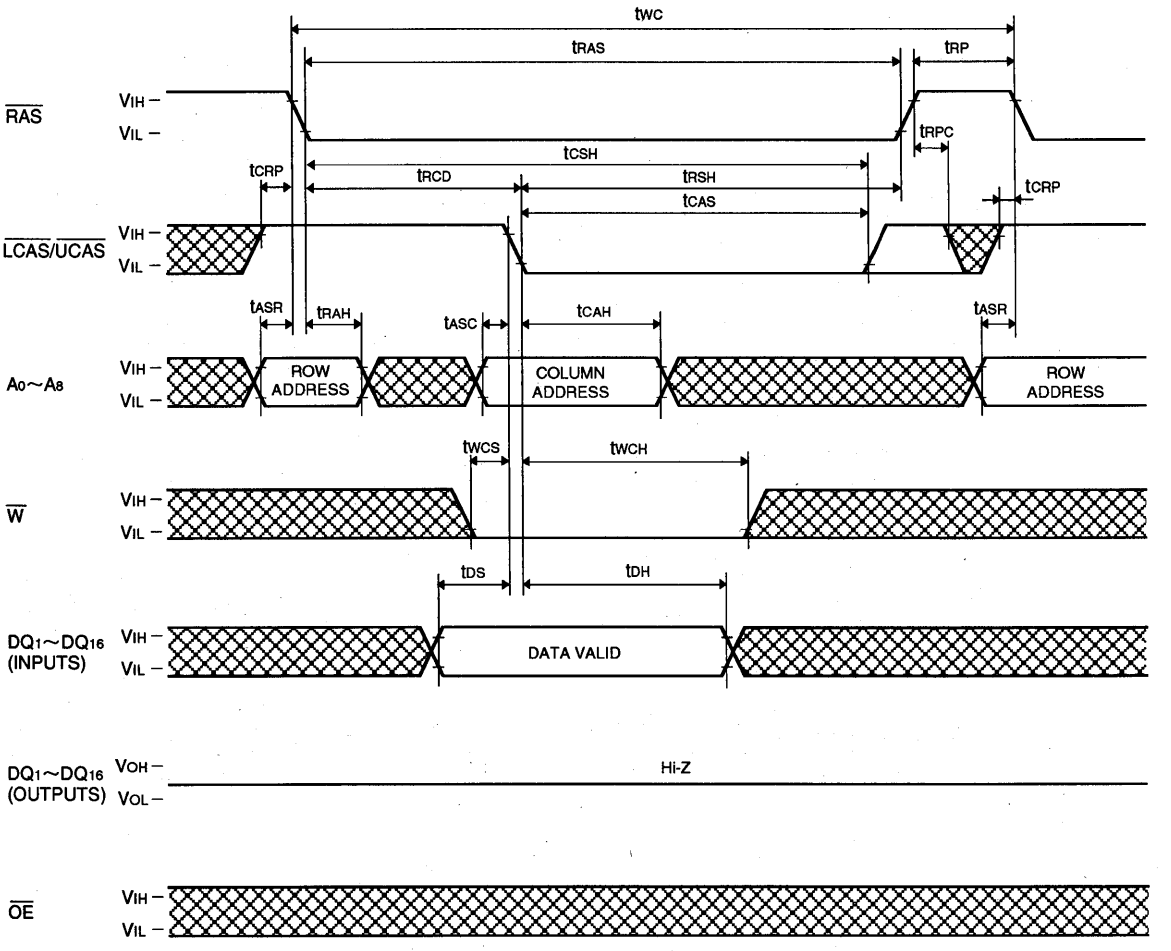
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

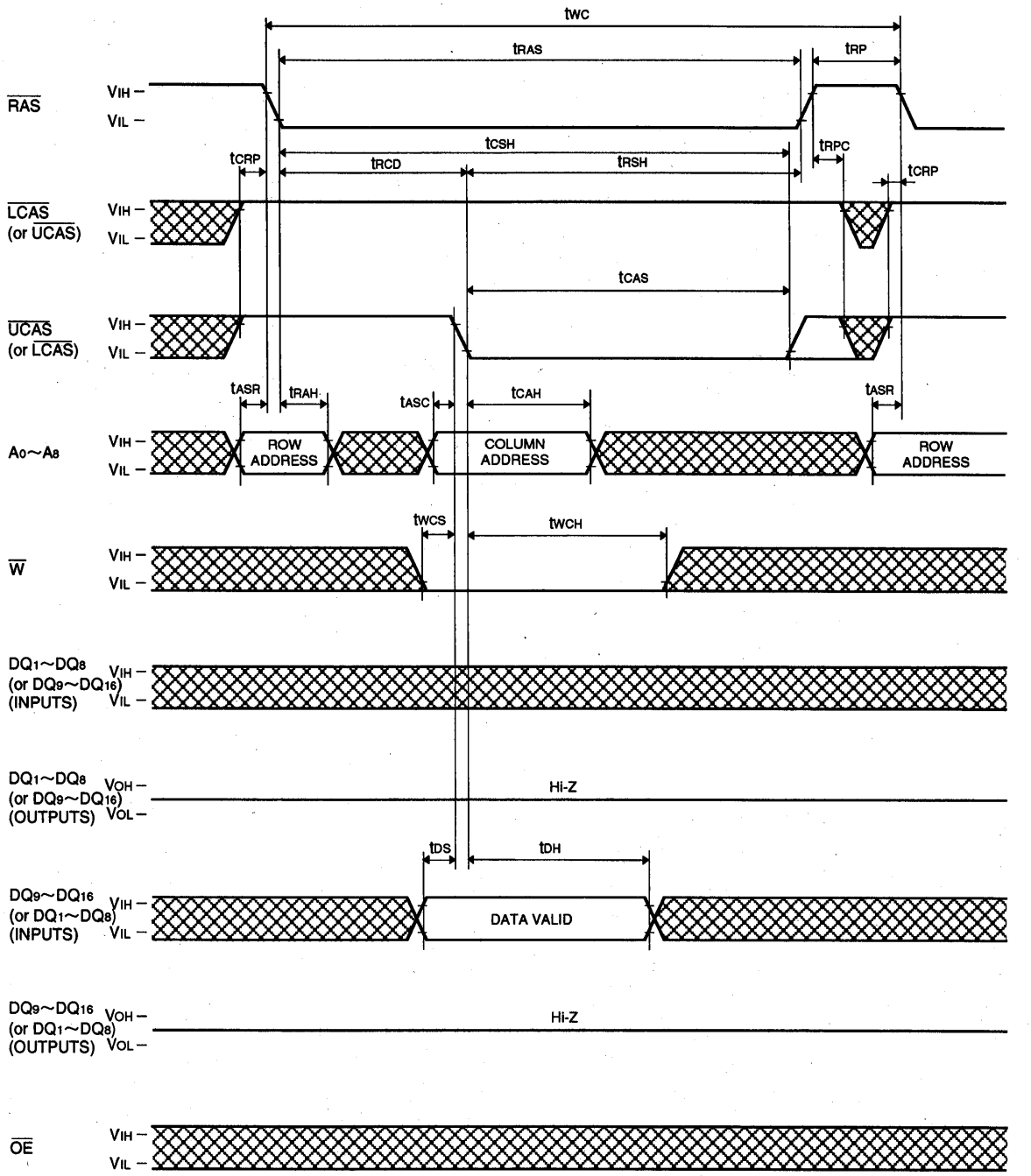
Byte Read Cycle



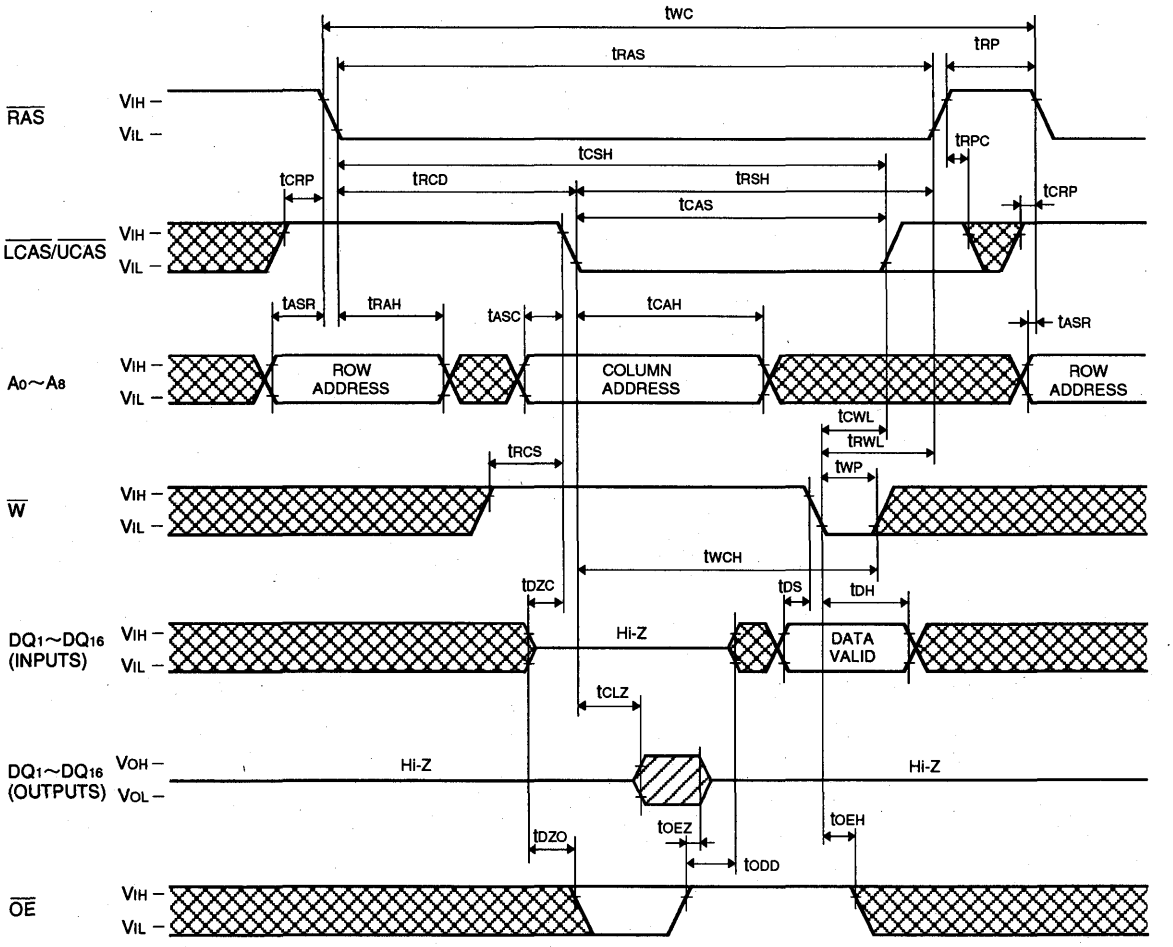
Early Write Cycle



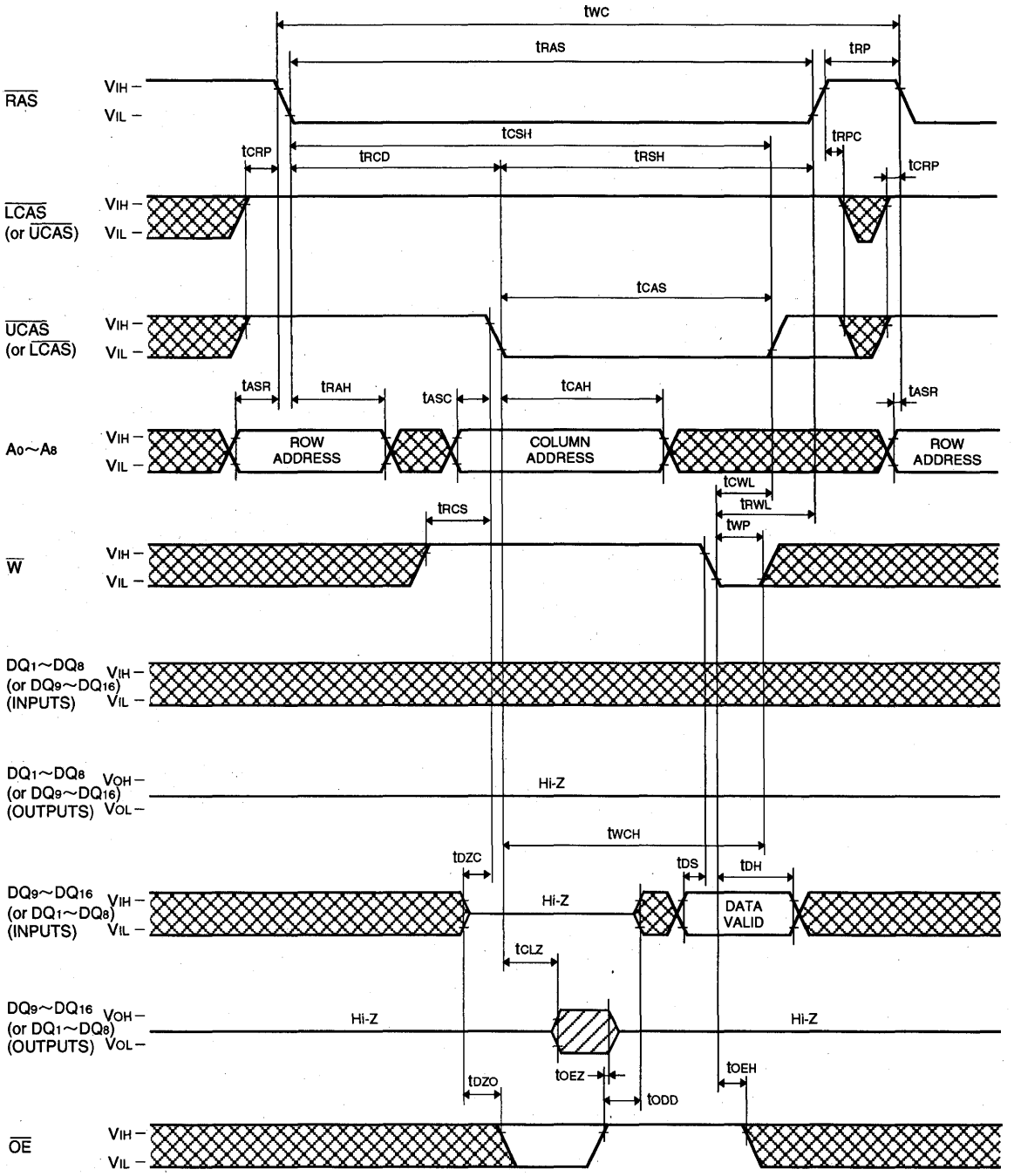
Byte Early Write Cycle



Delayed Write Cycle

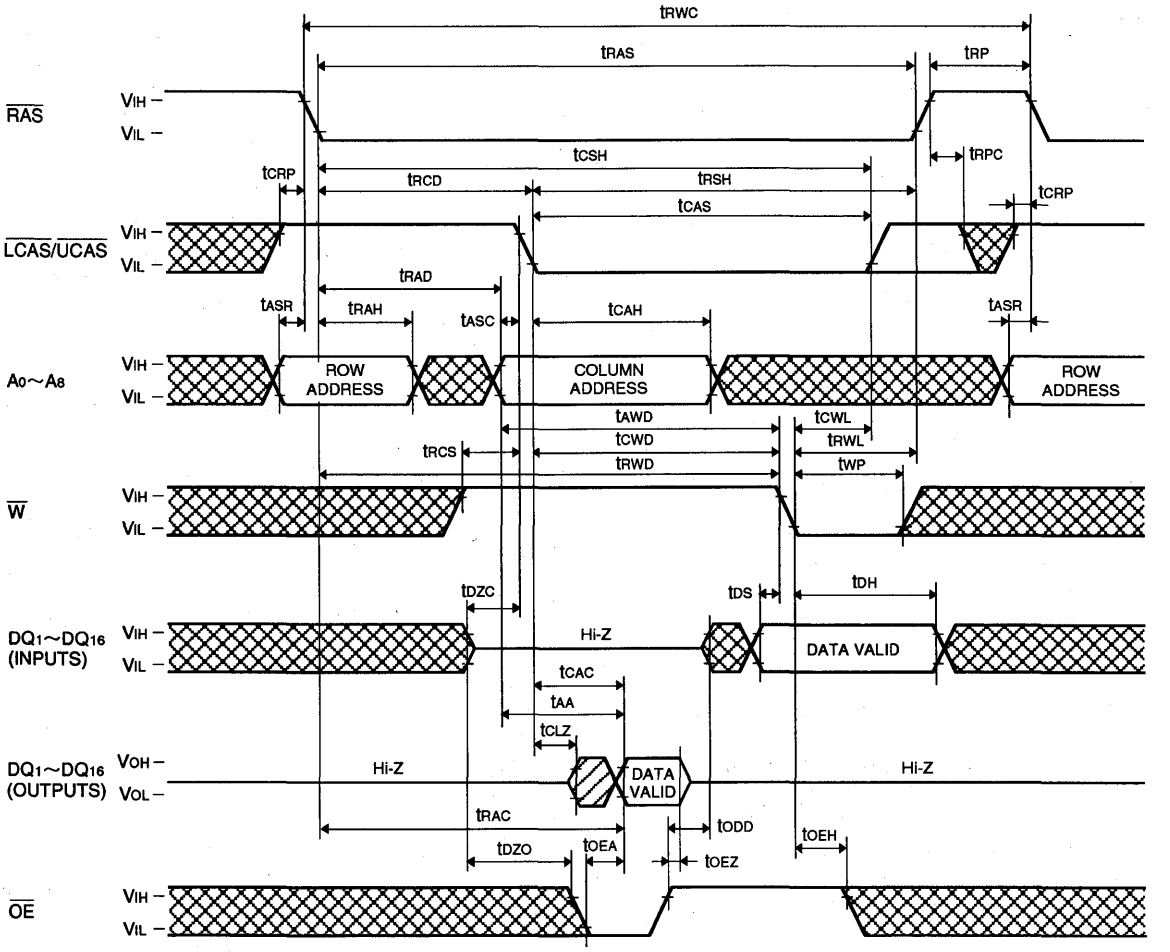


Byte Delayed Write Cycle

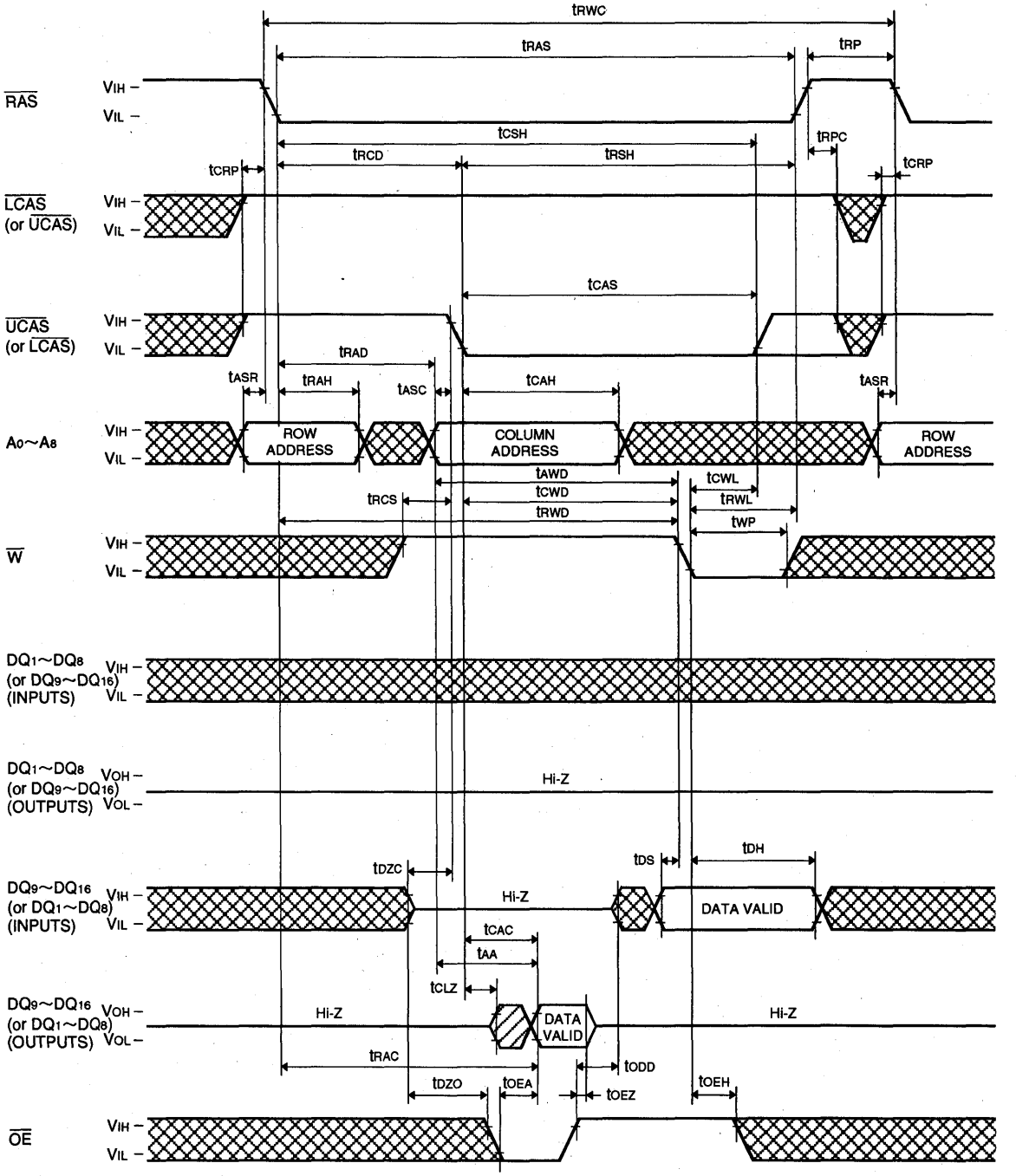


MITSUBISHI ELECTRIC

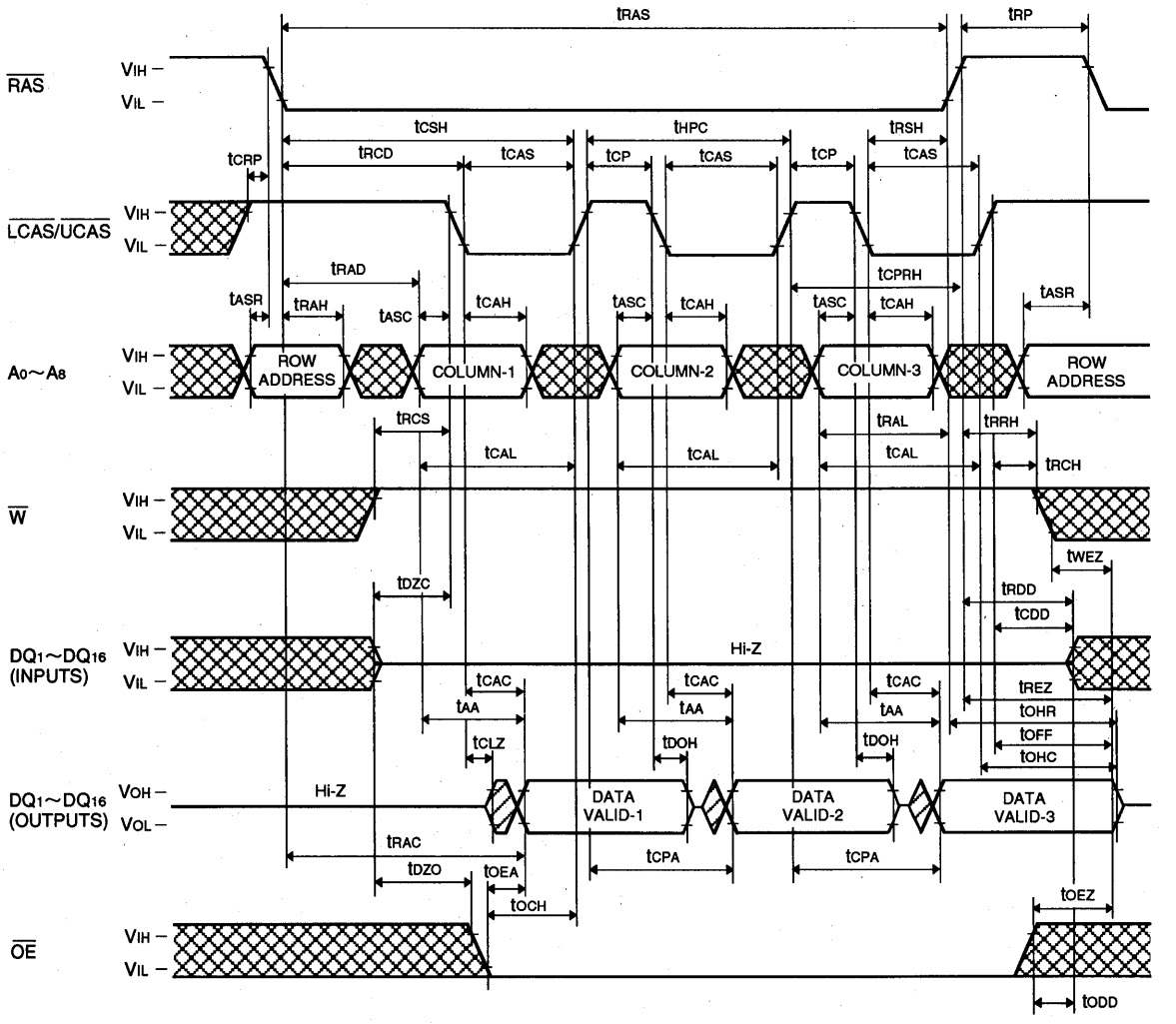
Read-Write, Read-Modify-Write Cycle



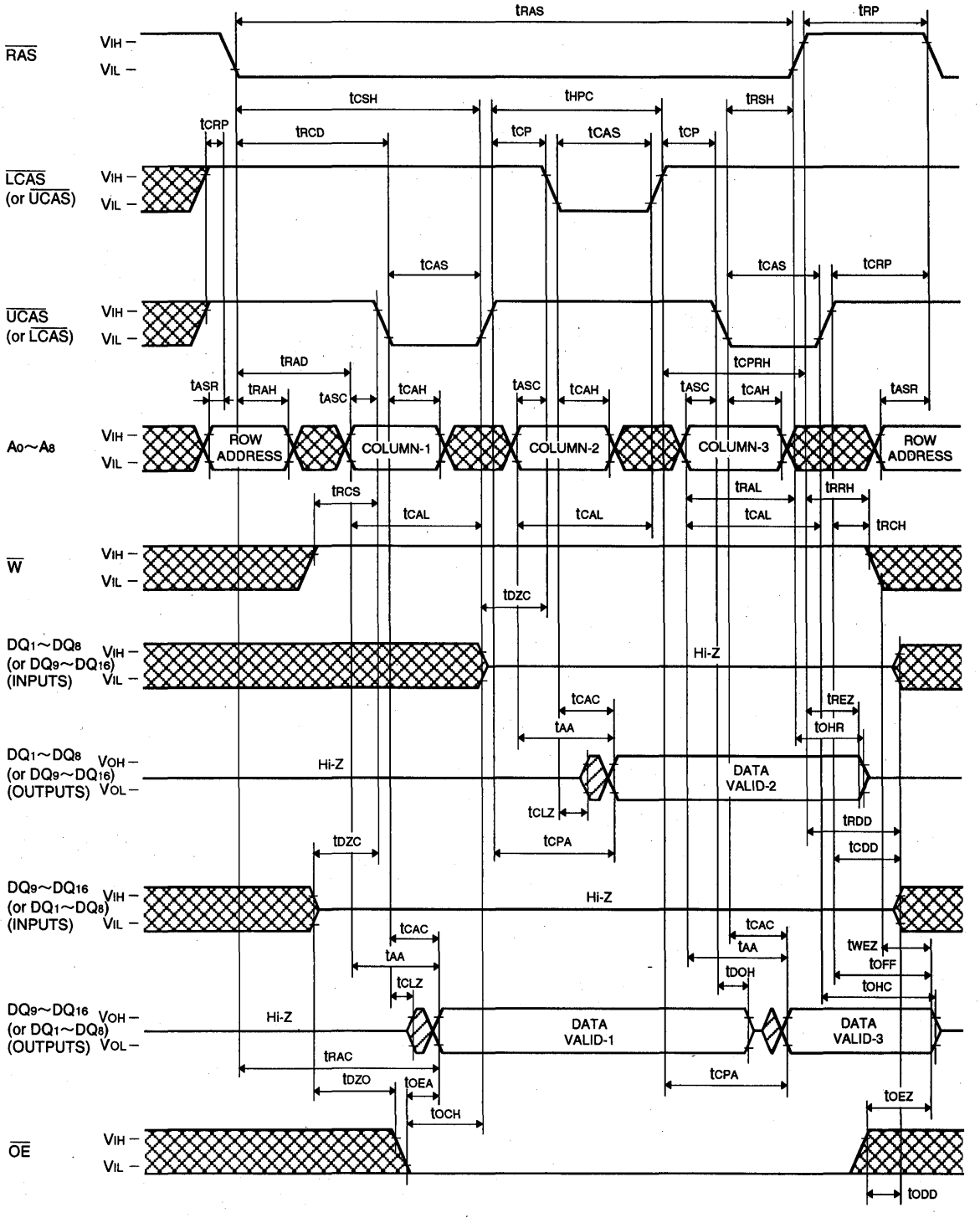
Byte Read-Write, Read-Modify-Write Cycle



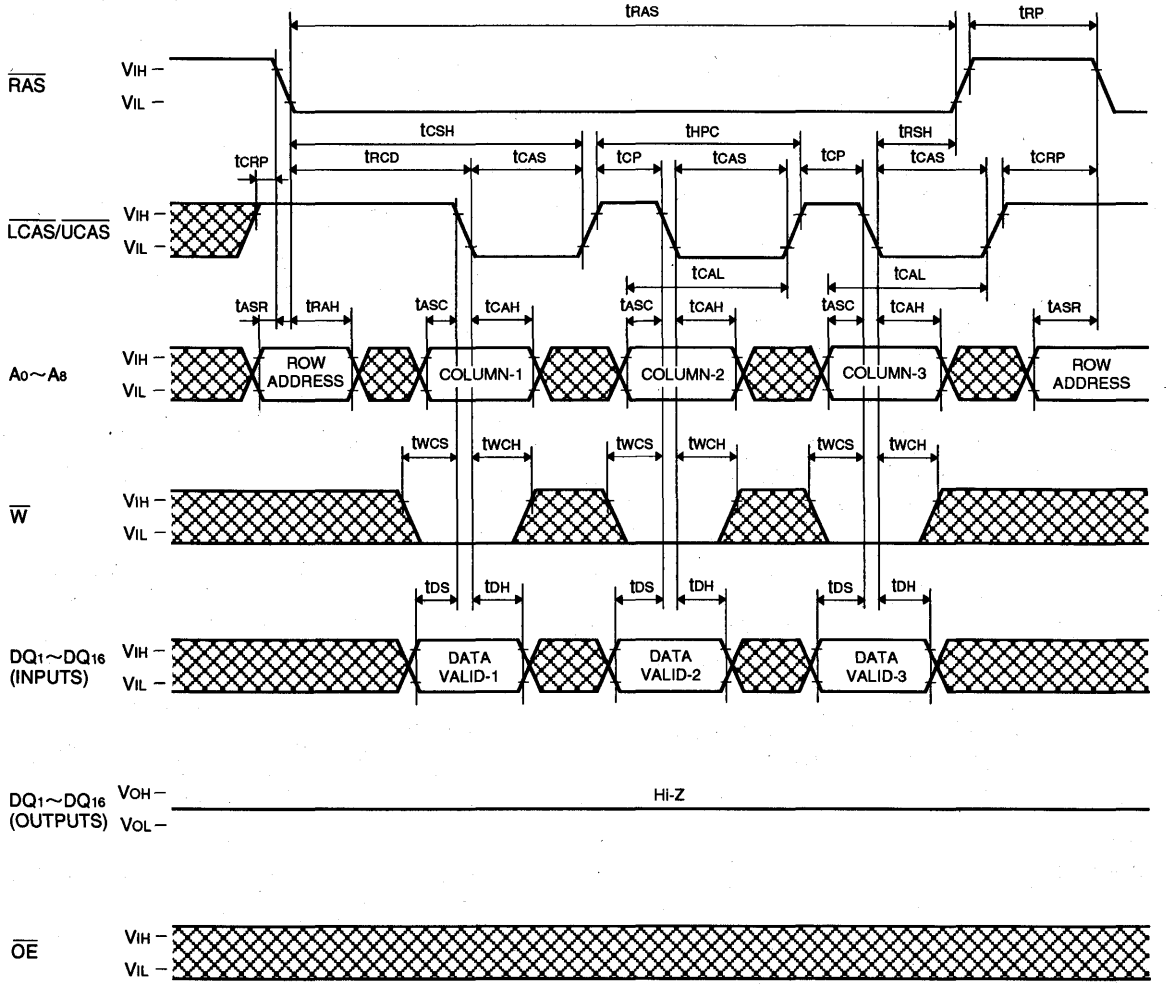
Hyper Page Mode Read Cycle



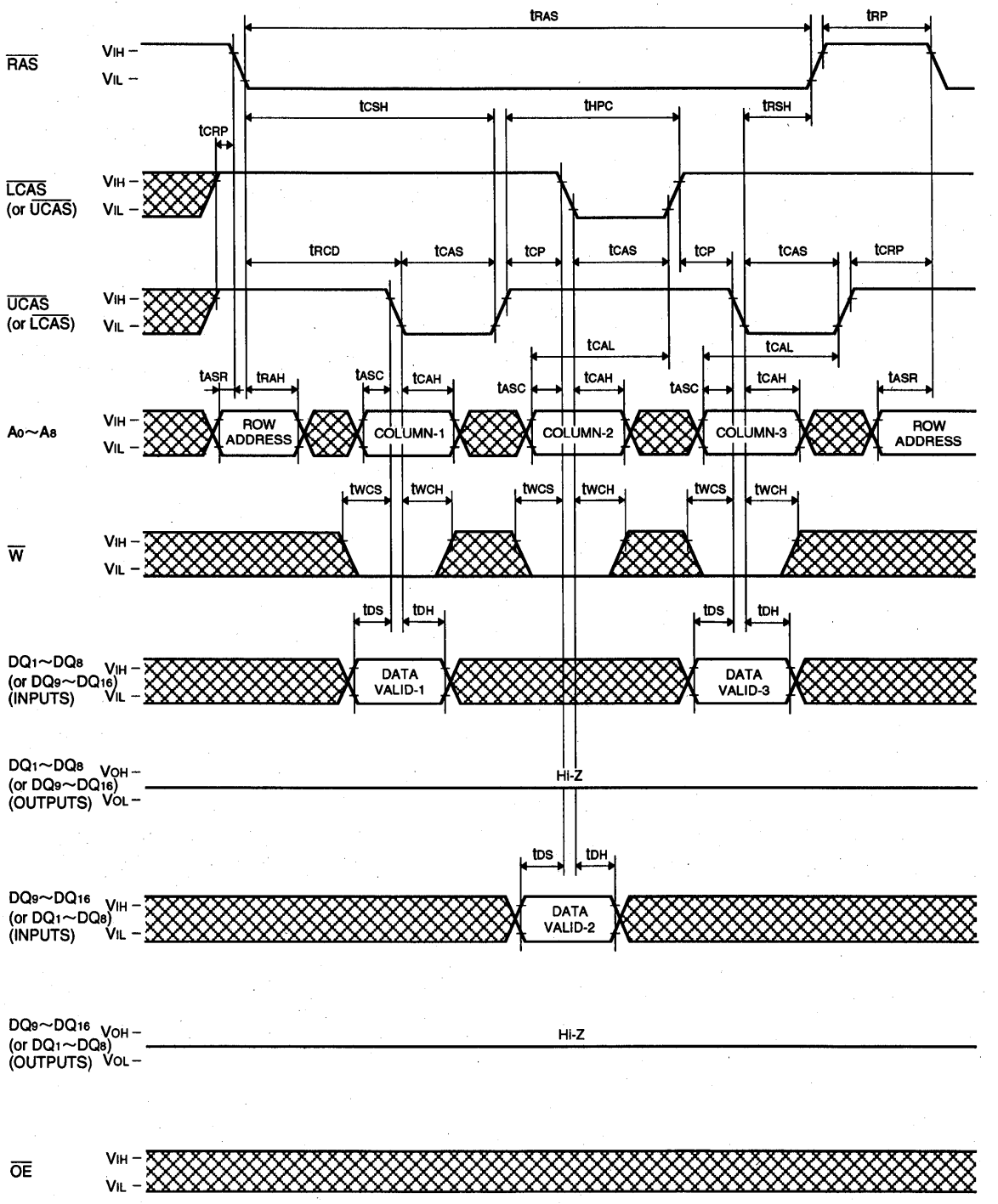
Hyper Page Mode Byte Read Cycle



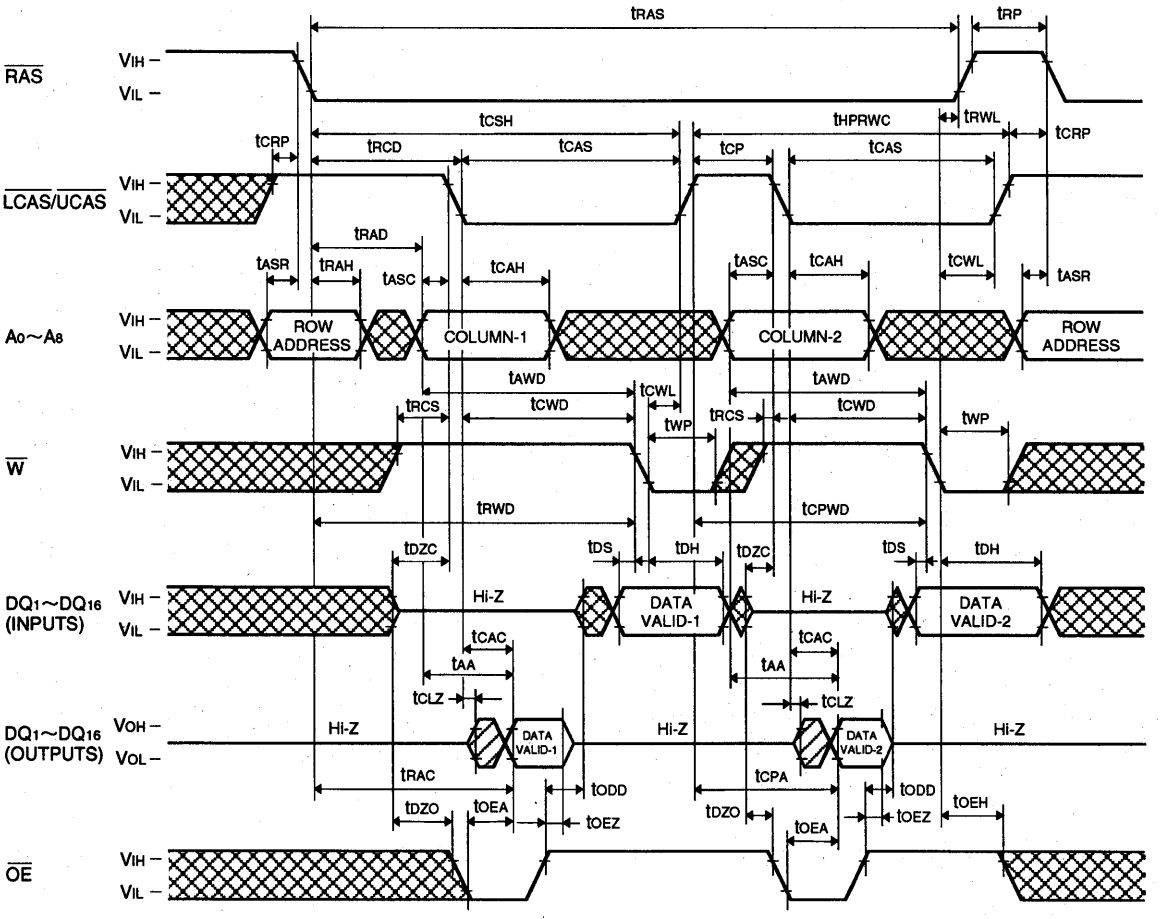
Hyper Page Mode Early Write Cycle



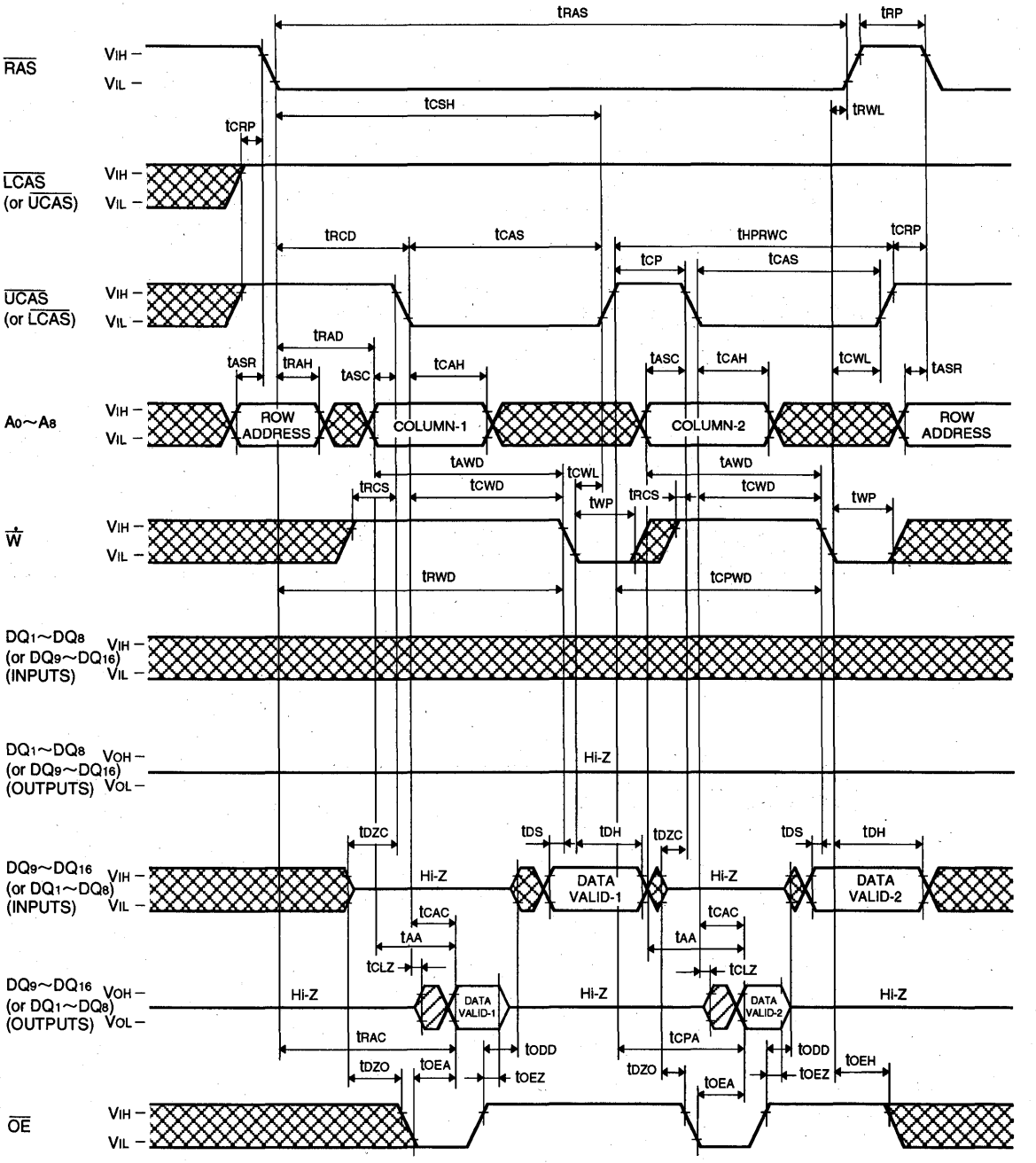
Hyper Page Mode Byte Early Write Cycle



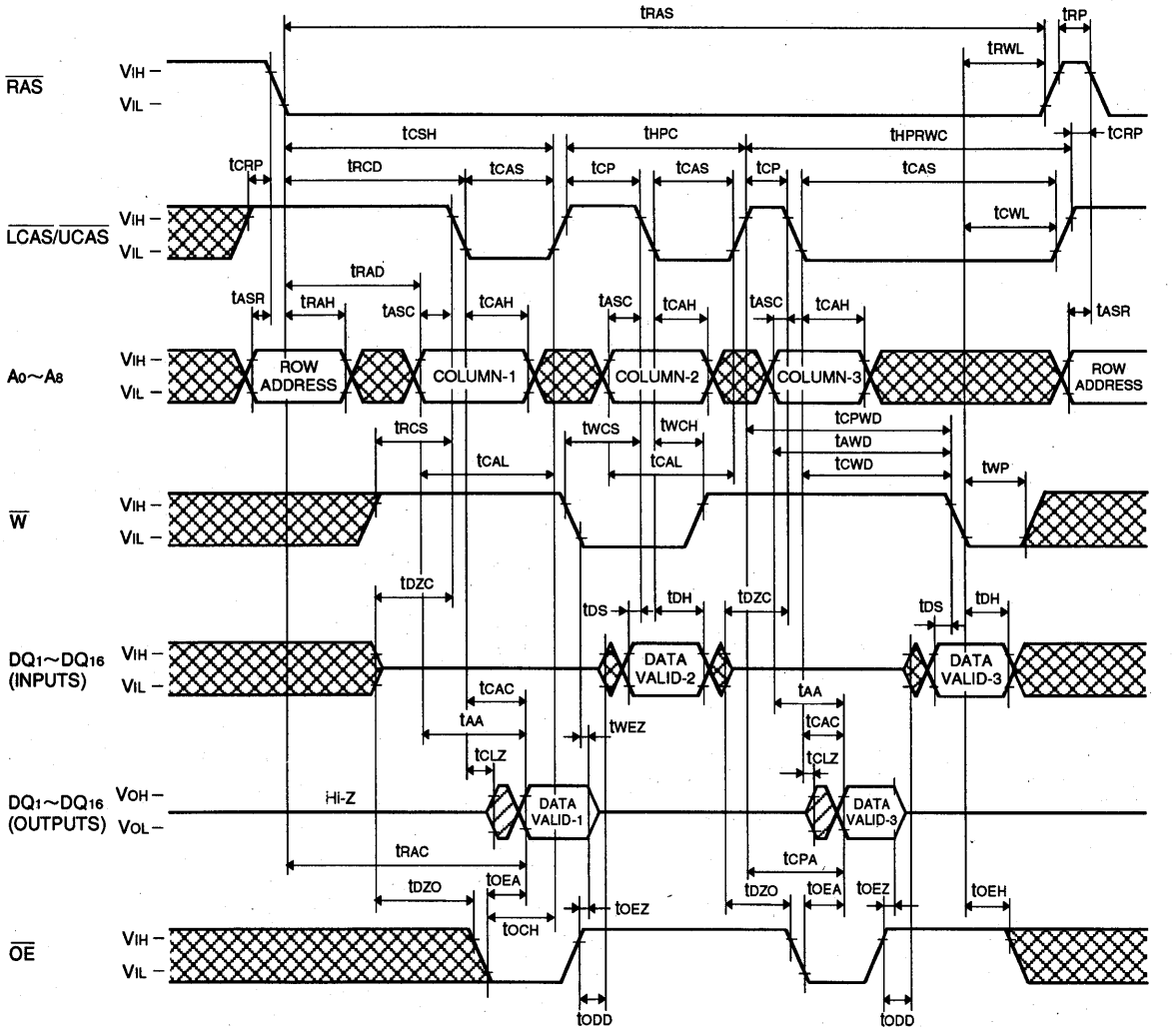
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



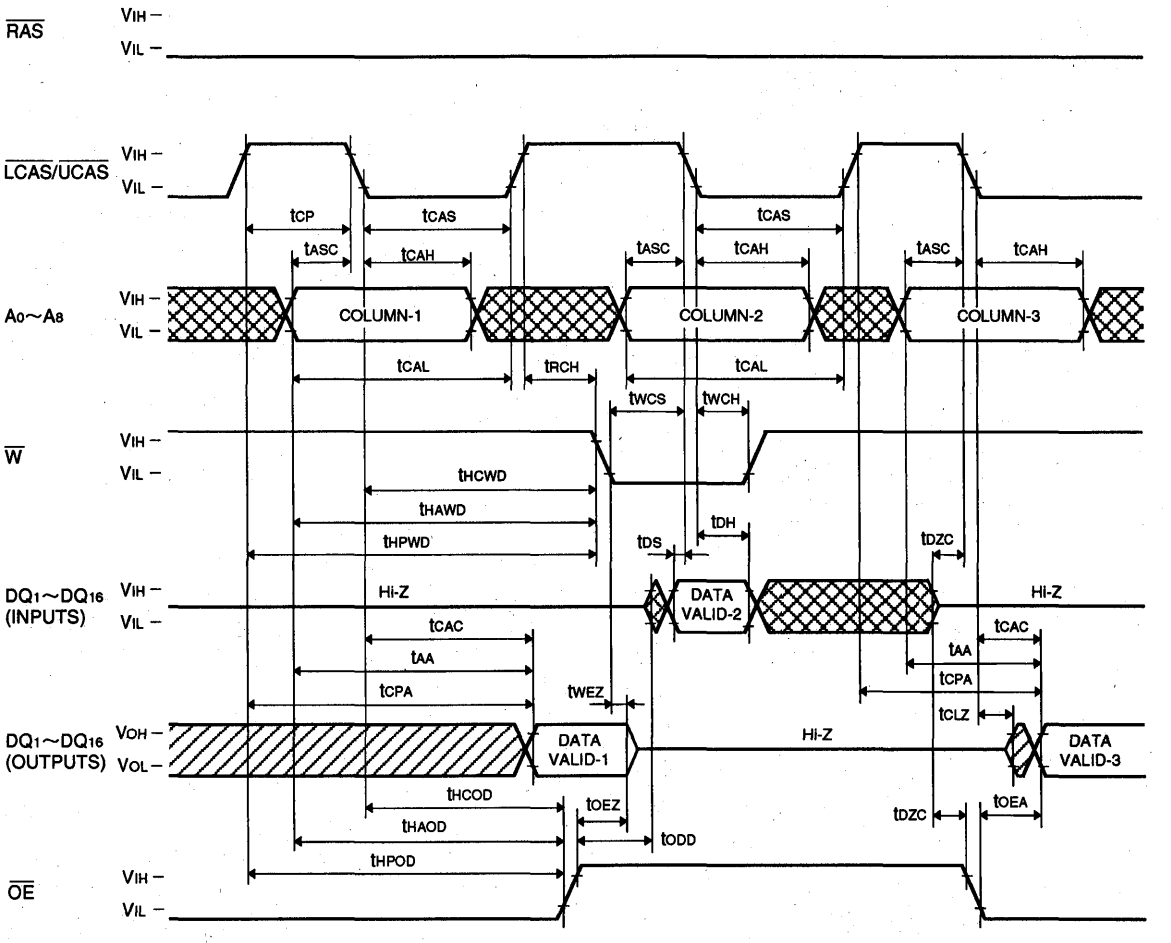
Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



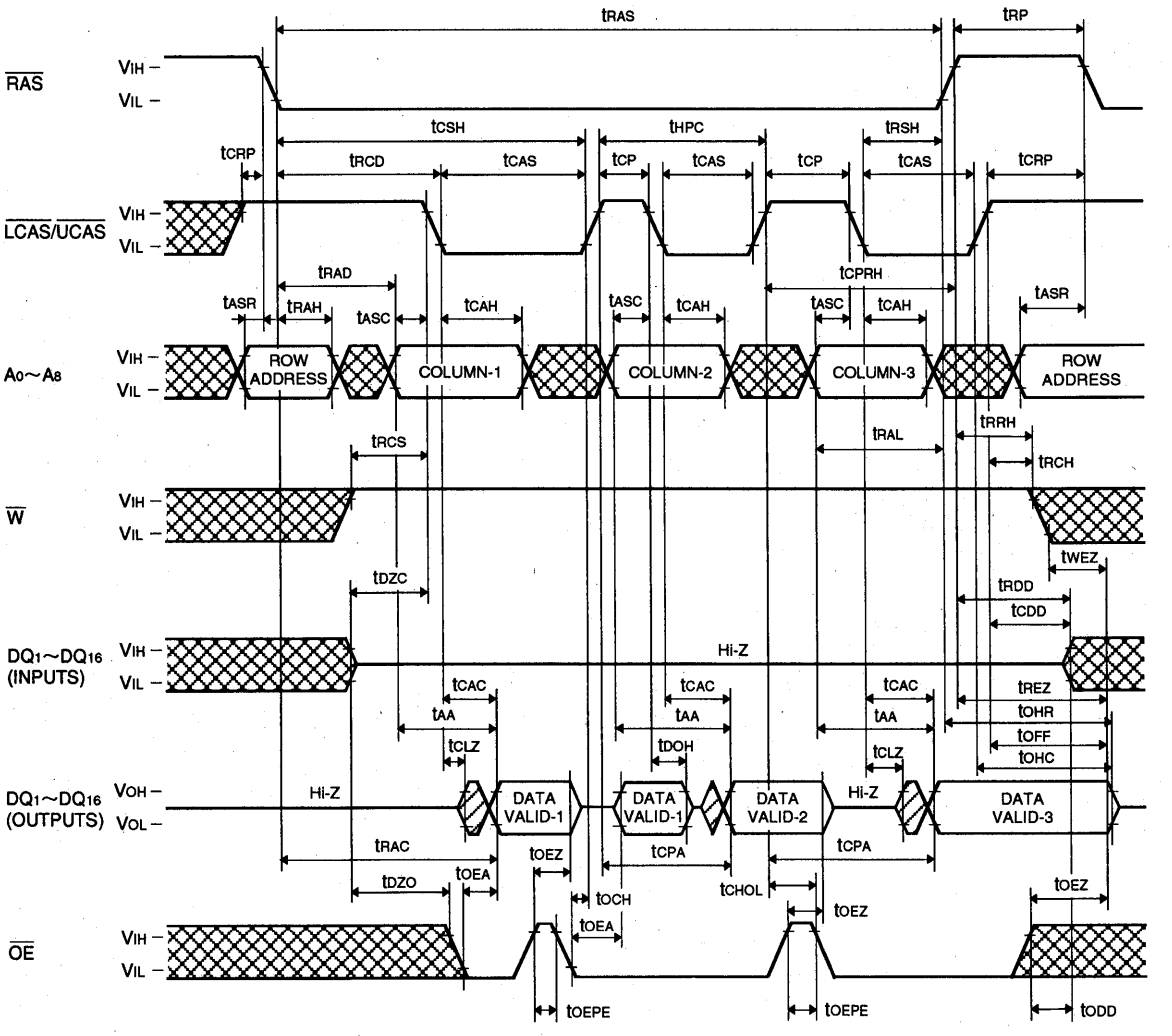
Hyper Page Mode Mix Cycle (1)



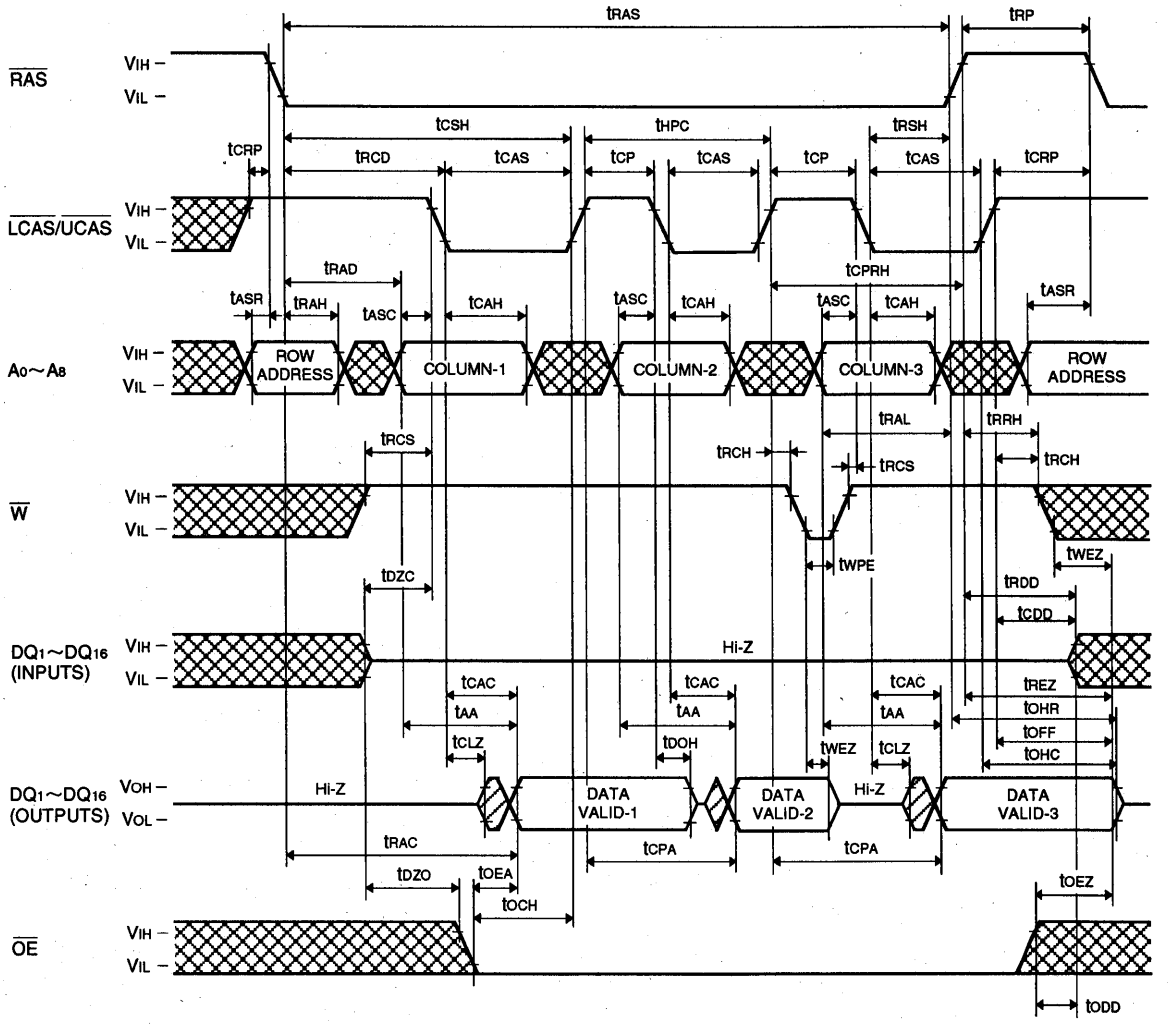
Hyper Page Mode Mix Cycle (2)



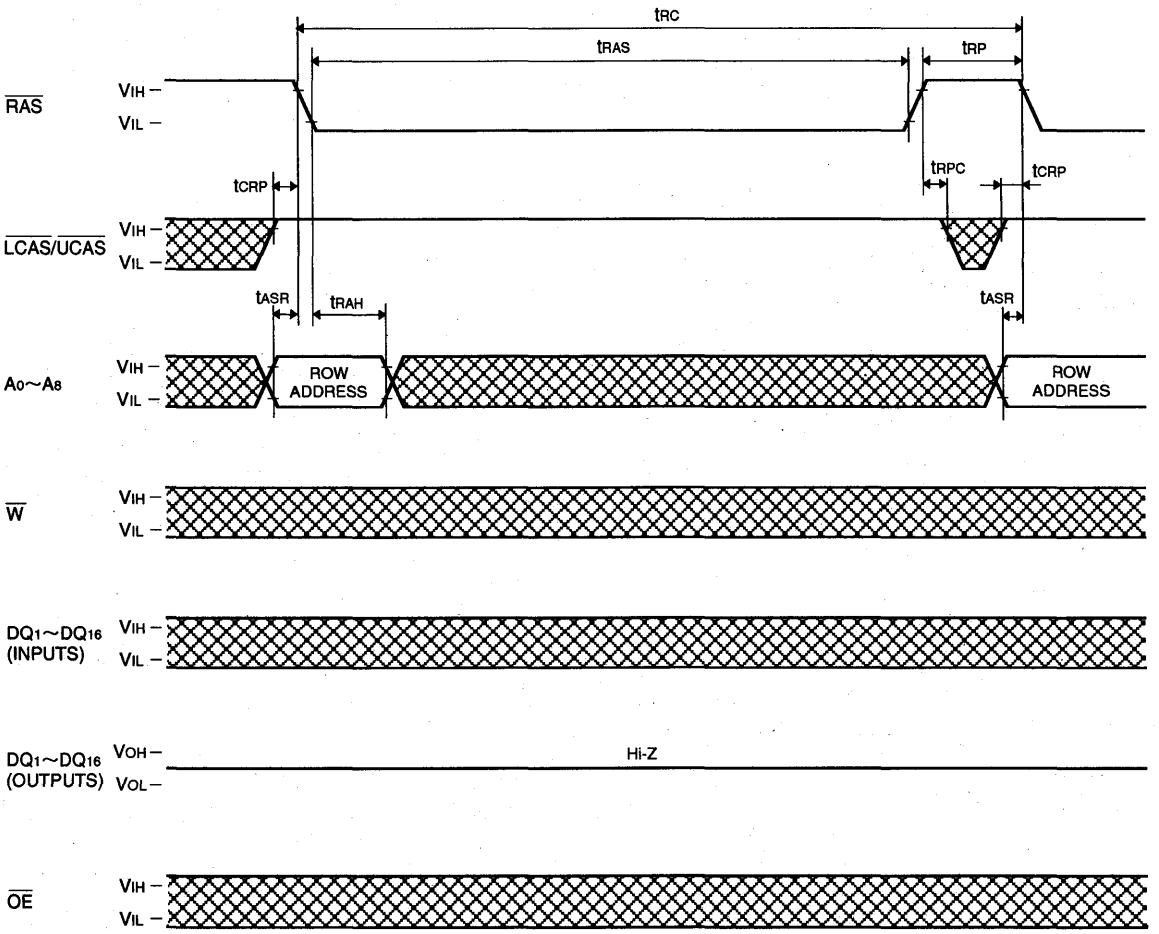
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



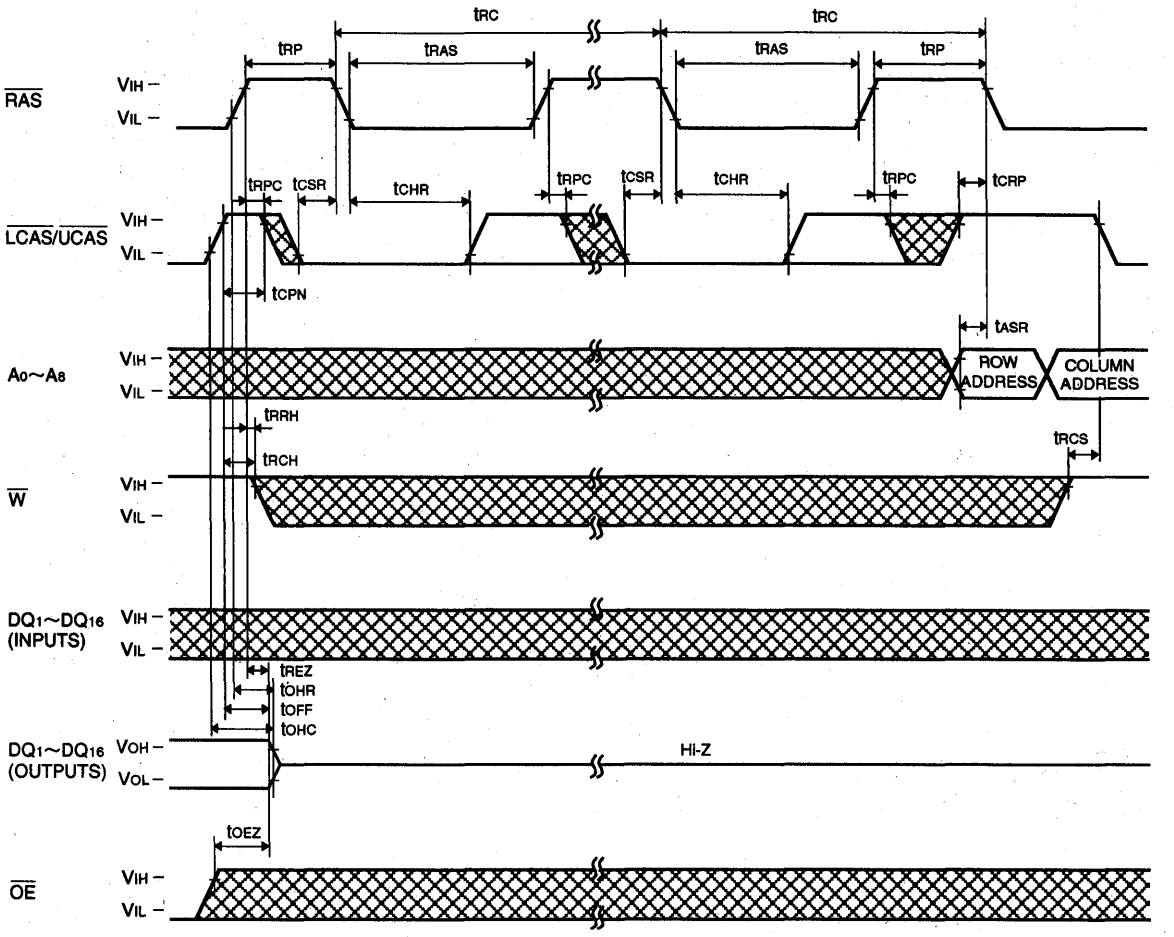
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



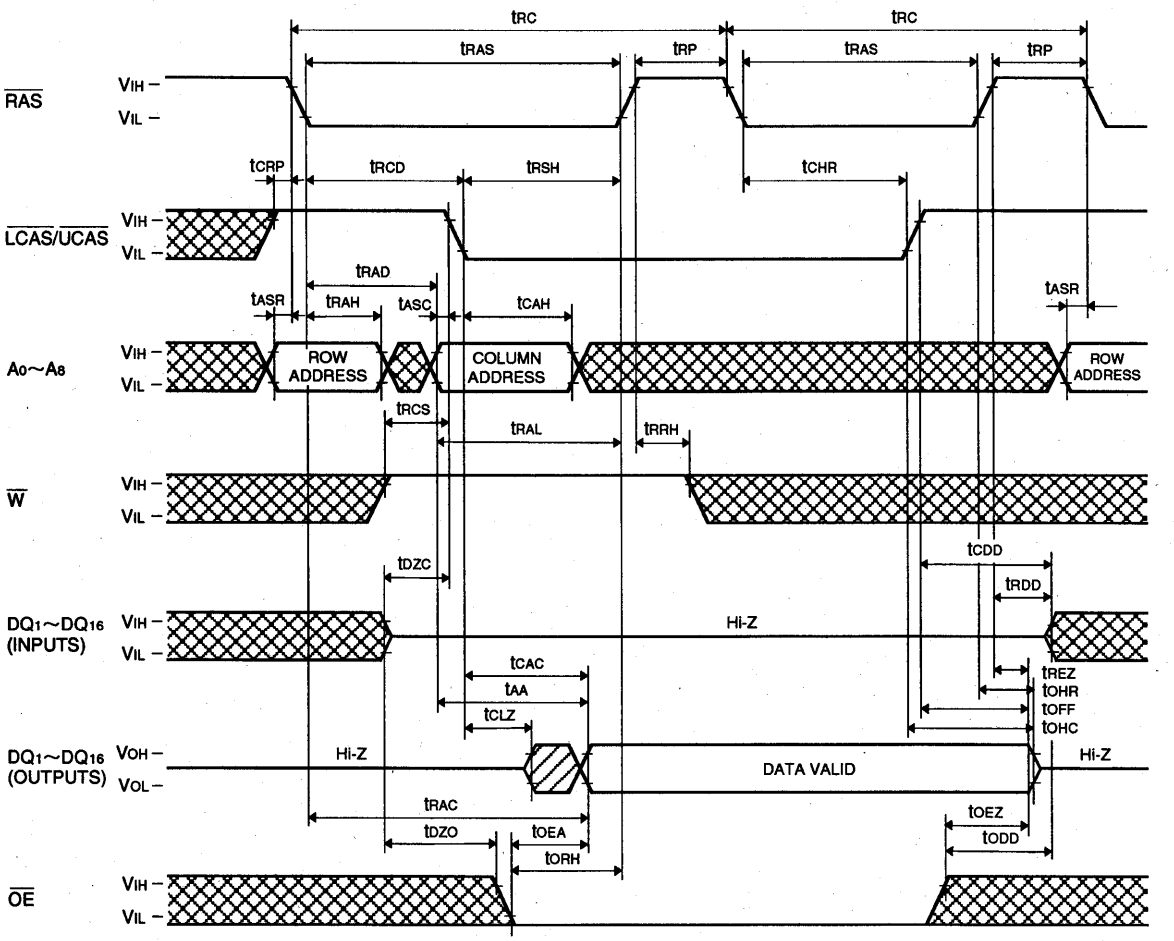
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

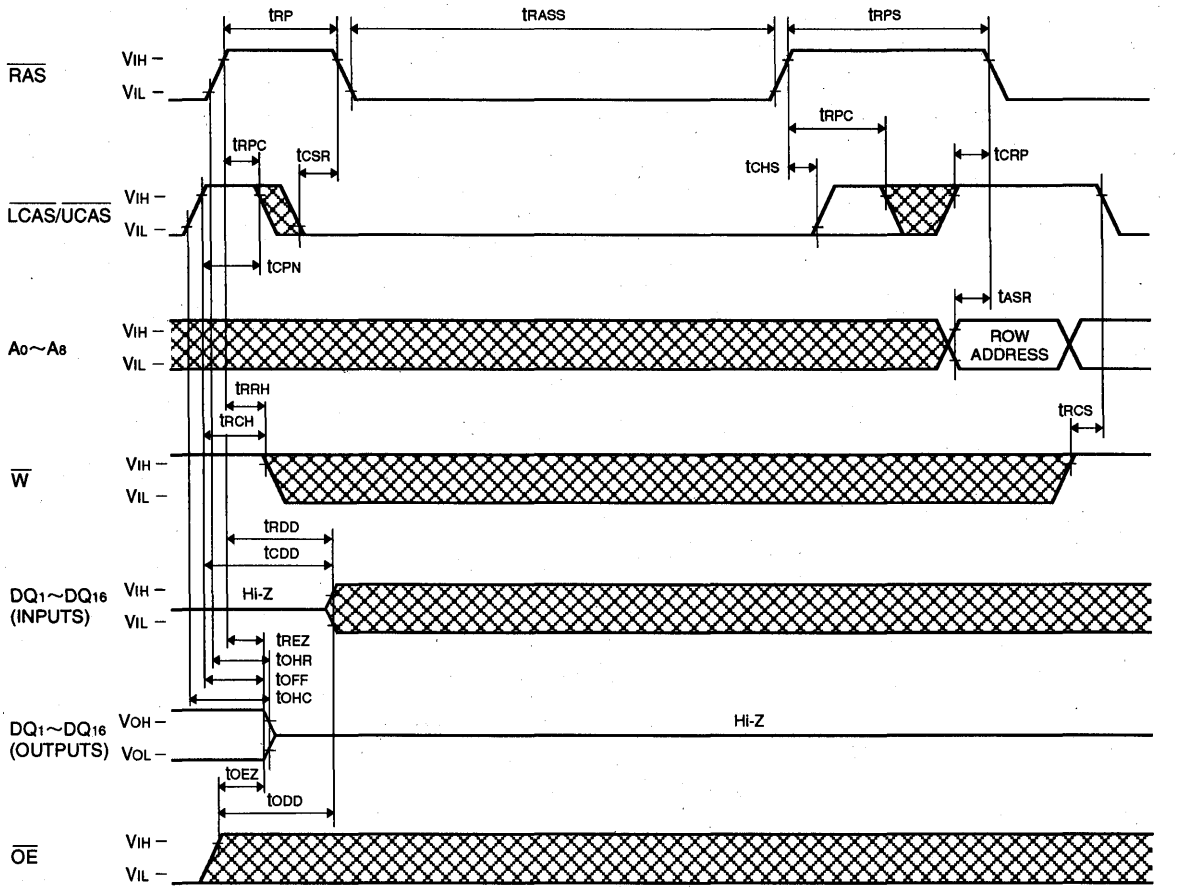


Hidden Refresh Cycle (Read) (Note 32)



Note 32: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle * (Note 30)



Note 30 : Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing Diagram

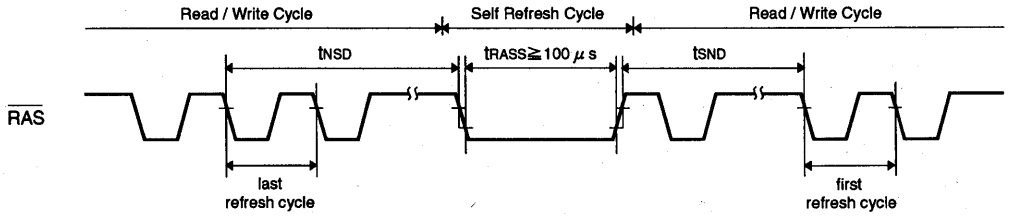
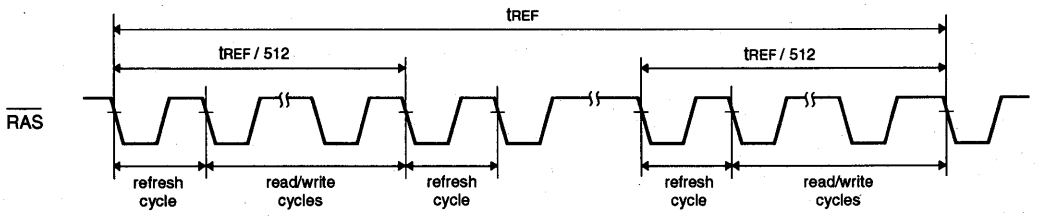


Table 2

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR distributed refresh	t_{NSD}≦250 μs	t_{SND}≦250 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≦16 μs	t_{SND}≦16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh (Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250 μs max.) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 8.2 ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation
(A) Timing diagram

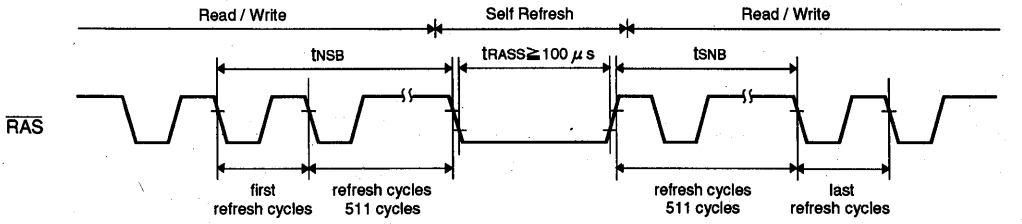
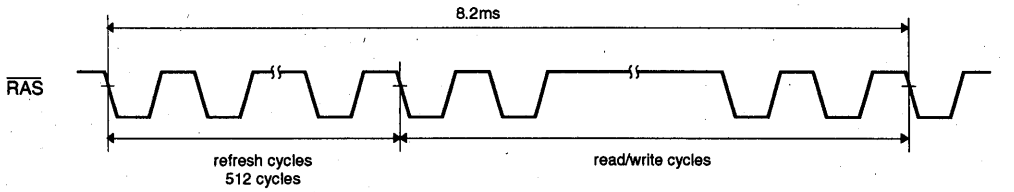


Table 3

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR burst refresh	tNSB≦8.2ms	tSNB≦8.2ms
RAS only burst refresh	tNSB+tSNB≦8.2ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of RAS only burst refresh

All combination of nine row address signals (A_0~A_8) are selected during 512 continuous RAS only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 RAS only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

4M DRAM(3.3V Version)

3

M5M4V4400TP-6,-7,-8, -6S,-7S,-8S

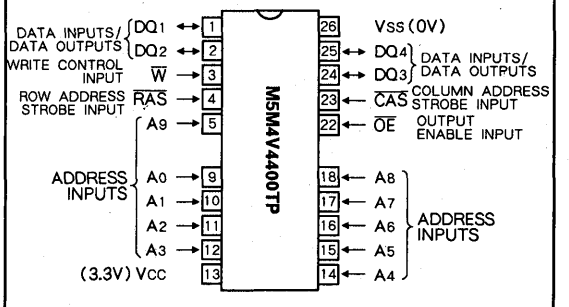
FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities

Self or extended refresh current is small enough for battery back-up application.

PIN CONFIGURATION (TOP VIEW)



Outline 26P3Z-E(TSOP)

FEATURES

Type name	RAS access time (max. ns)	CAS access time (max. ns)	Address access time (max. ns)	OE access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M4V4400TP-6, -6S	60	15	30	15	110	180
M5M4V4400TP-7, -7S	70	20	35	20	130	160
M5M4V4400TP-8, -8S	80	20	40	20	150	130

- Standard 26 pin TSOP(II)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
  - CMOS input level ..... 1.8mW (max)
  - CMOS input level ..... 180 µW (max)*
- Low operating power dissipation
  - M5M4V4400TP-6,-6S ..... 288.0mW (max)
  - M5M4V4400TP-7,-7S ..... 252.0mW (max)
  - M5M4V4400TP-8,-8S ..... 216.0mW (max)
- Self refresh capability*
  - Self refresh current ..... 120 µA (max)
- Extended refresh capability*
  - Extended refresh current ..... 120 µA (max)
- Fast-page mode, (1024-bit random access) Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early write operation and OE to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9)*

* Applicable to self refresh version (M5M4V4400TP-6S, -7S, -8S : option) only.

APPLICATION

Lap top personal computer, Solid state disc, Microcomputer memory, Refresh memory for CRT

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

FUNCTION

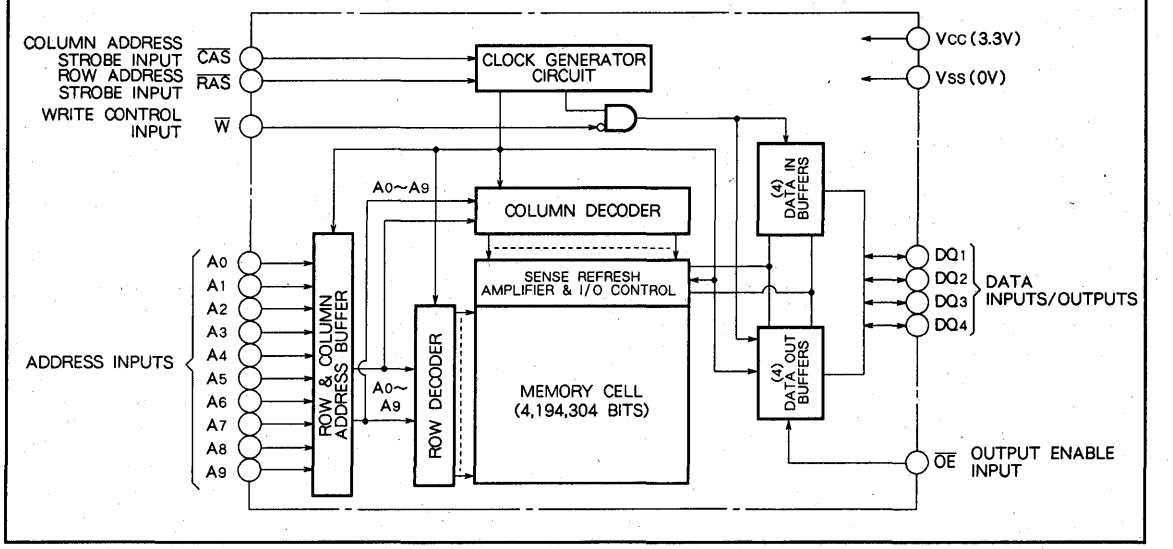
In addition to normal read, write, and read-modify-write operations the M5M4V4400TP provides, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed -write. The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ V_{CC}	−5		5	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}+0.3V Other inputs pins = 0V	−5		5	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4, 5)	M5M4V4400-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling			80	mA
		M5M4V4400-7,-7S	t_{RC} = t_{WC} = min.			70	
		M5M4V4400-8,-8S	output open			60	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2V output open			0.5	
						0.05*	
$I_{CC3(AV)}$	Average supply current from V_{CC}, $\overline{RAS}$ only refreshing (Note 3, 5)	M5M4V4400-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}			80	mA
		M5M4V4400-7,-7S	t_{RC} = min.			70	
		M5M4V4400-8,-8S	output open			60	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Pge-Mode (Note 3, 4, 5)	M5M4V4400-6,-6S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling			70	mA
		M5M4V4400-7,-7S	t_{RC} = min.			60	
		M5M4V4400-8,-8S	output open			50	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M4V4400-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			70	mA
		M5M4V4400-7,-7S	t_{RC} = min.			60	
		M5M4V4400-8,-8S	output open			50	
$I_{CC8(AV)}$*	Average supply current from V_{CC} Battery back-up (Note 6)		Stand-by : $\overline{RAS}$ ≧ V_{CC} − 0.2V, $\overline{CAS}$ ≧ V_{CC} − 0.2V or $\overline{CAS}$ ≦ 0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh : $\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$ ≦ 0.2V or ≧ V_{CC} − 0.2V $\overline{OE}$ ≦ 0.2V or ≧ V_{CC} − 0.2V A_0~A_9 ≦ 0.2V or ≧ V_{CC} − 0.2V DQ = open t_{RC} = 125 μs t_{RAS} = t_{RAS} min~1 μs			120	μA
$I_{CC9(AV)}$*	Average supply current from V_{CC}, Self refresh mode (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output open			120	μA

Note 2 : Current flowing into an IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5 : Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = Vss f = 1MHz V_I = 25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits						Unit
			M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		60		70		80	ns
t_{AA}	Column Address access time	(Note 7, 10)		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	0	20	ns

Note 6 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note that $\overline{RAS}$ may be cycled during the initial pause. Any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 100pF, V_{OH} = 2.4V (I_{OH} = − 2mA) and V_{OL} = 0.4V (I_{OL} = 2mA).
The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V (V_{OL}).

8 : Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).

9 : Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount which t_{RCD} or t_{RAD} exceeds the value shown.

10 : Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max).

11 : Assumes that $t_{CP} \leq t_{CP}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).

12 : t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ | ± 10 μA |) and is not reference to V_{OH} (min) or V_{OL} (max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		16.4		16.4		16.4	ms
t_{REF}*	Refresh cycle time		128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	40		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 16)	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 17)	0	10	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note 18)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note 18)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note 19)	15		20		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note 19)	15		20		20		ns
t_T	Transition time (Note 20)	1	50	1	50	1	50	ns

Note 13 : The timing requirements are assumed t_T = 5ns.

14 : V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

15 : Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only ; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} or t_{AA}. t_{RCD} (min) is specified as t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).

16 : Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only ; if t_{RAD} is greater than specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{CAC} or t_{AA}.

17 : Operation within the t_{ASC} (max) limit insures that t_{RAC} (max) can be met. t_{ASC} (max) is specified as a reference point only ; if t_{ASC} is greater than the specified t_{ASC} (max) limit and t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

18 : Either t_{DZC} or t_{DZO} must be satisfied.

19 : Either t_{CDD} or t_{ODD} must be satisfied.

20 : t_T is measured between V_{IH} (min) and V_{IL} (max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		20		ns

Note 21 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		15		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		20		ns
tWP	Write pulse width	10		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 22)	150		175		195		ns
tRAS	$\overline{RAS}$ low pulse width	95	10000	115	10000	125	10000	ns
tCAS	$\overline{CAS}$ low pulse width	50	10000	65	10000	65	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		115		125		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		65		65		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	35		40		40		ns
tRWD	Delay time, $\overline{RAS}$ low, to $\overline{W}$ low (Note 23)	80		90		100		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	50		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		20		ns
tWP	Write pulse width	10		15		15		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		20		ns

Note 22 : t_{RWC} is specified as $t_{RWC}(min) = t_{RAC}(max) + t_{ODD}(min) + t_{RWL}(min) + t_{RP}(min) + 4t_T$.

23 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPWD} \geq t_{CPWD}(min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	75		95		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	100	100000	115	100000	135	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	10	15	10	15	10	20	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	35		40		45		ns

Note 24 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25 : t_{RAS}(min) is specified as two cycles of $\overline{CAS}$ input are executed.
26 : t_{CP}(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh* Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		30		ns

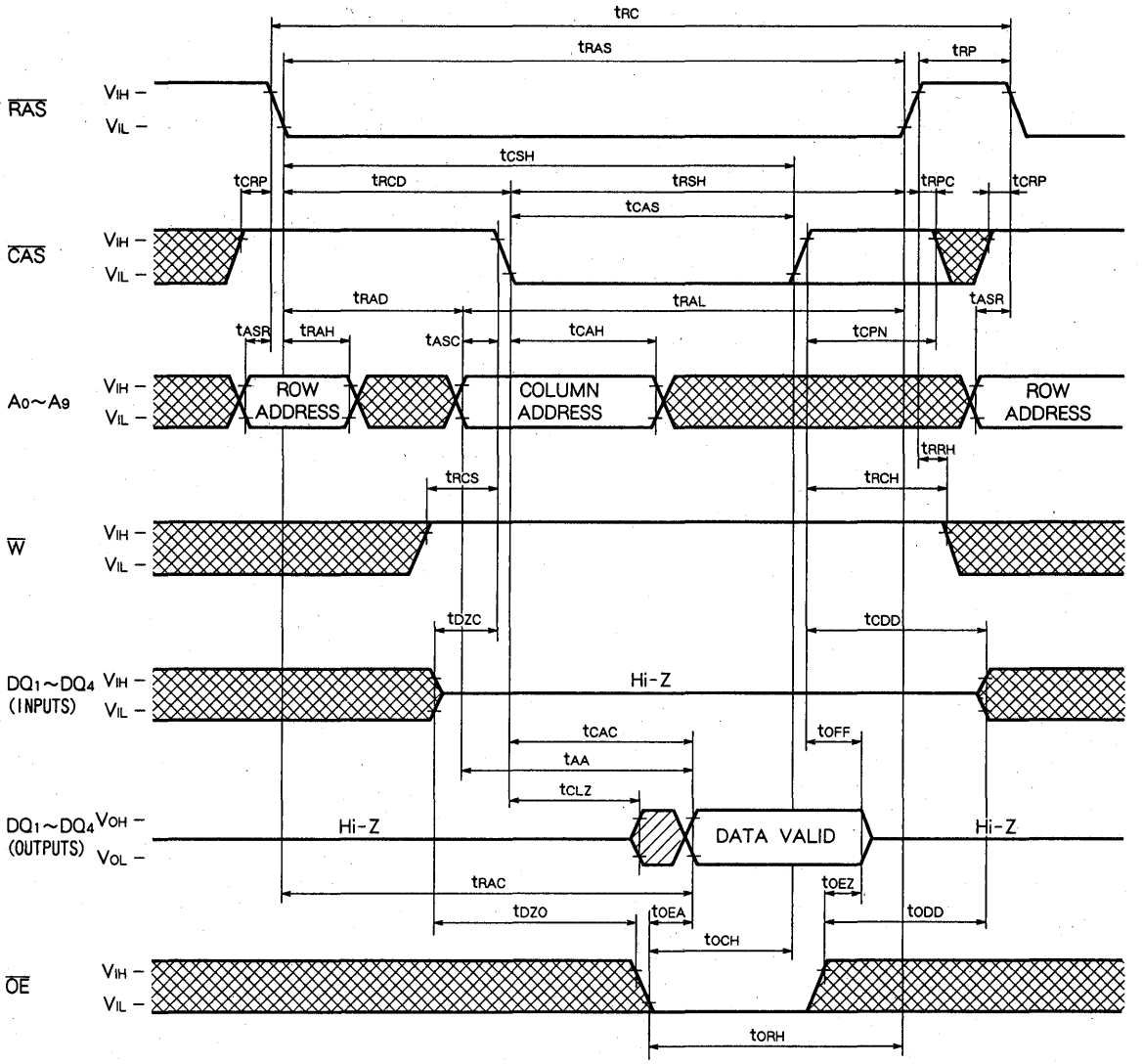
Note 27 : Eight or mode $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits						Unit
		M5M4V4400-6, -6S		M5M4V4400-7, -7S		M5M4V4400-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	$\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	$\overline{RAS}$ high pulse width	110		130		150		ns
t_{CHS}	$\overline{CAS}$ hold time after $\overline{RAS}$ high	−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		ns

Timing Diagrams (Note 28)

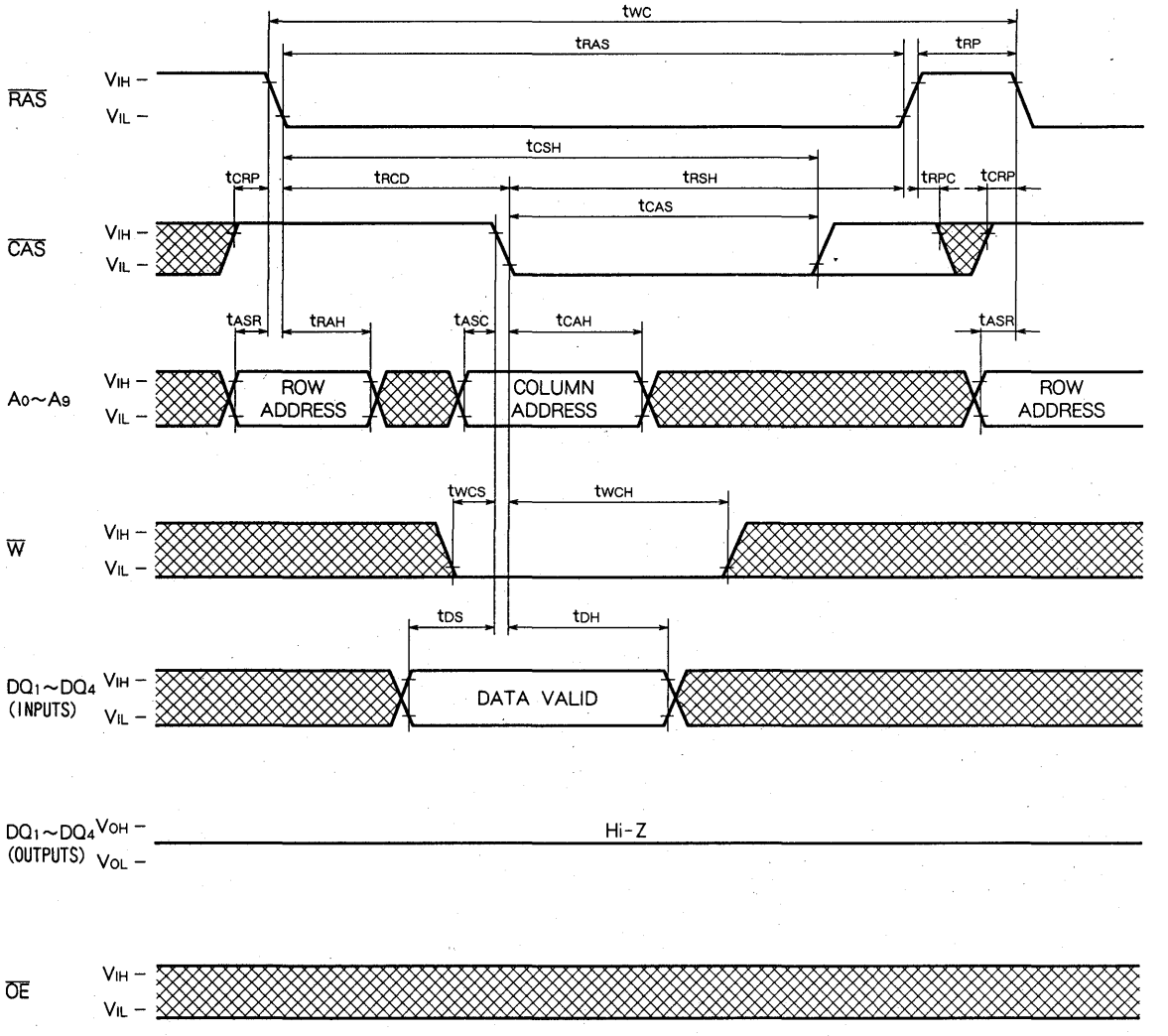
Read Cycle



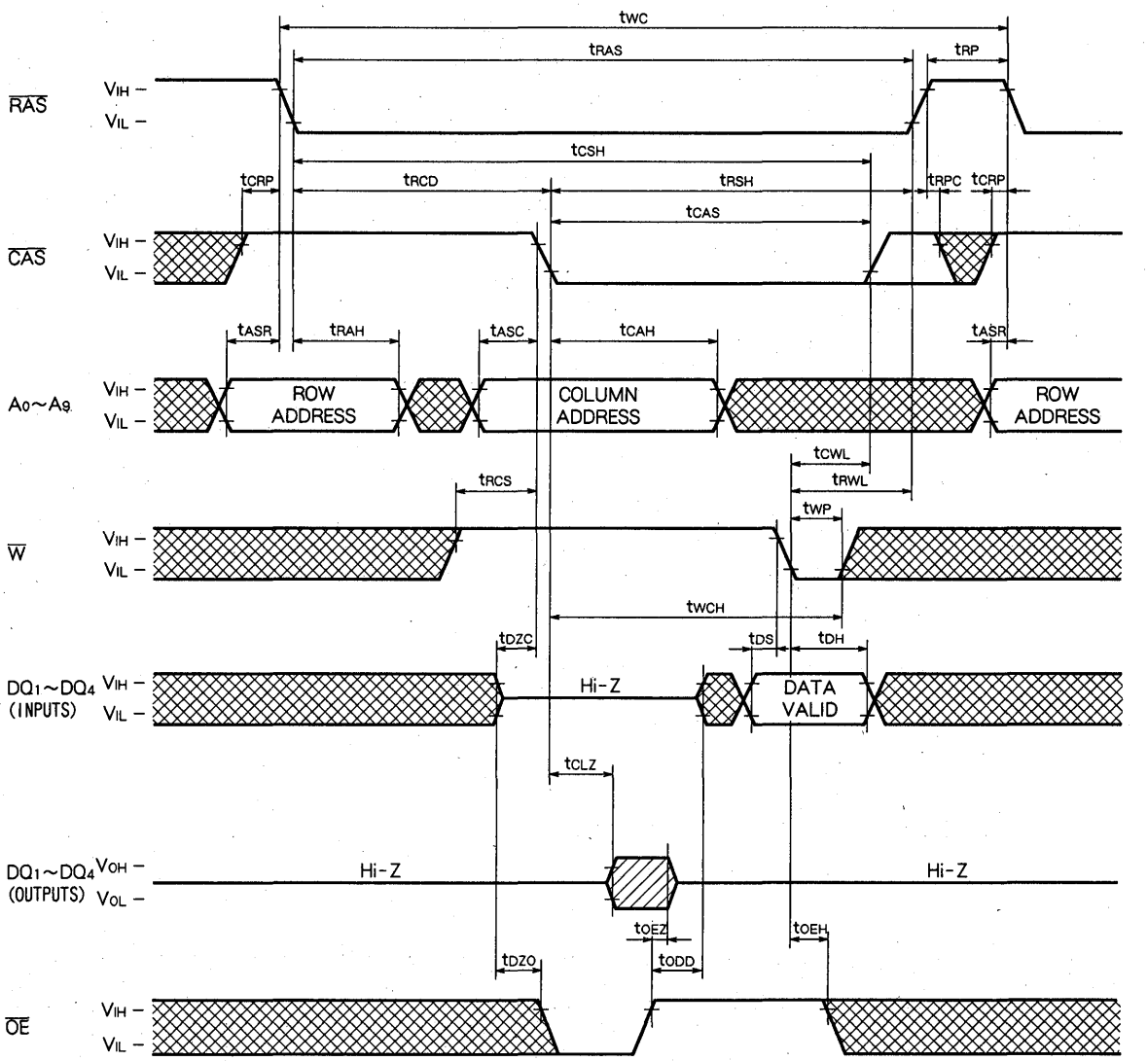
Note 28 Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicatea the invalid output.

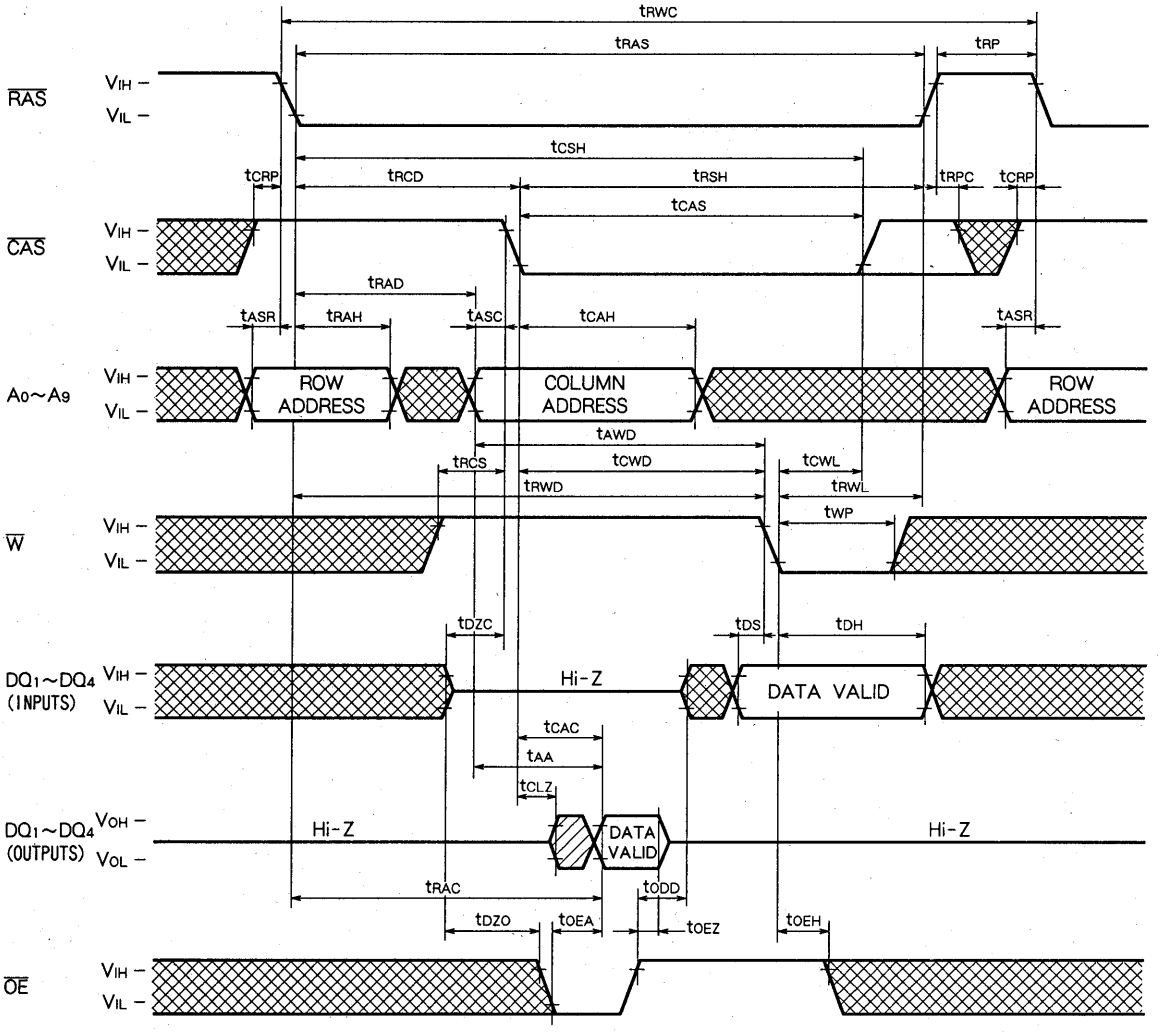
Write Cycle (Early write)



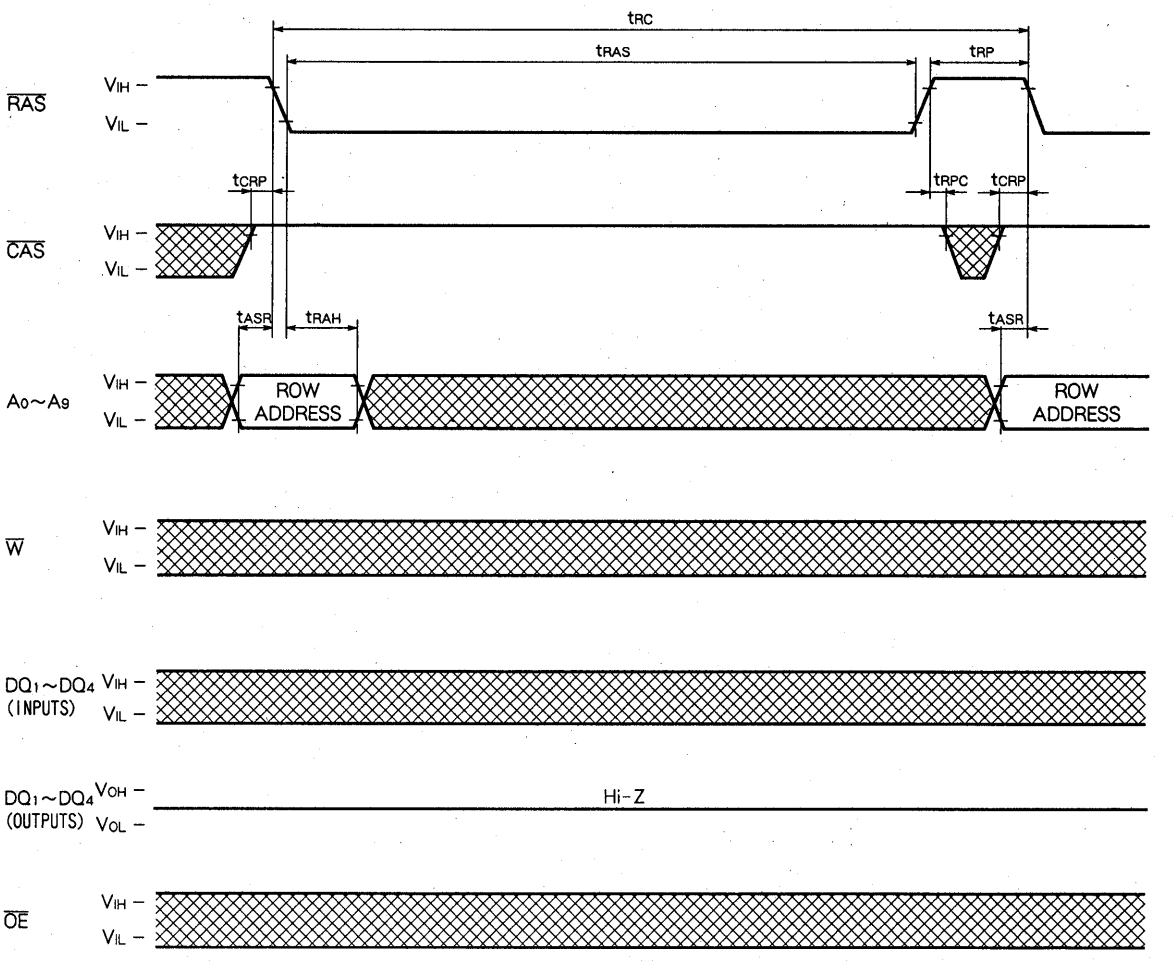
Write Cycle (Delayed Write)



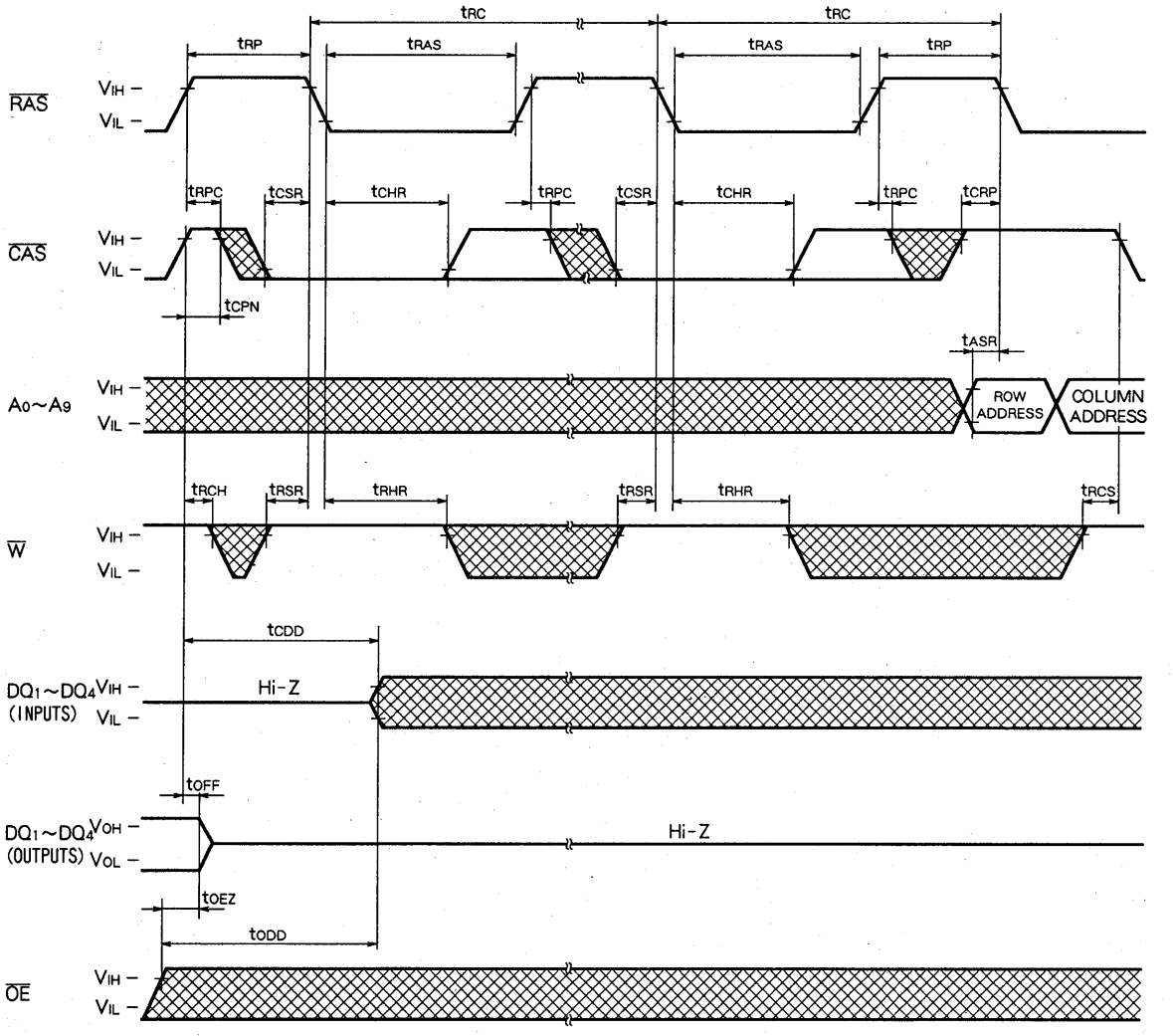
Read-Write, Read-Modify-Write Cycle



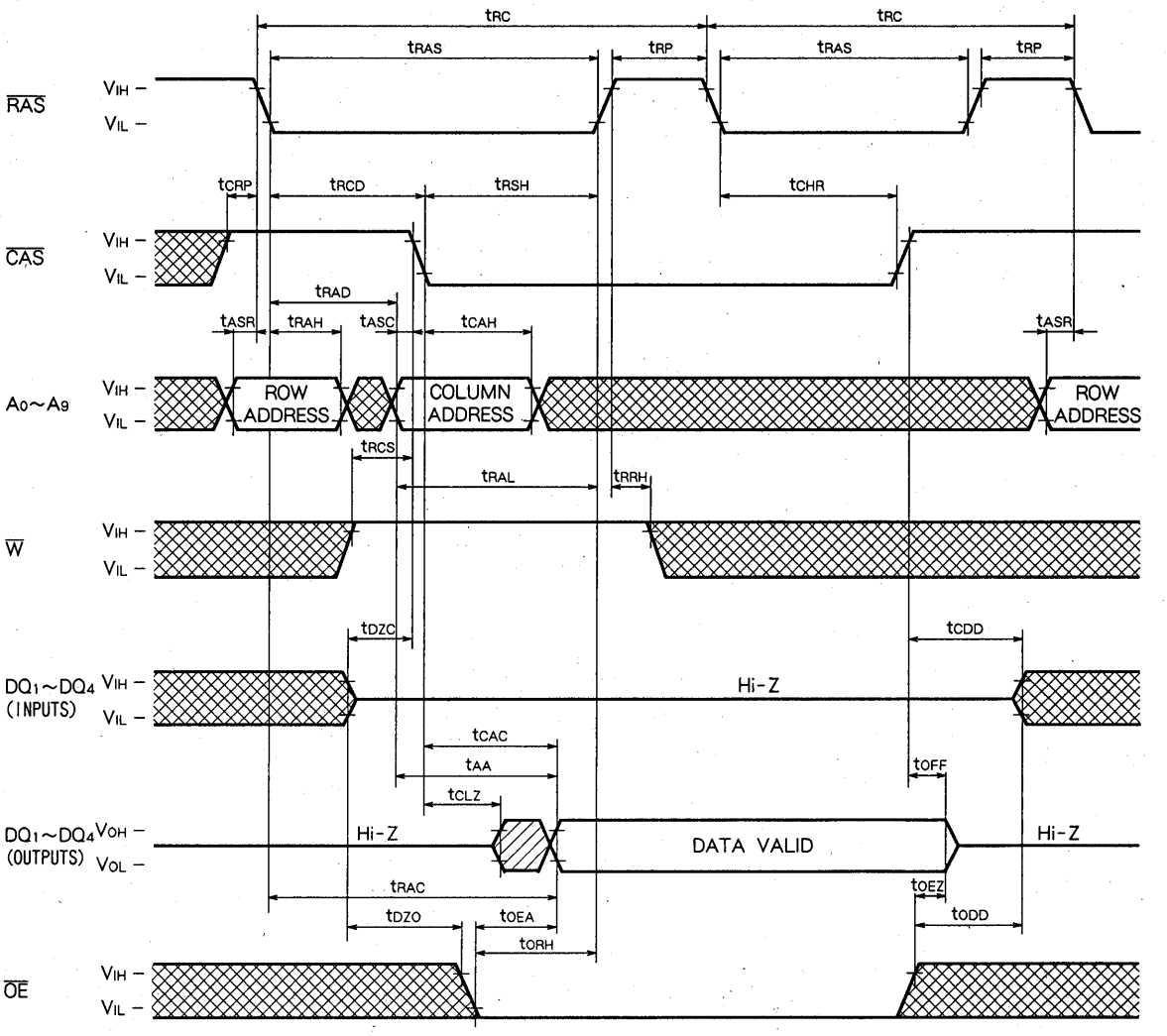
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

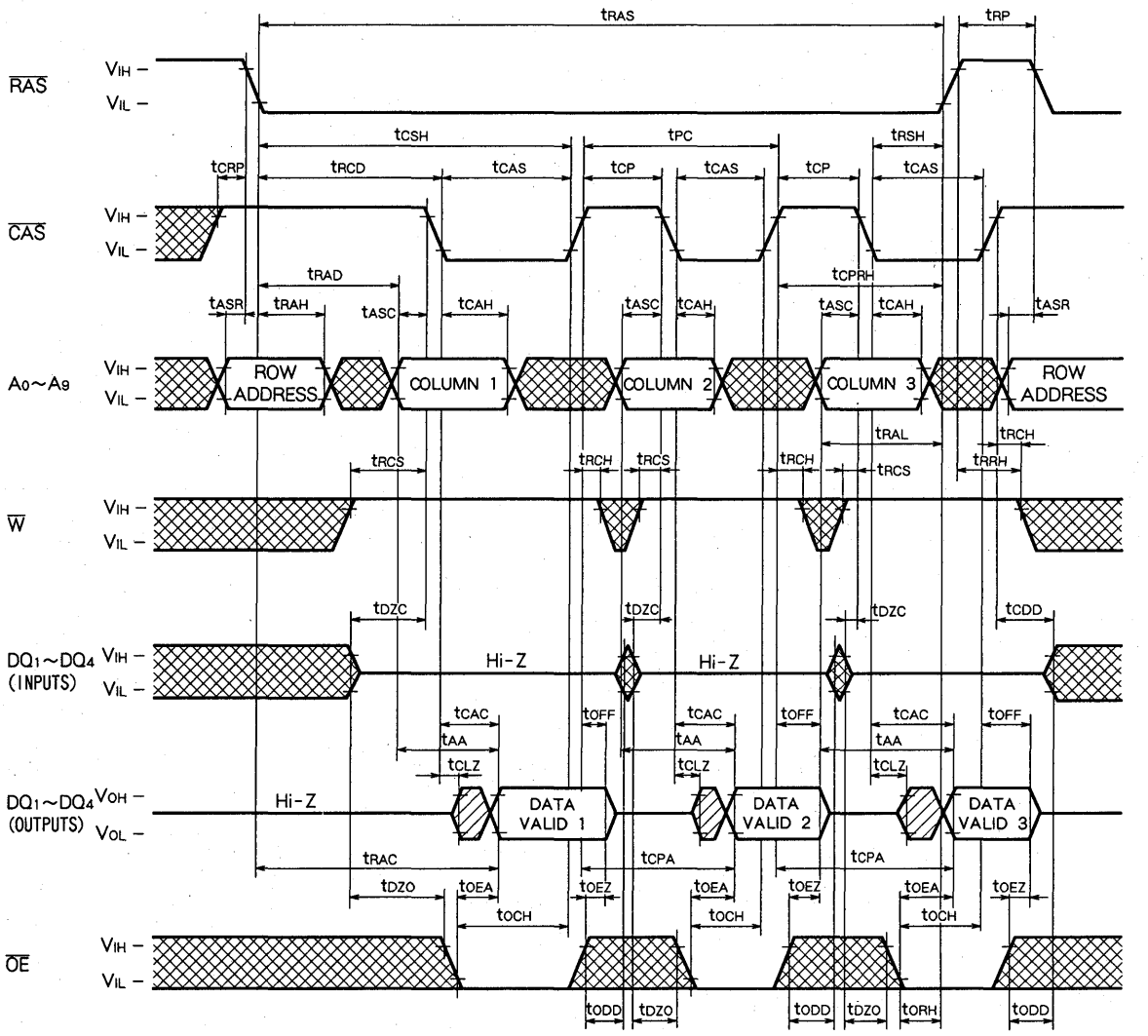


Hidden Refresh Cycle (Read) (Note 29)

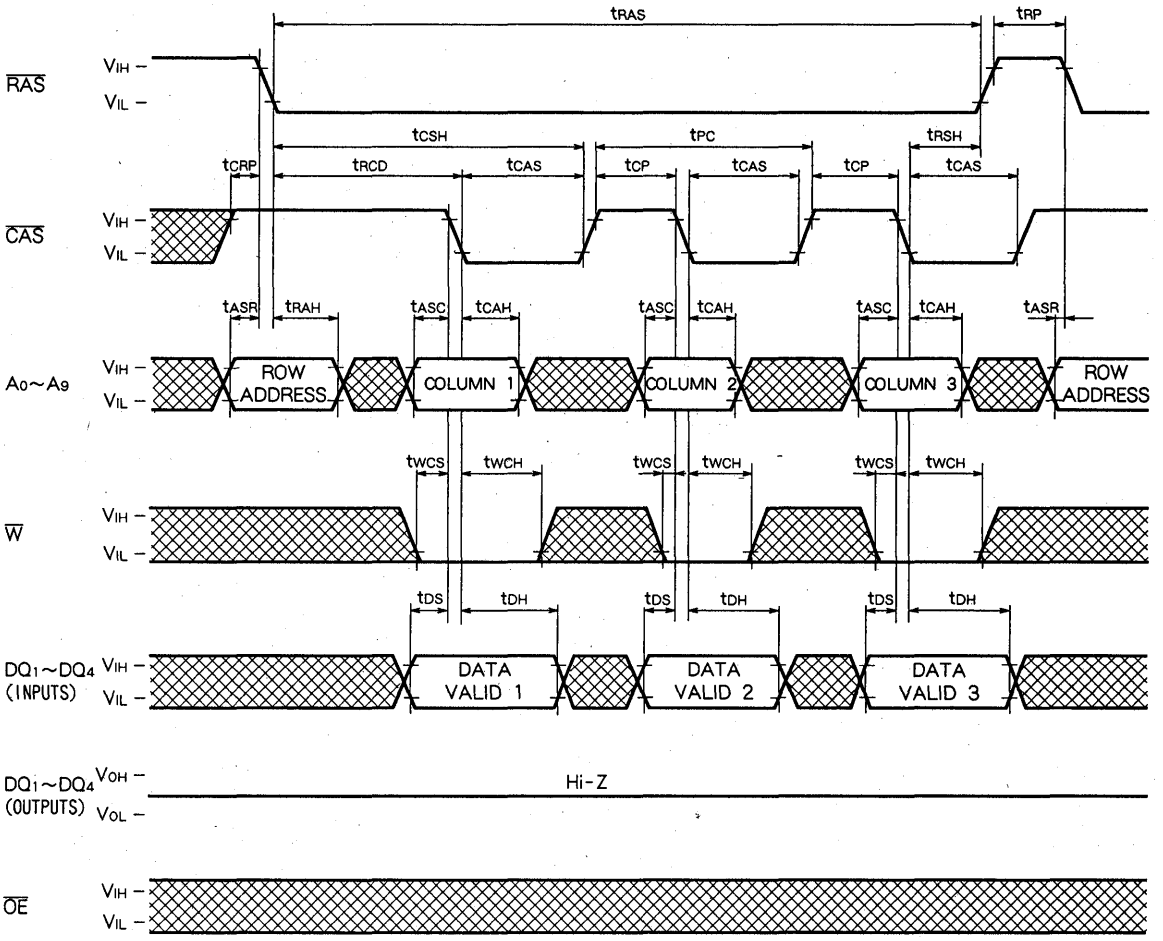


Note 29 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

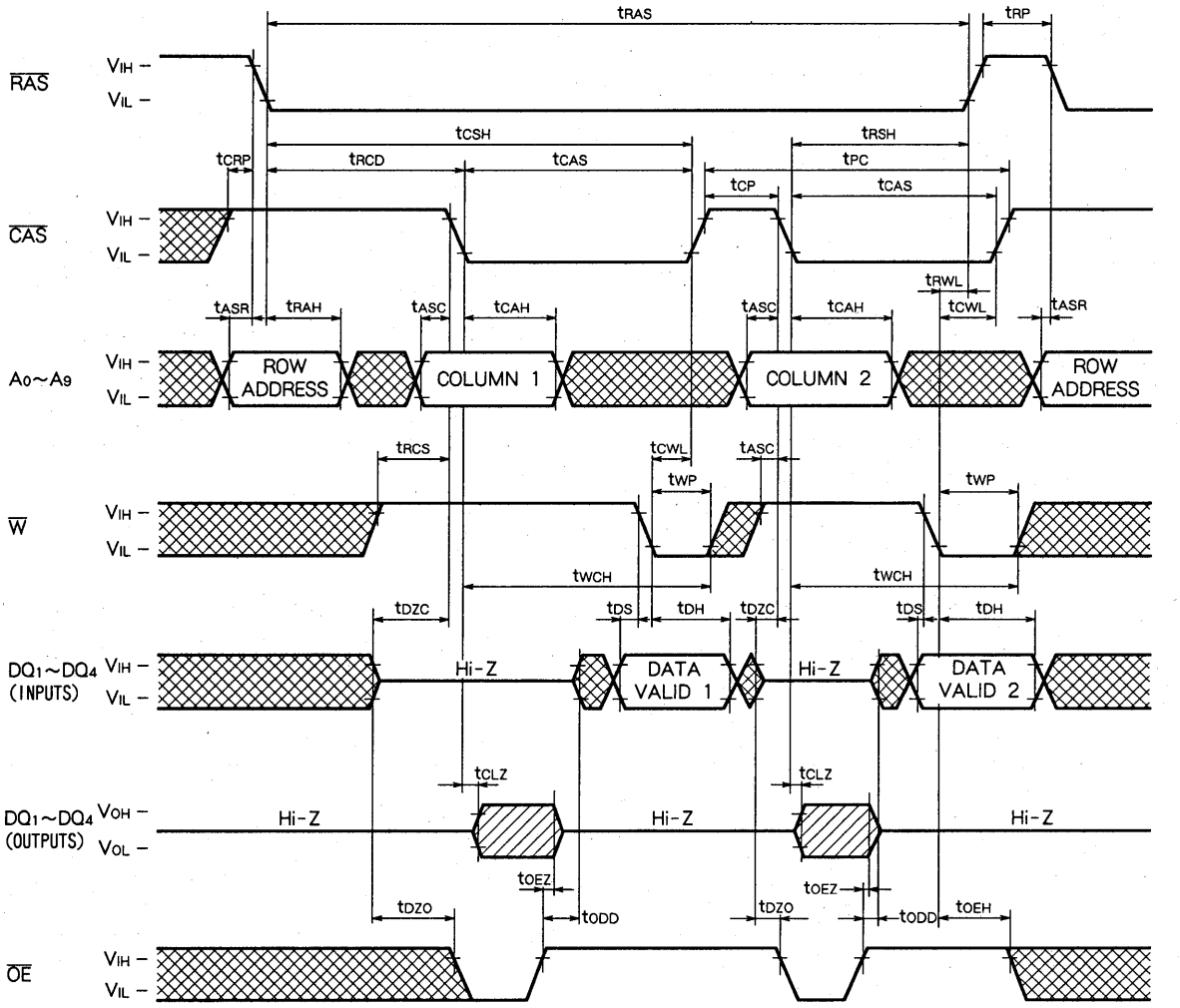
Fast Page Mode Read Cycle



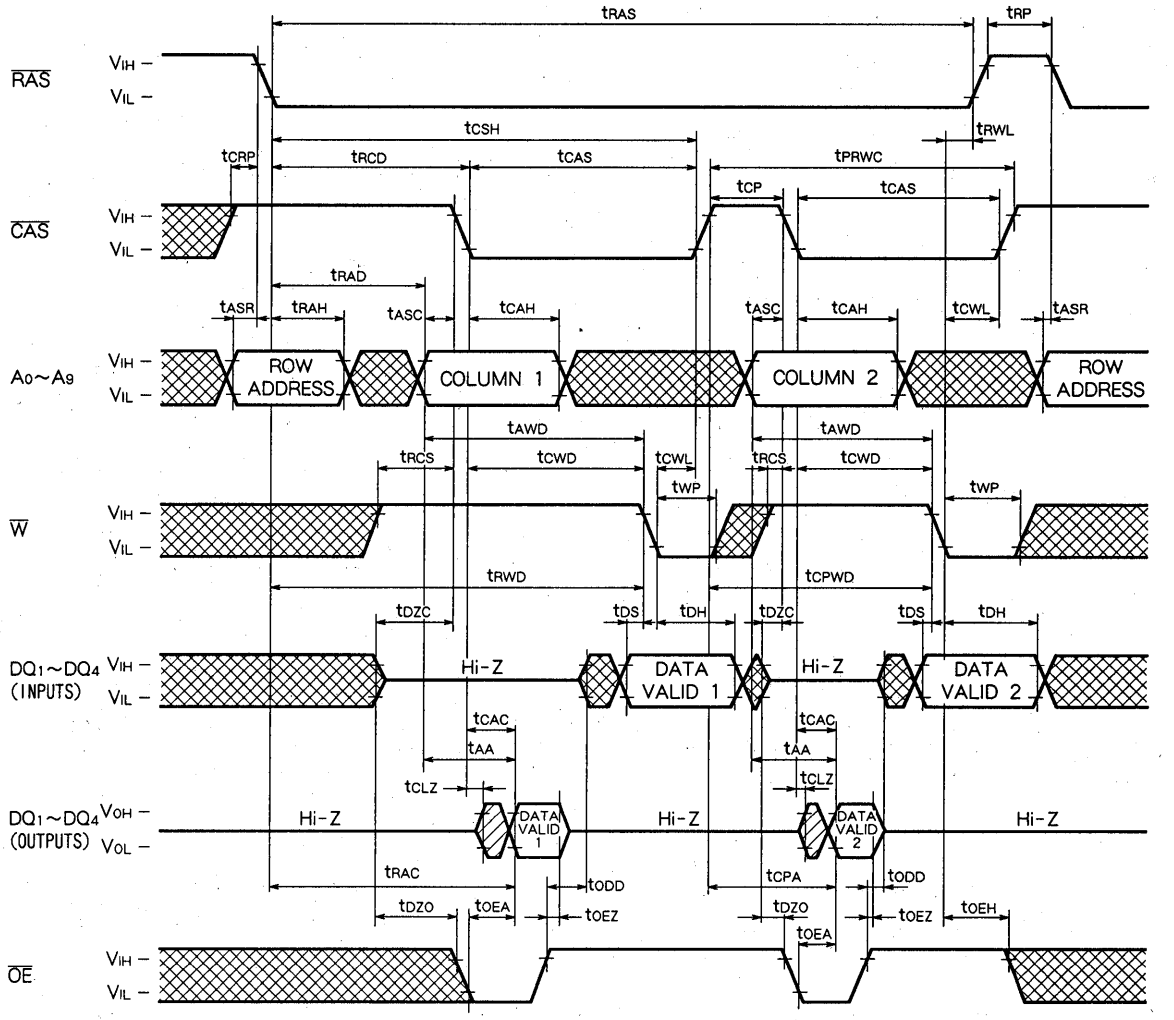
Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Write Cycle (Delayed Write)

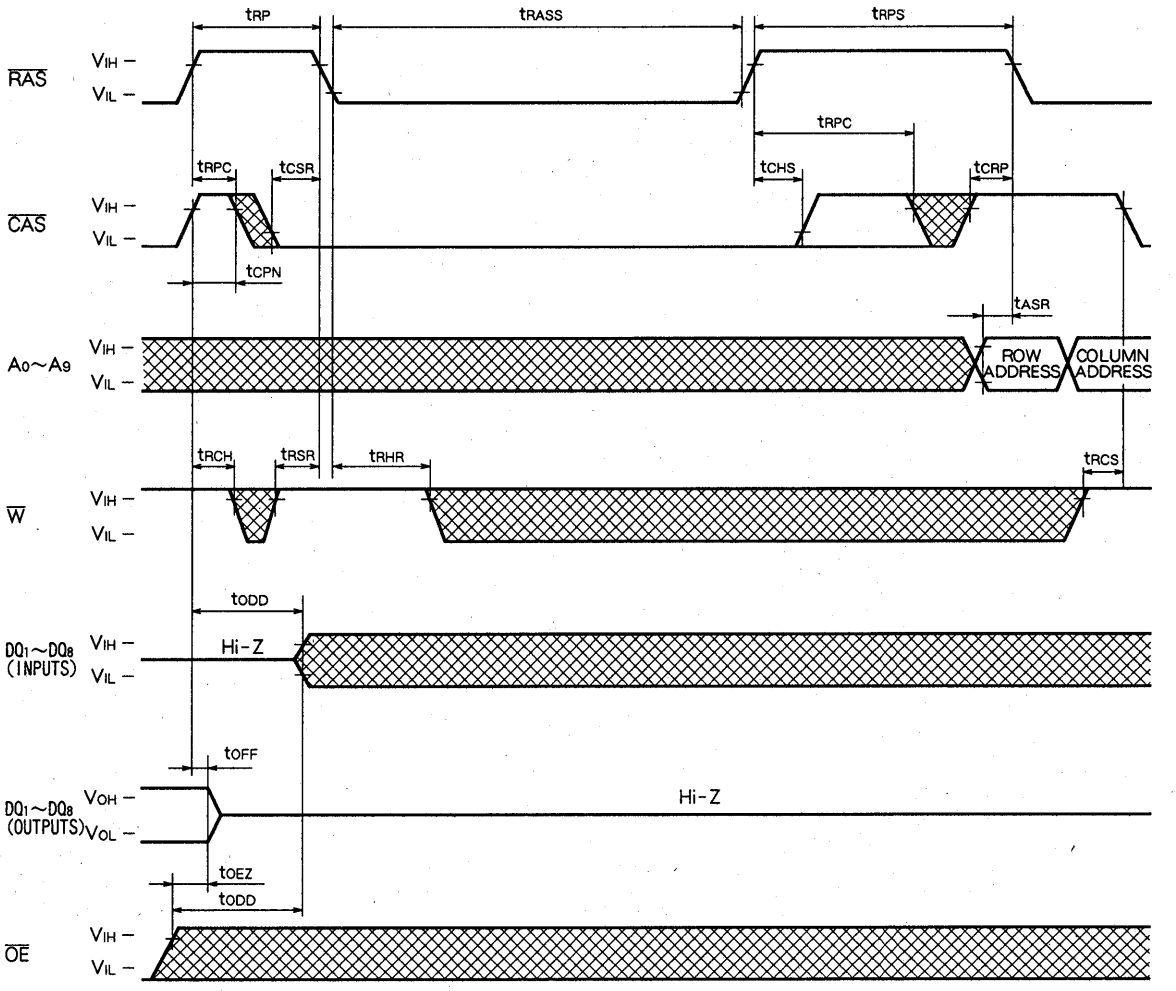


Fast Page Mode Read-Write, Read-Modify-Write Cycle



MITSUBISHI ELECTRIC

Self Refresh Cycle* (Note 30)



Note 30. Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

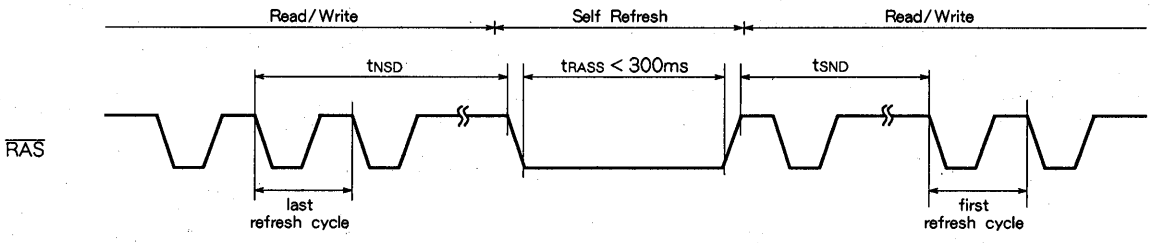
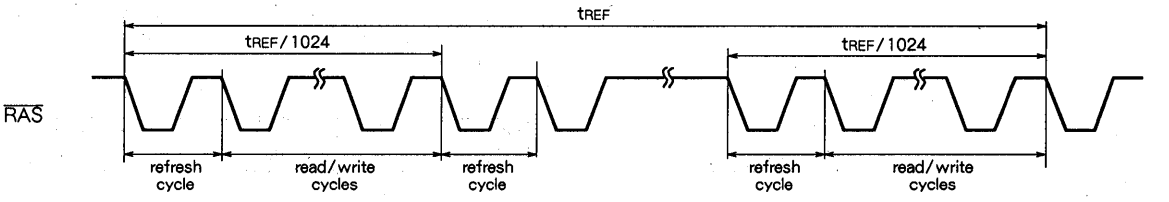


Table 2

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leq 16\ \mu s$	$t_{SND} \leq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 constant period (16 μs max) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note :
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

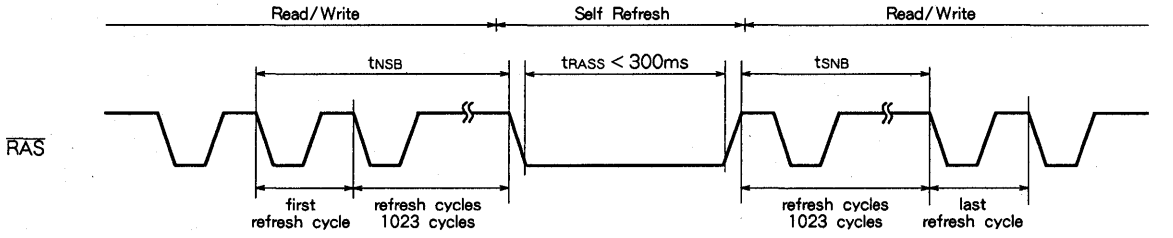
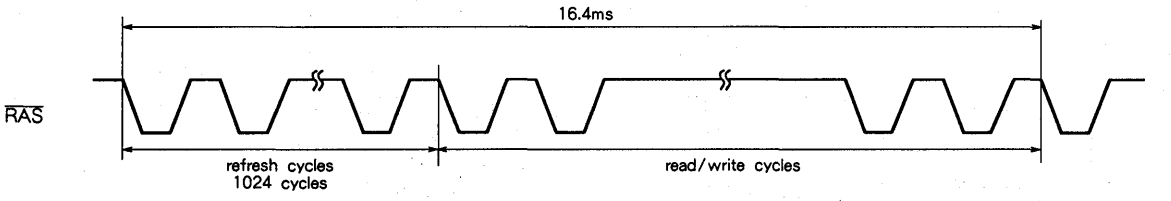


Table 3

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

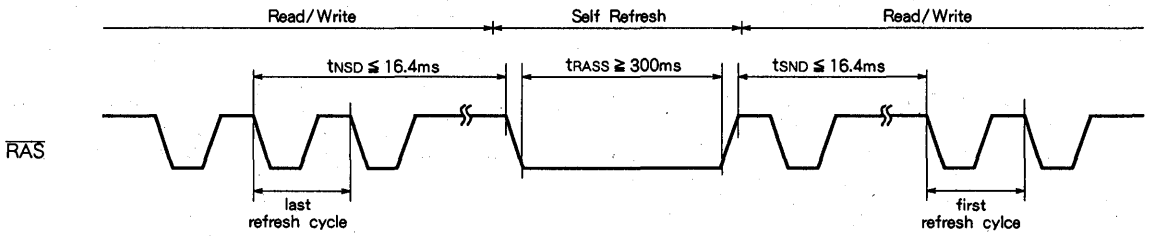
1.2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4ms.

1.2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read /write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram-A



Timing diagram-B

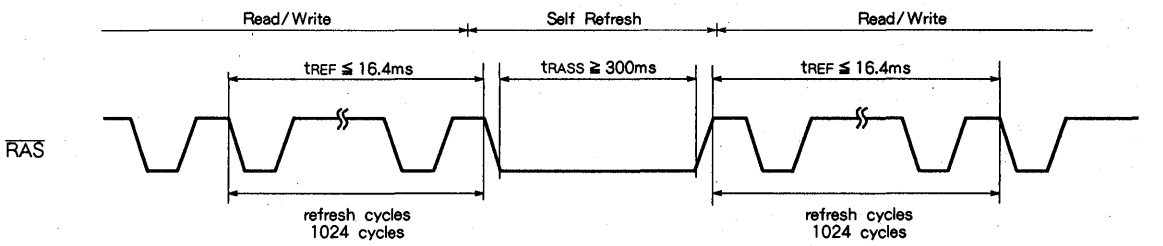


Table 4

Read/Write	Read/Write→Self Refresh	Self Refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
$\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read /write operation period should be set within 16.4ms.

2.1.2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh

- Before and after the self refresh, 1024 refresh cycles should be executed within 16.4ms for each refresh operation.

M5M4V4800TP-7,-8,-7S,-8S

FAST PAGE MODE 4194304-BIT (524288-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 524288-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit a reduction in pins and an increase in system density.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ. mW)
M5M4V4800TP-7, -7S	70	20	35	20	130	190
M5M4V4800TP-8, -8S	80	20	40	20	150	160

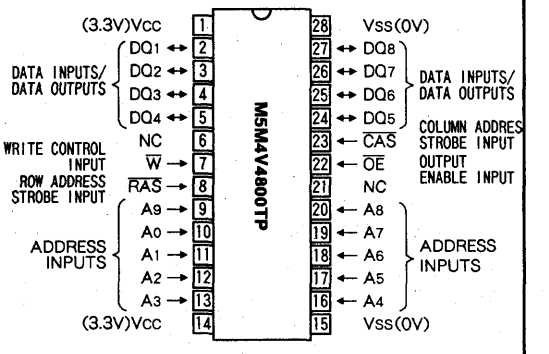
- Standard 28pin TSOP (II)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
  - CMOS input level ..... 2.52mW(max)
  - CMOS input level ..... 252μW(max)*
- Low operating power dissipation
  - M5M4V4800TP-7,-7S ..... 252mW(max)
  - M5M4V4800TP-8,-8S ..... 216mW(max)
- Self refresh capability*
  - Self refresh current ..... 120μA(max)
- Extended refresh capability*
  - Extended refresh current ..... 120μA(max)
- Fast-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early write mode and $\overline{OE}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9)*

* : Applicable to self refresh version (M5M4V4800TP -7S, -8S : option) only.

APPLICATION

Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 28P3Y-H (400mil TSOP Normal Bend)

NC : NO CONNECTION

FUNCTION

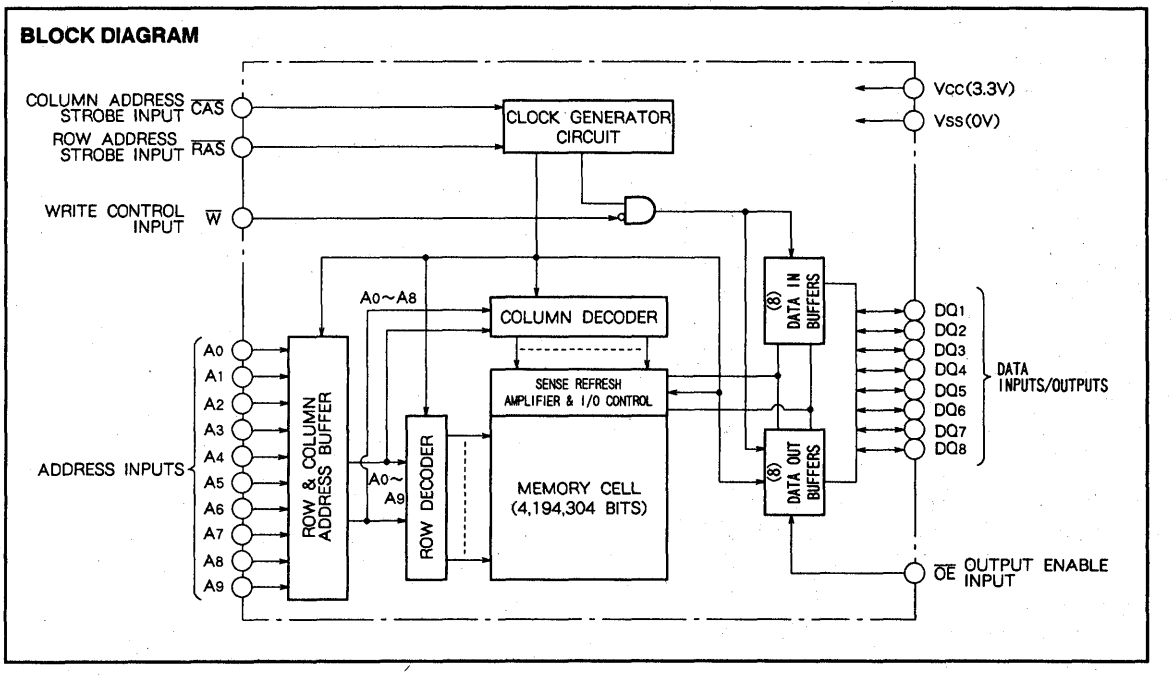
In addition to normal read, write, and read-modify-write operations the M5M4V4800TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode indential
Write(Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write(Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V \leq V_{OUT} \leq V_{CC}$	−5		5	μA
I_I	Input current		$0V \leq V_{IN} \leq V_{CC}+0.3V$, Other inputs pins=0V	−5		5	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3,4,5)	M5M4V4800-7,-7S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = twc = min. output open			70	mA
		M5M4V4800-8,-8S				60	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2V output open			0.5	
						0.07*	
$I_{CC3(AV)}$	Average supply current from V_{CC}, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V4800-7,-7S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			70	mA
		M5M4V4800-8,-8S				60	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-page-mode (Note 3,4,5)	M5M4V4800-7,-7S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			70	mA
		M5M4V4800-8,-8S				60	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M4V4800-7,-7S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			65	mA
		M5M4V4800-8,-8S				55	
$I_{CC8(AV)}$*	Average supply current from V_{CC}, Extended refresh mode (Note 6)		Stand-by: $\overline{RAS} \geq V_{CC}-0.2V$ $\overline{CAS} \geq V_{CC}-0.2V$ or $\overline{CAS} \leq 0.2V$ $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS} \leq 0.2V$ or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W} \leq 0.2V$ or $\geq V_{CC}-0.2V$ $\overline{OE} \leq 0.2V$ or $\geq V_{CC}-0.2V$ $A_0 \sim A_9 \leq 0.2V$ or $\geq V_{CC}-0.2V$ DQ=open t_{RC}=125μs $t_{RAS}=t_{RASmin}\sim 1\mu s$			120	μA
$I_{CC9(AV)}$*	Average supply current from V_{CC}, Self refresh mode (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V output open			120	μA

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance,address inputs	V_I = Vss f = 1MHz V_I = 25mVrms			6	pF
$C_{I(\overline{OE})}$	Input capacitance,$\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance,write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance,$\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance,$\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted, See notes 6, 13, 14)

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		70		80	ns
t_{AA}	Column Address access time	(Note 7, 10)		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	20	0	20	ns

Note 6 : An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh.)
Note that $\overline{RAS}$ may be cycled during the initial pause. Any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods(greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 100pF, V_{OH} = 2.4V(I_{OH} = − 2mA) and V_{OL} = 0.4V(I_{OL} = 2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8 : Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9 : Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If either t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table. t_{RAC} will increase by the amount which t_{RCD} or t_{RAD} exceeds the value shown.

10 : Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11 : Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12 : $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 5\mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted, See notes 13, 14)

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4	ms
t_{REF}	Refresh cycle time *			128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 19)	20		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 19)	20		20		ns
t_T	Transition time	(Note 20)	1	50	1	50	ns

Note 13 : The timing requirements are assumed t_T = 5ns.

14 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

15 : Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only ; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

16 : Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only ; if t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{CAC} or t_{AA}.

17 : Operation within the $t_{ASC(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{ASC(max)}$ is specified as a reference point only ; if t_{ASC} is greater than the specified $t_{ASC(max)}$ limit and t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

18 : Either t_{DZC} or t_{DZO} must be satisfied.

19 : Either t_{CDD} or t_{ODD} must be satisfied.

20 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		20		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		20		20		ns

Note 21 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		20		ns
t_{WP}	Write pulse width		15		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 22)	175		195		ns
t_{RAS}	$\overline{RAS}$ low pulse width		115	10000	125	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		65	10000	65	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		115		125		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		65		65		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	40		40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	90		100		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		20		ns
t_{WP}	Write pulse width		15		15		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		20		20		ns

Note 22 : t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

23 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M4V4800-7, -7S		M5M4V4800-8, -8S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		95		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 25)	115	100000	135	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 26)	10	15	10	20	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	40		45		ns

Note 24 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25 : $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26 : $t_{CP(max)}$ is specified as a refereńce point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits				Unit
		M5M4V4800-7, -7S		M5M4V4800-8, -8S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	30		30		ns

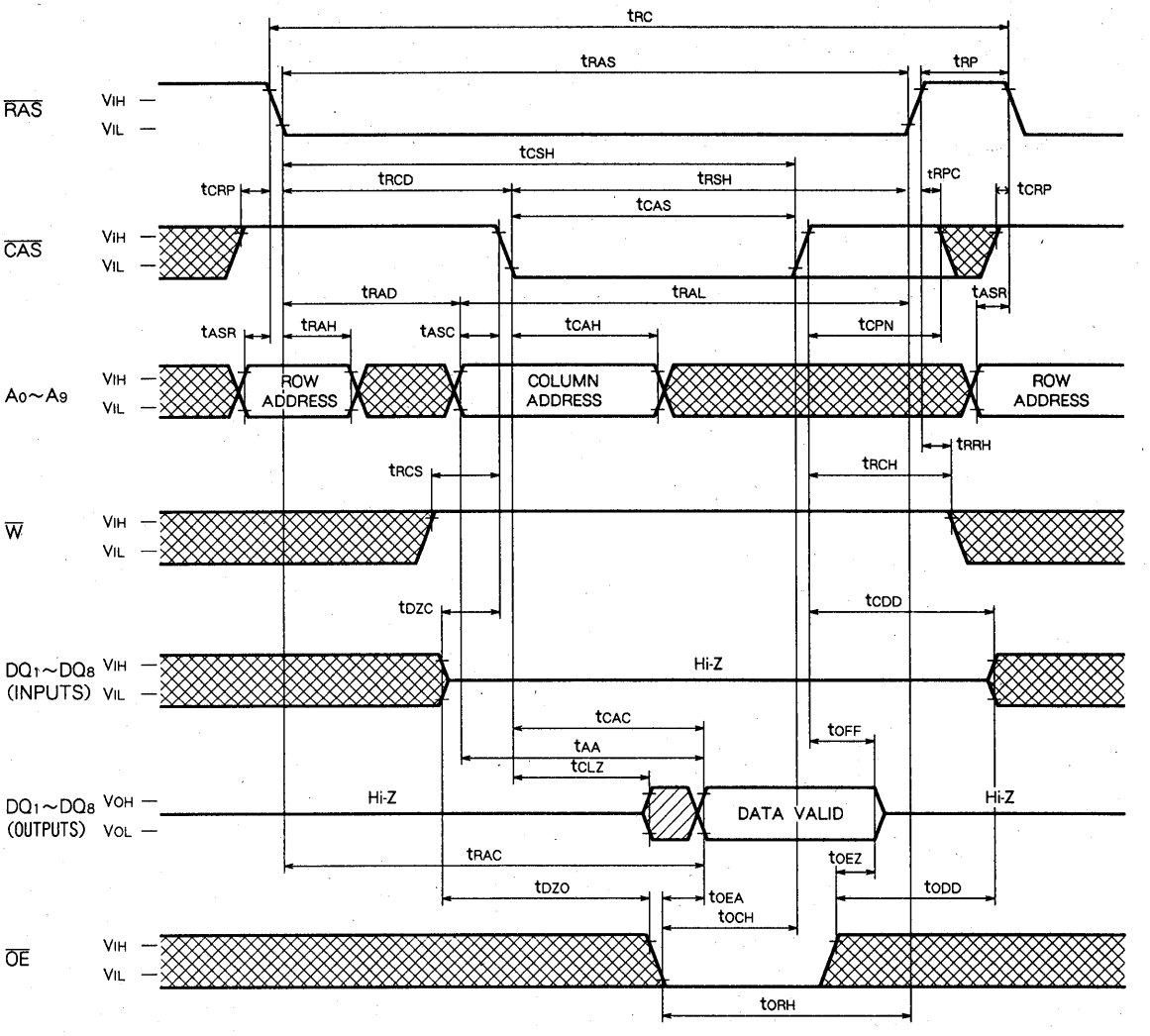
Note 27 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits				Unit
		M5M4V4800-7, -7S		M5M4V4800-8, -8S		
		Min	Max	Min	Max	
t_{RASS}	$\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	$\overline{RAS}$ high pulse width	130		150		ns
t_{CHS}	$\overline{CAS}$ hold time after $\overline{RAS}$ high	− 50		− 50		ns

Timing Diagrams (Note 28)

Read Cycle



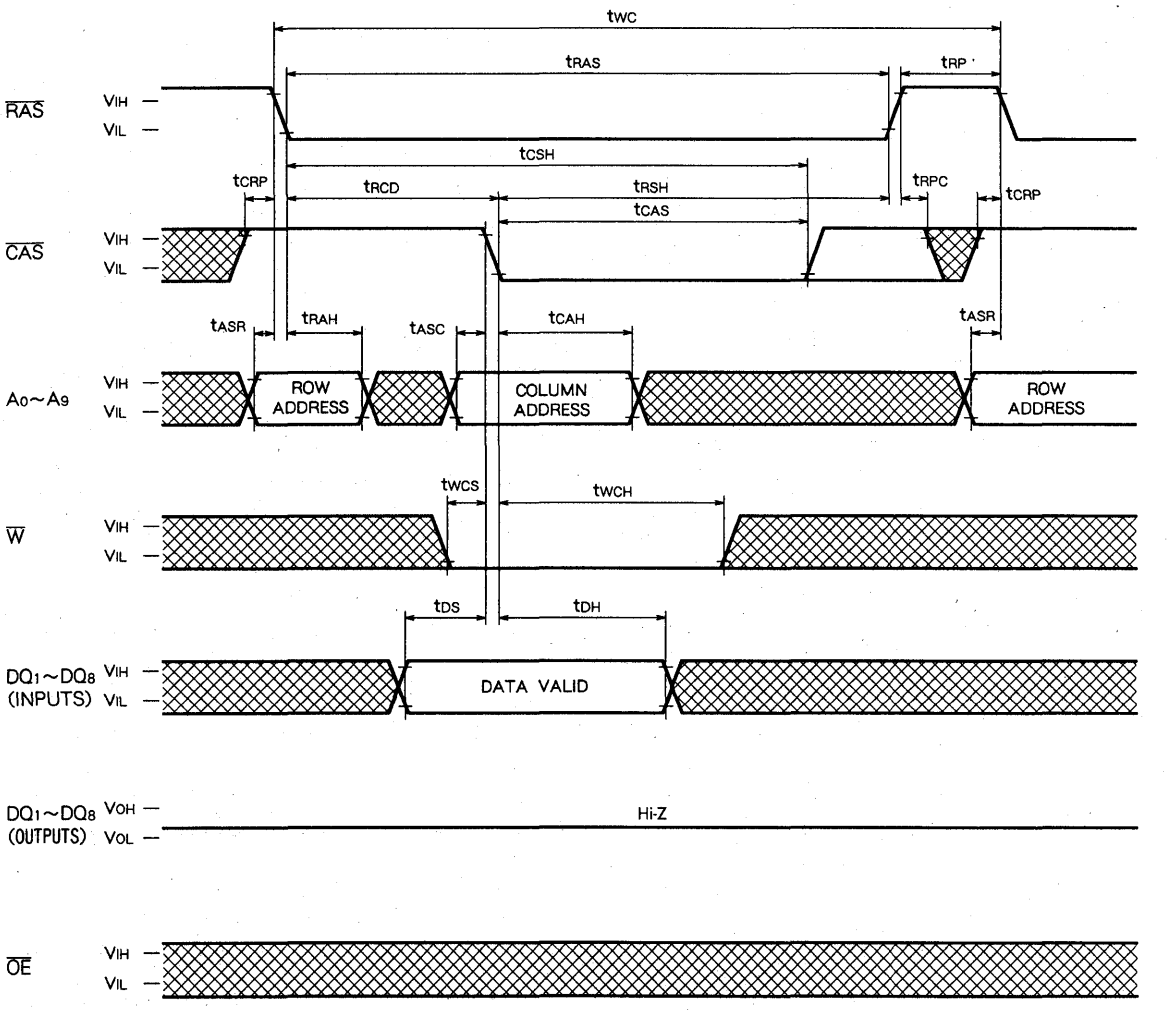
Note 28

Indicates the don't care input
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

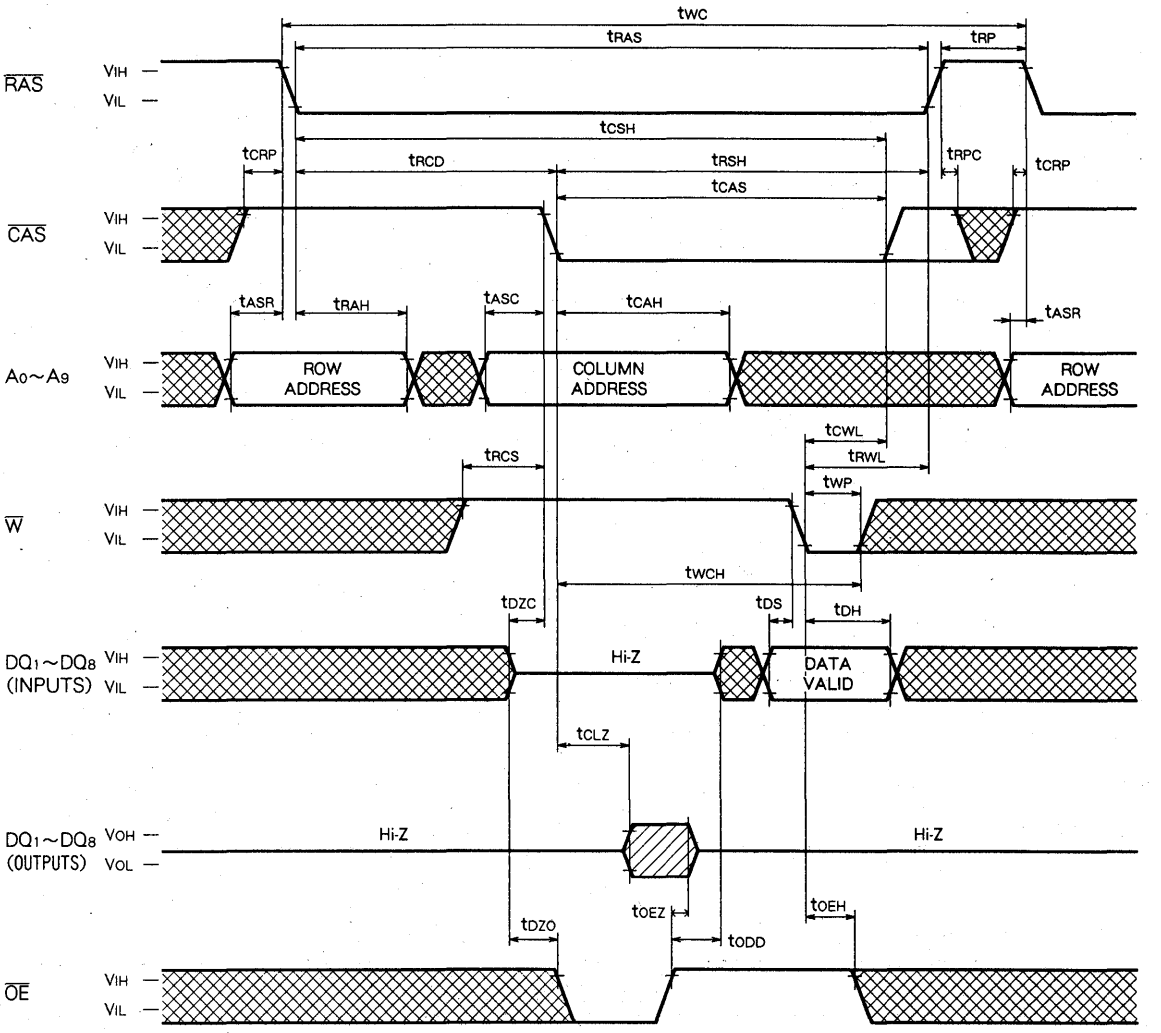
Indicates the invalid output

Only t_{ASR} and t_{RAH} are specified for A9 input.

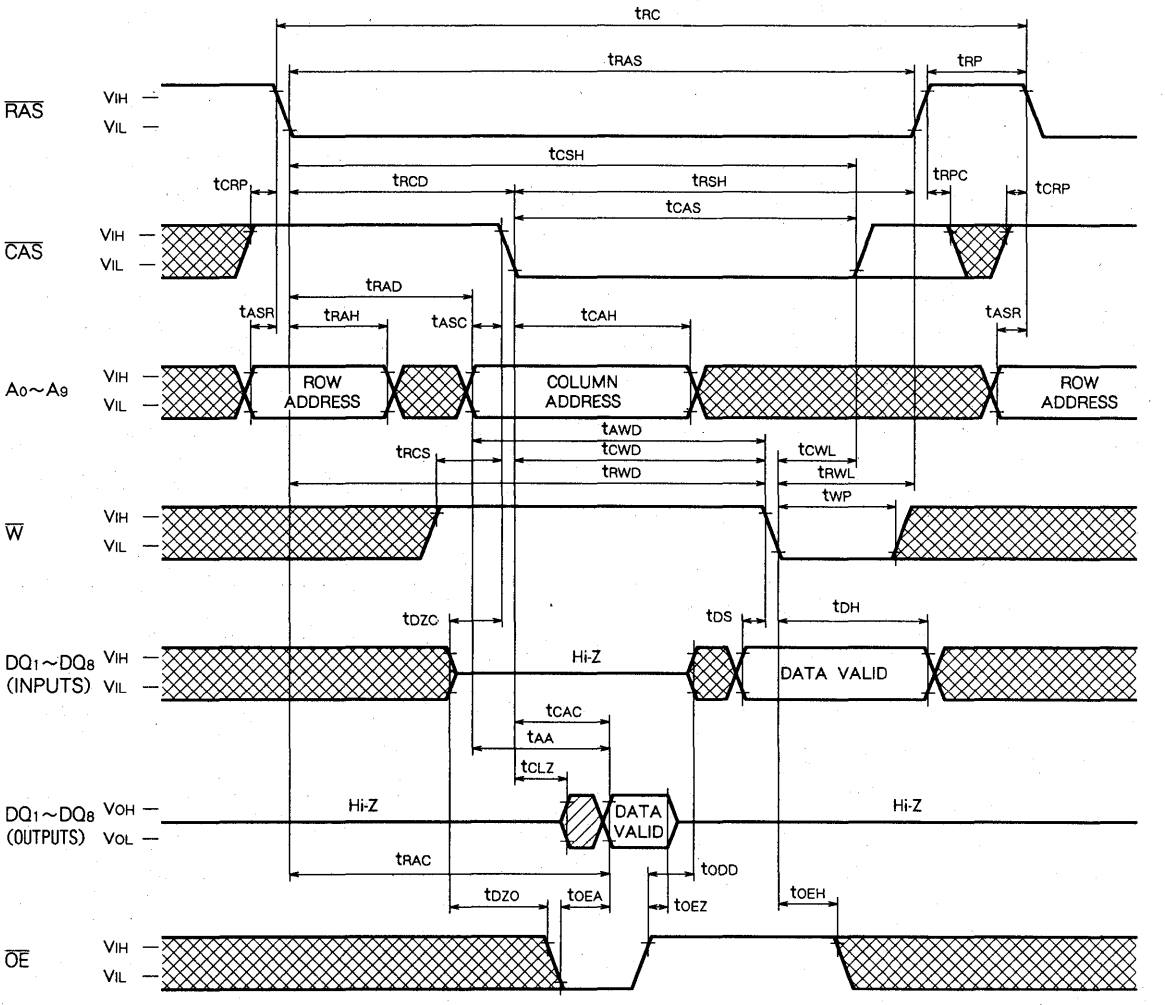
Write Cycle (Early Write)



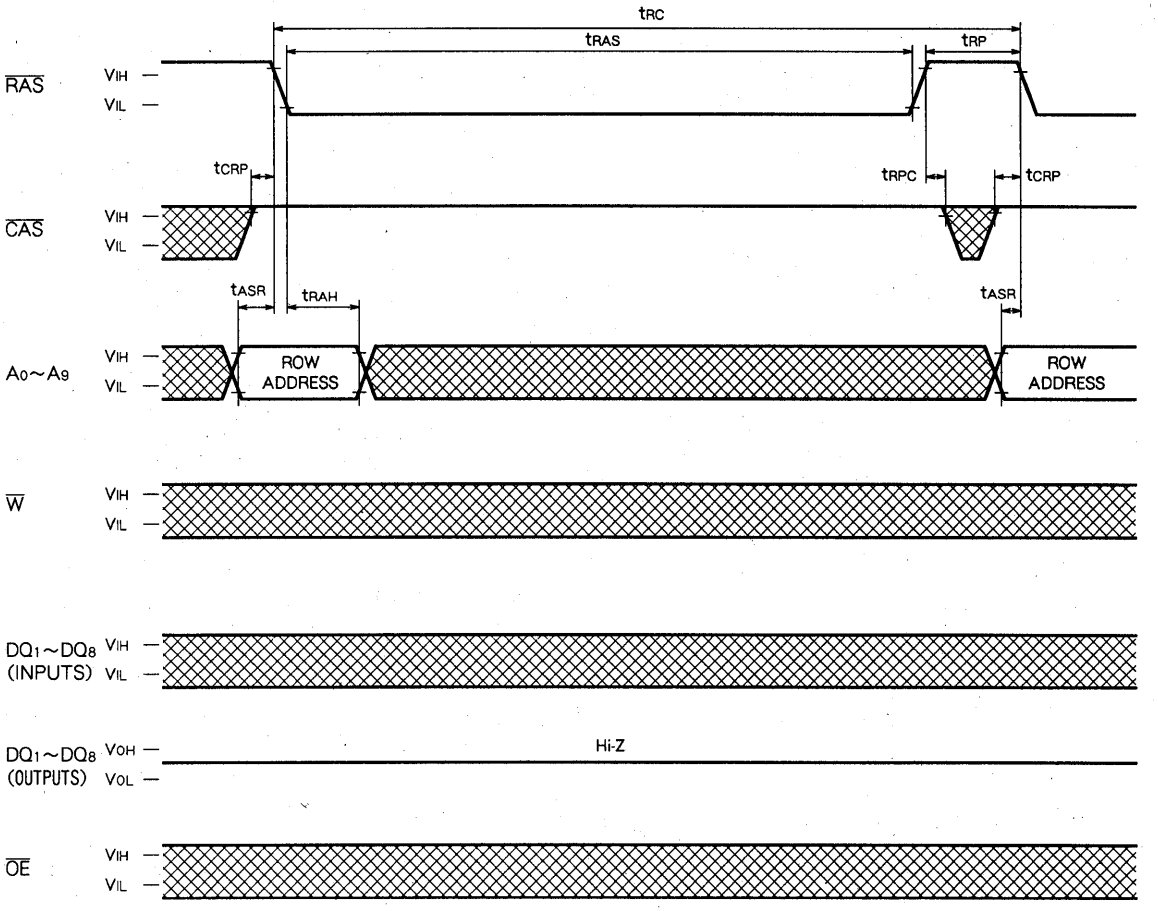
Write Cycle (Delayed Write)



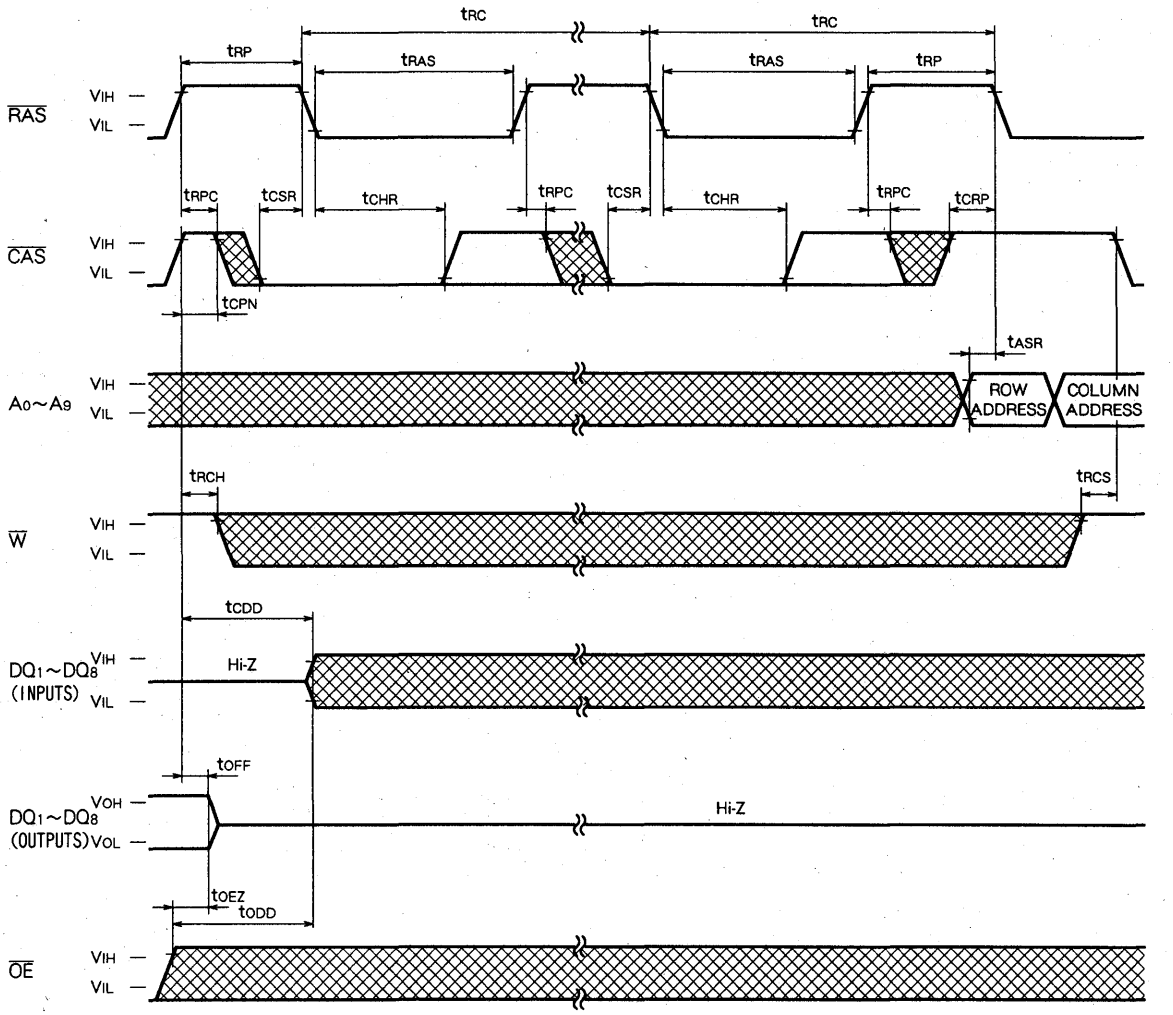
Read-Write, Read-Modify-Write Cycle



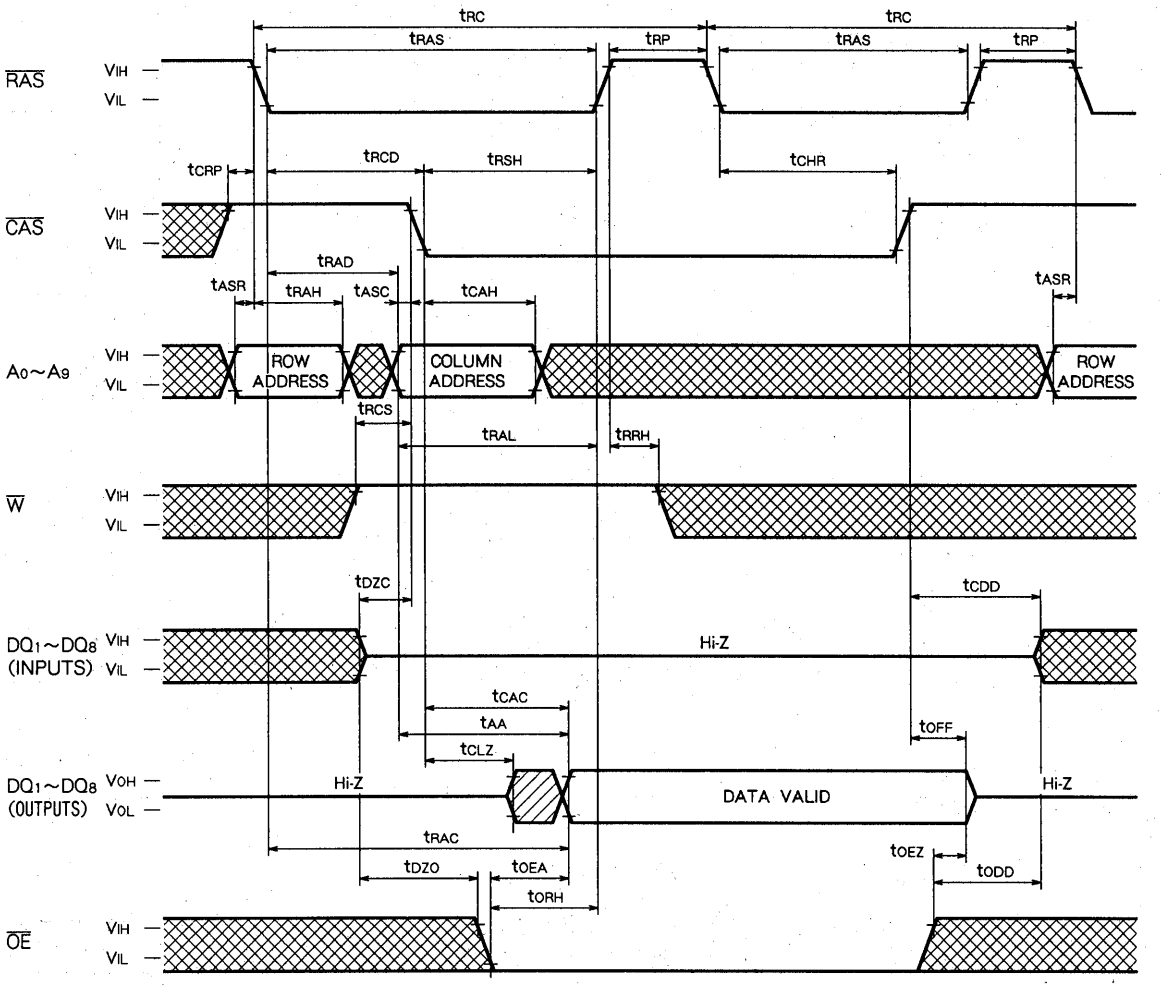
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

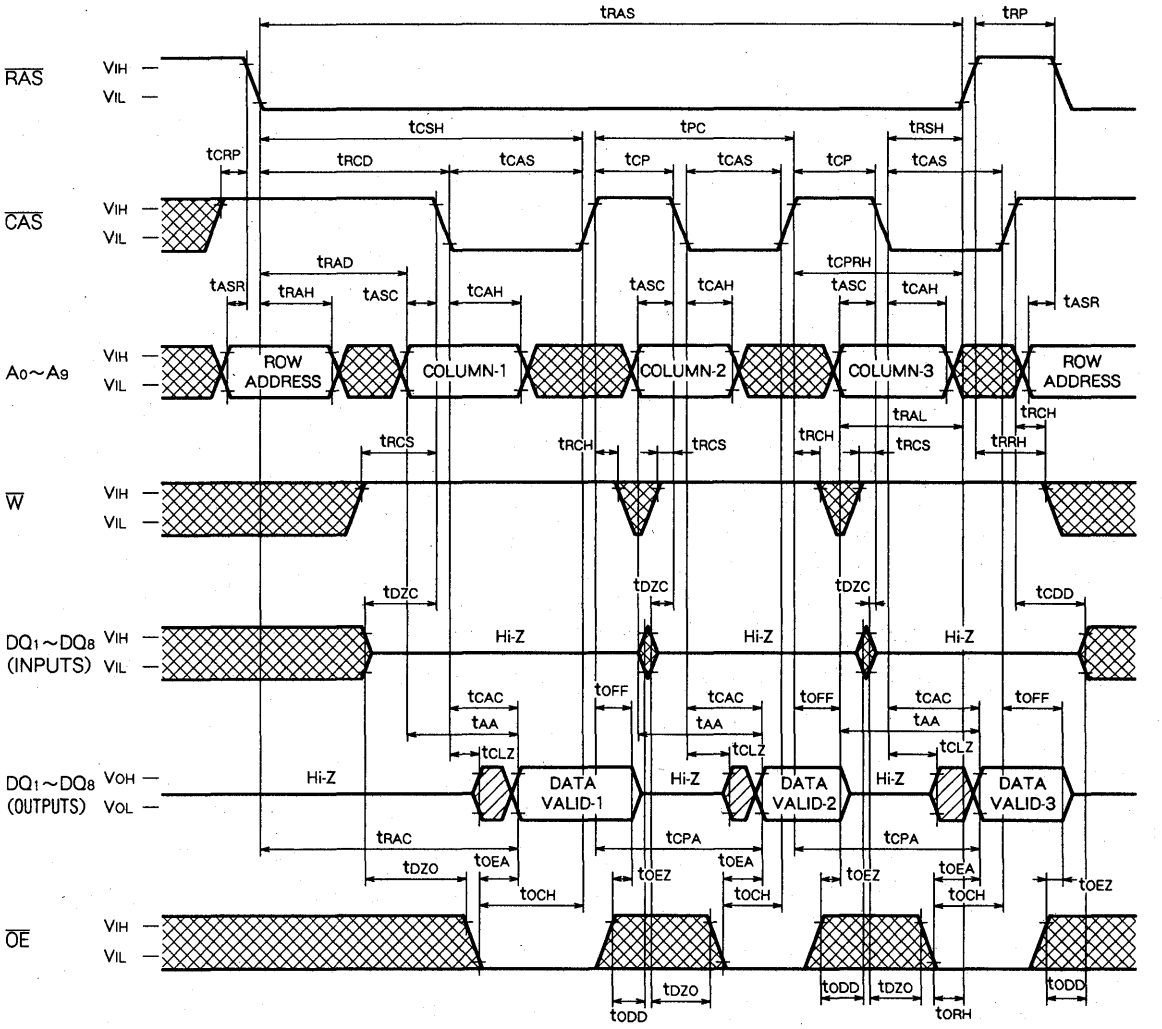


Hidden Refresh Cycle (Read) (Note 29)

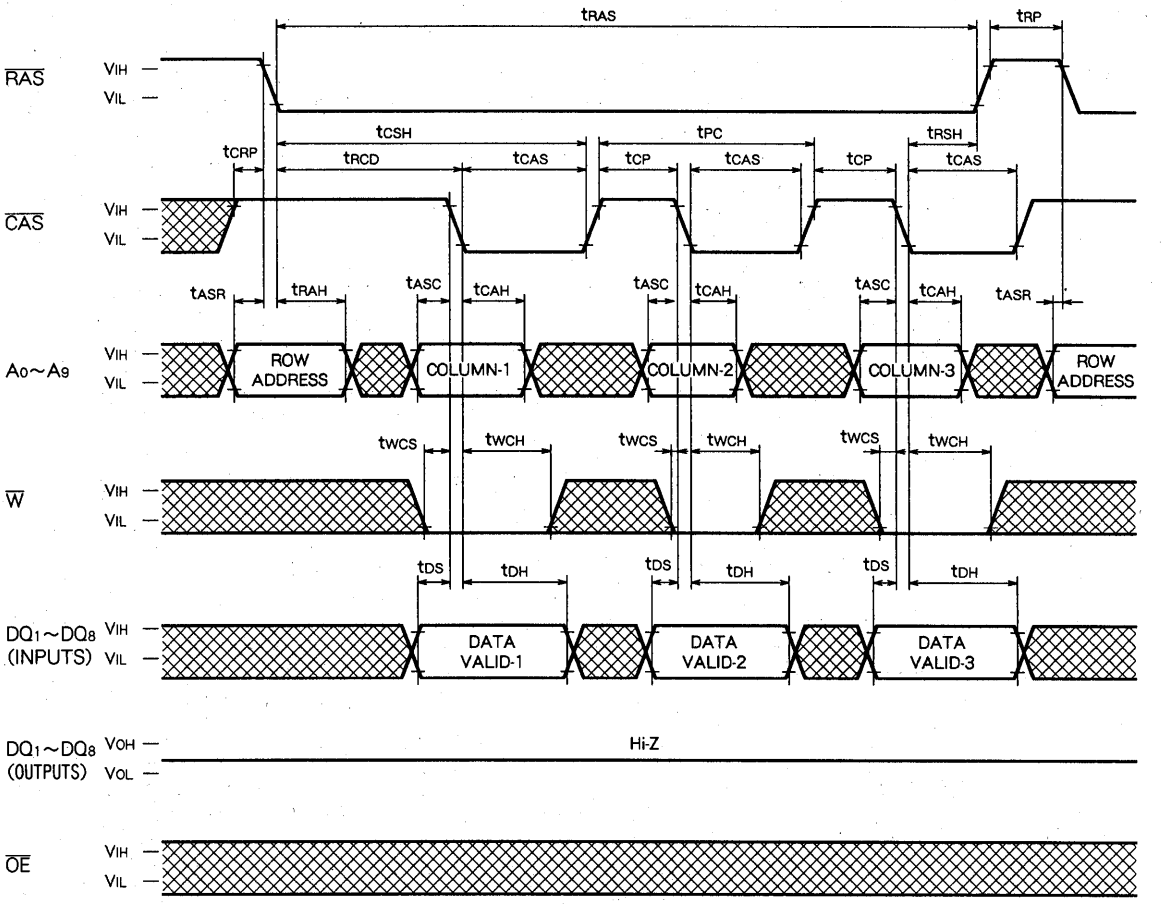


Note 29. Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

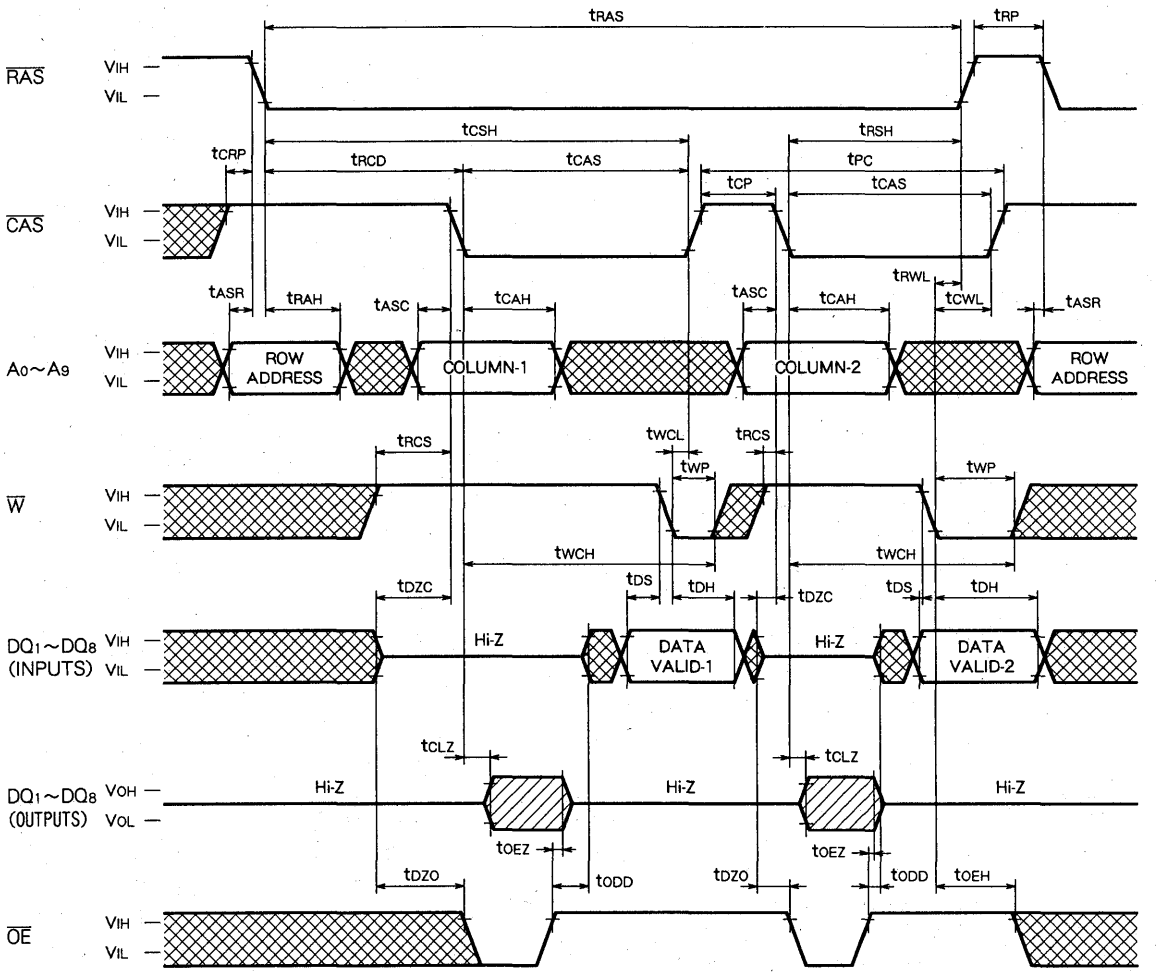
Fast Page Mode Read Cycle



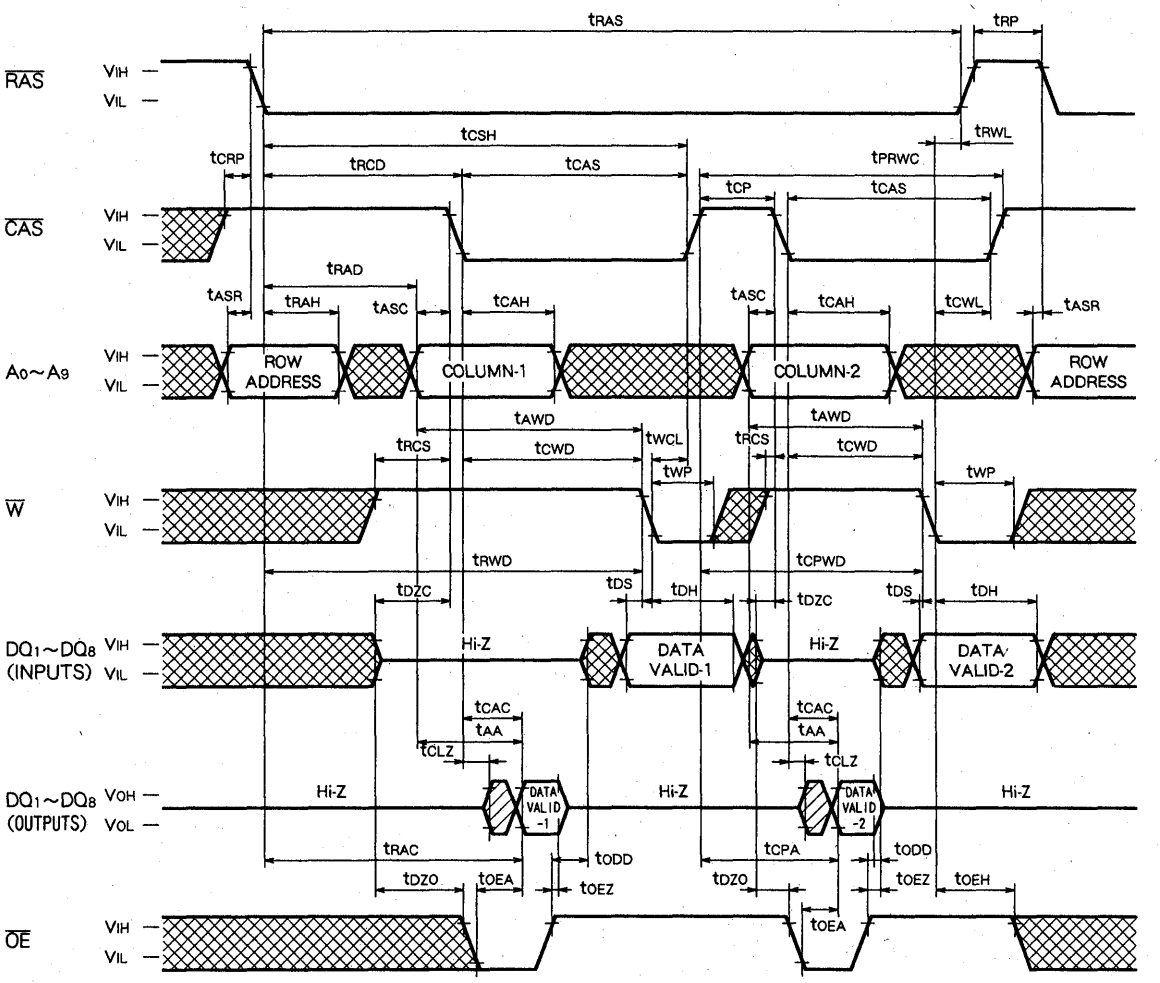
Fast Page Mode Write Cycle (Early Write)



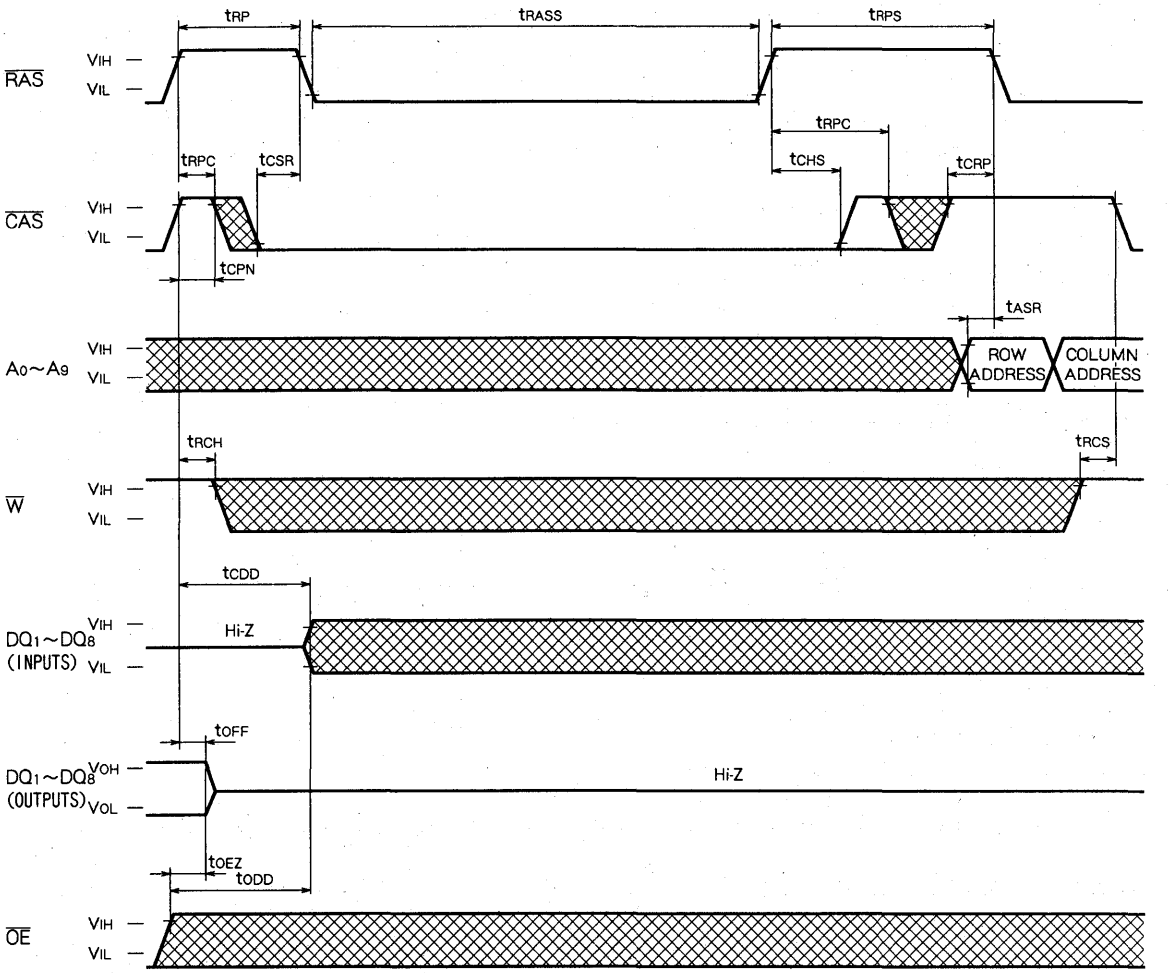
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 30)



Note 30. Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

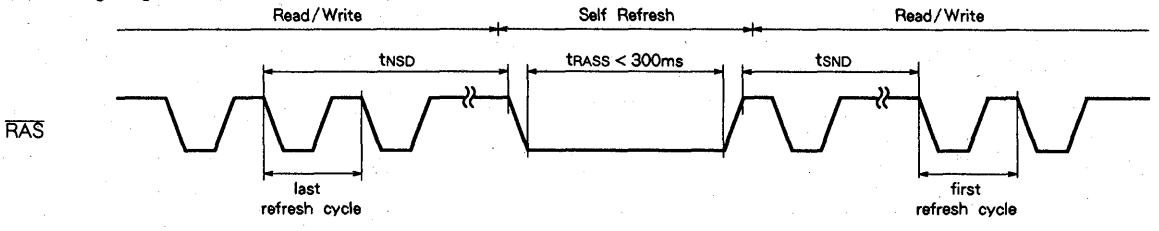
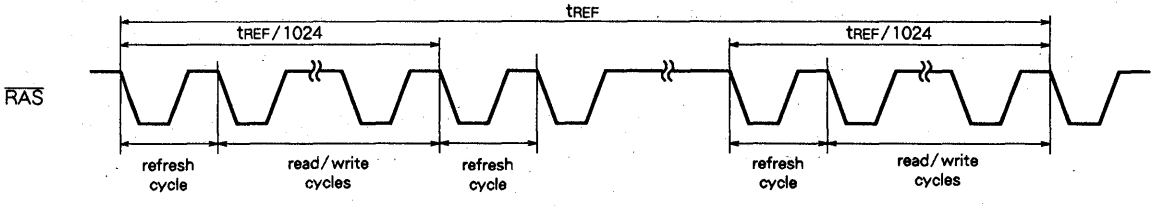


Table 2

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh (Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125μs max) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 constant period (16μs max) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note :

Hidden refresh may be used instead of CBR refresh.

$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

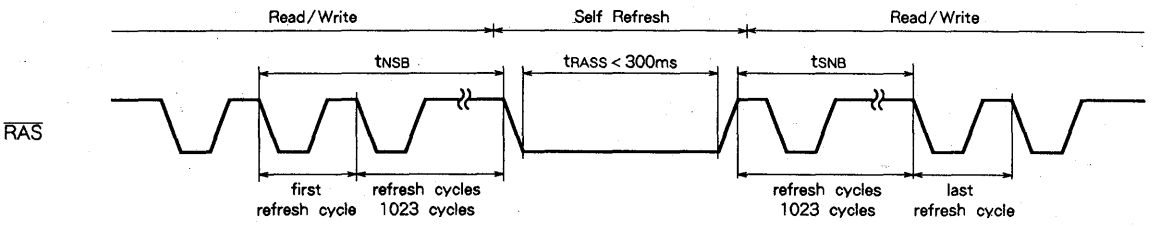
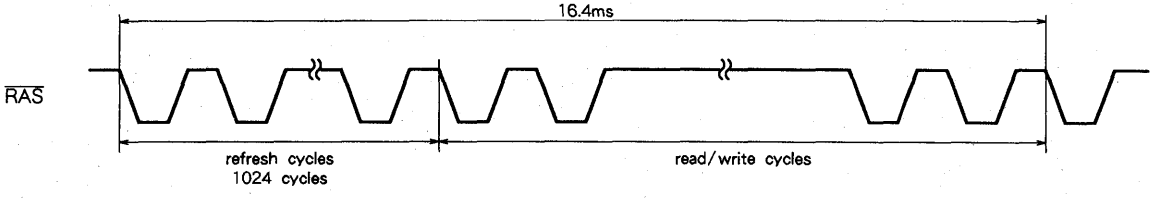


Table 3

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only burst refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

1.2.1 CBR burst refresh

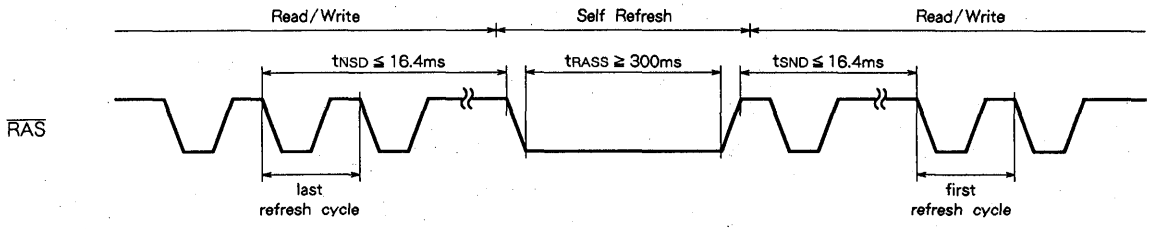
- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

1.2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geq 300ms$

(A) Timing diagram-A



Timing diagram-B

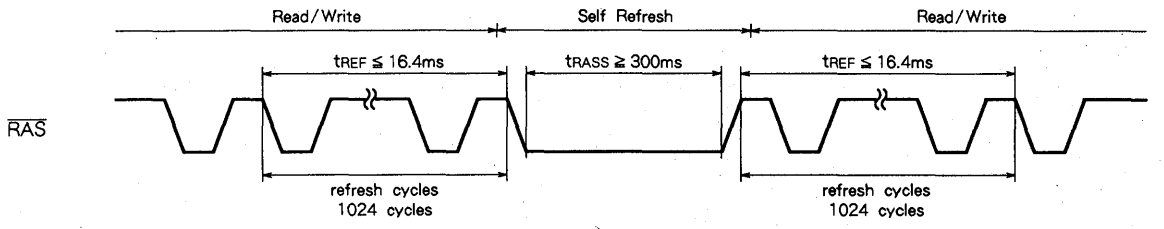


Table 4

Read/Write	Read/Write→Self Refresh	Self Refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
$\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.1.2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh

- Before and after the self refresh, 1024 refresh cycles should be executed within 16.4ms for each refresh operation.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V4800CTP-6,-7,-6S,-7S

FAST PAGE MODE 4194304-BIT (524288-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 524288-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4800CTP-6,-6S	60	15	30	15	110	230
M5M4V4800CTP-7,-7S	70	20	35	20	130	200

- Standard 28pin TSOP (Ⅱ)
- Single 3.3V±0.3V supply
- Low stand-by power dissipation
  - CMOS Input level ----------5.5mW (Max)
  - CMOS Input level ----------550 μW (Max) *
- Operating power dissipation
  - M5M4V4800CTP-6,-6S ----------270mW (Max)
  - M5M4V4800CTP-7,-7S ----------234mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 100 μA(Max)
- Extended refresh capability
  - Extended refresh current ---------- 100 μA(Max)
- Fast page mode(1024-column random access),Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{CAS}$ and $\overline{OE}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0 ~A_9)
- 1024 refresh cycles every 128ms (A_0 ~A_9) *

*: Applicable to self refresh version (M5M4V4800CTP-6S, -7S :option) only

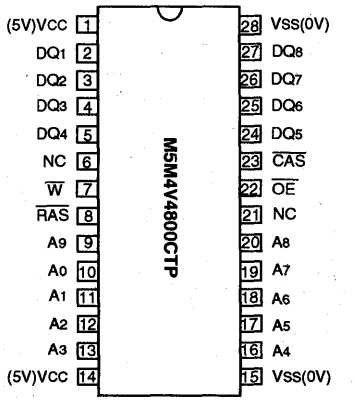
APPLICATION

Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_8	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P3Y-H(400mil TSOP Normal Bend)

NC:NO CONNECTION

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 4194304-BIT (524288-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

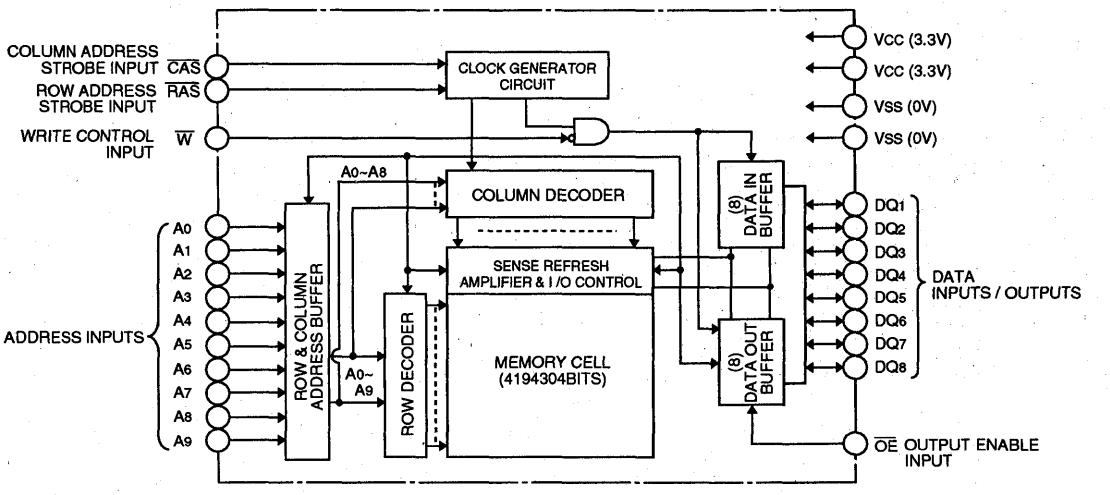
In addition to normal read, write, and read-modify-write operations the M5M4V4800CTP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
V_I	Input voltage		-0.5 ~ 4.6	V
V_O	Output voltage		-0.5 ~ 4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦V_{CC}	-5		5	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}+0.3V, Other inputs pins=0V	-5		5	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V4800C-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			75	mA
		M5M4V4800C-7,-7S				65	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧V_{CC} -0.2V output open			0.5	
						0.1*	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V4800C-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			75	mA
		M5M4V4800C-7,-7S				65	
I_{CC4}(AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M4V4800C-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			75	mA
		M5M4V4800C-7,-7S				65	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V4800C-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			65	mA
		M5M4V4800C-7,-7S				55	
I_{CC8}(AV)*	Average supply current from Vcc, Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_9≦0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=125 μs, t_{RAS}=t_{RAS}min~1 μs			100	μA
I_{CC9}(AV)*	Average supply current from Vcc, Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			100	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		15		20	ns

Note 6:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$- only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7:Measured with a load circuit equivalent to 100pF, V_{OH}(I_{OH}=-2mA) and V_{OL}(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V(V_{OL}).
8:Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9:Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10:Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11:Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12:$t_{OFF(max)}$, $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10 \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~70°C , Vcc = 3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4	ms
tREF	Refresh cycle time*			128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	15		20		ns
tT	Transition time	(Note 20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tT=5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
16: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
		Min	Max	Min	Max	
tRC	Read cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 21)	0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
			Min	Max	Min	Max	
tWC	Write cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
tWP	Write pulse width		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
			Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	150		180		ns
tRAS	$\overline{RAS}$ low pulse width		100	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		55	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		55		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	35		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	80		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	50		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
tWP	Write pulse width		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle	(Note 25)	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits				Unit
		M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		25		ns

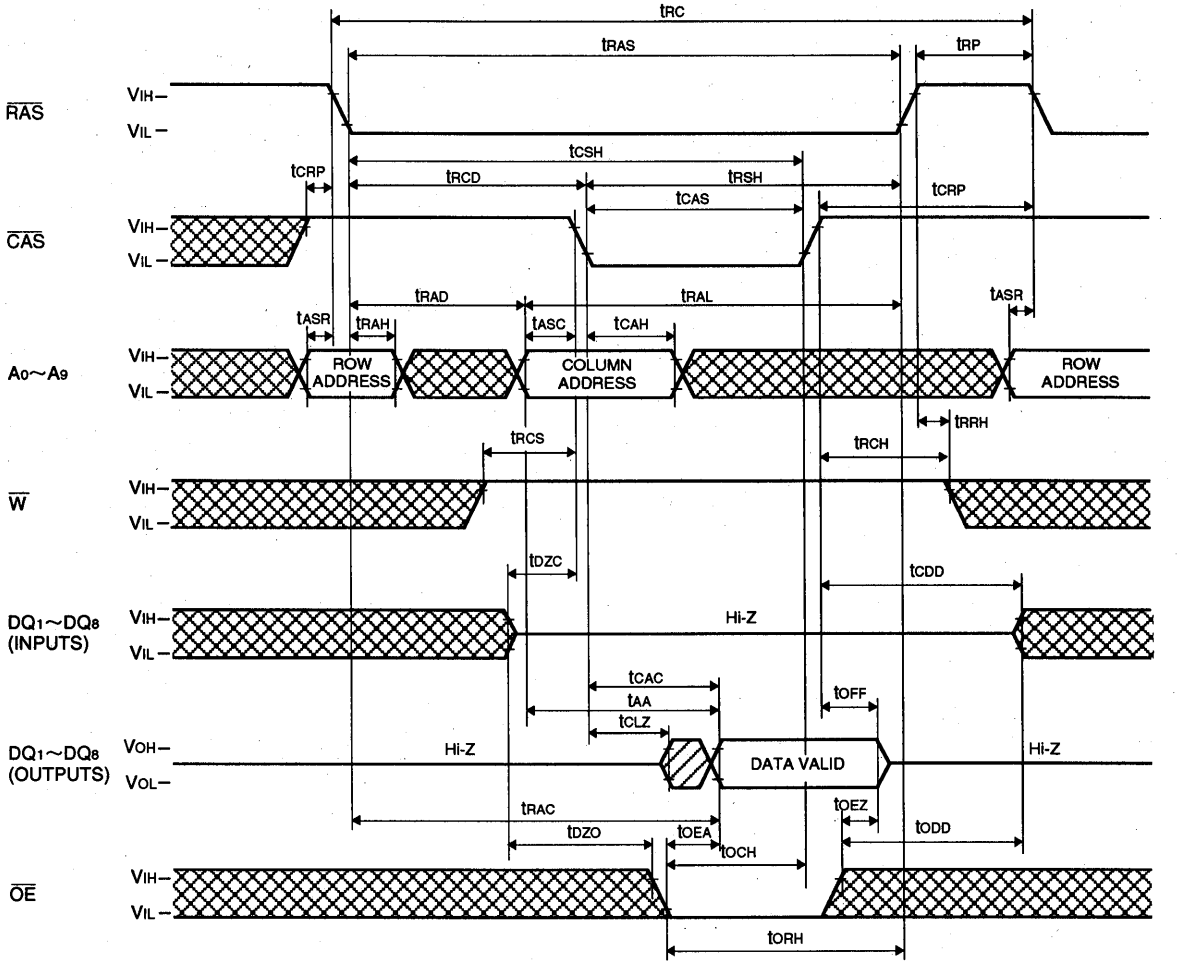
Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits				Unit
		M5M4V4800C-6,-6S		M5M4V4800C-7,-7S		
		Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 29)
Read Cycle



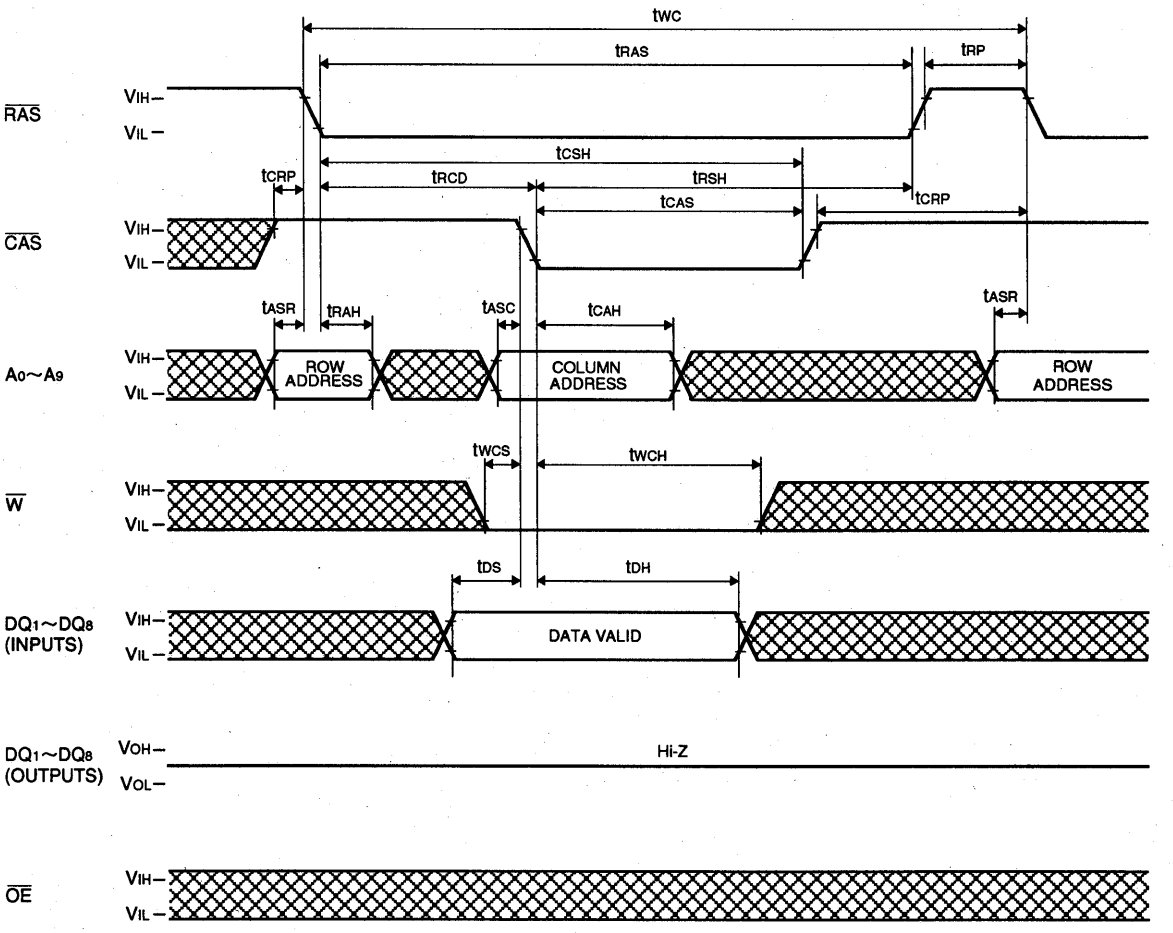
Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

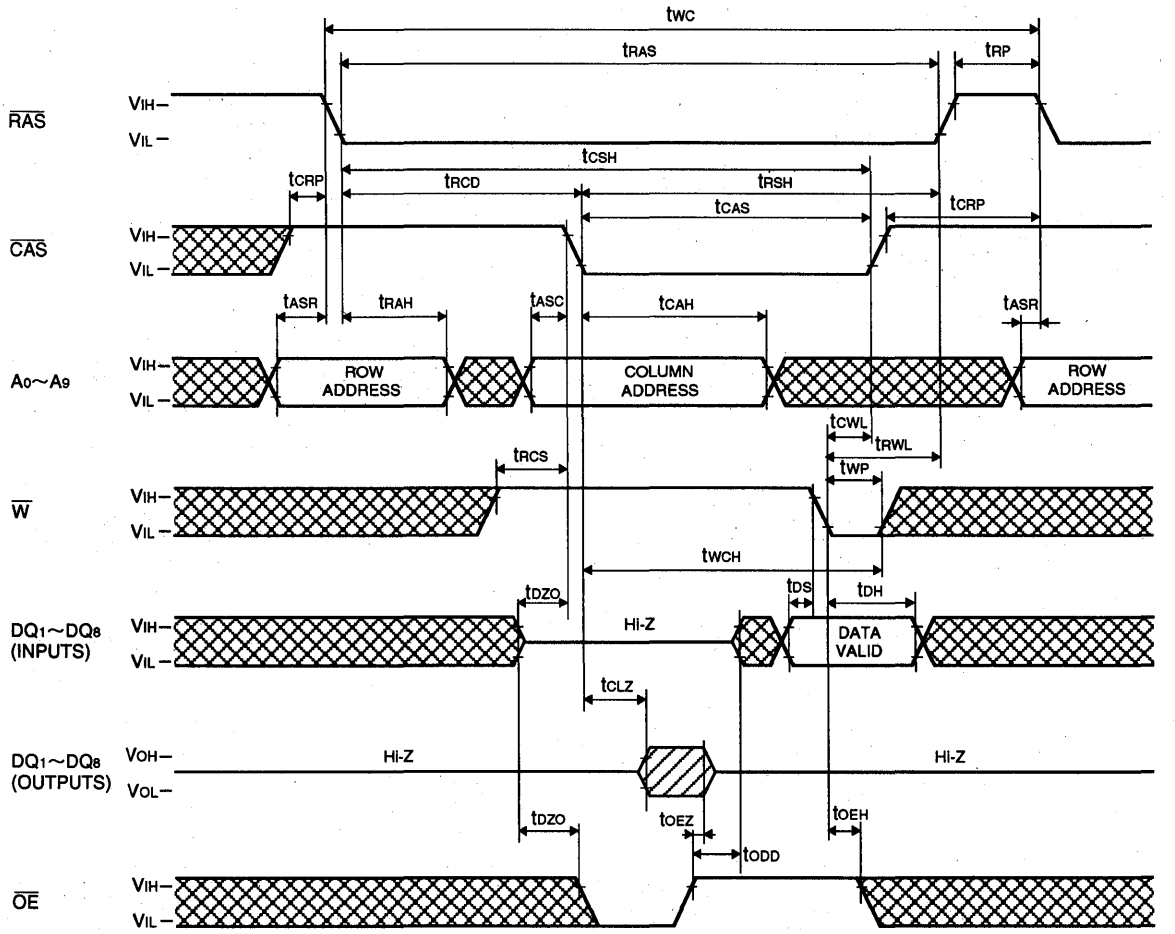
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

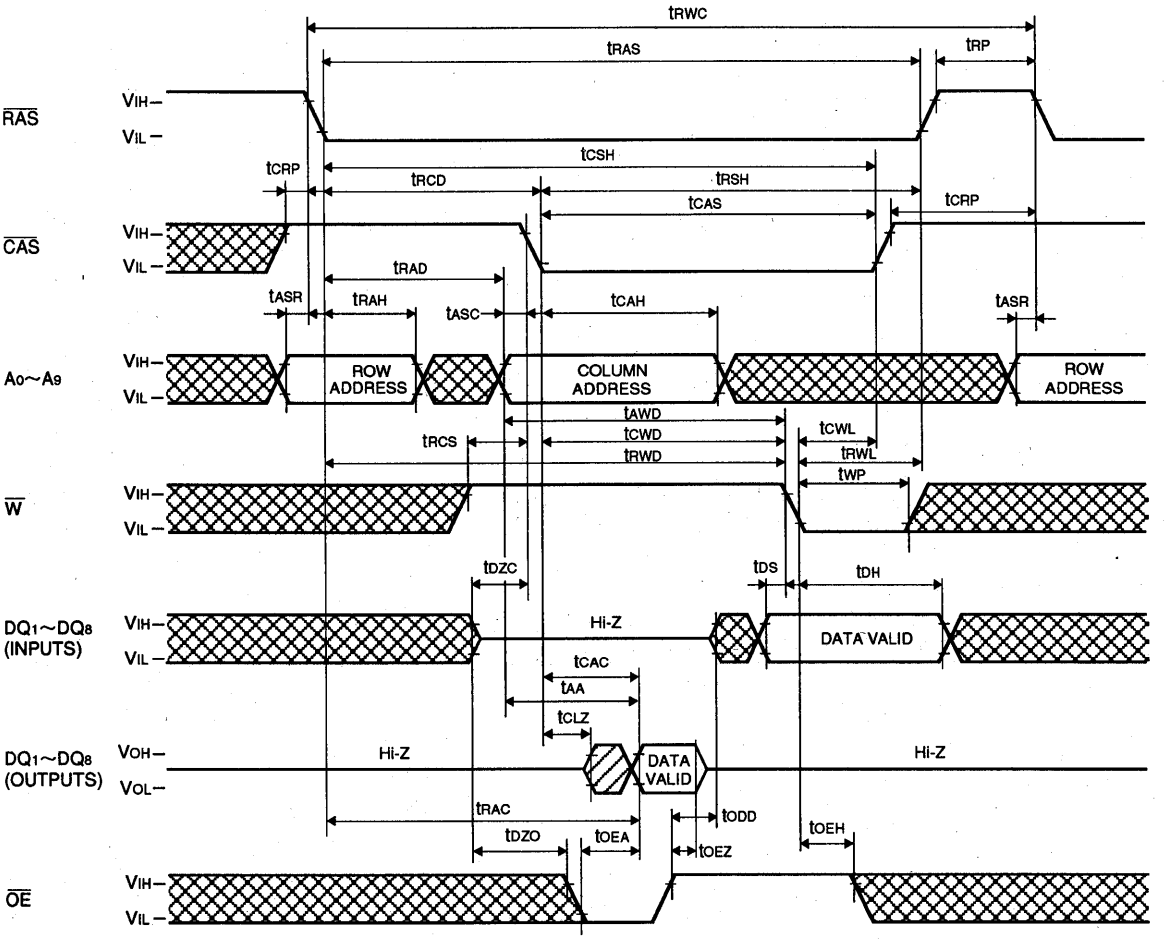
Write Cycle (Early write)



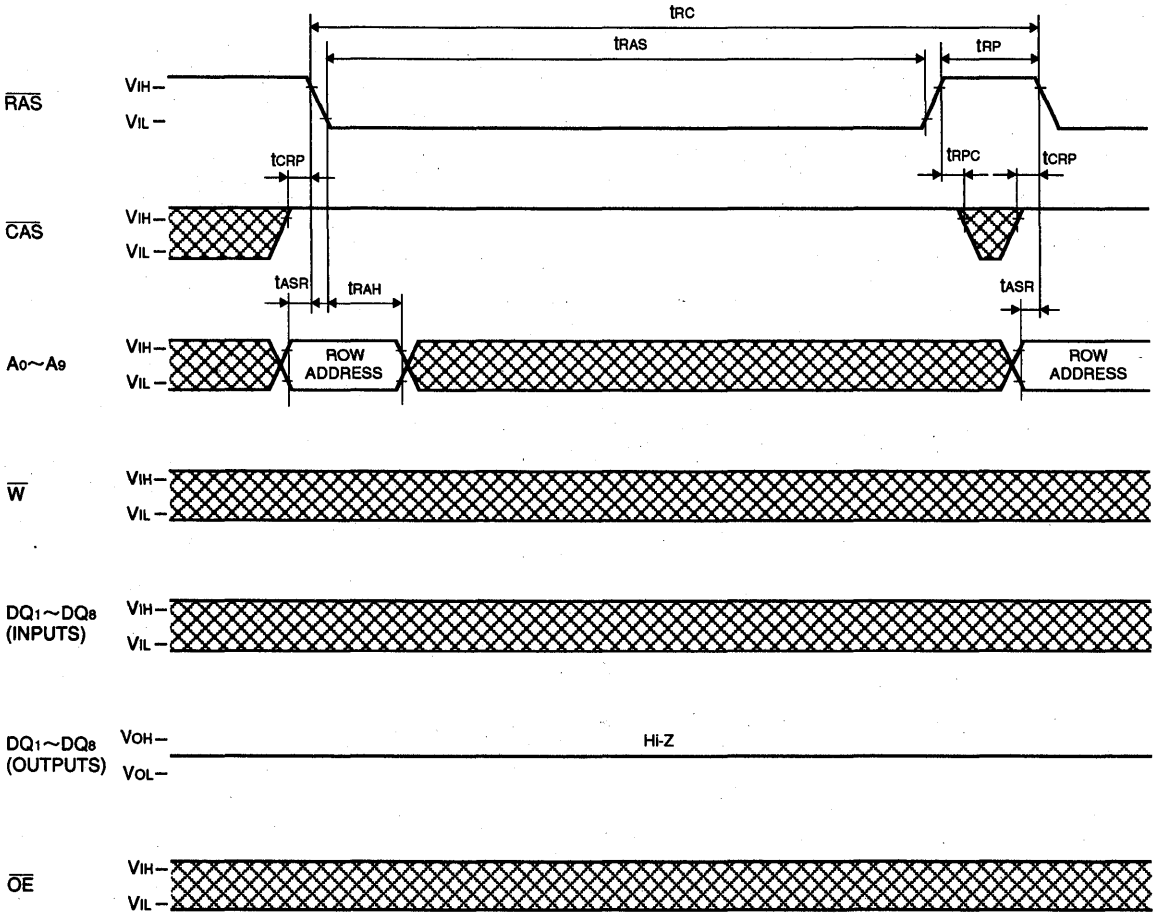
Write Cycle (Delayed write)



Read-Write, Read-Modify-Write Cycle

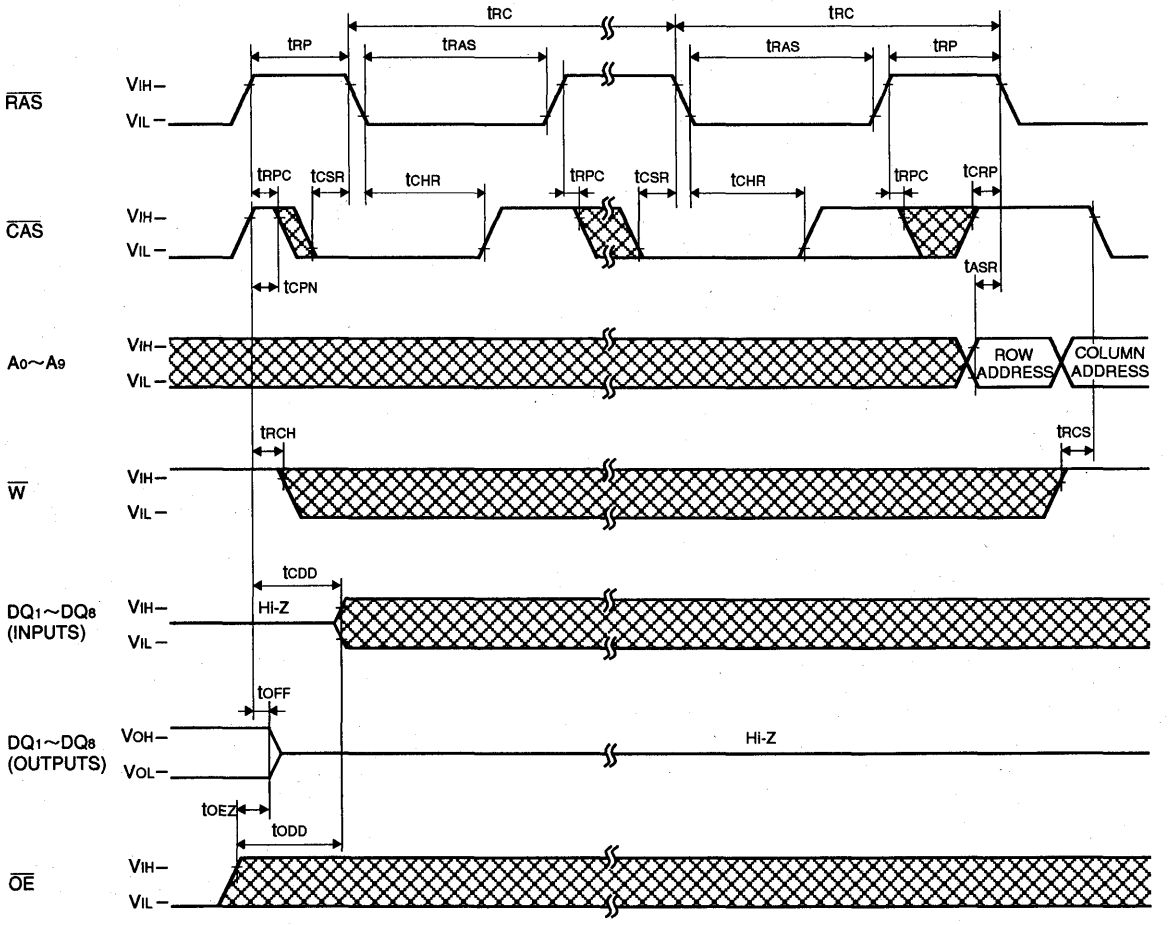


$\overline{RAS}$-only Refresh Cycle



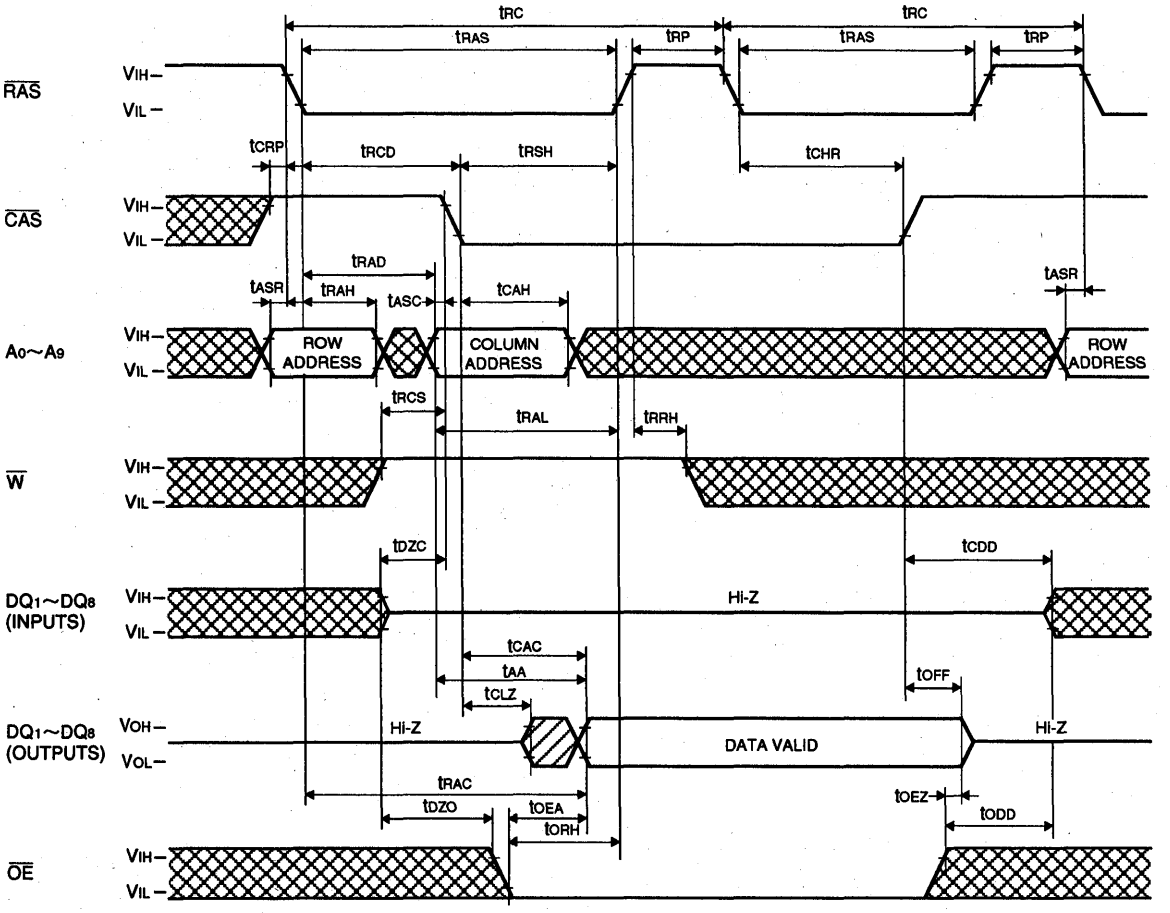
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

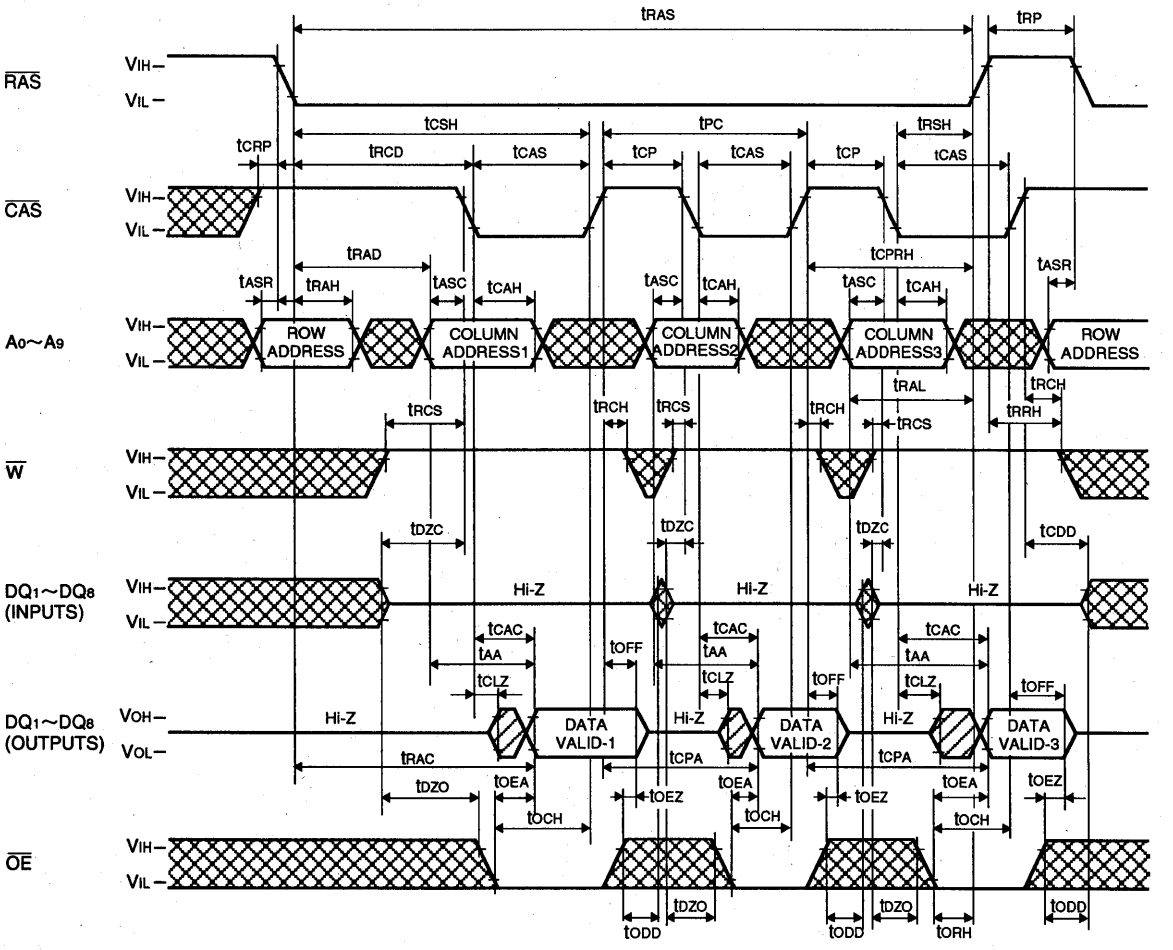
Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

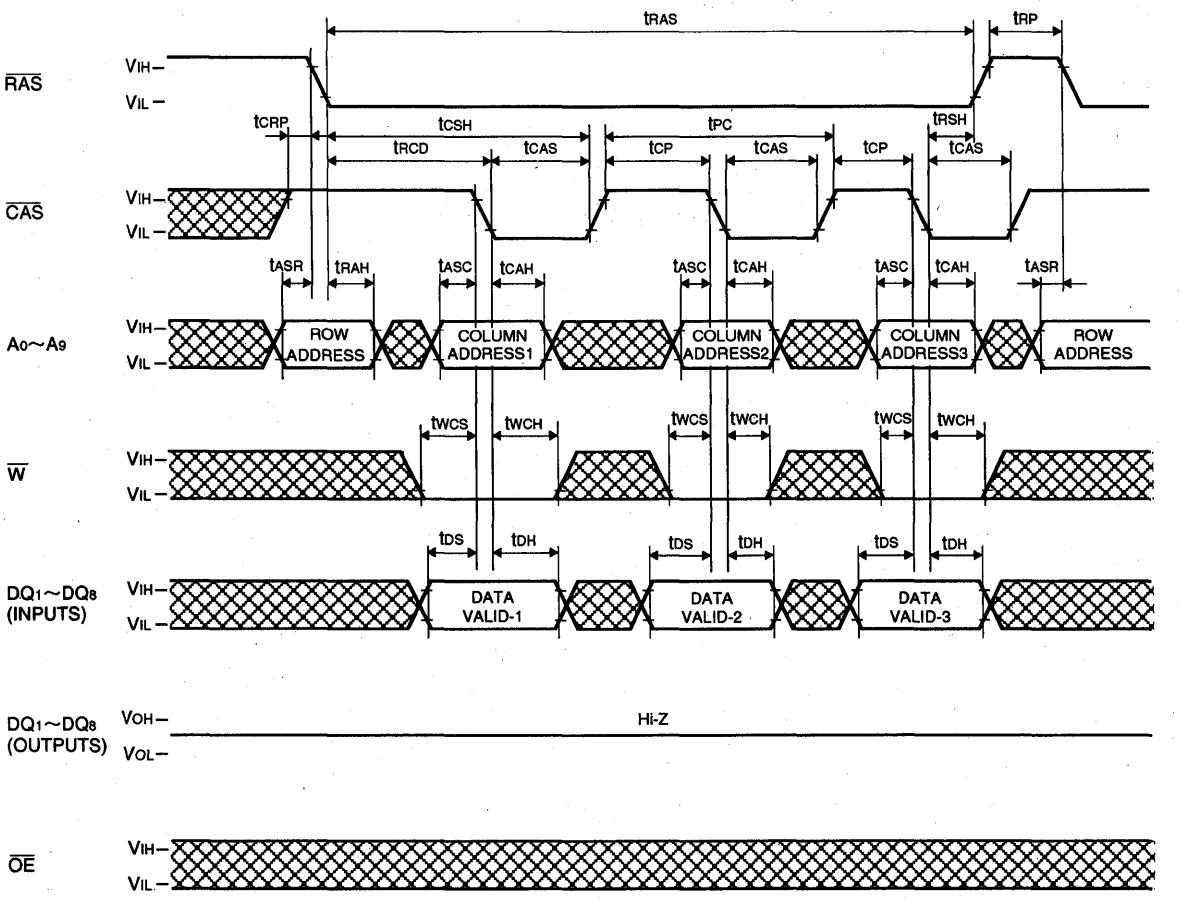
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

Fast Page Mode Read Cycle



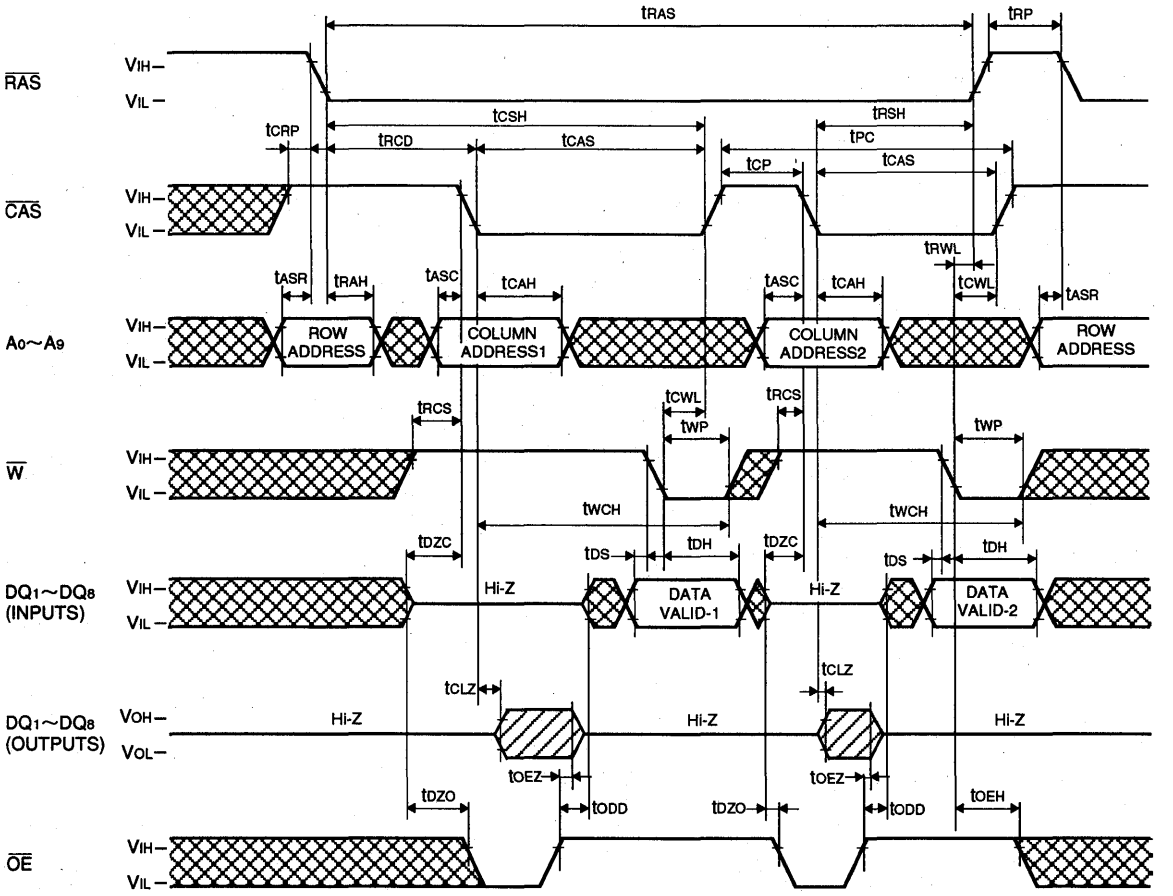
PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

Fast Page Mode Write Cycle (Early Write)



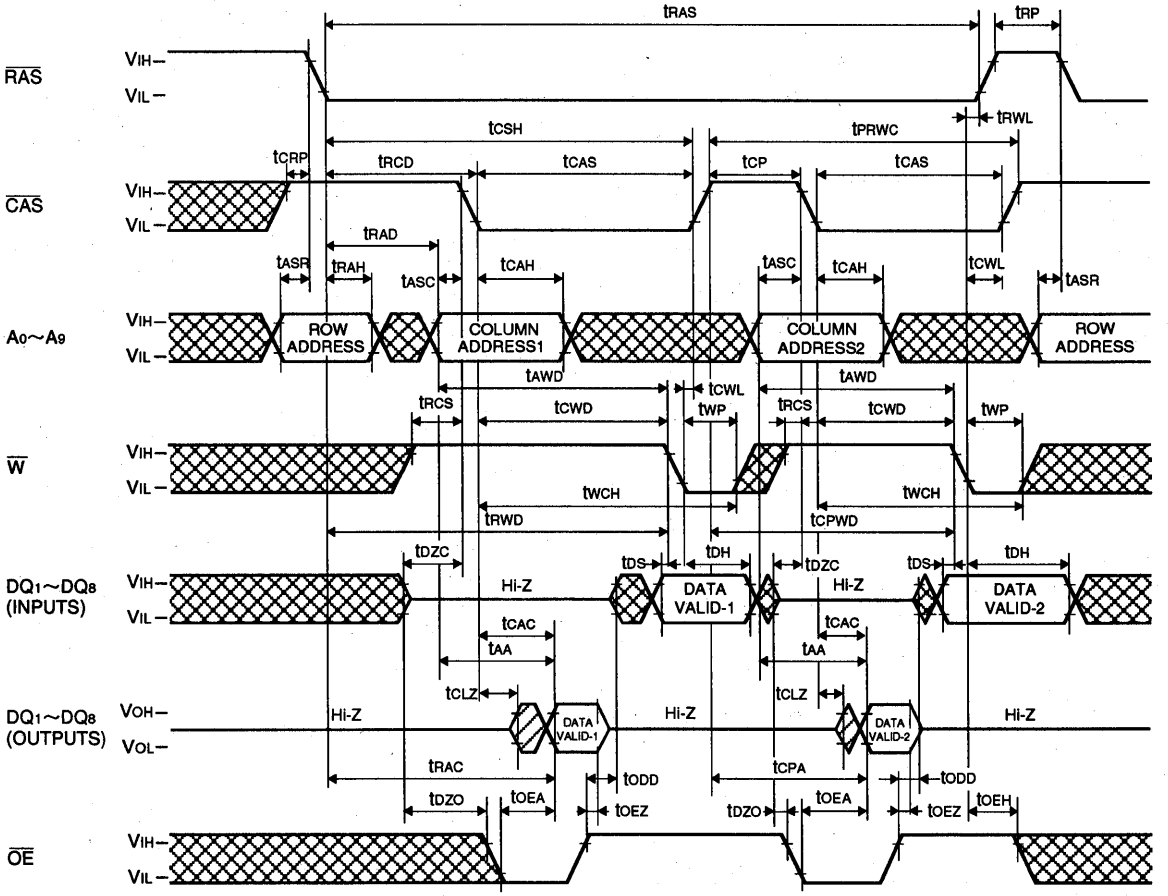
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast-Page Mode Write Cycle (Delayed Write)

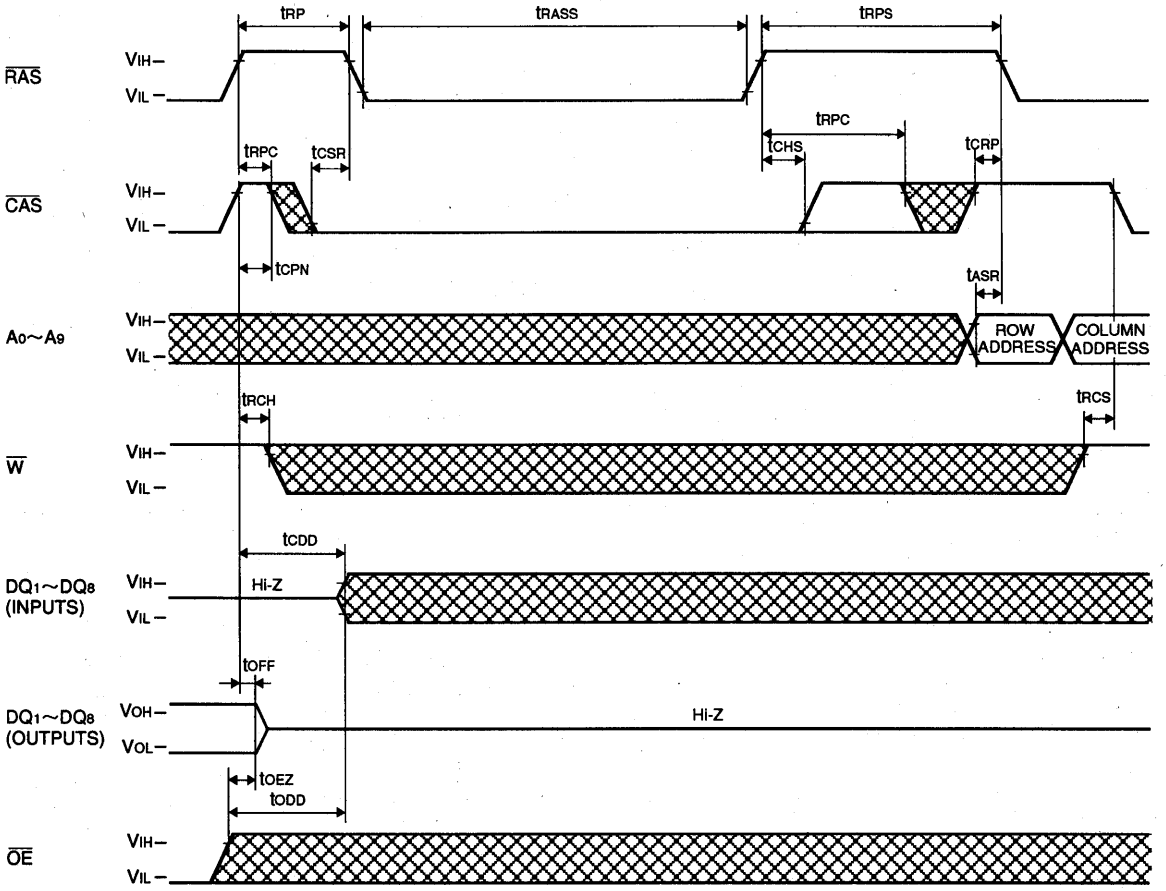


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 28)



Note 28:Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing diagram

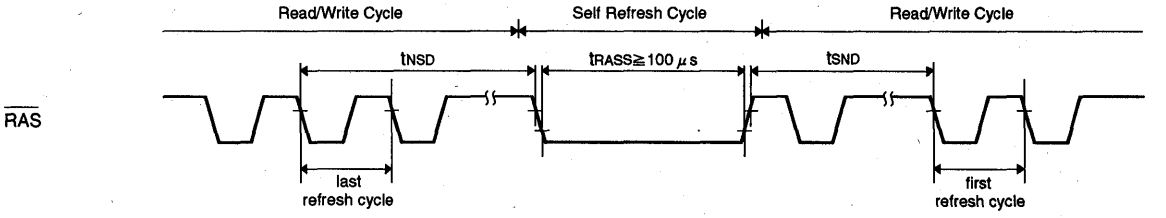
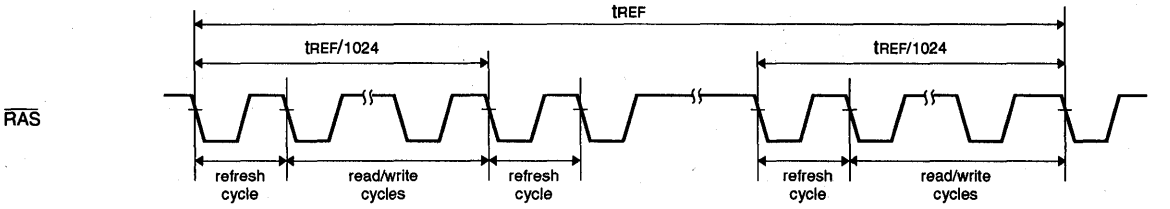


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	t_{NSD}≦125 μs	t_{SND}≦125 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≦16 μs	t_{SND}≦16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max.) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_9) are selected during 1024 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation

(A) Timing diagram

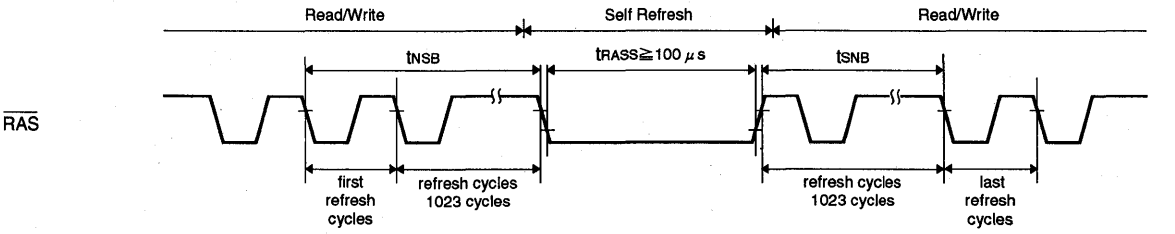
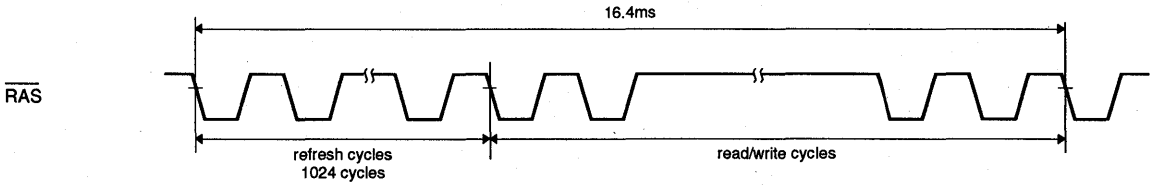


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	tNSB≦16.4ms	tSNB≦16.4ms
$\overline{RAS}$ only burst refresh	tNSB+tSNB≦16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of nine row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read / write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

M5M4V4260TP-7,-8,-7S,-8S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essental. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit a reduction in pins and an increase in system density.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4260TP-7,-7S	70	20	35	20	130	300
M5M4V4260TP-8,-8S	80	20	40	20	150	260

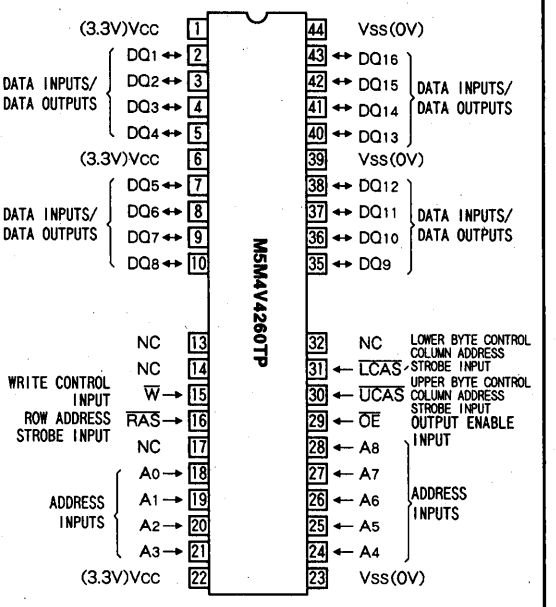
- Standard 44pin TSOP (II)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
  - CMOS input level ..... 2.52mW(max)
  - CMOS input level ..... 252μW(max) *
- Operating power dissipation
  - M5M4V4260TP-7, -7S ..... 396mW(max)
  - M5M4V4260TP-8, -8S ..... 342mW(max)
- Self refresh capability *
  - Self refresh current ..... 120μA(max)
- Extended refresh capability *
  - Extended refresh current ..... 120μA(max)
- Fast-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early write mode, $\overline{LCAS}$/$\overline{UCAS}$ and $\overline{OE}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 128ms (A_0~A_8) *
- Byte or Word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

* : Applicable to self refresh version (M5M4V4260TP-7S, -8S : option) only.

APPLICATION

Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-L(400mil TSOP Normal Bend)

NC : NO CONNECTION

FUNCTION

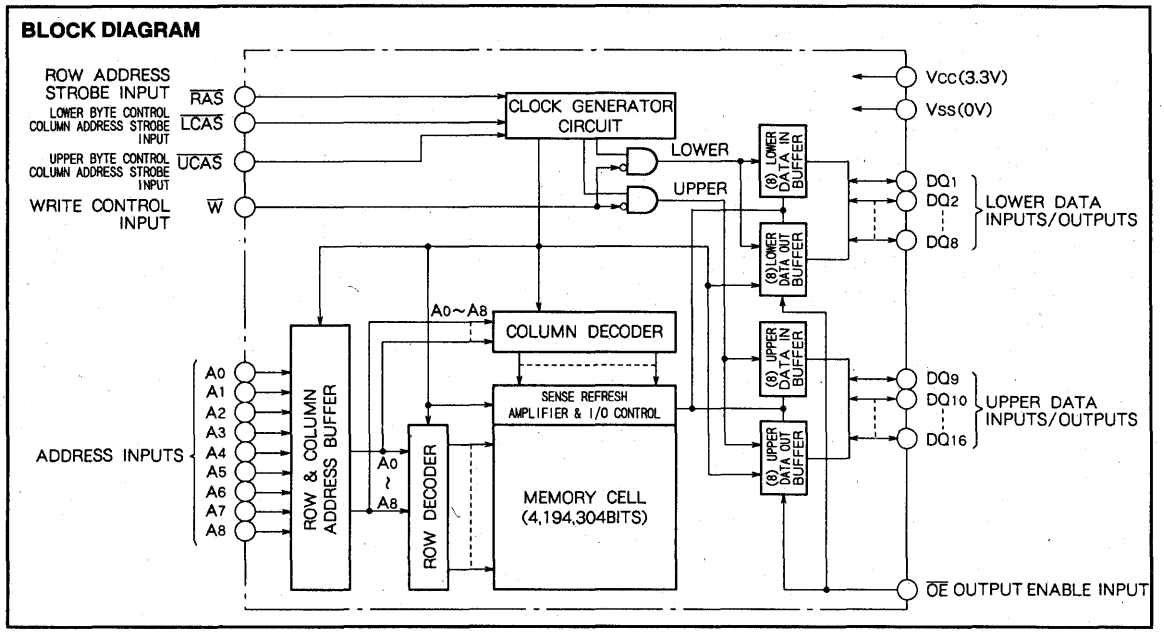
In addition to normal read, write, and read-modify-write operations the M5M4V4260TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$ only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ (Extended *) refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Self refresh *	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUN RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 1. All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦Vcc	−5		5	μA
I_I	Input current		0≦V_{IN}≦Vcc+0.3V, 0ther inputs pins=0V	−5		5	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3, 4, 5)	M5M4V4260-7,-7S	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = twc = min. output open			120	mA
		M5M4V4260-8,-8S				100	
$I_{CC2(AV)}$	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ Vcc − 0.2V output open			0.5	
						0.07*	
$I_{CC3(AV)}$	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V4260-7,-7S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			110	mA
		M5M4V4260-8,-8S				95	
$I_{CC4(AV)}$	Average supply current from Vcc, Fast-page-mode (Note 3, 4, 5)	M5M4V4260-7,-7S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			110	mA
		M5M4V4260-8,-8S				95	
$I_{CC6(AV)}$	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M4V4260-7,-7S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			110	mA
		M5M4V4260-8,-8S				95	
$I_{CC8(AV)}$*	Average supply current from Vcc, Extended refresh mode (Note 6)		Stand-by: $\overline{RAS}$≧Vcc−0.2V $\overline{CAS}$≧Vcc−0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc−0.2V $\overline{OE}$≦0.2V or ≧Vcc−0.2V A_0~A_9≦0.2V or ≧Vcc−0.2V DQ=open t_{RC}=125μs t_{RAS}=t_{RASmin}~1μs			120	μA
$I_{CC9(AV)}$*	Average supply current from Vcc, Self refresh mode (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output open			120	μA

Note 2 : Current flowing into a IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximun current is measured at the fastest cycle rate.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5 : Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}

CAPACITANCE (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = Vss f = 1MHz V_I = 25mVrms			6	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted. See notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V4260-7,-7S		M5M4V4260-8,-8S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		70		80	ns
t_{AA}	Column address access time	(Note 7, 10)		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	20	0	20	ns

Note 6 : An initial pause of 500 μs is required after power-up followed by a minimun of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh.)
Note that $\overline{RAS}$ may be cycled during the initial pause. Any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods(greater than 8.2ms)of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 100pF, V_{OH} = 2.4V(I_{OH} = − 2mA) and V_{OL} = 0.4V(I_{OL} = 2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V (V_{OL}).

8 : Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9 : Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If either t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table. t_{RAC} will increase by the amount which t_{RCD} or t_{RAD} exceeds the value shown.

10 : Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11 : Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12 : $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 5\mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted. See notes 6,13,14)

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{REF}	Refresh cycle time		8.2		8.2	ms
t_{REF}	Refresh cycle time *		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 16)	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 17)	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note 18)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note 18)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note 19)	20		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note 19)	20		20		ns
t_T	Transition time (Note 20)	1	50	1	50	ns

Note 13 : The timing requirements are assumed t_T = 5ns.

14 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

15 : Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only ; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

16 : Operation within the $t_{RAD(max)}$ limit insures that t_{RAC} (max) can be met. $t_{RAD(max)}$ is specified as a reference point only ; if t_{RAD} is greater than specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{CAC} or t_{AA}.

17 : Operation within the $t_{ASC(max)}$ limit insures that t_{RAC} (max) can be met. $t_{ASC(max)}$ is specified as a reference point only ; if t_{ASC} is greater than the specified $t_{ASC(max)}$ limit and t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

18 : Either t_{DZC} or t_{DZO} must be satisfied.

19 : Either t_{CDD} or t_{ODD} must be satisfied.

20 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		20		ns

Note 21 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	20		20		ns
t_{WP}	Write pulse width	15		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 22)	175		195		ns
t_{RAS}	$\overline{RAS}$ low pulse width	115	10000	125	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	65	10000	65	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	115		125		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	65		65		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time. $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	40		40		ns
t_{RWD}	Delay time. $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	90		100		ns
t_{AWD}	Delay time. address to $\overline{W}$ low (Note 23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	20		20		ns
t_{WP}	Write pulse width	15		15		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	20		20		ns

Note 22 : t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

23 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	95		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	115	100000	135	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	10	15	10	20	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	40		45		ns

Note 24 : All previously specified timing requirements and switching characterisitics are applicable to their respective fast page mode cycle.

25 : $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26 : $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	30		30		ns

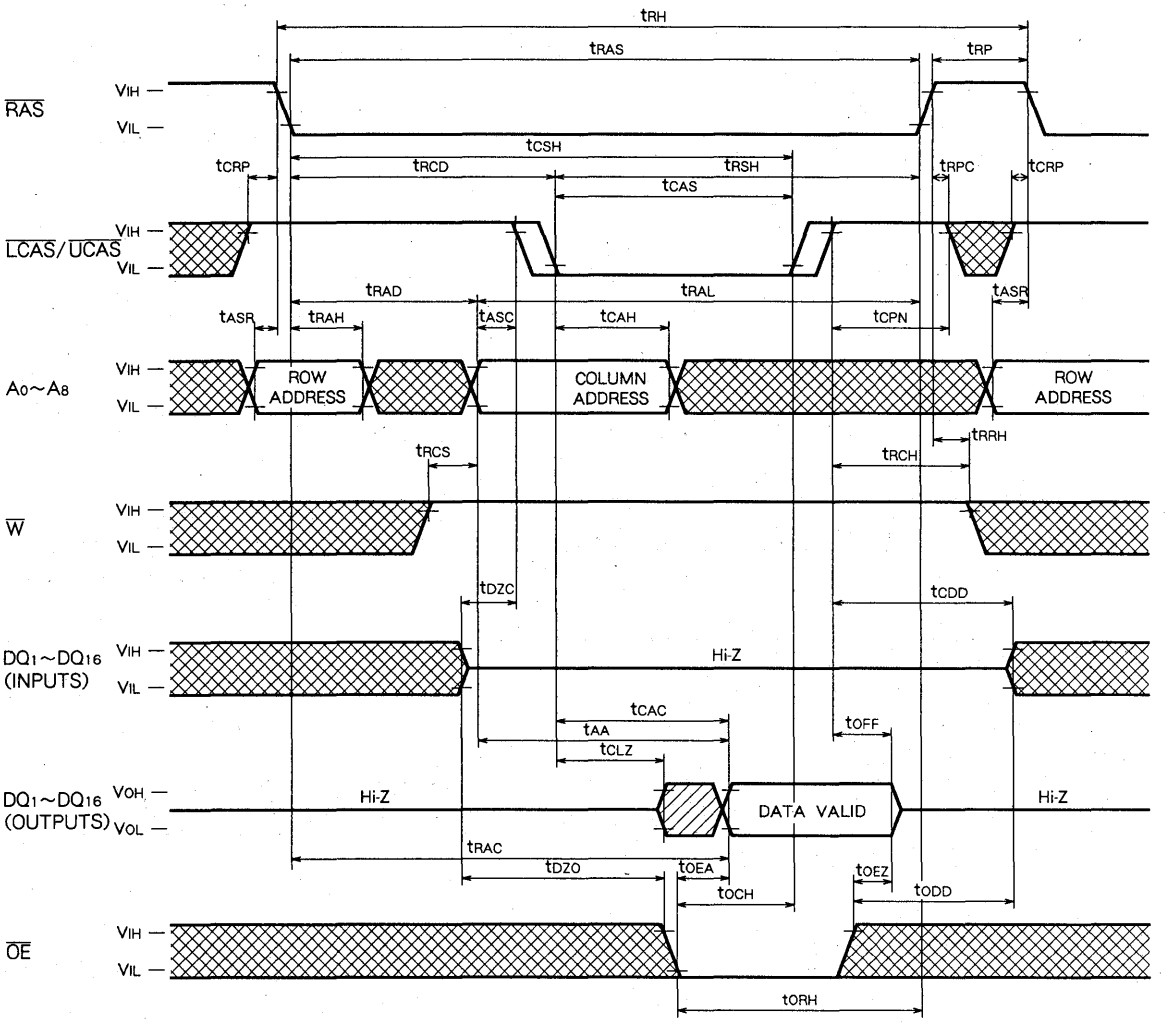
Note 27 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle *

Symbol	Parameter	Limits				Unit
		M5M4V4260-7,-7S		M5M4V4260-8,-8S		
		Min	Max	Min	Max	
t_{RASS}	$\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	$\overline{RAS}$ high pulse width	130		150		ns
t_{CHS}	$\overline{CAS}$ hold time after $\overline{RAS}$ high	−50		−50		ns

Timing Diagrams (Note 28)

Read Cycle

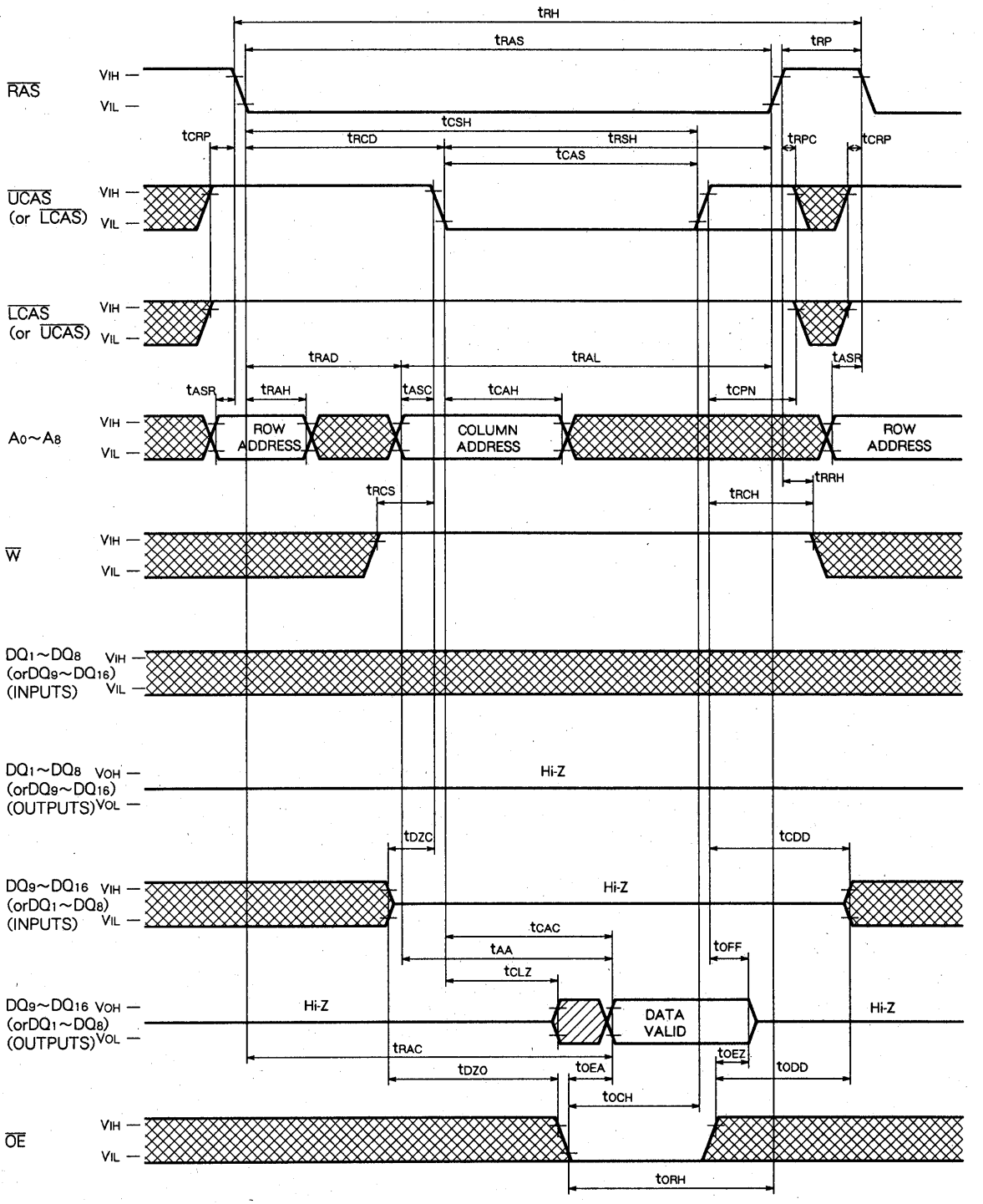


Note 28

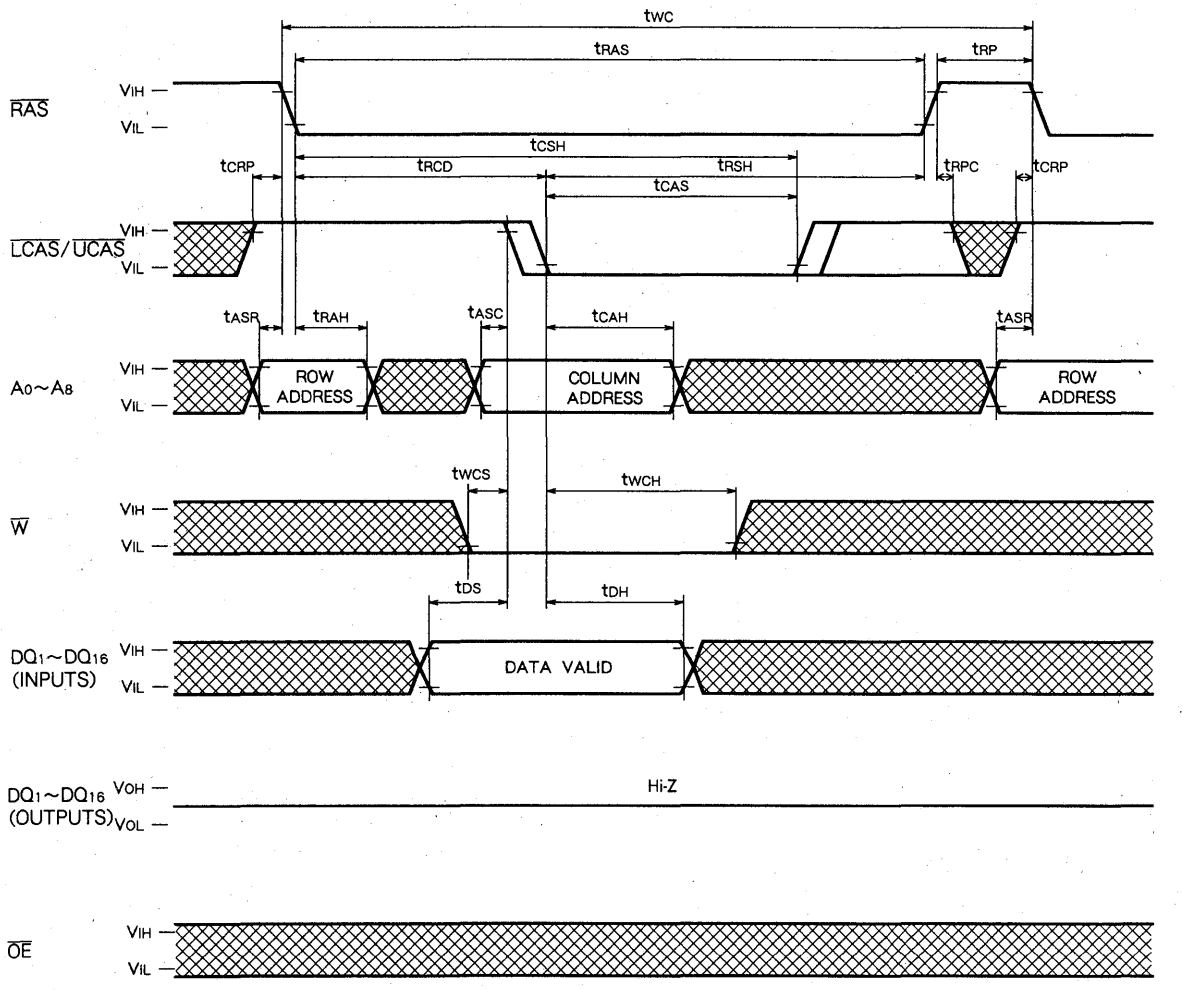
Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output.

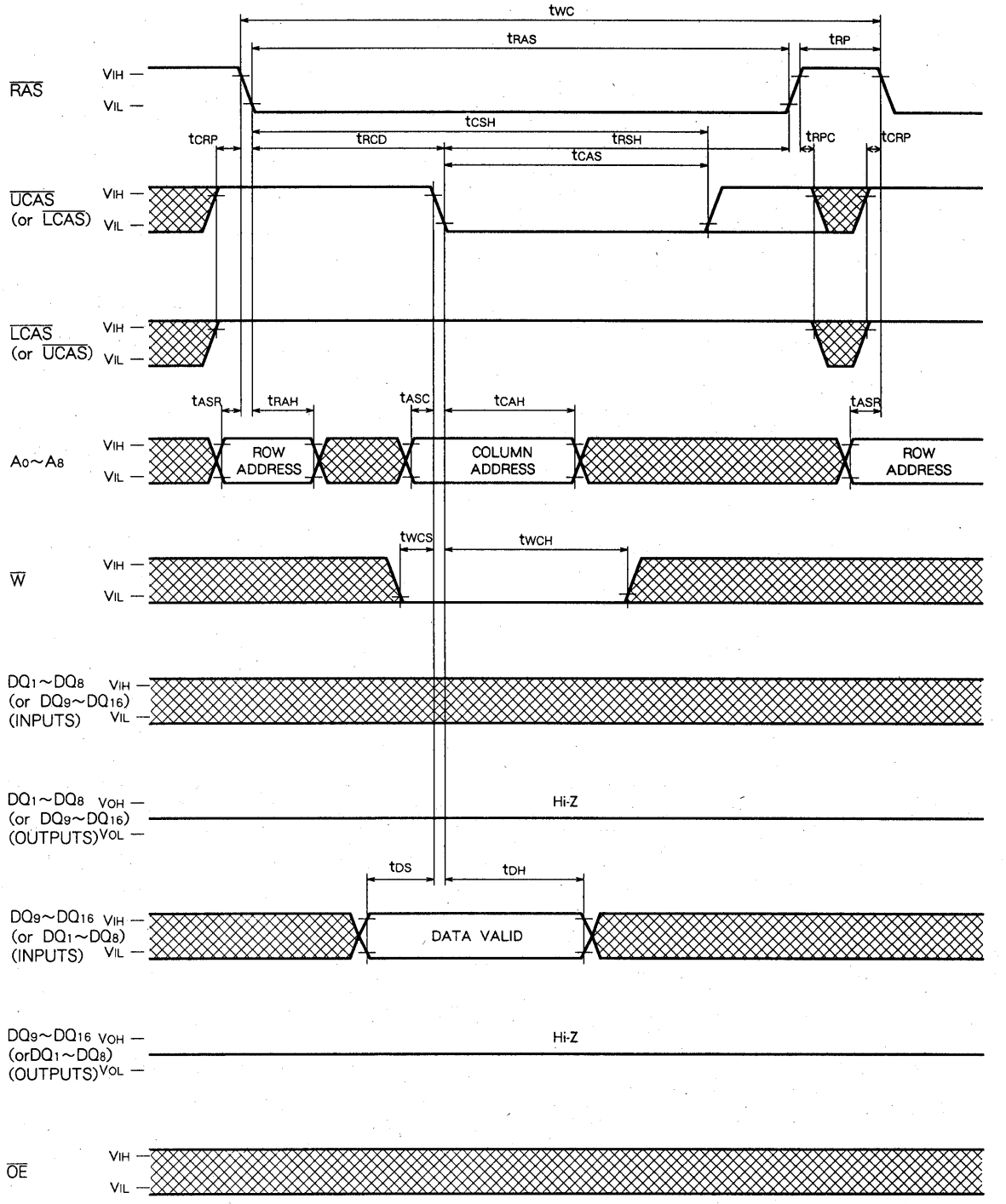
Byte Read Cycle



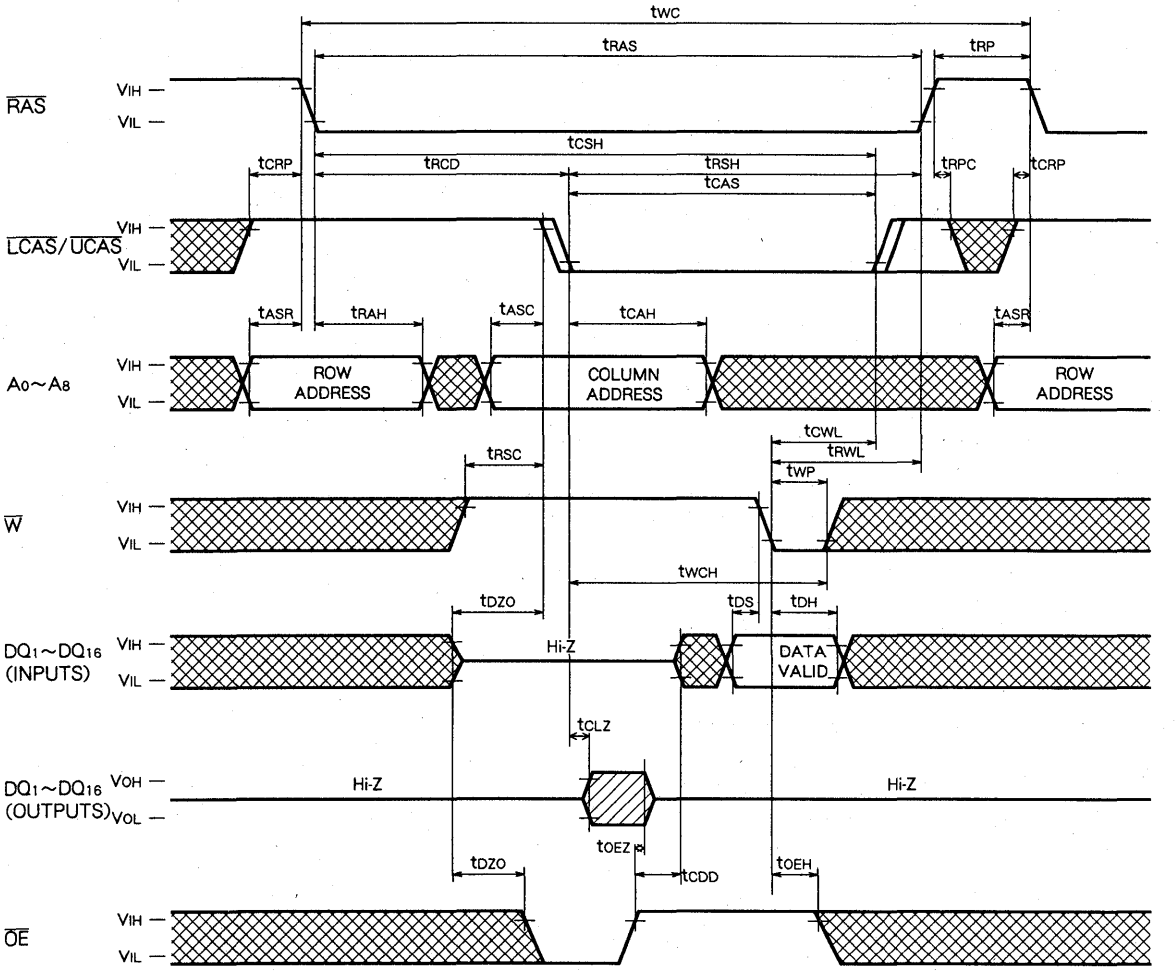
Write Cycle (Early Write)



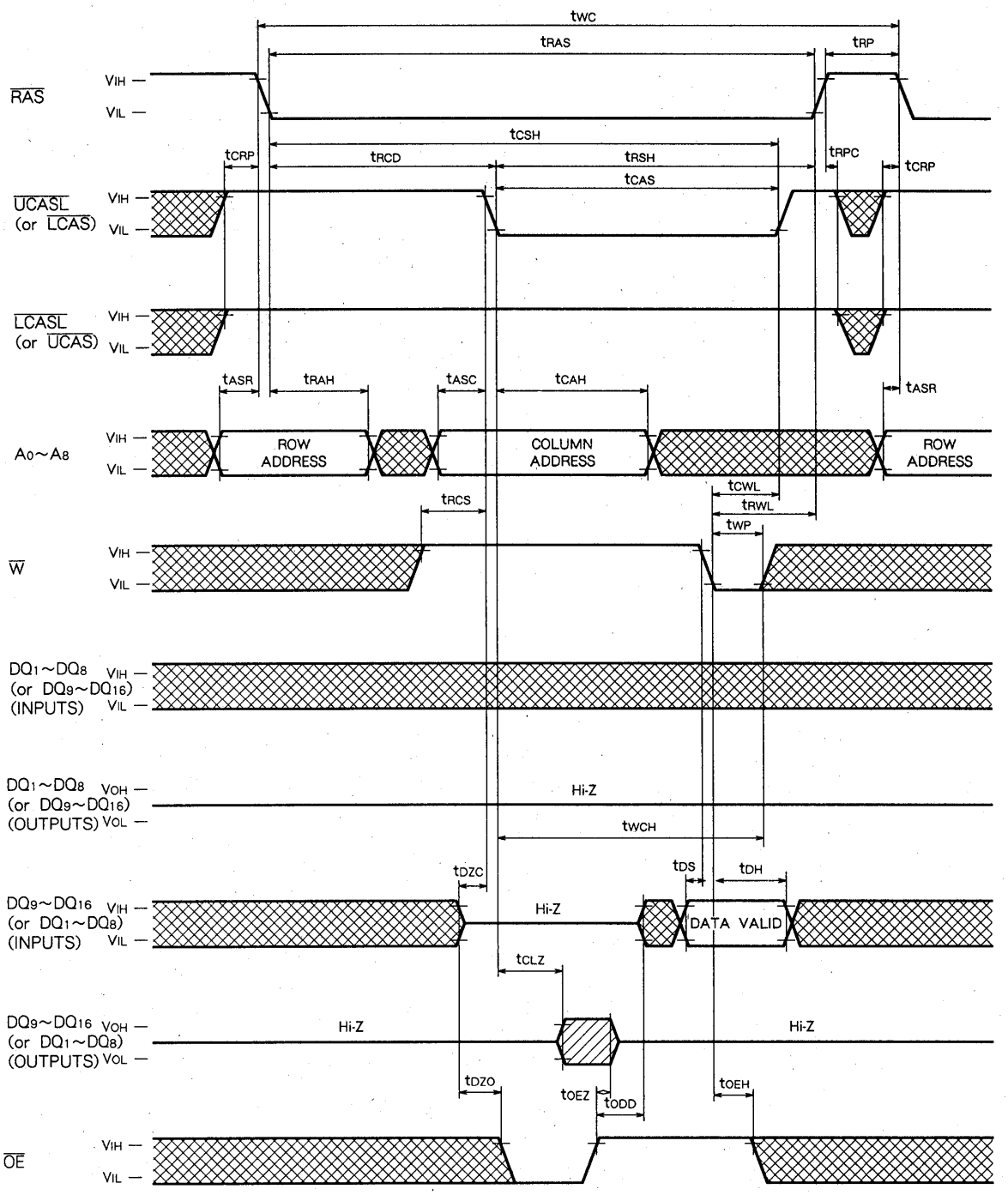
Byte Write Cycle (Early Write)



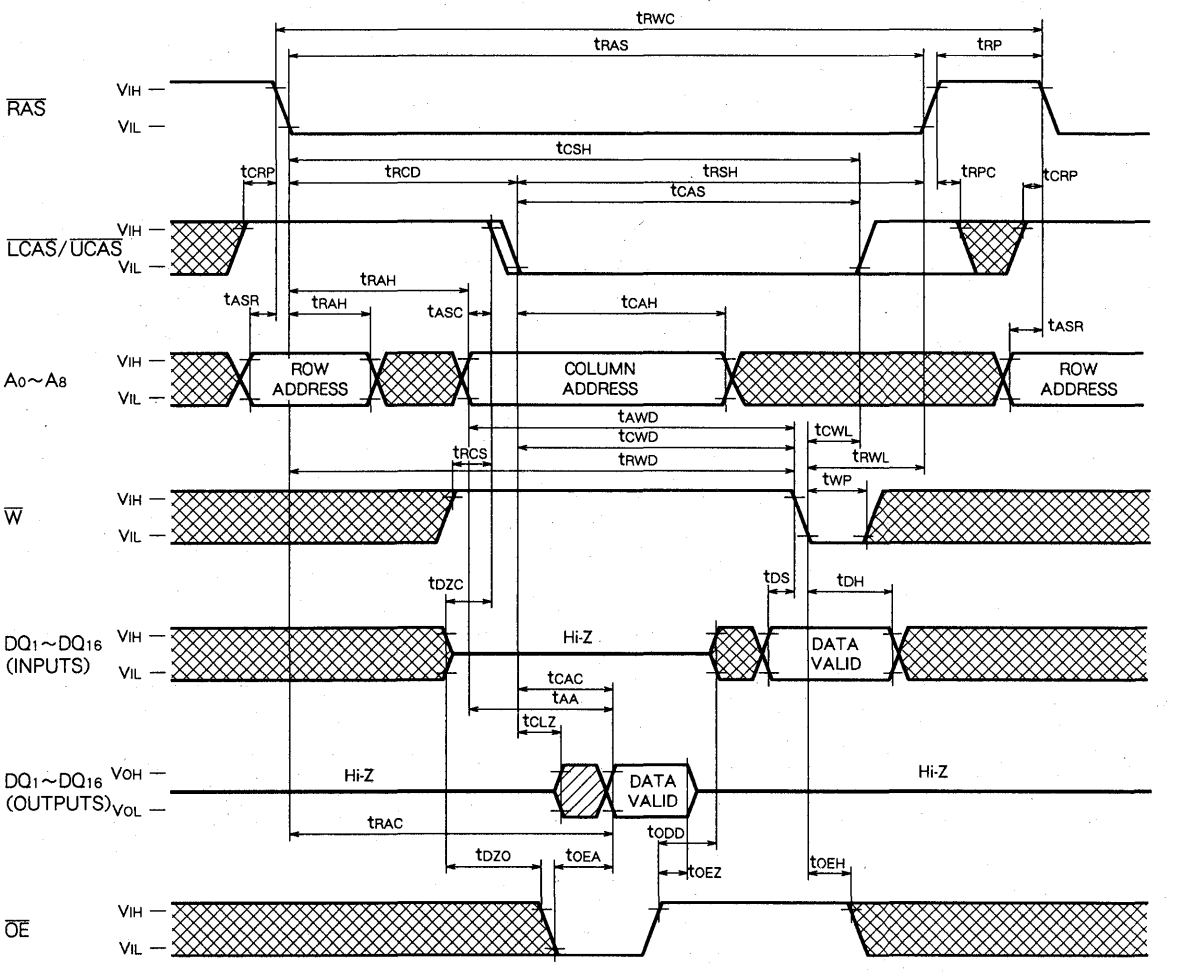
Write Cycle (Delayed Write)



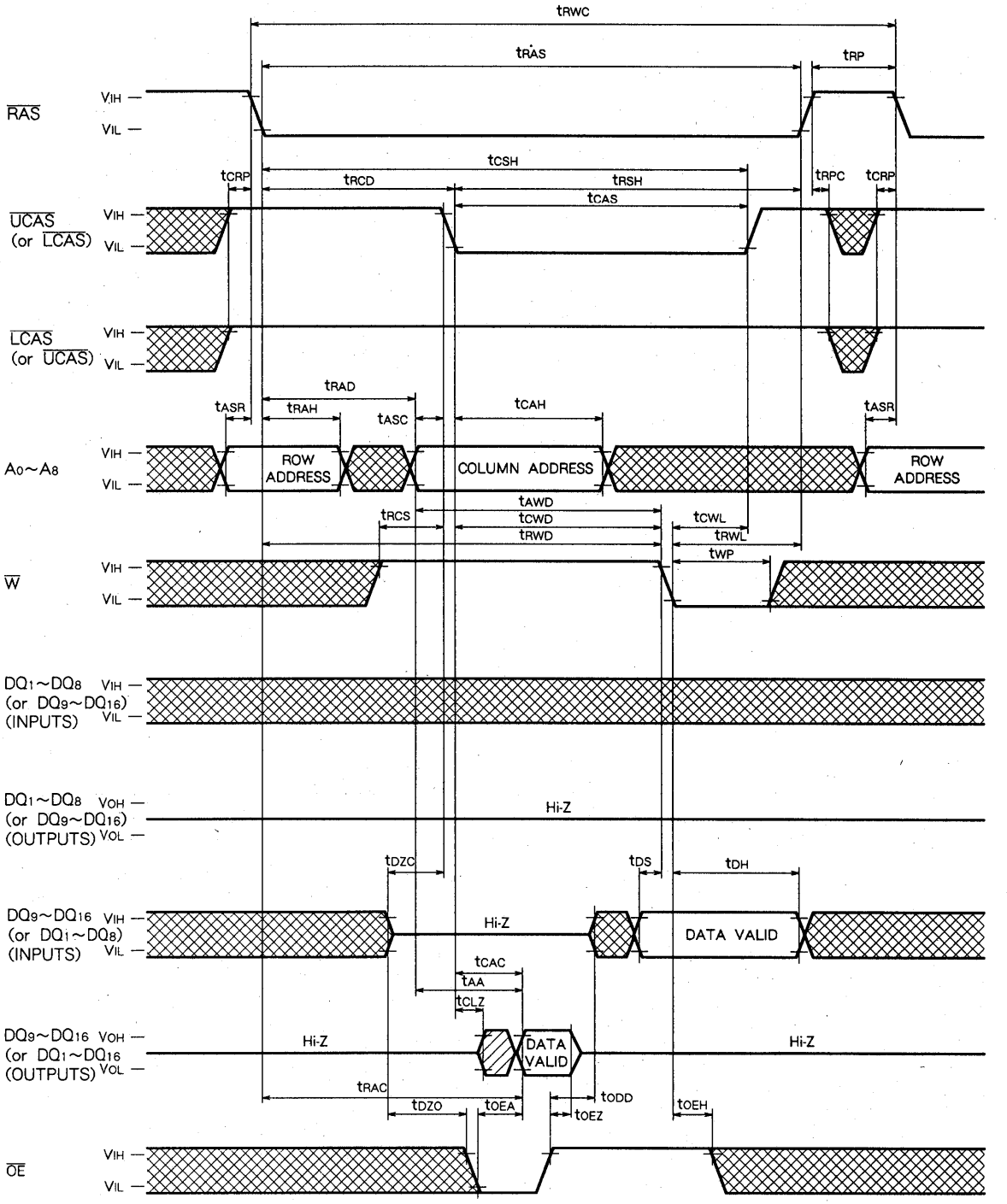
Byte Write Cycle (Delayed Write)



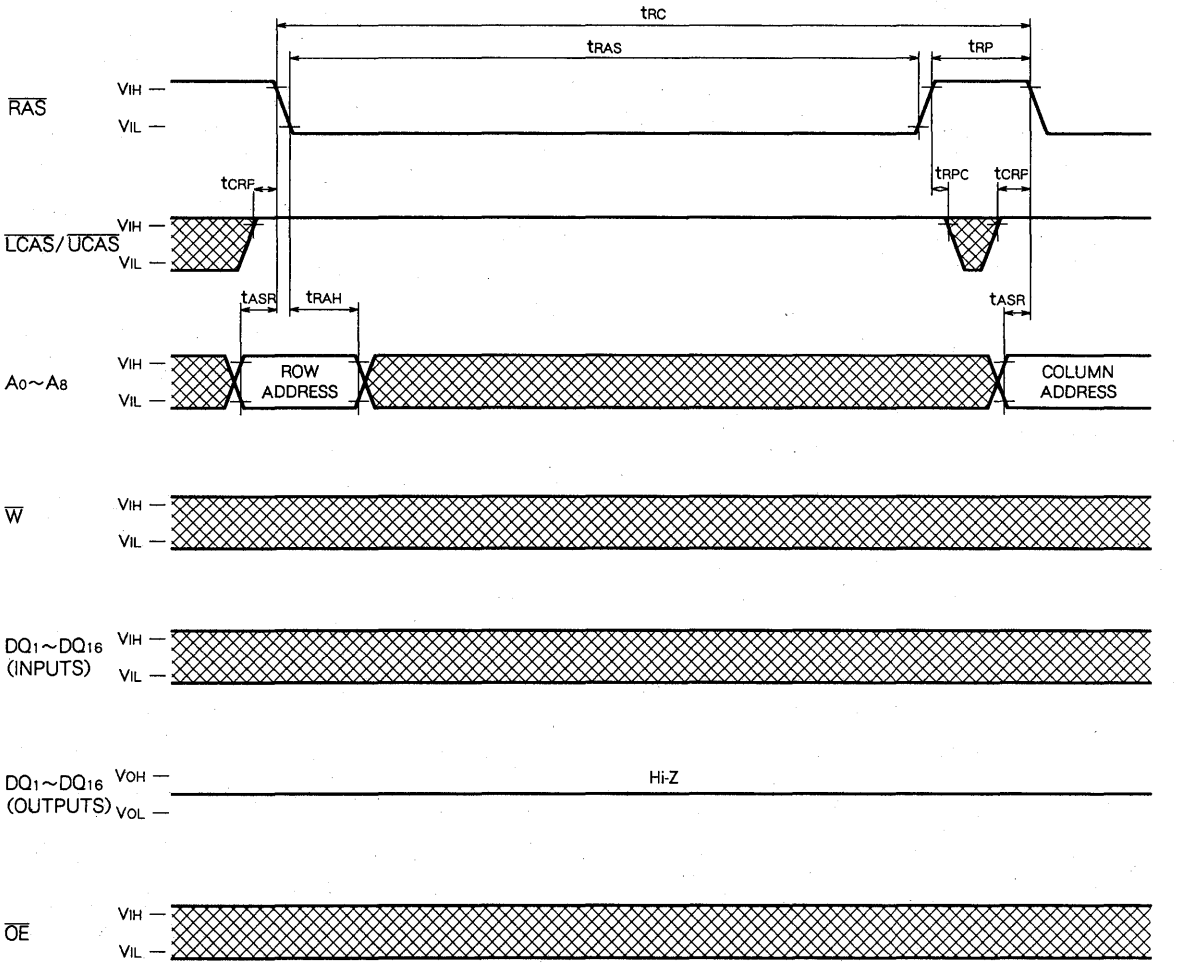
Read-Write, Read-Modify-Write Cycle



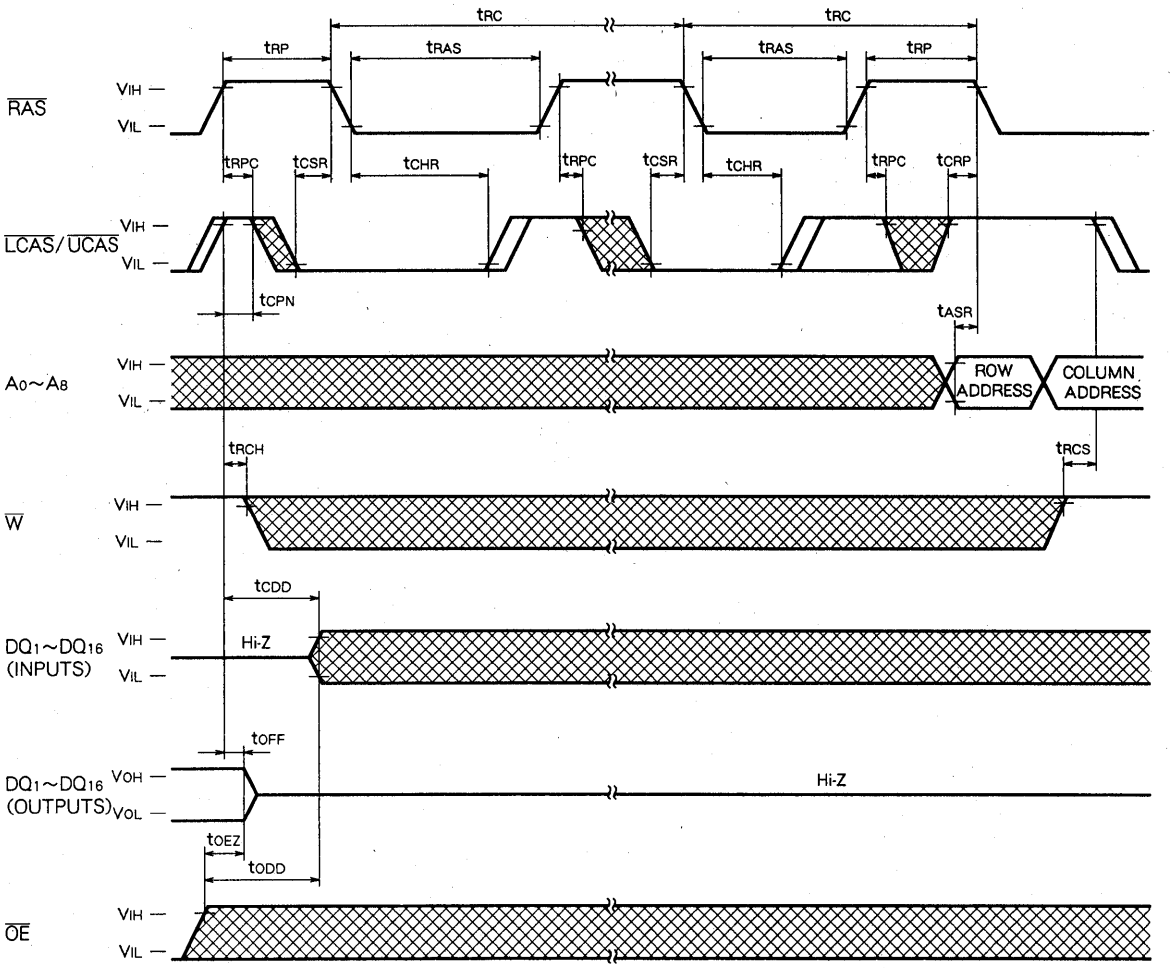
Byte Read-Write, Read-Modify-Write Cycle



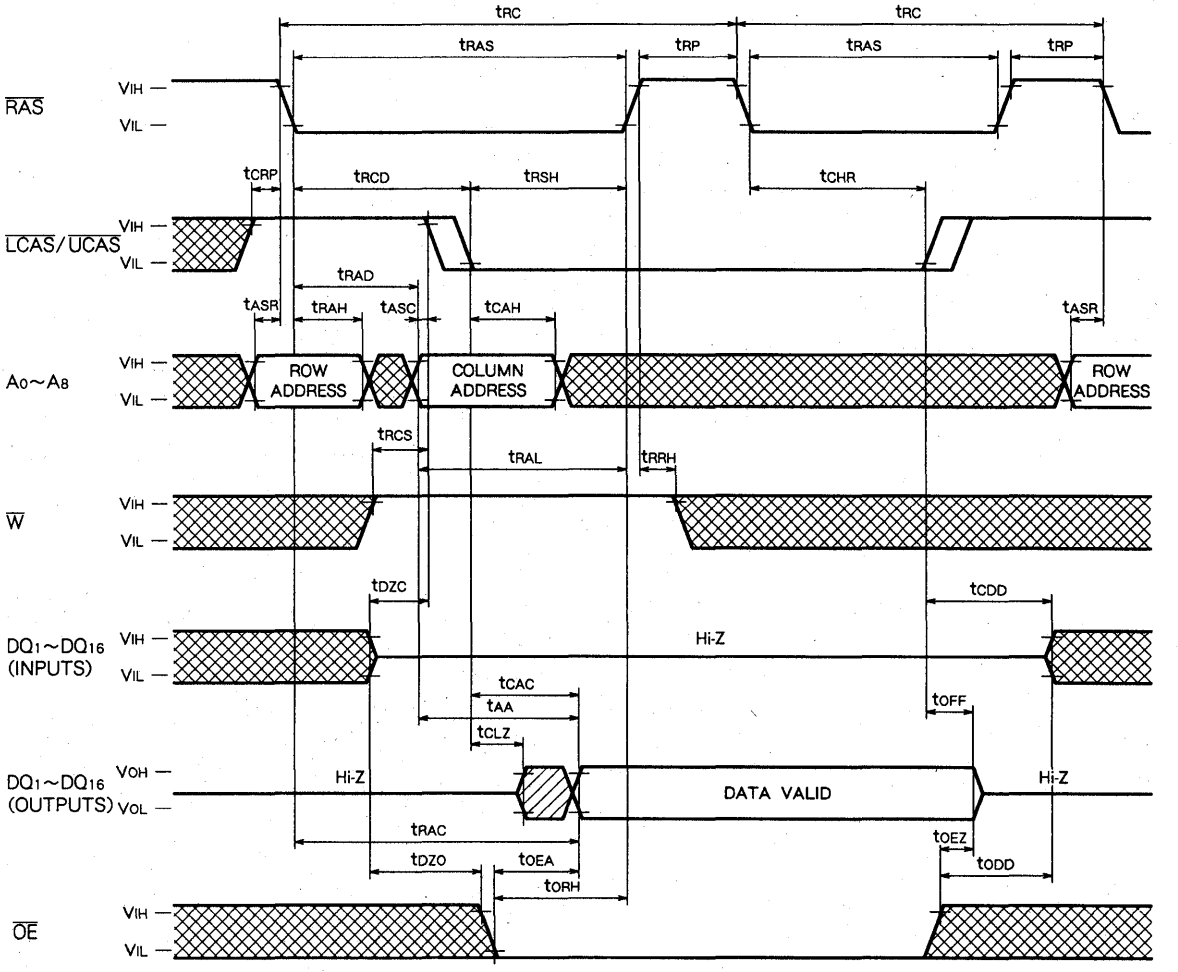
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

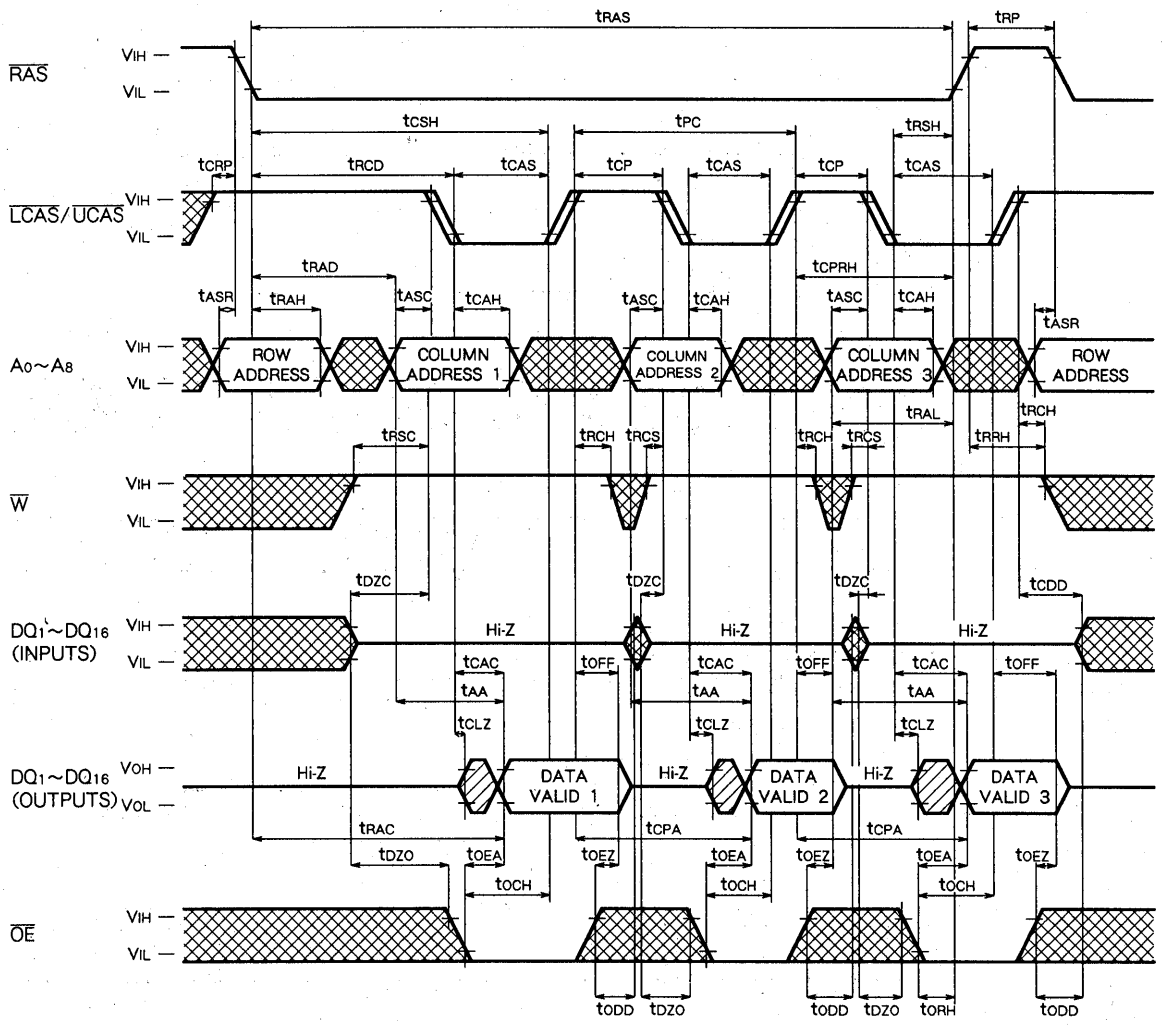


Hidden Refresh Cycle (Read) (Note 29)

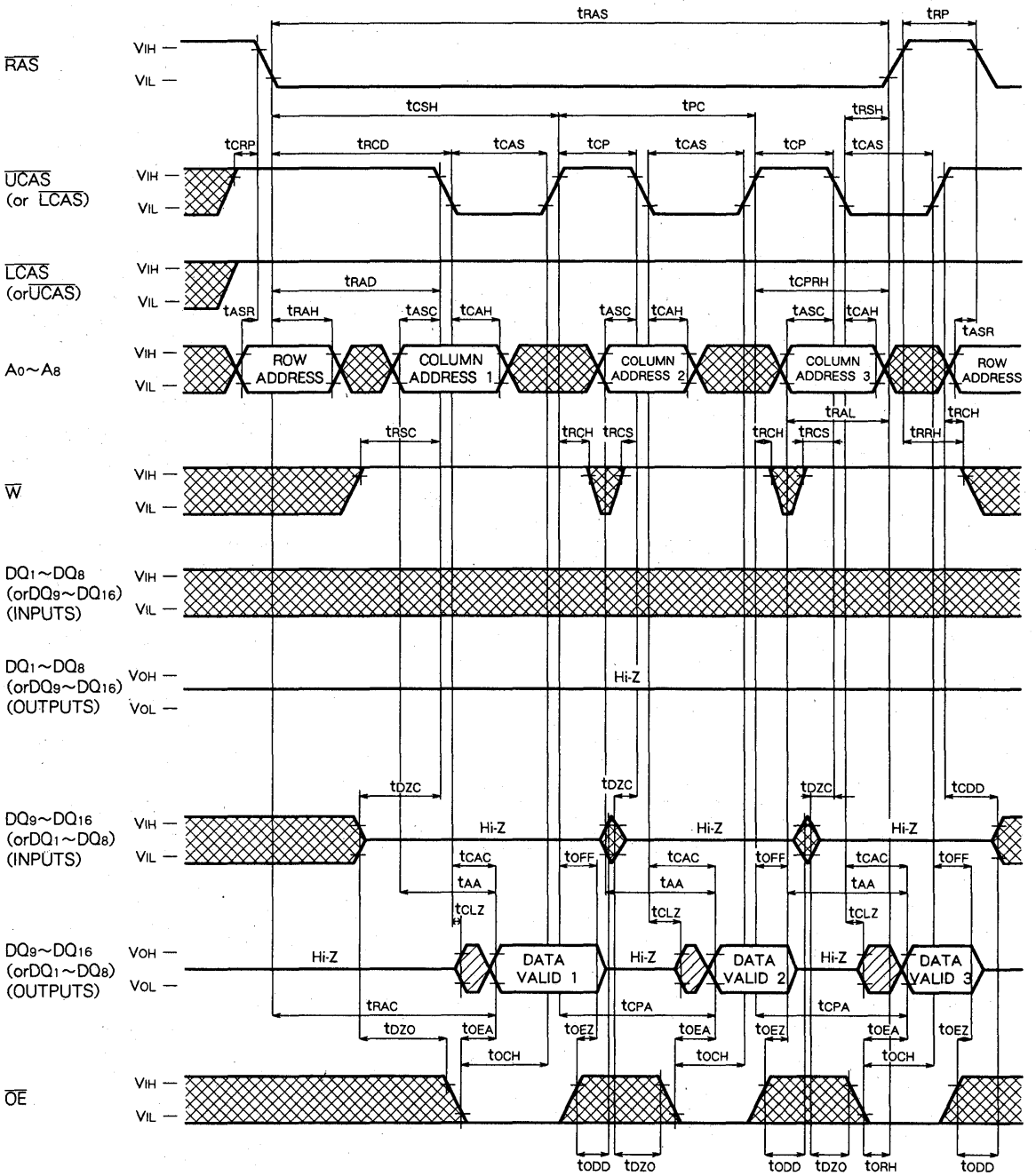


Note 29 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

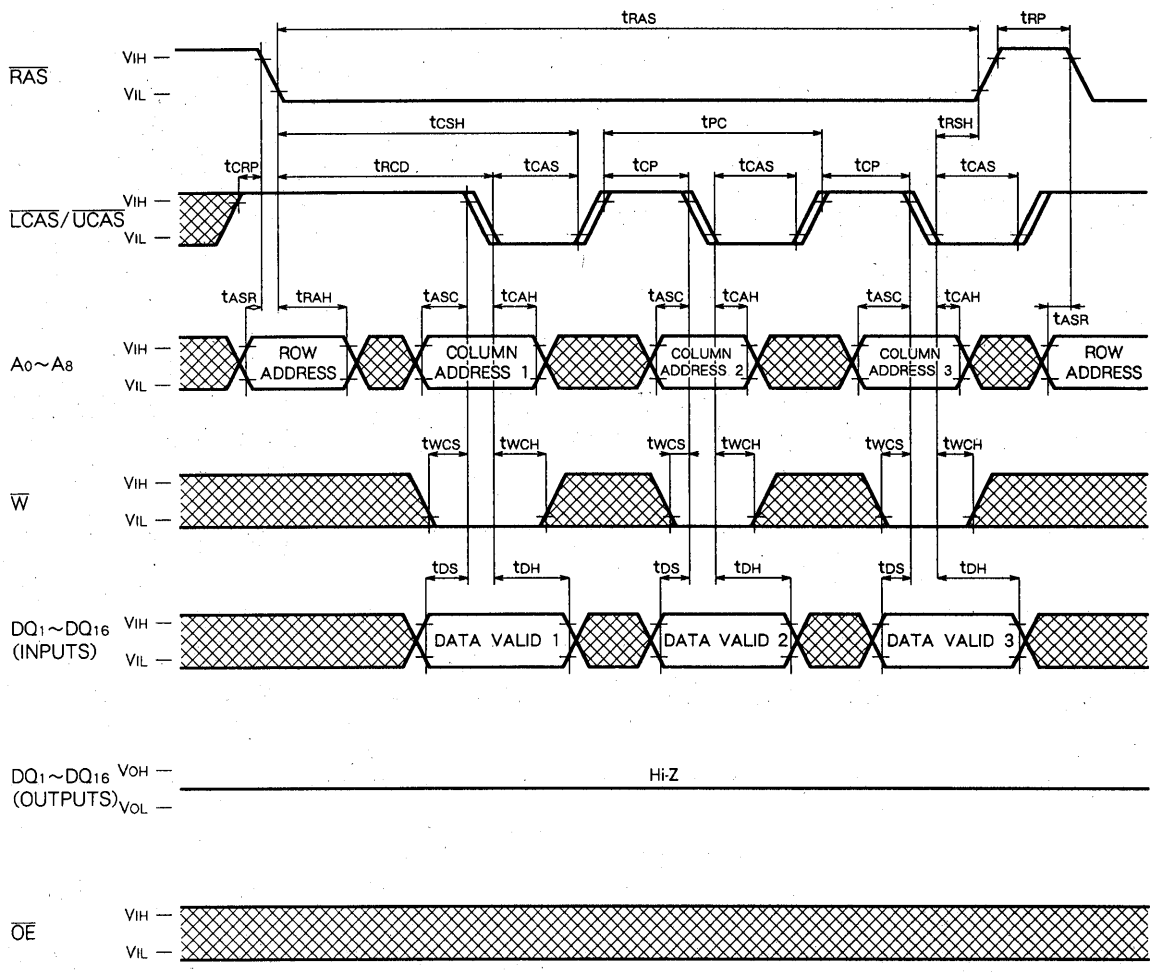
Fast Page Mode Read Cycle



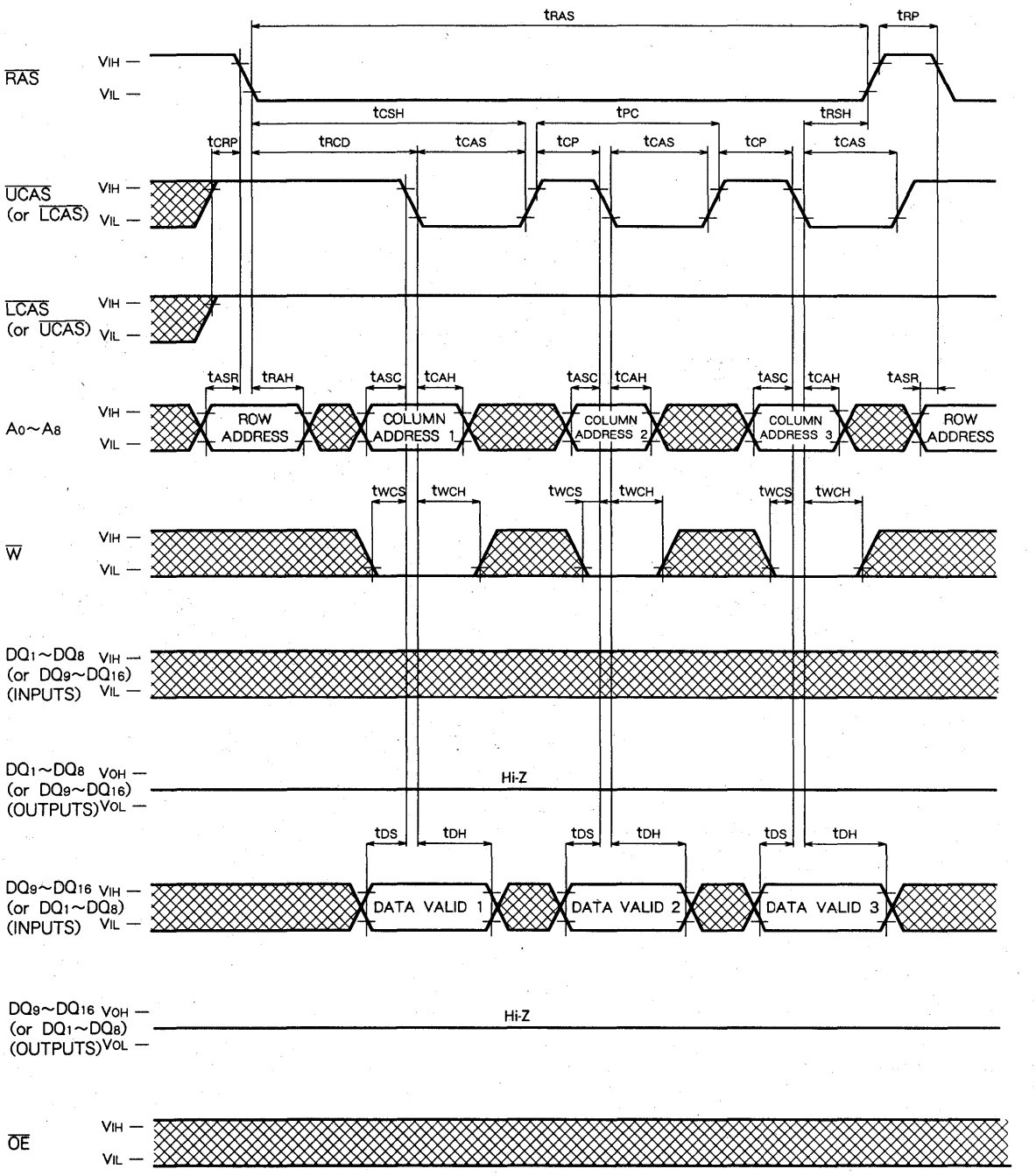
Fast Page Mode Byte Read Cycle



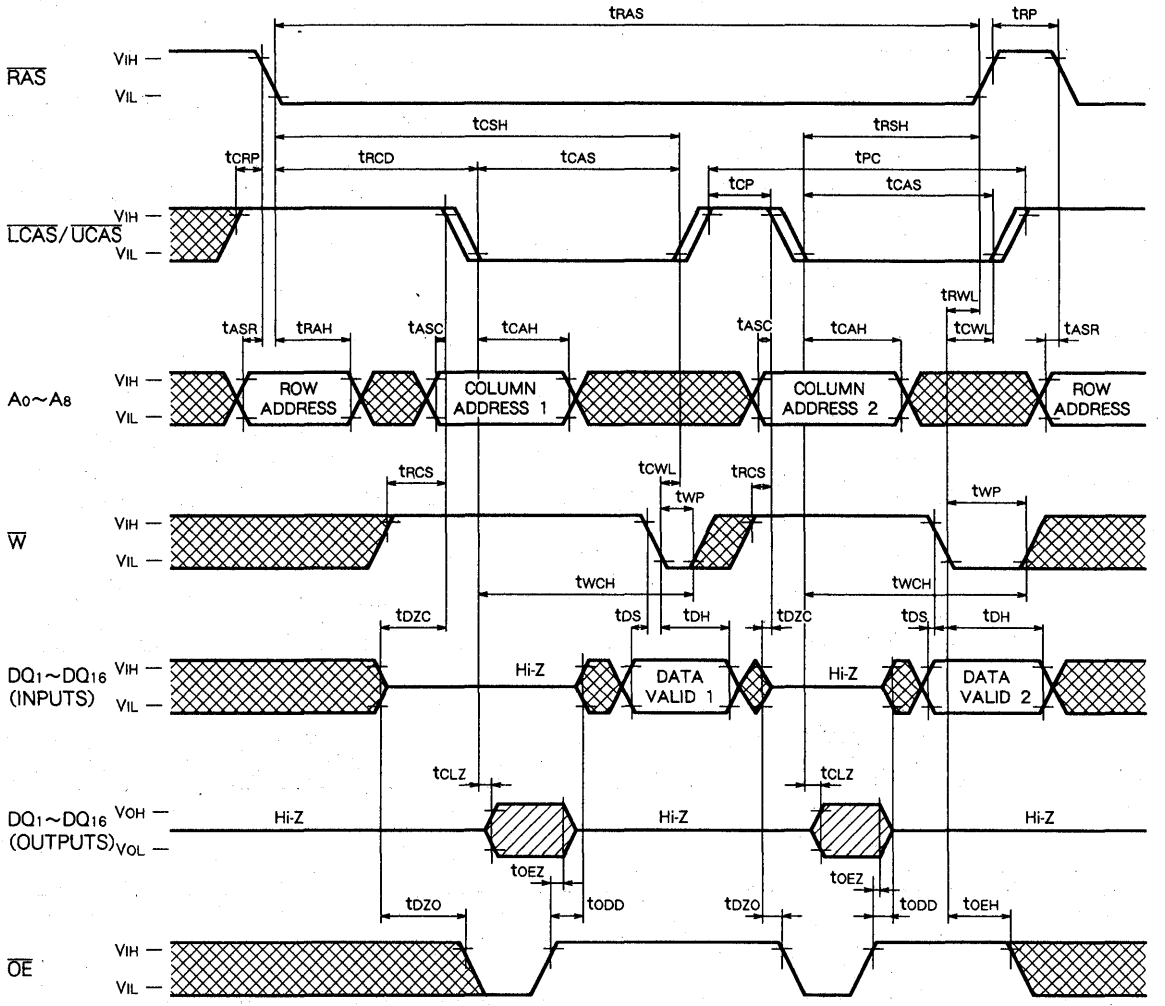
Fast Page Mode Write Cycle (Early Write)



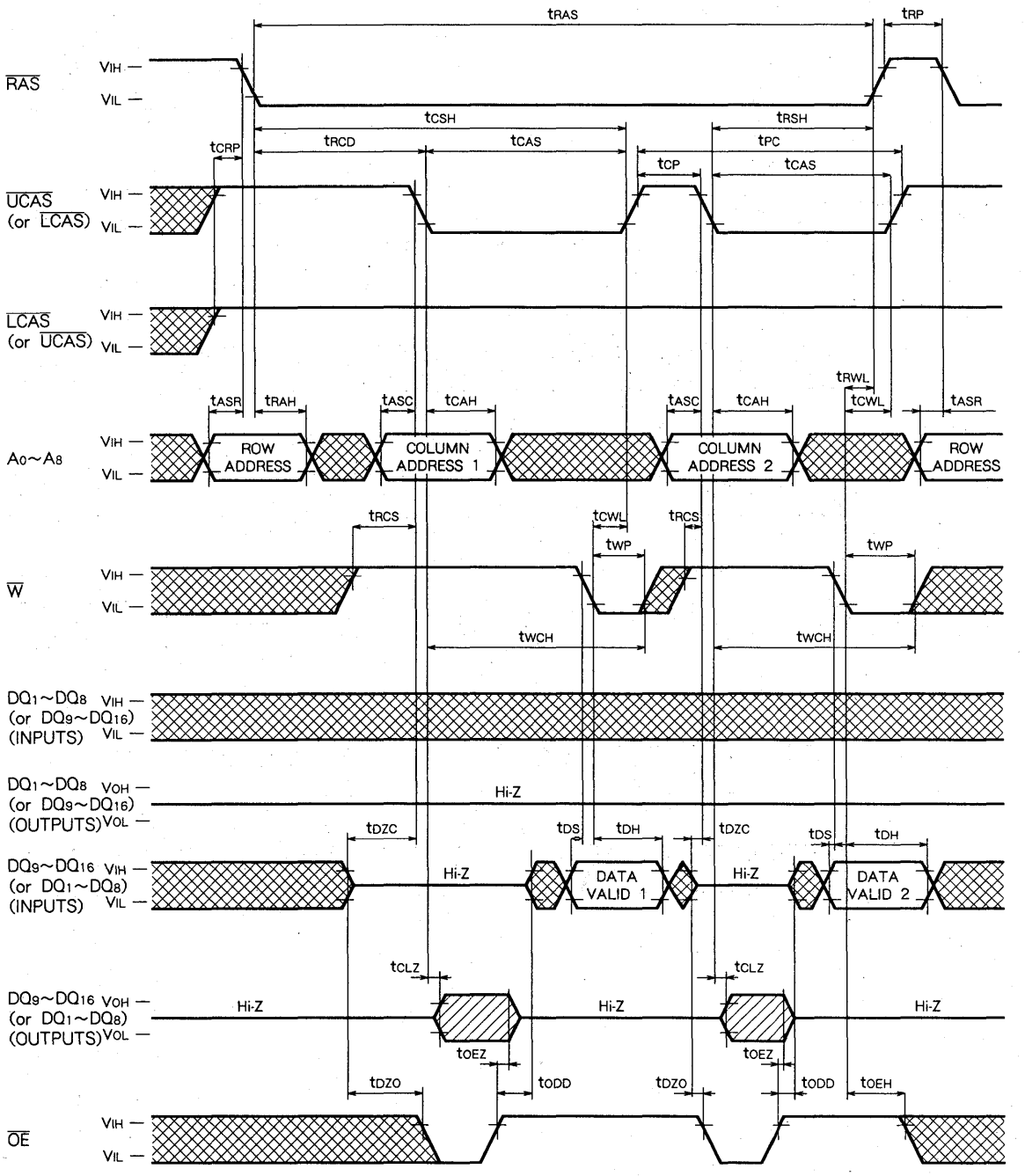
Fast Page Mode Byte Write Cycle (Early Write)



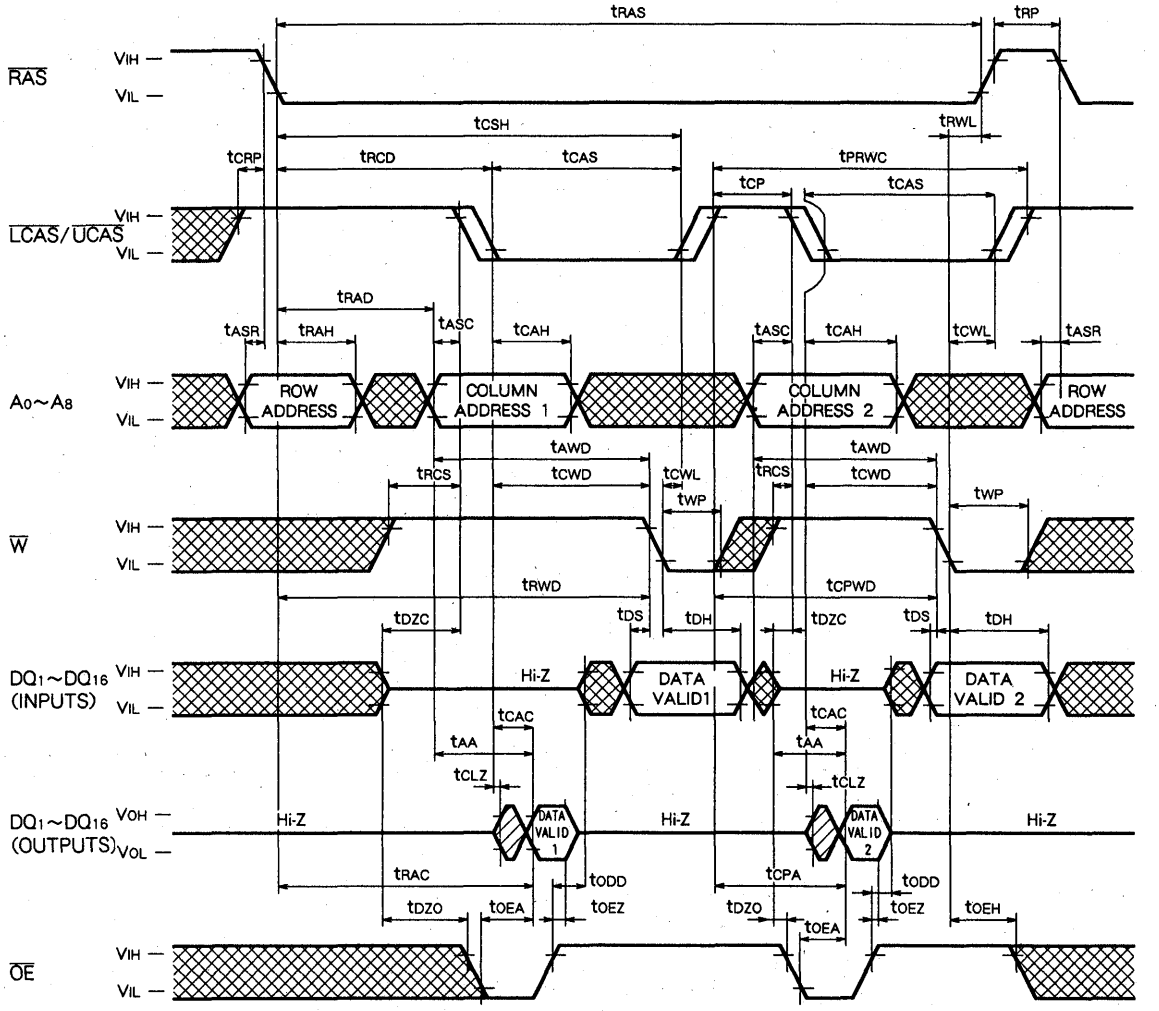
Fast Page Mode Write Cycle (Delayed Write)



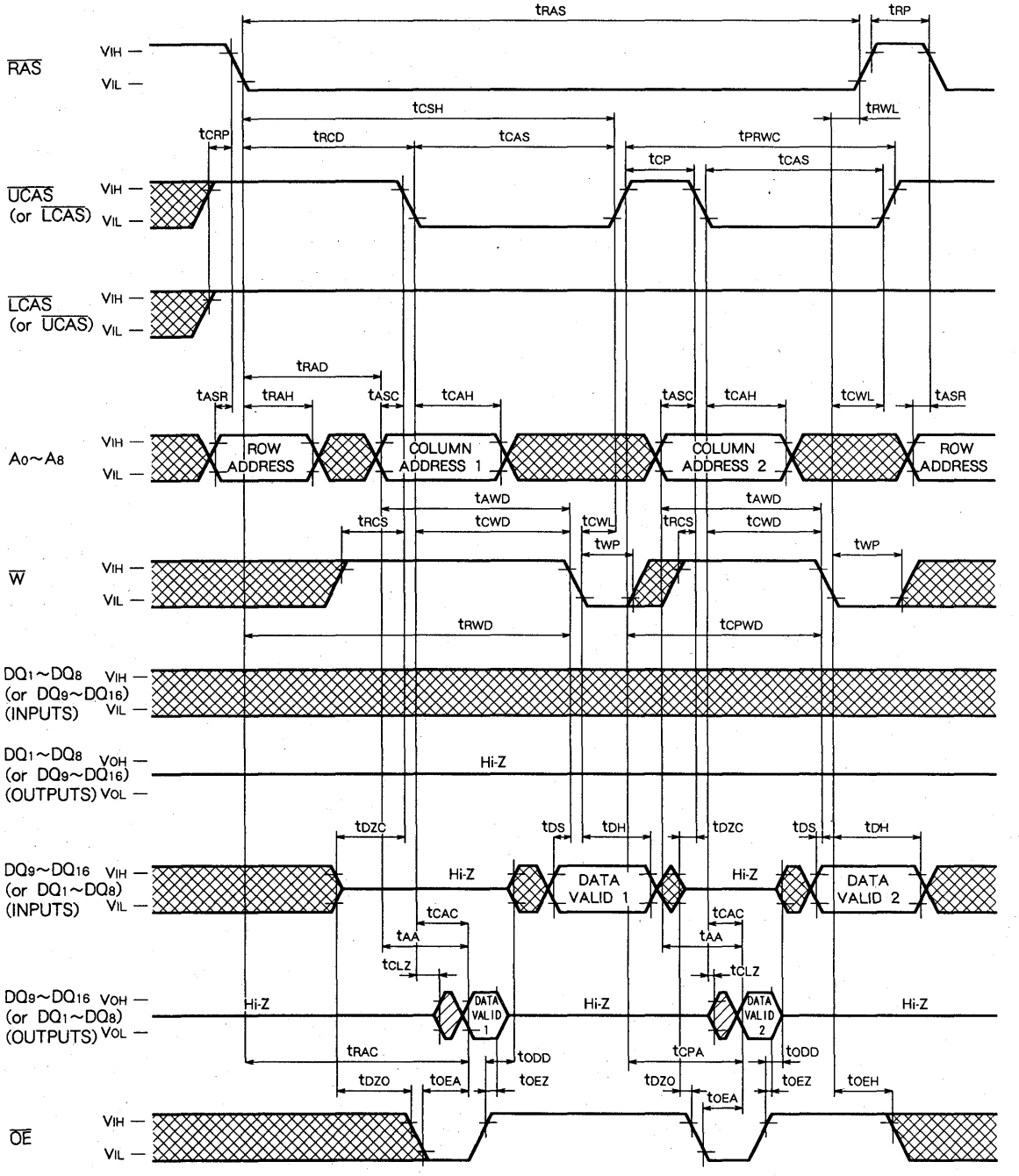
Fast Page Mode Byte Write Cycle (Delayed Write)



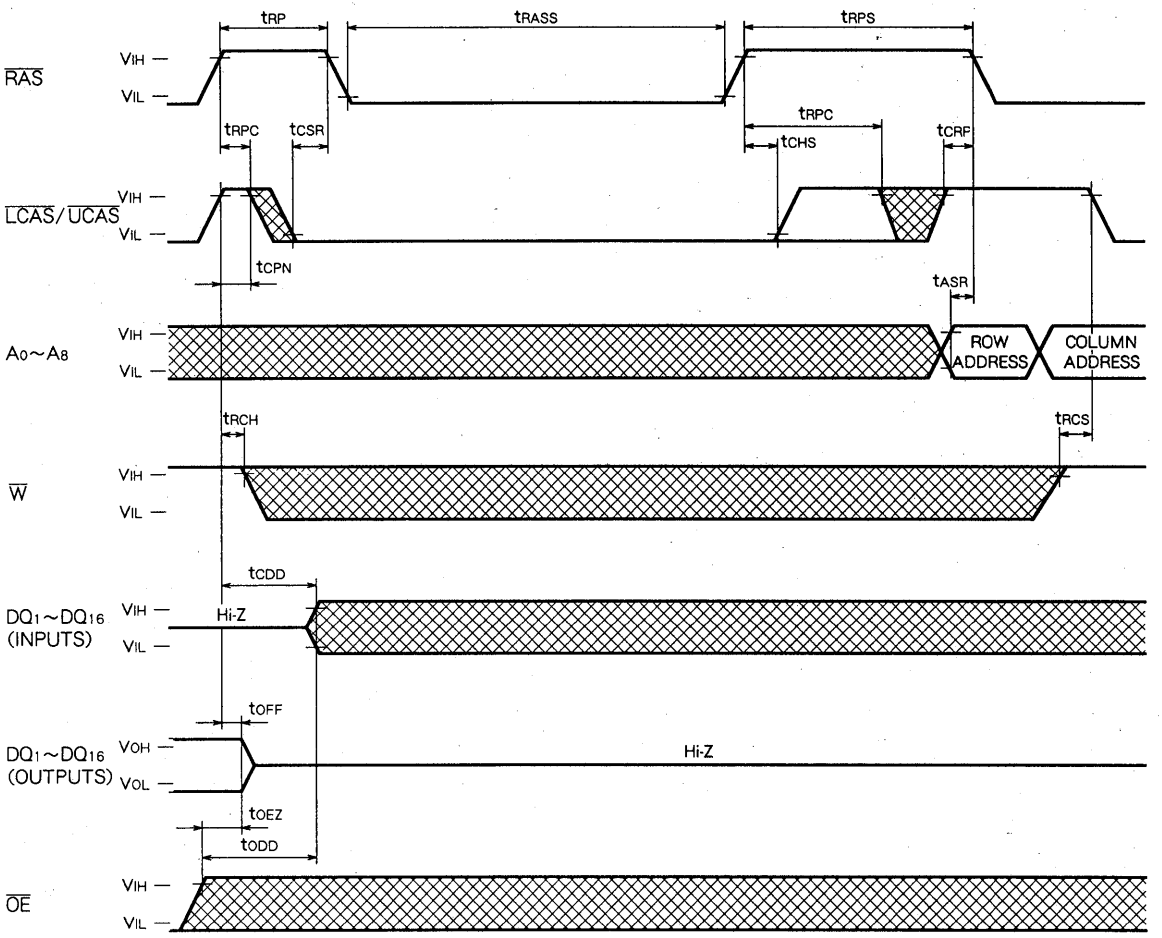
Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Byte Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 30)



Note 30. Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

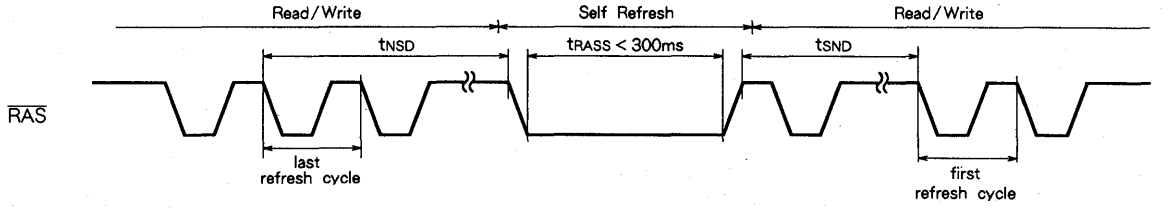
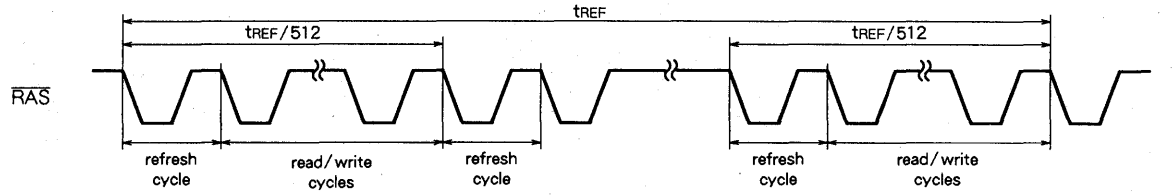


Table 2

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 8.2ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250μs max) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 constant period (16μs max) $\overline{RAS}$ only refresh cycles within 8.2ms.

Note :
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

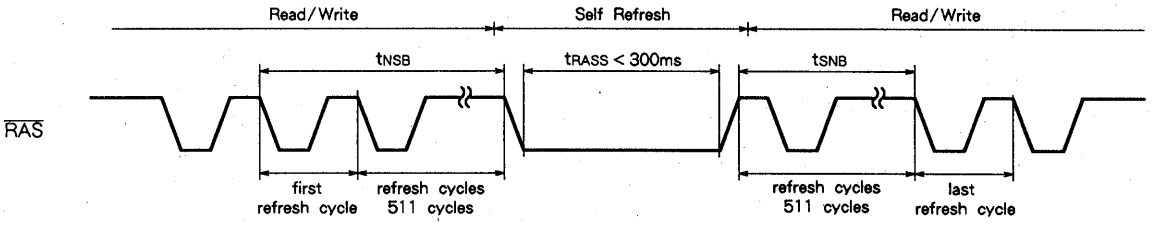
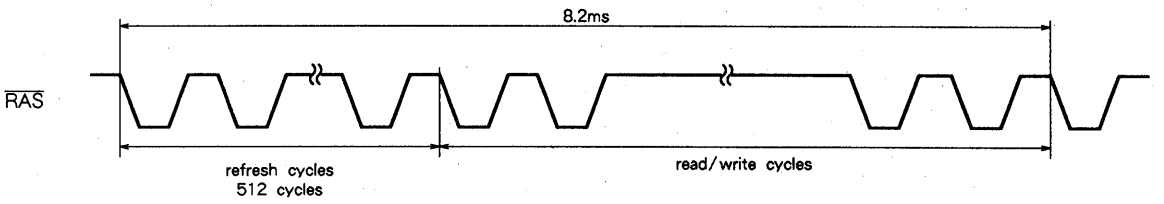


Table 3

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} + t_{SNB} \leqq 8.2ms$	
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 8.2ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2ms.

Definition of $\overline{RAS}$ only burst refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 continuous $\overline{RAS}$ only refresh cycles within 8.2ms.

1.2.1 CBR burst refresh

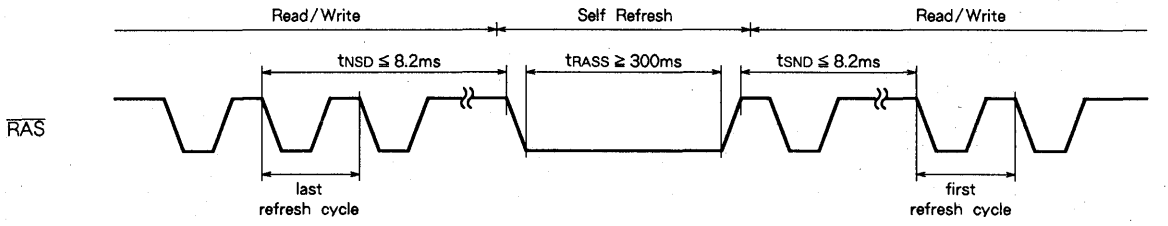
- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

1.2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geq 300ms$

(A) Timing diagram-A



Timing diagram-B

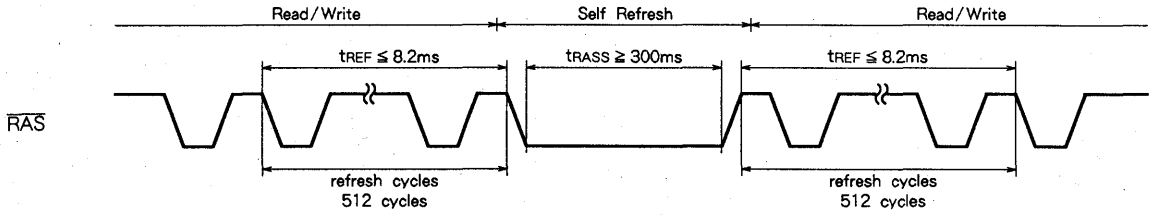


Table 4

Read/Write	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
$\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 8.2ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 8.2ms.

2.1. 2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh

- Before and after the self refresh, 512 refresh cycles should be executed within 8.2ms for each refresh operation.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V4260CTP-6,-7,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is small enough for battery back-up application.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4260CTP-6,-6S	60	15	30	15	110	333
M5M4V4260CTP-7,-7S	70	20	35	20	130	290

- Standard 44 pin TSOP (II)
- Single 3.3±0.3V supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW (Max)
  - CMOS Input level ---------- 550 μW (Max)*
- Operating power dissipation
  - M5M4V4260CTP-6,-6S ---------- 396mW (Max)
  - M5M4V4260CTP-7,-7S ---------- 342mW (Max)
- Self refresh capability*
  - Self refresh current ---------- 100 μA (Max)
- Extended refresh capability
  - Extended refresh current ---------- 100 μA (Max)
- Fast-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{LCAS}$ / $\overline{UCAS}$ and $\overline{OE}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 128ms (A_0~A_8)*
- Byte or word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

*: Applicable to self refresh version (M5M4V4260CTP-6S,-7S : option) only

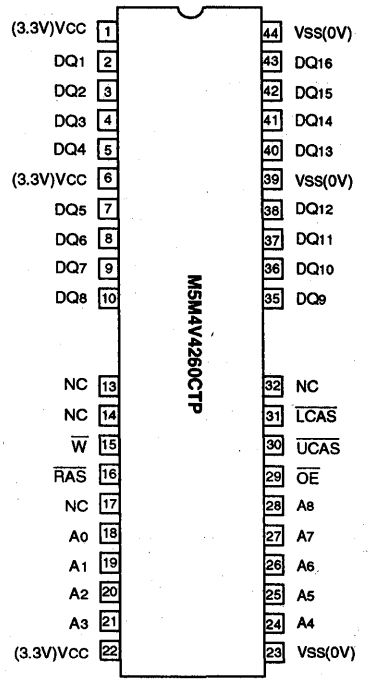
APPLICATION

Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_8	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-L (400mil TSOP Nomal Bend)

NC: NO CONNECTION

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

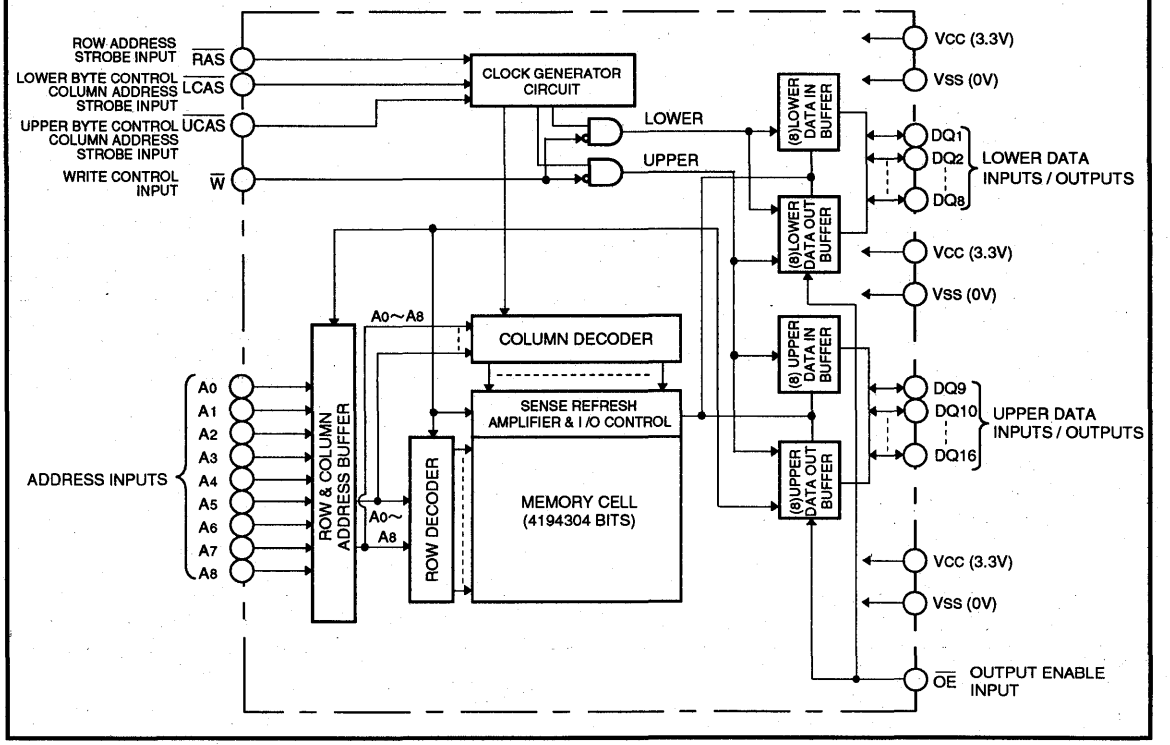
In addition to normal read,write and read-modify-write operations the M5M4V4260CTP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs							Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	DQ1~DQ8	DQ9~DQ16		
Lower byte read	ACT	ACT	NAC	NAC	ACT	APD	APD	DOUT	OPN	YES	Fast page mode identical
Upper byte read	ACT	NAC	ACT	NAC	ACT	APD	APD	OPN	DOUT	YES	
Word read	ACT	ACT	ACT	NAC	ACT	APD	APD	DOUT	DOUT	YES	
Lower byte write	ACT	ACT	NAC	ACT	NAC	APD	APD	DIN	DNC	YES	
Upper byte write	ACT	NAC	ACT	ACT	NAC	APD	APD	DNC	DIN	YES	
Word write	ACT	ACT	ACT	ACT	NAC	APD	APD	DIN	DIN	YES	
$\overline{RAS}$ only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	DNC	ACT	DNC	DNC	DOUT	DOUT	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Self refresh*	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	No	

Note : ACT : active, NAC : nonactive, DNC : don' t care, OPN : open

BLOCK DIAGRAM



PRELIMINARY
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5～4.6	V
V_I	Input voltage		-0.5～4.6	V
V_O	Output voltage		-0.5～4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70℃ , Vcc=3.3±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦Vcc	-5		5	μA
I_I	Input current		0V≦V_{IN}≦Vcc+0.3V, Other inputs pins=0V	-5		5	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V4260C-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M4V4260C-7,-7S				95	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V output open			0.5	
						0.1*	
$I_{CC3(AV)}$	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V4260C-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			110	mA
		M5M4V4260C-7,-7S				95	
$I_{CC4(AV)}$	Average supply current from Vcc Fast page mode (Note 3,4,5)	M5M4V4260C-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			110	mA
		M5M4V4260C-7,-7S				95	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V4260C-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			100	mA
		M5M4V4260C-7,-7S				85	
$I_{CC8(AV)}$*	Average supply current from Vcc Extended-refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0～A_8 ≦ 0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=250 μs, t_{RAS}=$t_{RAS\ min}$～1 μs			100	μA
$I_{CC9(AV)}$*	Average supply current from Vcc Self-refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			100	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

PRELIMINARY
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CAPACITANCE (Ta=0~70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		15		20	ns

Note 6: An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 100pF, V_{OH}(I_{OH}=-2mA) and V_{OL}(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).
8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 5\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			8.2		8.2	ms
tREF	Refresh cycle time *			128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	15		20		ns
tT	Transition time	(Note 20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 22)	150		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	55	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	55		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	35		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	80		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 23)	50		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 25)	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

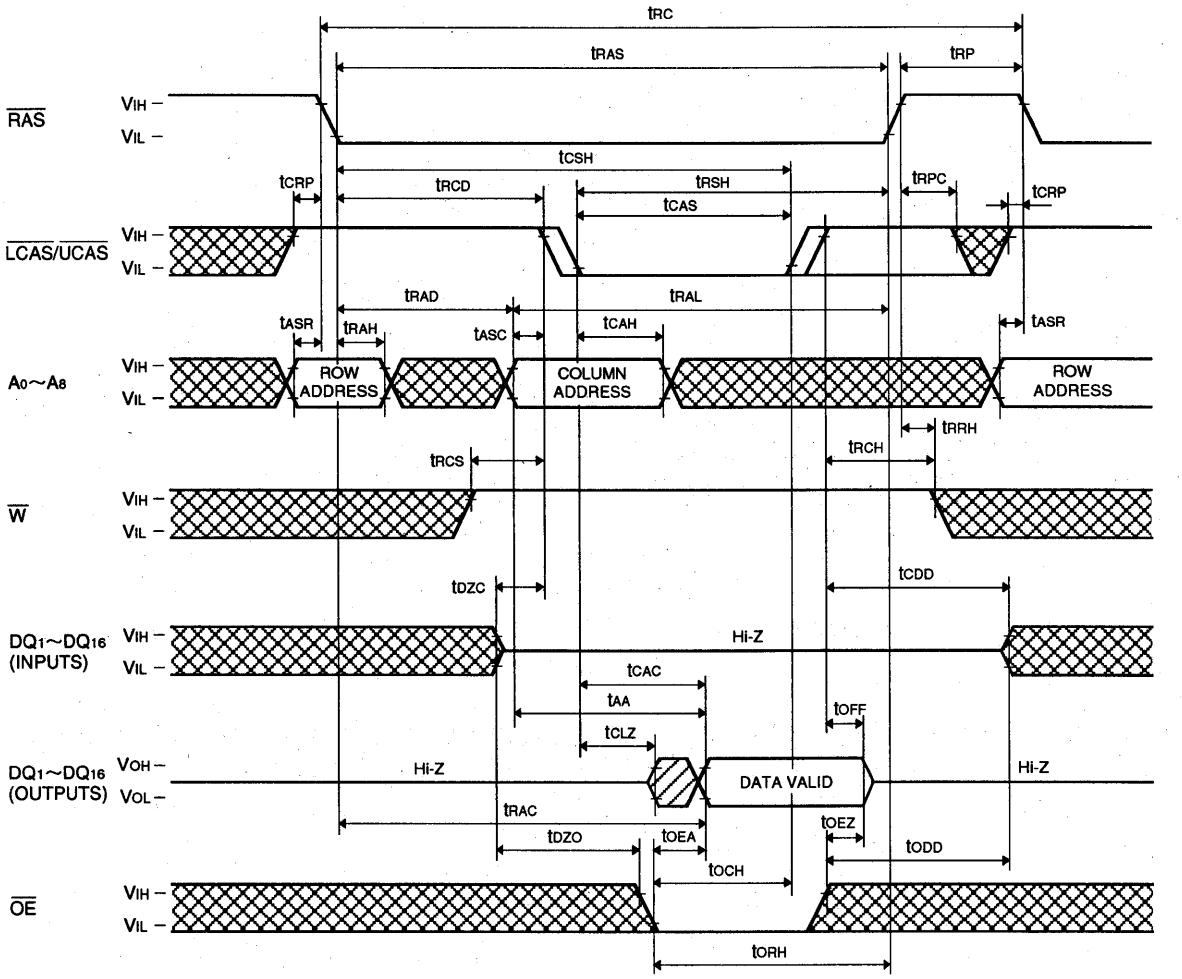
Symbol	Parameter	Limits				Unit
		M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	20		25		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle * (Note 28)

Symbol	Parameter	Limits				Unit
		M5M4V4260C-6,-6S		M5M4V4260C-7,-7S		
		Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		ns

Timing Diagrams (Note 29)
Read Cycle



Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
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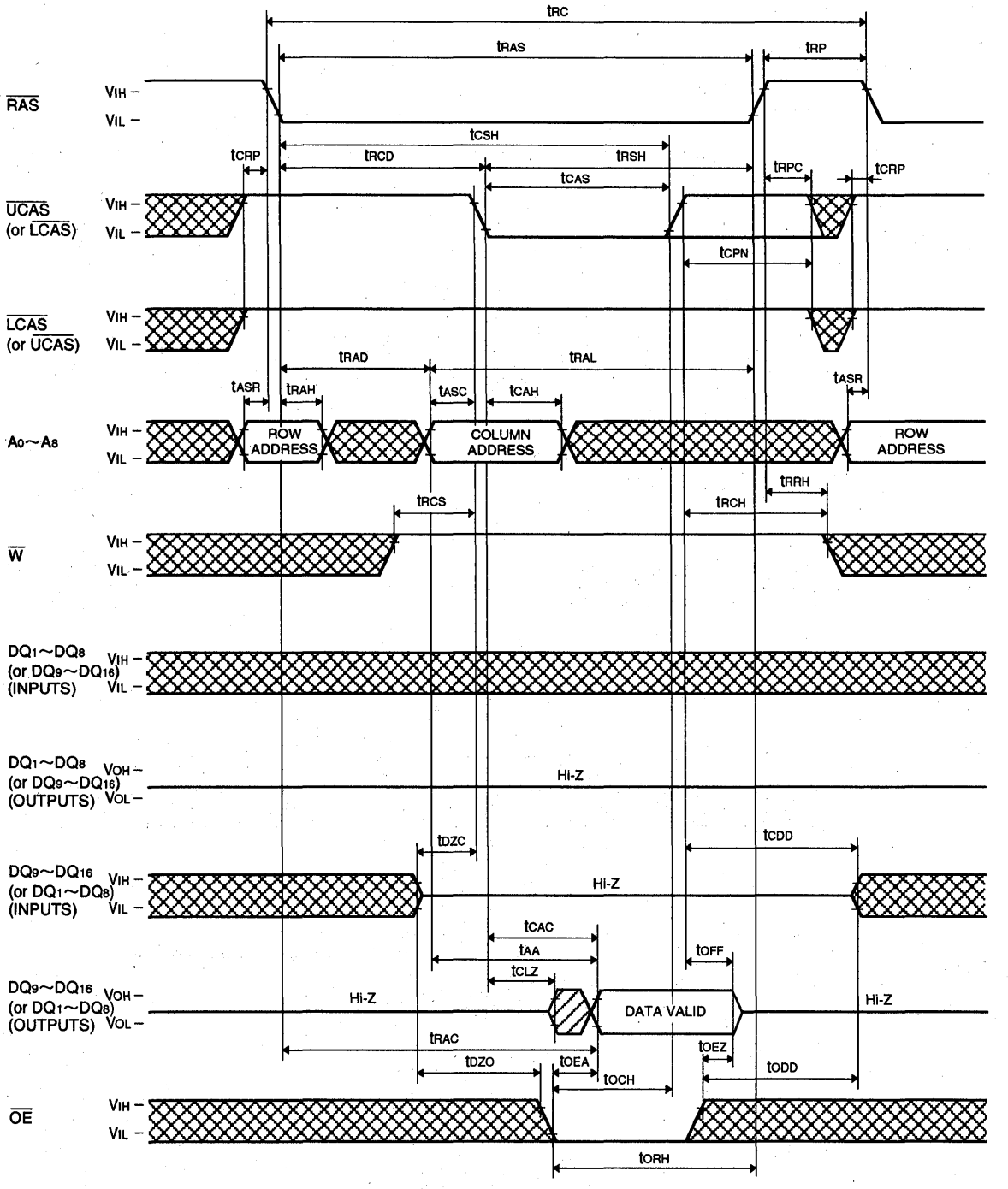
Byte Read Cycle



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PRELIMINARY
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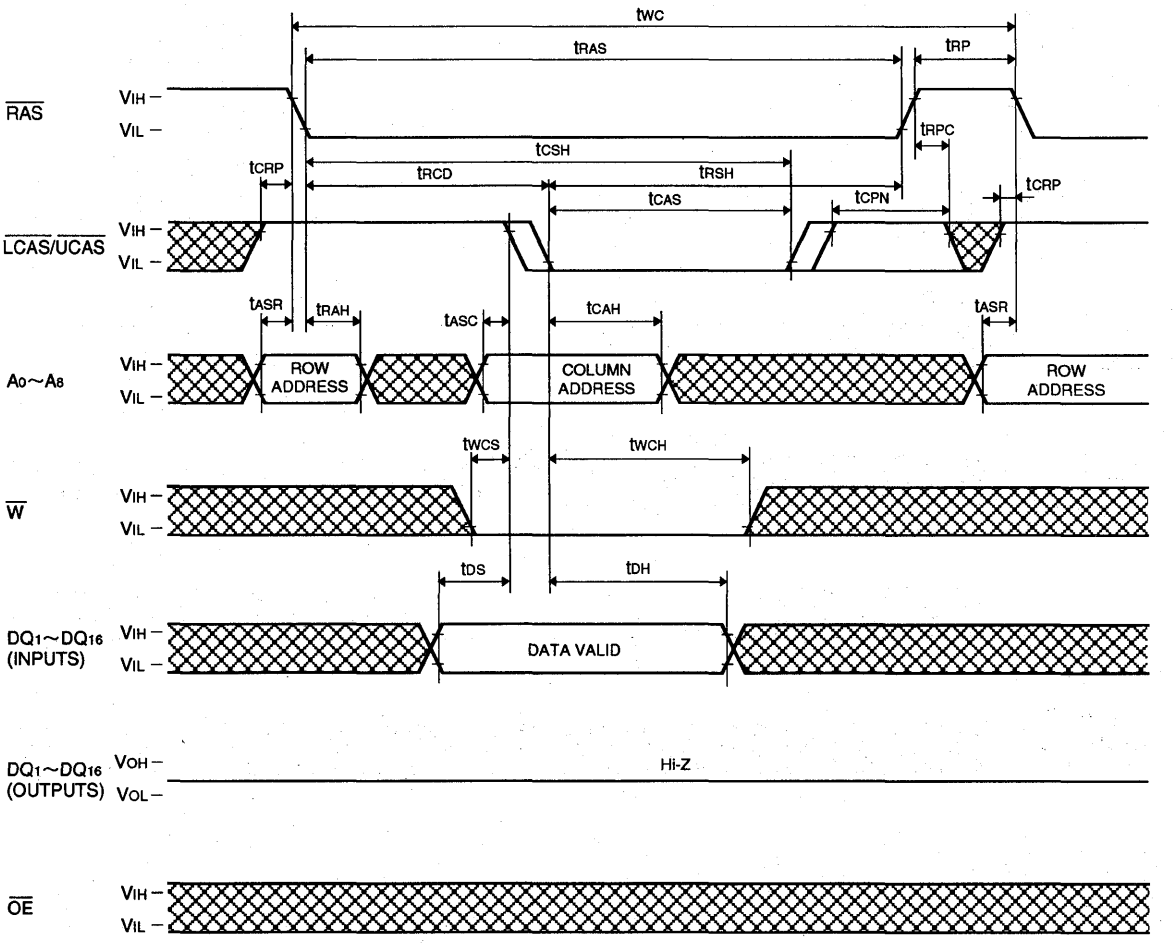
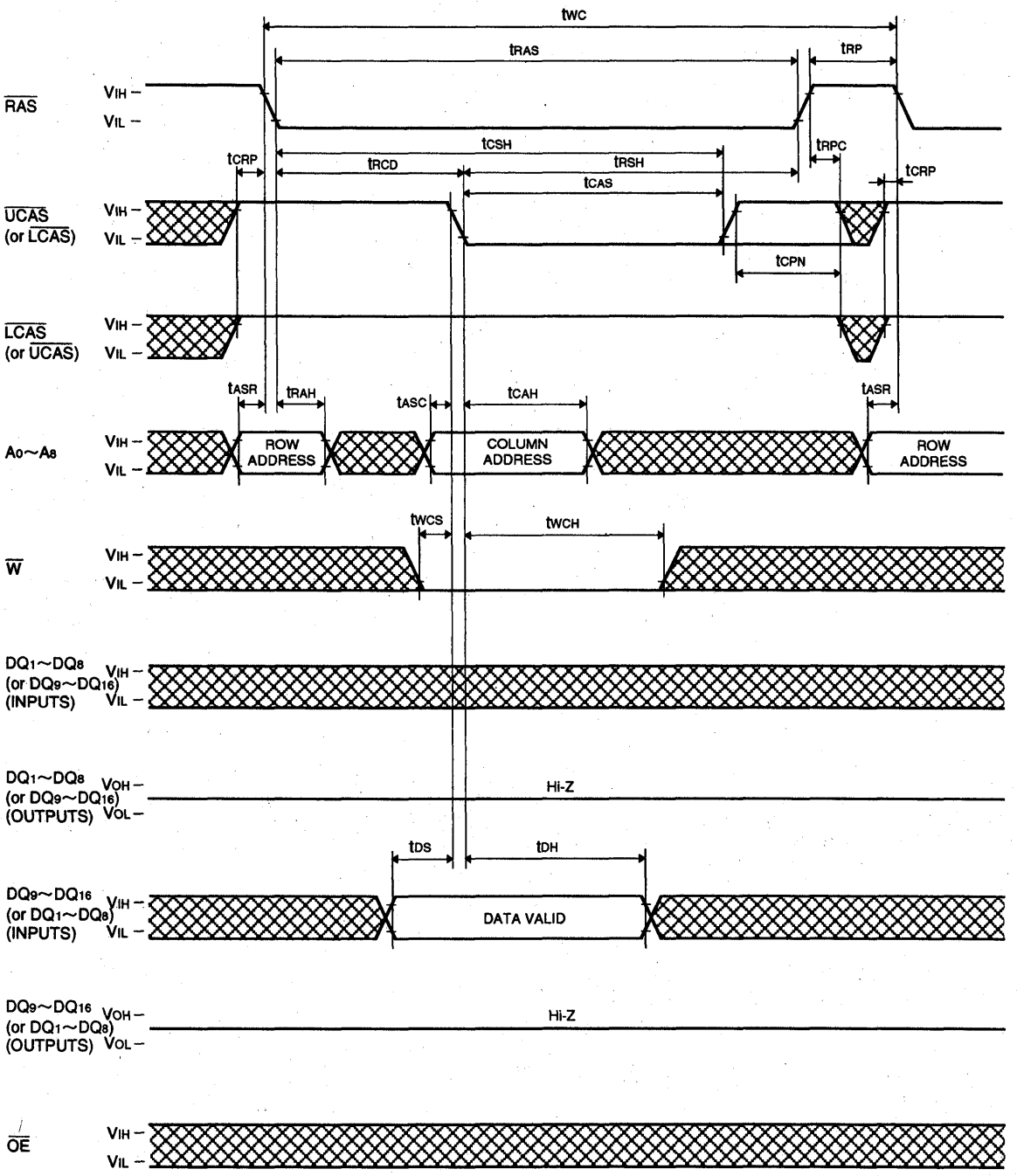
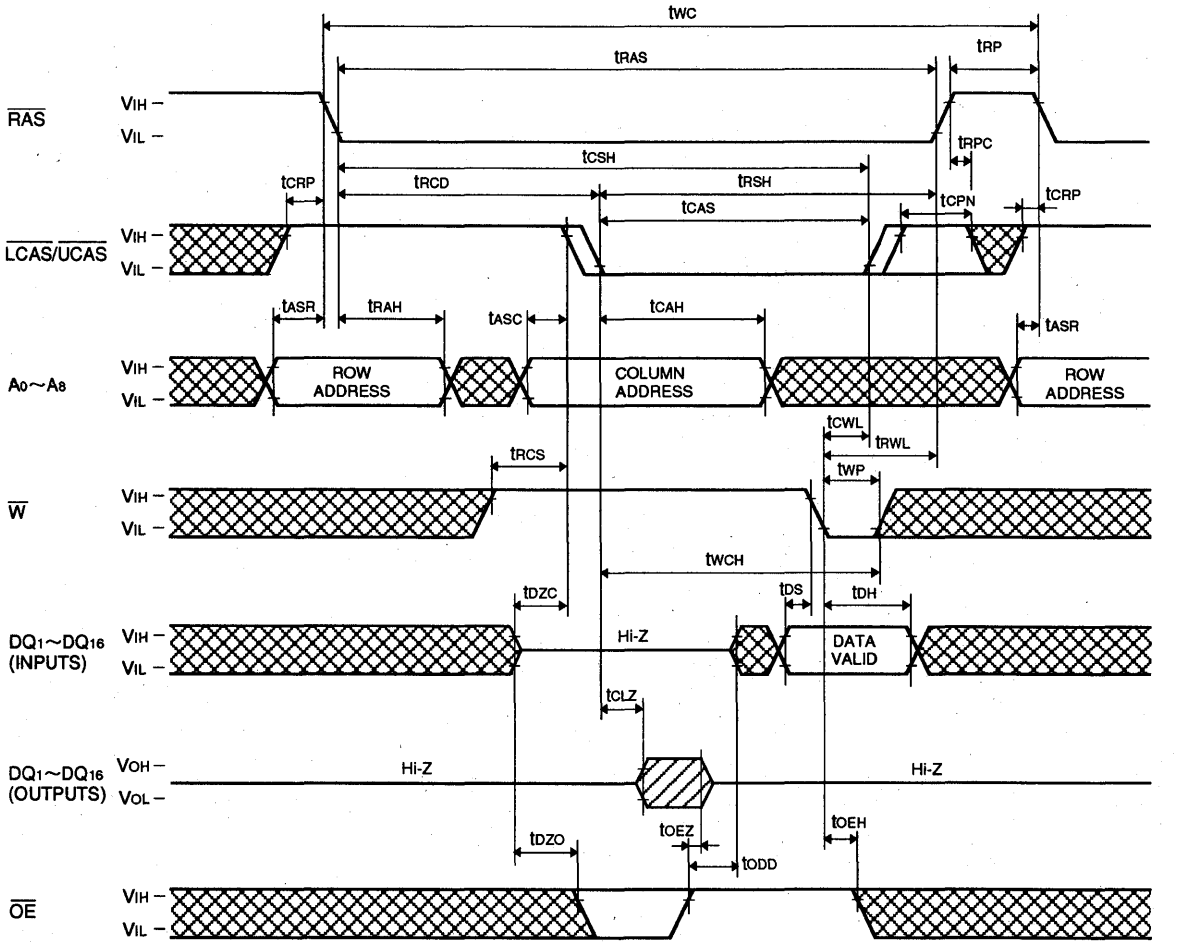
Write Cycle (Early write)



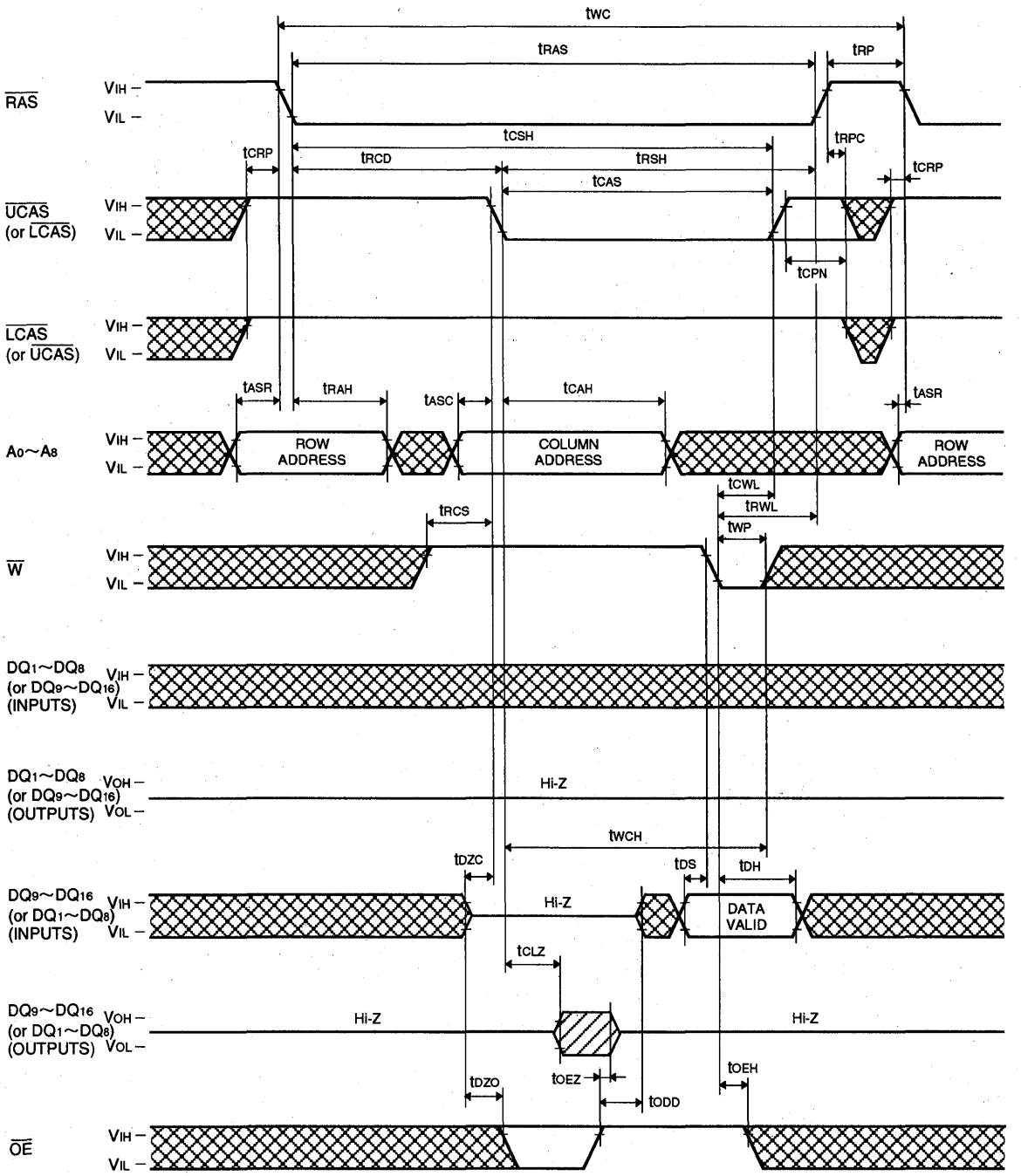
Byte Write Cycle (Early write)



Write Cycle (Delayed write)



Byte Write Cycle (Delayed write)



PRELIMINARY
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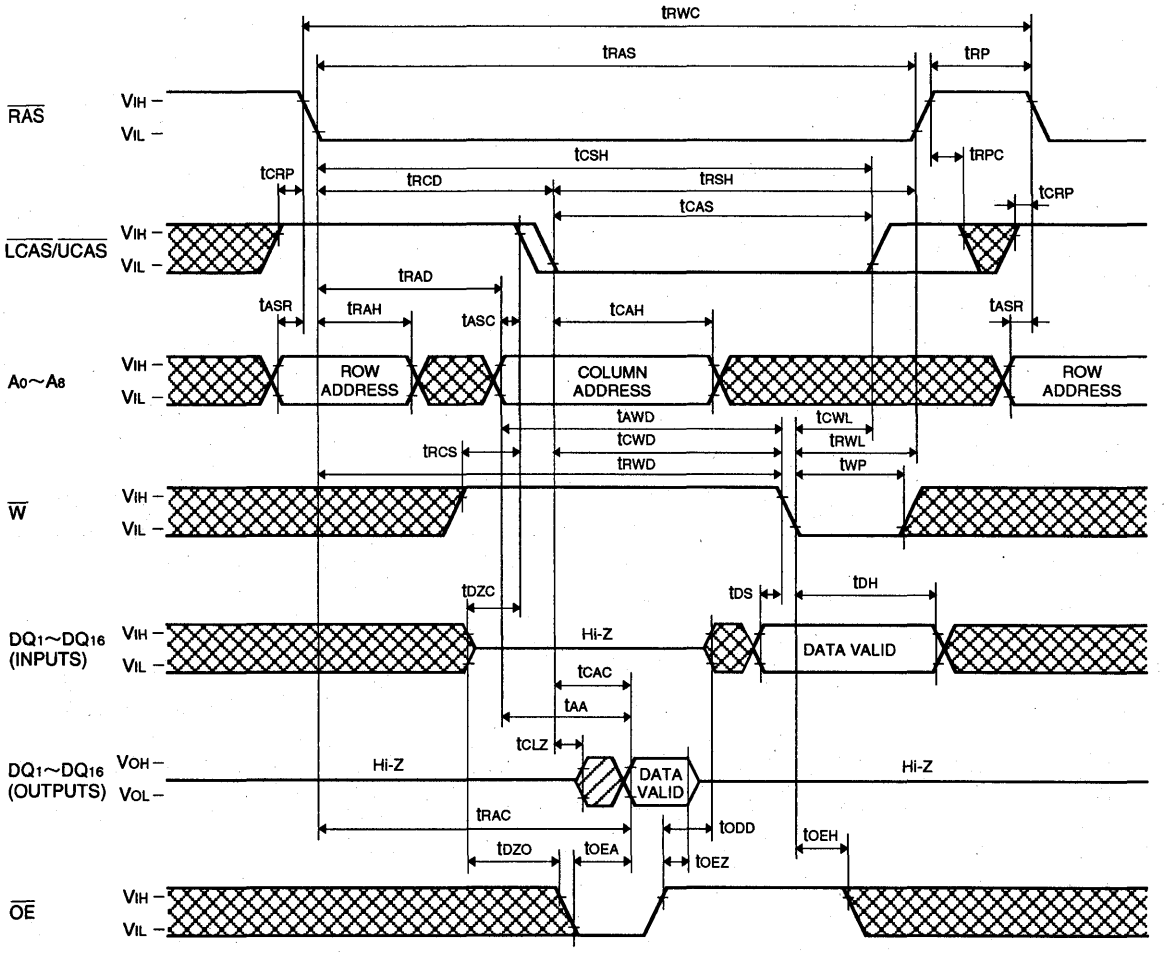
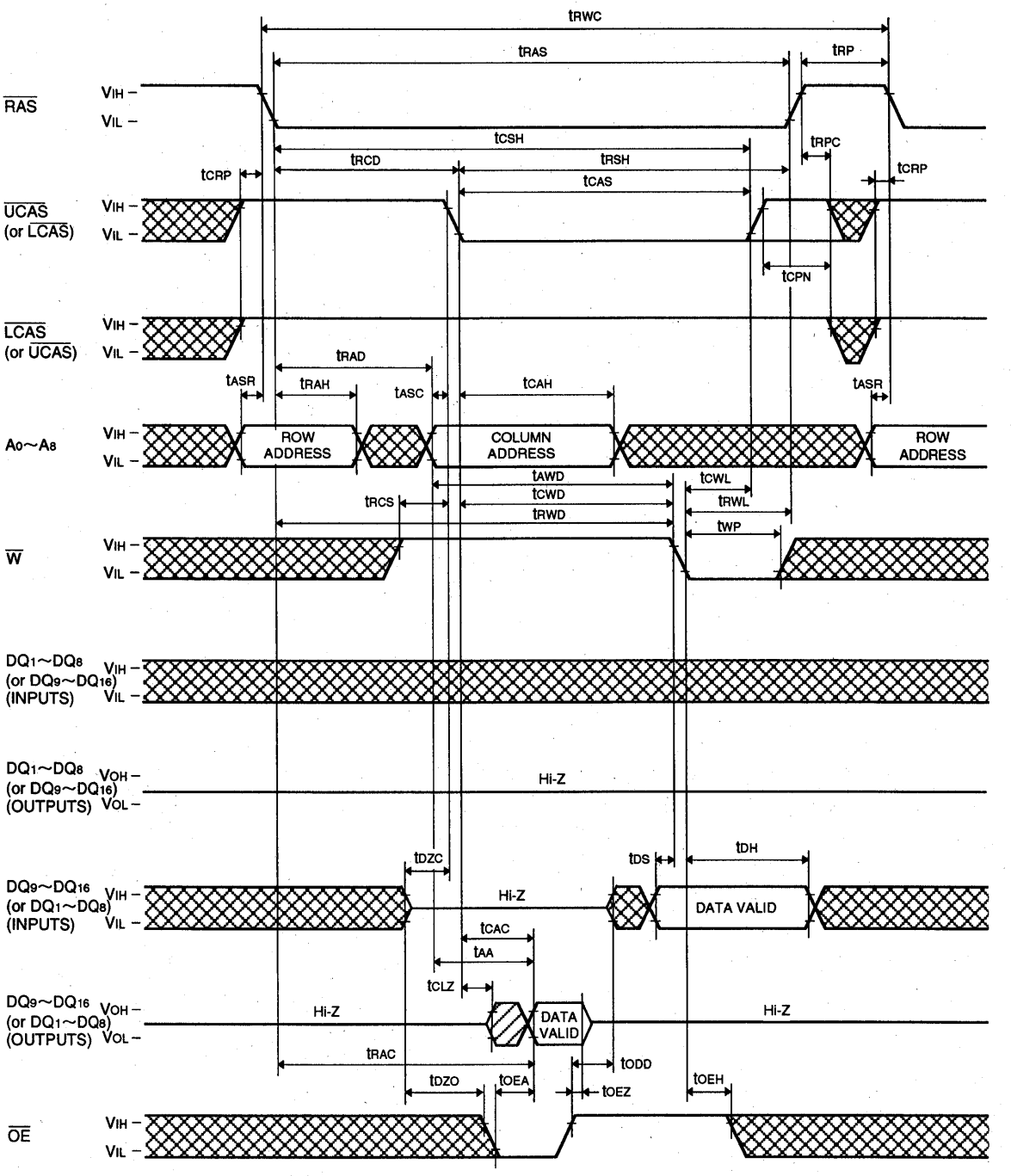
Read-Write, Read-Modify-Write Cycle

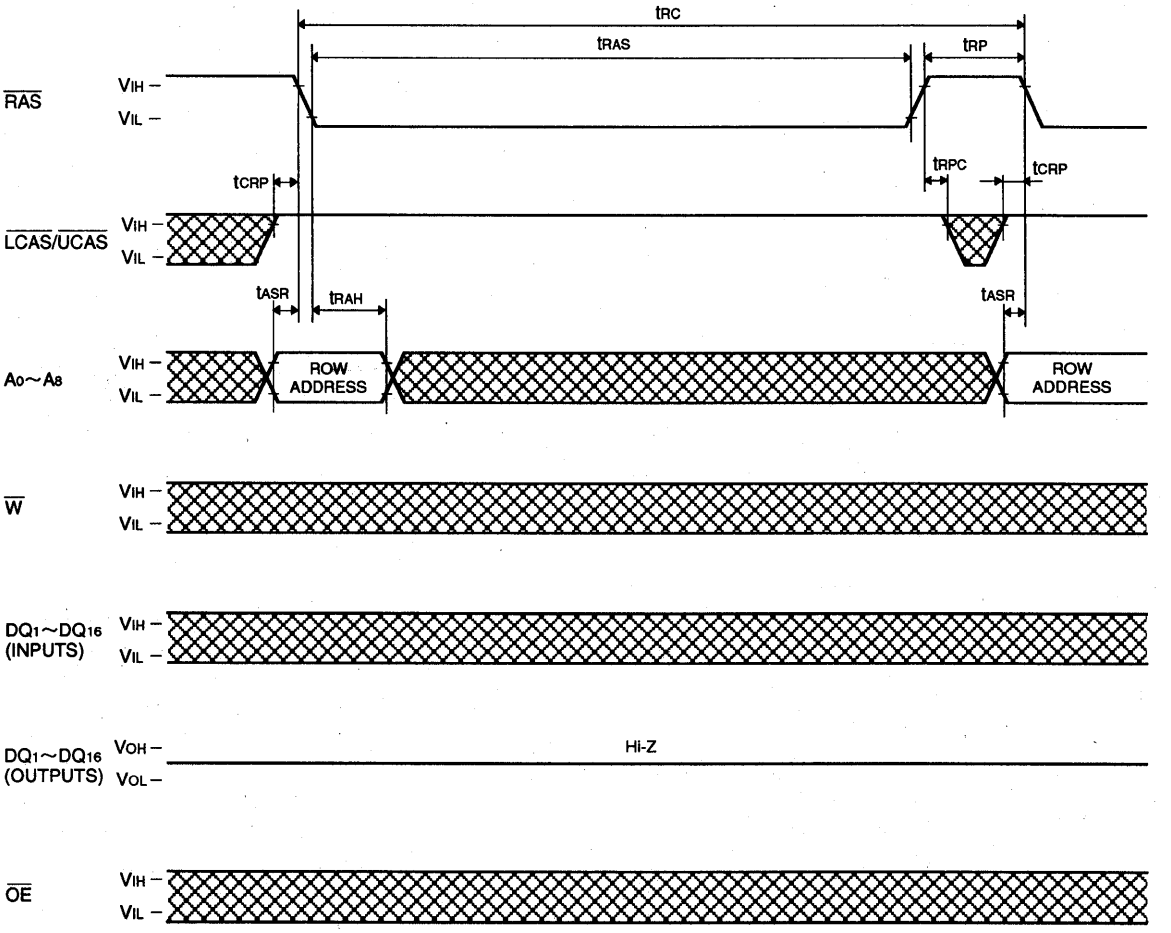


PRELIMINARY
Notice. This is not a final specification.
Some parametric limits are subject to change.

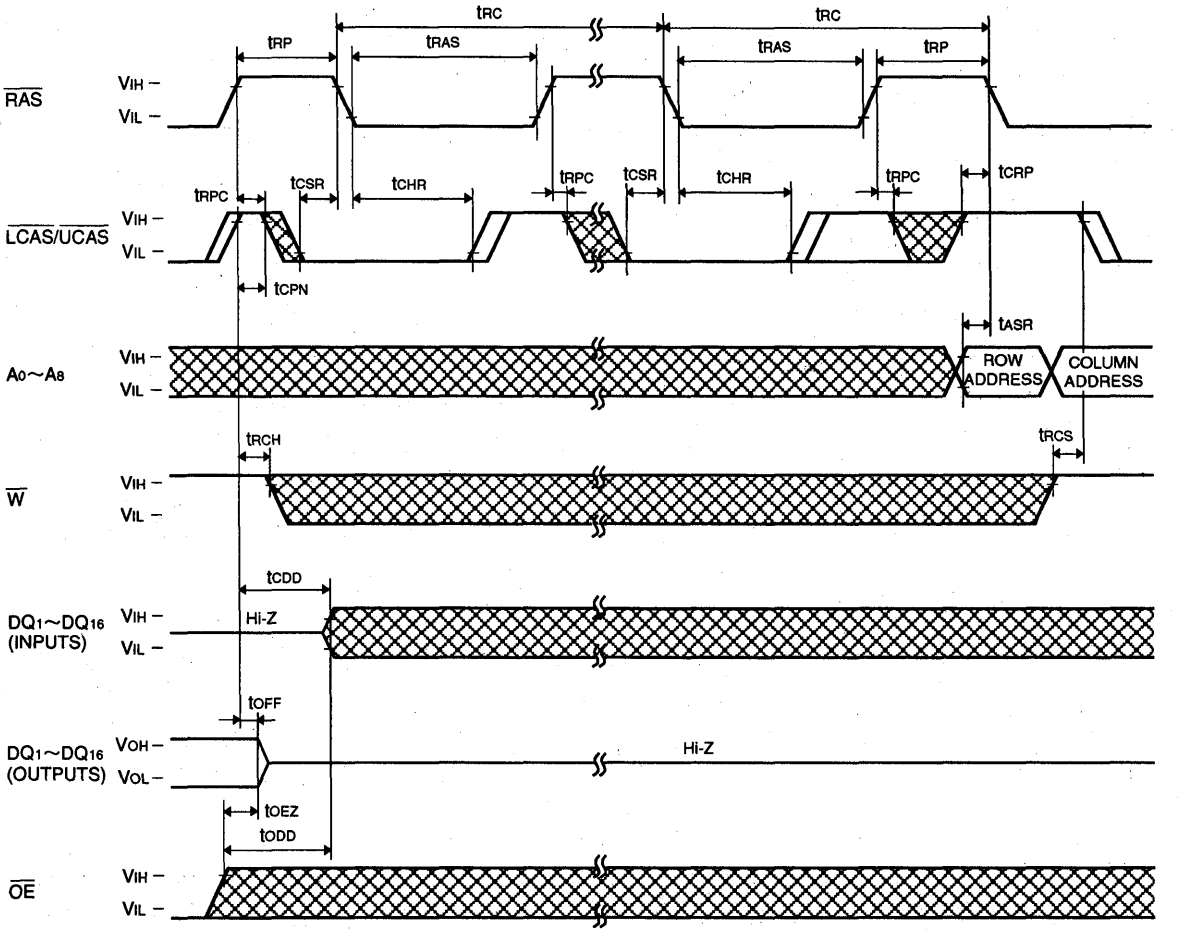
Byte Read-Write, Read-Modify-Write Cycle



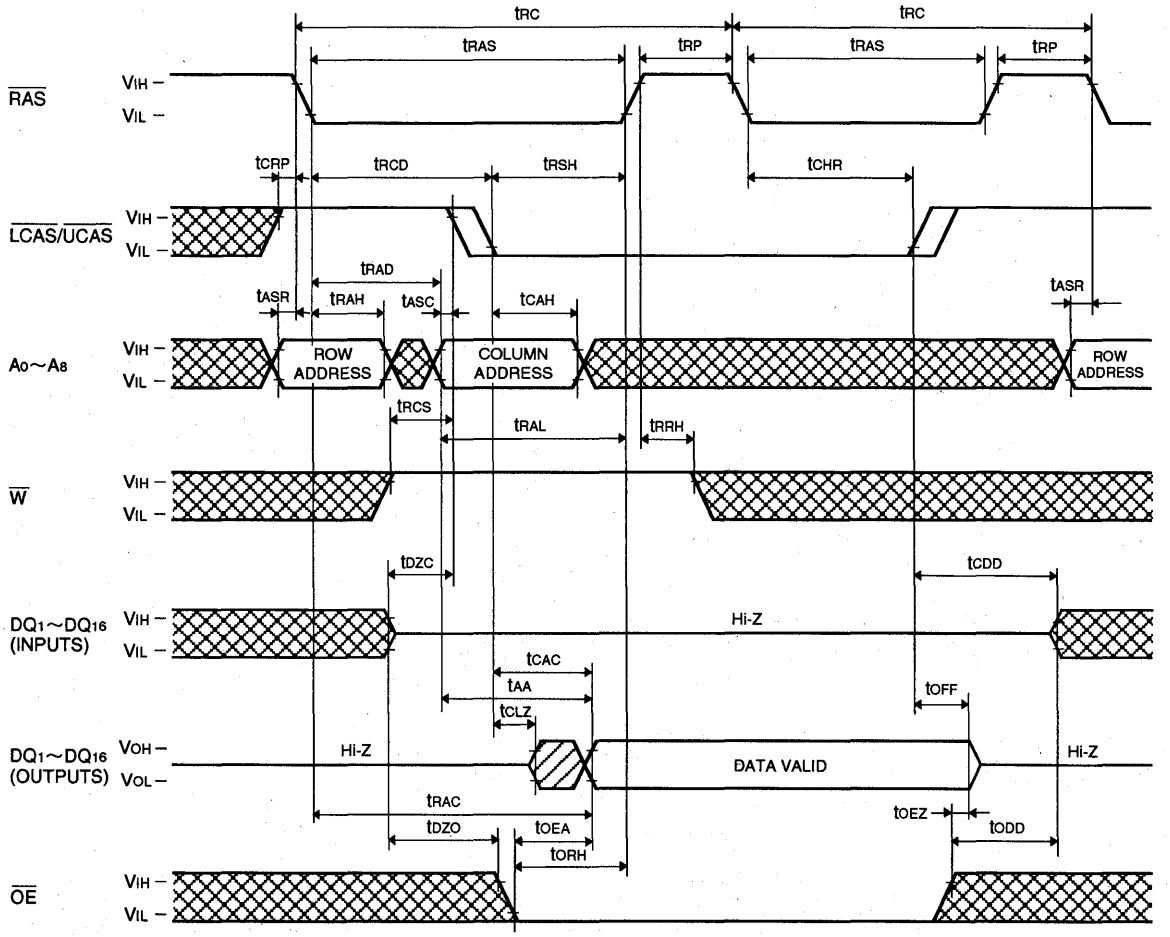
$\overline{RAS}$-only Refresh Cycle



CAS before RAS Refresh Cycle, Extended Refresh Cycle *

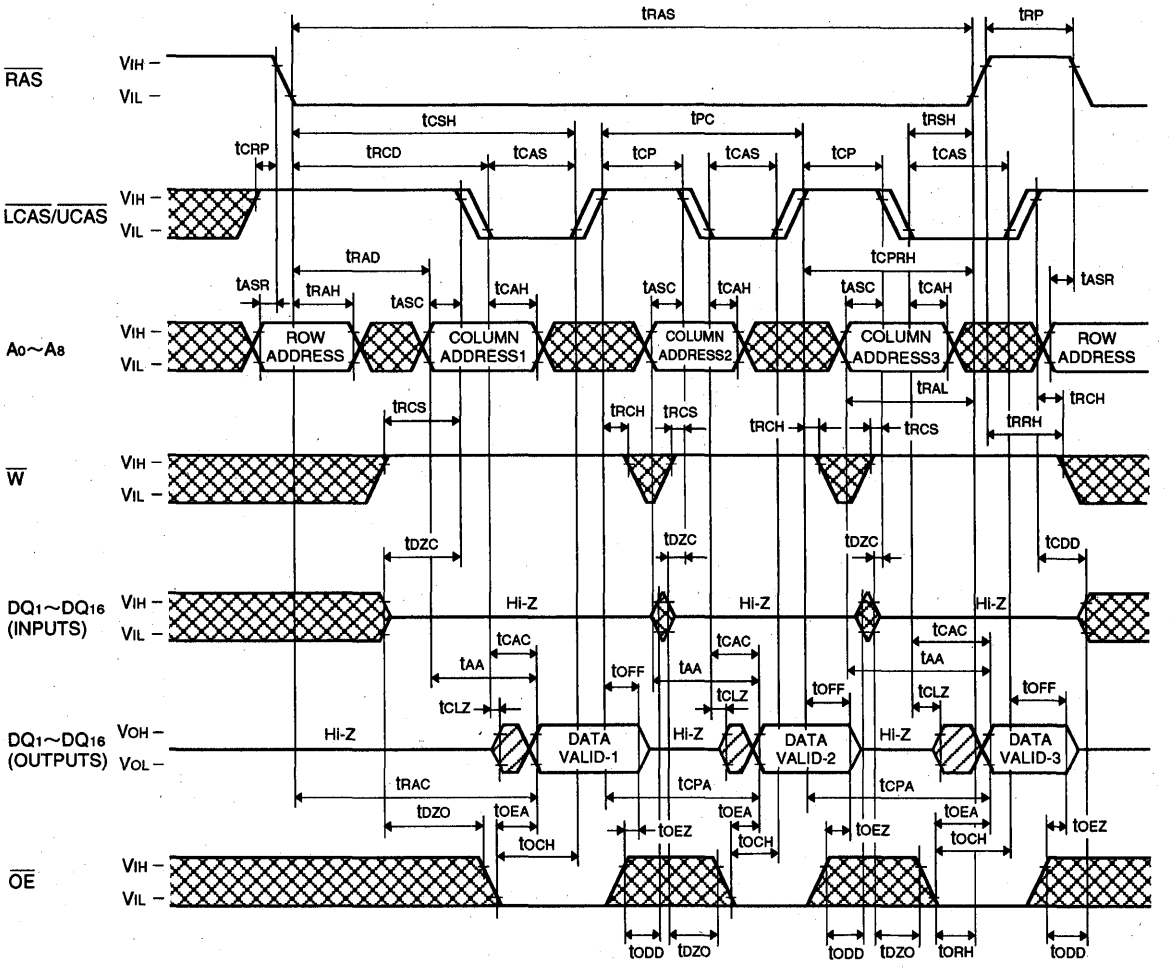


Hidden Refresh Cycle (Read) (Note 30)



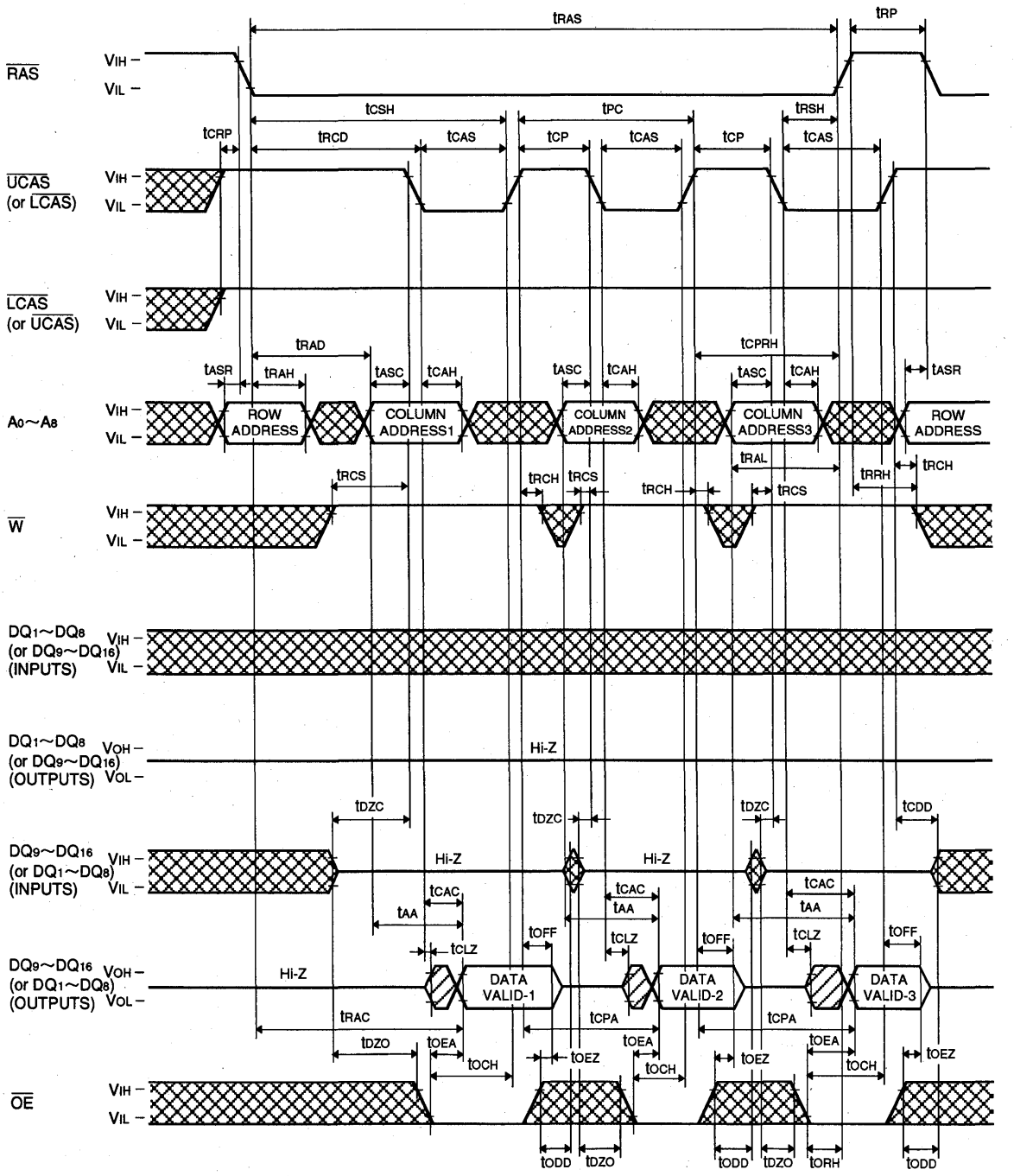
Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

Fast Page Mode Read Cycle



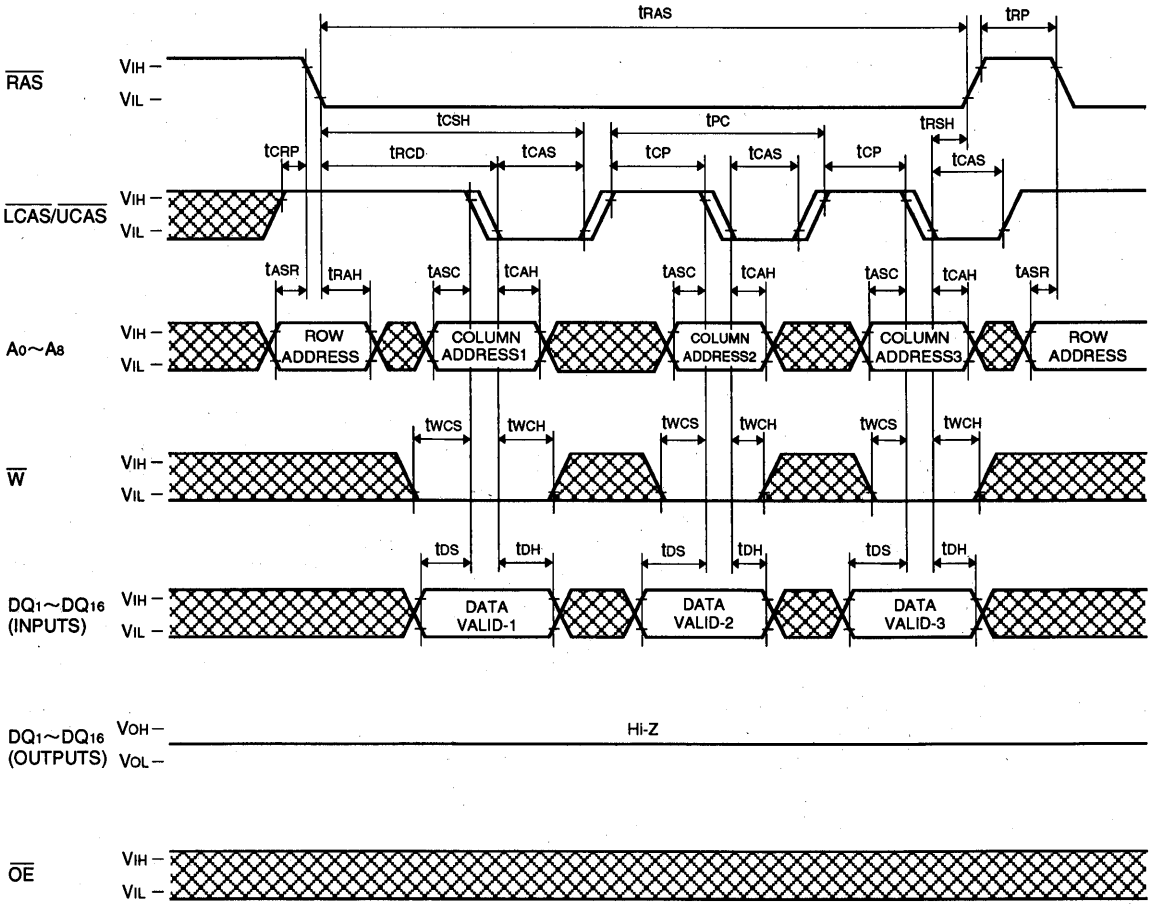
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Byte Read Cycle



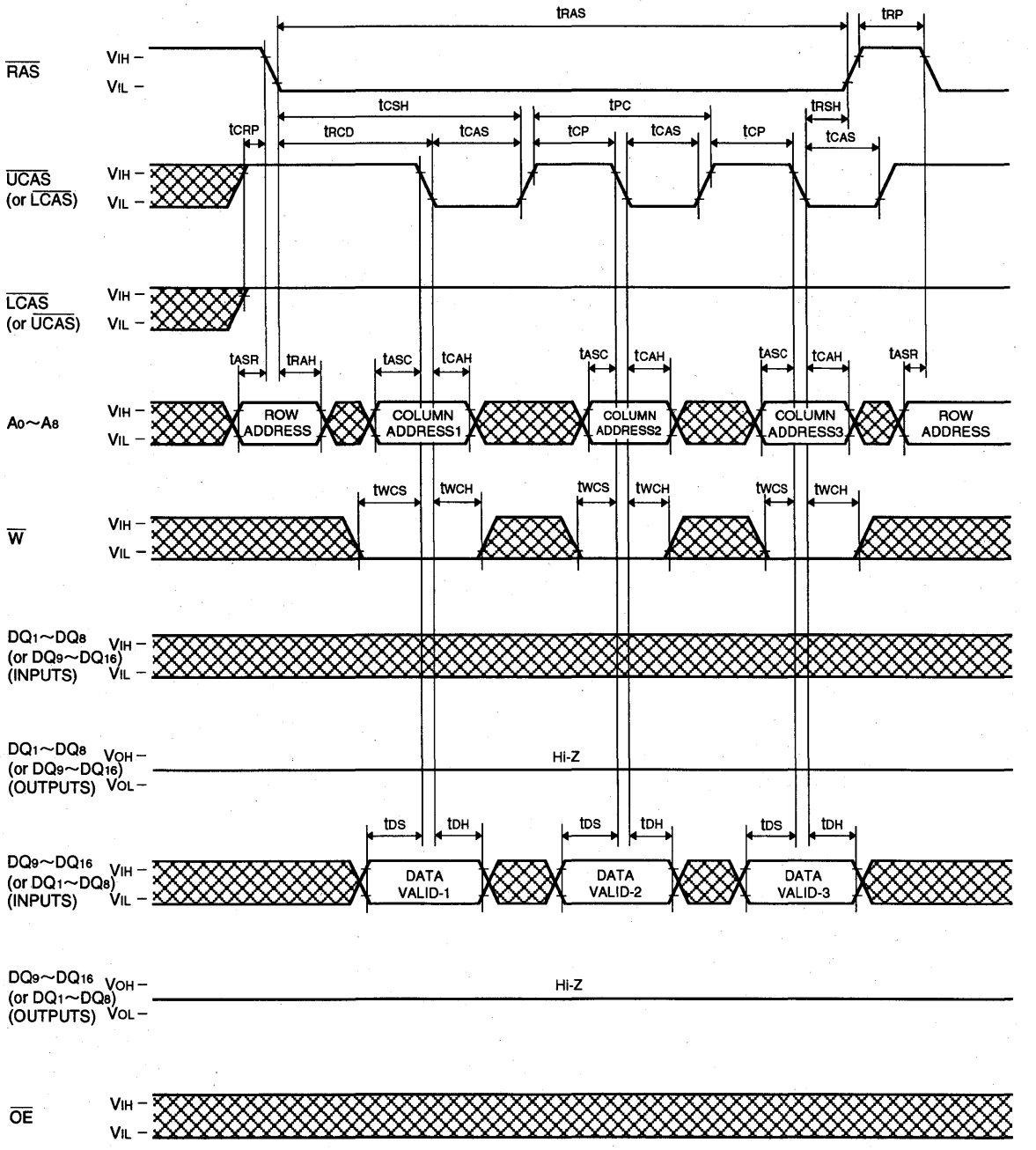
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)

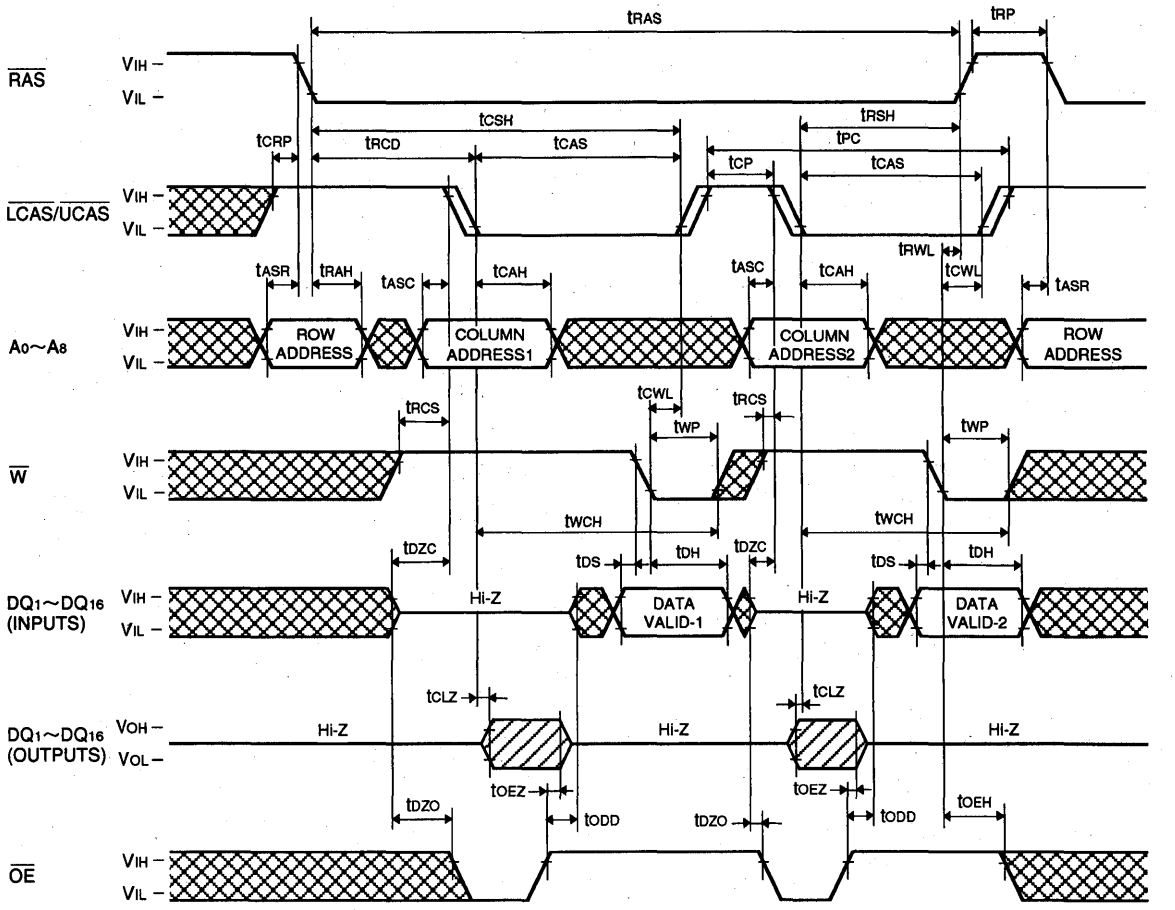


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Byte Write Cycle (Early Write)

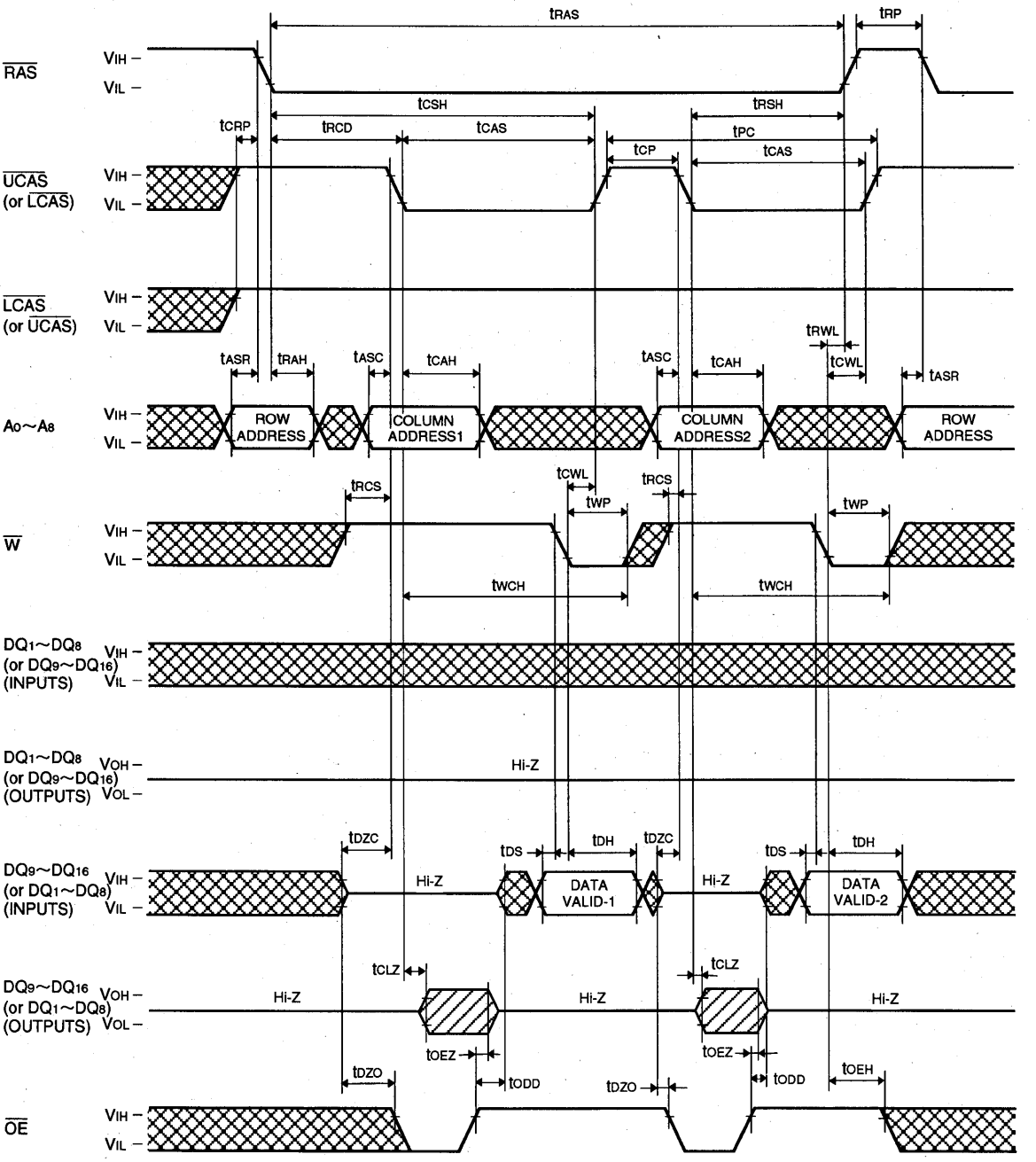


Fast-Page Mode Write Cycle (Delayed Write)

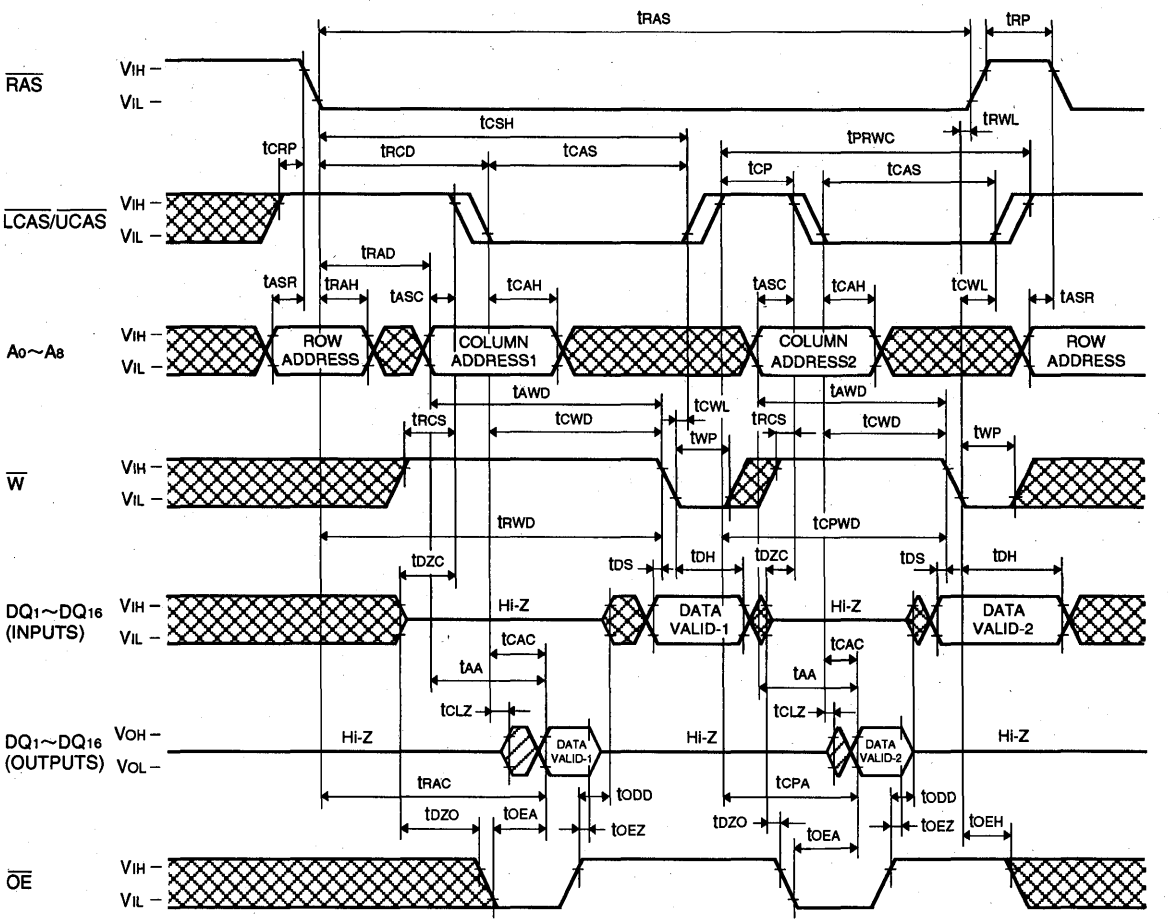


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast-Page Mode Byte Write Cycle (Delayed Write)

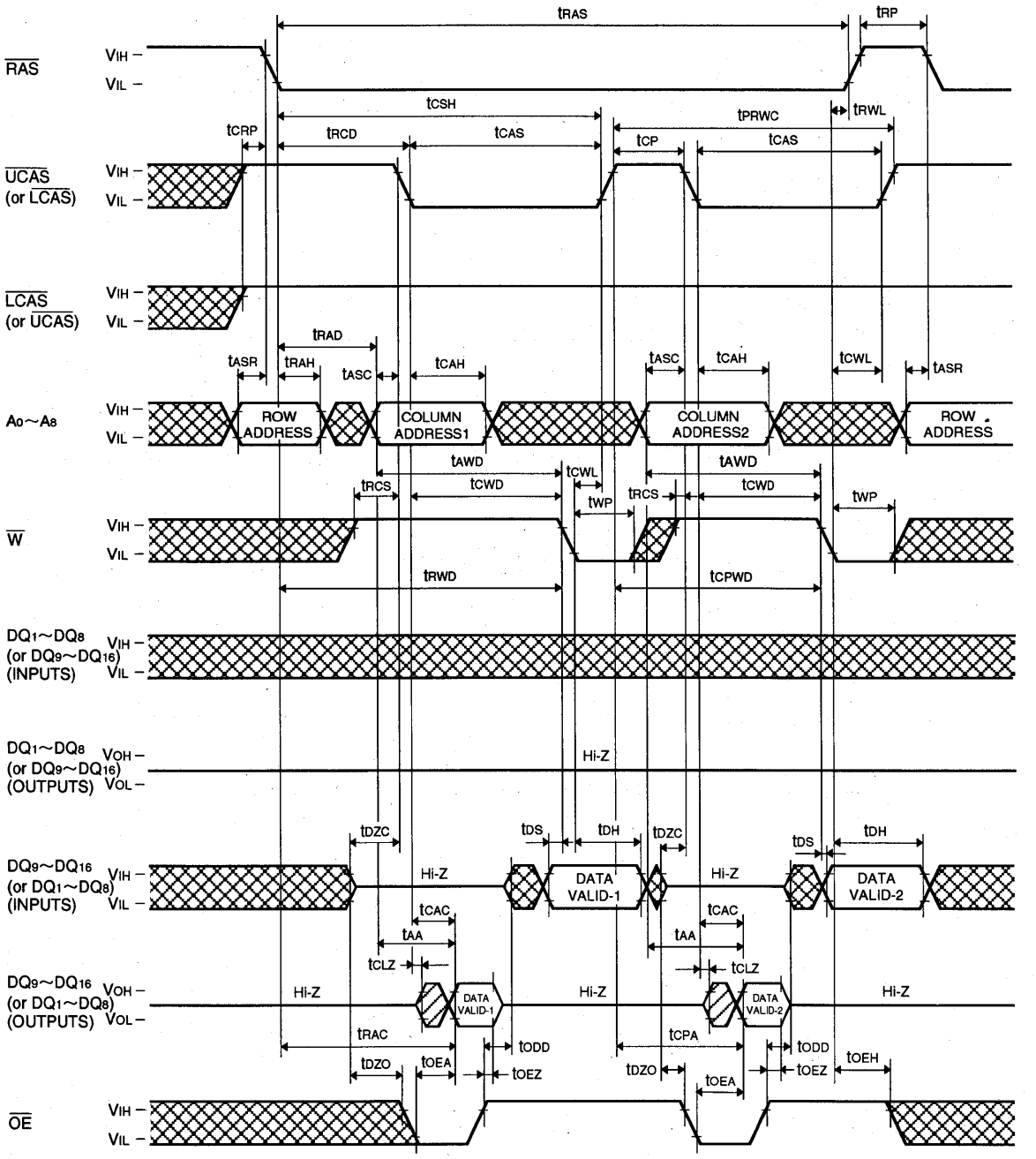


Fast Page Mode Read-Write, Read-Modify-Write Cycle

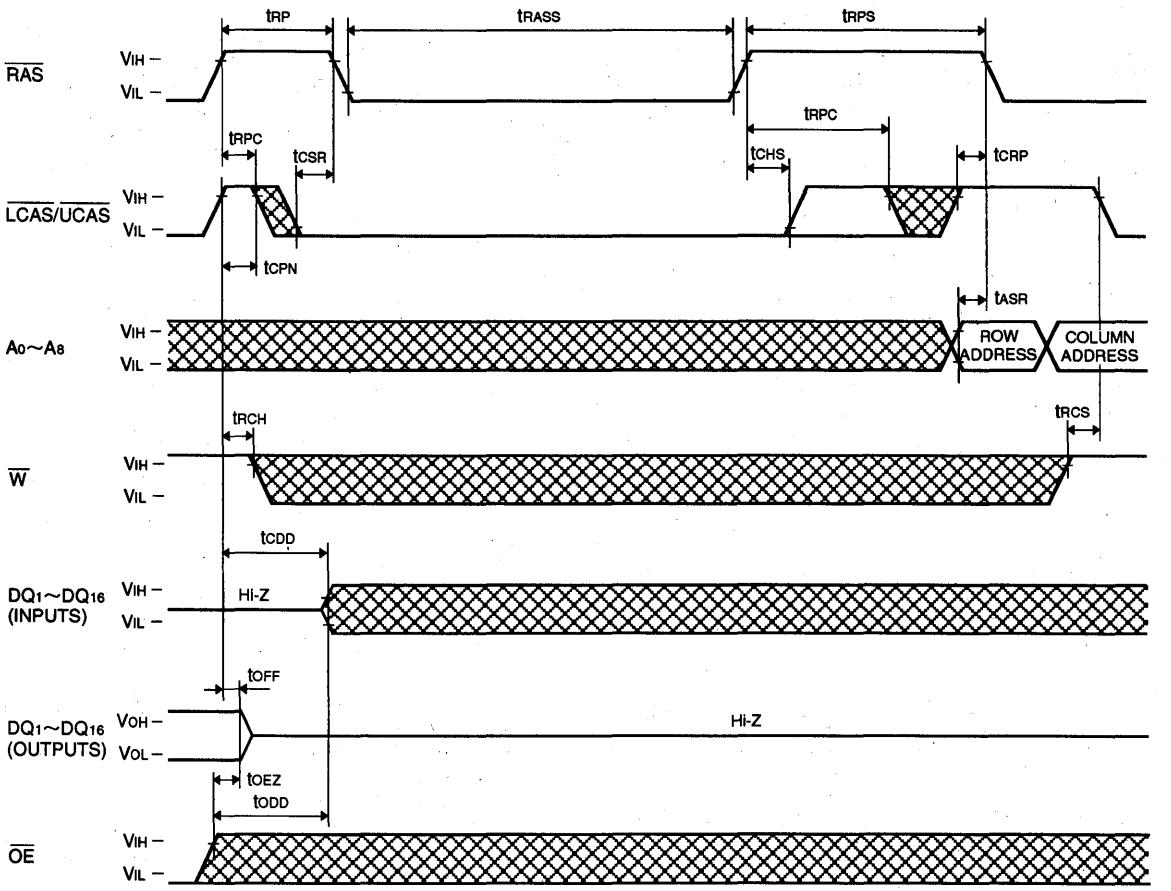


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Byte Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle * (Note28)



Note 28 : Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing Diagram

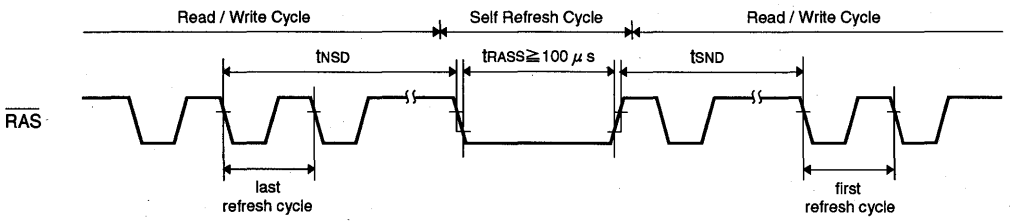
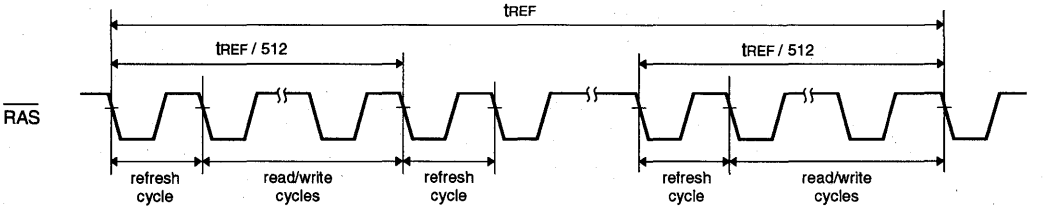


Table 2

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR distributed refresh	t_{NSD}≦250 μs	t_{SND}≦250 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≦16 μs	t_{SND}≦16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250 μs max.) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 8.2 ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

2. Burst refresh during Read/Write operation
(A) Timing diagram

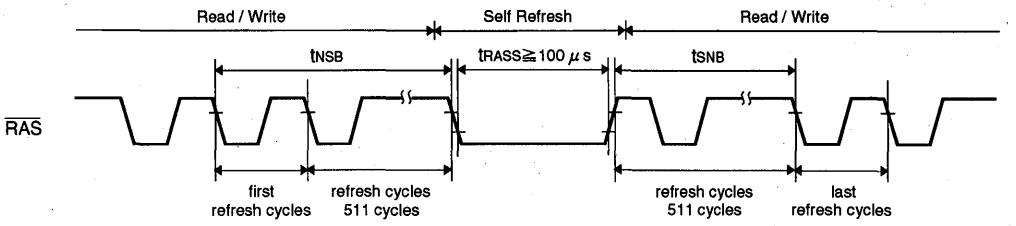
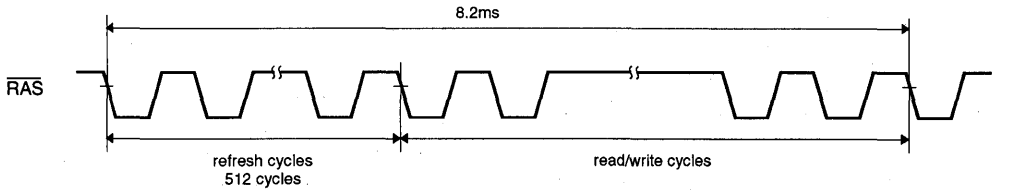


Table 3

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR burst refresh	tNSB≦8.2ms	tSNB≦8.2ms
RAS only burst refresh	tNSB+tSNB≦8.2ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of RAS only burst refresh

All combination of nine row address signals (A_0~A_8) are selected during 512 continuous RAS only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 RAS only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M5M4V4265CTP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs with Hyper page mode fuction, fabricated with the high performance CMOS process, and is ideal for the buffer memory systems of personal computer graphics and HDD where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4265CTP-6,-6S	60	15	30	15	110	333
M5M4V4265CTP-7,-7S	70	20	35	20	130	290

- Standard 44 pin TSOP (Ⅱ)
- Single 3.3±0.3V supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 1.8mW (Max)
  - CMOS Input level ---------- 360 μW (Max)*
- Operating power dissipation
  - M5M4V4265CTP-6,-6S ---------- 396mW (Max)
  - M5M4V4265CTP-7,-7S ---------- 342mW (Max)
- Self refresh capability*
  - Self refresh current ---------- 100 μA (Max)
- Extended refresh capability
  - Extended refresh current ---------- 100 μA (Max)
- Hyper-page mode (512-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 128ms (A_0~A_8)*
- Byte or word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

*: Applicable to self refresh version (M5M4V4265CTP-6S,-7S : option) only

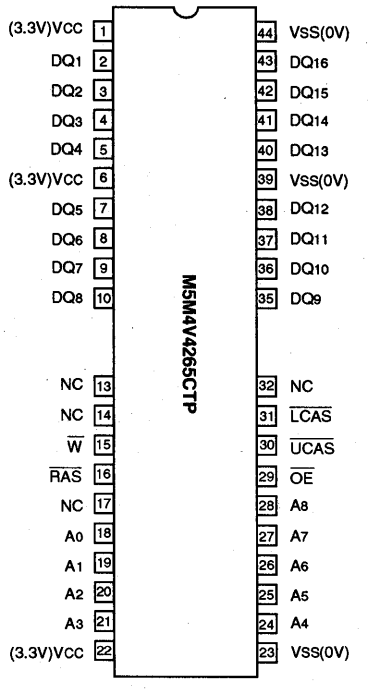
APPLICATION

Microcomputer memory, Refresh memory for CRT, Frame buffer memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_8	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+3.3V)
V_{SS}	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-L (400mil TSOP Nomal Bend)

NC: NO CONNECTION

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

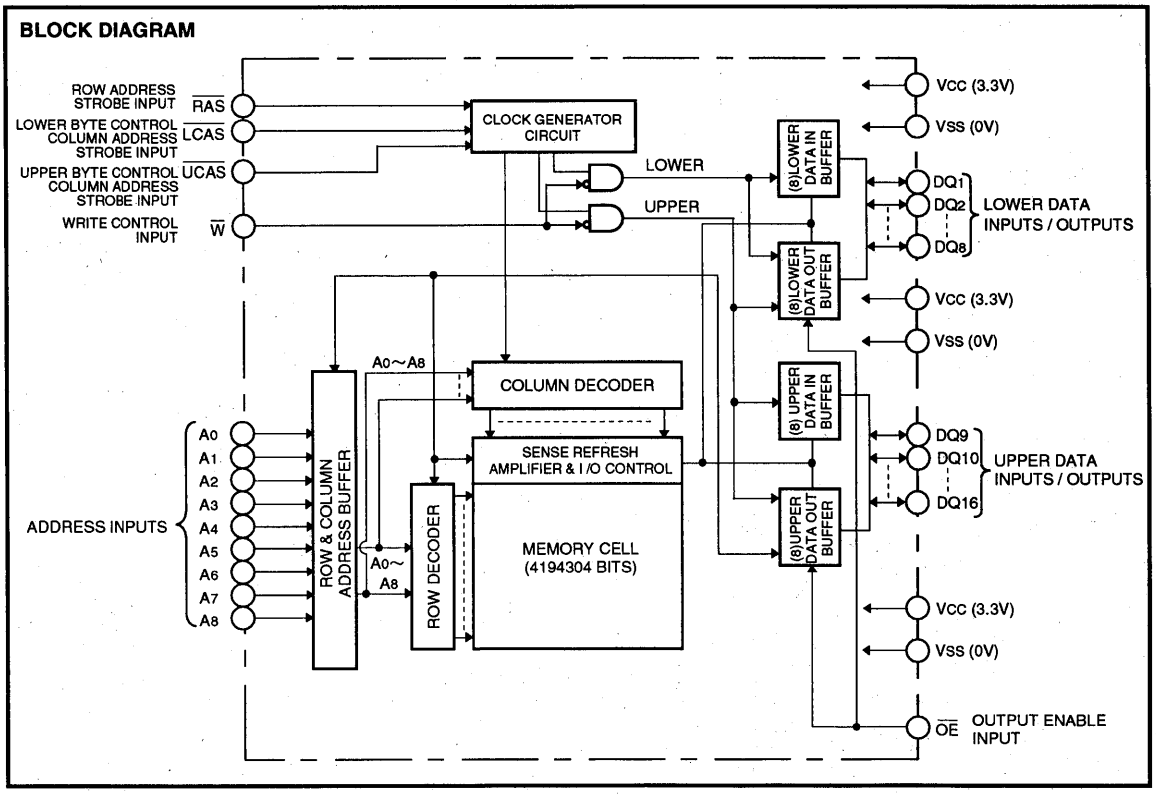
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M4V4265CTP provides a number of other functions, e.g., $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$ only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ (Extended *) refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Self refresh *	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5～4.6	V
V_I	Input voltage		-0.5～4.6	V
V_O	Output voltage		-0.5～4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70℃ , Vcc=3.3±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦Vcc	-5		5	μA
I_I	Input current		0V≦V_{IN}≦Vcc+0.3V, Other inputs pins=0V	-5		5	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V4265C-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M4V4265C-7,-7S				95	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V output open			0.5	
						0.1*	
$I_{CC3(AV)}$	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V4265C-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			110	mA
		M5M4V4265C-7,-7S				95	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper page mode (Note 3,4,5)	M5M4V4265C-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			110	mA
		M5M4V4265C-7,-7S				95	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V4265C-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			100	mA
		M5M4V4265C-7,-7S				85	
$I_{CC8(AV)}$*	Average supply current from Vcc Extended-refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0～A_8 ≦ 0.2V or ≧Vcc-0.2V, DQ=open t_{RC}=250 μs, t_{RAS}=$t_{RAS\ min}$～1 μs			100	μA
$I_{CC9(AV)}$*	Average supply current from Vcc Self-refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			100	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAPACITANCE (Ta=0～70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0～70 ℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		33		38	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$	(Note 13)	5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		15		20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high	(Note 12)		15		20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)		15		20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)		15		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).
Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 50pF, V_{OH}(I_{OH}=-2mA) and V_{OL}(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).
8: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.
9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq \pm 5$ μA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.
13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0～70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	
t_{REF}	Refresh cycle time		8.2		8.2	ms
t_{REF}	Refresh cycle time *		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 16)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 17)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 18)	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	10		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note 19)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note 19)	0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data (Note 20)	15		20		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note 20)	15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note 20)	15		20		ns
t_T	Transition time (Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 22)	0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	18		23		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
			Min	Max	Min	Max	
tWC	Write cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		10	10000	10	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		10		13		ns
tWP	Write pulse width		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
			Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	133		161		ns
tRAS	$\overline{RAS}$ low pulse width		89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧ tCPWD(min) (for Hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V IH) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

EDO (HYPER PAGE MODE) 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	25		30		ns
tHPRWC	Hyper page mode read write/read modify write cycle time	66		79		ns
tDOH	Output hold time from $\overline{CAS}$ low	5		5		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note 28)	10	16	10	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		ns
tOEPE	$\overline{OE}$ pulse width (Hi-Z control)	7		7		ns
tWPE	$\overline{W}$ pulse width (Hi-Z control)	7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	50		60		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	15		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: tHPC(min) is specified in the case of read-only and early write-only in Hyper page mode.
27: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
28: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

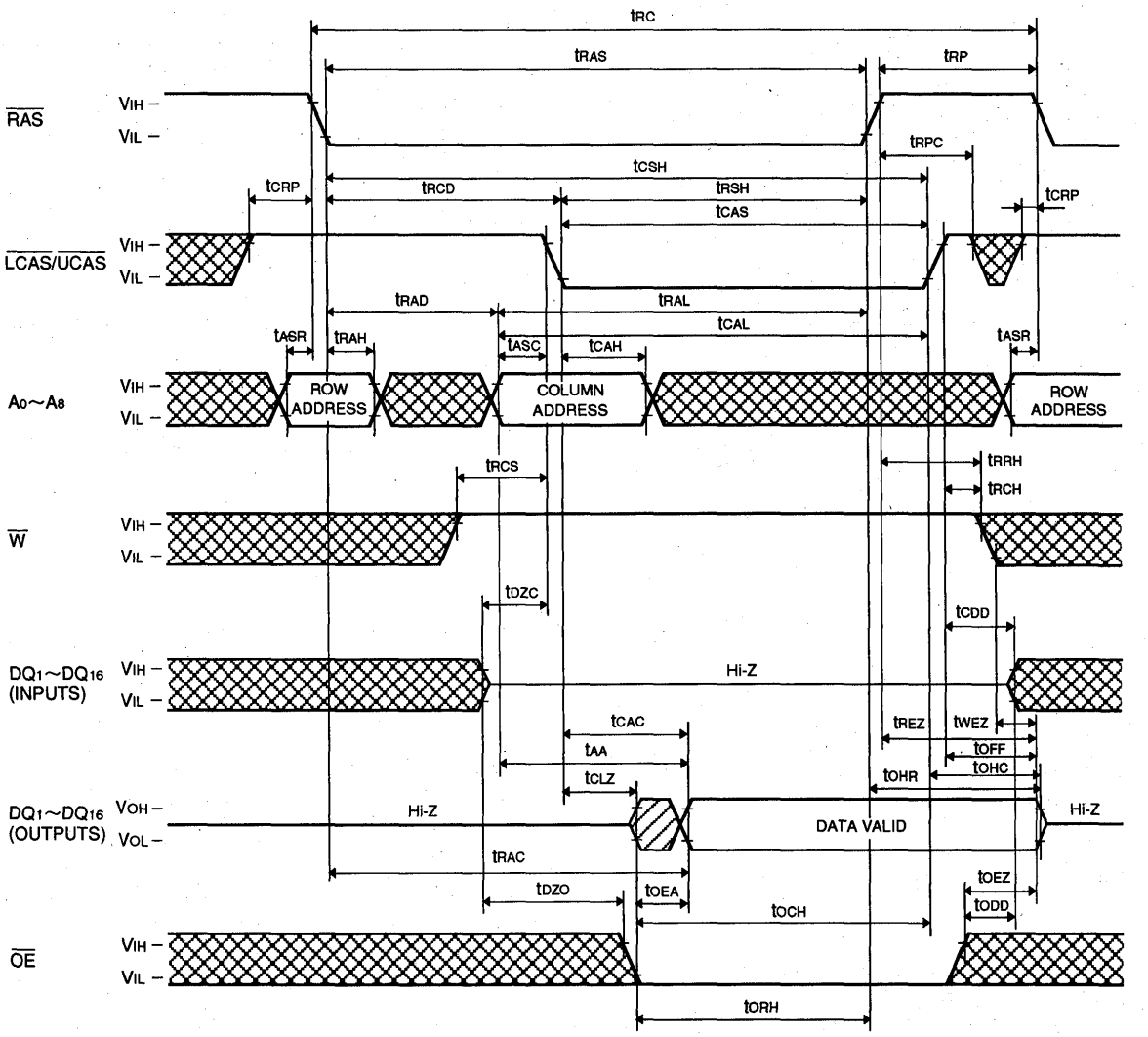
Symbol	Parameter	Limits				Unit
		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
tCAS	$\overline{CAS}$ low pulse width	17		22		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle * (Note 30)

Symbol	Parameter	Limits				Unit
		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	
tRASS	CBR self refresh $\overline{RAS}$ low pulse width	100		100		μs
tRPS	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
tCHS	CBR self refresh $\overline{CAS}$ hold time	-50		-50		ns

Timing Diagrams (Note 31)
Read Cycle



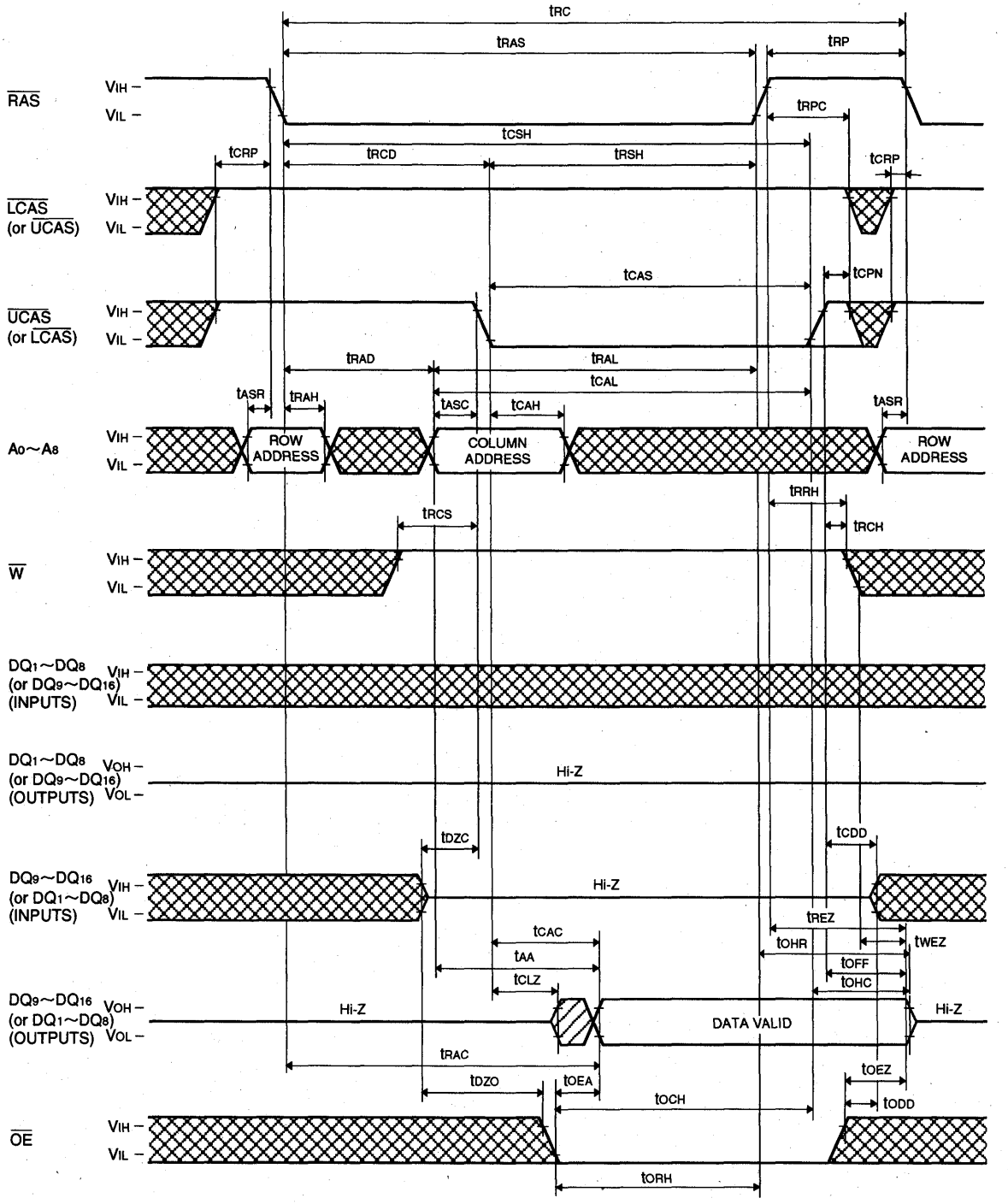
Note 31

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

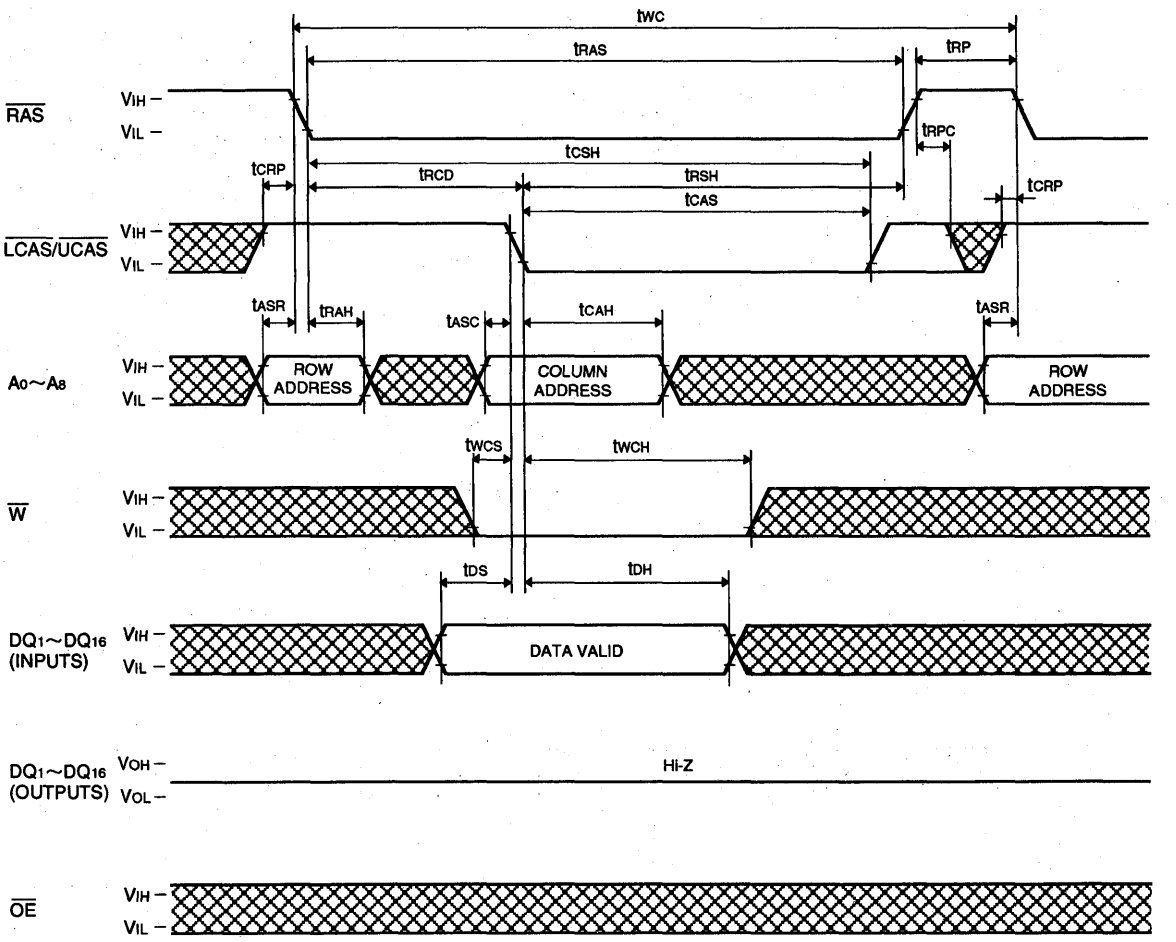
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Read Cycle

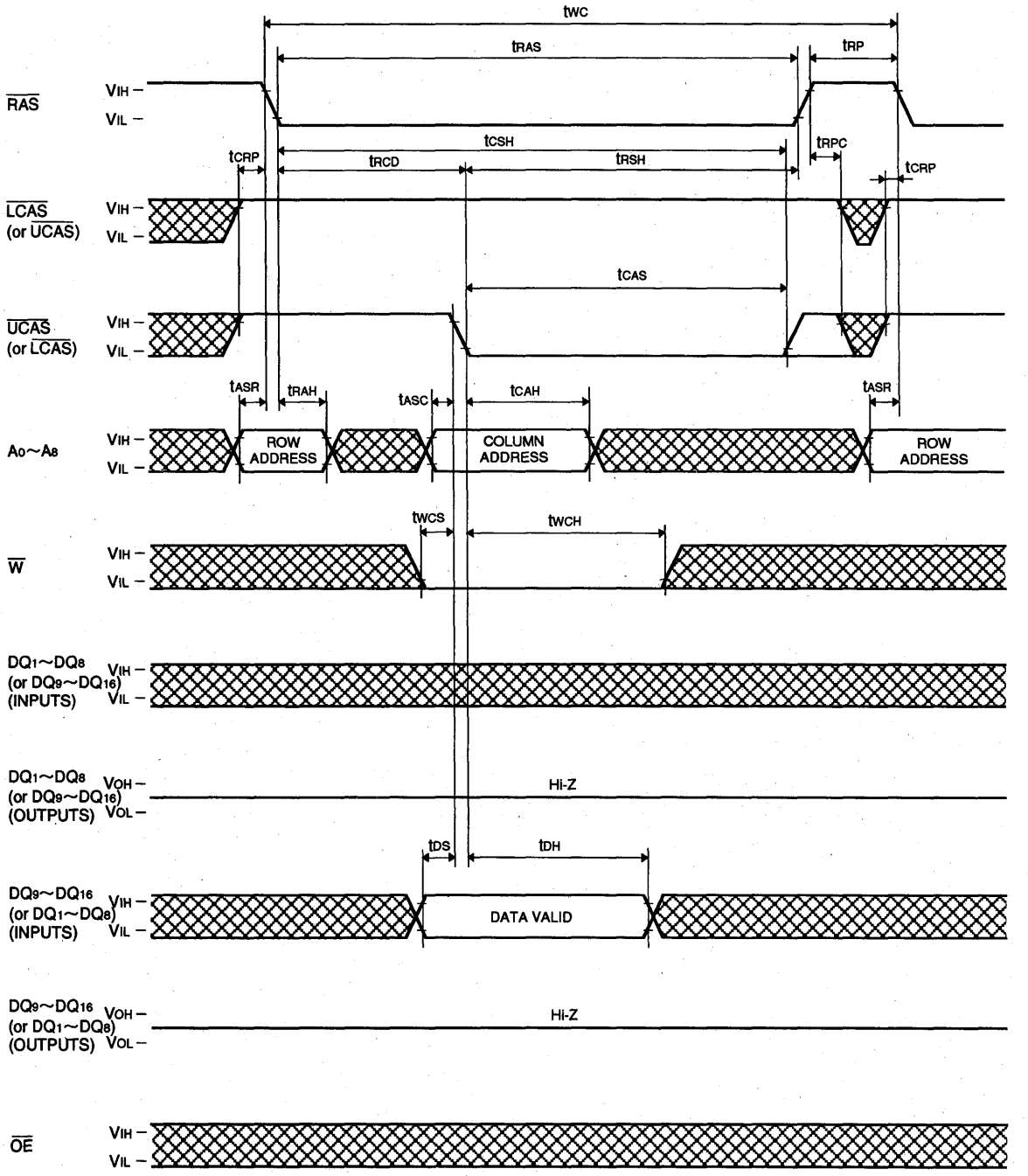


Early Write Cycle

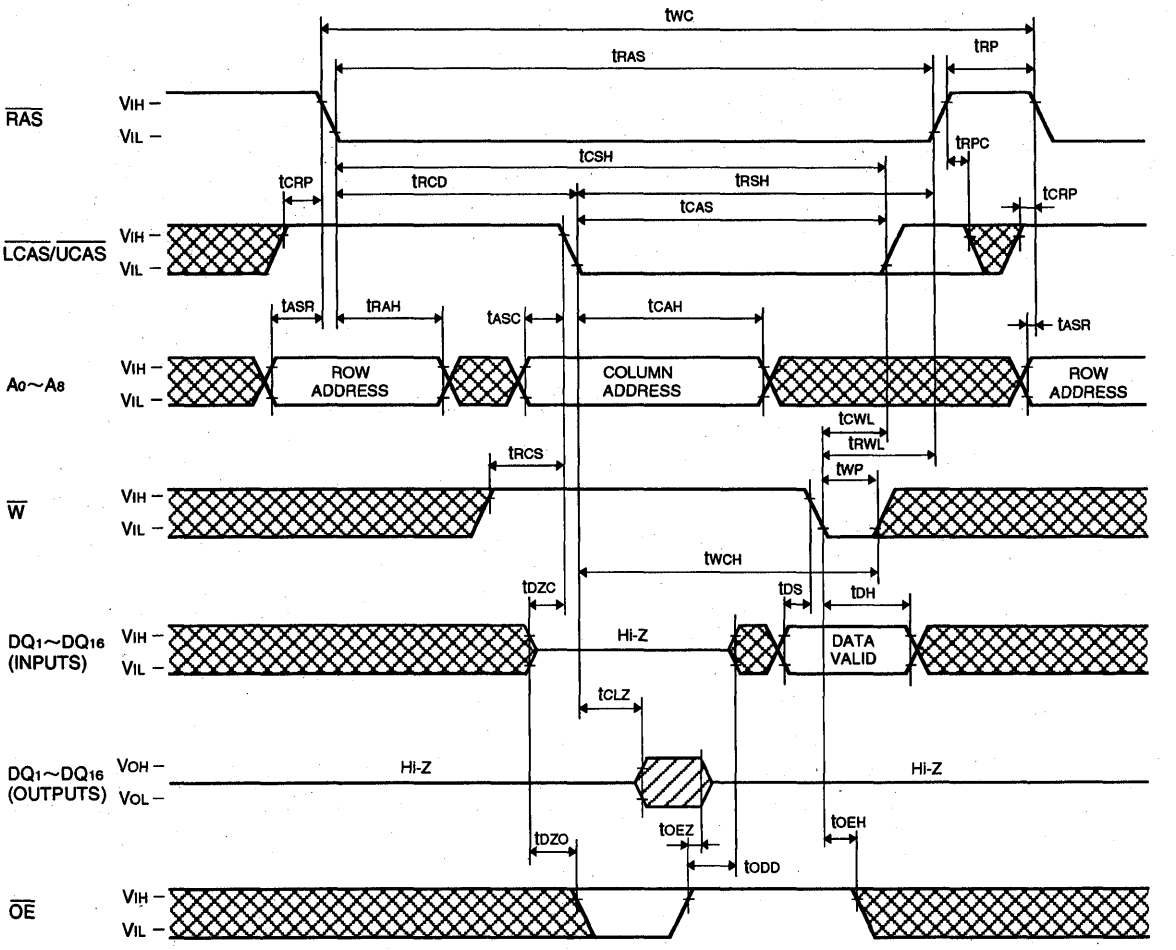


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

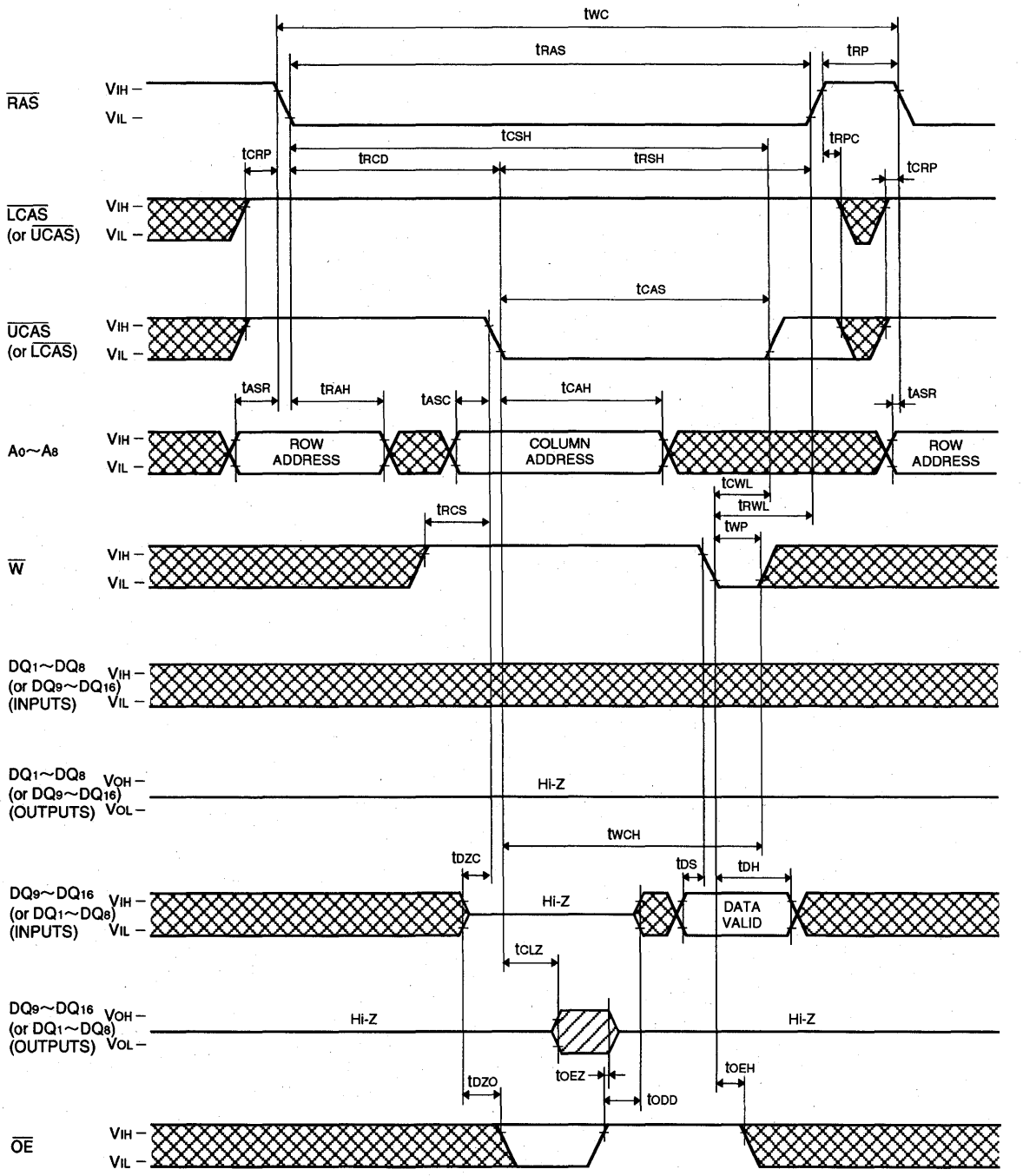
Byte Early Write Cycle



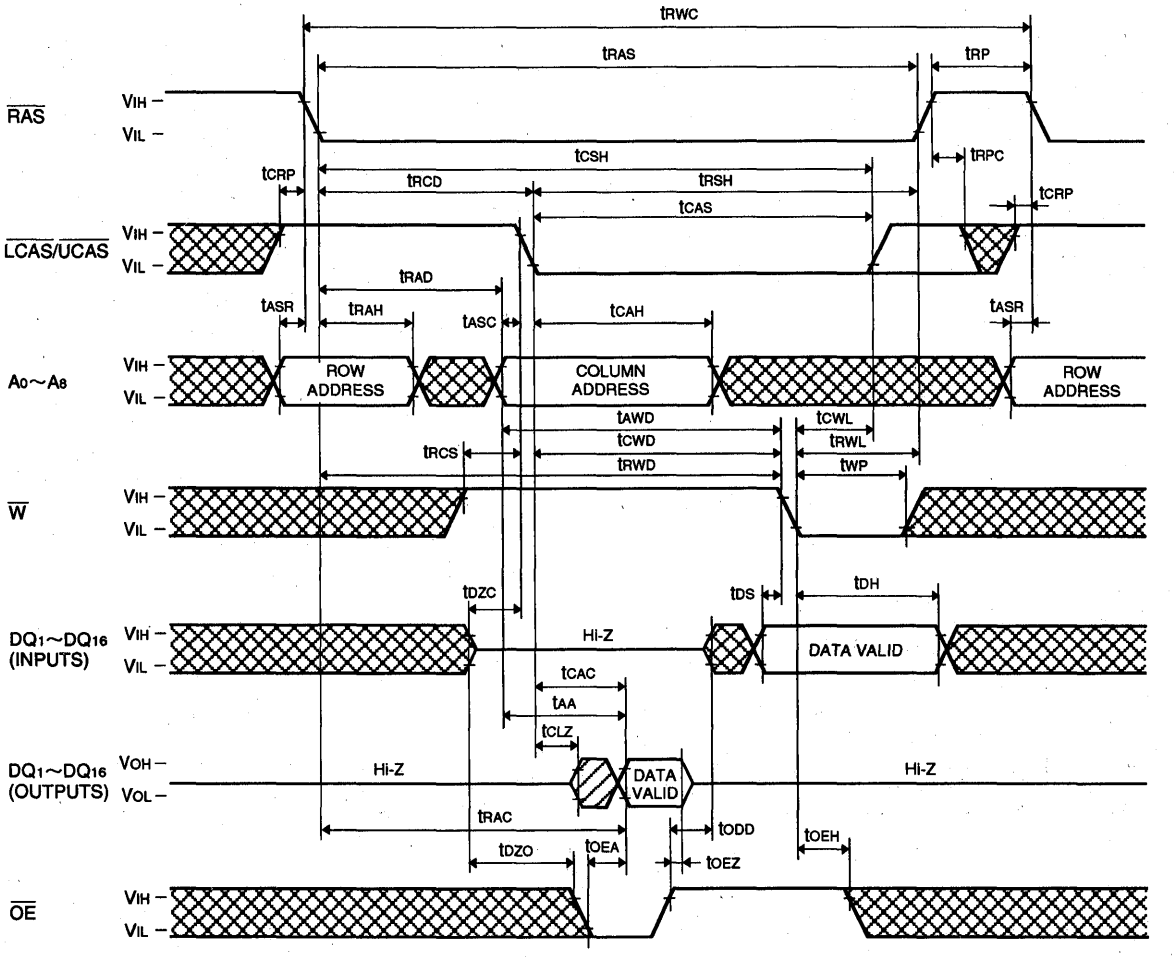
Delayed Write Cycle



Byte Delayed Write Cycle

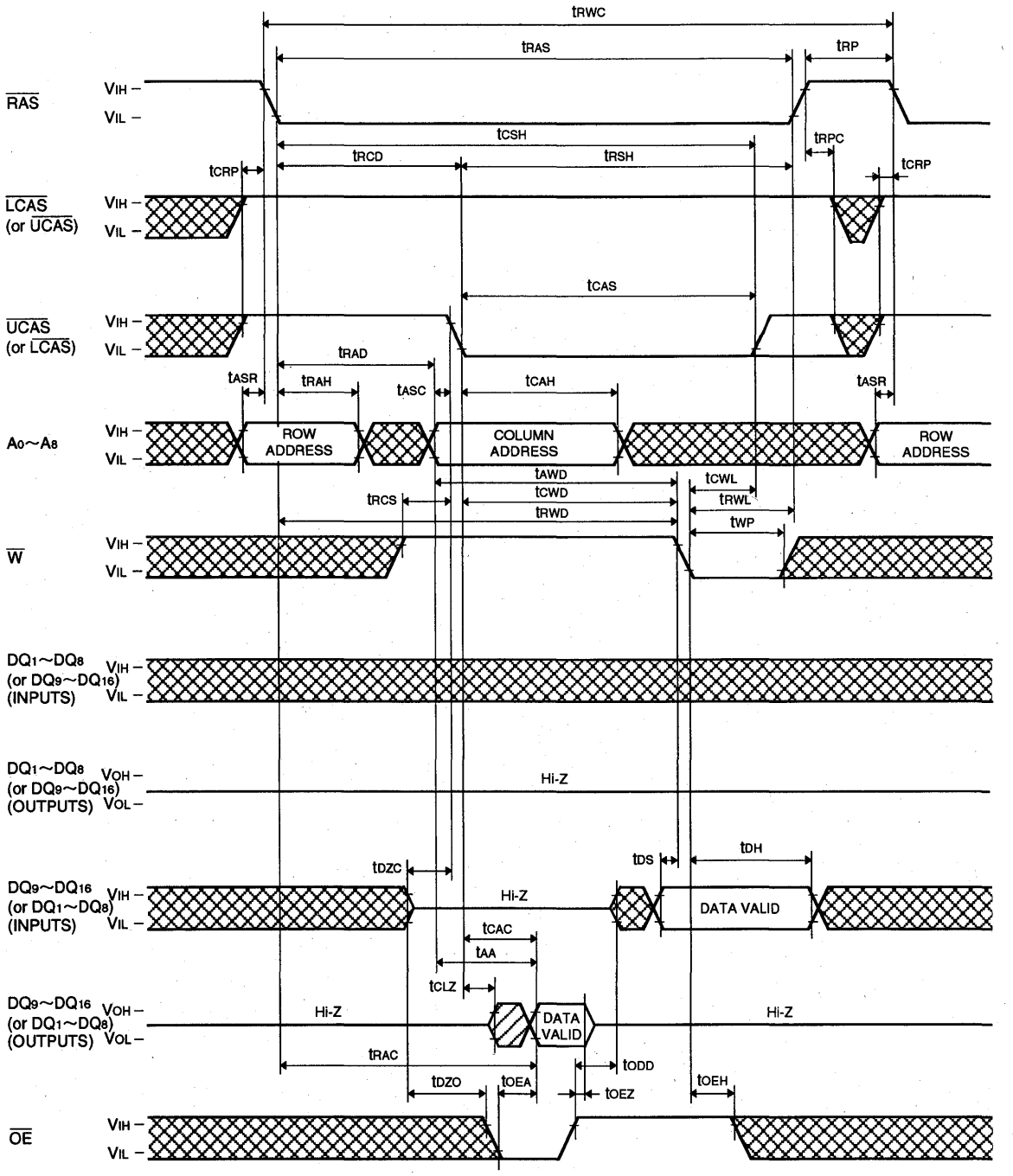


Read-Write, Read-Modify-Write Cycle

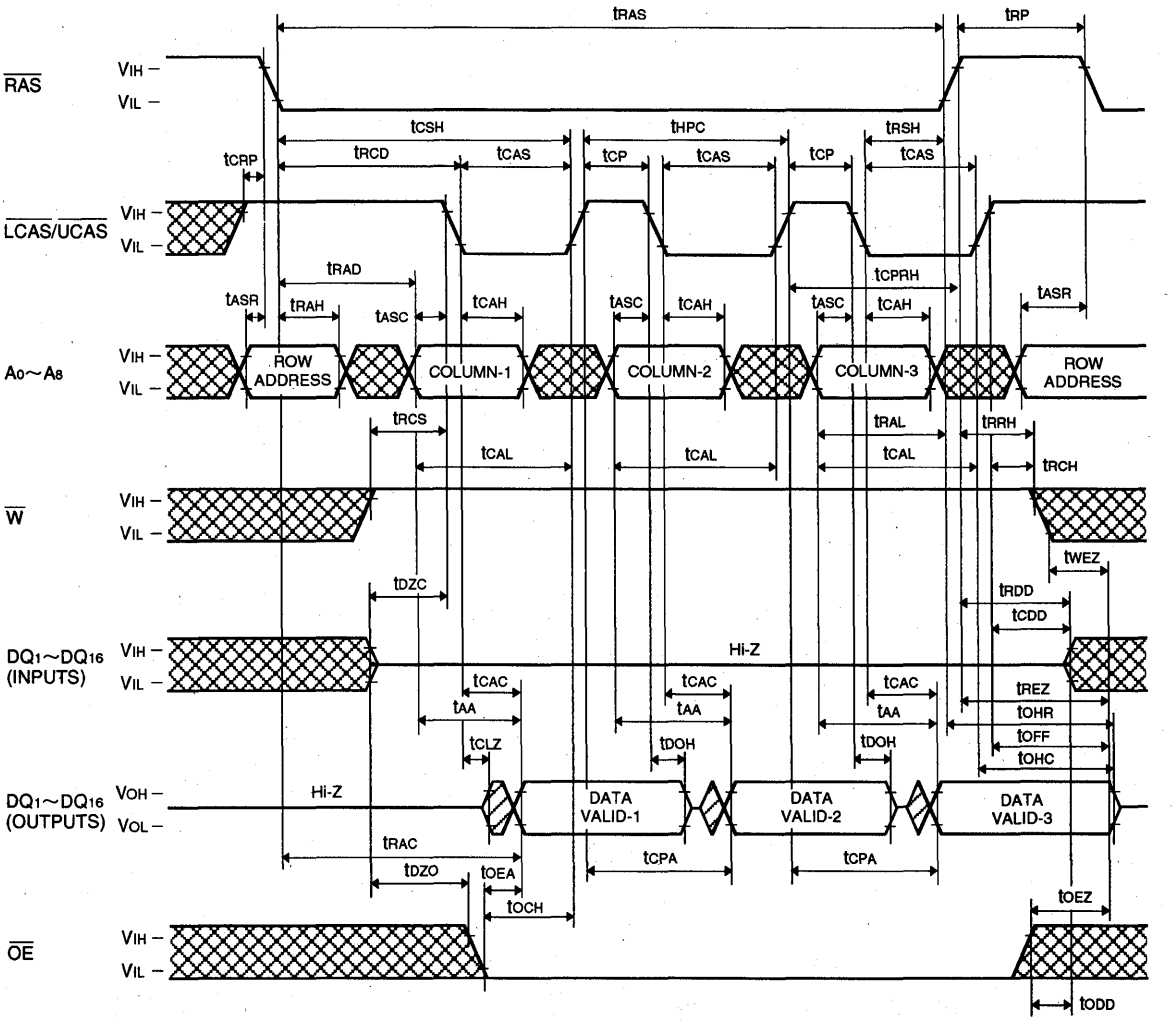


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Read-Write, Read-Modify-Write Cycle

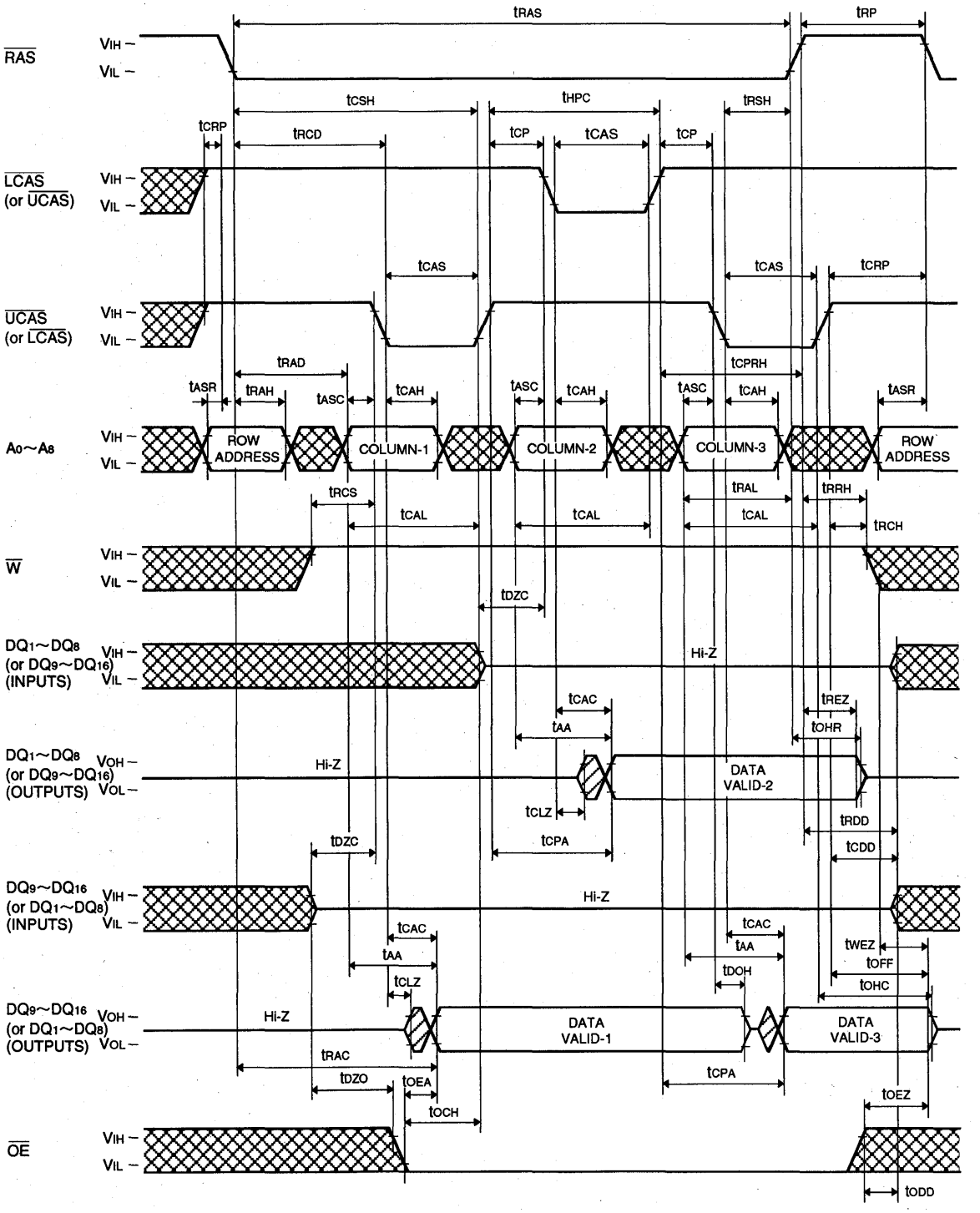


Hyper Page Mode Read Cycle

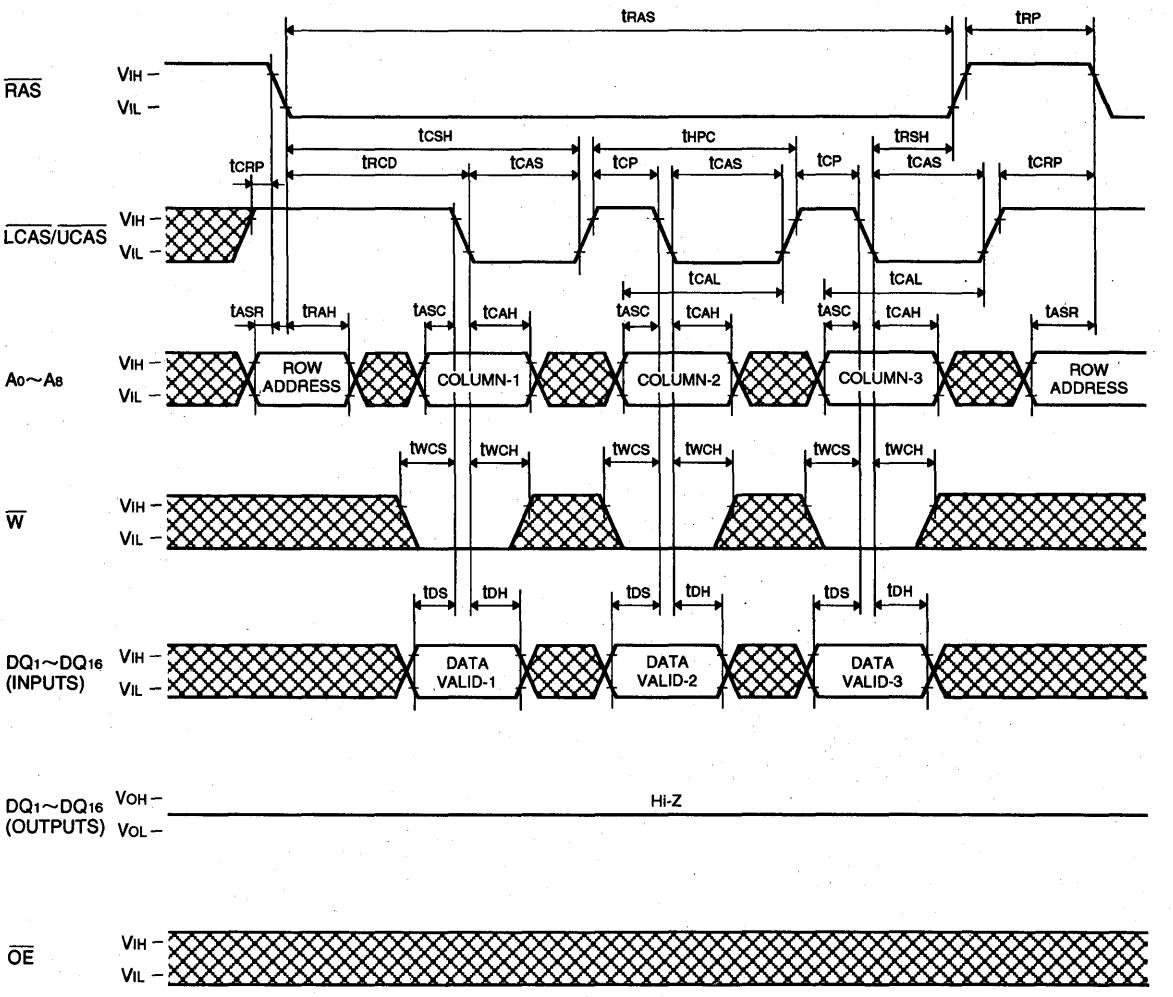


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Read Cycle

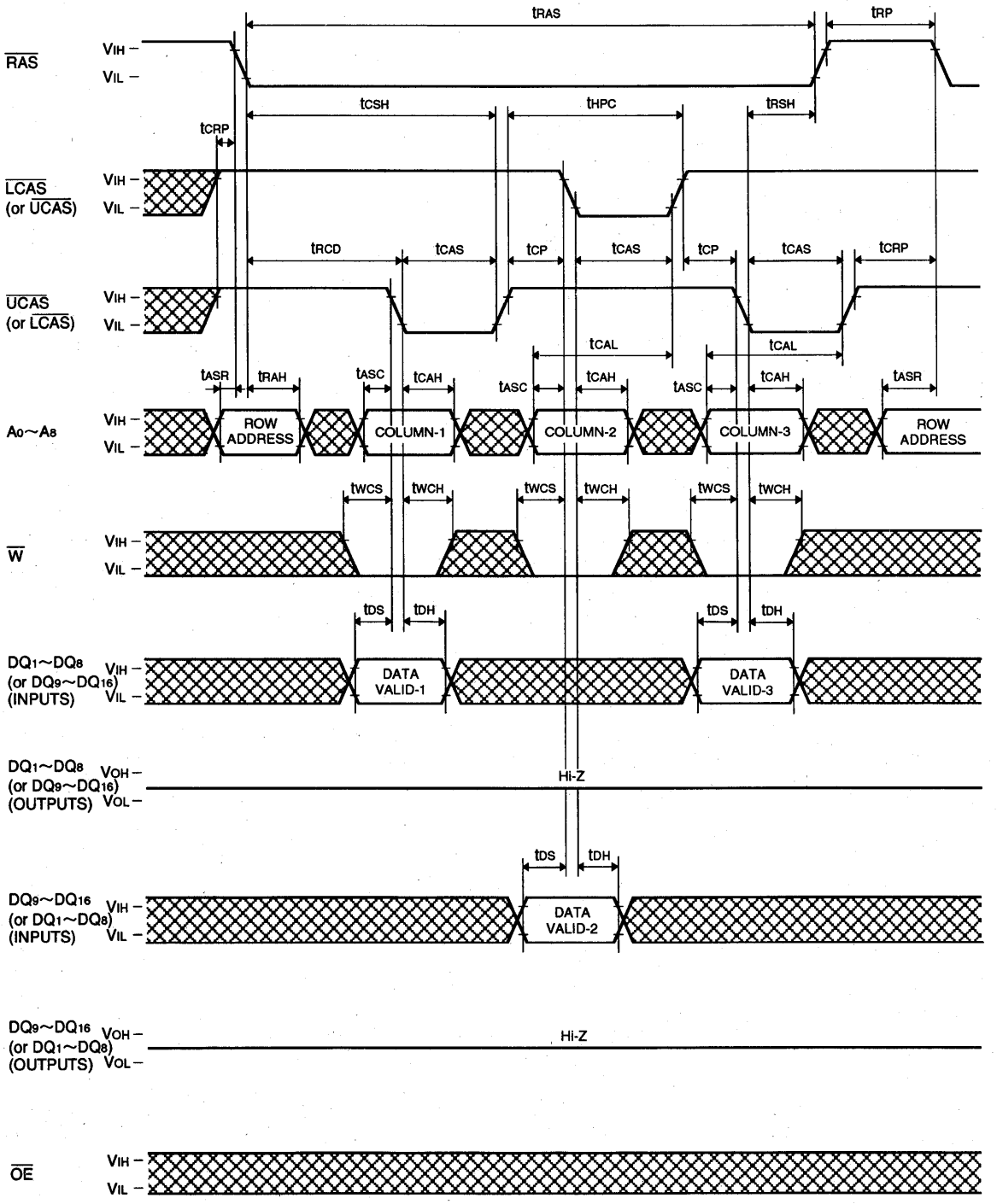


Hyper Page Mode Early Write Cycle

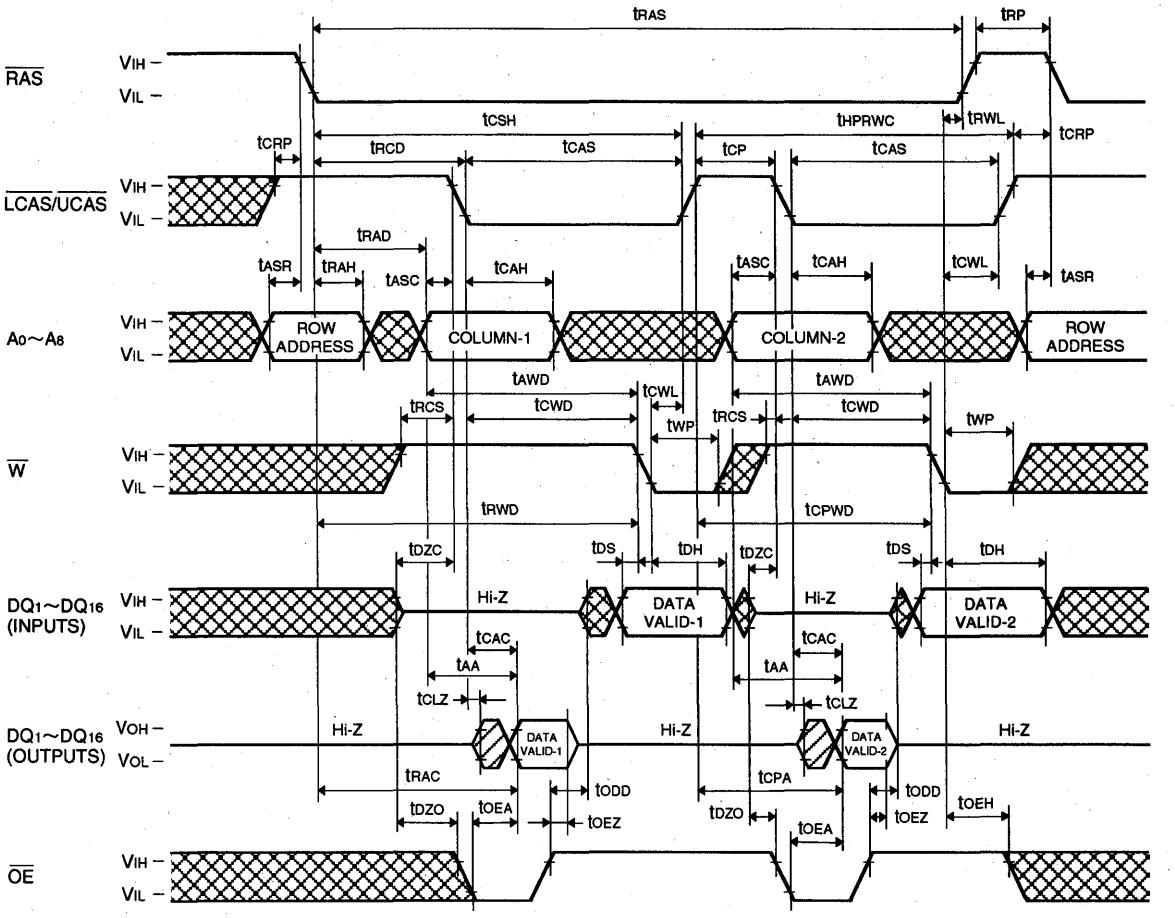


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Early Write Cycle

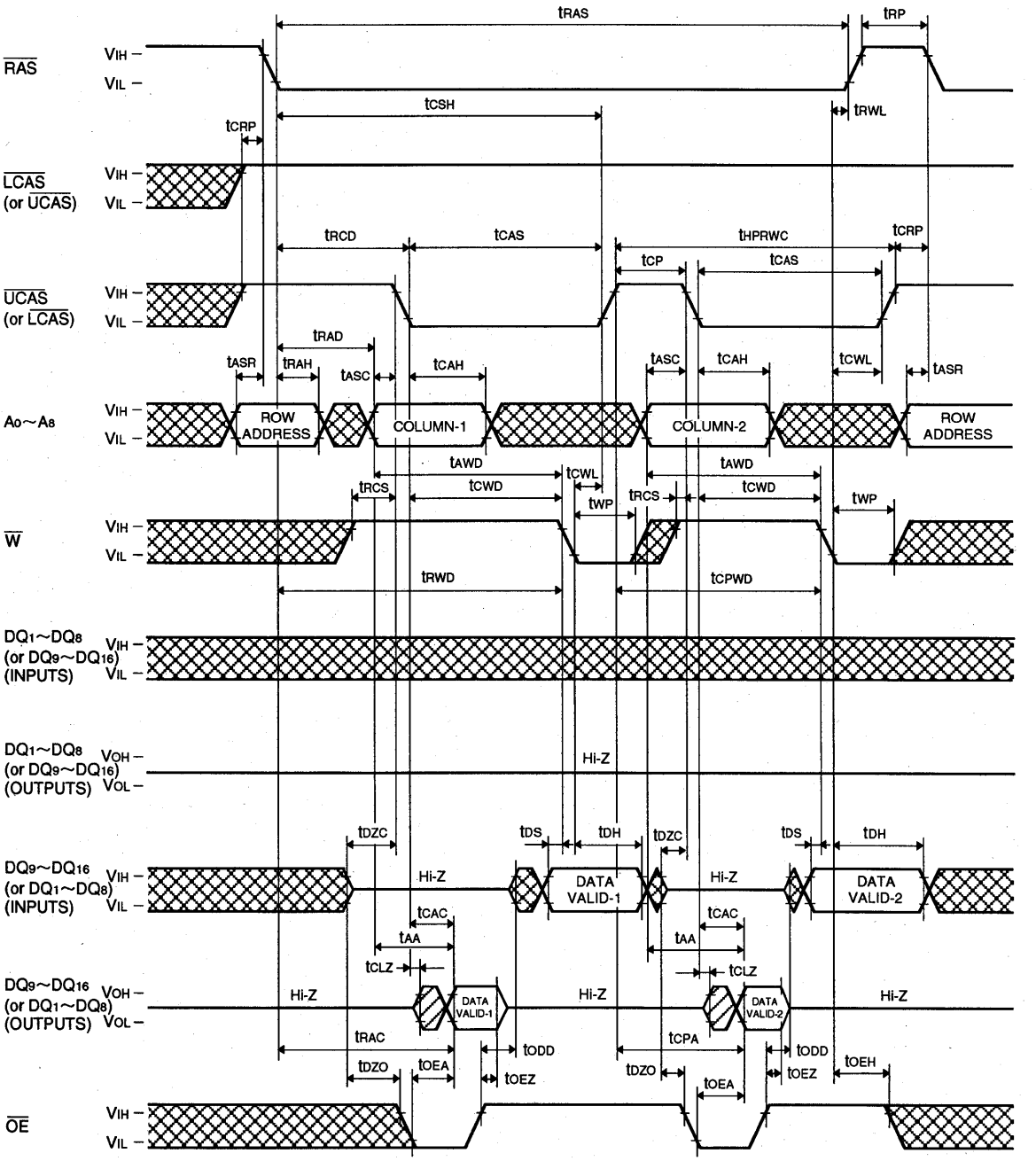


Hyper Page Mode Read-Write, Read-Modify-Write Cycle

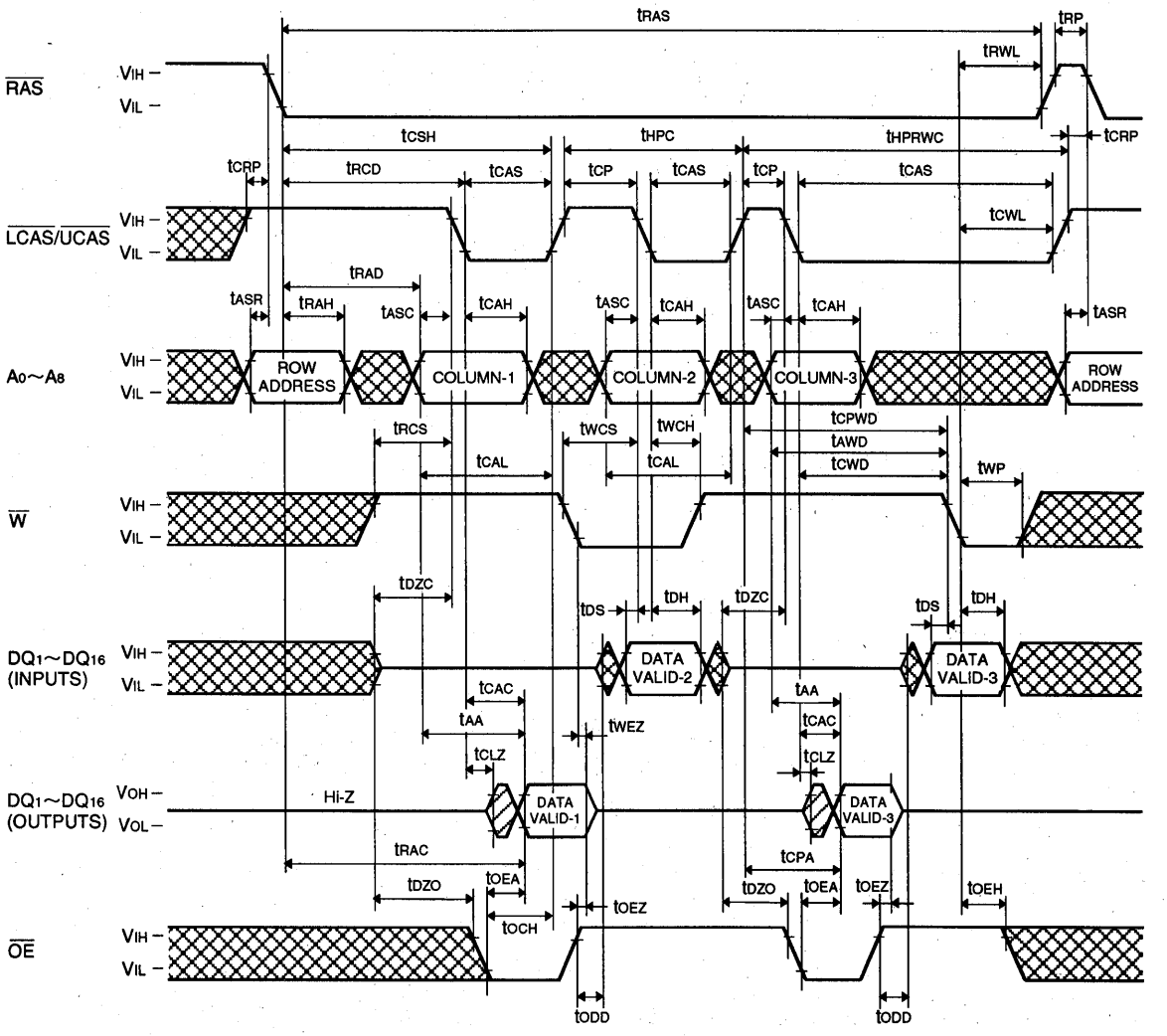


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

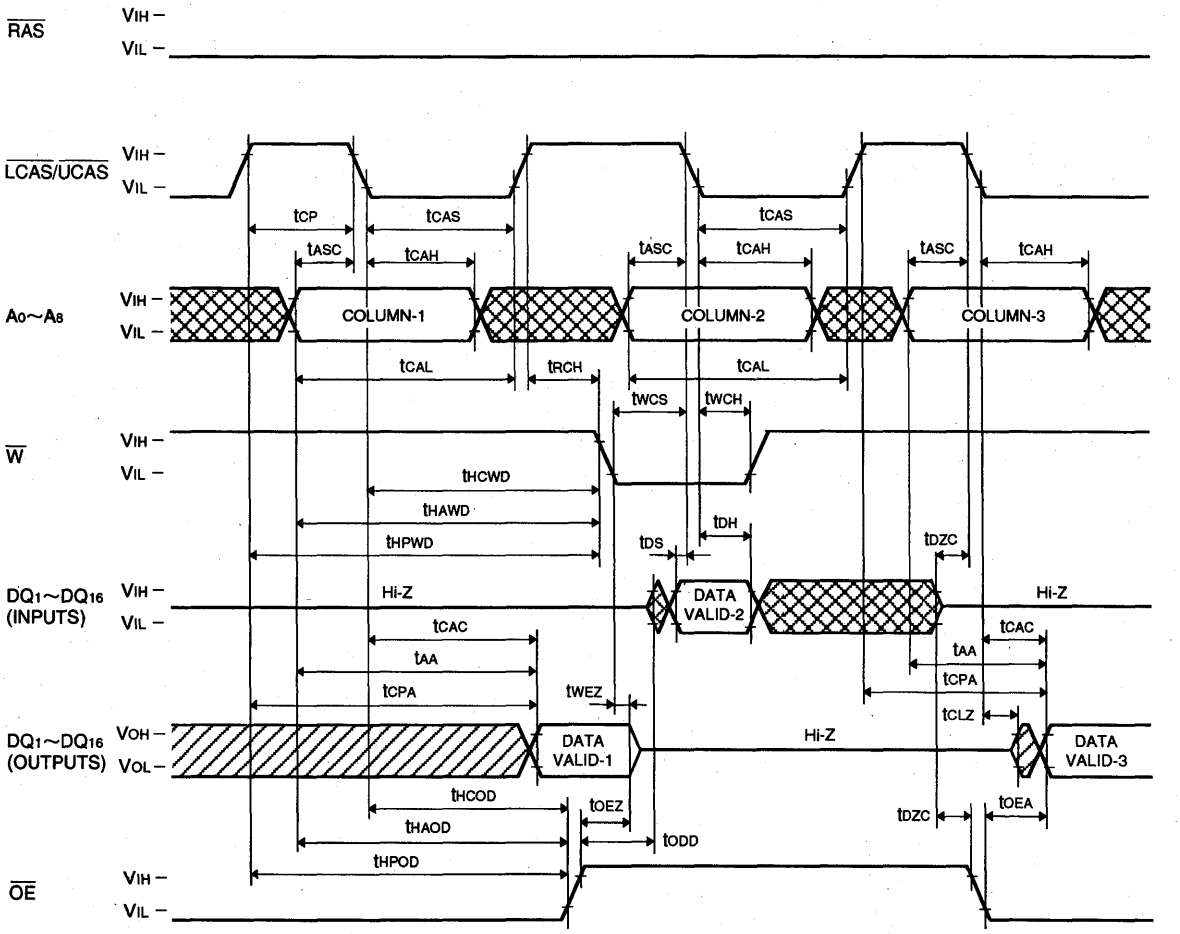
Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



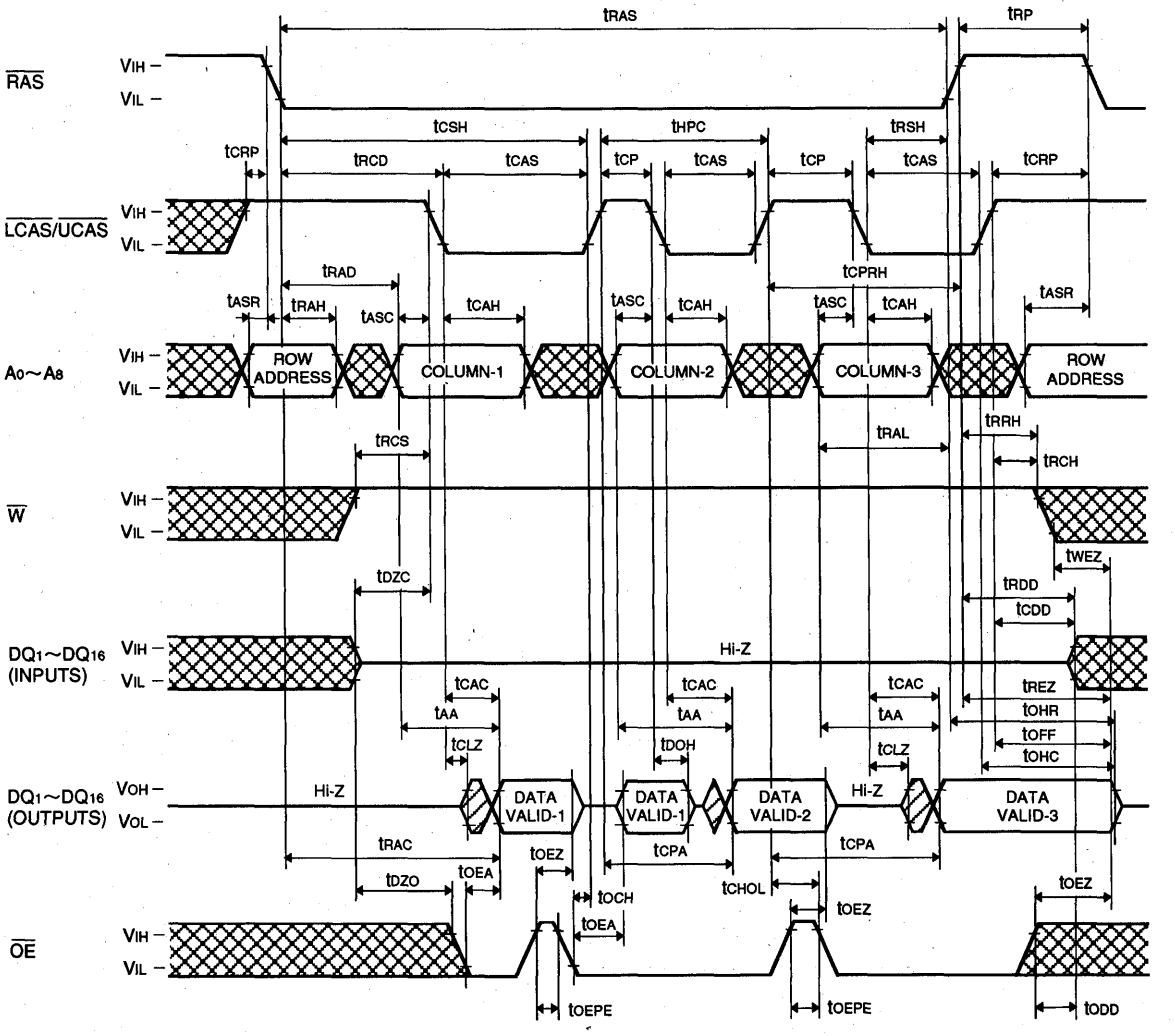
Hyper Page Mode Mix Cycle (1)



Hyper Page Mode Mix Cycle (2)

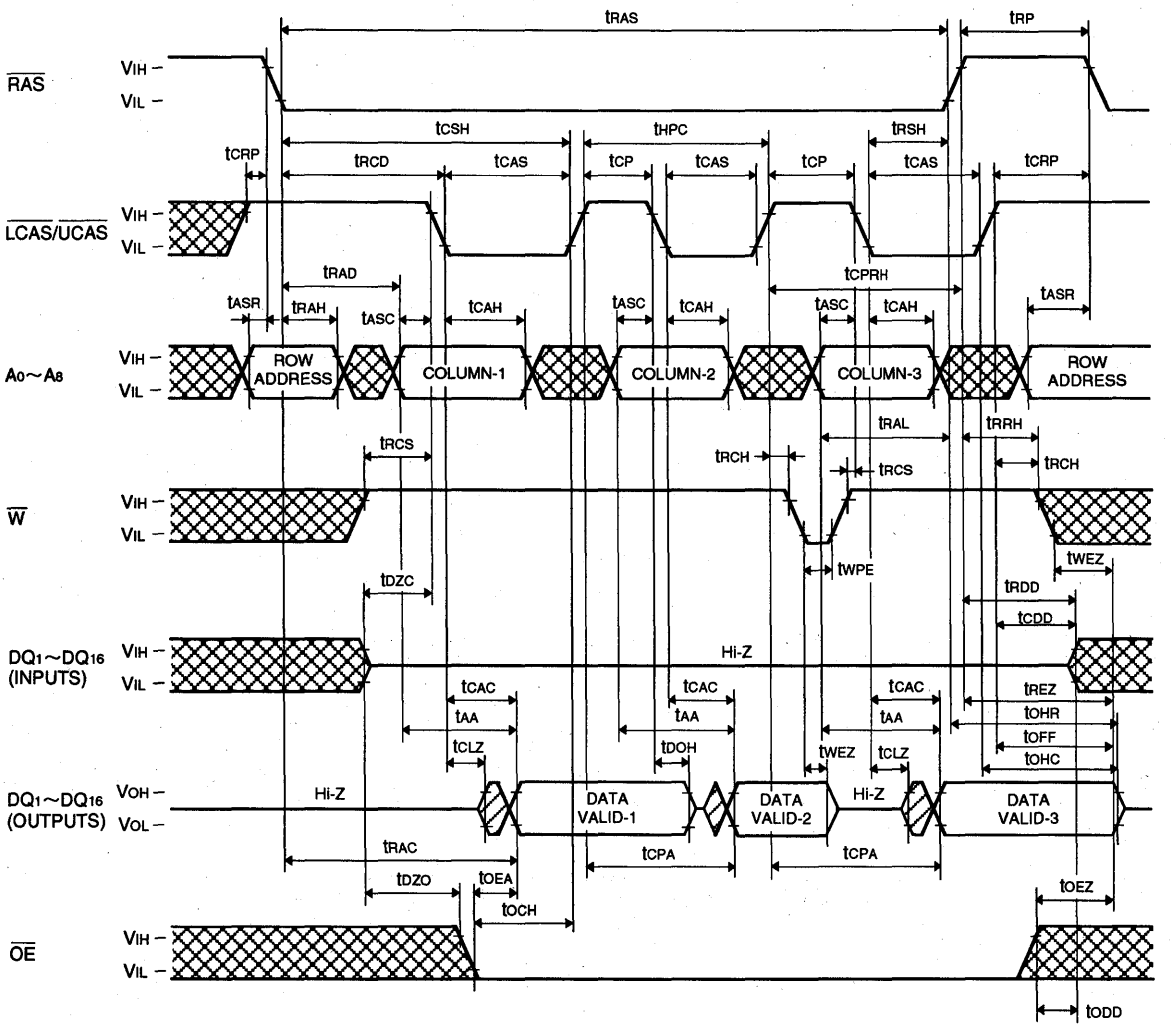


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



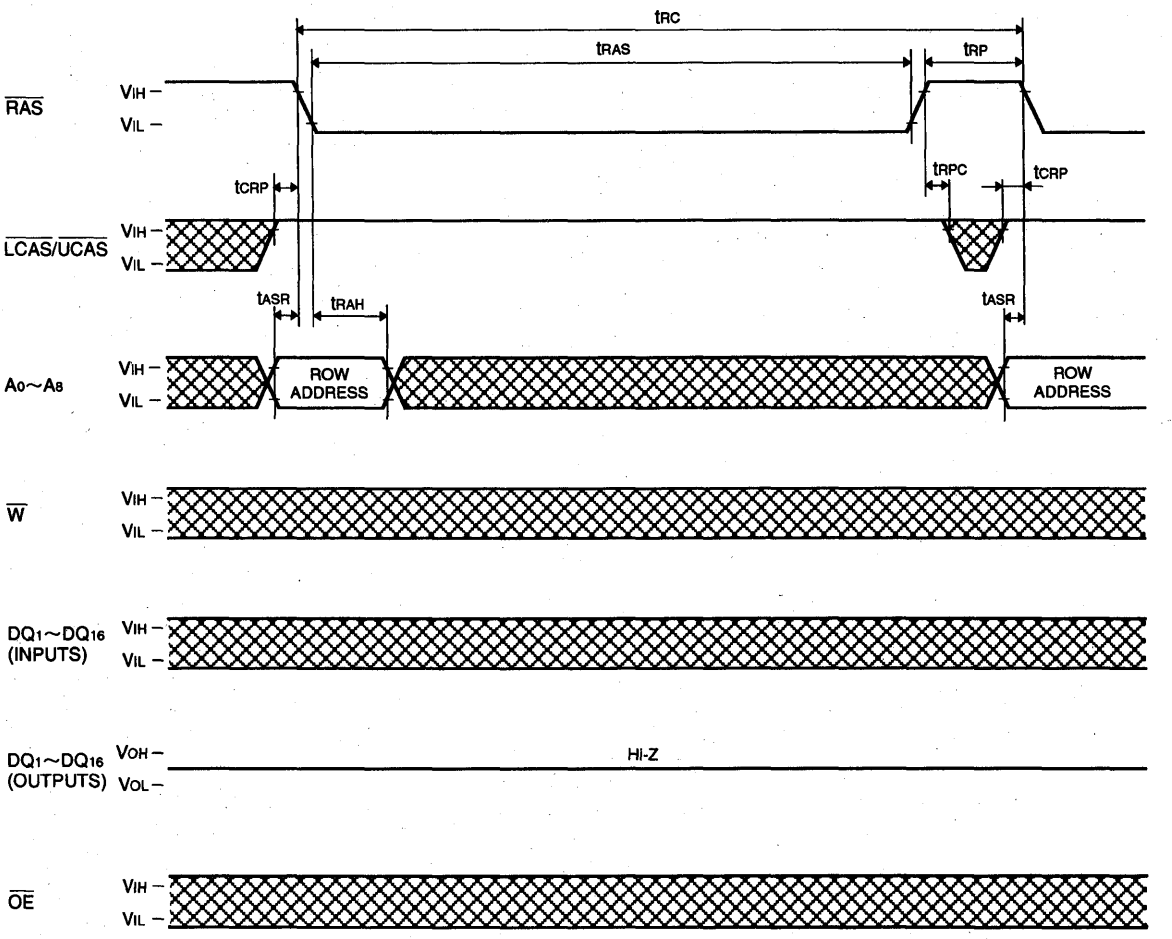
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

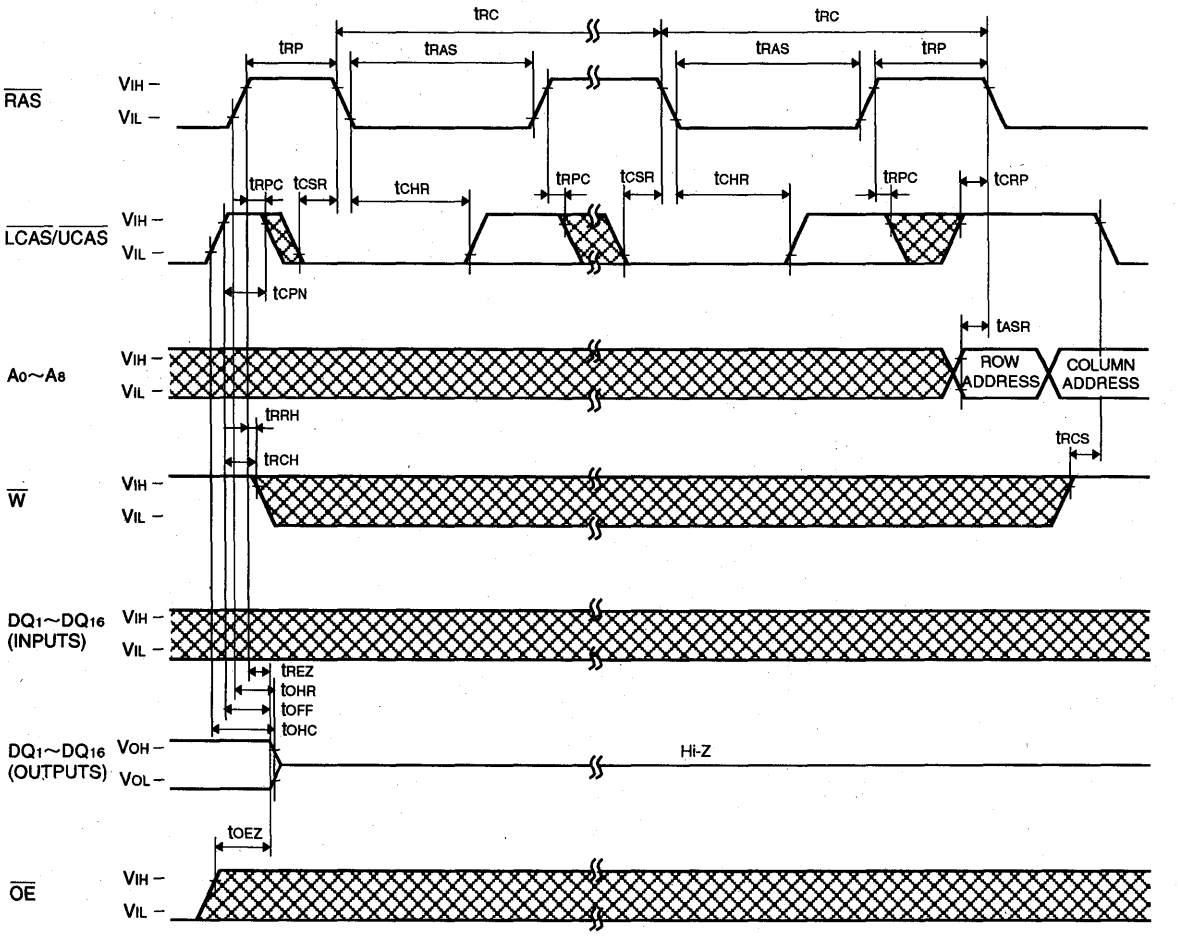


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle

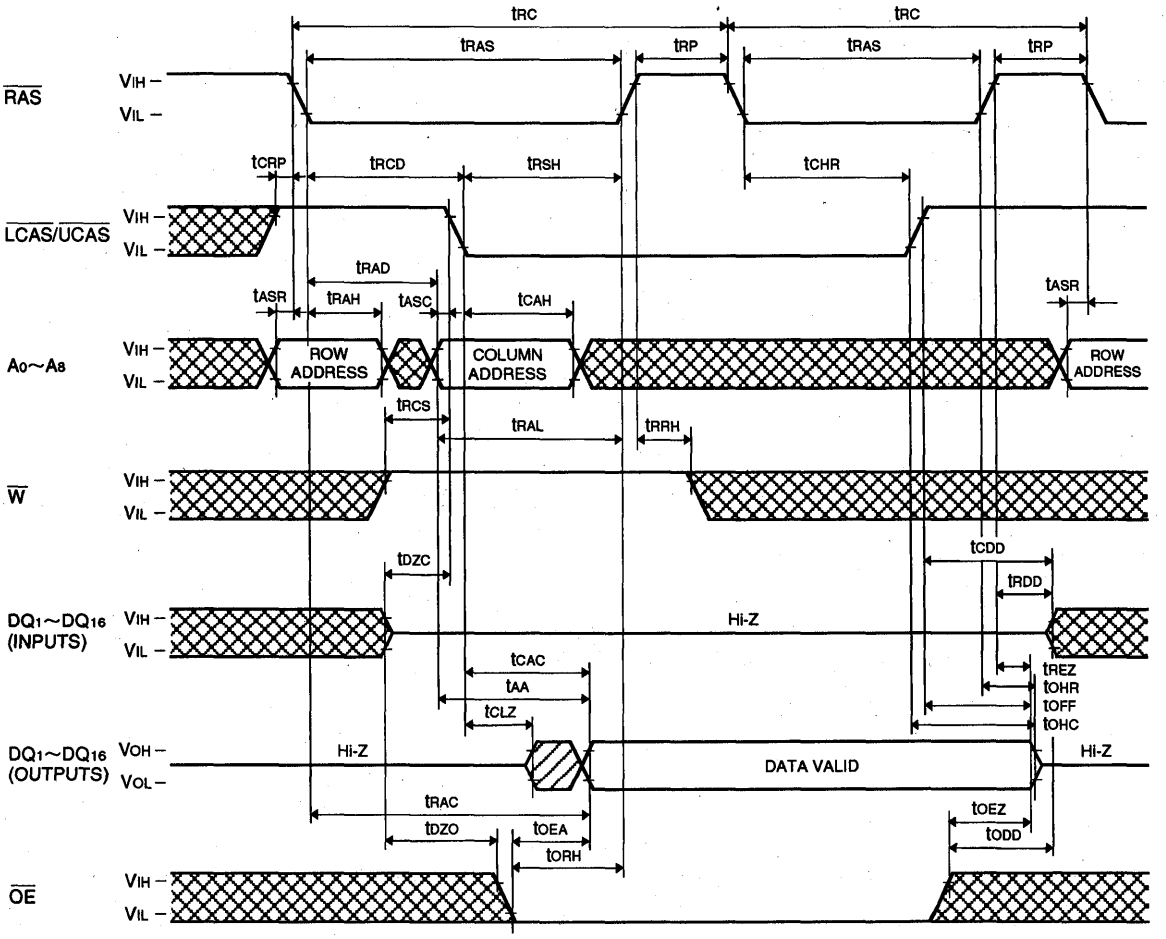


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



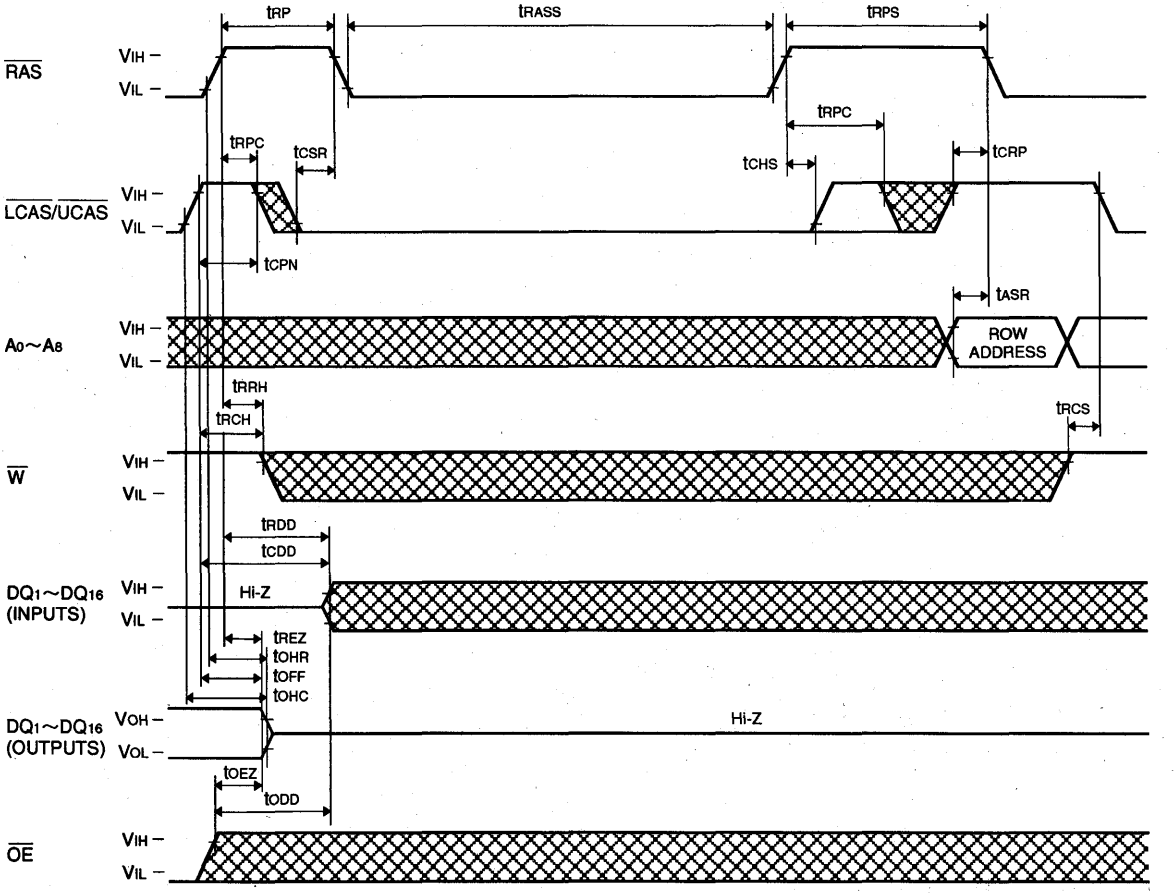
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hidden Refresh Cycle (Read) (Note 32)



Note 32: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle * (Note 30)



Note 30 : Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read/Write operation
(A) Timing Diagram

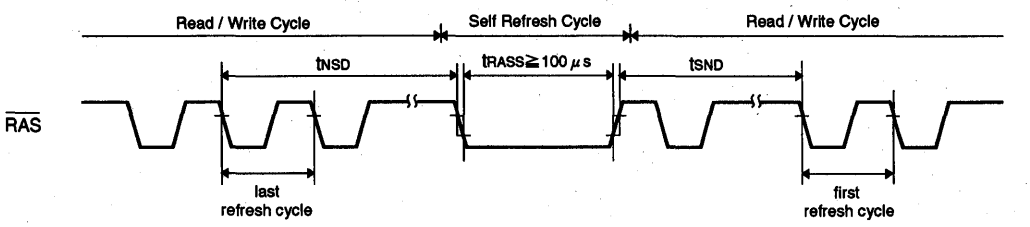
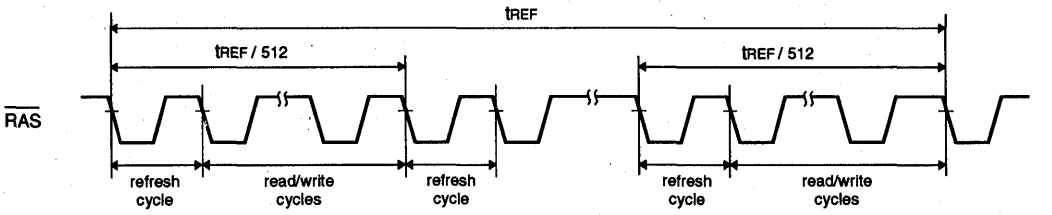


Table 2

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR distributed refresh	t_{NSD}≦250 μs	t_{SND}≦250 μs
$\overline{RAS}$ only distributed refresh	t_{NSD}≦16 μs	t_{SND}≦16 μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250 μs max.) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_8) are selected during 512 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 8.2 ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

2. Burst refresh during Read/Write operation
(A) Timing diagram

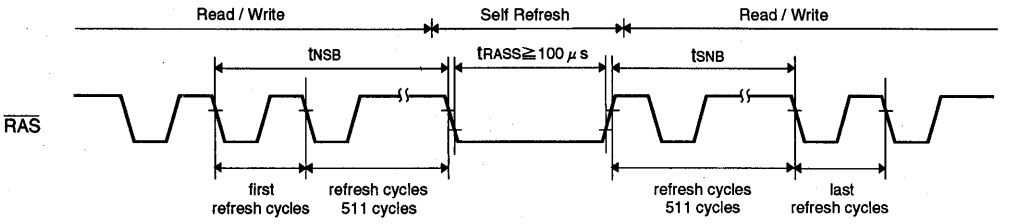
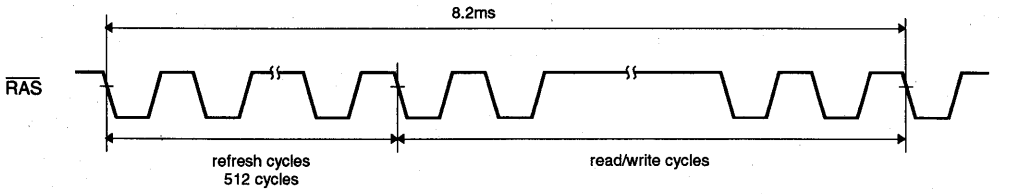


Table 3

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR burst refresh	tNSB≦8.2ms	tSNB≦8.2ms
RAS only burst refresh	tNSB+tSNB≦8.2ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of RAS only burst refresh

All combination of nine row address signals (A_0~A_8) are selected during 512 continuous RAS only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval tNSB from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval tSNB from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 RAS only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period should be set within tSNB (shown in table 3).

16M DRAM(5V Version)

M5M416100BJ,TP-5,-6,-7

FAST PAGE MODE 16777216-BIT (16777216-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 16777216-word by 1-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416100BXX-5	50	13	25	90	495
M5M416100BXX-6	60	15	30	110	405
M5M416100BXX-7	70	20	35	130	340

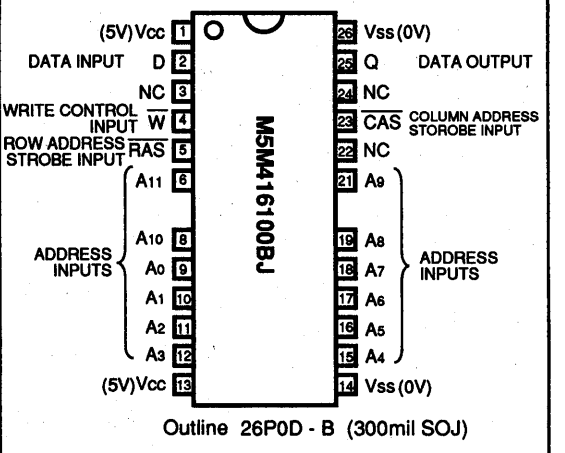
XX=J,TP

- Standard 26 pin SOJ,26 pin TSOP
- Single 5V ±10%supply
- Low stand-by power dissipation
  M5M416100B ····· 5.5mW (Max)CMOS input level
- Low operating power dissipation
  M5M416100Bxx- 5 ····· 605.0mW (Max)
  M5M416100Bxx- 6 ····· 495.0mW (Max)
  M5M416100Bxx- 7 ····· 415.0mW (Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh and Hidden refresh capabilities
- Early-write operation gives common I/O capability
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})

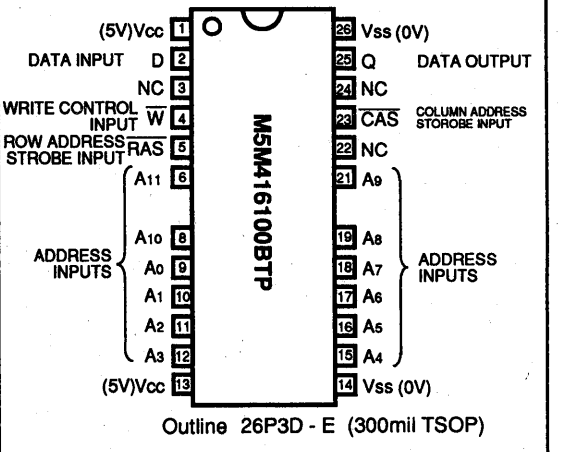
APPLICATION

Main memory unit for computers, Microcomputer memory,Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D - B (300mil SOJ)



Outline 26P3D - E (300mil TSOP)

NC : NO CONNECTION

M5M416100BJ,TP-5 : Under development

FUNCTION

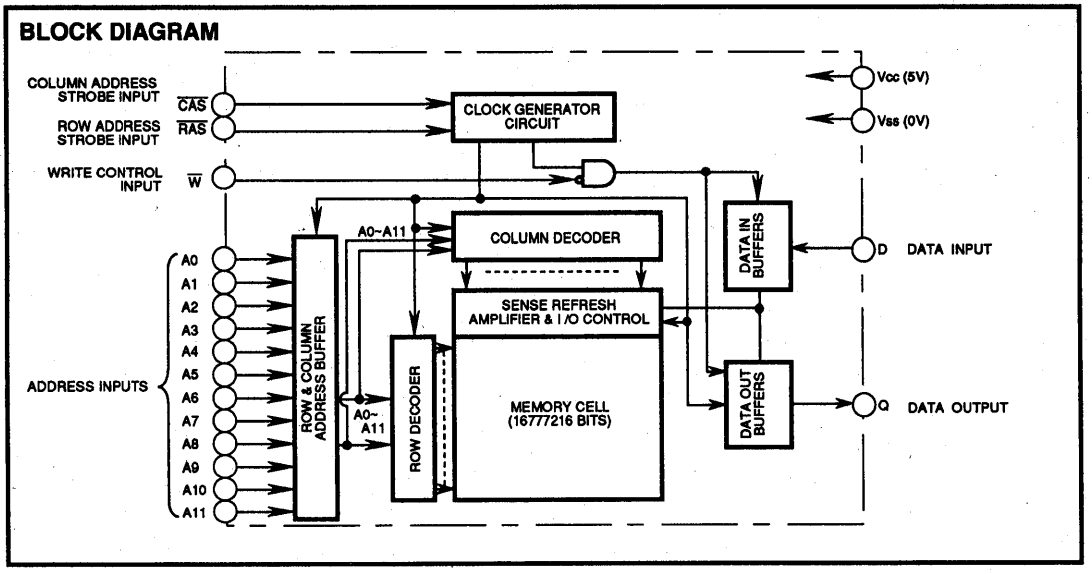
The M5M416100BJ, TP provide, in addition to normal read, write , and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	
Write (Early write)	ACT	ACT	ACT	APD	APD	APD	OPN	YES	Fast page mode identical
Write (Delayed write)	ACT	ACT	ACT	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
V_O	Output voltage		-1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6.0V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4)	M5M416100B-5	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M416100B-6				90	
		M5M416100B-7				75	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
		M5M416100B	$\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=A_0～A_{11}≧Vcc-0.5V output open			1	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3)	M5M416100B-5	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			110	mA
		M5M416100B-6				90	
		M5M416100B-7				75	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M416100B-5	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M416100B-6				70	
		M5M416100B-7				60	
I_{CC8}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416100B-5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			110	mA
		M5M416100B-6				90	
		M5M416100B-7				75	
I_{CC8}(AV)	Average supply current from Vcc Extended refresh (Note 5)	M5M416100B	$\overline{RAS}$ cycling and $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling Vcc-0.2V≦$\overline{W}$=A_0～A_{11}≦0.2V output open, t_{RC}=32μs, t_{RAS}=t_{RAS}min～1μs			0.6	mA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M416100B	$\overline{RAS}$=$\overline{CAS}$≦0.2V, output open Vcc-0.2V≦$\overline{W}$=A_0～A_{11}≦0.2V			0.4	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance				7	pF

SWITCHING CHARACTERISTICS (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M416100B-5		M5M416100B-6		M5M416100B-7		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
t_{AA}	Column address access time	(Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

10: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11: $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leq 10\mu$ A) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M416100B-5		M5M416100B-6		M5M416100B-7		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			64		64		64	ms
t_{REF}	Refresh cycle time *			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_T	Transition time	(Note17)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 18)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 20)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note19)	108		130		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width	68	10000	80	10000	95	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	31	10000	35	10000	45	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	68		80		95		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	31		35		45		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note20)	13		15		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note20)	50		60		70		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note20)	25		30		35		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		10		15		ns

Note 19: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{RWL(min)}+t_{RP(min)}+3t_T$.

20: t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the Q pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the Q will contain the data read from the selected address. If neither of the above condition (delayed write) of the Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 21)

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	53		60		70		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note22)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note23)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note20)	30		35		40		ns

Note 21: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
22: $t_{RAS(min)}$ is specified as $t_{RAS(min)}=t_{CSH(min)}+t_{PC(min)}$.
23: $t_{CP(max)}$ is specified as a reference point only.

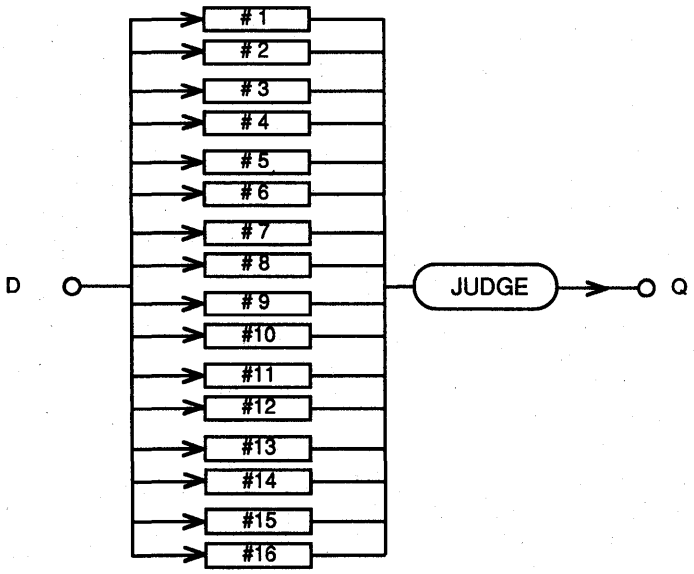
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 24: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

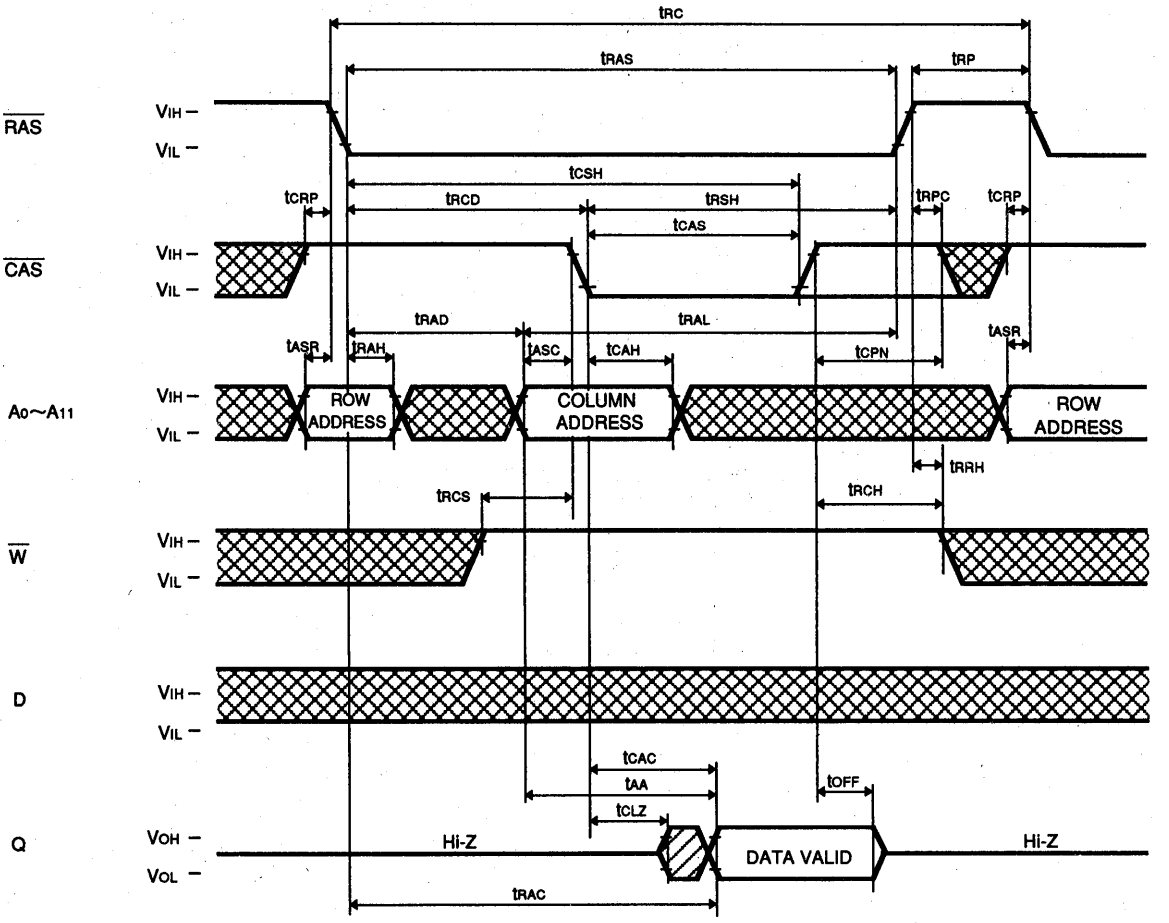
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M416100B-5		M5M416100B-6		M5M416100B-7		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns



Timing Diagrams (Note 25)

Read Cycle

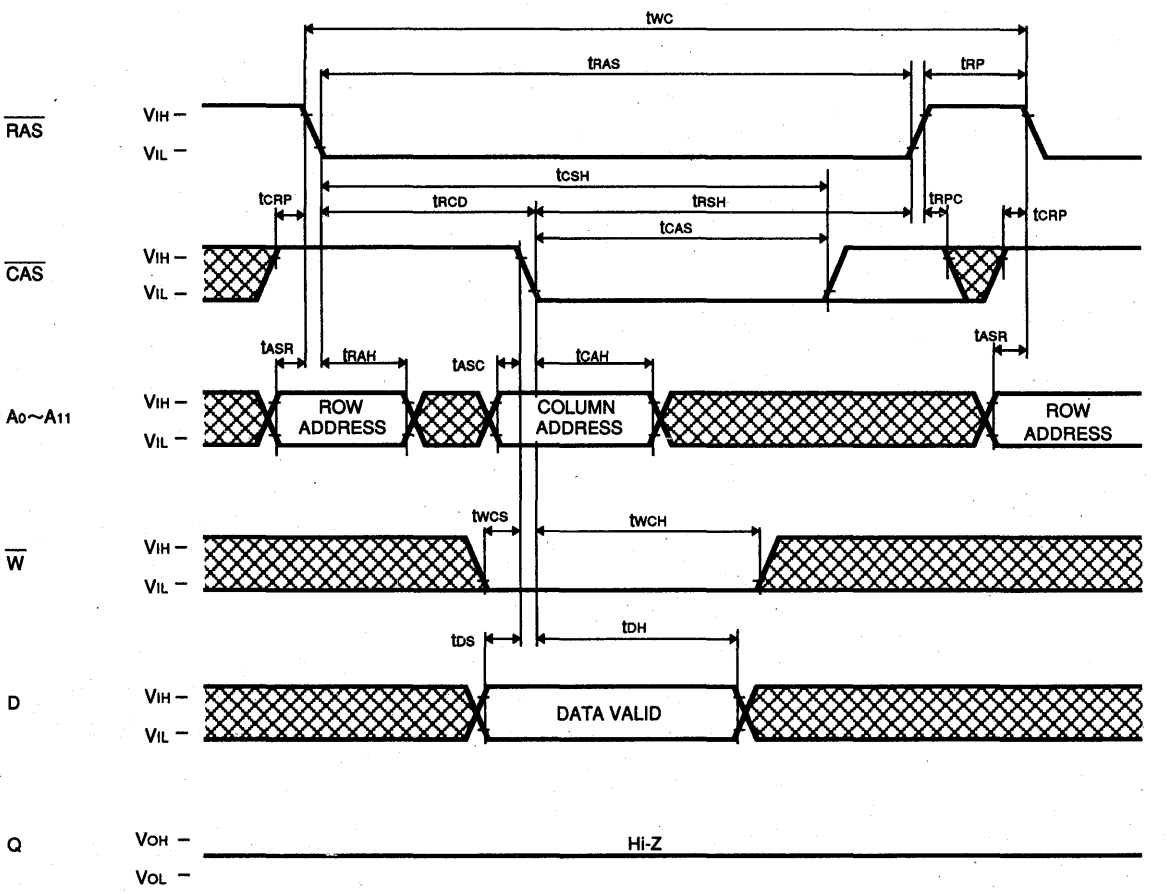


Note 25

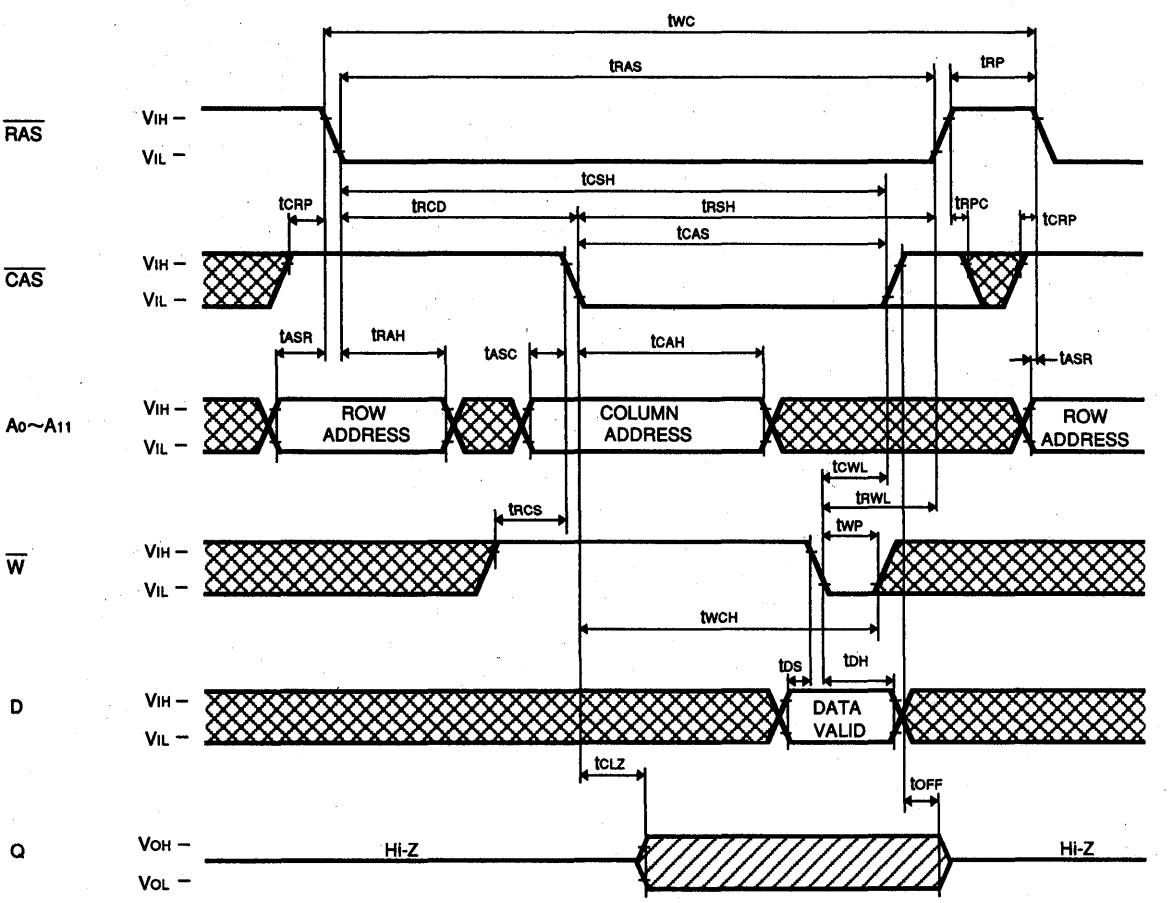
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

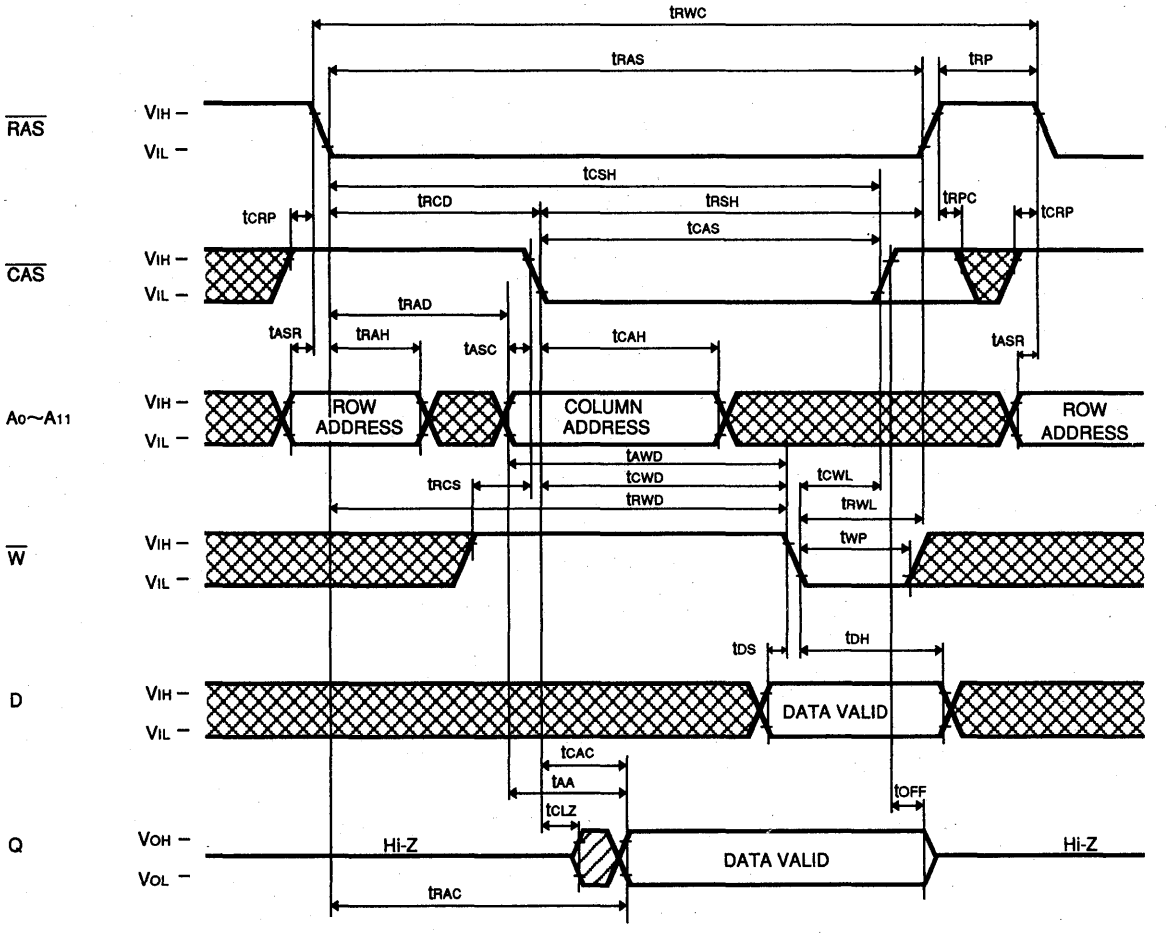
Write Cycle (Early write)



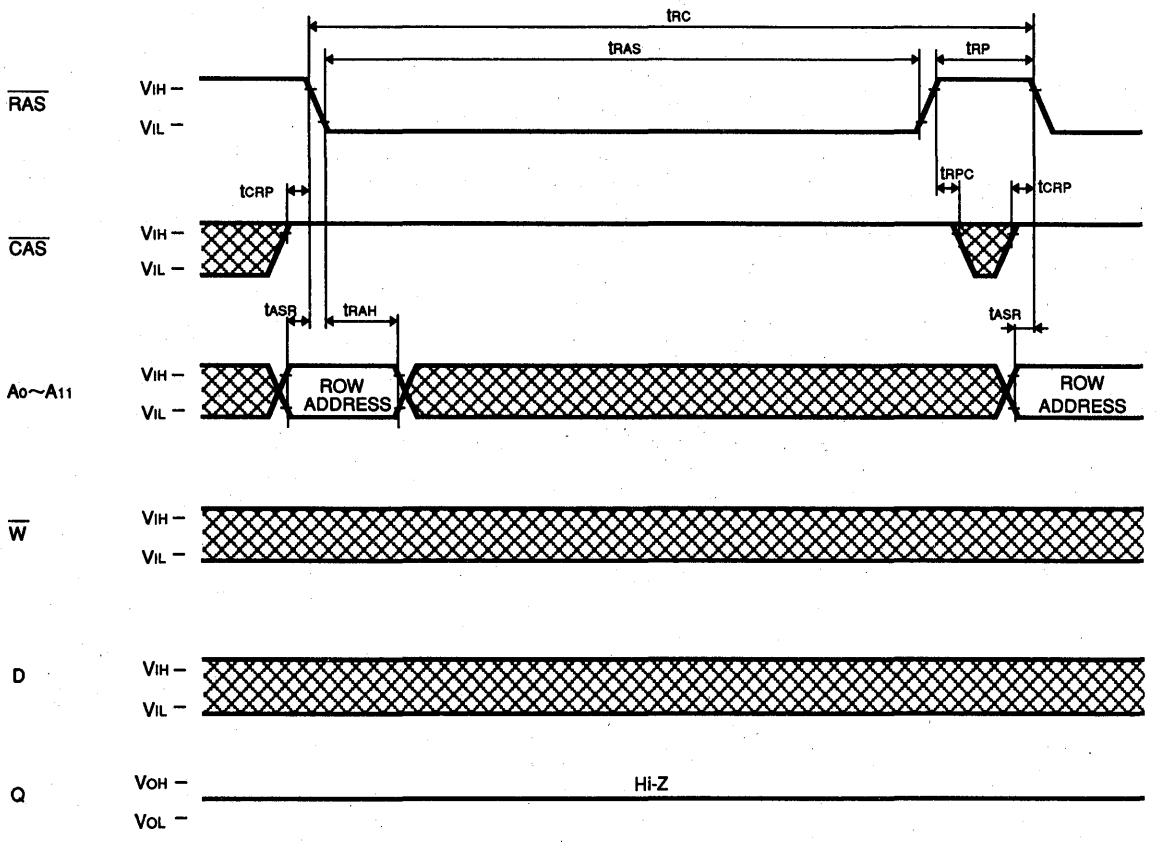
Write Cycle (Delayed write)



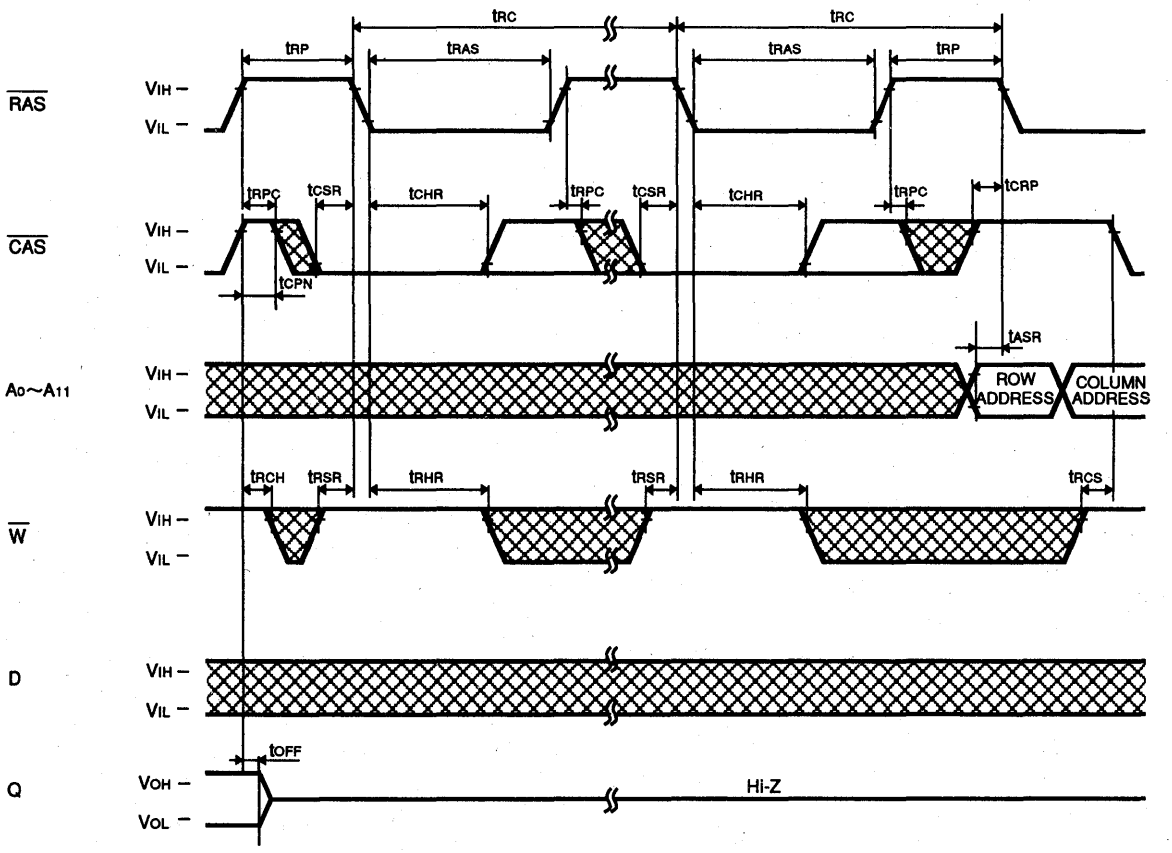
Read-Write, Read-Modify-Write Cycle



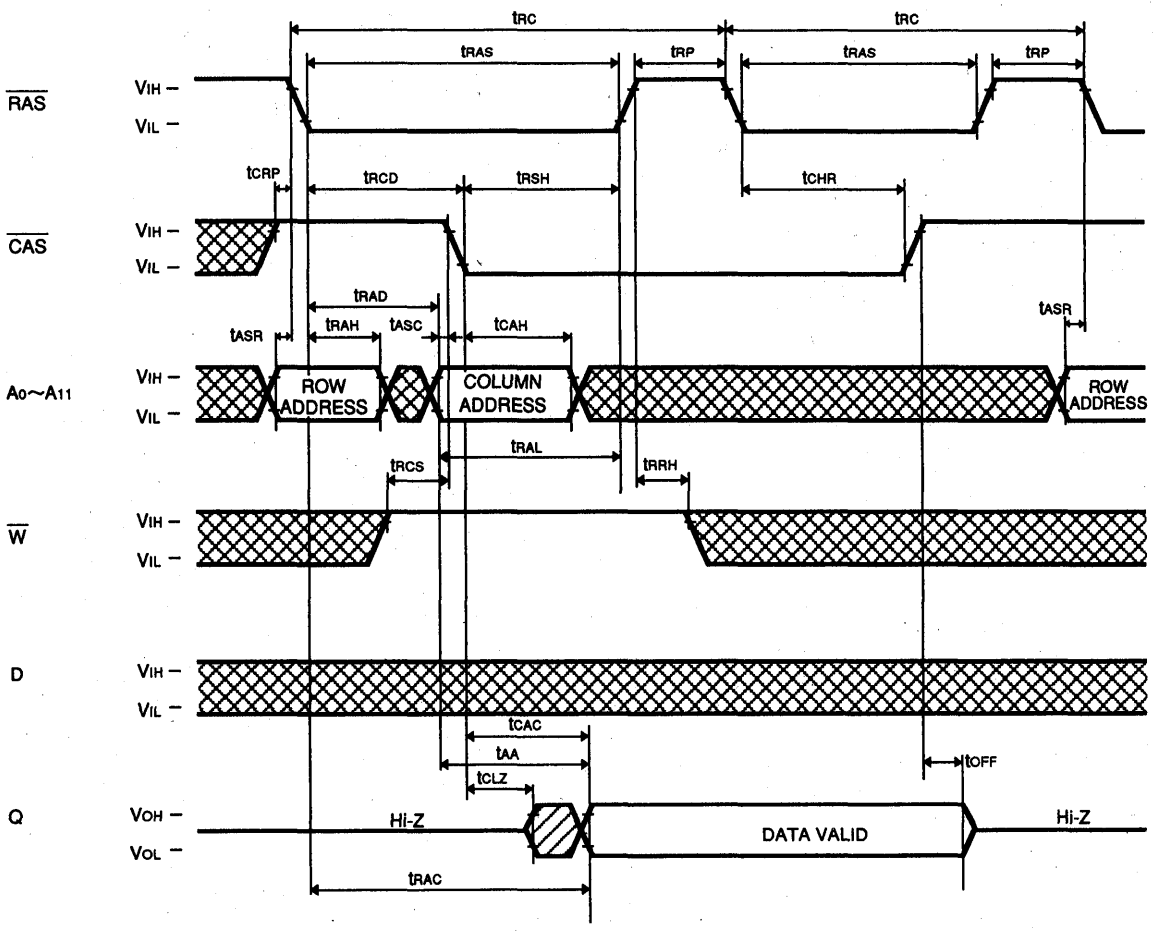
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

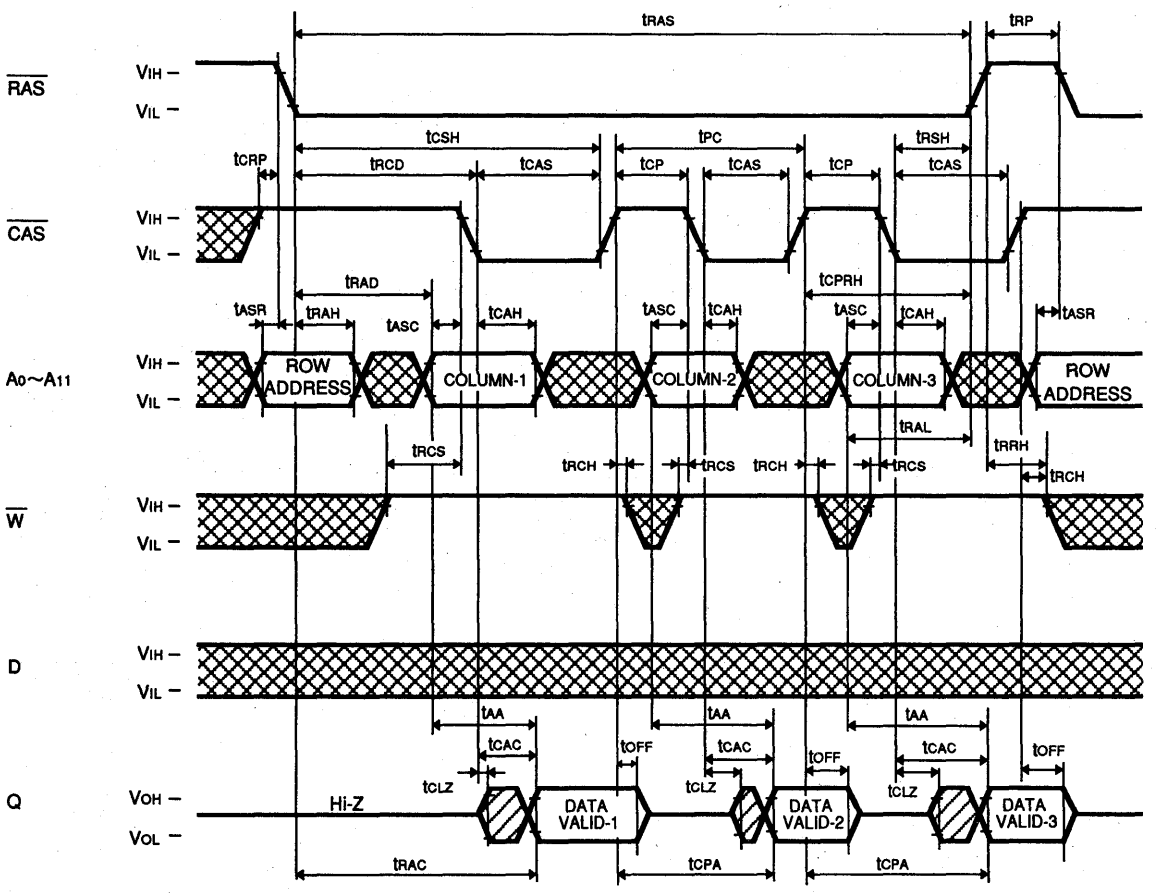


Hidden Refresh Cycle (Read) (Note 26)

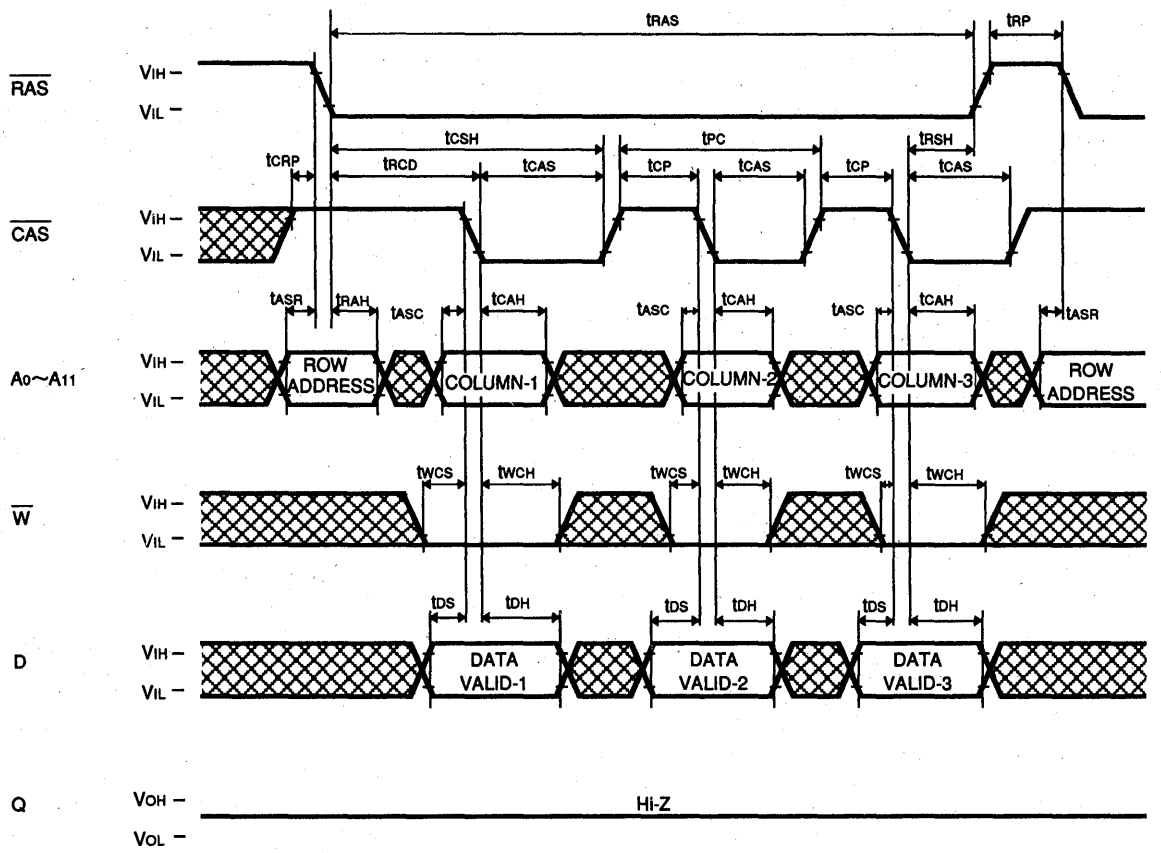


Note 26: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

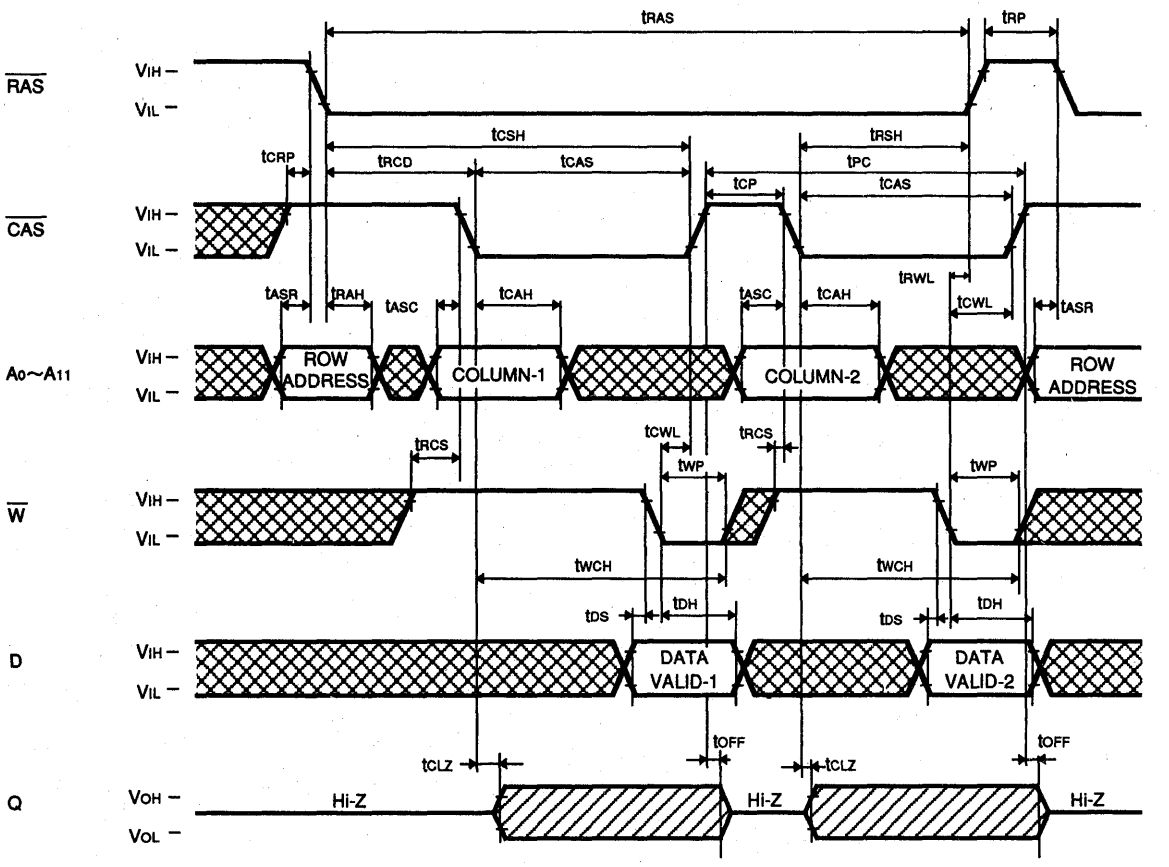
Fast Page Mode Read Cycle



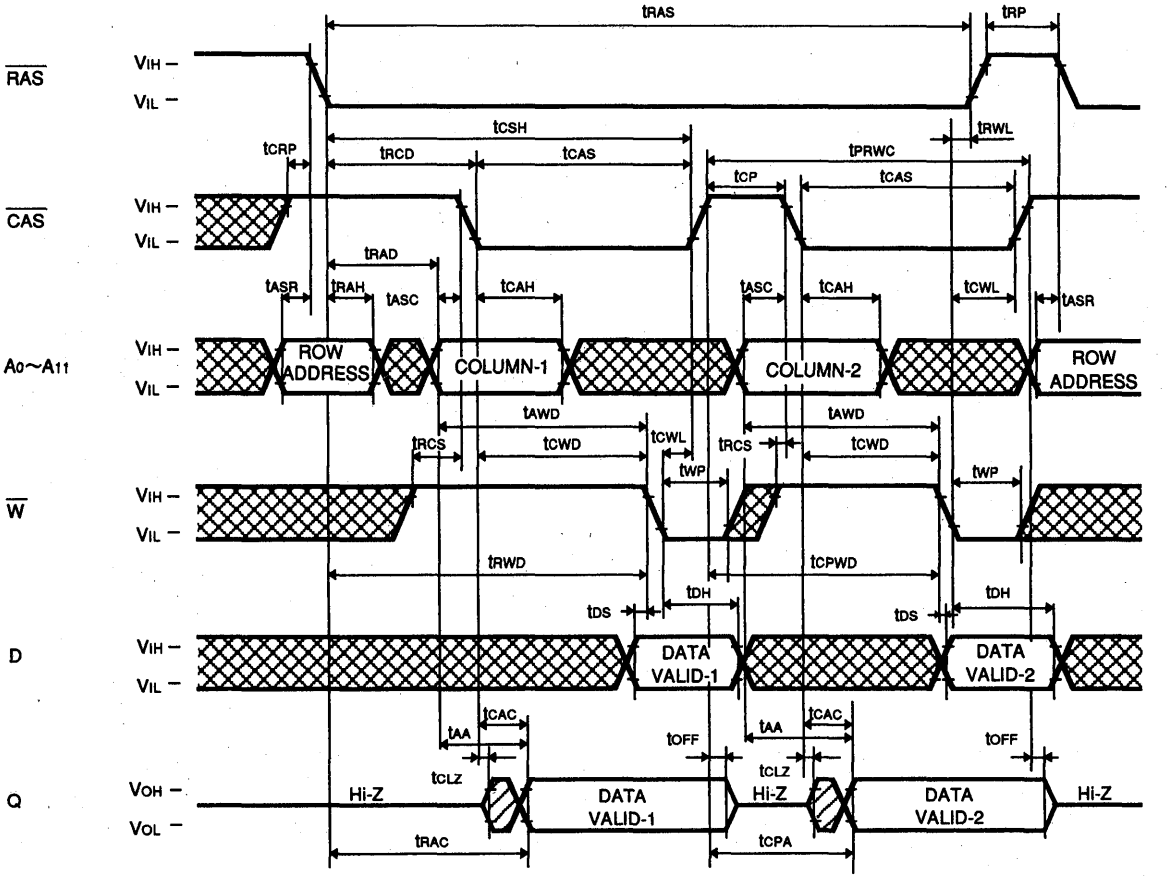
Fast Page Mode Write Cycle (Early Write)



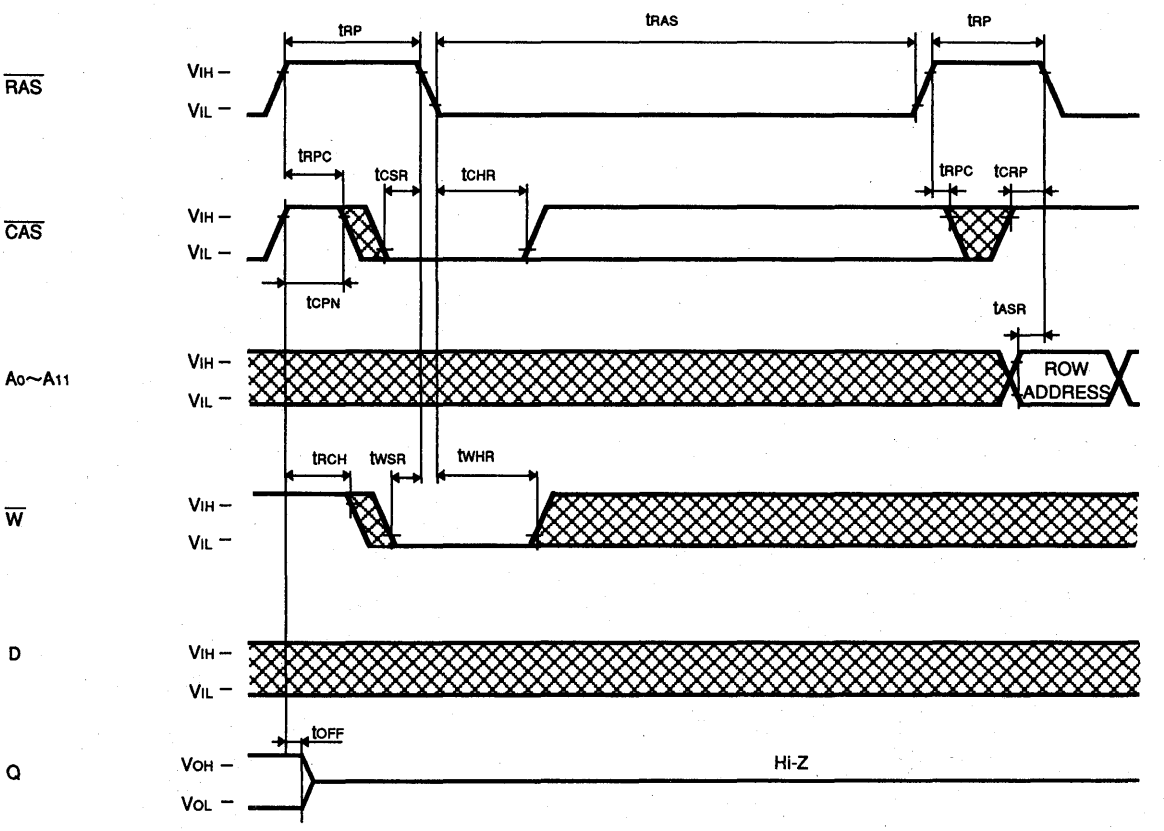
Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write,Read-Modify-Write Cycle



TEST Mode SET Cycle (Note 27)



Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a CAS before RAS refresh cycle (CBR refresh cycle) or a RAS only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . No addressing of CA11, CA10, CA1 and CA0 is required.
During a write cycle, data on D (input) pin is written into 16 bits memory cells. During a read cycle, Q (output) pin shows the test result of the 16 bit. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.

M5M416400BJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416400BXX-5,-5S	50	13	25	13	90	495
M5M416400BXX-6,-6S	60	15	30	15	110	405
M5M416400BXX-7,-7S	70	20	35	20	130	340

XX=J,TP

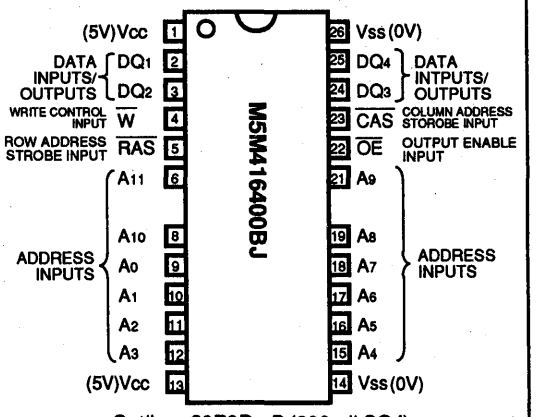
- Standard 26 pin SOJ,26 pin TSOP
- Single 5V ±10%supply
- Low stand-by power dissipation
  - M5M416400B ····· 5.5mW (Max)CMOS input level
  - M5M416400B(S) ····· 2.2mW (Max)CMOS input level
- Low operating power dissipation
  - M5M416400Bxx- 5,- 5S ····· 605.0mW (Max)
  - M5M416400Bxx- 6,- 6S ····· 495.0mW (Max)
  - M5M416400Bxx- 7,- 7S ····· 415.0mW (Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh and Self refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})
- 4096 refresh cycles every 128ms (A_0 ~A_{11}) *

  * : Applicable to self refresh version only

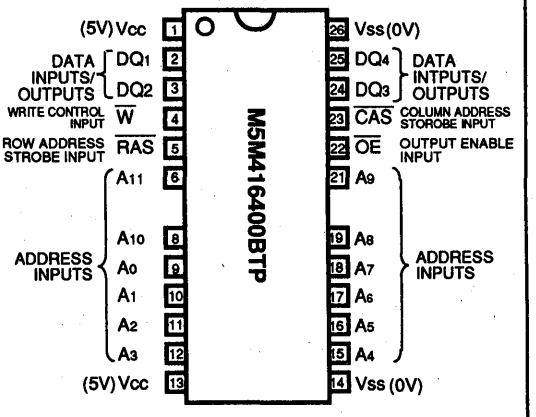
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D - B (300mil SOJ)



Outline 26P3D - E(300mil TSOP)

M5M416400BJ,TP-5, -5S : Under development

MITSUBISHI ELECTRIC

FUNCTION

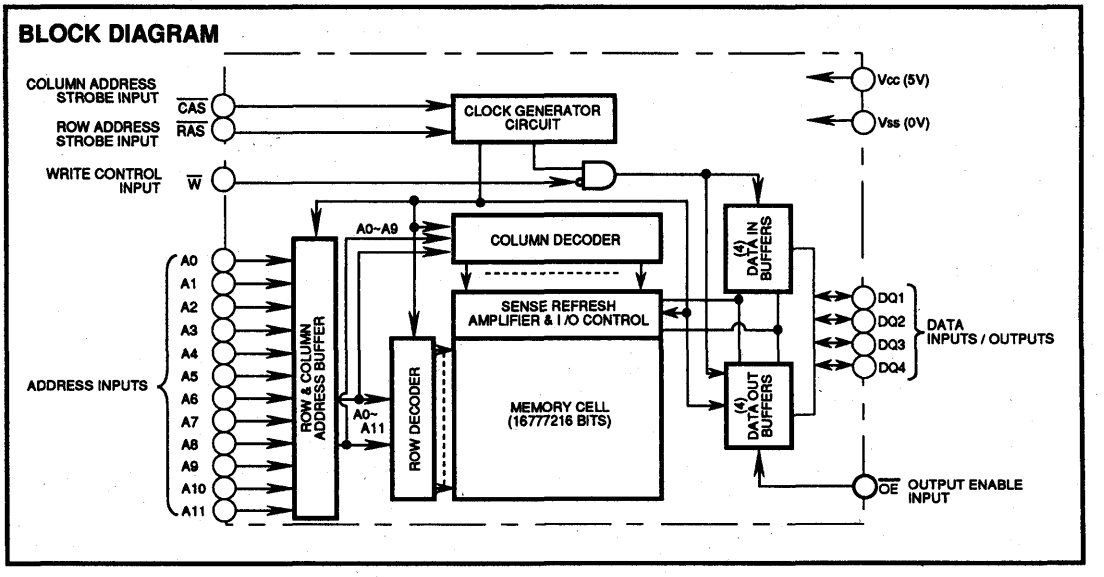
The M5M416400BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
Vo	Output voltage		-1～7	V
Io	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
Ioz	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6.0V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4)	M5M416400B-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M416400B-6,-6S				90	
		M5M416400B-7,-7S				75	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
		M5M416400B	$\overline{RAS}$=$\overline{CAS}$=$\overline{OE}$=$\overline{W}$=A_0～A_{11}≧Vcc -0.5V output open			1	
		M5M416400B(S)				0.4	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3)	M5M416400B-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			110	mA
		M5M416400B-6,-6S				90	
		M5M416400B-7,-7S				75	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M416400B-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M416400B-6,-6S				70	
		M5M416400B-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416400B-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			110	mA
		M5M416400B-6,-6S				90	
		M5M416400B-7,-7S				75	
I_{CC8}(AV)	Average supply current from Vcc Extended refresh (Note 5)	M5M416400B(S)	$\overline{RAS}$ cycling and $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A_0～A_{11}≦0.2V output open, t_{RC}=32μs, t_{RAS}=t_{RAS}min～1μs			0.6	mA
I_{CC9} (AV)	Average supply current from Vcc Self - Refresh cycle (Note 5)	M5M416400B(S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V, output open Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A_0～A_{11}≦0.2V			0.4	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0～70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0～70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
t_{AA}	Column address access time	(Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
8: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
9: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
10: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			64		64		64	ms
t_{REF}	Refresh cycle time *			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note18)	13		15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note18)	13		15		15		ns
t_T	Transition time	(Note19)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.
15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
17: Either t_{DZC} or t_{DZO} must be satisfied.
18: Either t_{CDD} or t_{ODD} must be satisfied.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

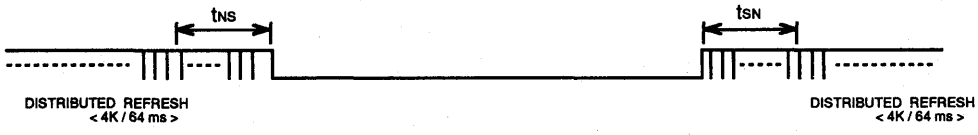
Self Refresh Cycle

Symbol	Parameter	Limits						Unit
		M5M416400B-5S		M5M416400B-6S		M5M416400B-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

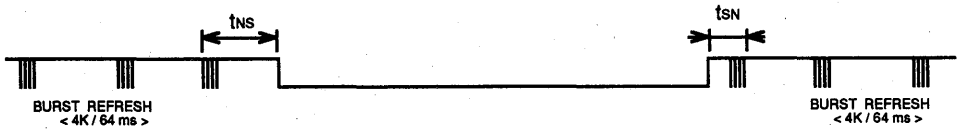
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leqq 64$ ms and $t_{SN} \leqq 64$ ms.



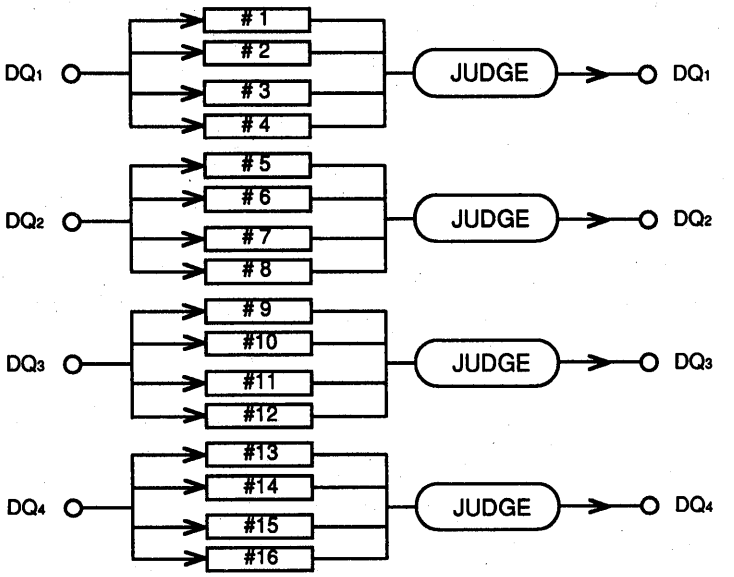
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} + t_{SN} \leqq 64$ ms.



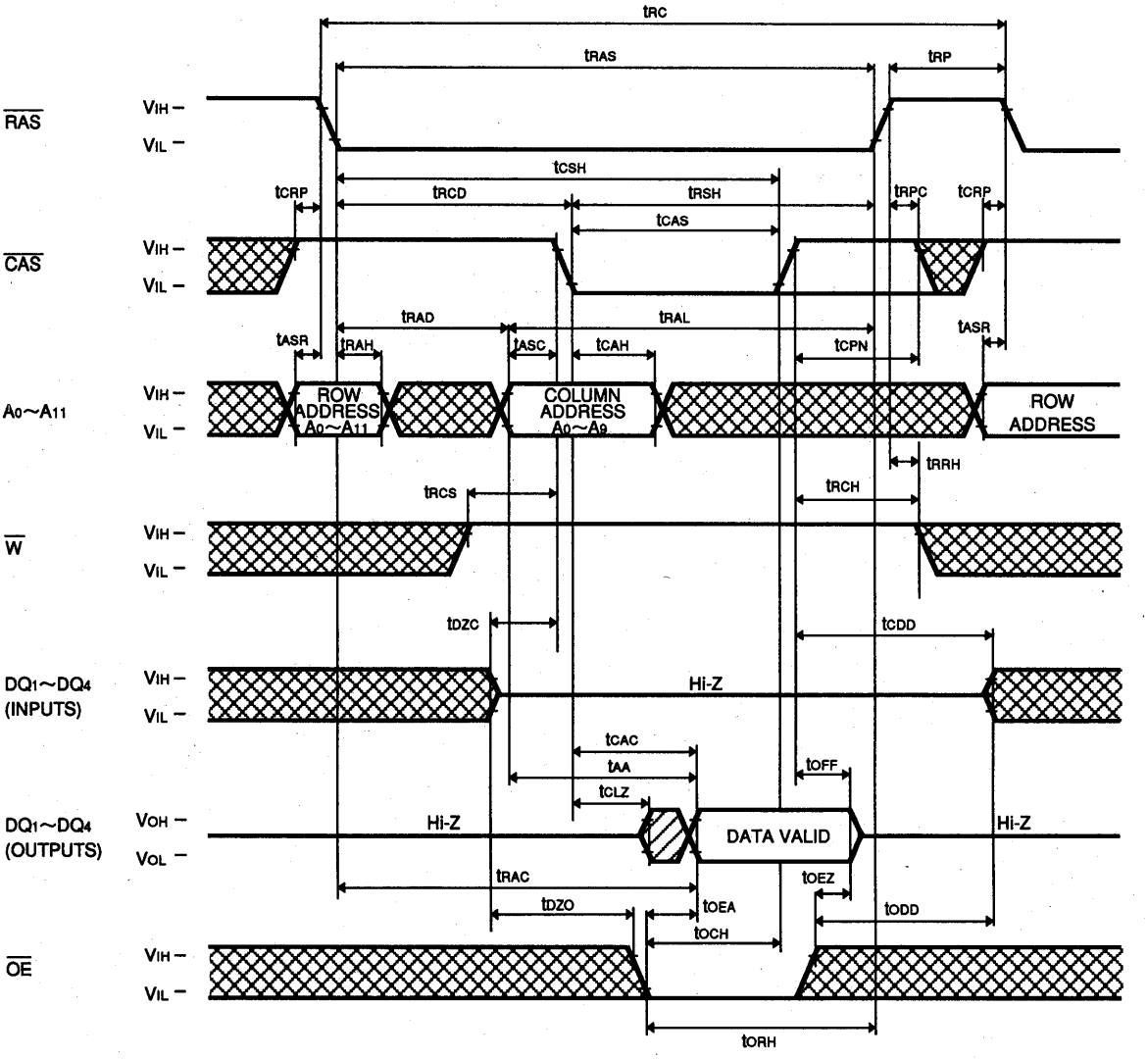
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M416400B-5,-5S		M5M416400B-6,-6S		M5M416400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns



Timing Diagrams (Note 27)

Read Cycle

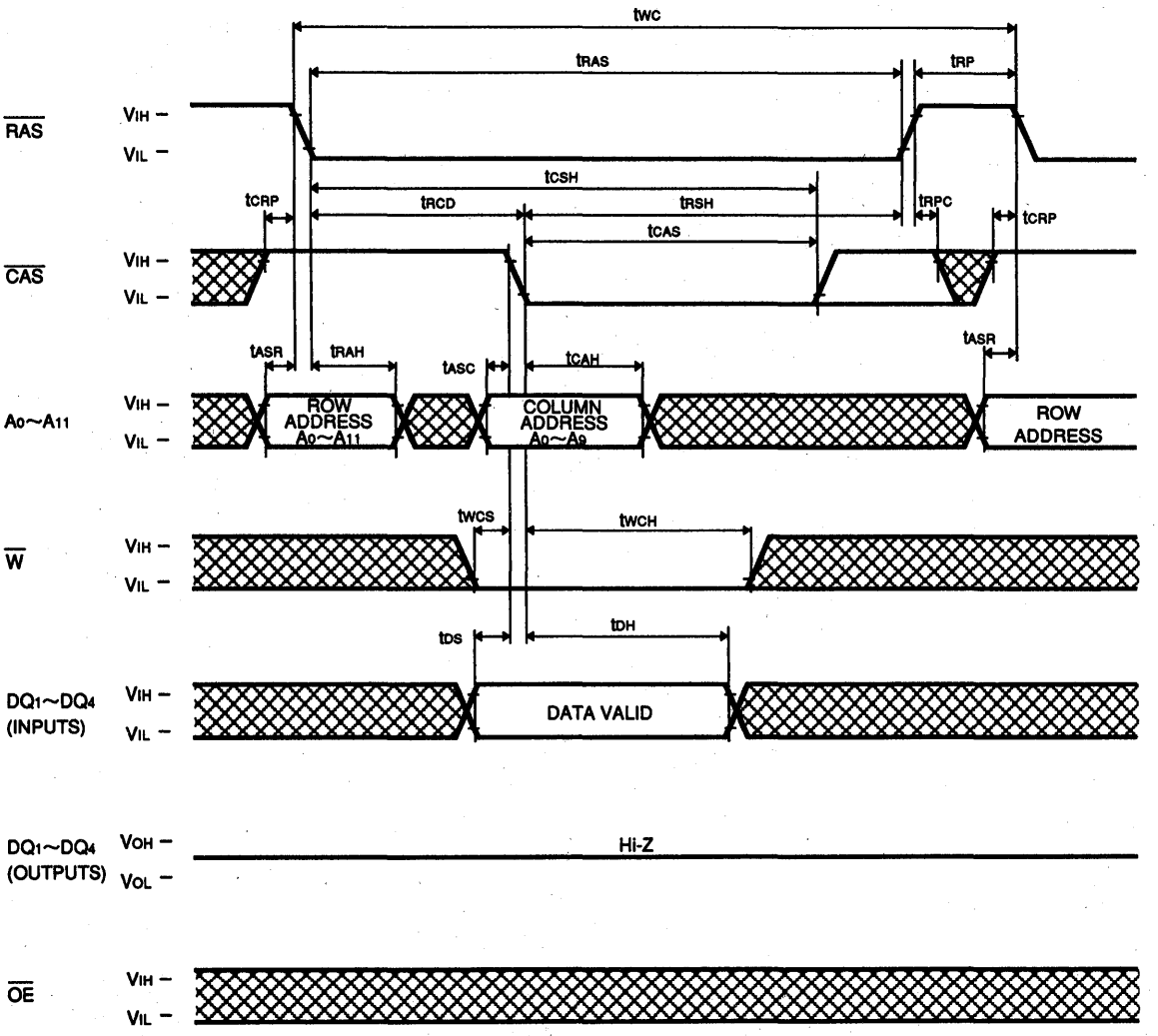


Note 27

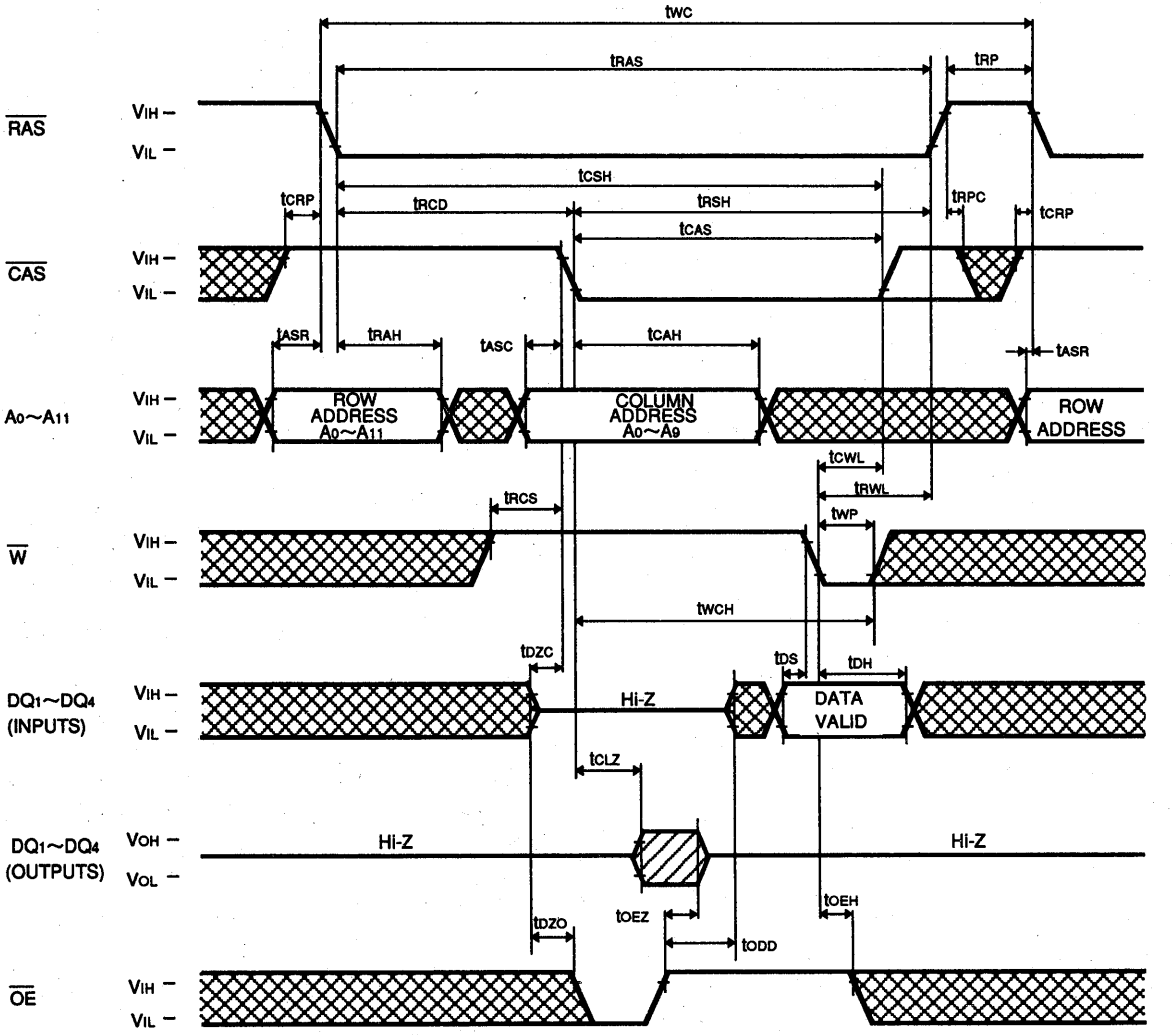
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

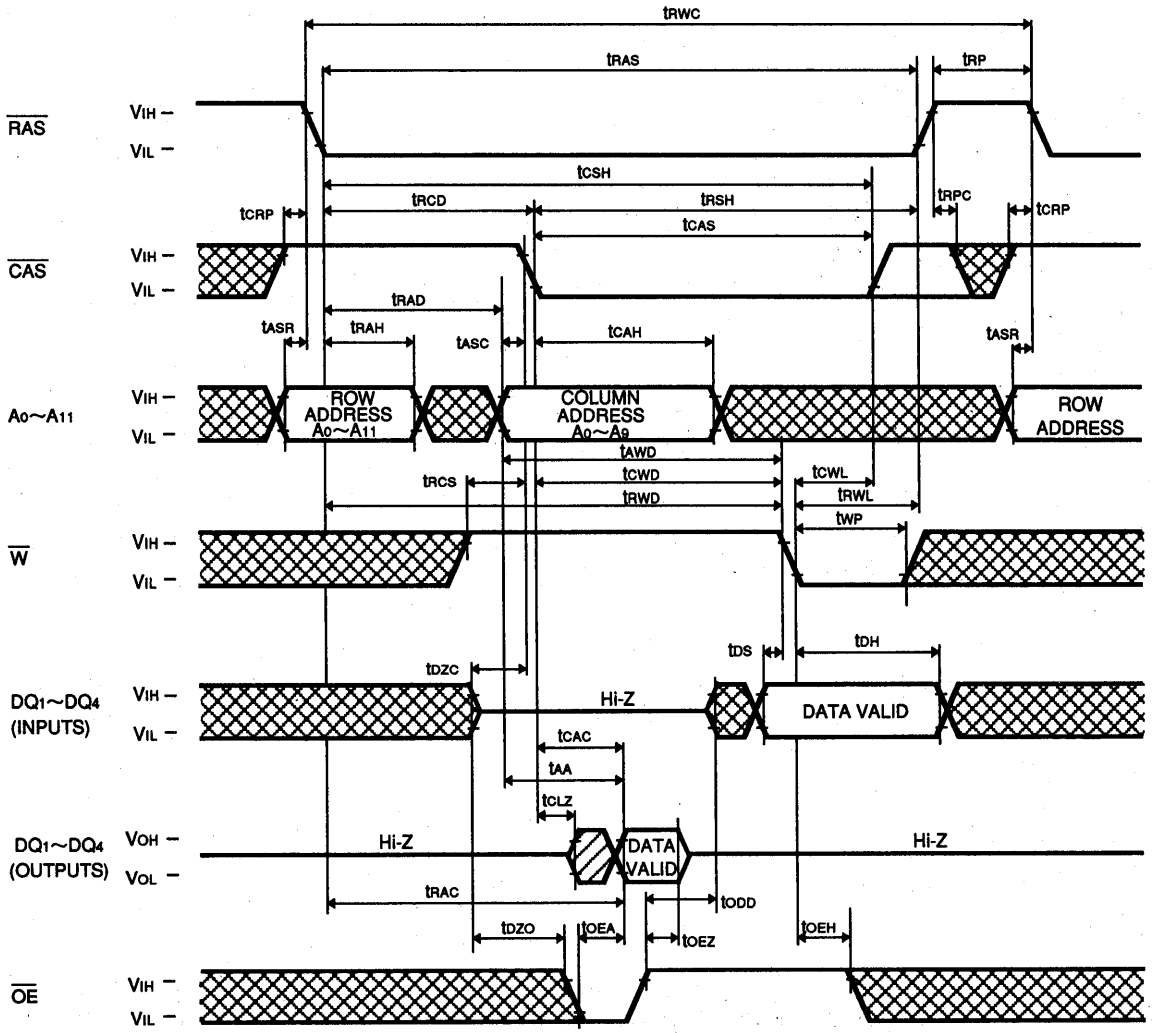
Write Cycle (Early write)



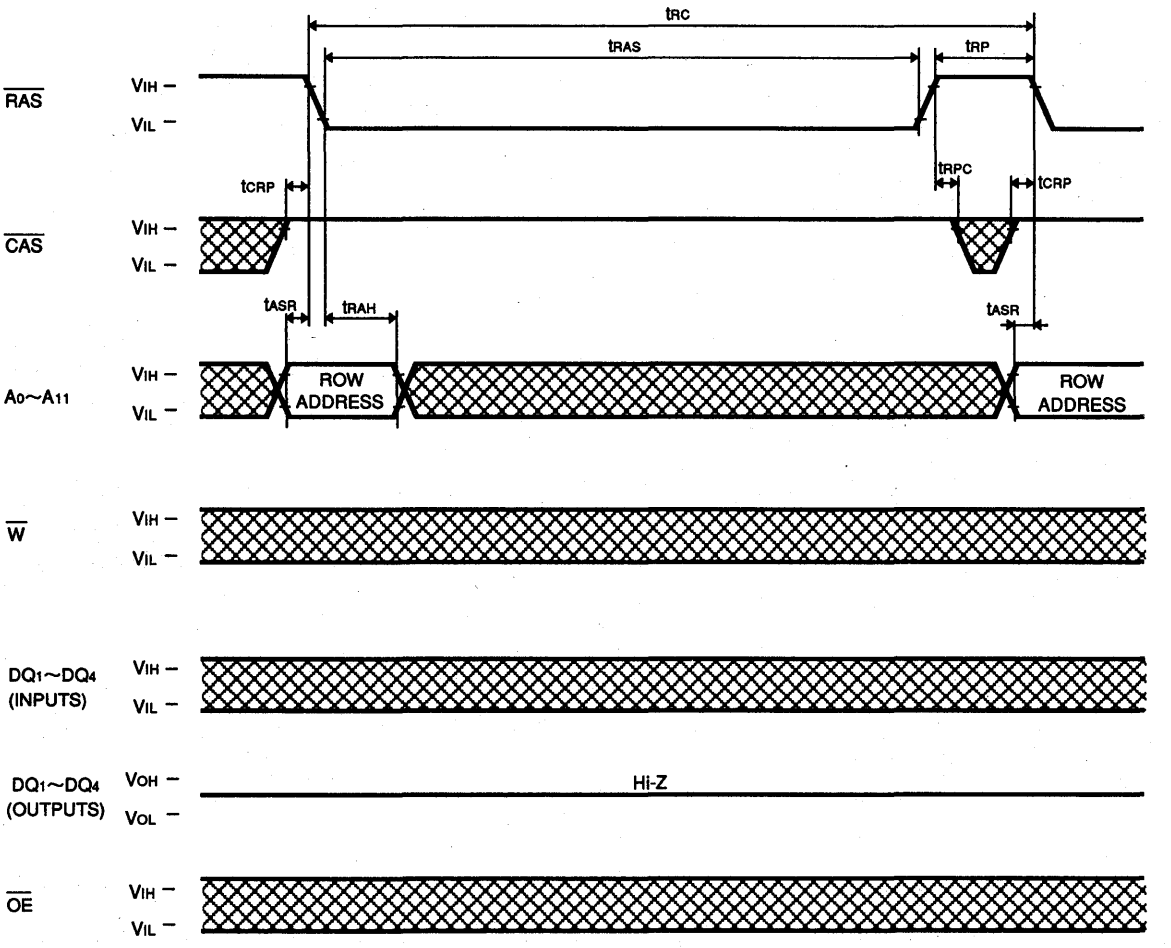
Write Cycle (Delayed write)



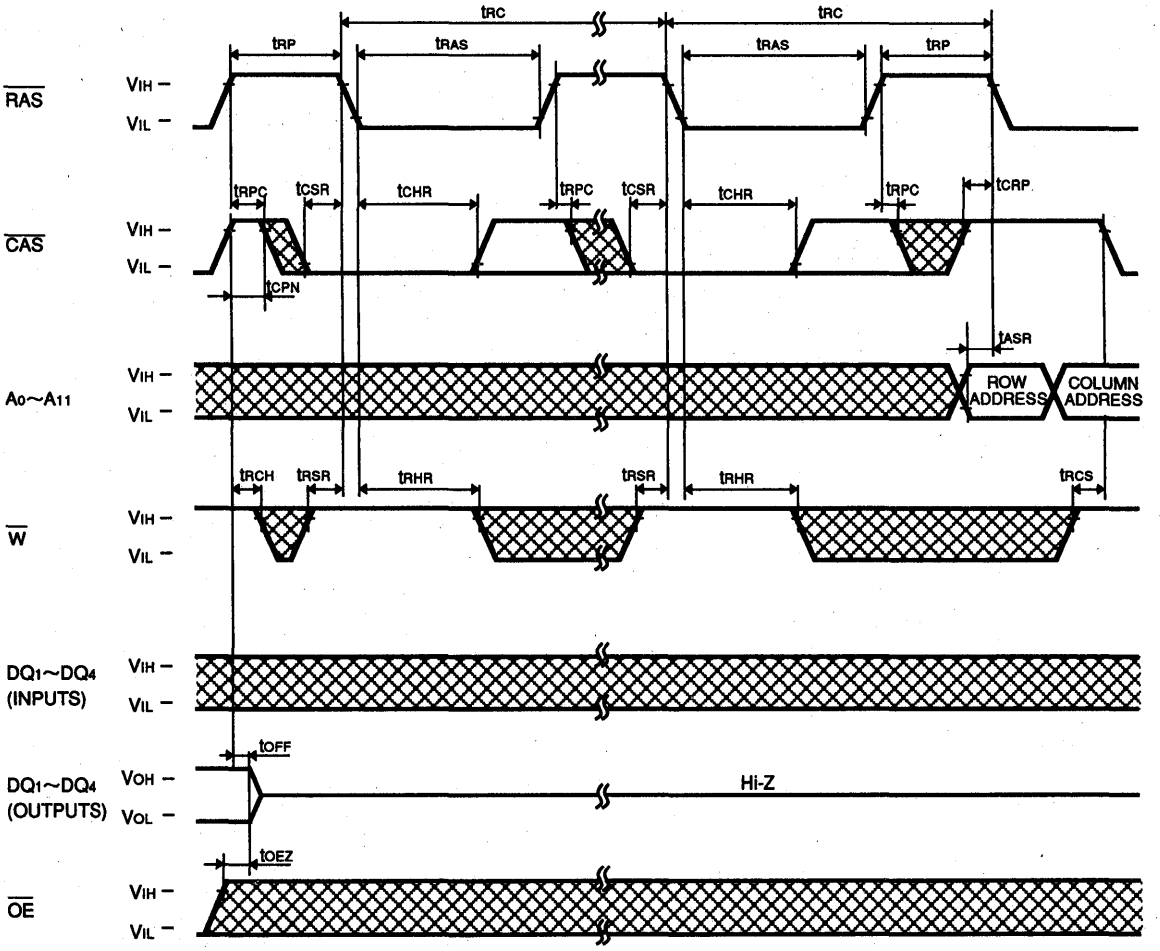
Read-Write, Read-Modify-Write Cycle



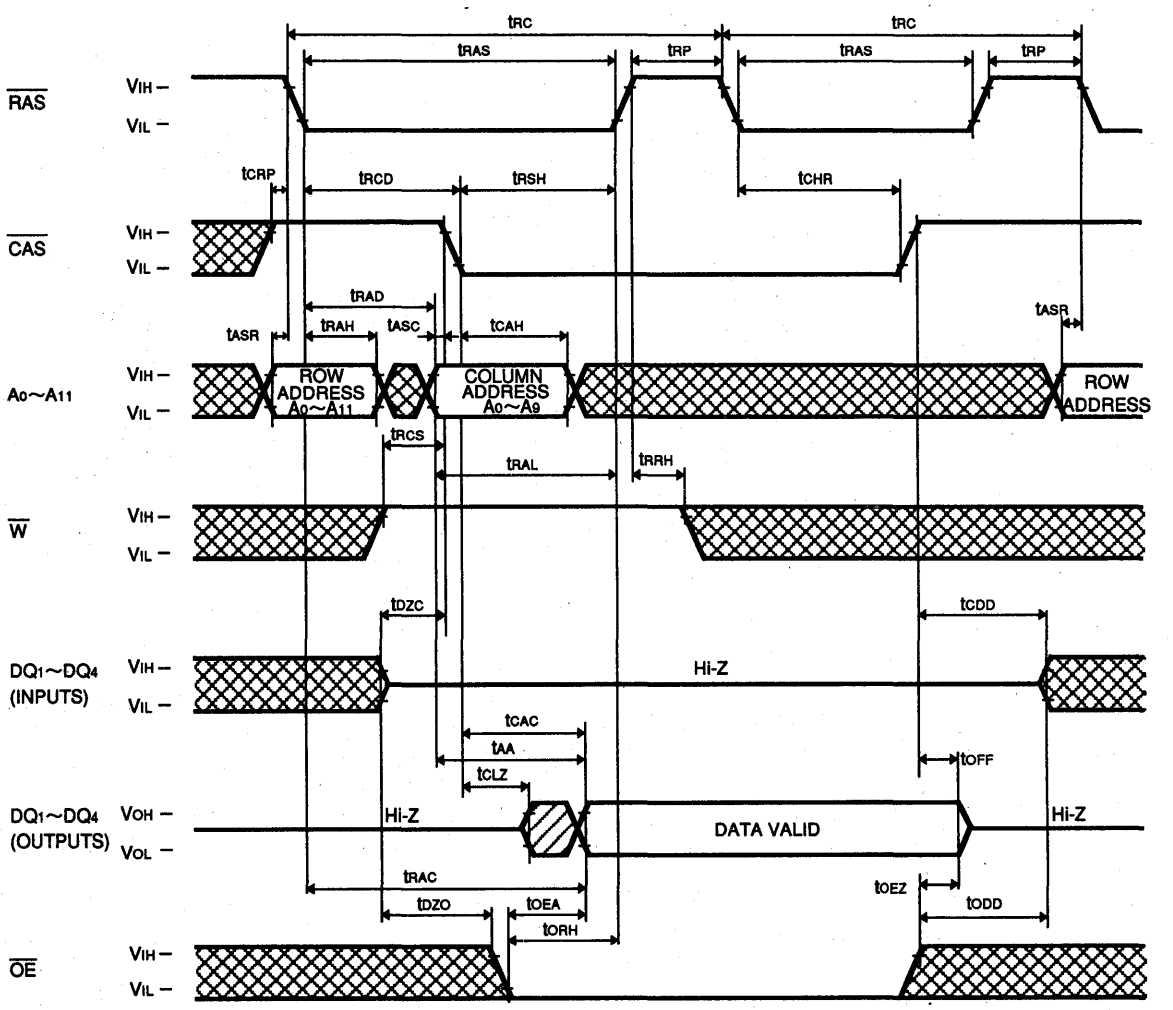
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

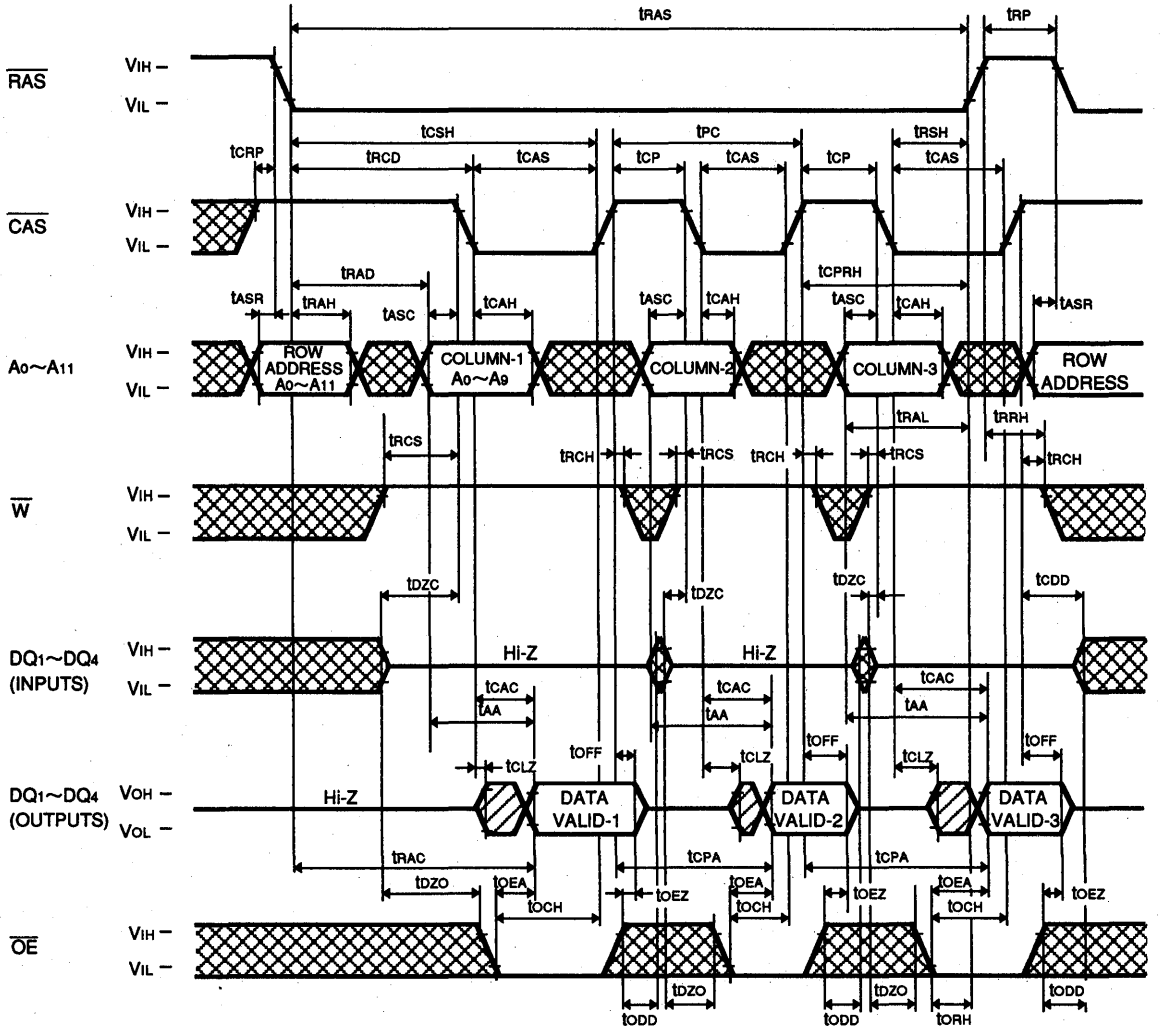


Hidden Refresh Cycle (Read) (Note 28)



Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



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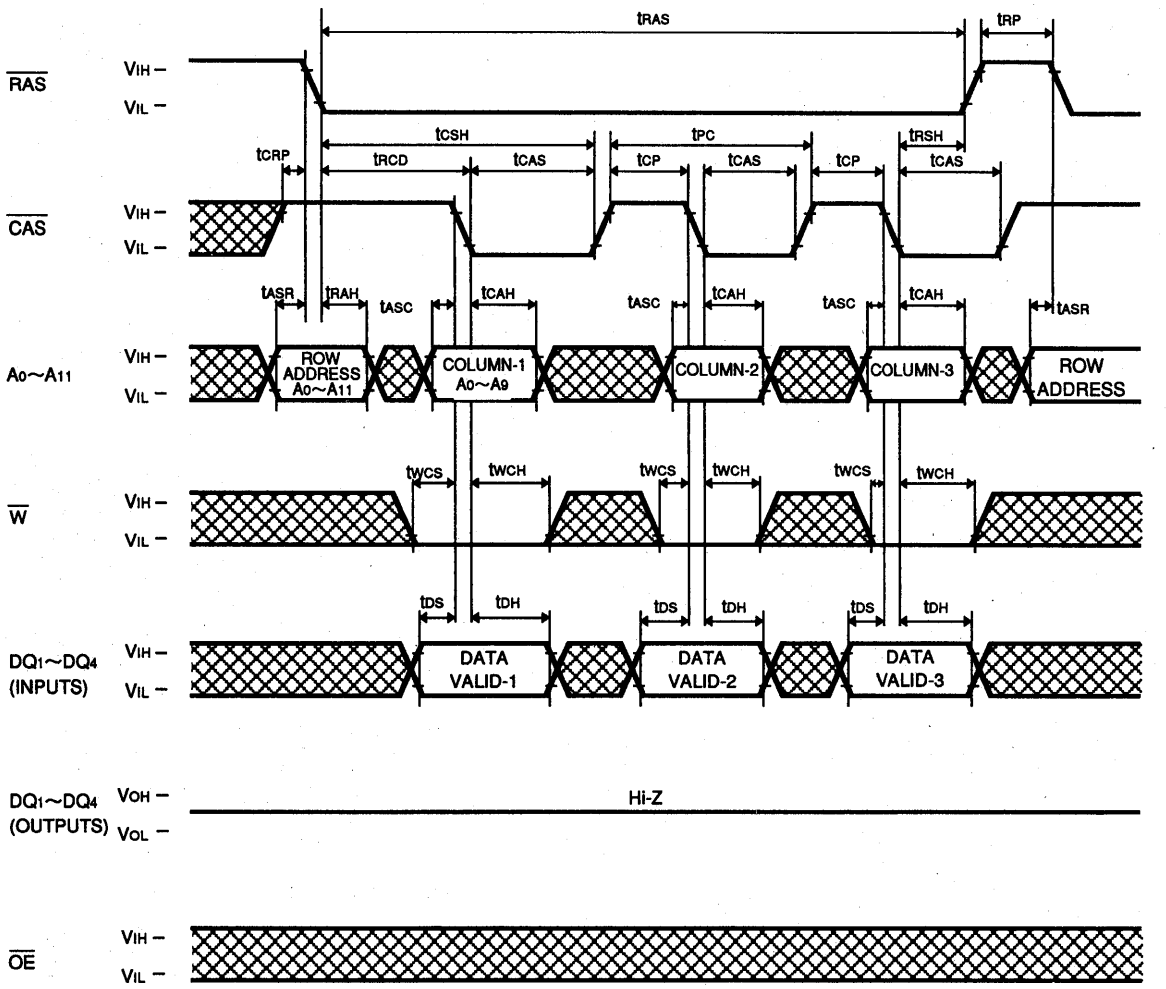
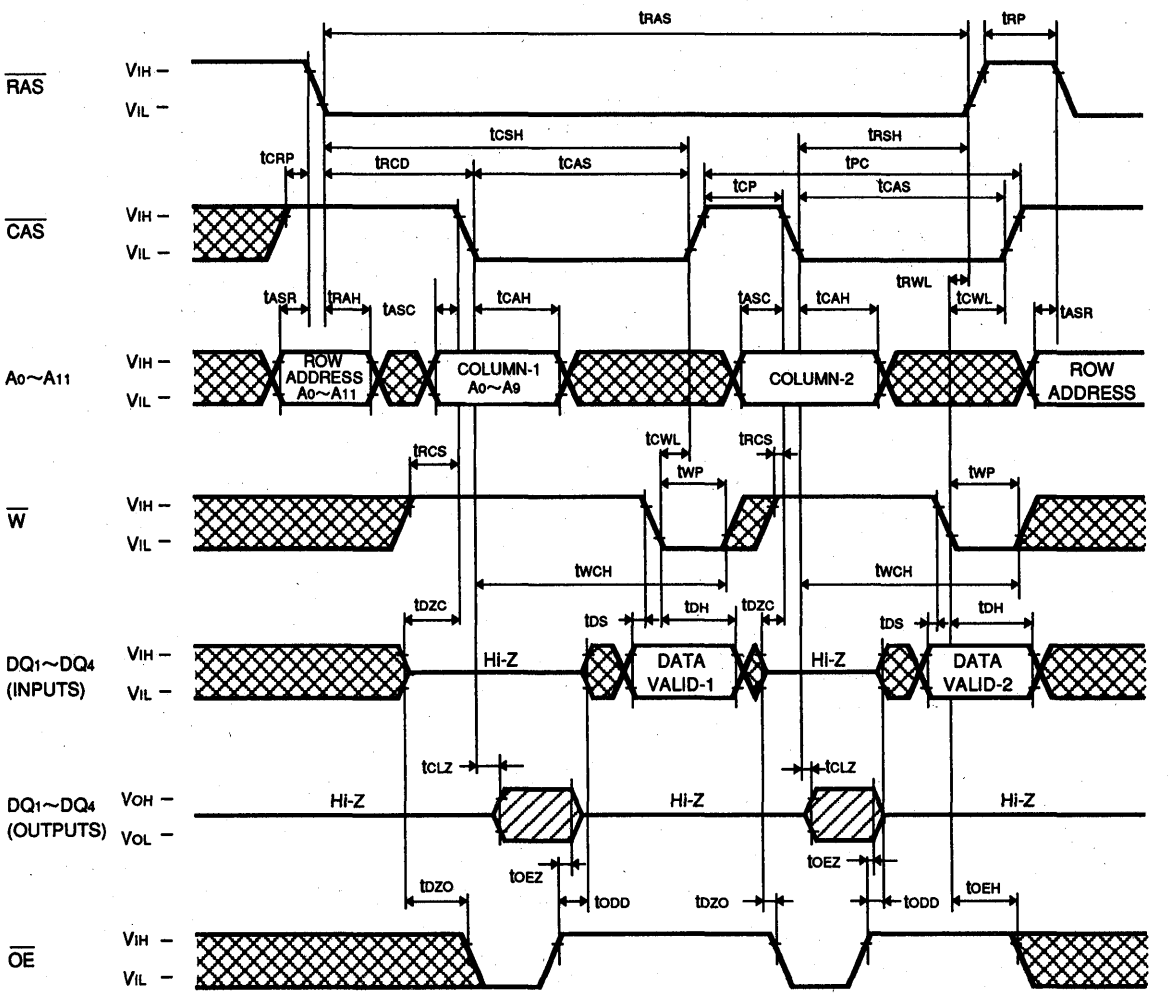
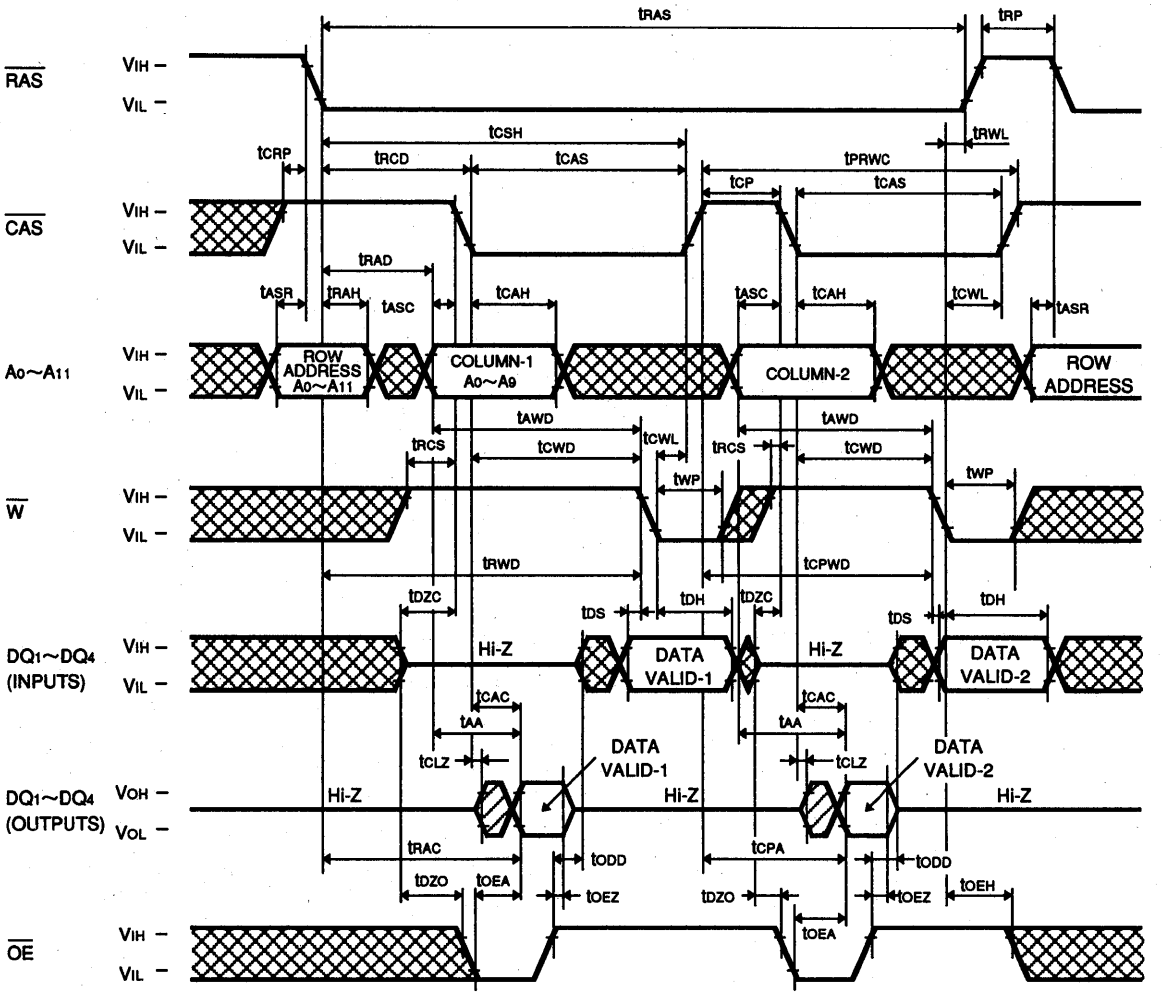
Fast Page Mode Write Cycle (Early Write)



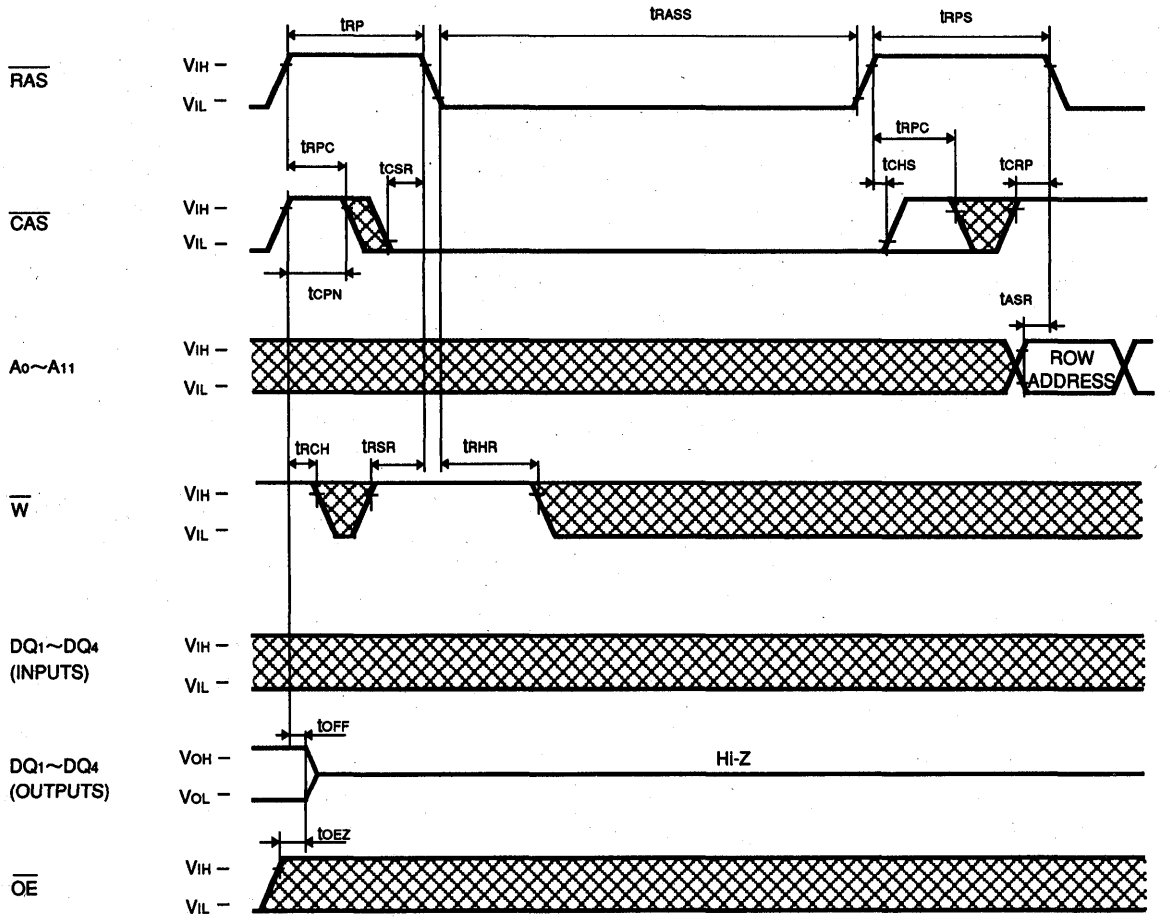
Fast-Page Mode Write Cycle (Delayed Write)



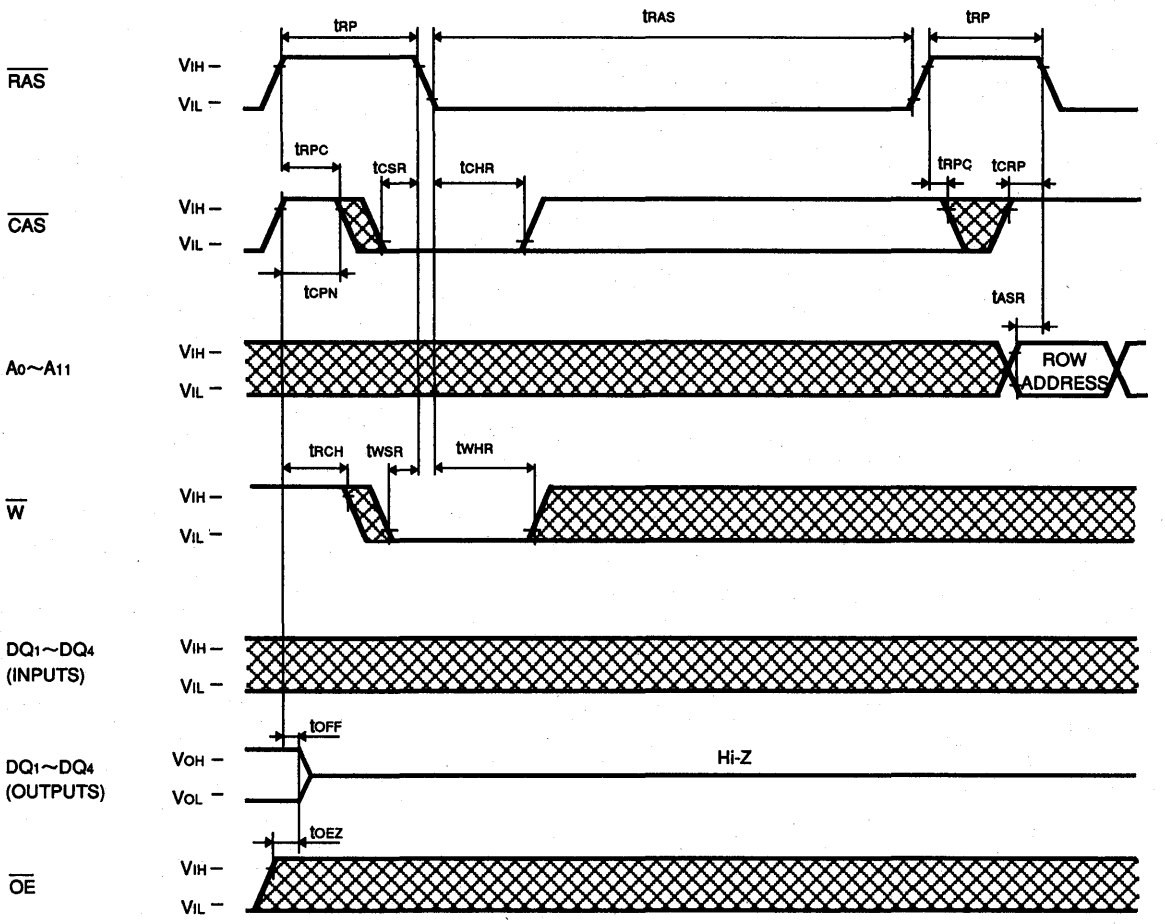
Fast Page Mode Read-Write,Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle (Note 29)



Note 29: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416400CXX-5,-5S	50	13	25	13	90	495
M5M416400CXX-6,-6S	60	15	30	15	110	405
M5M416400CXX-7,-7S	70	20	35	20	130	340

XX=J,TP

- Standard 26pin SOJ, 26pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 2.2mW (Max)* ---------- CMOS Input level
- Low operating power dissipation
  - M5M416400Cxx-5,-5S ---------- 605.0mW (Max)
  - M5M416400Cxx-6,-6S ---------- 495.0mW (Max)
  - M5M416400Cxx-7,-7S ---------- 415.0mW (Max)
- Self refresh capability *
  - self refresh current ---------- 200.0 μA(Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0~A_{11})

  *Applicable to self refresh version(M5M416400CJ,TP-5S,-6S,-7S :option) only

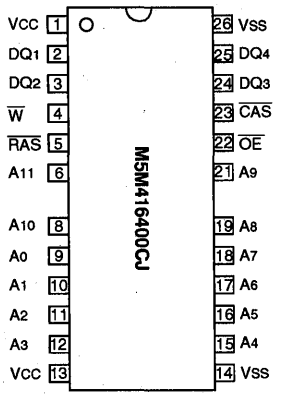
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

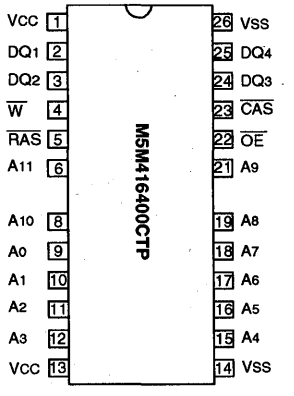
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_4	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

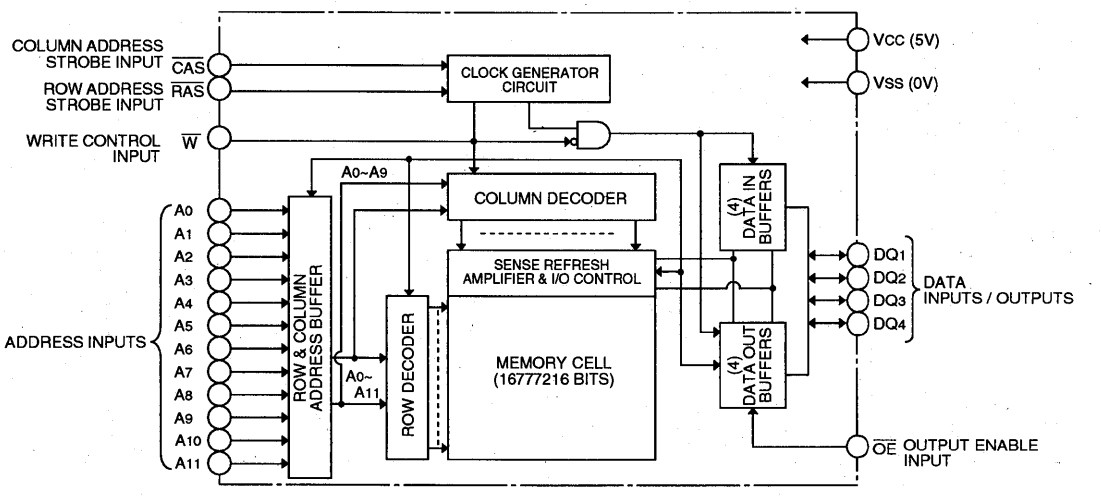
The M5M416400CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25℃	1000	mW
Topr	Operating temperature		0 ~ 70	℃
Tstg	Storage temperature		-65 ~ 150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
**: V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦5.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M416400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			110	mA
		M5M416400C-6,-6S	t_{RC}=t_{WC}=min.			90	
		M5M416400C-7,-7S	output open			75	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M416400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH}			110	mA
		M5M416400C-6,-6S	t_{RC}=min.			90	
		M5M416400C-7,-7S	output open			75	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M416400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			80	mA
		M5M416400C-6,-6S	t_{PC}=min.			70	
		M5M416400C-7,-7S	output open			60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			110	mA
		M5M416400C-6,-6S	t_{RC}=min.			90	
		M5M416400C-7,-7S	output open			75	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70℃, V_{CC}=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

MITSUBISHI ELECTRIC

PRELIMINARY
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SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.
6:Measured with a load circuit equivalent to 2TTL loads and 100pF.
7:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max).
8:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
9:Assumes that tRAD≧tRAD(max) and tASC≦tASC(max).
10:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT≦|±10μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.
13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).
15:tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
16:tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
17:Either tDZC or tDZO must be satisfied.
18:Either tCDD or tODD must be satisfied.
19:tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

PRELIMINARY
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Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 21)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 22)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 21: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.

22: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits						Unit
			M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 25)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

25: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
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SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	M5M416400C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}\&\overline{WE} \leqq 0.2V$ or $\overline{OE}\&\overline{WE} \geqq Vcc-0.2V$ $A_0 \sim A_{11} \leqq 0.2V$ or $A_0 \sim A_{11} \geqq Vcc-0.2V$ t_{REF}=128ms (4096cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~500ns			500	μA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M416400C (S)	$\overline{RAS}$ = $\overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

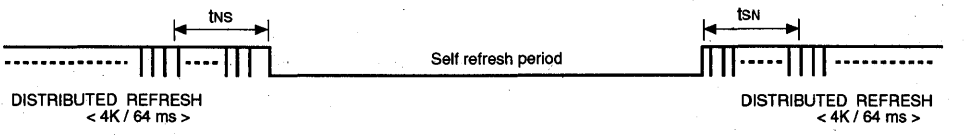
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M416400C-5S		M5M416400C-6S		M5M416400C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

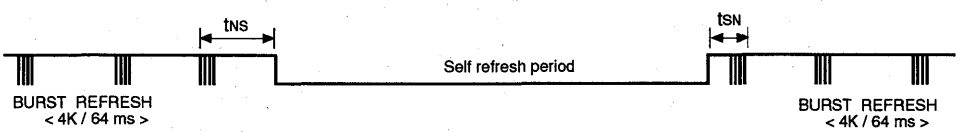
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64ms$ and $t_{SN} \leqq 64ms$.



(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 64ms$.



PRELIMINARY
Notice: This is not a final specification.
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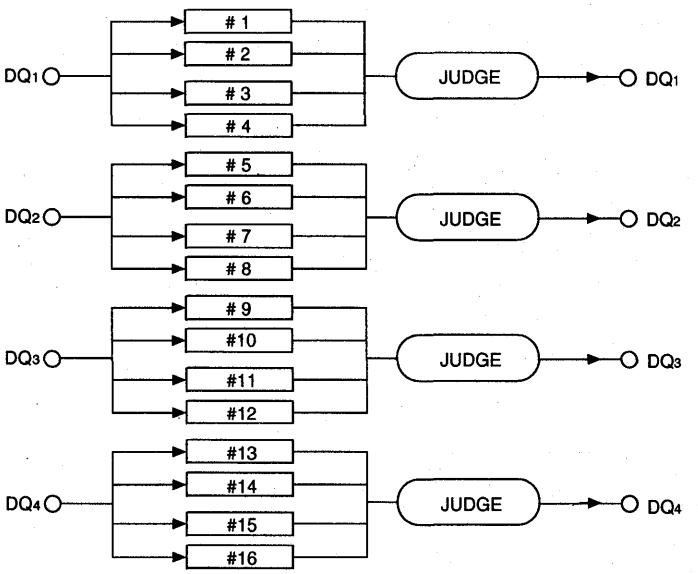
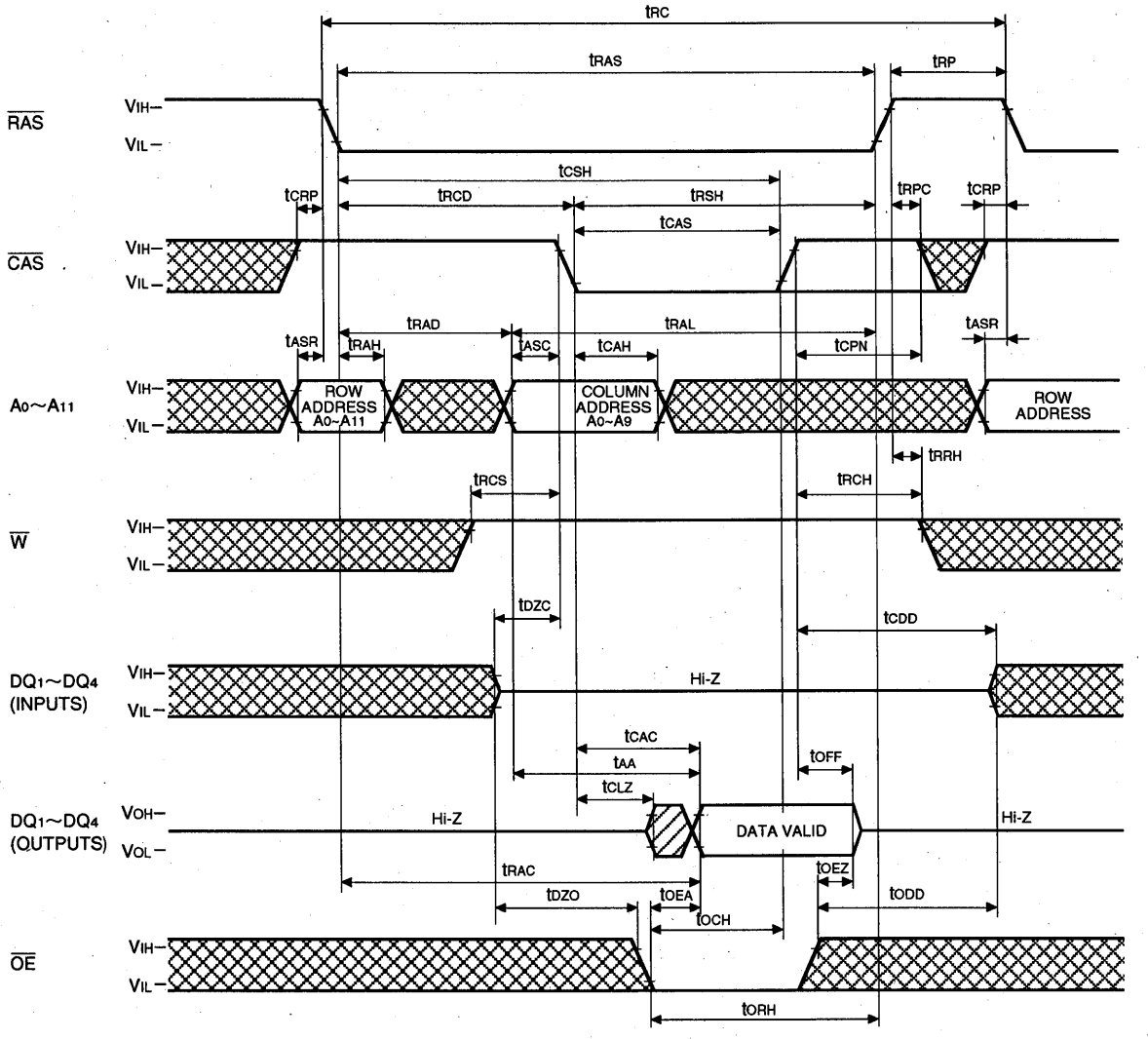
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M416400C-5,-5S		M5M416400C-6,-6S		M5M416400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0, CA_1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 28)
Read Cycle

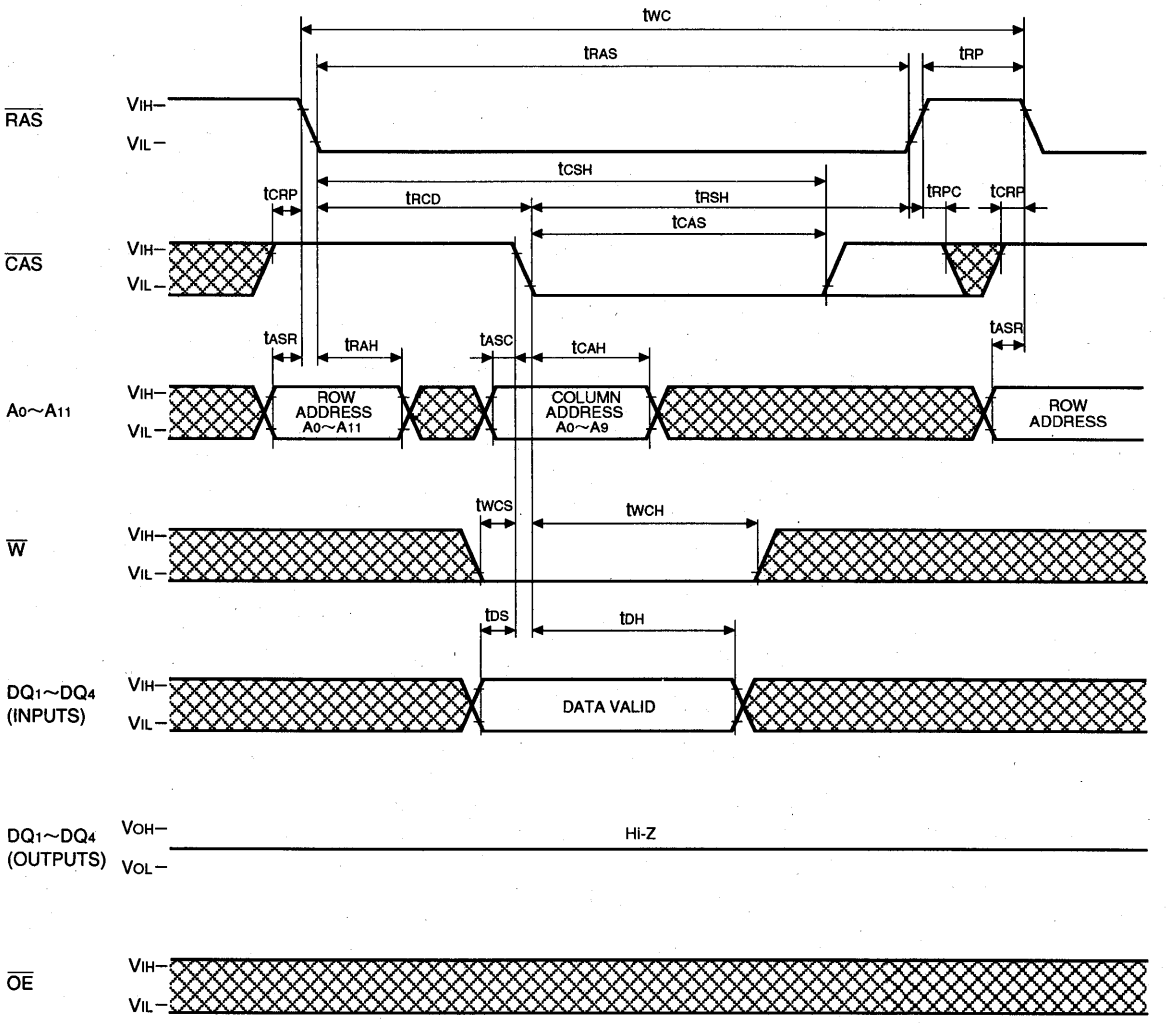


Note 28

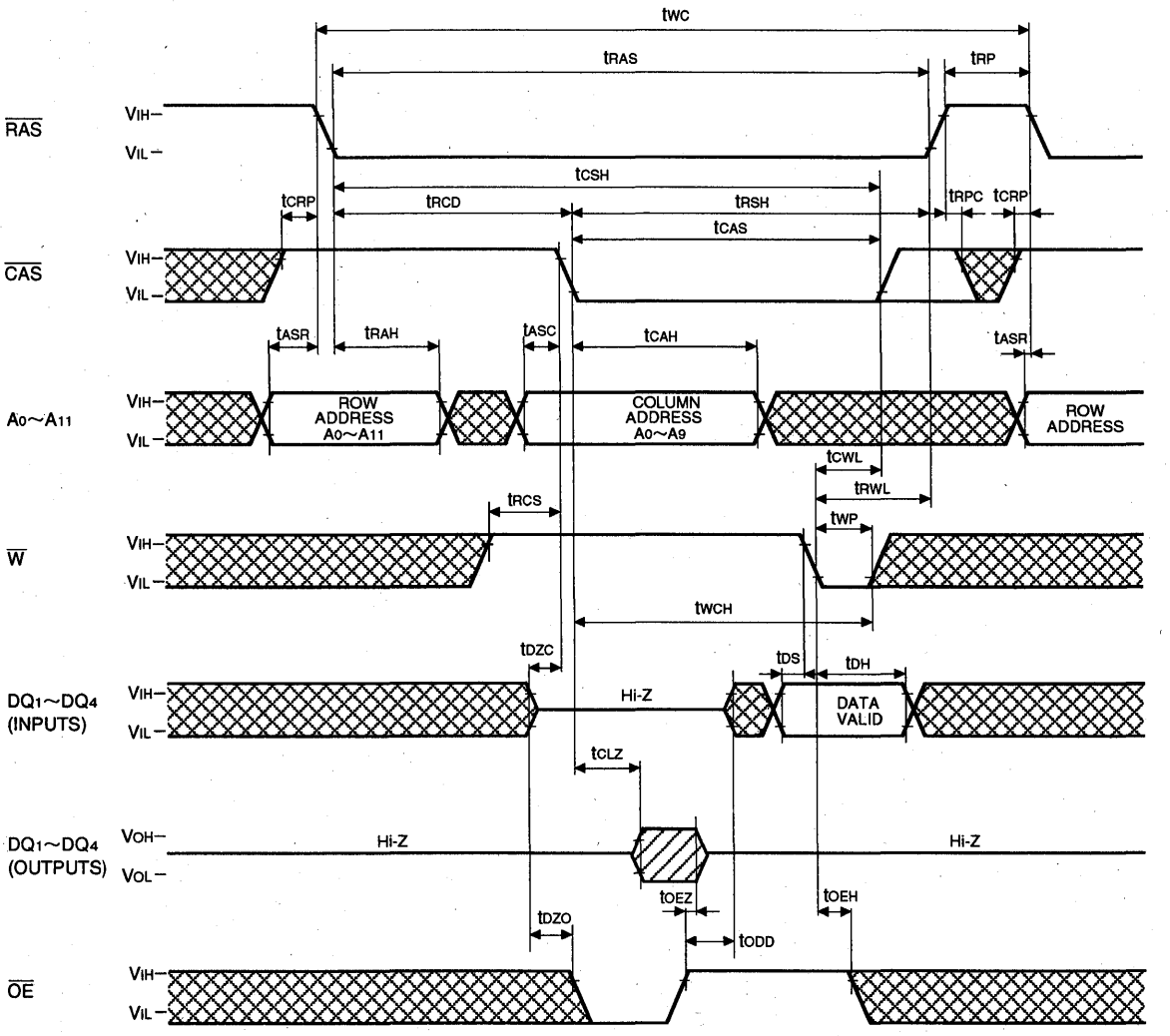
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

Write Cycle (Early write)



Write Cycle (Delayed write)



PRELIMINARY
Notice: This is not a final specification.
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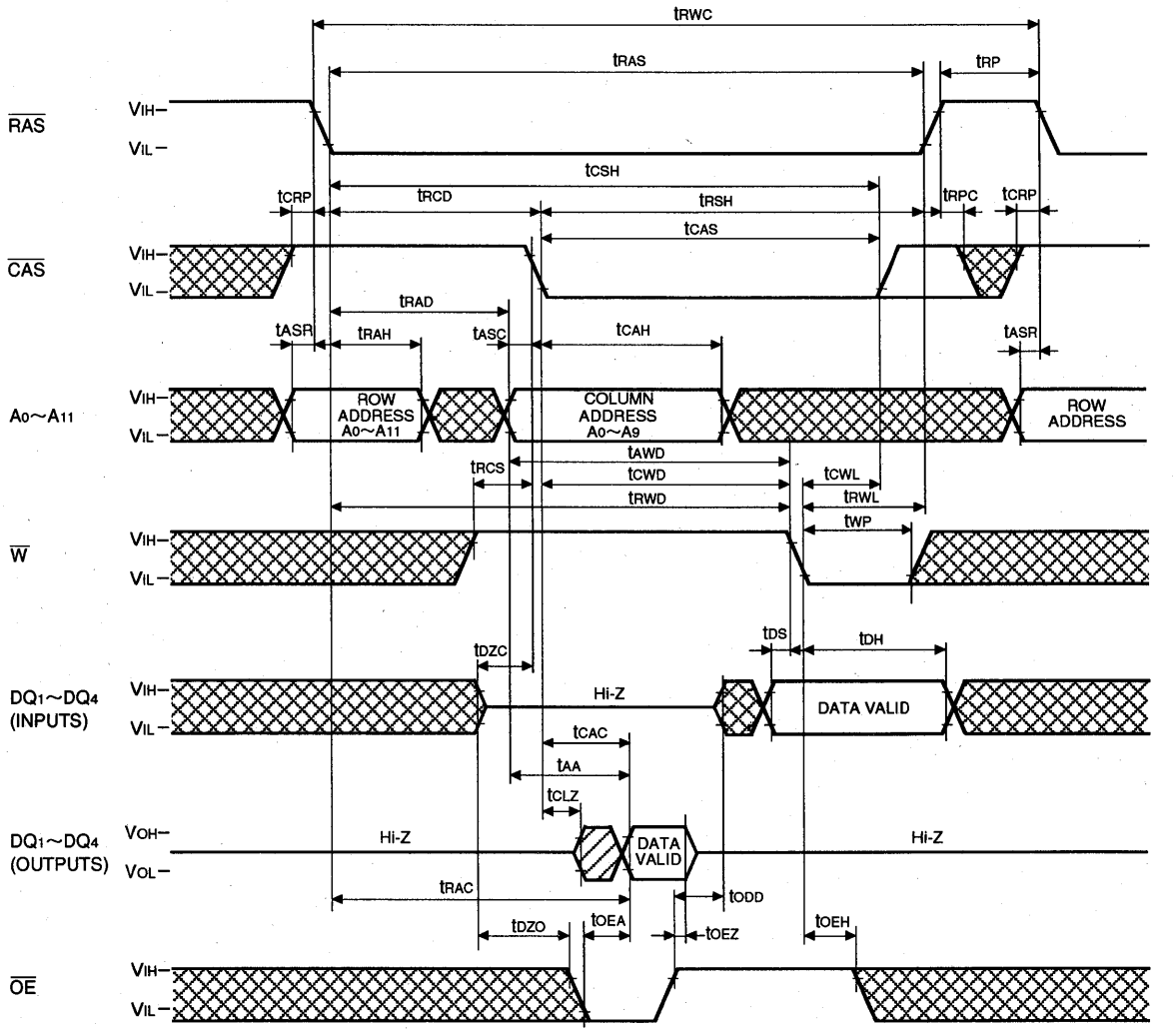
Read-Write, Read-Modify-Write Cycle



PRELIMINARY
Notice: This is not a final specification.
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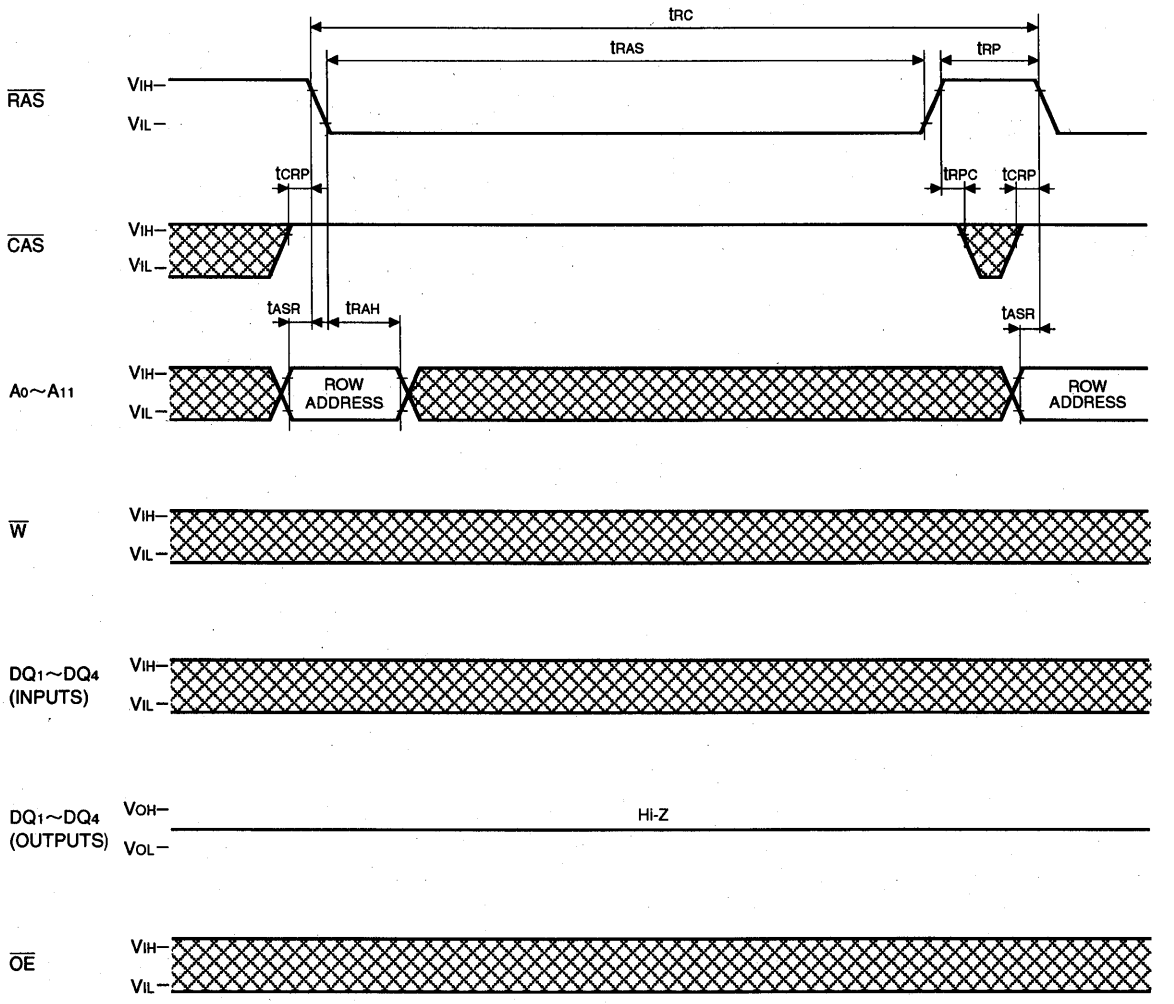
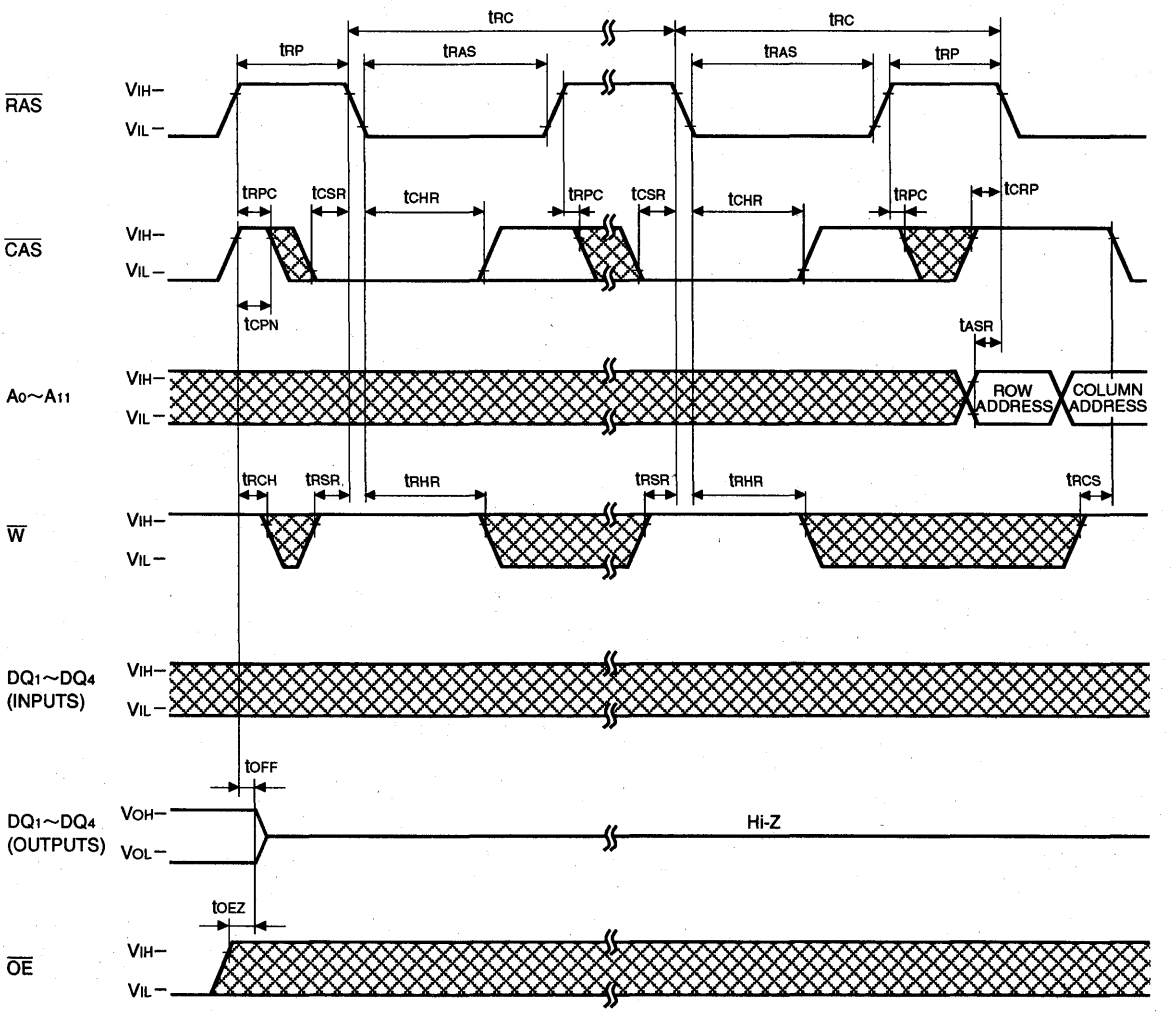
$\overline{RAS}$-only Refresh Cycle

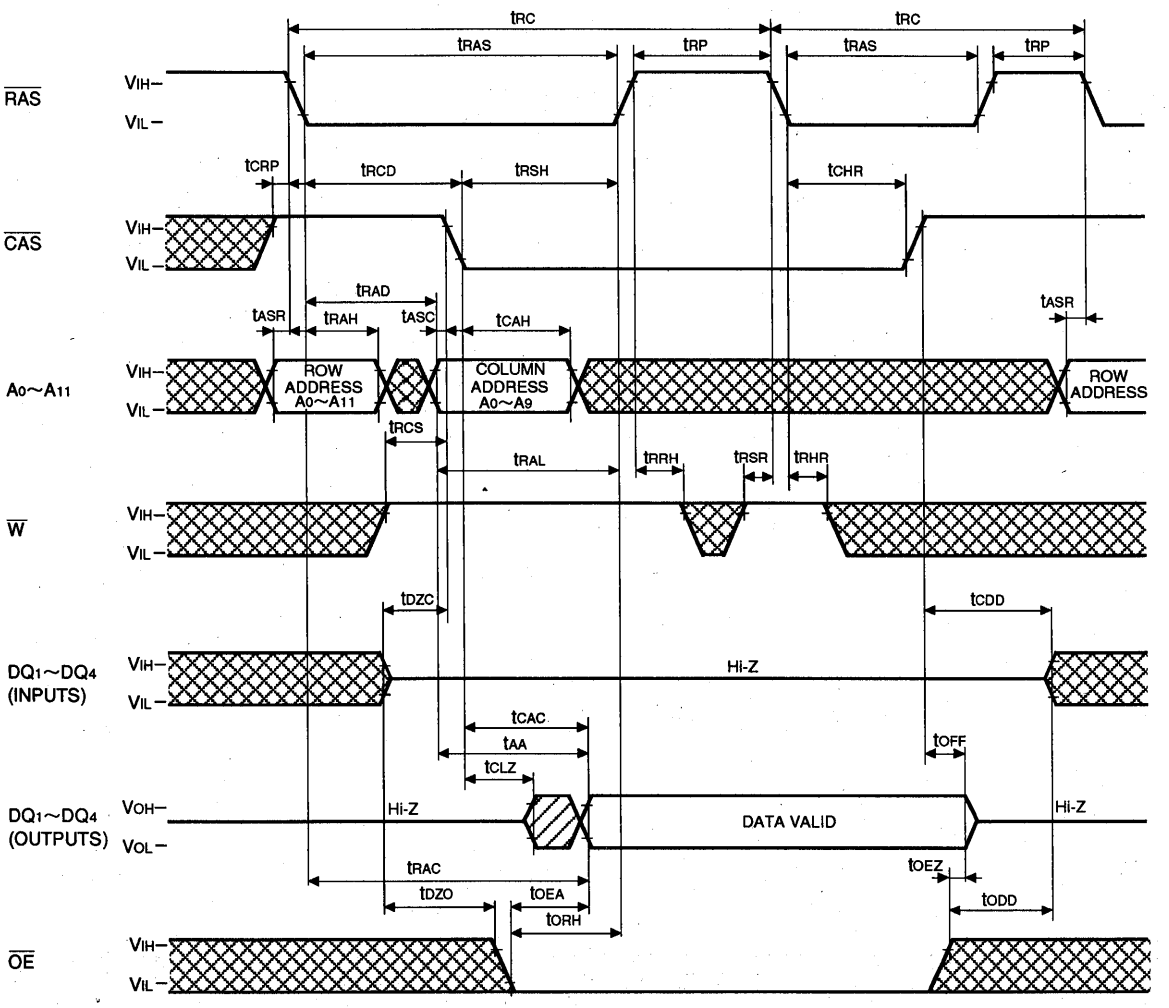


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAS before RAS Refresh Cycle, Slow Refresh Cycle



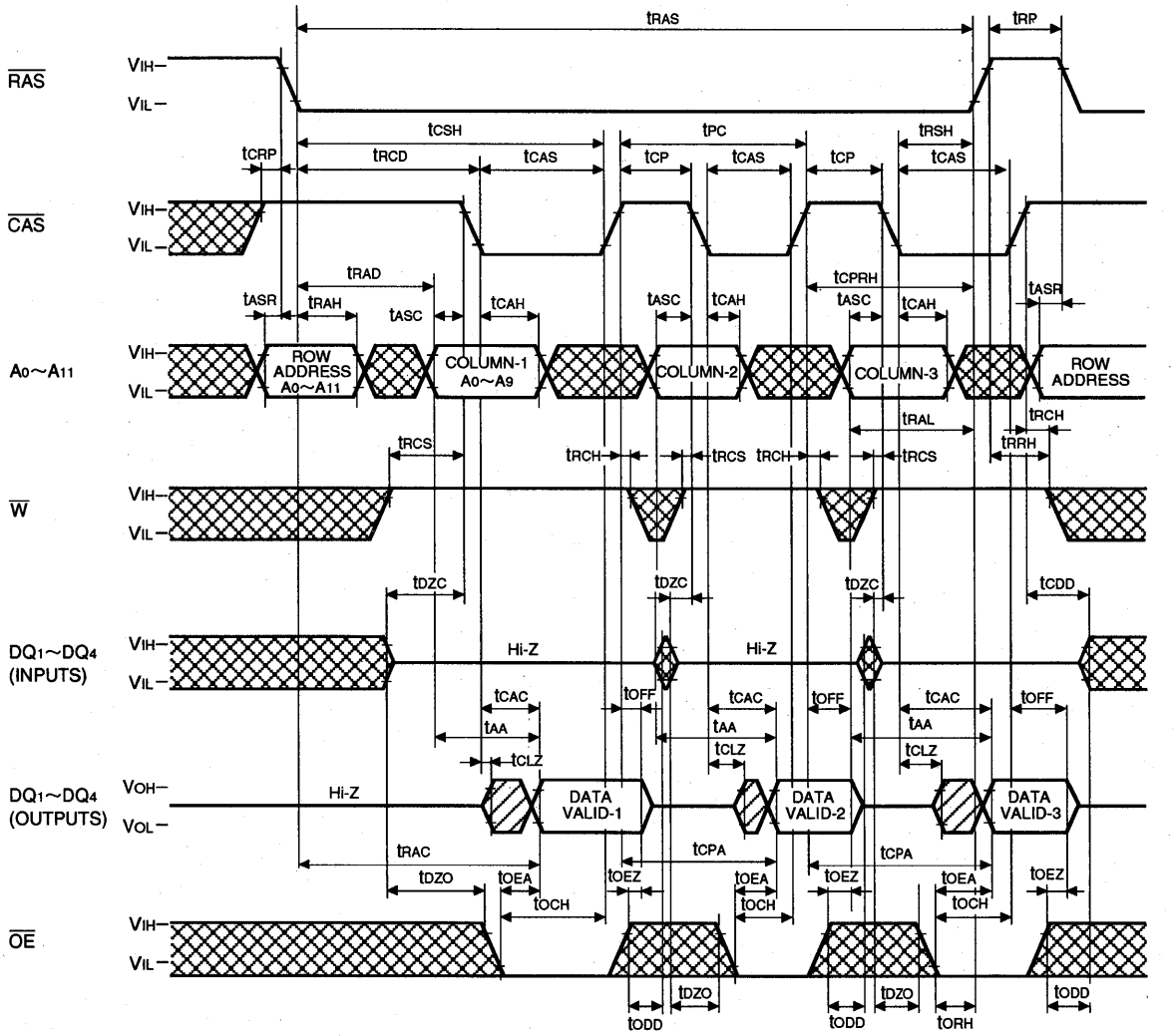
Hidden Refresh Cycle (Read) (Note 29)



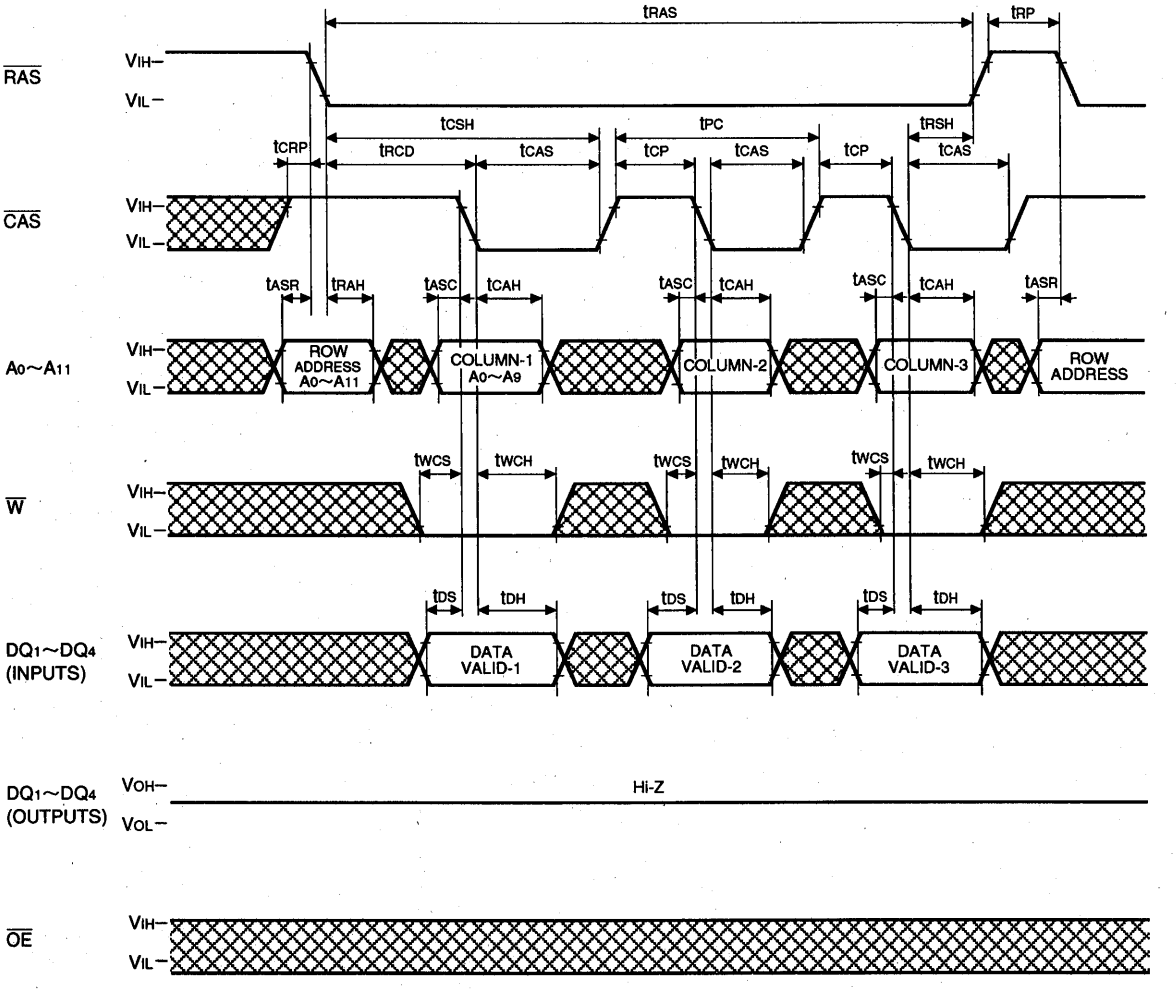
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle

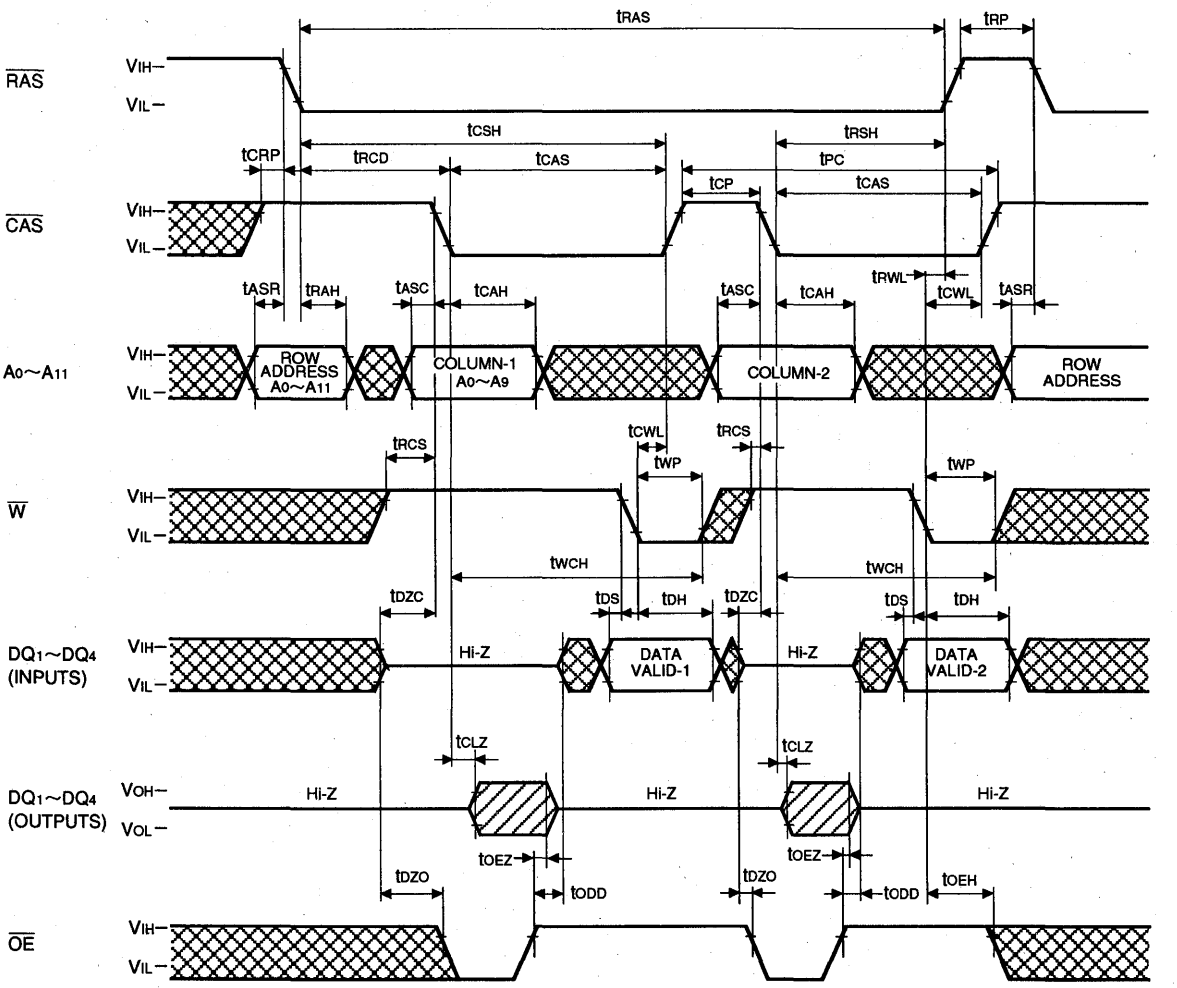


Fast Page Mode Write Cycle (Early Write)

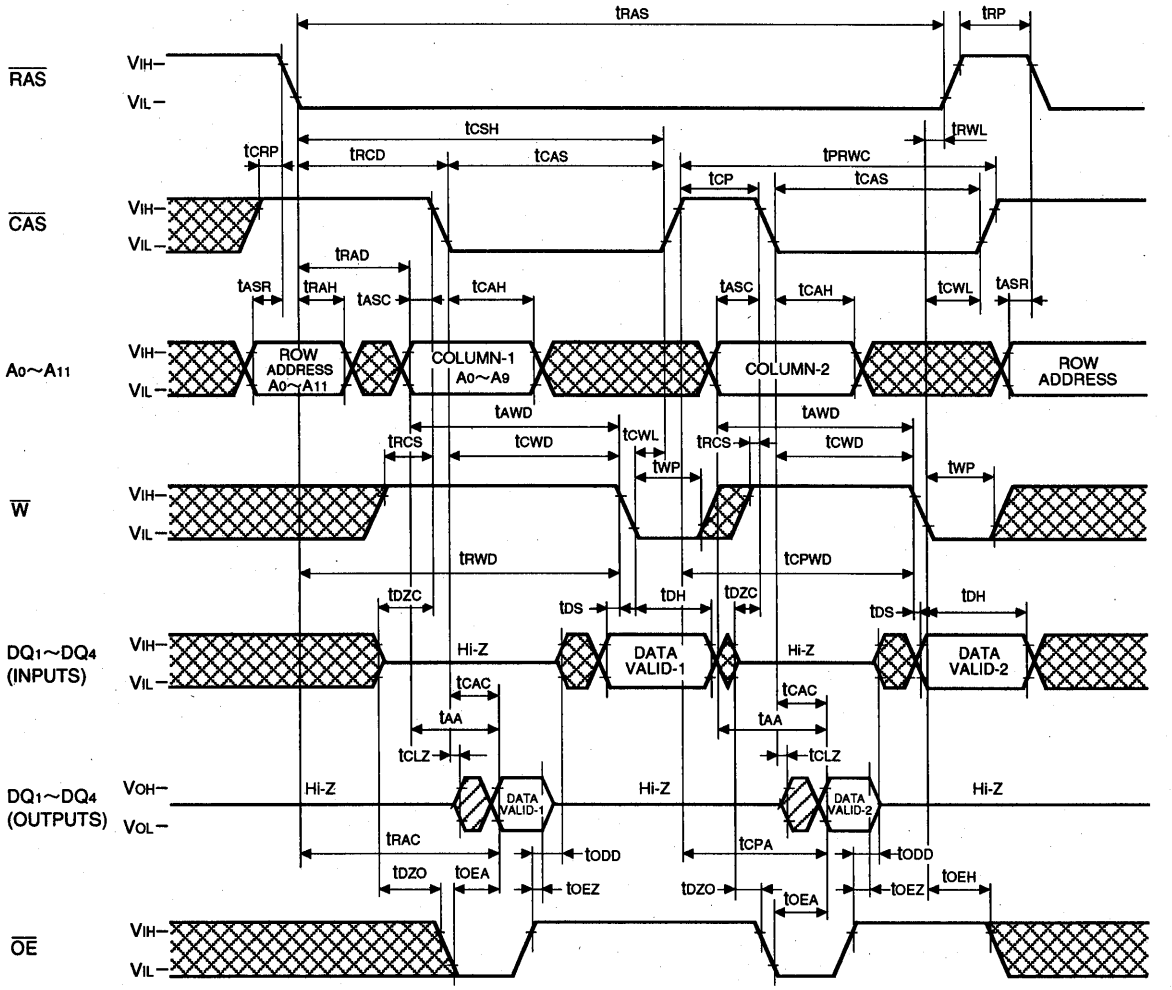


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast-Page Mode Write Cycle (Delayed Write)

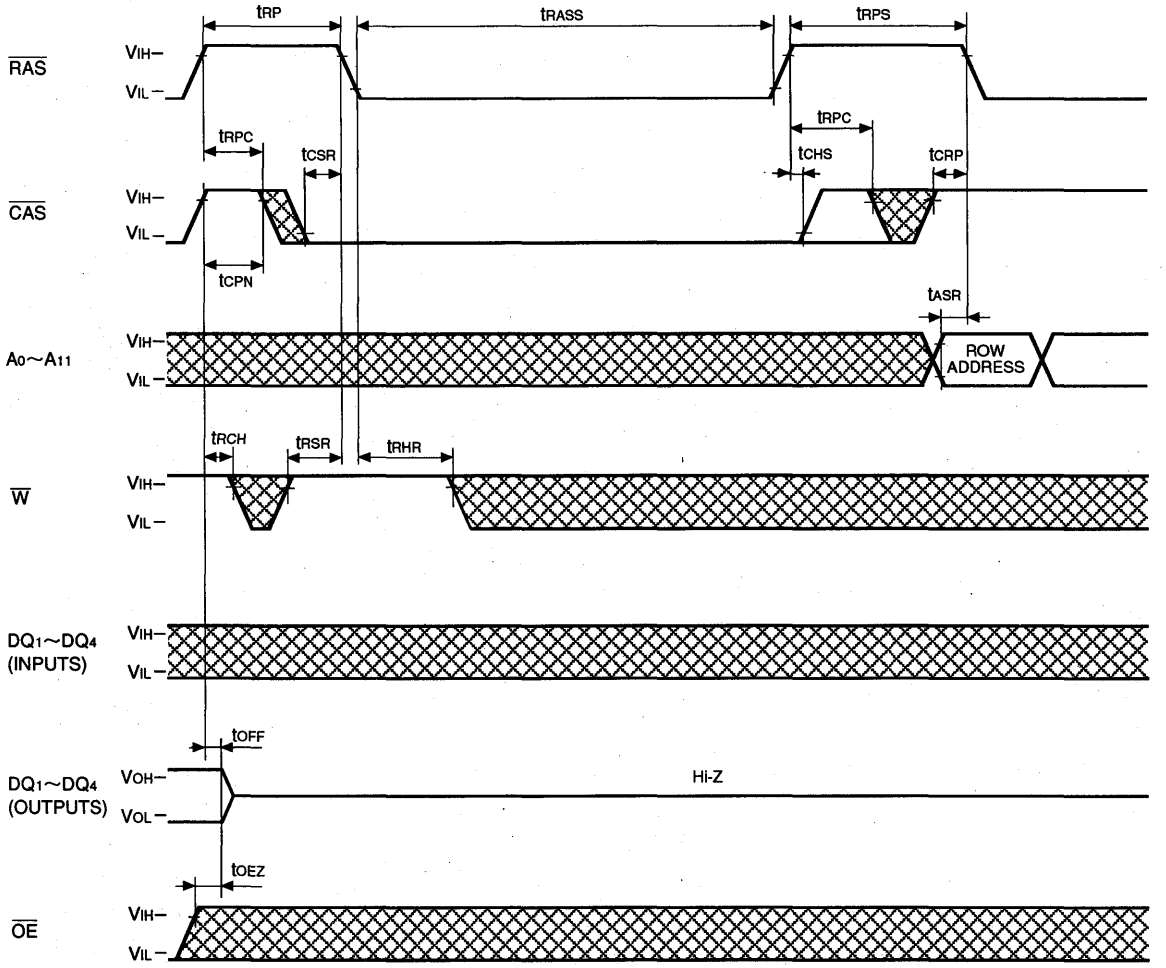


Fast Page Mode Read-Write,Read-Modify-Write Cycle

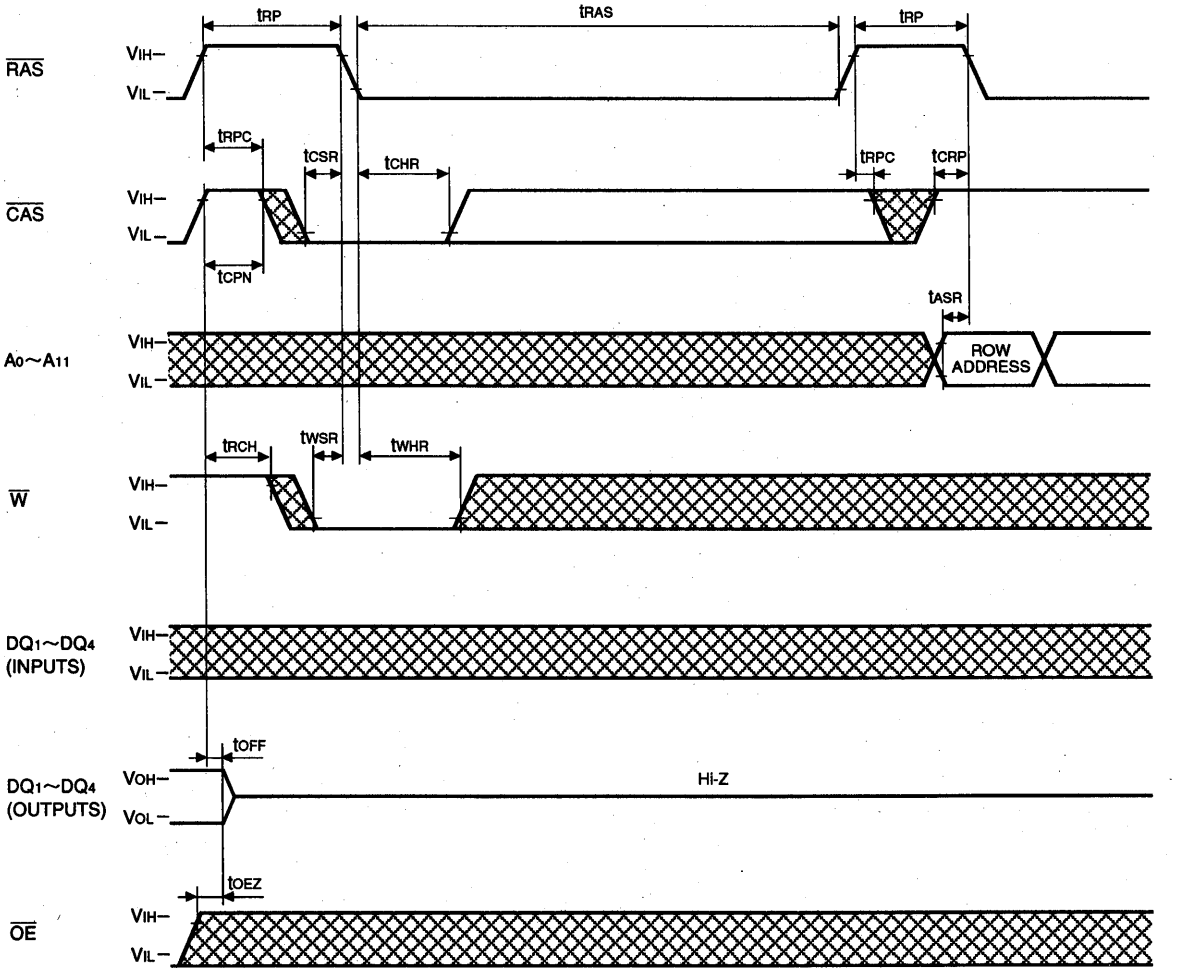


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle



TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416405CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416405CXX-5,-5S	50	13	25	13	90	495
M5M416405CXX-6,-6S	60	15	30	15	110	405
M5M416405CXX-7,-7S	70	20	35	20	130	340

XX=J,TP

- Standard 26pin SOJ, 26pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 2.2mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M416405Cxx-5,-5S ---------- 605mW (Max)
  - M5M416405Cxx-6,-6S ---------- 495mW (Max)
  - M5M416405Cxx-7,-7S ---------- 415mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~ A_{11})

  *:Applicable to self refresh version (M5M416405CJ,TP-5S,-6S, -7S:option) only

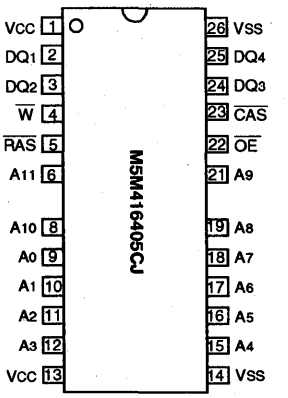
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

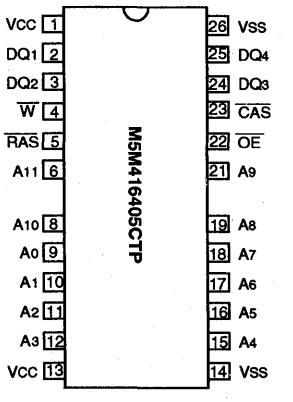
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

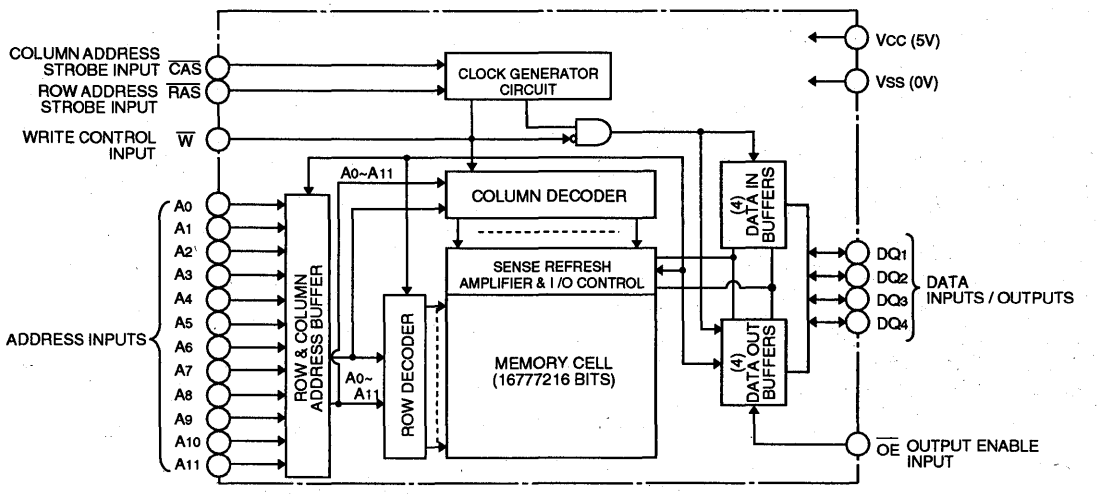
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M416405CJ, TP provides a number of other functions, e.g.,$\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M416405C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M416405C-6,-6S				90	
		M5M416405C-7,-7S				75	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M416405C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			110	mA
		M5M416405C-6,-6S				90	
		M5M416405C-7,-7S				75	
I_{CC4}(AV)	Average supply current from Vcc, Hyper Page Mode (Note 3,4,5)	M5M416405C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M416405C-6,-6S				115	
		M5M416405C-7,-7S				90	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M416405C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			110	mA
		M5M416405C-6,-6S				90	
		M5M416405C-7,-7S				75	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) , I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (|IOUT|≦±10 μ A) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT=2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper Page Mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 6)	**M5M416405C (S)**	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$≦0.2V $\overline{OE}$ & $\overline{WE}$≦0.2V or $\overline{OE}$ & $\overline{WE}$≧Vcc-0.2V A_0~ A_{11}≦0.2V or A_0~ A_{11}≧Vcc-0.2V t_{REF}=128ms (4096cycles) output=OPEN t_{RAS}=t_{RAS}min. ~500ns			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 6)	**M5M416405C (S)**	$\overline{RAS}$=$\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

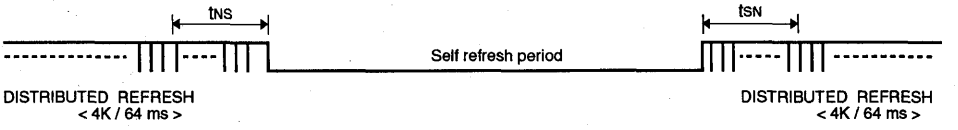
TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, see notes 14, 15)

Symbol	Parameter	Limits						Unit
		M5M416405C-5S		M5M416405C-6S		M5M416405C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

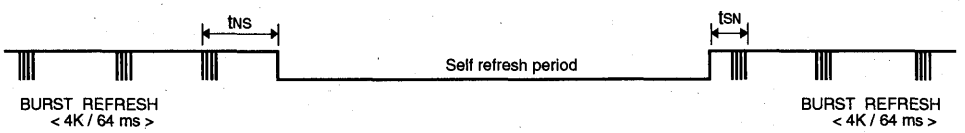
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦64ms and t_{SN}≦64ms.



(2) In case of burst refresh

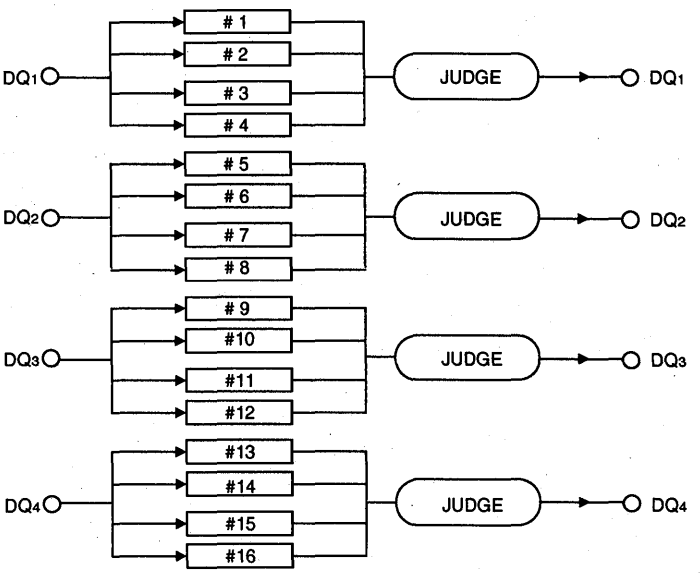
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}+t_{SN}≦64ms.



TEST Mode SET Cycle (Note 31)

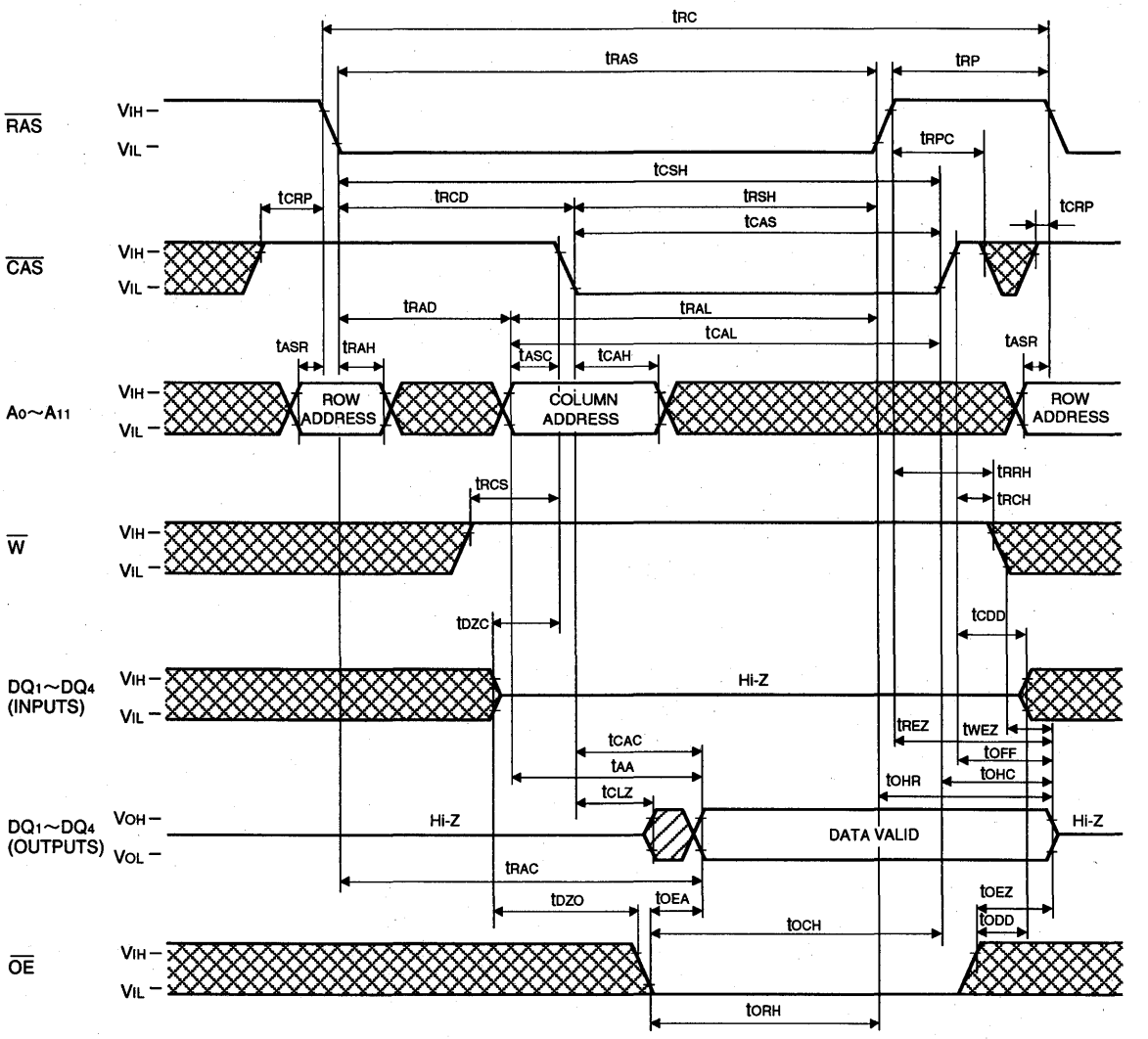
Symbol	Parameter	Limits						Unit
		M5M416405C-5,-5S		M5M416405C-6,-6S		M5M416405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31:The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA 0 and CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 32)
Read Cycle



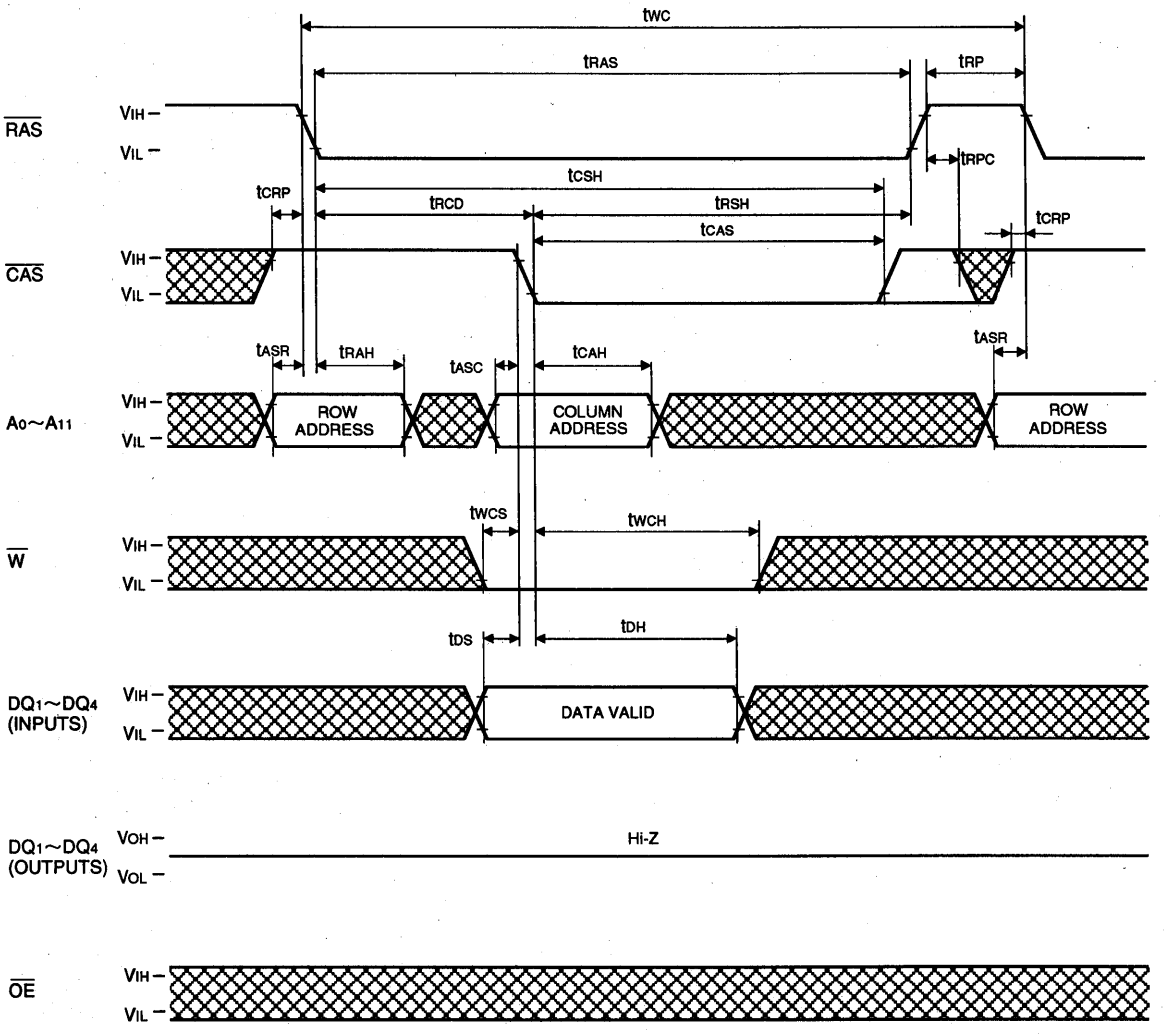
Note 32

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

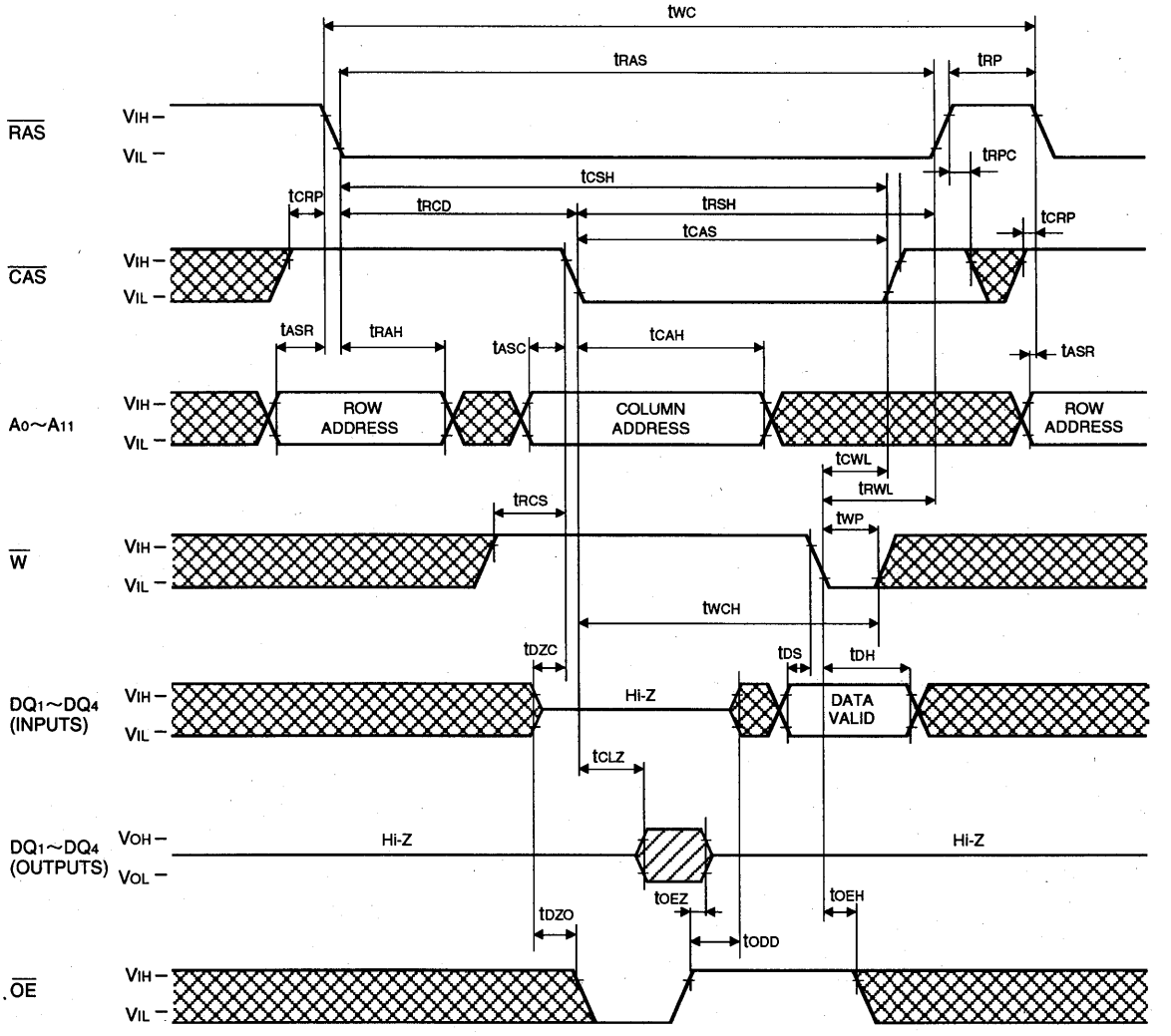
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Early Write Cycle



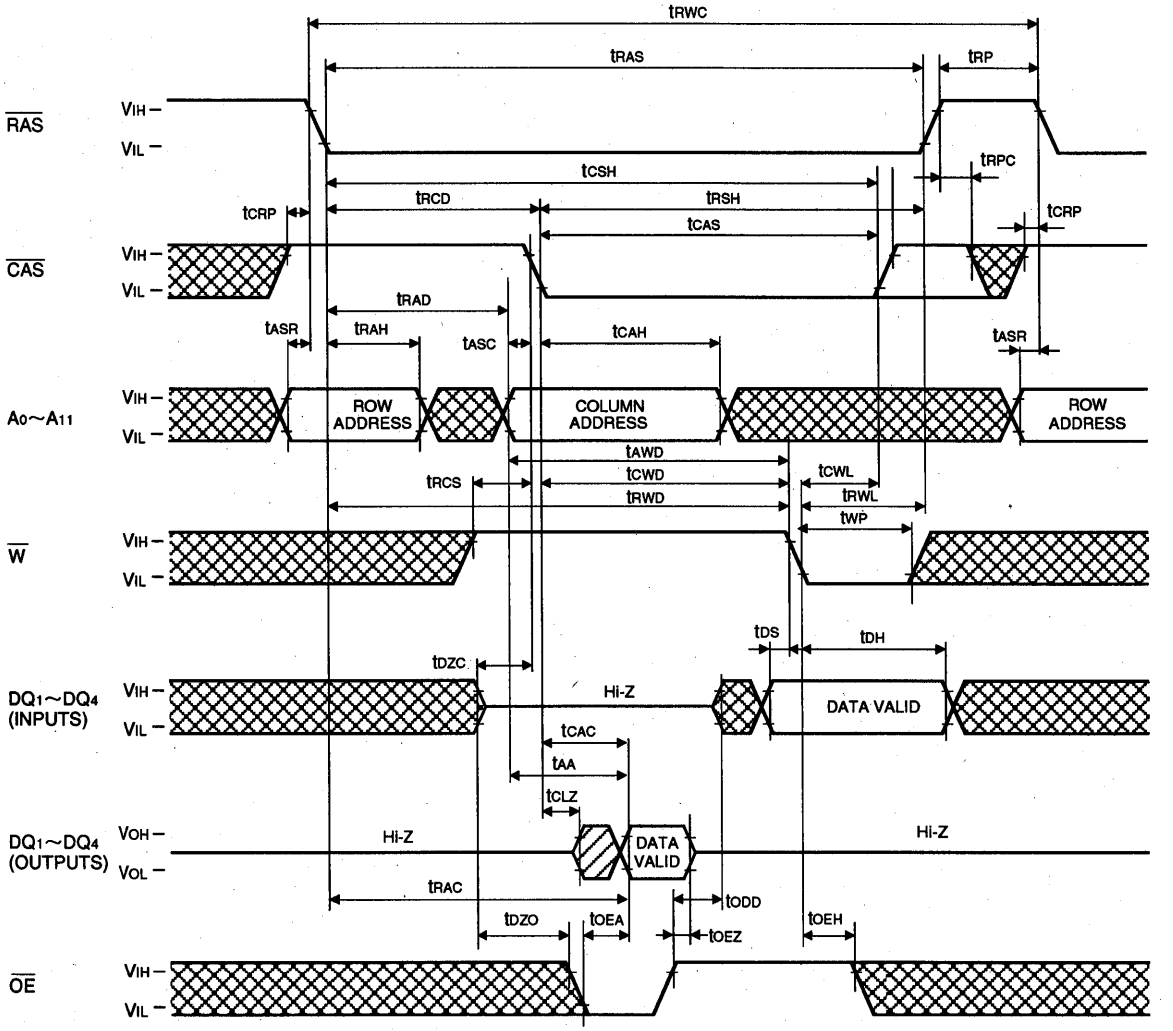
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Delayed Write Cycle



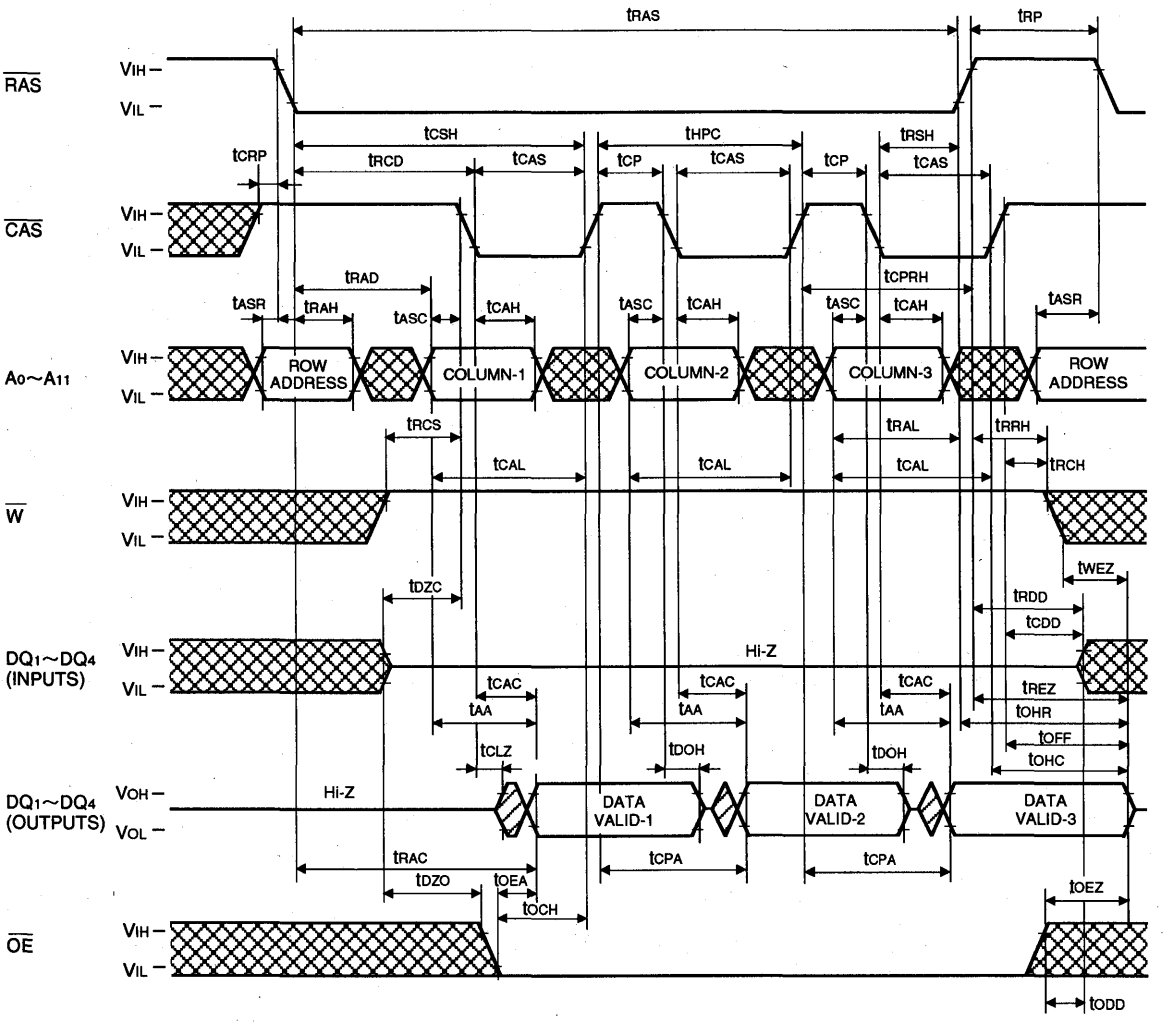
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle



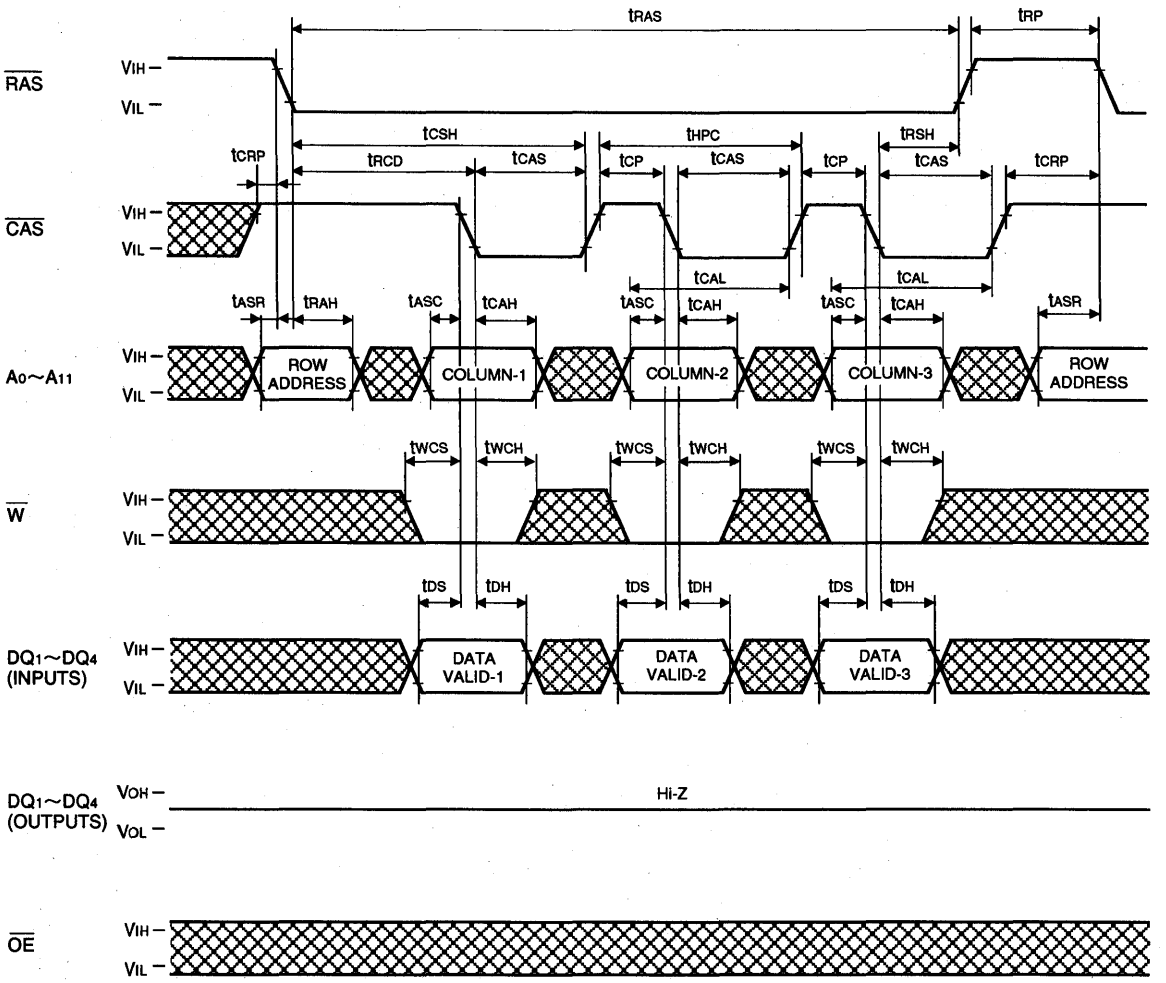
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle

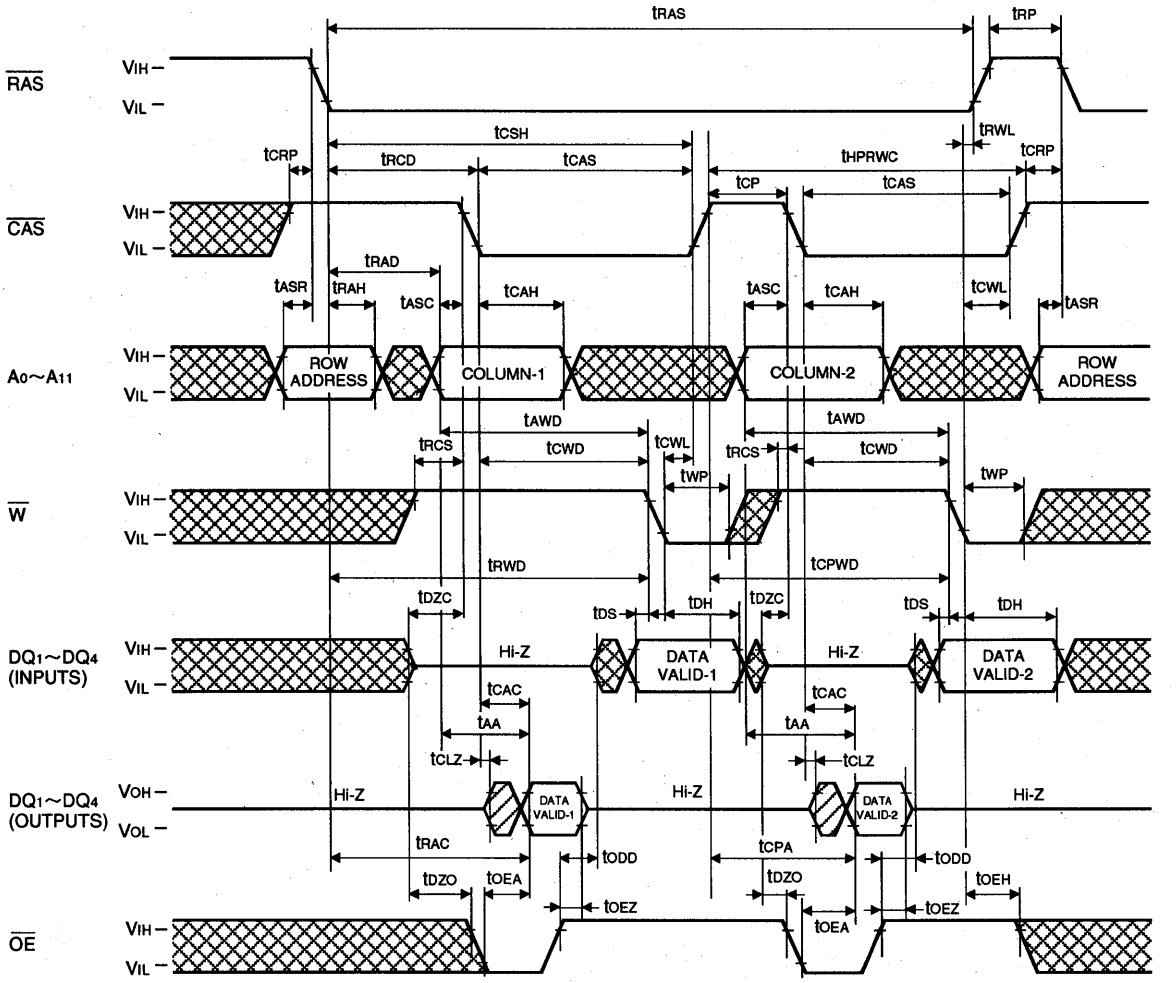


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Early Write Cycle

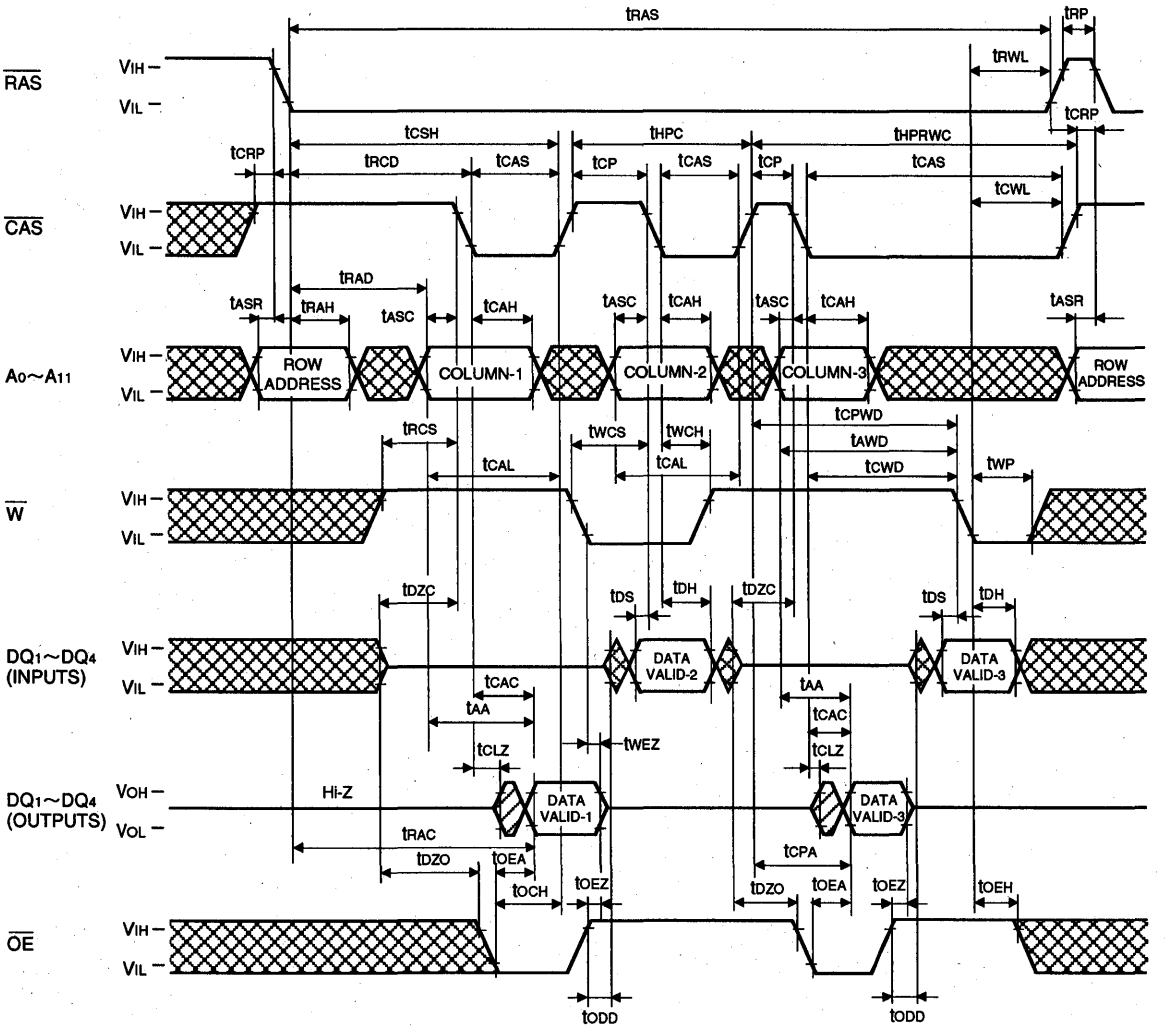


Hyper Page Mode Read-Write, Read-Modify-Write Cycle



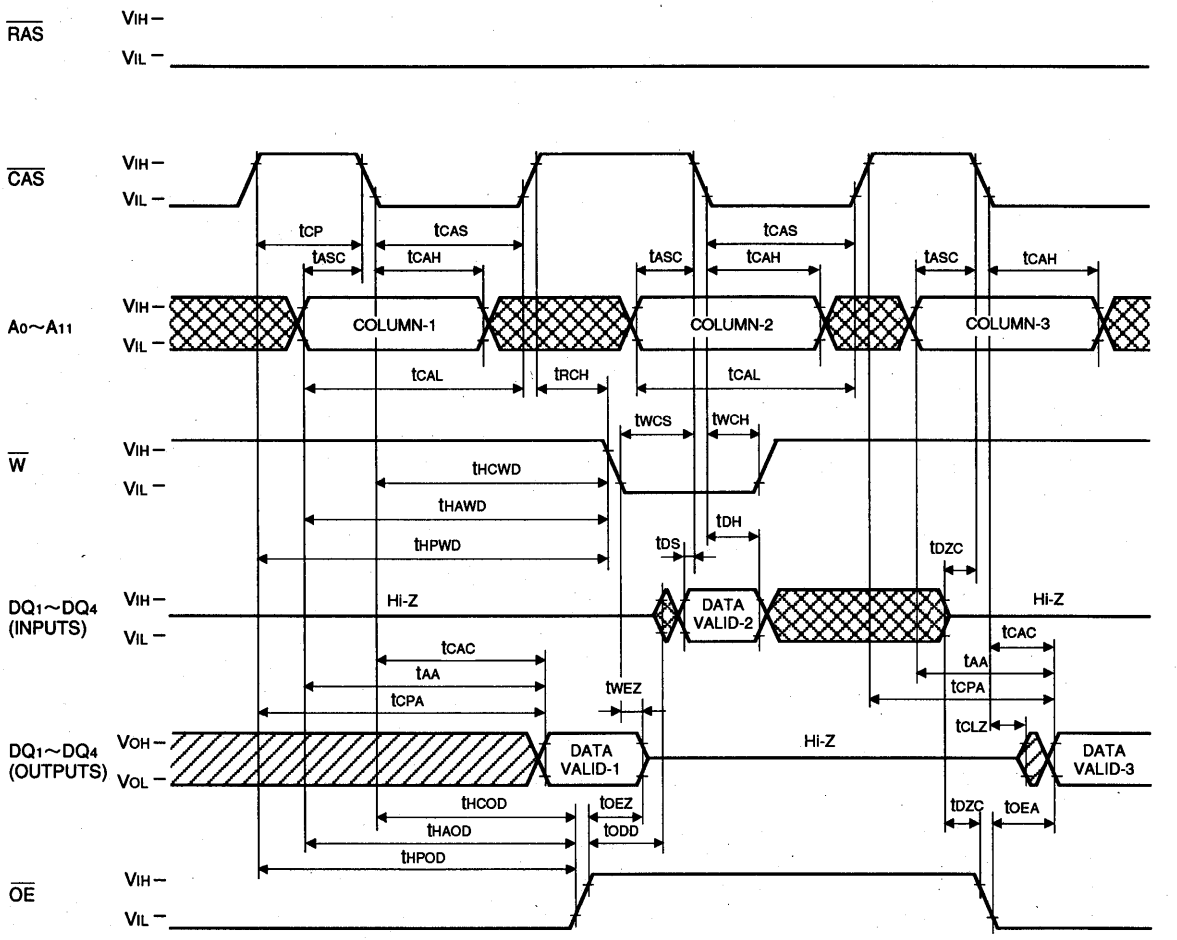
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (1)

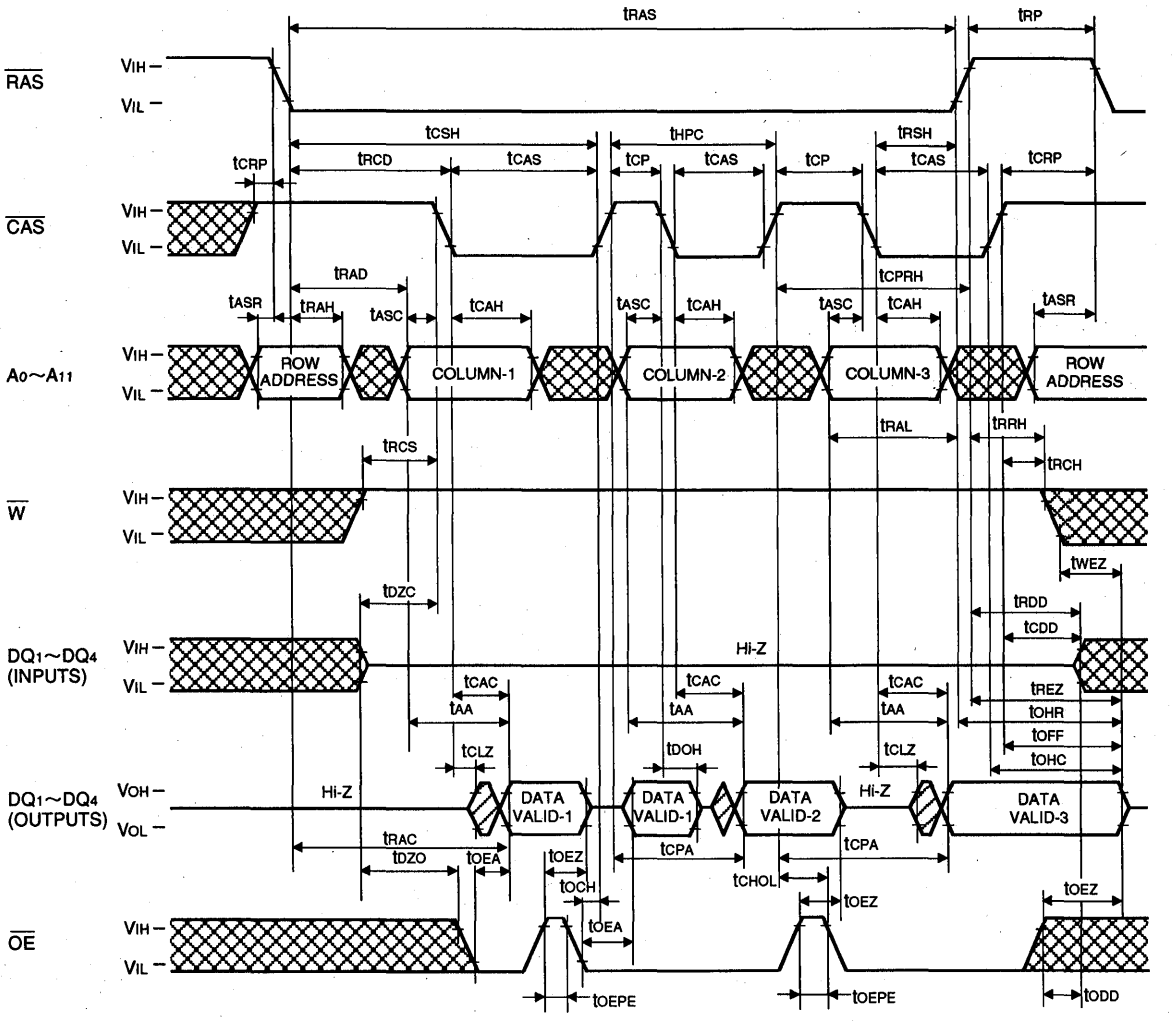


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

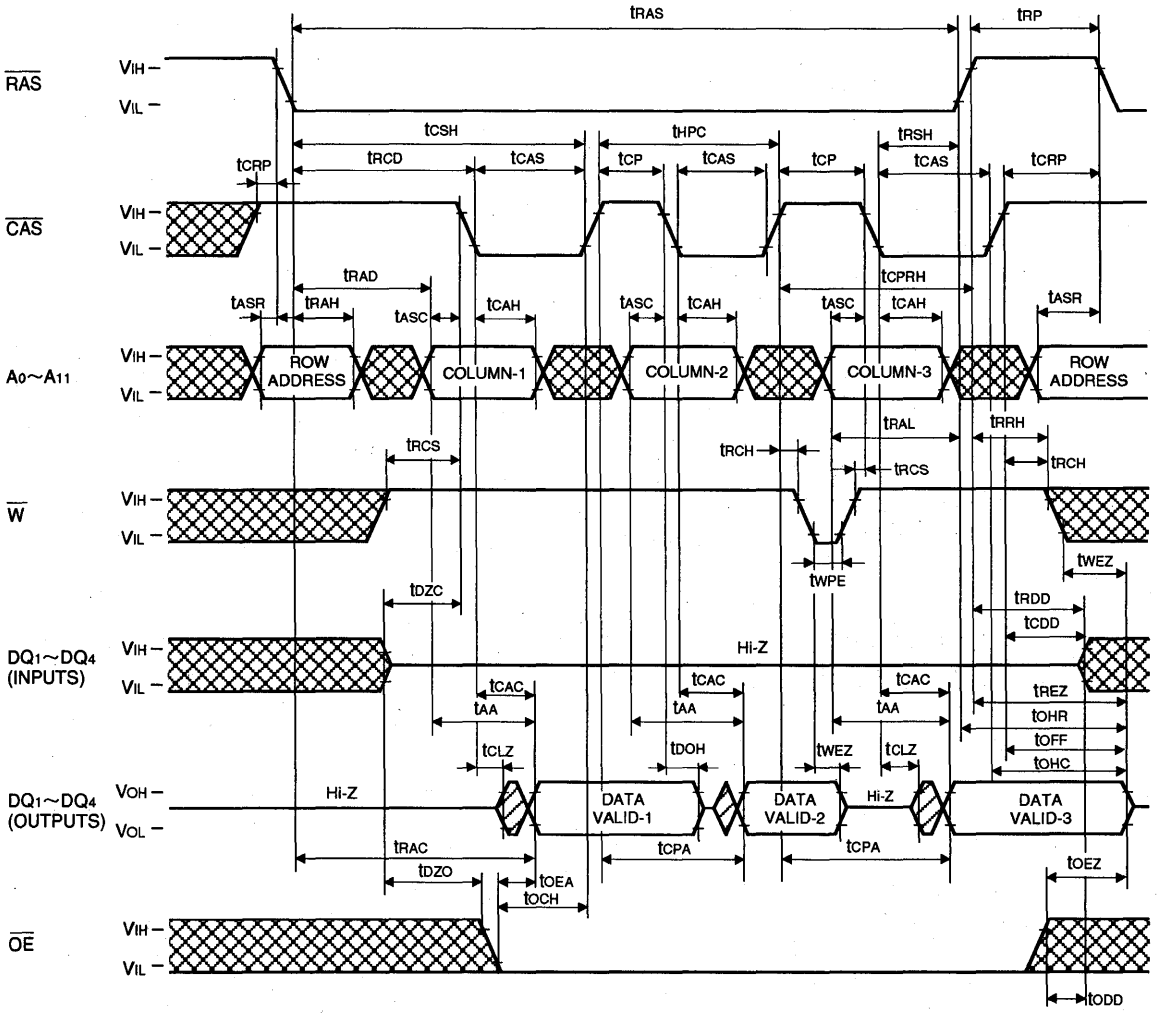
Hyper Page Mode Mix Cycle (2)



Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)

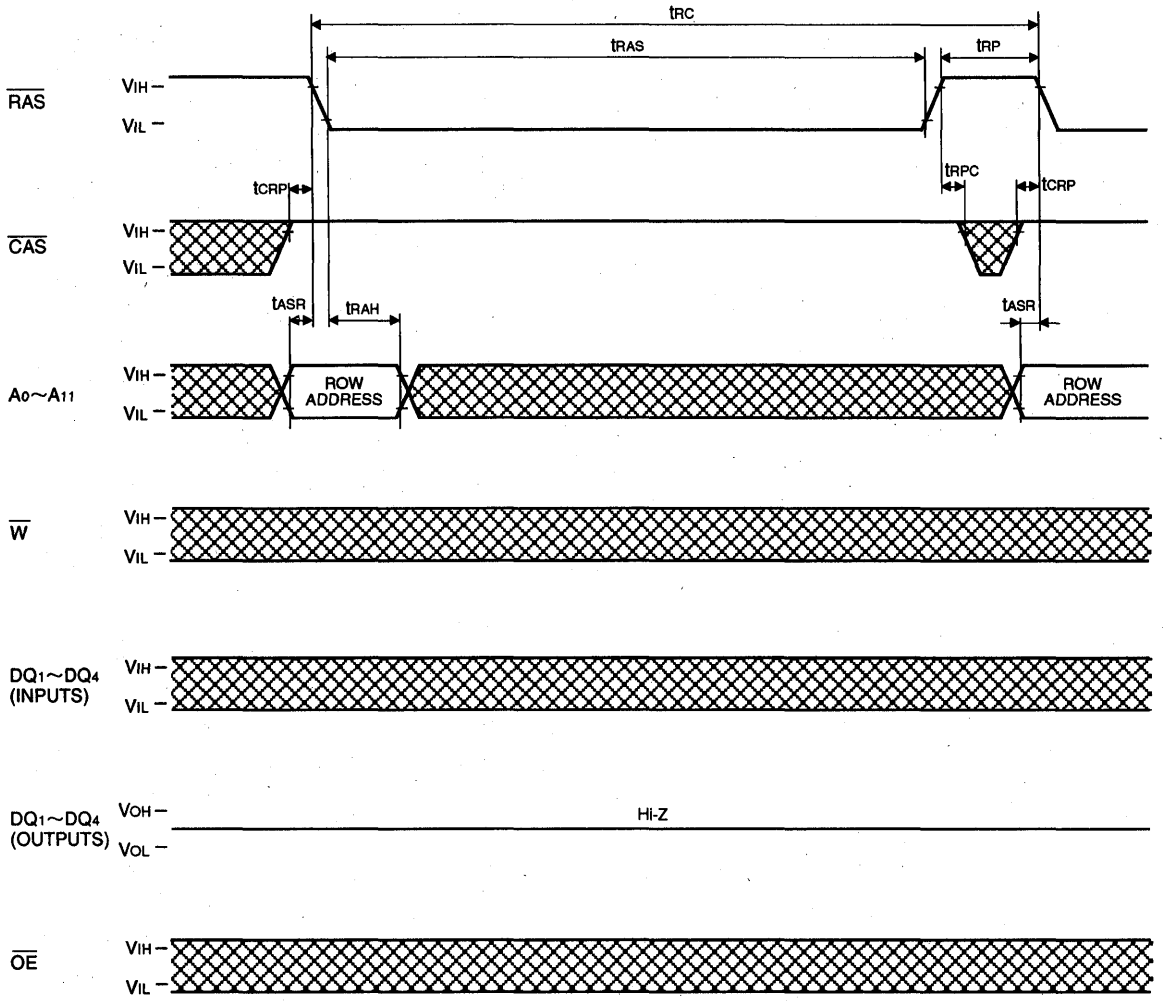


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

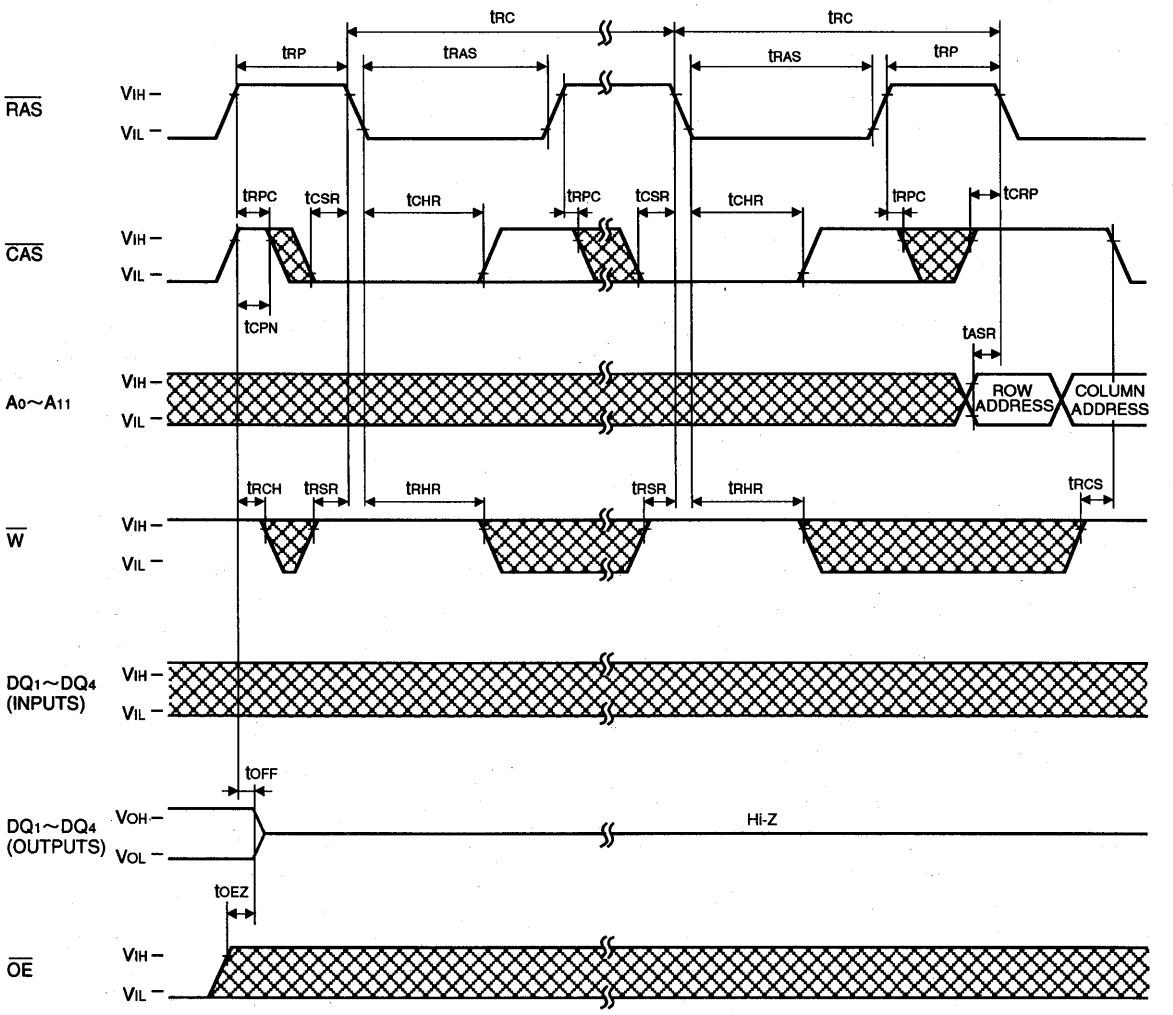


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

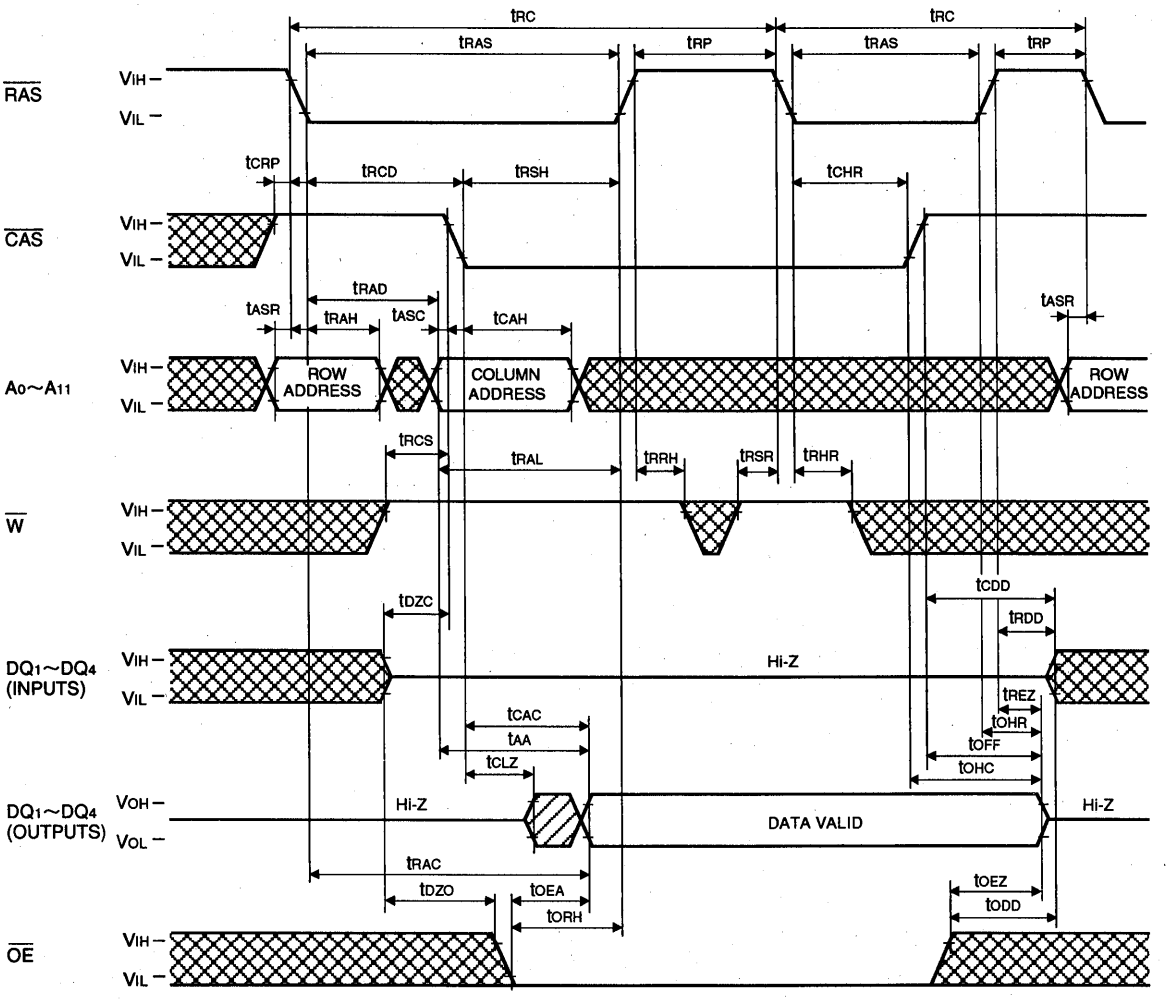
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

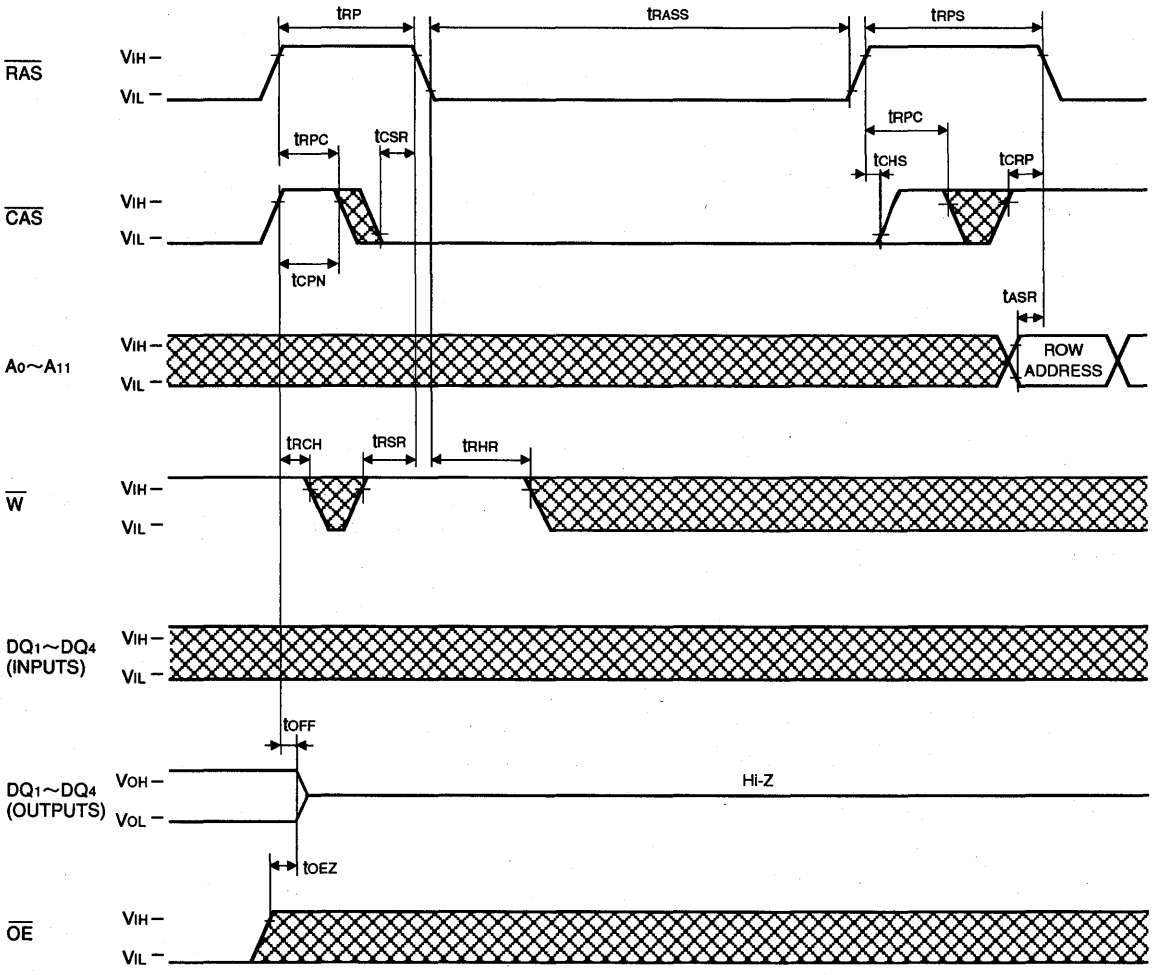


Hidden Refresh Cycle (Read) (Note 33)



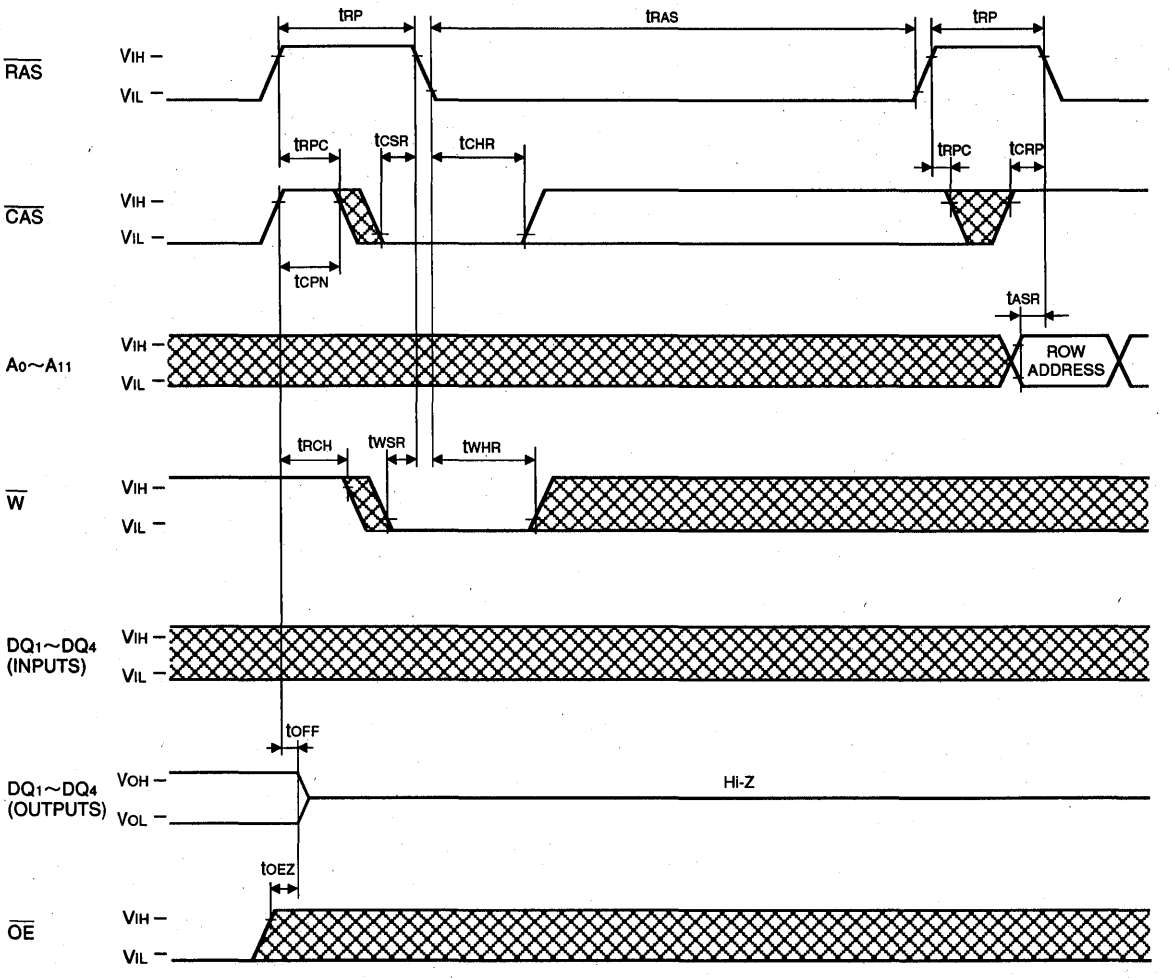
Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases t_{RSR} and t_{RHR} should be satisfied.

Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

M5M417400BJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417400BXX-5,-5S	50	13	25	13	90	655
M5M417400BXX-6,-6S	60	15	30	15	110	540
M5M417400BXX-7,-7S	70	20	35	20	130	475

XX=J,TP

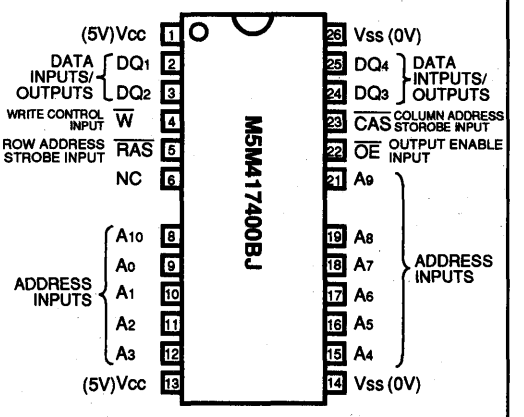
- Standard 26 pin SOJ,26 pin TSOP
- Single 5V ±10%supply
- Low stand-by power dissipation
  - M5M417400B ····· 5.5mW (Max)CMOS Input level
  - M5M417400B(S) ····· 2.2mW (Max)CMOS Input level
- Low operating power dissipation
  - M5M417400Bxx- 5,- 5S ····· 800.0mW (Max)
  - M5M417400Bxx- 6,- 6S ····· 660.0mW (Max)
  - M5M417400Bxx- 7,- 7S ····· 580.0mW (Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh and Self refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0 ~A_{10})
- 2048 refresh cycles every 128ms (A_0 ~A_{10}) *

  *: Applicable to self refresh version only

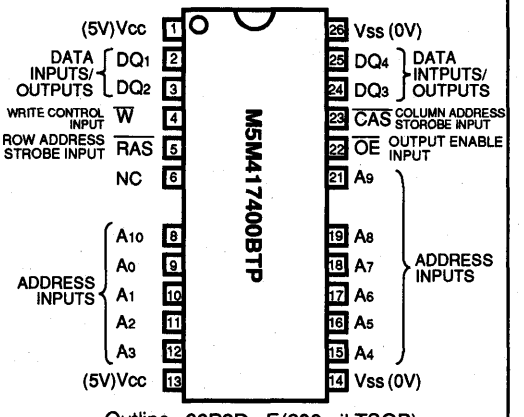
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D - B(300mil SOJ)



Outline 26P3D - E(300mil TSOP)

NC : NO CONNECTION

FUNCTION

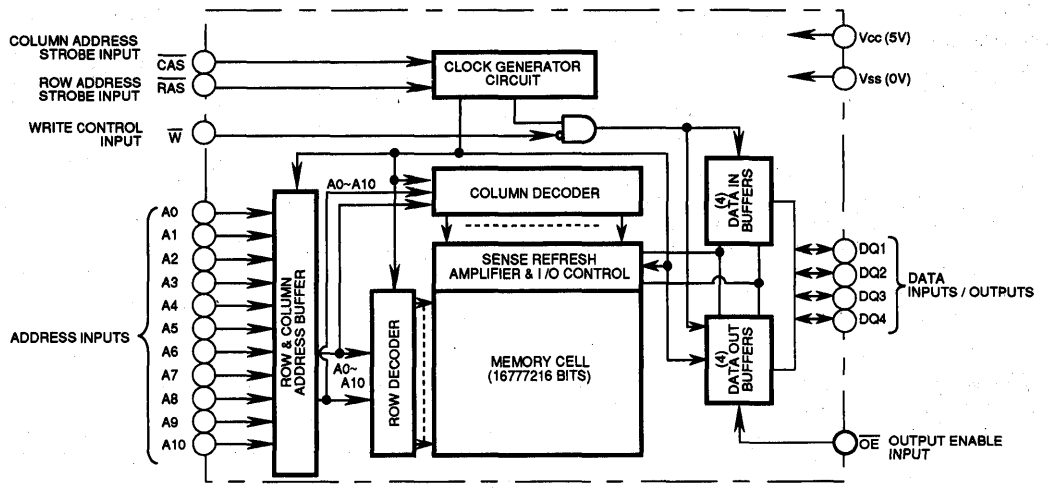
The M5M417400BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～ 7	V
V_I	Input voltage		-1～ 7	V
V_O	Output voltage		-1～ 7	V
Io	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～ 70	°C
Tstg	Storage temperature		-65～ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦ 6.0V, Other inputs pins=0V	-10		10	μA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4)	M5M417400B-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417400B-6,-6S				120	
		M5M417400B-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M417400B	$\overline{RAS}$= $\overline{CAS}$=$\overline{OE}$=$\overline{W}$=A_0～A_{10}≧Vcc -0.5V output open			1	
		M5M417400B(S)				0.4	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3)	M5M417400B-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417400B-6,-6S				120	
		M5M417400B-7,-7S				105	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M417400B-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M417400B-6,-6S				70	
		M5M417400B-7,-7S				60	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417400B-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417400B-6,-6S				120	
		M5M417400B-7,-7S				105	
$I_{CC8(AV)}$	Average supply current from Vcc Extended refresh (Note 5)	M5M417400B(S)	$\overline{RAS}$ cycling and $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A_0～A_{10}≦0.2V output open, t_{RC}=64 μs, t_{RAS}=t_{RAS}min～1 μs			0.5	mA
$I_{CC9\ (AV)}$	Average supply current from Vcc Self - Refresh cycle (Note 5)	M5M417400B(S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V, output open Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A_0～A_{10}≦0.2V			0.4	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
t_{AA}	Column address access time	(Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
8: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
9: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
10: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
11: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leq 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			32		32		32	ms
t_{REF}	Refresh cycle time *			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note18)	13		15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note18)	13		15		15		ns
t_T	Transition time	(Note19)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.
15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
17: Either t_{DZC} or t_{DZO} must be satisfied.
18: Either t_{CDD} or t_{ODD} must be satisfied.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note21)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note22)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note22)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note22)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 21: tRWC is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note24)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note25)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

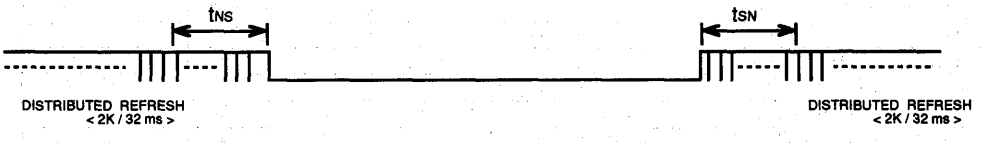
Self Refresh Cycle

Symbol	Parameter	Limits						Unit
		M5M417400B-5S		M5M417400B-6S		M5M417400B-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		15		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

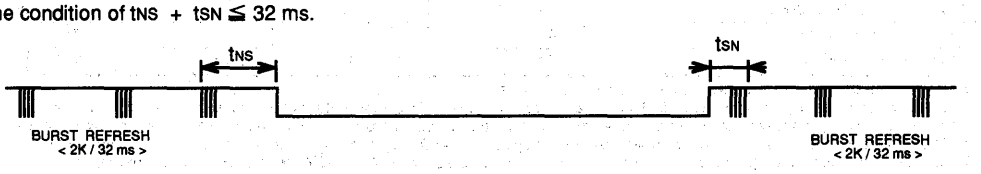
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 32$ ms and $t_{SN} \leqq 32$ ms.



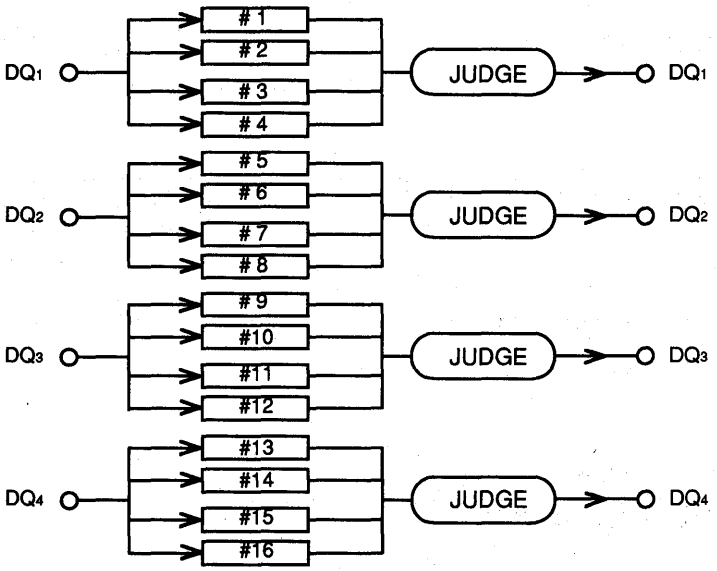
(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 32$ ms.

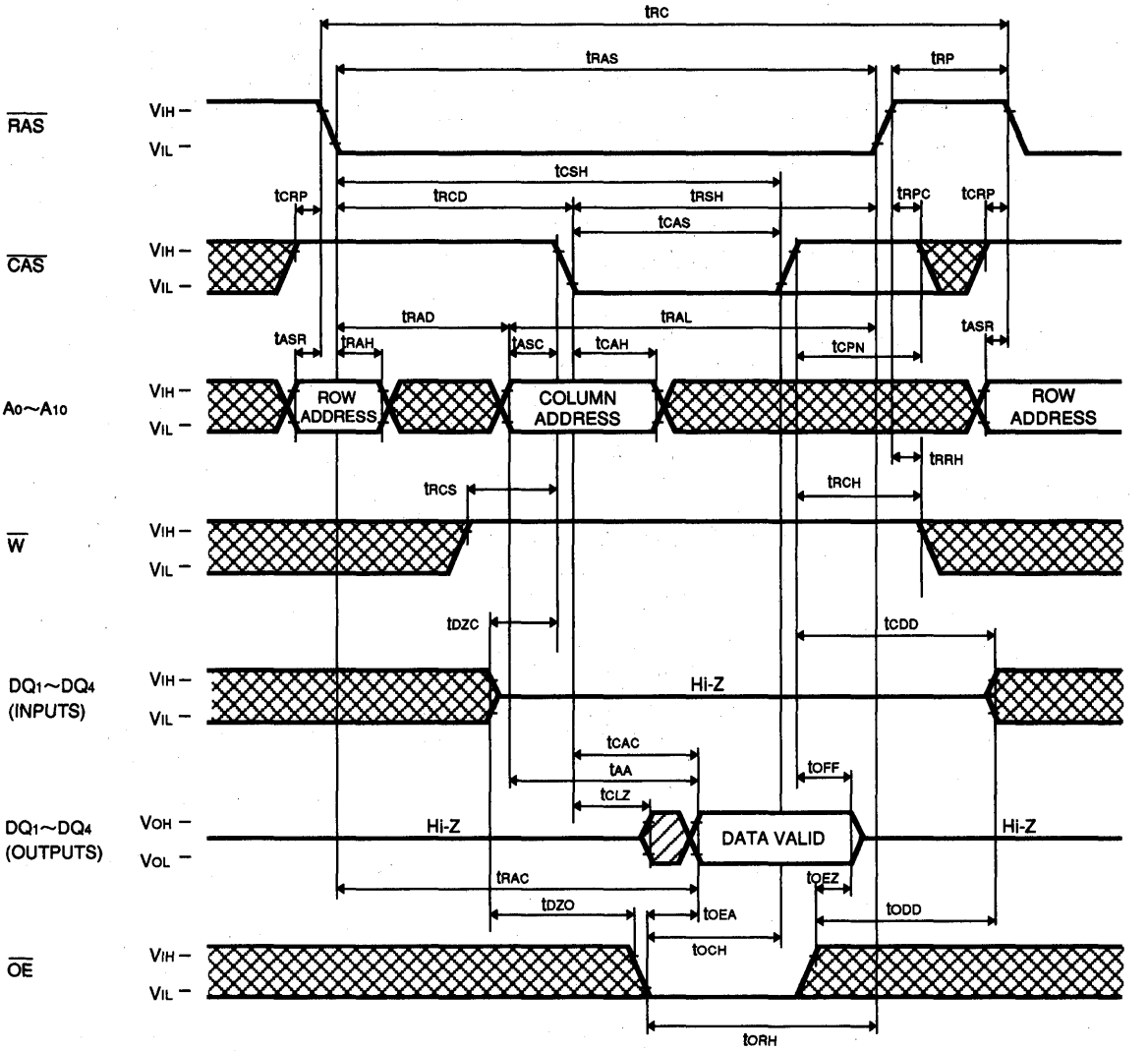


TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M417400B-5,-5S		M5M417400B-6,-6S		M5M417400B-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns



Timing Diagrams (Note 27)
Read Cycle

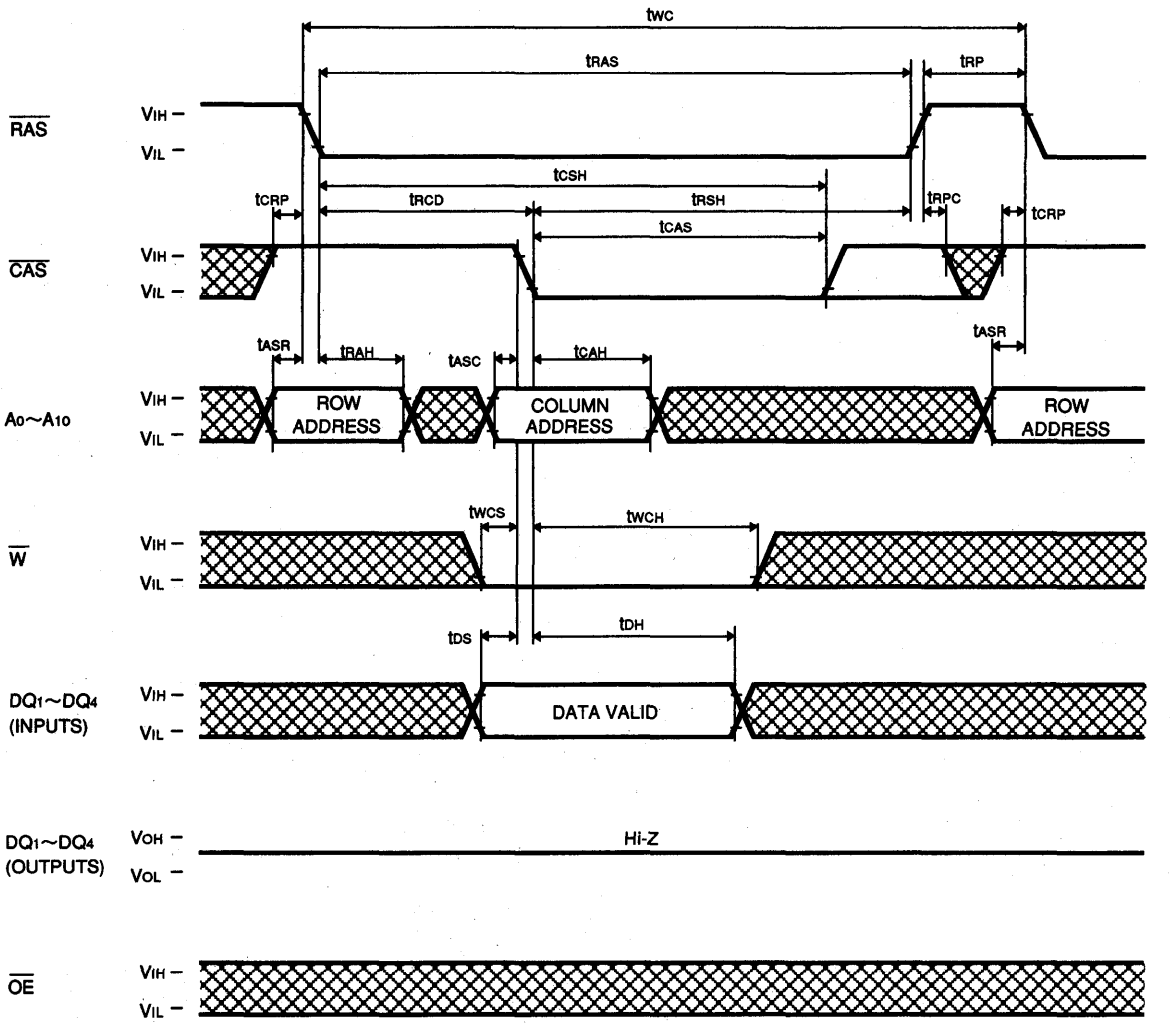


Note 27

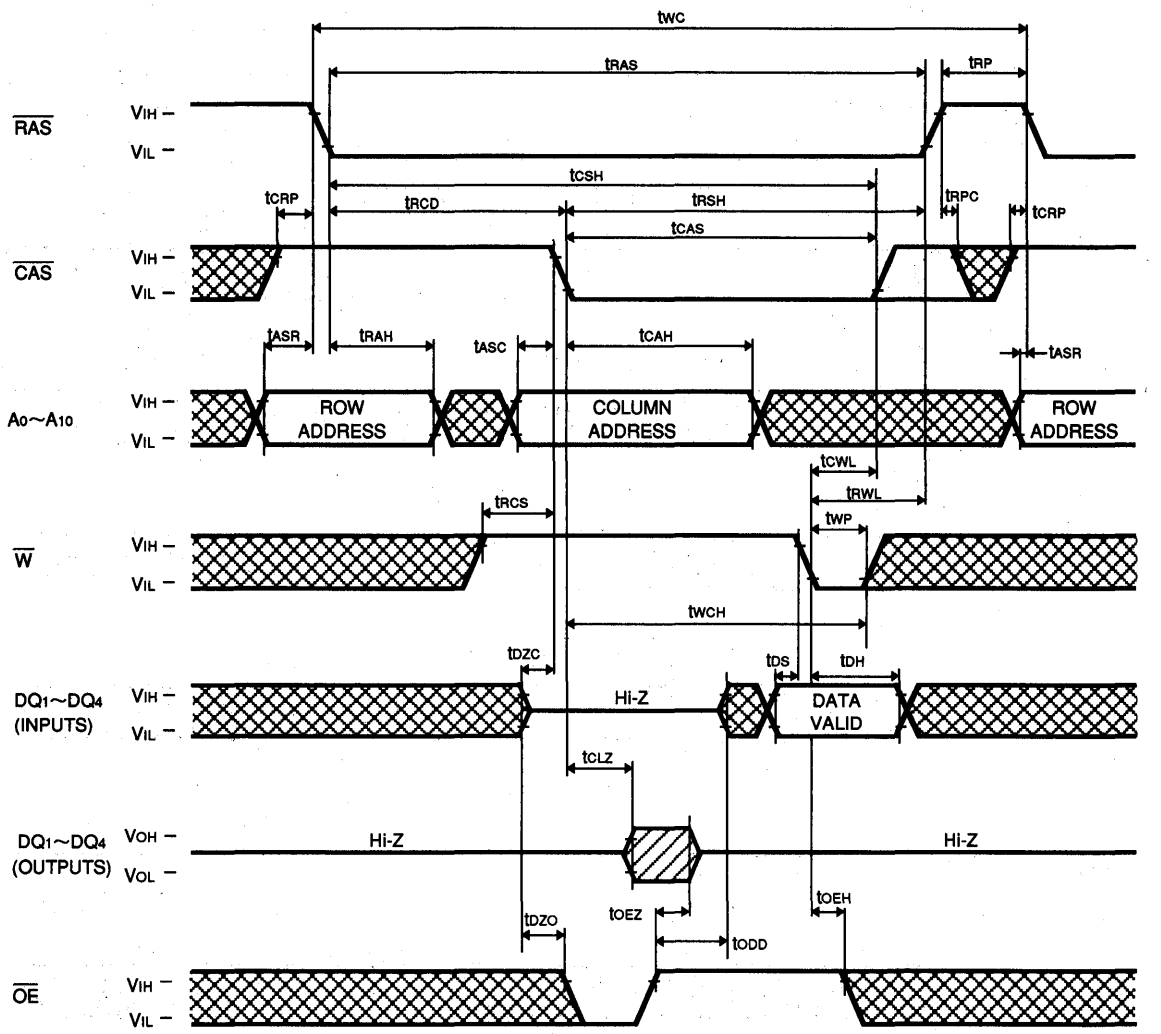
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

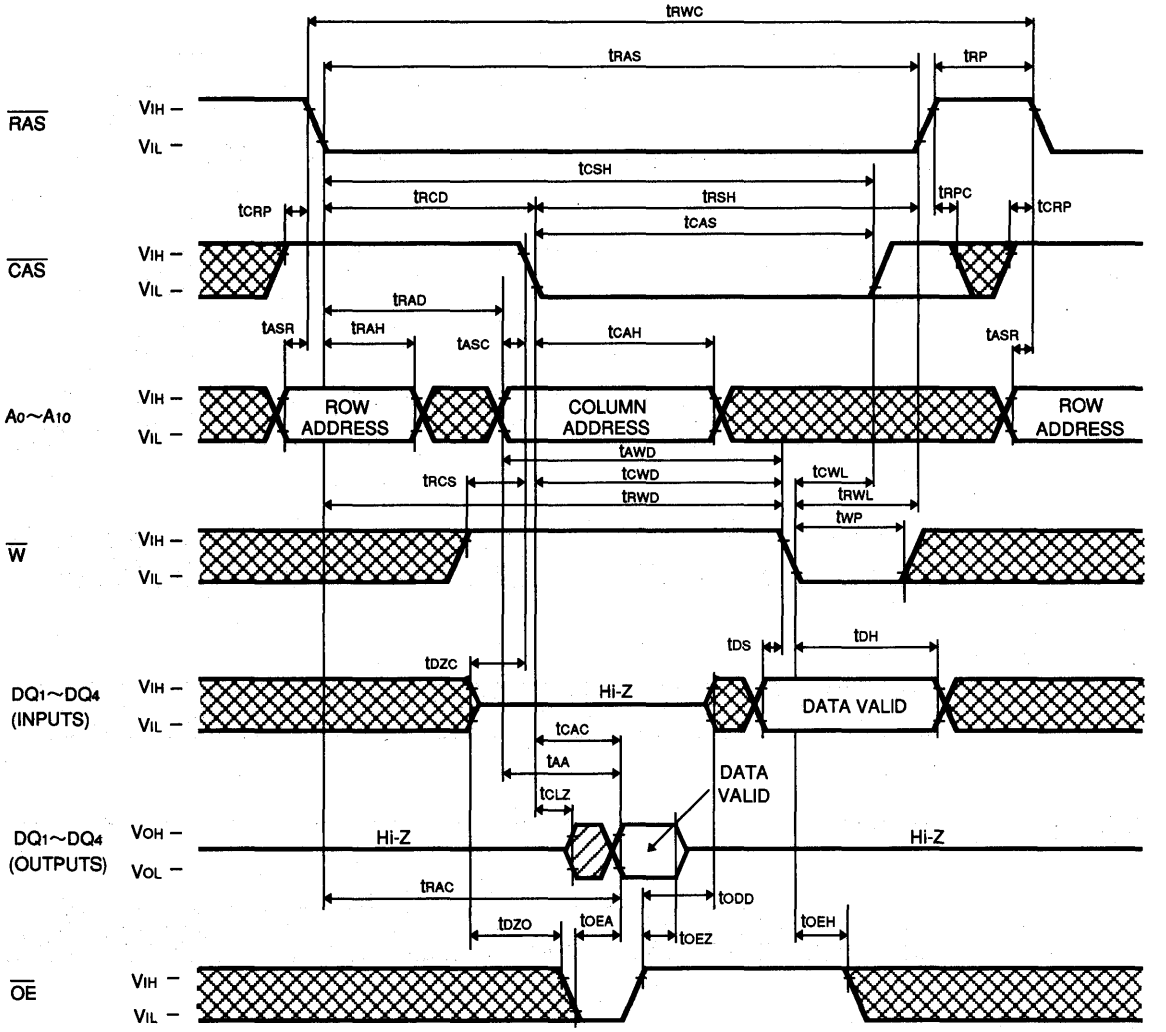
Write Cycle (Early write)



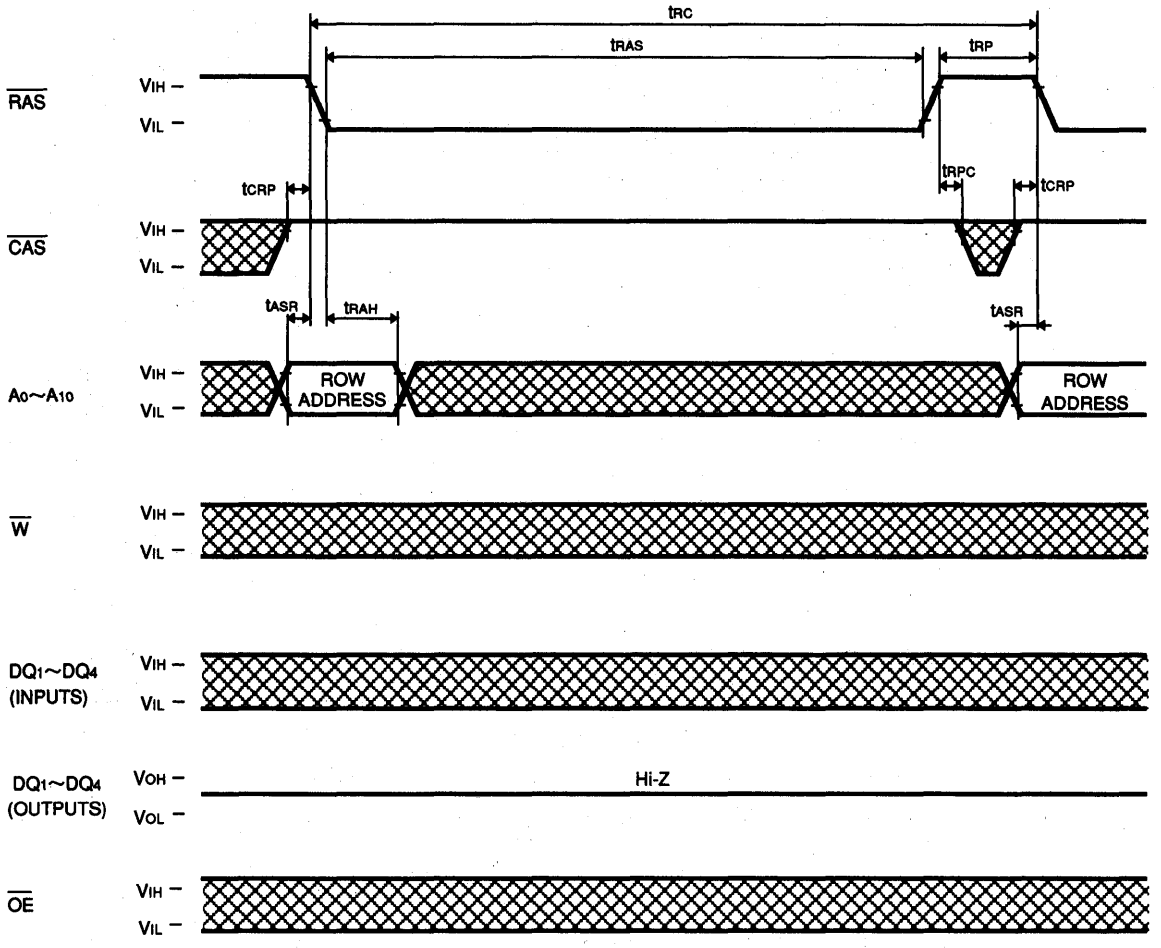
Write Cycle (Delayed write)



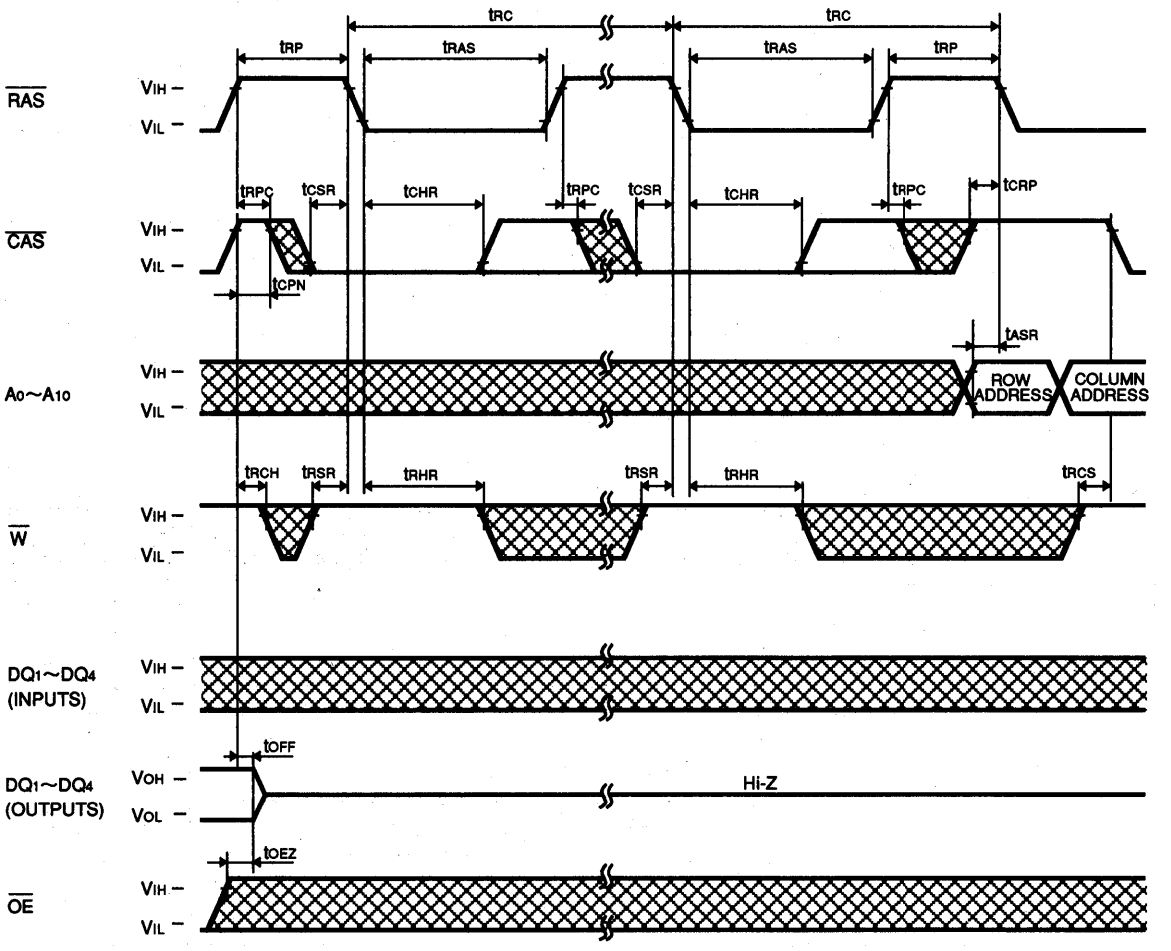
Read-Write, Read-Modify-Write Cycle



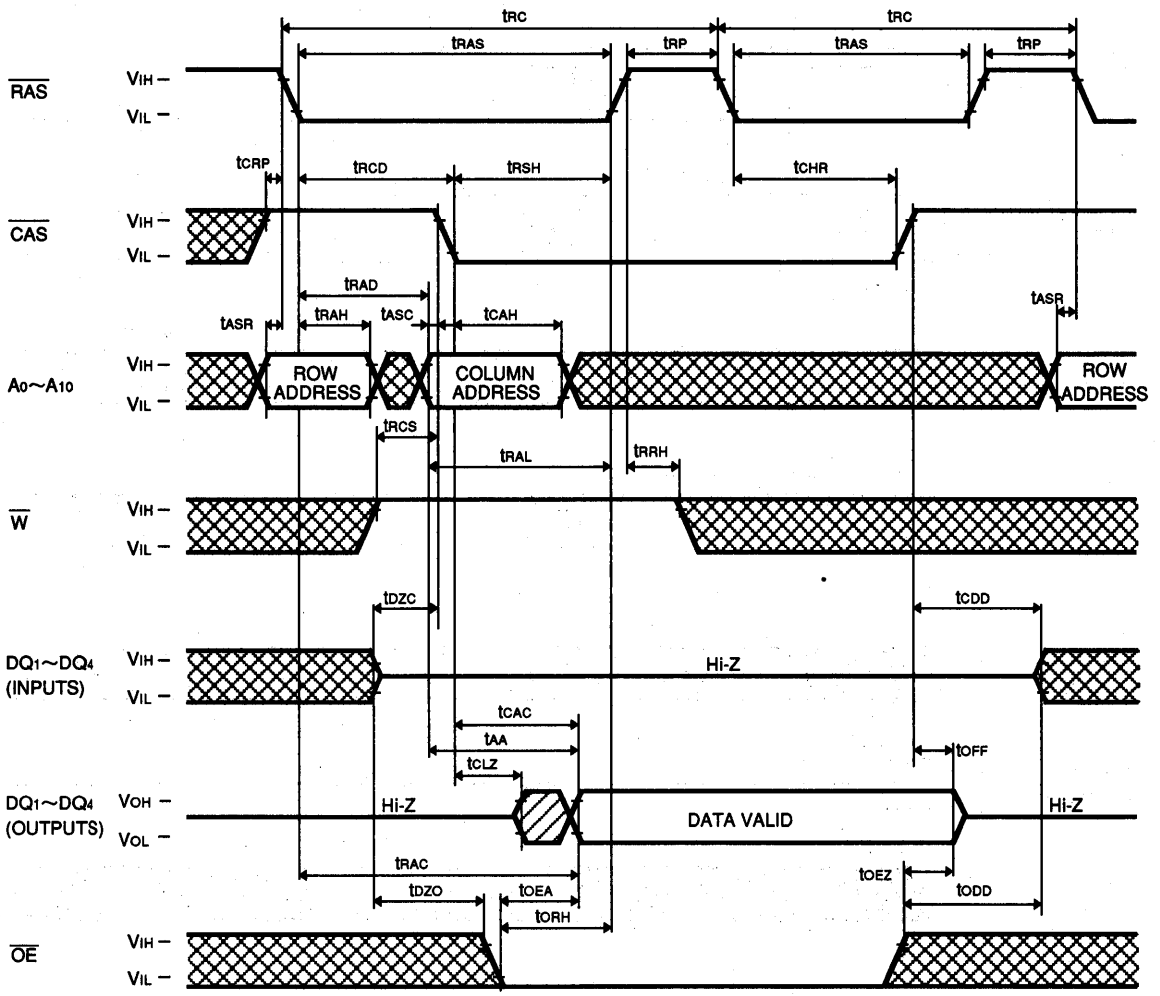
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

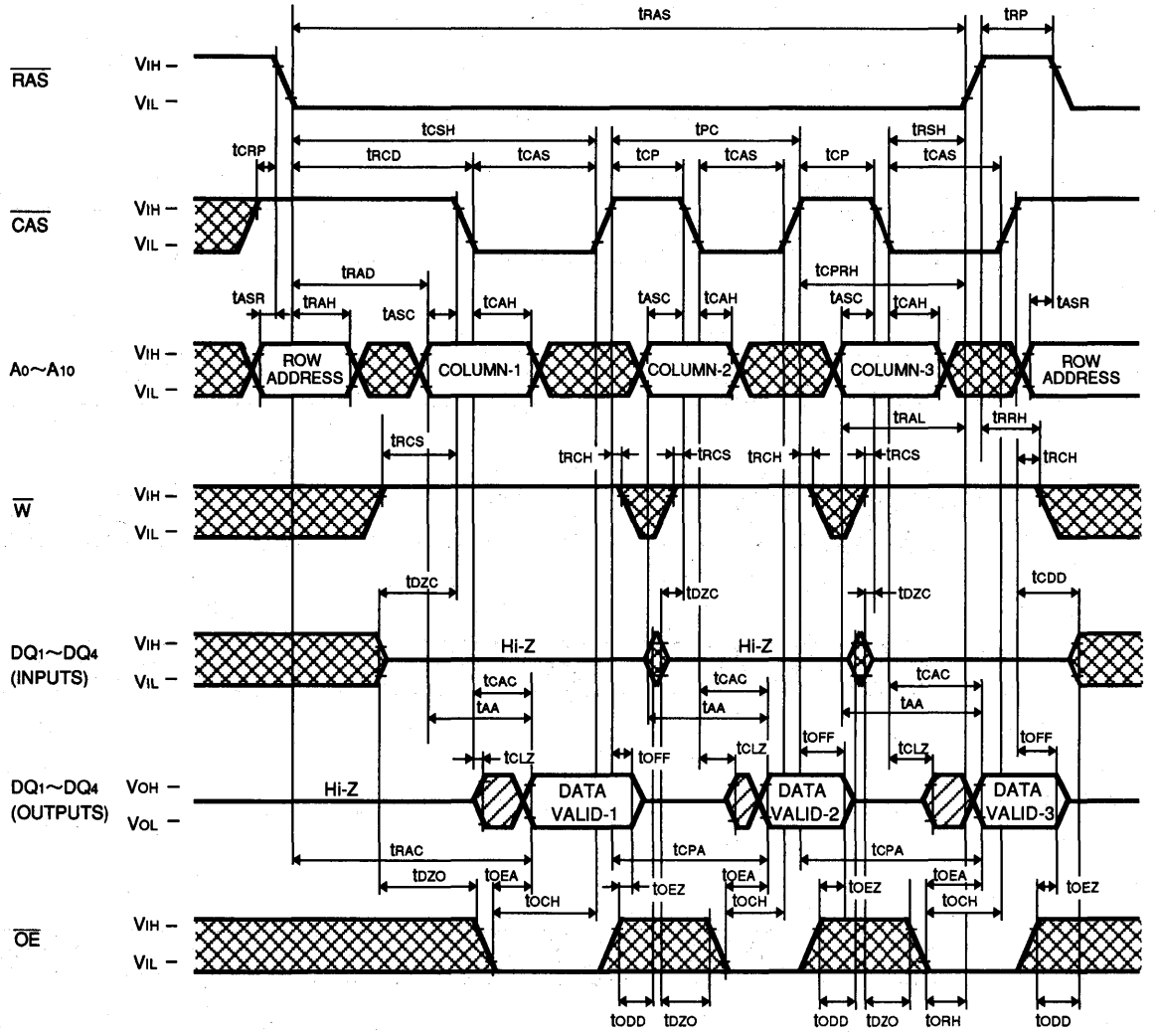


Hidden Refresh Cycle (Read) (Note 28)

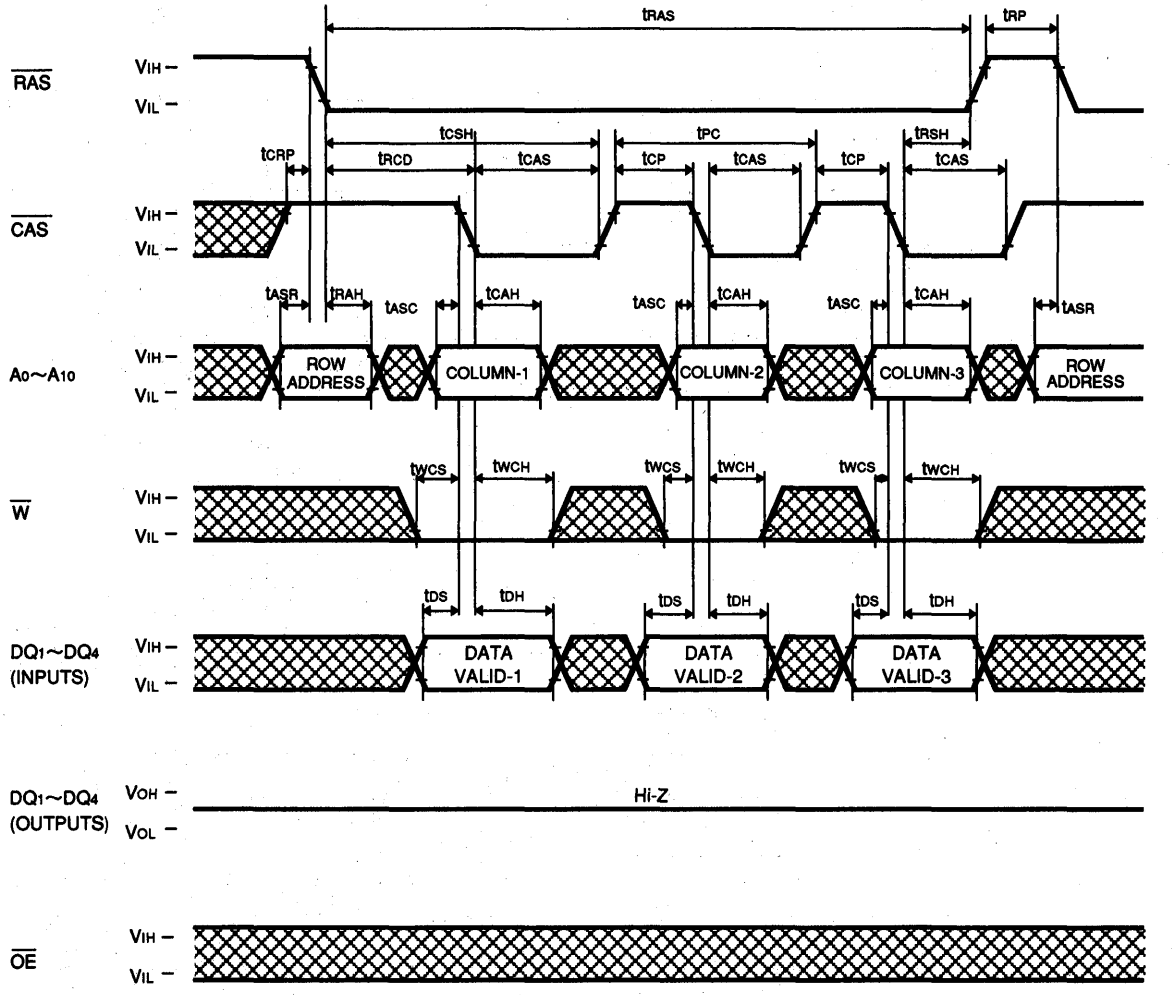


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

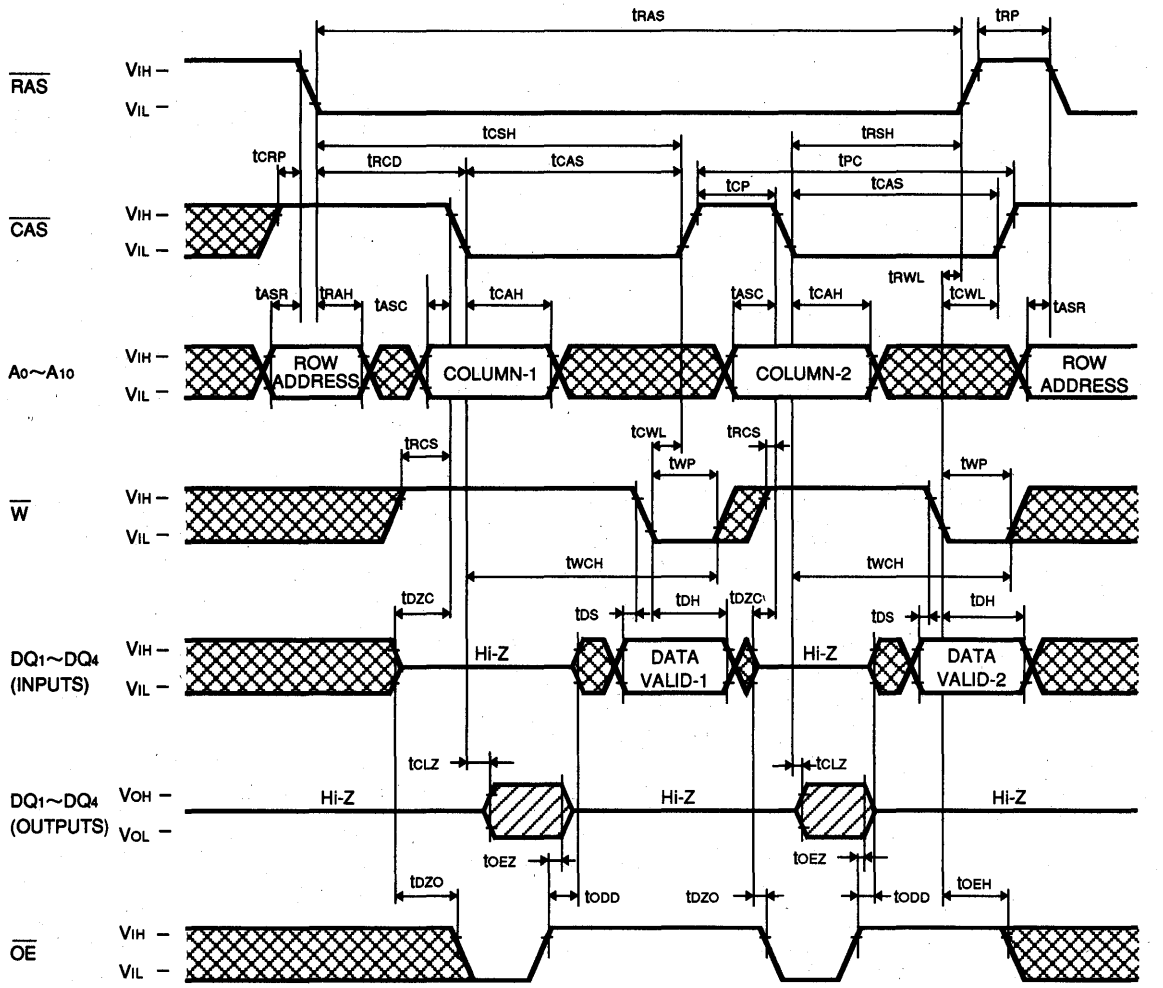
Fast Page Mode Read Cycle



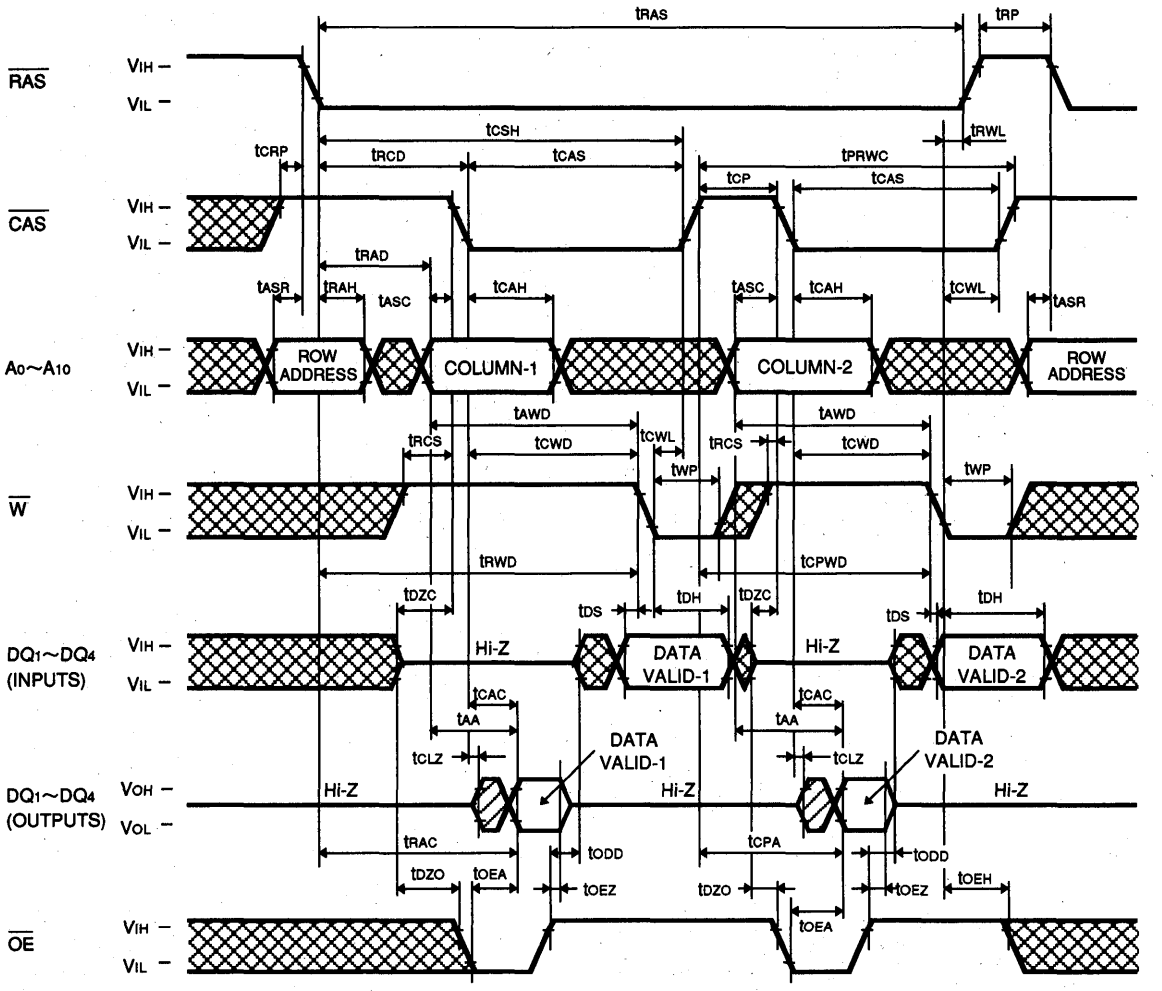
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)

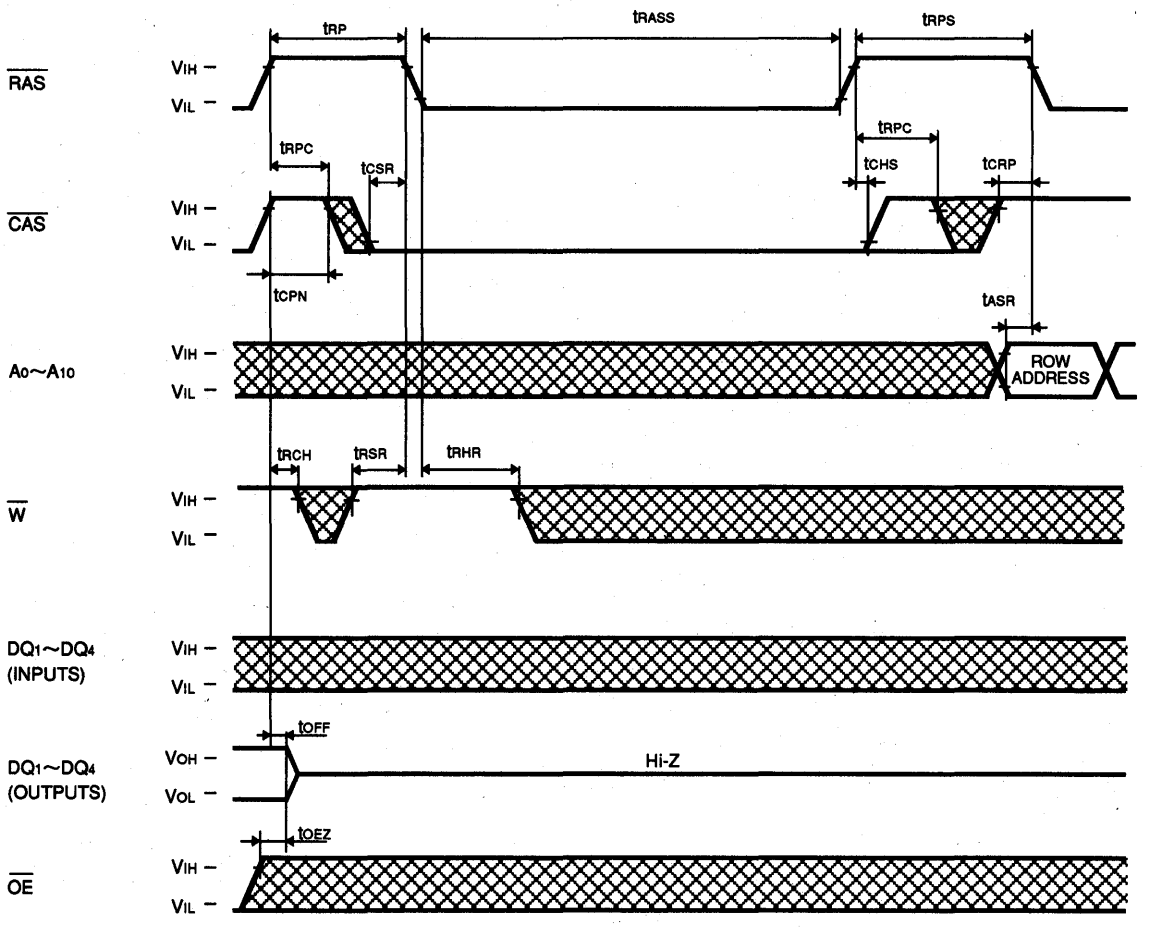


Fast Page Mode Read-Write,Read-Modify-Write Cycle

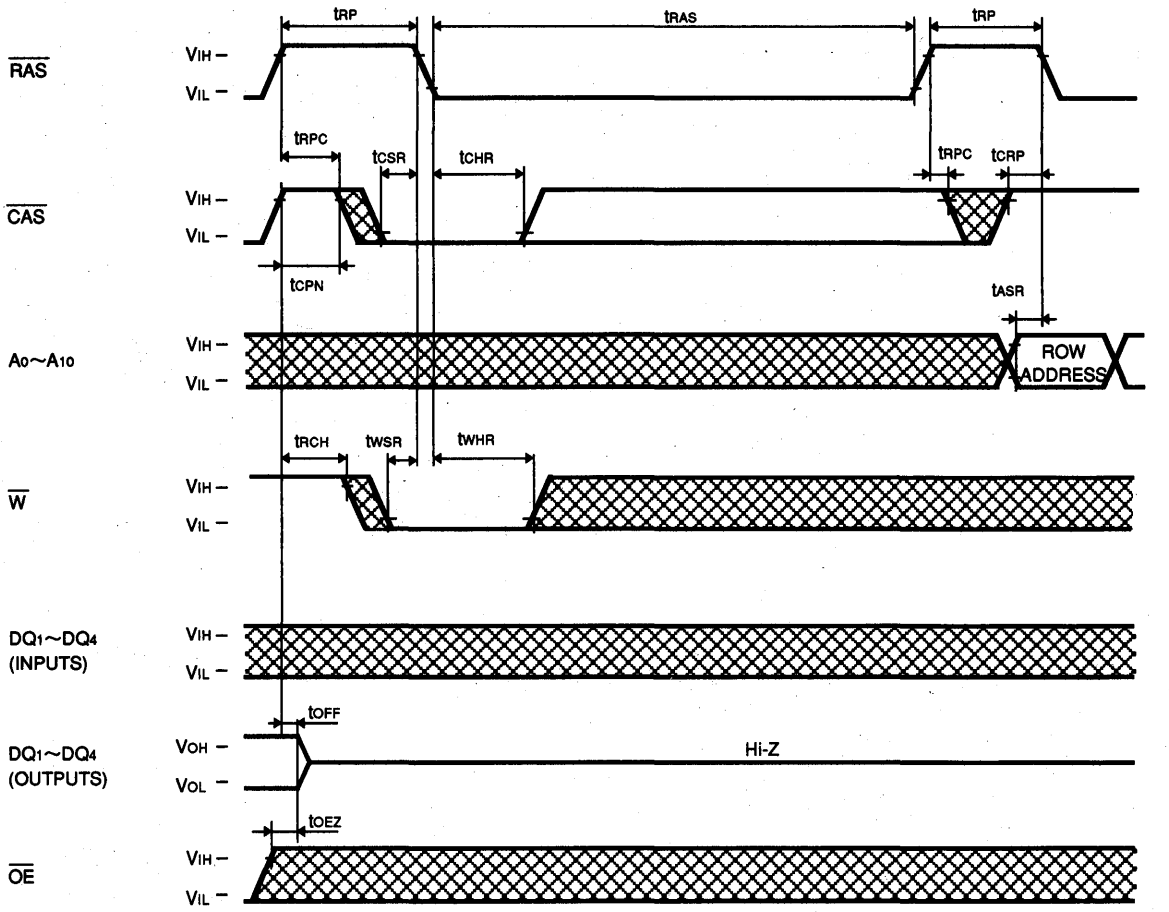


MITSUBISHI ELECTRIC

Self Refresh Cycle



TEST Mode SET Cycle (Note 29)



Note 29: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.

M5M417400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417400CXX-5,-5S	50	13	25	13	90	655
M5M417400CXX-6,-6S	60	15	30	15	110	540
M5M417400CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

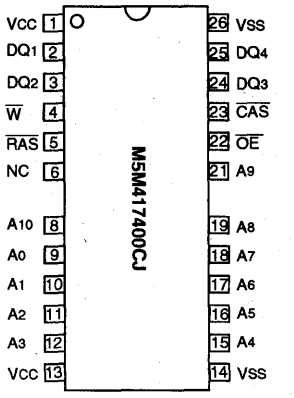
- Standard 26pin SOJ, 26pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 2.2mW (Max)* ---------- CMOS Input level
- Low operating power dissipation
  - M5M417400Cxx-5,-5S ---------- 800.0mW (Max)
  - M5M417400Cxx-6,-6S ---------- 660.0mW (Max)
  - M5M417400Cxx-7,-7S ---------- 580.0mW (Max)
- Self refresh capability *
  - self refresh current ---------- 200.0 μA(Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

*Applicable to self refresh version(M5M417400CJ,TP-5S,-6S,-7S :option) only

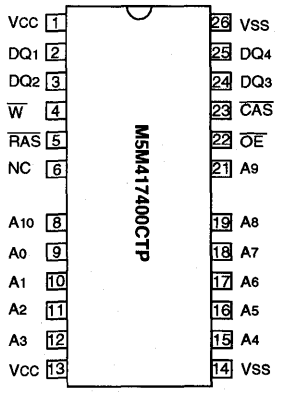
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

M5M417400CJ,TP-5,-5S:Under development

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

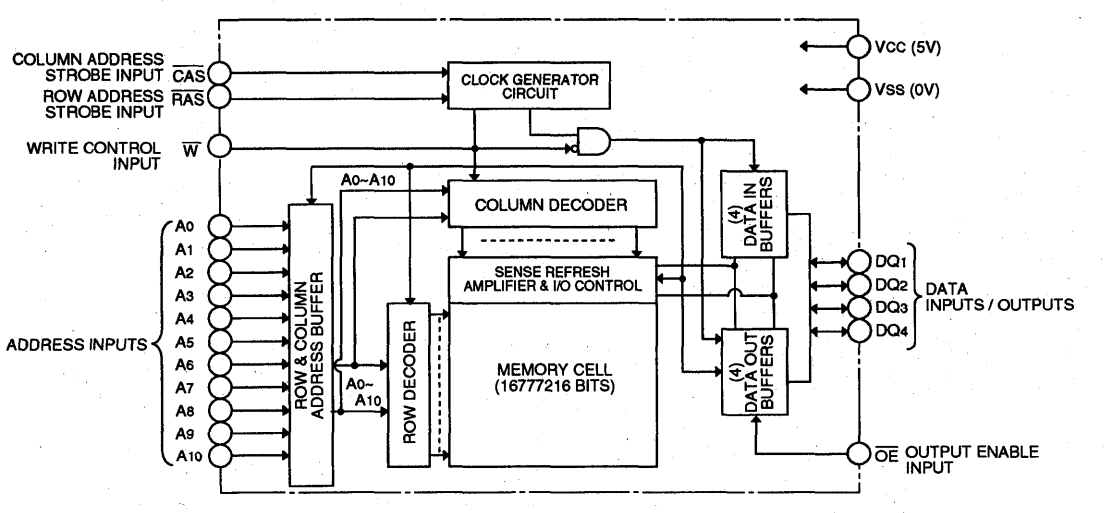
The M5M417400CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
**: V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V ±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	-10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 5.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M417400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417400C-6,-6S				120	
		M5M417400C-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧ Vcc -0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M417400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417400C-6,-6S				120	
		M5M417400C-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M417400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M417400C-6,-6S				70	
		M5M417400C-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417400C-6,-6S				120	
		M5M417400C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max).

8: Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9: Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).

10: Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).

11: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦ |±10 μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed tT=5ns.

13: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

14: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).

15: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

16: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

17: Either tDZC or tDZO must be satisfied.

18: Either tCDD or tODD must be satisfied.

19: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V ±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	**M5M417400C (S)**	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$ ≦0.2V $\overline{OE}$ & $\overline{WE}$ ≦0.2V or $\overline{OE}$ & $\overline{WE}$ ≧Vcc-0.2V A_0 ~ A_{10} ≦0.2V or A_0 ~ A_{10} ≧Vcc-0.2V t_{REF}=128ms (2048cycles) output = OPEN t_{RAS}=t_{RAS}min. ~1 μs			500	μA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	**M5M417400C (S)**	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

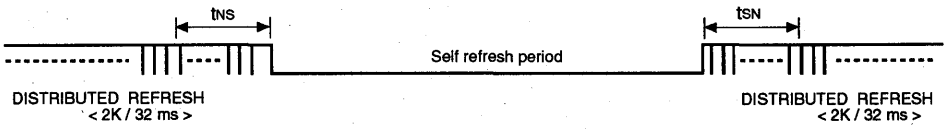
TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=5V ± 10%, V_{SS}=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M417400C-5S		M5M417400C-6S		M5M417400C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

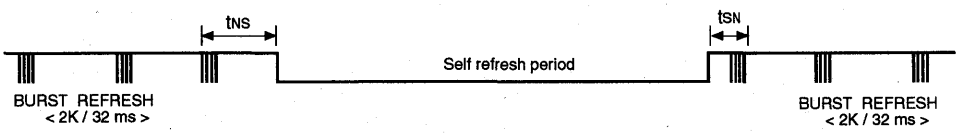
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦32ms and t_{SN}≦32ms.



(2) In case of burst refresh

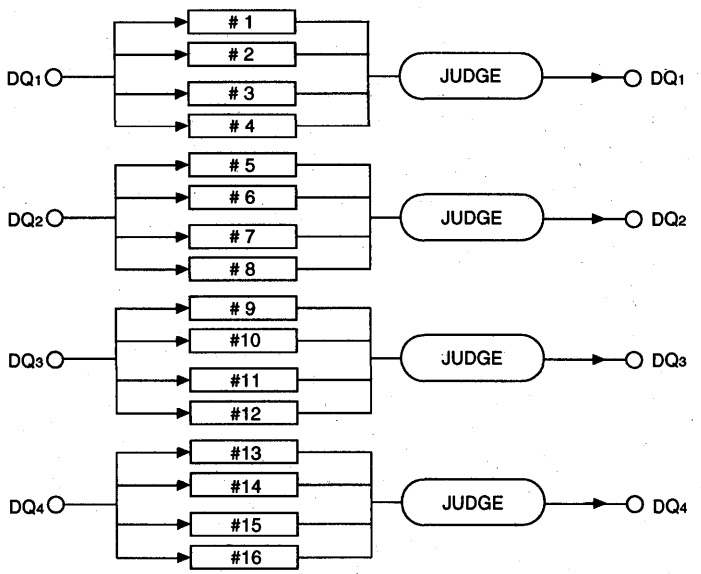
The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}+t_{SN}≦32ms.



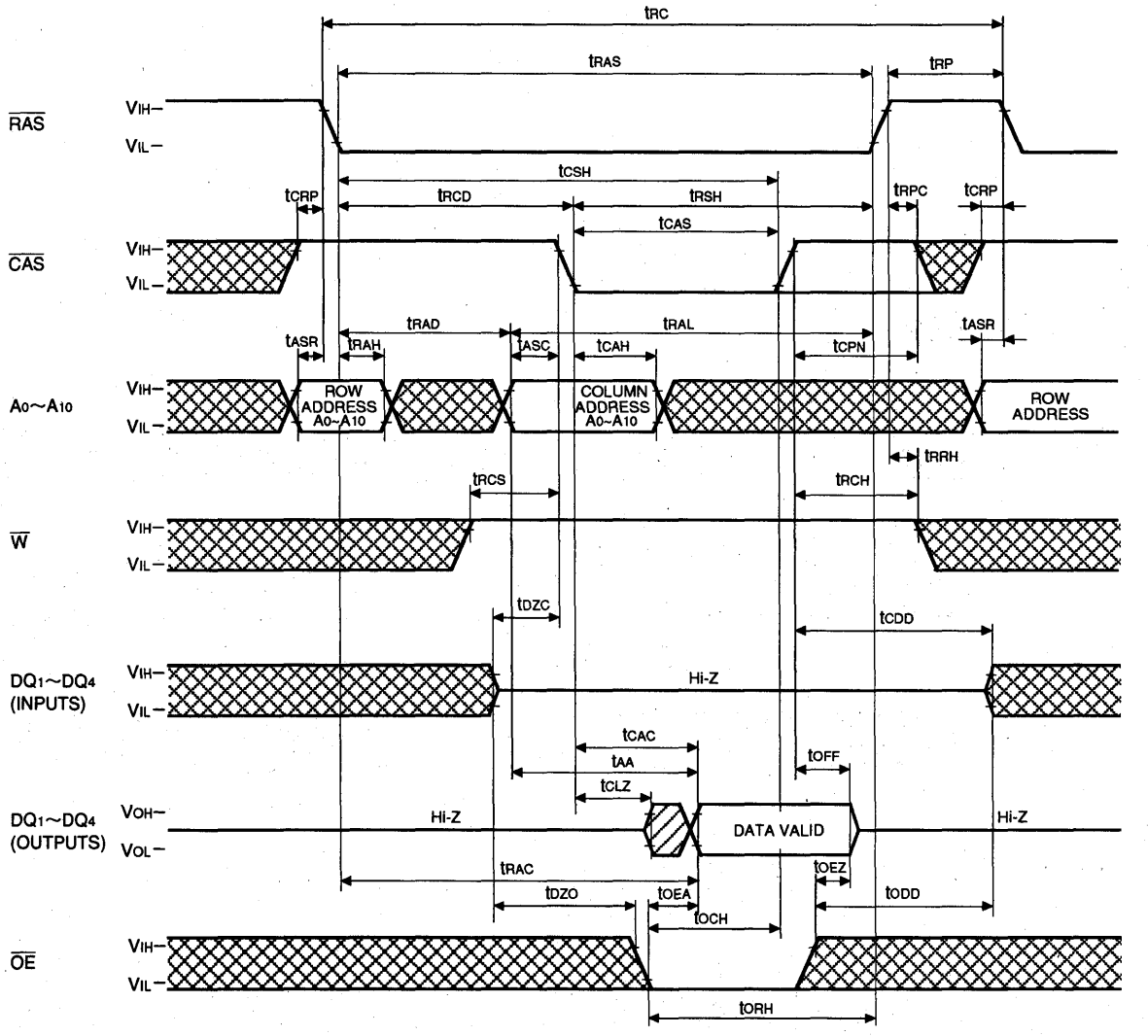
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M417400C-5,-5S		M5M417400C-6,-6S		M5M417400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0 and CA_1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 28)
Read Cycle

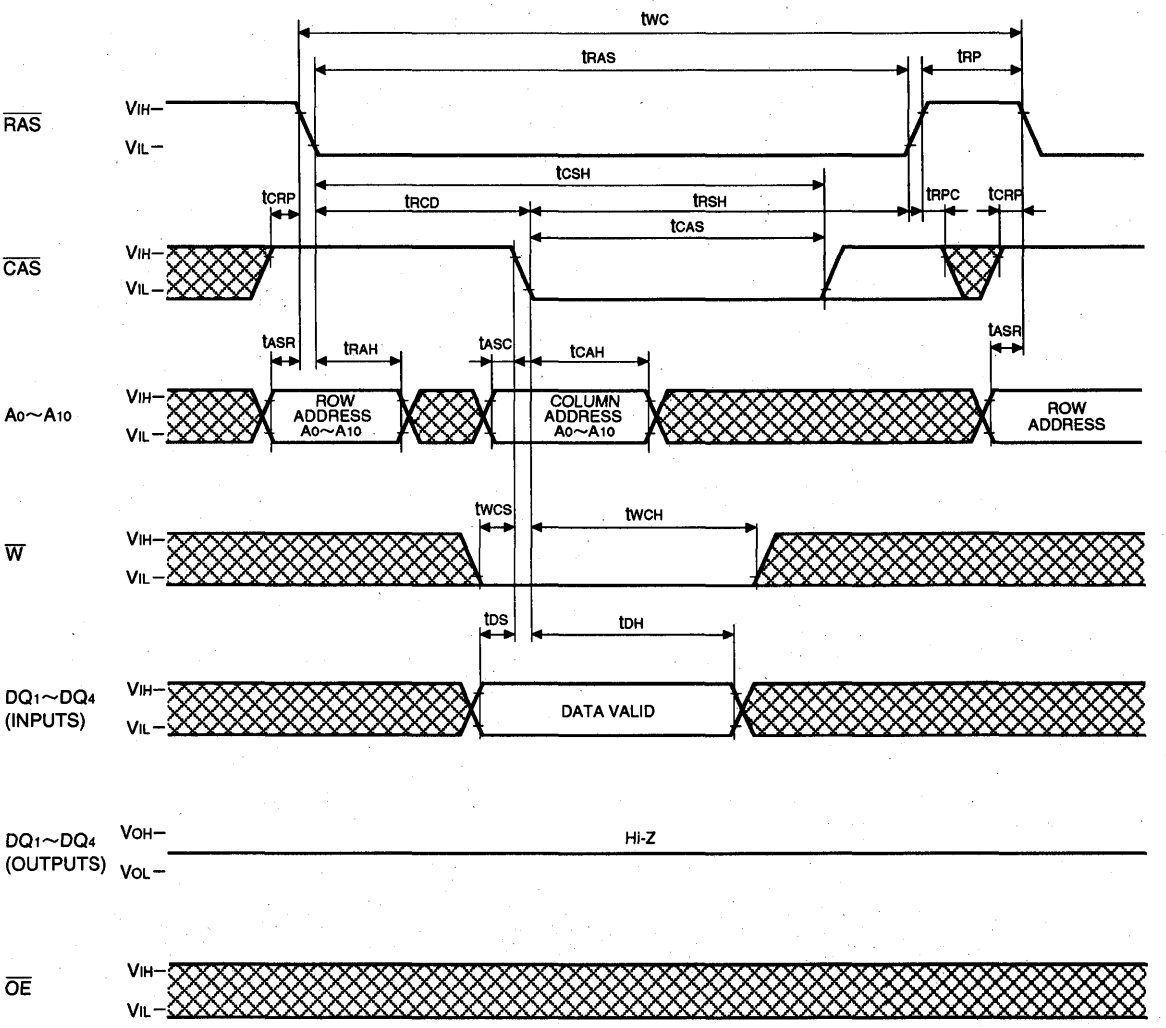


Note 28

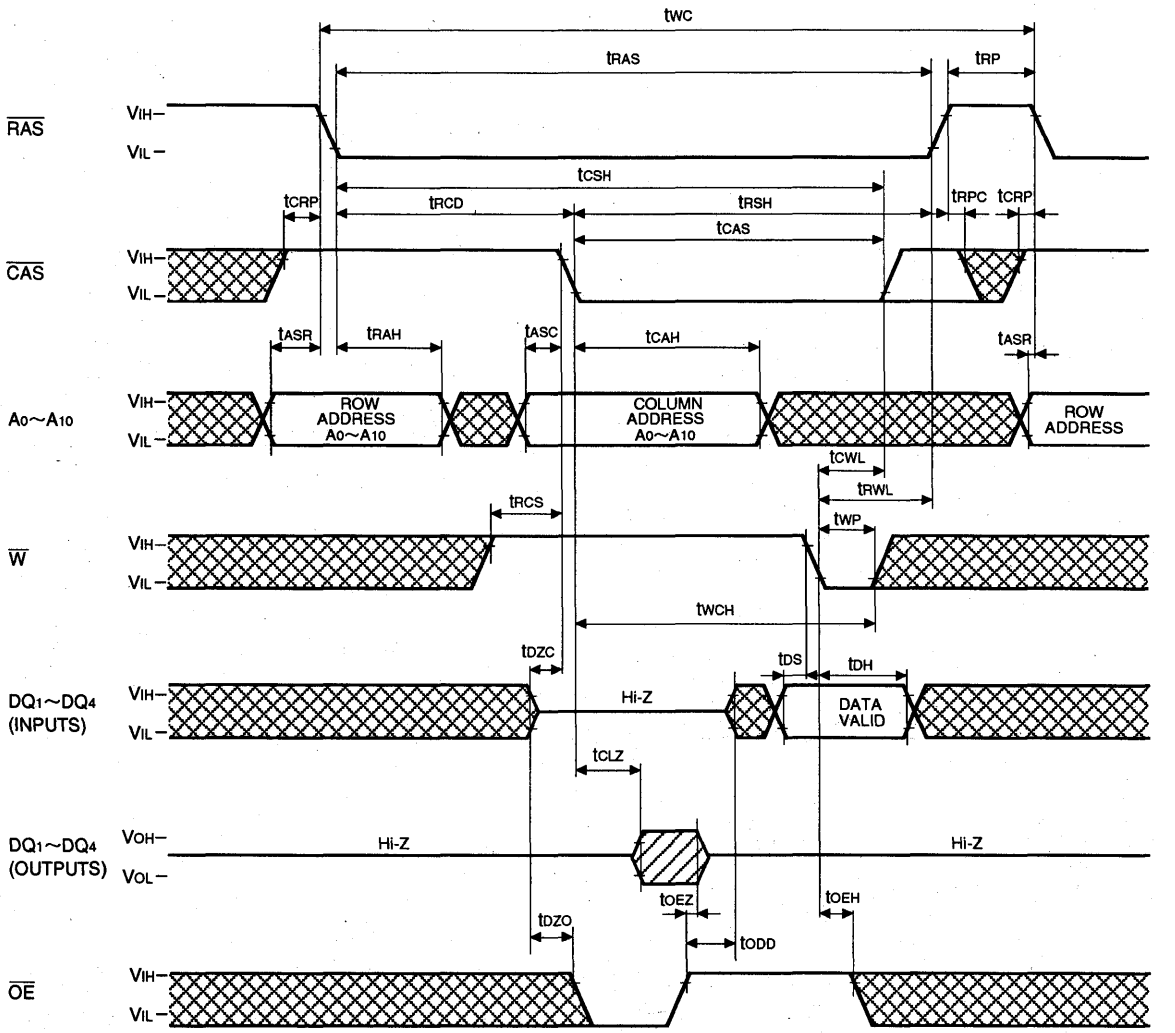
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

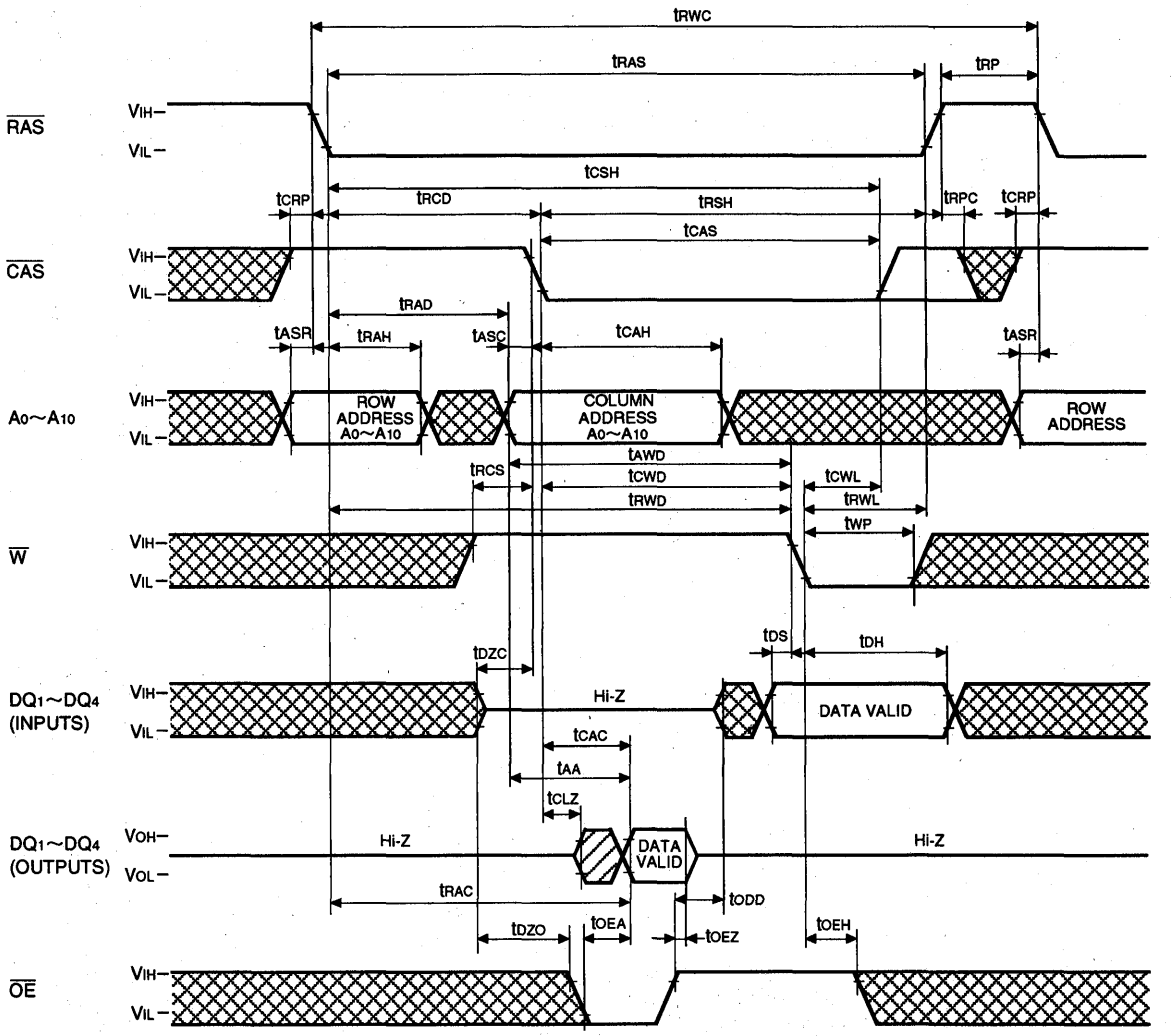
Write Cycle (Early write)



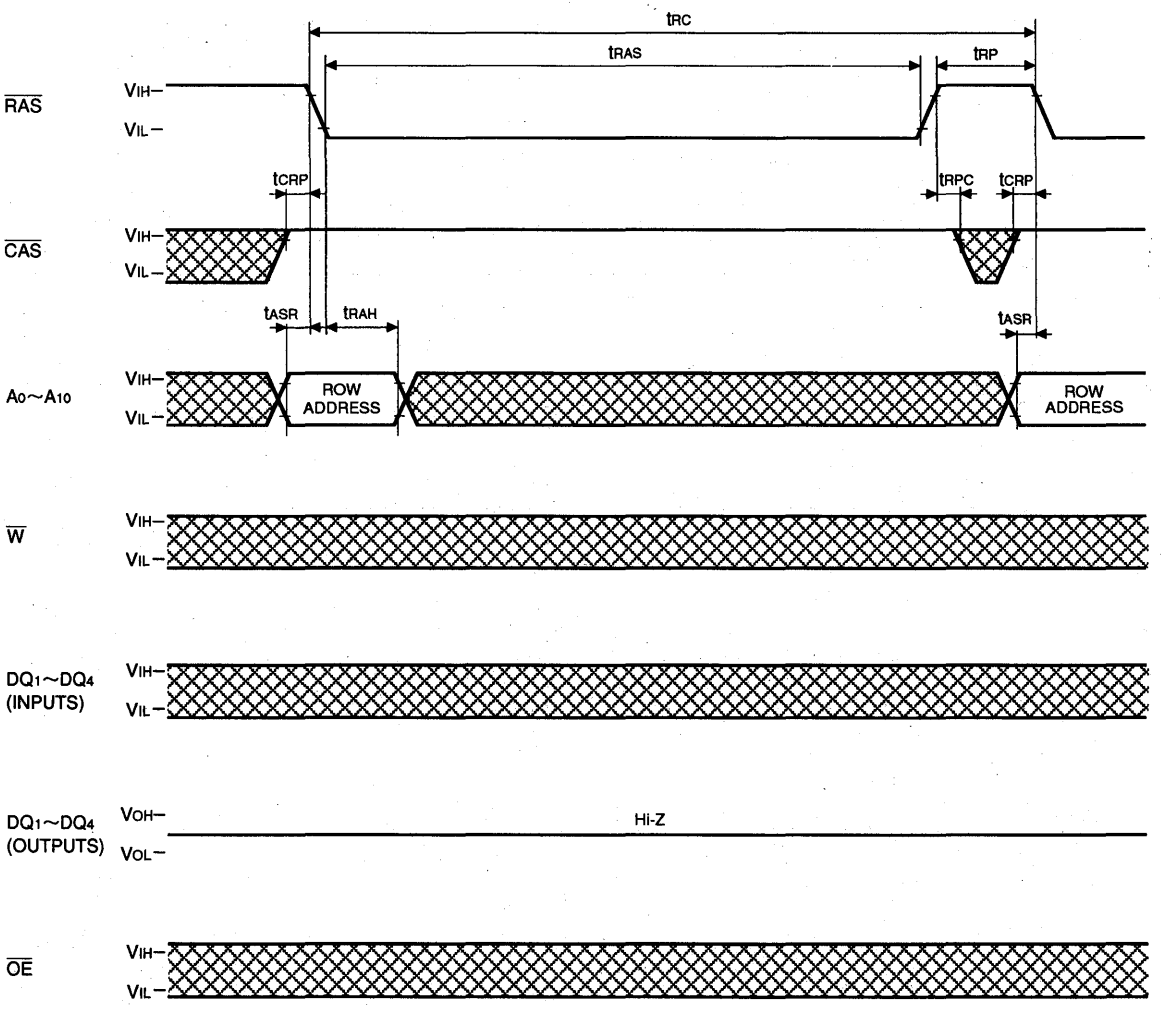
Write Cycle (Delayed write)



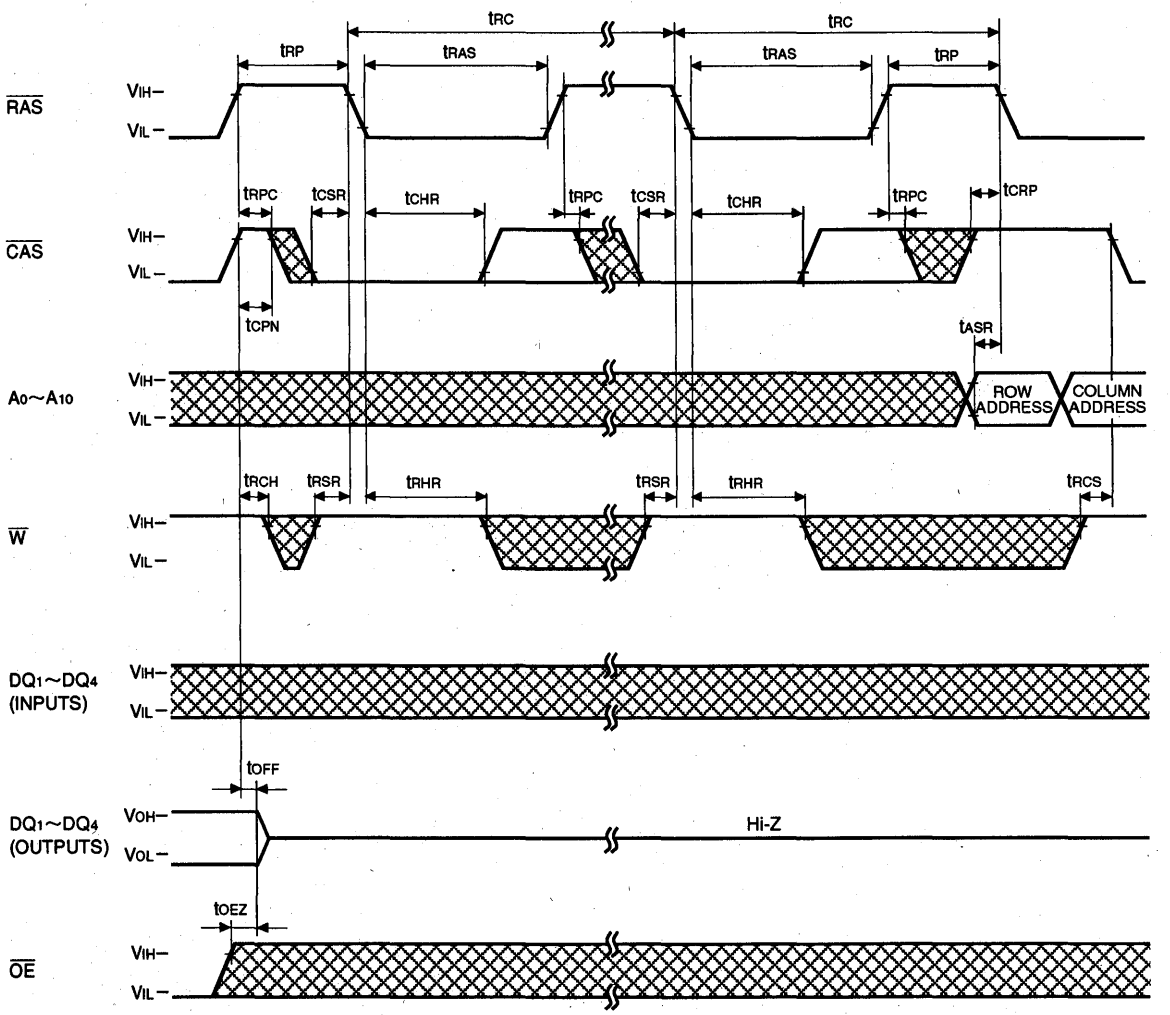
Read-Write, Read-Modify-Write Cycle



$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



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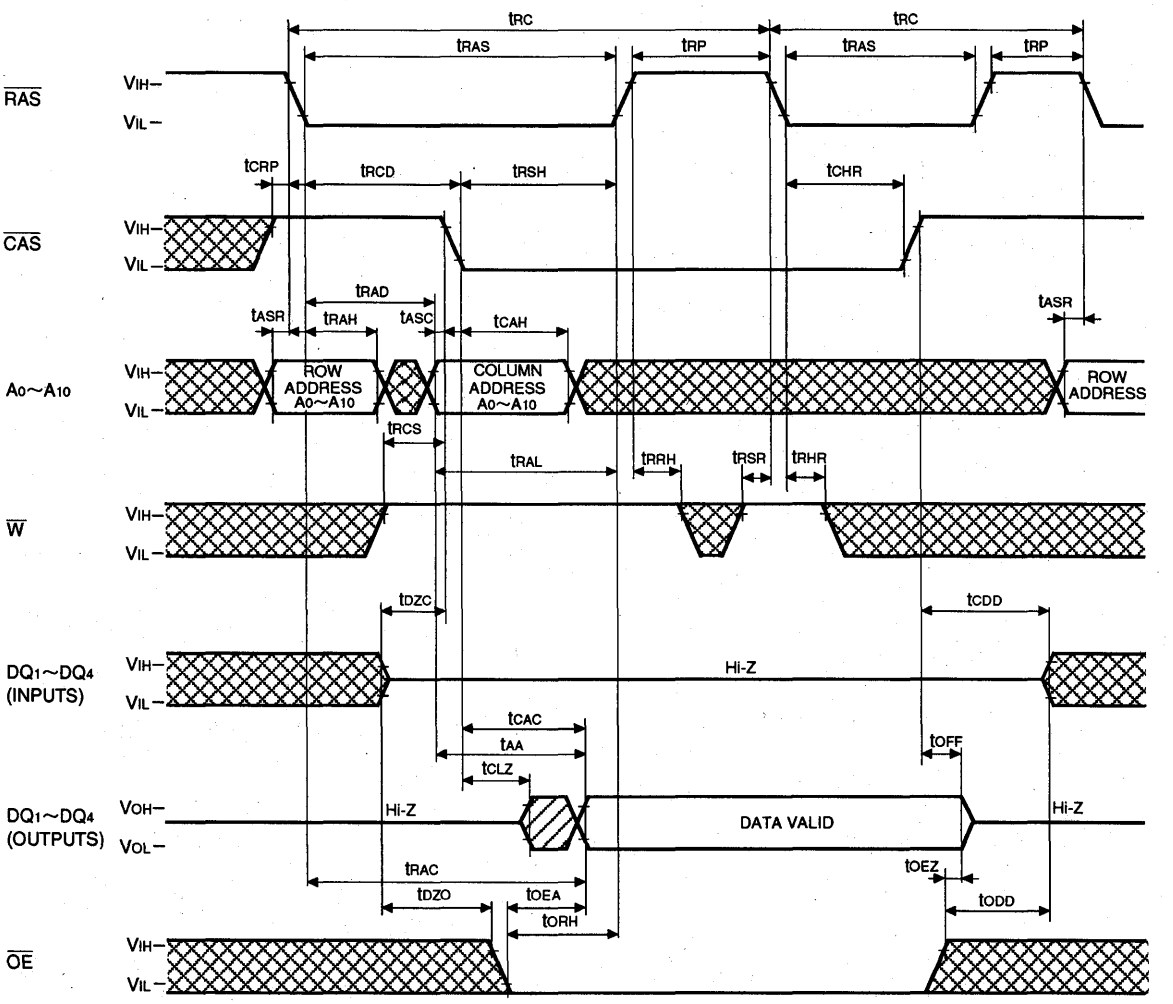
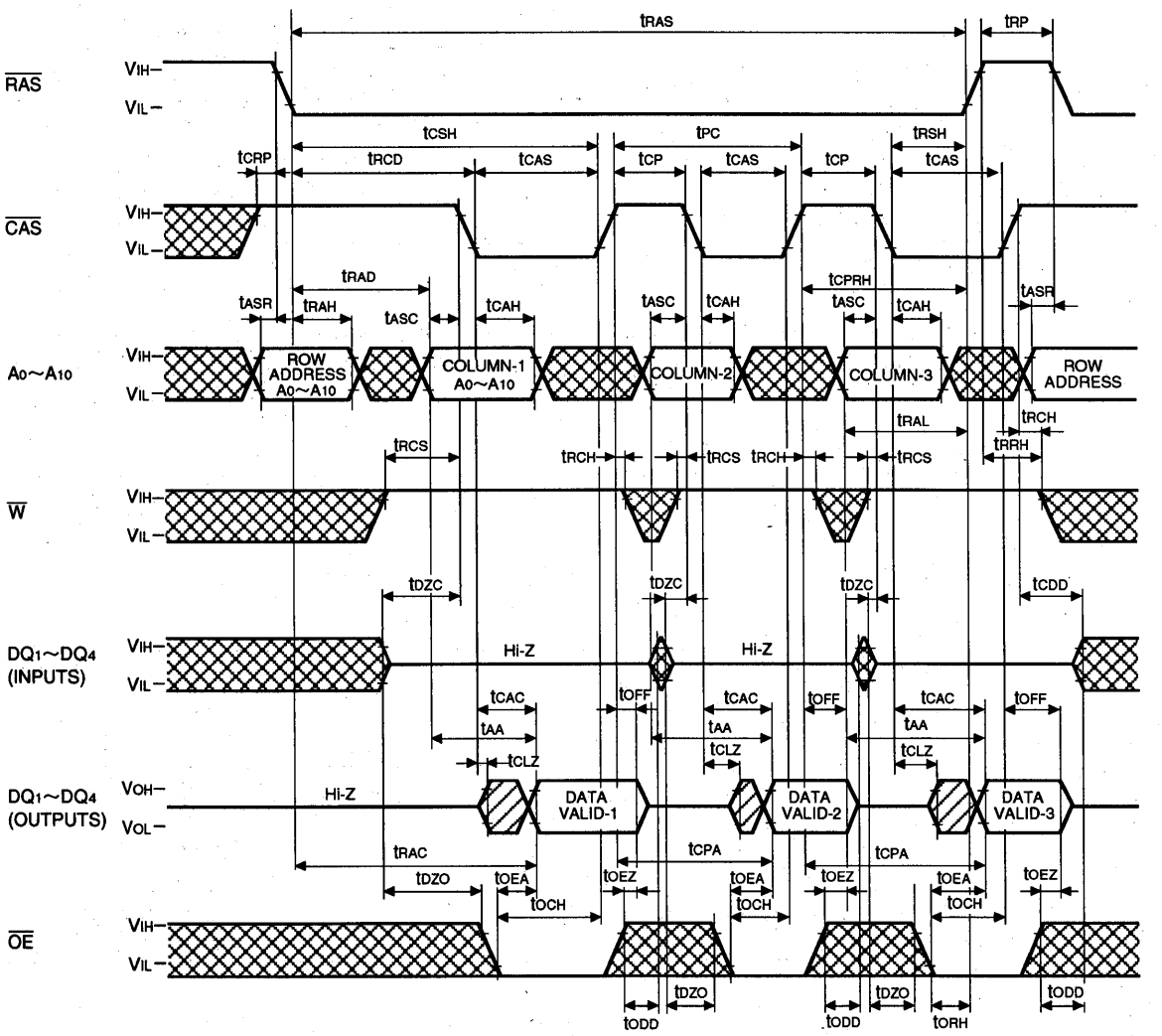
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR & tRHR should be satisfied not to enter TEST MODE .

Fast Page Mode Read Cycle



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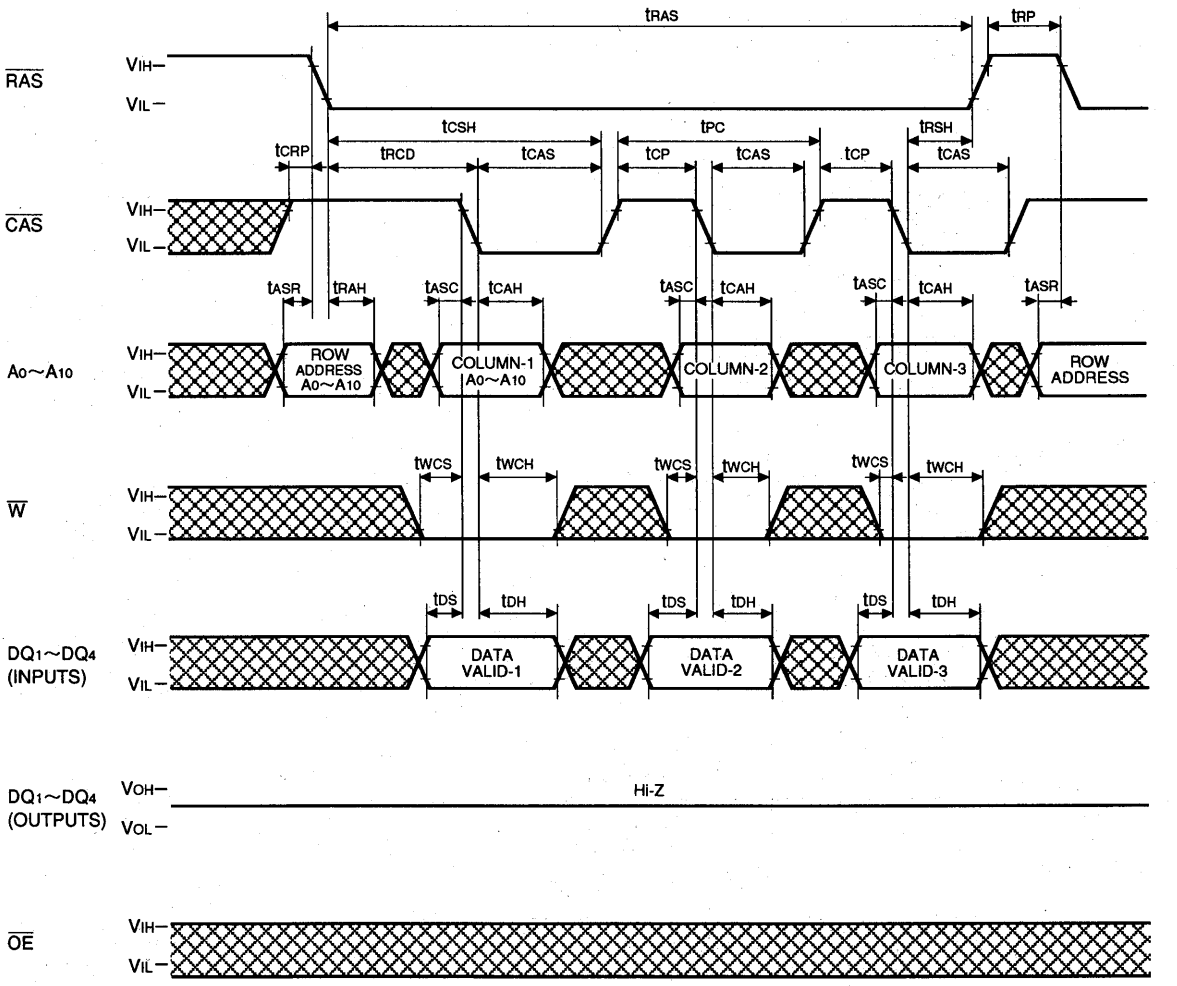
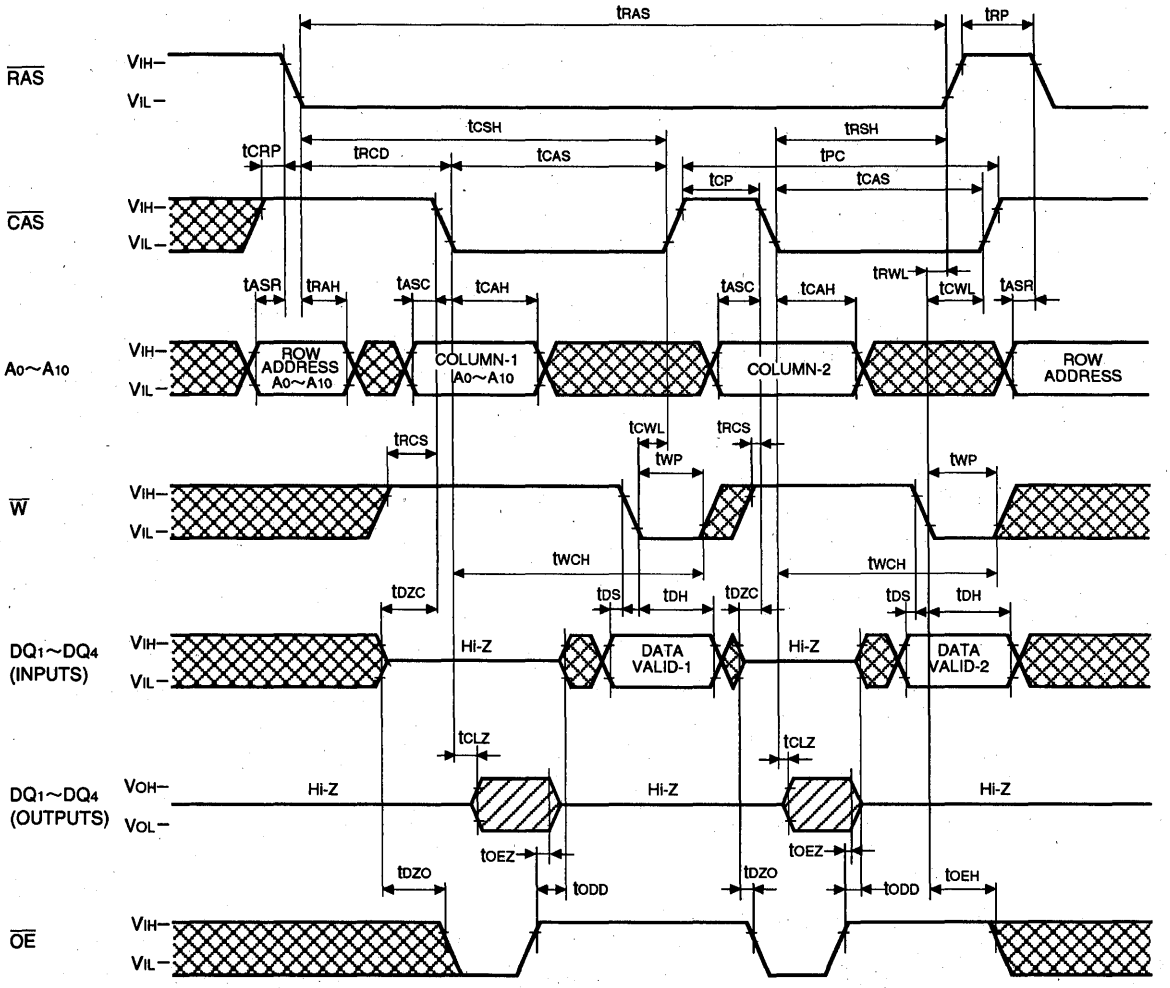
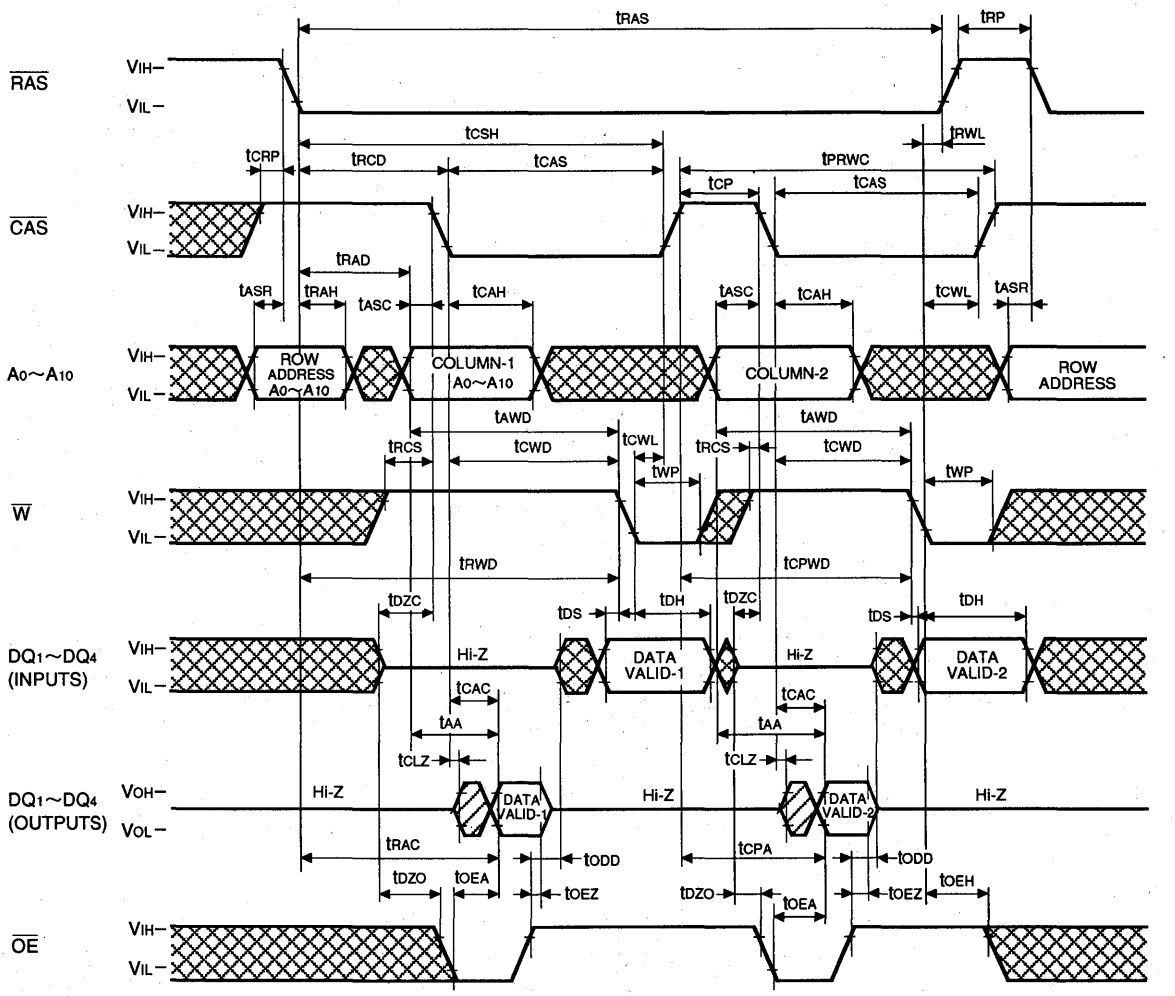
Fast Page Mode Write Cycle (Early Write)



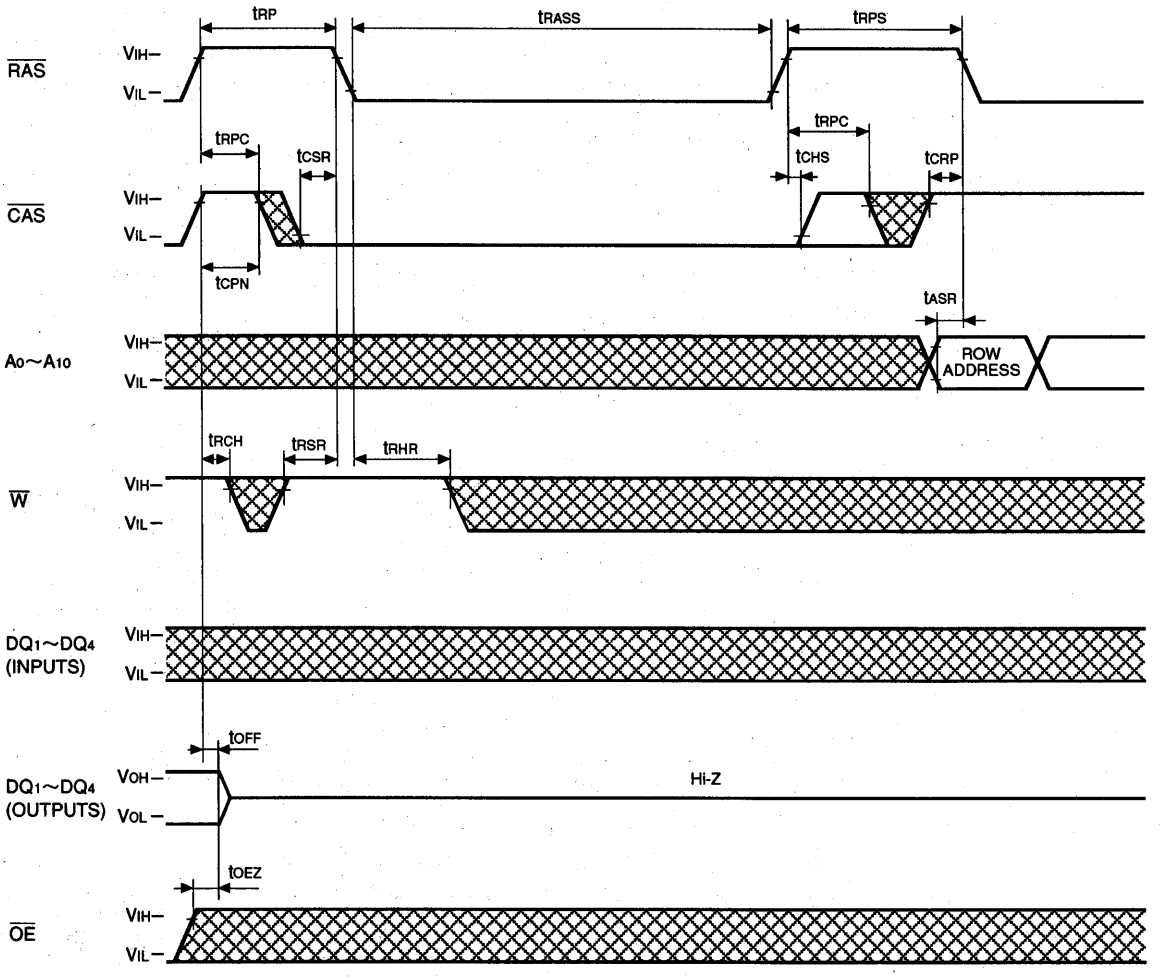
Fast-Page Mode Write Cycle (Delayed Write)



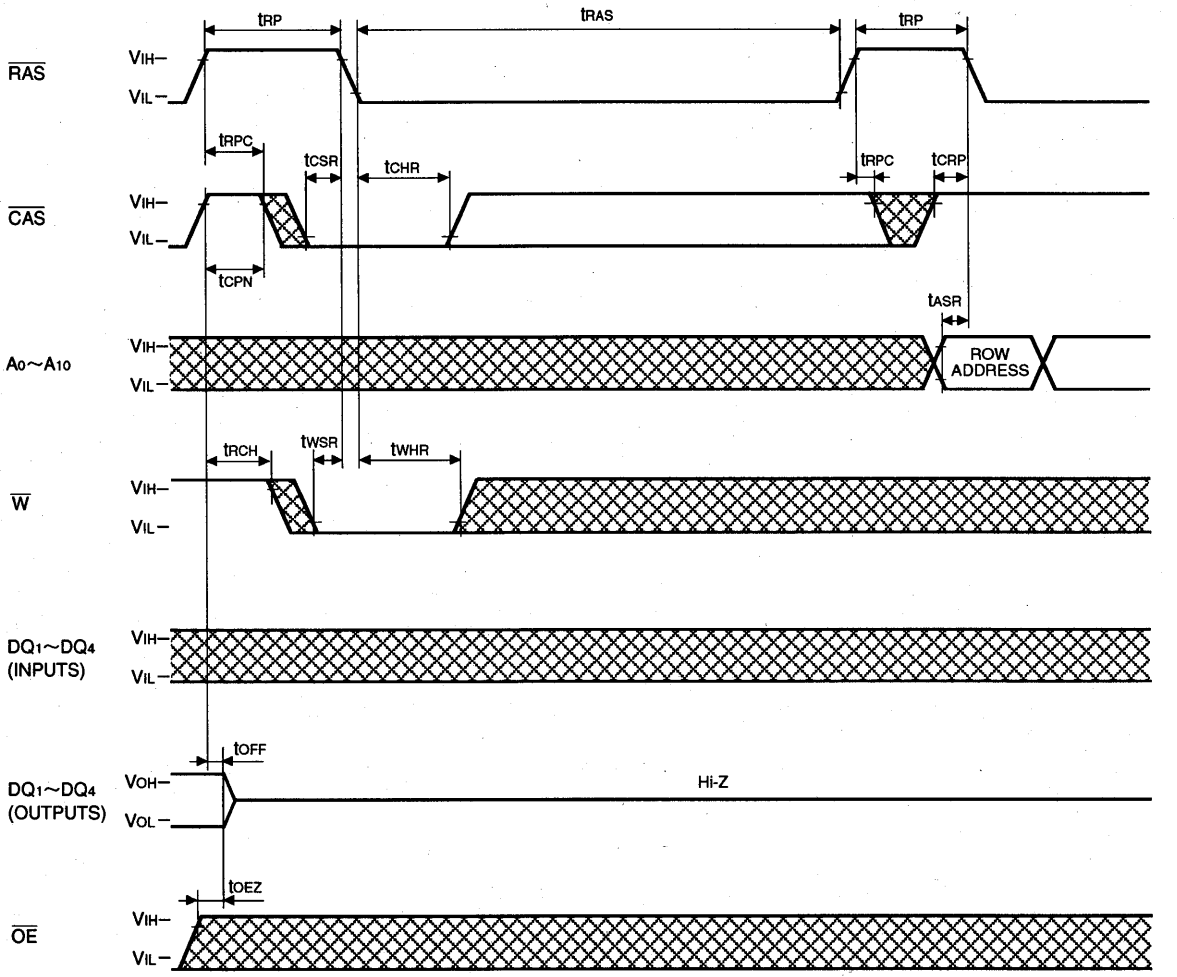
Fast Page Mode Read-Write,Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417405CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417405CXX-5,-5S	50	13	25	13	90	655
M5M417405CXX-6,-6S	60	15	30	15	110	540
M5M417405CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

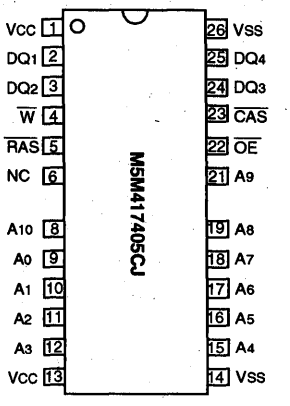
- Standard 26pin SOJ, 26pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 1.1mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M417405Cxx-5,-5S ---------- 800mW (Max)
  - M5M417405Cxx-6,-6S ---------- 660mW (Max)
  - M5M417405Cxx-7,-7S ---------- 580mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 200 μA(Max)
- Hyper page mode (2048-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0 ~ A_{10})

  *:Applicable to self refresh version(M5M417405CJ,TP-5S,-6S, -7S:option) only

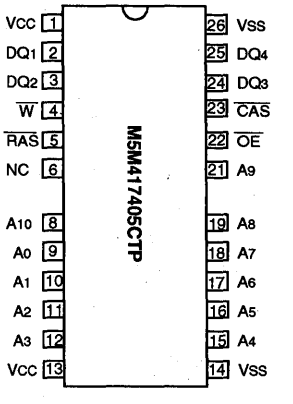
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

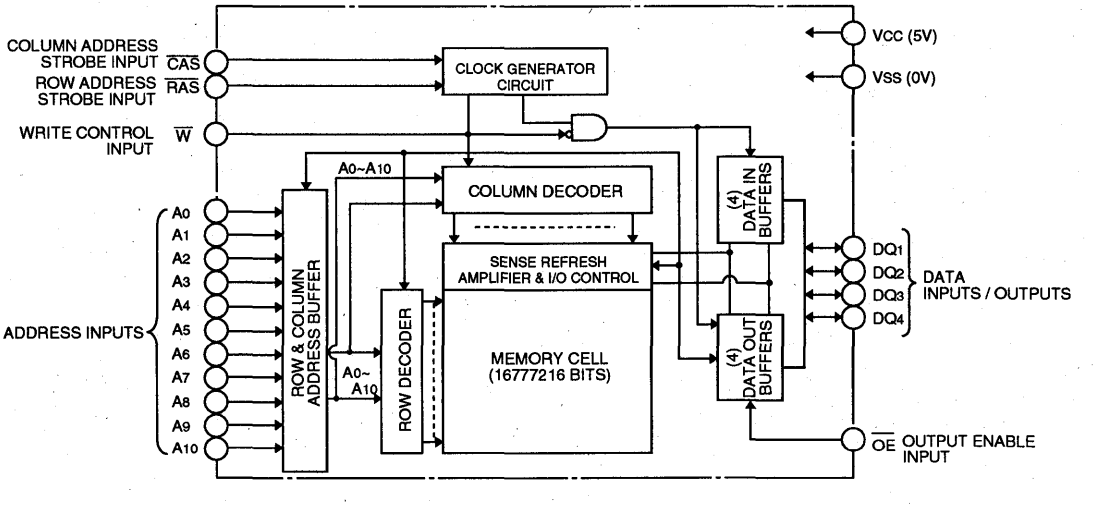
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M417405CJ, TP provides a number of other functions, e.g., $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M5M417405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : VIL(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to VSS.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+6.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M417405C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			145	mA
		M5M417405C-6,-6S	t_{RC}=t_{WC}=min.			120	
		M5M417405C-7,-7S	output open			105	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M417405C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH}			145	mA
		M5M417405C-6,-6S	t_{RC}=min.			120	
		M5M417405C-7,-7S	output open			105	
I_{CC4}(AV)	Average supply current from Vcc, Hyper Page Mode (Note 3,4,5)	M5M417405C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			140	mA
		M5M417405C-6,-6S	t_{HPC}=min.			115	
		M5M417405C-7,-7S	output open			90	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M417405C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			145	mA
		M5M417405C-6,-6S	t_{RC}=min.			120	
		M5M417405C-7,-7S	output open			105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			8	pF

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0～70℃, Vcc = 5V±10 %, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (IOUT≦|±10 μ A|) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ～70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT=2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write/read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper Page Mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 6)	M5M417405C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}$ & $\overline{WE} \leqq 0.2V$ or $\overline{OE}$ & $\overline{WE} \geqq Vcc-0.2V$ $A_0 \sim A_{10} \leqq 0.2V$ or $A_0 \sim A_{10} \geqq Vcc-0.2V$ t_{REF}=128ms (2048cycles) output=OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 6)	M5M417405C (S)	$\overline{RAS}=\overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

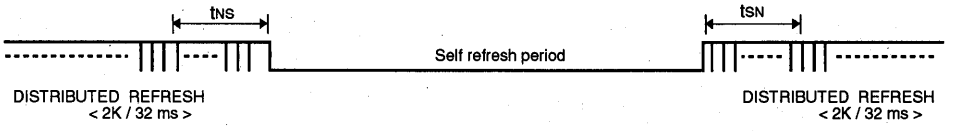
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417405C-5S		M5M417405C-6S		M5M417405C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

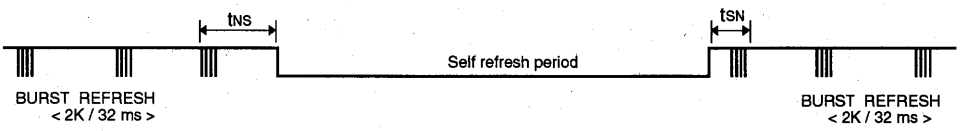
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS}/t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 32$ms and $t_{SN} \leqq 32$ms.



(2) In case of burst refresh

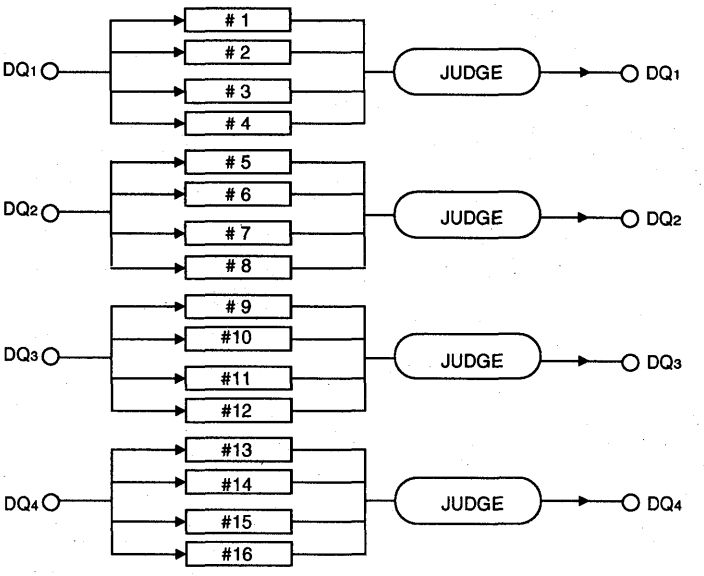
The last / first full refresh cycles (2K) must be made within t_{NS} /t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 32$ms.



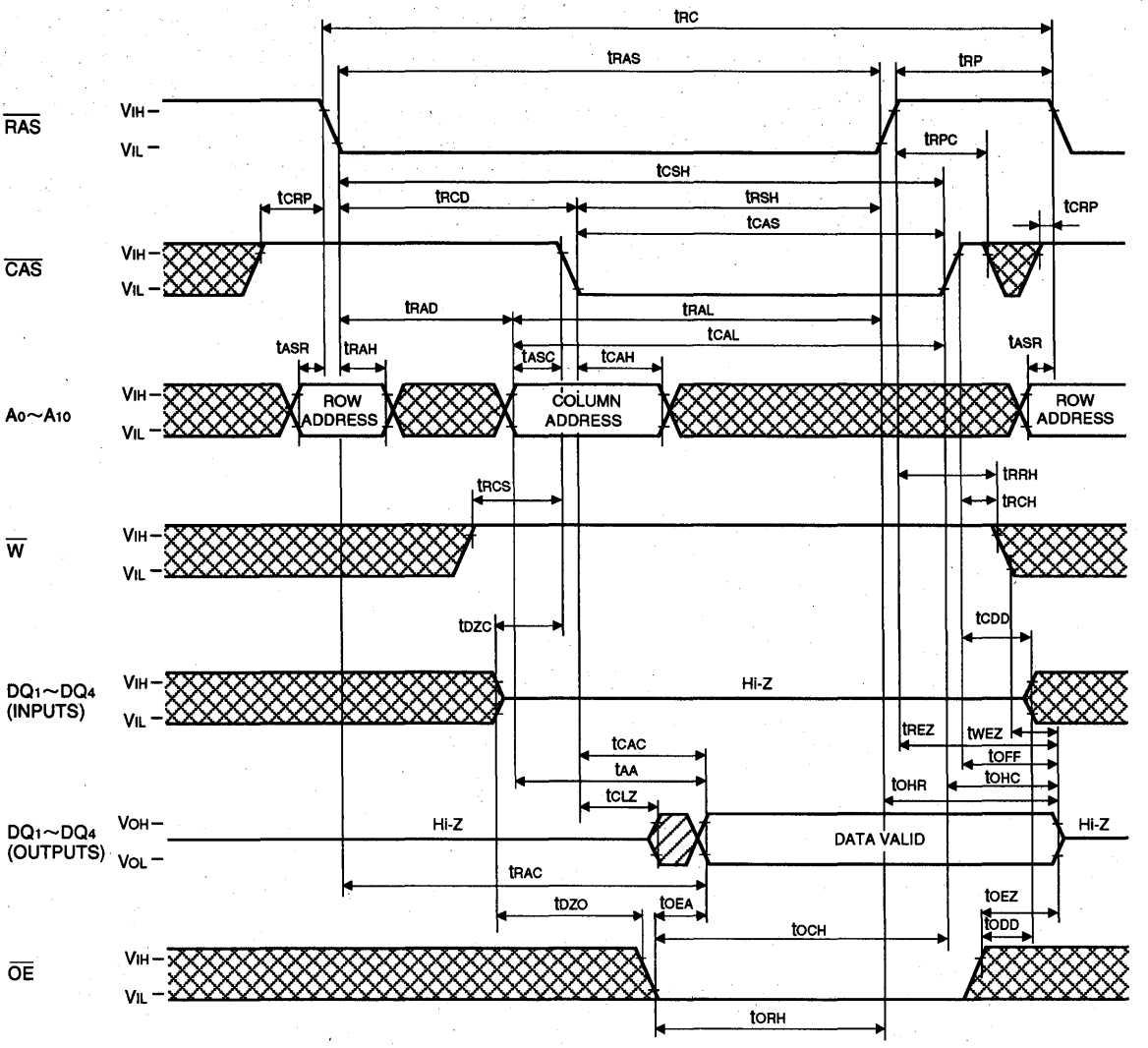
TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M417405C-5,-5S		M5M417405C-6,-6S		M5M417405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0 and CA_1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 32)
Read Cycle



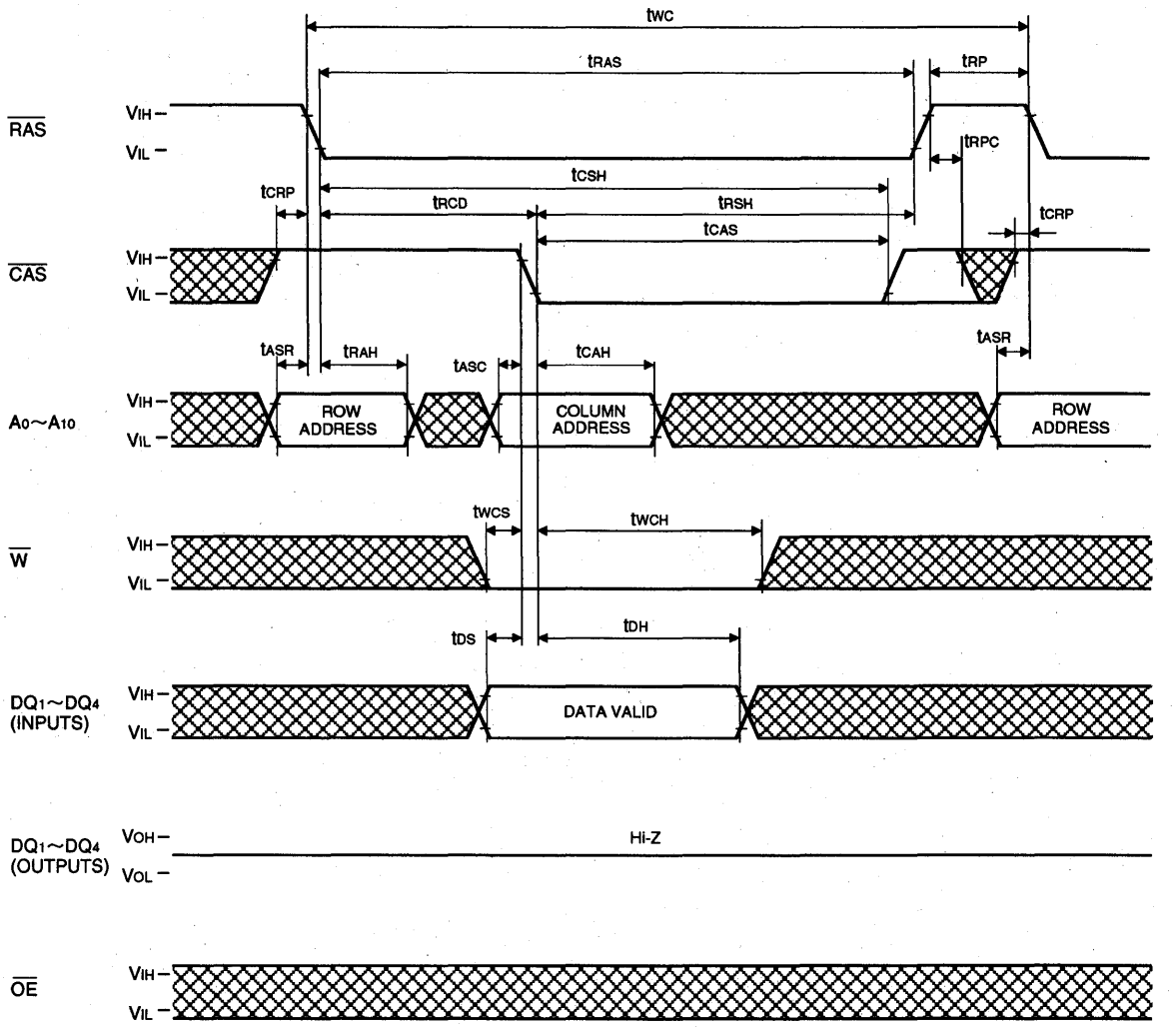
Note 32

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

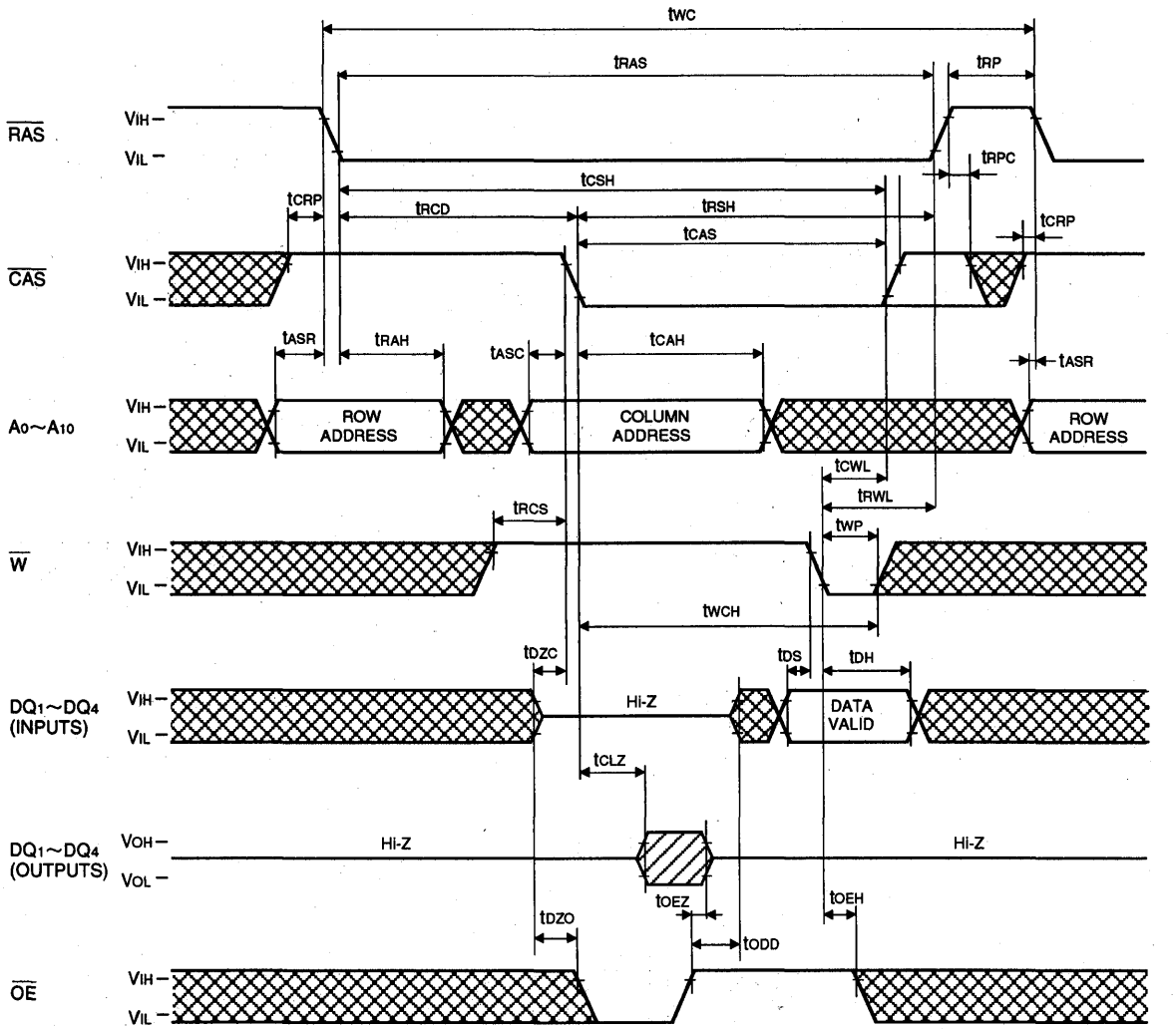
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Early Write Cycle

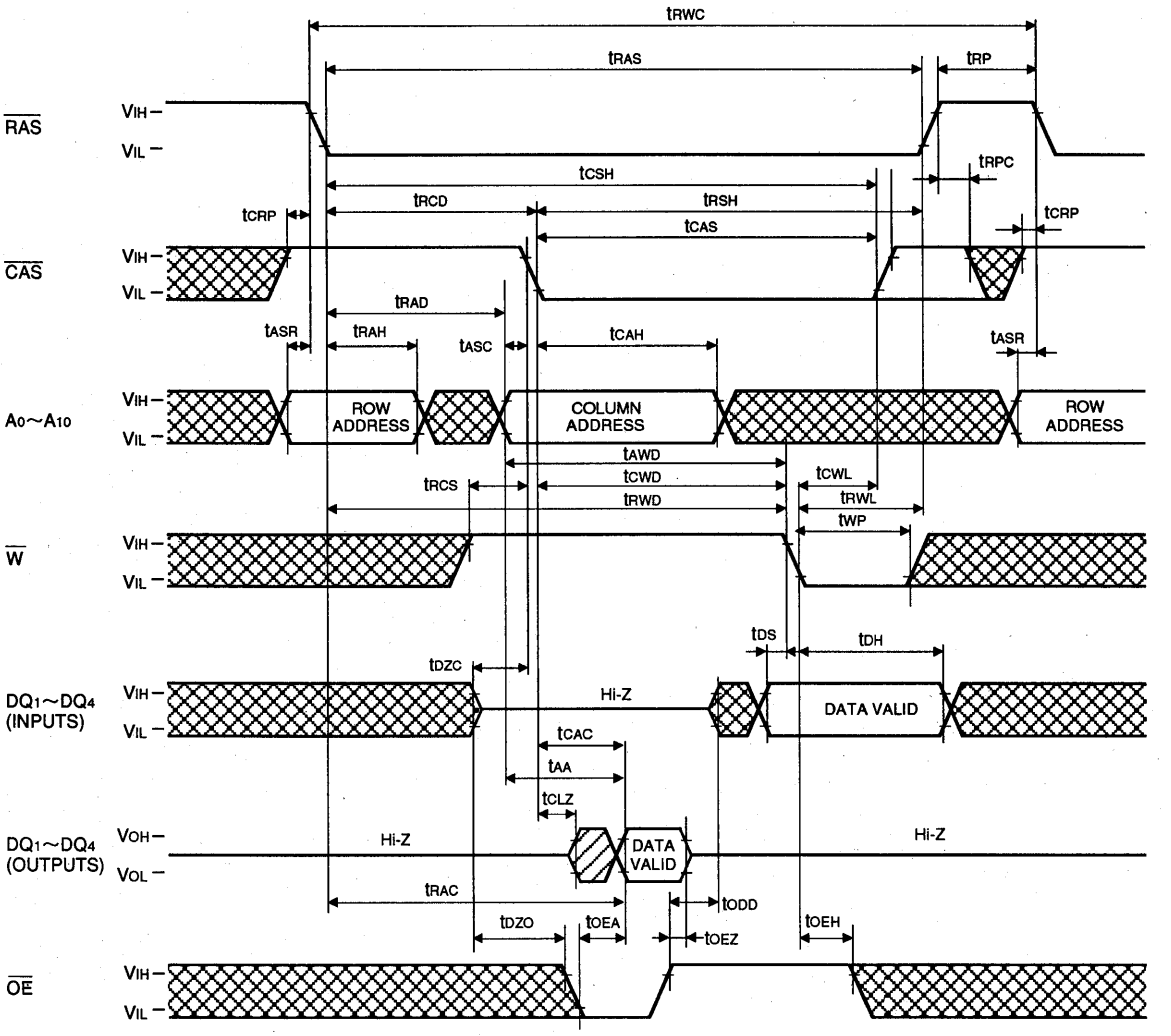


Delayed Write Cycle



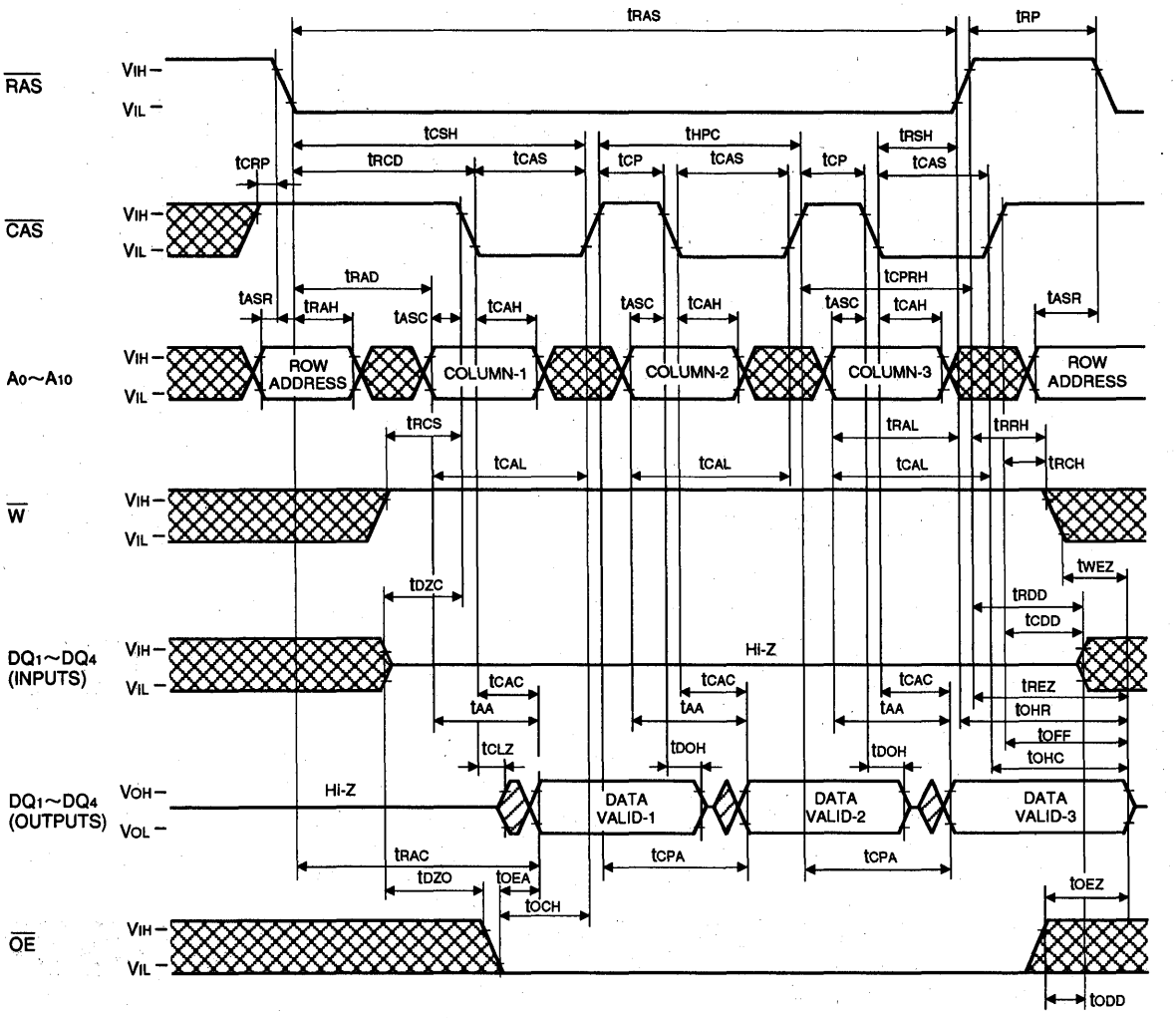
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle



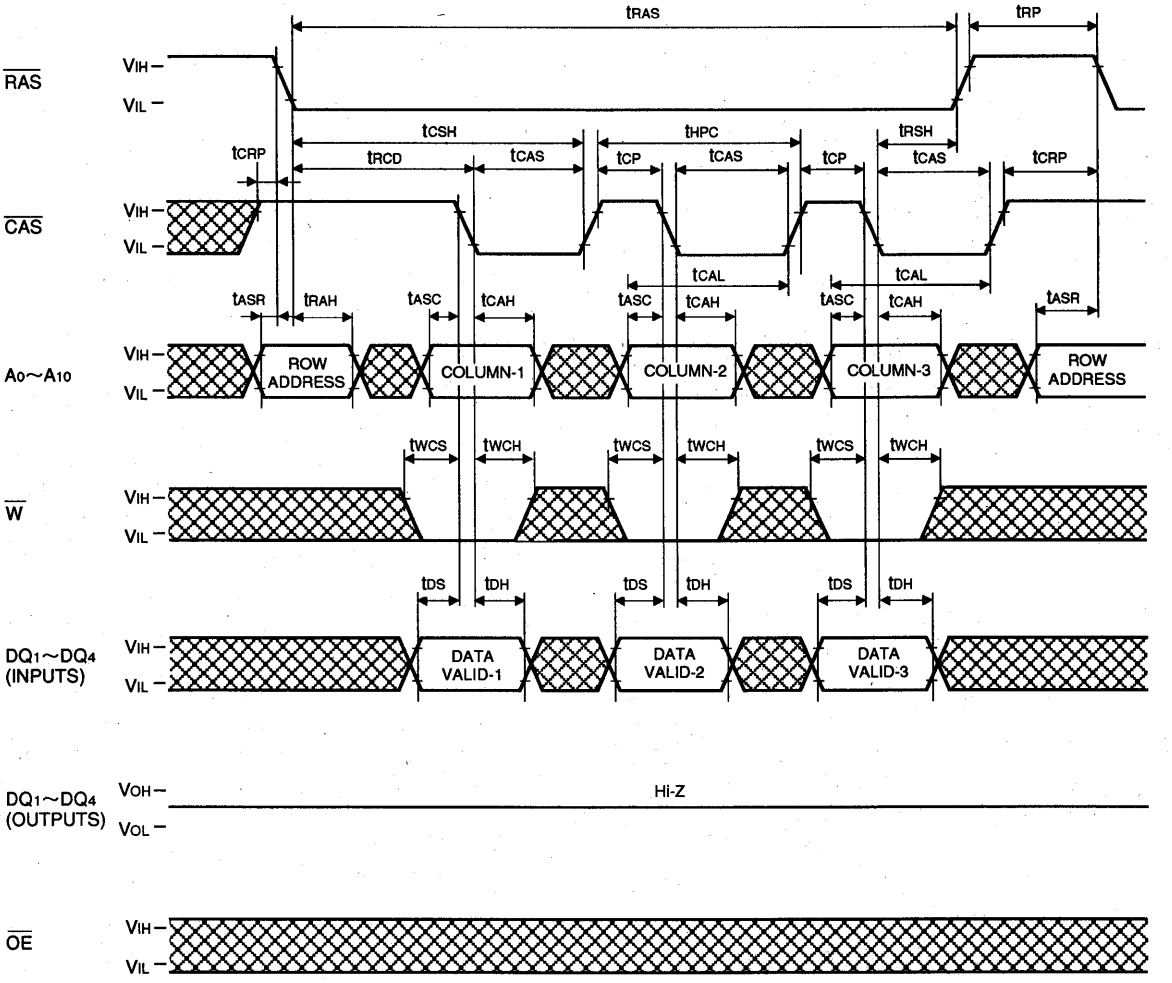
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle



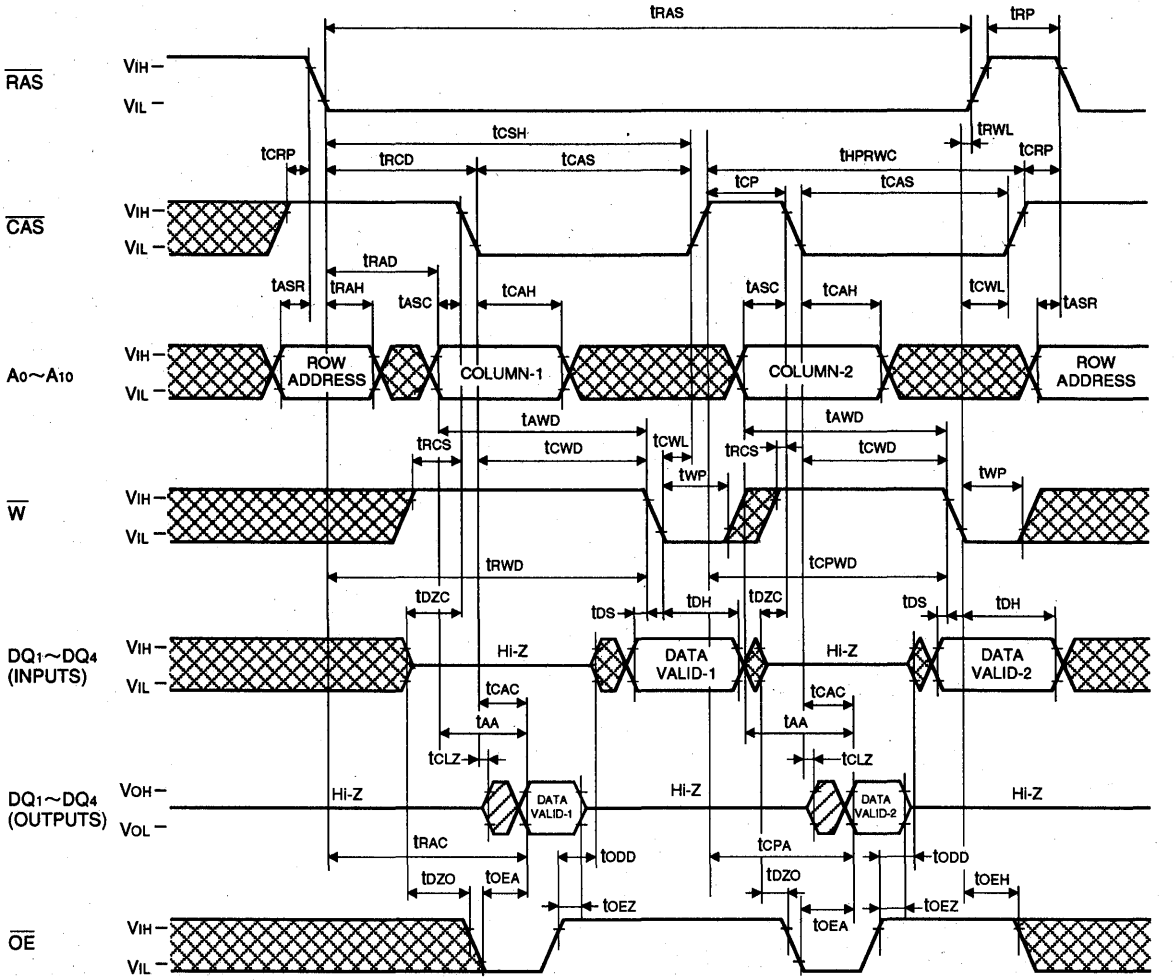
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Early Write Cycle



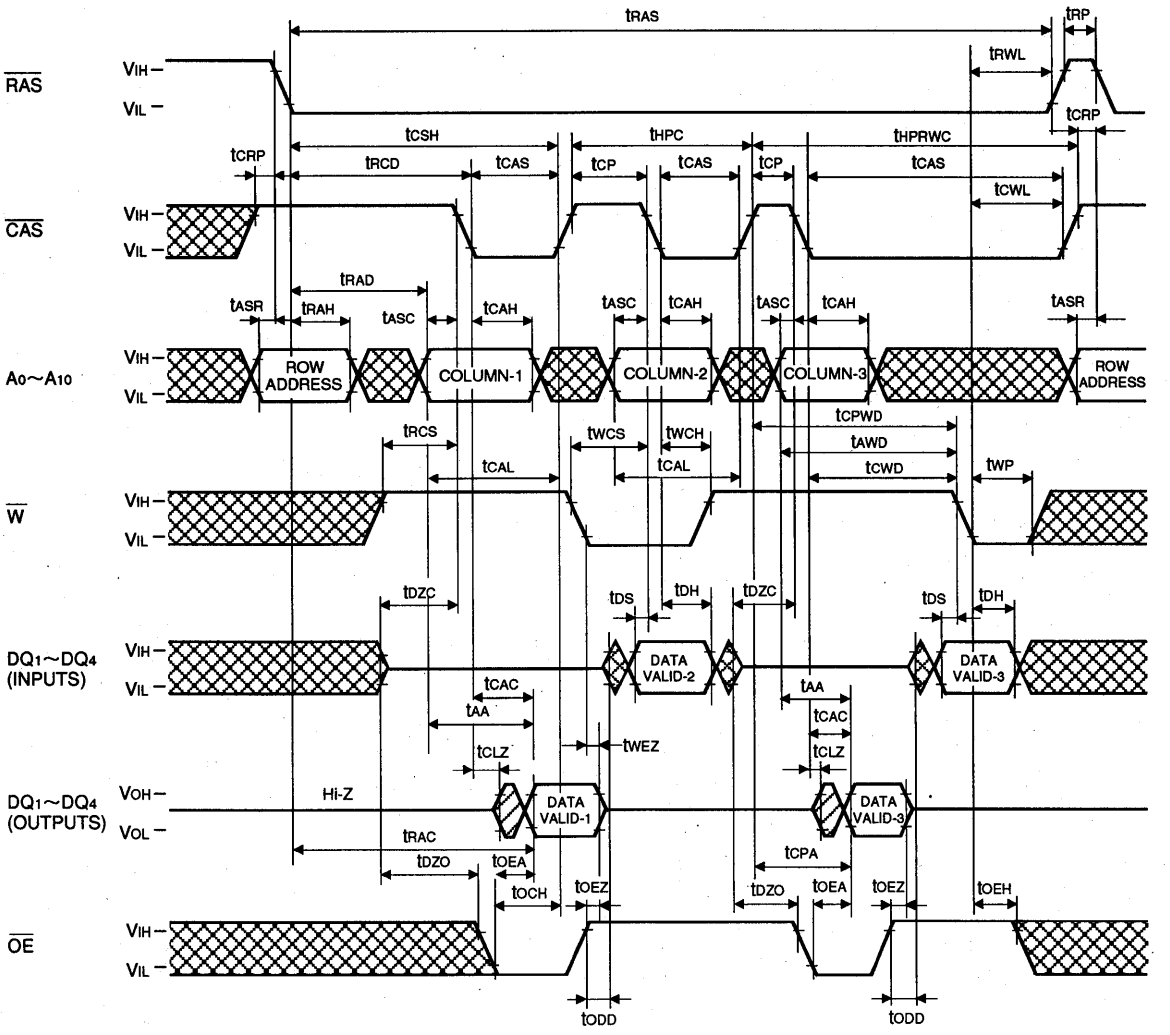
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read-Write, Read-Modify-Write Cycle

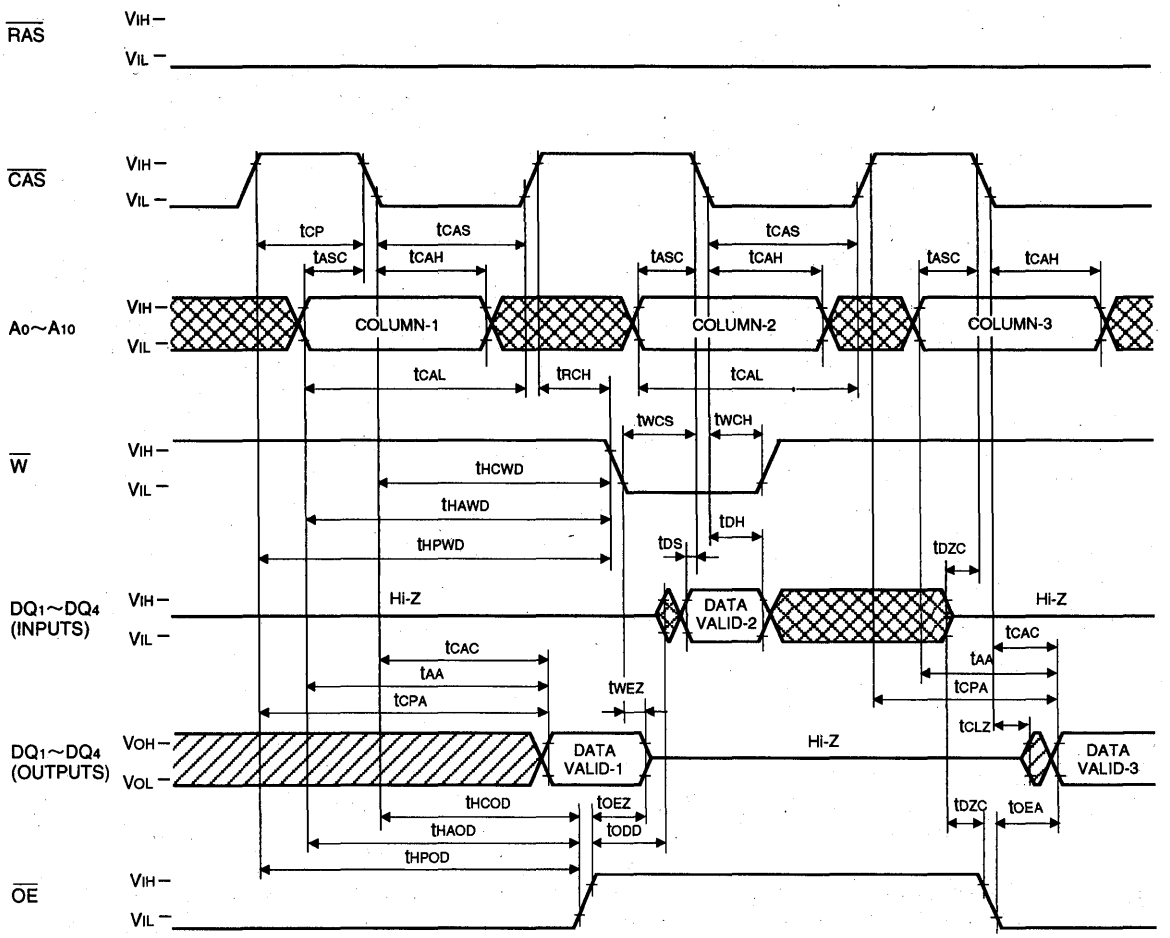


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (1)

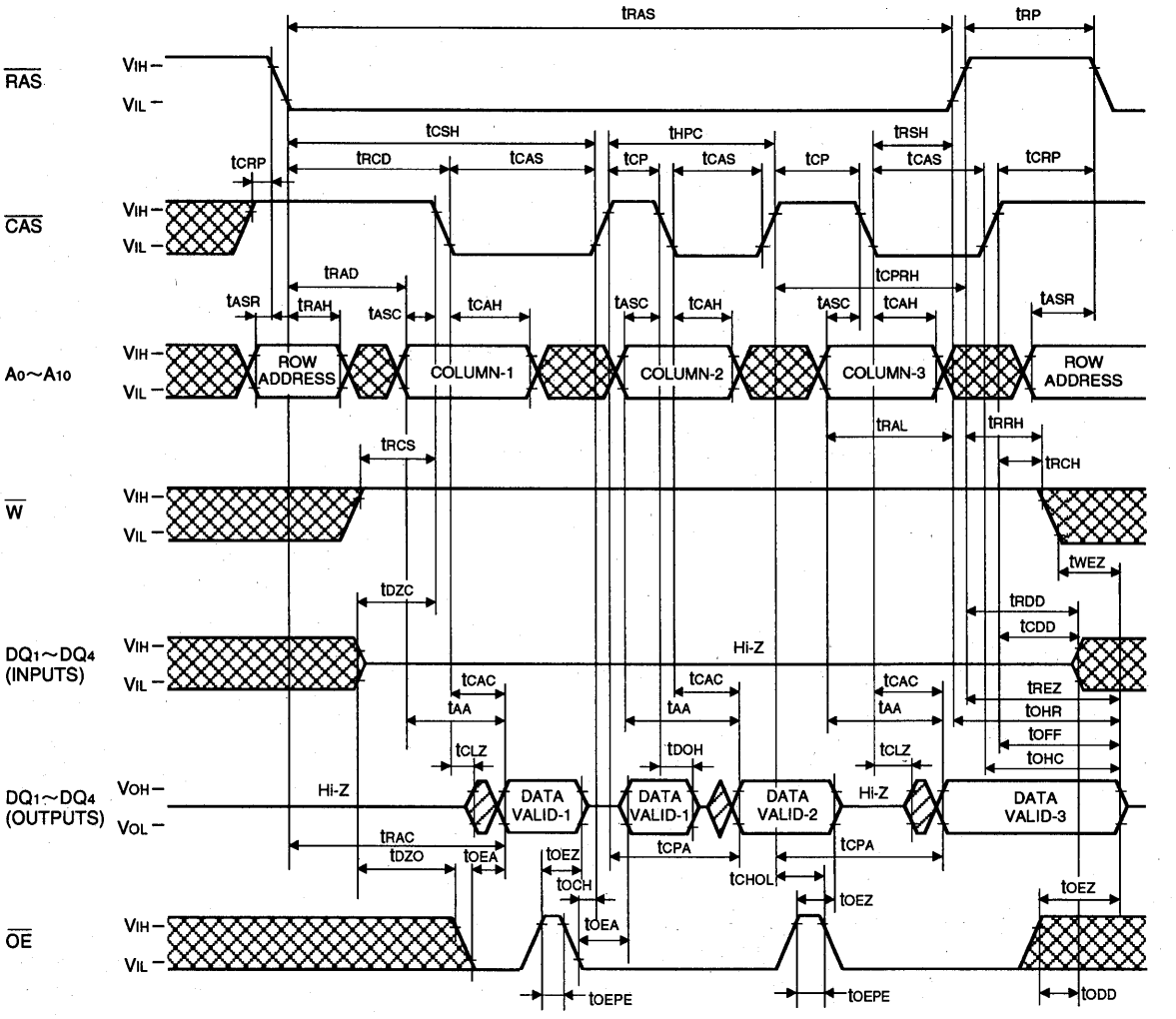


Hyper Page Mode Mix Cycle (2)



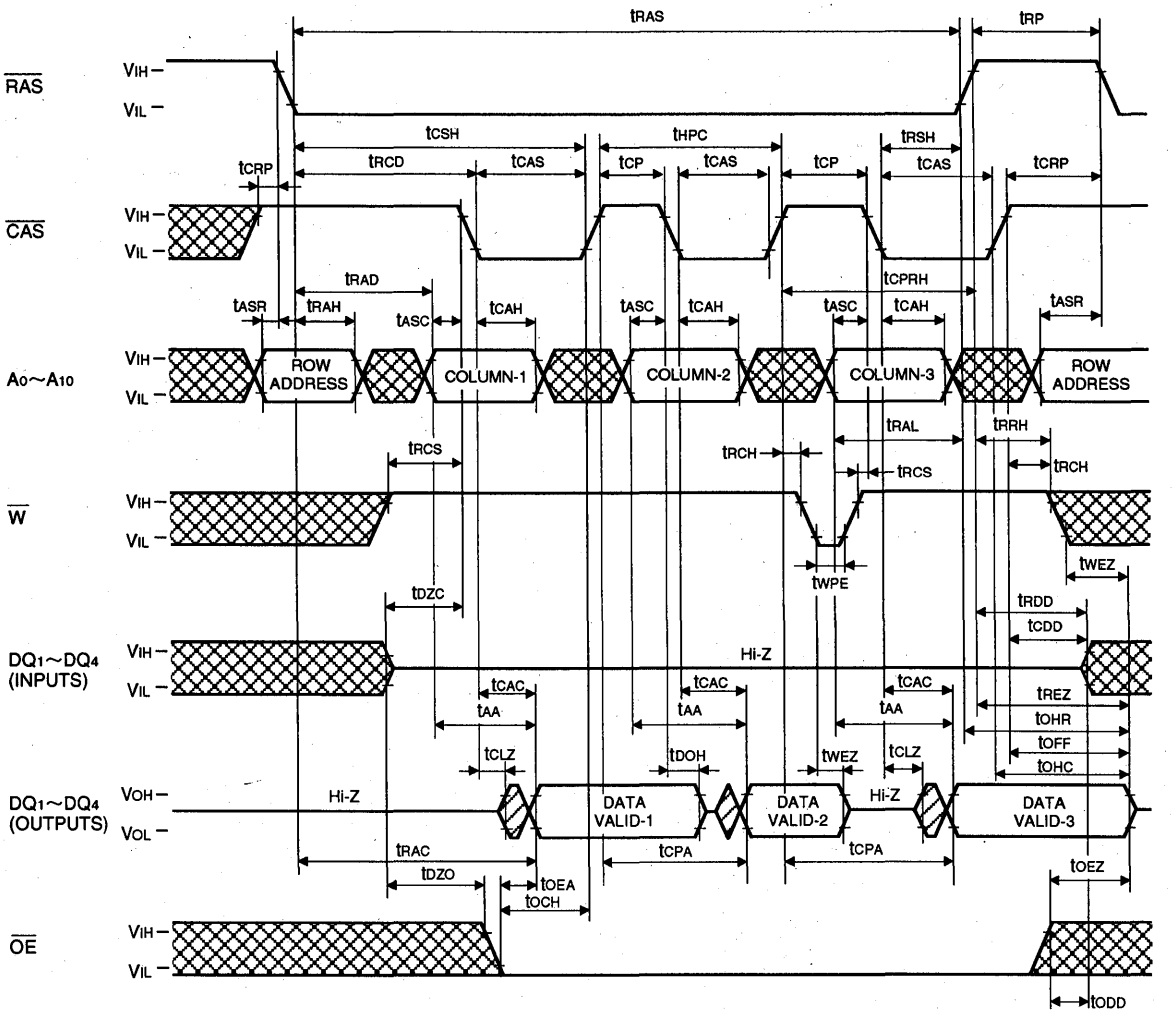
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



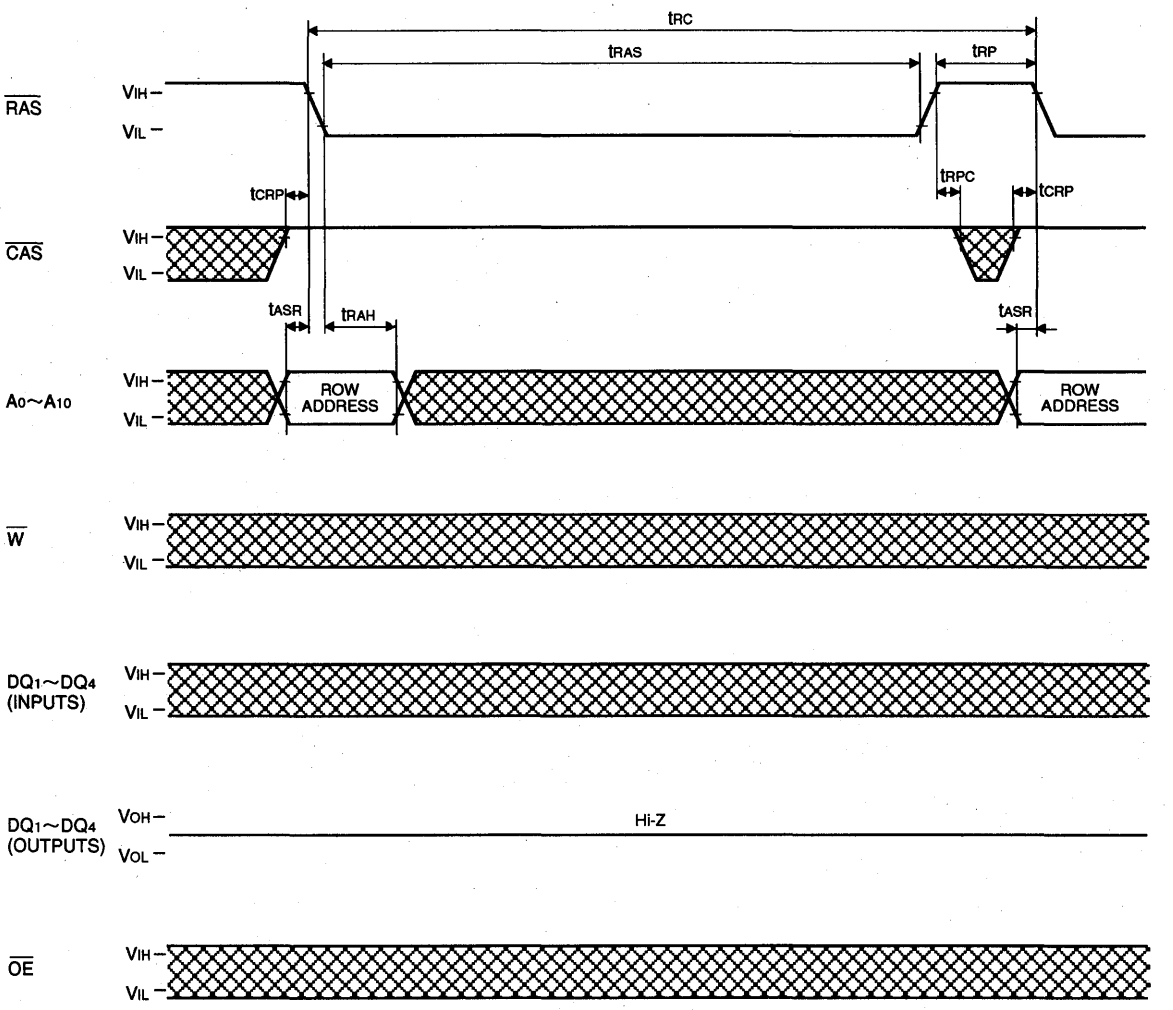
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



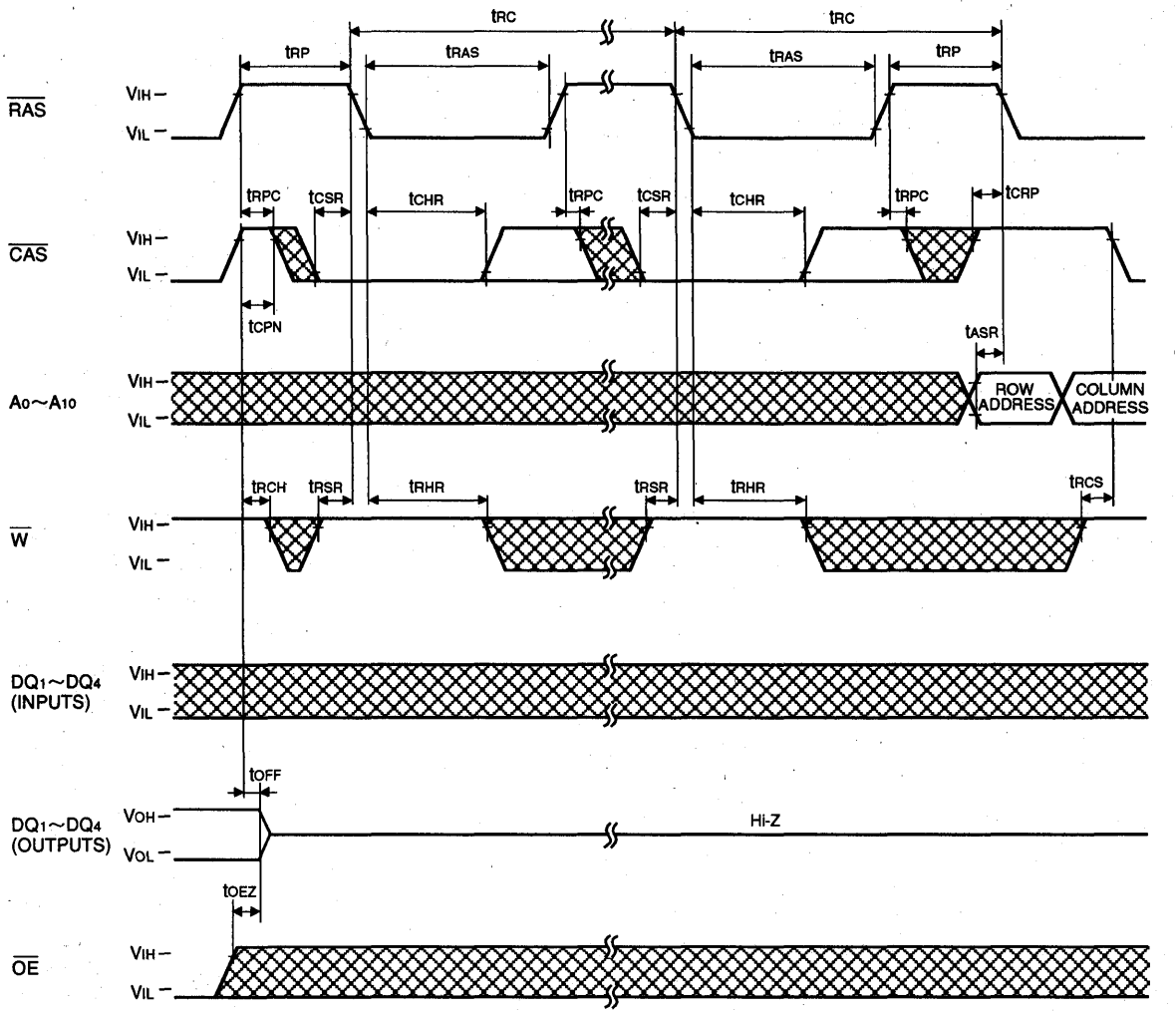
PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle

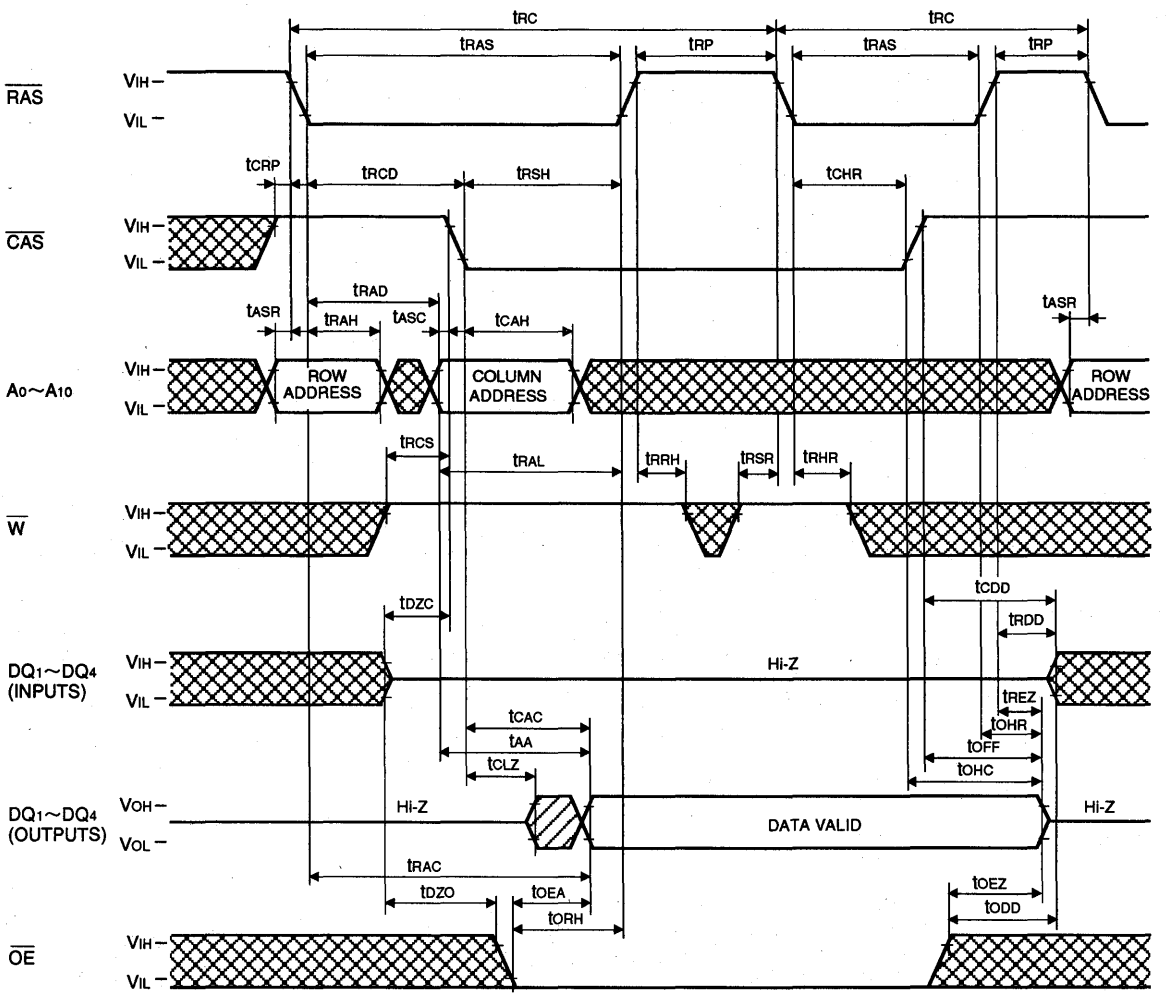


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

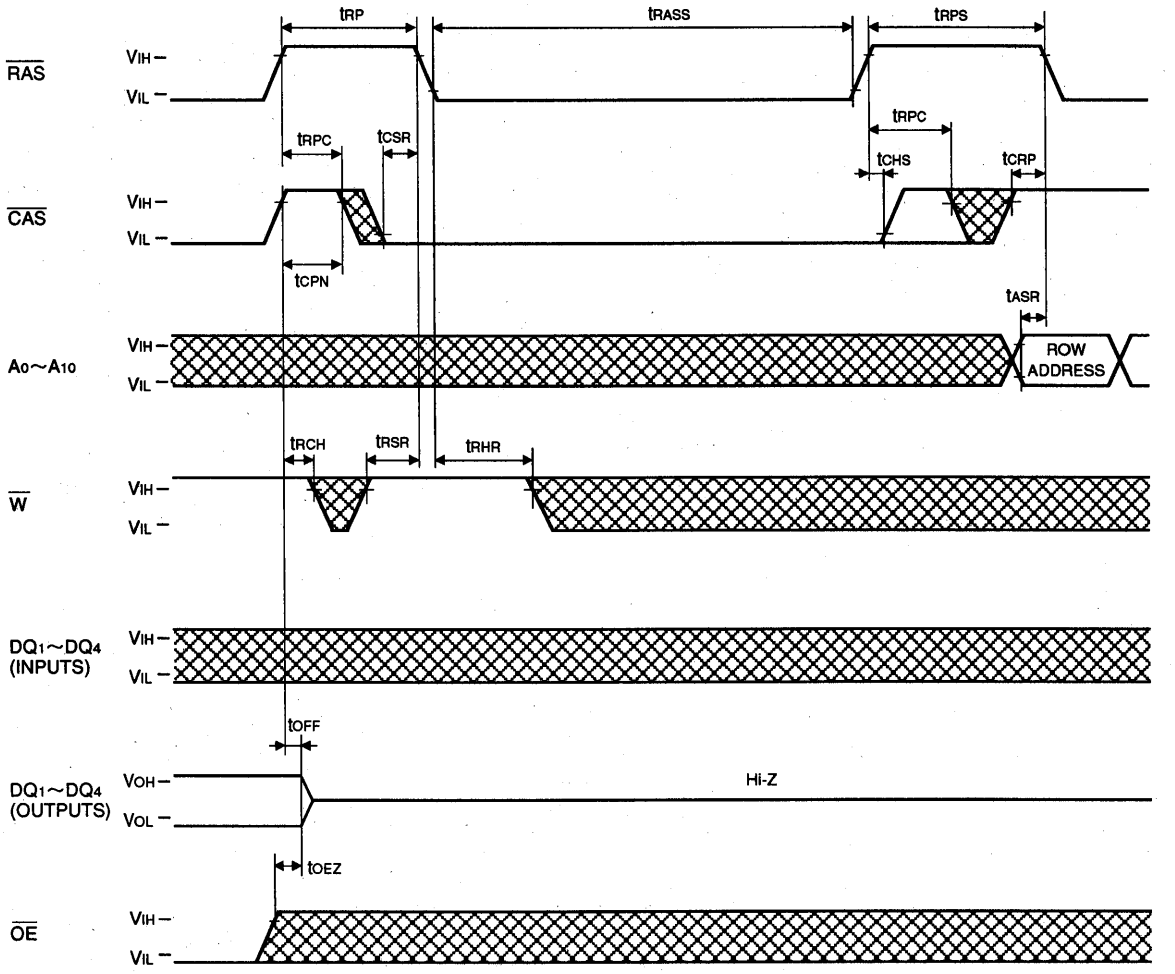


Hidden Refresh Cycle (Read) (Note 33)



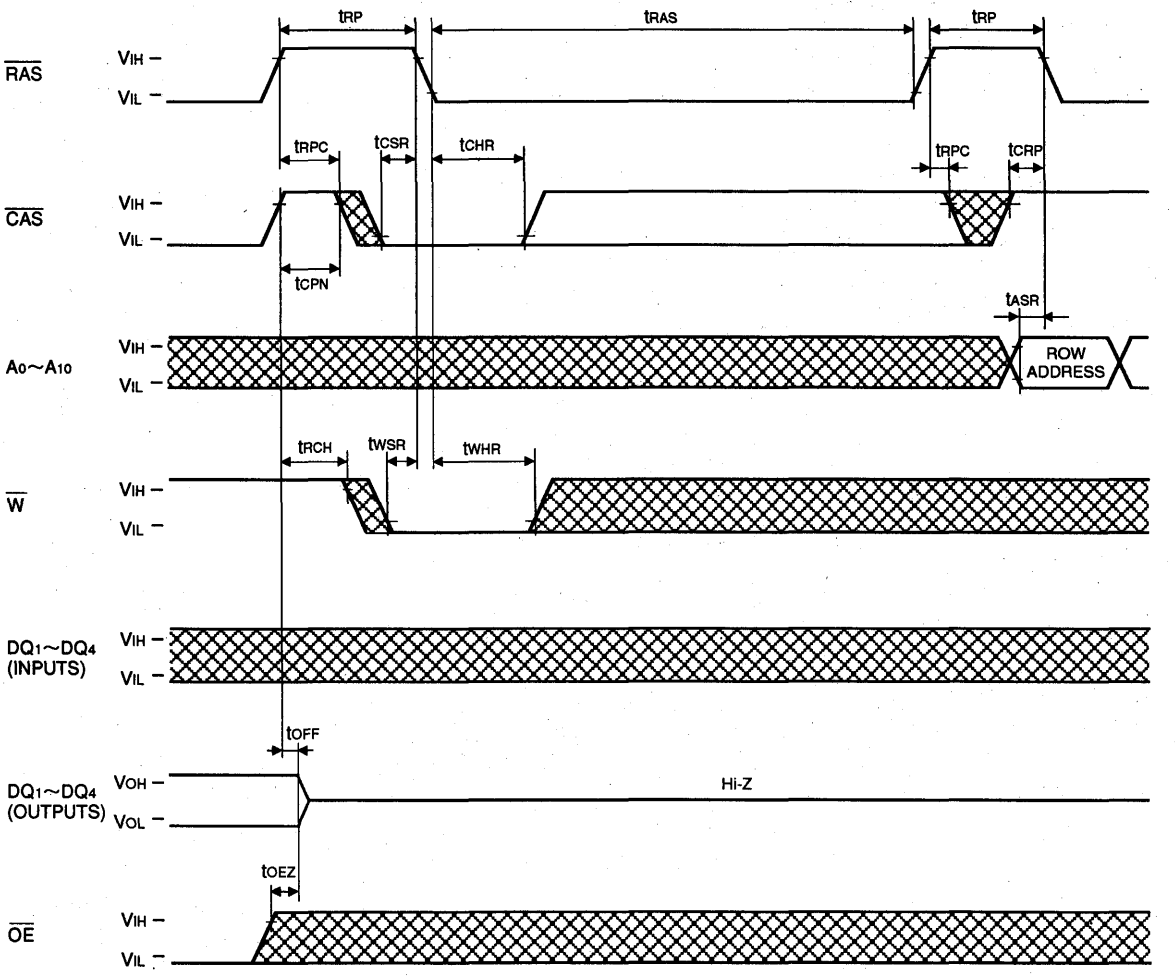
Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle, Slow Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

M5M417800AJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800AXX-6,-6S	60	15	30	15	110	540
M5M417800AXX-7,-7S	70	20	35	20	130	475

XX = J, TP

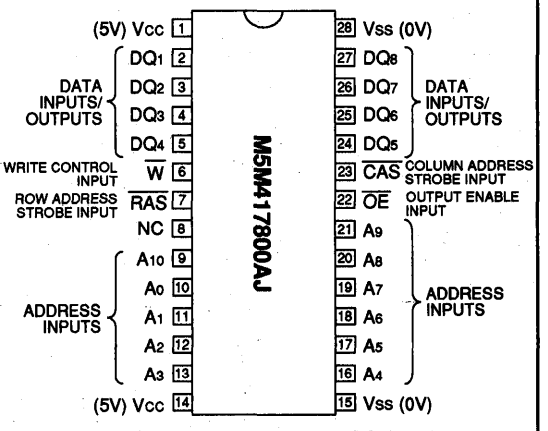
- Standard 28 pin SOJ, 28 pin TSOP
- Single 5V±10%supply
- Low stand-by power dissipation
  - 5.5mW (Max) ····· CMOS Input level
  - 2.2mW*(Max) ····· CMOS Input level
- Low operating power dissipation
  - M5M417800Axx- 6, -6S ····· 660.0mW (Max)
  - M5M417800Axx- 7, -7S ····· 580.0mW (Max)
- Self refresh capability *
  - self refresh current ····· 400.0μA (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

*Applicable to self refresh version (M5M417800AJ, TP-6S, -7S : option only)

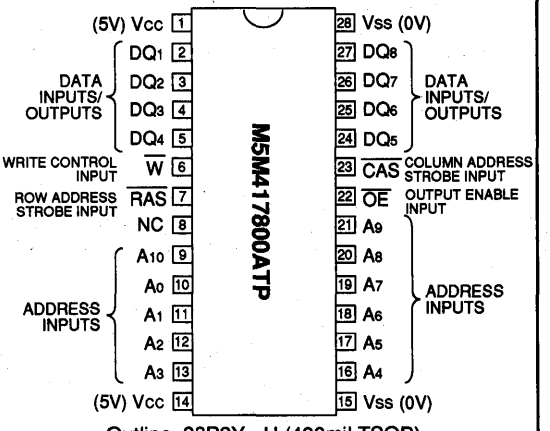
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K (400mil SOJ)



Outline 28P3Y - H (400mil TSOP)

NC : NO CONNECTION

FUNCTION

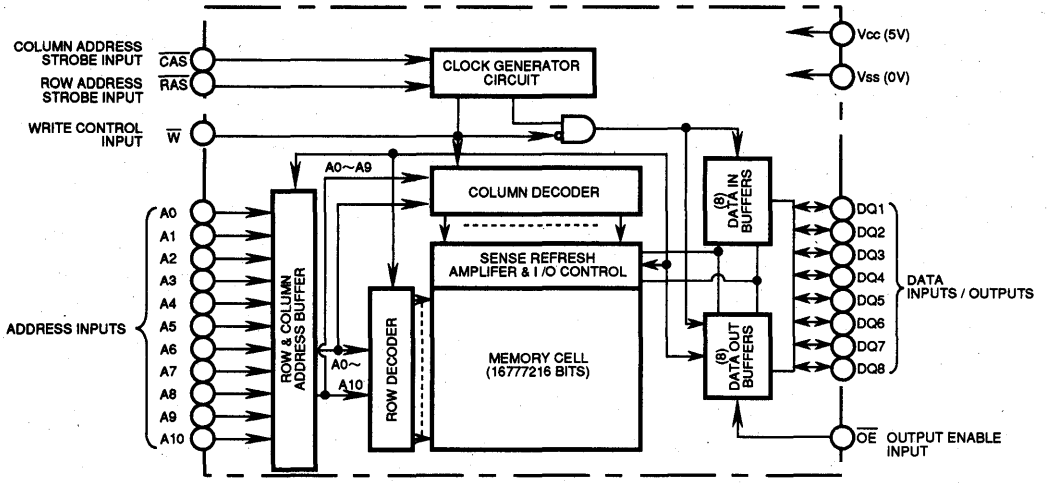
The M5M417800AJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	−1∼7	V
V_I	Input voltage		−1∼7	V
Vo	Output voltage		−1∼7	V
Io	Output current		50	mA
Pd	Power dissipation	Ta = 25℃	1000	mW
Topr	Operating temperature		0∼70	℃
Tstg	Storage temperature		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0∼70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	−1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta = 0∼70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, Other inputs pins = 0V	−10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4)	M5M417800A-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			120	mA
		M5M417800A-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by		$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$≧Vcc -0.5			1	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3)	M5M417800A-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			120	mA
		M5M417800A-7,-7S				105	
I_{CC4} (AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M417800A-6,-6S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			70	mA
		M5M417800A-7,-7S				60	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417800A-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			120	mA
		M5M417800A-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0∼70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = Vss f = 1MHz V_I = 25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		60		70	ns
tAA	Columu address access time	(Note 6,9)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	15	ns

Note 5 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.
7 : Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max).
8 : Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
9 : Assumes that $t_{RAD} \geqq t_{RAD}$ (max) and $t_{ASC} \leqq t_{ASC}$ (max).
10 : Assumes that $t_{CP} \leqq t_{CP}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max).
11 : tOFF (max) and tOEZ (max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq I \pm 10\ \mu A$) and is not reference to VOH (min) or VOL (max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			32		32	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note18)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note18)	15		15		ns
tT	Transition time	(Note19)	1	50	1	50	ns

Note 12 : The timing requirements are assumed tT =5ns.
13 : VIH (min) and VIL (max) are reference levels for measuring timing of input signals.
14 : tRCD (max) is specified as a reference point only. If tRCD is less than tRCD (max), access time is tRAC. If tRCD is greater than tRCD (max), access time is controlled exclusively by tCAC or tAA. tRCD (min) is specified as tRCD (min) = tRAH (min) + 2tH + tASC (min).
15 : tRAD (max) is specified as a reference point only. If $t_{RAD} \geqq t_{RAD}$ (max) and $t_{ASC} \leqq t_{ASC}$ (max), access time is controlled exclusively by tAA.
16 : tASC (max) is specified as a reference point only. If $t_{RCD} \geqq t_{RCD}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max), access time is controlled exclusively by tCAC.
17 : Either tDZC or tDZO must be satisfied.
18 : Either tCDD or tODD must be satisfied.
19 : tT is measured between VIH (min) and VIL (max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 20 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note21)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note22)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note22)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note22)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 21 : t_{RWC} is specified as t_{RWC} (min) = t_{RAC} (max) + t_{ODD} (min) + t_{RWL} (min) + t_{RP} (min) + 5t_{TT}.
22 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS}$ (min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note24)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note25)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note22)	60		65		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24 : t_{RAS} (min) is specified as two cycles of $\overline{CAS}$ input are performed.
25 : t_{CP} (max) is specified as a reference point only.

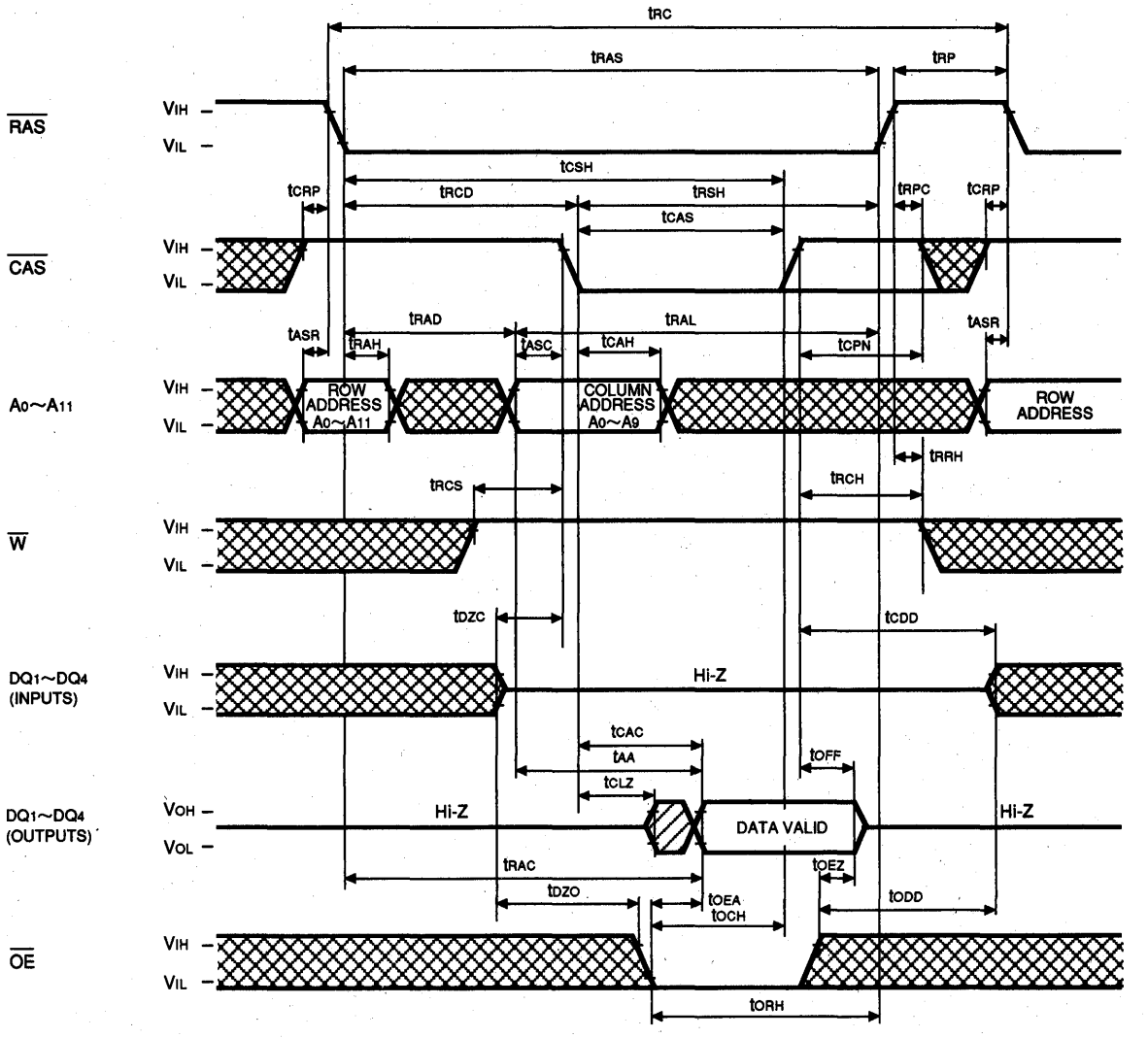
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 26 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 27)

Read Cycle

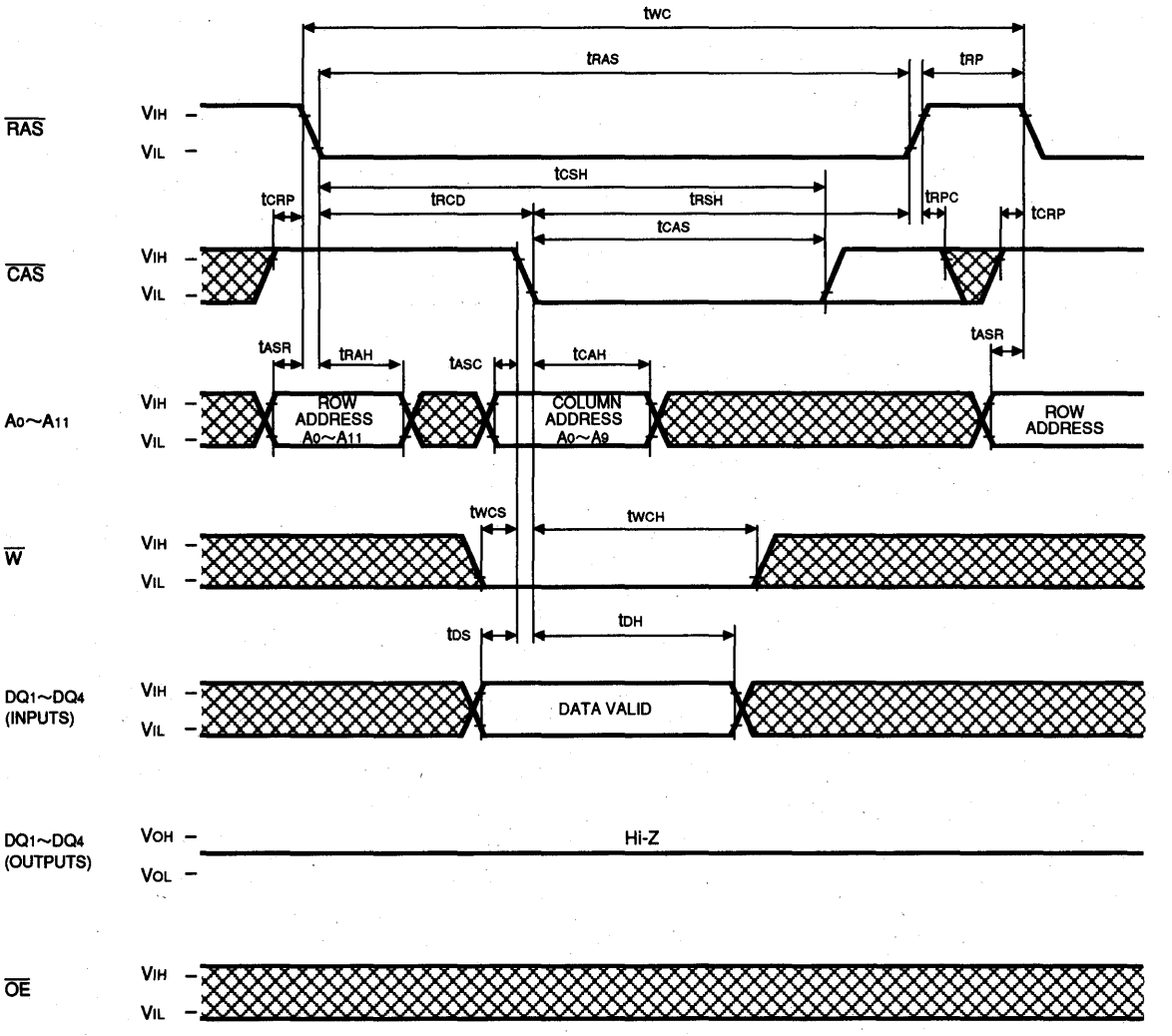


Note 27

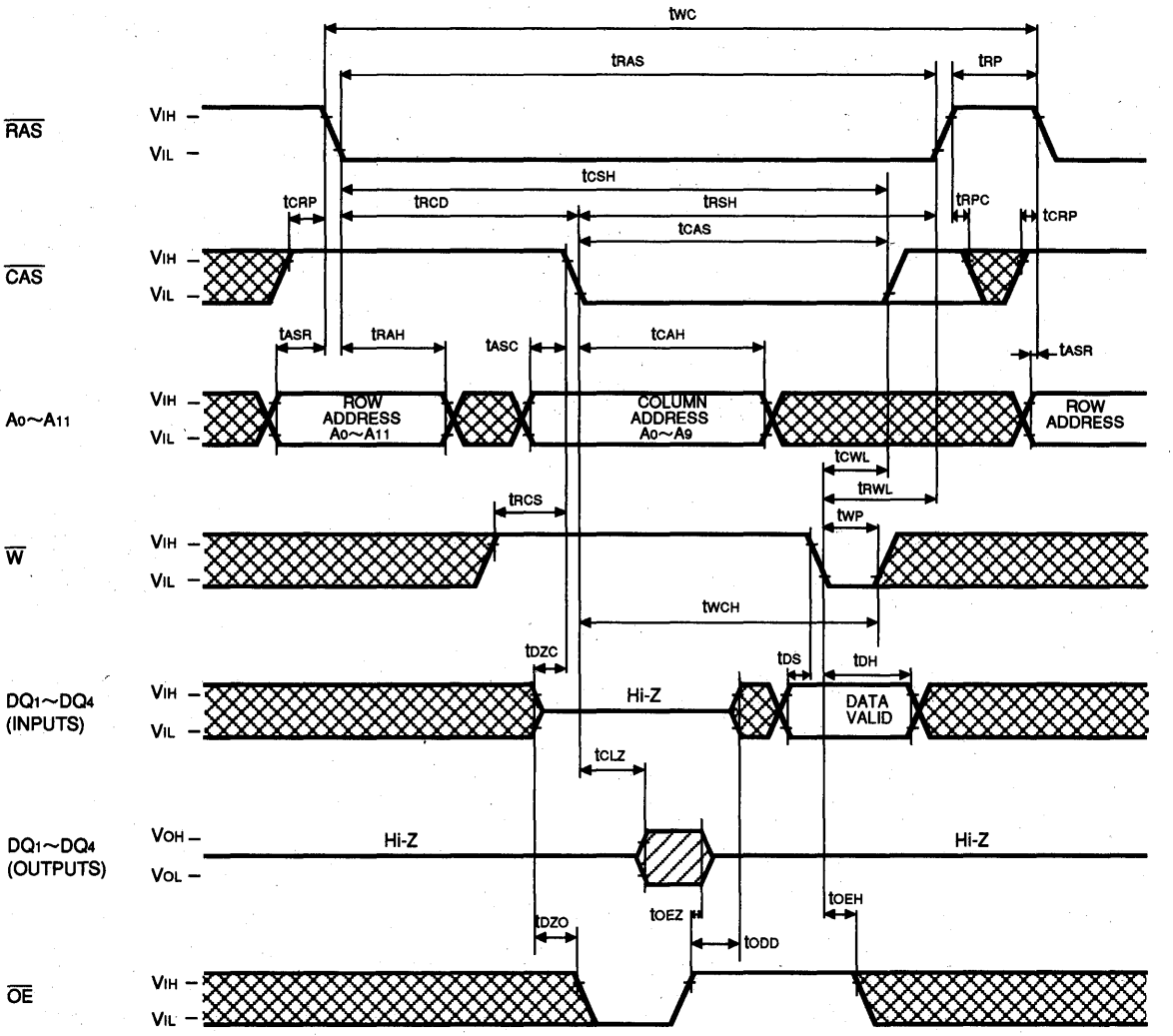
Indicates the don't care input.
$V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

Indicates the invalid output.

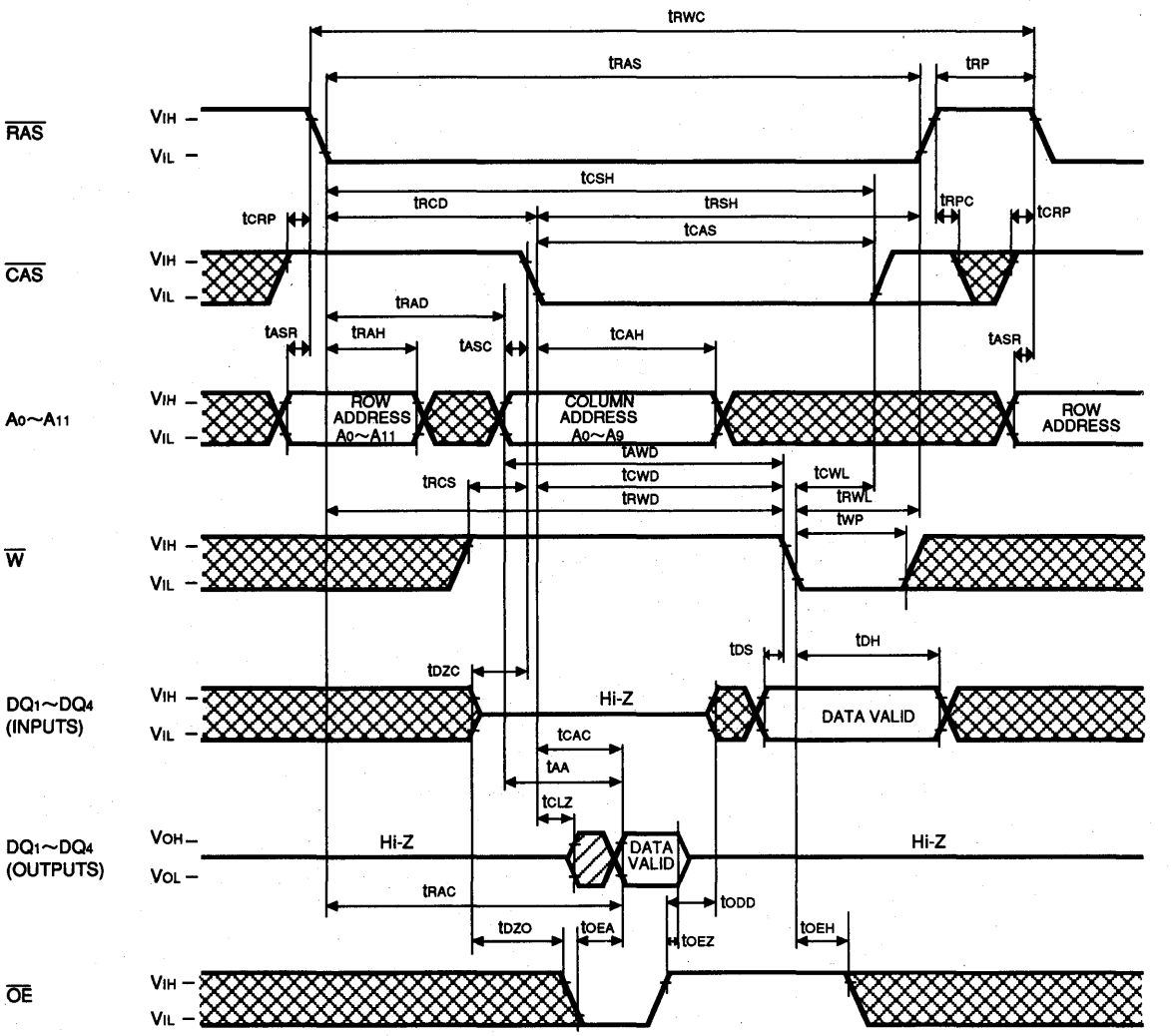
Write Cycle (Early write)



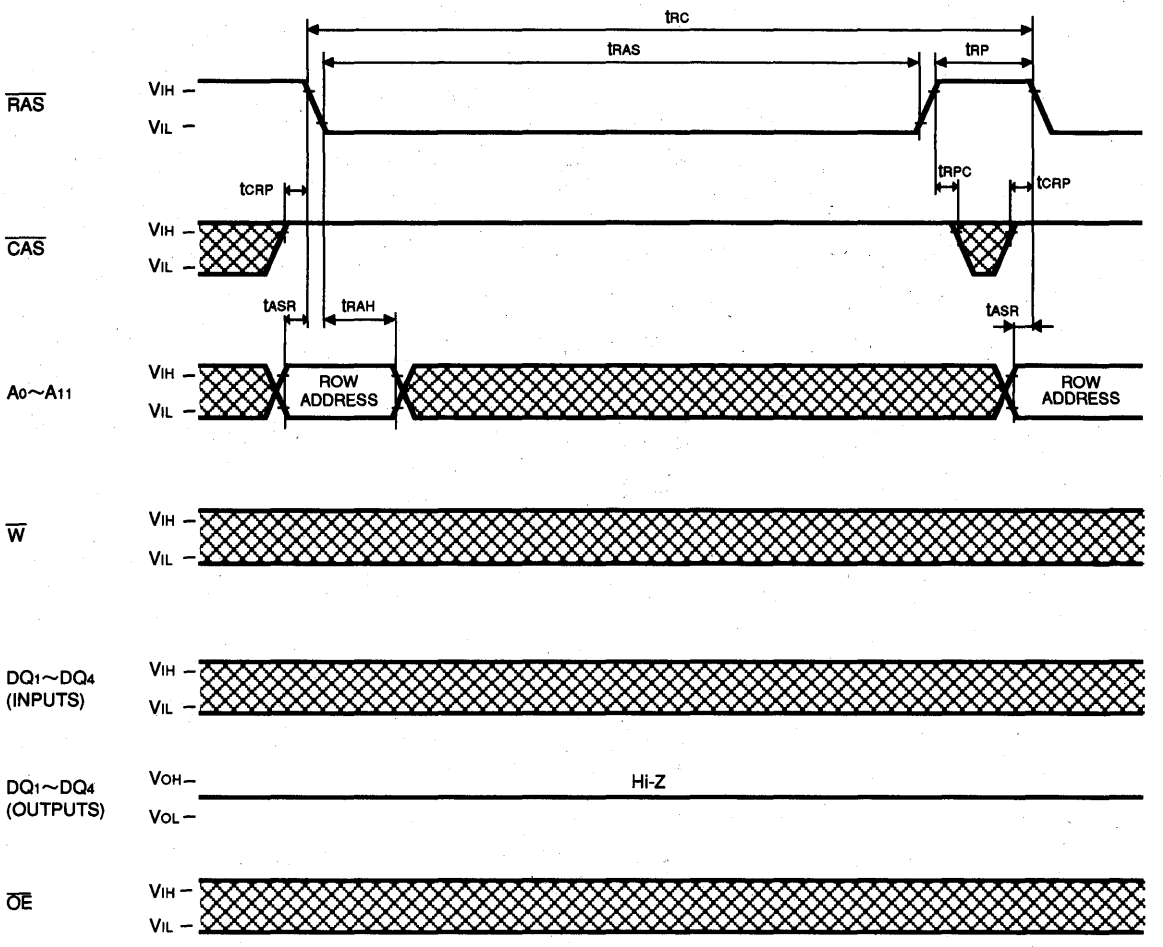
Write Cycle (Delayed write)



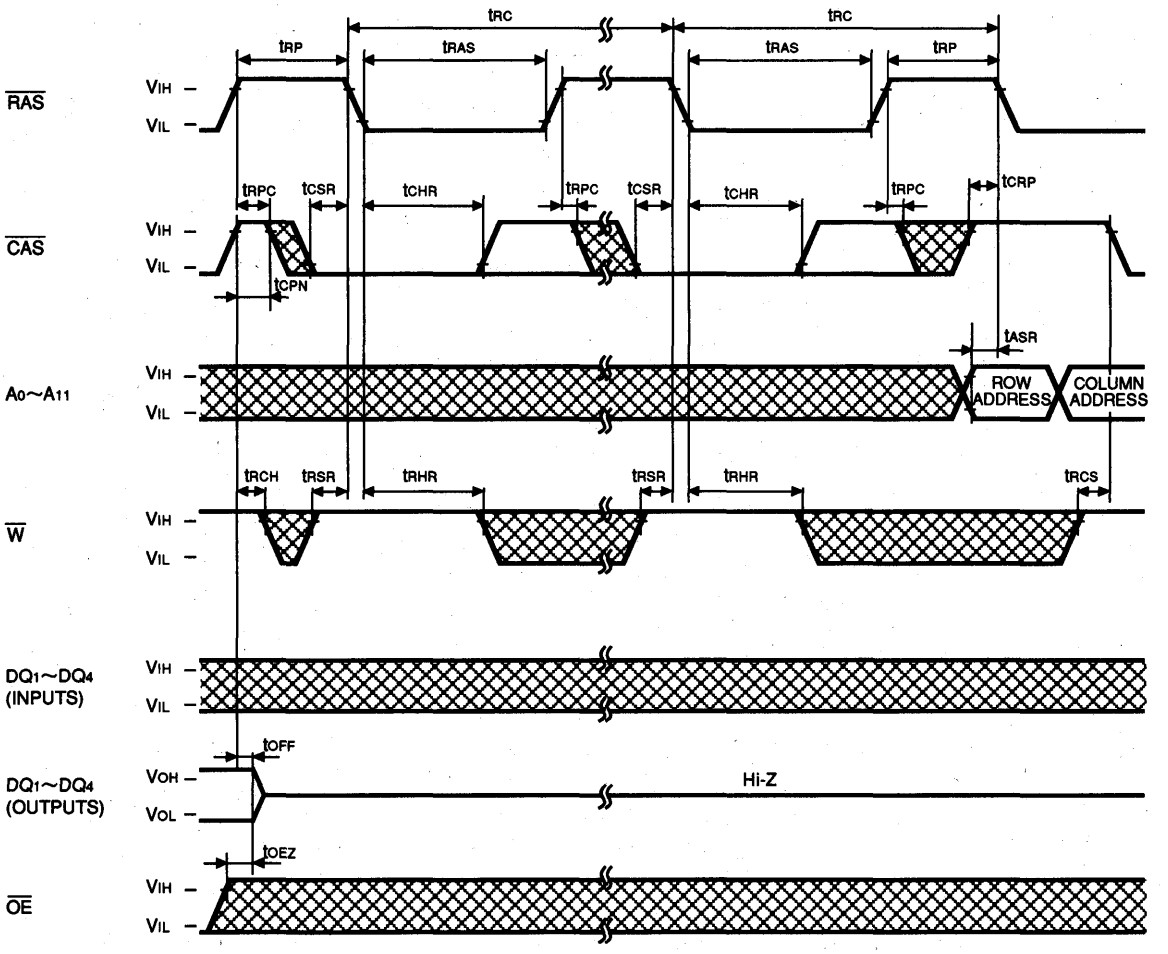
Read-Write, Read-Modify-Write Cycle



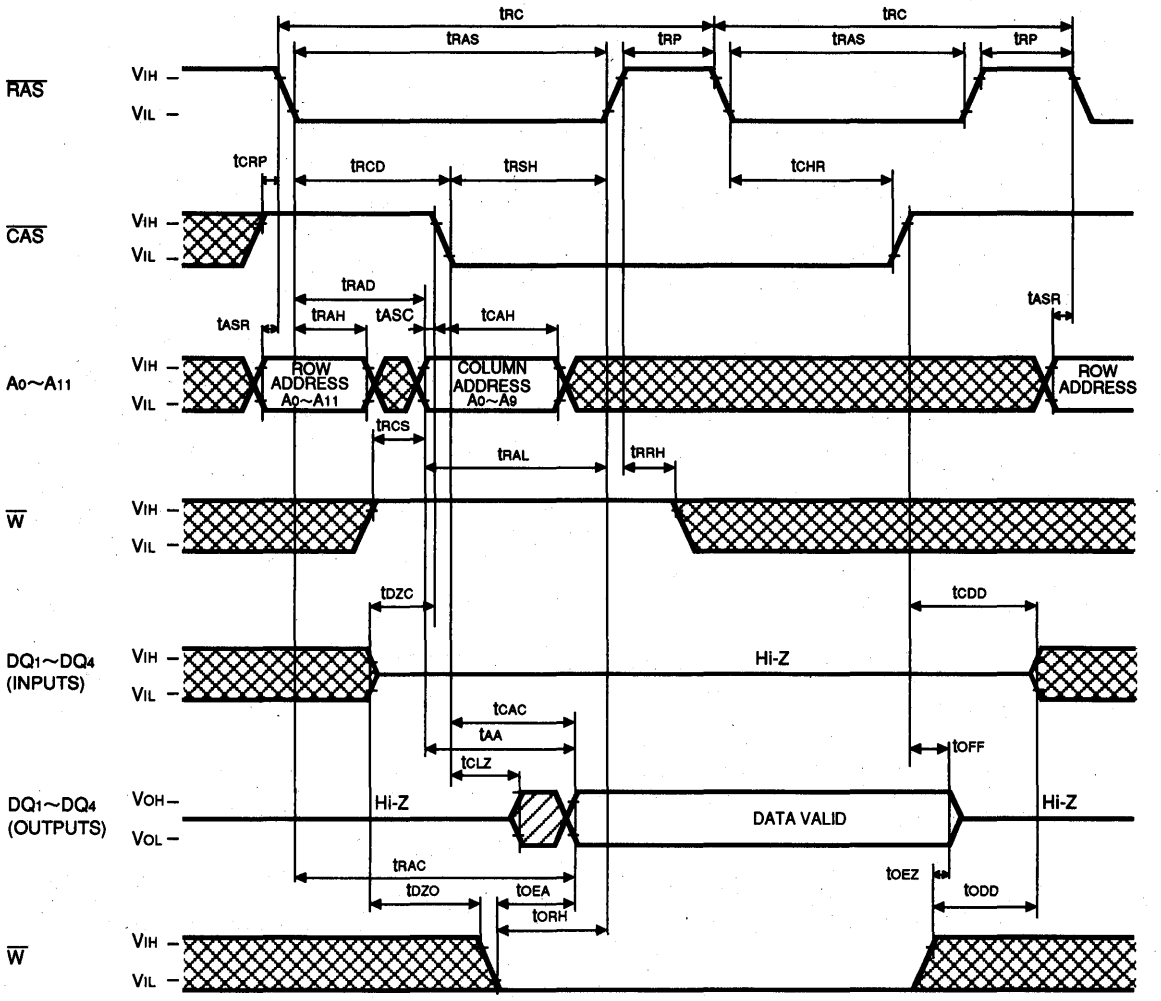
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

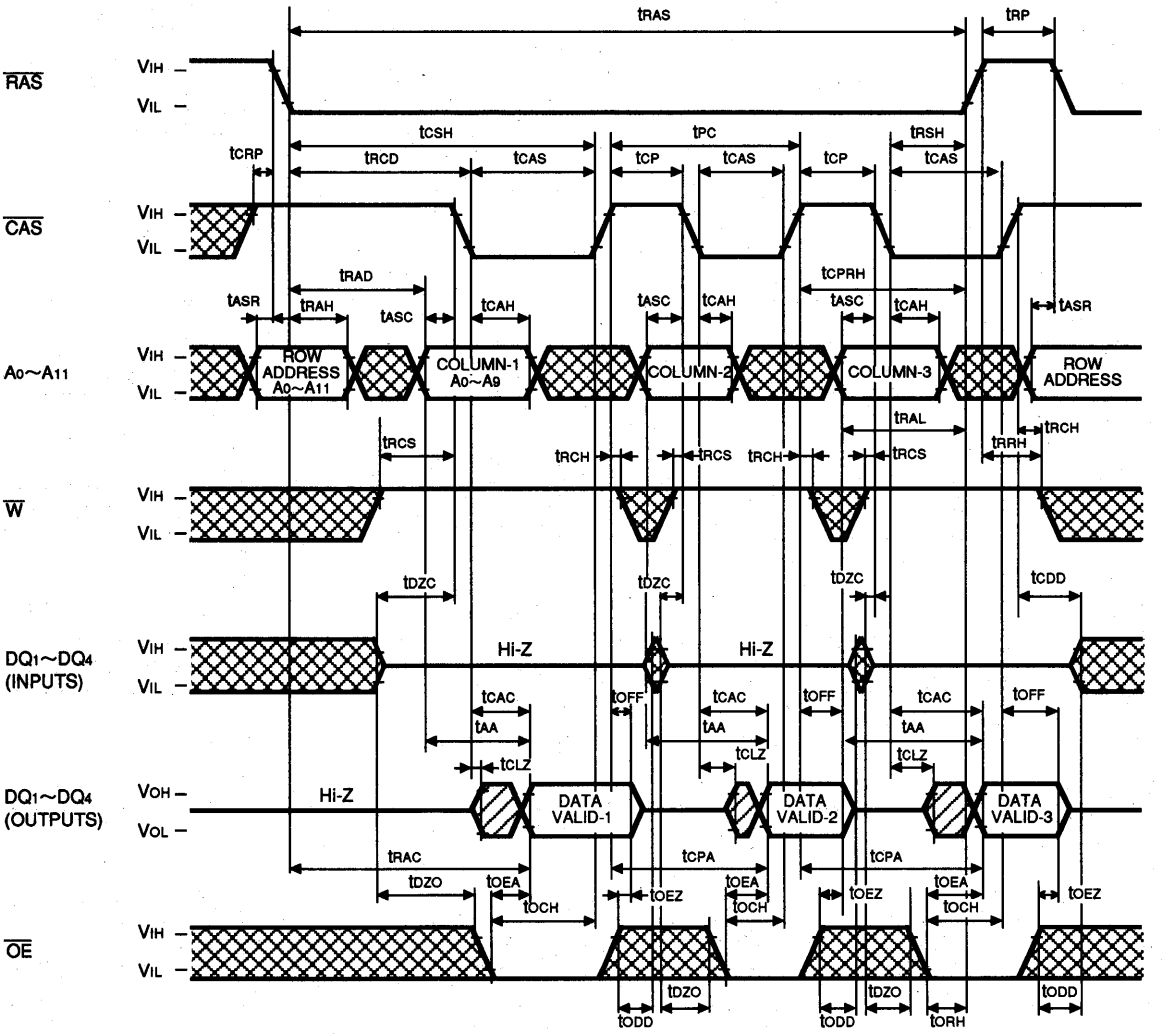


Hidden Refresh Cycle (Read) (Note 28)

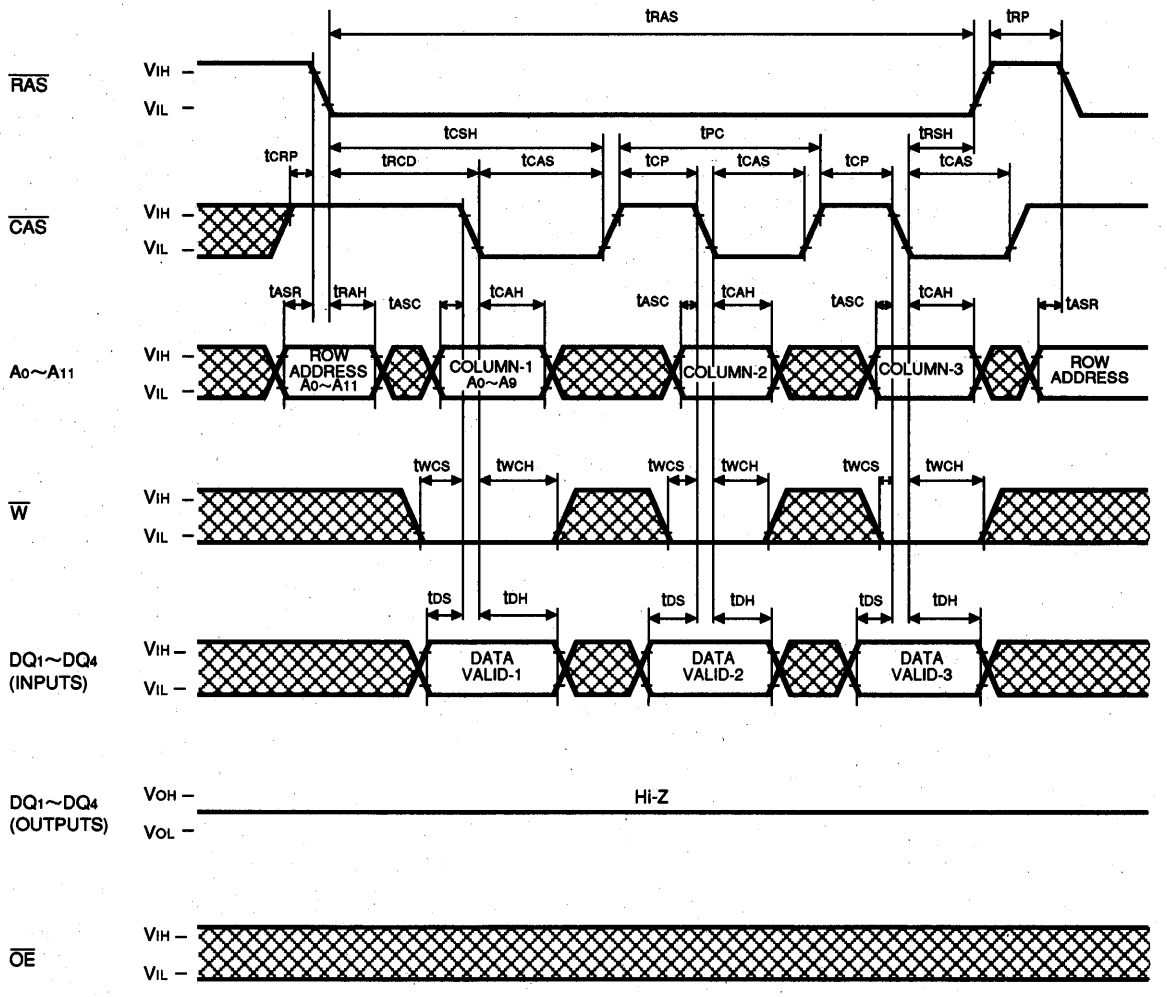


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

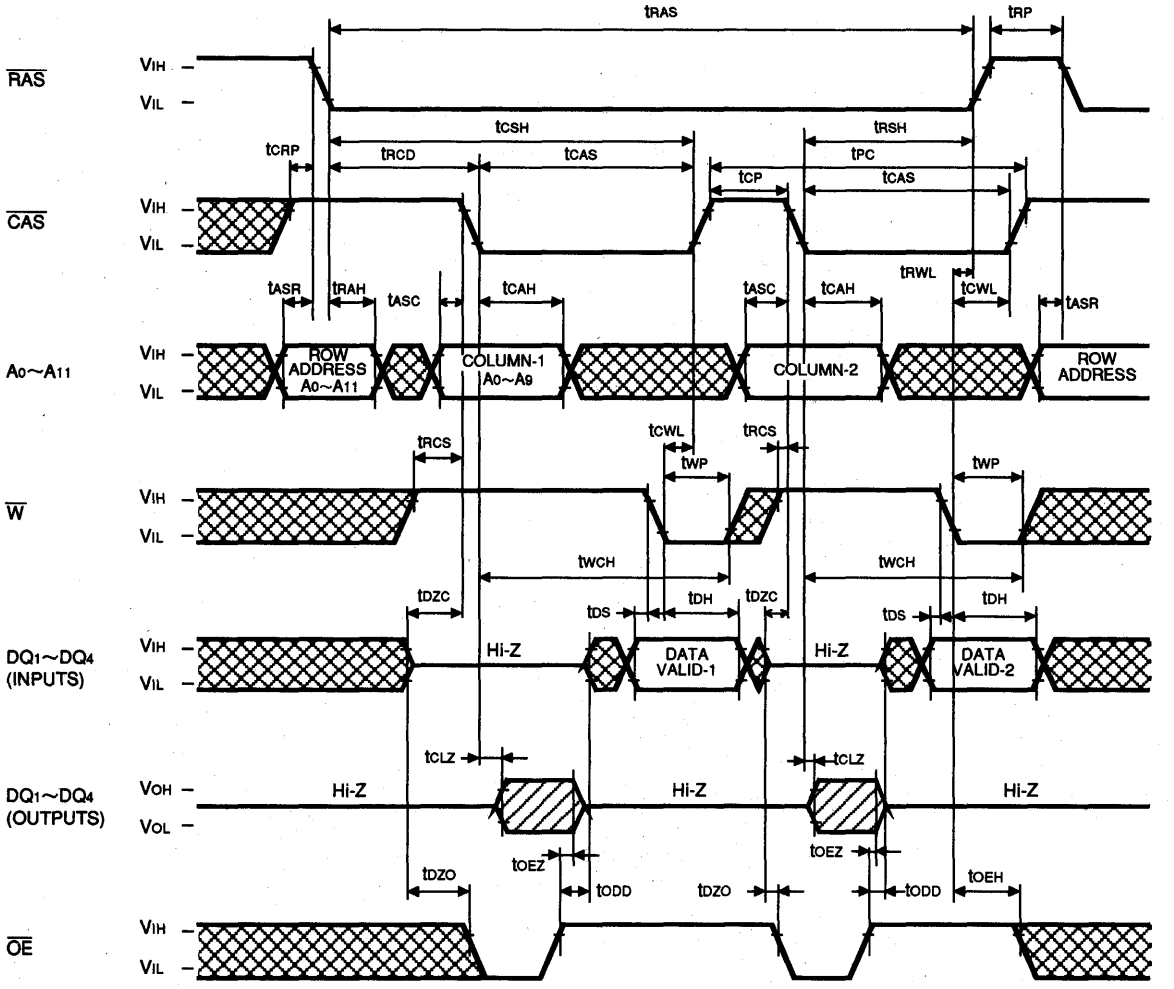
Fast Page Mode Read Cycle



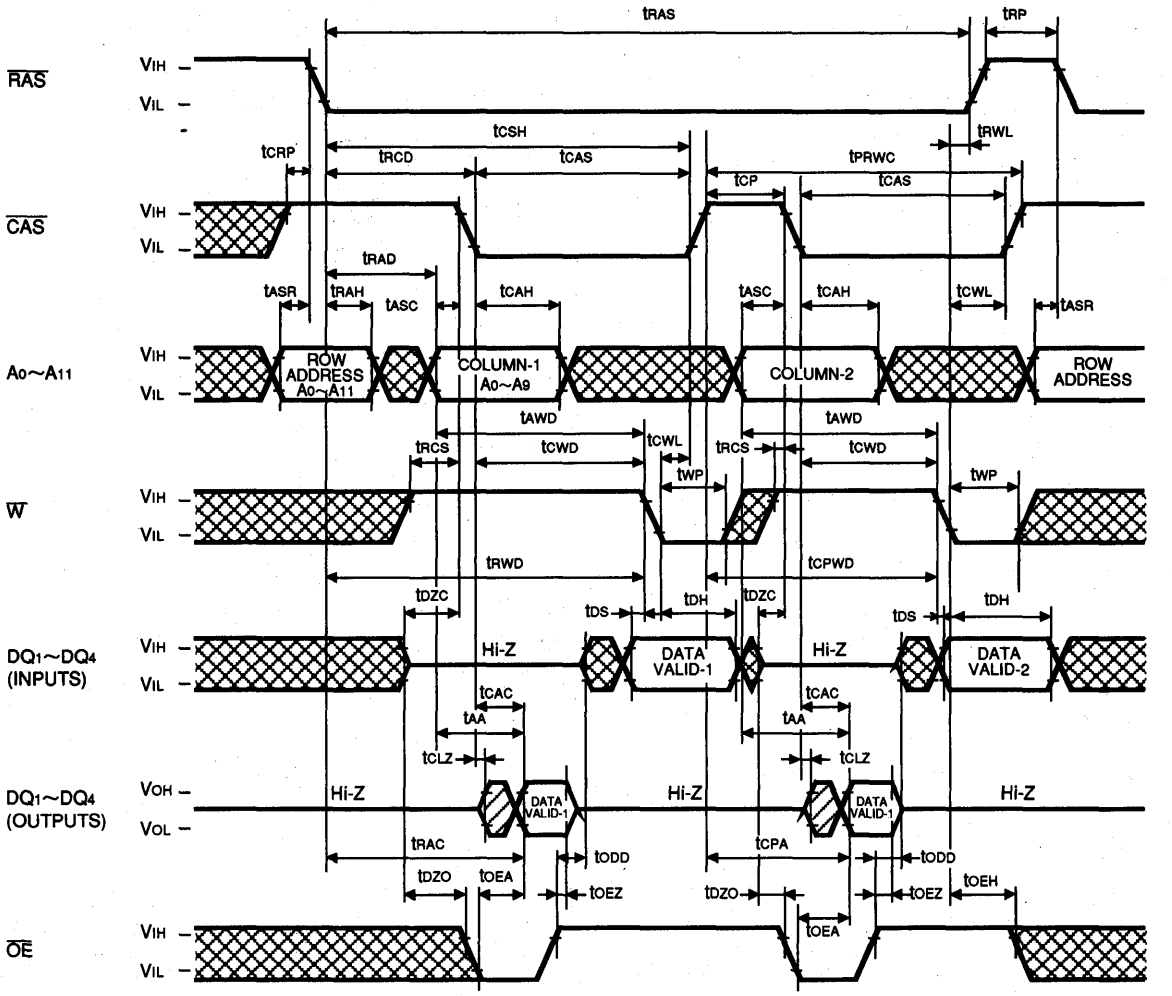
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



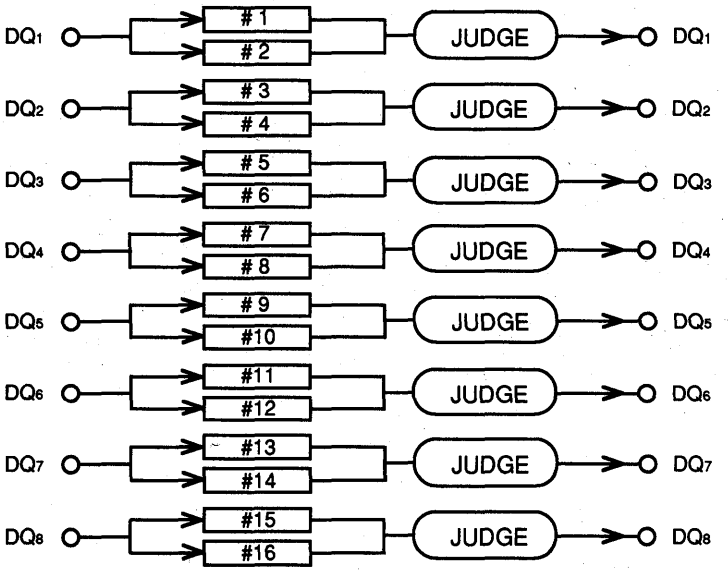
Fast Page Mode Read-Write, Read-Modify-Write Cycle



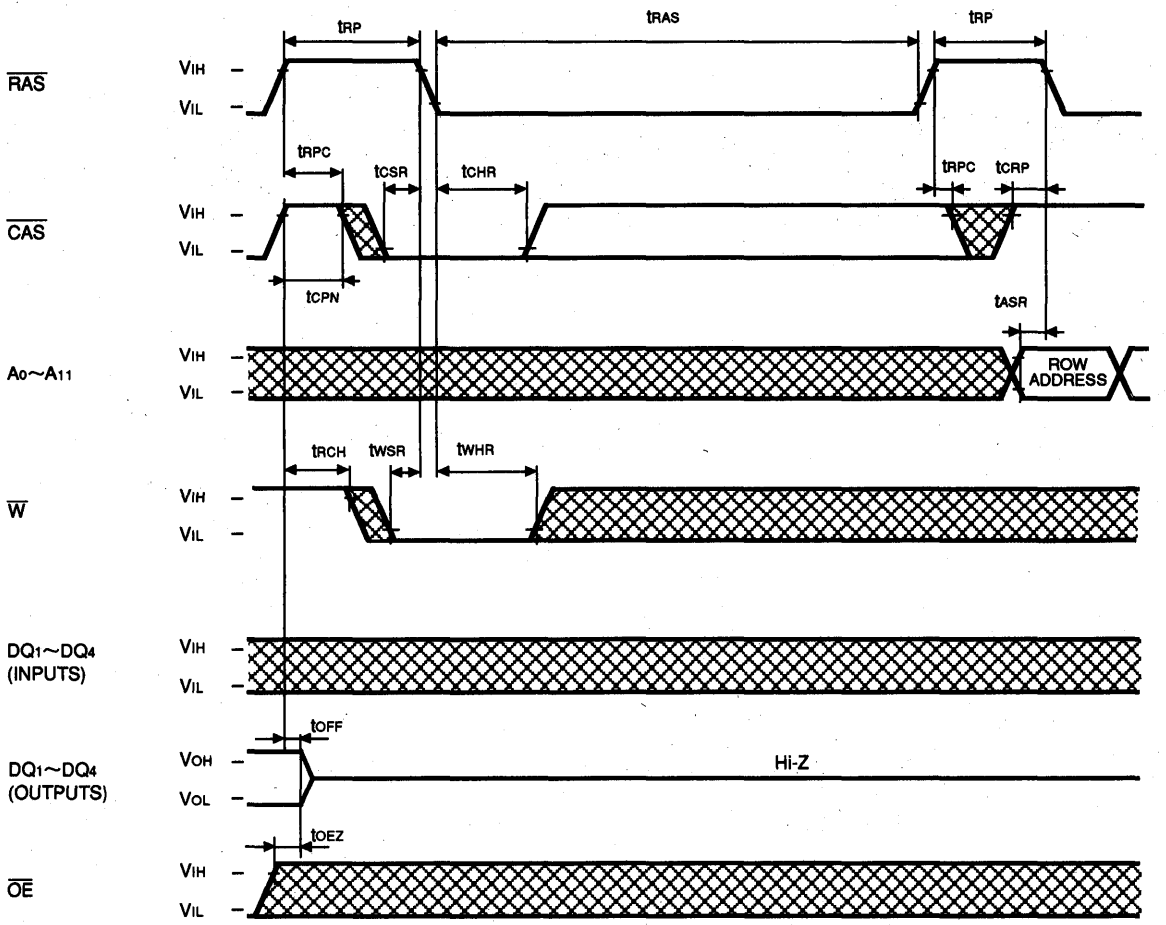
TEST Mode SET Cycle

Symbol	Parameter	Limits				Unit
		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 29 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.



TEST Mode SET Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC9\ (AV)}$	Average supply current from Vcc Self-Refresh cycle	M5M417800A (S)	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V			400	μA

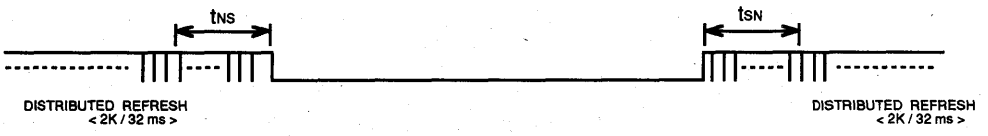
TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits				Unit
		M5M417800A-6S		M5M417800A-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

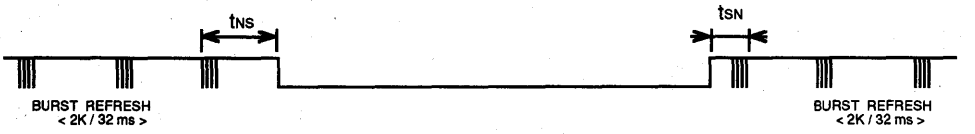
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} ≤ 32 ms and t_{SN} ≤ 32 ms.

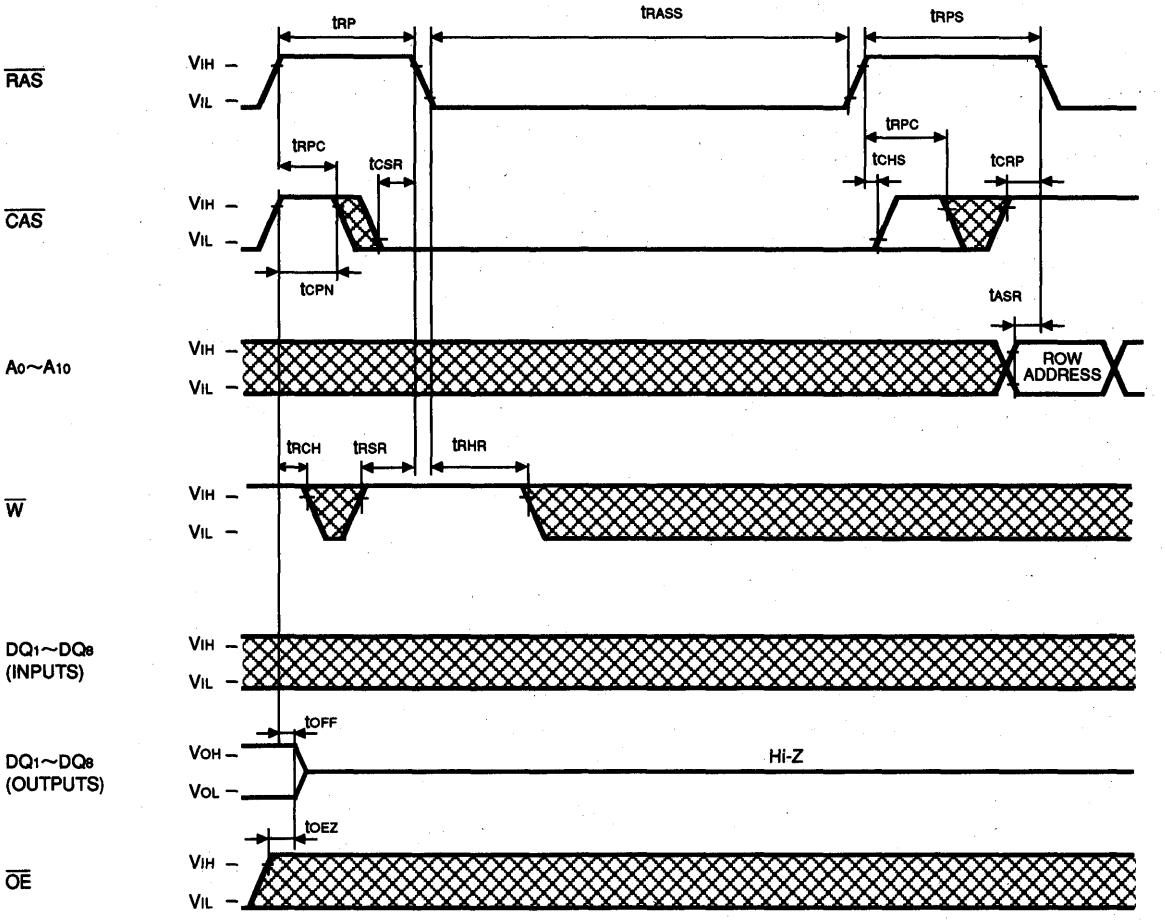


(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} + t_{SN} ≤ 32 ms.



Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417800CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800CXX-5,-5S	50	13	25	13	90	655
M5M417800CXX-6,-6S	60	15	30	15	110	540
M5M417800CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

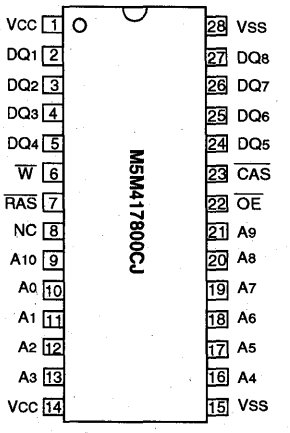
- Standard 28pin SOJ, 28pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 2.2mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M417800Cxx-5,-5S ----------800.0mW (Max)
  - M5M417800Cxx-6,-6S ----------660.0mW (Max)
  - M5M417800Cxx-7,-7S ----------580.0mW (Max)
- Self refresh capability *
  - Self refresh current ----------200.0 μA(Max)
- Fast-page mode, Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

  * Applicable to self refresh version (M5M417800CJ,TP-5S,-6S,-7S :option) only

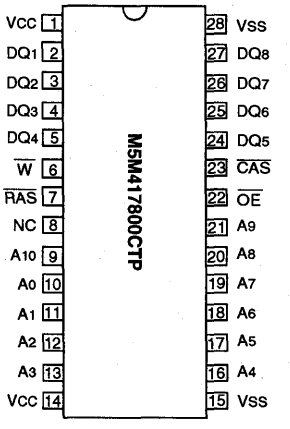
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417800CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

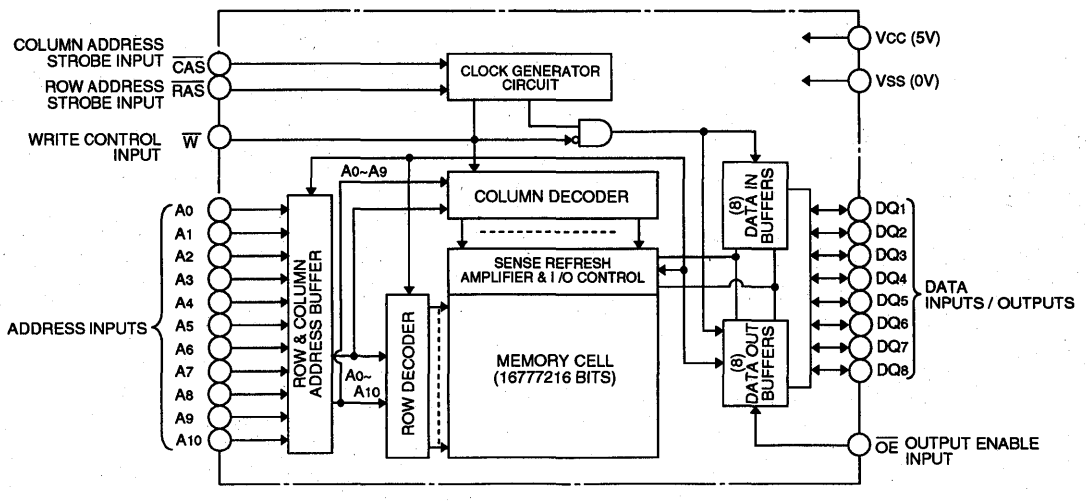
The M5M417800CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417800CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
**: V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to VSS.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦5.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M417800C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc-0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M417800C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M417800C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M417800C-6,-6S				70	
		M5M417800C-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417800C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/output capacitance, data ports				8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.

6:Measured with a load circuit equivalent to 2TTL loads and 100pF.

7:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max).

8:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9:Assumes that tRAD≧tRAD(max) and tASC≦tASC(max).

10:Assumes that tCP≦tCP(max) and tASC≧tASC(max).

11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦|±10 μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.

13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).

15:tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

16:tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

17:Either tDZC or tDZO must be satisfied.

18:Either tCDD or tODD must be satisfied.

19:tT is measured between VIH(min) and VIL(max).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{RCS}	Read setup time after $\overline{CAS}$ high		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		8		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
t_{WP}	Write pulse width		8		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 21)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 22)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 25)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	M5M417800C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}$ & $\overline{WE} \leqq 0.2V$ or $\overline{OE}$ & $\overline{WE} \geqq Vcc-0.2V$ $A_0 \sim A_{11} \leqq 0.2V$ or $A_0 \sim A_{11} \geqq Vcc-0.2V$ t_{REF}=128ms (2048cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M417800C (S)	$\overline{RAS} = \overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

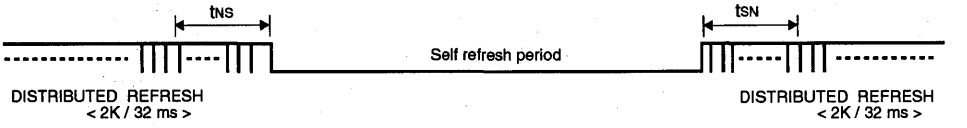
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M417800C-5S		M5M417800C-6S		M5M417800C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

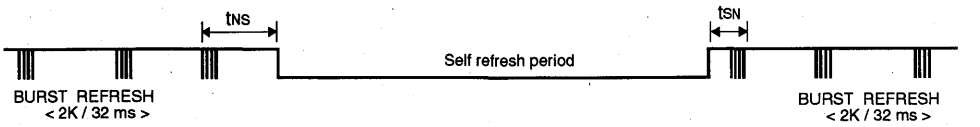
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 32$ms and $t_{SN} \leqq 32$ms.



(2) In case of burst refresh

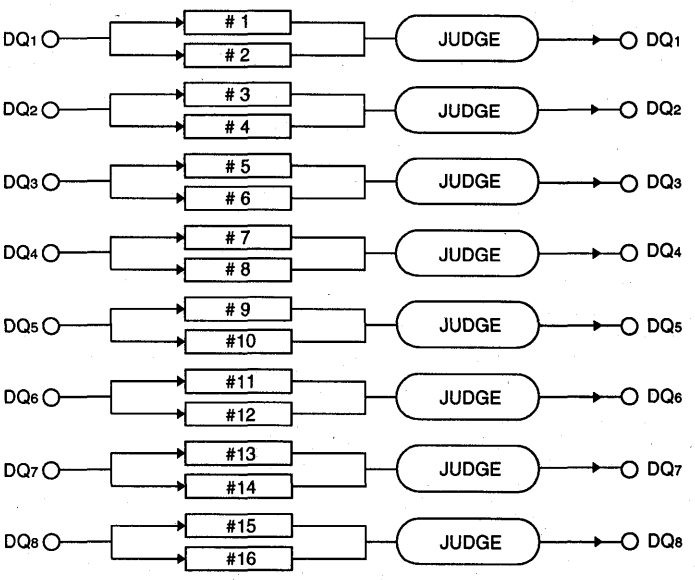
The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 32$ms.



TEST Mode SET Cycle

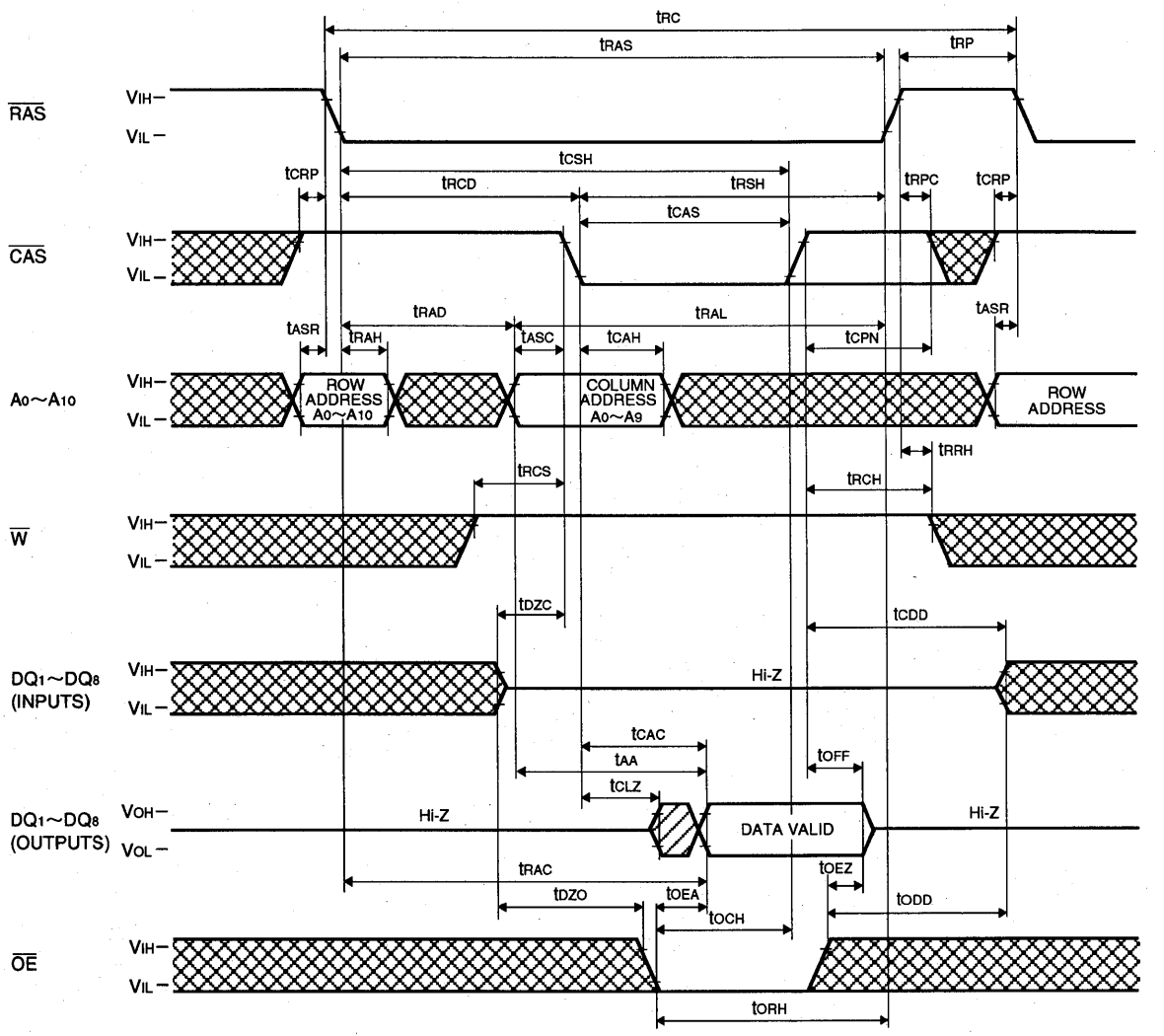
Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



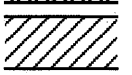
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 28)
Read Cycle



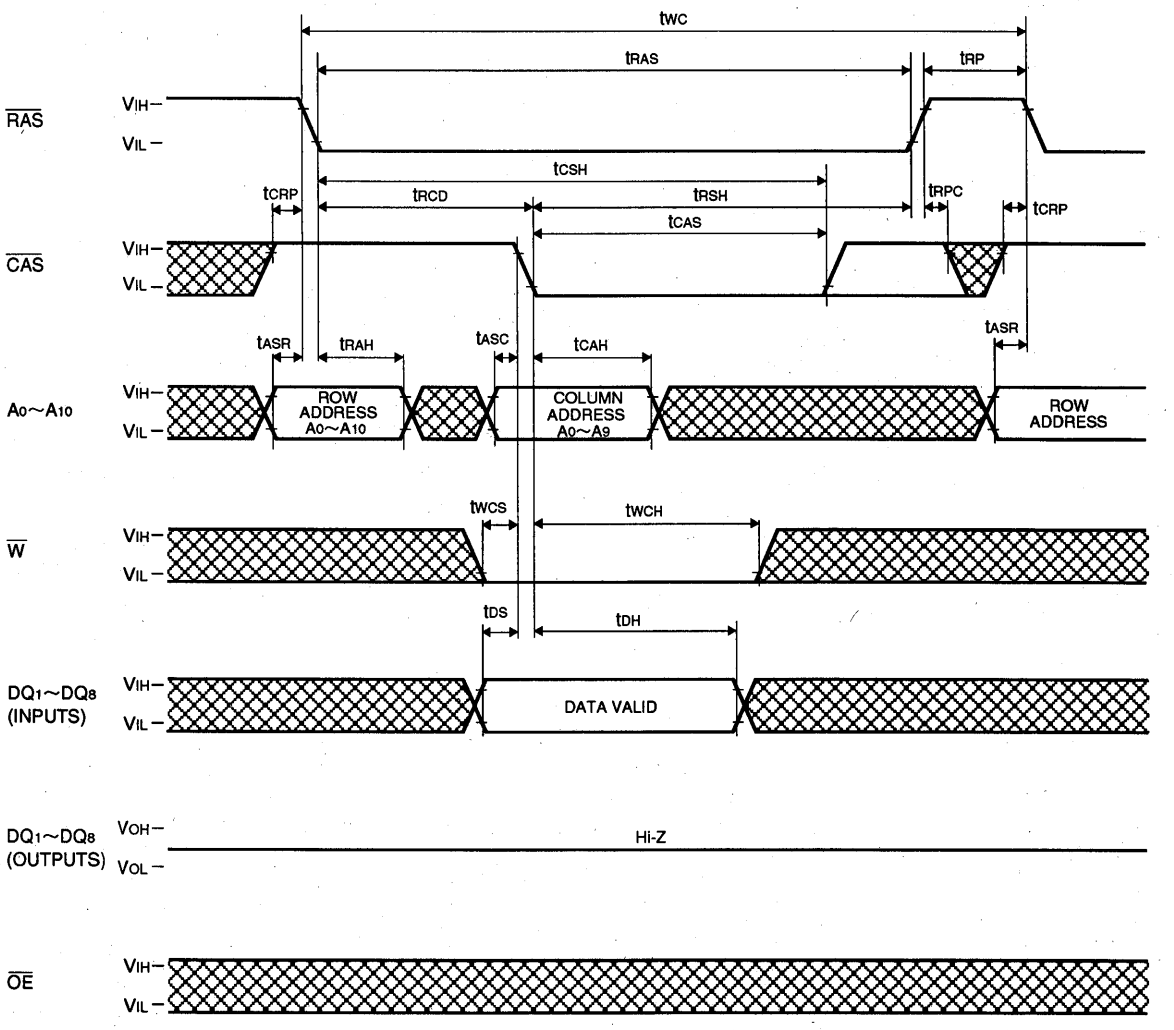
Note 28

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

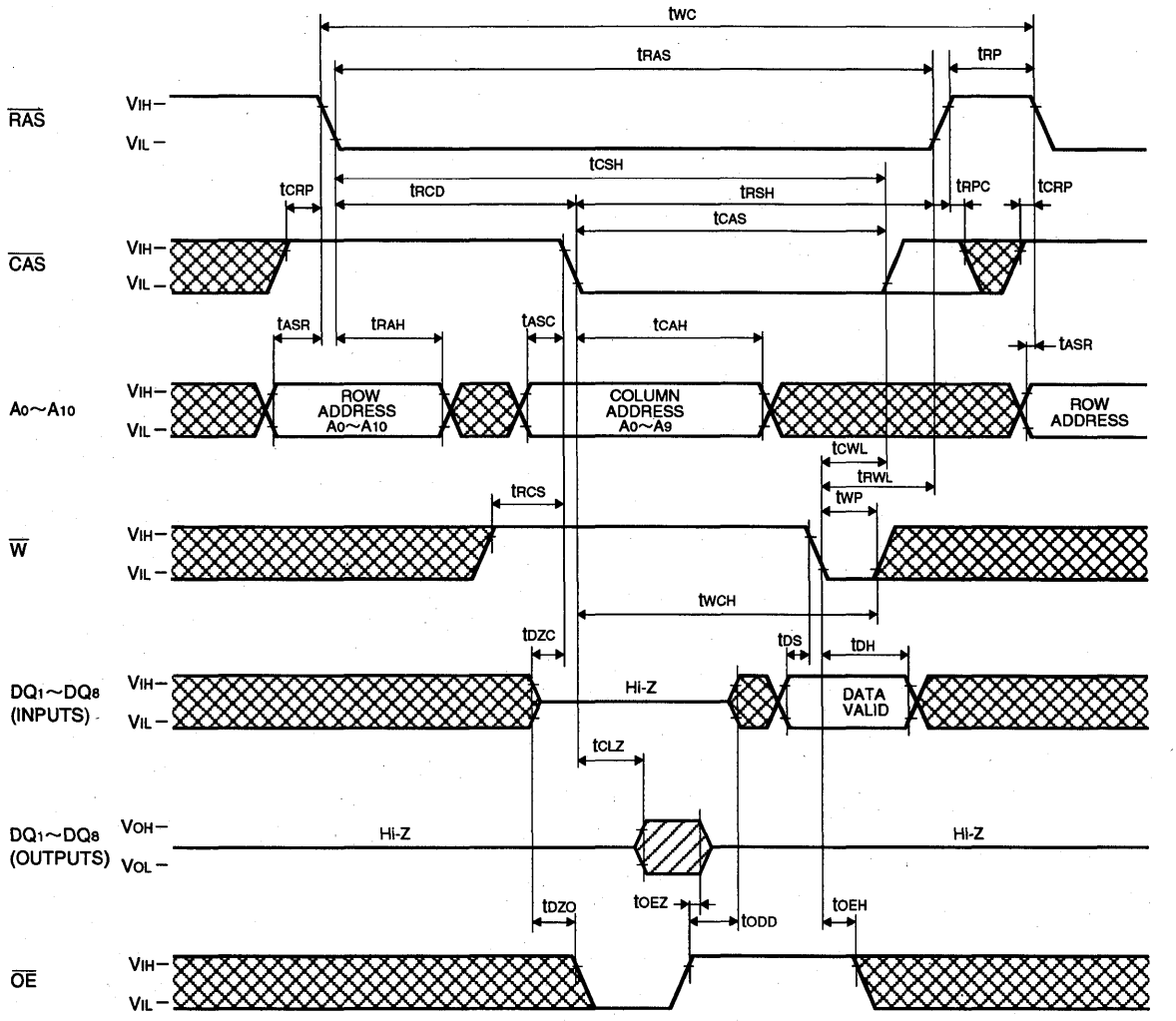


Indicates the invalid output.

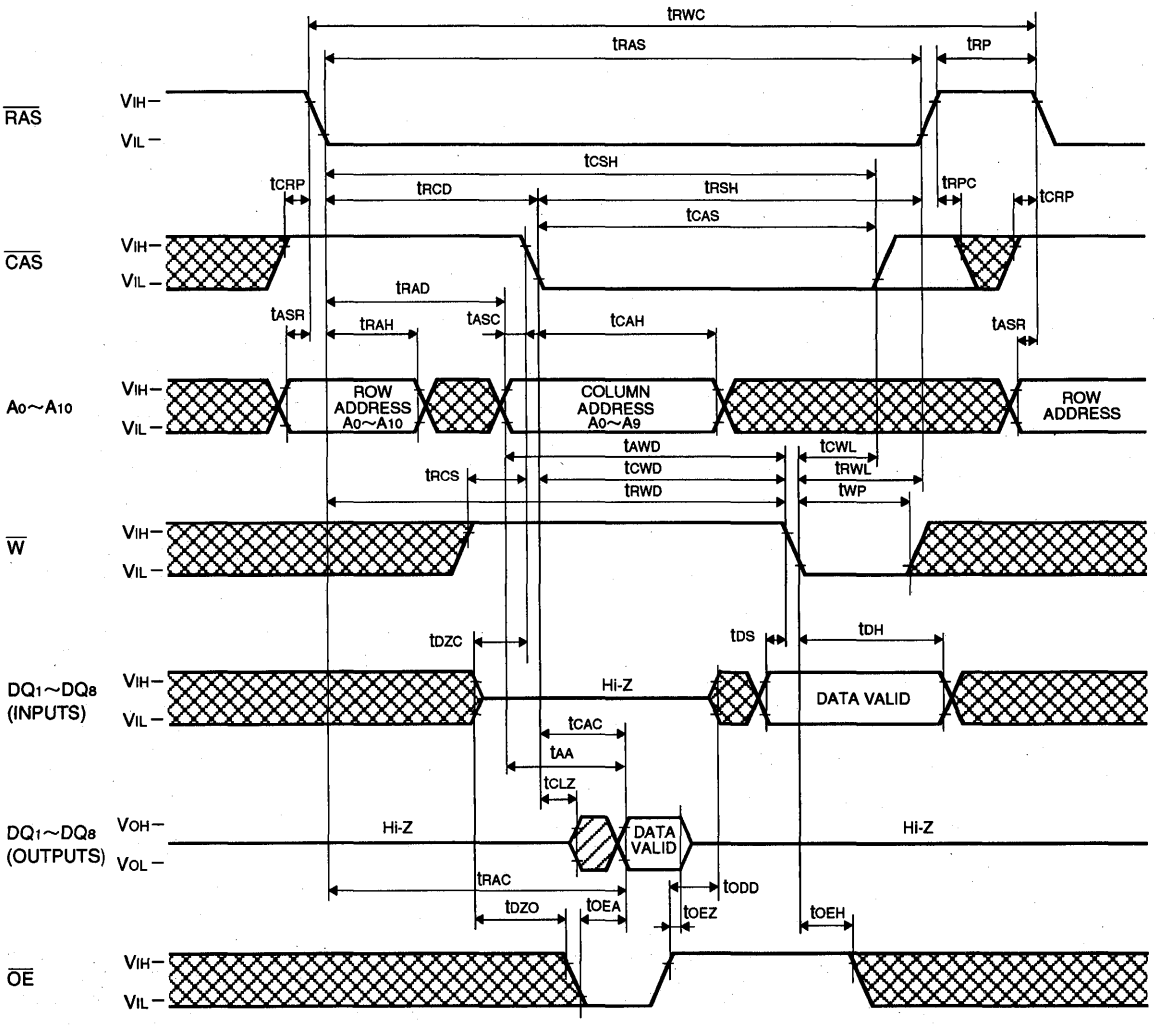
Write Cycle (Early write)



Write Cycle (Delayed write)

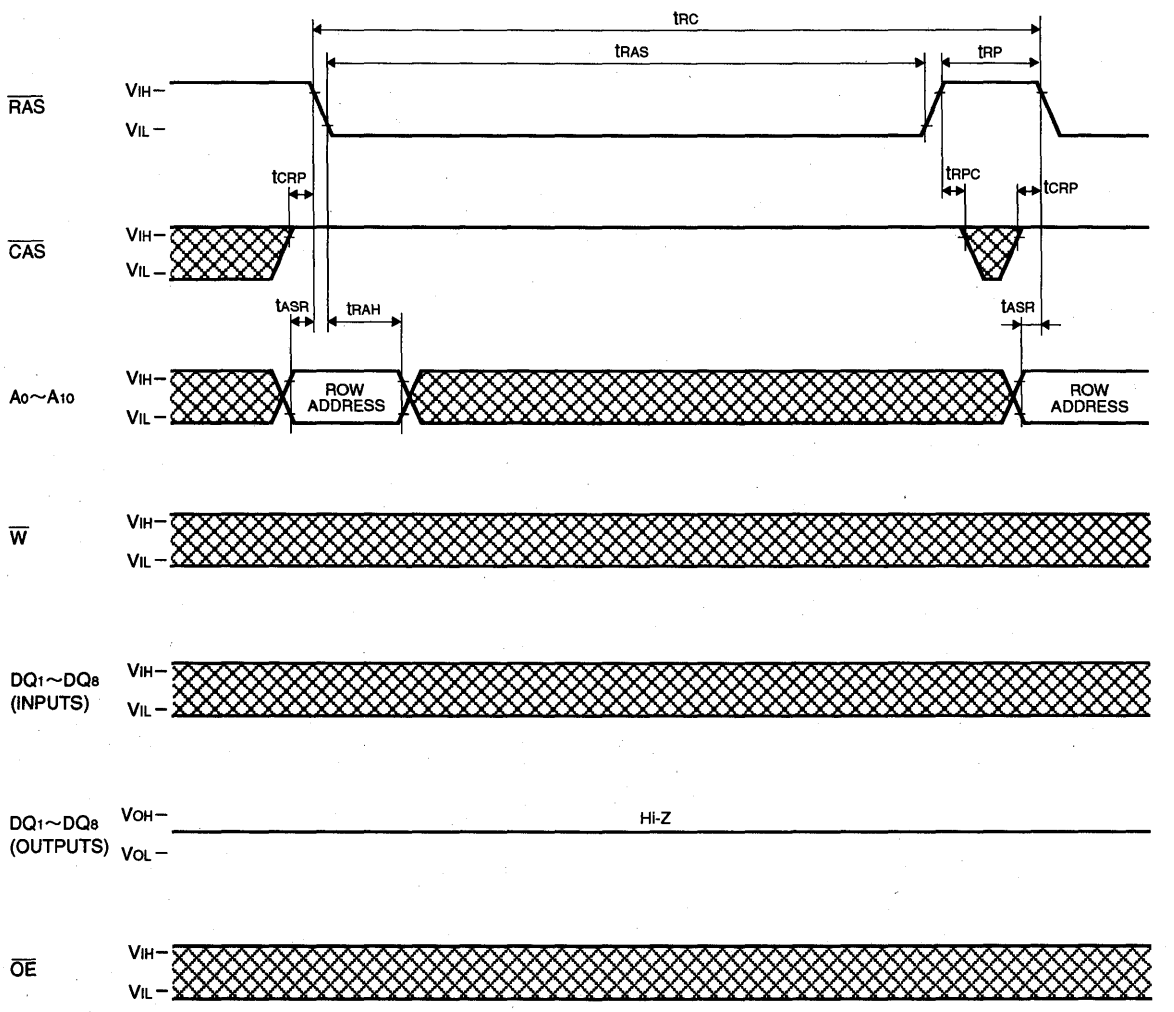


Read-Write, Read-Modify-Write Cycle

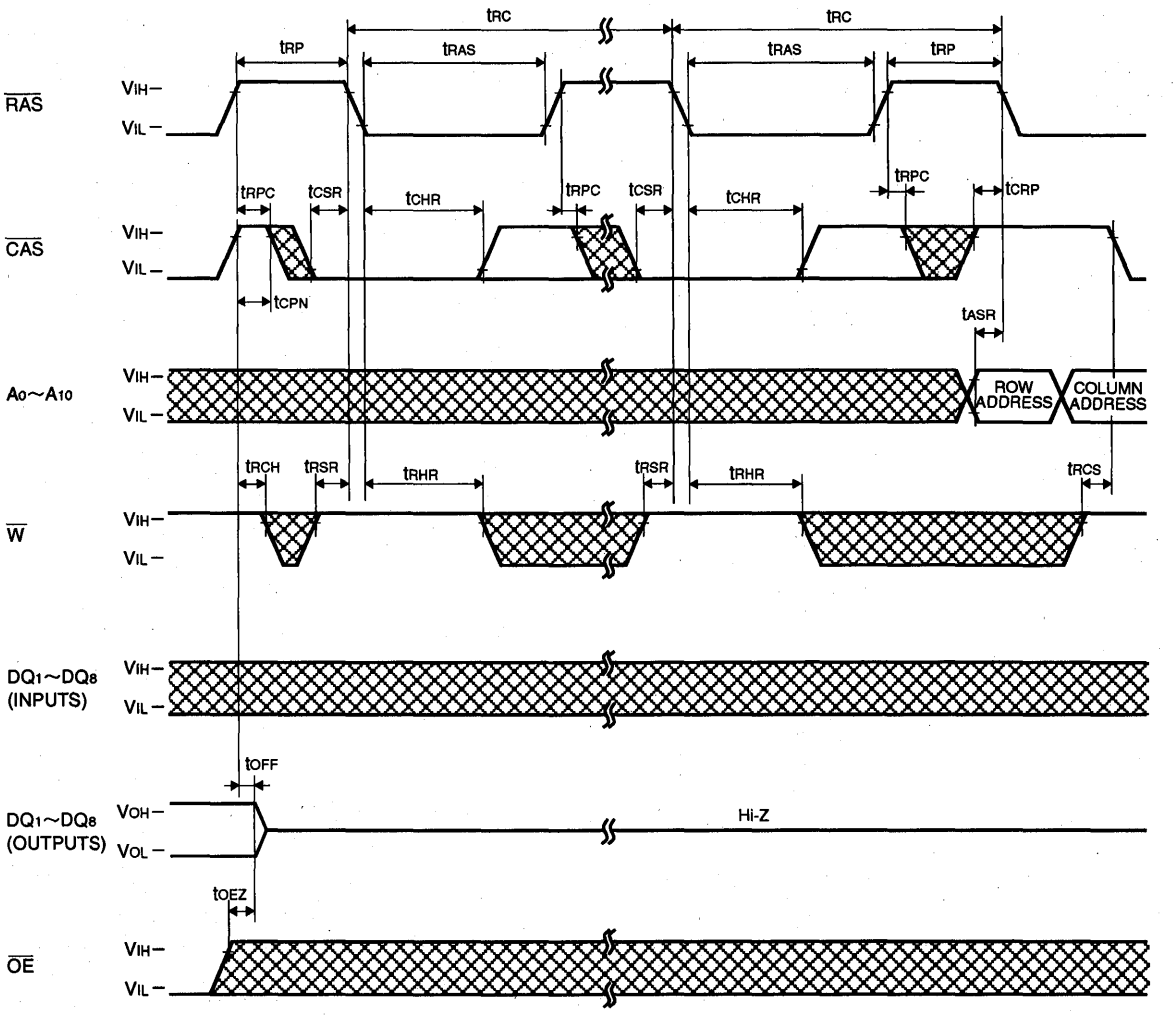


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle

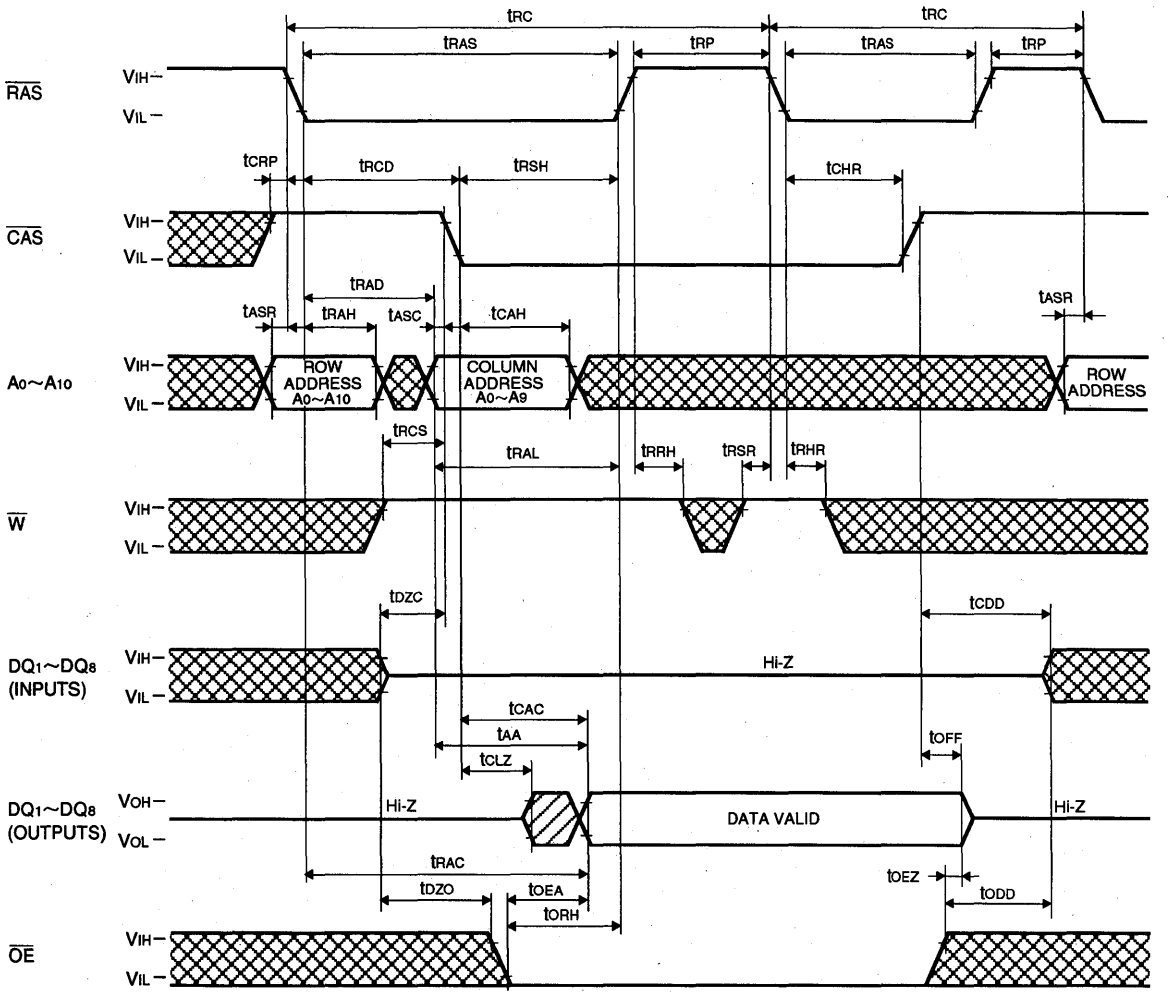


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

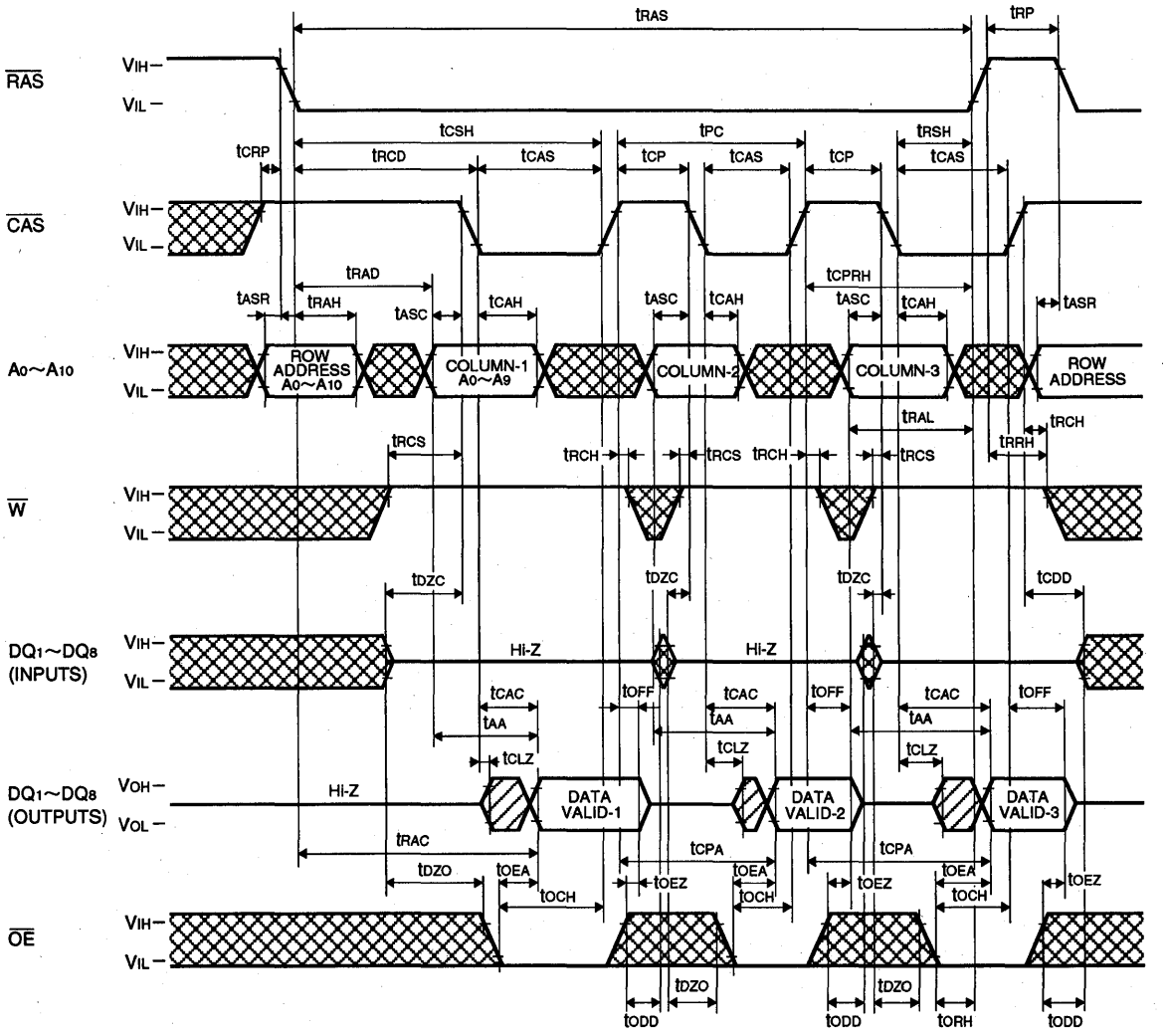
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

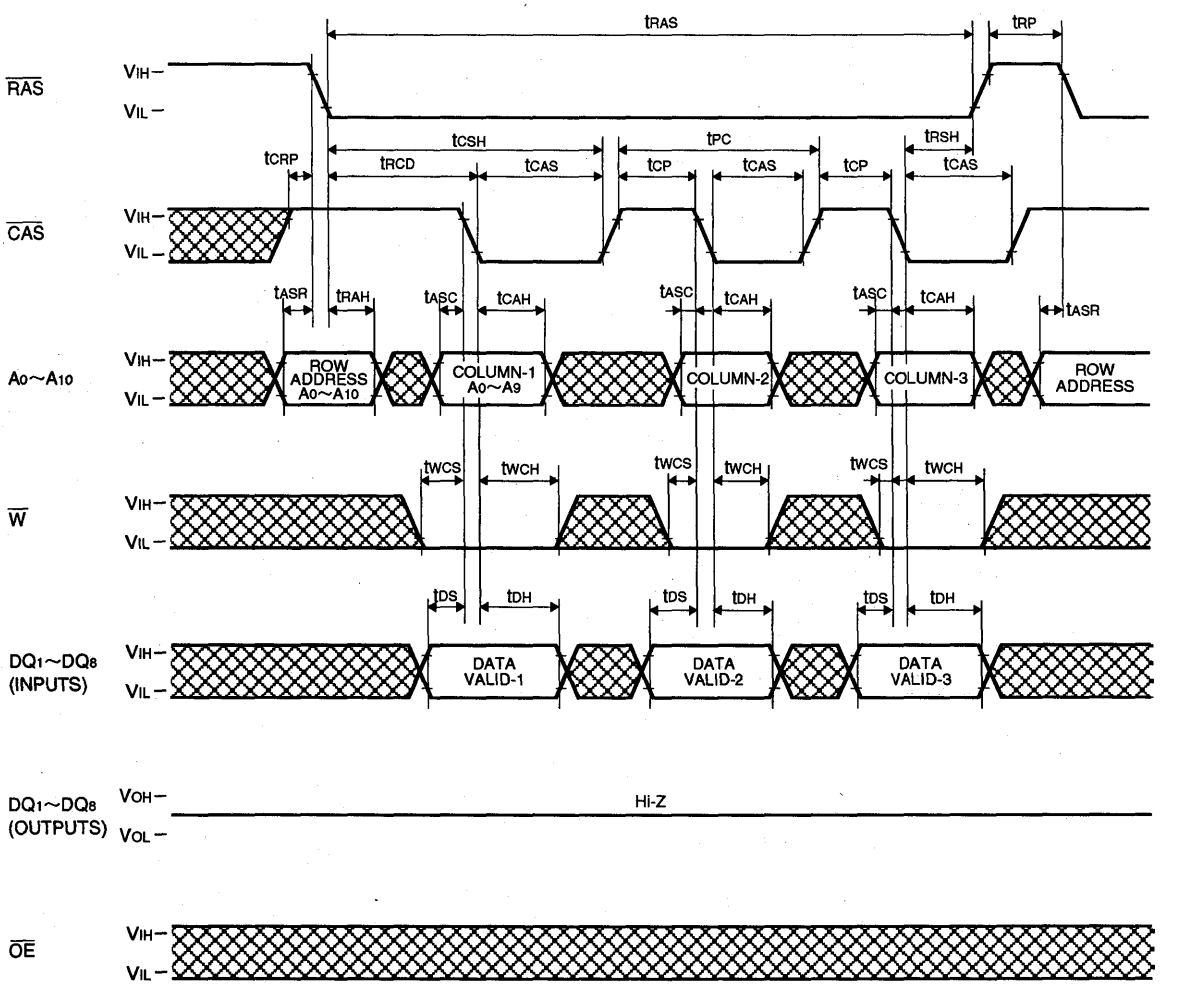
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle

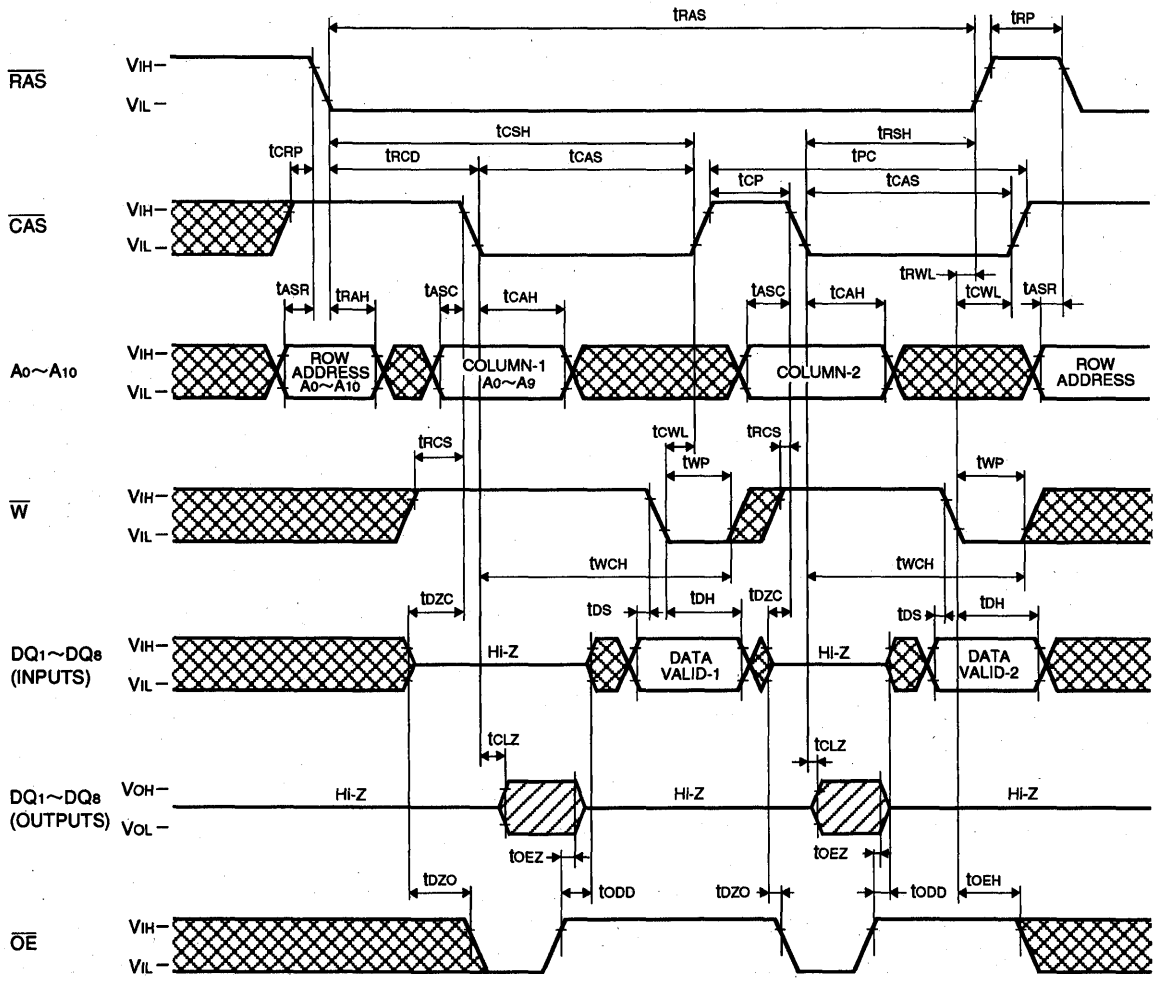


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

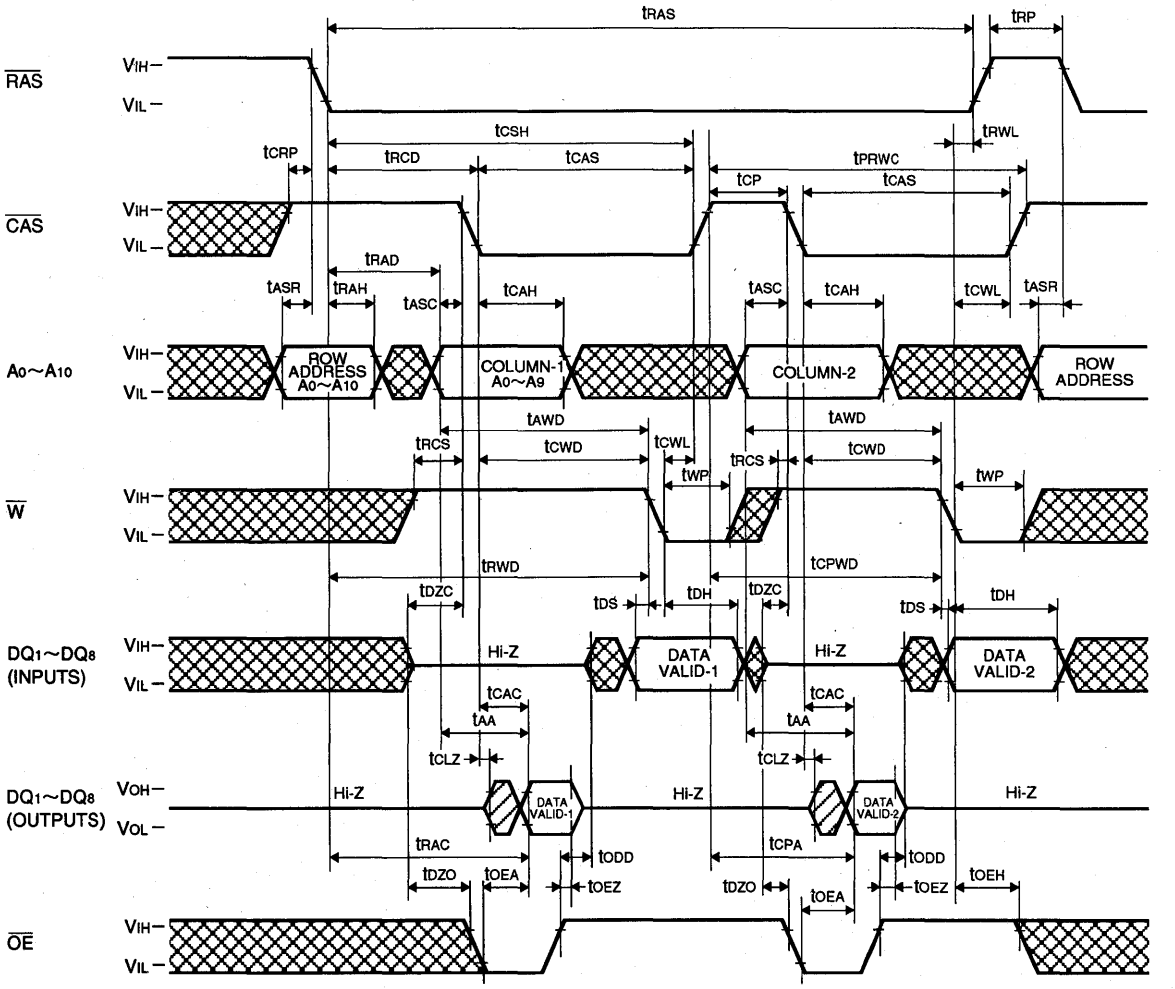
Fast Page Mode Write Cycle (Early Write)



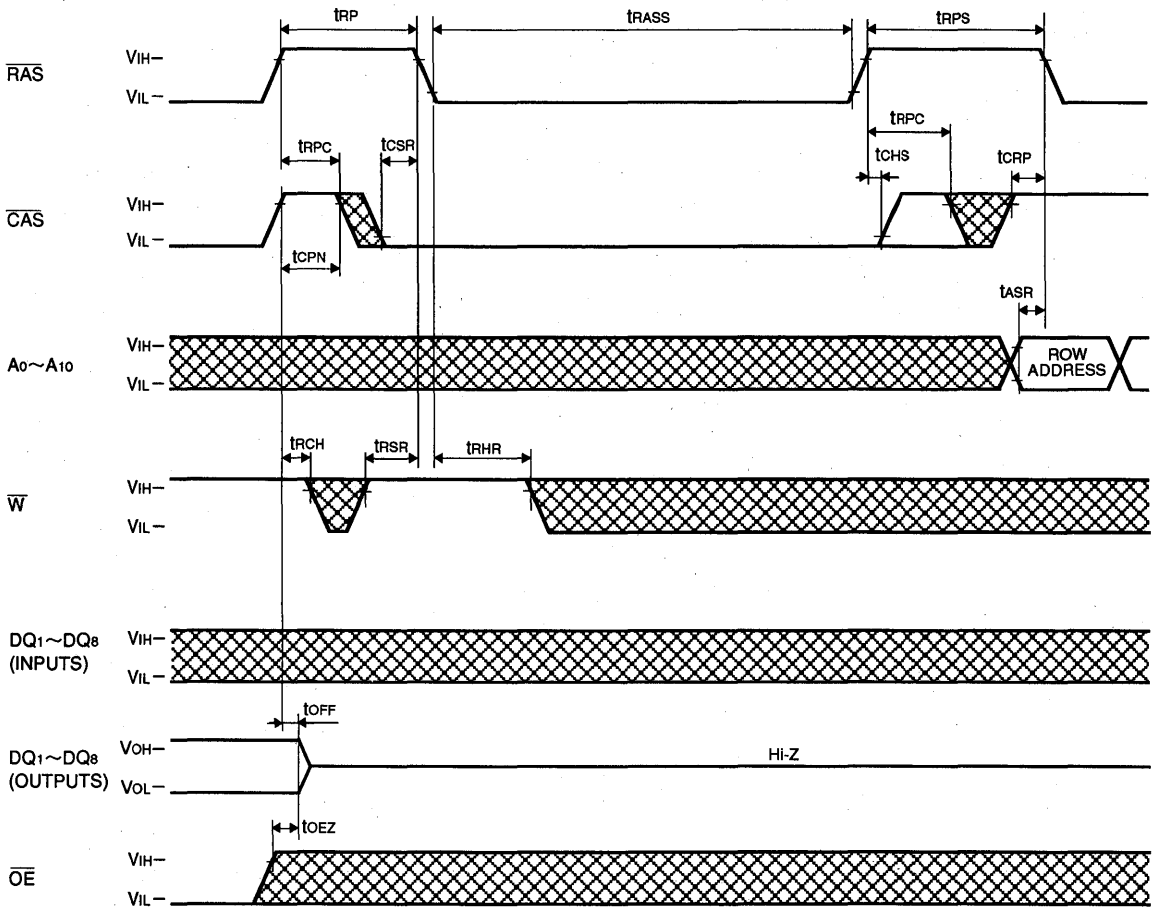
Fast-Page Mode Write Cycle (Delayed Write)



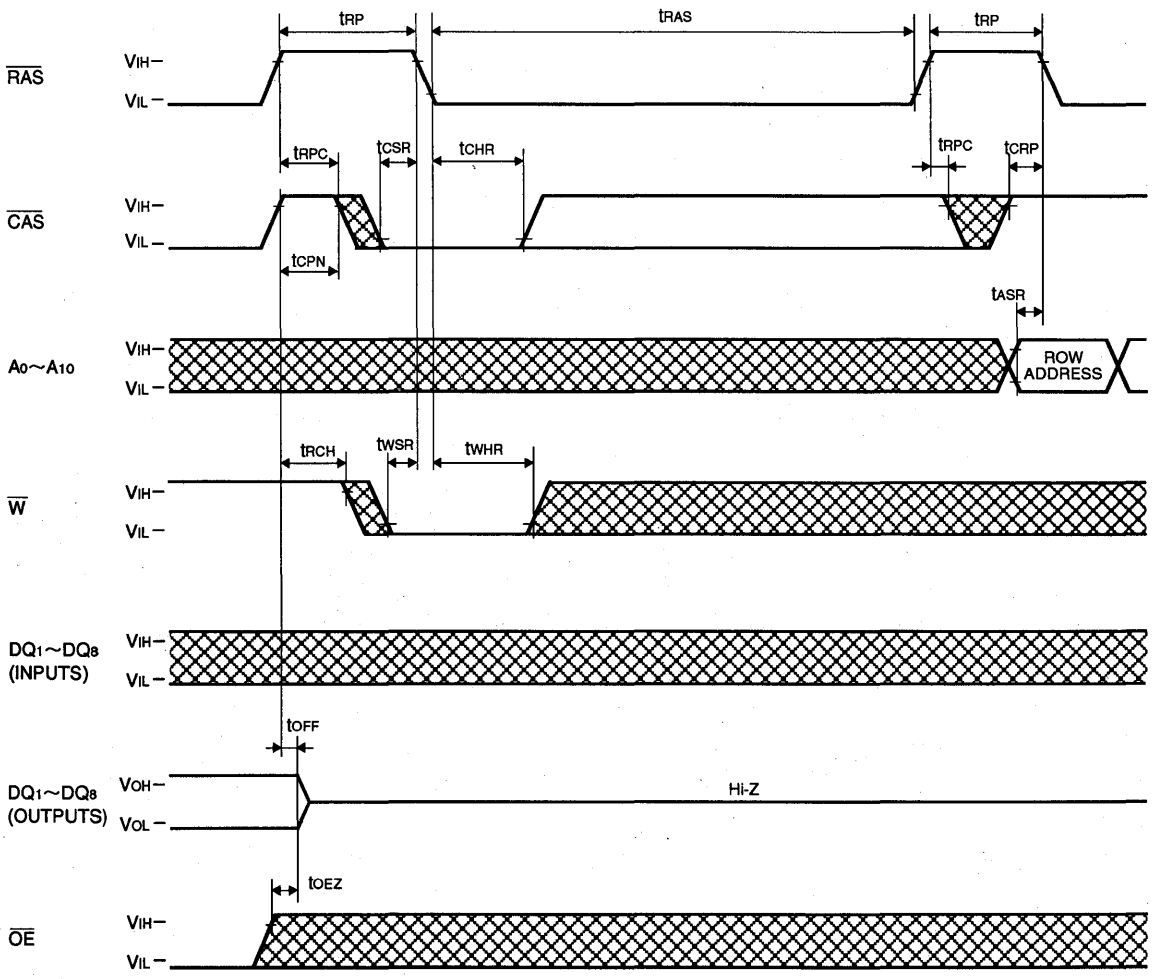
Fast Page Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M417805CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs with Hyper page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417805CXX-5,-5S	50	13	25	13	90	655
M5M417805CXX-6,-6S	60	15	30	15	110	540
M5M417805CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 28 pin SOJ,28 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ····· CMOS Input level
  - 1.1mW (Max)* ····· CMOS Input level
- Operating power dissipation
  - M5M417805CXX-5,-5S ····· 800mW (Max)
  - M5M417805CXX-6,-6S ····· 660mW (Max)
  - M5M417805CXX-7,-7S ····· 580mW (Max)
- Self refresh capability*
  - Self refresh current ····· 200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})
- *: Applicable to self refresh version (M5M417805CJ,TP-5S,-6S, -7S :option) only

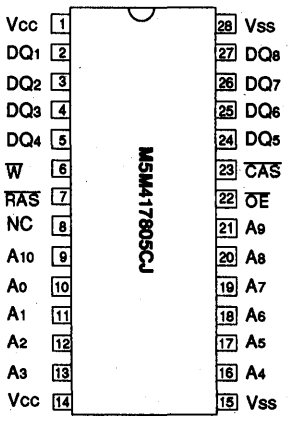
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

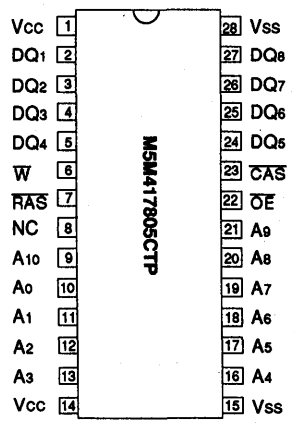
PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC: NO CONNECTION

MITSUBISHI ELECTRIC

FUNCTION

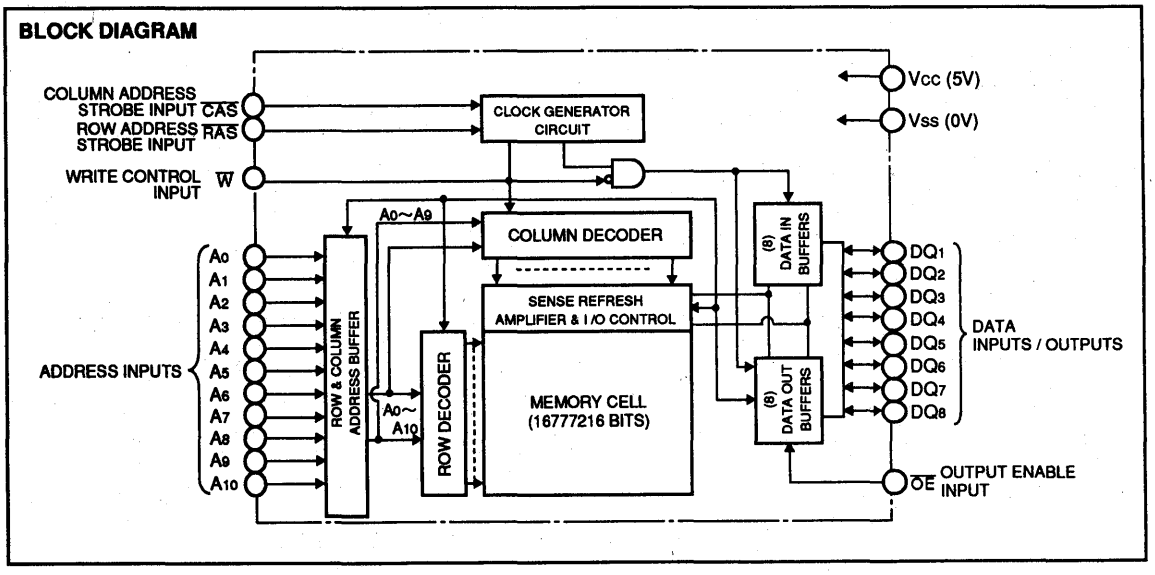
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M417805CJ, TP provides a number of other functions,e.g., $\overline{RAS}$-only refresh,and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	−1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : $V_{IL(min)}$ is −2.0V when undershoot width is less than 25ns.(Undershoot width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ +6.5V, Other inputs pins=0V	−10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M417805C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc−0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from Vcc,$\overline{RAS}$ only refresh mode (Note 3,5)	M5M417805C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	
I_{CC4} (AV)	Average supply current from Vcc Hyper Page Mode (Note 3,4,5)	M5M417805C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M417805C-6,-6S				115	
		M5M417805C-7,-7S				90	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M417805C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) ,I_{CC4} (AV) , and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0~70℃ , Vcc = 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHZ			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0~70℃ , Vcc = 5V±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods(greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH (min) or lower than VIL (max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD ≧tRCD(max) and tASC ≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP ≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max) ,tWEZ(max) ,tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (IOUT≦ | ±10μA |) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted, See notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note20)	13		15		20		ns
tT	Transition time	(Note21)	1	50	1	50	1	50	ns

Note 14:The timing requirements are assumed tT =2ns.
15:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17:tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18:tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
19:Either tDZC or tDZO must be satisfied.
20:Either tRDD or tCDD or tODD must be satisfied.
21:tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD(min) and tCPWD ≧tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: t_{HPC}(min) is specified in the case of read-only and early write-only in Hyper Page Mode.
27: t_{RAS}(min) is specified as two cycles of $\overline{CAS}$ input are performed.
28: t_{CP}(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow - Refresh cycle (note 6)	M5M417805C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}$ & $\overline{WE} \leqq 0.2V$ or $\overline{OE}$ & $\overline{WE} \geqq V_{CC}-0.2V$ $A_0 \sim A_{10} \leqq 0.2V$ or $A_0 \sim A_{10} \geqq V_{CC}-0.2V$ t_{REF}=128ms (2048 cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M417805C (S)	$\overline{RAS}$= $\overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

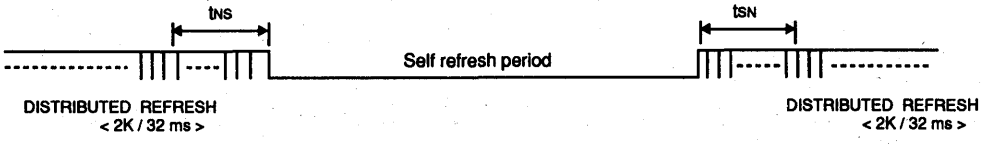
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417805C-5S		M5M417805C-6S		M5M417805C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

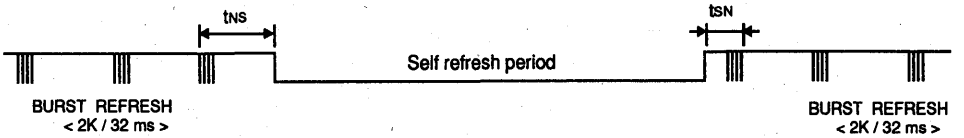
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 32$ms and $t_{SN} \leqq 32$ ms.



(2) In case of burst refresh

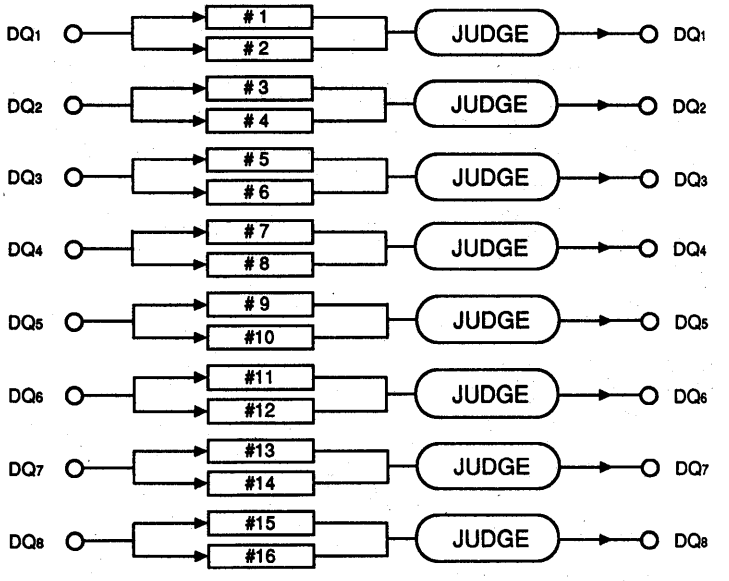
The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 32$ ms.



TEST Mode SET Cycle (Note 31)

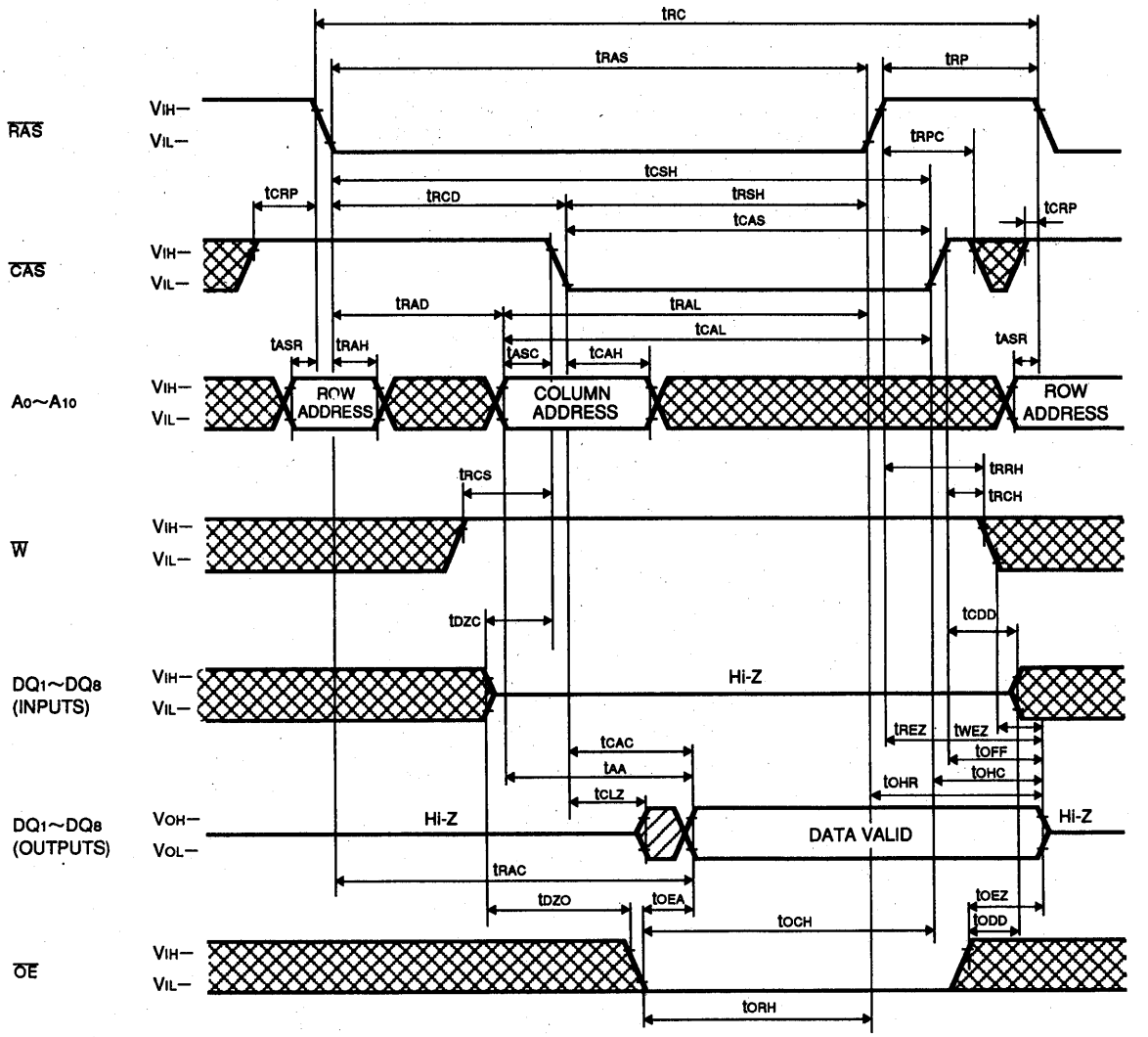
Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth) . No addressing of CA0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 32)

Read Cycle

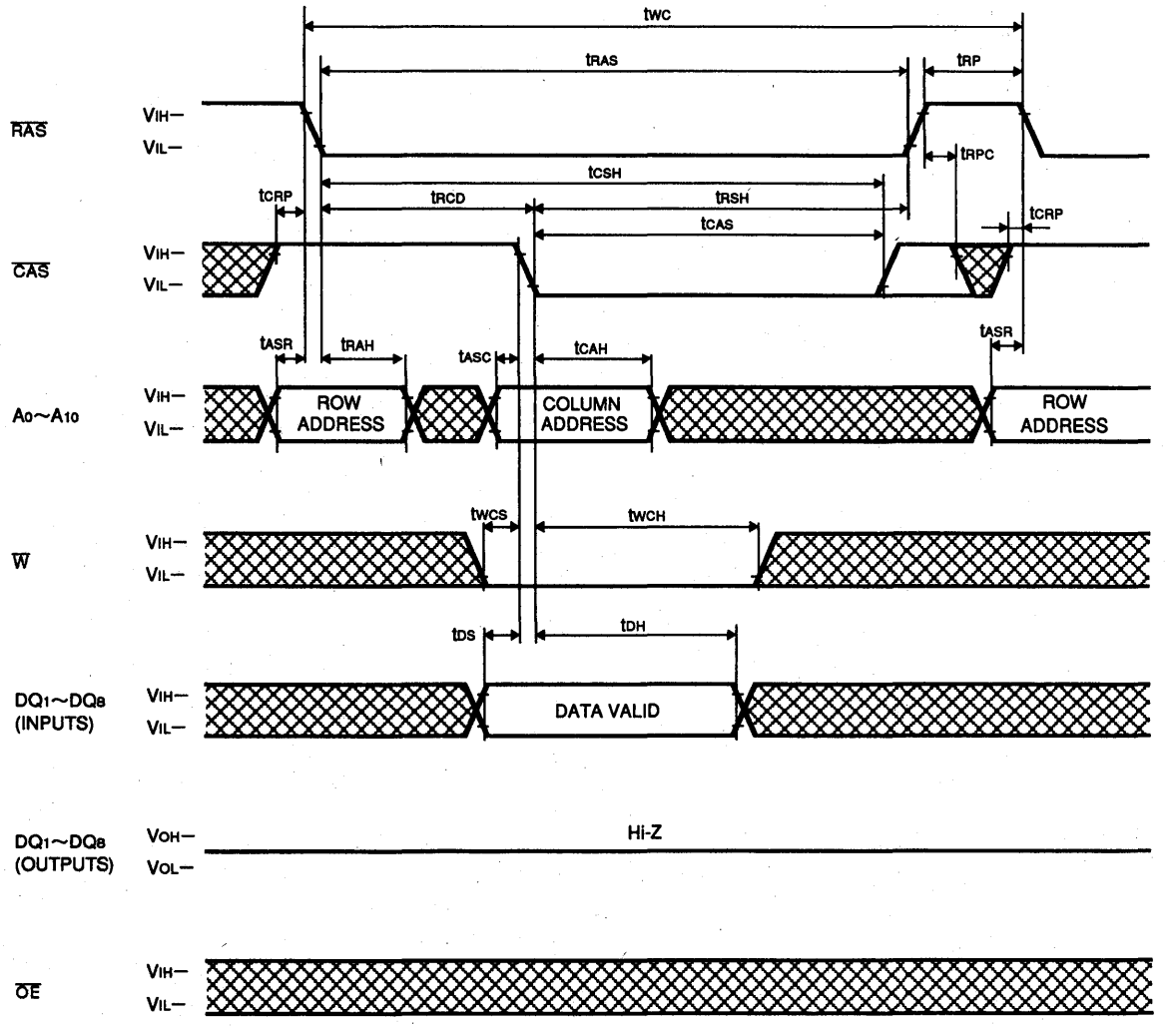


Note 32

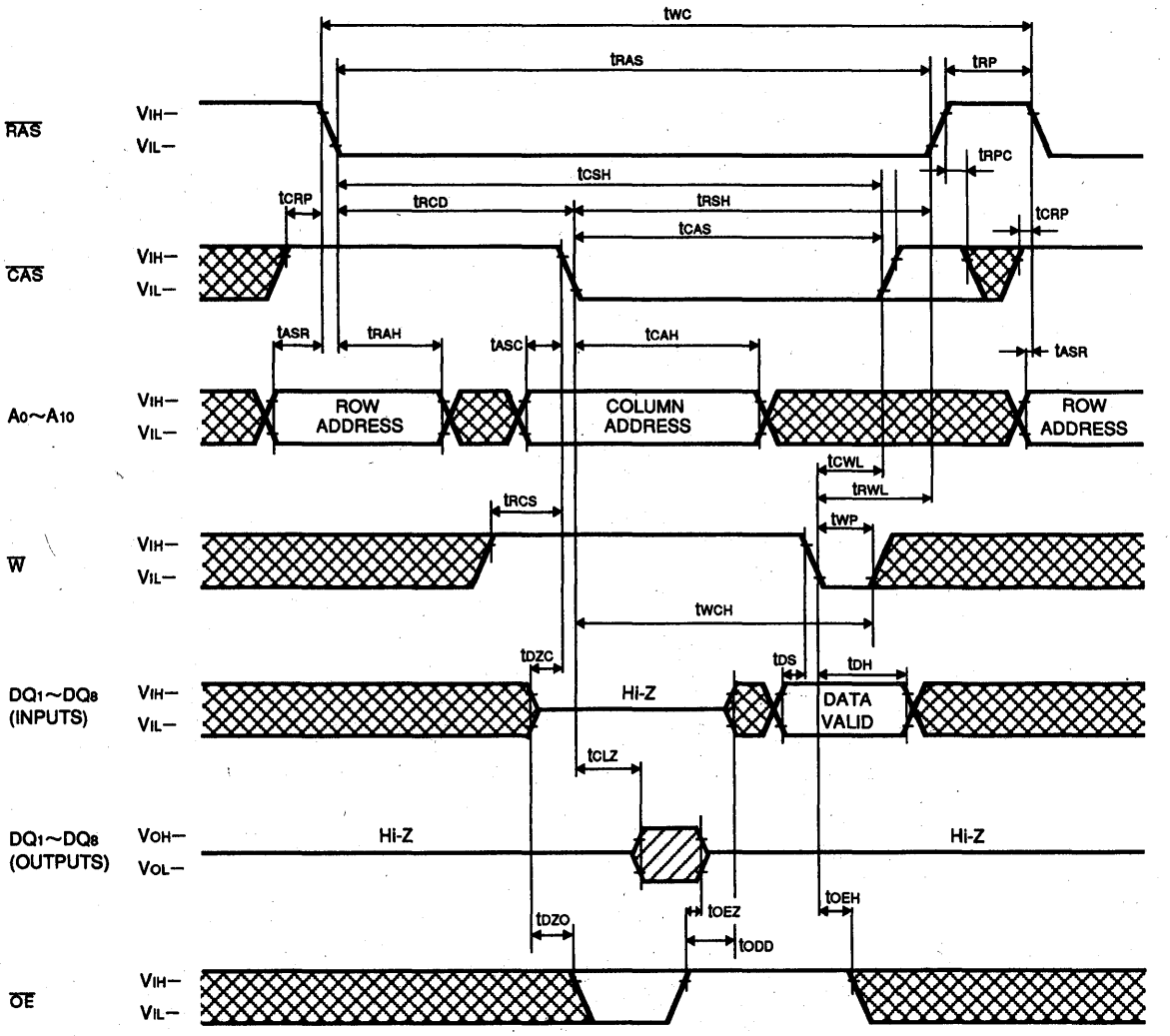
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

Early Write Cycle

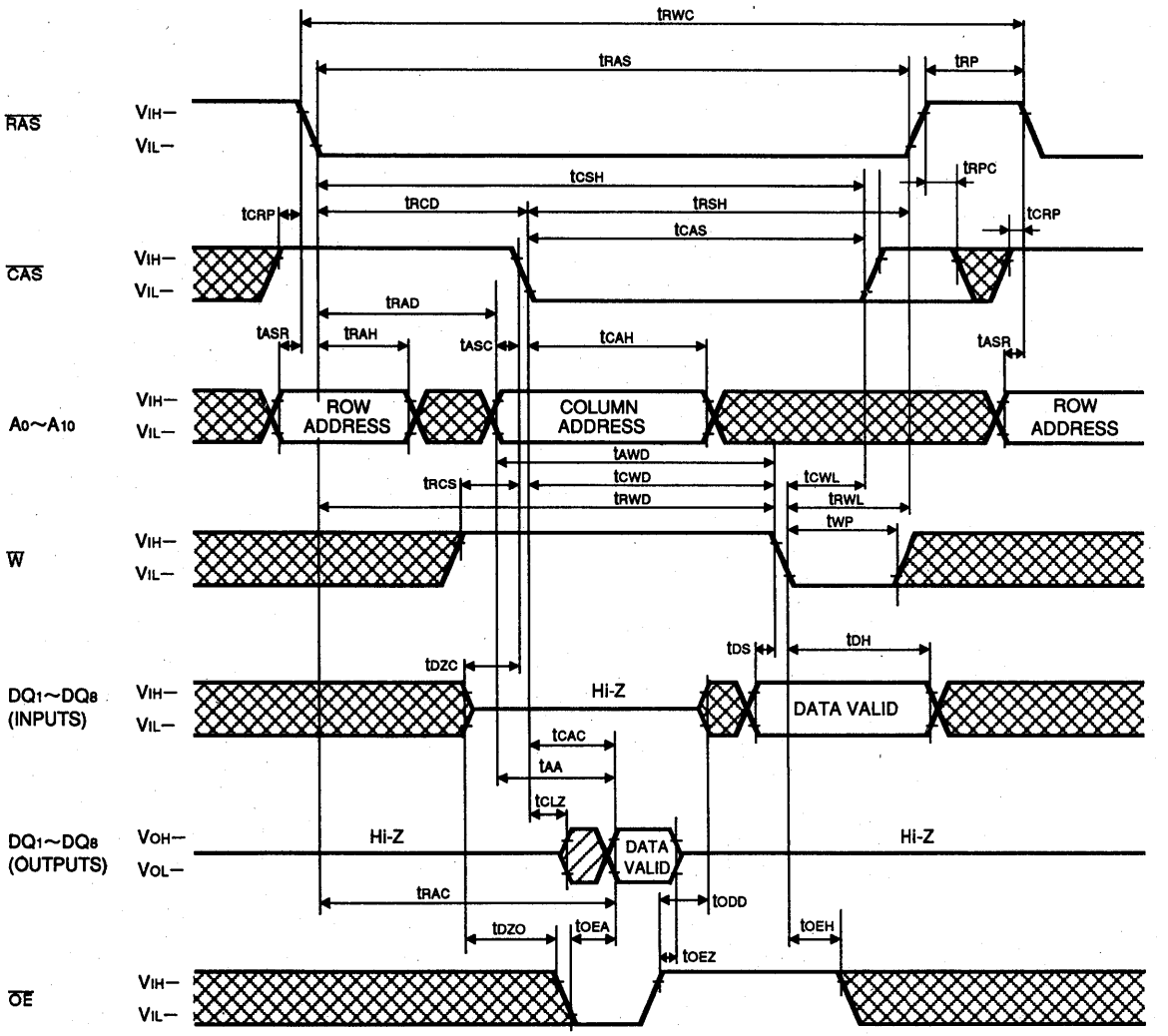


Delay_d Write Cycle

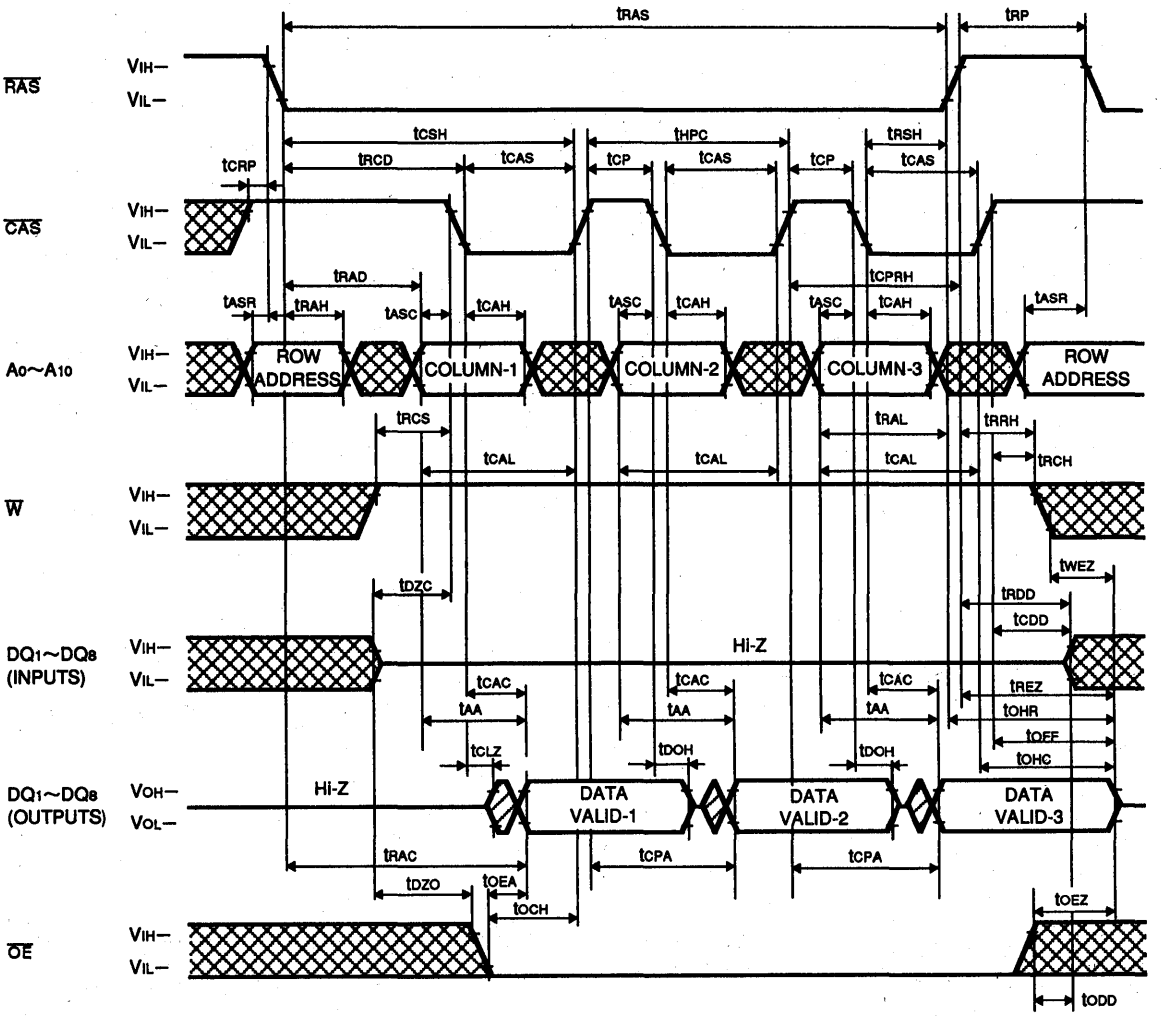


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

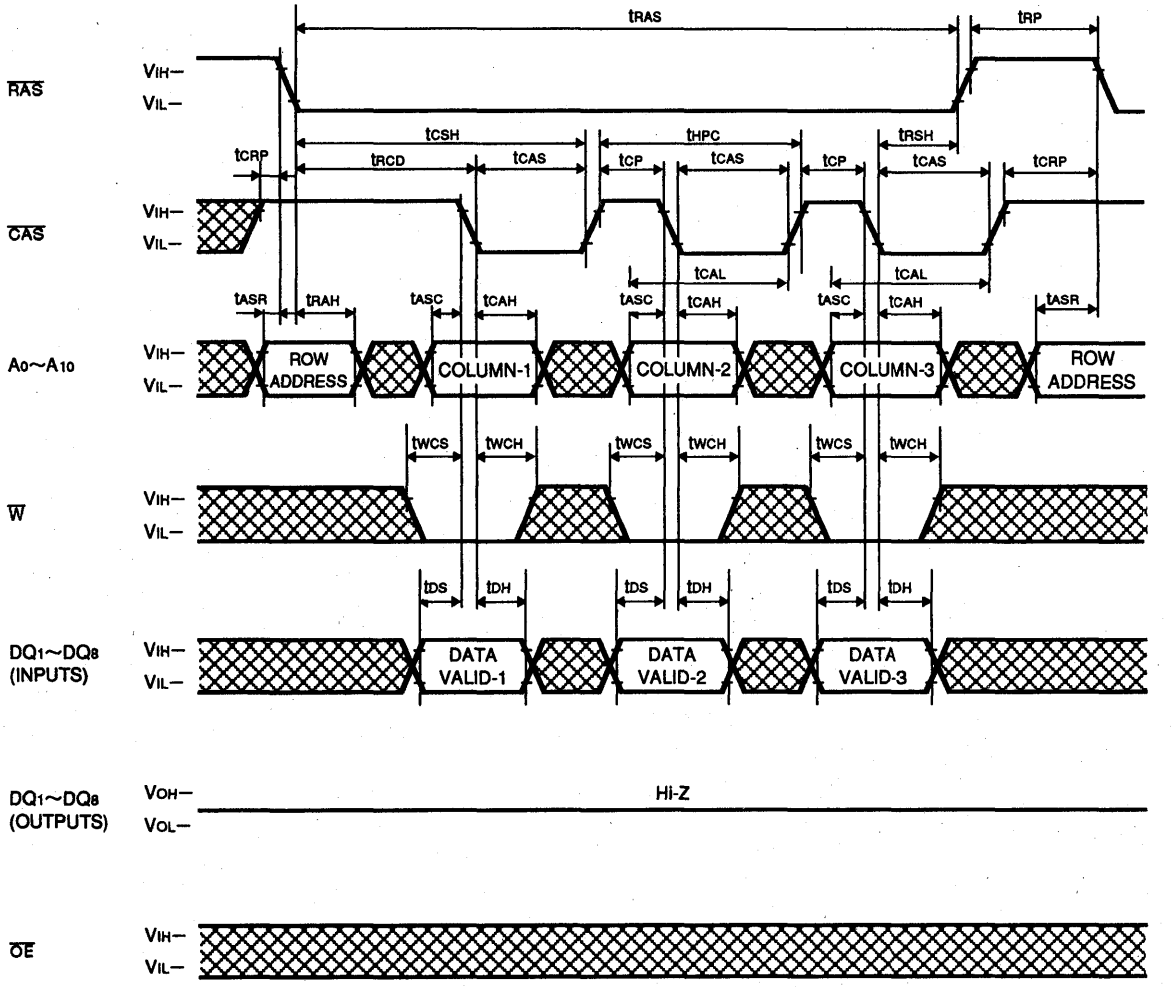
Read-Write, Read-Modify-Write Cycle



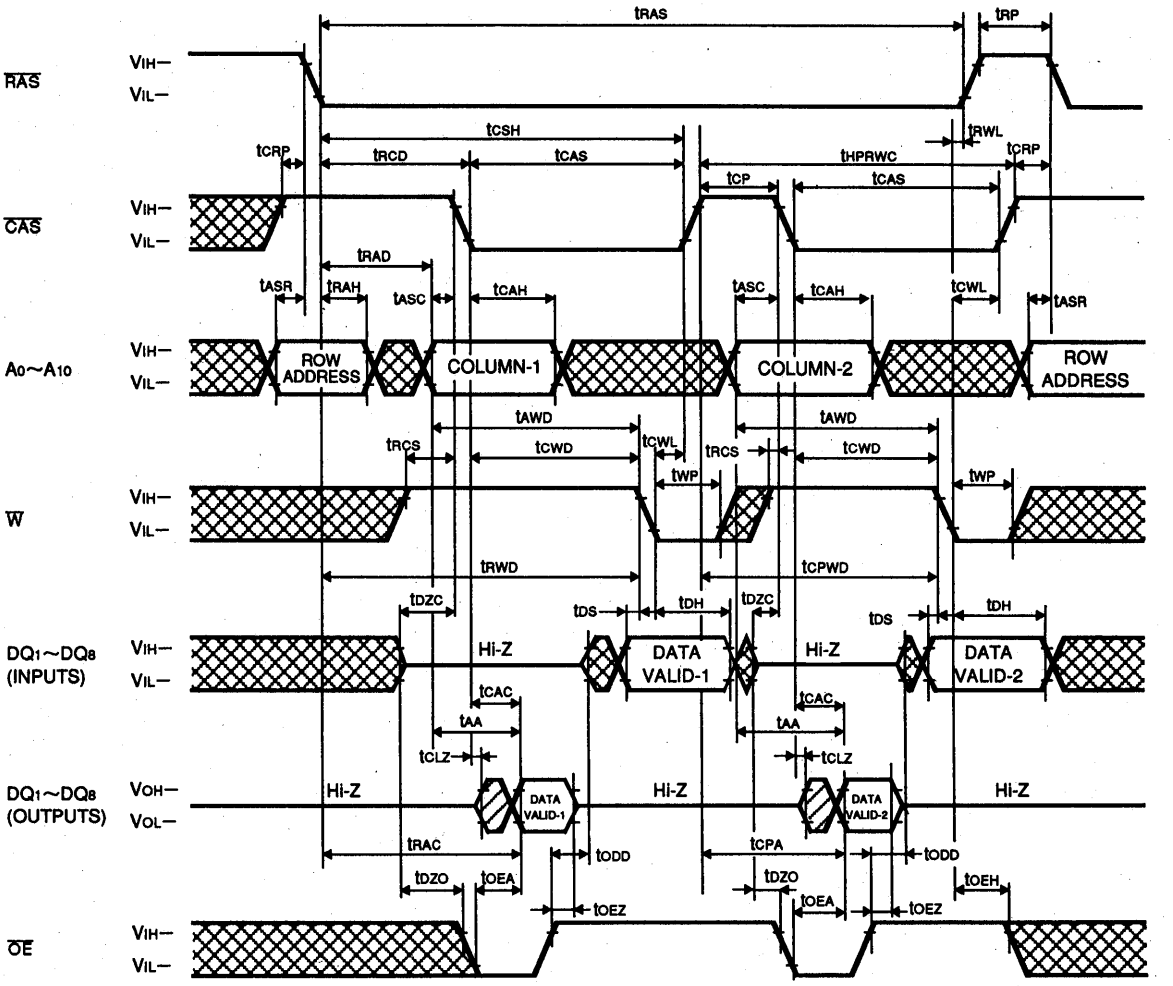
Hyper Page Mode Read Cycle



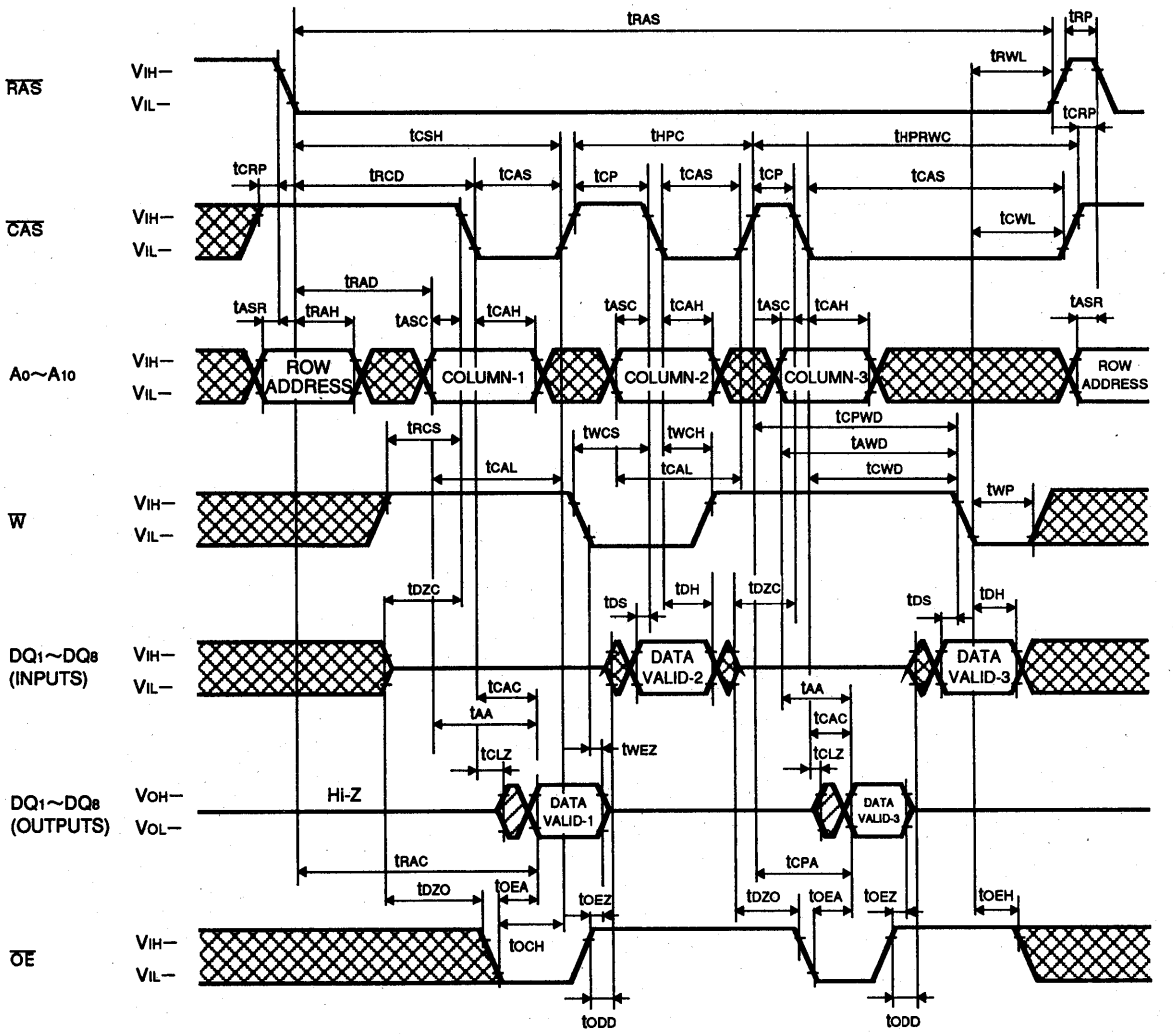
Hyper Page Mode Early Write Cycle



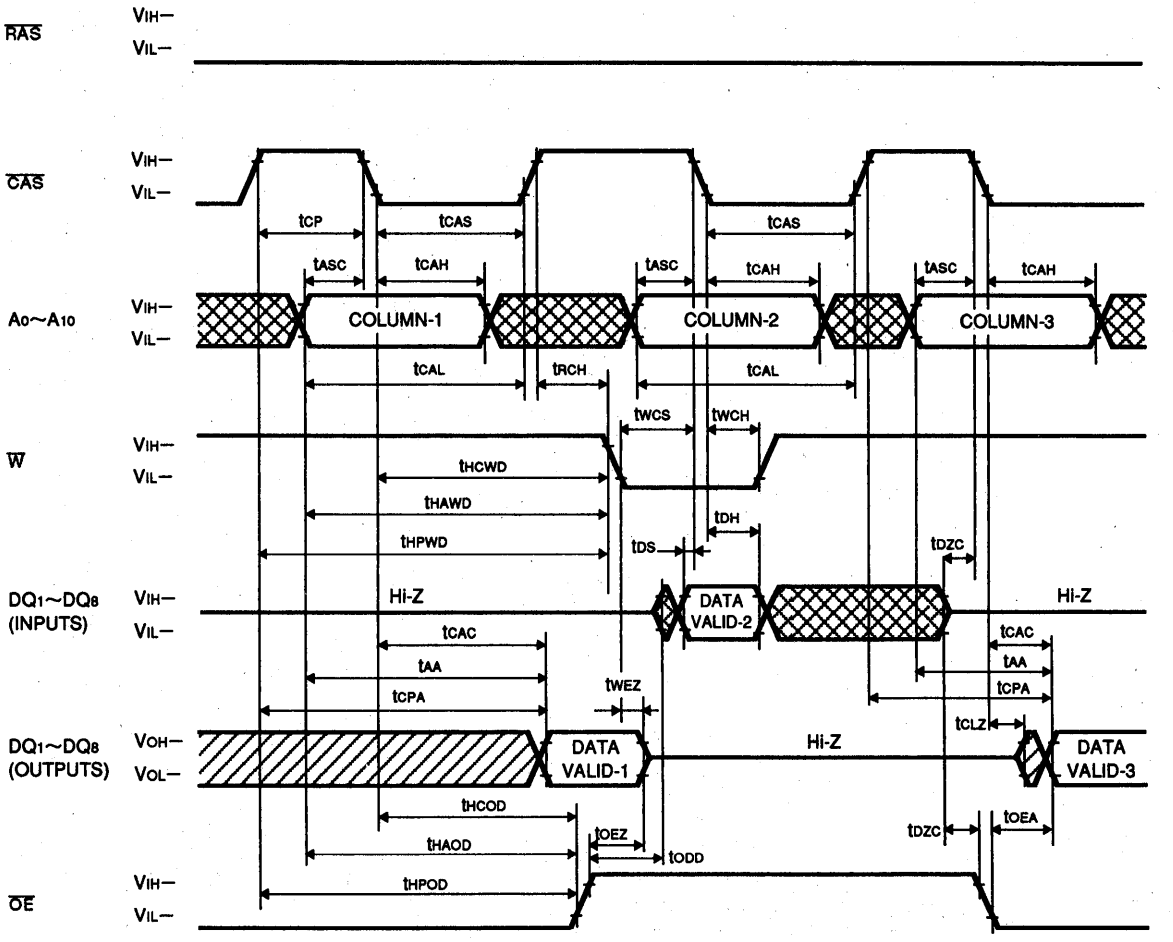
Hyper Page Mode Read-Write,Read-Modify-Write Cycle



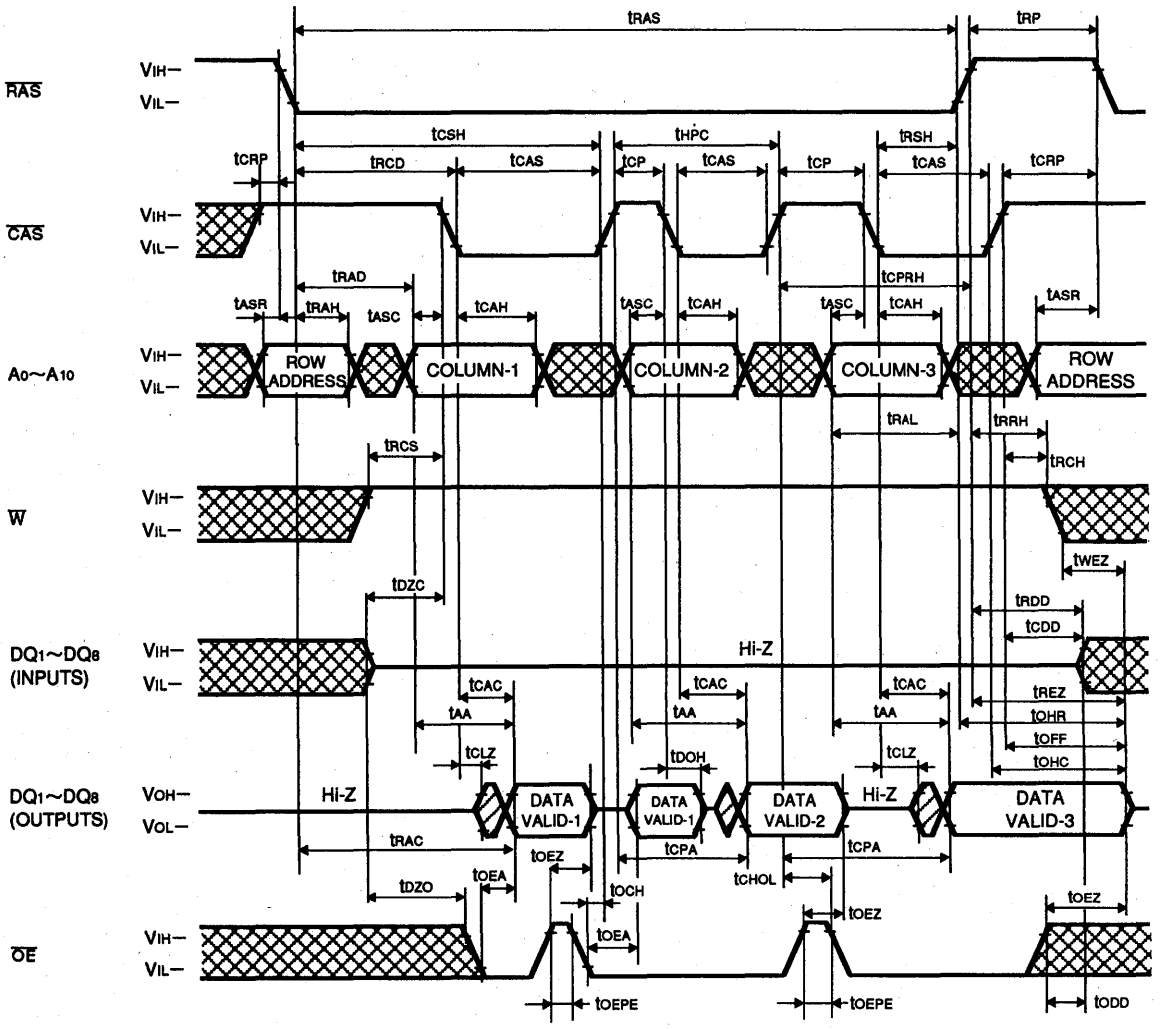
Hyper Page Mode Mix Cycle (1)



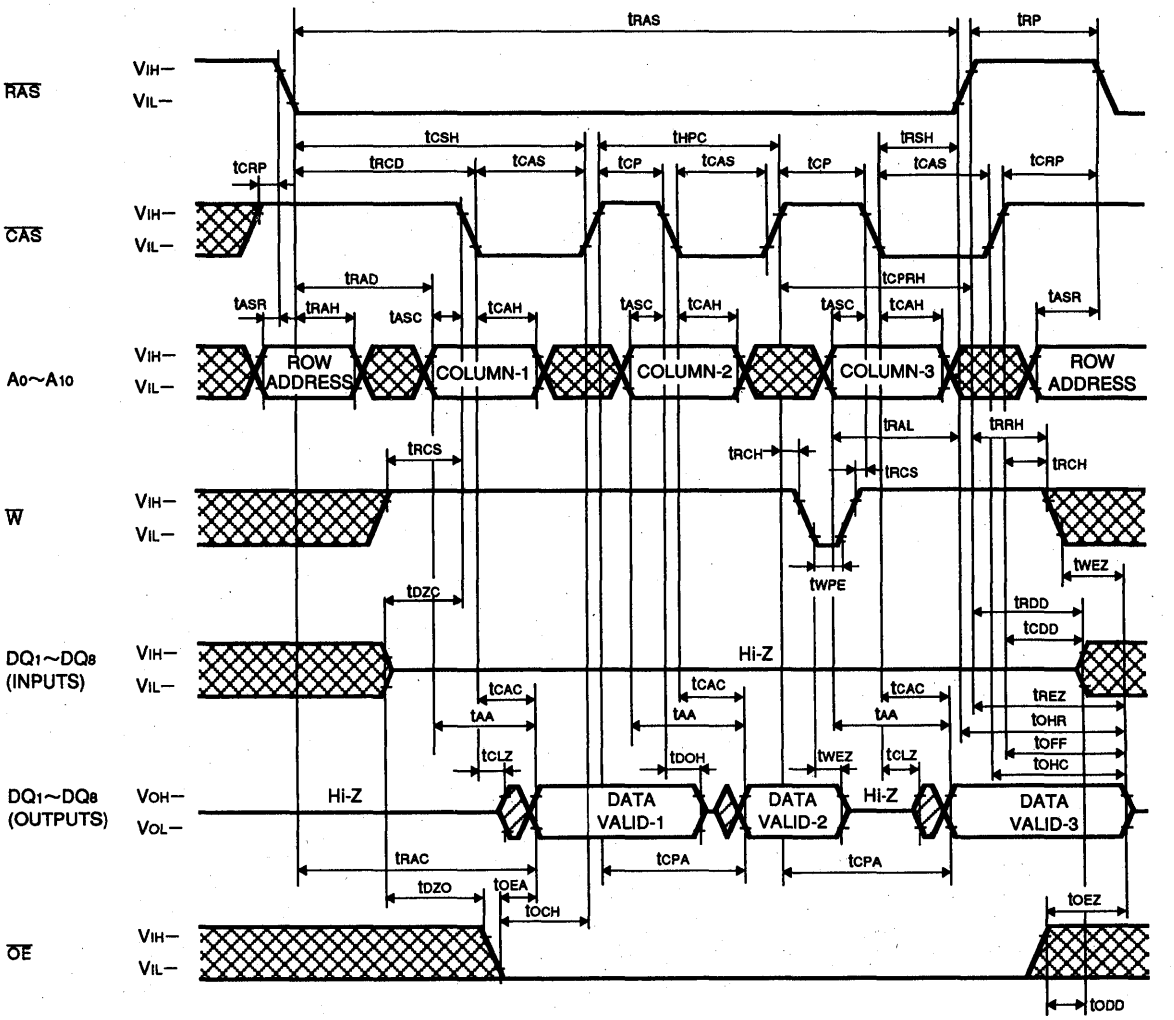
Hyper Page Mode Mix Cycle (2)



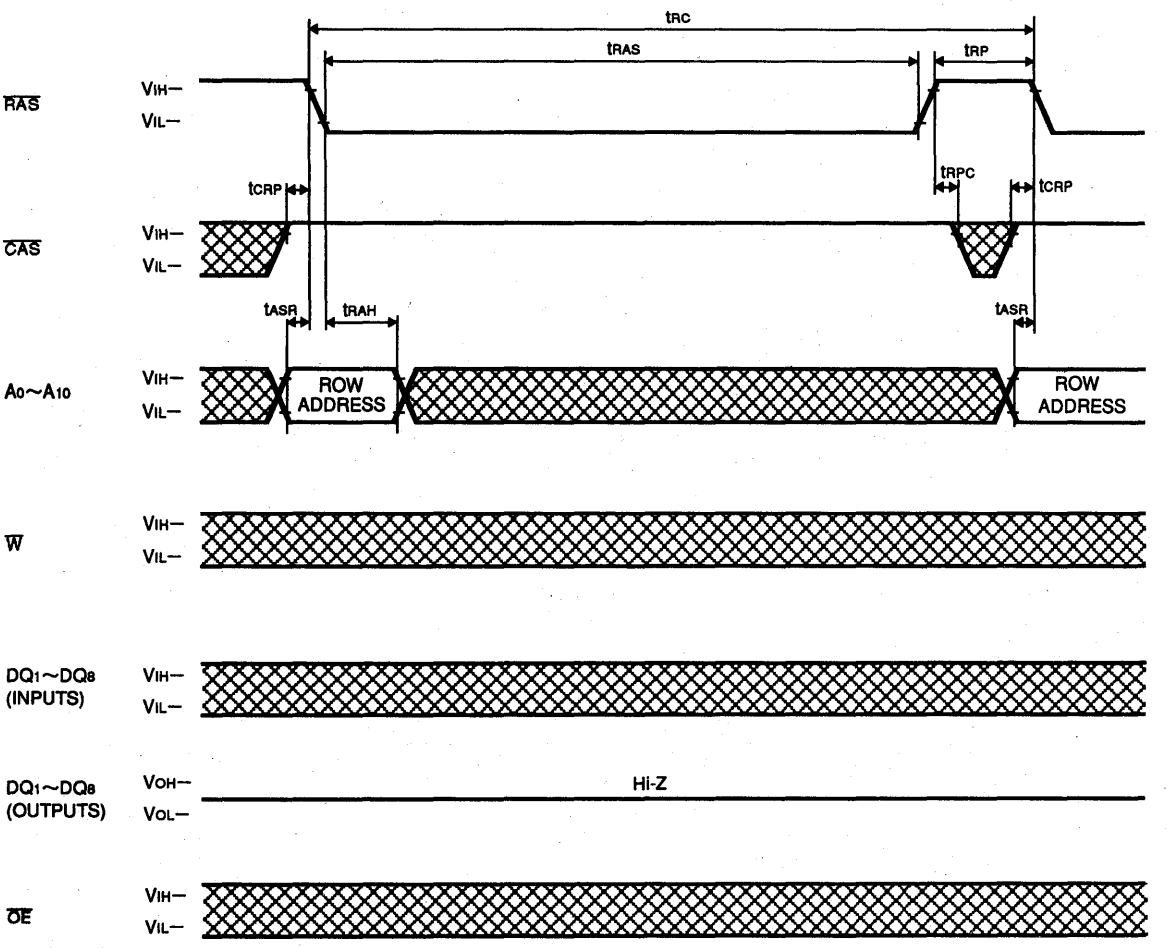
Hyper Page Mode Read Cycle (HI-Z control by $\overline{OE}$)



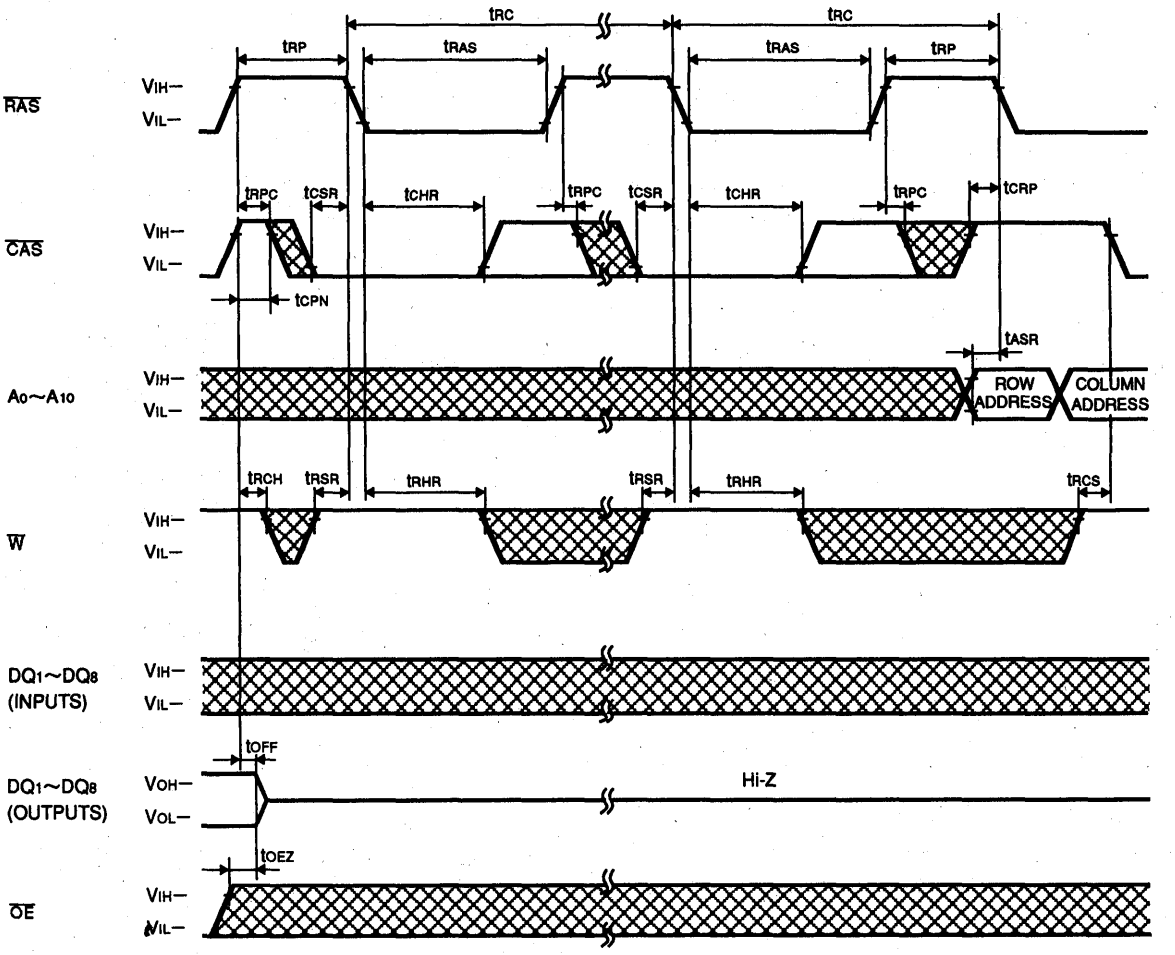
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



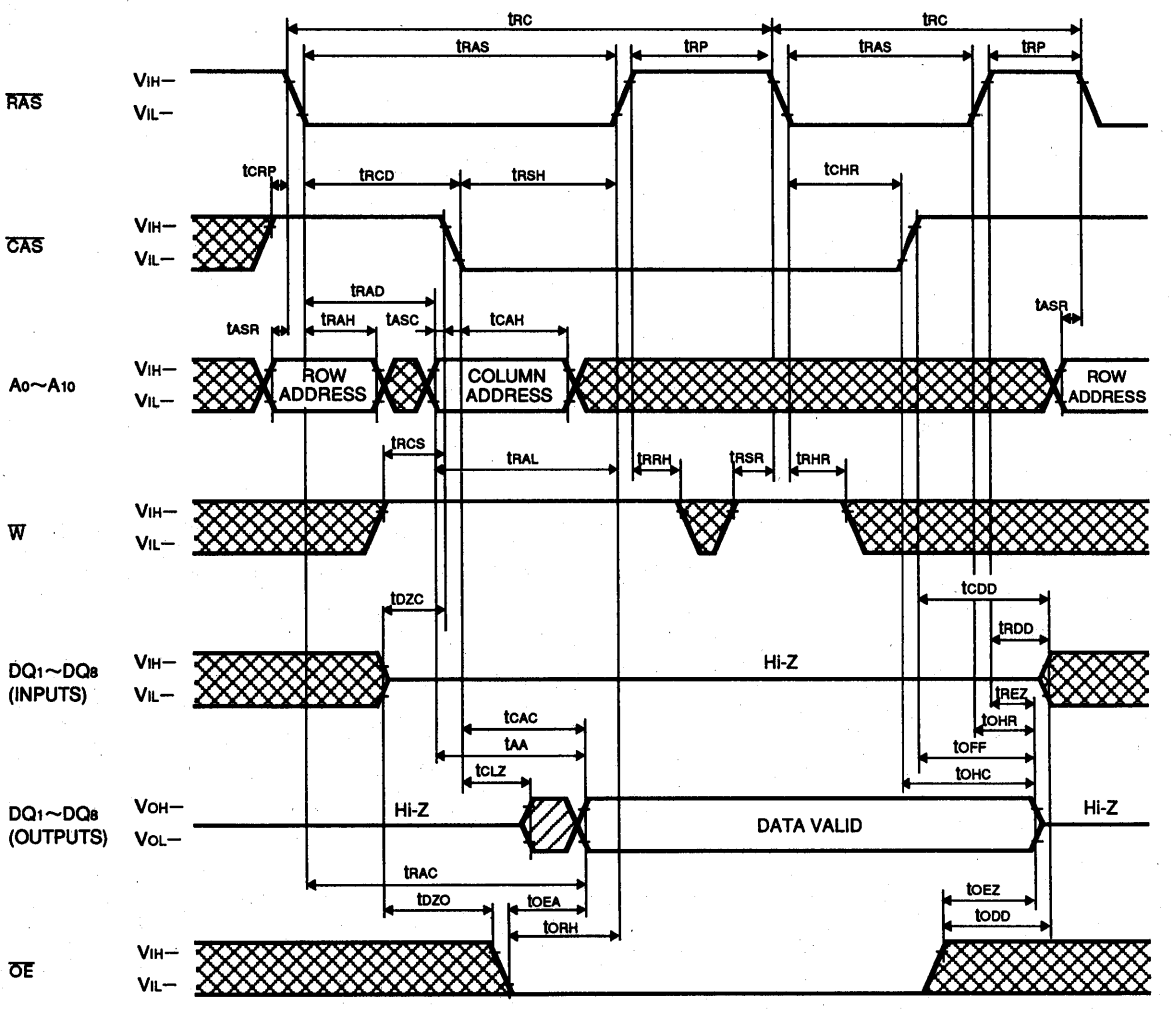
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

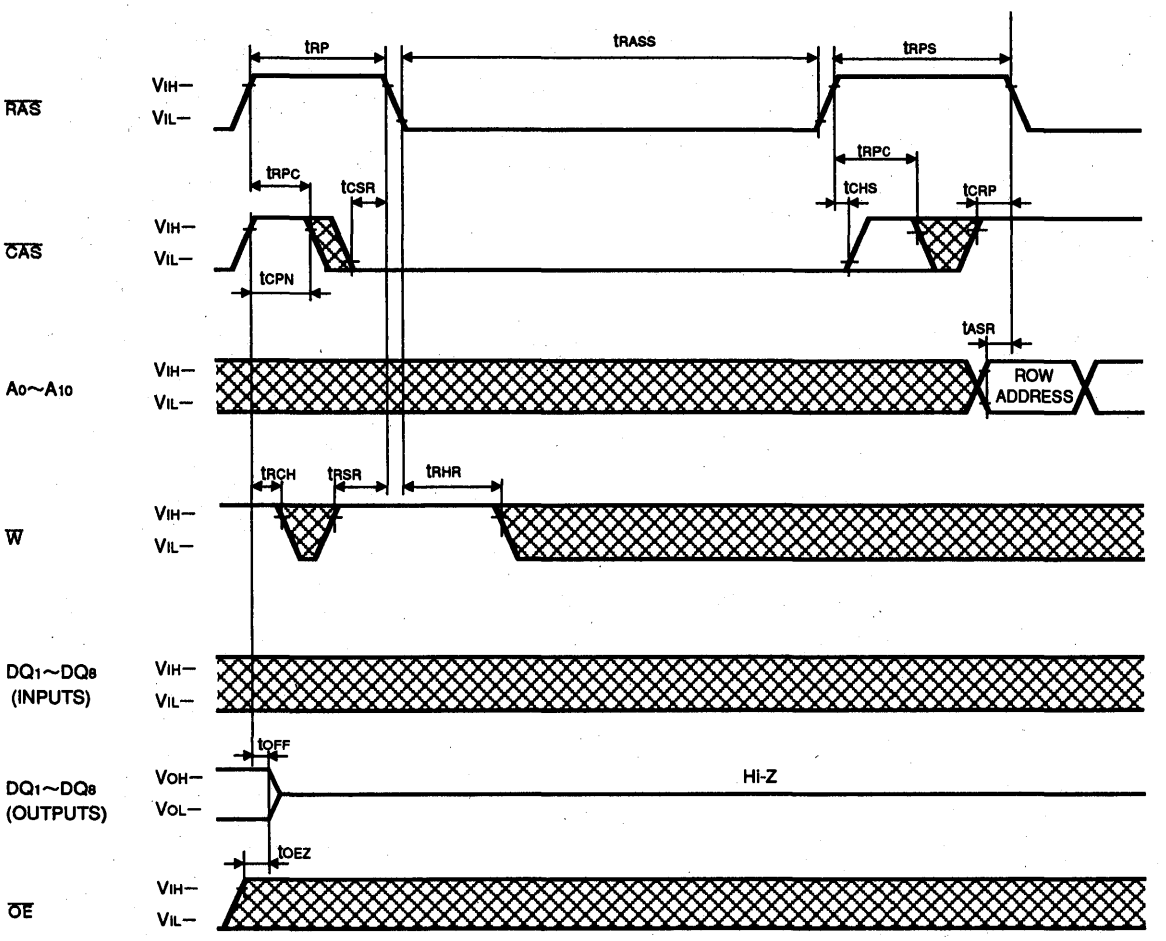


Hidden Refresh Cycle (Read) (Note 33)

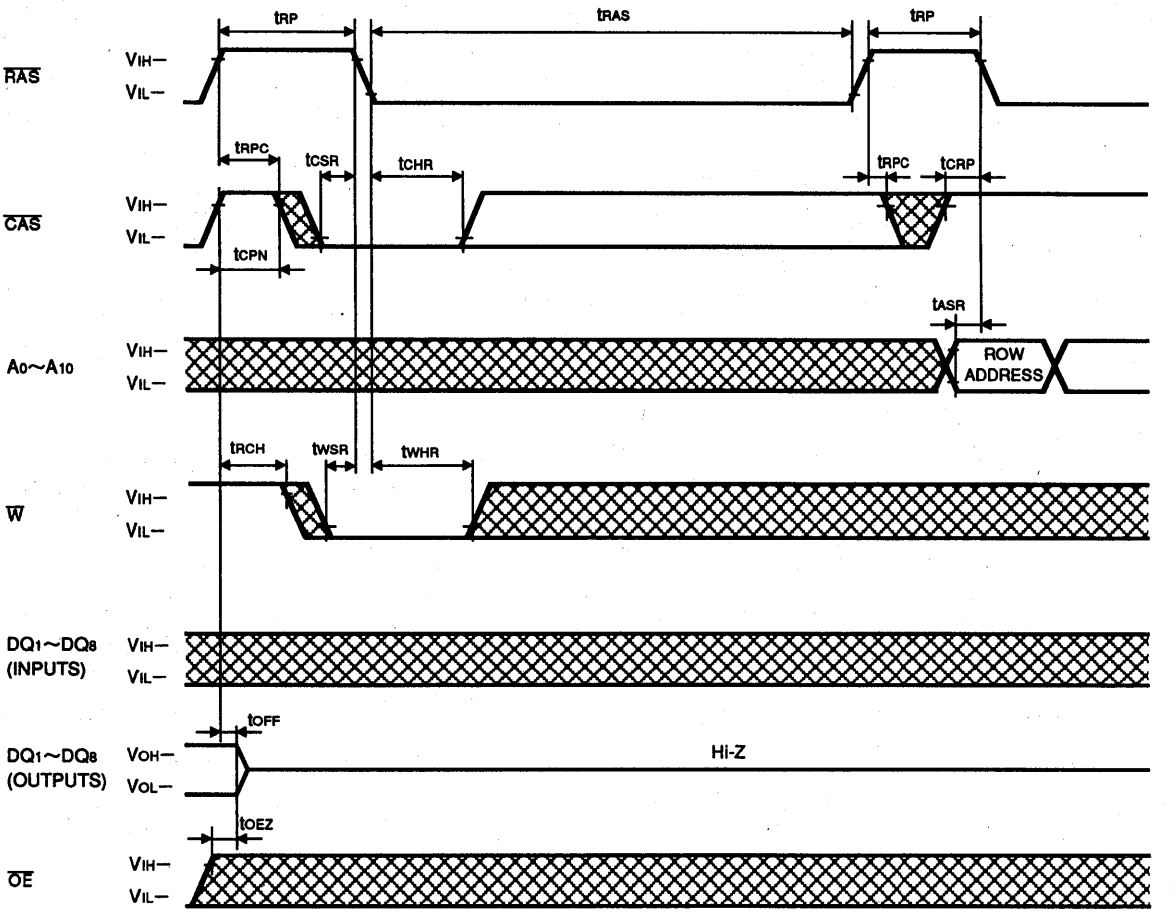


Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up , however entried into Test Mode.

M5M416160BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416160BXX-6,-6S	60	15	30	15	110	430
M5M416160BXX-7,-7S	70	20	35	20	130	385

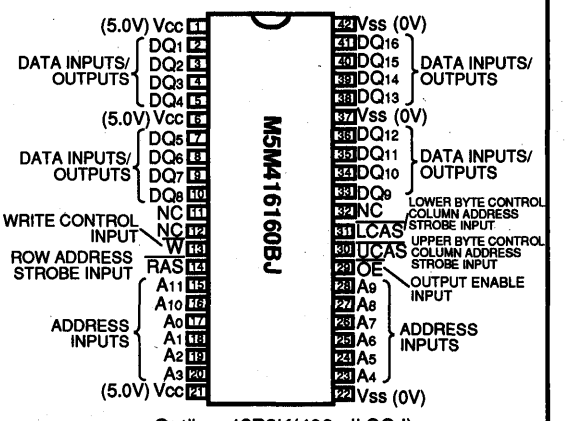
XX=J,TP

- Standard 42pin SOJ, 50pin TSOP
- Single 5.0V ± 10% supply
- Low stand-by power dissipation
  5.5mW (Max) ..... CMOS Input level
- Low operating power dissipation
  M5M416160Bxx -6, -6S ..... 530.0mW (Max)
  M5M416160Bxx -7, -7S ..... 470.0mW (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})

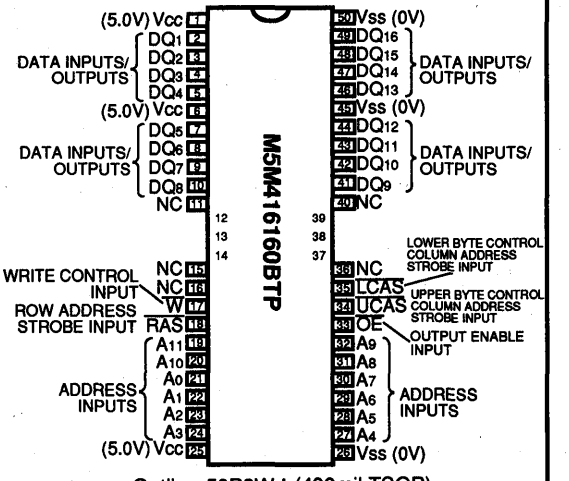
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 42P0K(400mil SOJ)



Outline 50P3W-L(400mil TSOP)

NC : NO CONNECTION

FUNCTION

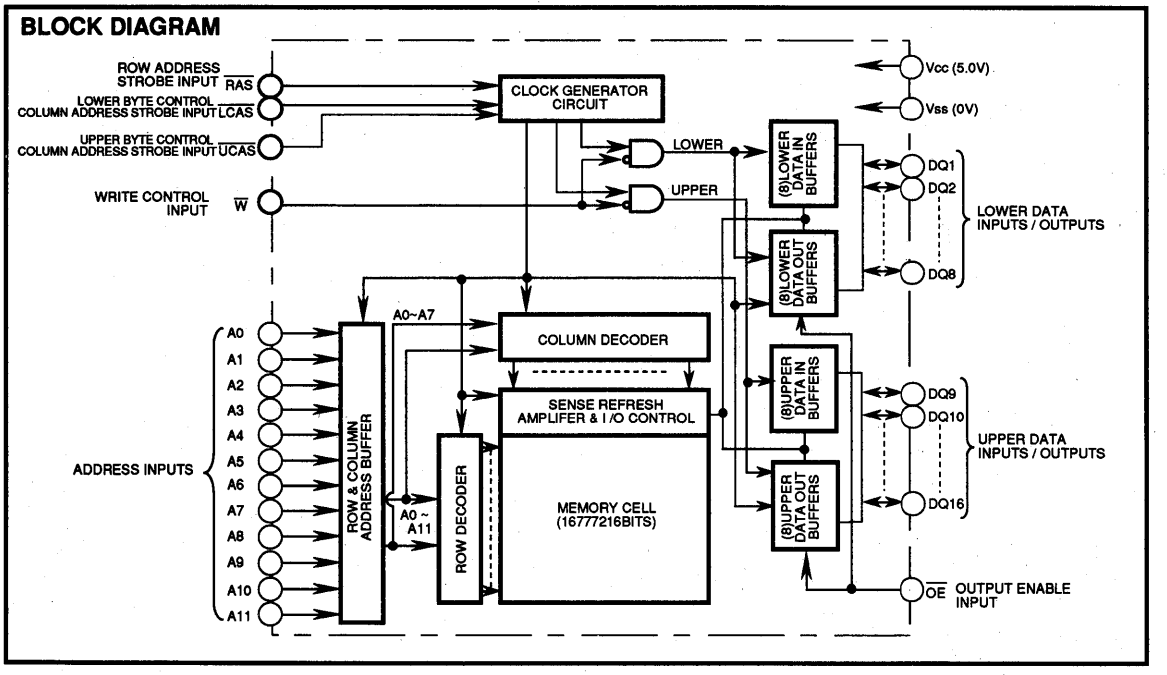
The M5M416160BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
Vo	Output voltage		-1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M416160B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			95	mA
		M5M416160B-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M416160B-6,-7	$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			1	
		M5M416160B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			0.3	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M416160B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			95	mA
		M5M416160B-7,-7S				85	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M416160B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			70	mA
		M5M416160B-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416160B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			95	mA
		M5M416160B-7,-7S				85	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS/UCAS}$=V_{IH} .

CAPACITANCE (Ta=0～70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, $\overline{W}$ input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~ 70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M416160B-6,-6S		M5M416160B-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note7,8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note7,9)		60		70	ns
tAA	Column address access time	(Note 7,10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 100pF, VOH=2.4V(IOH=-5mA) and VOL=0.4V(IOL=4.2mA).
8: Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max).
9: Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10: Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).
11: Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).
12: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (|IOUT| ≦ ± 10 μA) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted , see notes 13,14)

Symbol	Parameter		Limits				Unit
			M5M416160B-6,-6S		M5M416160B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		64		64	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note19)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note19)	15		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M416160B-6,-6S		M5M416160B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note22)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note23)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note23)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD\ (min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M416160B-6,-6S		M5M416160B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note25)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note23)	60		65		ns

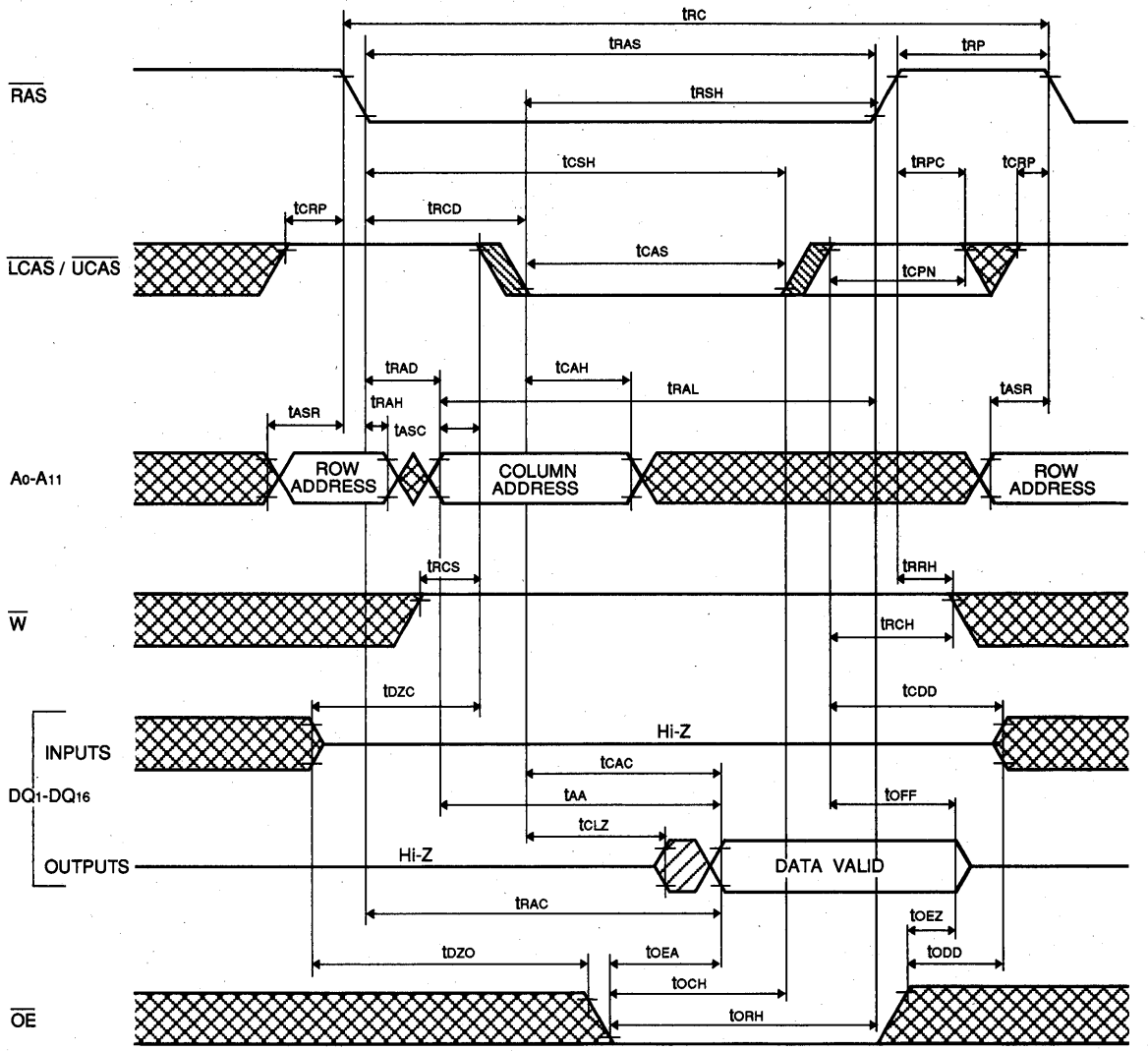
Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



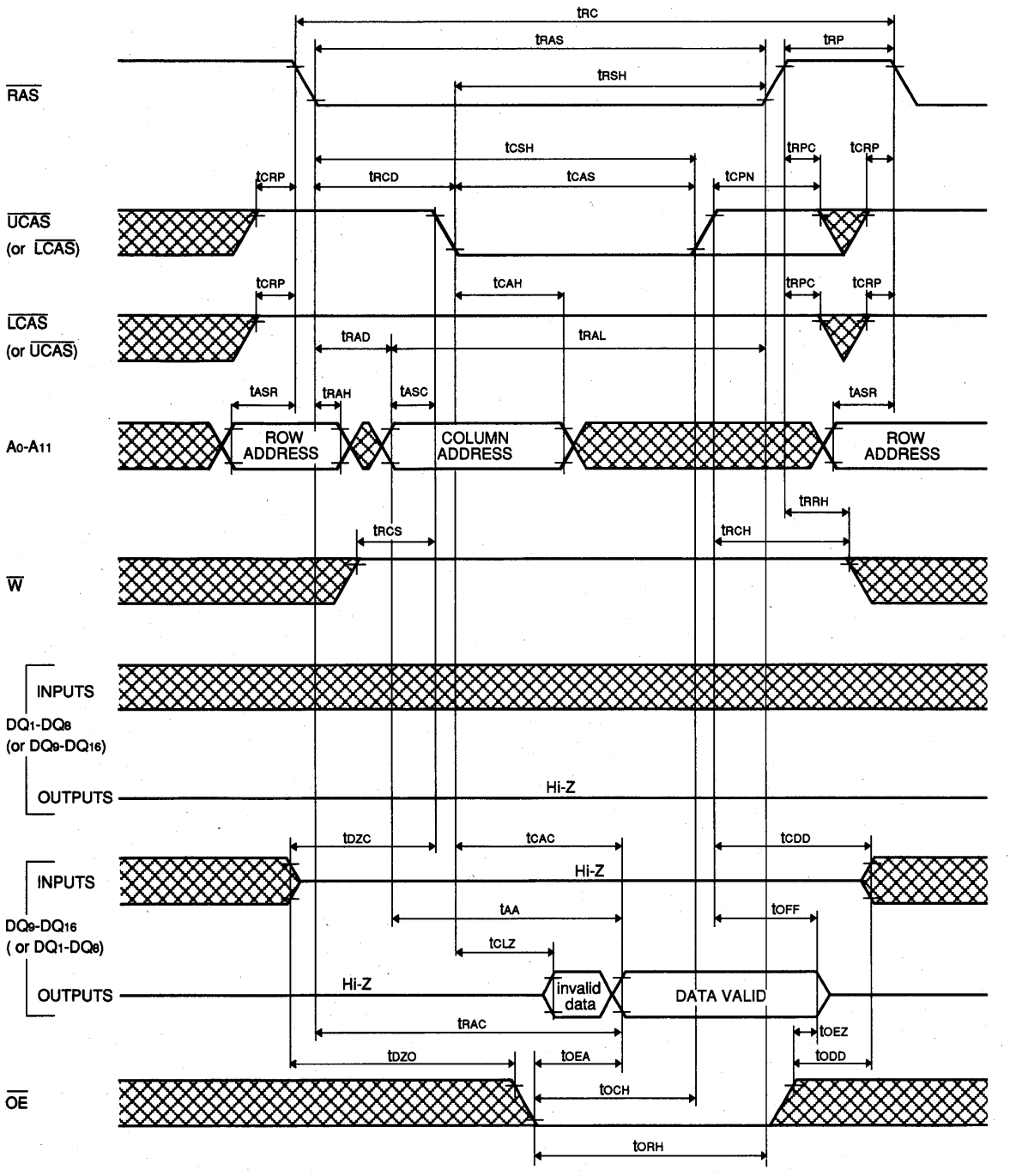
Note 28

Indicates the don't care input.
$V_{IH}(min.) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min.) \leqq V_{IN} \leqq V_{IL}(max)$

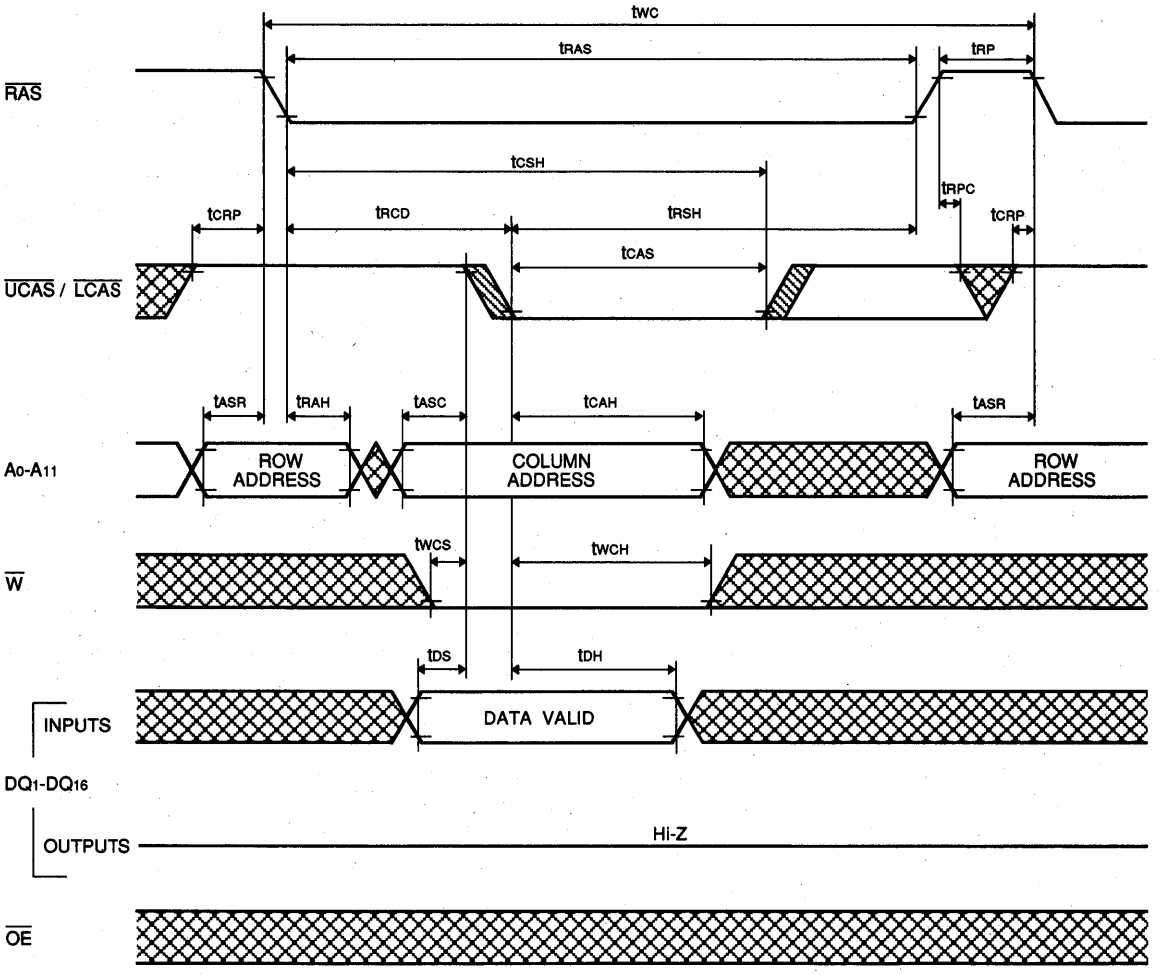
Indicates the invalid output.

Indicates the skew of the two inputs.

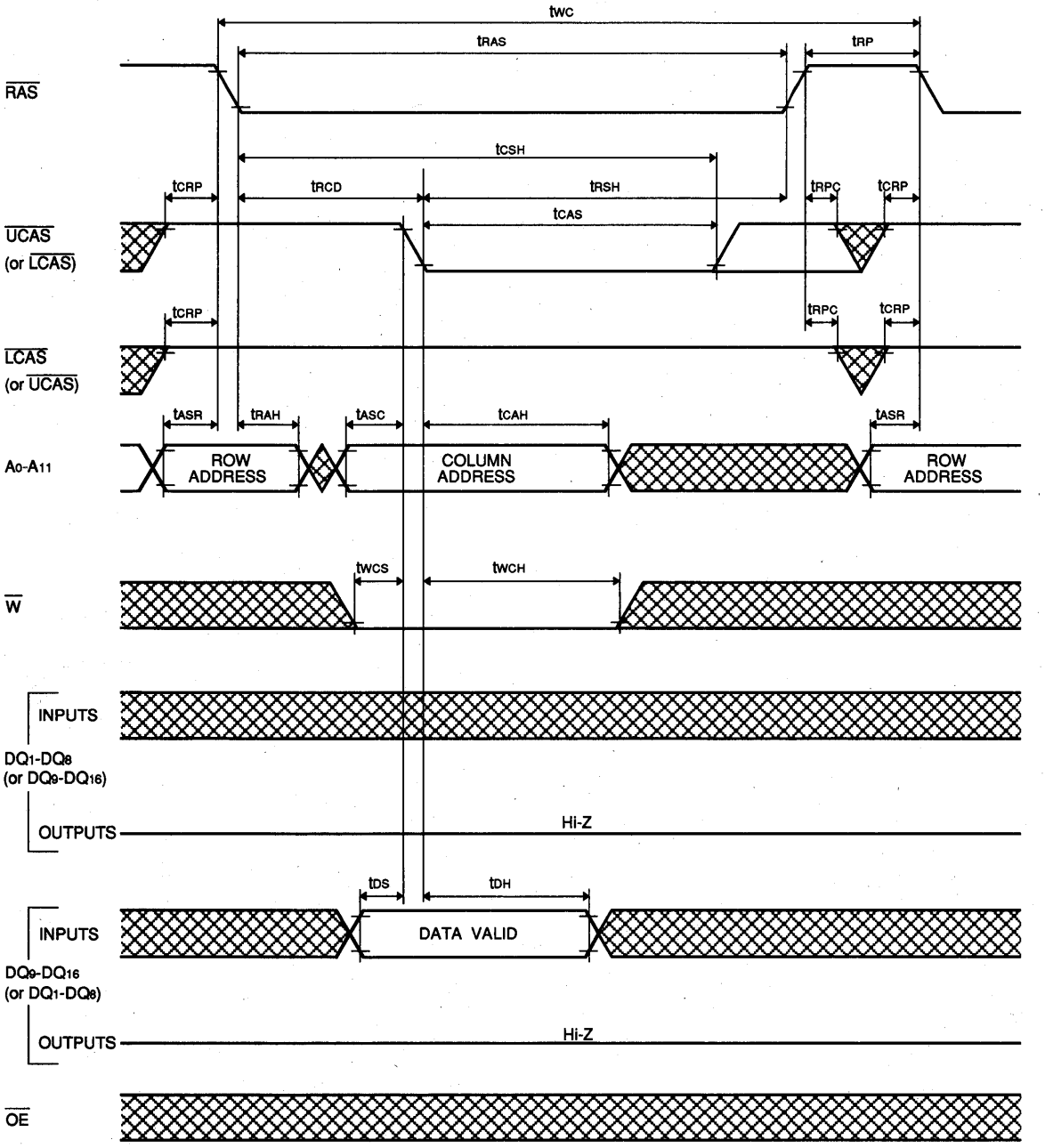
Upper / (Lower) Byte Read Cycle



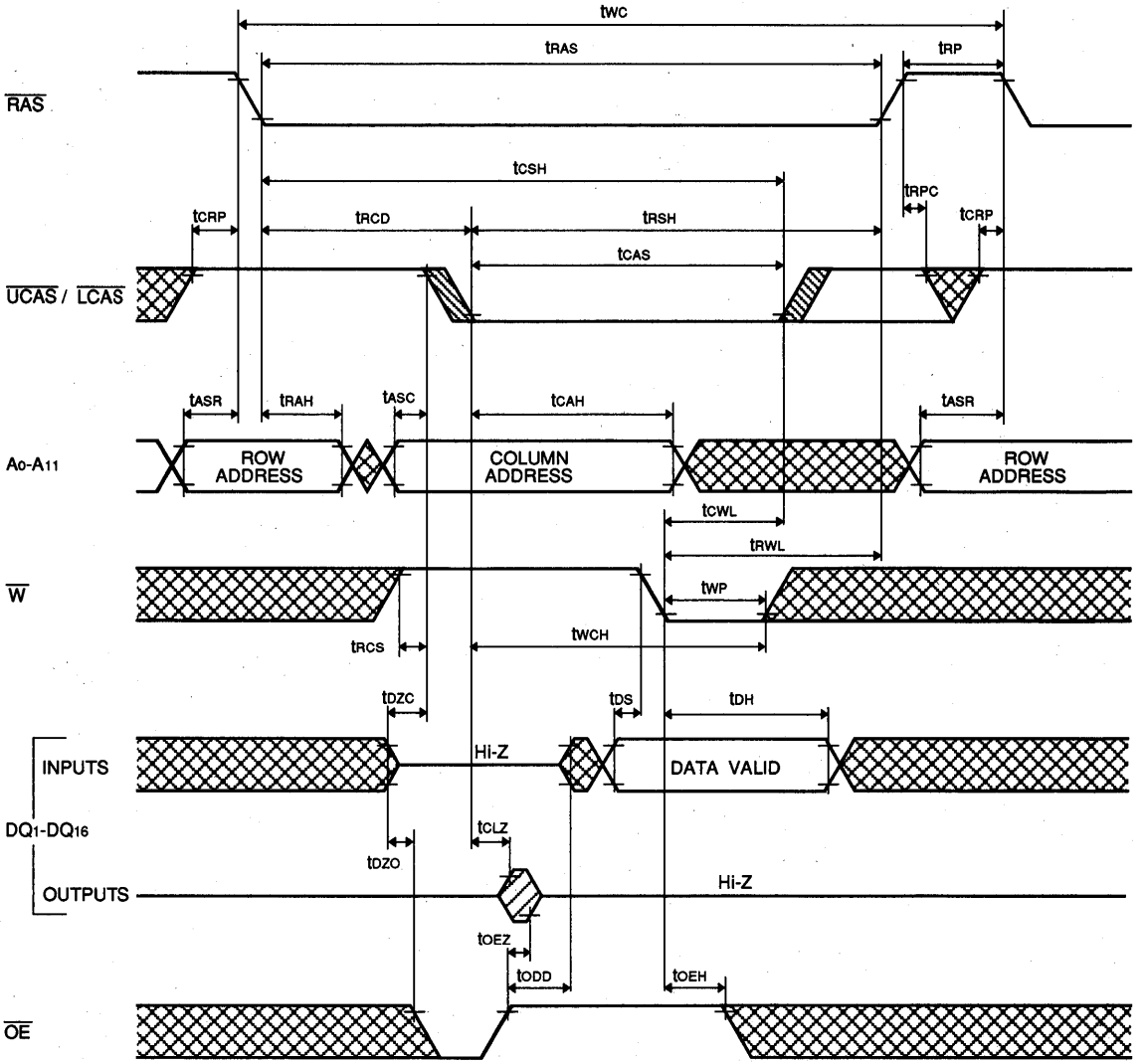
Write Cycle (Early write)



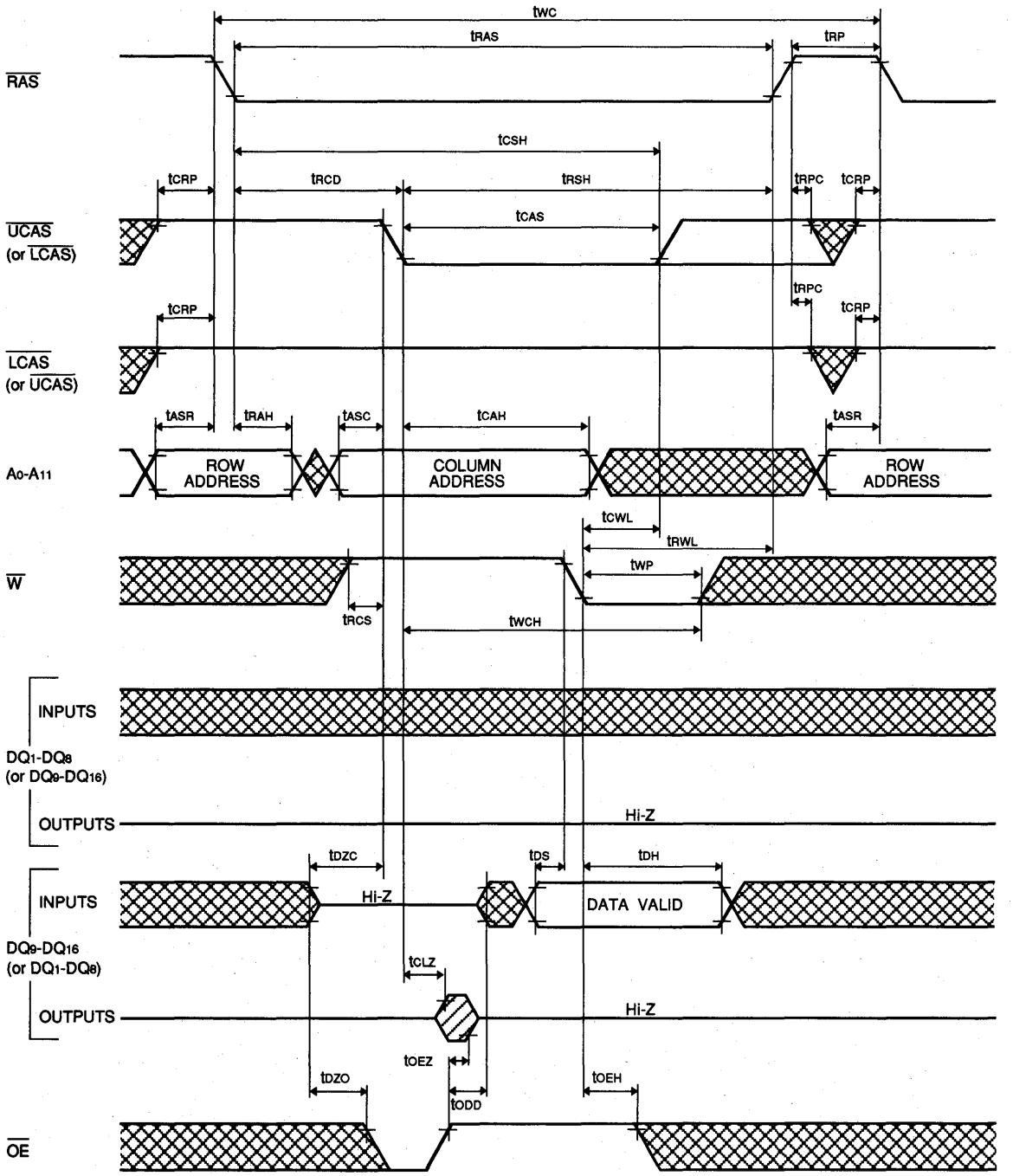
Upper/(Lower) Byte Write Cycle (Early write)



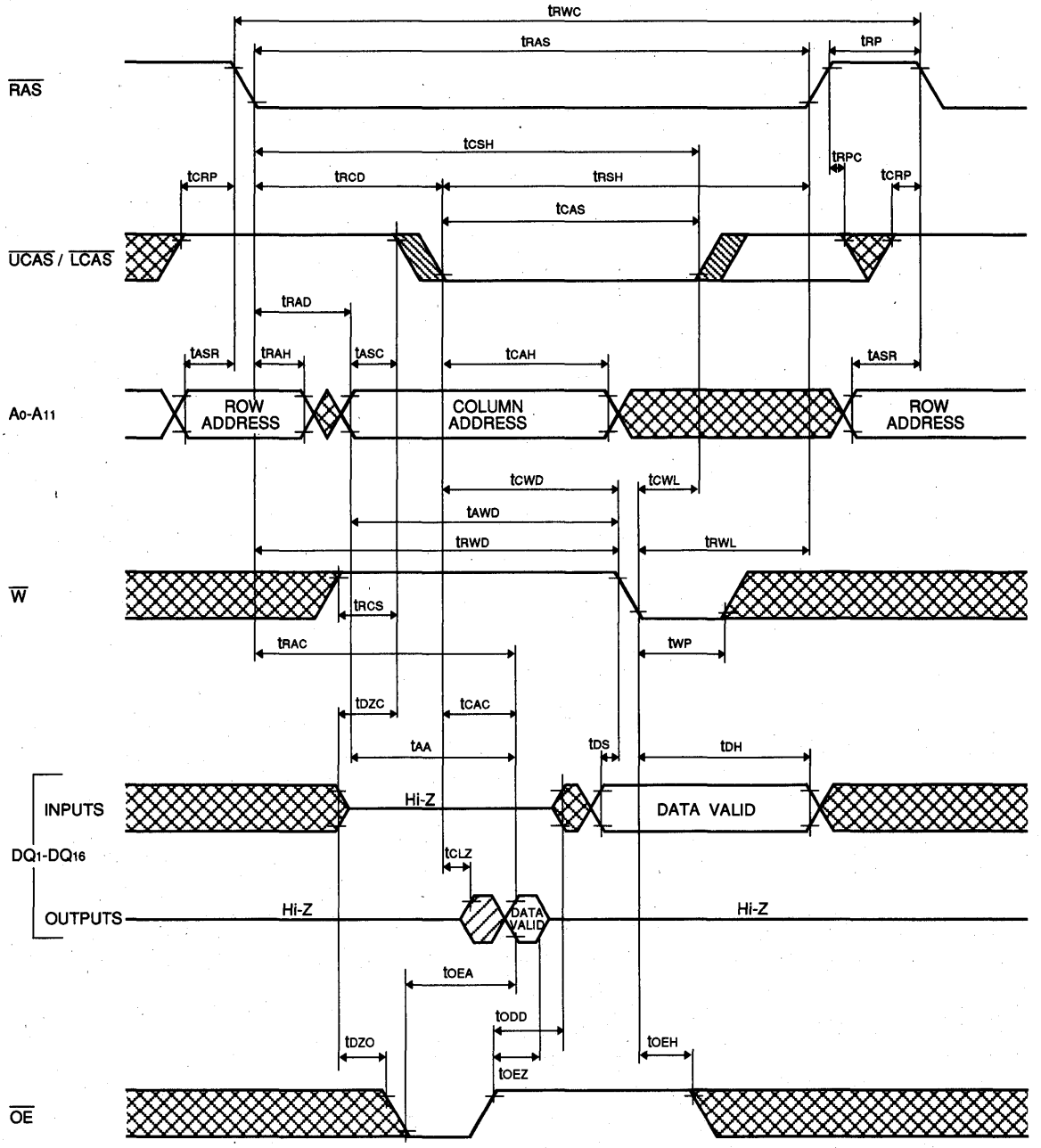
Write Cycle (Delayed write)



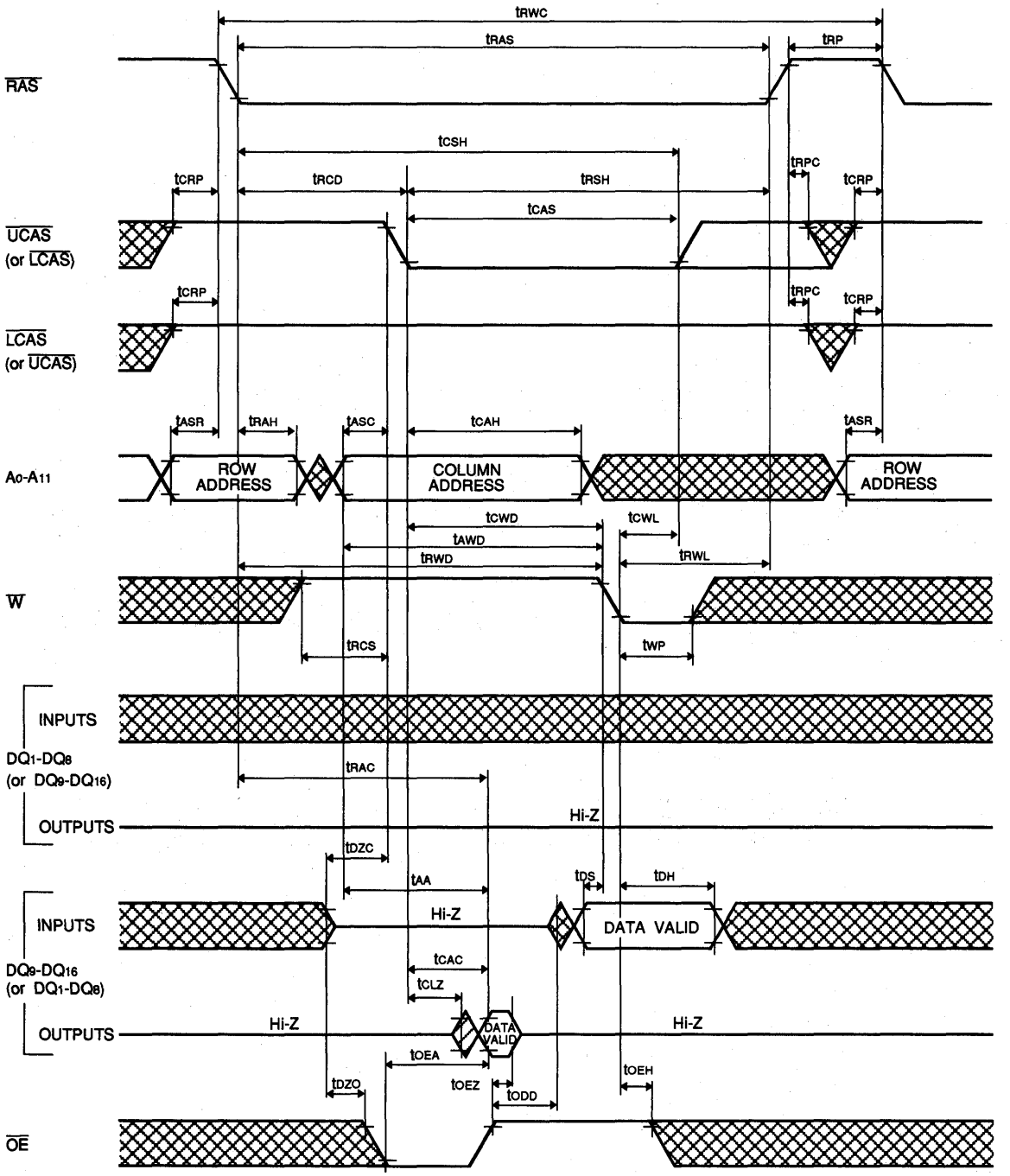
Upper/(Lower) Byte Write Cycle (Delayed write)



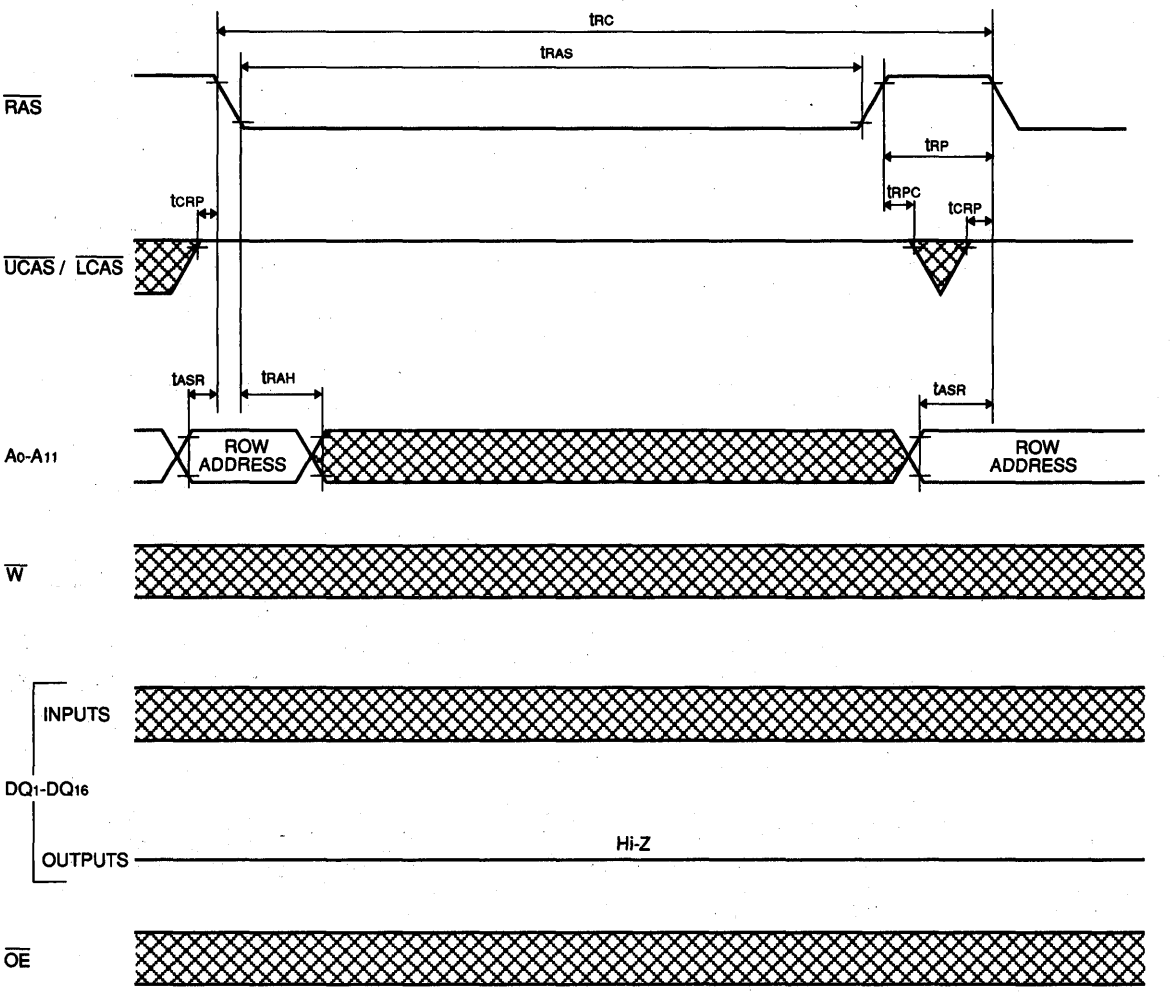
Read-Write, Read-Modify-Write Cycle



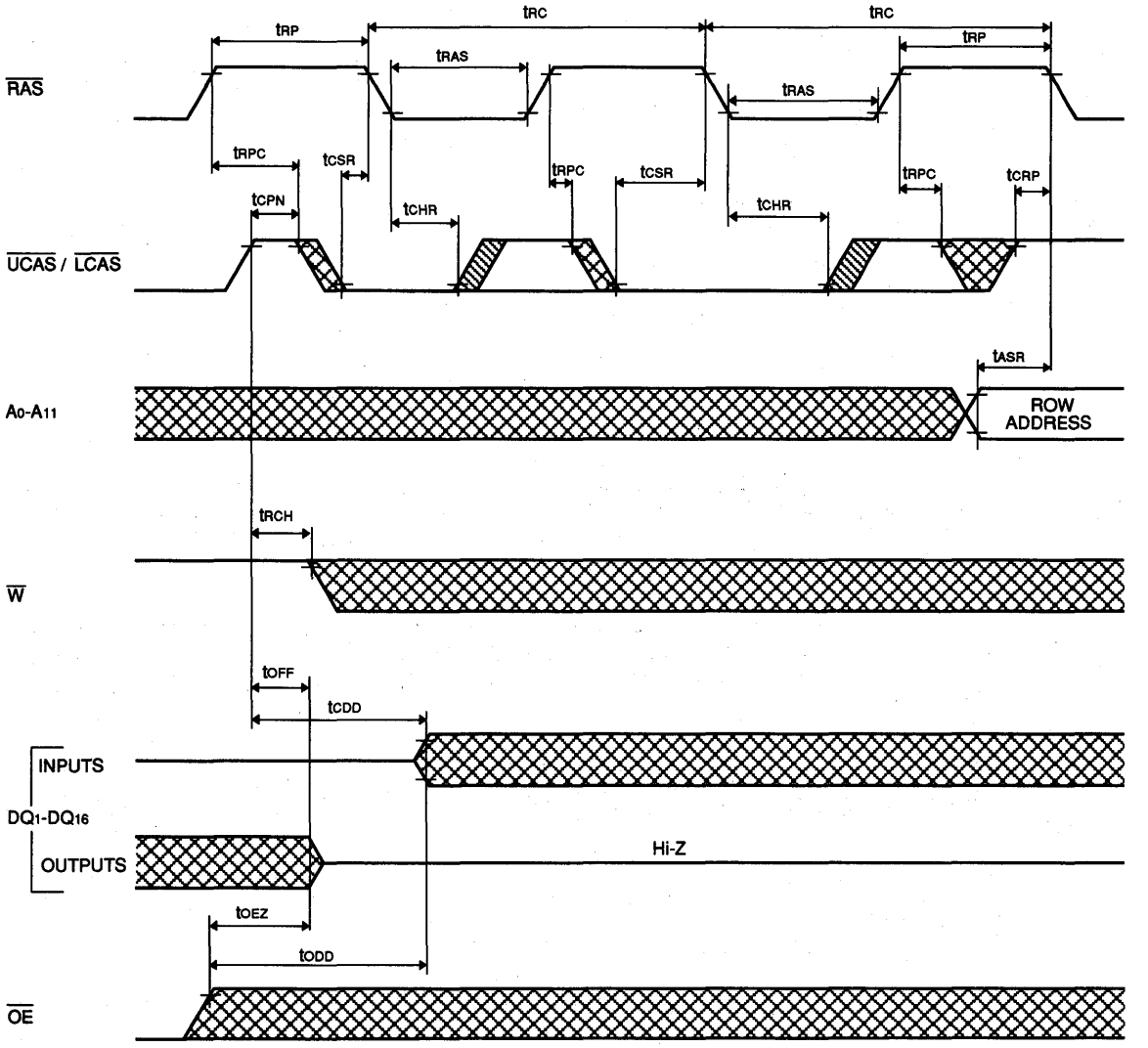
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



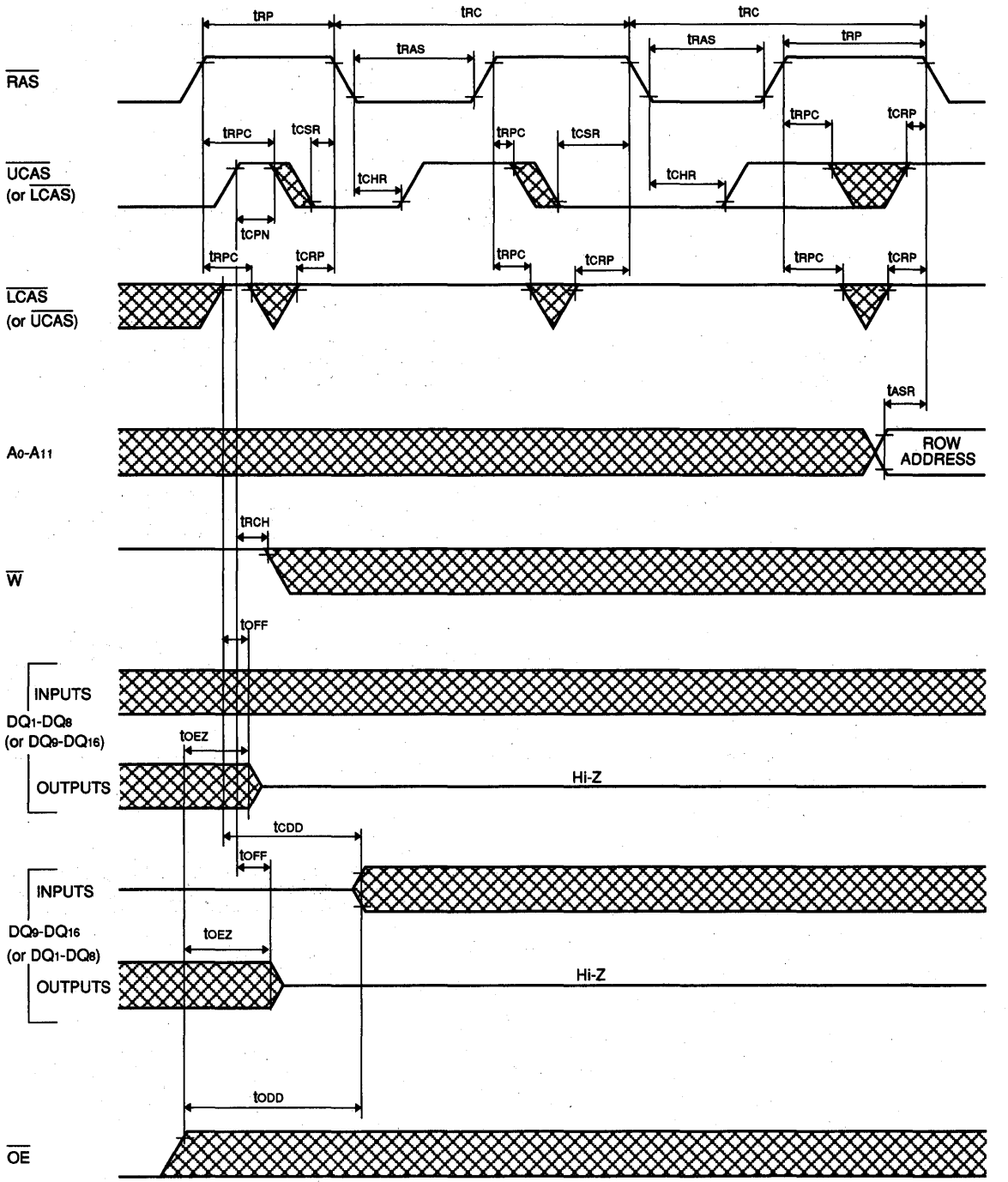
$\overline{\text{RAS}}$-only Refresh Cycle



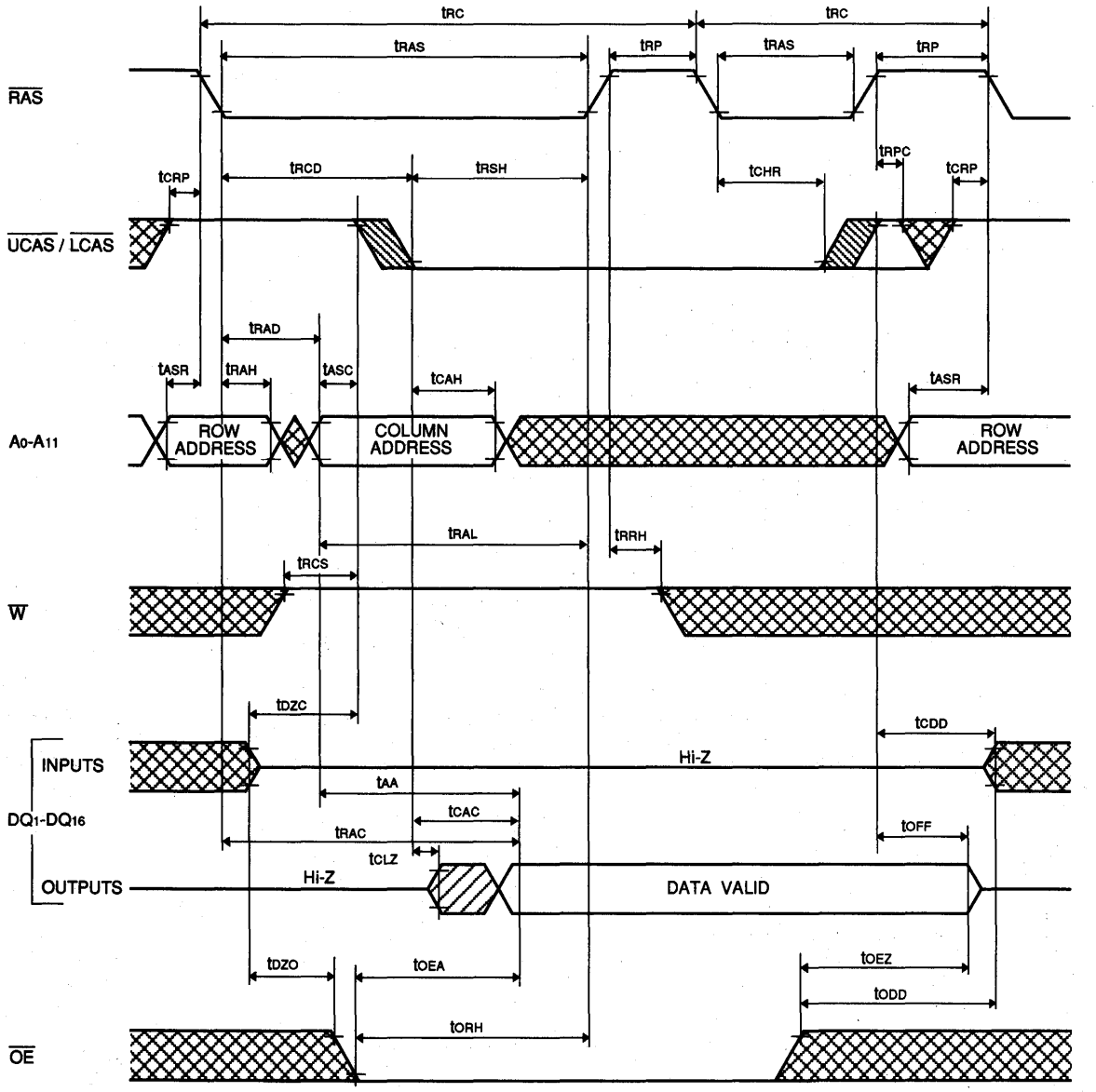
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

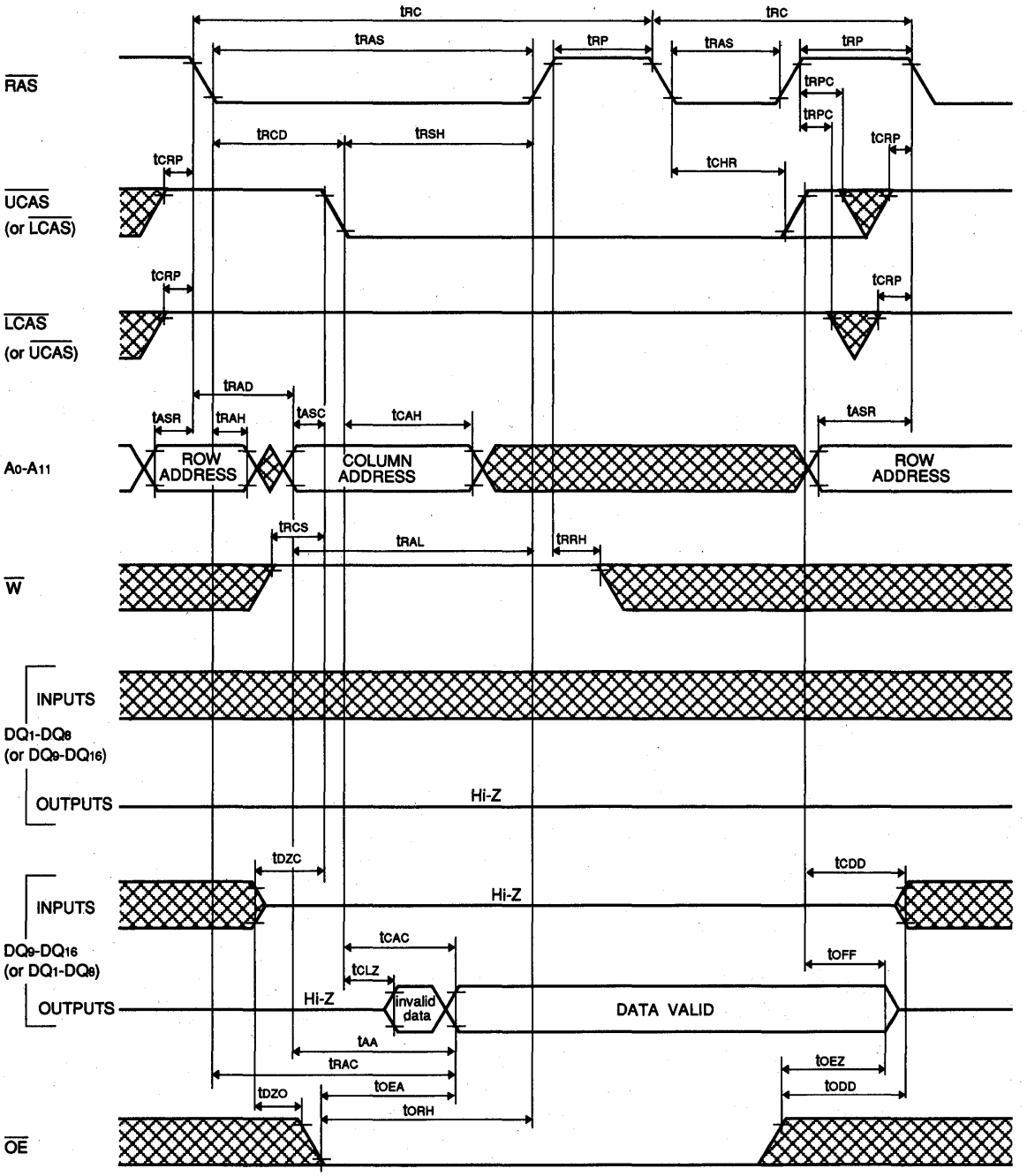


Hidden Refresh Cycle (Read) (Note 29)

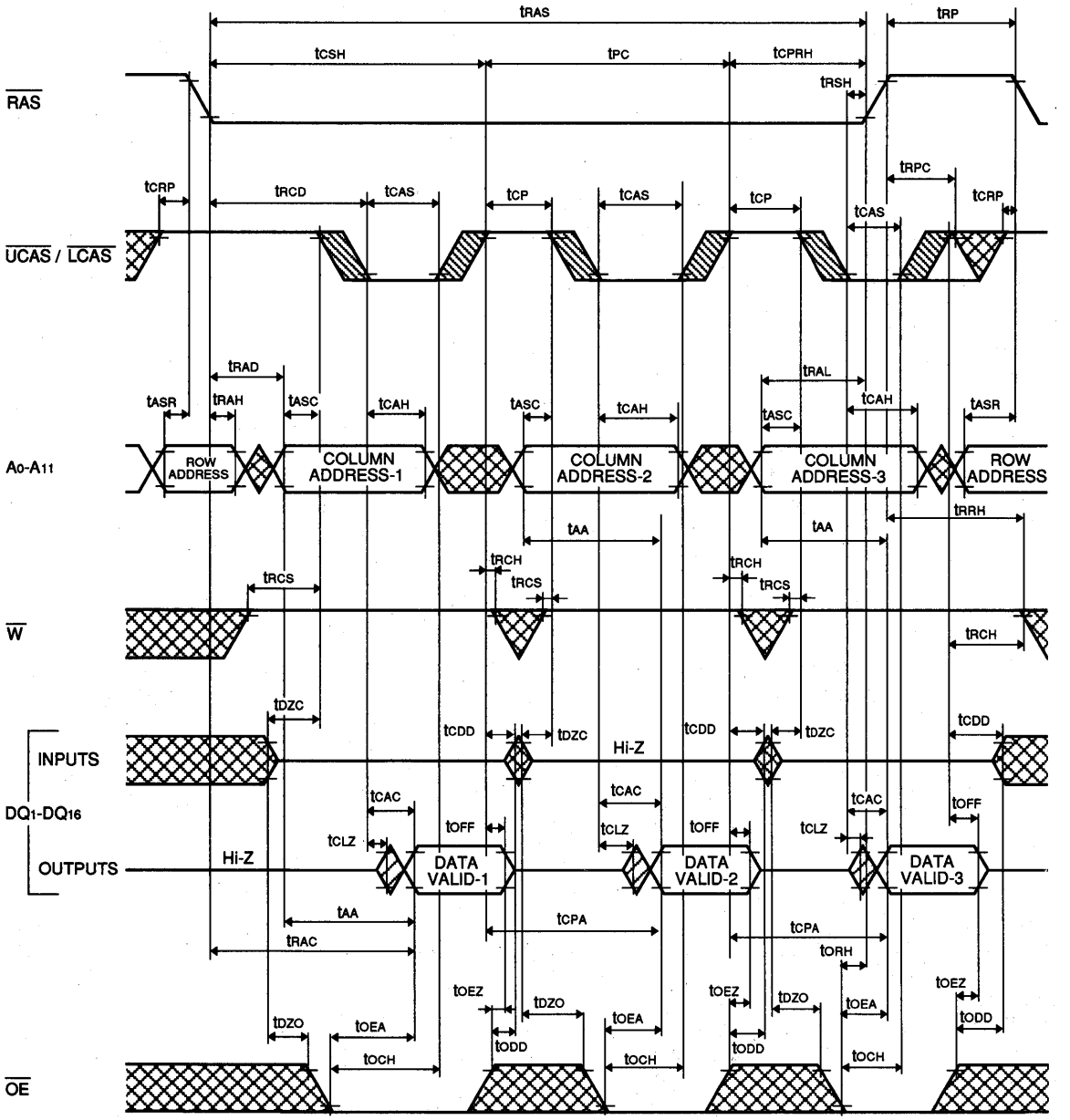


Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

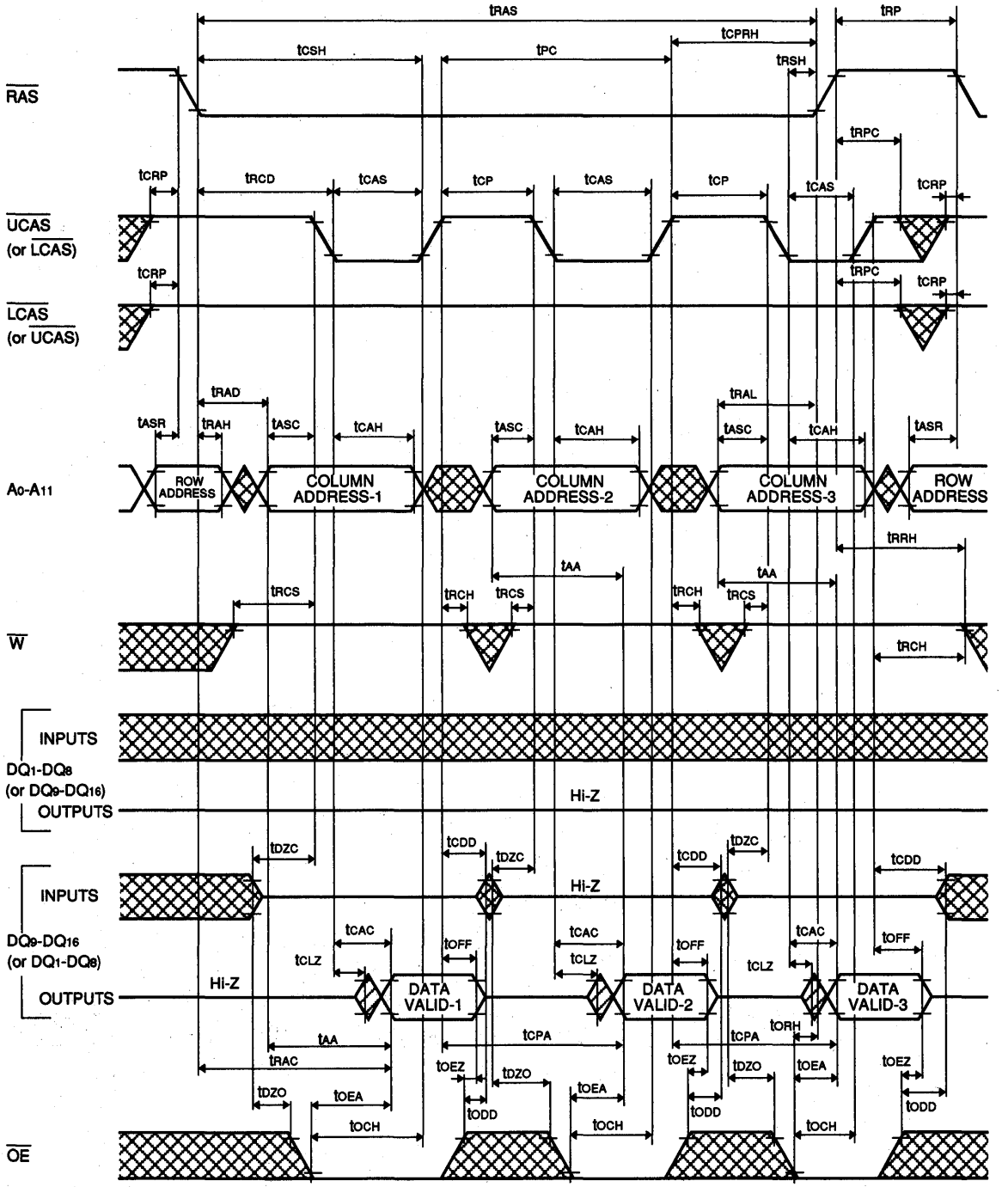
Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



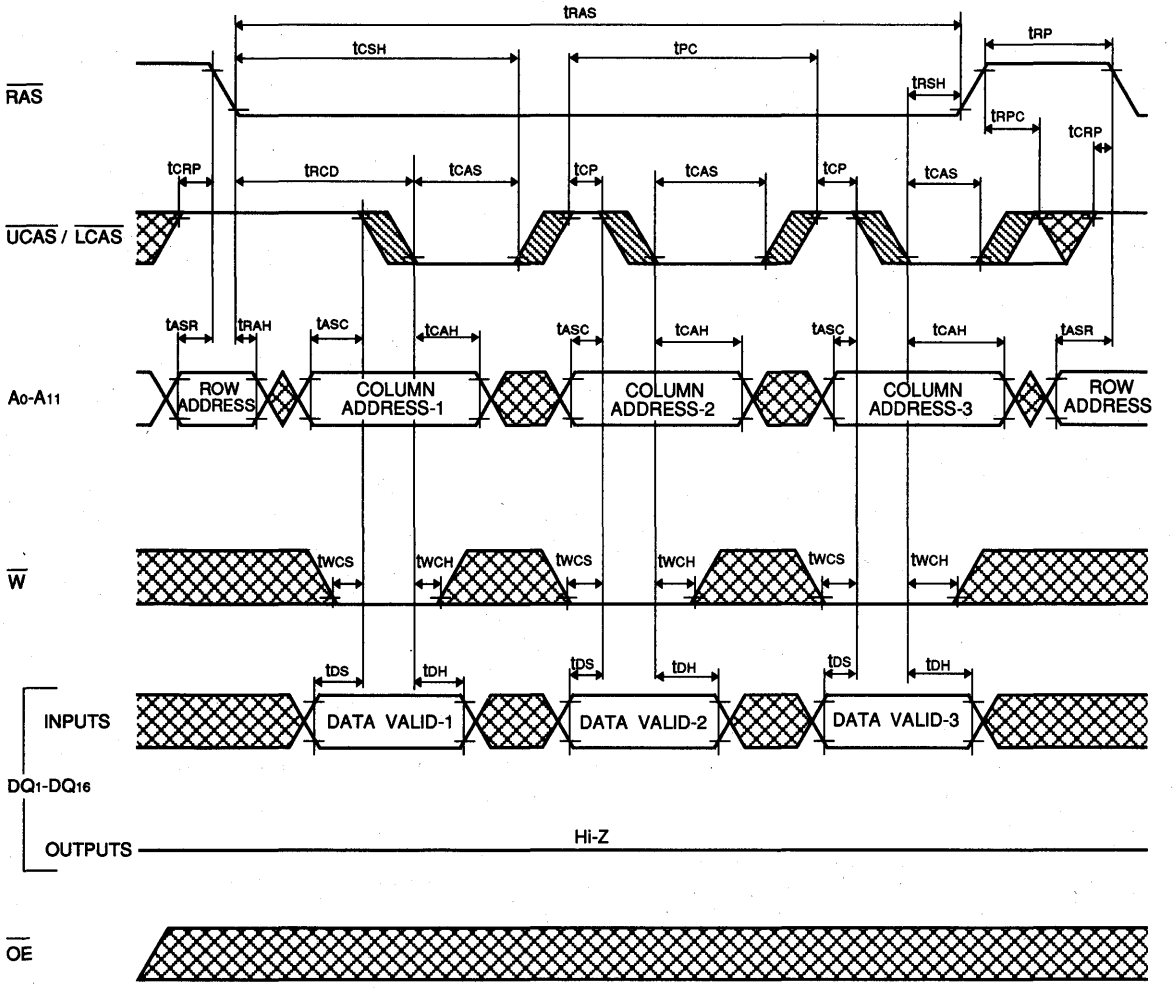
Fast Page Mode Read Cycle



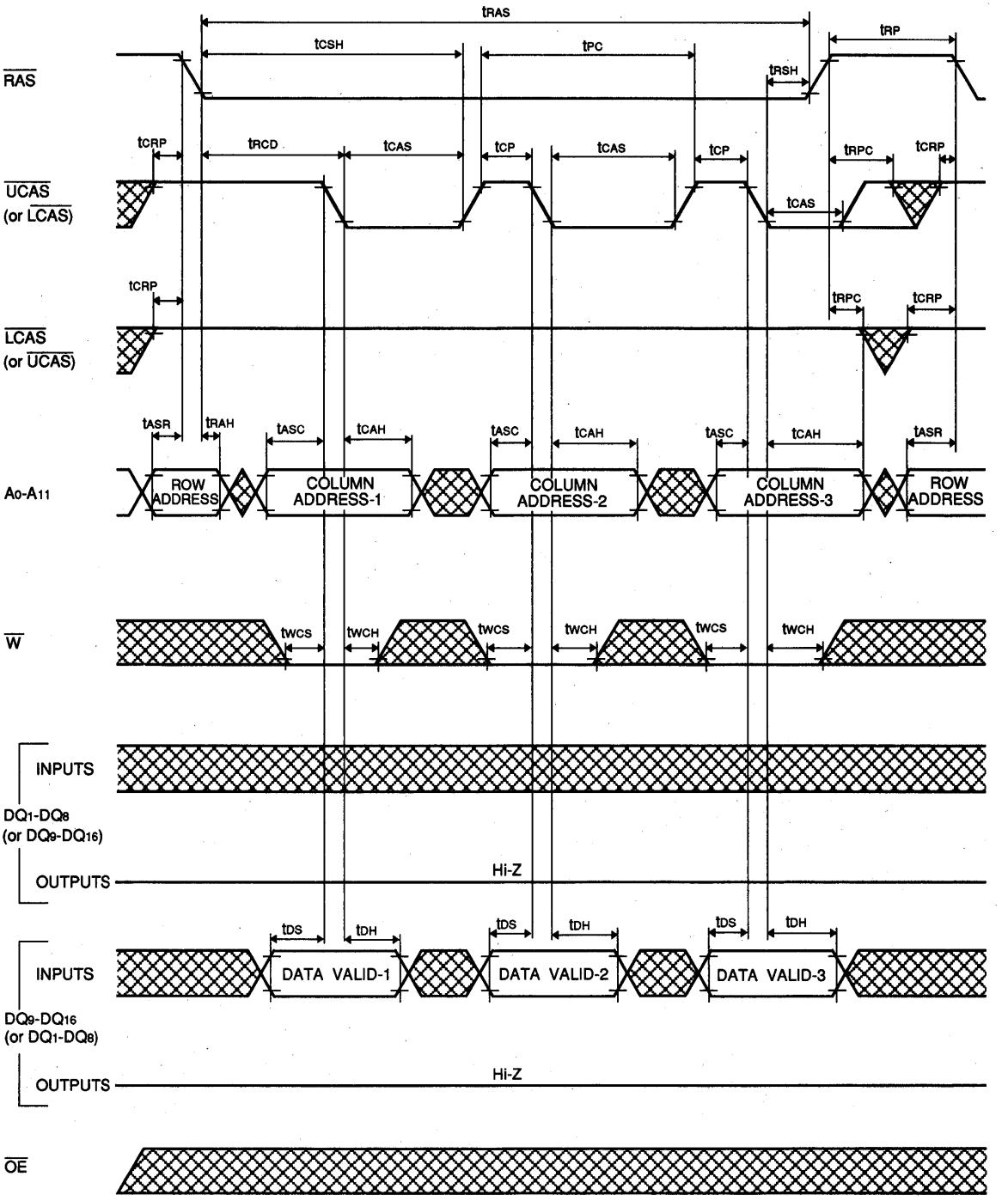
Upper/(Lower) Fast Page Mode Read Cycle



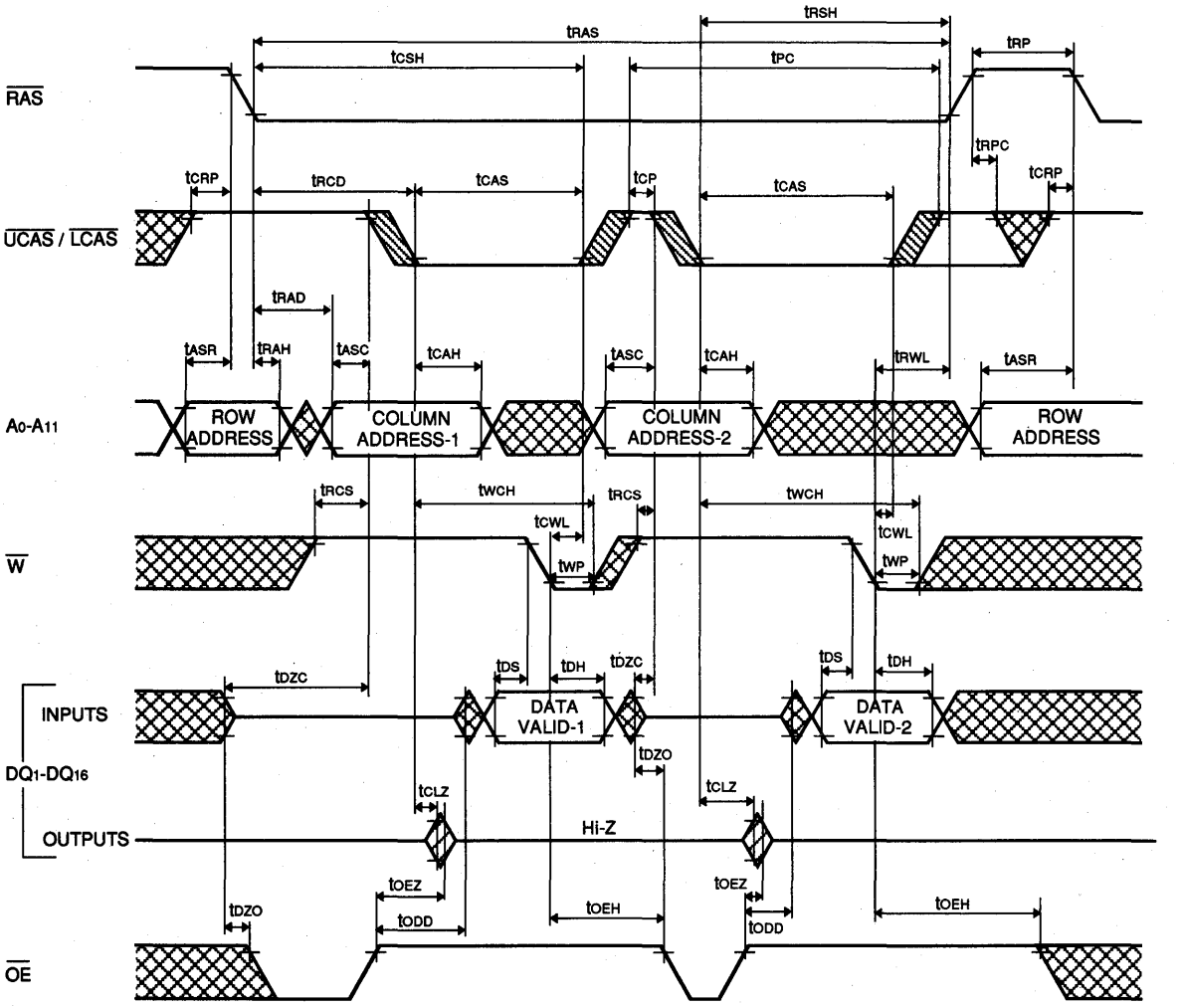
Fast Page Mode Write Cycle (Early Write)



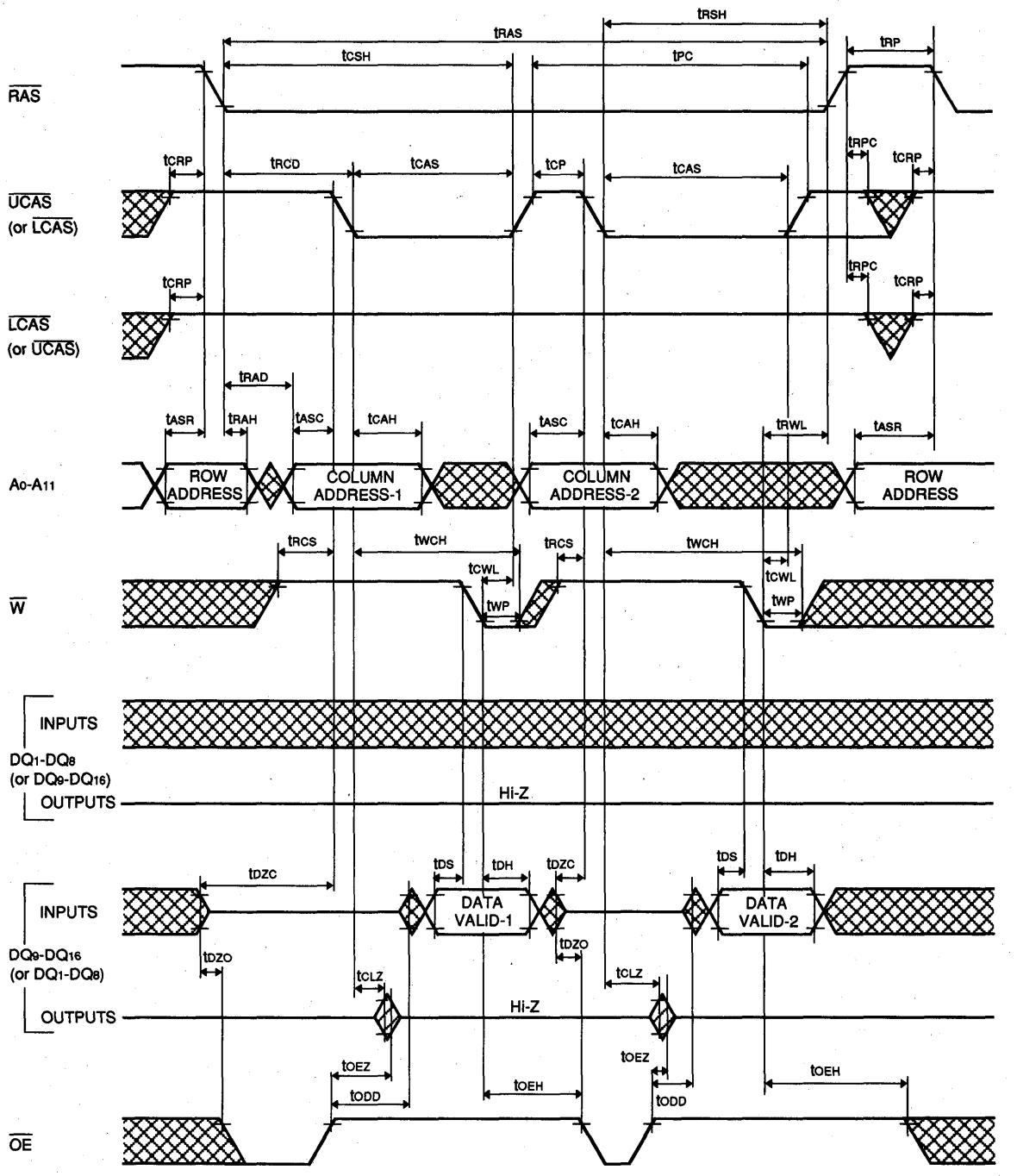
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



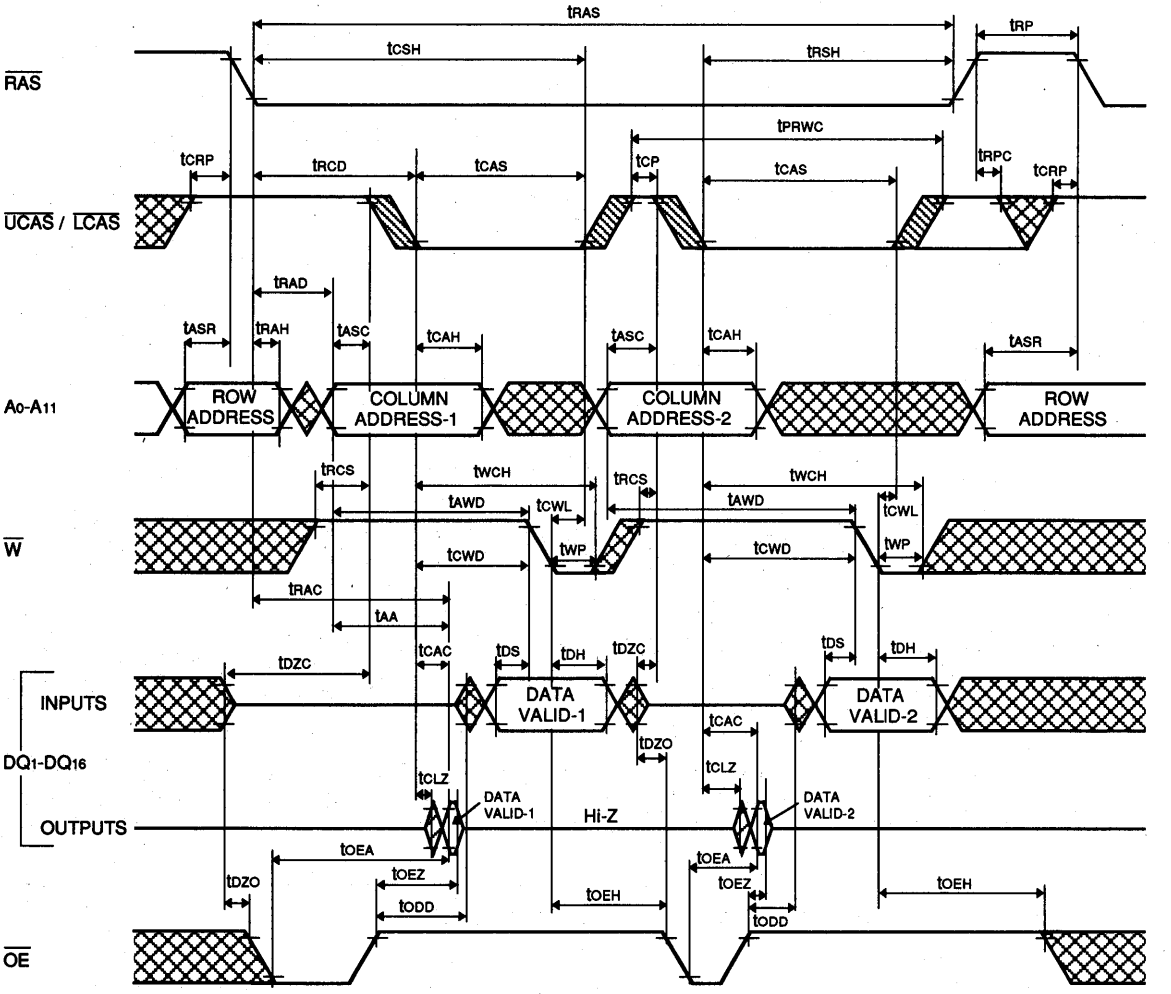
Fast Page Mode Write Cycle (Delayed Write)



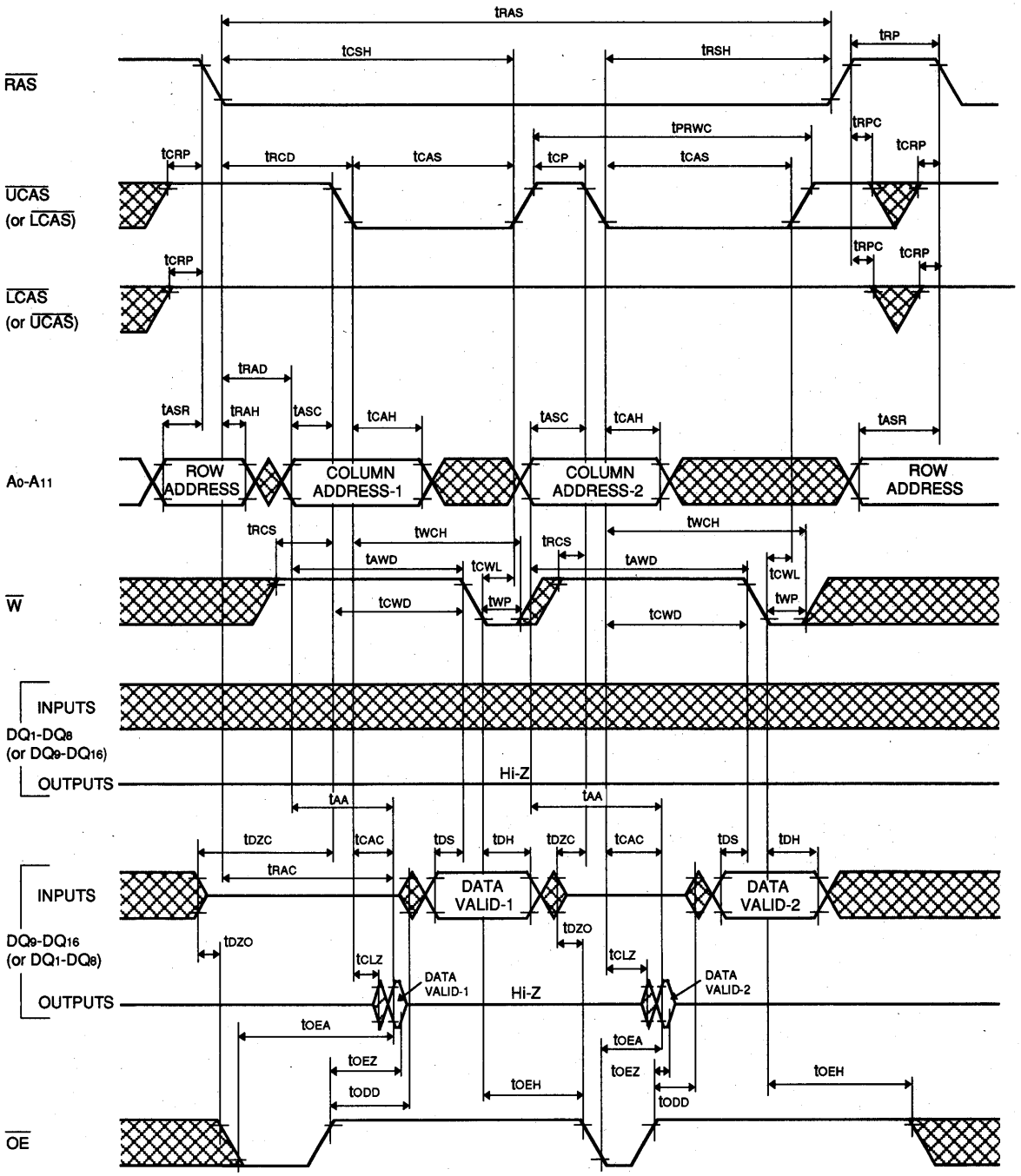
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8}	Supply current from Vcc Extended refresh cycle	M5M416160B -6S,-7S	$\overline{RAS}$ cycling $\overline{CAS} \leq 0.2V$ or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W} \leq 0.2V$ or $\geq Vcc - 0.2V$ $\overline{OE} \leq 0.2V$ or $\geq Vcc - 0.2V$ $A_0 \sim A_{11} \leq 0.2V$ or $\geq Vcc - 0.2V$ DQ = open t_{REF} = 128ms $t_{RAS} = t_{RAS}$ min～1 μs			600	μA
$I_{CC9\ (AV)}$	Average supply current from Vcc Self - Refresh cycle	M5M416160B -6S,-7S	$\overline{RAS} = \overline{CAS} \leq 0.2V$			400	μA

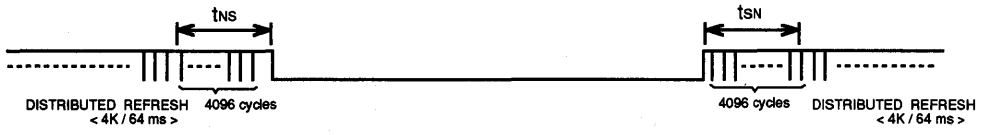
TIMING REQUIREMENTS (Ta=0～70°C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M416160B-6S		M5M416160B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

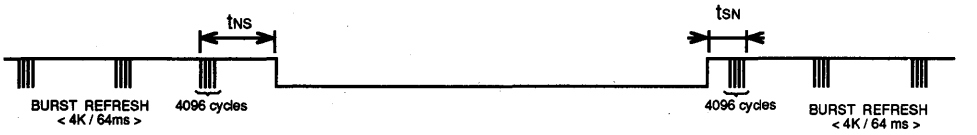
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leq$ 64 ms and $t_{SN} \leq$ 64 ms.

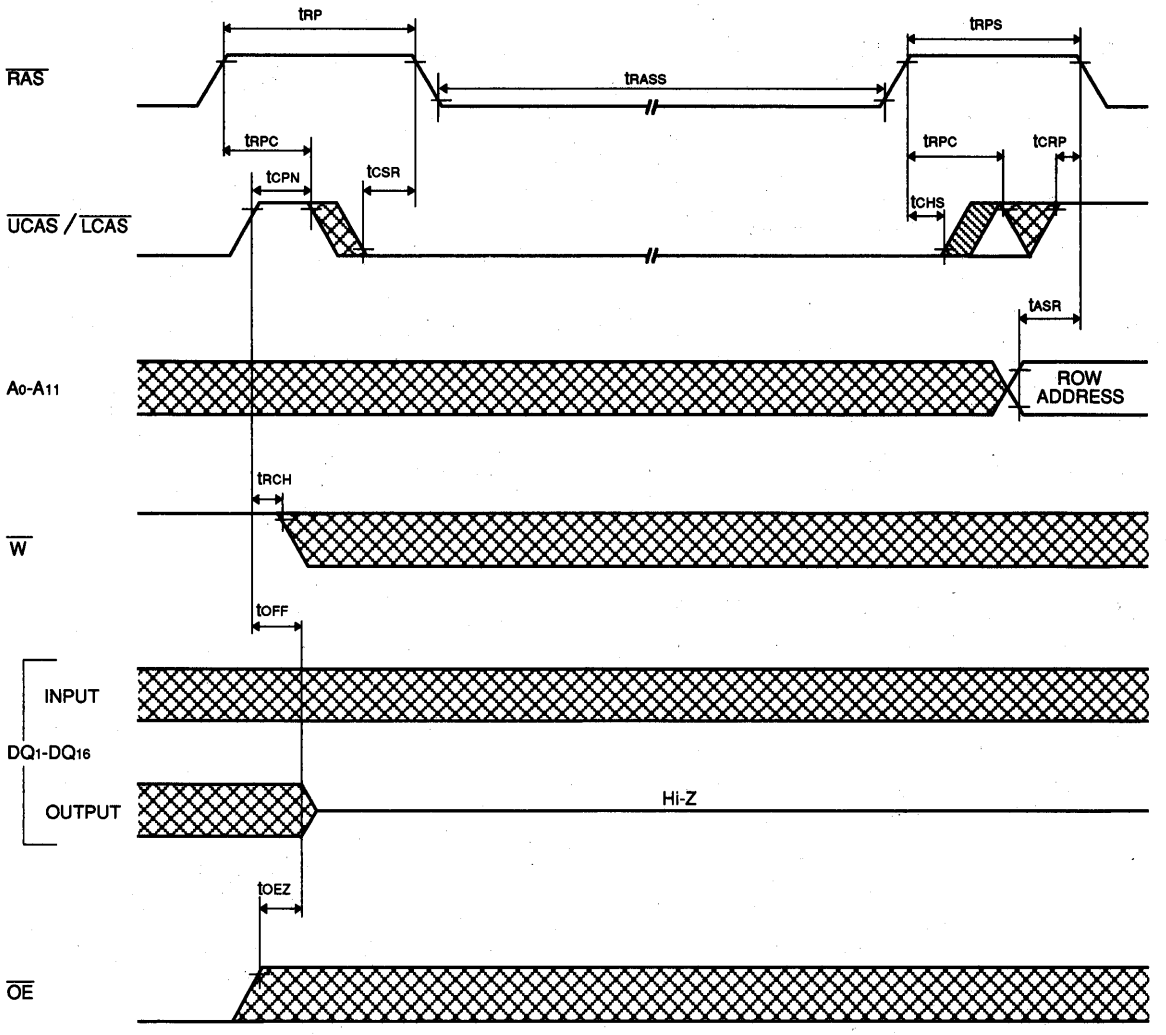


(2) In case of burst refresh

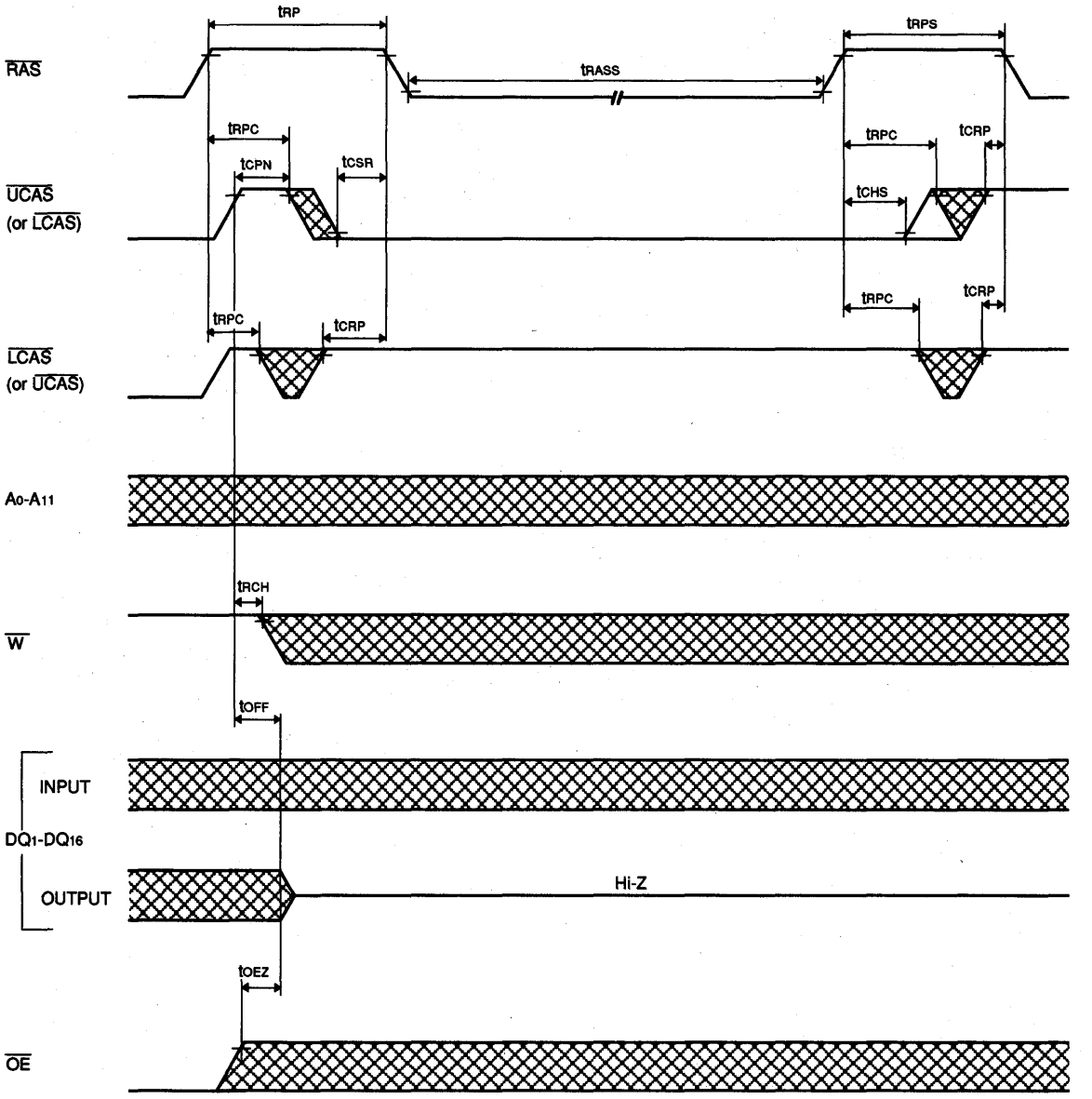
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} + t_{SN} \leq$ 64 ms.



Self Refresh Cycle



Upper/(Lower) Self Refresh Cycle*



M5M418160BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418160BXX-6,-6S	60	15	30	15	110	680
M5M418160BXX-7,-7S	70	20	35	20	130	590

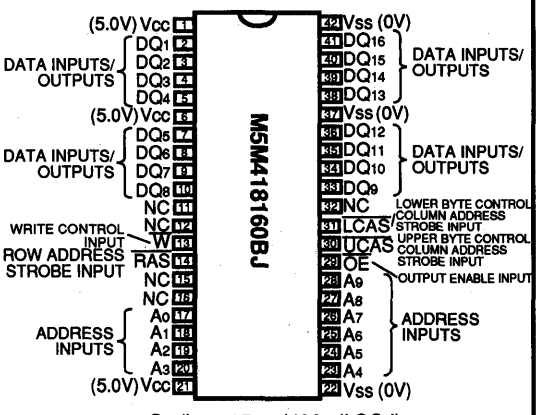
XX=J,TP

- Standard 42pin SOJ, 50pin TSOP
- Single 5.0V ± 10% supply
- Low stand-by power dissipation
  5.5mW (Max) ..... CMOS Input level
- Low operating power dissipation
  M5M418160Bxx -6, -6S ..... 940.0mW (Max)
  M5M418160Bxx -7, -7S ..... 830.0mW (Max)
- Fast-page mode, Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)

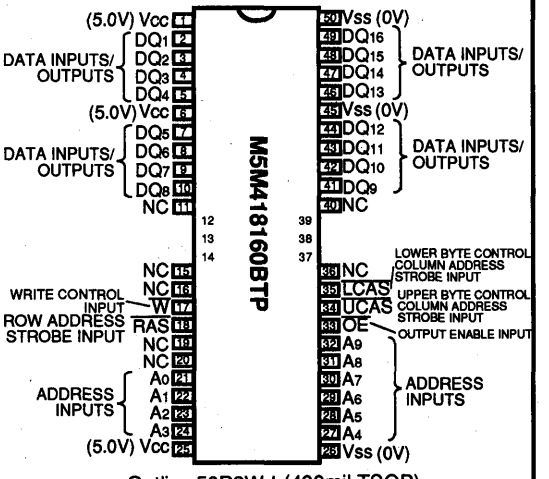
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 42P0K(400mil SOJ)



Outline 50P3W-L(400mil TSOP)

NC : NO CONNECTION

FUNCTION

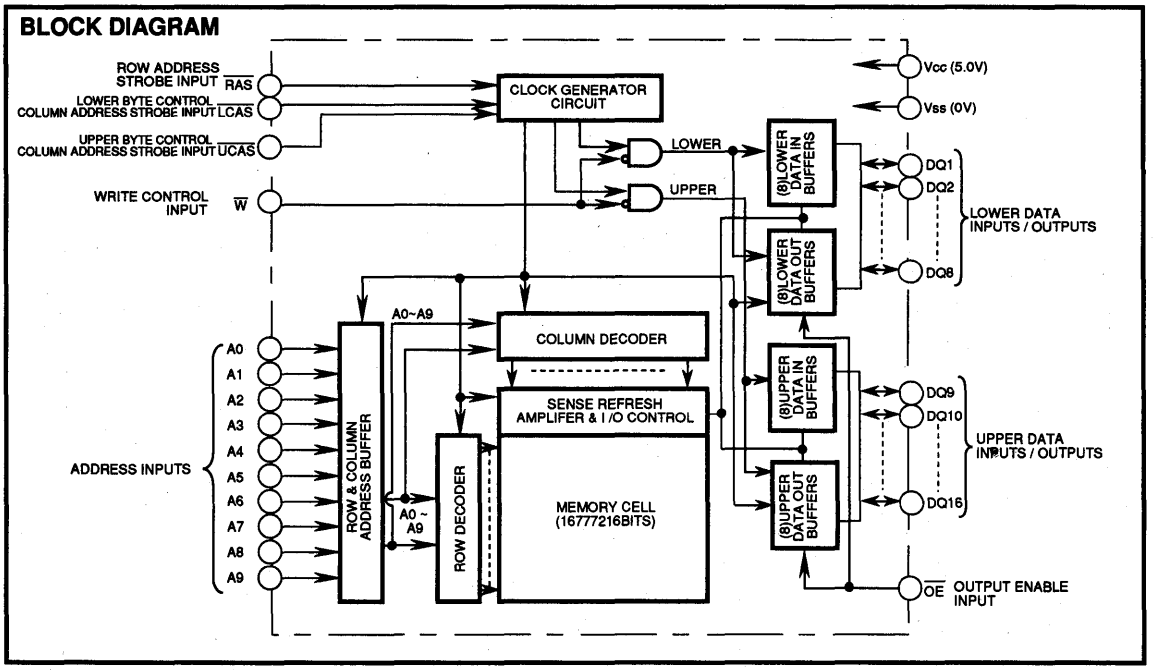
The M5M418160BJ,TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
Vo	Output voltage		-1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M418160B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			170	mA
		M5M418160B-7,-7S				150	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M418160B-6,-7	$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V, output open			1	
		M5M418160B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V, output open			0.3	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M418160B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			170	mA
		M5M418160B-7,-7S				150	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M418160B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			85	mA
		M5M418160B-7,-7S				75	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418160B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			170	mA
		M5M418160B-7,-7S				150	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

CAPACITANCE (Ta=0～70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, $\overline{W}$ input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0～70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note7,8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note7,9)		60		70	ns
tAA	Column address access time	(Note 7,10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 100pF, V_{OH}=2.4V(I_{OH}=-5mA) and V_{OL}=0.4V(I_{OL}=4.2mA).
8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq \pm 10\ \mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		16.4		16.4	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note19)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note19)	15		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T=5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note22)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note23)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note23)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M418160B-6,-6S		M5M418160B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note25)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note23)	60		65		ns

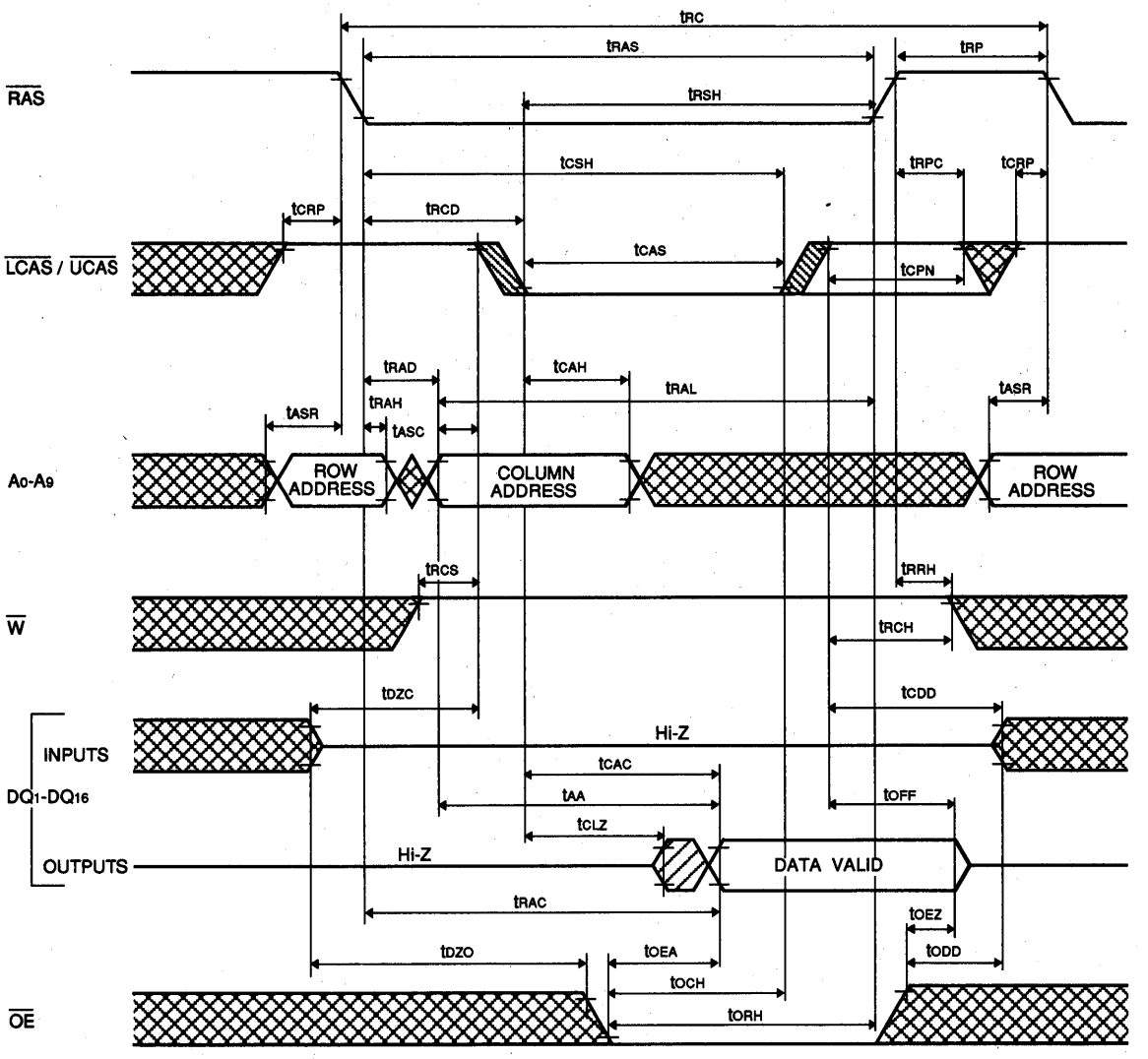
Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



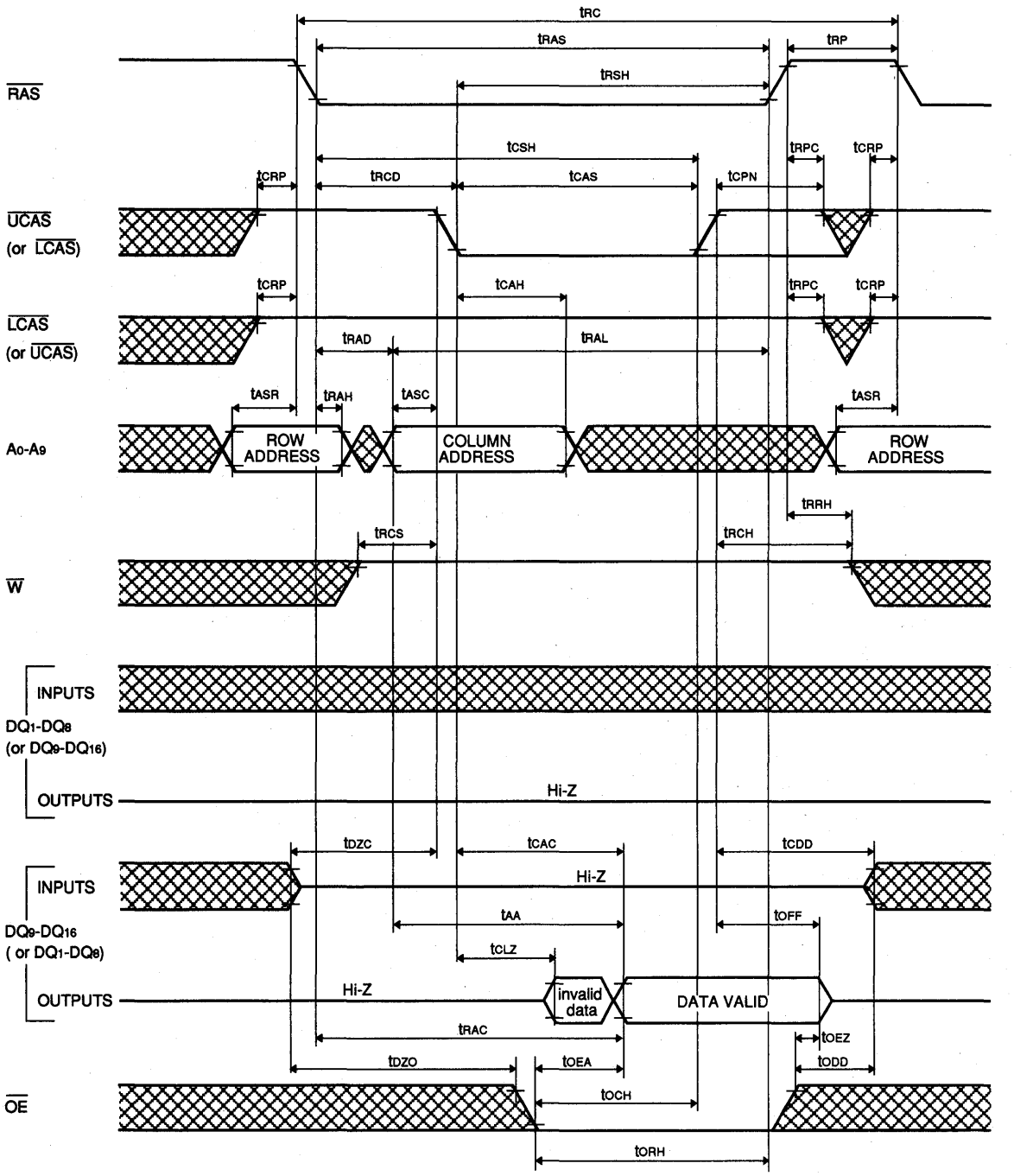
Note 28

Indicates the don't care input.
$V_{IH}(min.) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min.) \leq V_{IN} \leq V_{IL}(max)$

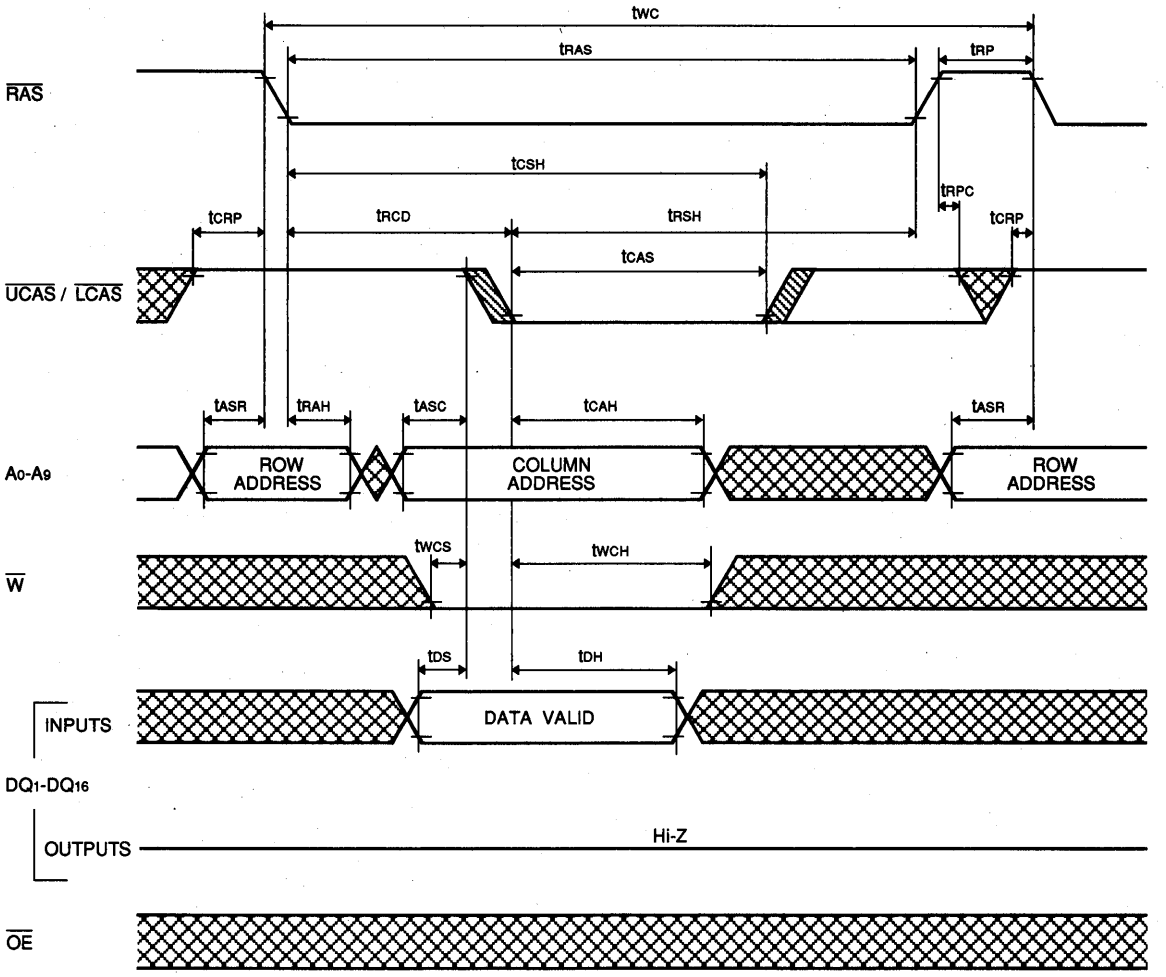
Indicates the invalid output.

Indicates the skew of the two inputs.

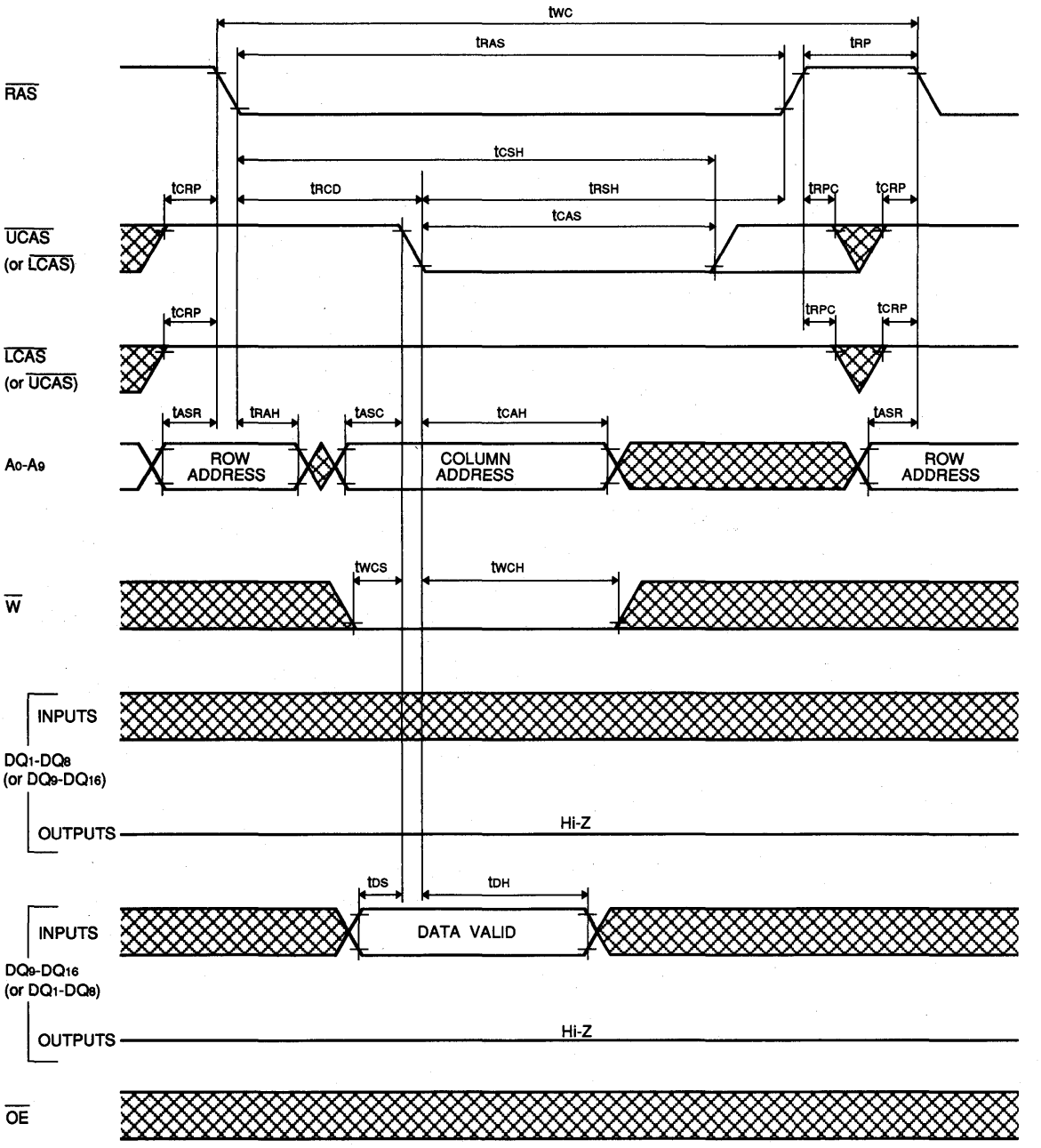
Upper / (Lower) Byte Read Cycle



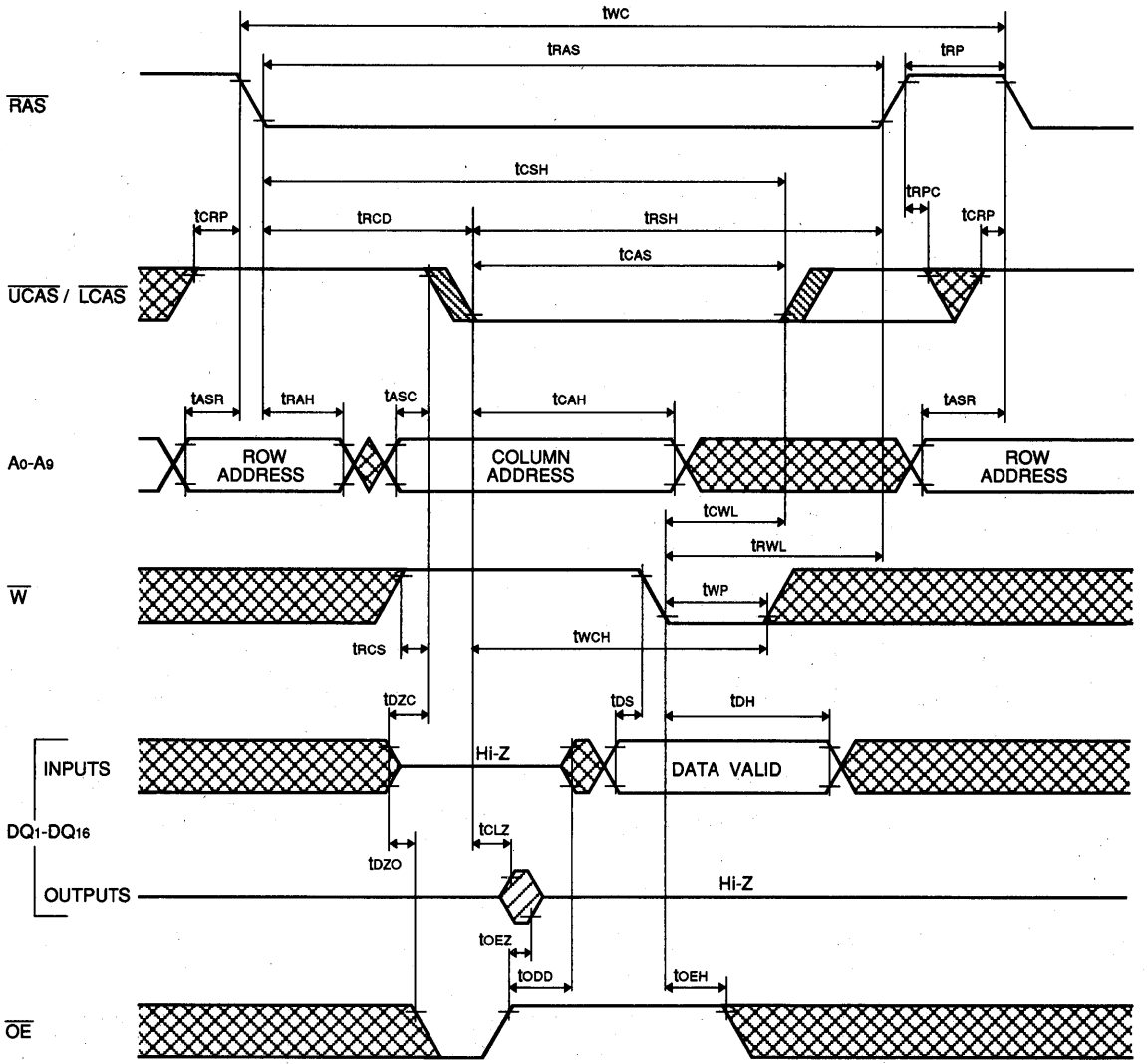
Write Cycle (Early write)



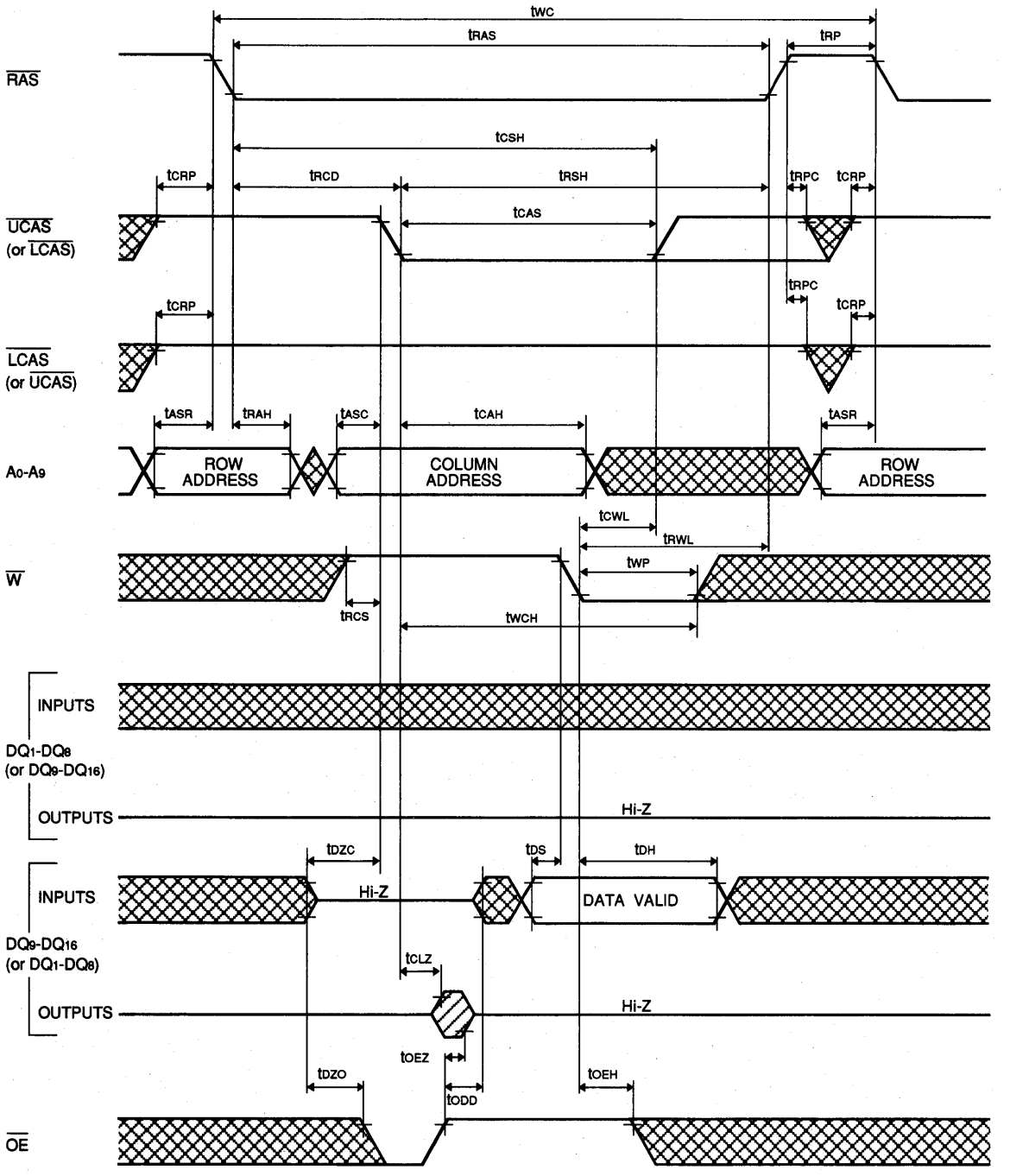
Upper/(Lower) Byte Write Cycle (Early write)



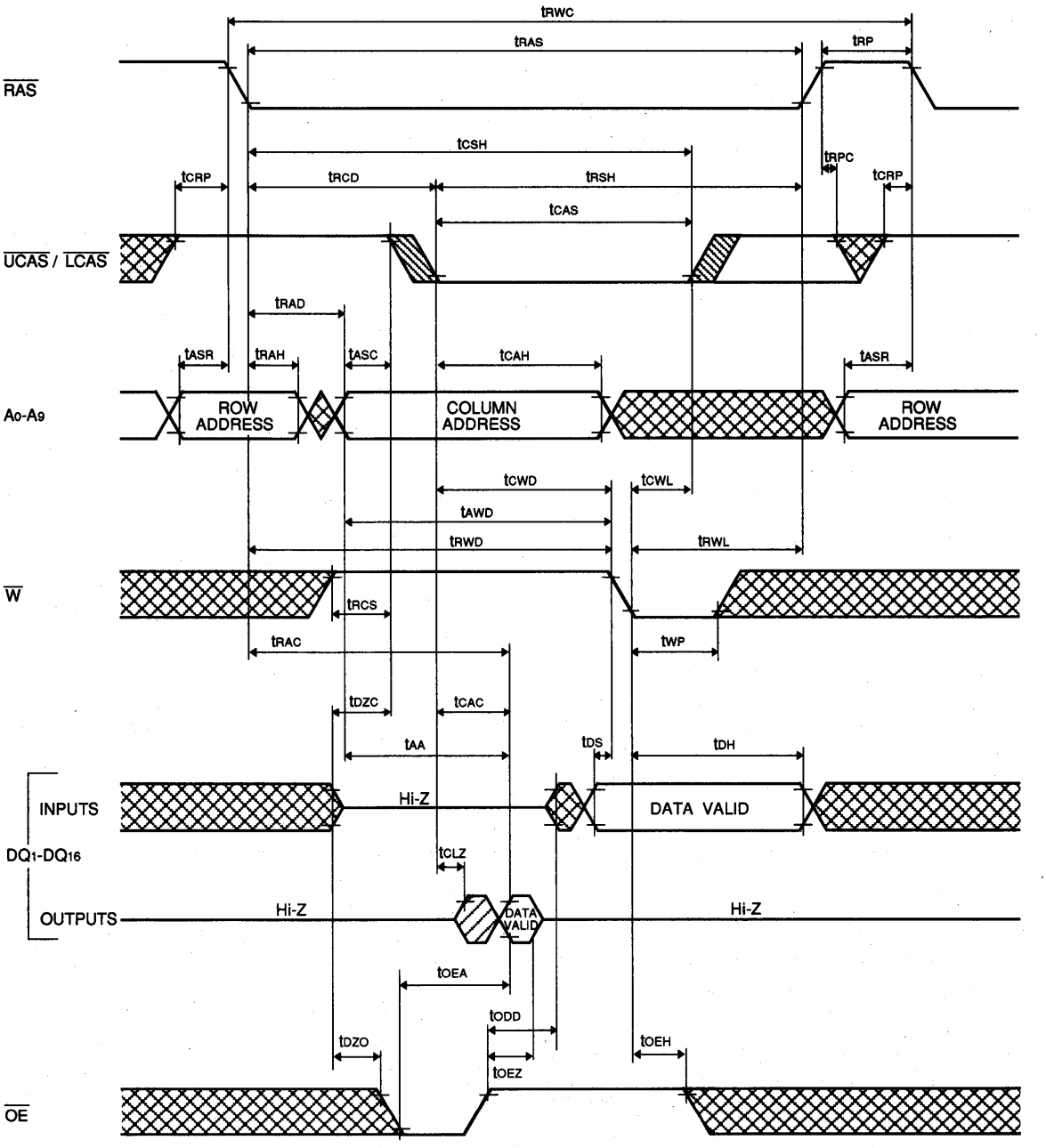
Write Cycle (Delayed write)



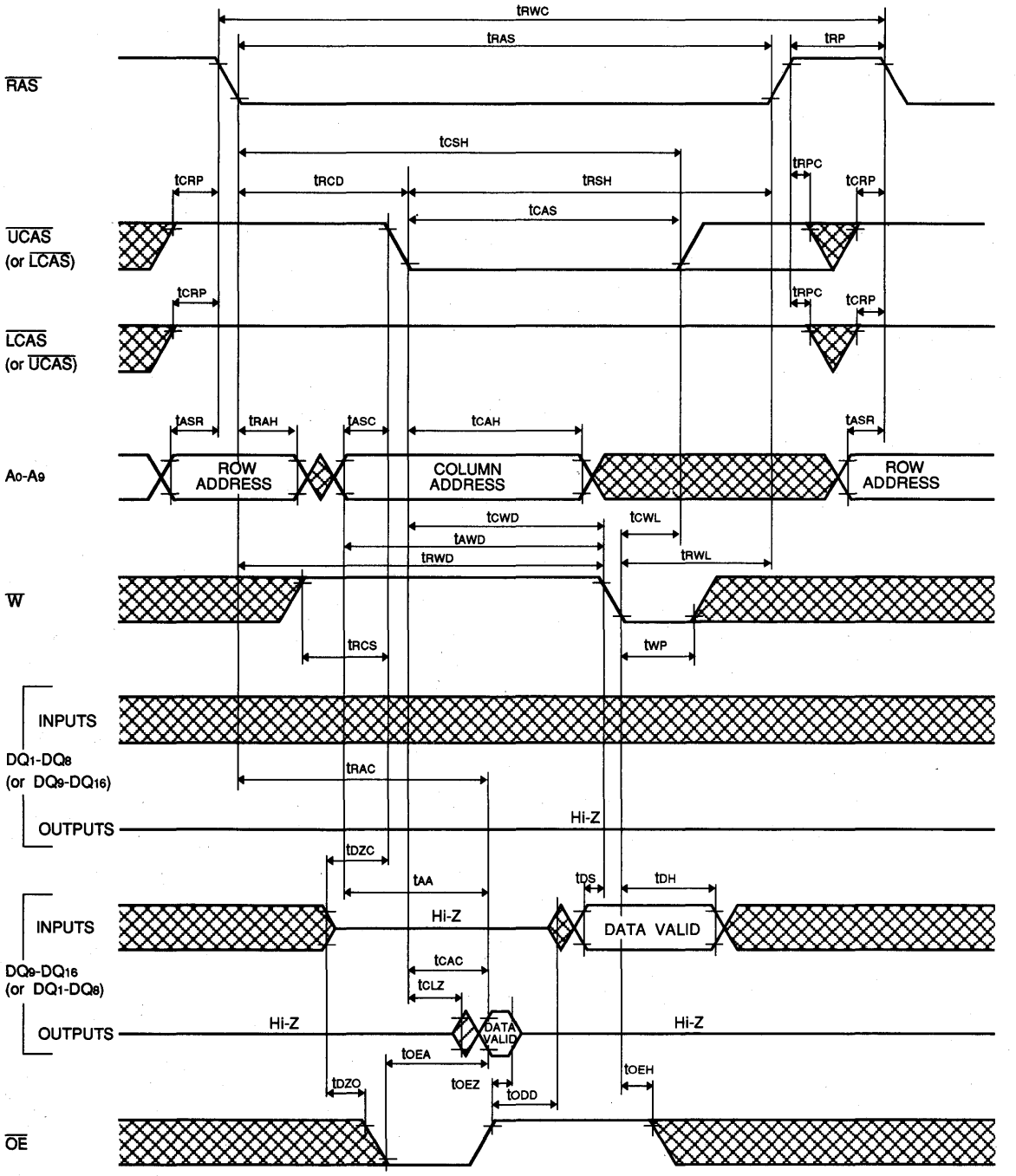
Upper/(Lower) Byte Write Cycle (Delayed write)



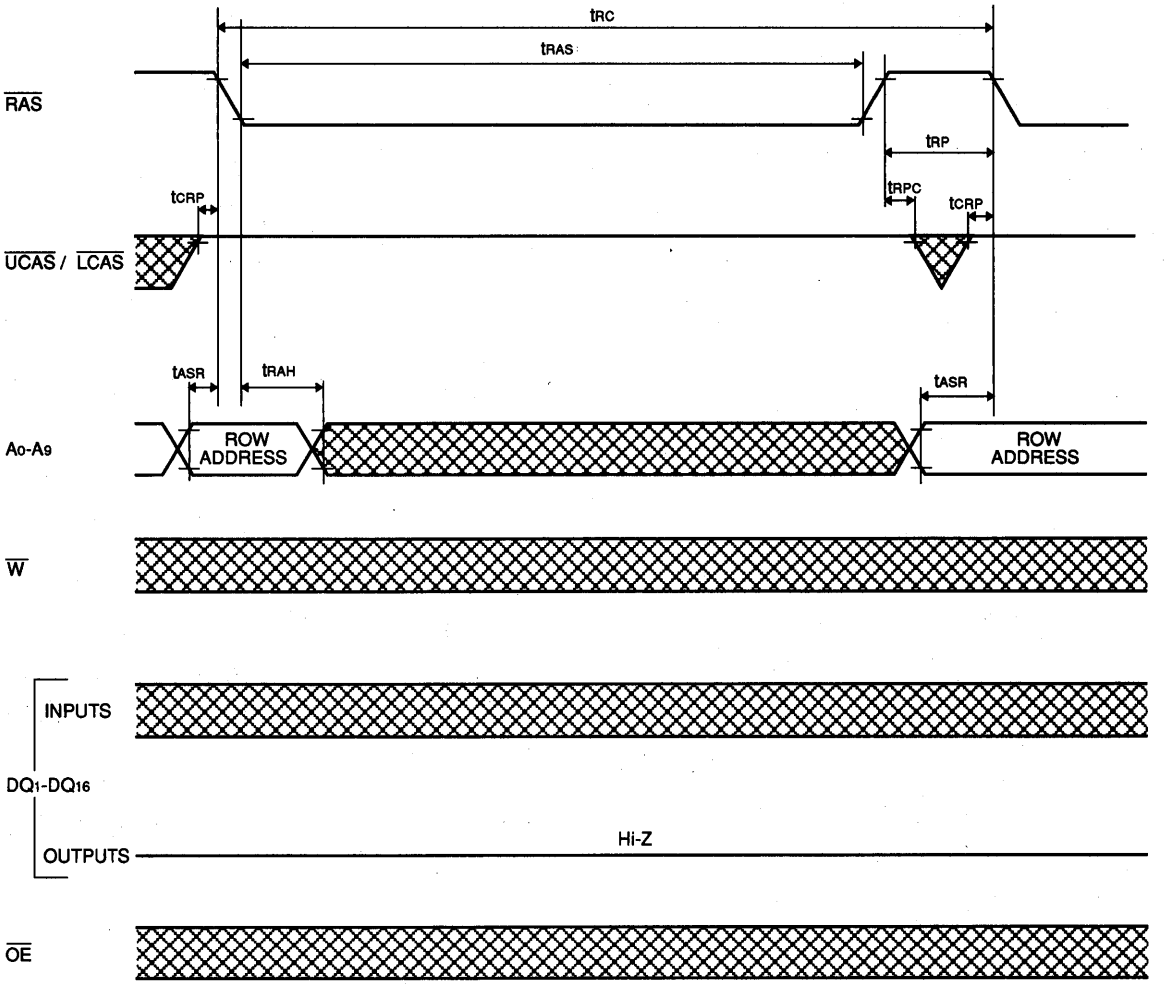
Read-Write, Read-Modify-Write Cycle



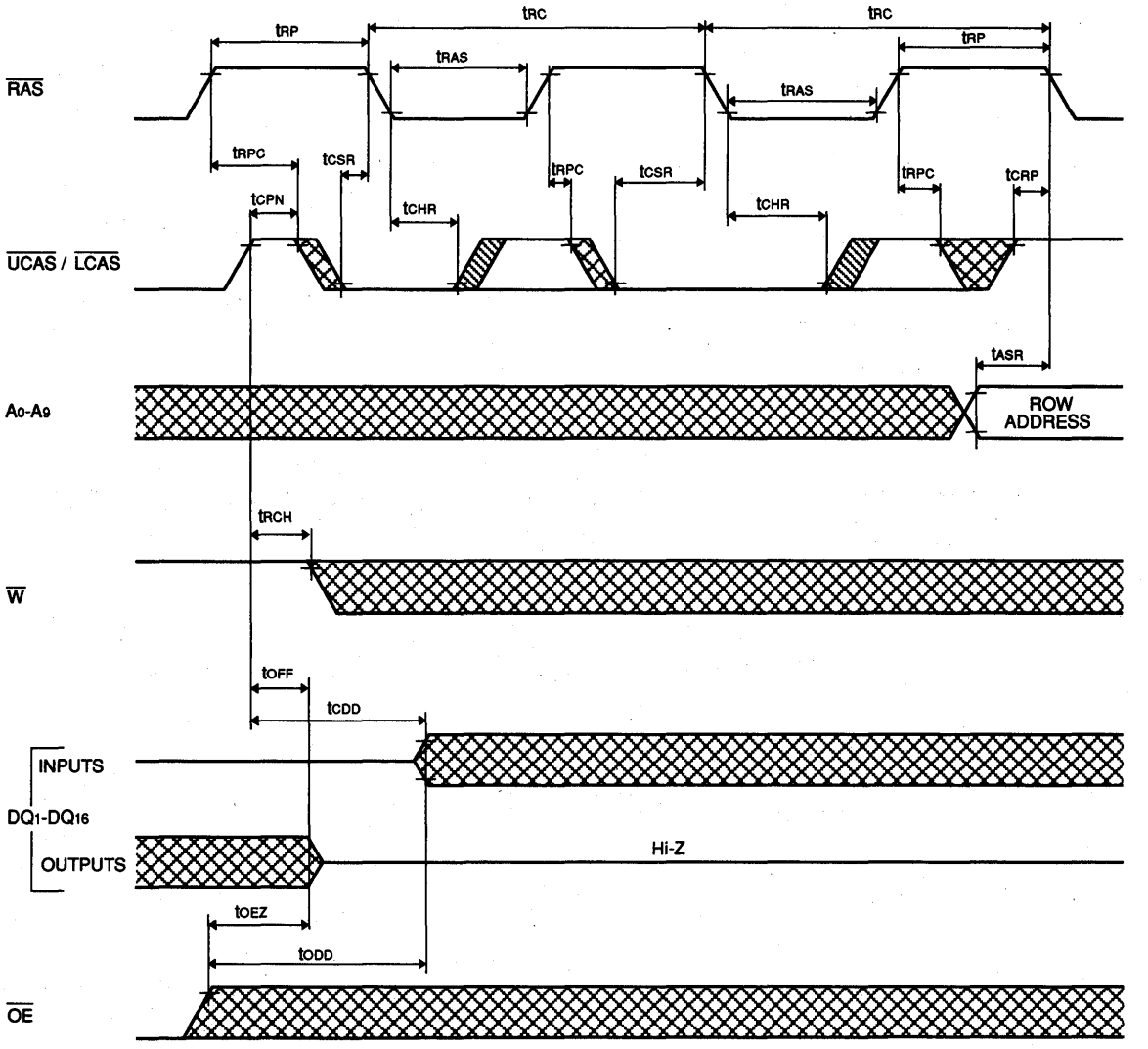
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



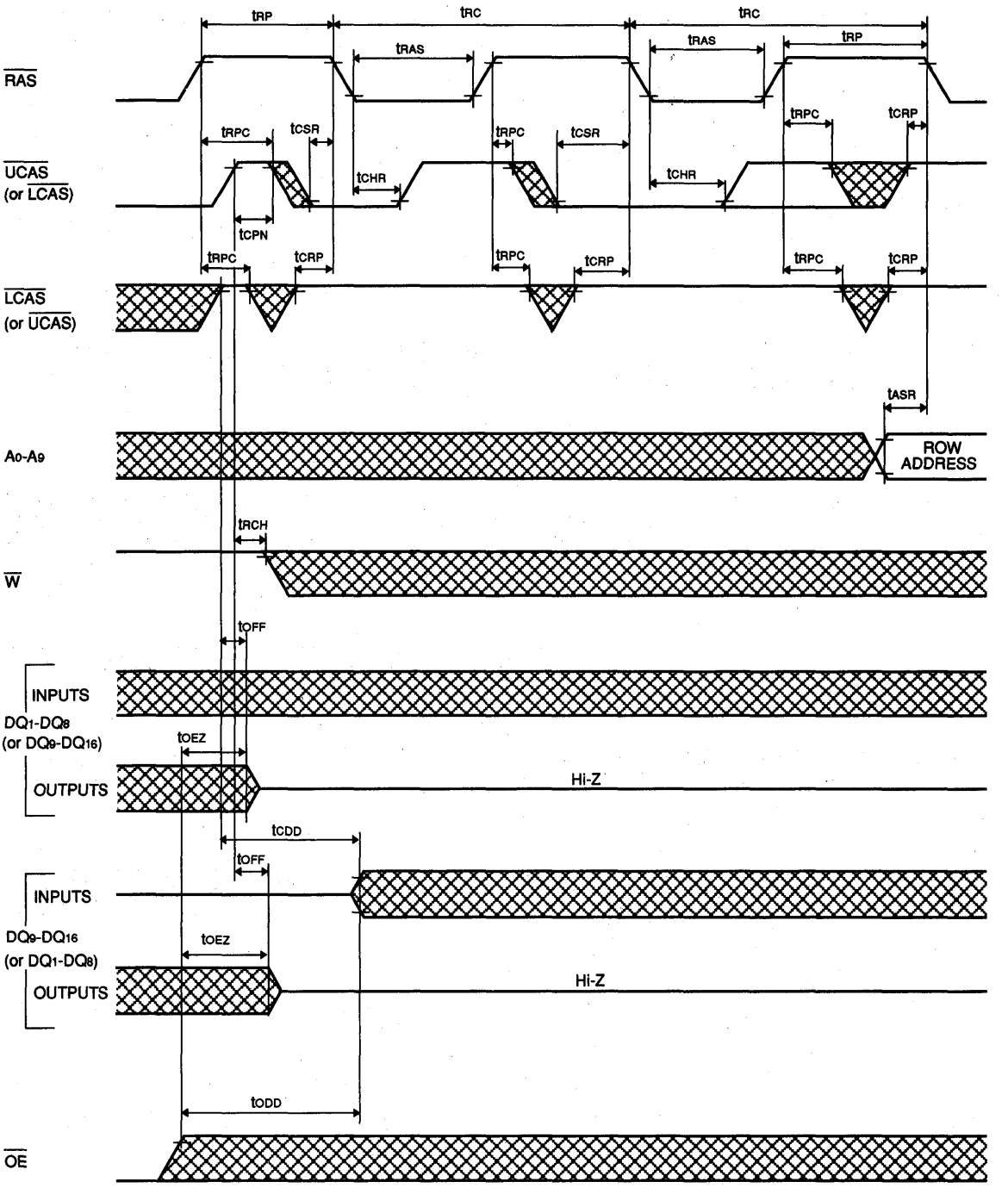
$\overline{\text{RAS}}$-only Refresh Cycle



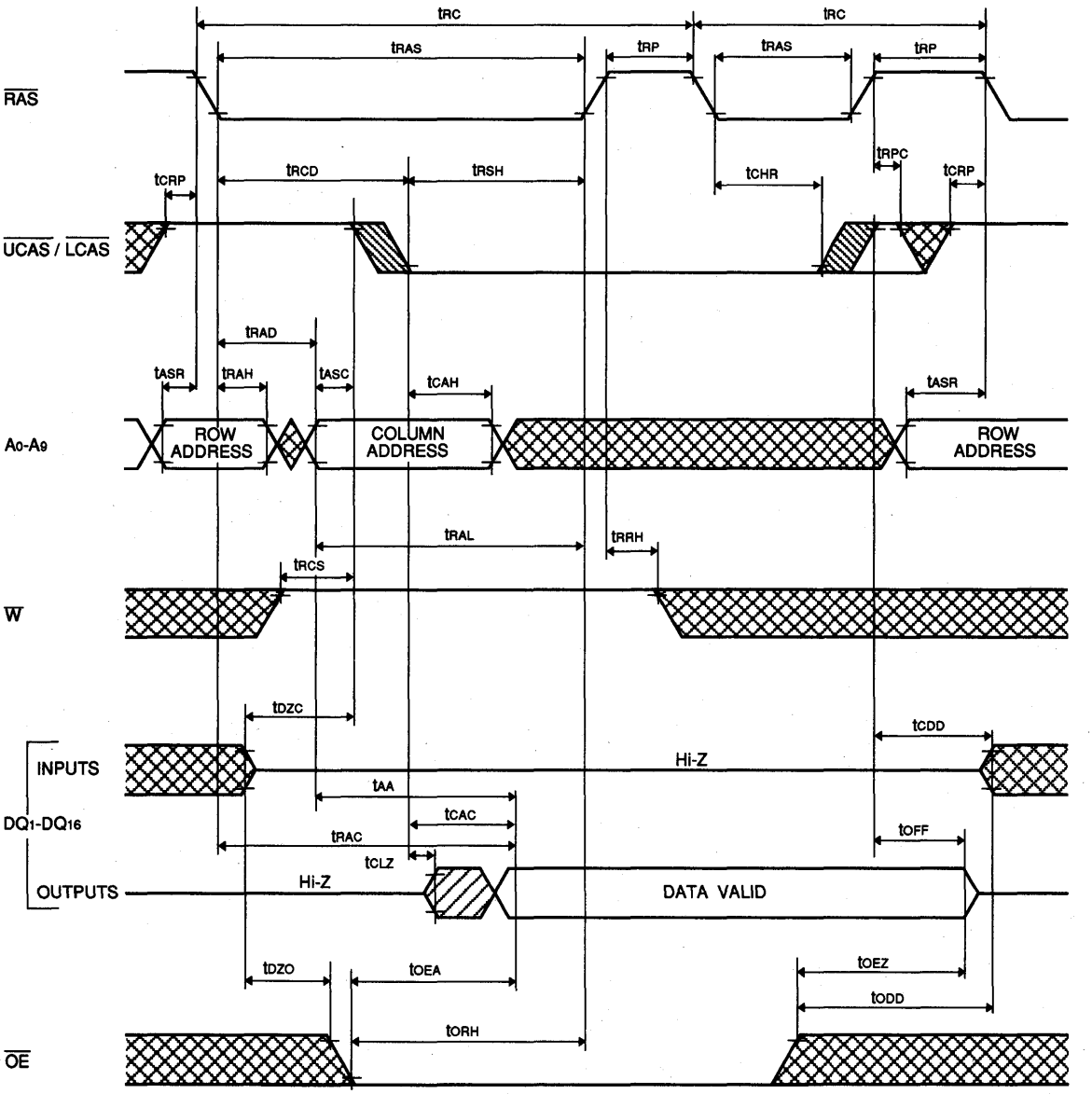
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

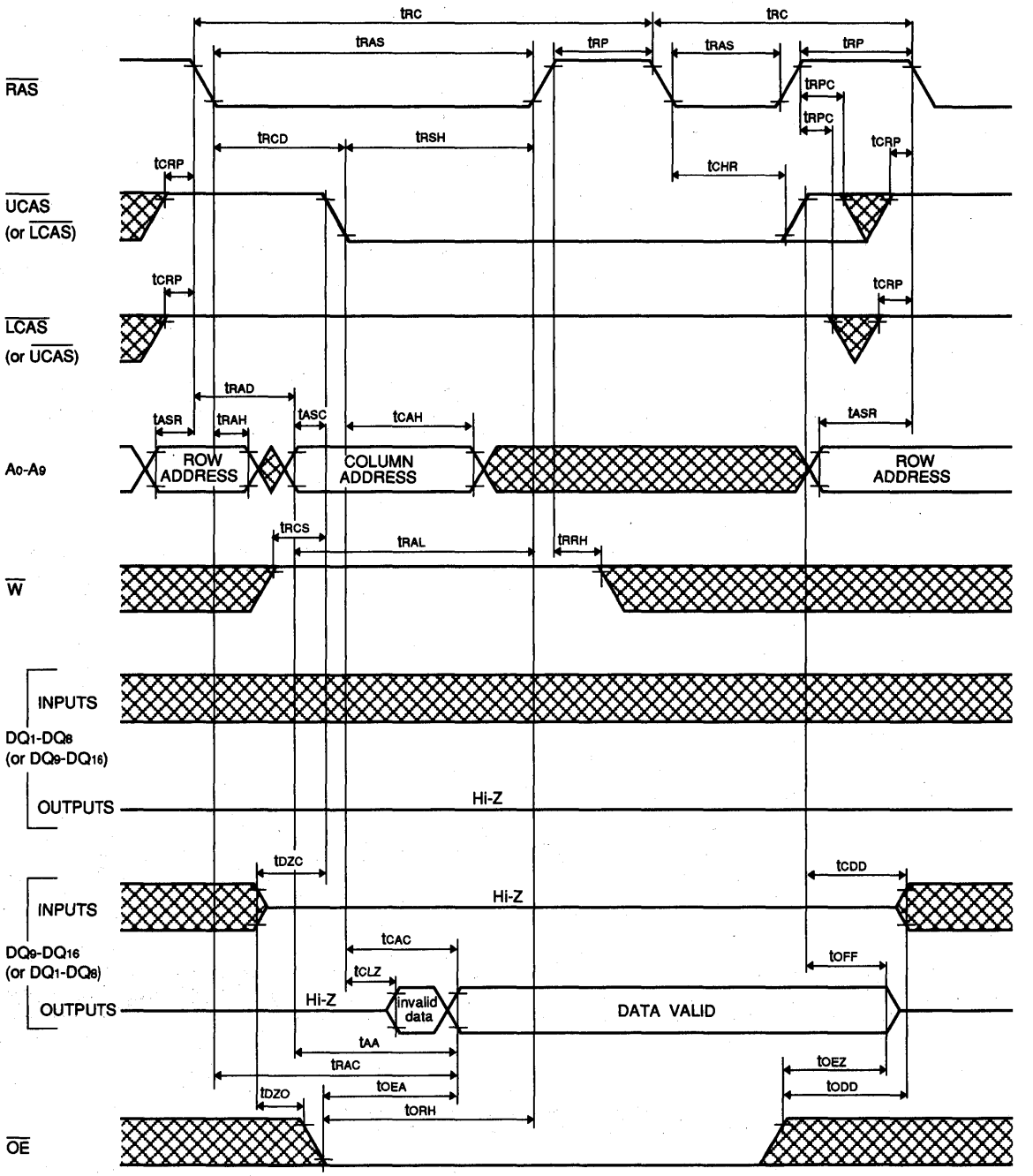


Hidden Refresh Cycle (Read) (Note 29)

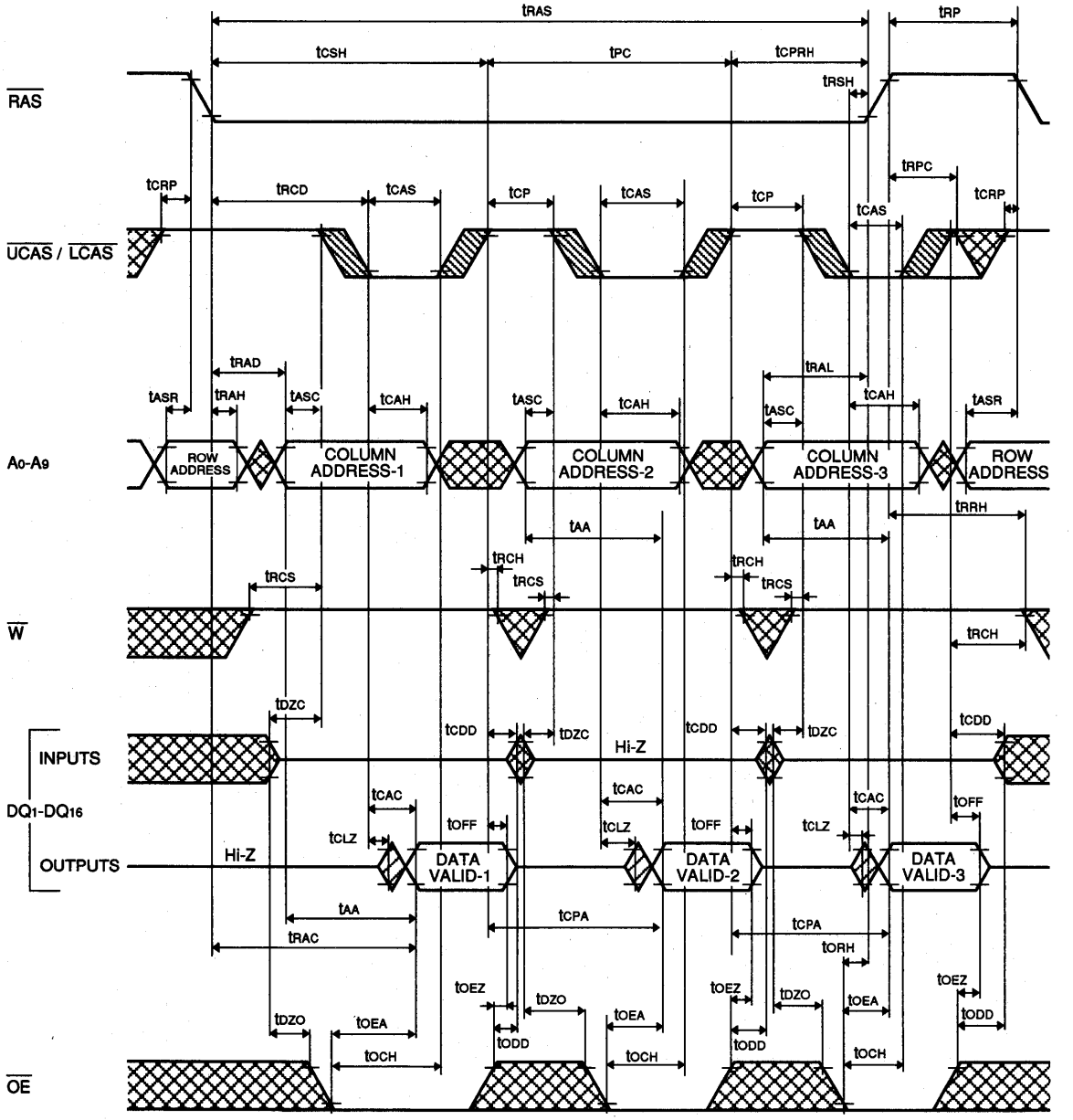


Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

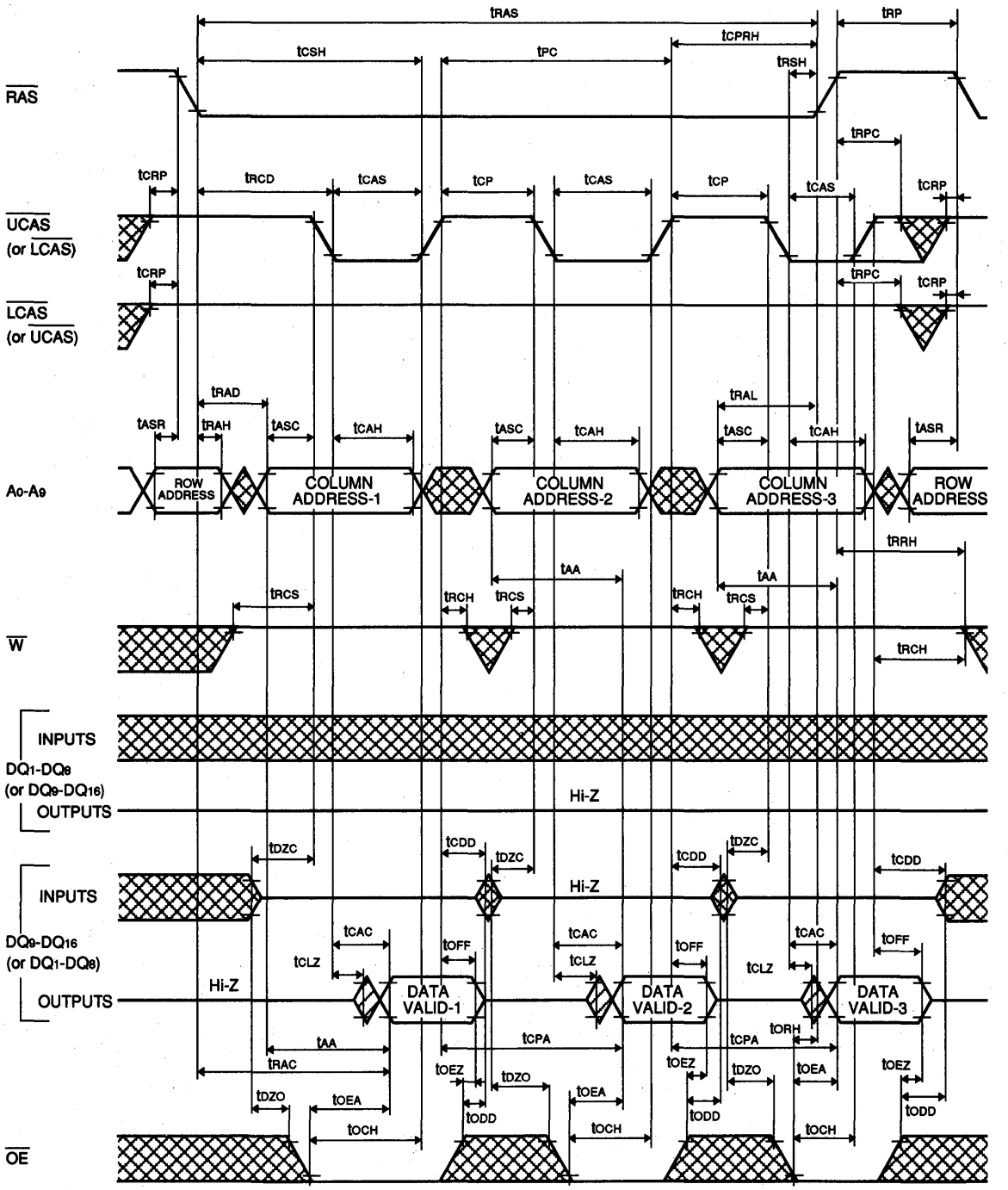
Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



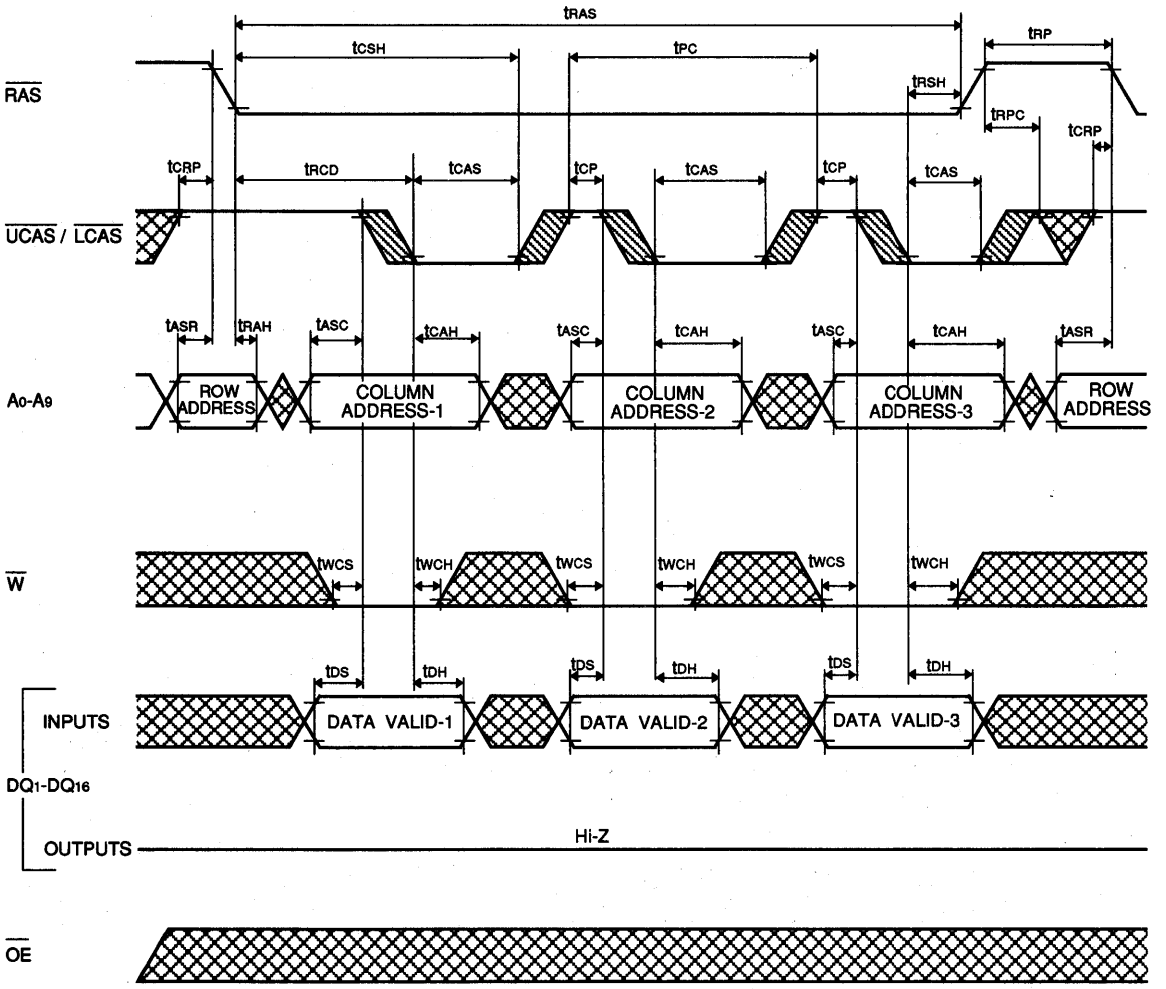
Fast Page Mode Read Cycle



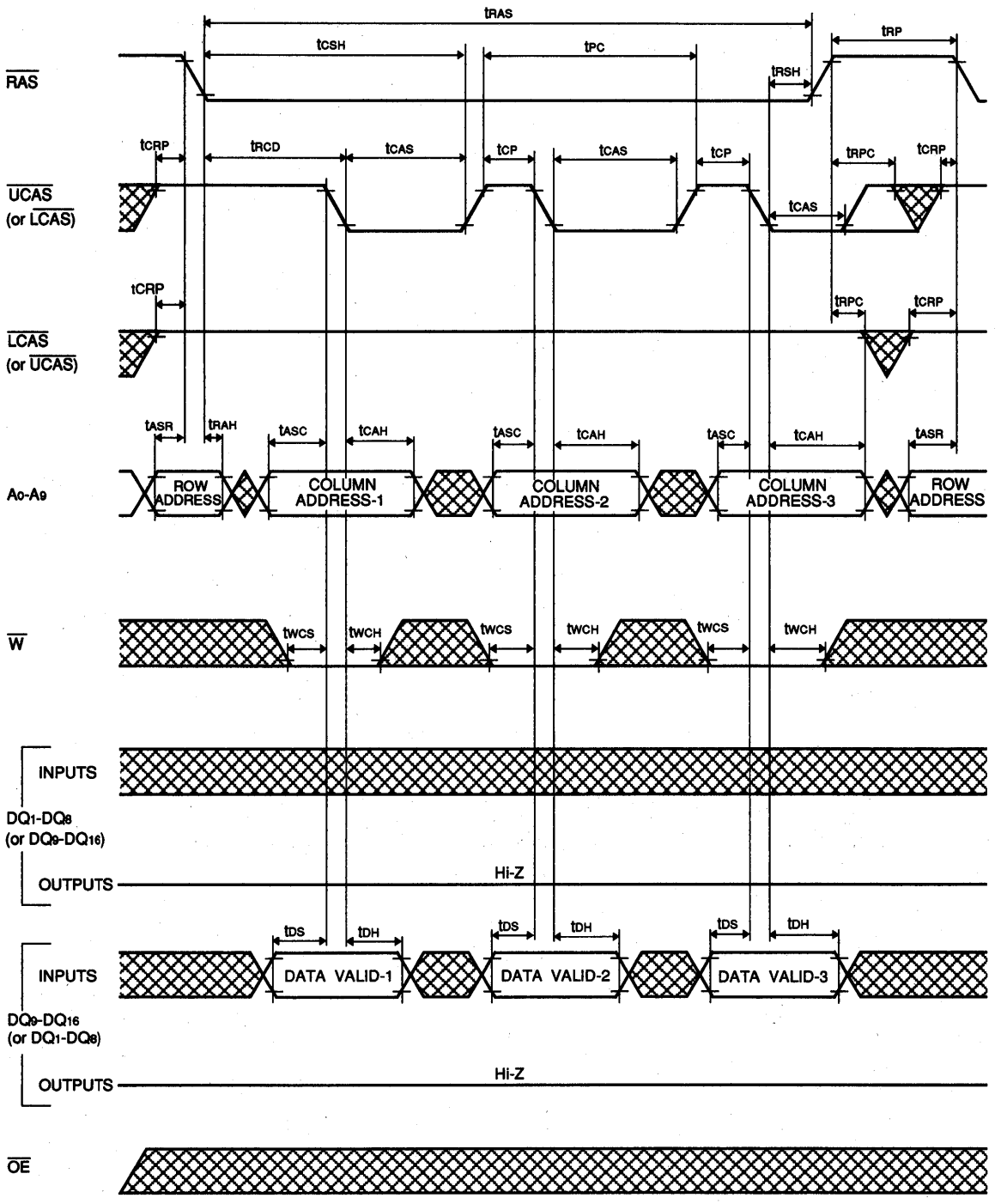
Upper/(Lower) Fast Page Mode Read Cycle



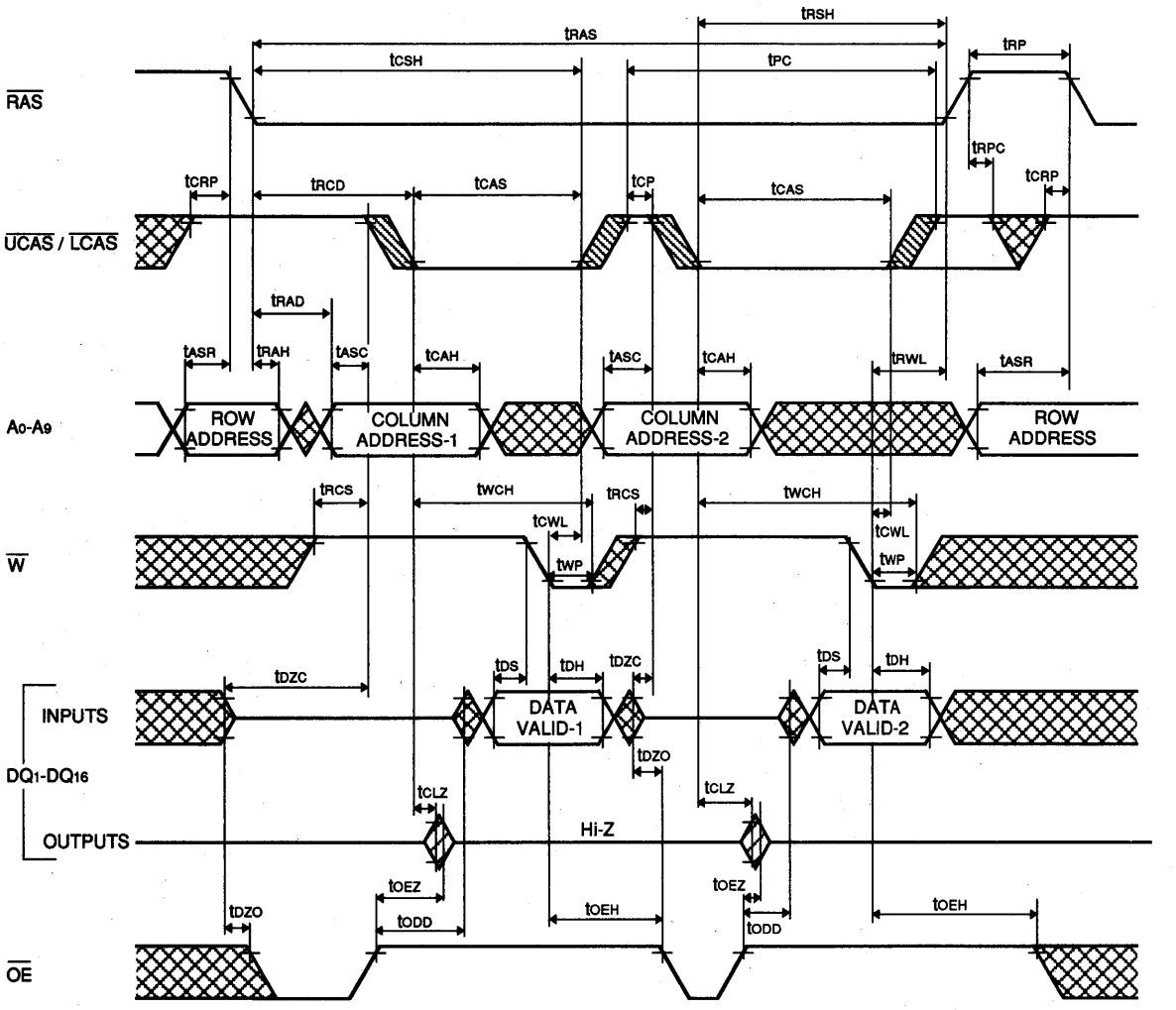
Fast Page Mode Write Cycle (Early Write)



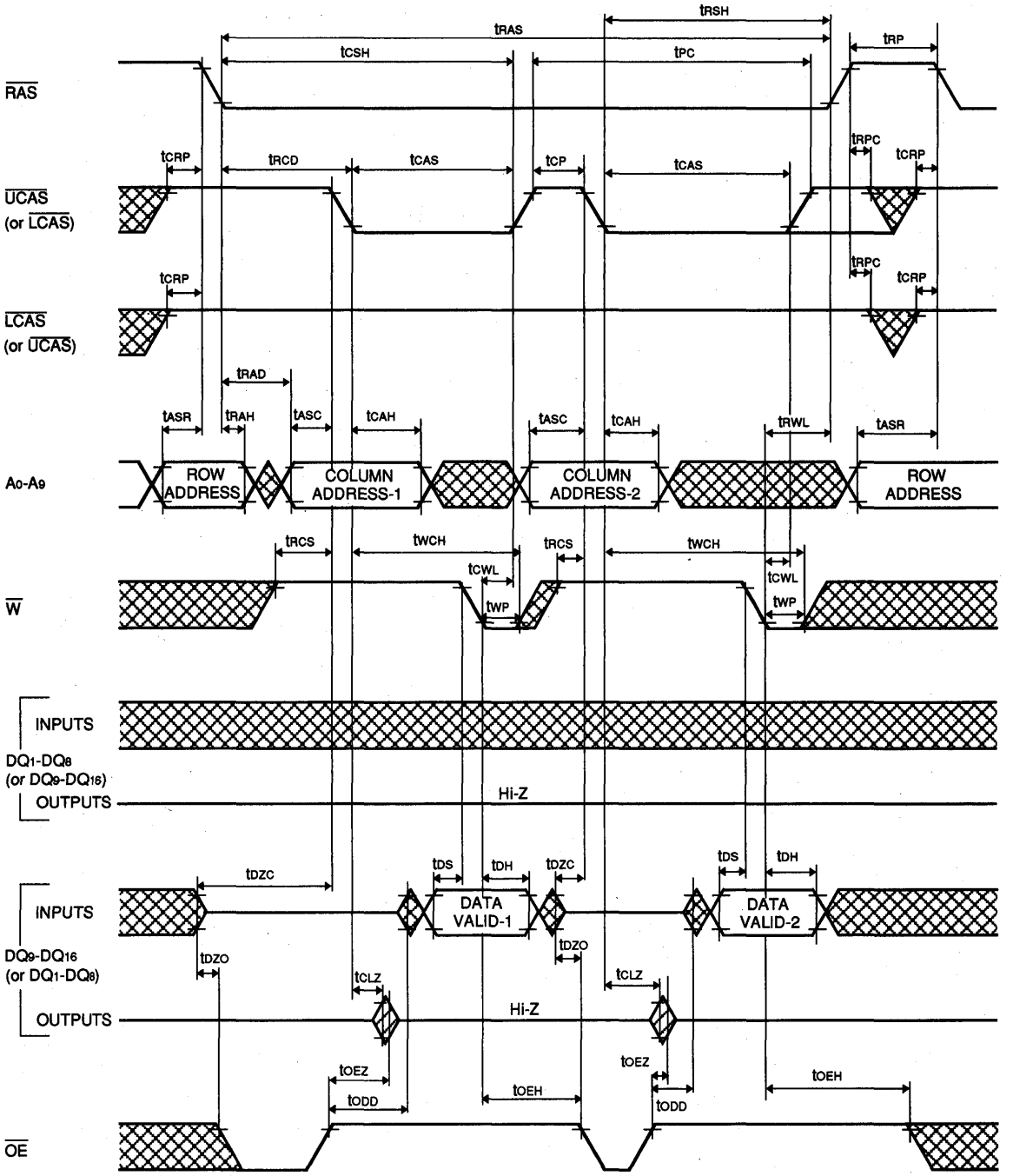
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



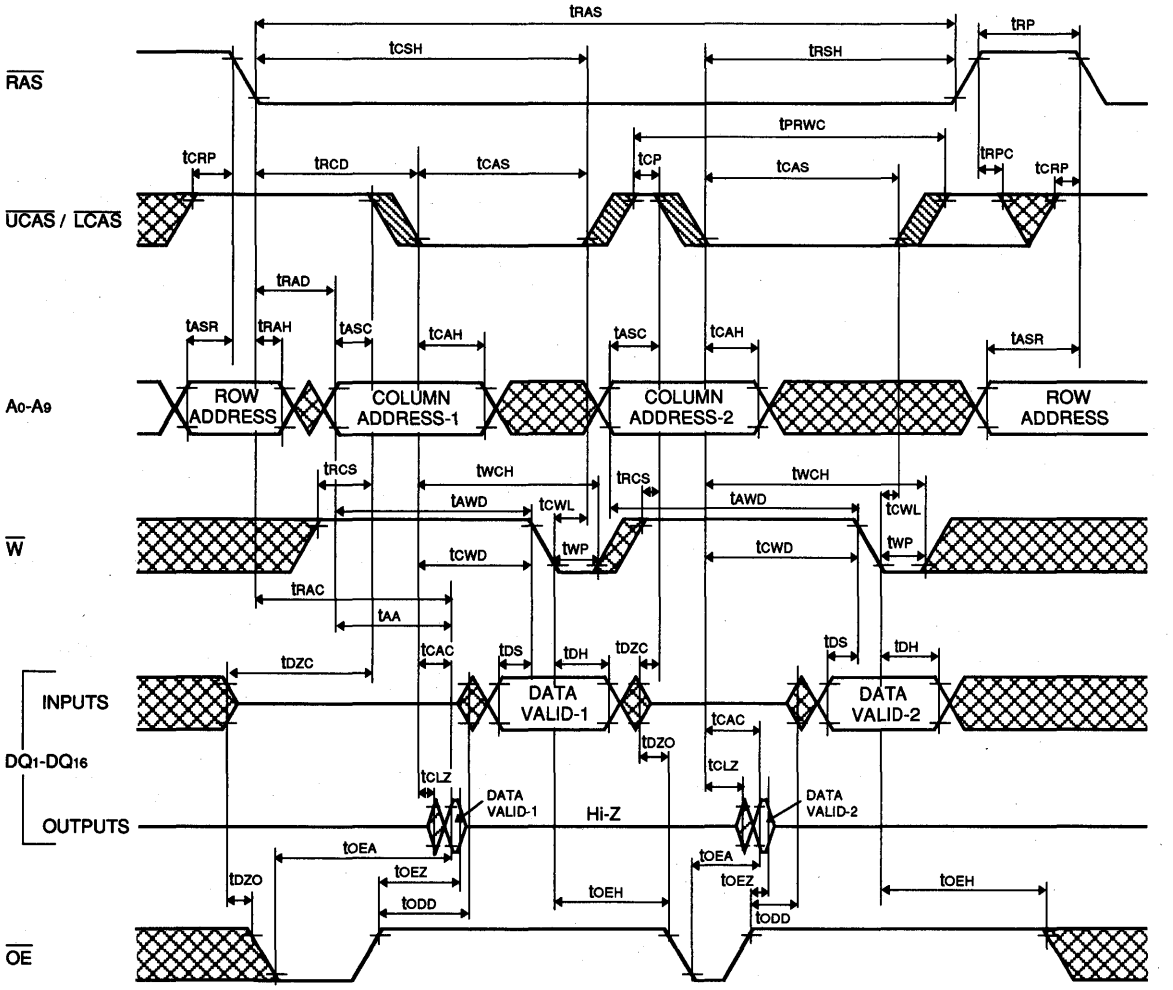
Fast Page Mode Write Cycle (Delayed Write)



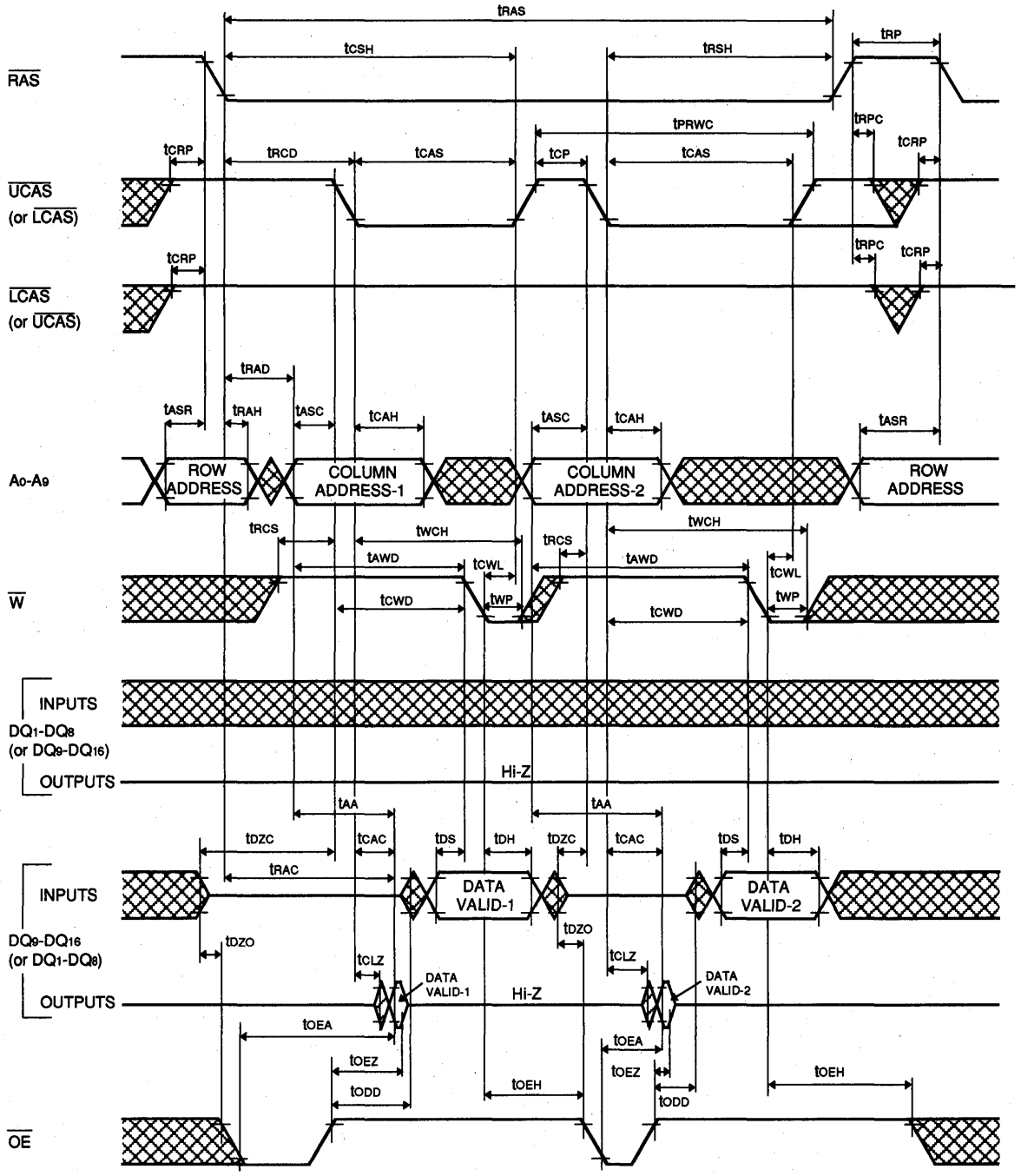
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8}	Supply current from Vcc Extended refresh cycle	M5M418160B -6S,-7S	$\overline{RAS}$ cycling $\overline{CAS} \leq 0.2V$ or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W} \leq 0.2V$ or $\geq Vcc - 0.2V$ $\overline{OE} \leq 0.2V$ or $\geq Vcc - 0.2V$ $A_0 \sim A_8 \leq 0.2V$ or $\geq Vcc - 0.2V$ DQ = open t_{REF} = 128ms t_{RAS} = t_{RAS} min～1 μs			500	μA
$I_{CC9\ (AV)}$	Average supply current from Vcc Self - Refresh cycle	M5M418160B -6S,-7S	$\overline{RAS} = \overline{CAS} \leq 0.2V$			400	μA

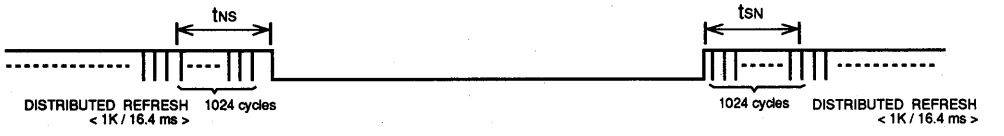
TIMING REQUIREMENTS (Ta=0～70°C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M418160B-6S		M5M418160B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

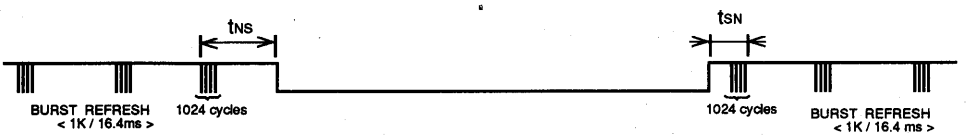
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leq$ 16.4 ms and $t_{SN} \leq$ 16.4 ms.

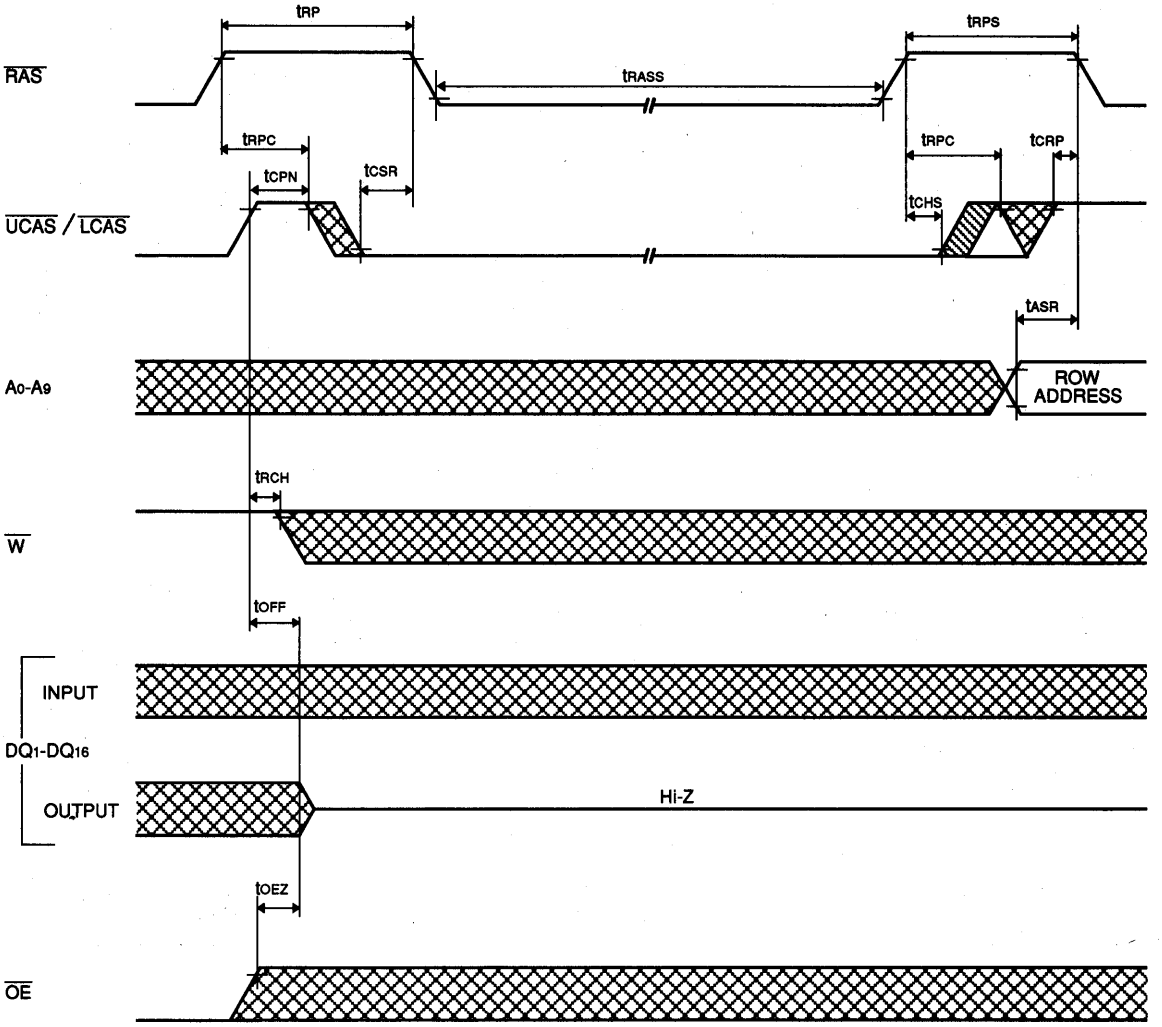


(2) In case of burst refresh

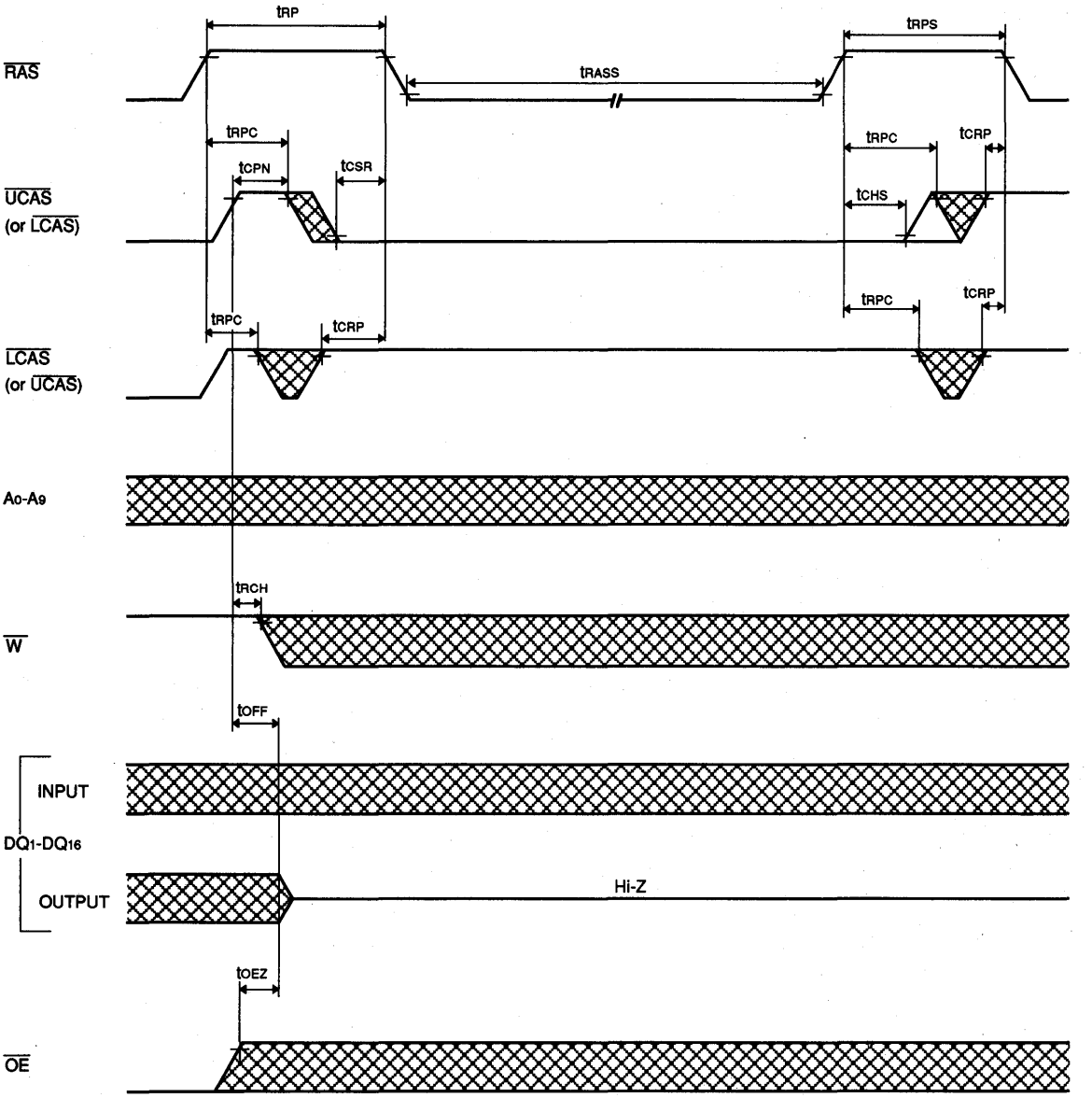
The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} + $t_{SN} \leq$ 16.4 ms.



Self Refresh Cycle



Upper/(Lower) Self Refresh Cycle*



M5M418165BJ,TP-6,-7,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418165BXX-6,-6S	60	15	30	15	110	680
M5M418165BXX-7,-7S	70	20	35	20	130	590

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M418165Bxx-6,-6S ---------- 940.0mW (Max)
  M5M418165Bxx-7,-7S ---------- 830.0mW (Max)
- Hyper-page mode, Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)

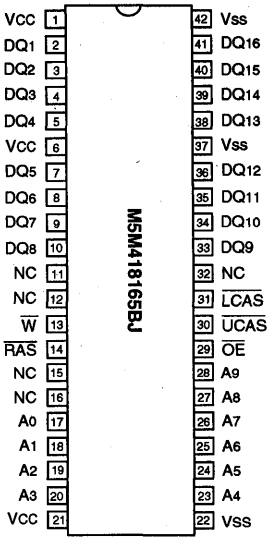
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

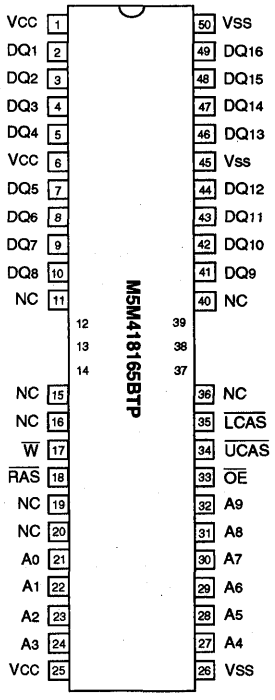
PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP Normal Bend)

NC : NO CONNECTION

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

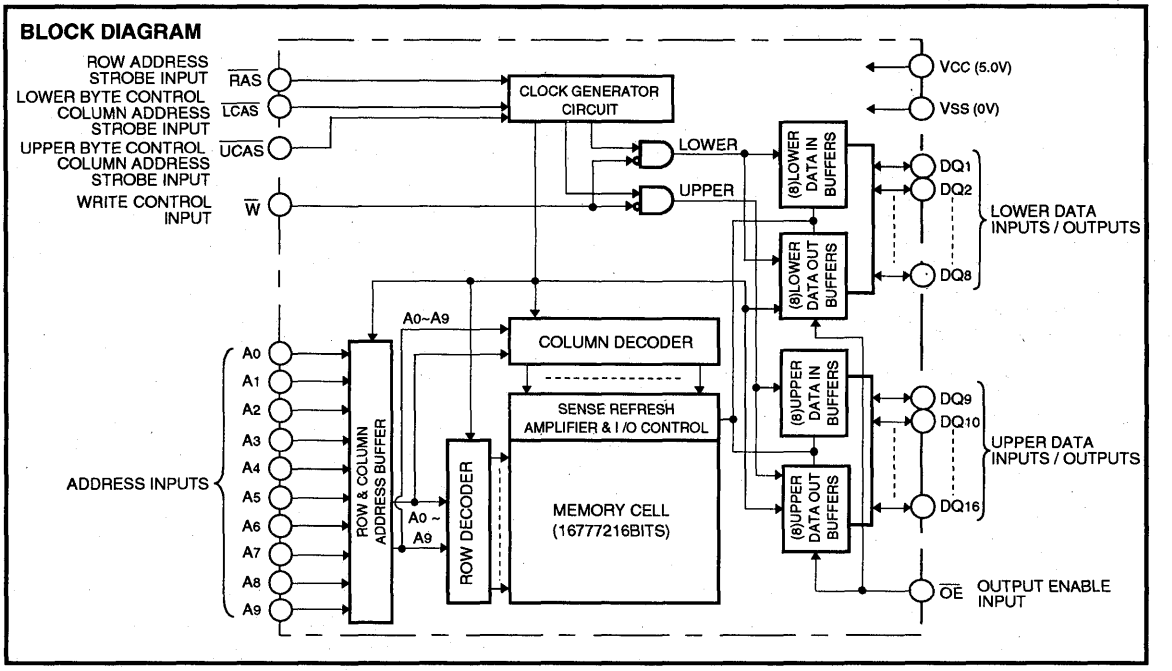
The M5M418165BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
V_O	Output voltage		-1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M418165B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			170	mA
		M5M418165B-7,-7S				150	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M418165B-6,-7	$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			1	
		M5M418165B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			0.3	
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 3,5)	M5M418165B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			170	mA
		M5M418165B-7,-7S				150	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M418165B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			135	mA
		M5M418165B-7,-7S				115	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418165B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			170	mA
		M5M418165B-7,-7S				150	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high	(Note 12)	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10uA|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		16.4		16.4	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		10		13		ns
t_{WP}	Write pulse width		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 23)	133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width		89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 24)	47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M418165B-6,-6S		M5M418165B-7,-7S		
		Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time	66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 27)	10	18	13	18	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)	7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read	62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read	30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	35		40		ns

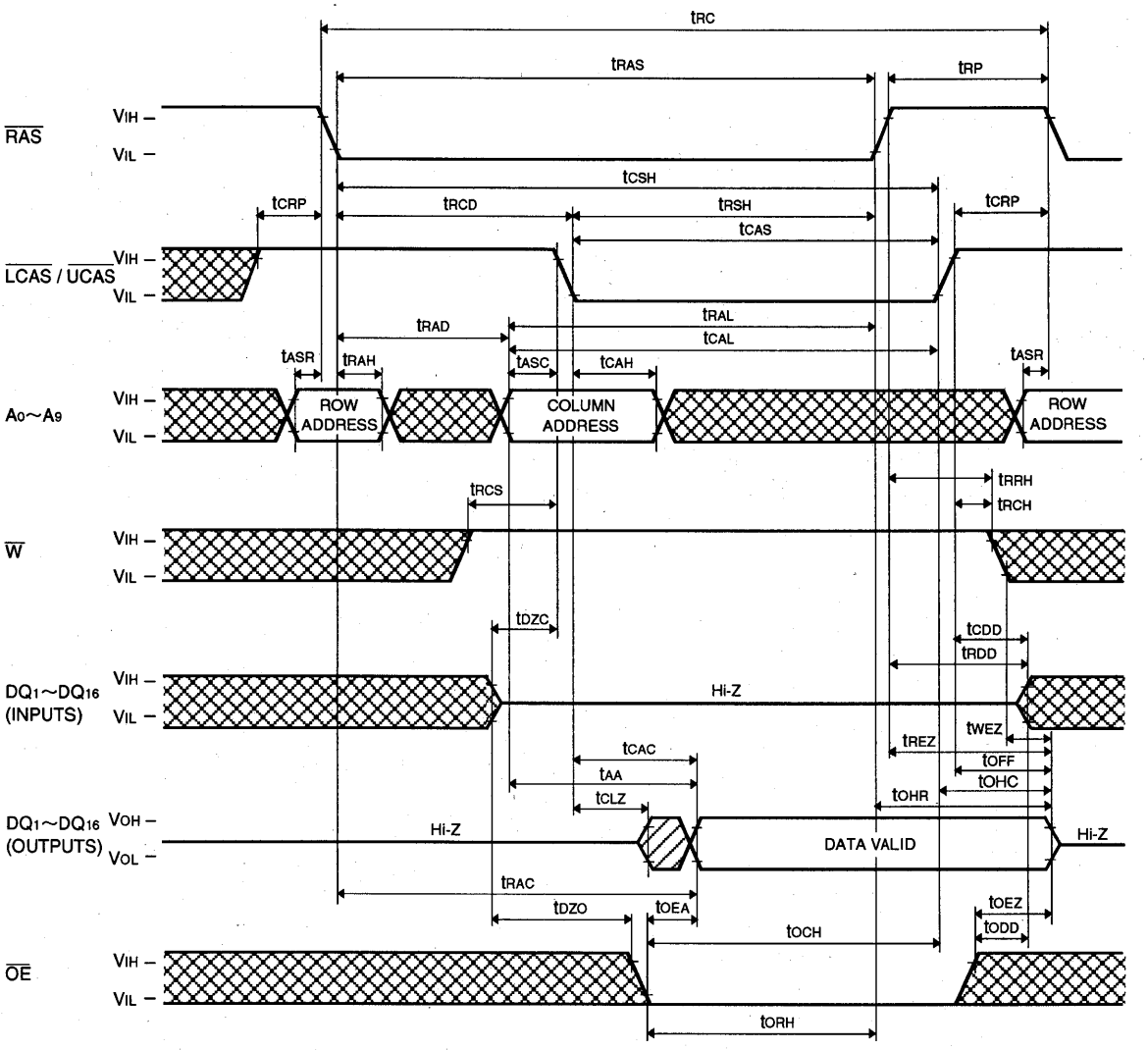
Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M418165B-6,-6S		M5M418165B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 29)
Read Cycle

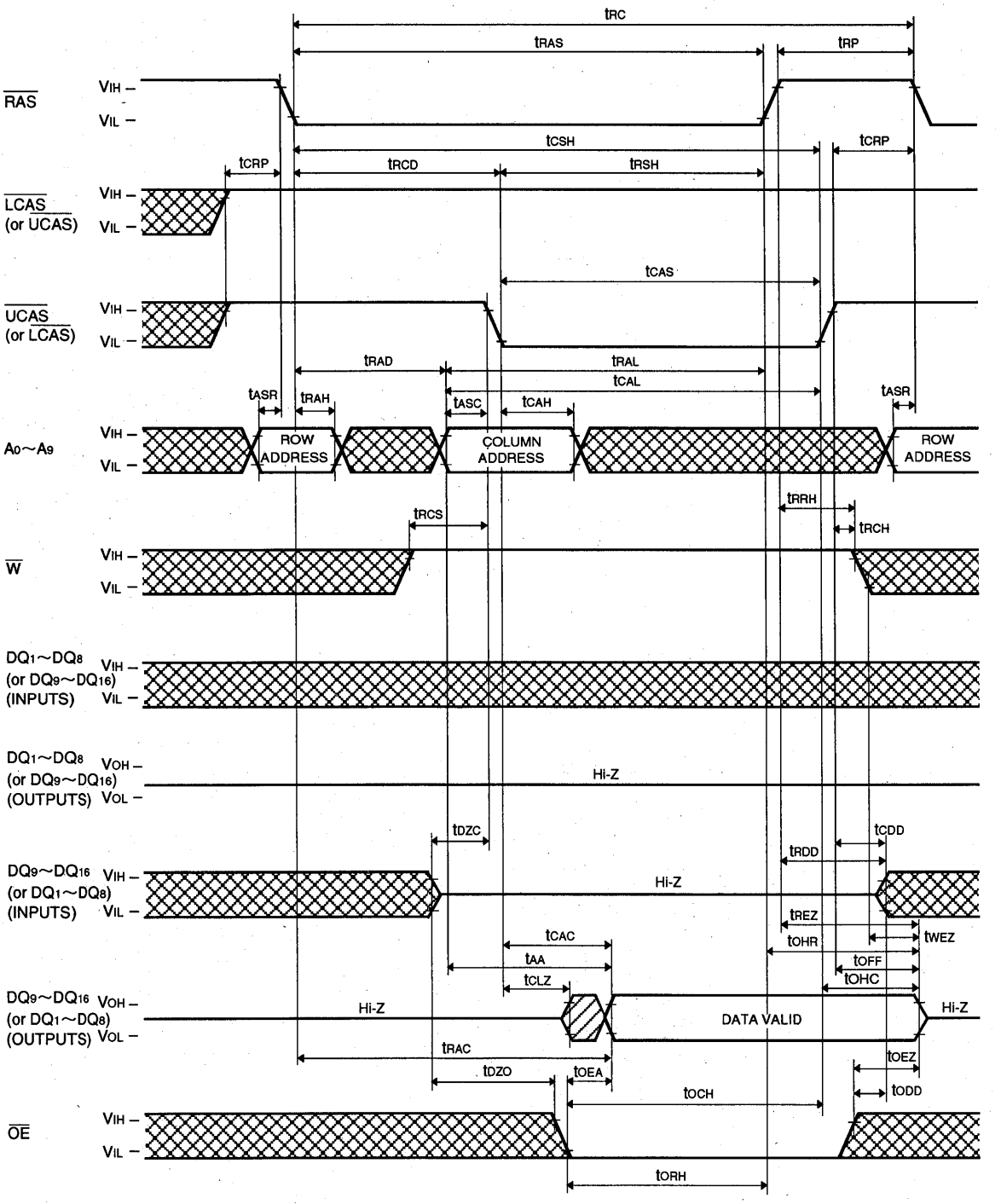


Note 29

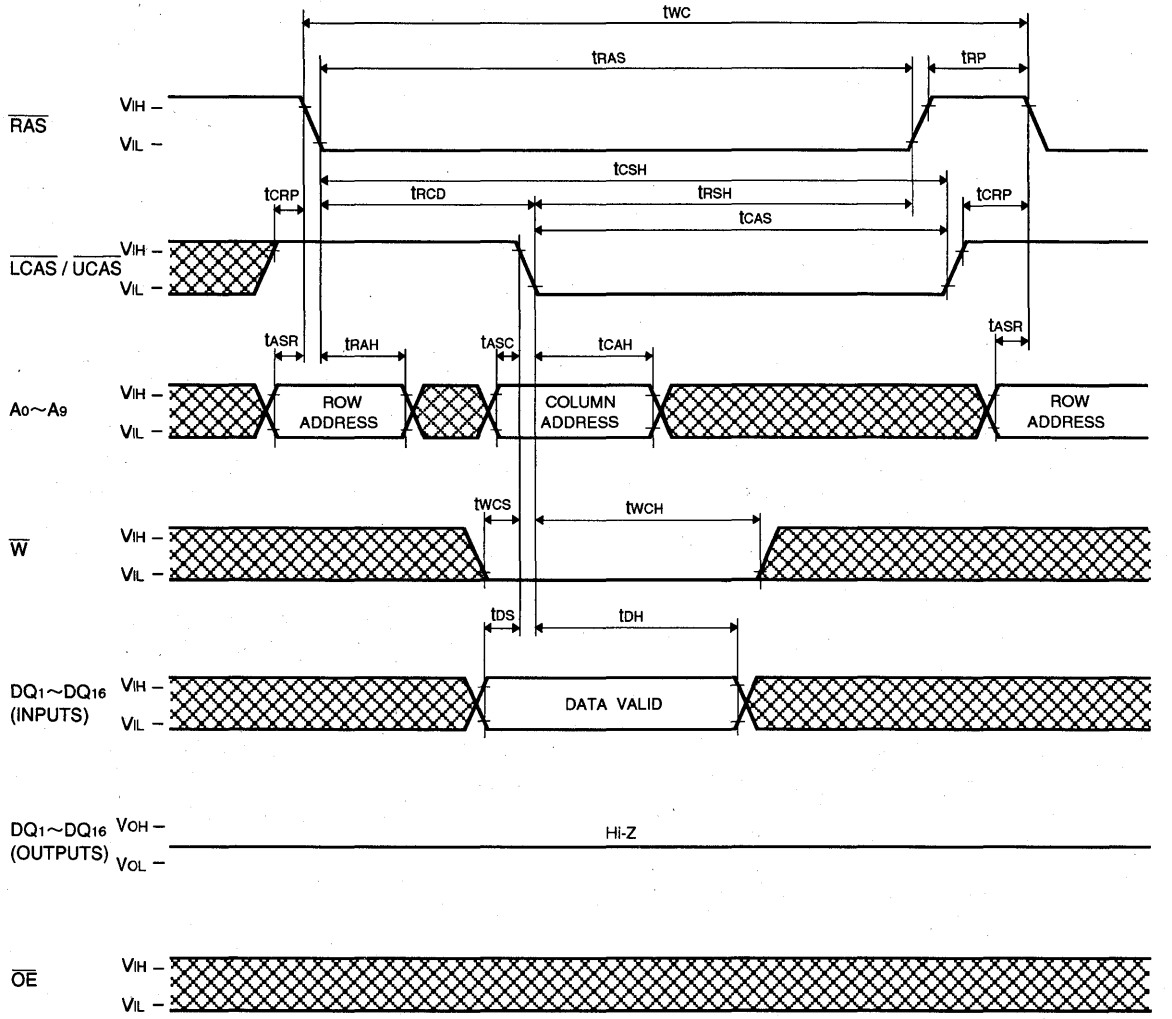
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

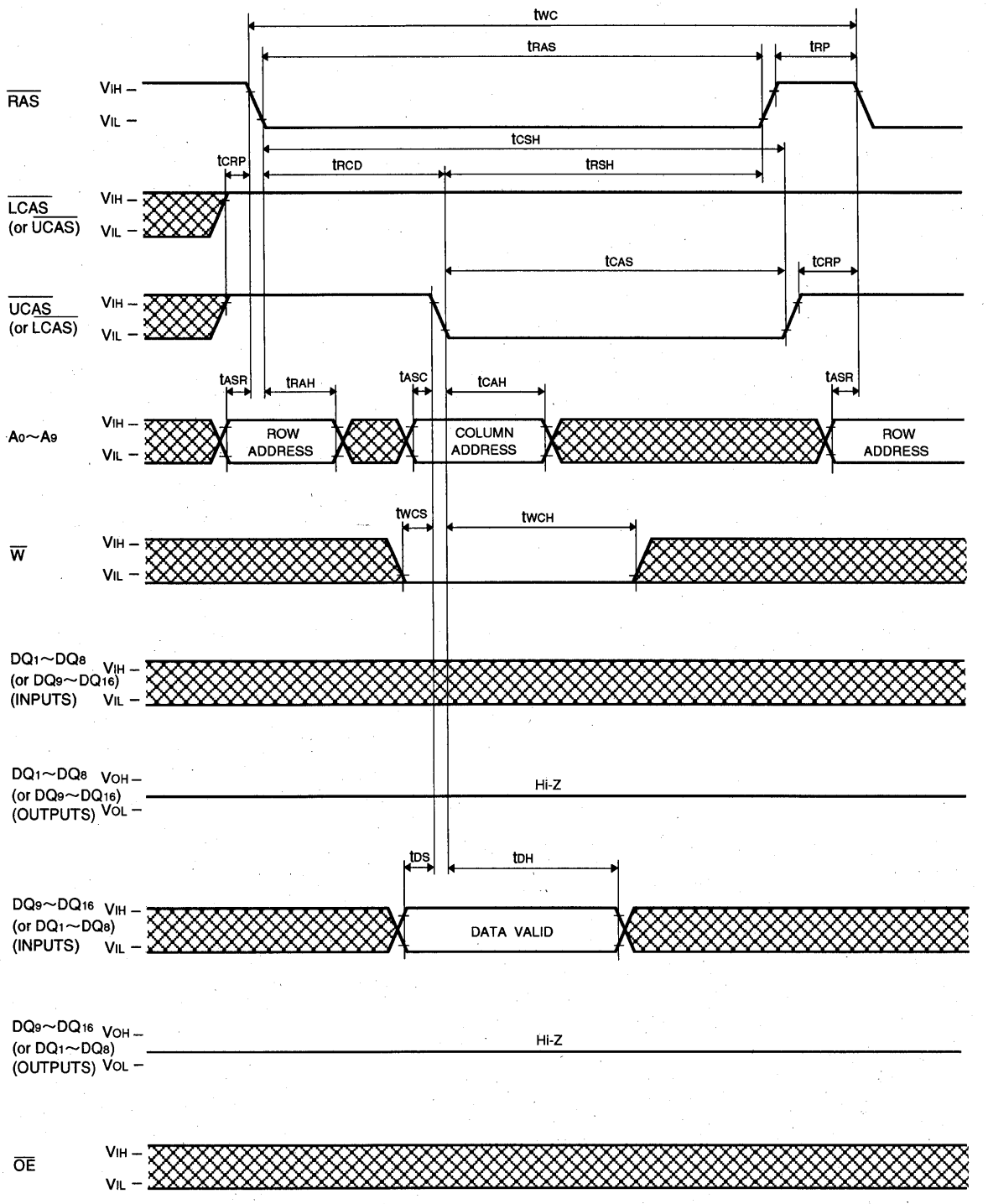
Byte Read Cycle



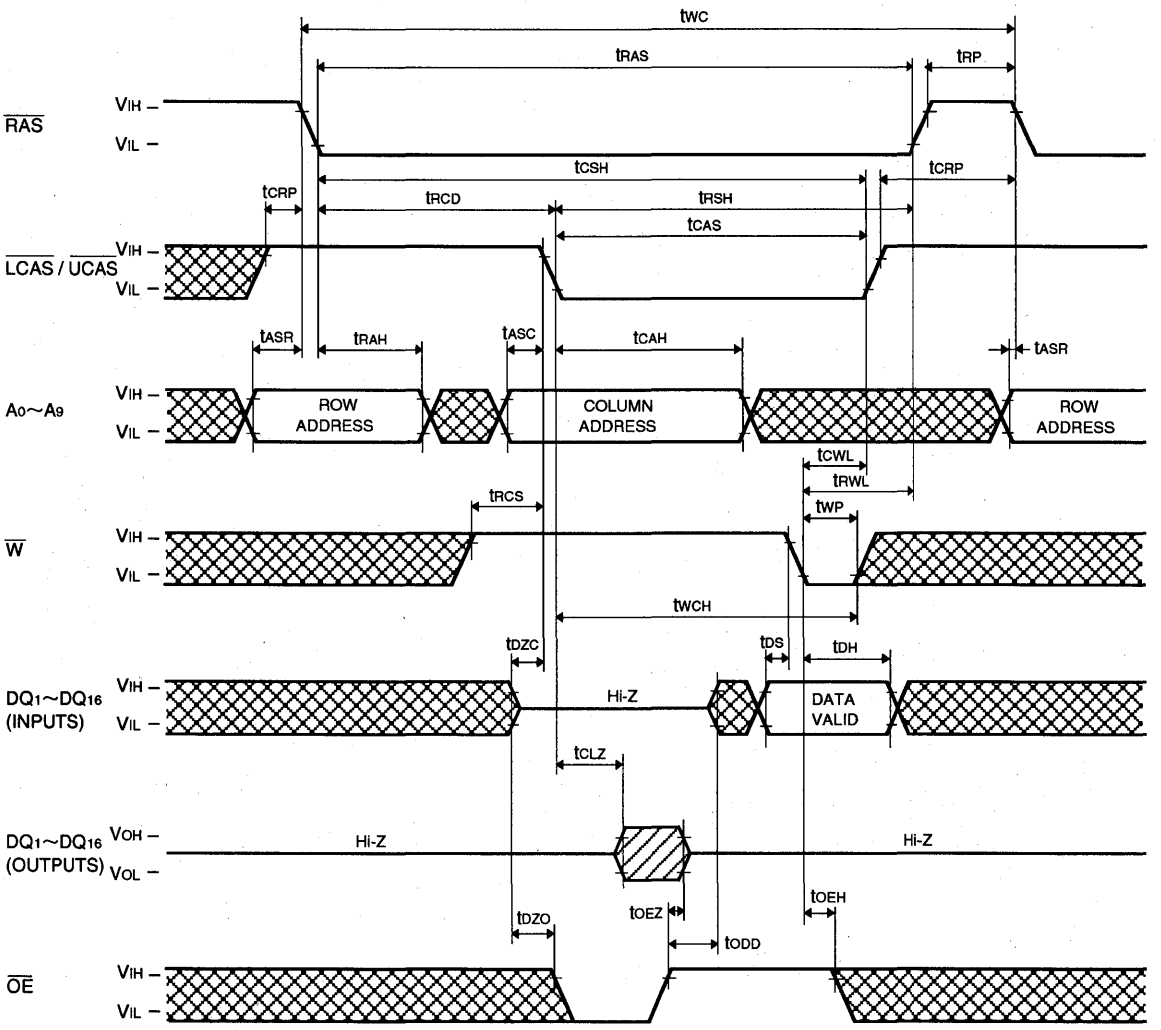
Early Write Cycle



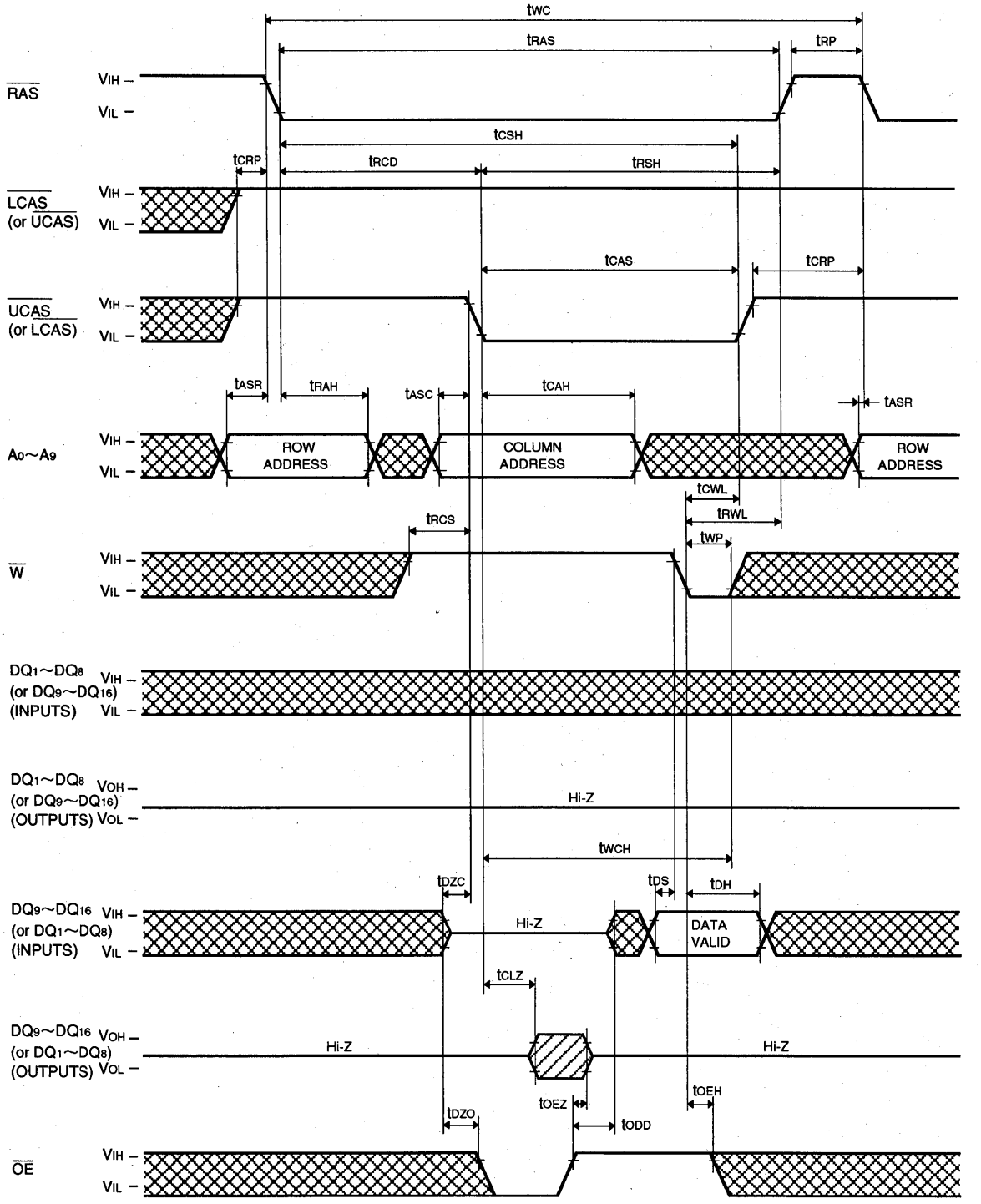
Byte Early Write Cycle



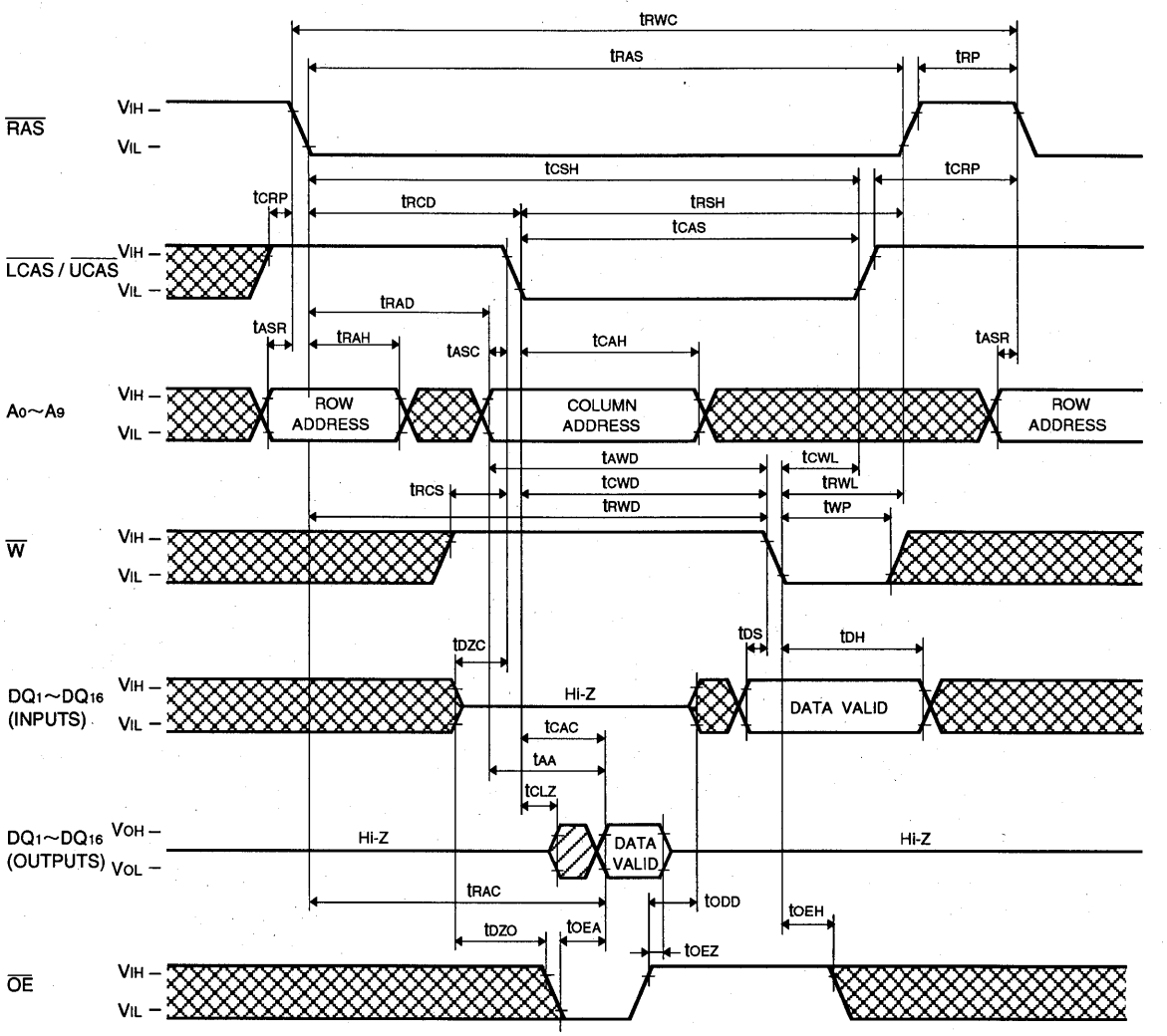
Delayed Write Cycle



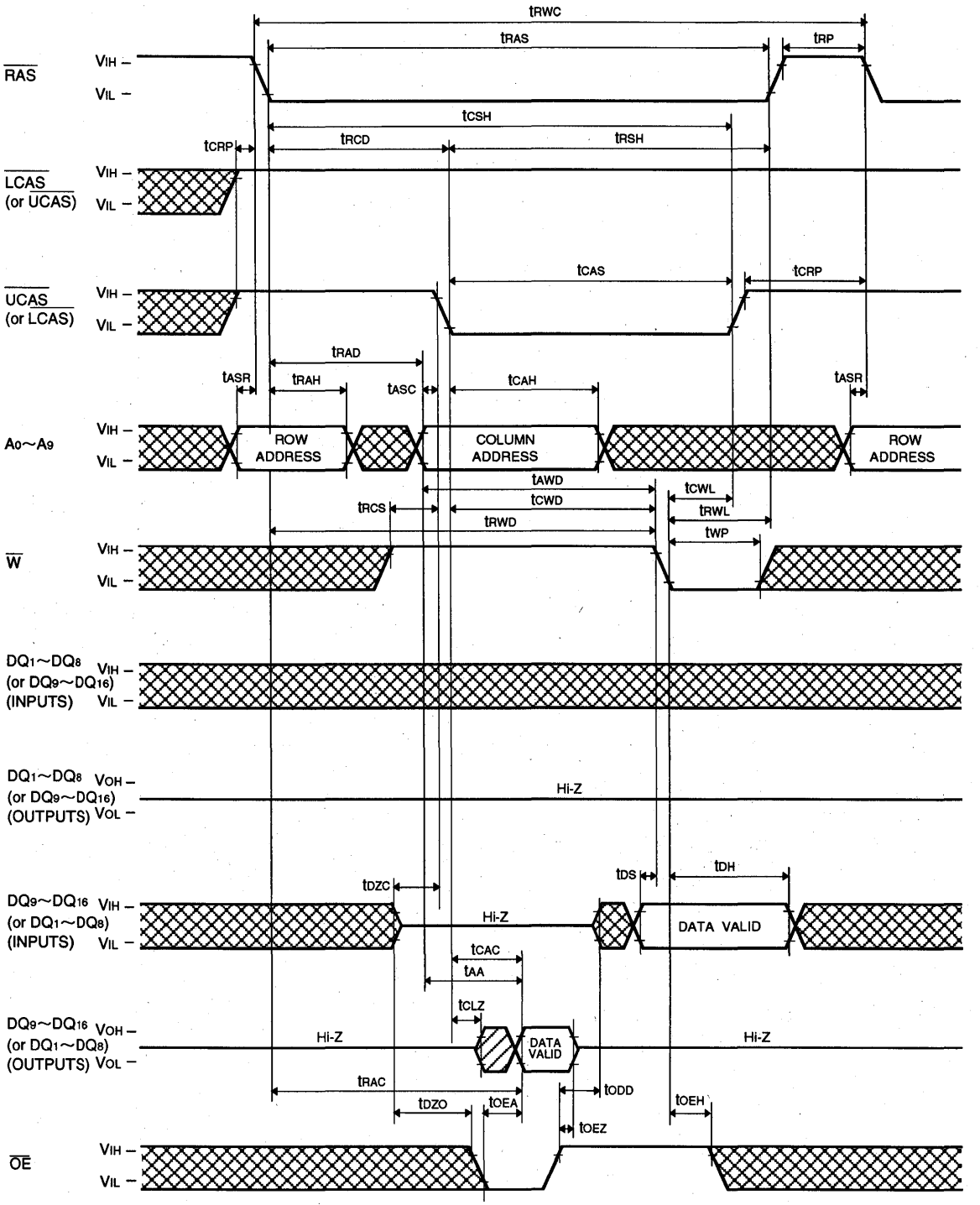
Byte Delayed Write Cycle



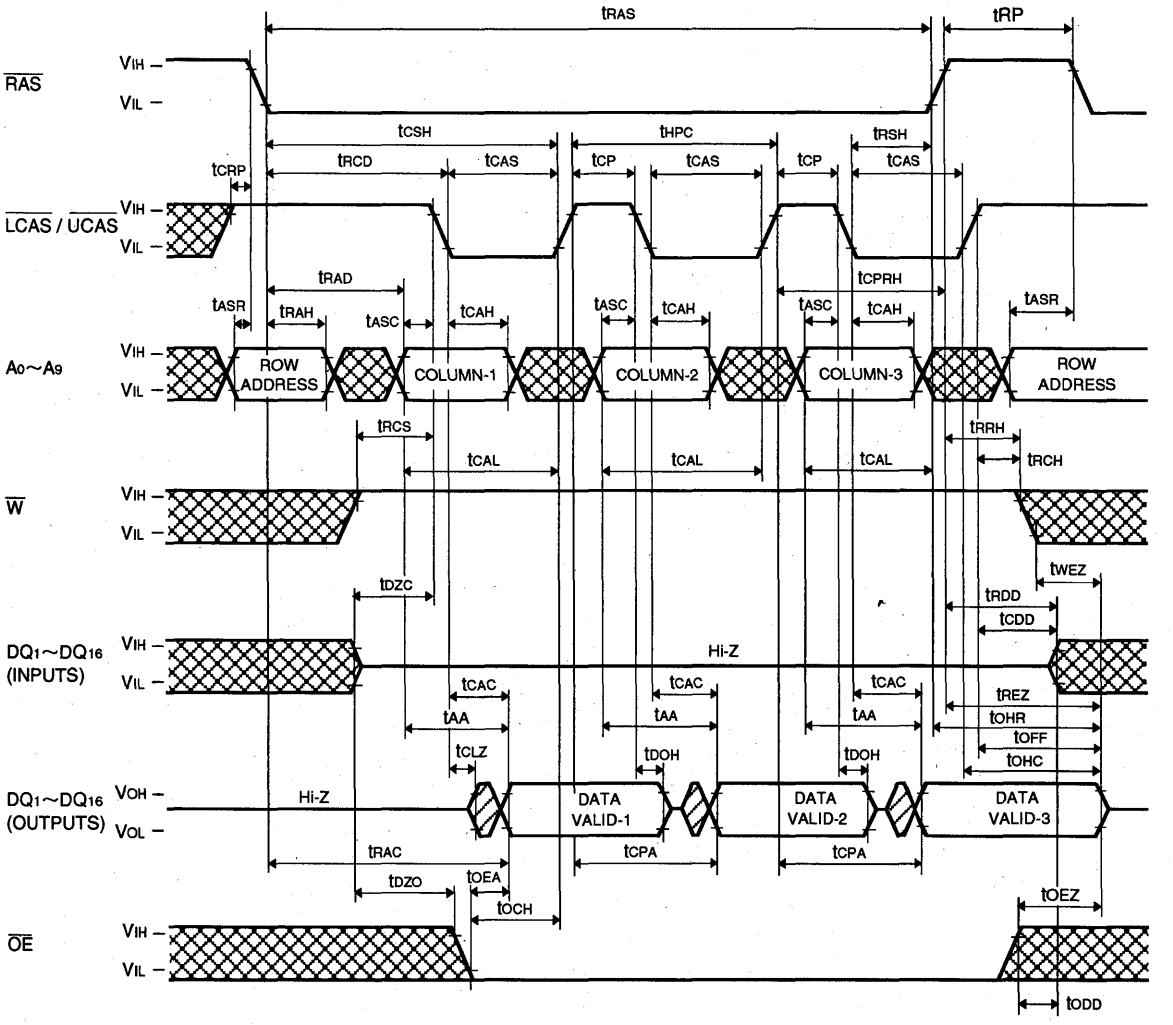
Read-Write, Read-Modify-Write Cycle



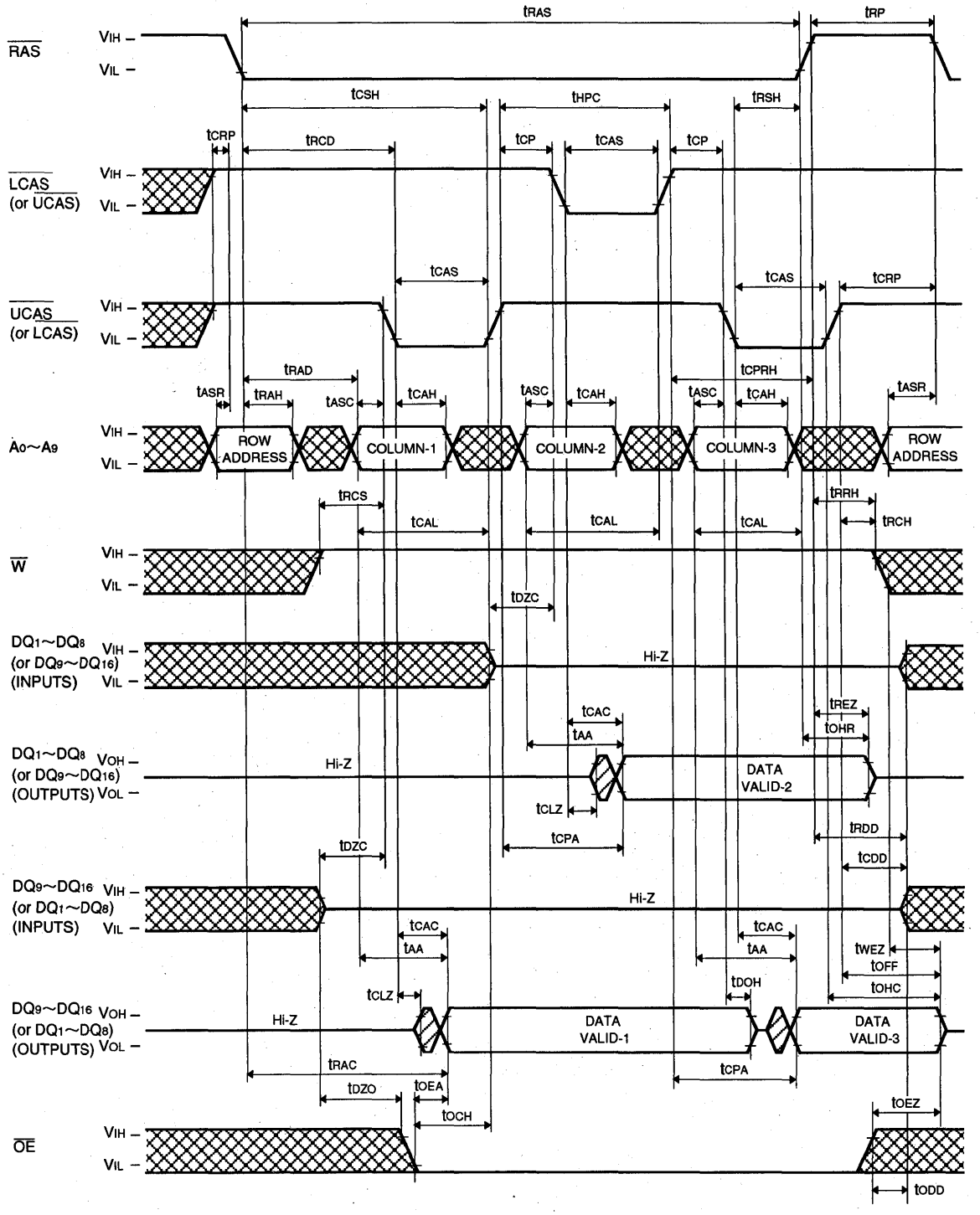
Byte Read-Write, Read-Modify-Write Cycle



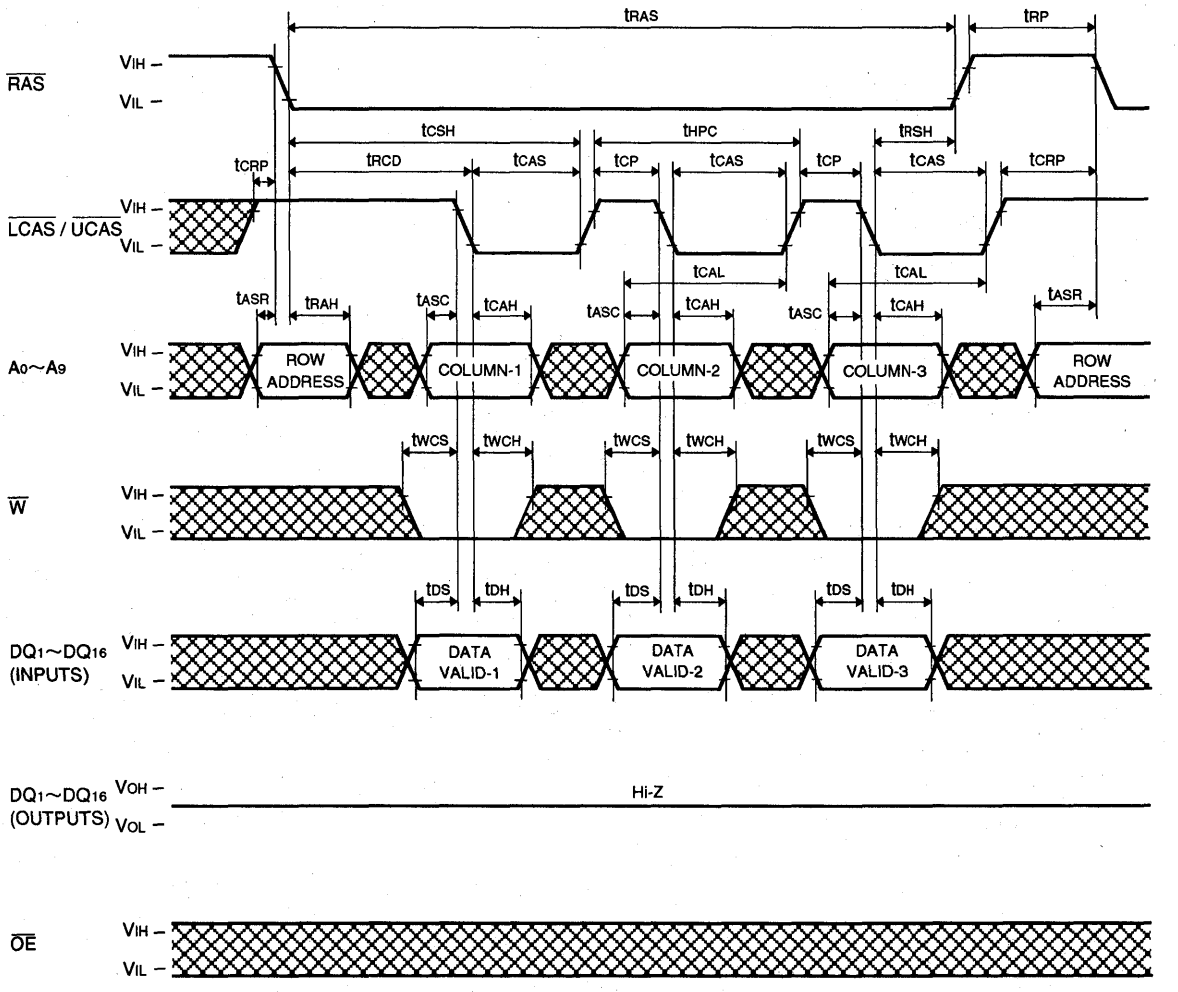
Hyper Page Mode Read Cycle



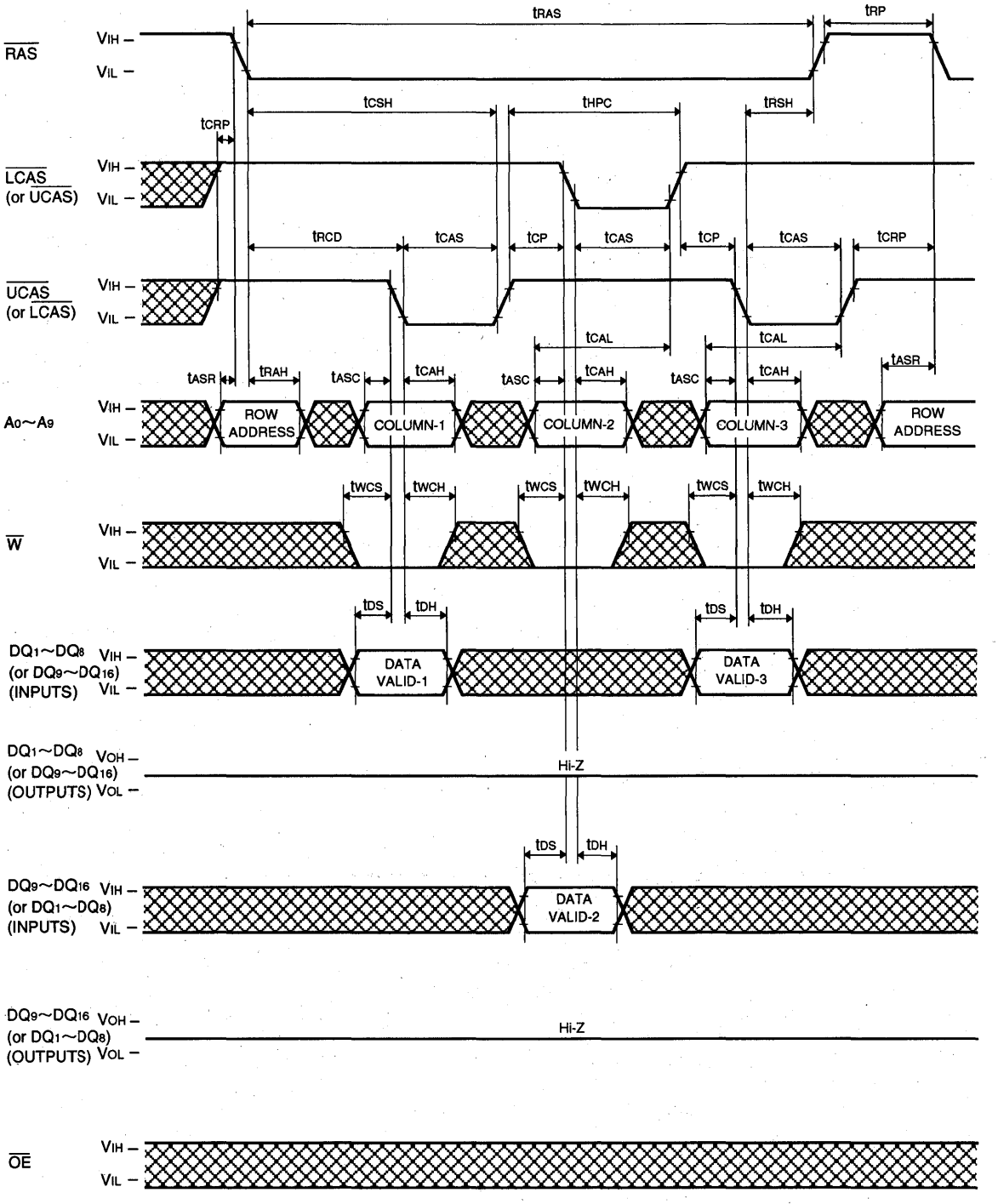
Hyper Page Mode Byte Read Cycle



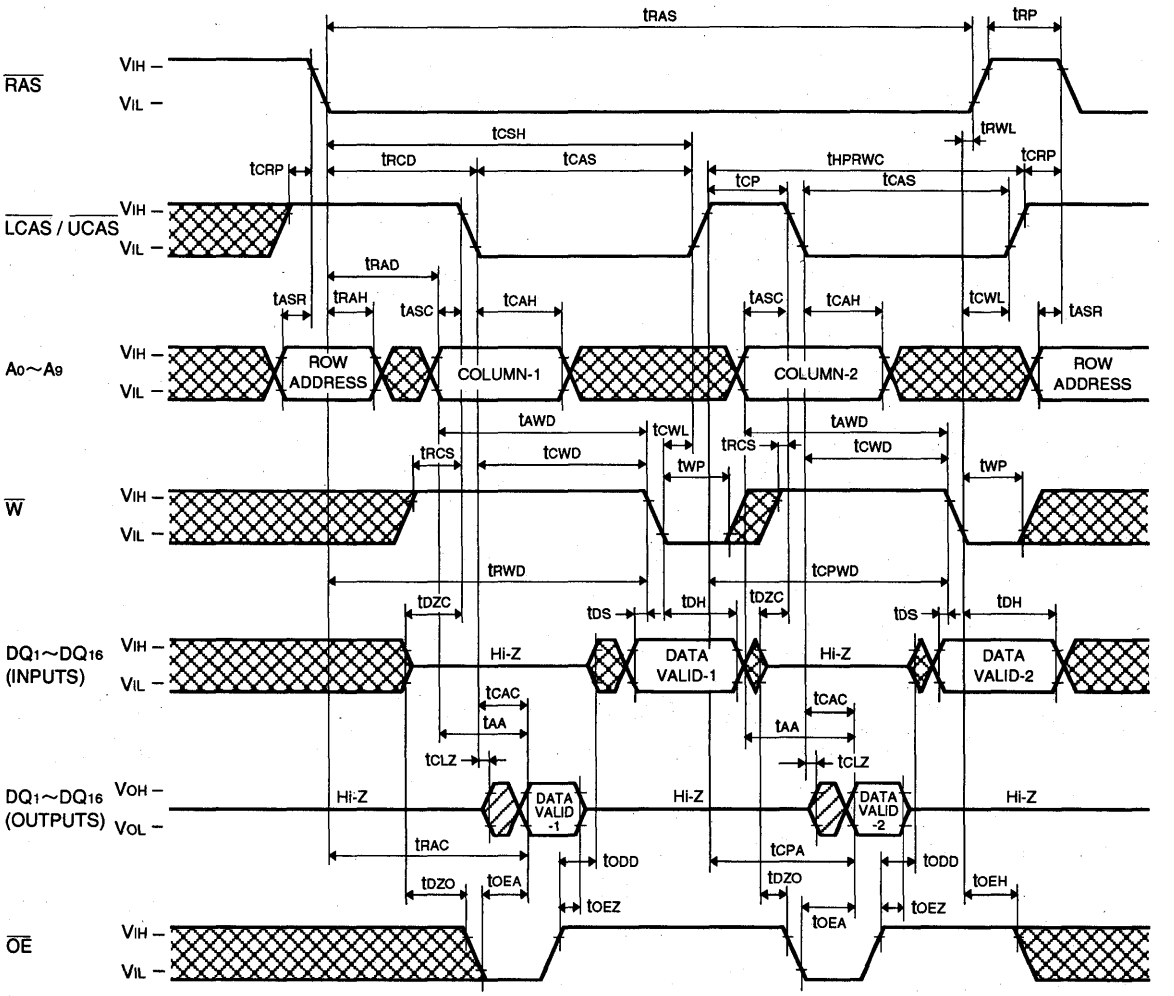
Hyper Page Mode Early Write Cycle



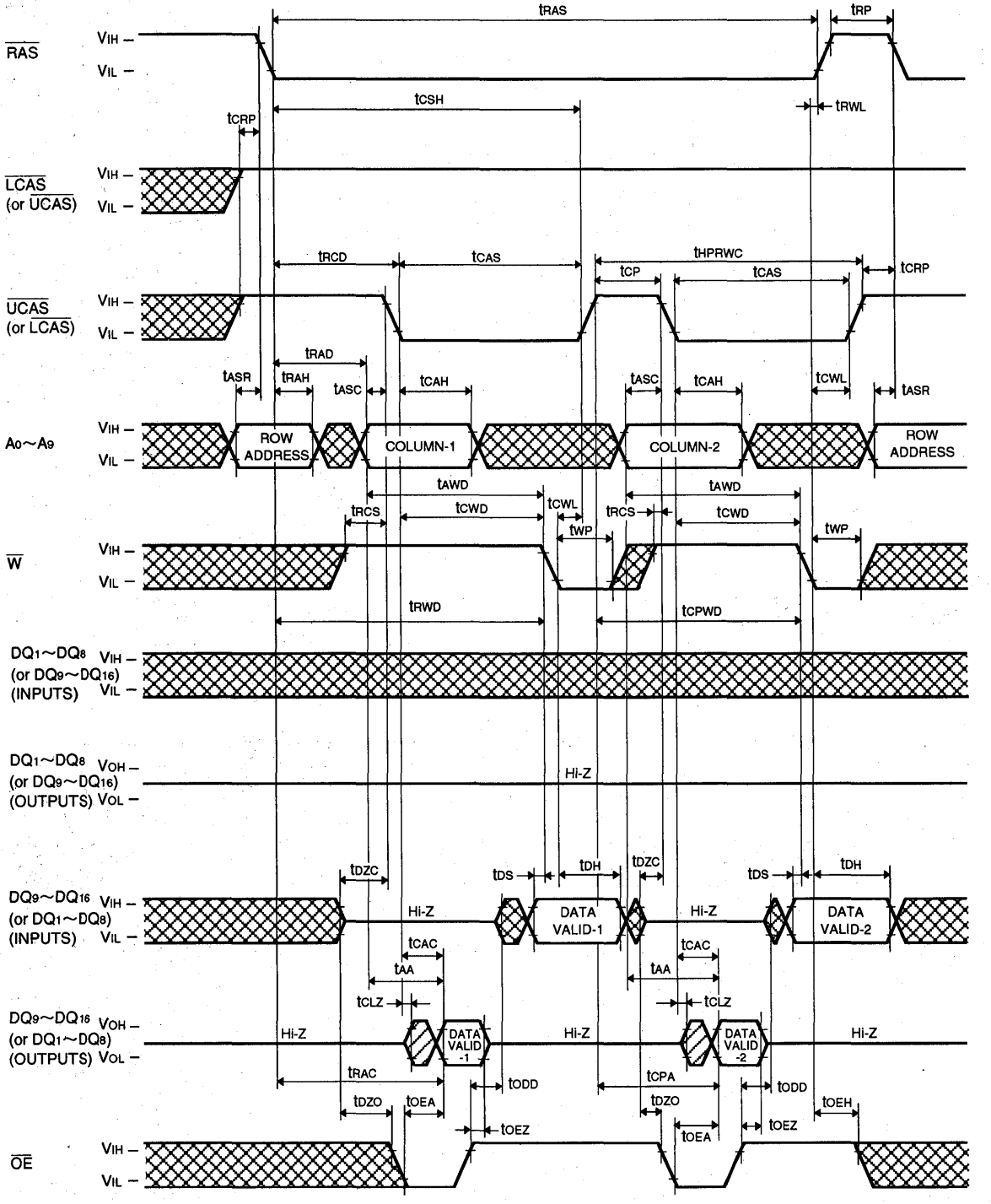
Hyper Page Mode Byte Early Write Cycle



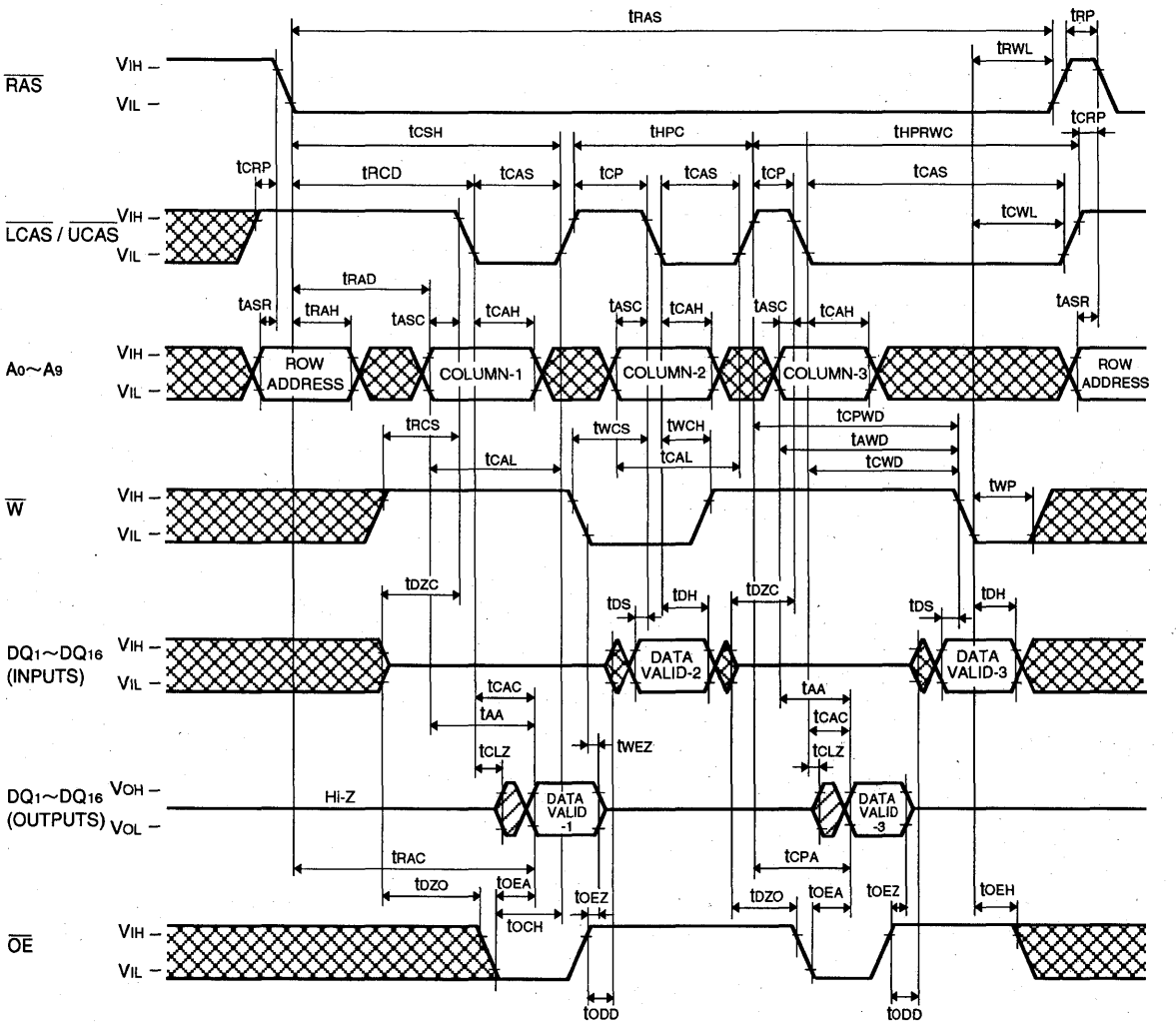
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



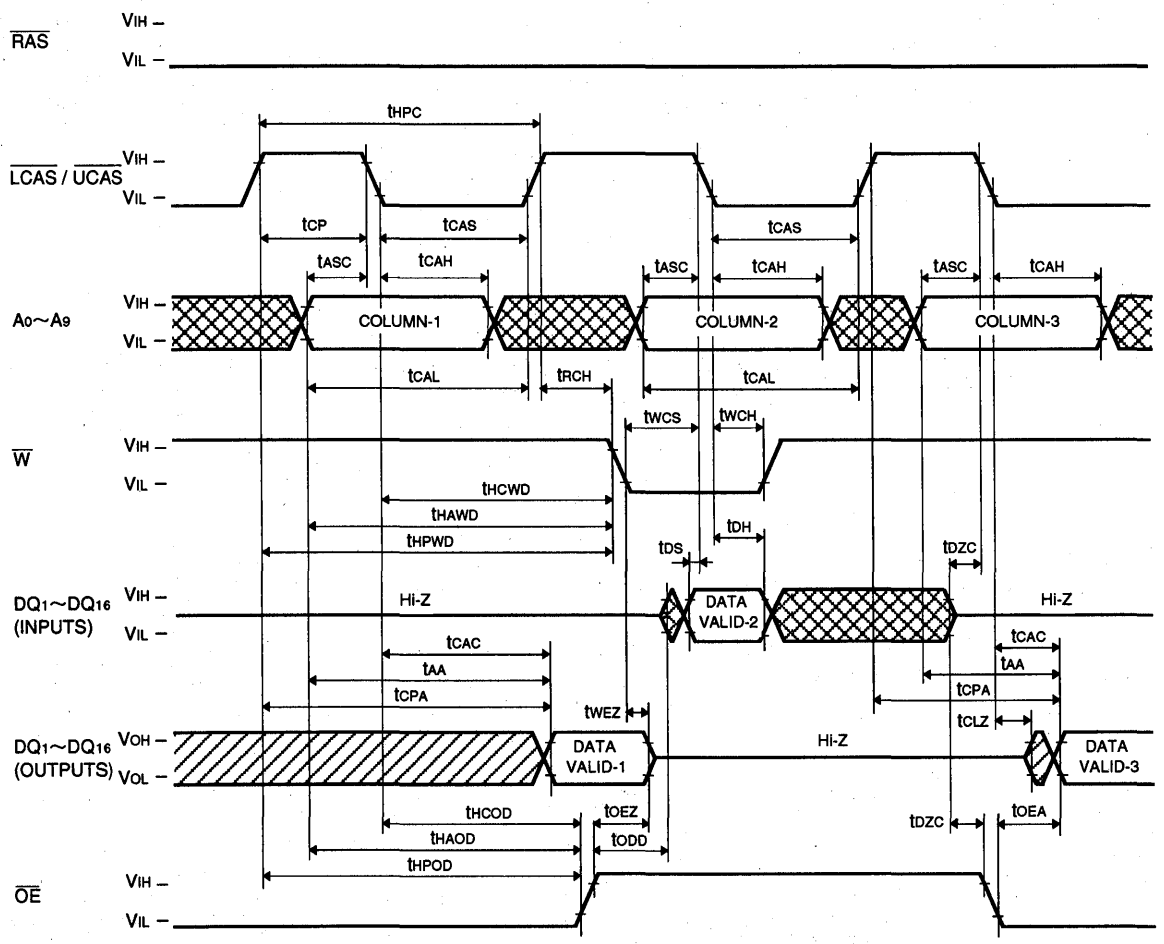
Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



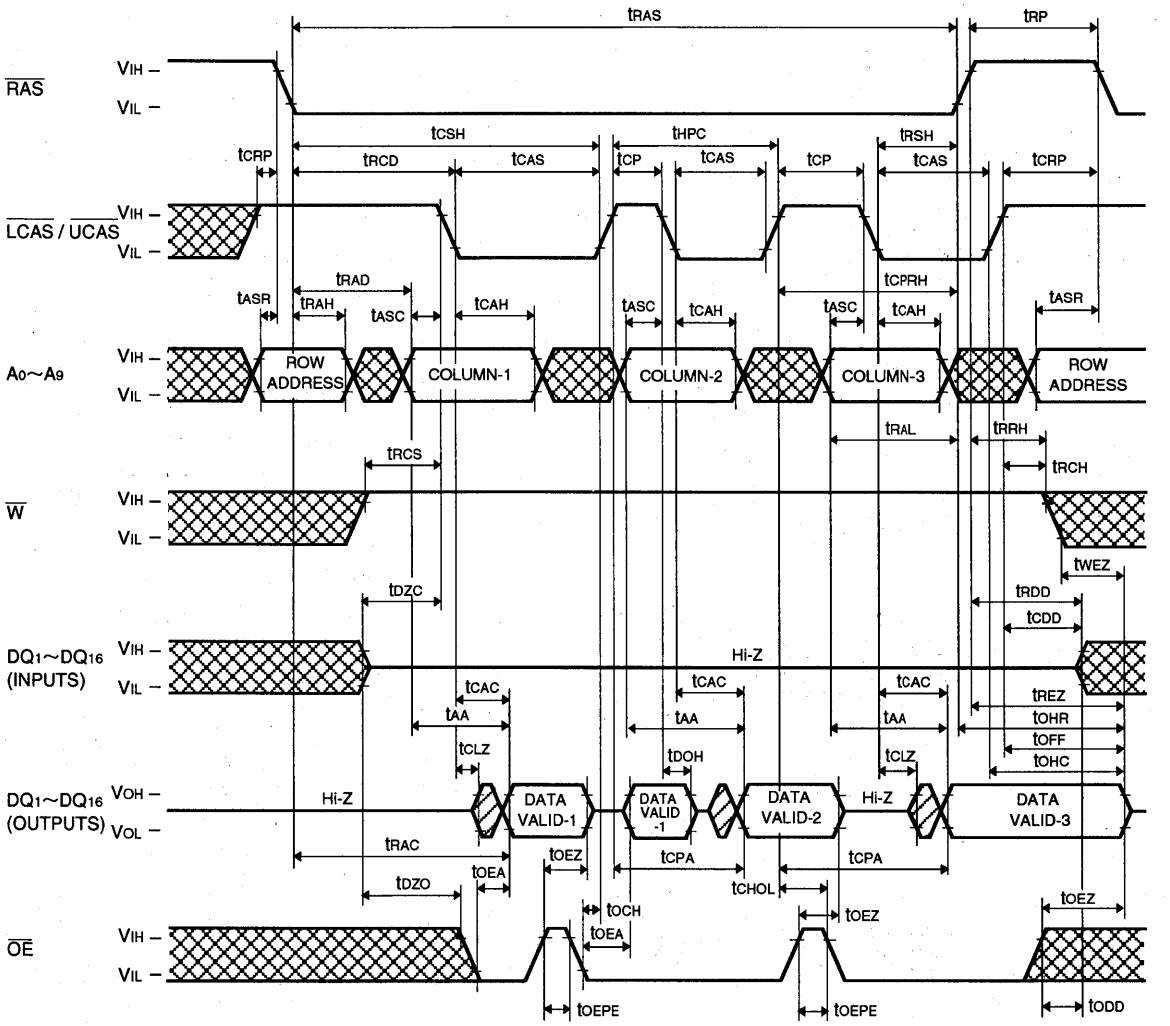
Hyper Page Mode Mix Cycle (1)



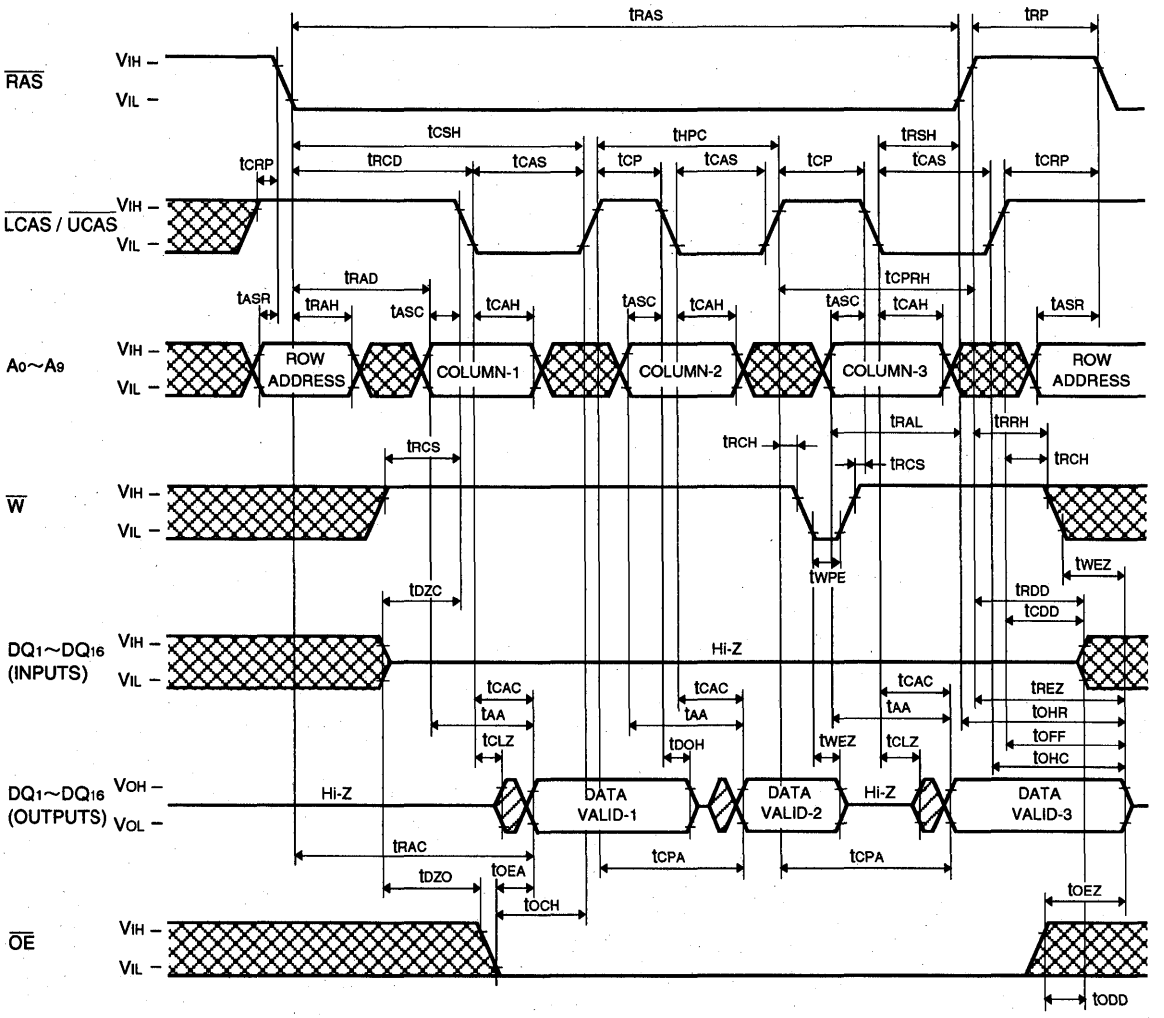
Hyper Page Mode Mix Cycle (2)



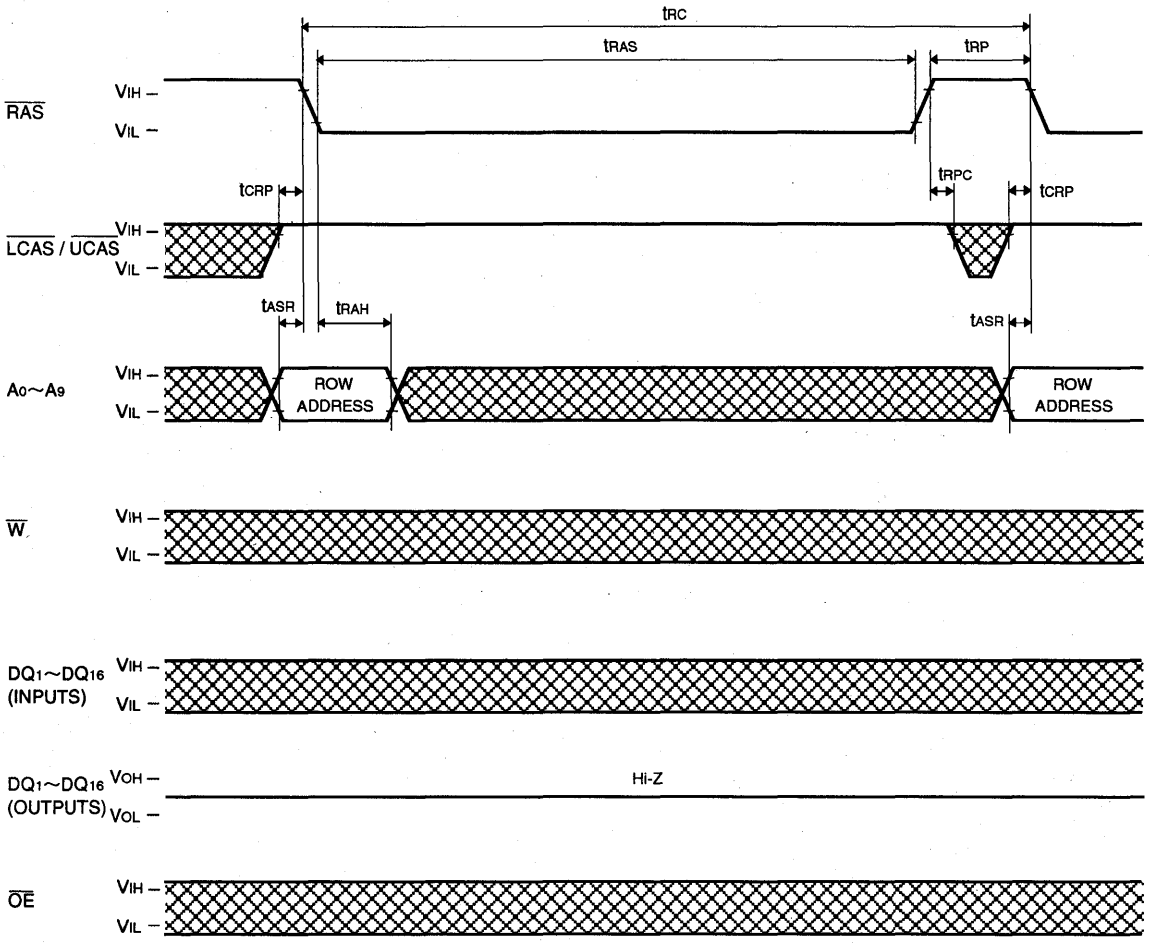
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



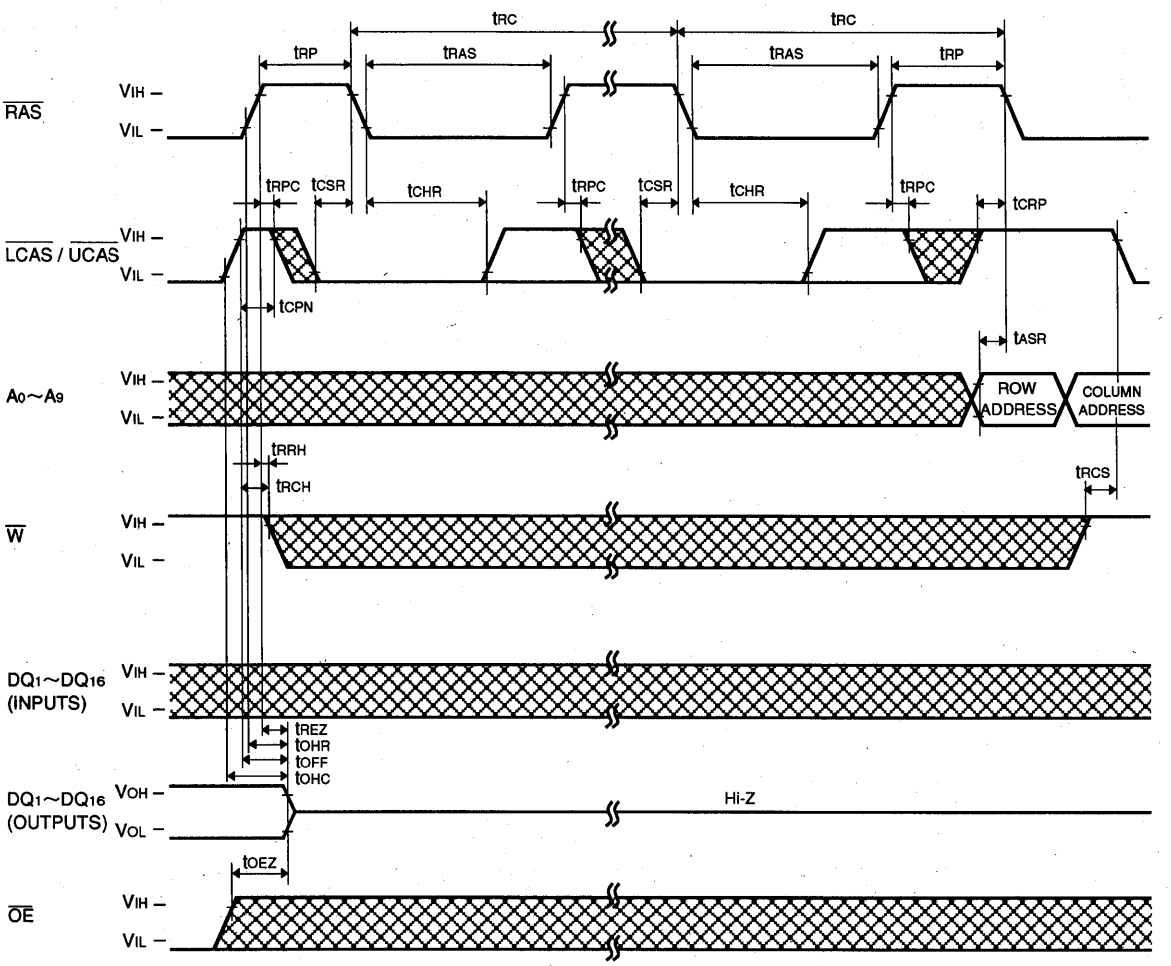
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



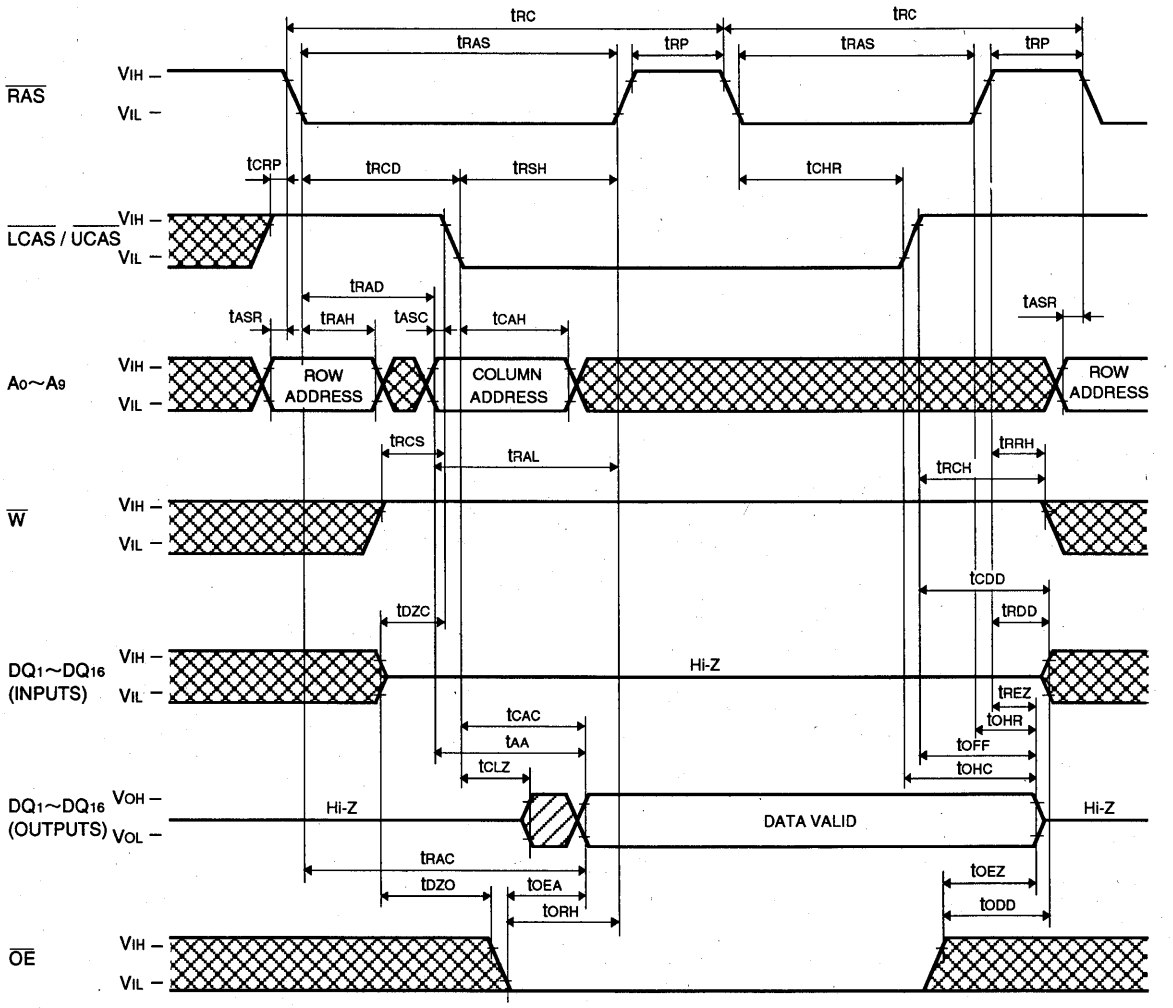
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

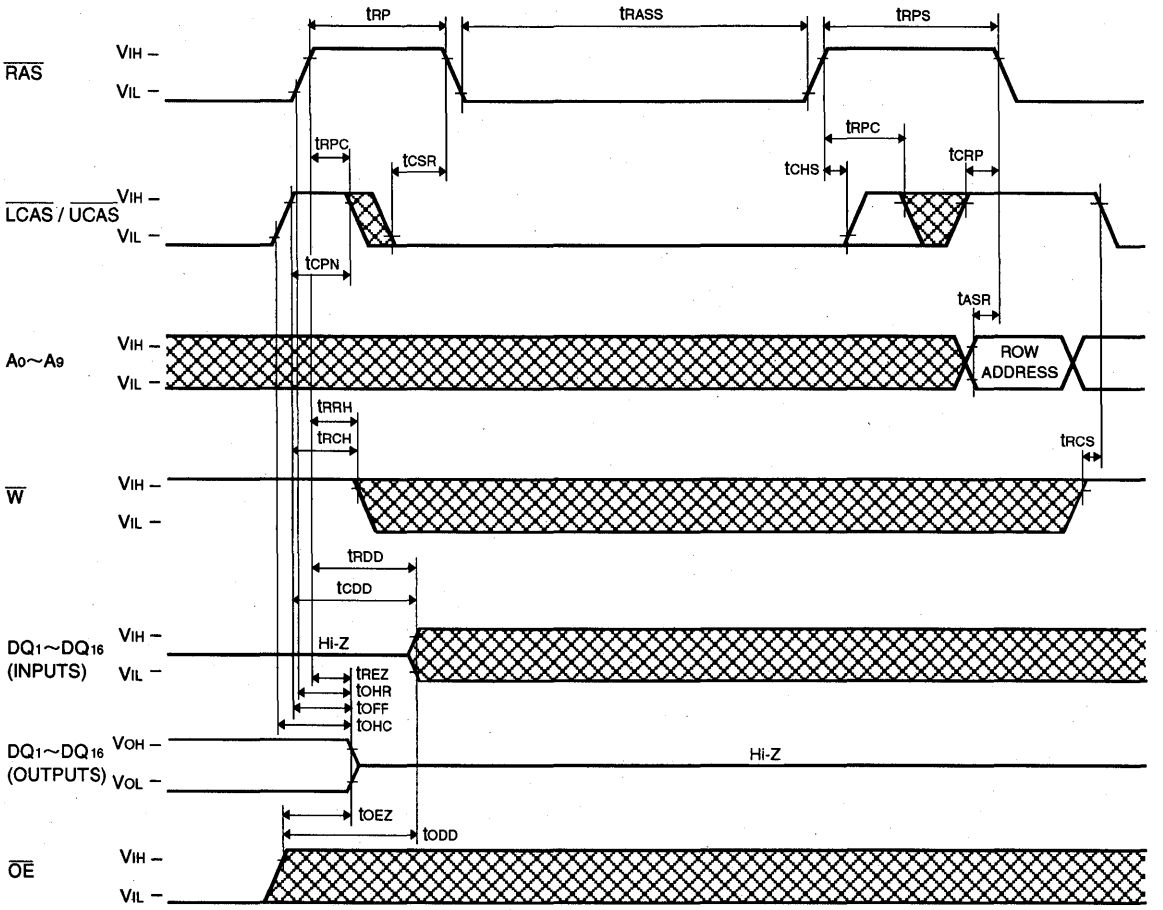


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle * (Note 31)



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8(AV)}$	Average supply current from Vcc Extended refresh mode	M5M418165B (S)	$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_9≦0.2V or ≧Vcc-0.2V t_{REF}=128ms, output open $t_{RAS}=t_{RASmin}$~1 μs			500	μA
$I_{CC9(AV)}$	Average supply current from Vcc Self-refresh cycle	M5M418165B (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			400	μA

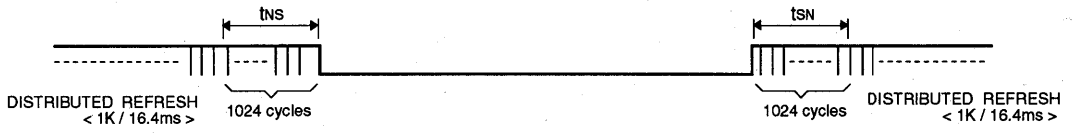
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M418165B-6S		M5M418165B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

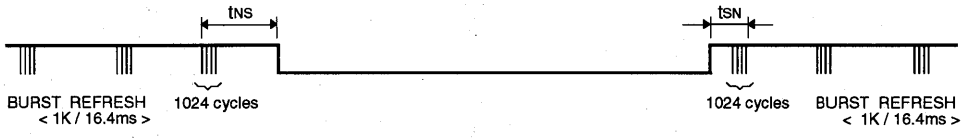
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦16.4ms and t_{SN}≦16.4ms.



(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} +t_{SN}≦16.4ms.



PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416160CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416160CXX-5,-5S	50	13	25	13	90	540
M5M416160CXX-6,-6S	60	15	30	15	110	430
M5M416160CXX-7,-7S	70	20	35	20	130	385

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M416160Cxx-5,-5S ---------- 660.0mW (Max)
  M5M416160Cxx-6,-6S ---------- 525.0mW (Max)
  M5M416160Cxx-7,-7S ---------- 470.0mW (Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~ A_{11})
  * : Applicable to self refresh version (M5M416160CJ,TP-5S,-6S, -7S : option) only

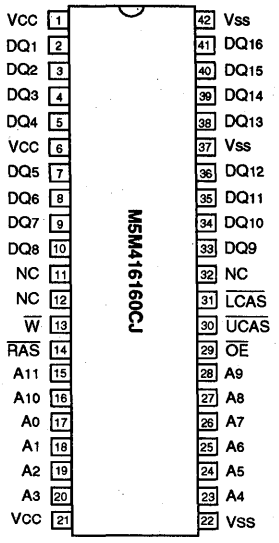
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

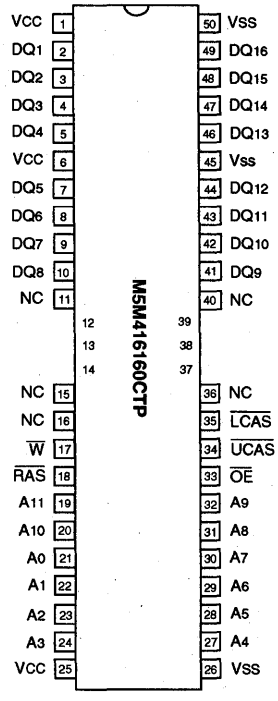
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe Input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

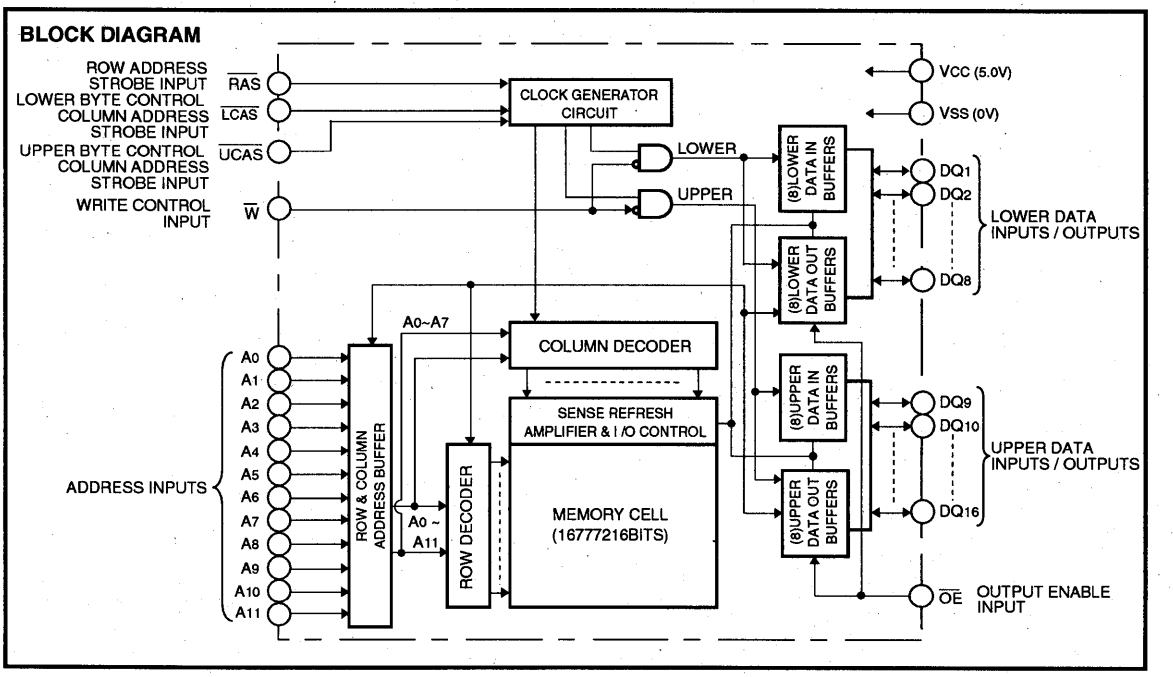
The M5M416160CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1～7	V
V_I	Input voltage		-1～7	V
V_O	Output voltage		-1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to VSS.

ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M416160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc -0.2V output open			1	
						0.3*	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M416160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-page-mode (Note 3,4,5)	M5M416160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M416160C-6,-6S				70	
		M5M416160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M416160C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0～A11≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125μs, t_{RAS}=t_{RASmin}～1μs			600	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M416160C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

MITSUBISHI ELECTRIC

PRELIMINARY
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CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.4V(V_{OH}) and 0.4V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq | \pm 10\ \mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

PRELIMINARY
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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧tRCD(max) and tASC ≧tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 25)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

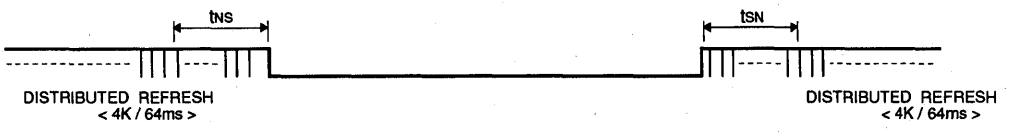
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M416160C-5S		M5M416160C-6S		M5M416160C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

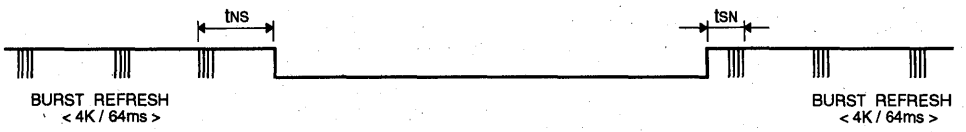
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦64ms and tSN≦64ms.



(2) In case of burst refresh

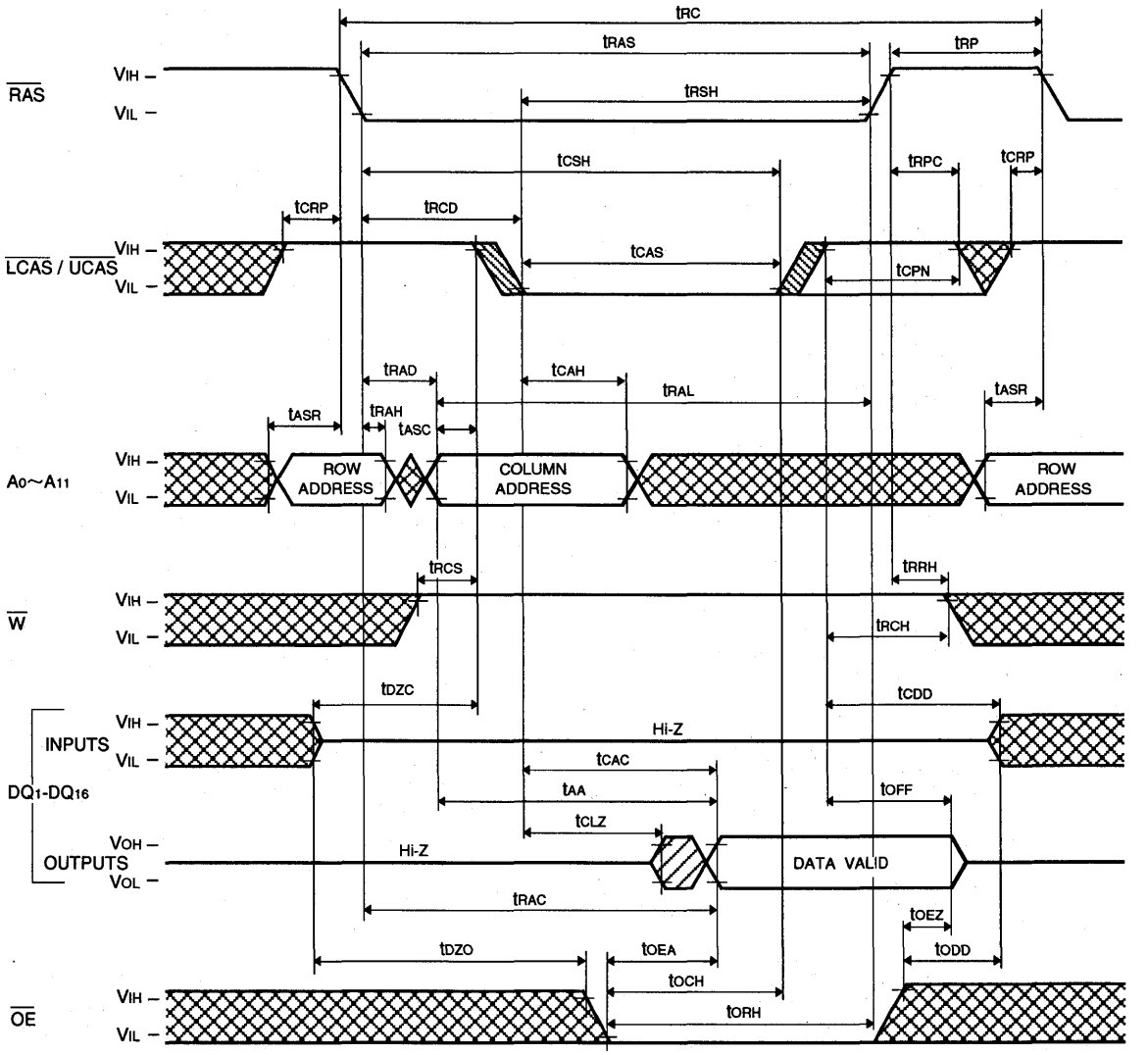
The last / first full refresh cycles (4K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦64ms.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 28)

Read Cycle



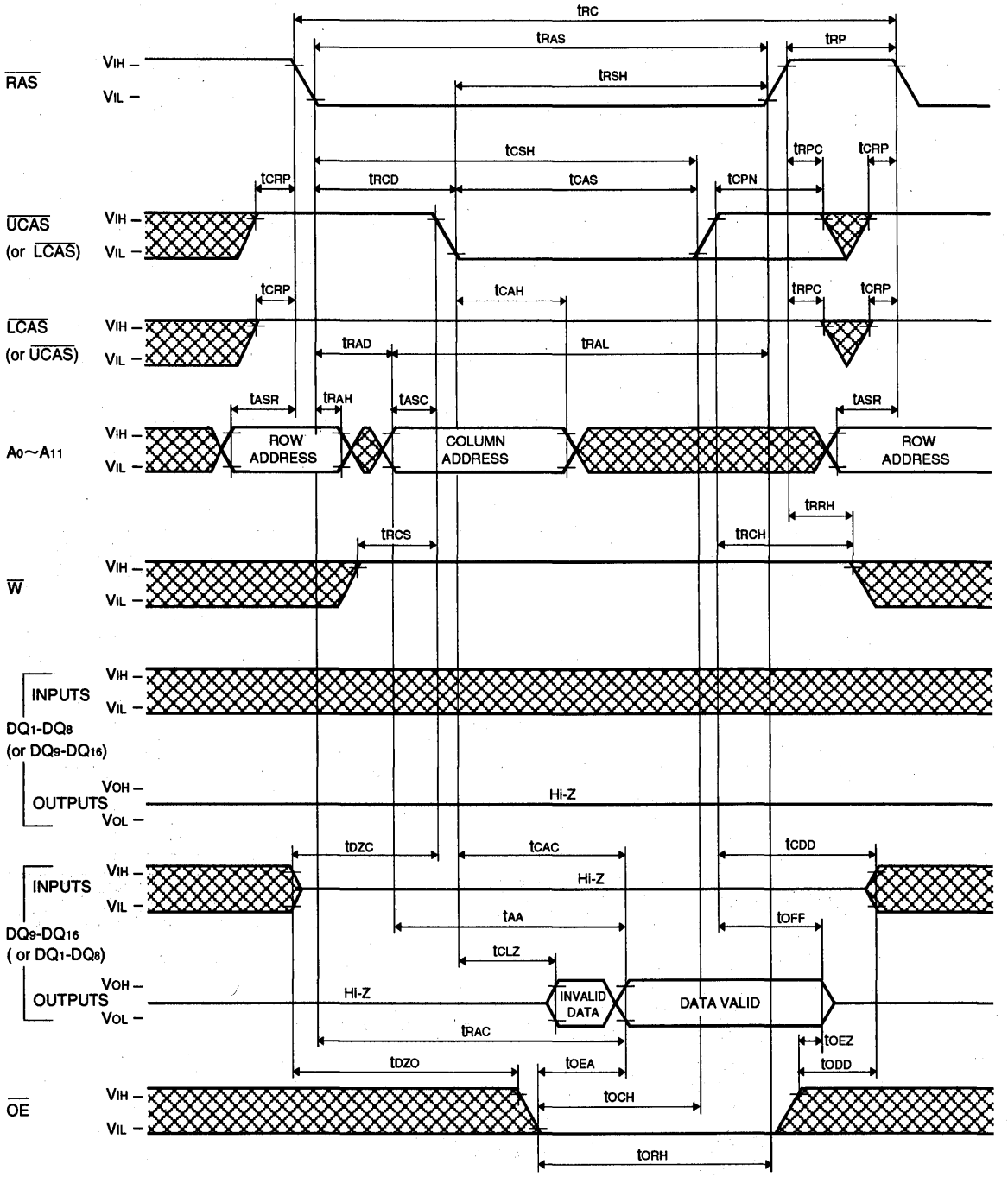
Note 28

Indicates the don't care input.
VIH(min.) ≦ VIN ≦ VIH(max) or VIL(min.) ≦ VIN ≦ VIL(max)

Indicates the invalid output.

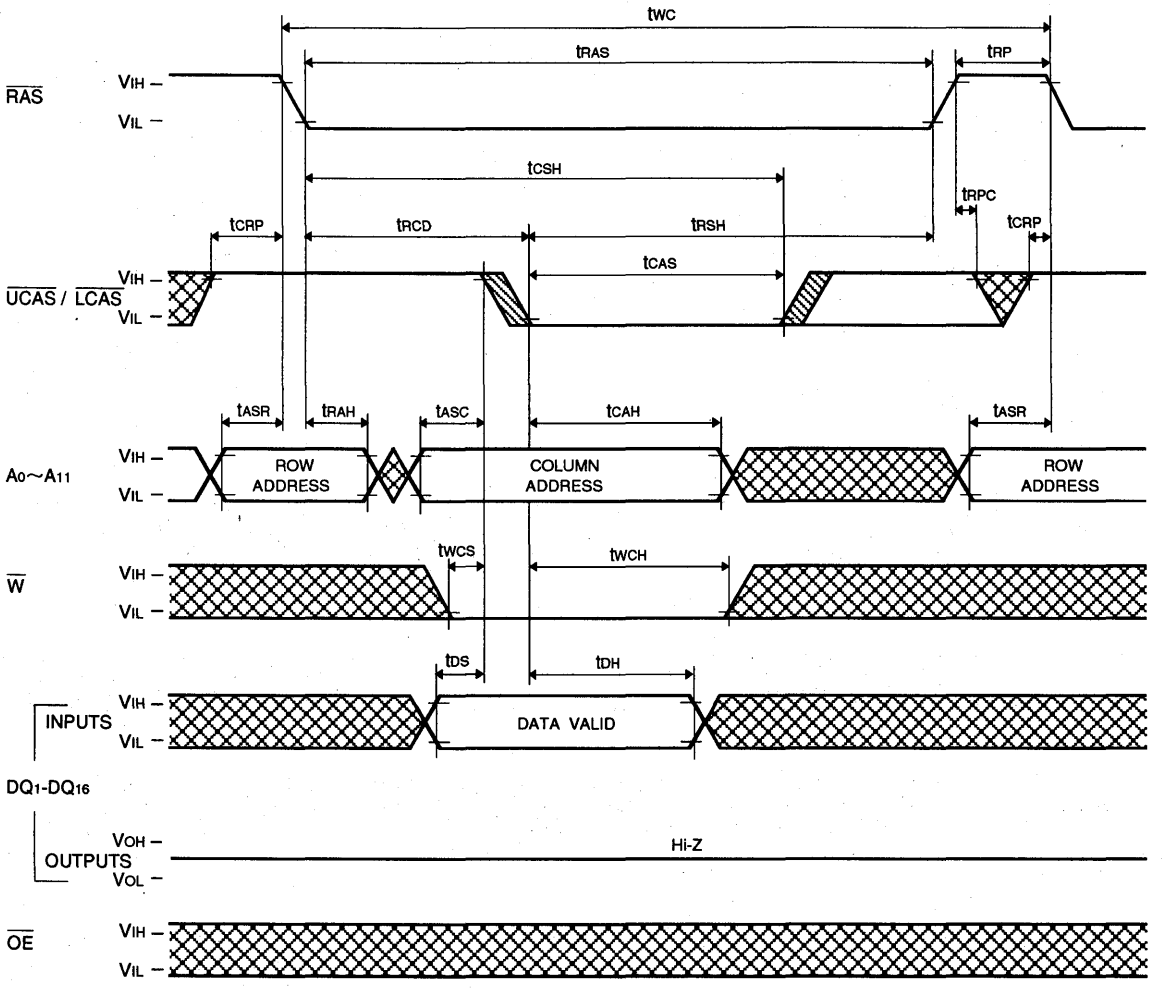
Indicates the skew of the two inputs.

Upper / (Lower) Byte Read Cycle

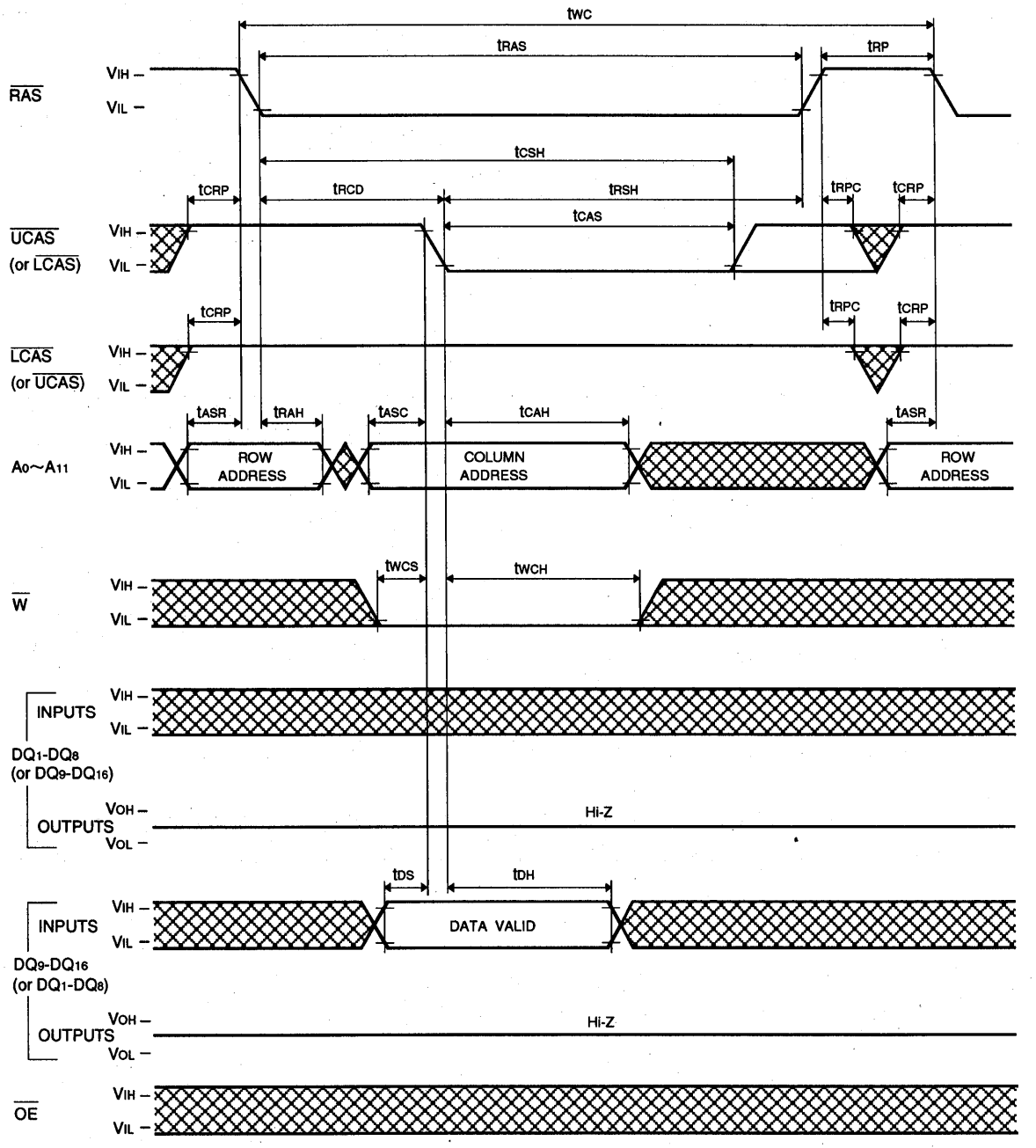


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early write)

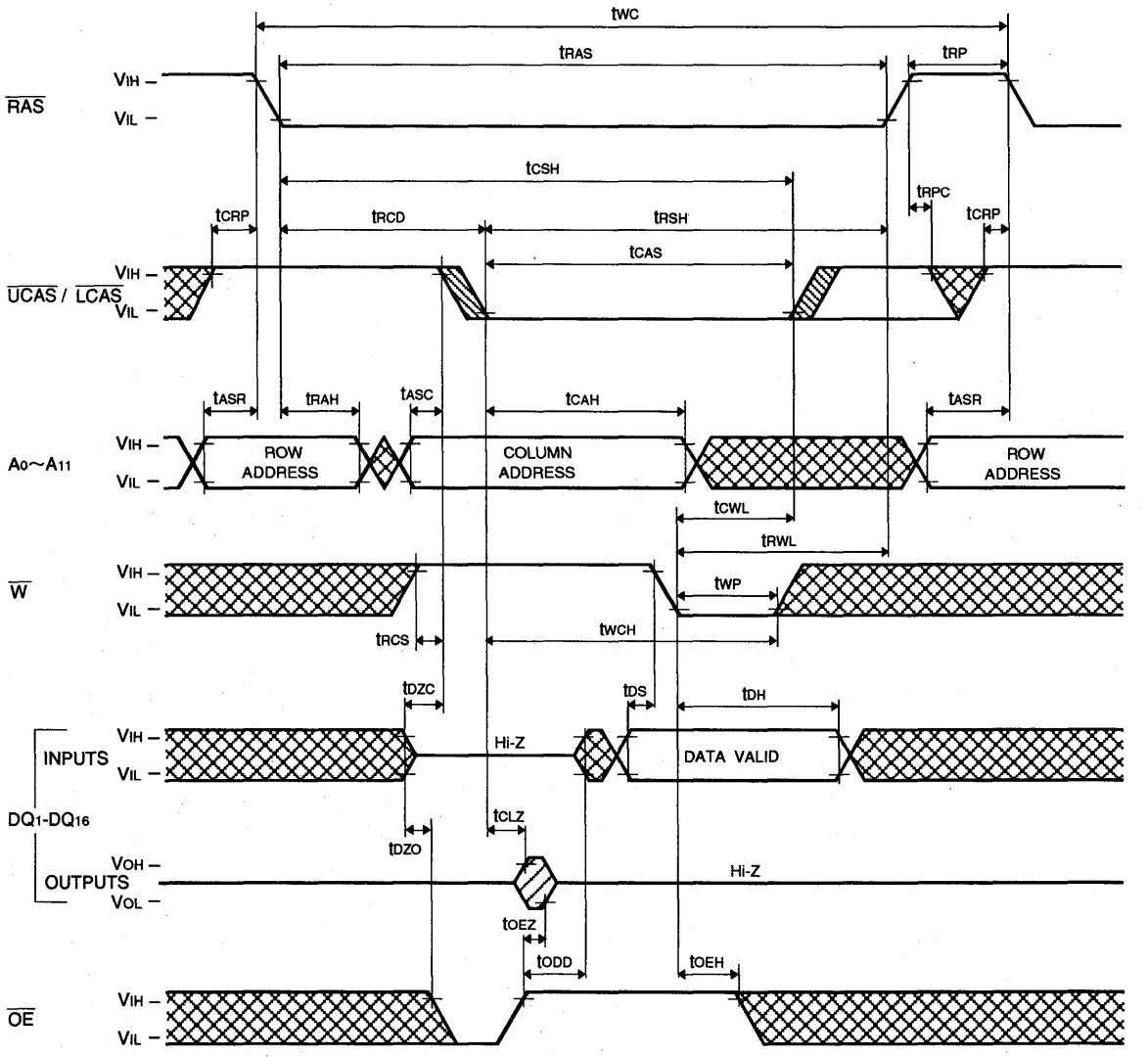


Upper / (Lower) Byte Write Cycle (Early write)

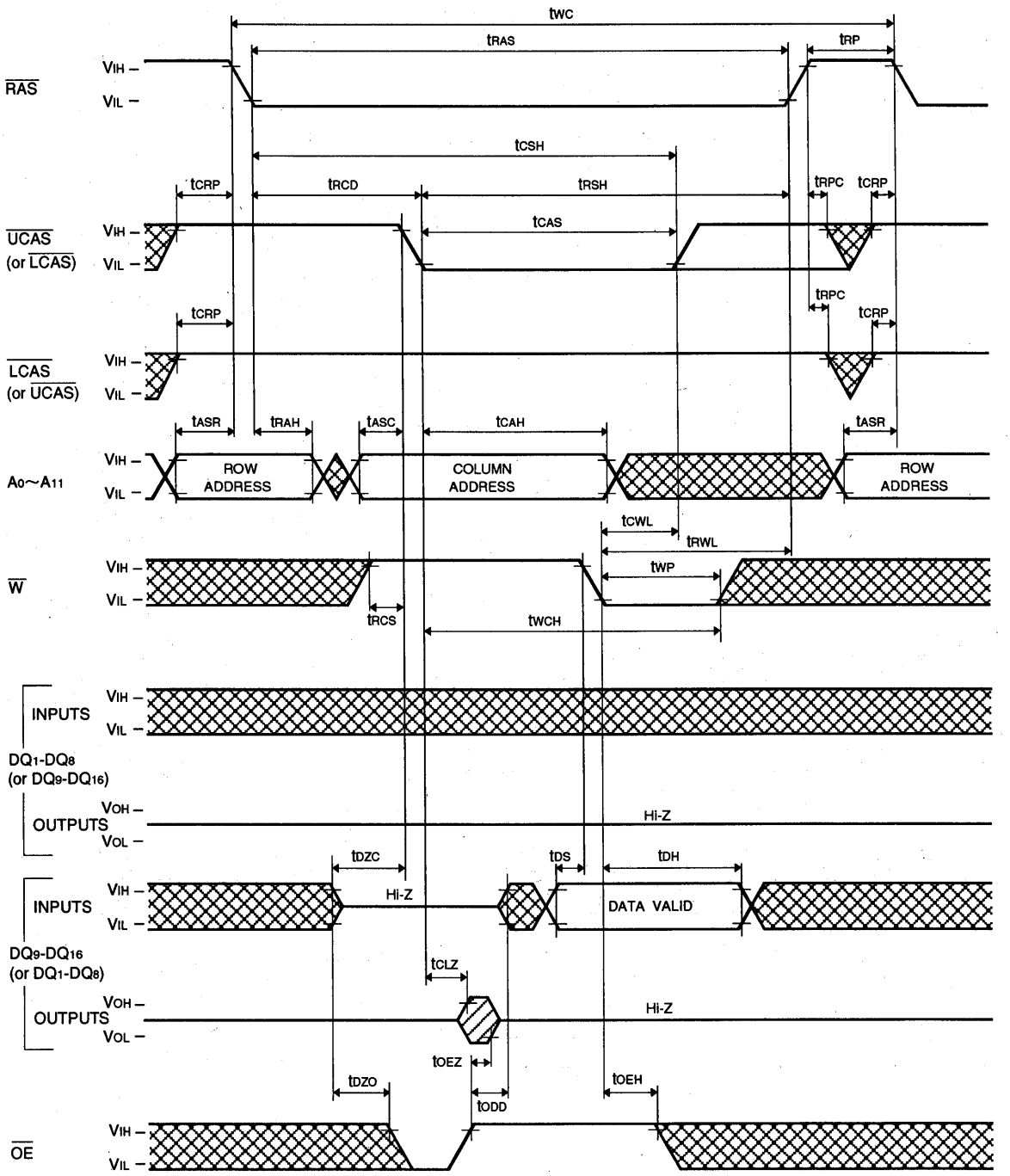


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Delayed write)

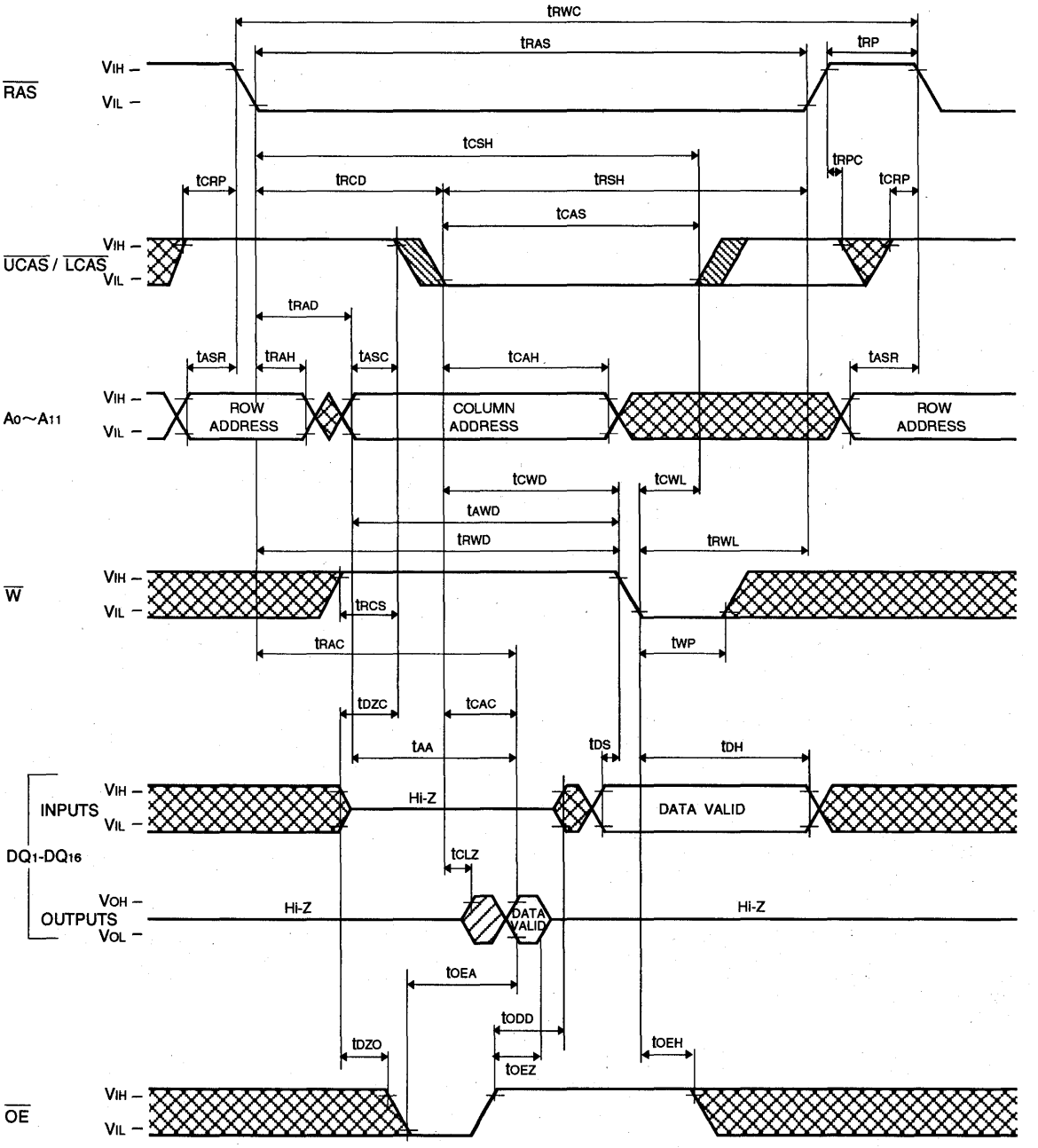


Upper / (Lower) Byte Write Cycle (Delayed write)



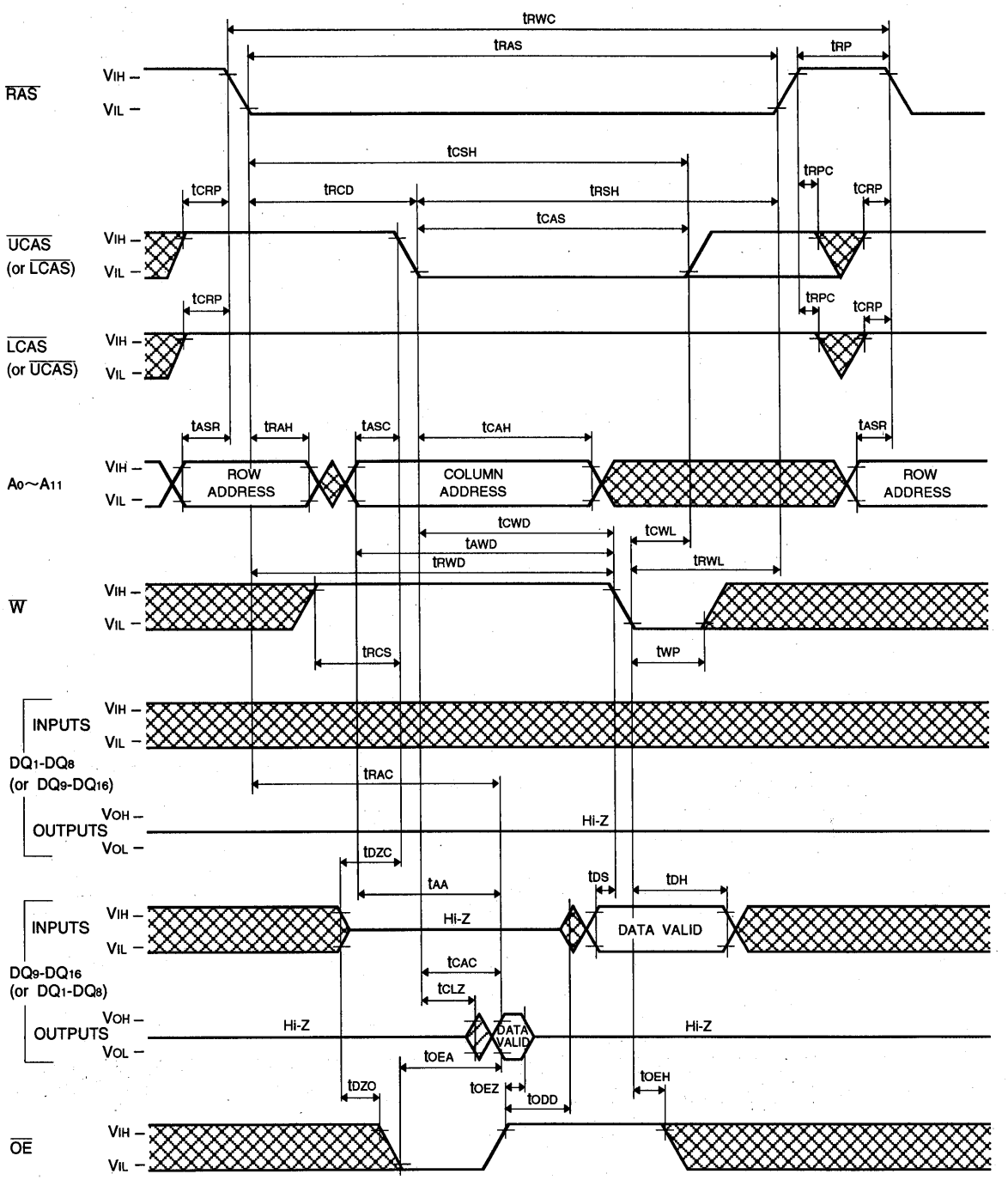
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle



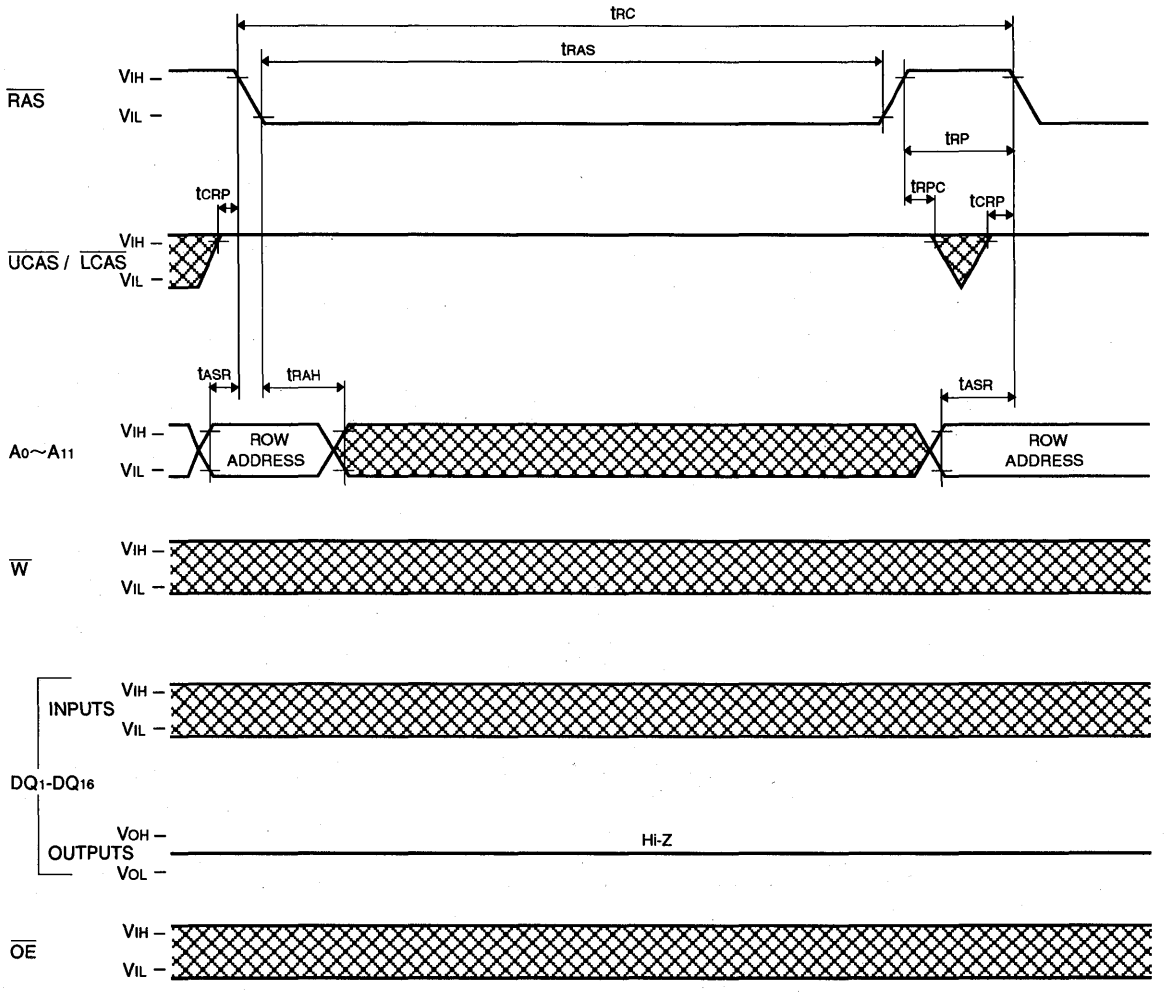
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle

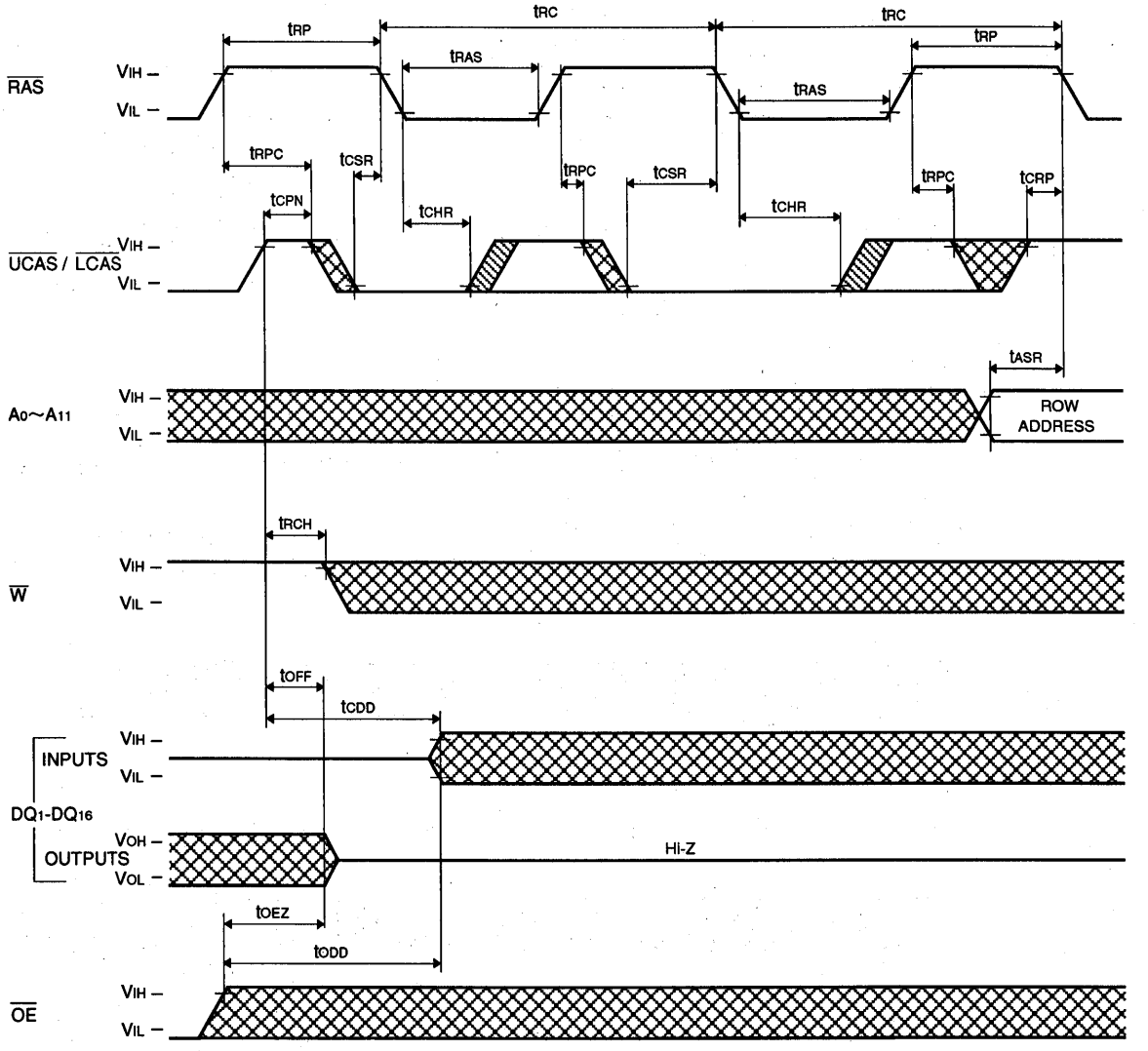


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle

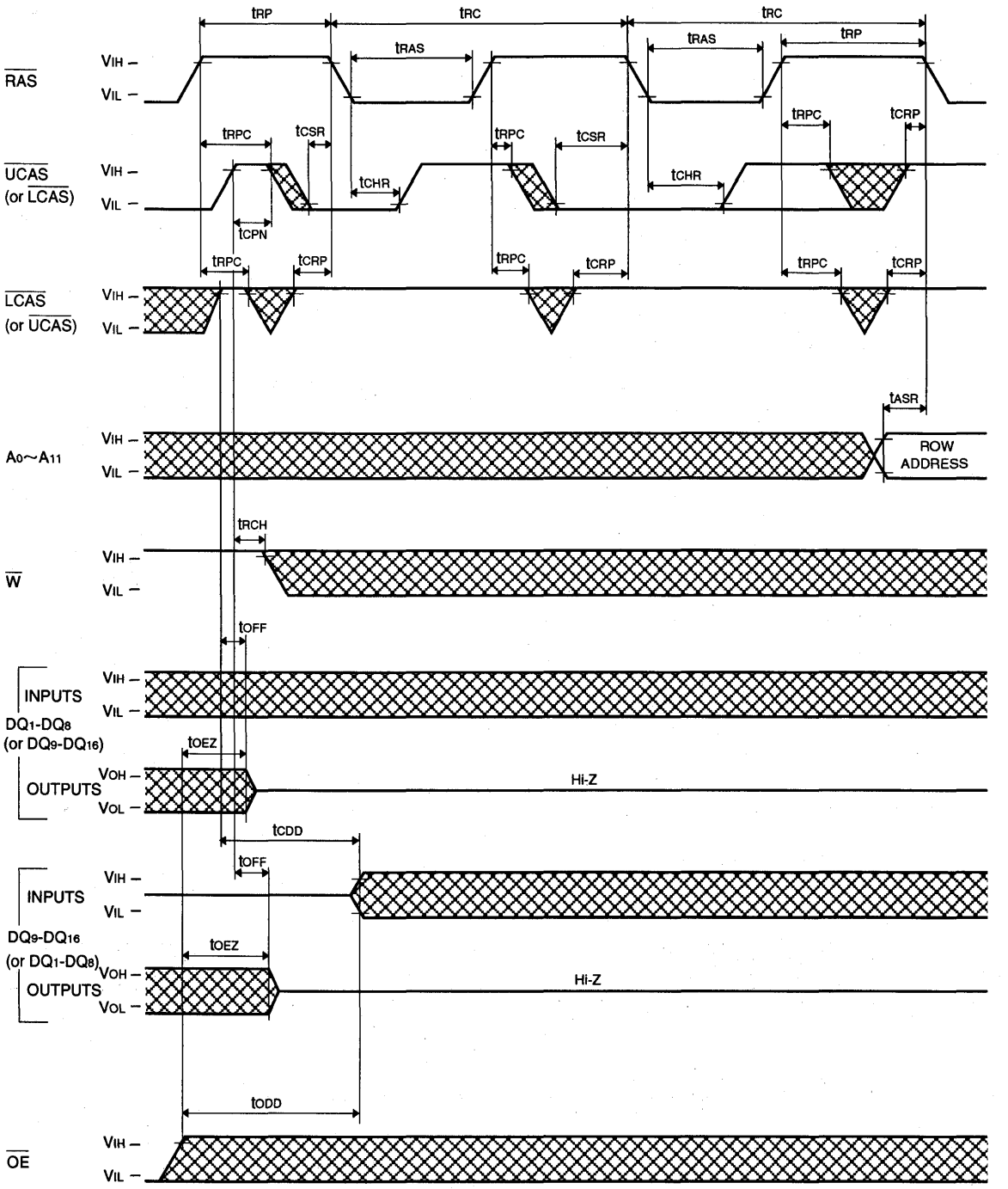


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

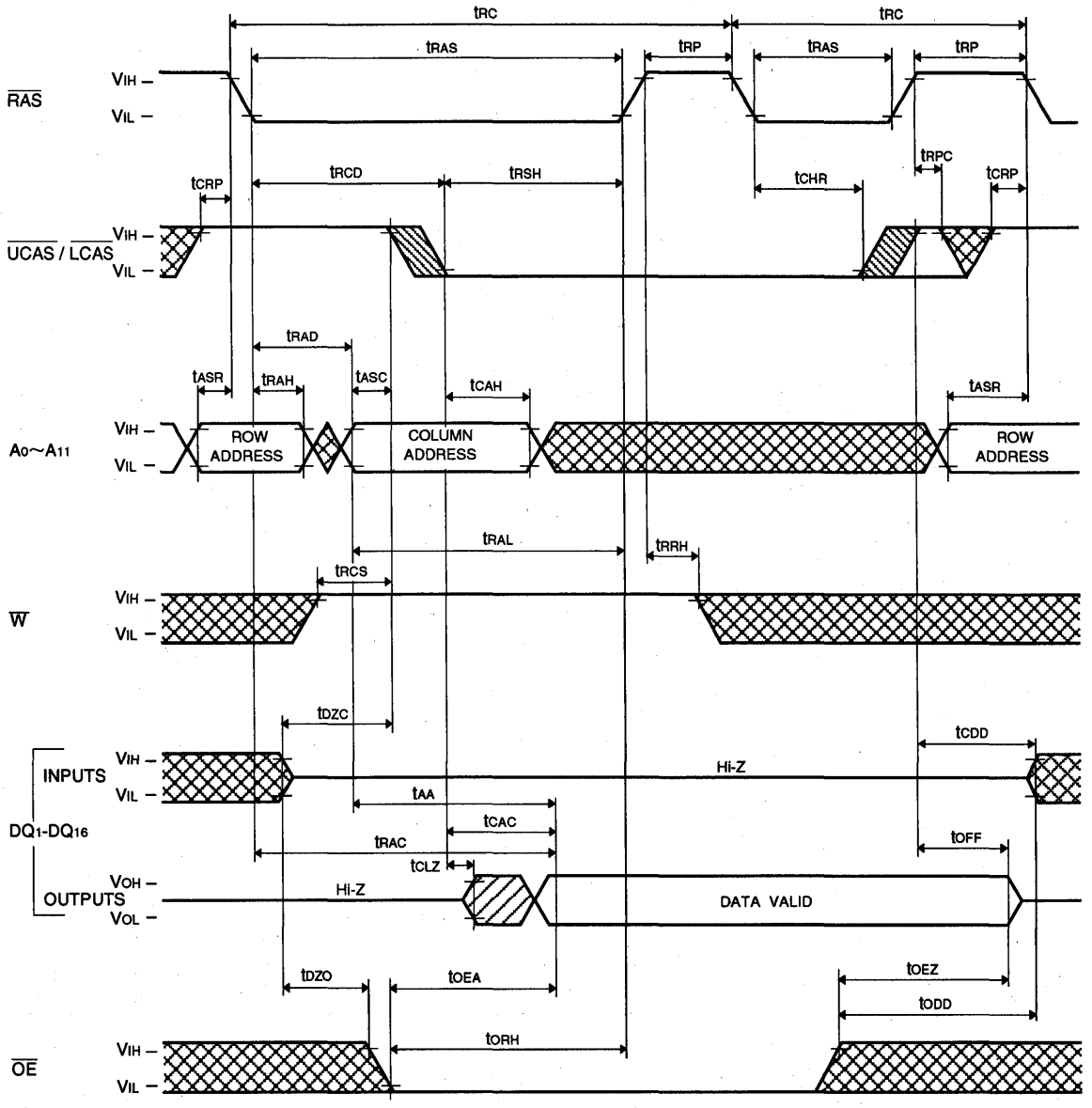


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



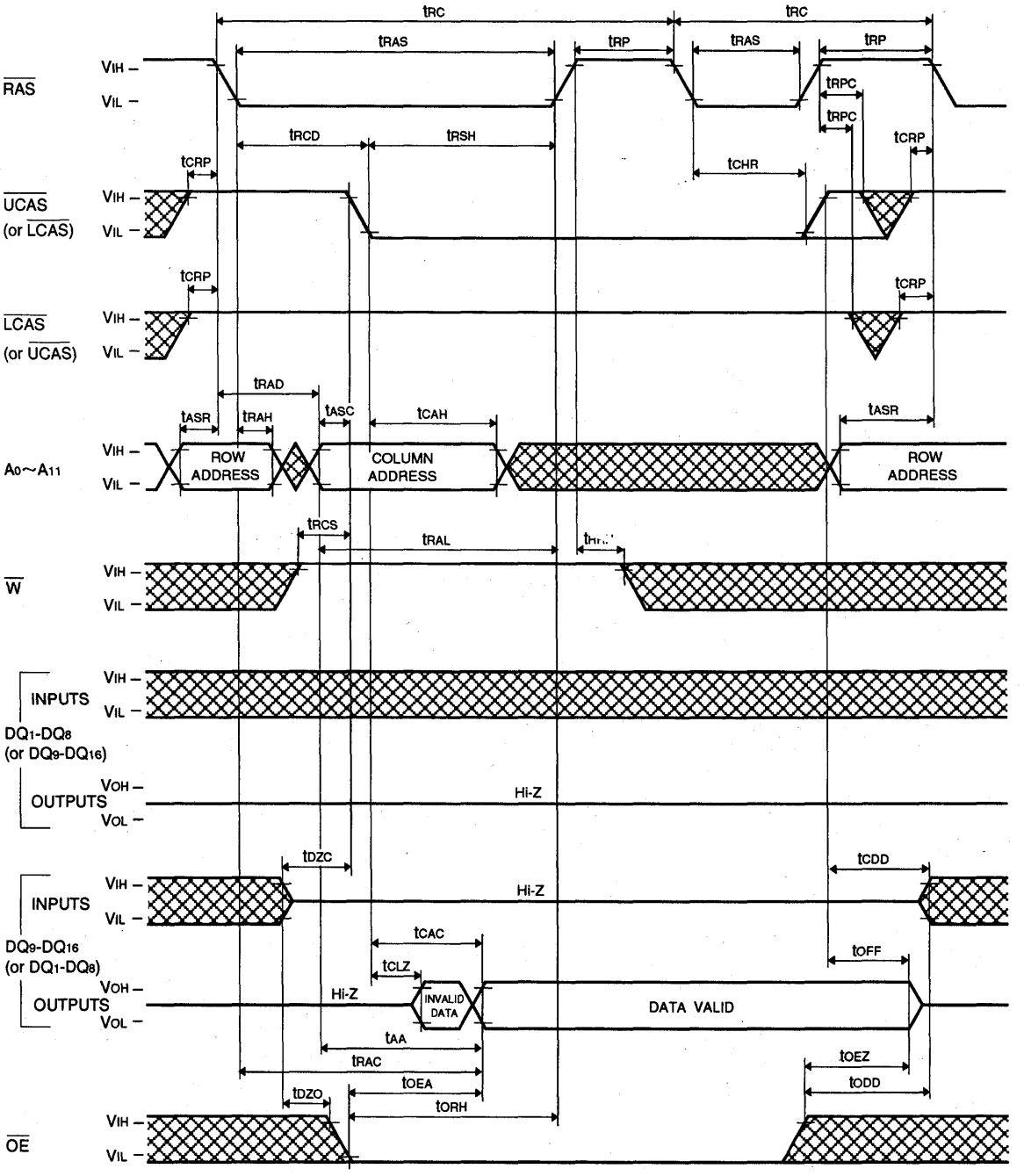
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

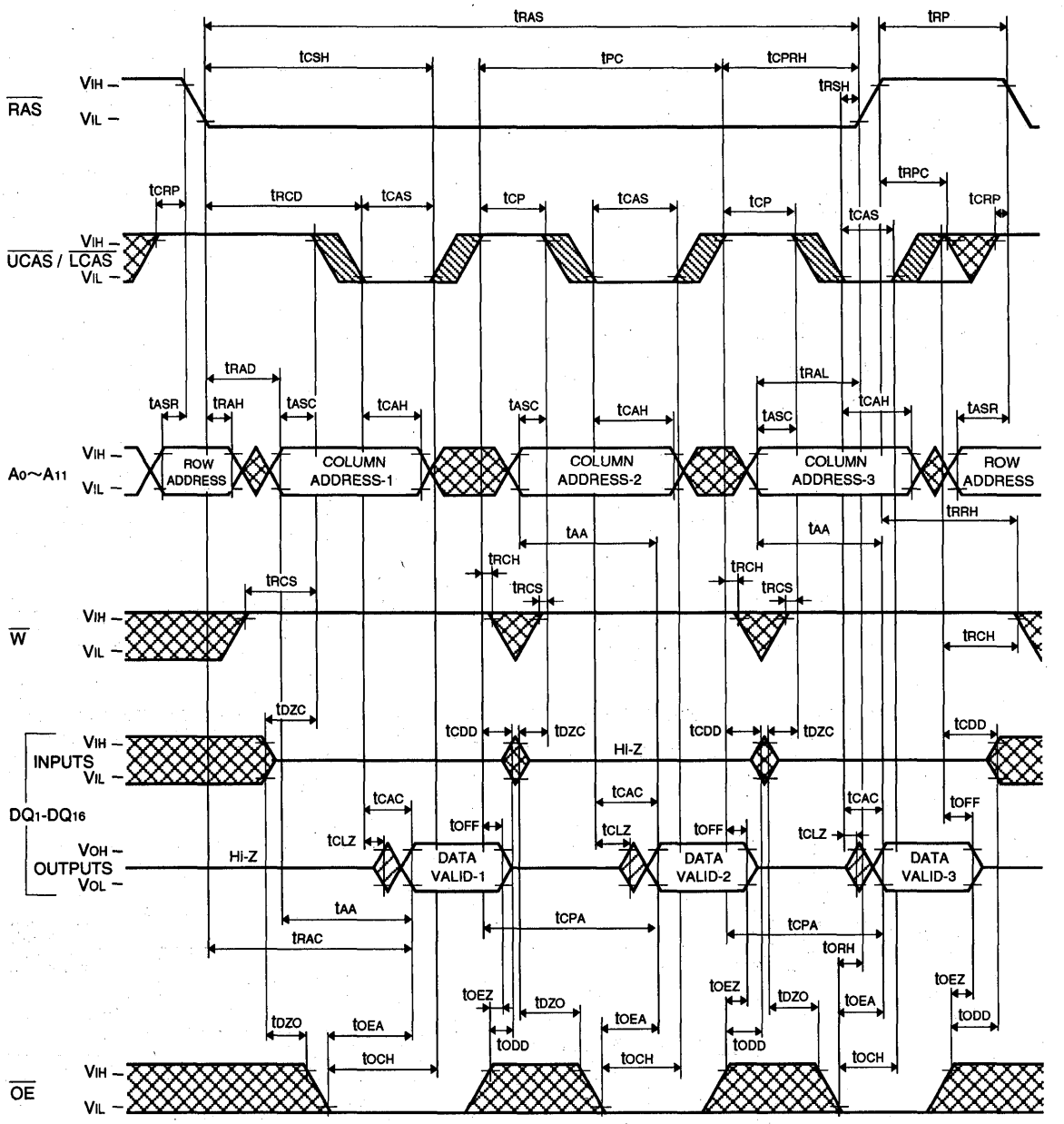
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



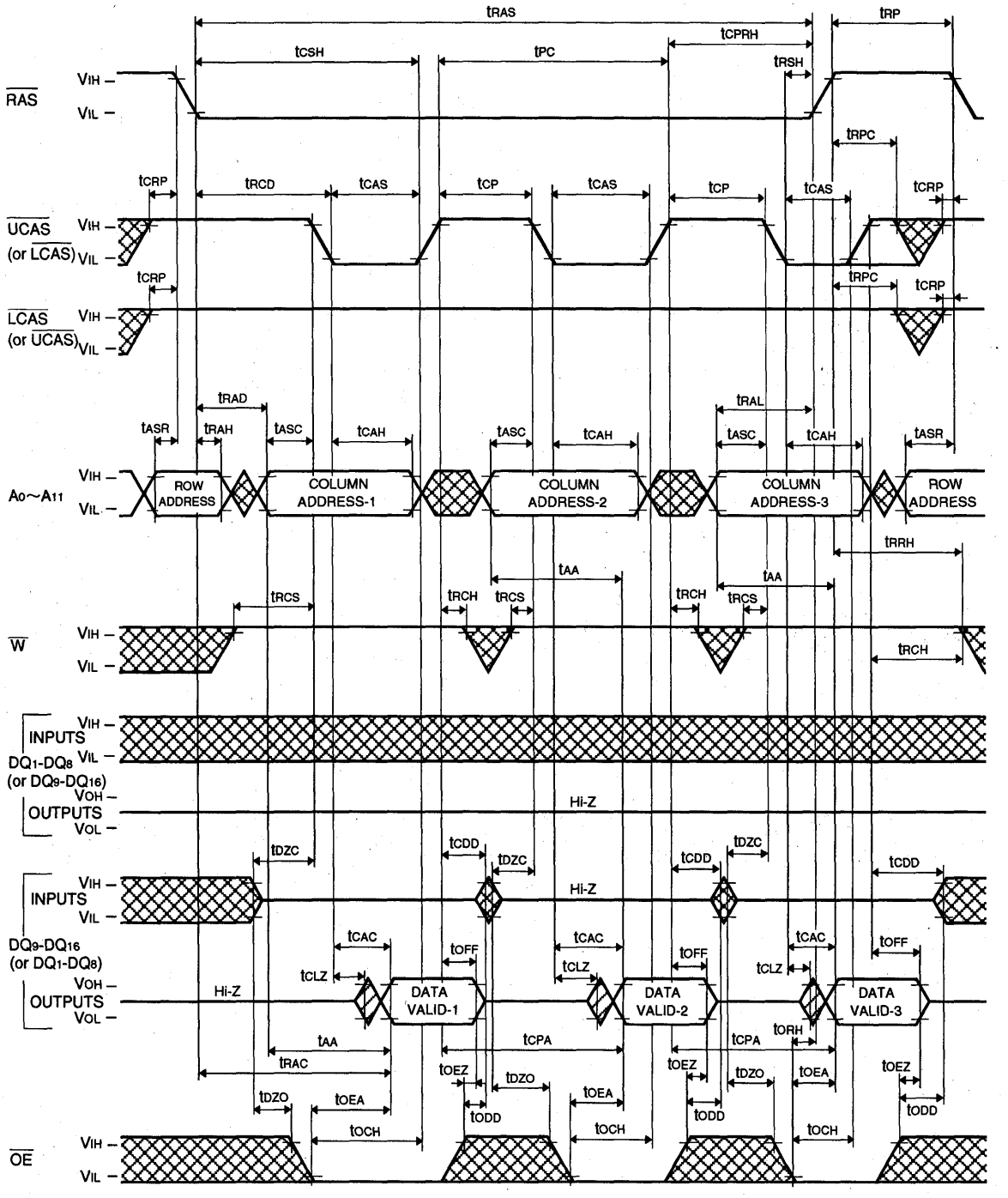
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle

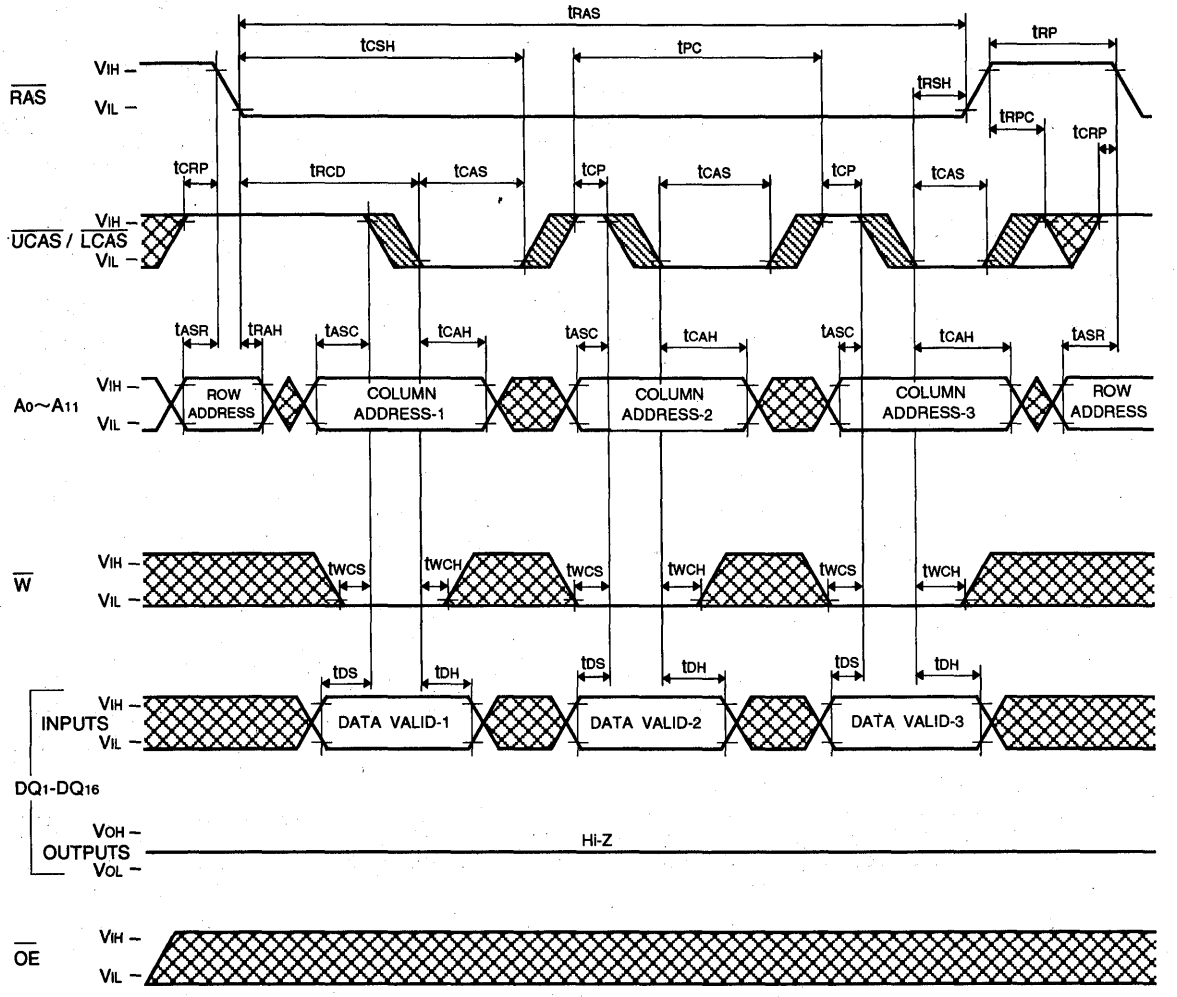


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Fast Page Mode Read Cycle

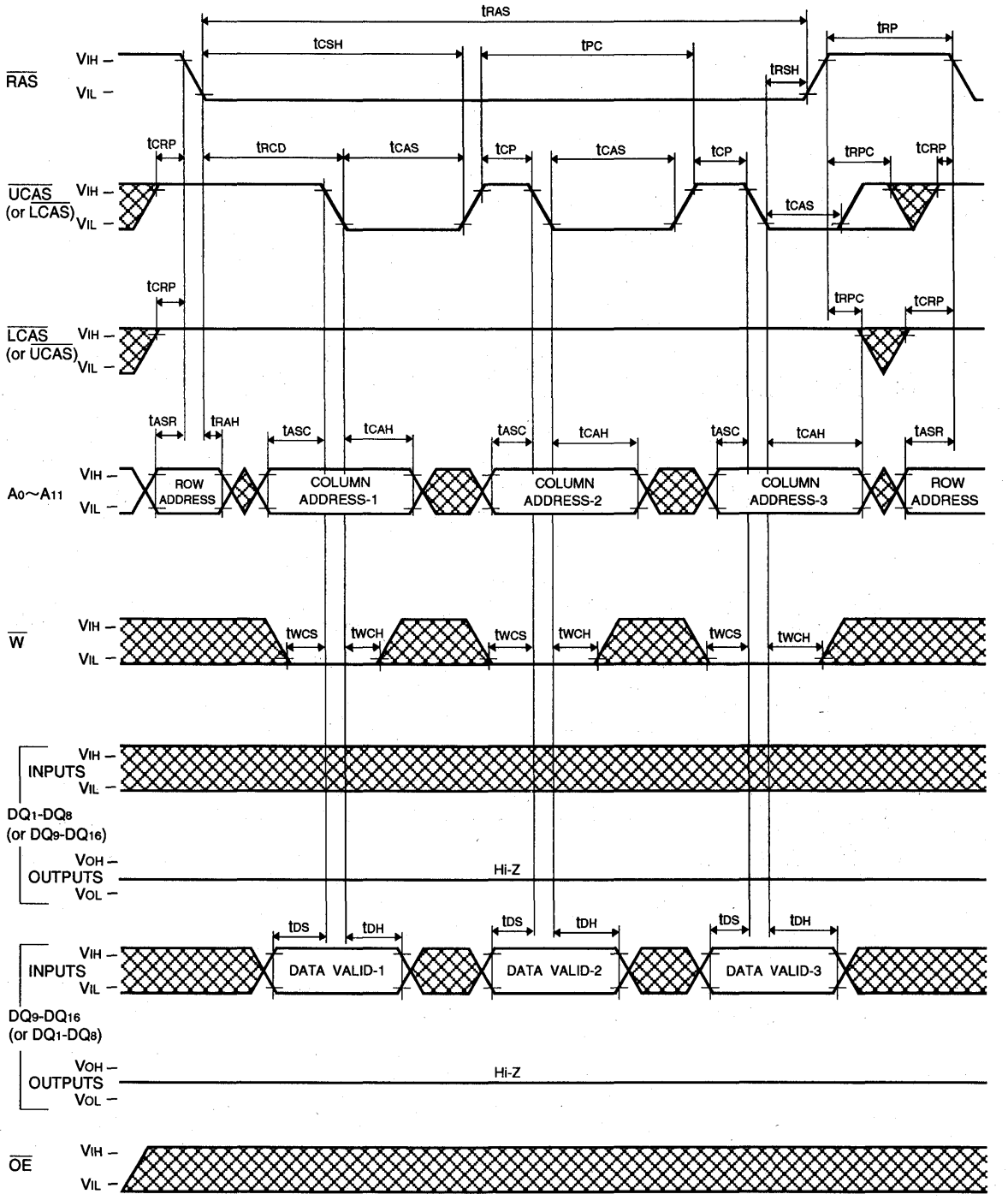


Fast Page Mode Write Cycle (Early Write)

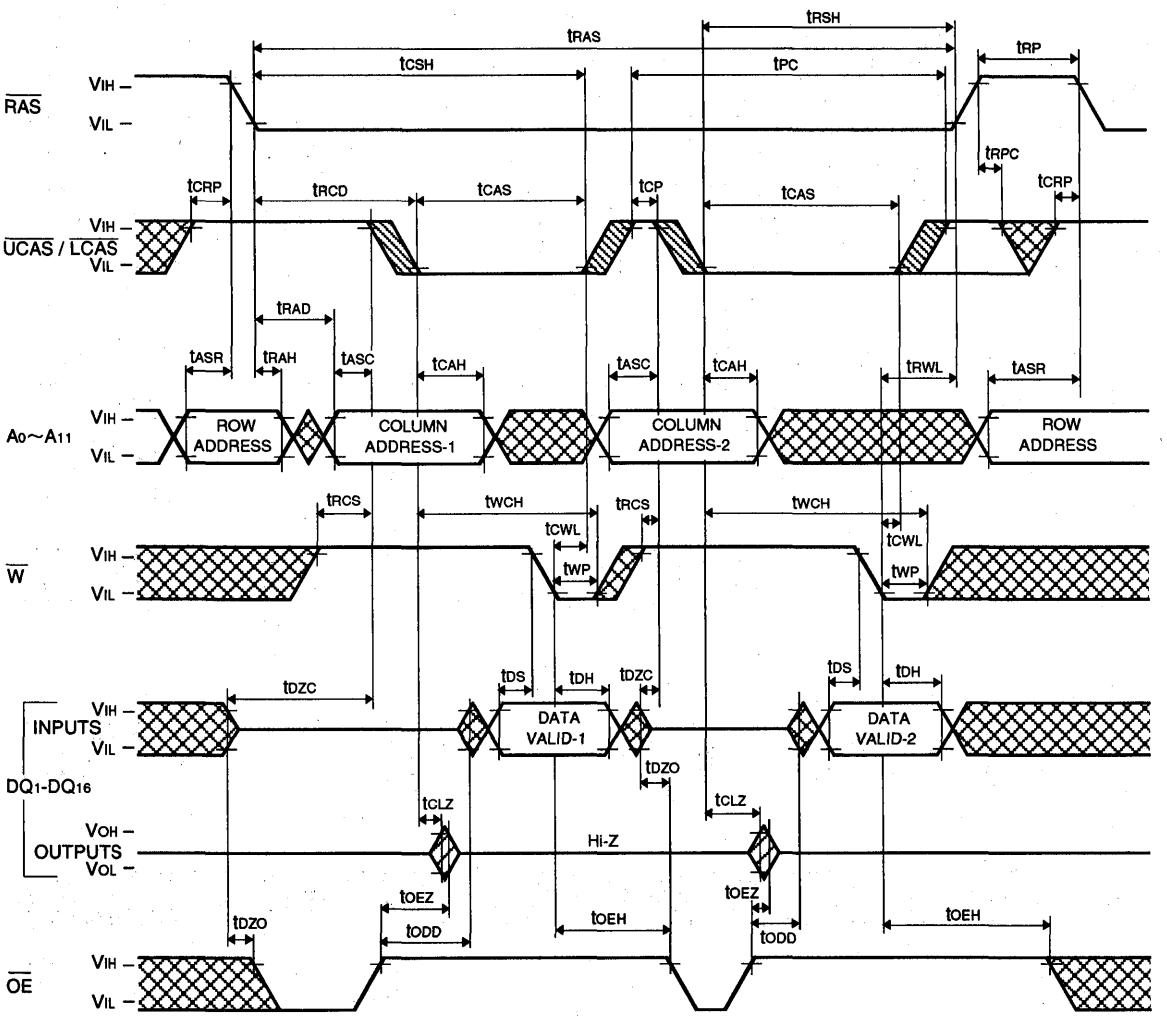


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)

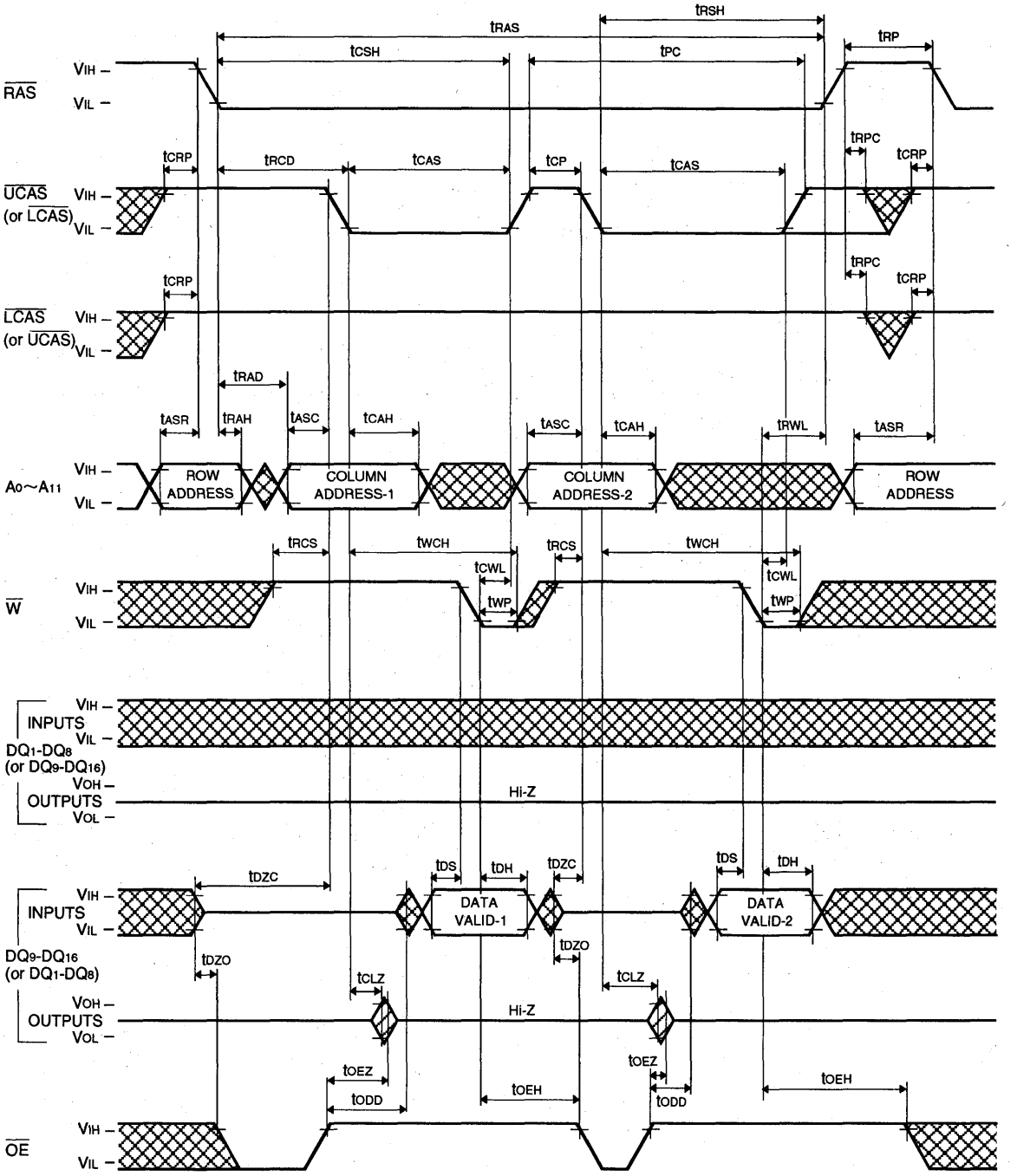


Fast Page Mode Write Cycle (Delayed Write)

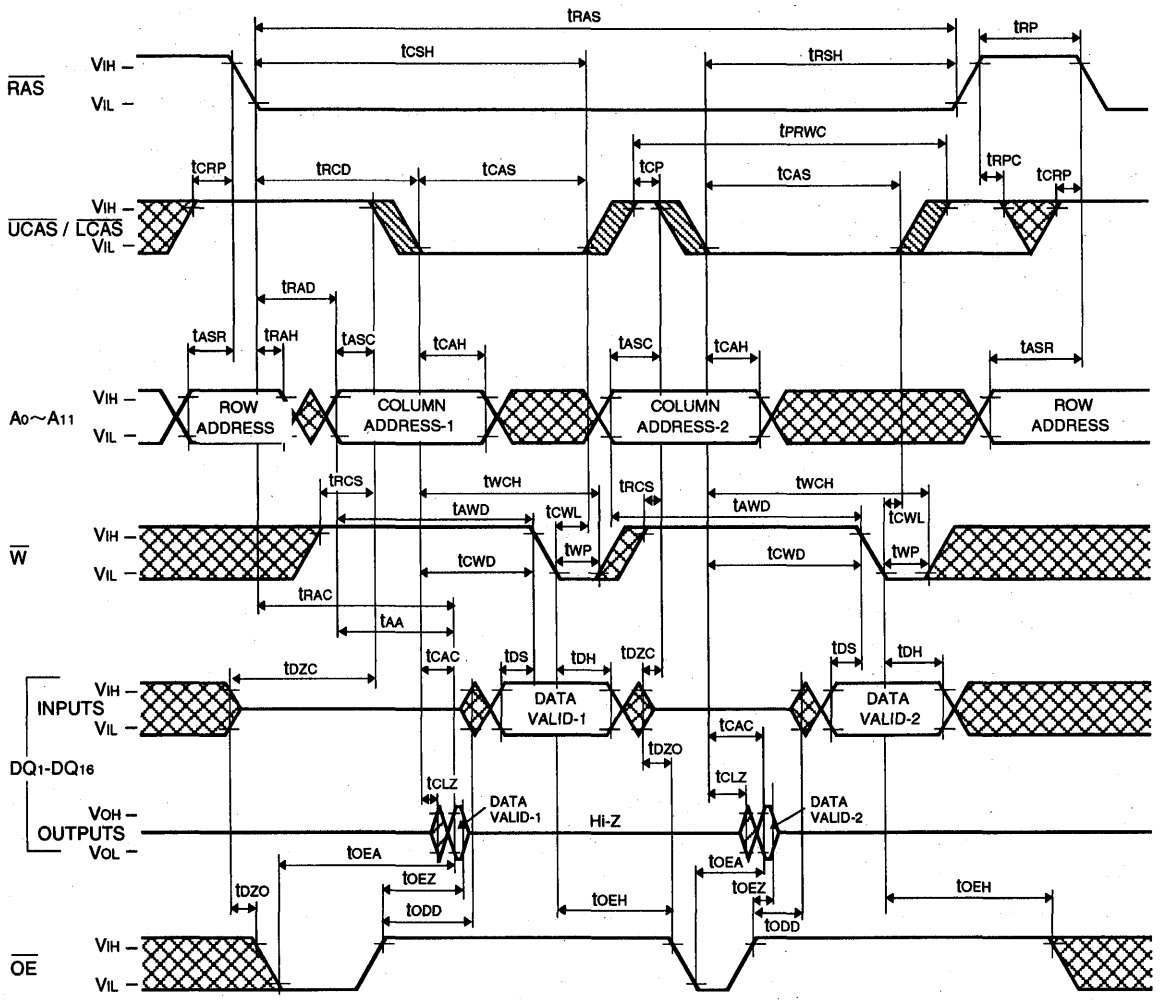


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)

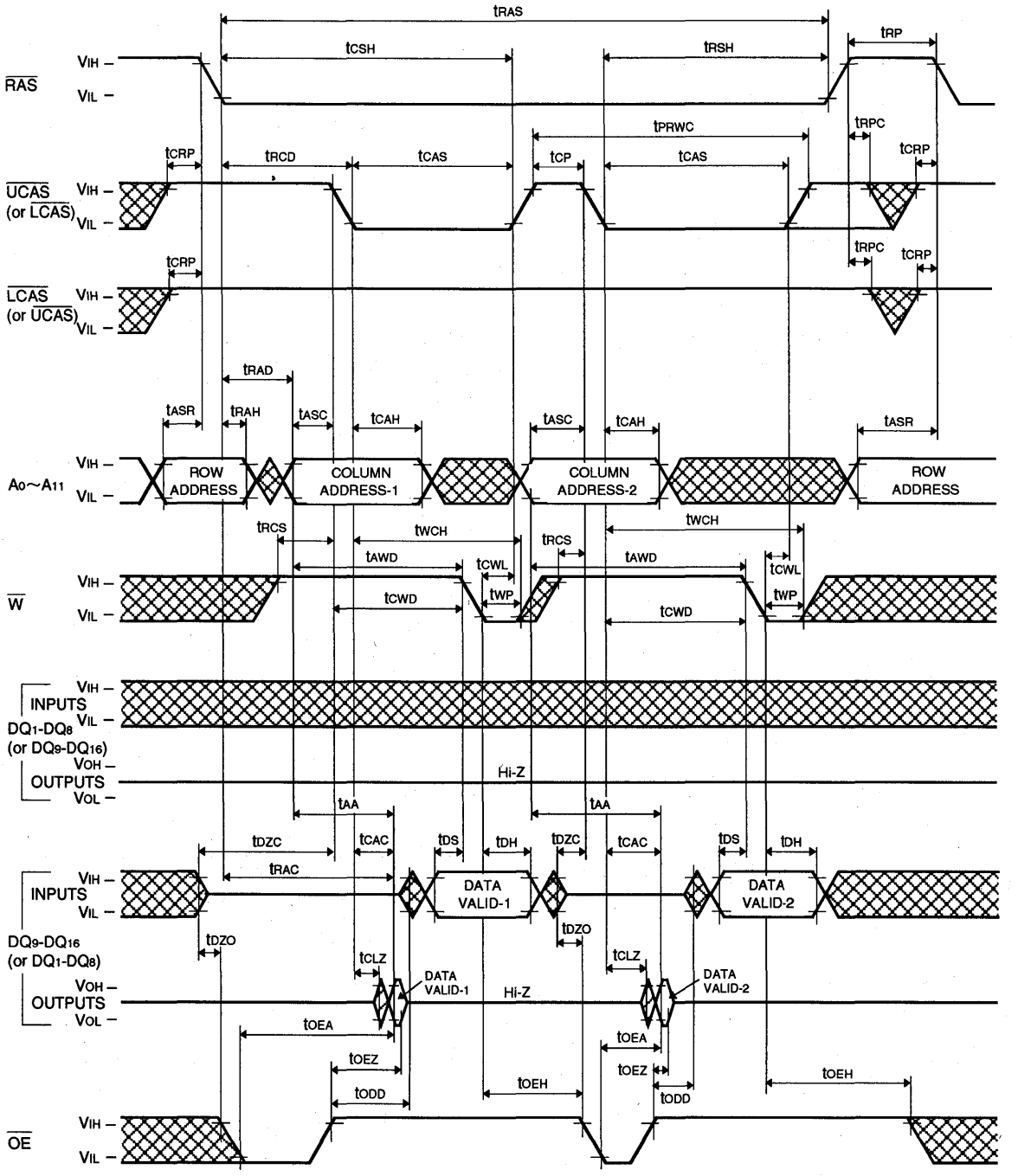


Fast Page Mode Read-Write, Read-Modify-Write Cycle

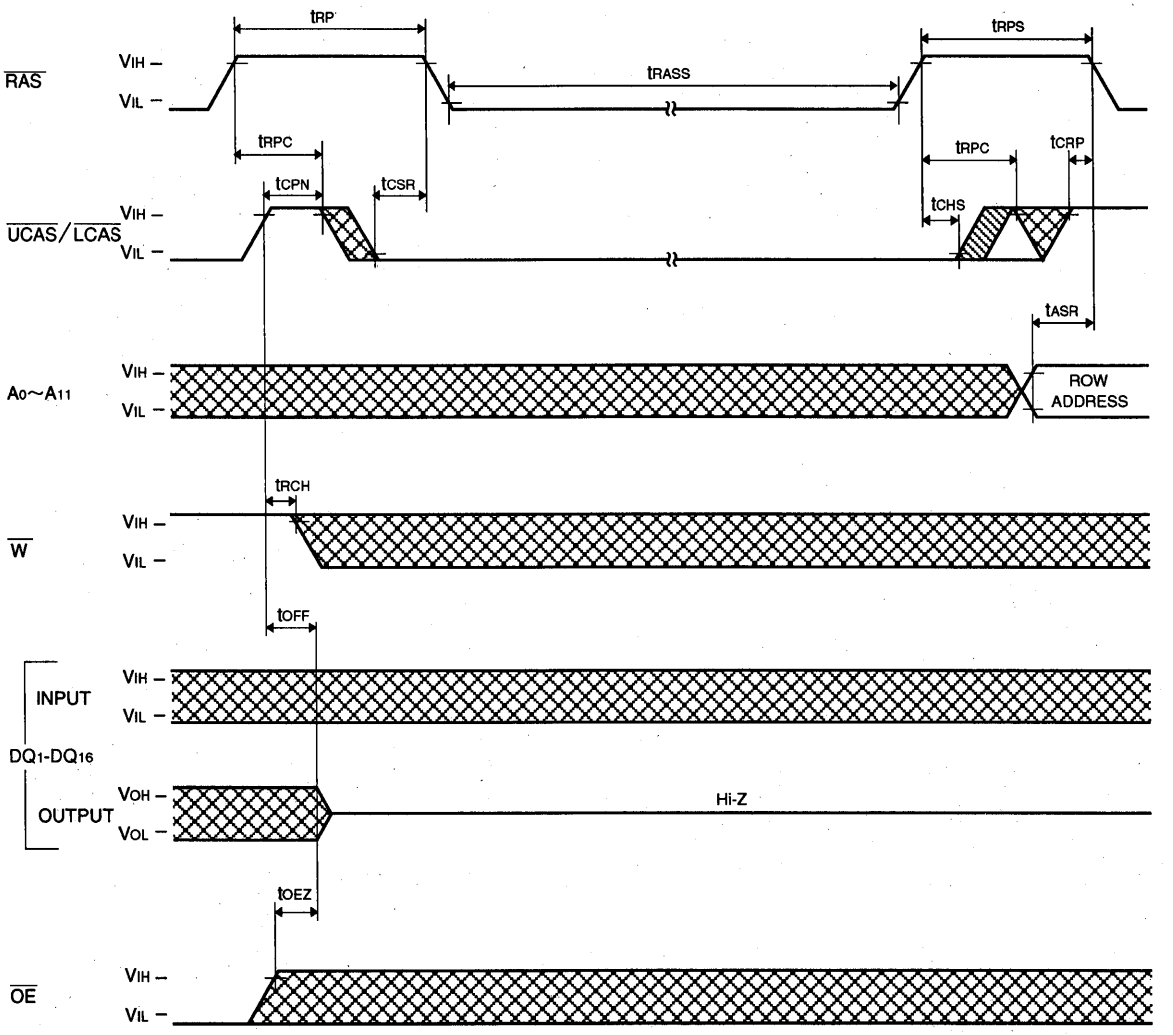


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

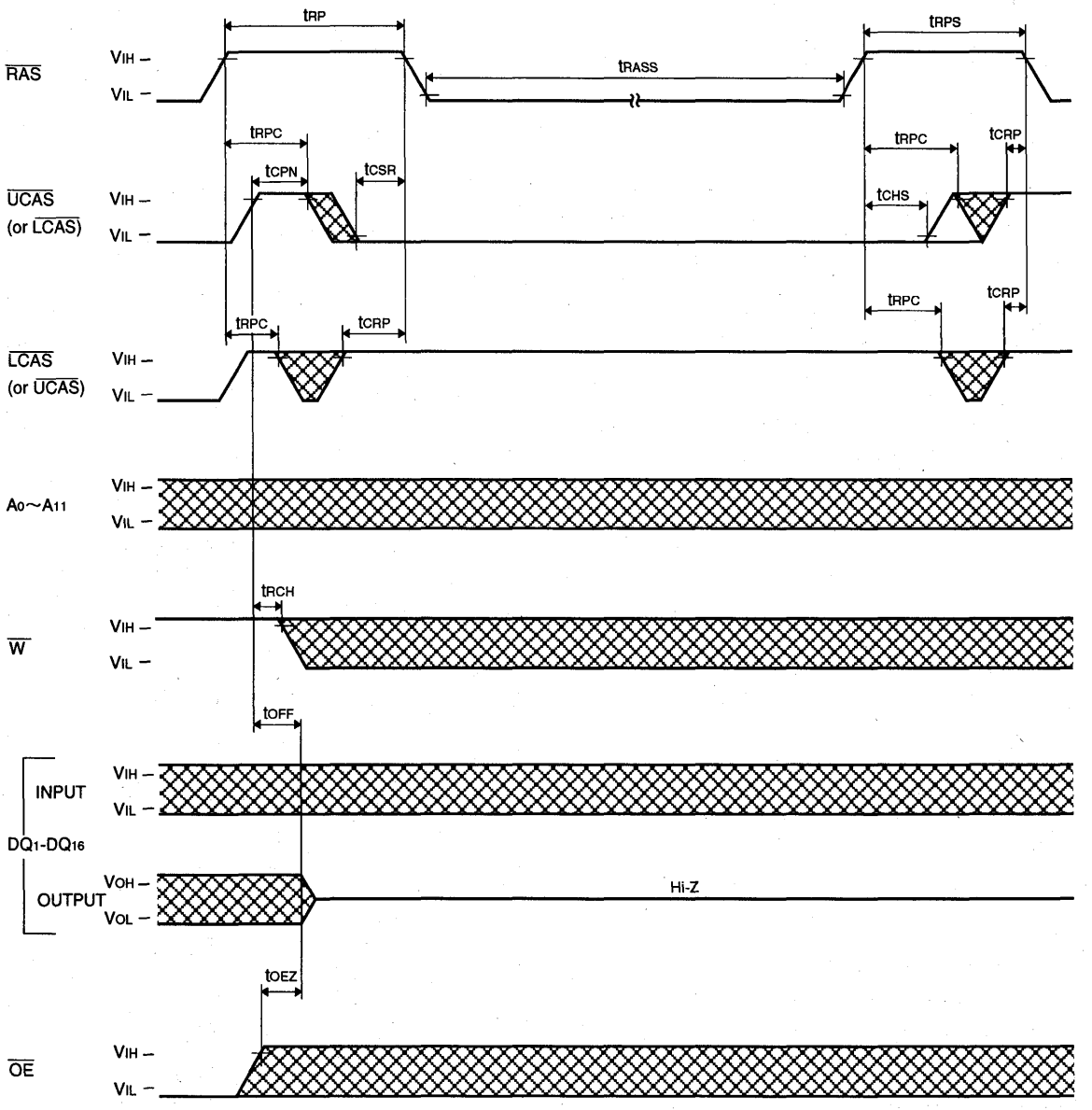
Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



Self Refresh Cycle∗



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418160CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418160CXX-5,-5S	50	13	25	13	90	810
M5M418160CXX-6,-6S	60	15	30	15	110	675
M5M418160CXX-7,-7S	70	20	35	20	130	585

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M418160Cxx-5,-5S ---------- 990.0mW (Max)
  M5M418160Cxx-6,-6S ---------- 825.0mW (Max)
  M5M418160Cxx-7,-7S ---------- 715.0mW (Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  * : Applicable to self refresh version (M5M418160CJ,TP-5S,-6S, -7S : option) only

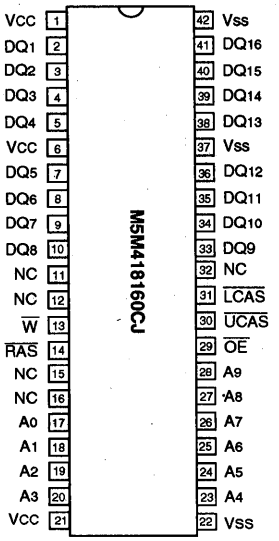
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

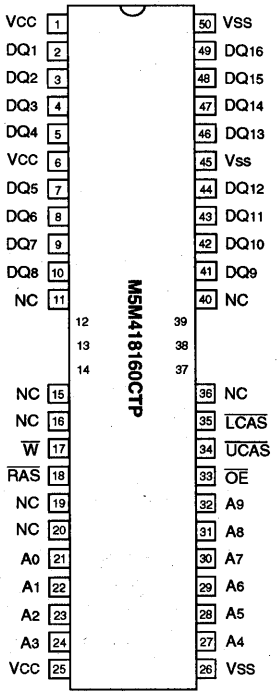
PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418160CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

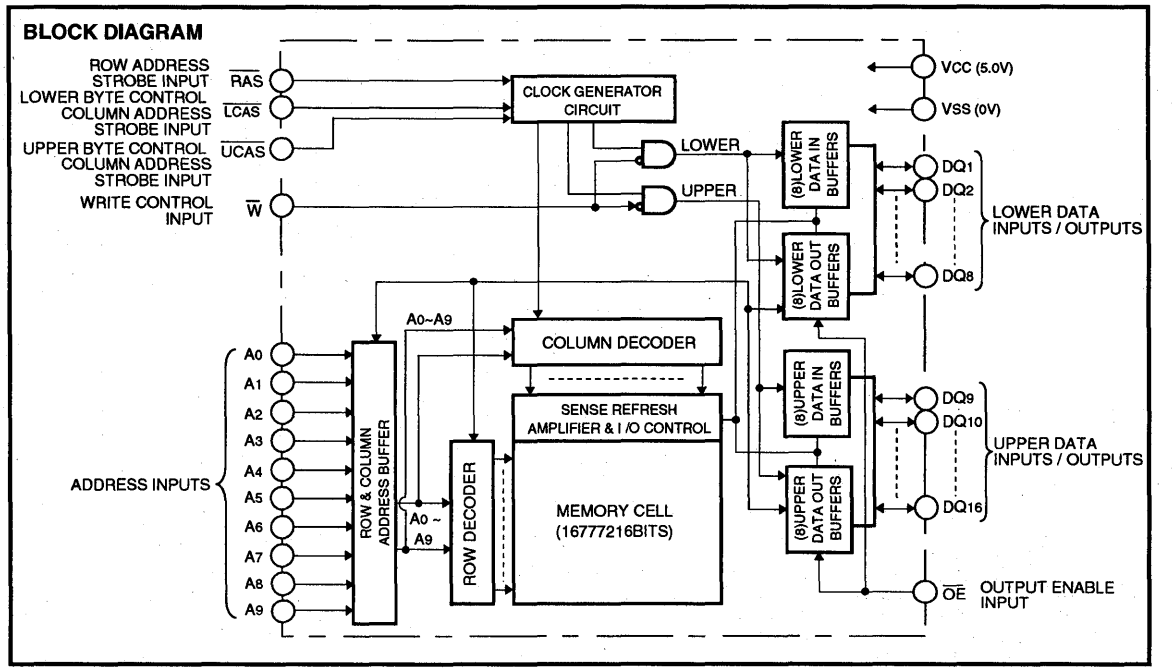
The M5M418160CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418160CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1~7	V
V_I	Input voltage		-1~7	V
V_O	Output voltage		-1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25 °C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to VSS.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M418160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M418160C-6,-6S				150	
		M5M418160C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc -0.2V output open			1	
						0.3 *	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M418160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M418160C-6,-6S				150	
		M5M418160C-7,-7S				130	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-page-mode (Note 3,4,5)	M5M418160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M418160C-6,-6S				70	
		M5M418160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M418160C-6,-6S				150	
		M5M418160C-7,-7S				130	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M418160C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0~A9≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125μs, t_{RAS}=$t_{RASmin.}$~1μs			500	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M418160C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70 ℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted,see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.4V(V_{OH}) and 0.4V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note22)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

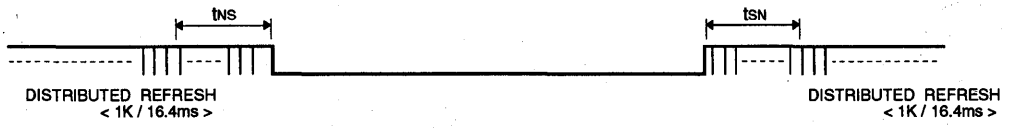
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418160C-5S		M5M418160C-6S		M5M418160C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

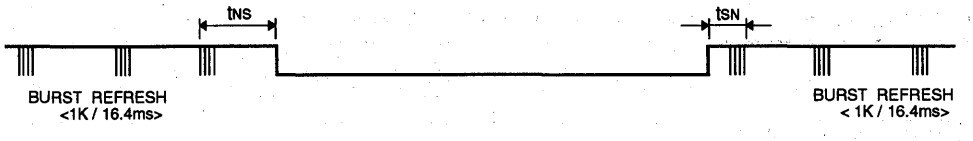
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦16.4ms and tSN≦16.4ms.



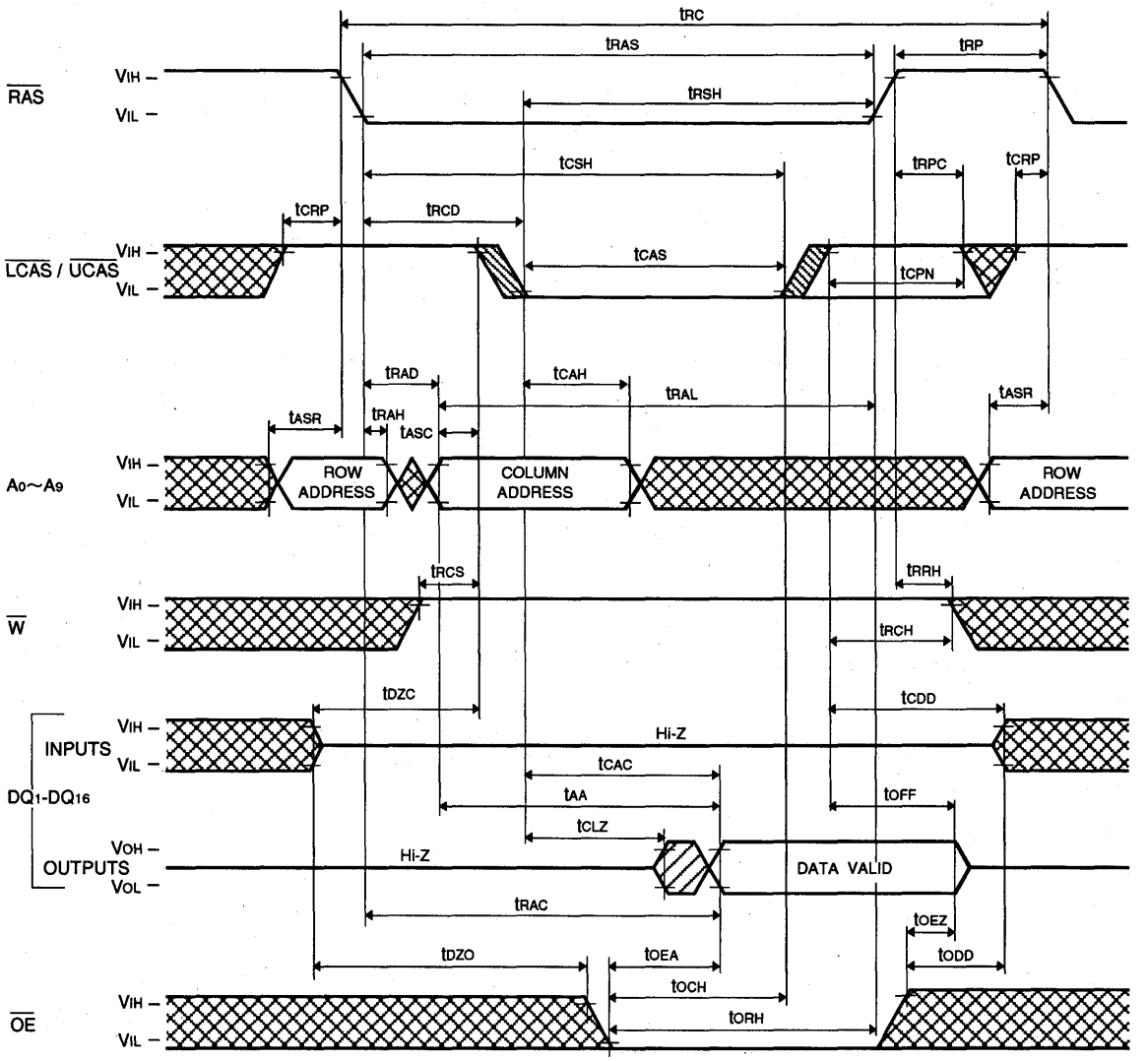
(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦16.4ms.



Timing Diagrams (Note 28)

Read Cycle



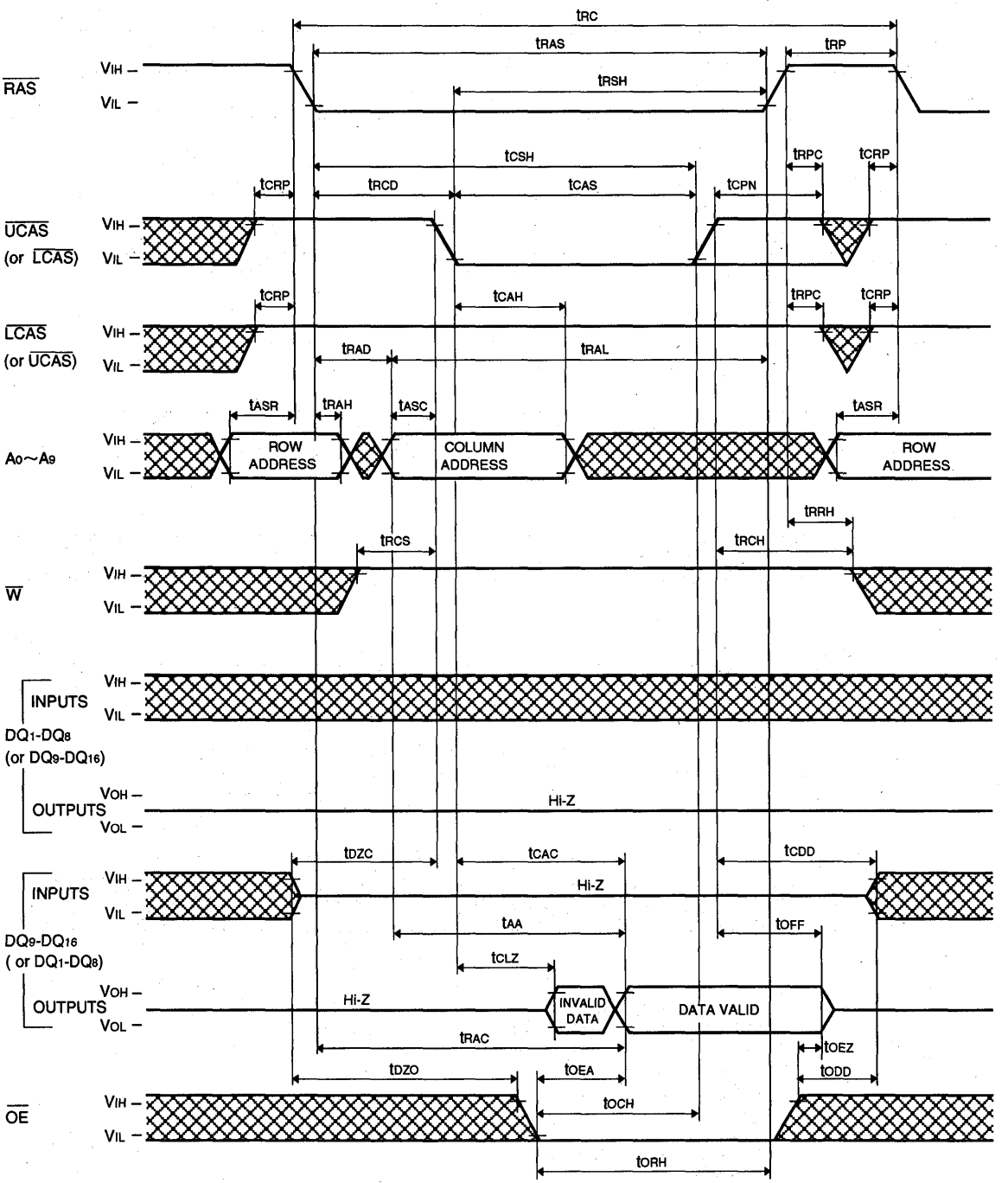
Note 28

Indicates the don't care input.
VIH(min.) ≦ VIN ≦ VIH(max) or VIL(min.) ≦ VIN ≦ VIL(max)

Indicates the invalid output.

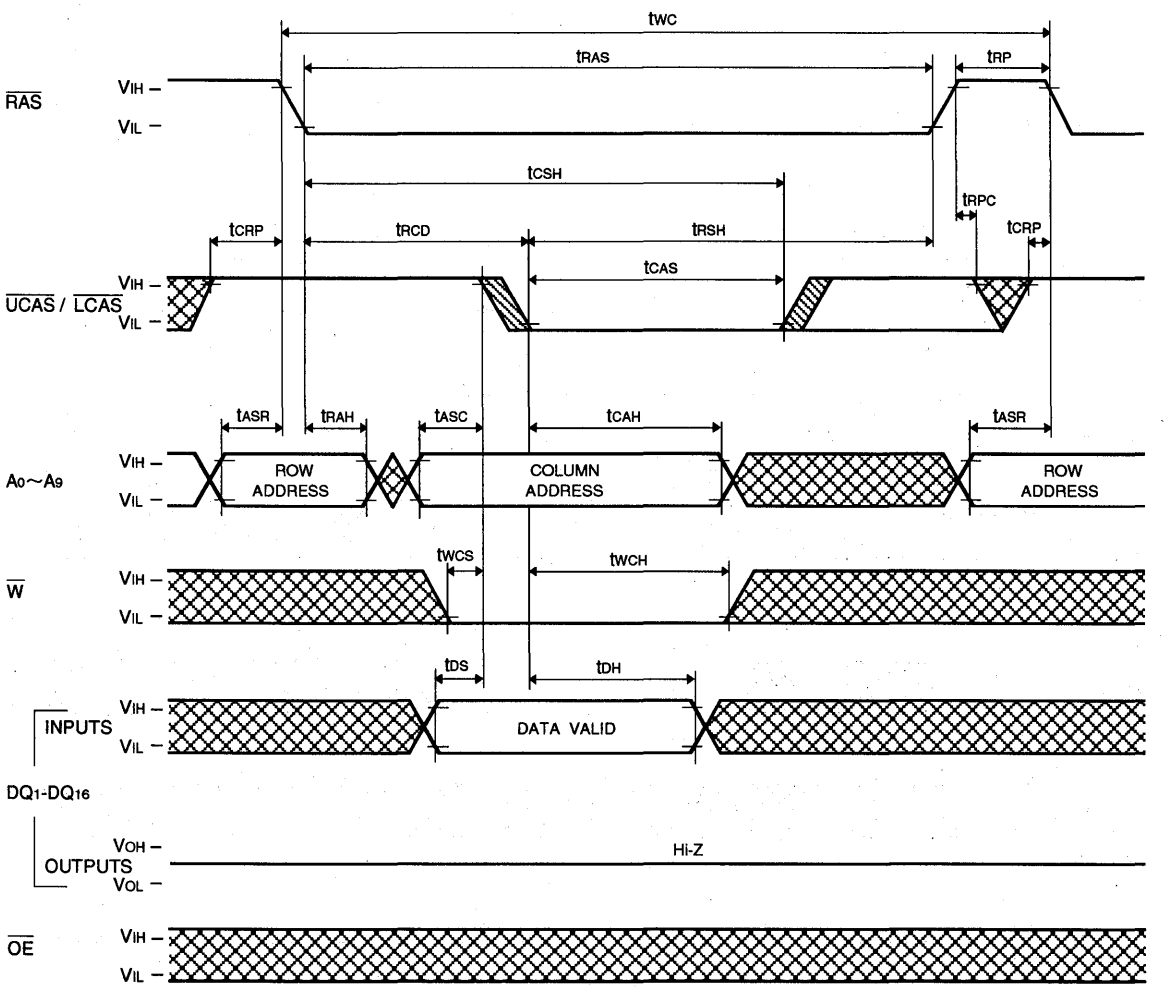
Indicates the skew of the two inputs.

Upper / (Lower) Byte Read Cycle

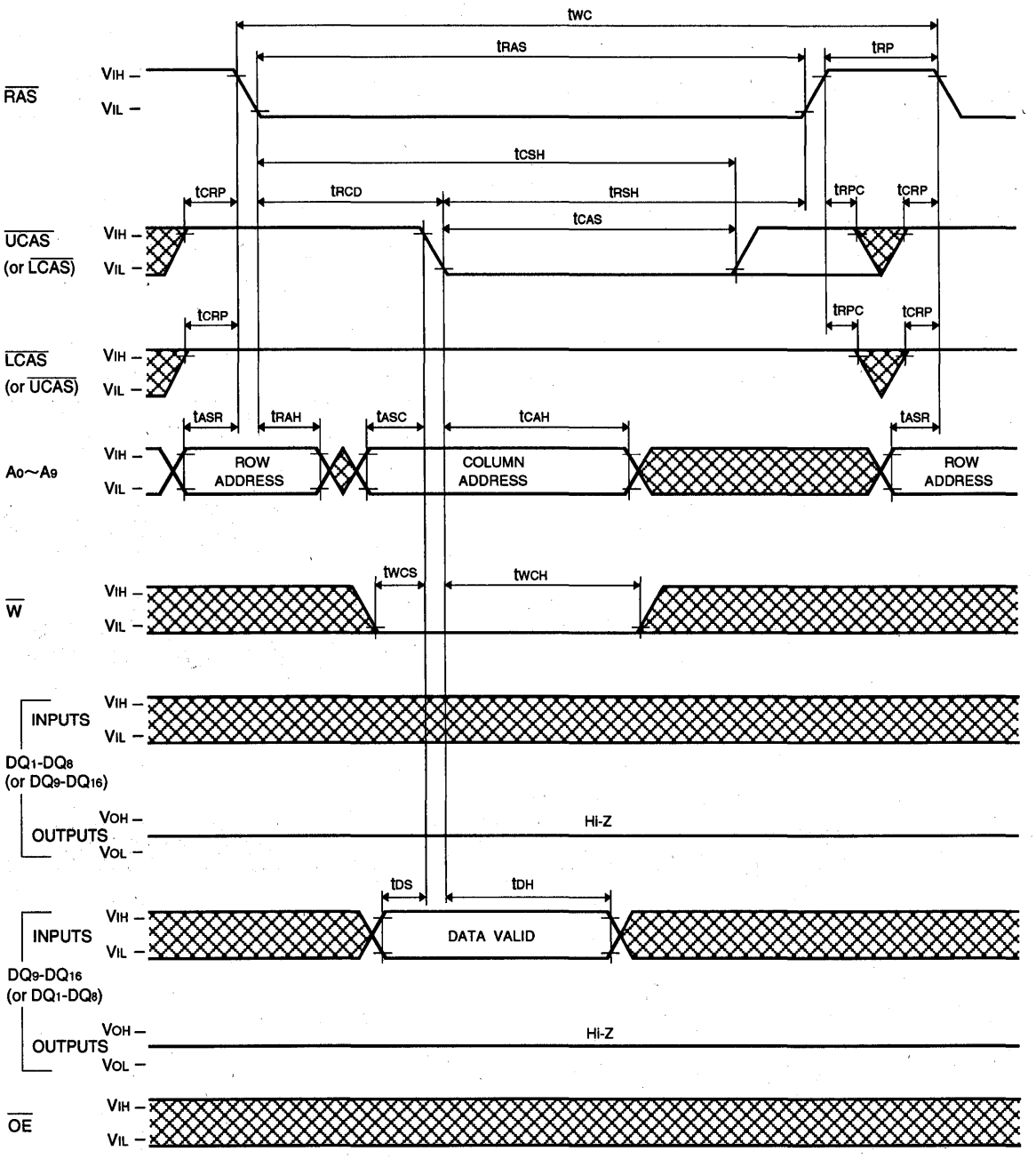


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early write)

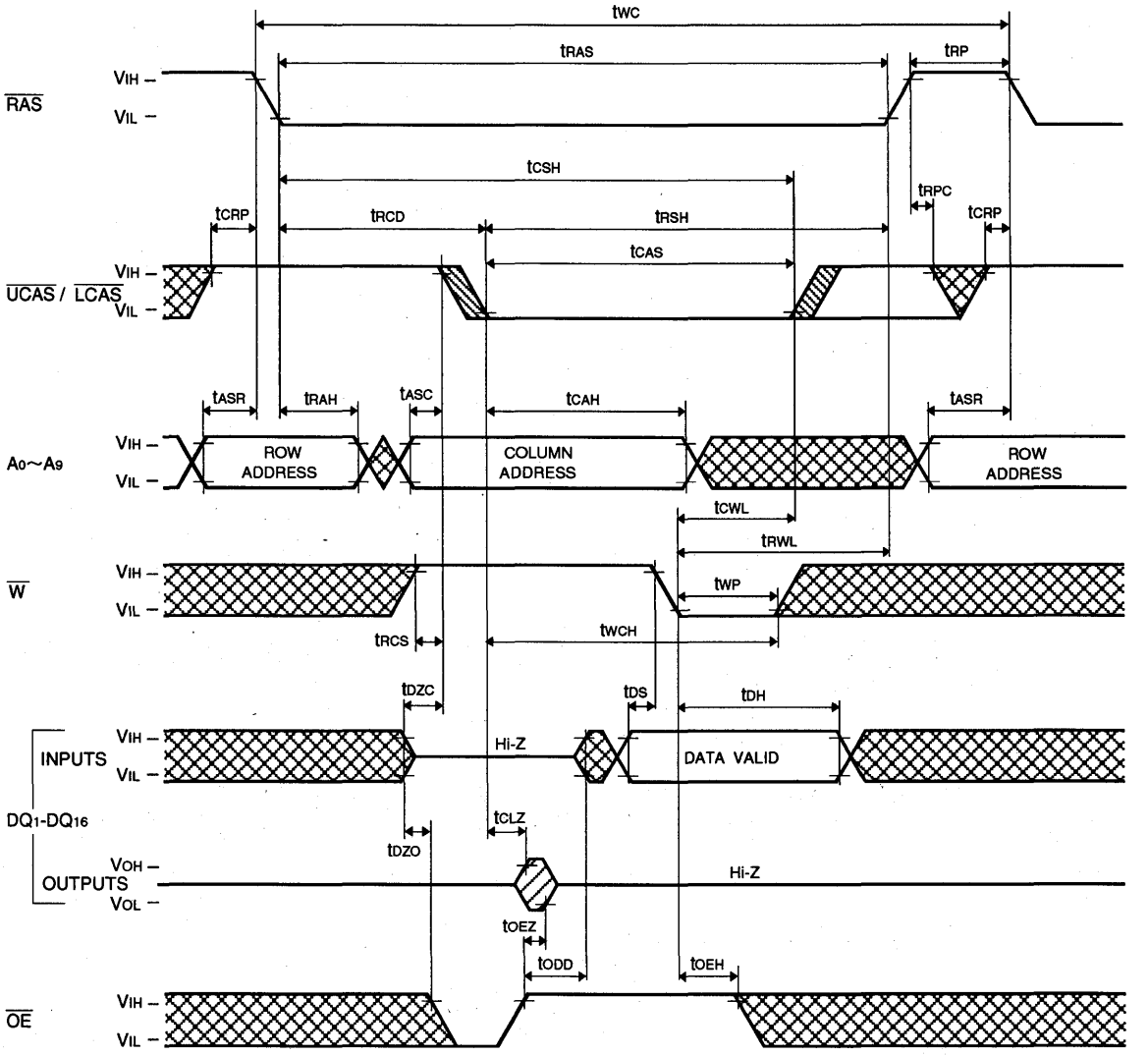


Upper / (Lower) Byte Write Cycle (Early write)

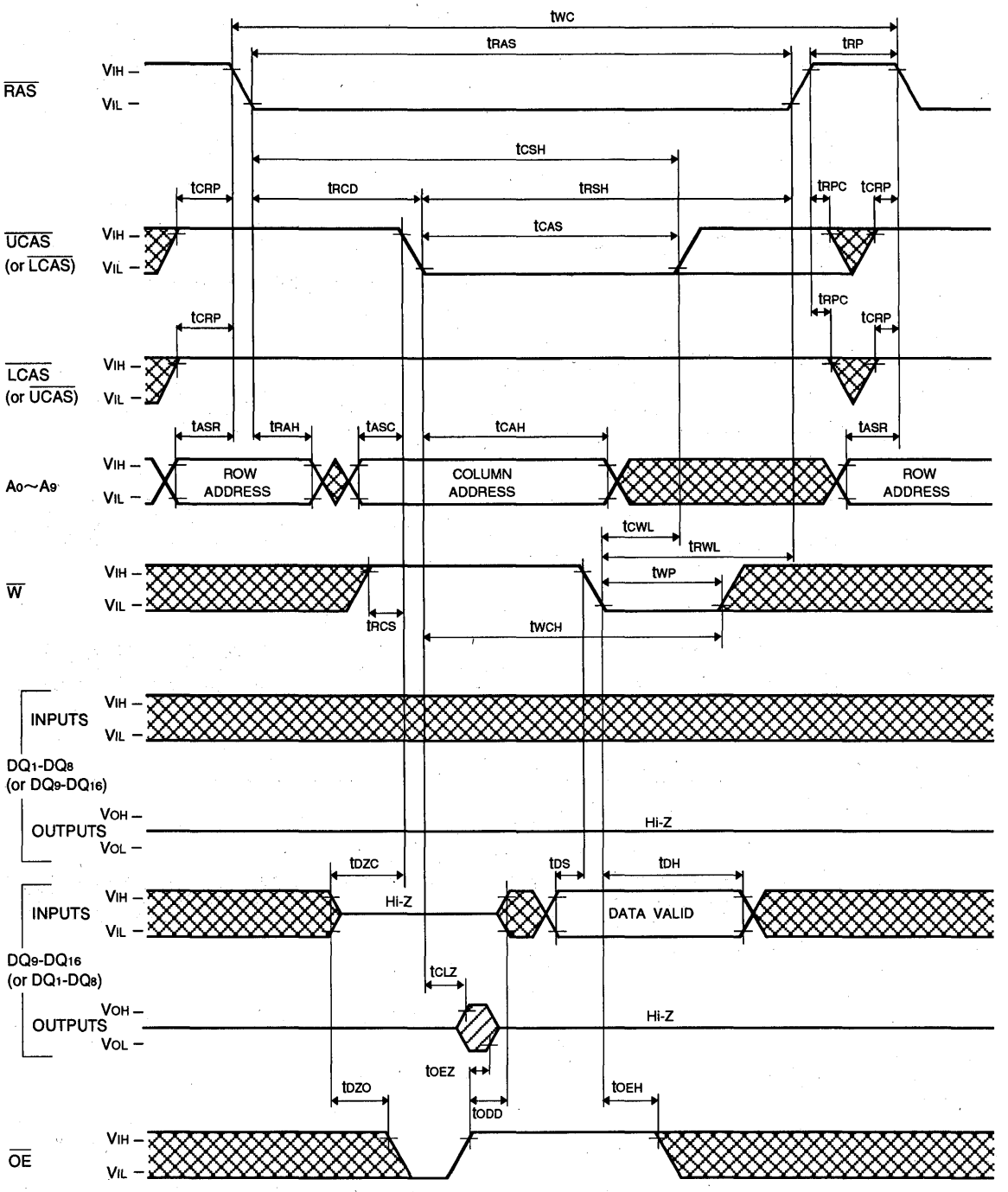


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Delayed write)

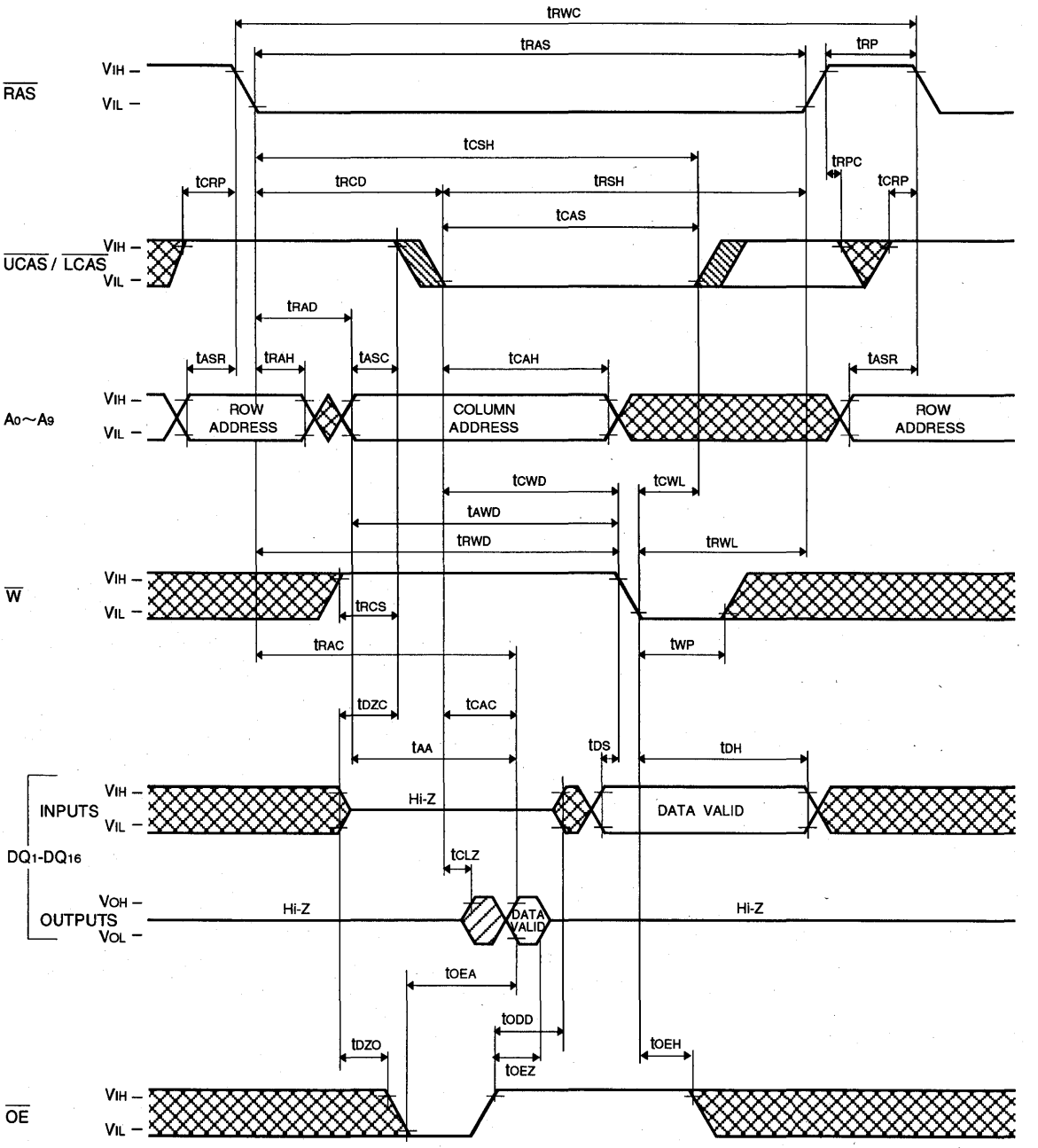


Upper / (Lower) Byte Write Cycle (Delayed write)

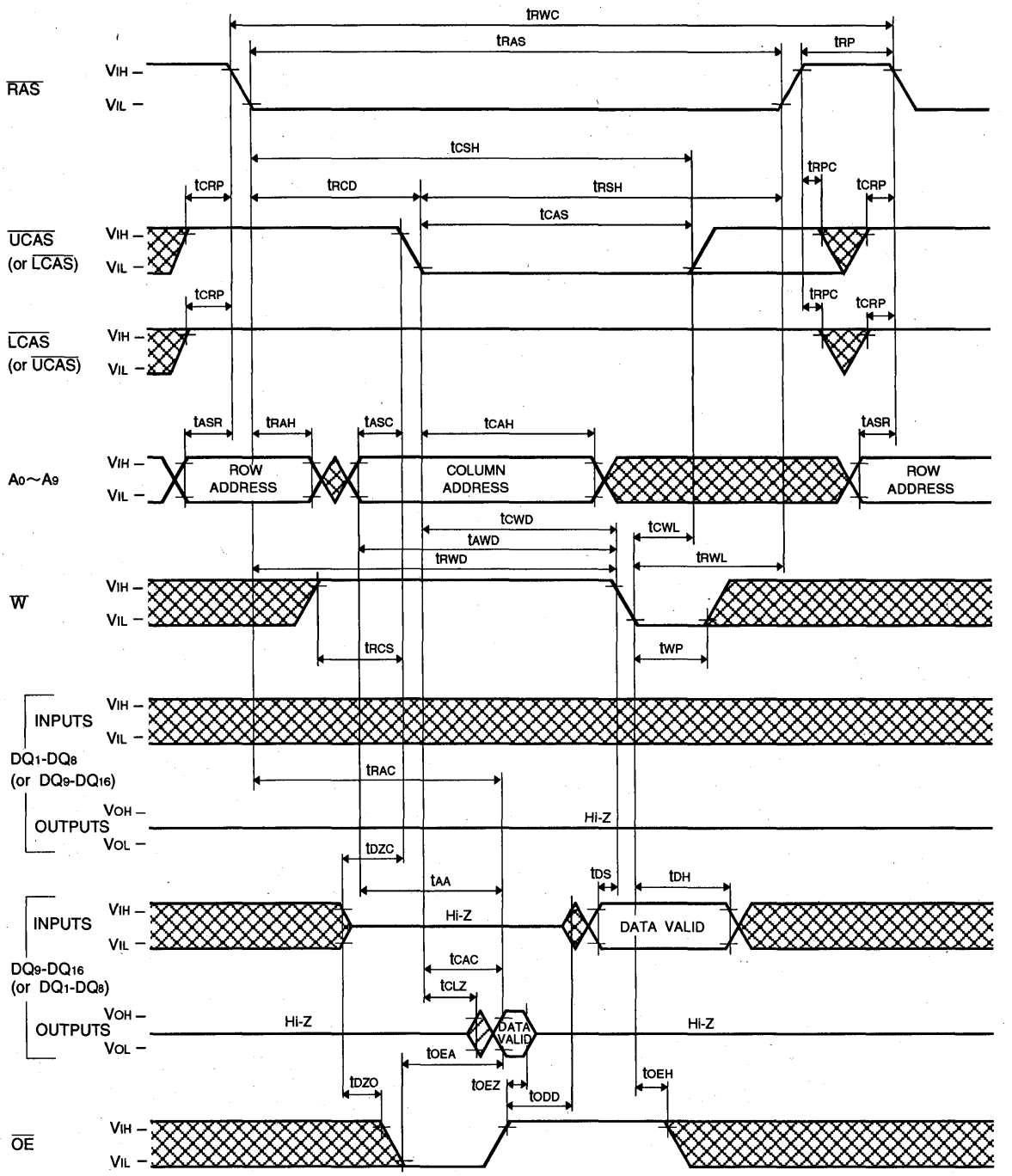


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle

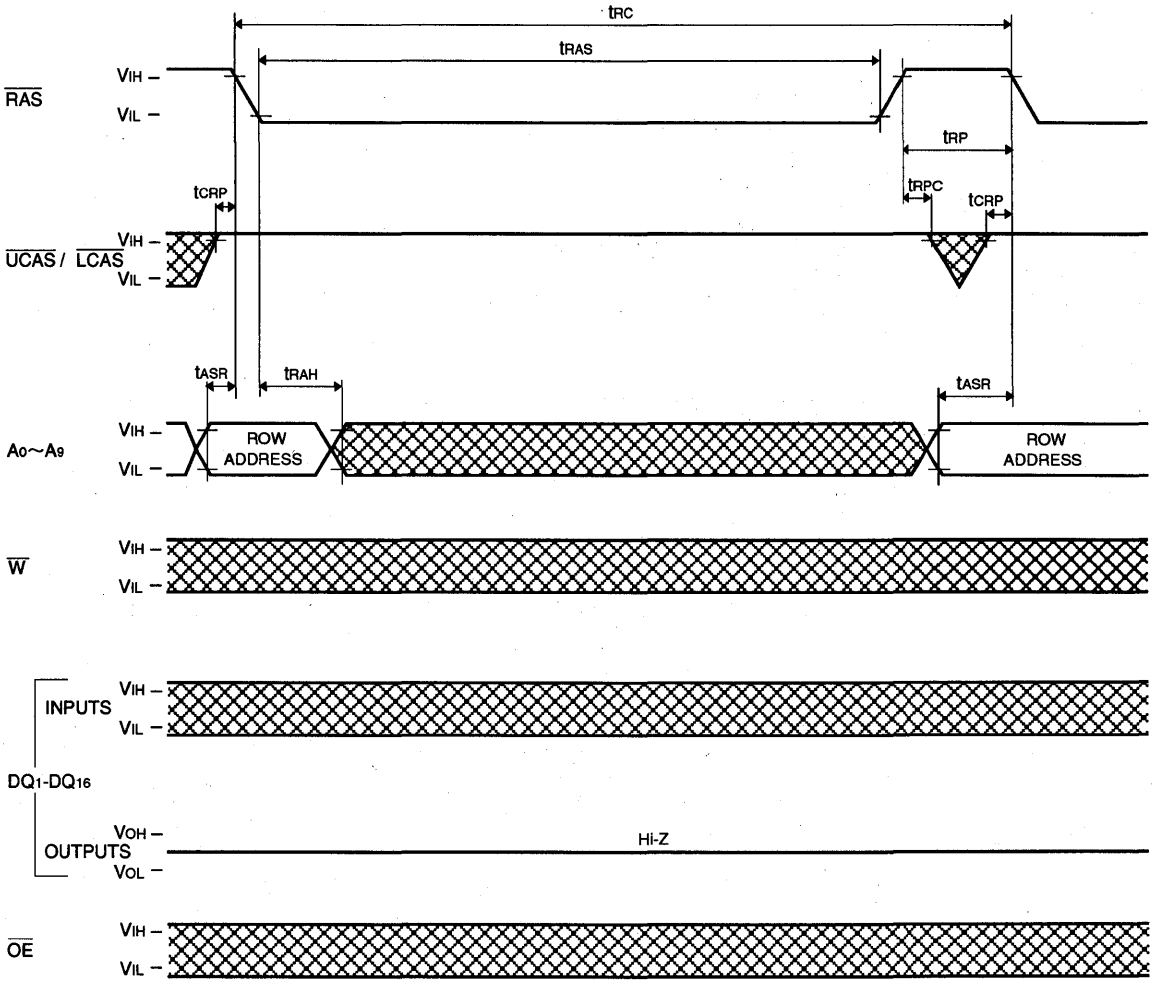


Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



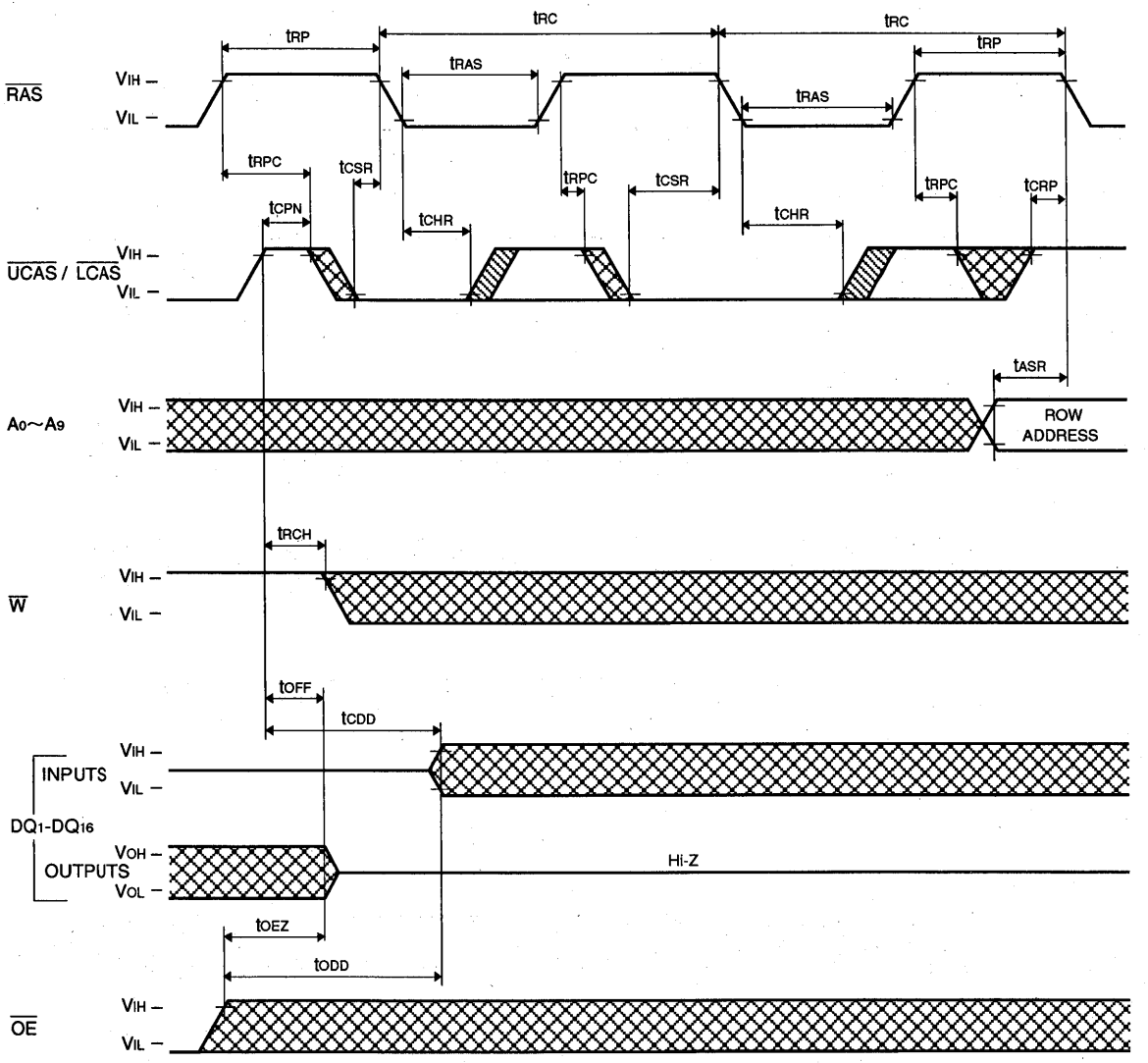
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle



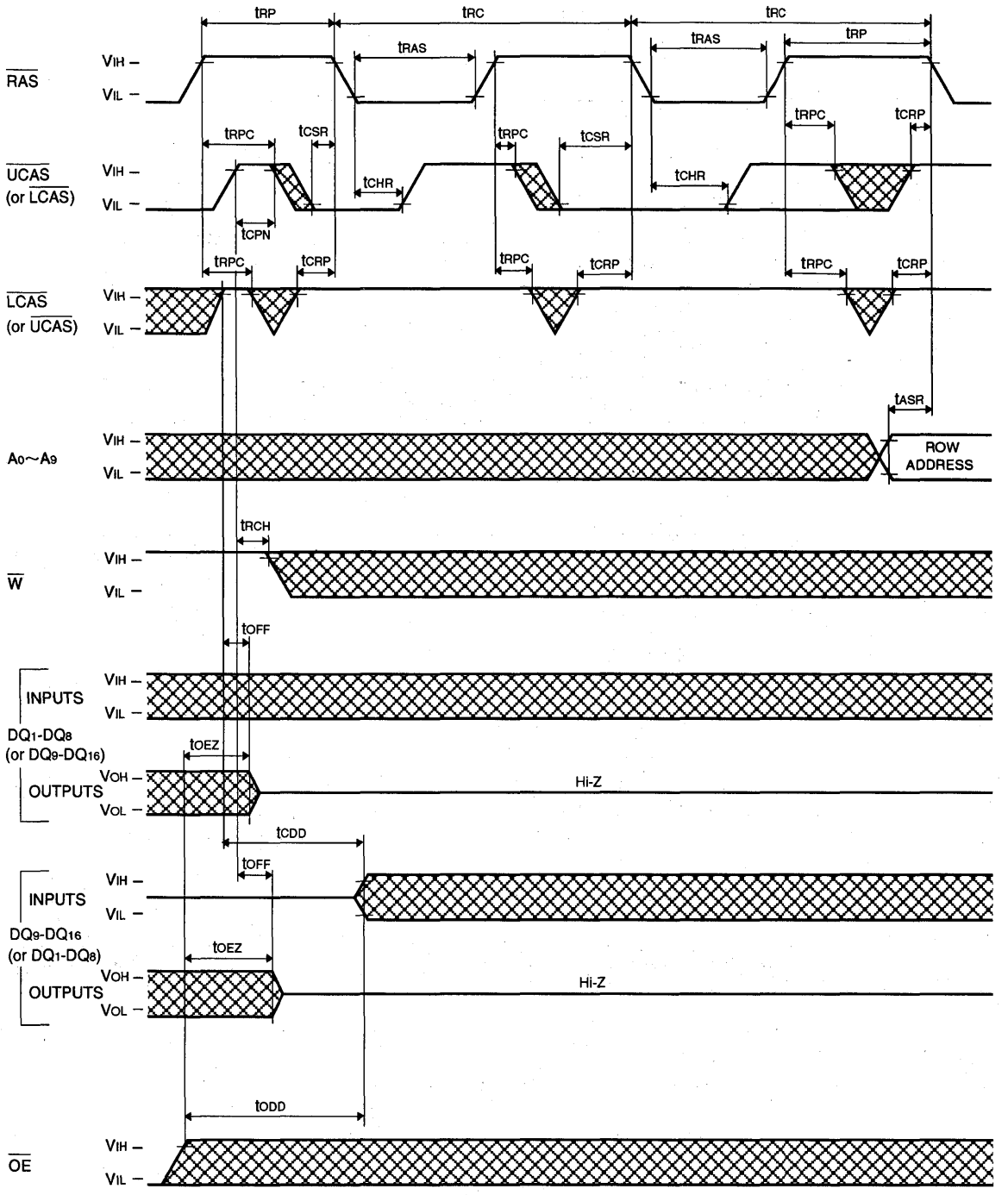
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

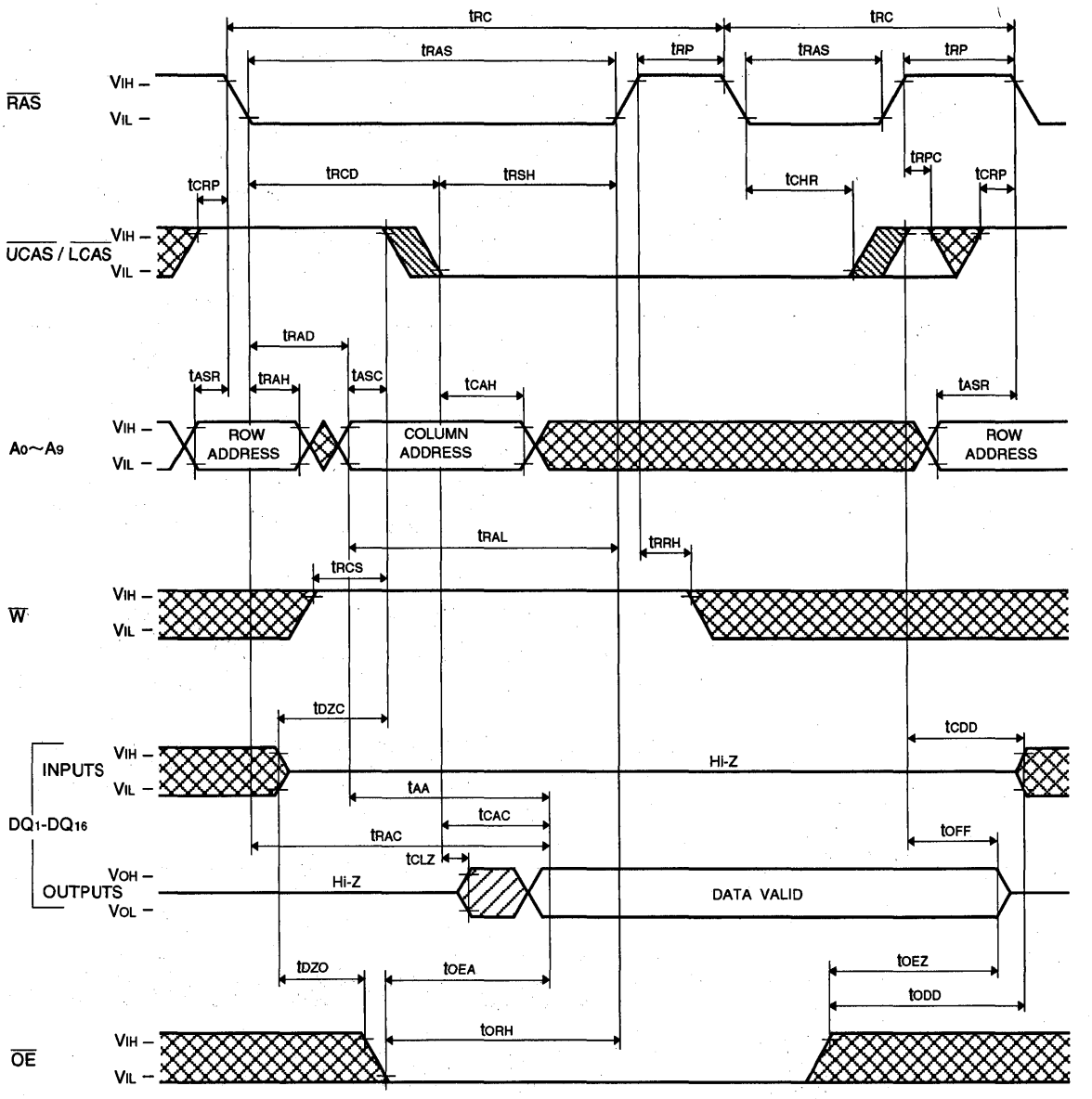


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

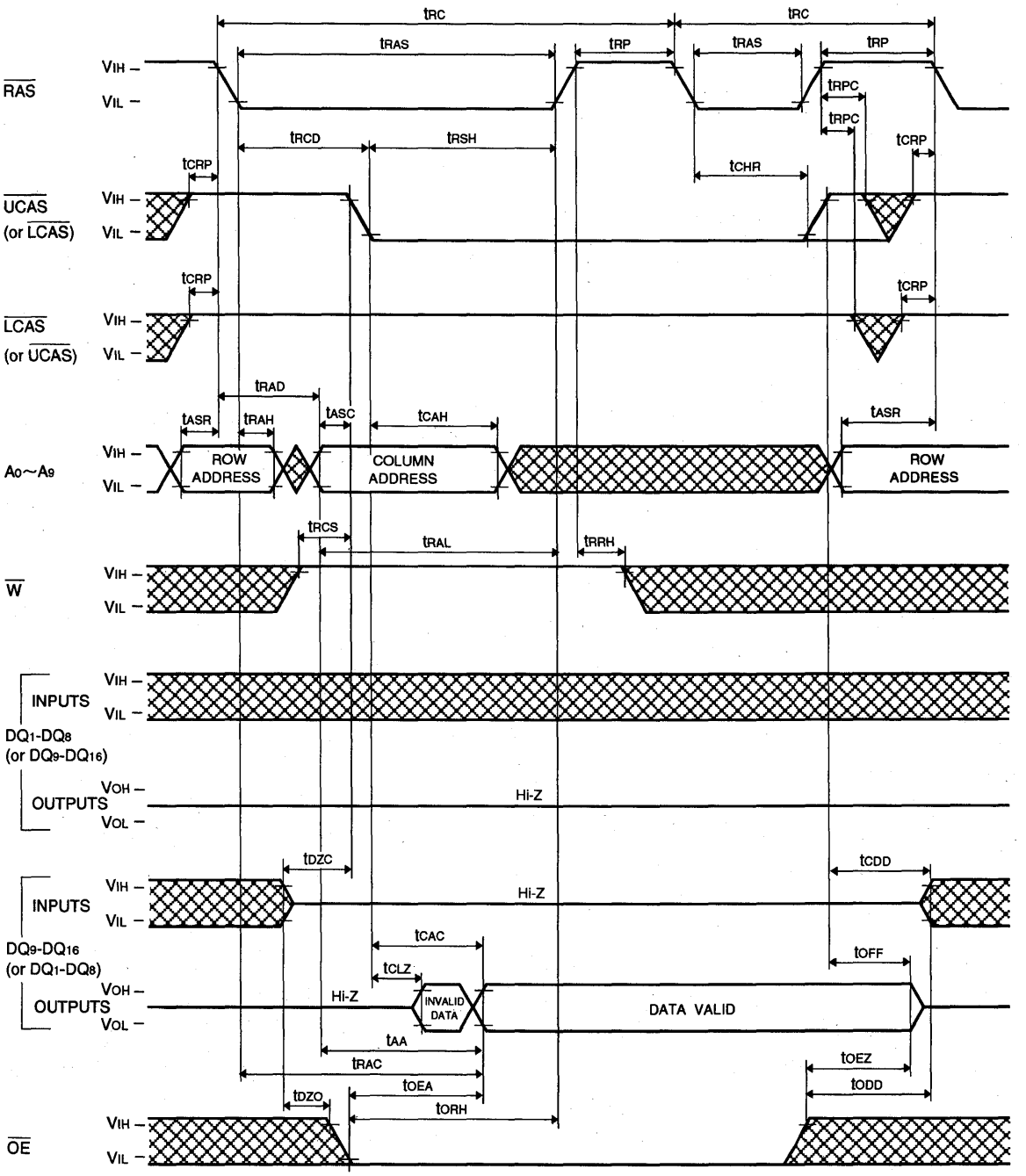


Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

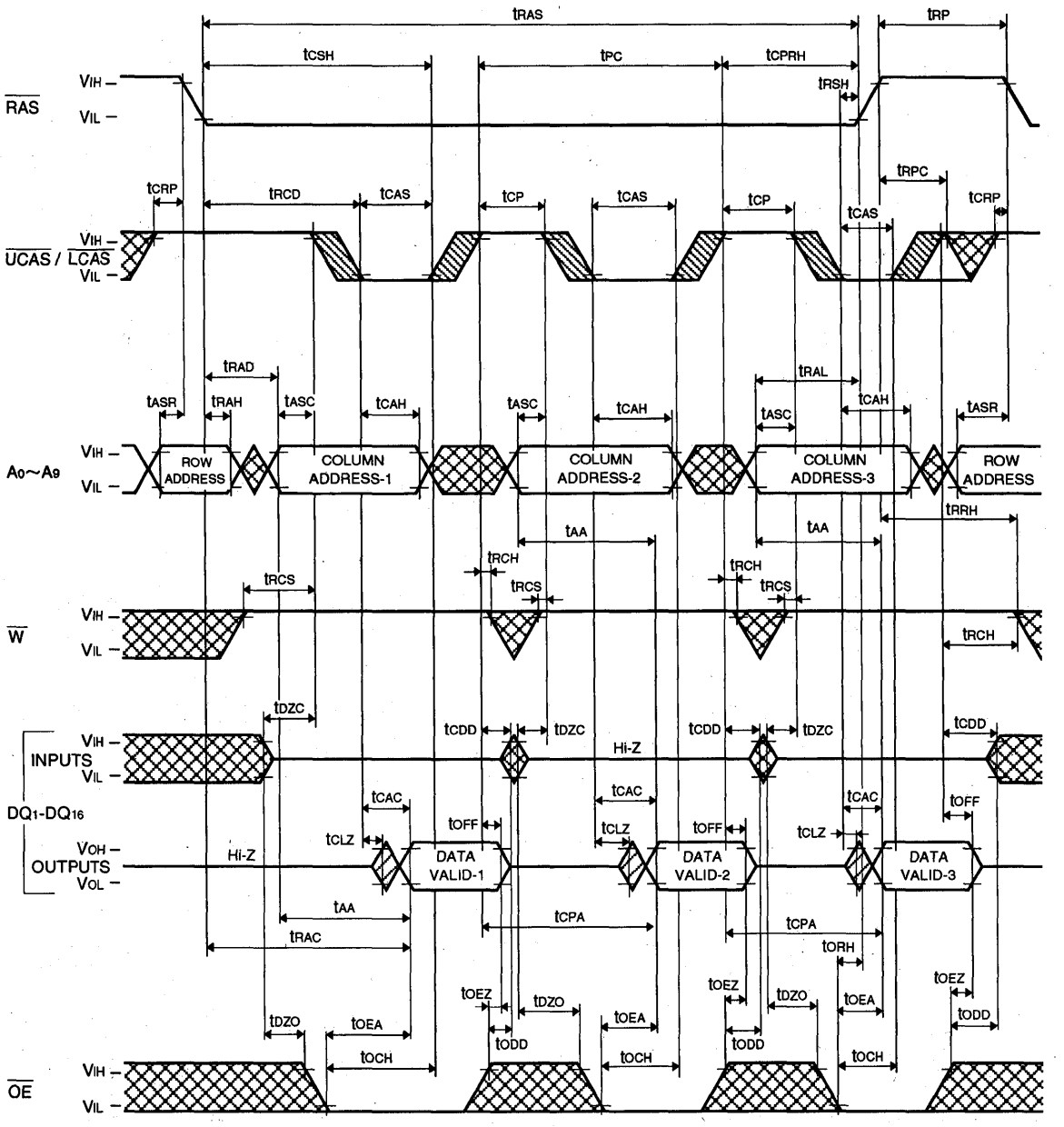
Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



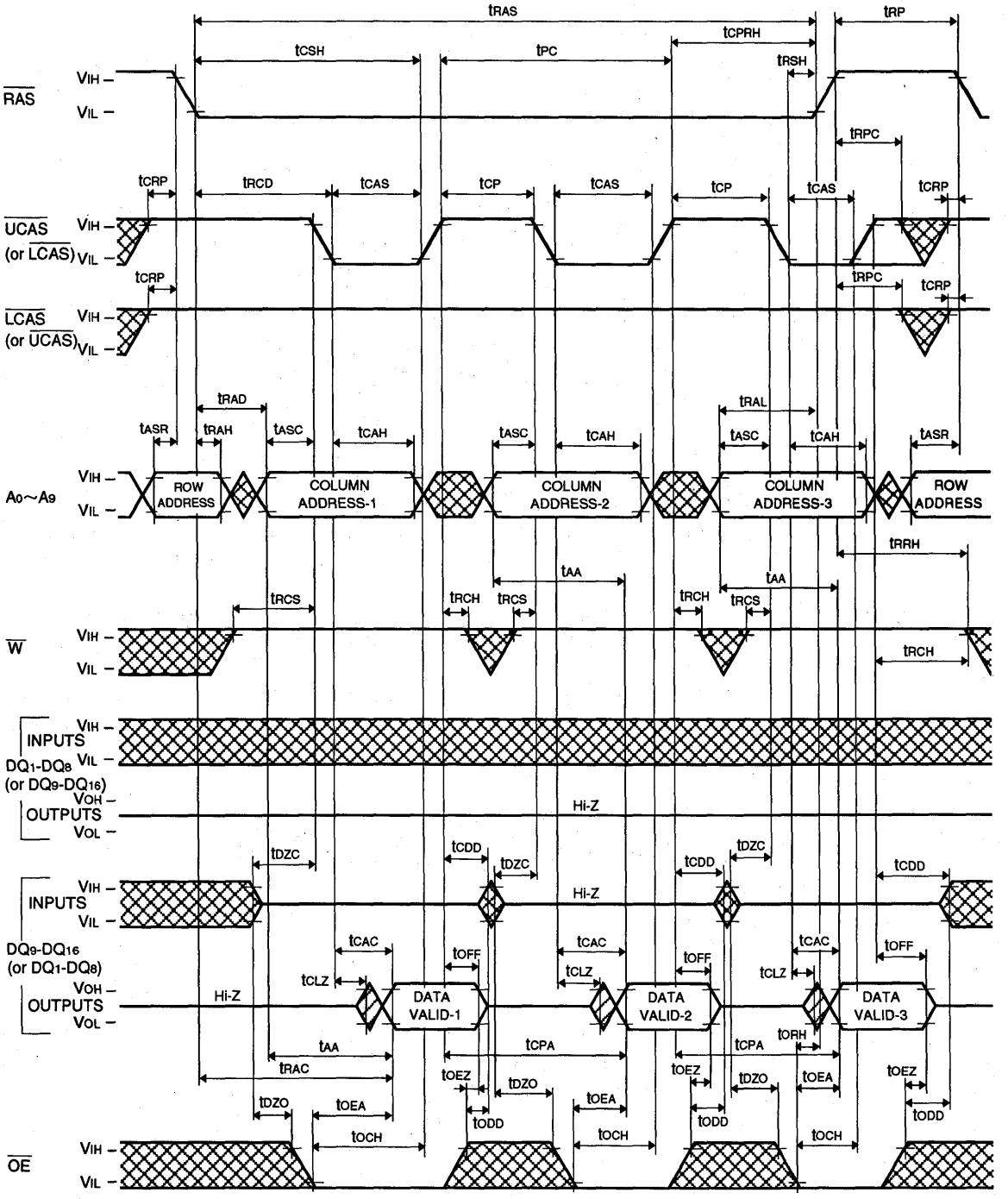
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle

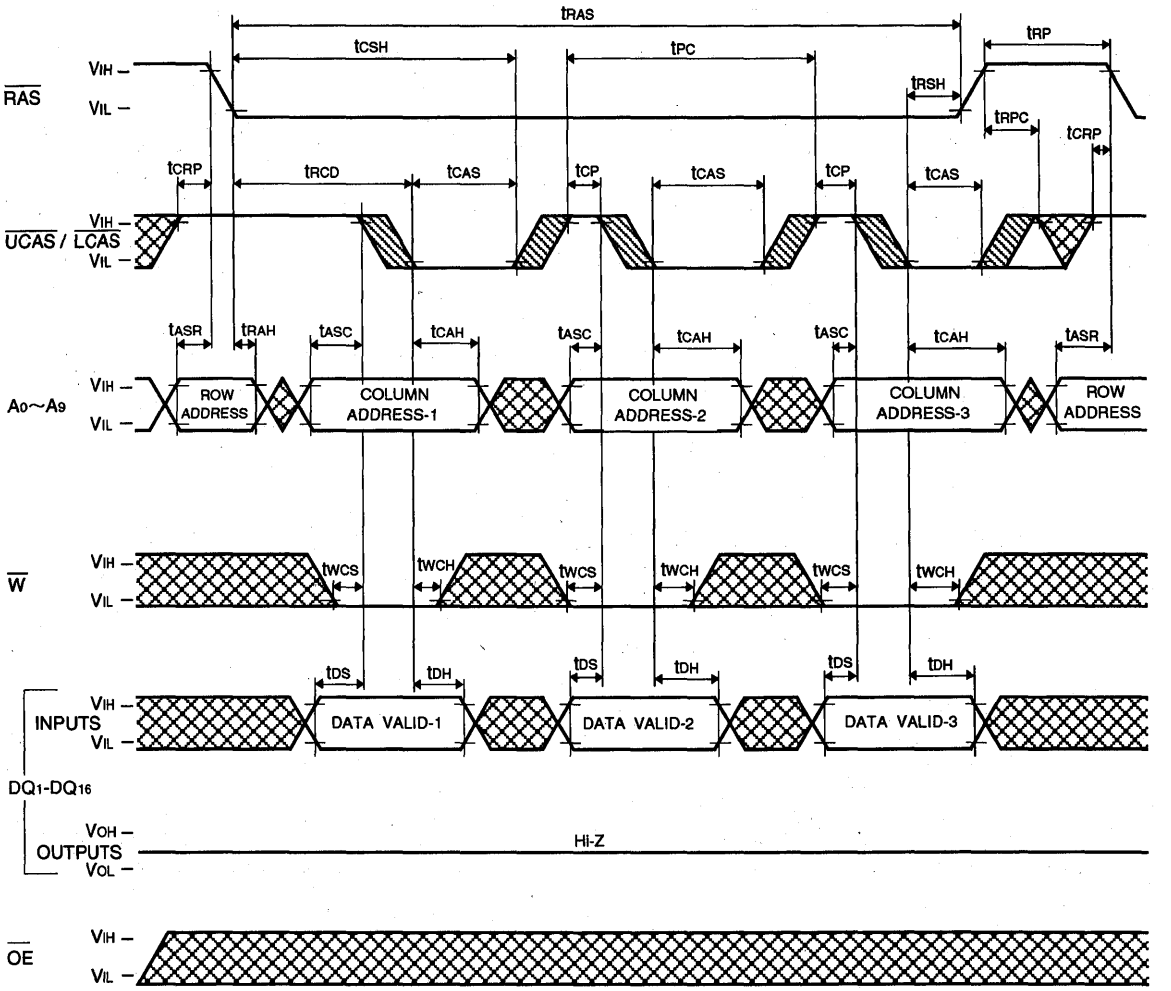


Upper / (Lower) Fast Page Mode Read Cycle

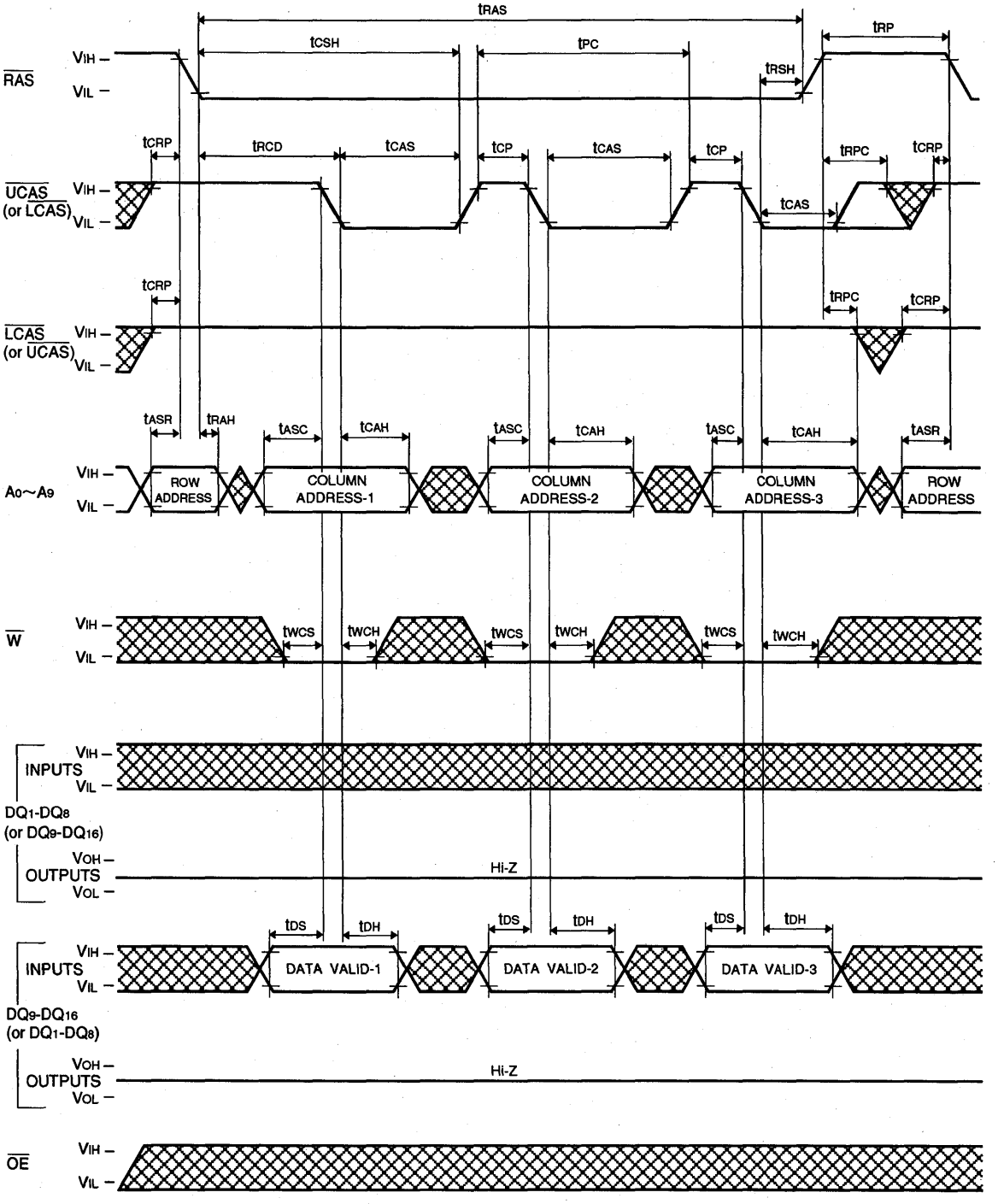


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)

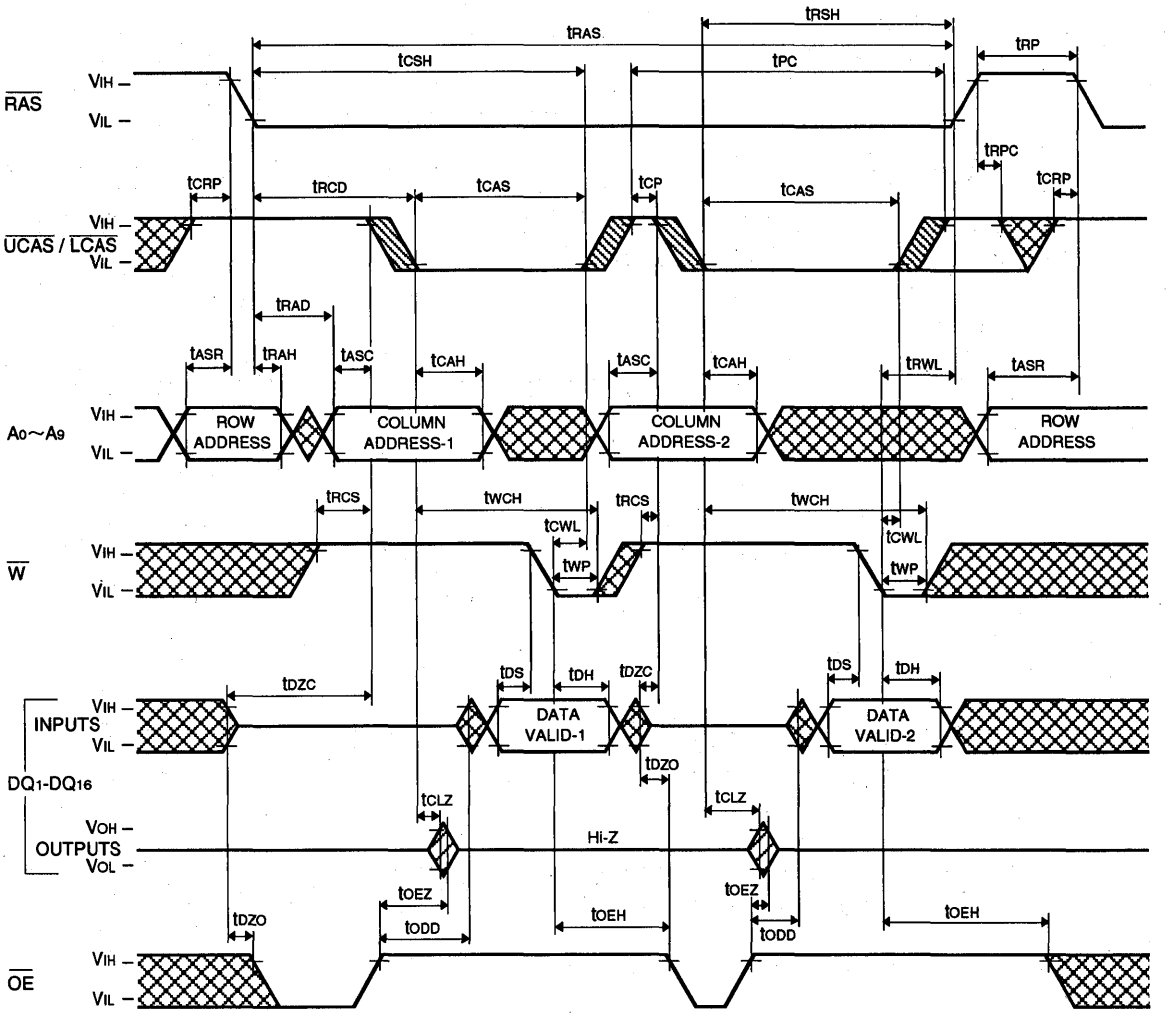


Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)



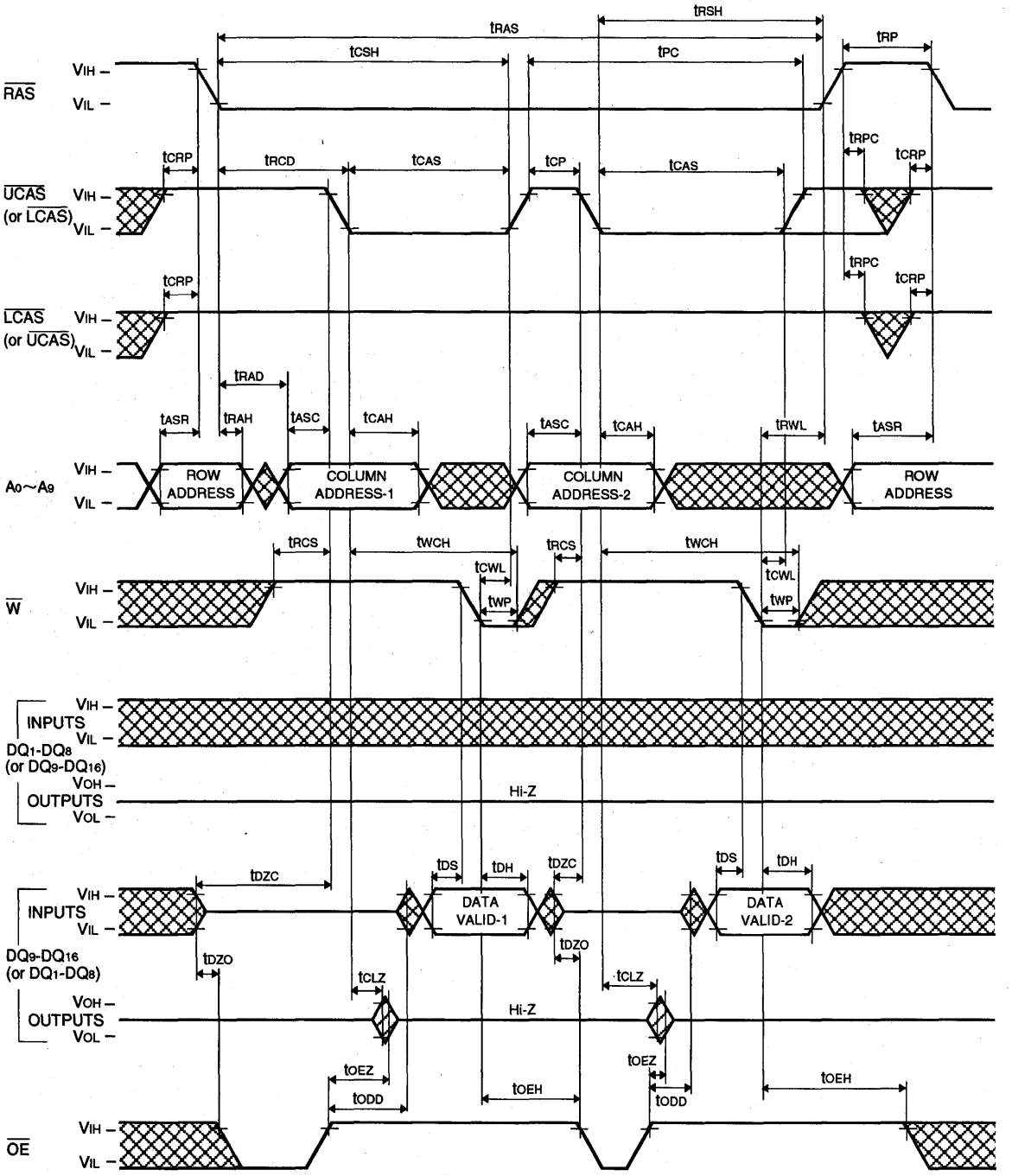
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Delayed Write)

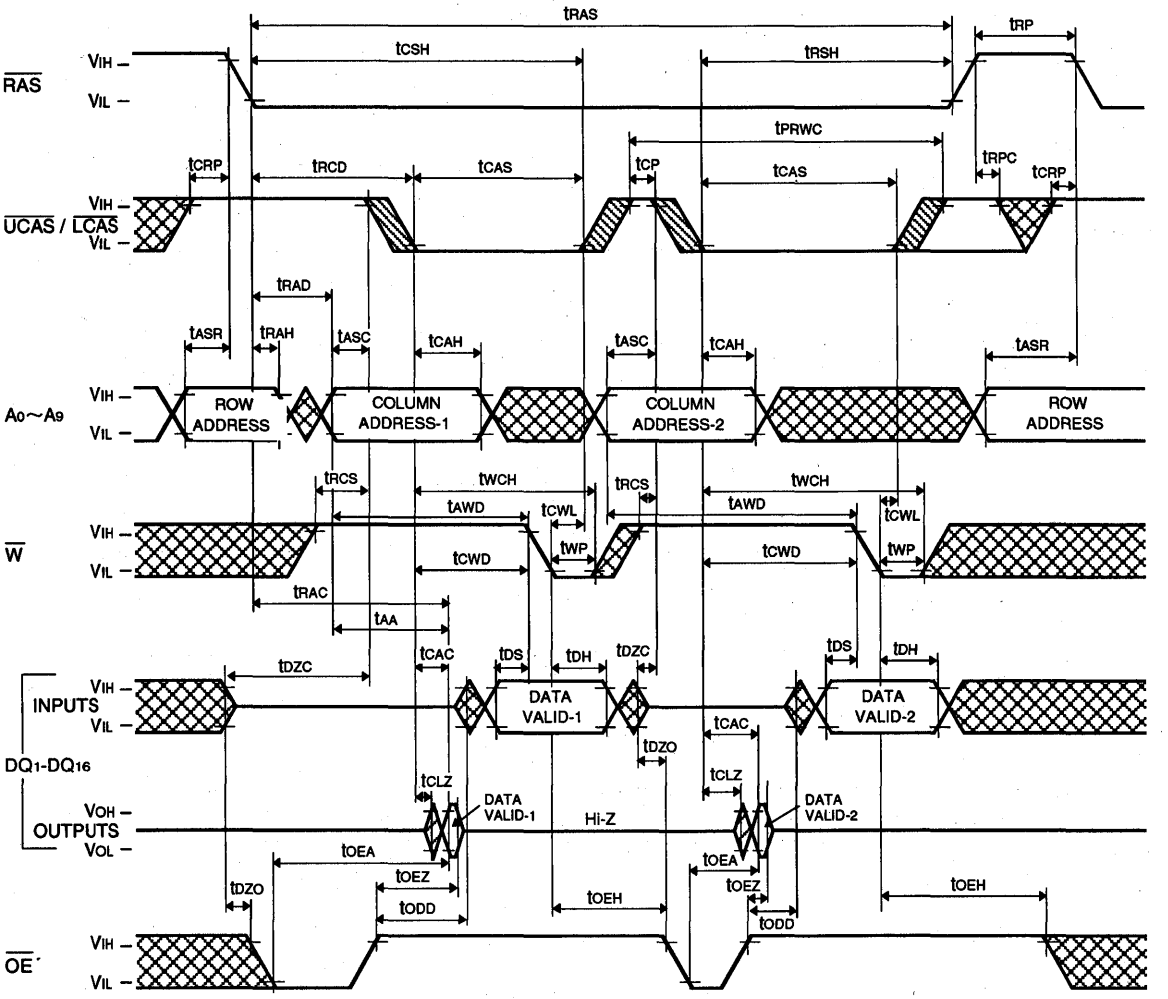


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)

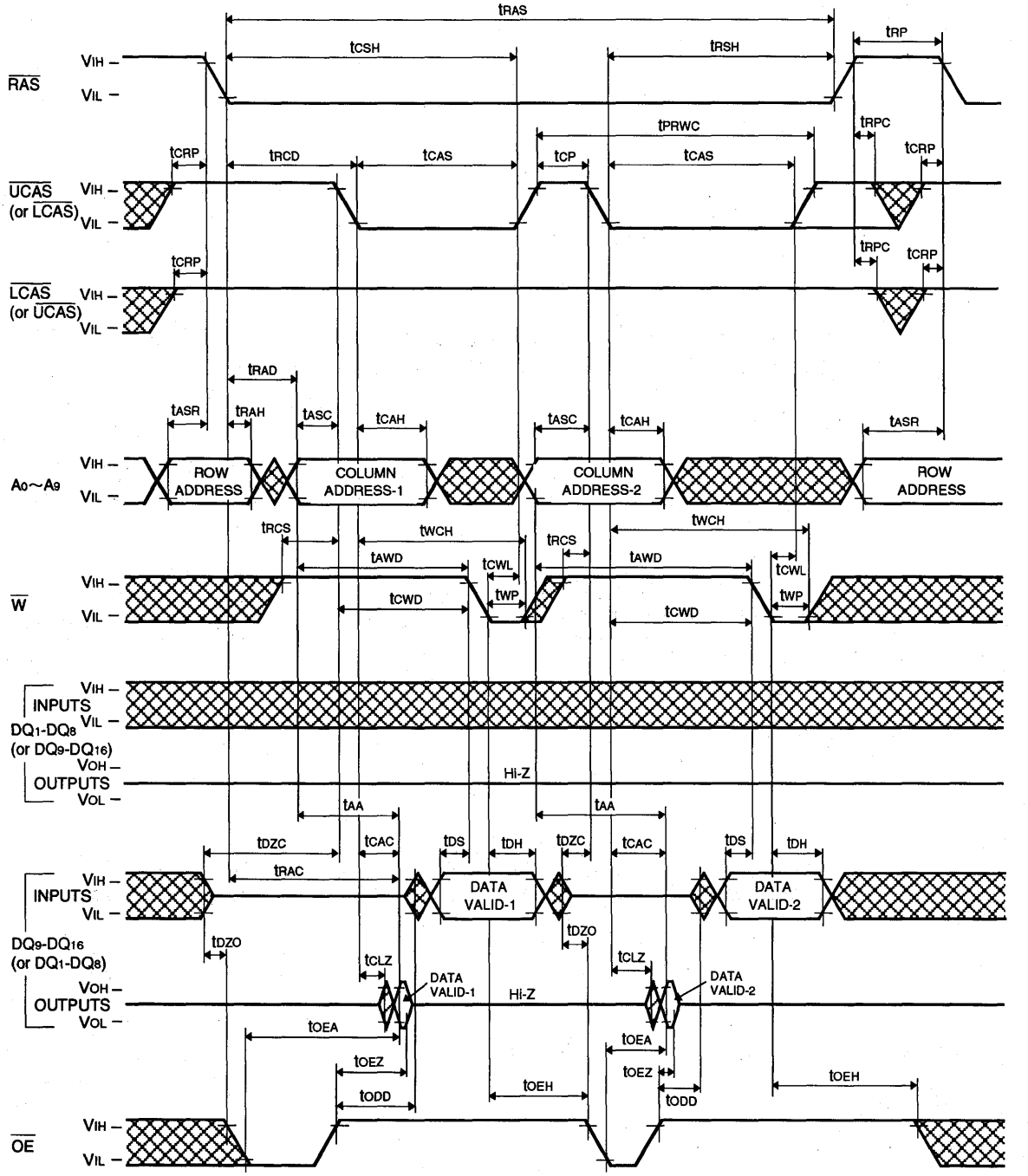


Fast Page Mode Read-Write, Read-Modify-Write Cycle

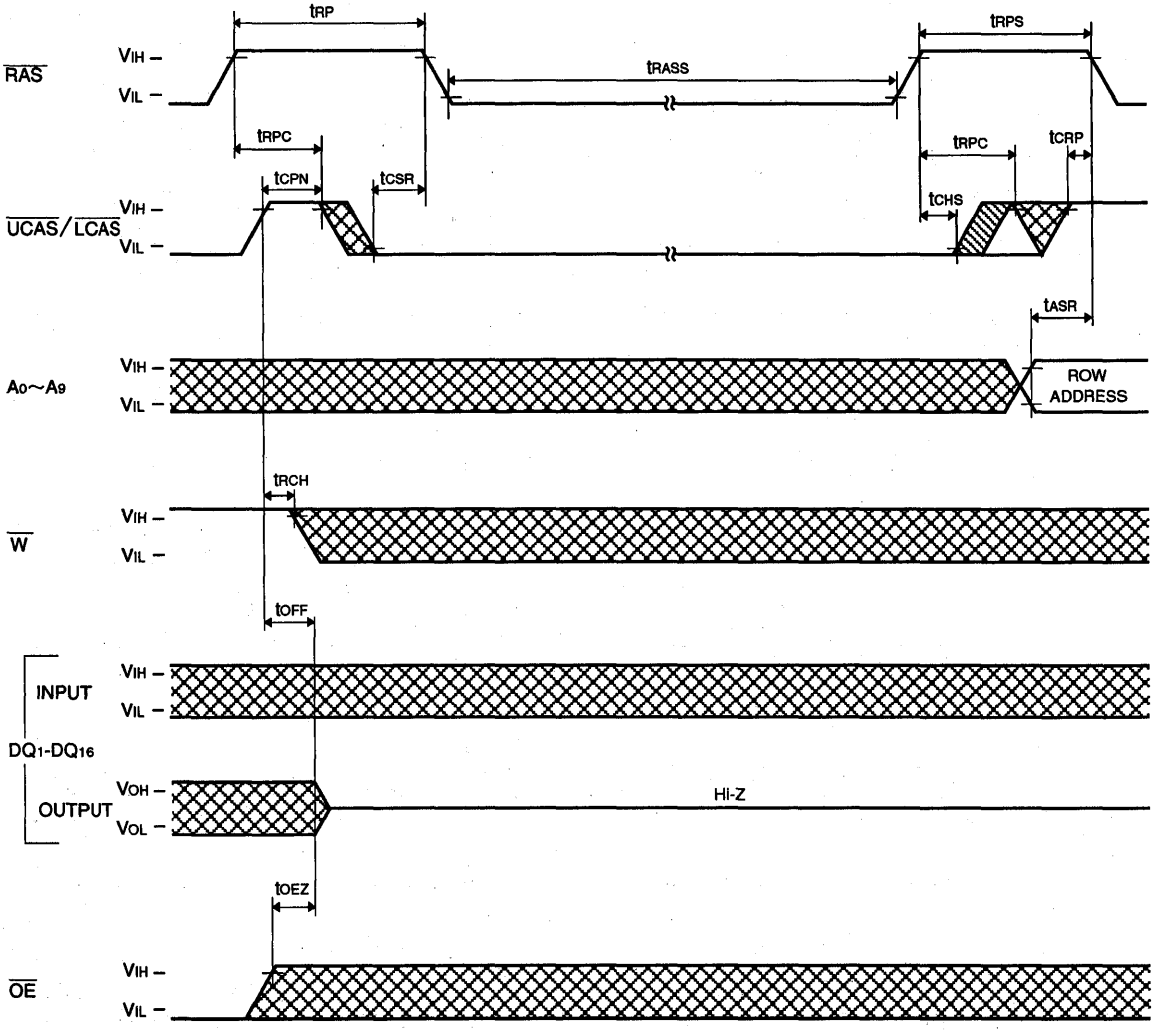


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

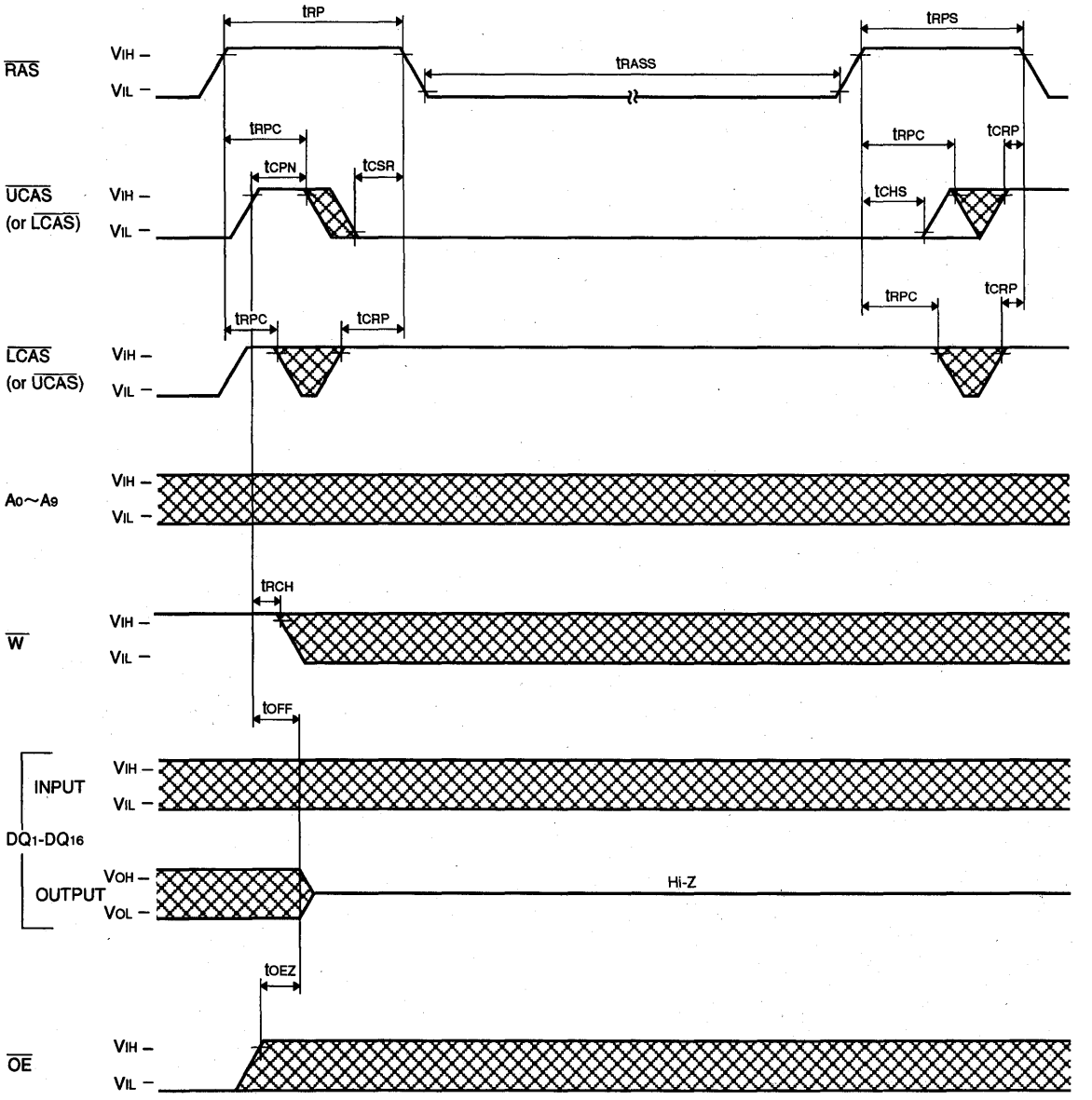
Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



Self Refresh Cycle∗



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416165CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416165CXX-5,-5S	50	13	25	13	90	540
M5M416165CXX-6,-6S	60	15	30	15	110	430
M5M416165CXX-7,-7S	70	20	35	20	130	385

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS input level
- Low operating power dissipation
  M5M416165Cxx-5,-5S ---------- 660.0mW (Max)
  M5M416165Cxx-6,-6S ---------- 525.0mW (Max)
  M5M416165Cxx-7,-7S ---------- 470.0mW (Max)
- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0~A_{11})
  * : Applicable to self refresh version (M5M416165CJ,TP-5S,-6S, -7S : option) only

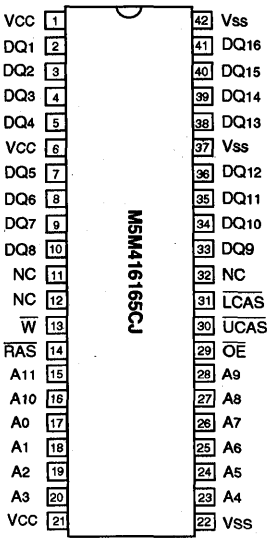
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

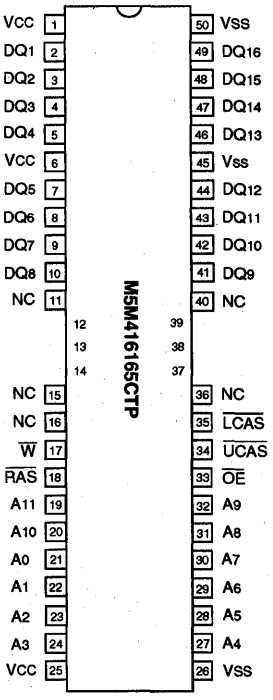
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

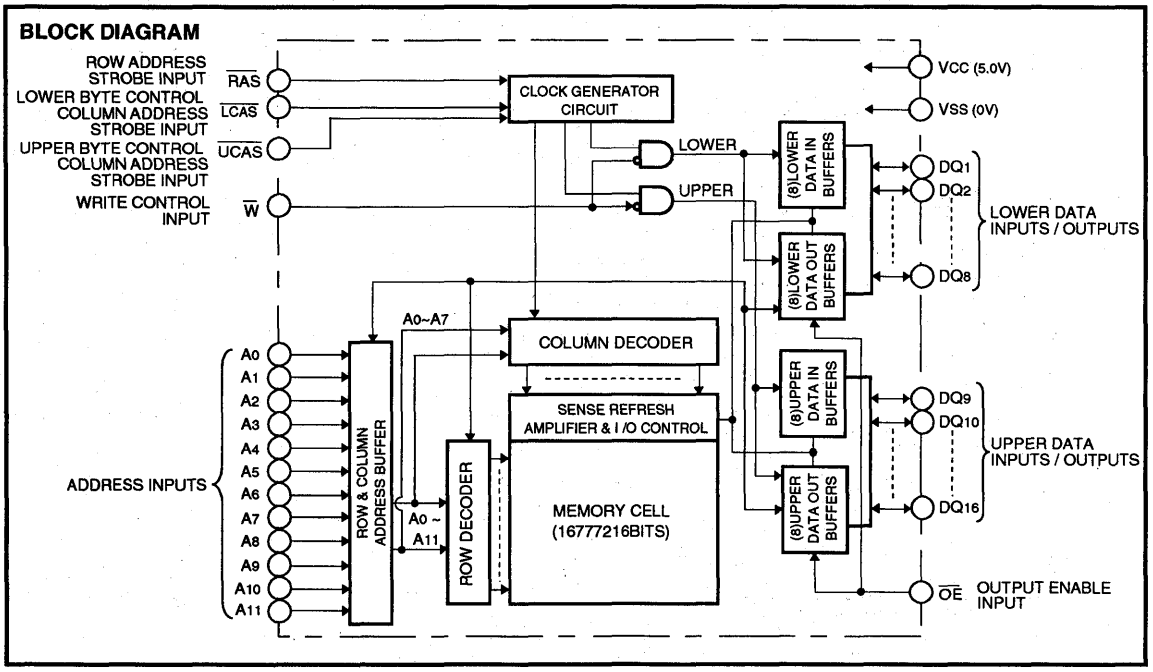
The M5M416165CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1~7	V
V_I	Input voltage		-1~7	V
V_O	Output voltage		-1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to VSS.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M416165C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M416165C-6,-6S				95	
		M5M416165C-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc-0.2V output open			1	
						0.3*	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M416165C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			120	mA
		M5M416165C-6,-6S				95	
		M5M416165C-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M416165C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			165	mA
		M5M416165C-6,-6S				130	
		M5M416165C-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416165C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M416165C-6,-6S				95	
		M5M416165C-7,-7S				85	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M416165C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V; $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling; $\overline{W}$≦0.2V or ≧Vcc-0.2V; $\overline{OE}$≦0.2V or ≧Vcc-0.2V; A_0~A_{11}≦0.2V or ≧Vcc-0.2V; DQ=open, t_{RC}=125μs, t_{RAS}=t_{RAS}min~1μs			600	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M416165C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 12)	0	13	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\,\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0～70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧ tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	20		25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time	57		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 27)	8	13	10	16	10	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	45		52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read	52		62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	62		72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M416165C-5,-5S		M5M416165C-6,-6S		M5M416165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

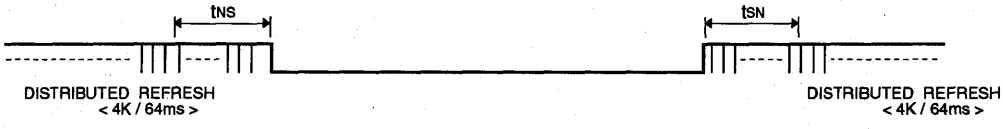
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M416165C-5S		M5M416165C-6S		M5M416165C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

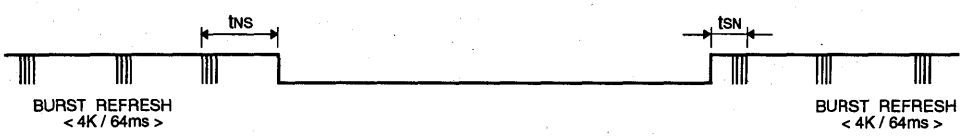
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64ms$ and $t_{SN} \leqq 64ms$.



(2) In case of burst refresh

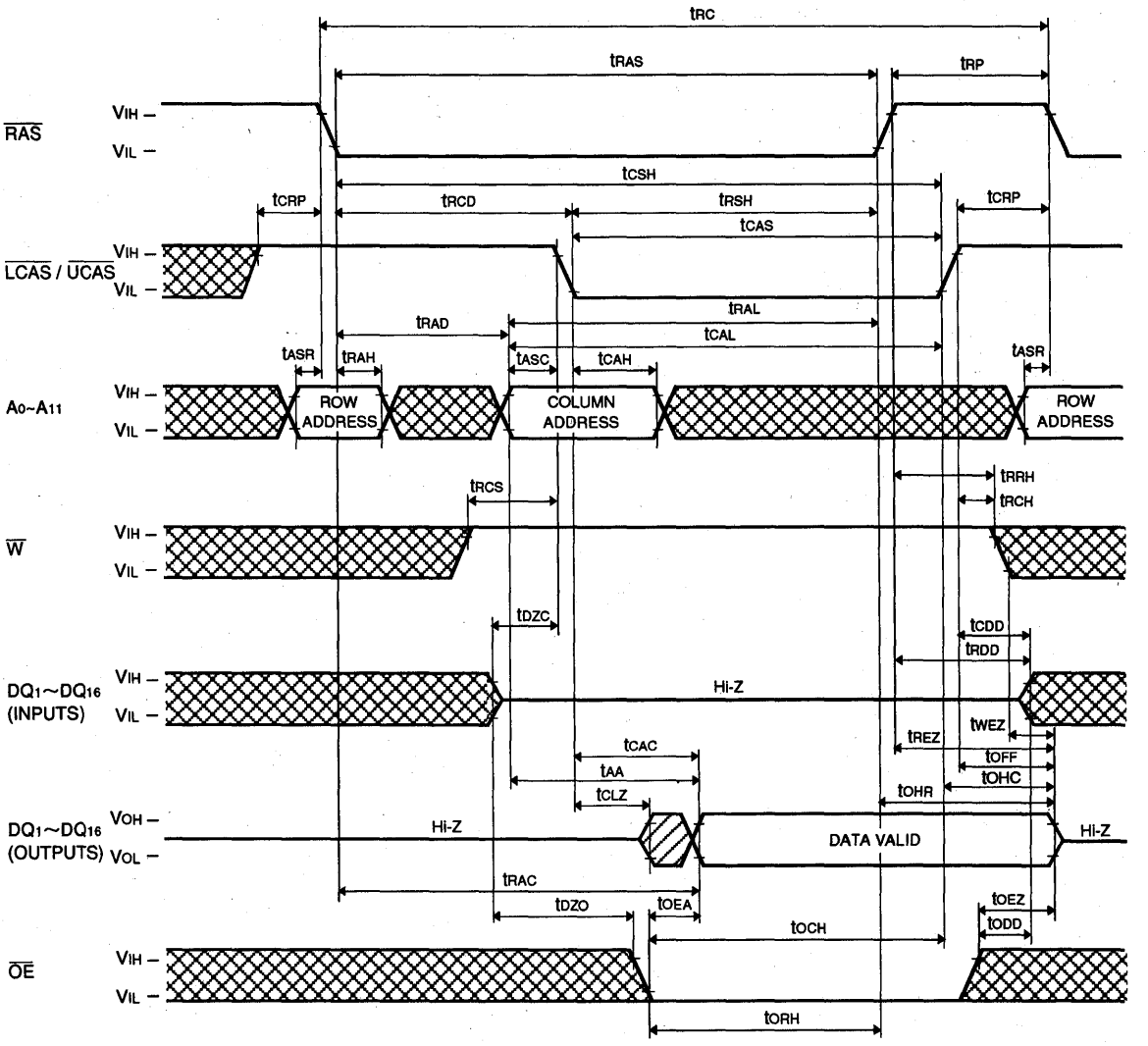
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 64ms$.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 29)

Read Cycle

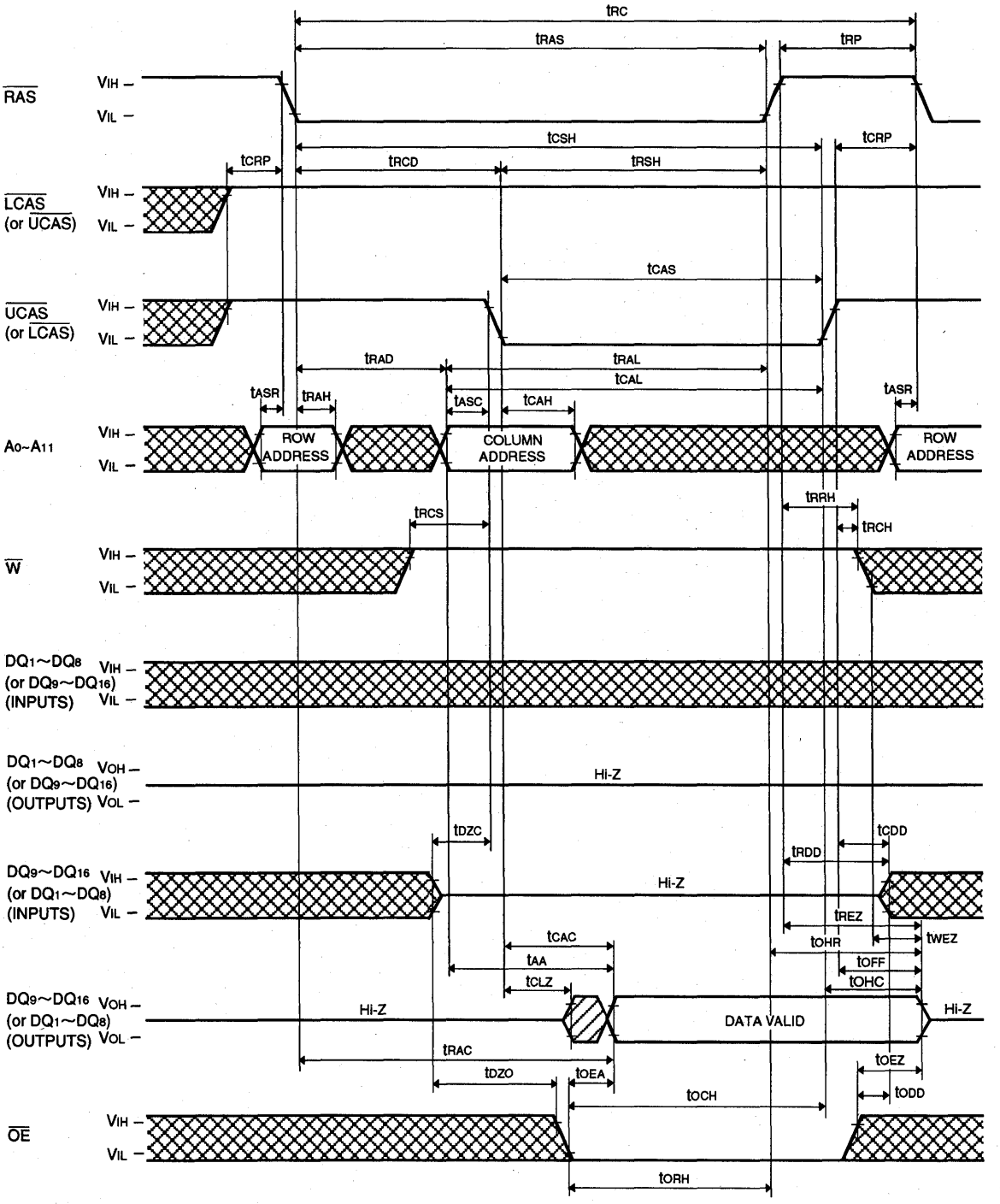


Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

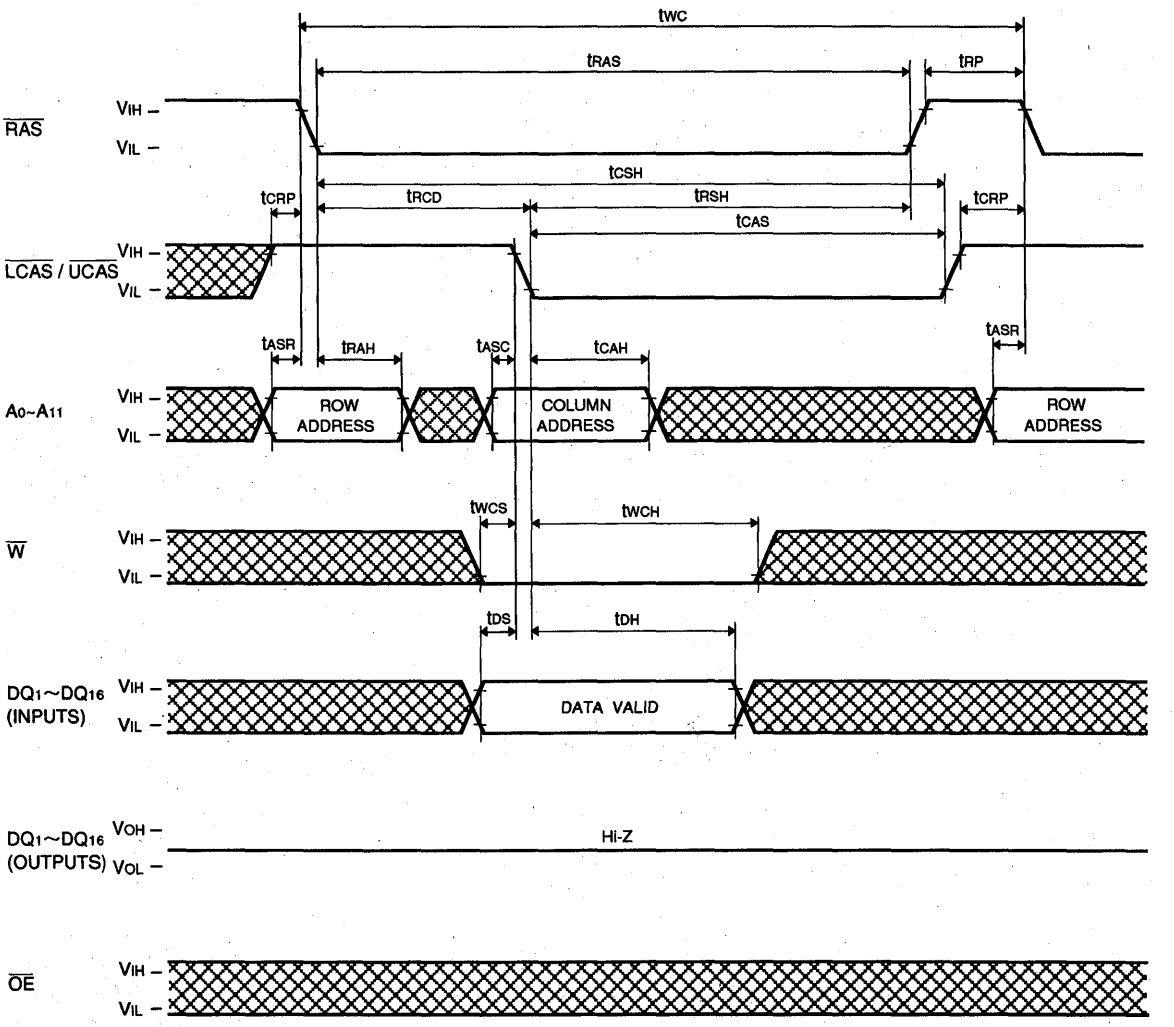
Indicates the invalid output.

Byte Read Cycle



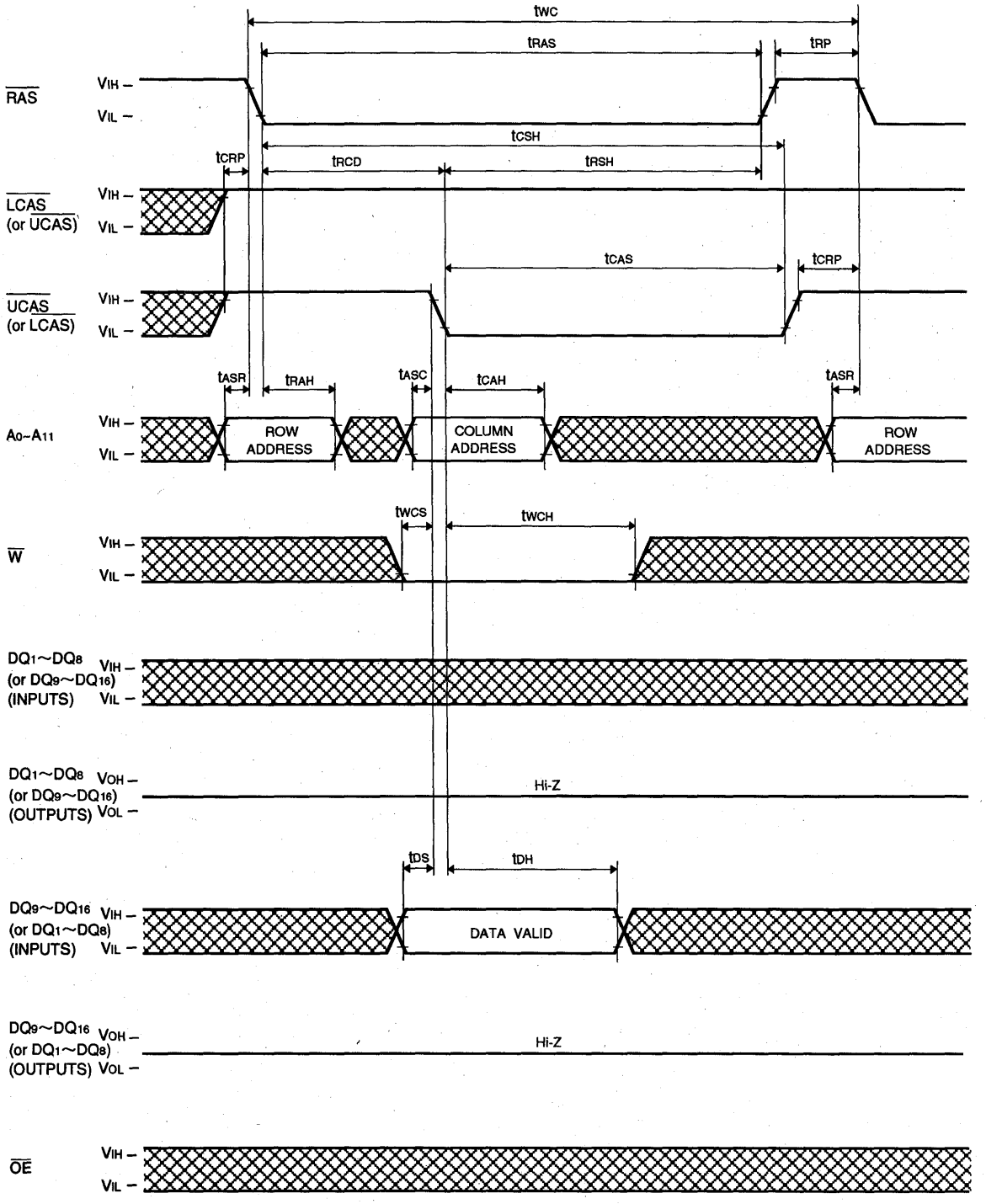
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Early Write Cycle

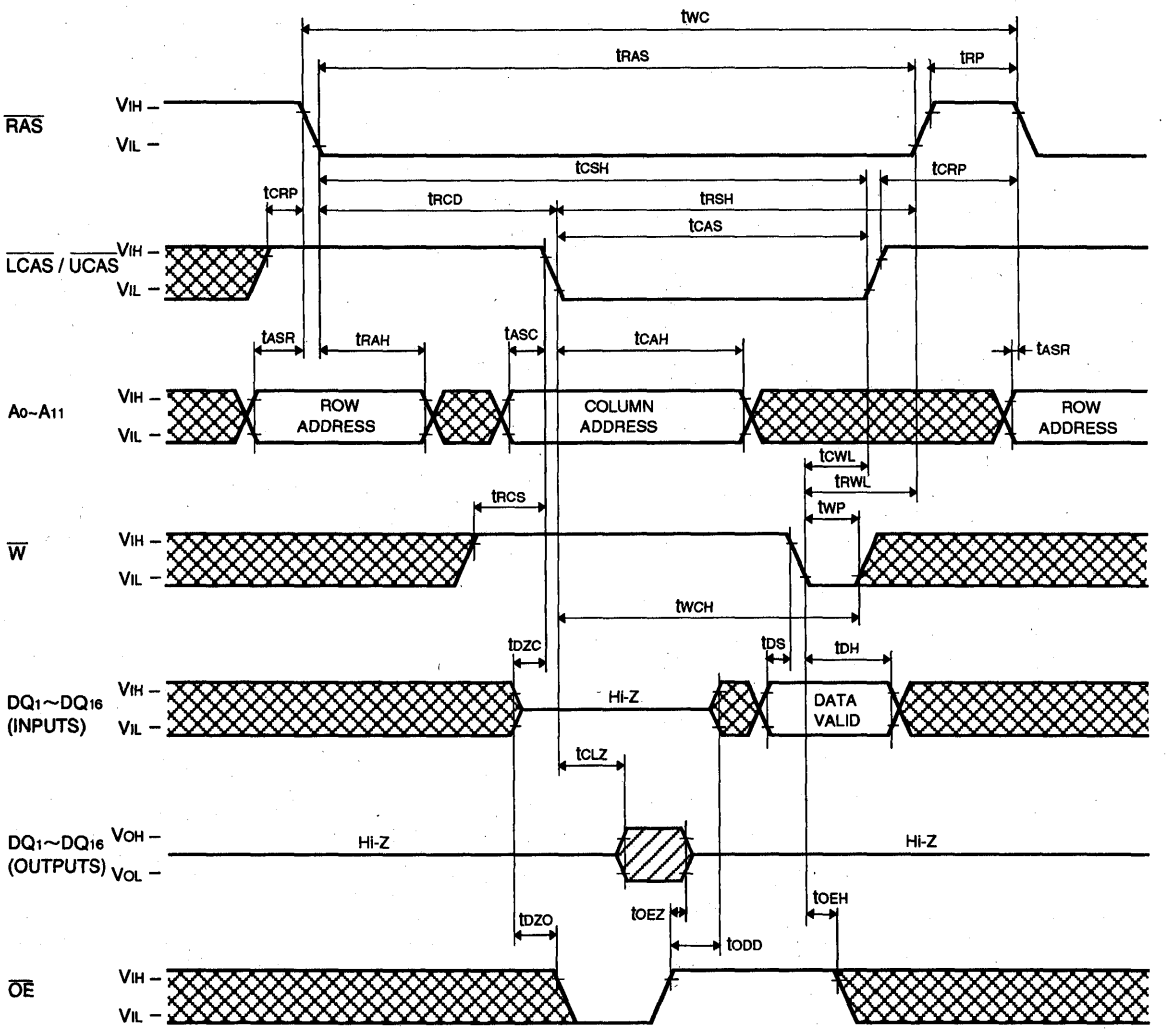


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Early Write Cycle

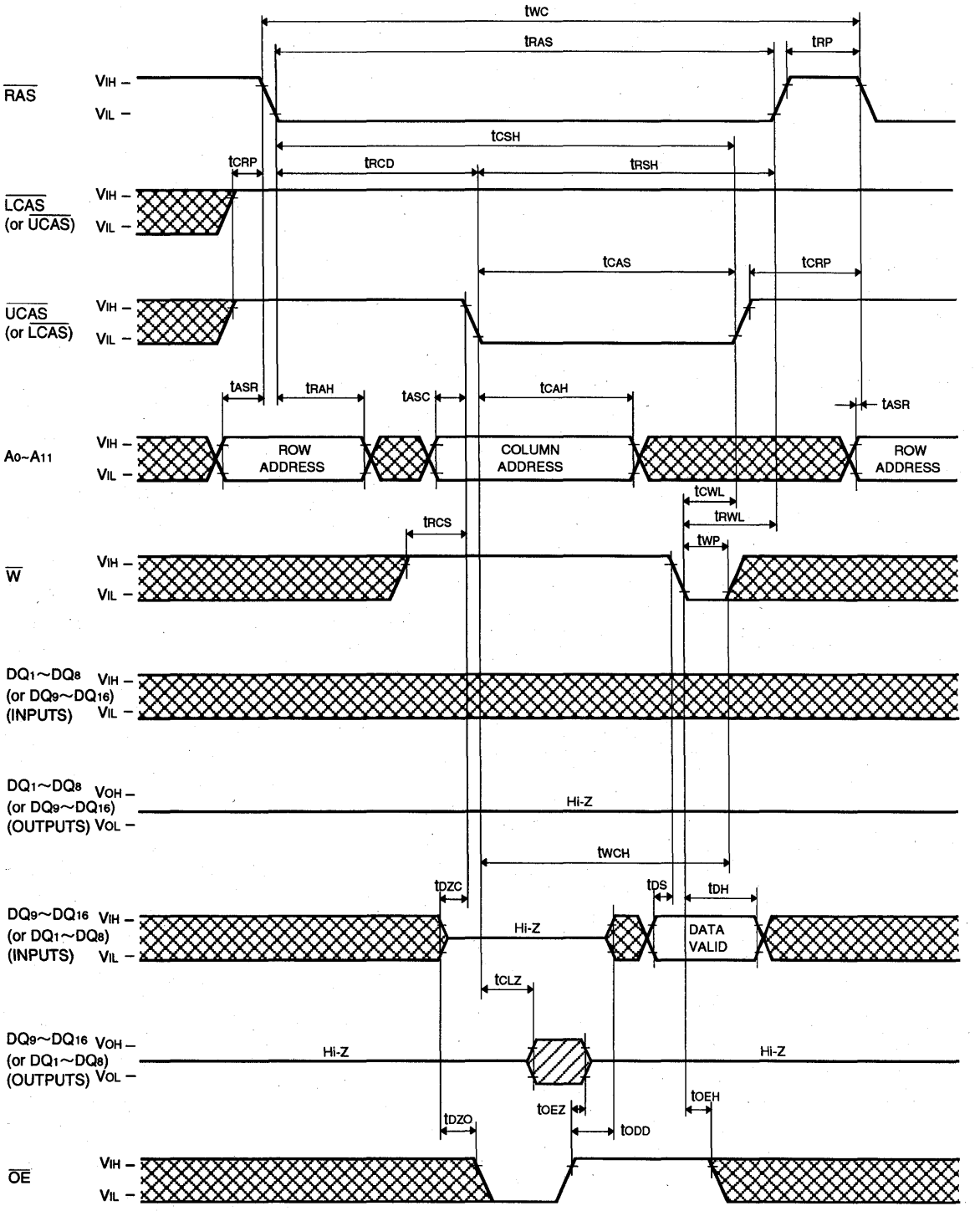


Delayed Write Cycle



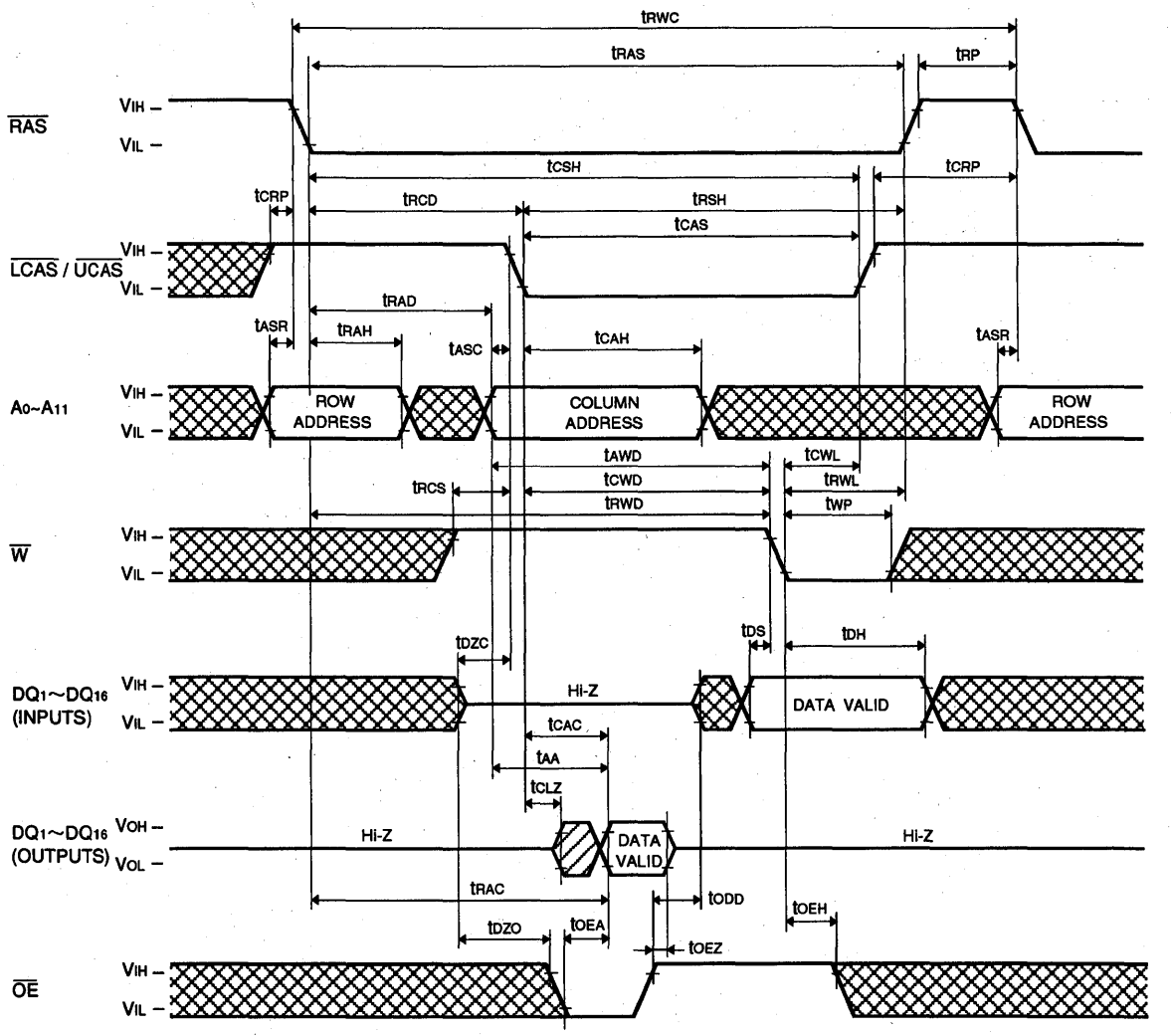
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Delayed Write Cycle



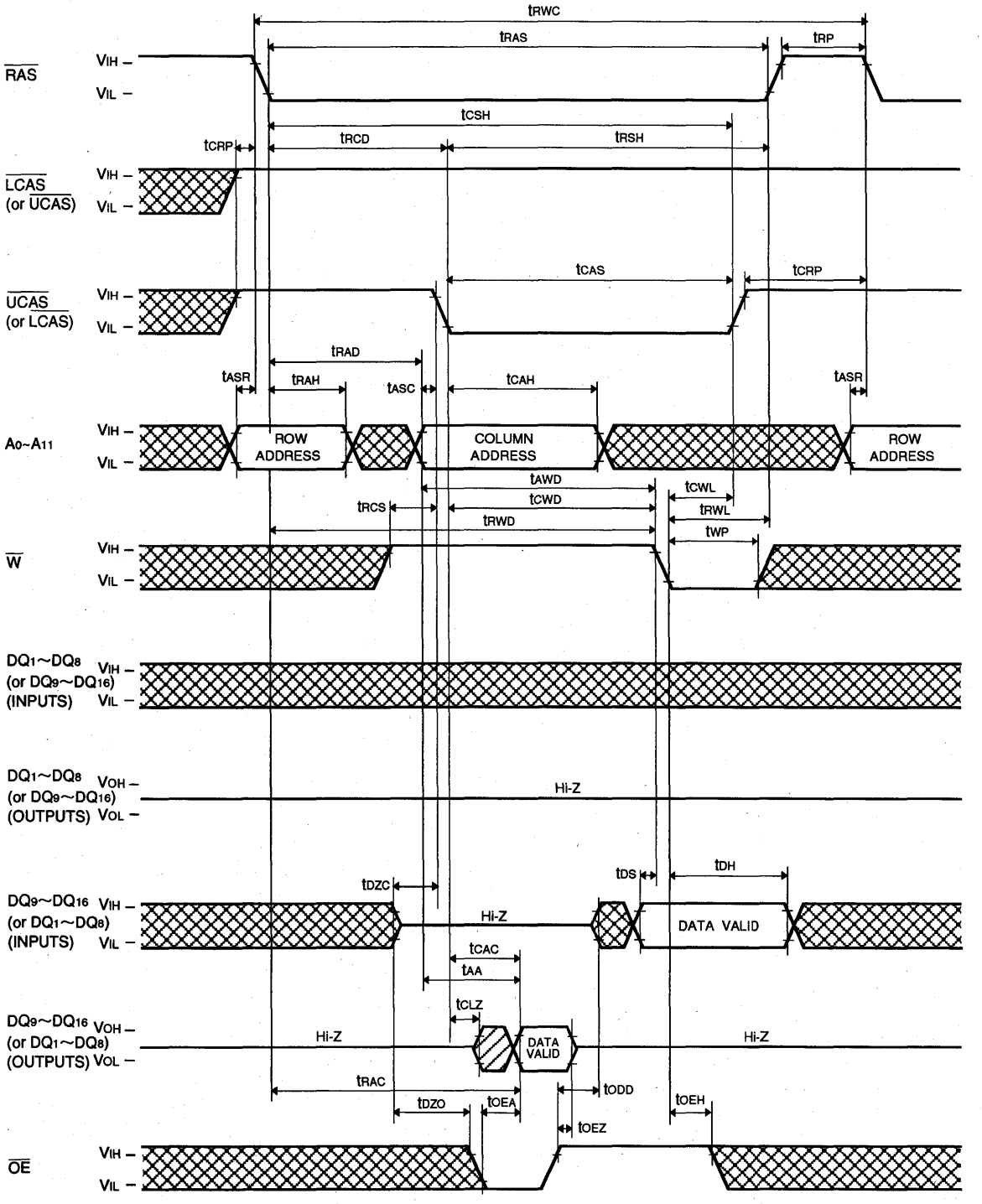
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle



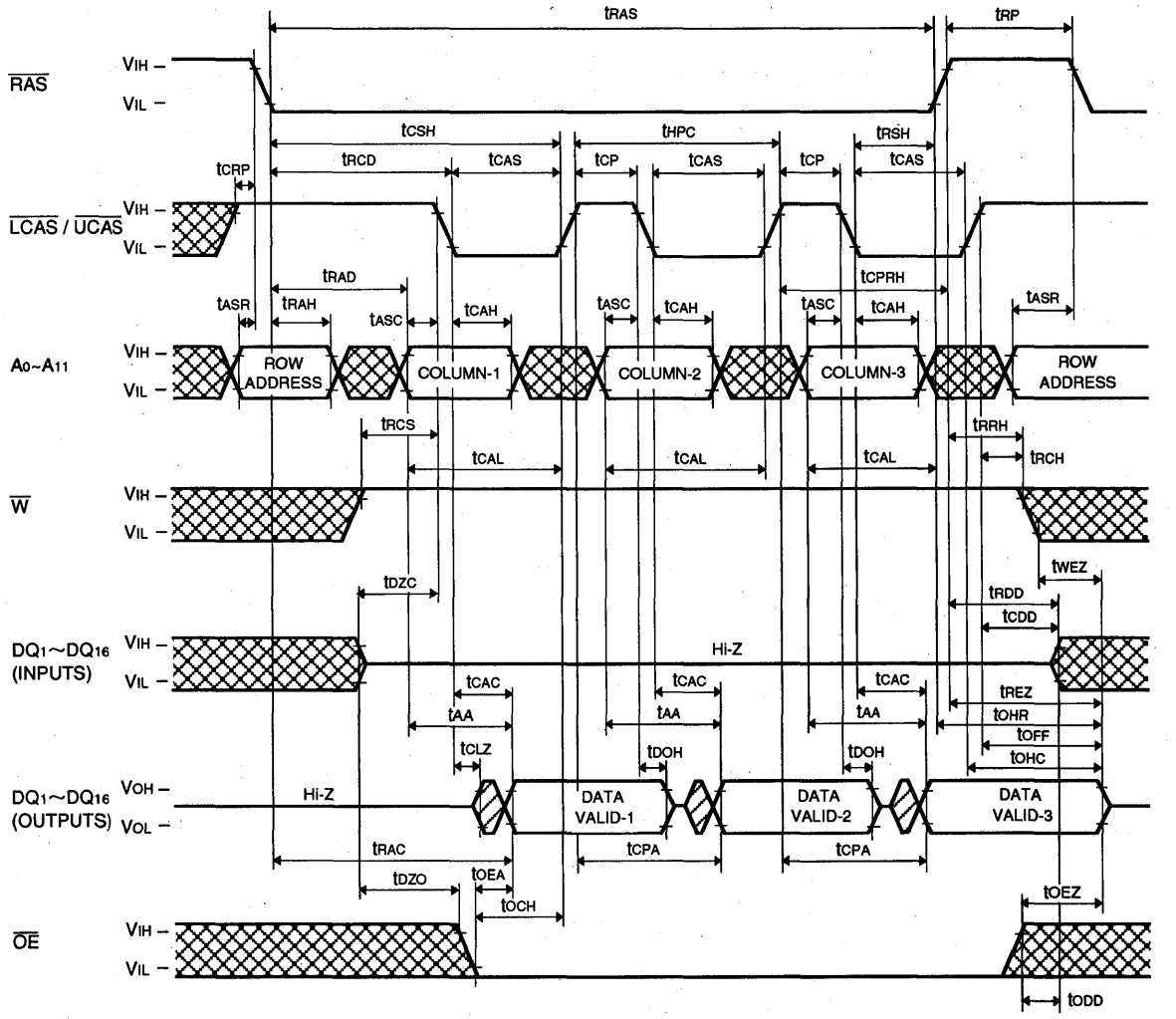
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Read-Write, Read-Modify-Write Cycle

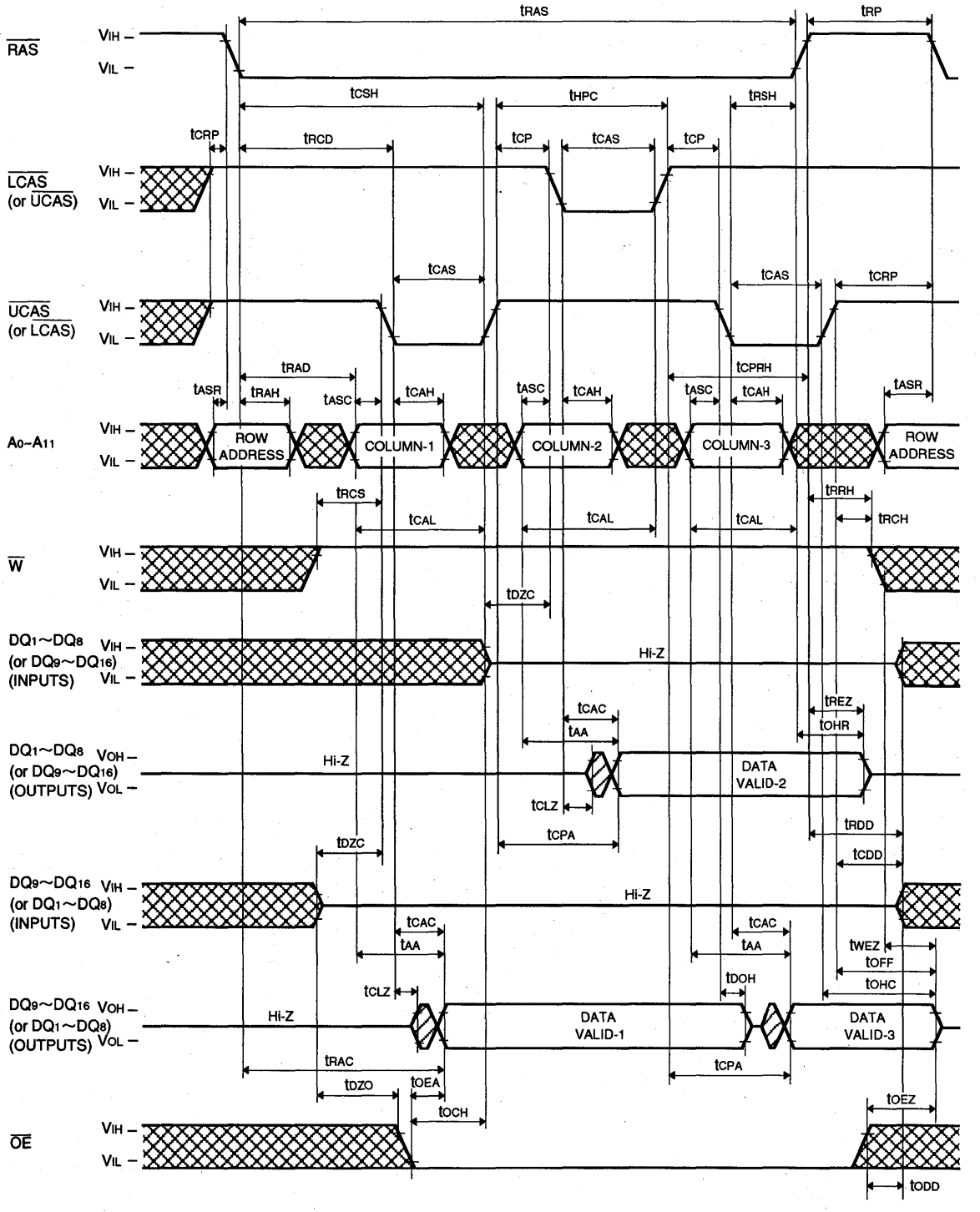


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle

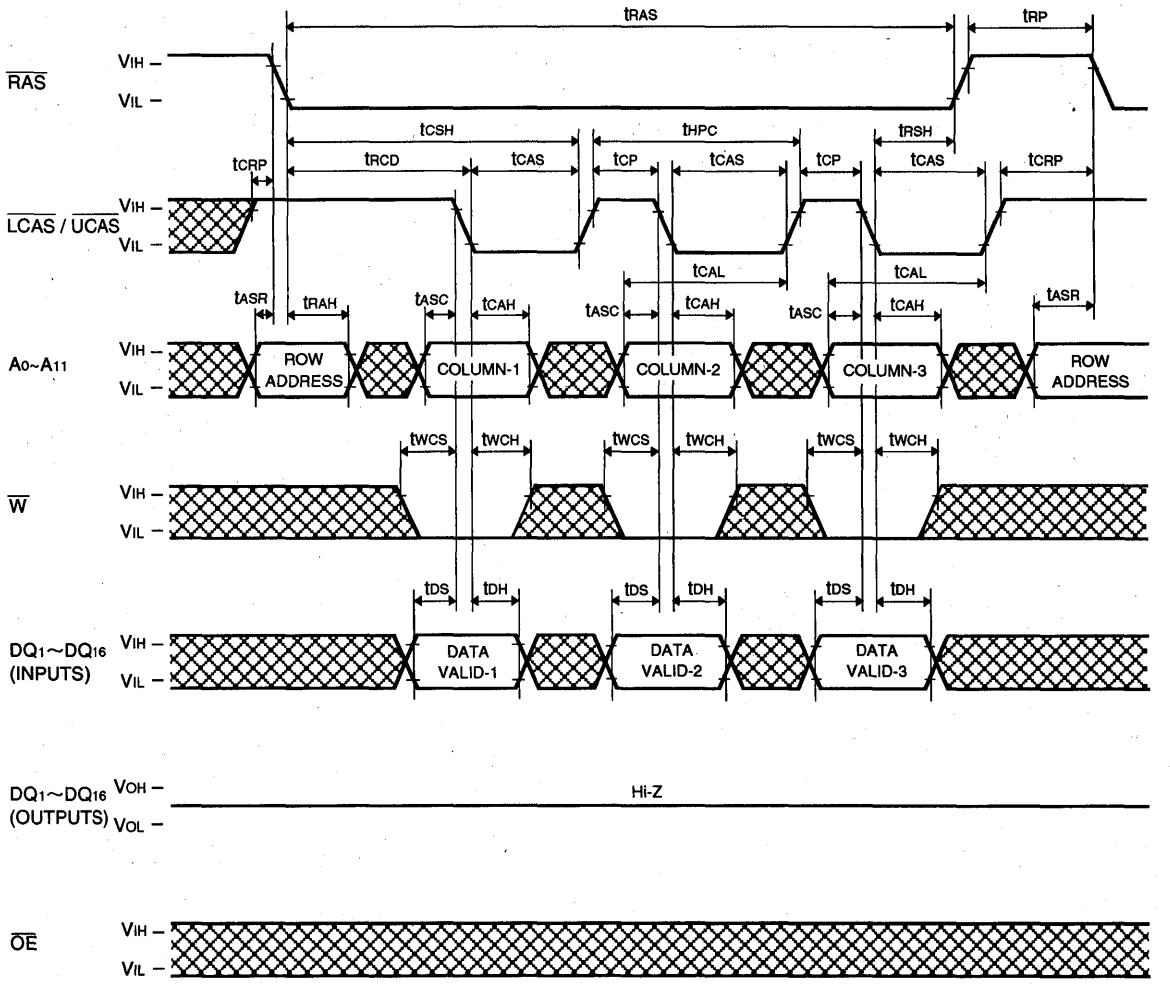


Hyper Page Mode Byte Read Cycle



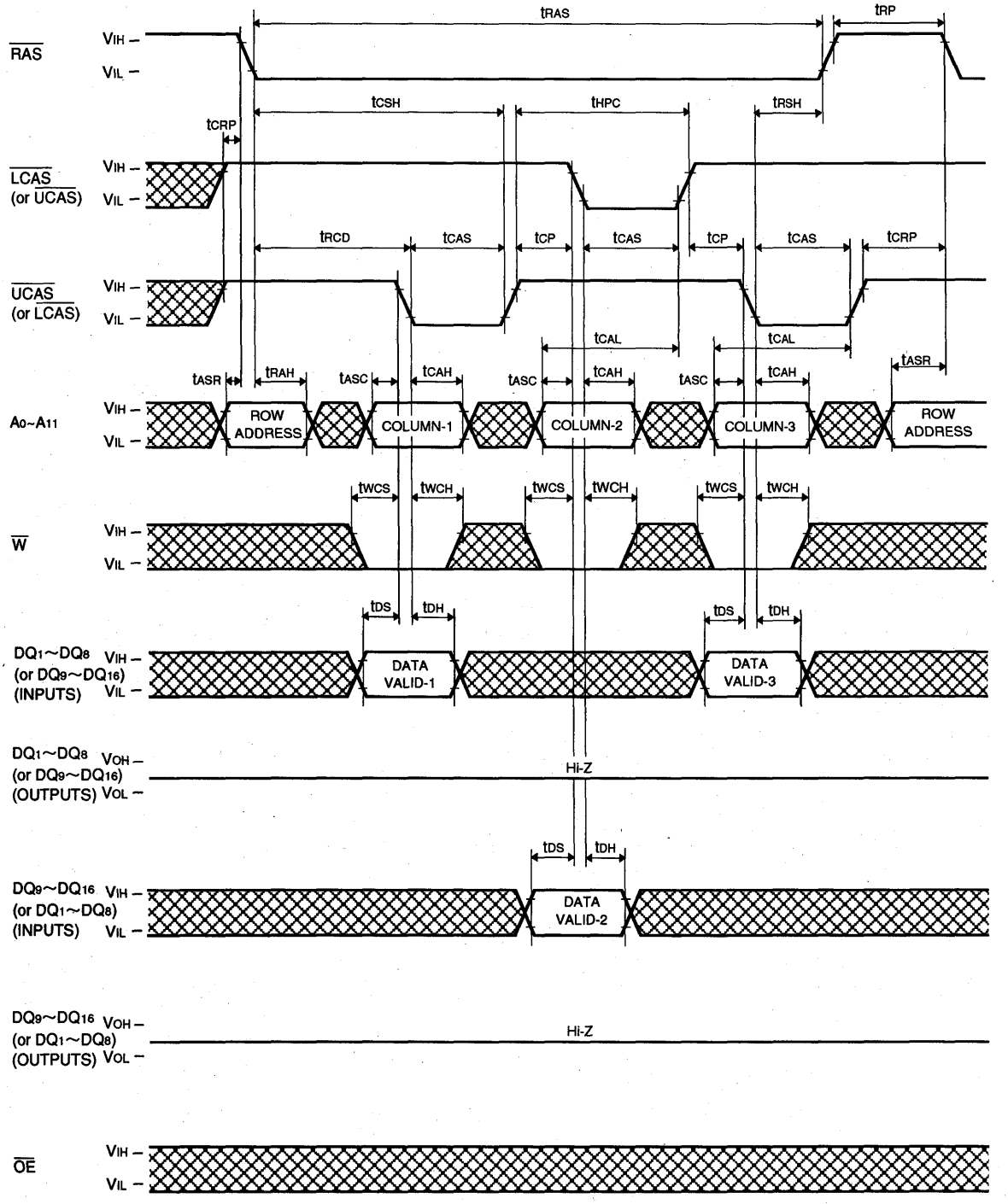
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Early Write Cycle



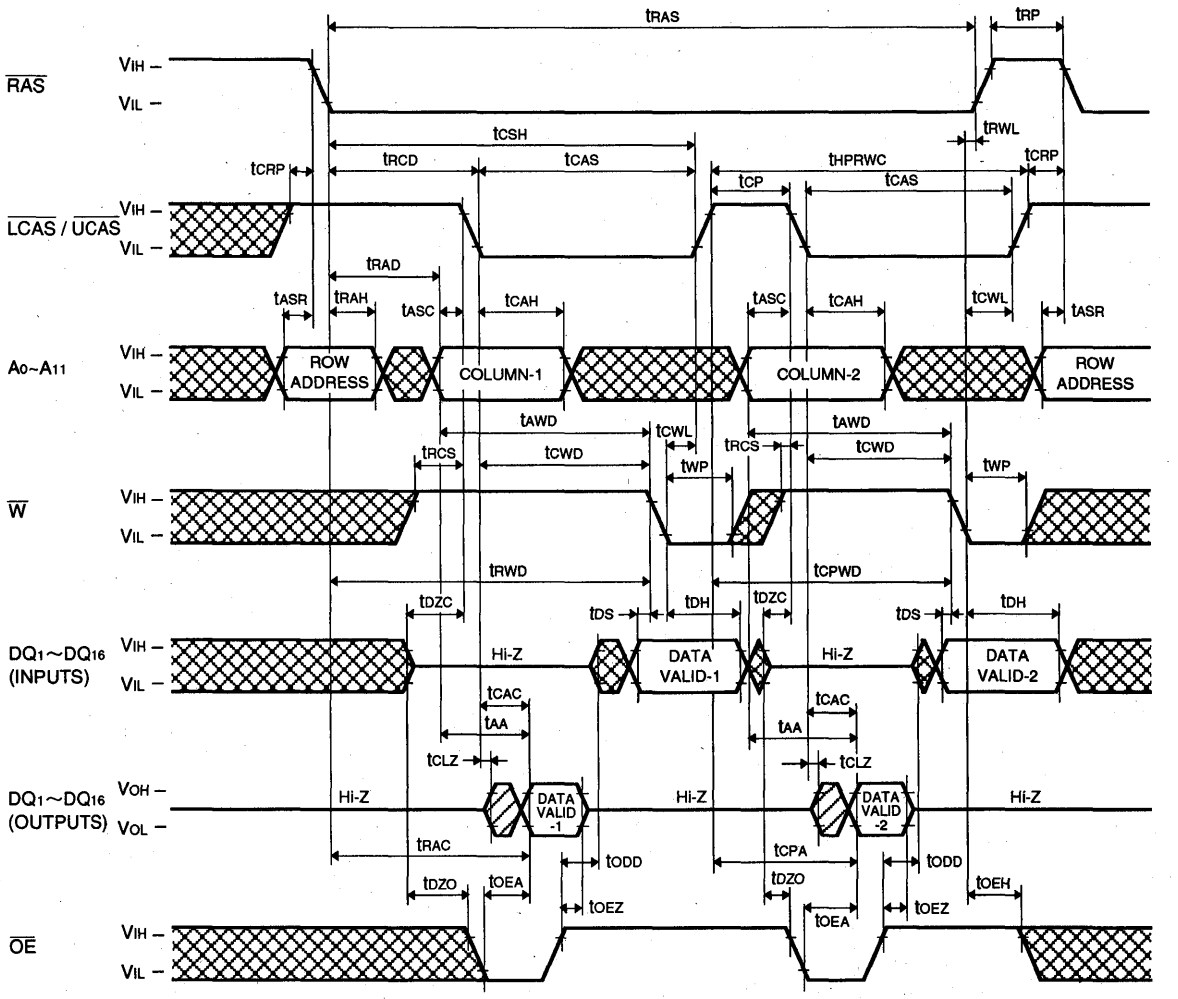
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Early Write Cycle



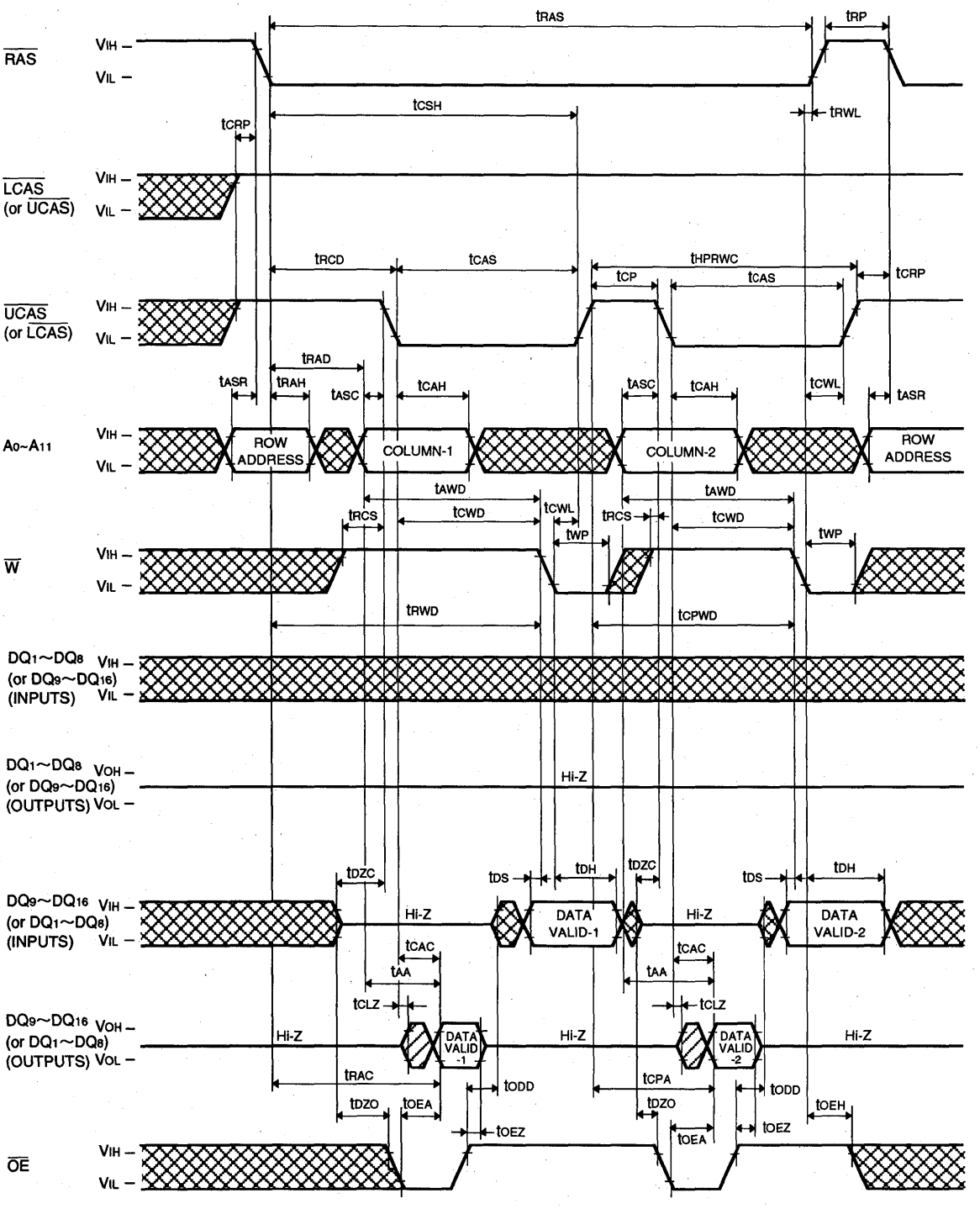
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read-Write, Read-Modify-Write Cycle



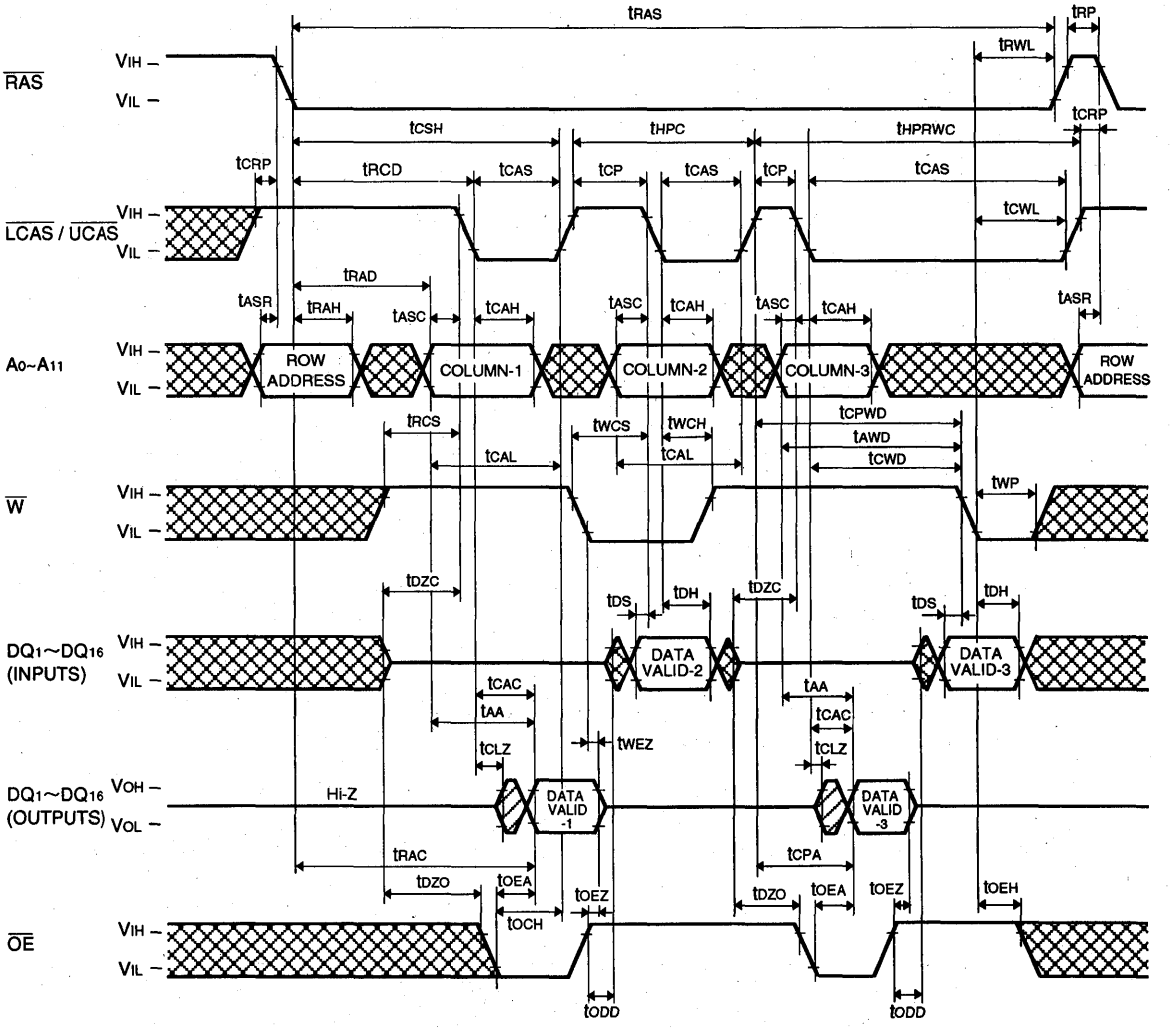
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



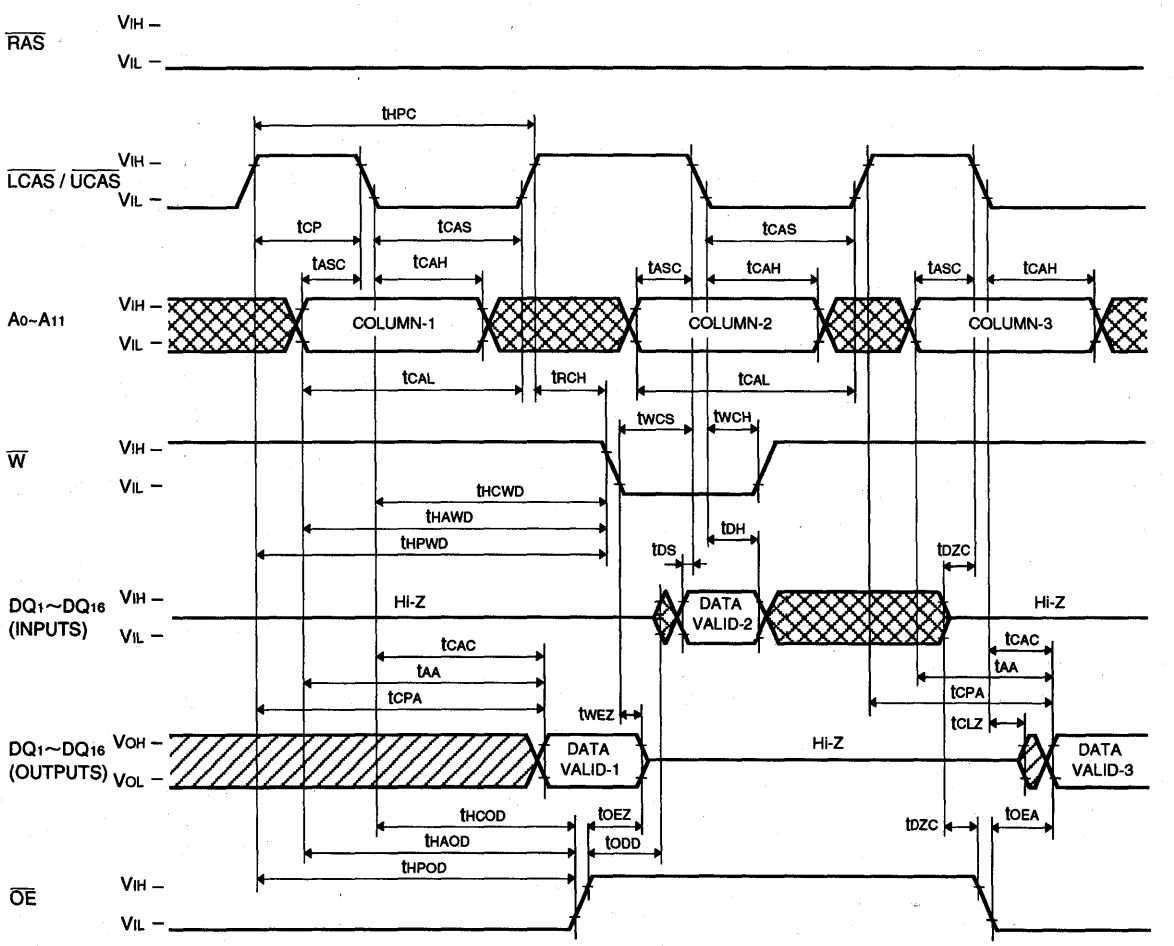
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (1)

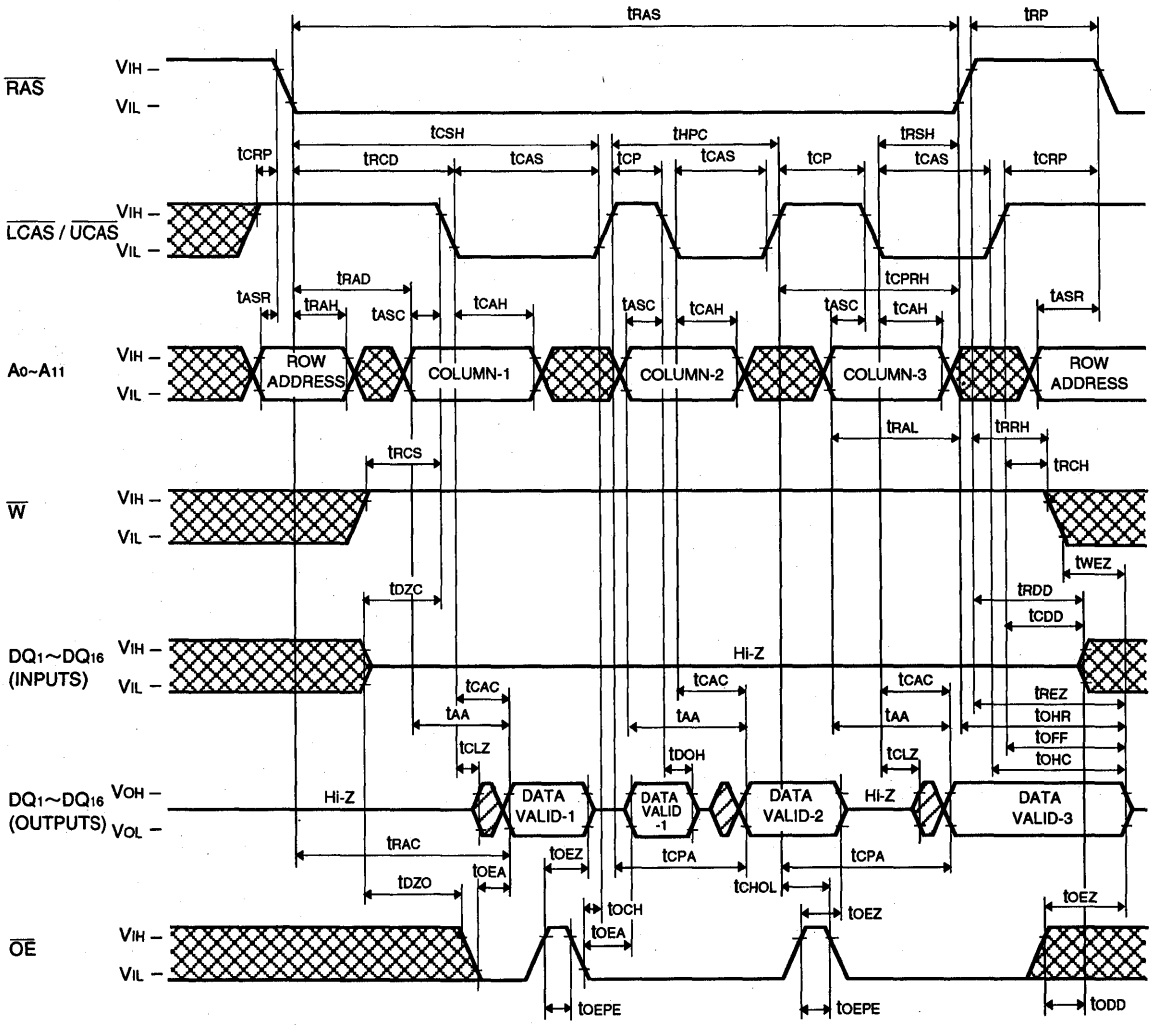


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (2)

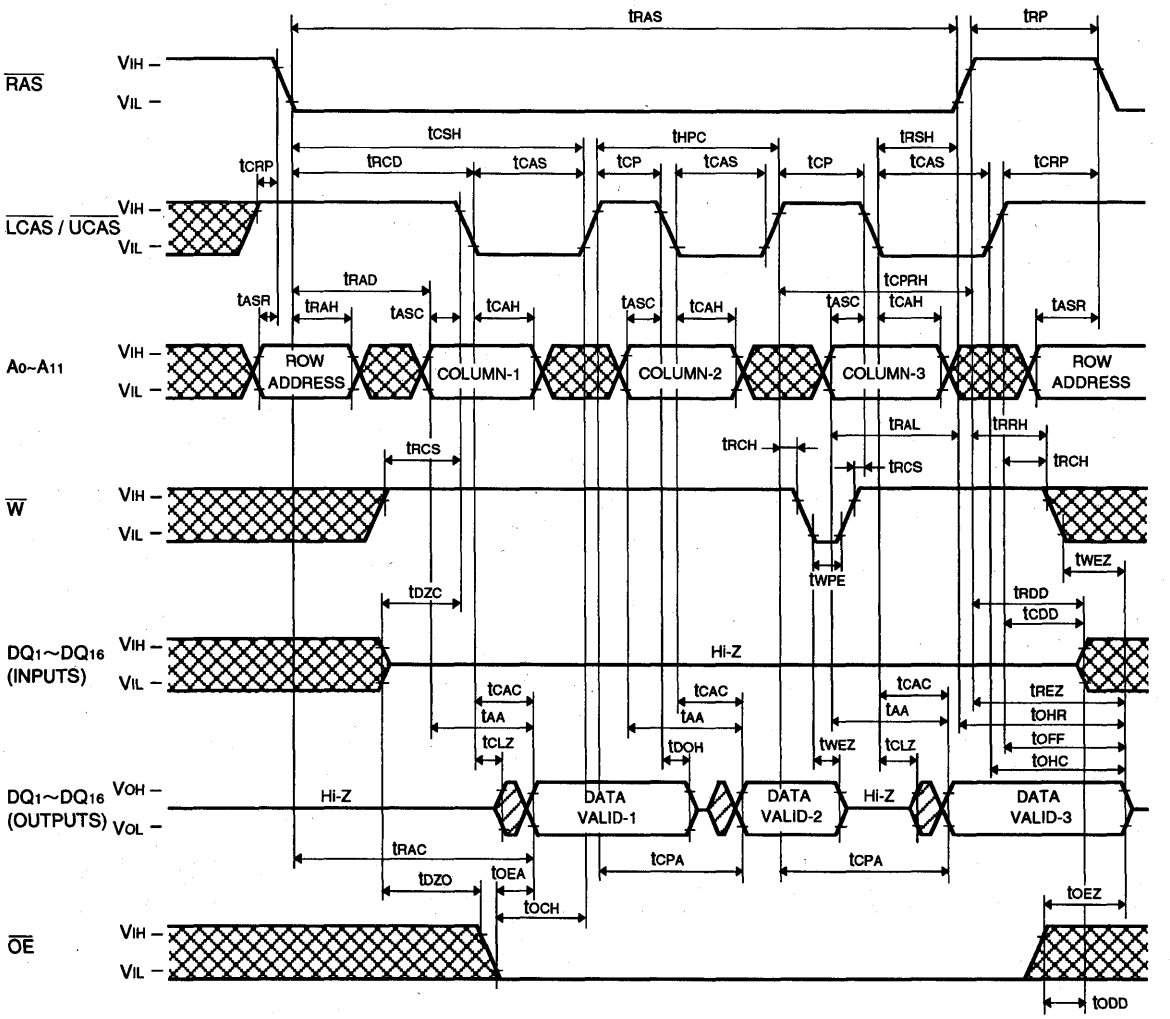


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



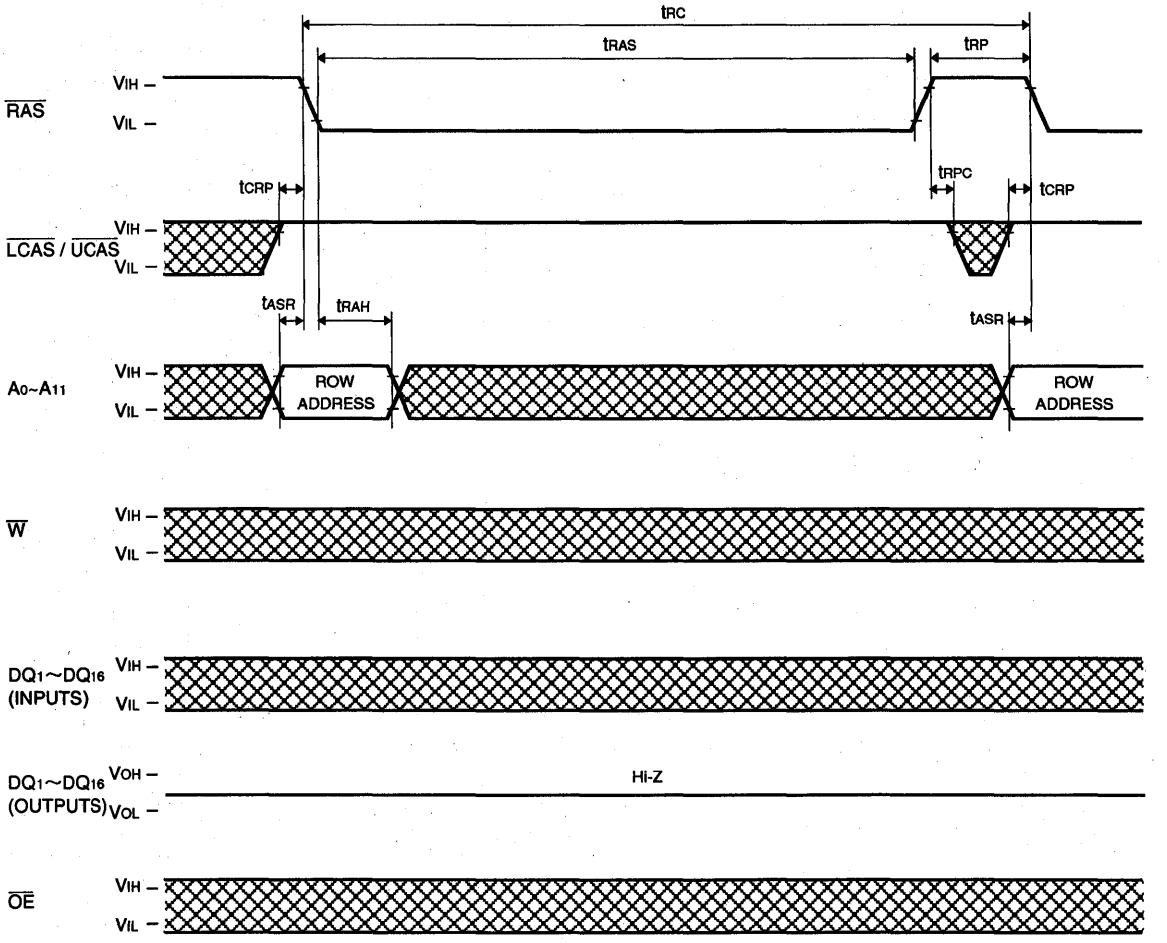
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



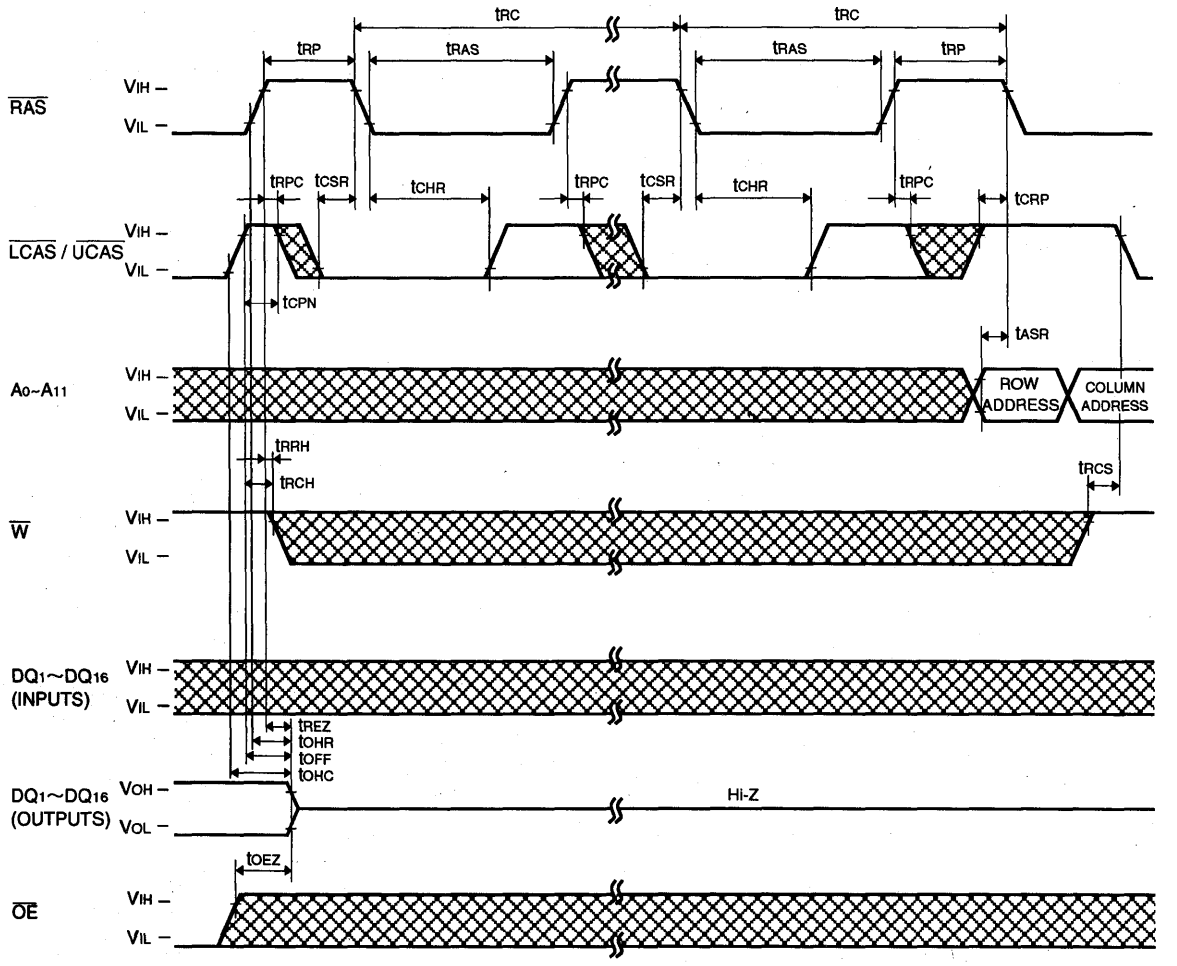
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{\text{RAS}}$-only Refresh Cycle

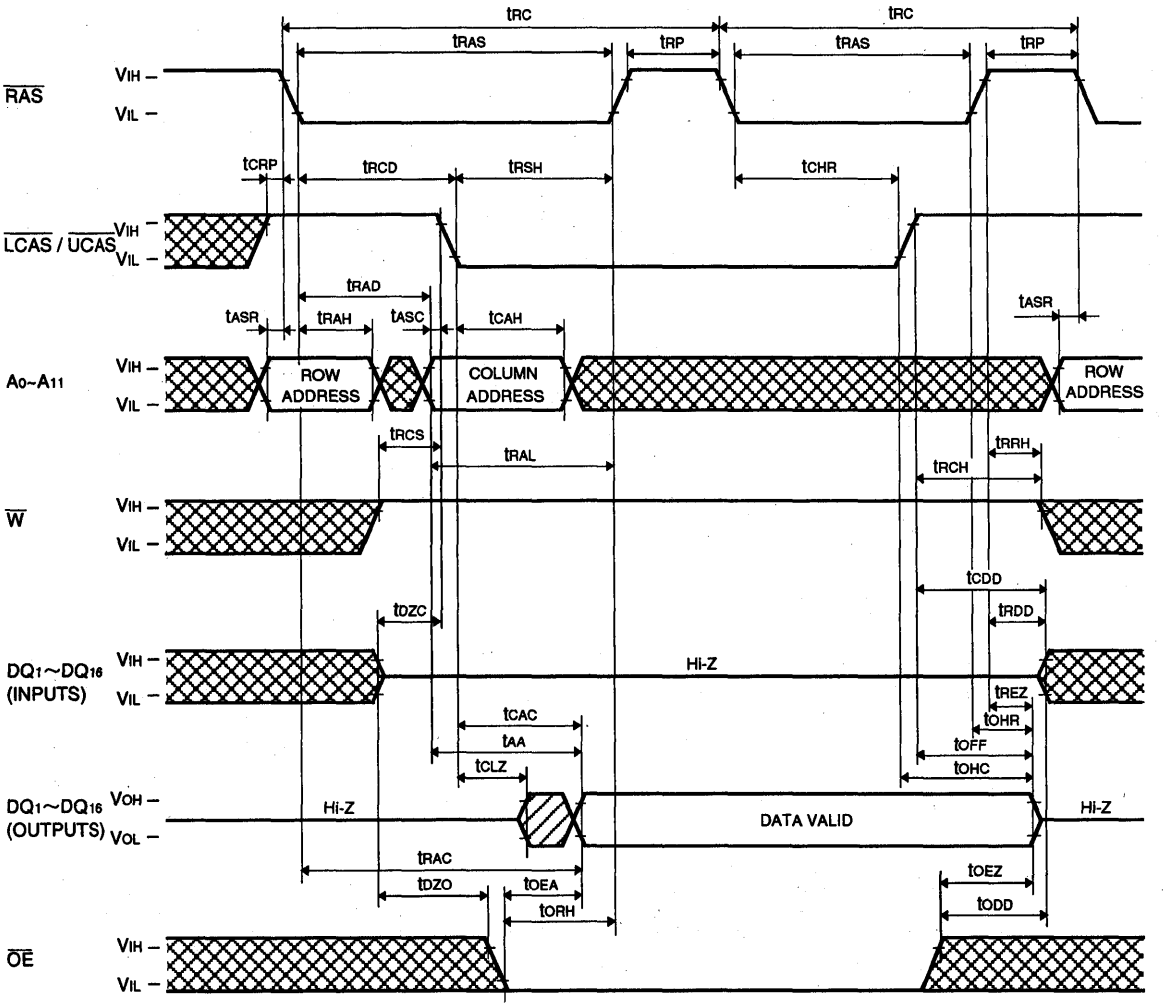


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



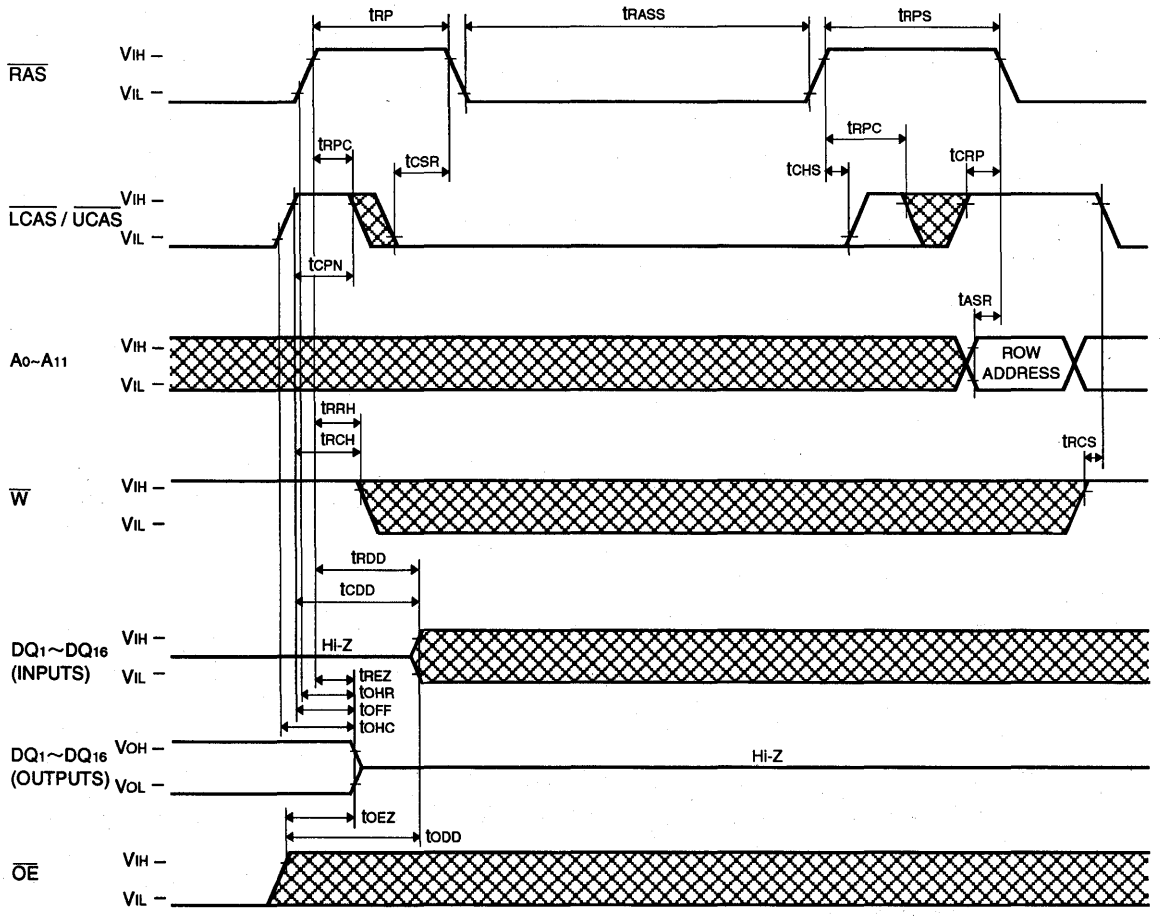
Hidden Refresh Cycle (Read) (Note 30)



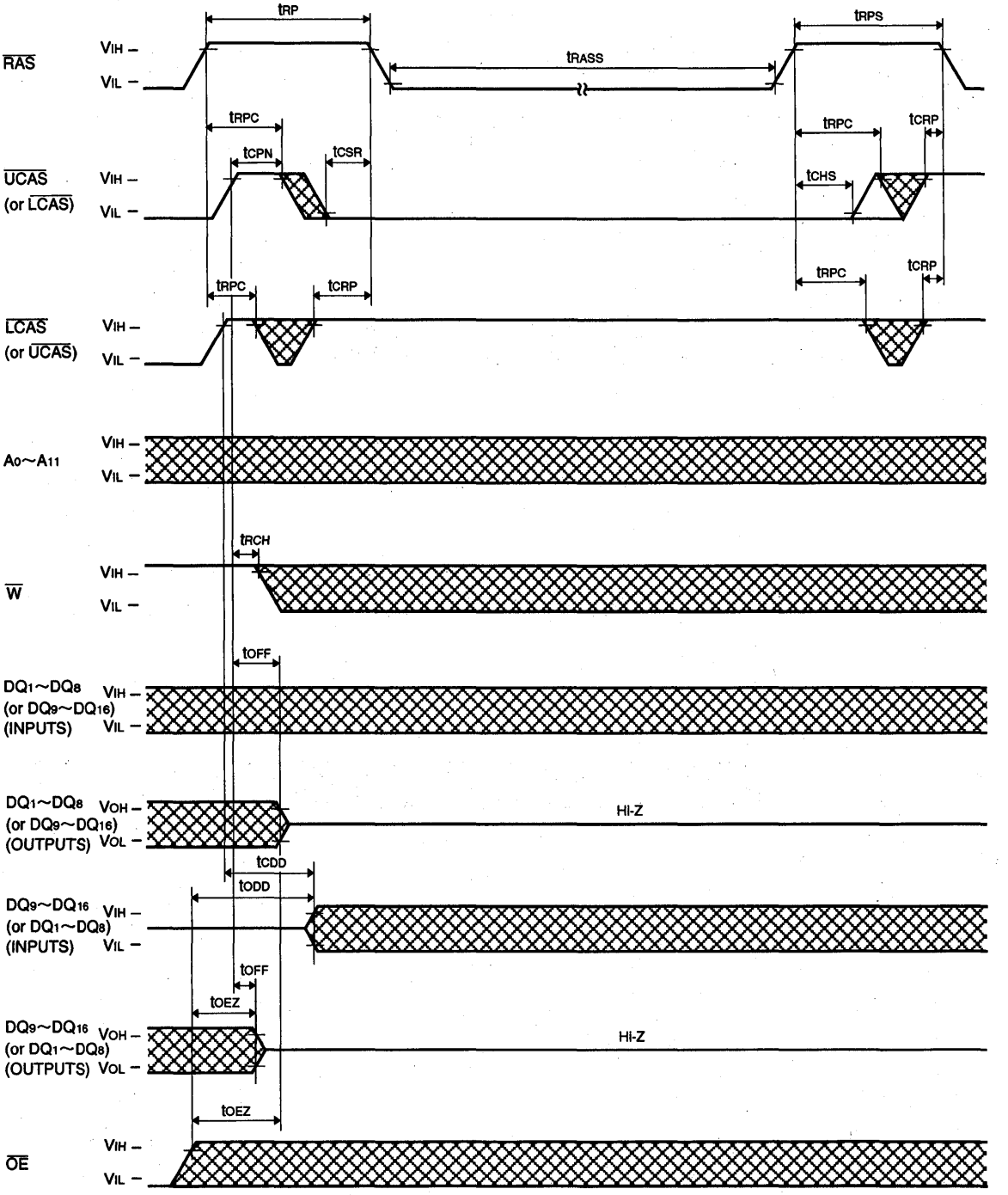
Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle *



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418165CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418165CXX-5,-5S	50	13	25	13	90	810
M5M418165CXX-6,-6S	60	15	30	15	110	675
M5M418165CXX-7,-7S	70	20	35	20	130	585

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M418165Cxx-5,-5S ---------- 990.0mW (Max)
  M5M418165Cxx-6,-6S ---------- 825.0mW (Max)
  M5M418165Cxx-7,-7S ---------- 715.0mW (Max)
- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  * : Applicable to self refresh version (M5M418165CJ,TP-5S,-6S, -7S : option) only

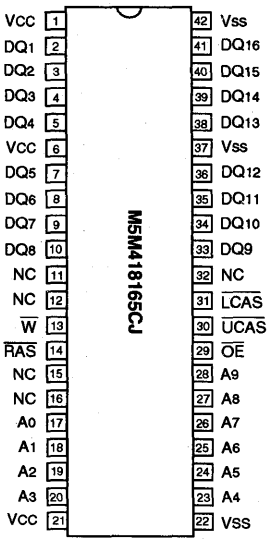
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

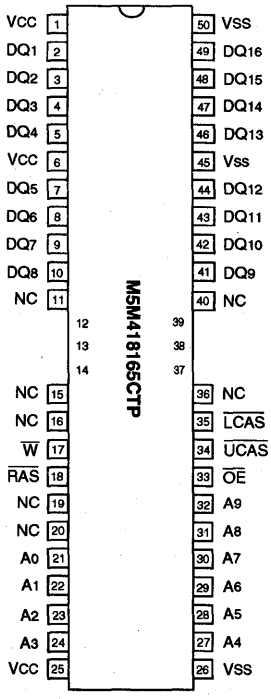
PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+5.0V)
V_{SS}	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

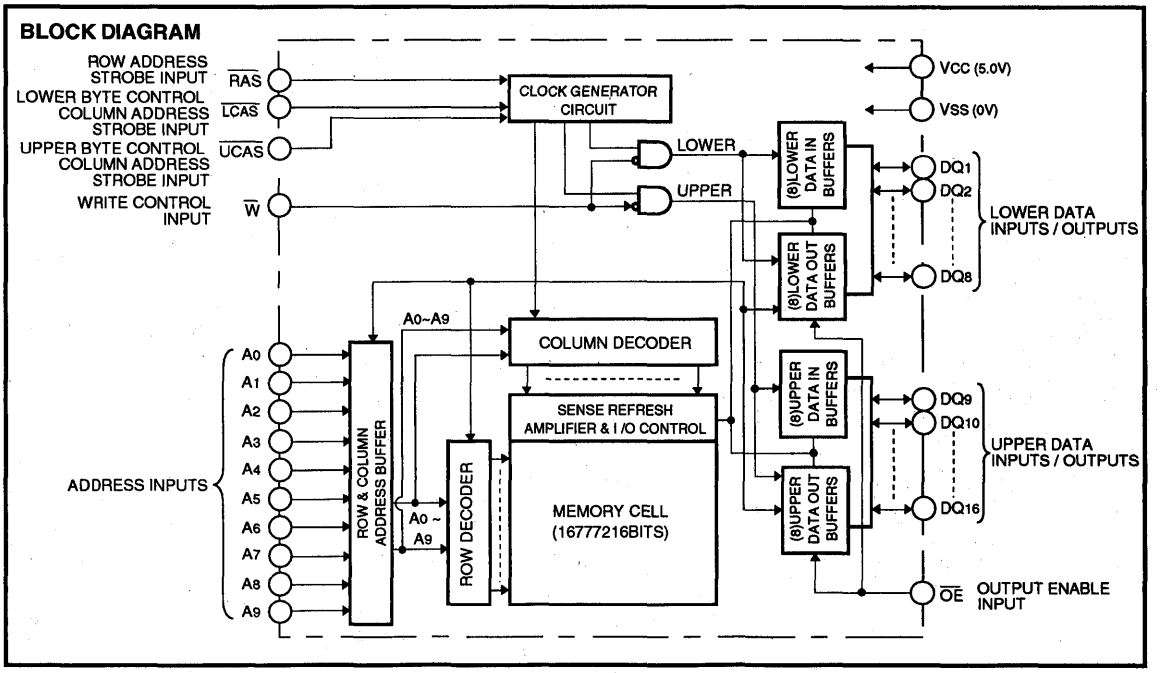
The M5M418165CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1~7	V
V_I	Input voltage		-1~7	V
V_O	Output voltage		-1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M418165C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M418165C-6,-6S				150	
		M5M418165C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc-0.2V output open			1	
						0.3*	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M418165C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M418165C-6,-6S				150	
		M5M418165C-7,-7S				130	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M418165C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			165	mA
		M5M418165C-6,-6S				130	
		M5M418165C-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418165C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M418165C-6,-6S				150	
		M5M418165C-7,-7S				130	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M418165C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0~A9≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125μs, t_{RAS}=t_{RAS}min~1μs			500	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M418165C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 12)	0	13	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\,\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418165CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or $\overline{OE}$ goes back to VIH) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	20		25		30		ns
tHPRWC	Hyper page mode read write/read modify write cycle time	57		66		79		ns
tDOH	Output hold time from $\overline{CAS}$ low	5		5		5		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note 27)	8	13	10	16	10	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	45		52		62		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, address to $\overline{W}$ low after read	52		62		72		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	62		72		82		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
tHAOD	Delay time, address to $\overline{OE}$ high after read	25		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M418165C-5,-5S		M5M418165C-6,-6S		M5M418165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

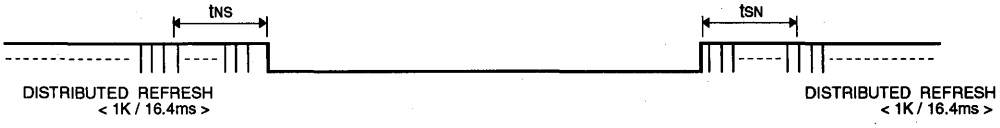
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418165C-5S		M5M418165C-6S		M5M418165C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

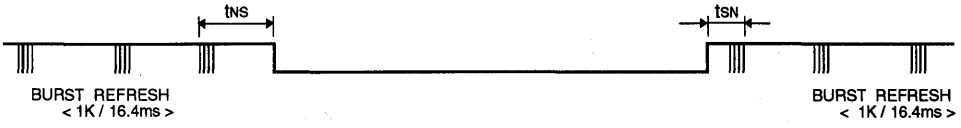
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 16.4ms$ and $t_{SN} \leqq 16.4ms$.



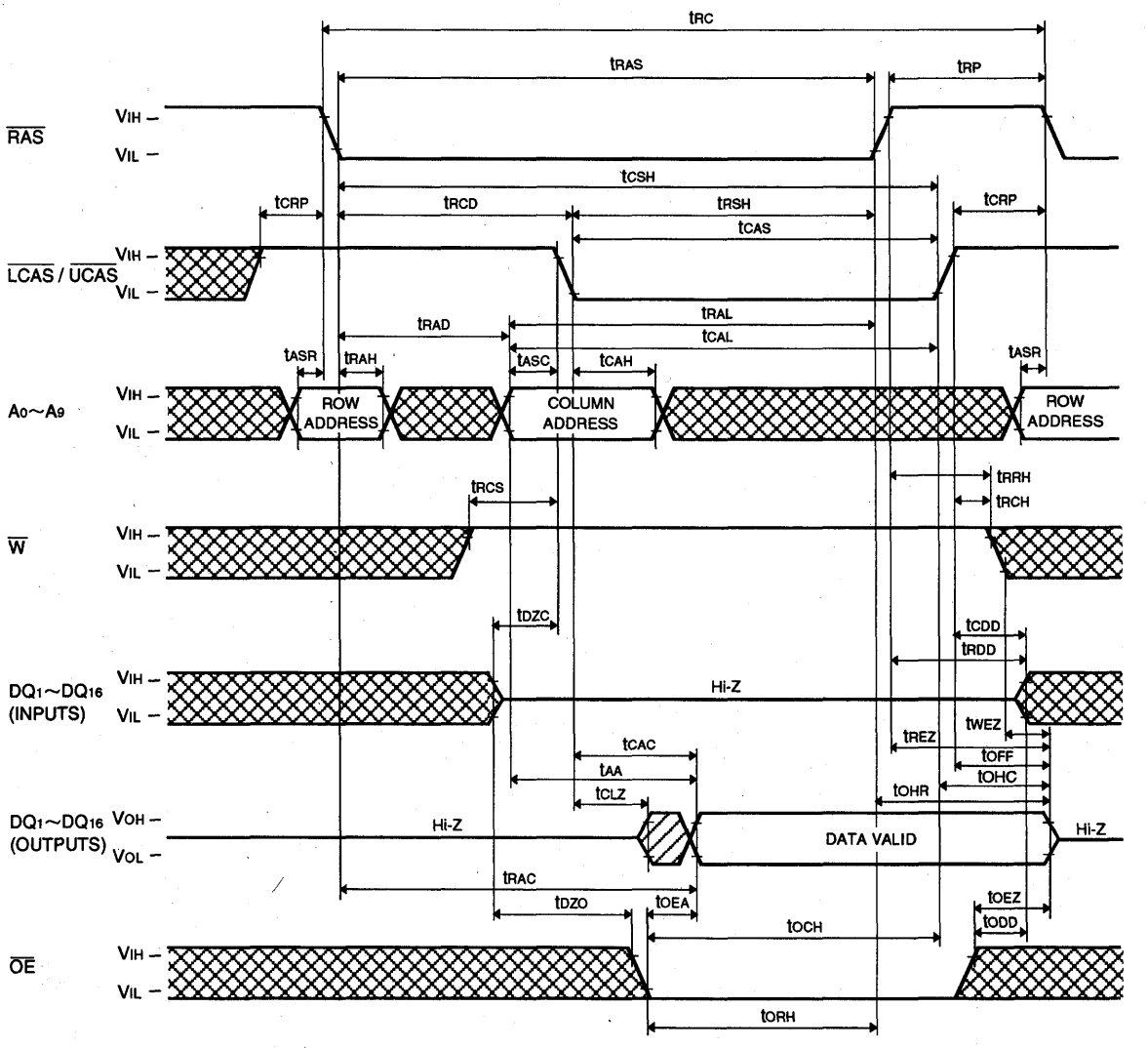
(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 16.4ms$.



Timing Diagrams (Note 29)

Read Cycle

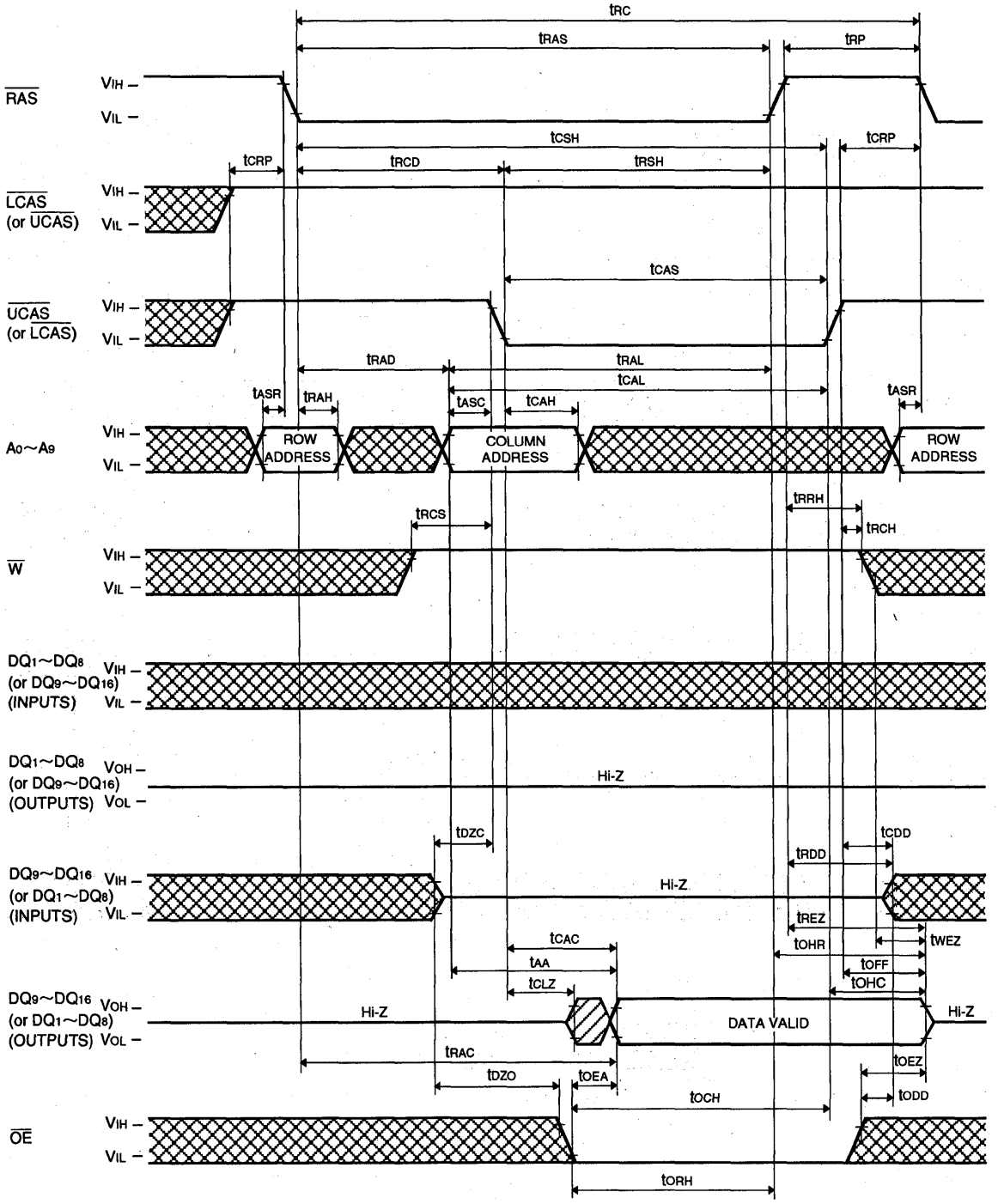


Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

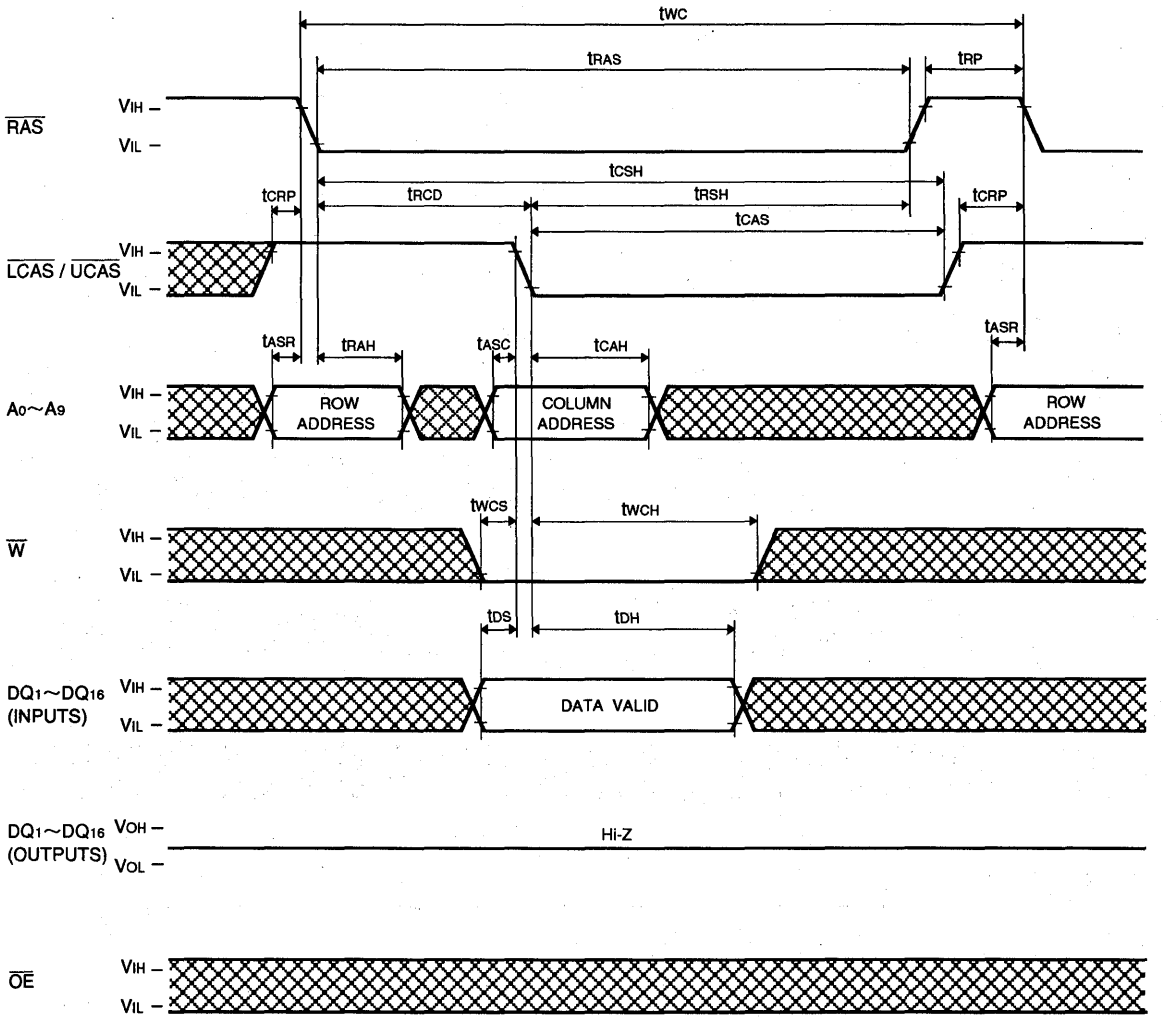
Indicates the invalid output.

Byte Read Cycle

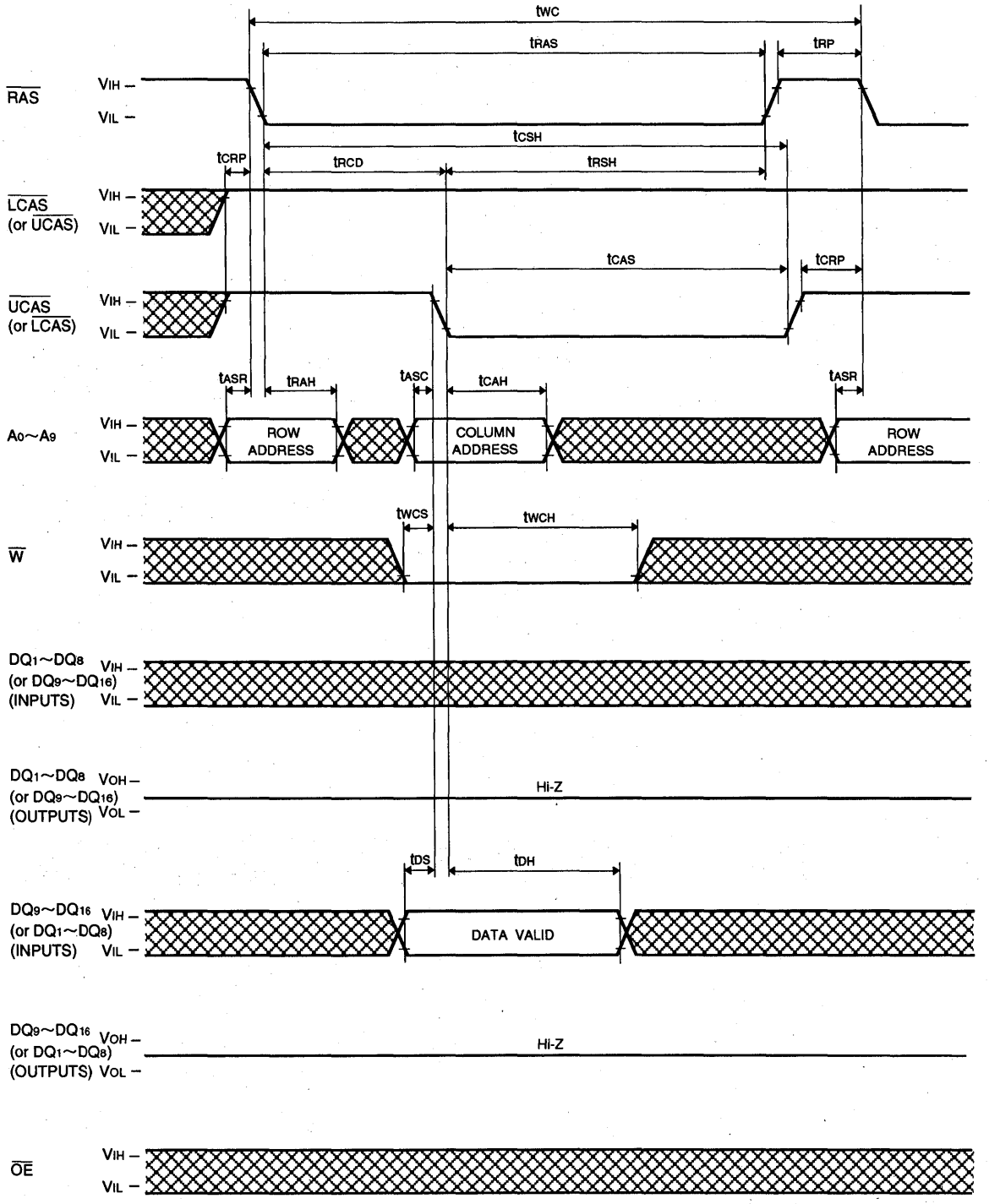


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Early Write Cycle

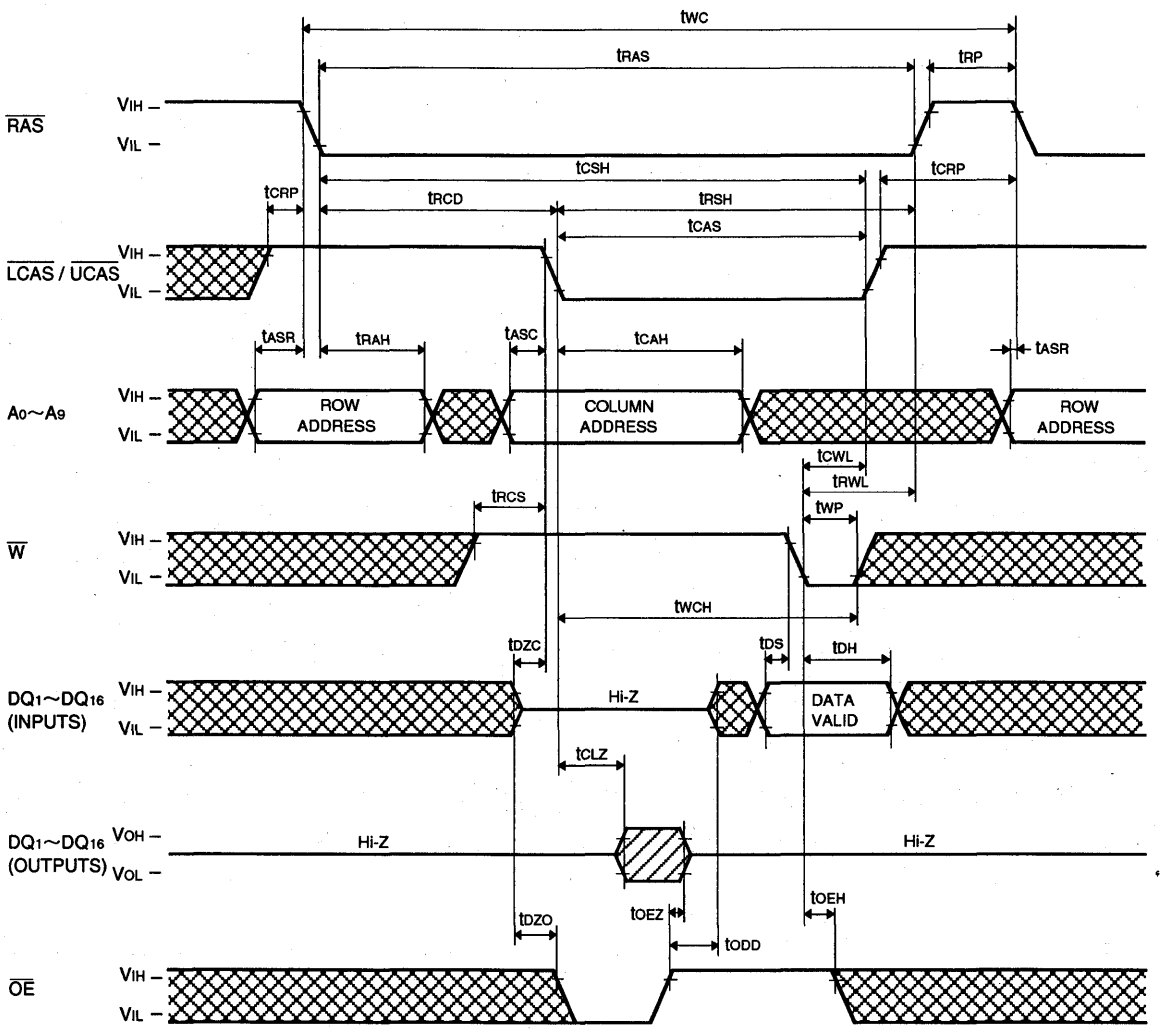


Byte Early Write Cycle

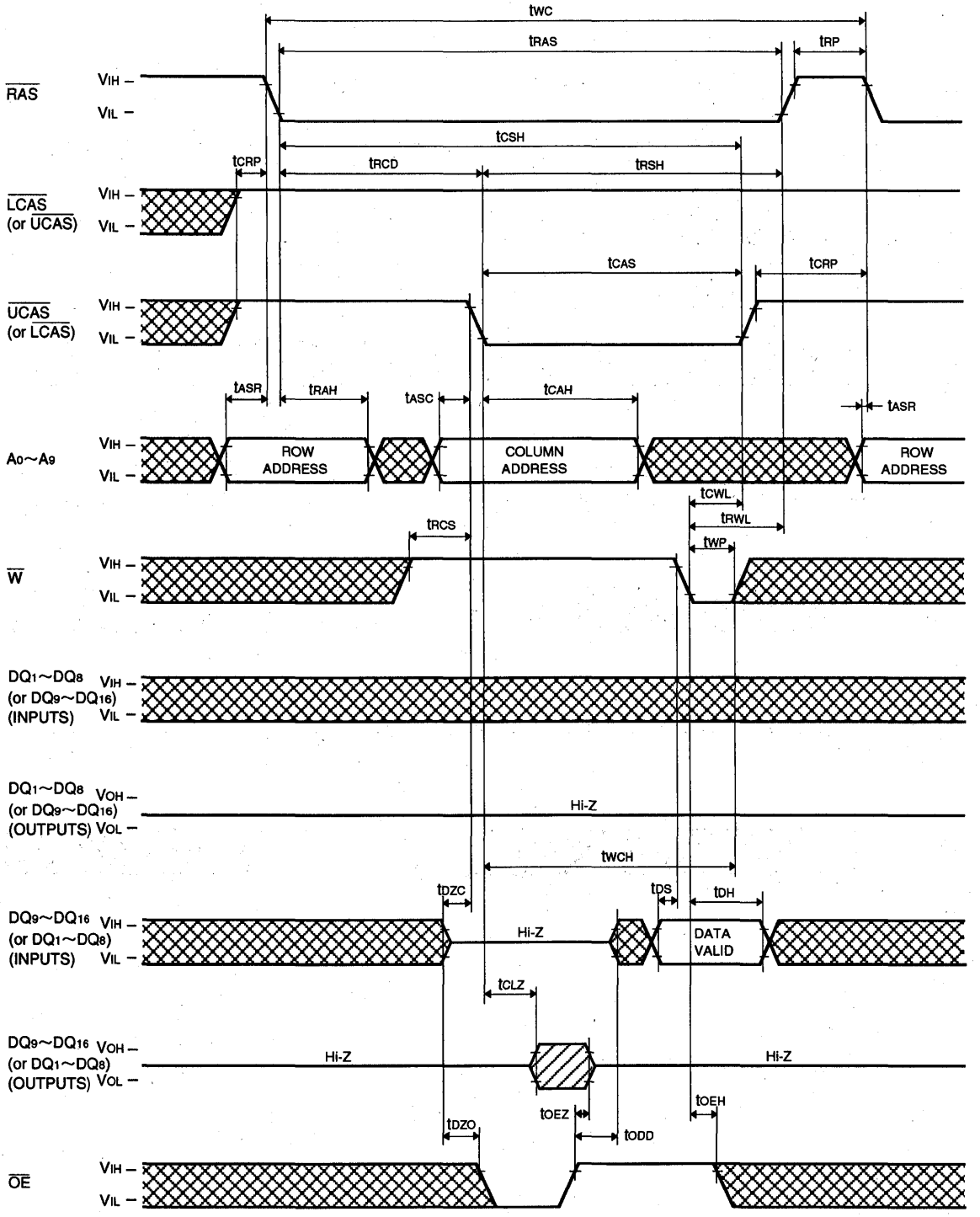


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Delayed Write Cycle



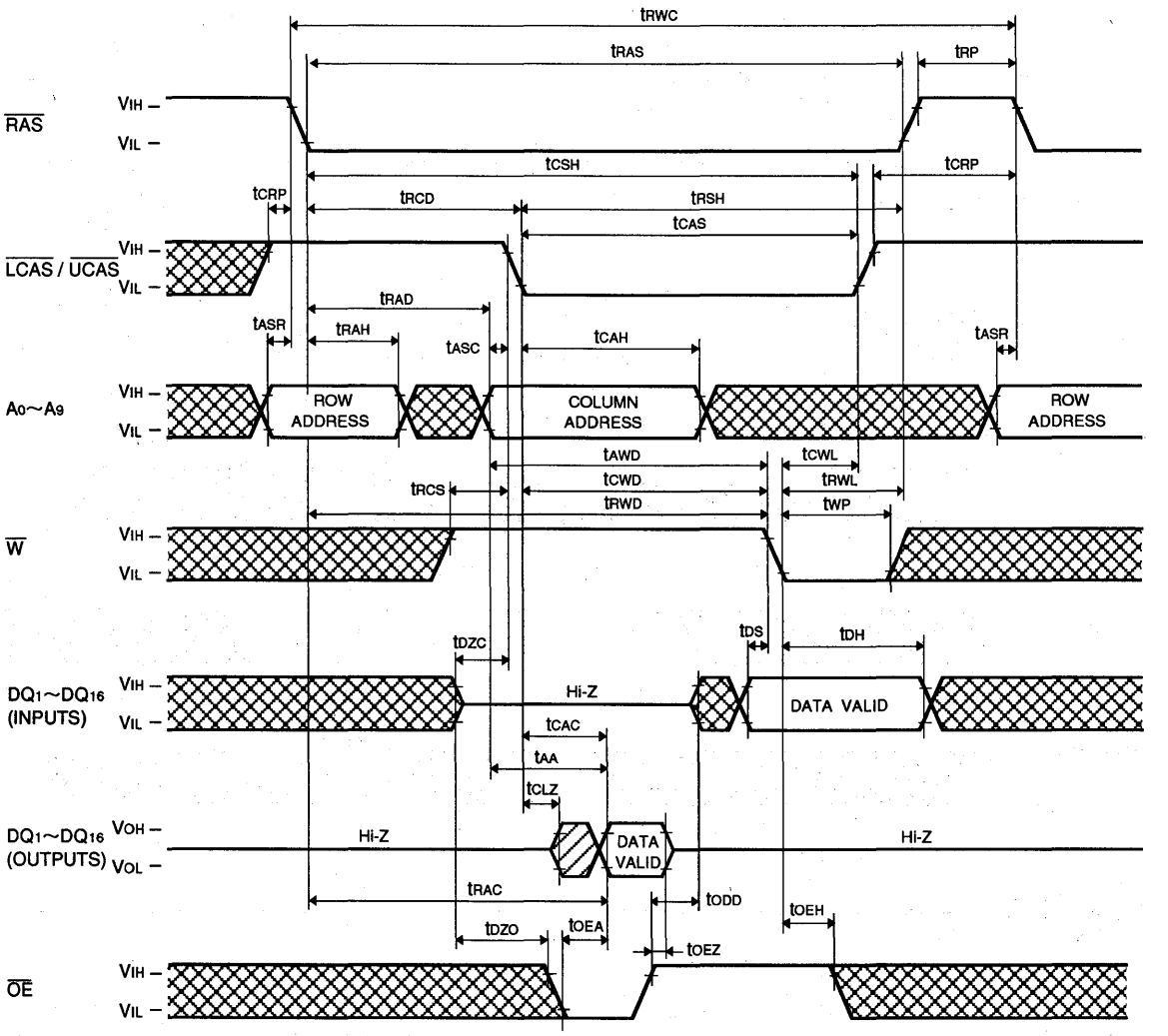
Byte Delayed Write Cycle



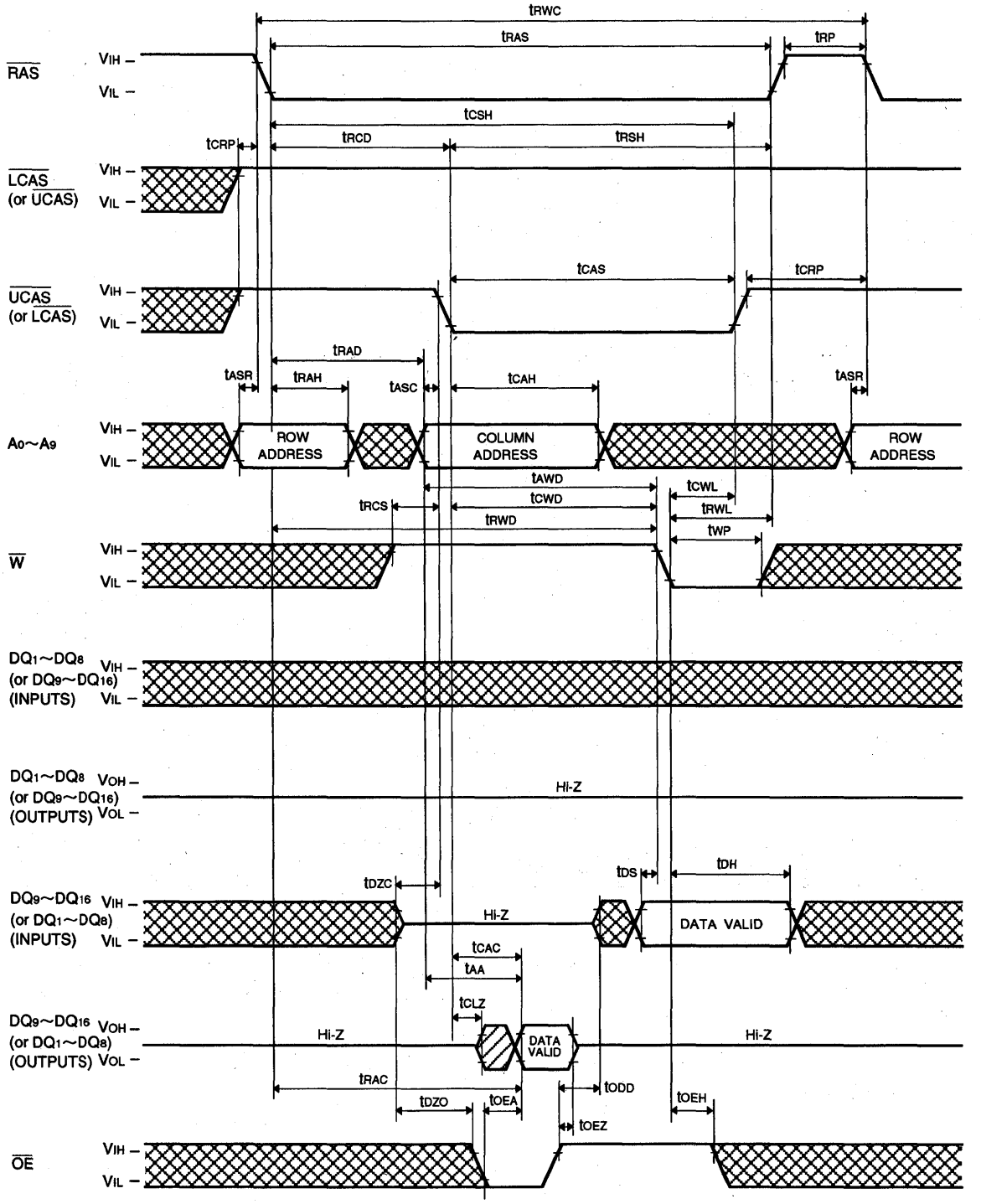
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M418165CJ,TP-5,-6,-7,-5S,-6S,-7S

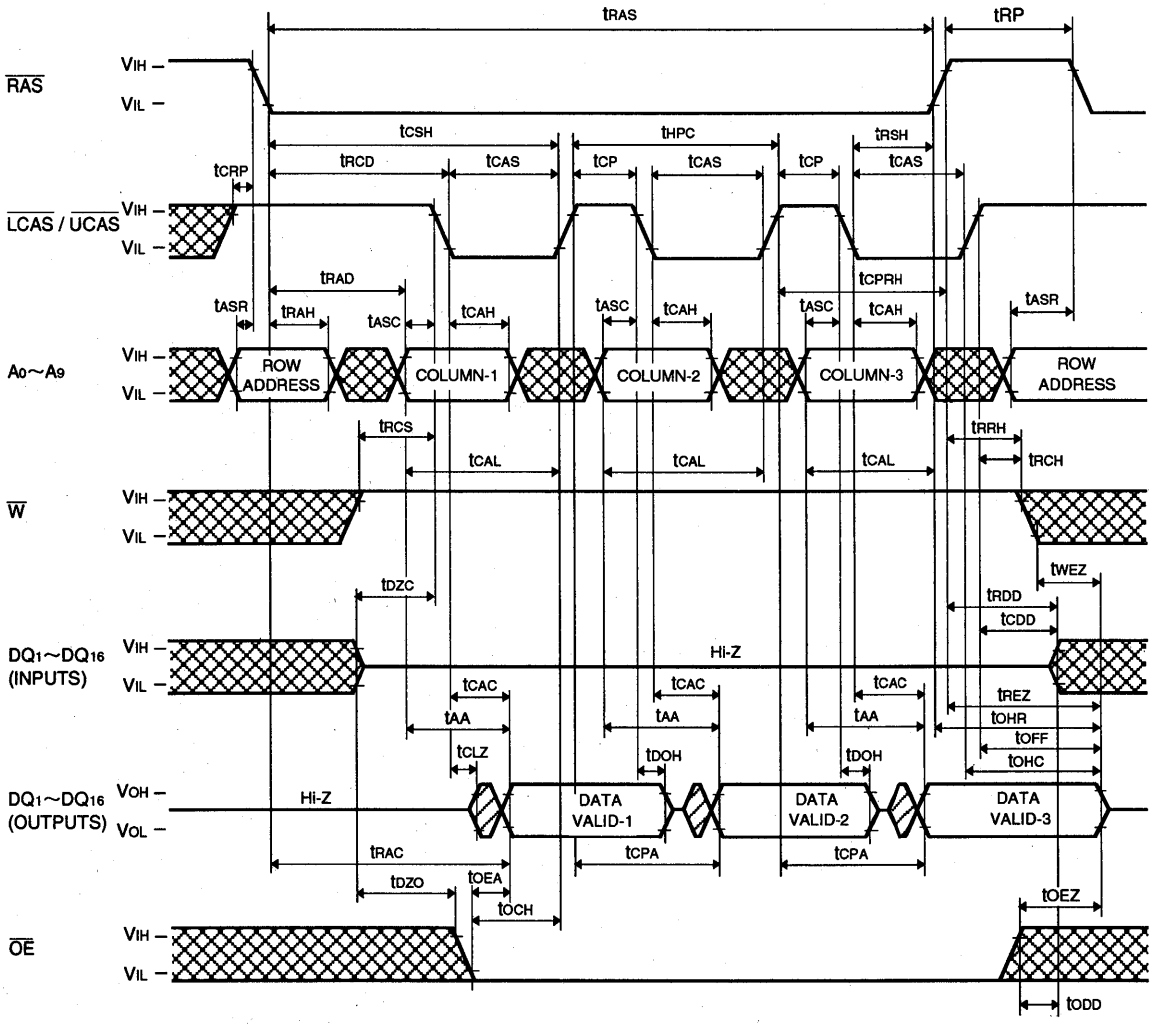
Read-Write, Read-Modify-Write Cycle



Byte Read-Write, Read-Modify-Write Cycle

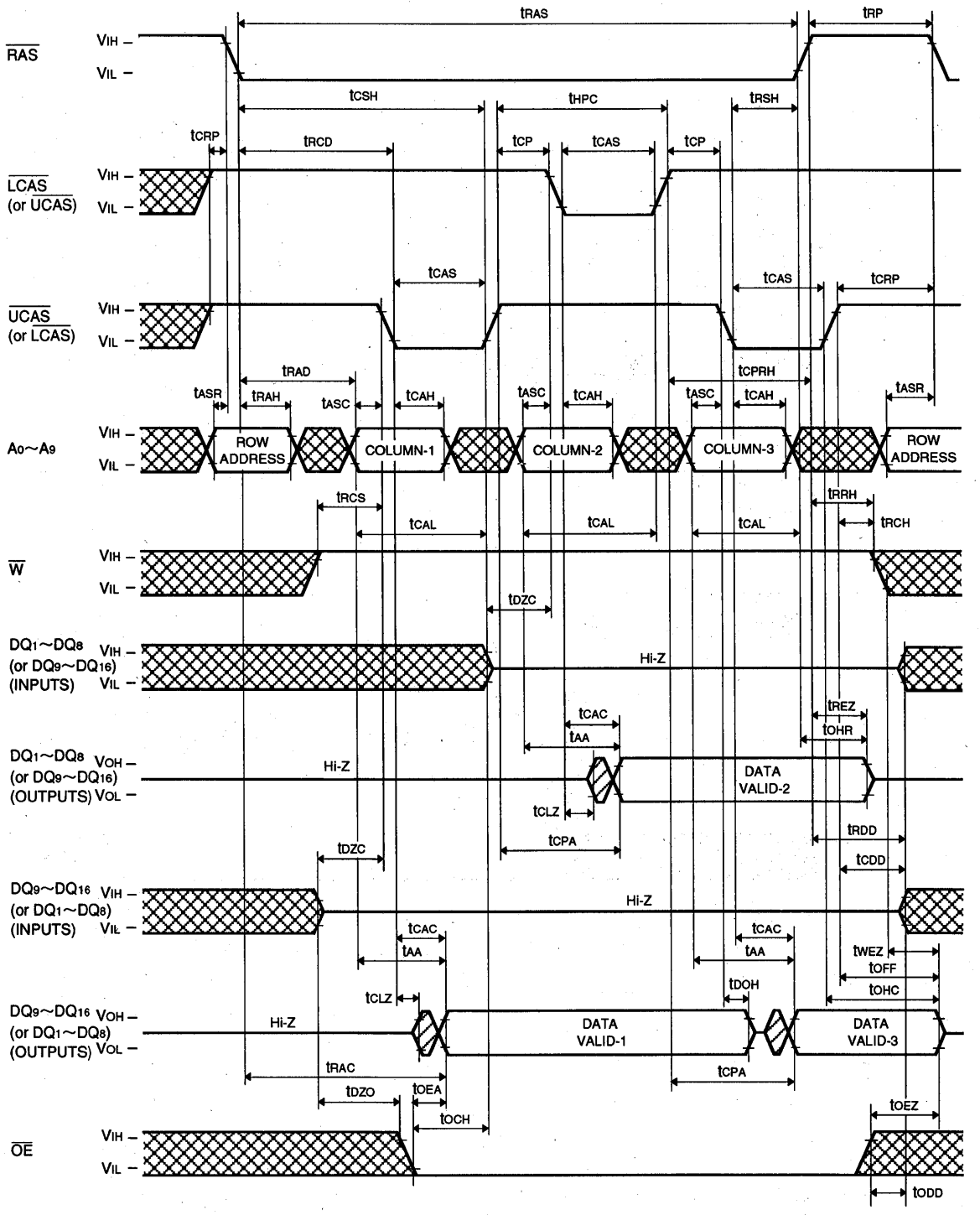


Hyper Page Mode Read Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Read Cycle



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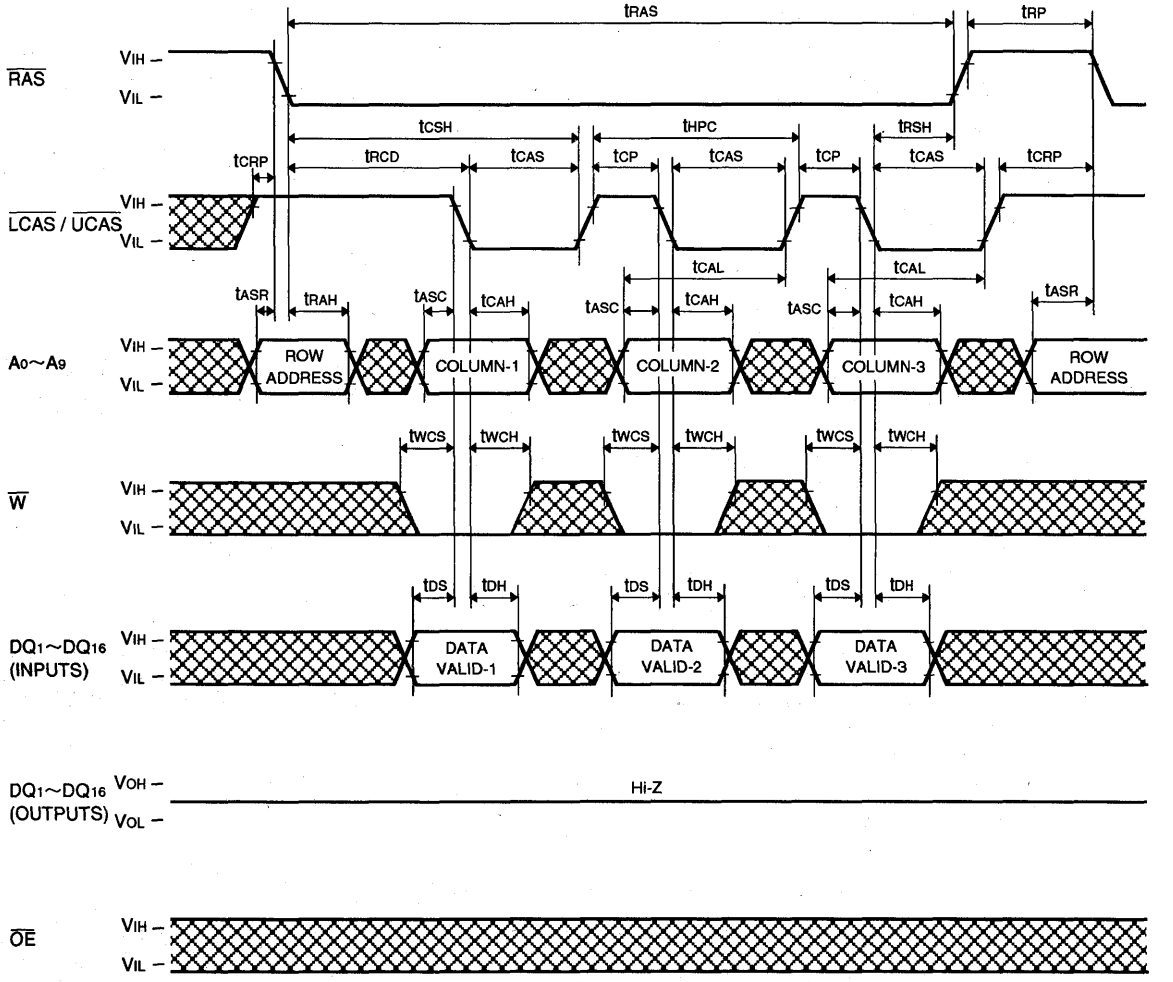
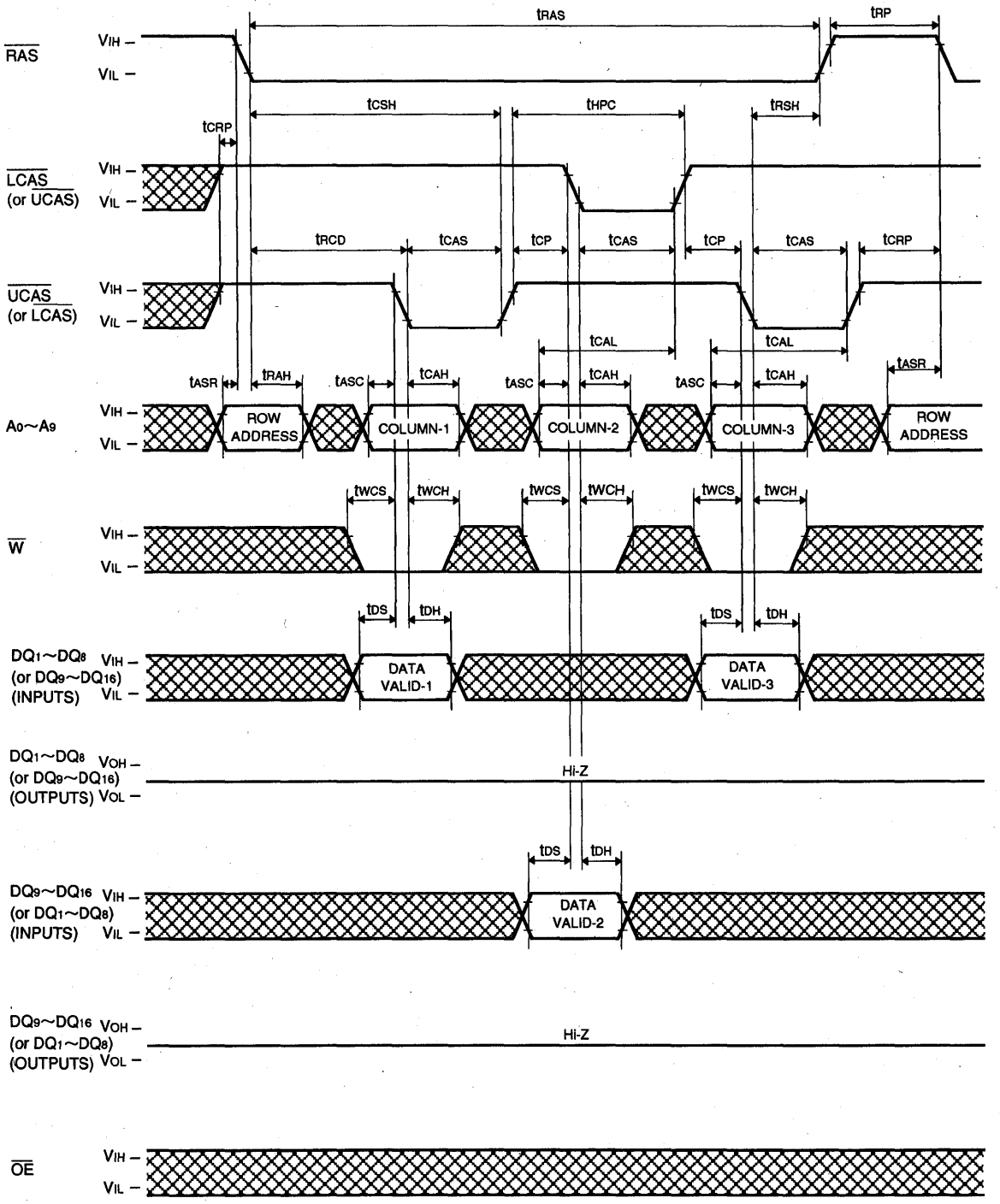
Hyper Page Mode Early Write Cycle



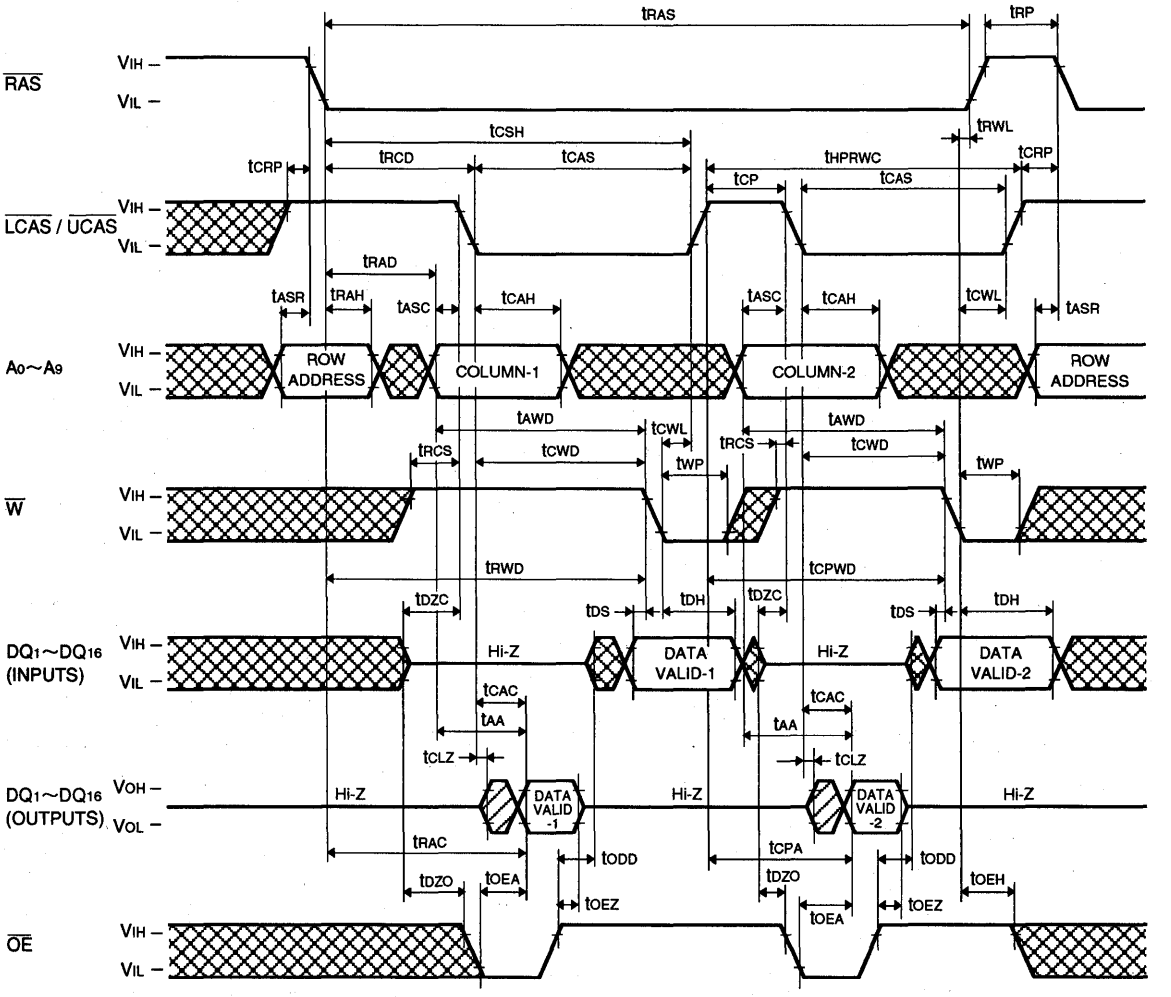
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Early Write Cycle

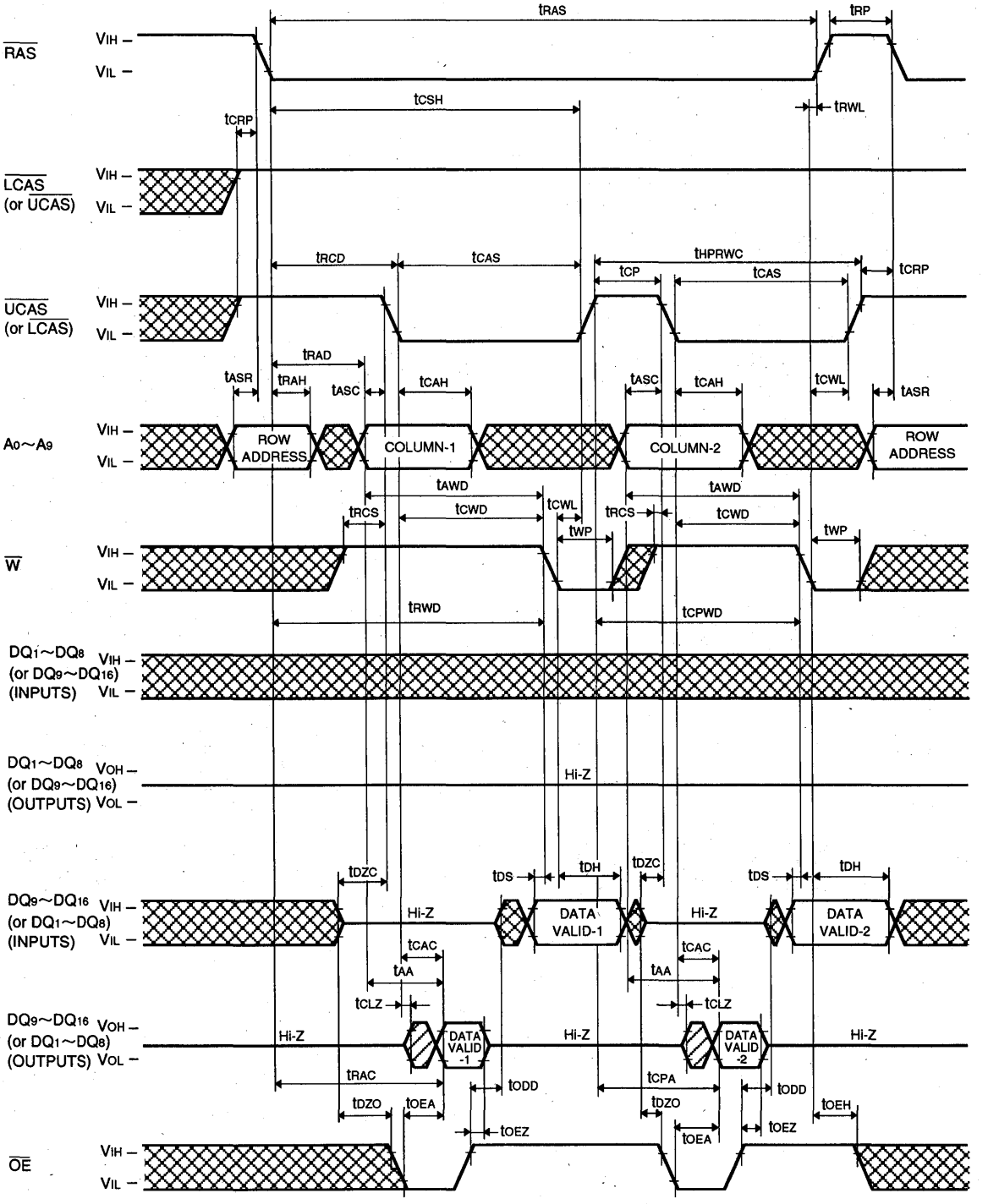


PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

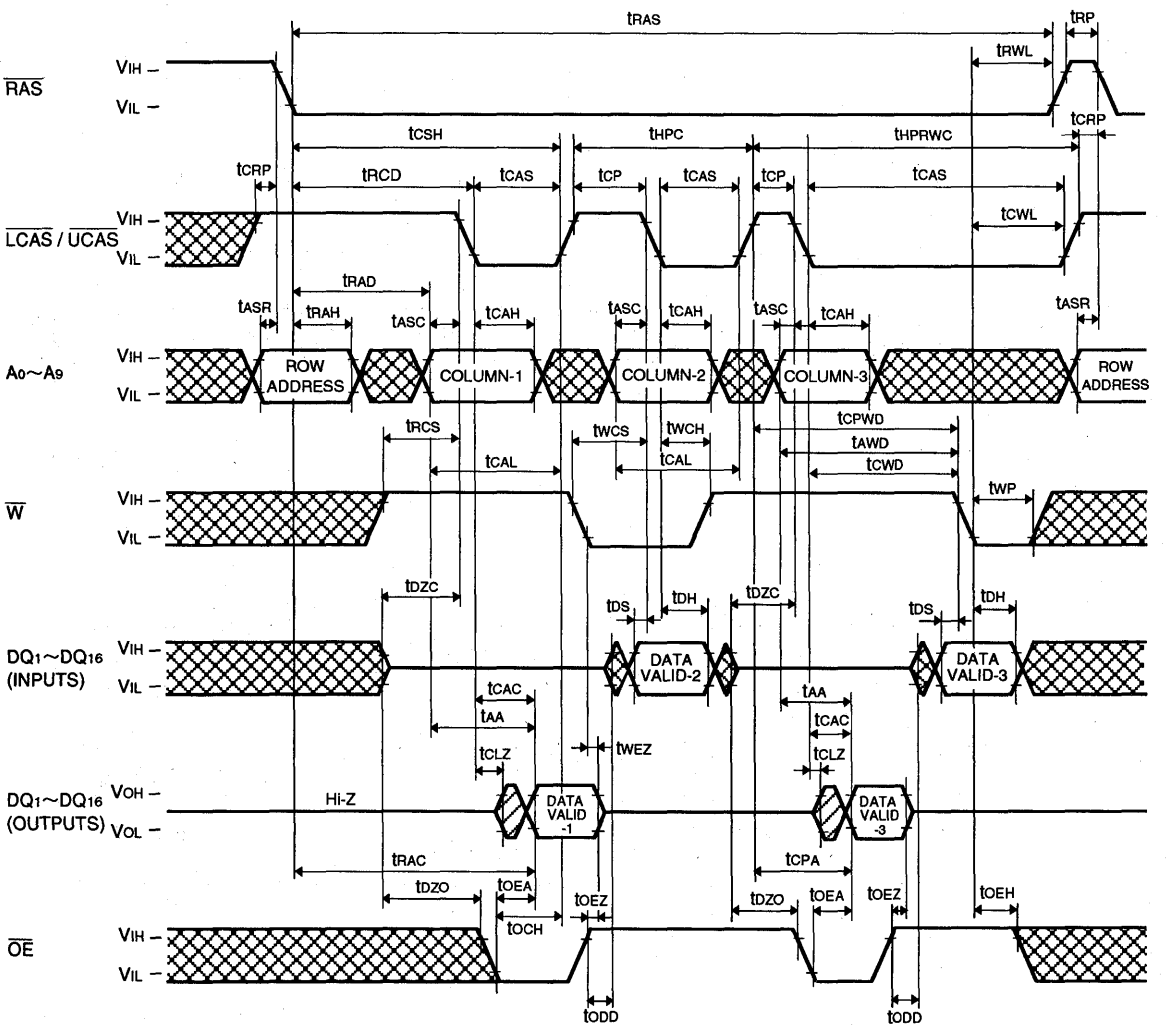
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle

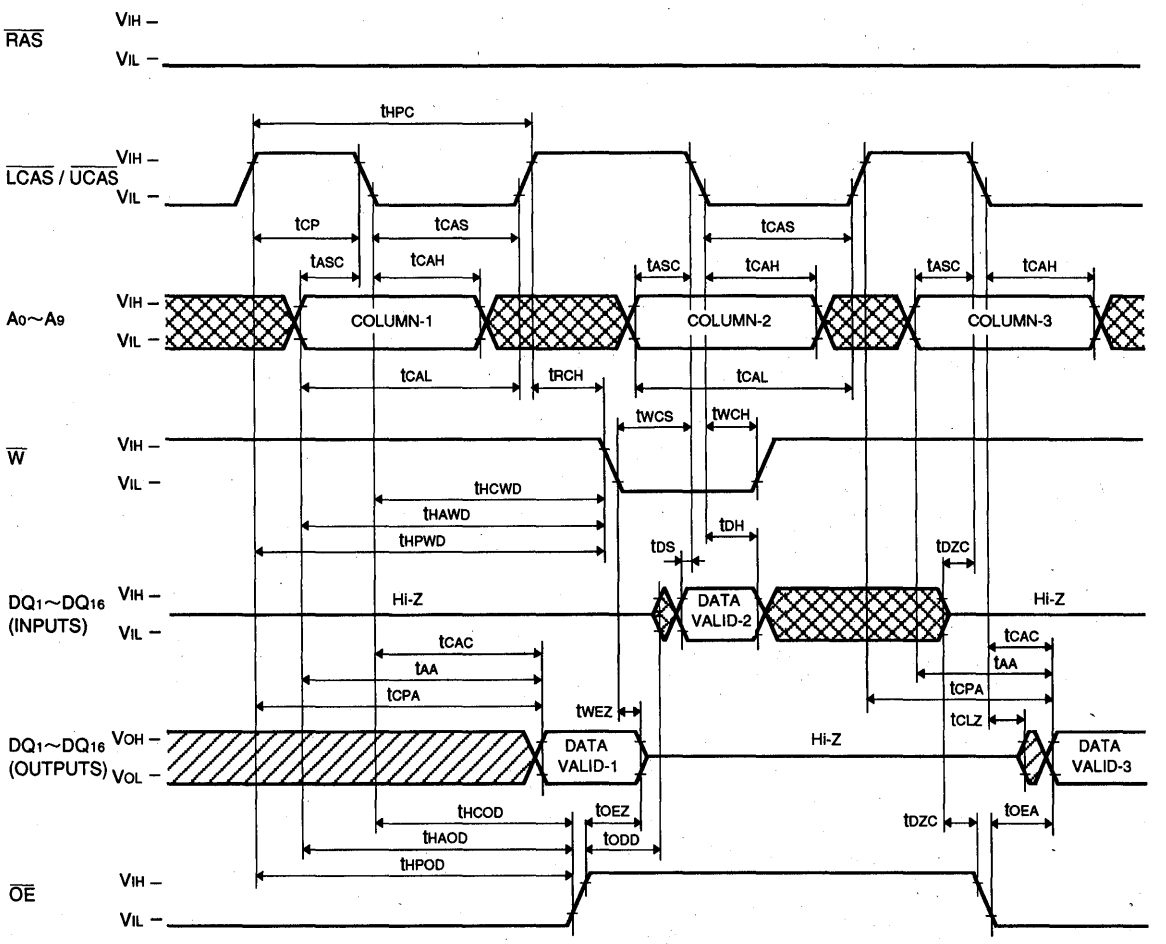


Hyper Page Mode Mix Cycle (1)

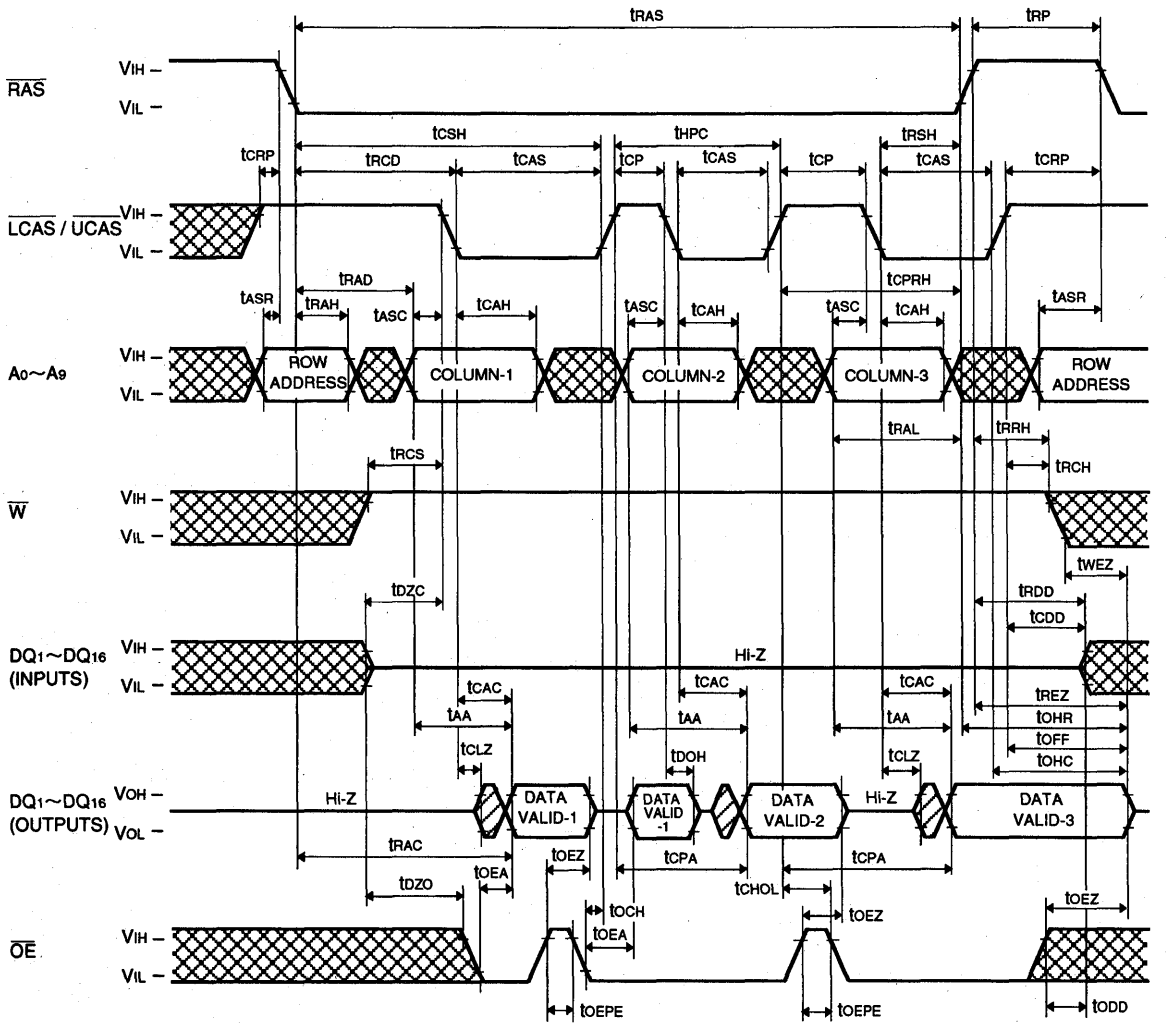


PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (2)

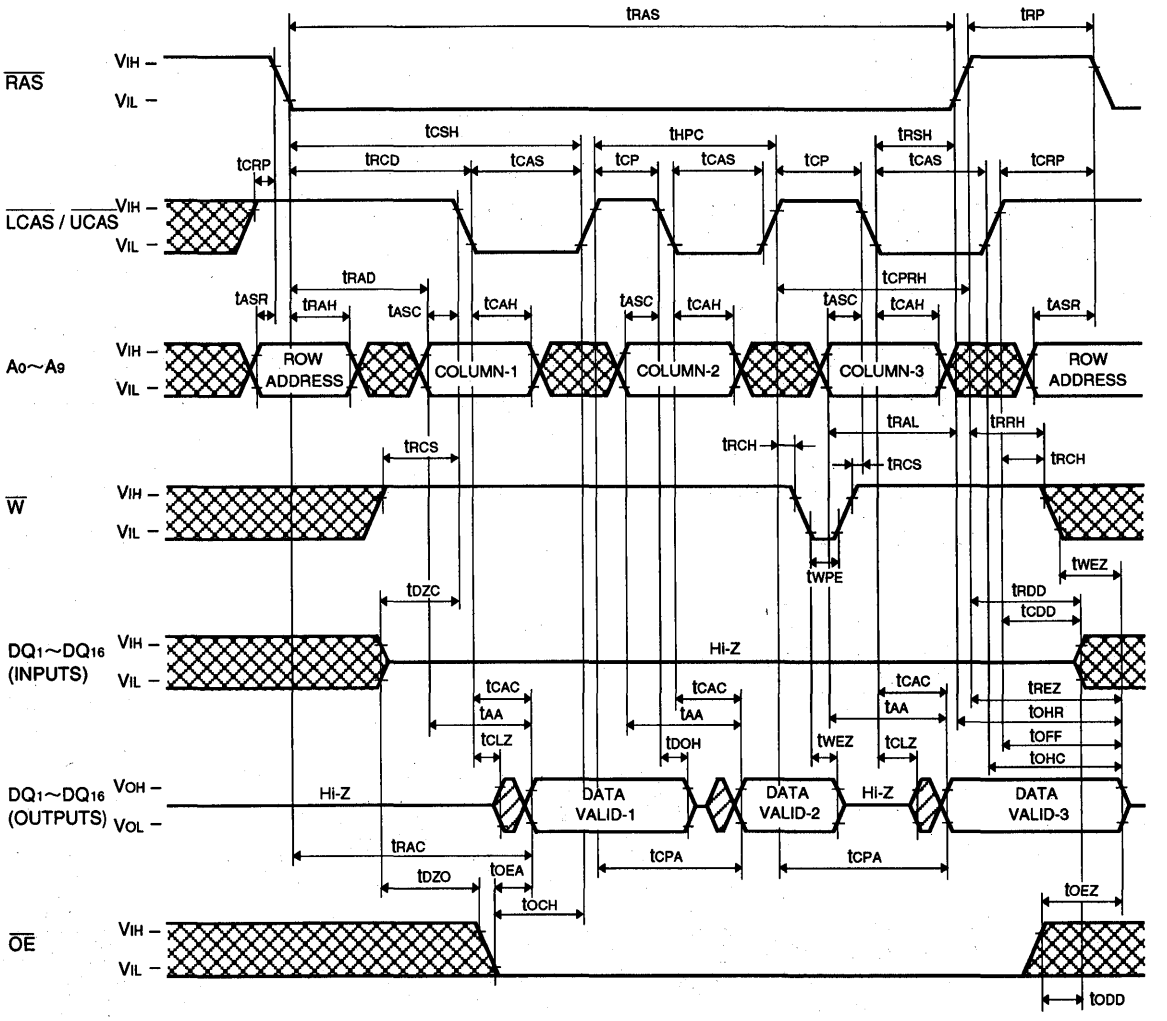


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



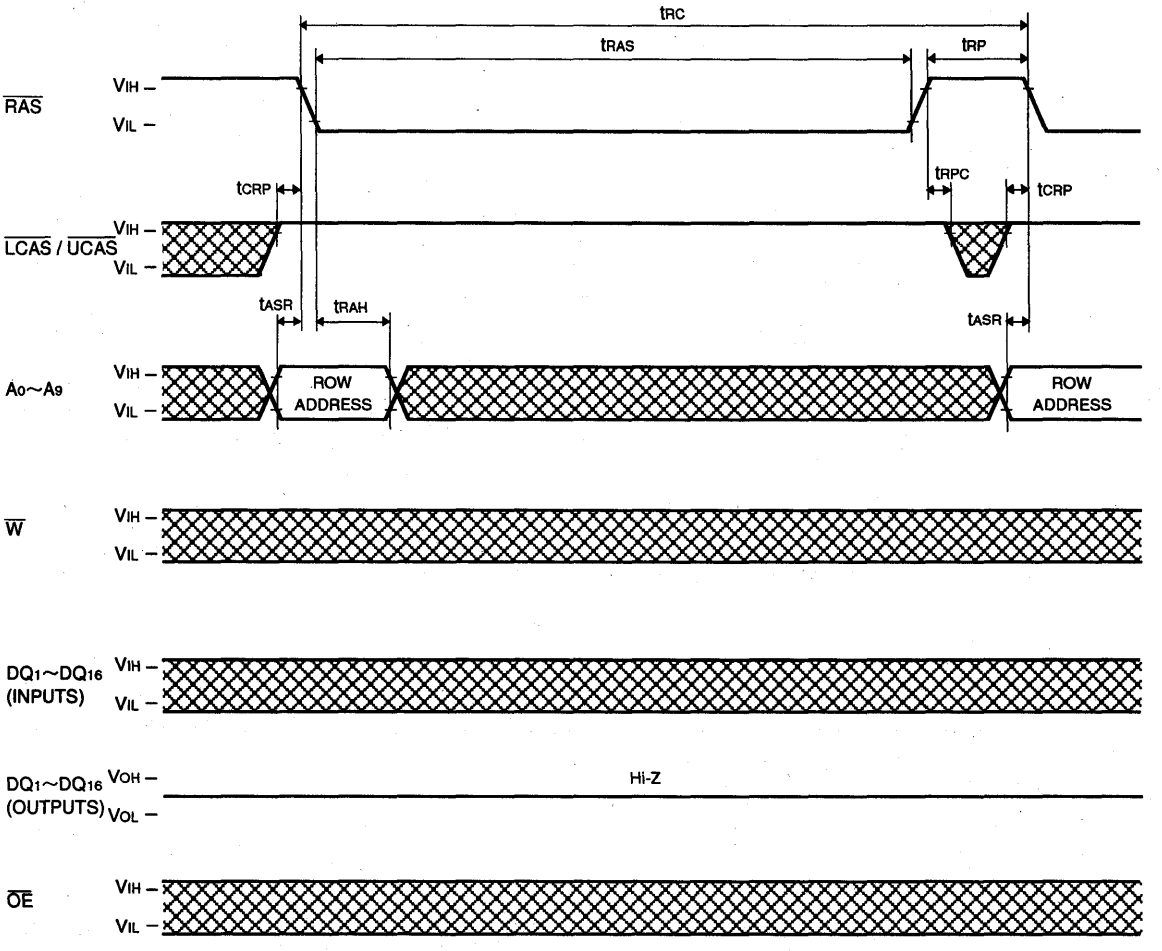
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



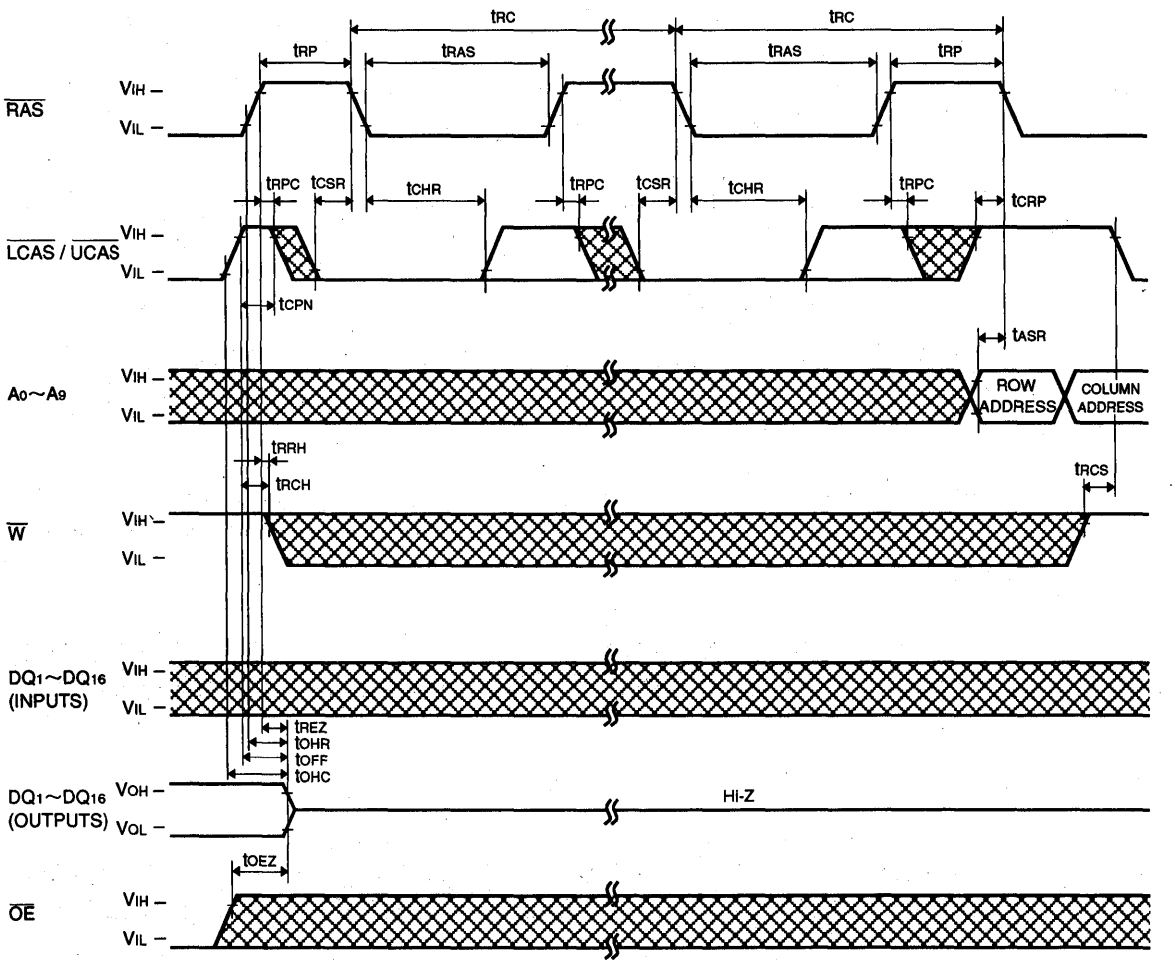
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{\text{RAS}}$-only Refresh Cycle

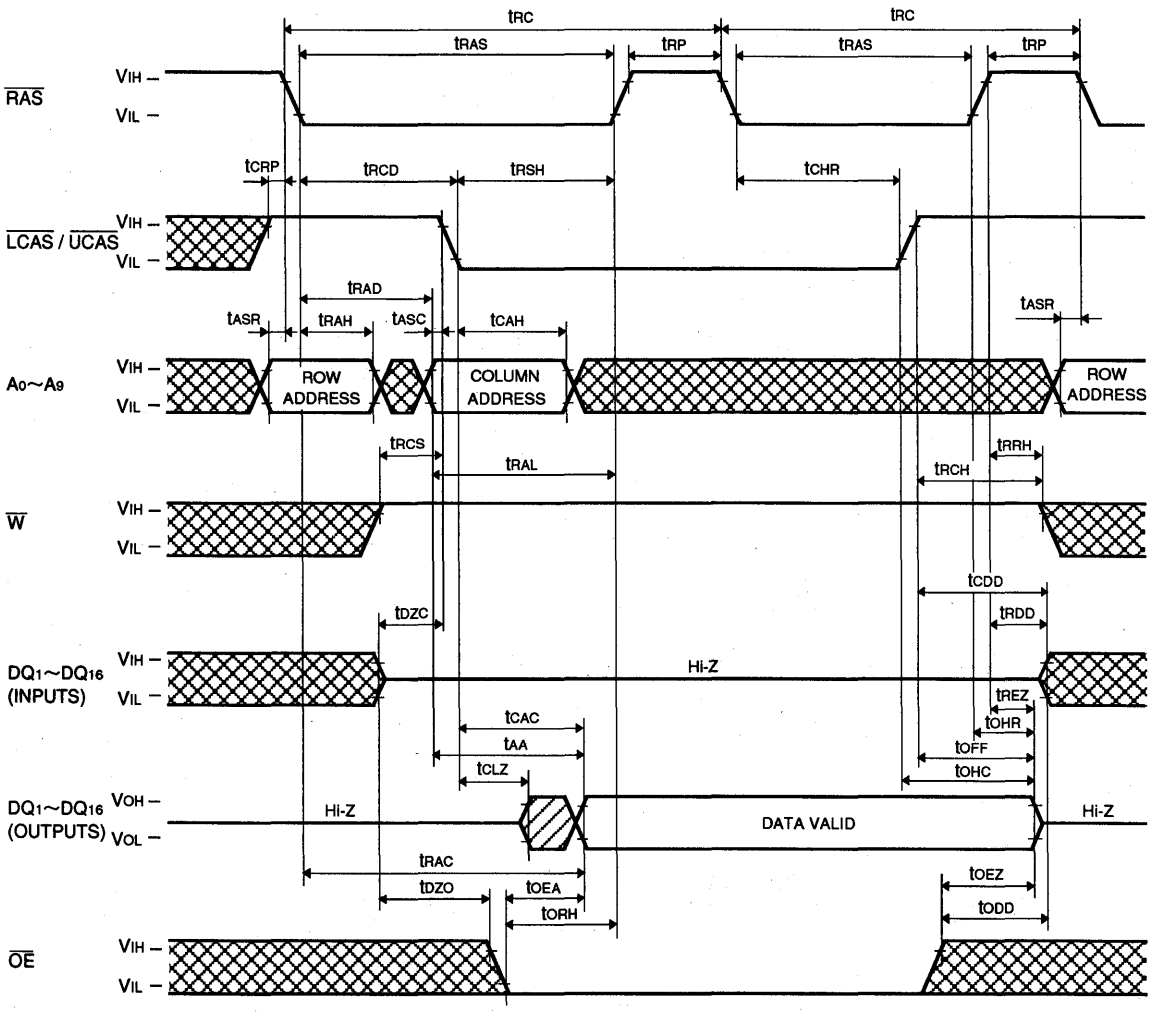


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAS before RAS Refresh Cycle, Extended Refresh Cycle*

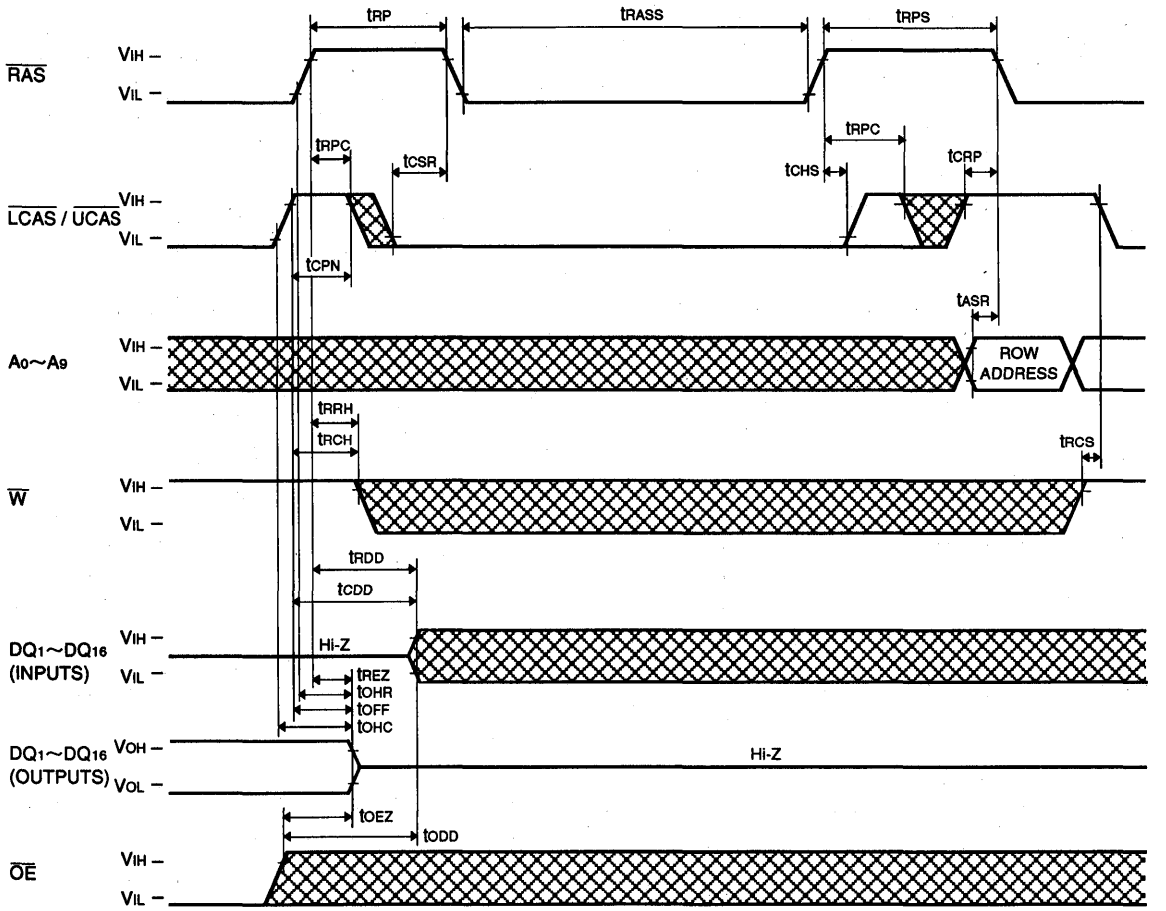


Hidden Refresh Cycle (Read) (Note 30)

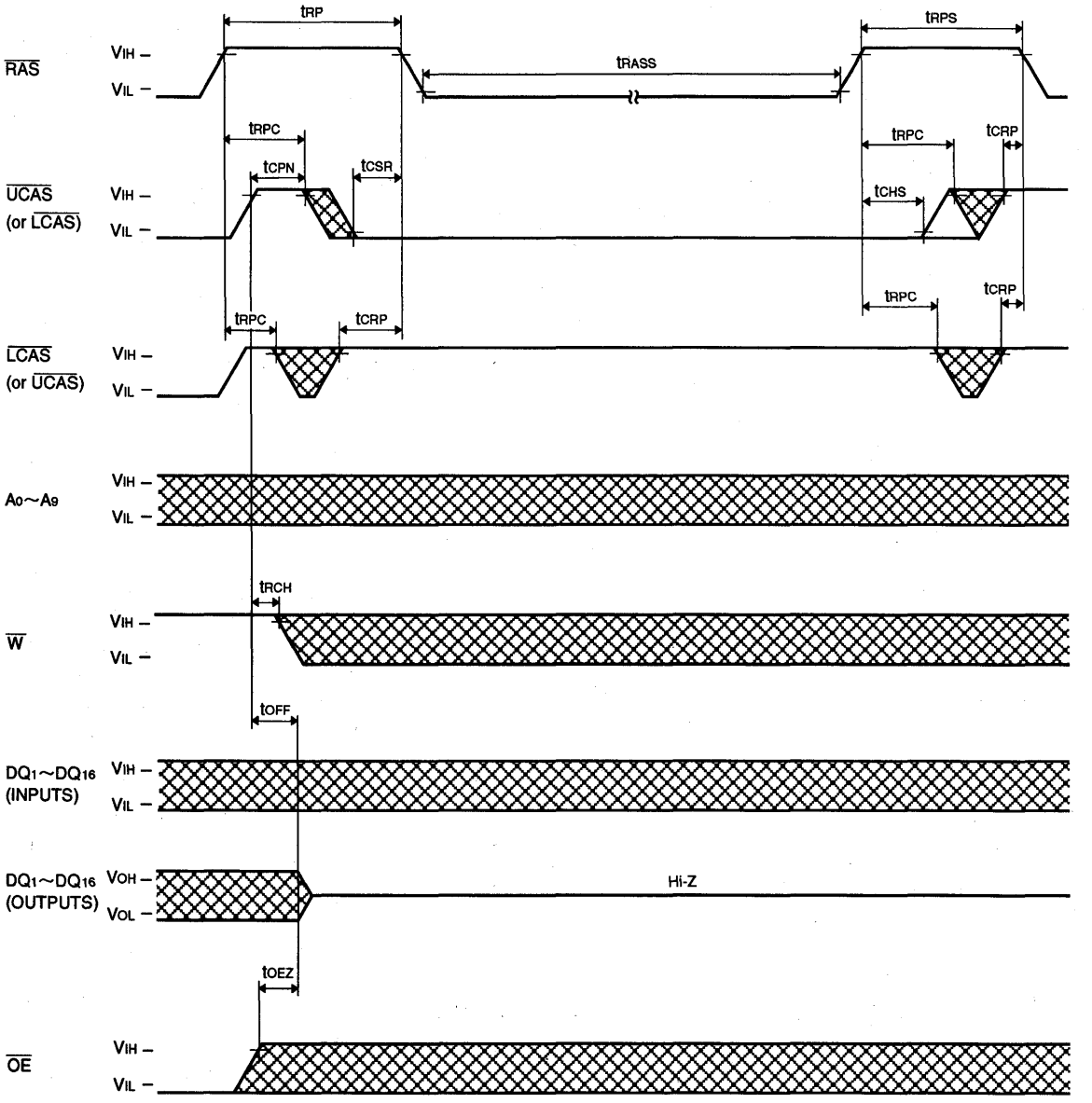


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle *



Upper / (Lower) Self Refresh Cycle*



16M DRAM(3.3V Version)

5

M5M4V16400BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16400BXX-6,-6S	60	15	30	15	110	270
M5M4V16400BXX-7,-7S	70	20	35	20	130	225

XX=J,TP

- Standard 26 pin SOJ,26 pin TSOP
- Single 3.3V ±10%supply
- Low stand-by power dissipation
  - M5M4V16400B ····· 1.8mW (Max)CMOS Input level
  - M5M4V16400B(S) ····· 0.72mW (Max)CMOS Input level
- Low operating power dissipation
  - M5M4V16400Bxx- 6,- 6S ····· 325.0mW (Max)
  - M5M4V16400Bxx- 7,- 7S ····· 270.0mW (Max)

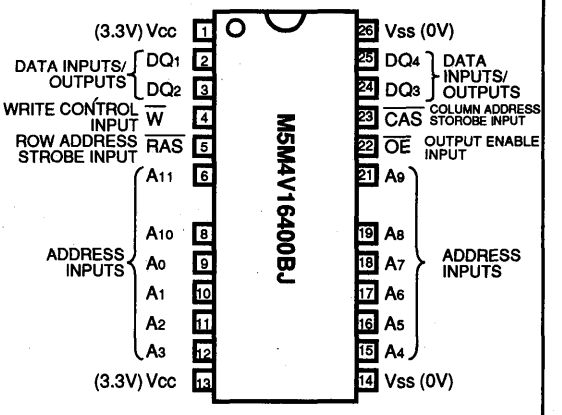
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh and Self refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~ A_{11})
- 4096 refresh cycles every 128ms (A_0 ~ A_{11}) *

  * : Applicable to self refresh version only

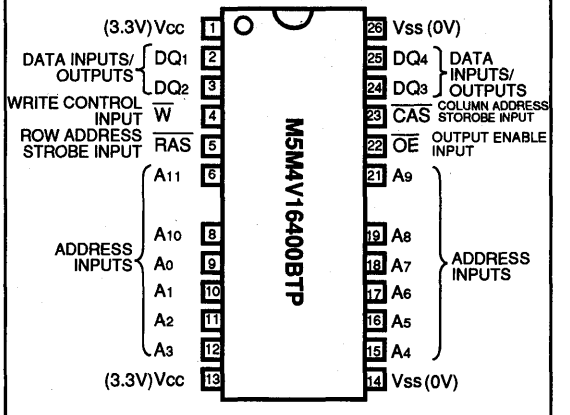
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D - B (300mil SOJ)



Outline 26P3D - E (300mil TSOP)

FUNCTION

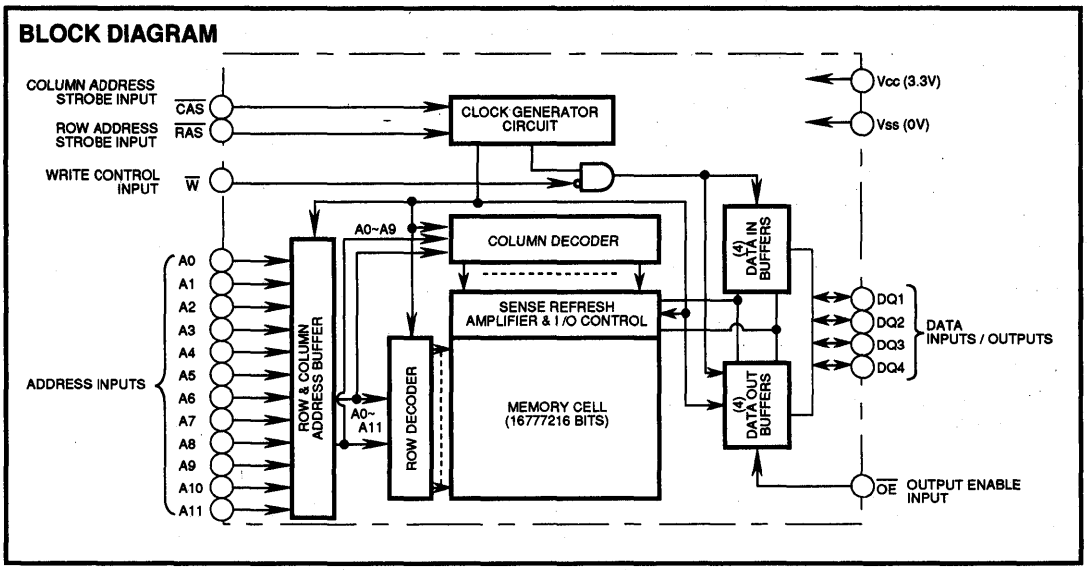
The M5M4V16400BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
VI	Input voltage		-0.5 ~ 4.6	V
Vo	Output voltage		-0.5 ~ 4.6	V
Io	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.0		Vcc+0.3	V
VIL	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≦VOUT≦3.6V	-10		10	μA
II	Input current		0V≦VIN≦3.6V, Other inputs pins=0V	-10		10	μA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4)	M5M4V16400B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open			90	mA
		M5M4V16400B-7,-7S				75	
ICC2	Supply current from Vcc , stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =VIH, output open			2	mA
		M5M4V16400B	$\overline{RAS}$= $\overline{CAS}$=$\overline{OE}$=$\overline{W}$=A0~A11≧Vcc -0.2V output open			0.5	
		M5M4V16400B(S)				0.2	
ICC3 (AV)	Average supply current from Vcc refreshing (Note 3)	M5M4V16400B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= VIH tRC=min. output open			90	mA
		M5M4V16400B-7,-7S				75	
ICC4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M4V16400B-6,-6S	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			70	mA
		M5M4V16400B-7,-7S				60	
ICC6(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16400B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			90	mA
		M5M4V16400B-7,-7S				75	
ICC8(AV)	Average supply current from Vcc Extended refresh (Note 5)	M5M4V16400B(S)	$\overline{RAS}$ cycling and $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A0-A11≦0.2V output open, tRC=32μs,tRAS=tRASmin~1μs			0.4	mA
ICC9 (AV)	Average supply current from Vcc Self - Refresh cycle (Note 5)	M5M4V16400B(S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V,output open Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A0~A11≦0.2V			0.2	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0～70°C, Vcc=3..3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0～70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits				Unit
			M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		60		70	ns
t_{AA}	Column address access time	(Note 6,9)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	15	ns

Note 5: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to V_{OH}=2.4V (I_{OH}=-2mA) / V_{OL}=2mA(I_{OL}=2mA) loads and 100pF. The reference level for measuring of output signals are V_{OH}=2.0V and V_{OL}=0.8V .

7: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

8: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

10: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

11: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits				Unit
			M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			64		64	ms
t_{REF}	Refresh cycle time *			128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note18)	15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note18)	15		15		ns
t_T	Transition time	(Note19)	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T=5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.

15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
		Min	Max	Min	Max	
tRC	Read cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note21)	155		180		ns
tRAS	$\overline{RAS}$ low pulse width	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note22)	40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note22)	85		95		ns
tAWD	Delay time, address to $\overline{W}$ low (Note22)	55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits				Unit
			M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note24)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note25)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note22)	60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

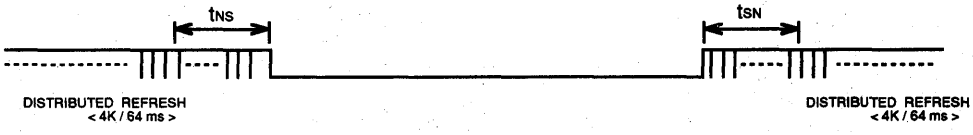
Self Refresh Cycle

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6S		M5M4V16400B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

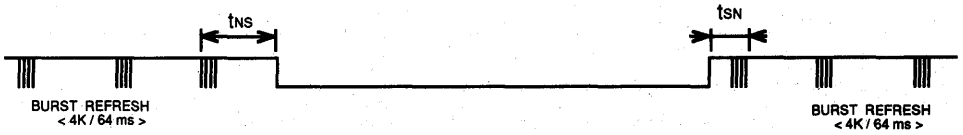
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leqq 64$ ms and $t_{SN} \leqq 64$ ms.



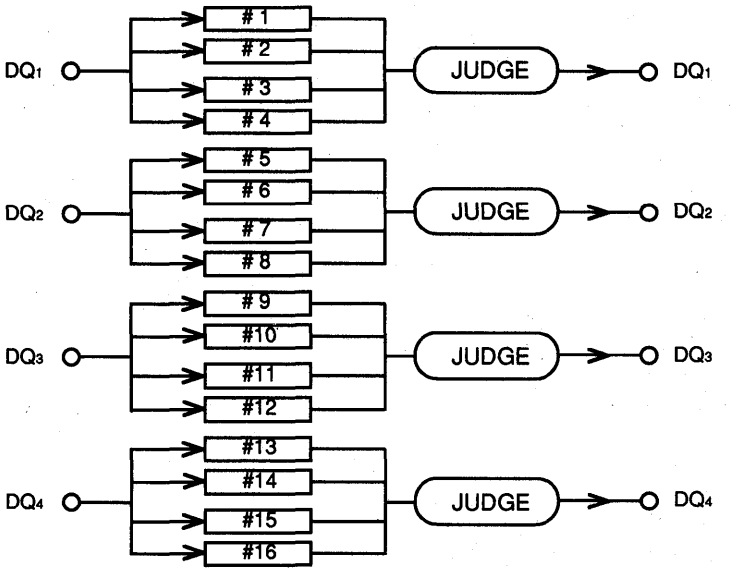
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} + t_{SN} \leqq 64$ ms.



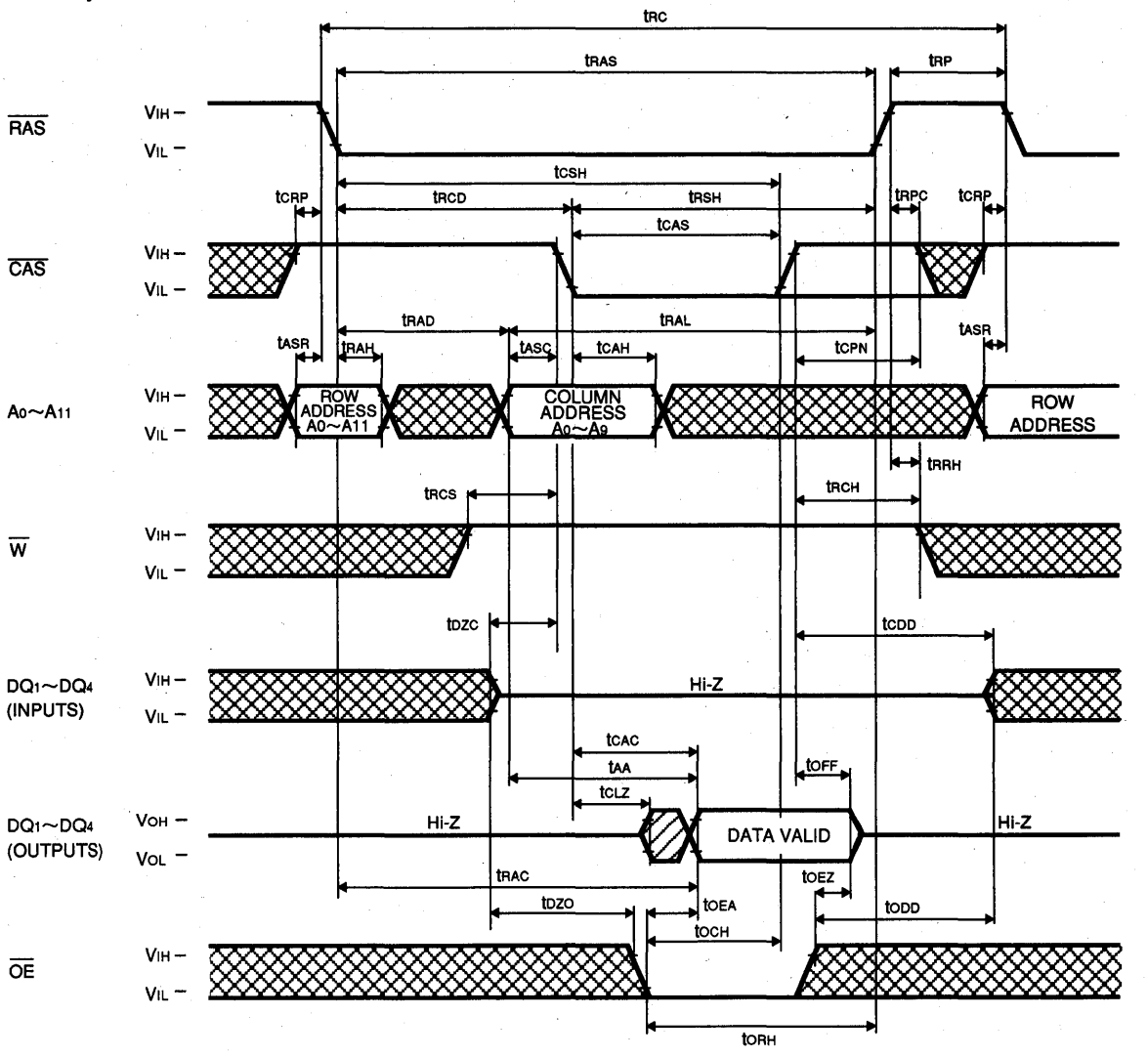
TEST Mode SET Cycle

Symbol	Parameter	Limits				Unit
		M5M4V16400B-6,-6S		M5M4V16400B-7,-7S		
		Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		15		ns



Timing Diagrams (Note 27)

Read Cycle

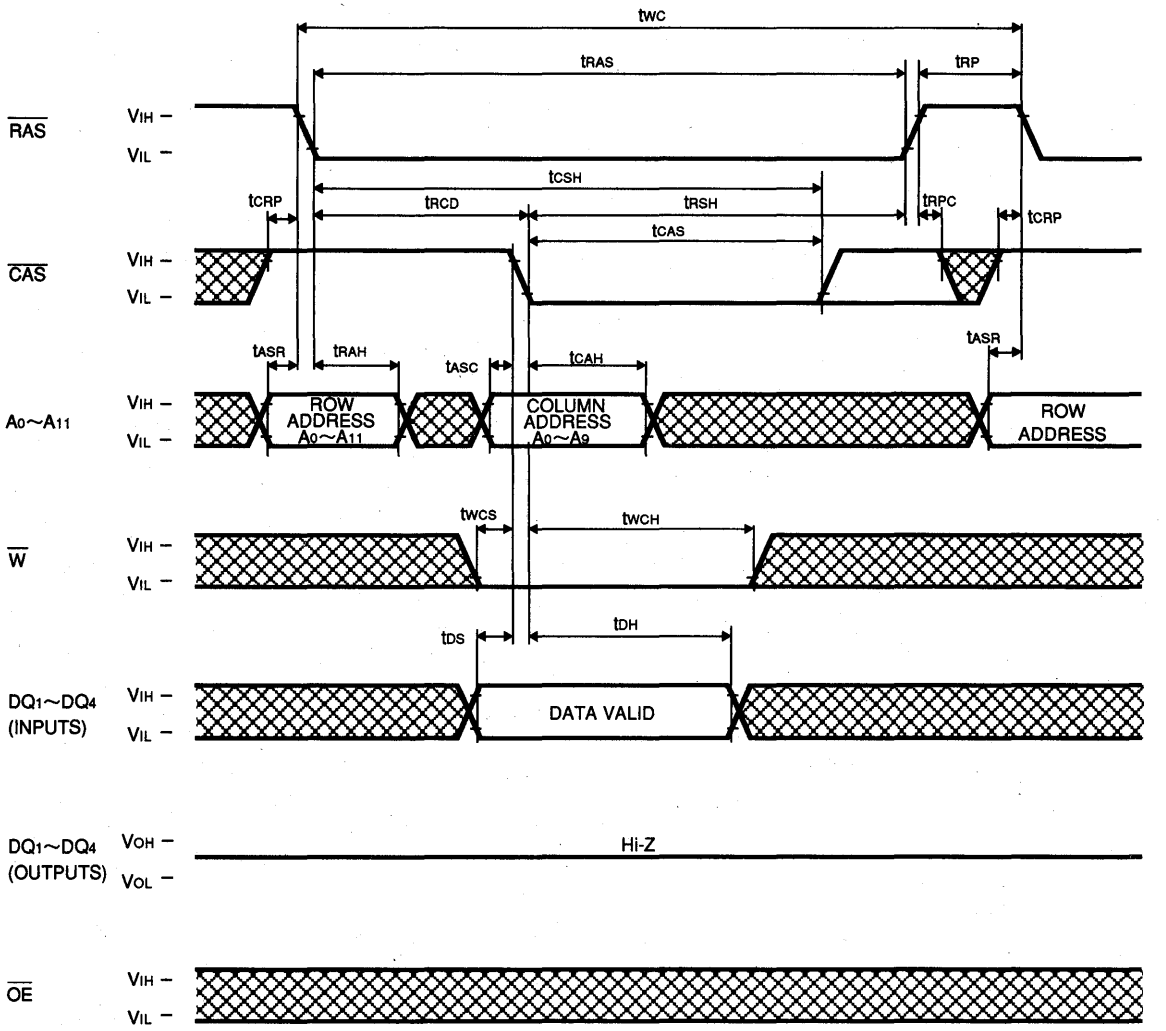


Note 27

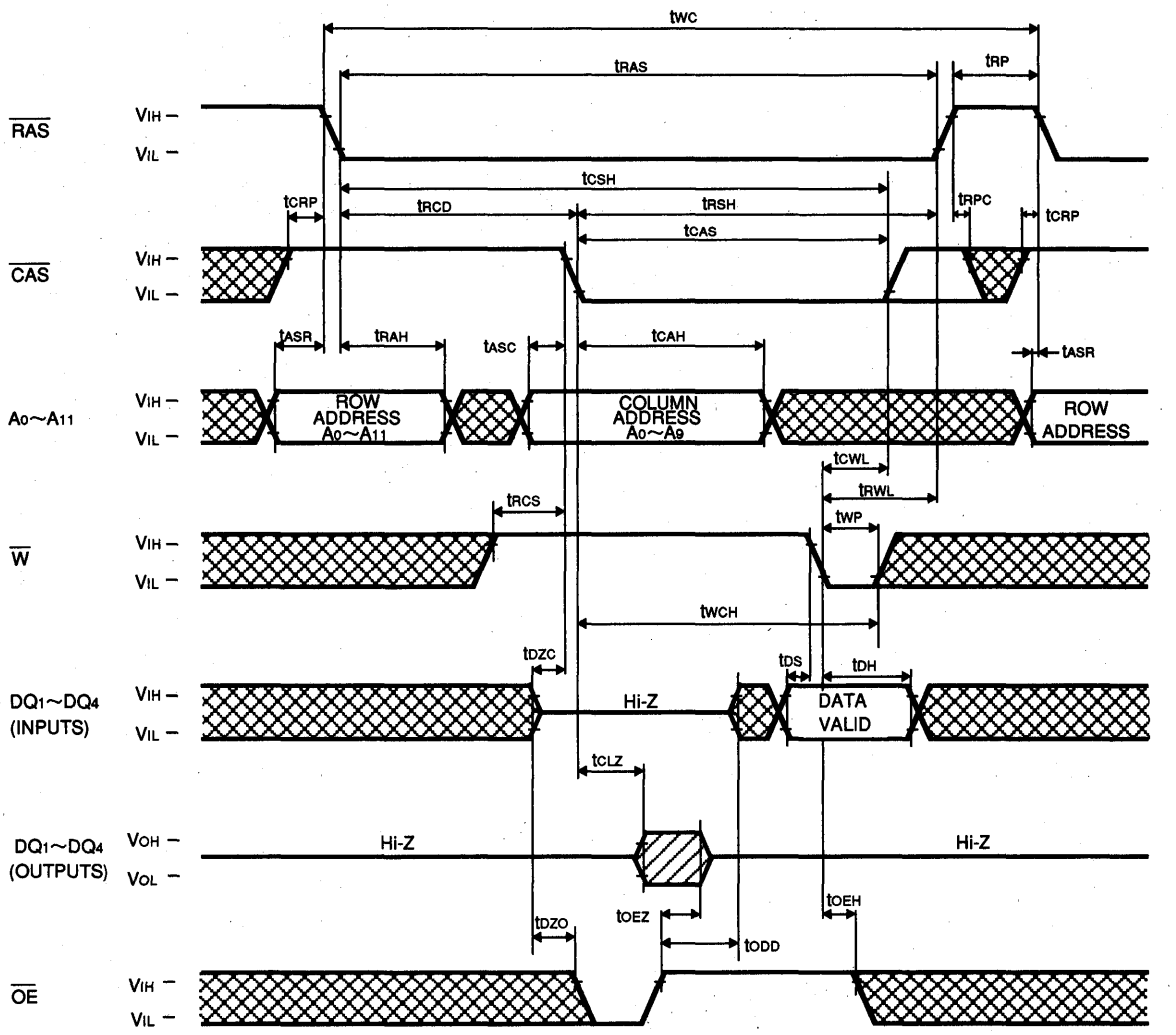
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

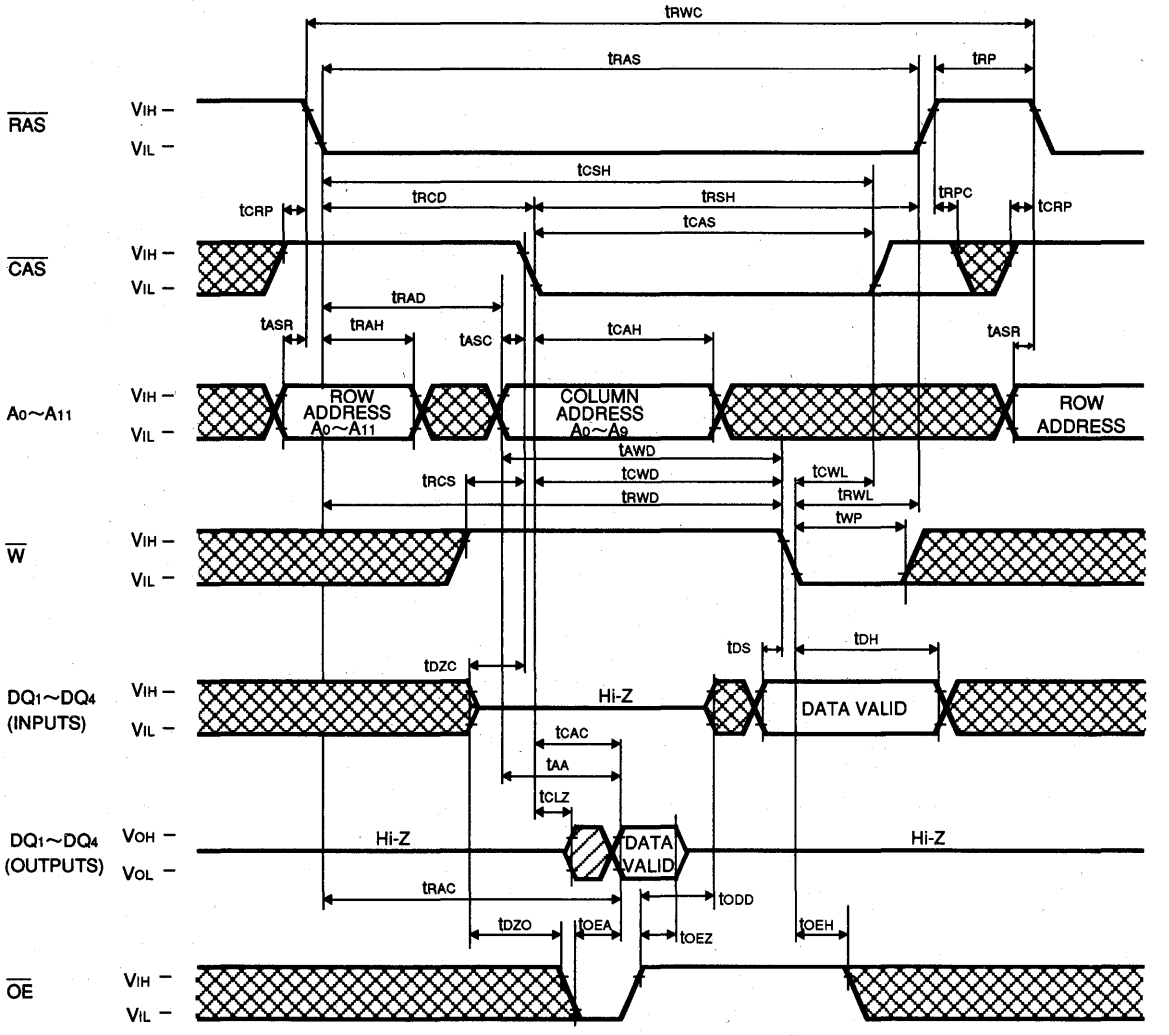
Write Cycle (Early write)



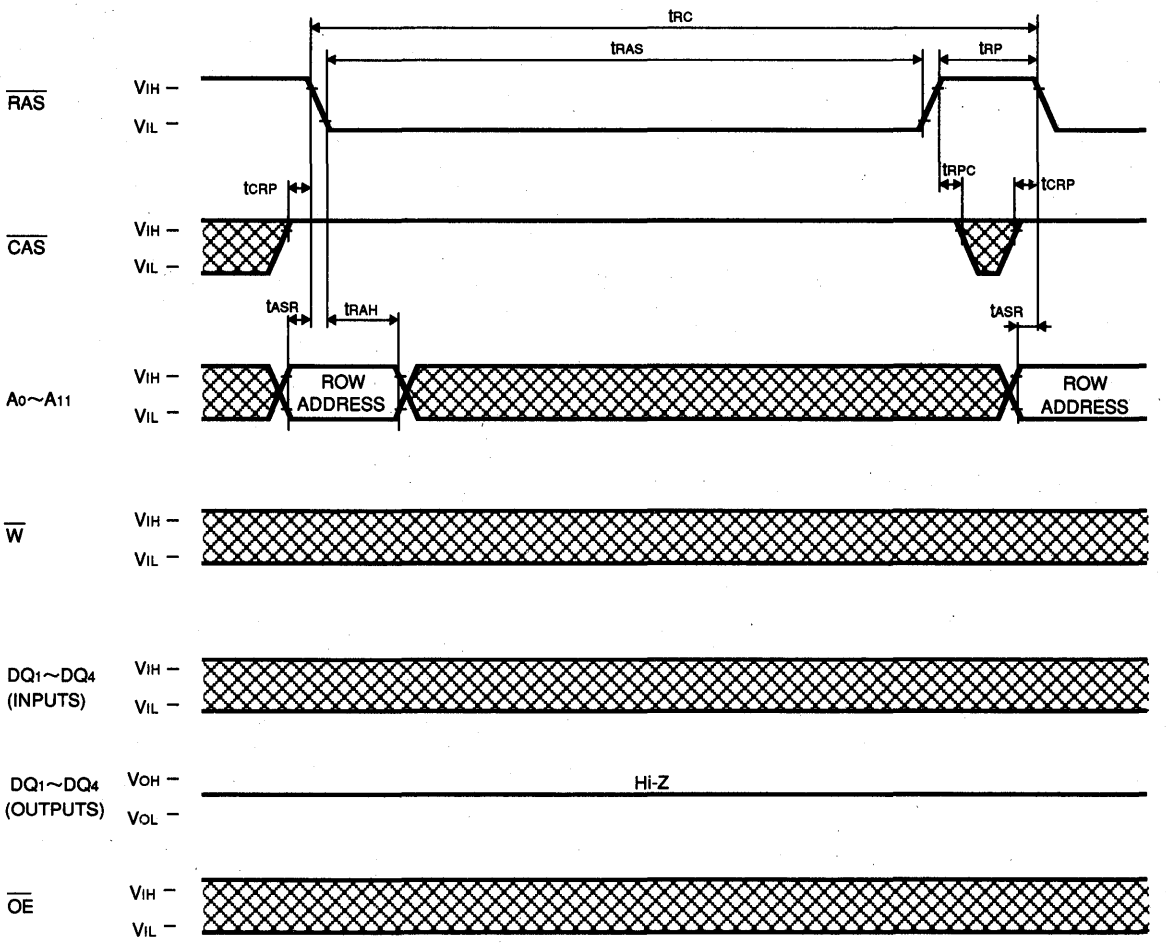
Write Cycle (Delayed write)



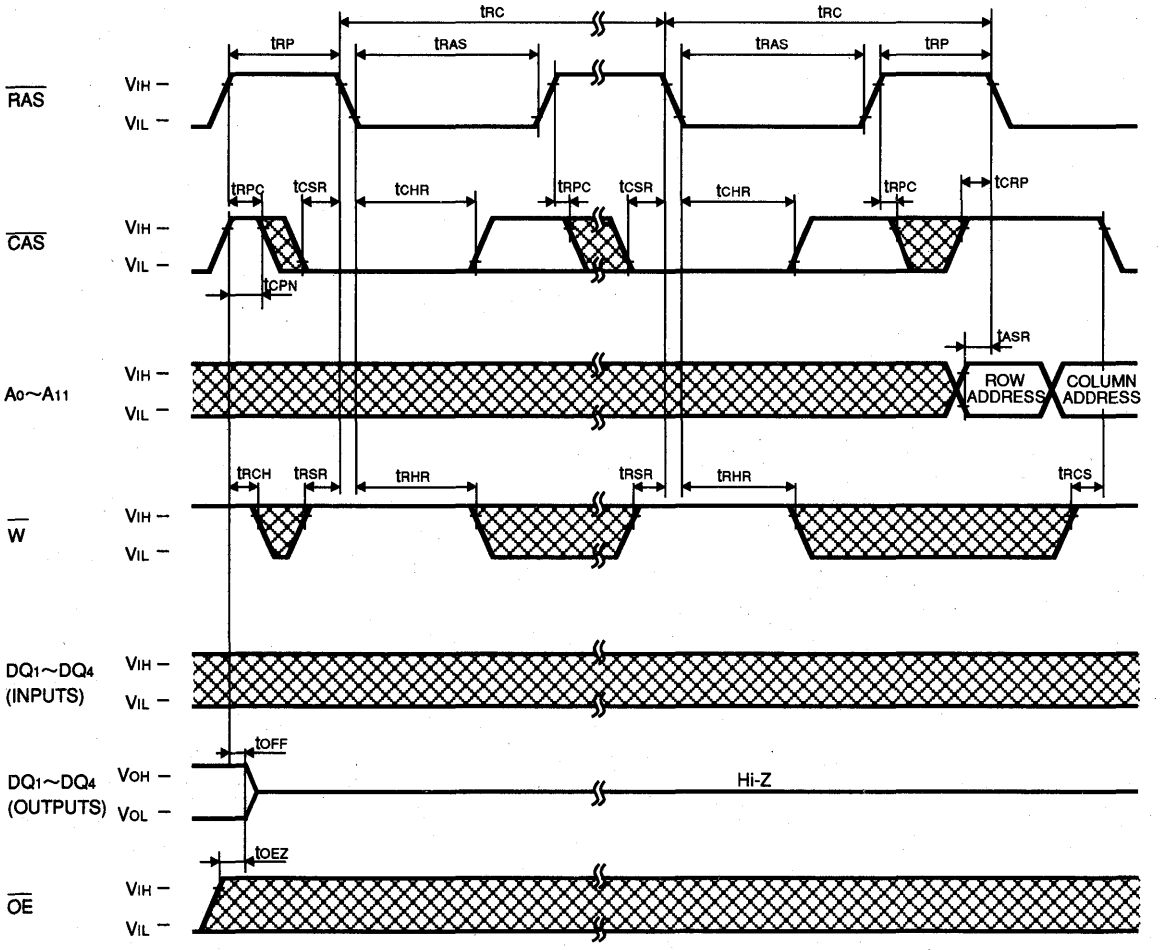
Read-Write, Read-Modify-Write Cycle



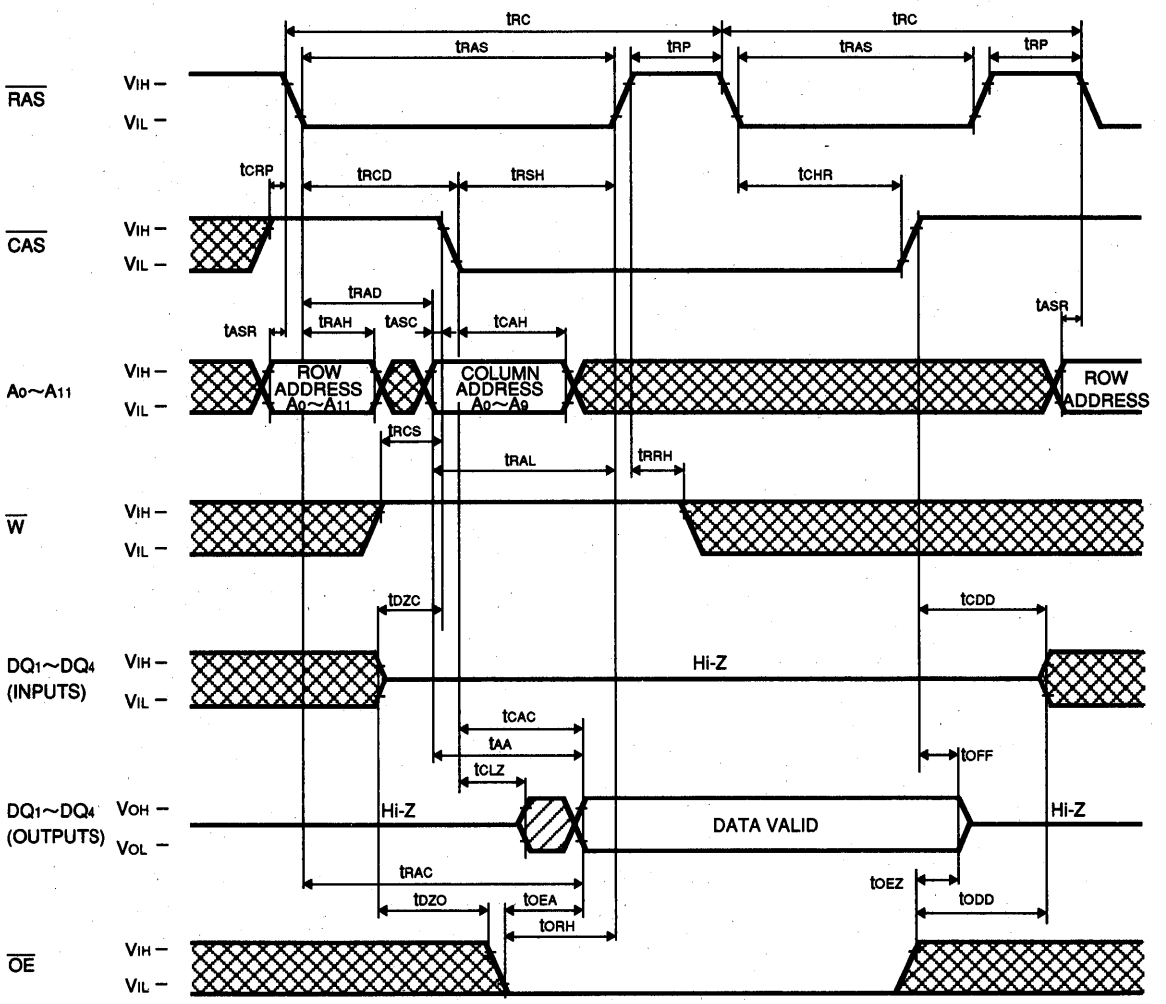
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

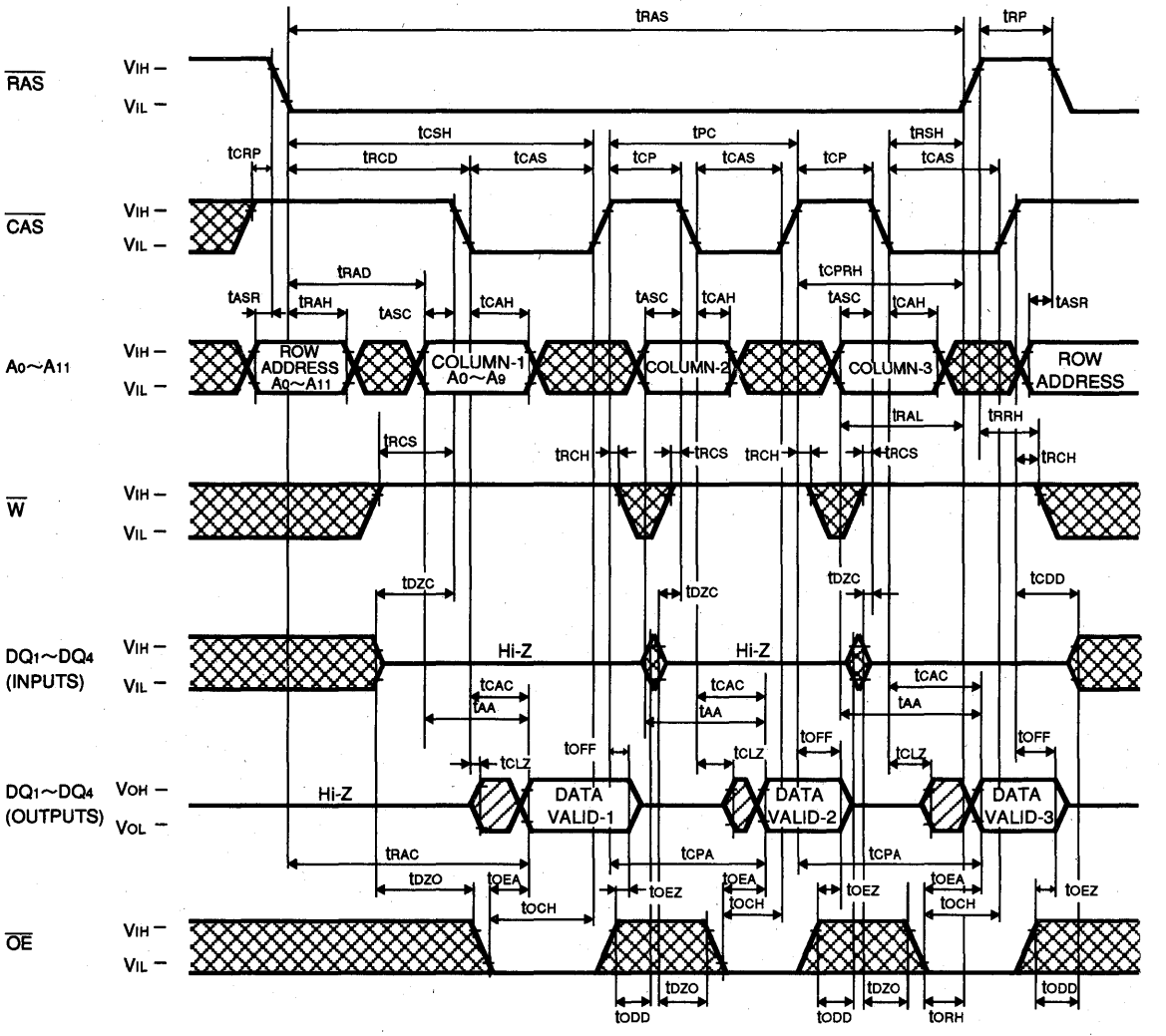


Hidden Refresh Cycle (Read) (Note 28)

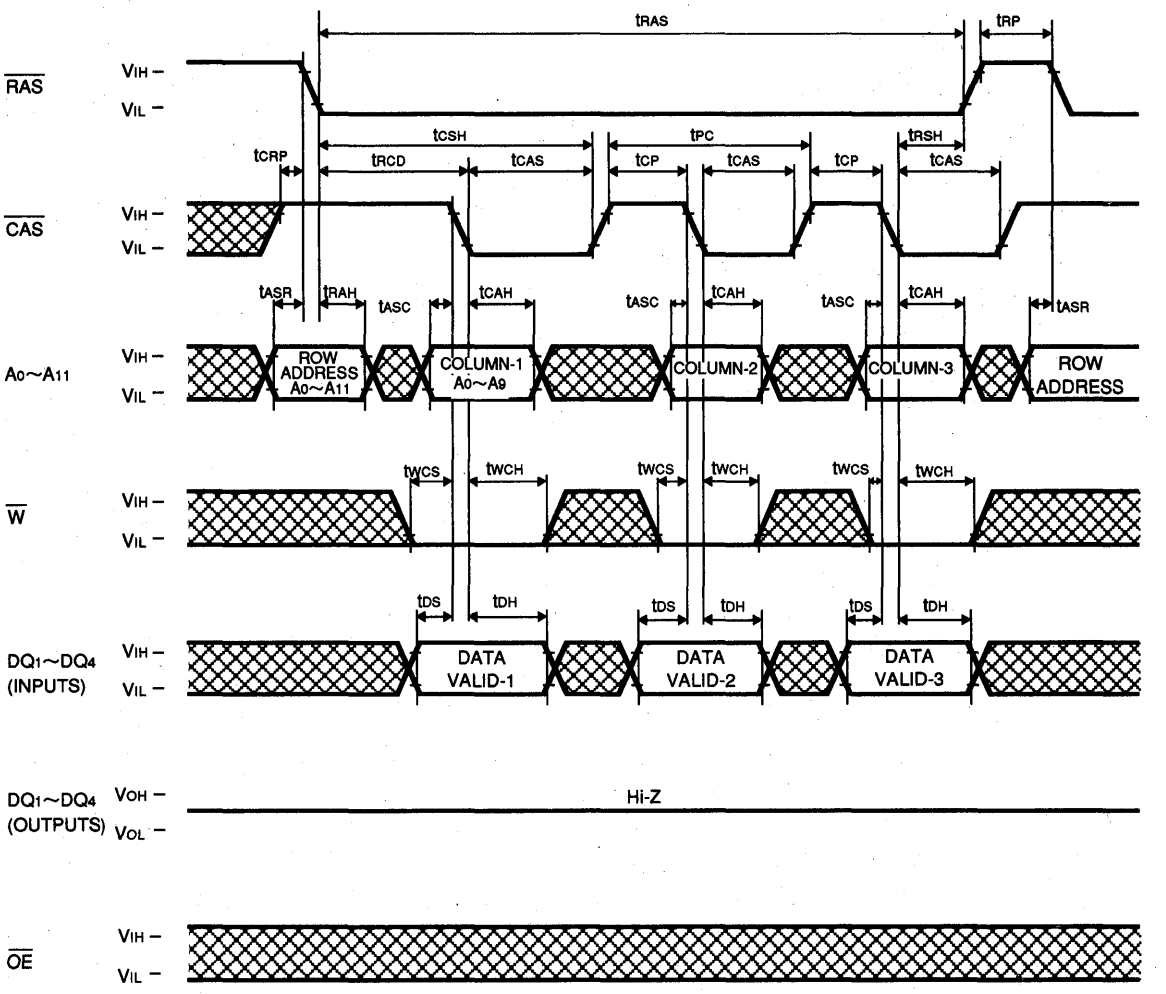


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

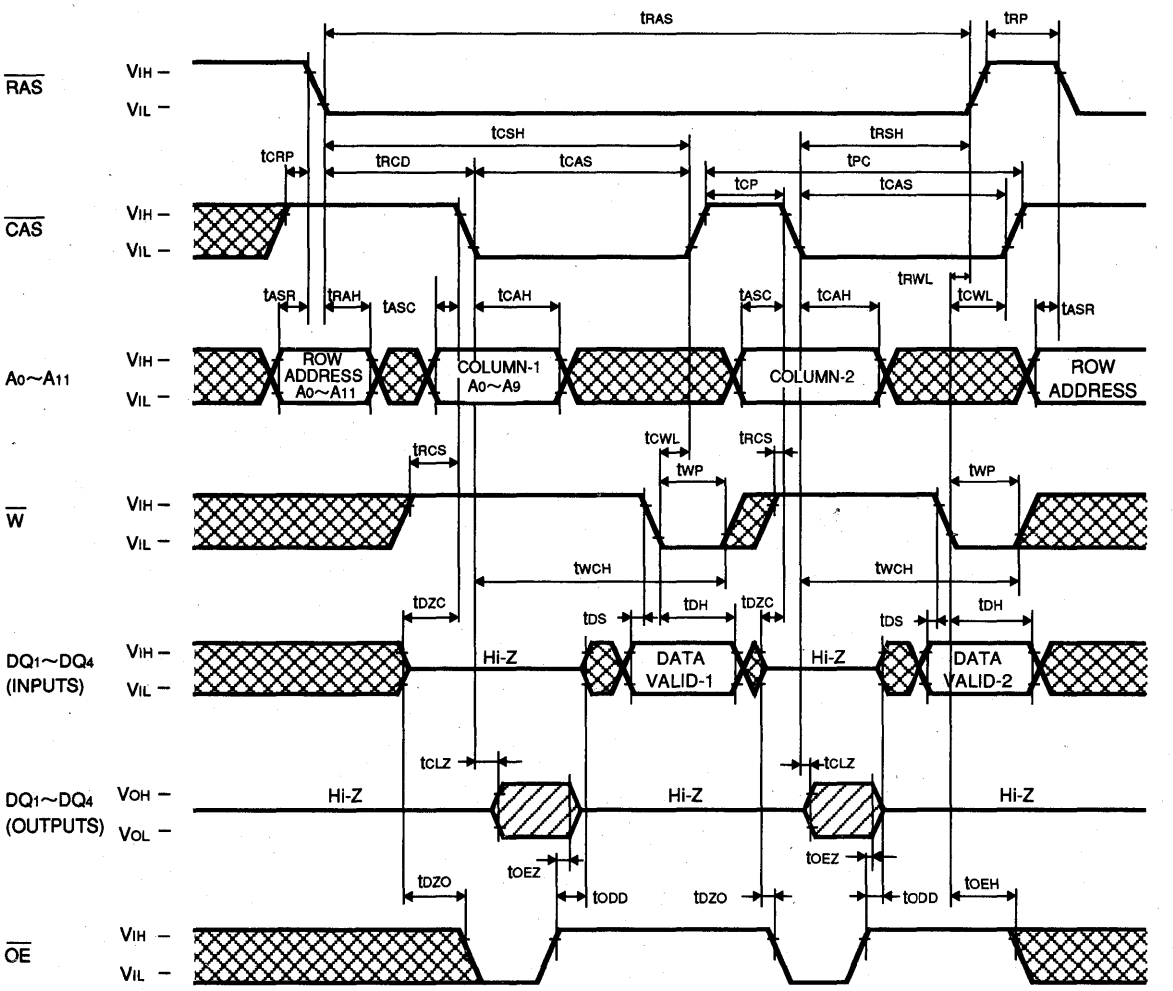
Fast Page Mode Read Cycle



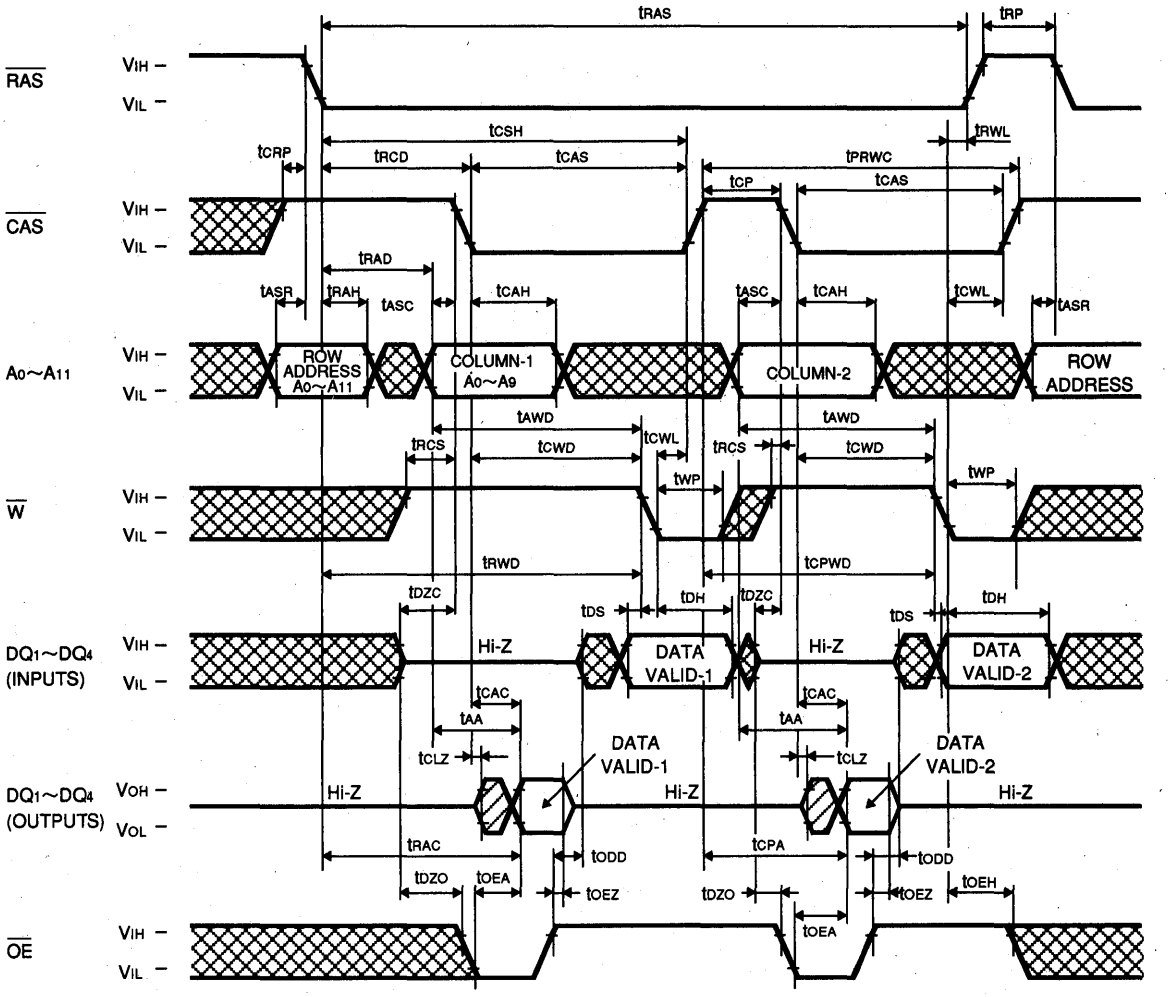
Fast Page Mode Write Cycle (Early Write)



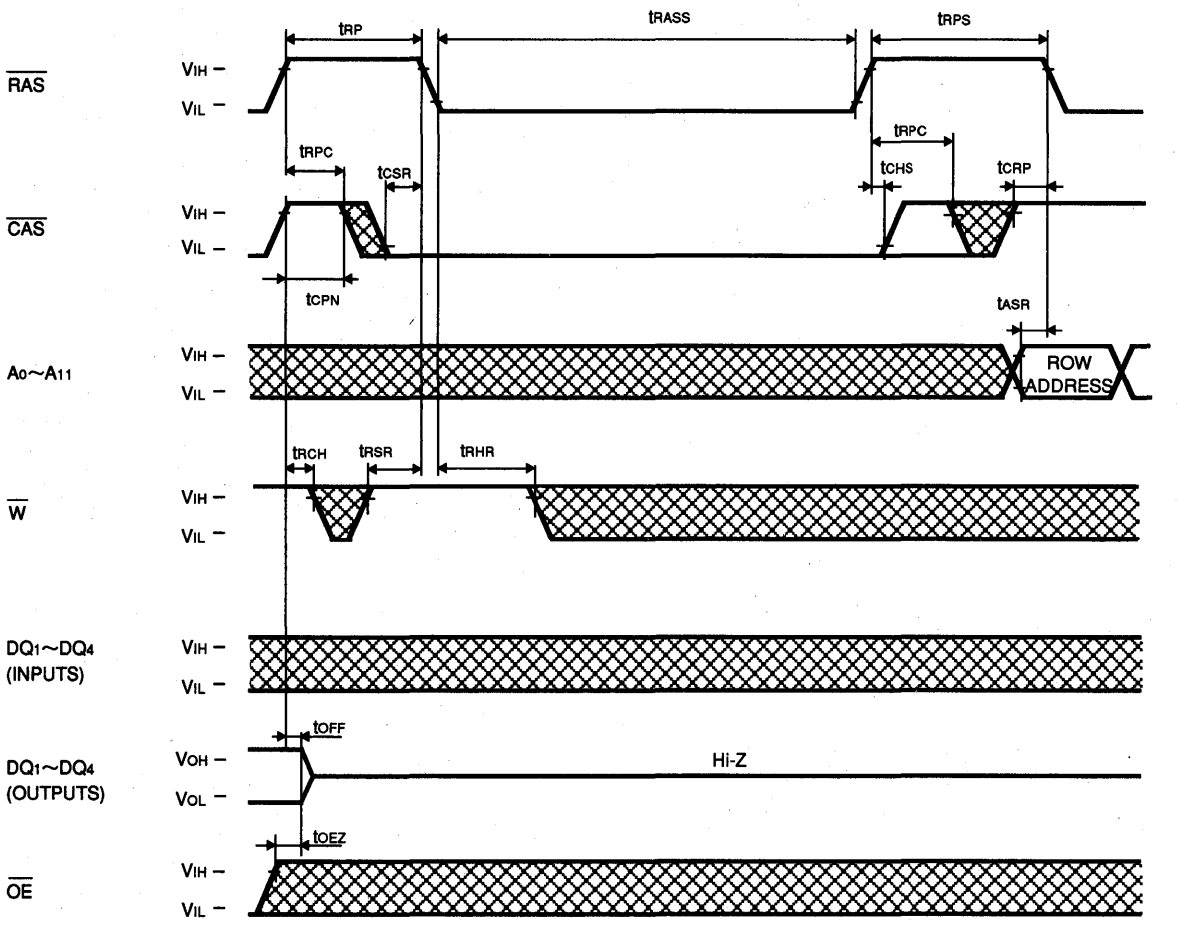
Fast-Page Mode Write Cycle (Delayed Write)



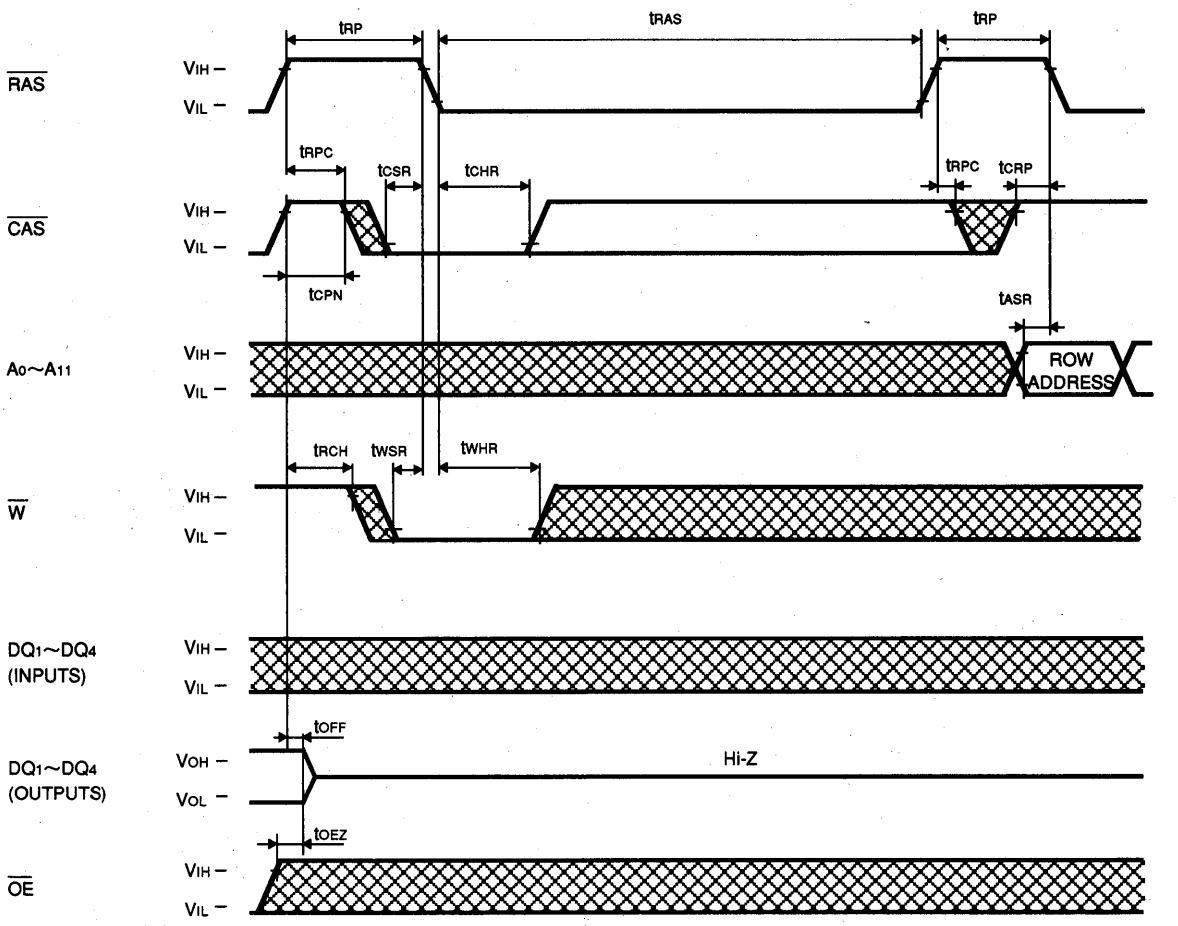
Fast Page Mode Read-Write,Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle (Note 29)



Note 29: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

M5M4V16400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16400CXX-5,-5S	50	13	25	13	90	330
M5M4V16400CXX-6,-6S	60	15	30	15	110	270
M5M4V16400CXX-7,-7S	70	20	35	20	130	225

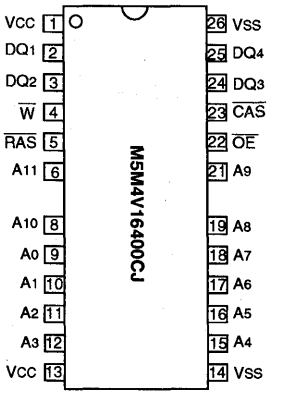
XX=J,TP

- Standard 26pin SOJ, 26pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.8mW (Max) ---------- CMOS Input level
  - 0.72mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M4V16400Cxx-5,-5S ---------- 400.0mW (Max)
  - M5M4V16400Cxx-6,-6S ---------- 325.0mW (Max)
  - M5M4V16400Cxx-7,-7S ---------- 270.0mW (Max)
- Self refresh capability *
  - self refresh current ---------- 200.0 μA(Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0~A_{11})
  * Applicable to self refresh version(M5M4V16400CJ,TP-5S,-6S,-7S :option) only

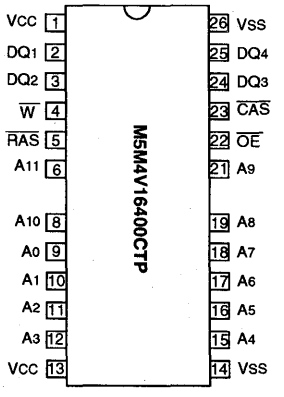
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_4	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

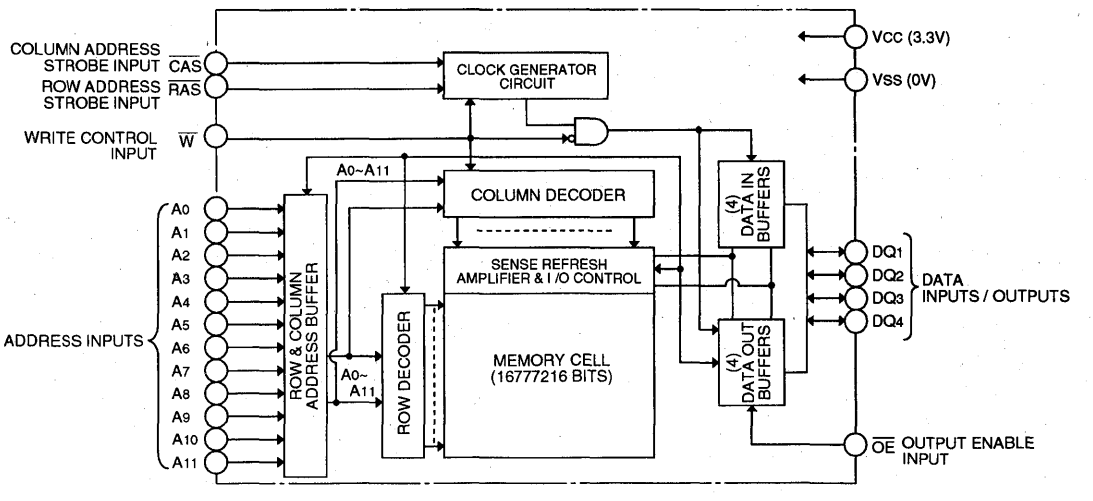
The M5M4V16400CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5～4.6	V
V_I	Input voltage		-0.5～4.6	V
V_O	Output voltage		-0.5～4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M4V16400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling			110	mA
		M5M4V16400C-6,-6S	t_{RC}=t_{WC}=min.			90	
		M5M4V16400C-7,-7S	output open			75	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M4V16400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH}			110	mA
		M5M4V16400C-6,-6S	t_{RC}=min.			90	
		M5M4V16400C-7,-7S	output open			75	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M4V16400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling			80	mA
		M5M4V16400C-6,-6S	t_{PC}=min.			70	
		M5M4V16400C-7,-7S	output open			60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			110	mA
		M5M4V16400C-6,-6S	t_{RC}=min.			90	
		M5M4V16400C-7,-7S	output open			75	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS(Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS	(Note 6,7)		13		15		20	ns
tRAC	Access time from RAS	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from CAS precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from OE	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from CAS low	(Note 6)	5		5		5		ns
tOFF	Output disable time after CAS high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after OE high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization RAS cycles. The initialization cycles should be done either by RAS-only refresh cycles or by CAS before RAS refresh cycles only.
Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 64ms) of RAS inactivity before proper device operation is achieved.
After the initialization cycles, RAS should be kept either higher than VIH(min) or lower than VIL(max) except RAS transition time.
6:Measured with a load circuit equivalent to 2TTL loads and 100pF. The reference levels for measuring of output signals are 2.0V (VOH) and 0.8V (VOL).
7:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max).
8:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
9:Assumes that tRAD≧tRAD(max) and tASC≦tASC(max).
10:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT≦|±10 μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tRP	RAS high pulse width		30		40		50		ns
tRCD	Delay time, RAS low to CAS low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low		10		10		10		ns
tRPC	Delay time, RAS high to CAS low		0		0		0		ns
tCPN	CAS high pulse width		10		10		10		ns
tRAD	Column address delay time from RAS low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low		0		0		0		ns
tASC	Column address setup time before CAS low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after RAS low		8		10		10		ns
tCAH	Column address hold time after CAS low		13		15		15		ns
tDZC	Delay time, data to CAS low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to OE low	(Note 17)	0		0		0		ns
tCDD	Delay time, CAS high to data	(Note 18)	13		15		15		ns
tODD	Delay time, OE high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.
13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).
15:tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
16:tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
17:Either tDZC or tDZO must be satisfied.
18:Either tCDD or tODD must be satisfied.
19:tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low (Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low (Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 21)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 22)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 21: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.

22: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits						Unit
			M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 25)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

25: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	M5M4V16400C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}\&\overline{WE} \leqq 0.2V$ or $\overline{OE}\&\overline{WE} \geqq Vcc-0.2V$ $A_0 \sim A_{11} \leqq 0.2V$ or $A_0 \sim A_{11} \geqq Vcc-0.2V$ t_{REF}=128ms (4096cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M4V16400C (S)	$\overline{RAS}$ = $\overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

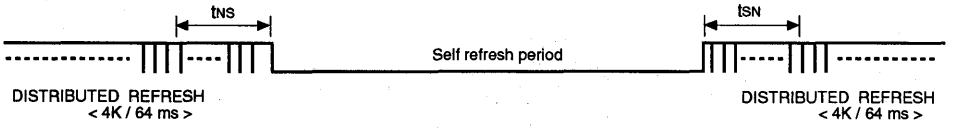
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M4V16400C-5S		M5M4V16400C-6S		M5M4V16400C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

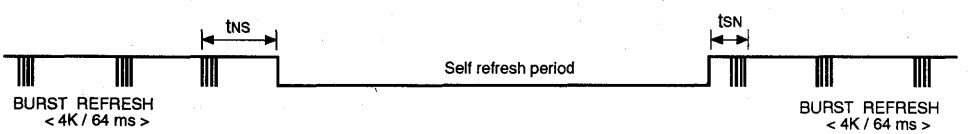
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64$ms and $t_{SN} \leqq 64$ms.



(2) In case of burst refresh

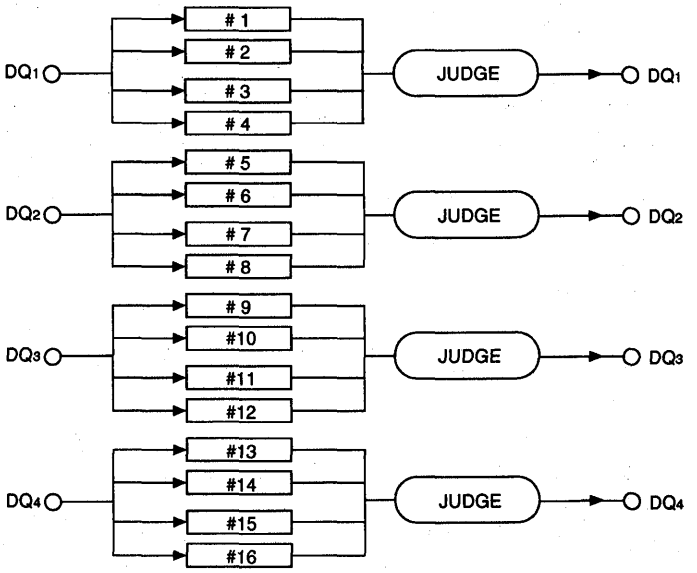
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 64$ms.



TEST Mode SET Cycle

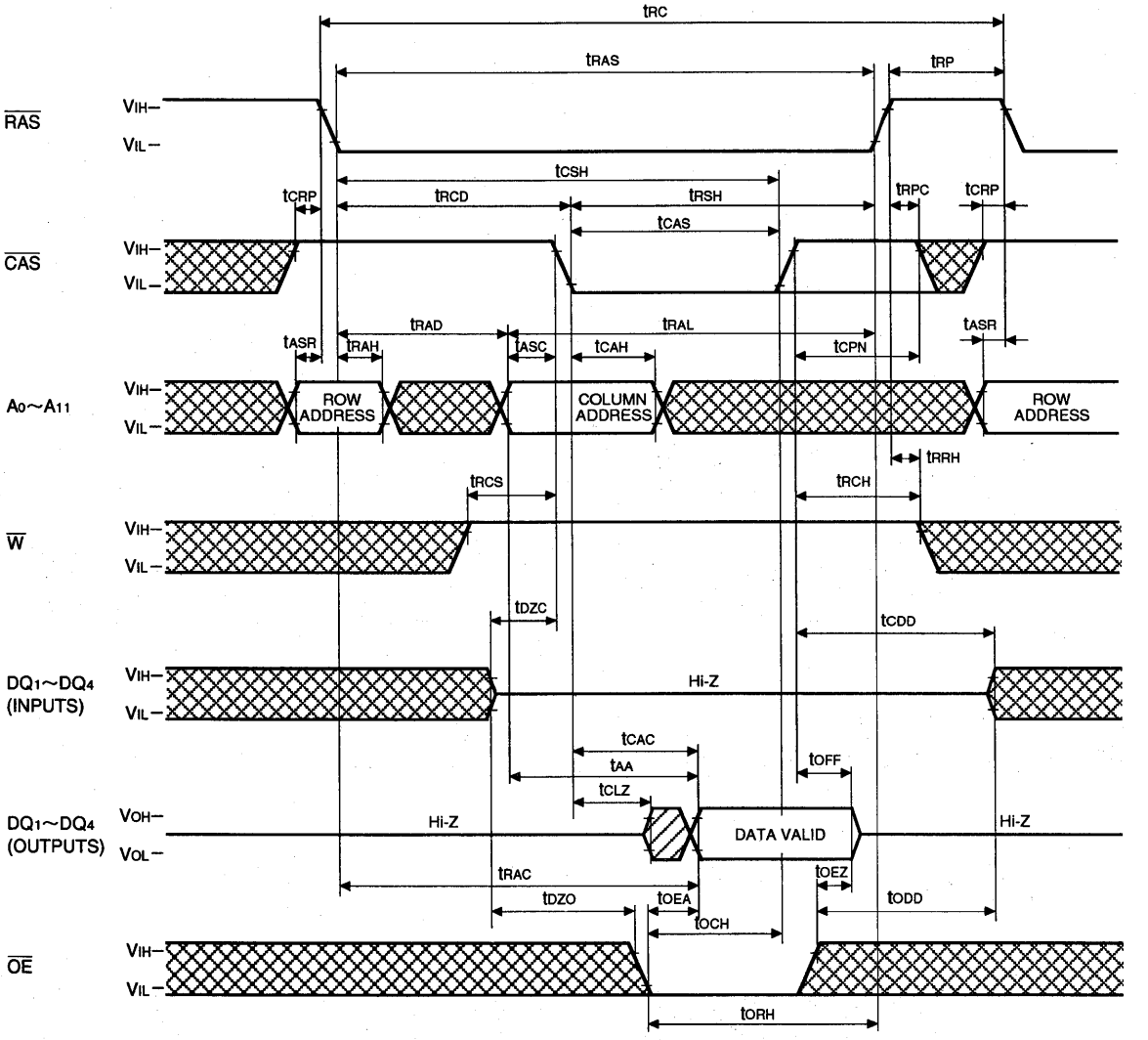
Symbol	Parameter	Limits						Unit
		M5M4V16400C-5,-5S		M5M4V16400C-6,-6S		M5M4V16400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0 and CA_1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 28)
Read Cycle

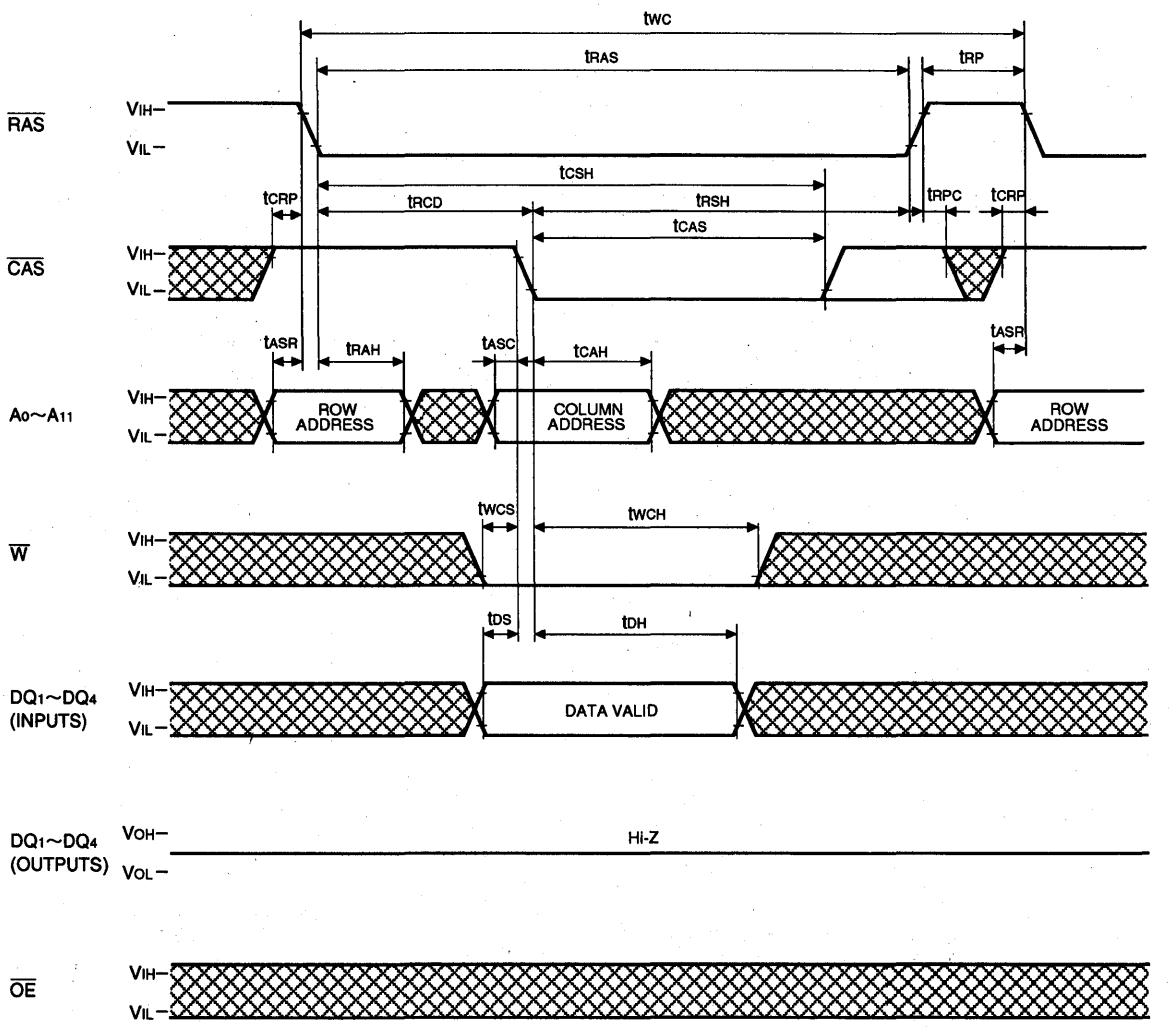


Note 28

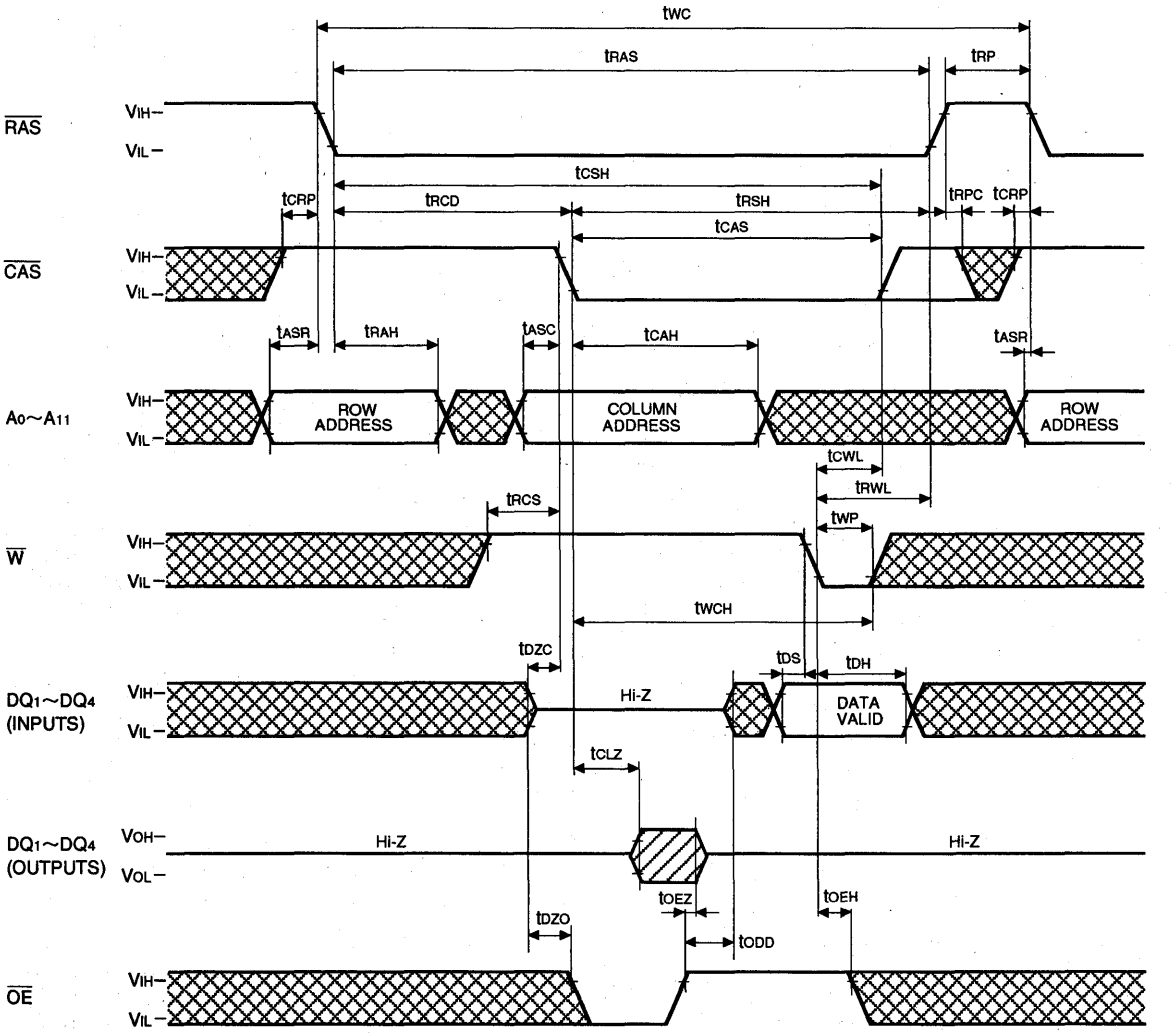
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

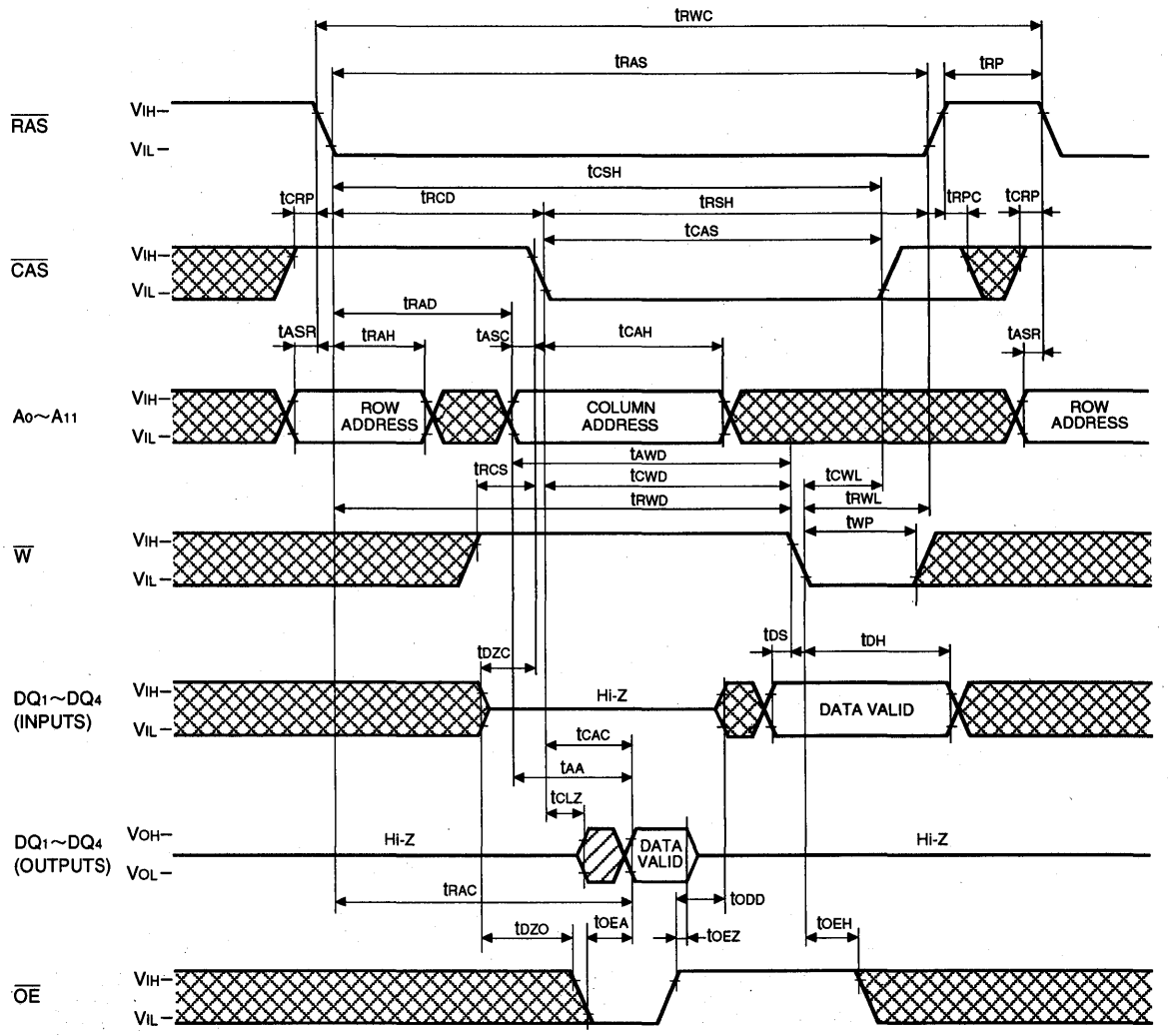
Write Cycle (Early write)



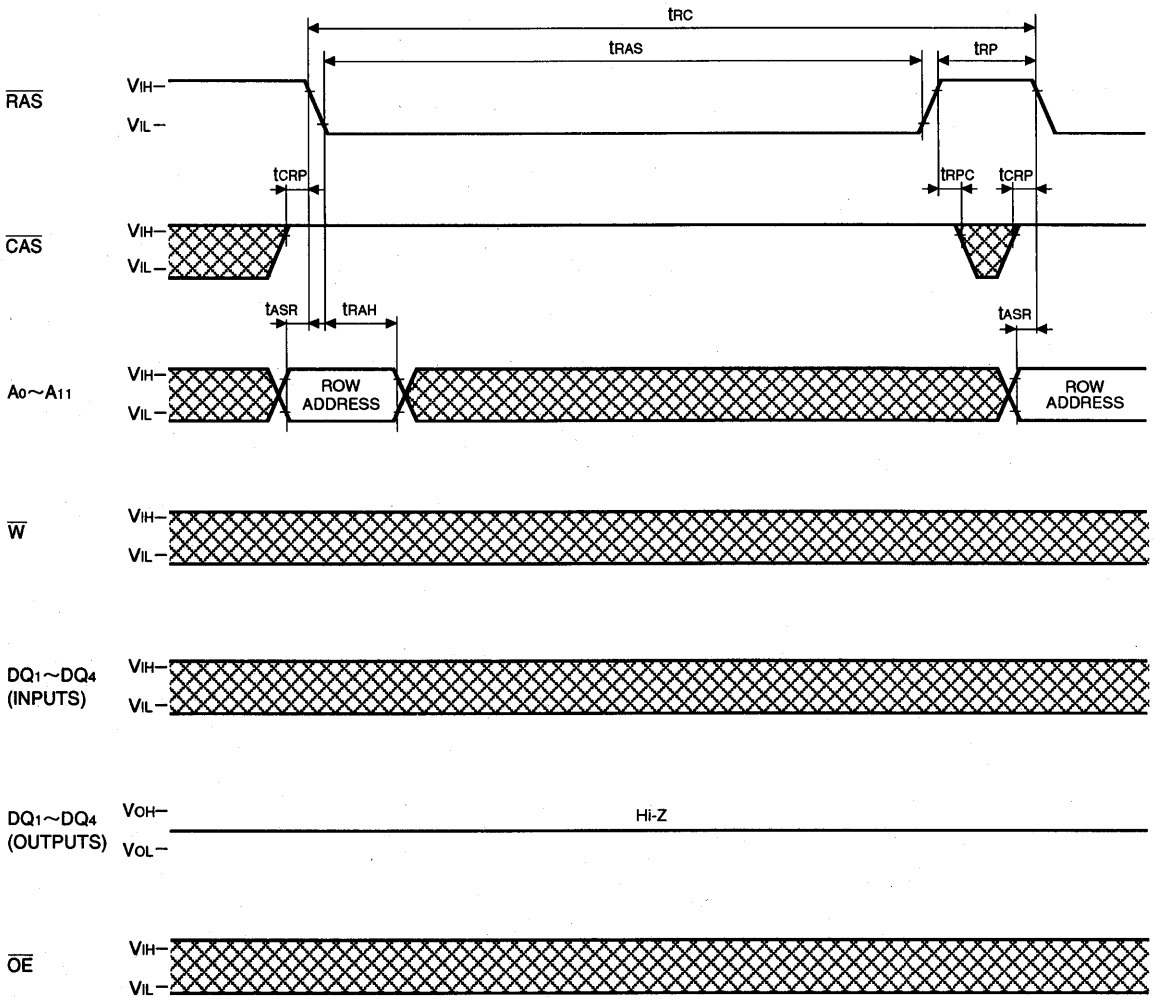
Write Cycle (Delayed write)



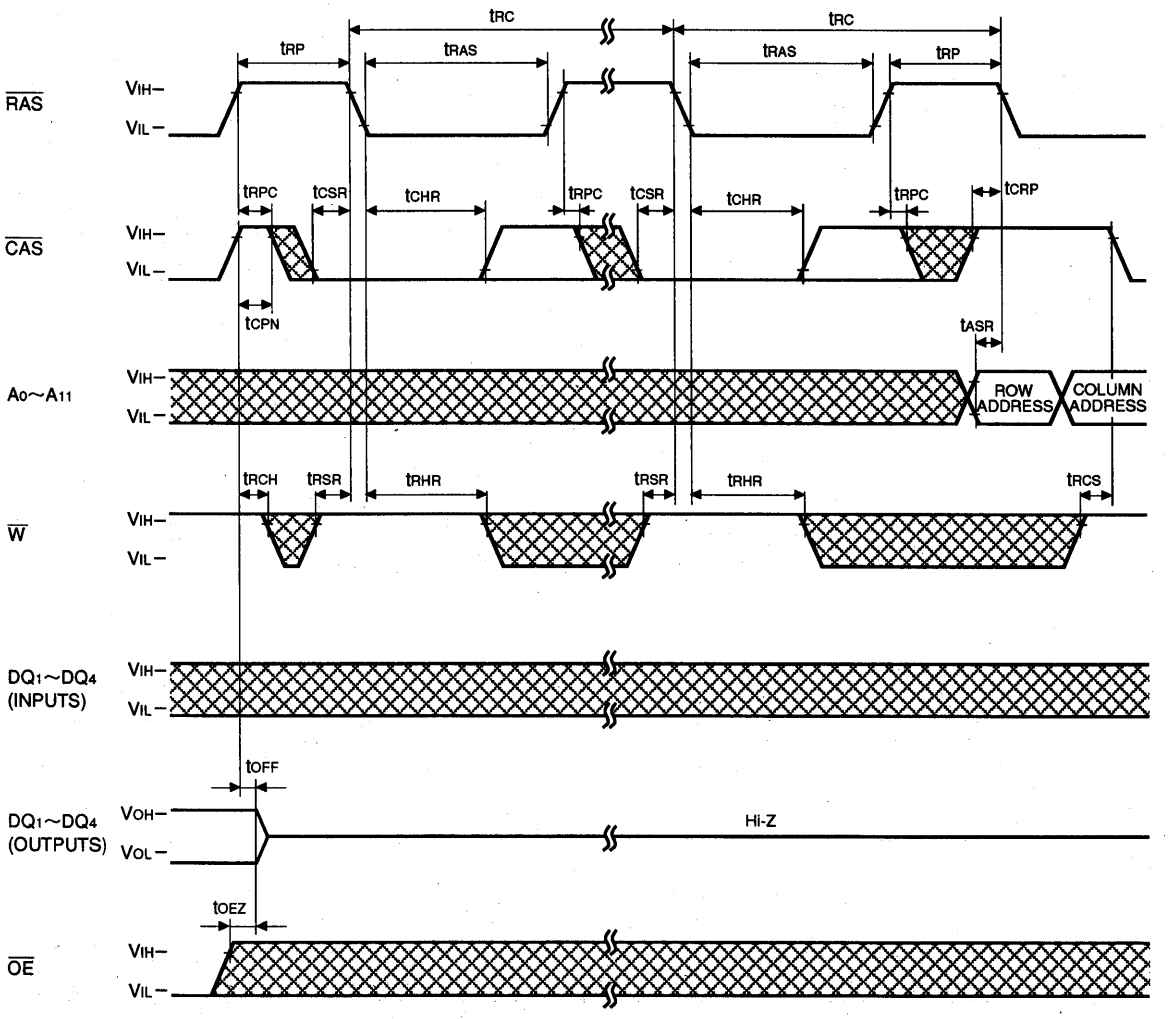
Read-Write, Read-Modify-Write Cycle



$\overline{\text{RAS}}$-only Refresh Cycle

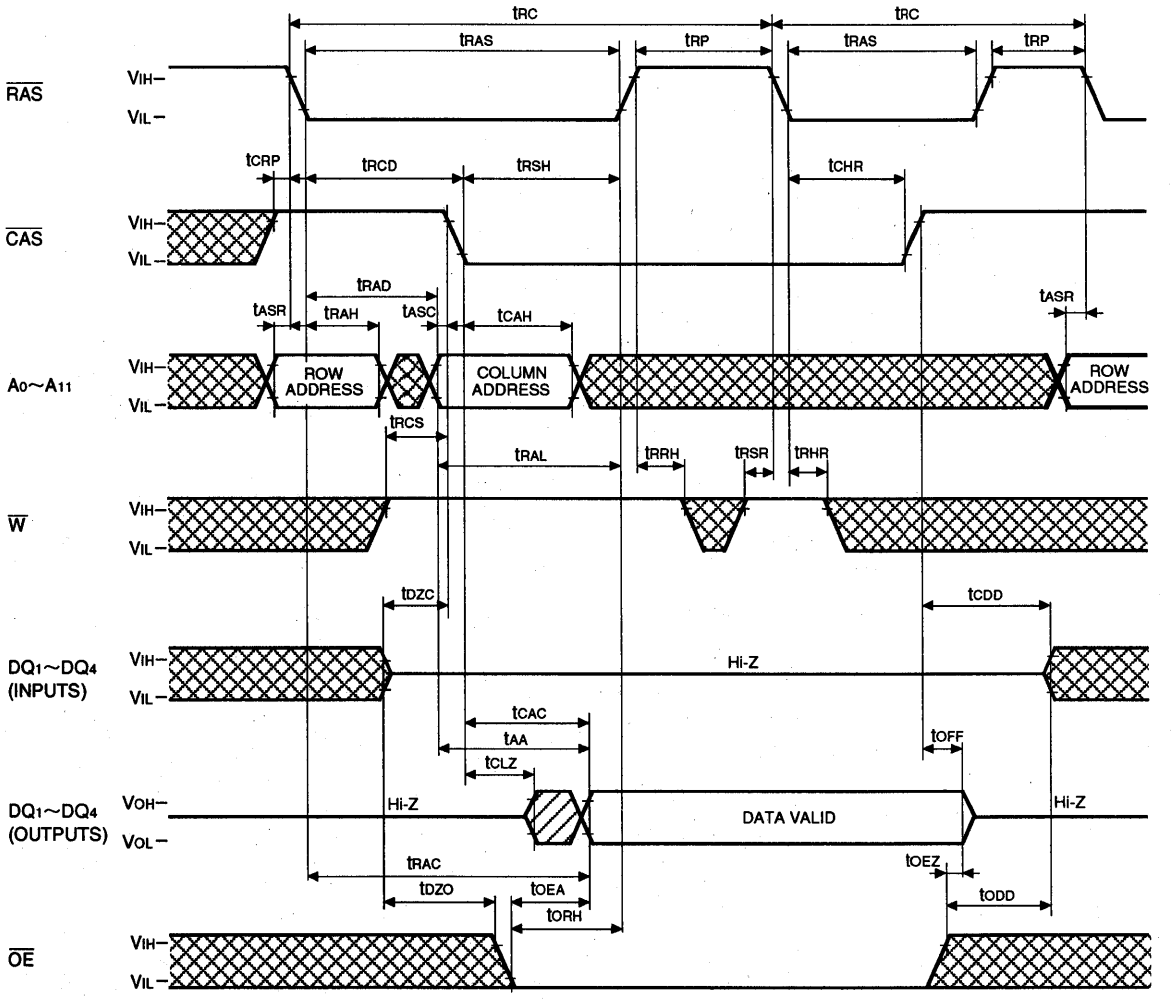


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle , Slow Refresh Cycle



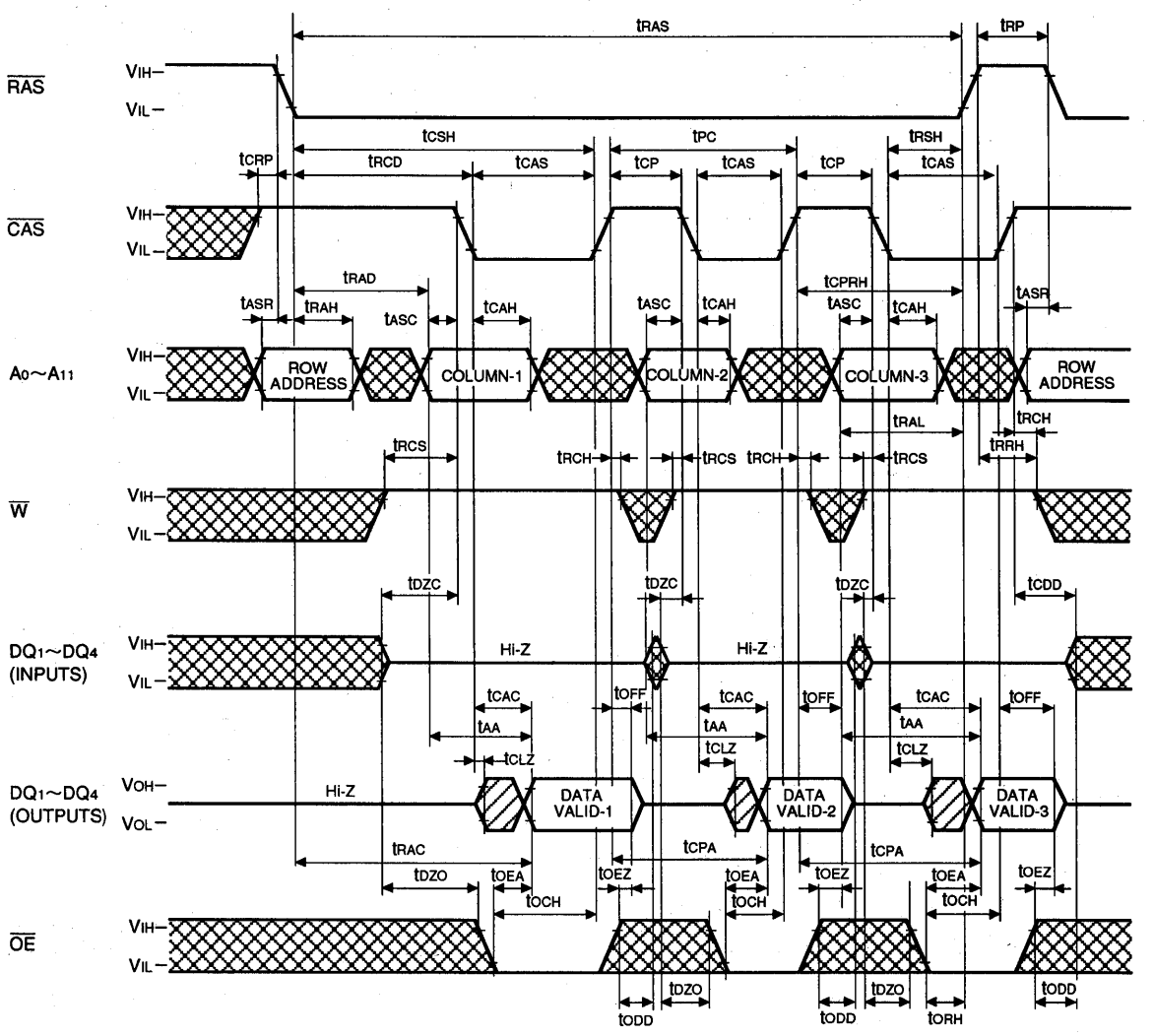
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hidden Refresh Cycle (Read) (Note 29)



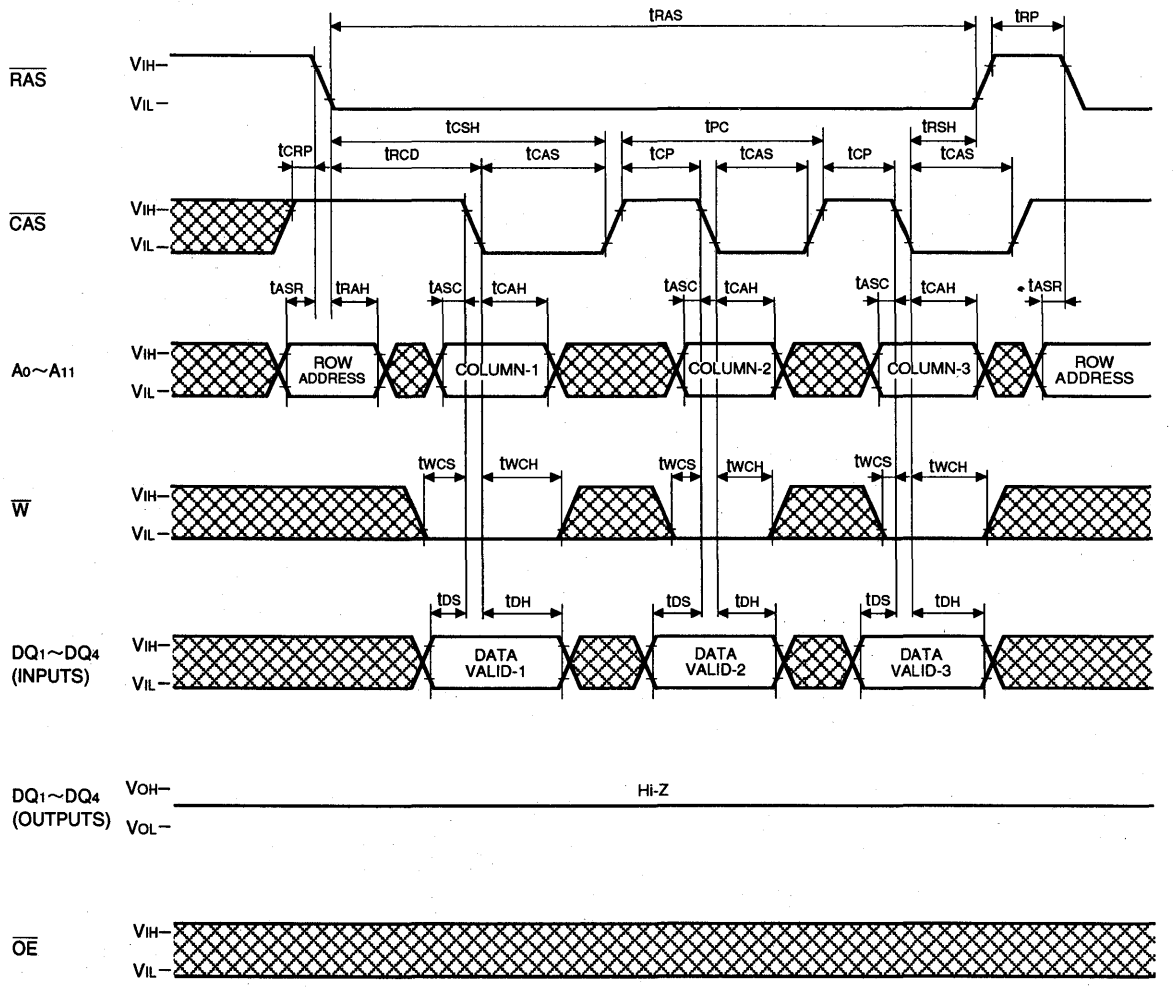
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

Fast Page Mode Read Cycle

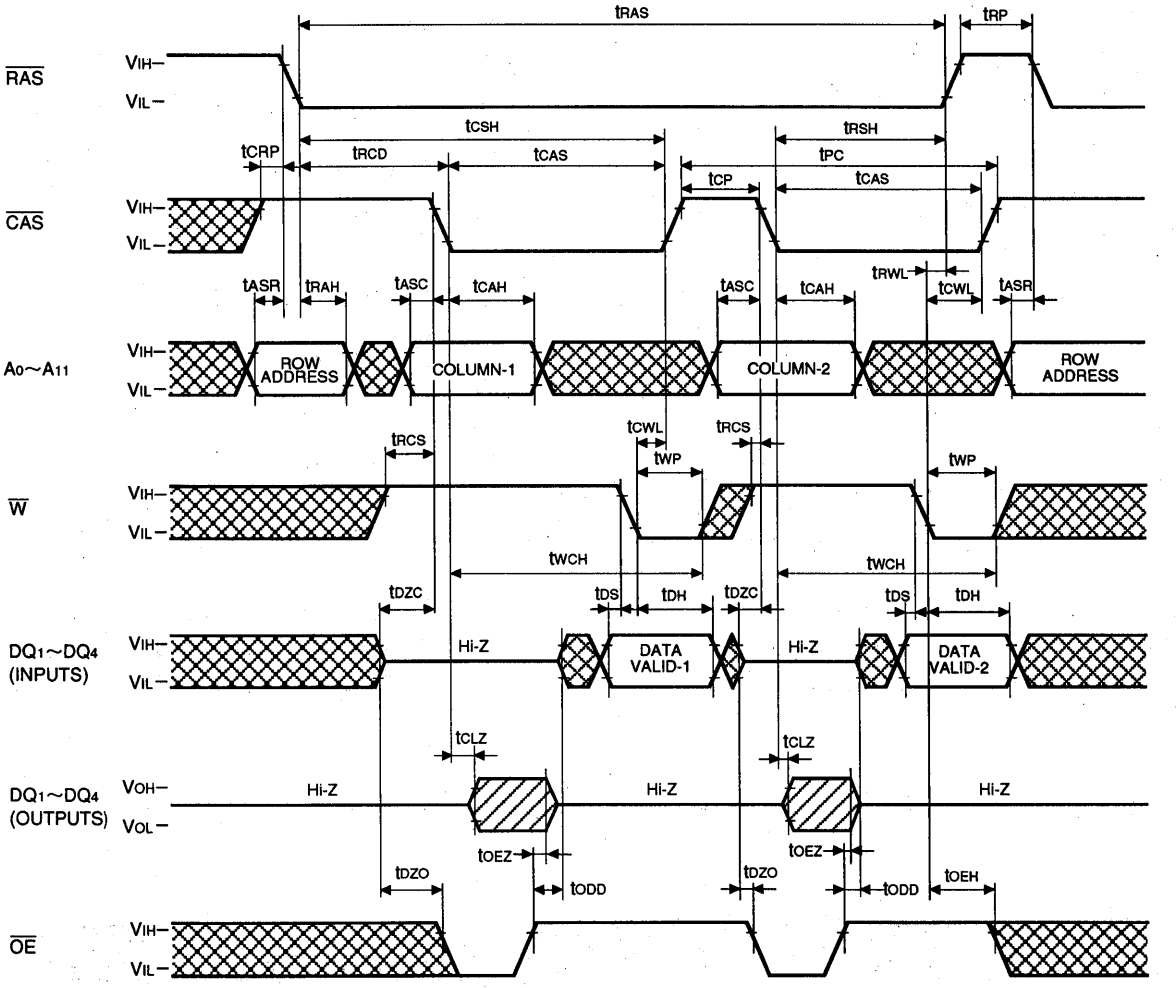


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)

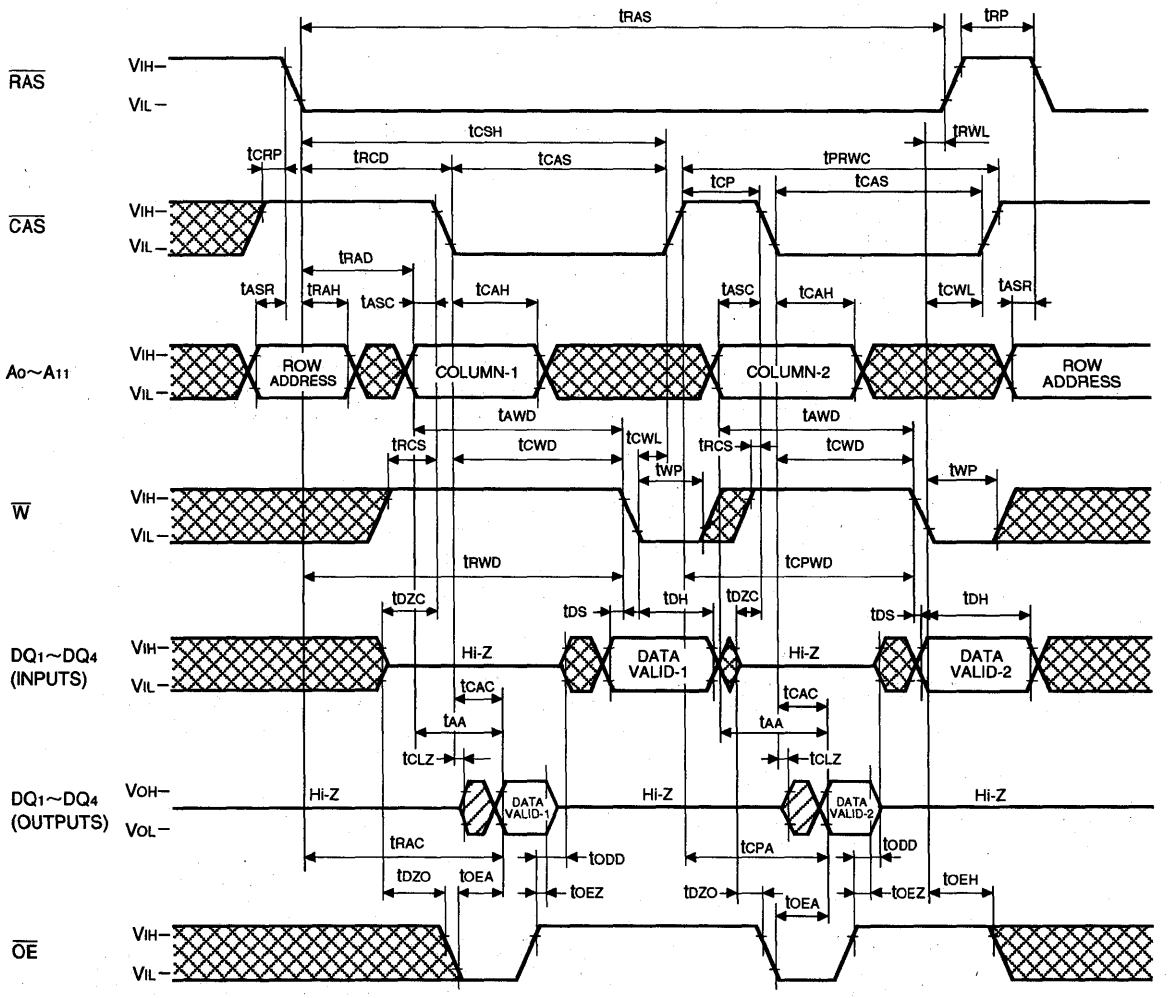


Fast-Page Mode Write Cycle (Delayed Write)

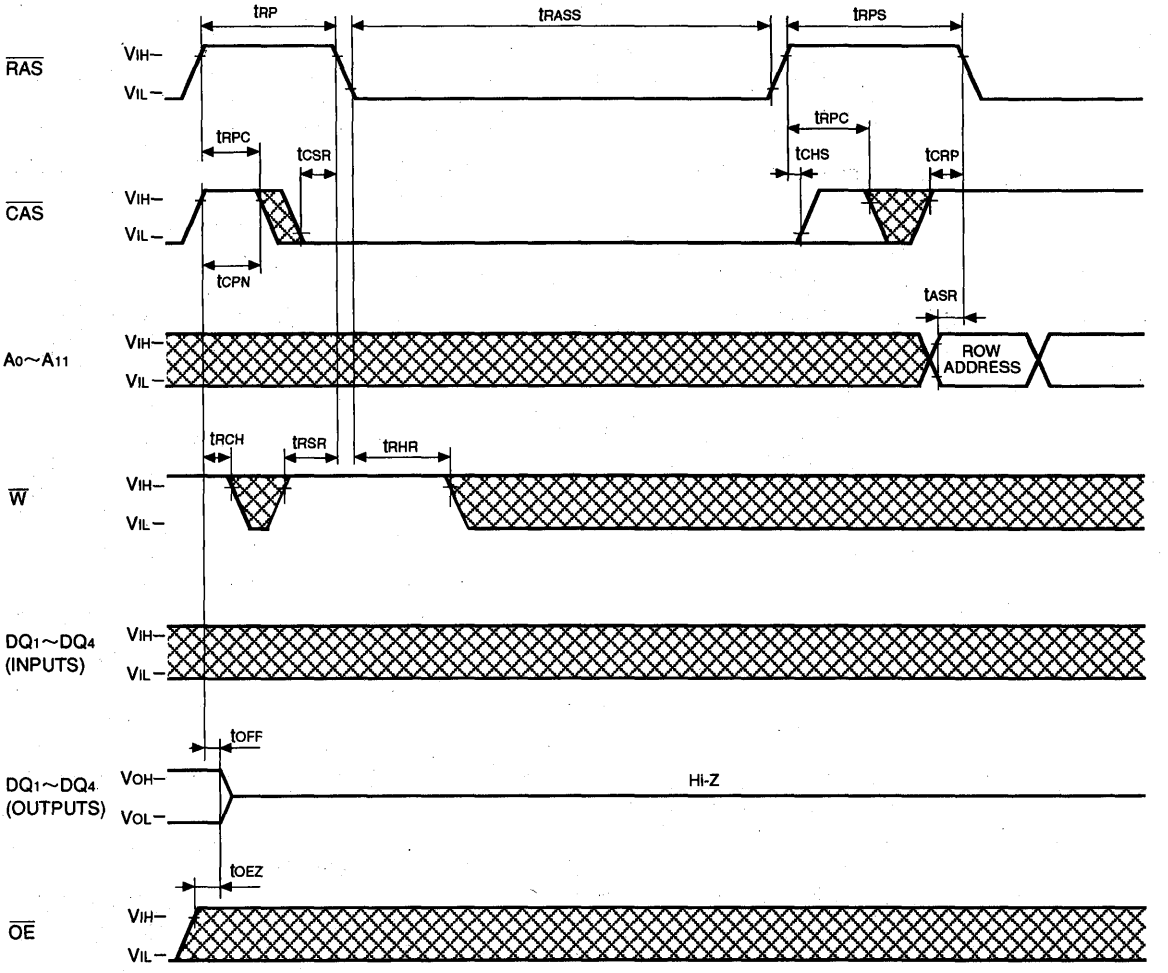


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read-Write,Read-Modify-Write Cycle

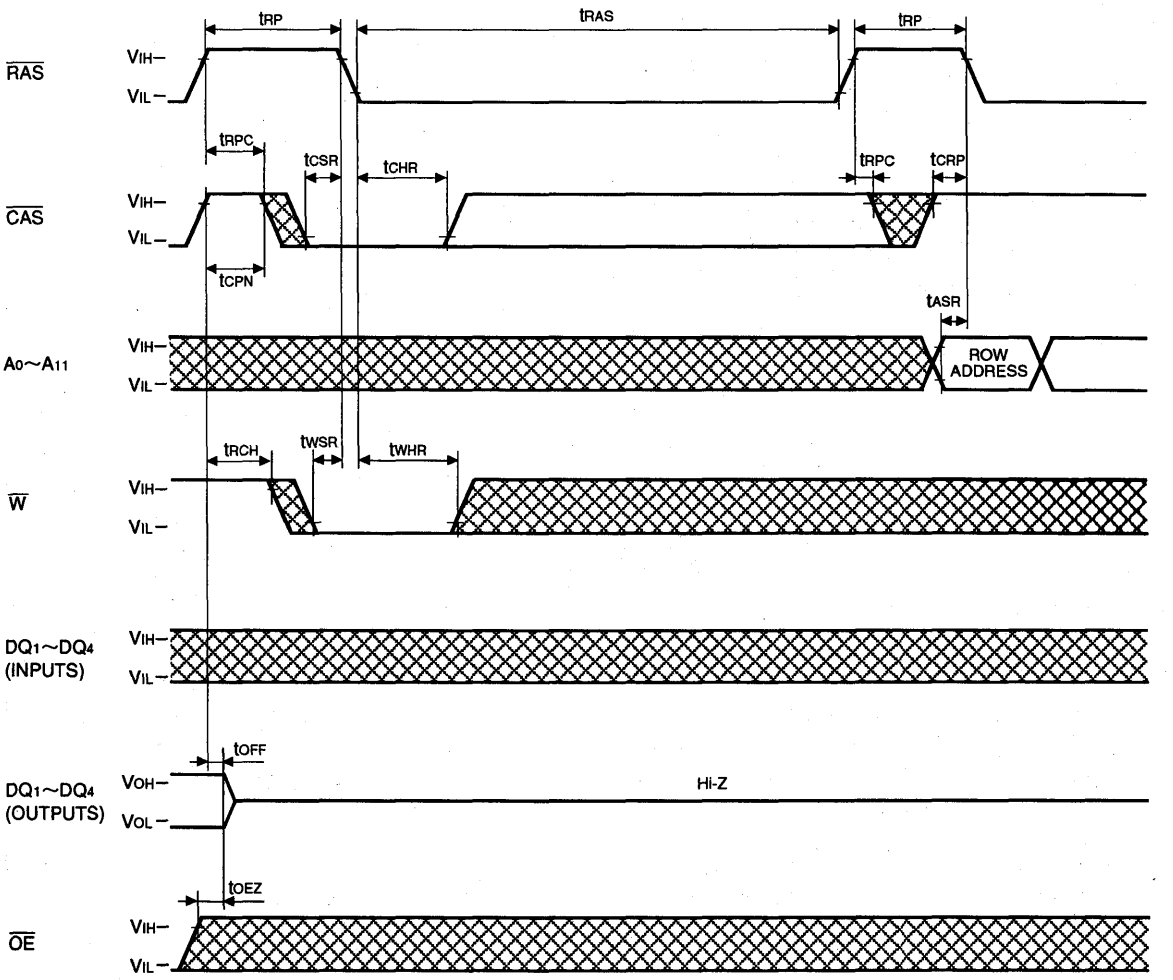


Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16405CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16405CXX-5,-5S	50	13	25	13	90	330
M5M4V16405CXX-6,-6S	60	15	30	15	110	270
M5M4V16405CXX-7,-7S	70	20	35	20	130	225

XX=J,TP

- Standard 26pin SOJ, 26pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.80mW (Max) ---------- CMOS Input level
  - 0.72mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M4V16405Cxx-5,-5S ---------- 400mW (Max)
  - M5M4V16405Cxx-6,-6S ---------- 325mW (Max)
  - M5M4V16405Cxx-7,-7S ---------- 270mW (Max)
- Self refresh capability *
  - Self refresh current ----------200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})

  *:Applicable to self refresh version (M5M4V16405CJ,TP-5S,-6S, -7S:option) only

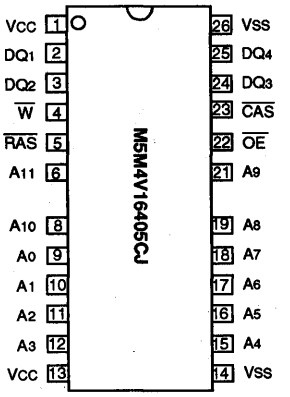
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

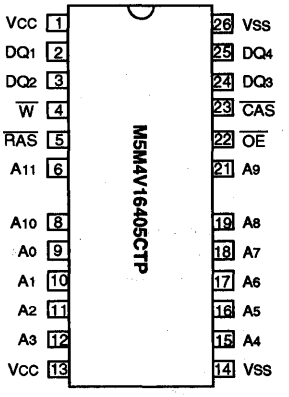
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

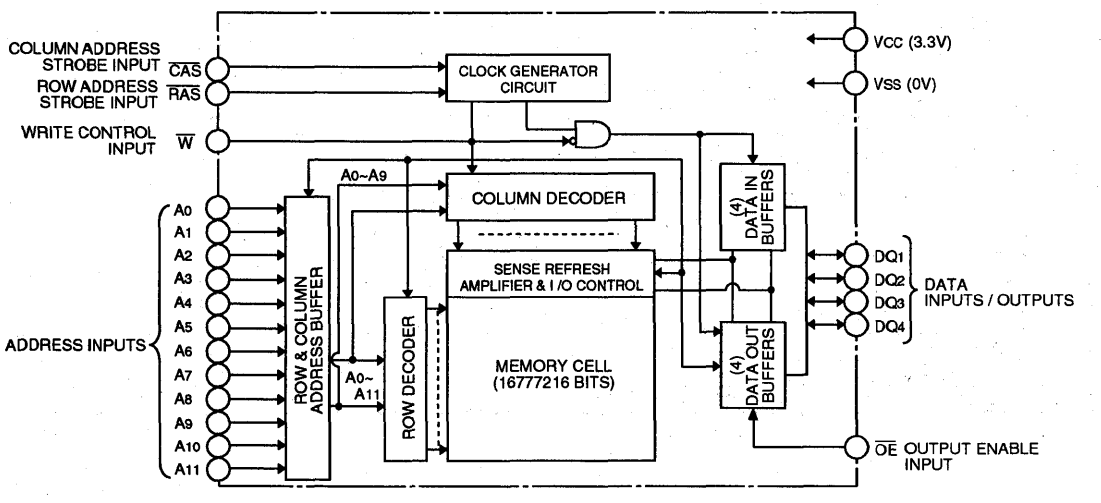
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M4V16405CJ,TP provides a number of other functions, e.g., $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
V_I	Input voltage		-0.5 ~ 4.6	V
V_O	Output voltage		-0.5 ~ 4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3**		0.8	V

Note 1 : All voltage values are with respect to Vss.
**: V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from V_{CC}, operating (Note 3,4,5)	M5M4V16405C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from V_{CC}, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V16405C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	
I_{CC4}(AV)	Average supply current from V_{CC}, Hyper Page Mode (Note 3,4,5)	M5M4V16405C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M4V16405C-6,-6S				115	
		M5M4V16405C-7,-7S				90	
I_{CC6}(AV)	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V16405C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) , I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			8	pF

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0～70℃, Vcc = 3.3V ±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (I OUT≦ |±10 μ A|) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ～70℃, Vcc = 3.3V ±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT=2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper Page Mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 6)	M5M4V16405C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$≦0.2V $\overline{OE}$ & $\overline{WE}$≦0.2V or $\overline{OE}$ & $\overline{WE}$≧Vcc-0.2V A_0~A_{11}≦0.2V or A_0~A_{11}≧Vcc-0.2V t_{REF}=128ms (4096cycles) output=OPEN t_{RAS}=t_{RAS}min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 6)	M5M4V16405C (S)	$\overline{RAS}$=$\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

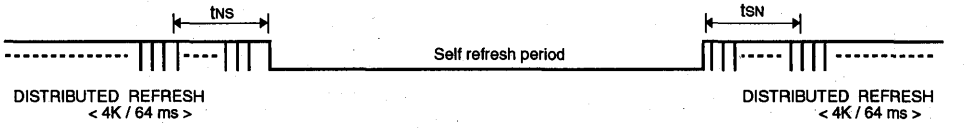
TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted, see notes 14, 15)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5S		M5M4V16405C-6S		M5M4V16405C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

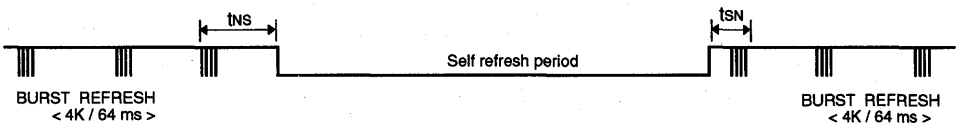
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦64ms and t_{SN}≦64ms.



(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}+t_{SN}≦64ms.

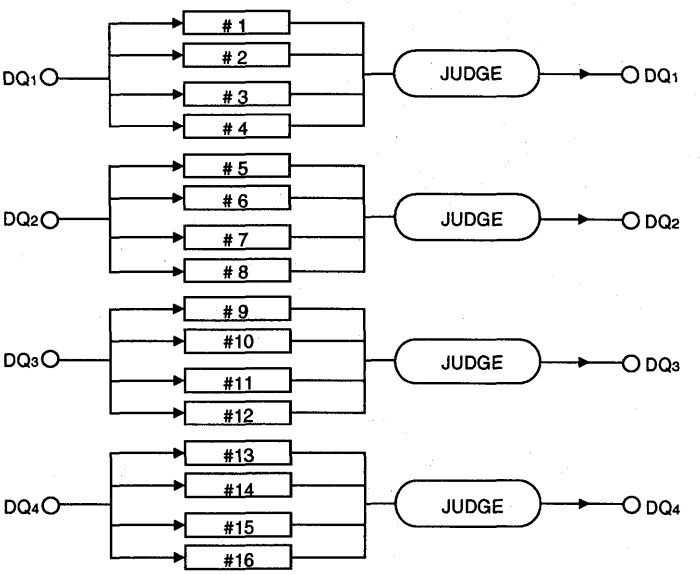


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

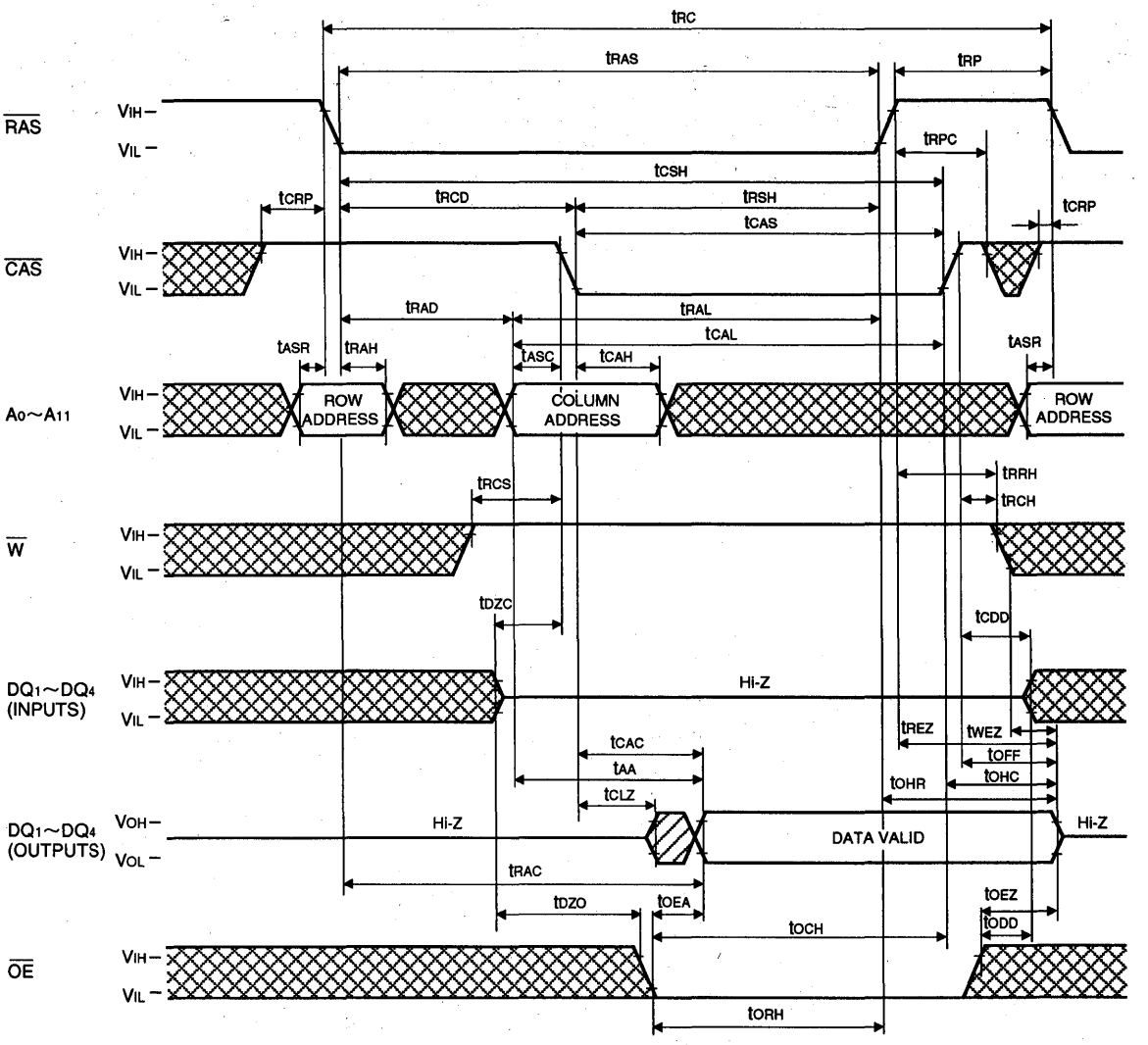
TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA 0 and CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 32)
Read Cycle

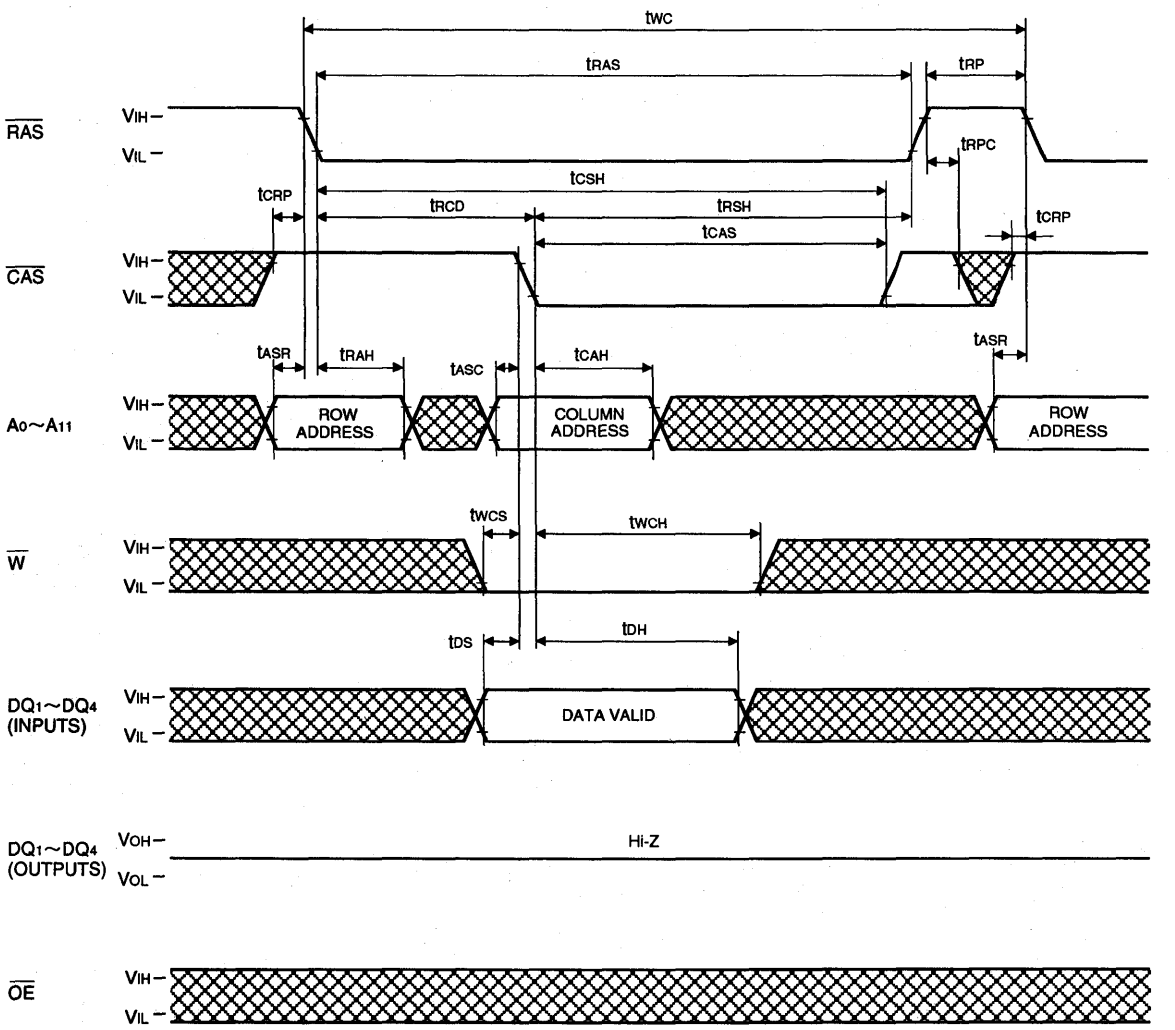


Note 32

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

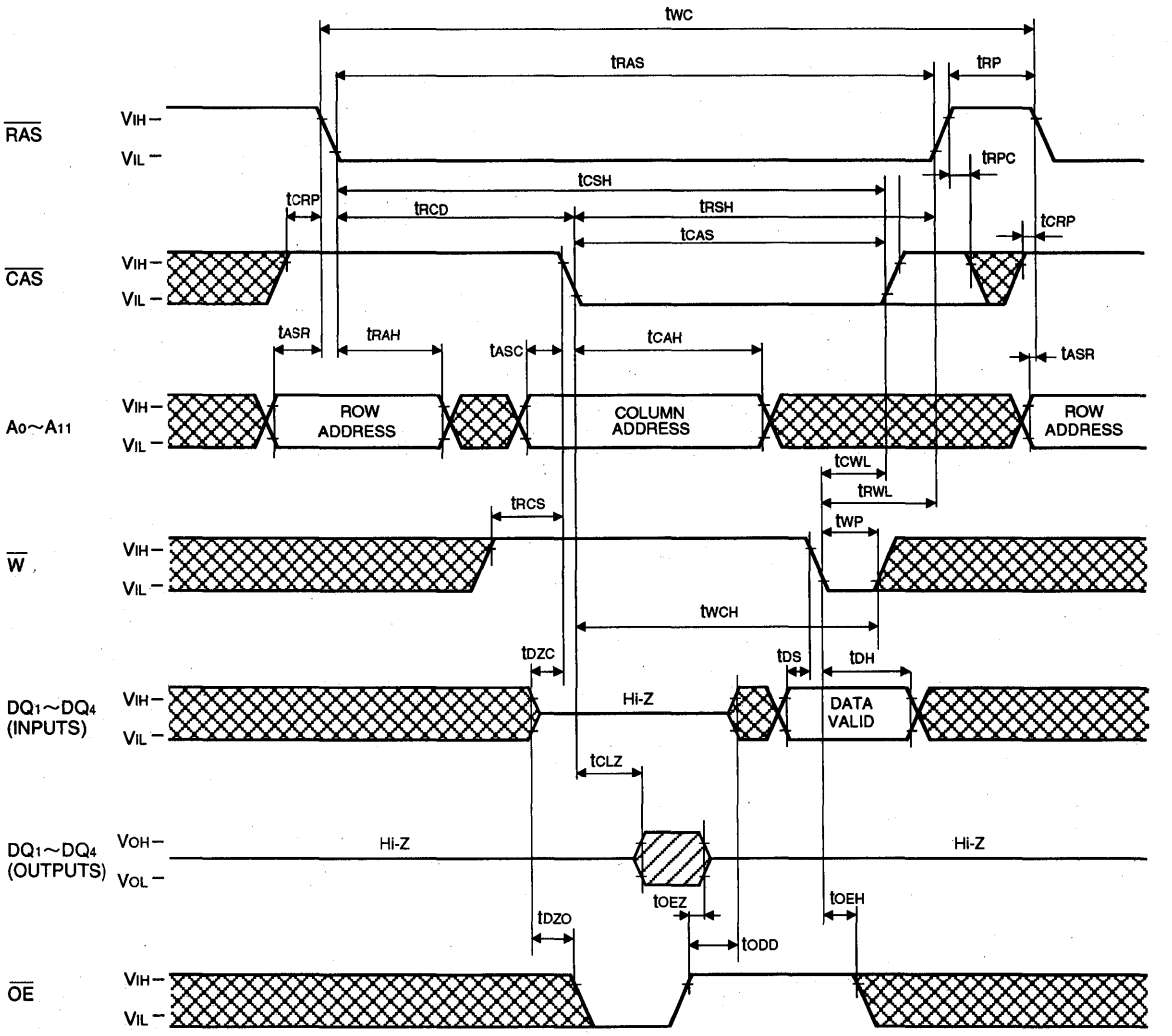
Indicates the invalid output.

Early Write Cycle

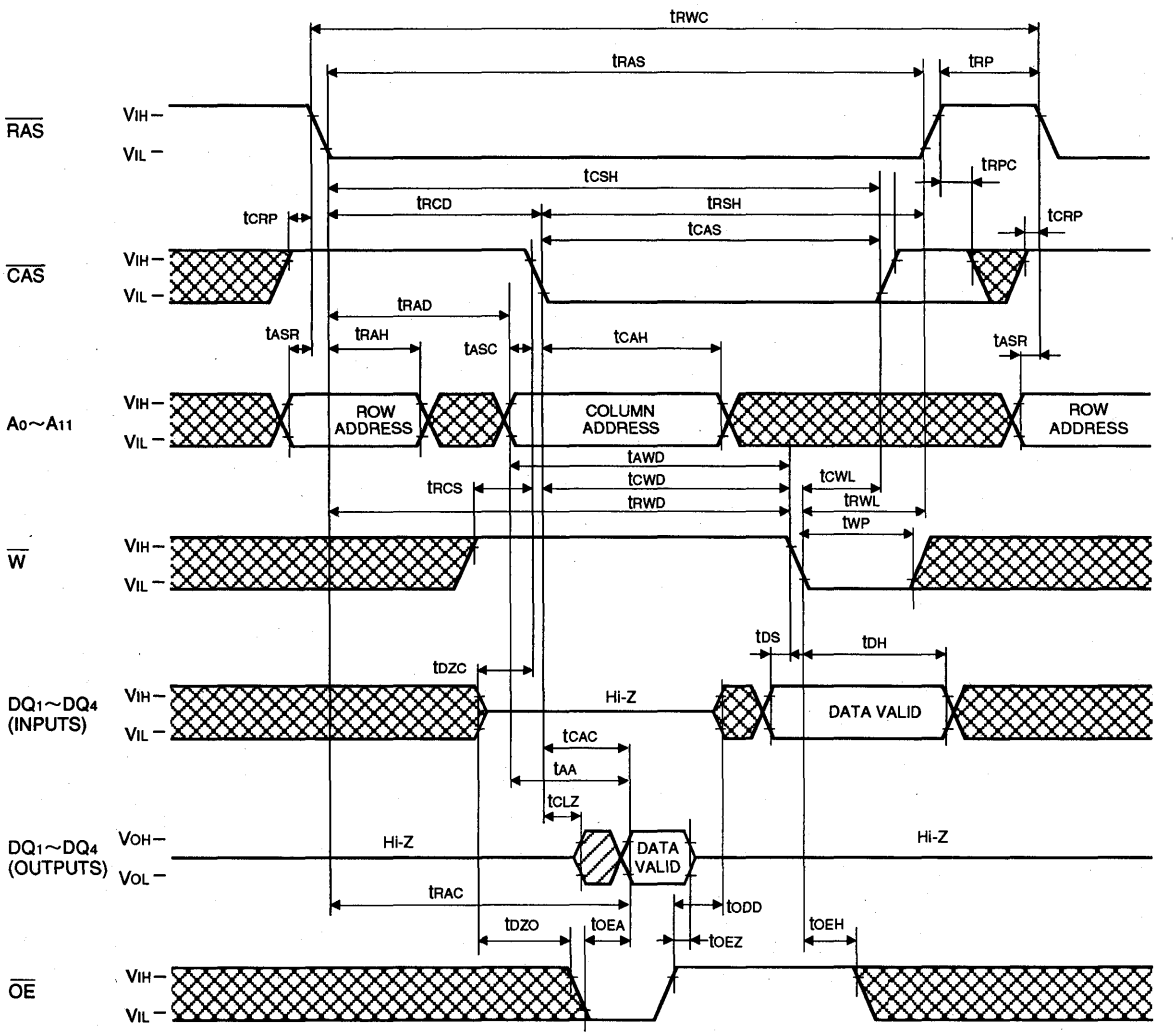


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Delayed Write Cycle

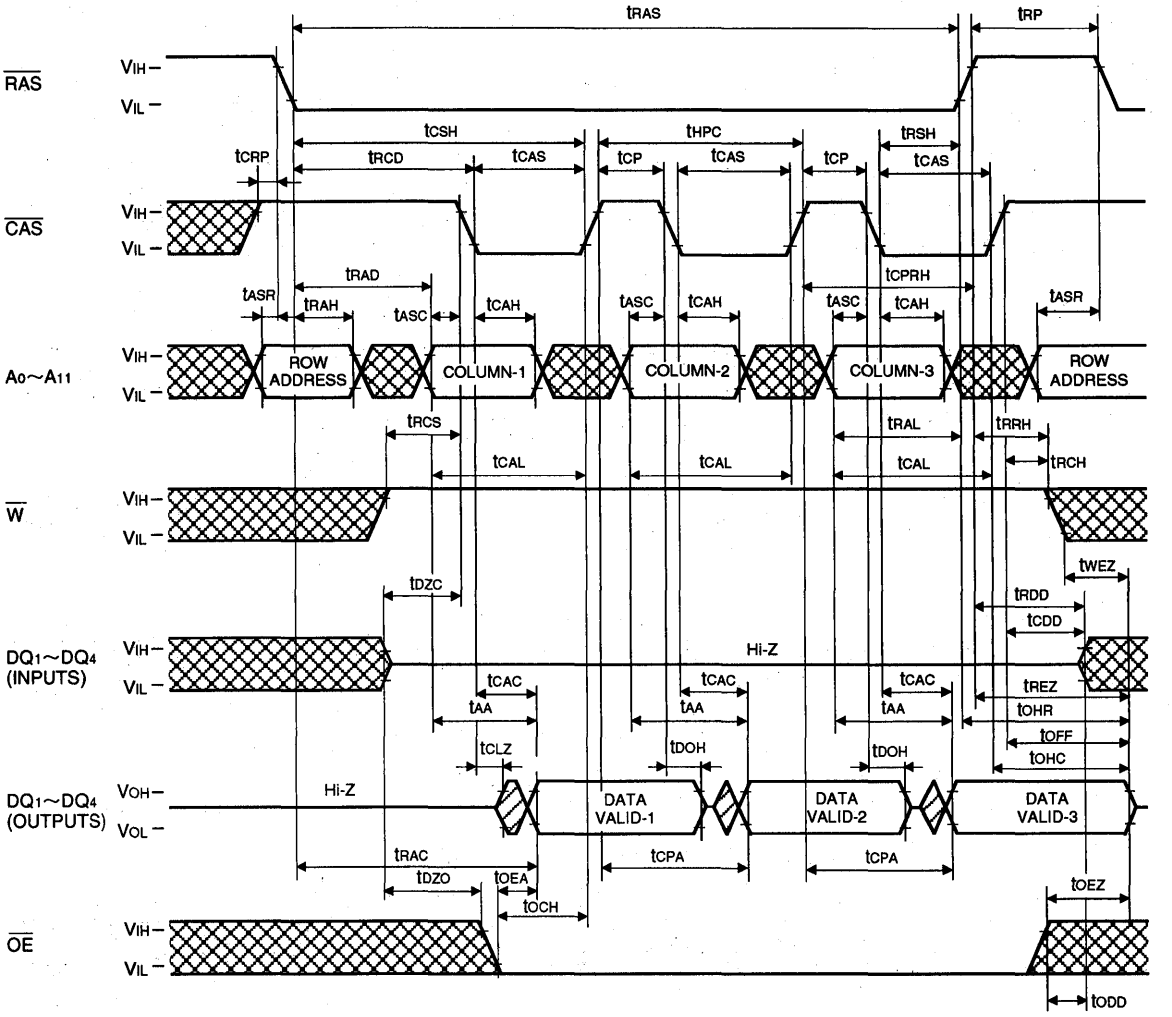


Read-Write, Read-Modify-Write Cycle

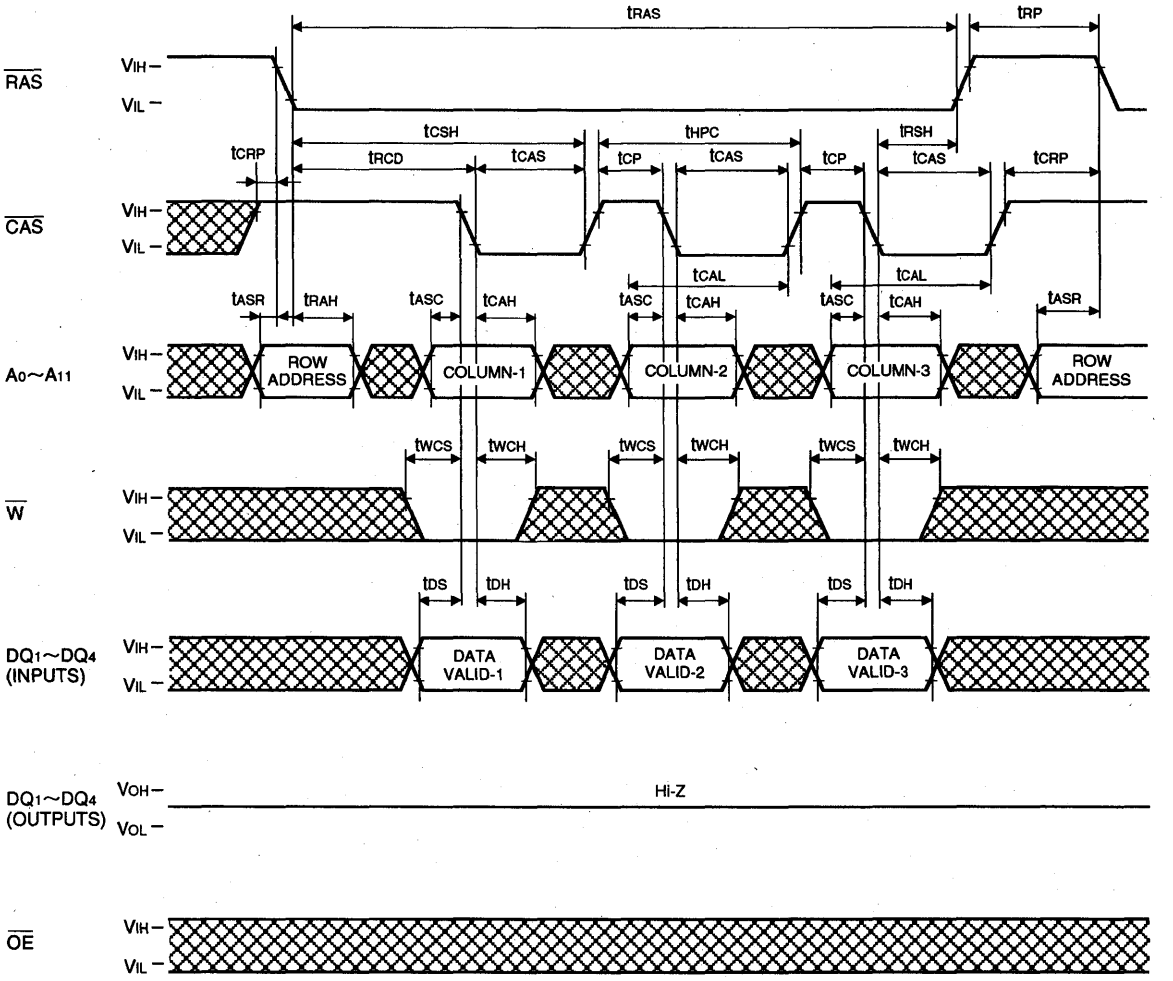


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

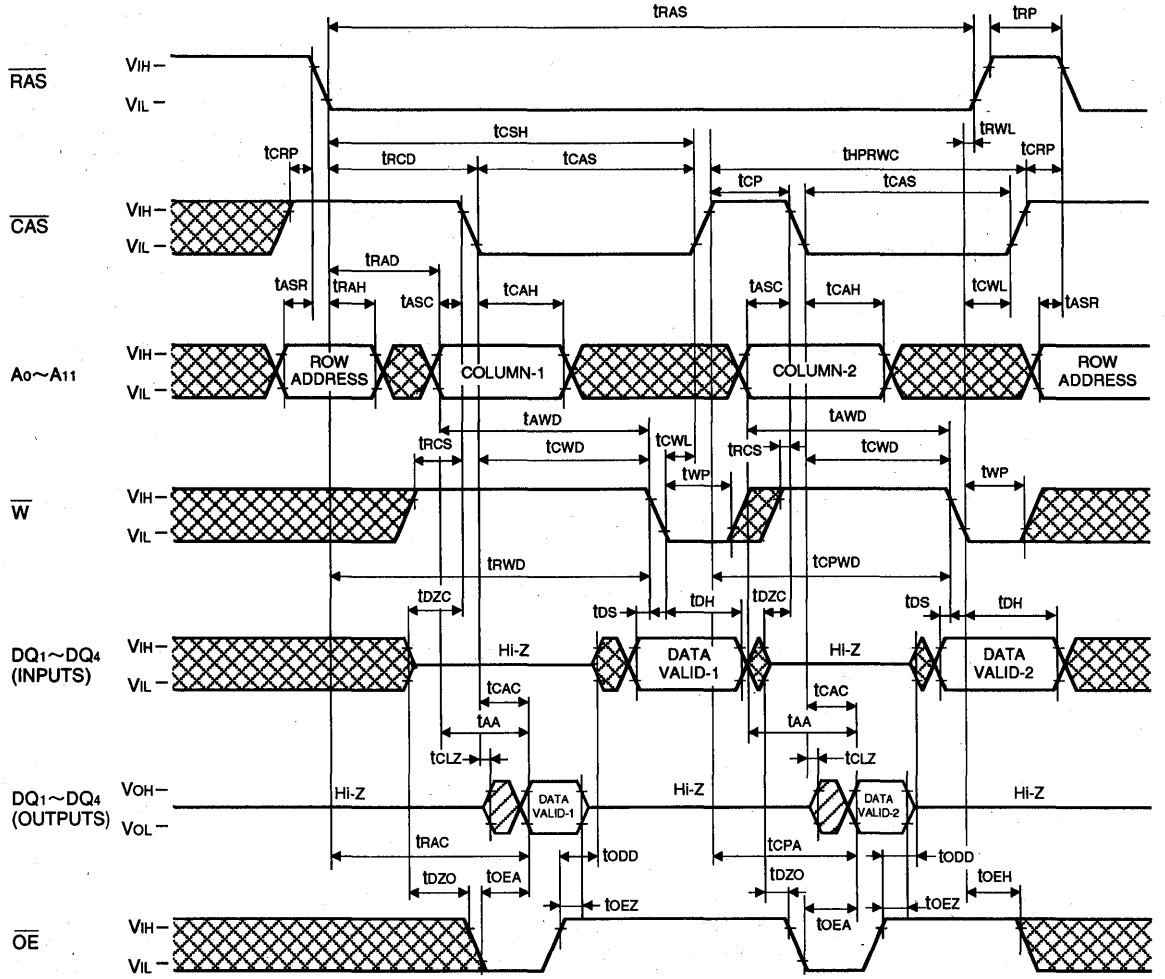
Hyper Page Mode Read Cycle



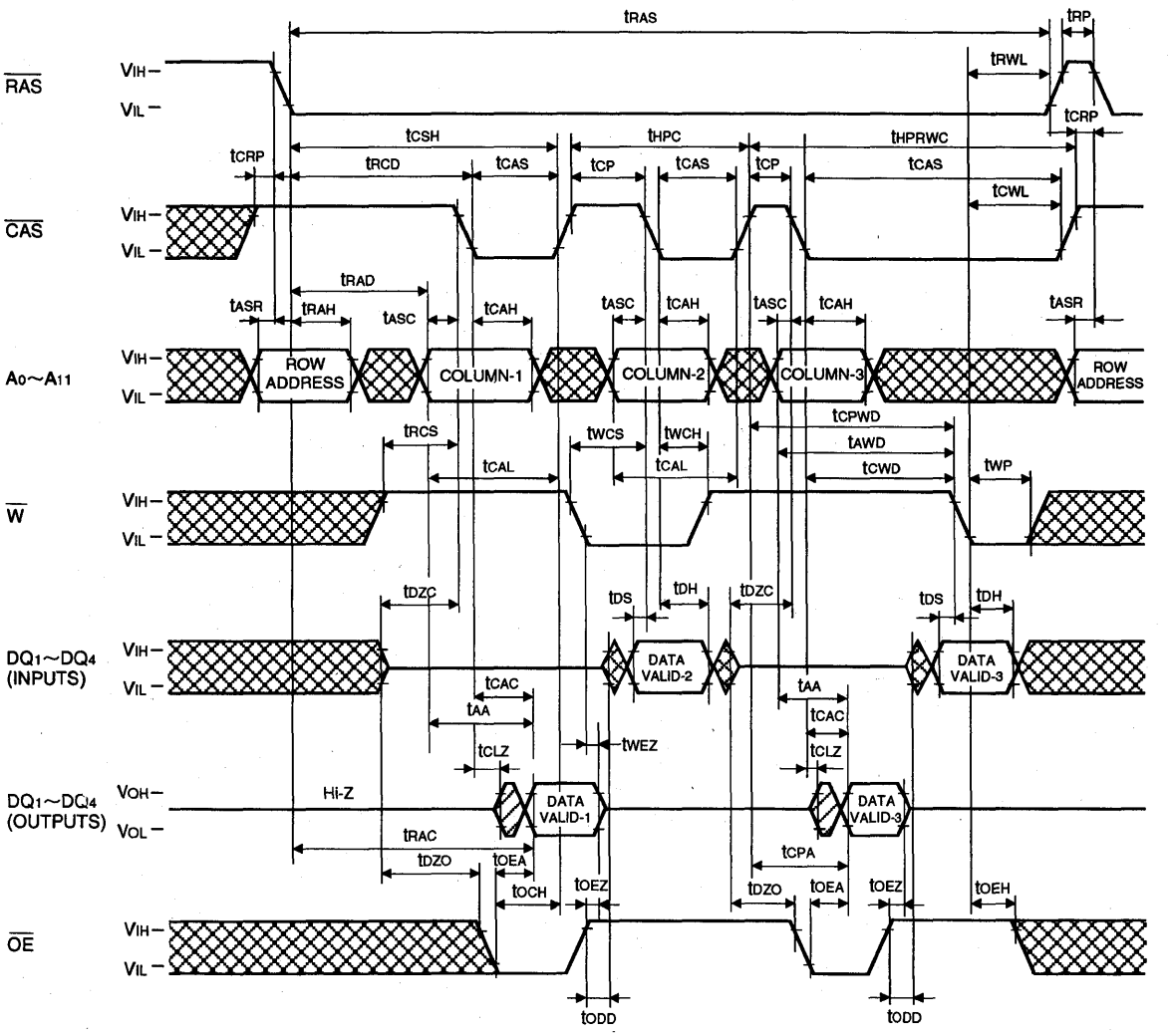
Hyper Page Mode Early Write Cycle



Hyper Page Mode Read-Write, Read-Modify-Write Cycle

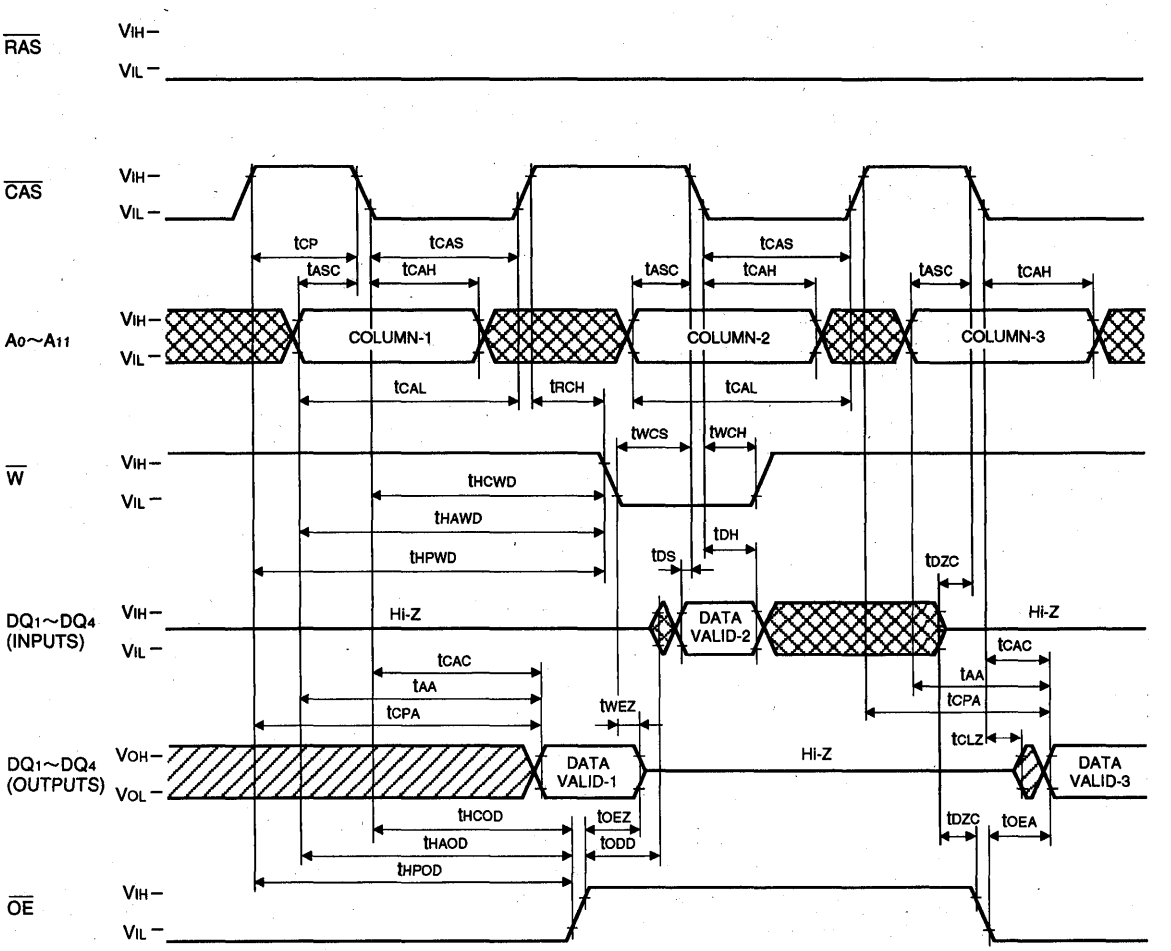


Hyper Page Mode Mix Cycle (1)



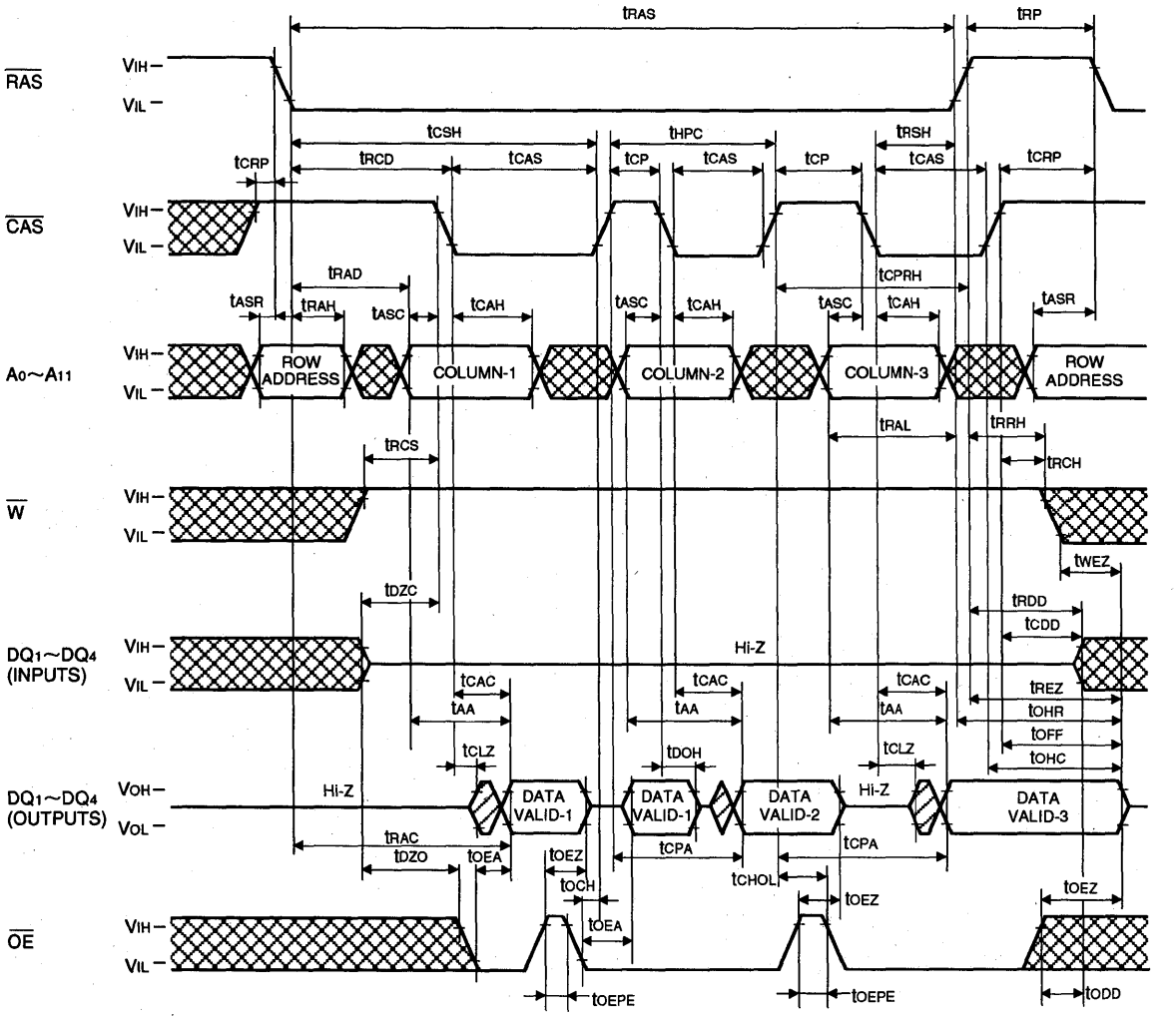
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (2)



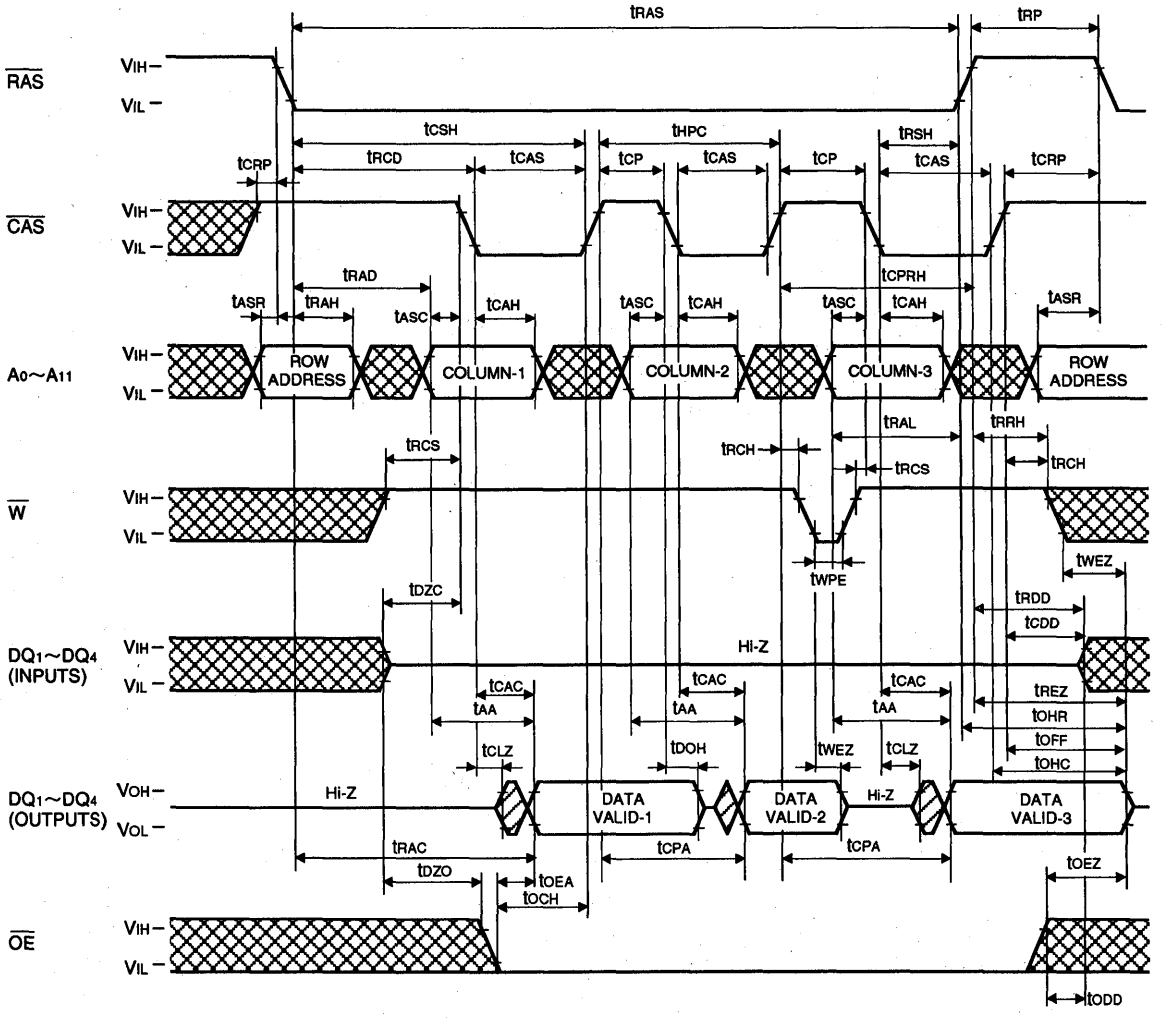
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



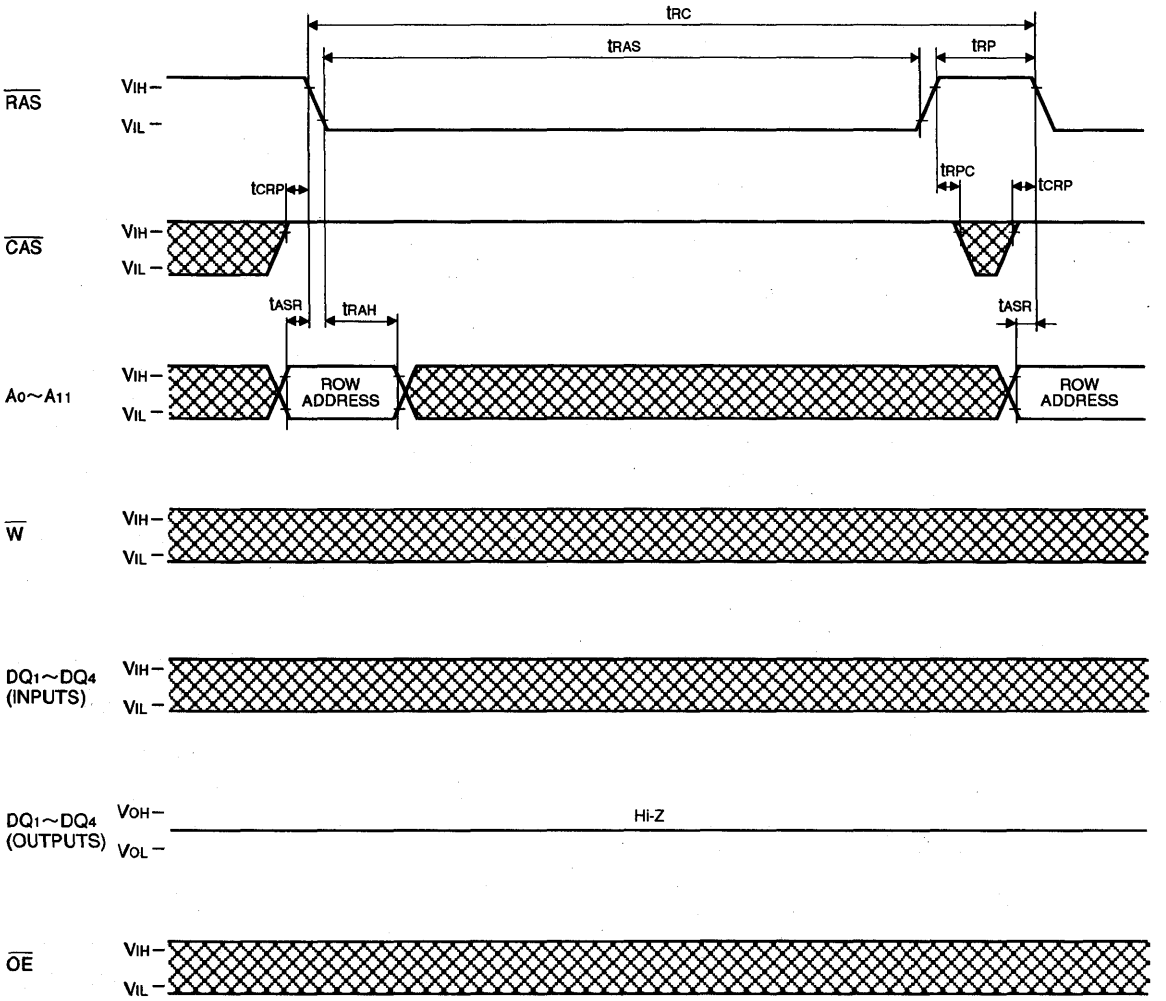
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

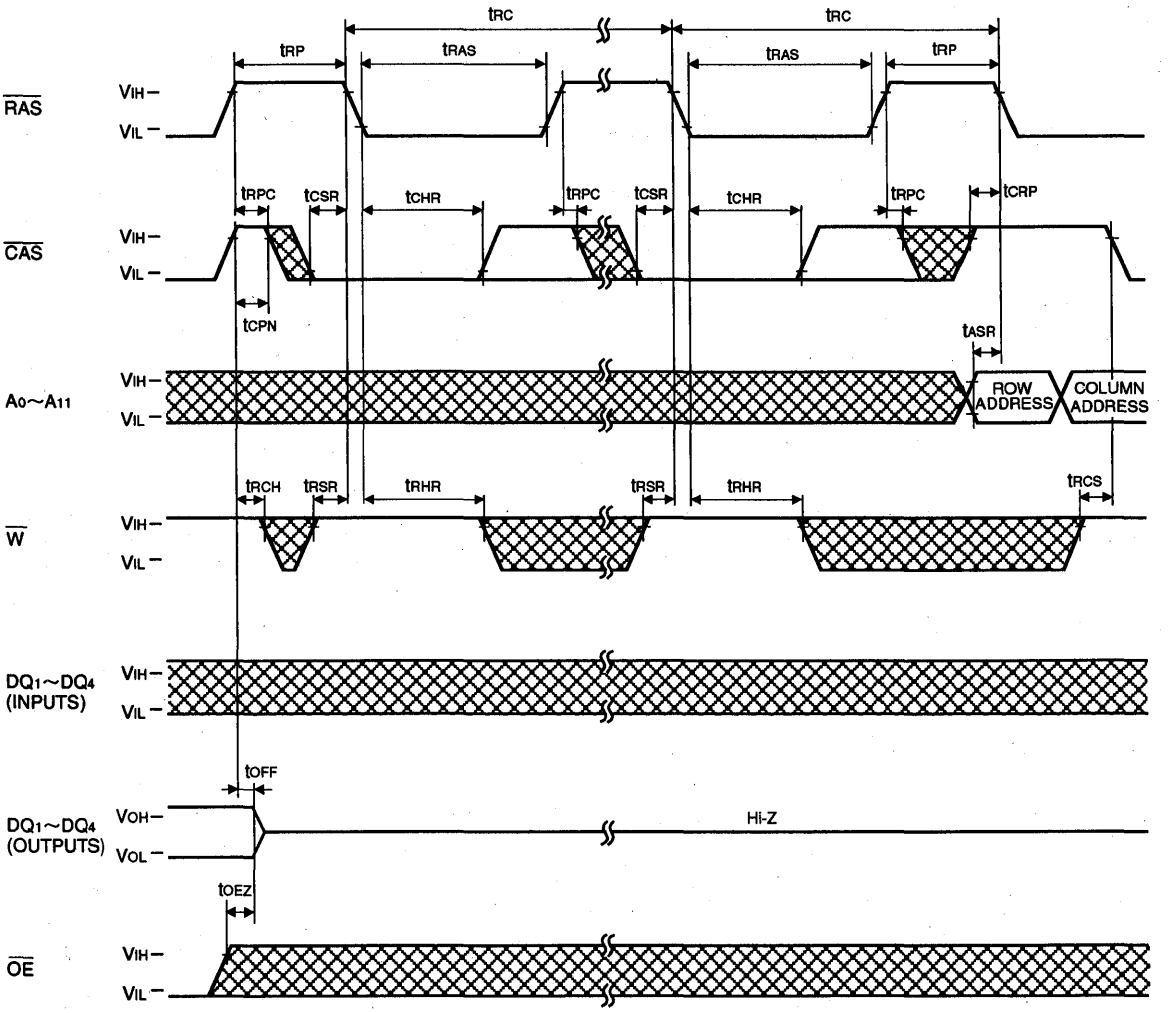


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

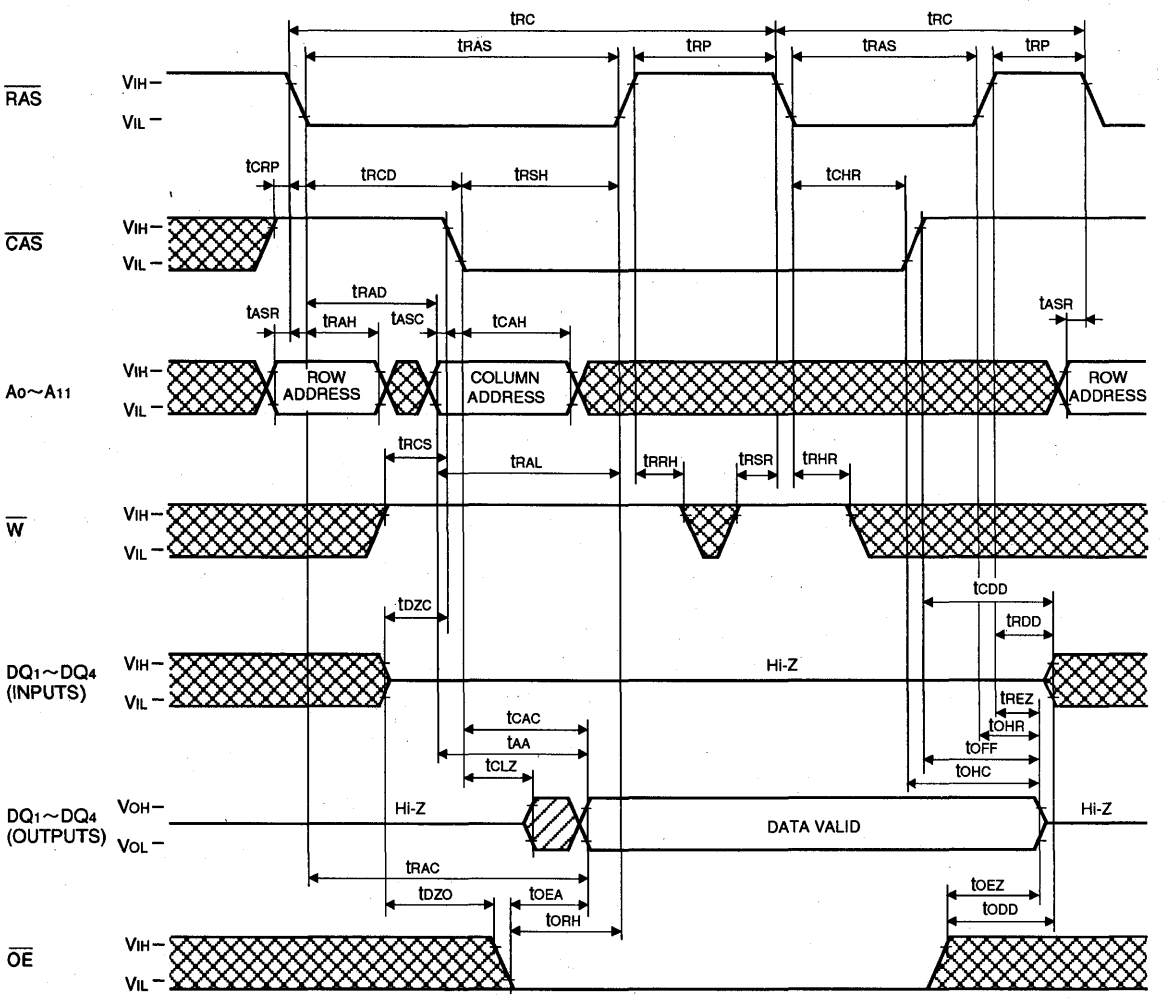
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

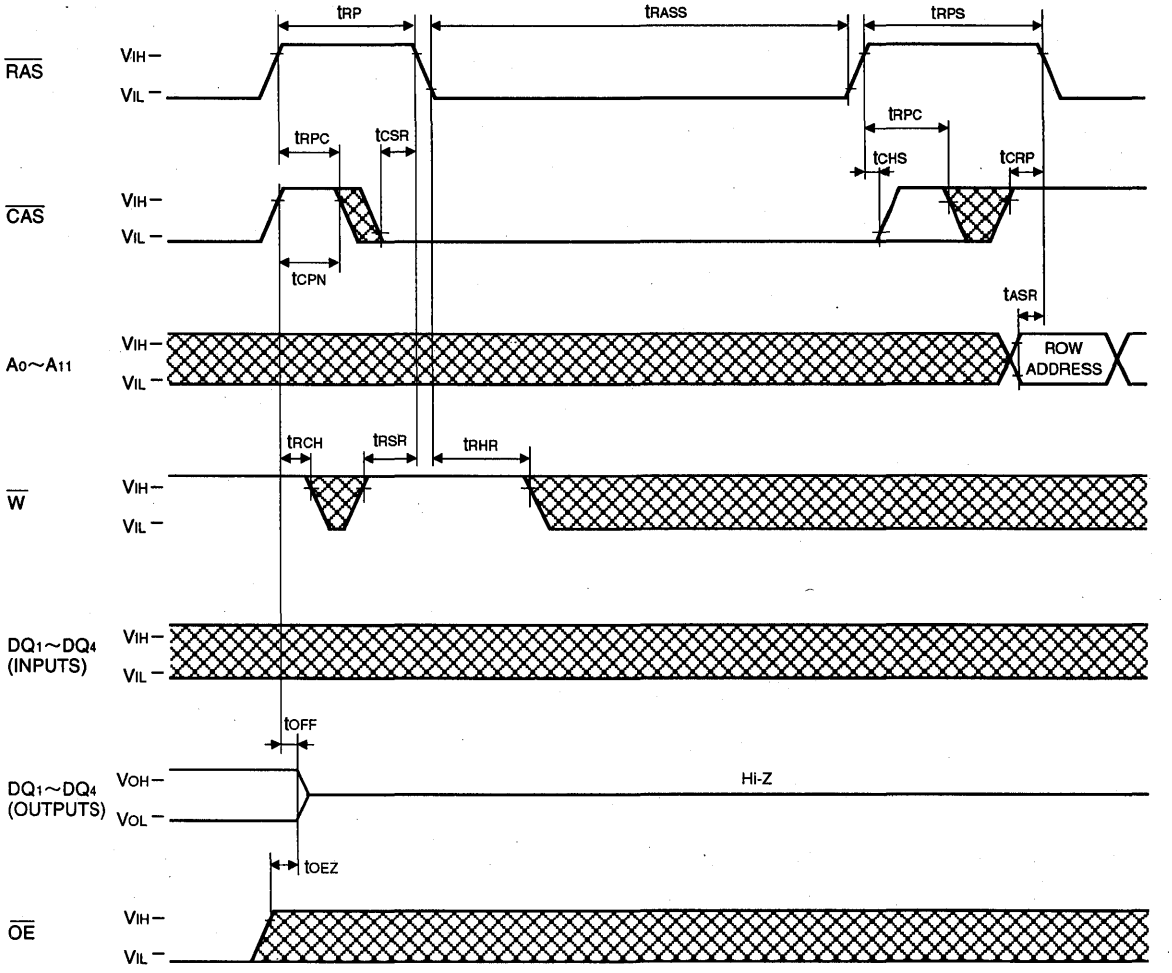


Hidden Refresh Cycle (Read) (Note 33)



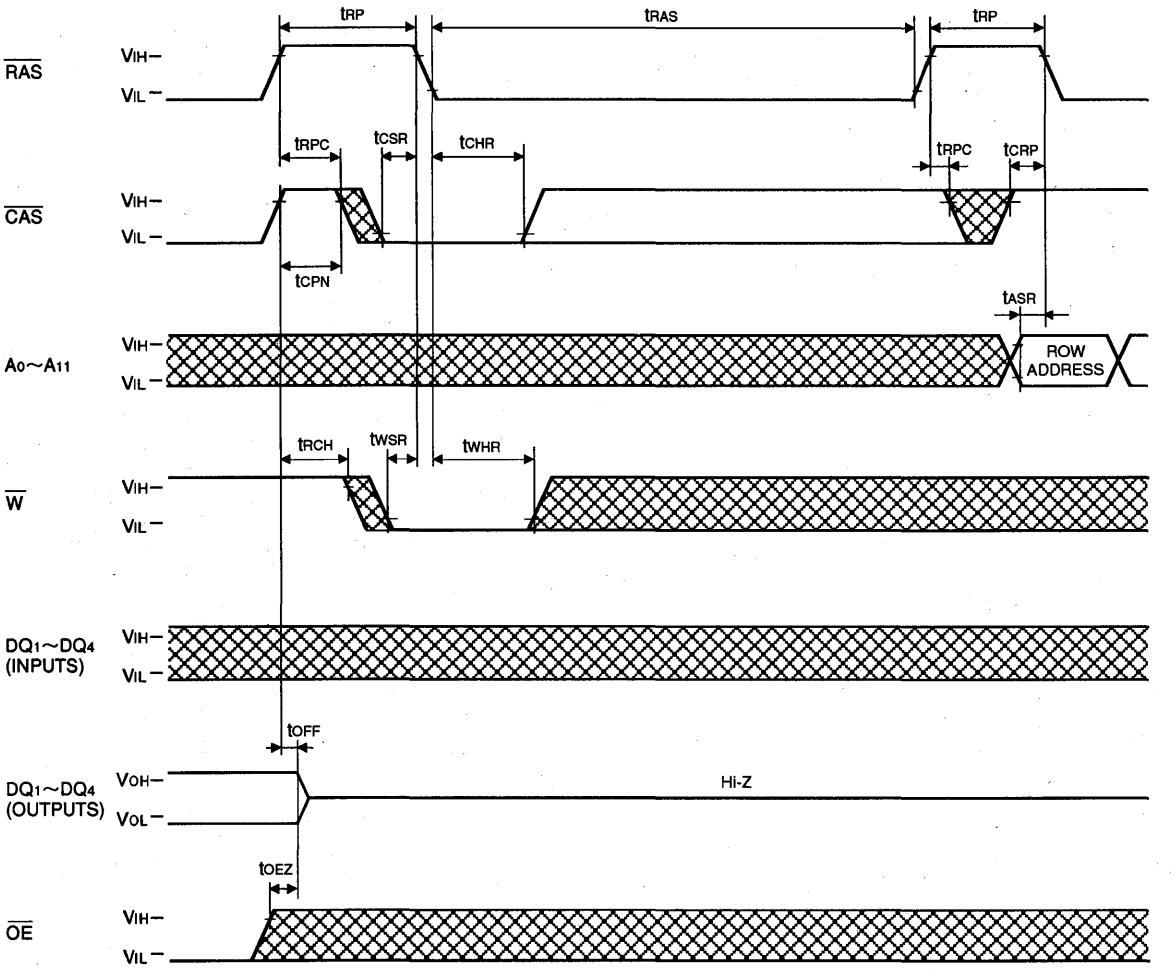
Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

M5M4V17400BJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17400BXX-6,-6S	60	15	30	15	110	360
M5M4V17400BXX-7,-7S	70	20	35	20	130	315

XX=J,TP

- Standard 26 pin SOJ, 26 pin TSOP
- Single 3.3V ±10%supply
- Low stand-by power dissipation
  - M5M4V17400B ····· 1.8mW (Max)CMOS Input level
  - M5M4V17400B(S) ····· 0.72mW (Max)CMOS Input level
- Low operating power dissipation
  - M5M4V17400Bxx- 6,- 6S ····· 435.0mW (Max)
  - M5M4V17400Bxx- 7,- 7S ····· 380.0mW (Max)

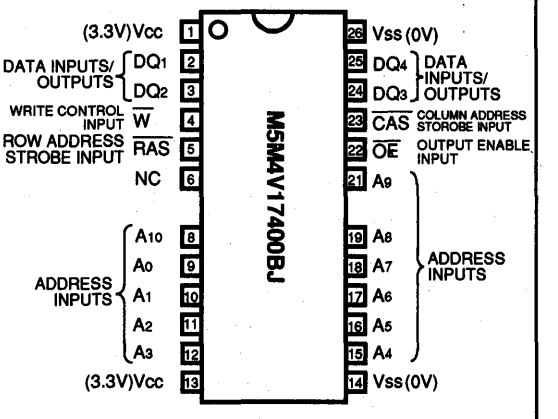
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh and Self refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0 ~A_{10})
- 2048 refresh cycles every 128ms (A_0 ~A_{10}) *

  * : Applicable to self refresh version only

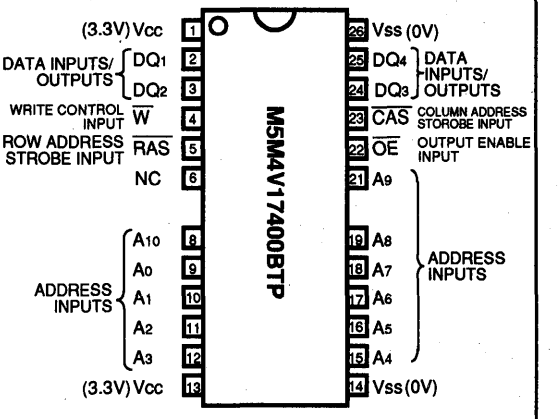
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D - B (300mil SOJ)



Outline 26P3D - E (300mil TSOP)

NC : NO CONNECTION

FUNCTION

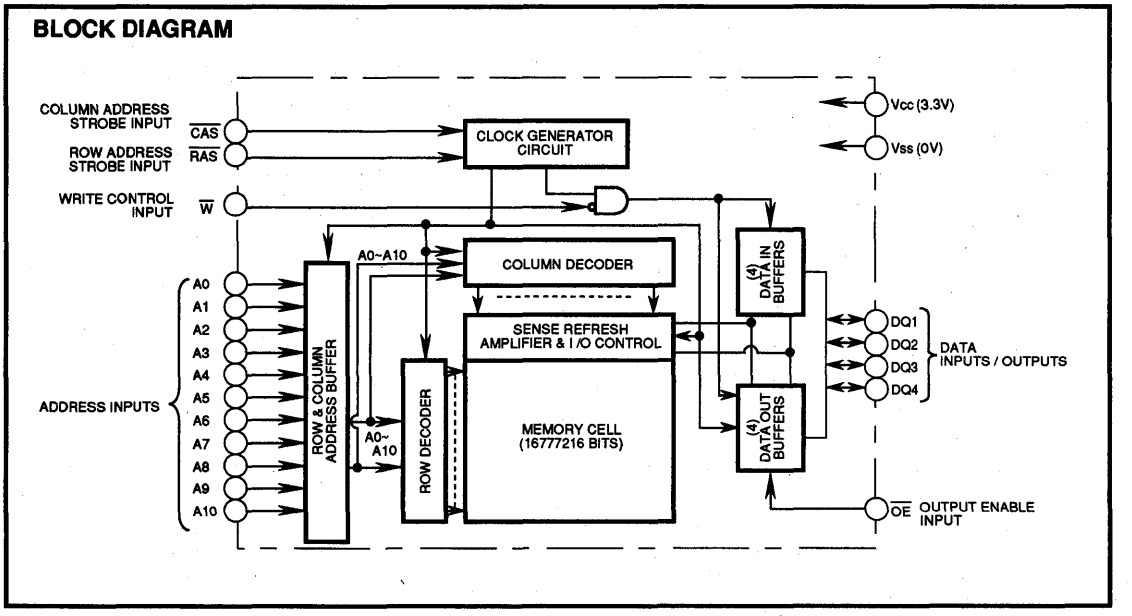
The M5M4V17400BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	Fast page mode identical
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5～4.6	V
V_I	Input voltage		-0.5～4.6	V
Vo	Output voltage		-0.5～4.6	V
Io	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4)	M5M4V17400B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M4V17400B-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V17400B	$\overline{RAS}$= $\overline{CAS}$=$\overline{OE}$=$\overline{W}$=A_0～A_{10}≧Vcc -0.2V output open			0.5	
		M5M4V17400B(S)				0.2	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3)	M5M4V17400B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			120	mA
		M5M4V17400B-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M4V17400B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			70	mA
		M5M4V17400B-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V17400B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M4V17400B-7,-7S				105	
I_{CC8}(AV)	Average supply current from Vcc Extended refresh (Note 5)	M5M4V17400B(S)	$\overline{RAS}$ cycling and $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling Vcc-0.2V≦$\overline{OE}$=$\overline{W}$=A_0～A_{10}≦0.2V output open, t_{RC}=64 μs, t_{RAS}=t_{RAS}min～1 μs			0.3	mA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M4V17400B(S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V, output open Vcc-0.2V≦$\overline{OE}$=W=A_0～A_{10}≦0.2V			0.2	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		60		70	ns
t_{AA}	Columu address access time	(Note 6,9)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	15	ns

Note 5: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to V_{OH}=2.4V (I_{OH}=-2mA) / V_{OL}=2mA(I_{OL}=2mA) loads and 100pF. The reference level for measuring of output signals are V_{OH}=2.0V and V_{OL}=0.8V .
7: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
8: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
9: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
10: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			32		32	ms
t_{REF}	Refresh cycle time *			128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note18)	15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note18)	15		15		ns
t_T	Transition time	(Note19)	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.
15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
17: Either t_{DZC} or t_{DZO} must be satisfied.
18: Either t_{CDD} or t_{ODD} must be satisfied.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note21)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note22)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note22)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note22)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits				Unit
			M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note24)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note25)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note22)	60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

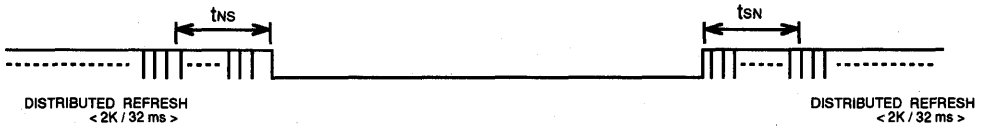
Self Refresh Cycle

Symbol	Parameter	Limits				Unit
		M5M4V17400B-6S		M5M4V17400B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

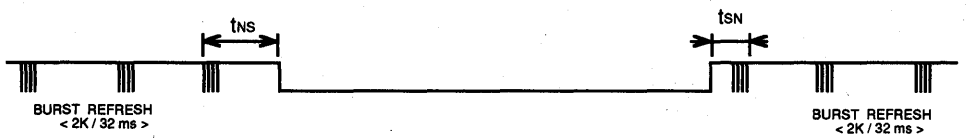
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leqq 32$ ms and $t_{SN} \leqq 32$ ms.



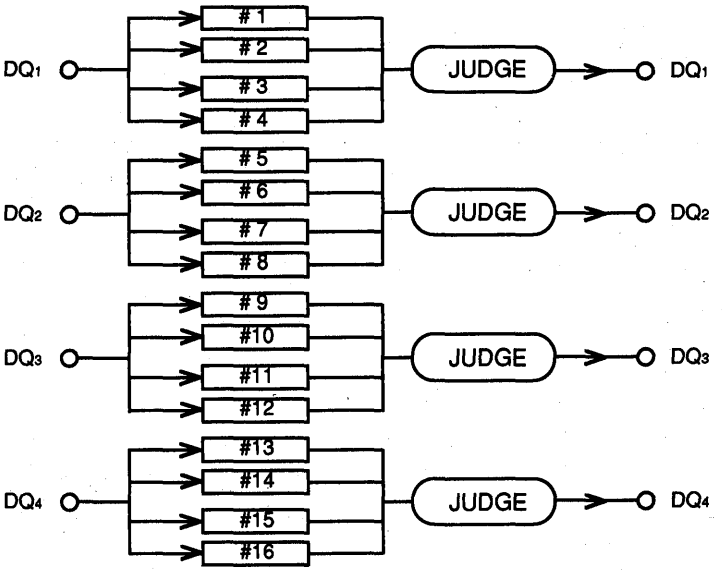
(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} + t_{SN} \leqq 32$ ms.

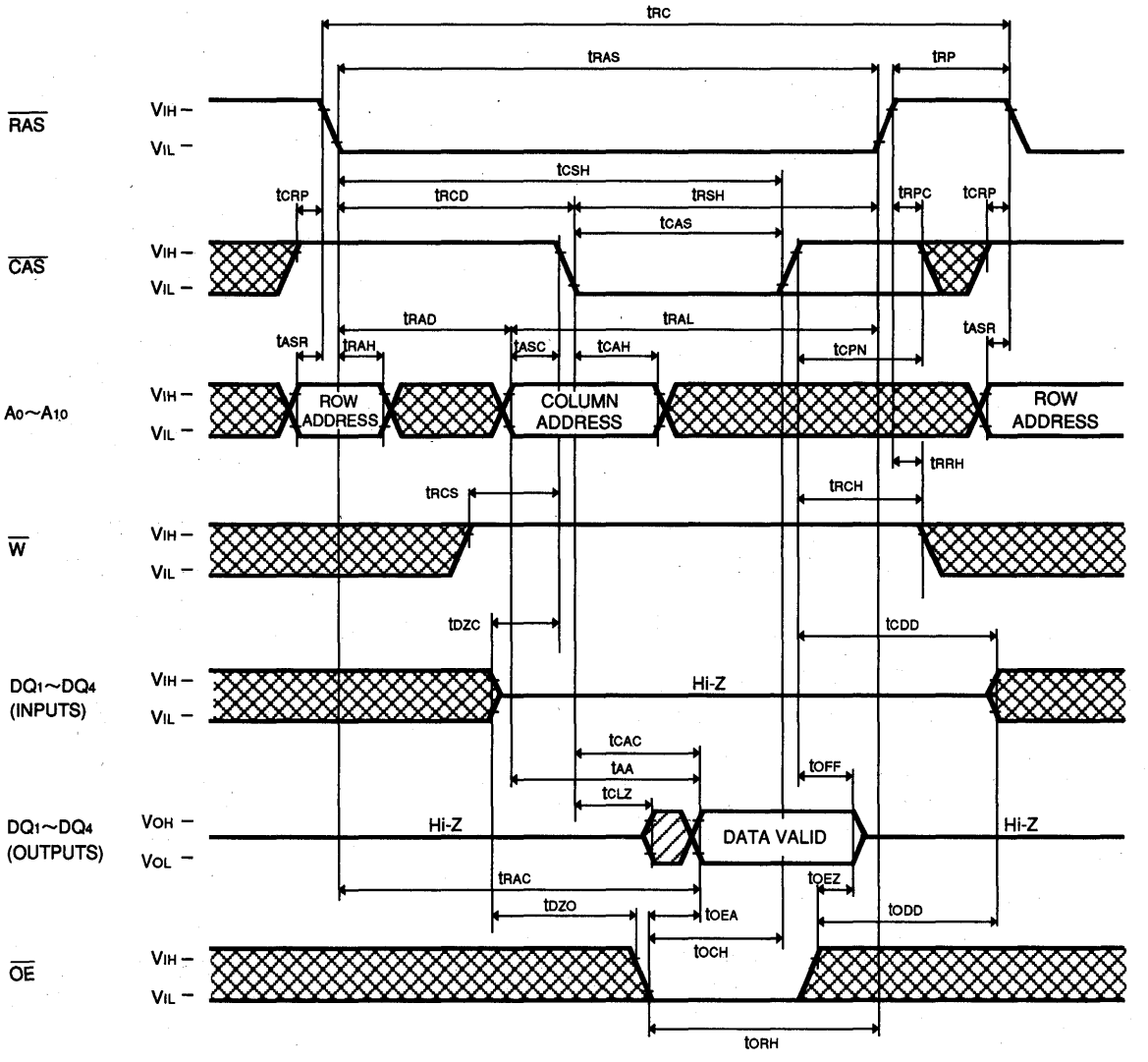


TEST Mode SET Cycle

Symbol	Parameter	Limits				Unit
		M5M4V17400B-6,-6S		M5M4V17400B-7,-7S		
		Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		15		ns



Timing Diagrams (Note 27)
Read Cycle

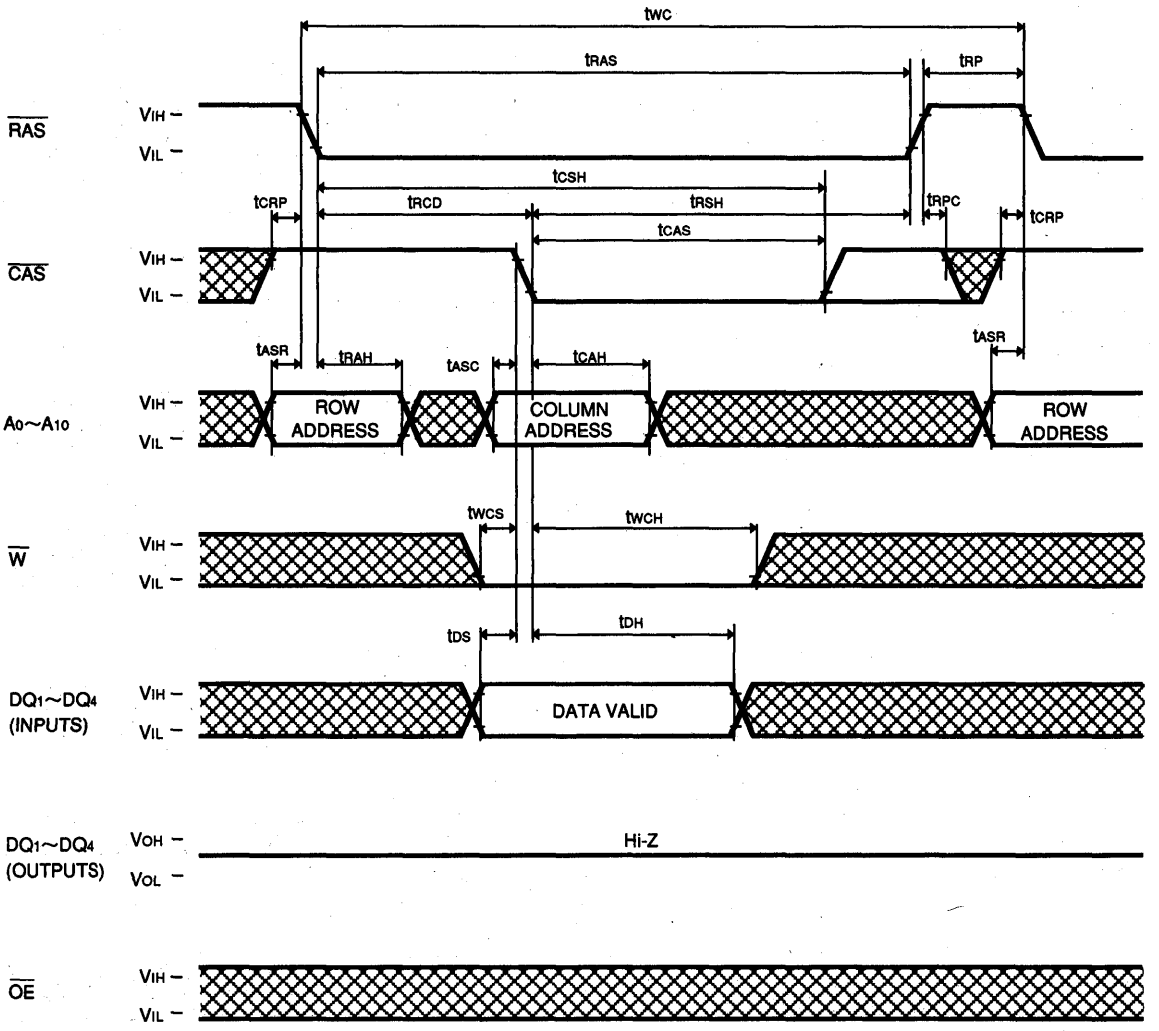


Note 27

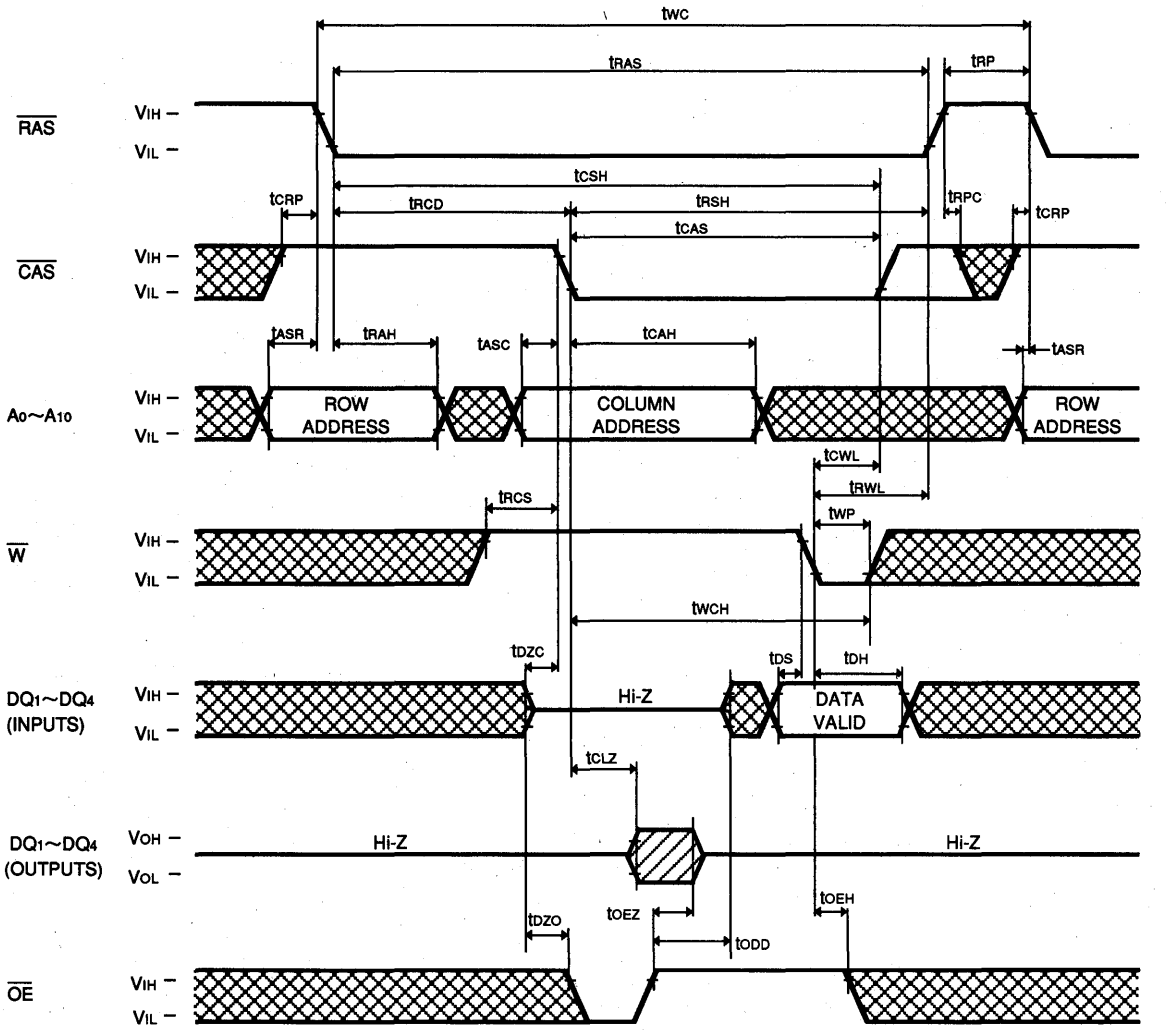
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

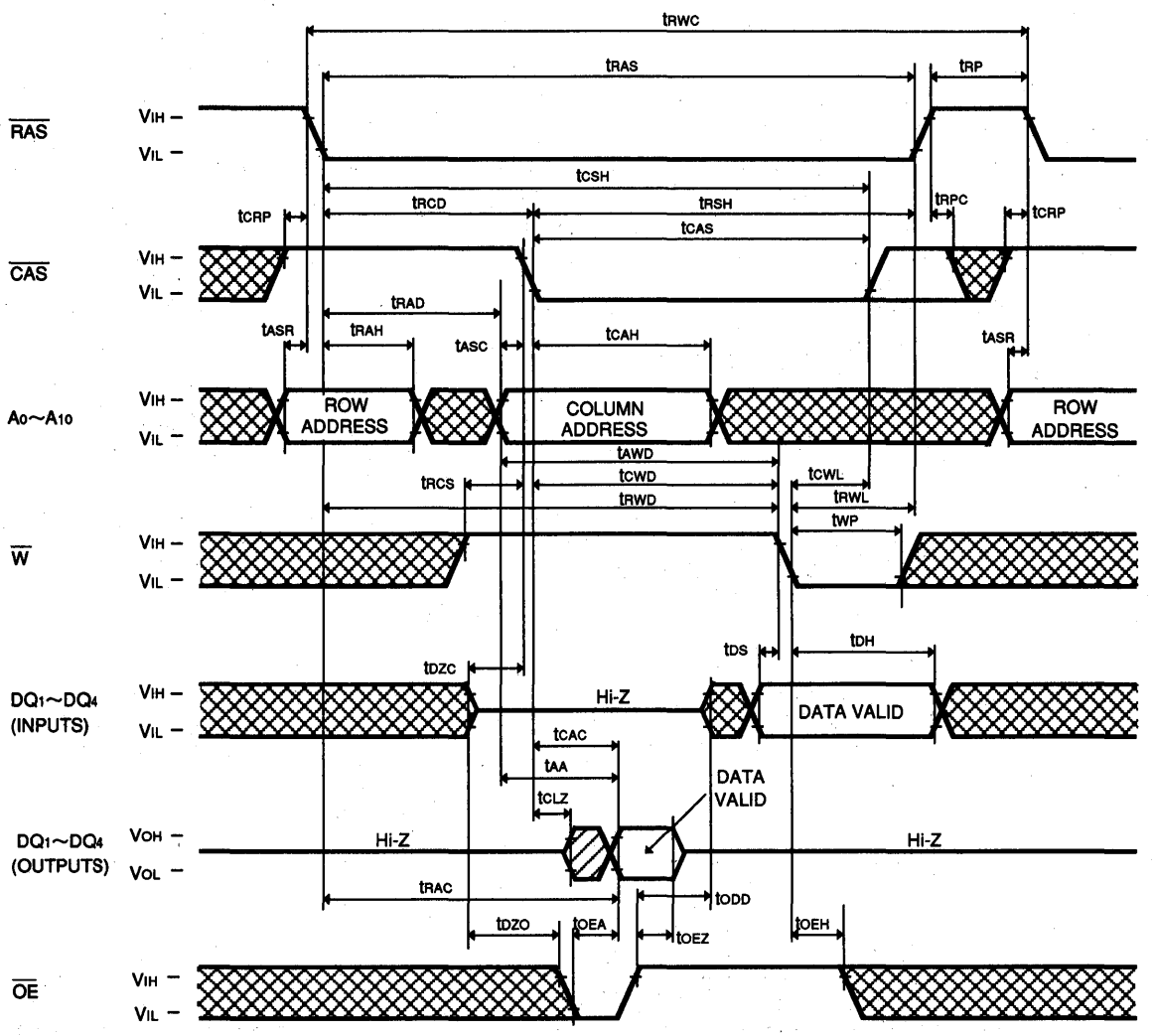
Write Cycle (Early write)



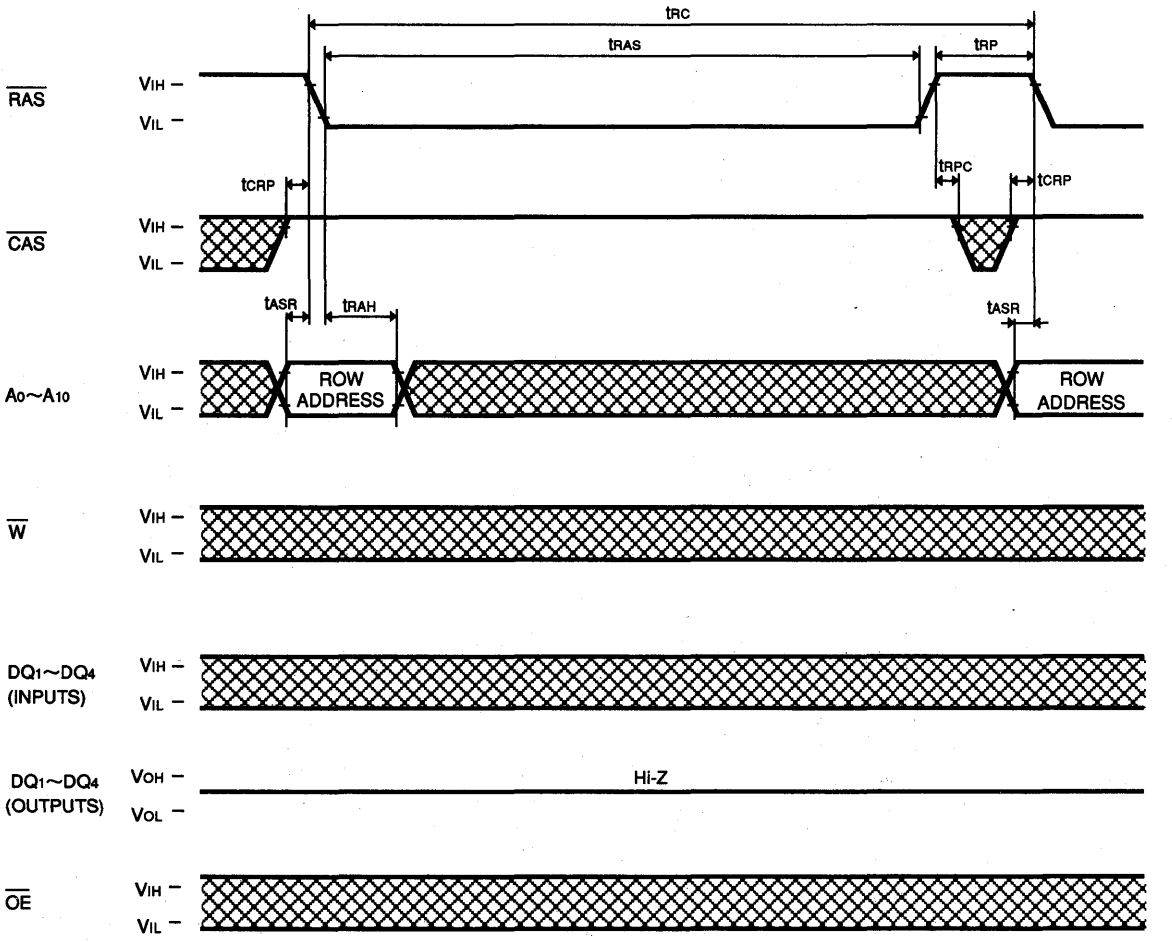
Write Cycle (Delayed write)



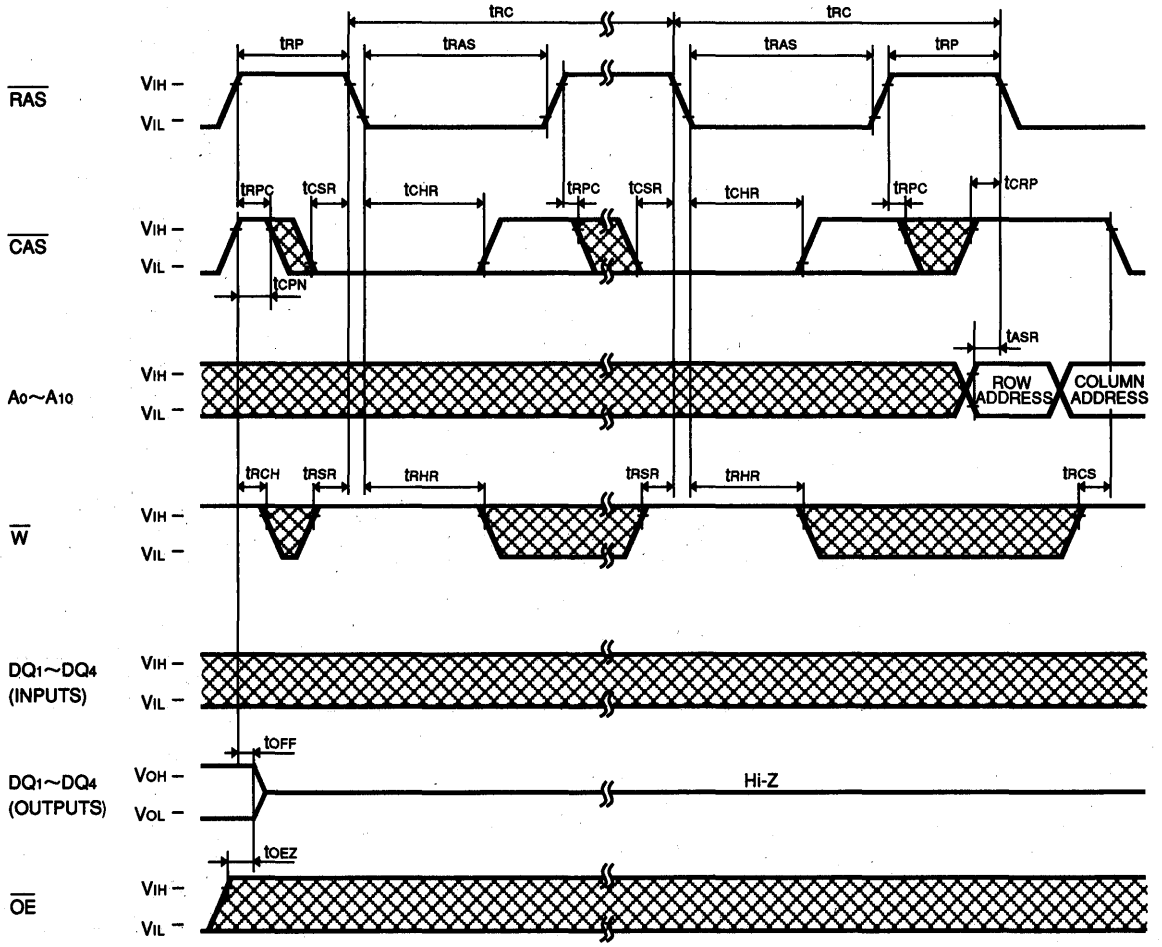
Read-Write, Read-Modify-Write Cycle



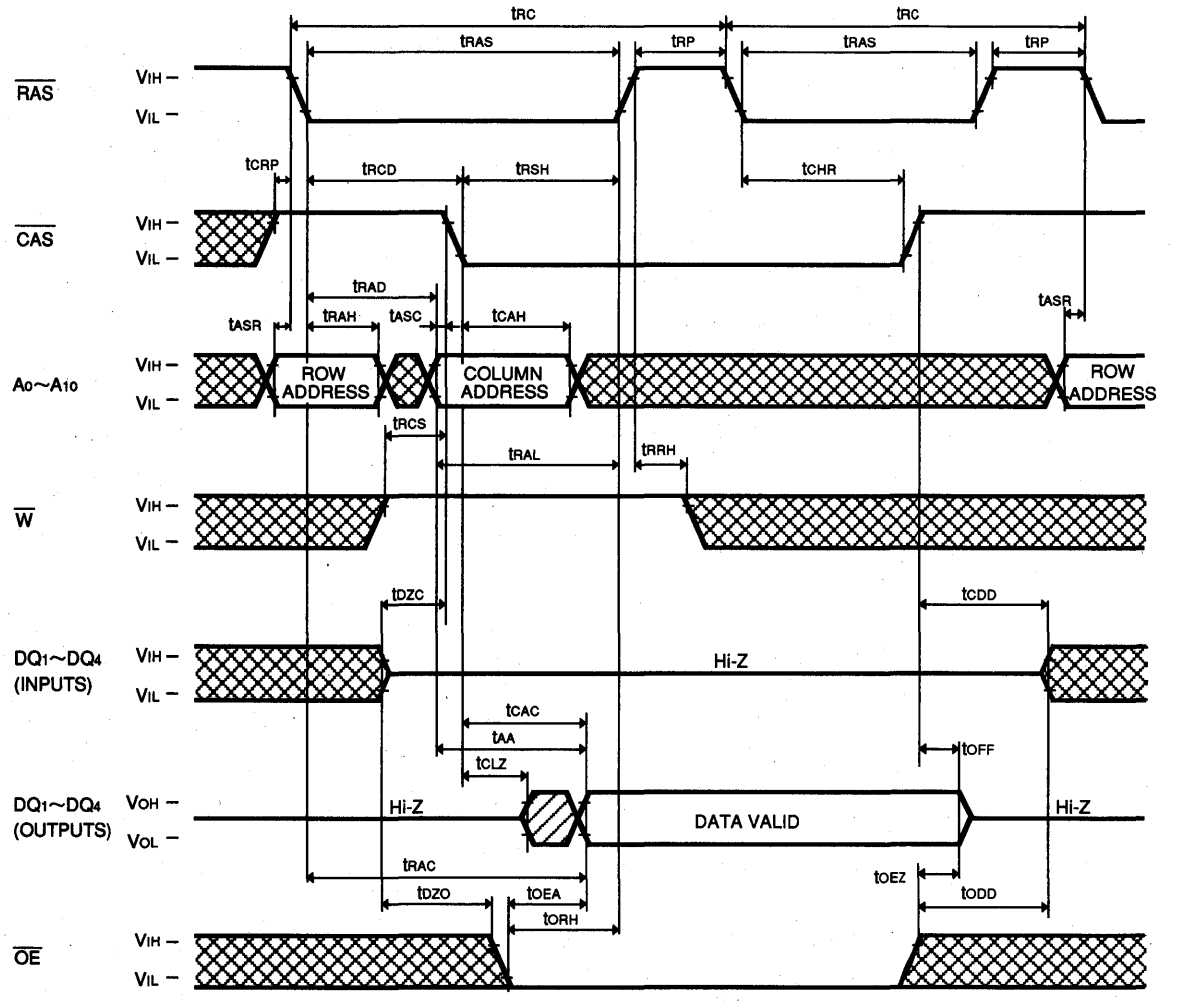
$\overline{RAS}$-only Refresh Cycle



CAS before RAS Refresh Cycle

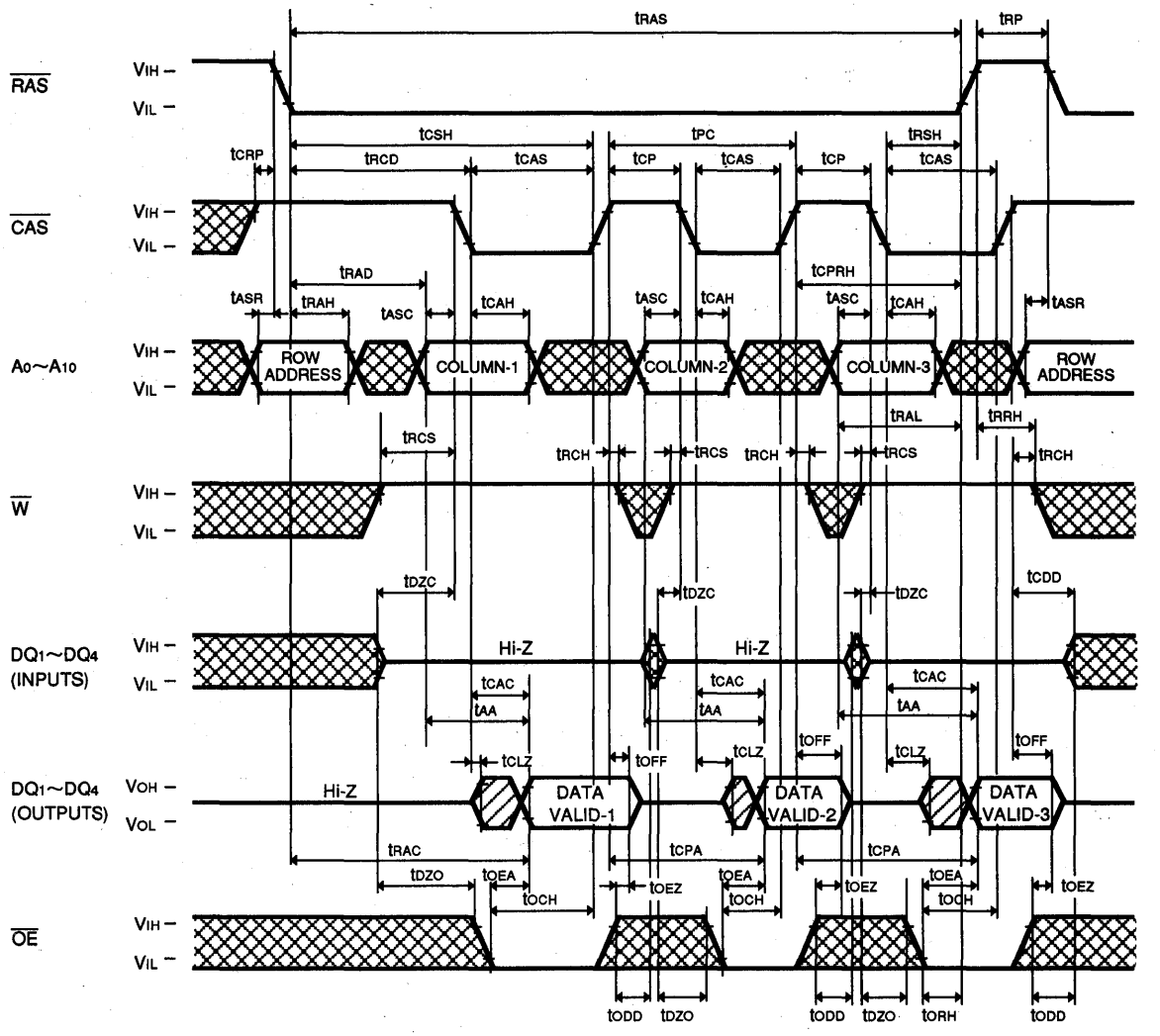


Hidden Refresh Cycle (Read) (Note 28)



Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



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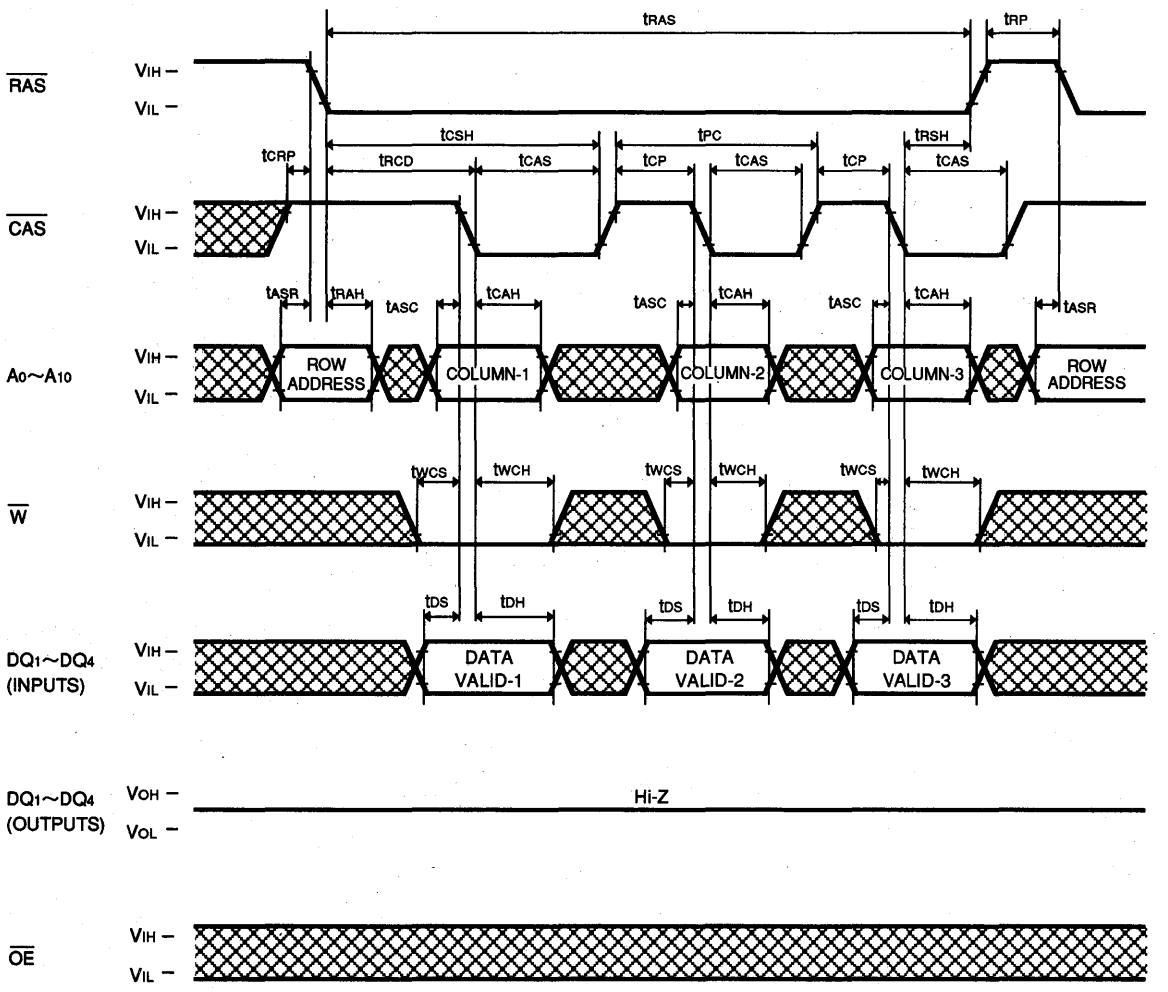
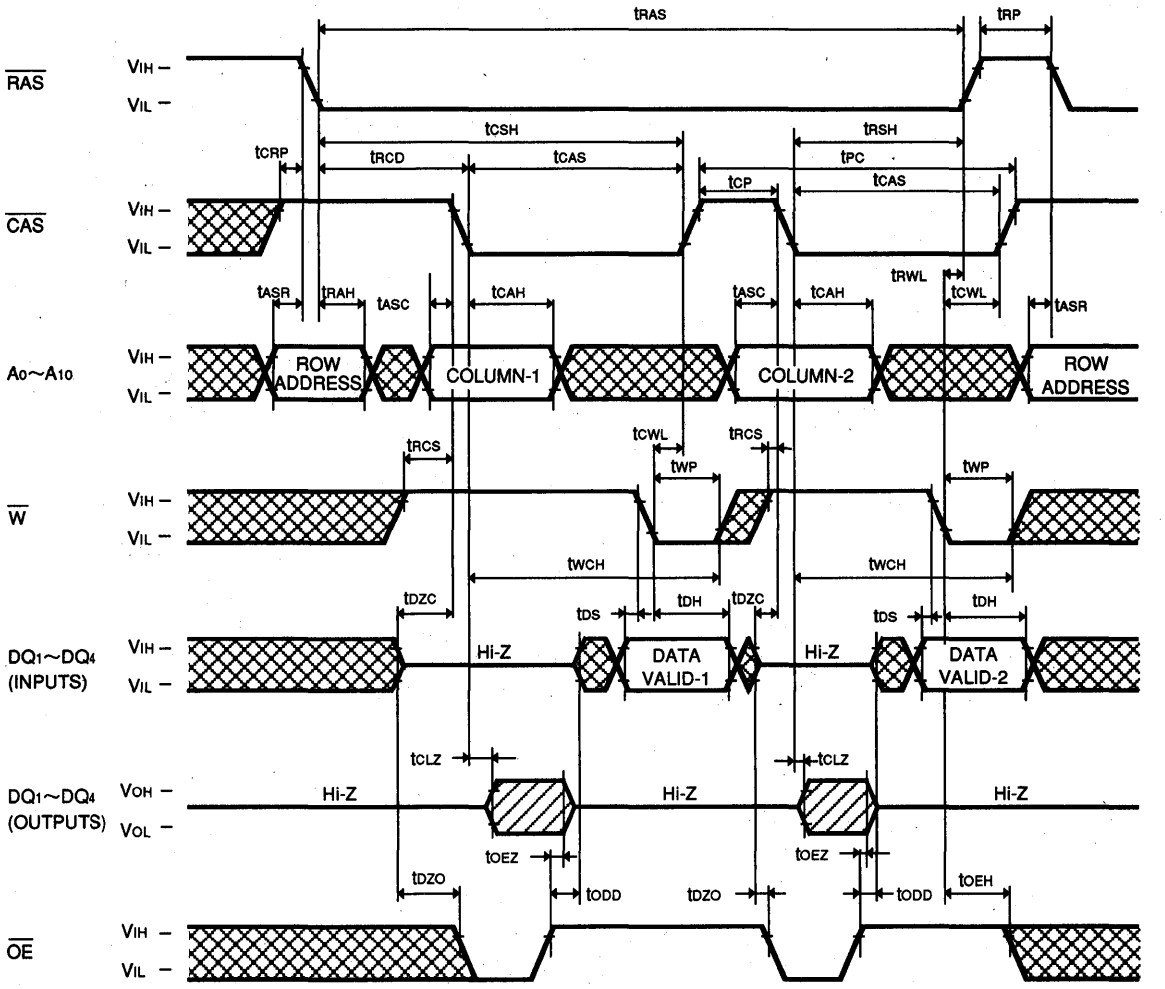
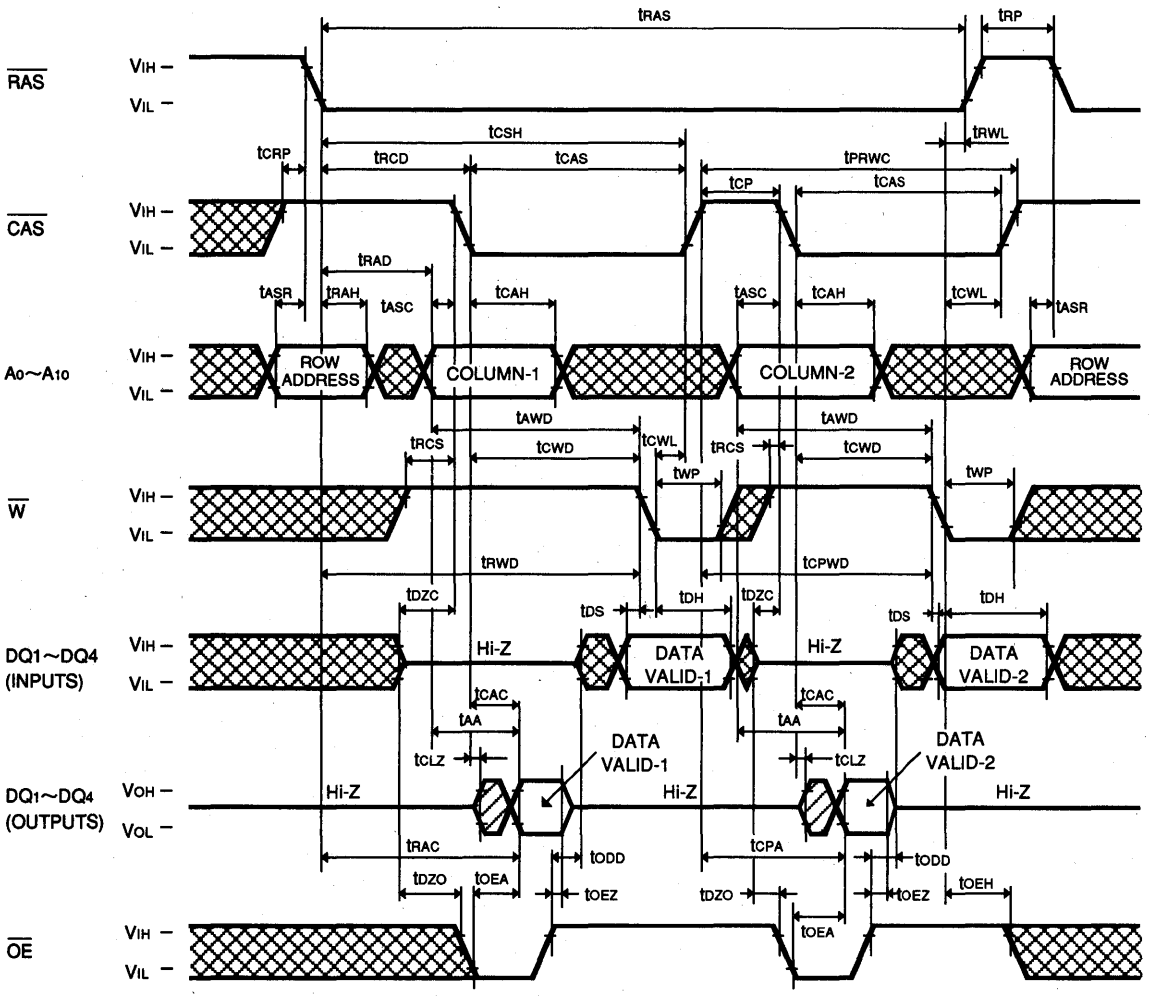
Fast Page Mode Write Cycle (Early Write)



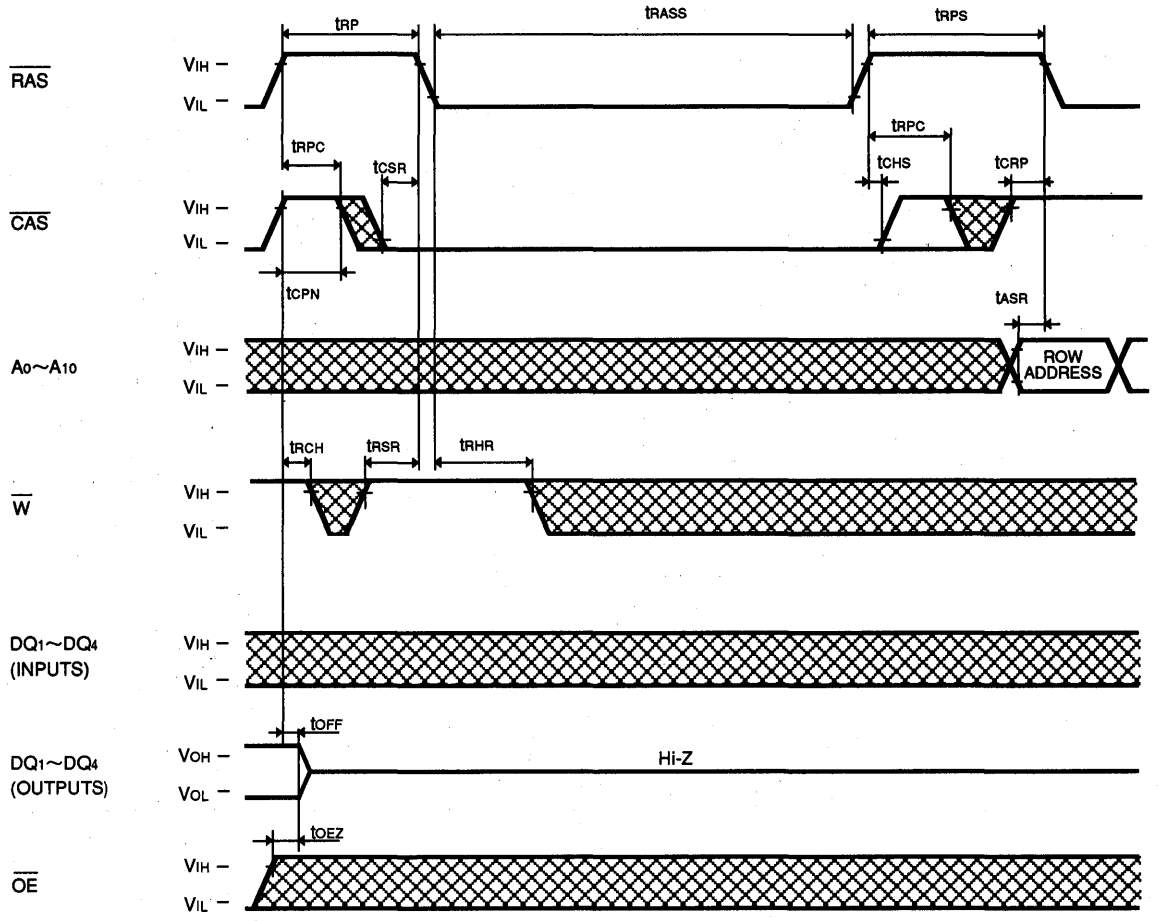
Fast-Page Mode Write Cycle (Delayed Write)



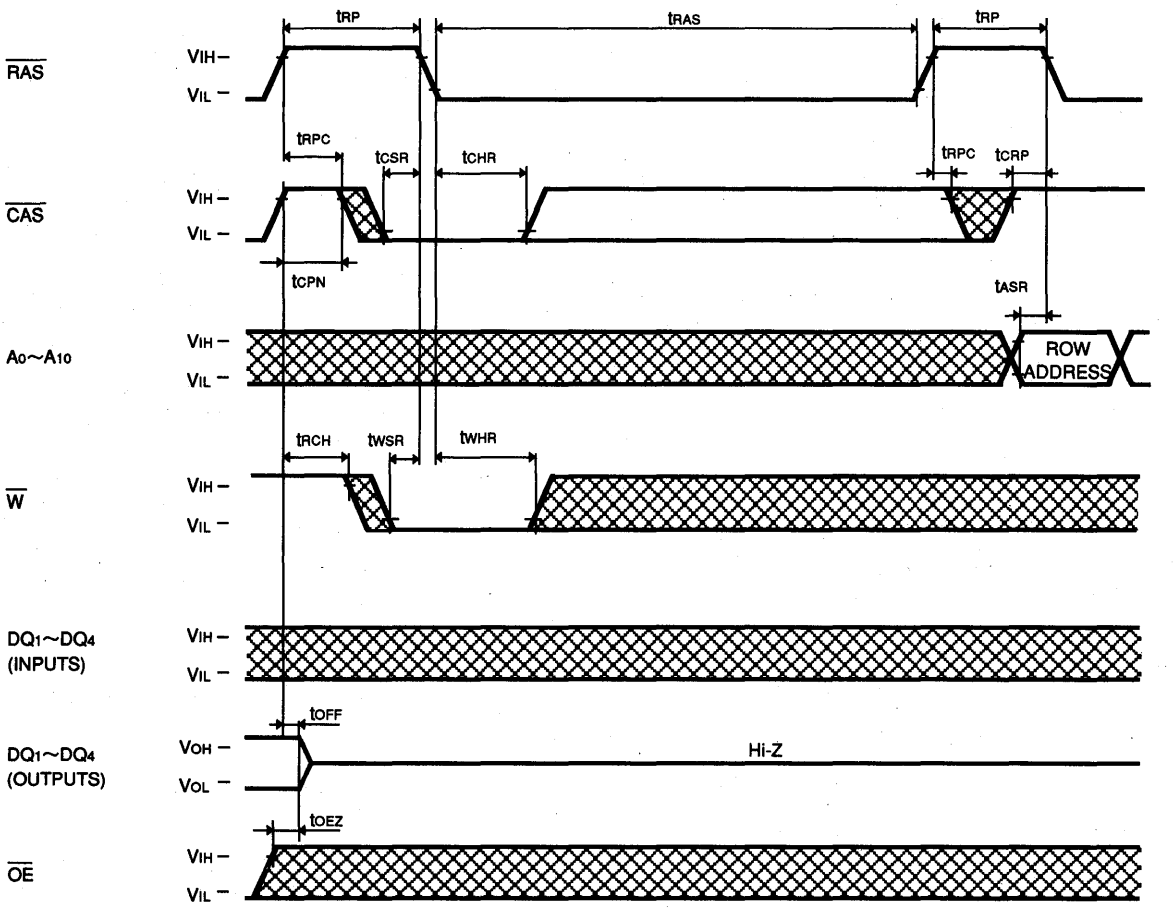
Fast Page Mode Read-Write,Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle (Note 29)



Note 29: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17400CXX-5,-5S	50	13	25	13	90	435
M5M4V17400CXX-6,-6S	60	15	30	15	110	360
M5M4V17400CXX-7,-7S	70	20	35	20	130	315

XX=J,TP

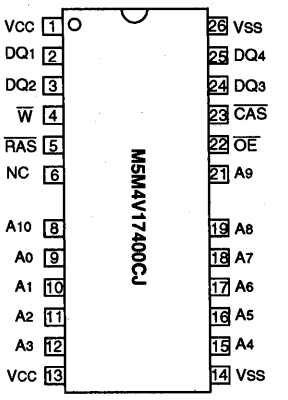
- Standard 26pin SOJ, 26pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.8mW (Max) ---------- CMOS Input level
  - 0.72mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M4V17400Cxx-5,-5S ---------- 525.0mW (Max)
  - M5M4V17400Cxx-6,-6S ---------- 435.0mW (Max)
  - M5M4V17400Cxx-7,-7S ---------- 380.0mW (Max)
- Self refresh capability *
  - self refresh current ---------- 200.0 μA(Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

*Applicable to self refresh version(M5M4V17400CJ,TP-5S,-6S,-7S :option) only

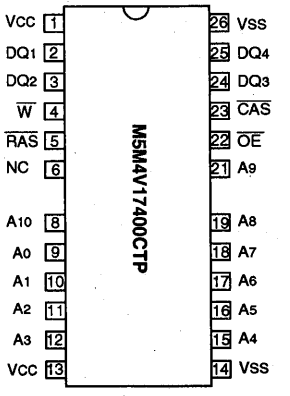
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

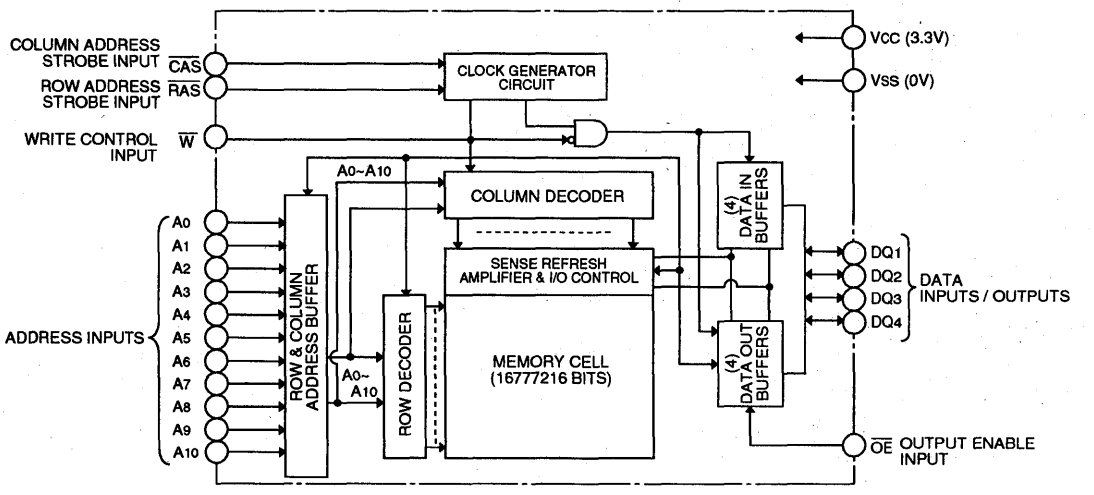
The M5M4V17400CJ, TP provide, in addition to normal read,write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5 ~4.6	V
V_I	Input voltage		-0.5 ~4.6	V
V_O	Output voltage		-0.5 ~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0 ~70	℃
T_{stg}	Storage temperature		-65 ~ 150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to VSS.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from V_{CC}, operating (Note 3,4)	M5M4V17400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M4V17400C-6,-6S				120	
		M5M4V17400C-7,-7S				105	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V			0.5	
I_{CC3} (AV)	Average supply current from V_{CC}, refreshing (Note 3)	M5M4V17400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M4V17400C-6,-6S				120	
		M5M4V17400C-7,-7S				105	
I_{CC4}(AV)	Average supply current from V_{CC}, Fast-Page-Mode (Note 3,4)	M5M4V17400C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V17400C-6,-6S				70	
		M5M4V17400C-7,-7S				60	
I_{CC6}(AV)	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V17400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M4V17400C-6,-6S				120	
		M5M4V17400C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=3.3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.

6:Measured with a load circuit equivalent to 2TTL loads and 100pF. The reference levels for measuring of output signals are 2.0V (VOH) and 0.8V (VOL).

7:Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max).

8:Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9:Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).

10:Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).

11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦ |±10 μ A |) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V ±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.

13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).

15:tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

16:tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

17:Either tDZC or tDZO must be satisfied.

18:Either tCDD or tODD must be satisfied.

19:tT is measured between VIH(min) and VIL(max).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	M5M4V17400C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$ ≦0.2V $\overline{OE}$&$\overline{WE}$ ≦0.2V or $\overline{OE}$&$\overline{WE}$ ≧Vcc-0.2V A_0 ~ A_{10} ≦0.2V or A_0 ~ A_{10} ≧Vcc-0.2V t_{REF}=128ms (2048cycles) output = OPEN t_{RAS}=t_{RAS}min. ~1 μs			500	μA
I_{CC9} (AV)	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M4V17400C (S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

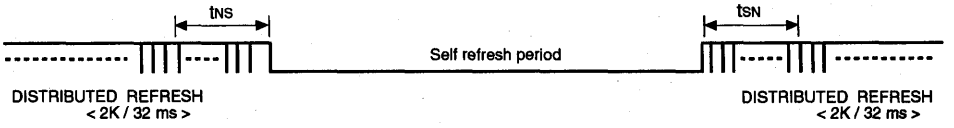
TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M4V17400C-5S		M5M4V17400C-6S		M5M4V17400C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

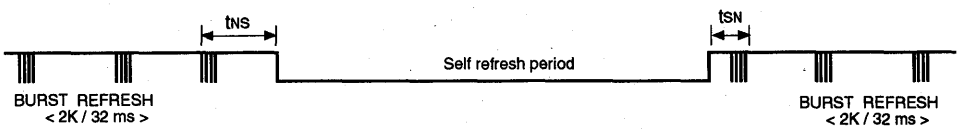
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦32ms and t_{SN}≦32ms.



(2) In case of burst refresh

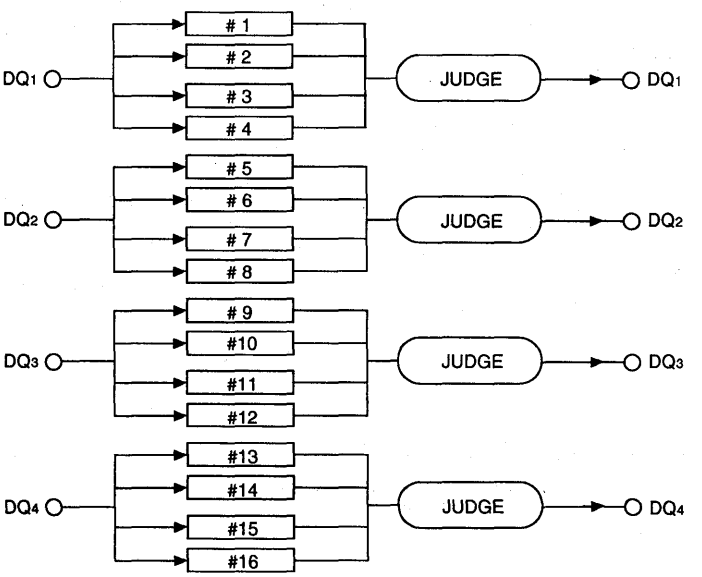
The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}+t_{SN}≦32ms.



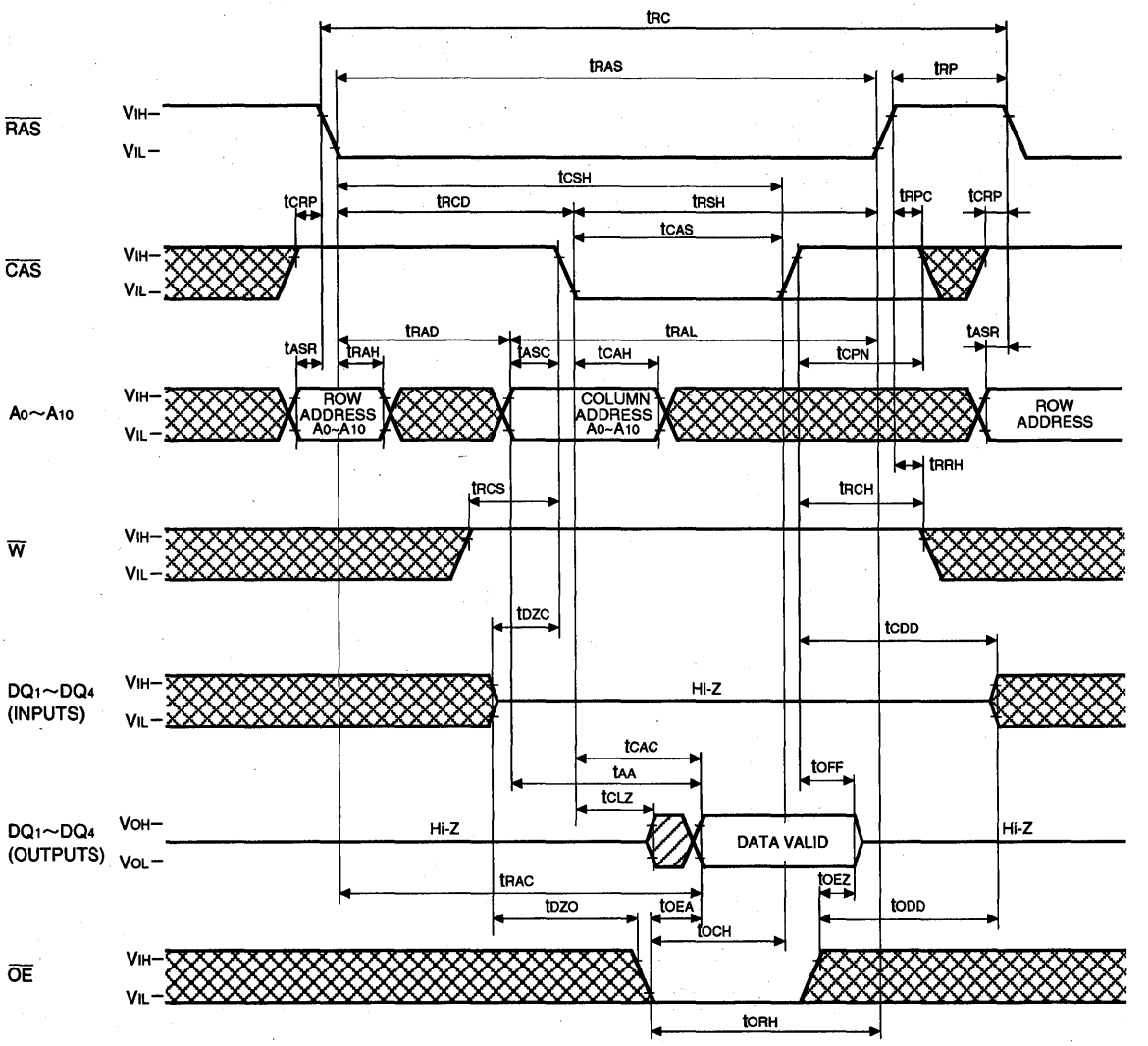
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M4V17400C-5,-5S		M5M4V17400C-6,-6S		M5M4V17400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA0 and CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 28)
Read Cycle



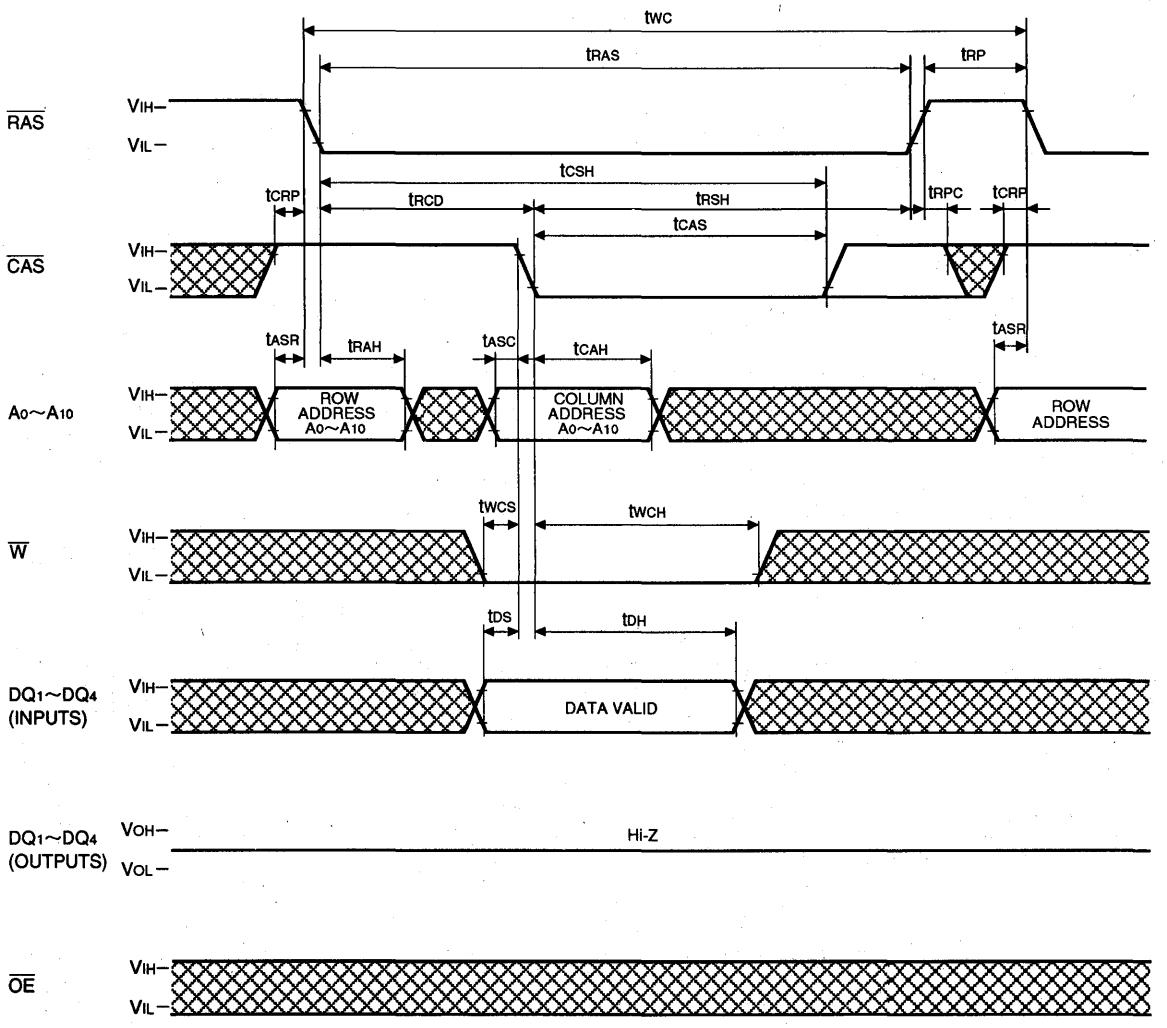
Note 28

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

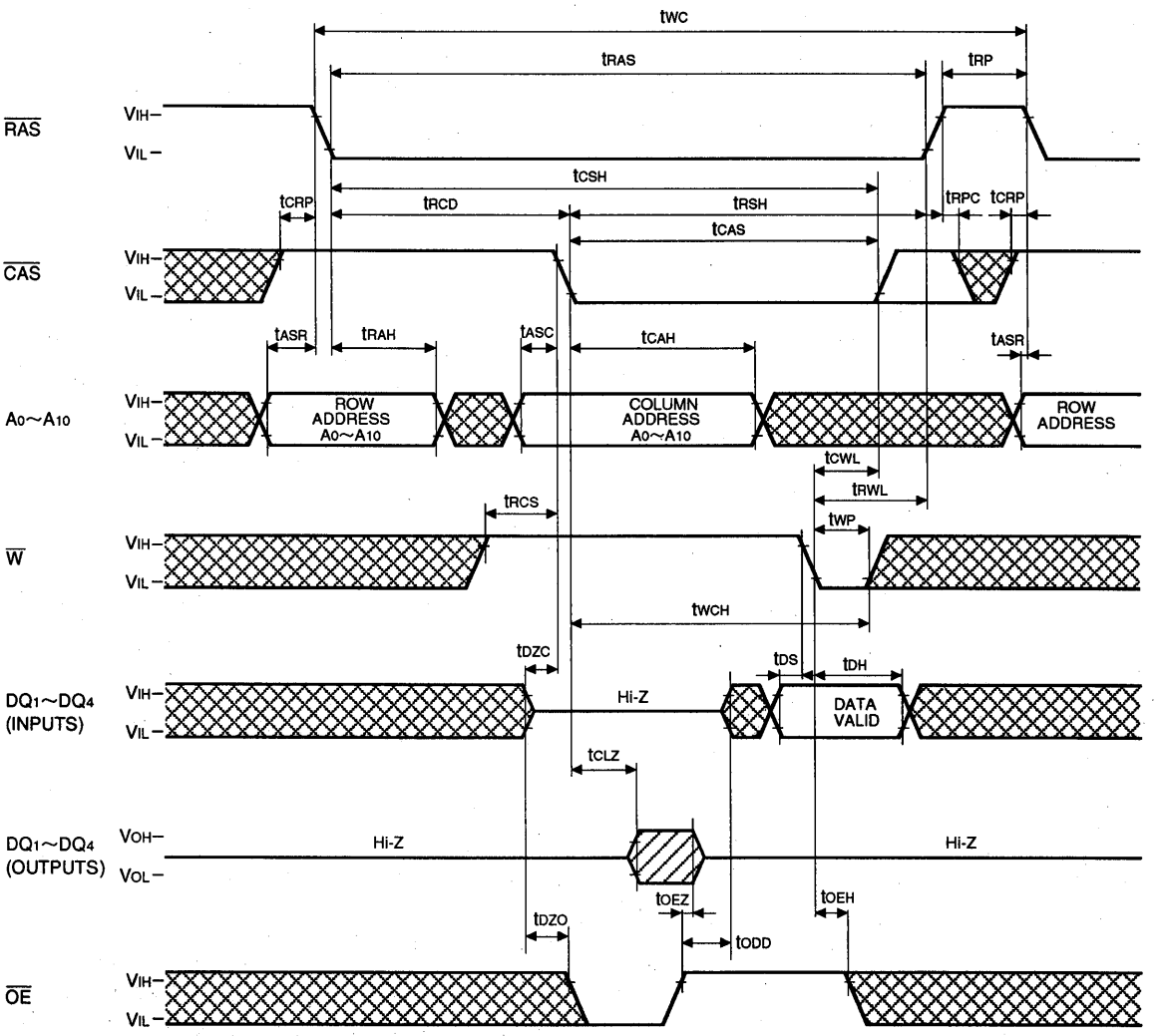
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early write)

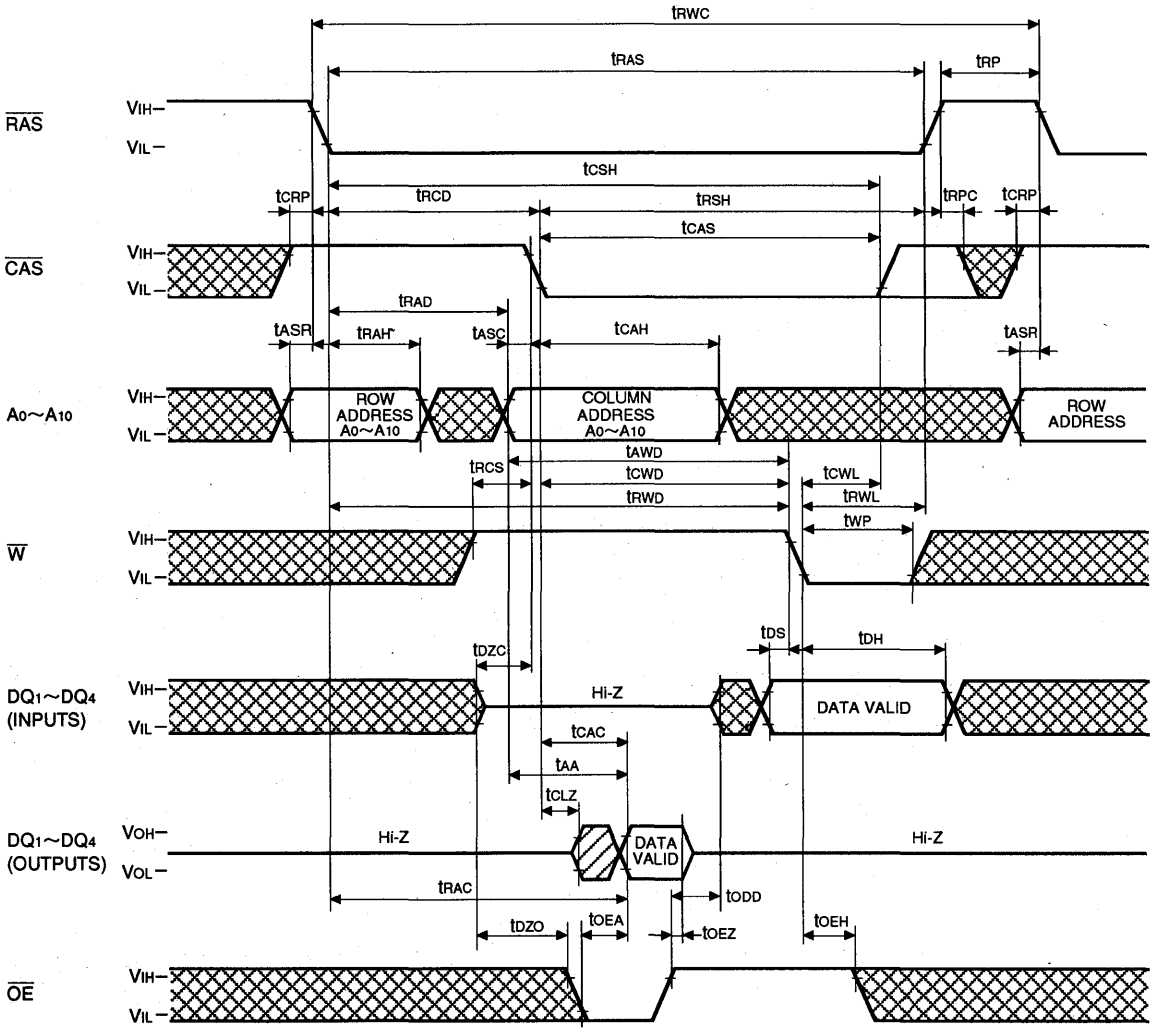


Write Cycle (Delayed write)



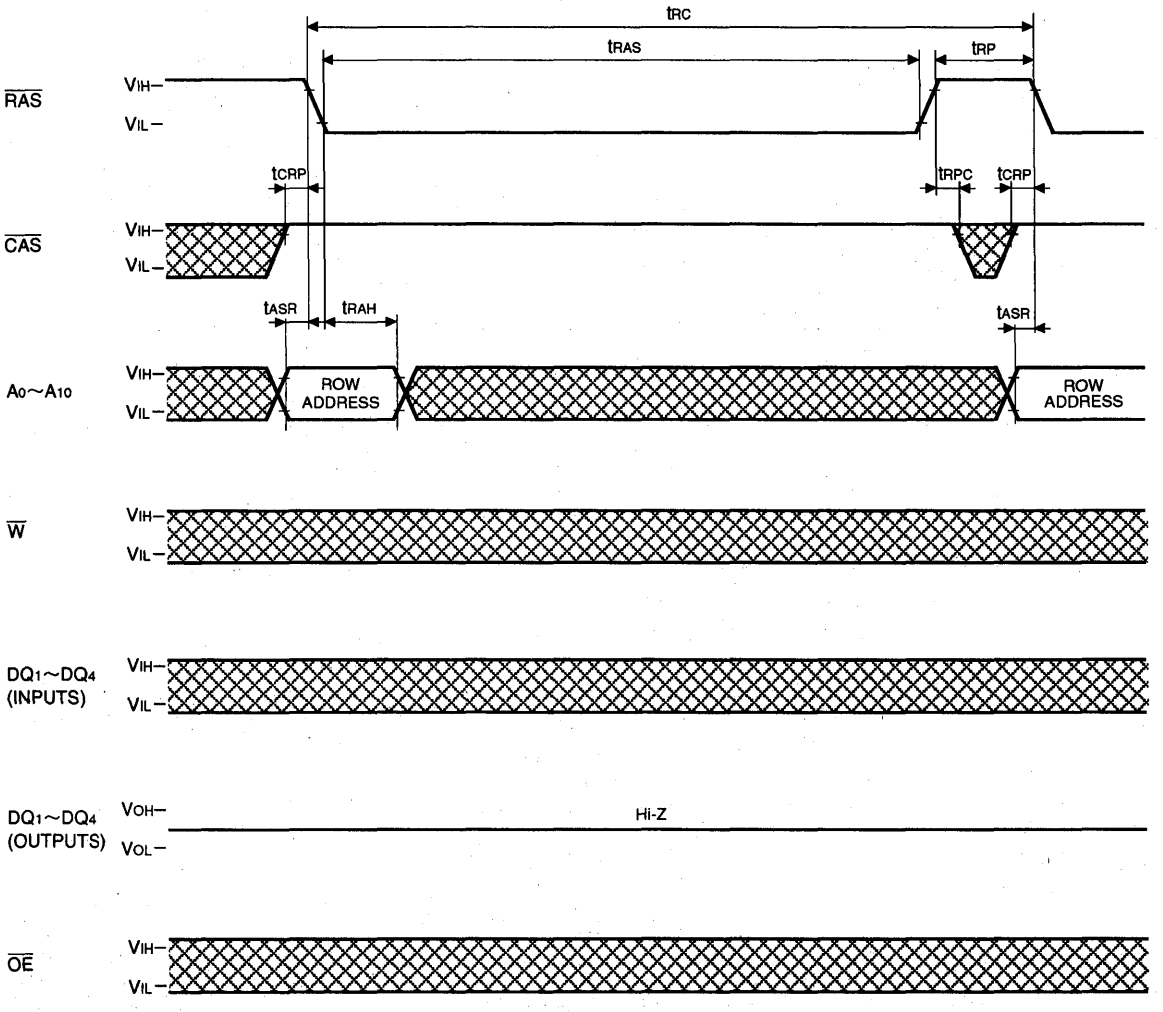
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle

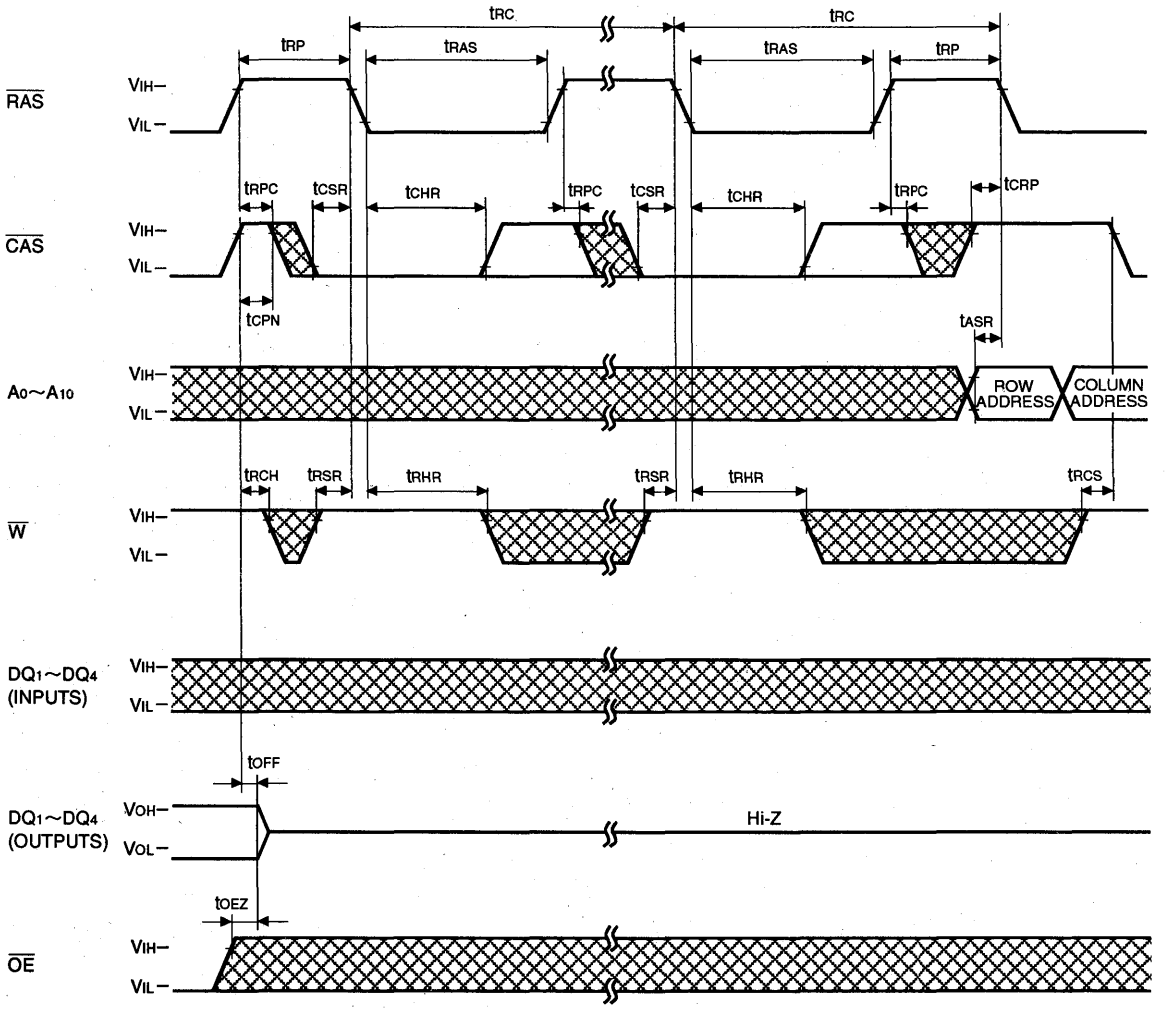


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

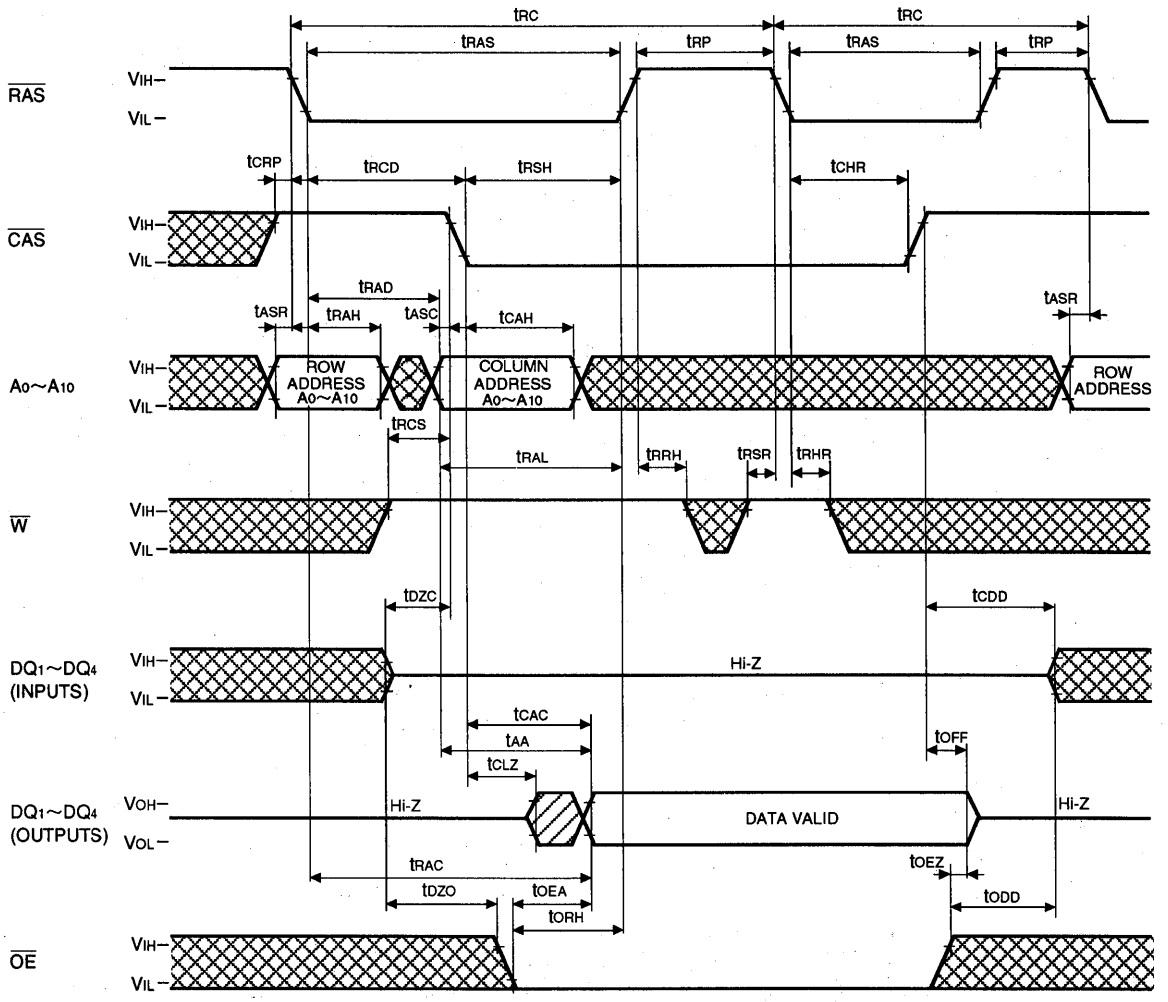
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



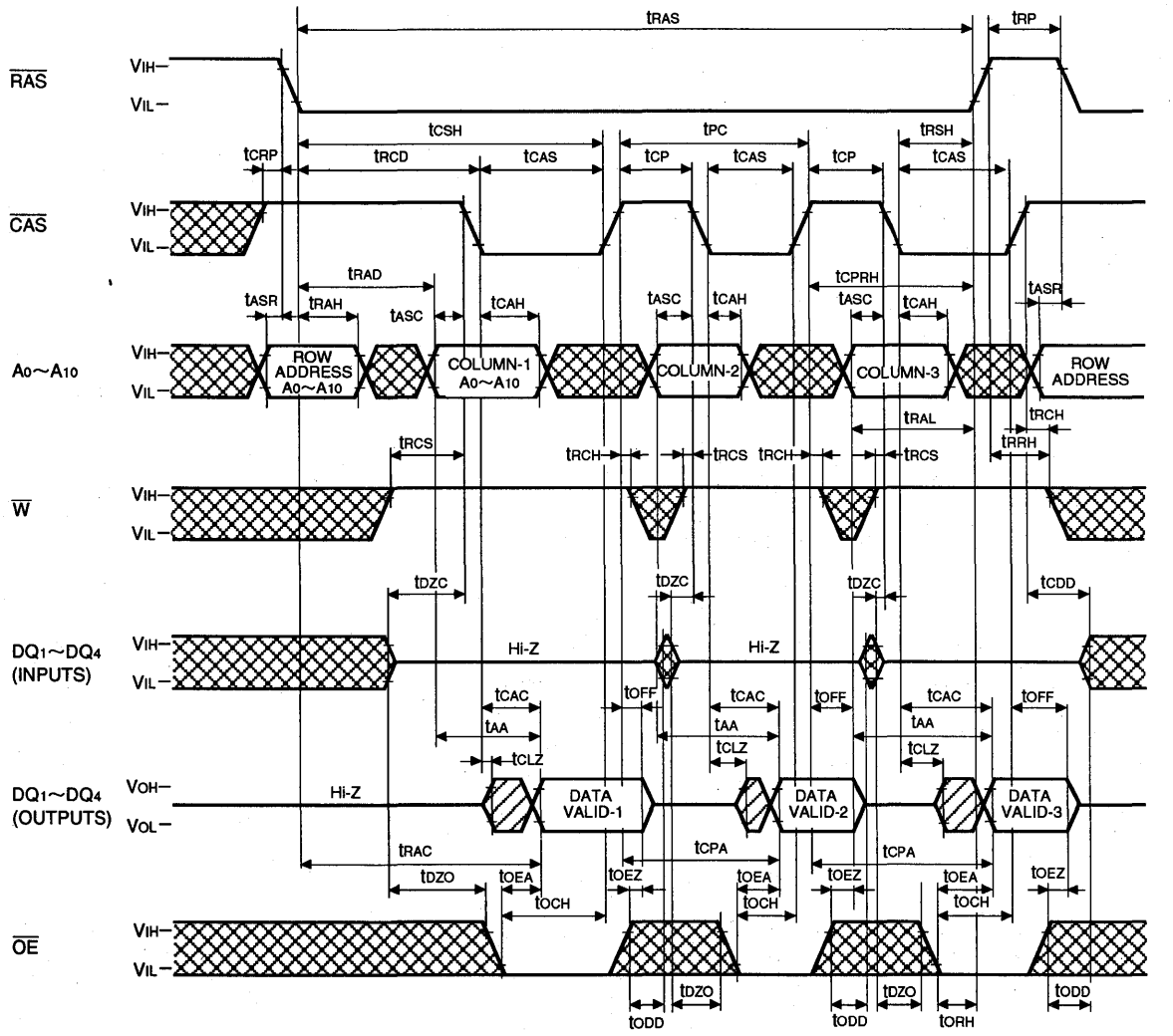
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR & tRHR should be satisfied not to enter TEST MODE .

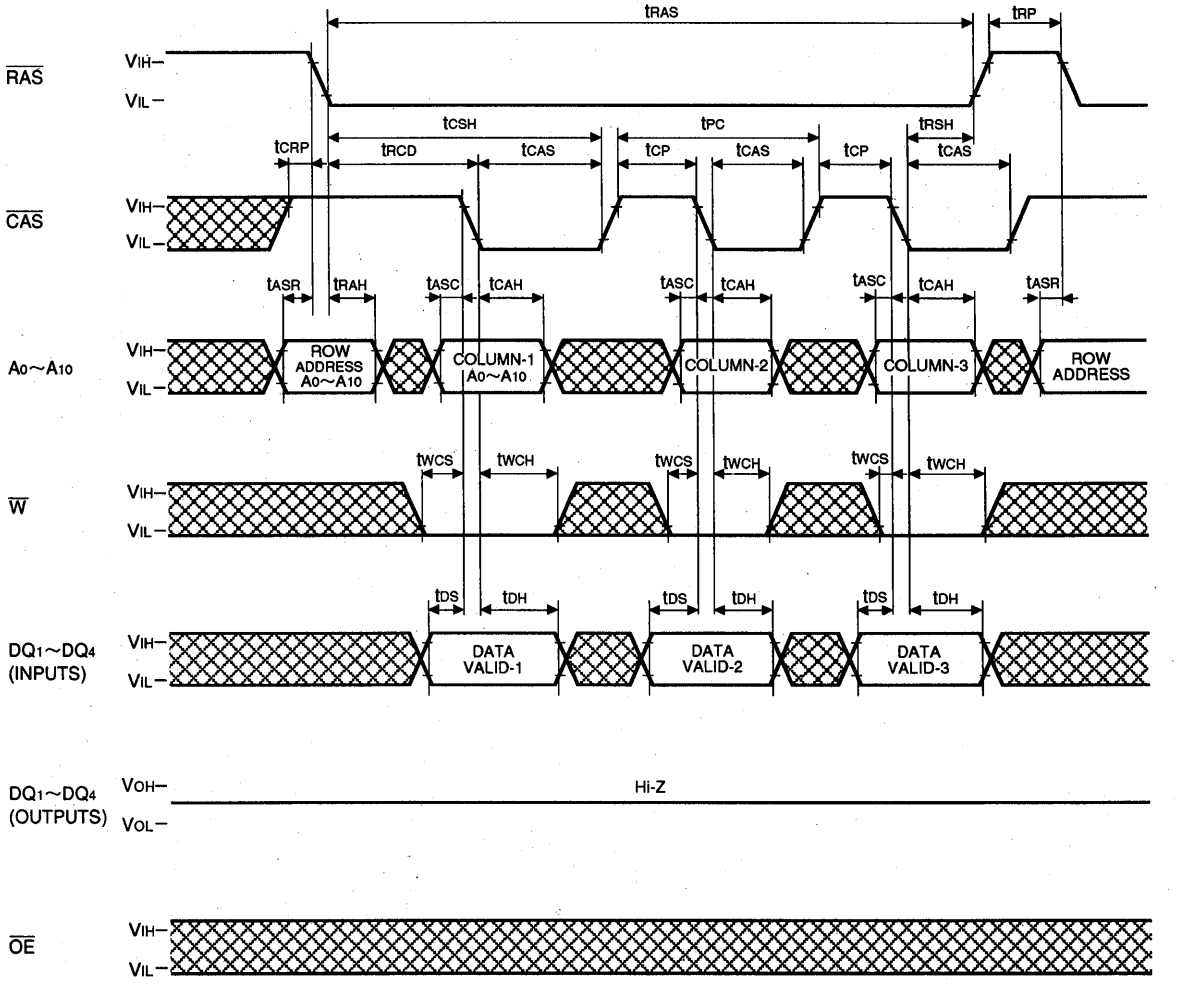
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle



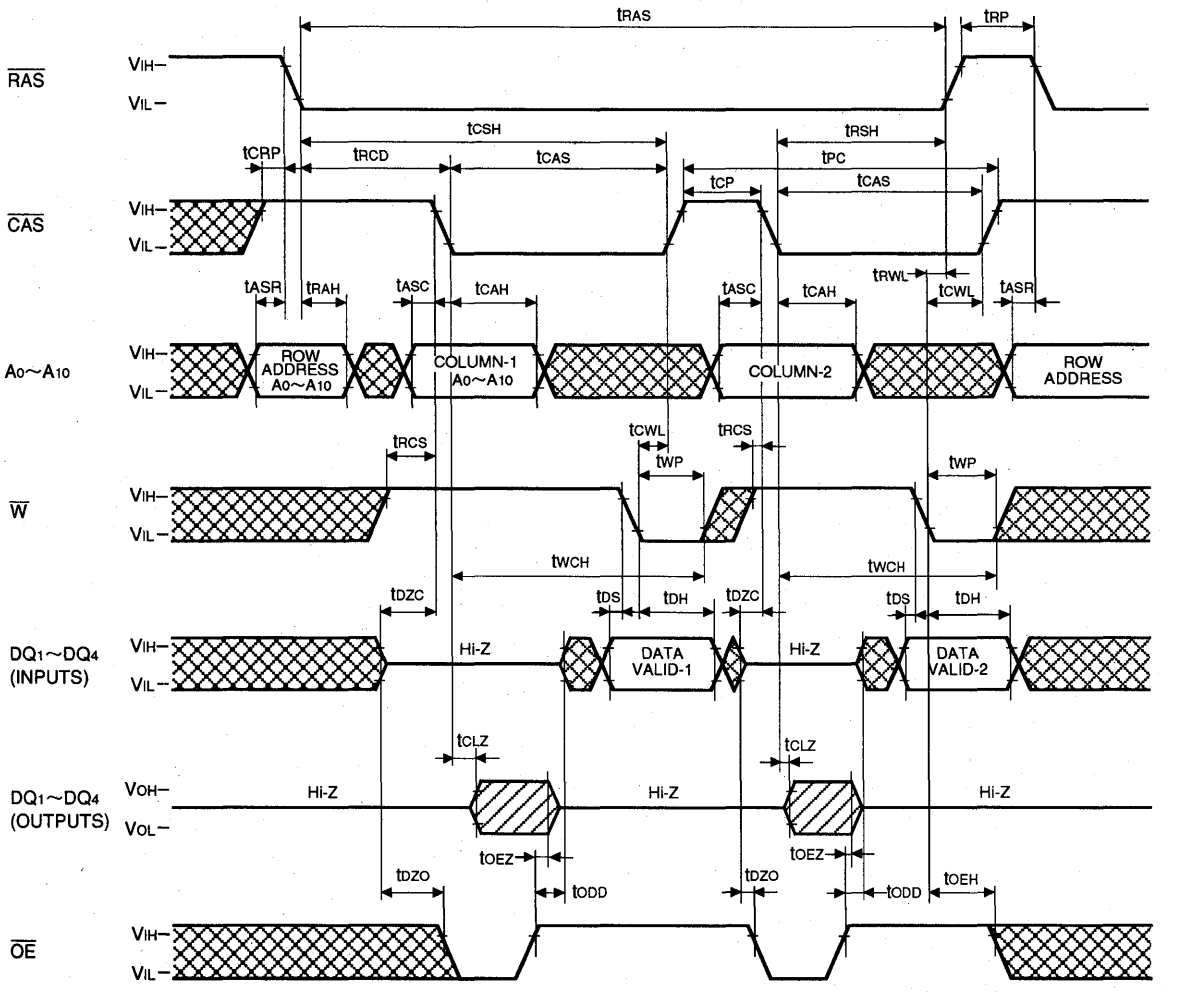
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)

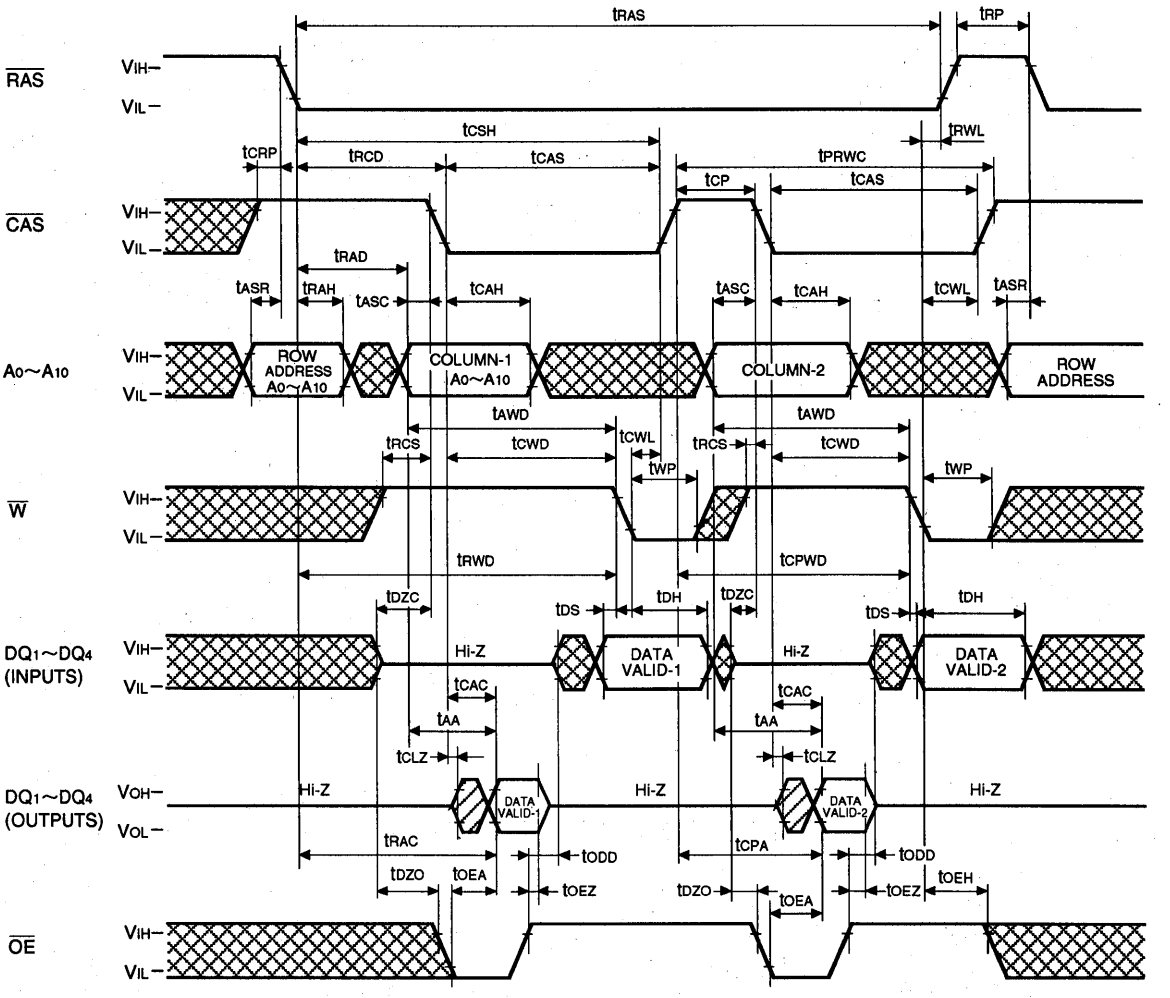


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast-Page Mode Write Cycle (Delayed Write)

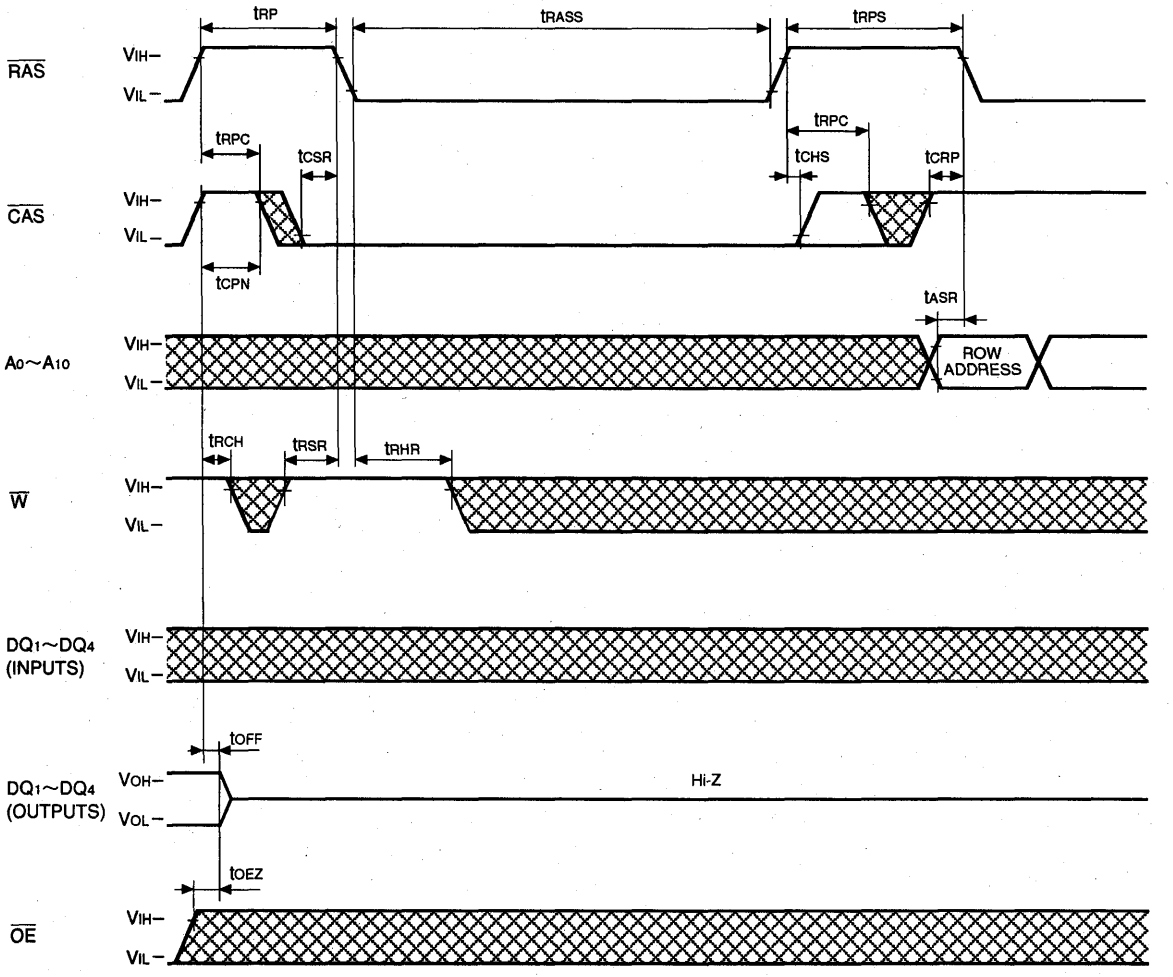


Fast Page Mode Read-Write,Read-Modify-Write Cycle



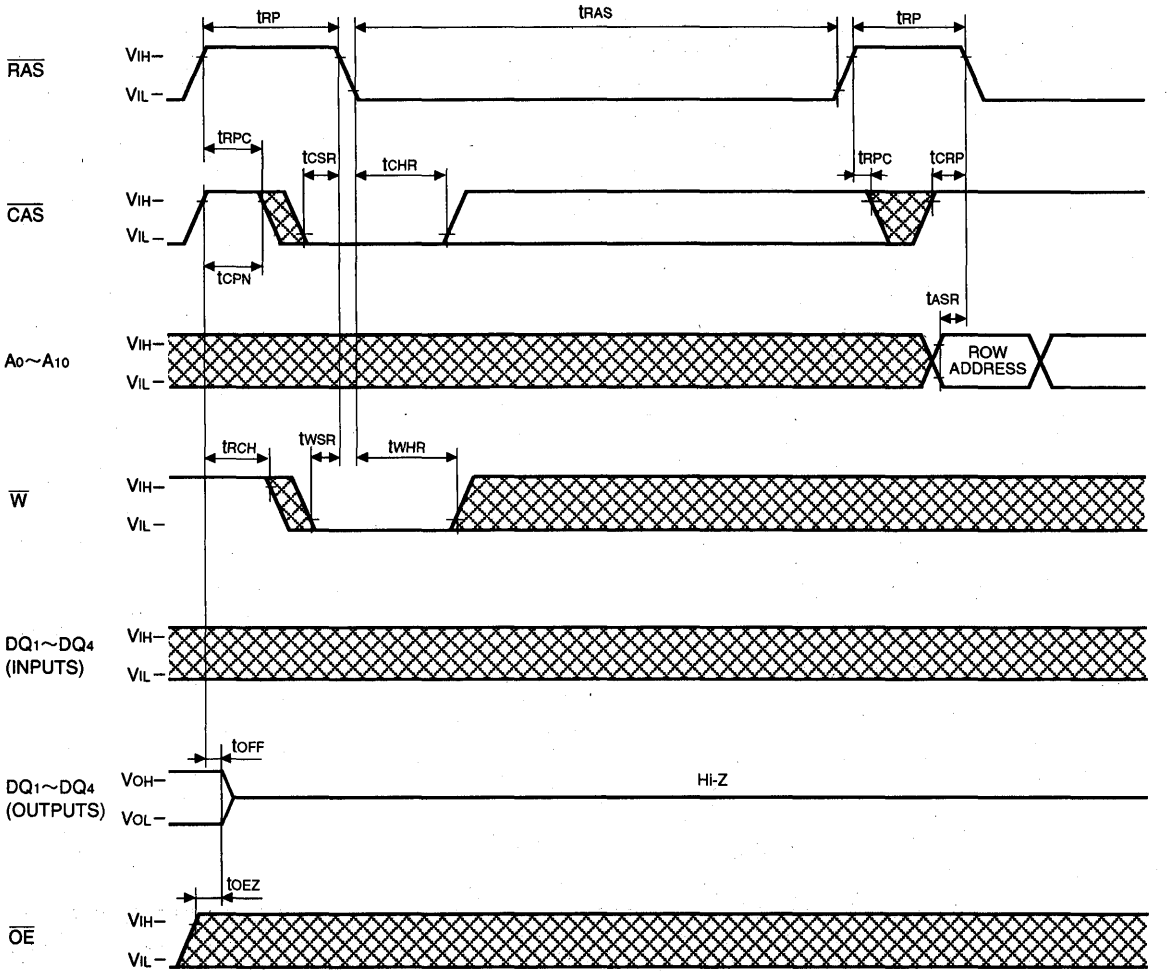
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17405CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17405CXX-5,-5S	50	13	25	13	90	435
M5M4V17405CXX-6,-6S	60	15	30	15	110	360
M5M4V17405CXX-7,-7S	70	20	35	20	130	315

XX=J,TP

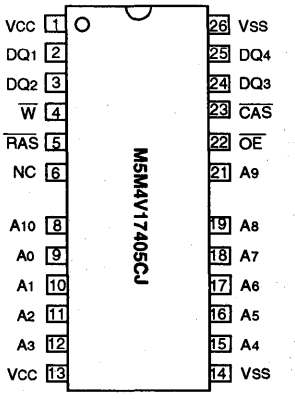
- Standard 26pin SOJ, 26pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.80mW (Max) ---------- CMOS Input level
  - 0.72mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M4V17405Cxx-5,-5S ---------- 525mW (Max)
  - M5M4V17405Cxx-6,-6S ---------- 435mW (Max)
  - M5M4V17405Cxx-7,-7S ---------- 380mW (Max)
- Self refresh capability *
  - Self refresh current ----------200 μA(Max)
- Hyper page mode (2048-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0 ~A_{10})

*:Applicable to self refresh version (M5M4V17405CJ,TP-5S,-6S, -7S:option) only

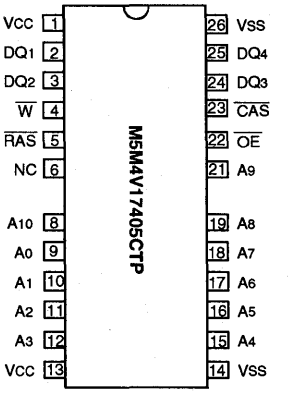
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

NC:NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

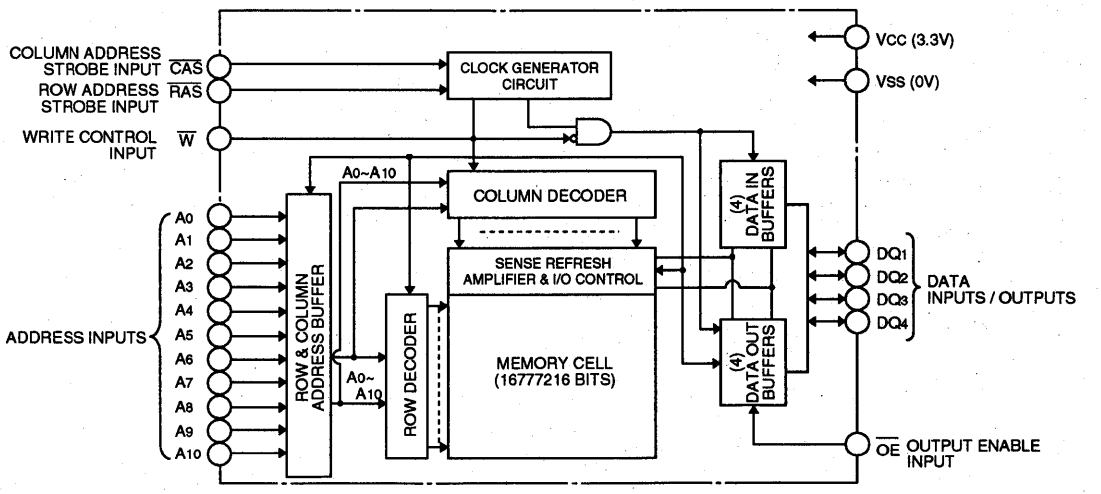
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M4V17405CJ,TP provides a number of other functions, e.g., $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17405CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
V_I	Input voltage		-0.5 ~ 4.6	V
V_O	Output voltage		-0.5 ~ 4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3 **		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V17405C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M4V17405C-6,-6S				120	
		M5M4V17405C-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V17405C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M4V17405C-6,-6S				120	
		M5M4V17405C-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc, Hyper Page Mode (Note 3,4,5)	M5M4V17405C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M4V17405C-6,-6S				115	
		M5M4V17405C-7,-7S				90	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V17405C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M4V17405C-6,-6S				120	
		M5M4V17405C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	V_I=25mVrms			8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 3.3V ±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (IOUT≦|±10 μ A|) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc = 3.3V ±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to CAS low	(Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT=2ns.
15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
19: Either tDZC or tDZO must be satisfied.
20: Either tRDD or tCDD or tODD must be satisfied.
21: tT is measured between VIH(min) and VIL(max).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V IH) is indeterminate.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper Page Mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC} = 3.3V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 6)	M5M4V17405C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$≦0.2V $\overline{OE}$ & $\overline{WE}$≦0.2V or $\overline{OE}$ & $\overline{WE}$≧Vcc-0.2V A_0~A_{10}≦0.2V or A_0~A_{10}≧Vcc-0.2V t_{REF}=128ms (2048cycles) output=OPEN t_{RAS}=t_{RAS}min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 6)	M5M4V17405C (S)	$\overline{RAS}$=$\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

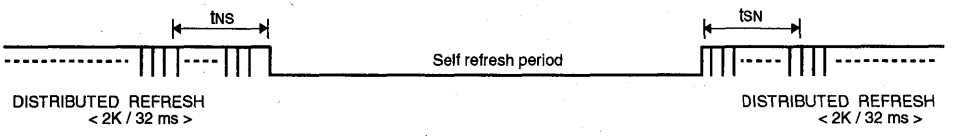
TIMING REQUIREMENTS (T_a=0~70℃, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted, see notes 14, 15)

Symbol	Parameter	Limits						Unit
		M5M4V17405C-5S		M5M4V17405C-6S		M5M4V17405C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

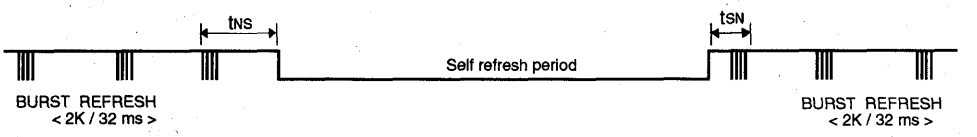
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦32ms and t_{SN}≦32ms.



(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} +t_{SN}≦32ms.

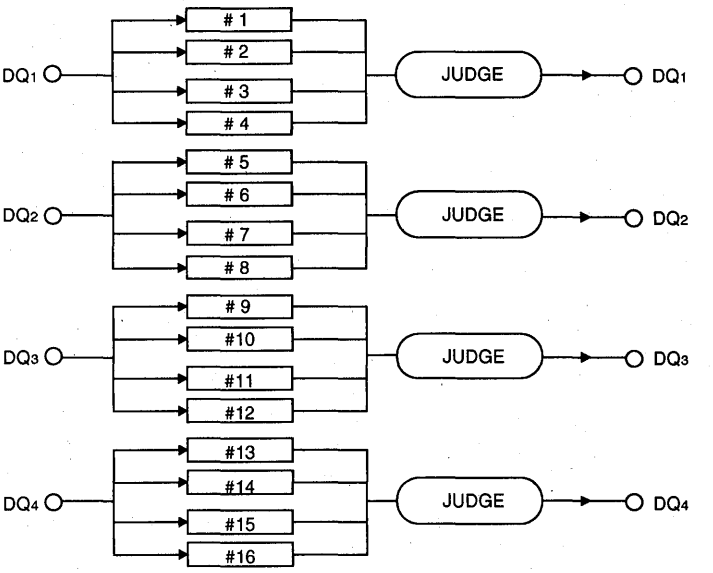


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle (Note 31)

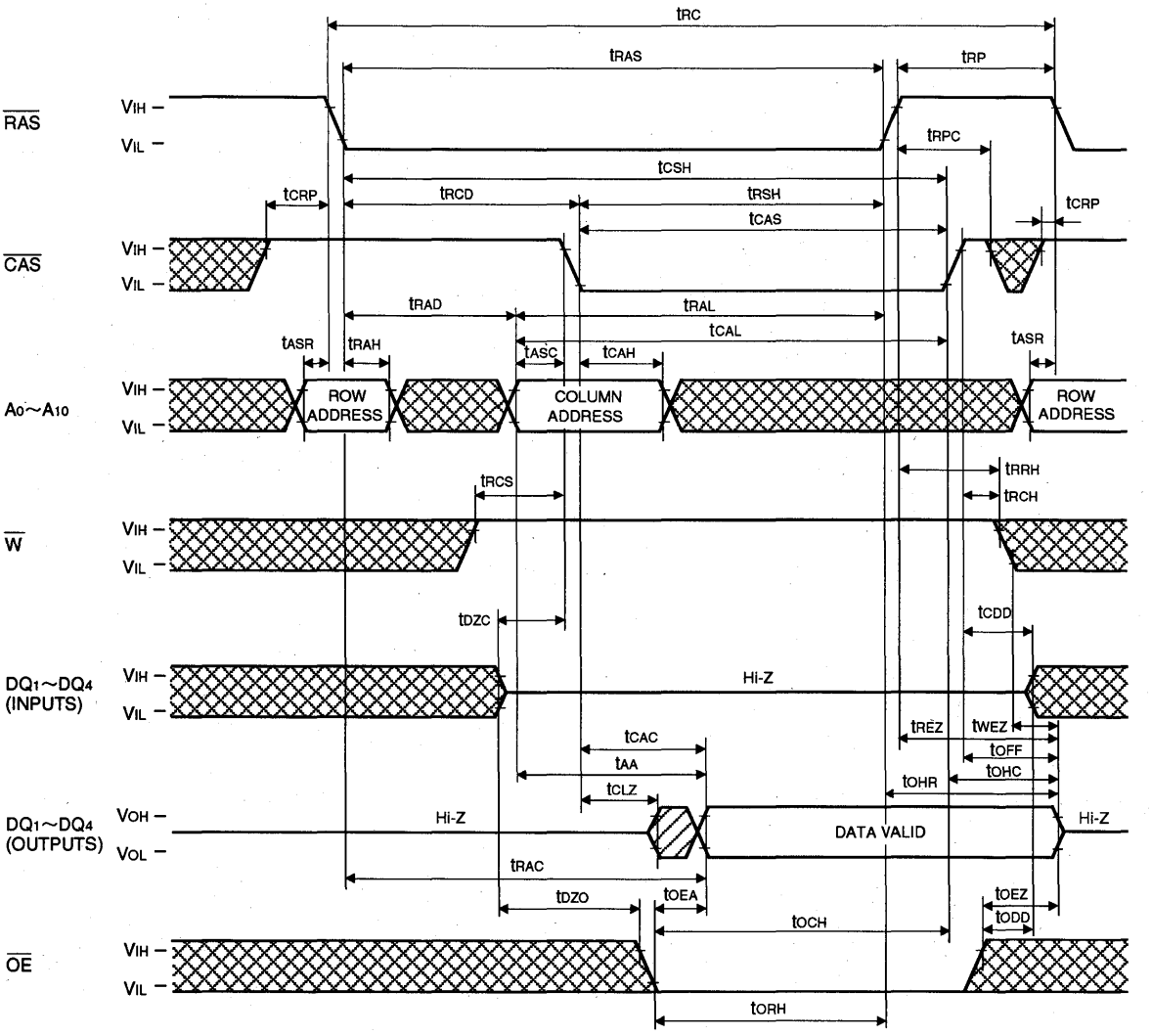
Symbol	Parameter	Limits						Unit
		M5M4V17405C-5,-5S		M5M4V17405C-6,-6S		M5M4V17405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 32)
Read Cycle



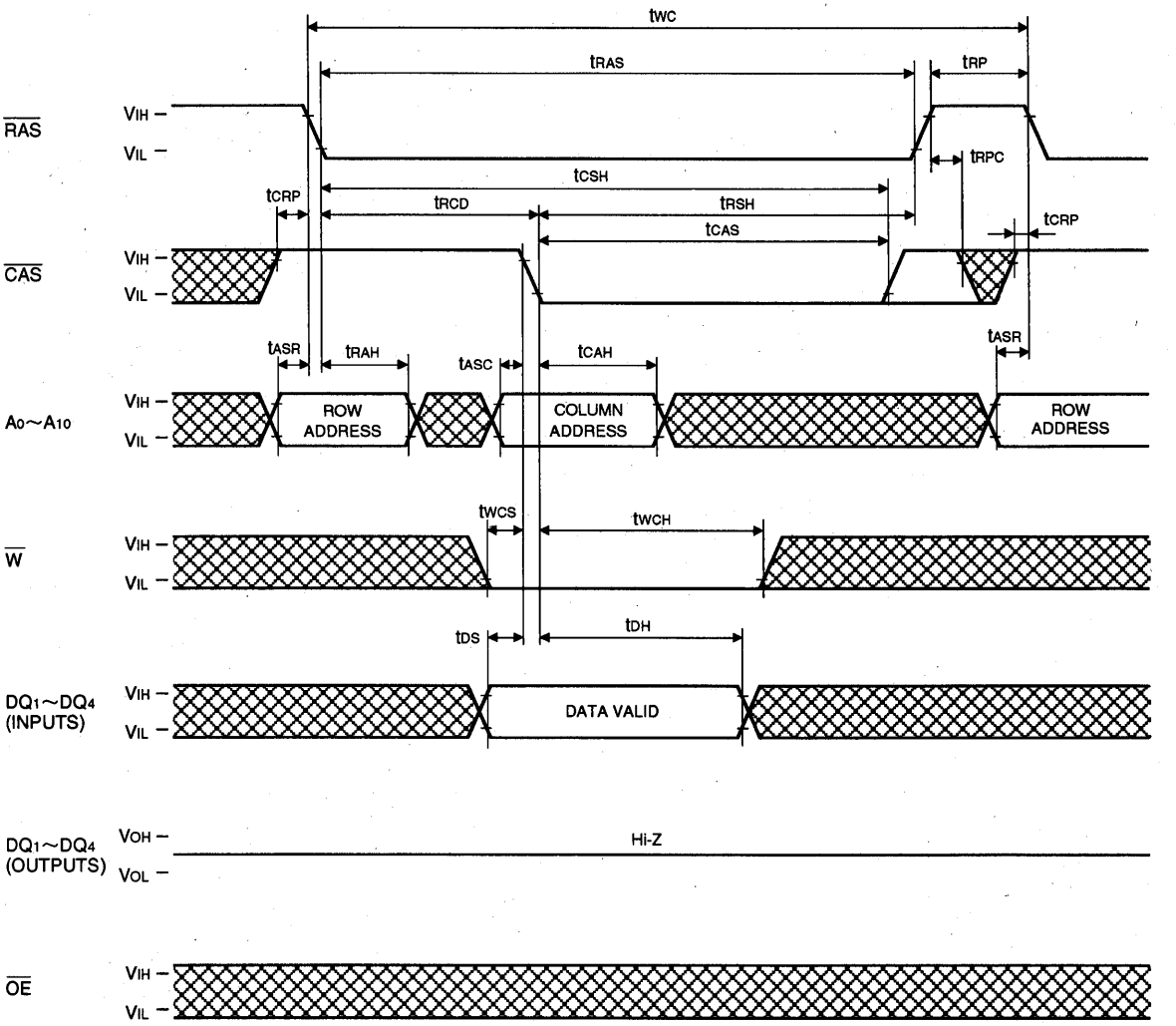
Note 32

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

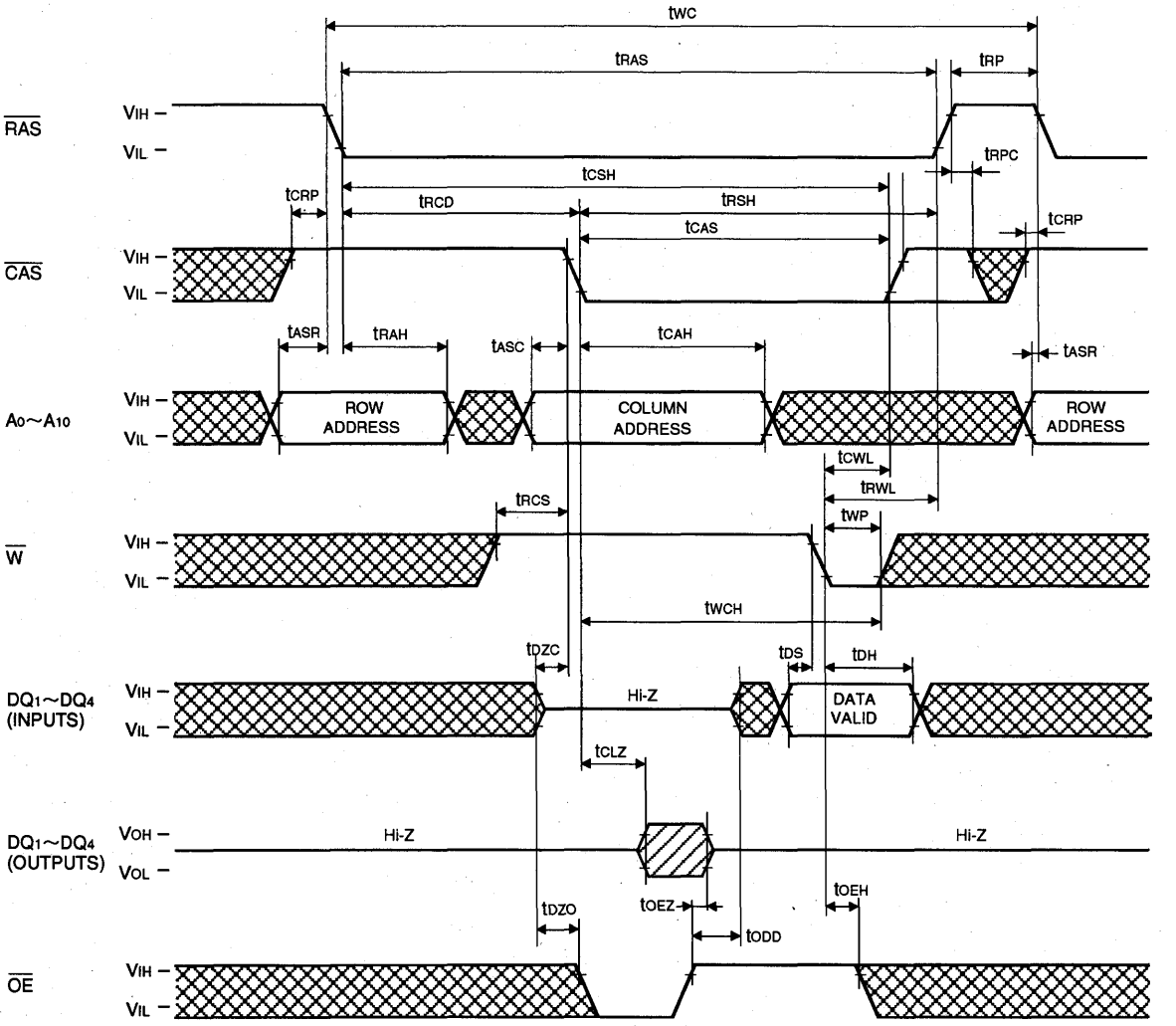
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Early Write Cycle



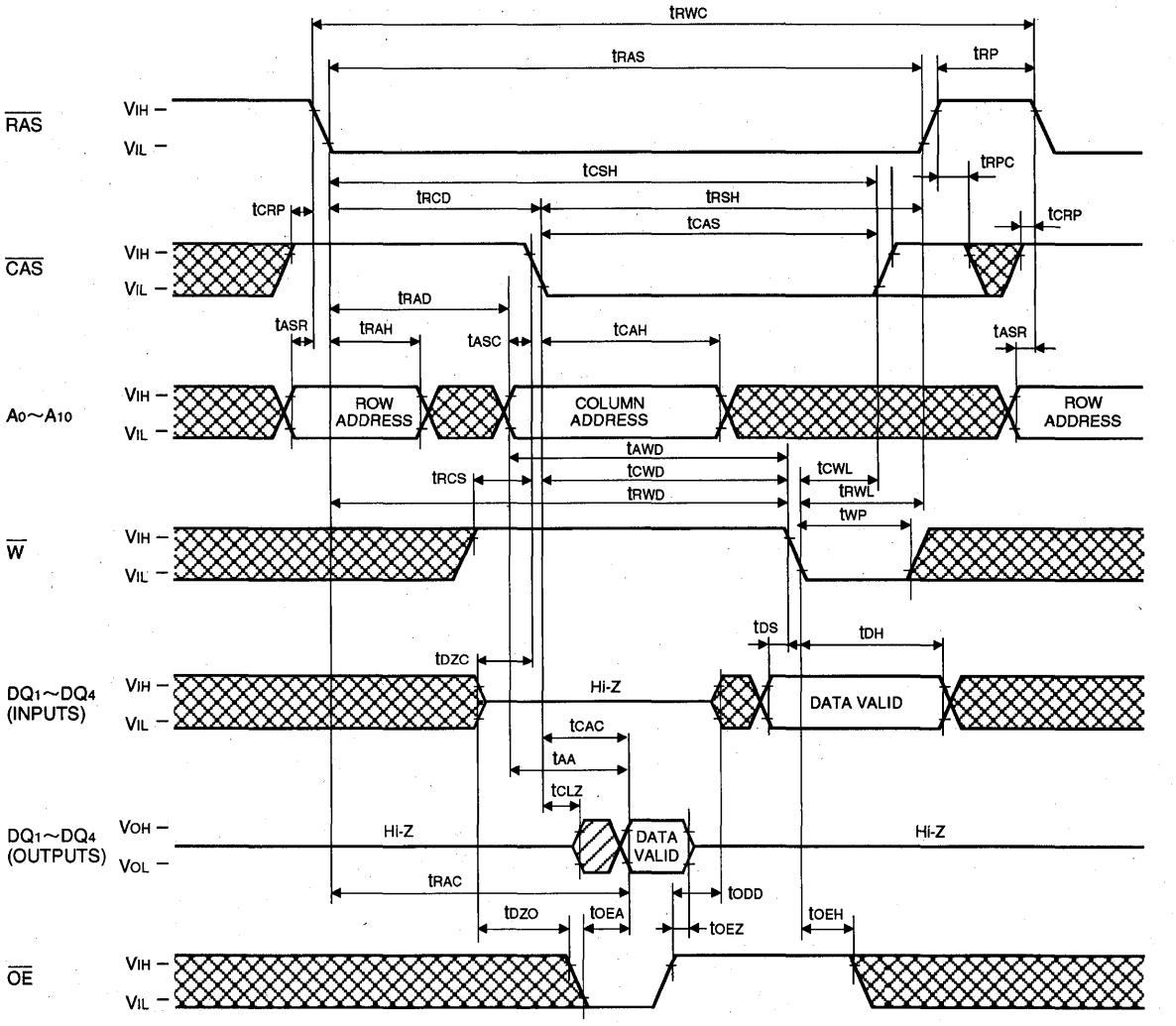
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Delayed Write Cycle



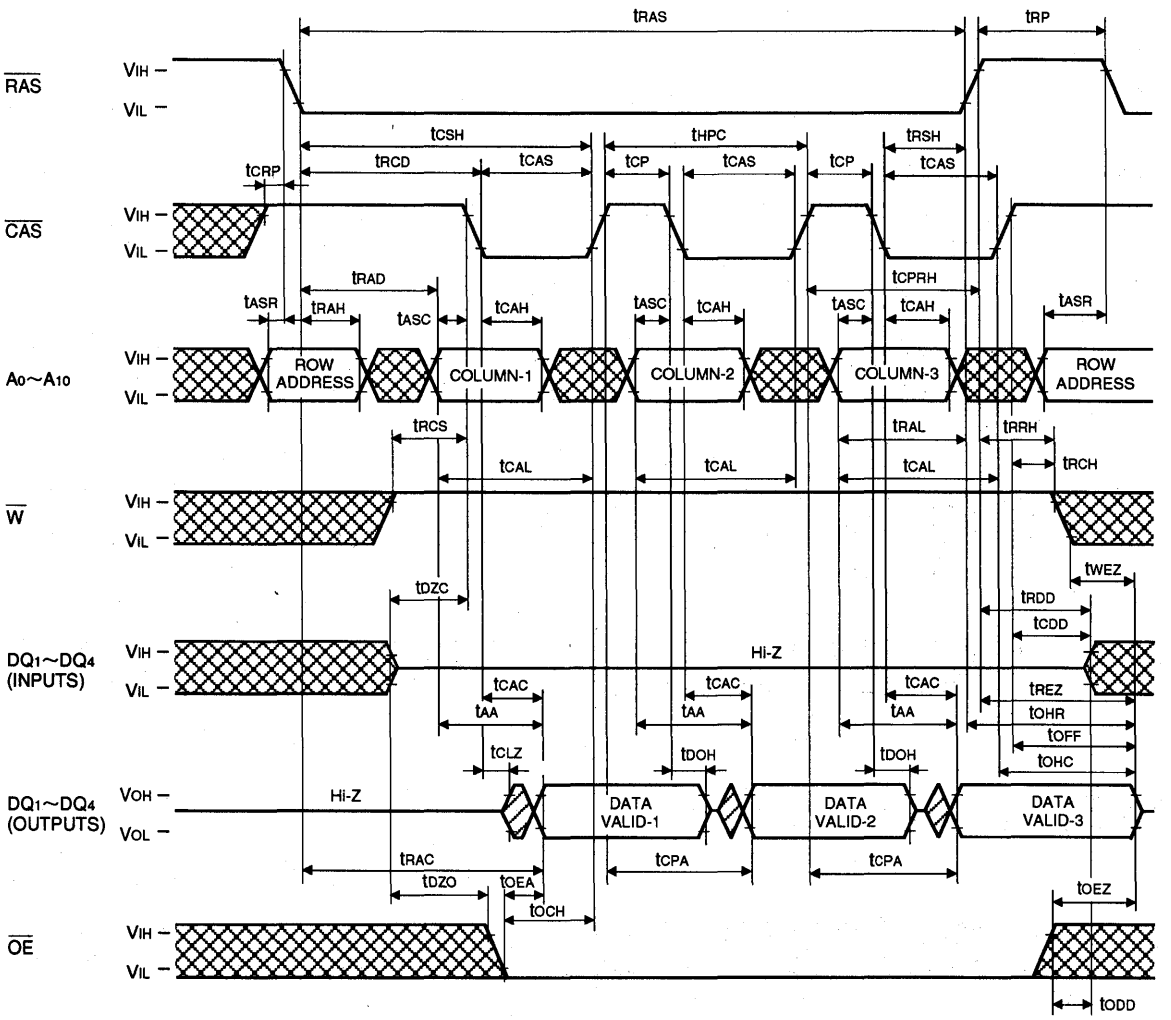
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle

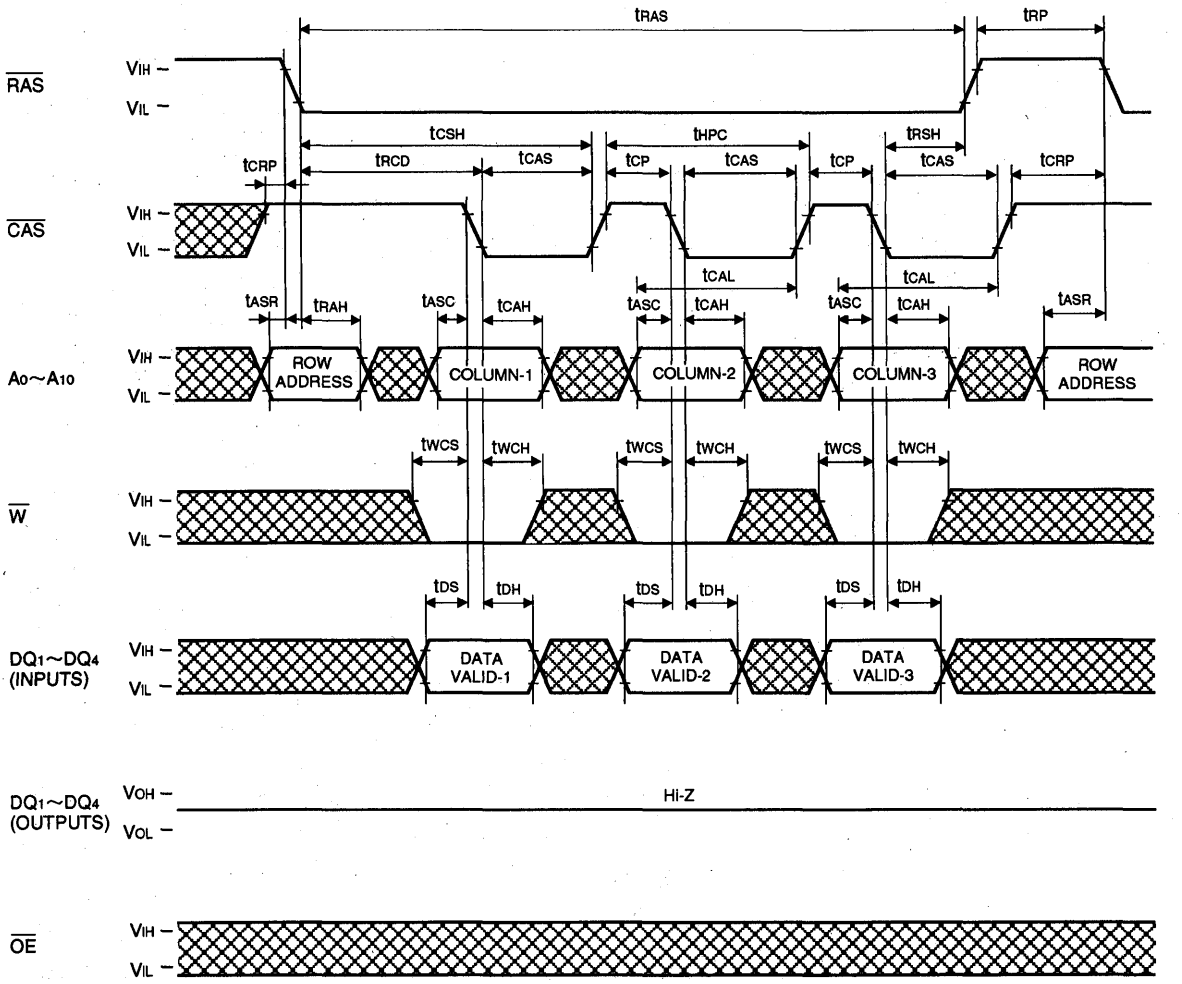


MITSUBISHI ELECTRIC

Hyper Page Mode Read Cycle

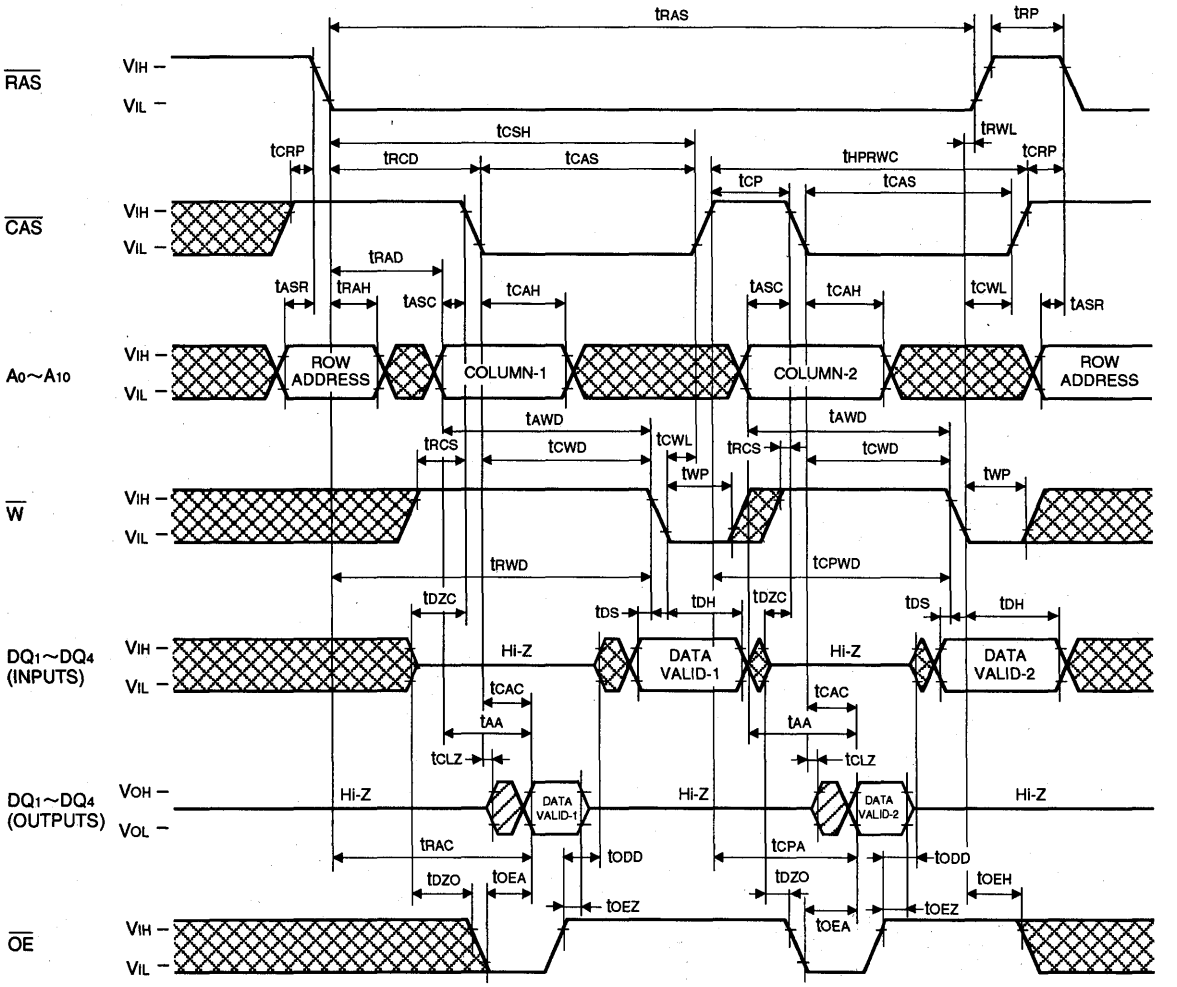


Hyper Page Mode Early Write Cycle

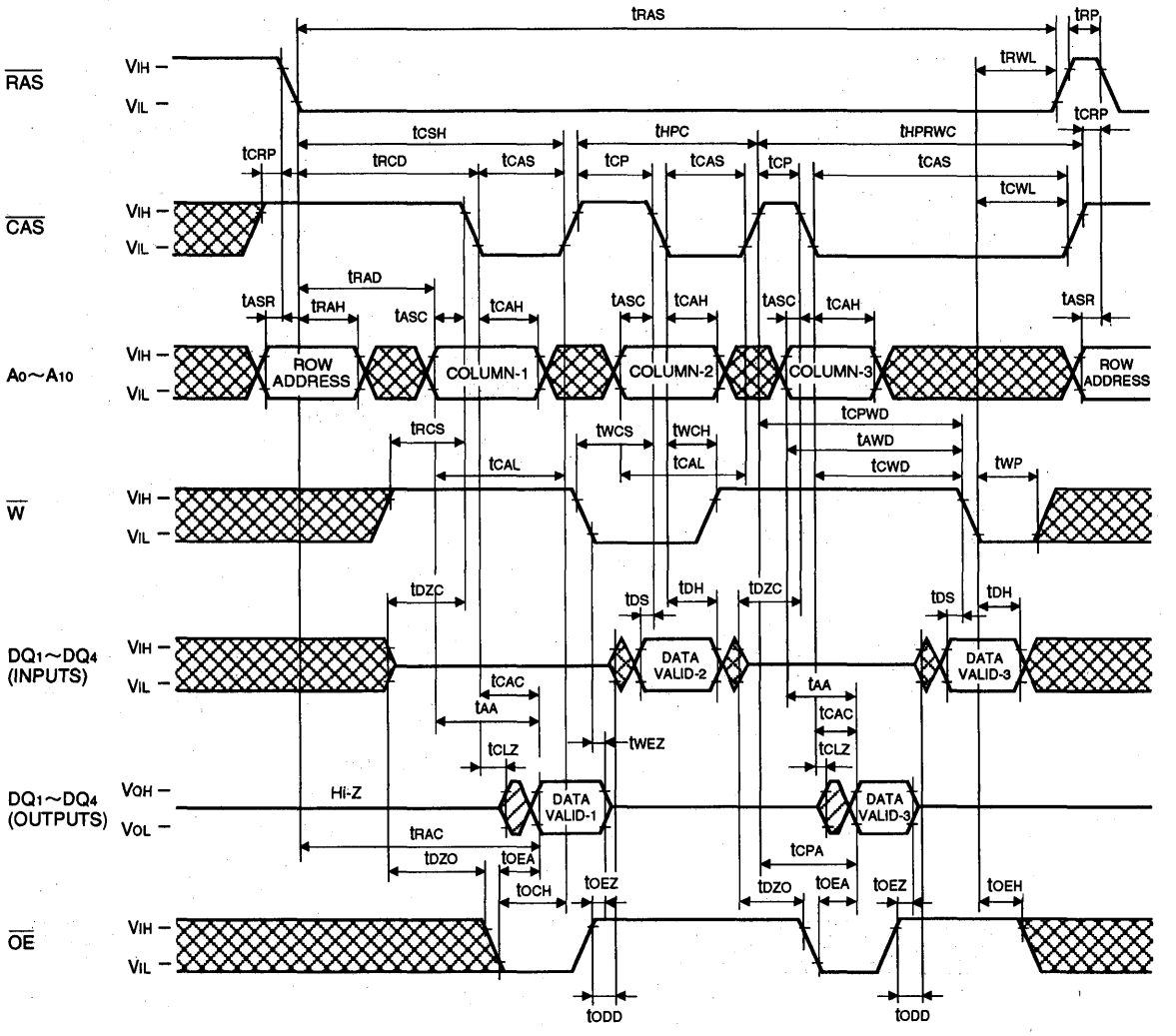


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read-Write, Read-Modify-Write Cycle

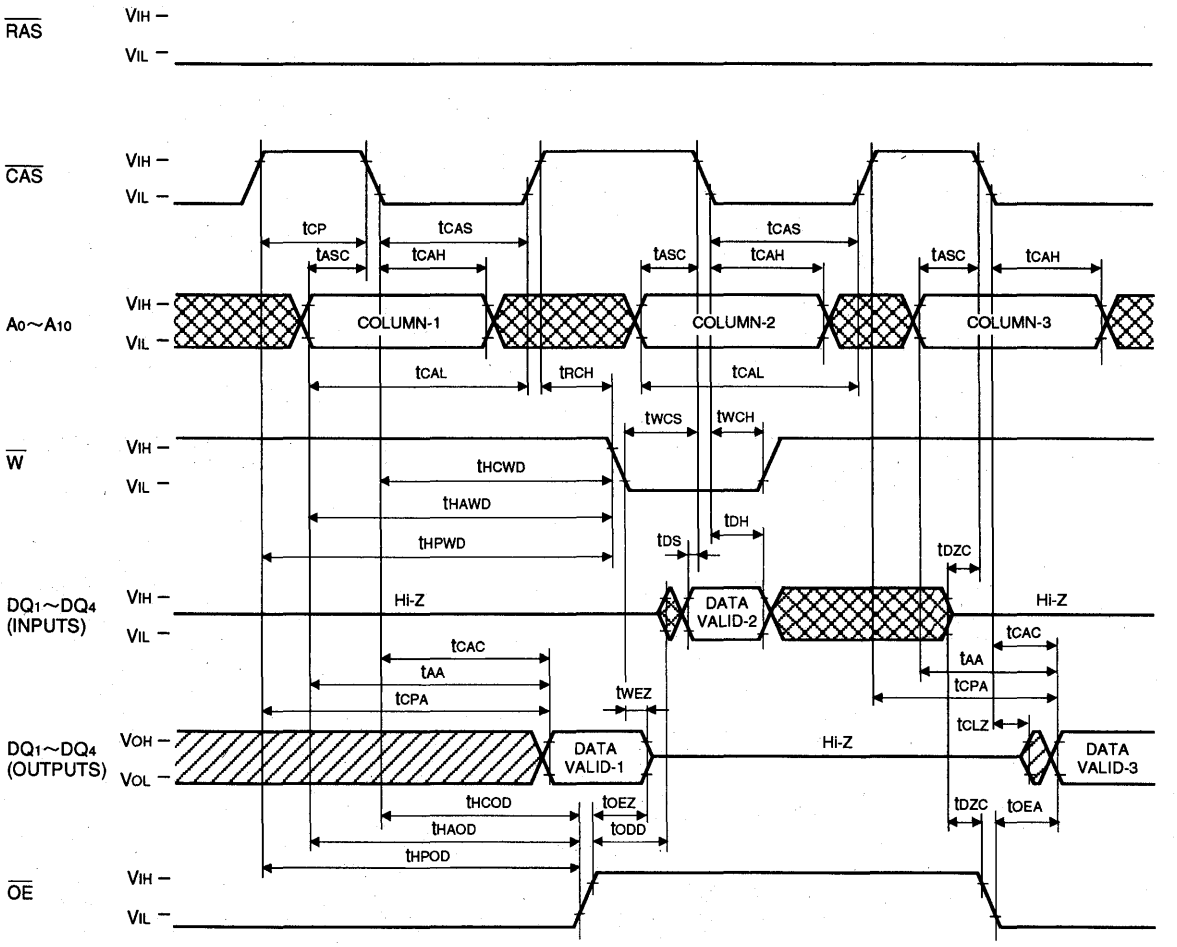


Hyper Page Mode Mix Cycle (1)



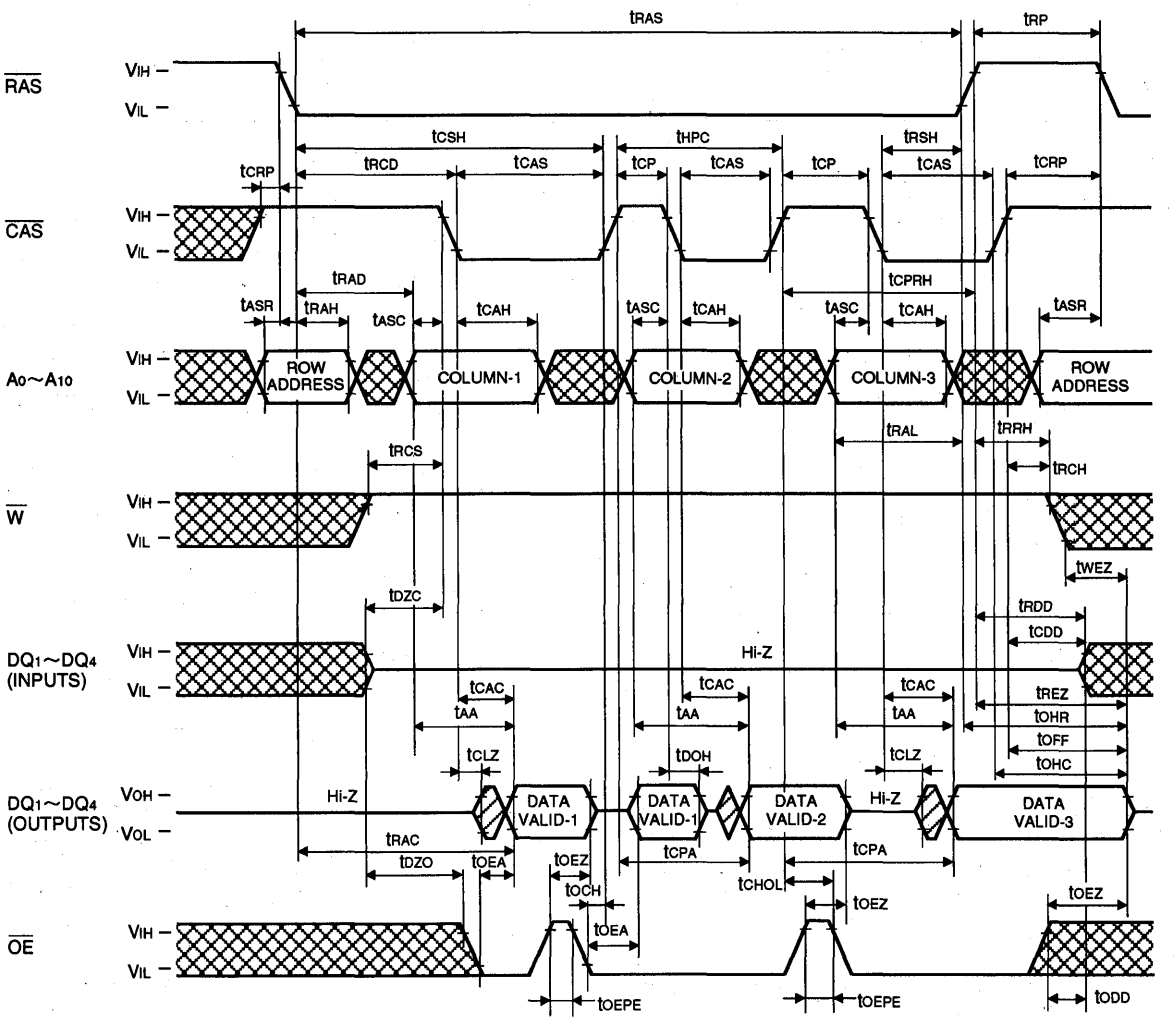
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (2)

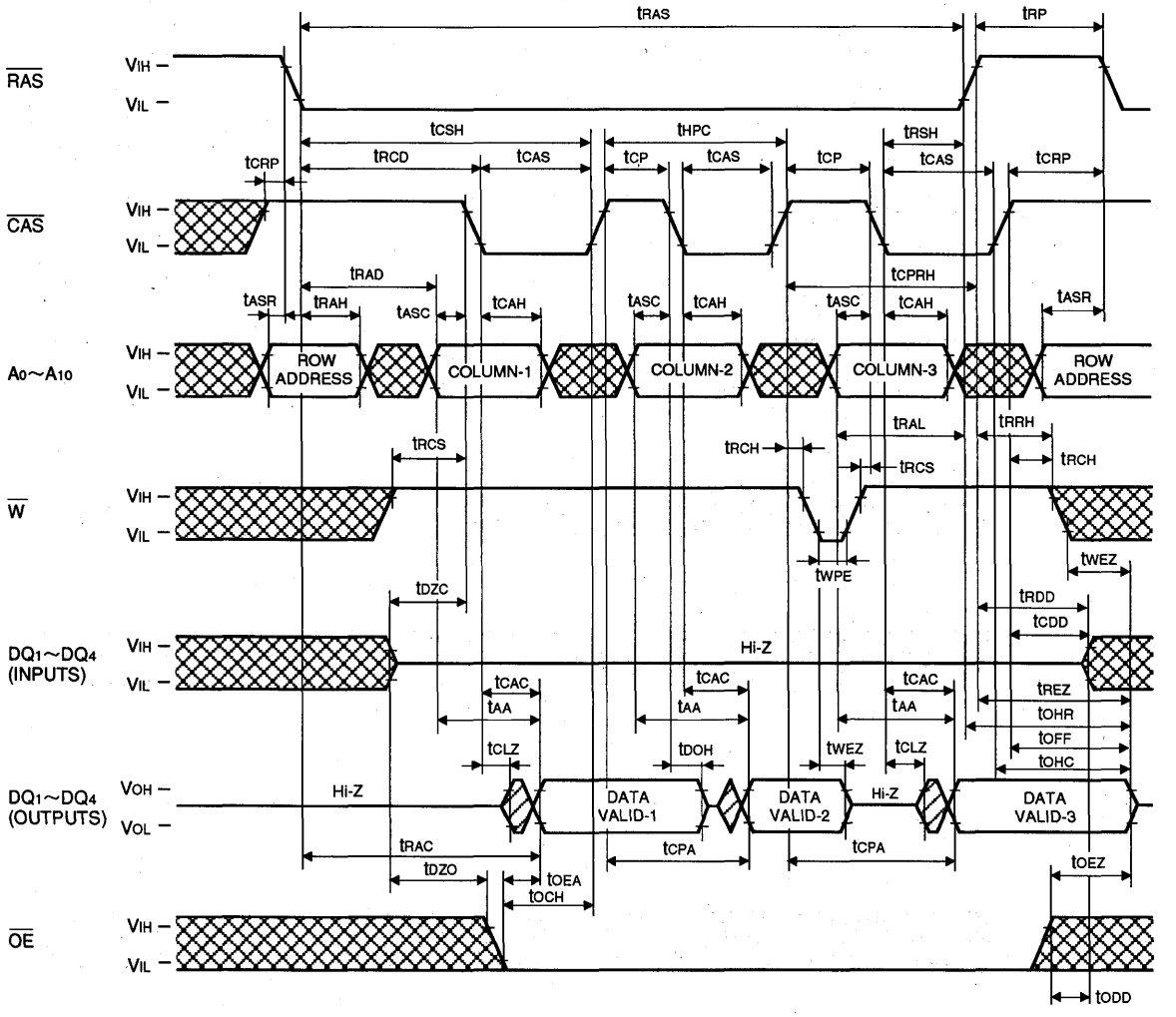


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

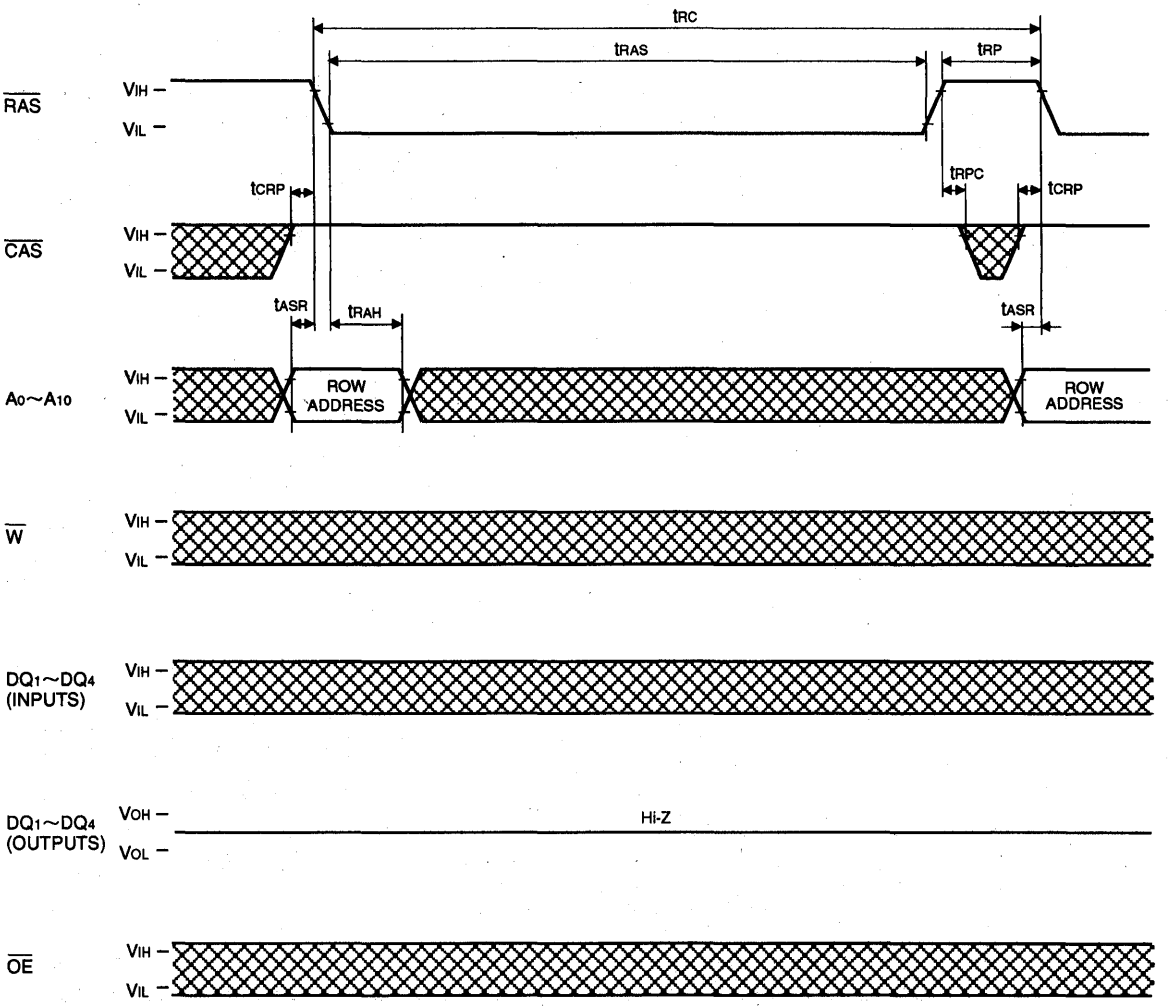
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

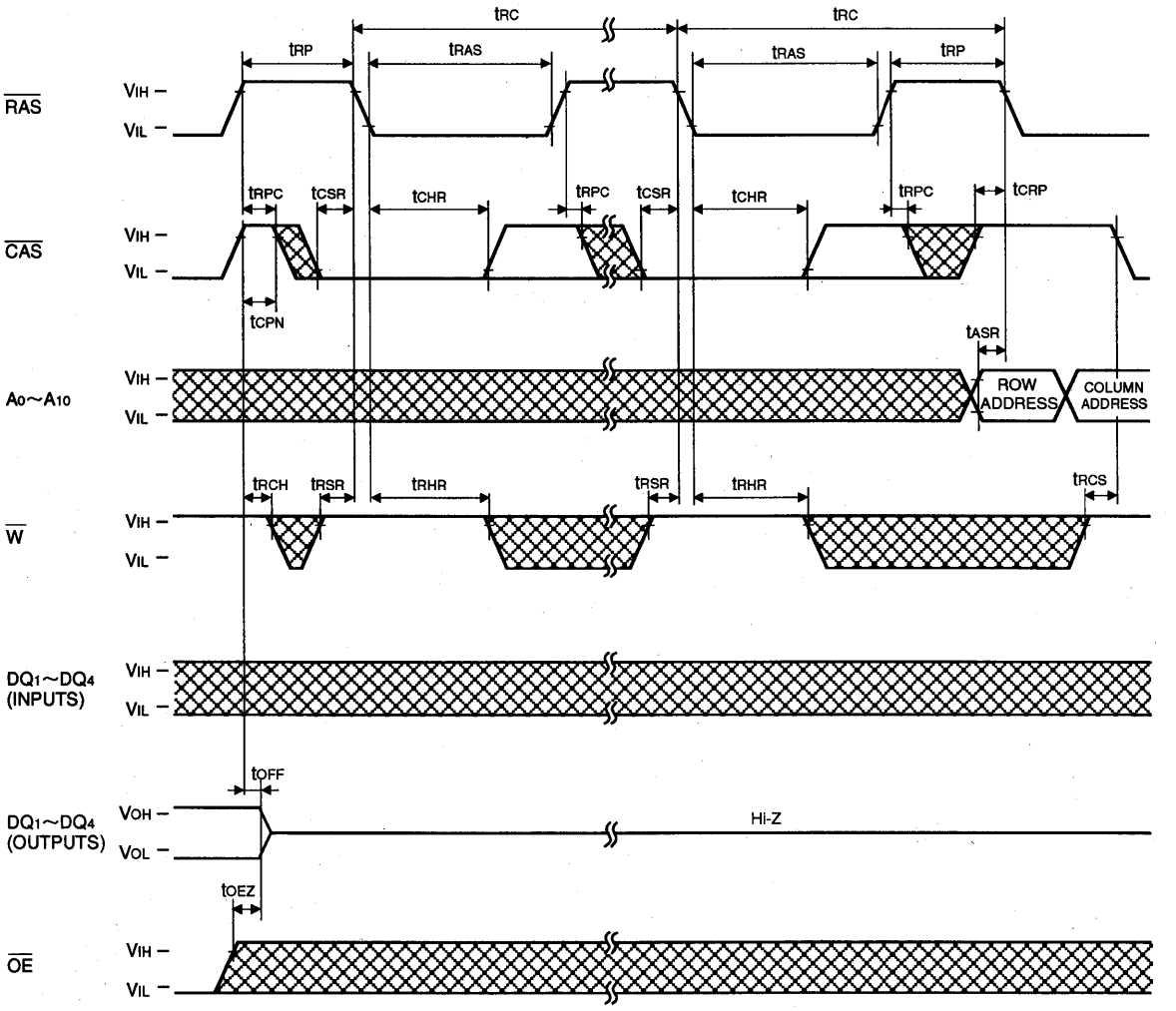


$\overline{RAS}$-only Refresh Cycle

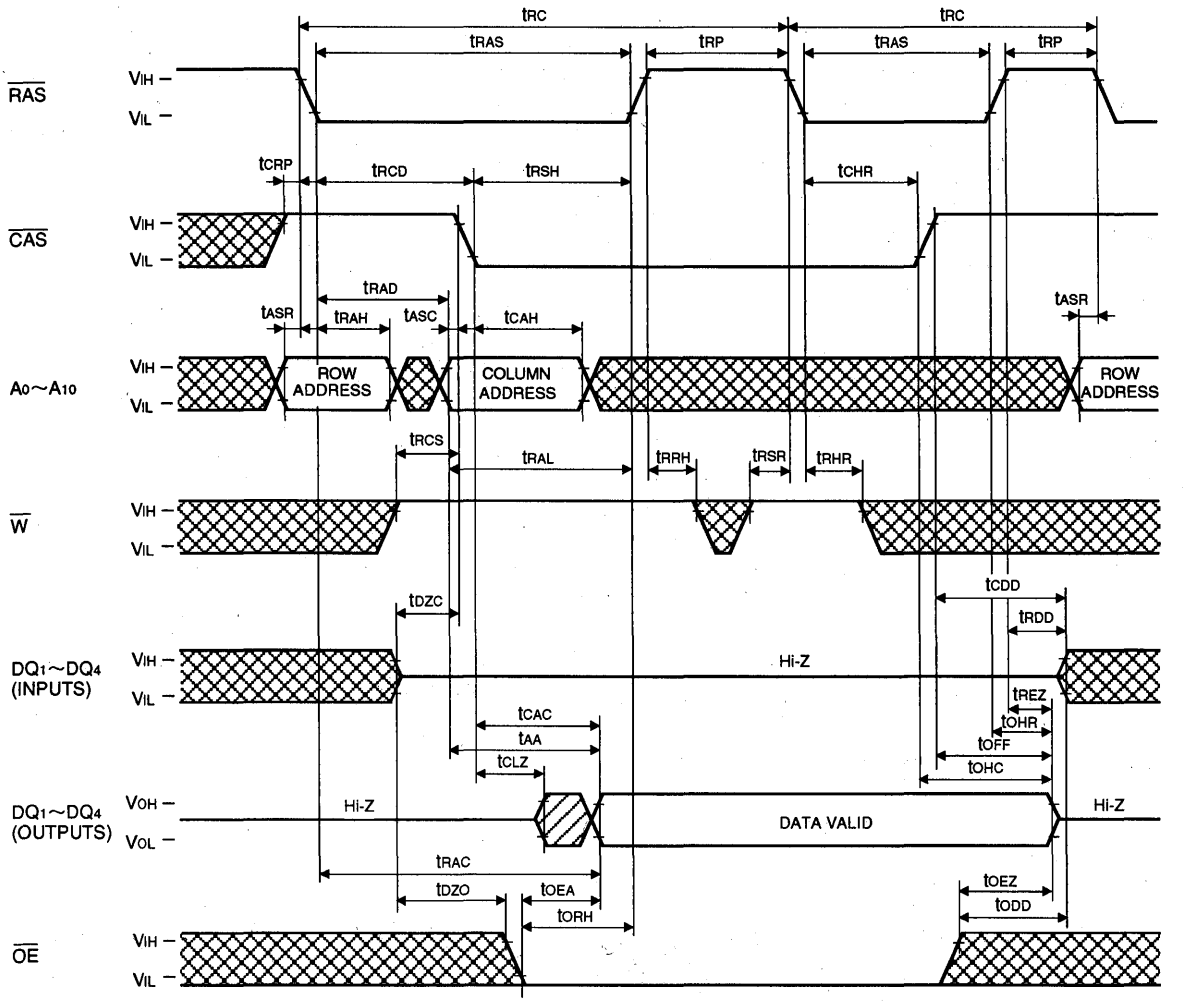


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

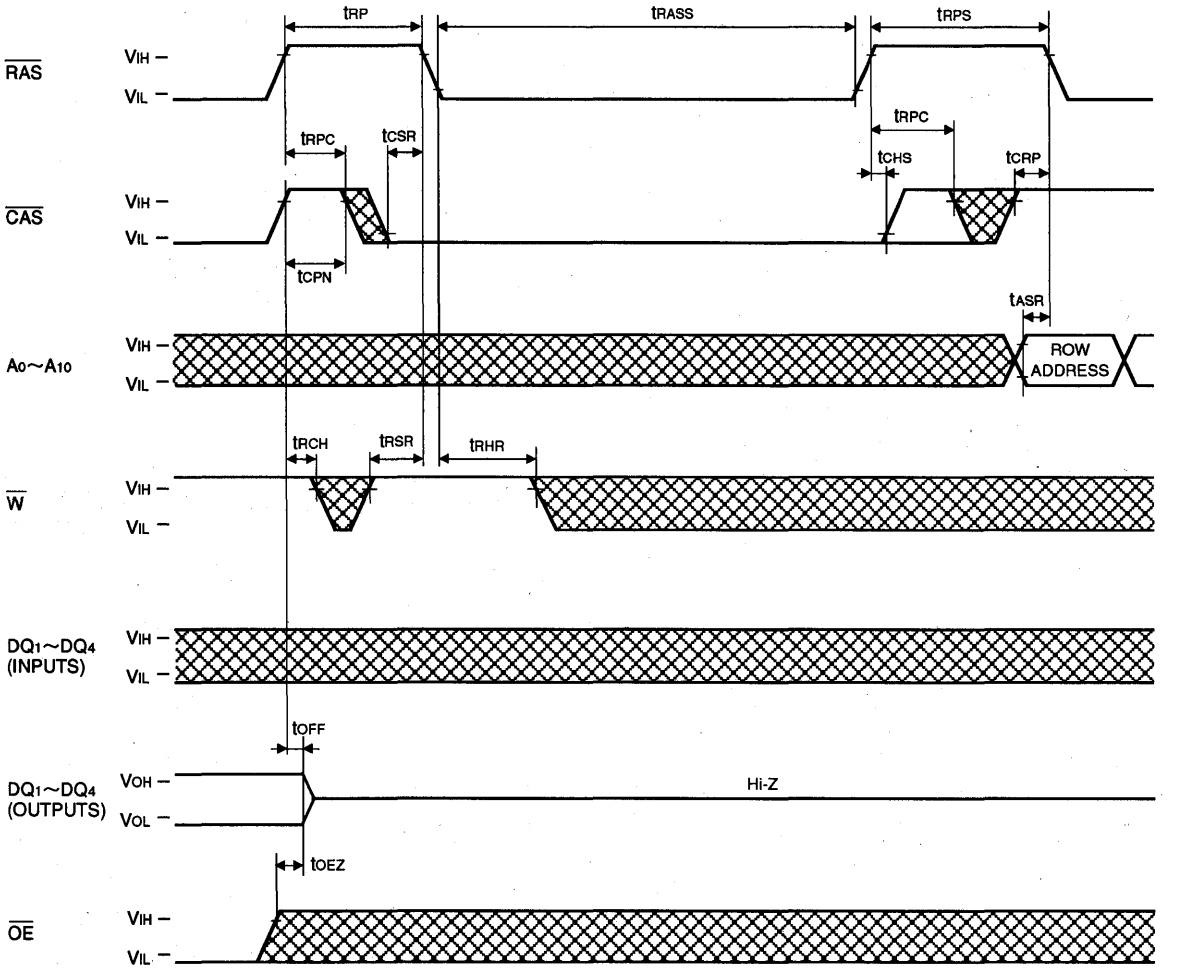


Hidden Refresh Cycle (Read) (Note 33)

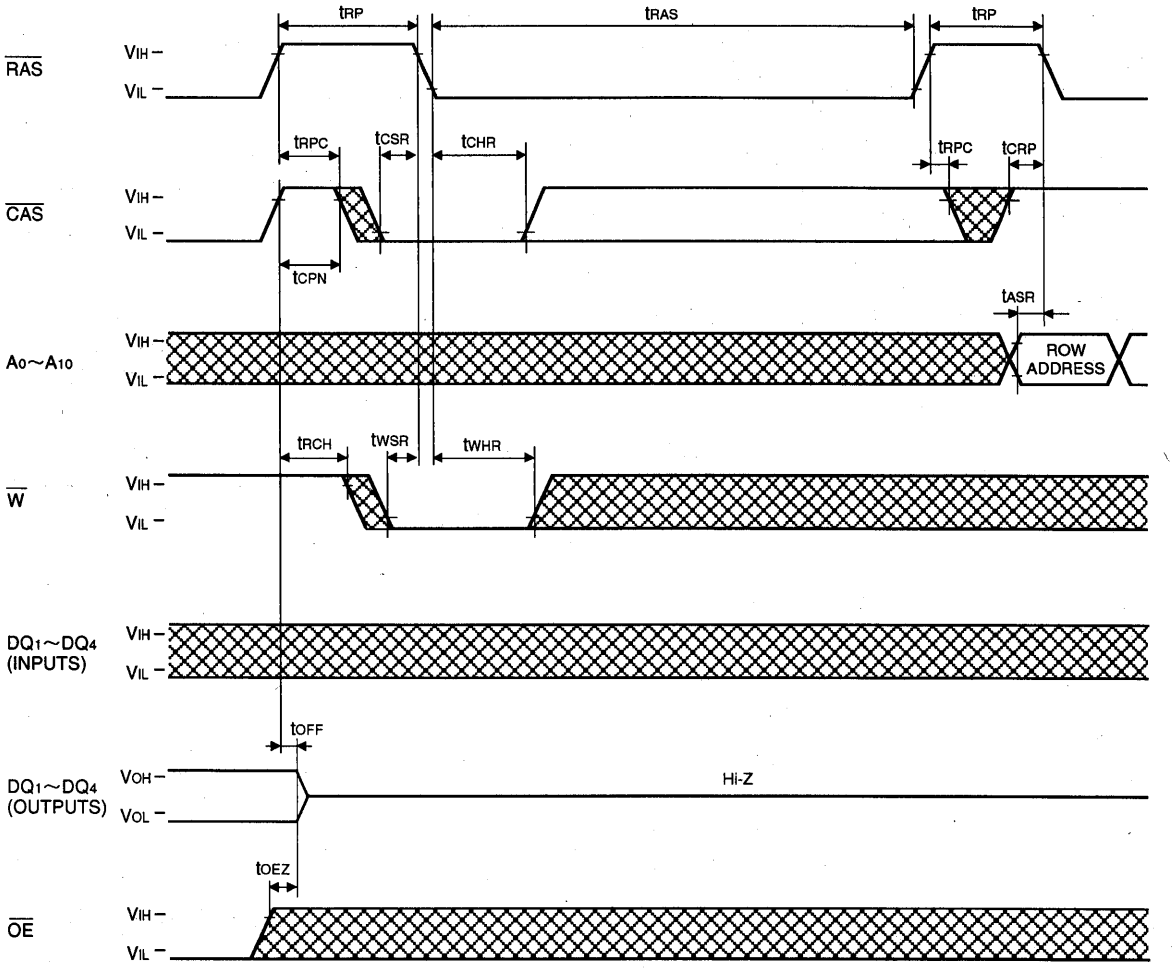


Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

M5M4V17800AJ,TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ acsess time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17800AXX-6,-6S	60	15	30	15	110	360
M5M4V17800AXX-7,-7S	70	20	35	20	130	315

XX = J, TP

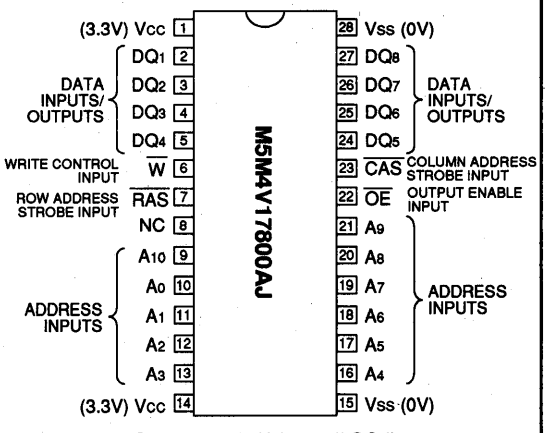
- Standard 28 pin SOJ, 28 pin TSOP
- Single 3.3V±10%supply
- Low stand-by power dissipation
  - 1.8mW (Max) ····· CMOS Input level
  - 1.44mW*(Max) ····· CMOS Input level
- Low operating power dissipation
  - M5M4V17800Axx- 6, -6S ····· 435.0mW (Max)
  - M5M4V17800Axx- 7, -7S ····· 380.0mW (Max)
- Self refresh capability *
  - self refresh current ····· 200.0μA (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

*Applicable to self refresh version (M5M4V17800AJ, TP-6S, -7S : option only)

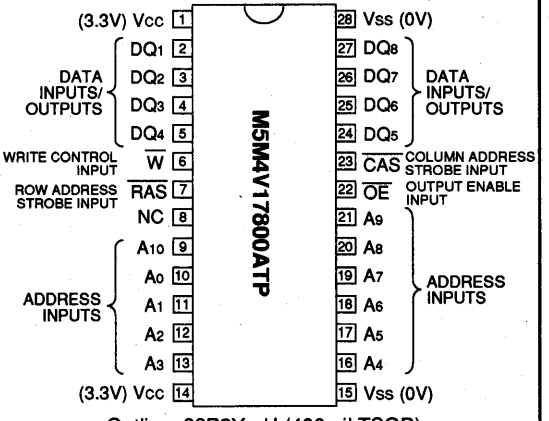
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K (400mil SOJ)



Outline 28P3Y - H (400mil TSOP)

NC : NO CONNECTION

FUNCTION

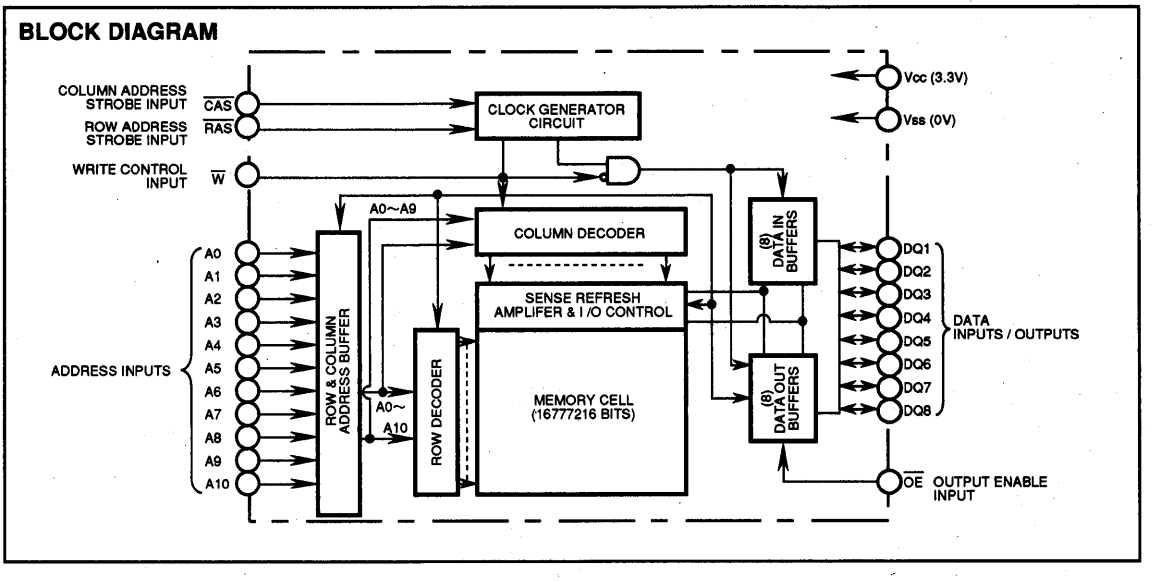
The M5M4V17800AJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	−0.5~4.6	V
VI	Input voltage		−0.5~4.6	V
Vo	Output voltage		−0.5~4.6	V
Io	Output current		50	mA
Pd	Power dissipation	Ta = 25℃	1000	mW
Topr	Operating temperature		0~70	℃
Tstg	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		3.6	V
VIL	Low-level input voltage, all inputs	−0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH = −2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL = 2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≦VOUT≦3.3V	−10		10	μA
II	Input current		0V≦VIN≦3.6V, Other inputs pins = 0V	−10		10	μA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4)	M5M4V17800A-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC = tWC = min. output open			120	mA
		M5M4V17800A-7,-7S				105	
ICC2	Supply current from Vcc , stand-by		$\overline{RAS}$ = $\overline{CAS}$ =VIH, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$≧Vcc -0.2V			0.5	
ICC3 (AV)	Average supply current from Vcc refreshing (Note 3)	M5M4V17800A-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH tRC = min. output open			120	mA
		M5M4V17800A-7,-7S				105	
ICC4 (AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M4V17800A-6,-6S	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling tPC = min. output open			70	mA
		M5M4V17800A-7,-7S				60	
ICC6 (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V17800A-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC = min. output open			120	mA
		M5M4V17800A-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: ICC1 (AV), ICC3 (AV), ICC4 (AV) and ICC6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs	VI = Vss f = 1MHz VI = 25mVrms			5	pF
CI ($\overline{OE}$)	Input capacitance, $\overline{OE}$ input				7	pF
CI ($\overline{W}$)	Input capacitance, write control input				7	pF
CI ($\overline{RAS}$)	Input capacitance, $\overline{RAS}$ input				7	pF
CI ($\overline{CAS}$)	Input capacitance, $\overline{CAS}$ input				7	pF
CI/O	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits				Unit
			M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		60		70	ns
tAA	Columu address access time	(Note 6,9)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	15	ns

Note 5 : An initial pause of 500 μ s is required after power-up followed by a minimum of eight initiallzation cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.

7 : Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max).

8 : Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9 : Assumes that $t_{RAD} \geqq t_{RAD}$ (max) and $t_{ASC} \leqq t_{ASC}$ (max).

10 : Assumes that $t_{CP} \leqq t_{CP}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max).

11 : t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq$ I±10 μ AI) and is not reference to V_{OH} (min) or V_{OL} (max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits				Unit
			M5M4V178A00-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			32		32	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note18)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note18)	15		15		ns
tT	Transition time	(Note19)	1	50	1	50	ns

Note 12 : The timing requirements are assumed t_T =5ns.

13 : V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

14 : t_{RCD} (max) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max), access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC} or t_{AA}. t_{RCD} (min) is specified as t_{RCD} (min) = t_{RAH} (min) + 2t_H + t_{ASC} (min).

15 : t_{RAD} (max) is specified as a reference point only. If $t_{RAD} \geqq t_{RAD}$ (max) and $t_{ASC} \leqq t_{ASC}$ (max), access time is controlled exclusively by t_{AA}.

16 : t_{ASC} (max) is specified as a reference point only. If $t_{RCD} \geqq t_{RCD}$ (max) and $t_{ASC} \geqq t_{ASC}$ (max), access time is controlled exclusively by t_{CAC}.

17 : Either t_{DZC} or t_{DZO} must be satisfied.

18 : Either t_{CDD} or t_{ODD} must be satisfied.

19 : t_T is measured between V_{IH} (min) and V_{IL} (max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low	(Note 20)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low	(Note 20)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 20 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note21)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note22)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note22)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note22)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 21 : t_{RWC} is specified as t_{RWC} (min) = t_{RAC} (max) + t_{ODD} (min) + t_{RWL} (min) + t_{RP} (min) + 5t_T.

22 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS}$ (min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits				Unit
			M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note24)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note25)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note22)	60		65		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24 : t_{RAS} (min) is specified as two cycles of $\overline{CAS}$ input are performed.

25 : t_{CP} (max) is specified as a reference point only.

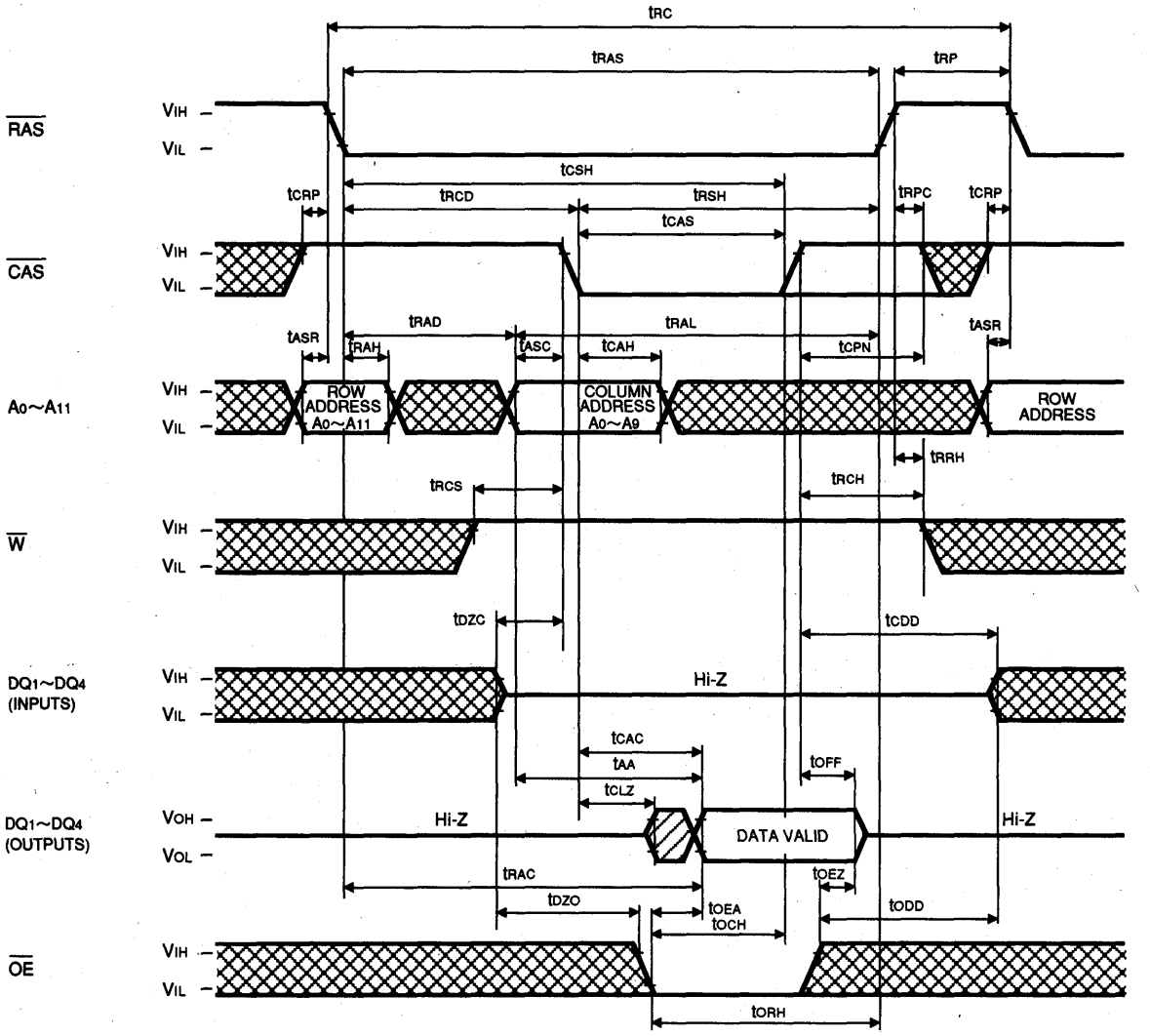
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 26 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 27)

Read Cycle

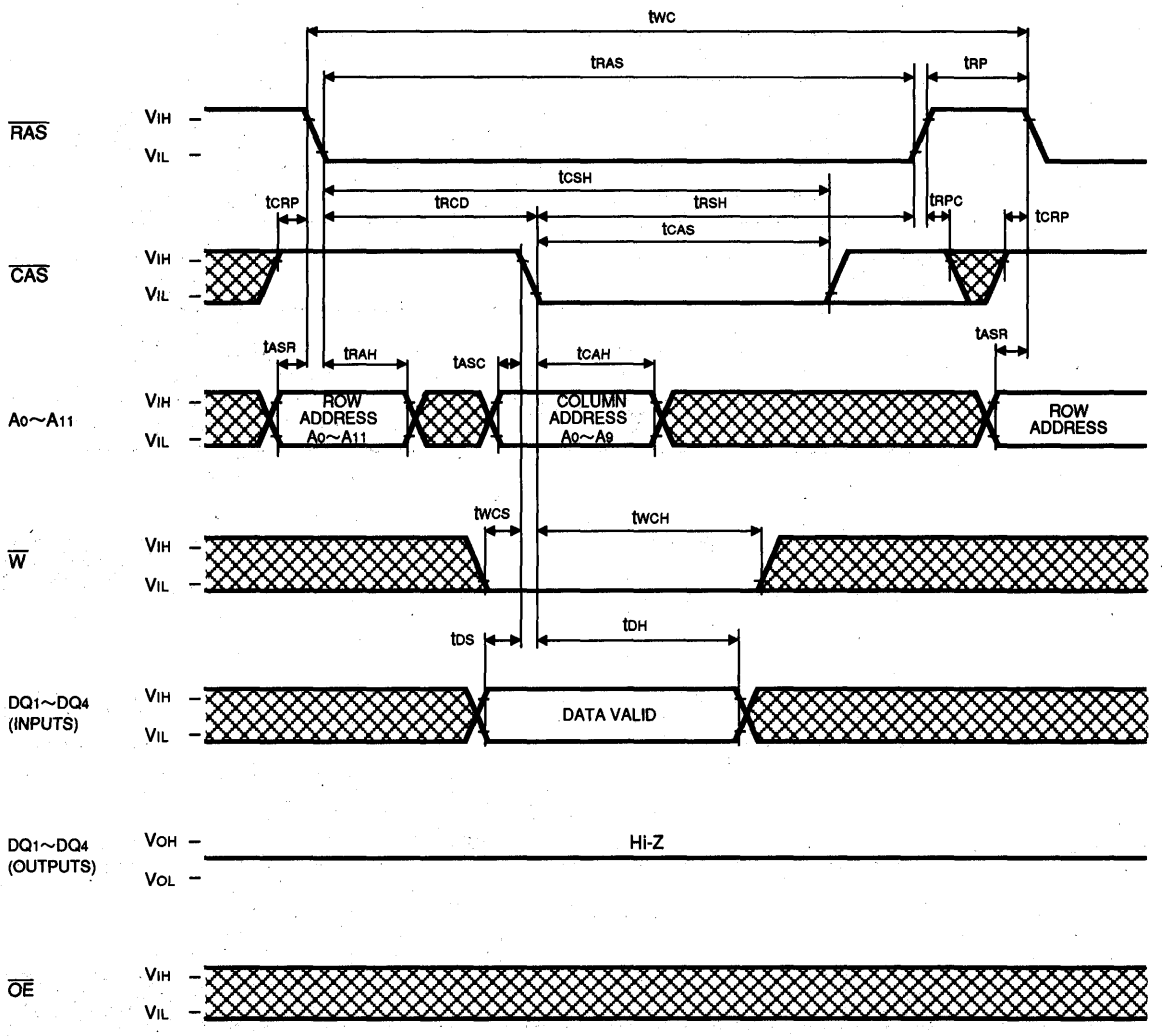


Note 27

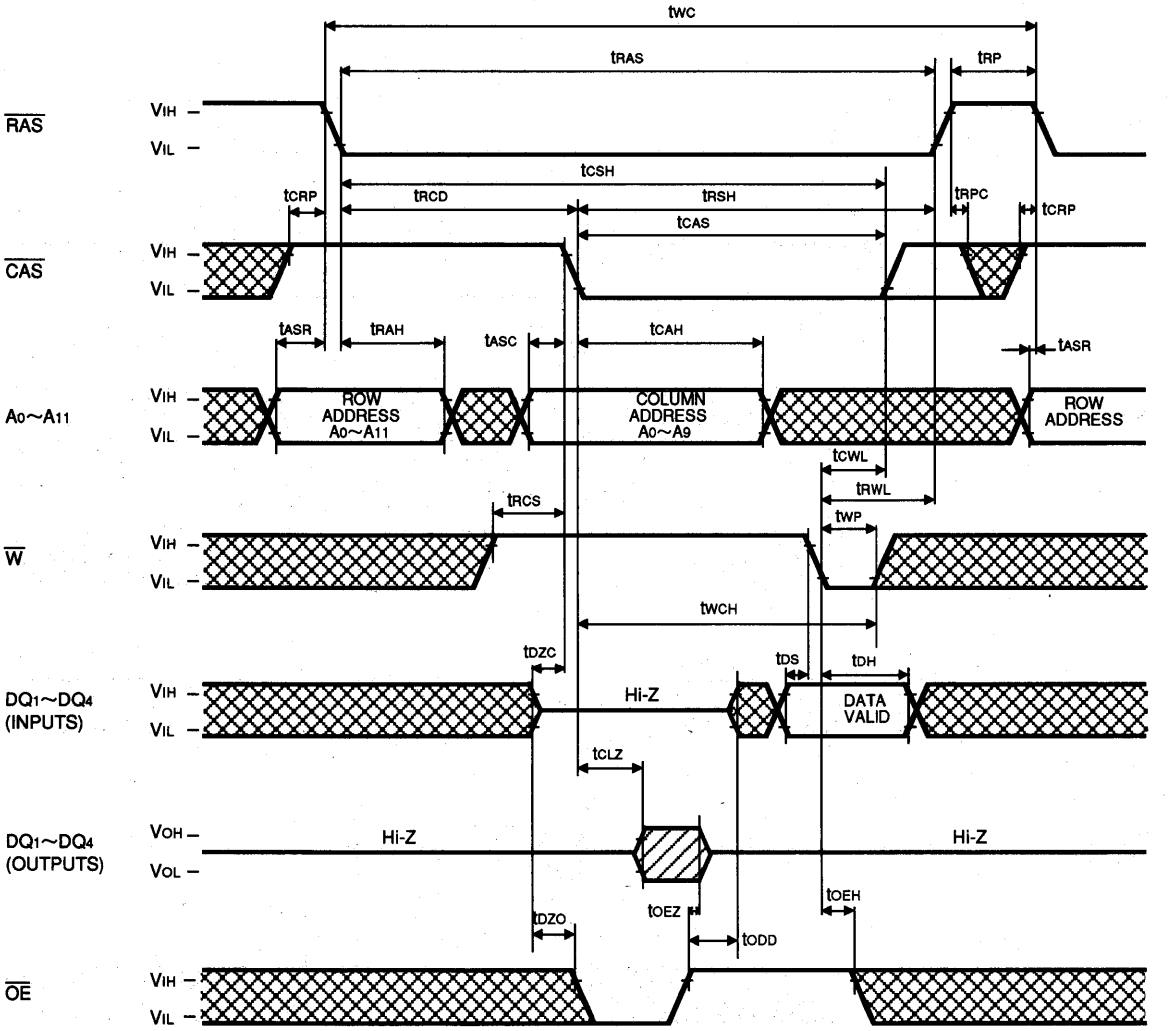
Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

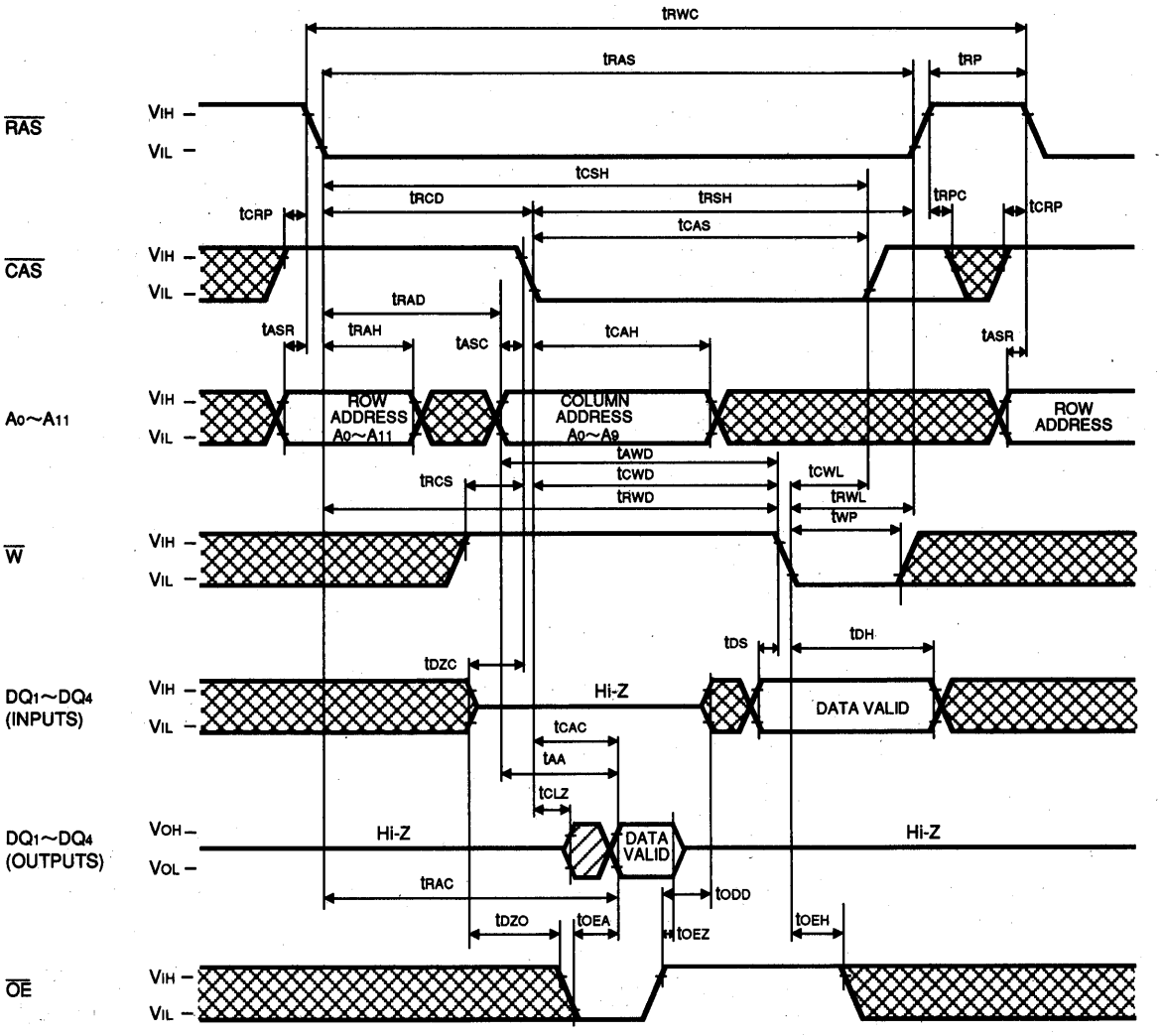
Write Cycle (Early write)



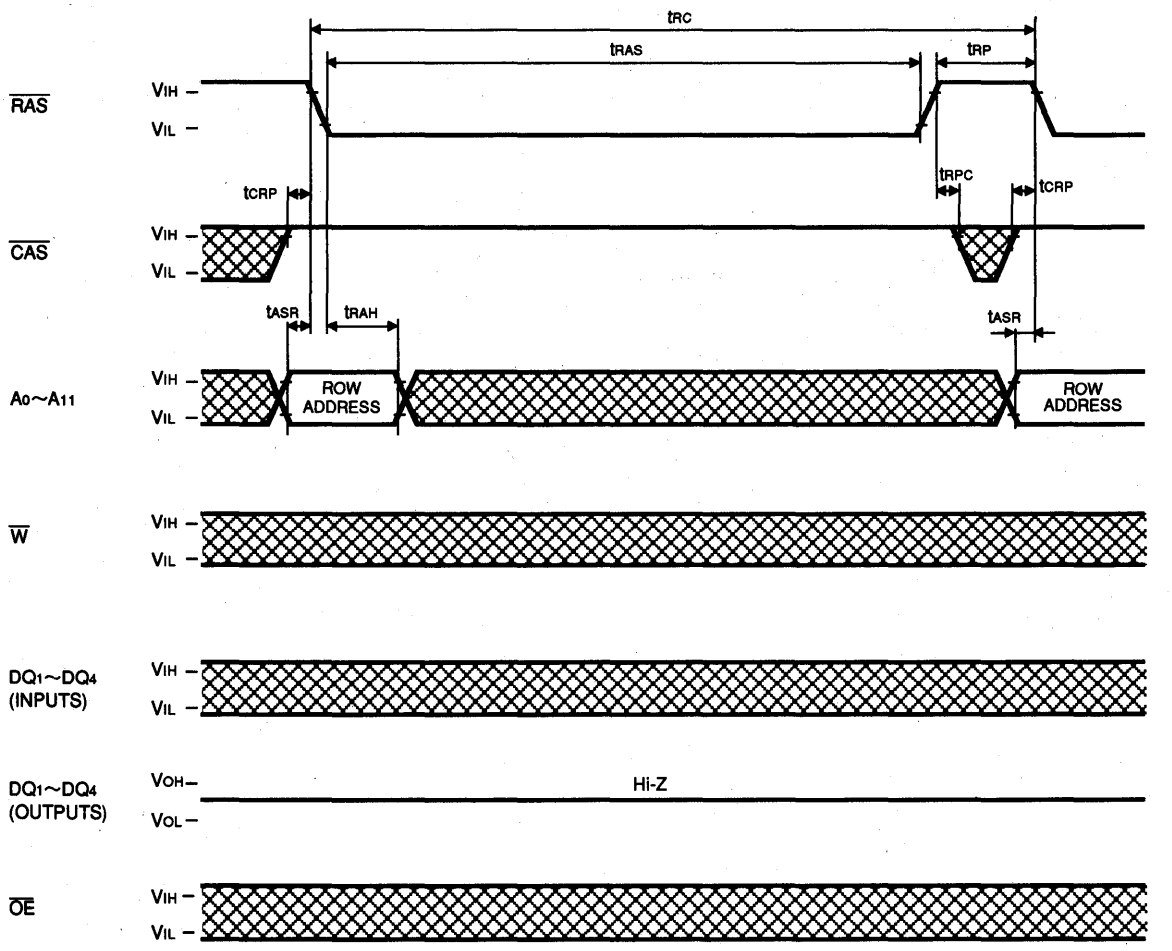
Write Cycle (Delayed write)



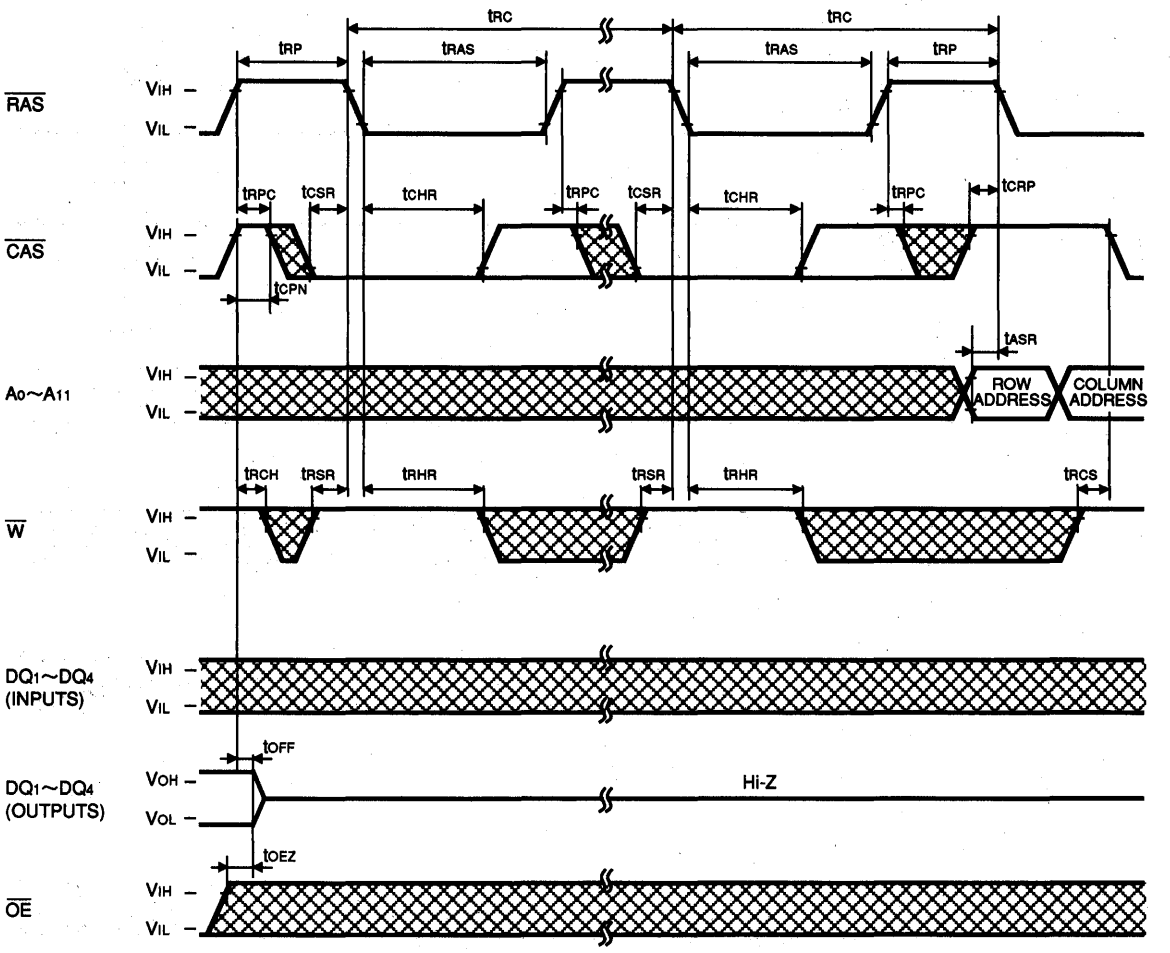
Read-Write, Read-Modify-Write Cycle



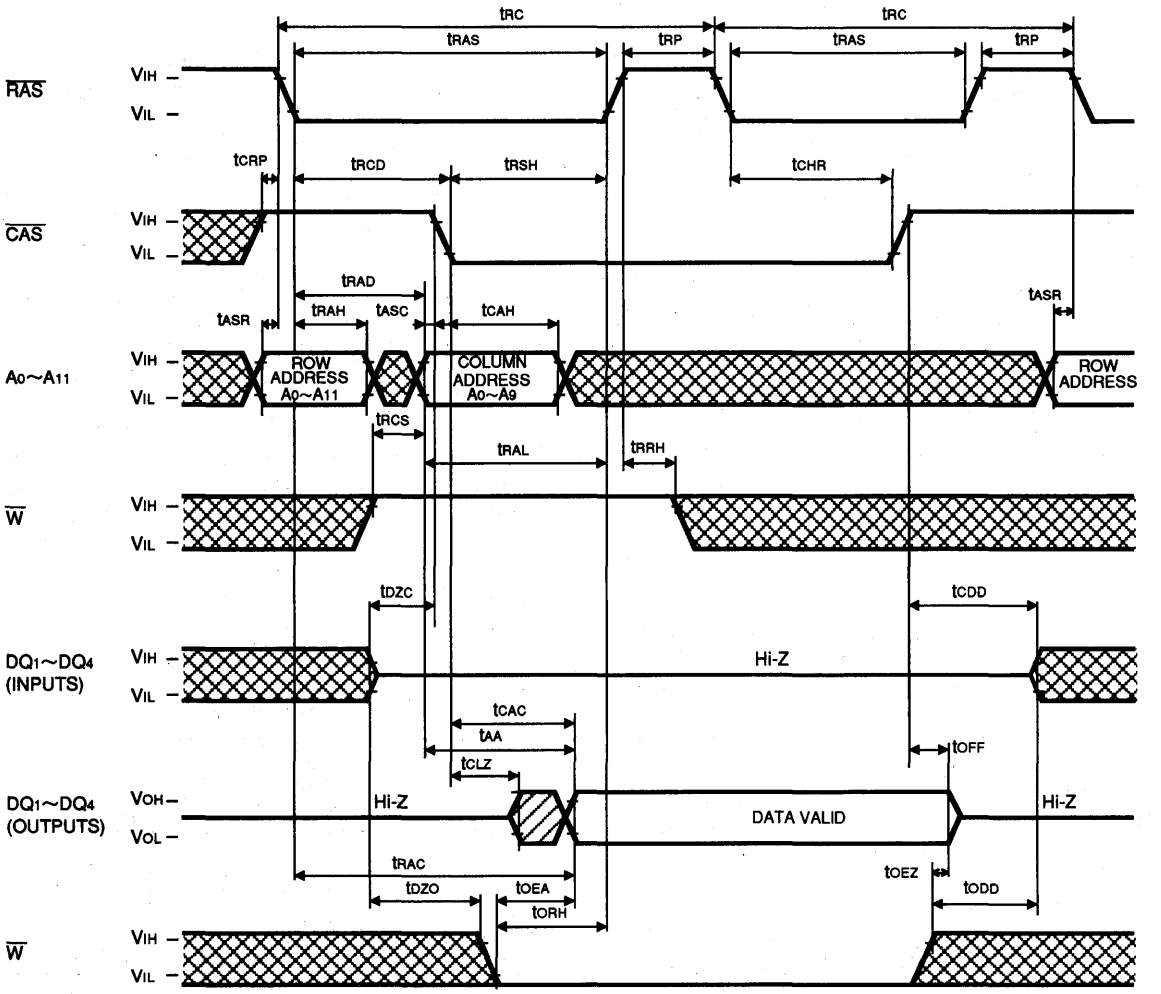
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

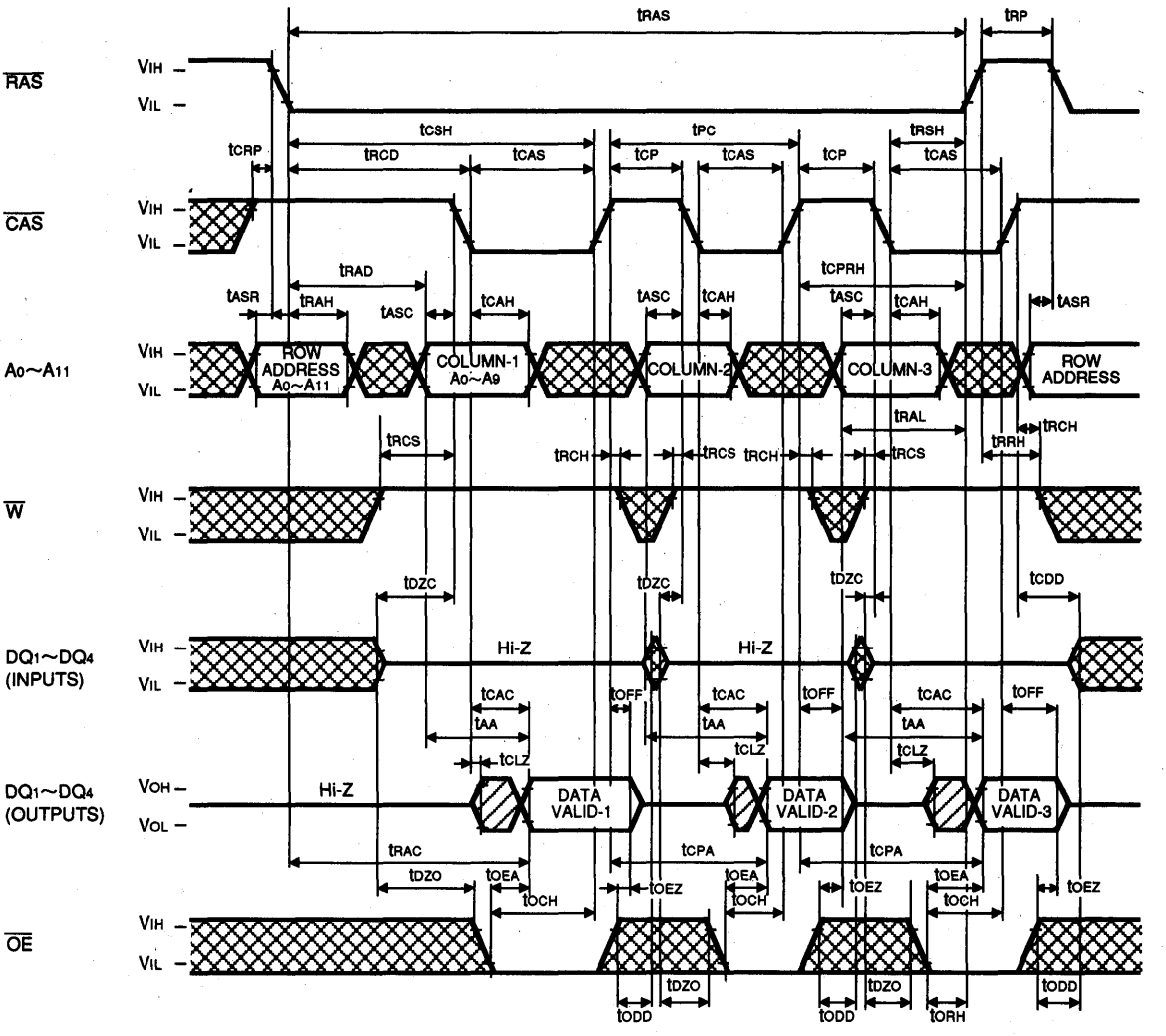


Hidden Refresh Cycle (Read) (Note 28)

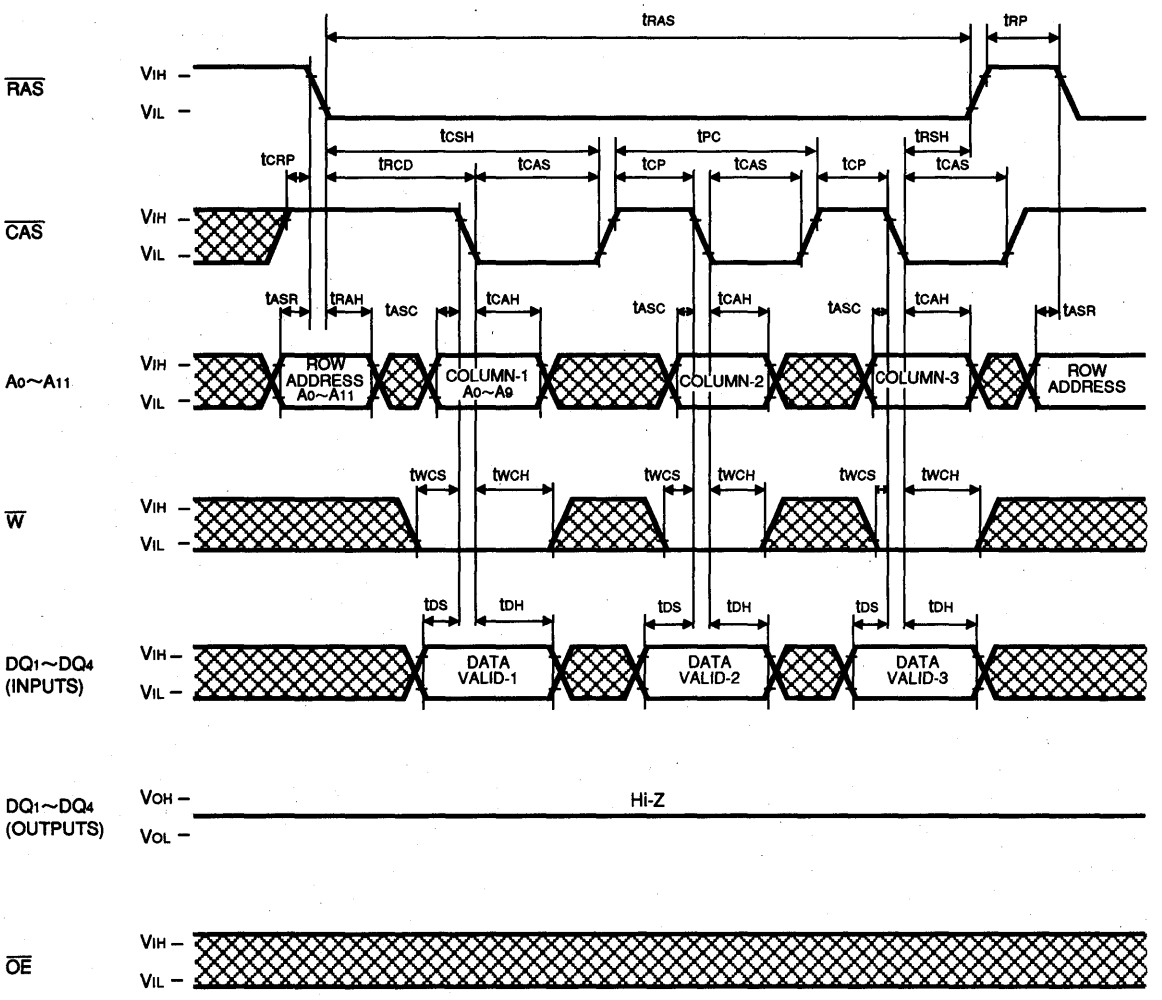


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

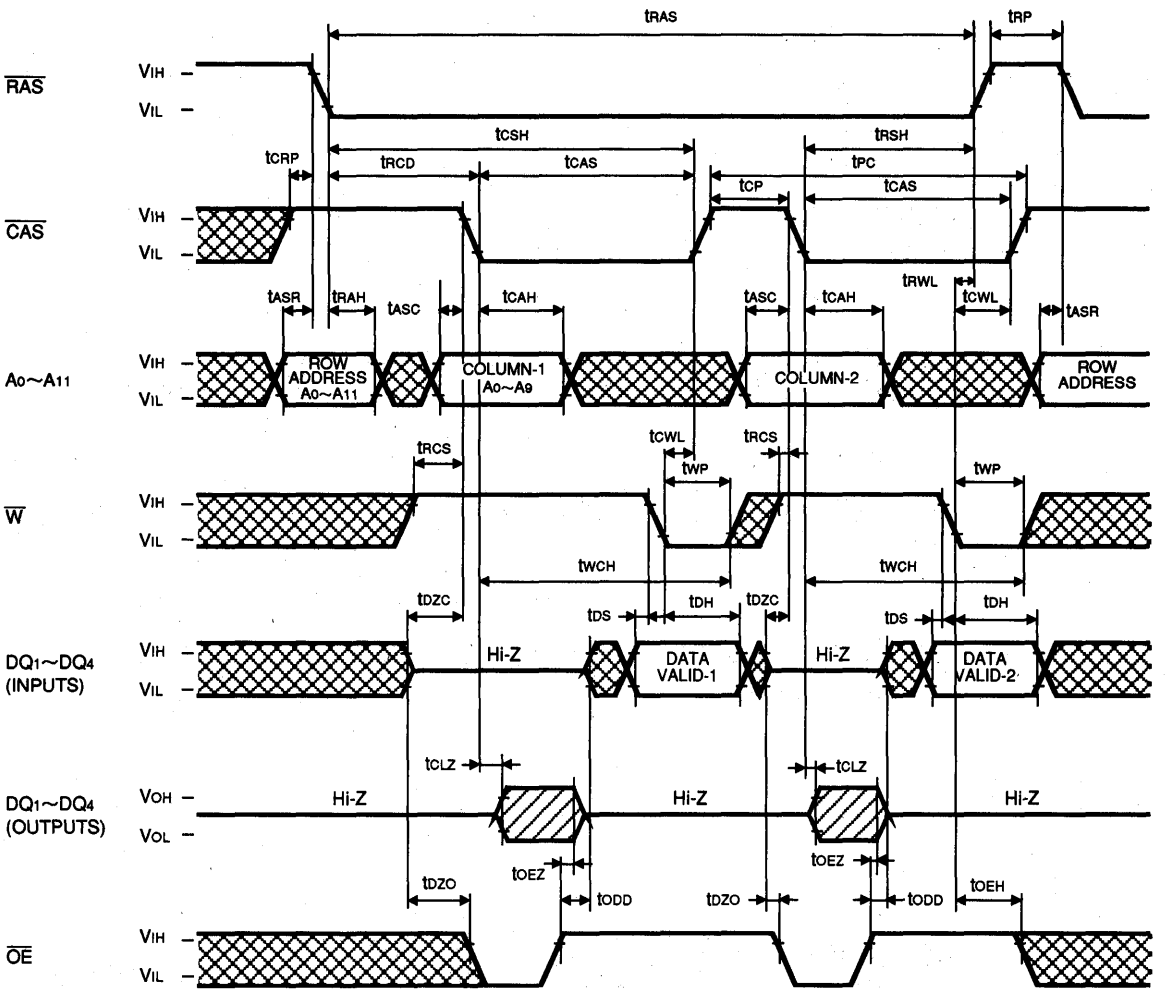
Fast Page Mode Read Cycle



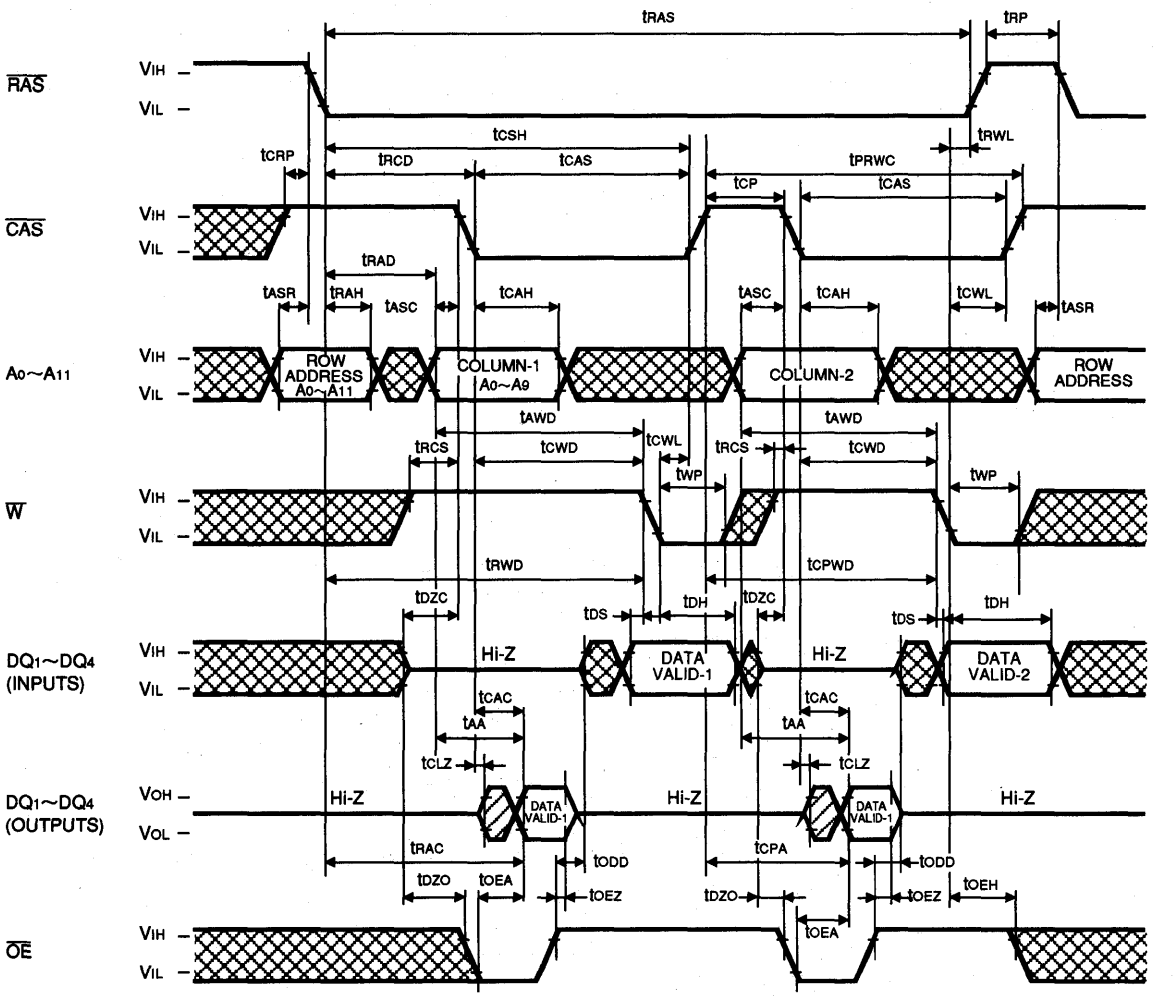
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



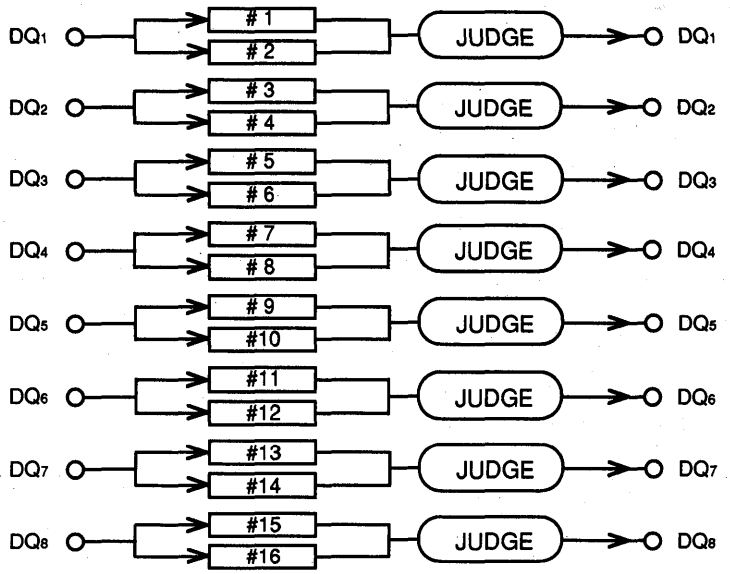
Fast Page Mode Read-Write, Read-Modify-Write Cycle



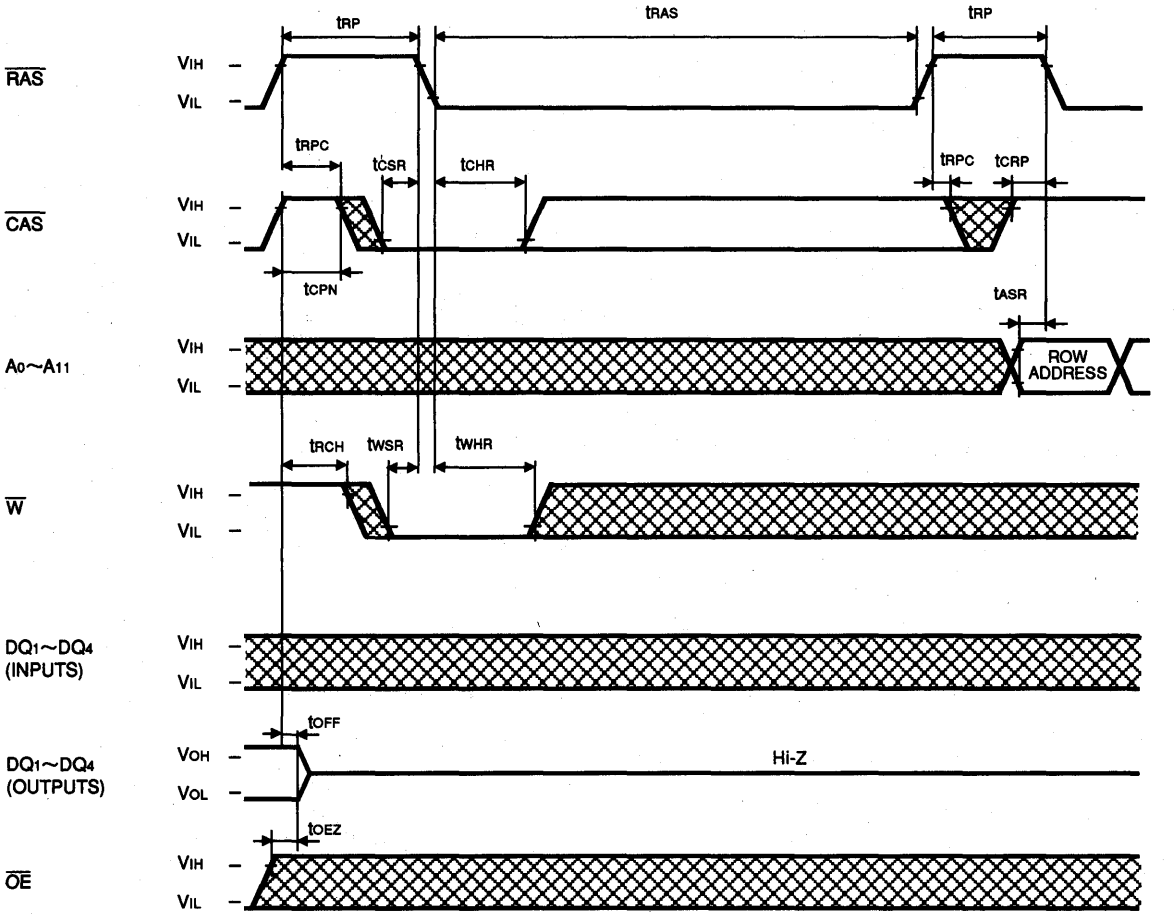
TEST Mode SET Cycle

Symbol	Parameter	Limits				Unit
		M5M4V17800A-6,-6S		M5M4V17800A-7,-7S		
		Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 29 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.



TEST Mode SET Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC9\ (AV)}$	Average supply current from Vcc Self-Refresh cycle	M5M4V17800A (S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			200	μA

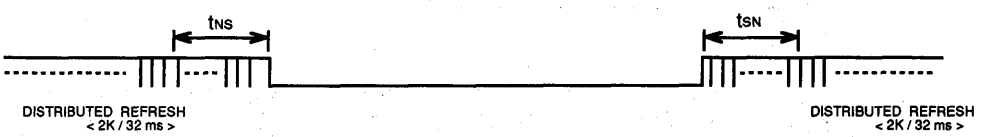
TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 3.3V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits				Unit
		M5M4V17800A-6S		M5M4V17800A-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

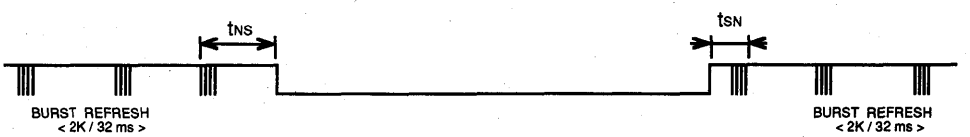
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} ≦ 32 ms and t_{SN} ≦ 32 ms.

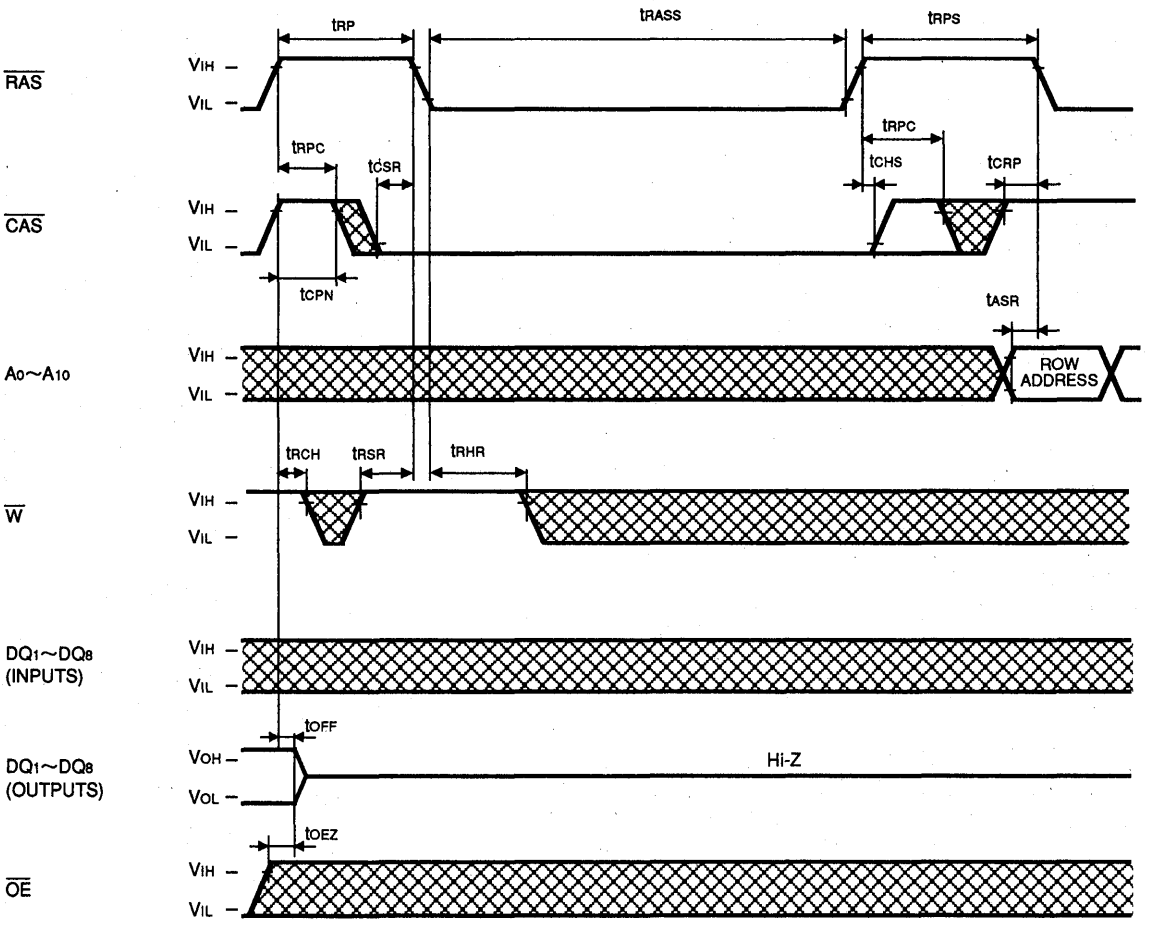


(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} + t_{SN} ≦ 32 ms.



Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17800CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17800CXX-5,-5S	50	13	25	13	90	435
M5M4V17800CXX-6,-6S	60	15	30	15	110	360
M5M4V17800CXX-7,-7S	70	20	35	20	130	315

XX=J,TP

- Standard 28pin SOJ, 28pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.8mW (Max) ---------- CMOS Input level
  - 0.72mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M4V17800Cxx-5,-5S ---------- 525.0mW (Max)
  - M5M4V17800Cxx-6,-6S ---------- 435.0mW (Max)
  - M5M4V17800Cxx-7,-7S ---------- 380.0mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 200.0μA(Max)
- Fast-page mode, Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})
  * Applicable to self refresh version (M5M4V17800CJ,TP-5S,-6S, -7S:option) only

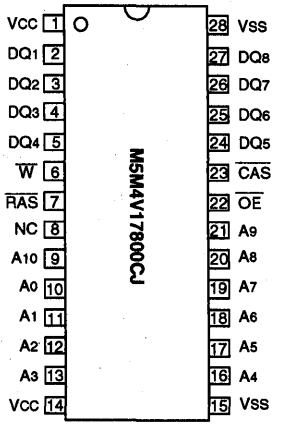
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

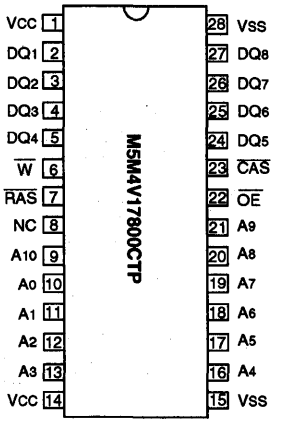
PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+3.3V)
V_{SS}	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC:NO CONNECTION

MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17800CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

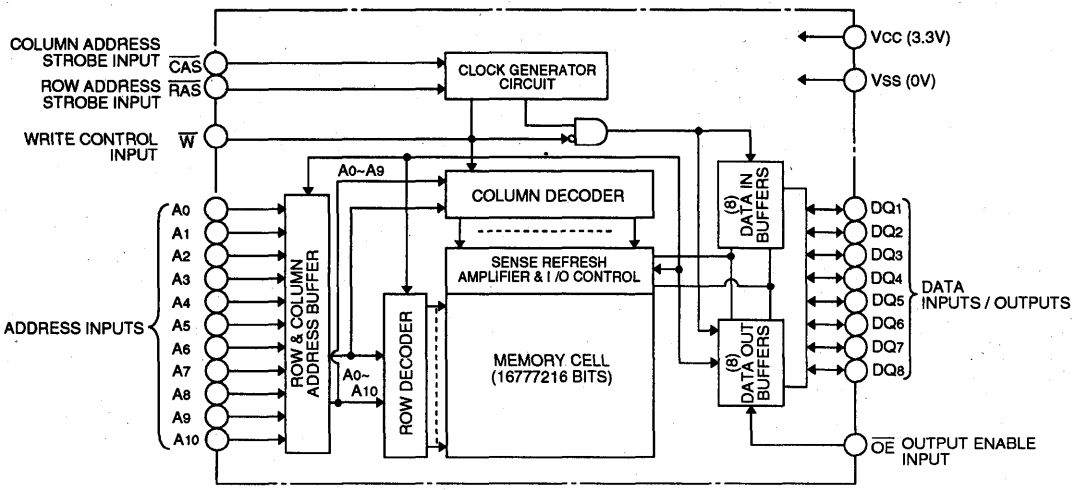
The M5M4V17800CJ, TP provide, in addition to normal read,write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
V_I	Input voltage		-0.5 ~ 4.6	V
V_O	Output voltage		-0.5 ~ 4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : VIL(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to VSS.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M4V17800C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M4V17800C-6,-6S				120	
		M5M4V17800C-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M4V17800C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M4V17800C-6,-6S				120	
		M5M4V17800C-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M4V17800C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V17800C-6,-6S				70	
		M5M4V17800C-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V17800C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M4V17800C-6,-6S				120	
		M5M4V17800C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=3.3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/output capacitance, data ports				8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.

6:Measured with a load circuit equivalent to 2TTL loads and 100pF. The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

7:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max).

8:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9:Assumes that tRAD≧tRAD(max) and tASC≦tASC(max).

10:Assumes that tCP≦tCP(max) and tASC≧tASC(max).

11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦|±10 μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.

13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).

15:tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

16:tASC(max) is specified as a reference point only. If tRCD ≧tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

17:Either tDZC or tDZO must be satisfied.

18:Either tCDD or tODD must be satisfied.

19:tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low (Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low (Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 5)	**M5M4V17800C (S)**	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leqq 0.2V$ $\overline{OE}$ & $\overline{WE} \leqq 0.2V$ or $\overline{OE}$ & $\overline{WE} \geqq Vcc-0.2V$ $A_0 \sim A_{10} \leqq 0.2V$ or $A_0 \sim A_{10} \geqq Vcc-0.2V$ t_{REF}=128ms (2048cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
I_{CC9} (AV) *	Average supply current from Vcc Self-Refresh cycle (Note 5)	**M5M4V17800C (S)**	$\overline{RAS} = \overline{CAS} \leqq 0.2V$ output = OPEN			200	μA

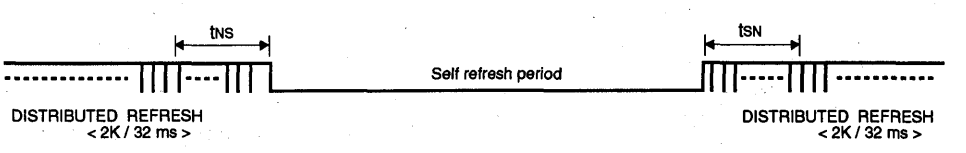
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5S		M5M4V17800C-6S		M5M4V17800C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

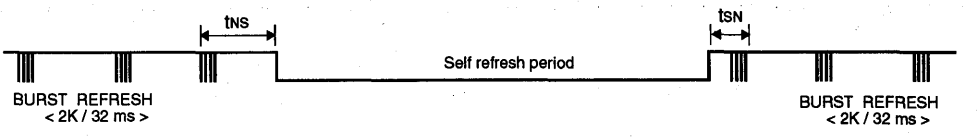
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 32ms$ and $t_{SN} \leqq 32ms$.



(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 32ms$.

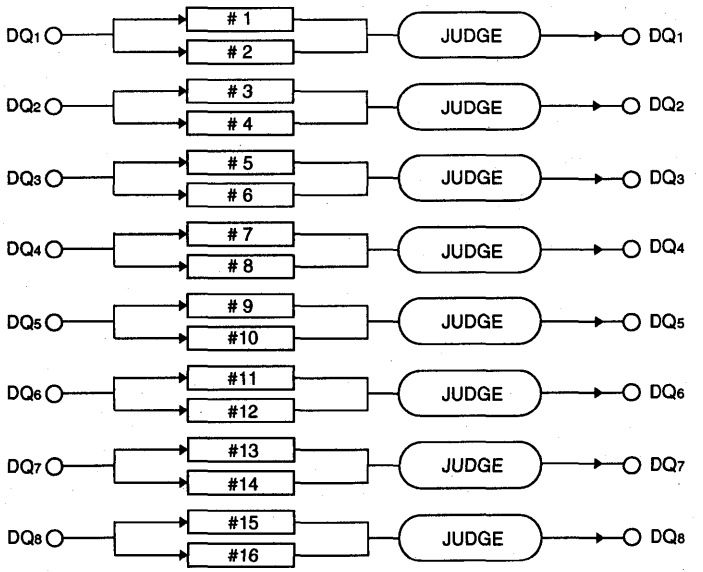


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

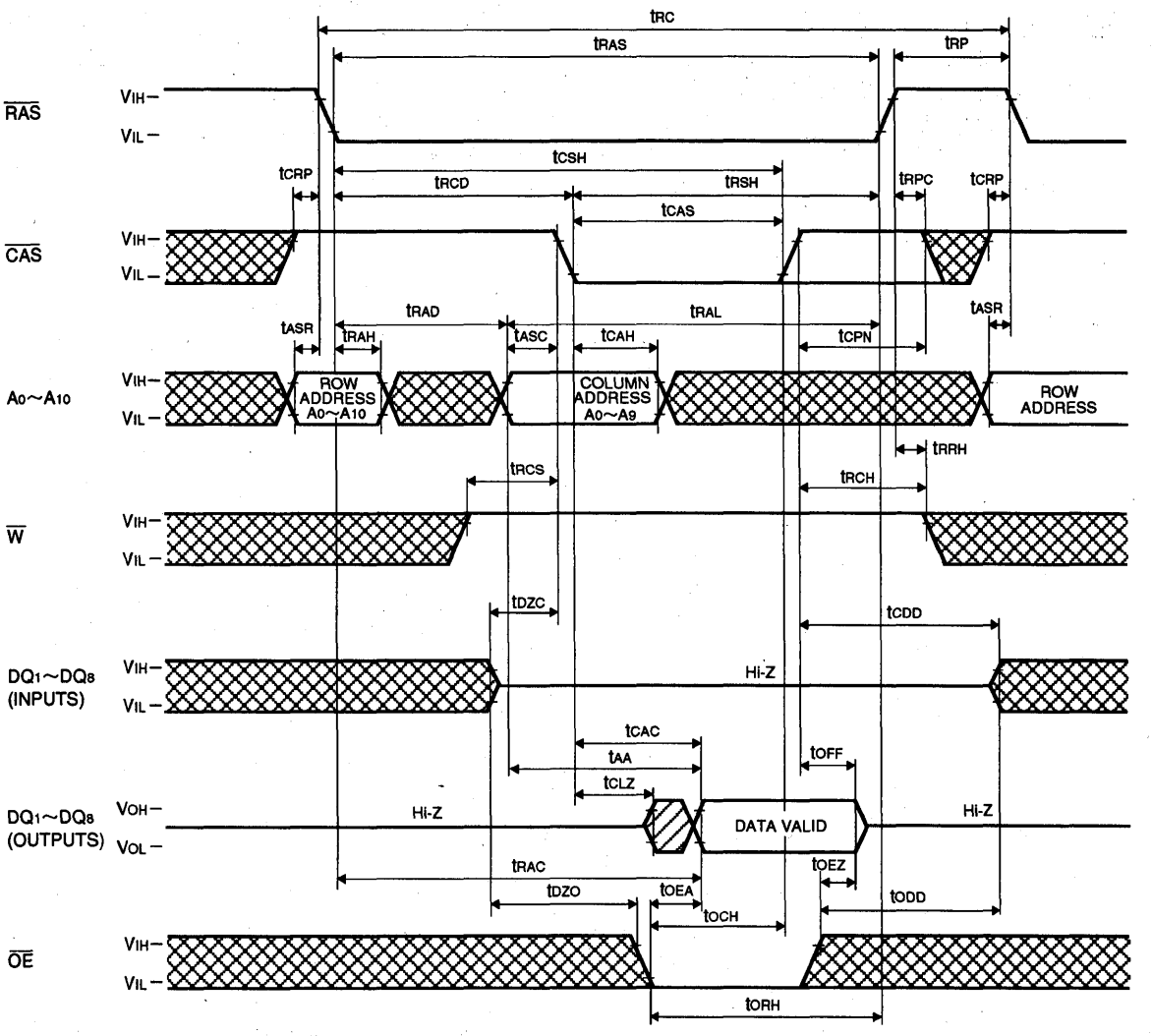
TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M4V17800C-5,-5S		M5M4V17800C-6,-6S		M5M4V17800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 28)
Read Cycle



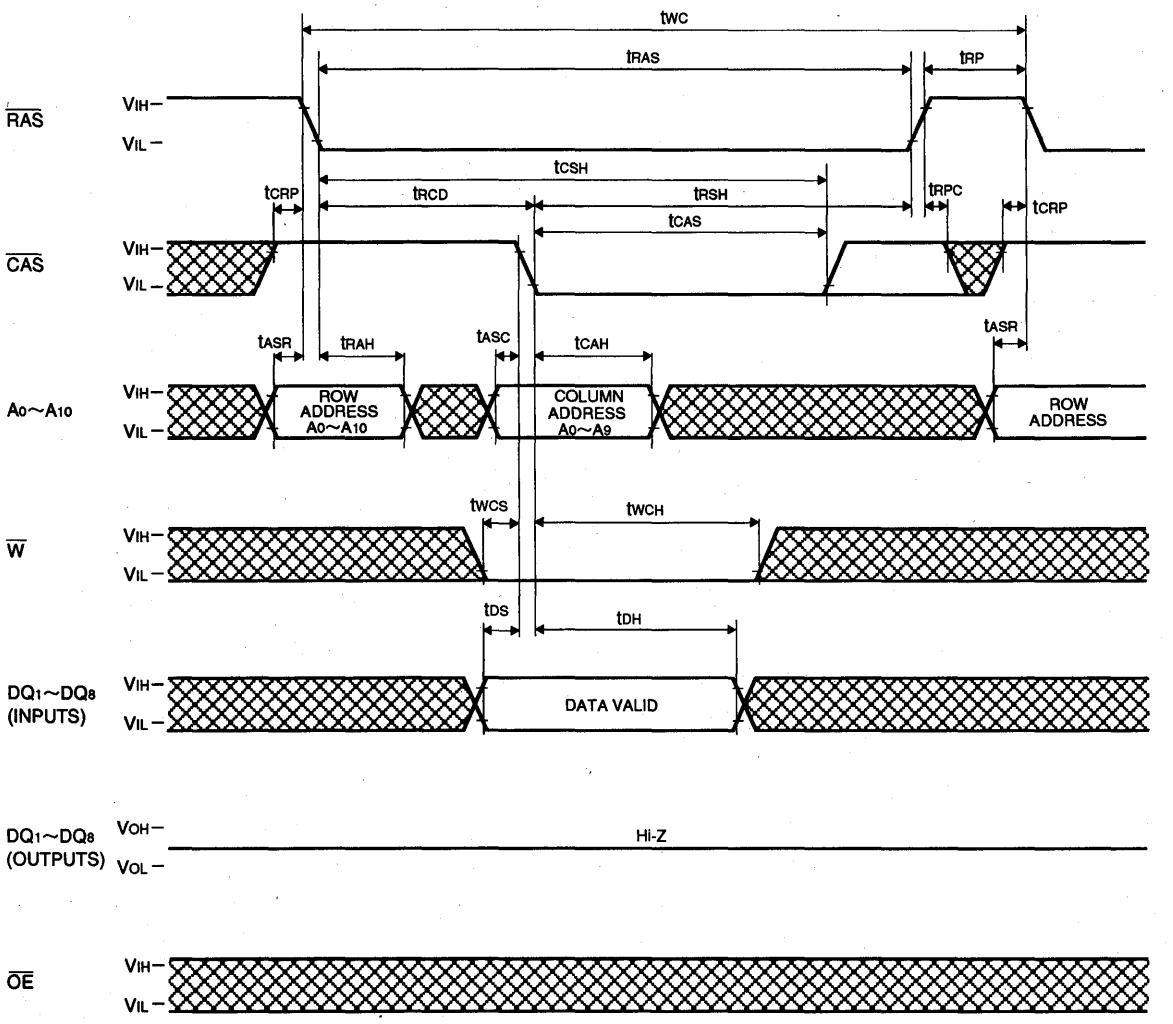
Note 28

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

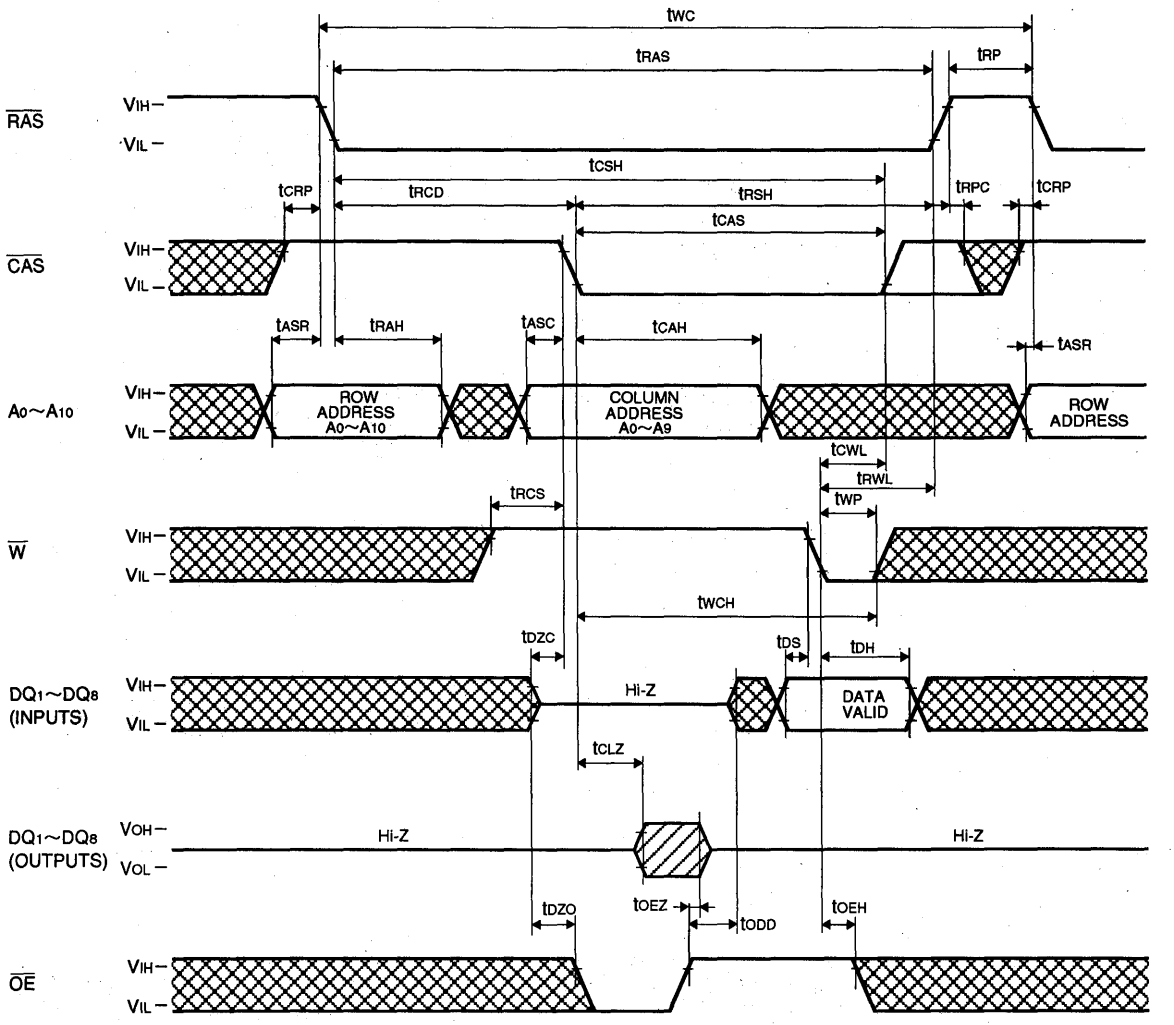
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

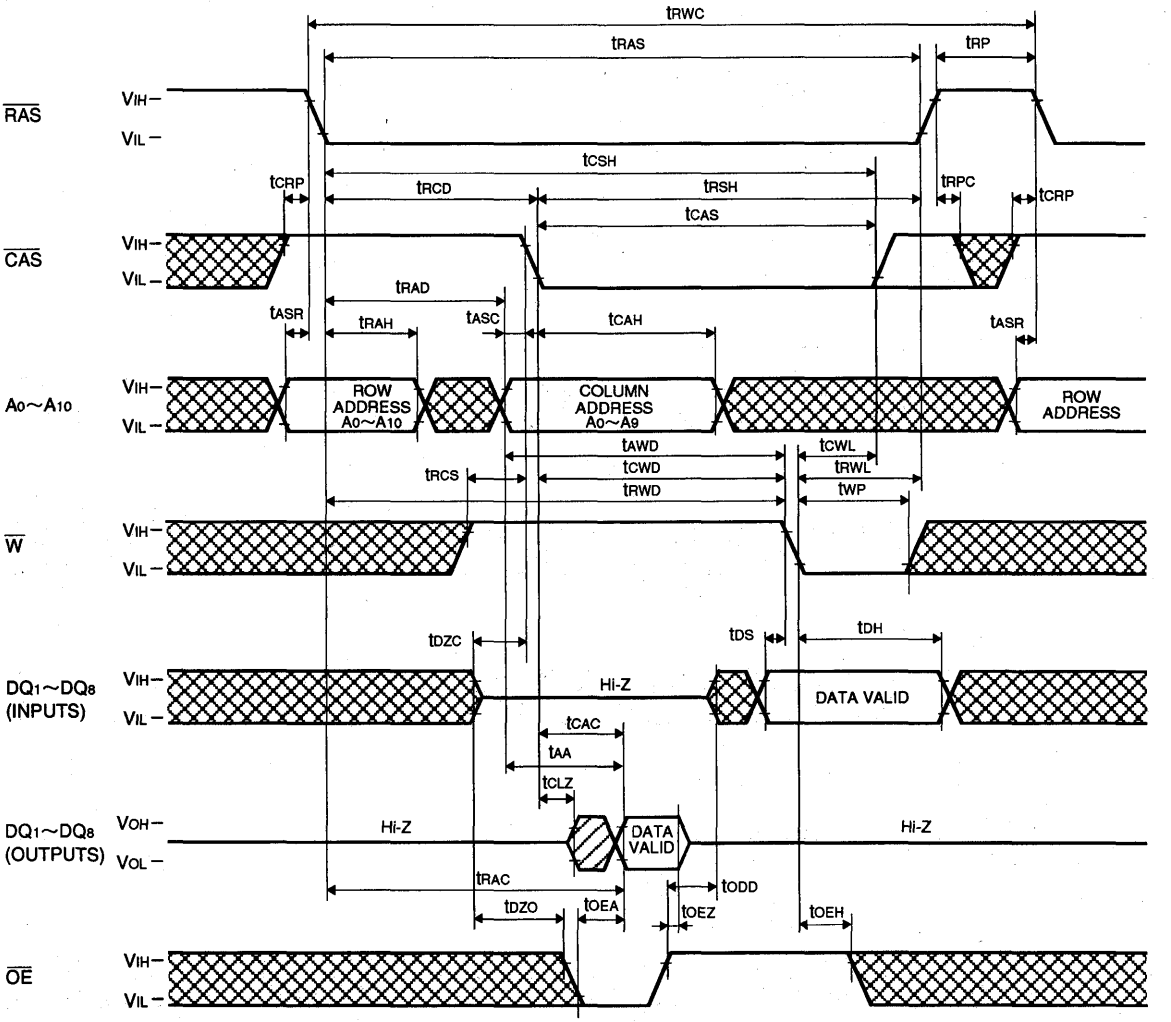
Write Cycle (Early write)



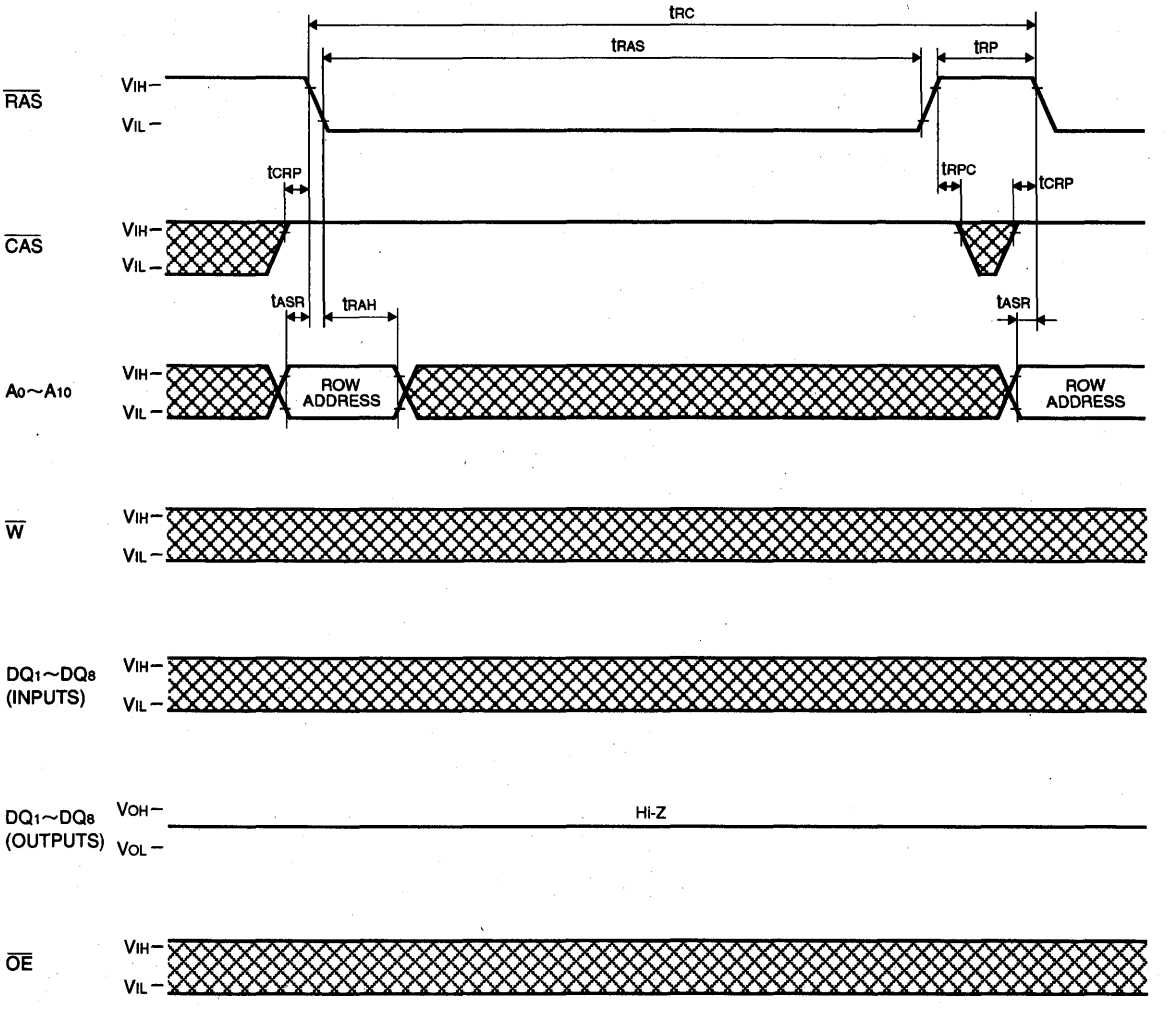
Write Cycle (Delayed write)



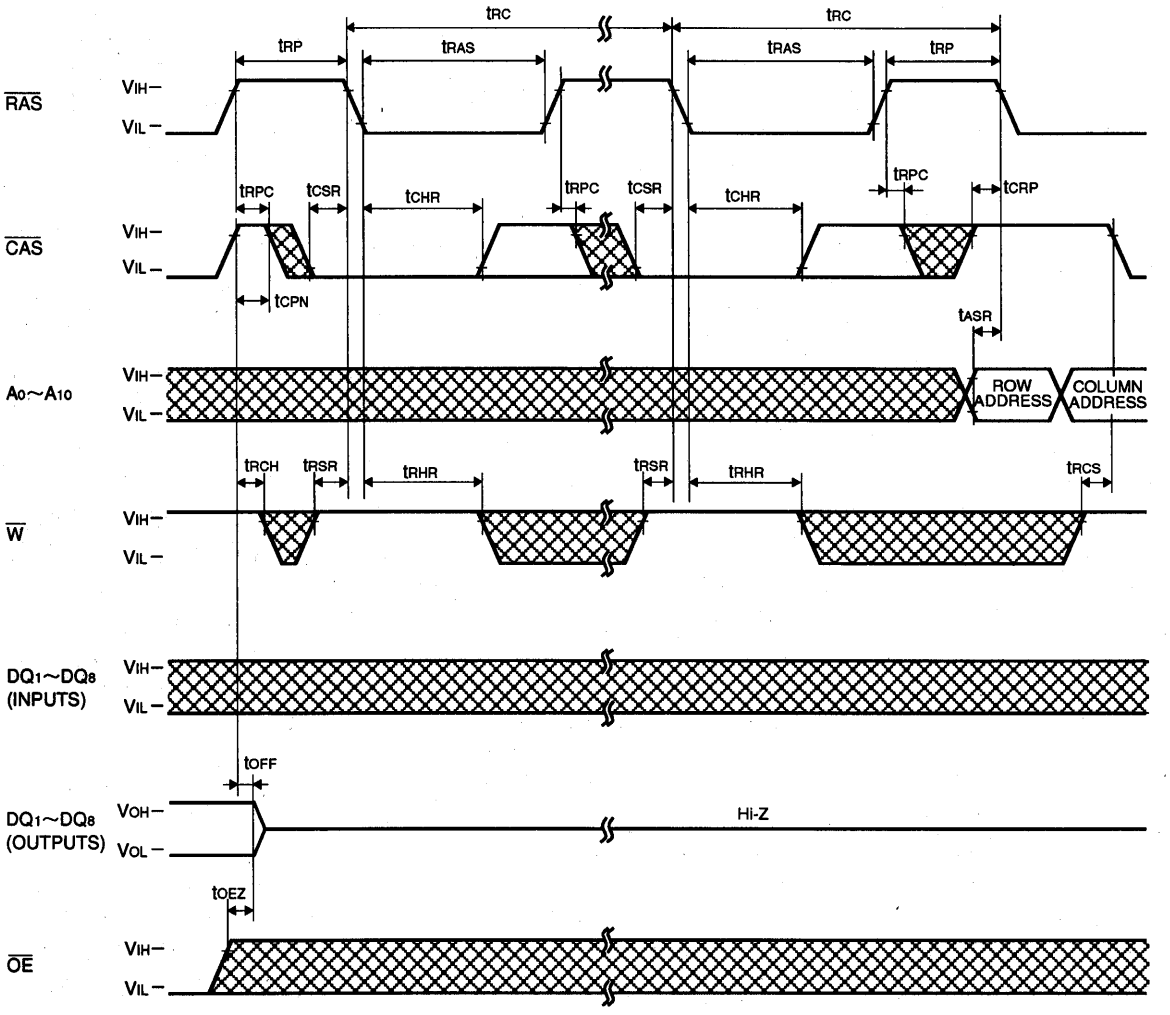
Read-Write, Read-Modify-Write Cycle



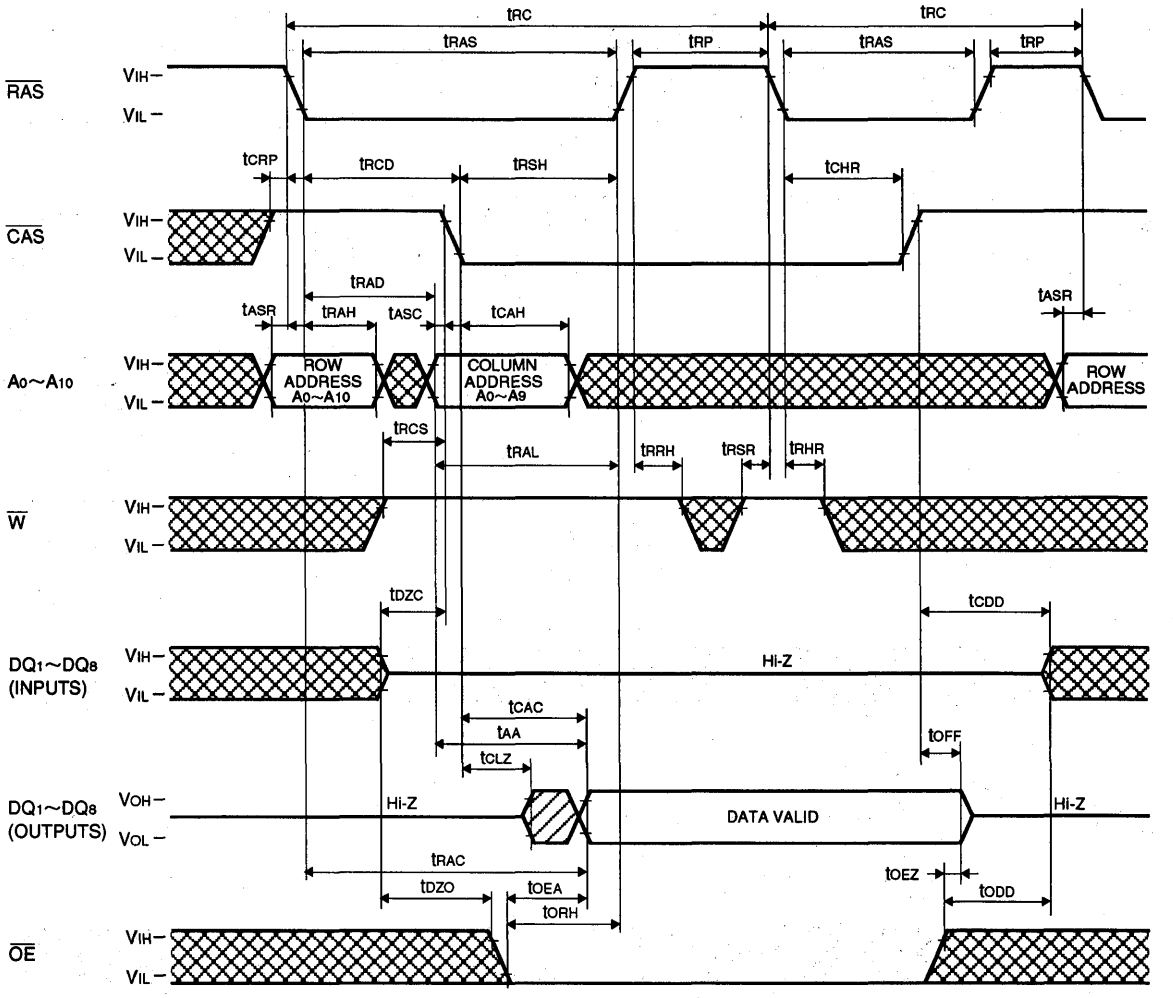
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



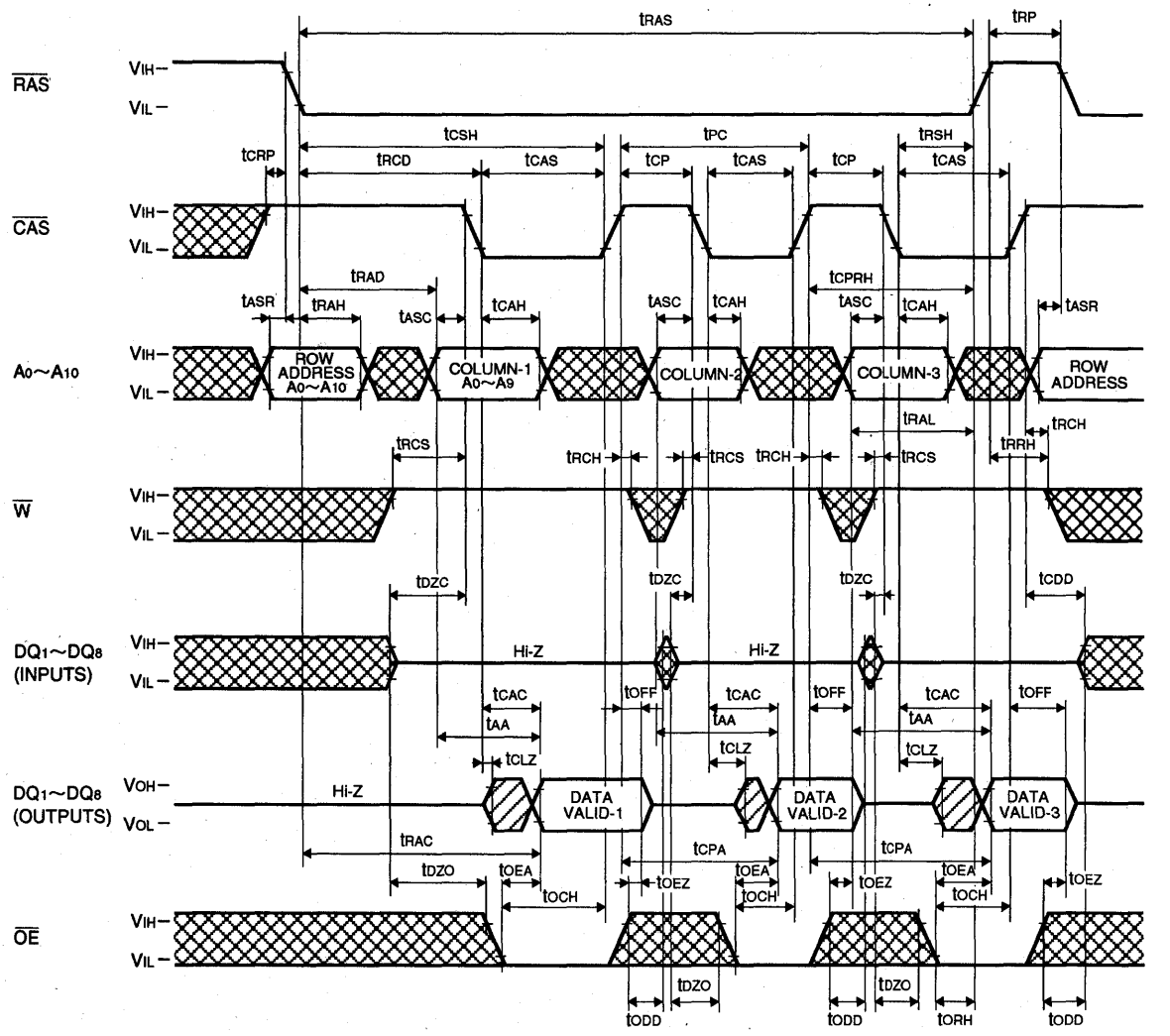
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

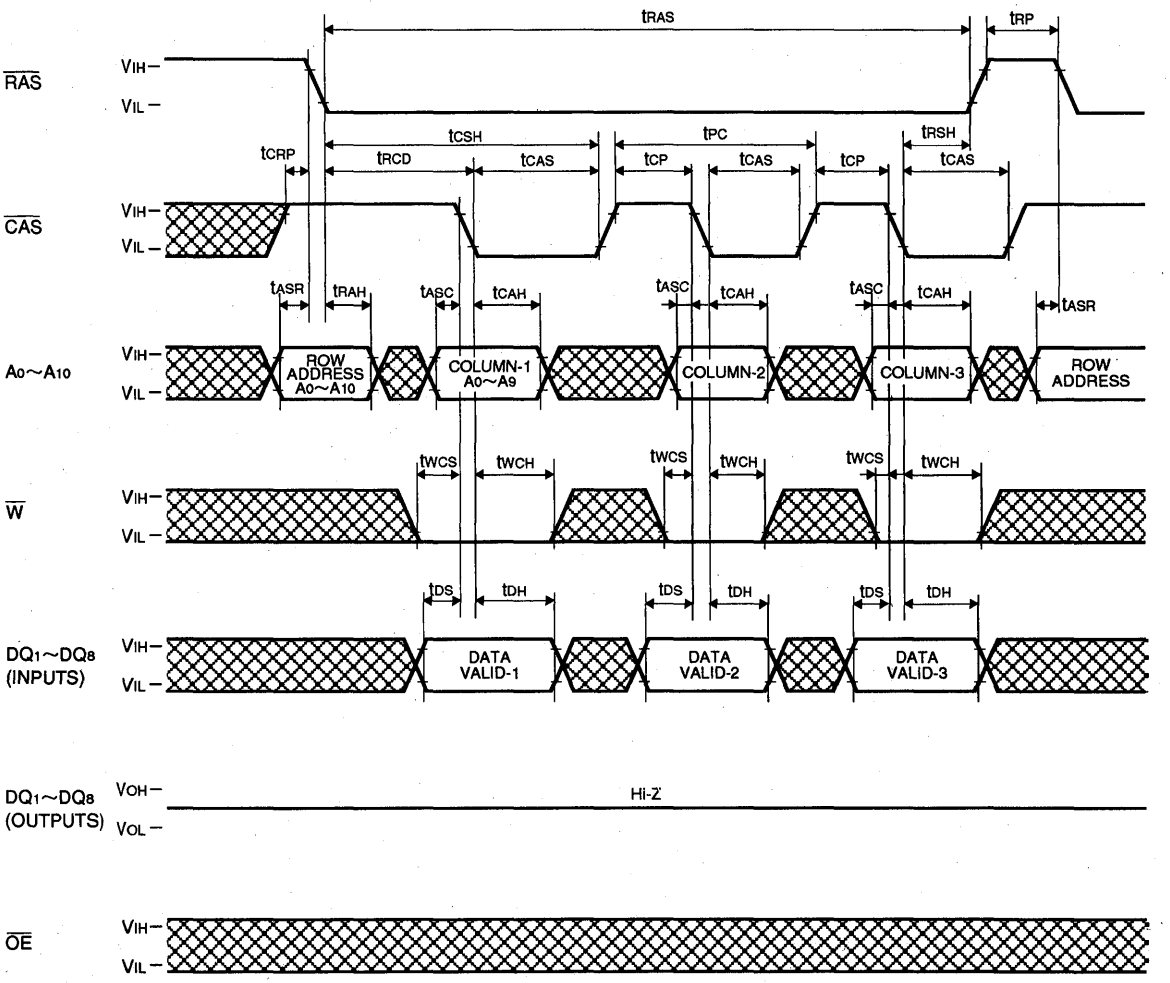
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle

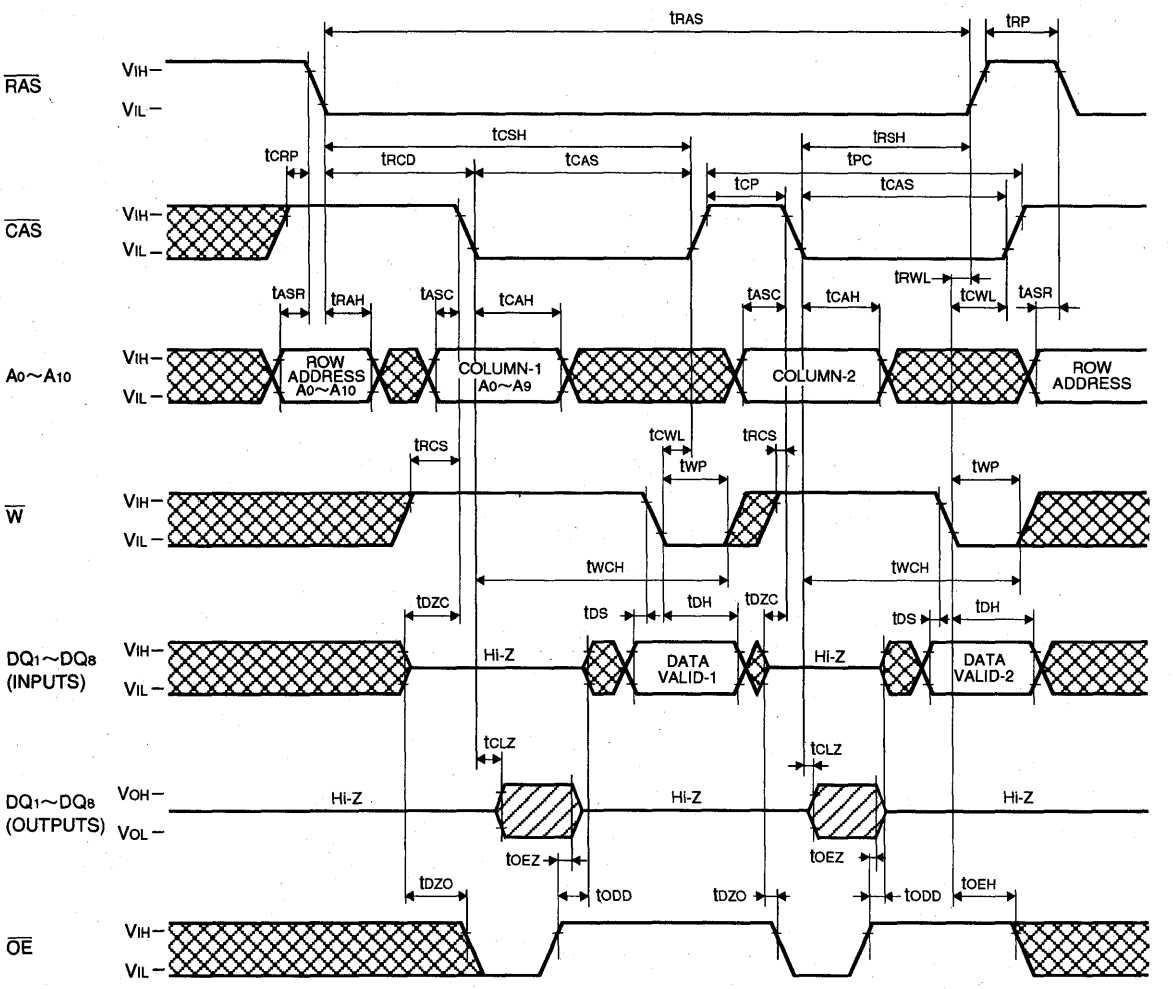


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

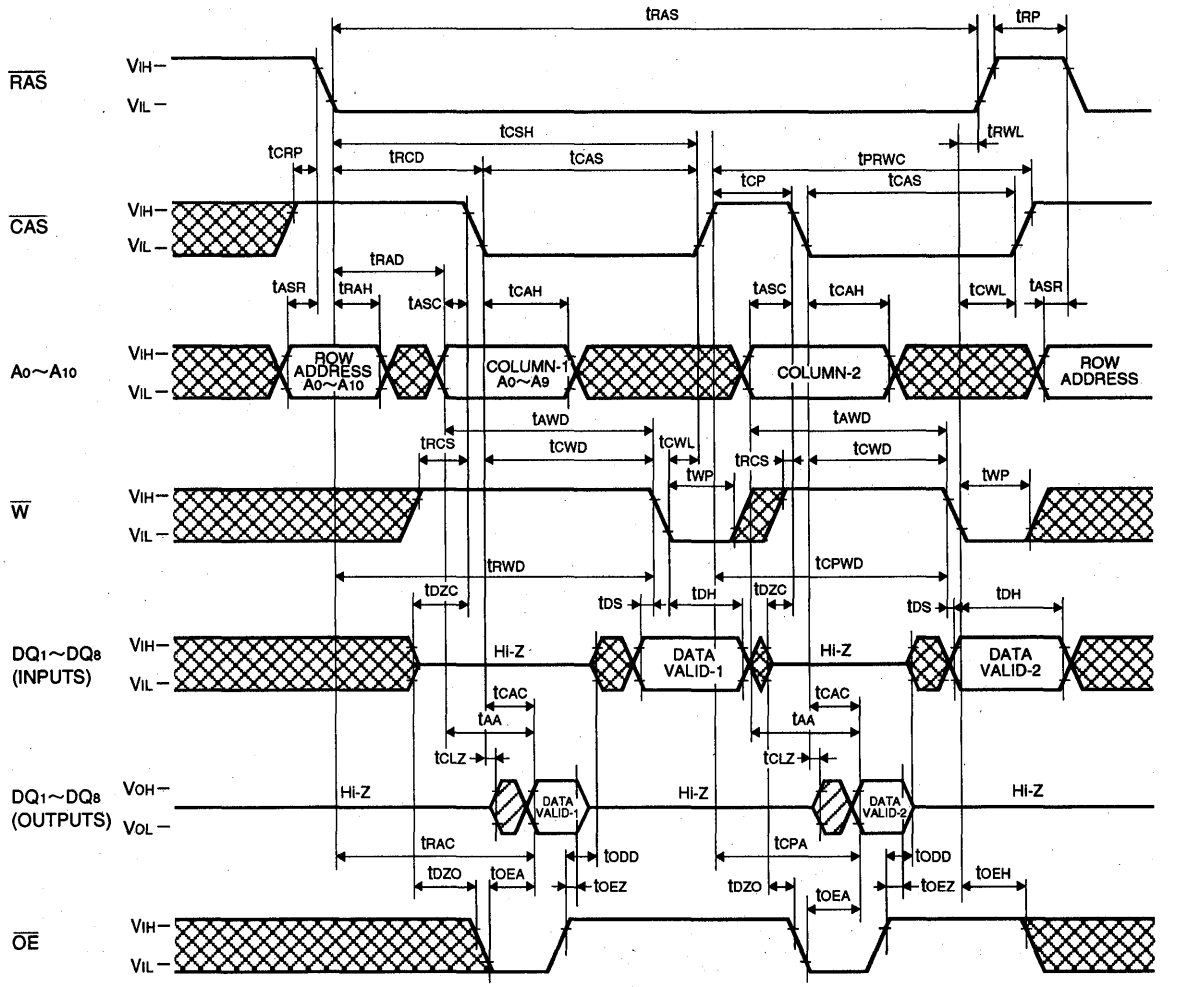
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)

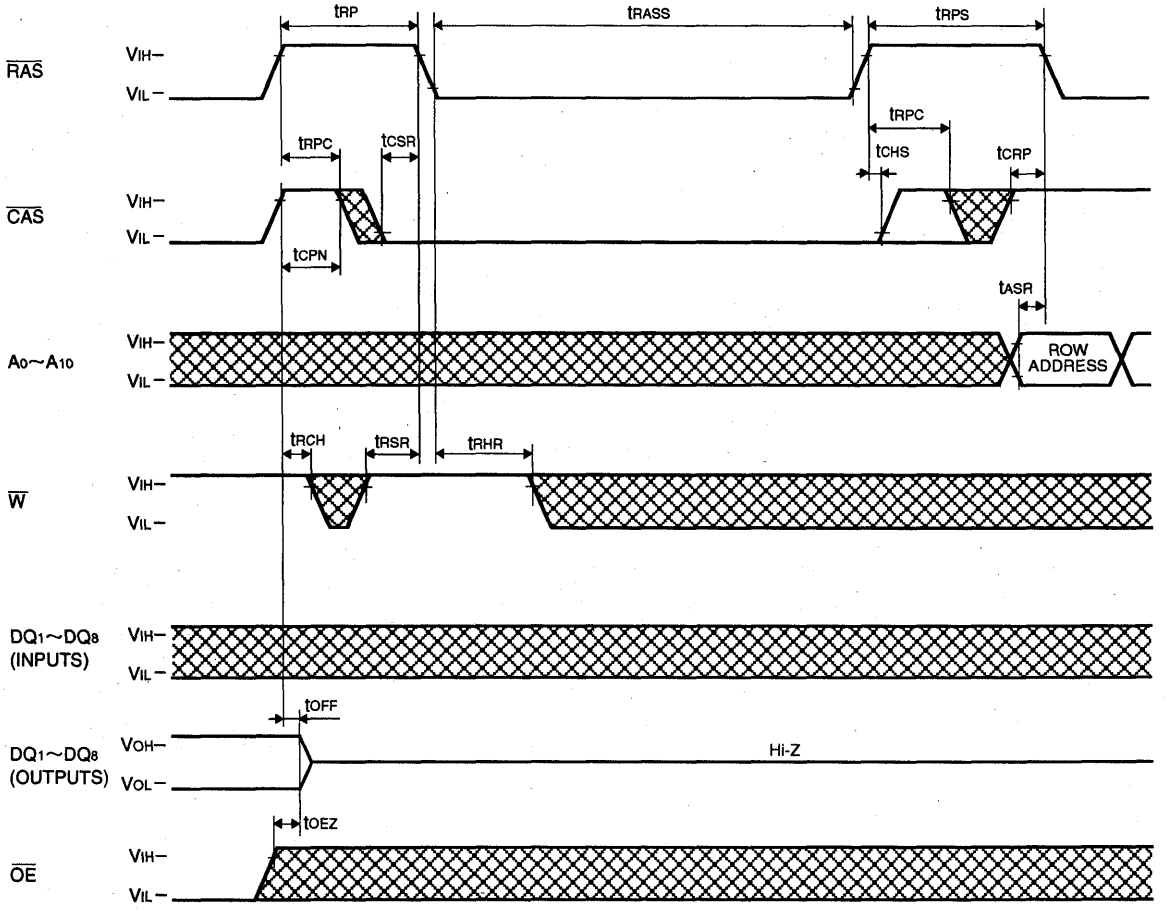


Fast Page Mode Read-Write, Read-Modify-Write Cycle

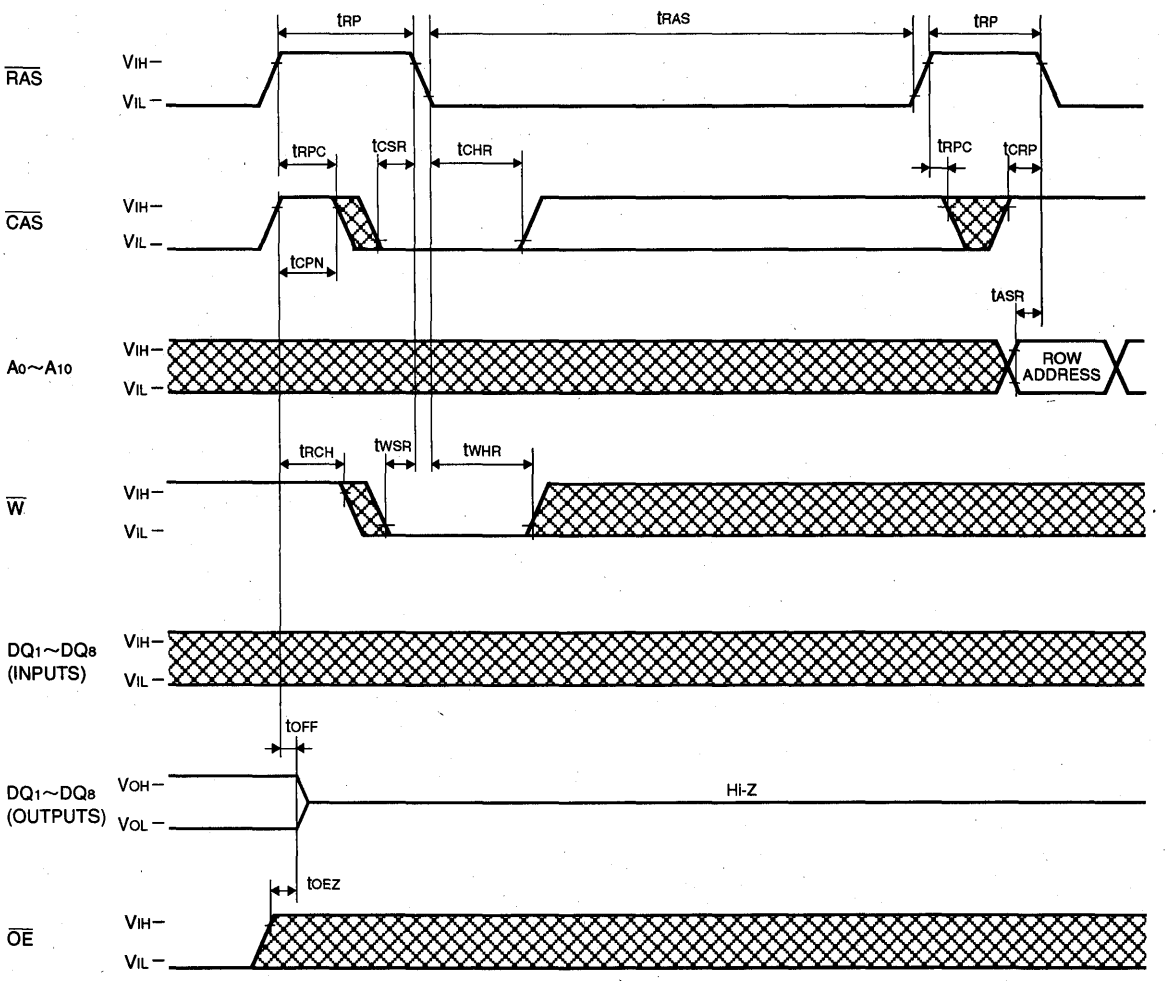


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle



TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17805CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs with Hyper page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V17805CXX-5,-5S	50	13	25	13	90	435
M5M4V17805CXX-6,-6S	60	15	30	15	110	360
M5M4V17805CXX-7,-7S	70	20	35	20	130	315

XX=J,TP

- Standard 28 pin SOJ,28 pin TSOP
- Single 3.3V±10% supply
- Low stand-by power dissipation
  - 1.8mW (Max) ..... CMOS Input level
  - 0.72mW (Max)* ..... CMOS Input level
- Operating power dissipation
  - M5M4V17805CXX-5,-5S ..... 525mW (Max)
  - M5M4V17805CXX-6,-6S ..... 435mW (Max)
  - M5M4V17805CXX-7,-7S ..... 380mW (Max)
- Self refresh capability*
  - Self refresh current ..... 200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

  * : Applicable to self refresh version(M5M4V17805CJ,TP-5S,-6S, -7S :option) only

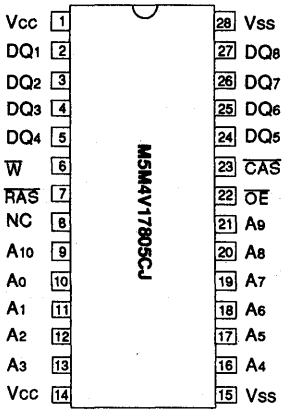
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

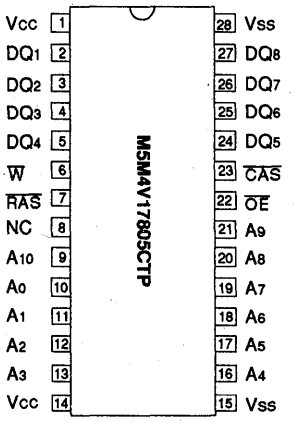
PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC: NO CONNECTION

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V17805CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

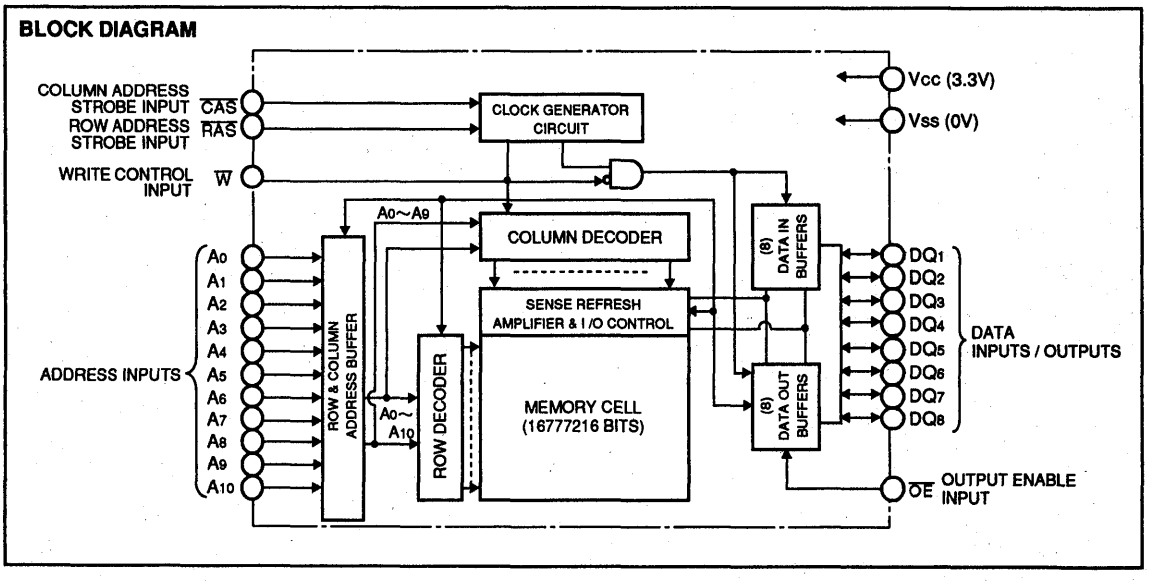
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M4V17805CJ, TP provides a number of other functions,e.g., $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC} +0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : $V_{IL(min)}$ is −2.0V when undershoot width is less than 25ns.(Undershoot width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc= 3.3V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 2.0mA	0		0.4	V
I_{OZ}	Off-state output voltage		Q floating, 0V≦V_{OUT}≦3.3V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 3.6V, Other inputs pins=0V	−10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M4V17805C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=twc=min. output open			145	mA
		M5M4V17805C-6,-6S				120	
		M5M4V17805C-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc−0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from Vcc,$\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V17805C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M4V17805C-6,-6S				120	
		M5M4V17805C-7,-7S				105	
I_{CC4} (AV)	Average supply current from Vcc, Hyper Page Mode (Note 3,4,5)	M5M4V17805C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M4V17805C-6,-6S				115	
		M5M4V17805C-7,-7S				90	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V17805C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M4V17805C-6,-6S				120	
		M5M4V17805C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) ,I_{CC4} (AV) , and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0~70℃ , Vcc = 3.3V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

HYPER PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta=0~70℃ , Vcc = 3.3V±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods(greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH (min) or lower than VIL (max) except $\overline{RAS}$ transition time.

7: Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max) and tCP ≧ tCP(max).

9: Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).

11: Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).

12: tOEZ (max) ,tWEZ(max) ,tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (IOUT ≦ | ±10 μA |) and is not reference to VOH(min) or VOL(max).

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)
(Ta=0~70℃, Vcc = 3.3V ±10%, Vss=0V, unless otherwise noted, See notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note20)	13		15		20		ns
tT	Transition time	(Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD(min) and tCPWD ≧tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note26)	20		25		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle (Note27)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note28)	8	13	10	16	13	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: tHPC(min) is specified in the case of read-only and early write-only in Hyper Page Mode.
27: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
28: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tCAS	$\overline{CAS}$ low pulse width	17		17		22		ns
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases tRSR and tRHR should be satisfied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow - Refresh cycle (note 6)	M5M4V17805C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$≦0.2V $\overline{OE}$ & $\overline{WE}$≦0.2V or $\overline{OE}$ & $\overline{WE}$ ≧ Vcc-0.2V A_0~A_{10}≦0.2V or A_0 ~A_{10} ≧Vcc-0.2V t_{REF}=128ms (2048 cycles) output = OPEN t_{RAS}=t_{RAS}min. ~1 μs			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M4V17805C (S)	$\overline{RAS}$= $\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

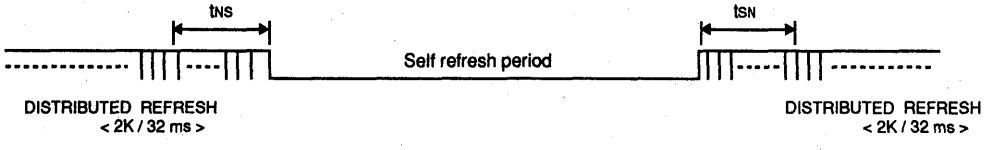
TIMING REQUIREMENTS (T_a=0~70℃, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted, See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M4V17805C-5S		M5M4V17805C-6S		M5M4V17805C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self refresh $\overline{CAS}$ hold time	−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

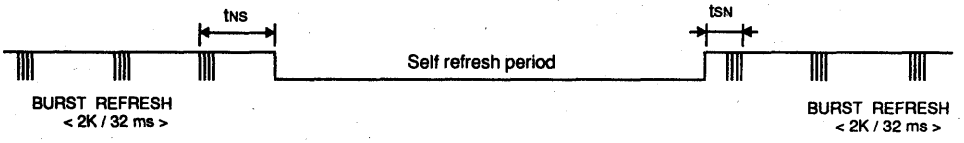
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦ 32 ms and t_{SN} ≦32 ms.



(2) In case of burst refresh

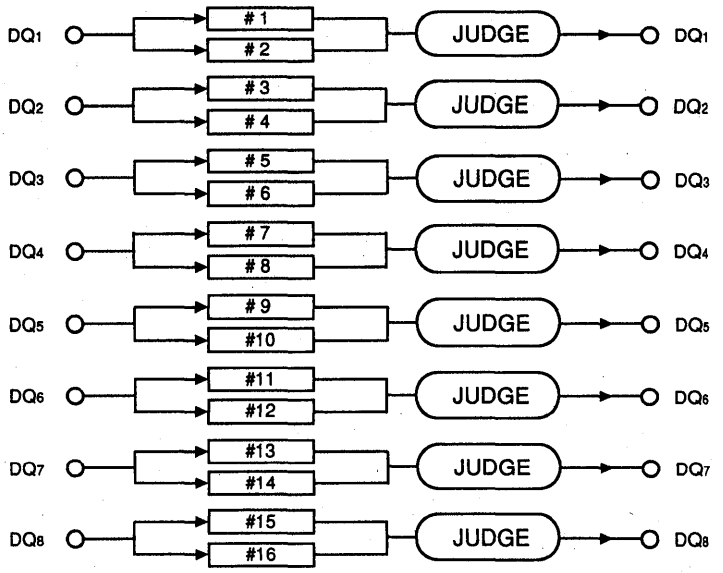
The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} + t_{SN} ≦ 32 ms.



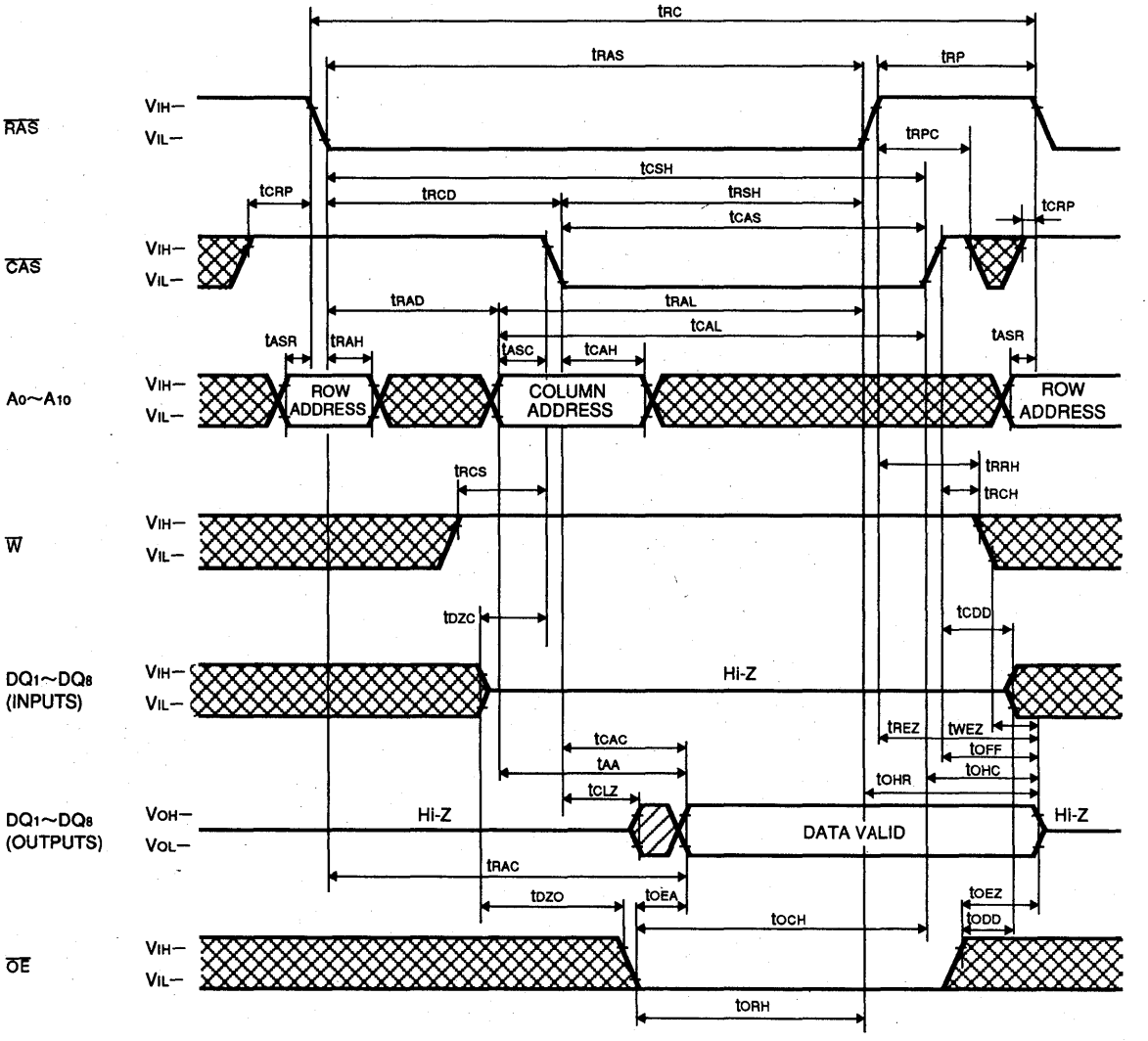
TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M4V17805C-5,-5S		M5M4V17805C-6,-6S		M5M4V17805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth) . No addressing of CA0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 32)
Read Cycle

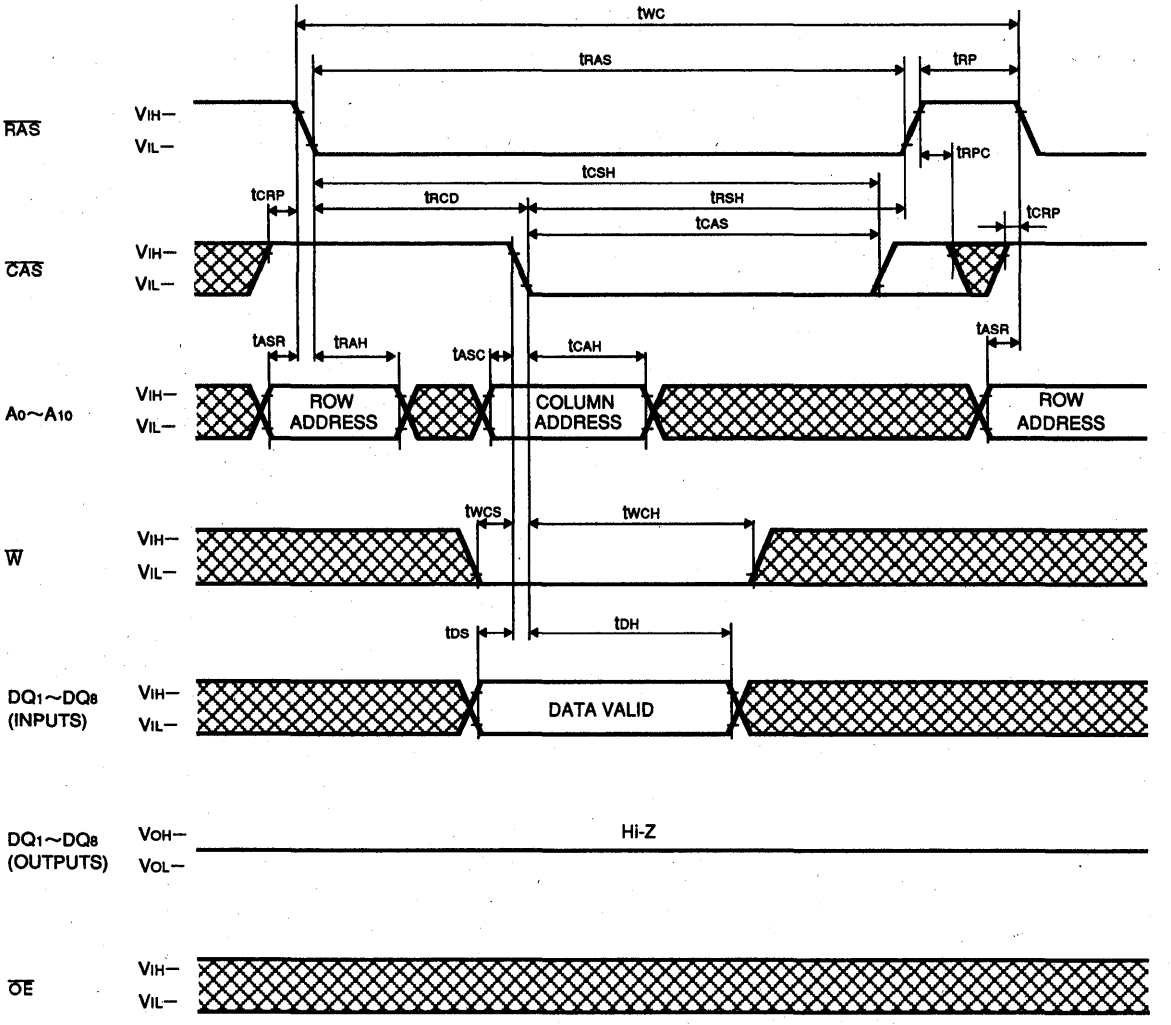


Note 32

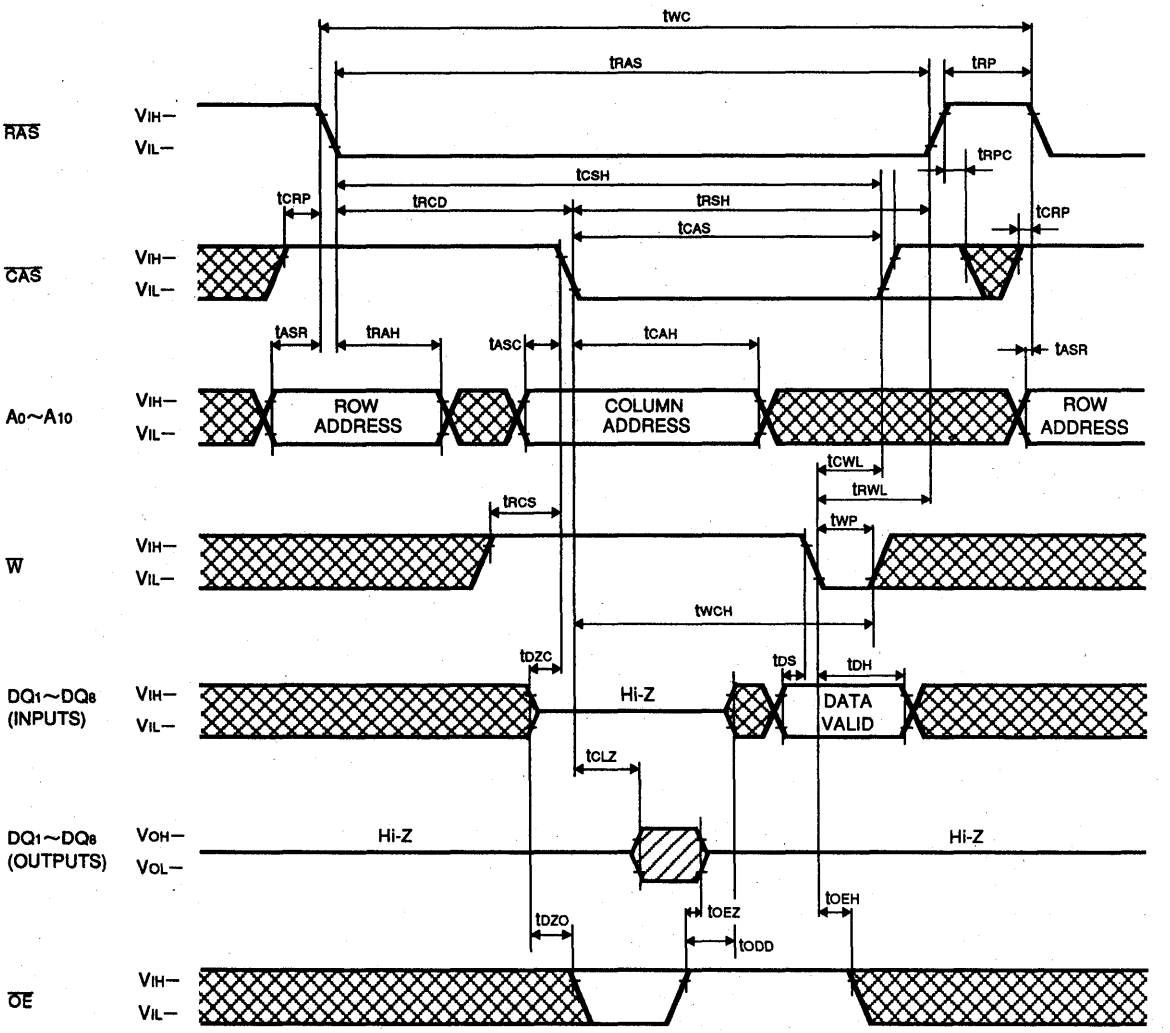
Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output.

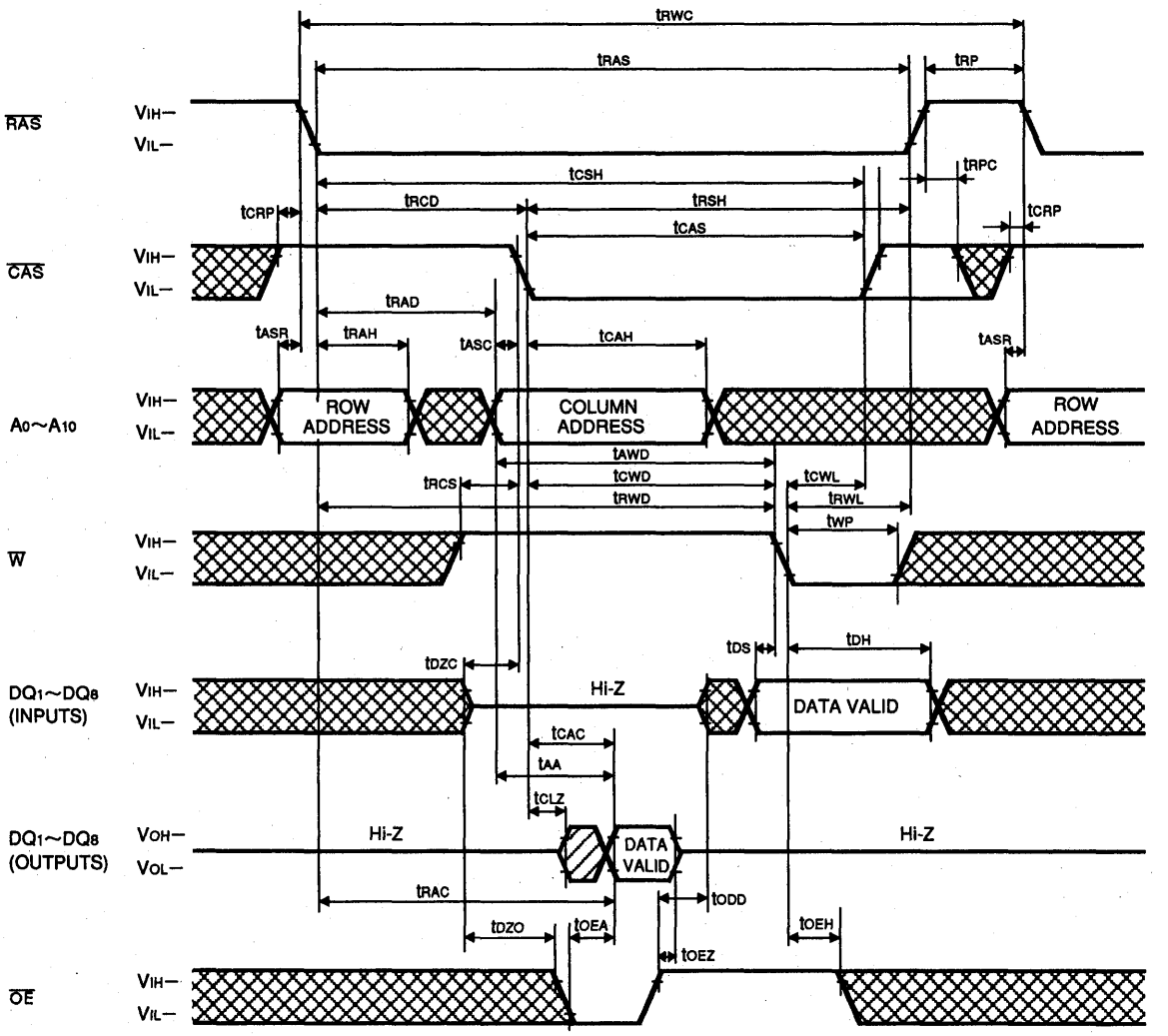
Early Write Cycle



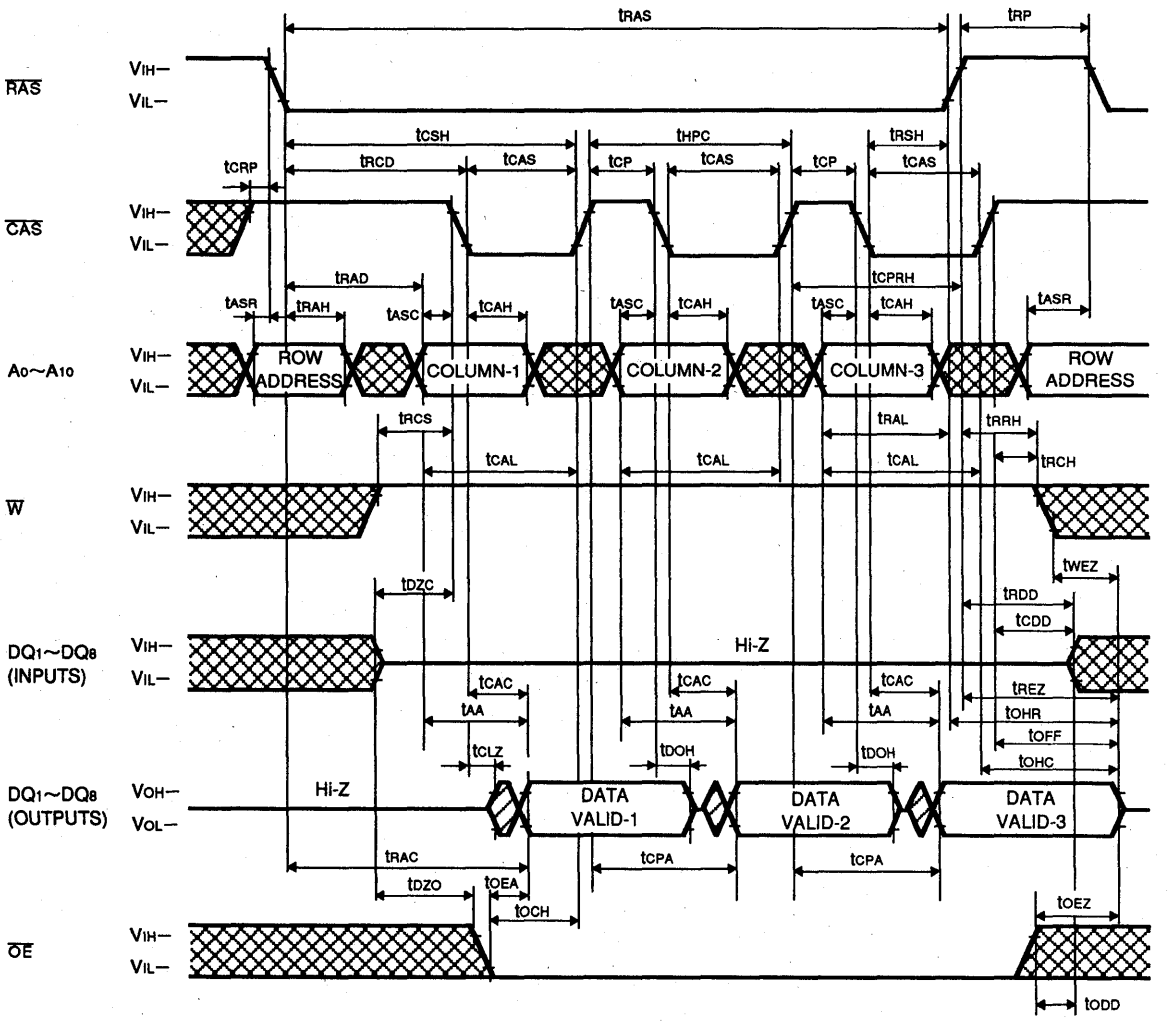
Delayed Write Cycle



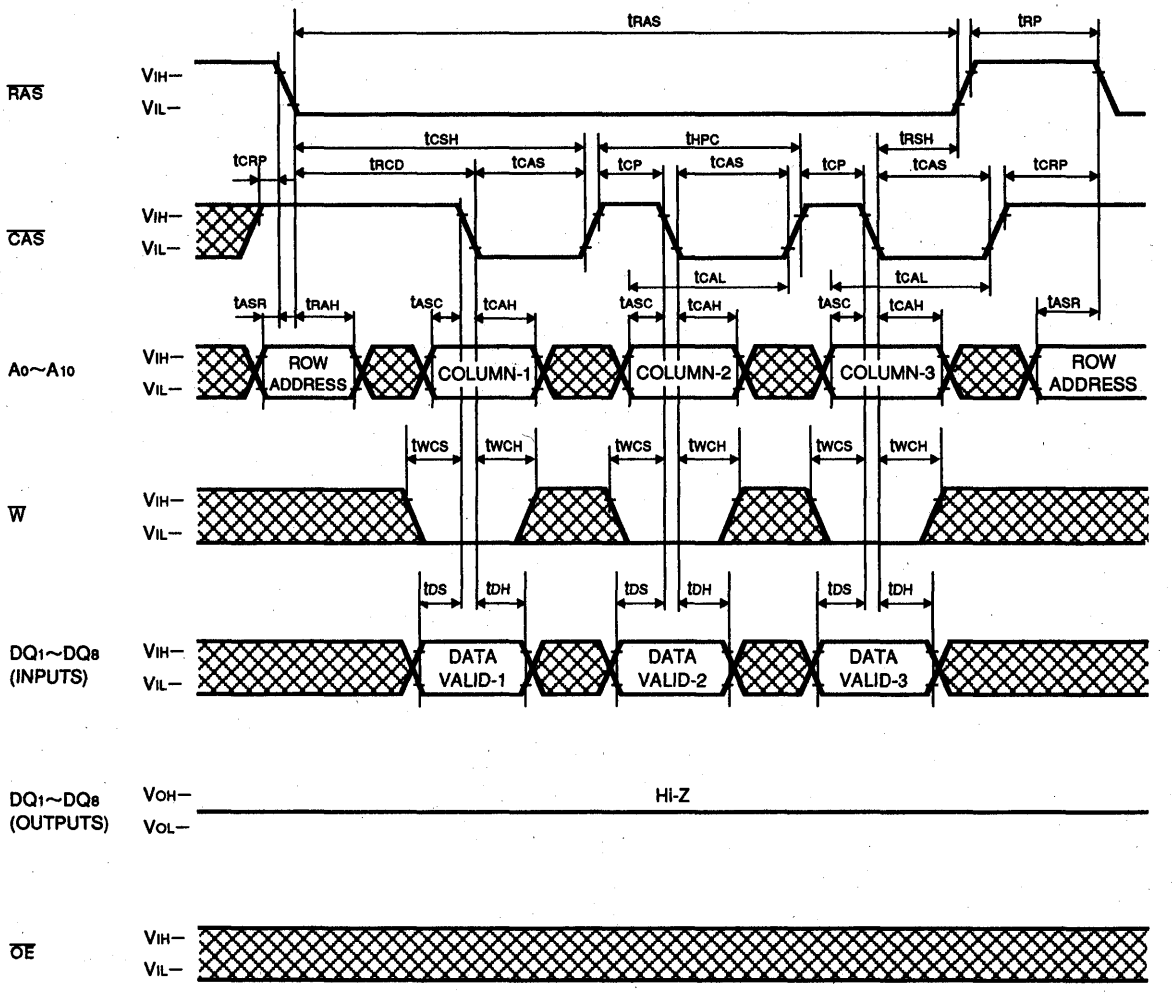
Read-Write, Read-Modify-Write Cycle



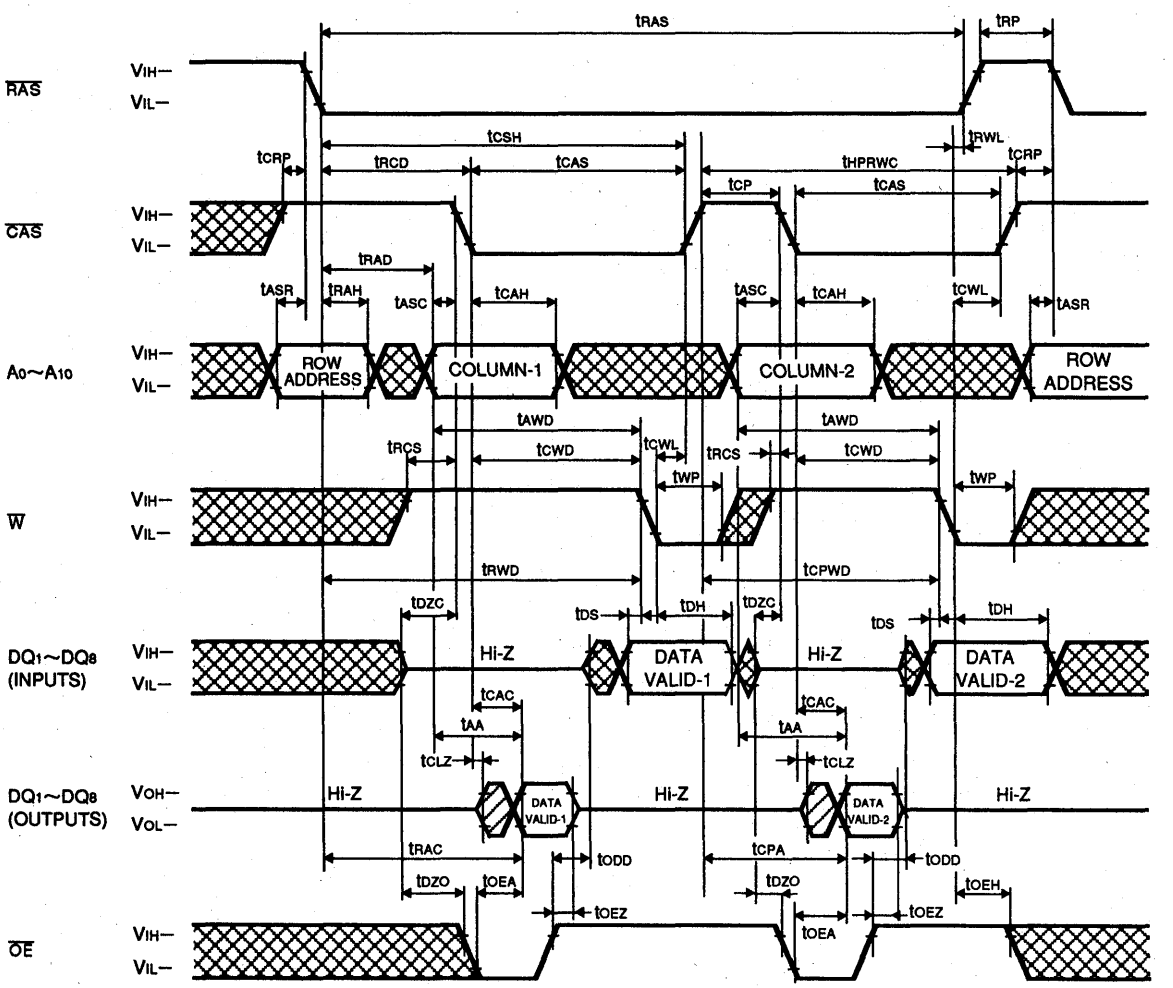
Hyper Page Mode Read Cycle



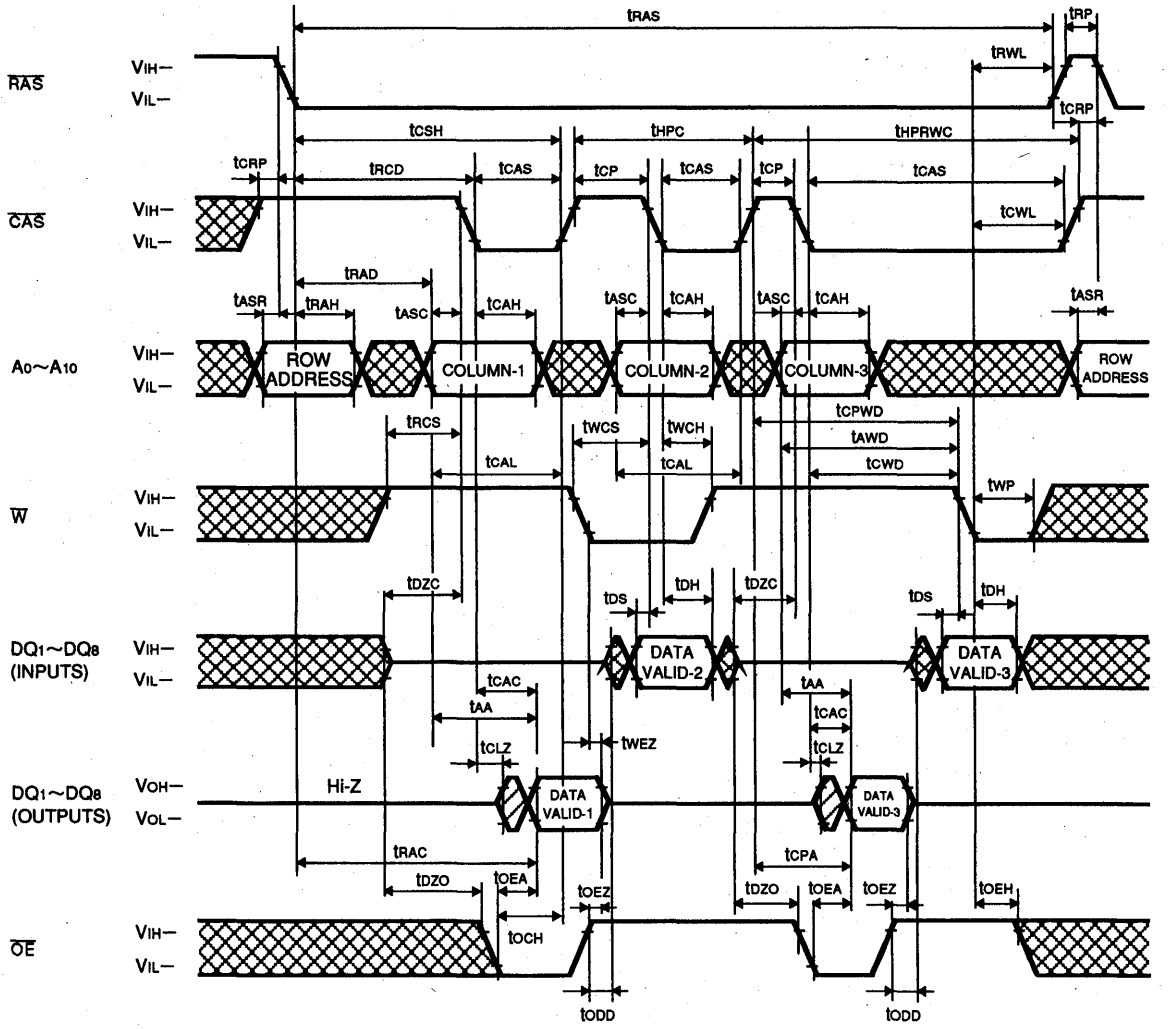
Hyper Page Mode Early Write Cycle



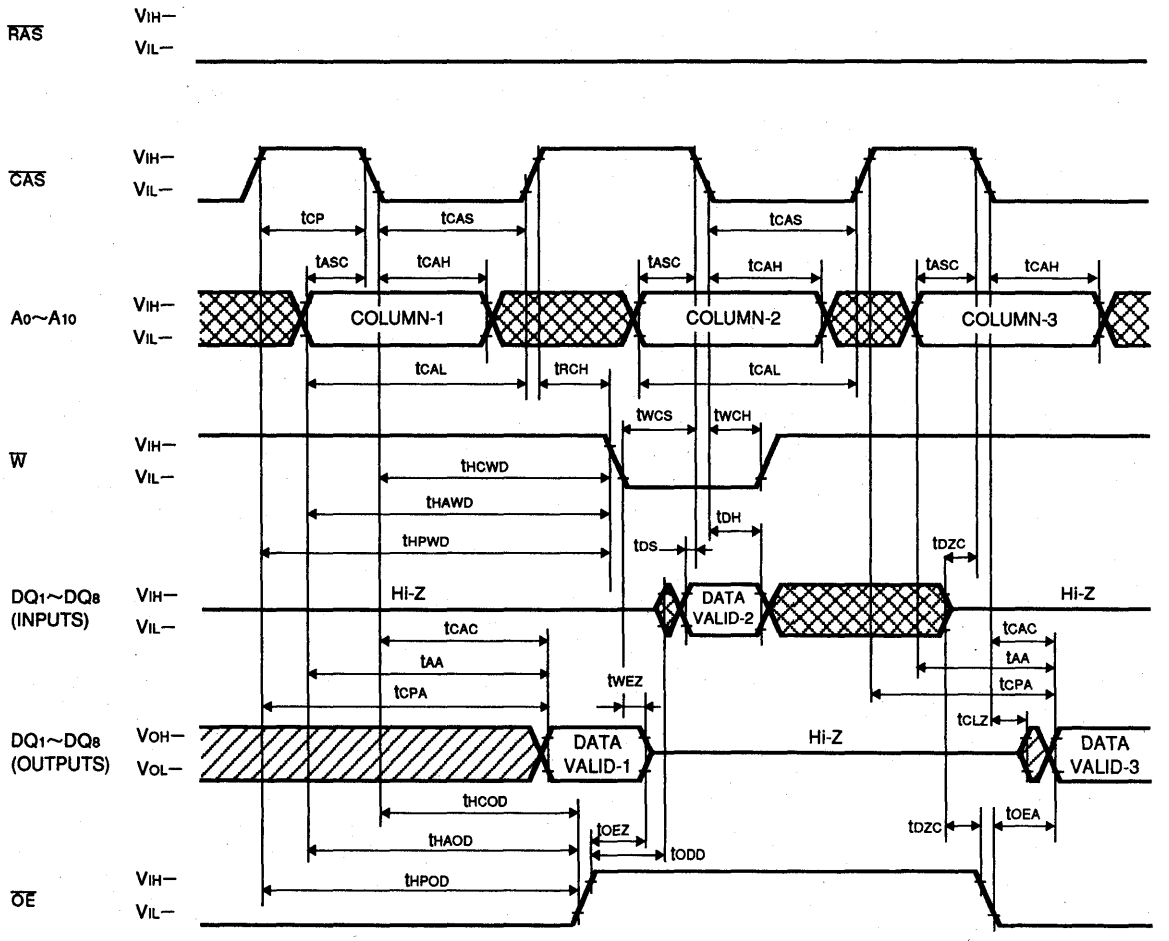
Hyper Page Mode Read-Write,Read-Modify-Write Cycle



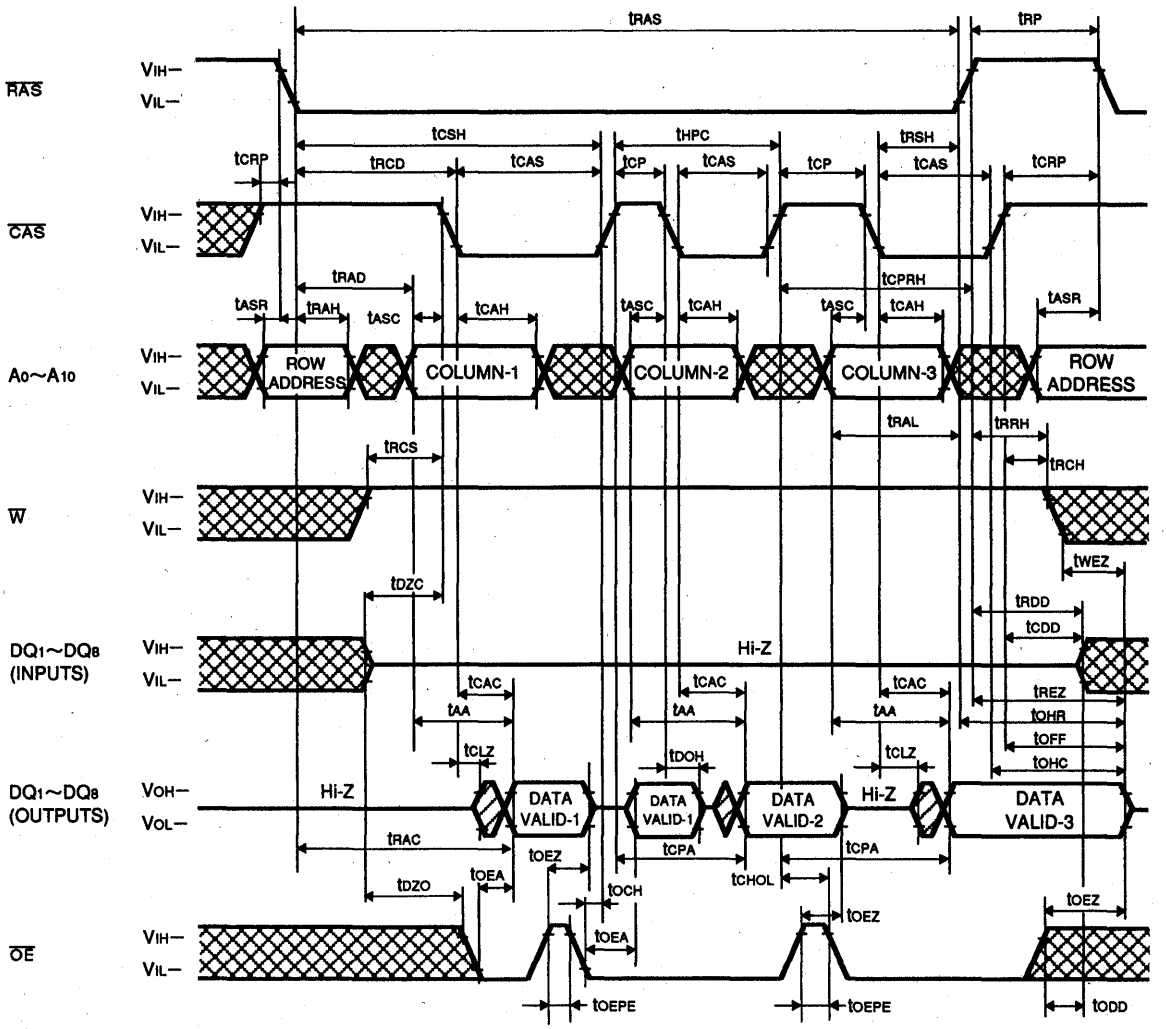
Hyper Page Mode Mix Cycle (1)



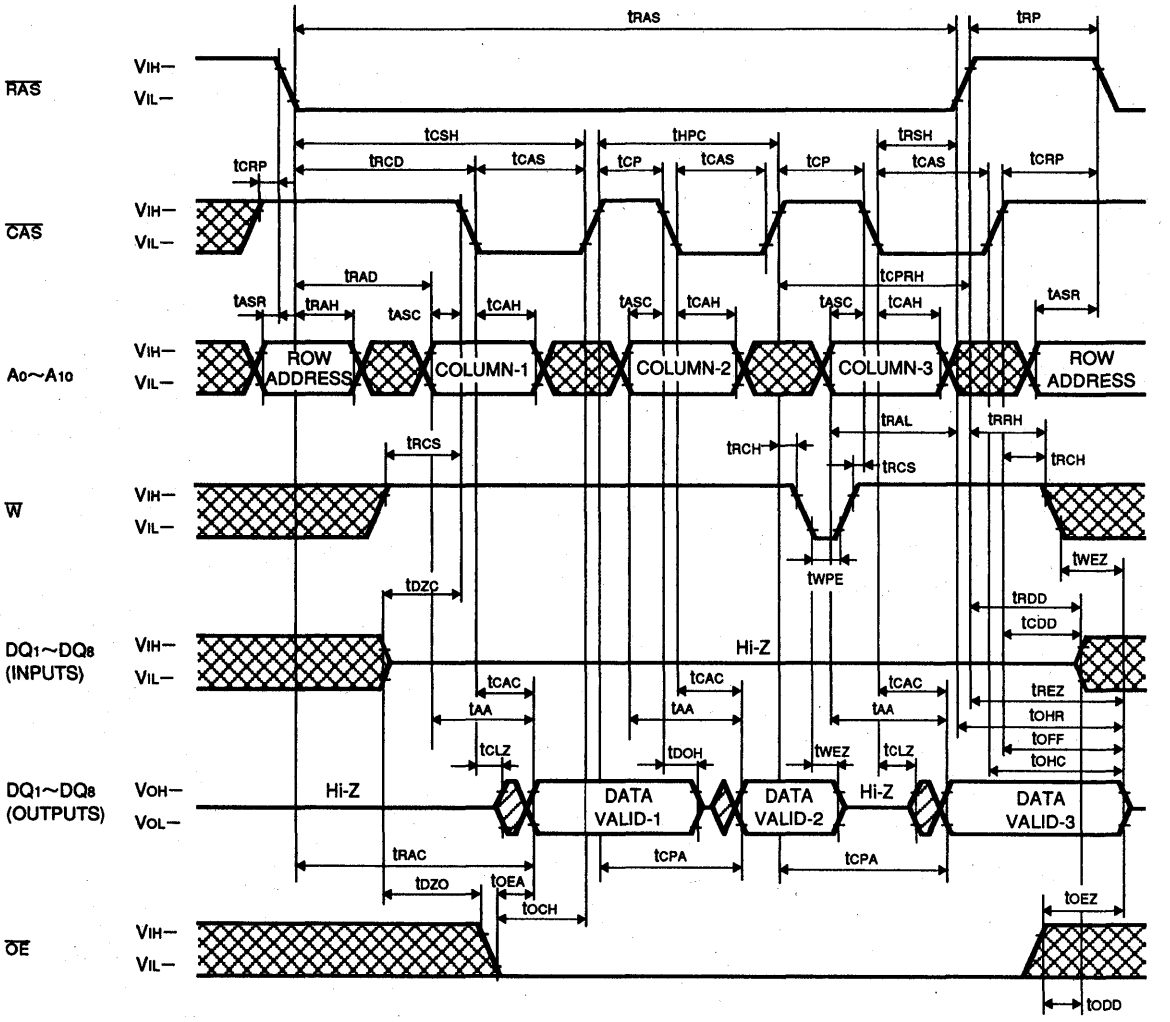
Hyper Page Mode Mix Cycle (2)



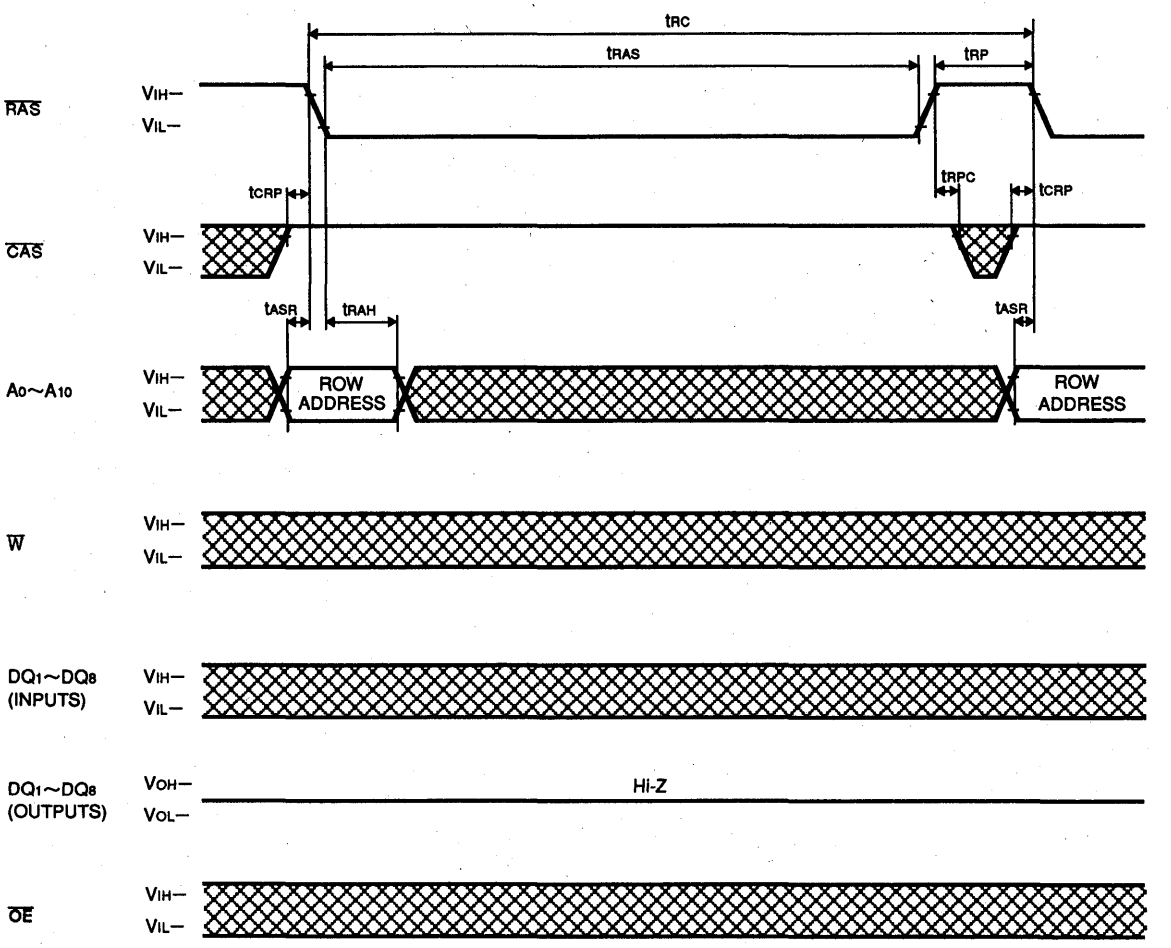
Hyper Page Mode Read Cycle (HI-Z control by $\overline{OE}$)



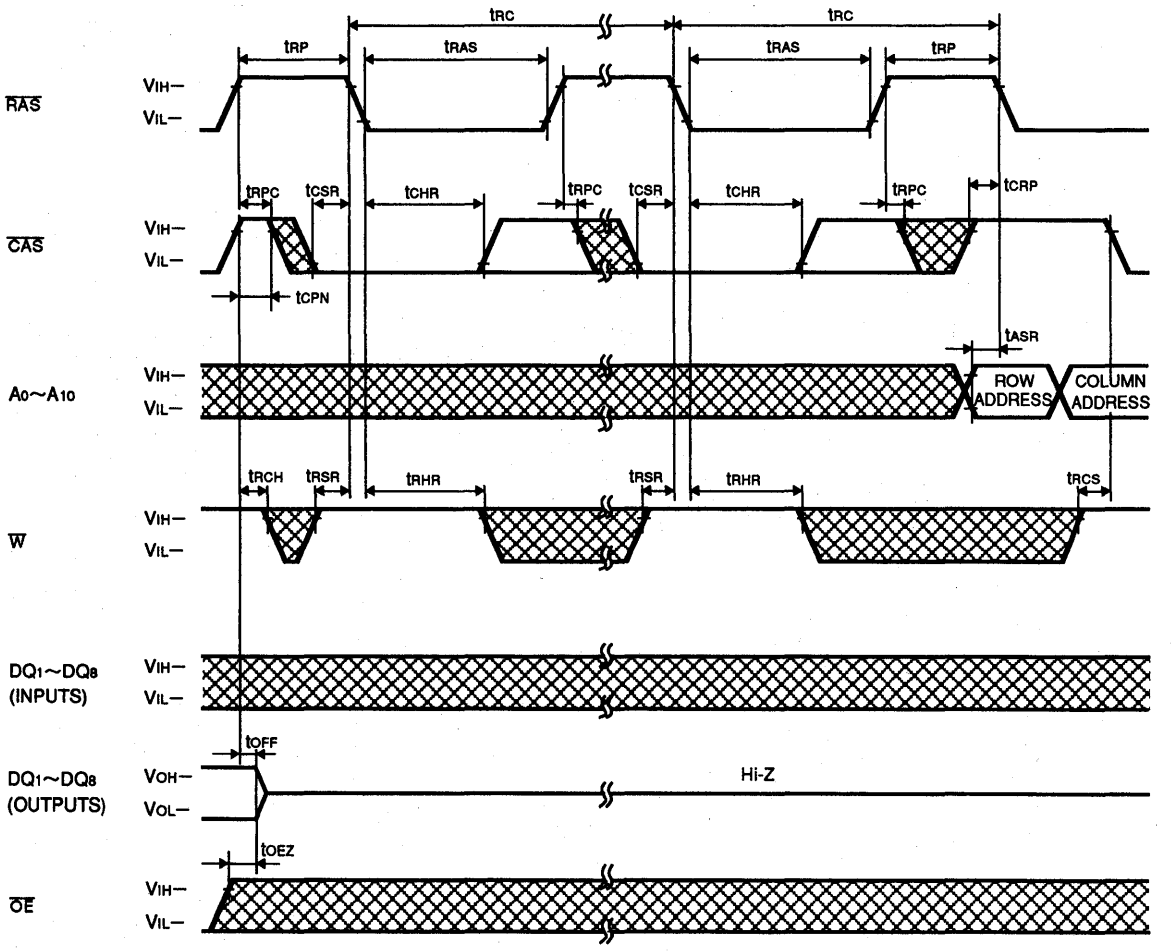
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



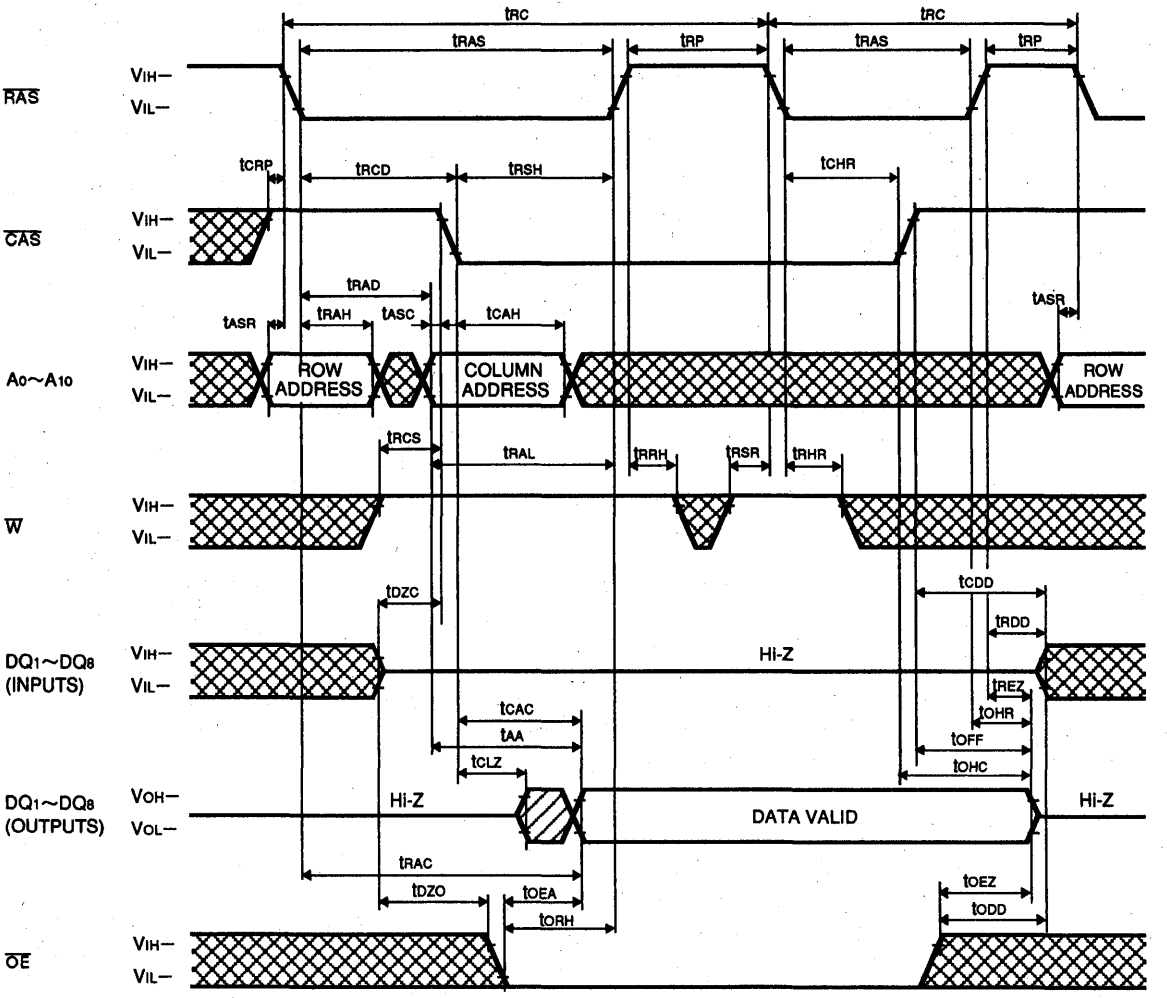
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

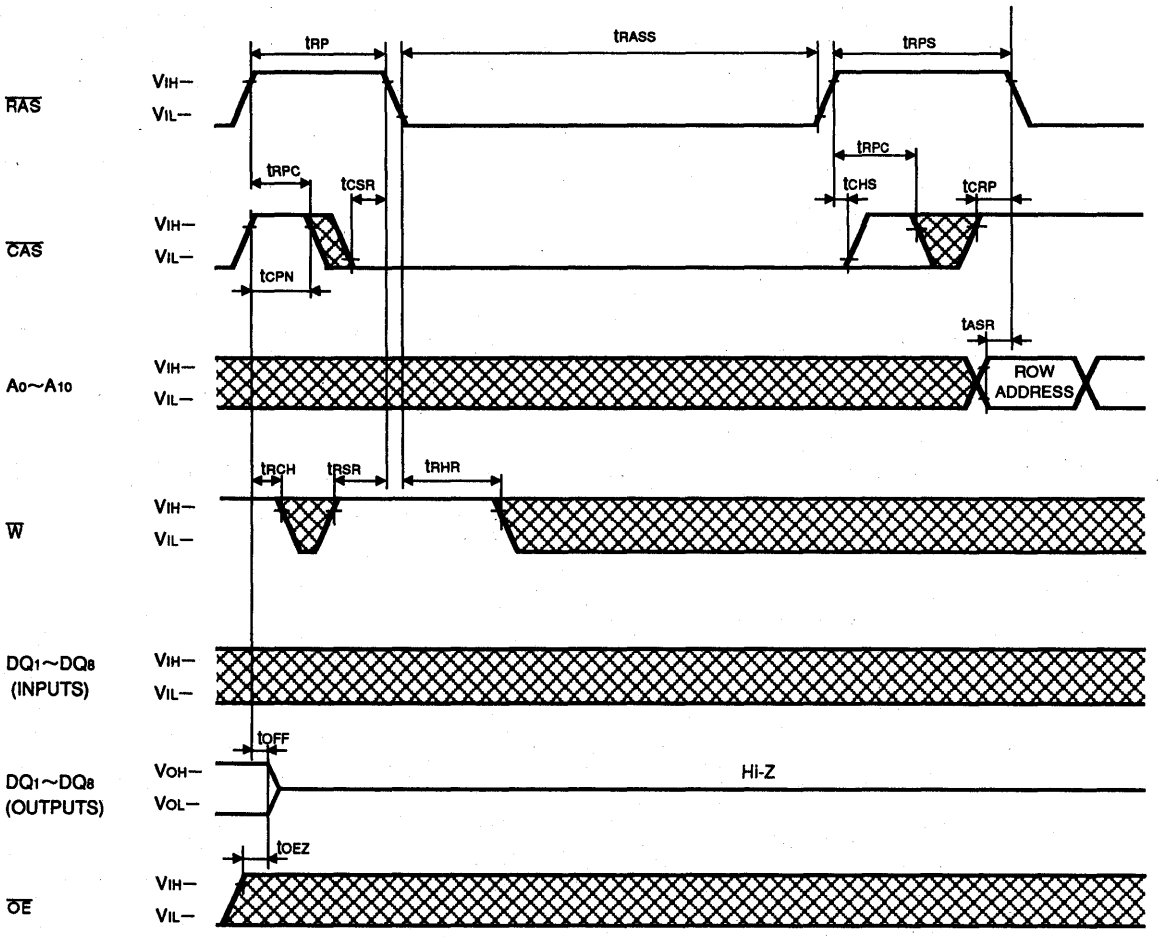


Hidden Refresh Cycle (Read) (Note 33)



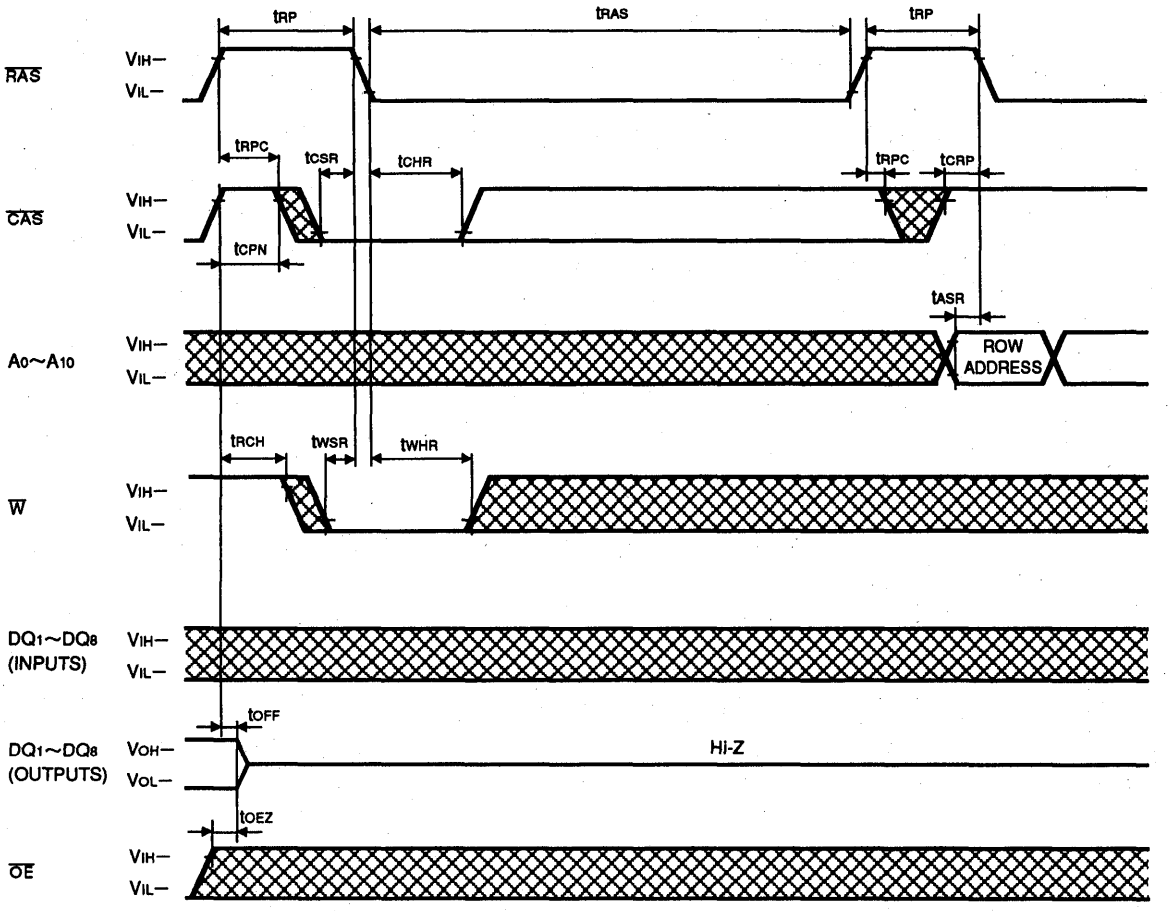
Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up , however entried into Test Mode.

M5M4V16160BTP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

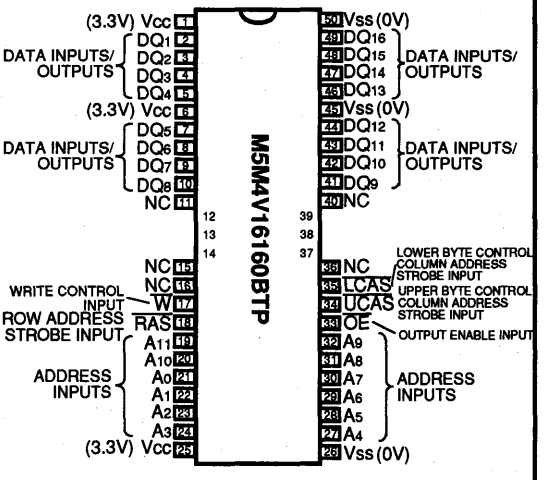
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16160BTP-6,-6S	60	15	30	15	110	285
M5M4V16160BTP-7,-7S	70	20	35	20	130	255

- Standard 50pin TSOP
- Single 3.3V ± 0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ..... CMOS Input level
- Low operating power dissipation
  M5M4V16160BTP -6, -6S ..... 345.0mW (Max)
  M5M4V16160BTP-7, -7S ..... 310.0mW (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 50P3W-L (400mil TSOP)

NC : NO CONNECTION

FUNCTION

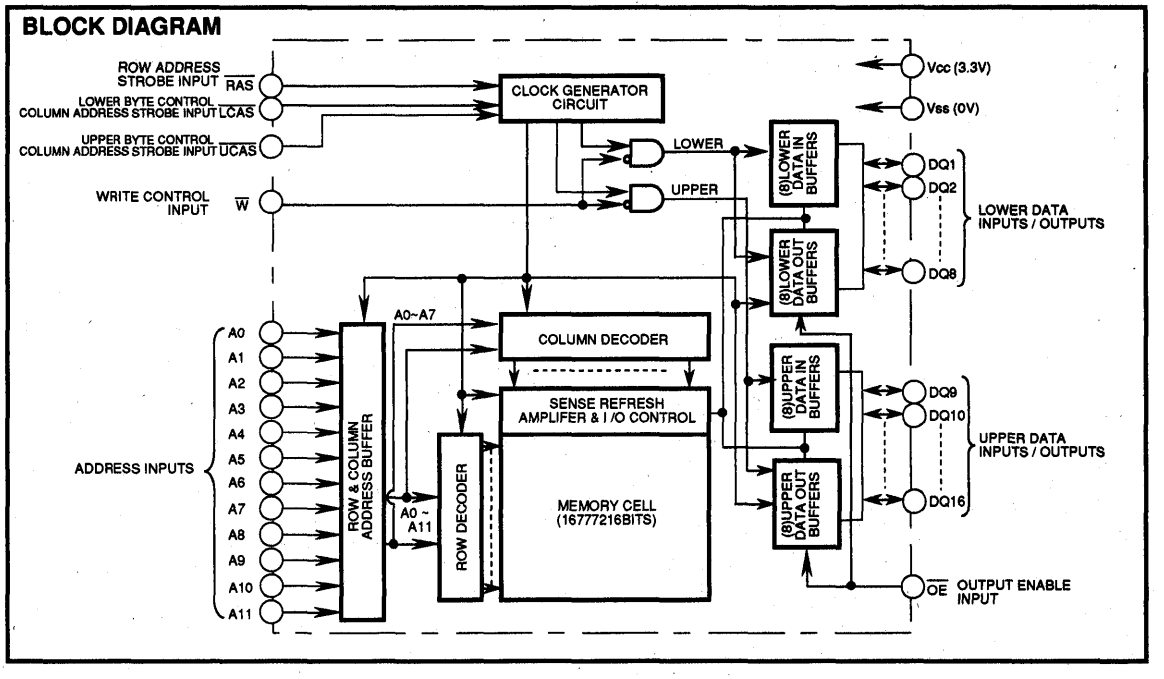
The M5M4V16160BTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
Vo	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦ V_{OUT}≦ 3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦ Vcc+0.3V,Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M4V16160B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			95	mA
		M5M4V16160B-7,-7S				85	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V16160B-6,-7	$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V, output open			0.5	
		M5M4V16160B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V, output open			0.15	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M4V16160B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			95	mA
		M5M4V16160B-7,-7S				85	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M4V16160B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			70	mA
		M5M4V16160B-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16160B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			95	mA
		M5M4V16160B-7,-7S				85	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0~70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, $\overline{W}$ input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0～70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note7,8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note7,9)		60		70	ns
tAA	Column address access time	(Note 7,10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 100pF, V_{OH}=2.4V(I_{OH}=-2mA) and V_{OL}=0.4V(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL})
8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		64		64	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note19)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note19)	15		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T =5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note22)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note23)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note23)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note25)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note23)	60		65		ns

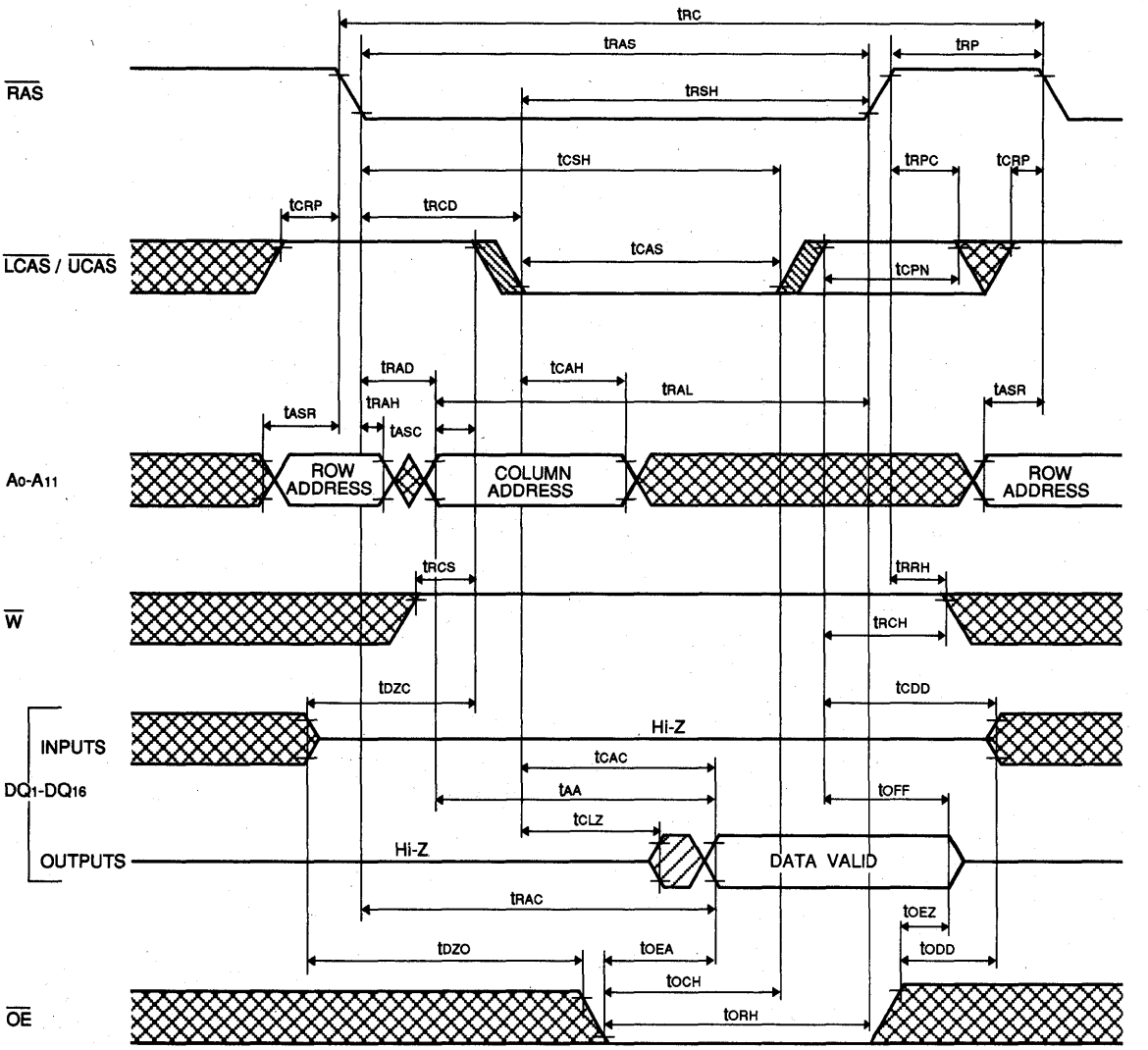
Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M4V16160B-6,-6S		M5M4V16160B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



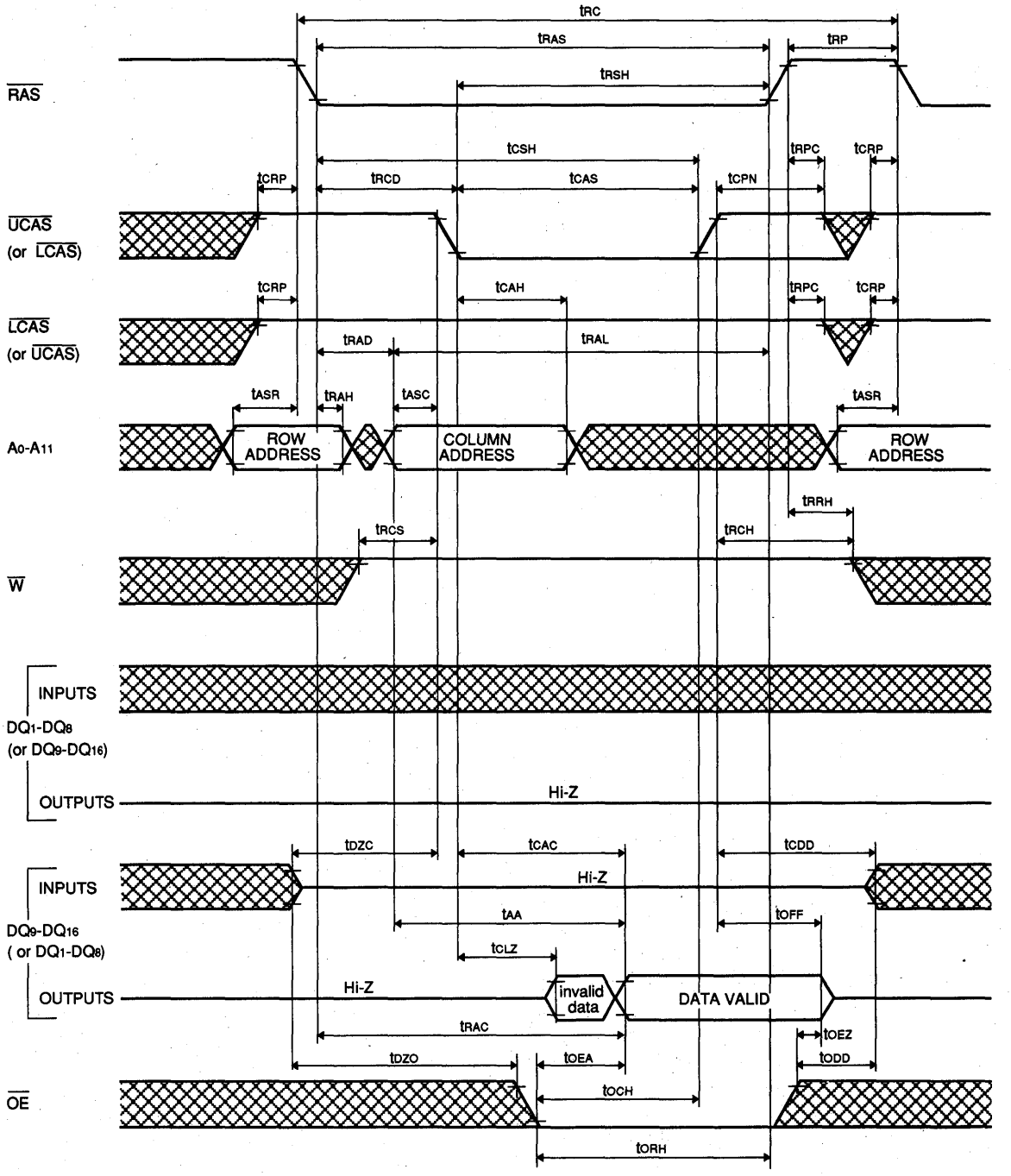
Note 28

Indicates the don't care input.
$V_{IH}(min.) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min.) \leqq V_{IN} \leqq V_{IL}(max)$

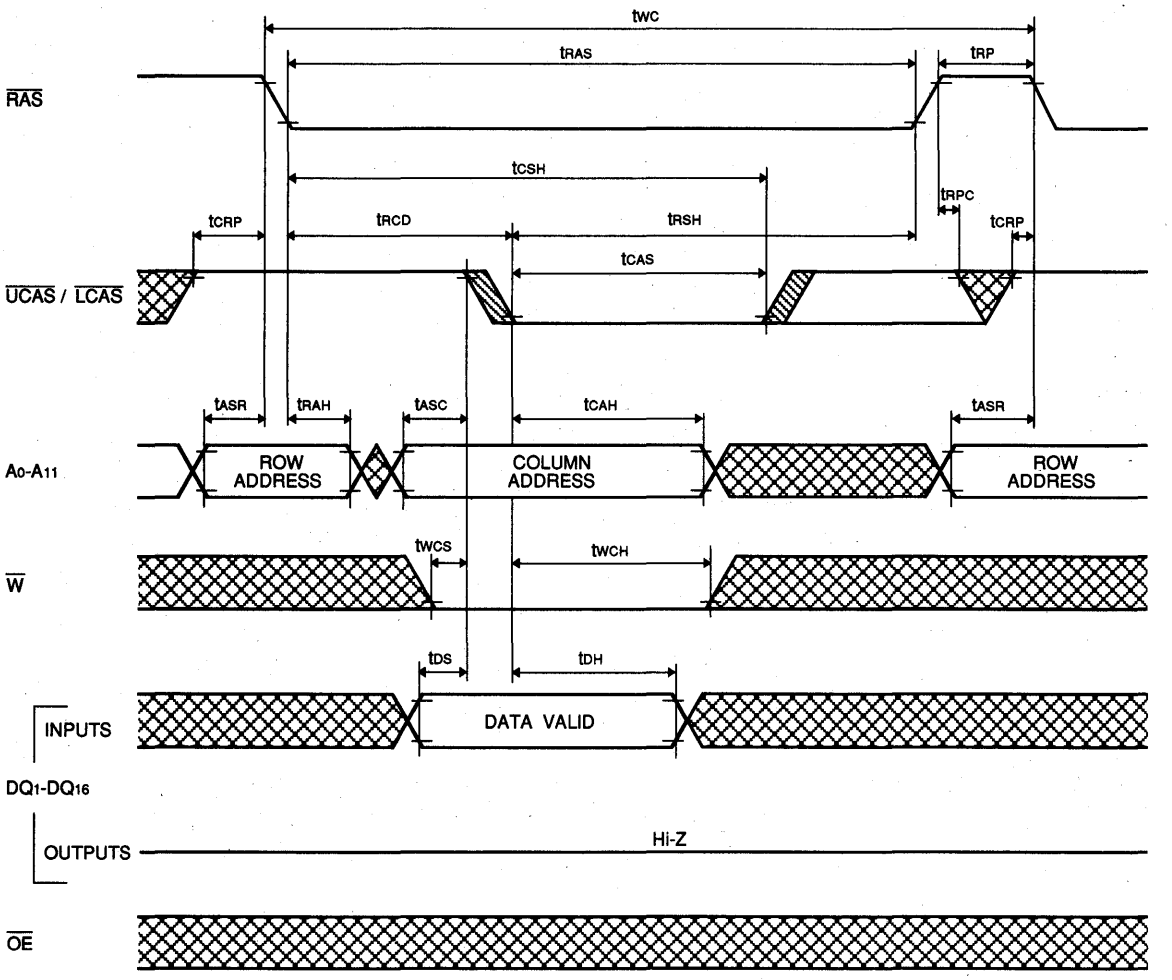
Indicates the invalid output.

Indicates the skew of the two inputs.

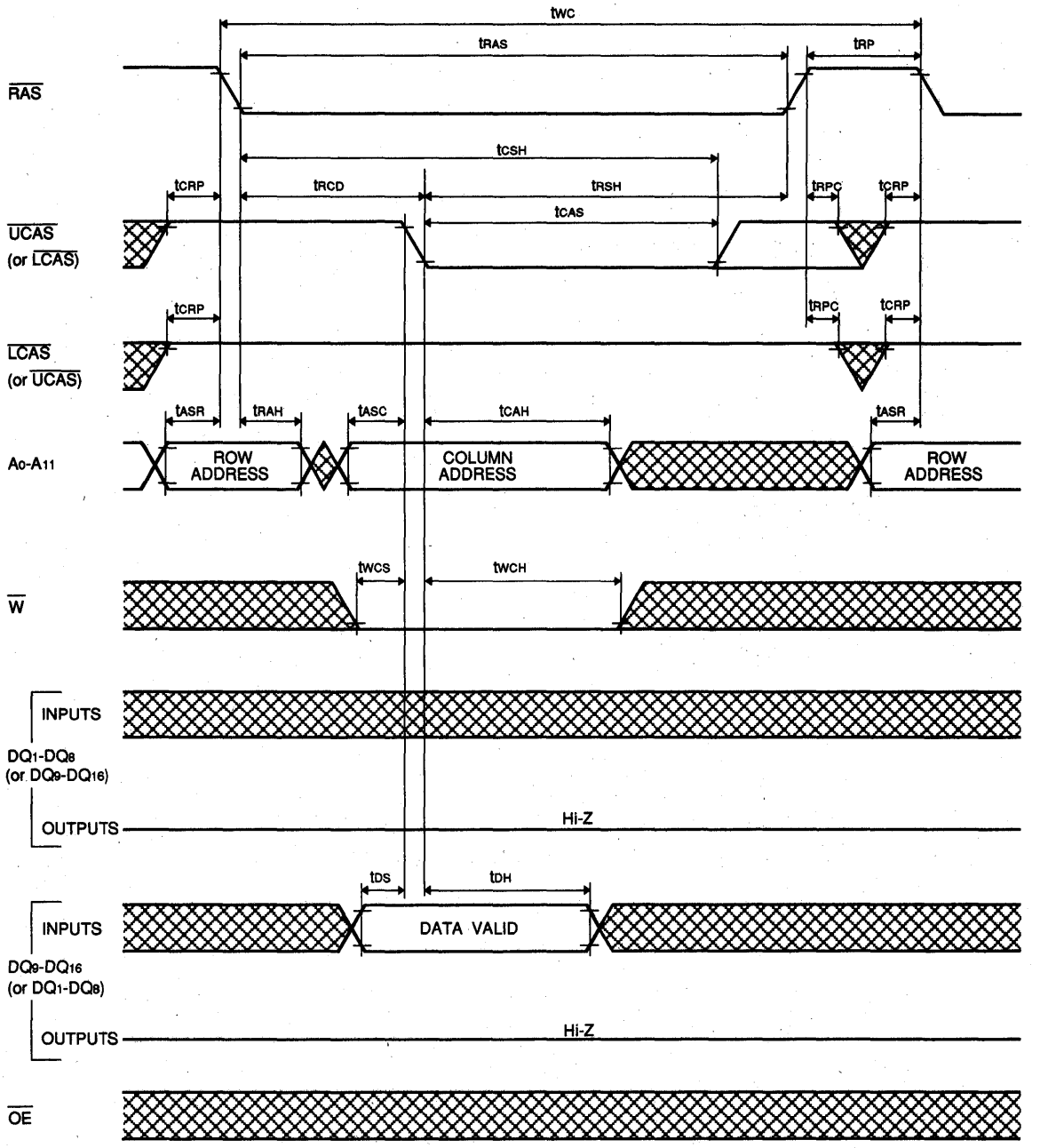
Upper / (Lower) Byte Read Cycle



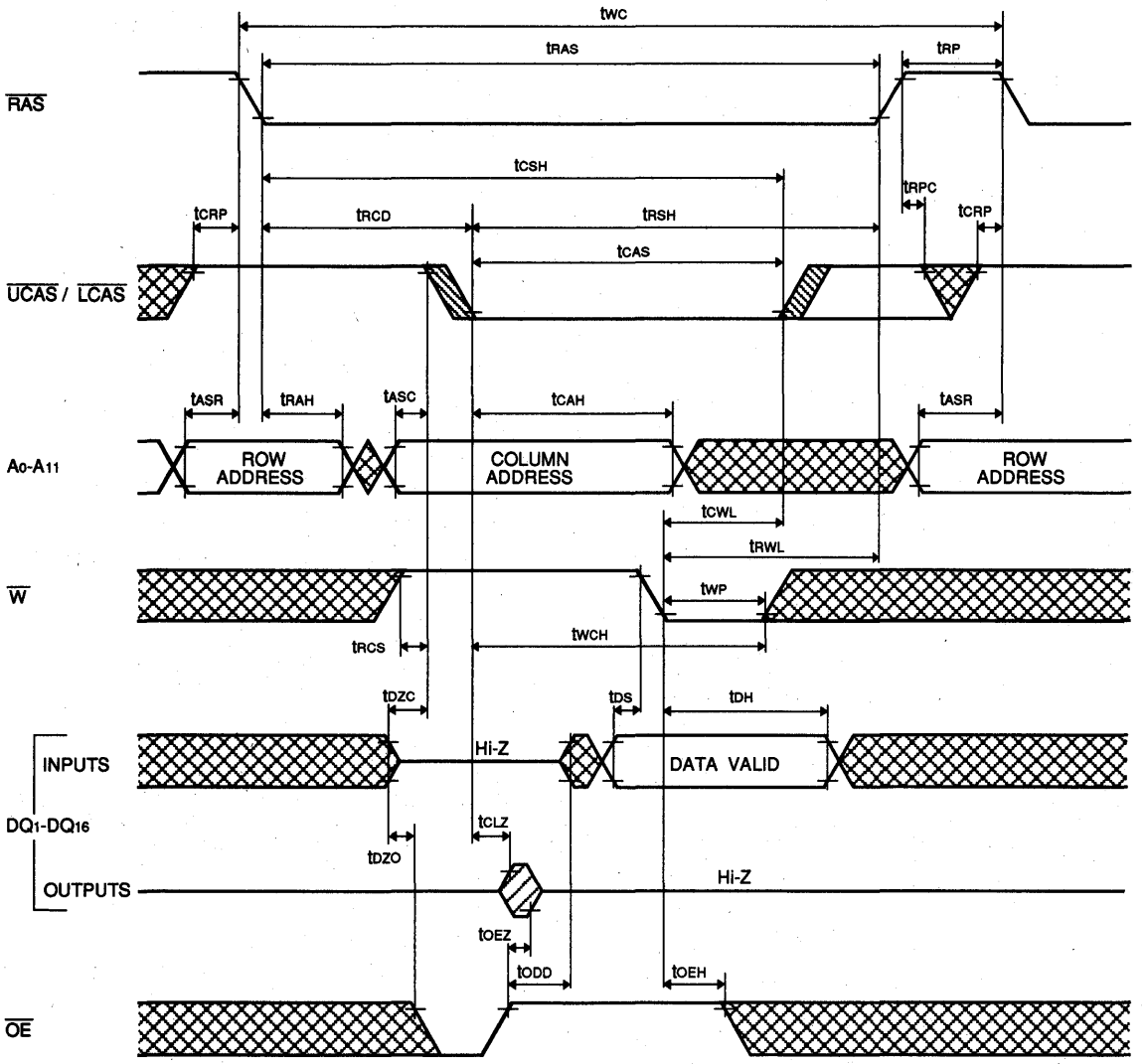
Write Cycle (Early write)



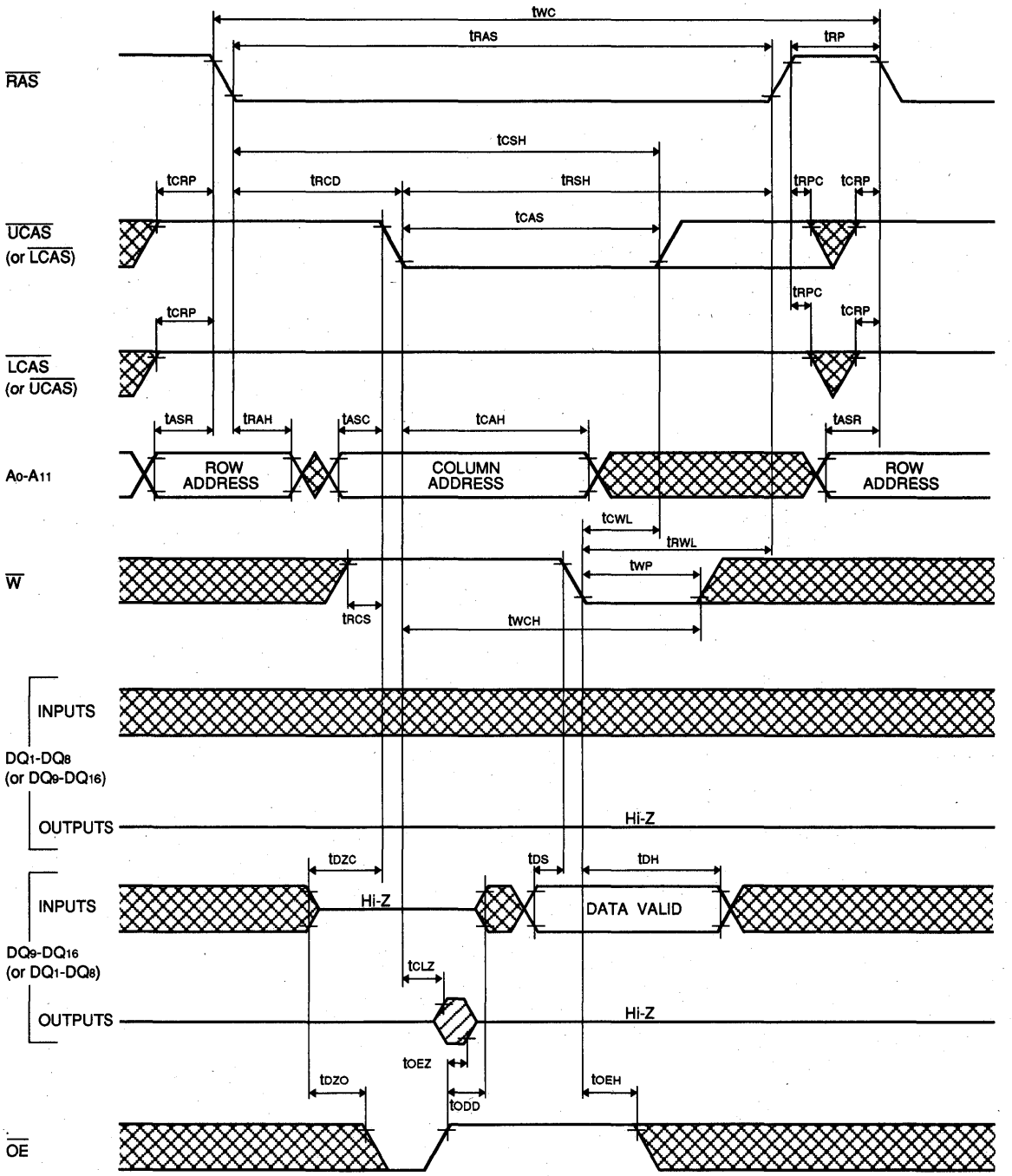
Upper/(Lower) Byte Write Cycle (Early write)



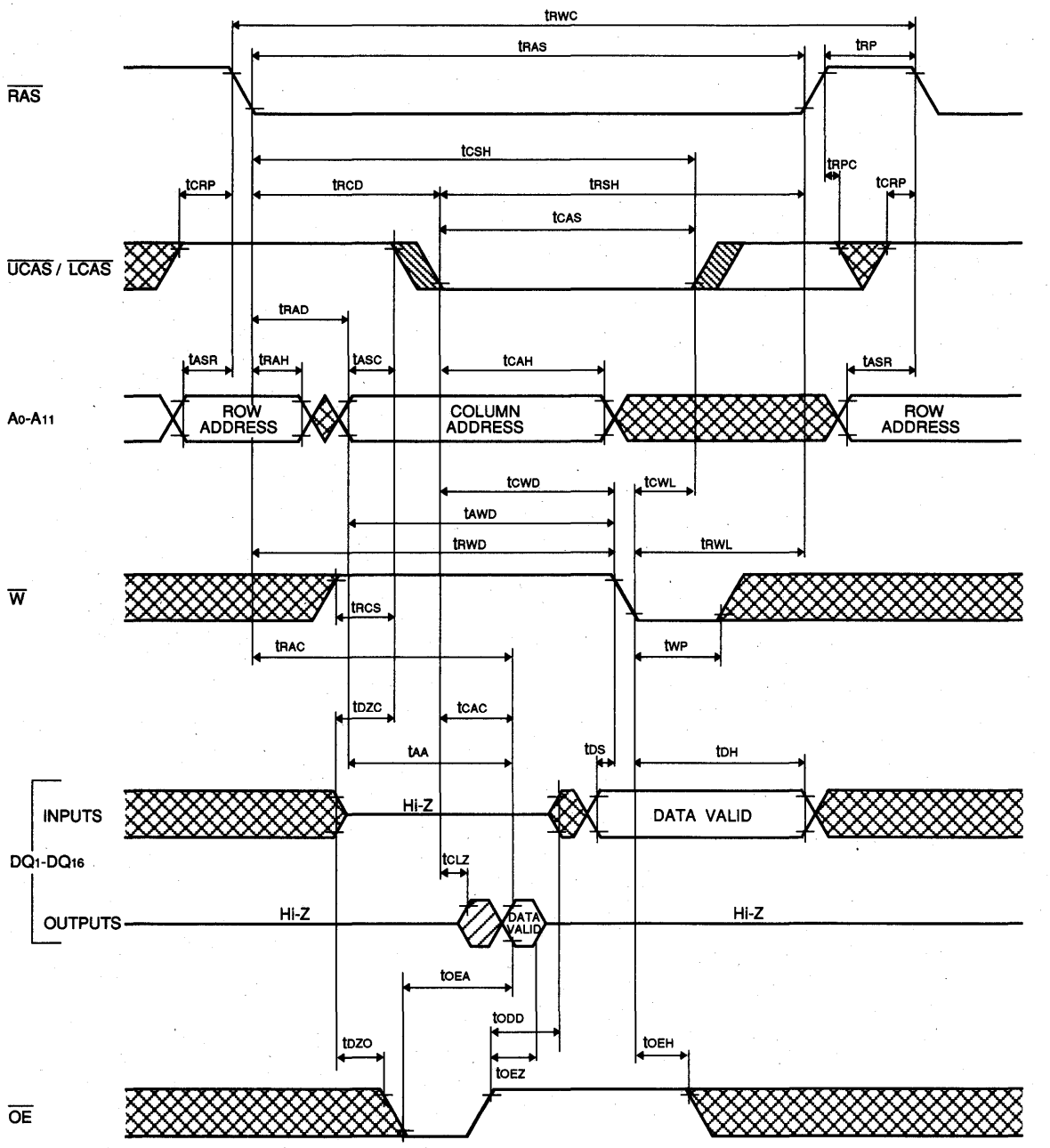
Write Cycle (Delayed write)



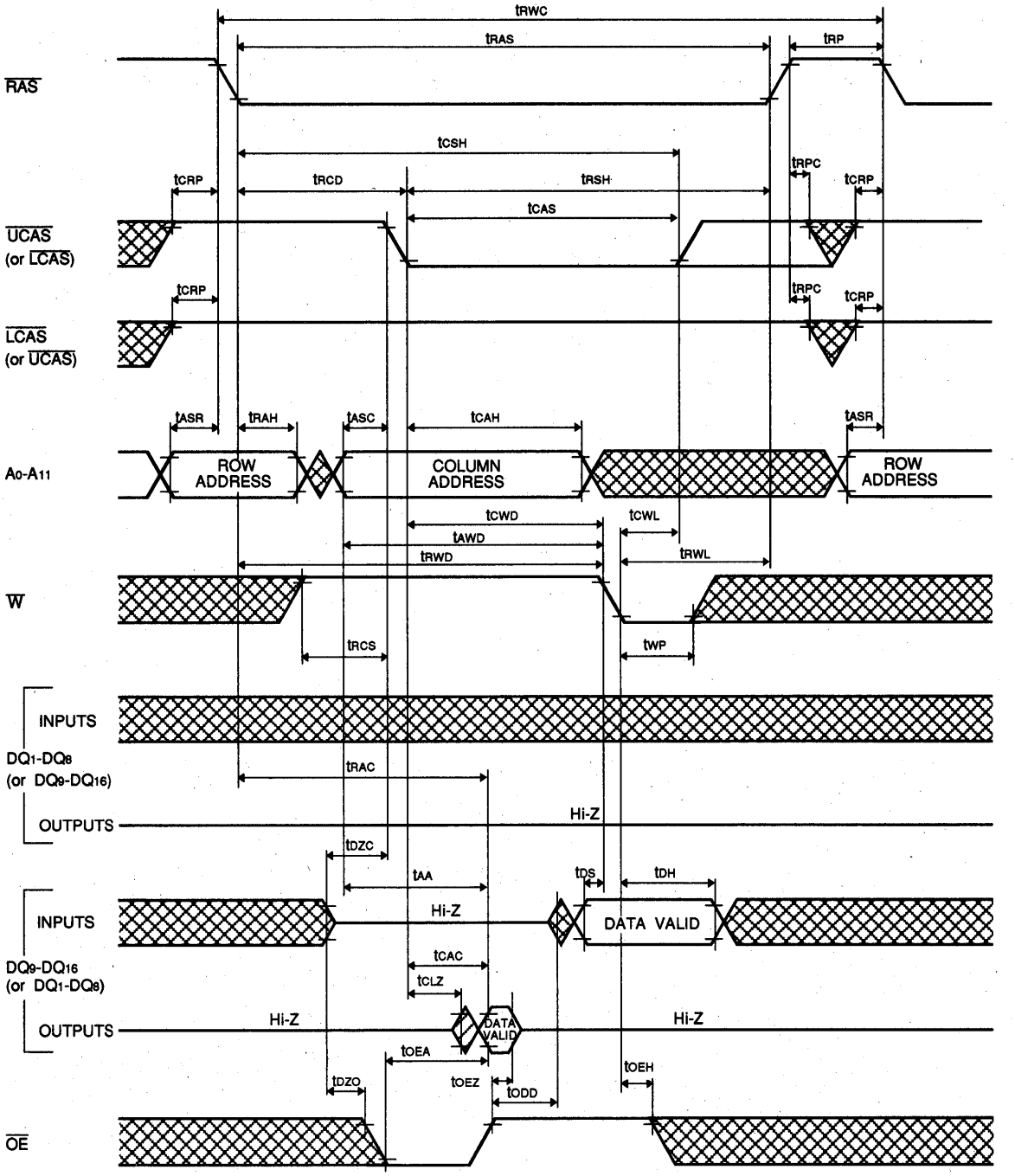
Upper/(Lower) Byte Write Cycle (Delayed write)



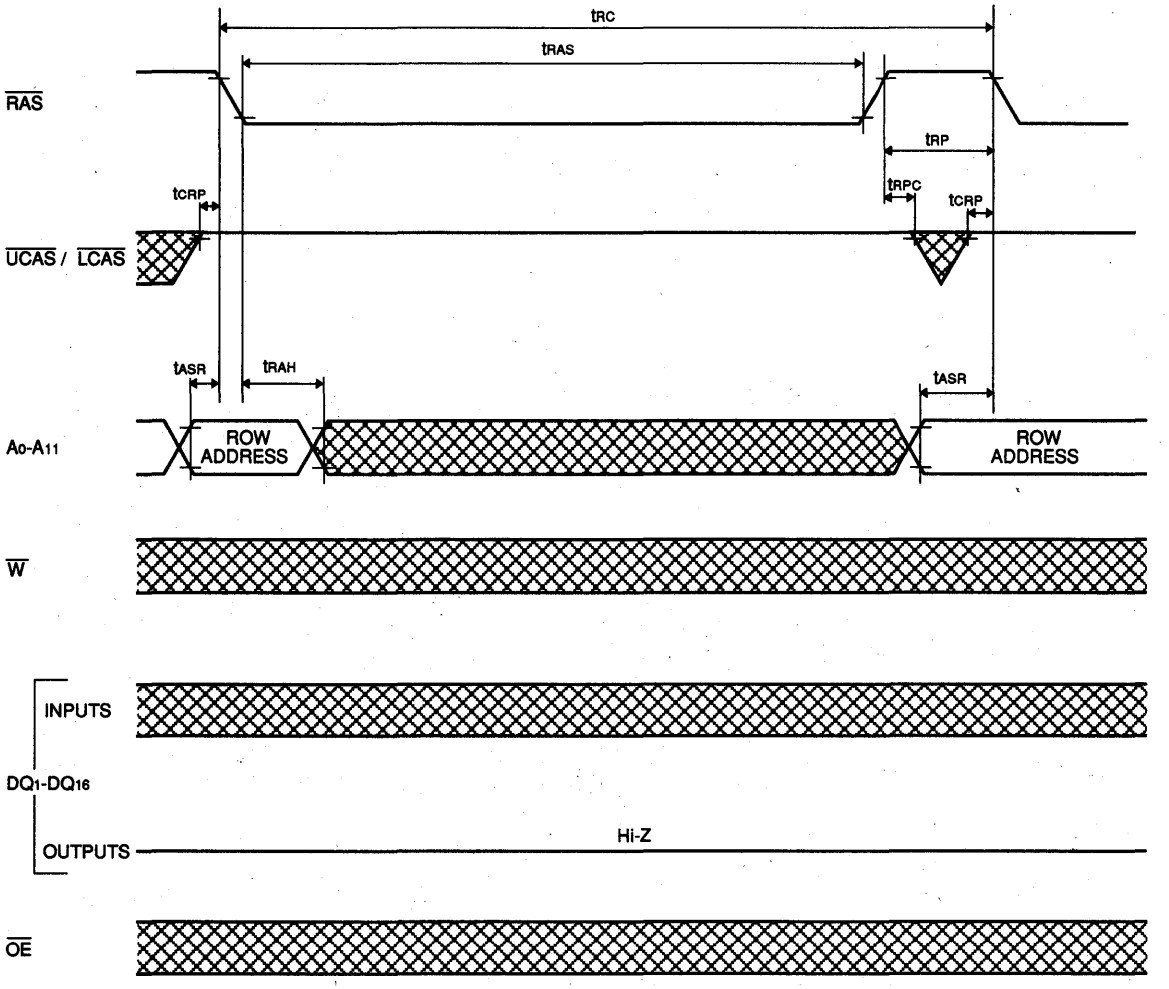
Read-Write, Read-Modify-Write Cycle



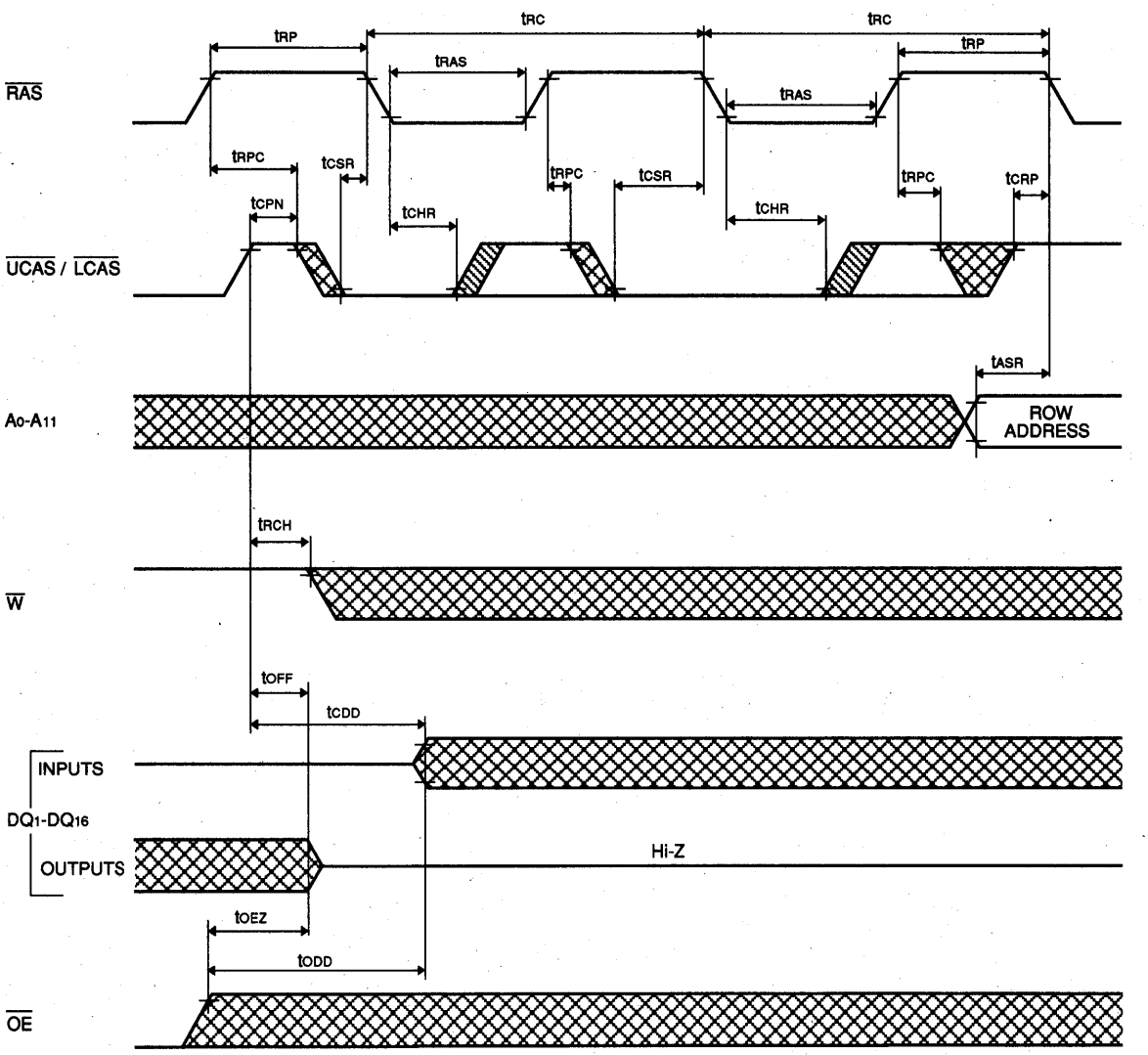
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



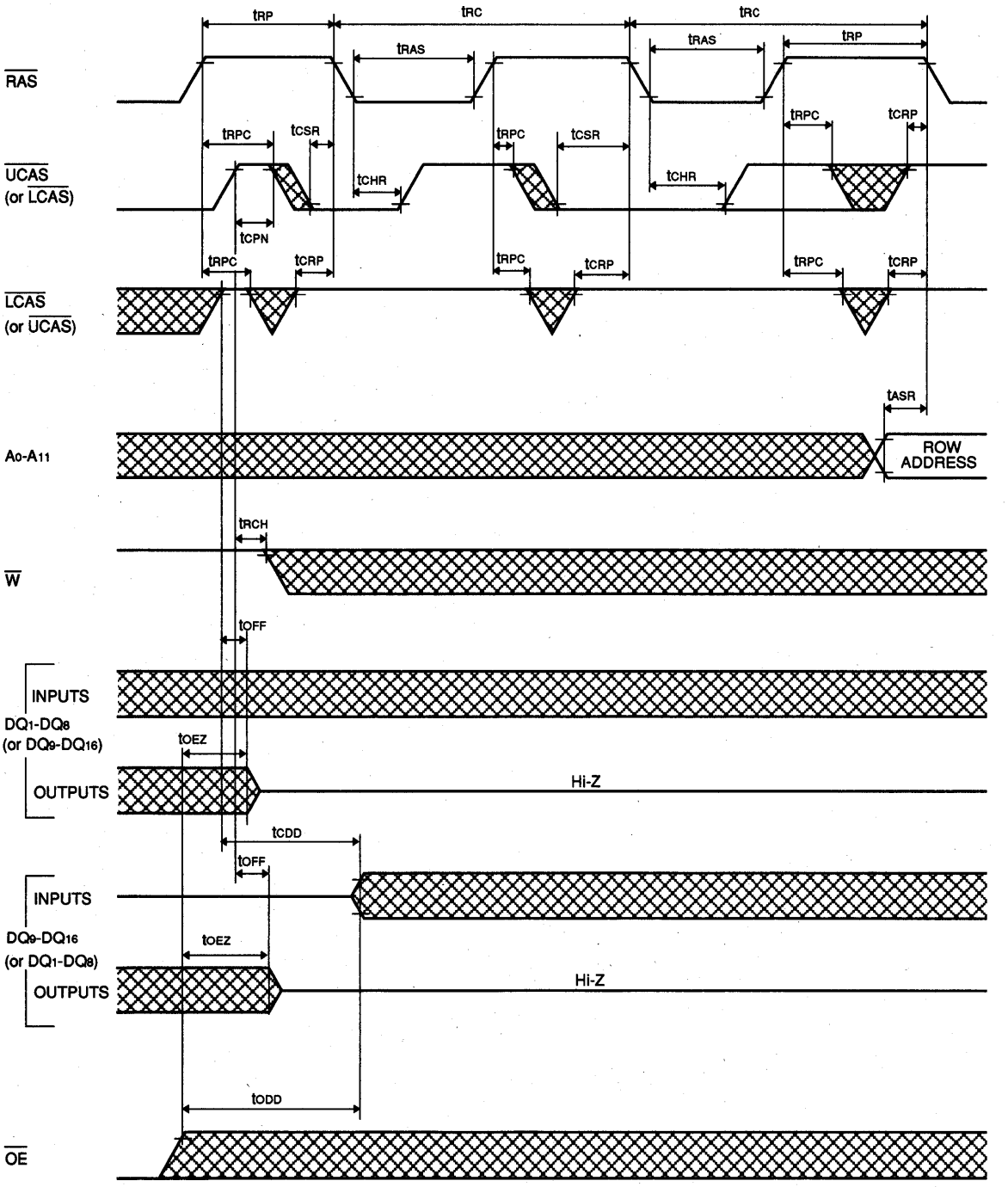
$\overline{\text{RAS}}$-only Refresh Cycle



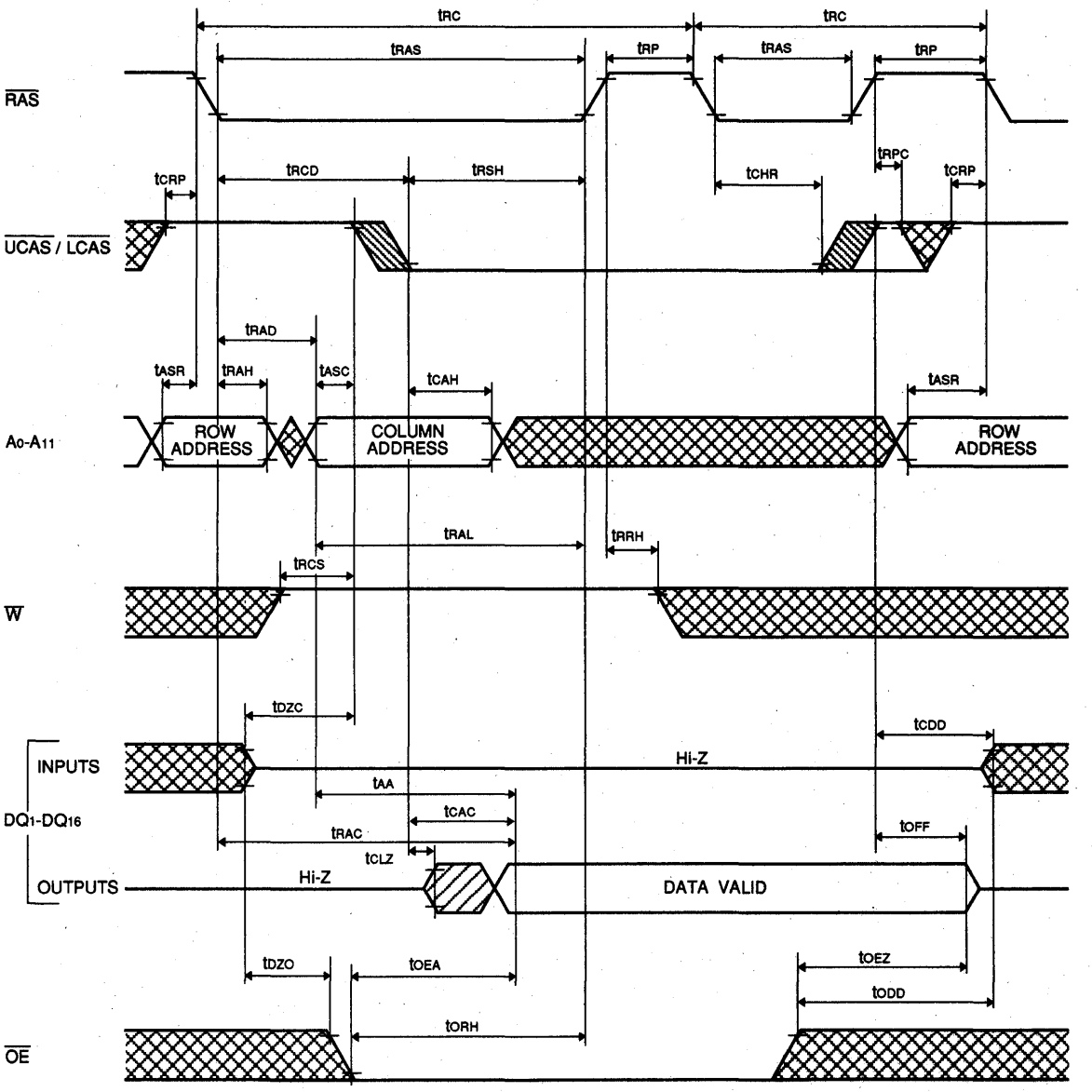
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

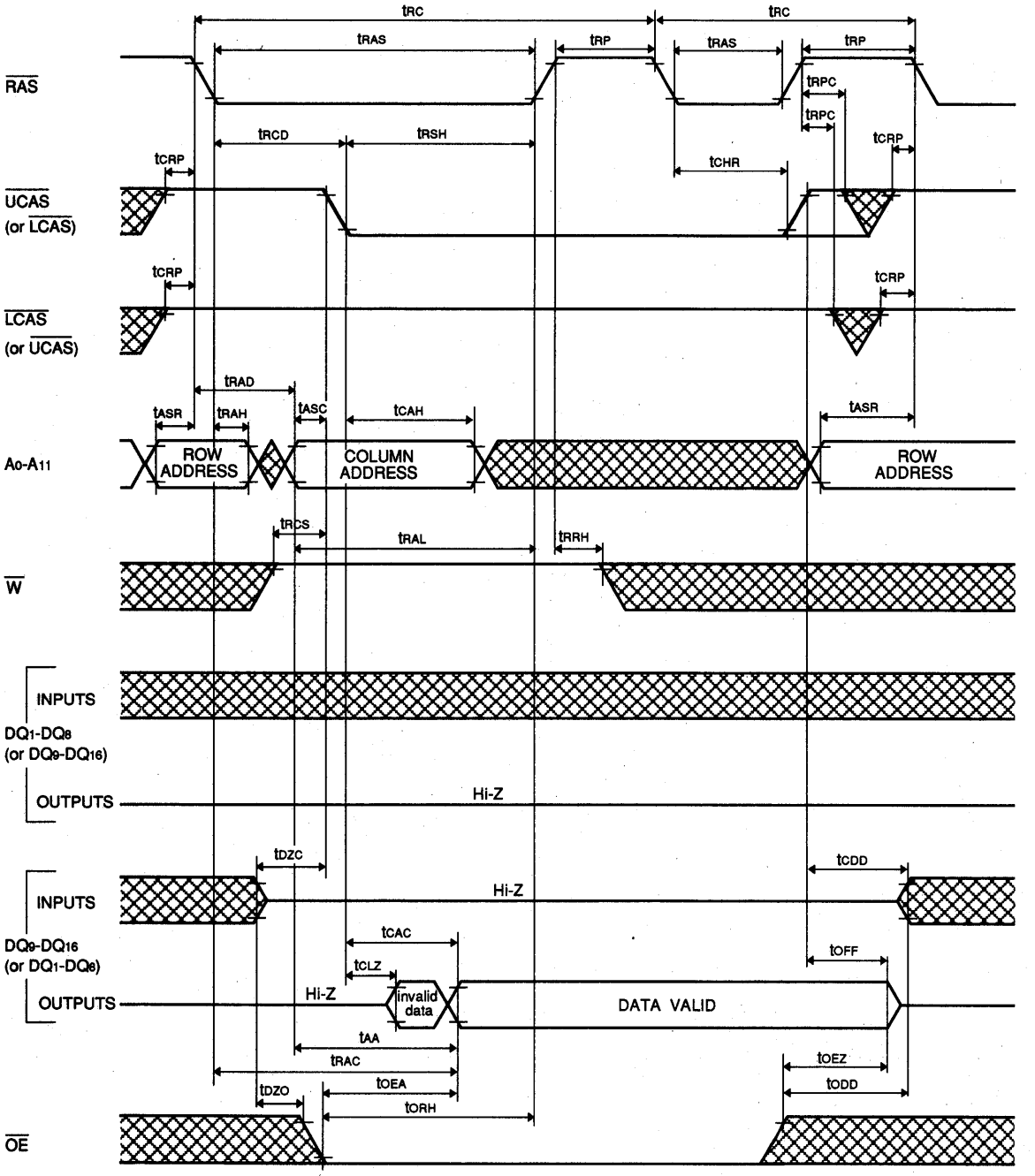


Hidden Refresh Cycle (Read) (Note 29)

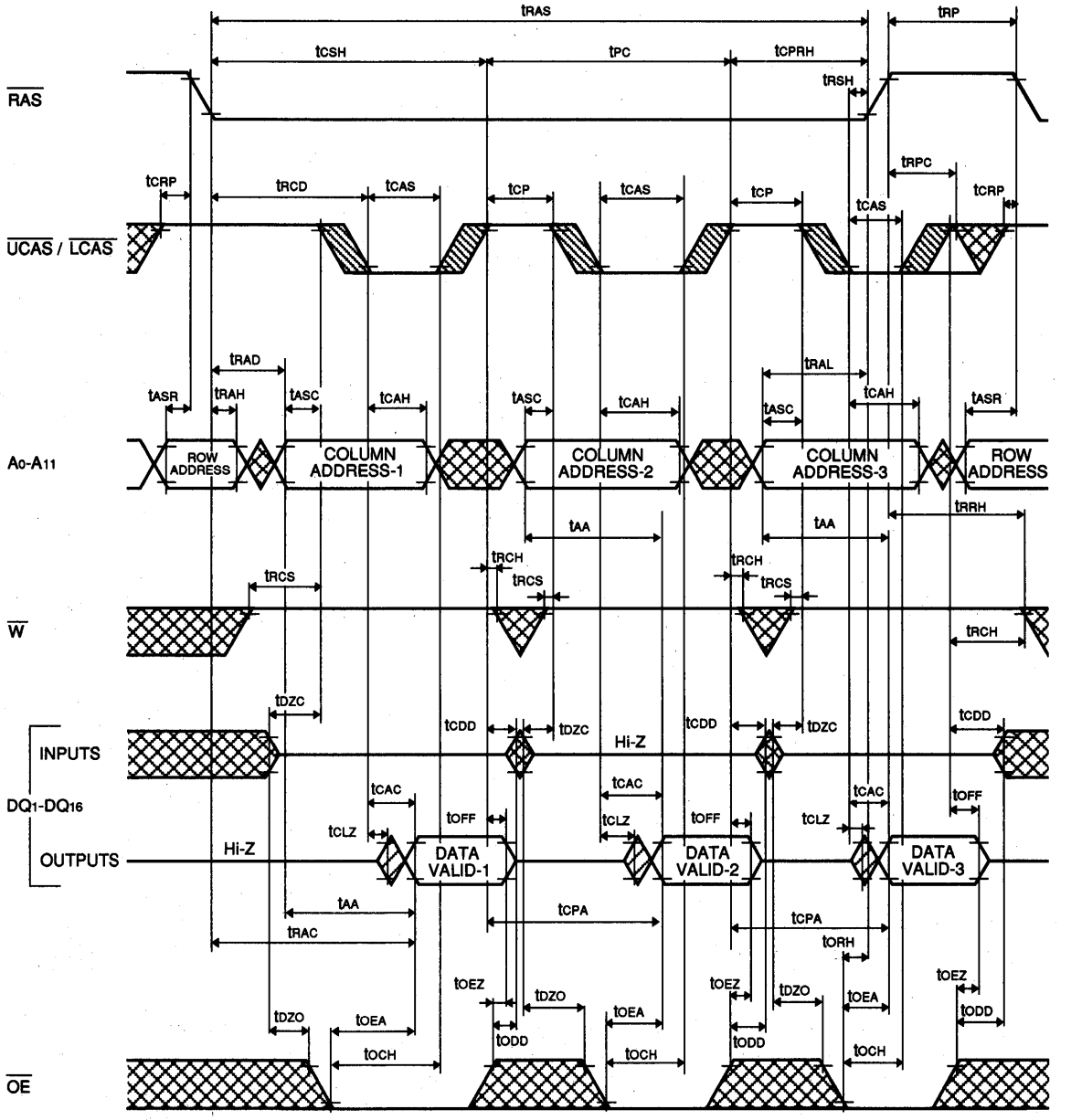


Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

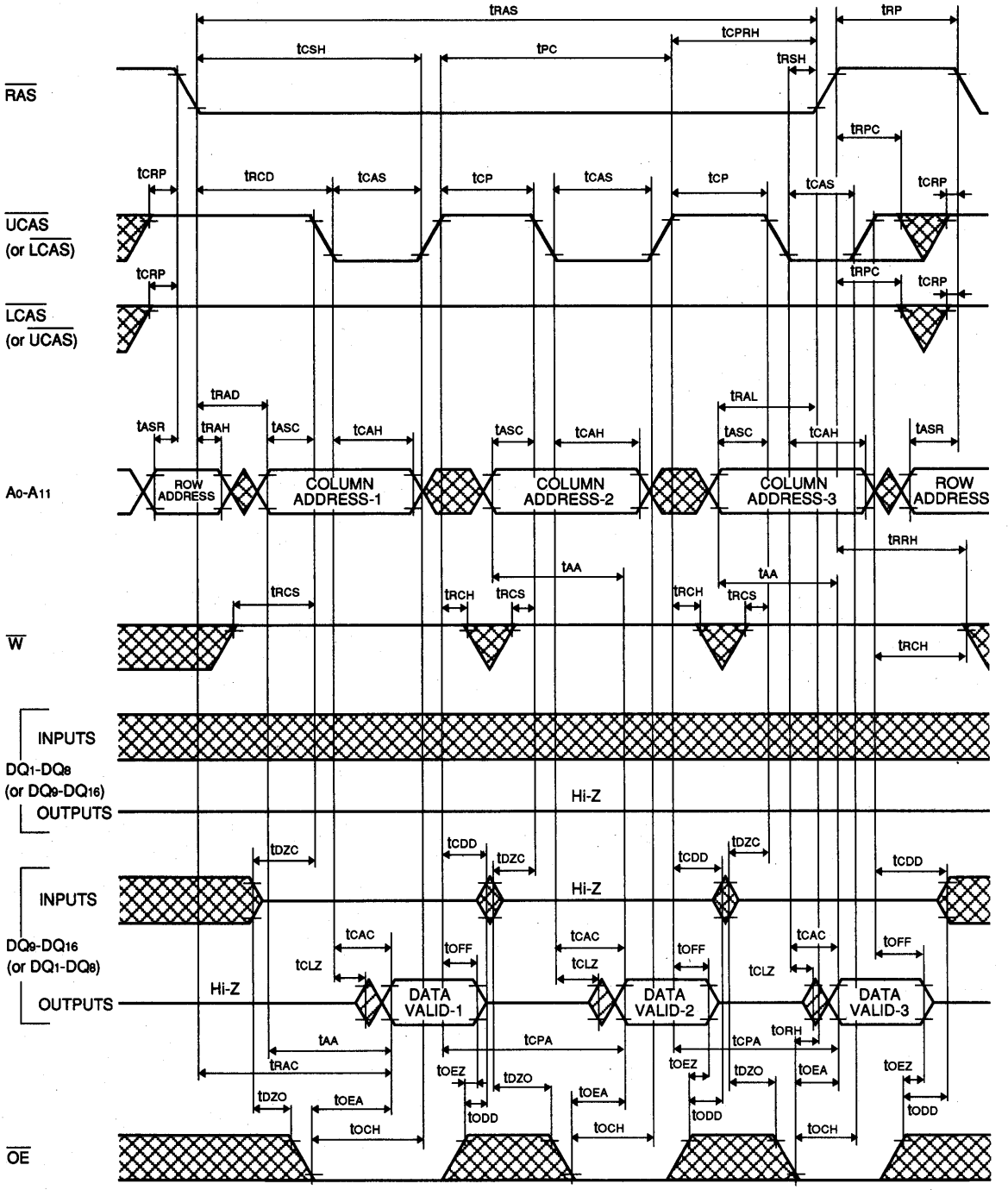
Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



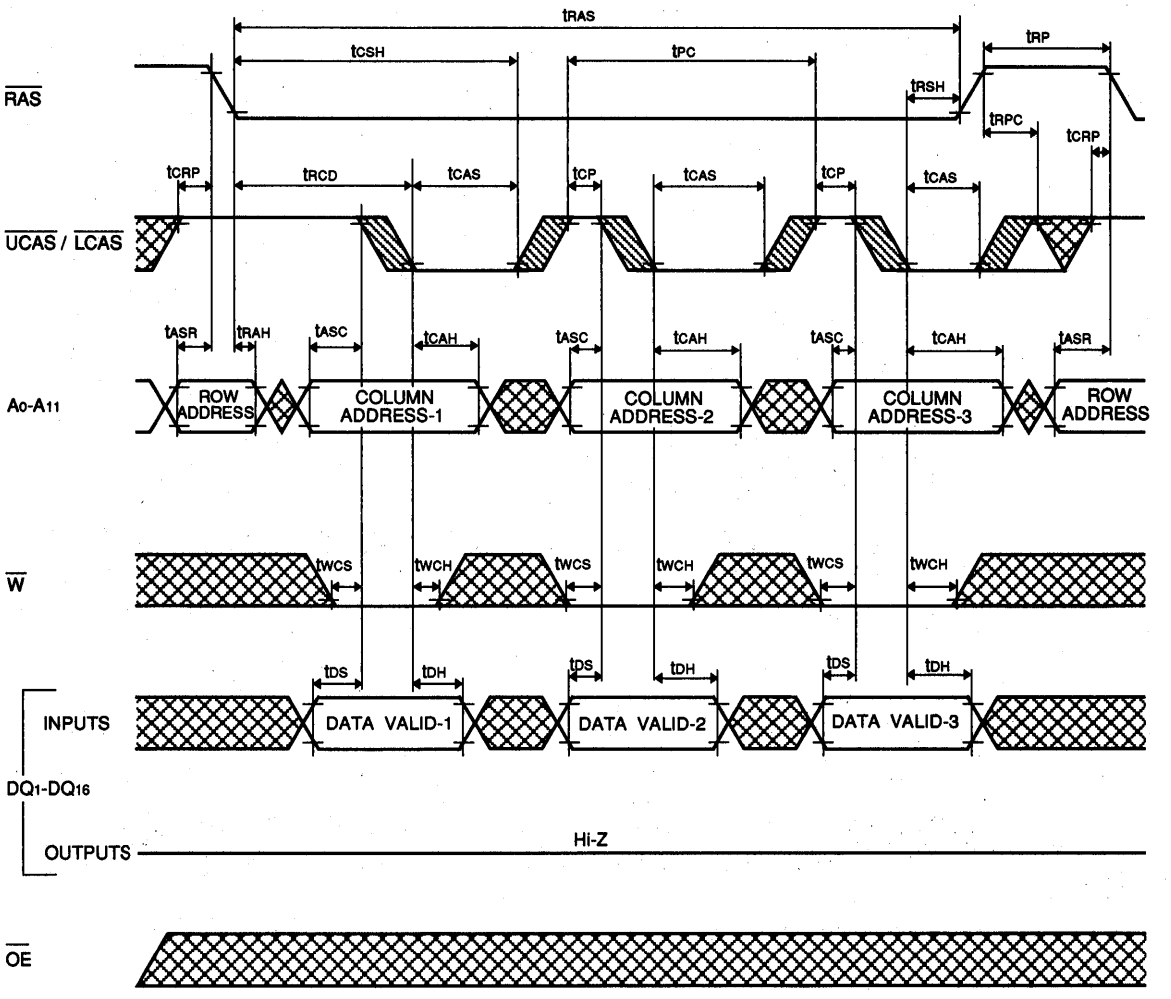
Fast Page Mode Read Cycle



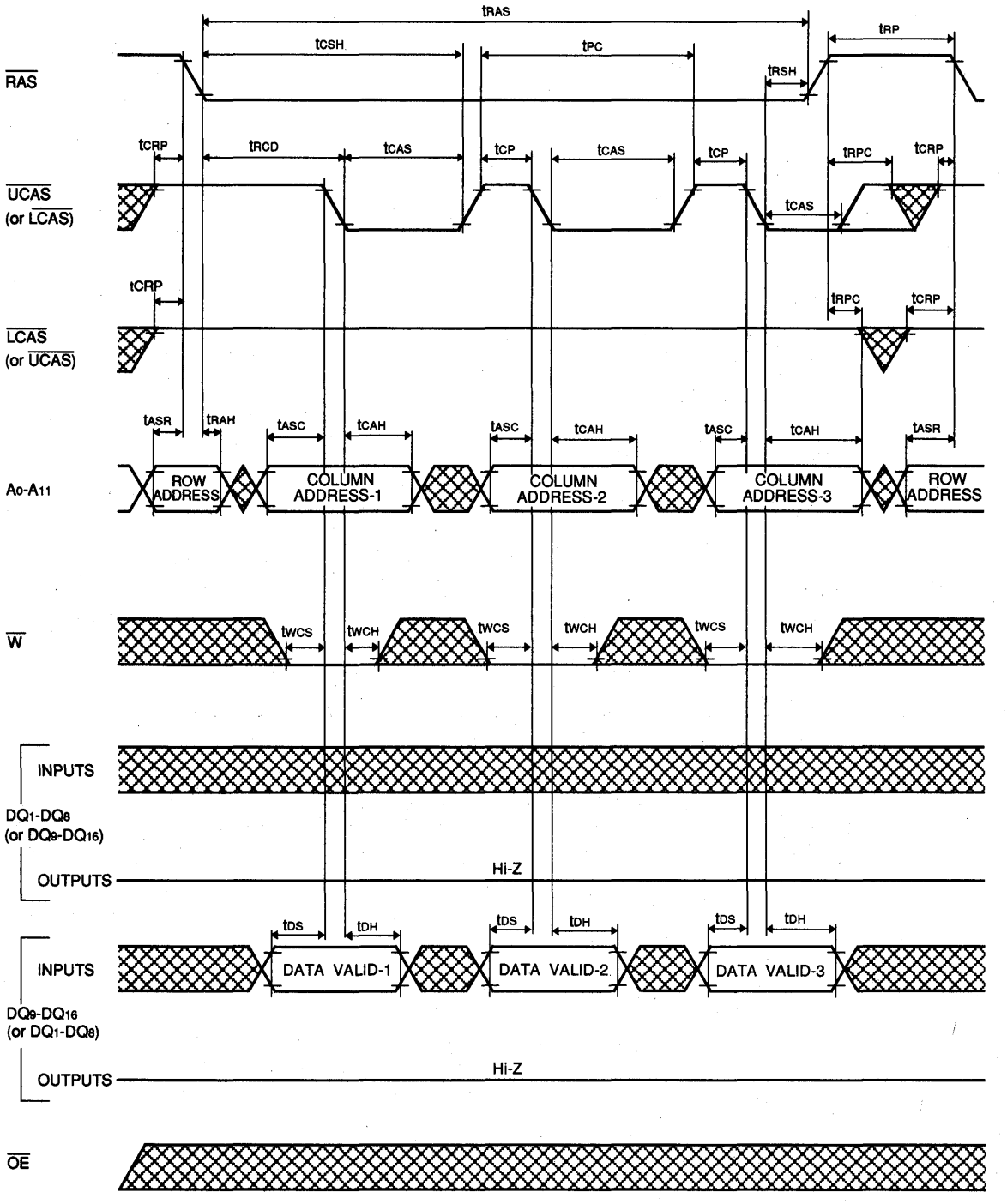
Upper/(Lower) Fast Page Mode Read Cycle



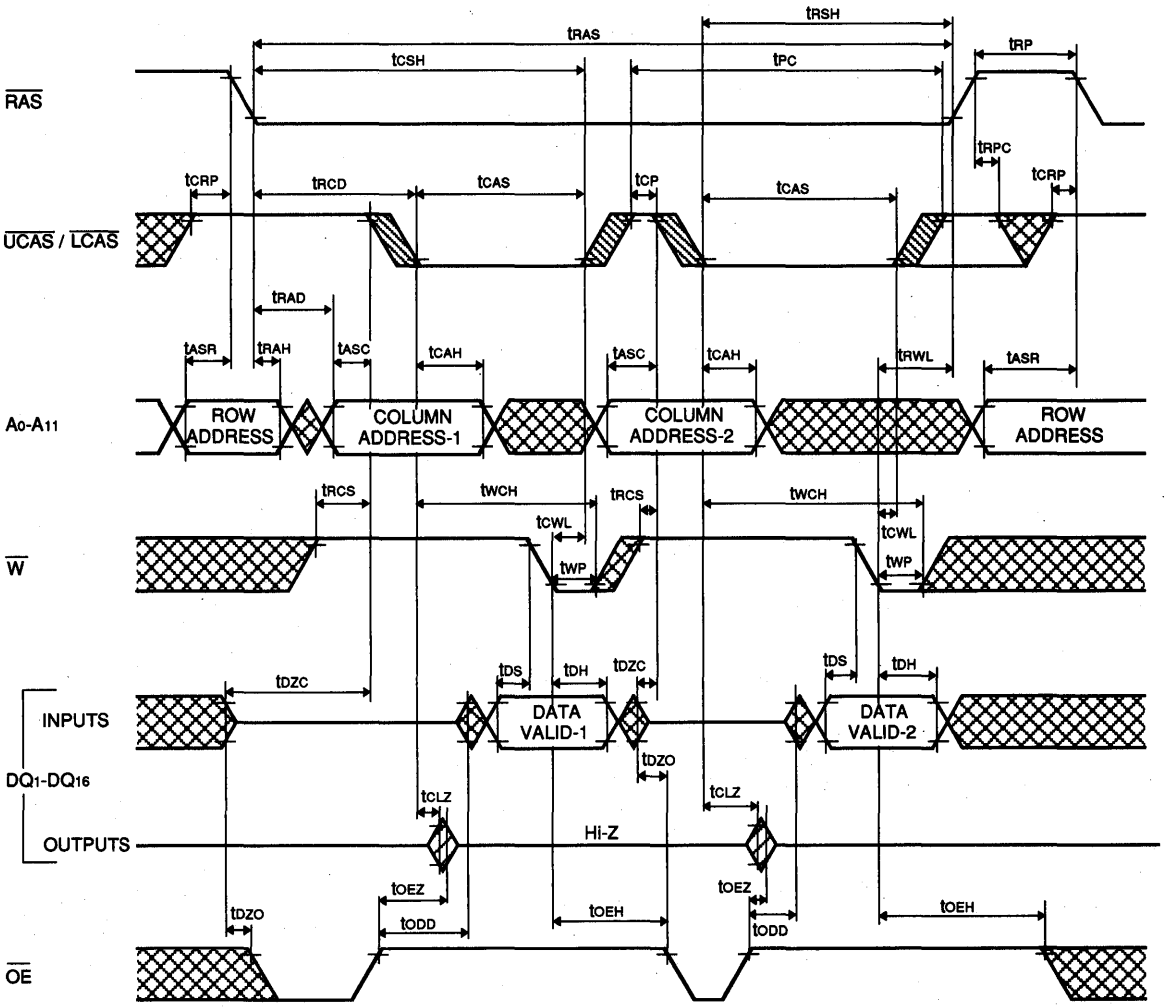
Fast Page Mode Write Cycle (Early Write)



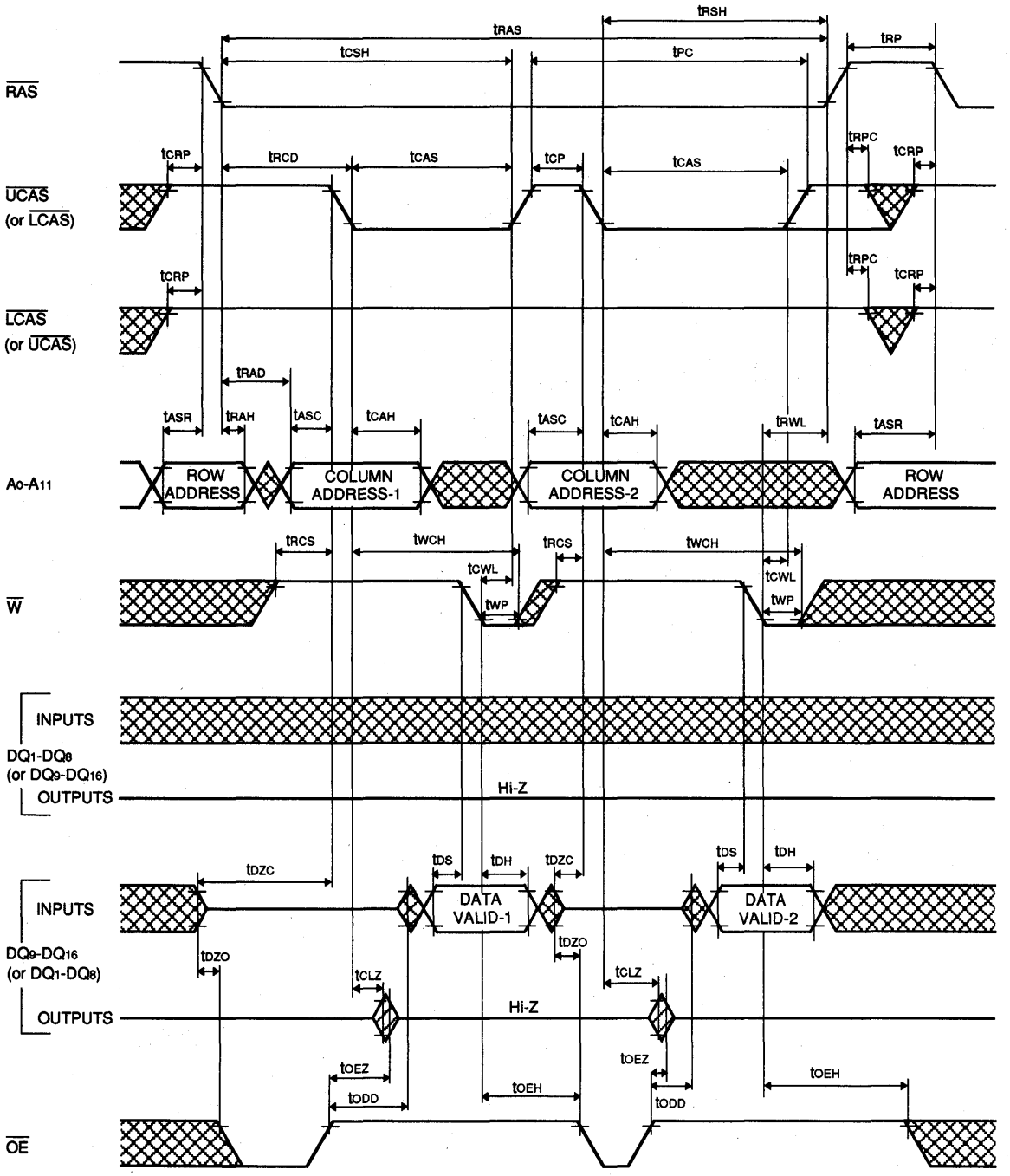
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



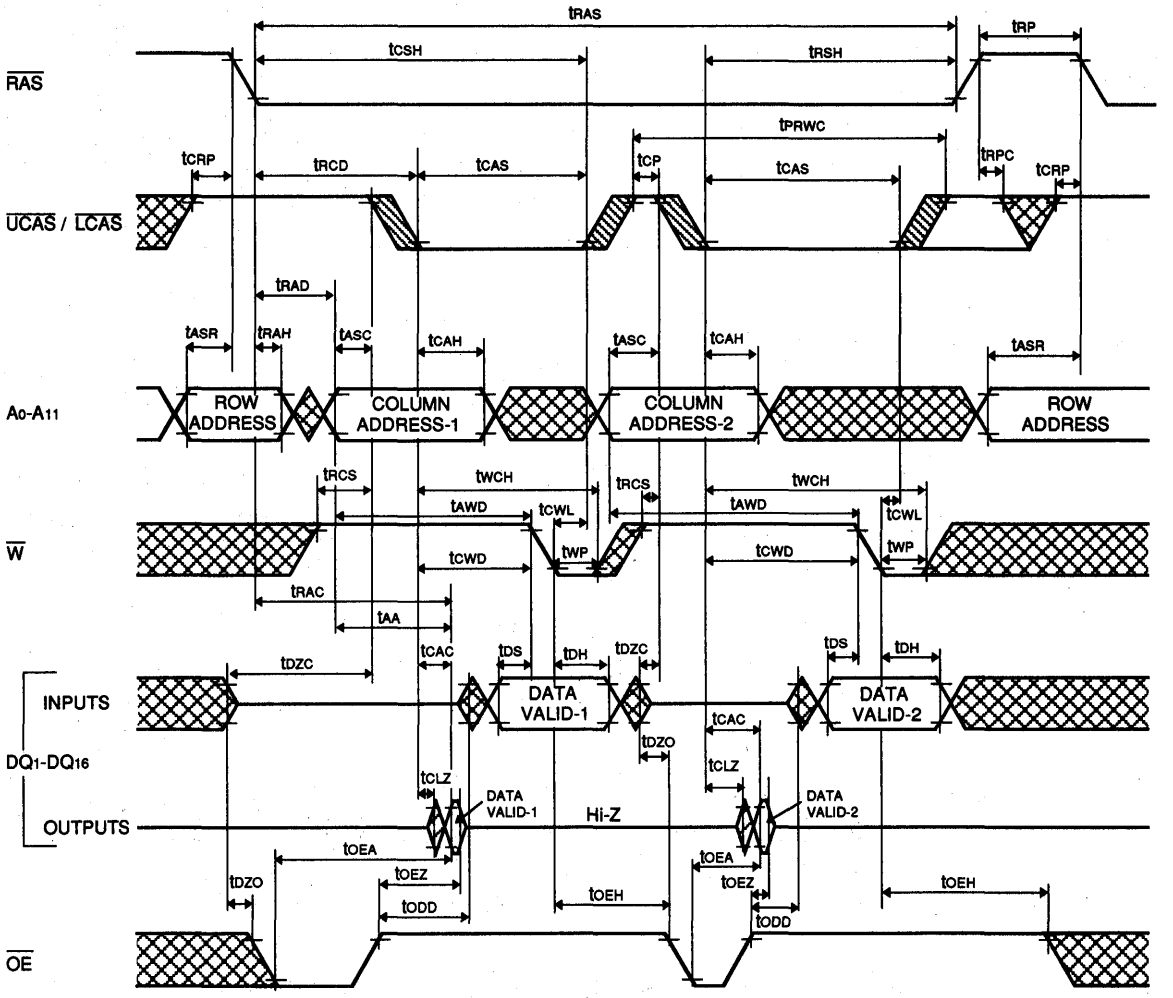
Fast Page Mode Write Cycle (Delayed Write)



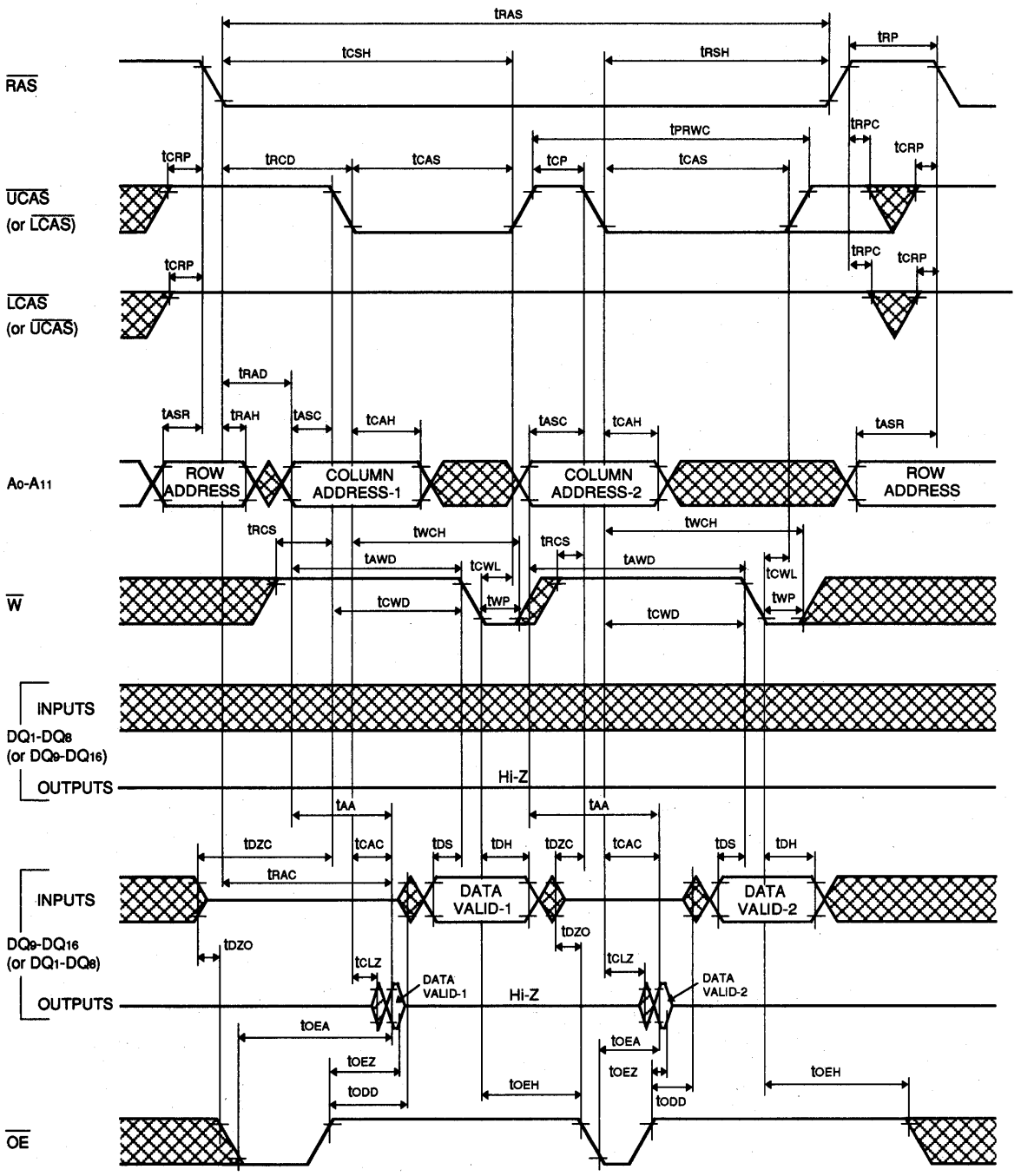
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S . The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8}	Supply current from Vcc Extended refresh cycle	M5M4V16160B -6S,-7S	$\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$ ≦ 0.2V or ≧ Vcc - 0.2V $\overline{OE}$ ≦ 0.2V or ≧ Vcc - 0.2V A_0~A_{11} ≦ 0.2V or ≧ Vcc - 0.2V DQ = open t_{REF} = 128ms t_{RAS} = t_{RAS} min~1 μs			400	μA
I_{CC9} (AV)	Average supply current from Vcc Self - Refresh cycle	M5M4V16160B -6S,-7S	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			200	μA

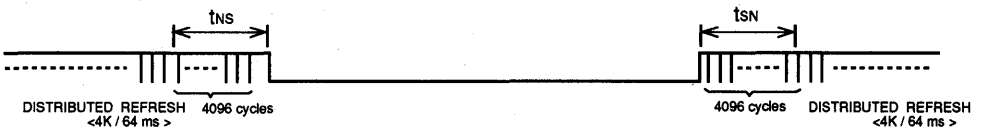
TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M4V16160B-6S		M5M4V16160B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

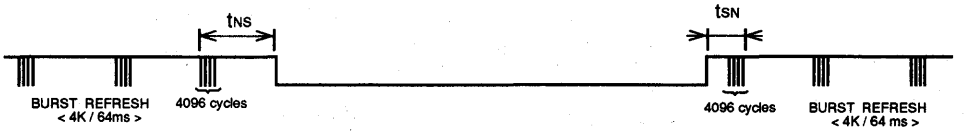
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} ≦ 64 ms and t_{SN} ≦ 64 ms.

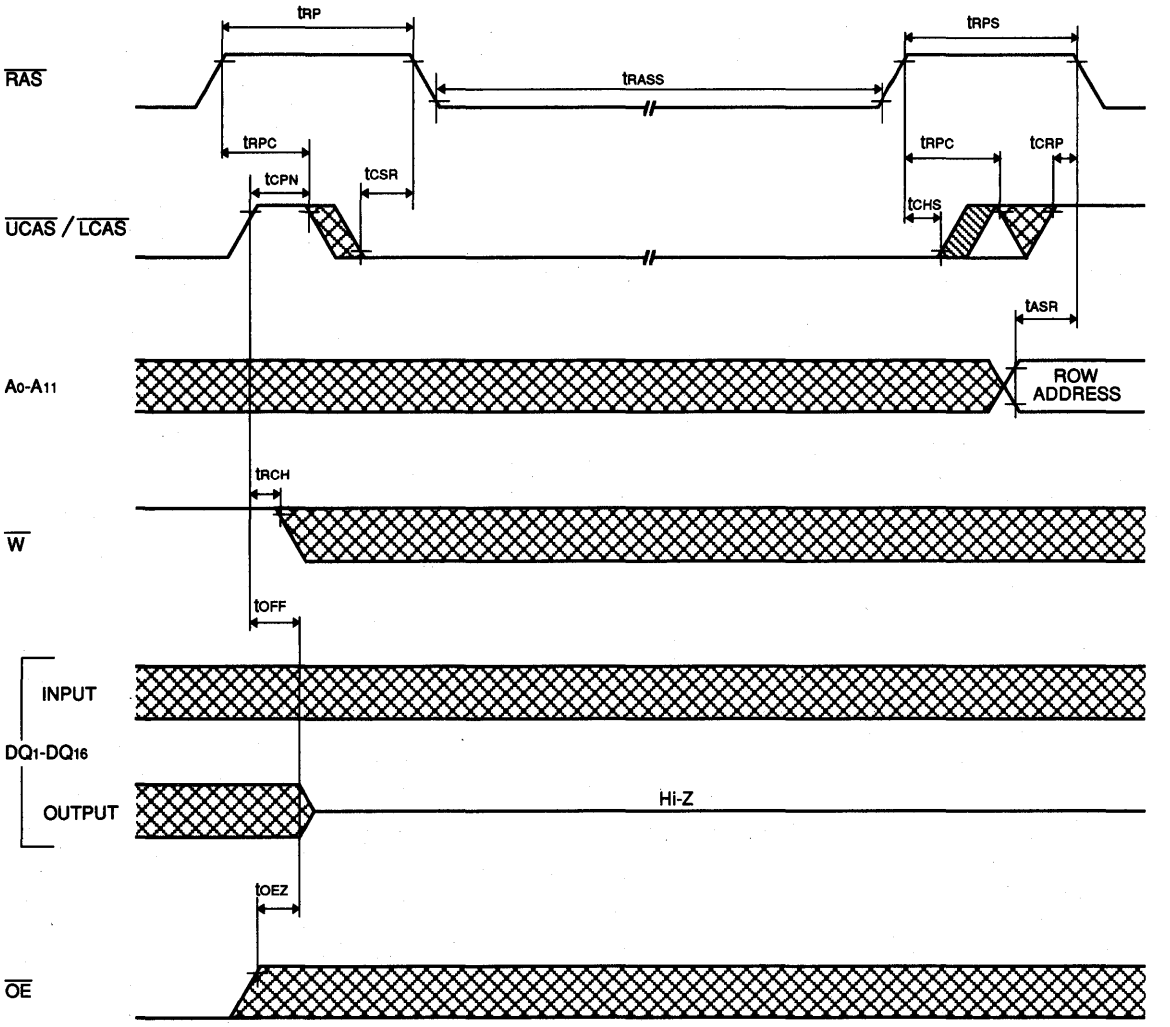


(2) In case of burst refresh

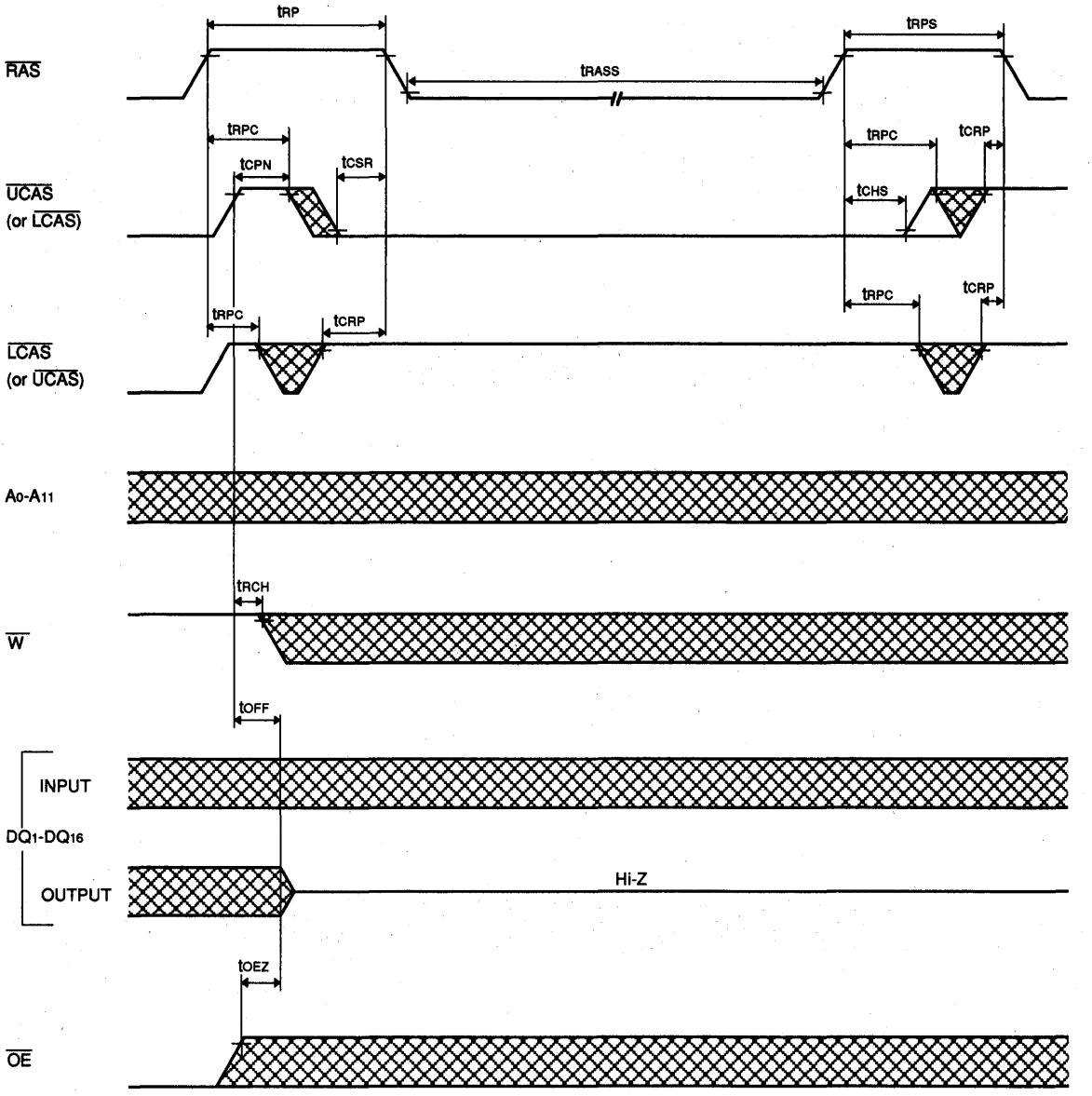
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} + t_{SN} ≦ 64 ms.



Self Refresh Cycle



Upper/(Lower) Self Refresh Cycle*



M5M4V18160BTP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

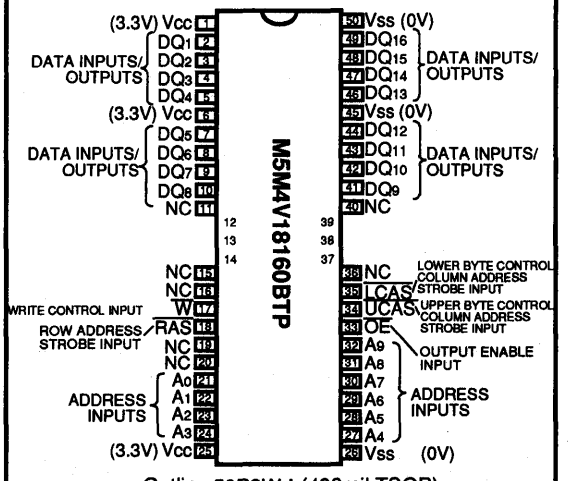
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18160BTP-6,-6S	60	15	30	15	110	450
M5M4V18160BTP-7,-7S	70	20	35	20	130	390

- Standard 50pin TSOP
- Single 3.3V ± 0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ..... CMOS Input level
- Low operating power dissipation
  M5M4V18160BTP -6, -6S ..... 620.0mW (Max)
  M5M4V18160BTP-7, -7S ..... 540.0mW (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 50P3W-L(400mil TSOP)

NC : NO CONNECTION

FUNCTION

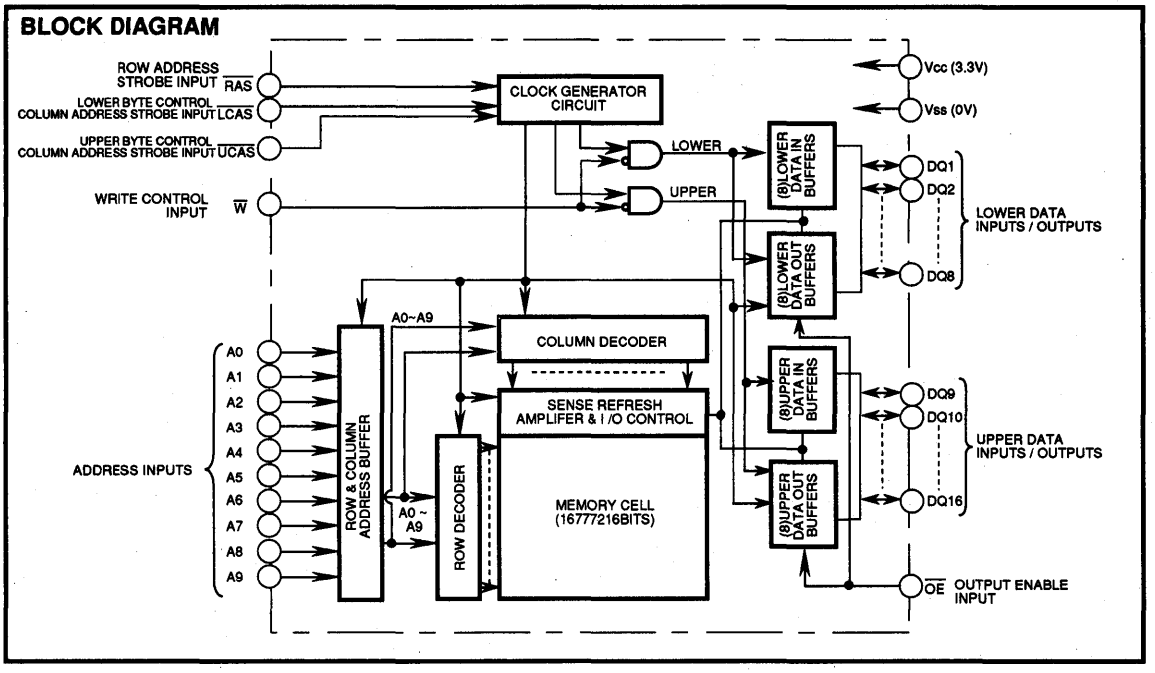
The M5M4V18160BTP provide, in addition to normal read, write, and read-modify-write operations, a number of otherv functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
Vo	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦Vcc+0.3V,Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M4V18160B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			170	mA
		M5M4V18160B-7,-7S				150	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V18160B-6,-7	$\overline{RAS}$= $\overline{CAS}$≧Vcc-0.2V, output open			0.5	
		M5M4V18160B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$≧Vcc-0.2V, output open			0.15	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M4V18160B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			170	mA
		M5M4V18160B-7,-7S				150	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M4V18160B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			85	mA
		M5M4V18160B-7,-7S				75	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18160B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			170	mA
		M5M4V18160B-7,-7S				150	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, $\overline{W}$ input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V± 0.3V, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note7,8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note7,9)		60		70	ns
tAA	Column address access time	(Note 7,10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 100pF, V_{OH}=2.4V(I_{OH}=-2mA) and V_{OL}=0.4V(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL})
8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\ \mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted , see notes 13,14)

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		16.4		16.4	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note19)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note19)	15		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T =5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
tWC	Write cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
tWP	Write pulse width		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note22)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note23)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note23)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits				Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note25)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note23)	60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

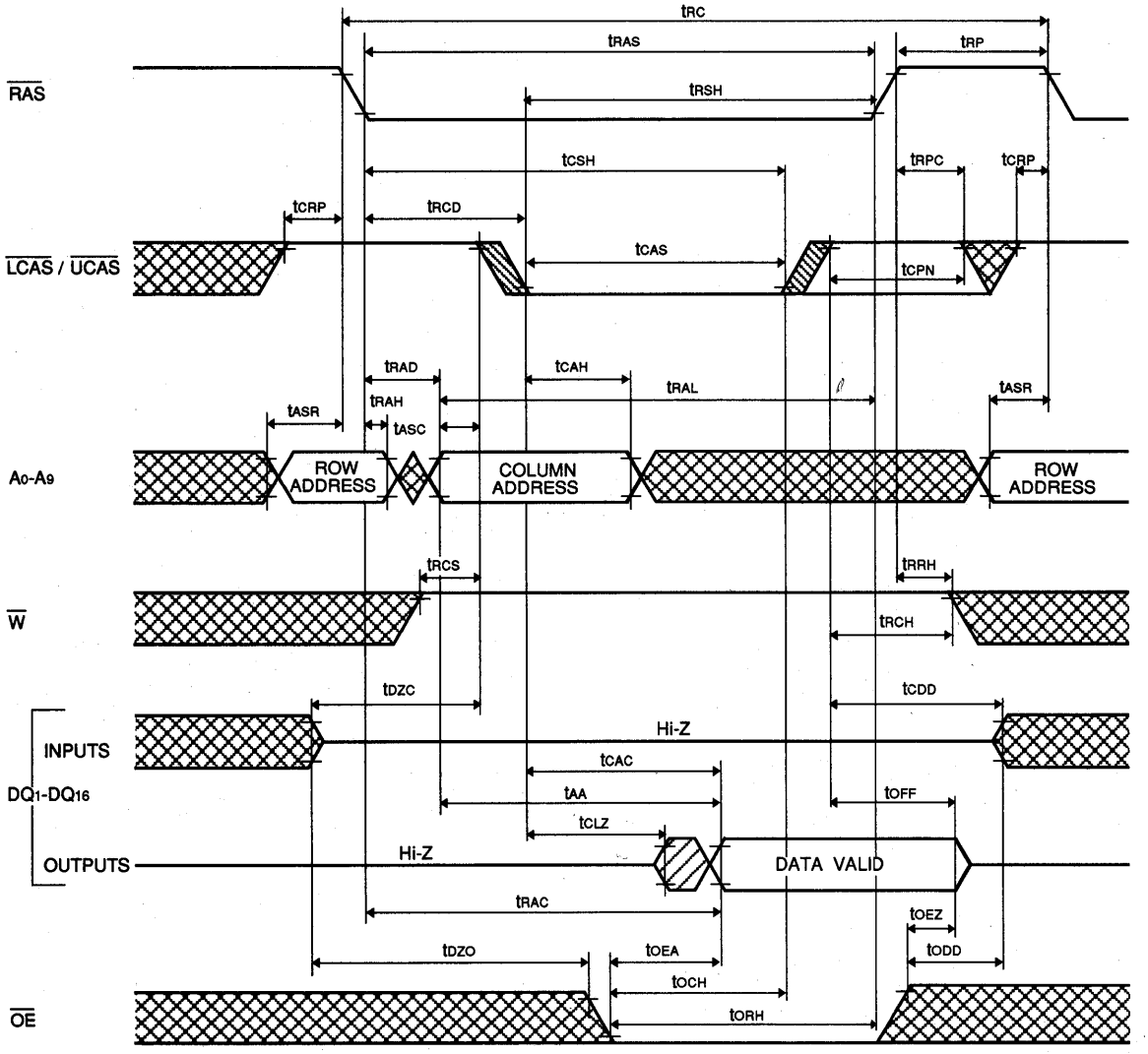
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



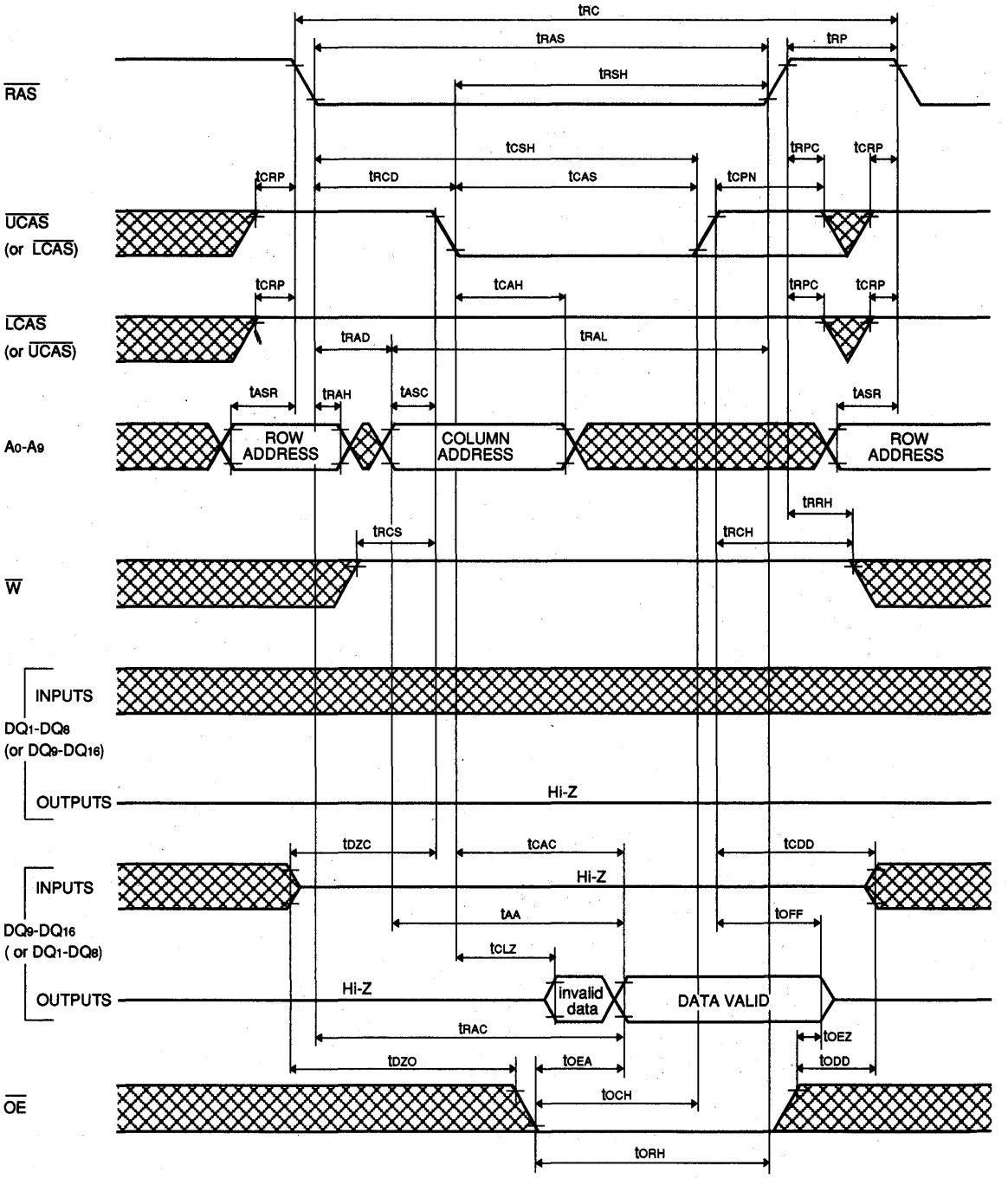
Note 28

Indicates the don't care input.
$V_{IH(min.)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min.)} \leq V_{IN} \leq V_{IL(max)}$

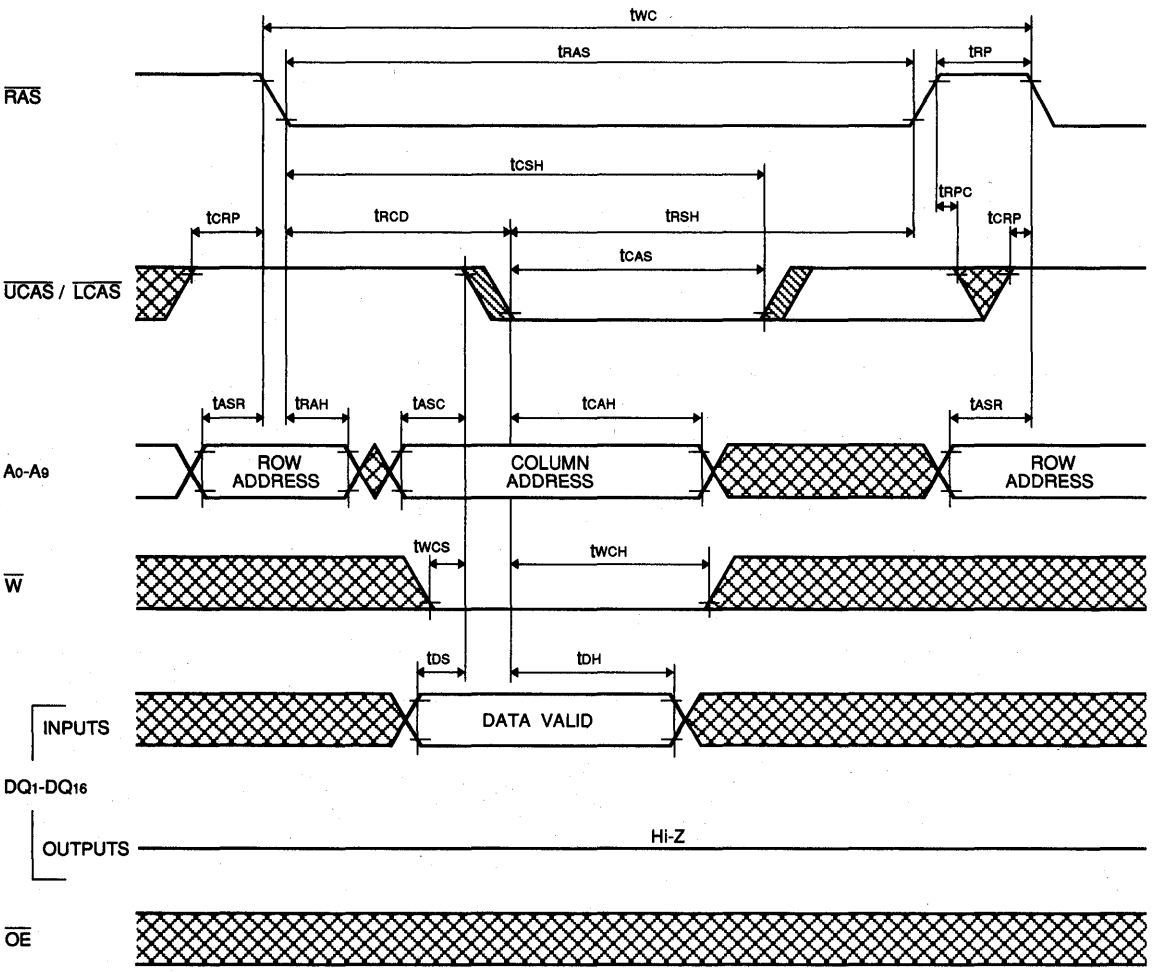
Indicates the invalid output.

Indicates the skew of the two inputs.

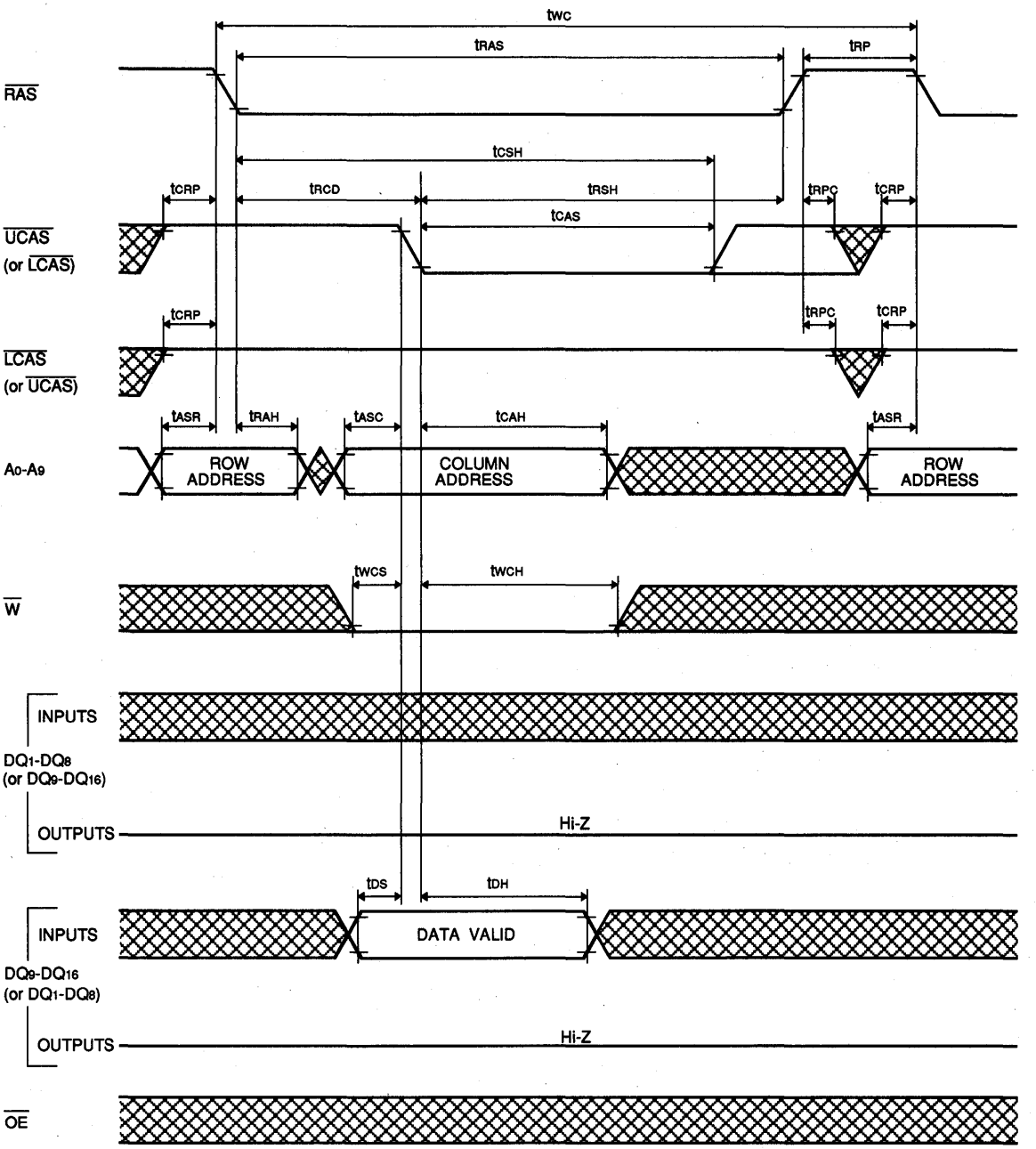
Upper / (Lower) Byte Read Cycle



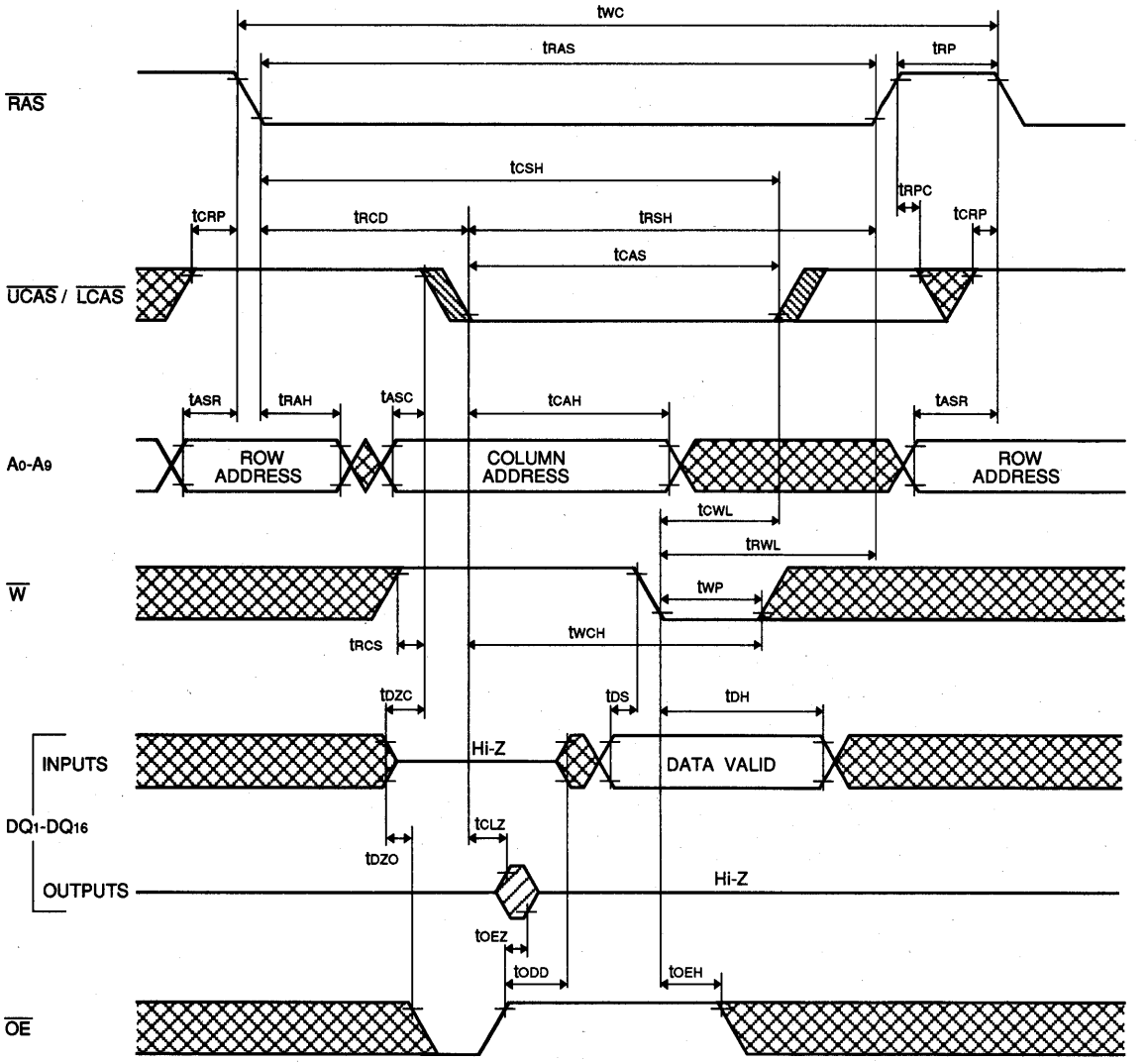
Write Cycle (Early write)



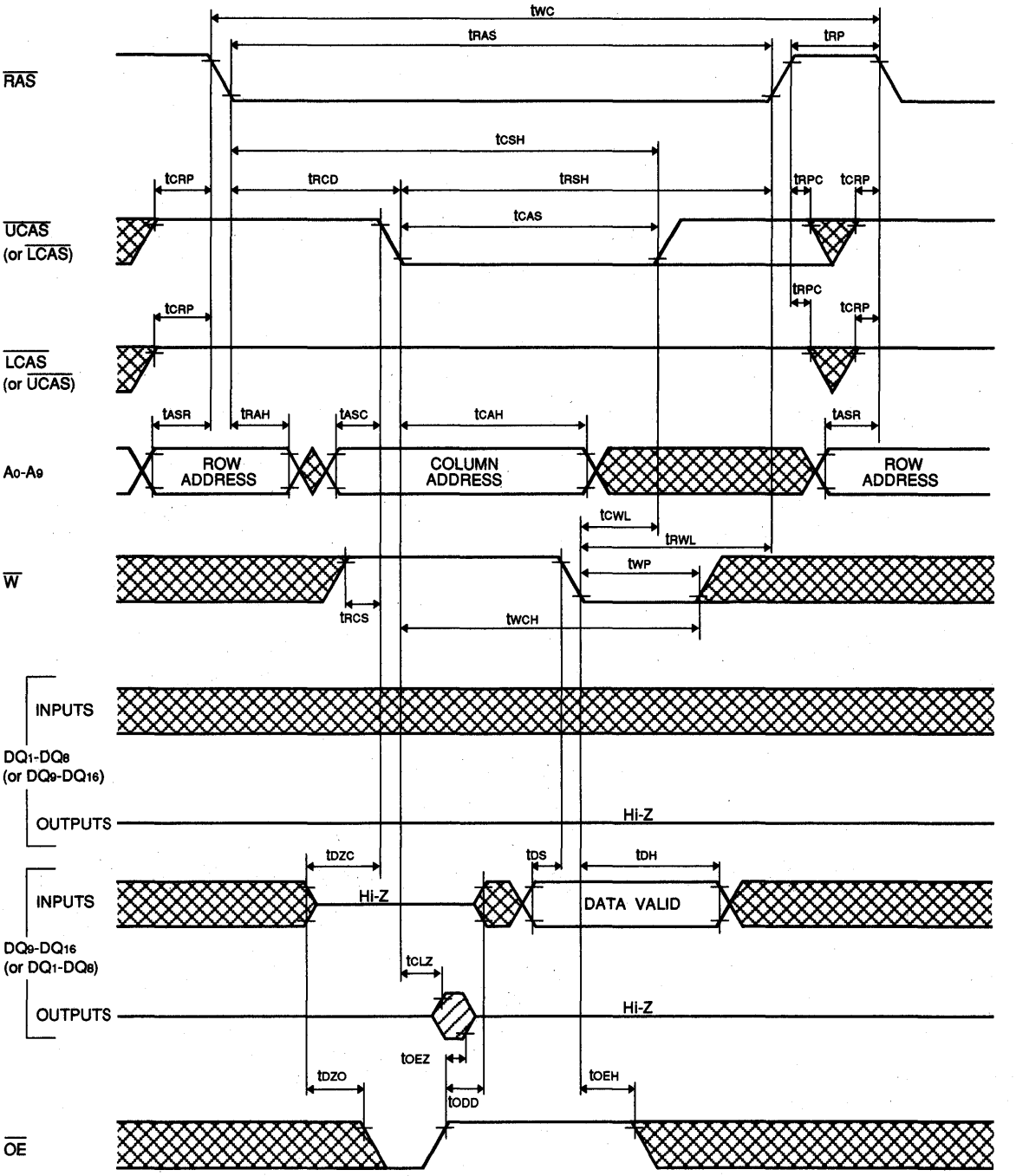
Upper/(Lower) Byte Write Cycle (Early write)



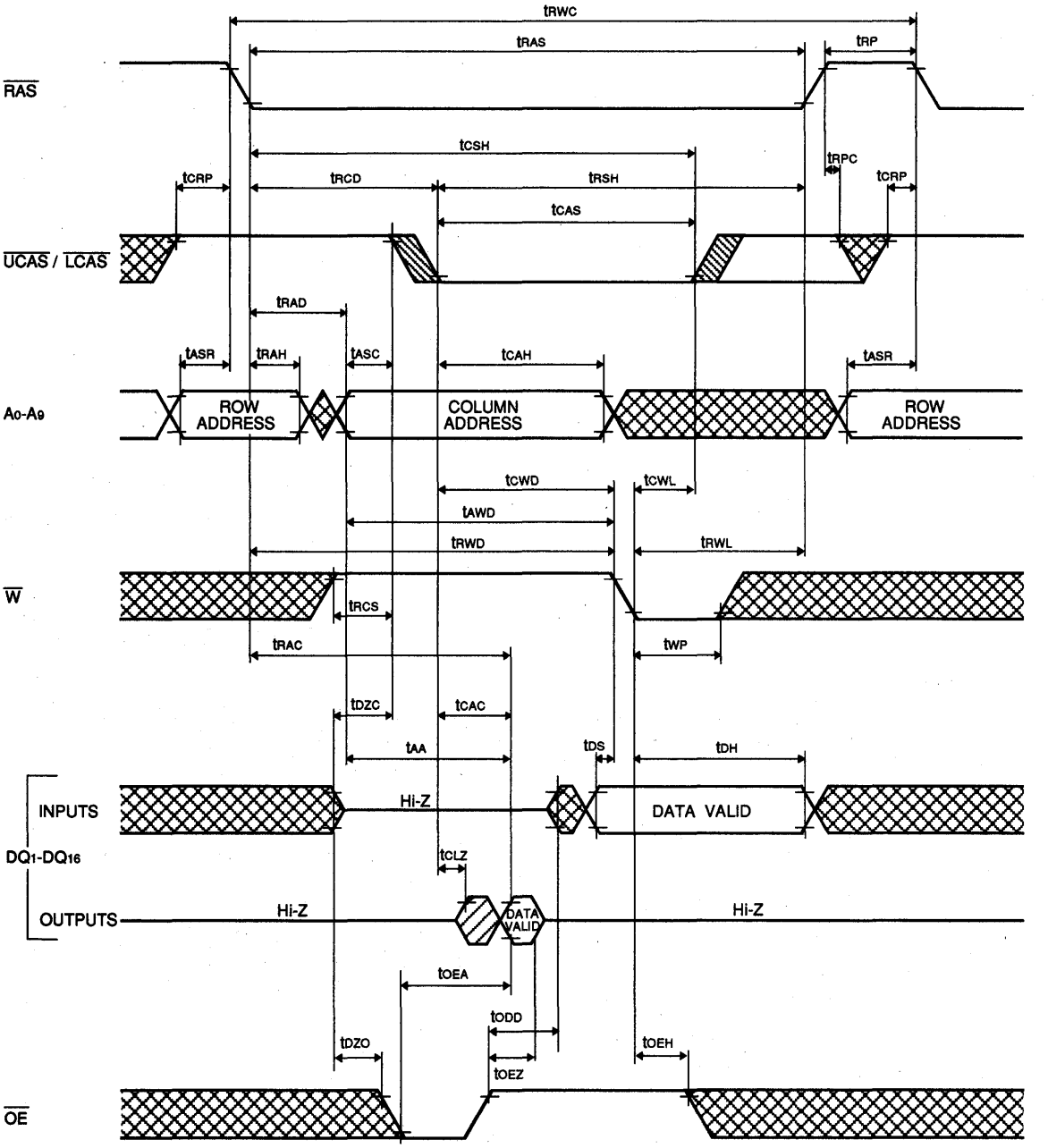
Write Cycle (Delayed write)



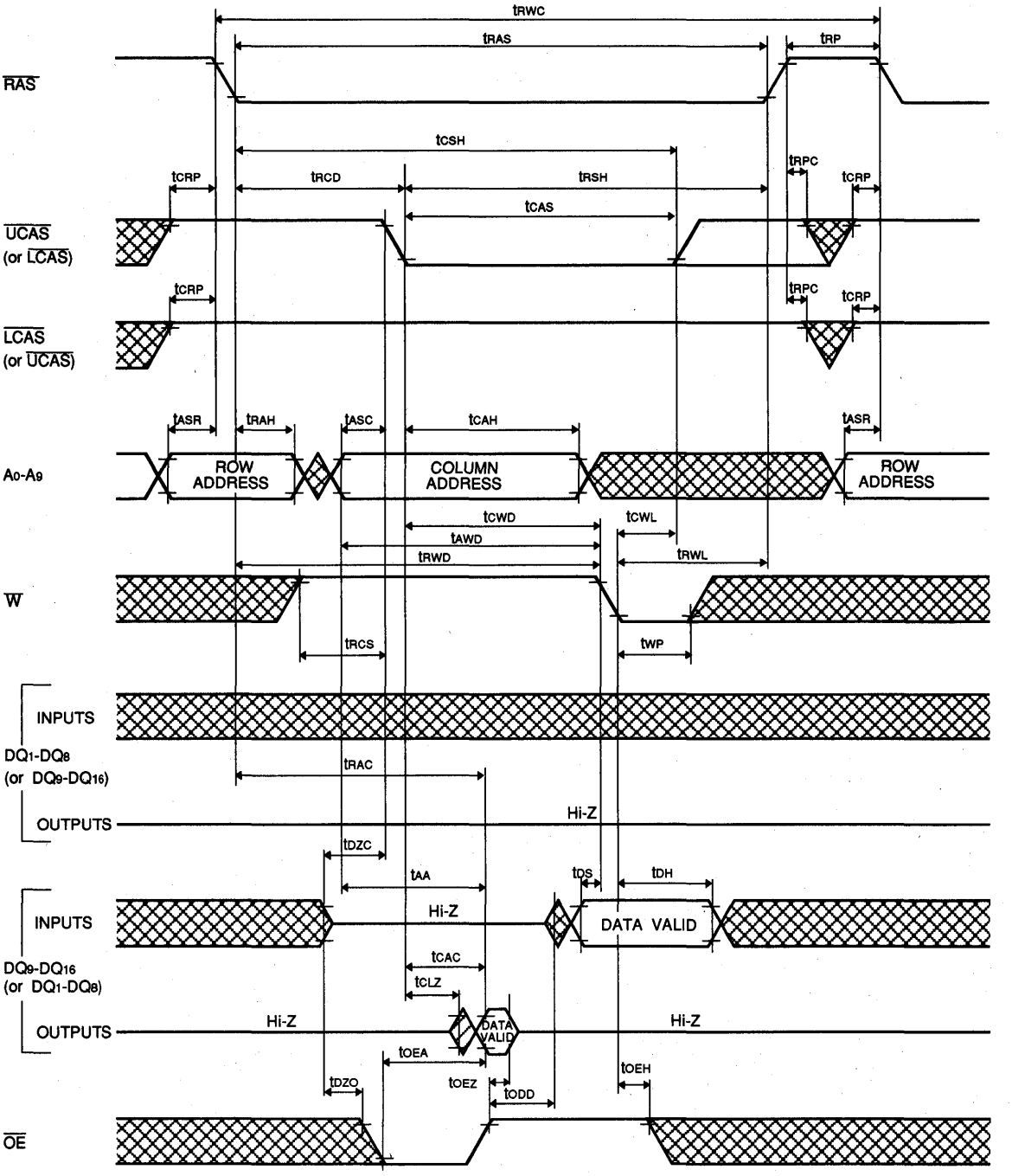
Upper/(Lower) Byte Write Cycle (Delayed write)



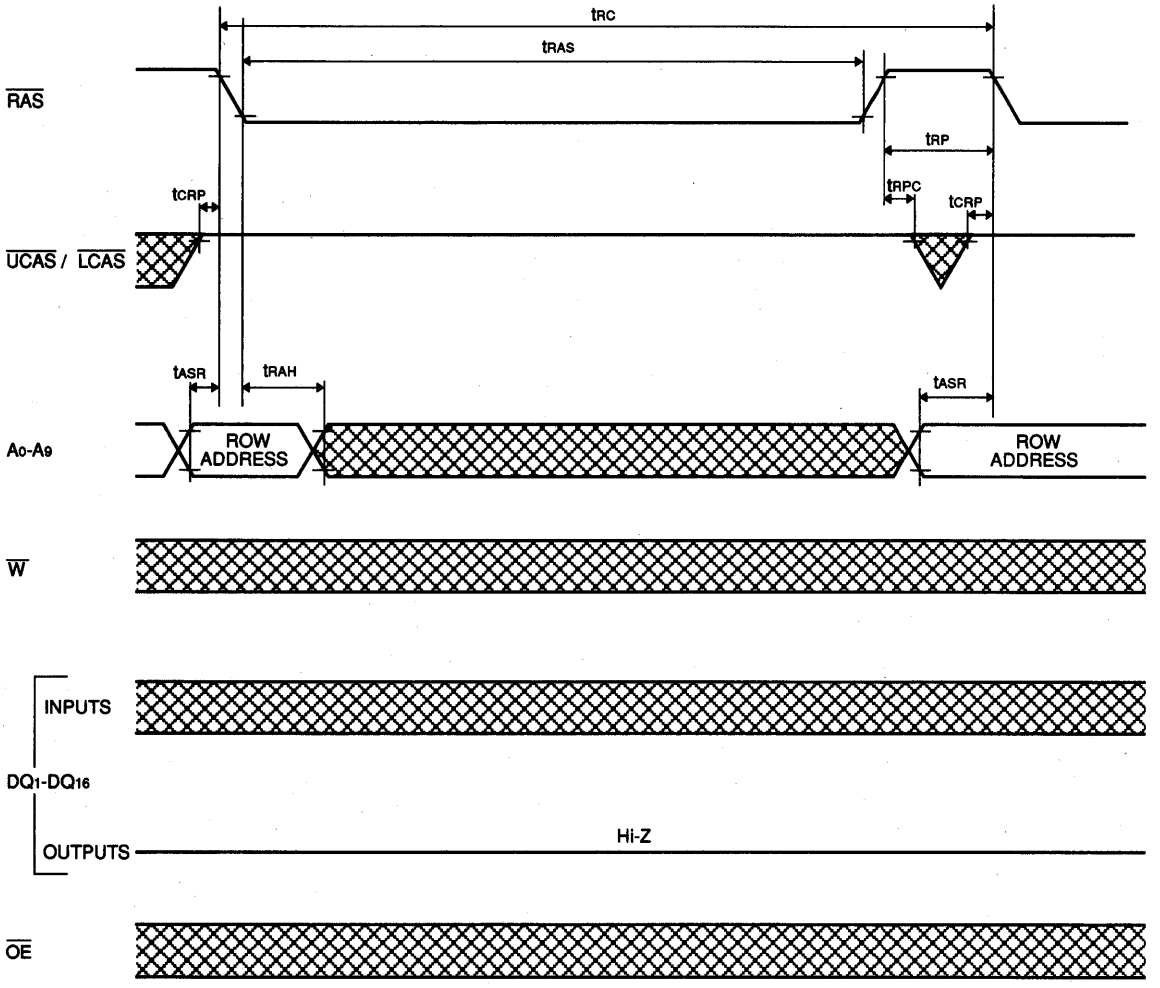
Read-Write, Read-Modify-Write Cycle



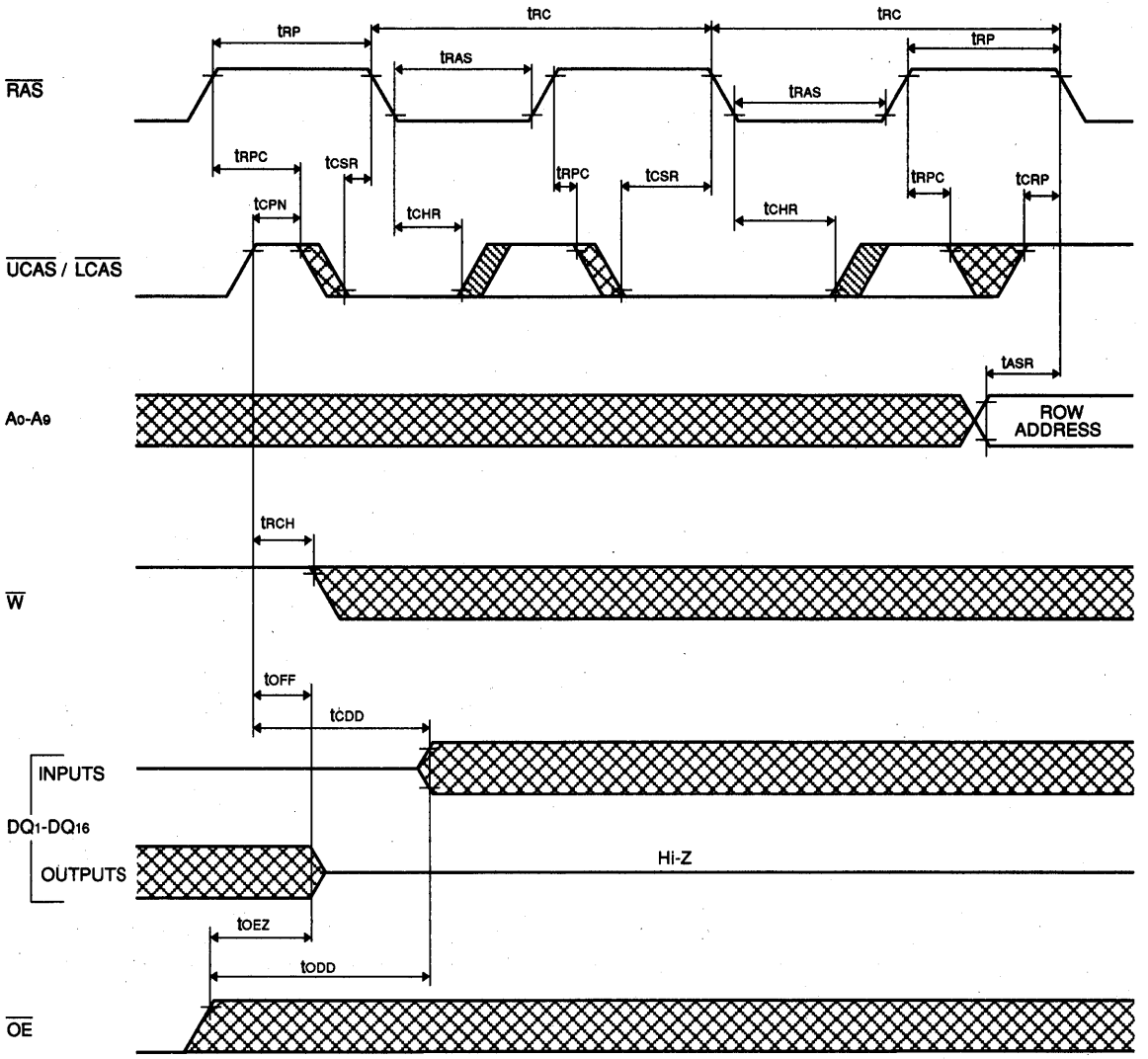
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



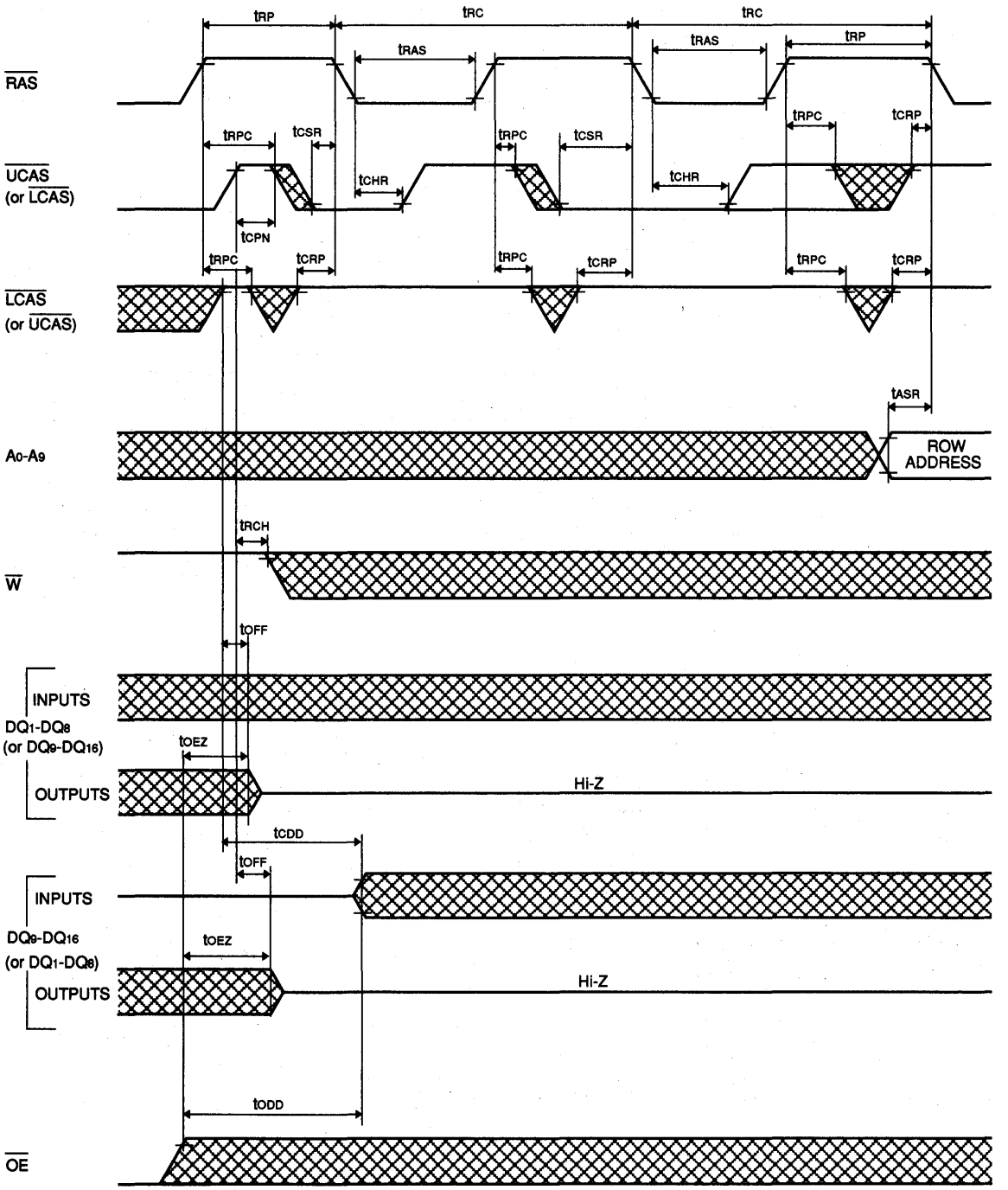
$\overline{\text{RAS}}$-only Refresh Cycle



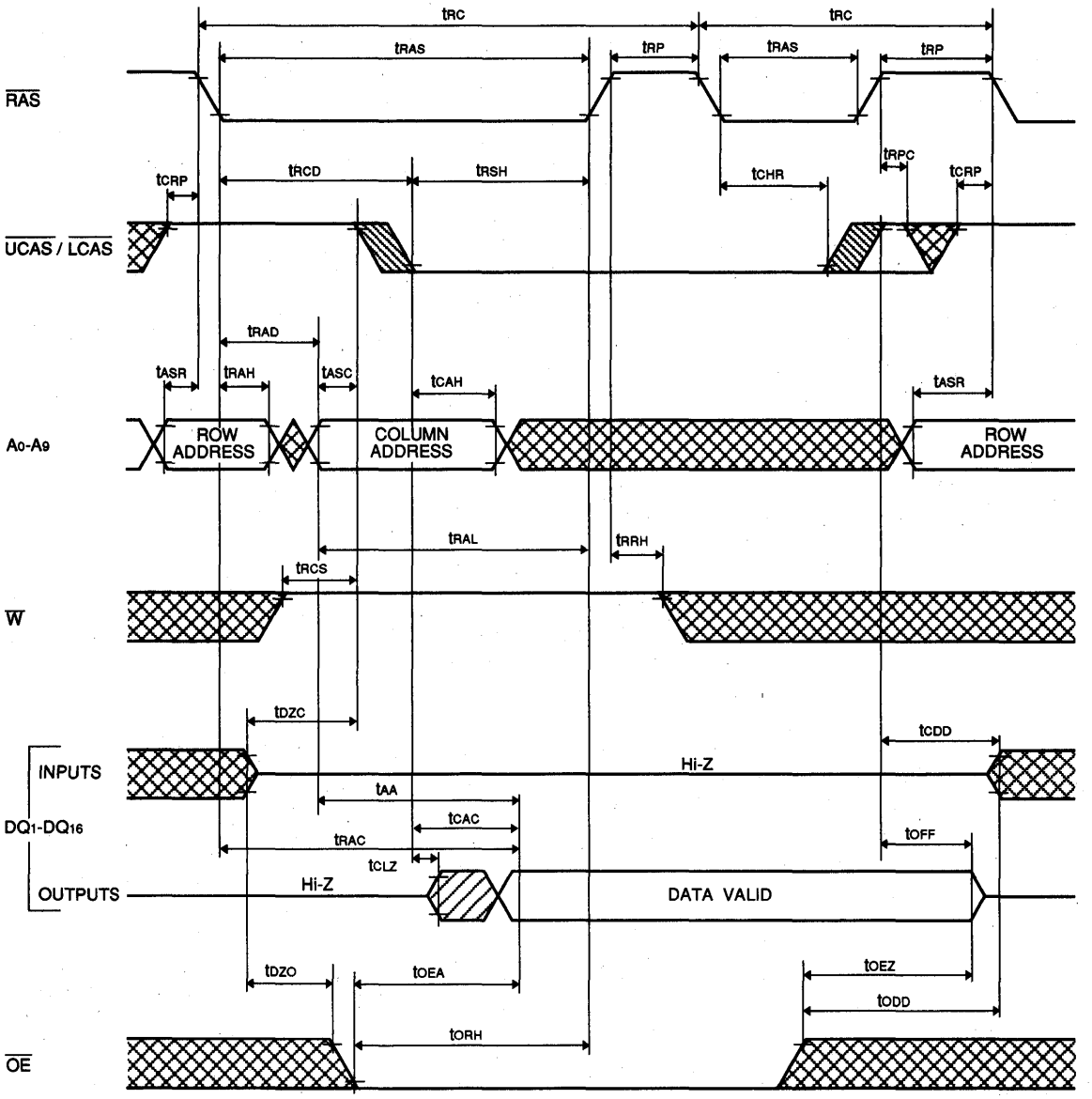
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

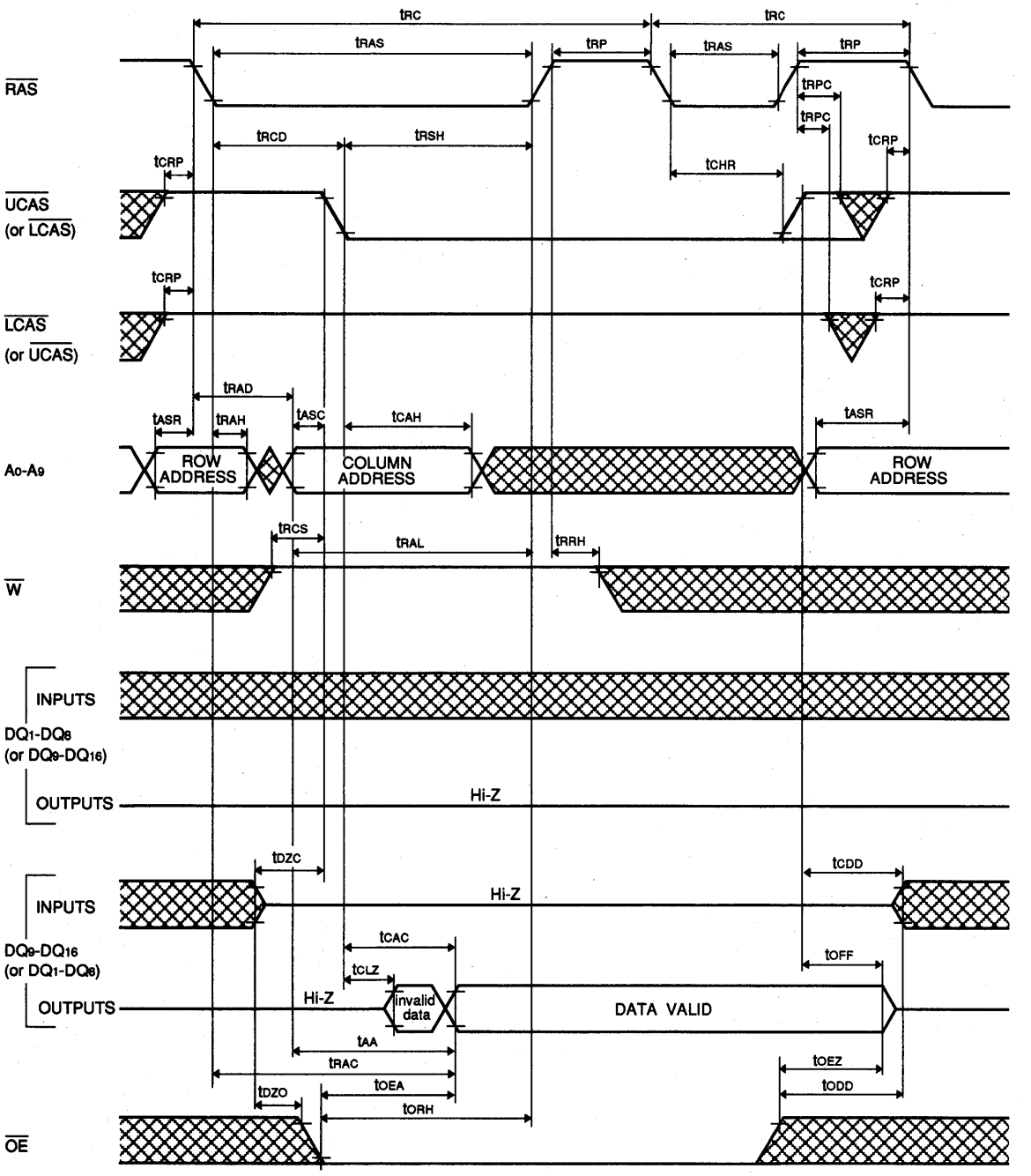


Hidden Refresh Cycle (Read) (Note 29)

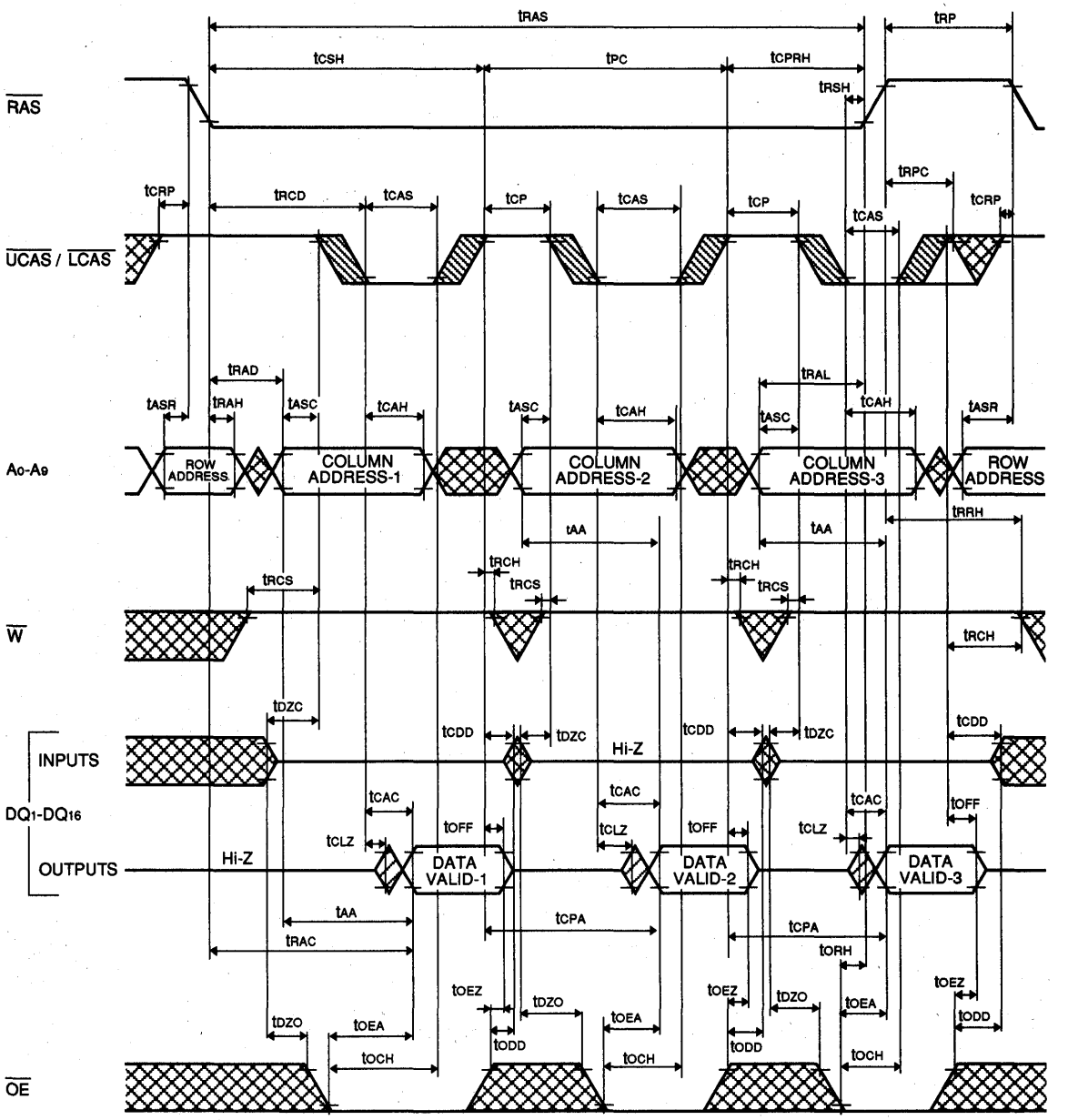


Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

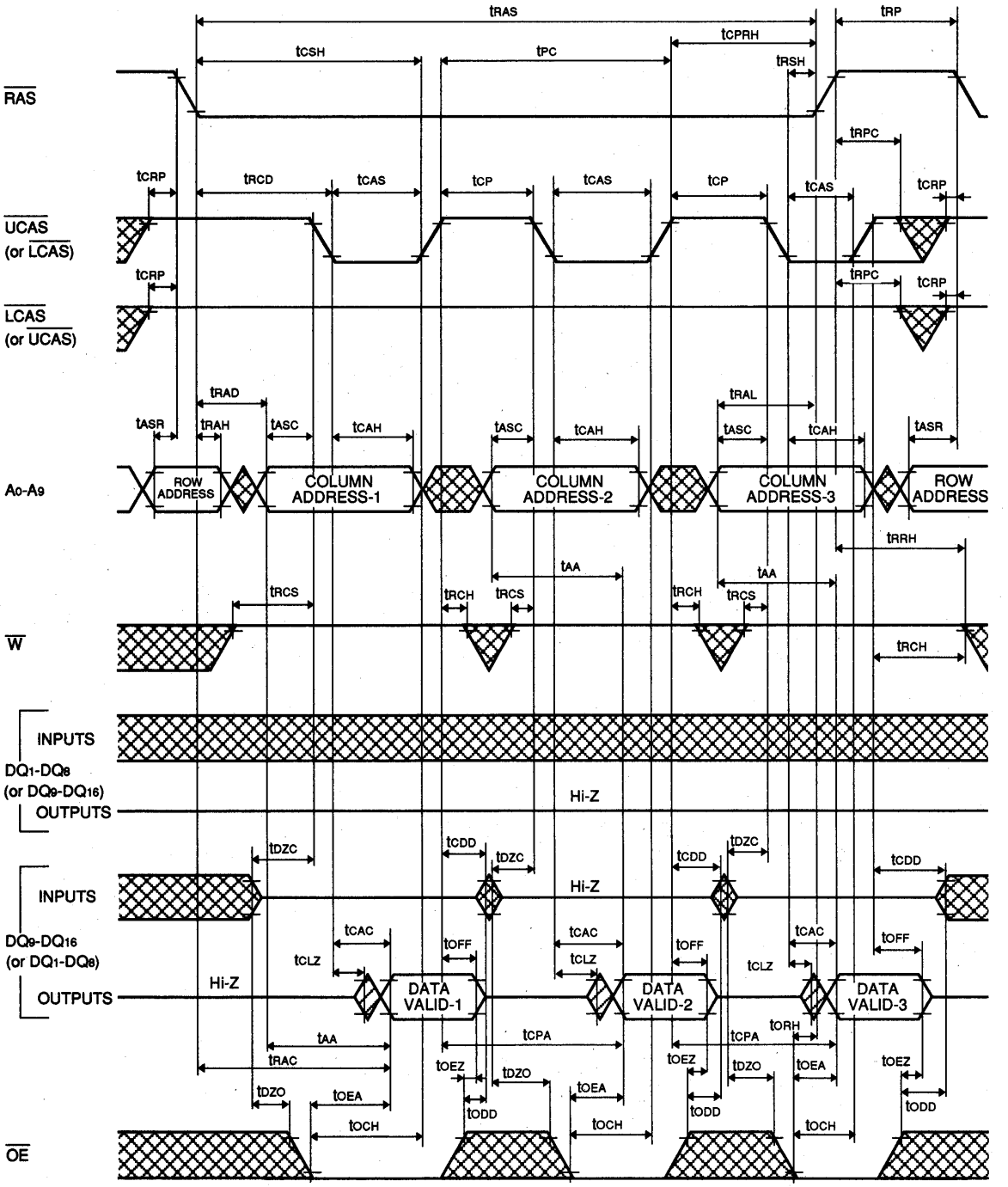
Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



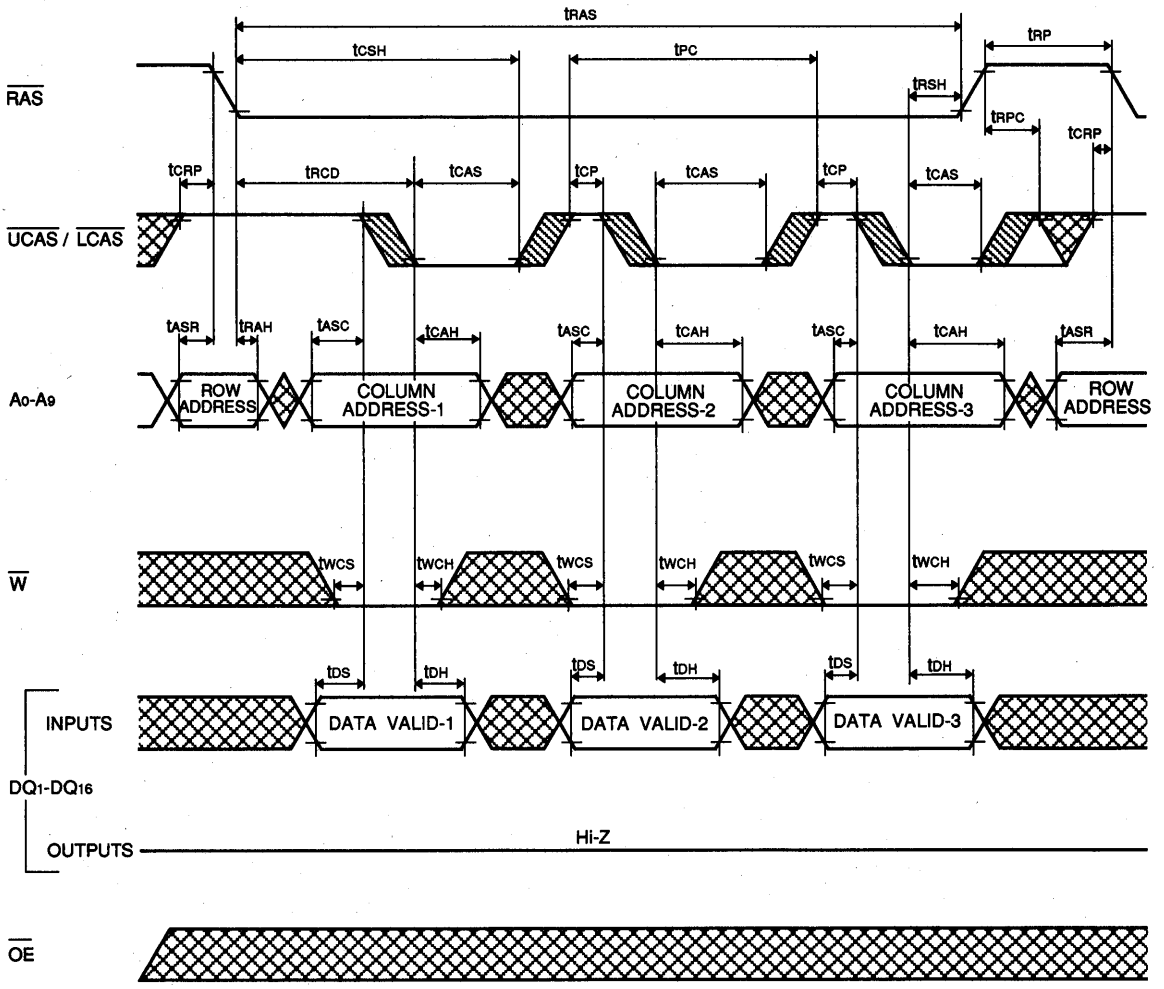
Fast Page Mode Read Cycle



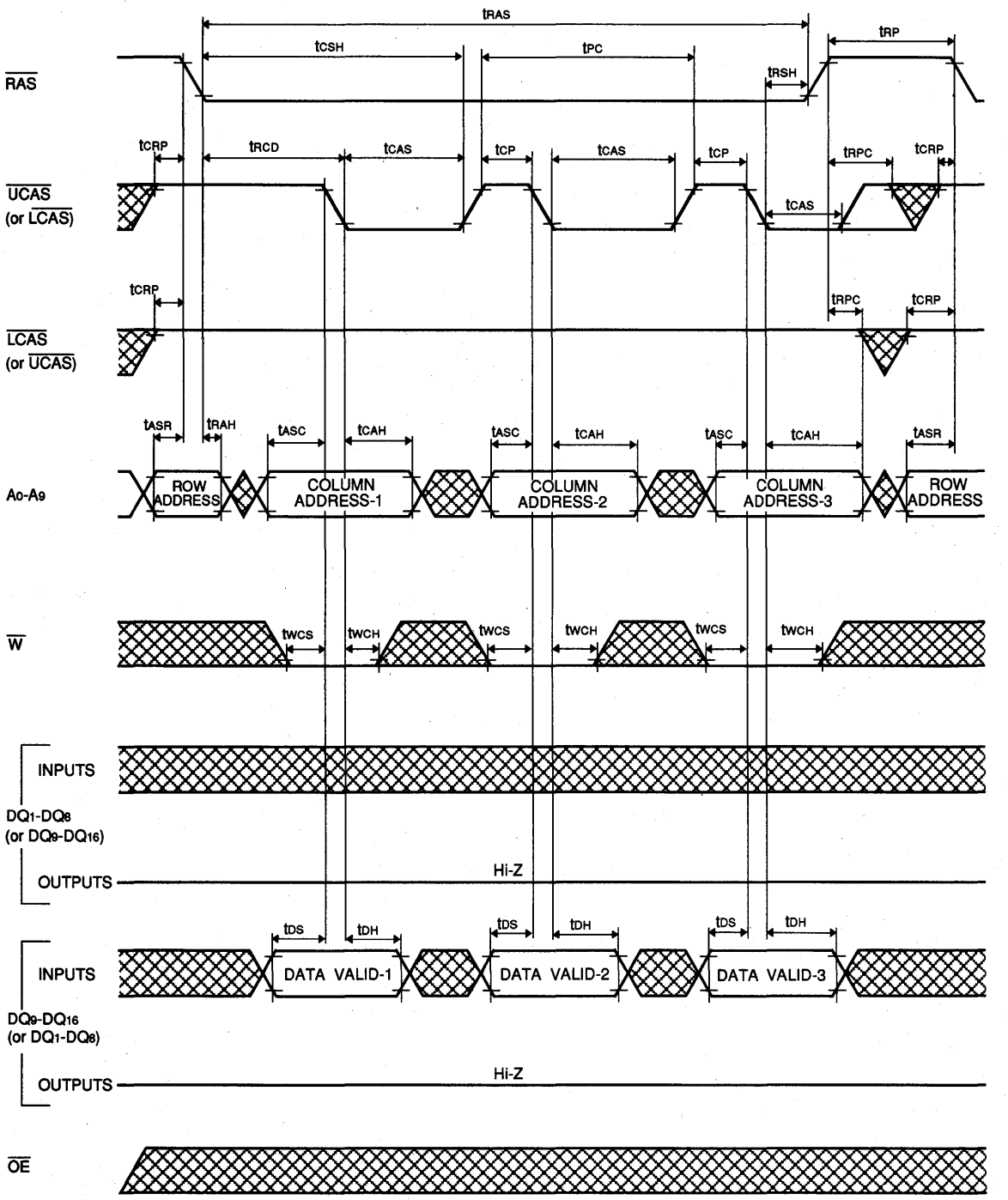
Upper/(Lower) Fast Page Mode Read Cycle



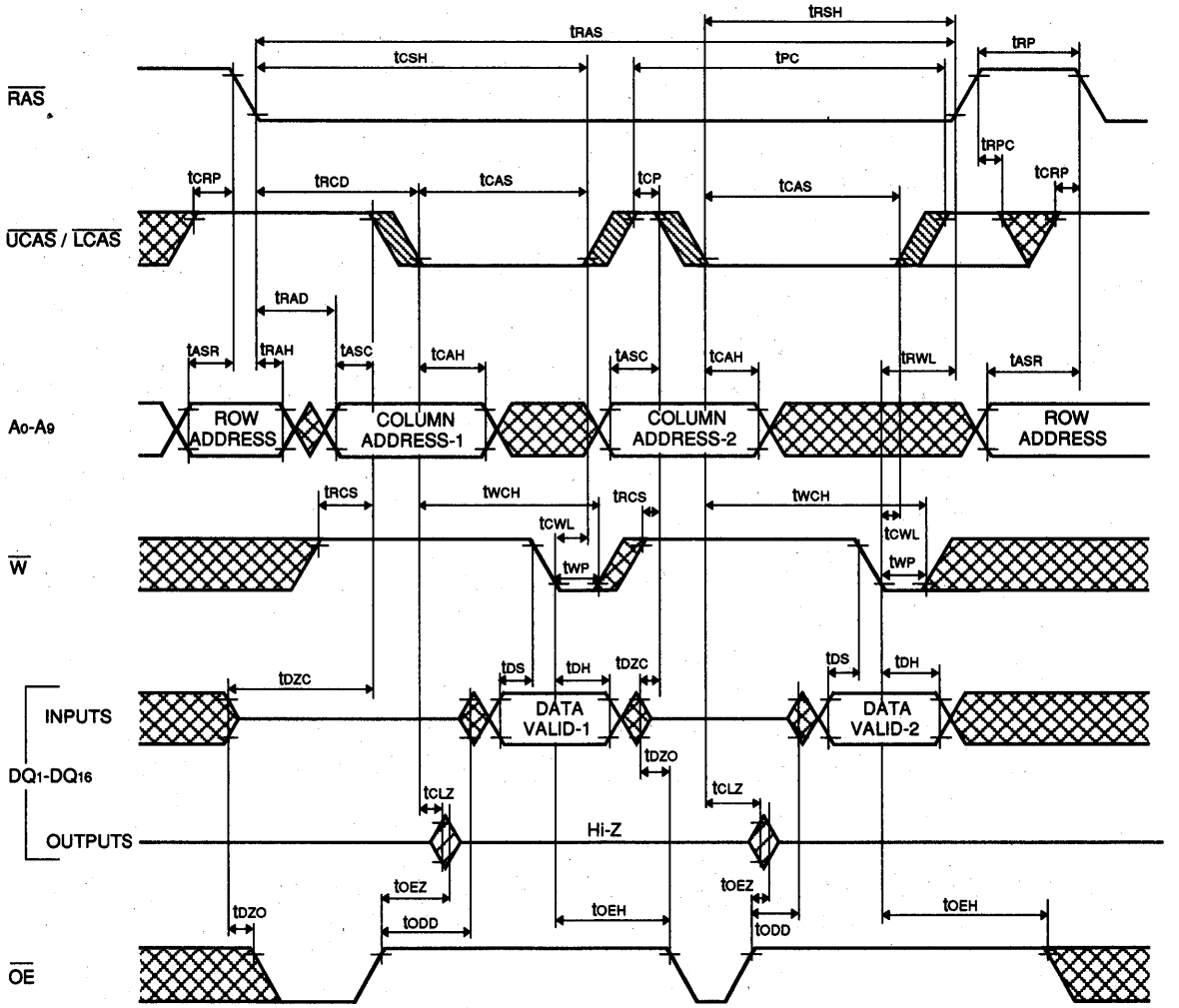
Fast Page Mode Write Cycle (Early Write)



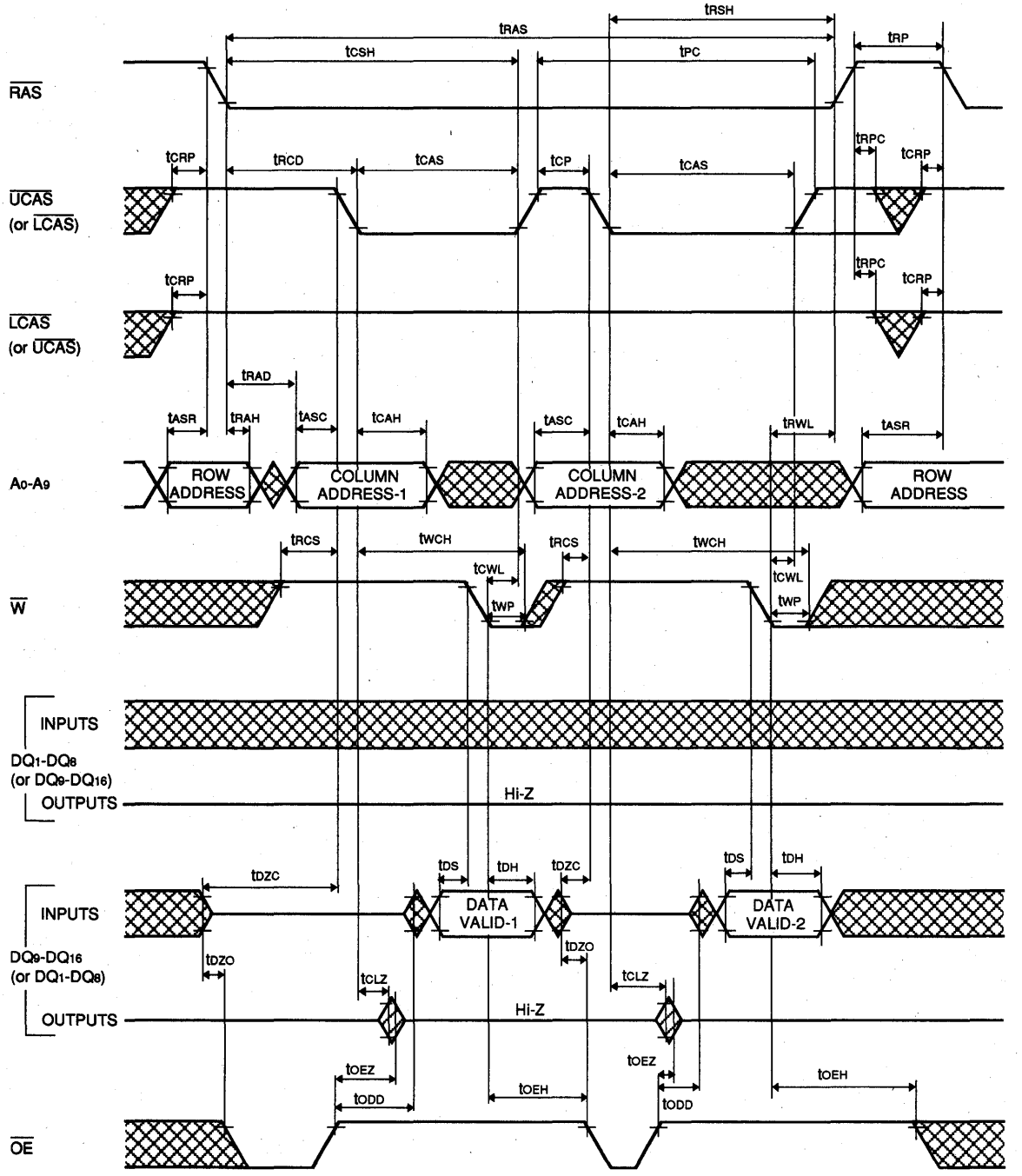
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



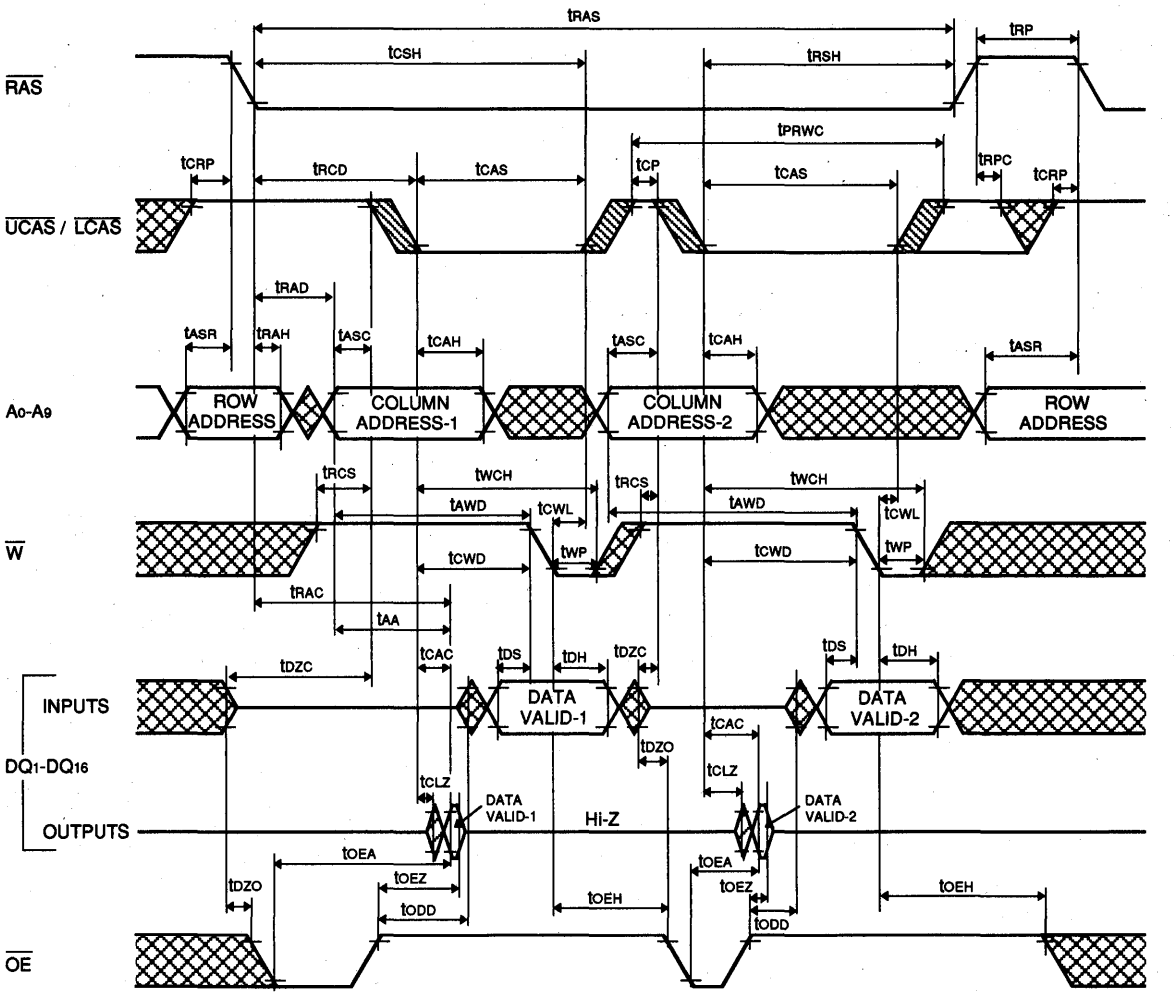
Fast Page Mode Write Cycle (Delayed Write)



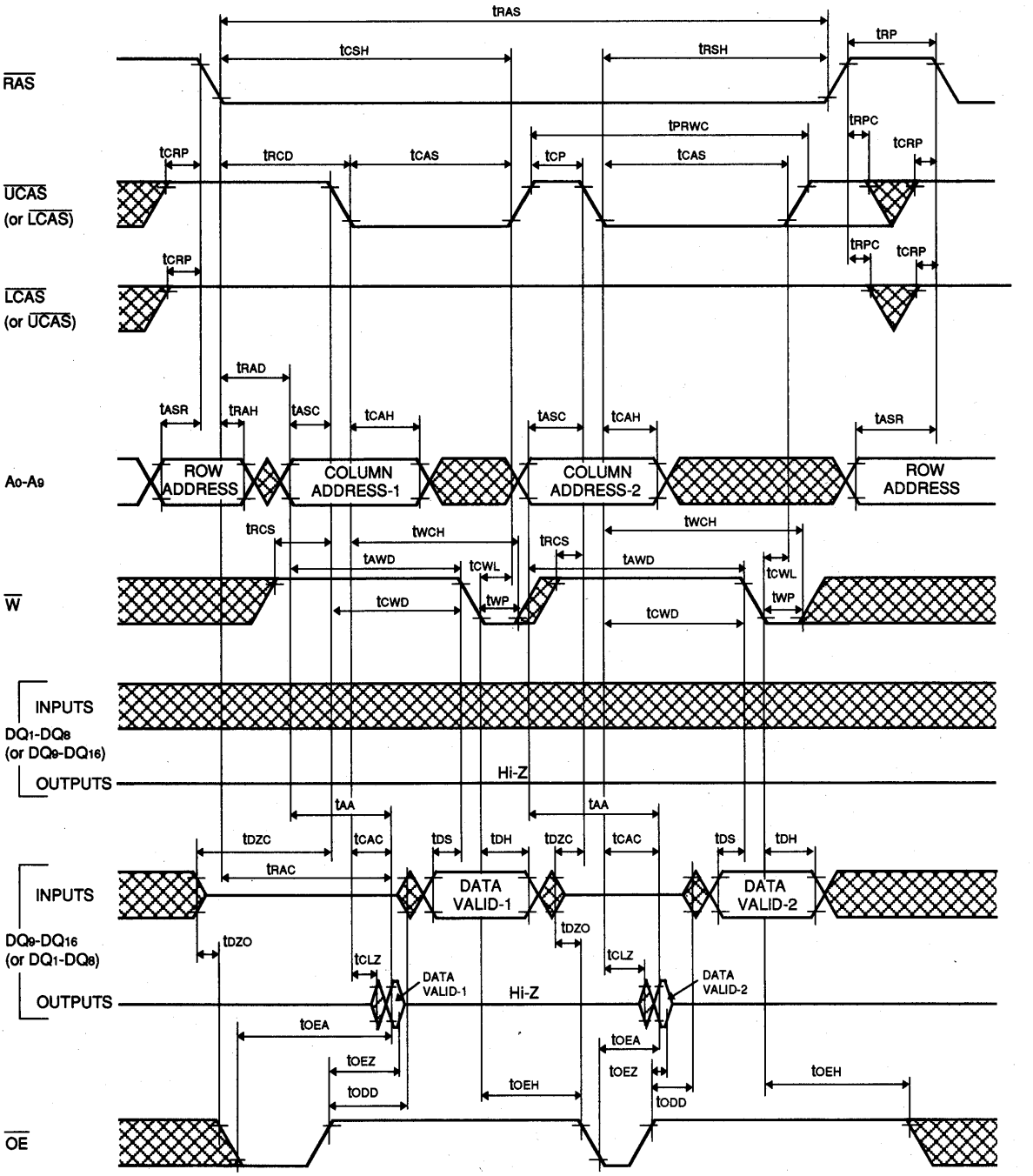
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S . The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8}	Supply current from Vcc Extended refresh cycle	M5M4V18160B -6S,-7S	$\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$ ≦ 0.2V or ≧ Vcc - 0.2V $\overline{OE}$ ≦ 0.2V or ≧ Vcc - 0.2V A_0~A_8 ≦ 0.2V or ≧ Vcc - 0.2V DQ = open t_{REF} = 128ms t_{RAS} = t_{RAS} min~1 μs			300	μA
I_{CC9} (AV)	Average supply current from Vcc Self - Refresh cycle	M5M4V18160B -6S,-7S	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			200	μA

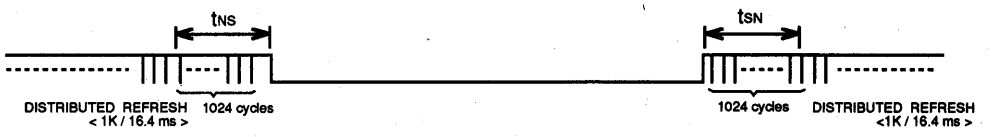
TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M4V18160B-6S		M5M4V18160B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

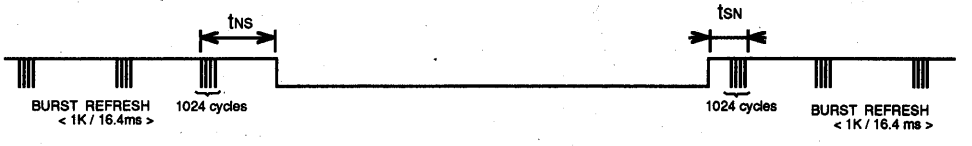
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} ≦ 16.4 ms and t_{SN} ≦ 16.4 ms.

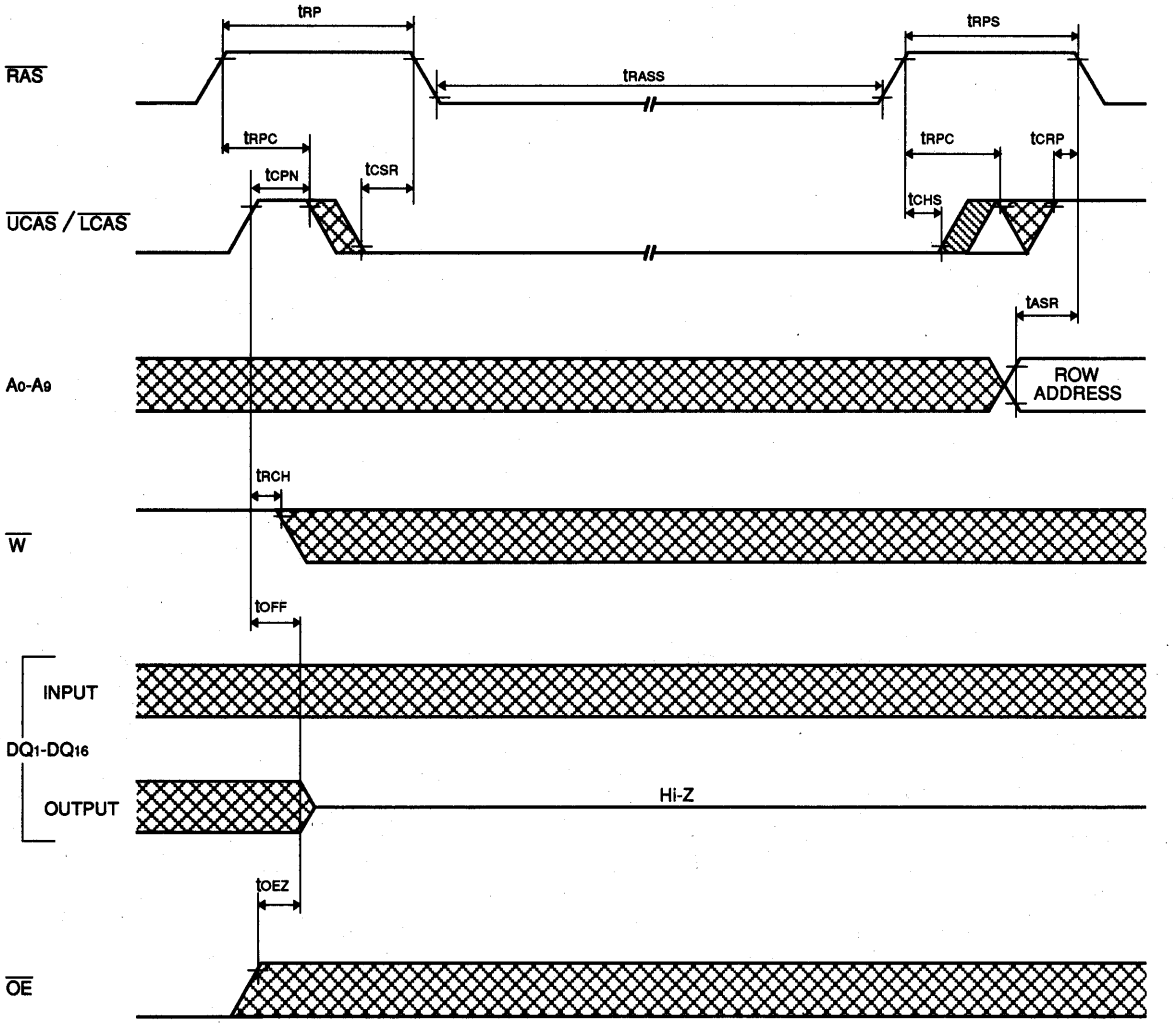


(2) In case of burst refresh

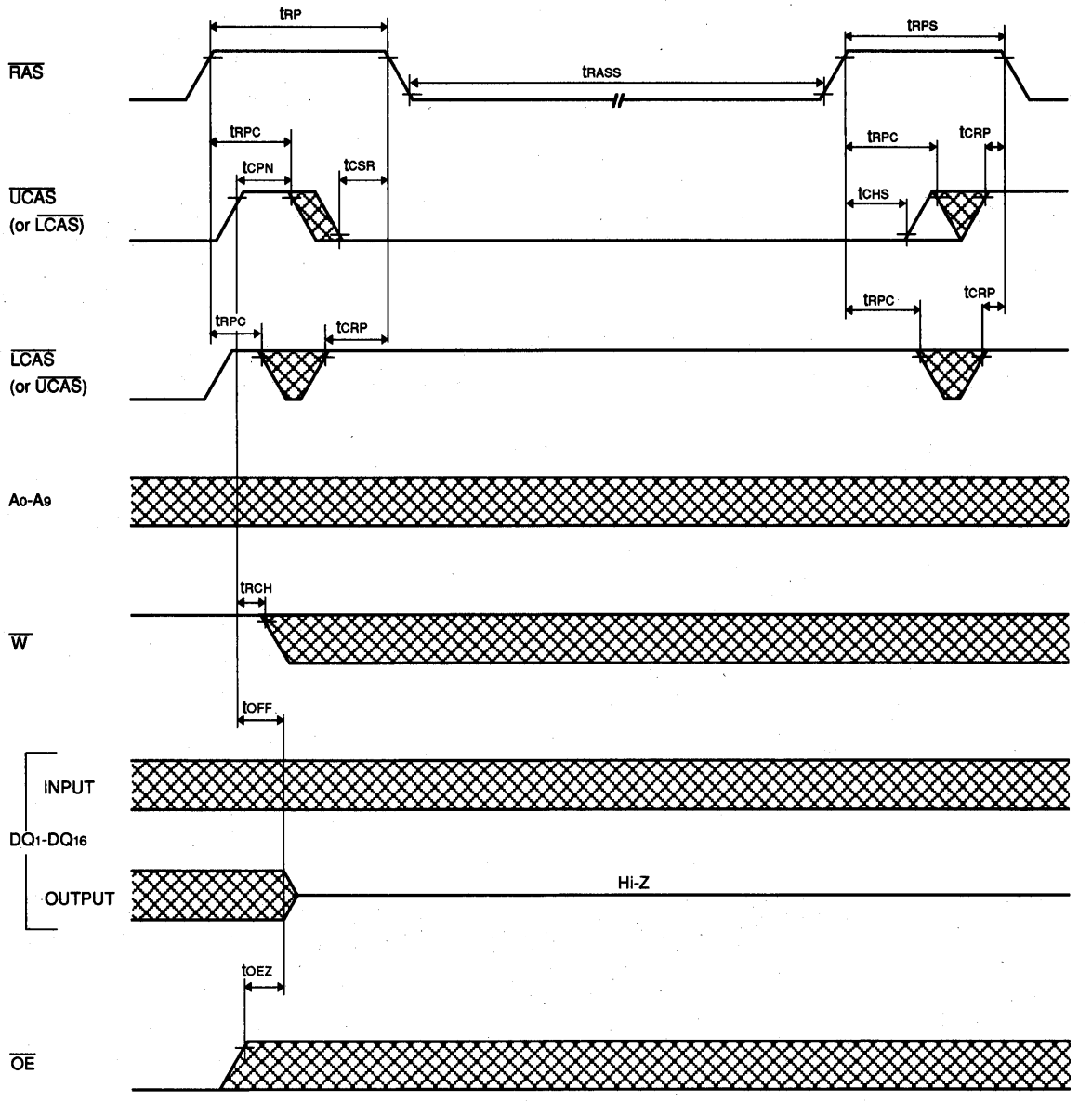
The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} + t_{SN} ≦ 16.4 ms.



Self Refresh Cycle



Upper/(Lower) Self Refresh Cycle*



M5M4V16165BTP-6,-7,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

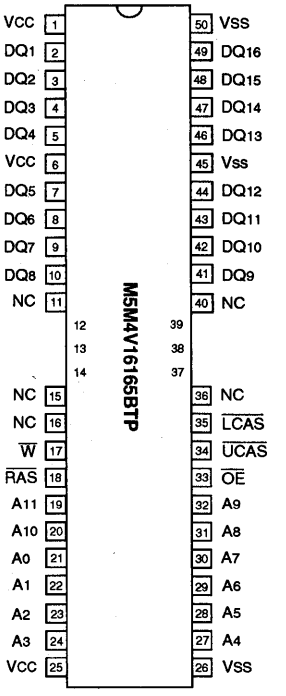
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16165BTP-6,-6S	60	15	30	15	110	285
M5M4V16165BTP-7,-7S	70	20	35	20	130	255

- Standard 50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V16165BTP-6,-6S ---------- 345.0mW (Max)
  M5M4V16165BTP-7,-7S ---------- 310.0mW (Max)
- Hyper-page mode, Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0~A_{11})

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 50P3W-L (400mil TSOP Normal Bend)

NC : NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

FUNCTION

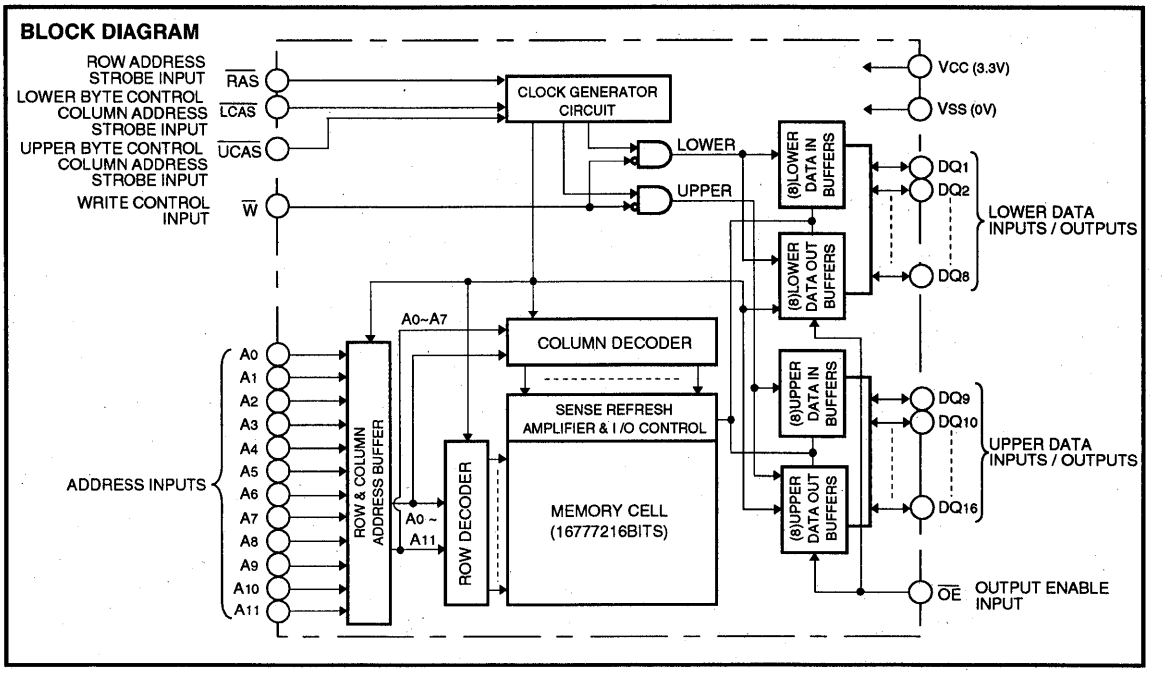
The M5M4V16165BTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦V_{CC}	-10		10	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}+0.3V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V16165B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			95	mA
		M5M4V16165B-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V16165B-6,-7	$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.5	
		M5M4V16165B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.15	
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 3,5)	M5M4V16165B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			95	mA
		M5M4V16165B-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M4V16165B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			130	mA
		M5M4V16165B-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16165B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			95	mA
		M5M4V16165B-7,-7S				85	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=00~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=00~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high	(Note 12)	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10uA|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits				Unit
			M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		64		64	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	10		13		ns
t_{WP}	Write pulse width	10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 23)	133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width	89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 24)	32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 24)	77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 24)	47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter		Limits				Unit
			M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
			Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time		25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 26)	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 27)	10	18	13	18	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 24)	52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)		7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read		32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read		62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read		72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read		15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

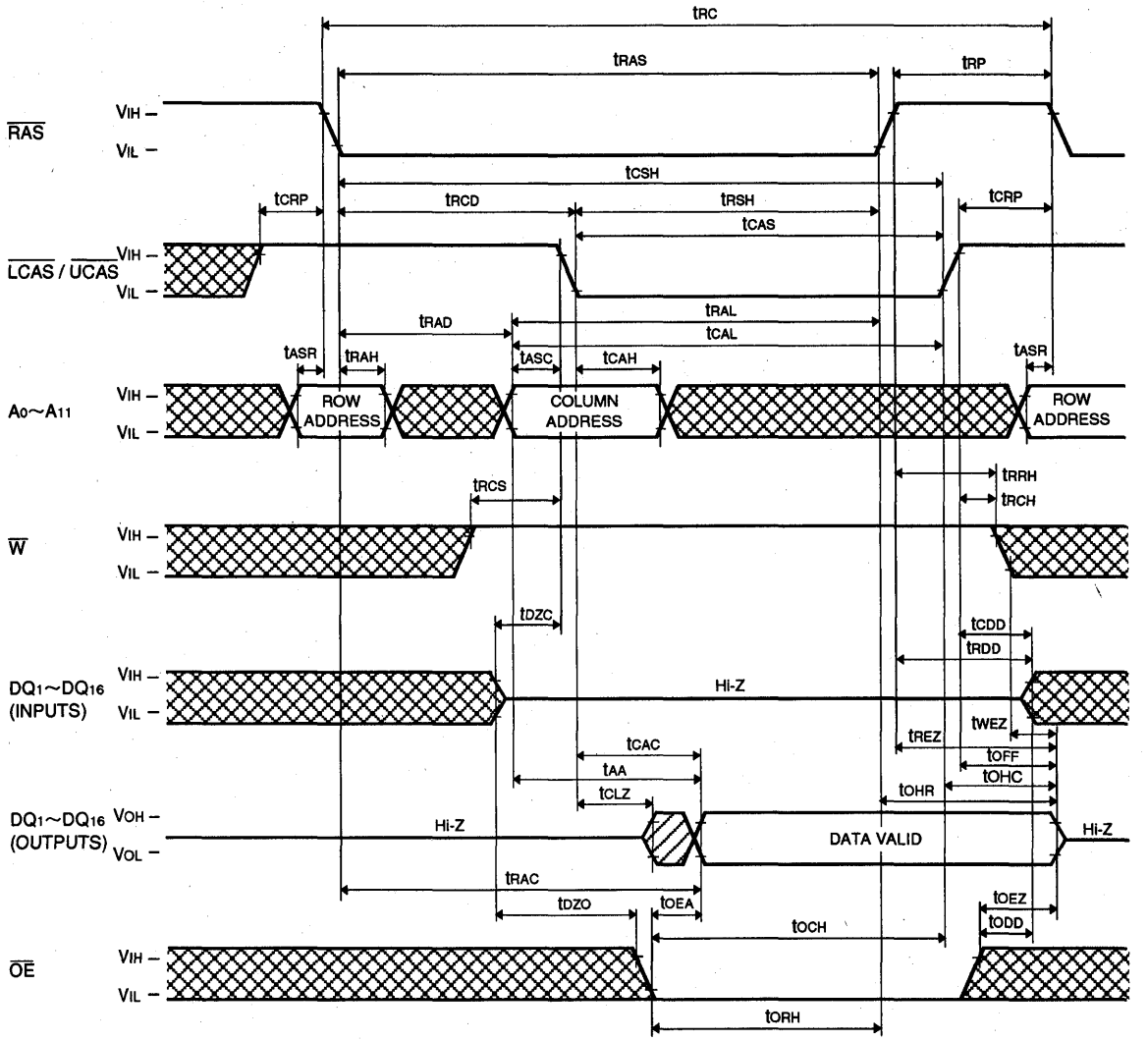
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M4V16165B-6,-6S		M5M4V16165B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 29)

Read Cycle

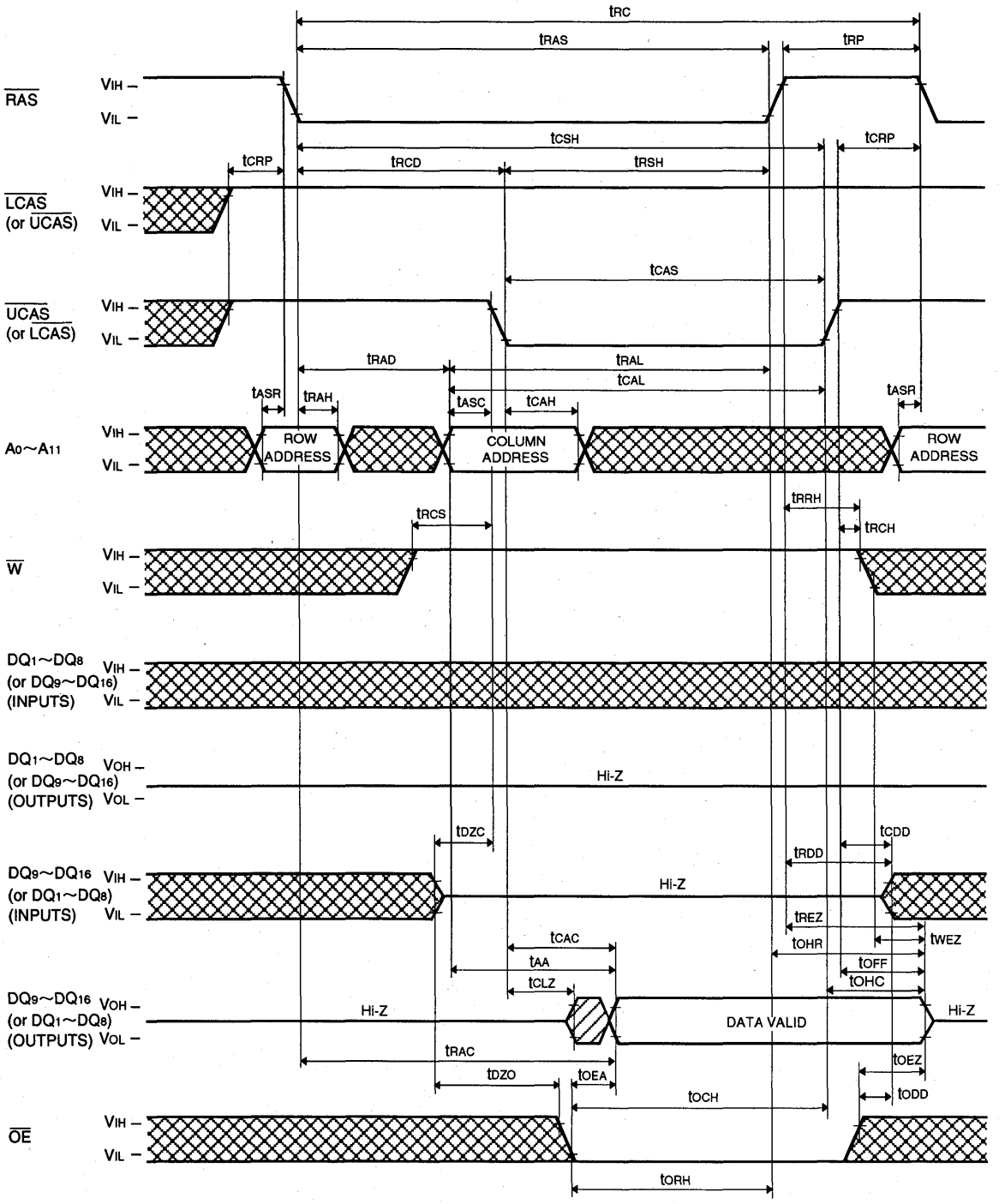


Note 29

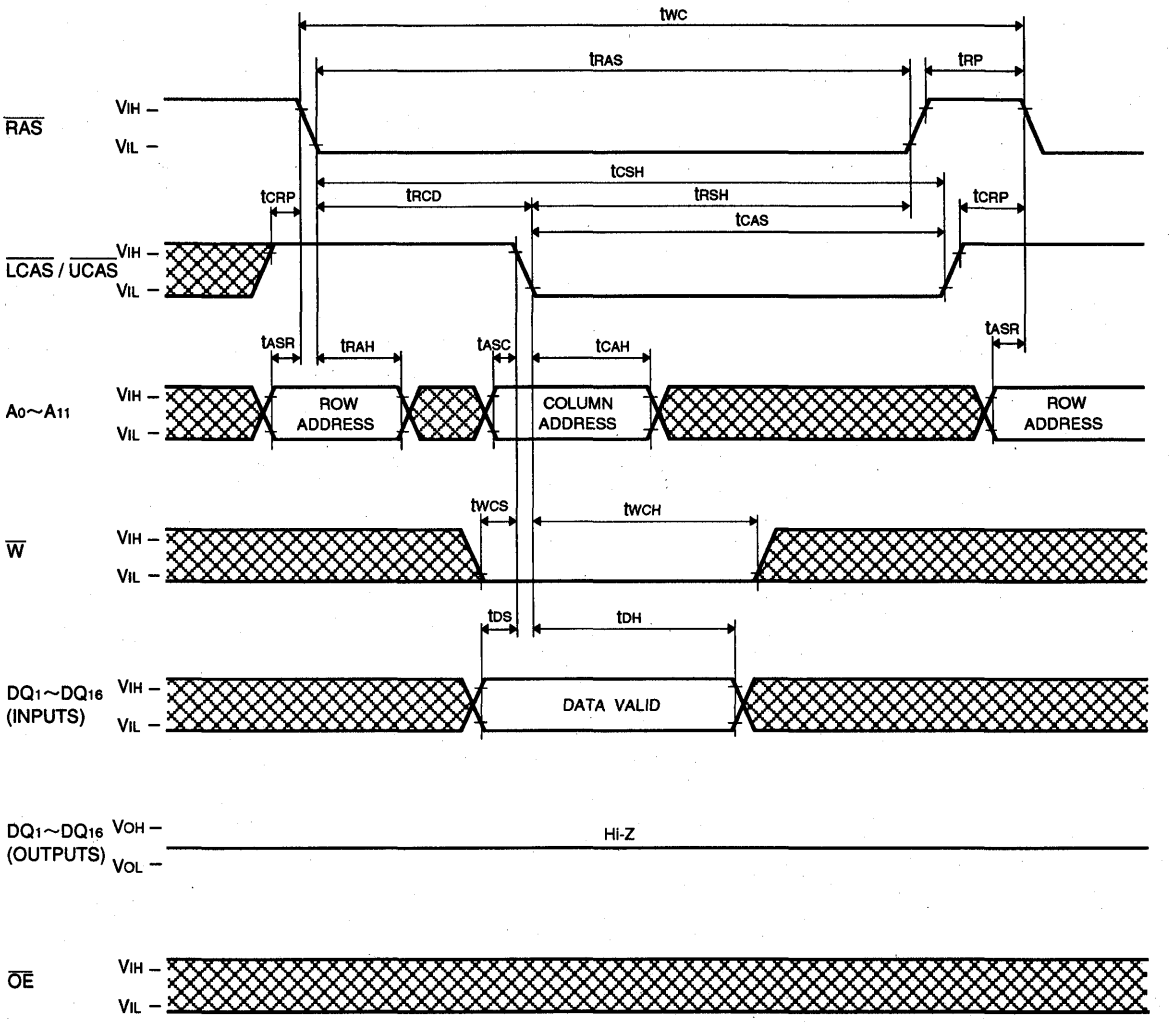
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

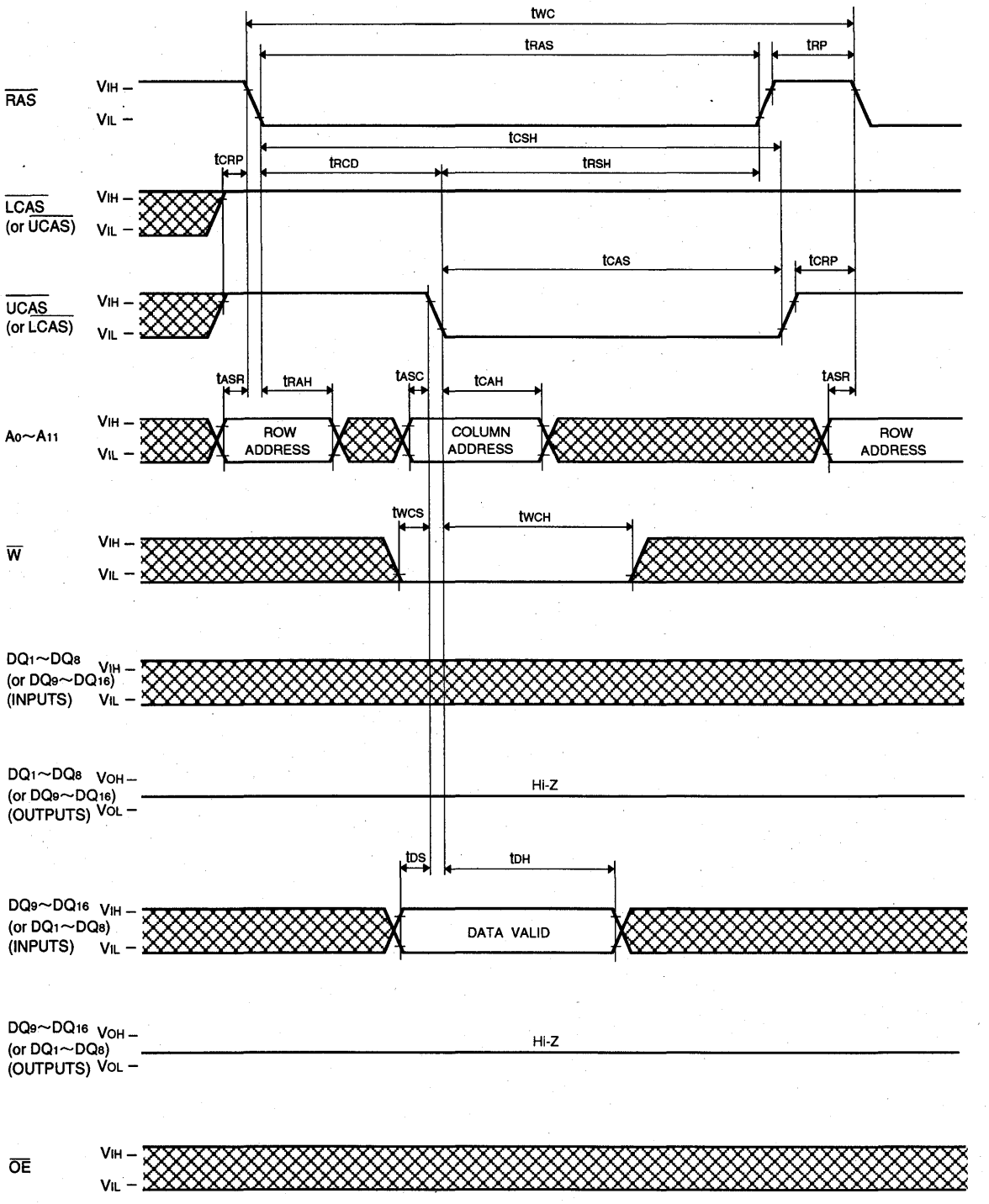
Byte Read Cycle



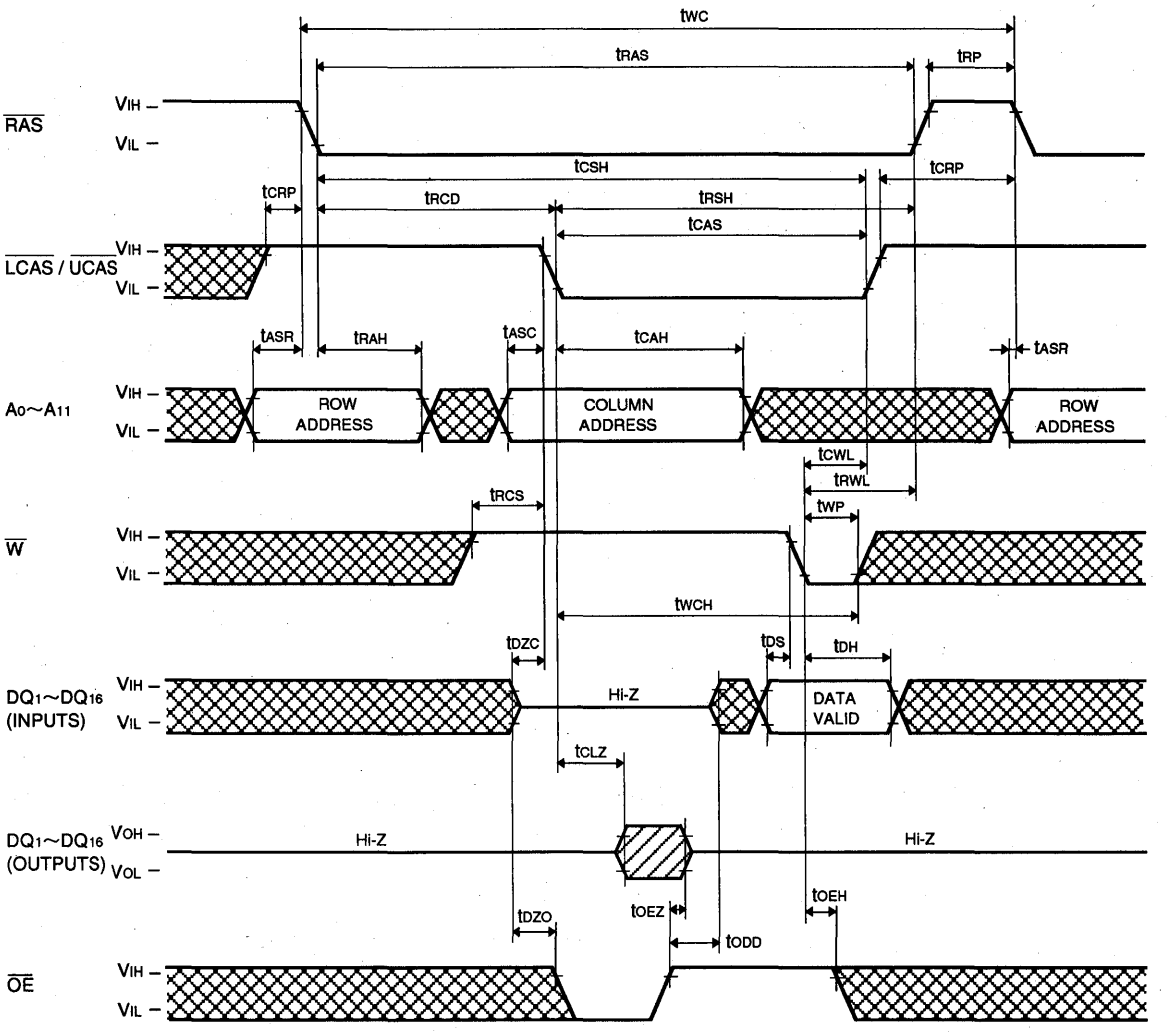
Early Write Cycle



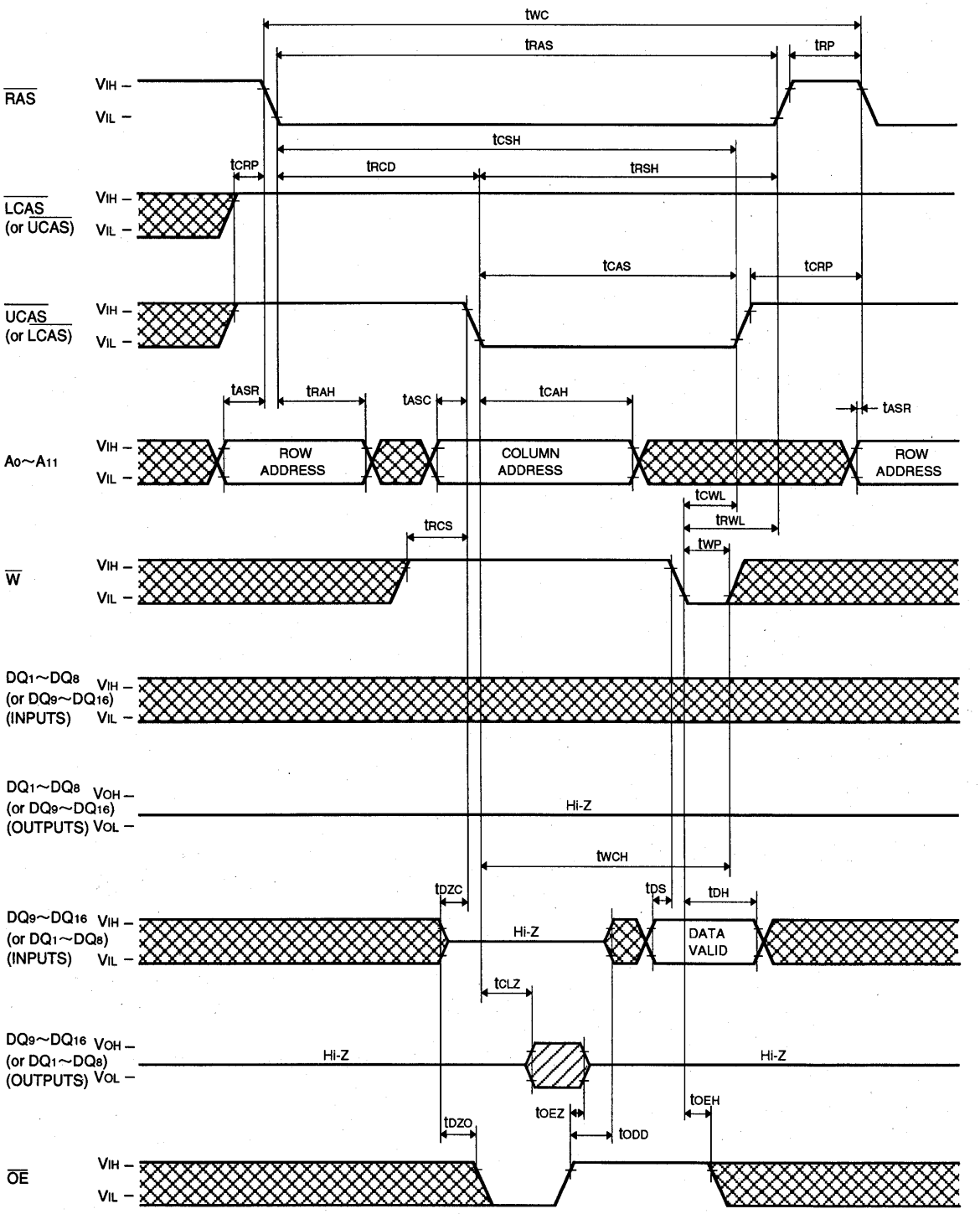
Byte Early Write Cycle



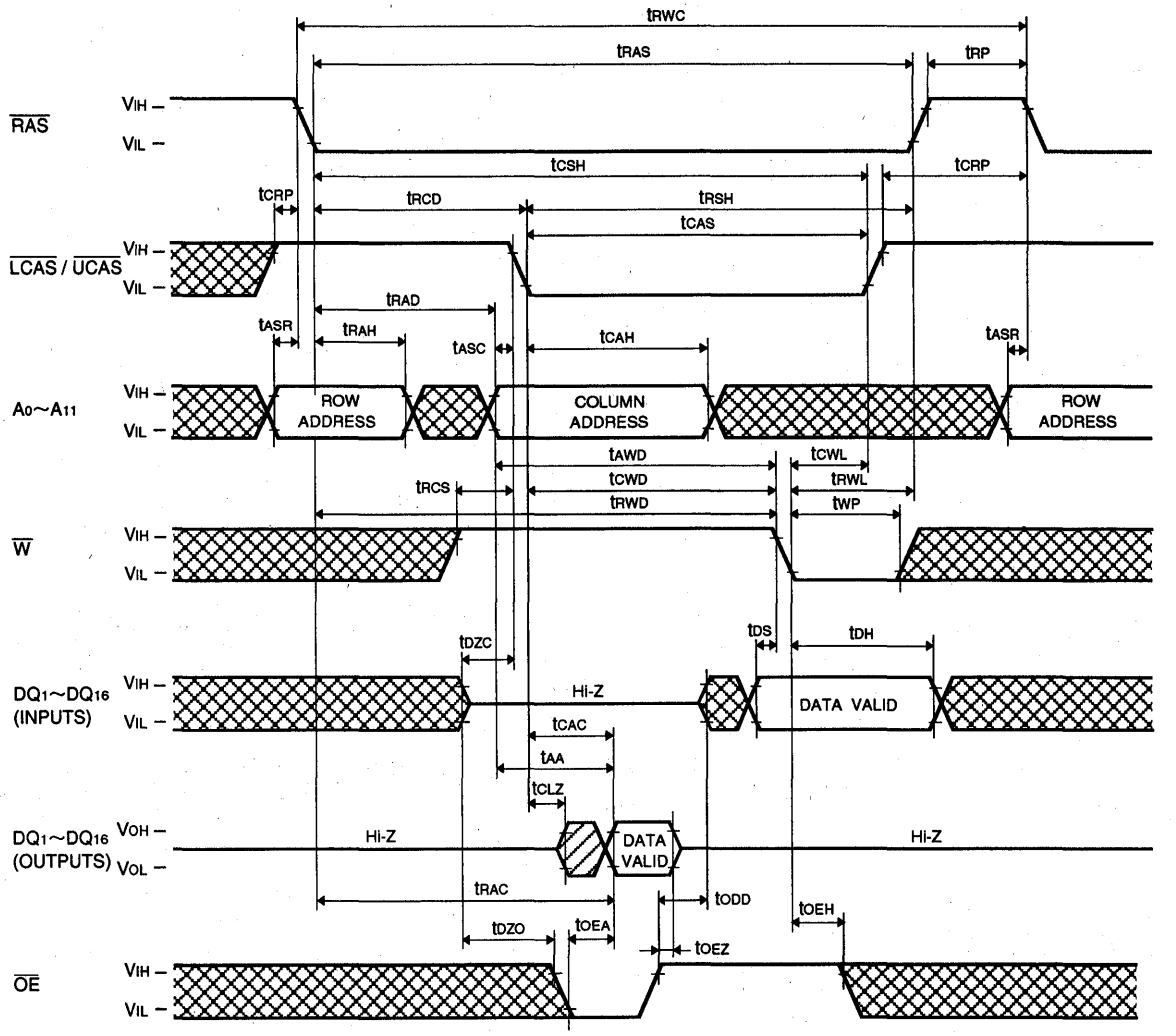
Delayed Write Cycle



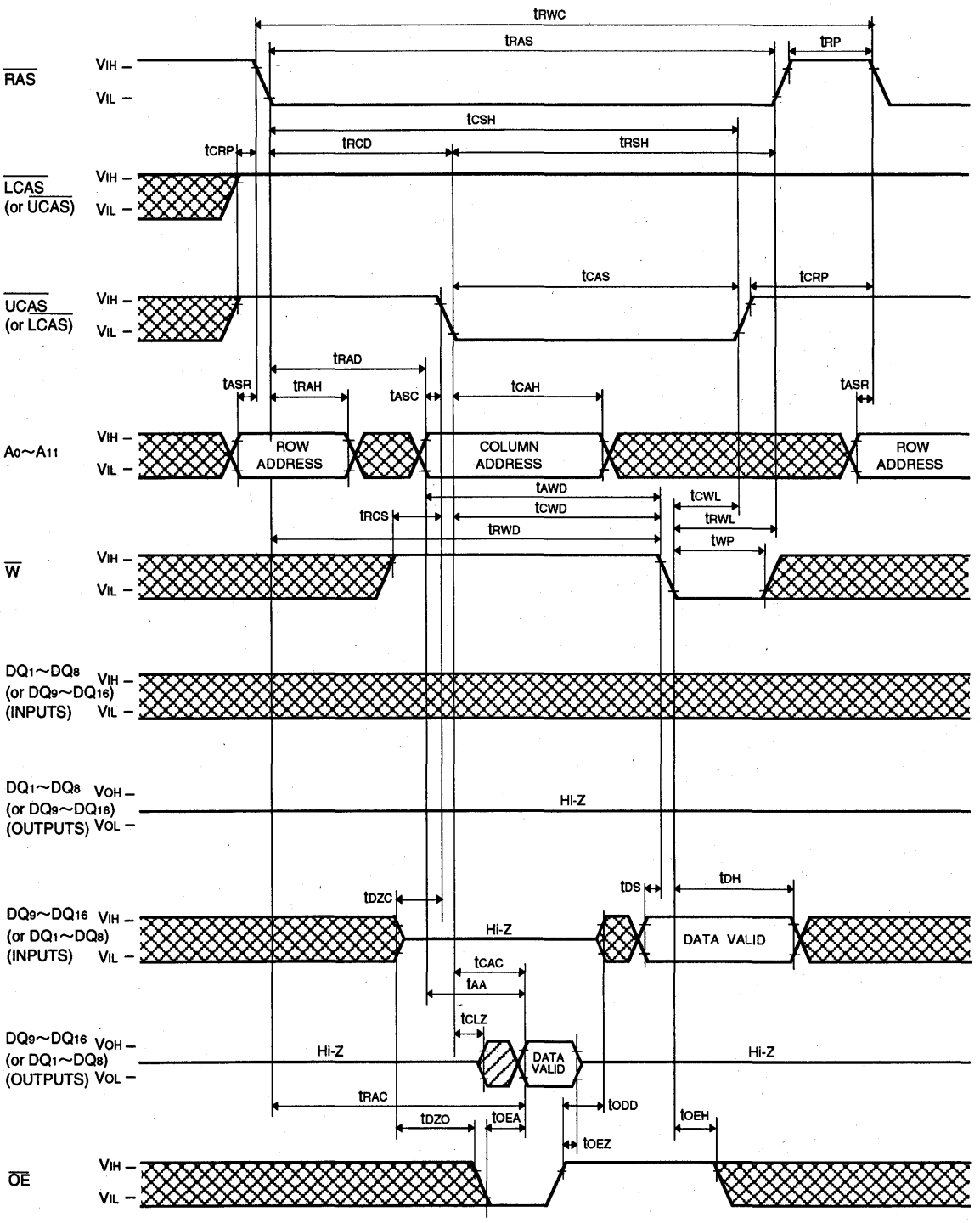
Byte Delayed Write Cycle



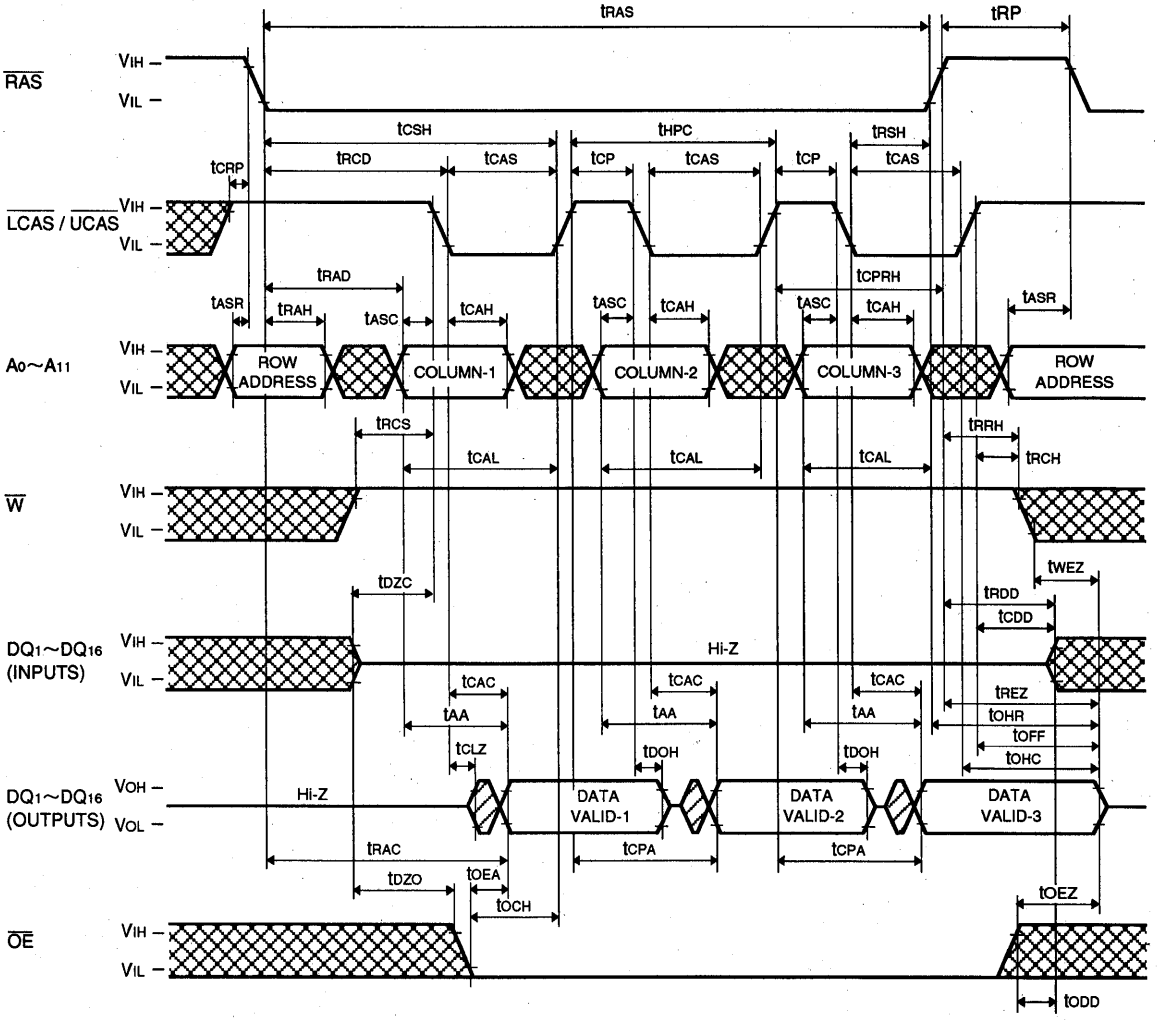
Read-Write, Read-Modify-Write Cycle



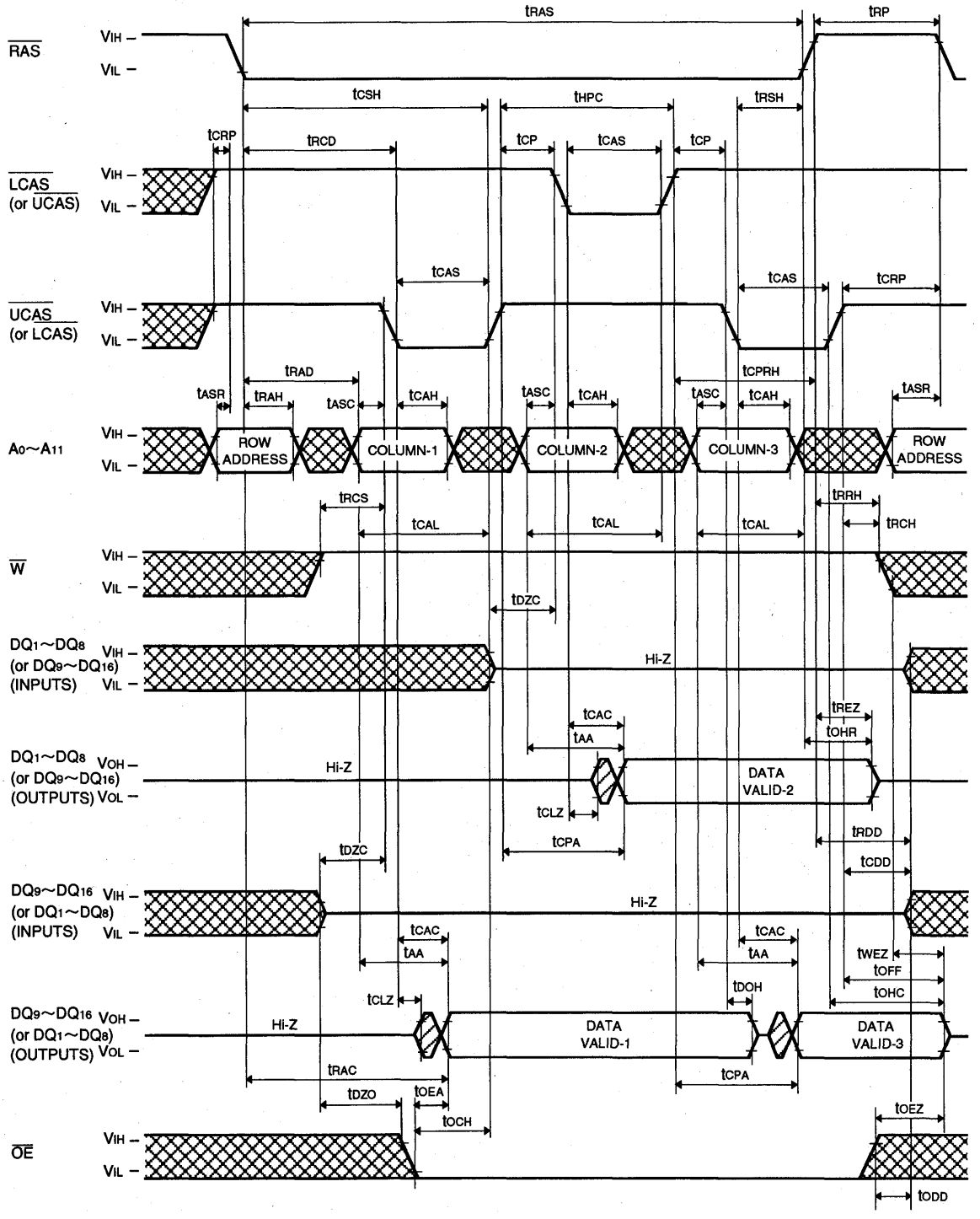
Byte Read-Write, Read-Modify-Write Cycle



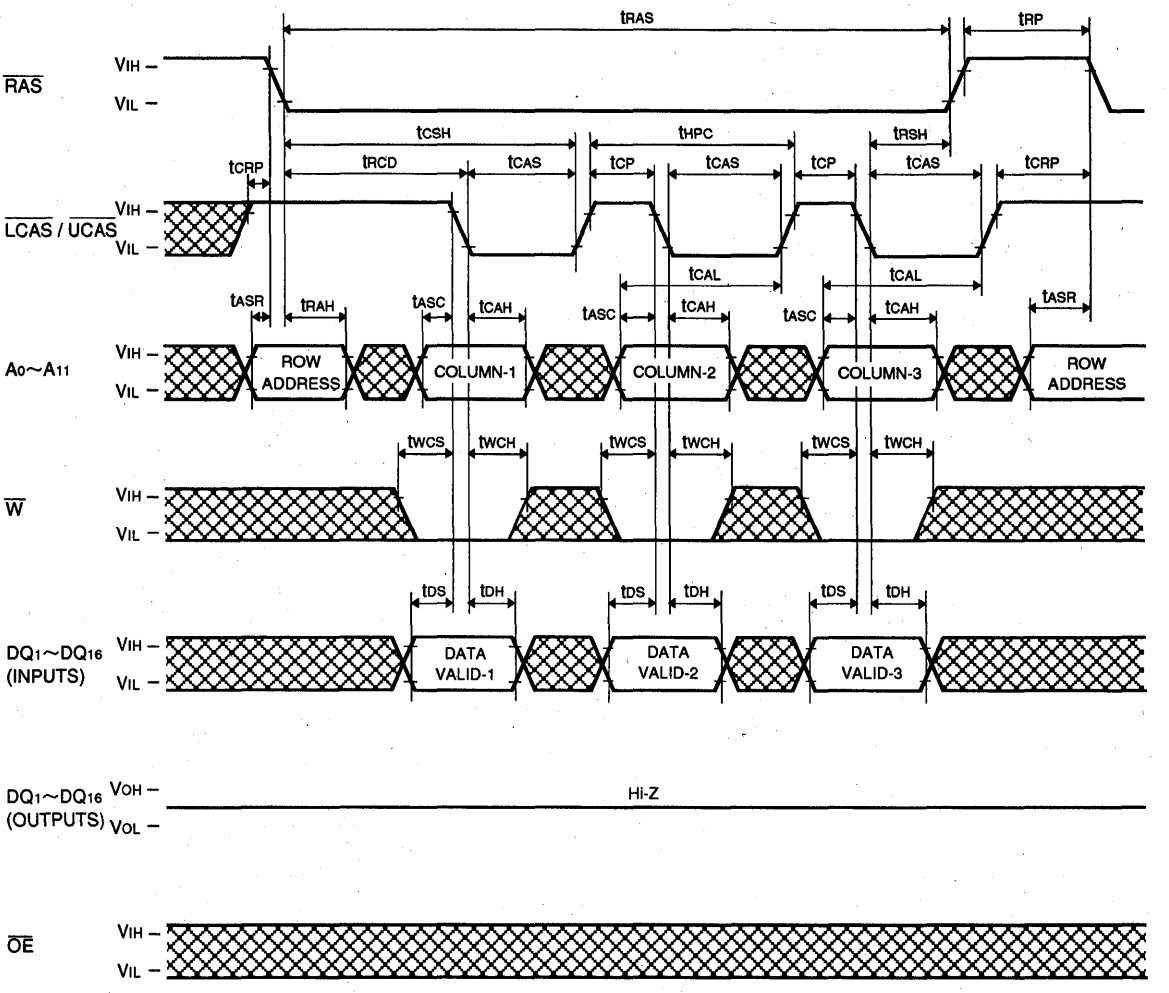
Hyper Page Mode Read Cycle



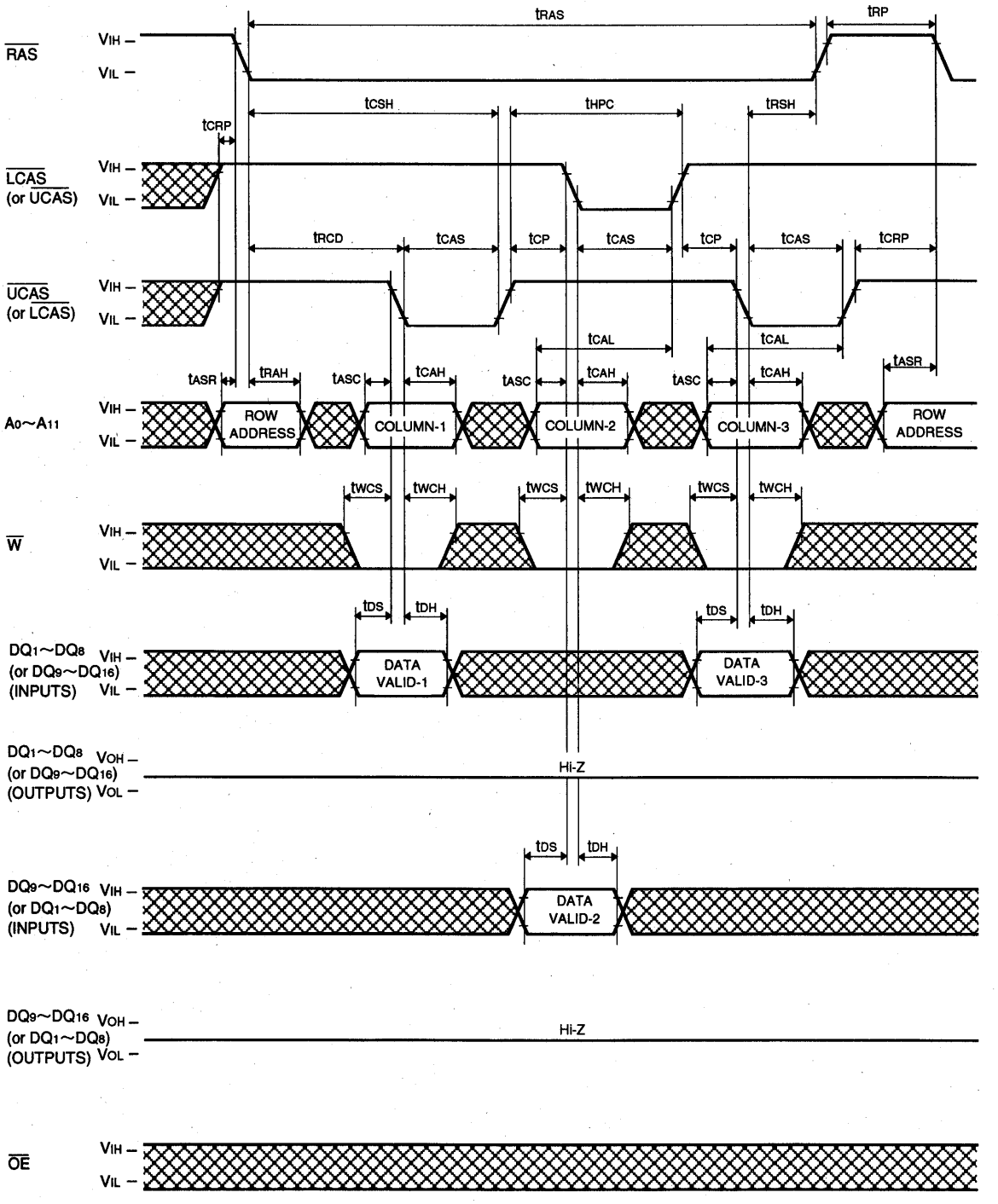
Hyper Page Mode Byte Read Cycle



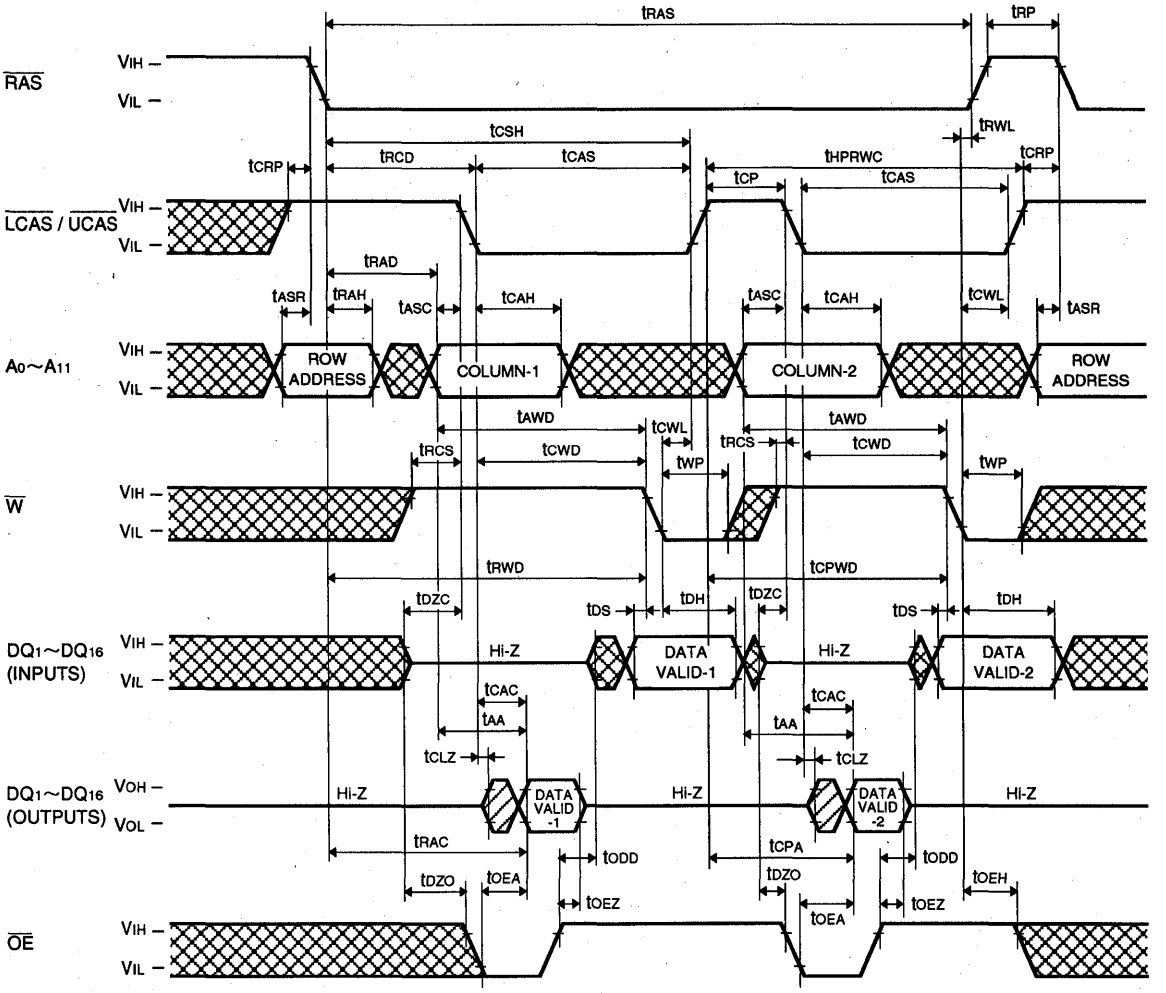
Hyper Page Mode Early Write Cycle



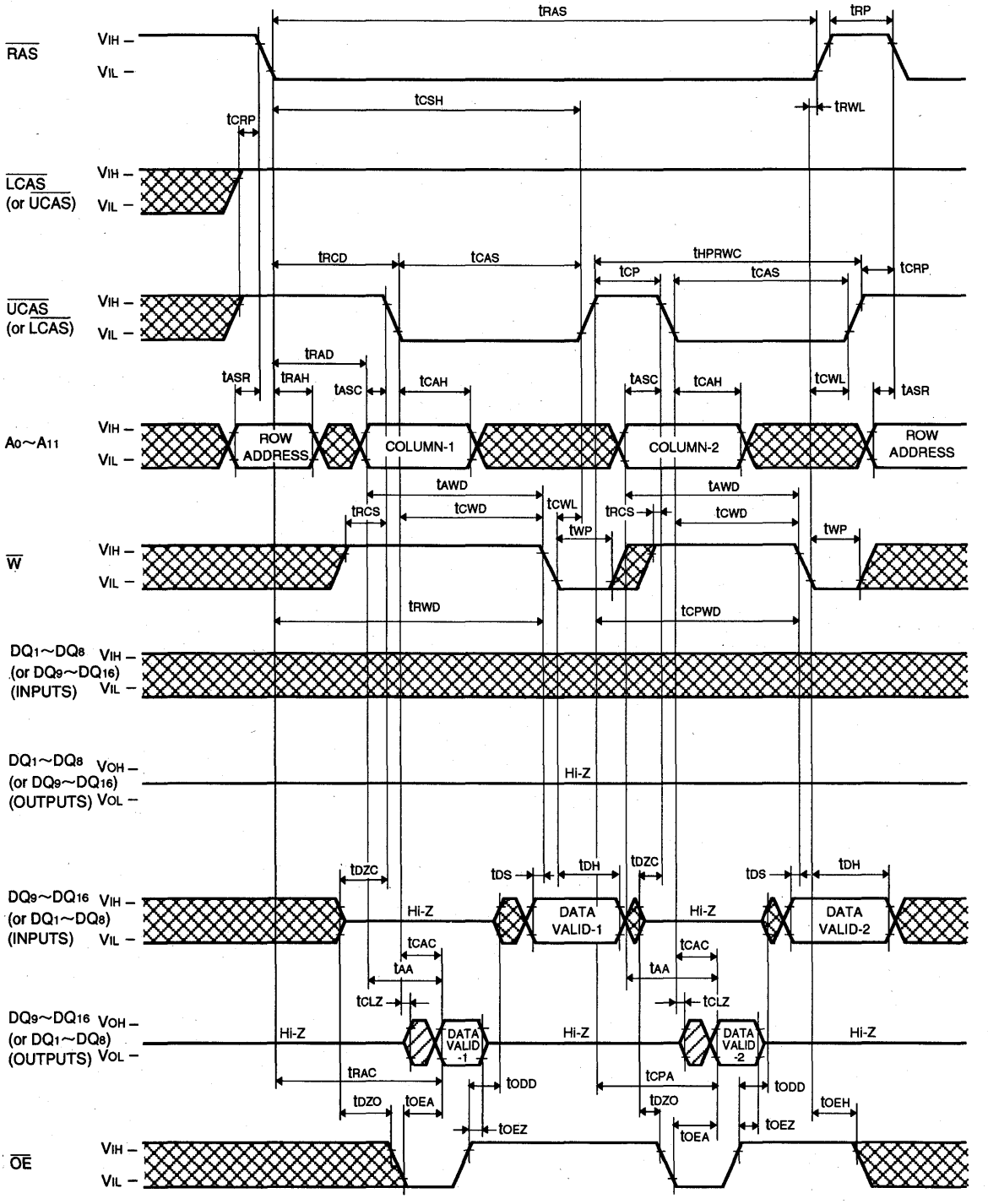
Hyper Page Mode Byte Early Write Cycle



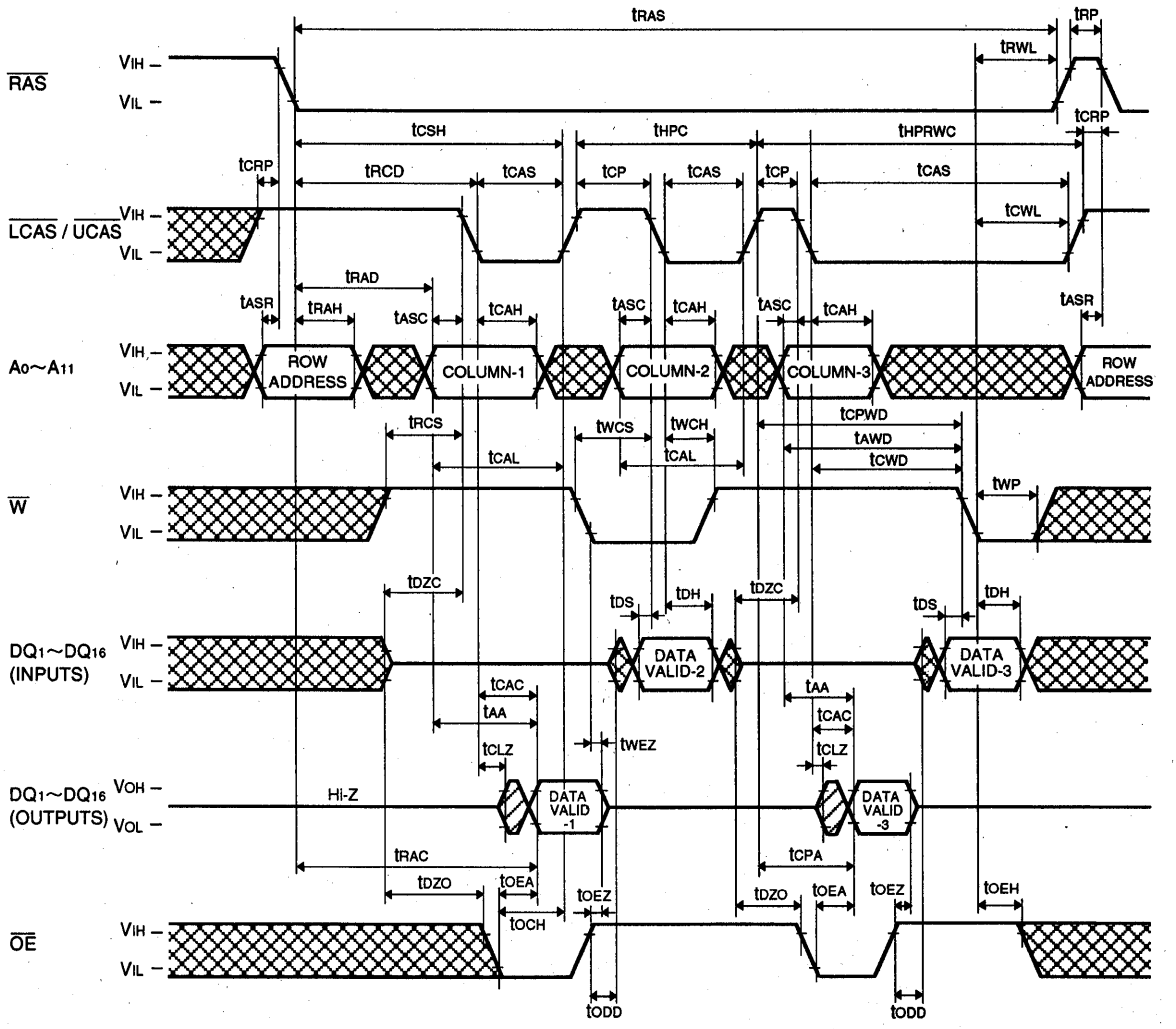
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



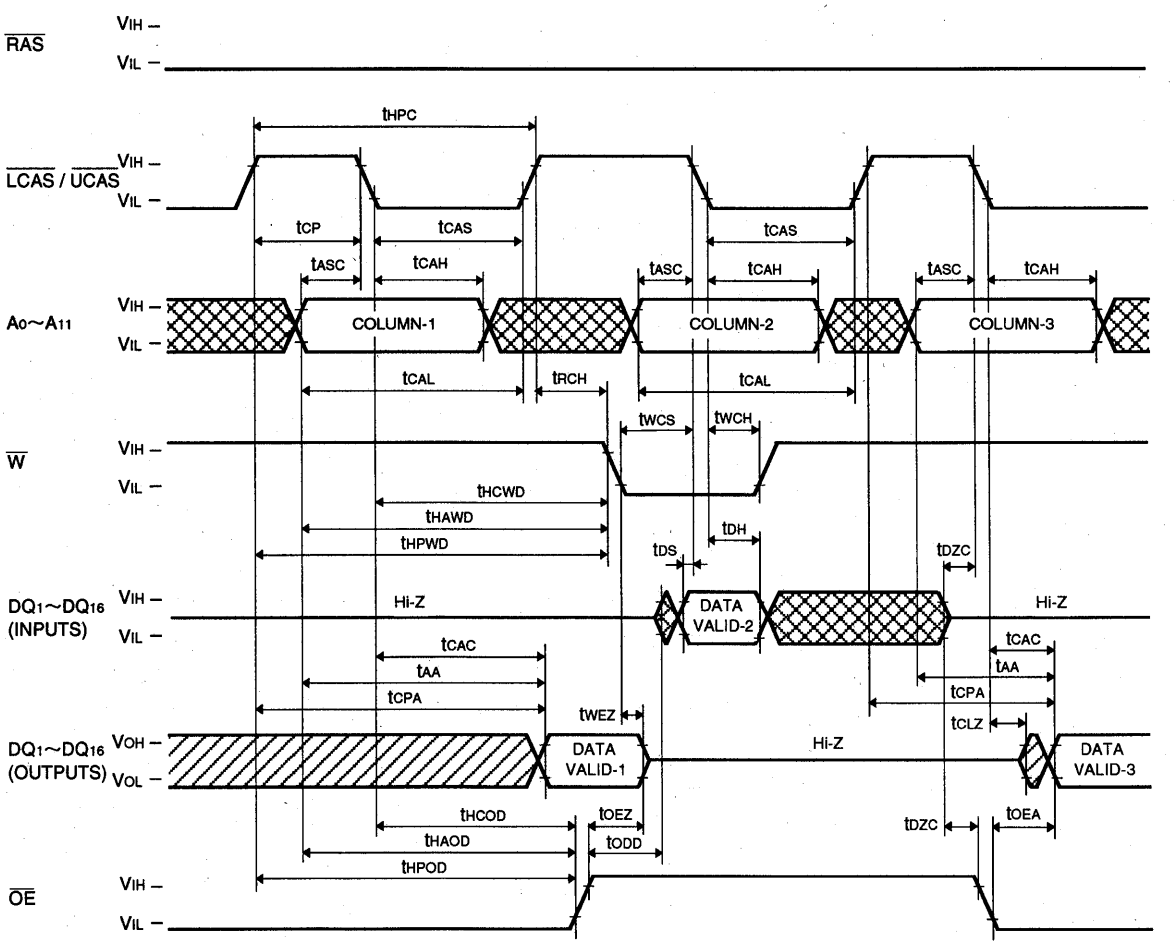
Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



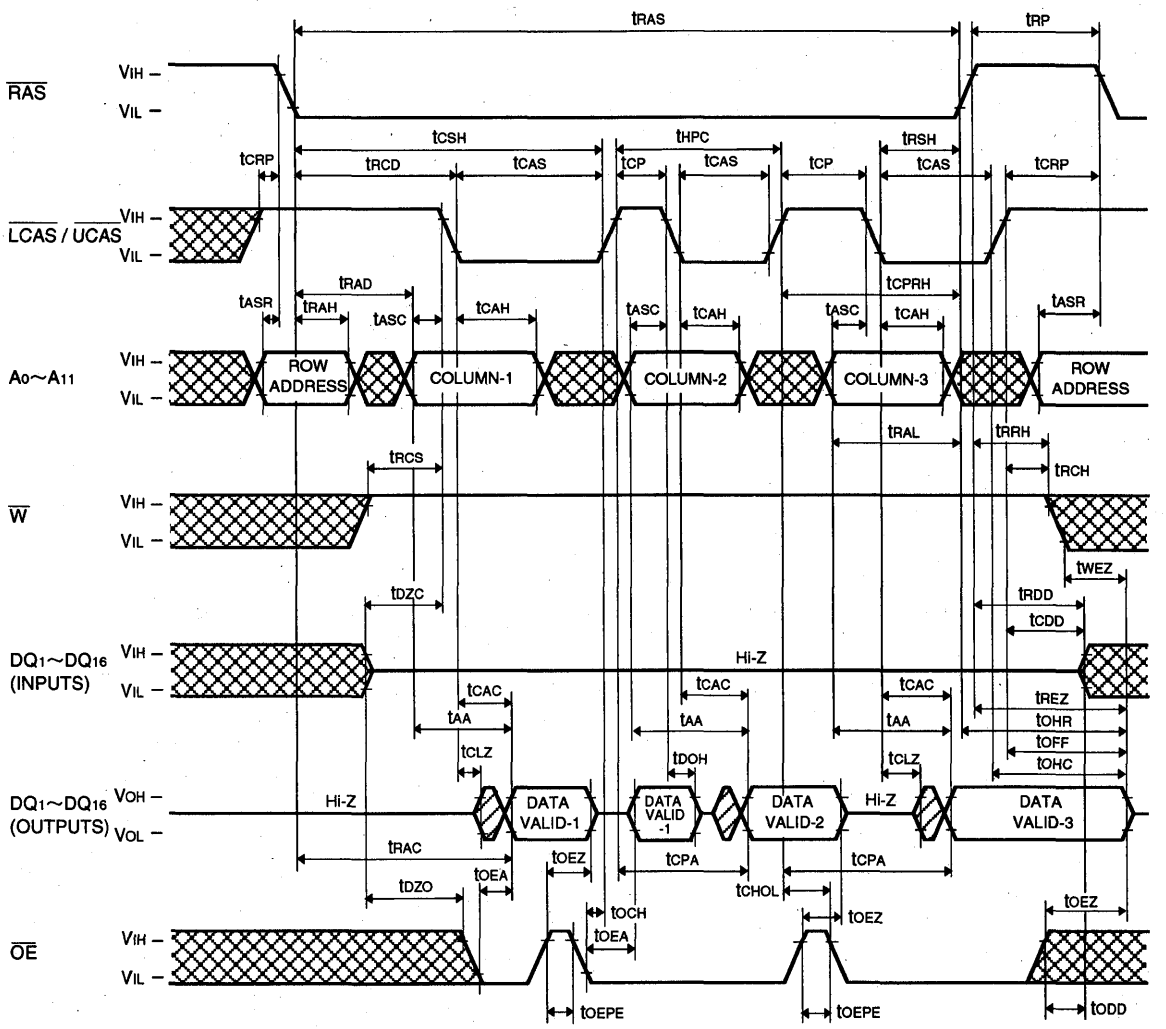
Hyper Page Mode Mix Cycle (1)



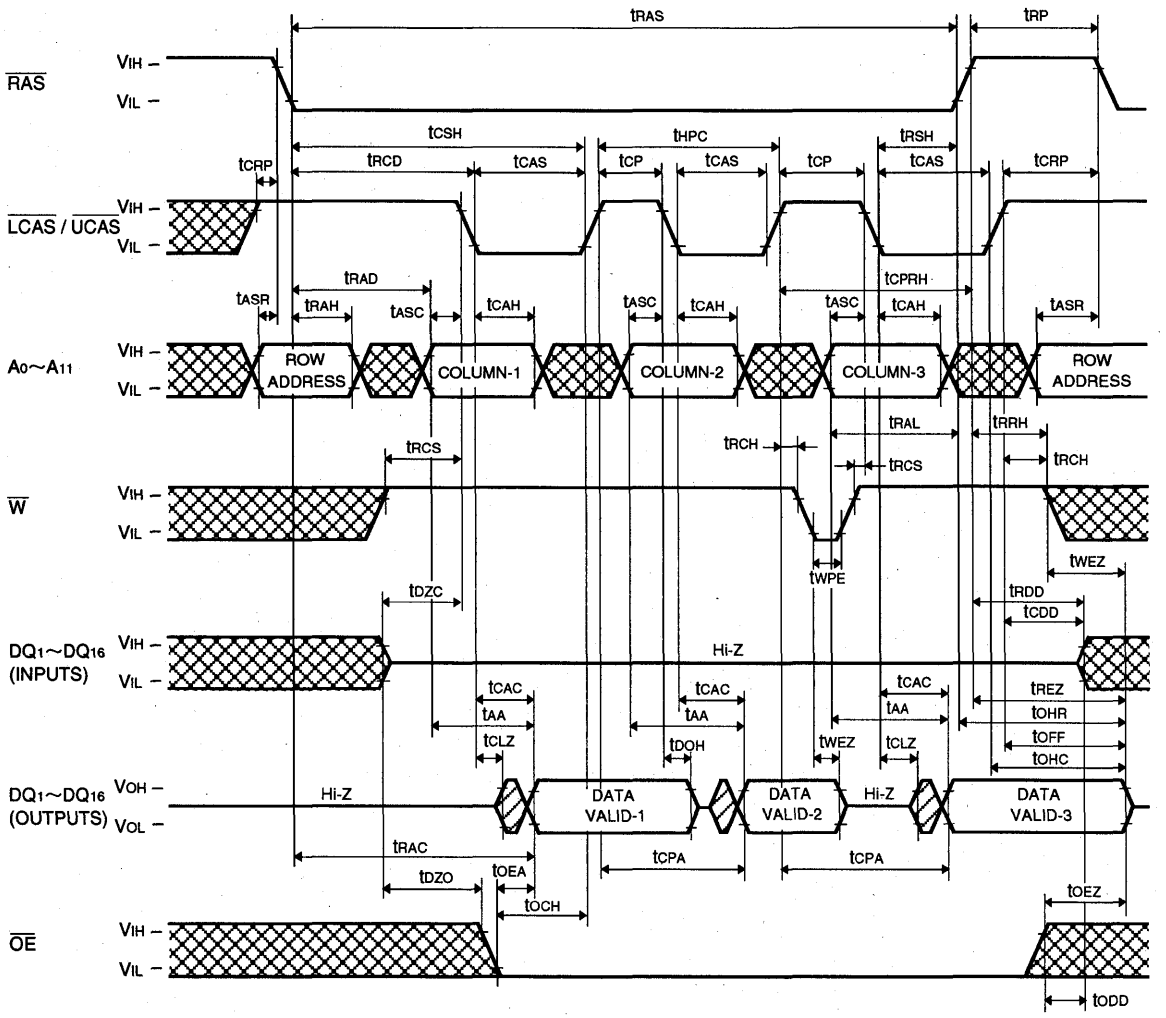
Hyper Page Mode Mix Cycle (2)



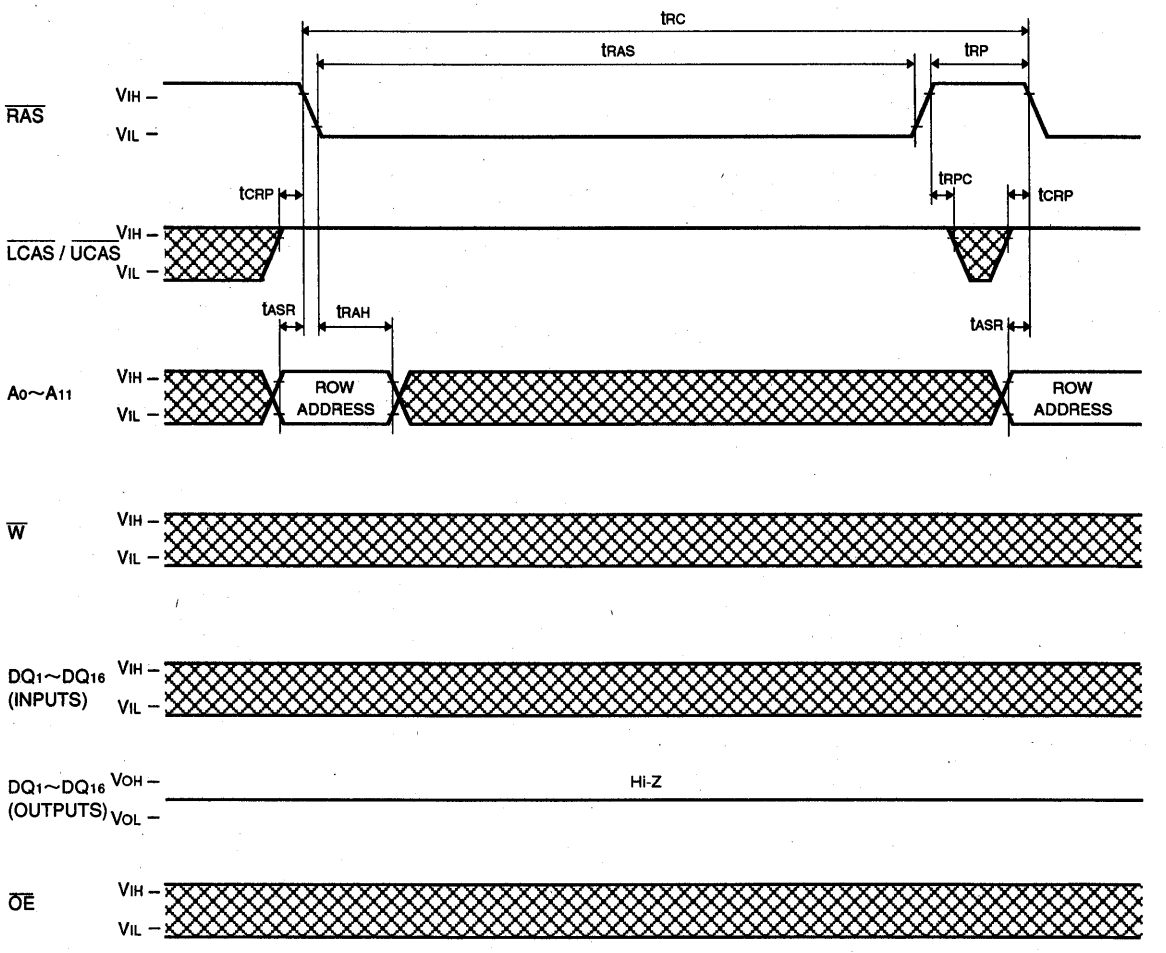
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



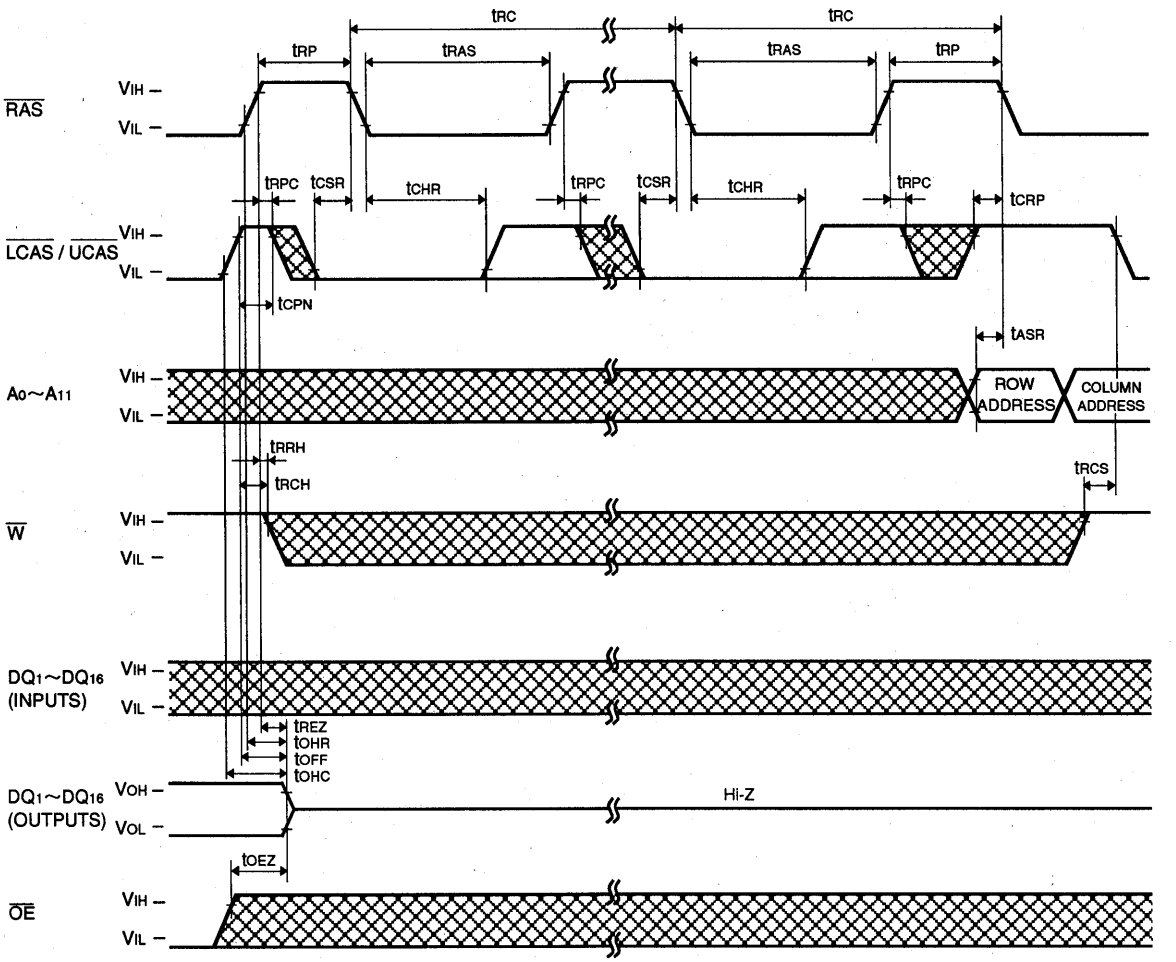
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



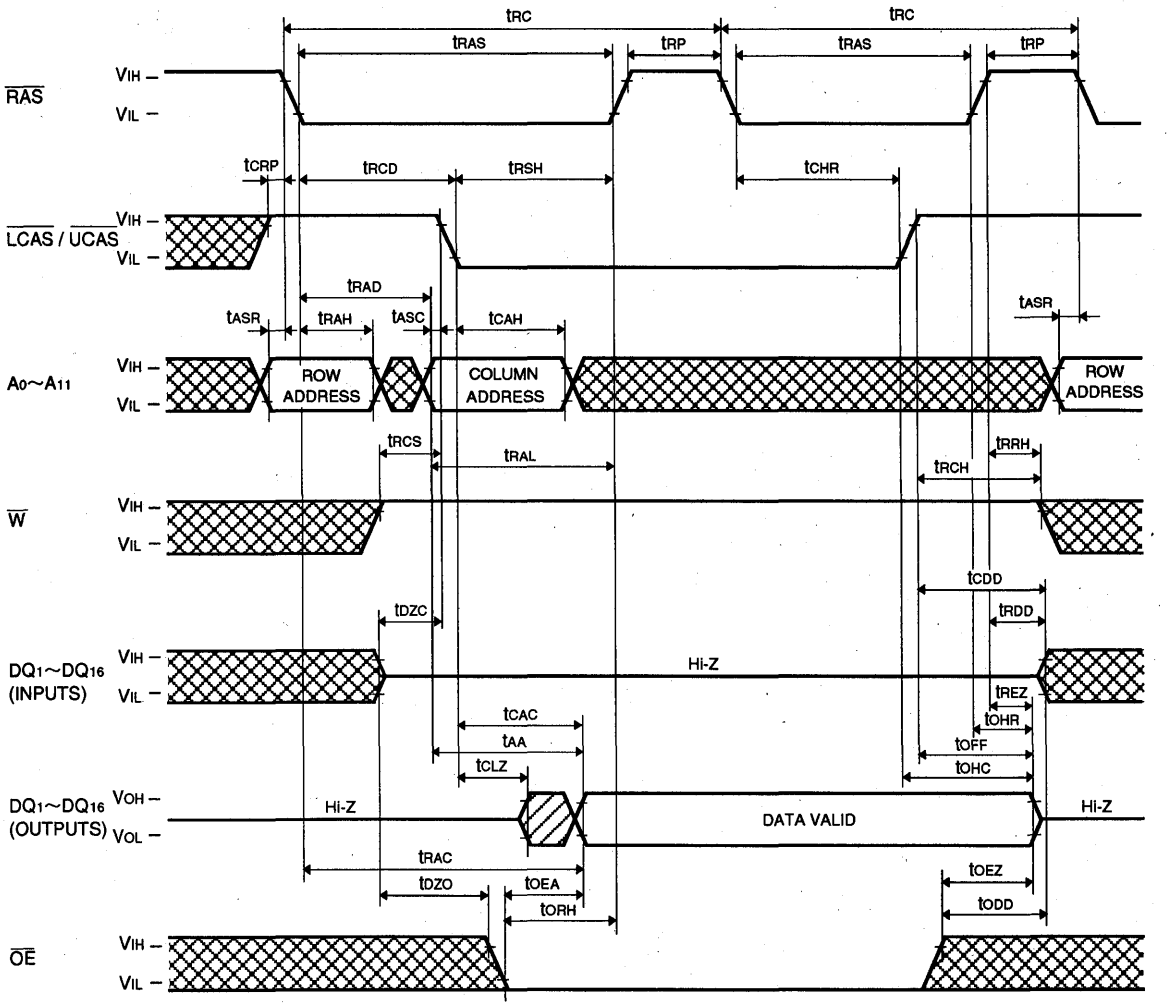
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

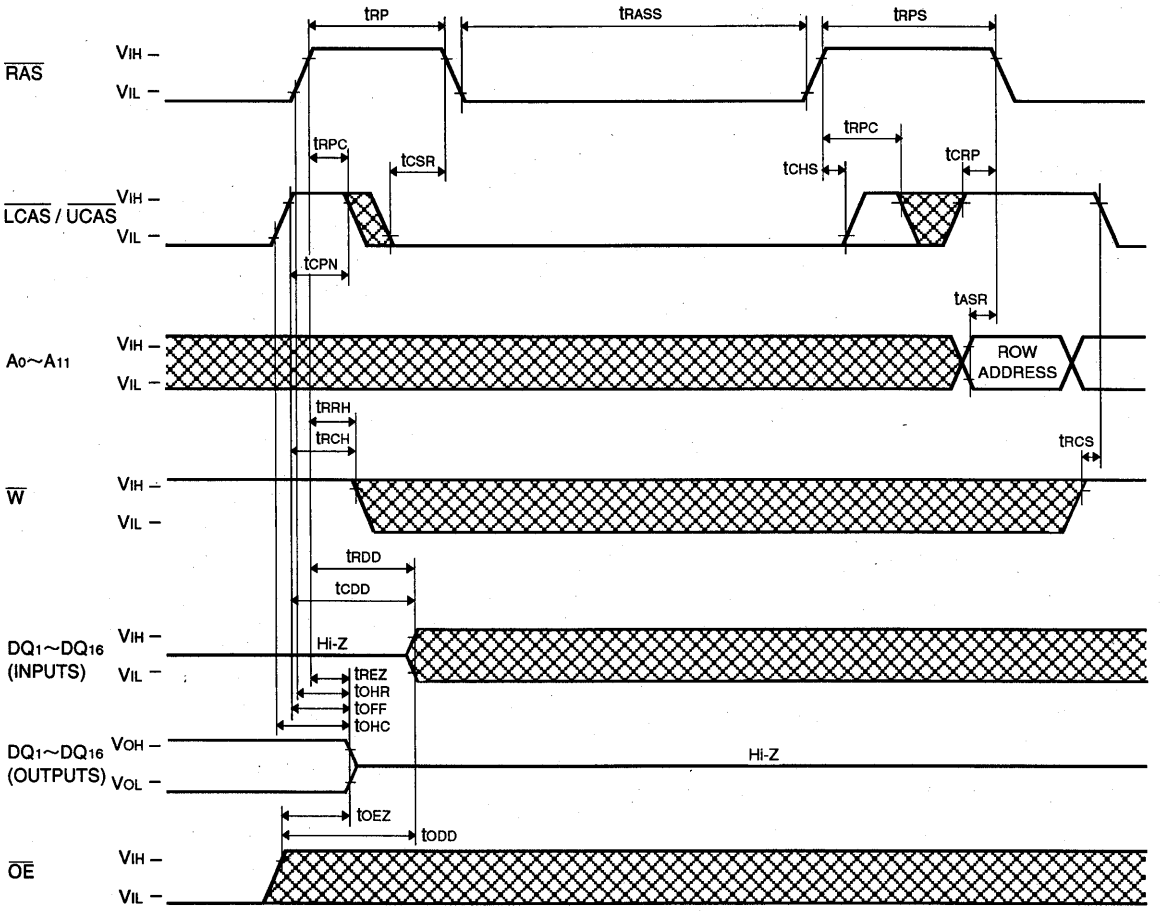


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle *



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8(AV)}$	Average supply current from Vcc Extended refresh mode	M5M4V16165B (S)	$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_{11}≦0.2V or ≧Vcc-0.2V t_{REF}=128ms, output open t_{RAS}=t_{RASmin}~1μs			400	μA
$I_{CC9(AV)}$	Average supply current from Vcc Self-refresh cycle	M5M4V16165B (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

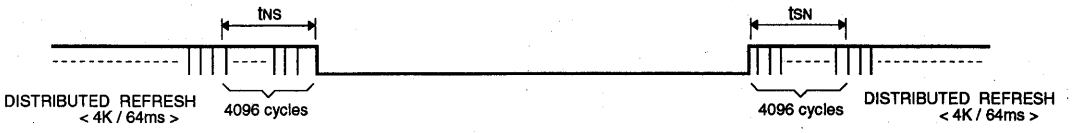
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M4V16165B-6S		M5M4V16165B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

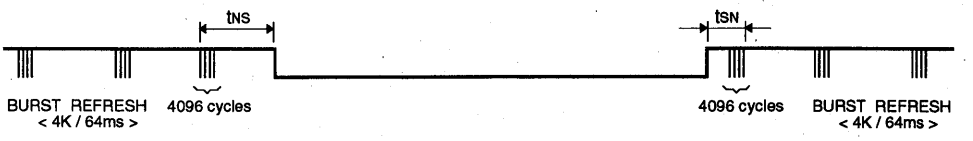
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦64ms and t_{SN}≦64ms.



(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} efore / after self refresh, on the condition of t_{NS} +t_{SN}≦64ms.



M5M4V18165BTP-6,-7,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

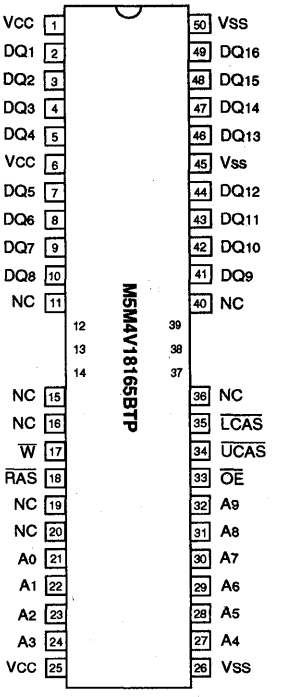
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18165BTP-6,-6S	60	15	30	15	110	450
M5M4V18165BTP-7,-7S	70	20	35	20	130	390

- Standard 50 pin TSOP
- Single 3.3V ±0.3v supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V18165BTP-6,-6S---------- 615.0mW (Max)
  M5M4V18165BTP-7,-7S---------- 540.0mW (Max)
- Hyper-page mode, Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 50P3W-L (400mil TSOP Normal Bend)

NC : NO CONNECTION

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

FUNCTION

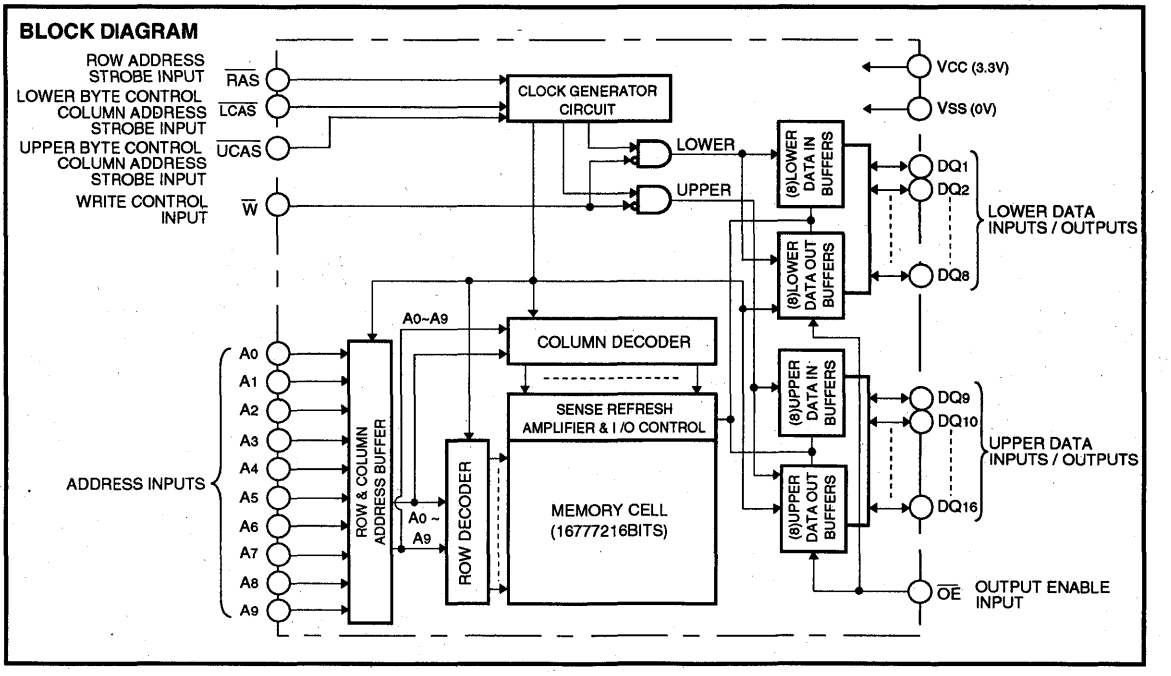
The M5M4V18165BTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25 °C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦V_{CC}	-10		10	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}+0.3V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3,4,5)	M5M4V18165B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			170	mA
		M5M4V18165B-7,-7S				150	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V18165B-6,-7	$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.5	
		M5M4V18165B-6S,-7S	$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.15	
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 3,5)	M5M4V18165B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			170	mA
		M5M4V18165B-7,-7S				150	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M4V18165B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			130	mA
		M5M4V18165B-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18165B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			170	mA
		M5M4V18165B-7,-7S				150	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high	(Note 12)	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10uA|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits				Unit
			M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time	-6, -7		16.4		16.4	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	10		13		ns
tWP	Write pulse width	10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 23)	133		161		ns
tRAS	$\overline{RAS}$ low pulse width	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 24)	32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 24)	77		92		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 24)	47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧ tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
		Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time	66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 27)	10	18	13	18	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)	7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read	62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read	30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	35		40		ns

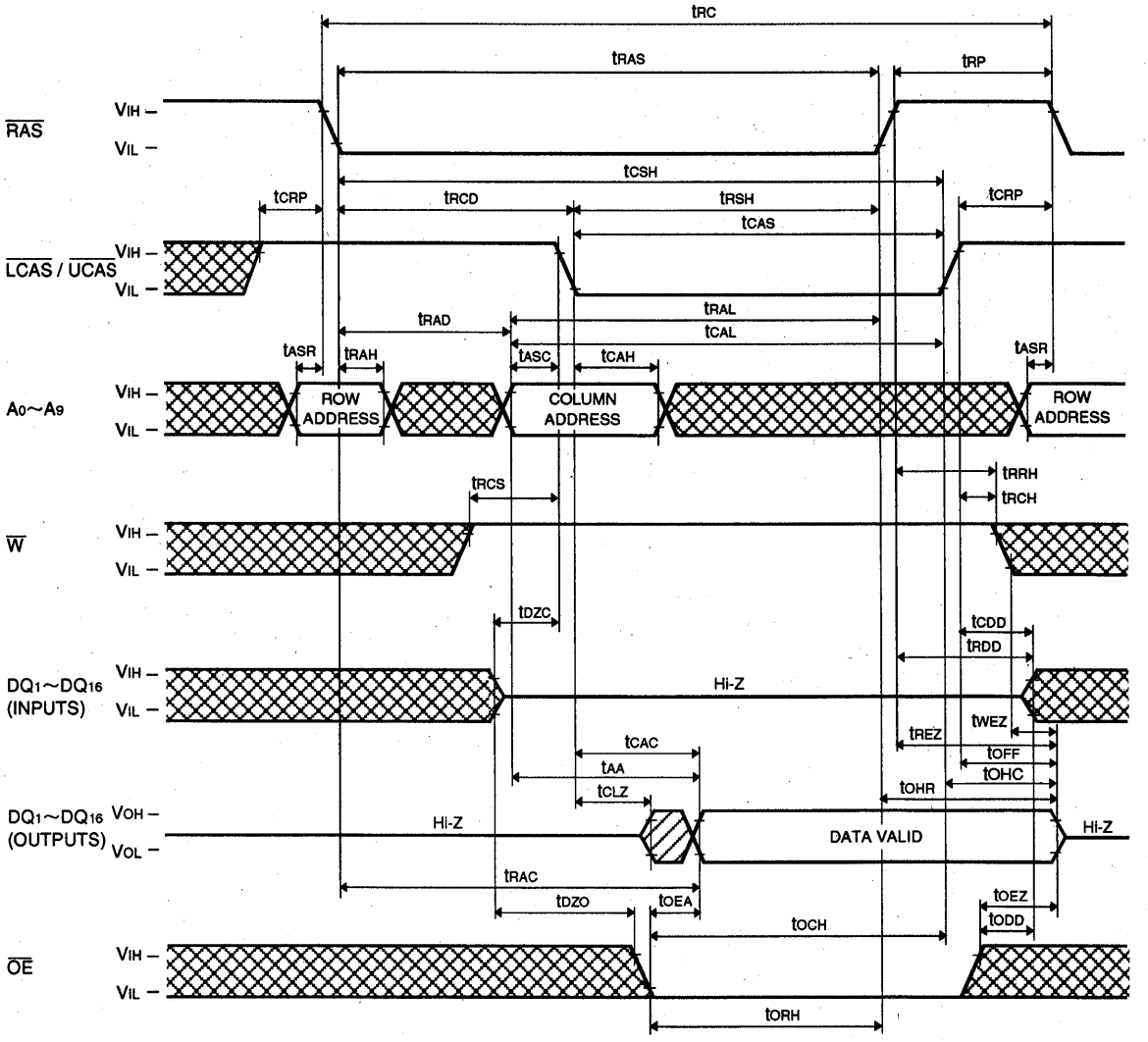
Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M4V18165B-6,-6S		M5M4V18165B-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 29)
Read Cycle

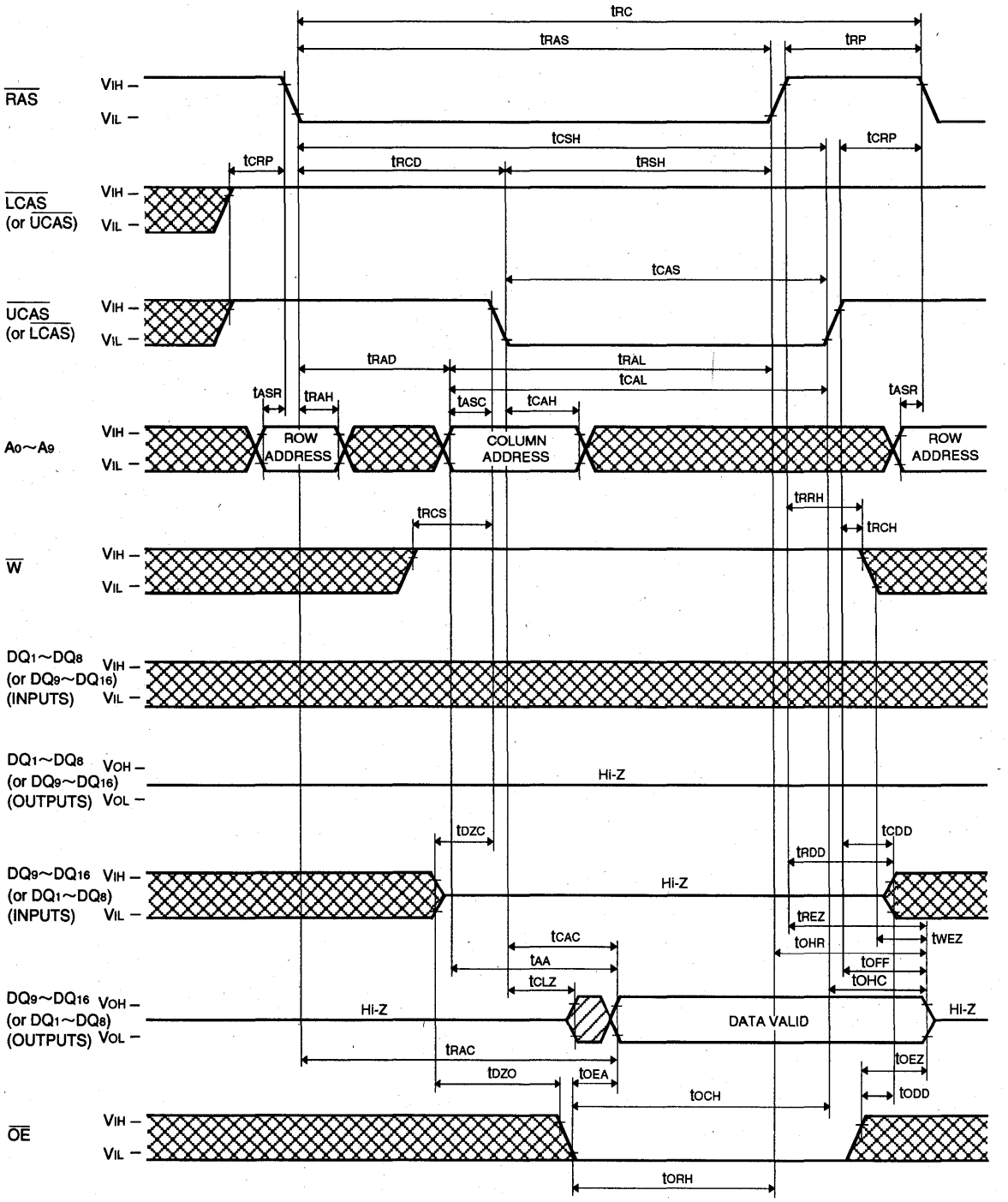


Note 29

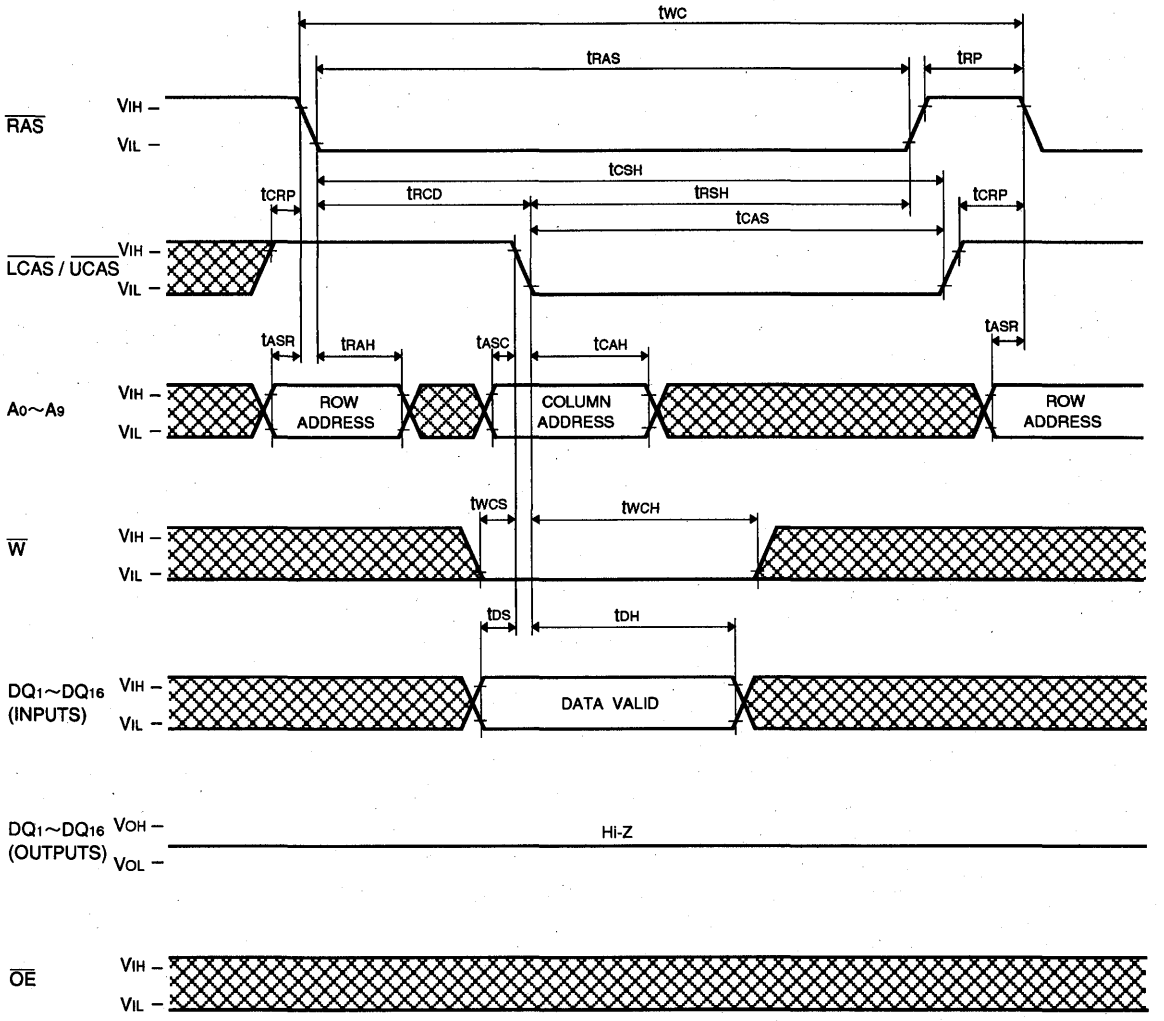
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

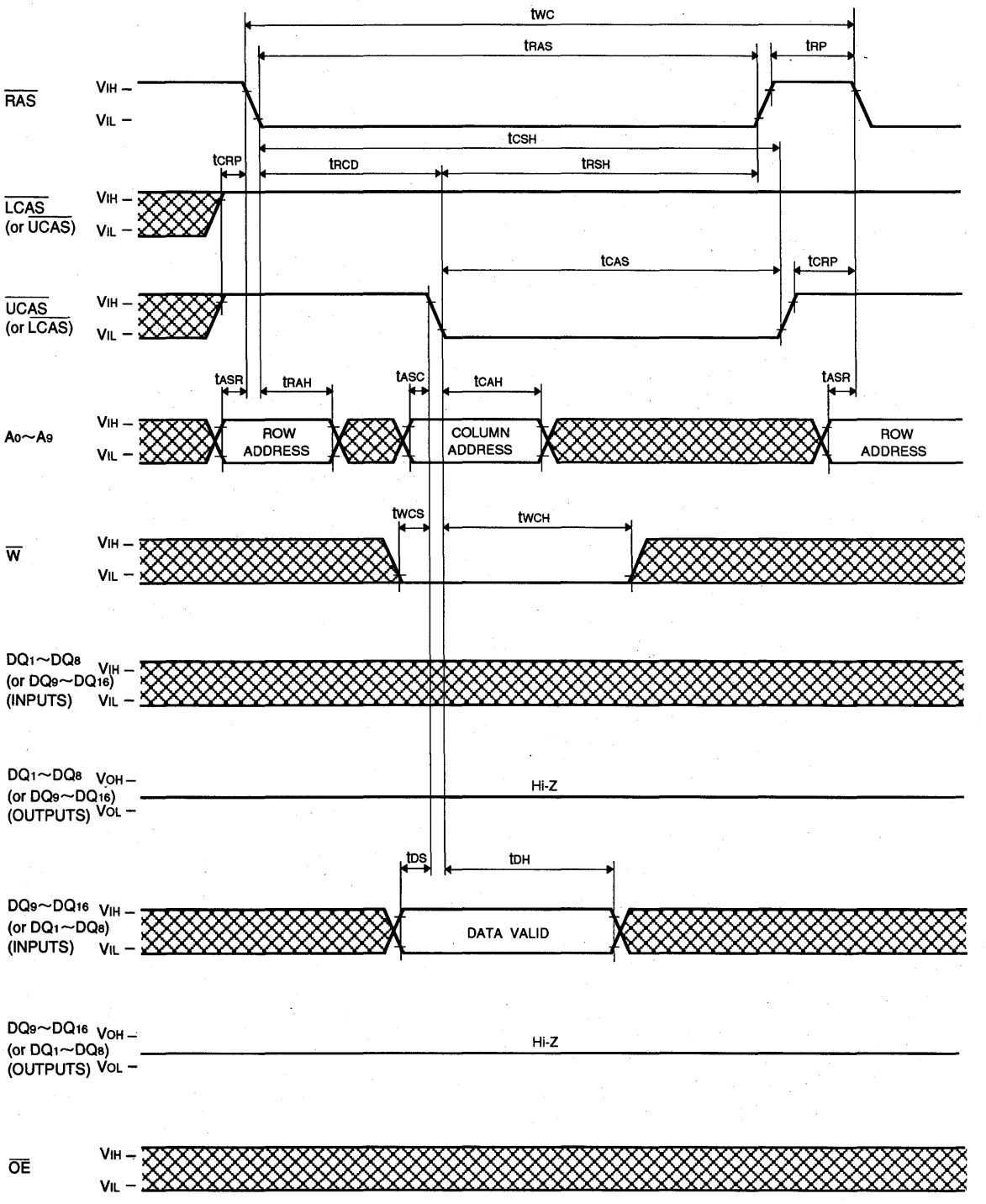
Byte Read Cycle



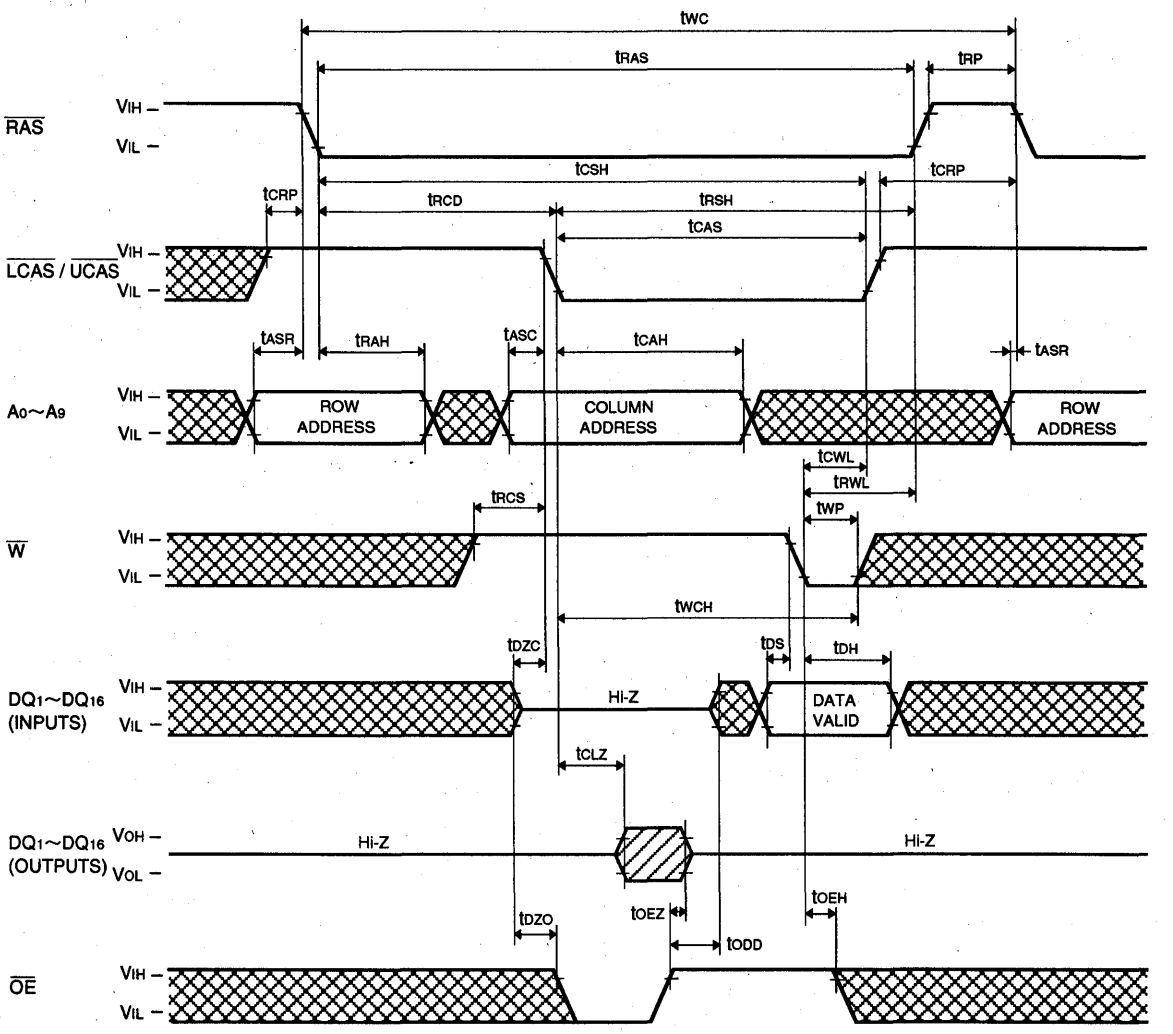
Early Write Cycle



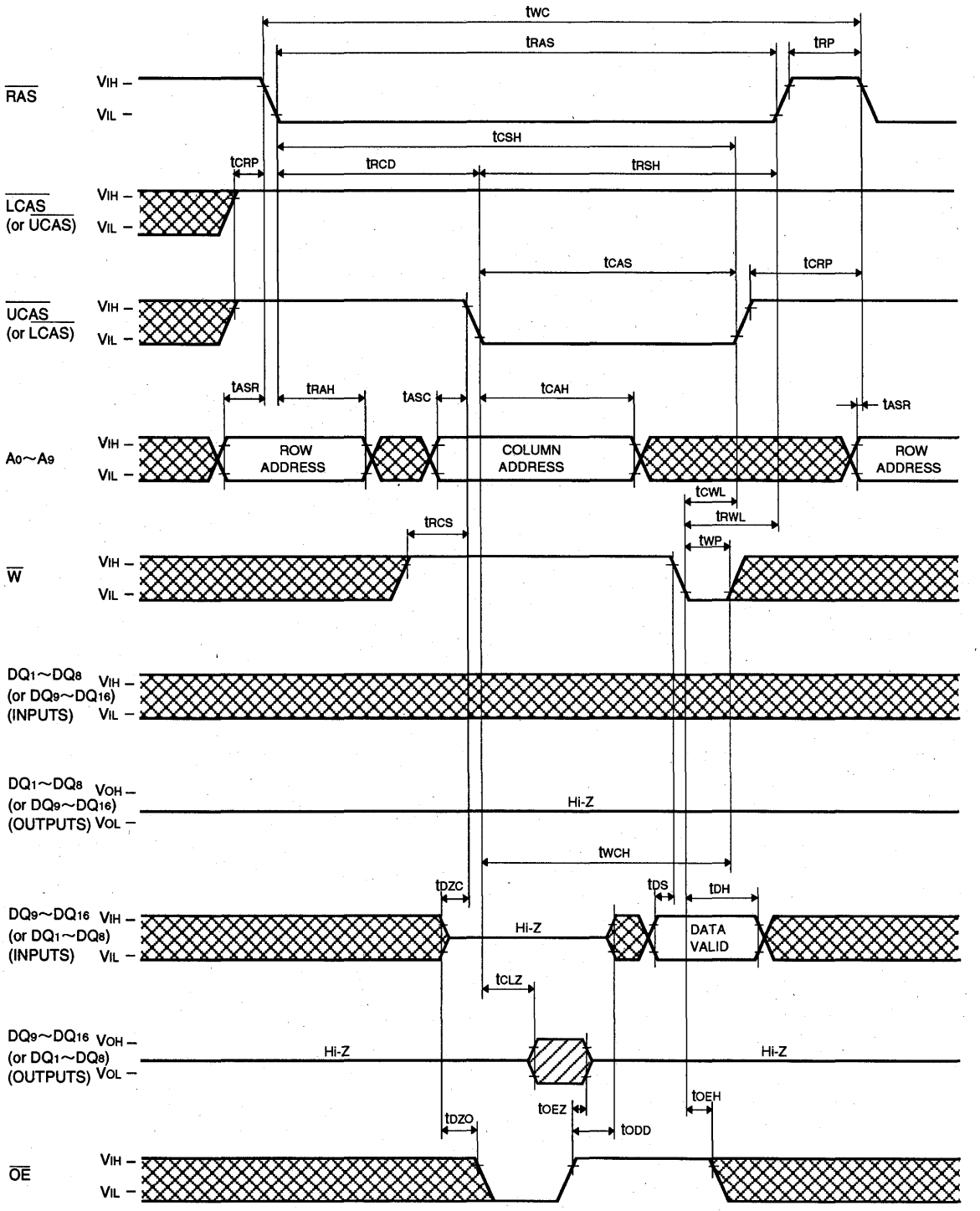
Byte Early Write Cycle



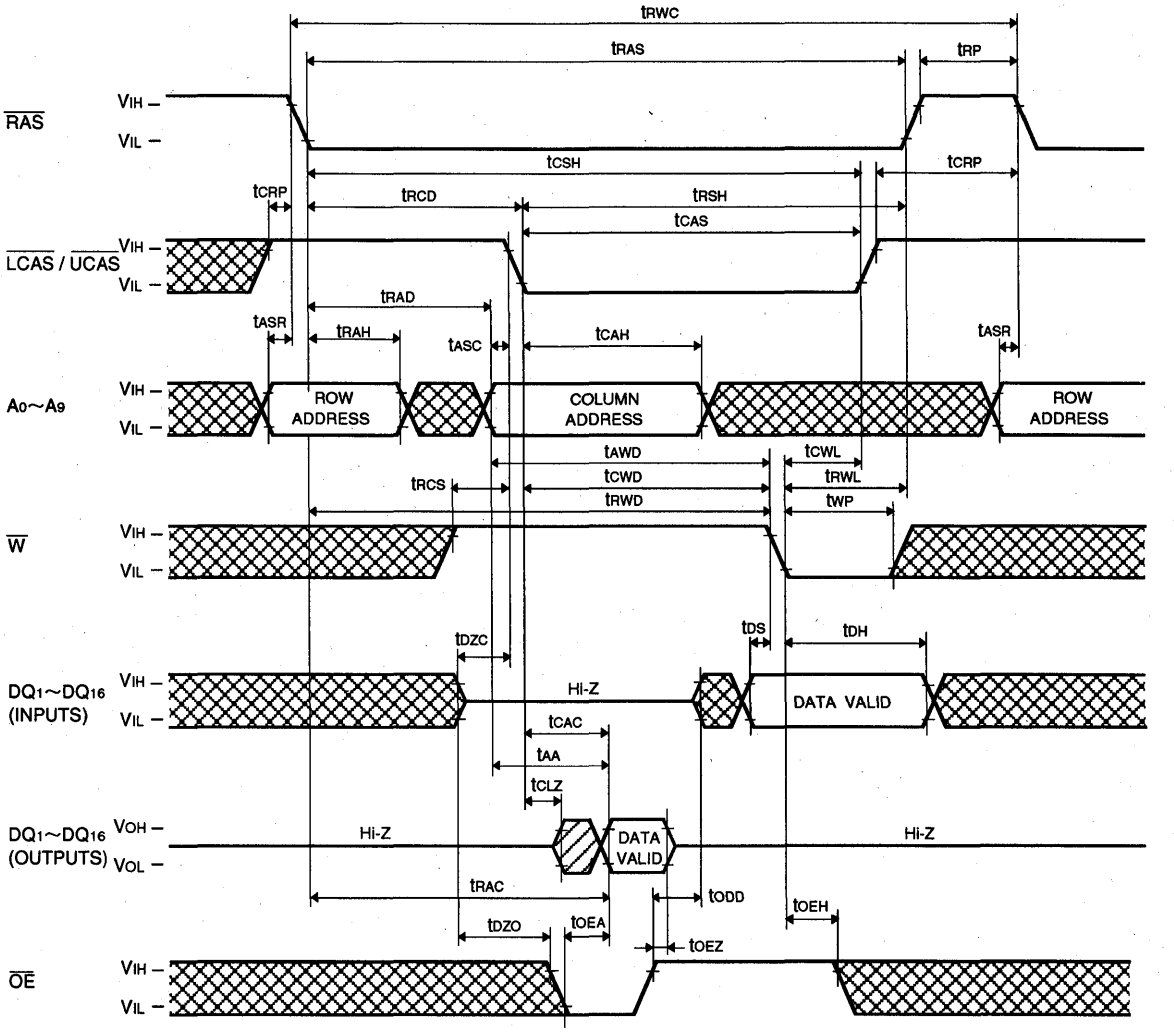
Delayed Write Cycle



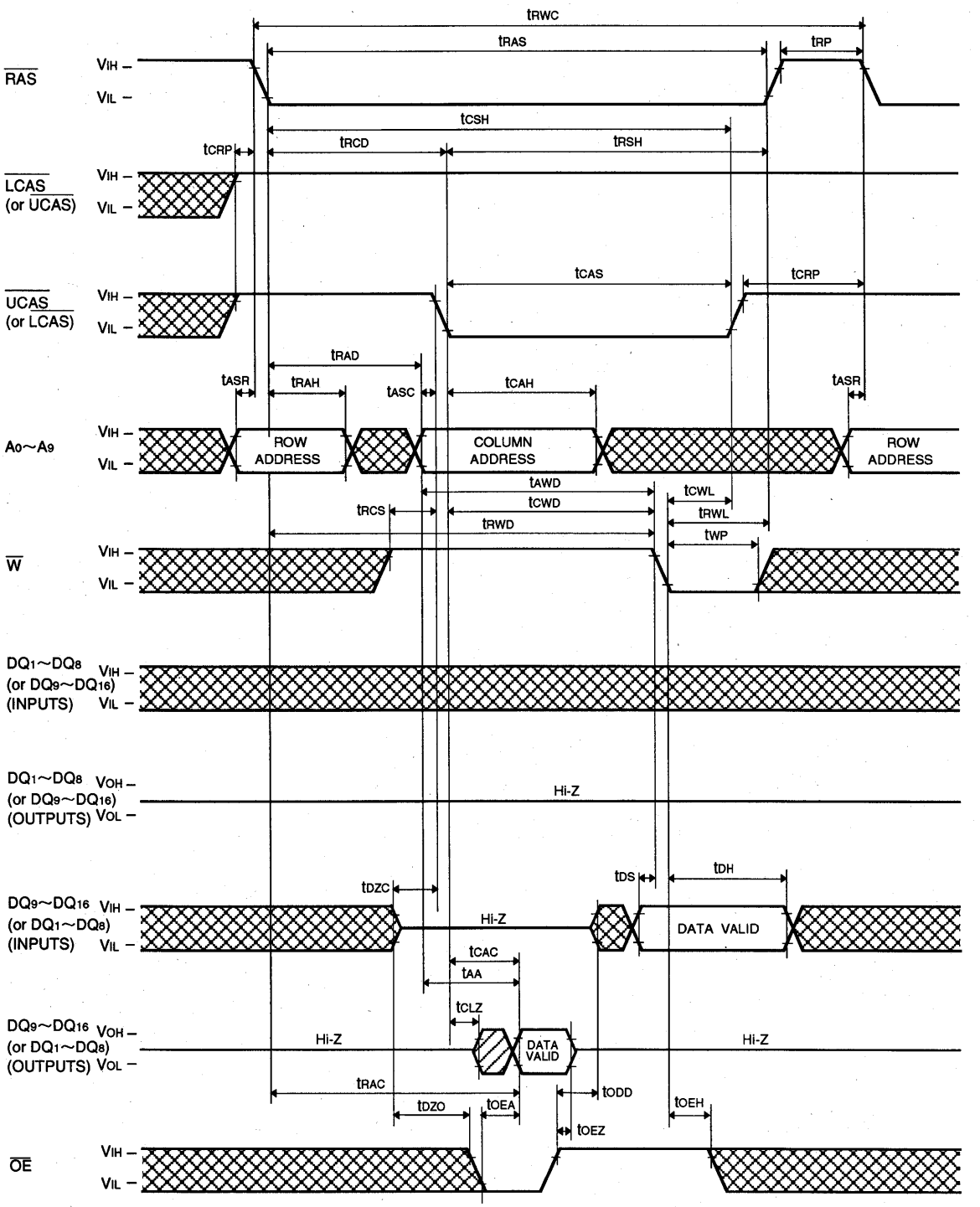
Byte Delayed Write Cycle



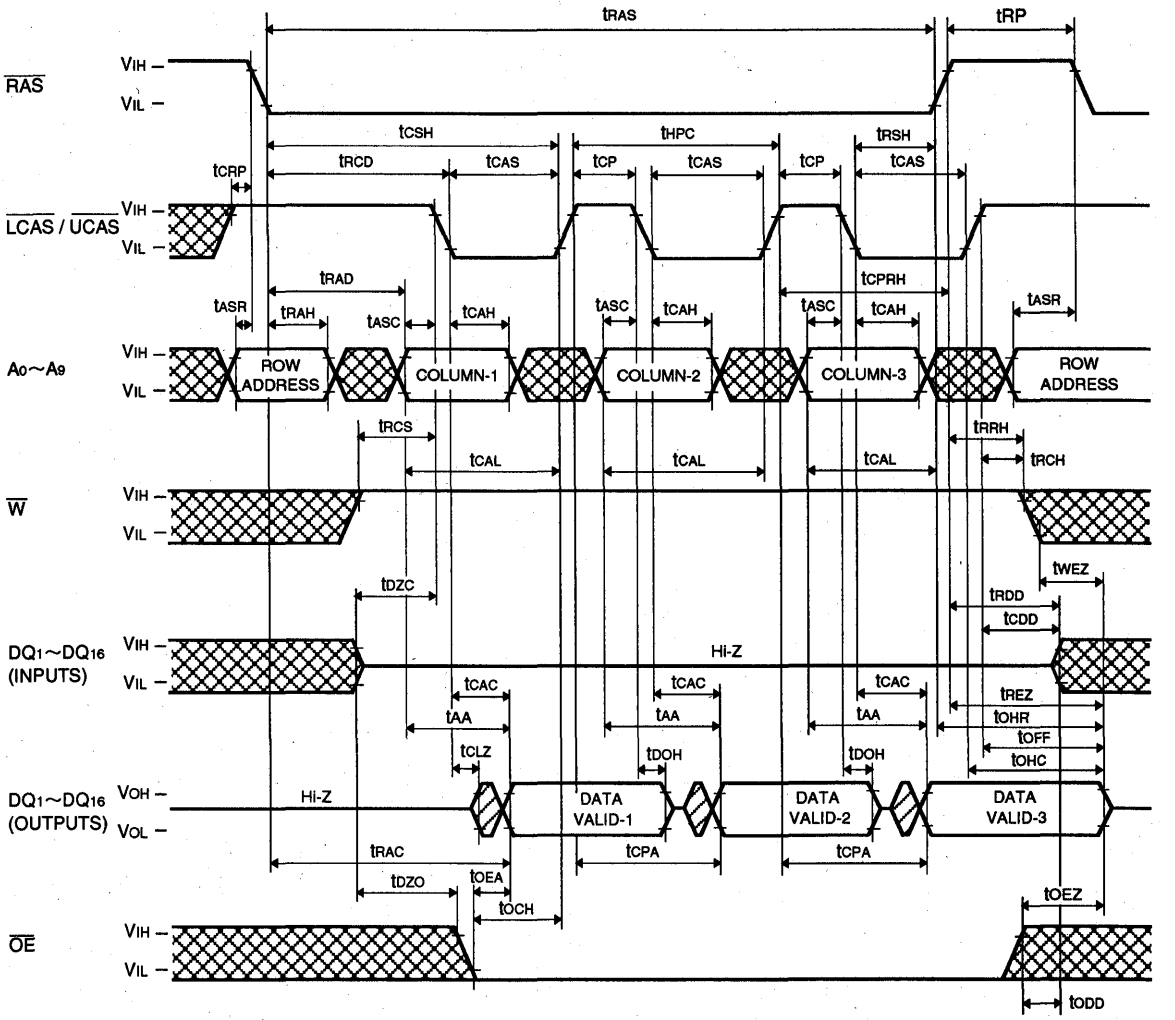
Read-Write, Read-Modify-Write Cycle



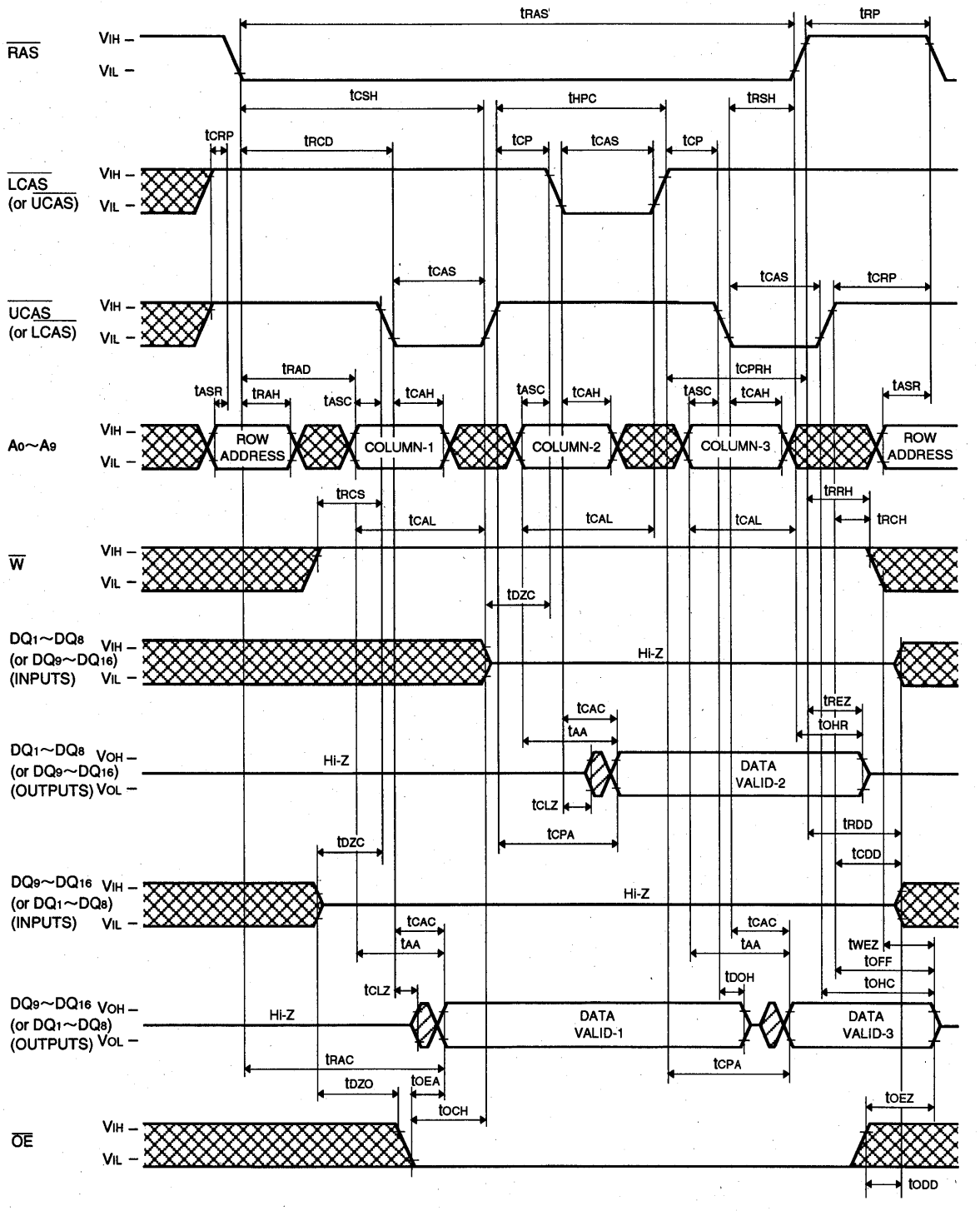
Byte Read-Write, Read-Modify-Write Cycle



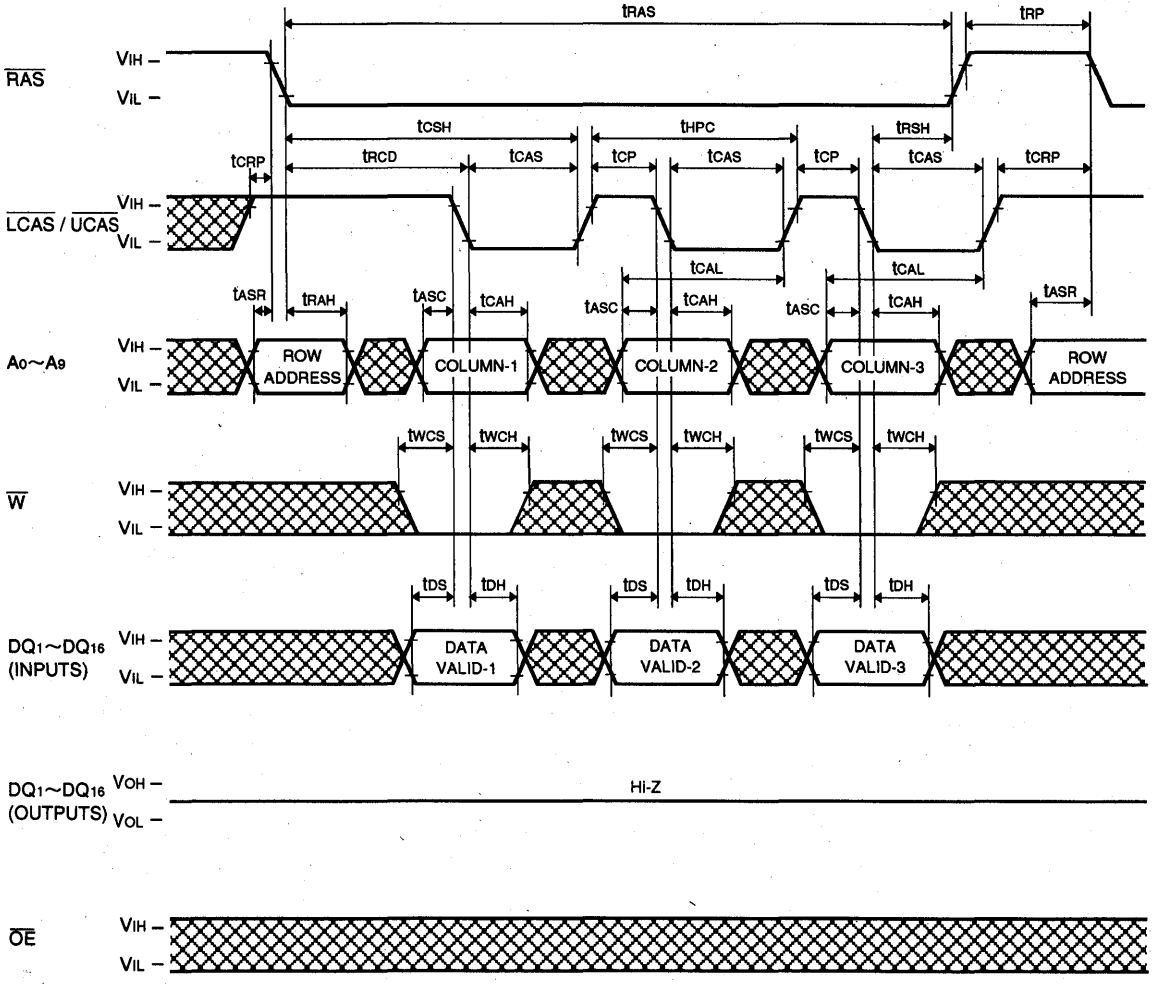
Hyper Page Mode Read Cycle



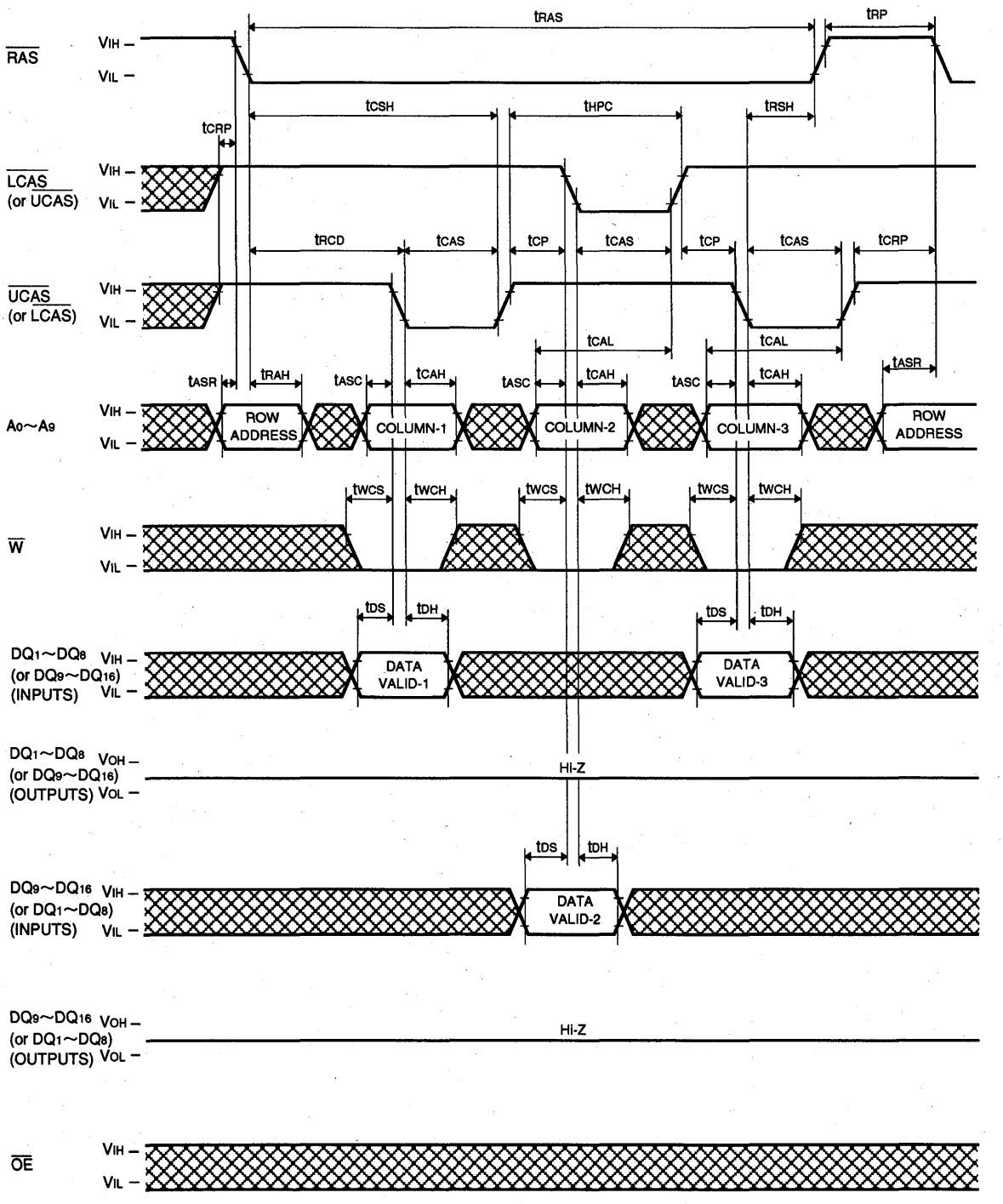
Hyper Page Mode Byte Read Cycle



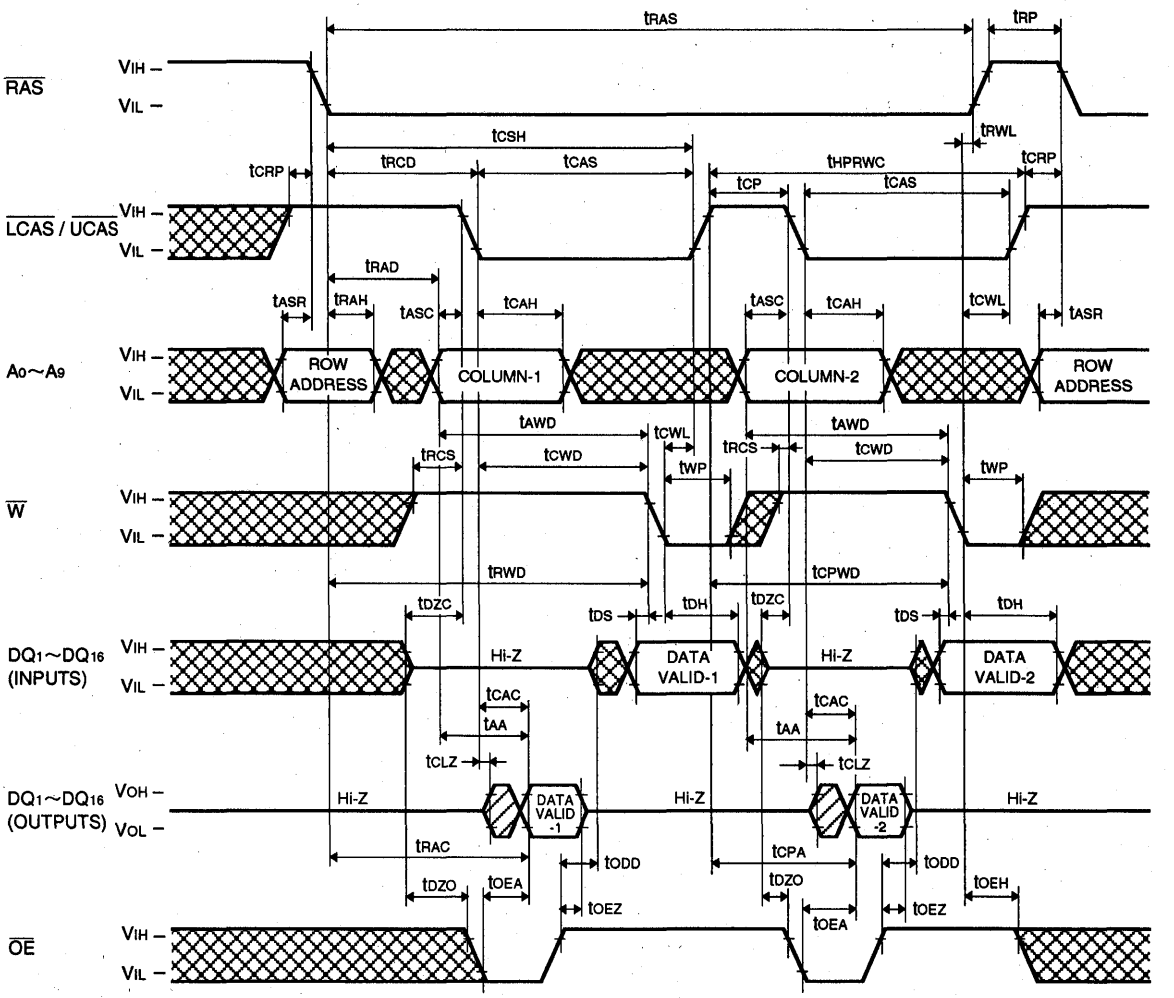
Hyper Page Mode Early Write Cycle



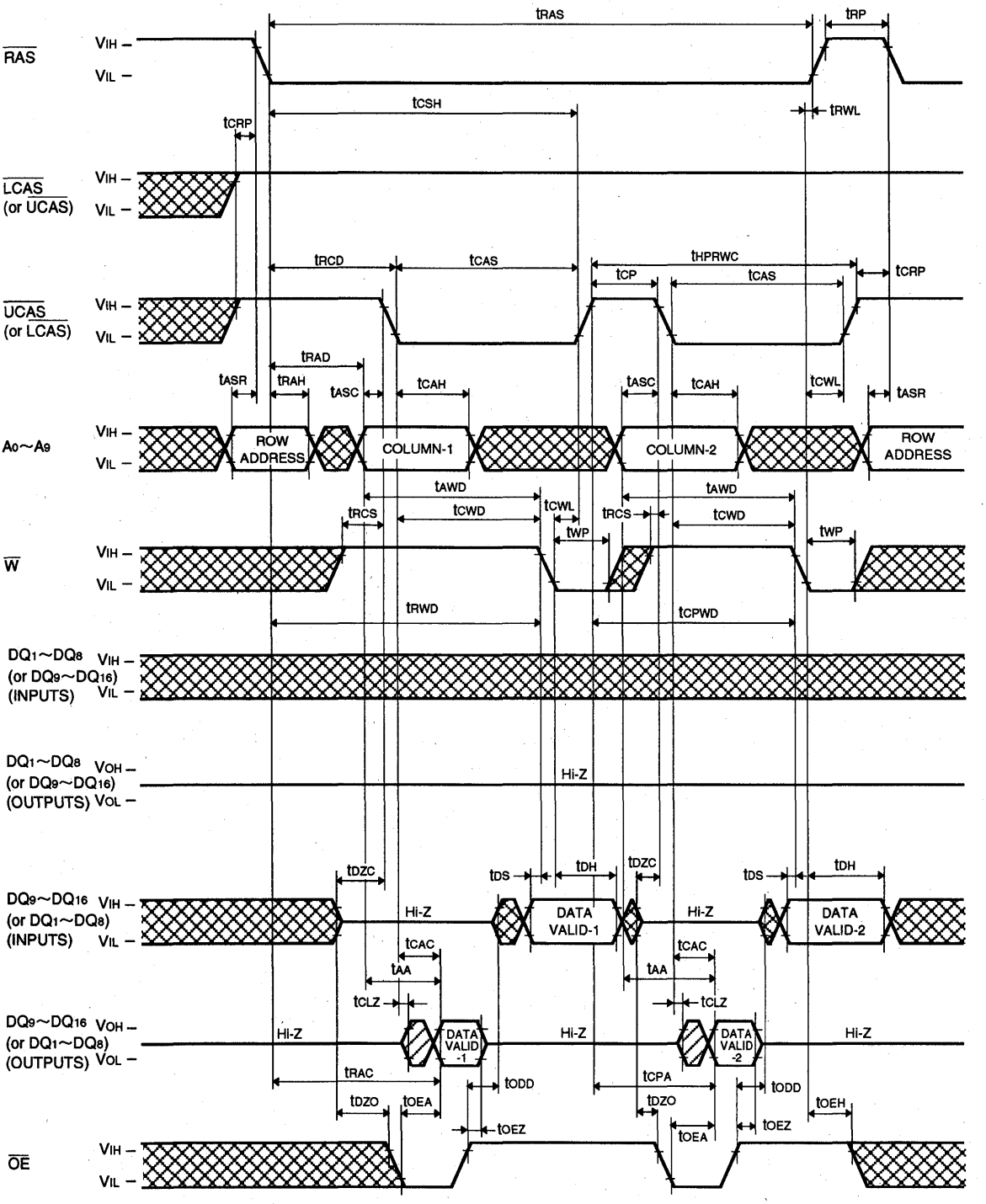
Hyper Page Mode Byte Early Write Cycle



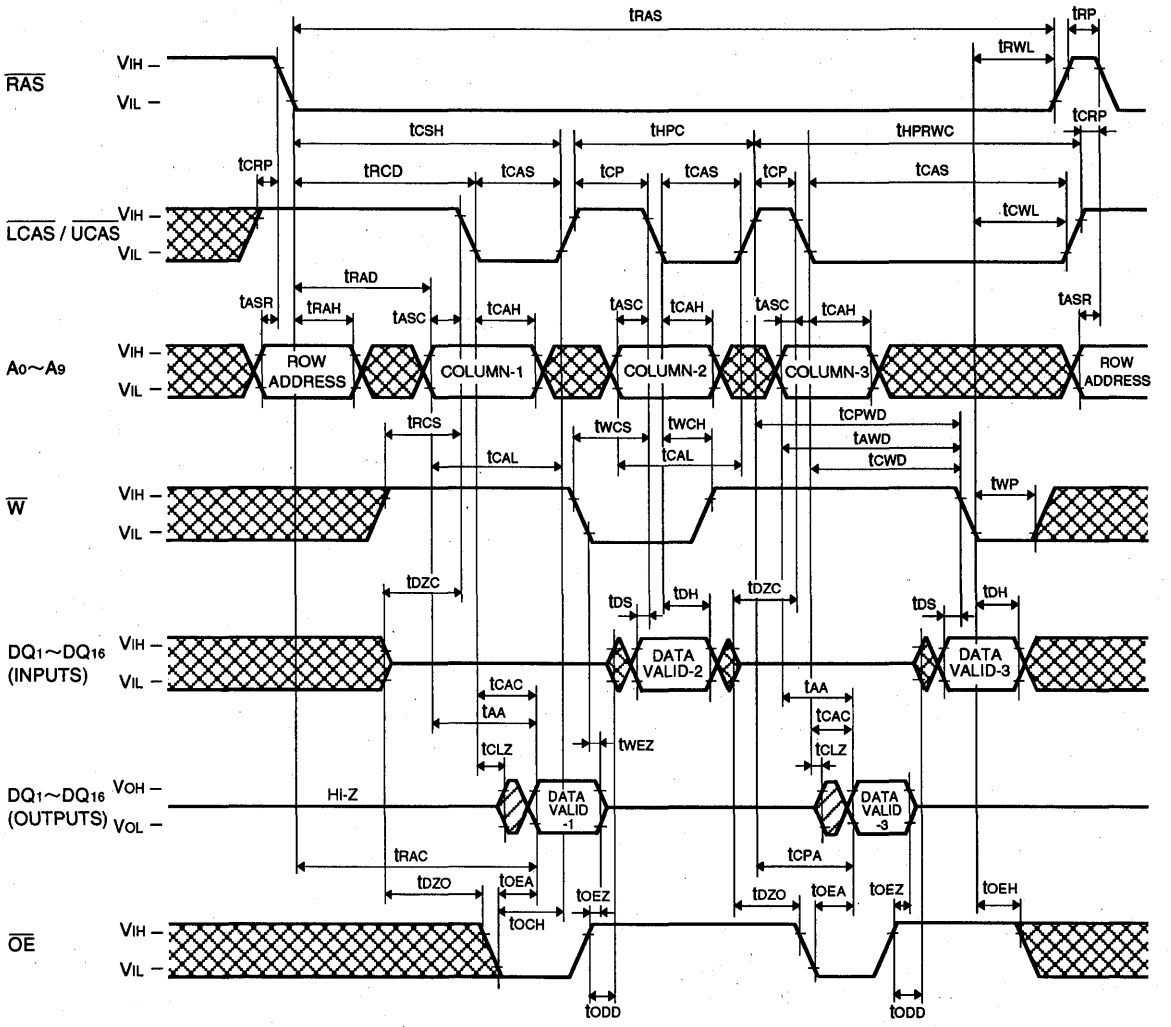
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



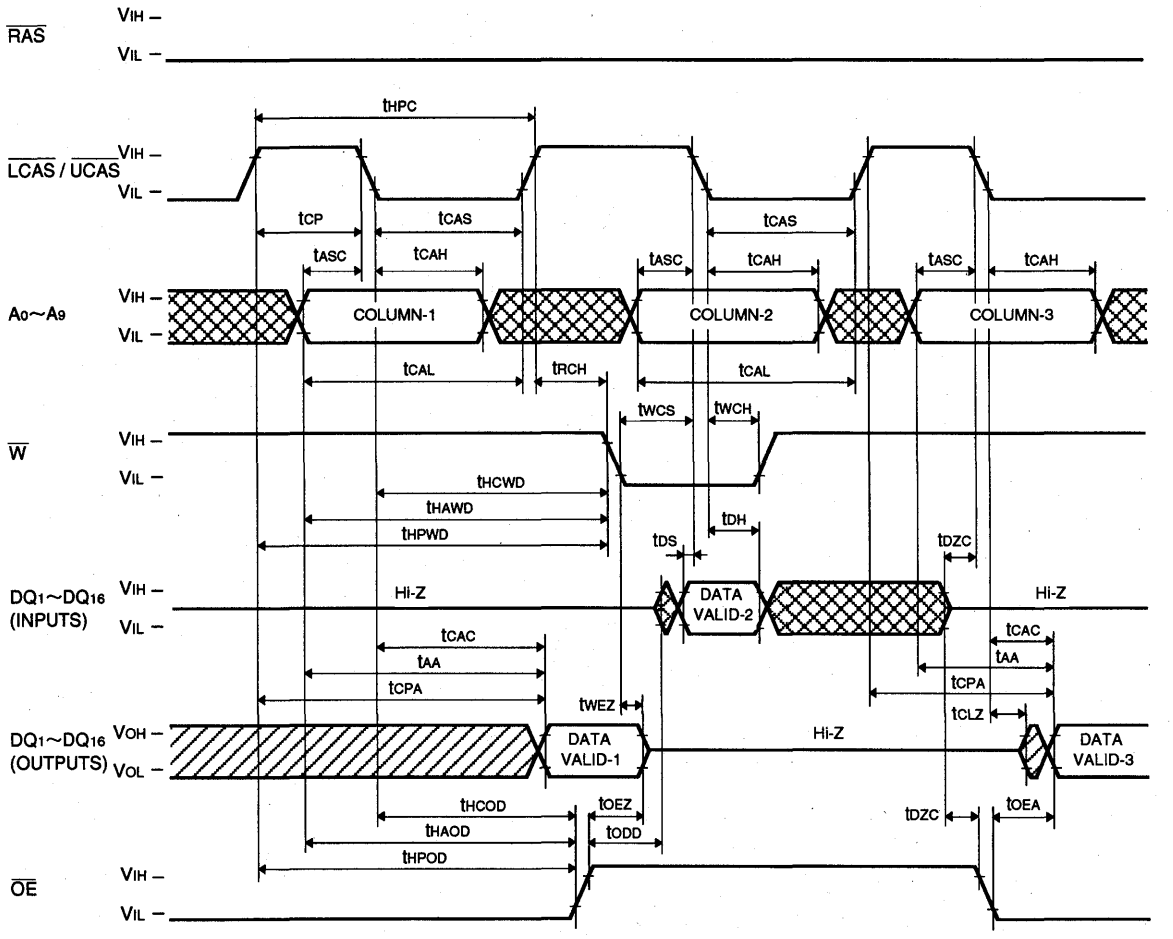
Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



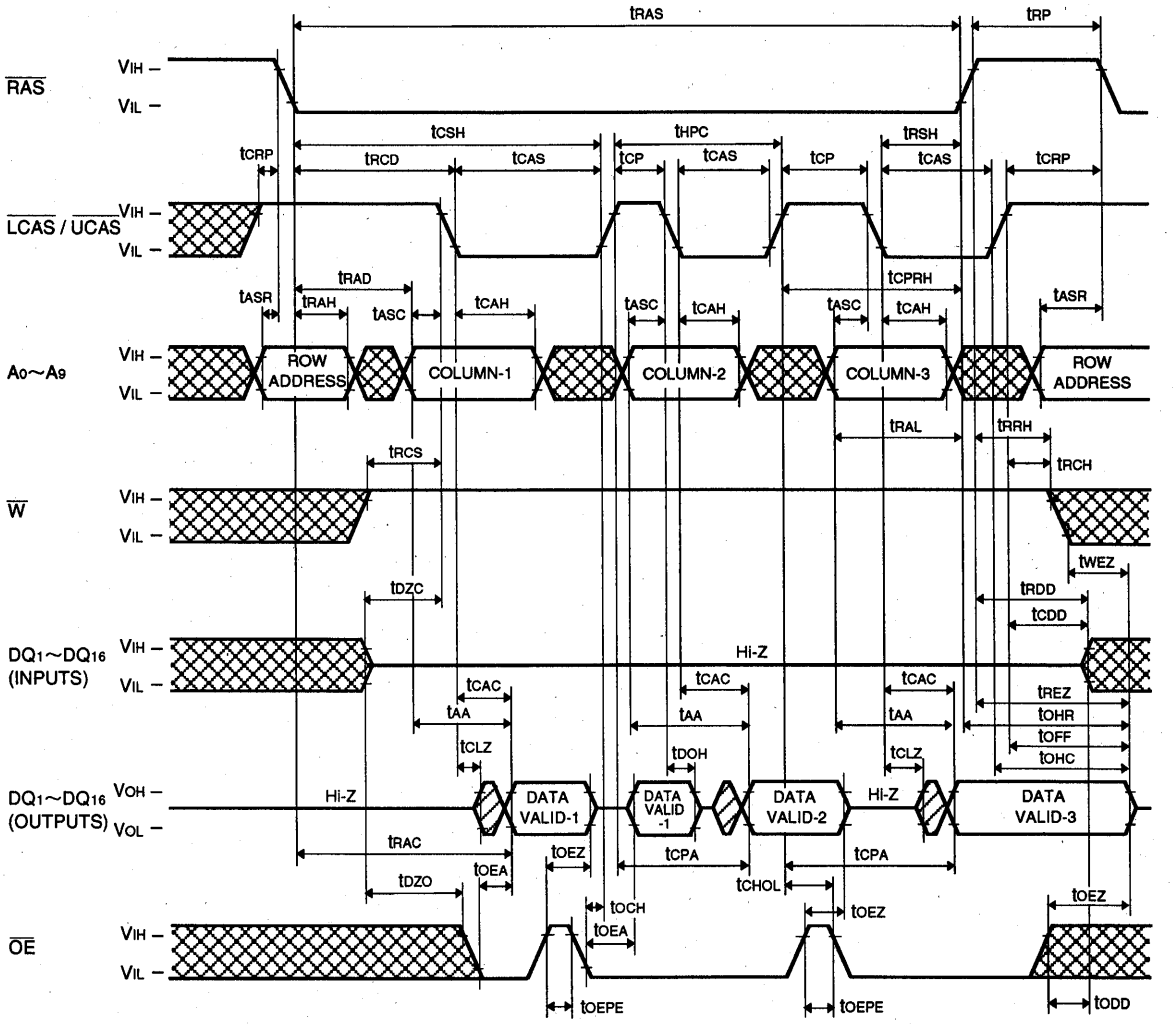
Hyper Page Mode Mix Cycle (1)



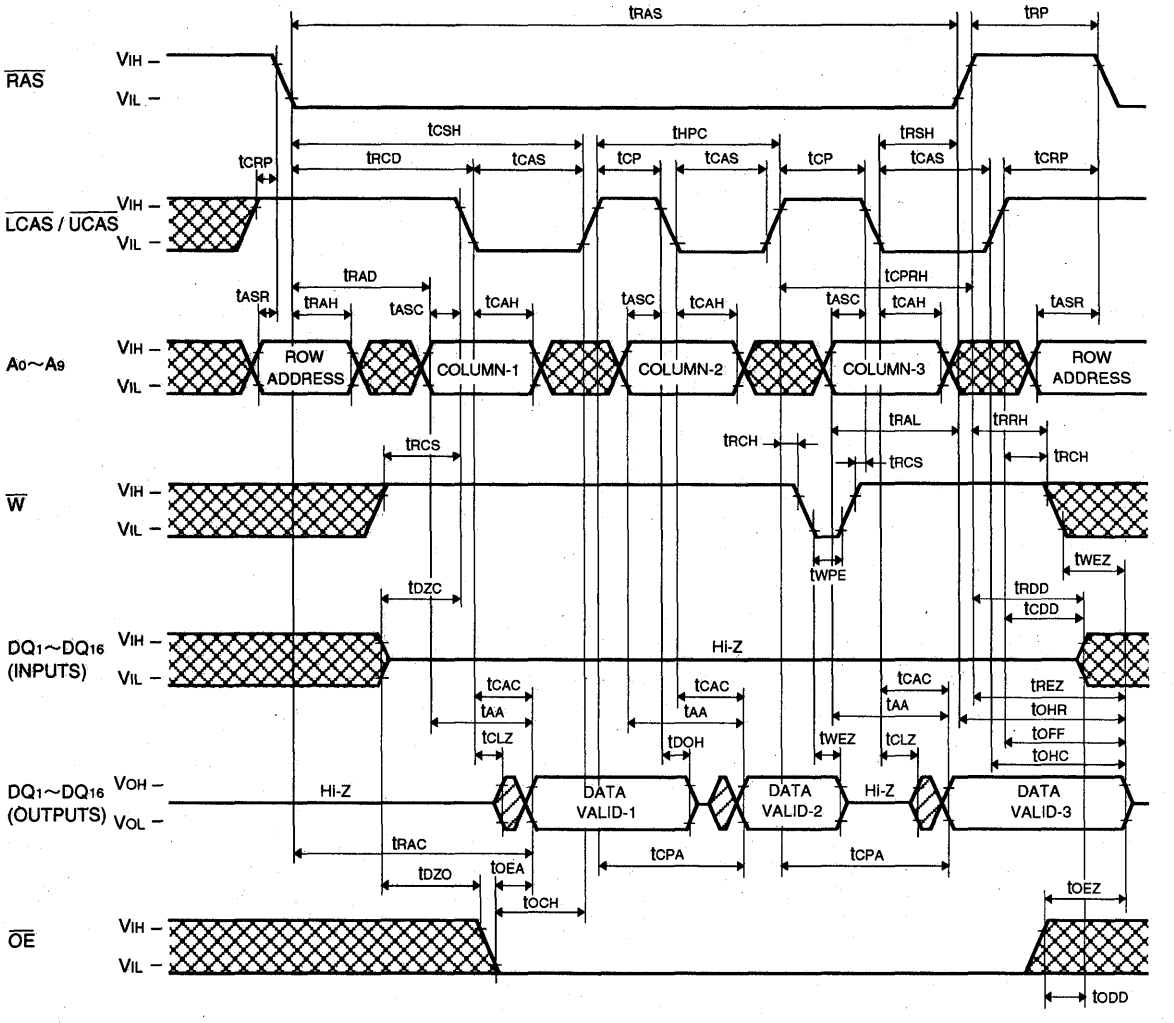
Hyper Page Mode Mix Cycle (2)



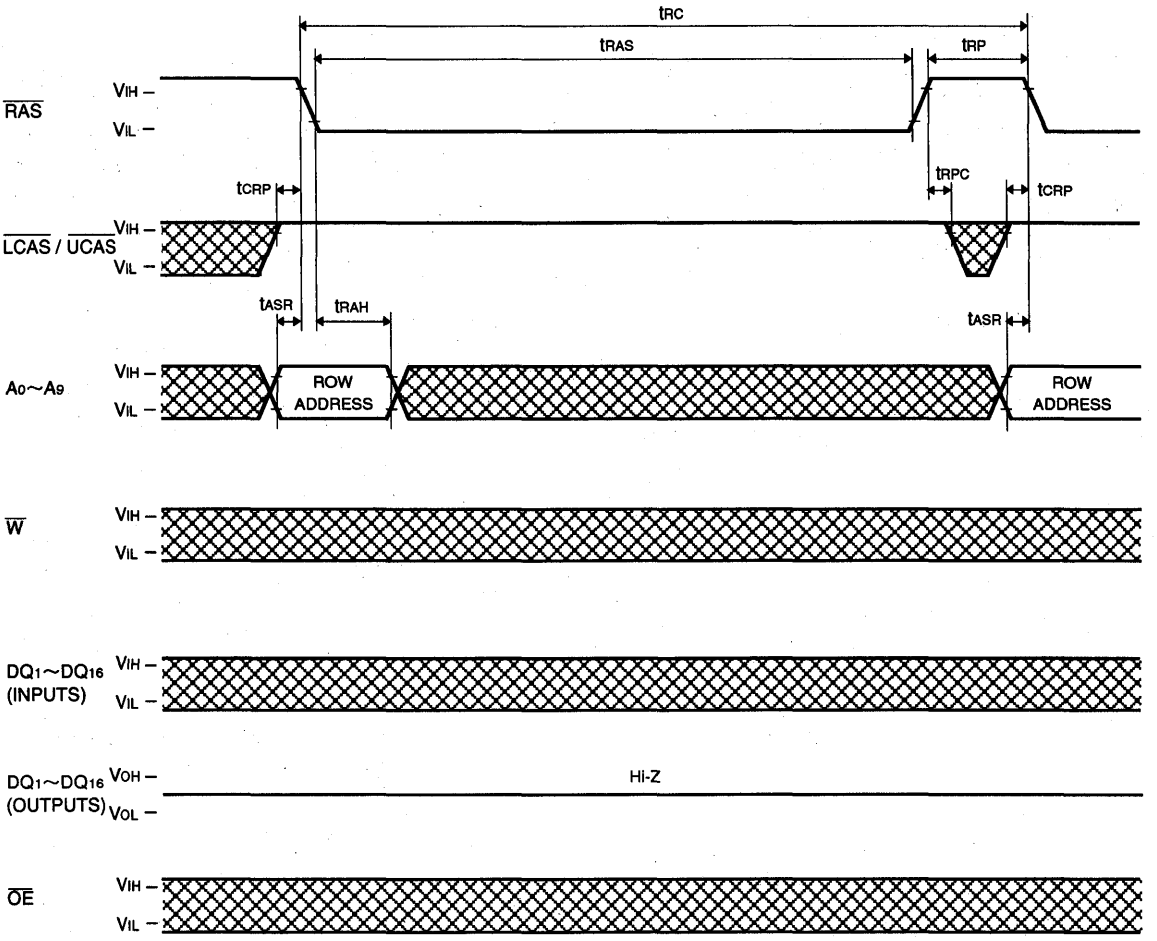
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



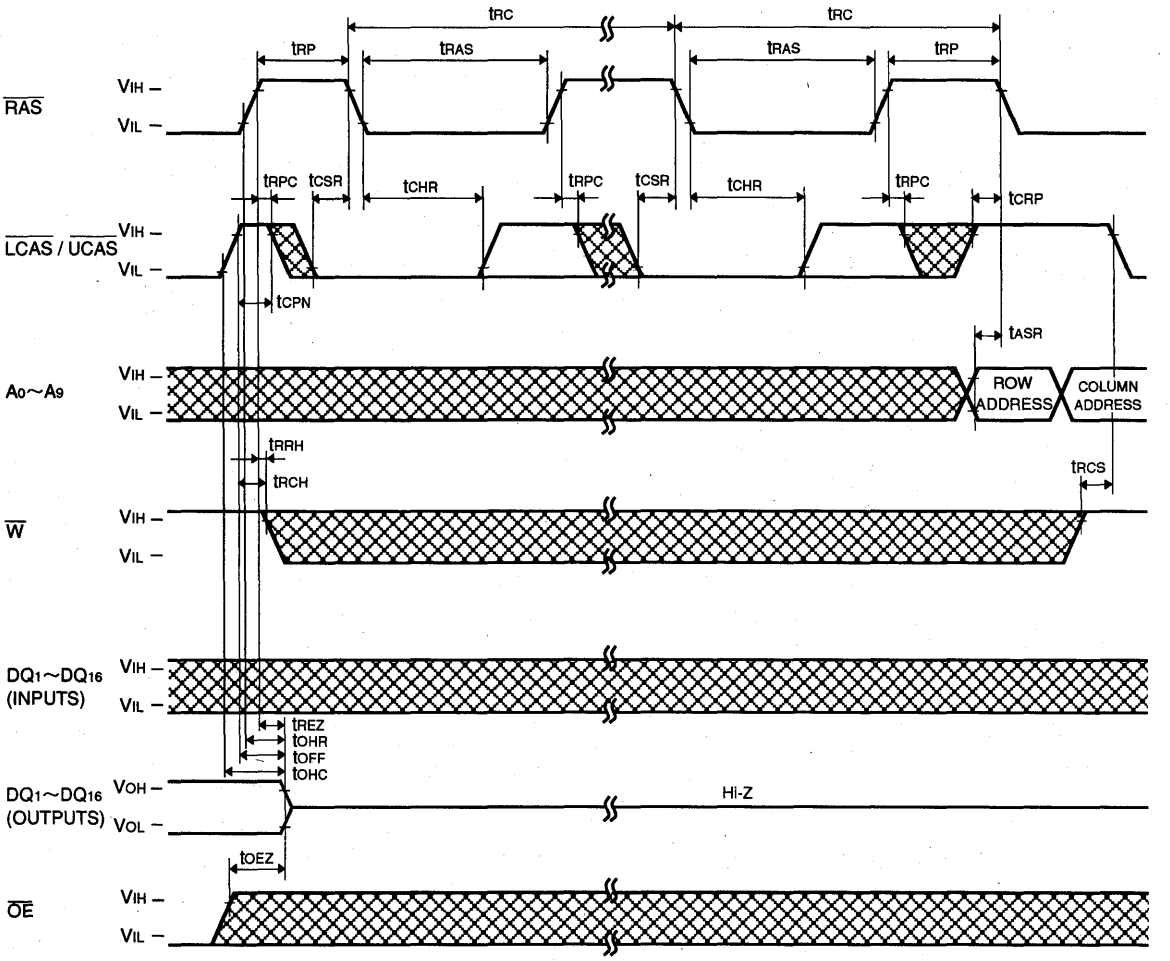
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



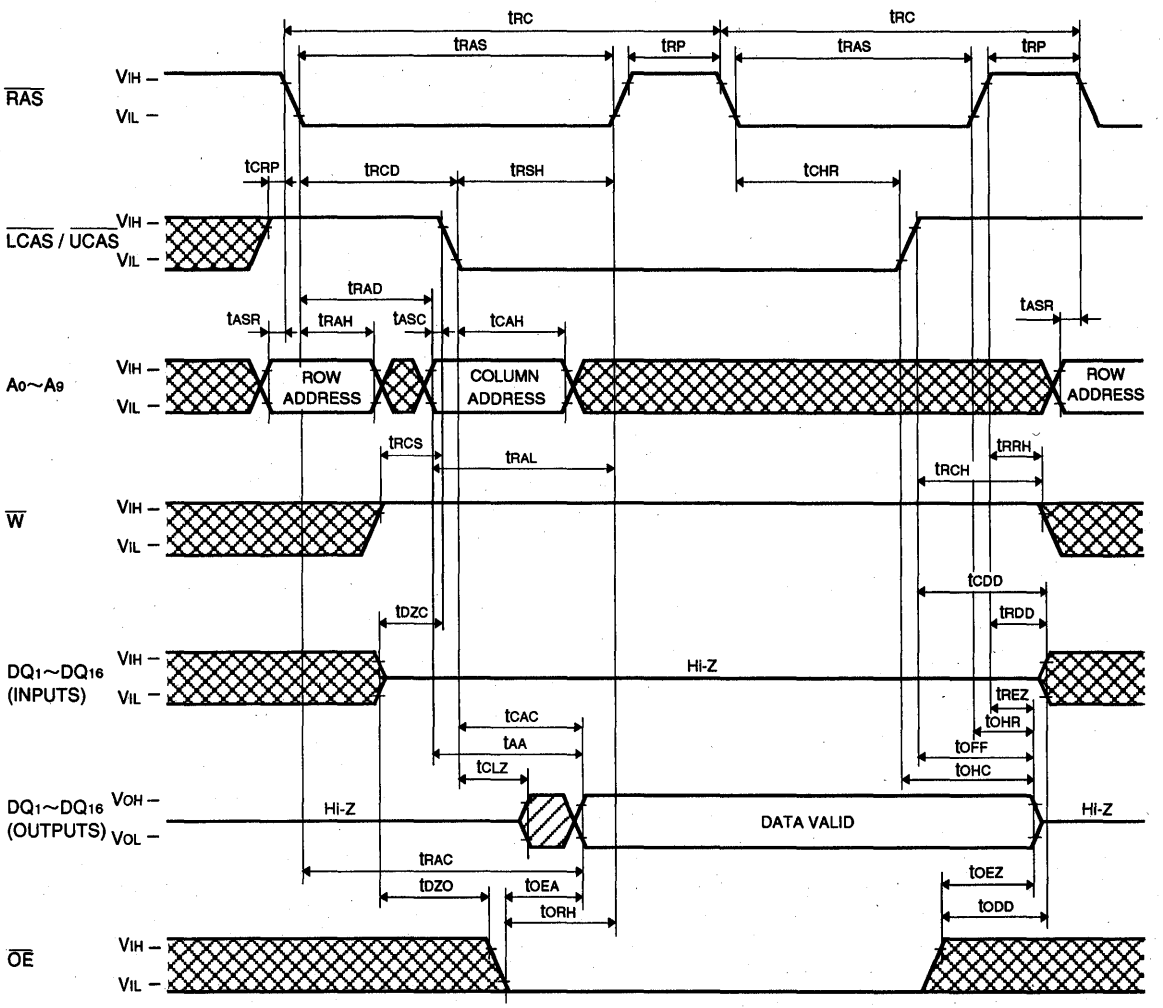
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

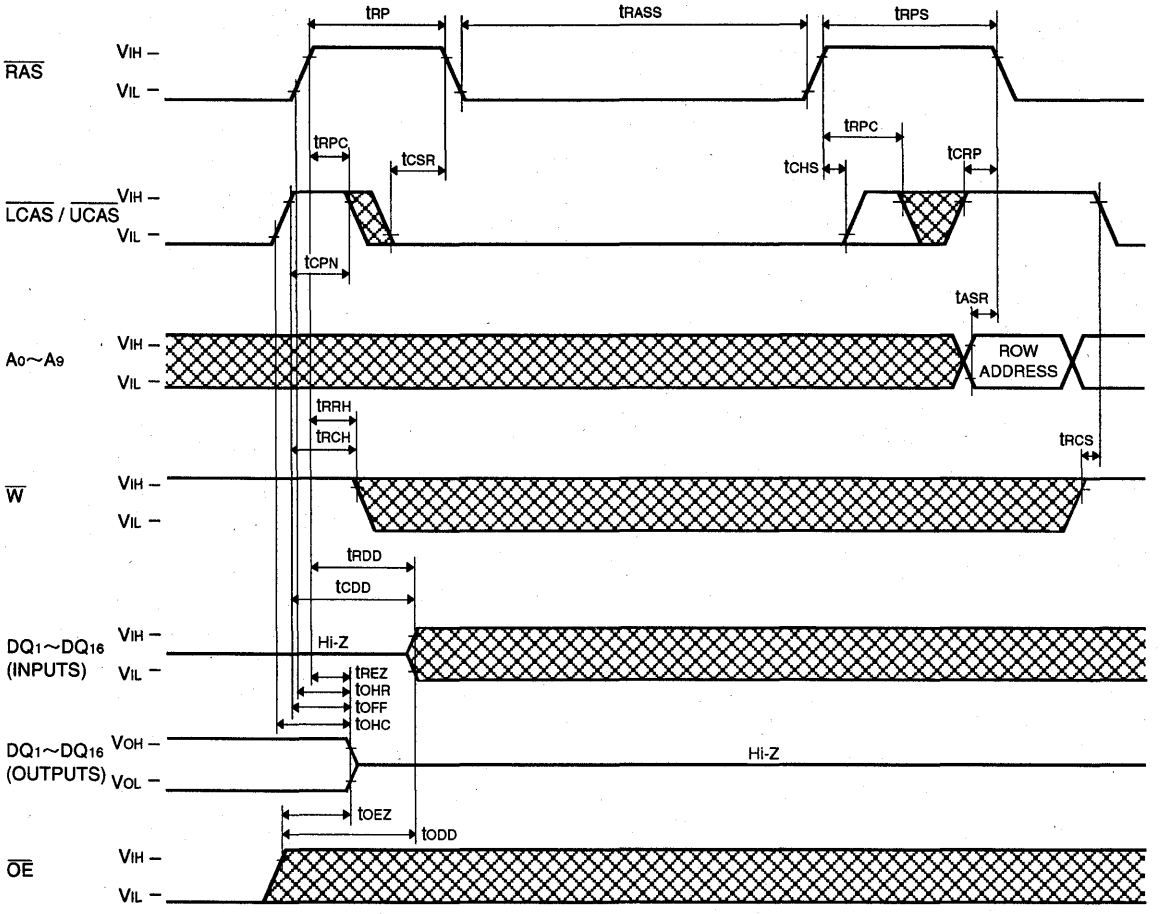


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle *



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8(AV)}$	Average supply current from Vcc Extended refresh mode	M5M4V18165B (S)	$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_9≦0.2V or ≧Vcc-0.2V t_{REF}=128ms, output open t_{RAS}=t_{RASmin}~1 μs			300	μA
$I_{CC9(AV)}$	Average supply current from Vcc Self-refresh cycle	M5M4V18165B (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

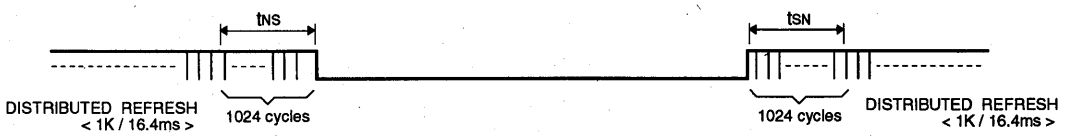
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M4V18165B-6S		M5M4V18165B-7S		
		Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

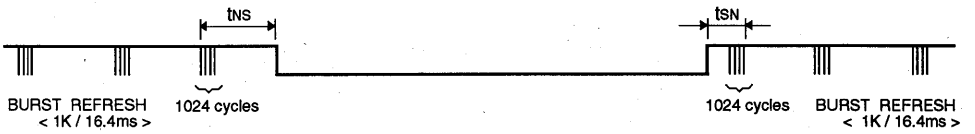
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦16.4ms and t_{SN}≦16.4ms.



(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} +t_{SN}≦16.4ms.



PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16160CTP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

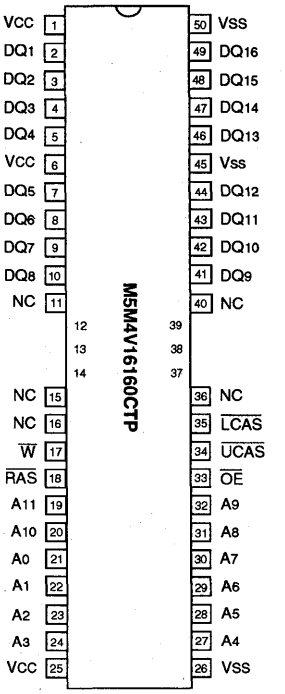
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16160CTP-5,-5S	50	13	25	13	90	360
M5M4V16160CTP-6,-6S	60	15	30	15	110	285
M5M4V16160CTP-7,-7S	70	20	35	20	130	255

- Standard 50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ----------CMOS Input level
- Low operating power dissipation
  M5M4V16160CTP-5,-5S ----------435.0mW (Max)
  M5M4V16160CTP-6,-6S ----------345.0mW (Max)
  M5M4V16160CTP-7,-7S ----------310.0mW (Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~ A_{11})
  * : Applicable to self refresh version (M5M4V16160CTP-5S,-6S, -7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

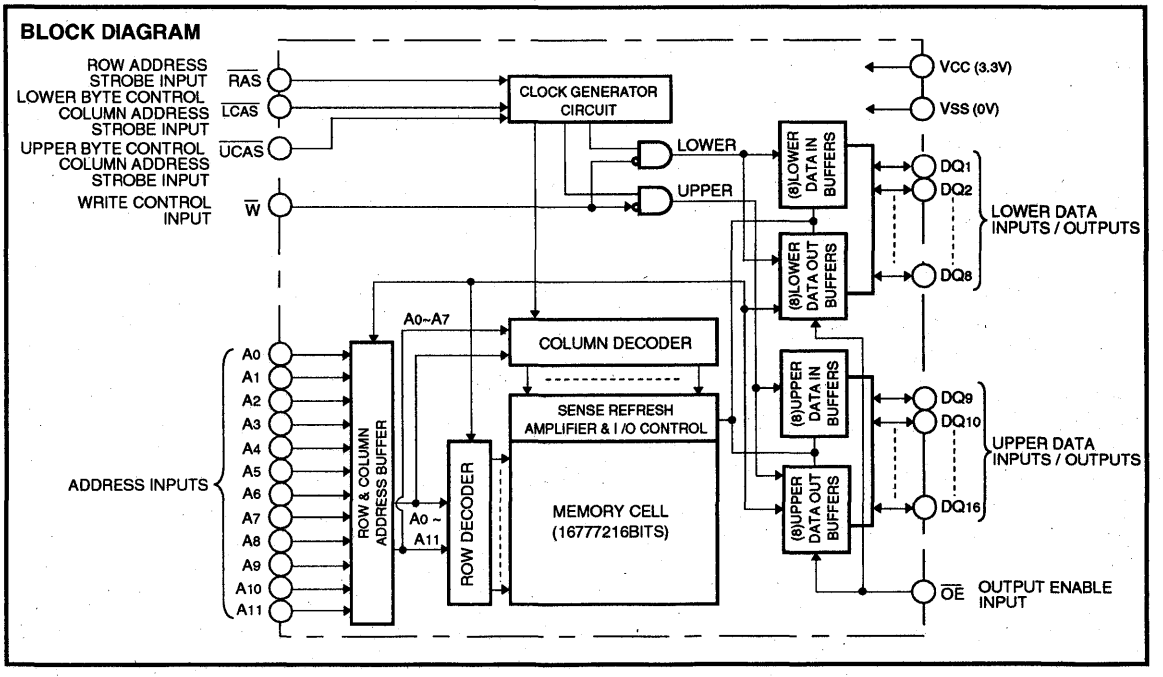
The M5M4V16160CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M4V16160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M4V16160C-6,-6S				95	
		M5M4V16160C-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}-0.2V output open			0.5	
						0.15 *	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M4V16160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			120	mA
		M5M4V16160C-6,-6S				95	
		M5M4V16160C-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-page-mode (Note 3,4,5)	M5M4V16160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V16160C-6,-6S				70	
		M5M4V16160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M4V16160C-6,-6S				95	
		M5M4V16160C-7,-7S				85	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M4V16160C (S)	Stand-by: $\overline{RAS}$≧V_{CC}-0.2V $\overline{CAS}$≧V_{CC}-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧V_{CC}-0.2V $\overline{OE}$≦0.2V or ≧V_{CC}-0.2V A0~A11≦0.2V or ≧V_{CC}-0.2V DQ=open, t_{RC}=125 μs, t_{RAS}=t_{RASmin}~1 μs			400	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M4V16160C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	VI=Vss f=1MHz VI=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq | \pm 10$ μA |) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note22)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V16160C-5,-5S		M5M4V16160C-6,-6S		M5M4V16160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V16160C-5,-5S		M5M41V6160C-6,-6S		M5M4V16160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

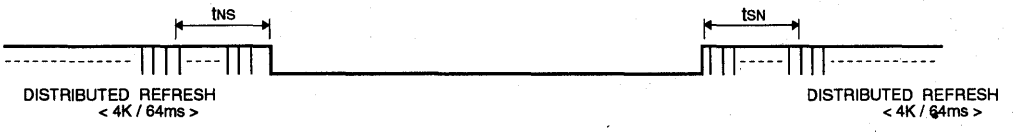
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V16160C-5S		M5M4V16160C-6S		M5M4V16160C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

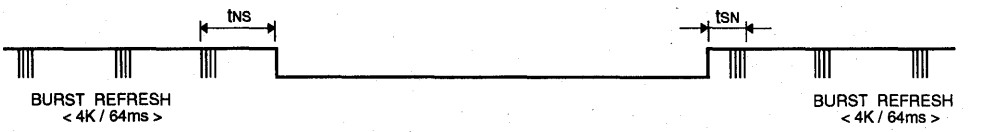
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64ms$ and $t_{SN} \leqq 64ms$.



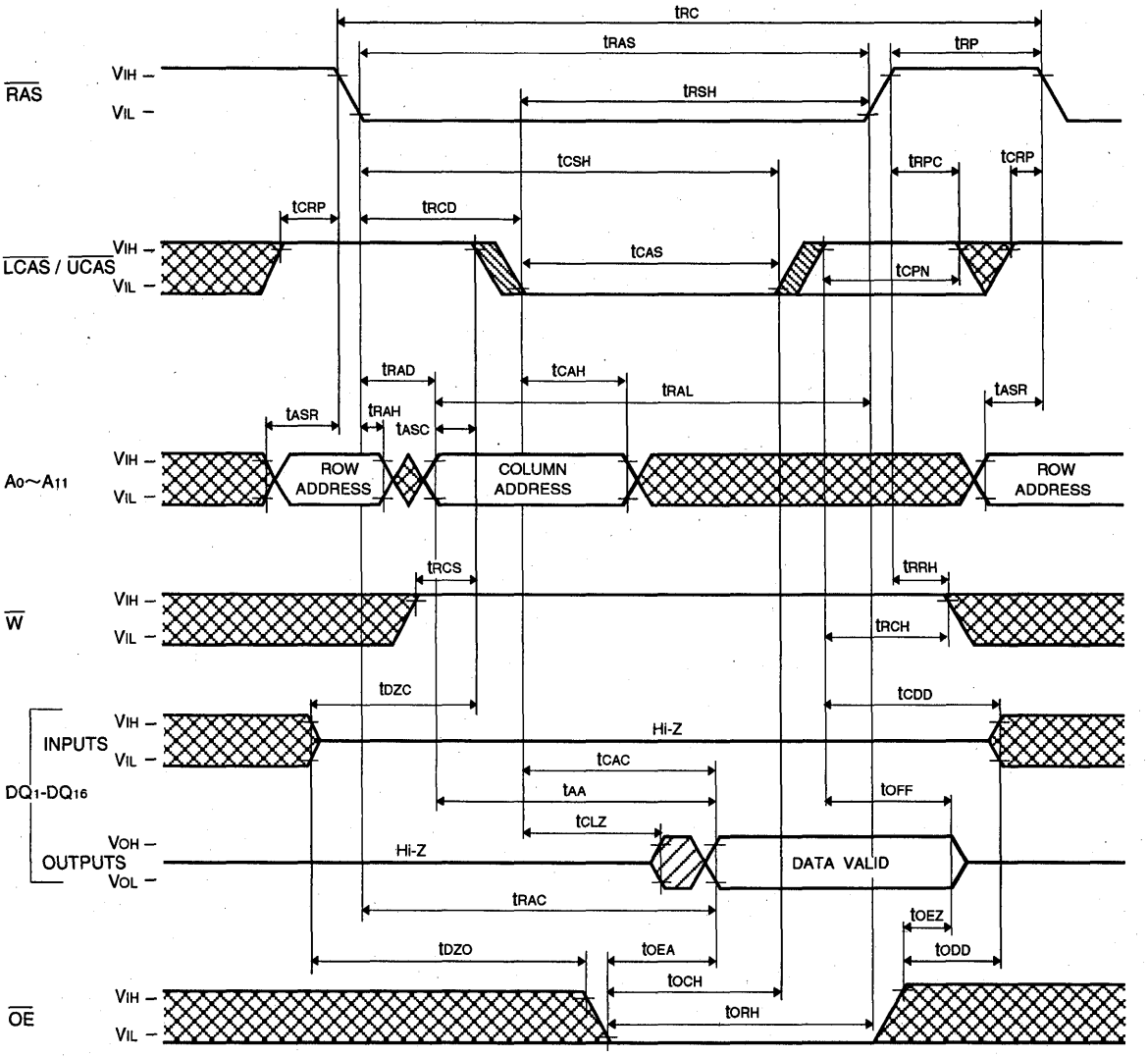
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 64ms$.



Timing Diagrams (Note 28)

Read Cycle



Note 28

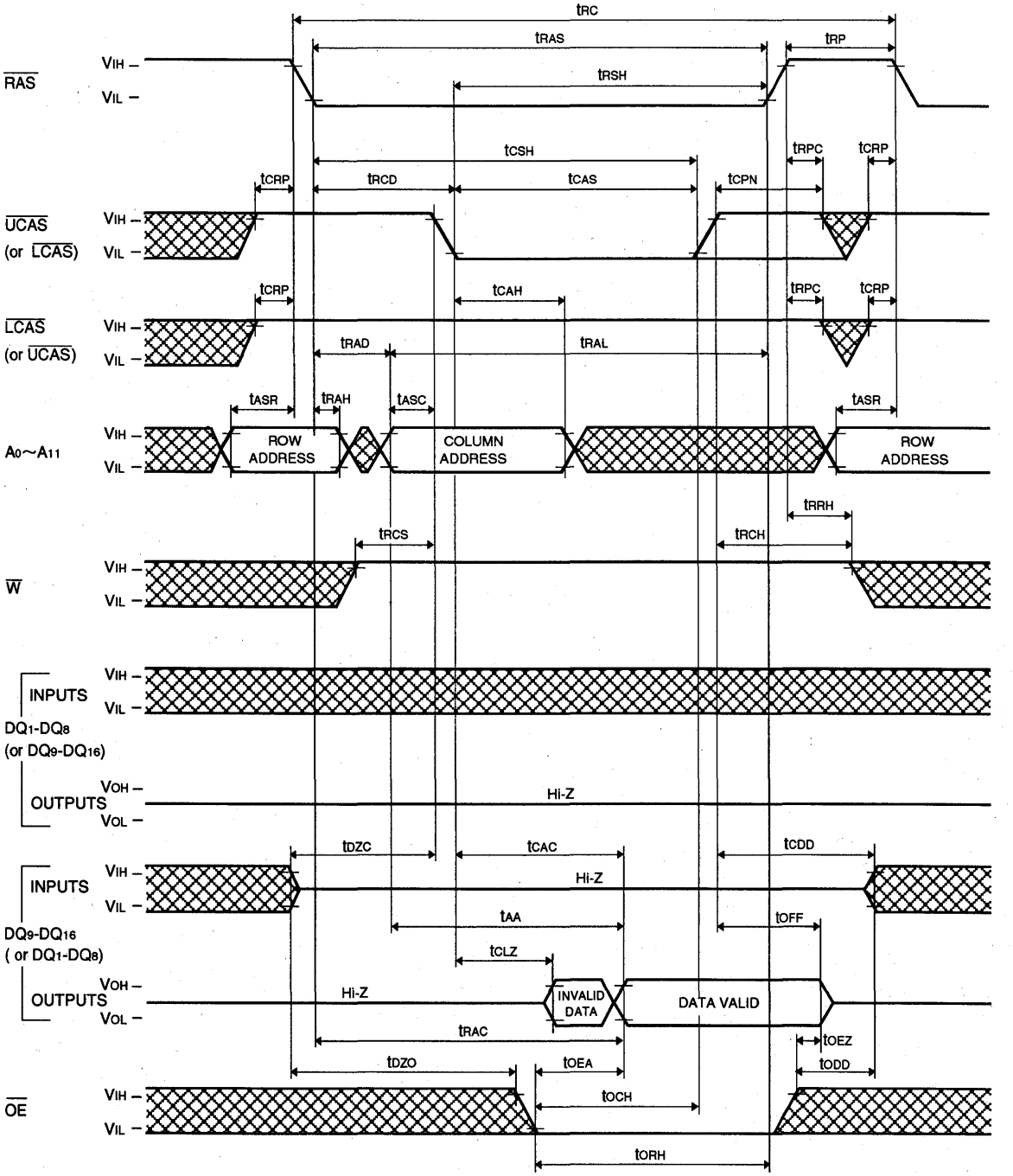
Indicates the don't care input.
VIH(min.) ≦ VIN ≦ VIH(max) or VIL(min.) ≦ VIN ≦ VIL(max)

Indicates the invalid output.

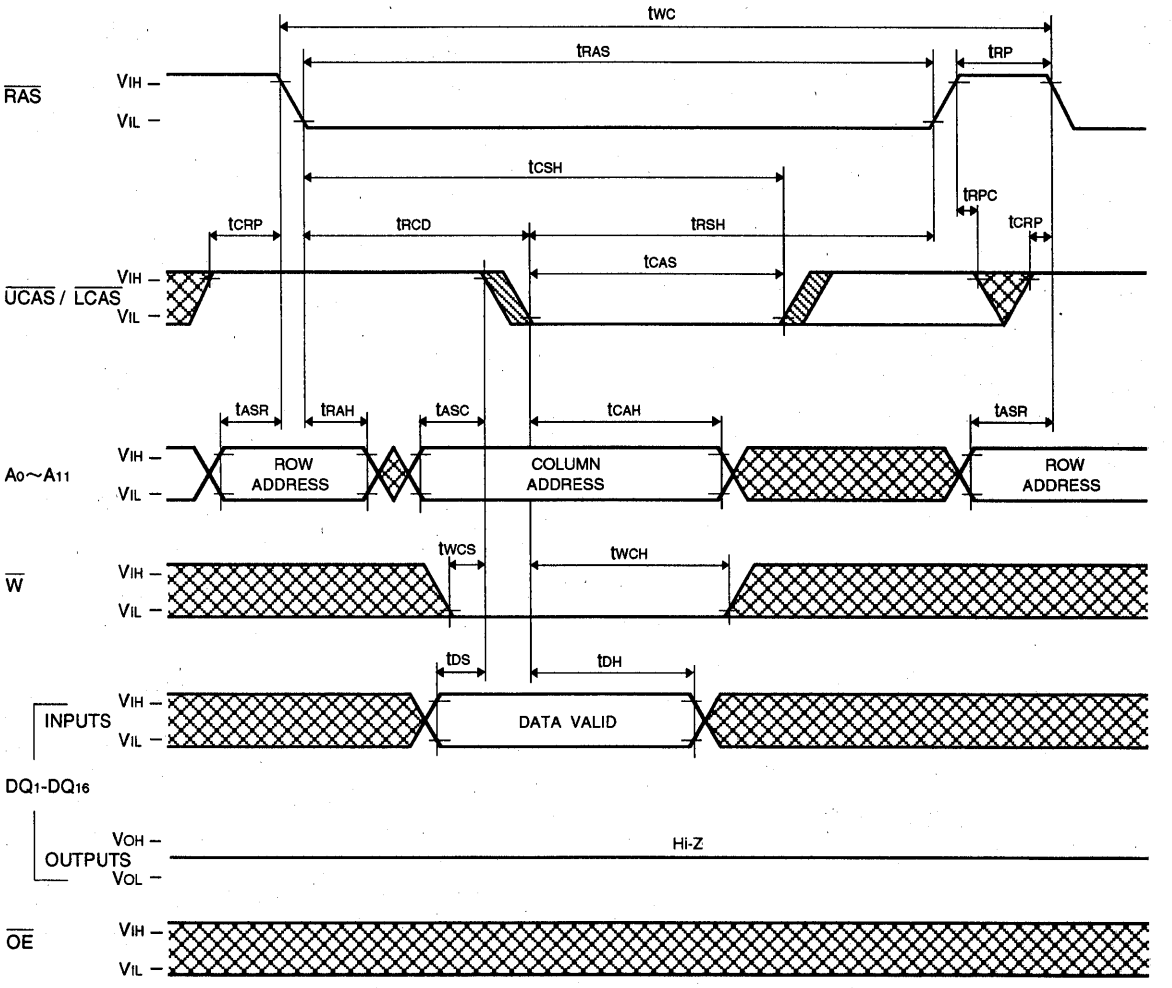
Indicates the skew of the two inputs.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Byte Read Cycle

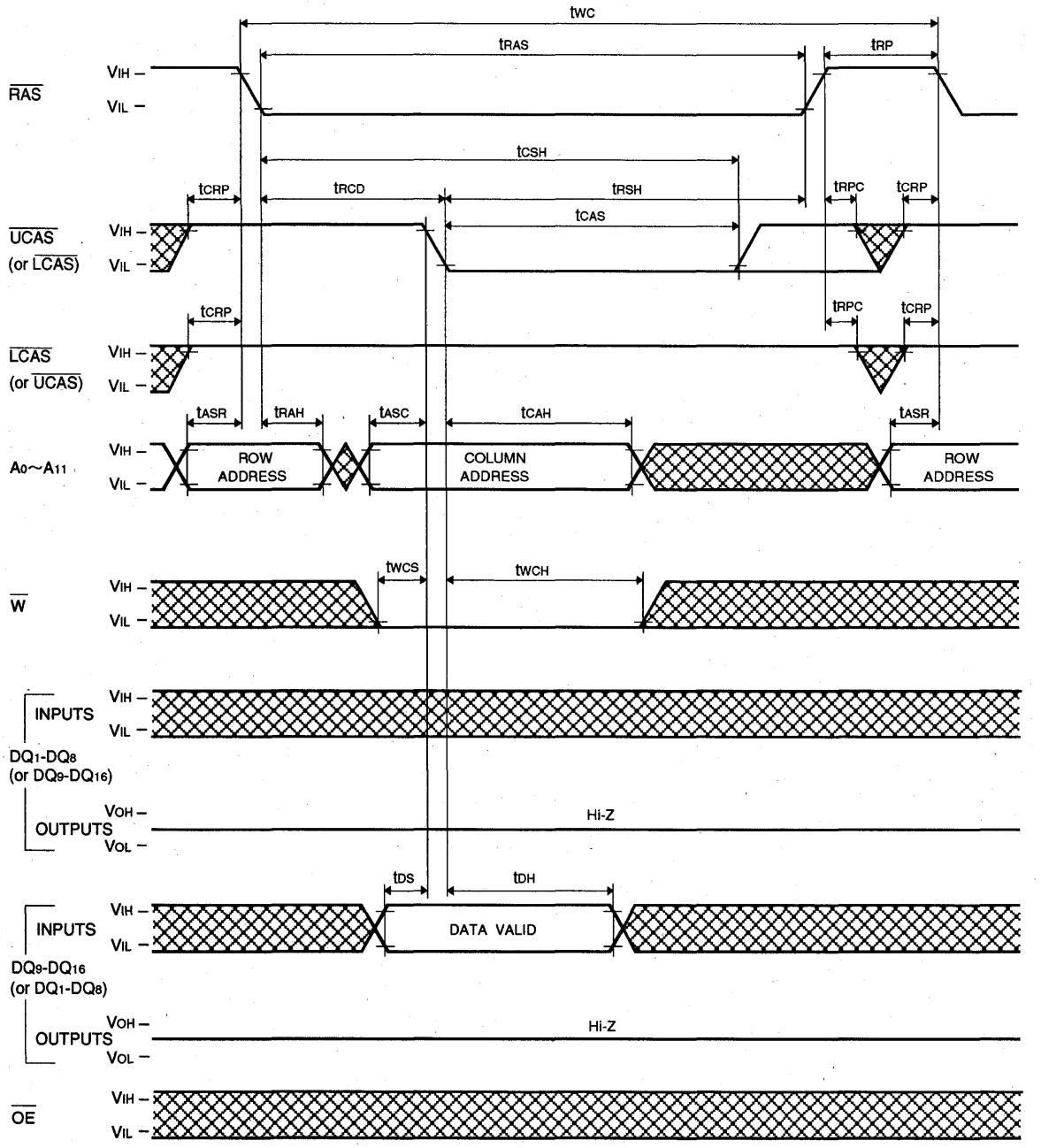


Write Cycle (Early write)



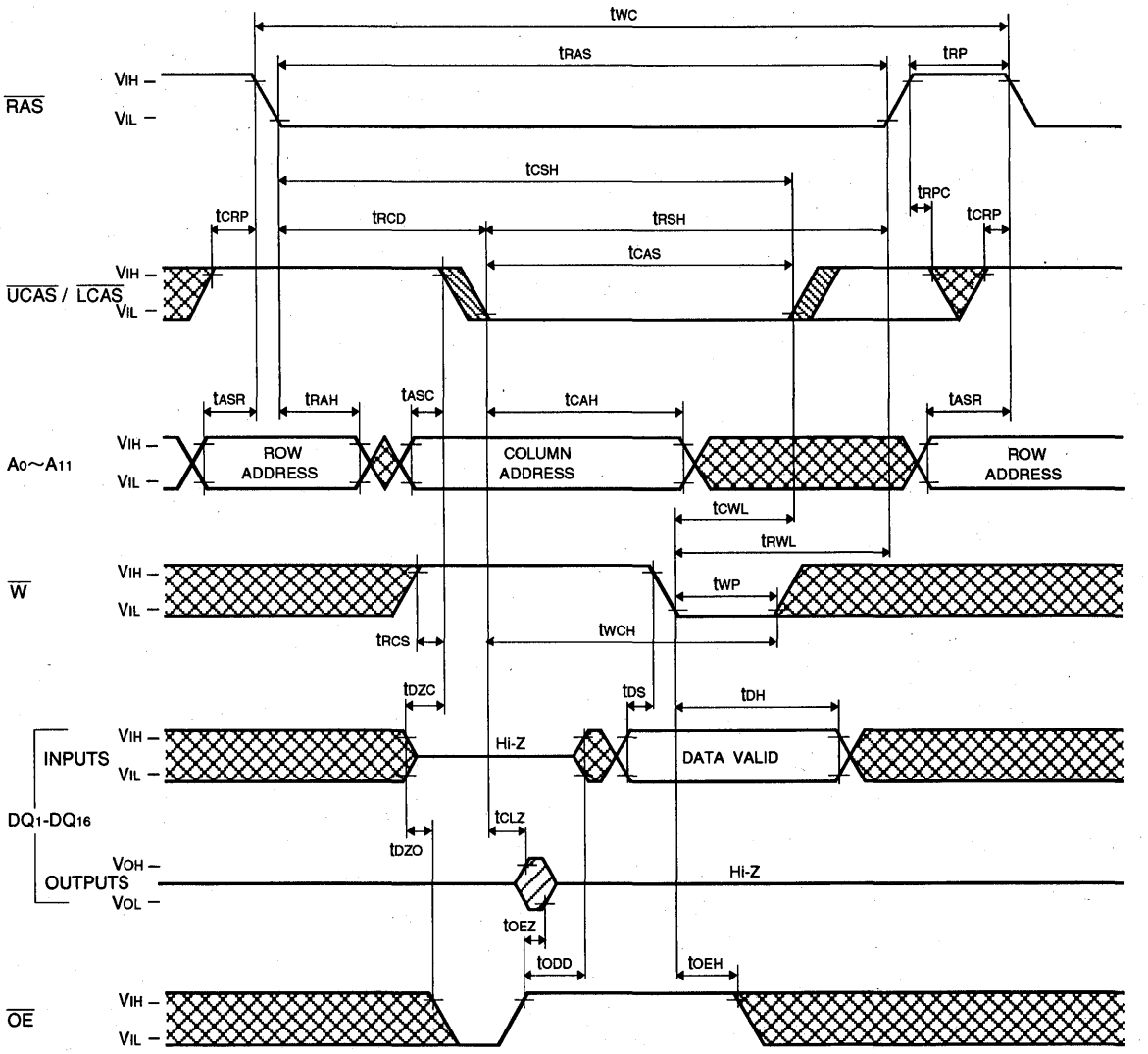
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Byte Write Cycle (Early write)



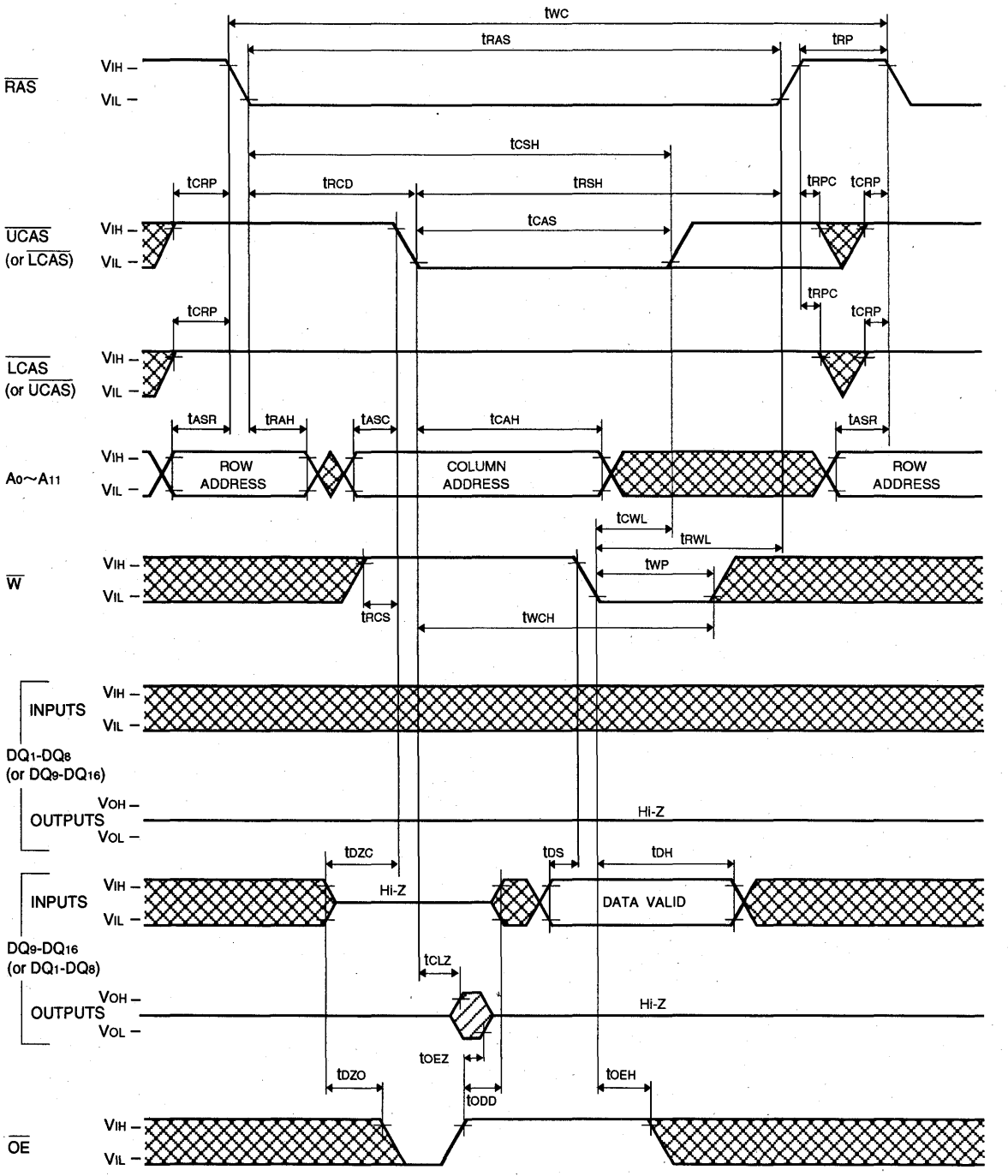
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Delayed write)

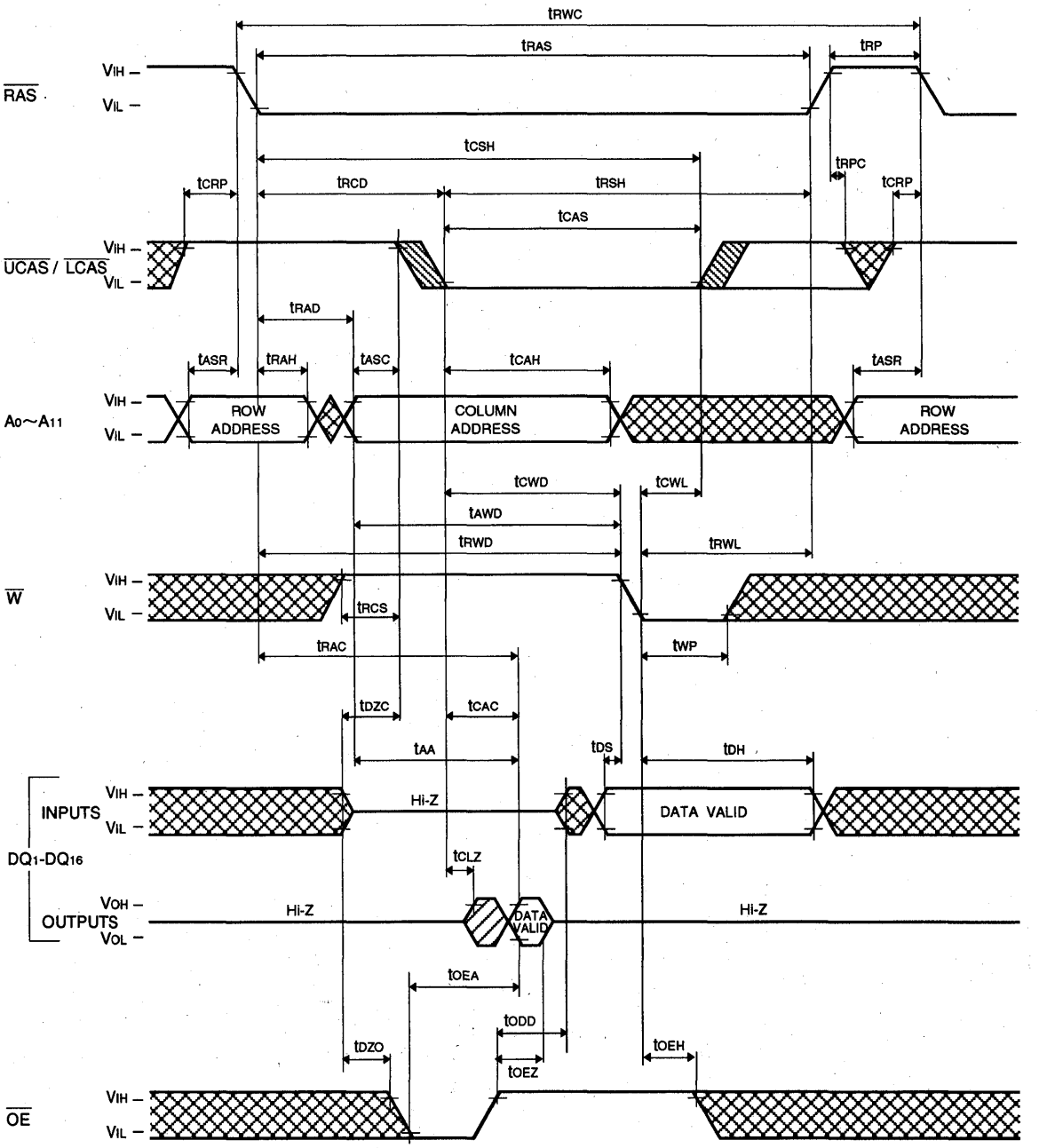


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

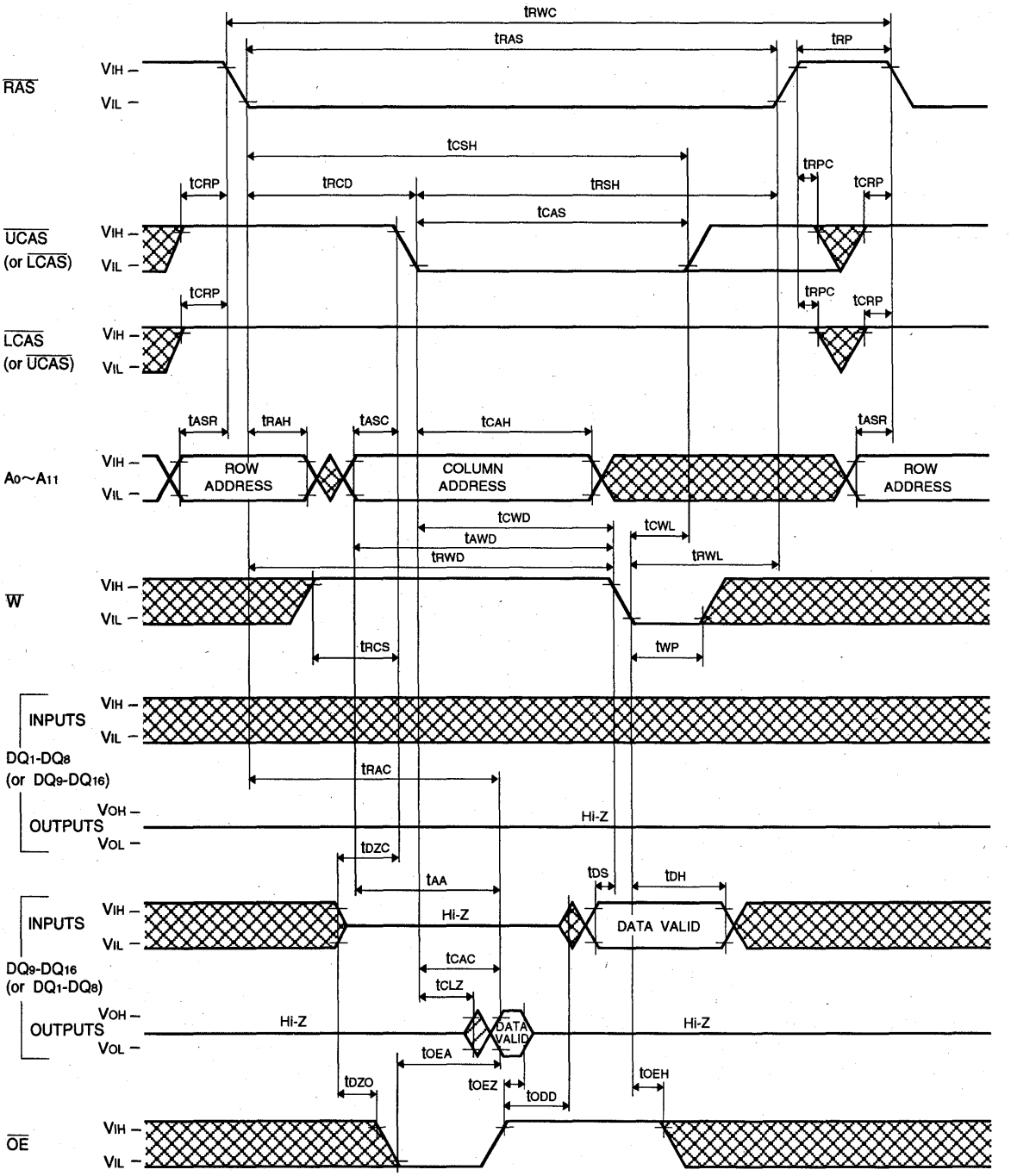
Upper / (Lower) Byte Write Cycle (Delayed write)



Read-Write, Read-Modify-Write Cycle

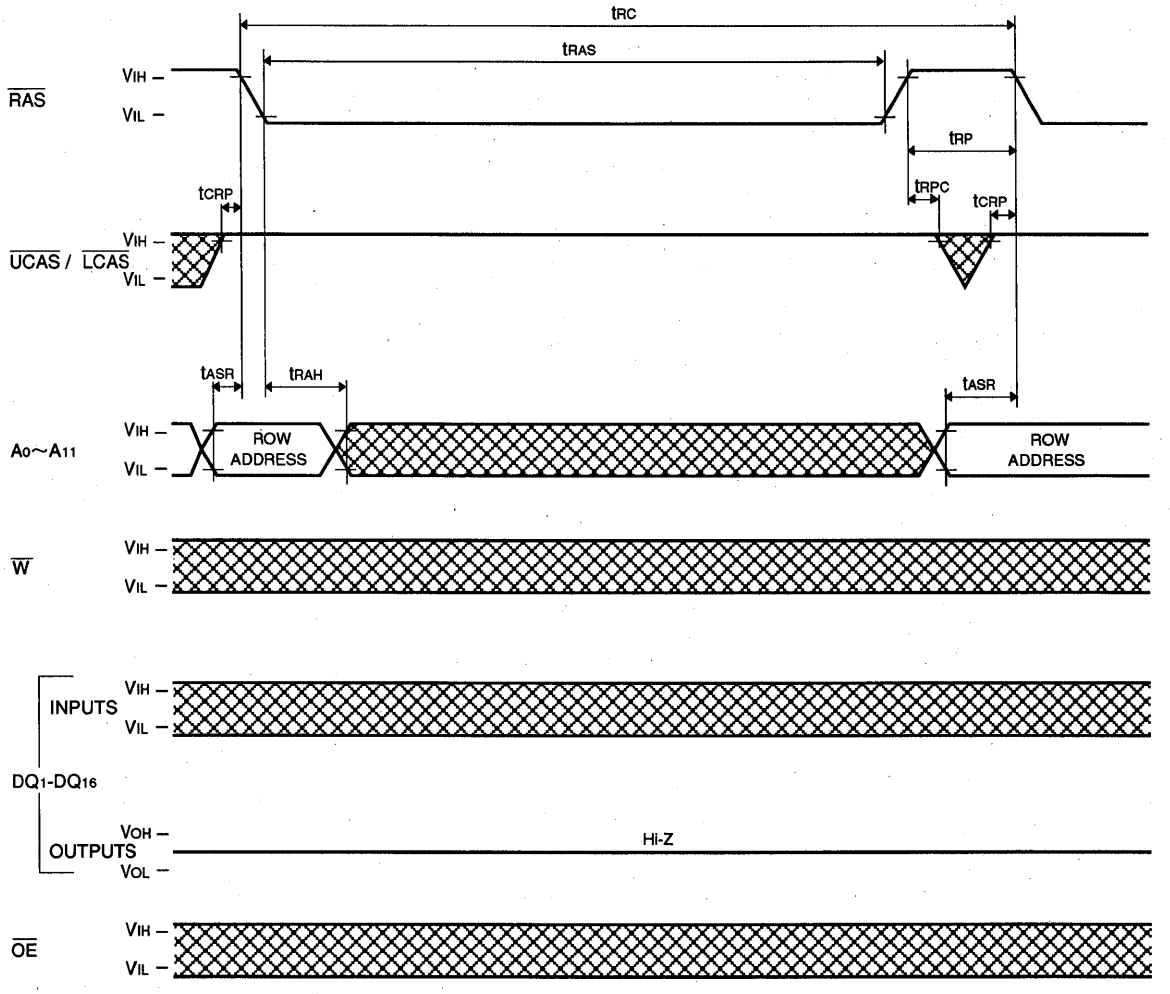


Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



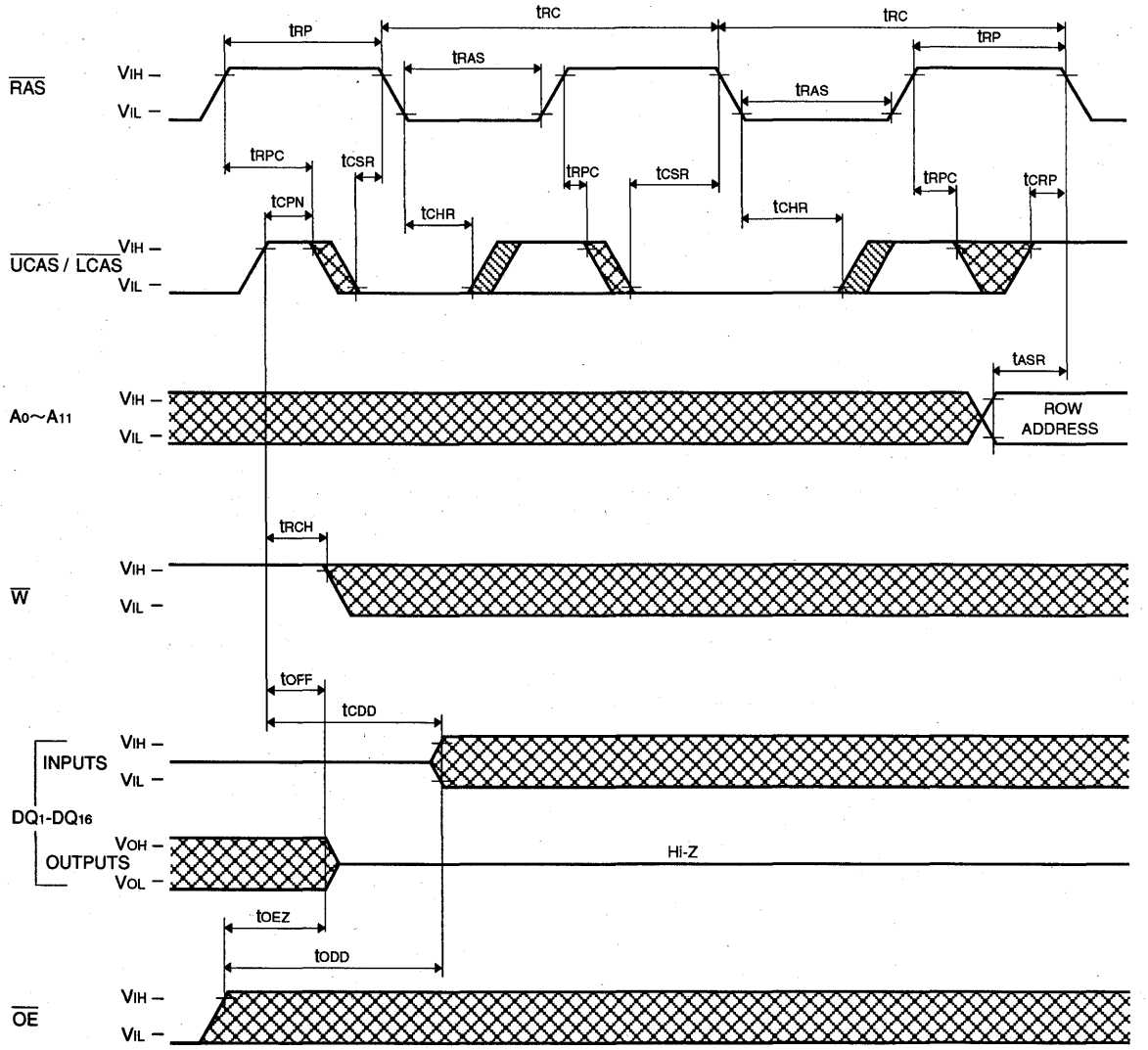
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle



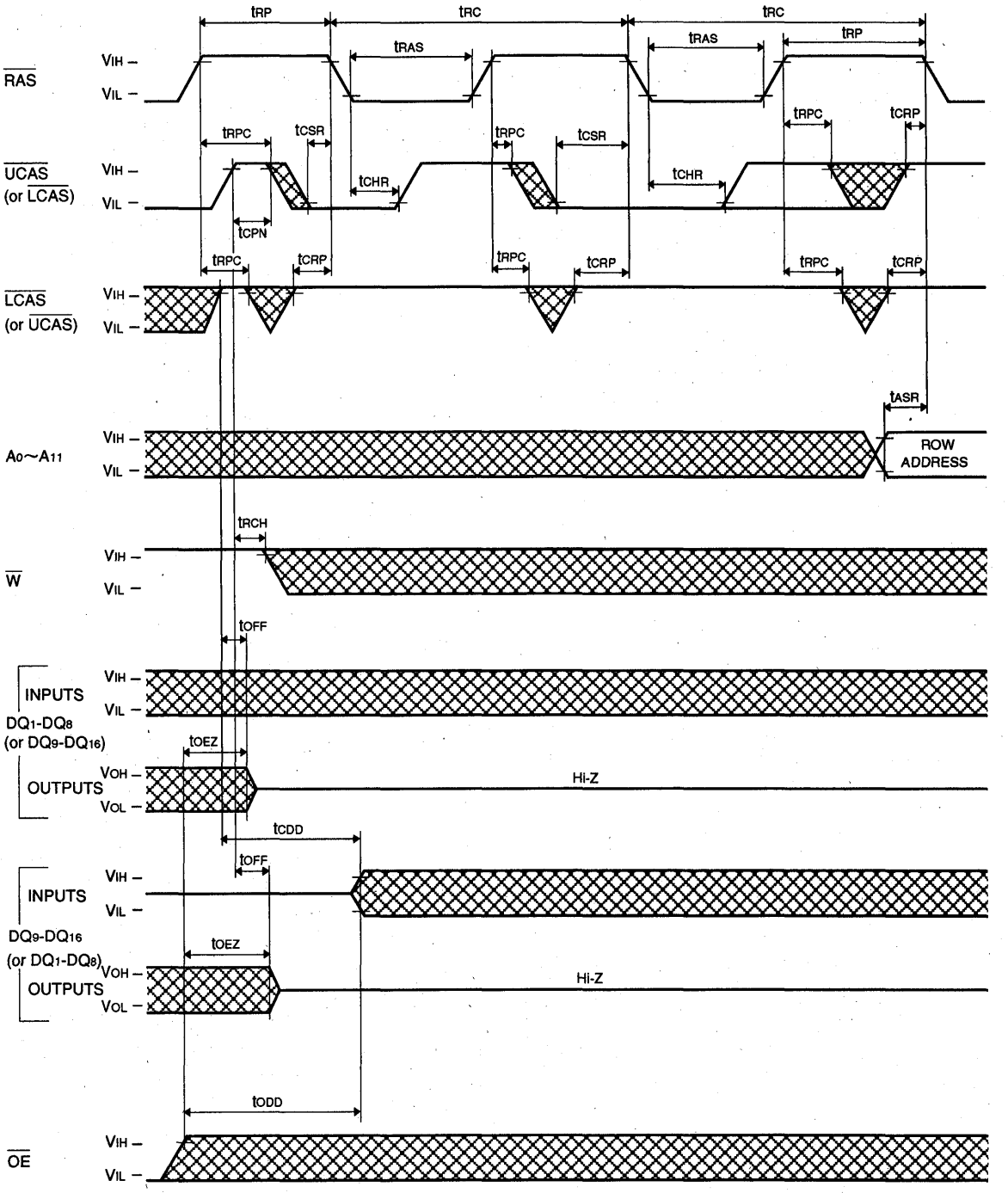
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



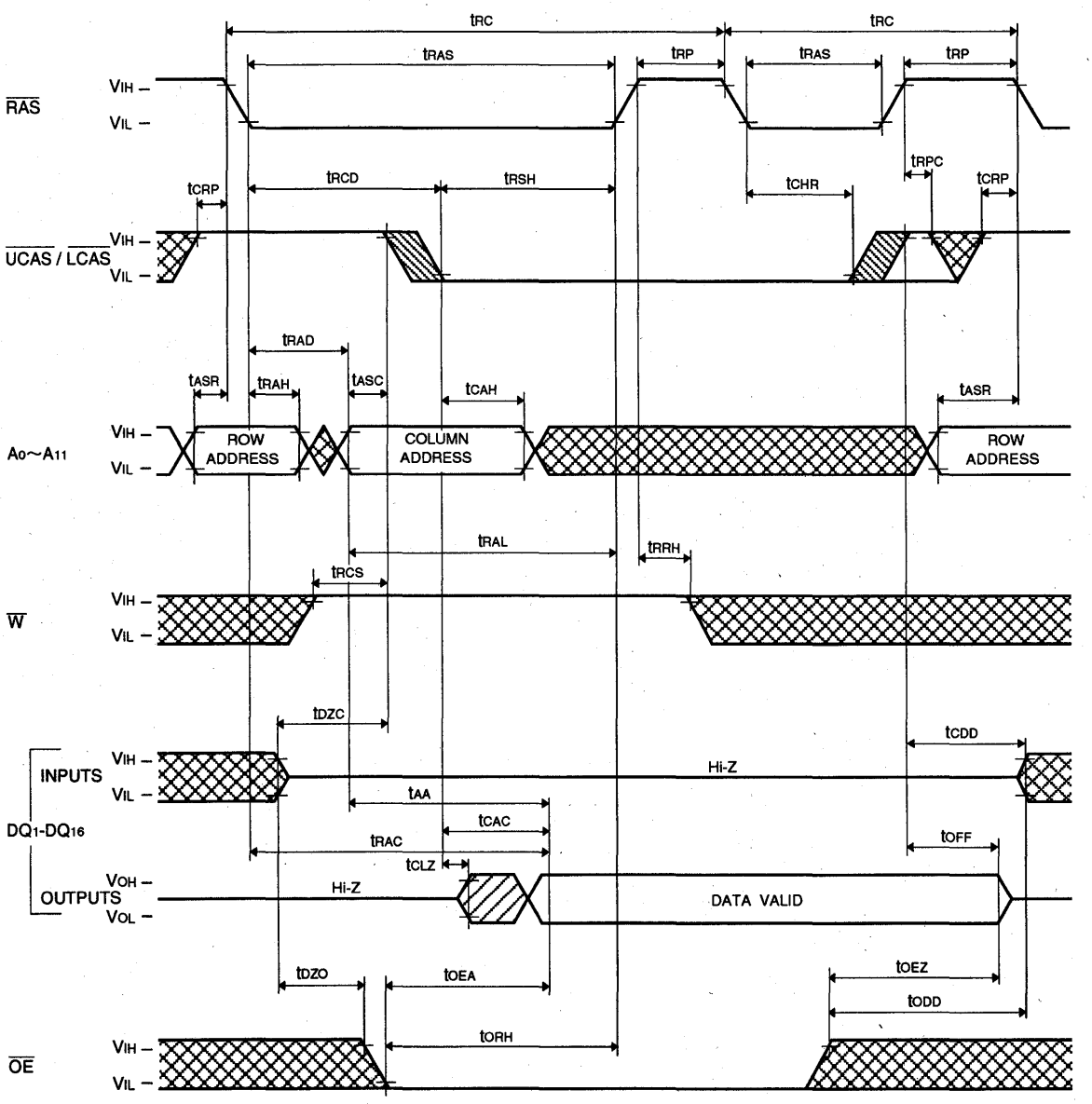
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



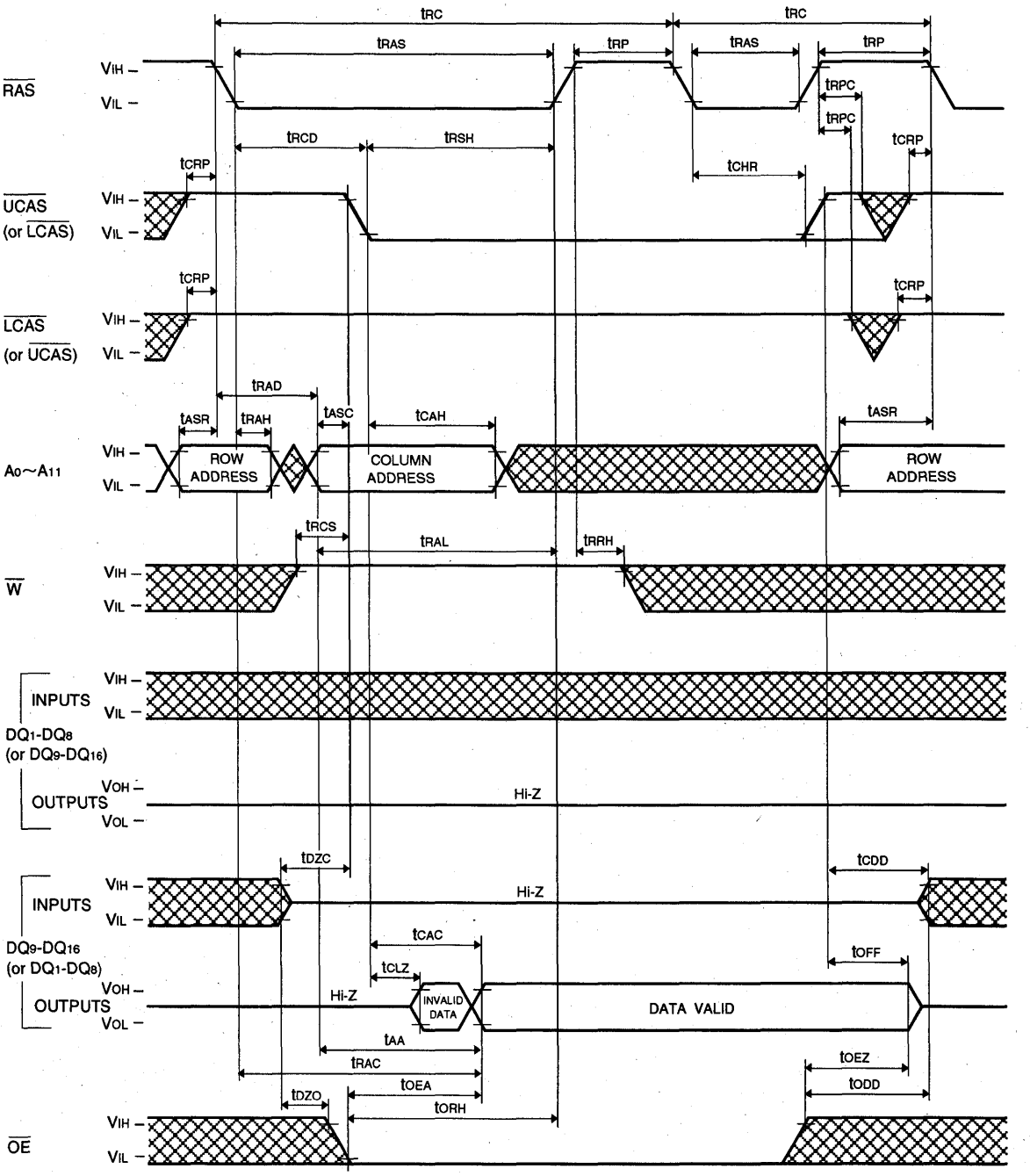
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

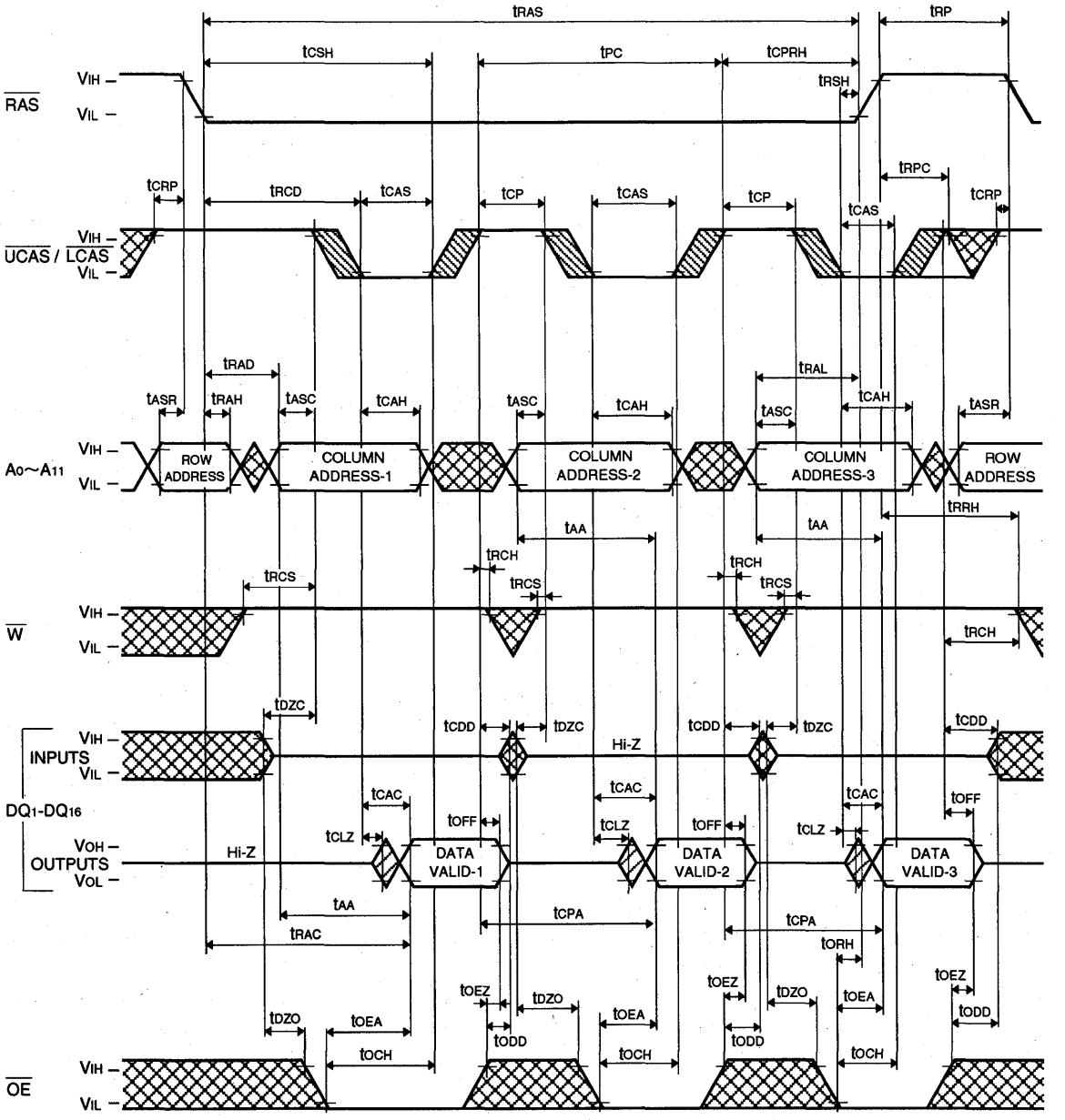
Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



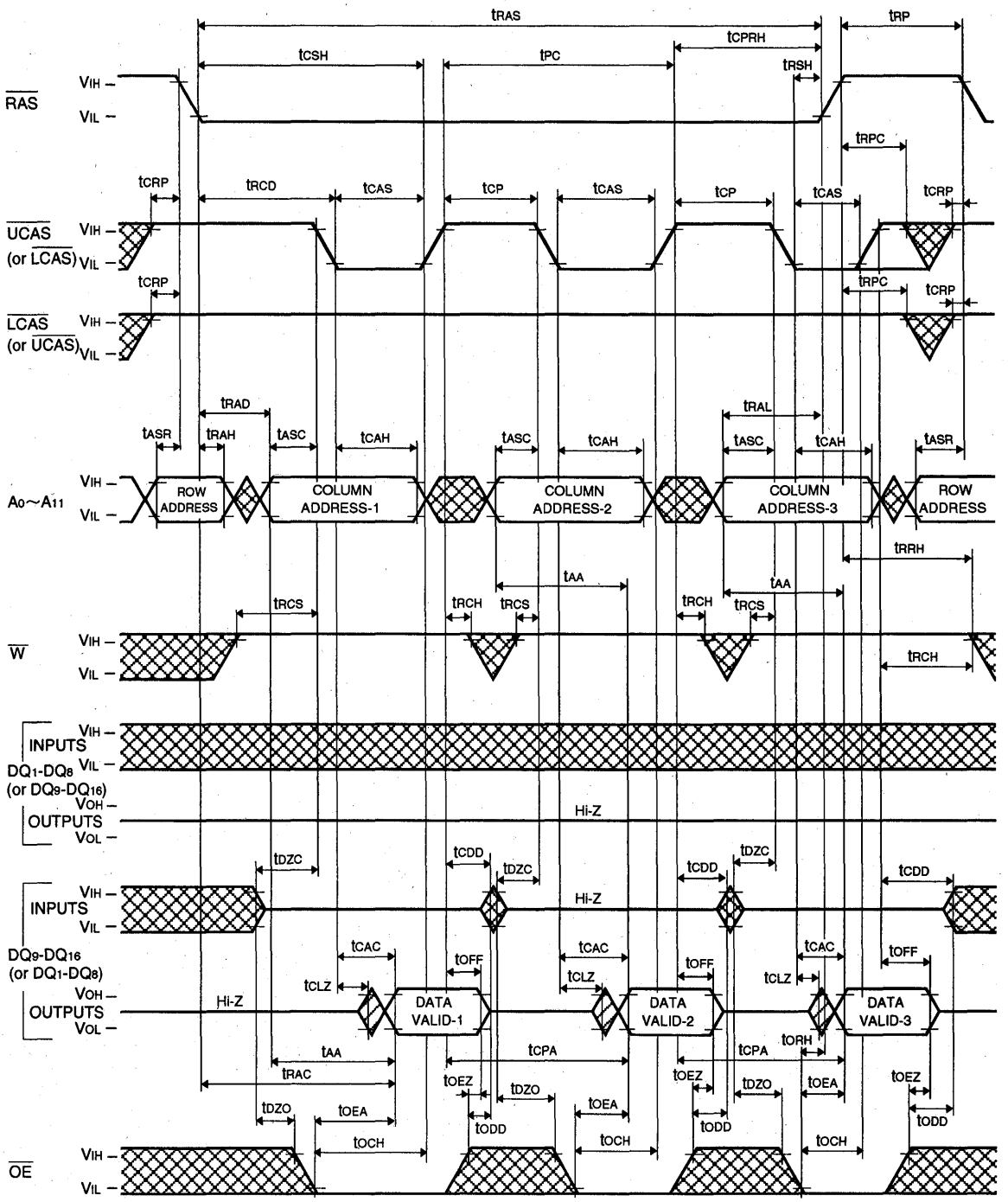
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

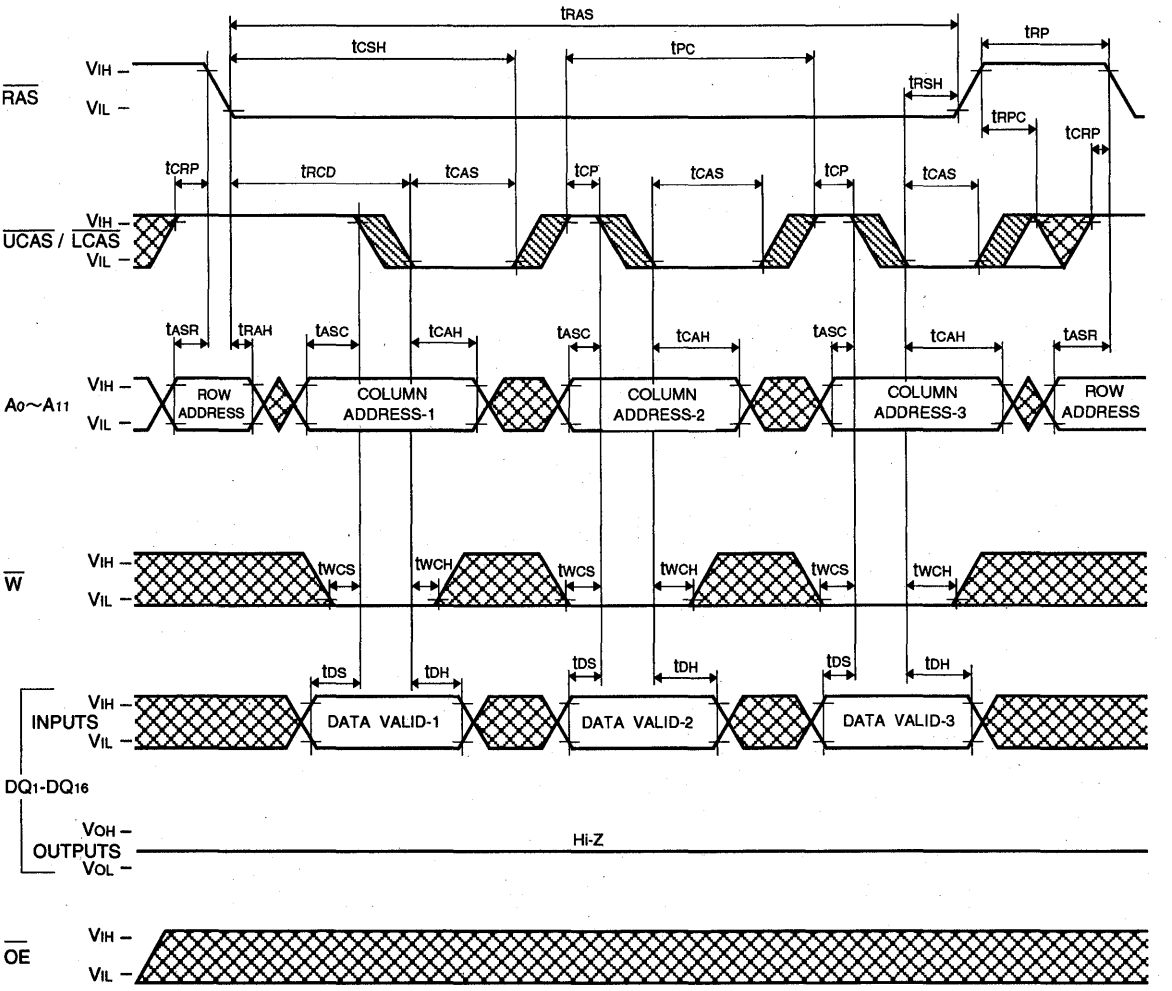
Fast Page Mode Read Cycle



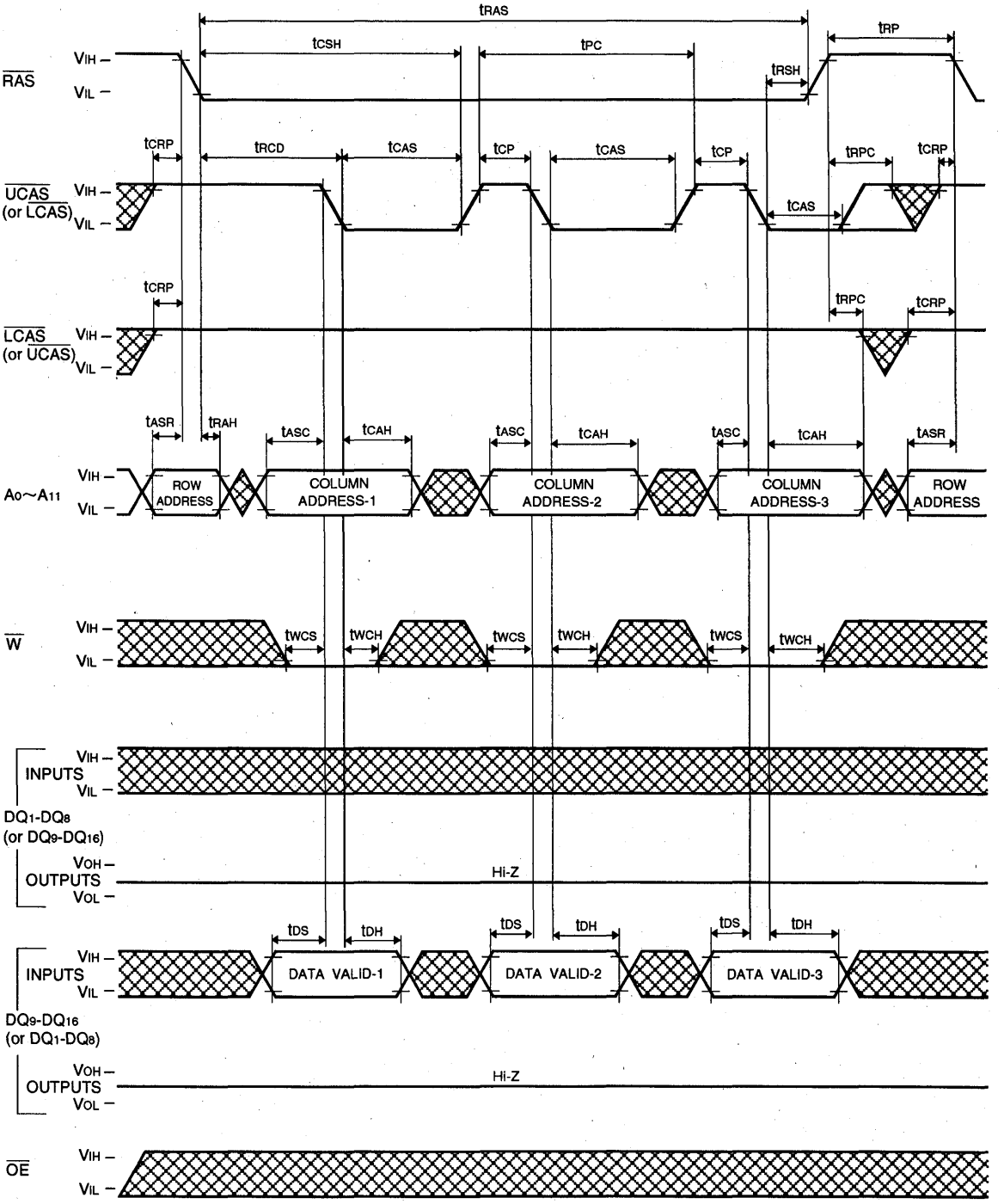
Upper / (Lower) Fast Page Mode Read Cycle



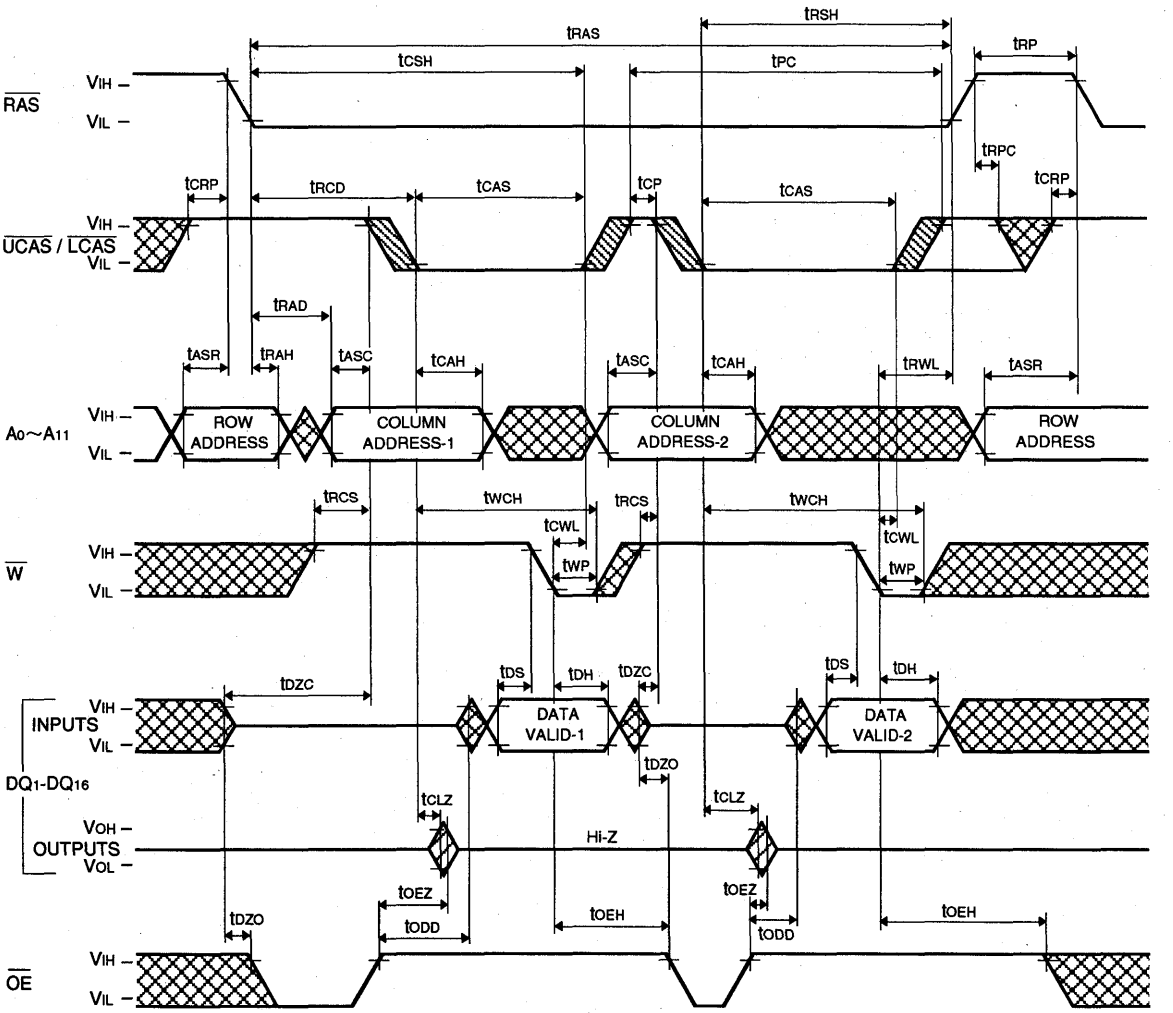
Fast Page Mode Write Cycle (Early Write)



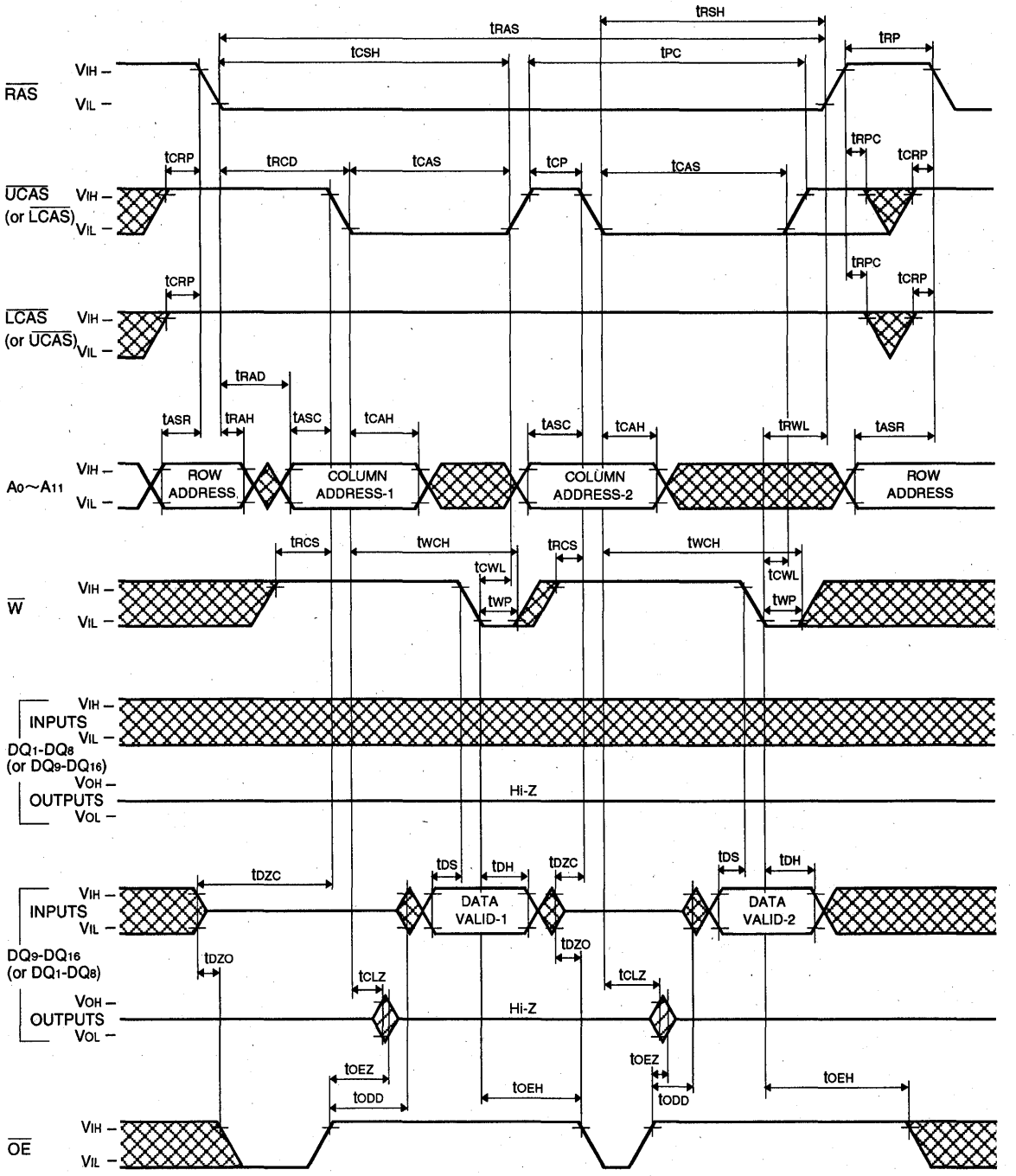
Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)



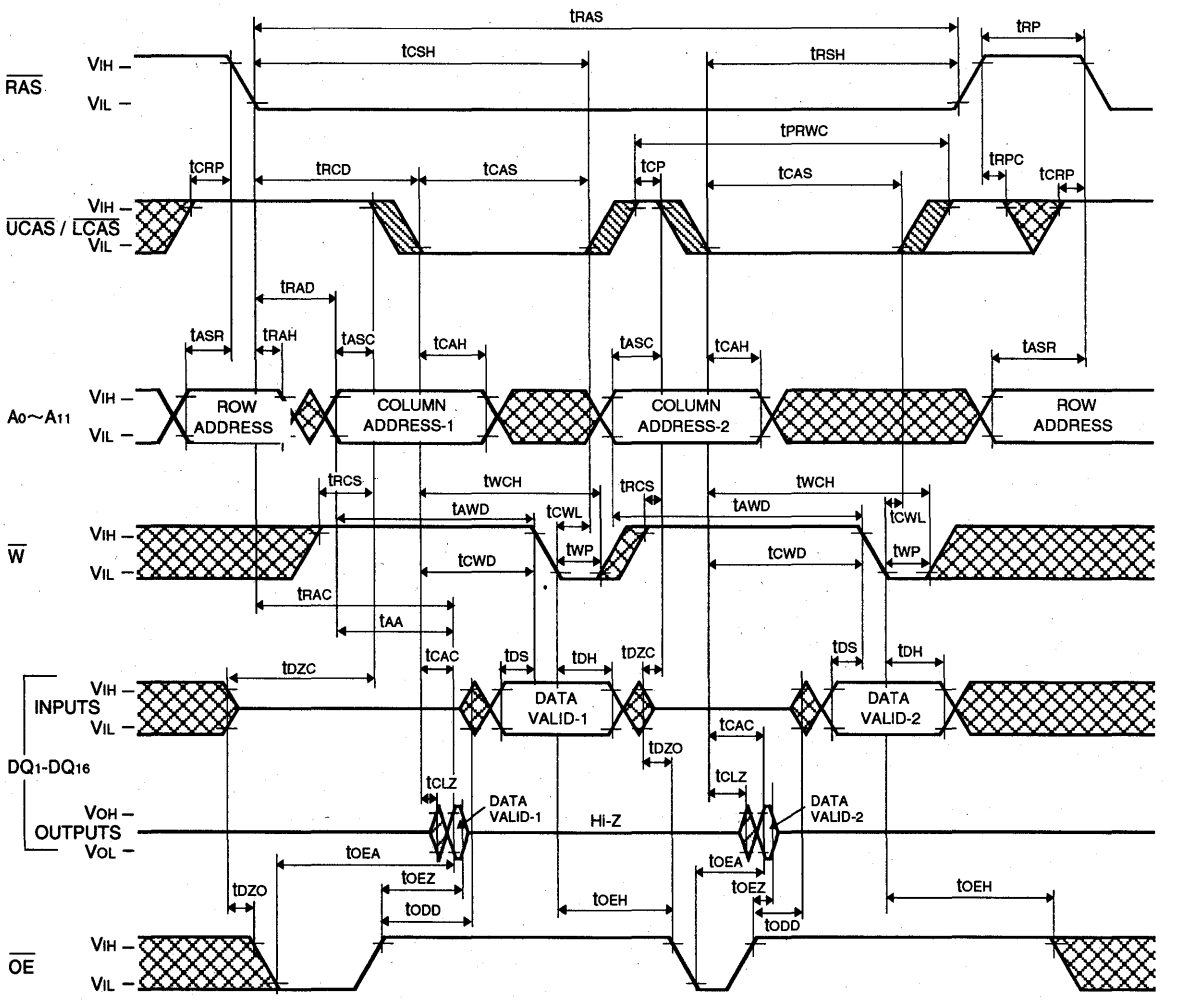
Fast Page Mode Write Cycle (Delayed Write)



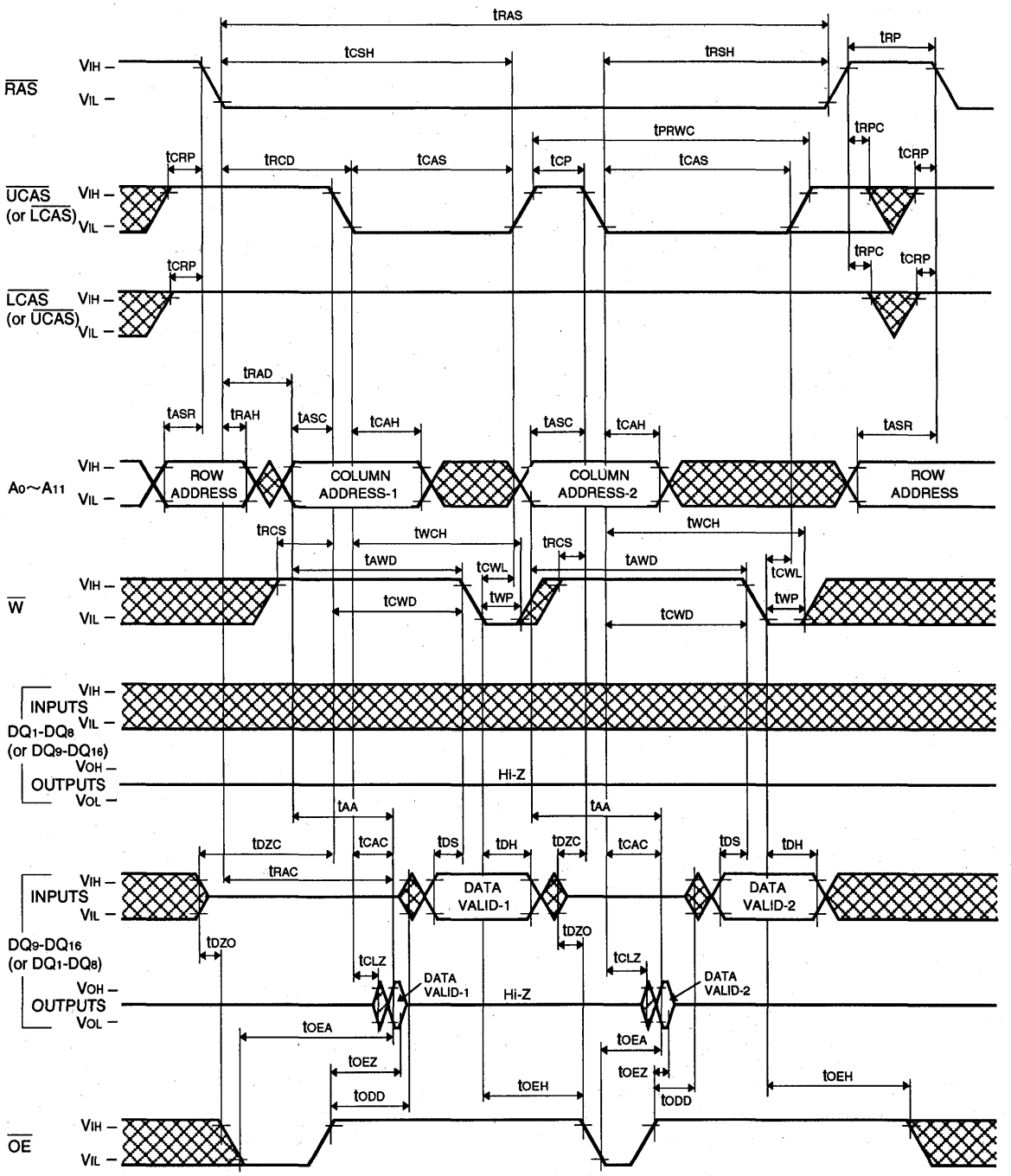
Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)



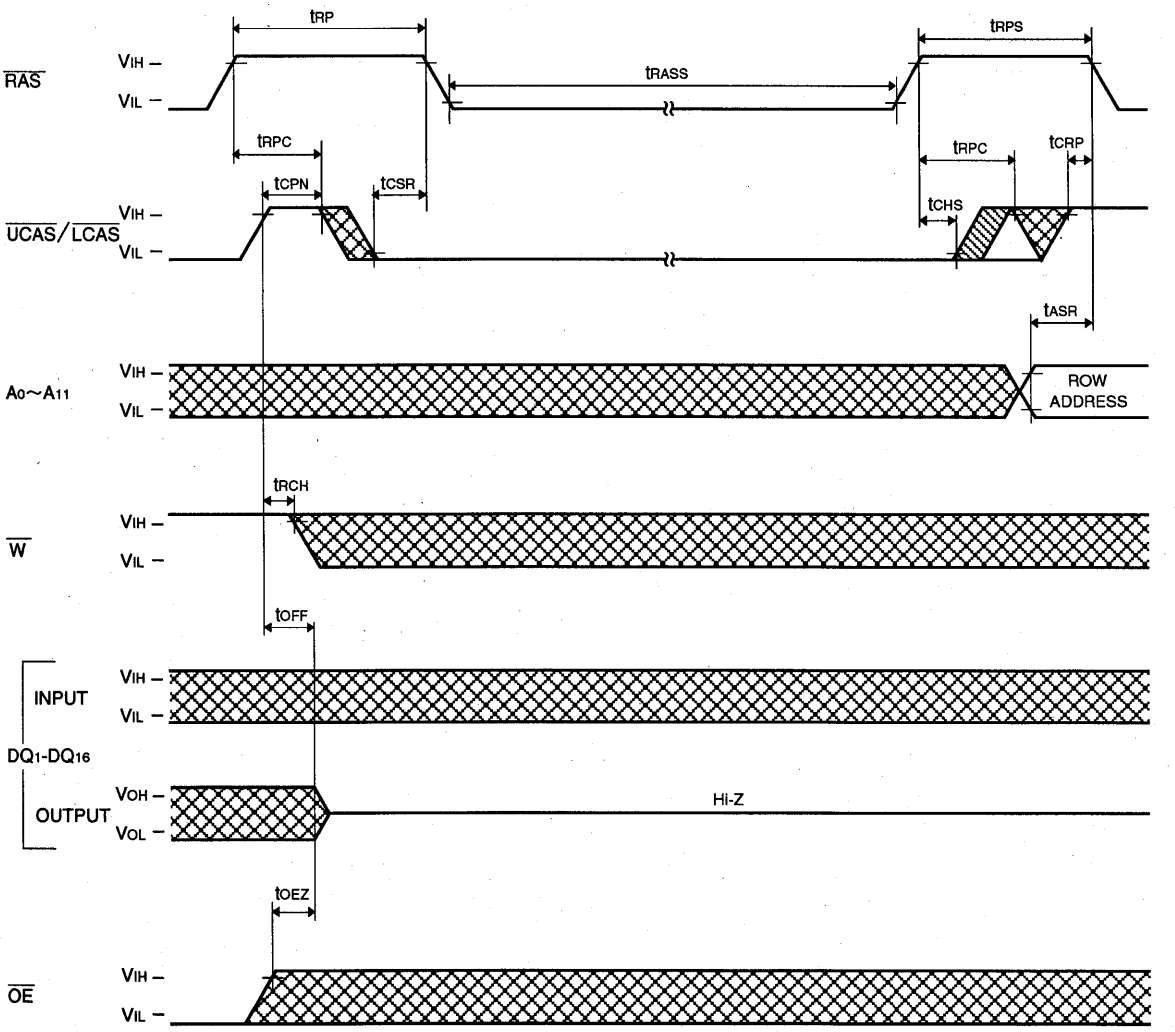
Fast Page Mode Read-Write, Read-Modify-Write Cycle



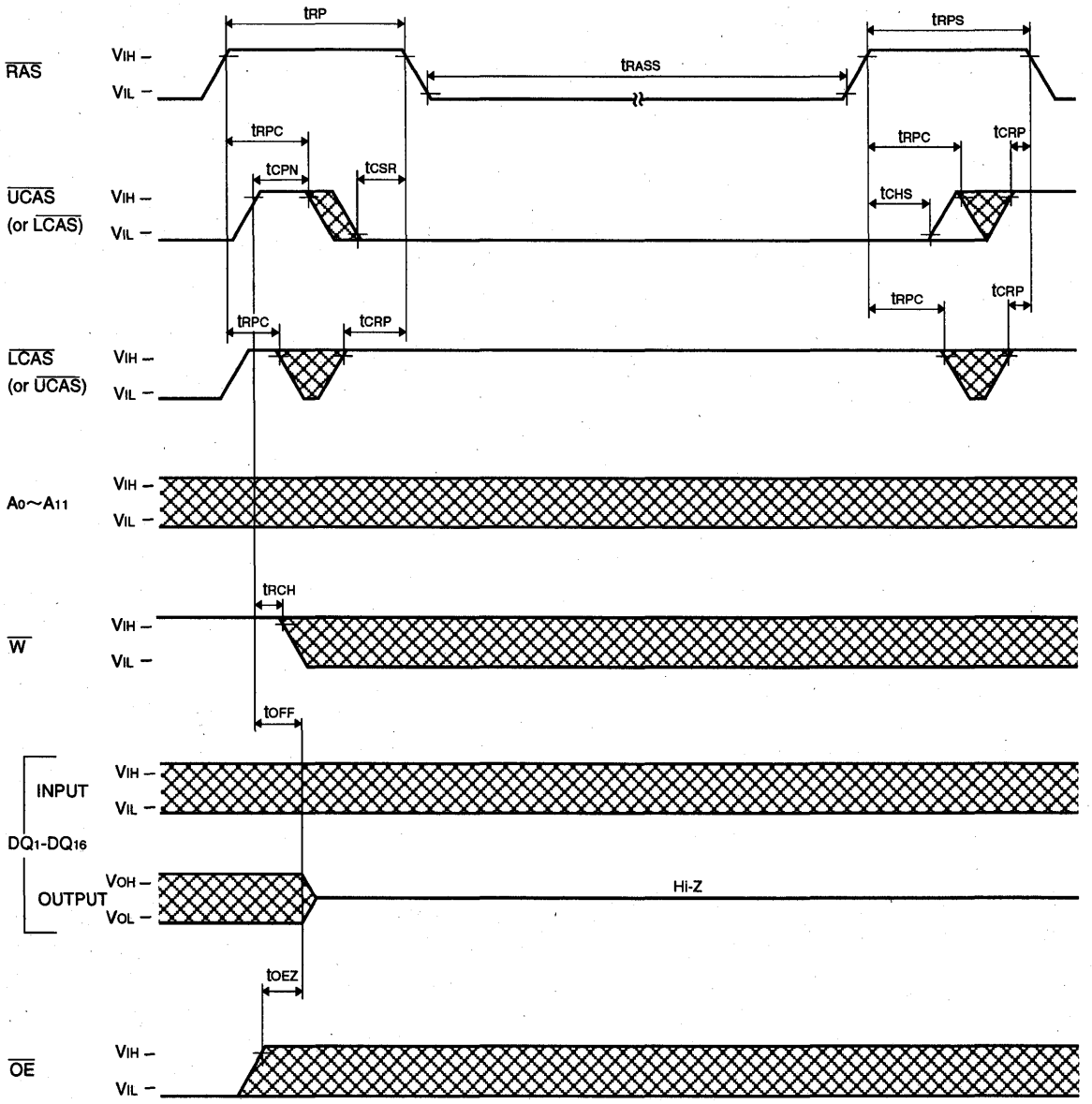
Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



Self Refresh Cycle∗



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18160CTP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

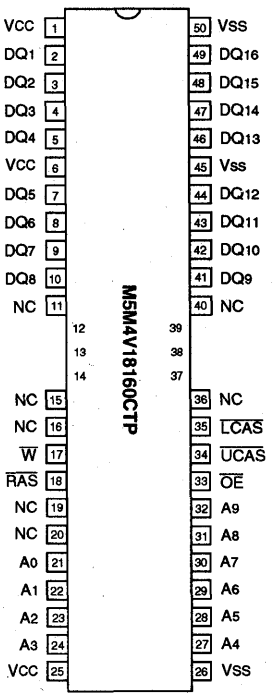
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18160CTP-5,-5S	50	13	25	13	90	540
M5M4V18160CTP-6,-6S	60	15	30	15	110	450
M5M4V18160CTP-7,-7S	70	20	35	20	130	390

- Standard 50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V18160CTP-5,-5S ---------- 650.0mW (Max)
  M5M4V18160CTP-6,-6S ---------- 540.0mW (Max)
  M5M4V18160CTP-7,-7S ---------- 470.0mW (Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  * : Applicable to self refresh version (M5M4V18160CTP-5S,-6S, -7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

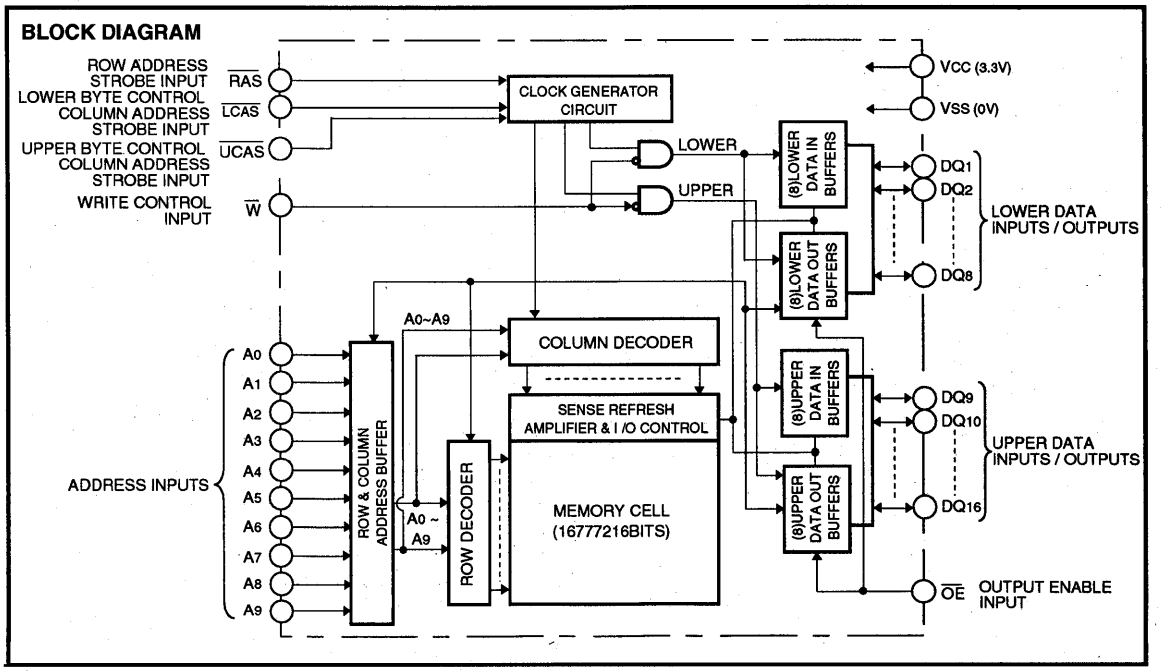
The M5M4V18160CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M4V18160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧V_{CC} -0.2V output open			0.5	
						0.15 *	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M4V18160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-page-mode (Note 3,4,5)	M5M4V18160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V18160C-6,-6S				70	
		M5M4V18160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M4V18160C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0~A9≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125 μs, t_{RAS}=t_{RAS}min.~1 μs			300	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M4V18160C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ\,(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq | \pm 10\ \mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

18: Either tDZC or tDZO must be satisfied.

19: Either tCDD or tODD must be satisfied.

20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		13		15		20		ns
tWP	Write pulse width		8		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 25)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

CAS before RAS Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		10		ns
tCHR	CAS hold time after RAS low	10		10		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

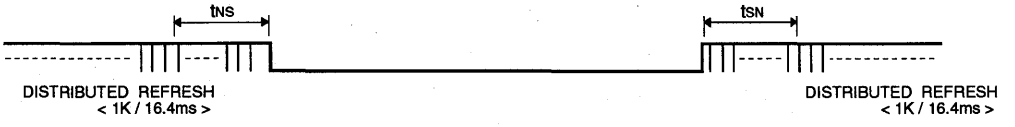
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5S		M5M4V18160C-6S		M5M4V18160C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh RAS low pulse width	100		100		100		μs
tRPS	Self refresh RAS high precharge time	90		110		130		ns
tCHS	Self refresh RAS hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

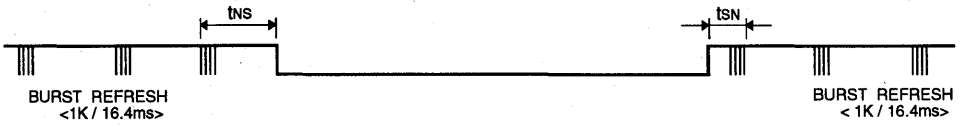
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦16.4ms and tSN≦16.4ms.



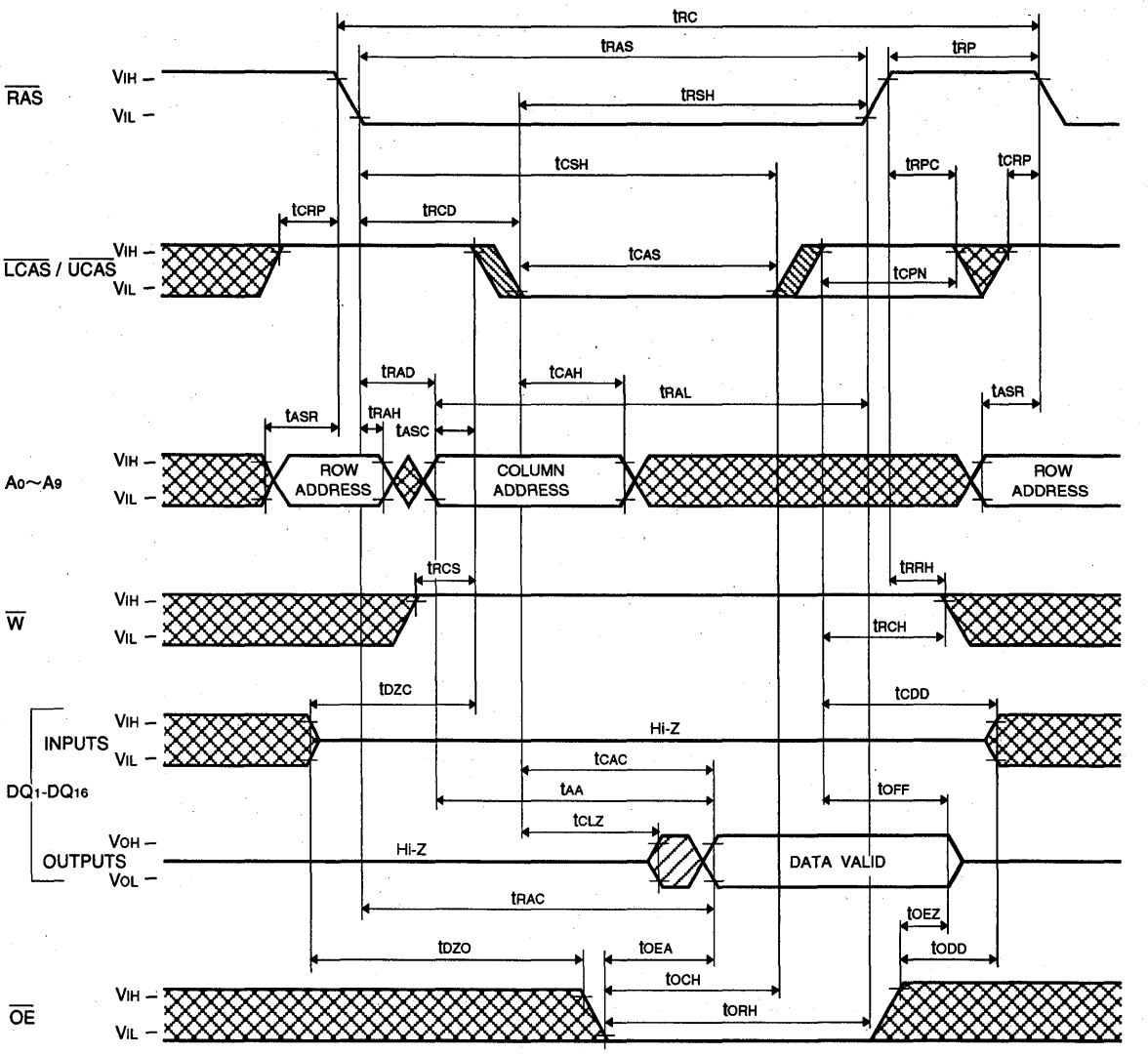
(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦16.4ms.



Timing Diagrams (Note 28)

Read Cycle



Note 28

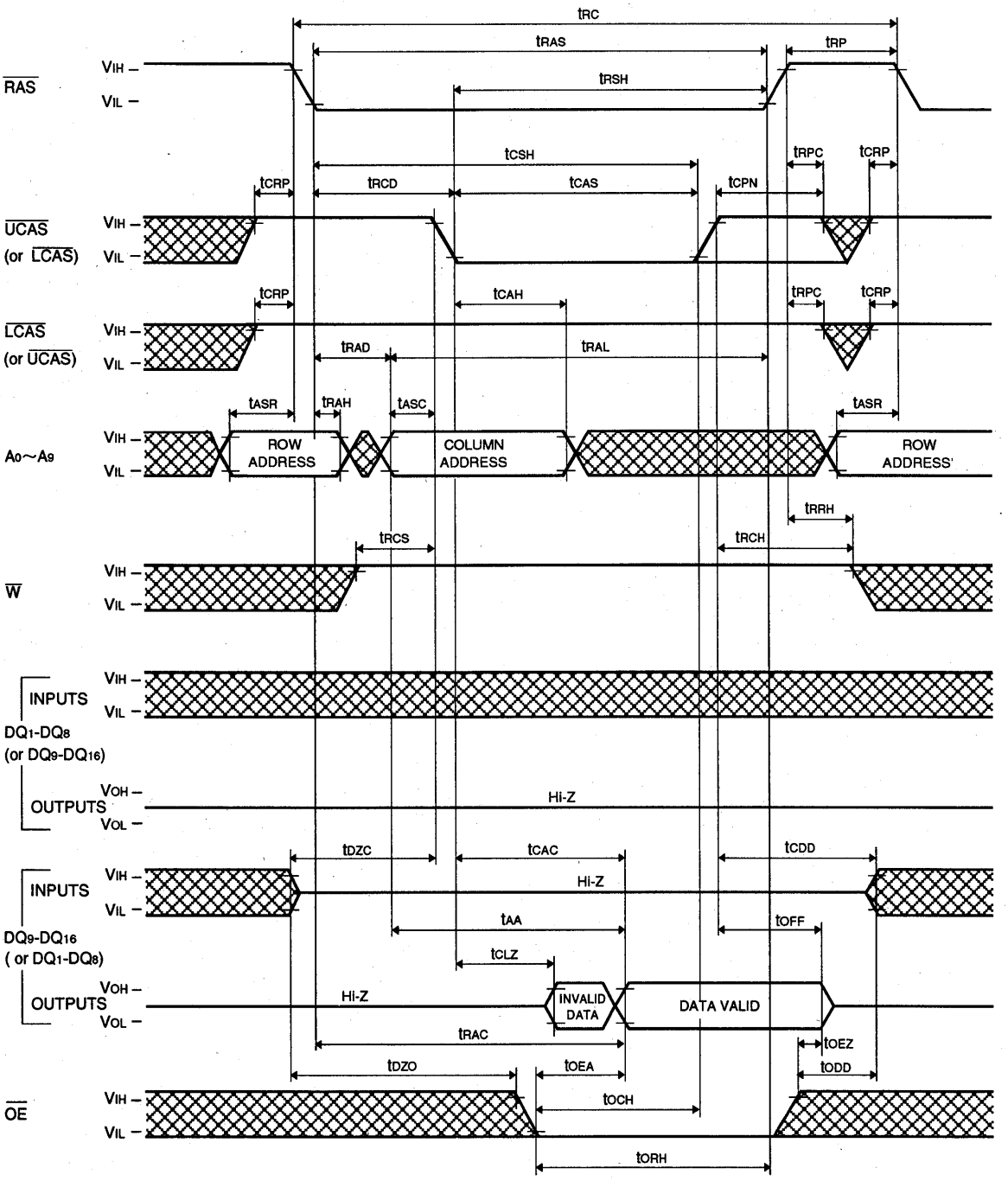
Indicates the don't care input.
VIH(min.) ≦ VIN ≦ VIH(max) or VIL(min.) ≦ VIN ≦ VIL(max)

Indicates the invalid output.

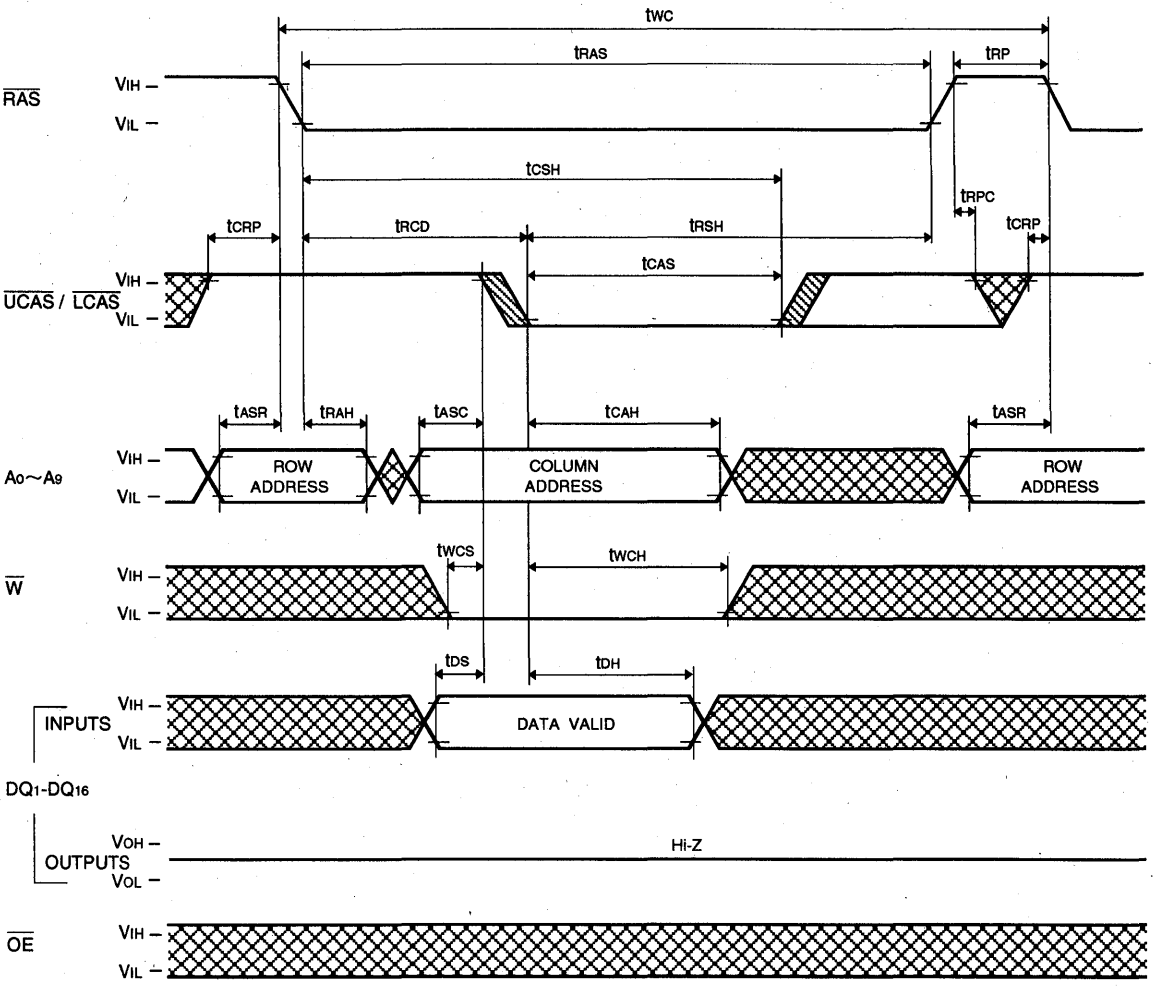
Indicates the skew of the two inputs.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Byte Read Cycle

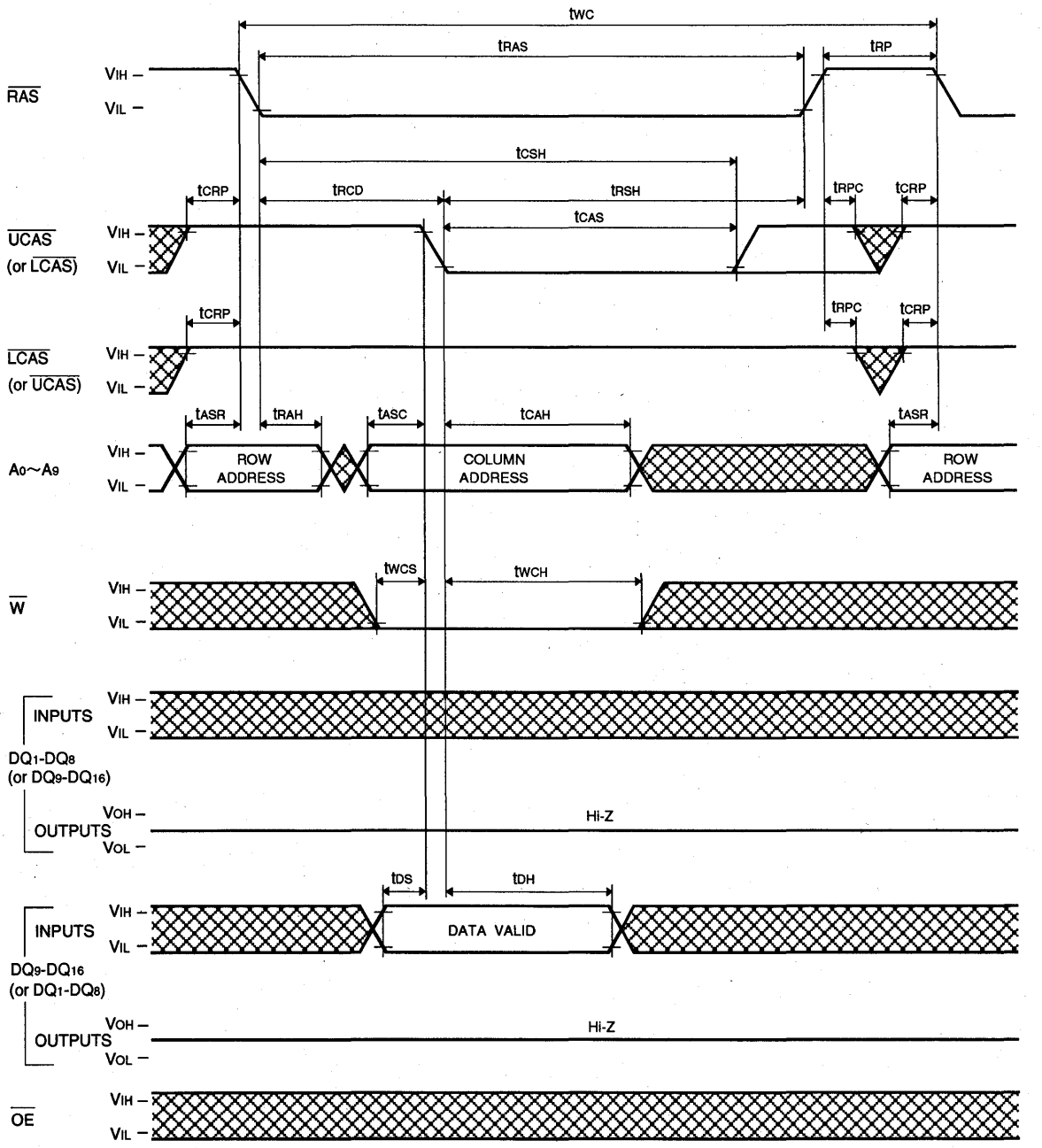


Write Cycle (Early write)

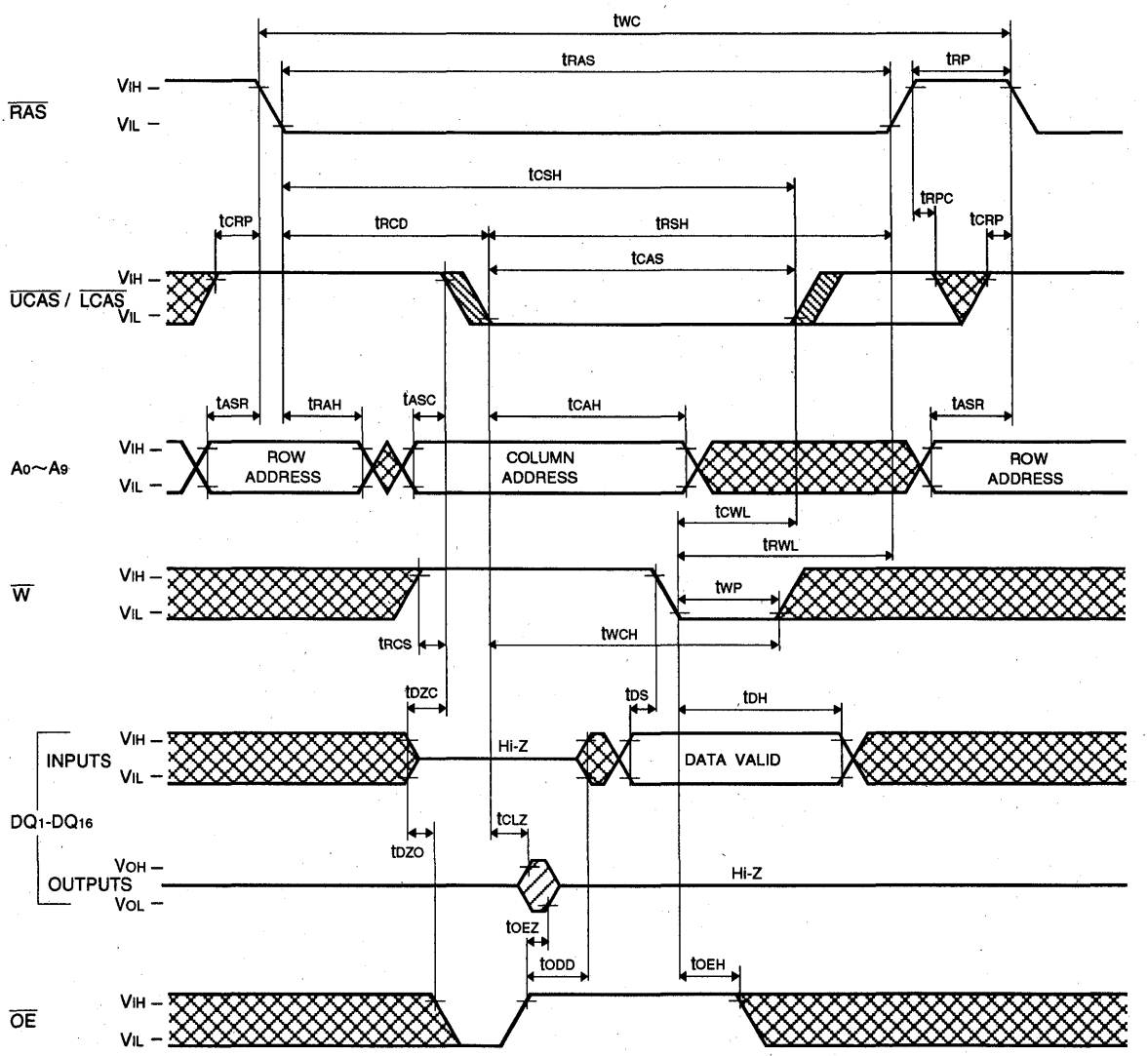


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

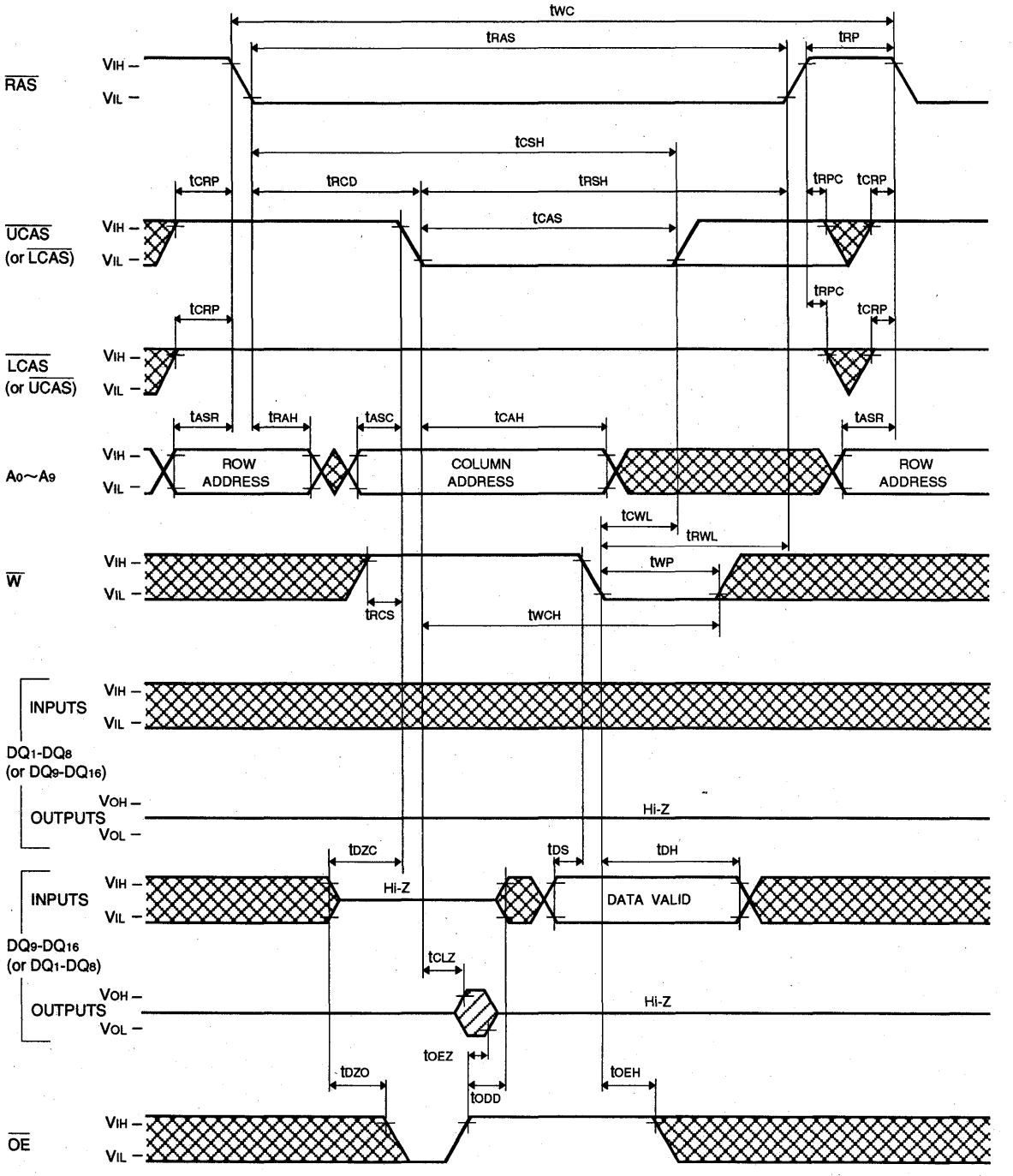
Upper / (Lower) Byte Write Cycle (Early write)



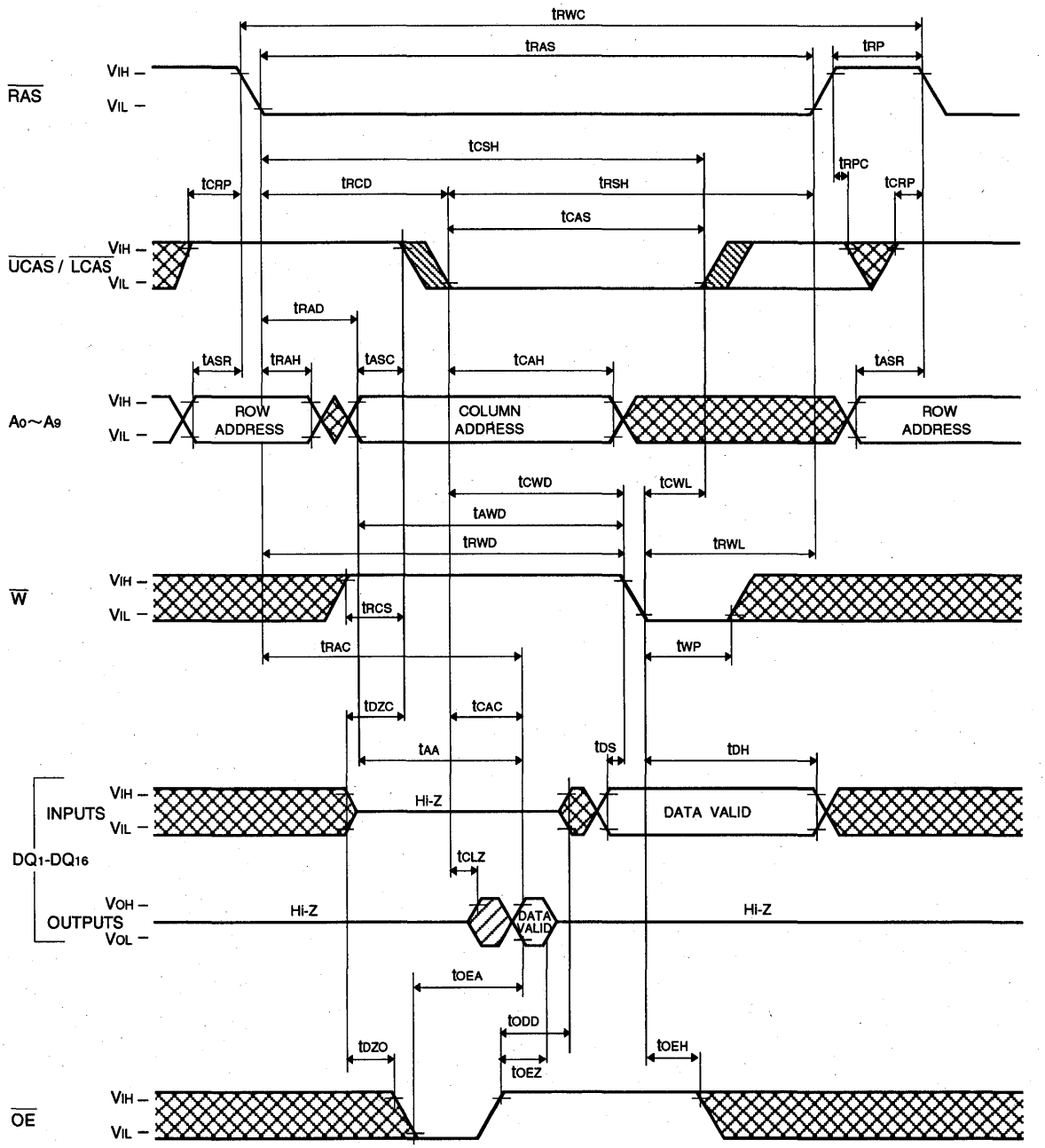
Write Cycle (Delayed write)



Upper / (Lower) Byte Write Cycle (Delayed write)

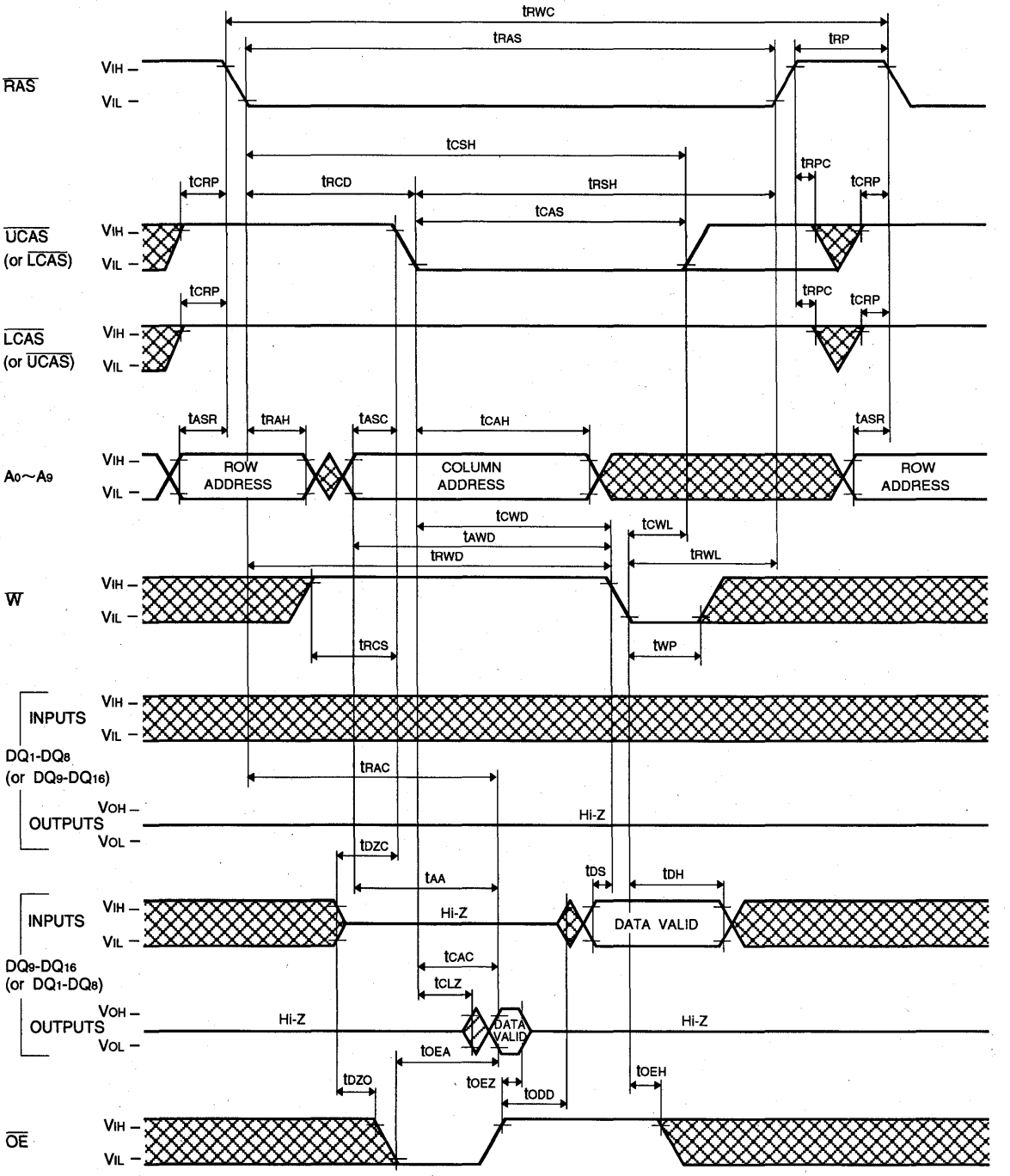


Read-Write, Read-Modify-Write Cycle

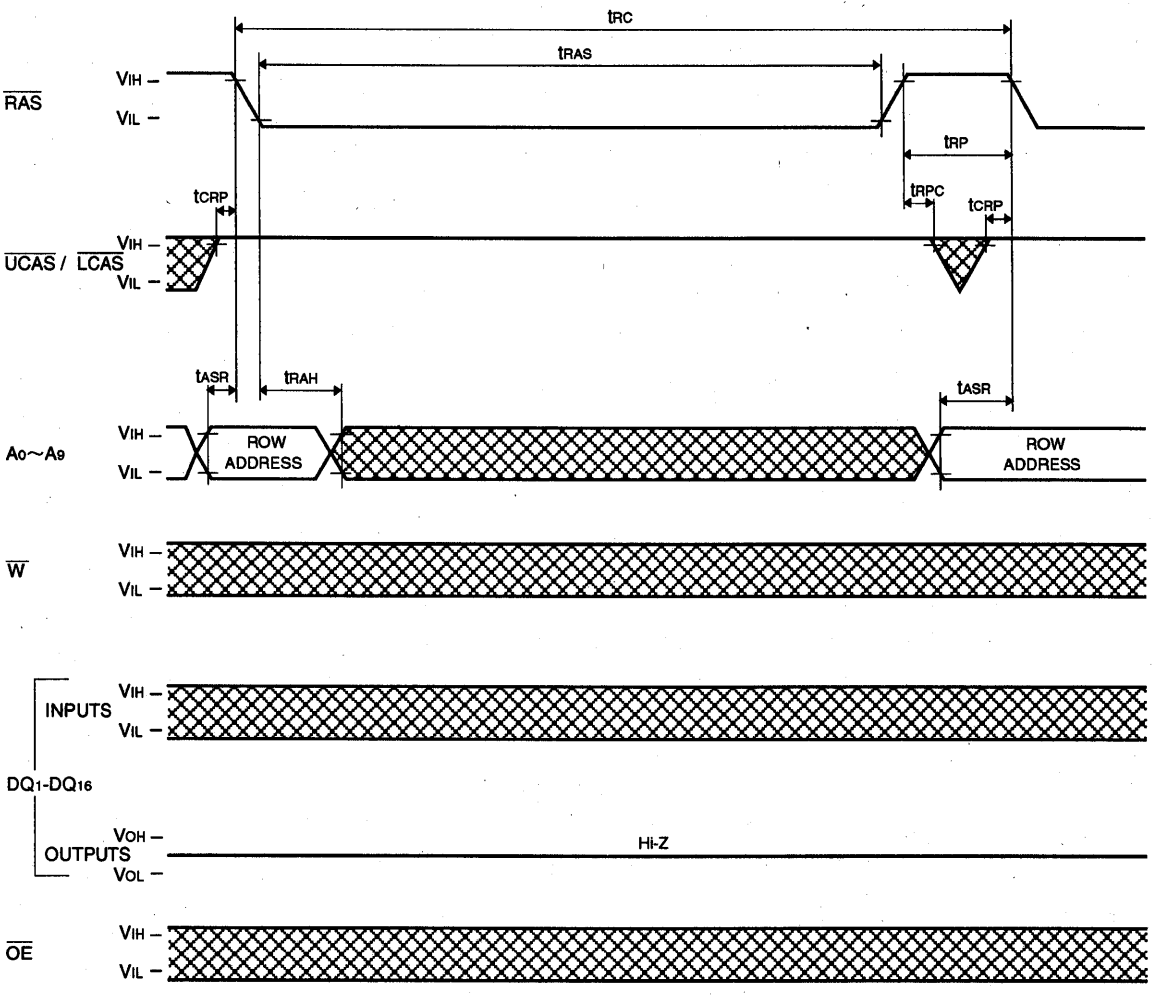


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle

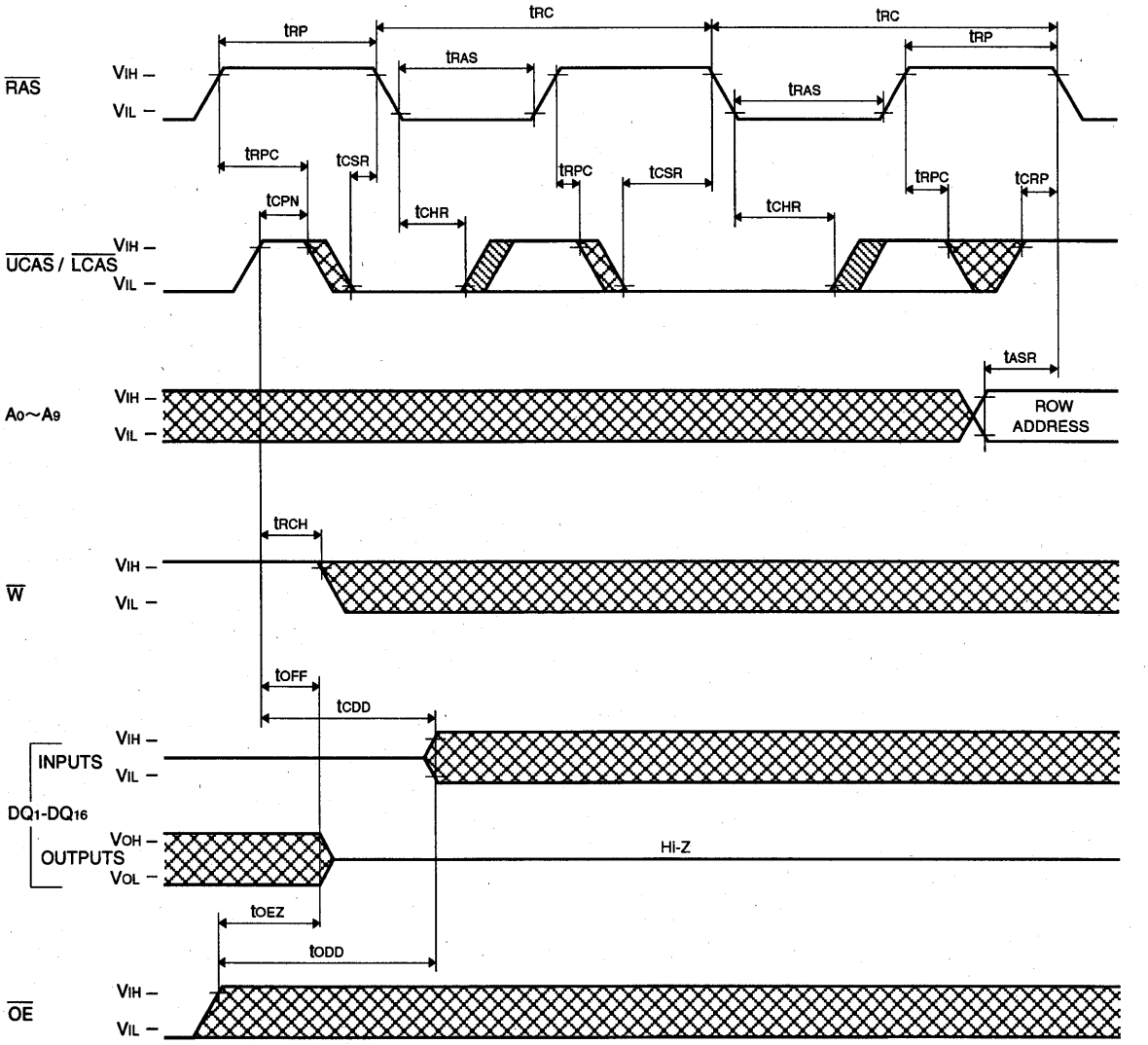


$\overline{RAS}$-only Refresh Cycle

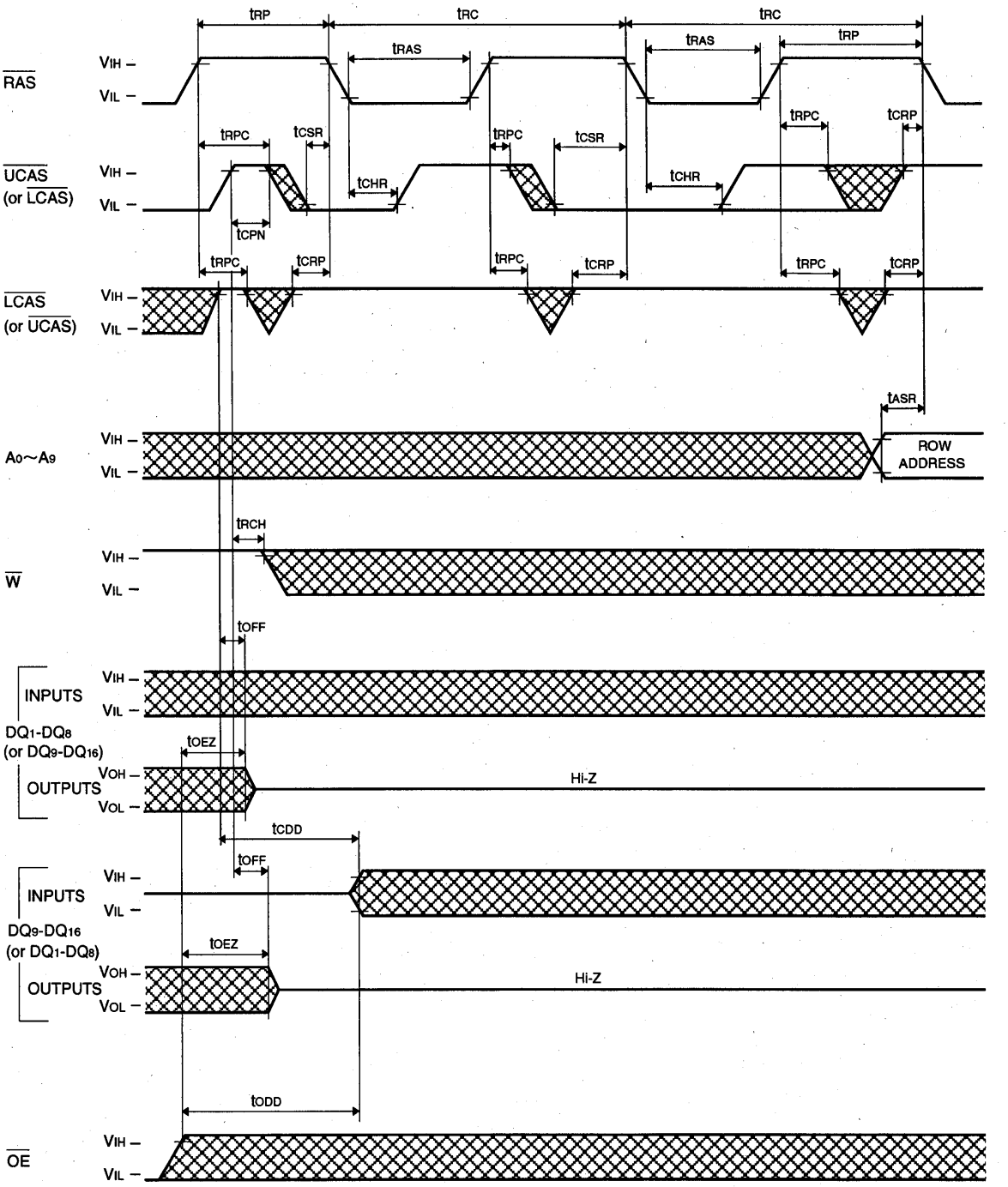


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

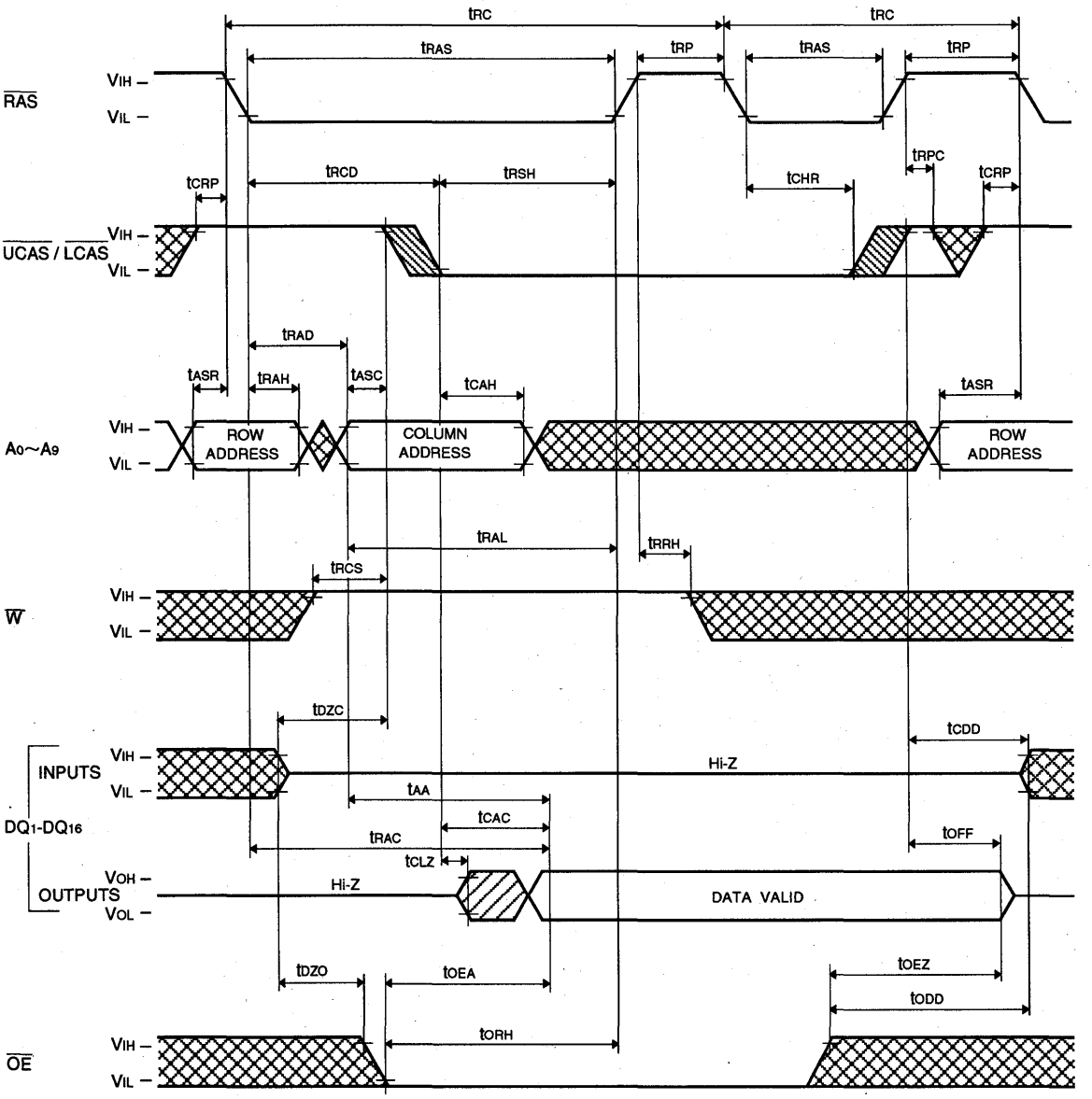
CAS before RAS Refresh Cycle, Extended Refresh Cycle*



Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle ∗

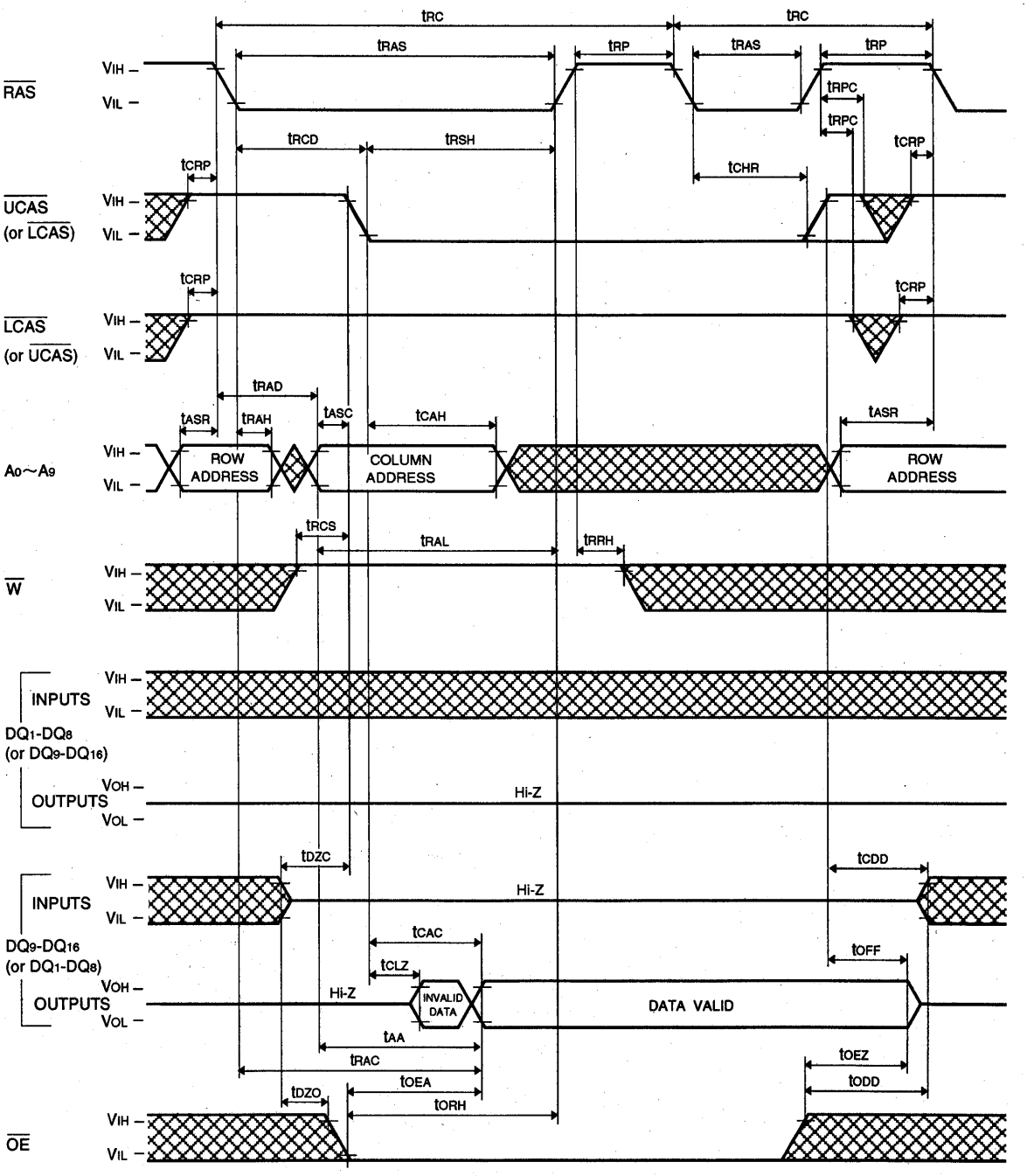


Hidden Refresh Cycle (Read) (Note 29)



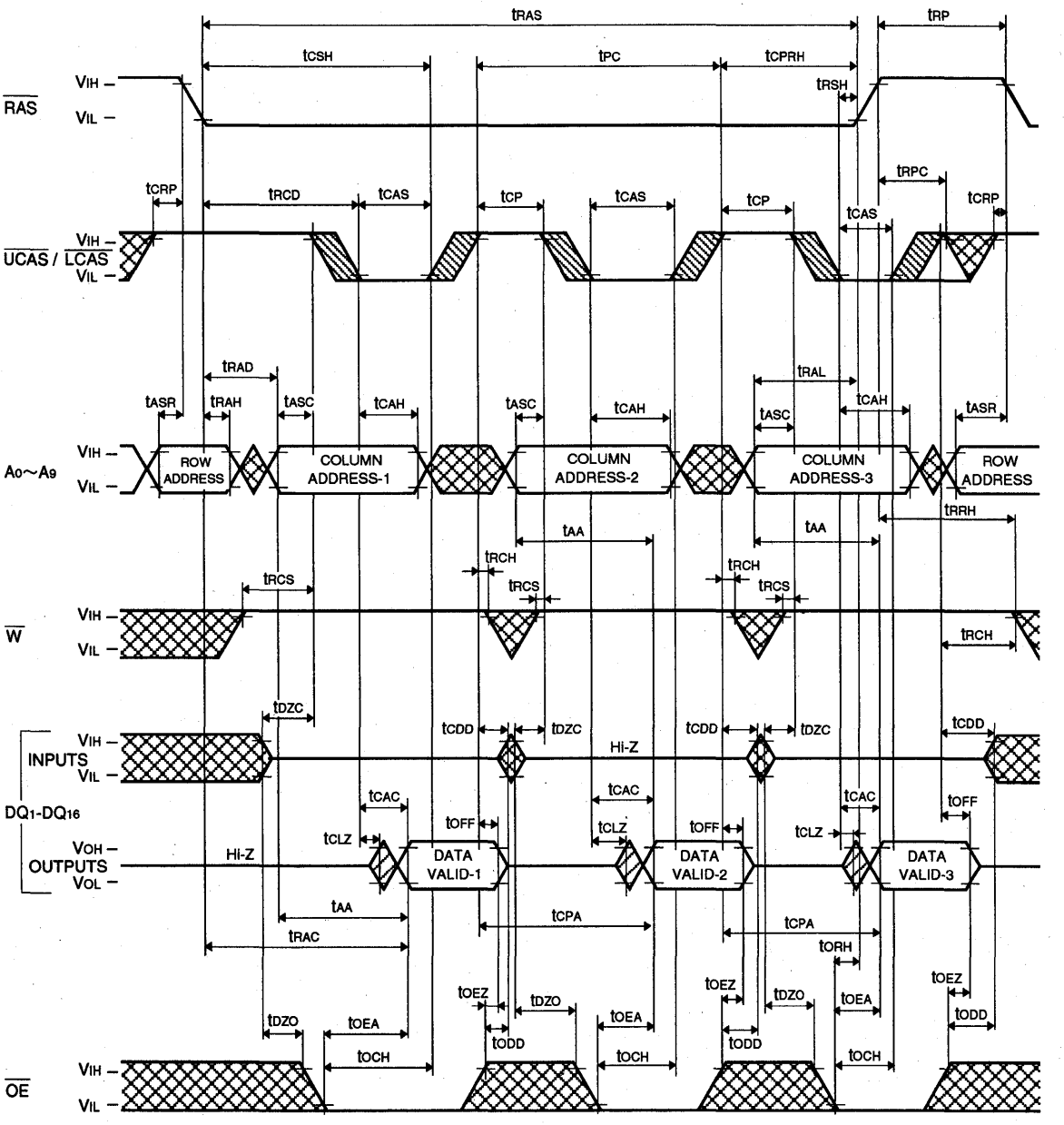
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)

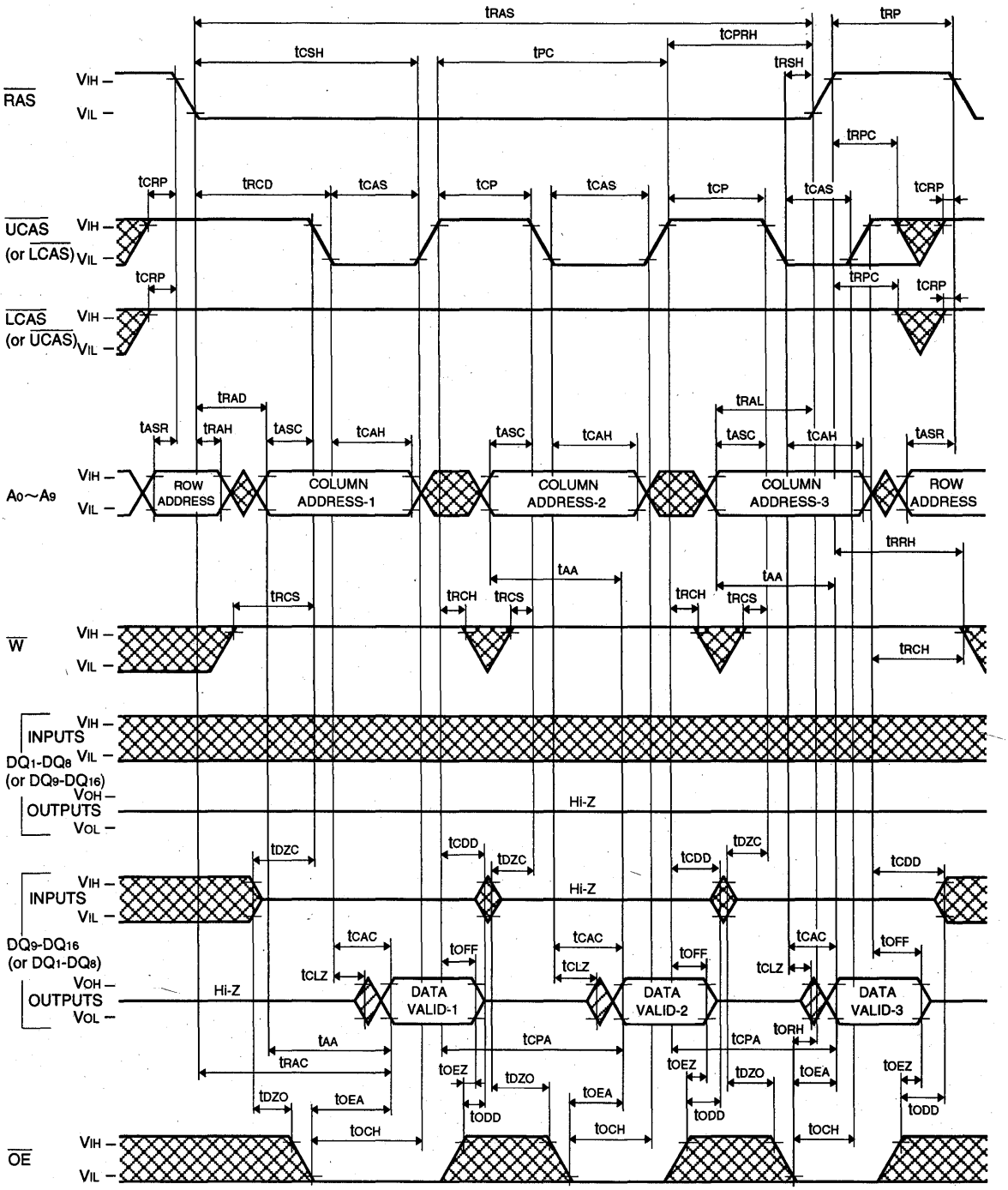


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

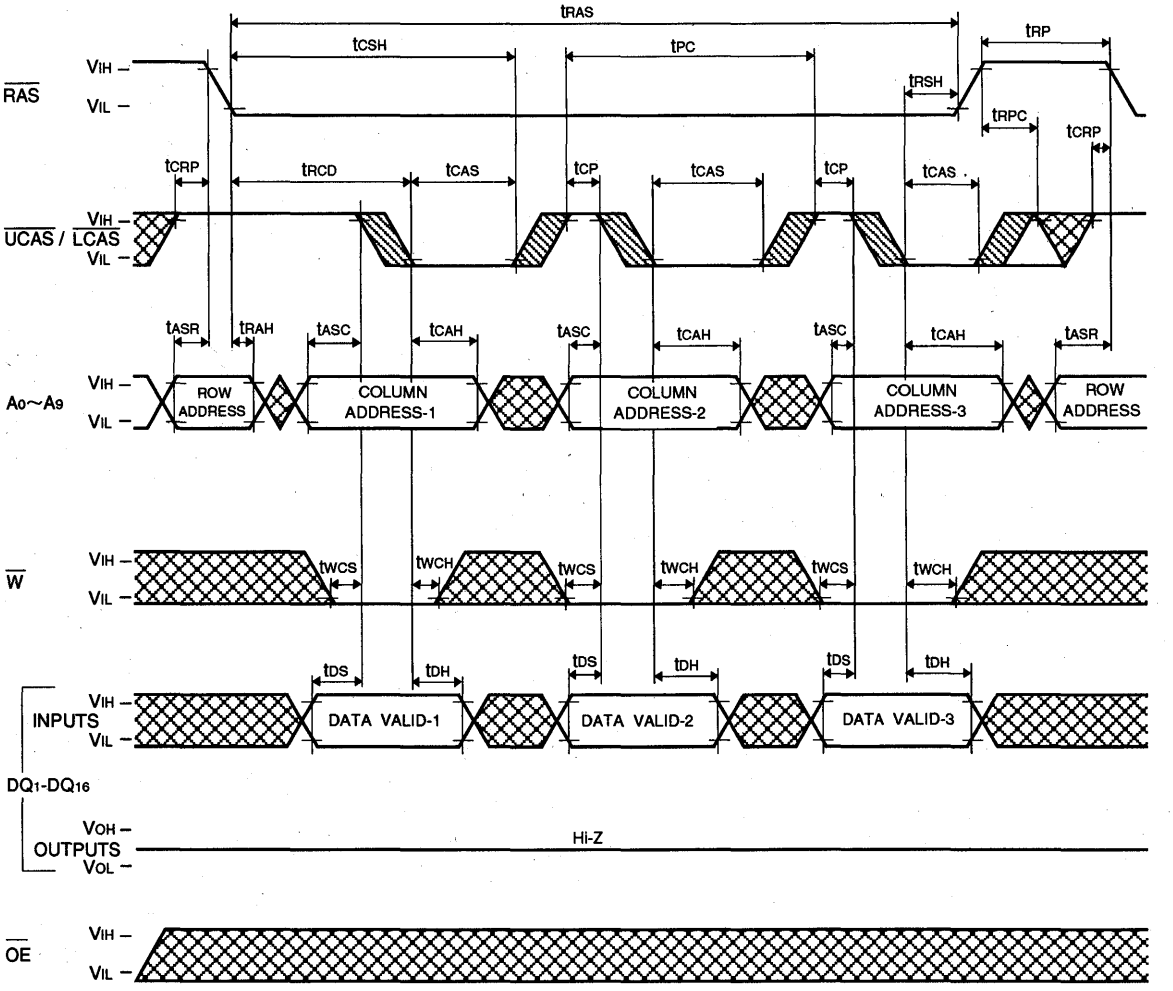
Fast Page Mode Read Cycle



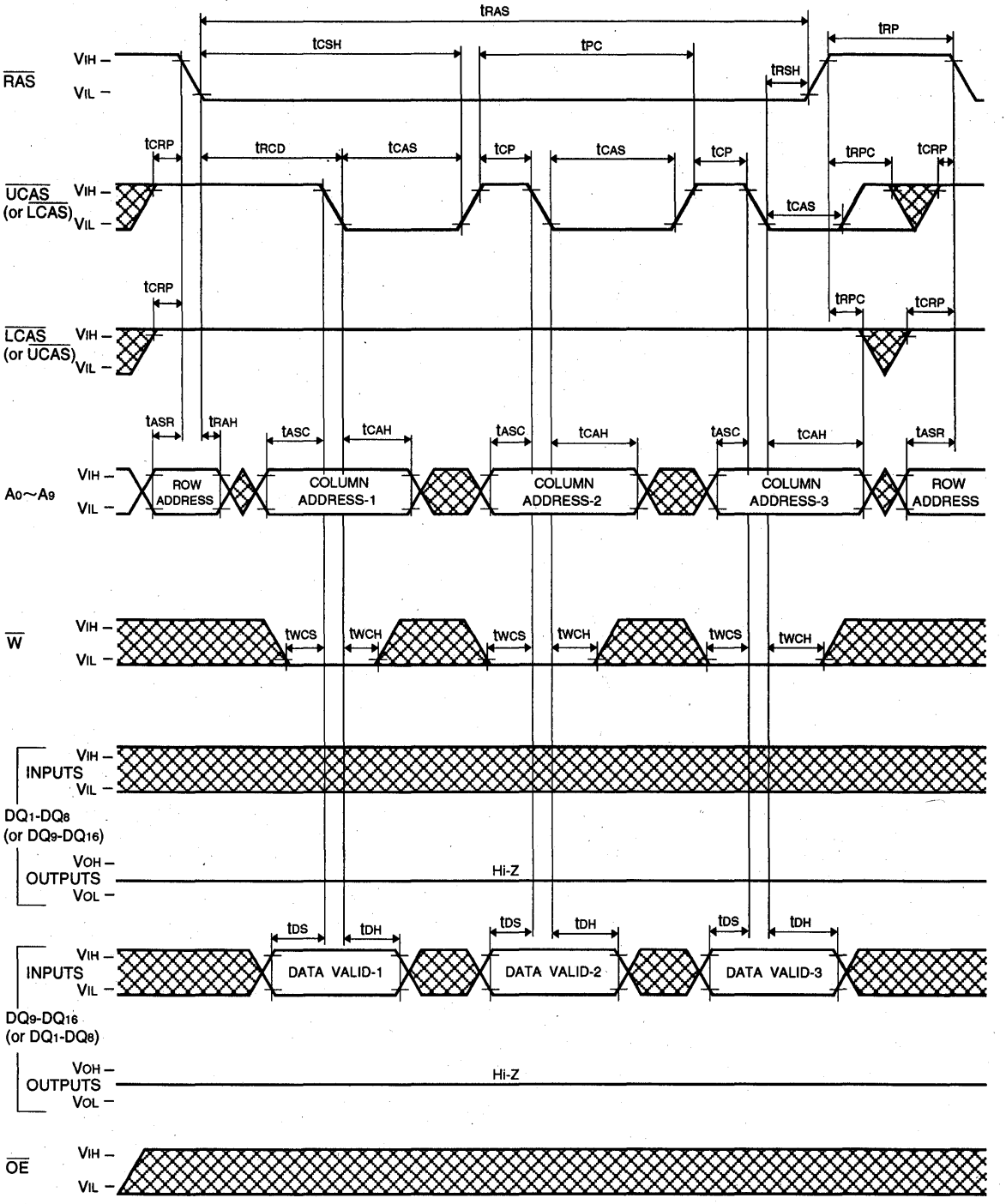
Upper / (Lower) Fast Page Mode Read Cycle



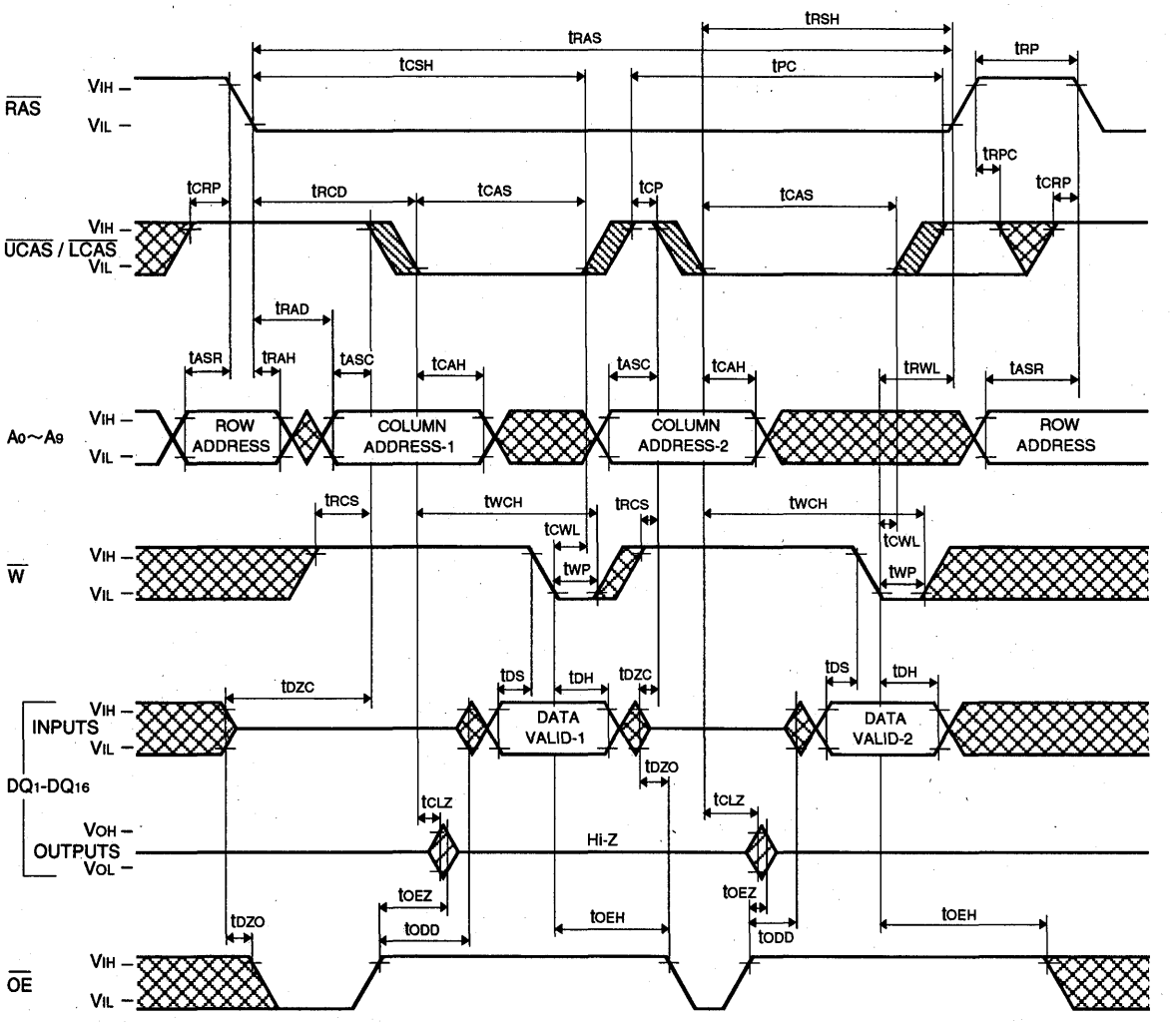
Fast Page Mode Write Cycle (Early Write)



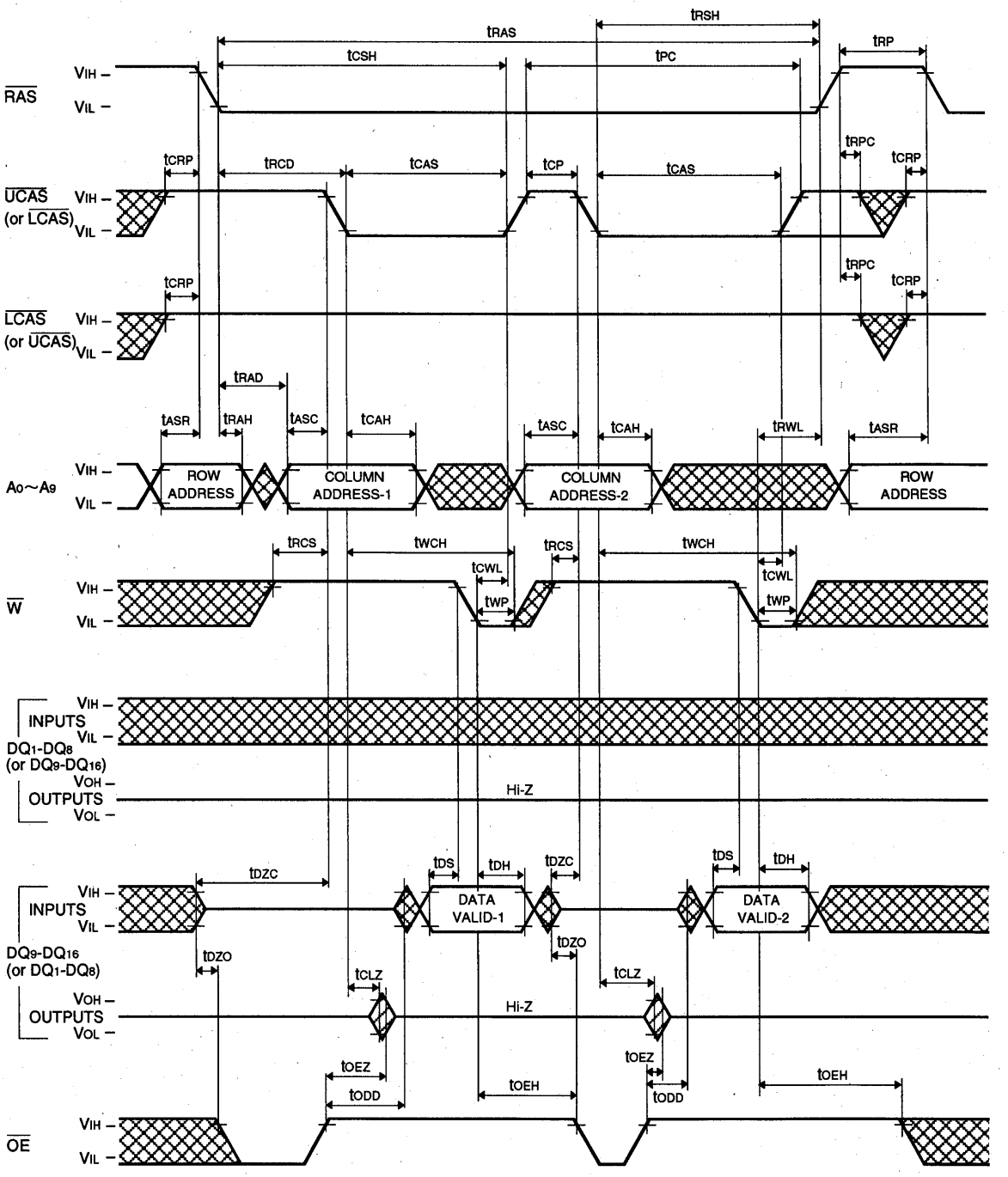
Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)



Fast Page Mode Write Cycle (Delayed Write)

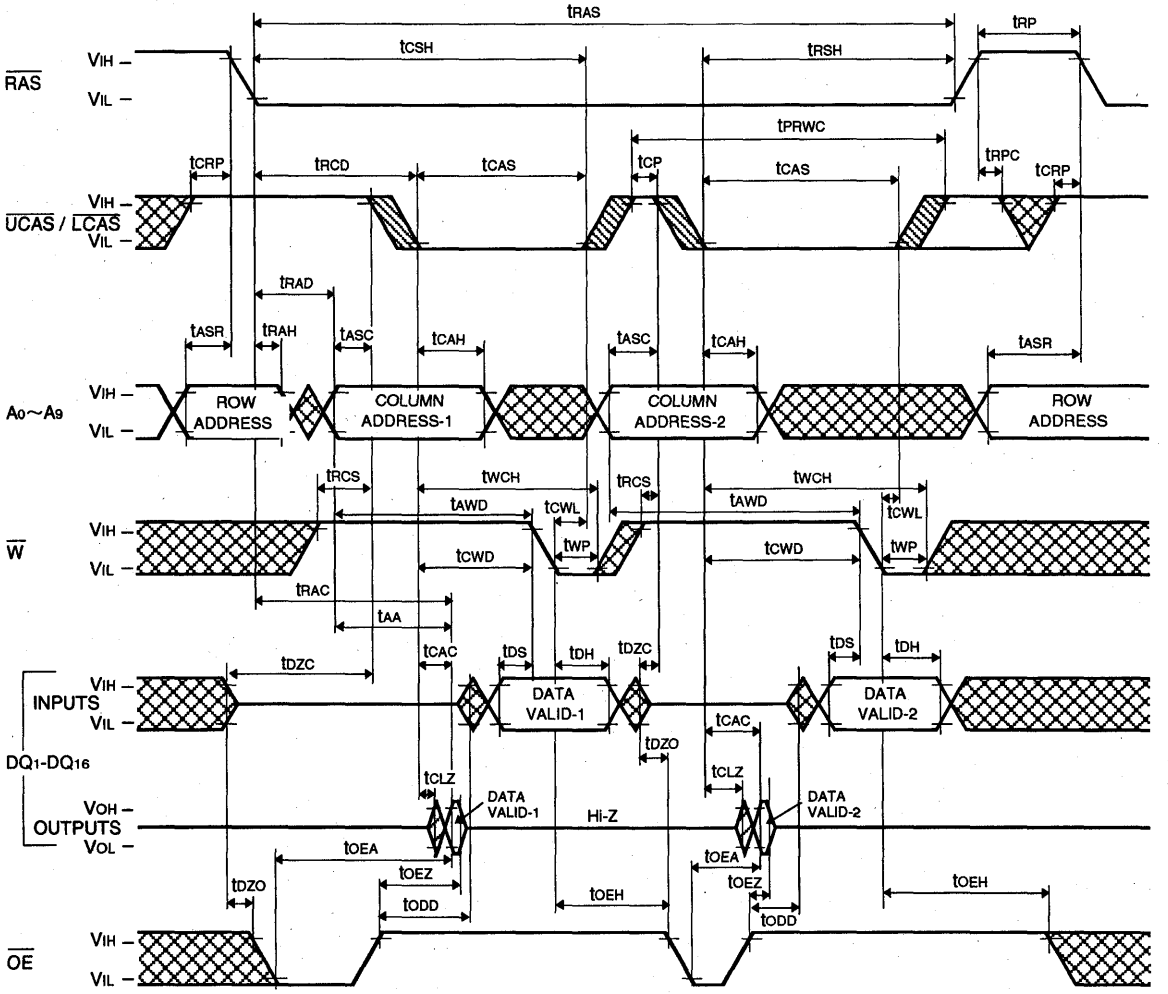


Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)

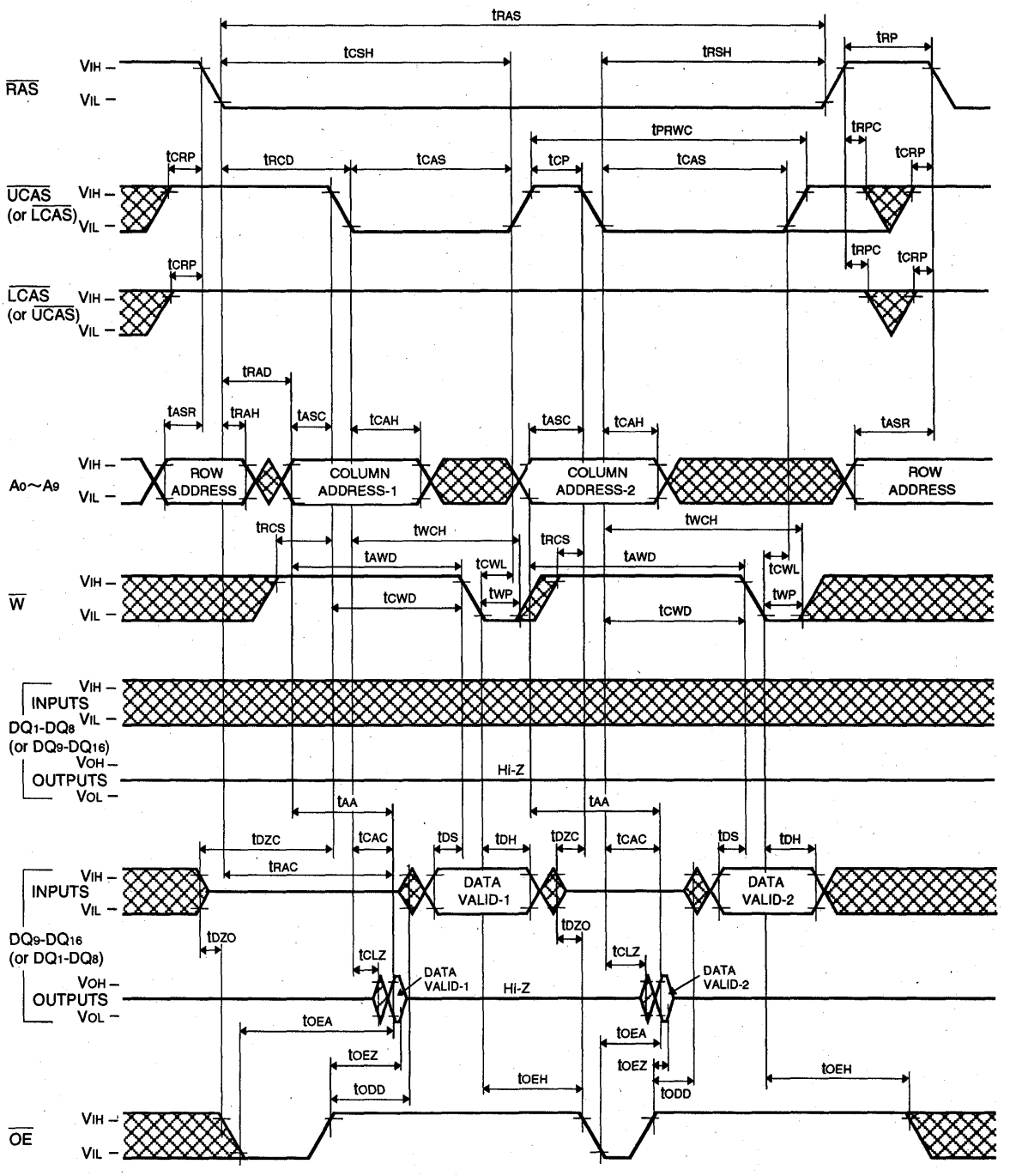


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read-Write, Read-Modify-Write Cycle

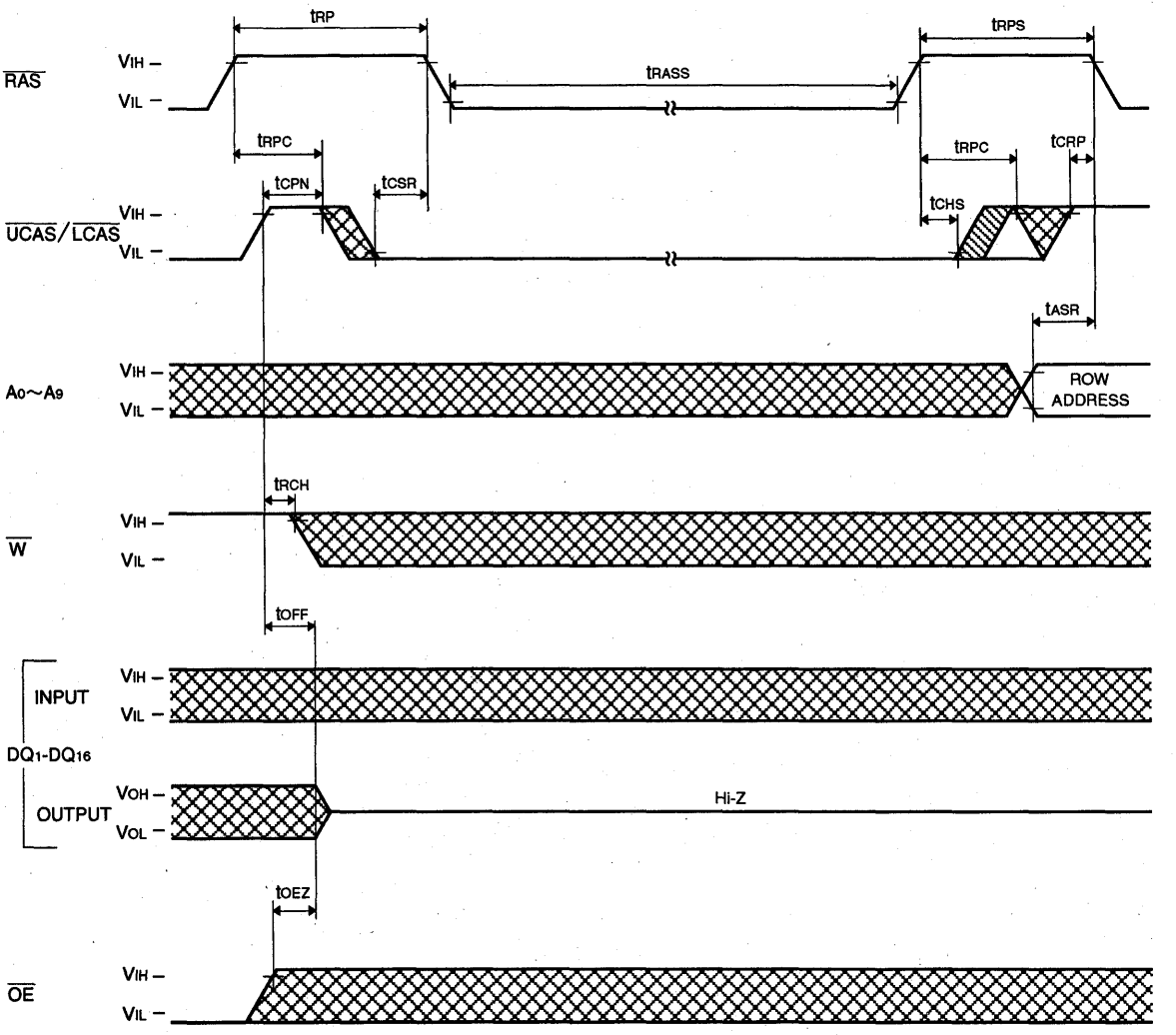


Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle

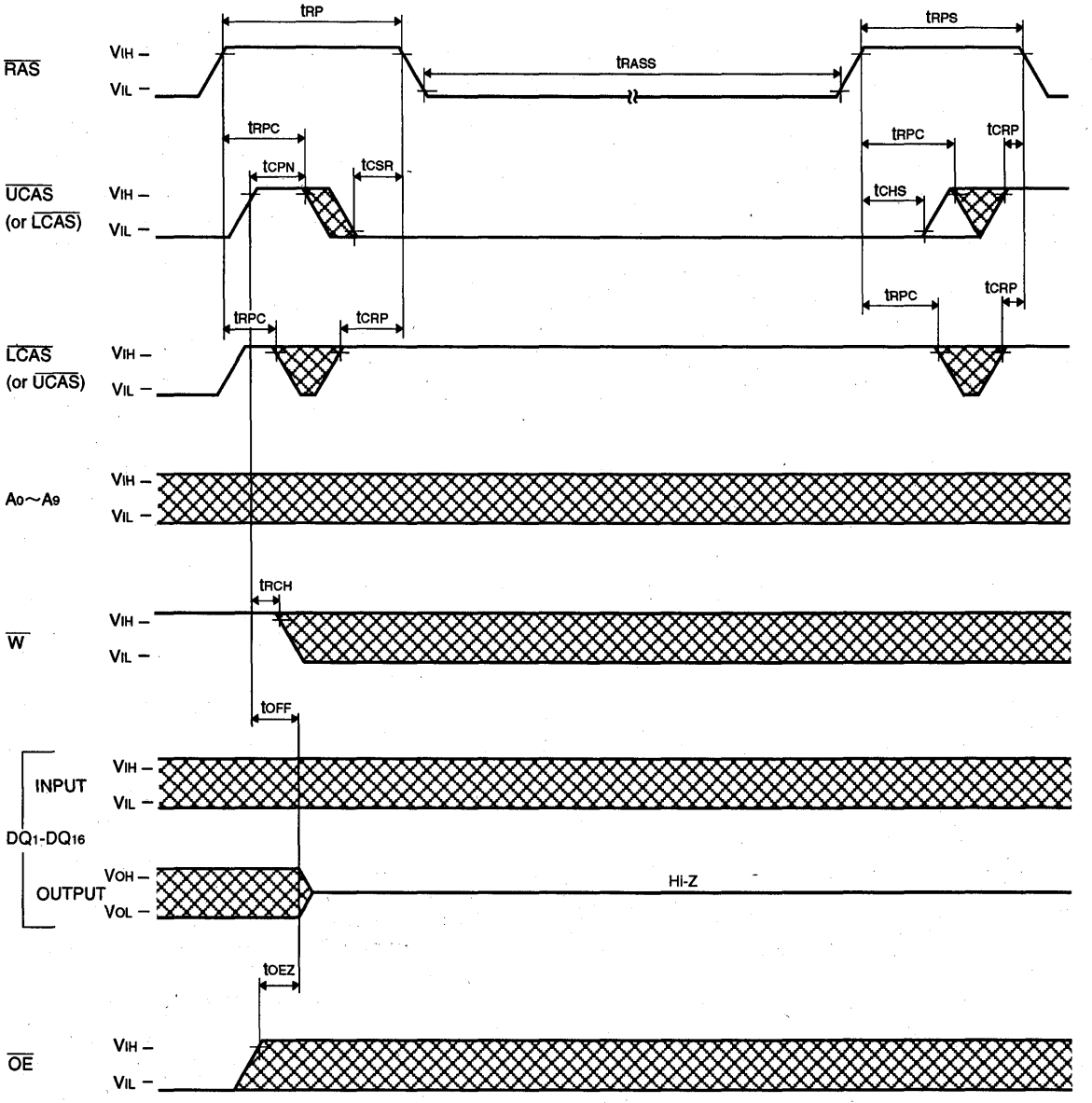


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle∗



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16165CTP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

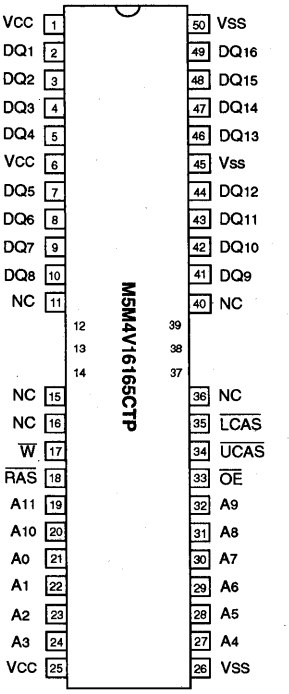
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16165CTP-5,-5S	50	13	25	13	90	360
M5M4V16165CTP-6,-6S	60	15	30	15	110	285
M5M4V16165CTP-7,-7S	70	20	35	20	130	255

- Standard 50 pin TSOP
- Single 3.3V ±10% supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V16165CTP-5,-5S ---------- 435.0mW (Max)
  M5M4V16165CTP-6,-6S ---------- 345.0mW (Max)
  M5M4V16165CTP-7,-7S ---------- 310.0mW (Max)
- Hyper-page mode, Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0~A_{11})
  * : Applicable to self refresh version (M5M4V16165CTP-5S,-6S, -7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F(400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

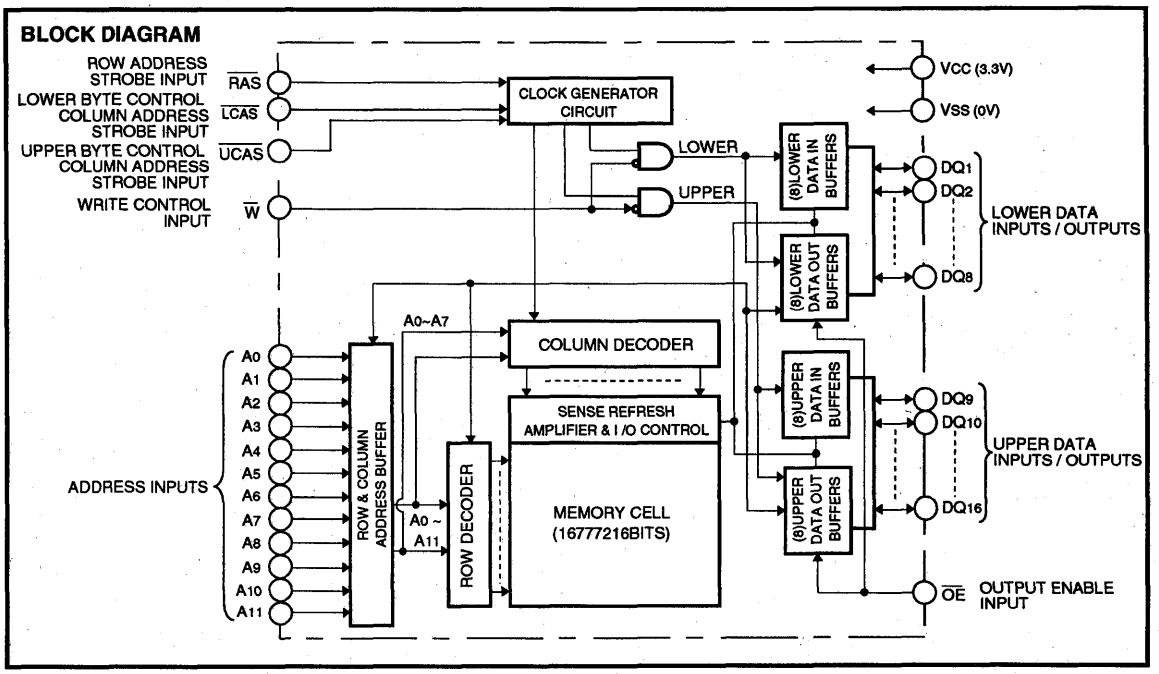
The M5M4V16165CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M4V16165C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}-0.2V output open			0.5	
						0.15*	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M4V16165C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M4V16165C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			165	mA
		M5M4V16165C-6,-6S				130	
		M5M4V16165C-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V16165C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
$I_{CC8(AV)}$*	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M4V16165C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A_0~A_{11}≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125μs, t_{RAS}=t_{RASmin}~1μs			400	μA
$I_{CC9(AV)}$*	Average supply current from Vcc Self-refresh cycle	M5M4V16165C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 12)	0	13	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$. and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\,\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	20		25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time	57		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 27)	8	13	10	16	10	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	45		52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read	52		62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	62		72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

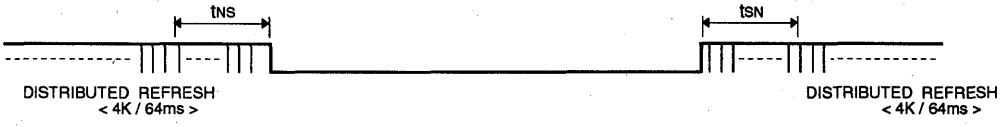
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5S		M5M4V16165C-6S		M5M4V16165C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

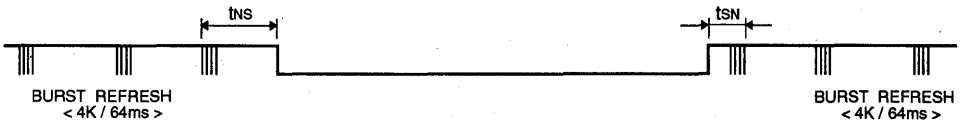
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64ms$ and $t_{SN} \leqq 64ms$.



(2) In case of burst refresh

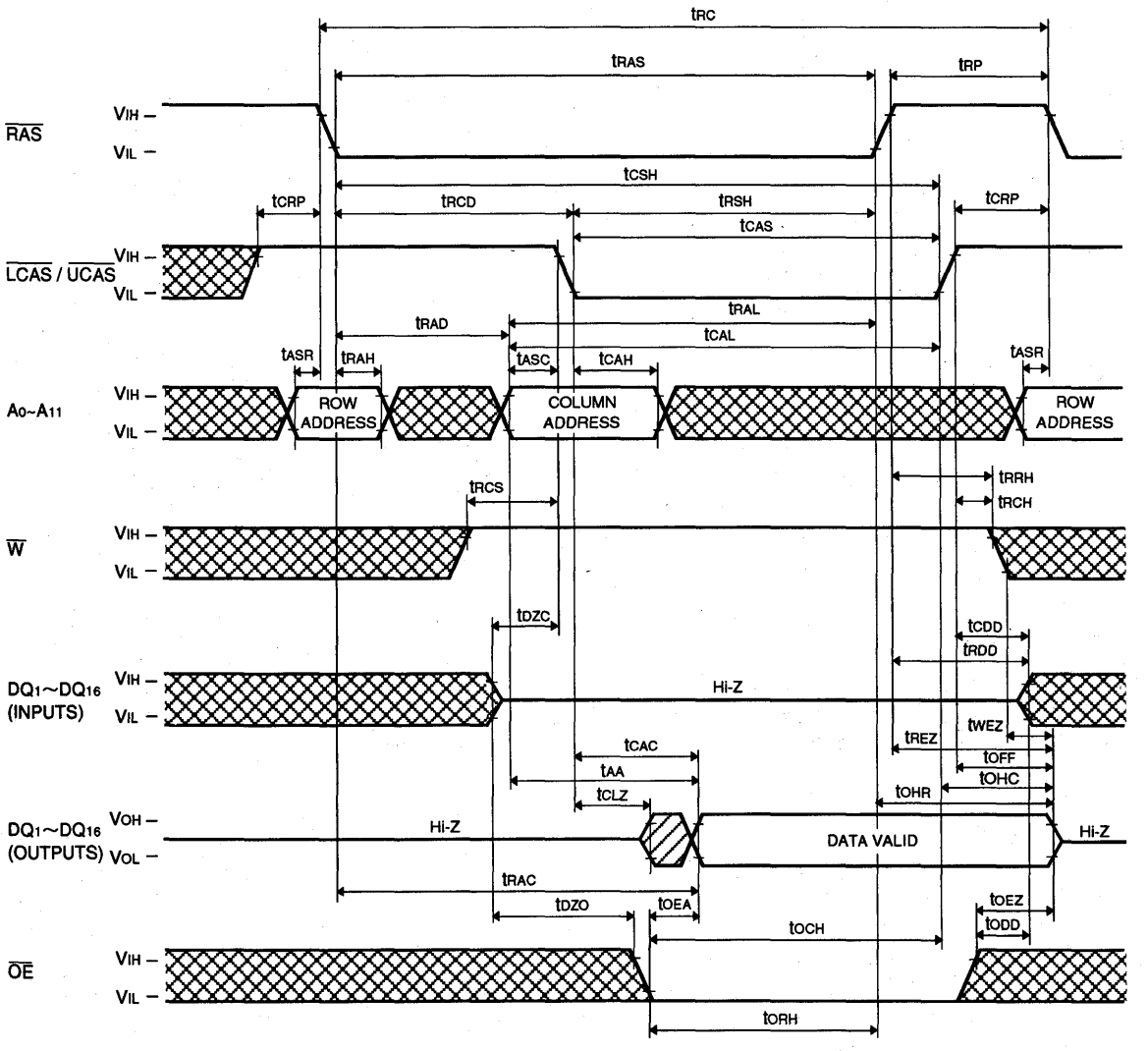
The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 64ms$.



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timing Diagrams (Note 29)

Read Cycle

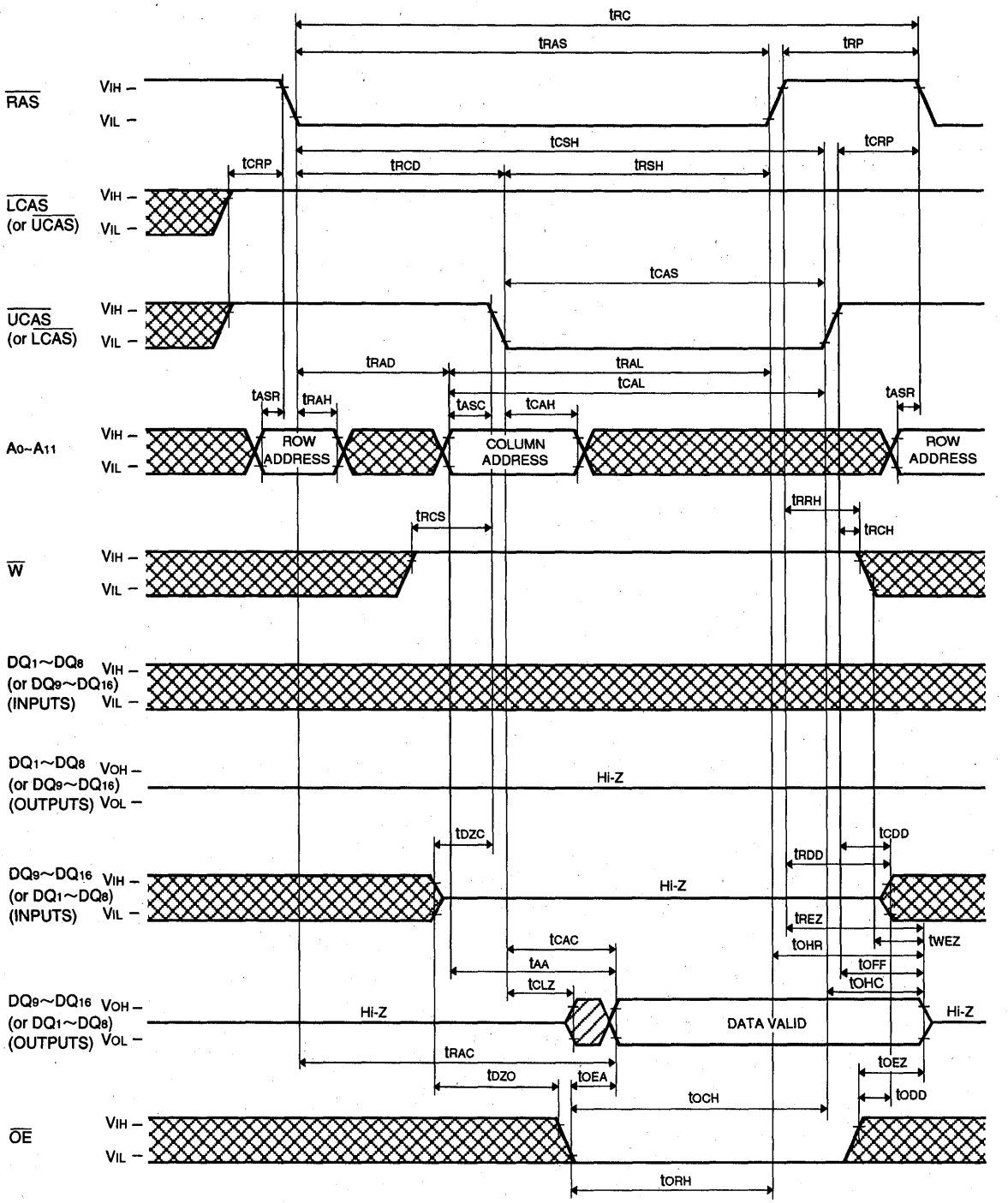


Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

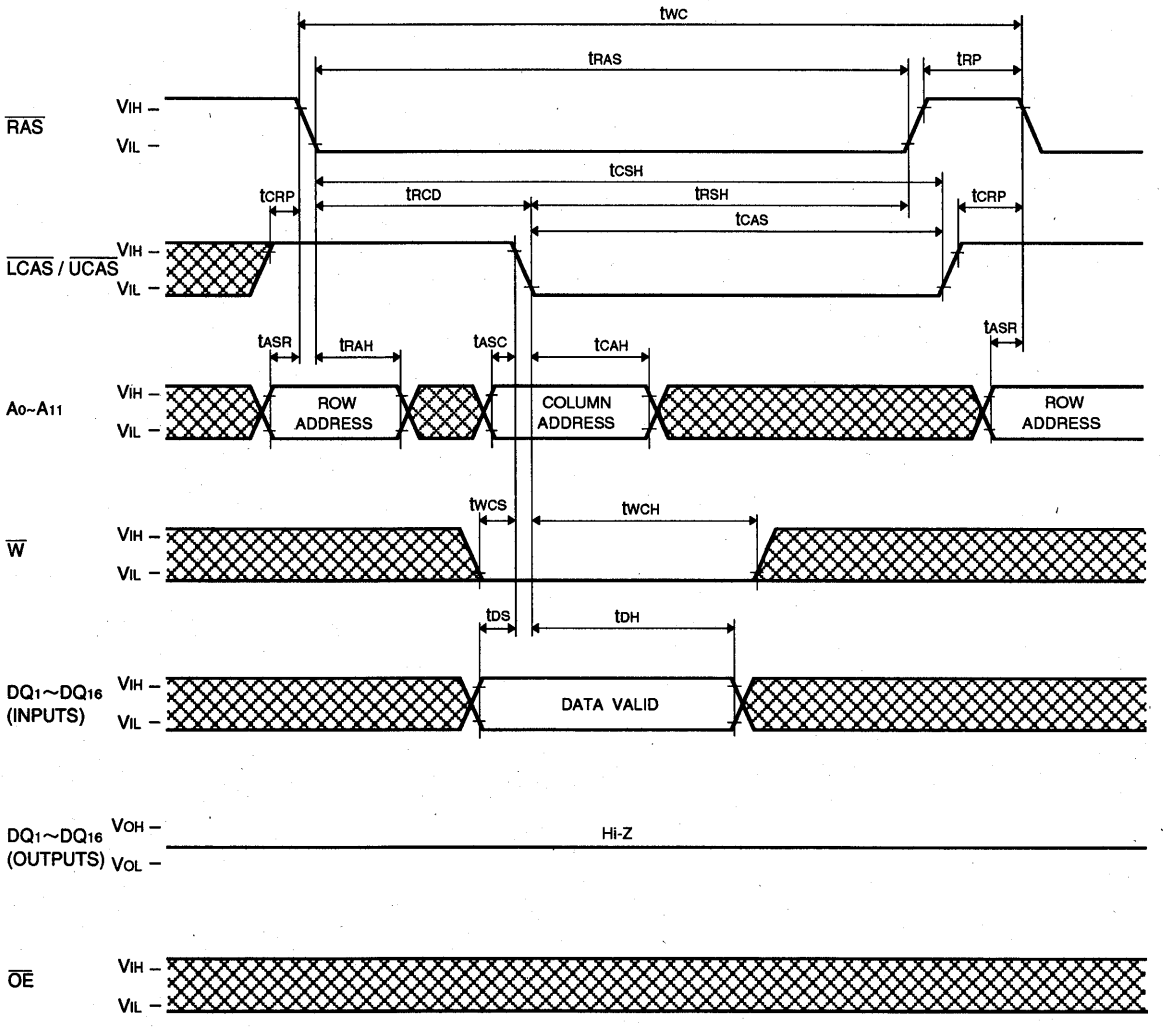
Indicates the invalid output.

Byte Read Cycle

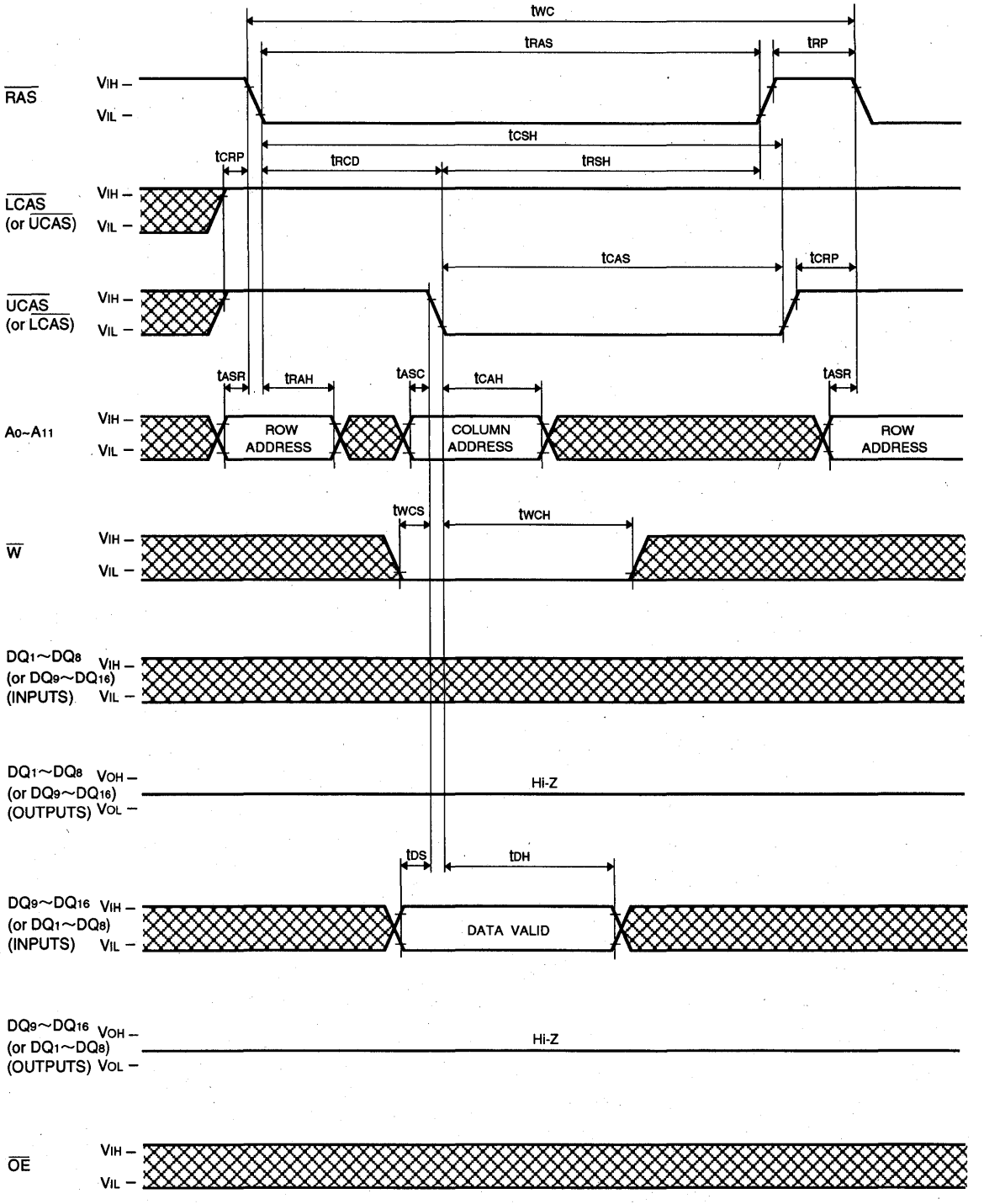


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

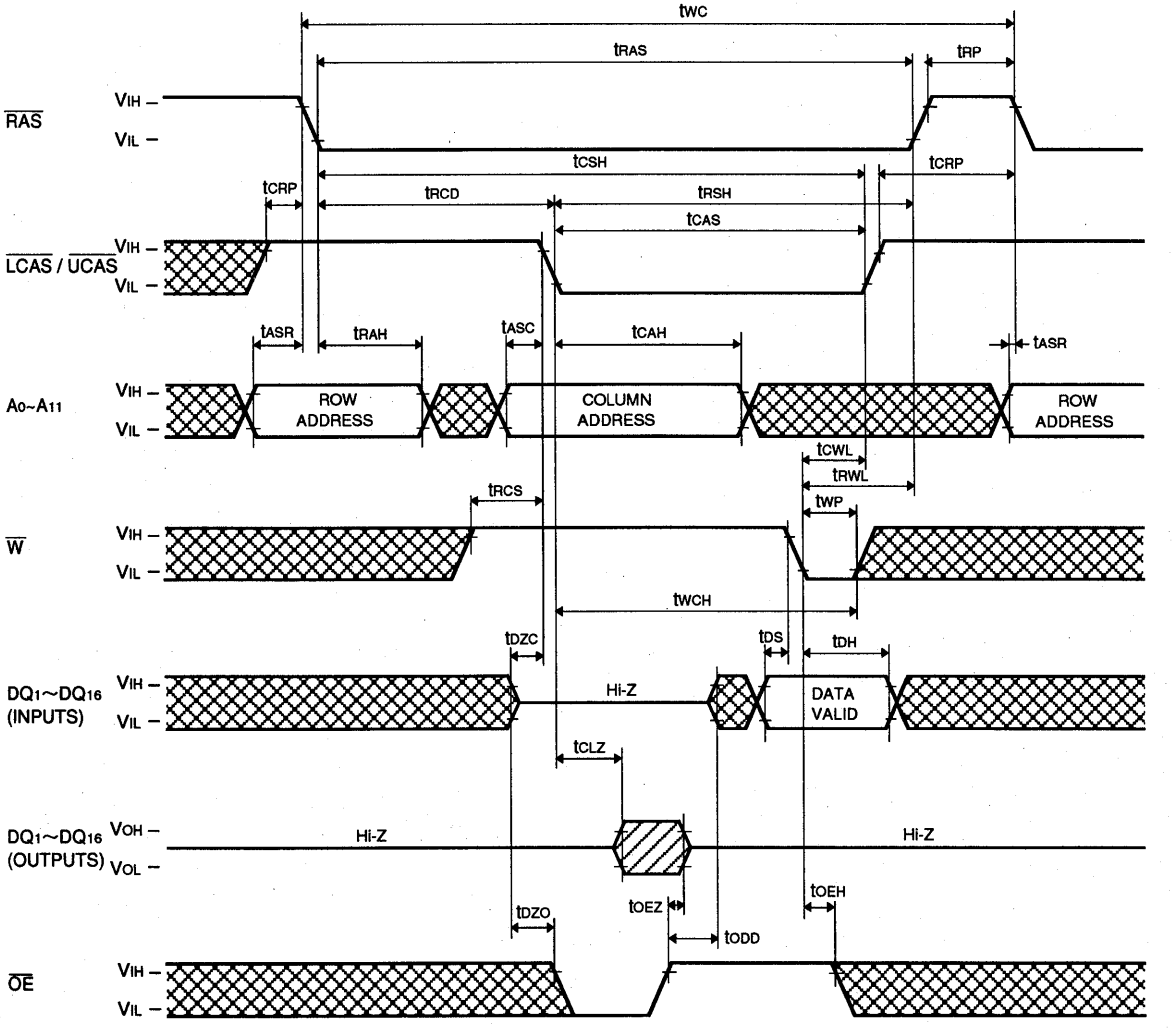
Early Write Cycle



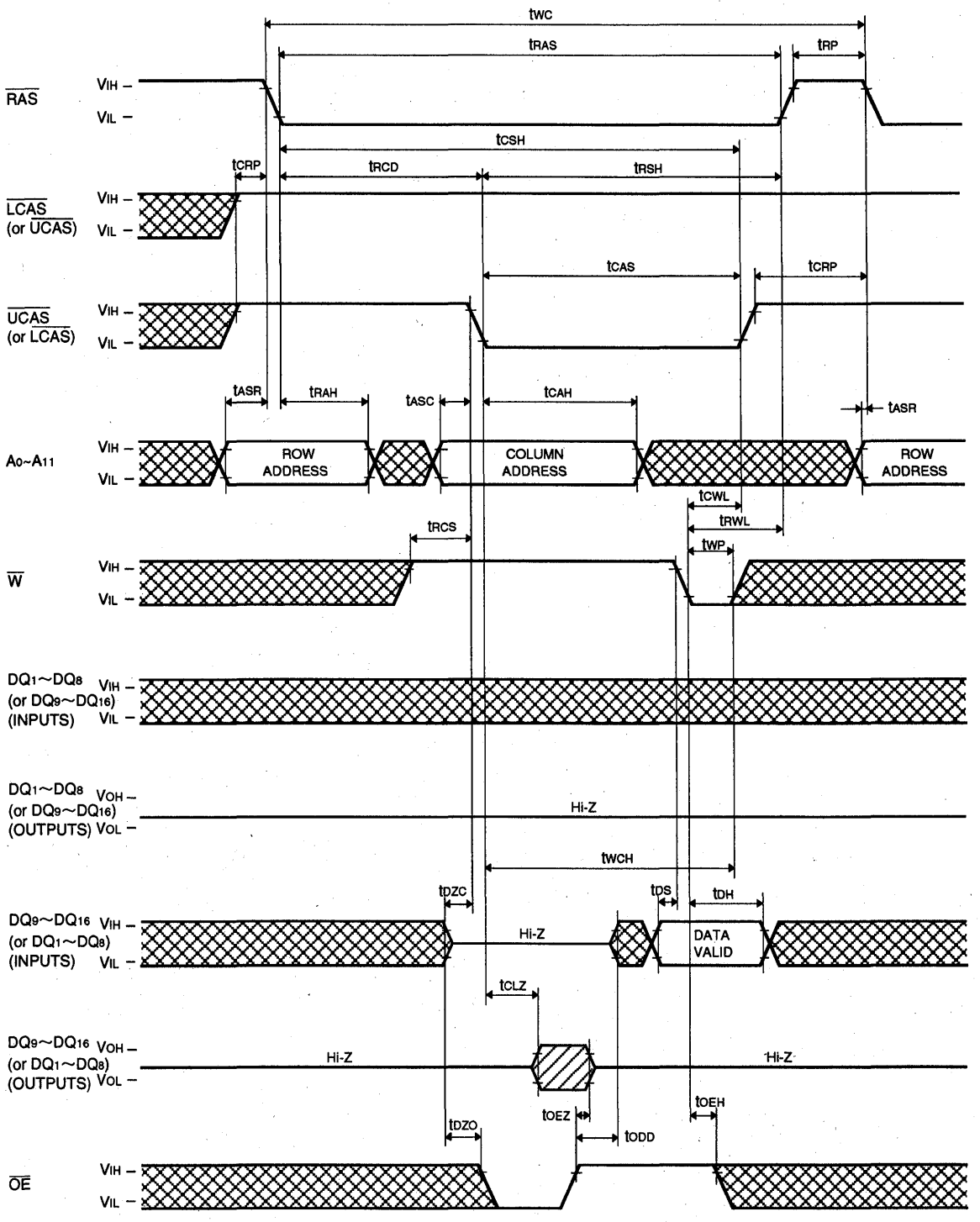
Byte Early Write Cycle



Delayed Write Cycle

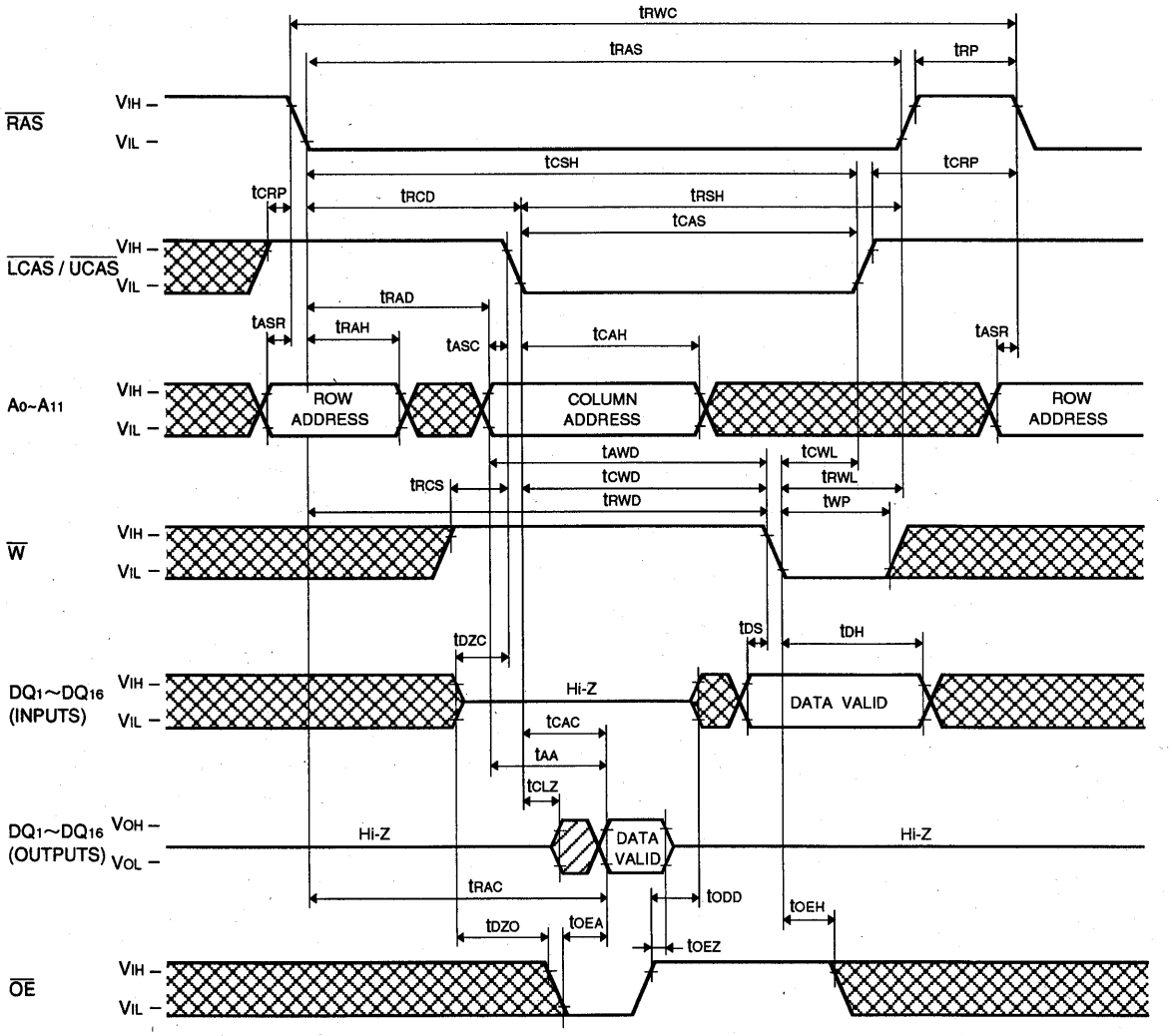


Byte Delayed Write Cycle

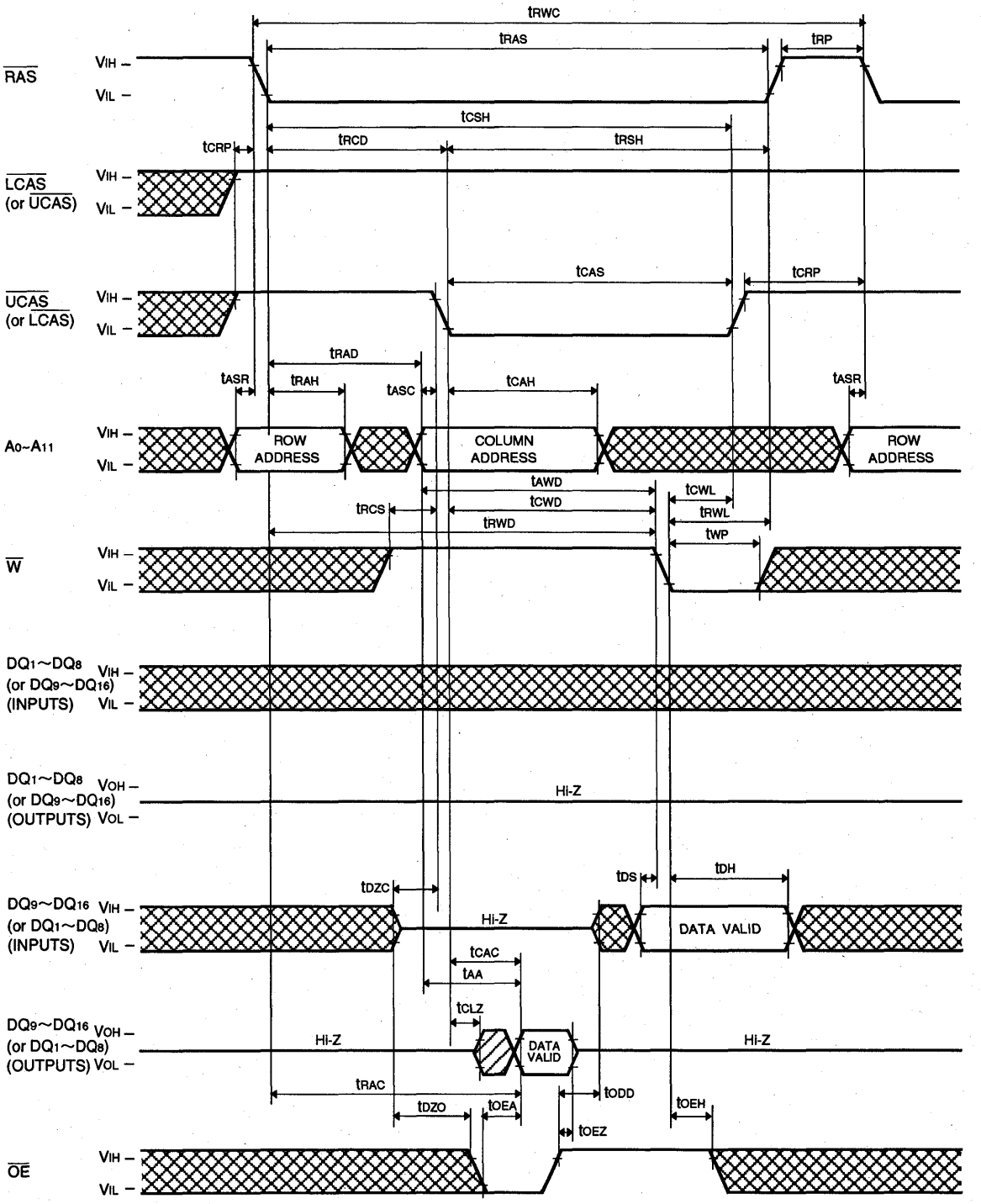


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle

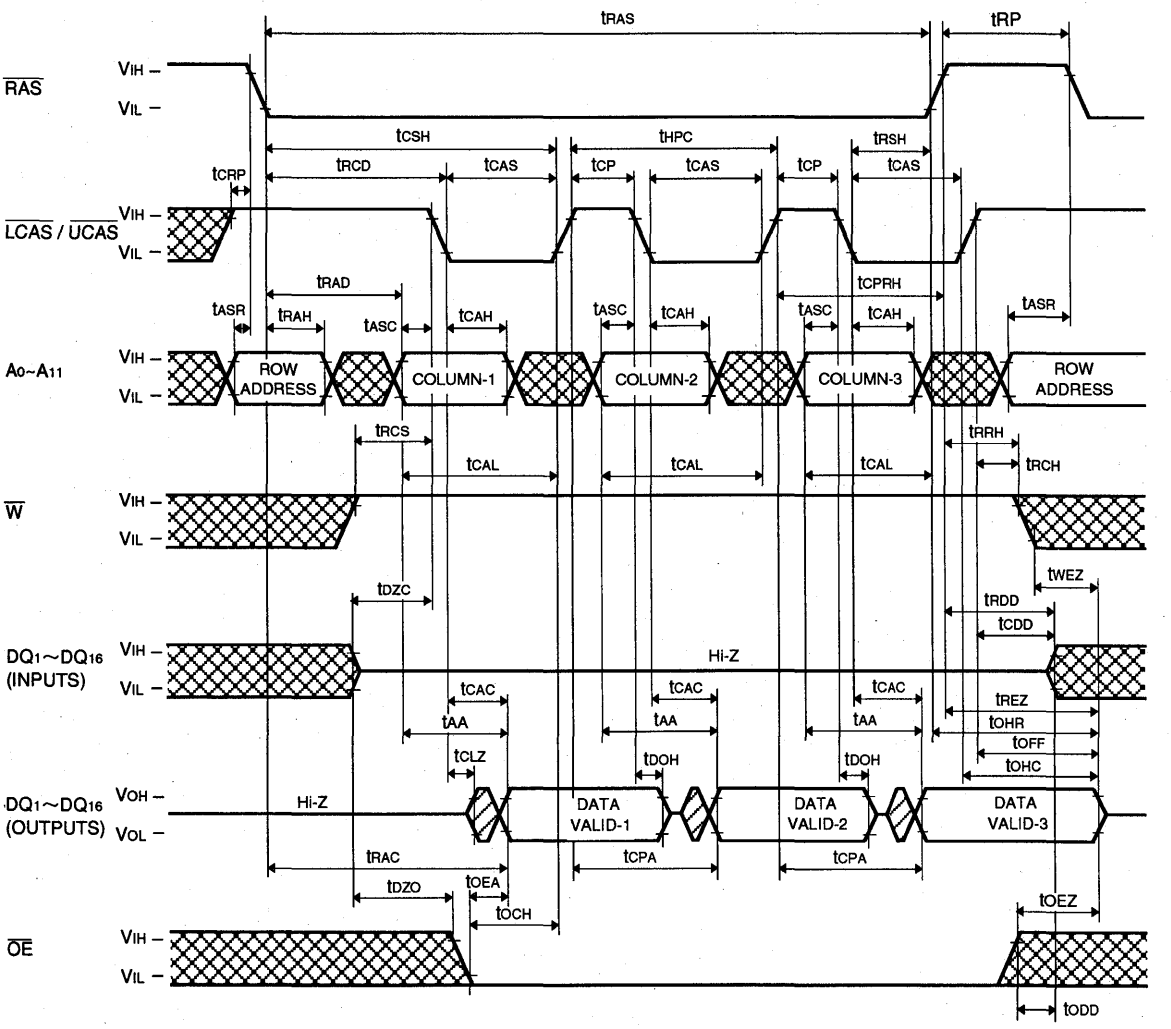


Byte Read-Write, Read-Modify-Write Cycle

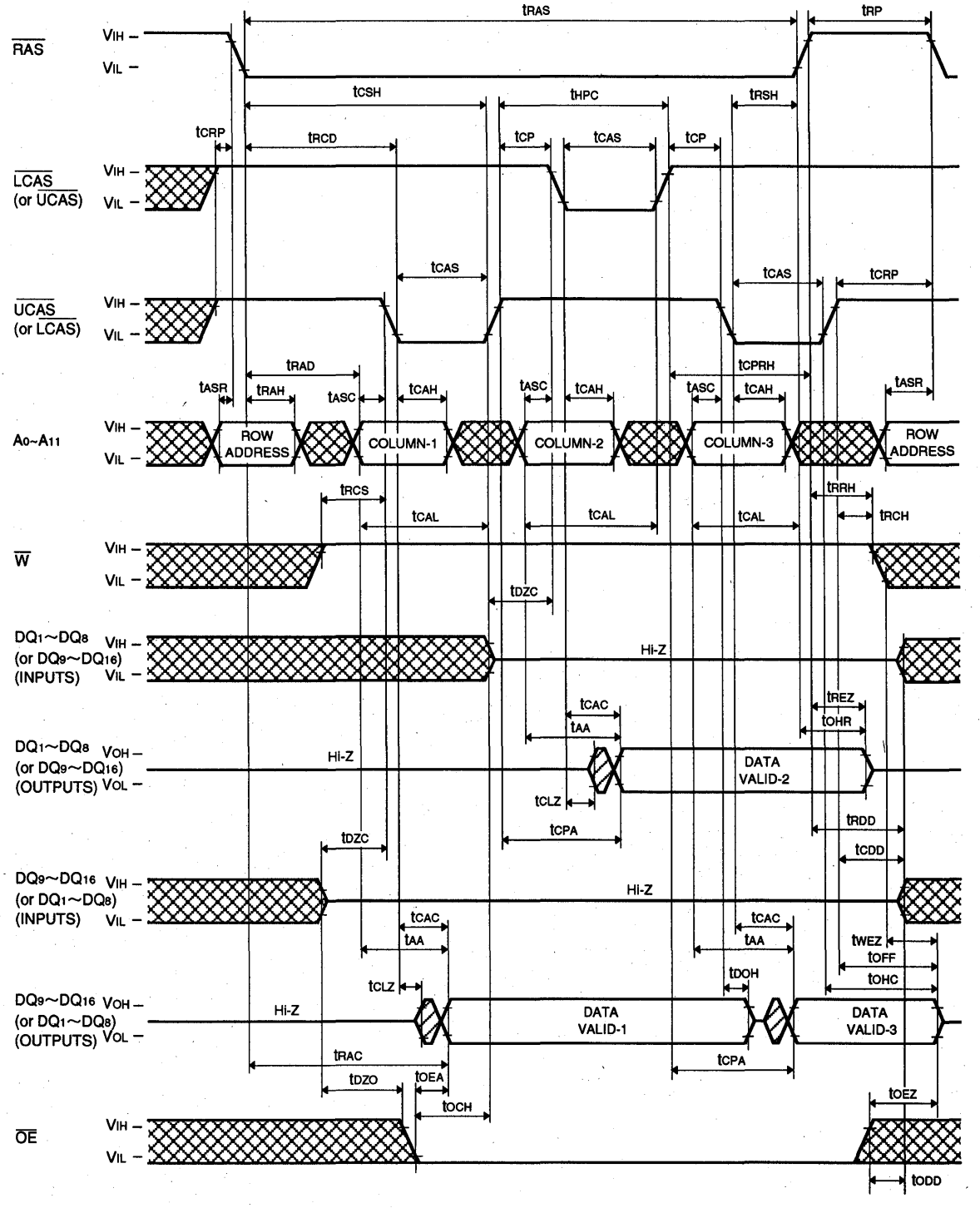


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle

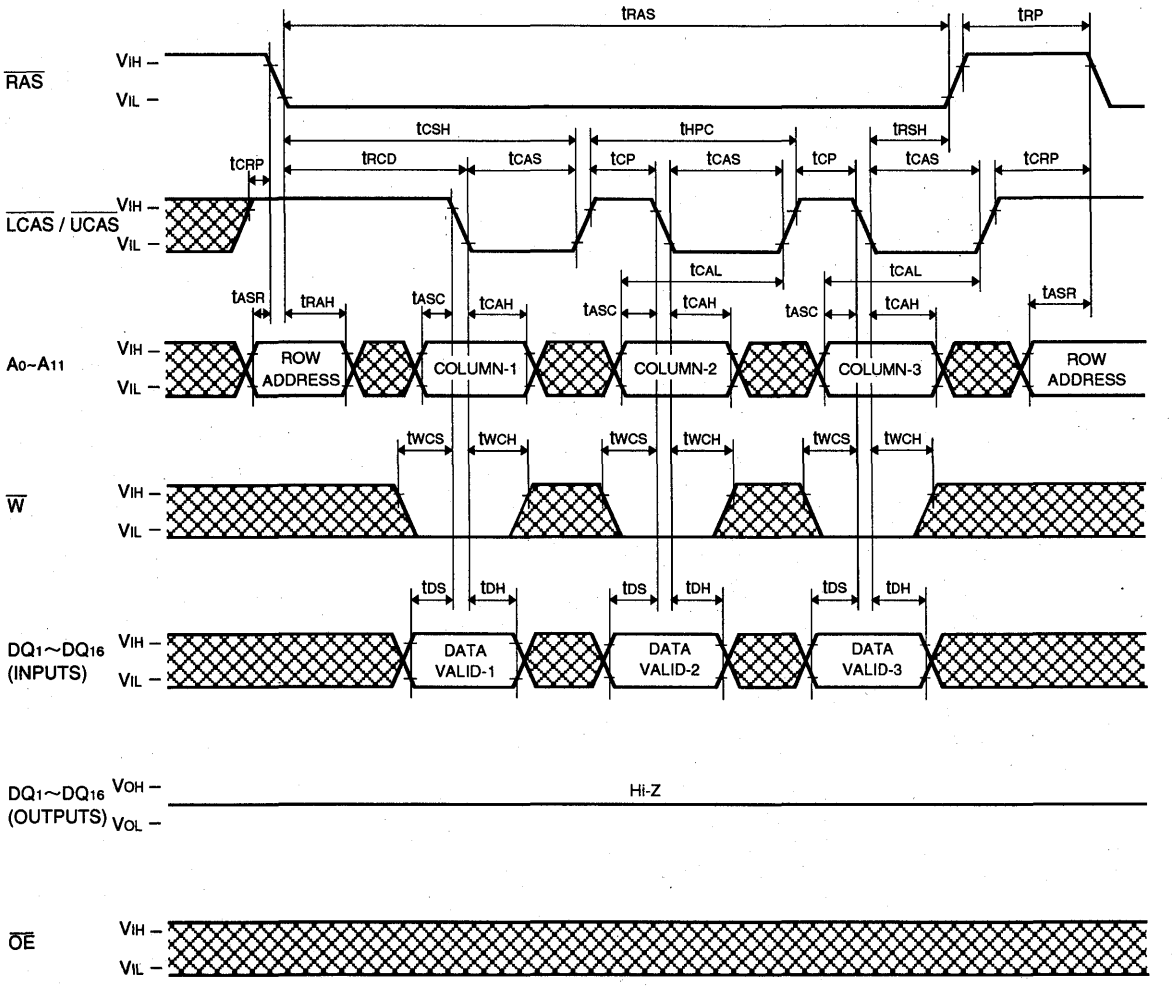


Hyper Page Mode Byte Read Cycle

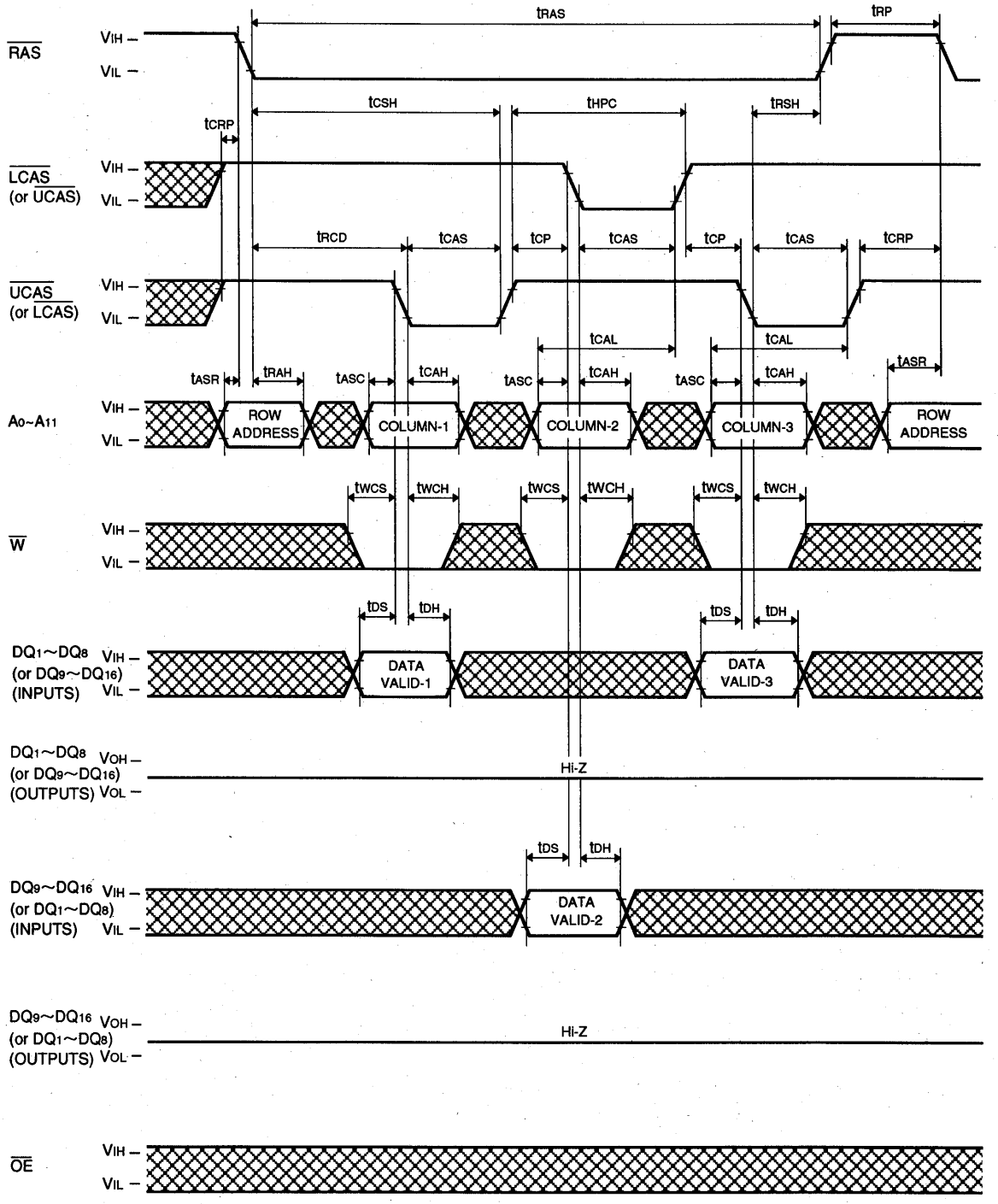


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Early Write Cycle

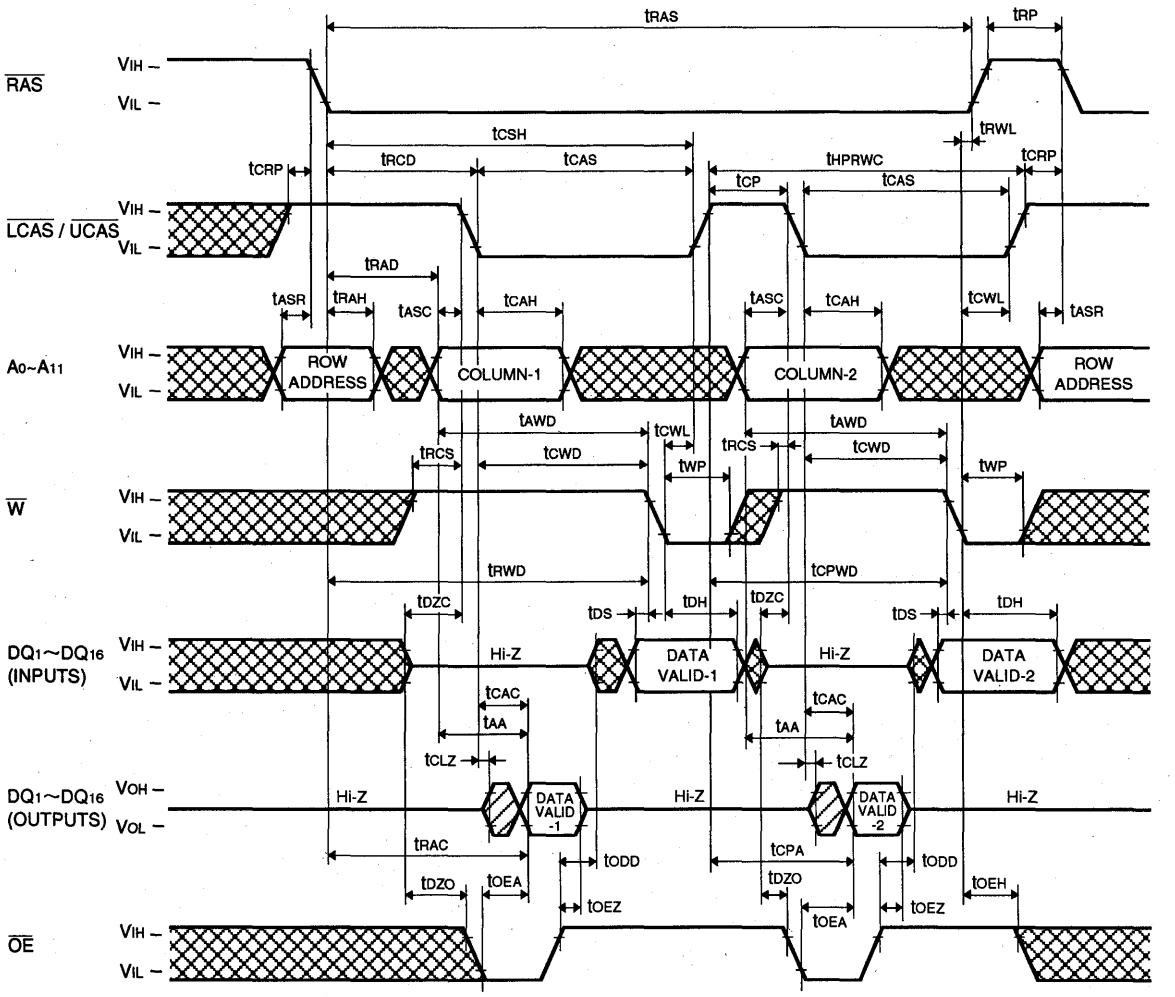


Hyper Page Mode Byte Early Write Cycle

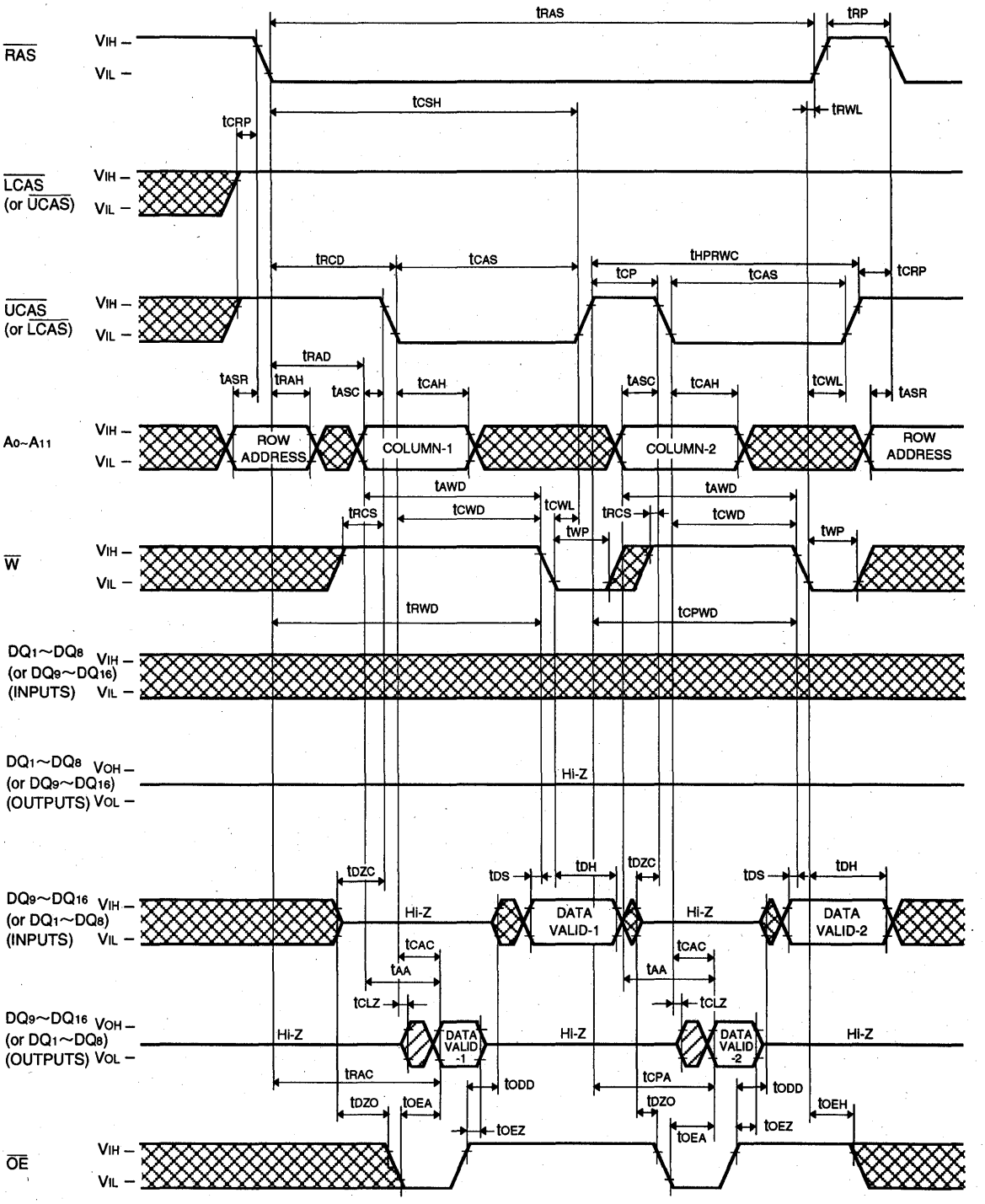


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read-Write, Read-Modify-Write Cycle

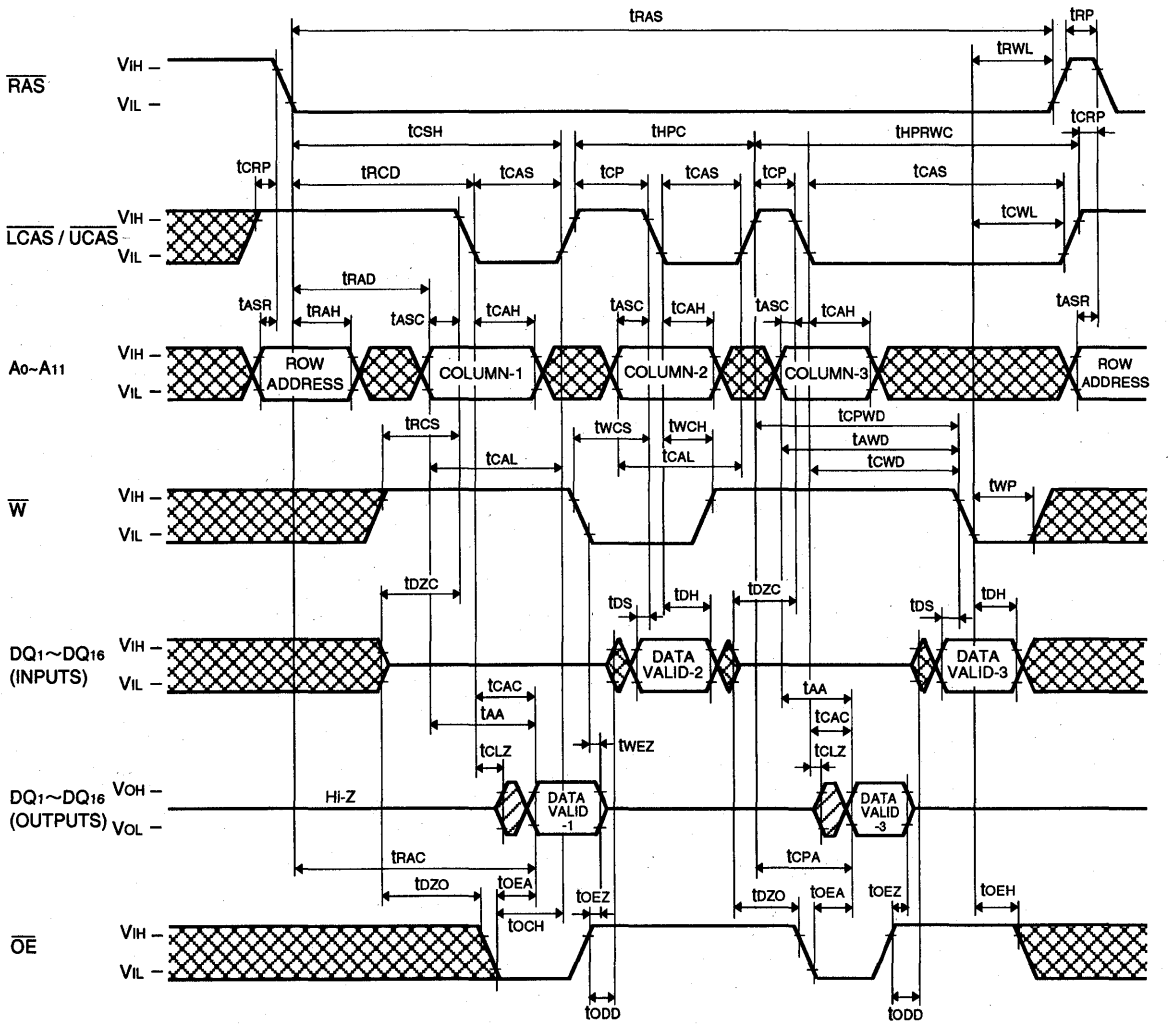


Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle

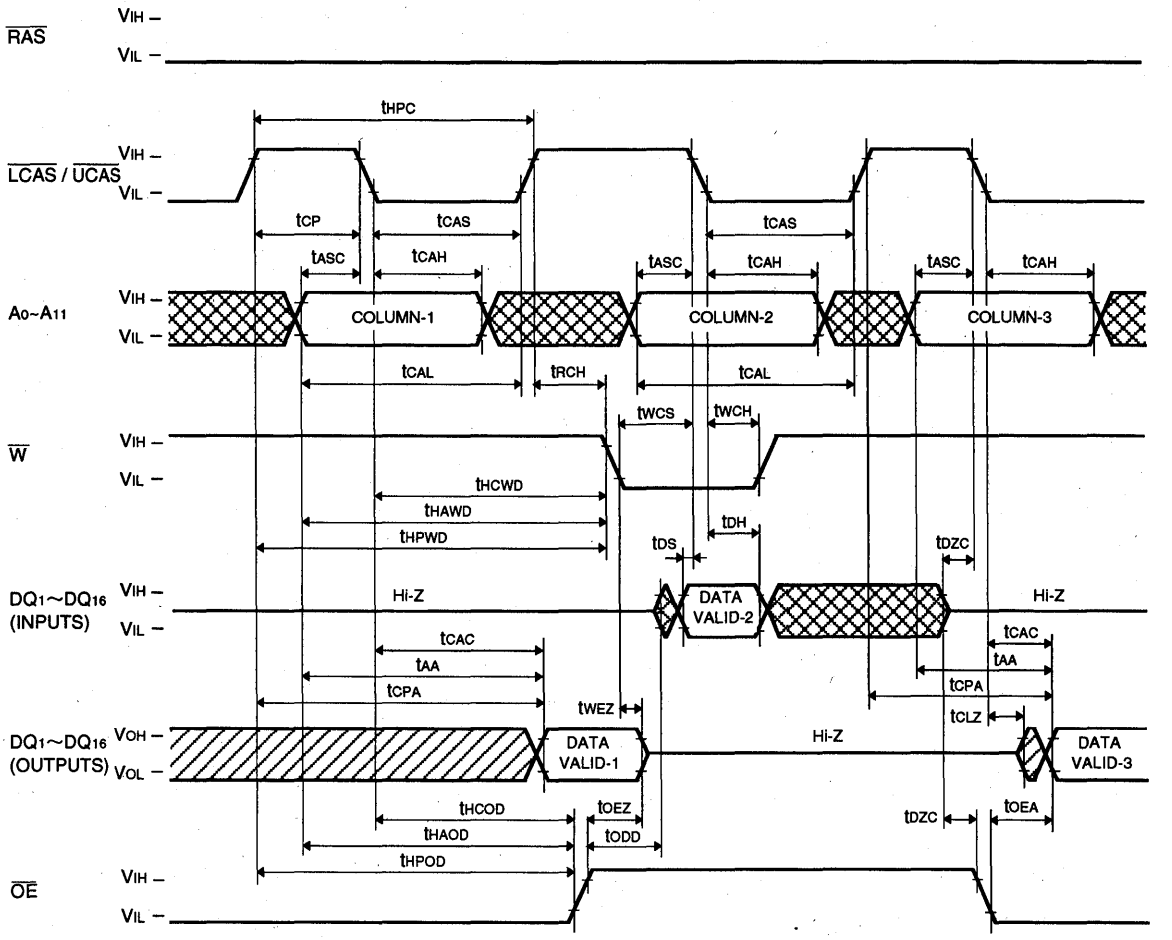


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (1)

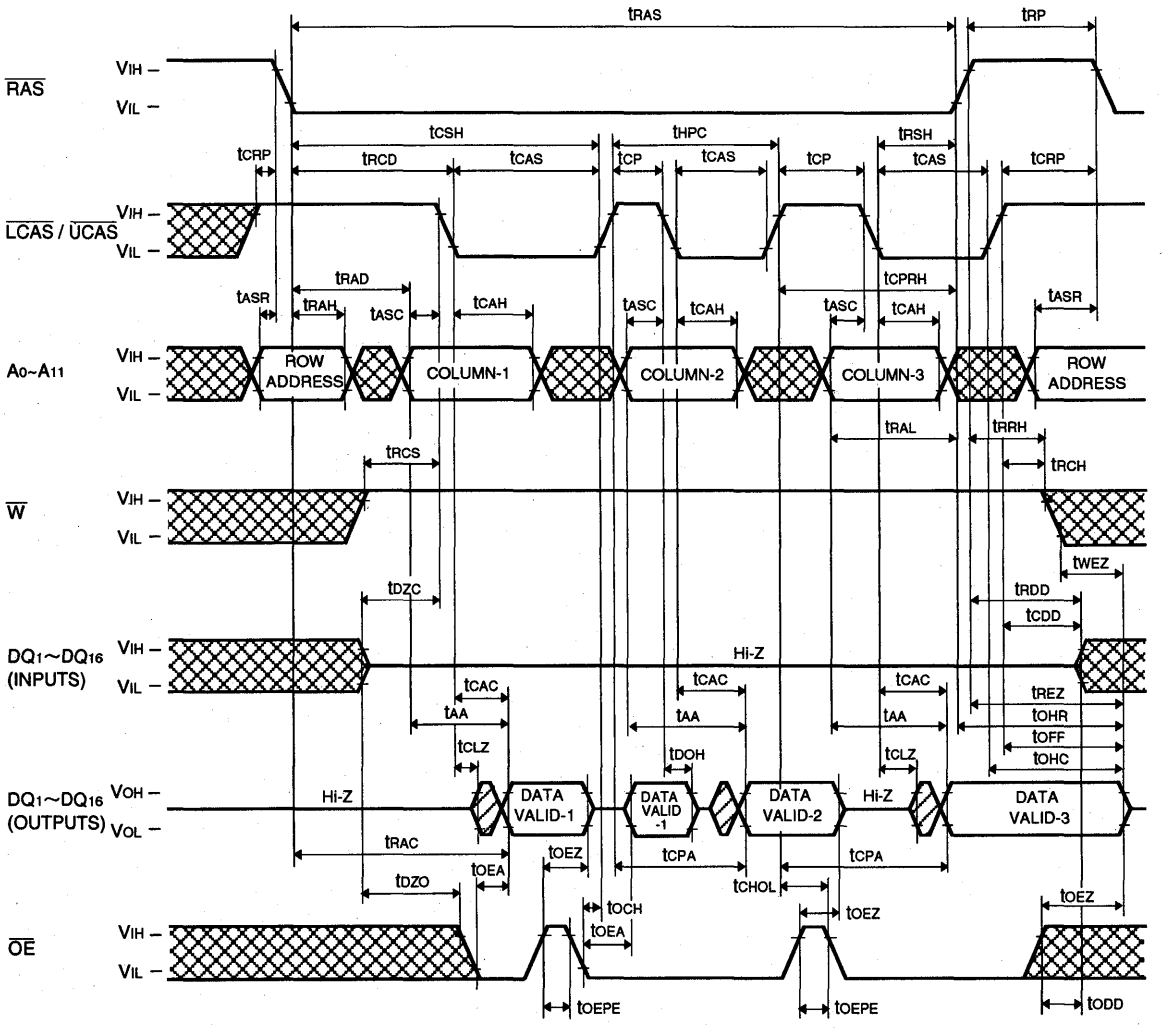


Hyper Page Mode Mix Cycle (2)

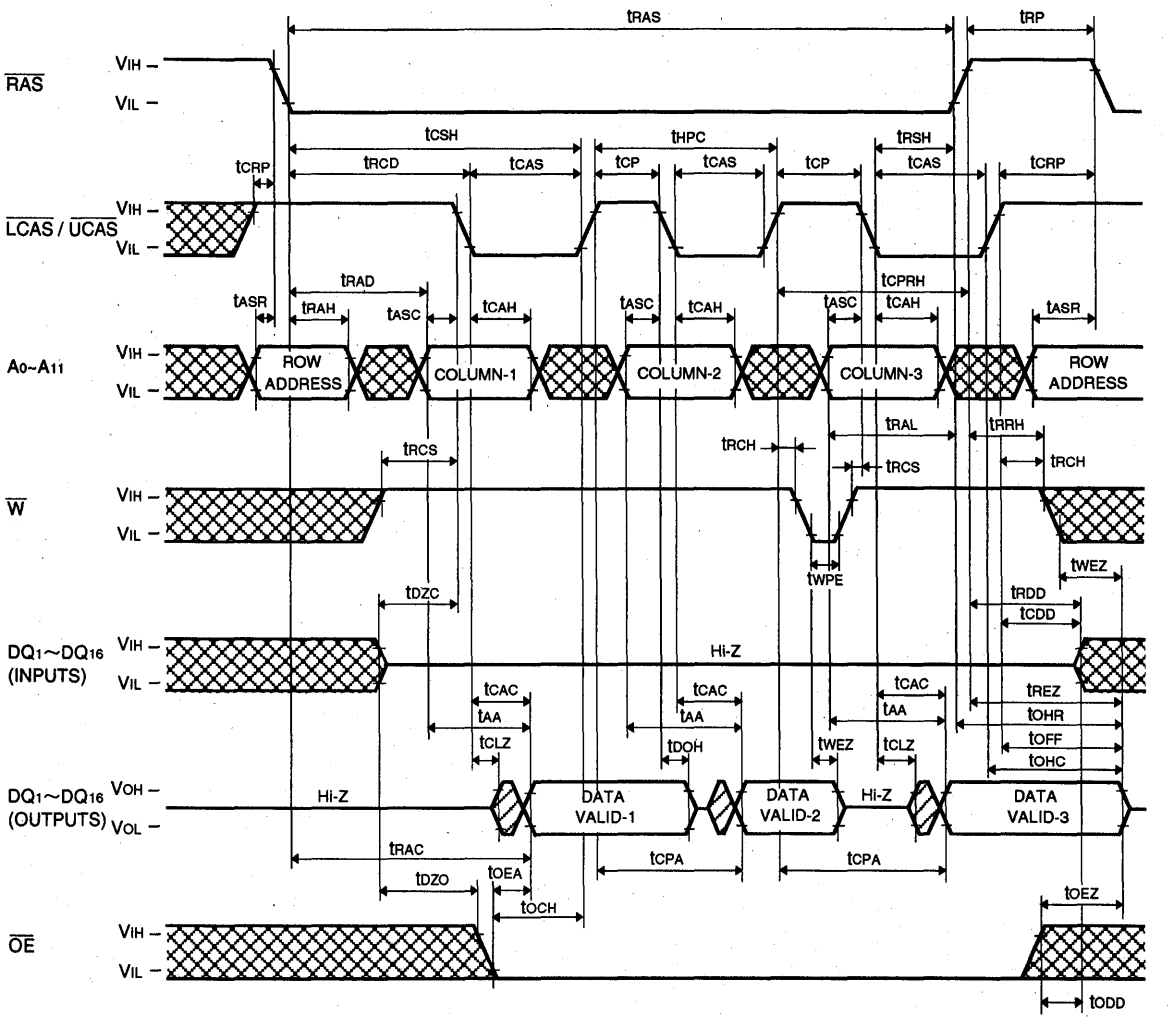


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

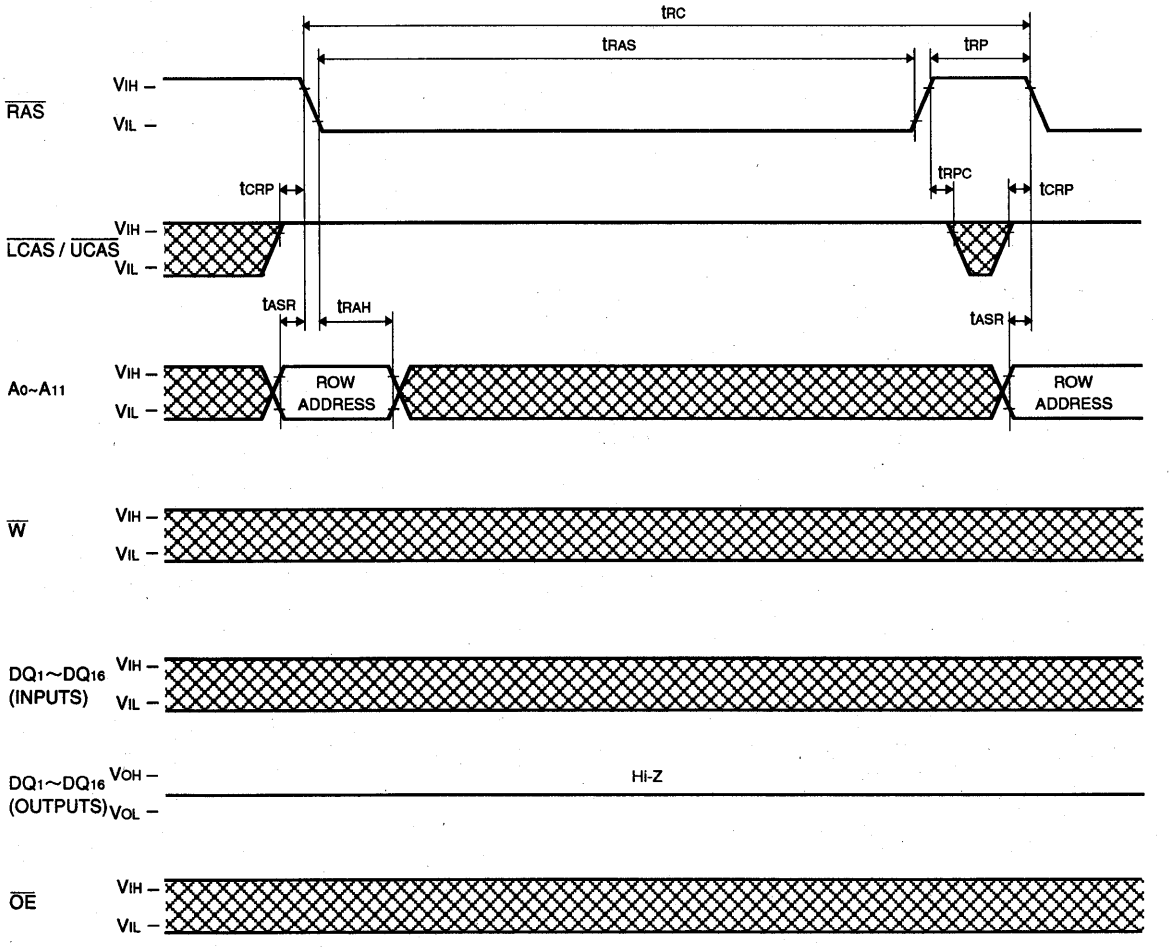
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



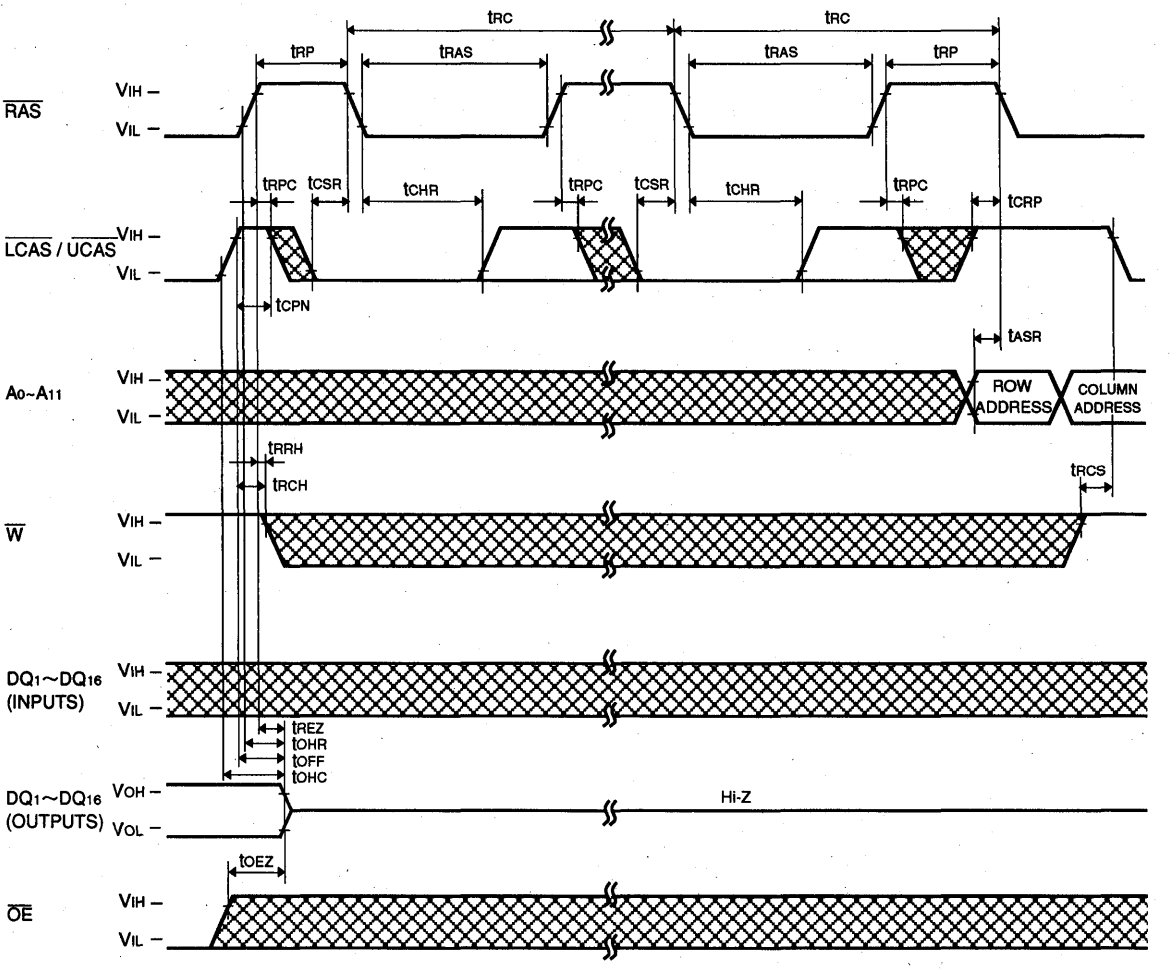
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



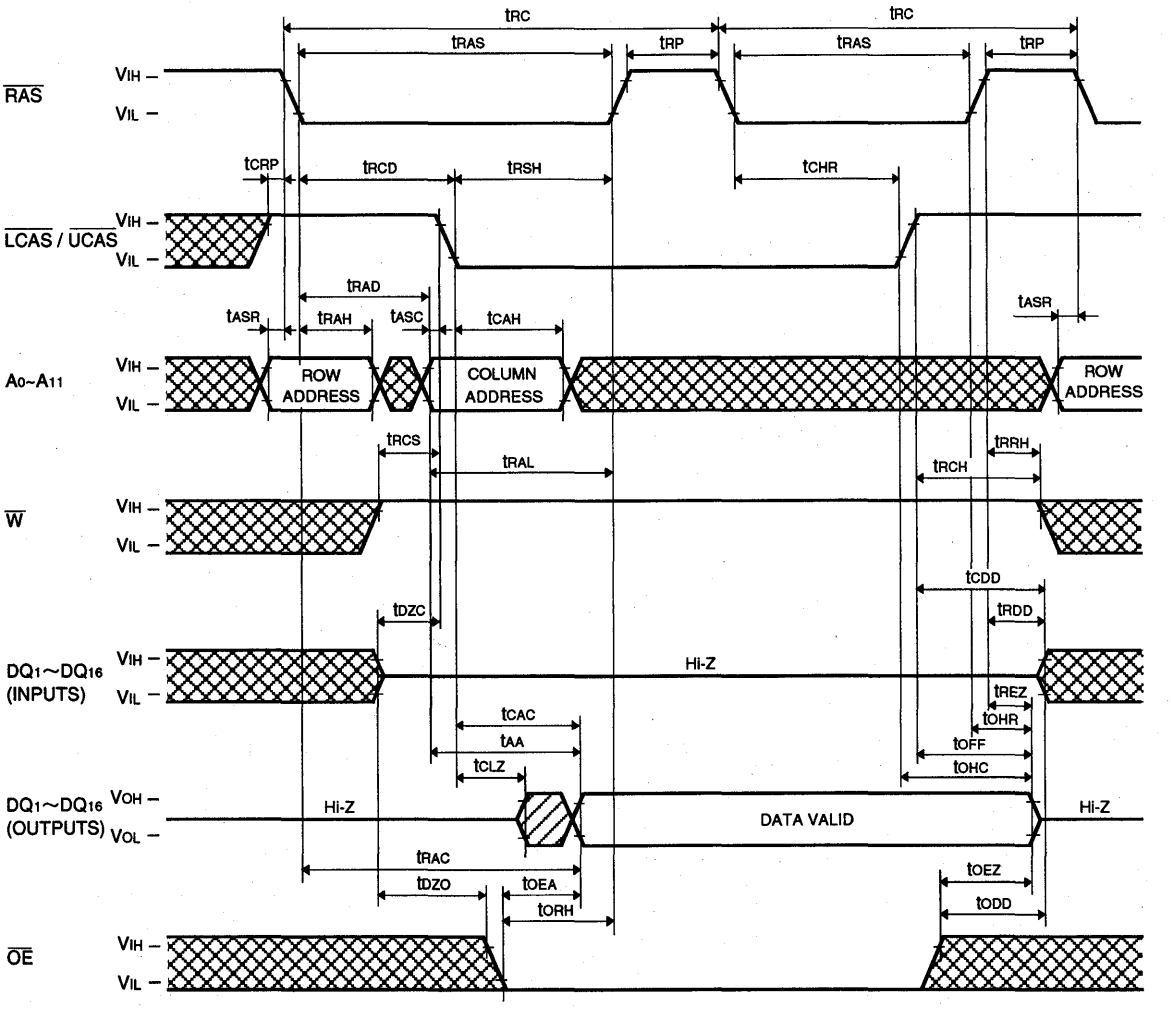
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

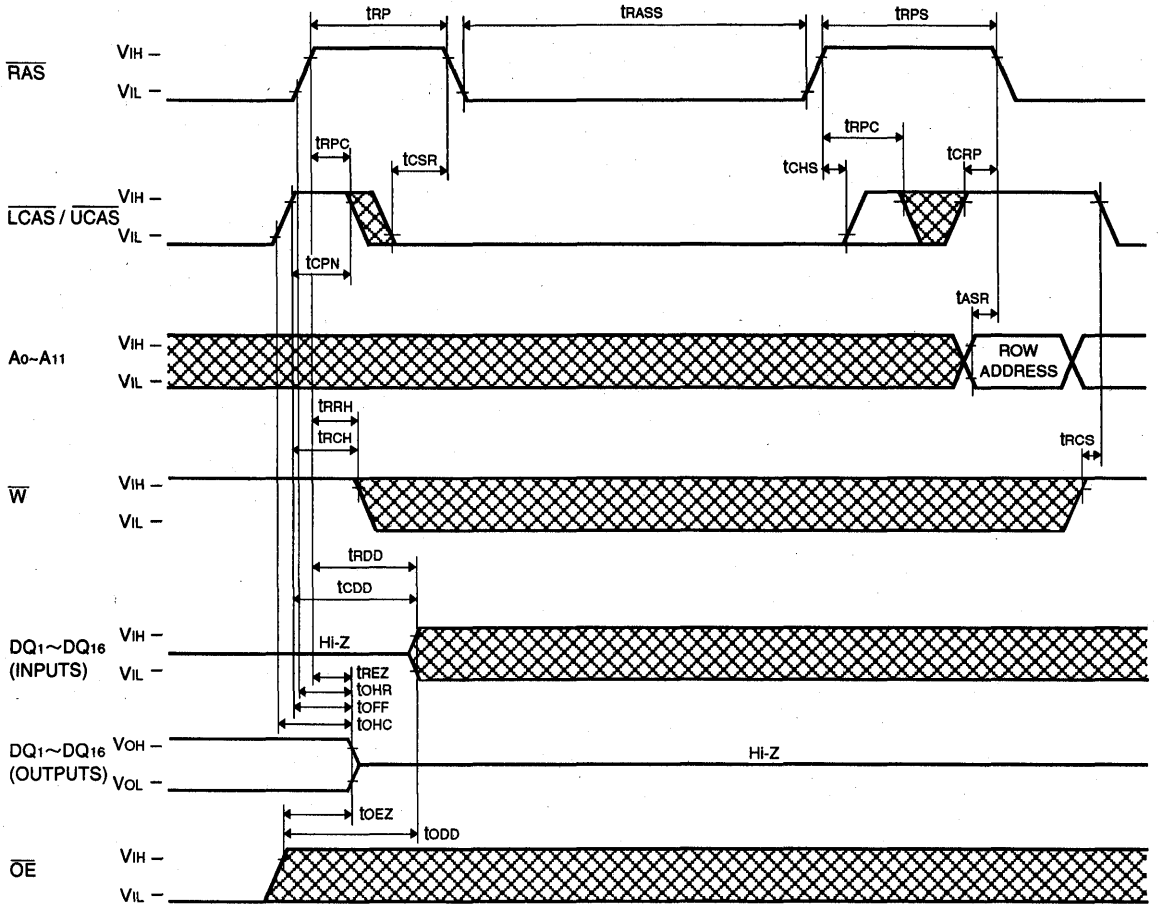


Hidden Refresh Cycle (Read) (Note 30)



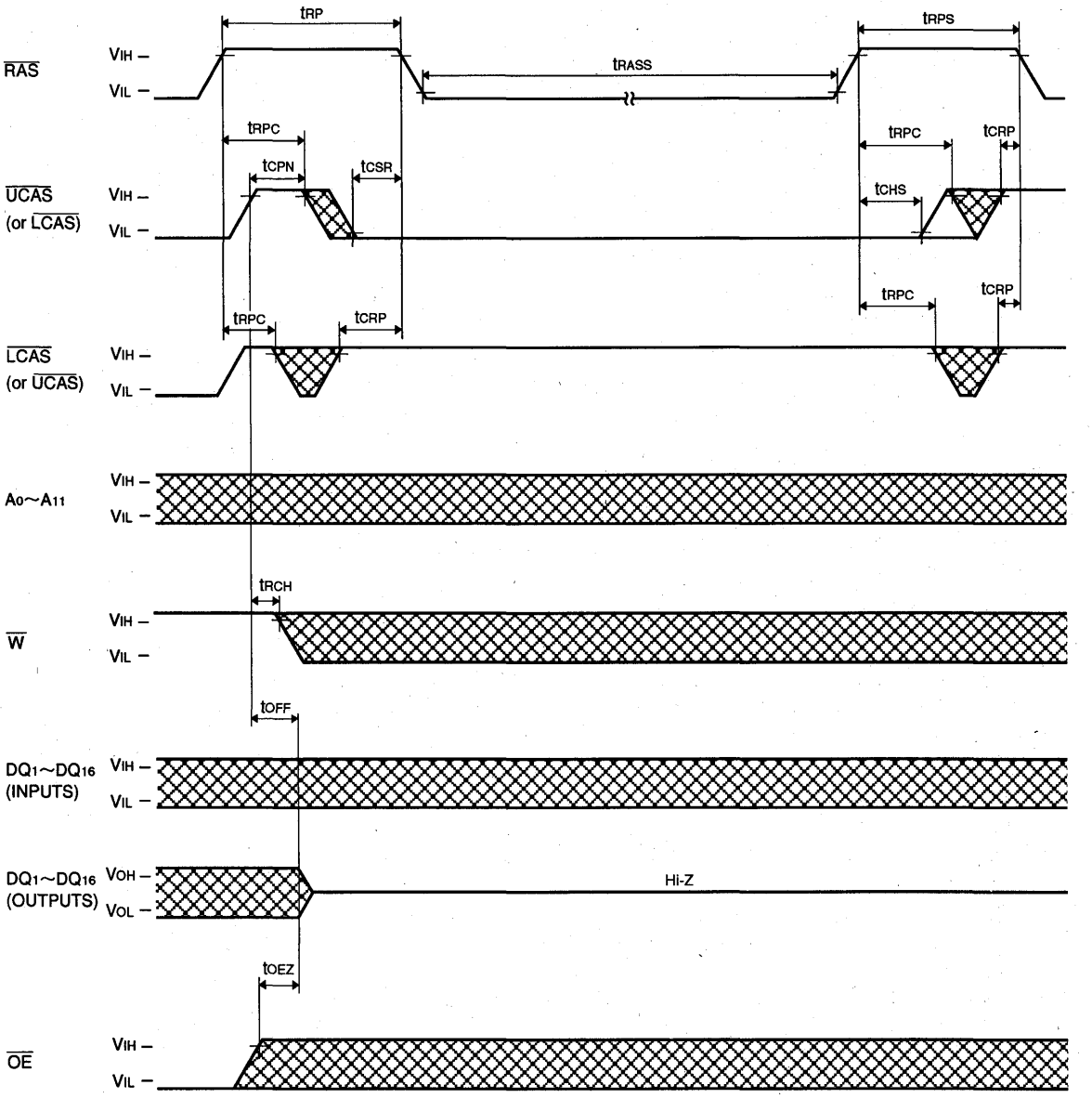
Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle *



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18165CTP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

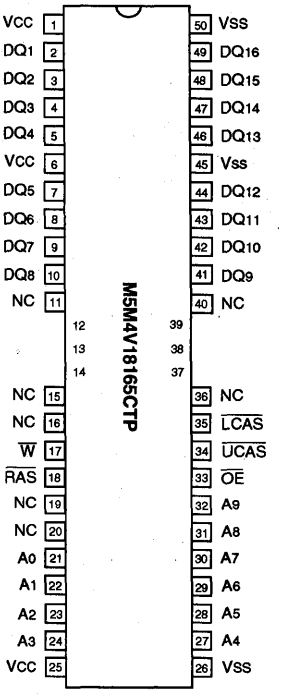
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18165CTP-5,-5S	50	13	25	13	90	540
M5M4V18165CTP-6,-6S	60	15	30	15	110	450
M5M4V18165CTP-7,-7S	70	20	35	20	130	390

- Standard 50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V18165CTP-5,-5S ---------- 650.0mW (Max)
  M5M4V18165CTP-6,-6S ---------- 540.0mW (Max)
  M5M4V18165CTP-7,-7S ---------- 470.0mW (Max)
- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  * : Applicable to self refresh version (M5M4V18165CTP-5S,-6S, -7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

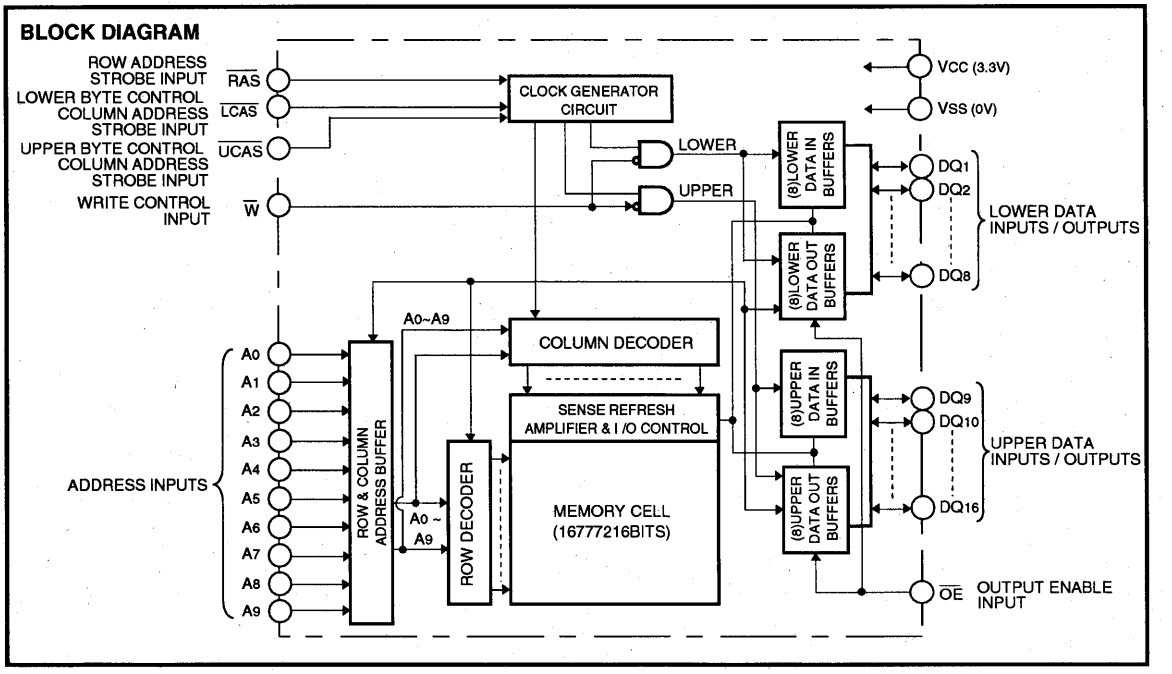
The M5M4V18165CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25 °C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M4V18165C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V18165C-6,-6S				150	
		M5M4V18165C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧V_{CC} -0.2V output open			0.5	
						0.15 *	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M4V18165C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M4V18165C-6,-6S				150	
		M5M4V18165C-7,-7S				130	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M4V18165C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			165	mA
		M5M4V18165C-6,-6S				130	
		M5M4V18165C-7,-7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18165C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M4V18165C-6,-6S				150	
		M5M4V18165C-7,-7S				130	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-refresh cycle (Note 6)	M5M4V18165C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0~A9≦0.2V or ≧Vcc-0.2V DQ=open, t_{RC}=125 μs, t_{RAS}=t_{RAS}min~1 μs			300	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-refresh cycle	M5M4V18165C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±3.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 12)	0	13	0	15	0	20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	13	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA) / V_{OL}=0.4V(I_{OL}=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$. and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$,$t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\,\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4	ms
t_{REF}*	Refresh cycle time			128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 16)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		8		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 19)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 19)	0		0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data	(Note 20)	13		15		20		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 20)	13		15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 20)	13		15		20		ns
t_T	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 22)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		35		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time		13		18		23		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	8		10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	8		10		13		ns
t_{WP}	Write pulse width	8		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 23)	109		133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width	75	10000	89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	38	10000	44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	38		44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 24)	28		32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 24)	65		77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 24)	40		47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	20		25		30		ns
t_{HPRWC}	Hyper page mode read write/read modify write cycle time	57		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 26)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 27)	8	13	10	16	10	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	45		52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, address to $\overline{W}$ low after read	52		62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	62		72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M4V18165C-5,-5S		M5M4V18165C-6,-6S		M5M4V18165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

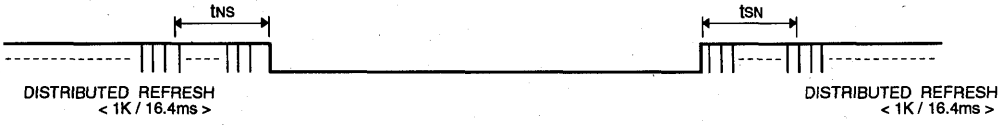
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18165C-5S		M5M4V18165C-6S		M5M41V8165C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

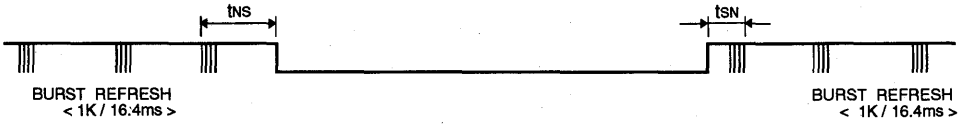
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦16.4ms and tSN≦16.4ms.



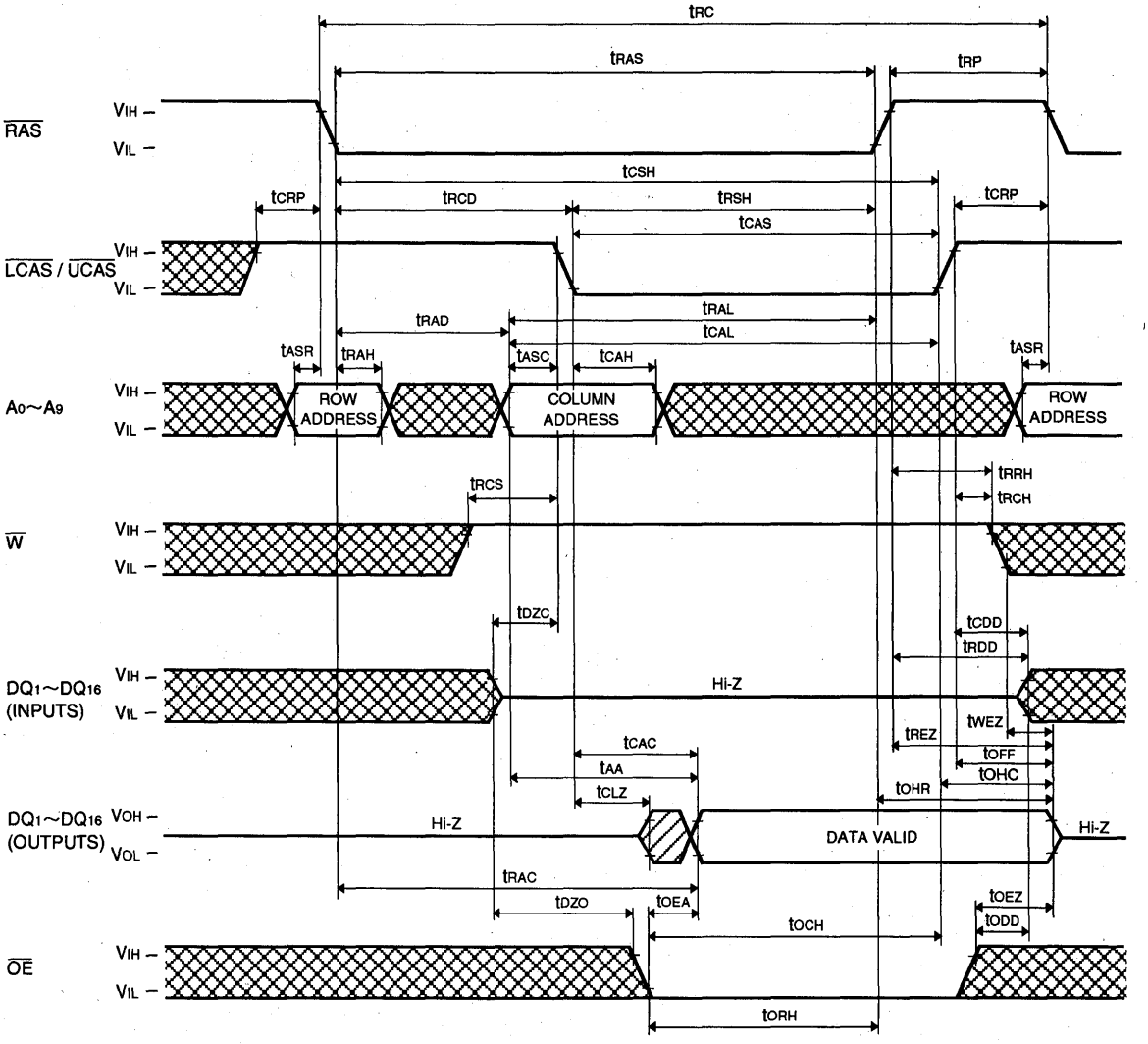
(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦16.4ms.



Timing Diagrams (Note 29)

Read Cycle



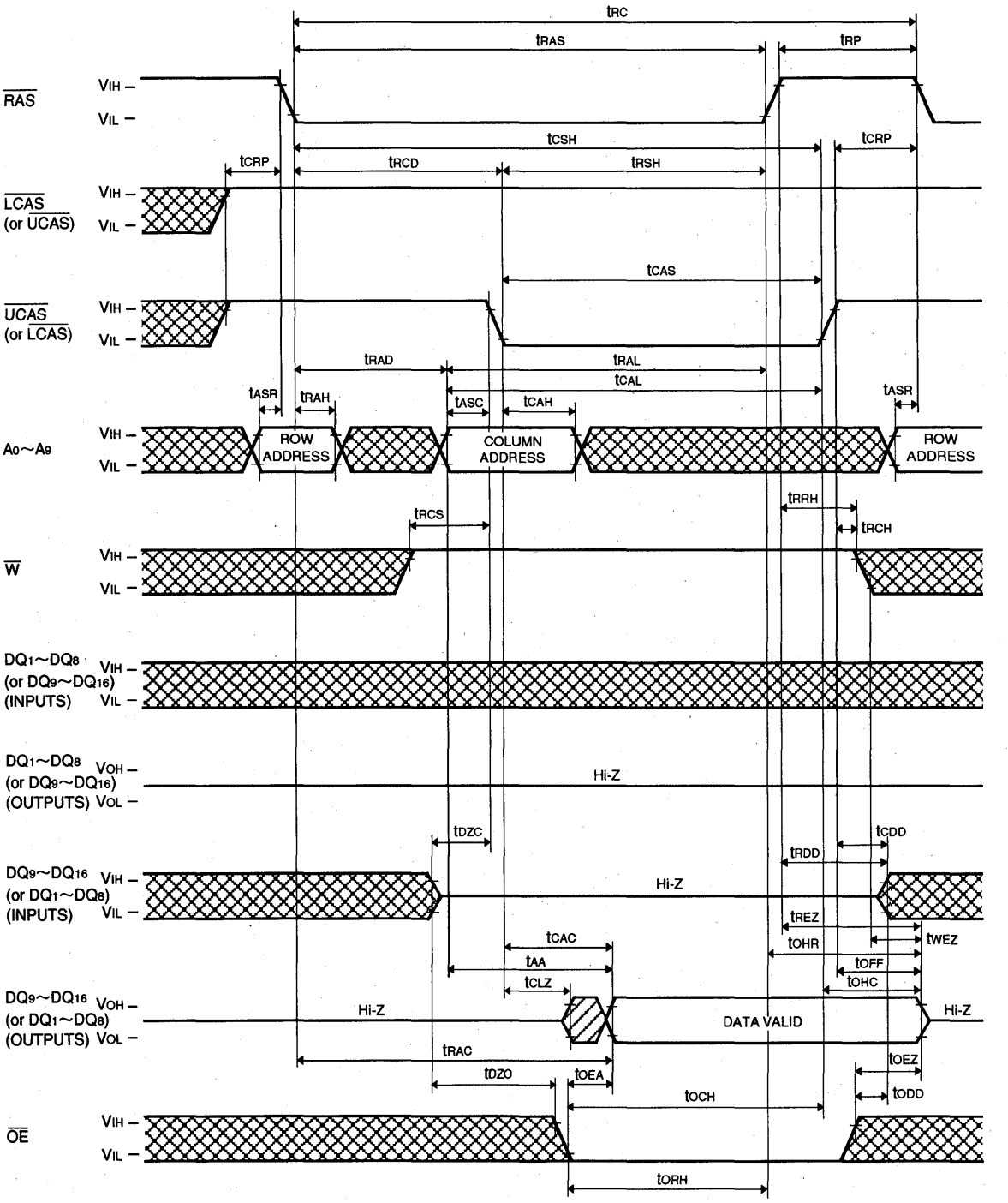
Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

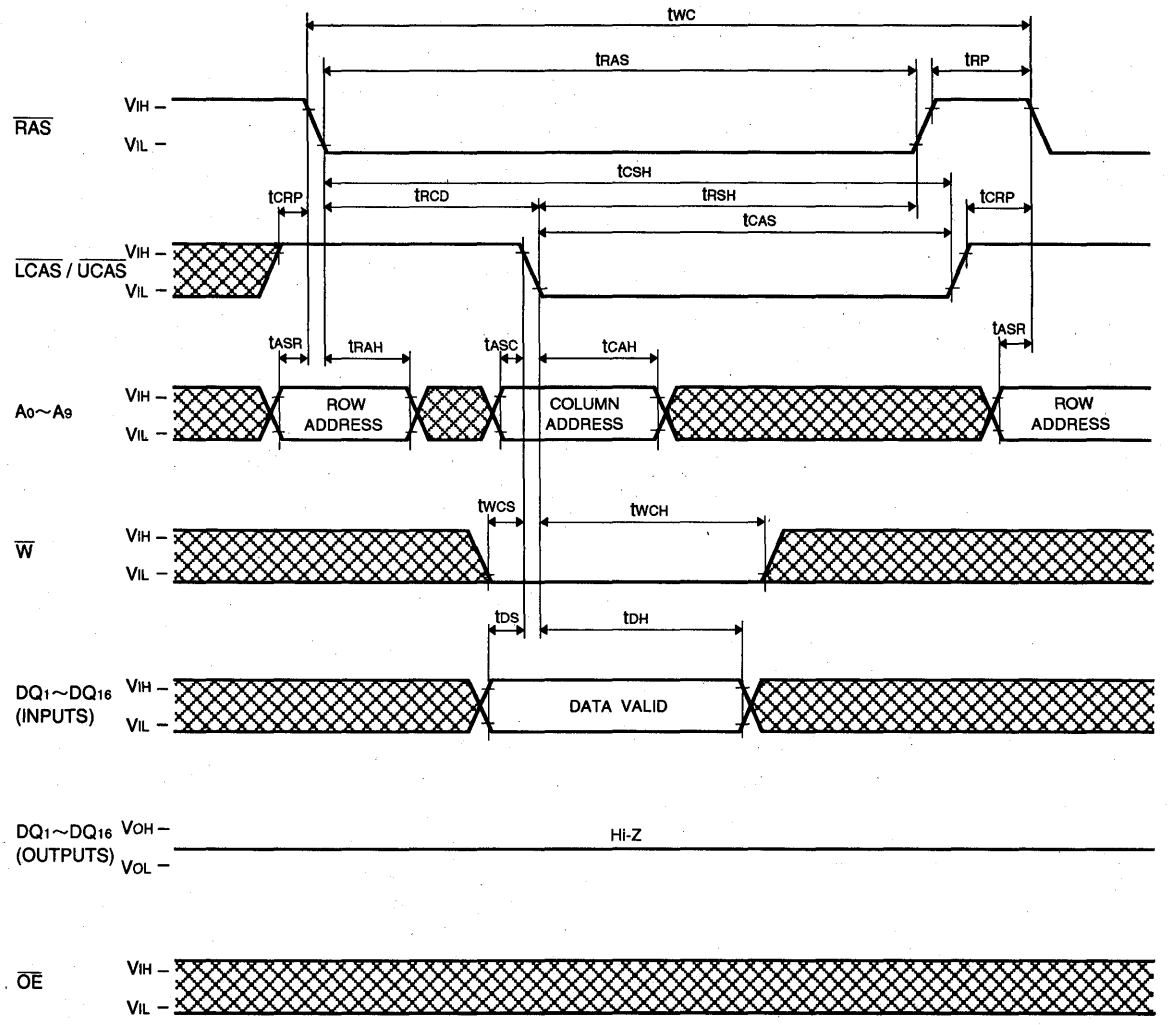
Indicates the invalid output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Read Cycle

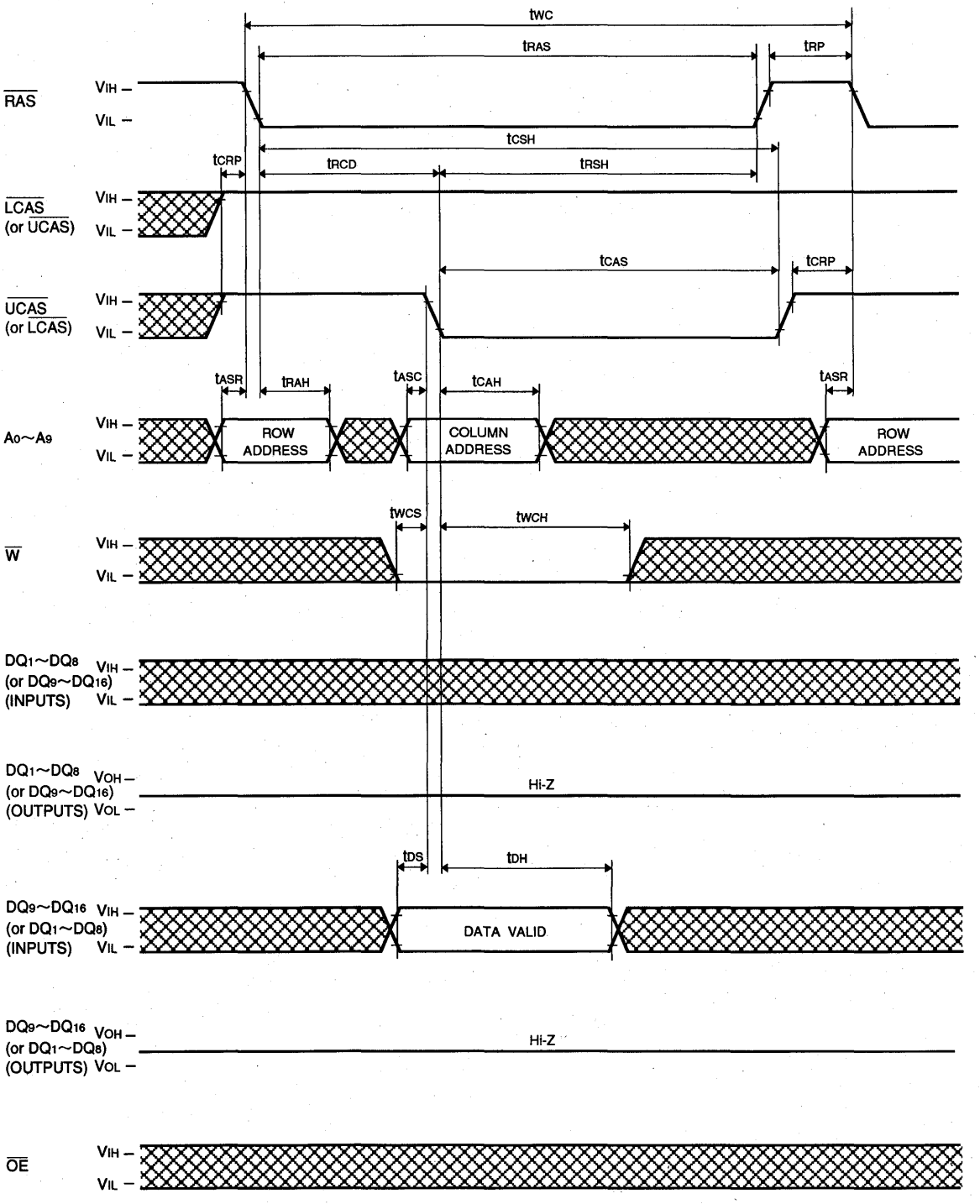


Early Write Cycle



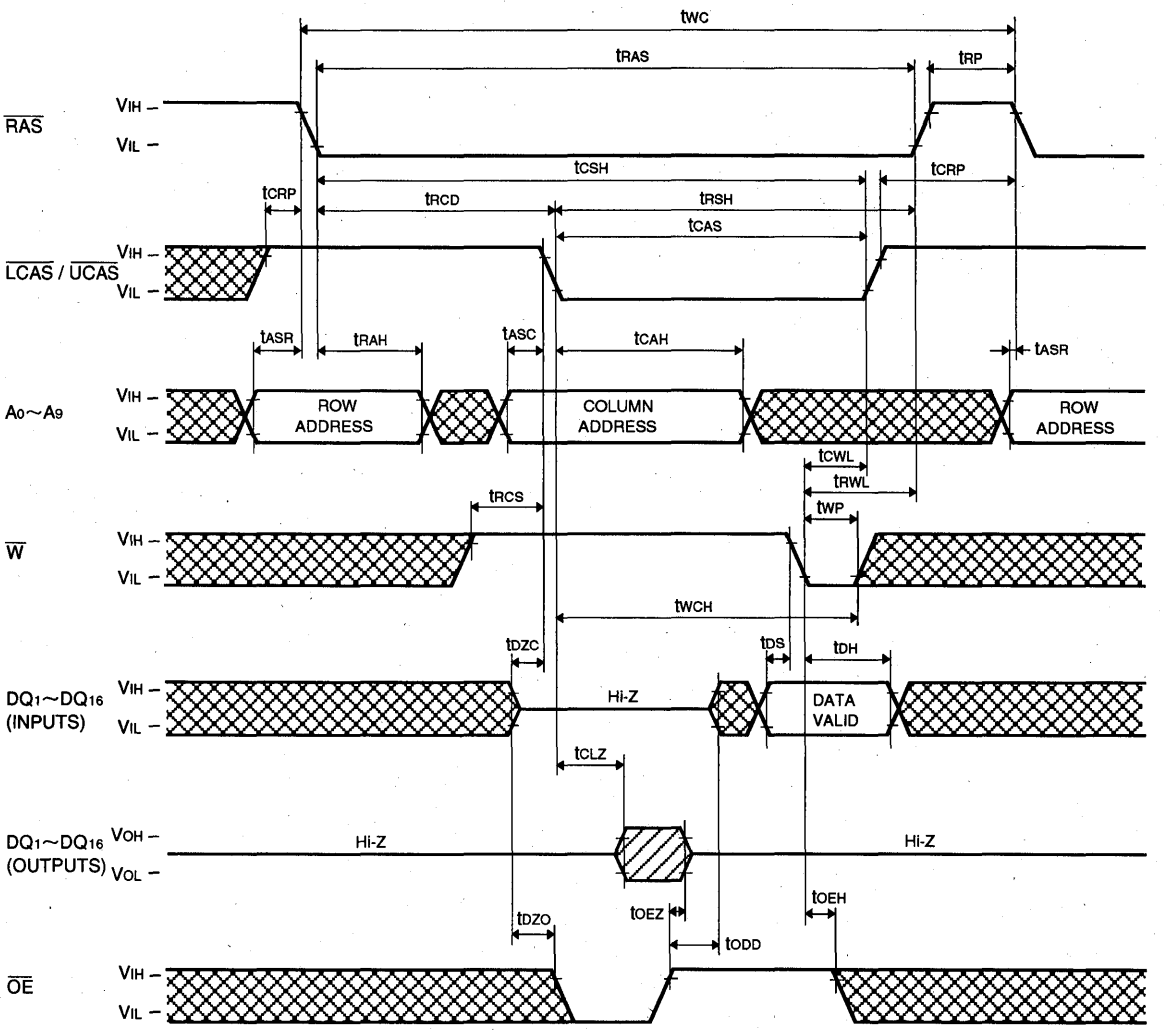
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Byte Early Write Cycle



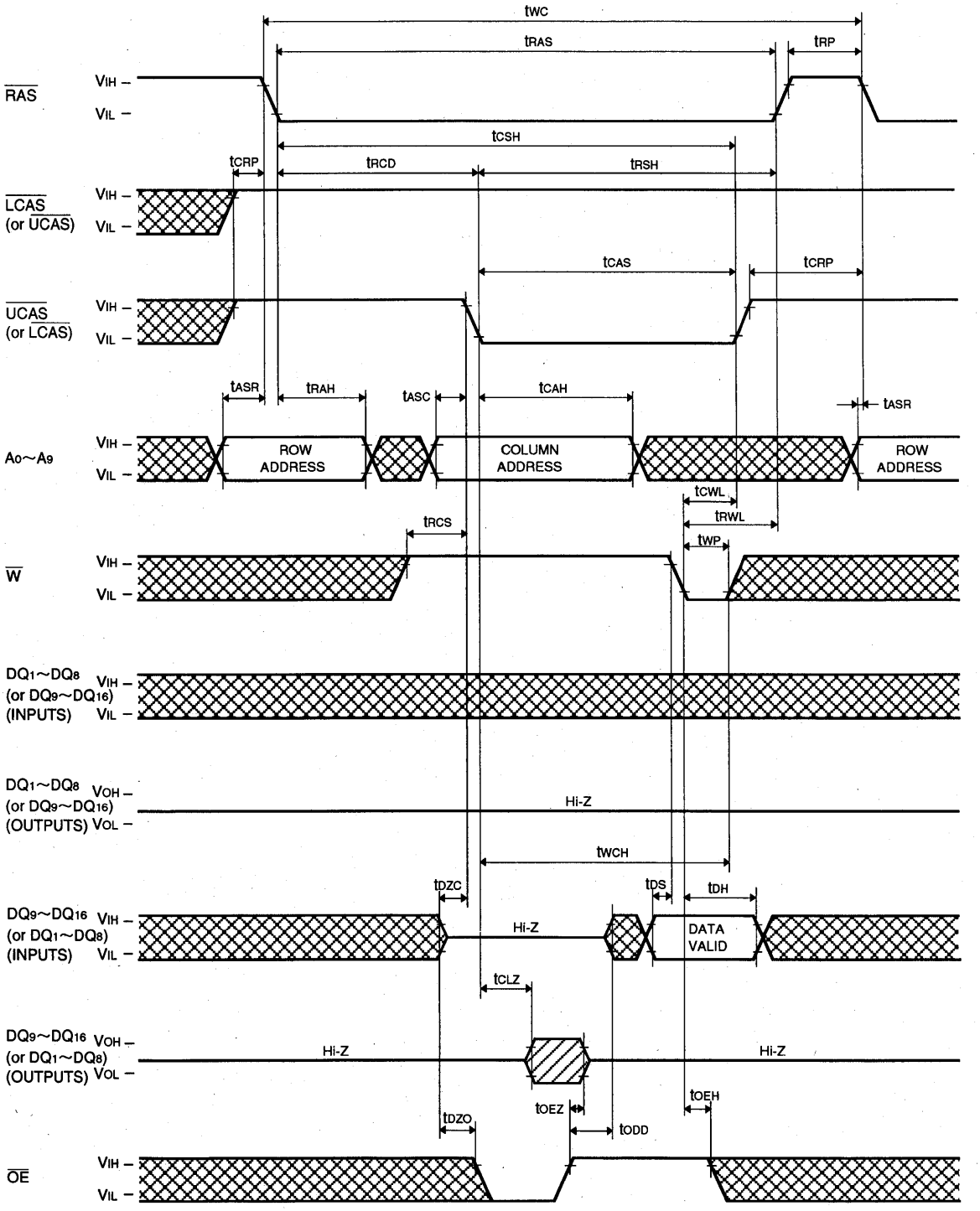
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Delayed Write Cycle

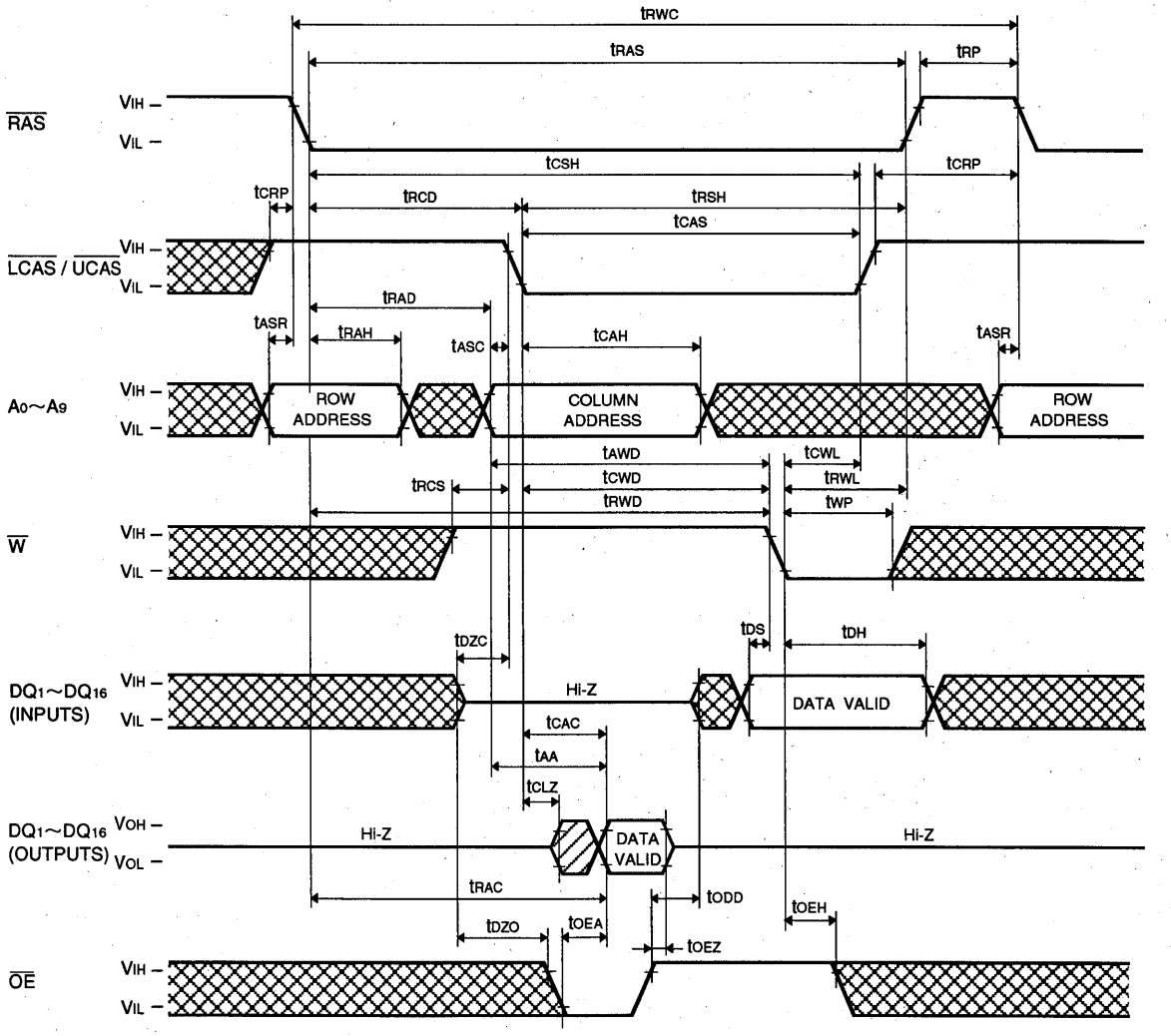


MITSUBISHI ELECTRIC

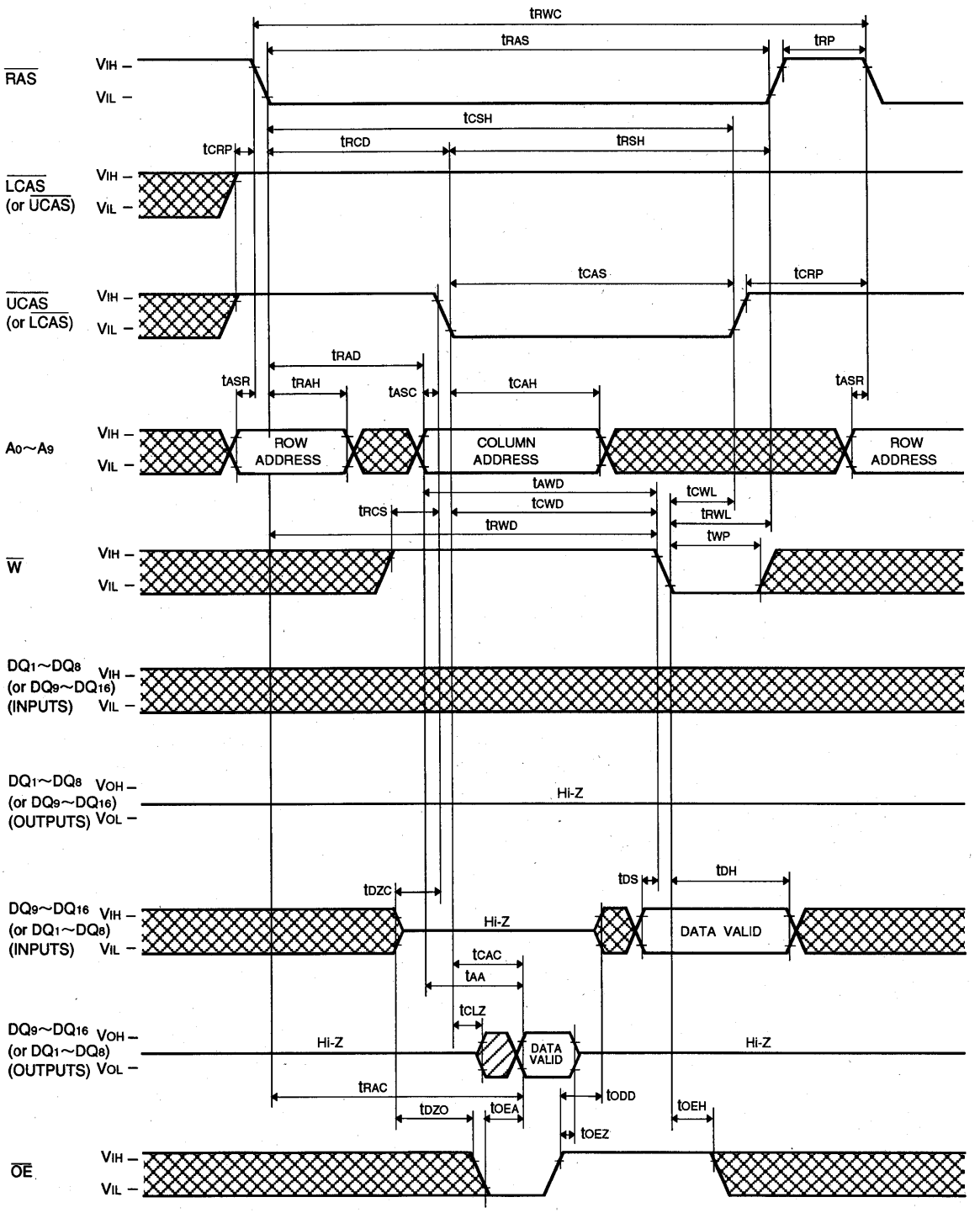
Byte Delayed Write Cycle



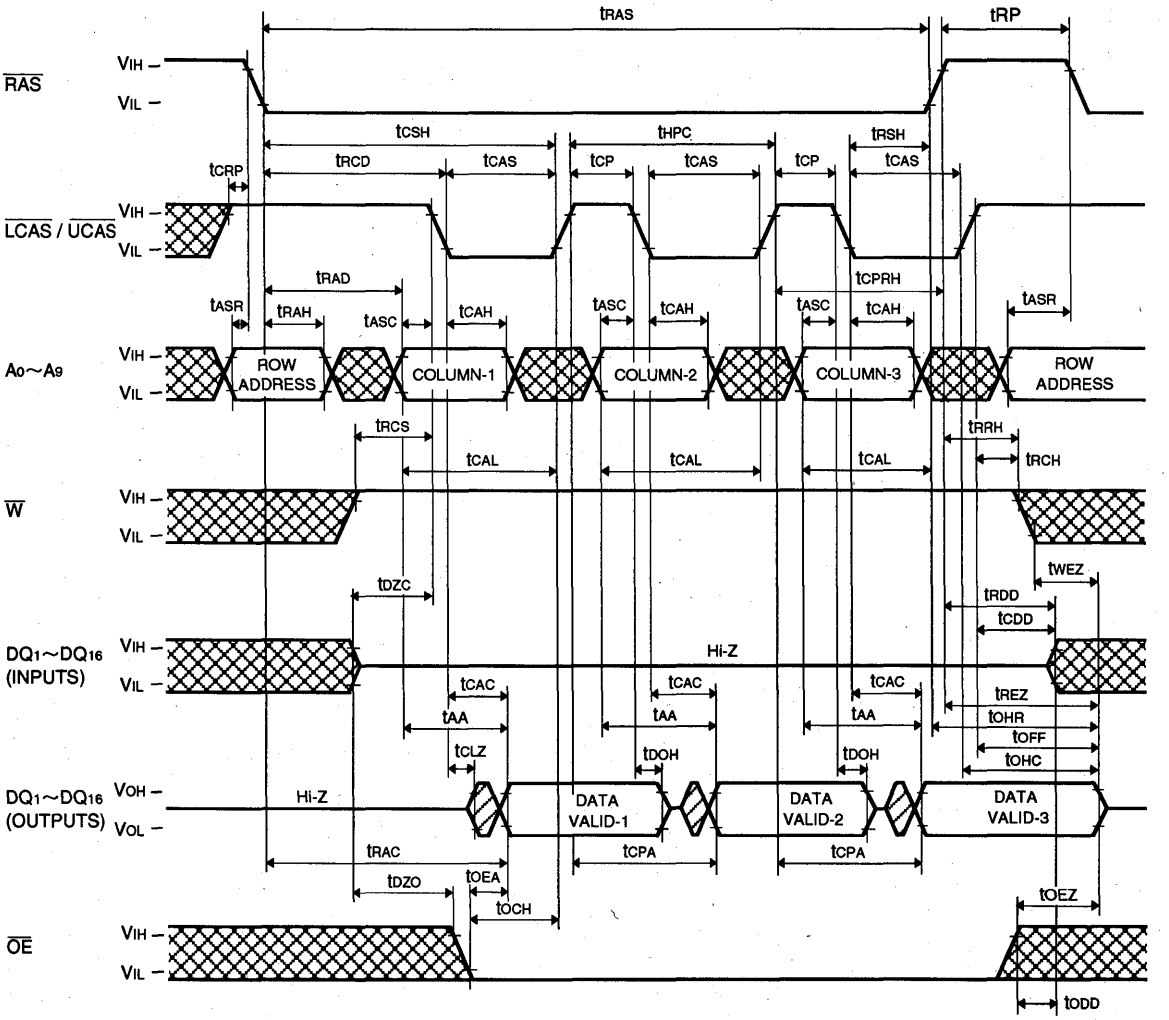
Read-Write, Read-Modify-Write Cycle



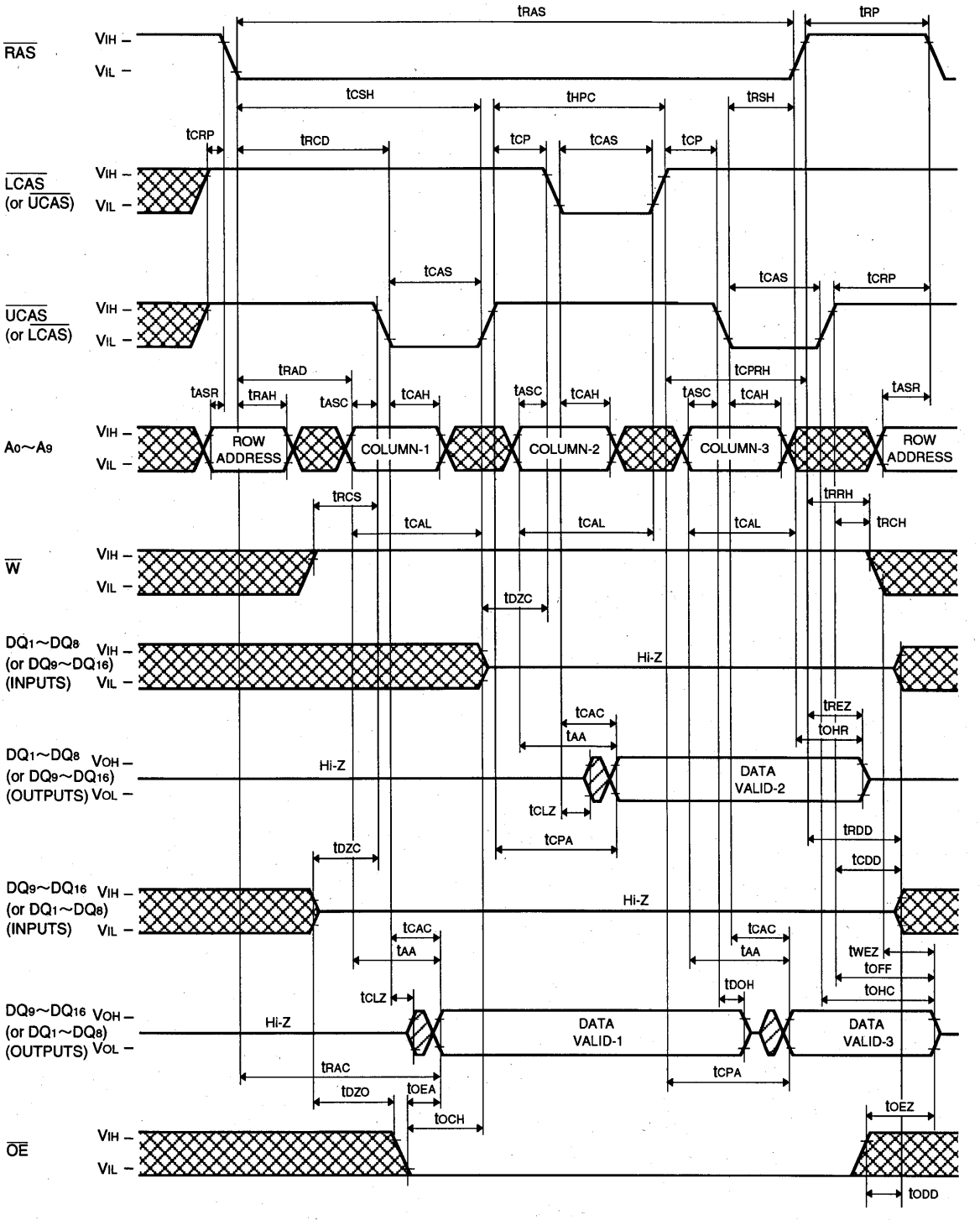
Byte Read-Write, Read-Modify-Write Cycle



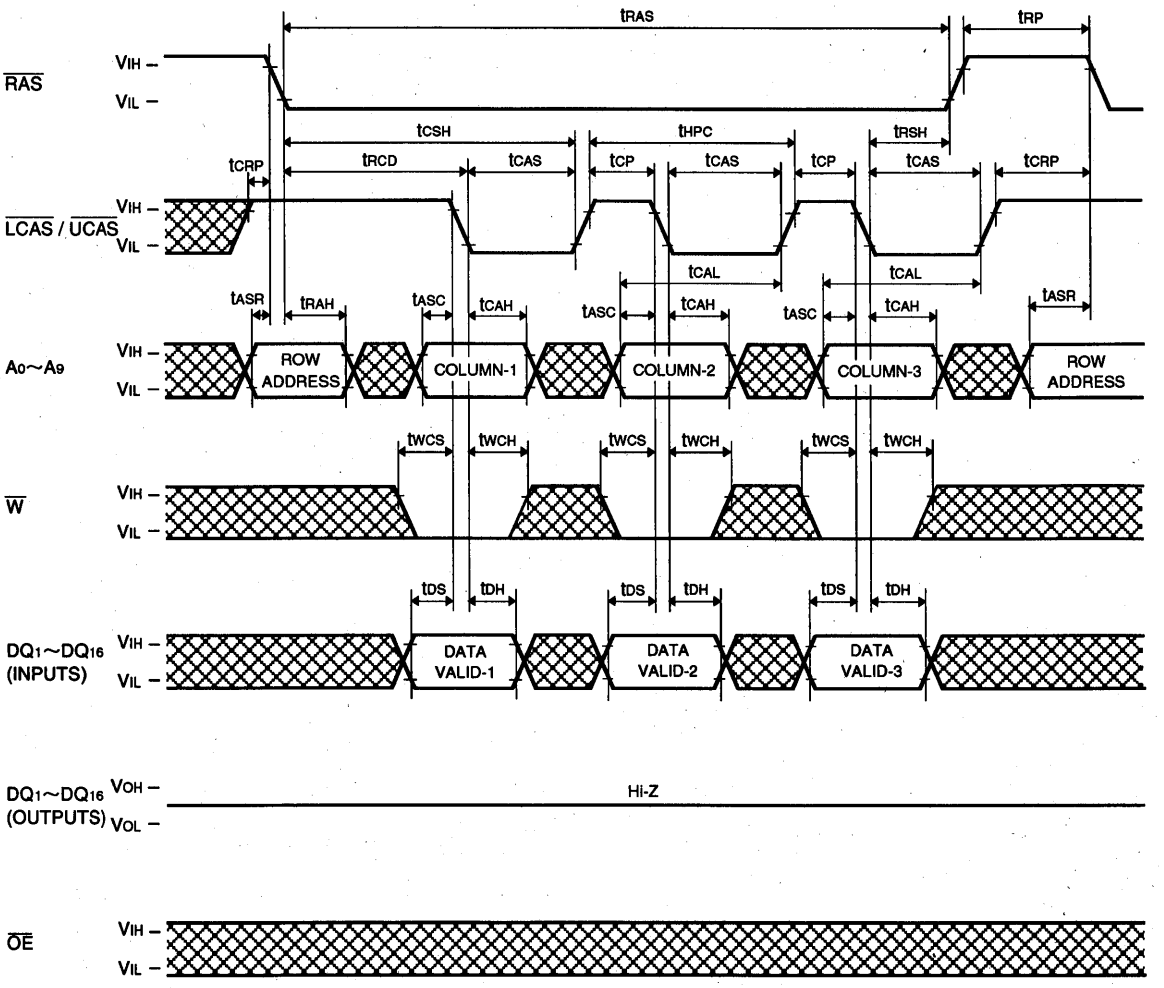
Hyper Page Mode Read Cycle



Hyper Page Mode Byte Read Cycle

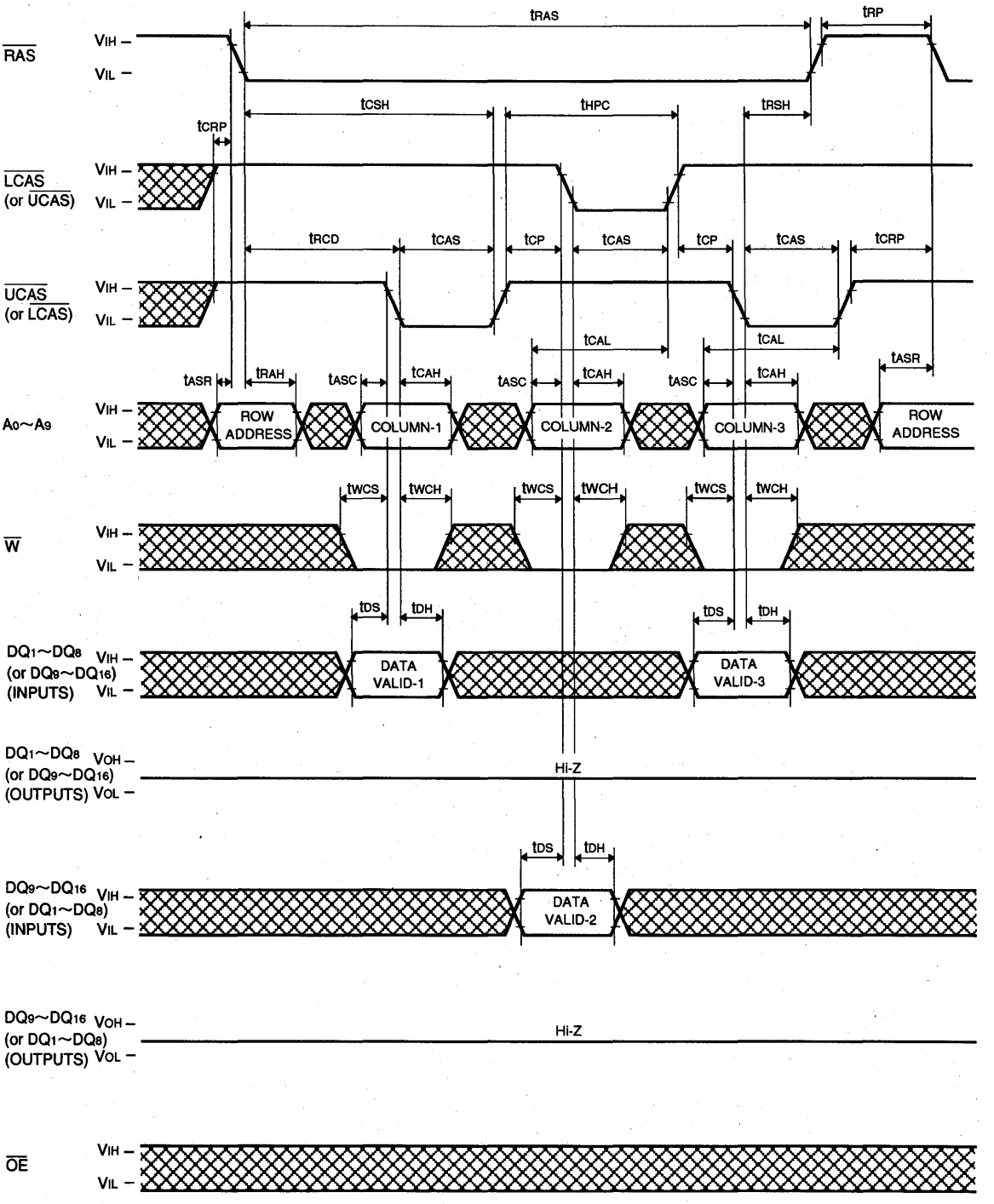


Hyper Page Mode Early Write Cycle

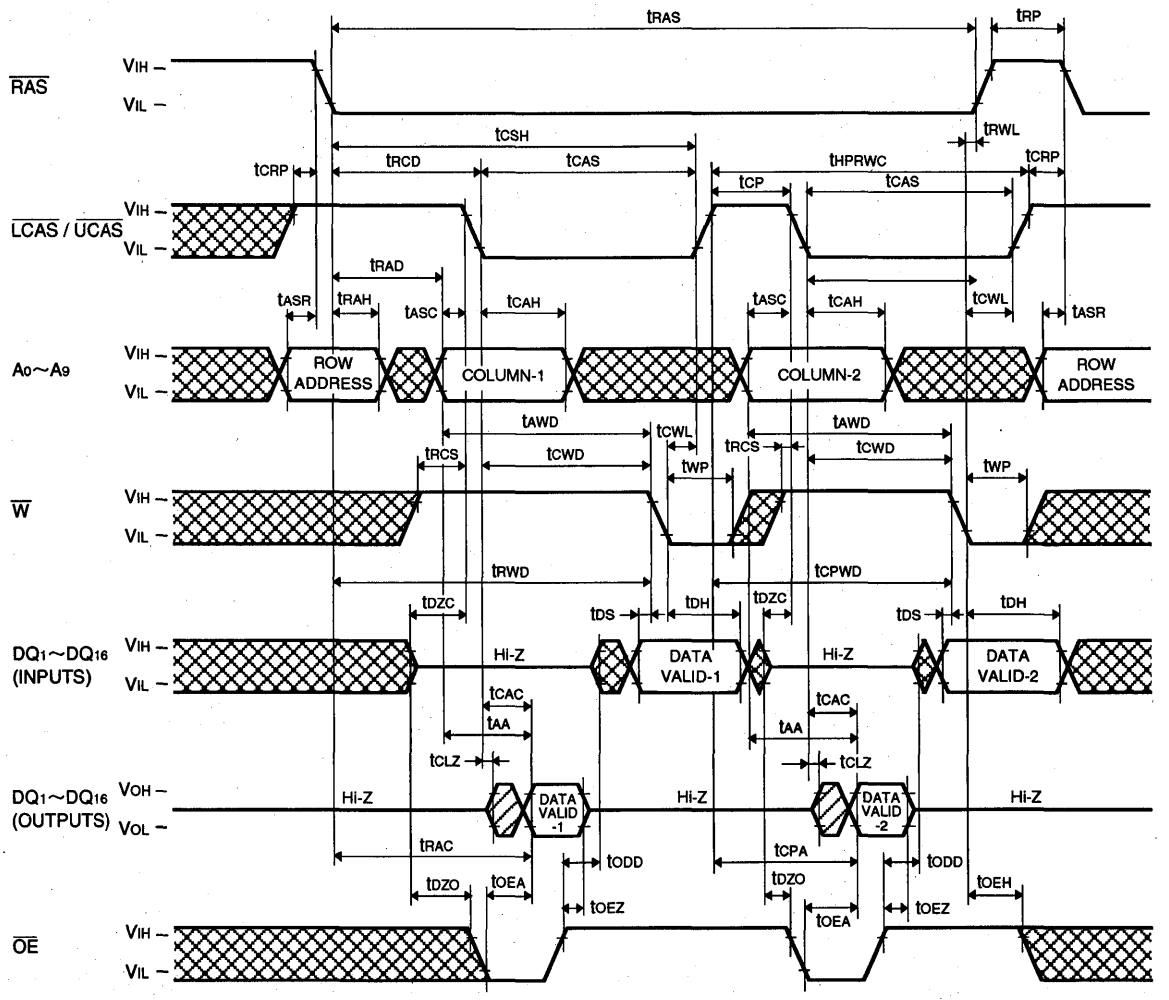


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Early Write Cycle

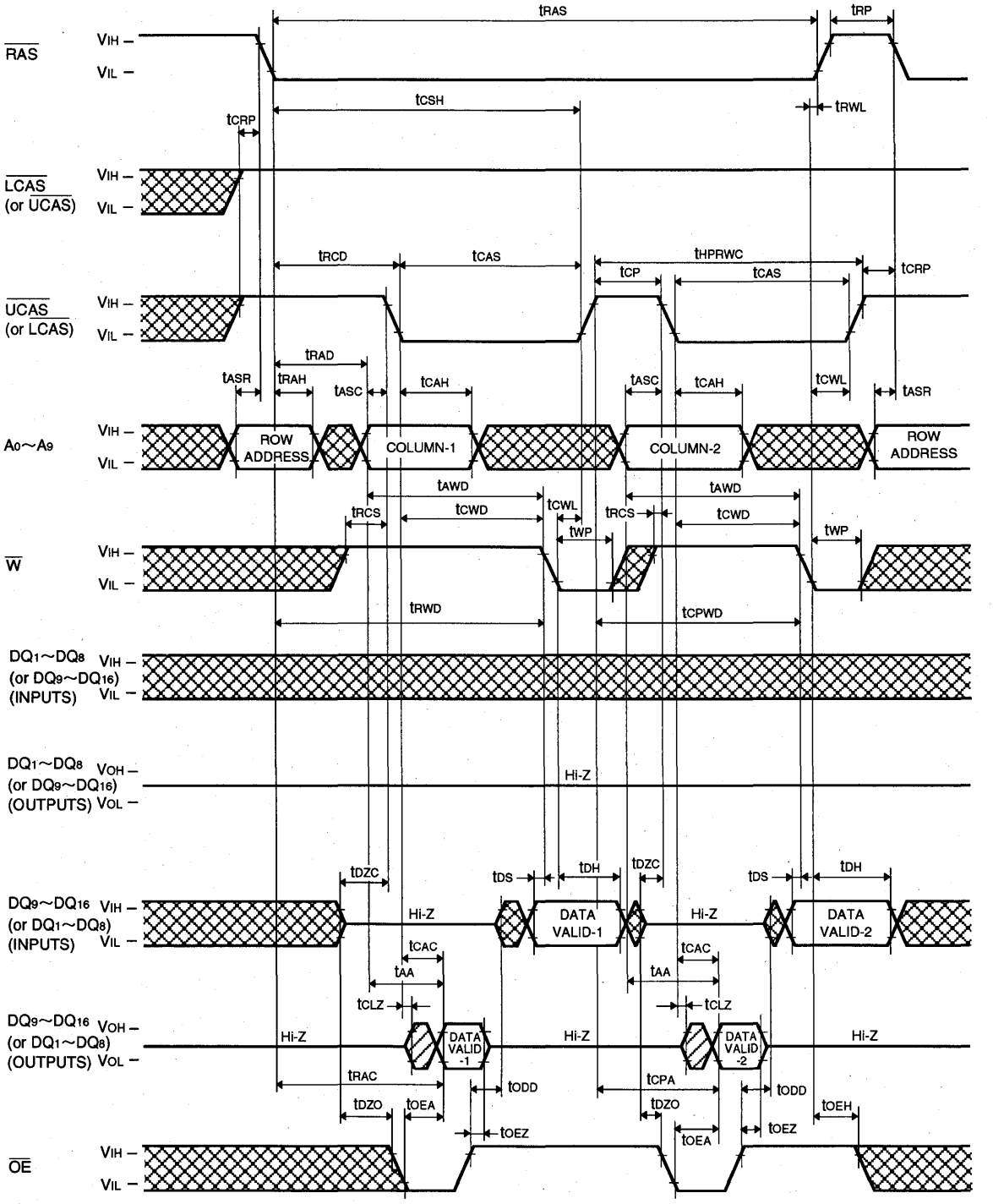


Hyper Page Mode Read-Write, Read-Modify-Write Cycle

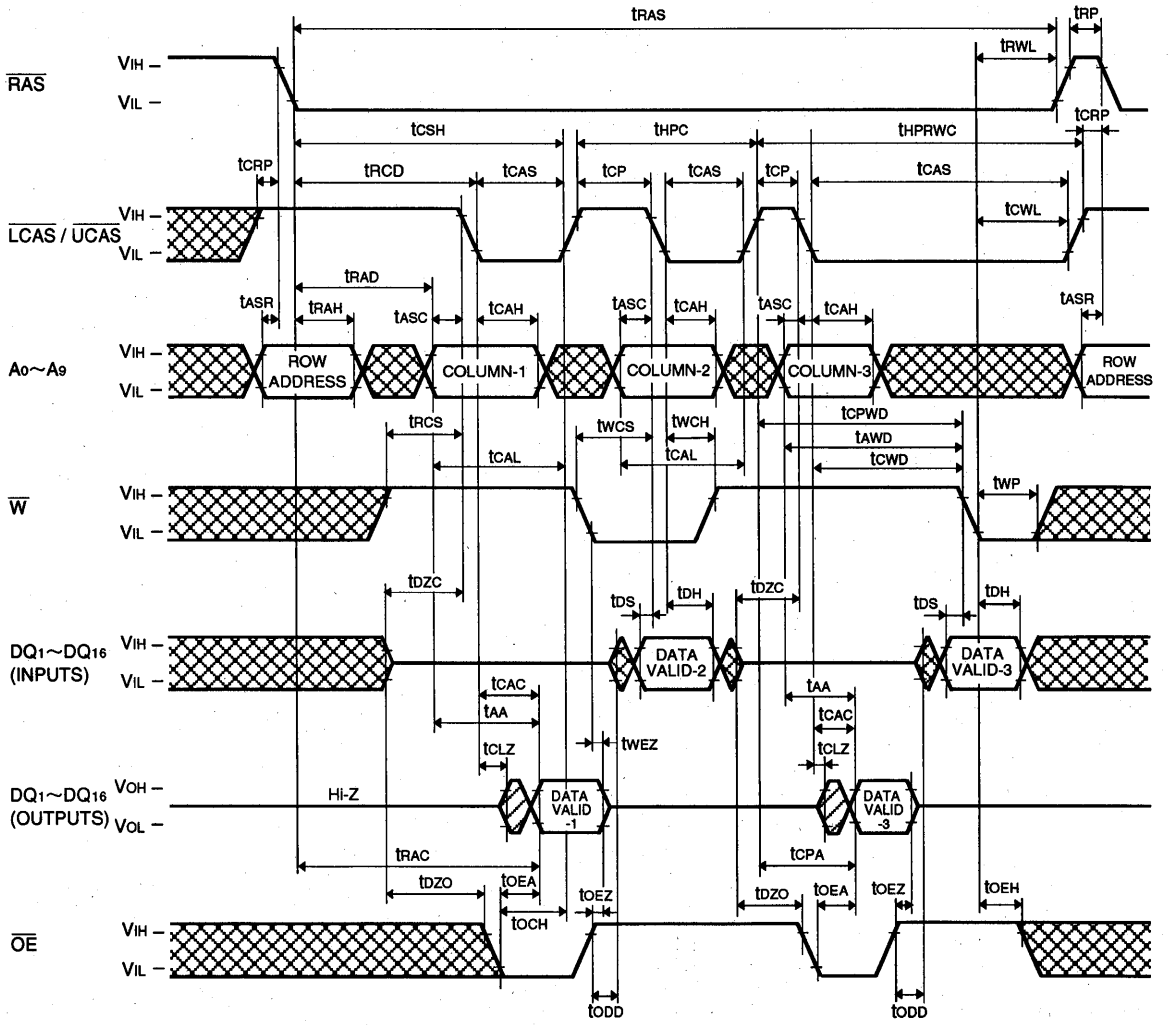


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle

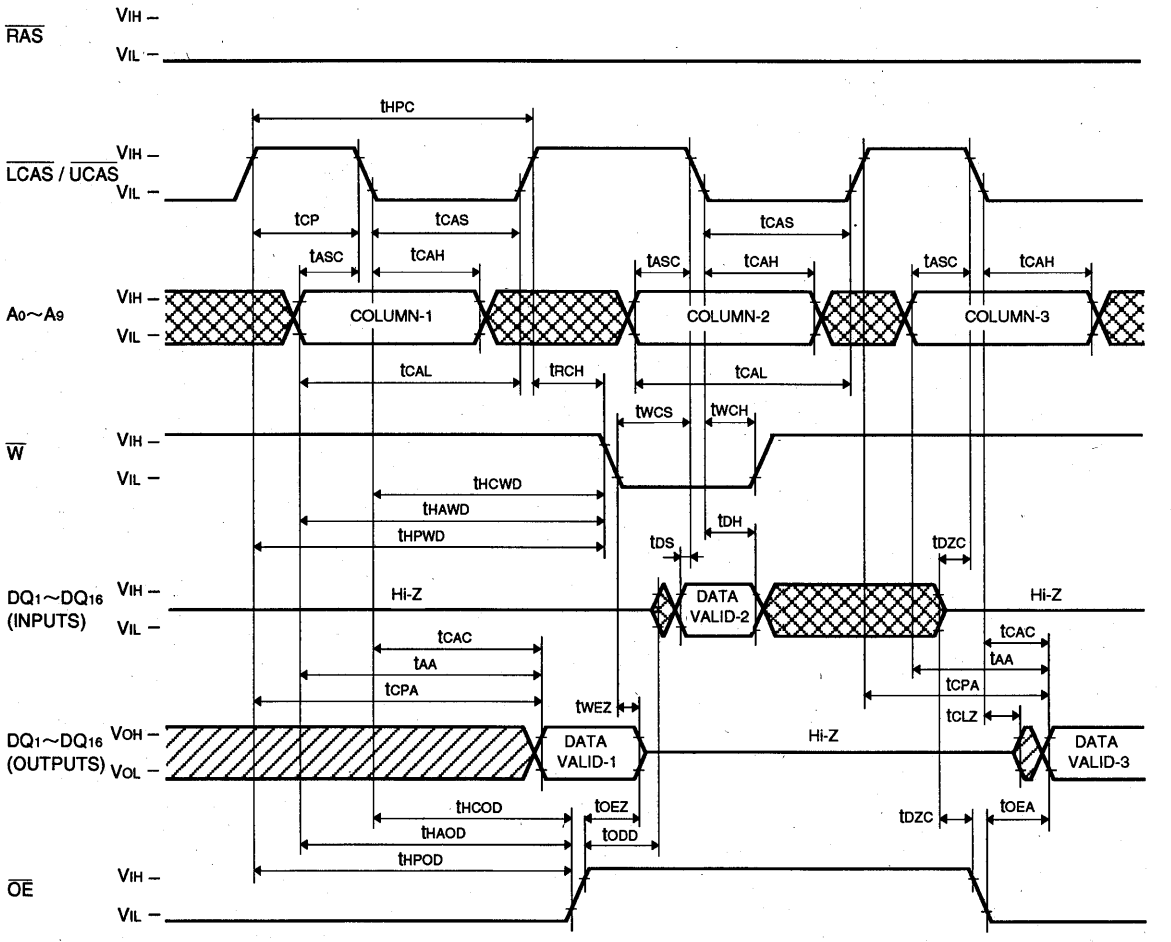


Hyper Page Mode Mix Cycle (1)

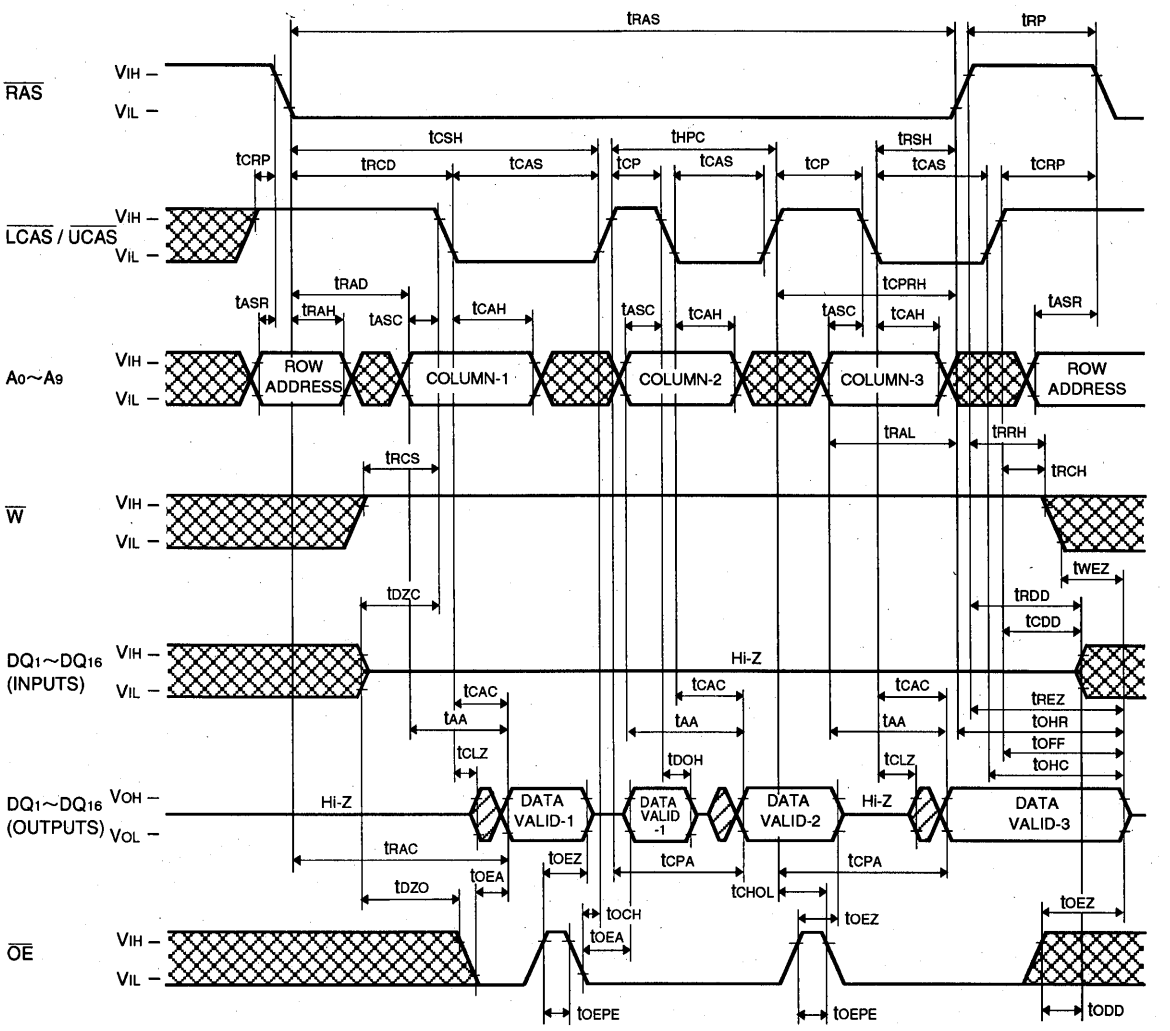


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Mix Cycle (2)

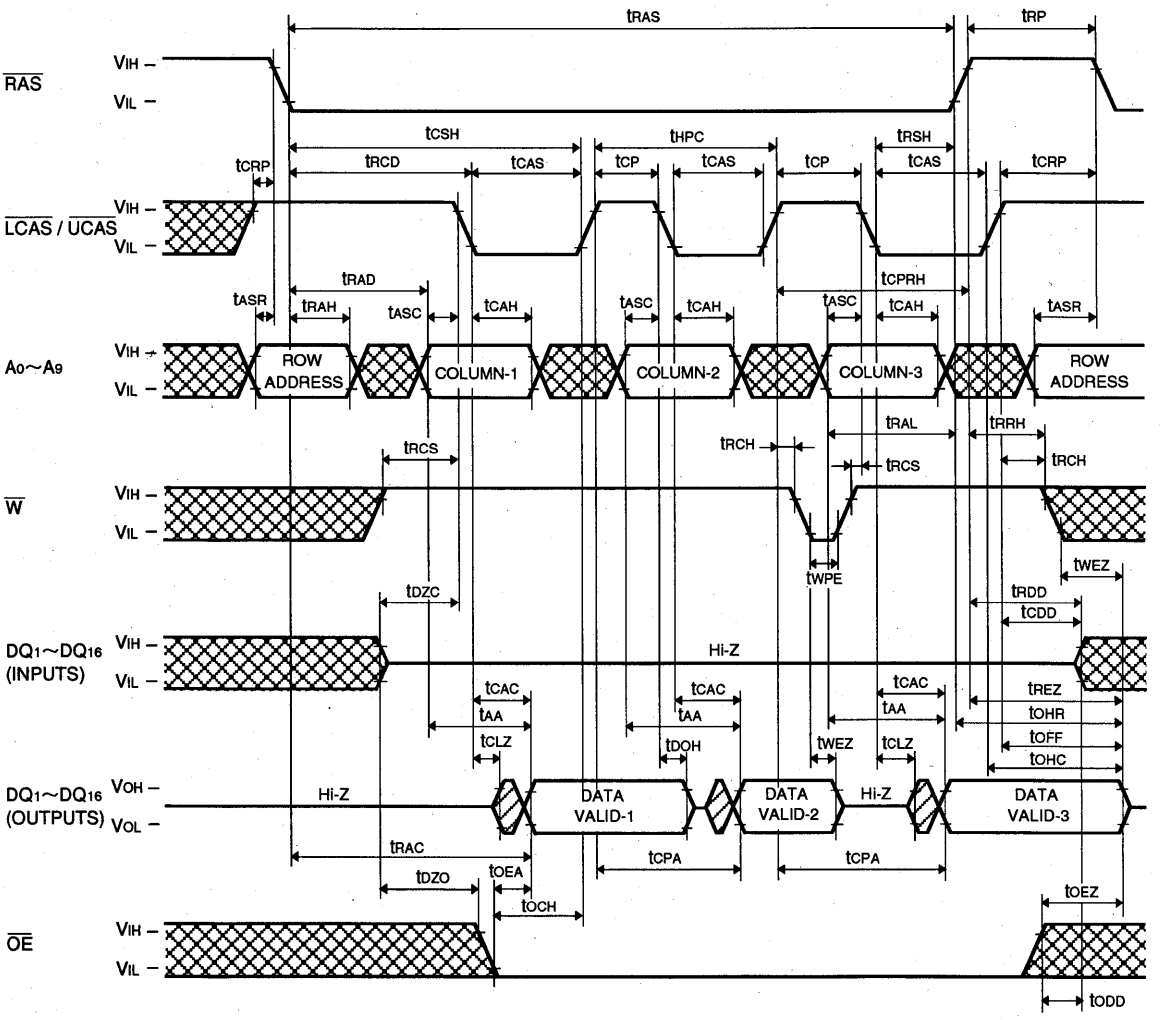


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)

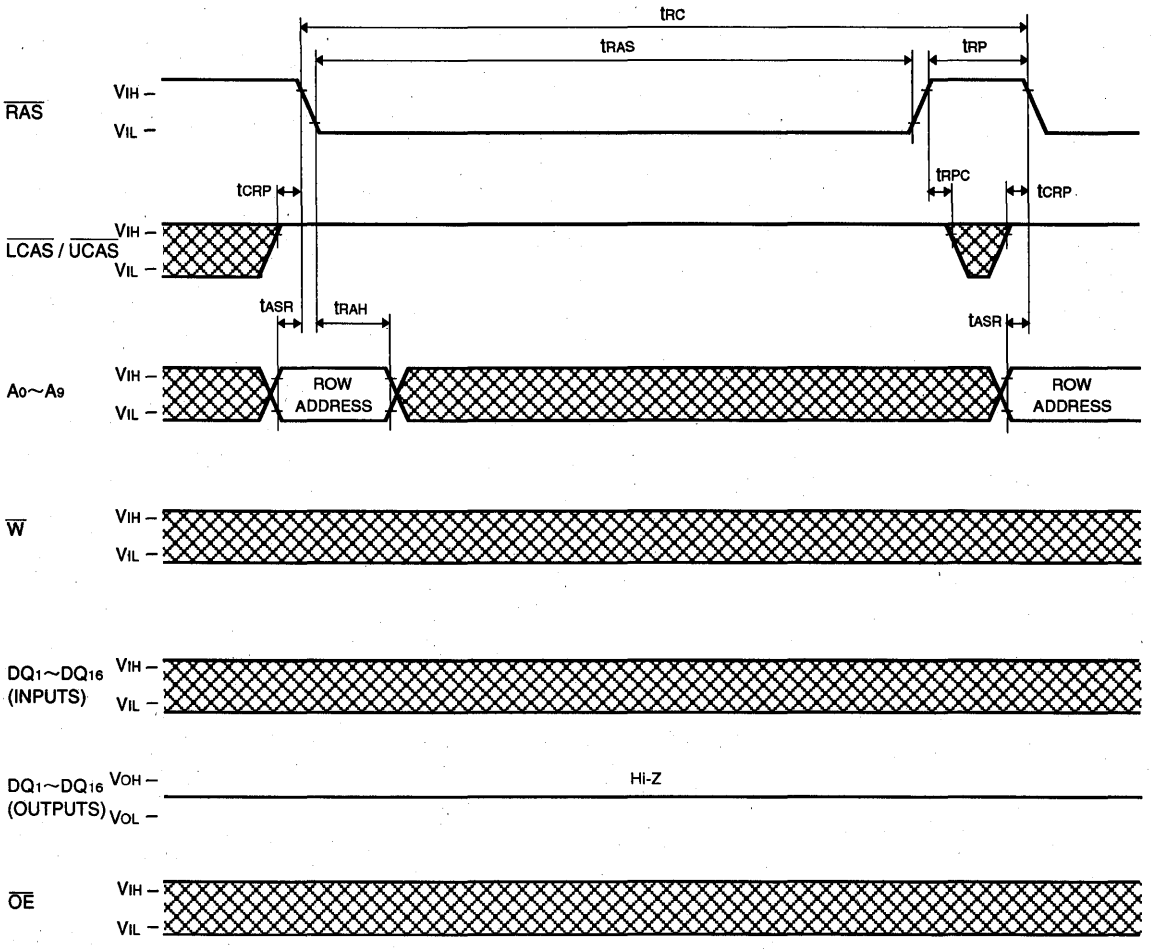


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

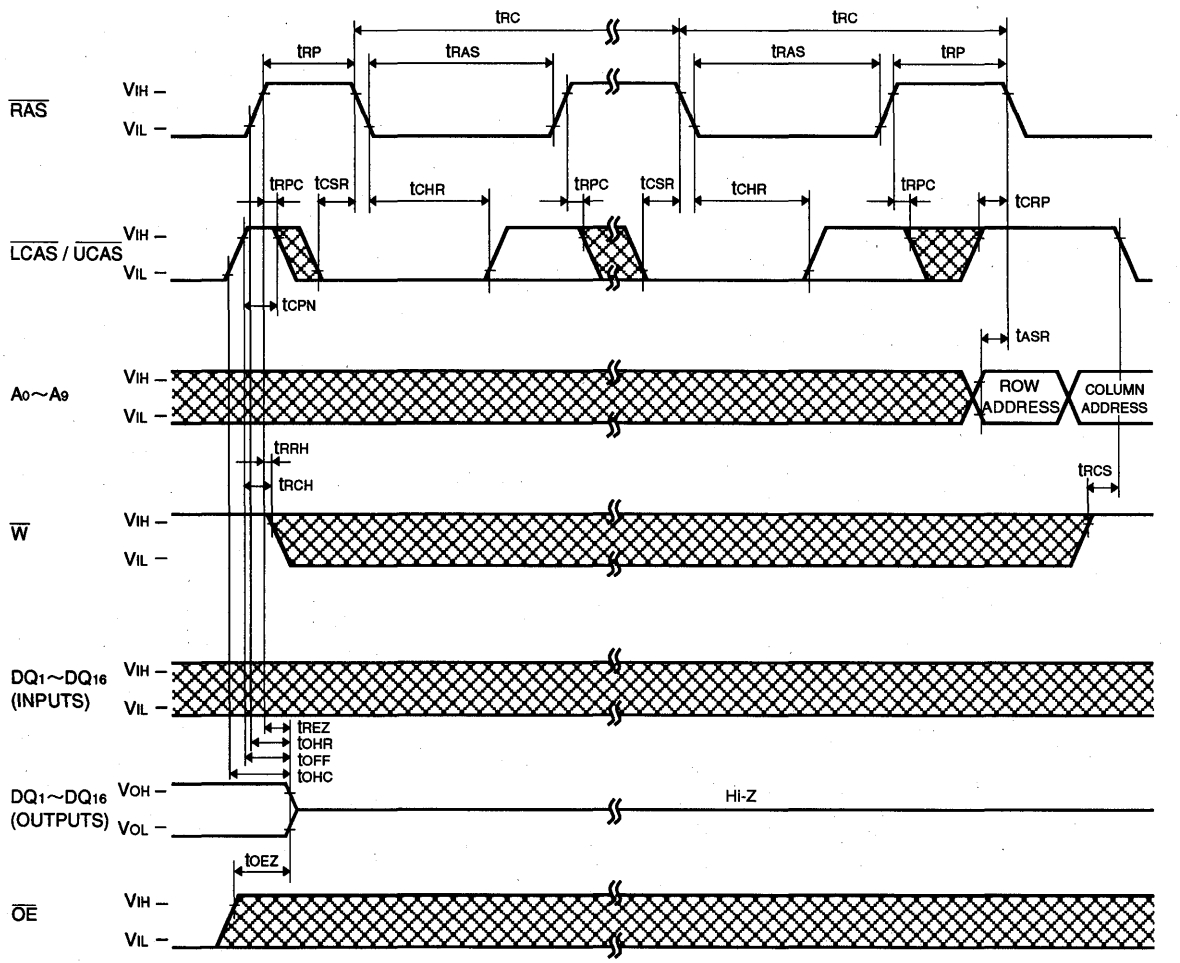


$\overline{\text{RAS}}$-only Refresh Cycle



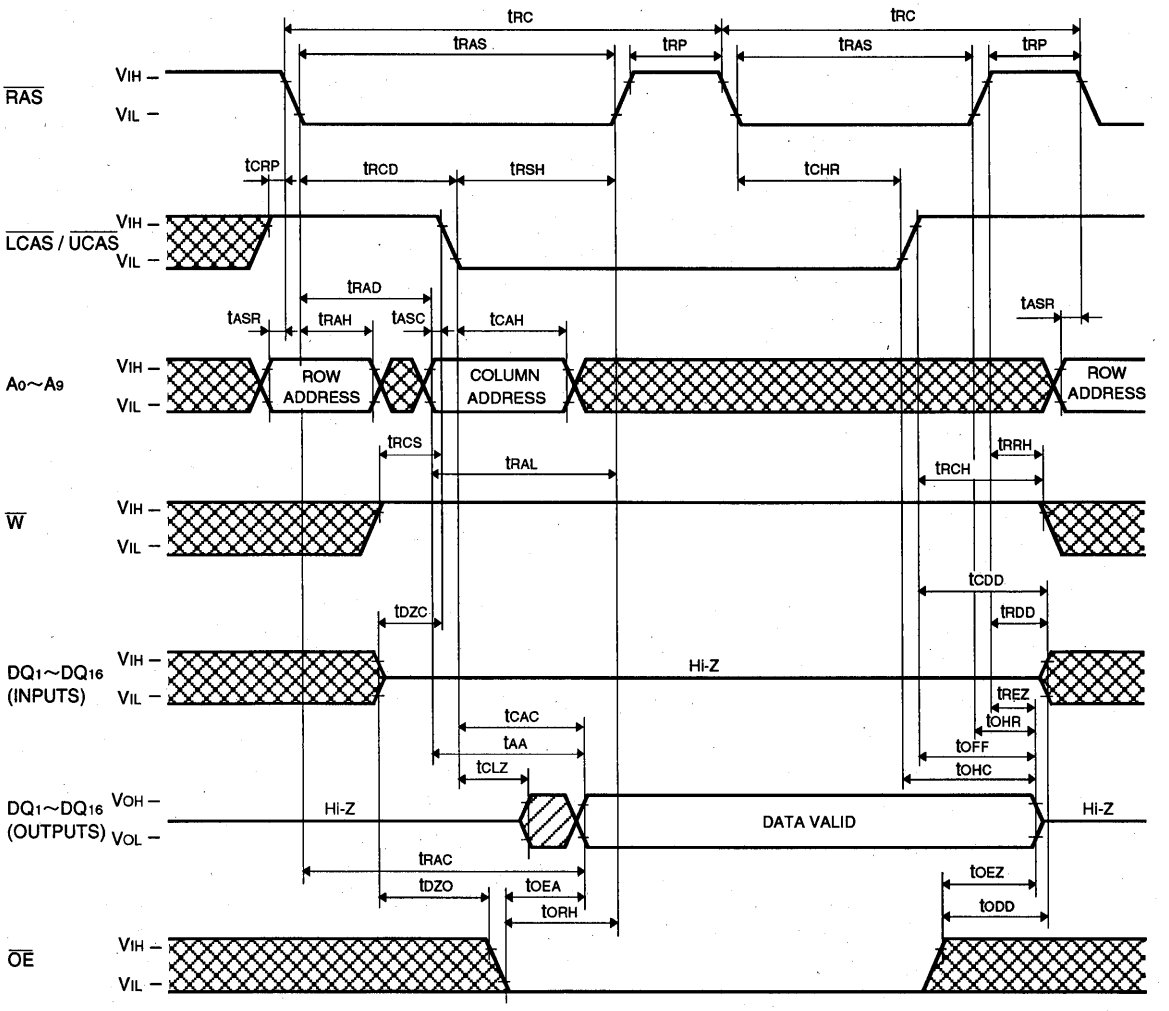
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

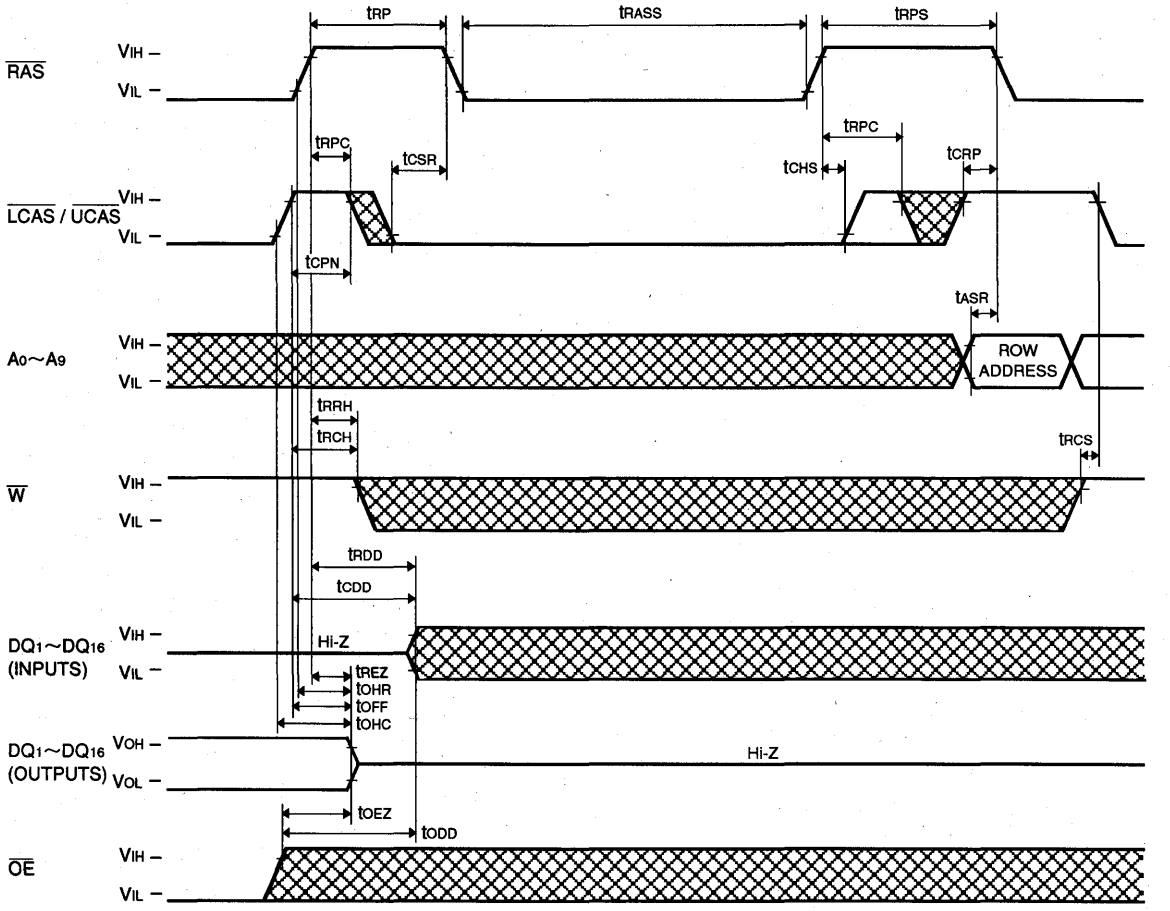
Hidden Refresh Cycle (Read) (Note 30)



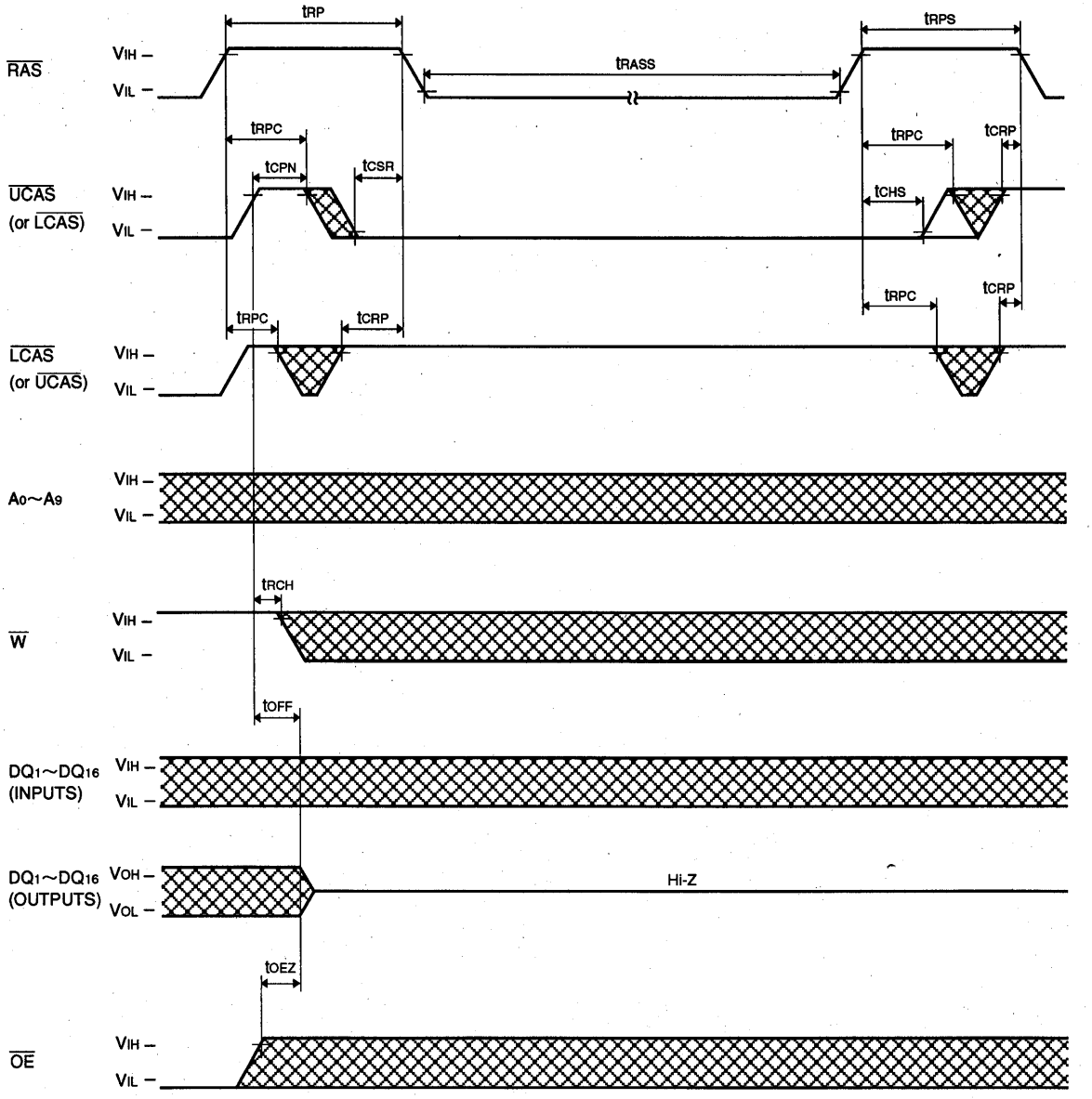
Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Self Refresh Cycle *



Upper / (Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18167CTP-5,-6,-7, -5S,-6S,-7S

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

The M5M4V18167CTP is pipeline burst dynamic RAM organized 1048574-words by 16-bits. This is fablicated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18167CTP-5,-5S	50	10	25	10	90	540
M5M4V18167CTP-6,-6S	60	11.6	30	12	110	450
M5M4V18167CTP-7,-7S	70	15	35	15	130	390

- Standard 50 pin TSOP
- Single 3.3V +0.3V, -0.15V supply (3.15V~3.6V)
- Low stand-by power dissipation
  1.8mW (Max) ·····CMOS Input level
- Low operating power dissipation
  M5M4V18167CTP- 5,-5S ·····650.0mW (Max)
  M5M4V18167CTP- 6,-6S ·····540.0mW (Max)
  M5M4V18167CTP- 7,-7S ·····470.0mW (Max)
- Pipeline Burst mode , $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output LVTTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  *: Applicable to self refresh version (M5M4V18167CTP-5S,-6S, -7S: option) only

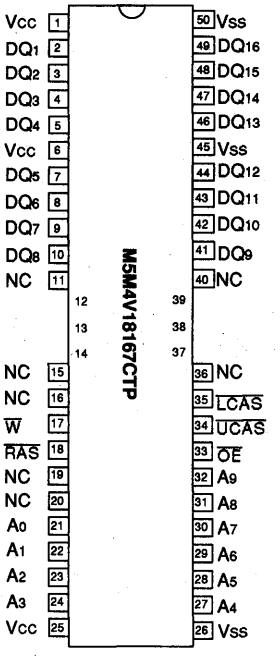
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC:NO CONNECTION

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

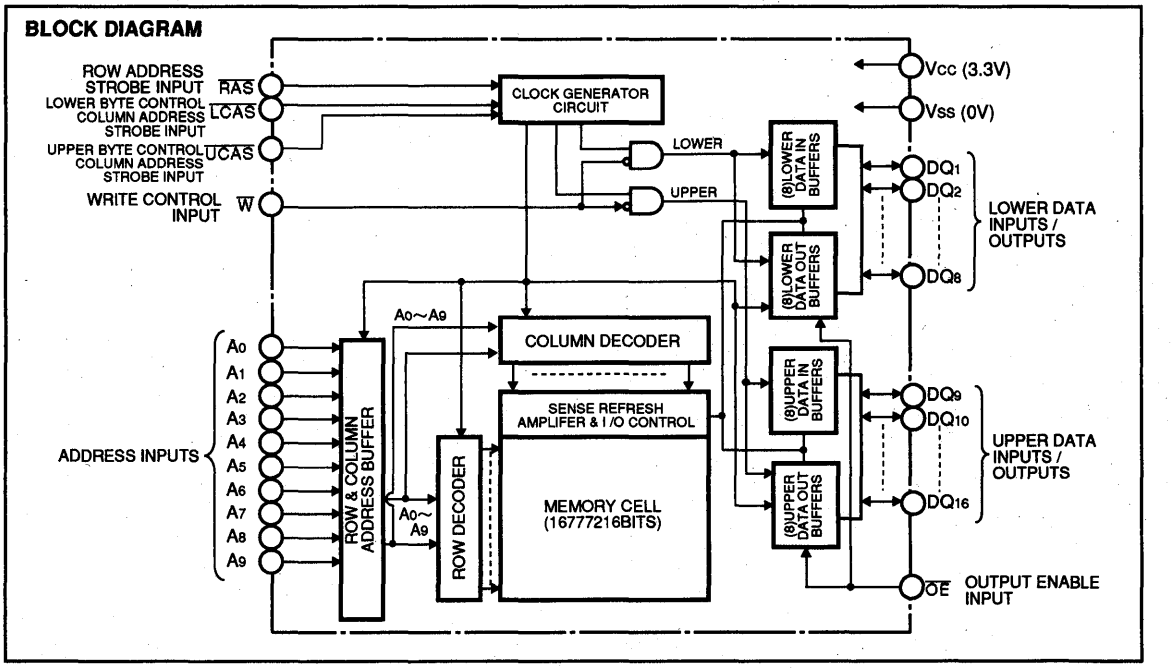
The M5M4V18167CTP provide, in addtion to normal read, write, and read-modify-write operations, a number of other functions, e.g., pipeline burst mode, $\overline{RAS}$ only refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



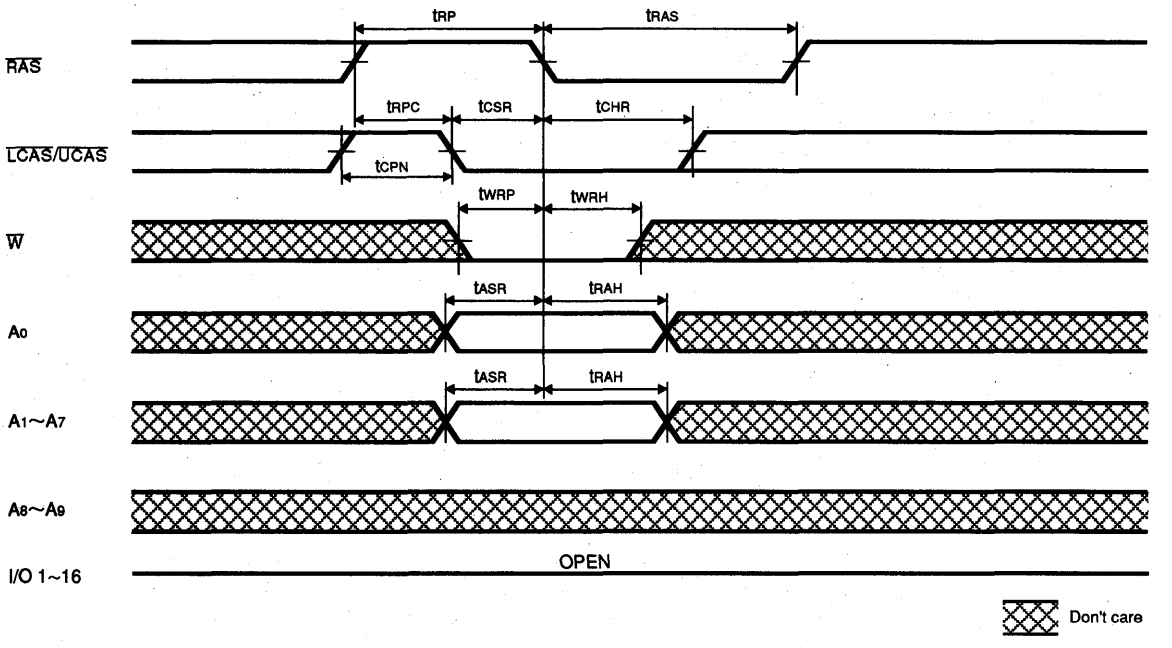
MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Burst Address Sequence Table

	INTERLEAVE				LINEAR			
1st	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01	X..X10	X..X11
2nd	X..X01	X..X00	X..X11	X..X10	X..X01	X..X10	X..X11	X..X00
3rd	X..X10	X..X11	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01
4th	X..X11	X..X10	X..X01	X..X00	X..X11	X..X00	X..X01	X..X10

Burst Address Sequence Set Cycle



Note 1: Address Table for Burst address sequence setting cycle.

	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Linear	X	X	L	L	H	L	L	L	L	L
Interleave	X	X	L	L	H	L	L	L	L	H

2: The burst sequence will remain set untill the device power is interrupted or another Burst address sequence setting cycle.

3: A $\overline{RAS}$ only or CBR refresh cycle must follow the Burst address setting cycle to exit the programming mode.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.5～4.6	V
V_I	Input voltage		−0.5～4.6	V
V_O	Output voltage		−0.5～4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 4)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.15	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 4 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70 ℃, V_{CC}=3.15V～3.6V, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	−10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 6,7,8)	M5M4V18167C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 8)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc −0.2 V			0.5	
I_{CC2}*	Supply current from Vcc, stand-by (Note 9)		$\overline{RAS}$= $\overline{CAS}$≧Vcc −0.2 V			150	μA
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 6,8)	M5M4V18167C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC4}(AV)	Average supply current from Vcc Pipeline-Burst-Mode (Note 6,7)	M5M4V18167C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			150	mA
		M5M4V18167C-6,-6S				140	
		M5M4V18167C-7,-7S				120	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 6)	M5M4V18167C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC8}(AV) *	Average supply current from Vcc Extended-Refresh-Mode (Note 9)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling ($\overline{W}$,$\overline{OE}$,A_0～A_9 ≦0.2V or ≧Vcc−0.2V) DQ=open,t_{RC}=125 μs,t_{RAS}=t_{RAS} min.～1 μs			300	μA
I_{CC9}(AV) *	Average supply current from Vcc Self-Refresh-Mode (Note 9)		$\overline{RAS}$= $\overline{CAS}$ ≦0.2V, output open			200	μA

Note 5: Current flowing into an IC is positive, out is negative.

6: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

7: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

8: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

9: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70 ℃, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHZ V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

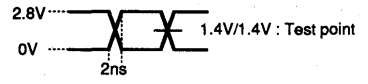
SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted, see notes 10,11)

Symbol	Parameter		Limits						Unit
			M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 12)		10		11.6		15	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 13)		50		60		70	ns
t_{AA}	Column address access time	(Note 14)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 15)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$			10		12		15	ns
t_{DOH}	Data hold time from $\overline{CAS}$ Low		3		3		3		ns
t_{OLZ}	Output low impedance time from $\overline{OE}$ low		3		3		3		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low		3		3		3		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 16)	4	10	4	10	4	15	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 16)	4	10	4	10	4	15	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 16,17)	4	10	4	10	4	15	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 16,17)	4	10	4	10	4	15	ns

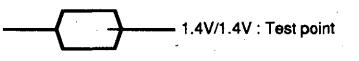
Note 10: AC Measurments t_T=2ns.

11: AC Characteristics test condition

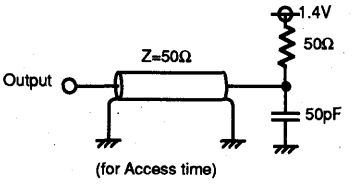
(1) Input timing Specification

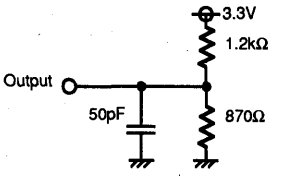


(2) Output timing Specification



(3) Output Load





Note 12: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

13: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

14: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

15: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

16: t_{OEZ} (max) , $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq | \pm 10 \mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

17: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (for Read, Write, and Refresh Cycles)

(Ta=0~70℃, Vcc = 3.15V~3.6V, Vss=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRP	$\overline{RAS}$ high pulse width	30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note18)	18	25	20	31.8	20	40	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	5		5		5		ns
tCPN	$\overline{CAS}$ high pulse width	10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low (Note19)	15	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low	1.5		1.5		1.5		ns
tASC	Column address setup time before $\overline{CAS}$ low (Note20)	1.5		1.5		1.5		ns
tRAH	Row address hold time after $\overline{RAS}$ low	8.5		8.5		8.5		ns
tCAH	Column address hold time after $\overline{CAS}$ low	8.5		8.5		8.5		ns
tDZC	Delay time, data to $\overline{CAS}$ low (Note21)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low (Note21)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data (Note22)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data (Note22)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data (Note22)	13		15		20		ns
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	5	10000	5	10000	5	10000	ns
tRCS	Read Setup time before $\overline{CAS}$ low	3		3		3		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 23)	5		5		5		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 23)	10		10		10		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	3		3		3		ns
tWCH	Write hold time after $\overline{CAS}$ low	5		5		5		ns
tWEP	Write pulse width	7		7		7		ns
tCRW	$\overline{CAS}$ Low to$\overline{RAS}$ High (Required only for Write Cycle)	15		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	3		3		3		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	5		5		5		ns
tT	Transition time	1.5	50	1.5	50	1.5	50	ns
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tREF*	Refresh cycle time		128		128		128	ms

Note 18: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

19: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

20: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

21: Either tDZC or tDZO must be satisfied.

22: Either tRDD or tCDD or tODD must be satisfied.

23: Either tRCH or tRRH must be satisfied for a read cycle.

Pipeline Burst Mode Cycle (Read,Read terminated Read,Write,Write terminated Write,Read-Write,Write-Read) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Pipeline Burst EDO Cycle	15		16.6		20		ns
tDOH	Output hold time from $\overline{CAS}$ low	3		3		3		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note25)	50	125000	60	125000	70	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note26)	5		5		5		ns
tCHOL	Hold time to maintain the data Hi -Z until $\overline{CAS}$ access	7		7		7		ns
tOEP	$\overline{OE}$ Pulse Width	7		7		7		ns
tWEP	$\overline{W}$ Pulse Width	7		7		7		ns
tWET	$\overline{W}$ Pulse Width (for Write comand termination)	7		7		7		ns
tWLC	$\overline{W}$ Lock out from $\overline{CAS}$ High	3		3		3		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

25: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

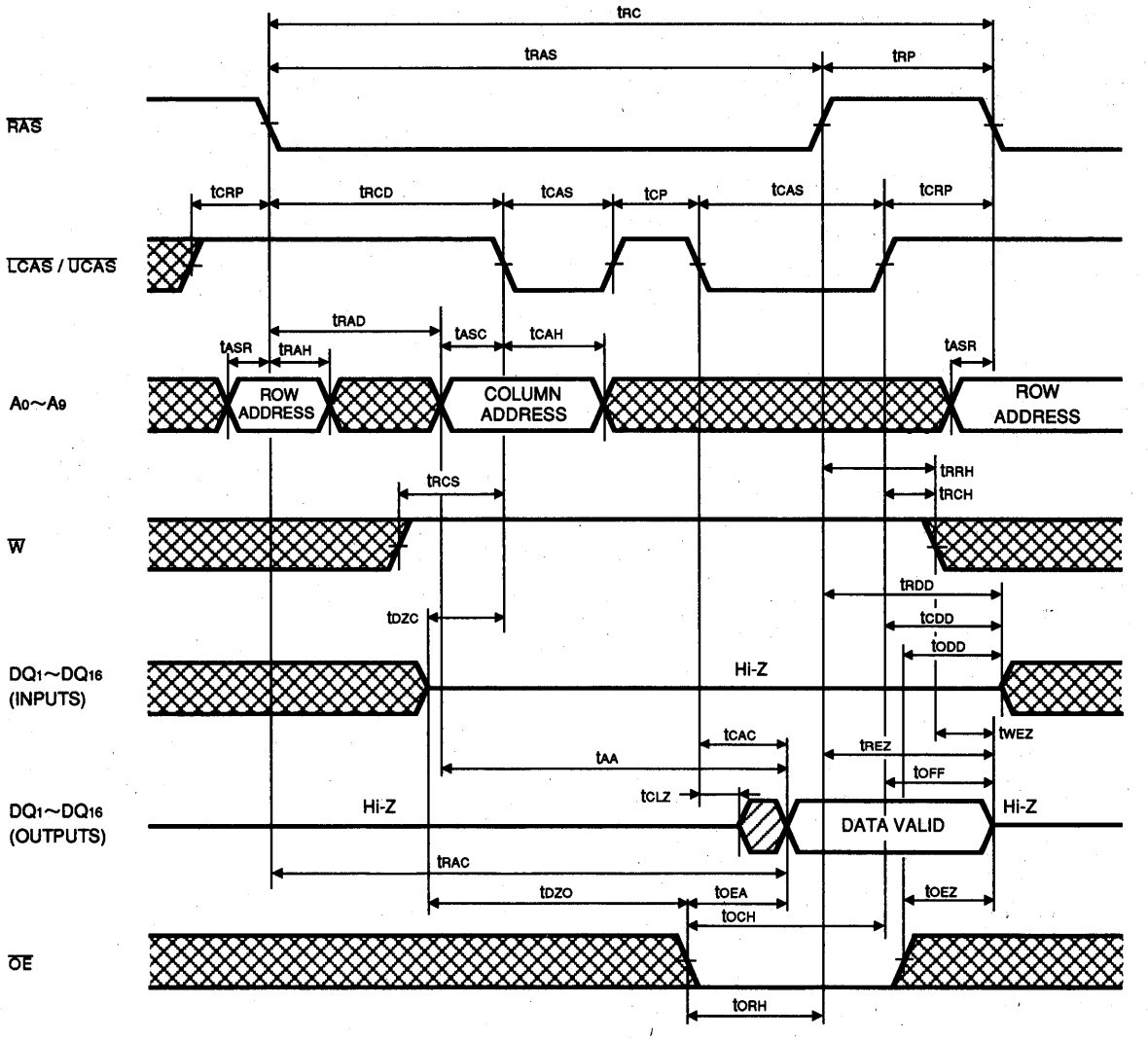
26: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, and WCBR Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		15		15		ns
tWRP	$\overline{WE}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWRH	$\overline{WE}$ hold time after $\overline{RAS}$ low	10		10		10		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

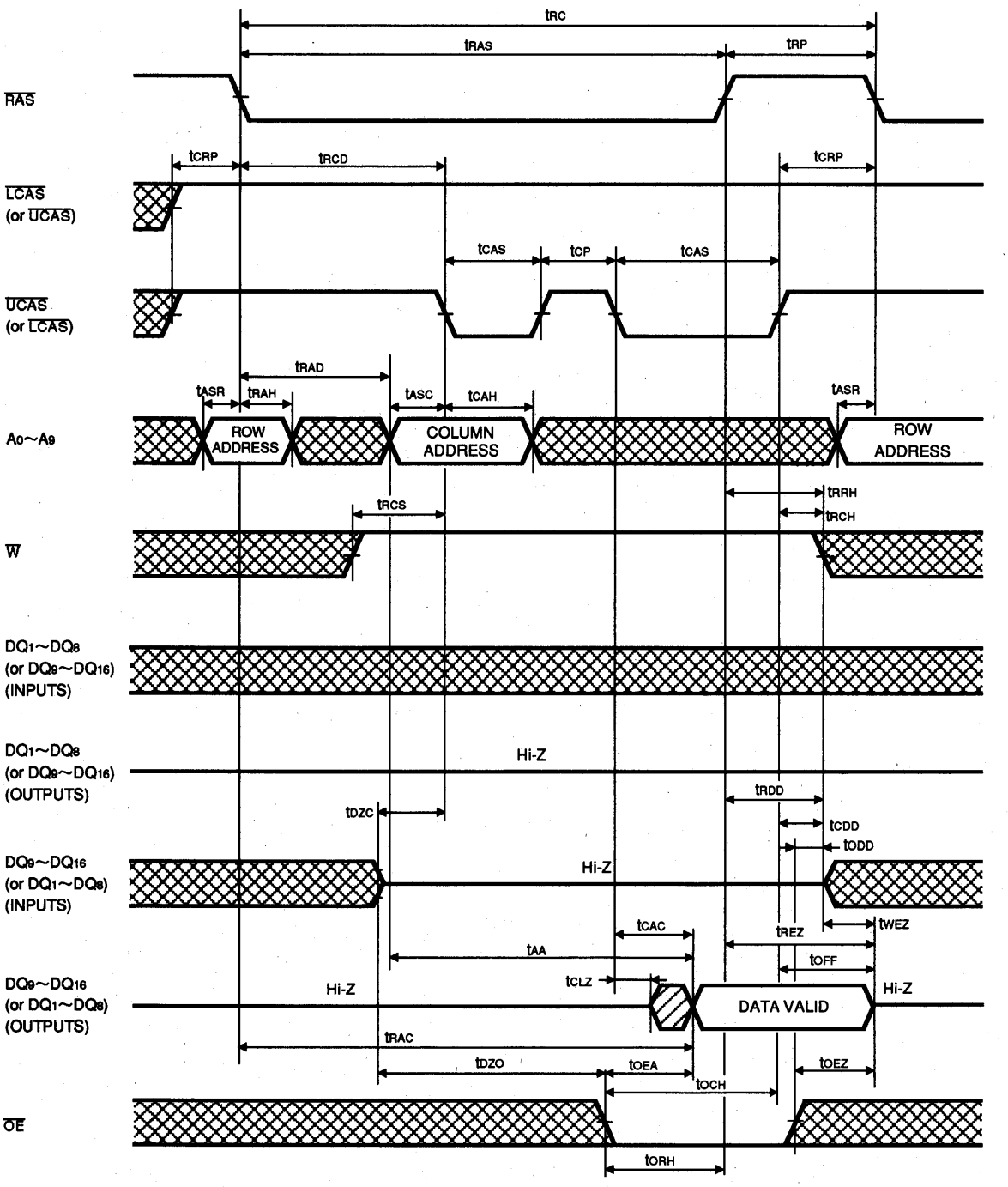
Timing Diagrams (Note 28)
Read Cycle



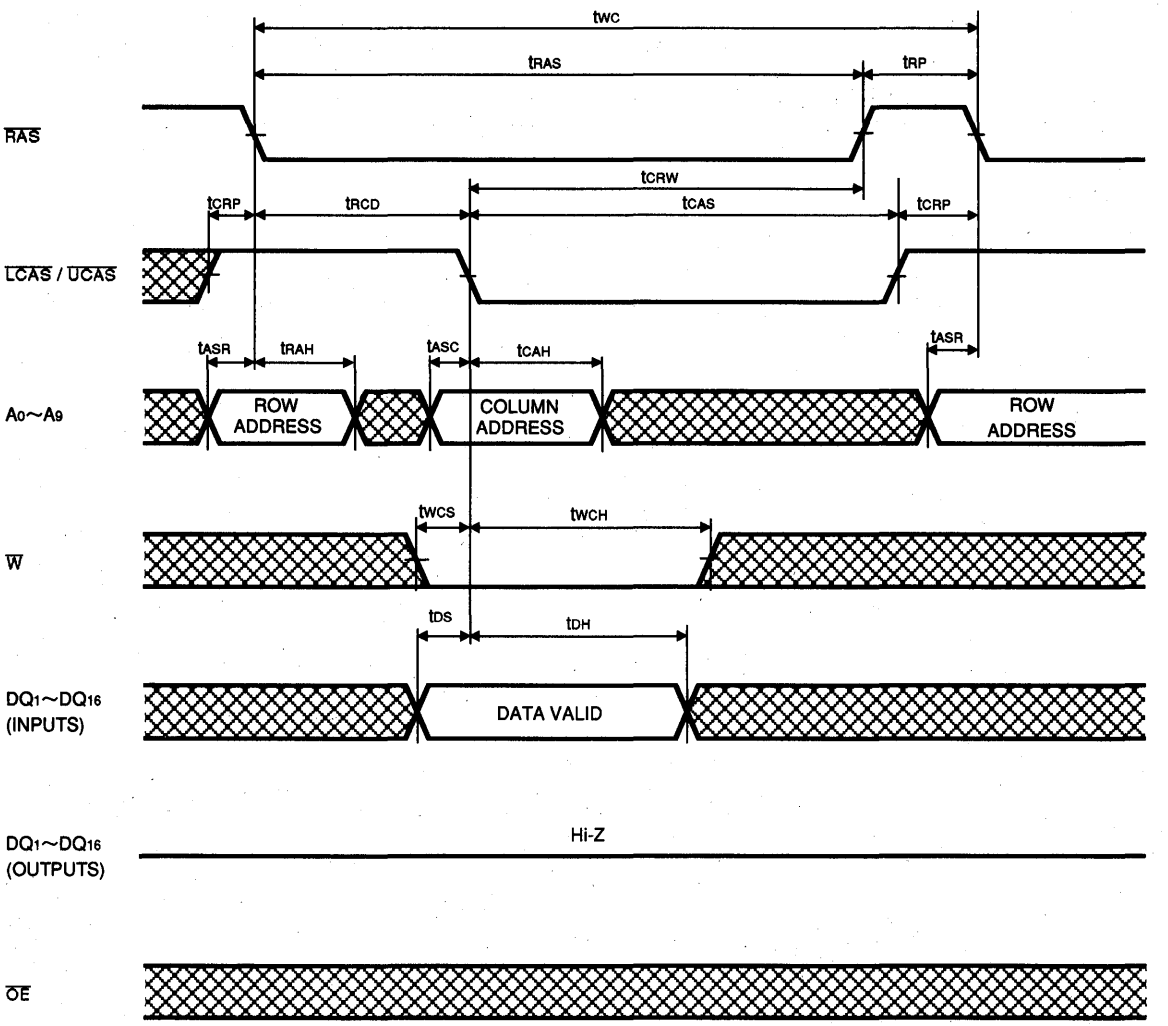
Note 28 Indicates the don't care input.

Indicates the invalid output.

Byte Read Cycle

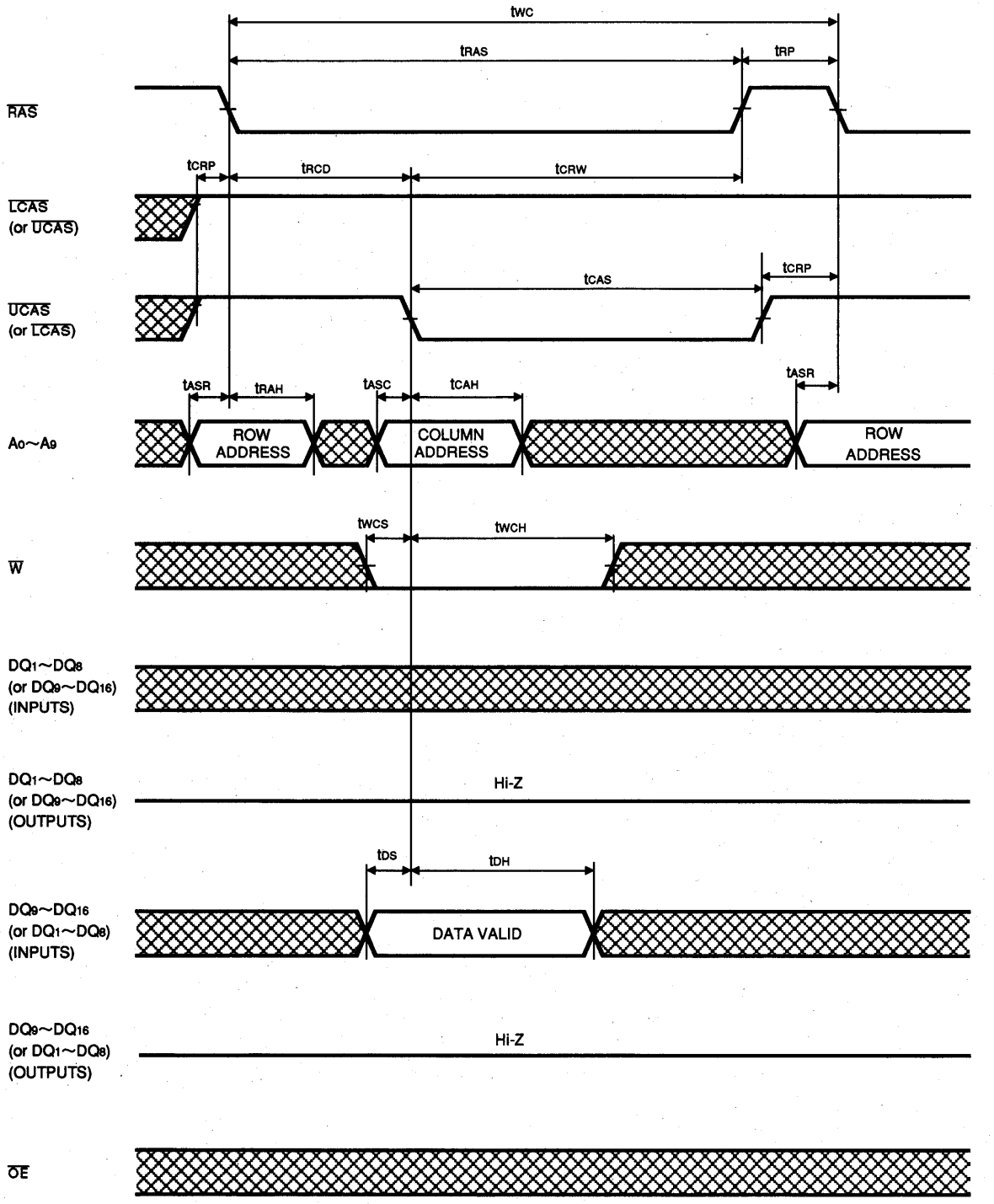


Write Cycle

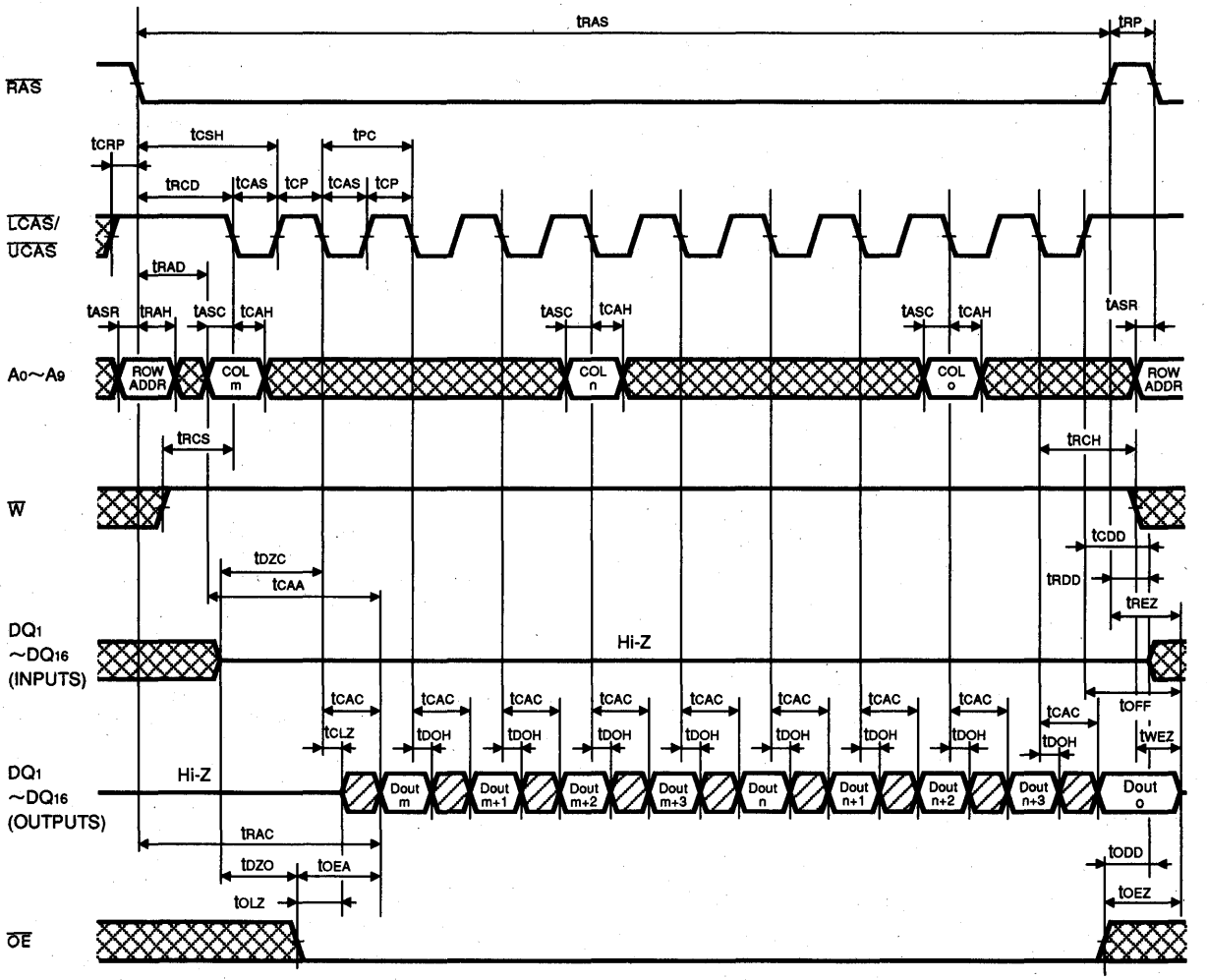

tWC
tRAS
tRP
RAS
tCRW
tCRP
tRCD
tCAS
tCRP
LCAS / UCAS
tASR
tRAH
tASC
tCAH
tASR
A0~A9
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
tWCS
tWCH
W
tDS
tDH
DQ1~DQ16 (INPUTS)
DATA VALID
DQ1~DQ16 (OUTPUTS)
Hi-Z
OE

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

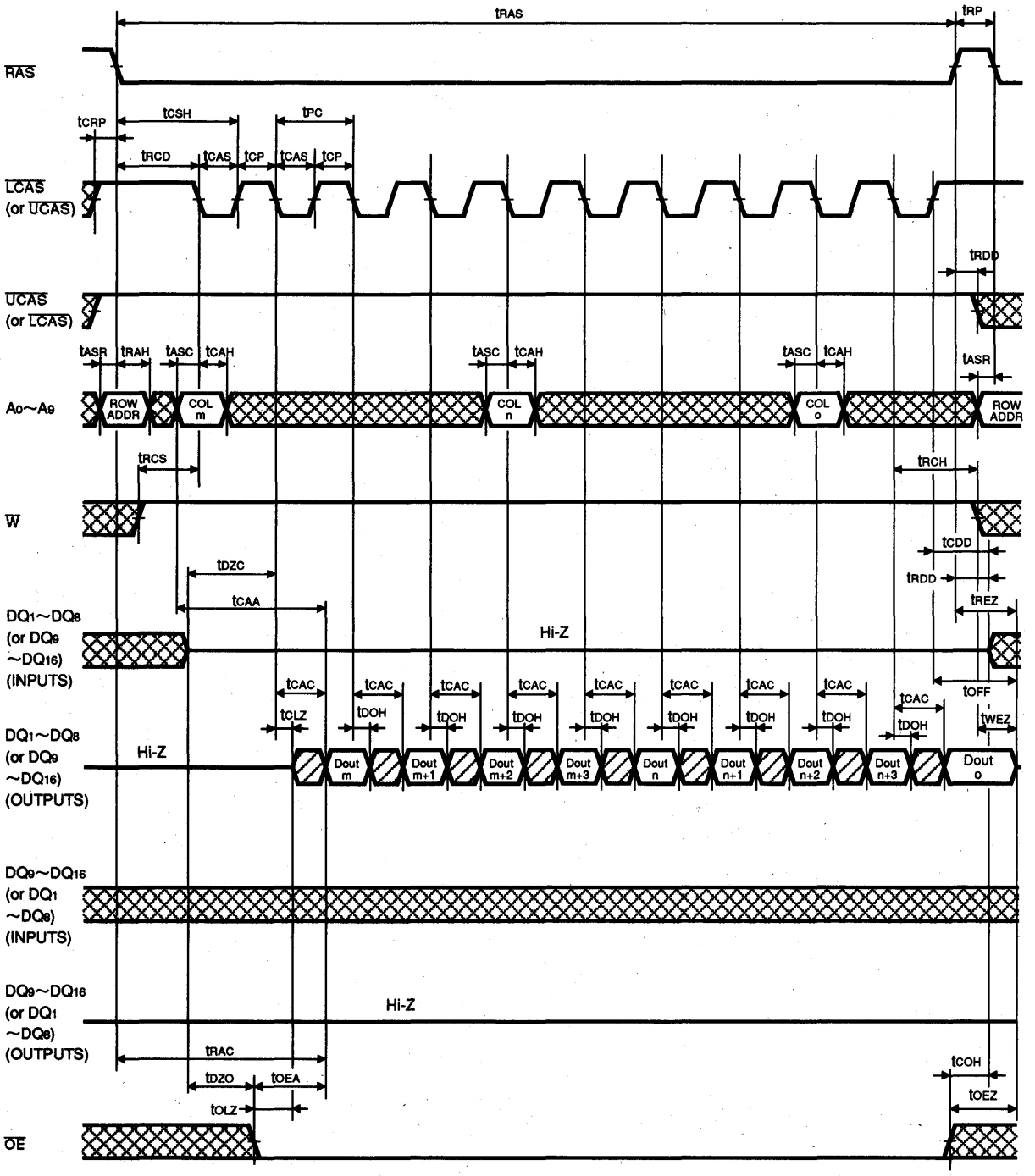
Byte Write Cycle



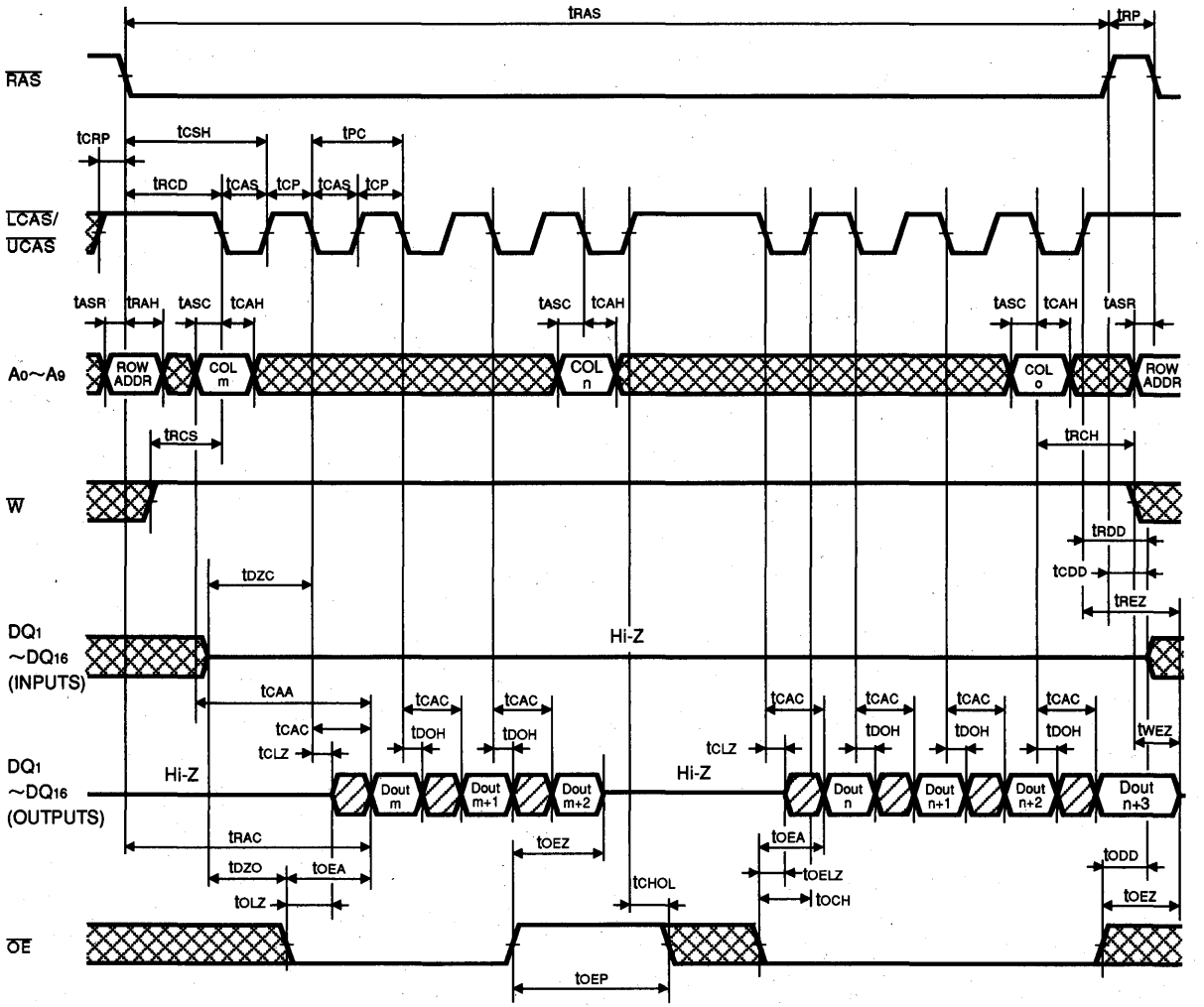
Pipeline Burst Mode Read Cycle (1)



Pipeline Burst Mode Byte Read Cycle (1)

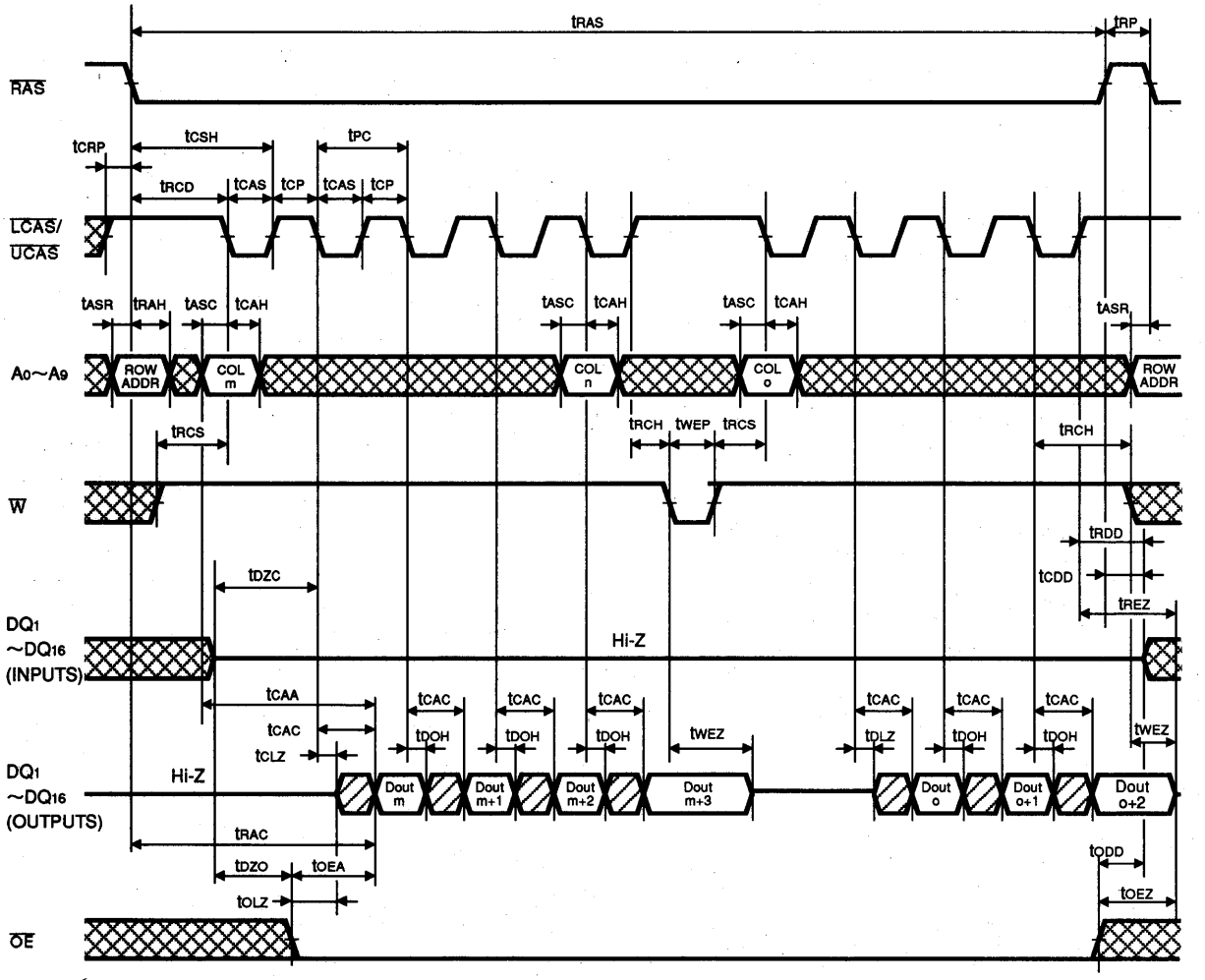


Pipeline Burst Mode Read Cycle (2)

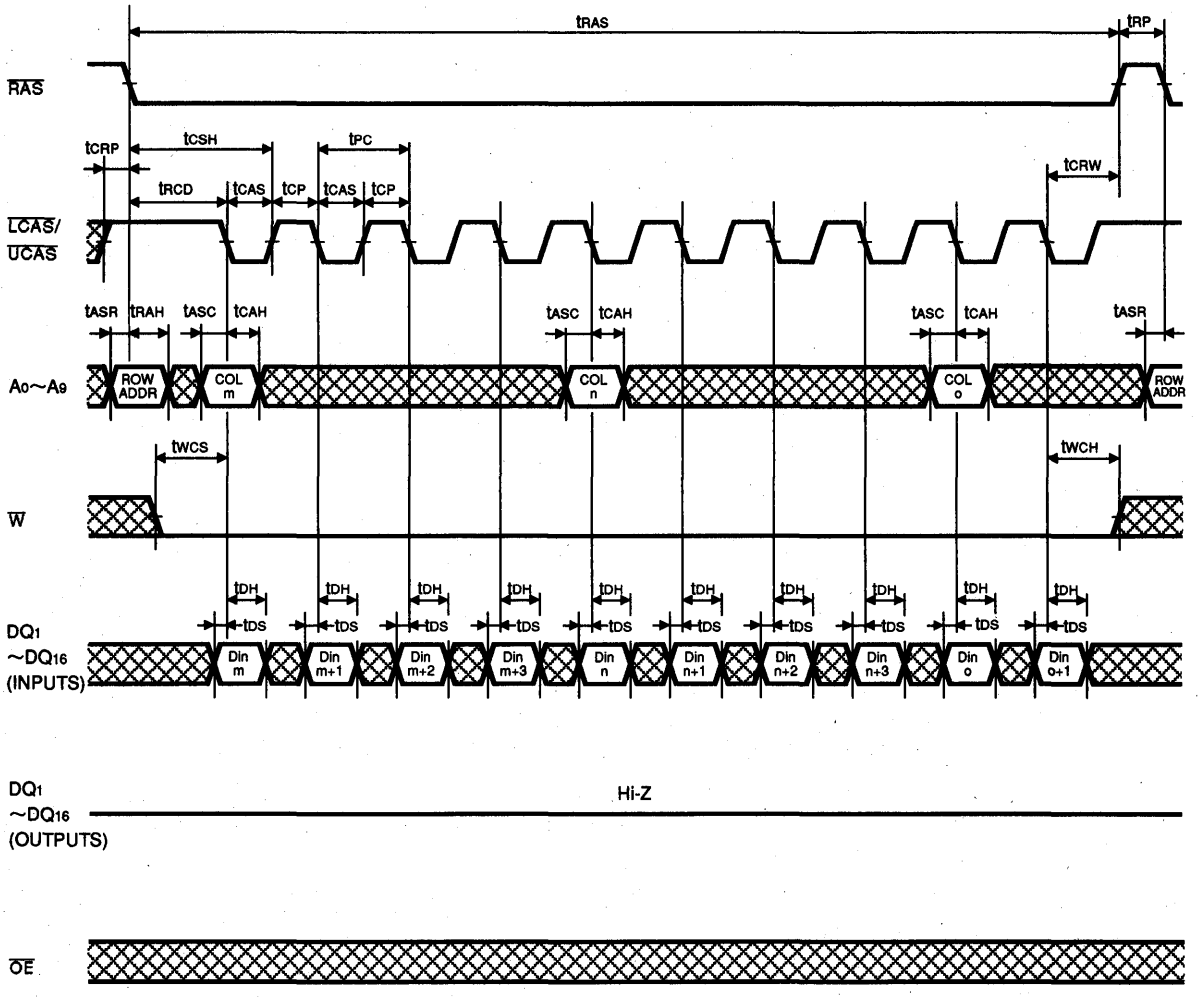


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

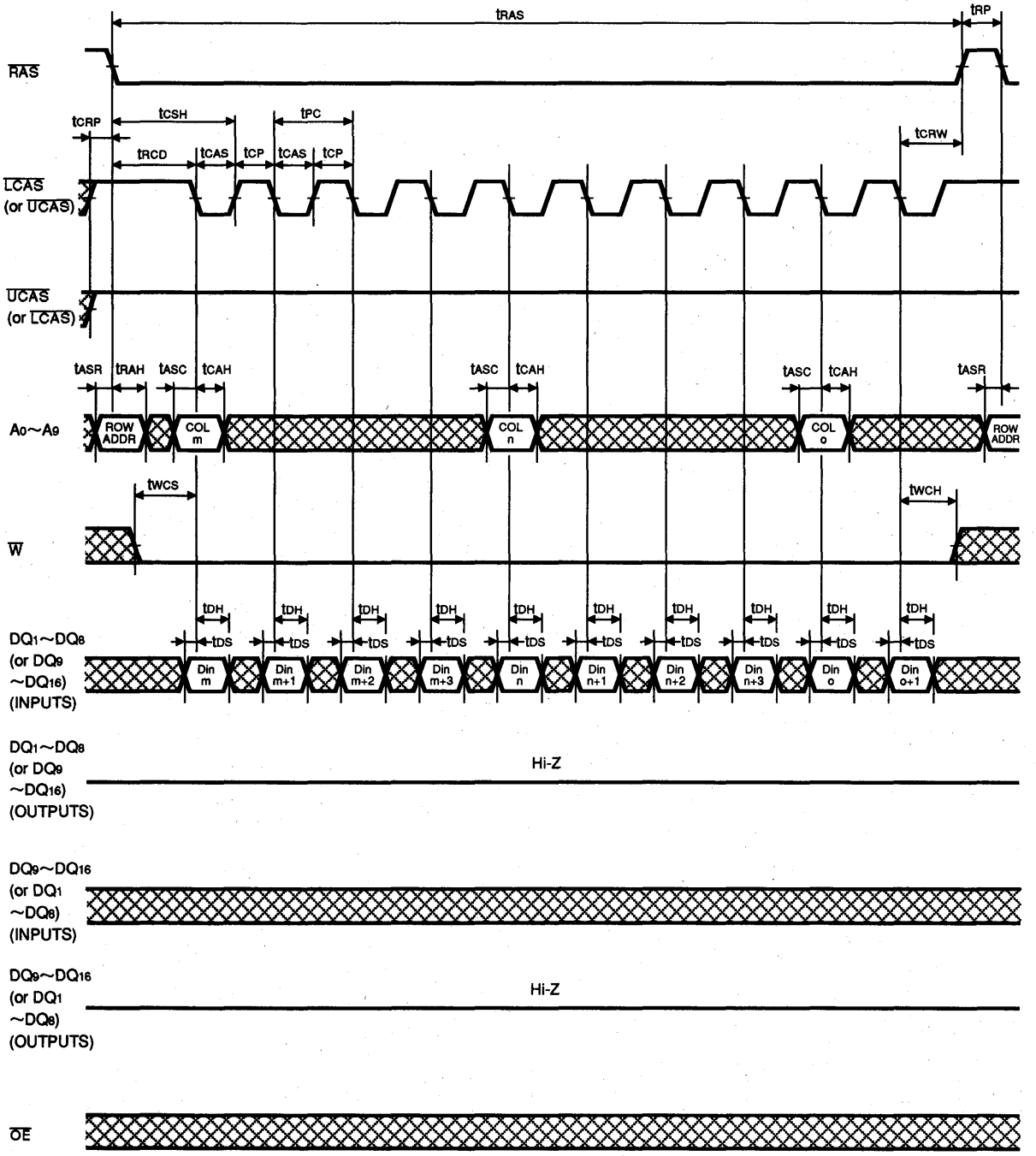
Pipeline Burst Mode Read Cycle (Read Terminated Read)



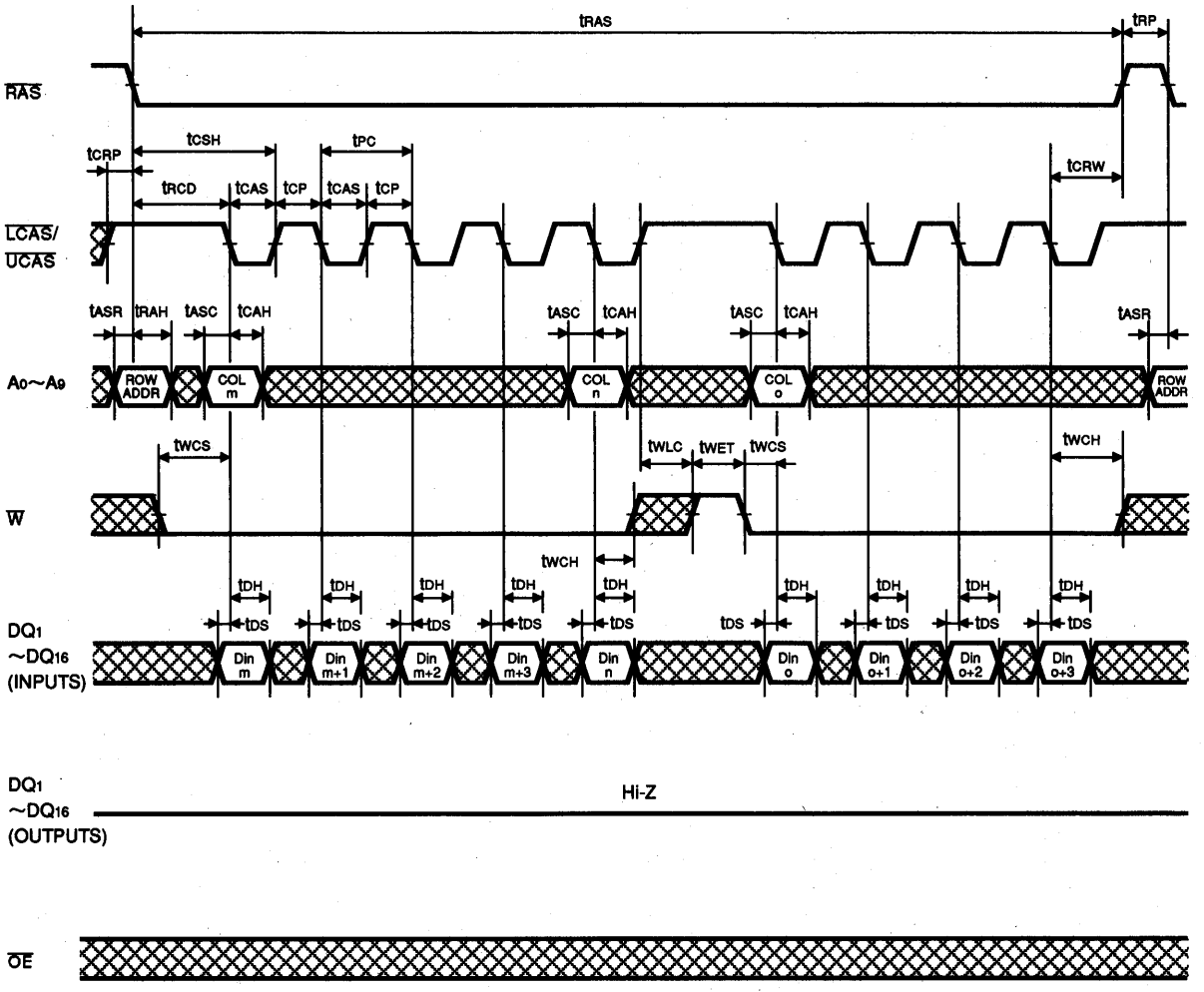
Pipeline Burst Mode Write Cycle



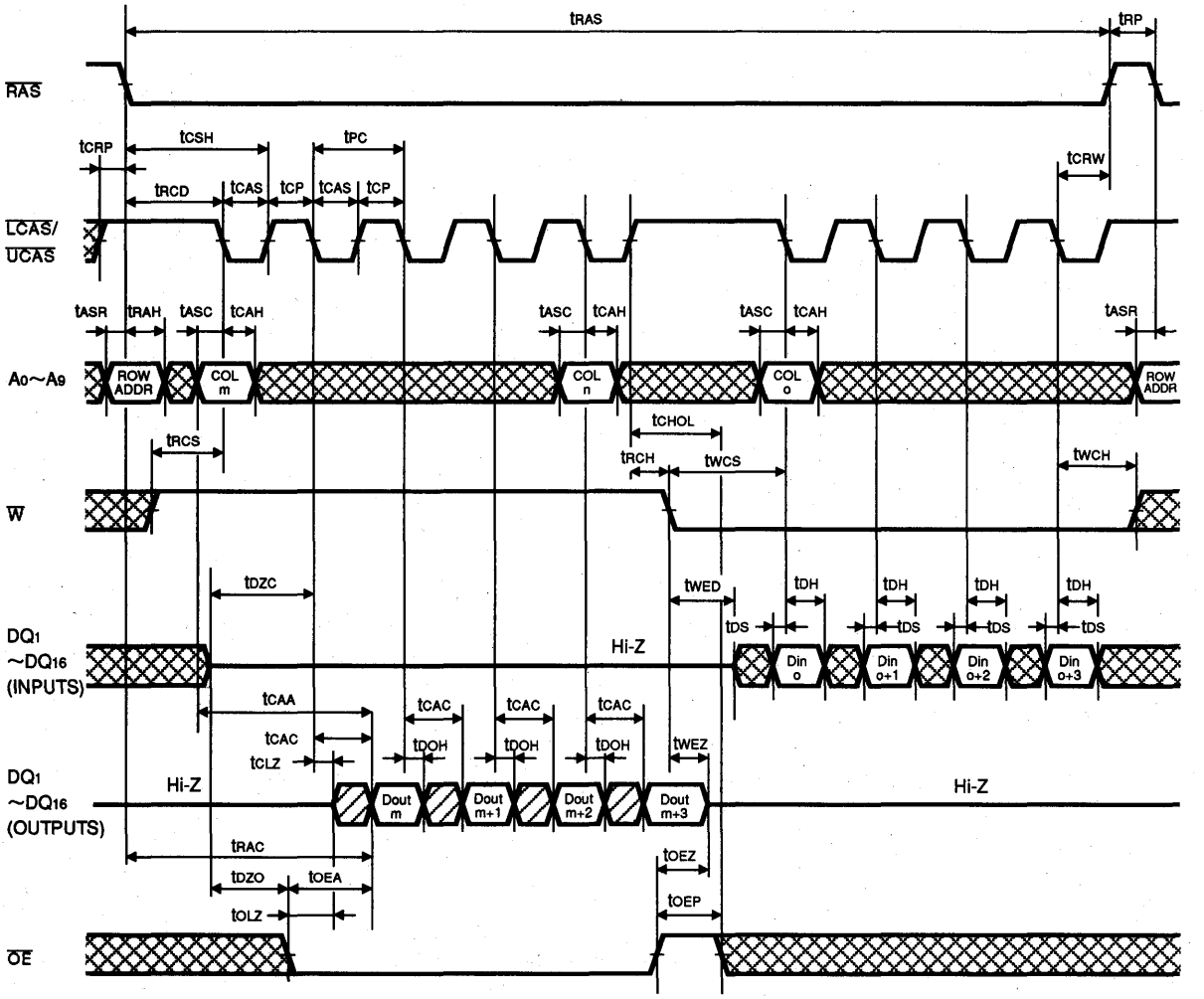
Pipeline Burst Mode Byte Write Cycle



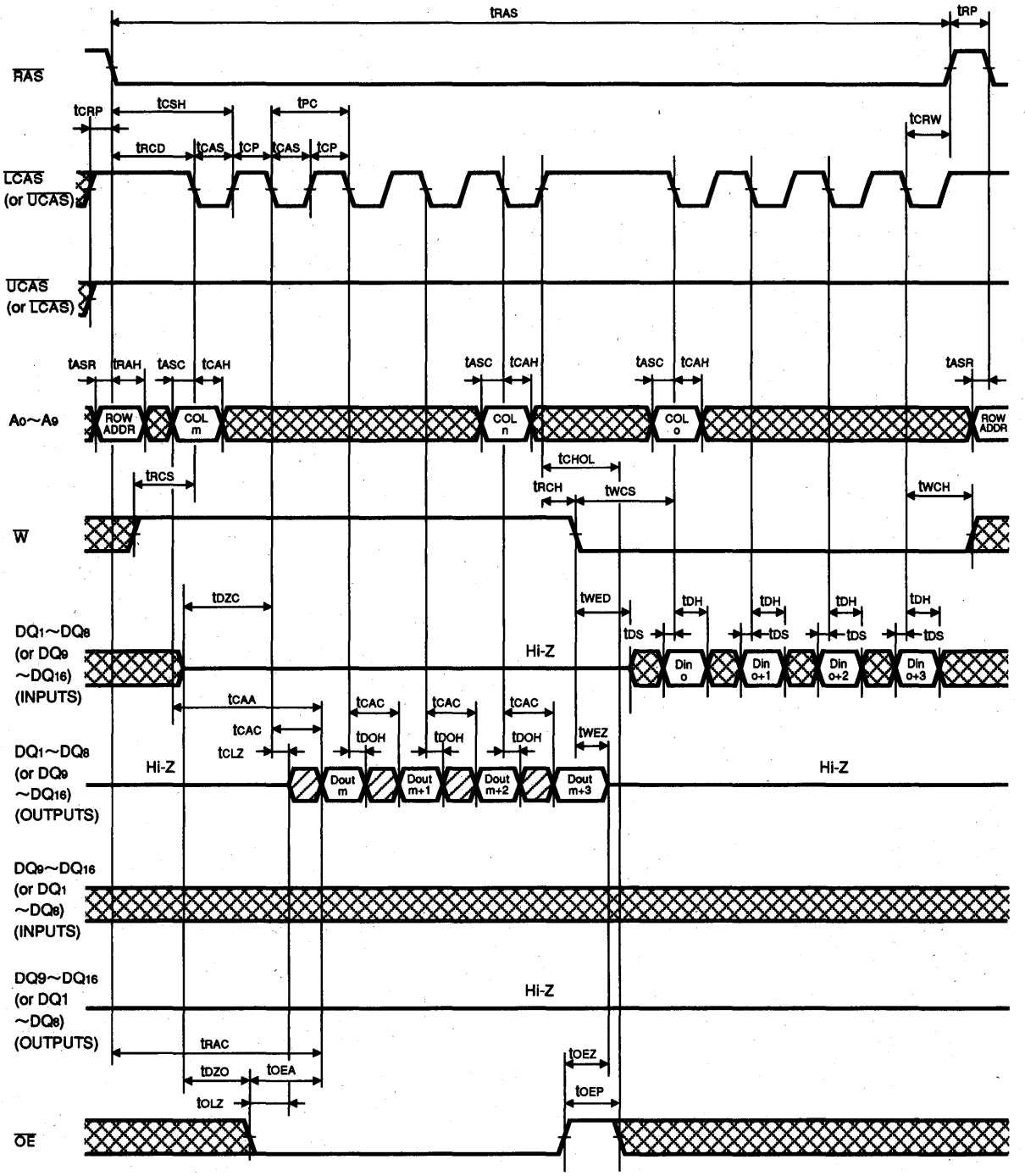
Pipeline Burst Mode Write Cycle (Write terminated Write)



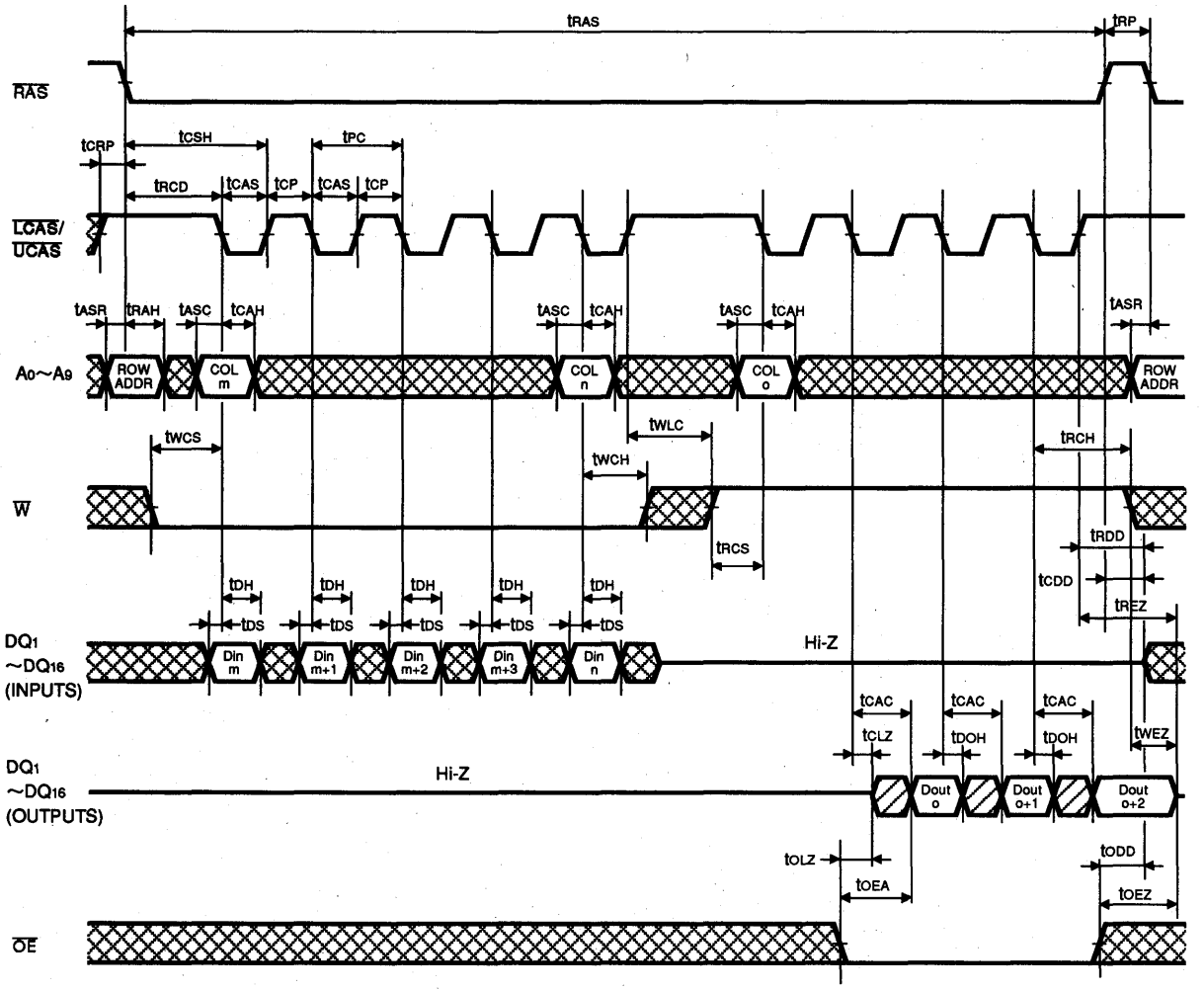
Pipeline Burst Mode Read-Write Cycle



Pipeline Burst Mode Byte Read-Write Cycle

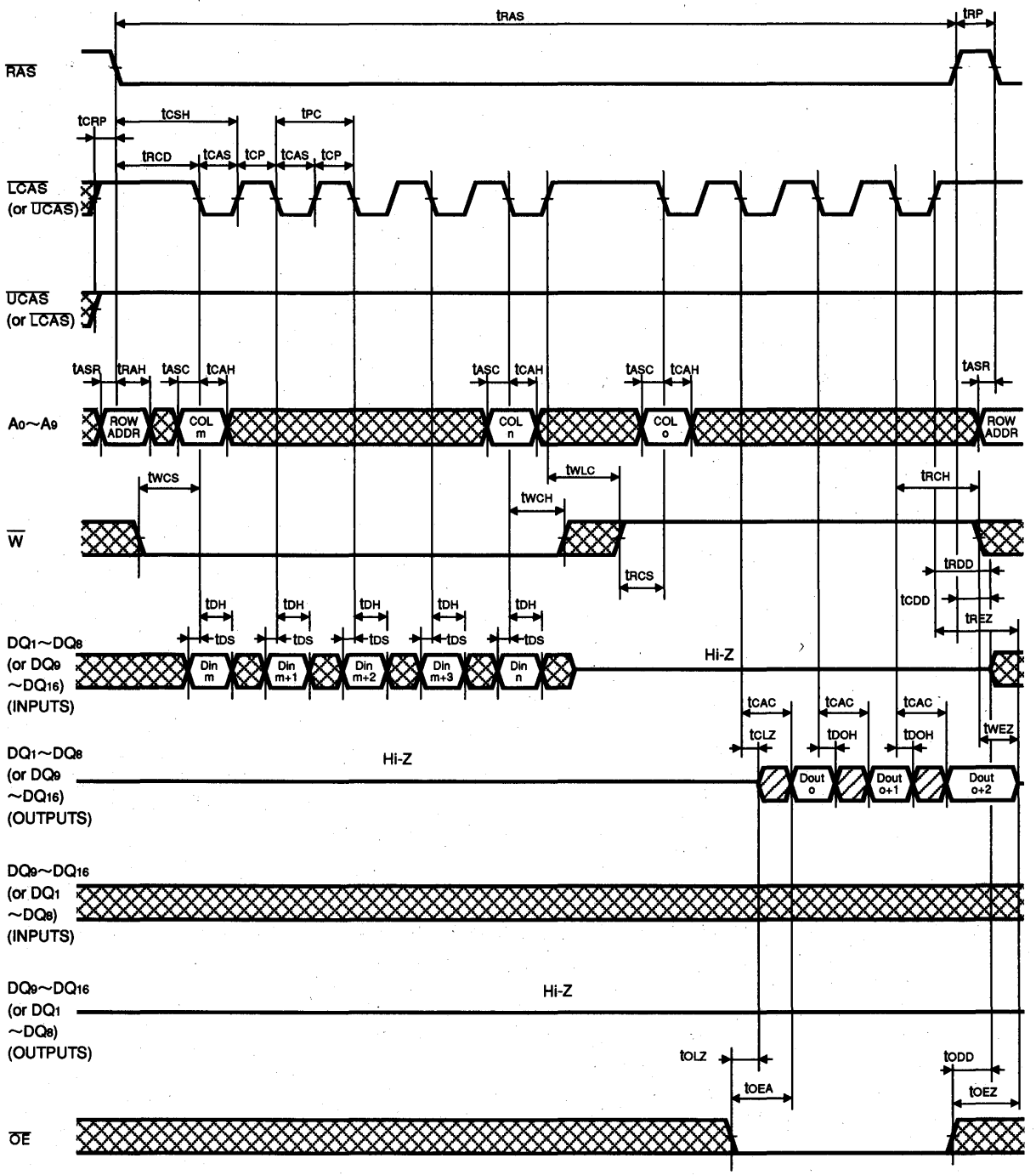


Pipeline Burst Mode Write-Read Cycle

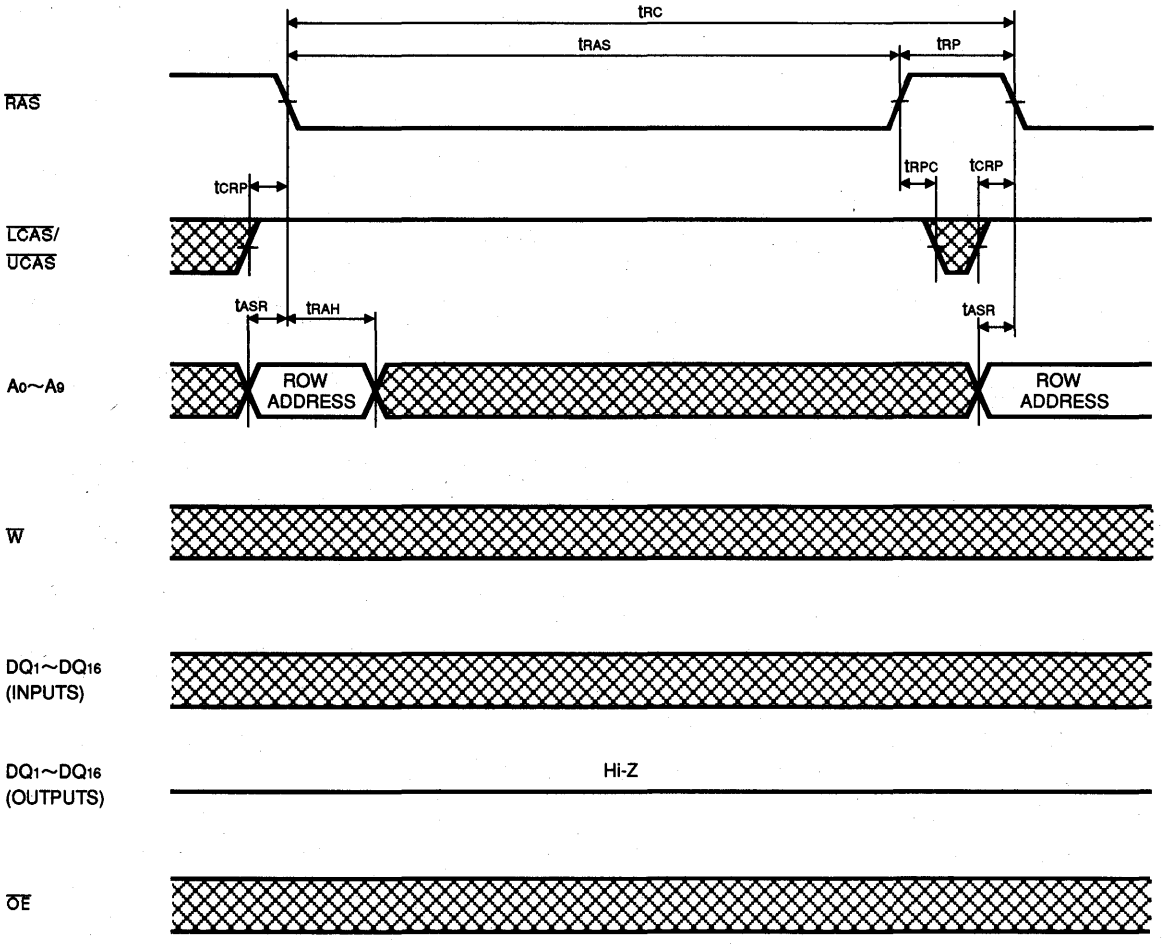


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

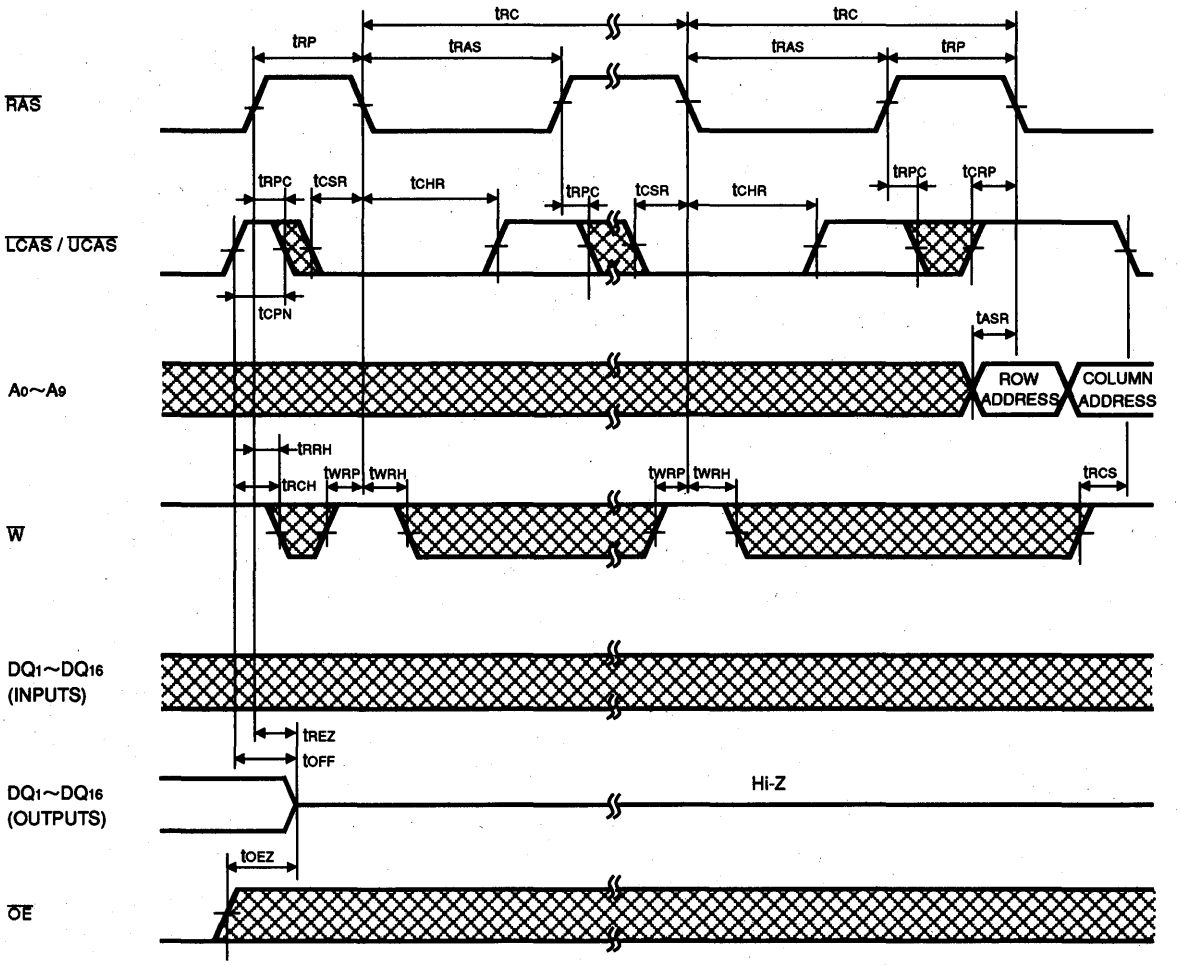
Pipeline Burst Mode Byte Write-Read Cycle



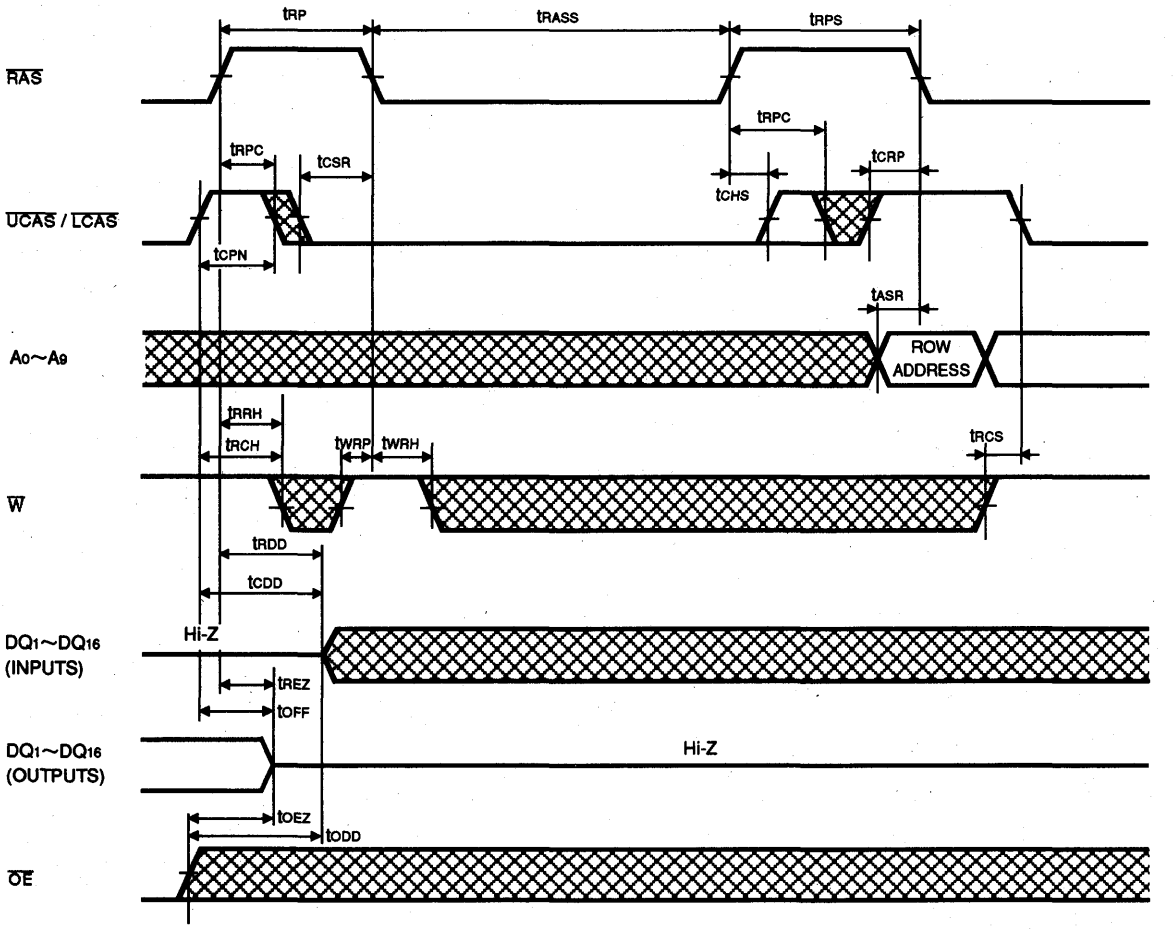
$\overline{RAS}$-only Refresh Cycle



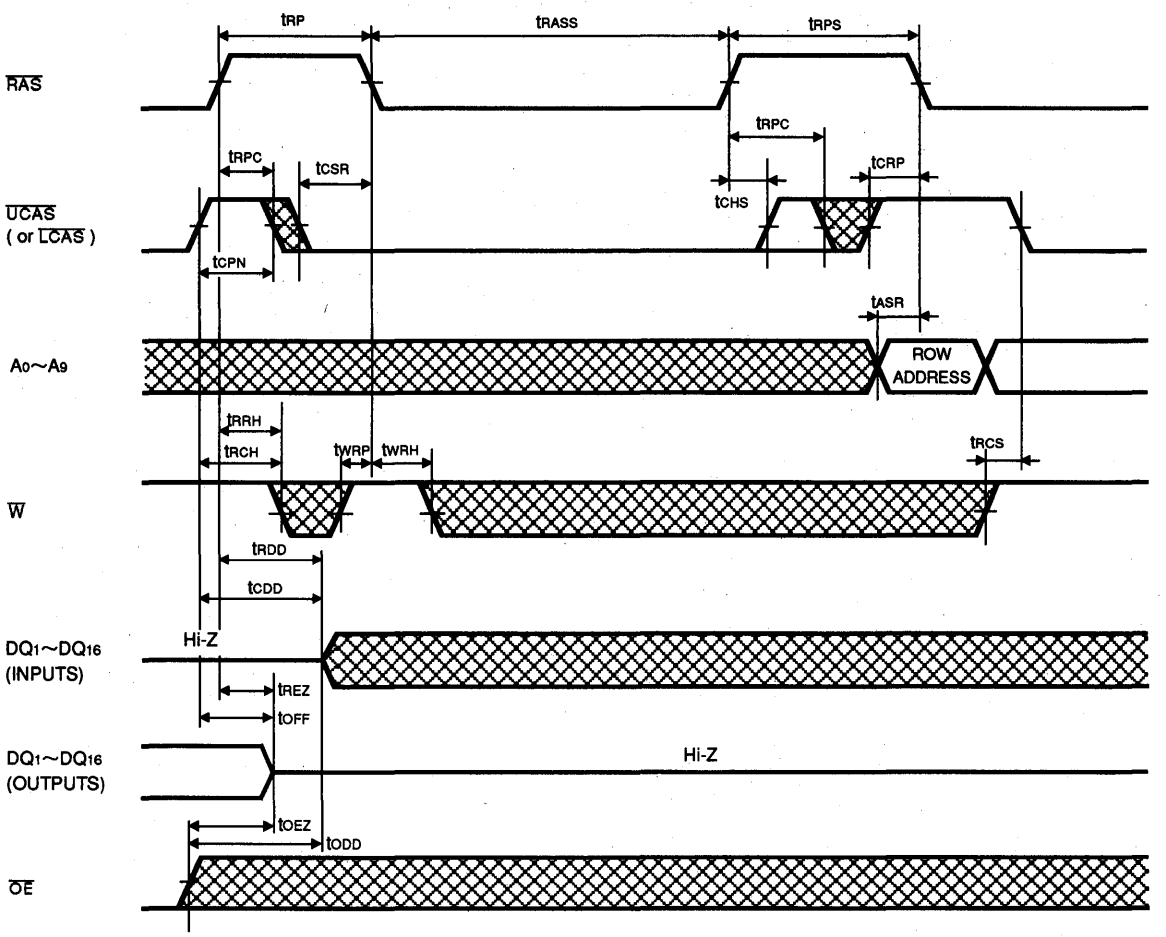
CAS before RAS Refresh Cycle, Extended Refresh Cycle *



Self Refresh Cycle*



Upper/(Lower) Self Refresh Cycle*



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SELF REFRESH SPECIFICATIONS *

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

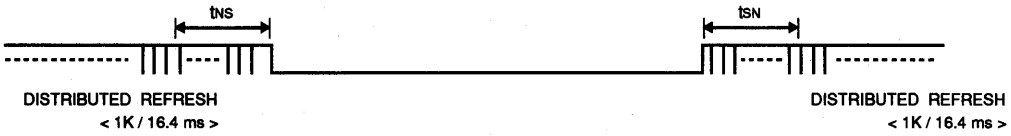
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5S		M5M4V18167C-6S		M5M4V18167C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		−50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

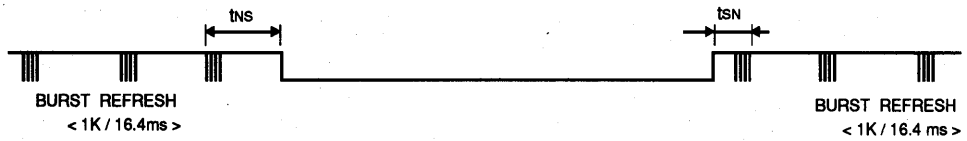
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 16.4$ ms and $t_{SN} \leqq 16.4$ ms.



(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 16.4$ ms.



16M SYNCHRONOUS DRAM(3.3V Version)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M4S16S31CTP-7,-8,-10

16777216-BIT (2-BANK x 1048576-WORD BY 8-BIT) SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The M5M4S16S31CTP is a 2-bank x 1048576-word by 8-bit Synchronous DRAM, with SSTL*1 interface. All inputs and out puts are referenced to the rising edge of CLK. The M5M4S16S31CTP realizes very high speed data transfer using 2-word parallel operation and small signal interface.

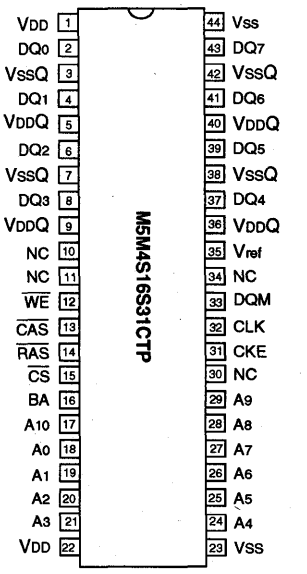
*1 SSTL : Stub Series Terminated Logic

FEATURES

Type name	Max. frequency	CLK access time
M5M4S16S31CTP-7	150MHz	5ns
M5M4S16S31CTP-8	125MHz	6ns
M5M4S16S31CTP-10	100MHz	8ns

- Single 3.3V±0.3V power supply
- Clock frequency 150MHz / 125MHz / 100MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA (Bank Address)
- $\overline{CAS}$ latency-1/2/3/4 (programmable)
- Burst length-1/2/4/8 (programmable)
- Burst type-sequential / interleave (programmable)
- Column access-2N-rule
- Auto precharge / All bank precharge controlled by A_{10}
- Auto refresh and Self refresh
- 4096 refresh cycles / 64ms
- SSTL Interface
- 300-mil, 44-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

PIN CONFIGURATION (TOP VIEW)



Outline 44P3L-B (300mil TSOP)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

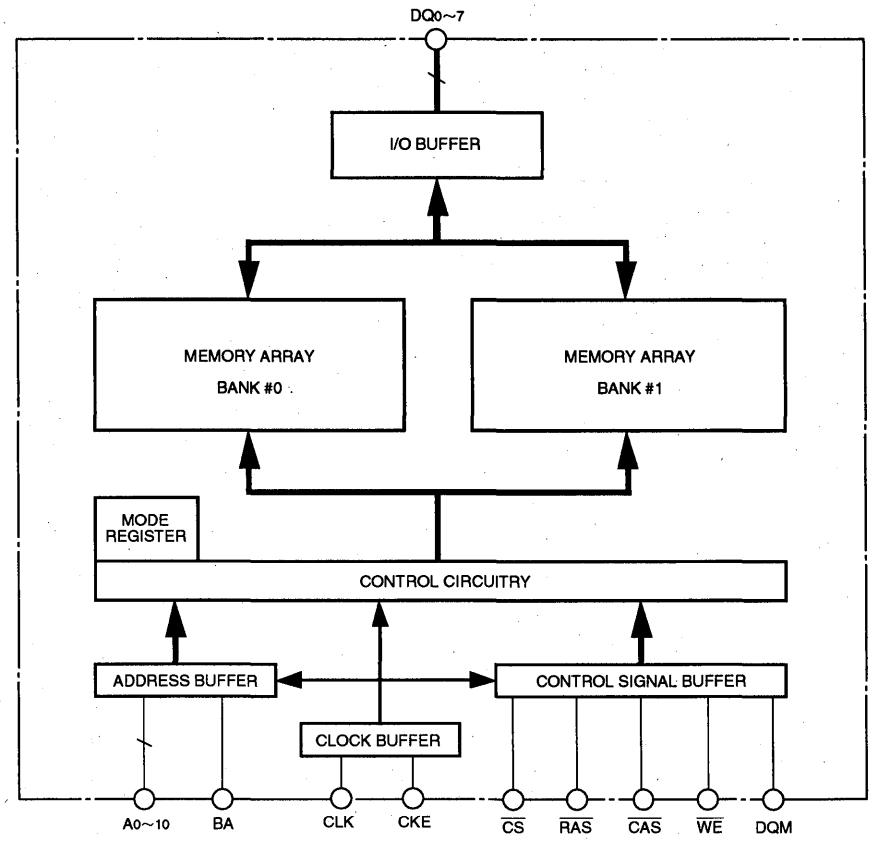
PIN DESCRIPTION

Pin name	Function
CLK	Master clock
CKE	Clock enable
CS	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$DQ_{0\sim7}$	Data I/O
DQM	Output disable/write mask
$A_{0\sim10}$	Address input
BA	Bank address
V_{ref}	Input reference voltage
V_{DD}	Power supply
V_{DDQ}	Power supply for output
Vss	Ground
VssQ	Ground for output

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

16777216-BIT (2-BANK x 1048576-WORD BY 8-BIT) SYNCHRONOUS DYNAMIC RAM

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PIN FUNCTION

Pin	I/O	Function
CLK	Input	Master clock : All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock enable : CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
$\overline{CS}$	Input	Chip select : When $\overline{CS}$ is high, any command means No operation.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Conbination of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ defines basic commands.
$A_{0\sim10}$	Input	$A_{0\sim10}$ specify the Row / Column address in conjunction with BA. The Row address is specified by $A_{0\sim10}$. The Column address is specified by $A_{0\sim9}$ ($\times4$), $A_{0\sim8}$ ($\times8$). A_{10} is also used to indicate precharge option. When A_{10} is high at a read / write command, an auto precharge is performed. When A_{10} is high at a precharge command, both banks are precharged.
BA	Input	Bank address: BA is not simply A_{11}. BA specifies the bank to which a command is applied. BA must be set with ACT, PRE, READ, WRITE commands.
$DQ_{0\sim7}$	Input / output	Data in and Data out are referenced to the rising edge of CLK.
DQM	Input	Din mask / output disable : When DQM is high in burst write, Din for the current cycle is masked. When DQM is high in burst read, Dout is disabled at the next but one cycle.
V_{DD}, V_{SS}	Power supply	Power supply for the memory array and peripheral circuitry.
V_{DDQ}, V_{SSQ}	Power supply	V_{DDQ} and V_{SSQ} are supplied to the output buffers only.
V_{ref}	Input	Reference voltage for all inputs. V_{ref} should be typically $0.45\times V_{DDQ}$.

PRELIMINARY
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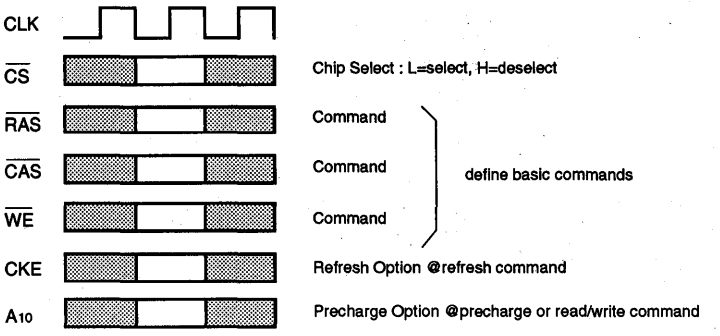
16777216-BIT (2-BANK x 1048576-WORD BY 8-BIT) SYNCHRONOUS DYNAMIC RAM

BASIC FUNCTIONS

The M5M4S16S31CTP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at CLK rising edge. In addition to 3 signals, $\overline{CS}$,CKE and A_{10} are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [$\overline{RAS}$=L, $\overline{CAS}$=$\overline{WE}$=H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [$\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=H]

READ command starts burst read from the active bank indicated by BA. First output data appears after $\overline{CAS}$ latency. When A_{10}=H at this command, the bank is deactivated after the burst read (auto-precharge, **READ A**).

Write (WRITE) [$\overline{RAS}$=H, $\overline{CAS}$=$\overline{WE}$=L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A_{10}=H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITE A**).

Precharge (PRE) [$\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A_{10} =H at this command, both banks are deactivated (precharge all, **PRE A**).

Auto-Refresh (REFA) [$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=CKE=H]

REF A command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

Command	Mnemonic	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10}	$A_{0\sim9}$
Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	V	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number
Note 1. $A_{7\sim9}$ =0, $A_{0\sim6}$ =Mode Address

FUNCTION TRUTH TABLE

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A_{10}	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A_{10}	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A_{10}	READ / READA	Terminate Burst, Latch CA, Bigin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A_{10}	READ / READA	Terminate Burst, Latch CA, Bigin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A_{10}	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A_{10}	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	NOP*4 (Idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after t_{RCD})
	L	H	H	H	X	NOP	NOP (Row Active after t_{RCD})
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after t_{RC})
	L	H	H	H	X	NOP	NOP (Idle after t_{RC})
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t_{RSC})
	L	H	H	H	X	NOP	NOP (Idle after t_{RSC})
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS : H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No OPeration

Note 1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n-rule", bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

PRELIMINARY
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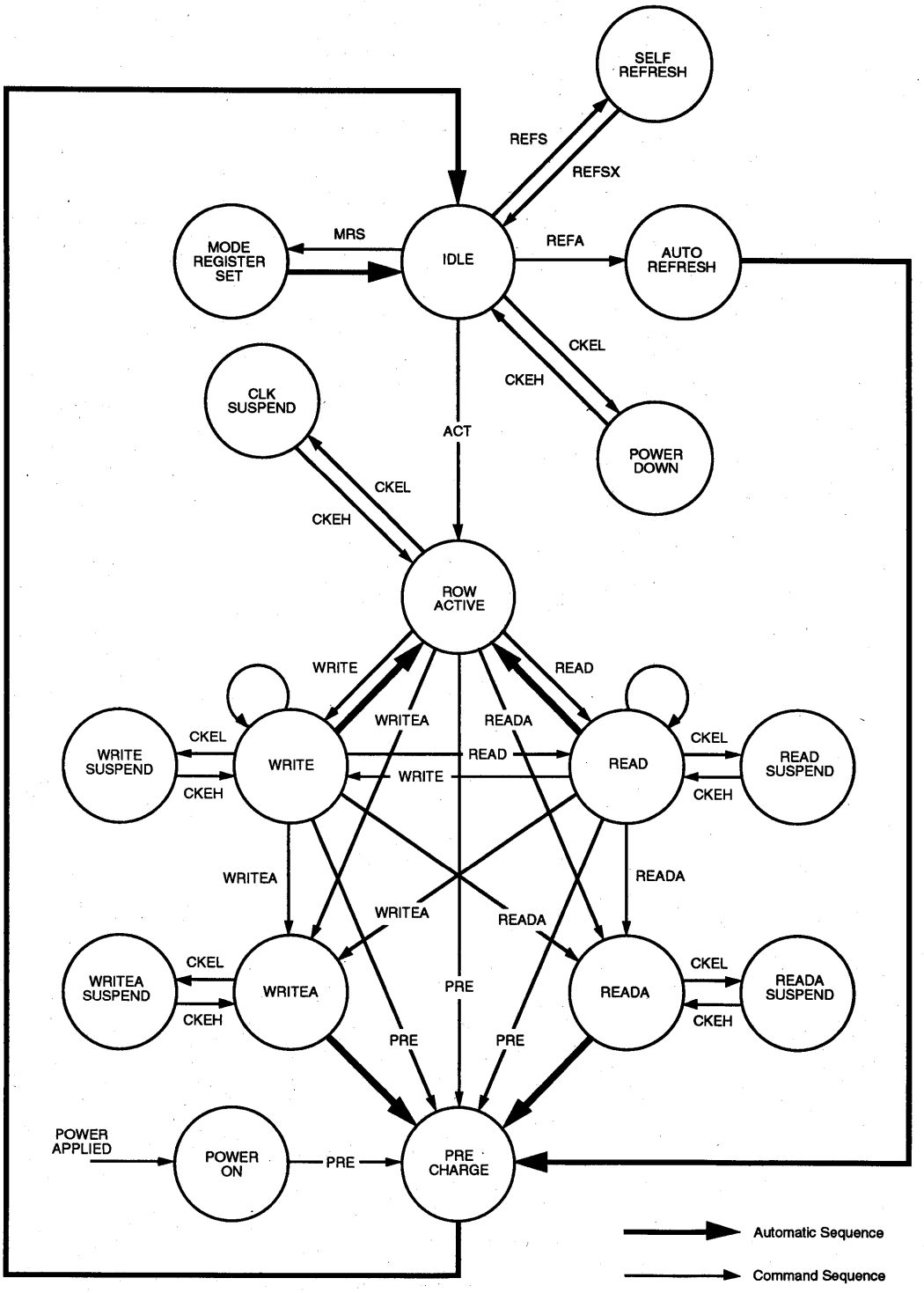
FUNCTION TRUTH TABLE for CKE

Current state	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS : H=High Level, L=Low Level, X=Don't Care

Note 1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

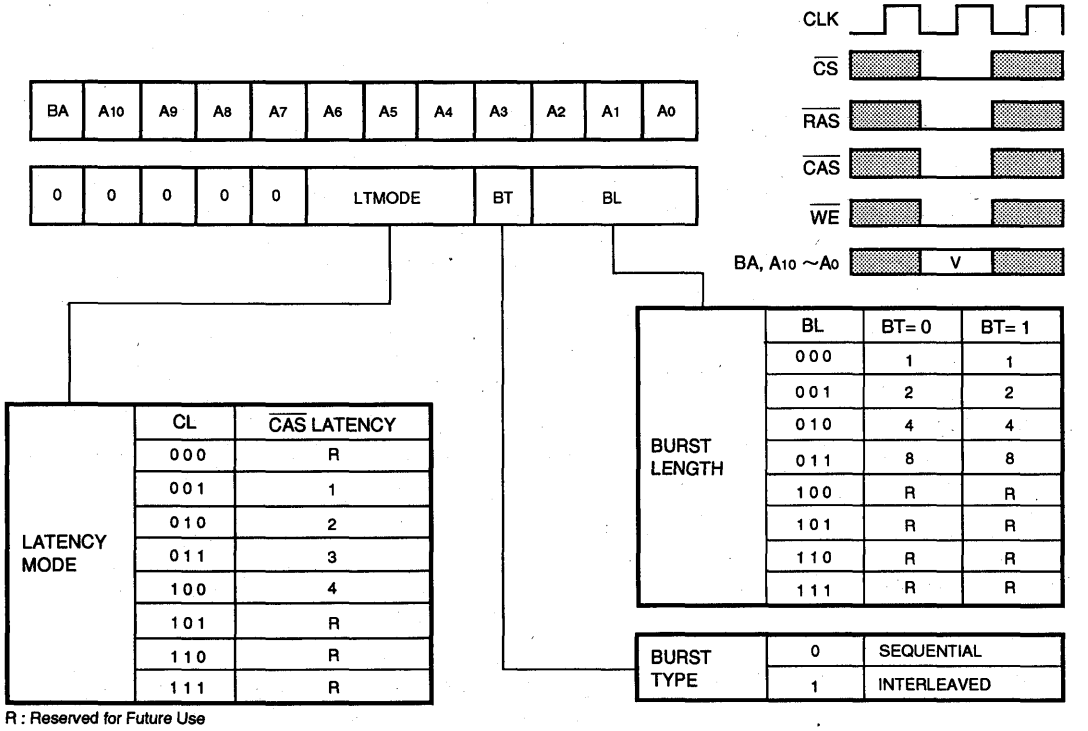
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after t_{RP}), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and $\overline{CAS}$ Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After t_{RSC} from a MRS command, the SDRAM is ready for new command.

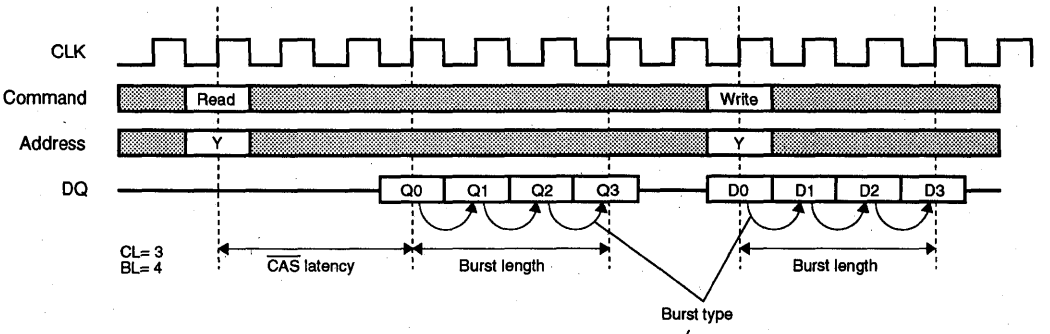


LATENCY MODE	CL	CAS LATENCY
	000	R
	001	1
	010	2
	011	3
	100	4
	101	R
	110	R
	111	R

R : Reserved for Future Use

BURST LENGTH	BL	BT= 0	BT= 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	R	R

BURST TYPE		
	0	SEQUENTIAL
	1	INTERLEAVED



Initial address			BL	Column addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATIONAL DESCRIPTION

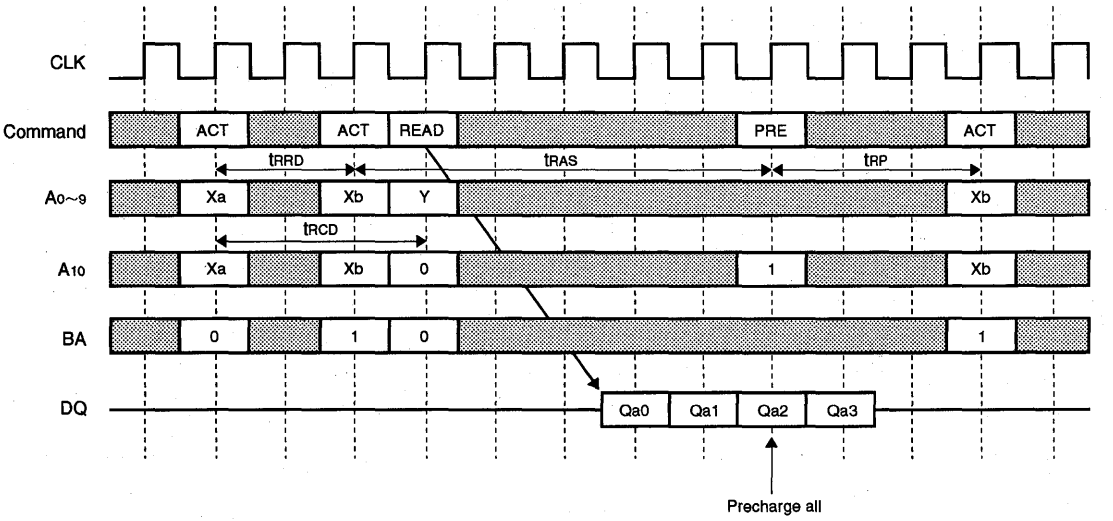
BANK ACTIVATE

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address (BA). A row is indicated by the row address A_{10}~0. The minimum activation interval between one bank and the other bank is t_{RRD}.

PRECHARGE

The PRE command deactivates the bank indicated by BA. When both banks are active, the precharge all command (PREA, PRE+ A_{10}=H) is available to deactivate them at the same time. After t_{RP} from the precharge, an ACT command can be issued.

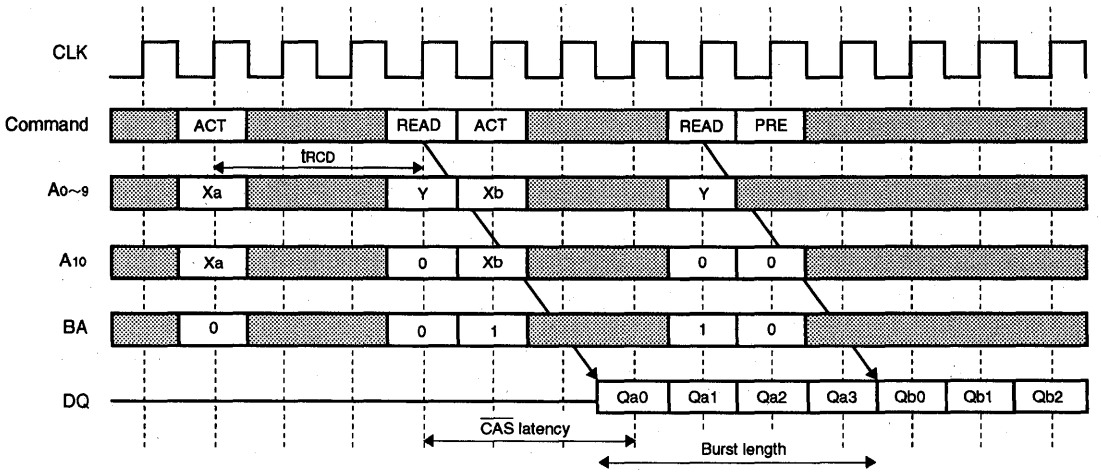
Bank Activation and Precharge All (BL=4, CL=3)



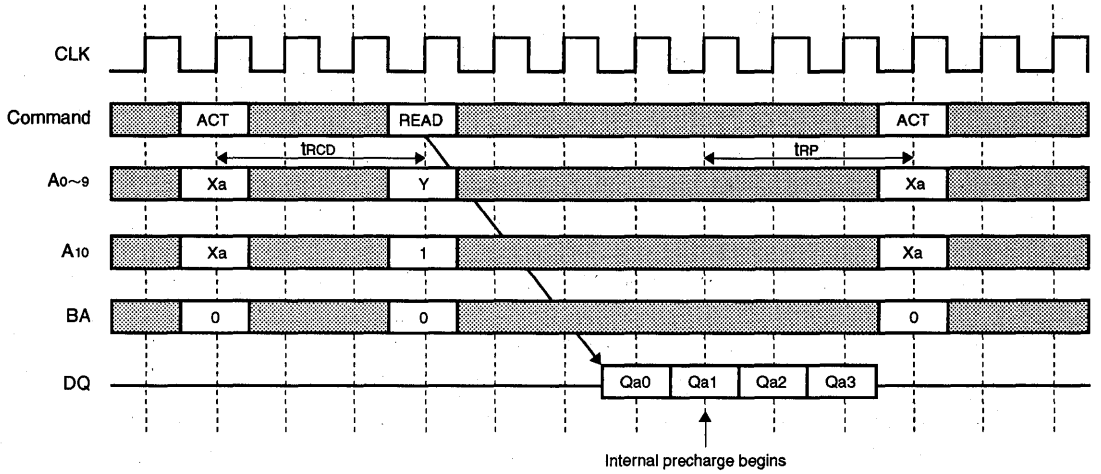
READ

After t_{RCD} from the bank activation, a READ command can be issued. 1st output data is available after the $\overline{CAS}$ Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A_8~0 (×8) / A_9~0 (× 4), and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (t_{RP}) can be hidden behind continuous output data (in case of BL=8) by interleaving the dual banks. When A_{10} is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge start timing depends on $\overline{CAS}$ Latency. The next ACT command can be issued after t_{RP} from the internal precharge timing.

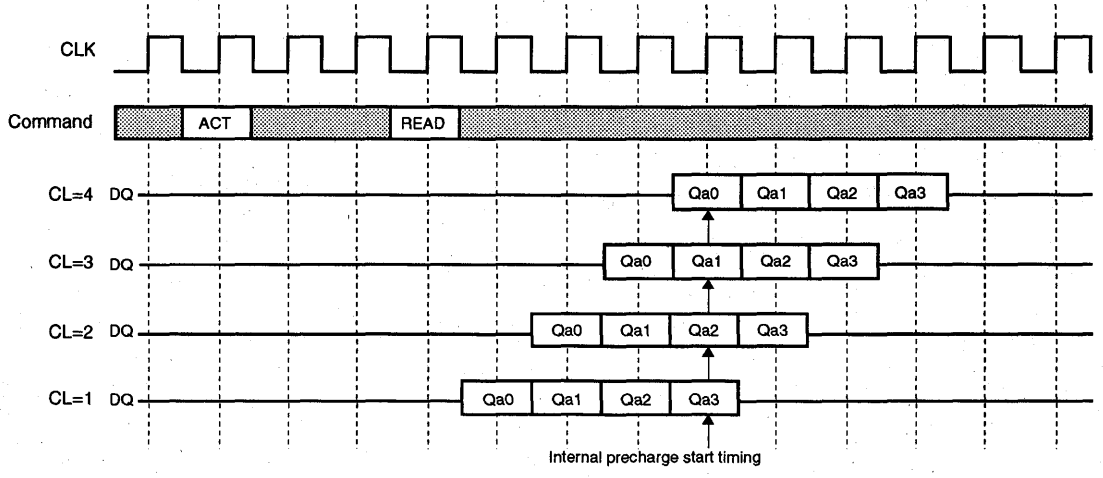
Dual Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



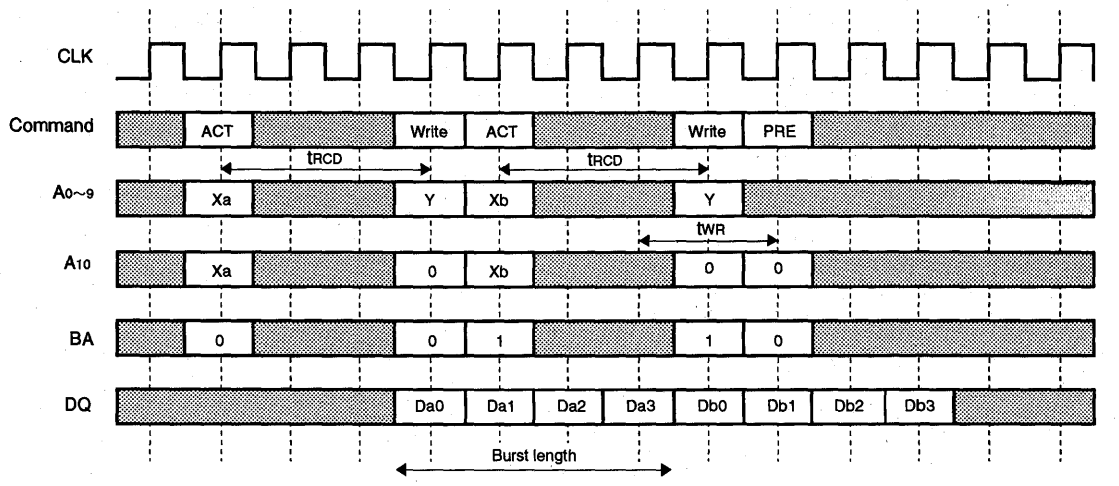
READ Auto-Precharge Timing (BL=4)



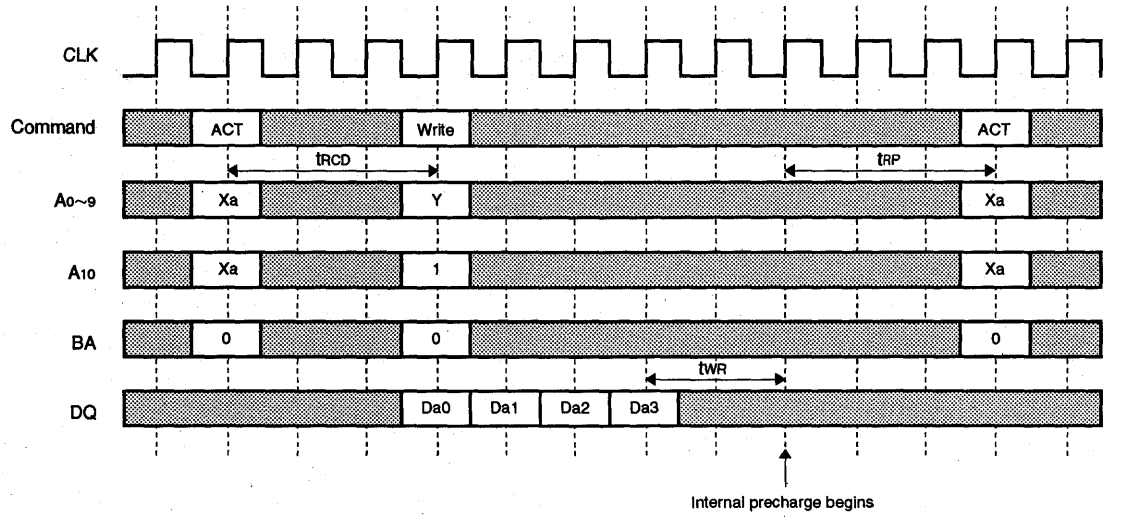
WRITE

After t_{RCD} from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL-1) data are written into the RAM, when the Burst Length is BL. The start address is specified by $A_{8\sim0}$ (×8) / $A_{9\sim0}$ (×4), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (t_{RP}) can be hidden behind continuous input data (in case of BL=8) by interleaving the dual banks. From the last input data to the PRE command, the write recovery time (t_{WR}) is required. When A_{10} is high at a WRITE command, the auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at t_{WR} after the last input data cycle. The next ACT command can be issued after t_{RP} from the internal precharge timing.

Dual Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

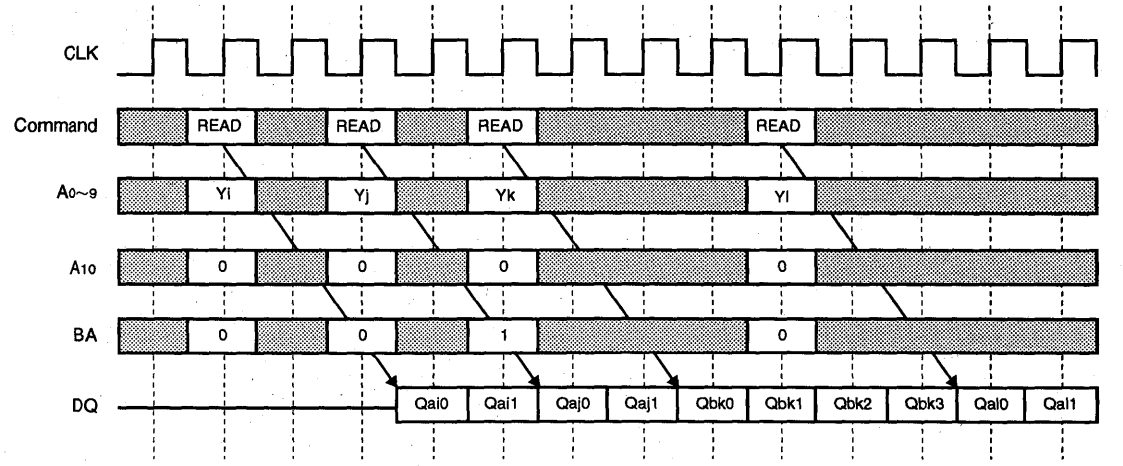


BURST INTERRUPTION

〔Read Interrupted by Read〕

Burst read operation can be interrupted by new read of the same or the other bank. As M5M4S16S31CTP/ M5M4S16S21CTP adopt 2-words parallel transfer architecture to realize very high speed data rate, JEDEC 2n-rule is required, where 2, 4 or 6 read to read interval is allowed in case of BL=8.

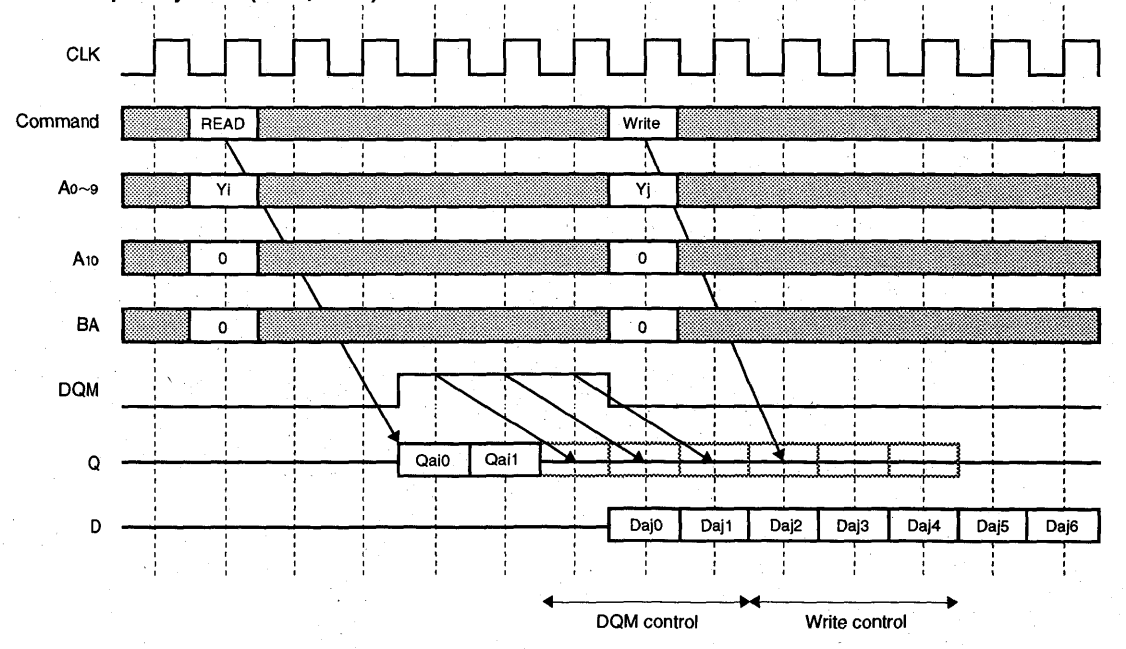
Read Interrupted by Read (BL=8, CL=3)



〔Read Interrupted by Write〕

Burst read operation can be interrupted by write of the same or the other bank. JEDEC 2n-rule also must be kept here. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 2 cycles after WRITE assertion.

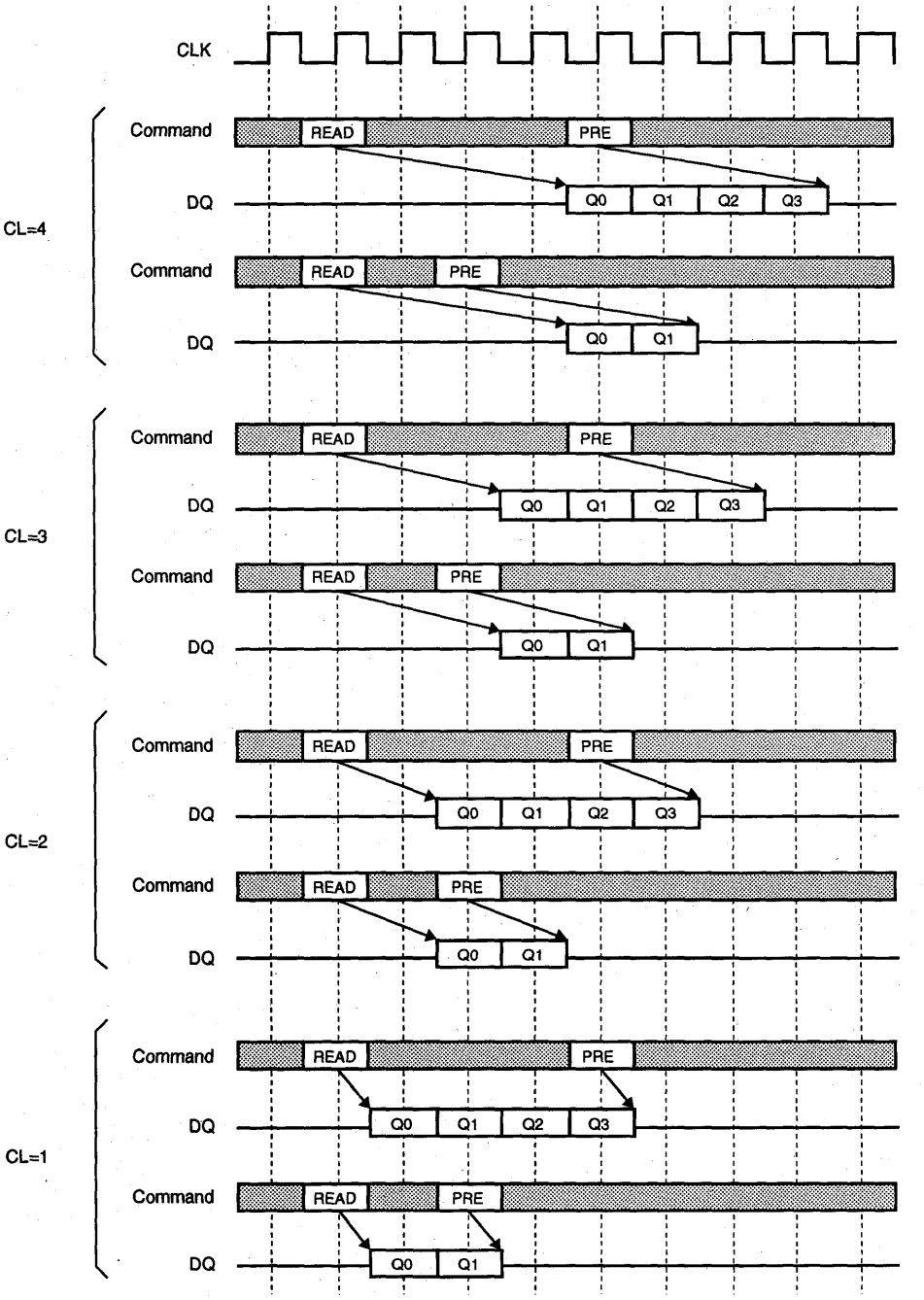
Read Interrupted by Write (BL=8, CL=3)



〔Read Interrupted by Precharge〕

Burst read operation can be interrupted by precharge of the same bank. JEDEC 2n-rule also must be kept here. A PRE command disables the data output, depending on the CAS Latency. The figure below shows when the dataout is terminated.

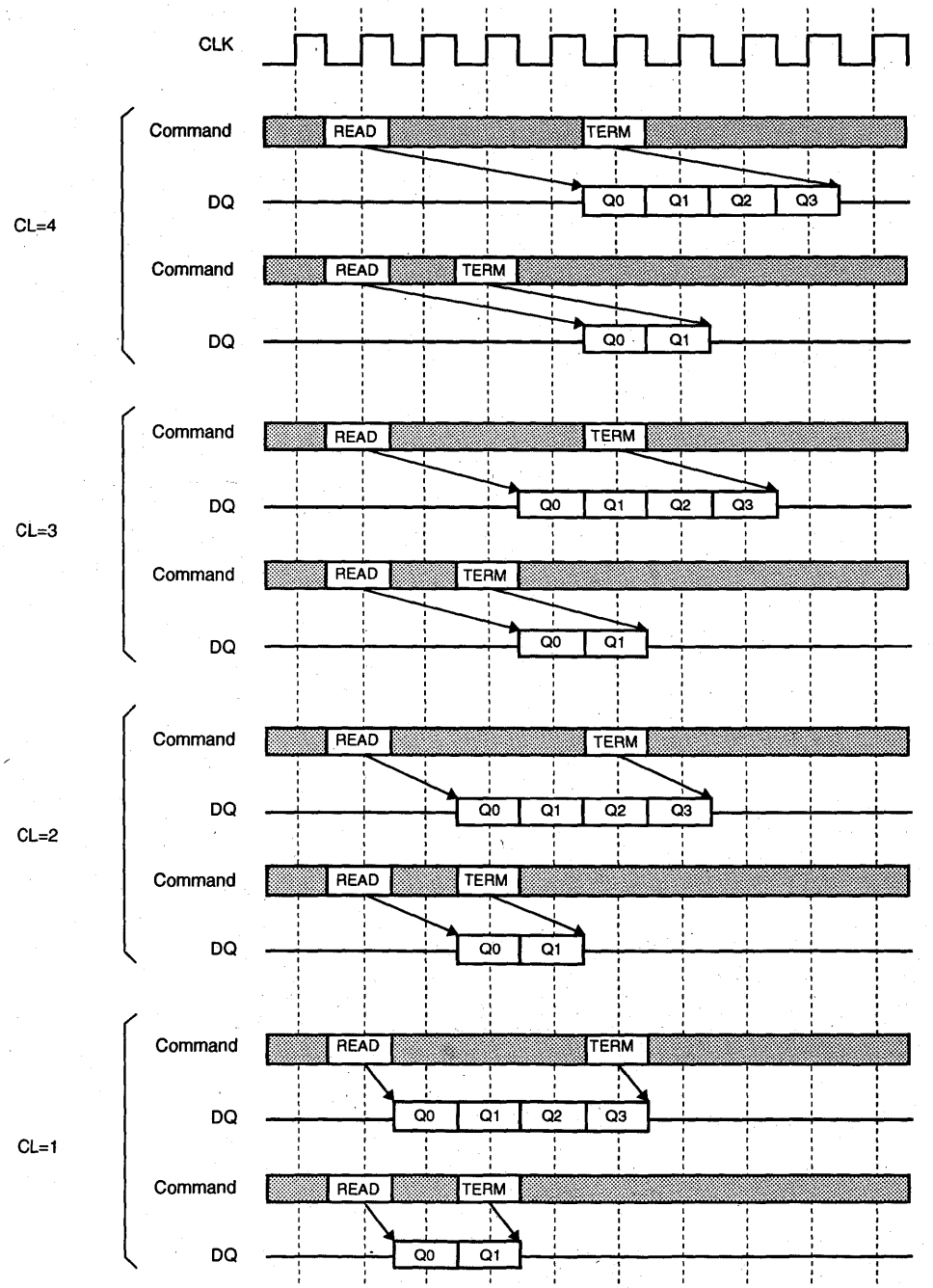
Read Interrupted by Precharge (BL=4)



〔Read Interrupted by Burst Terminate〕

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. JEDEC 2n-rule also must be kept here. The figure below shows when the dataout is terminated.

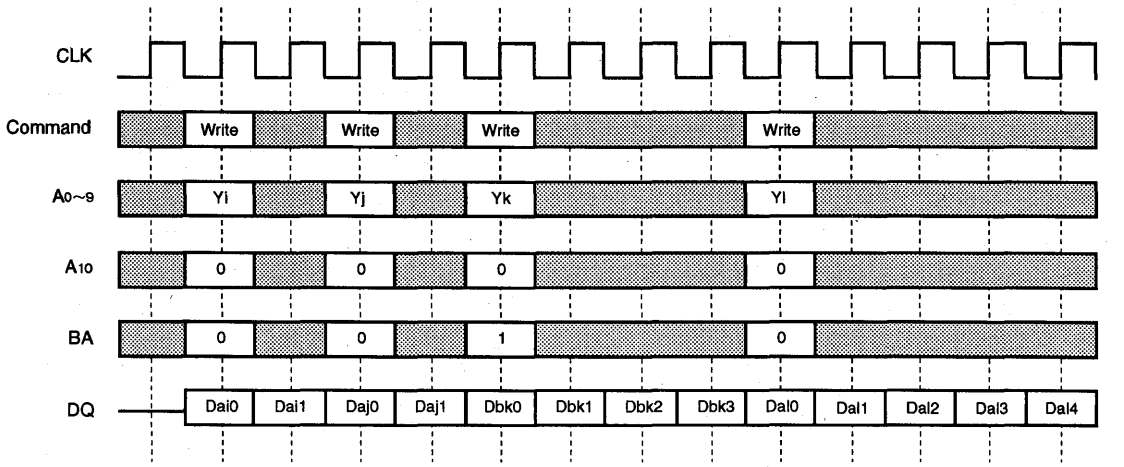
Read Interrupted by Burst Terminate (BL=4)



〔**Write Interrupted by Write**〕

Burst write operation can be interrupted by new write of the same or the other bank. JEDEC 2n-rule also must be kept. 2, 4 or 6 write to write interval is allowed in case of BL=8.

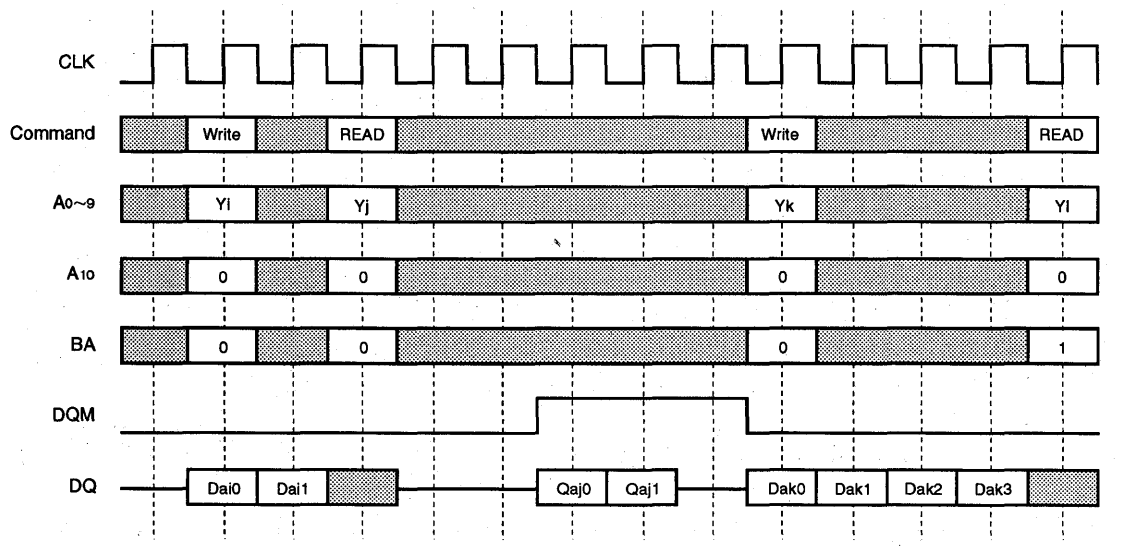
Write Interrupted by Write (BL=8)



〔**Write Interrupted by Read**〕

Burst write operation can be interrupted by read of the same or the other bank. JEDEC 2n-rule also must be kept here. The input data on DQ at the interrupting READ cycle is "don't care".

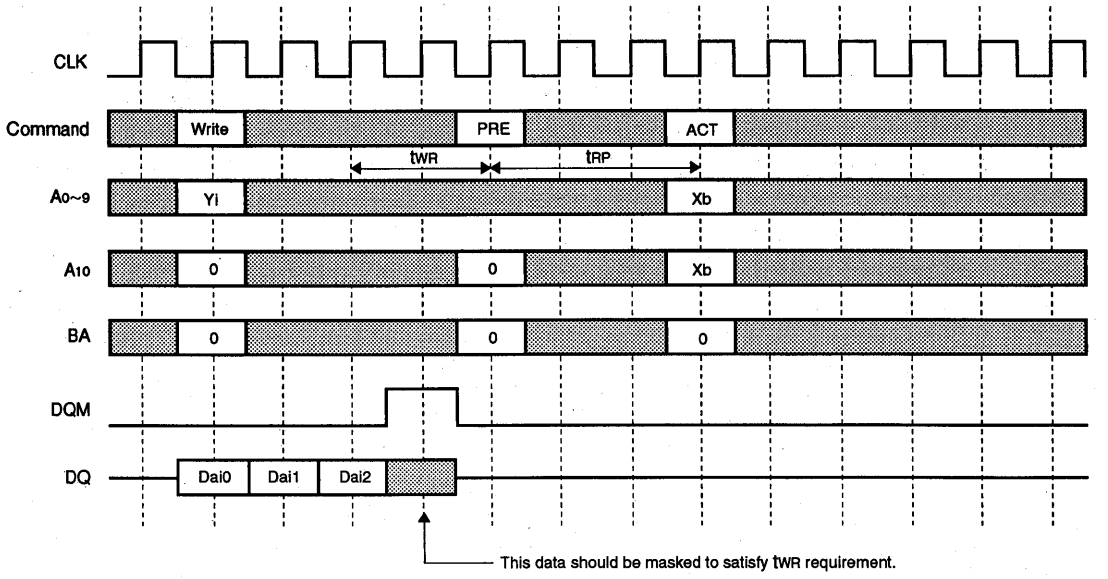
Write Interrupted by Read (BL=8, CL=3)



〔**Write Interrupted by Precharge**〕

Burst write operation can be interrupted by precharge of the same bank. JEDEC 2n-rule also must be kept here. Because the write recovery time (tWR) is required between the last input data and the next PRE, 4th data should be masked with DQM shown as below.

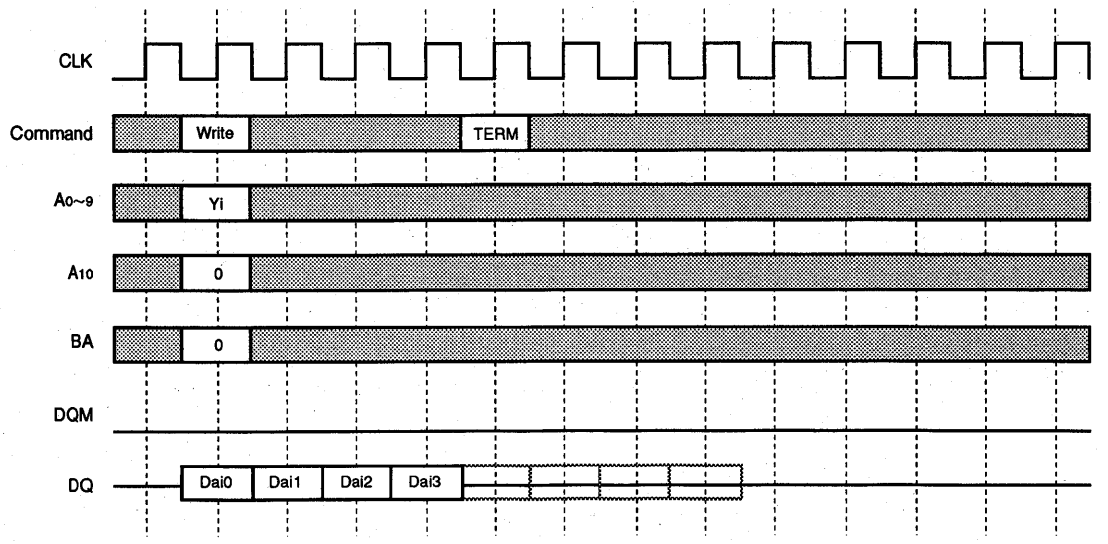
Write Interrupted by Precharge (BL=8)



〔**Write Interrupted by Burst Terminate**〕

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 4 words of data are written. JEDEC 2n-rule also must be kept here.

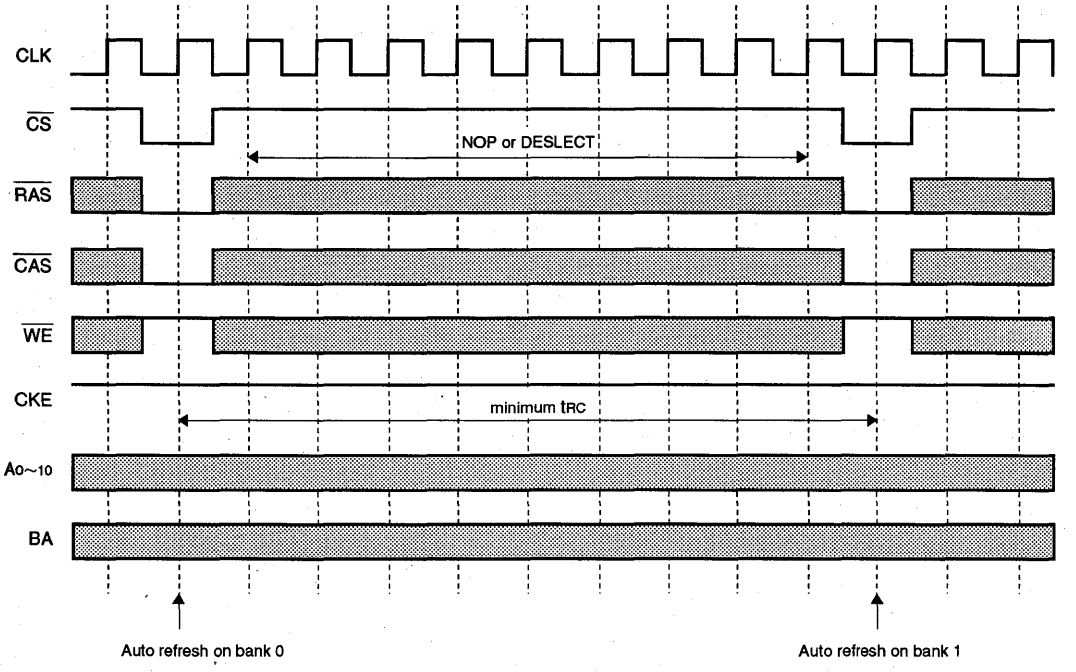
Write Interrupted by Burst Terminate (BL=8)



AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA ($\overline{CS}$=$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 16Mbit memory cells. The auto-refresh is performed on each bank alternately (ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before t_{RC} from the REFA command.

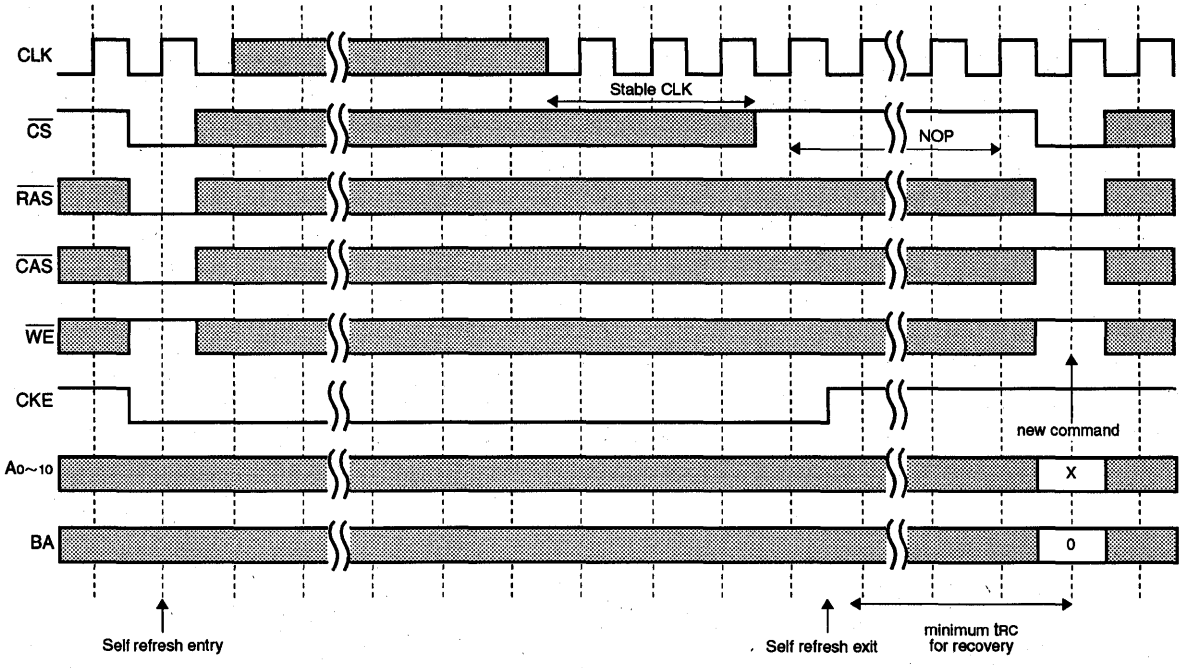
Auto-Refresh



SELF REFRESH

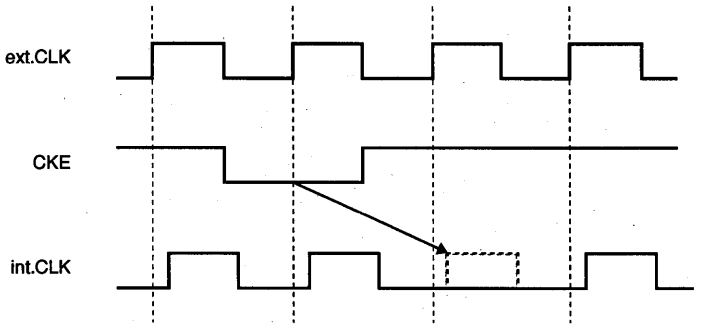
Self-refresh mode is entered by issuing a REFS command ($\overline{CS}$=$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=H, CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input (but asynchronous), all other inputs including CLK are disabled and ignored, and power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE (REFSX). After t_{RC} from REFSX both banks are in the idle state and a new command can be issued after t_{RC}, but DESEL or NOP commands must be asserted till then.

Self-Refresh

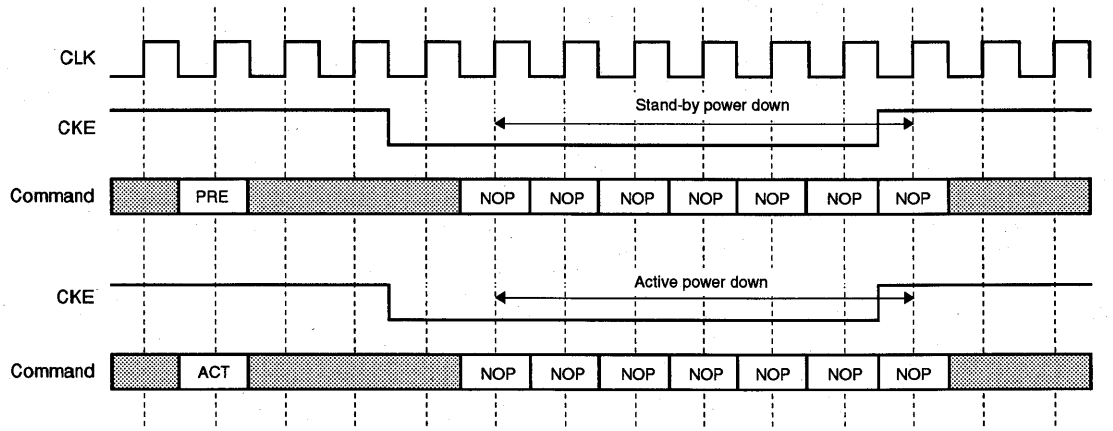


CLK SUSPEND

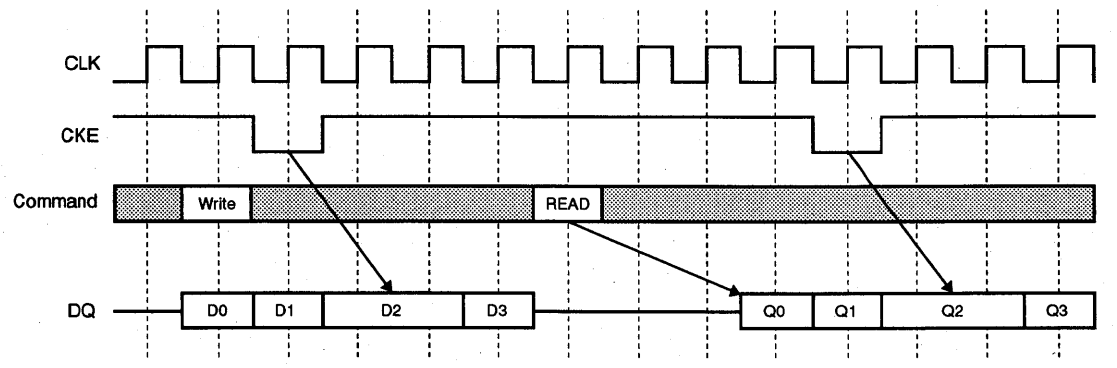
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



Power Down by CKE



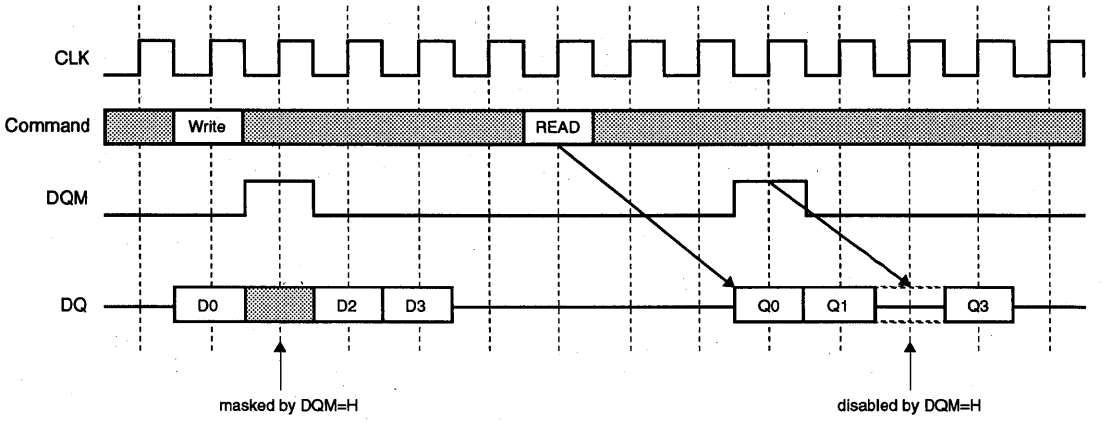
DQ Suspend by CKE



DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQM masks input data word by word. DQM to write mask latency is 0. During reads, DQM forces output to Hi-Z word by word. DQM to output Hi-Z latency is 2.

DQM Function



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_{DDQ}	Supply voltage for output	With respect to VssQ	-0.5~4.6	V
V_I	Input voltage	With respect to Vss	-0.5~4.6	V
V_O	Output voltage	With respect to VssQ	-0.5~4.6	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25 °C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{DDQ}	Supply voltage for output	3.0	3.3	3.6	V
VssQ	Supply voltage for output	0	0	0	V
V_{REF}	Input reference voltage	1.3	1.5	1.7	V
V_{IH}	High-level input voltage, all inputs	V_{REF}+0.4		V_{DDQ}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		V_{REF}-0.4	V
V_{TT}	Termination voltage	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V

CAPACITANCE (Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, V_{REF}=0.45×V_{DDQ}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address pin	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(C)}$	Input capacitance, control pin				5	pF
$C_{I(K)}$	Input capacitance, CLK pin				5	pF
$C_{I/O}$	Input capacitance, I/O pin				7	pF

AVERAGE SUPPLY CURRENT from V_{DD} (Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			M5M4S16S31CTP			
			-7	-8	-10	
			Max	Max	Max	
I_{CC1S}	Operating current, single bank	t_{RC}=min, t_{CLK}=min, BL=1, CL=3 or 4	155	140	115	mA
I_{CC1d}	Operating current, dual bank	t_{RC}=min, t_{CLK}=min, BL=1, CL=3 or 4	230	205	170	mA
I_{CC2h}	Stand-by current, CKE=H	Both banks idle, t_{CLK}=min, CKE=H	65	60	50	mA
I_{CC2l}	Stand-by current, CKE=L	Both banks idle, t_{CLK}=min, CKE=L	10	9	7	mA
I_{CC3}	Active stand-by current	Both banks active, t_{CLK}=min, CKE=H	95	80	65	mA
I_{CC4}	Burst current	t_{CLK}=min, BL=4, CL=3 or 4, 1 bank idle	120	100	80	mA
I_{CC5}	Auto-refresh current	t_{RC}=min, t_{CLK}=min	140	125	105	mA
I_{CC6}	Self-refresh current		8	8	8	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, V_{TT}=0.45×V_{DDQ}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$V_{OH(DC)}$	High-level output voltage (DC)	I_{OH}=16mA	V_{TT}+0.8		V
$V_{OL(DC)}$	Low-level output voltage (DC)	I_{OL}=16mA		V_{TT}-0.8	V
I_{OZ}	Off-state output current	Q floating V_O=0 ~ V_{DDQ}	-10	10	µA
I_I	Input current	V_{IH} = 0 ~ V_{DDQ}+0.3V	-10	10	µA

PRELIMINARY
Notice: This is not a final specification.
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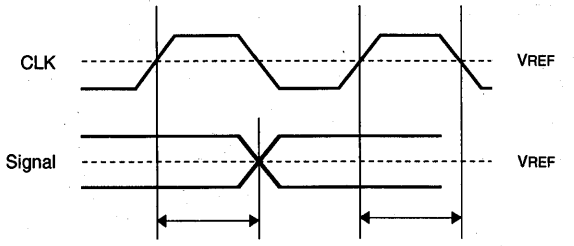
16777216-BIT (2-BANK x 1048576-WORD BY 8-BIT) SYNCHRONOUS DYNAMIC RAM

AC TIMING REQUIREMENTS (Ta=0~70°C, V_{DD}=V_{DD}Q=3.3±0.3V, V_{SS}=V_{SS}Q=0V, V_{REF}=0.45×V_{DD}Q, unless otherwise noted)

Input pulse levels ---------- V_{REF}±0.4V

Input timing measurement level ---------- V_{REF}

Symbol	Parameter		Limits						Unit
			M5M4S16S31CTP-7		M5M4S16S31CTP-8		M5M4S16S31CTP-10		
			Min	Max	Min	Max	Min	Max	
t_{CLK}	CLK cycle time	CL=1	27		28		30		ns
		CL=2	13.5		14		15		ns
		CL=3	9		9.5		10		ns
		CL=4	6.7		8		10		ns
t_{CH}	CLK high pulse width		2.5		3		4		ns
t_{CL}	CLK low pulse width		2.5		3		4		ns
t_T	Transition time of CLK		1	10	1	10	1	10	ns
t_{IS}	Input setup time (all inputs)		1.5		1.5		2		ns
t_{IH}	Input hold time (all inputs)		0.5		1		1		ns
t_{RC}	Row cycle time		80		90		100		ns
t_{RCD}	Row to column delay		21		24		30		ns
t_{RAS}	Row active time		50	10000	55	10000	60	10000	ns
t_{RP}	Row precharge time		28		32		40		ns
t_{WR}	Write recovery time		14		16		20		ns
t_{RRD}	Act to act delay time		21		24		30		ns
t_{RSC}	Mode register set cycle time		14		16		20		ns
t_{PDE}	Power down exit time		7		8		10		ns
t_{REF}	Refresh interval time			65.6		65.6		65.6	ms



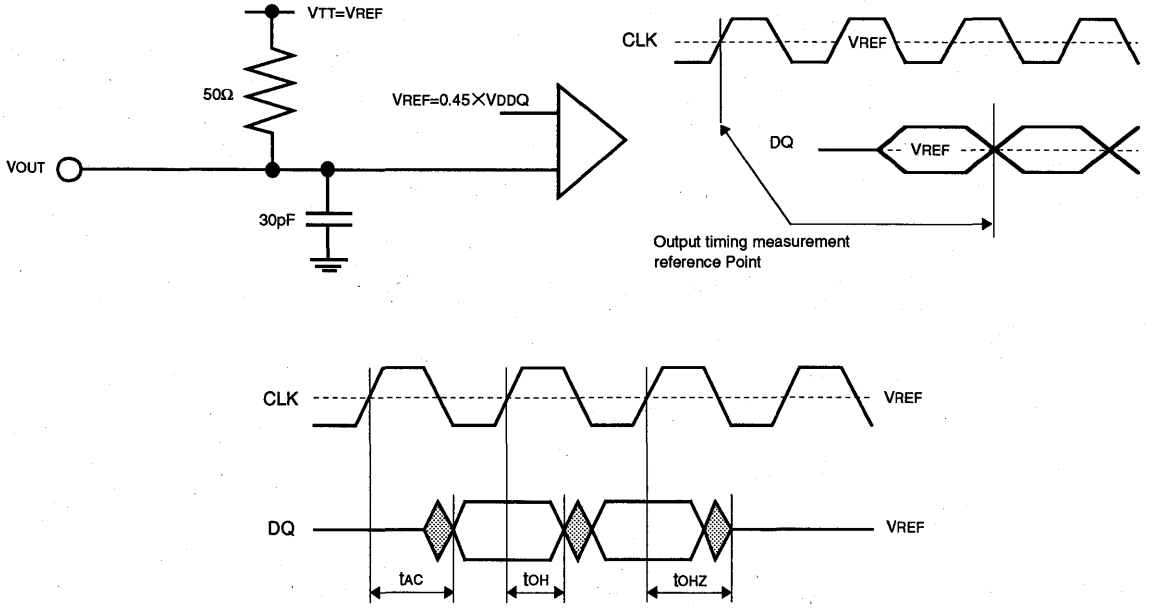
Any AC timing is referenced to the input signal crossing through the VREF level.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

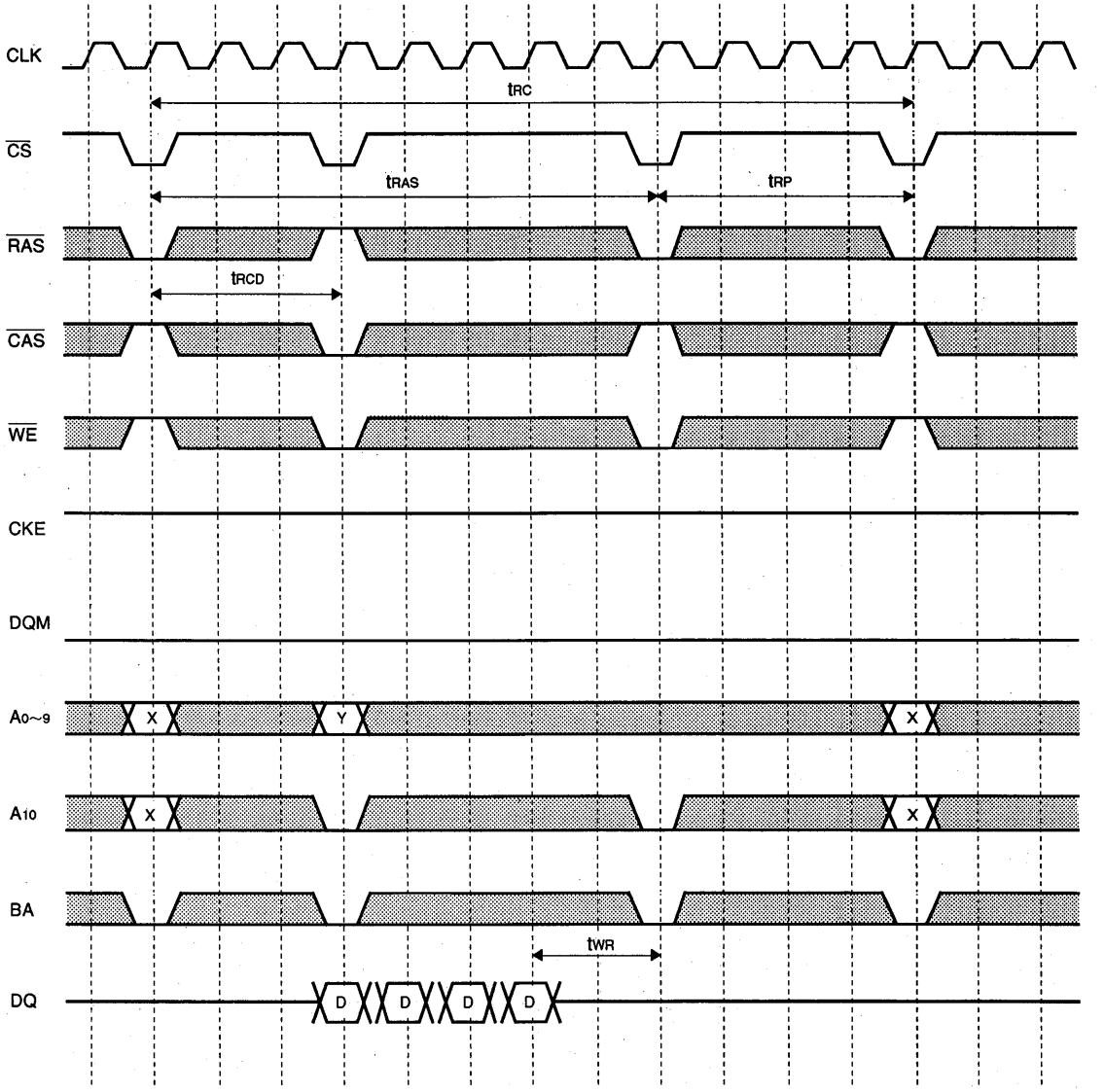
SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{DD}=V_{DD}Q=3.3±0.3V, V_{SS}=V_{SS}Q=0V, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			M5M4S16S31CTP-7		M5M4S16S31CTP-8		M5M4S16S31CTP-10		
			Min	Max	Min	Max	Min	Max	
t_{AC}	Access time from CLK	CL=1		25		26		27	ns
		CL=2		11.5		12		12	ns
		CL=3		7		7		8	ns
		CL=4		5		6		8	ns
t_{CAC}	Column access time			25		26		27	ns
t_{RAC}	Row access time			50		55		57	ns
t_{OH}	Output hold time from CLK		2		2.5		3		ns
t_{OLZ}	Delay time, output low impedance from CLK		0		0		0		ns
t_{OHZ}	Delay time, output high impedance from CLK		2	7	2.5	8	3	10	ns

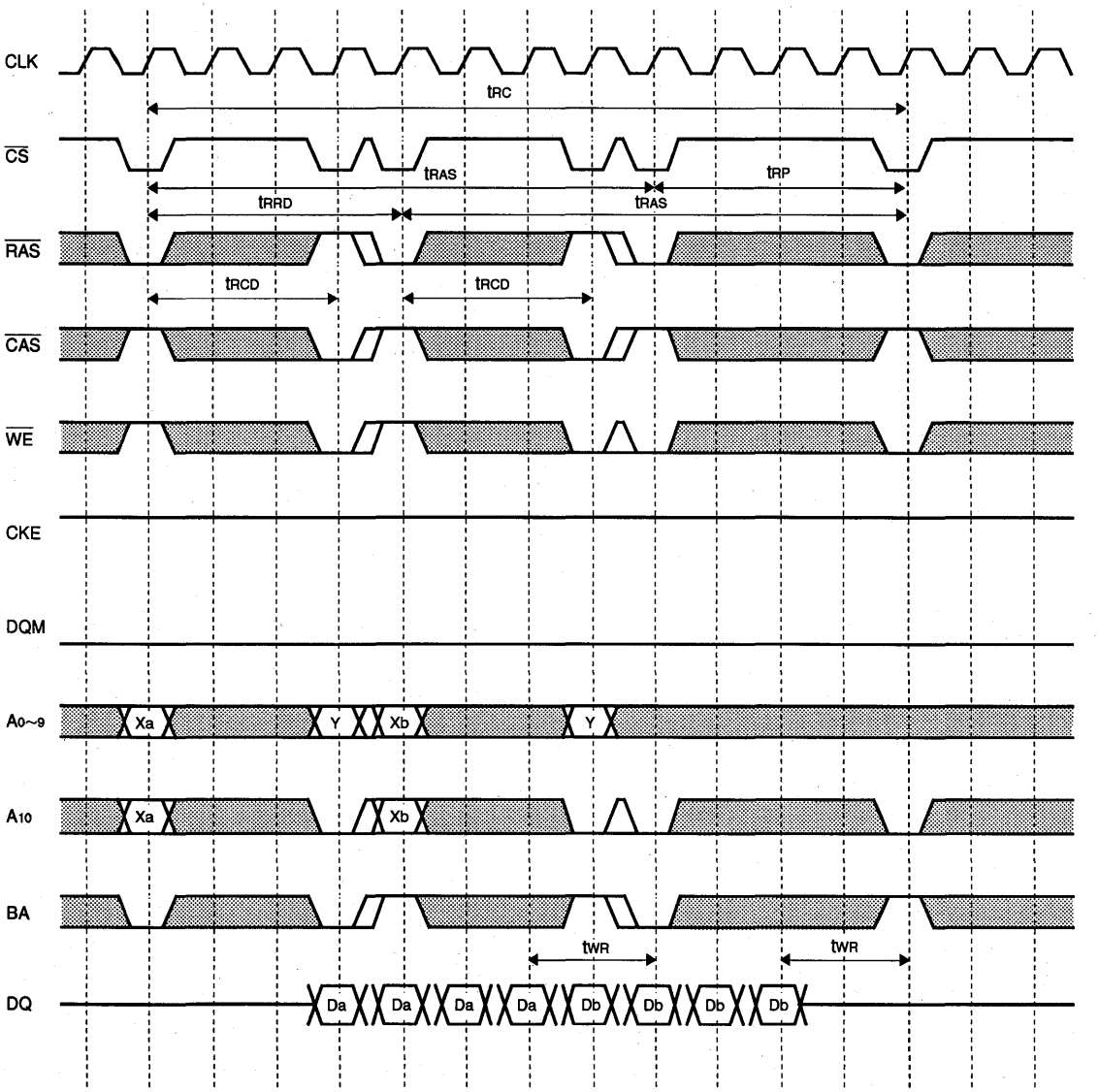
OUTPUT LOAD CONDITION



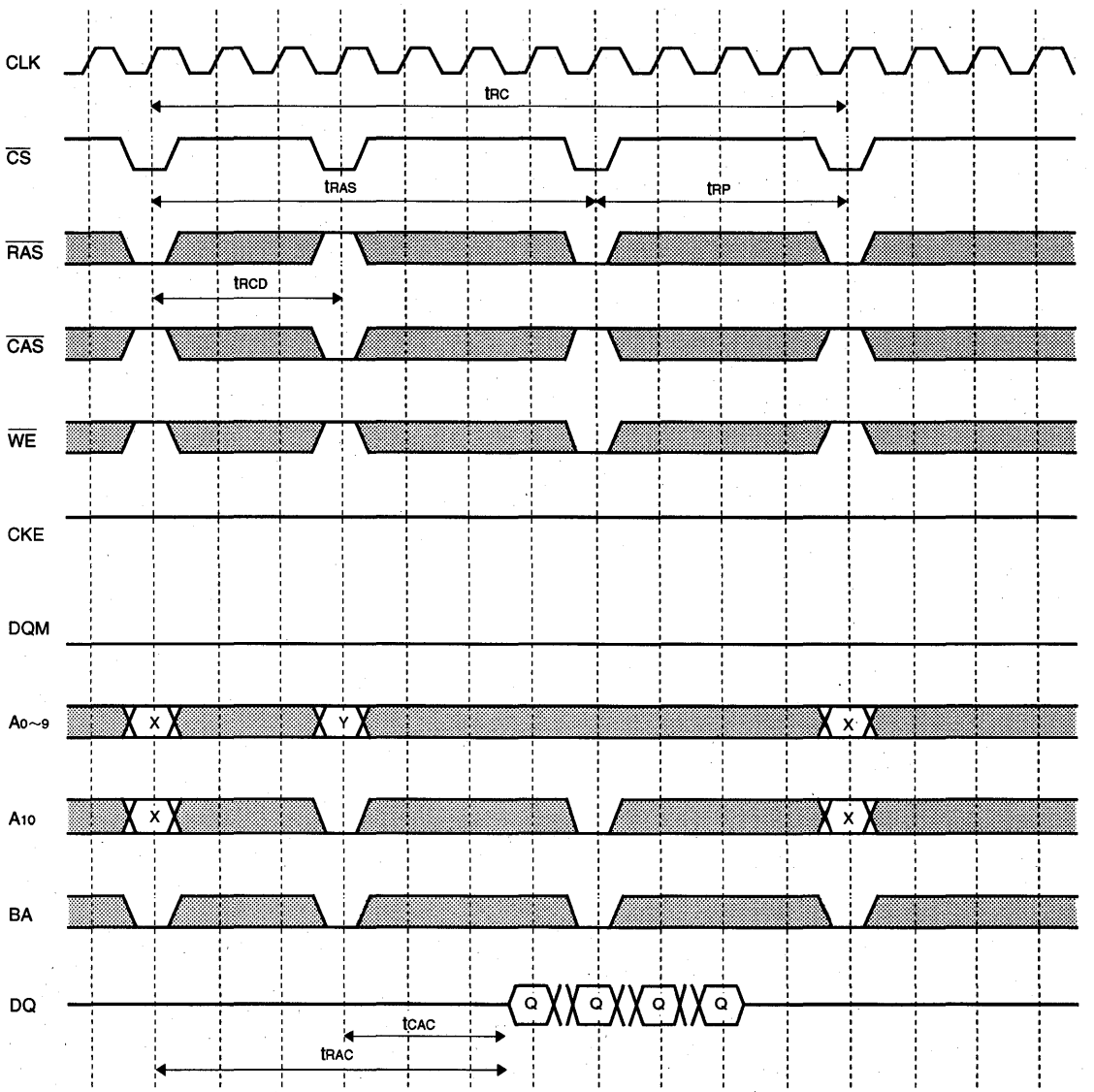
WRITE CYCLE (single bank) BL=4



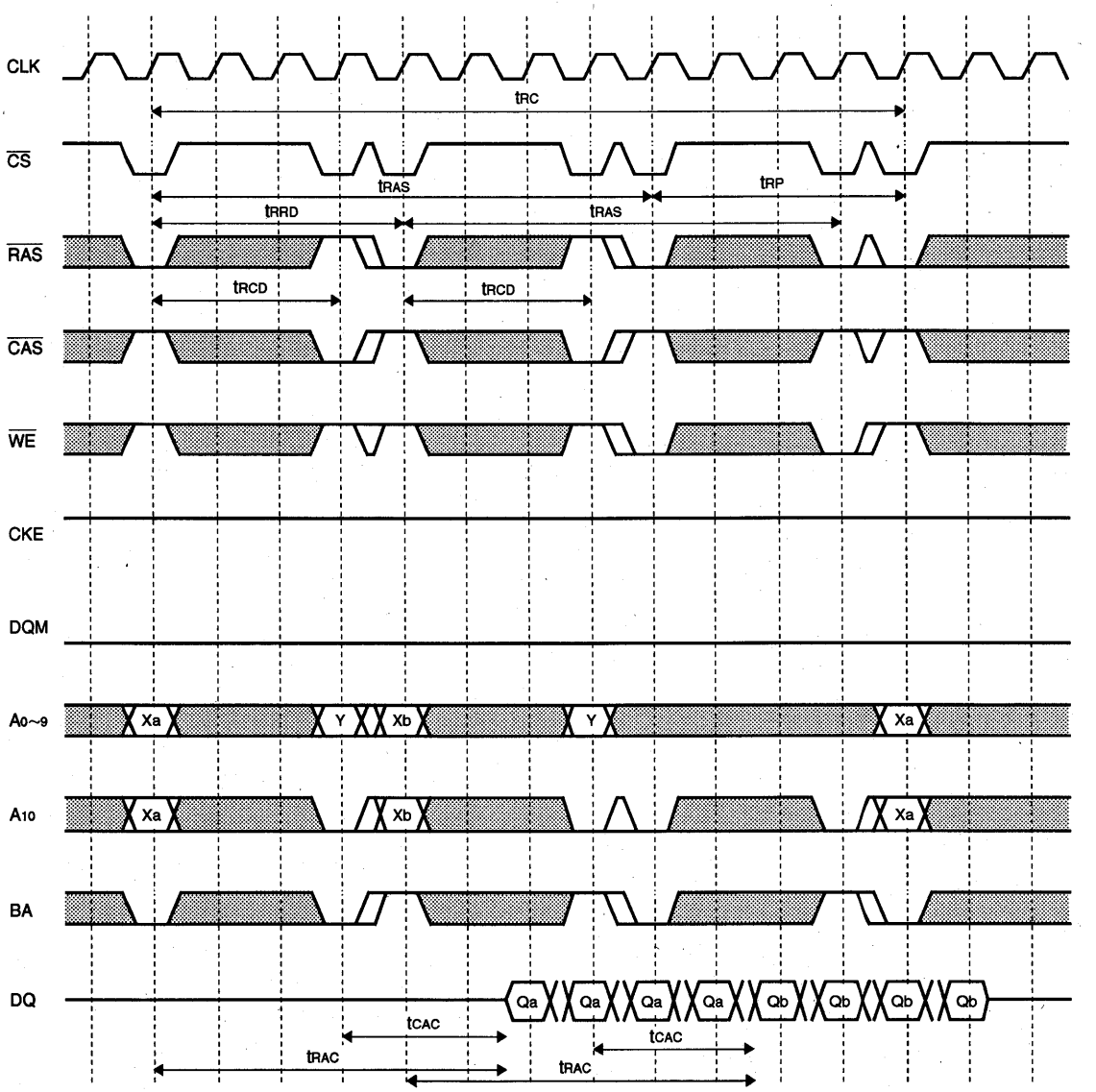
WRITE CYCLE (dual bank) BL=4



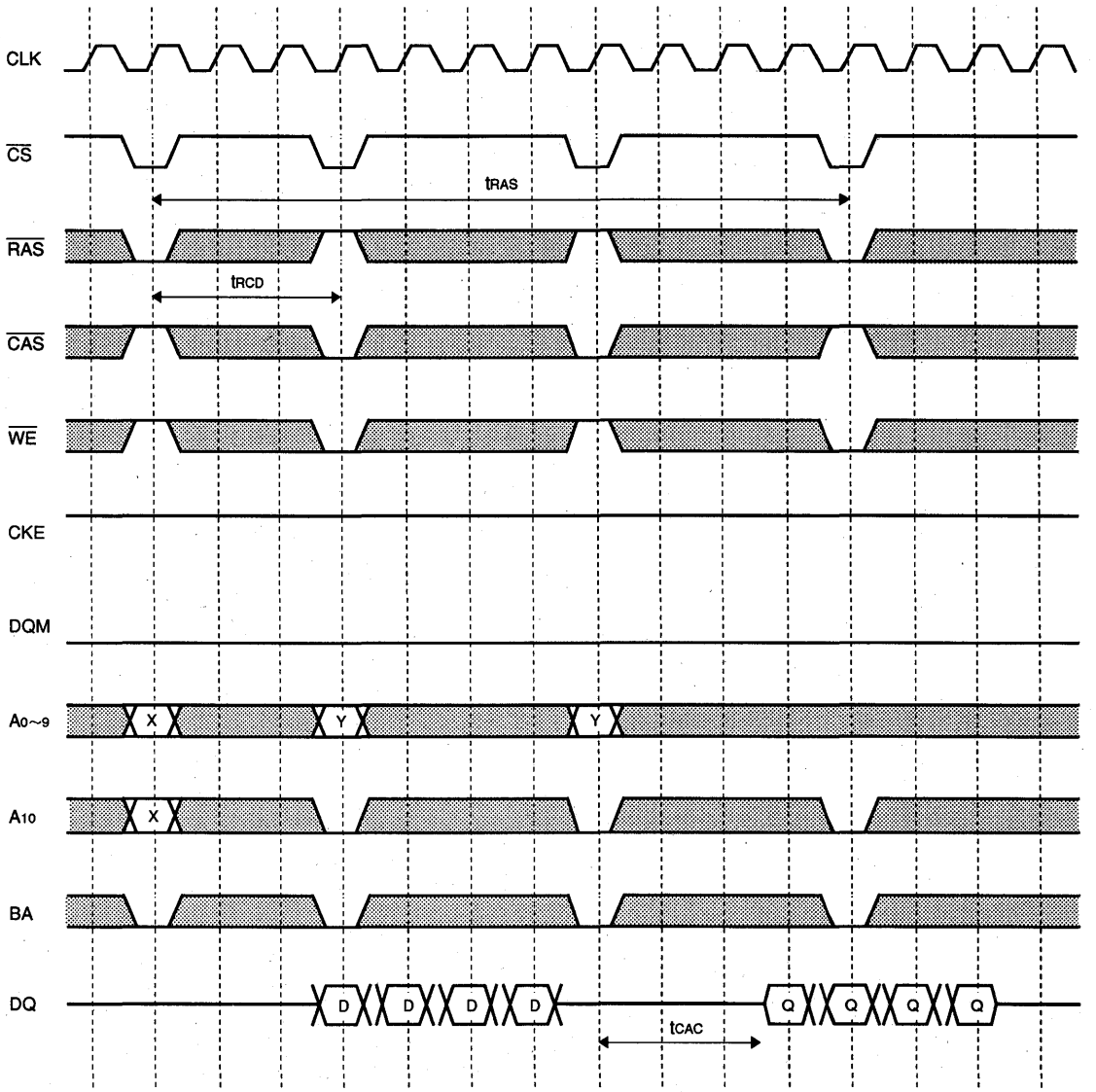
READ CYCLE (single bank) BL=4, CL=3



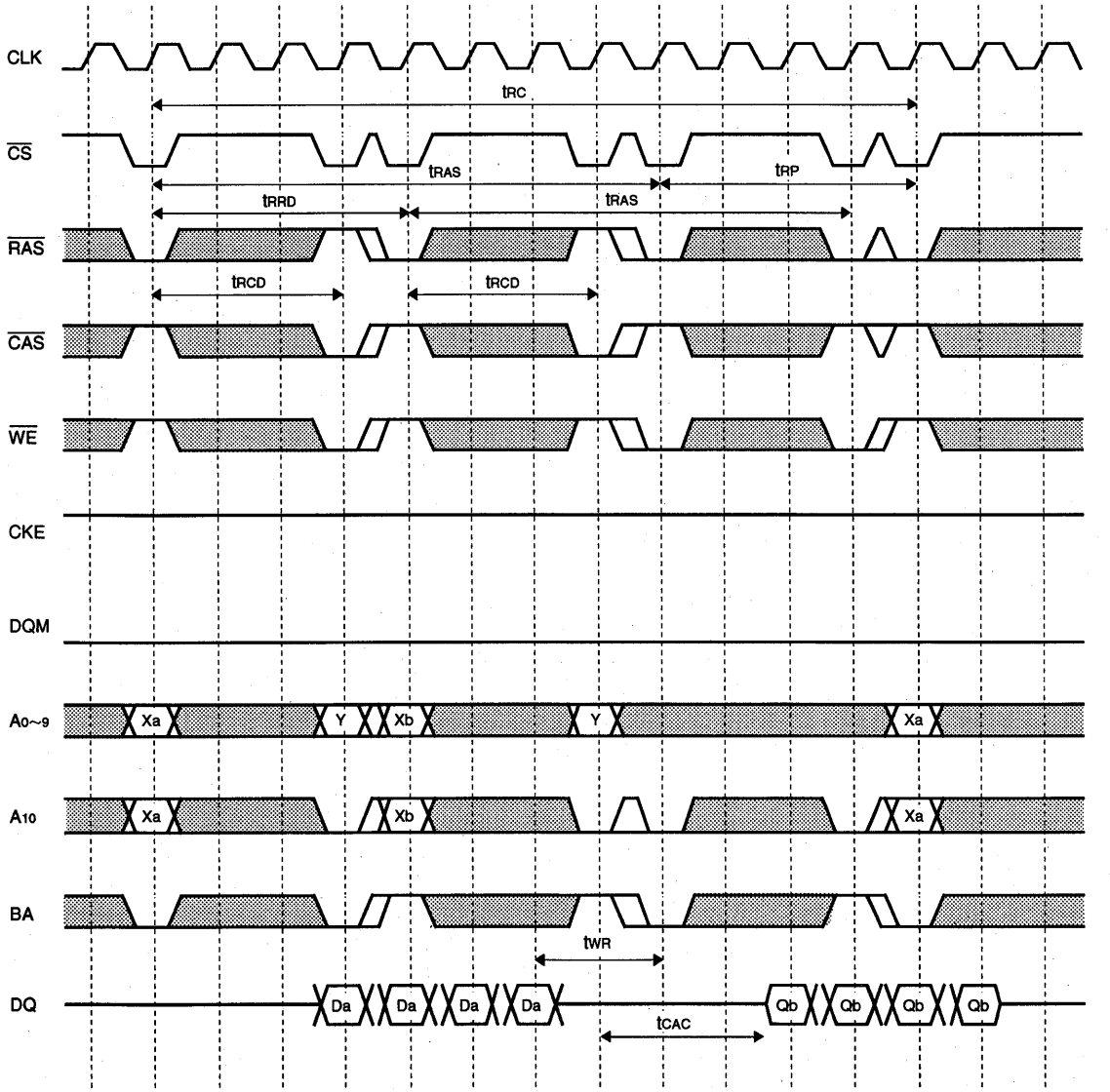
READ CYCLE (dual bank) BL=4, CL=3



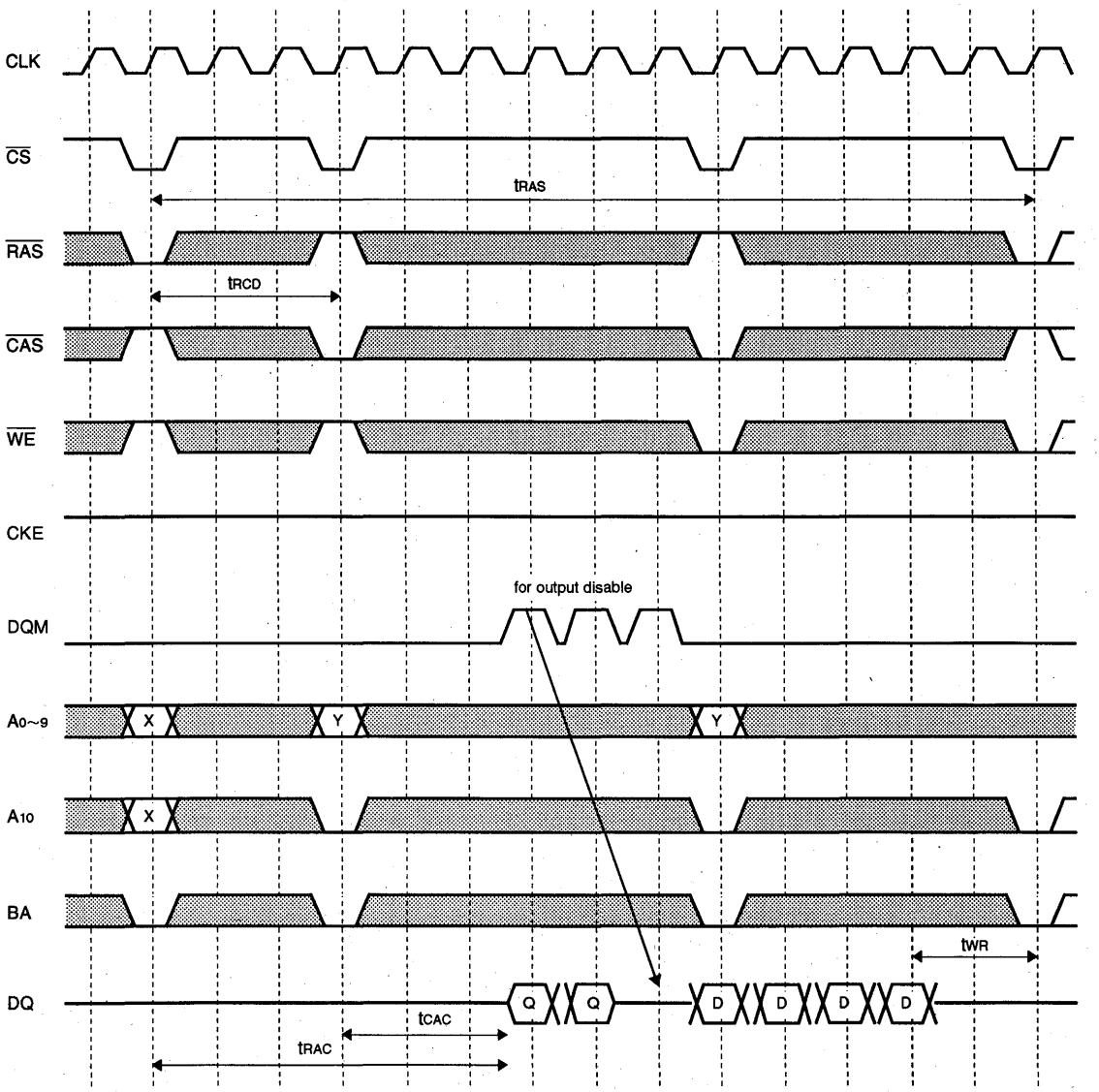
WRITE to READ (single bank) BL=4, CL=3



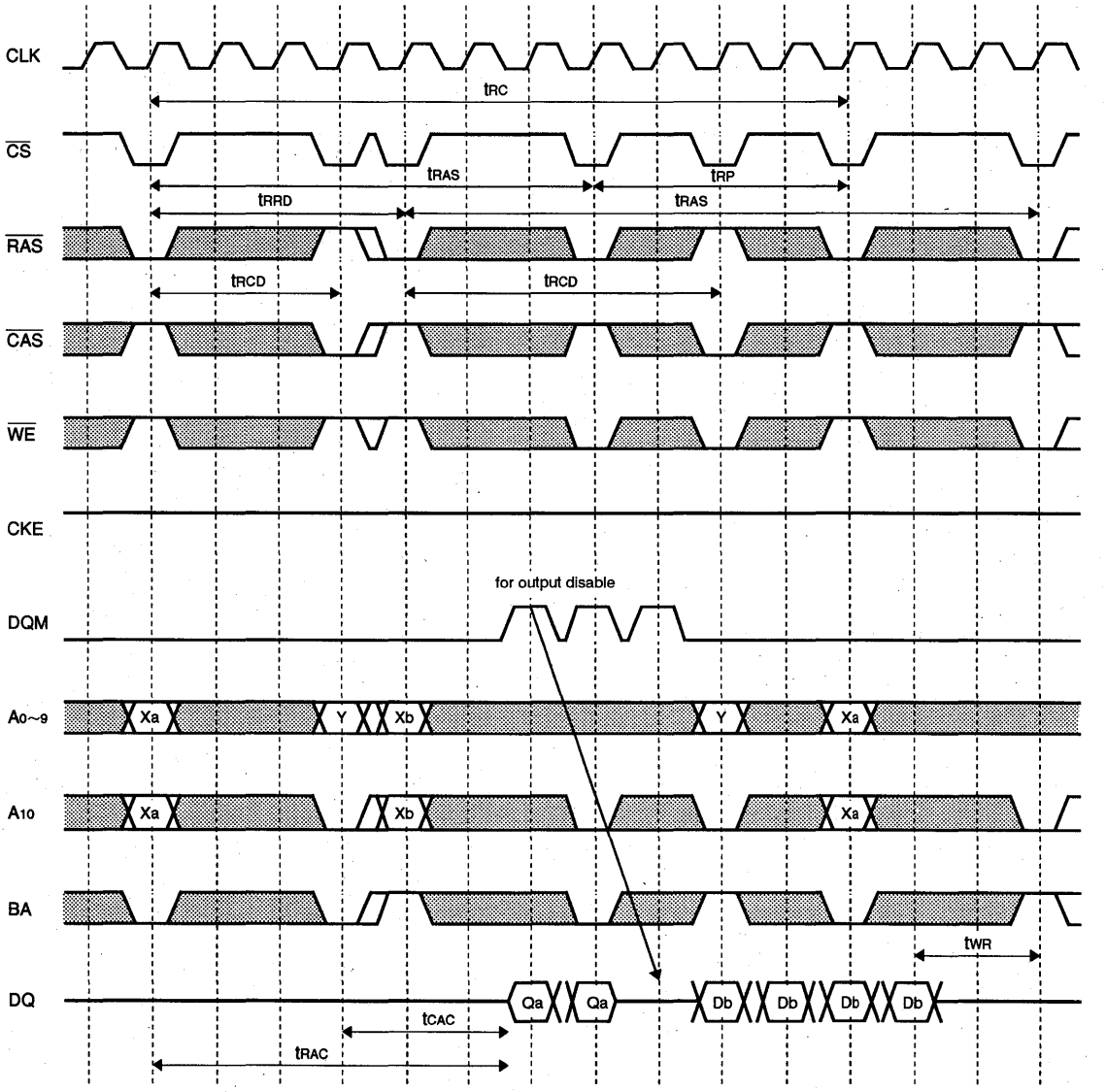
WRITE to READ (dual bank) BL=4, CL=3



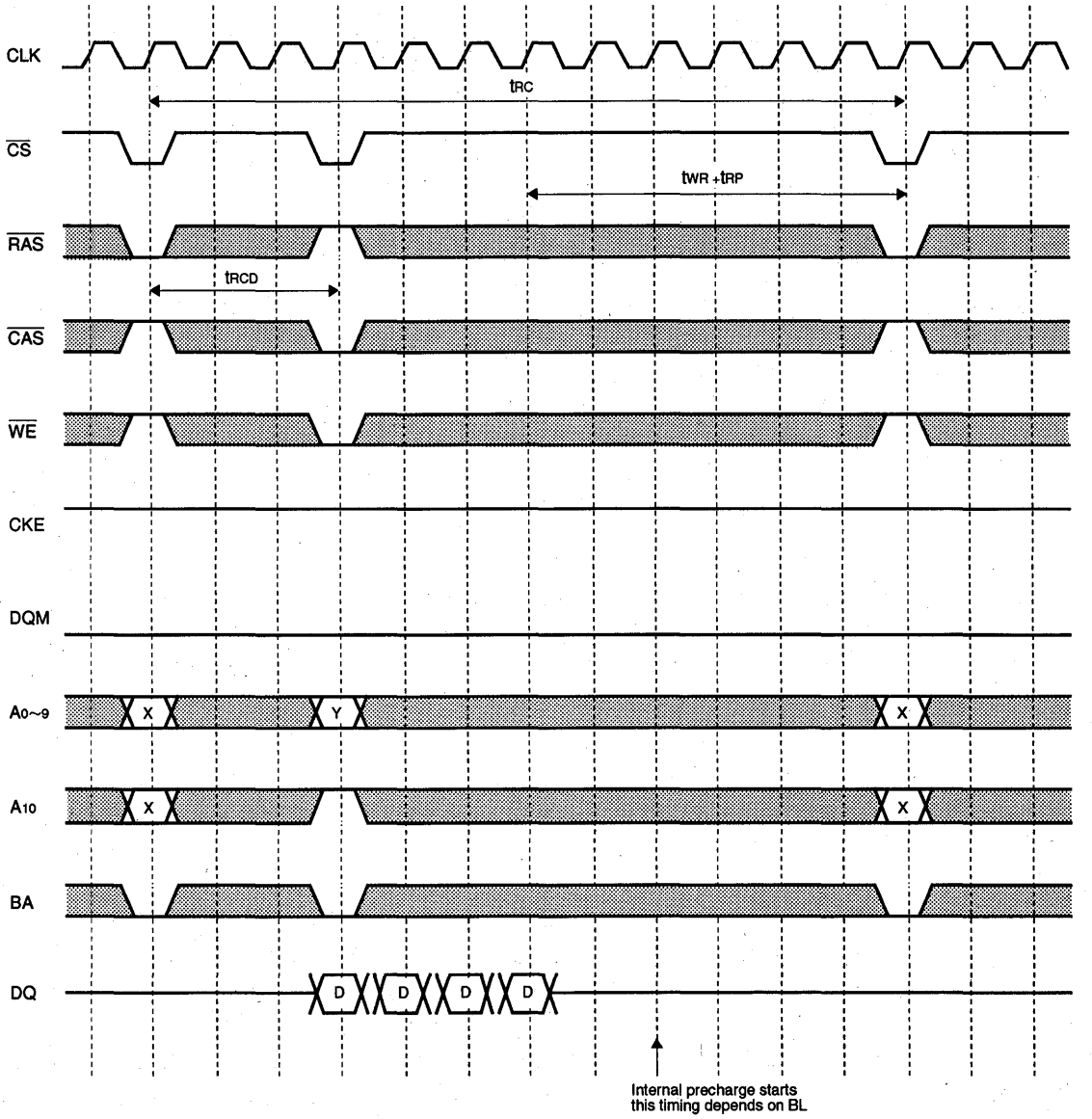
READ to WRITE (single bank) BL=4, CL=3



READ to WRITE (dual bank) BL=4, CL=3

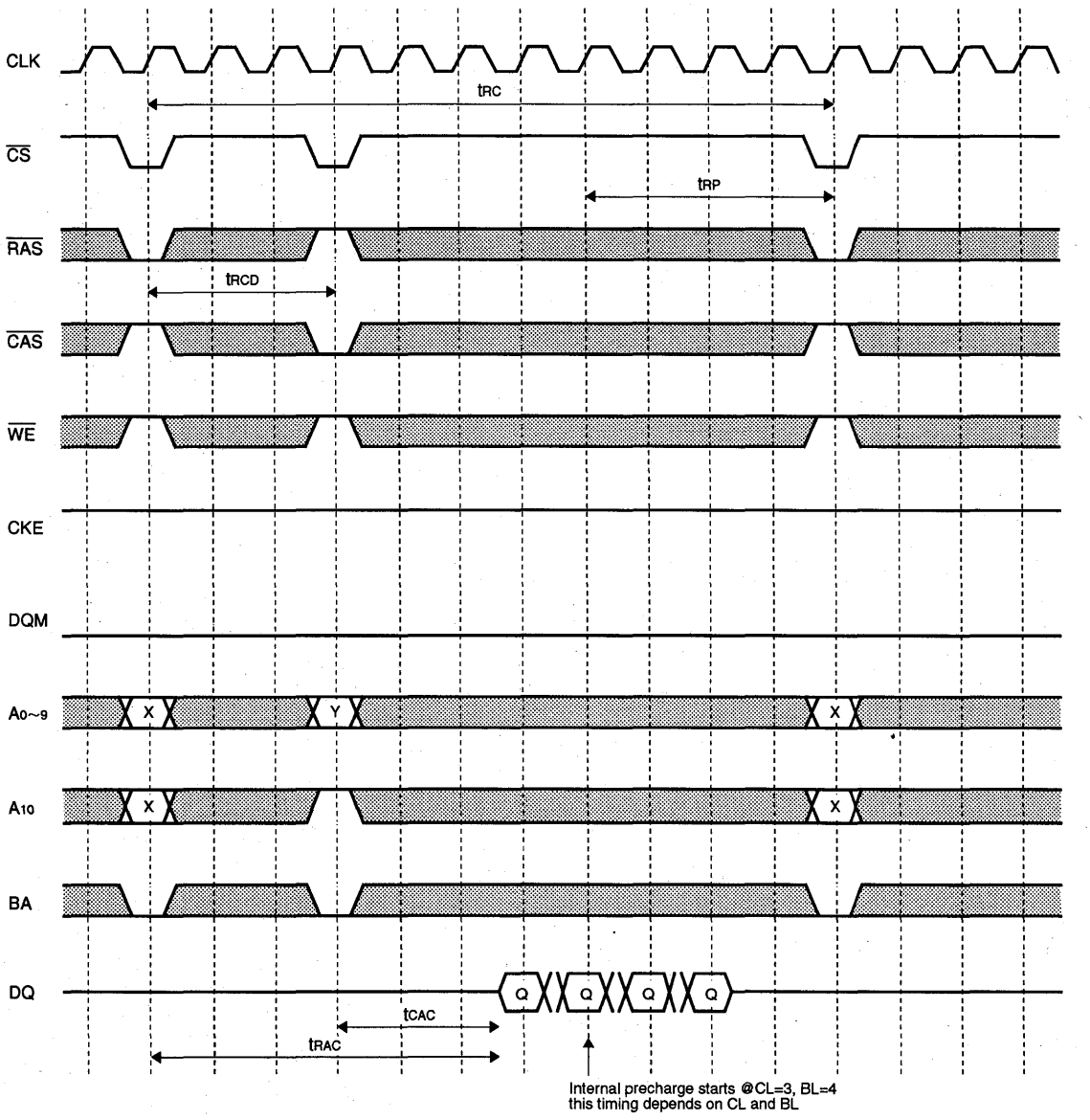


WRITE with AUTO-PRECHARGE BL=4

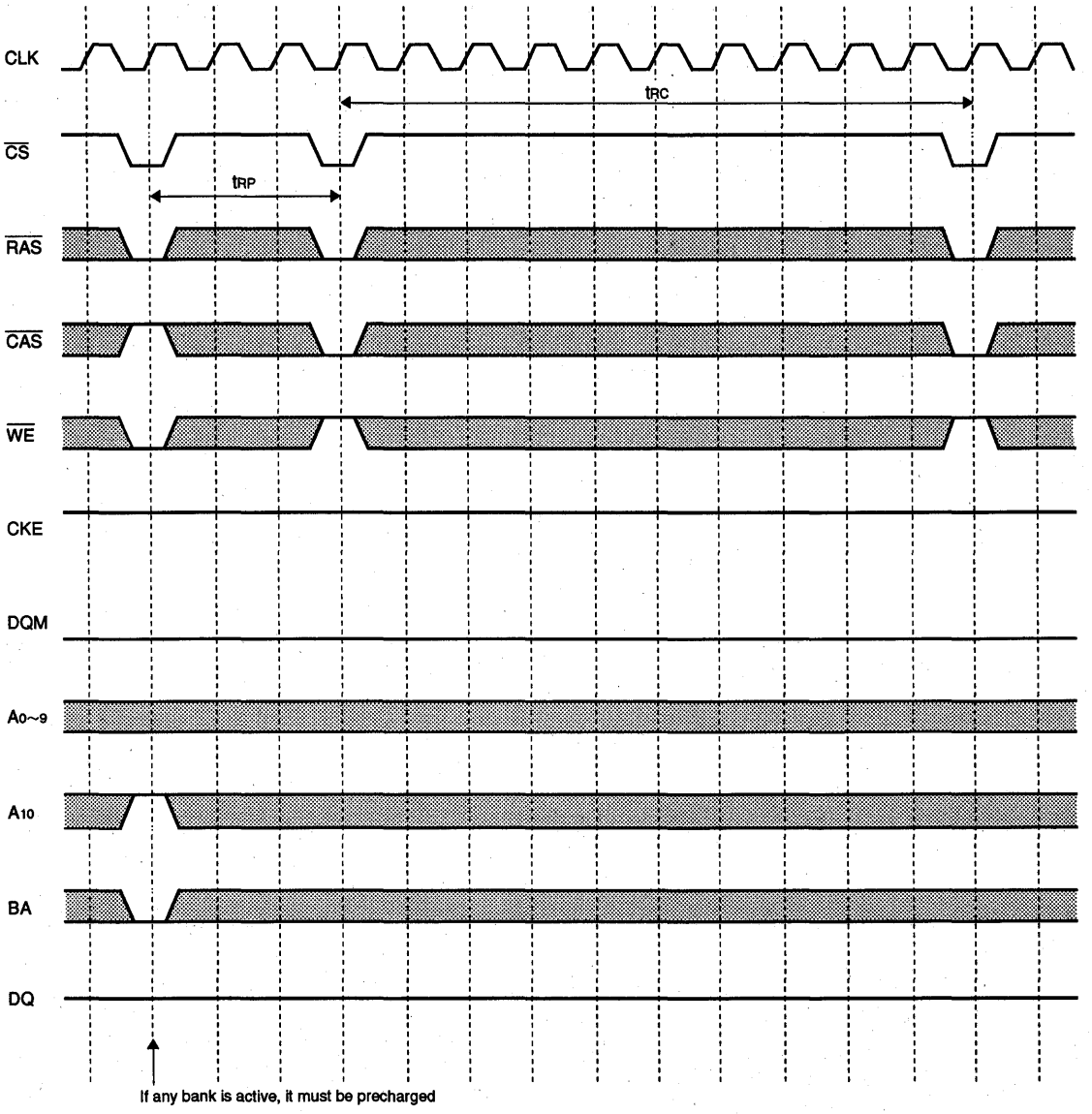


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

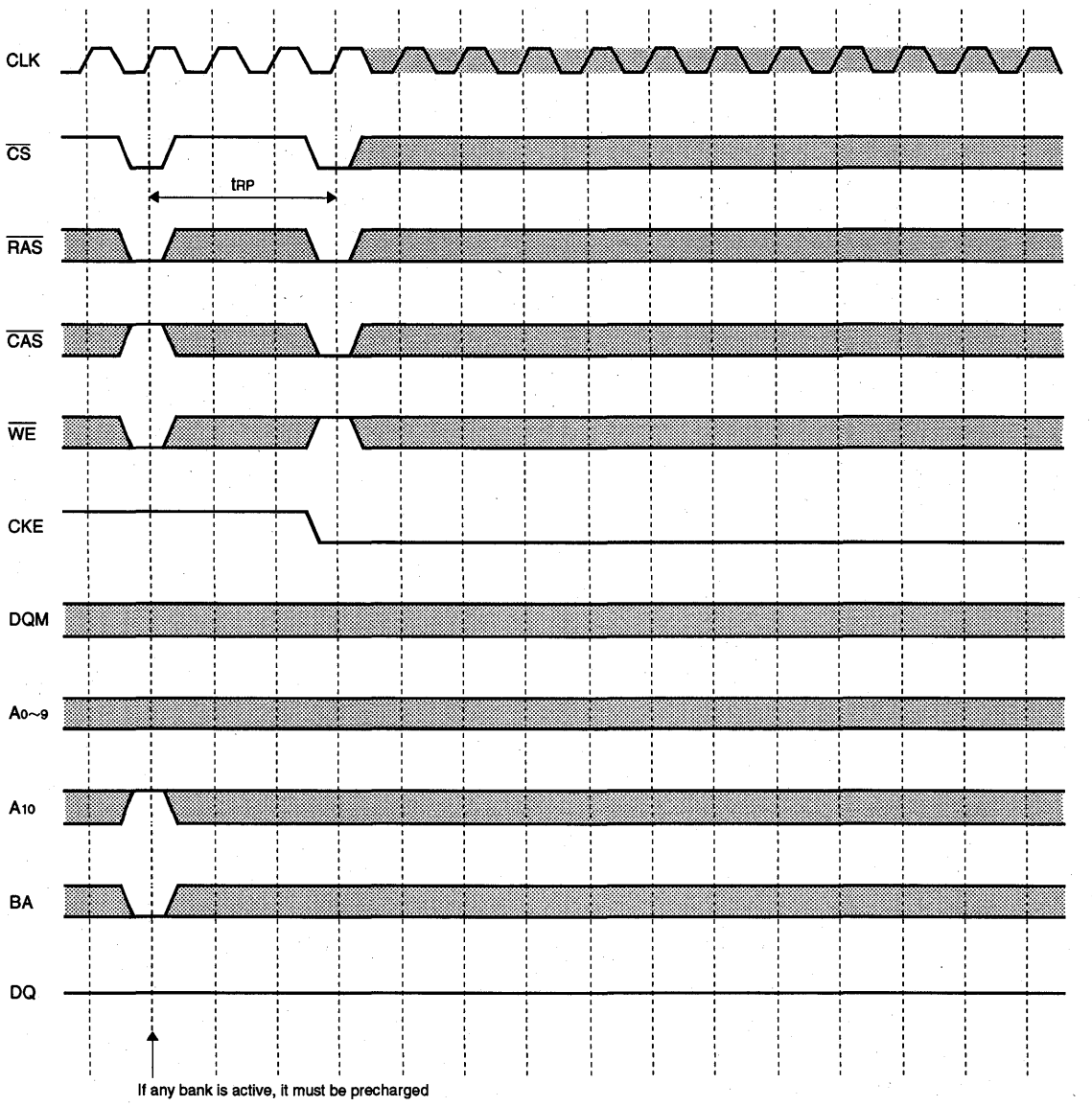
READ with AUTO-PRECHARGE BL=4, CL=3



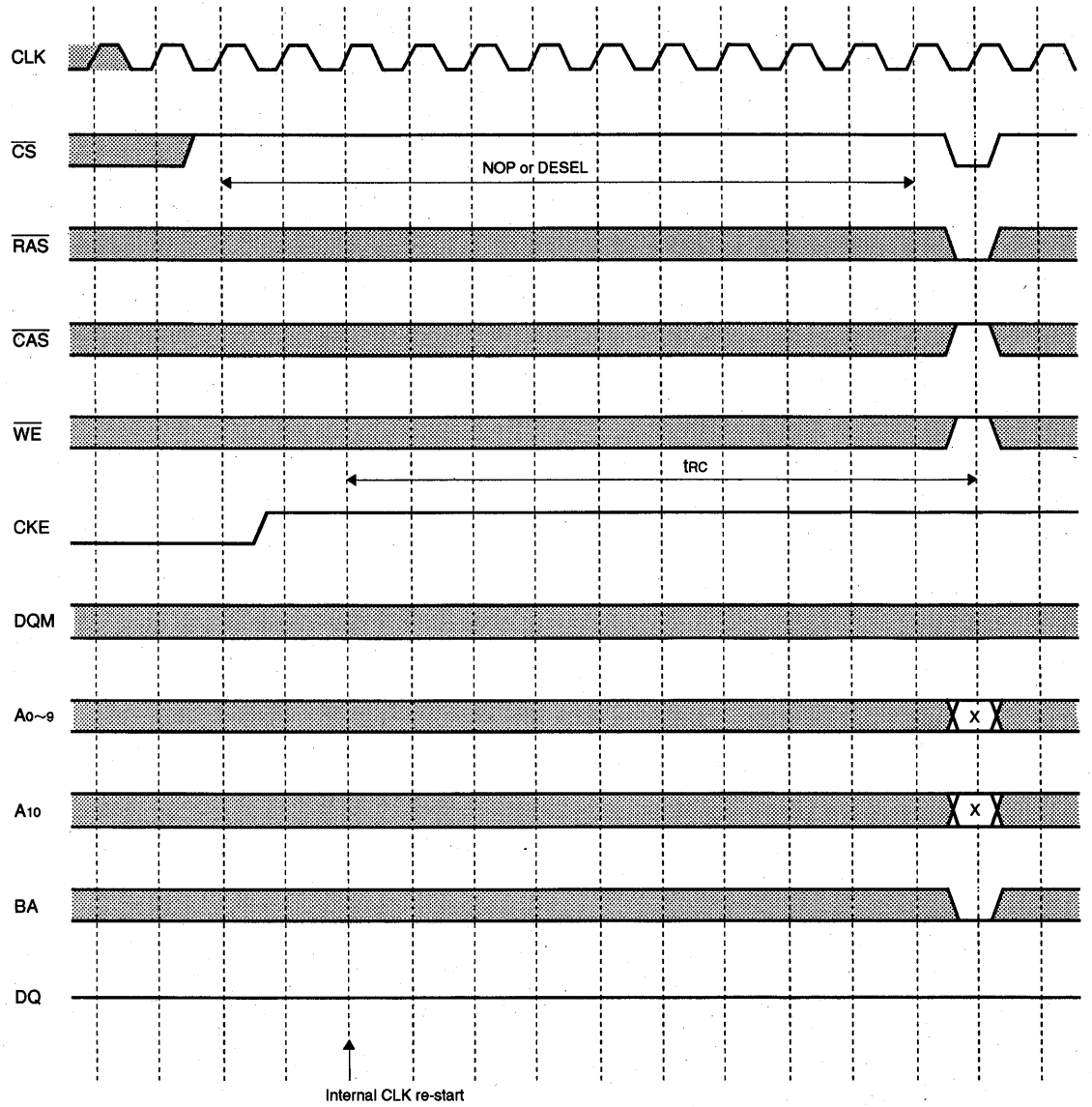
AUTO-REFRESH



SELF-REFRESH ENTRY



SELF-REFRESH EXIT



PRELIMINARY
Notice: This is not a final specification.
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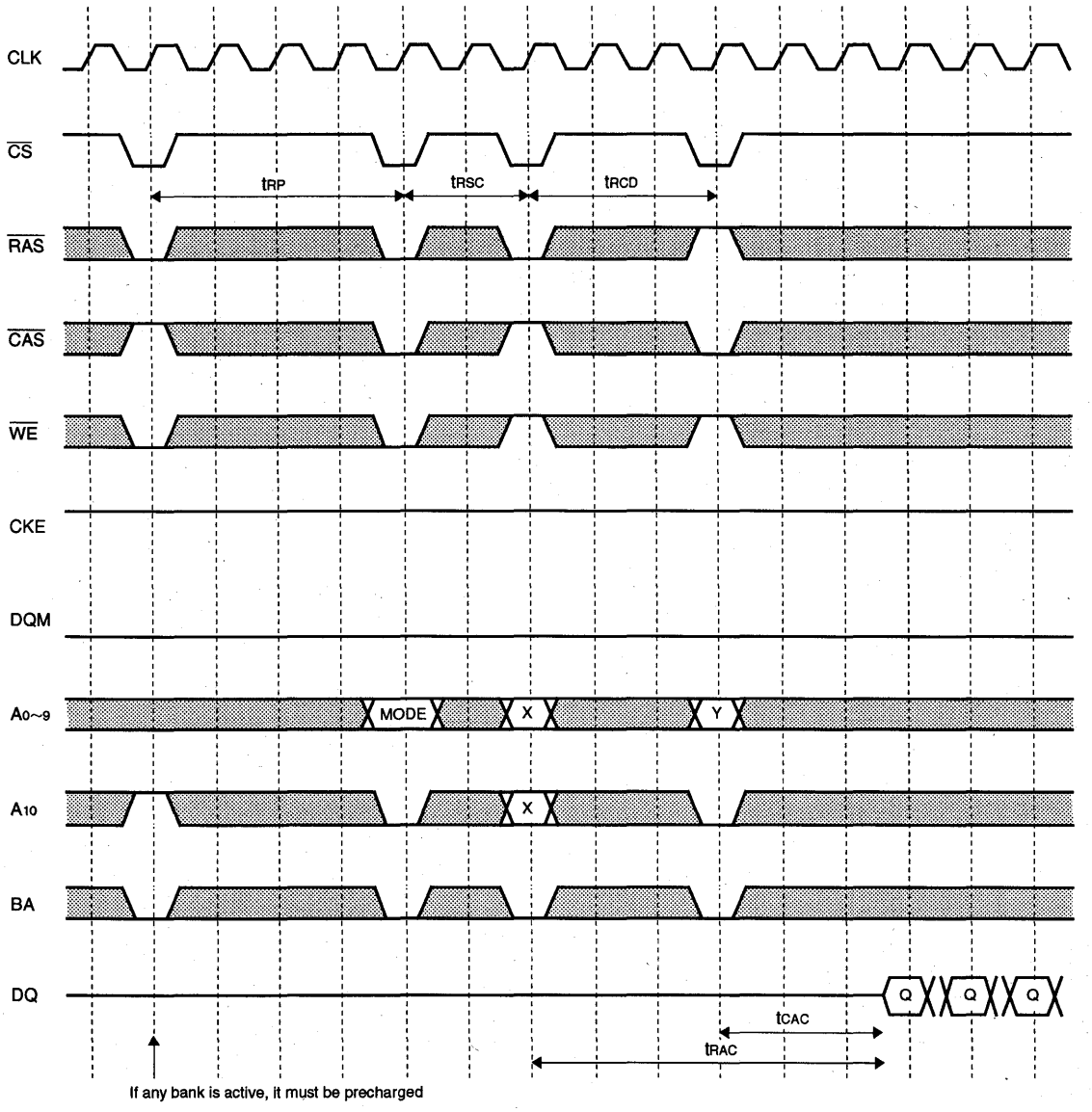
MODE REGISTER SET BL=4, CL=3



PRELIMINARY
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M5M4S16S21CTP-7,-8,-10

16777216-BIT (2-BANK x 2097152-WORD BY 4-BIT) SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The M5M4S16S21CTP is a 2-bank x 2097152-word by 4-bit Synchronous DRAM, with SSTL*1 interface. All inputs and out puts are referenced to the rising edge of CLK. The M5M4S16S21CTP realizes very high speed data transfer using 2-word parallel operation and small signal interface.

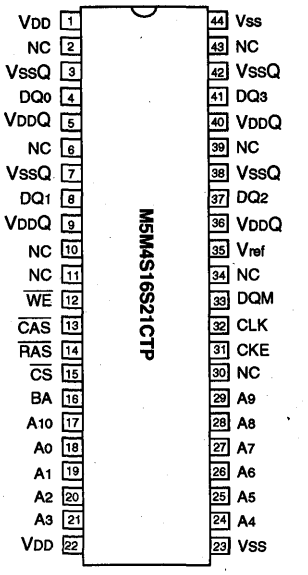
*1 SSTL : Stub Series Terminated Logic

FEATURES

Type name	Max. frequency	CLK access time
M5M4S16S21CTP-7	150MHz	5ns
M5M4S16S21CTP-8	125MHz	6ns
M5M4S16S21CTP-10	100MHz	8ns

- Single 3.3V±0.3V power supply
- Clock frequency 150MHz / 125MHz / 100MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA (Bank Address)
- $\overline{CAS}$ latency-1/2/3/4 (programmable)
- Burst length-1/2/4/8 (programmable)
- Burst type-sequential / interleave (programmable)
- Column access-2N-rule
- Auto precharge / All bank precharge controlled by A_{10}
- Auto refresh and Self refresh
- 4096 refresh cycles / 64ms
- SSTL Interface
- 300-mil, 44-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

PIN CONFIGURATION (TOP VIEW)



Outline 44P3L-B (300mil TSOP)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

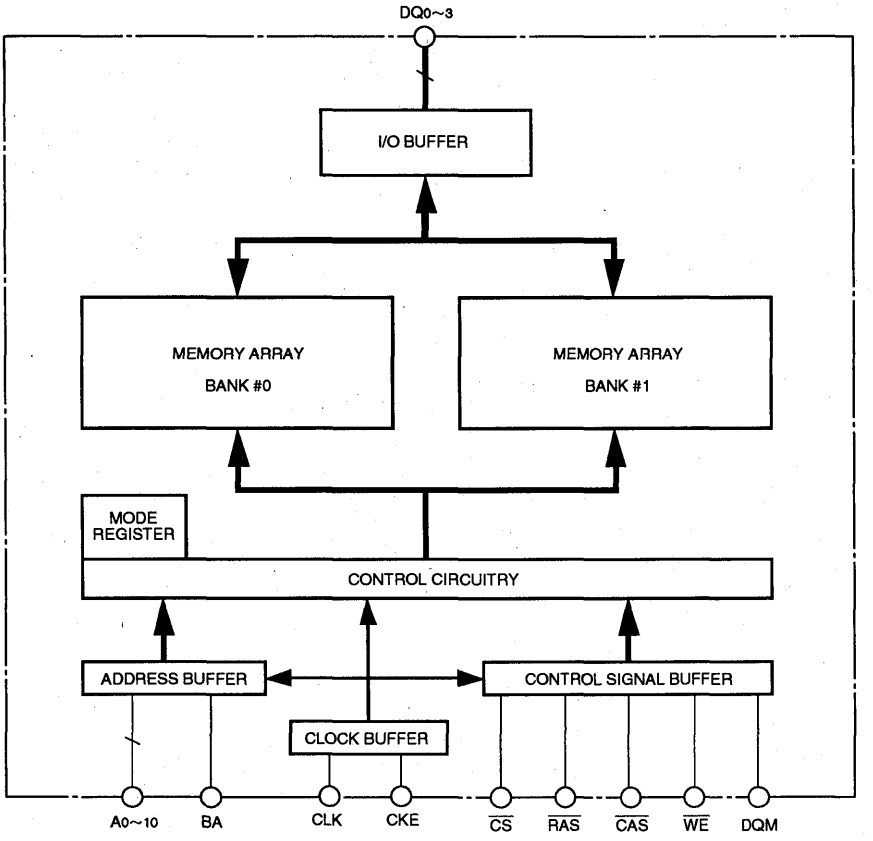
Pin name	Function
CLK	Master clock
CKE	Clock enable
CS	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$DQ_{0\sim3}$	Data I/O
DQM	Output disable/write mask
$A_{0\sim10}$	Address input
BA	Bank address
V_{ref}	Input reference voltage
V_{DD}	Power supply
V_{DDQ}	Power supply for output
Vss	Ground
VssQ	Ground for output

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

16777216-BIT (2-BANK x 2097152-WORD BY 4-BIT) SYNCHRONOUS DYNAMIC RAM

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PIN FUNCTION

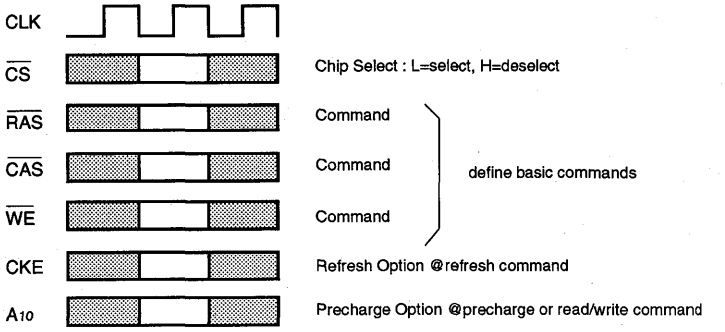
Pin	I/O	Function
CLK	Input	Master clock : All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock enable : CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
$\overline{CS}$	Input	Chip select : When $\overline{CS}$ is high, any command means No operation.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Conbination of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ defines basic commands.
$A_{0\sim10}$	Input	$A_{0\sim10}$ specify the Row / Column address in conjunction with BA. The Row address is specified by $A_{0\sim10}$. The Column address is specified by $A_{0\sim9}$ ($\times4$), $A_{0\sim8}$ ($\times8$). A_{10} is also used to indicate precharge option. When A_{10} is high at a read / write command, an auto precharge is performed. When A_{10} is high at a precharge command, both banks are precharged.
BA	Input	Bank address: BA is not simply A_{11}. BA specifies the bank to which a command is applied. BA must be set with ACT, PRE, READ, WRITE commands.
$DQ_{0\sim3}$	Input / output	Data in and Data out are referenced to the rising edge of CLK.
DQM	Input	Din mask / output disable : When DQM is high in burst write, Din for the current cycle is masked. When DQM is high in burst read, Dout is disabled at the next but one cycle.
V_{DD}, V_{SS}	Power supply	Power supply for the memory array and peripheral circuitry.
V_{DDQ}, V_{SSQ}	Power supply	V_{DDQ} and V_{SSQ} are supplied to the output buffers only.
V_{ref}	Input	Reference voltage for all inputs. V_{ref} should be typically $0.45\times V_{DDQ}$.

BASIC FUNCTIONS

The M5M4S16S21CTP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at CLK rising edge. In addition to 3 signals, $\overline{CS}$,CKE and A_{10} are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [$\overline{RAS}$=L, $\overline{CAS}$=$\overline{WE}$=H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [$\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=H]

READ command starts burst read from the active bank indicated by BA. First output data appears after $\overline{CAS}$ latency. When A_{10}=H at this command, the bank is deactivated after the burst read (auto-precharge, **READ A**).

Write (WRITE) [$\overline{RAS}$=H, $\overline{CAS}$=$\overline{WE}$=L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A_{10}=H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITE A**).

Precharge (PRE) [$\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A_{10} =H at this command, both banks are deactivated (precharge all, **PRE A**).

Auto-Refresh (REFA) [$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=CKE=H]

REF A command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

Command	Mnemonic	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10}	$A_{0\sim9}$
Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	V	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number
Note 1. $A_7\sim A_9$ =0, $A_0\sim A_6$ =Mode Address

PRELIMINARY
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FUNCTION TRUTH TABLE

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL∗2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL∗2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A_{10}	PRE / PREA	NOP∗4
	L	L	L	H	X	REFA	Auto-Refresh∗5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set∗5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A_{10}	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL∗2
	L	L	H	L	BA, A_{10}	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A_{10}	READ / READA	Terminate Burst, Latch CA, Bigin New Read, Determine Auto-Precharge∗3
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge∗3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL∗2
	L	L	H	L	BA, A_{10}	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A_{10}	READ / READA	Terminate Burst, Latch CA, Bigin Read, Determine Auto-Precharge∗3
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge∗3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL∗2
	L	L	H	L	BA, A_{10}	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A_{10}	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A_{10}	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A_{10}	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	NOP*4 (Idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after t_{RCD})
	L	H	H	H	X	NOP	NOP (Row Active after t_{RCD})
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

PRELIMINARY
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Some parametric limits are subject to change.

FUNCTION TRUTH TABLE (Cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after t_{RC})
	L	H	H	H	X	NOP	NOP (Idle after t_{RC})
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t_{RSC})
	L	H	H	H	X	NOP	NOP (Idle after t_{RSC})
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A_{10}	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A_{10}	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS : H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No OPeration

Note 1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n-rule", bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

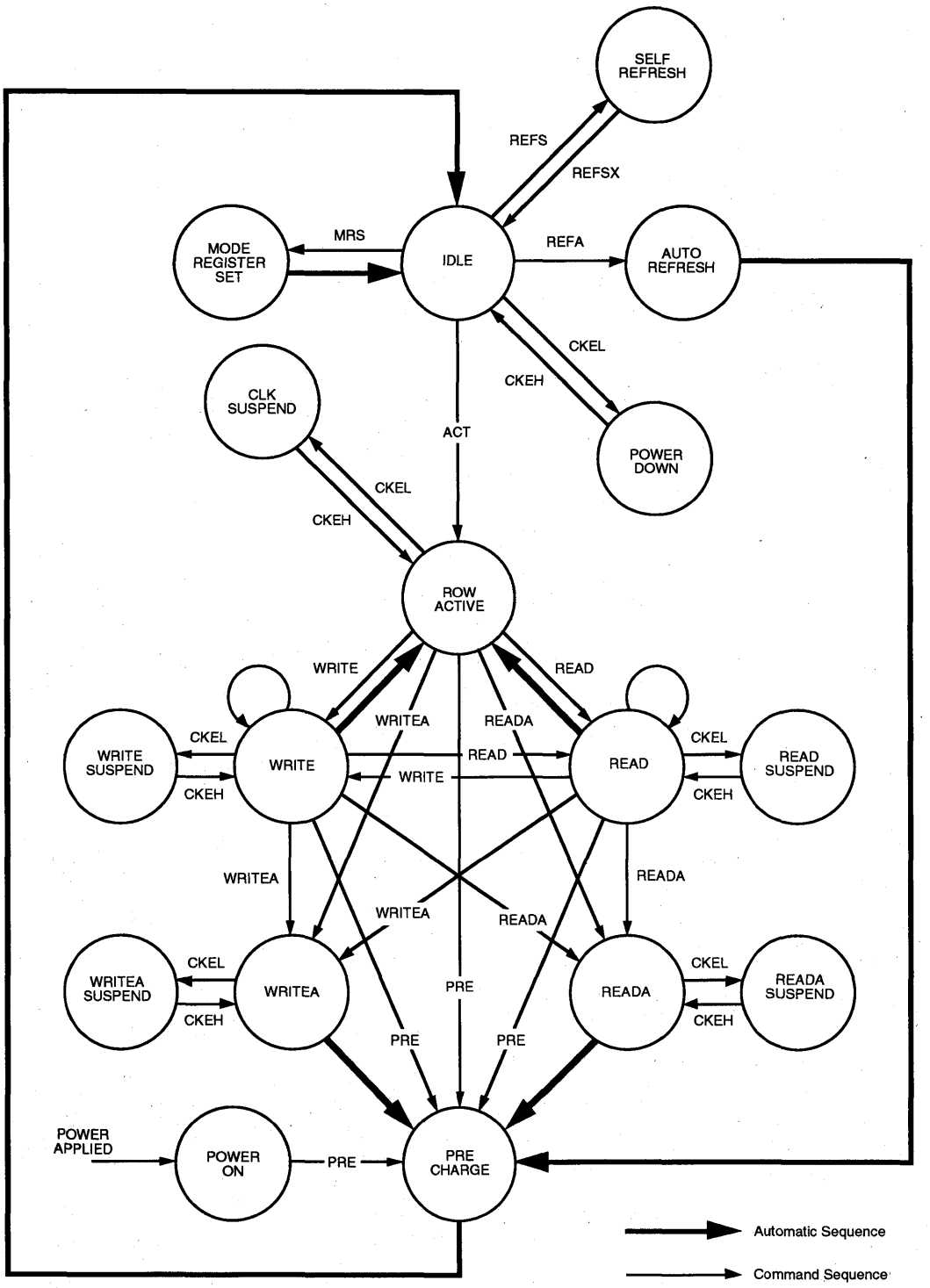
FUNCTION TRUTH TABLE for CKE

Current state	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS : H=High Level, L=Low Level, X=Don't Care

Note 1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

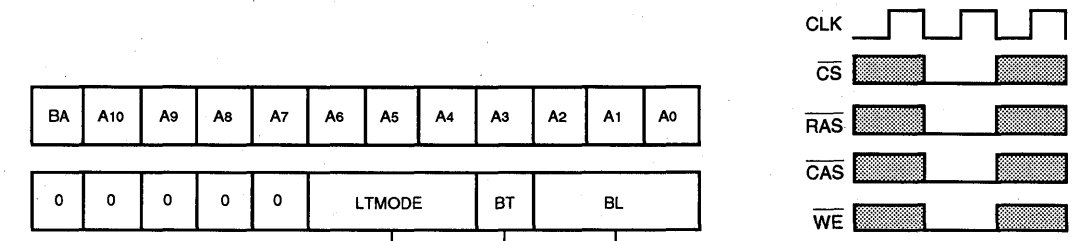
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500μs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after t_{RP}), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and $\overline{CAS}$ Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After t_{RSC} from a MRS command, the SDRAM is ready for new command.

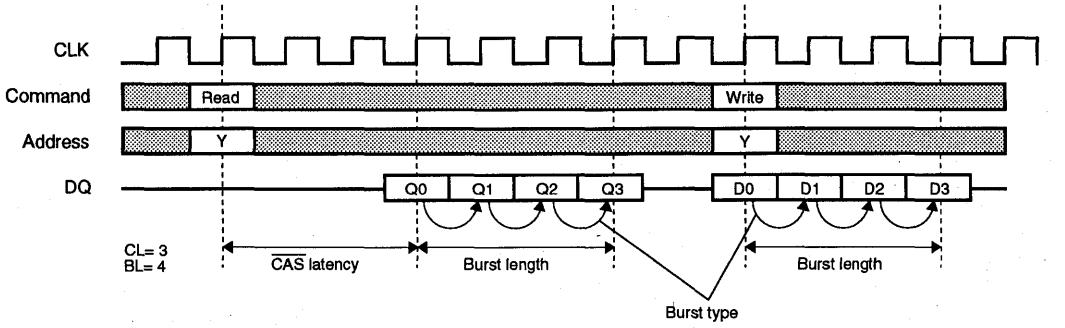


	CL	CAS LATENCY
LATENCY MODE	000	R
	001	1
	010	2
	011	3
	100	4
	101	R
	110	R
	111	R

R : Reserved for Future Use

	BL	BT= 0	BT= 1
BURST LENGTH	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	R	R

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED



Initial address			BL	Column addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATIONAL DESCRIPTION

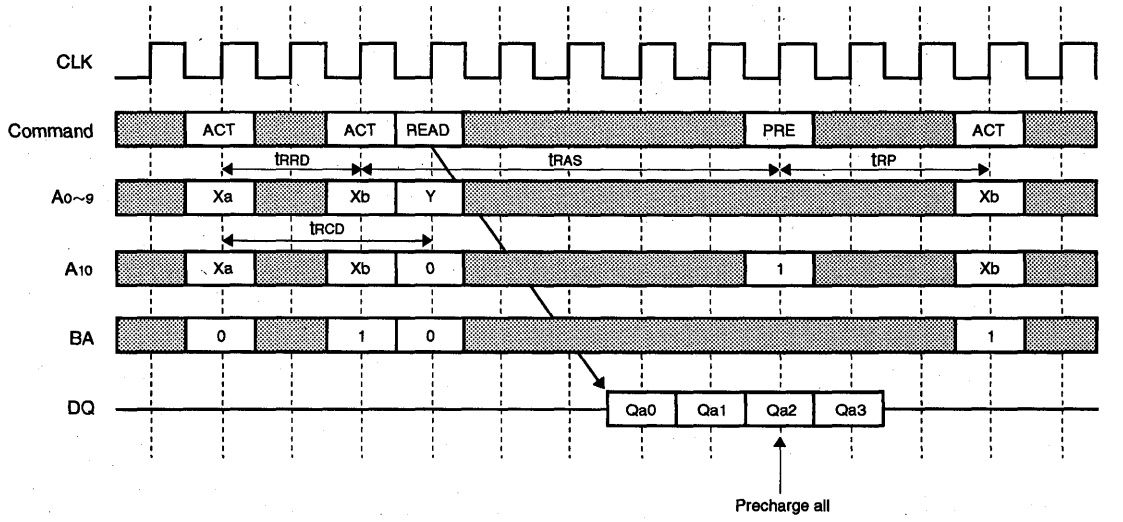
BANK ACTIVATE

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address (BA). A row is indicated by the row address $A_{10\sim0}$. The minimum activation interval between one bank and the other bank is t_{RRD}.

PRECHARGE

The PRE command deactivates the bank indicated by BA. When both banks are active, the precharge all command (PREA, PRE+ A_{10}=H) is available to deactivate them at the same time. After t_{RP} from the precharge, an ACT command can be issued.

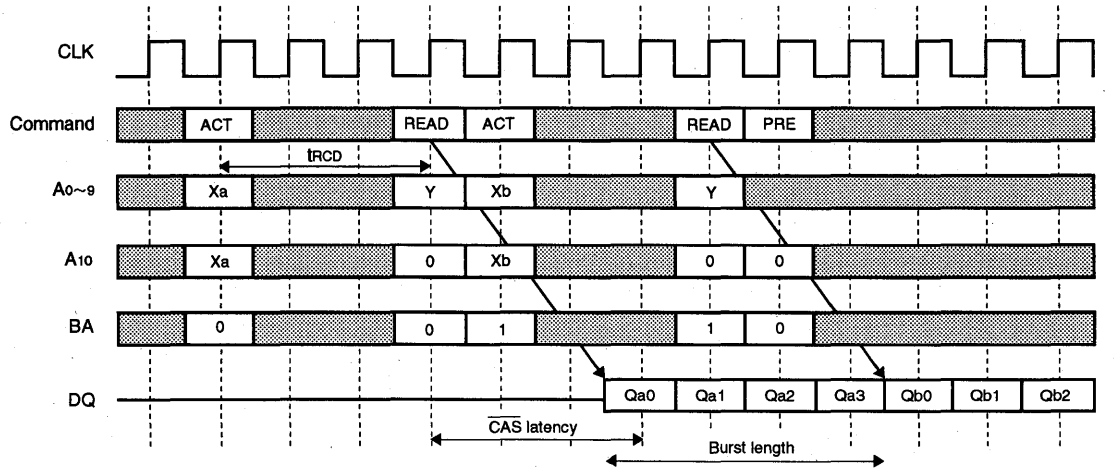
Bank Activation and Precharge All (BL=4, CL=3)



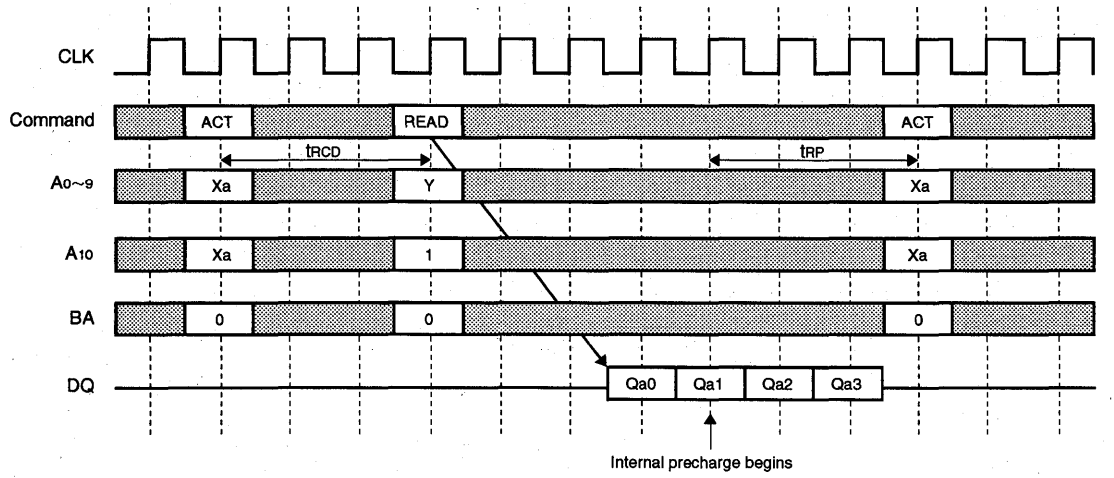
READ

After t_{RCD} from the bank activation, a READ command can be issued. 1st output data is available after the $\overline{CAS}$ Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by $A_{8\sim0}$ (×8) / $A_{9\sim0}$ (×4), and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (t_{RP}) can be hidden behind continuous output data (in case of BL=8) by interleaving the dual banks. When A_{10} is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge start timing depends on $\overline{CAS}$ Latency. The next ACT command can be issued after t_{RP} from the internal precharge timing.

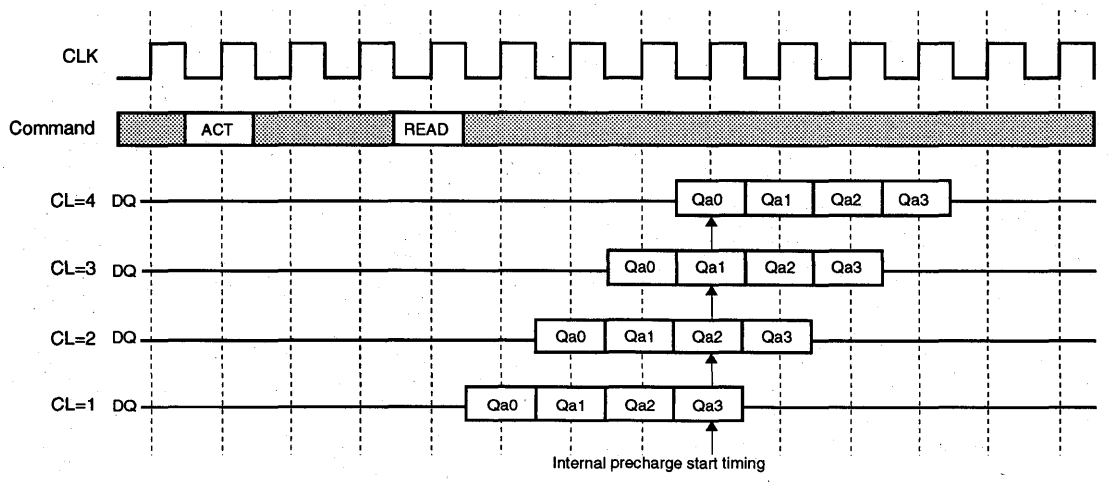
Dual Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



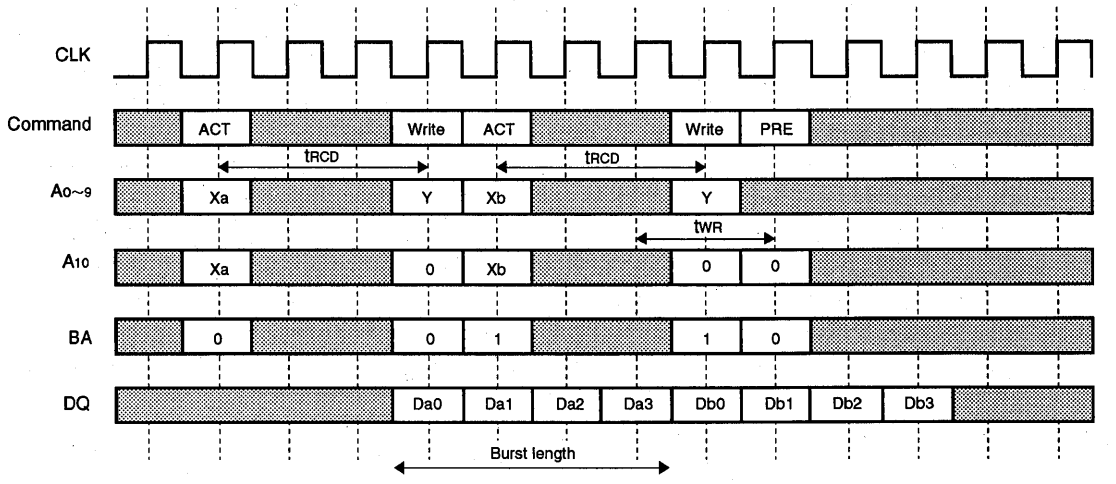
READ Auto-Precharge Timing (BL=4)



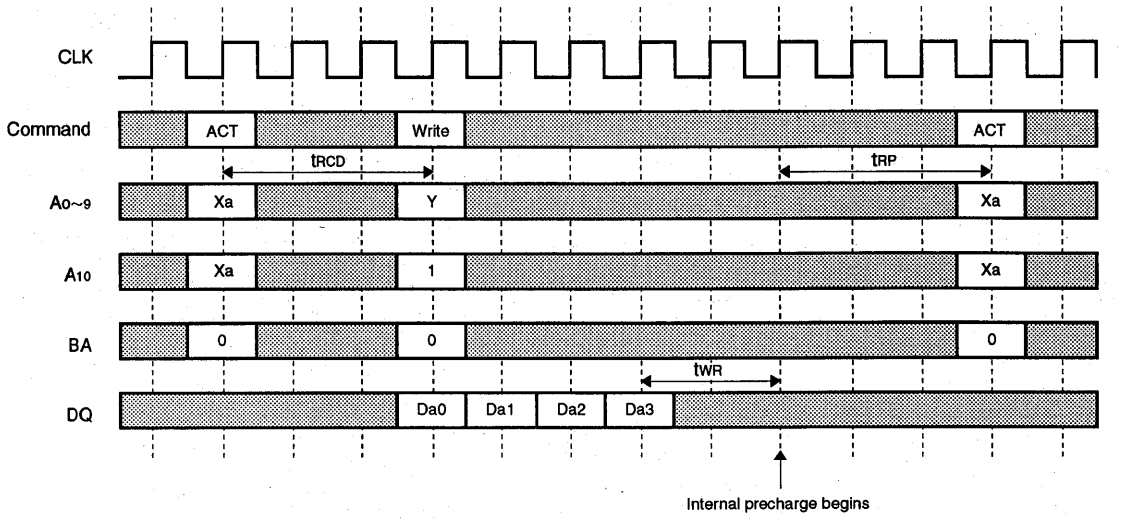
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL-1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A8~0 (×8) / A9~0 (×4), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data (in case of BL=8) by interleaving the dual banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP from the internal precharge timing.

Dual Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

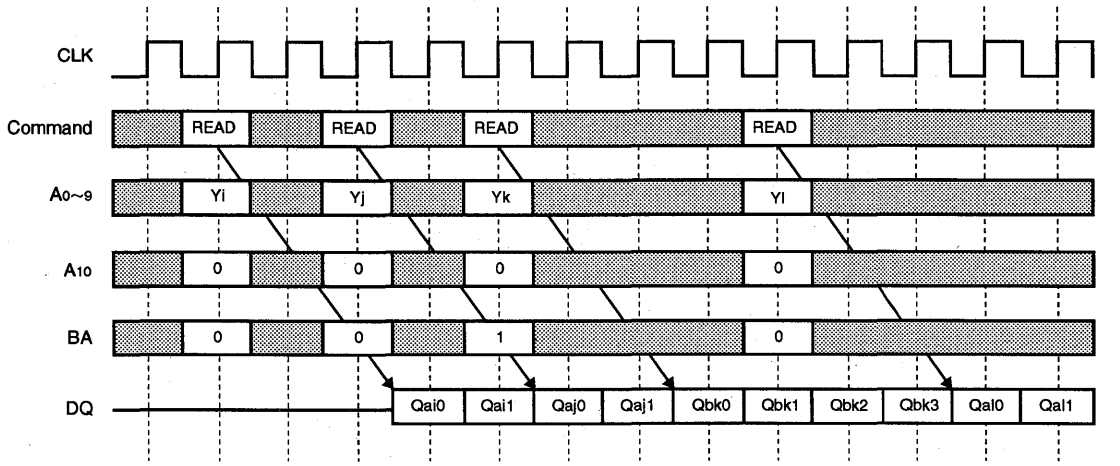


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of the same or the other bank. As M5M4S16S31CTP/ M5M4S16S21CTP adopt 2-words parallel transfer architecture to realize very high speed data rate, JEDEC 2n-rule is required, where 2, 4 or 6 read to read interval is allowed in case of BL=8.

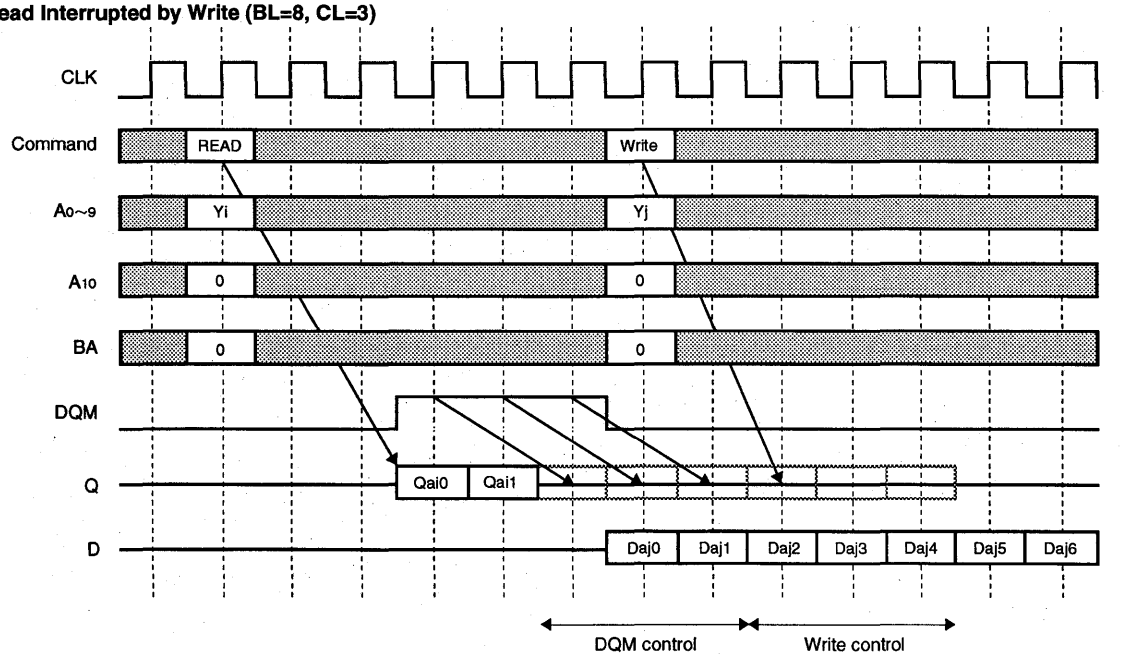
Read Interrupted by Read (BL=8, CL=3)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of the same or the other bank. JEDEC 2n-rule also must be kept here. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 2 cycles after WRITE assertion.

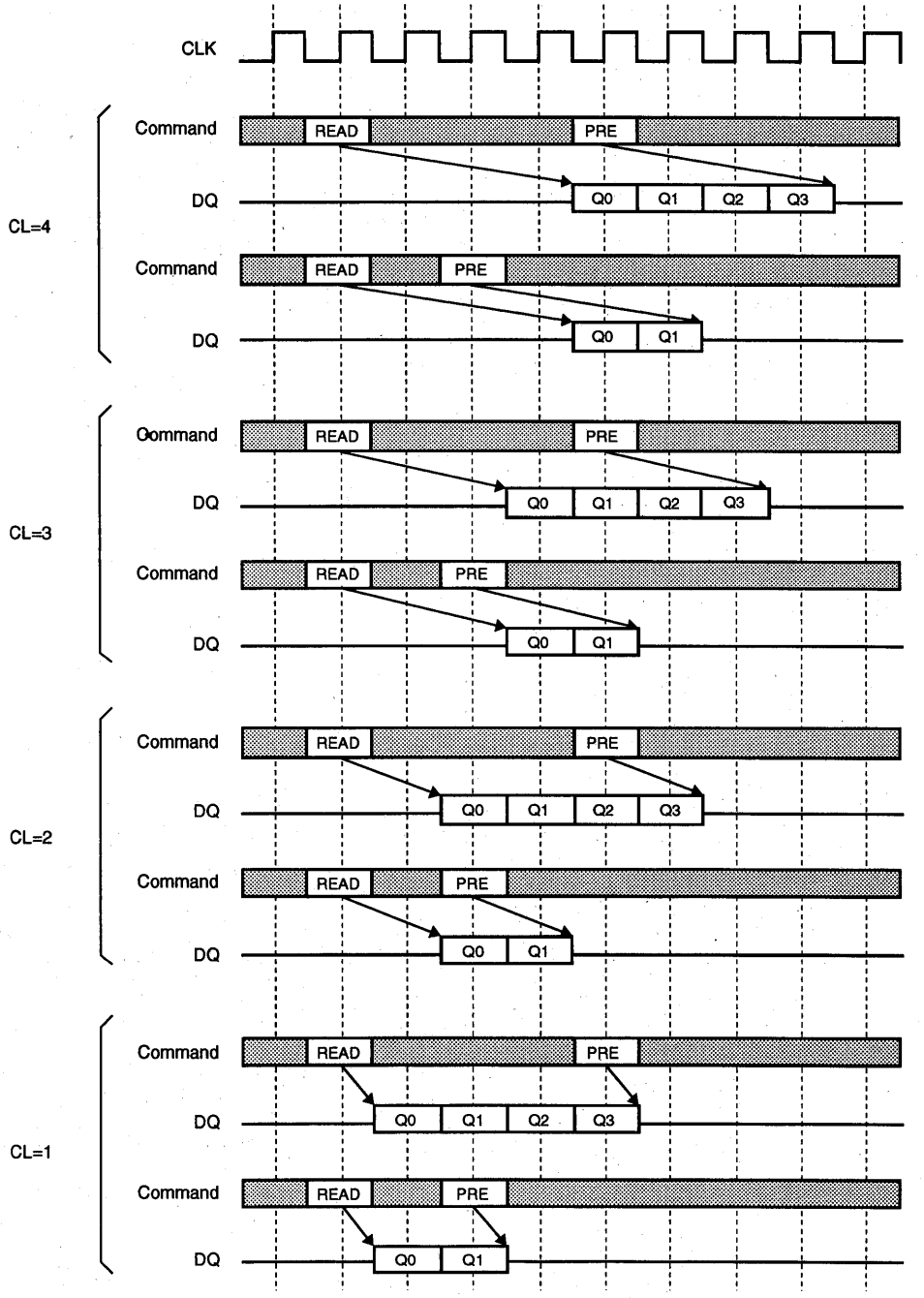
Read Interrupted by Write (BL=8, CL=3)



〔Read Interrupted by Precharge〕

Burst read operation can be interrupted by precharge of the same bank. JEDEC 2n-rule also must be kept here. A PRE command disables the data output, depending on the $\overline{CAS}$ Latency. The figure below shows when the dataout is terminated.

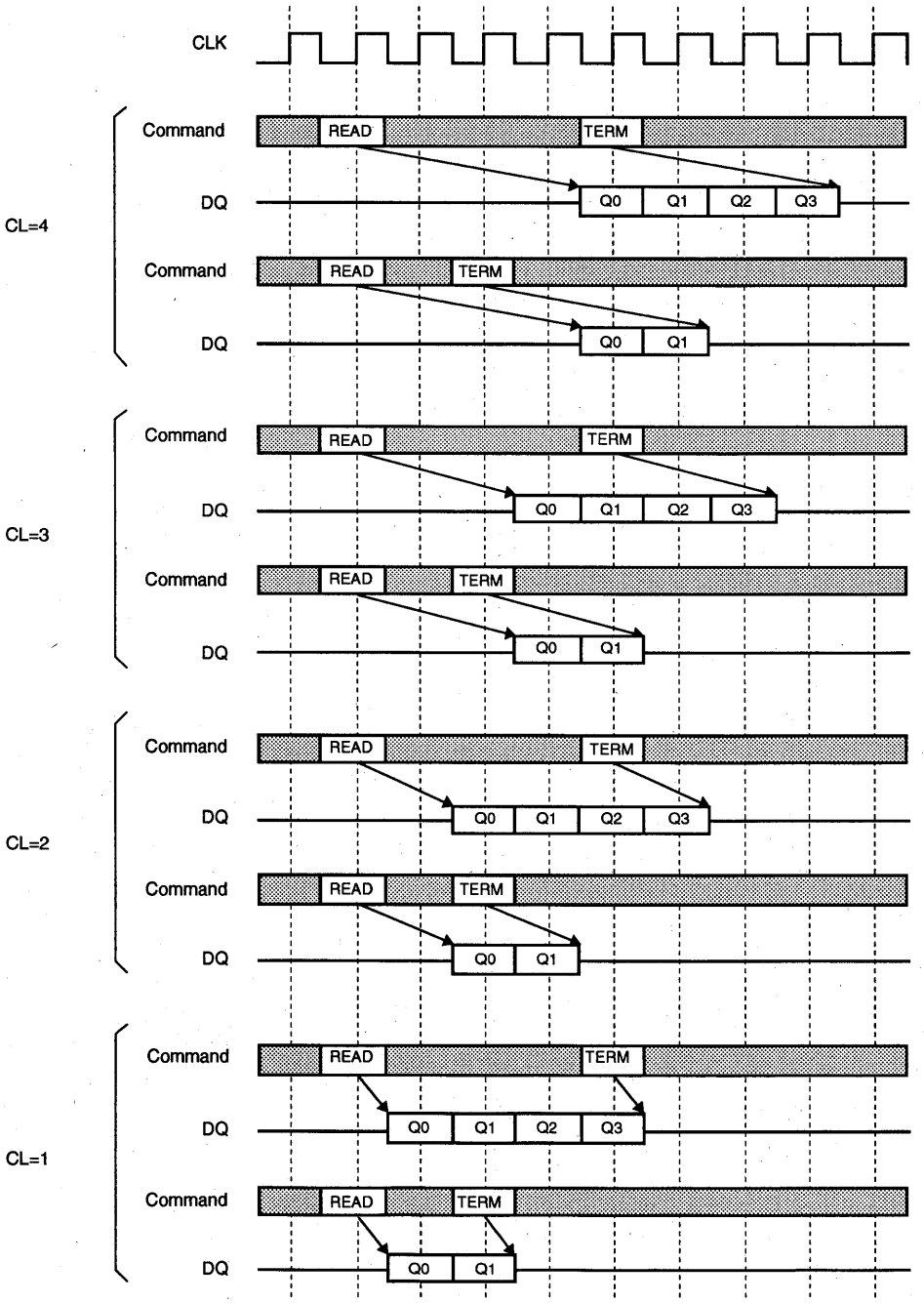
Read Interrupted by Precharge (BL=4)



〔Read Interrupted by Burst Terminate〕

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. JEDEC 2n-rule also must be kept here. The figure below shows when the dataout is terminated.

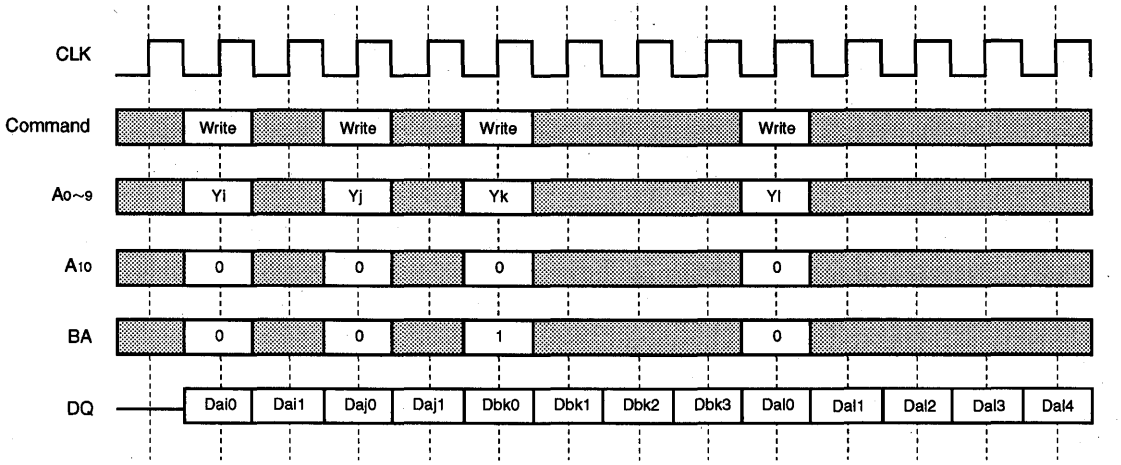
Read Interrupted by Burst Terminate (BL=4)



〔**Write Interrupted by Write**〕

Burst write operation can be interrupted by new write of the same or the other bank. JEDEC 2n-rule also must be kept. 2, 4 or 6 write to write interval is allowed in case of BL=8.

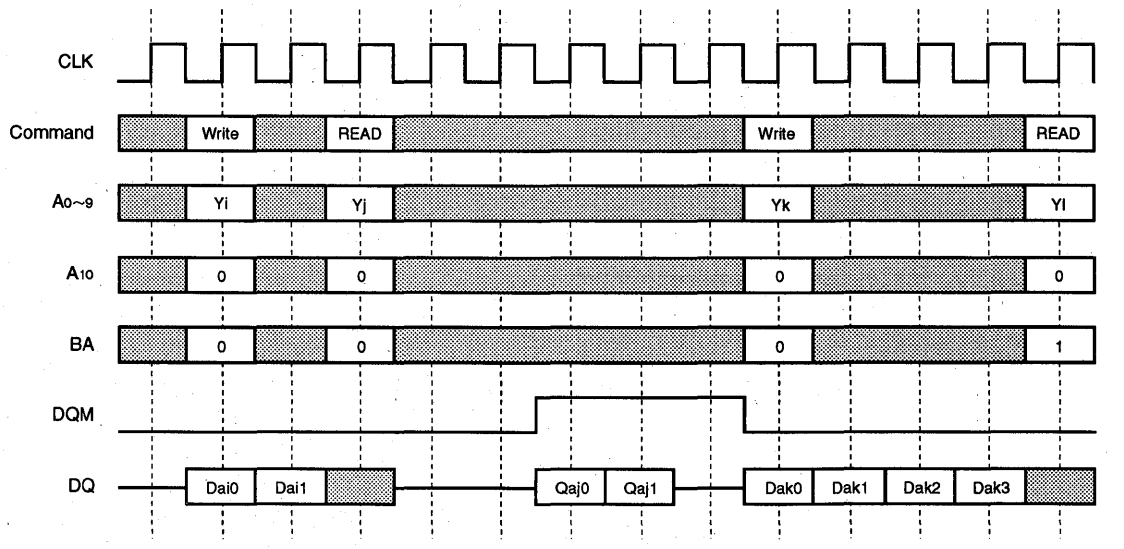
Write Interrupted by Write (BL=8)



〔**Write Interrupted by Read**〕

Burst write operation can be interrupted by read of the same or the other bank. JEDEC 2n-rule also must be kept here. The input data on DQ at the interrupting READ cycle is "don't care".

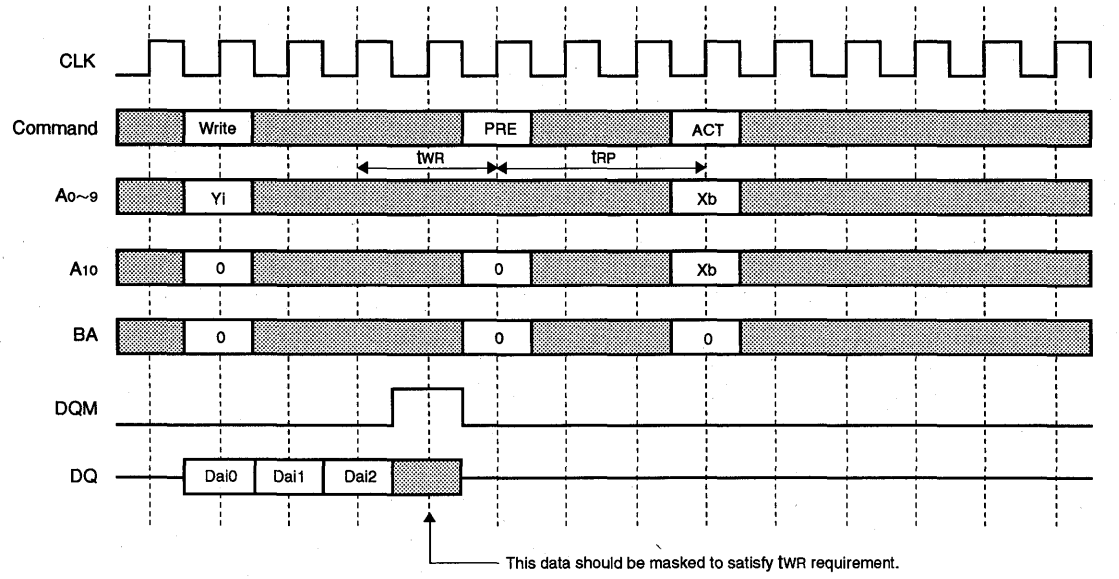
Write Interrupted by Read (BL=8, CL=3)



〔**Write Interrupted by Precharge**〕

Burst write operation can be interrupted by precharge of the same bank. JEDEC 2n-rule also must be kept here. Because the write recovery time (tWR) is required between the last input data and the next PRE, 4th data should be masked with DQM shown as below.

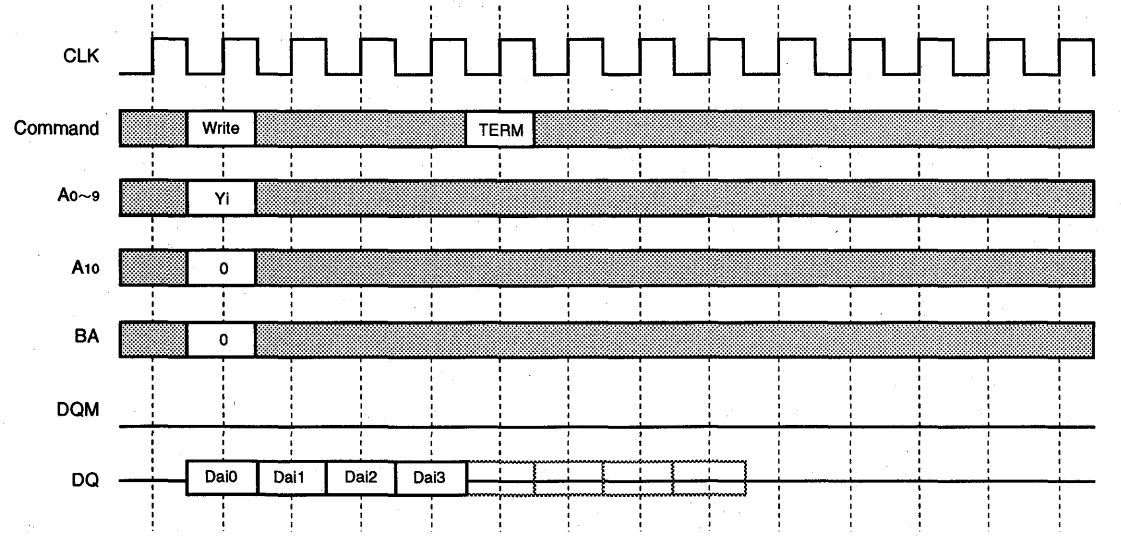
Write Interrupted by Precharge (BL=8)



〔**Write Interrupted by Burst Terminate**〕

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 4 words of data are written. JEDEC 2n-rule also must be kept here.

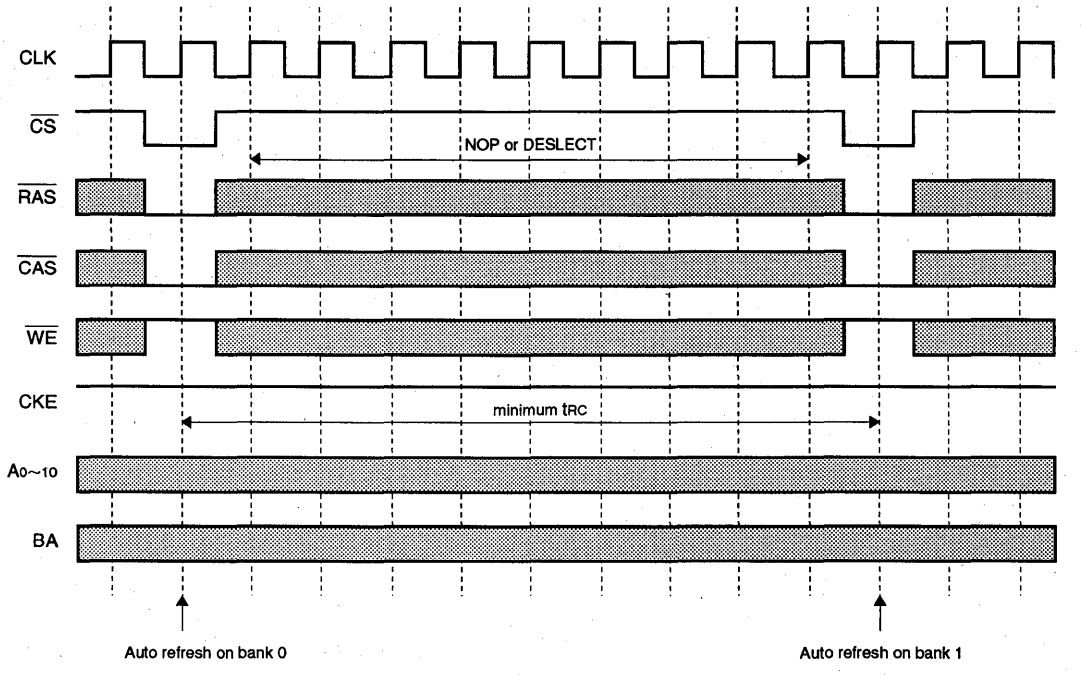
Write Interrupted by Burst Terminate (BL=8)



AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA ($\overline{CS}$=$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 16Mbit memory cells. The auto-refresh is performed on each bank alternately (ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before t_{RC} from the REFA command.

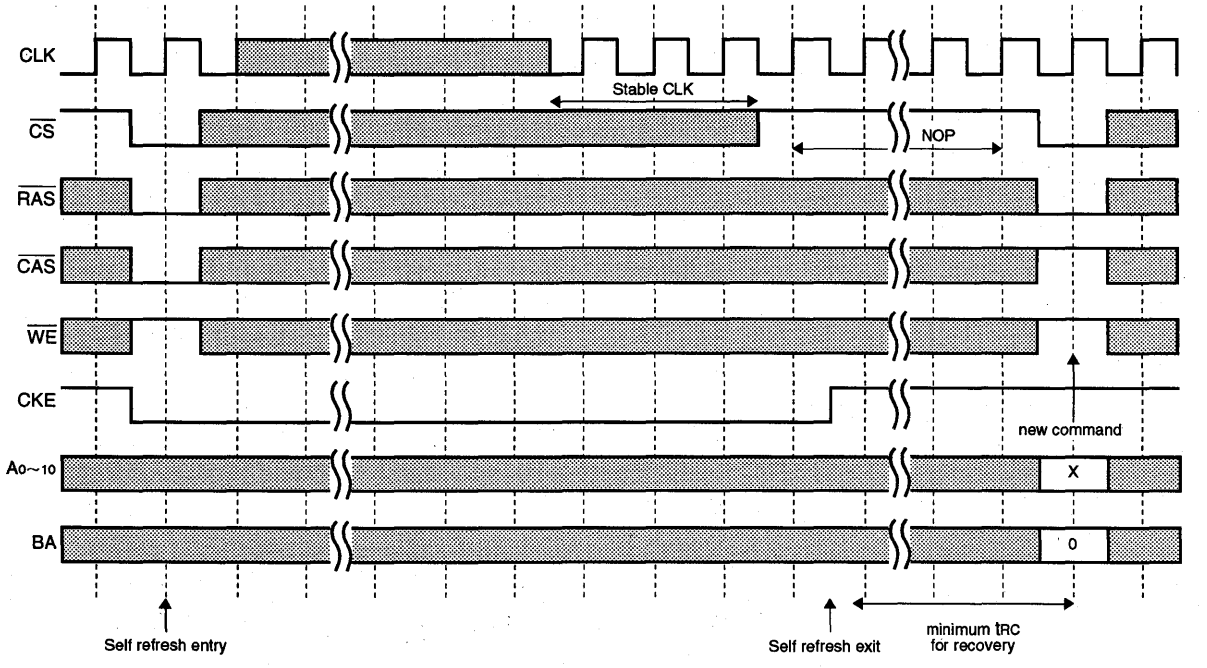
Auto-Refresh



SELF REFRESH

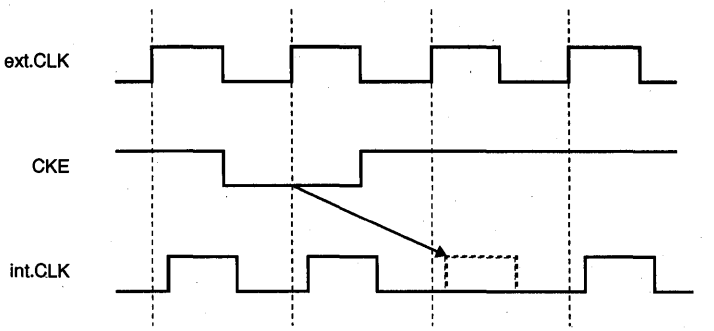
Self-refresh mode is entered by issuing a REFS command ($\overline{CS}$=$\overline{RAS}$=$\overline{CAS}$=L, $\overline{WE}$=H, CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input (but asynchronous), all other inputs including CLK are disabled and ignored, and power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE (REFSX). After t_{RC} from REFSX both banks are in the idle state and a new command can be issued after t_{RC}, but DESEL or NOP commands must be asserted till then.

Self-Refresh

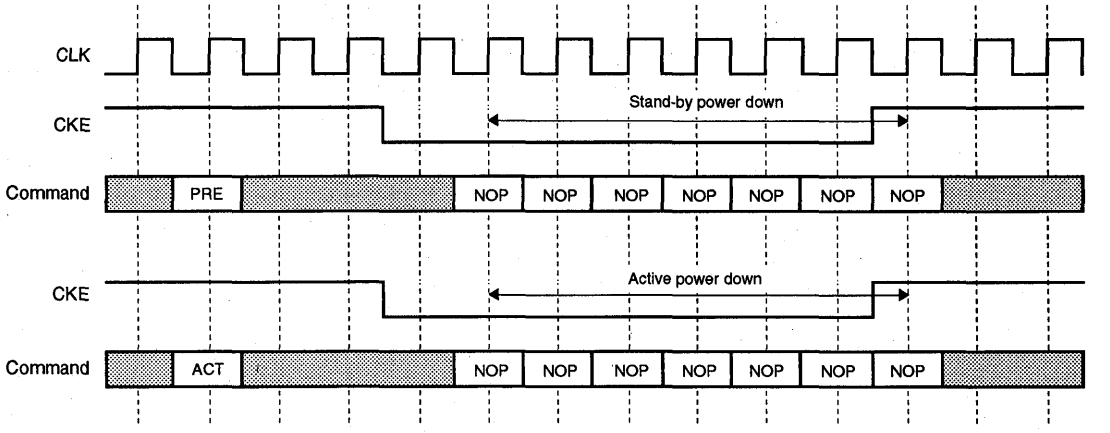


CLK SUSPEND

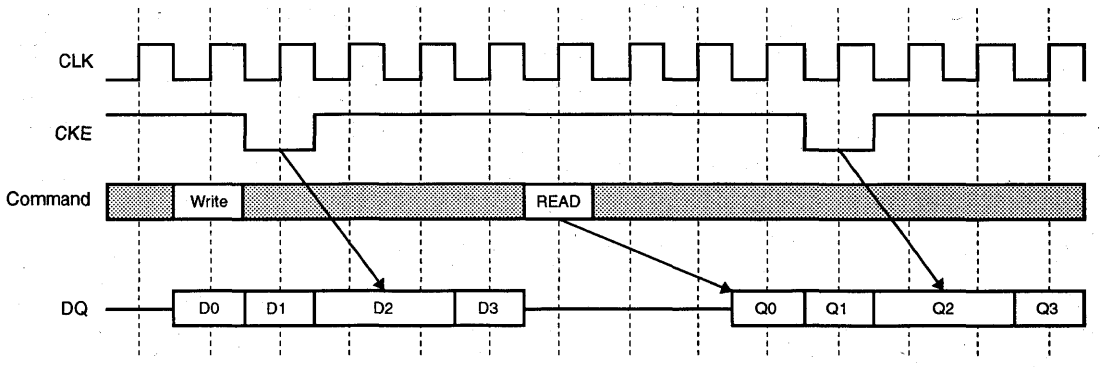
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



Power Down by CKE



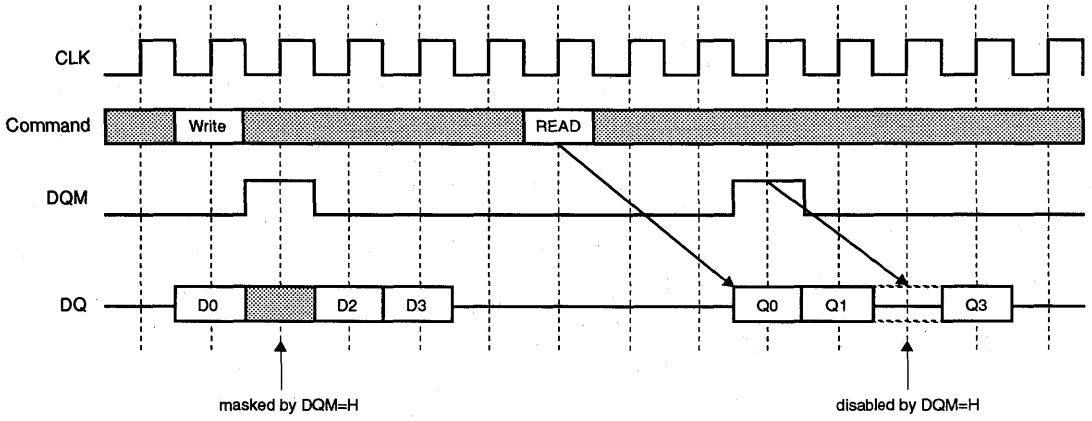
DQ Suspend by CKE



DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQM masks input data word by word. DQM to write mask latency is 0. During reads, DQM forces output to Hi-Z word by word. DQM to output Hi-Z latency is 2.

DQM Function



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

16777216-BIT (2-BANK x 2097152-WORD BY 4-BIT) SYNCHRONOUS DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_{DDQ}	Supply voltage for output	With respect to VssQ	-0.5~4.6	V
V_I	Input voltage	With respect to Vss	-0.5~4.6	V
V_O	Output voltage	With respect to VssQ	-0.5~4.6	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{DDQ}	Supply voltage for output	3.0	3.3	3.6	V
VssQ	Supply voltage for output	0	0	0	V
V_{REF}	Input reference voltage	1.3	1.5	1.7	V
V_{IH}	High-level input voltage, all inputs	V_{REF}+0.4		V_{DDQ}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		V_{REF}-0.4	V
V_{TT}	Termination voltage	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V

CAPACITANCE (Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, V_{REF}=0.45×V_{DDQ}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address pin	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(C)}$	Input capacitance, control pin				5	pF
$C_{I(K)}$	Input capacitance, CLK pin				5	pF
$C_{I/O}$	Input capacitance, I/O pin				7	pF

AVERAGE SUPPLY CURRENT from V_{DD} (Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			M5M4S16S21CTP			
			-7	-8	-10	
			Max	Max	Max	
I_{CC1S}	Operating current, single bank	t_{RC}=min, t_{CLK}=min, BL=1, CL=3 or 4	155	140	115	mA
I_{CC1d}	Operating current, dual bank	t_{RC}=min, t_{CLK}=min, BL=1, CL=3 or 4	230	205	170	mA
I_{CC2h}	Stand-by current, CKE=H	Both banks idle, t_{CLK}=min, CKE=H	65	60	50	mA
I_{CC2l}	Stand-by current, CKE=L	Both banks idle, t_{CLK}=min, CKE=L	10	9	7	mA
I_{CC3}	Active stand-by current	Both banks active, t_{CLK}=min, CKE=H	95	80	65	mA
I_{CC4}	Burst current	t_{CLK}=min, BL=4, CL=3 or 4, 1 bank idle	120	100	80	mA
I_{CC5}	Auto-refresh current	t_{RC}=min, t_{CLK}=min	140	125	105	mA
I_{CC6}	Self-refresh current		8	8	8	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0~70°C, V_{DD}=V_{DDQ}=3.3±0.3V, Vss=VssQ=0V, V_{TT}=0.45×V_{DDQ}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$V_{OH(DC)}$	High-level output voltage (DC)	I_{OH}=16mA	V_{TT}+0.8		V
$V_{OL(DC)}$	Low-level output voltage (DC)	I_{OL}=16mA		V_{TT}-0.8	V
I_{OZ}	Off-state output current	Q floating V_O=0 ~ V_{DDQ}	-10	10	µA
I_I	Input current	V_{IH} = 0 ~ V_{DDQ}+0.3V	-10	10	µA

MITSUBISHI ELECTRIC

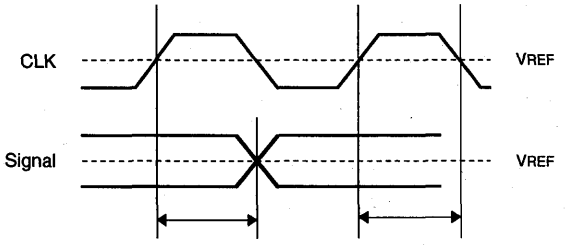
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

AC TIMING REQUIREMENTS (Ta=0~70°C, V_{DD}=$V_{DD}Q$=3.3±0.3V, V_{SS}=$V_{SS}Q$=0V, V_{REF}=0.45×$V_{DD}Q$, unless otherwise noted)

Input pulse levels ---------- V_{REF}±0.4V

Input timing measurement level ---------- V_{REF}

Symbol	Parameter		Limits						Unit
			M5M4S16S21CTP-7		M5M4S16S21CTP-8		M5M4S16S21CTP-10		
			Min	Max	Min	Max	Min	Max	
t_{CLK}	CLK cycle time	CL=1	27		28		30		ns
		CL=2	13.5		14		15		ns
		CL=3	9		9.5		10		ns
		CL=4	6.7		8		10		ns
t_{CH}	CLK high pulse width		2.5		3		4		ns
t_{CL}	CLK low pulse width		2.5		3		4		ns
t_T	Transition time of CLK		1	10	1	10	1	10	ns
t_{IS}	Input setup time (all inputs)		1.5		1.5		2		ns
t_{IH}	Input hold time (all inputs)		0.5		1		1		ns
t_{RC}	Row cycle time		80		90		100		ns
t_{RCD}	Row to column delay		21		24		30		ns
t_{RAS}	Row active time		50	10000	55	10000	60	10000	ns
t_{RP}	Row precharge time		28		32		40		ns
t_{WR}	Write recovery time		14		16		20		ns
t_{RRD}	Act to act delay time		21		24		30		ns
t_{RSC}	Mode register set cycle time		14		16		20		ns
t_{PDE}	Power down exit time		7		8		10		ns
t_{REF}	Refresh interval time			65.6		65.6		65.6	ms

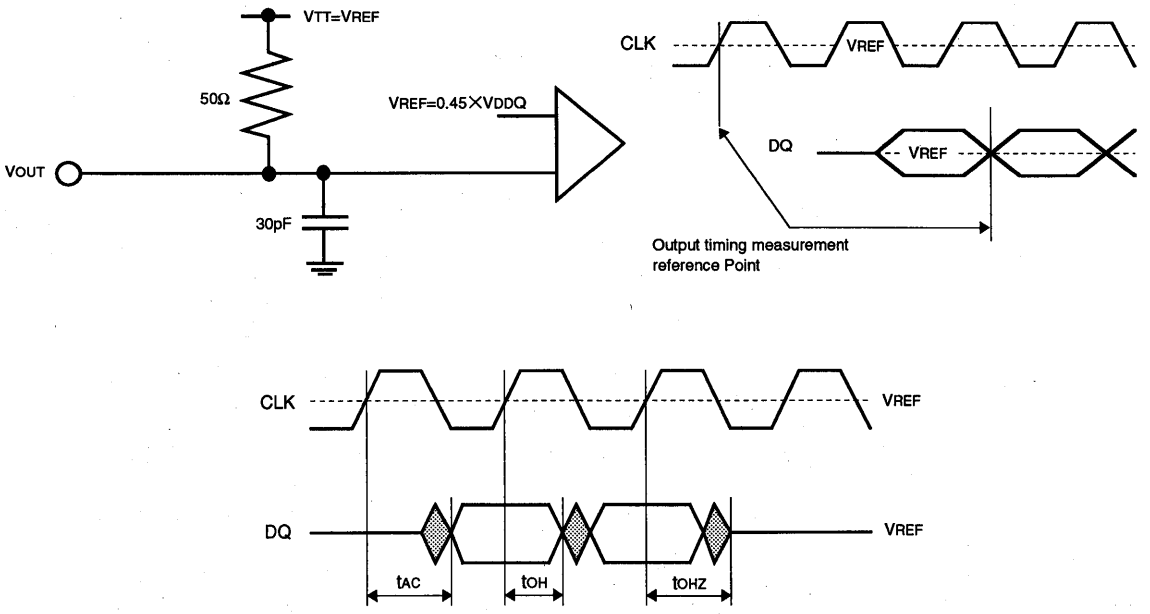


Any AC timing is referenced to the input signal crossing through the VREF level.

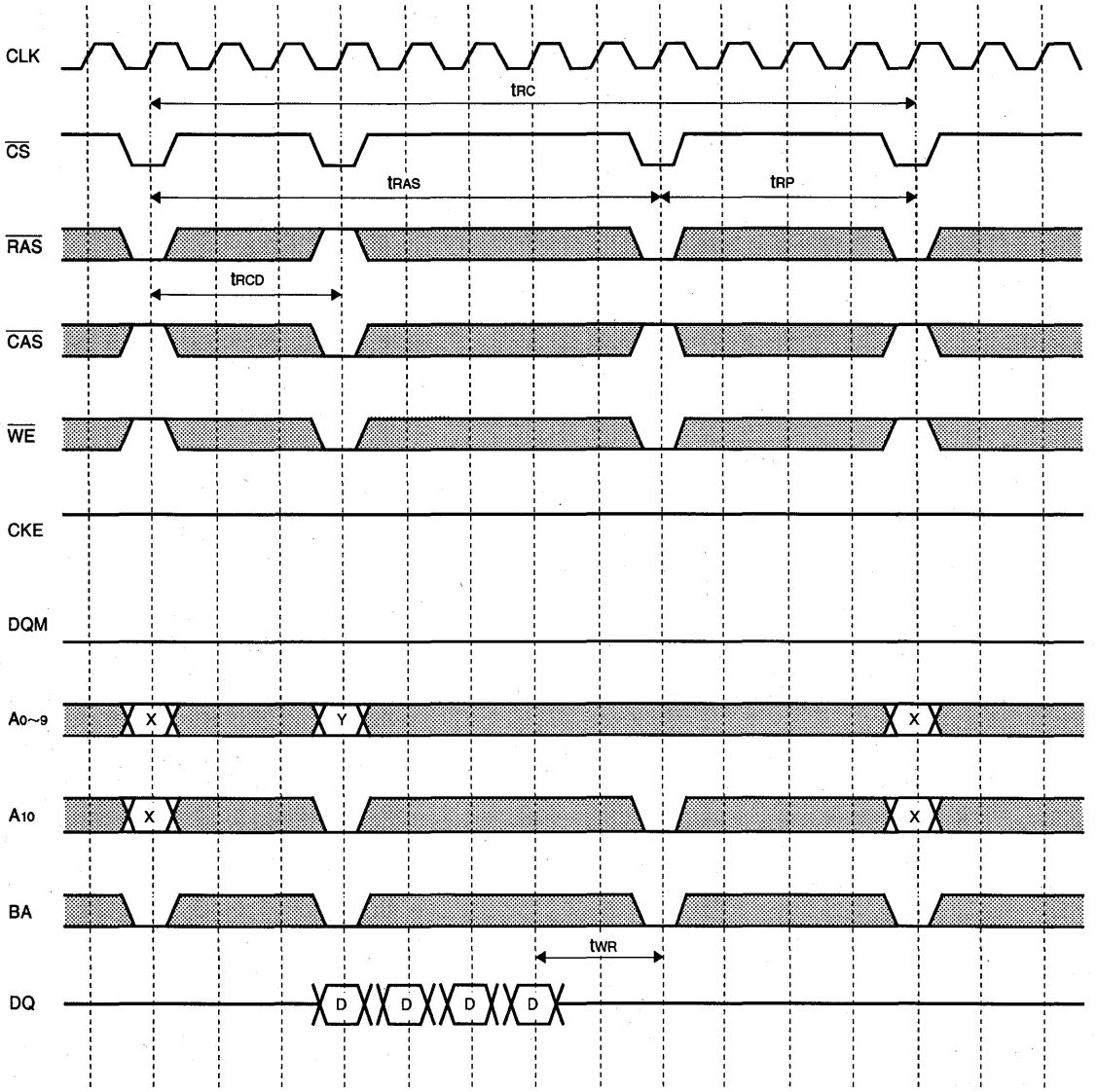
SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{DD}=V_{DD}Q=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			M5M4S16S21CTP-7		M5M4S16S21CTP-8		M5M4S16S21CTP-10		
			Min	Max	Min	Max	Min	Max	
t_{AC}	Access time from CLK	CL=1		25		26		27	ns
		CL=2		11.5		12		12	ns
		CL=3		7		7		8	ns
		CL=4		5		6		8	ns
t_{CAC}	Column access time			25		26		27	ns
t_{RAC}	Row access time			50		55		57	ns
t_{OH}	Output hold time from CLK		2		2.5		3		ns
t_{OLZ}	Delay time, output low impedance from CLK		0		0		0		ns
t_{OHZ}	Delay time, output high impedance from CLK		2	7	2.5	8	3	10	ns

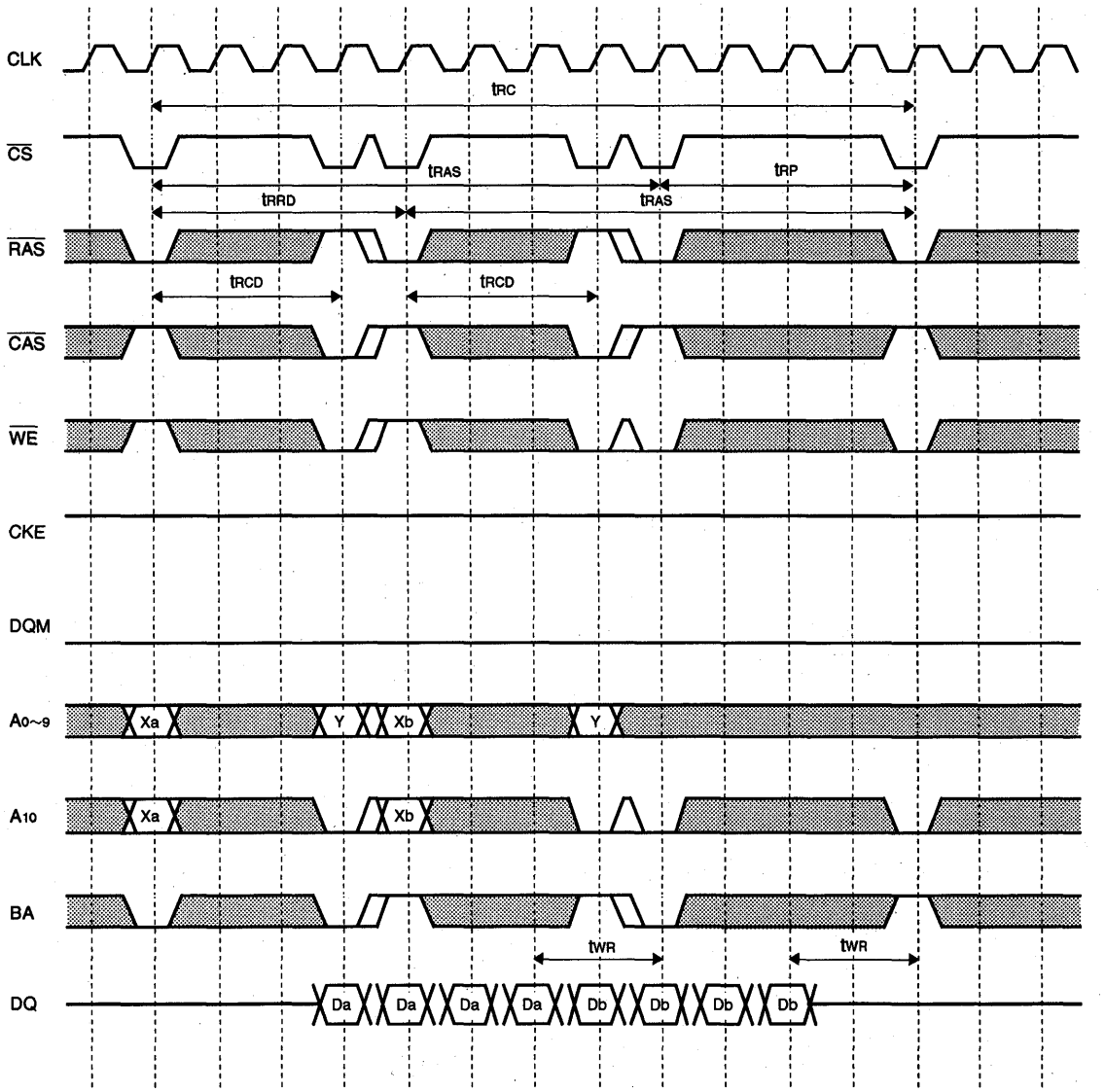
OUTPUT LOAD CONDITION



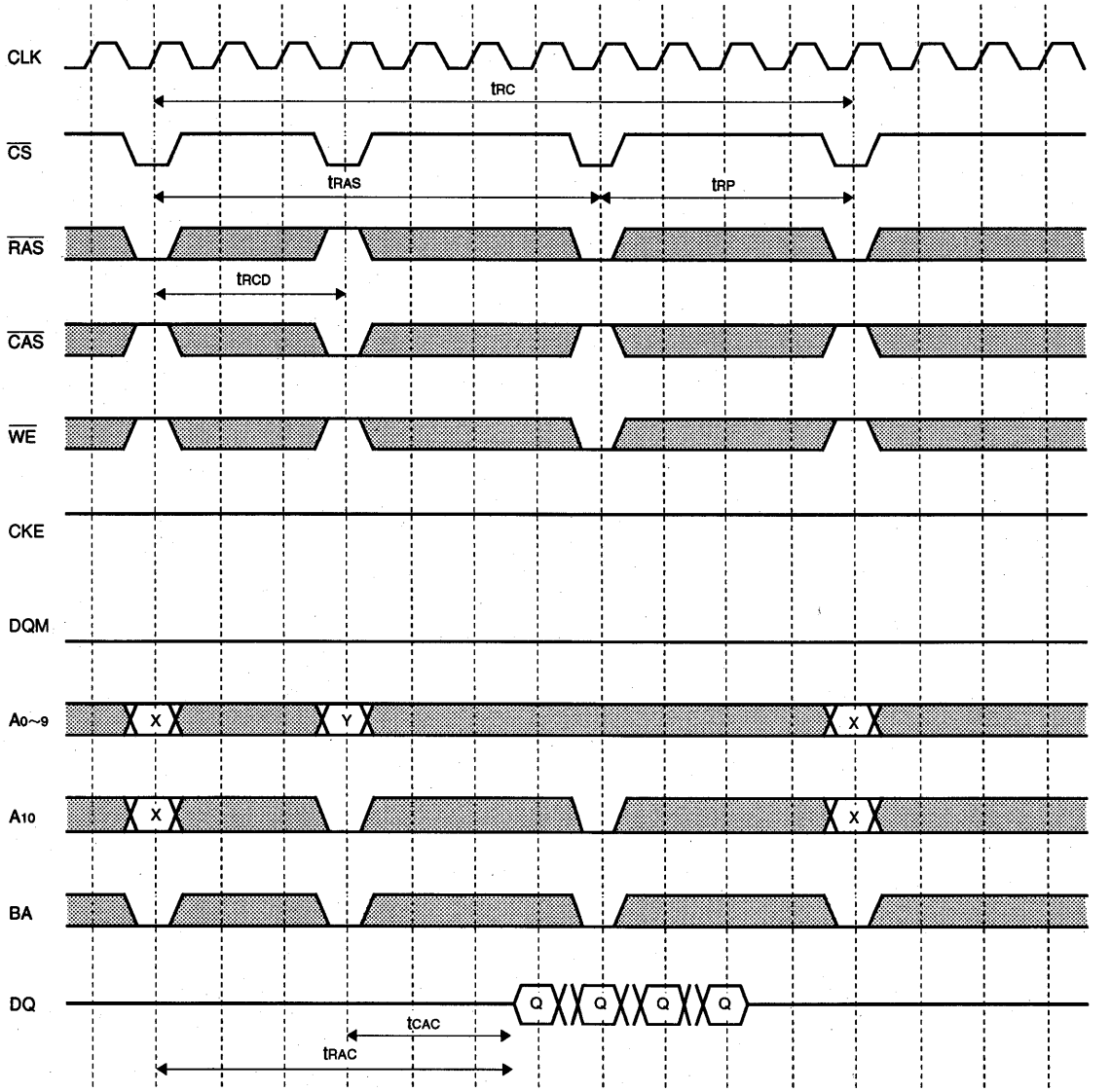
WRITE CYCLE (single bank) BL=4



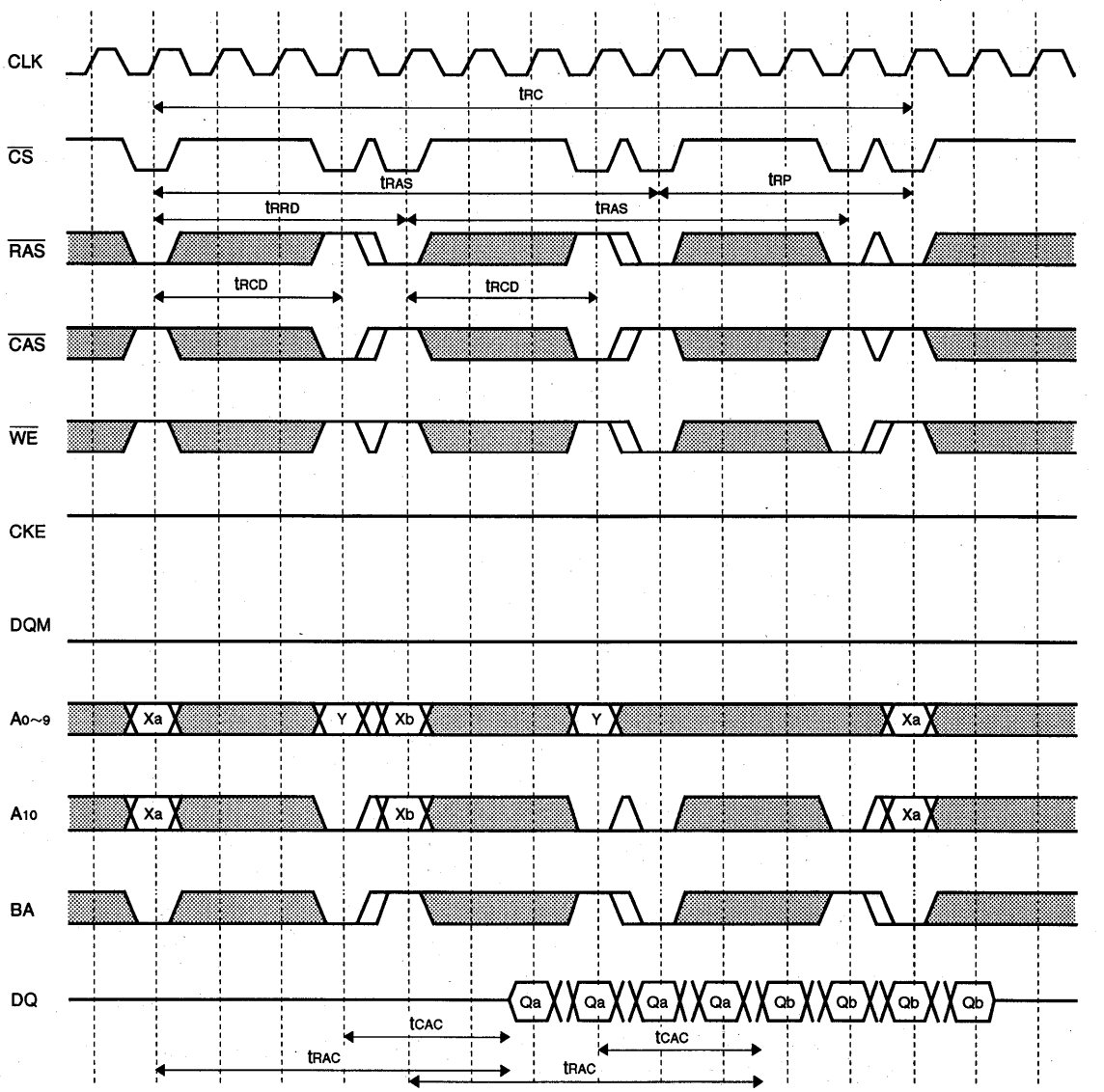
WRITE CYCLE (dual bank) BL=4



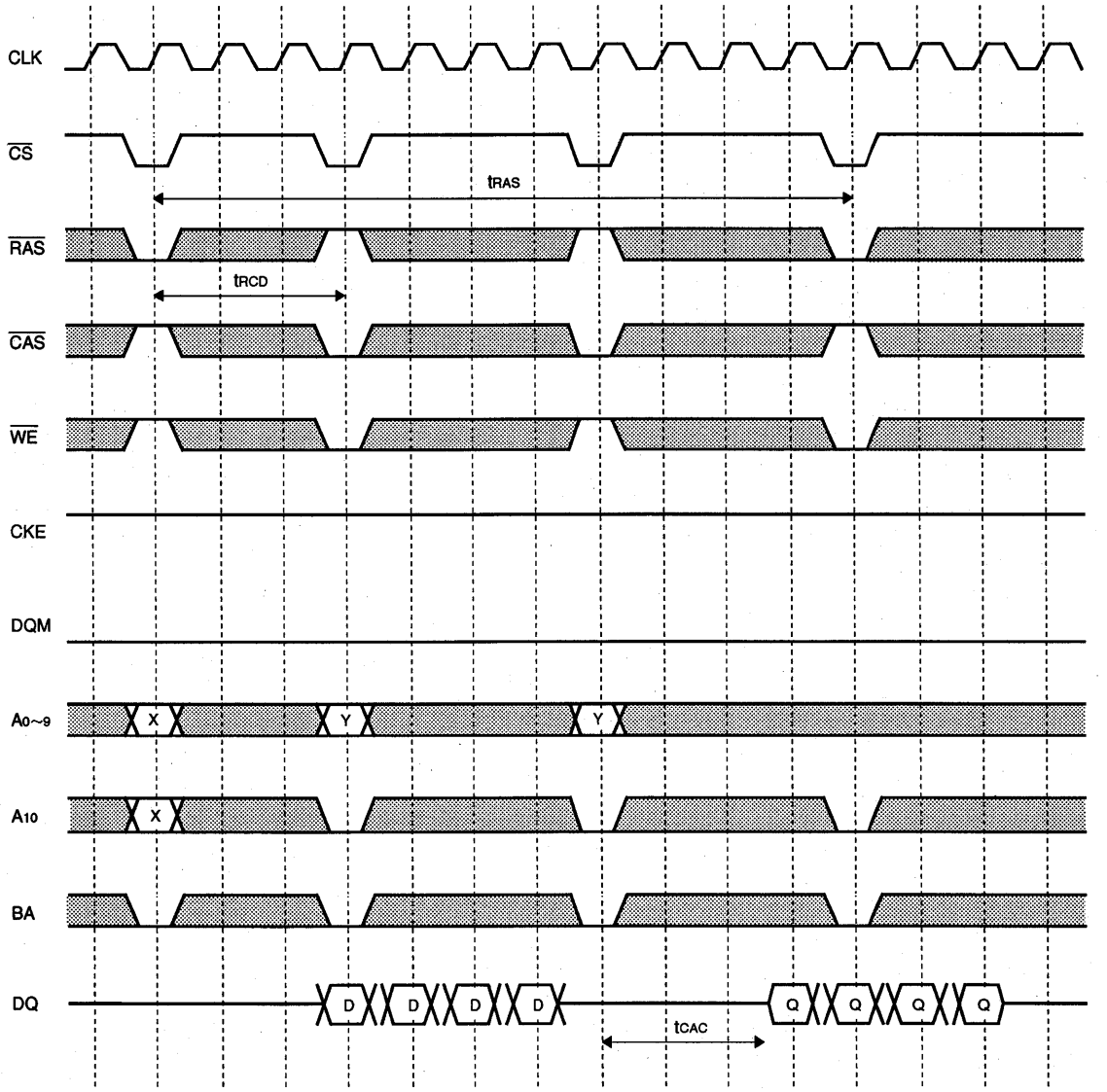
READ CYCLE (single bank) BL=4, CL=3



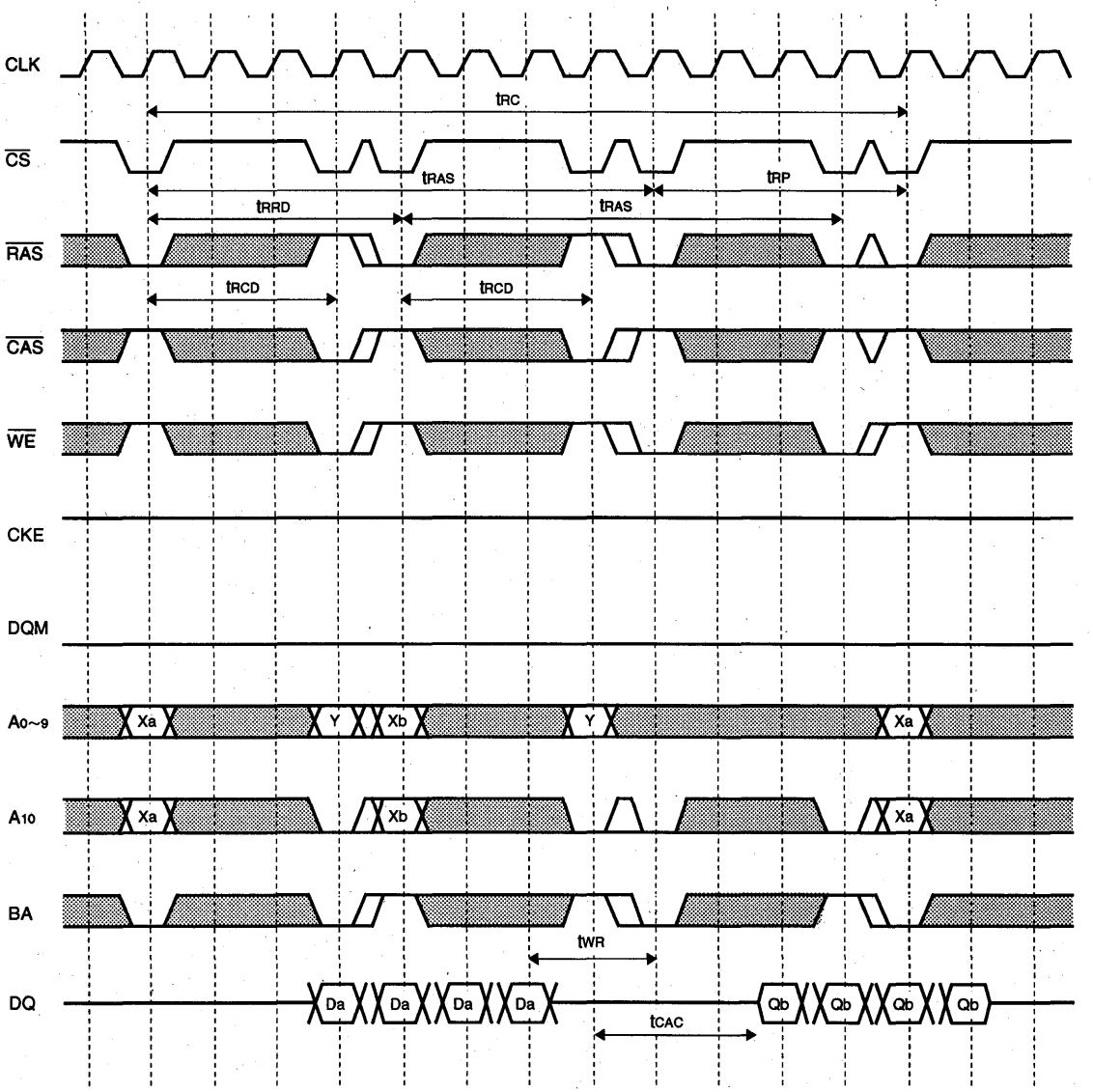
READ CYCLE (dual bank) BL=4, CL=3



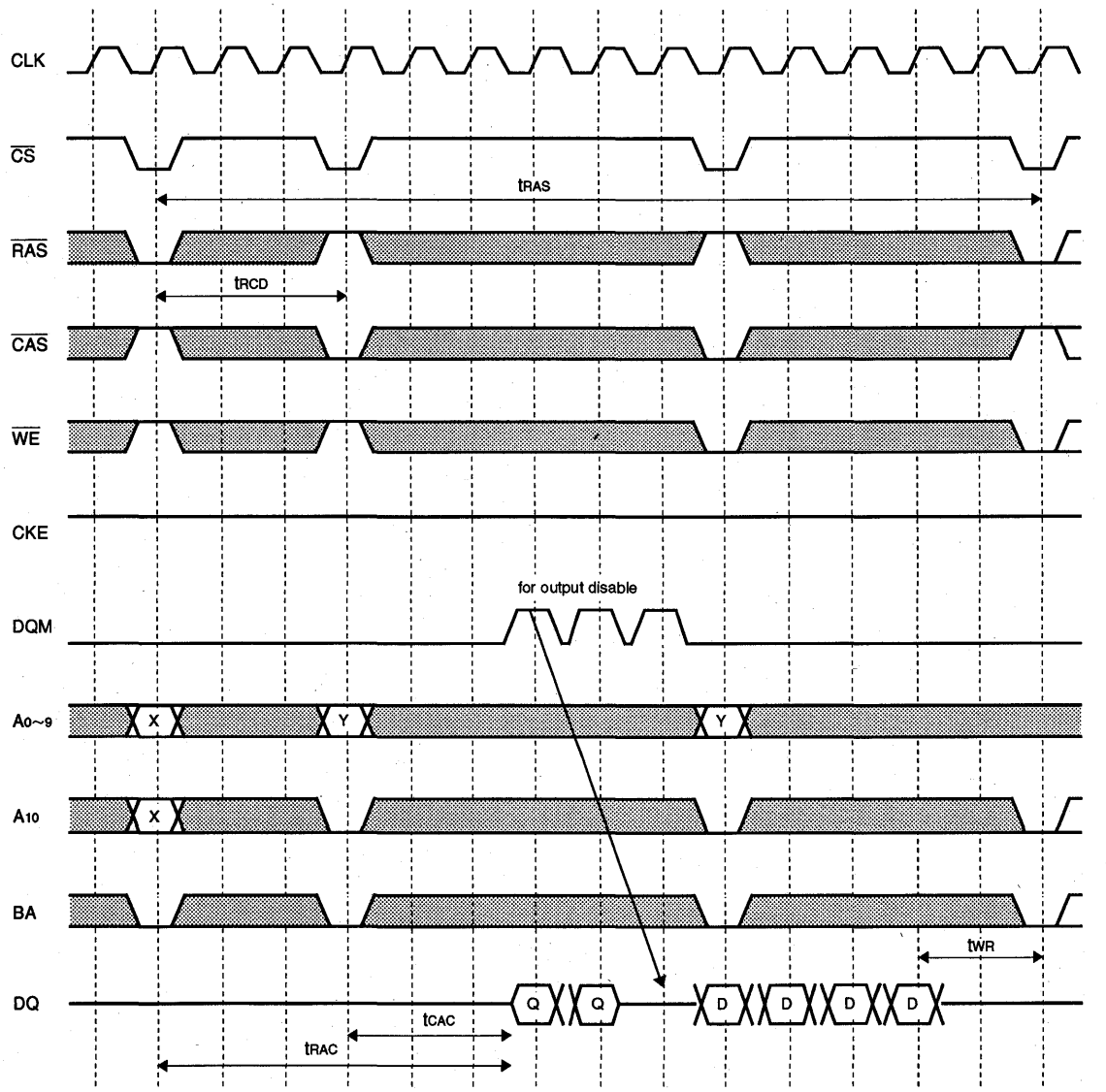
WRITE to READ (single bank) BL=4, CL=3



WRITE to READ (dual bank) BL=4, CL=3

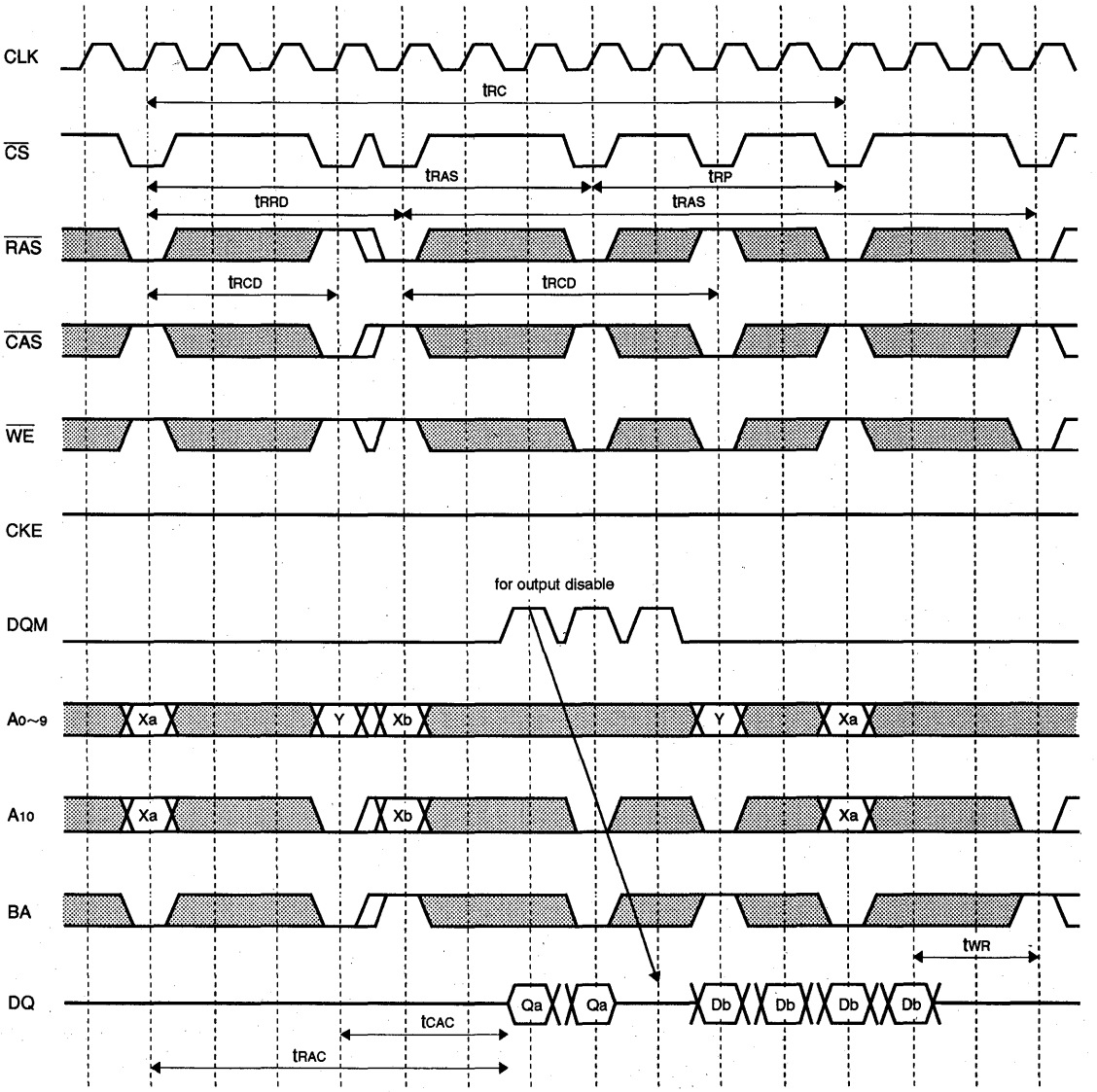


READ to WRITE (single bank) BL=4, CL=3

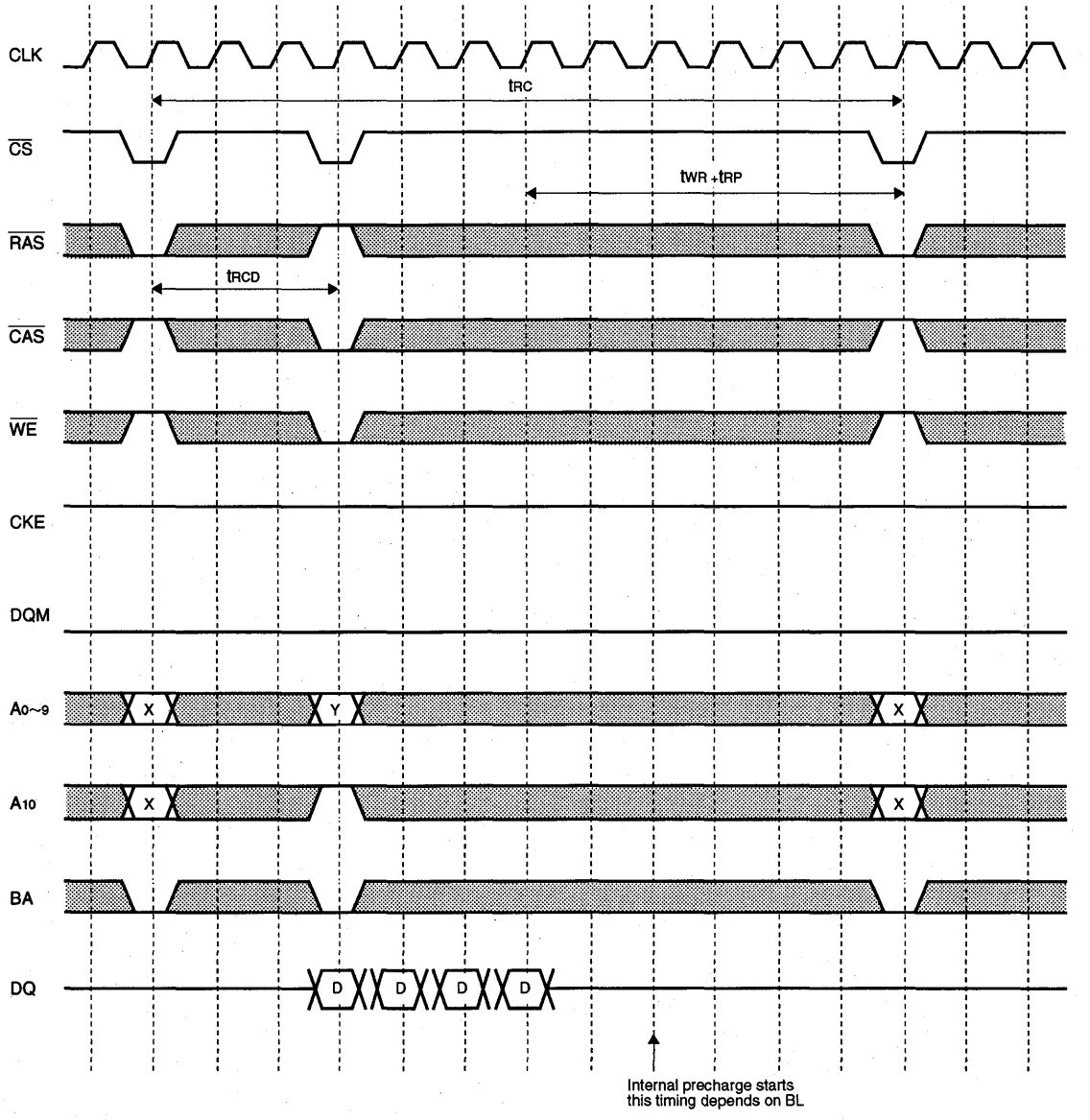


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

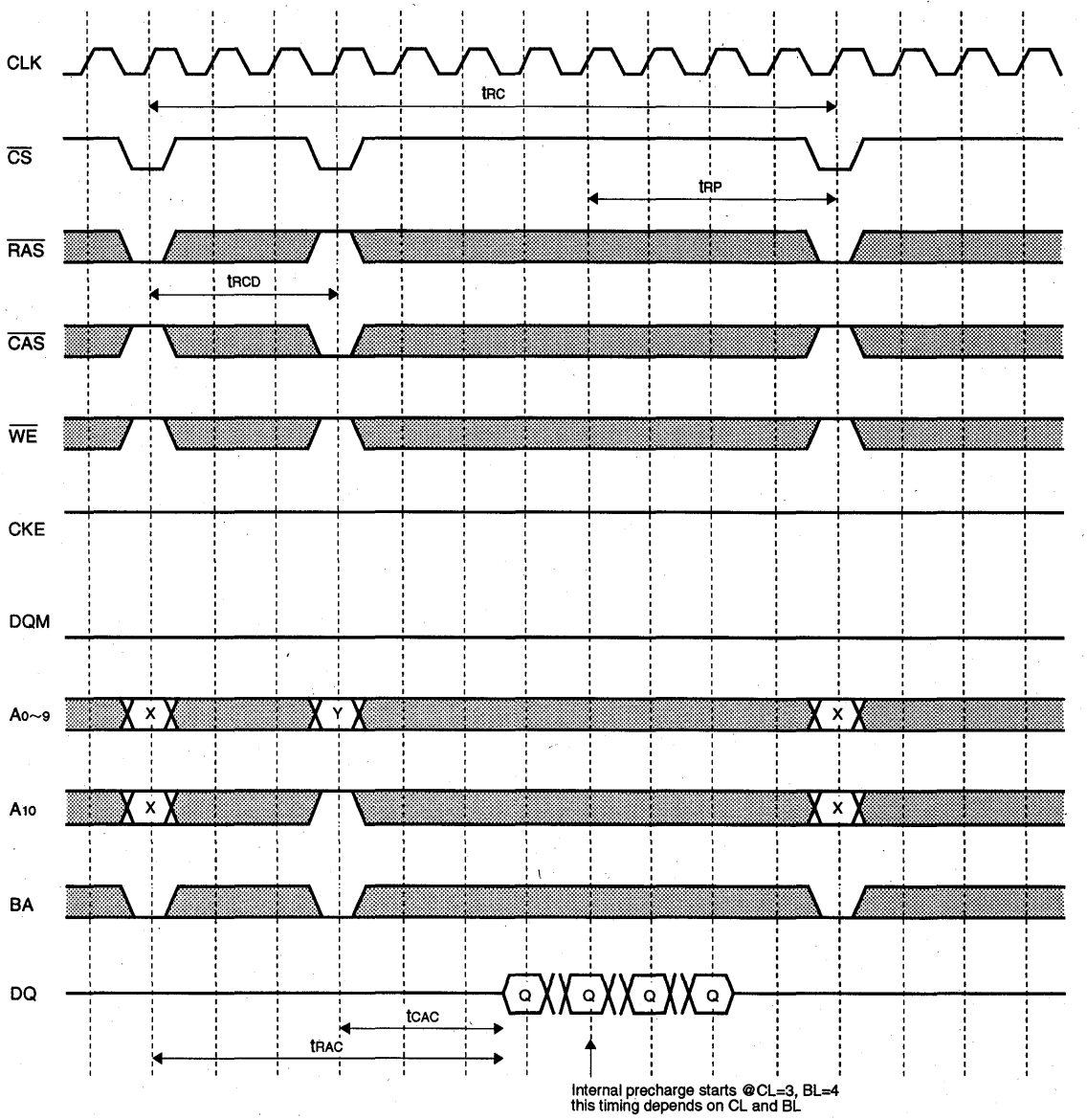
READ to WRITE (dual bank) BL=4, CL=3



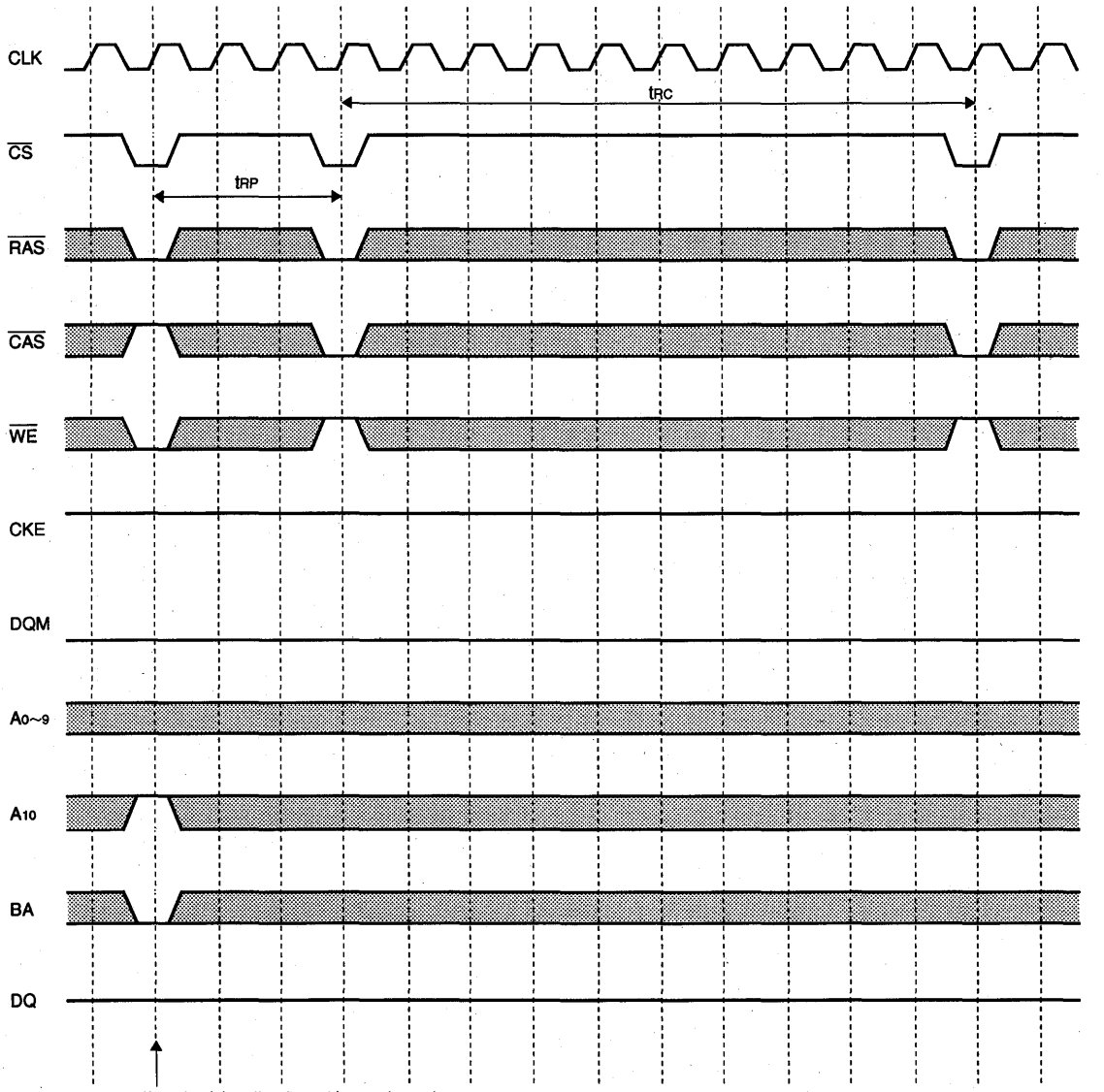
WRITE with AUTO-PRECHARGE BL=4



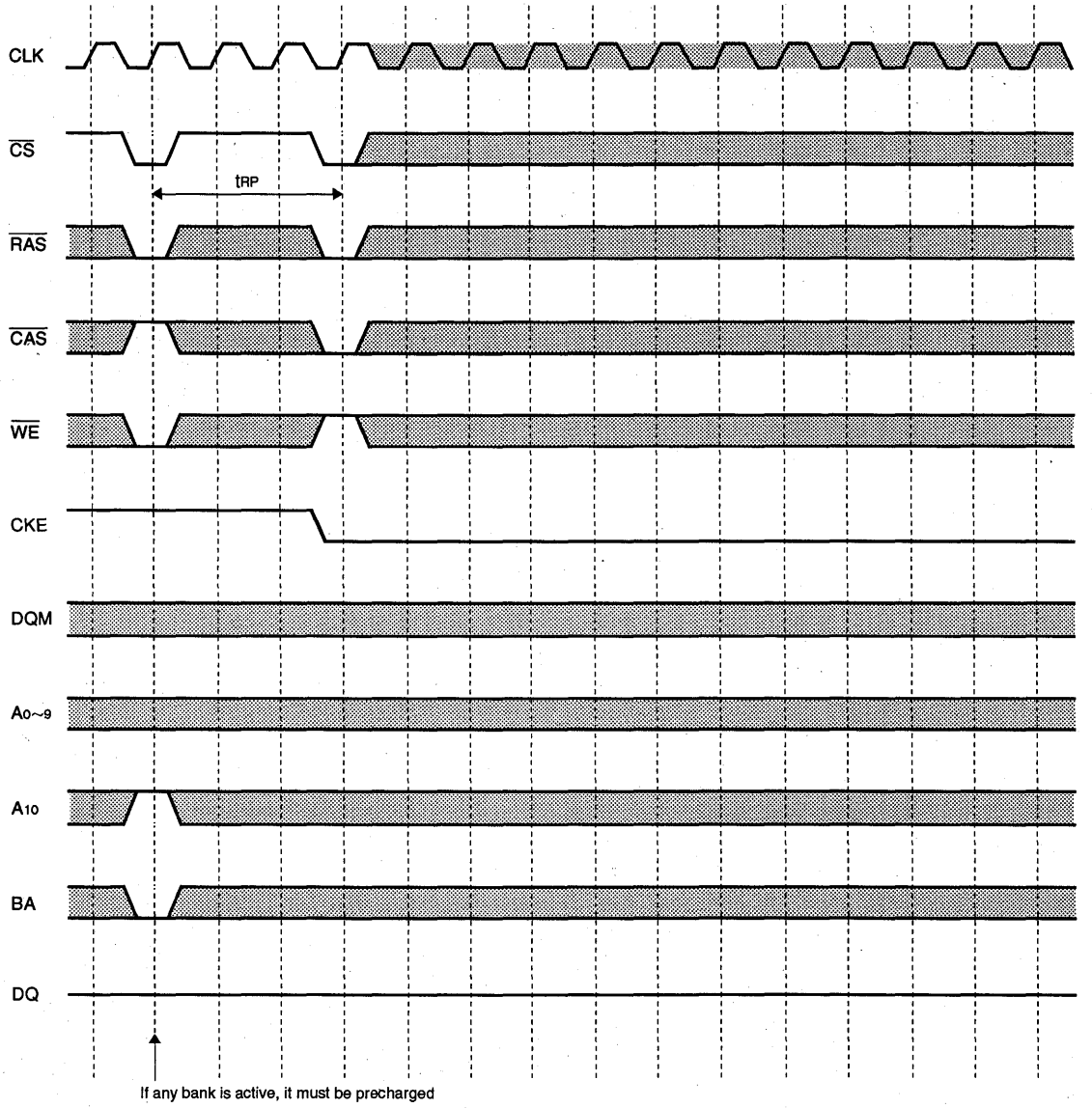
READ with AUTO-PRECHARGE BL=4, CL=3



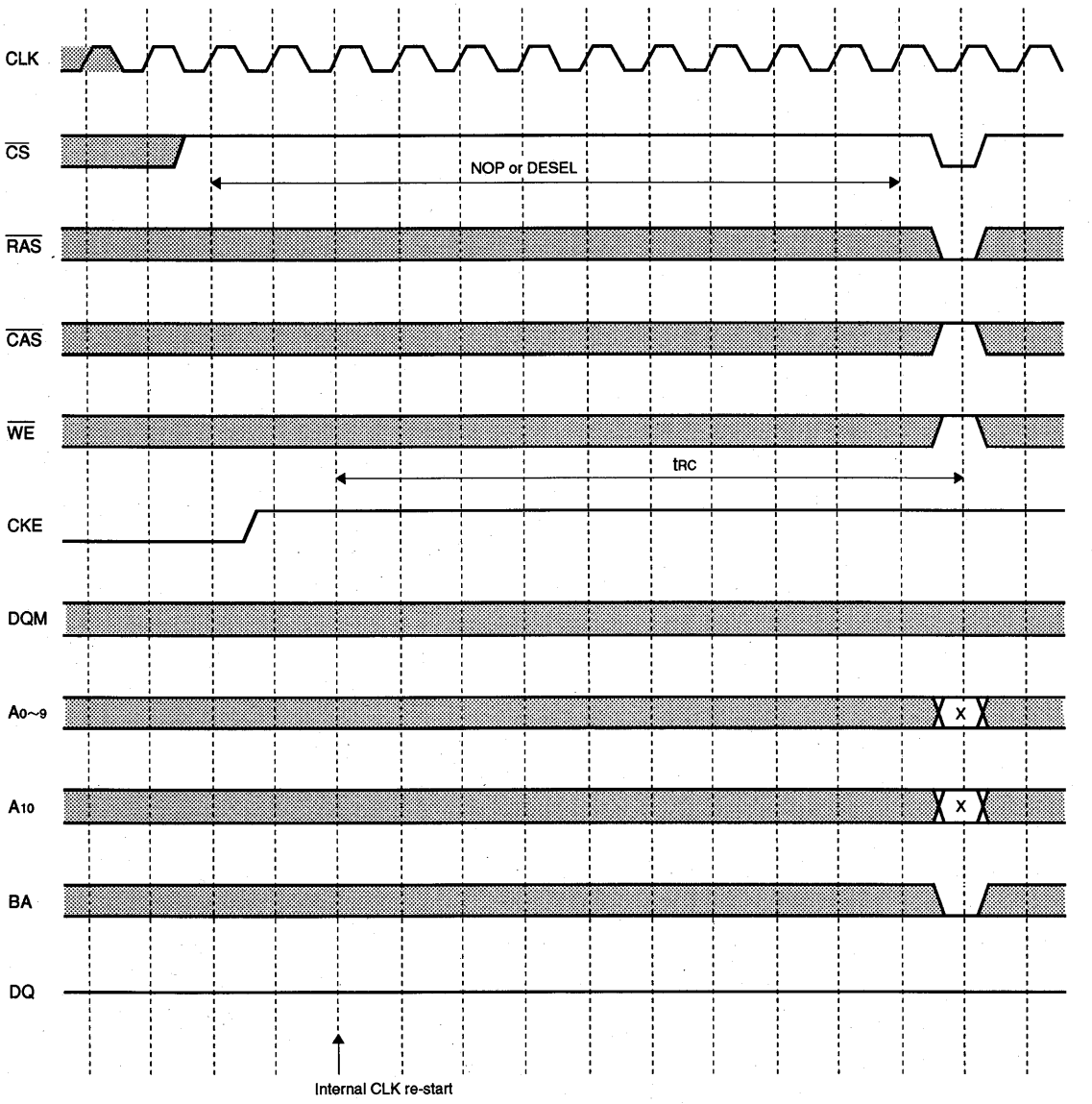
AUTO-REFRESH



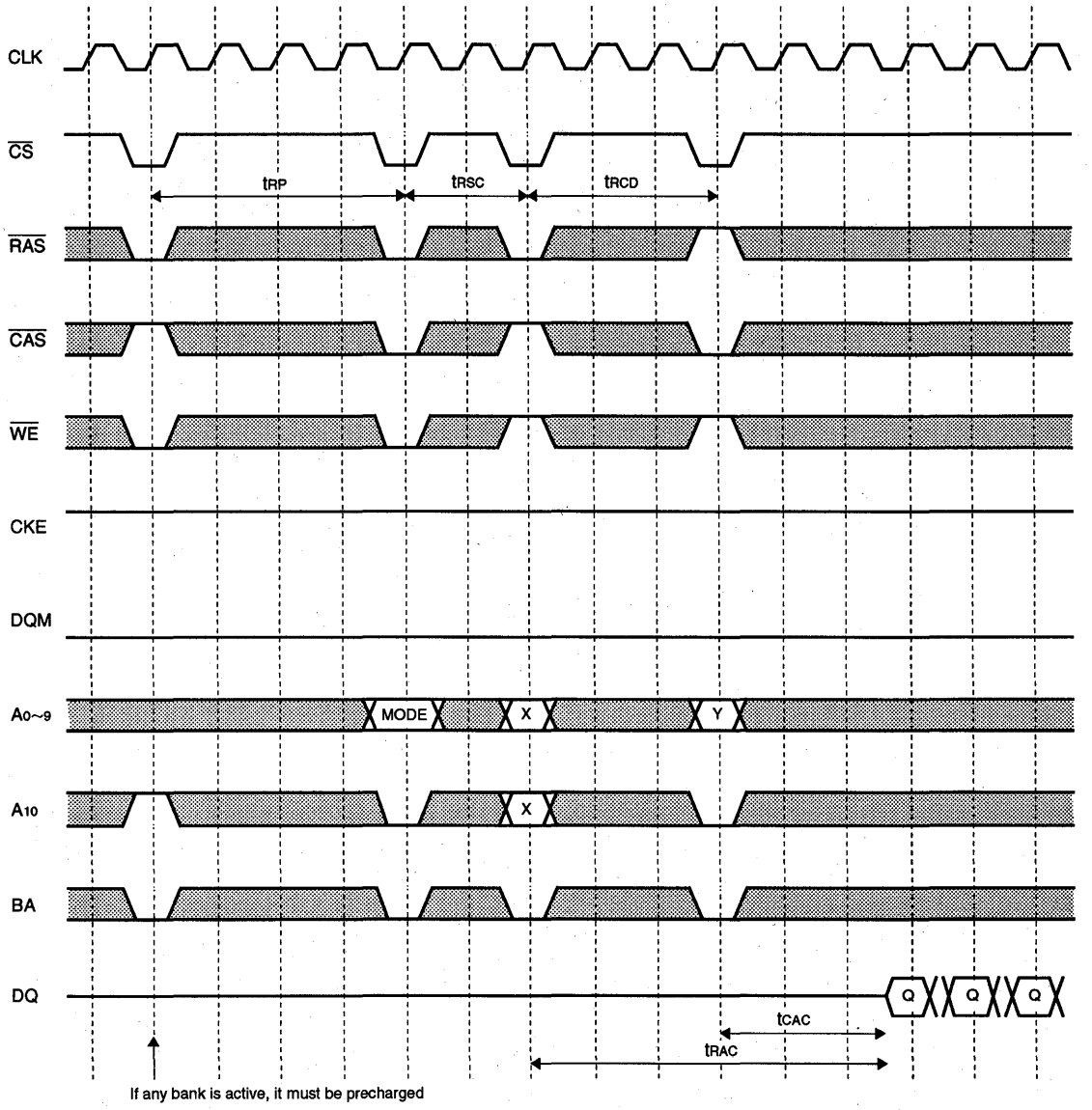
SELF-REFRESH ENTRY



SELF-REFRESH EXIT



MODE REGISTER SET BL=4, CL=3



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MITSUBISHI ELECTRIC

MITSUBISHI SEMICONDUCTORS
MEMORIES DRAM
DATA BOOK

December, First Edition 1995
Editioned by
Committee of editing of Mitsubishi Semiconductor Data Book

Published by
Mitsubishi Electric Corp., Semiconductor Marketing Division