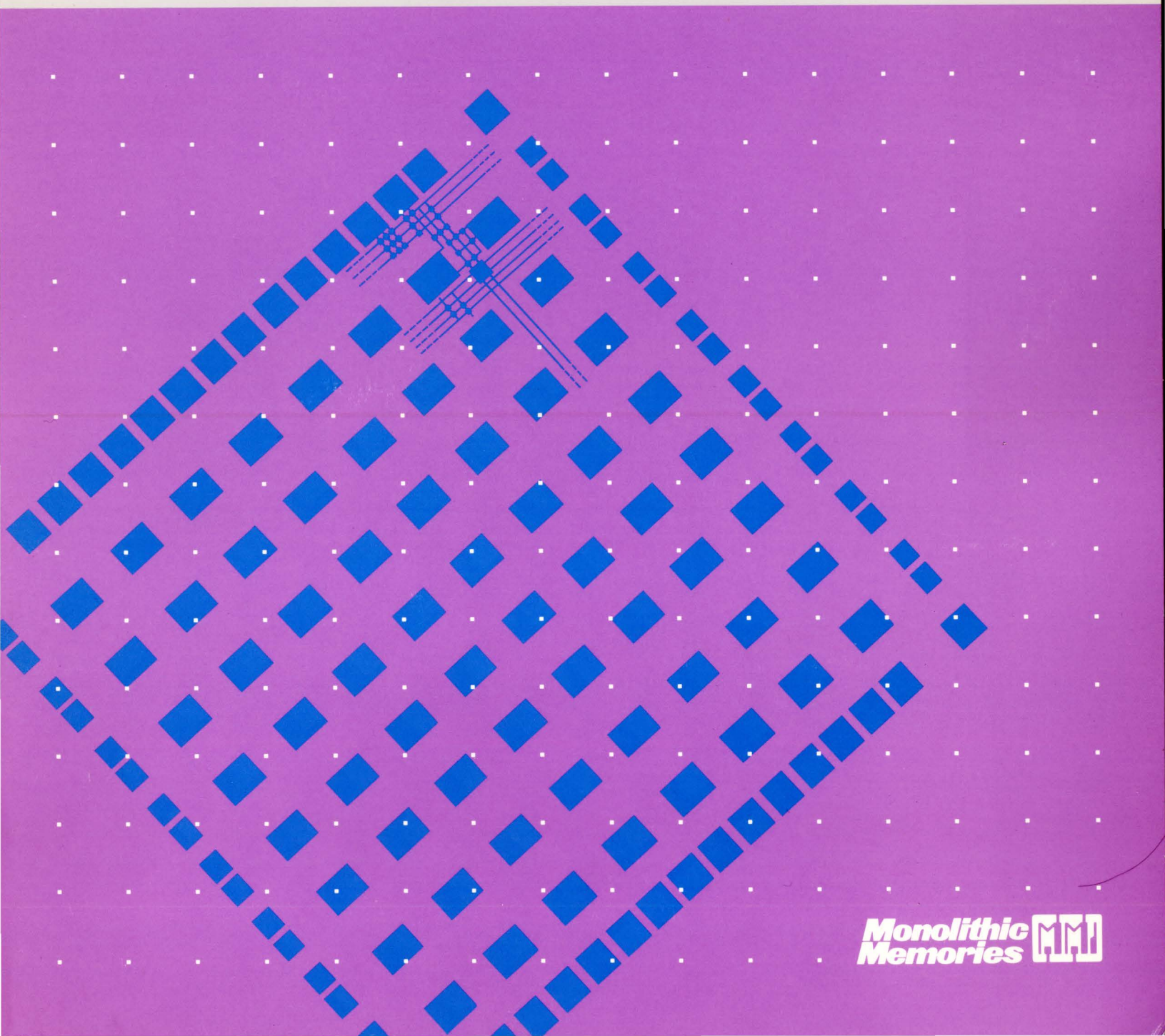
Logic Cell™ Array and Development System



Monolithic Memories MMI

Logic Cell™ Array and Development Systems

The Logic Cell Array

The Logic Cell Array (LCA) is the first device to successfully bridge the gap between field programmable logic and gate arrays. The LCA™ successfully combines the benefits of low-power CMOS LSI technology and the advantages of user programmability with the gate density and logic flexibility previously obtainable only with gate arrays.

The LCA provides a quantum jump in field-programmable logic device capability extending its usable functional density into a realm beyond that of more conventional programmable logic devices. Much greater gate utilization is achieved with the LCA by use of a flexible array type architecture more versatile than that of conventional PLDs, which is increasingly inefficient as gate density is increased. The Monolithic Memories M2018 1800-gate LCA device can replace as many as six 1200-gate PLD devices in some applications.

Gate arrays, on the other hand, provide densities higher than those of current LCAs. However, gate arrays typically require longer development times, design risks and significant cost.

The LCA is the ideal option for the PLD designer wishing to achieve a new level of system functional density and for the gate array user looking for a low-cost and easy-to-use alternative which provides instant prototyping through the power of in-circuit emulation

Component Ordering Information

M2018-50 CNL84

PART NUMBER
M2064 (1200 Gates, 58 IOB)
M2018 (1800 Gates, 74 IOB)

SPEED GRADE
-33 = 33 MHz Toggle Rate
-50 = 50 MHz Toggle Rate
-70 = 70 MHz Toggle Rate

PACKAGE TYPE
N48 = 48 Pin Molded DIP
NL68 = 68 Pin PLCC
NL84 = 84 Pin PLCC
P68 = 68 Pin PGA
P84 = 84 Pin PGA

TEMPERATURE RANGE
C = Commercial
M = Military

Package Availability

PART NUMBER	48-PIN PLASTIC DIP N48	68-PIN PLCC NL68	68-PIN PGA P68	84-PIN PLCC NL84	84-PIN PGA P84
M2064	X	X	X		
M2018		X	X	X	X

Ordering Information Development Systems

PART NUMBER	DESCRIPTION
LCA-MEK01	Logic Cell Array Evaluation Kit
LCA-MDS21	XACT™ Design Editor System
LCA-MDS22	P-SILOS™ Simulator
LCA-MDS23	Automatic Placement and Routing Program
LCA-MDS24-48N	XACTOR™ In-Circuit Emulator for 48-Pin DIP (includes one LCA-MDS26 and one LCA-MDS27-48N)
LCA-MDS24-68NL	XACTOR In-Circuit Emulator for 68-Pin PLCC (includes one LCA-MDS26 and one LCA-MDS27-68NL)
LCA-MDS24-68P	XACTOR In-Circuit Emulator for 68-Pin PGA (includes one LCA-MDS26 and one LCA-MDS27-68P)
LCA-MDS24-84NL	XACTOR In-Circuit Emulator for 84-Pin PLCC (includes one LCA-MDS26 and one LCA-MDS27-84NL)
LCA-MDS24-84P	XACTOR In-Circuit Emulator for 84-Pin PGA (includes one LCA-MDS26 and one LCA-MDS27-84P)
LCA-MDS26	Universal Emulation Pod
LCA-MDS27-48N	Emulation Header Cable for 48-Pin DIP
LCA-MDS27-68NL	Emulation Header Cable for 68-Pin PLCC
LCA-MDS27-68P	Emulation Header Cable for 68-Pin PGA
LCA-MDS27-84NL	Emulation Header Cable for 84-Pin PLCC
LCA-MDS27-84P	Emulation Header Cable for 84-Pin PGA
LCA-MDS31	FutureNet® DASH™ Schematic Design Entry Interface

Service Contracts

PART NUMBER	DESCRIPTION
LCA-MSC21	XACT Design Editor System (LCA-MDS21) Annual Support Agreement

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Logic Cell Array M2064, M2018

Features

- Fully Programmable
  - I/O functions
  - Digital logic functions
  - Interconnections
- General purpose array architecture
- Complete user control of design cycle
- Compatible arrays with logic cell complexity equivalent to 1200 and 1800 usable gates
- Standard product availability
- 100% factory-tested
- Selectable configuration modes
- Low-power, CMOS, static memory technology
- Three performance options: 33, 50, and 70 MHz
- TTL or CMOS input threshold levels
- Complete development system support
  - XACT Design Editor
  - Macro Library
  - Timing analyzer
  - Design rules checker
  - Configuration file generator
  - Configuration file formatter
- Optional features
  - Schematic capture entry
  - XACTOR in-circuit emulator
  - Logic and timing simulator
  - Auto Place/Route

Description

The Logic Cell Array (LCA) is a high-density CMOS user-programmable logic device. The array architecture of the LCA allows the designer total flexibility and yields extremely high gate utilization. The LCA is composed of three configurable logic elements: Input/Output Blocks (IOBs), Configurable Logic Blocks (CLBs), and Programmable Interconnect. The XACT development system Design Editor provides a graphical interface to configure individual IOBs for external interface, define CLBs to implement internal logic, and assemble an internal network of interconnect to accomplish larger logic functions. The XACT Design Editor provides an interactive graphic design capture system with an automatic routing feature. Both logic simulation and emulation are available for design verification.

Programming

The Logic Cell Array's logic functions and interconnections are determined by a configuration program stored in internal static memory cells. On-chip logic provides for automatic loading of configuration data at power-up or on command. The program data can reside in an EEPROM, EPROM, or ROM on the circuit board or on a floppy disk or hard disk.

Several methods of automatically loading the required data are designed into the Logic Cell Array and are determined by logic levels applied to mode selection pins at configuration time. The form of the data may be either serial or parallel, depending on the configuration mode. The programming data are independent of the configuration mode selected.

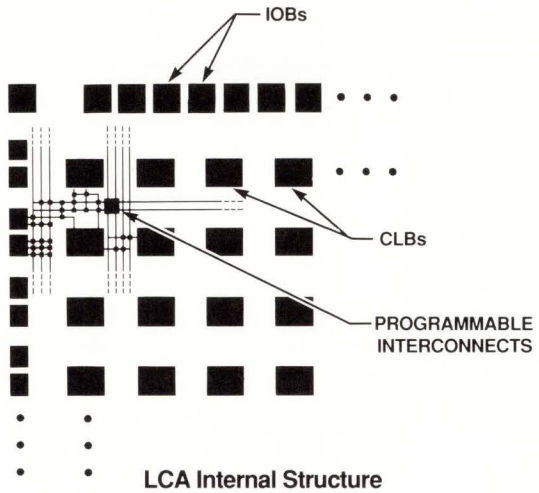
The Logic Cell Array is available in a variety of logic capacities, package styles, temperature ranges and speed grades.

Input/Output Block

Each user-configurable I/O block (IOB) provides an interface between the external package pin of the device and the internal logic. Each I/O block includes programmable input path and a programmable output buffer as shown in Figure 1. It also provides input clamping diodes to provide protection from electrostatic damage, and circuits to protect the LCA from latch-up due to input currents.

The input buffer portion of each I/O block provides threshold detection to translate external signals applied to the package pin to internal logic levels. The input buffer threshold of the I/O blocks can be programmed to be compatible with either TTL (1.4 V) or CMOS (2.2 V) levels.

Output buffers in the I/O blocks provide 4-mA drive for high fan-out CMOS- or TTL-compatible signal levels.



LCA Internal Structure

PART NUMBER	LOGIC CAPACITY (USABLE GATES)	CONFIG-URABLE LOGIC BLOCKS	USER I/Os	CONFIG-URATION PROGRAM (BITS)
M2064	1200	64	58	12038
M2018	1800	100	74	17878

Configurable Logic Block

An array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The Logic Blocks are arranged in a matrix in the center of the device. The M2064 has 64 such blocks arranged in an 8-row by 8-column matrix. The M2018 has 100 logic blocks arranged in a 10 by 10 matrix.

Each logic block has a combinatorial logic section, a storage element, and an internal routing and control section as shown in Figure 2. Each CLB has four general-purpose inputs: A, B, C, and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks.

Additional memory bits are used to set the user-definable path selectors, shown in Figure 2, which determine CLB internal connections. All memory bits are determined automatically by the XACT design editor as the design is entered.

The logic block combinatorial logic uses a table look-up memory to implement Boolean functions. This technique can generate any logic function of up to four variables with a high-speed, sixteen-bit memory. The propagation delay through the combinatorial network is independent of the function generated. Each block can perform any function of four input variables or any two functions of three input variables each. The input variables may be selected from among the four inputs and the block's storage element output "Q."

Programmable Interconnect

Programmable interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into desired networks. All interconnections are composed of metal segments, with programmable switching points provided to implement the necessary routing. Three types of resources accommodate different types of networks:

- General-purpose interconnect
- Long lines
- Direct connection

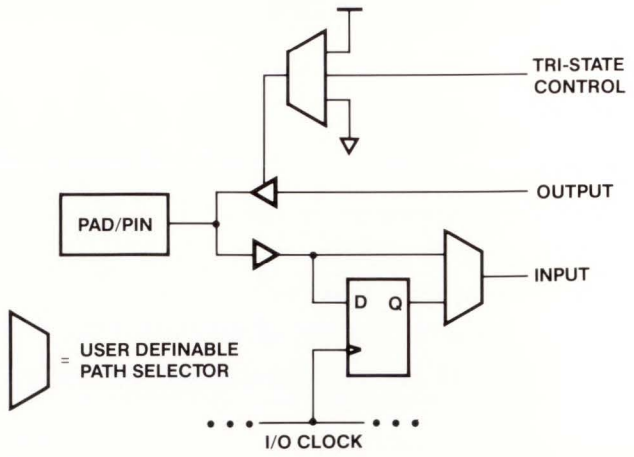


Figure 1. IOB Logic Equivalent

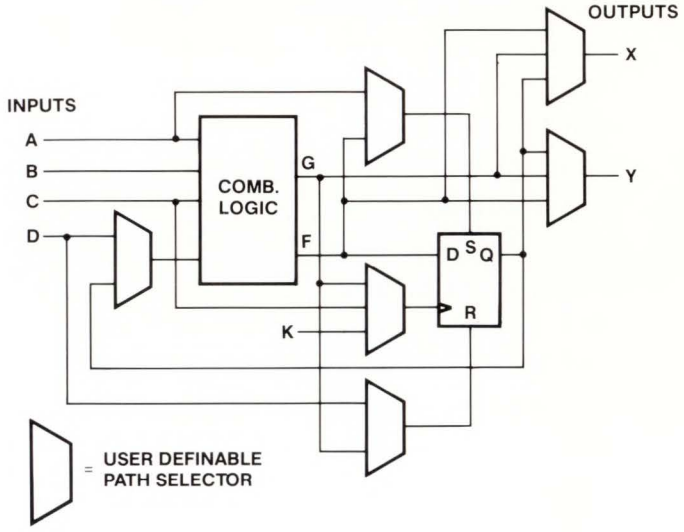


Figure 2. CLB Logic Equivalent

Summary of CLB Switching Characteristics

SYMBOL	PARAMETER		SPEED GRADE						UNIT
			-33		-50		-70		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ILO}	Logic input to output	Combinatorial		20		15		10	ns
t_{CKO}	K Clock	To output		20		15		10	ns
t_{ICK}		Logic-input setup	12		8		7		
t_{CKI}		Logic-input hold	0		0		0		
t_{PID}	Input/Output	Pad to input (direct)		12		8		6	ns
t_{OP}		Output to pad (enabled)		15		12		9	ns
F_{CLK}	Maximum flip-flop toggle frequency		33		50		70		MHz

LCA-MDS21 XACT Design Editor System

Features

- **Runs on an IBM® PC-XT™ or compatible computer**
- **Complete basic system for designing with Logic Cell Arrays**
- **Interactive graphical design editor**
- **Simplified definition, placement and interconnection capability for logic design and implementation**
- **Macro library of 113 standard logic family equivalents**
- **Utility for user-defined macros**
- **Boolean equation or Karnaugh map alternatives to specify logic functions**
- **Point-to-point timing calculations for critical path analysis**
- **Automatic design consistency checking for connectivity and design violations**
- **Documentation support with hardcopy output of logic and physical configuration information**
- **Download cable to transfer configuration programs from personal computer to LCA in target system**
- **Compatible hardware and software options to enhance design productivity**
- **File formatter for EPROM programmer**

General

The XACT Design Editor provides users with a complete design and development system for specification and implementation of designs using Monolithic Memories' Logic Cell Arrays. Functional definition of Configurable Logic Blocks (CLBs), Input/Output Blocks (IOBs) and interconnection is performed with a menu-driven interactive graphics editor. An automatic router greatly reduces the effort to interconnect logic.

Designs are captured with a graphics-based design editor using either a mouse for menu-driven entry, or a keyboard for command-driven entry. Functions are specified by CLB and IOB definitions plus their interconnections. The macro library and user-defined macros enable the user to easily implement complex functions.

The check for logic connectivity and design rule violation is easily performed. All unused internal nodes are automatically configured to minimize power dissipation.

Interactive point-to-point timing delay calculation is provided for timing analysis and critical path determination. This ability enables the user to quickly identify and correct timing problems while the design is in progress.

Automatic generation of similar input netlist files with timing parameters simplifies the use of P-SILOS for logic and timing simulation.

The XACT Design Editor includes hardcopy generation to document a design and automatically track design changes. Logic Cell Array configuration programs can be automatically translated into standard EPROM programming bit pattern formats.

A download cable included with XACT is useful for transferring configuration programs serially from the PC workstation to a Logic Cell Array installed in a system. During product development and debug this capability can be used to save the time required to write a modified configuration program into an EPROM.

Monolithic Memories provides ongoing support for XACT users. For the first year, software updates are included. After that the user may purchase the LCA-MSC21 Annual Support Agreement to continue to receive the latest software releases. XACT users also receive Monolithic Memories' technical information, which includes information about Logic Cell Arrays and PAL® devices, as well as software updates and application notes for designers. In addition, Monolithic Memories provides comprehensive field and factory support.

System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer with:

- MS-DOS™ 2.1 or higher
- 1M Bytes RAM
- 1 Diskette Drive
- 10-MB Hard Disk
- IBM compatible Color Graphic Adapter and Display
- 1 Serial Interface Port
- 1 Parallel Interface Port
- Mouse System™, Microsoft® or compatible mouse

Design Editor with Routed Design

XACT Macro Library

General		CLBs
GADD	Adder	1
GCOMP	Compare	1
GEQGT	Equal or Greater	1
GMAJ	Majority	1
GMux	2-to-1 Mux	1
GPAR	Parity	1
GXOR	Exclusive-OR	1
GXOR2	Dual Exclusive-OR	1
GXTL	Crystal Oscillator	0 + 2IOB
GOSC	Low Frequency Resistor-Capacitor Oscilator	1 + 2IOB

Pads		IOBs
PIN	Input Pad	1
PINQ	Input Pad with Storage	1
PIO	Input/Output Pad	1
PIOQ	Input/Output Pad with Input Storage	1
PIOC	Input/Output Pad with 'Open Collector'	1
PIOQC	Input/Output Pad with Input Storage, 'Open Collector'	1
POUT	Output Pad	1
POUTC	Output Pad with 'Open Collector'	1
POUTZ	Output Pad with 3-State Control	1
PREG	Output Pad with Input Storage	1

Latches		CLBs
LD	Data Latch	1
LC-rd	Data Latch with ResetDir	1
LC-sd	Data Latch with SetDir	1
LD-srd	Data Latch with SetDir, ResetDir	1
LDM	Data Latch with 2-Input Data Mux	1
LDM-rd	Data Latch with 2-Input Data Mux, ResetDir	1
LDM-sd	Data Latch with 2-Input Data Mux, SetDir	1

Flip-Flops		CLBs
FD	D Flip-Flop	1
FDR	D Flip-Flop with Reset	1
FDS	D Flip-Flop with Set	1
FD-rd	D Flip-Flop with ResetDir	1
FD-sd	D Flip-Flop with SetDir	1
FD-srd	D Flip-Flop with SetDir, ResetDir	1
FDC	D Flip-Flop with ClkEna	1
FDCR	D Flip-Flop with ClkEna, Reset	1
FDCS	D Flip-Flop with ClkEna, Set	1
FDM	D Flip-Flop 2-Input Data Mux	1
FDMR	D Flip-Flop 2-Input Data Mux, Reset	1
FDMS	D Flip-Flop 2-Input Data Mux, Set	1
FDM-rd	D Flip-Flop 2-Input Data Mux, ResetDir	1
FDM-sd	D Flip-Flop 2-Input Data Mux, SetDir	1
FSR	Set-Reset Flip-Flop with Set Dominate	1
FRS	Set-Reset Flip-Flop with Reset Dominate	1
FJK	J-K Flip Flop	1
FJKS	J-K Flip Flop with Synchronous Set	1
FJK-rd	J-K (Set-Reset) Flip Flop with ResetDir	1
FJK-sd	J-K (Set-Reset) Flip Flop with SetDir	1
FJK-srd	J-K (Set-Reset) Flip Flop with SetDir, ResetDir	1
FT0	Self Toggle Flip-Flop	1
FT0R	Self Toggle Flip-Flop with Reset	1
FT	Toggle Flip-Flop	1
FTP	Toggle Flip-Flop with ParEna	1
FTP-rd	Toggle Flip-Flop with ParEna, ResetDir	1
FTR	Toggle Flip-Flop with Reset	1
FTS	Toggle Flip-Flop with Set	1
FT2	2-Input Toggle Flip-Flop	1
FT2R	2-Input Toggle Flip-Flop with Reset	1

Decoders		CLBs
D2-4	1-of-4 Decoder	2
D2-4E	1-of-4 Decoder, with Ena	2
74-139	1-of-4 Single Decoder with Low Output, Ena	4
D3-8	1-of-8 Decoder	5
D3-8E	1-of-8 Decoder with Ena	6
74-138	1-of-8 Decoder with Enables, Low Output	7
74-42	1-of-10 Decoder with Low Output	8

Multiplexers		CLBs
M3-1	3-to-1 Mux	2
M3-1E	3-to-1 Mux with Ena	2
M4-1	4-to-1 Mux	3
M4-1E	4-to-1 Mux with Ena	3
74-352	4-to-1 Mux with Low Output, Ena	3
M8-1	8-to-1 Mux	7
M8-1E	8-to-1 Mux with Ena	7
74-151	8-to-1 Mux with Ena Complementary Outputs	7
74-152	8-to-1 Mux with Low Output	7

XACT Macro Library

Registers — CLBs

Data Registers

RD4	4-Bit Data Register	4
RD8	8-Bit Data Register	8
RE8CR	8-Bit Data Register with ClkEna, Reset	8

Serial to Parallel

RS4	4-Bit Shift Register	4
74-195	4-Bit Serial to Parallel Shift Register with ParEna, Reset	5
74-194	4-Bit Bidirectional Shift Register with ClkEna, ParEna, ResetDir	12
RS8	8-Bit Shift Register	8
RS8CR	8-Bit Shift Register with ClkEna, Reset	8
RS8PR	8-Bit Shift Register with ParEna, Reset	8
RS8R	8-Bit Shift Register with Reset	8
74-164	8-Bit Serial to Parallel Shift Register with ResetDir	8

Counters — CLBs

Modulo 2

C2BCR	1-Bit Binary Counters with ClkEna, Reset	1
C2BC-rd	1-Bit Binary Counters with ClkEna, ResetDir	1
C2BP	1-Bit Binary Counters with ParEna	1
C2BR	1-Bit Binary Counters with Reset	1
C2B-rd	1-Bit Binary Counters with ResetDir	1

Modulo 4

C4BCP	2-Bit Binary Counters with ClkEna, ParEna	3
C4BCR	2-Bit Binary Counters with ClkEna, Reset	2
C4BC-rd	2-Bit Binary Counters with ClkEna, ResetDir	2
C4JCR	2-Bit Johnson Counters with ClkEna, Reset	2

Modulo 6

C6JCR	3-Bit Johnson Counter with ClkEna, Reset	3

Modulo 8

C8BCP	3-Bit Binary Counters with ClkEna, ParEna	5
C8BCR	3-Bit Binary Counters with ClkEna, Reset	4
C8BC-rd	3-Bit Binary Counters with ClkEna, ResetDir	4
C8JCR	3-Bit Johnson Counters with ClkEna, Reset	4

Modulo 10

C10BC-rd	4-Bit BCD Counter with ClkEna, ResetDir	4
C10BCP-rd	4-Bit BCD Counter with ClkEna, ParEna, ResetDir	7
74-160	4-Bit BCD Counter with ClkEna, ParEna, ResetDir	8
C10BP-rd	4-Bit BCD Counter with ParEna, ResetDir	6
C10JCR	5-Bit Johnson Counter with ClkEna, Reset	5

Modulo 12

C12JCR	6-Bit Johnson Counter with ClkEna, Reset	6

Modulo 16

C16BA-rd	4-Bit Binary Ripple Counter with ResetDir	4
C16BC-rd	4-Bit Binary Counter with ClkEna, ResetDir	4
C16BCPR	4-Bit Binary Counter with ClkEna, ParEna, Reset	10
C16BCP-rd	4-Bit Binary Counter with ClkEna, ParEna, ResetDir	6
74-161	4-Bit Binary Counter with ResetDir	8
C16BP-rd	4-Bit Binary Counter with ParEna, ResetDir	5
C16BUD-rd	4-Bit Binary Up-Down Counter with ParEna, ResetDir	8
C16JCR	8-Bit Johnson Counter with ClkEna, Reset	8

Modulo 256

C256FC-rd	8-Bit Modulo 256 Feedback Shift Register with ClkEna, ResetDir	9

LCA-MDS22 P-SILOS Simulator

Features

- **Event-driven logic and timing simulator**
- **Logic network input automatically generated by XACT Design Editor**
- **Control and observation of any physical circuit node**
- **Multiple file input for vectors and commands**
- **Interactive or batch mode operation**
- **Output available in printed or tabular formats**
- **Runs on an IBM PC-XT, PC-AT or compatible personal computer**

General

P-SILOS is a powerful PC-based simulator that provides event-driven logic and timing simulation of Logic Cell Array designs. Simulation is particularly useful for testing logic or logic segments as well as for verifying critical timing over worst case power supply, temperature and process conditions.

Simulation is useful in several stages of the design cycle. After design entry, simulation may be used to debug logic in an unplaced and unrouted design. This saves design time because logic errors can be detected and corrected prior to final placement and routing. After a circuit has been placed, routed, and then fully debugged using in-circuit emulation, worst case timing may be verified. This enables the user to select the correct Logic Cell Array speed for a particular application.

Network inputs for Logic Cell Array designs are automatically created by the Simgen utility in the XACT system. The network includes logic and routing delay parameters and setup and hold times based upon the selected speed grade operating under worst case conditions. Simulation stimuli are created with a set of clock statements or with an input pattern for either pad inputs or internal nodes. Simulation results are available in tabular, plotted, and graphic formats. This flexibility makes debugging easy for both the circuit function and timing.

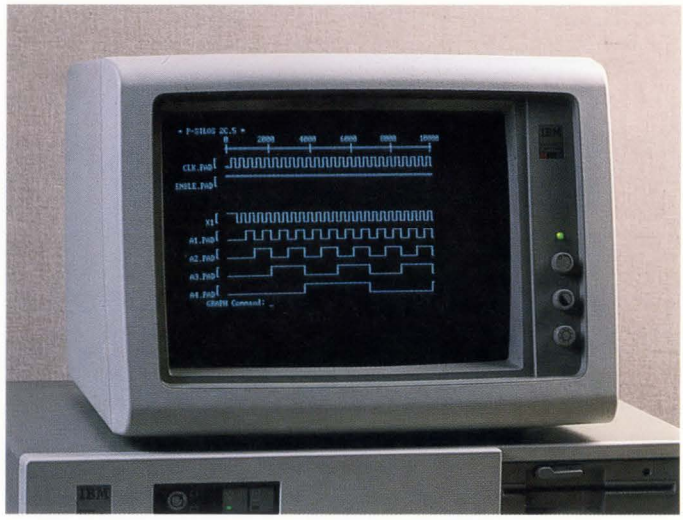
System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer with:

- MS-DOS 2.1 or higher
- 640 K Bytes RAM
- 1 Diskette Drive
- 10-MB Hard Disk
- 1 Parallel Interface Port

Refer to the MDS21 XACT Design Editor Product Datasheet for additional equipment required for systems which will also run the XACT Design Editor.



P-SILOS Waveform Output

LCA-MDS23 Automatic Placement and Routing Program

Features

- **Automatic placement and routing of logic to minimize design cycle time**
- **User control over placement of logic blocks**
- **User specification of critical paths**
- **Netlist inputs from either schematic capture or XACT**
- **May be used in conjunction with schematic capture or with the XACT Design Editor**
- **Runs on IBM PC-XT, PC-AT or compatible personal computer**

General

The automatic Placement and Routing program enhances the productivity of designers using Logic Cell Arrays by reducing design placement and routing time, whether the design logic is entered from a schematic capture package or from the XACT Design Editor.

Designs that are developed incrementally can also take advantage of Automatic Placement and Routing. Partial Logic Cell Array layouts can be locked in place while additions to the design are automatically placed and routed, or the design can be completely rearranged to yield a new placement.

The Automatic Placement and Routing program is extremely flexible. Through placement directives the user can control the placement process to achieve the best placement for a particular design. Routing resources can be specified to minimize clock skews and signal delays for critical paths. The result is faster product developement.

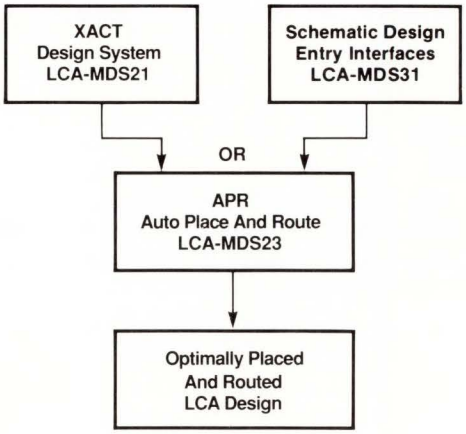
System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer with:

- MS-DOS 2.1 or higher
- 640 K Bytes RAM
- 1 Diskette Drive
- 10-MB Hard Disk
- 1 Parallel Interface Port

Refer to the MDS21 XACT Design Editor Product Datasheet for additional equipment required for systems which will also run the XACT Design Editor.



APR Diagram

LCA-MDS31 FutureNet DASH Schematic Design Entry Interface

Features

- **Design entry to XACT via the FutureNet DASH Schematic Designer**
- **Macro library of over 100 standard logic family equivalents derived from the XACT Macro Library**
- **Library of logic symbols including all two-input, three-input, and four-input AND, OR, and XOR gates plus storage, input/output, and clock elements**
- **User control for flagging critical paths for the LCA-MDS23 Automatic Placement and Routing Program**
- **Automatic partitioning and conversion of schematic drawings to a Monolithic Memories' Logic Cell Array design file**
- **Output compatibility with XACT Design Editor and the Automatic Placement and Routing Program**
- **Runs on an IBM PC-XT, PC-AT or compatible personal computer**

General

Schematic entry and automatic partitioning of Logic Cell Array designs shortens product development times. Complex designs can be specified schematically and quickly implemented for in-circuit design verification.

Monolithic Memories FutureNet DASH Schematic Design Entry Interface provides the symbol library and conversion utility to permit designers to enter Logic Cell Array designs with the FutureNet DASH Schematic Designer. The Monolithic Memories module provides the logic, I/O and macro symbols to be used in the schematic and a conversion utility which automatically partitions and translates the schematic into a Logic Cell Array design.

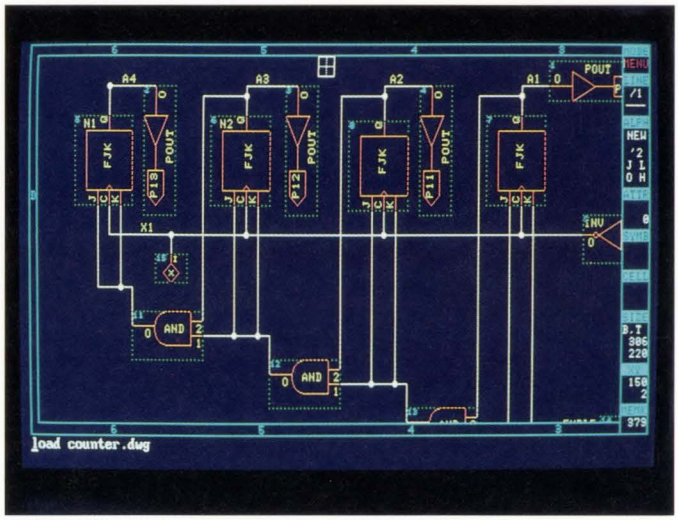
System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer with:

- FutureNet DASH-2 or later, and associated hardware including mouse, Enhanced Graphics Adapter and Display
- MS-DOS 2.1 or higher
- 640 K Bytes RAM
- 1 Diskette Drive
- 10-MB Hard Disk

Refer to the MDS21 XACT Design Editor Product Datasheet for additional equipment required for systems which will also run the XACT Design Editor.



Schematic Capture

LCA-MDS24, LCA-MDS26, LCA-MDS27 XACTOR In-Circuit Emulator

Features

- **Real-time in-circuit emulation in user's target system**
- **Concurrent emulation of up to four devices**
- **Readback and display of Logic Cell Array internal storage element states**
- **Device status display with automatic update of asynchronous events**
- **Control and I/O pin isolation from target system**
- **Support for daisy chain programming of up to seven devices in a daisy chain**
- **On-chip crystal oscillator support during emulation**
- **Support for multiple device and package types**
- **Runs on an IBM PC-XT, PC-AT or compatible personal computer**

General

The XACTOR real-time in-circuit emulator provides interactive target-system emulation of up to four Logic Cell Arrays from the host PC system. In-circuit emulation provides a powerful productivity enhancement to simulation, providing capabilities to verify functionality in the target system at full speed with all other circuits and system software.

The emulation system is composed of a microcomputer-based controller (LCA-MDS24), and from one to four universal emulation pods (LCA-MDS26), each with a package-specific emulation header (LCA-MDS27). One universal emulation pod is included with the system. The controller is connected to the host PC through a serial port and provides local storage of configuration programs, control of individual device configurations and control of the isolation of the pod device(s) from the target system. The user can set the state and isolation for each of the control signals to provide debugging of target hardware. Four general I/O pins are available to provide test points which may also be isolated from the target system.

Target Logic Cell Arrays can be programmed individually or in a daisy chain. Daisy chains of up to seven devices may be supported from any of the four pods. Individual device isolation and configuration is controlled with mouse or keyboard commands and may be supplemented with user-defined setup files for easy system debugging.

Readback of device configuration may be performed on command for verification of the configuration process and interrogation of the internal states. The state of all internal storage elements is displayed after readback has been performed. Status displays showing the state of all isolation switches and control signal states are provided. The status display includes automatic reporting of asynchronous status changes in the target system.

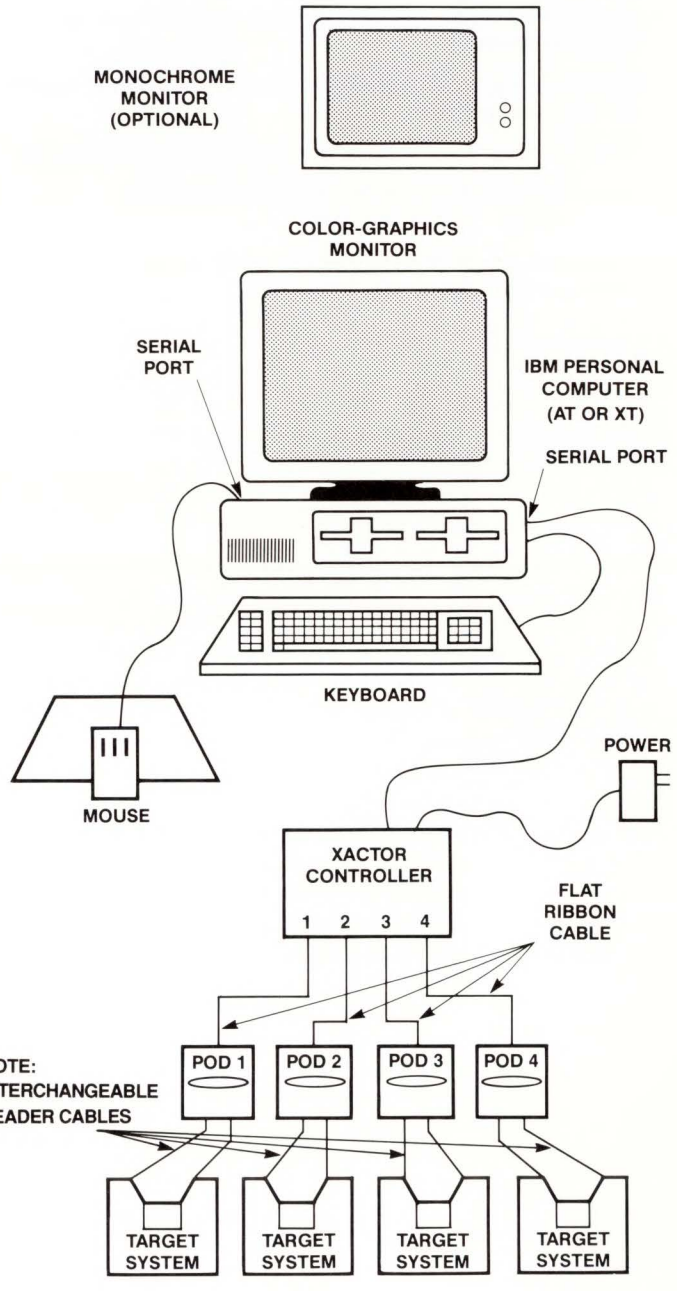
Universal In-Circuit Emulator Pod (LCA-MDS26)

Additional pods may be connected to the XACTOR in-circuit emulator controller, up to a maximum of four pods per controller. Pod headers (LCA-MDS27) are interchangeable for different device and package types. Each pod provides a direct in-socket connection for a minimum disruption of the target system. Test points are provided to allow connection of a logic analyzer or other test equipment to aid in the system debugging.

System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer as configured for MDS21 XACT Design Editor, plus second serial interface port.



XACTOR Hardware

LCA-MEK01 Logic Cell Array Evaluation Kit

The Monolithic Memories Logic Cell Array is a high-performance CMOS user-programmable gate array. The Monolithic Memories' Logic Cell Array Evaluation Kit is a software package that provides the capability to evaluate the Logic Cell Array for new applications.

Features

- **Design software package for IBM PC-XT, PC-AT or compatible computer**
- **Interactive graphics-oriented designer interface**
- **Simplified definition, placement and connection capability for implementation of complex logic**
- **Boolean equation or Karnaugh map alternatives to specify logic functions**
- **Macro library of 113 standard logic equivalents plus support for user-defined macros**
- **Point-to-point timing calculations for critical path analysis**
- **Automatic checking for connectivity and design consistency**
- **Hardcopy output of logical and physical configuration information**

General

The Evaluation Kit can be used to enter complete designs using a subset of the XACT design editor, including the use of the Monolithic Memories macro library. Critical timing for the design can be evaluated with the timing delay calculator to evaluate the applicability of the Logic Cell Array technology to a particular design.

Functional definition of Configurable Logic Blocks (CLBs), and their internal routing,I/O Block (IOB) definitions, and interconnection are all done within an integrated graphics-oriented system. Interactive placement and automatic routing of logic and I/O elements are accomplished quickly and easily via an easy-to-learn user interface.

Designs are captured with a graphics-oriented design editor, using either a mouse or keyboard entry, driven from command or files. User functions are specified in terms of CLB definitions and interconnections. Standard logic functions from the macro library or user-defined macro capabilities can be utilized to quickly implement complex logic functions. Placement and routing can be edited easily to modify or optimize a design.

Checking of logical connectivity is performed automatically. All unused internal nodes are automatically configured to minimize power dissipation.

Interactive point-to-point timing delay calculation is provided to simplify timing analysis and critical path determination.

The Evaluation Kit includes hardcopy generation to document a design and automatically track design changes.

System Requirements

Minimum System Configuration

IBM PC-XT, PC-AT or compatible computer with:

- MS-DOS 2.1 or higher
- 640K Bytes RAM
- 1 Diskette Drive
- 10-MB Hard Disk
- IBM or compatible Color Graphic Adapter and Display
- 1 Serial Interface Port
- Mouse Systems, Microsoft or compatible mouse

Evaluation Kit

Minimum Requirements of Software and Hardware Configurations for Monolithic Memories LCA Design System

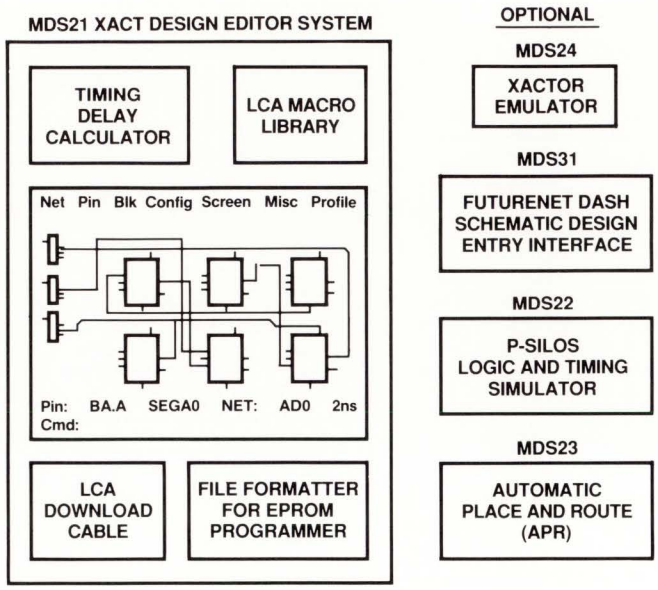
Legend R Required S Supported — Not required or supported		Software Package											
		XACT DESIGN EDITOR LCA-MDS21		XACT EVALUATION KIT LCA-MEK01		P-SILOS SIMULATOR LCA-MDS22		AUTOMATIC PLACEMENT AND ROUTING LCA-MDS23	FutureNet DASH SCHEMATIC DESIGN ENTRY INTERFACE LCA-MDS31			XACTOR IN-CIRCUIT EMULATOR LCA-MDS24	
		Version 1.30		Version 1.30		Version 1U.3	Version 2C.5	Version 1.0	Version 1.00**			1.10	1.30 1.33*
		Version 1.2		Version 1.2					DASH 2	DASH 3C	DASH 4		
XACT Version Required						Version 1.2	Version 1.2 or 1.3	Version 1.3	Version 1.3			Version 1.2	Version 1.3
MS-DOS PC-DOS Operating System		Version 2.1 or above	Version 2.1 or above	Version 2.1 or above	Version 2.1 or above	Version 2.1 or above	Version 2.1 or above	Version 2.1 or above	Version 2.1 or above			Version 2.1 or above	Version 2.1 or above
Logic Cell Arrays Supported		M2064 (8x8) only	M2064 (8x8) and M2018 (10x10)	M2064 (8x8) only	M2064 (8x8) and M2018 (10x10)	M2064 (8x8) only	M2064 (8x8) and M2018 (10x10)	M2064 (8x8) and M2018 (10x10)	M2064 (8x8) and M2018 (10x10)			M2064 (8x8) 68NL only	M2064* (8x8) and M2018 (10x10)
IBM PC XT or 100% compatible		R	R	R	R	R	R	R	R			R	R
IBM PC AT or 100% compatible		S	S	S	S	S	S	S	S			S	S
Memory	Minimum System RAM	640 KB	1 MB	640 KB	1 MB	640 KB	640 KB	640 KB	256 KB	512 KB	512 KB	640 KB	1 MB
	Hard Disk (10 MB min 30 MB REC)	R	R	R	R	R	R	R	R	R	R	R	R
Graphics Boards and Displays	Monochrome	—	—	—	—	R	R	—	R	—	—	—	—
	CGA (Color graphics adapter)	R	R	R	R	S	S	R	—	—	—	R	R
	EGA (Enhanced color graphics adapter)	S	S	S	S	S	S	S	—	R (with 192 KB)	R (with 192 KB)	S	S
	Lotus/Intel EMS (Expanded memory specifications)	—	R (with 256 KB)	—	R (with 256 KB)	—	—	—	—	—	—	—	R (with 256 KB)
	Vendor graphics board								Future-Net graphics controller board				
Other Devices	Security key	R	R	—	—	R	R	R	—	—	—	R	R
	Mouse	R†	R†	R†	R†	—	—	—	R (Future-Net)	R (Future-Net)	R (Future-Net)	R†	R†
	Min. number of parallel ports	1	1	1	1	1	1	1	1	Future-Net mouse/ parallel port board	Future-Net mouse/ parallel port board	1	1
	Min. number of serial ports	1	1	1	1	0	0	0	0	0	0	2	2

* XACTOR Version 1.33 supports the universal emulator pod with interchangeable header cables for each package type. Versions 1.10 and 1.30 or XACTOR support only the dedicated 68-Pin PLCC emulation pod originaly offered with XACTOR Version 1.10. XACTOR Version 1.33 will also support the original 68-Pin PLCC Emulator Pod.

** LCA-MDS31 FutureNet DASH Schematic Design Entry Interface version 1.00 is compatible with FutureNet DASH Schematic Designer versions 2, 3C and 4.

† Must be Mouse Systems™, FutureNet® or Microsoft® mouse compatible.

Logic Cell Array



Development System

The DS21 XACT Design Editor provides all capabilities required for Logic Cell Array design. Additional development system options provide enhanced designer productivity during design entry, placement and routing, and design verification.

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